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Arm Inductance and Sub-module Capacitance Selection in Modular Multilevel Converter

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To the Graduate Council:

I am submitting herewith a thesis written by Yalong Li entitled "Arm Inductance and Sub-module Capacitance Selection in Modular Multilevel Converter." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

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Arm Inductance and Sub-module Capacitance Selection in Modular Multilevel Converter

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Abstract

Arm inductor and sub-module (SM) capacitor are two key components in the modular multilevel converter (MMC). Optimizing the selection of arm inductance and sub-module capacitance is thus critical for the converter design. This report aims at developing a selection principle for arm inductance and sub-module capacitance in MMC.

Arm inductors in MMC are used to limit the circulating current which flows within the converter. The switching frequency harmonic is found to be the dominant component in the circulating current when an active circulating current suppressing controller is implemented. The analytical relationship between the arm inductance and switching frequency circulating current is derived, based on which the arm inductance requirement is obtained by limiting the circulating current to meet the defined specifications. In some applications, the arm inductors can also be used to limit the overcurrent during a dc side short circuit fault. The relationship between the arm inductance and fault current is investigated, as well as its impact on arm inductance selection.

The sub-module capacitance in MMC is selected mainly based on the capacitor voltage fluctuation constrain. The voltage unbalance among sub-module capacitors is revealed to have a significant impact on the sub-module capacitance selection, as the unbalanced voltage would increase the total capacitor voltage fluctuation. The impact of

sub-module capacitors' unbalanced voltage on the total voltage fluctuation is evaluated. An analytical expression of the unbalanced voltage is derived; it can be used to calculate the maximum capacitor voltage fluctuation, and thus used for the sub-module capacitance selection.

A simulation has been carried out in the MATLAB, and the simulation results verify the theoretical analysis. A scaled-down MMC prototype has been built, and the experimental results validate part of the analysis.

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Chapter 1 Introduction

This chapter starts with an introduction to the background of modular multilevel converter (MMC). Some main characteristics of MMC and the state-of-art research activities are reviewed. The objectives of the thesis are then discussed, and the structure and organization of the thesis are presented.

1.1 Research background

The ever increasing demand for energy resources, such as renewable energy resources in remote locations, requires a strong high voltage electric power transmission system [1]. Dc grid concept has been proposed for its superior system performance in some of these applications. The high voltage direct current (HVDC) grid, linking more than two interfacing converters to form a meshed dc system, would have several advantages compared with the traditional two-terminal point-to-point HVDC transmission: fewer interfacing converters allows for reduced cost and loss, and the outage of one dc line does not interrupt the power flow at other terminals [2]-[5].

The voltage source converter (VSC) based HVDC transmission system is considered a more suitable system architecture for the future meshed dc grid or multi-terminal HVDC transmission system. Compared with the traditional thyristor-based line-commutated converter (LCC), VSC has the advantages of smaller size of converter site, smaller filters, fast active power reversal, inherent dynamic reactive power support, and VSC also has the possibility to use extruded polymeric cable system [6]-[8].

The use of VSC for HVDC transmission systems was first pioneered over 15 years ago. Traditional two-level converter and three-level neutral-point diode-clamped converter topologies were used originally. Recently, the MMC emerges as a better candidate due to the following advantages [9]-[10]:

1) No direct series of power switches;
2) Much reduced slope (di/dt) of the arm currents and thus reduced high frequency noise;
3) Lower switching frequency and as a result of lower power loss;
4) Less requirement on ac filters;
5) Distributed locations of capacitive energy storages;
6) Inherent redundancy for sub-module failure management;

Among them, it is the multilevel construction enabling the advantages of 1 to 4. While, compared to the traditional multilevel converter, like the diode-clamped multilevel converter and flying capacitor multilevel converter, the modular structure brings the advantages of easy assembly and flexibility in converter design. Furthermore, the capacitor voltage balance issue is much relieved in MMC. Thus MMC becomes the most popular converter topology for HVDC transmission systems, and has already been used in the commercial industry products like Siemens “HVDC plus” and ABB “HVDC light”.

Except for the HVDC applications, it has been evaluated that MMC is also attractive for applications like static synchronous compensator (STATCOM), electric

railway supplies and medium-voltage motor drives. Related research works are presented in [11]-[13].

MMC was first introduced by Marquart and Lesnicar in 2003 [14], and since then several research activities have been carried out focusing on the modulation [15]-[21], control [22]-[27], modeling [28]-[33], design [34]-[38] and protection [39]-[44]. For converter design, even though the arm inductor and sub-module capacitor are essential for the operation of MMC, only a few papers have discussed the design of arm inductance and sub-module capacitance. References [34]-[36] have discussed the arm inductance selection. In [34], the arm inductance selection principle based on limiting the circulating current is proposed. It is also proposed in [35], that the arm inductance selection should consider its impact on limiting the dc short circuit fault current. References [37]-[38] present a work on sub-module capacitance selection. The main selection principle is based on the capacitor voltage fluctuation constrain.

1.2 Thesis objective

This thesis aims at investigating selection criteria for arm inductance and sub-module capacitance in MMC. As discussed in 1.1, some related works have been published in literature. A selection criterion of arm inductance based on limiting the circulating current is developed in [34]. However, the circulating current suppressing control is not considered. Since the implementation of suppressing control can largely reduce the circulating current [45]-[46], the requirement on the arm inductance is changed. Thus the selection criterion in [34] is a much conservative method considering

the circulating current suppressing control. Furthermore, the impact of the arm inductor on limiting the dc side short circuit fault current is not fully explained in [34]-[35].

In [37], the sub-module capacitance selection principle is proposed based on the capacitor voltage fluctuation constrain. The relationship between sub-module capacitance and the steady-state capacitor voltage ripple is derived in [47]. However, the derivation is based on the assumption that all the sub-module capacitor voltages are the same. In practice, the sub-module capacitor voltage unbalance issue could be significant in some applications which will influence the capacitance selection. Thus a better sub-module capacitance selection criterion in MMC should consider the impact of the voltage unbalance.

Based on the state-of-art techniques on arm inductance and sub-module capacitance selection, the main objectives of the research in this thesis are:

1) Develop the arm inductance selection criterion based on limiting the circulating current when the circulating current suppressing control is implemented;
2) Fully understand the arm inductance requirement for limiting the dc side short circuit fault current;
3) Develop the sub-module capacitance selection principle considering the sub-module capacitor voltage unbalance.

1.3 Organization of the thesis

The chapters of this thesis are organized as follows:

Chapter 2 introduces some foundations of MMC as the preparation for the analysis. The basic concept of MMC and its operating principle will first be explained. The modulation method and voltage-balancing control considered in this thesis are also briefly introduced. Then, the definition of operation conditions is presented.

Chapter 3 investigates the arm inductance selection principle. The switching frequency harmonic is proposed to replace the second-order harmonic as the dominant component of circulating current when the circulating current suppressing control is implemented. The relationship between the arm inductance and switching frequency circulating current is then derived. The fault analysis of the dc side short circuit fault is conducted, based on which the impact of arm inductor on limiting the fault current is analyzed.

Chapter 4 studies the sub-module capacitance design. The impact of sub-module capacitors' unbalanced voltage on the sub-module capacitor voltage fluctuation is first explored. The analytical expression of the unbalanced voltage is then derived. The impact of switching frequency on the sub-module capacitance selection is further discussed.

Chapter 5 presents the hardware design of a down-scaled MMC prototype.

Chapter 6 summarizes the conclusions of the thesis, and proposes some future work.

Chapter 2 Foundation of the Analysis

This chapter presents the necessary preparation for the analysis in the following chapters. The basic operating principle of MMC is presented, as well as an overview of the modulation schemes and voltage-balancing control. The variables and parameters are defined in the last part of this chapter.

2.1 Basic operating principle

Figure 2-1 shows the basic structure of the MMC. A three-phase MMC consists of six arms. Each arm is a series connection of sub-modules and an arm inductor. There are several different sub-module topologies proposed in the literature [10], shown in Figure 2-2. The most popular one is the half-bridge circuit including two power switches and a dc capacitor. The other three topologies are also based the half-bridge circuit, and the operating principles during normal conditions are nearly the same. The main difference of these four topologies is the performance during fault conditions. In this thesis, the half-bridge sub-module is considered for the analysis.

Figure 2-3 shows the four possible switching states for sub-module. (a) and (b) show the "inserted" state when the upper IGBT is switched on and the lower IGBT is switched off; (c) and (d) show the "bypassed" state when the upper IGBT is switched off and the lower IGBT is switched on. When sub-module is at "inserted" state, the sub-module voltage of v_{sm} (defined as the output voltage of the sub-module) is equal to the capacitor voltage of v_c; when the sub-module is at "bypassed" mode, sub-module voltage is then equal to zero.

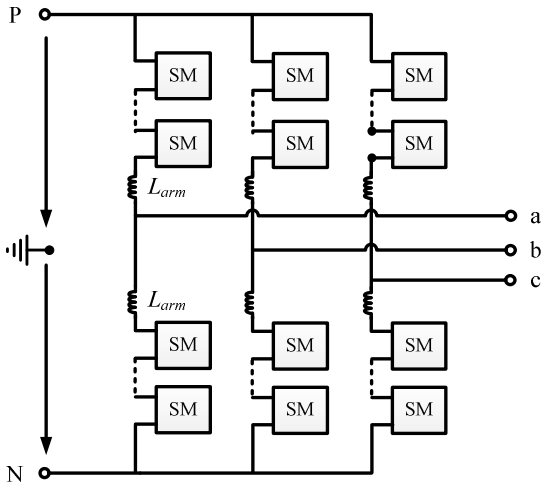


Figure 2-1. Basic structure of MMC

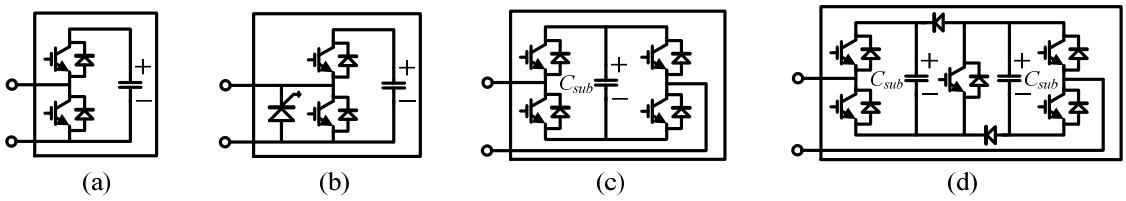


Figure 2-2. Different sub-module topologies: (a) half-bridge circuit, (b) half-bridge circuit with bypass thyristor, (c) full-bridge circuit, and (d) clamped double half-bridge circuit

Therefore, by controlling the number of inserted sub-modules in each arm, the converter arm voltage is determined. Figure 2-4 shows an equivalent circuit of MMC for a single phase (*a* phase for example), where the series connection of sub-modules is represented by a controllable voltage source. The relationship between the ac side phase voltage and the dc side voltage can be expressed as:

$$v_a = \frac{v_{dc}}{2} - v_{ap} - L_{arm}\frac{di_{ap}}{dt} \tag{2-1}$$

$$v_a = -\frac{v_{dc}}{2} + v_{an} + L_{arm}\frac{di_{an}}{dt} \tag{2-2}$$

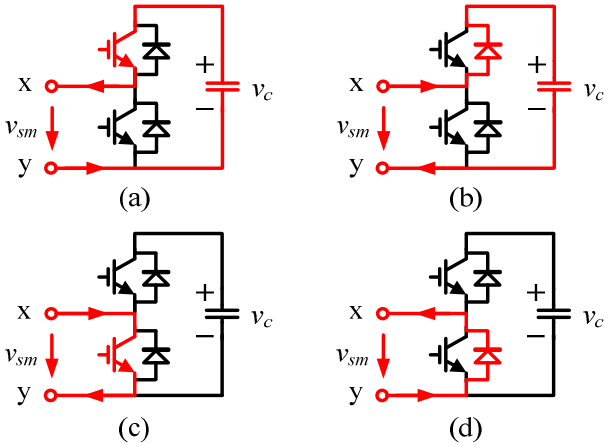


Figure 2-3. Four switching states of sub-module: (a) upper IGBT is conducting, (b) upper diode is conducting, (c) lower IGBT is conducting, and (d) lower diode is conducting

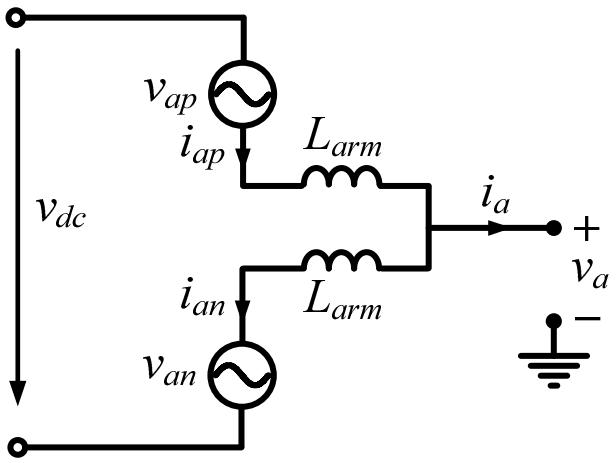


Figure 2-4. Equivalent circuit of MMC for a single phase

Adding (2-1) to (2-2), the phase voltage can be obtained as:

$$v_a = \frac{v_{an} - v_{ap}}{2} - \frac{L_{arm}}{2}\frac{di_a}{dt} \tag{2-3}$$

Subtracting (2-1) by (2-2) yields

$$v_{dc} = v_{ap} + v_{an} + 2L_{arm}\frac{di_{cm}}{dt} \tag{2-4}$$

where i_{cm} is defined as:

$$i_{cm} = \frac{i_{ap} + i_{an}}{2} \tag{2-5}$$

Eq. (2-3) and (2-4) show that by controlling the converter arm voltages, the desired sinusoidal voltage at the ac terminal for inverter operation or the constant voltage at the dc terminal for rectifier operation can be achieved. This is the basic operating principle of MMC.

As arm inductors do not have an impact on the basic operation of MMC, the reference for arm voltages can be obtained based on (2-3) and (2-4):

$$v_{ap} = \frac{v_{dc}}{2} - v_a \tag{2-6}$$

$$v_{an} = \frac{v_{dc}}{2} + v_a \tag{2-7}$$

The sub-module capacitors in MMC are intended to work as constant voltage sources. Thus the number of inserted sub-modules can be derived as:

$$N_{ap} = \frac{v_{ap}}{v_c} \tag{2-8}$$

$$N_{ap} = \frac{v_{an}}{v_c} \tag{2-9}$$

2.2 Modulation schemes and voltage-balancing control

Eq. (2-6) and (2-7) give the reference for arm voltages. In order to achieve the desired arm voltage, the modulation is then required to generate the pulses for each device. Many modulation schemes have been introduced in the literature. Among them, the carrier-based phase-shifted modulation and direct modulation with active selection method are the two most popular ones.

1) Carrier-based phase-shifted modulation

This modulation scheme has already been widely used in the cascaded multilevel converters. As explained in [18], each sub-module has the same reference waveform, but the corresponding carrier waveform has a phase difference of $2\pi/N$ (N is the number of sub-modules per arm) to each other. The pulses for the two devices in each sub-module are complementary. The illustration of this modulation is shown in Figure 2-5. One advantage of the phase-shifted modulation is its simplicity for implementation.

The reference waveform is obtained based on the insertion index (the ratio of inserted sub-module numbers to the whole sub-module numbers per arm).

$$n_{ap} = \frac{N_{ap}}{N} = \frac{v_{ap}}{N \cdot v_c} \tag{2-10}$$

$$n_{an} = \frac{N_{an}}{N} = \frac{v_{an}}{N \cdot v_c} \tag{2-11}$$

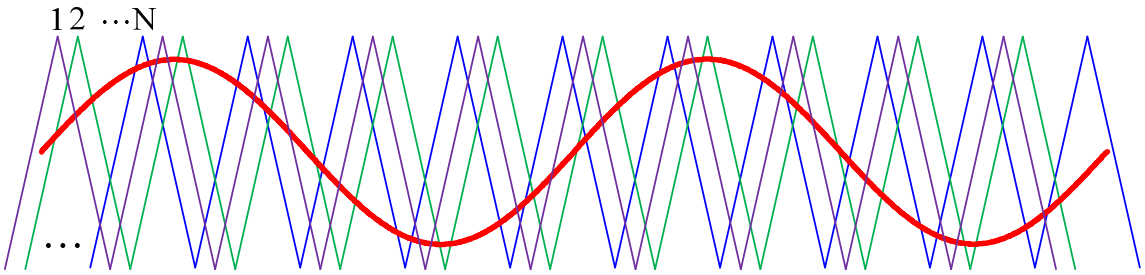


Figure 2-5. Carrier-based phase-shifted modulation

As the carriers are phase shifted to each other, the switching state for each sub-module is different to each other. Since arm current flows through the sub-module capacitor only when the sub-module is at inserted mode, the currents of sub-module capacitors are thus different from each other. As a result, the voltages of sub-module capacitors are different. Because the sub-module capacitor voltages are assumed the same for obtaining the insertion indices in (2-10) and (2-11), the voltage unbalance among sub-module capacitors would deteriorate the normal operation of MMC. Thus, voltage-balancing control is required for this modulation scheme.

In [19], a voltage-balancing control including averaging control, individual-balancing control and arm-balancing control has been proposed for the phase-shifted modulation scheme. The validity of this control method has been verified by the simulation and experimental results in [19].

2) Direct modulation with active selection method

In this modulation scheme, a dynamic assignment of the switching states of the sub-modules is adopted. Eq. (2-8) and (2-9) show the number of inserted sub-modules in

each arm; but they cannot indicate which individual sub-module should be inserted or bypassed. The inserted sub-modules are then actively selected based on the voltage-balancing control algorithm.

As the number of inserted sub-modules in (2-8) and (2-9) might not be an integer, pulse-width modulation (PWM) would be applied for one sub-module (defined as the PWM sub-module) during each control cycle while other sub-modules are either inserted or bypassed for the whole control cycle. Therefore, the number of inserted sub-modules and the duty cycle of the PWM sub-module can be expressed as (upper arm for example):

$$N_{ap\_real} = \lfloor N_{ap} \rfloor \tag{2-12}$$

$$D_{ap\_real} = N_{ap} - \lfloor N_{ap} \rfloor \tag{2-13}$$

where $\lfloor x \rfloor$ stands for the floor function whose value is the largest integer that is not larger than x.

If the sub-module number in MMC is large, (2-8) and (2-9) can be approximated by integers. In that case, the PWM sub-module is no longer required. Therefore, the number of inserted sub-modules can be obtained as:

$$N_{ap\_real} = round(N_{ap}) \tag{2-14}$$

where $round(x)$ stands for the closest integer to x.

For the voltage-balancing control, the traditional sorting method proposed in [12] is the most popular one. The selection criteria are based on 1) capacitor voltages and 2) the sign of the arm currents. If the arm current is charging the sub-module capacitors, the sub-modules with the lowest capacitor voltages are selected to be inserted; on the other

hand, if the arm current is discharging the sub-module capacitors, the sub-modules with the highest capacitor voltages are selected to be inserted. With this selection algorithm, sub-module capacitor voltages can be well balanced.

A disadvantage of the above algorithm is the high switching frequency. A modified sorting method in [48] avoids the high switching frequency by setting an unbalanced voltage threshold. Switching operation is applied only when extra sub-modules are required to be inserted or bypassed. The selection criterion for the extra sub-module is the same as that in the traditional sorting algorithm. And if the maximum voltage difference among sub-module capacitors exceeds the threshold, an exchange of switching states for two sub-modules would be executed: a previous inserted sub-module with the highest or lowest capacitor voltage is selected to be bypassed, and a previous bypassed sub-module with lowest or highest capacitor voltage is selected to be inserted based on the arm current direction.

In the following part of the thesis, the modulation scheme with active selection method is considered.

2.3 Definition of operation conditions

In order to assist the following analysis, some voltages and currents need to be defined first. The directions of voltages and currents are shown in Figure 2-6.

The ac side phase voltage and current are defined (for *a* phase) as:

$$v_a = V_{ac}\cos(\omega t) \tag{2-15}$$

$$i_a = I_{ac}\,cos(\omega t + \theta) \tag{2-16}$$

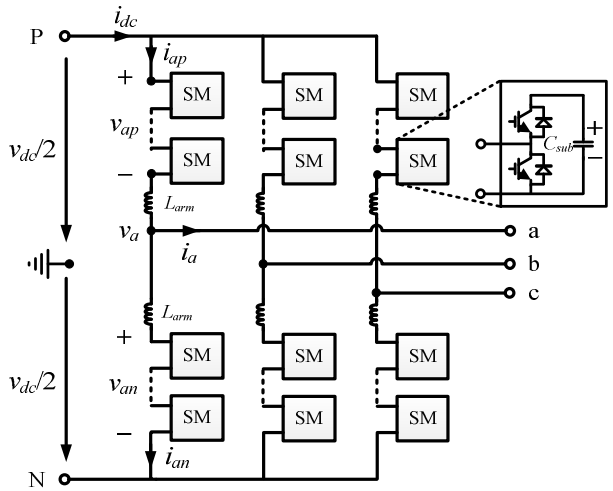


Figure 2-6. Voltage and current definition in MMC

where θ represents the phase angle between voltage and current. The arm voltages can thus be expressed as:

$$v_{ap} = \frac{v_{dc}}{2}(1 - M\,cos(\omega t)) \tag{2-17}$$

$$v_{an} = \frac{v_{dc}}{2}(1 + M\,cos(\omega t)) \tag{2-18}$$

where M is the modulation index defined as $2V_{ac}/v_{dc}$. Since N SMs are always inserted in the circuit, v_c in (2-10) and (2-11) can be assumed as:

$$v_c = \frac{V_{dc}}{N} \tag{2-19}$$

The insertion indices in (2-10) and (2-11) are rewritten as:

$$n_{ap} = \frac{1}{2} - \frac{1}{2}M\,cos(\omega t) \tag{2-20}$$

$$n_{an} = \frac{1}{2} + \frac{1}{2}M\,cos(\omega t) \tag{2-21}$$

Assuming a balanced three-phase condition, and the upper and lower arms in MMC are symmetrical, the arm currents can be expressed as:

$$i_{ap} = \frac{i_{dc}}{3} + \frac{I_{ac}}{2} cos(\omega t + \theta) + i_{cir} \tag{2-22}$$

$$i_{an} = \frac{i_{dc}}{3} - \frac{I_{ac}}{2} cos(\omega t + \theta) + i_{cir} \tag{2-23}$$

where i_{cir} represents the circulating current within the three phase-legs in the MMC.

It has been explained in 2.2 that the currents flowing through sub-module capacitors are different, but on average (instantaneous balanced sub-module capacitor voltage is assumed) the sub-module capacitor current can be obtained as:

$$i_{ap\_c} = n_{ap} \cdot i_{ap} \tag{2-24}$$

$$i_{an\_c} = n_{an} \cdot i_{an} \tag{2-25}$$

Based on the average model in [47], the average sub-module voltages are given as:

$$v_{ap\_sm} = n_{ap} \cdot v_{ap\_c} \tag{2-26}$$

$$v_{an\_sm} = n_{an} \cdot v_{an\_c} \tag{2-27}$$

where v_{ap_c} and v_{an_c} represent the sub-module capacitor voltages in upper arm and lower arm of *a* phase respectively.

Chapter 3 Arm Inductance Selection Principle

3.1 Introduction

The existence of arm inductors is one of the main characteristics of MMC. The arm inductor is in series with sub-modules in each arm. It is used to compensate for the voltage difference between the phase-leg voltage and dc side voltage. This voltage difference would as a result cause circulating current, and the arm inductance has a significant impact on the magnitude of the circulating current. In some applications, like HVDC transmission systems, the ac side of the MMC is connected to voltage sources. The arm inductor can be used to limit the fault current during dc side short circuit fault. Thus the arm inductance selection should first consider the circulating current constrain, and also consider the requirement for limiting dc short circuit fault current in some applications.

In [26], it is found that the second-order harmonic component dominates the circulating current. The relationship between the arm inductance and second-order circulating current is developed in [47], which can provide a selection criterion for the arm inductance based on the circulating current constrain. Several control methods (circulating current suppressing control) have then been proposed to actively reduce the circulating current in [45]-[46]. The effectiveness of these methods has been verified, with the circulating current being effectively reduced. Therefore, the arm inductance requirement is also reduced, and the previous arm inductance selection criterion is not suitable when the circulating current suppressing control is implemented. In this thesis,

the arm inductance selection criterion for MMC with a circulating current suppressing controller is investigated.

During a dc side short circuit fault, a large fault current is generated by the discharge of sub-module capacitors as well as fed by ac side voltage source. The fault current flows through the power devices (IGBT and anti-paralleled diode); and the converter would be destroyed if the fault current is not limited to a tolerant level. Reference [34] has explained that the arm inductor is a key component for limiting the fault current. In [34], the arm inductance requirement is proposed based on limiting the fault current rising rate for IGBT. Reference [36] investigates the impact of arm inductor on limiting the steady state fault current based on the fault analysis. In this thesis, a more detailed fault analysis will be conducted, and the arm inductance requirement is fully evaluated for limiting the fault current.

3.2 Arm inductance requirement for limiting circulating current

3.2.1 Circulating current suppressing control

The mechanism of the circulating current and circulating current suppressing control should be introduced first. The mechanism of second-order circulating current has been fully explained in [47], so a brief explanation is presented here.

It has been shown in (2-19) that the insertion indices are obtained based on an average sub-module capacitor voltage. The actual capacitor voltage contains alternating components. So by using the insertion indices in (2-20) and (2-21), the generated arm

voltages will not be equal to the desired arm voltages in (2-17) and (2-18). The generated arm voltages can be given as:

$$v_{ap\_real} = N\left(\frac{1}{2} - \frac{M}{2}cos(\omega t)\right) \cdot v_{ap\_c\_real} \tag{3-1}$$

$$v_{an\_real} = N\left(\frac{1}{2} + \frac{M}{2}cos(\omega t)\right) \cdot v_{an\_c\_real} \tag{3-2}$$

where $v_{ap\_c\_real}$, $v_{ap\_c\_real}$ are the actual sub-module capacitor voltages.

According to [47], the arm voltages can be described as:

$$v_{ap\_real} = \frac{v_{dc}}{2}(1 - M\,cos(\omega t)) + v_{cir} \tag{3-3}$$

$$v_{an\_real} = \frac{v_{dc}}{2}(1 + M\,cos(\omega t)) + v_{cir} \tag{3-4}$$

Compared to the desired arm voltages in (2-17) and (2-18), a common mode voltage is generated. Thus the phase-leg voltage will not be equal to the dc side voltage, and the voltage difference ($2v_{cir}$) is applied on the arm inductors, which causes the circulating current. The harmonics of the circulating current have been analyzed in [47], showing that the second-order harmonic is the dominant component.

In order to suppress this low frequency circulating current, several active methods have been proposed. The essential ideas of these methods are actually the same, and the circulating current suppressing controller introduced in [45] is considered in this thesis.

According to [45], a common mode component ($-v_{cm}$) is added to the arm voltage reference in (2-17) and (2-18) in order to compensate for the sub-module capacitor voltage variation. The insertion indices are thus changed to:

$$n_{ap\_real} = \frac{1}{2} - \frac{M}{2}cos(\omega t) - n_{cm} \tag{3-5}$$

$$n_{an\_real} = \frac{1}{2} + \frac{M}{2}cos(\omega t) - n_{cm} \tag{3-6}$$

where n_{cm} is the common mode component added to the insertion indices, and defined as $2v_{cm}/V_{dc}$. Using the above insertion indices, the generated arm voltages are given as:

$$v_{ap\_real} = N\left(\frac{1}{2} - \frac{M}{2}cos(\omega t) - n_{cm}\right) \cdot v_{ap\_c\_real} \tag{3-7}$$

$$v_{an\_real} = N\left(\frac{1}{2} + \frac{M}{2}cos(\omega t) - n_{cm}\right) \cdot v_{an\_c\_real} \tag{3-8}$$

Compared to (3-3) and (3-4), the arm voltage can be rewritten as:

$$v_{ap\_real} = \frac{v_{dc}}{2}(1 - M\,cos(\omega t)) + v_{cir} - n_{cm} \cdot v_{an\_c\_real} \tag{3-9}$$

$$v_{an\_real} = \frac{v_{dc}}{2}(1 + M\,cos(\omega t)) + v_{cir} - n_{cm} \cdot v_{an\_c\_real} \tag{3-10}$$

The phase-leg voltage is thus derived as

$$v_{a\_leg} = v_{dc} + 2v_{cir} - n_{cm} \cdot \left(v_{c\_up} + v_{c\_low}\right) \tag{3-11}$$

According to (3-11), the phase leg voltage can be controlled equal to the dc voltage by adjusting n_{cm}, which means the circulating current at the frequency below the bandwidth of the controller can be theoretically eliminated. As stated previously, second-order harmonic component dominates the circulating current, so the circulating current suppressing controller can effectively reduce the circulating current.

3.2.2 Switching frequency circulating current

Eq. (3-11) shows that the circulating current suppressing controller can effectively eliminate the second-order harmonic. But for a circulating current component at high

frequency like the switching frequency, which is out of the bandwidth of the controller, it can only be limited by the arm inductors. This section is intended to explain the mechanism of the switching frequency circulating current, and provides the guidance for arm inductance selection based on the circulating current.

The modulation scheme analyzed in this section includes the PWM sub-module. Figure 3-1 shows the pulse-width voltages generated for the PWM sub-modules. The reference voltages are compared with the triangular carriers to decide whether the sub-modules should be inserted or bypassed. The triangular carriers for the upper and lower arms are complementary. The reference voltages are actually the representation of the insertion indices. When circulating current suppressing control is not implemented, the sum of insertion indices for the upper and lower is unity based on (2-20) and (2-21), which means there are N sub-modules always inserted in one phase-leg. Thus the voltages of PWM sub-modules in the upper and lower arms are complementary. Based on (3-3) and (3-4), the resulting phase-leg voltage has an error of $2v_{cir}$ compared to the dc voltage reference. The phase-leg voltage difference between I, III and II represents the different sub-module capacitor voltages in the upper and lower arms.

With the circulating current suppressing controller, a common mode component is added into the insertion indices. The voltages of PWM sub-modules in the upper and lower arms are no longer complementary, but have an overlap as shown in Figure 3-1. Additional sub-modules would be inserted or bypassed in the circuit based on the sign of n_{cir} during the overlap period, which means it is no longer true that N sub-modules are

always inserted in the circuit for a phase-leg. So the phase-leg voltage has two pulses with magnitude of v_c in each switching period because of the circulating current suppressing control.

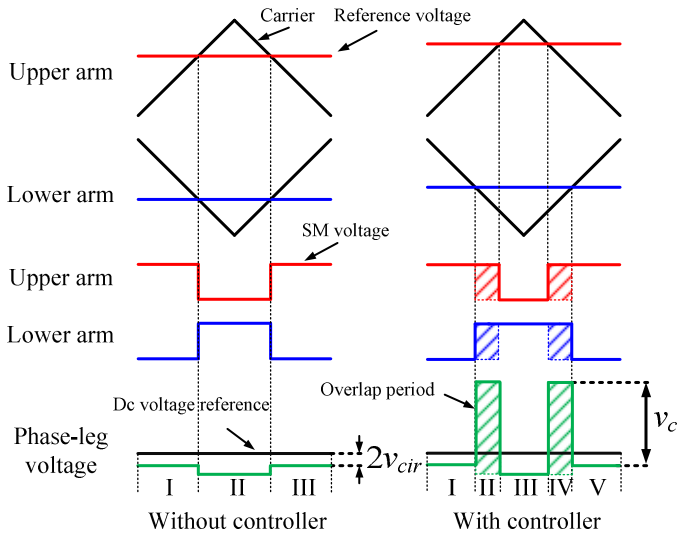


Figure 3-1. Voltage generation of PWM sub-modules

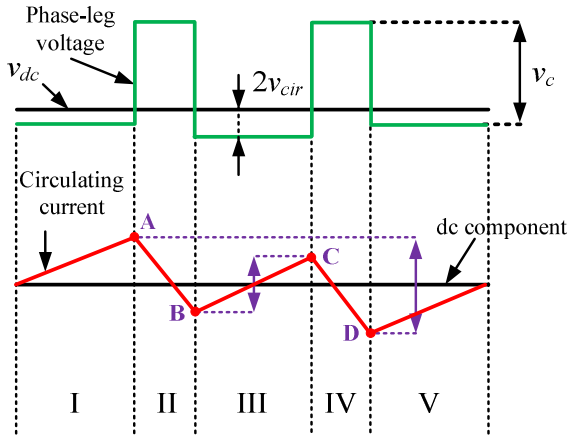


Figure 3-2. Phase-leg voltage and circulating current in a switching period

Based on the equivalent circuit in Figure 2-4, the voltage difference between the phase-leg voltage and dc side voltage is applied on the arm inductors. Figure 3-2 shows the resulting phase-leg voltage with the circulating current suppressing controller and the corresponding circulating current in one switching period. In Figure 3-2, a switching cycle is divided into 5 stages. Stages II and IV represent the overlap periods, and the phase-leg voltages in these two periods are v_c higher than the voltages in the other periods. The phase-leg voltages in stages I, III and V are nearly the same, with a small variation representing the capacitor voltages difference between the upper and lower arms. The voltage difference between $\mathrm{v_{dc}}$ and the phase-leg voltages in stages I, III and V is $2v_{cir}$, as shown in (6). If the circulating current suppressing controller is not implemented, the phase-leg voltages in stages II and IV would be the same as the other periods, and the circulating current would keep increasing or decreasing in the whole switching cycle, resulting in a second-order line frequency circulating current.

But with the circulating current suppressing controller, the voltages in stages II and IV can compensate for the voltage differences in the other three periods and make the average value of the phase-leg voltage in each switching cycle equal to v_{dc}. The second-order circulating current is thus eliminated, but the switching frequency circulating current comes out.

As shown in Figure 3-2, in order to calculate the switching frequency circulating current, the voltage difference between the phase-leg voltage and dc side voltage should be obtained. Based on [47], v_{cir} can be derived as:

$$v_{cir} = \frac{N}{8C_{sub}}\left\{-\frac{3}{4\omega}M \cdot I_{ac} \cdot \sin(2\omega t - \theta) + \frac{1}{3\omega}M^2 I_{dc} \cdot \sin(2\omega t)\right\} \quad (3\text{-}12)$$

where I_{dc} represent the dc component of dc side current. It is shown in Figure 3-2, the peak current would occur either at A and D, or at B and C, determined by the length of periods I, V, and III. Considering the overlap periods are relatively small, and the longest time period among I, V, and III can thus be derived as:

$$\Delta T = max(\, D_{ap\_real} \quad D_{an\_real}) \cdot T_s \quad (3\text{-}13)$$

where T_s is the switching period. Thus the peak to peak value of the switching frequency circulating current can be derived as

$$I_{pp} = \frac{v_{cir}}{L_{arm}} \cdot \Delta T \quad (3\text{-}14)$$

Eq. (3-14) presents the relationship between the arm inductance and switching frequency circulating current, so that the arm inductance can be selected to meet the circulating current limit for a given operating condition. However, the arm inductance should be selected to meet the circulating current limit for all different working conditions. Assuming the maximum modulation index is 1, the maximum v_{cir} can be derived as:

$$v_{cir\_max} = \frac{N}{8\omega C_{sub}}\sqrt{\frac{9}{16}I_{ac}^2 + \frac{1}{9}I_{dc}^2 - \frac{1}{2}I_{ac}I_{dc}} \quad (3\text{-}15)$$

As shown in Figure 3-2, the largest ΔT would be T_s. Thus the maximum switching frequency circulating current is obtained as:

$$I_{pp\_max} = \frac{N \cdot T_s}{8\omega L_{arm} C_{sub}} \sqrt{\frac{9}{16} I_{ac}^2 + \frac{1}{9} I_{dc}^2 - \frac{1}{2} I_{ac} I_{dc}} \tag{3-16}$$

It is shown in (3-16) that the switching frequency circulating current is dependent on the arm inductance and sub-module capacitance. The sub-module capacitance is mainly designed by its voltage ripple requirement, which will be presented in chapter 4. Then, the arm inductance requirement based on the switching frequency circulating current can be derived.

3.3 Arm inductance requirement for limiting DC short circuit fault current

In this section, the MMC based HVDC transmission systems are considered. For a dc short circuit fault, the pole-to-pole fault is the most severe case. A detailed analysis of the pole-to-pole fault is presented, and arm inductance selection criterion is discussed.

3.3.1 Fault analysis

Figure 3-3 shows a pole-to-pole fault occur at the terminal of the MMC. The definitions of the system parameters are the same as that in chapter 2, but the current direction definition is different. The following analysis divides the fault into several different stages and the corresponding equivalent circuits for each stage are shown in Figure 3-4. Figure 3-5 shows the analytical current waveform during the fault.

1) Stage 1: (t_0, t_1)

This stage starts at the time (t_0) when the fault occurs and ends at the time (t_1) when IGBTs are turned off. The duration of this stage is mainly determined by the fault detection time, pulse delay time and IGBT turn off time, usually at the range of several

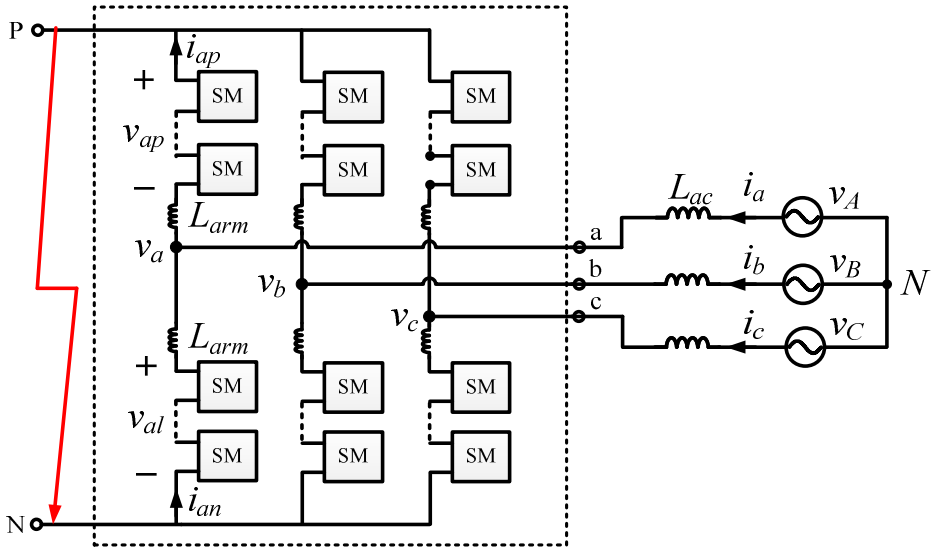


Figure 3-3. Pole to pole fault for a grid connected MMC

microseconds. The arm voltages can be assumed unchanged for such a short time. Thus, the phase-leg voltage (equal to v_{dc}) is all applied on the arm inductors, and i_{cir} (including dc component) increases rapidly. The ac terminal (for *a* phase) voltage can be obtained as:

$$v_a = \frac{v_{dc}}{2} - v_{ap} = -\frac{v_{dc}}{2} + v_{an} \tag{3-17}$$

It is shown that the ac terminal voltages remain the same. Thus ac current can be assumed constant for this stage. The equivalent circuit is shown in Figure 3-4 (a).

For this stage, the equivalent circuit can be considered as a shoot through of IGBTs with a large loop inductance (because of additional arm inductance). A larger loop inductance can increase the IGBT short circuit withstand time. However, if de-saturation protection is implemented, the IGBTs can still be protected even with a small loop

inductor. Thus, the arm inductance has a soft impact on the shoot through protection, and the selection of the arm inductance based on this stage is out of the scope for the thesis.

The current waveforms in Figure 3-5 are based on the linear approximation. The arm currents at t_1 can be expressed as:

$$i_{ap}(t_1) = I_{sat} \tag{3-18}$$

$$i_{an}(t_1) = I_{sat} - i_a(t_0) \tag{3-19}$$

where I_{sat} is the IGBT saturation current.

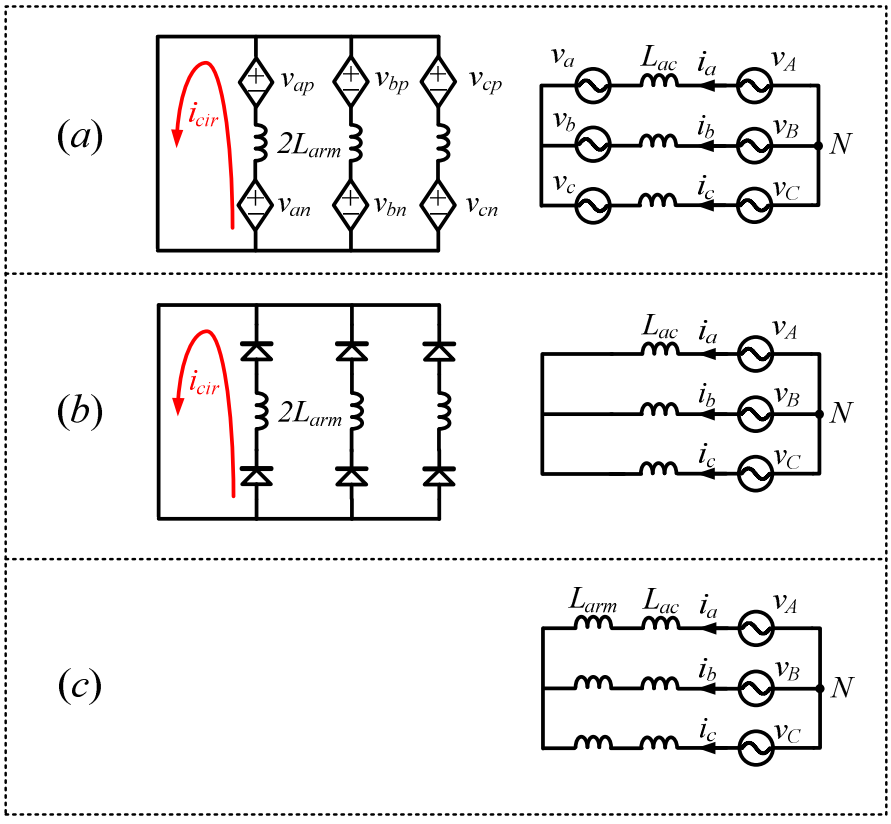


Figure 3-4. Equivalent circuit for pole to ground fault. (a) Stage 1: (t_0, t_1), (b) Stage 2: (t_1, t_2), (c) Stage 3: after t_2.

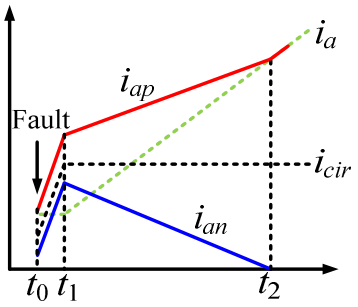


Figure 3-5. Fault current waveform illustration

2) Stage 2: (t_1, t_2)

At t_1, IGBTs are blocked and fault currents flow through diodes. The equivalent circuit is shown in Figure 3-4 (b). Since IGBTs are blocked, the arm voltages become to zero, and the circulating current is freewheeling. On the ac side, three phases at MMC terminal are shorted and the ac source voltages are all applied on the AC inductors, leading to the change of ac currents. According to (5) and (6), one arm current increases and the other arm current decreases until the current reaches zero at t_2.

The arm currents at t_2 can be expressed as:

$$i_{ap}(t_2) = i_a(t_2) \tag{3-20}$$

$$i_{an}(t_2) = 0 \tag{3-21}$$

3) Stage 3: after t_2

During this stage, only diodes in one arm for a phase-leg are conducting. So there is no circulating current. The arm current will either be zero or equal to the ac side current, based on the ac side current direction. The fault current in this stage is limited by

both the ac inductors and arm inductors. The equivalent circuit is shown in Figure 3-4 (c). The calculation of the fault current has been explained in [36].

3.3.2 Discussion on arm inductance selection

As discussed in 3.3.1, the arm inductor can limit the transient fault current flowing through IGBTs and the steady state fault current flowing through diodes. The requirement on inductance for limiting the steady state fault current is definitely larger than that for limiting the transient fault current. But the ac side inductor can also be used to limit the steady state fault current. Thus there are two types of arrangement of inductors as shown in Figure 3-6. Two separate arm inductors are used in Figure 3-6 (a). In this case, the arm inductor is designed to limit the steady state fault current. While in Figure 3-6 (b), coupled arm inductors are used and an additional ac inductor is used to limit the steady state fault current. In this case, the arm inductors are used only for limiting the transient fault current. Both arrangements have been used in the literature. The pros and cons of these two arrangements need to be further studied.

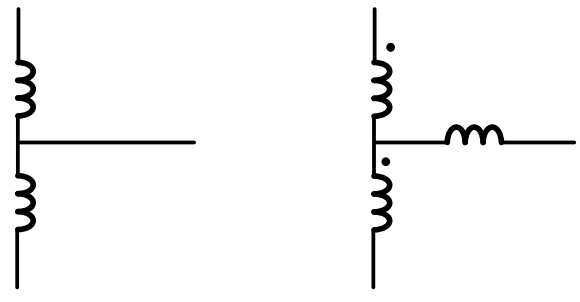


Figure 3-6. Arrangement of inductors in MMC.

3.4 Simulation Verification

To verify the theoretical analysis of the switching frequency circulating current, a simulation model of three-phase MMC with 4 SMs per arm is built in MATLAB. Table 1 summarizes the parameters of the system. The ac side inductance includes the transformer leakage inductance, ac side equivalent inductance and the additional ac side inductance for limiting the steady state fault current. The arm inductance is selected without the consideration on limiting the steady state fault current.

Since experimental results of a down-scaled prototype will be presented to validate the analysis on switching frequency circulating current in chapter 5, the related simulation results for switching frequency circulating current are not presented here.

Table 1. Parameters of the simulation system

Capacity	5 MW
Rated ac grid voltage	1.67 kV
Rated ac current	1 kA
Rated dc voltage	3.2 kV
Rated sub-module capacitor votlage	1.6 kV
Ac side inductance	0.45 mH (0.1 in pu)
Arm inductance	0.045 mH (0.01 in pu)
Sub-module capacitance	10 mF

Figure 3-7 shows the steady state fault currents at ac side, and Figure 3-8 shows the transient fault current of arm currents. The transient fault current waveforms match the waveforms in Figure 3-5, which verify the theoretical analysis.

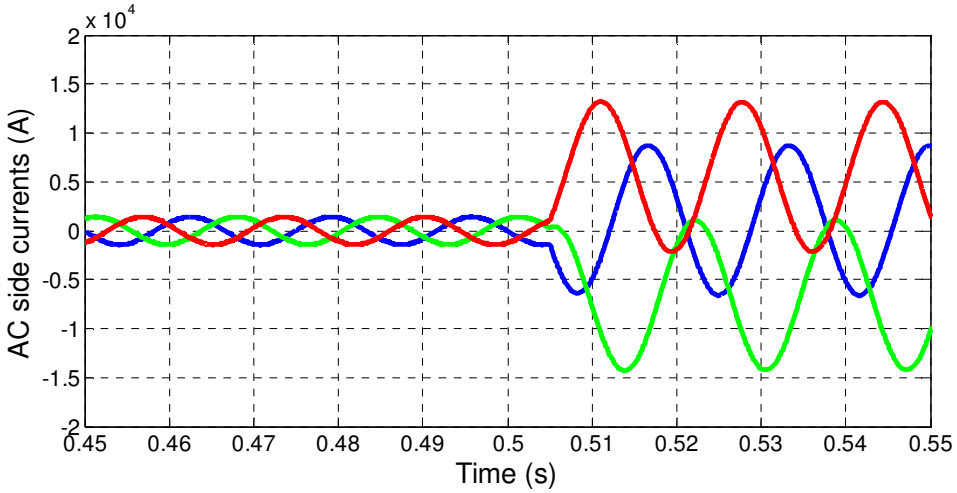


Figure 3-7. Ac side currents for pole-to-pole short circuit fault.

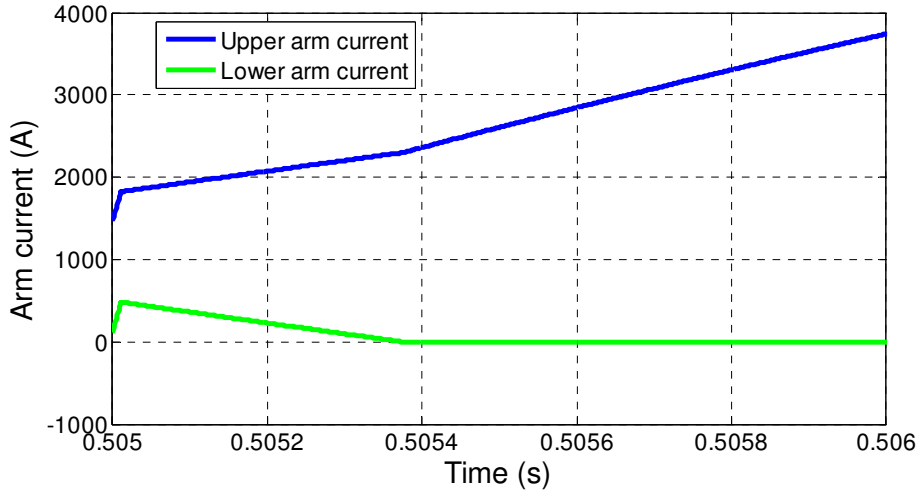


Figure 3-8. Arm currents after a pole-to-pole short circuit fault.

3.5 Conclusions

The dominating second-order circulating current in MMC can be theoretically eliminated after the implementation of the circulating current suppressing control, but switching frequency harmonic is produced as a result. The theoretical analysis presented in this thesis shows that the switching frequency circulating current has a dependence on the arm inductance. Thus the arm inductance should be selected based on the switching frequency circulating current limit.

A detailed fault analysis of pole-to-pole fault has been conducted, showing the arm inductor can be used to limit fault current. As the analysis also indicates the ac side inductor could also be used to limit the fault current, the selection of arm inductance based on limiting fault current is related to the overall design of arm inductors and ac side inductors.

Chapter 4 Sub-Module Capacitance Selection Principle

4.1 Introduction

As the number of sub-modules in MMC can be large, especially for applications like HVDC transmission systems, the sub-module capacitor is thus a main component of the converter. So, optimizing the selection of sub-module capacitance is a critical design in MMC. When the sub-module is in inserted mode, arm current flows through the sub-module capacitor causing the capacitor voltage fluctuations. The sub-module capacitance is designed to suppress the voltage fluctuation to meet the required specifications.

In [47], the analytical relationship between sub-module capacitance and its voltage fluctuation is developed, on which the sub-module capacitance can be selected to meet the voltage fluctuation specifications. However, this relationship is derived based on the assumption that all sub-module capacitor voltages are well balanced. As defined in this thesis, “well balanced” means the sub-module capacitor voltages are nearly the same. The well balanced case can be approximately achieved when the traditional sorting method is implemented or by setting a small voltage threshold for the modified sorting method. However, both approaches would result in relatively high switching frequency. Reference [45] has explained that the voltage-balancing control is under the cost of higher switching frequency to reduce the unbalanced voltage. For some applications like HVDC transmission systems, MMC needs to operate at relatively low switching frequency conditions [22], in which case sub-module capacitor voltage-unbalance issue

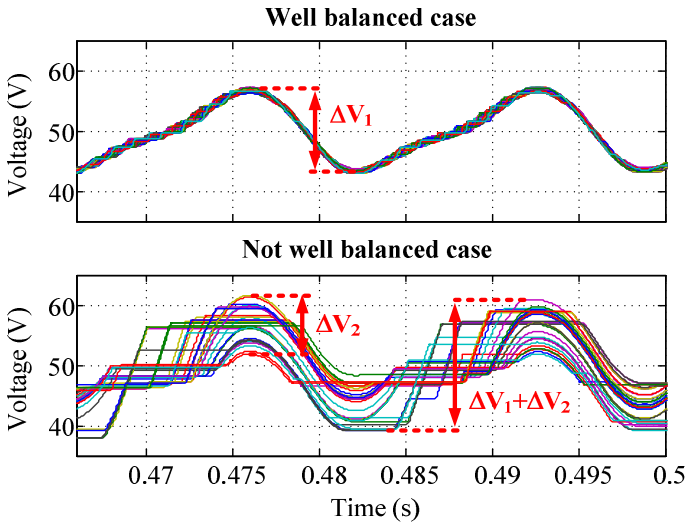


Figure 4-1. Simulation waveform of sub-module capacitor voltages

cannot be neglected. As the unbalanced voltage increases the sub-module capacitor voltage fluctuation, the sub-module capacitance selection criterion based on the relationship between the sub-module capacitance and voltage fluctuation derived in [47] is no longer accurate in these conditions.

Figure 4-1 shows the simulation waveforms of sub-module capacitor voltages for the well balanced case and not well balanced case respectively. For the well balanced case, all the capacitor voltages have nearly the same voltage variation of ΔV_1, which is required by the operating principle. While for the not well balanced case, the capacitor voltage variation is increased to $\Delta V_1 + \Delta V_2$, where ΔV_2 represents the unbalanced voltage which should be equal to the threshold voltage of the modified sorting method (V_{th}). As it is shown in Figure 4-1, ΔV_2 is comparable to ΔV_1, which indicates the unbalanced voltage cannot be neglected in the case when sub-module capacitor voltages are not well

balanced. Therefore, the sub-module capacitance design for MMC operating at low switching frequency conditions should consider the unbalanced voltage, and the relationship between the switching frequency and unbalanced voltage is required.

4.2 Analytical expression of unbalanced voltage

As discussed in chapter 2, the key operating principle of MMC is to generate the desired arm voltage. The derivation of the number of inserted sub-modules in (2-8) and (2-9) is based on the assumption that all sub-module capacitor voltages are identical. If the capacitor voltages are not well balanced, the generated arm voltage will thus not be equal to the reference. Therefore, the voltage-balancing control, on the other hand, can be understood as the way to compensate for the arm voltage error.

For a better explanation, the arm voltage reference in the following section is approximated by the arm voltage when MMC operates with instantaneously balanced SM capacitor voltages.

4.2.1 Arm voltage error

The arm voltage is the sum of capacitor voltages for those inserted sub-modules, which can be expressed as:

$$v_{ap\_act}(t) = \sum_{inserted} v_{c\_act}(t) = N \cdot n_{ap}(t) \cdot \bar{v}_{c\_act}(t) \tag{4-1}$$

where $v_{c\_act}(t)$ represents the sub-module capacitor voltage, and $\bar{v}_{c\_act}(t)$ is denoted as the average value of the capacitor voltages of inserted sub-modules. Based on (2-10), the arm voltage reference can also be rewritten as:

$$v_{ap\_ref}(t) = N \cdot n_{ap}(t) \cdot v_{c\_ref}(t) \tag{4-2}$$

Subtracting (4-2) from (4-1), the arm voltage error is given as:

$$v_{ap\_err}(t) = N \cdot n_{ap}(t) \cdot \left(\bar{v}_{c\_act}(t) - v_{c\_ref}(t)\right) \tag{4-3}$$

The increment on arm voltage error in each control cycle (dt) can then be derived as:

$$\begin{aligned} dv_{ap\_err}(t) = N \cdot n_{ap}(t) \cdot d\left(\bar{v}_{c\_act}(t) - v_{c\_ref}(t)\right) + N \cdot dn_{ap}(t) \\ \cdot \left(\bar{v}_{c\_act}(t) - v_{c\_ref}(t)\right) \end{aligned} \tag{4-4}$$

For each control cycle, only the capacitor voltages of the inserted sub-modules will change. But by assuming instantaneously balanced sub-module capacitor voltages, all the sub-module capacitors share the voltage change, that is:

$$N \cdot n_{ap}(t) \cdot d\bar{v}_{c\_act}(t) = N \cdot dv_{c\_ref}(t) \tag{4-5}$$

where $dv_{c\_ref}(t)$ can be derived based on the average model in [47].

$$dv_{c\_ref}(t) = \frac{1}{C_{sub}} n_{ap}(t) \cdot i_{ap}(t)dt \tag{4-6}$$

Considering $\bar{v}_{sub\_act}(t) \approx v_{sub\_ref}(t)$, (4-4) can be rewritten as:

$$dv_{ap\_err}(t) = \frac{1}{C_{sub}} \cdot N \cdot n_{ap}(t) \cdot \left[1 - n_{ap}(t)\right] \cdot i_{ap}(t) \cdot dt \tag{4-7}$$

4.2.2 Effect of voltage-balancing control on compensating arm voltage error

Based on the modified sorting method, switching events occur under the following two conditions.

1. Extra sub-module is required to be inserted or bypassed based on the modulation

Suppose the arm current is charging the sub-module capacitor and an extra sub-module needs to be inserted, the previous bypassed SM with the lowest capacitor voltage is chosen to be inserted. Thus the arm voltage is increased by the lowest capacitor voltage. However, for the instantaneously balanced case the arm voltage is increased by the average capacitor voltage. Therefore, this switching event would introduce an error on arm voltage, but as a way to compensate for the error in (4-7), which caused by the modulation. The voltage difference between the lowest capacitor voltage and the average voltage can be approximated as half of the unbalanced voltage threshold as shown in Figure 4-2. Thus, the compensated voltage introduced by this switching event can be given as:

$$\Delta v_{ap\_com} = -\frac{V_{th}}{2} \tag{4-8}$$

If the arm current is discharging the sub-module capacitor, the introduced voltage error would be $V_{th}/2$. But this voltage is still compensating the voltage error caused by modulation. Thus, (13) can be used to describe the introduced arm voltage error by this switching event, with "$-$" represents it compensates for the error introduced by modulation.

2. Maximum voltage difference among sub-module capacitors exceeds the set threshold value

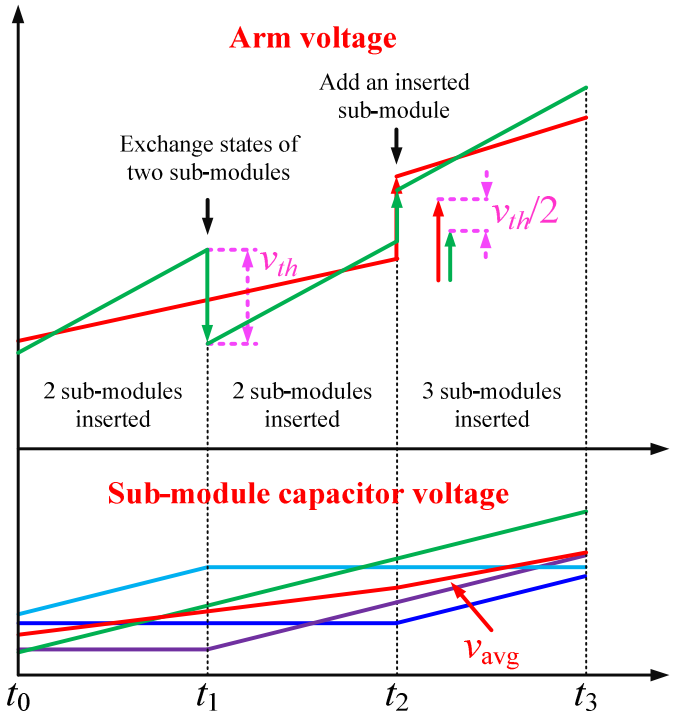


Figure 4-2. Explanation of voltage-balancing control's effect on compensating arm voltage error

In this case, the previously inserted sub-module with the highest or lowest capacitor voltage is bypassed, and the previously bypassed sub-module with lowest or highest capacitor voltage is inserted. So this switching event can be considered as two switching events in case 1. The introduced arm voltage error is thus given as:

$$\Delta v_{ap\_com} = -V_{th} \tag{4-9}$$

As mentioned above, the voltage-balancing control needs to compensate for the arm voltage error introduced by modulation. Hence, the voltage error introduced by modulation in a fundamental period can be derived as:

$$\int_0^T \left|dv_{ap\_err}(t)\right| = \int_0^T \left|\frac{N}{C_{sub}} \cdot \left(\frac{1}{2} - \frac{1}{2}M\cos\omega t\right)\left(\frac{1}{2} + \frac{1}{2}M\cos\omega t\right) \cdot \left(\frac{I_{dc}}{3} + \frac{I_{ac}}{2}cos(\omega t + \theta)\right)\right| \cdot dt \tag{4-10}$$

Based on (4-8) and (4-9), the compensated voltage introduced by voltage-balancing control is given as:

$$v_{up\_com} = -\frac{V_{th}}{2} \cdot N_{sw} \tag{4-11}$$

where N_{sw} represents the total number of switching events, with one switching event is denoted as a change of sub-module switching state. Based on the definition of switching frequency, the average switching frequency for MMC can be obtained as:

$$f_{sw} = \frac{N_{sw}}{2N} \tag{4-12}$$

Inserting (4-12) into (4-10) and (4-11) yields

$$f_{sw} \times v_{th} = \int_0^T \left|\frac{1}{C_{sub}} \cdot \left(\frac{1}{2} - \frac{1}{2}M\cos\omega t\right)\left(\frac{1}{2} + \frac{1}{2}M\cos\omega t\right) \cdot \left(\frac{I_{dc}}{3} + \frac{I_{ac}}{2}cos(\omega t + \theta)\right)\right| \cdot dt \tag{4-13}$$

4.3 Simulation verification

To verify the developed relationship between the switching frequency and the unbalanced SM capacitor voltage, a simulation model of MMC with 32 SMs per arm is built in MATLAB. Nearest level modulation with the modified sorting method is implemented. The SM capacitance is 2.7 mF, and the capacitor average voltage is 50 V. Thus the dc bus voltage is 1600 V, and the rated phase current is 40 A. These parameters are chosen to match those of down-scaled MMC prototype in the lab.

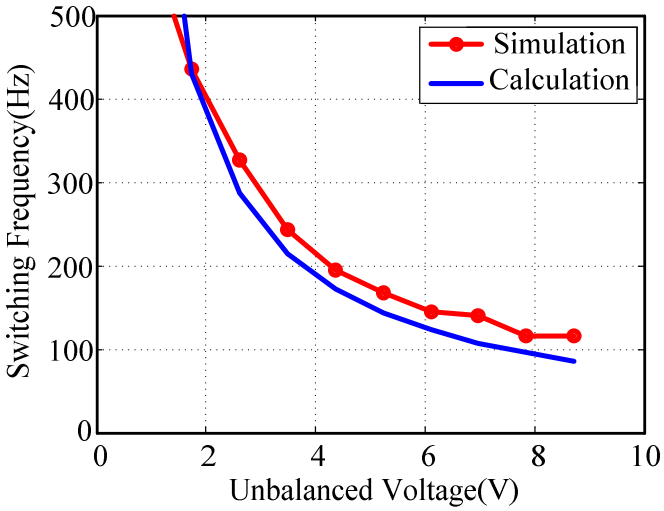
Figure 4-3 (a) shows the comparison of the calculation and simulation results on the relationship between switching frequency and unbalanced voltage with the given operating condition ($M = 0.8$ and $\theta = \pi/4$). The simulation results match the calculation well, with a tolerable error. The error is mainly caused by the approximation on compensated voltage in case. For case 2, the compensated voltage is exactly equal to V_{th}, as the switching event occurs once the voltage difference is larger than the threshold voltage. However, for case 1 the switching event is determined by the modulation, and it is possible that the unbalanced voltage is smaller than the threshold voltage. As a result, the compensated voltage would be smaller than that in (4-8).

Figure 4-3 (b) and Figure 4-3 (c) show the simulation results still match the theoretical analysis under different operating conditions, thus validating the derived relationship between switching frequency and unbalanced SM capacitor voltage in MMC.

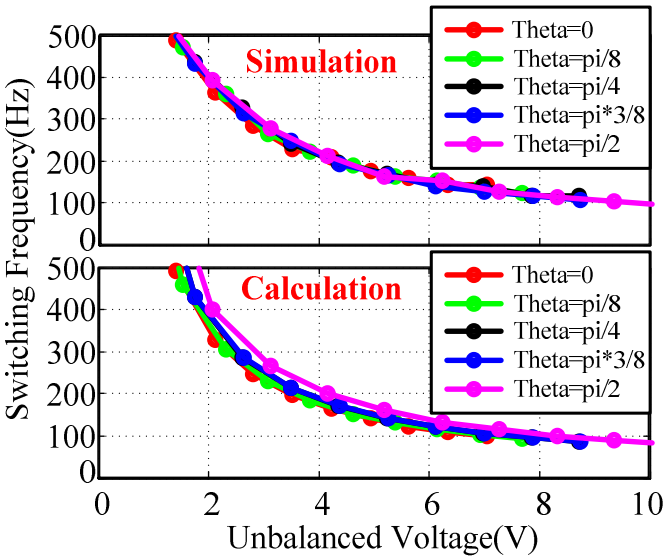
4.4 Conclusions

Voltage difference among sub-module capacitors increases the capacitor voltage fluctuation, and its impact on the total voltage fluctuation is large when MMC operates at low switching frequency conditions. The analytical relationship between sub-module capacitor unbalanced voltage and the switching frequency is derived based on the voltage-balancing control with the modified sorting method. It is shown that the switching frequency in MMC is inversely proportional to the sub-module capacitor unbalanced voltage, which influences the sub-module capacitance selection. Simulation results verify the

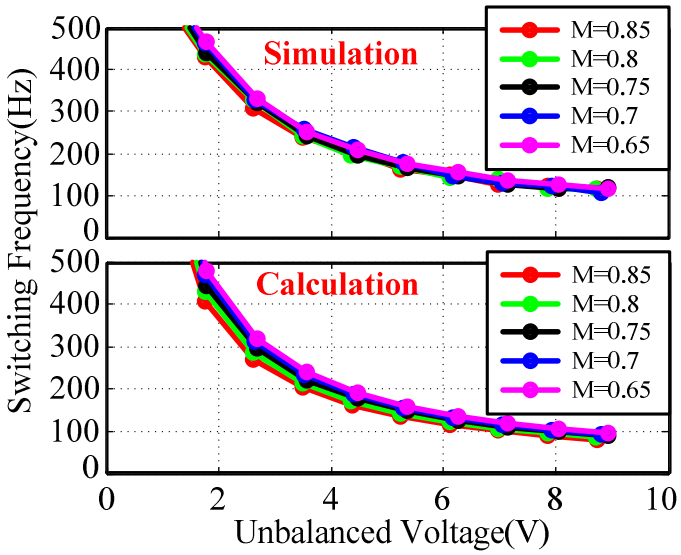
Figure 4-3. Comparison of the simulation and calculation results on the relationship between switching frequency and unbalanced voltage: (a) $M = 0.8$ and $\theta = \pi/4$, (b) $M = 0.8$, and (c) $\theta = \pi/4$


Simulation
Calculation
Switching Frequency(Hz)
Unbalanced Voltage(V)
0
100
200
300
400
500
0
2
4
6
8
10

(a)


Simulation
Calculation
Theta=0
Theta=pi/8
Theta=pi/4
Theta=pi*3/8
Theta=pi/2
Switching Frequency(Hz)
Unbalanced Voltage(V)
0
100
200
300
400
500
0
2
4
6
8
10

(b)


Simulation
Calculation
M=0.85
M=0.8
M=0.75
M=0.7
M=0.65
Switching Frequency(Hz)
Unbalanced Voltage(V)
0
100
200
300
400
500
0
2
4
6
8
10

(c)

developed relationship between sub-module capacitor unbalanced voltage and the switching frequency.

The derived relationship between unbalanced voltage and switching frequency, on the other hand, can also provide a guide for determing the threshold voltage for the modified sorting method when the switching frequency is chosen first.

Chapter 5 Hardware Design and Experimental Verification

Considering the available experimental conditions, a scaled down prototype of three-phase MMC with 2 sub-modules per arm is built for the preliminary verification of the analysis on arm inductance and sub-module capacitance design.

5.1 Scaled down prototype design

At the preliminary stage, only 2 sub-modules are used in each arm. It would be fine for the switching frequency circulating current analysis. But in order to verify the proposed sub-module capacitance selection criterion, voltage unbalance issue should be considered. In this case, 2 sub-modules per arm would not be enough. Thus a single-phase MMC with 6 sub-modules per arm is also configured. Figure 5-1 shows the three-phase MMC prototype configuration. The MMC is connected to a constant dc voltage source as inverter mode. The load bank with inductors and resistors are used.

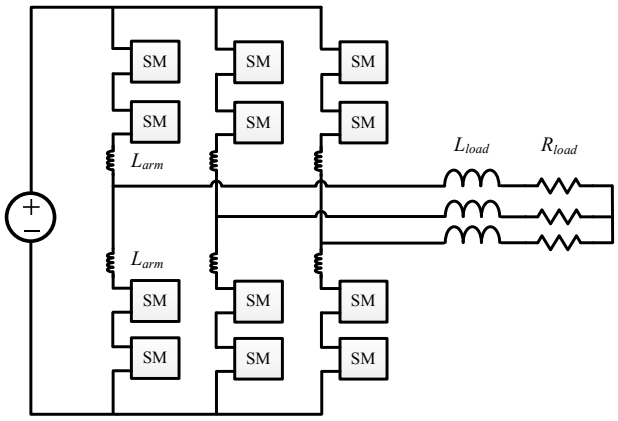


Figure 5-1. Three-phase MMC prototype configuration

The system configuration of the hardware test is shown in Figure 5-2. For the control unit, a TI TMS320F28335 DSP developer board and an Altera Cyclone III FPGA starter board are used. The DSP board is used as the main controller, including the ac side current control, ac side voltage control, and generating the arm voltage reference for the FPGA board. The FPGA board works as the auxiliary controller for the voltage-balancing control and generating the pulses for devices. The reason for using two control board is that the DSP board cannot output enough PWM signals, while the FPGA board is not good at dealing with the complex control.

Based on the system architecture of Figure 5-2, the hardware development includes three parts: sub-module board, sensor board and interface board.

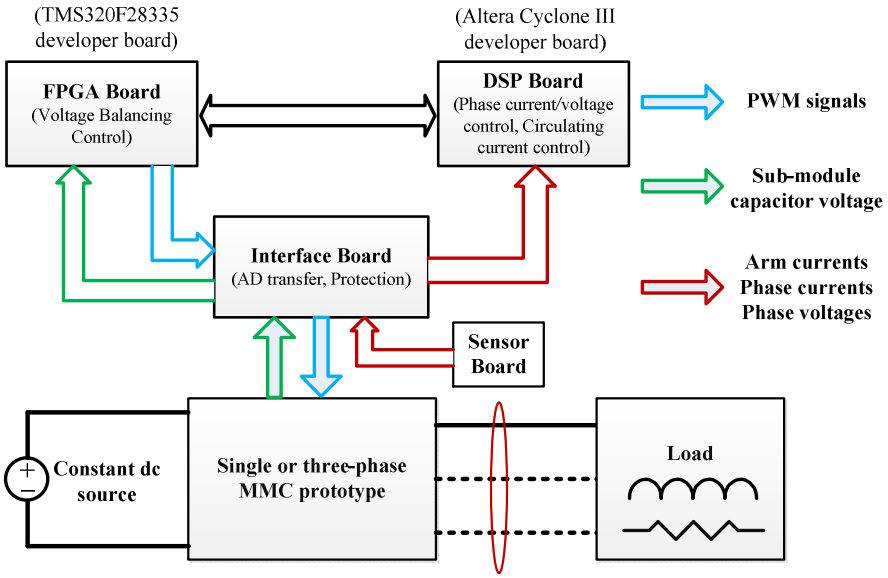


Figure 5-2. Three-phase MMC prototype configuration

1) Sub-module board

The sub-module board includes two half-bridges and required gate drivers and the sub-module capacitor voltage measurement. MOSFET IPP320N20N3 and fast recovery diode STPS20SM120SR are used as the power devices. The gate drive circuit is shown in Figure 5-3. The bootstrapping circuit is used.

A photo of the built sub-module board is shown in Figure 5-4. The sub-module board receives the pulse signals from the interface board, and also need to send measurement of the capacitor voltage back to the interface board.

2) Sensor board

The sensor board includes the measurement of ac side phase currents, phase voltages and arm currents. The measurement signals are sent to the interface board. Figure 5-5 shows a photo of the sensor board.

3) Interface board

The interface board contains the functions of analog-to-digital and digital-to-analog transfer, voltage level transfer, signal isolation and protection. It works as the interface between the sub-module board, sensor board and the control unit.

A photo of the interface board with the DSP board and FPGA board is shown in Figure 5-6.

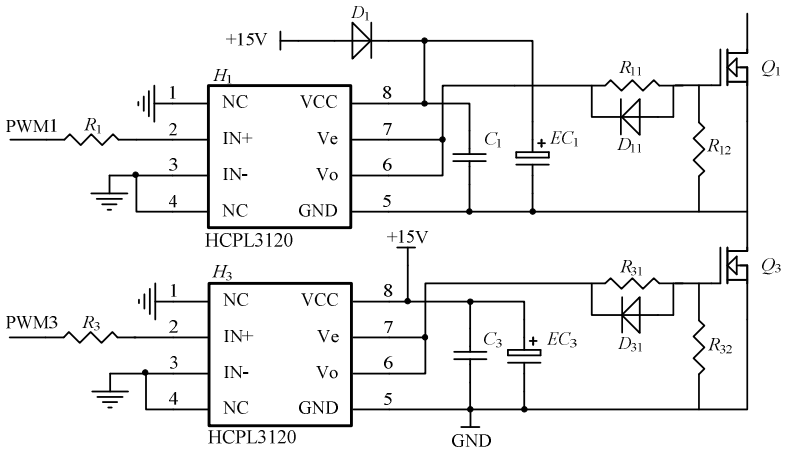


Figure 5-3. System architecture of the hardware test

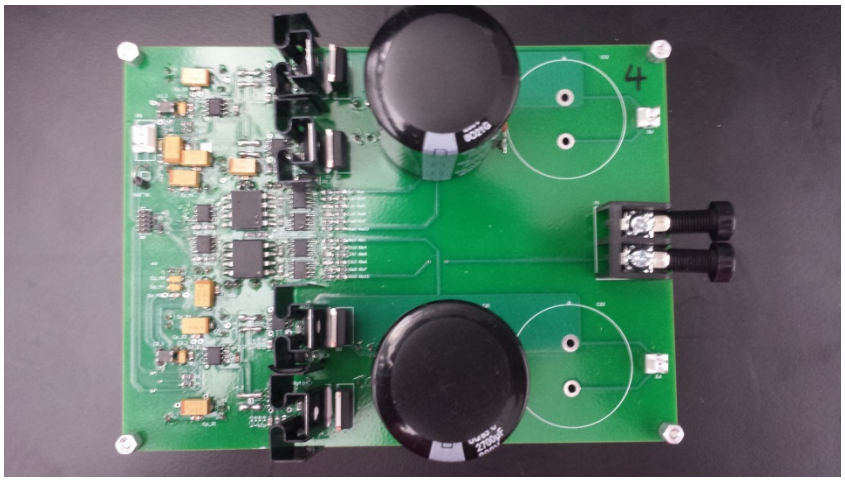


Figure 5-4. Photo of sub-module board

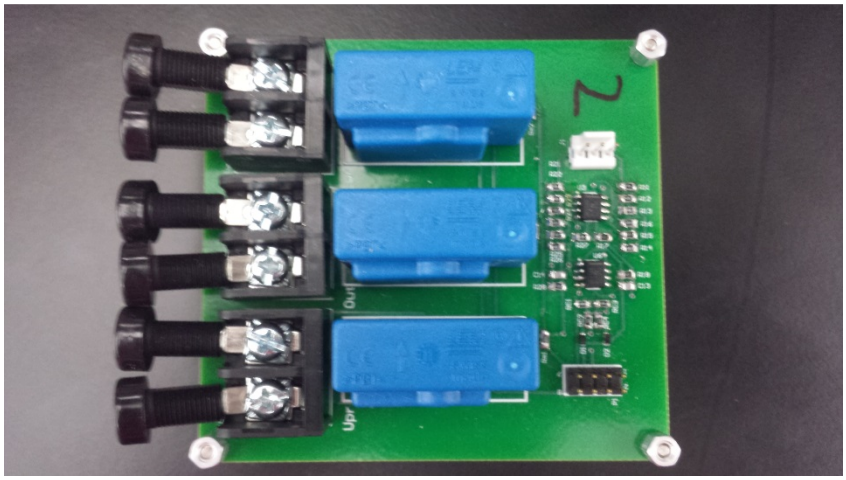


Figure 5-5. Photo of sensor board

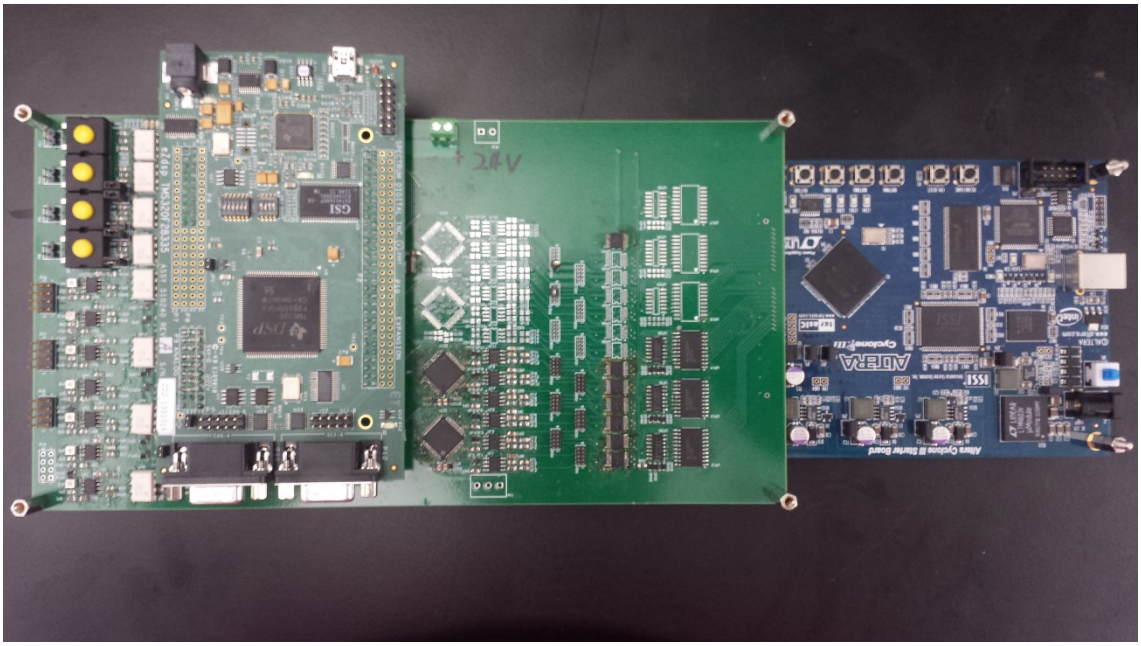


Figure 5-6. Photo of interface board with DSP board and FPGA board

5.2 Experimental verification

Both three-phase and single-phase test of the MMC prototype have been conducted. The system parameters are shown in Table 2.

5.2.1 Three-phase MMC test

Figure 5-7 shows the experimental results at rated conditions. The arm inductance is 1 mH, and the circulating current suppressing control is disabled. The large circulating current contains a large second-order harmonic. In Figure 5-8, the arm inductance is still 1 mH, but the circulating current suppressing control is enabled. It can be seen clearly that the second-order circulating current is largely reduced.

Figure 5-7 and Figure 5-8 also show that the two capacitor voltage waveforms in

Table 2. System parameters for hardware test

Descriptions	Three-phase MMC	Single-phase MMC
Rated power	1 kW	1 kW
Rated ac current	10 A	10A
Rated dc voltage	100 V	300 V
Rated ac frequency	60 Hz	60 Hz
Average sub-module capacitor voltage	50 V	50 V
Sub-module number per arm	2	6
Sub-module capacitance	2.7 mF	2.7 mF

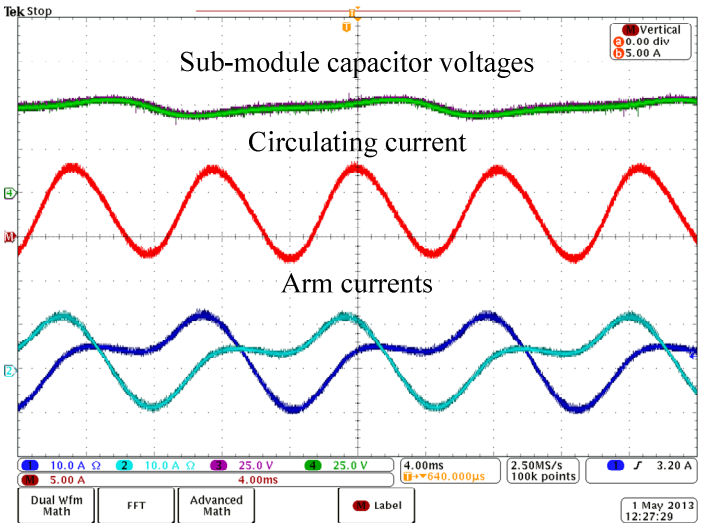


Figure 5-7. Experimental results at $L_{arm} = 1$ mH with circulating current suppressing control disabled

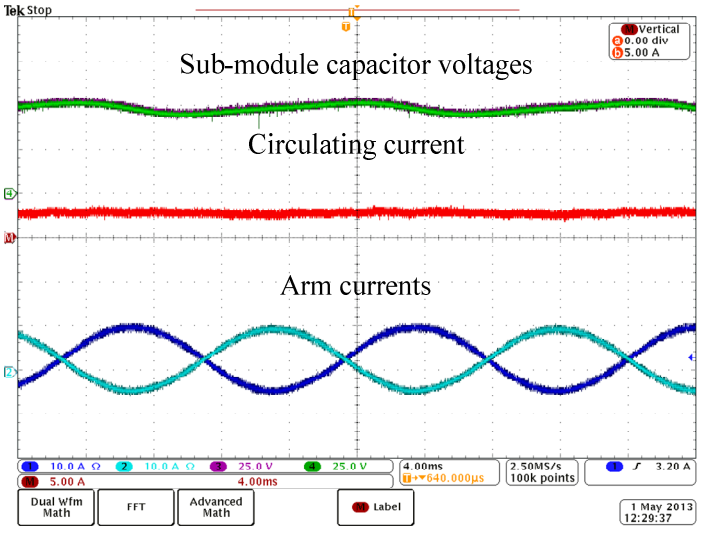


Figure 5-8. Experimental results at $L_{arm} = 1$ mH with circulating current suppressing control enabled

one arm. The two capacitor voltages are nearly the same, which validates the effectiveness of the voltage-balancing control.

Figure 5-9 shows the experimental result for arm inductance of 0.1 mH, which is 1/10 of that in Figure 5-8. It is shown that the circulating current contains high frequency harmonics. Figure 5-10 shows the circulating current and the corresponding phase-leg voltage for a small time scale. This waveform matches the theoretical analysis in Figure 3-2 well, thus validating the existence of the switching frequency circulating current.

Tests have been conducted for different arm inductors. Figure 5-11 shows a comparison of the theoretical and experimental values of the maximum peak to peak switching frequency circulating currents with different arm inductors. The experimental results show a close agreement with the calculation.

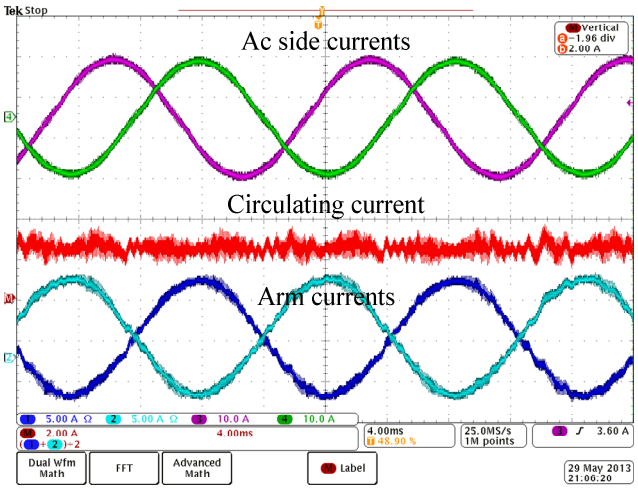


Figure 5-9. Experimental results at $L_{arm} = 0.1$ mH with circulating current suppressing control enabled

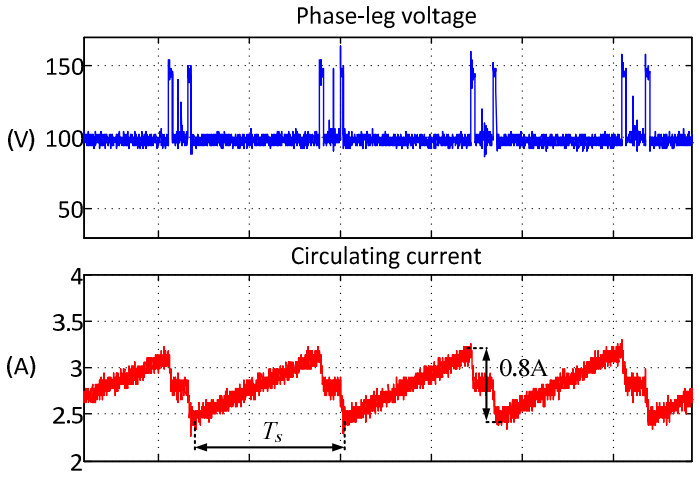


Figure 5-10. Experimental results at $L_{arm} = 0.1$ mH with circulating current suppressing control enabled

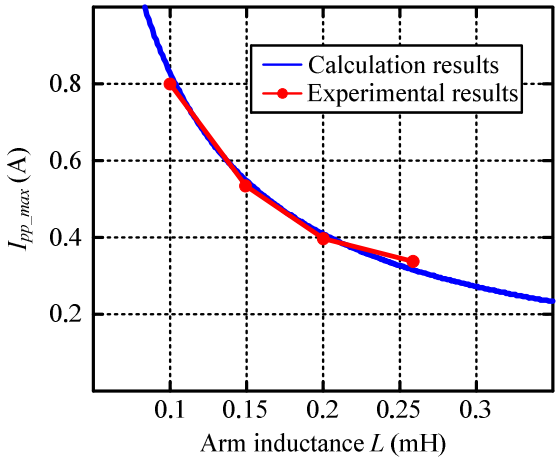


Figure 5-11. Maximum switching frequency circulating current versus arm inductance

For a test at arm inductance of 15 uH, the switching frequency circulating current is even increased. The waveforms are shown in Figure 5-12. It can be seen that dc side current also contains large high frequency components which means the switching frequency circulating current will distort the dc current. Thus additional dc filter would be required to achieve a smooth dc current. So the reduction of arm inductors is limited to make the switching frequency circulating current not too large.

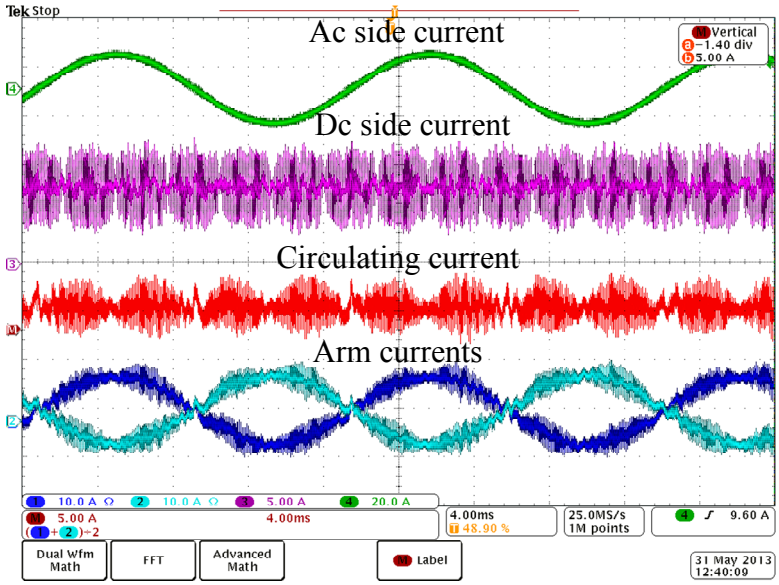


Figure 5-12. Experimental results at $L_{arm} = 0.015$ mH with circulating current suppressing control enabled

5.2.2 Single-phase MMC test

The test of the single-phase MMC with 6 sub-modules per arm is intended to verify the analysis on sub-module capacitance selection.

The basic operating principle has been verified. Figure 5-13 shows the experimental result when the circulating current suppressing control is enabled. More tests will be conducted in the future to verify the sub-module capacitance selection principle.

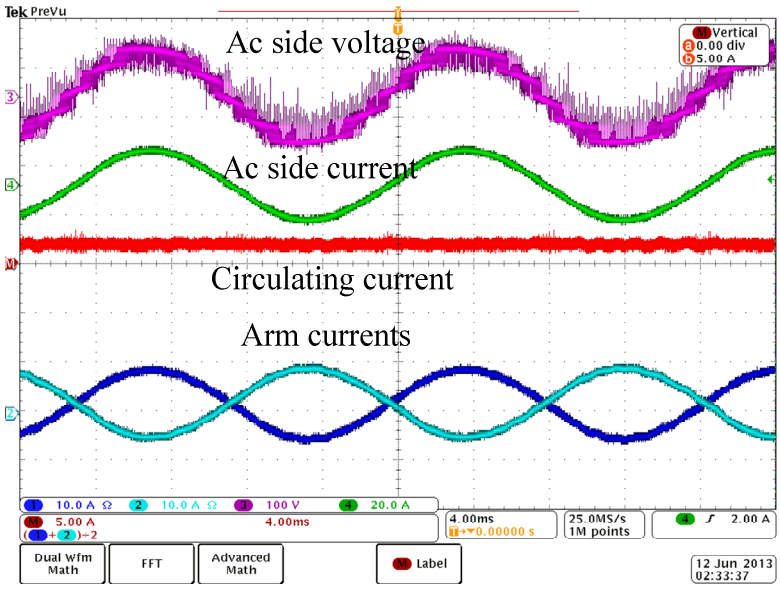


Figure 5-13. Experimental results at $L_{arm} = 1$ mH with circulating current suppressing control enabled

Chapter 6 Conclusion and Future Work

6.1 Conclusion

This thesis has investigated the selection principle of the arm inductance and sub-module capacitance in MMC. It is proposed that the arm inductance should be designed based on limiting the switching frequency circulating current when the circulating current suppressing control is implemented. The derived relationship between the arm inductance and switching frequency circulating current has been verified by the experimental results from a down-scaled three-phase MMC prototype.

For some applications, arm inductance selection also needs to consider for limiting dc side short circuit fault current. The impact of arm current on limiting the fault current has been fully discussed; it is found that the design of ac side inductors will have a critical impact on arm inductance selection.

It is also proposed in this thesis that the sub-module capacitance selection criterion should consider the impact of voltage unbalance among sub-module capacitors. The derived analytical expression of the unbalanced voltage enables the theoretical calculation of maximum sub-module capacitor voltage ripple, which can be used for sub-module capacitance selection. Simulation results from a MMC with 32 sub-modules per arm validate the analytical expression.

6.2 Future work

In order to finish the study on arm inductance and sub-module capacitance design, the following works should be conducted in the future:

1) The derivation of the relationship between the arm inductance and switching frequency circulating current is based on the PWM. It should be further evaluated whether this relationship applies to modulation methods without PWM.
2) A comparison of the two arrangements of inductors in 3.3 should be conducted. The impact of the arm inductor and ac side inductor on limiting the fault current has been understood. But it is still unknown whether the arm inductor or the ac side inductor should be used to limit the fault current.
3) The benefits of the proposed selection methods on arm inductance and sub-module capacitance compared to the previous methods should be evaluated.

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