



University of Tennessee, Knoxville  
Trace: Tennessee Research and Creative  
Exchange

---

Masters Theses

Graduate School

---

8-2005

# Analytical Modeling and Simulation of SiGe MOS Gate HEMT

Mohammad Tanvir Alam  
*University of Tennessee - Knoxville*

---

## Recommended Citation

Alam, Mohammad Tanvir, "Analytical Modeling and Simulation of SiGe MOS Gate HEMT. " Master's Thesis, University of Tennessee, 2005.  
[https://trace.tennessee.edu/utk\\_gradthes/1575](https://trace.tennessee.edu/utk_gradthes/1575)

This Thesis is brought to you for free and open access by the Graduate School at Trace: Tennessee Research and Creative Exchange. It has been accepted for inclusion in Masters Theses by an authorized administrator of Trace: Tennessee Research and Creative Exchange. For more information, please contact [trace@utk.edu](mailto:trace@utk.edu).

To the Graduate Council:

I am submitting herewith a thesis written by Mohmmad Tanvir Alam entitled "Analytical Modeling and Simulation of SiGe MOS Gate HEMT." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Syed K. Islam, Major Professor

We have read this thesis and recommend its acceptance:

Donald W. Bouldin, Benjamin J. Blalock

Accepted for the Council:

Dixie L. Thompson

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

---

To the Graduate Council:

I am submitting herewith a thesis written by Mohammad Tanvir Alam entitled “Analytical Modeling and Simulation of SiGe MOS Gate HEMT.” I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirement for the degree of Master of Science, with a major in Electrical Engineering.

Syed K. Islam  
Major Professor

We have read this thesis  
and recommend its acceptance:

Donald W. Bouldin

Benjamin J. Blalock

Accepted for the Council:

Anne Mayhew  
Vice Chancellor and Dean of  
Graduate Studies

(Original signatures are on file with official student records.)

# **Analytical Modeling and Simulation of SiGe MOS Gate HEMT**

*A Thesis  
Presented For the  
Master of Science  
Degree*

**The University of Tennessee, Knoxville**

**Mohammad Tanvir Alam  
August 2005**

## **Dedication**

*This work is dedicated to my parents and my sister. Without their love, support and encouragement, I could not come to this point of my life.*

## Acknowledgements

At first, I would like to thank my supervisor Dr. Syed K. Islam for providing me the opportunity to work with him. His constant inspiration, guidance and comments have helped me in my research as well as in course works. I would like to thank Dr. Donald Bouldin and Dr. Benjamin Blalock for their guidance and help. I would like to convey my special thanks to Dr. Hanno Weitering of Physics department for doing an excellent job in teaching quantum mechanics and helping me in my research works.

I would like to thank all my group members for their continuous support. I want to specially thank Dr. Hasanuzzaman for his valuable advice, Mohammad Adeeb and Mohammad. Rahman for their help in course work and research, Hung Nguyen and Rajagopal Vijayaraghavan for their help on different occasions.

Matt Disney deserves special thanks for helping me solve some problems with *Medici<sup>TM</sup>*.

Finally, I want to thank all my friends and family for helping and encouraging me at good times as well as at bad times.

# Abstract

This thesis presents work on analytical modeling and simulation of SiGe MOS gate HEMT. A modified model for the threshold voltage of the MOS-gate HEMT is presented. An expression to calculate accurately minimum gate voltage  $V_{Gmin}$  of p-channel MOS-gate HEMT is derived. Using the modified expressions,  $V_{THp}$  and  $V_{Gmin}$  are calculated. Current-voltage characteristics, transconductance and cutoff frequency are calculated and plotted using the modified model and the results are compared with the results obtained from an existing model. The effects of different device and material parameter variation on  $V_{THp}$  and  $V_{Gmin}$  are also investigated.

An analytical temperature model for the MOS-gate HEMT is proposed. The temperature variation of threshold voltage, current-voltage characteristics and transconductance are simulated using the analytical model.

A model for a delta-doped MOS-gate HEMT is proposed which is valid for any width of the delta-doped layer. Effects of different device parameters on  $V_{THp}$  and  $V_{tl}$  have been investigated using this model.

In addition, device simulator *Medici<sup>TM</sup>* has been used to simulate the delta-doped and regular-doped MOS-gate HEMTs. The results obtained from the *Medici<sup>TM</sup>* simulations are compared to some of the results obtained from the analytical model.

Chapter 1 .....	1
<i>Introduction</i> .....	1
1.1 Background.....	1
1.2 Limitations of Silicon-Based MOSFET with Short Channel .....	1
1.3 HEMT: A Light of Hope.....	3
1.4 MOS-Gate HEMT.....	4
1.5 SiGe MOS-Gate HEMT.....	5
1.6 Proposed Work.....	6
1.7 Outline of the Thesis.....	7
 Chapter 2.....	 10
<i>Literature Review</i> .....	10
2.1 HEMT .....	10
2.1.1 What is HEMT.....	10
2.1.2 GaAs/AlGaAs HEMT.....	10
2.1.3 SiGe MOS- gate HEMT.....	13
2.2 Properties of SiGe and Si/SiGe Heterostructure.....	16
2.3 Development of SiGe MOS-Gate HEMT.....	18
 Chapter 3.....	 22
<i>Modified Model for MOS-Gate SiGe HEMT</i> .....	22
3.1 Existing Model for the MOS-Gate HEMT .....	22
3.1.1 The threshold voltage expression.....	22
3.1.2 Calculation of $V_{THp}$ .....	28
3.1.3 Calculation of $V_{Gmin}$ .....	31
3.1.4 The current-voltage characteristics.....	32
3.1.5 The transconductance ( $g_{ms}$ ) and cutoff frequency ( $f_T$ ).....	35
3.2 The Modified Model.....	38
3.2.1 The threshold voltage expression.....	38
3.2.2 Calculation of threshold voltage using modified model.....	46
3.2.3 Calculation of $V_{Gmin}$ .....	49
3.2.4 Current-voltage characteristics .....	51
3.2.5 Transconductance ( $g_{ms}$ ) and cutoff frequency ( $f_T$ ).....	51
3.3 Effect of Device and Material Parameters on $V_{THp}$ and $V_{Gmin}$ .....	54
3.3.1 Effect of doping concentration.....	54
3.3.2 Effect of spacer layer width.....	56
3.3.3 Effect of silicon layer Width.....	58
3.3.4 Effect of oxide thickness.....	60
3.3.5 Effect of mole fraction in $Si_xGe_{1-x}$ .....	62
3.4 Conclusions.....	62
 Chapter 4.....	 65
<i>The Temperature Model</i> .....	65
4.1 Effect of Temperature on Threshold Voltage.....	65
4.1.1 Temperature dependence of doping concentration.....	66



4.1.2 Temperature dependence of metal work function ( $\phi_m$ ) .....	66
4.1.3 Temperature dependence of semiconductor electron affinity ( $\chi_2$ ) .....	67
4.1.4 Temperature dependence of bandgap .....	68
4.1.5 Temperature dependence of $\Delta E_v$ .....	68
4.1.6 Temperature dependence of $\Delta E_{fo}$ .....	69
4.1.7 Calculation of temperature dependence of $V_{THp}$ .....	69
4.2 Effect of Temperature on Hole Mobility ( $\mu_h$ ).....	70
4.3 The Current-Voltage Characteristics .....	72
4.4 Transconductance .....	72
4.5 Conclusions.....	74
Chapter 5.....	76
<i>Analytical Modeling of Delta-Doped HEMT</i> .....	76
5.1 The Existing Threshold Voltage Model.....	76
5.1.1 The threshold voltage expression.....	76
5.1.2 Limitations of the existing model .....	77
5.2 The Modified Threshold Voltage Model .....	78
5.2.1 Need for the modified model .....	78
5.2.2 The threshold voltage expression.....	78
5.2.3 Calculation of threshold voltage .....	81
5.3 The Expression for $V_{tl}$ .....	83
5.4 Effect of $d_1$ and $\delta$ on $V_{THp}$ and $V_{tl}$ .....	84
5.4.1 Effect of $d_1$ .....	85
5.4.2 Effect of $\delta$ .....	87
5.5 Conclusions.....	87
Chapter 6.....	90
<i>Medici<sup>TM</sup> Simulation of MOS-Gate HEMT</i> .....	90
6.1 Brief Introduction To <i>Medici<sup>TM</sup></i> .....	90
6.2 $V_{THp}$ and $V_{Gmin}$ for the MOS-gate HEMT .....	91
6.3 Current Voltage Characteristics of the MOS-Gate HEMT.....	91
6.4 Doping Concentration Dependence of $V_{THp}$ .....	95
6.5 The Temperature Variation of the Threshold Voltage.....	97
6.6 The Temperature Dependence of the $I_D$ - $V_D$ Characteristics.....	97
6.7 $V_{THp}$ and $V_{tl}$ for Delta-Doped MOS-Gate HEMT.....	100
6.8 Discussion.....	102
Chapter 7.....	103
<i>Conclusions</i> .....	103
7.1 Summary of the Work.....	103
7.2 Future Work Directions .....	106
References.....	108

VITA..... 111

## List of Tables

Table 2.1: Basic parameters of bulk $\text{Si}_{1-y}\text{Ge}_y$ , at 300 K.....	19
Table 3. 1: Device and material parameters used to calculate $V_{\text{THp}}$ at 300 K. ....	29
Table 3. 2: Device and material parameters for the calculation of $V_{\text{THp}}$ using modified model.....	47
Table 4. 1: The hole hall mobility at different temperature as estimated from the experimental plot. ....	71
Table 5. 1: Device and material parameters used to calculate $V_{\text{THp}}$ of the delta-doped MOS-gate HEMT.....	82

## List of Figures

Figure 1. 1: The first HEMT, fabricated by Fujitsu Corp in Japan [3]. .....	4
Figure 2. 1: The cross-sectional view of a GaAs/AlGaAs n-channel HEMT.....	12
Figure 2. 2: The cross-sectional view of a p-channel SiGe MOS-gate HEMT. ....	14
Figure 2. 3: The cross-sectional view of an n-channel SiGe MOS-gate HEMT. ....	15
Figure 3. 1: Cross-sectional schematic of a p-Channel SiGe MOS-gate HEMT.....	23
Figure 3. 2: Device schematic, charge distribution and energy band diagram of the p-channel MOS-gate HEMT. ....	25
Figure 3. 3: (a) The $I_{Dsat}$ - $V_G$ and (b) the $I_D$ - $V_D$ characteristics of the p-channel SiGe MOS-gate HEMT, using the analytical model of Jain et al [16]. ....	34
Figure 3. 4: (a) The $g_{ms}$ vs. $V_G$ and (b) the $f_T$ vs. $L$ plot of the p-channel SiGe MOS-gate HEMT, using the analytical model of Jain et al [16]. ....	37
Figure 3. 5: Device schematic, charge distribution and energy band diagram of the p-channel MOS-gate HEMT, used in the modified model. ....	39
Figure 3. 6: (a) The $I_{Dsat}$ - $V_G$ and (b) the $I_D$ - $V_D$ characteristics, using existing and modified model.....	52
Figure 3. 7: (a) The $g_{ms}$ vs. $V_G$ and (b) The $f_T$ vs. $L$ plot, using existing and modified model.....	53
Figure 3. 8: (a) $N_2$ vs. $V_{THp}$ plot and (b) $N_2$ vs. $V_{Gmin}$ plot of the p-channel .....	55
Figure 3. 9: (a) $d_i$ vs. $V_{THp}$ plot and (b) $d_i$ vs. $V_{Gmin}$ plot of the p-channel.....	57
Figure 3. 10: (a) $d_s$ vs. $V_{THp}$ plot and (b) $d_s$ vs. $V_{Gmin}$ plot of the p-channel.....	59
Figure 3. 11: (a) $t_{ox}$ vs. $V_{THp}$ plot and (b) $t_{ox}$ vs. $V_{Gmin}$ plot of the p-channel .....	61
Figure 3. 12: (a) Mole fraction $x$ vs. $V_{THp}$ plot and (b) mole fraction $x$ vs. $V_{Gmin}$ plot of the p-channel SiGe MOS-gate HEMT.....	63
Figure 4. 1: Temperature variation of the threshold voltage. ....	70
Figure 4. 2: Temperature variation of (a) the $I_{Dsat}$ - $V_G$ and (b) the $I_D$ - $V_D$ characteristics.....	73
Figure 4. 3: $g_{ms}$ vs. $V_G$ plot of different temperatures. ....	74
Figure 5. 1: The device structure of the delta-doped MOS-gate SiGe HEMT. ....	79
Figure 5. 2: The device schematic, charge distribution and band diagram used to derive $V_{THp}$ expression.....	80
Figure 5. 3: (a) $d_1$ vs. $V_{THp}$ plot and (b) $d_1$ vs. $V_{tl}$ plot of the p-channel delta-doped.....	86
Figure 5. 4: (a) $\delta$ vs. $V_{THp}$ plot and (b) $\delta$ vs. $V_{tl}$ plot of the p-channel delta-doped.....	88
Figure 6. 1: <i>Medici</i> <sup>TM</sup> simulation result used to determine $V_{THp}$ and $V_{Gmin}$ . ....	92
Figure 6. 2: (a) Comparison of $I_{Dsat}$ - $V_G$ plot obtained from analytical model and <i>Medici</i> Simulation and (b) $I_D$ - $V_D$ plot from <i>Medici</i> <sup>TM</sup> . ....	93
Figure 6. 3: $I_D$ - $V_G$ characteristics of the p-channel SiGe MOS-gate for different supply layer doping concentrations. ....	96

Figure 6. 4: Temperature Variation of $V_{THp}$ measured from $I_D$ - $V_G$ plots at different temperatures.....	98
Figure 6. 5: Comparison of $I_D$ - $V_D$ characteristics at different temperatures, obtained from <i>Medici</i> <sup>TM</sup> simulation.....	99
Figure 6. 6: <i>Medici</i> <sup>TM</sup> simulation results used to determine $V_{THp}$ and $V_{tl}$ for the p-channel delta-doped SiGe MOS-gate HEMT.....	101

# Chapter 1

## *Introduction*

### **1.1 Background**

In recent years the increasing need for high-speed communication and computation has pushed silicon-based MOSFET technology to the edge. To meet the ever-increasing speed requirement, the gate length of the MOSFET has been continually reduced. The gate length of the MOSFET has reached such small dimension that several detrimental effects are taking place in the MOSFET. The overall behavior of the short channel MOSFET is quite different from the long channel MOSFET. In this situation, scientists and engineers are constantly looking for new materials as well as new device structures that can replace silicon-based MOSFETs and cope up with the speed requirement.

### **1.2 Limitations of Silicon-Based MOSFET with Short Channel**

The short channel device is distinguished from a long channel device by the following criteria [1]:

1. In short channel device, the drain current no longer varies as  $1/(\text{gate length})$ .
2. The threshold voltage decreases.
3. The gate voltage required to reduce the sub-threshold current becomes larger.

Various effects occur due to the shrinking of the gate length and oxide thickness, which are known as “short channel effects”. The gate length at which the short channel effects starts to take place depends on the device dimensions, doping and other device parameters. Some of the short channel effects are described below:

- *Hot Carriers*: As the gate length of the short channel MOSFET is very small, the critical electric field is reached for small drain-source voltage. Velocity saturation occurs above the critical electric field. The carriers traveling at the saturation velocity  $v_s$  are called the hot carriers. These hot carriers can get trapped in the gate oxide and change the threshold voltage of the MOSFET. Also, they can tunnel through the gate oxide (as the gate oxide of short channel MOSFET is thin) and cause gate leakage current.
- *Drain- Induced Barrier Lowering (DIBL)*: For an n-type MOSFET, the positive potential at the drain terminal attracts electrons under the gate oxide. In short channel devices, these electrons cause lowering of the potential barrier between the drain and the source. Thus, as the drain-source voltage increases, potential barrier in the channel decreases. Eventually this reduction in the potential barrier causes current flow between drain and source even at a gate voltage lower than the threshold voltage. This current is called subthreshold current.
- *Oxide Breakdown*: Maximum electric field across a MOSFET gate oxide should be limited to 7MV/cm [2]. Thus, to prevent possible oxide breakdown and ensure

long-term operation, the gate bias is limited by a maximum value. The oxide thickness in a short channel MOSFET is usually small. As a result, the maximum permissible gate voltage is small for a short channel MOSFET.

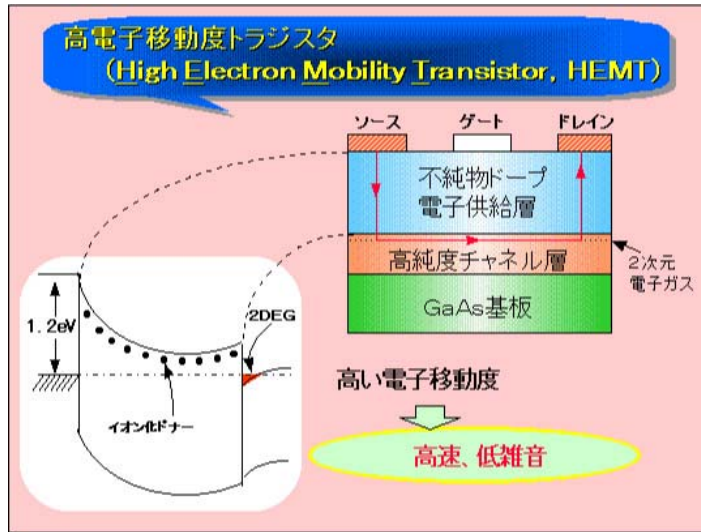
- *Relationship between drain current and gate voltage:* In long channel MOSFET, the drain current in saturation region is proportional to the square of the gate-source voltage. For the short channel, this theory does not apply. The saturation drain current varies linearly with the gate-source voltage. This effect is the result of the velocity saturation of the channel carriers.

### **1.3 HEMT: A Light of Hope**

High Electron Mobility Transistor (HEMT) was invented in the beginning of 1980's. The HEMT is basically a high-speed heterojunction device, which uses two-dimensional electron or hole gas trapped in a quantum well as the carrier. The structure of the HEMT is such that the carriers in the channel are far from the ionized dopant atoms. Thus, the carriers encounter small Coulombic interaction with the ionized dopant atoms and the carrier mobility is increased.

The formation of the quantum well in the HEMT restricts the carrier movement to only two dimensions. This is another reason why the carriers in the channel acquire high mobility. Figure 1.1 [3] shows the first HEMT fabricated by Fujitsu Corp, Japan. This is





**Figure 1. 1: The first HEMT, fabricated by Fujitsu Corp in Japan [3].**

a Schottky-gate GaAs/AlGaAs HEMT. The band diagram and device cross section are also shown in the figure.

## 1.4 MOS-Gate HEMT

Integration of the HEMT into the CMOS microelectronic circuits is a very important step that can enable us to use the excellent properties of the HEMT. Research efforts are going on to make this integration possible. One of the difficulties of integration is the fact that the traditional HEMT uses a Schottky gate. On the other hand, the CMOS circuits use oxide-gate devices such as the MOSFET. To solve this problem, research efforts have been driven to design and fabricate an oxide-gate HEMT. Most of the HEMTs fabricated in the early days used GaAs and AlGaAs. But GaAs or AlGaAs do not have a native oxide. On the other hand,  $\text{SiO}_2$  possesses attractive properties that made it suitable for

microelectronic integration. To utilize  $\text{SiO}_2$  as the gate oxide of the HEMT device, Si based material technology is incorporated in the design of the MOS-gate HEMT. As a result, the MOS-gate HEMT has been fabricated by growing  $\text{SiO}_2$  on top of the Si/SiGe heterostructure [4].

## **1.5 SiGe MOS-Gate HEMT**

The SiGe MOS-gate HEMT demonstrates quite a few advantages over the traditional Schottky-Gate HEMT. Some of the advantages are listed below:

- The MOS-gate HEMT has high input resistance like the MOSFET.
- The MOS-gate HEMT is capable of accepting a wider range of gate voltage swing than the Schottky-gate HEMT. For example, an n-channel Schottky-gate HEMT can accept only negative gate voltage. On the other hand, an n-channel MOS-gate HEMT can accept both positive and negative gate bias.
- The gate voltage operating range of a MOS-gate HEMT can be controlled by varying the thickness of the oxide layer.

Although fabrication of a MOS-gate HEMT is one step toward the integration of a HEMT into mainstream CMOS integrated circuits, more research challenges remain. The HEMT has multiple layers and the number of layers is more than that of a conventional

MOSFET. That makes it unsuitable for the conventional CMOS process, which deals with only a few layers. Also, there are still some problems associated with the growth of oxide in the MOS-gate SiGe HEMTs. These will be discussed in the next chapter.

## 1.6 Proposed Work

In recent years, the HEMT has been subjected to lot of research efforts in various material system including SiGe. SiGe HEMT is one of the hot topics. The SiGe HEMTs can be broadly classified into two groups: the Schottky-gate SiGe HEMT and the MOS-gate SiGe HEMT. Due to some fabrication difficulties of the MOS-gate HEMT, more research efforts have been devoted to Schottky-gate HEMT. But efforts have been made to solve the fabrication problems of the MOS-gate HEMT and researchers have come up with some possible solutions.

Quite a few research groups around the world are working on the SiGe MOS gate HEMT. Most of the works concentrate on fabrication and experimental characterization of MOS gate HEMTs. Not much work has been devoted to the analytical modeling and simulation of these devices. A reliable device model is very important in device design and in predicting the behavior of an existing device. The analytical model can be used as the first tool in device design, which is able to provide a rough, if not very accurate, idea about the behavior of the device to be designed. As a second step of the design process, numerical simulation software such as *Medici<sup>TM</sup>*, *Davinci<sup>TM</sup>*, *Atlas<sup>TM</sup>*, etc. can be used

Analytical modeling of the MOS-gate HEMT is the main scope of this research work. Also, device simulator *Medici*<sup>TM</sup> has been used to compare the results obtained from these analytical models. The main research goals of this thesis are to: (1) propose a modified analytical model for calculating the threshold voltage  $V_{TH}$  and the minimum gate voltage  $V_{Gmin}$  of a p-channel MOS-gate HEMT, (2) calculate the current-voltage characteristics using the modified model, (3) examine the effects of different device and material parameters on  $V_{TH}$  and  $V_{Gmin}$ , using the modified analytical model, (4) introduce an analytical model to predict the temperature dependency of  $V_{TH}$  and the current-voltage characteristics of the MOS-gate HEMT, (5) propose a modified threshold voltage model for the delta-doped MOS-gate HEMT (6) derive the expression for the minimum gate voltage  $V_{tl}$  of delta-doped MOS-gate HEMT, (7) examine the effects of some device parameters on  $V_{TH}$  and  $V_{tl}$  of the delta-doped HEMT, (8) perform *Medici*<sup>TM</sup> simulations of the MOS-gate HEMT to investigate device behavior as well as compare the results obtained from the analytical model to the results of the *Medici*<sup>TM</sup> simulations.

The p-channel MOS-gate SiGe HEMT has been used in the analytical models and the *Medici*<sup>TM</sup> simulations. But the analytical models can be extended to other MOS-gate HEMTs with similar structure including the n-channel MOS-gate SiGe HEMT.

## **1.7 Outline of the Thesis**

Chapter 2 presents a review of the literature that includes: HEMT, SiGe material properties and recent works on SiGe MOS-gate HEMT.

Chapter 3 starts with the discussion of the existing model of the MOS-gate HEMT. Then, a modified model is proposed, and  $V_{THp}$ ,  $V_{Gmin}$ , current voltage characteristics, transconductance and cutoff frequency are calculated using the modified model. The results obtained from two models are compared. The last part of this chapter examines the effect of different device and material parameters on  $V_{THp}$  and  $V_{Gmin}$ .

A simple temperature model for the MOS-gate HEMT is introduced in Chapter 4. The effects of temperature variation on threshold voltage, current voltage characteristics and transconductance of the MOS-gate HEMT are investigated using the temperature model.

A modified threshold voltage model for the delta-doped MOS-gate HEMT has been proposed in Chapter 5 that can be applicable to any width of delta-doped layer as well as any distance of the layer from the oxide interface. An expression of the minimum gate voltage  $V_{tl}$  for the delta-doped HEMT has been derived and its value is calculated using a p-channel SiGe delta-doped MOS-gate HEMT. The effects of doping concentration, distance of the delta-doped layer from oxide interface and width of the delta-doped layer on  $V_{THp}$  and  $V_{tl}$  have been examined using the model.

Chapter 6 consists of the *Medici*<sup>TM</sup> simulations of the regular-doped and the delta-doped SiGe MOS gate HEMT. These simulations have been used to explore the device behavior as well as the simulation results have been compared to some of the results obtained from the analytical models.

Chapter 7 summarizes the work done in the thesis. Also, it includes the discussion of the future work directions that may help to improve the analytical models.

## Chapter 2

### *Literature Review*

#### **2.1 HEMT**

##### ***2.1.1 What is HEMT***

HEMT (High Electron Mobility Transistor) is a heterojunction device that uses the carriers in 2DEG or 2DHG for current transport. It is one of the fastest solid-state devices ever reported. The name HEMT was proposed by Fujitsu Corp. Japan. Some other names of the HEMT, proposed by different laboratories are: the MODFET (Modulation-Doped FET) (Univ. of Illinois), the TEGFET (Two-Dimensional Electron-Gas FET) (Thomson CSF), the SDHT (Selectively-Doped Heterojunction Transistor) (Bell Labs.) and the HFET (Heterojunction FET).

##### ***2.1.2 GaAs/AlGaAs HEMT***

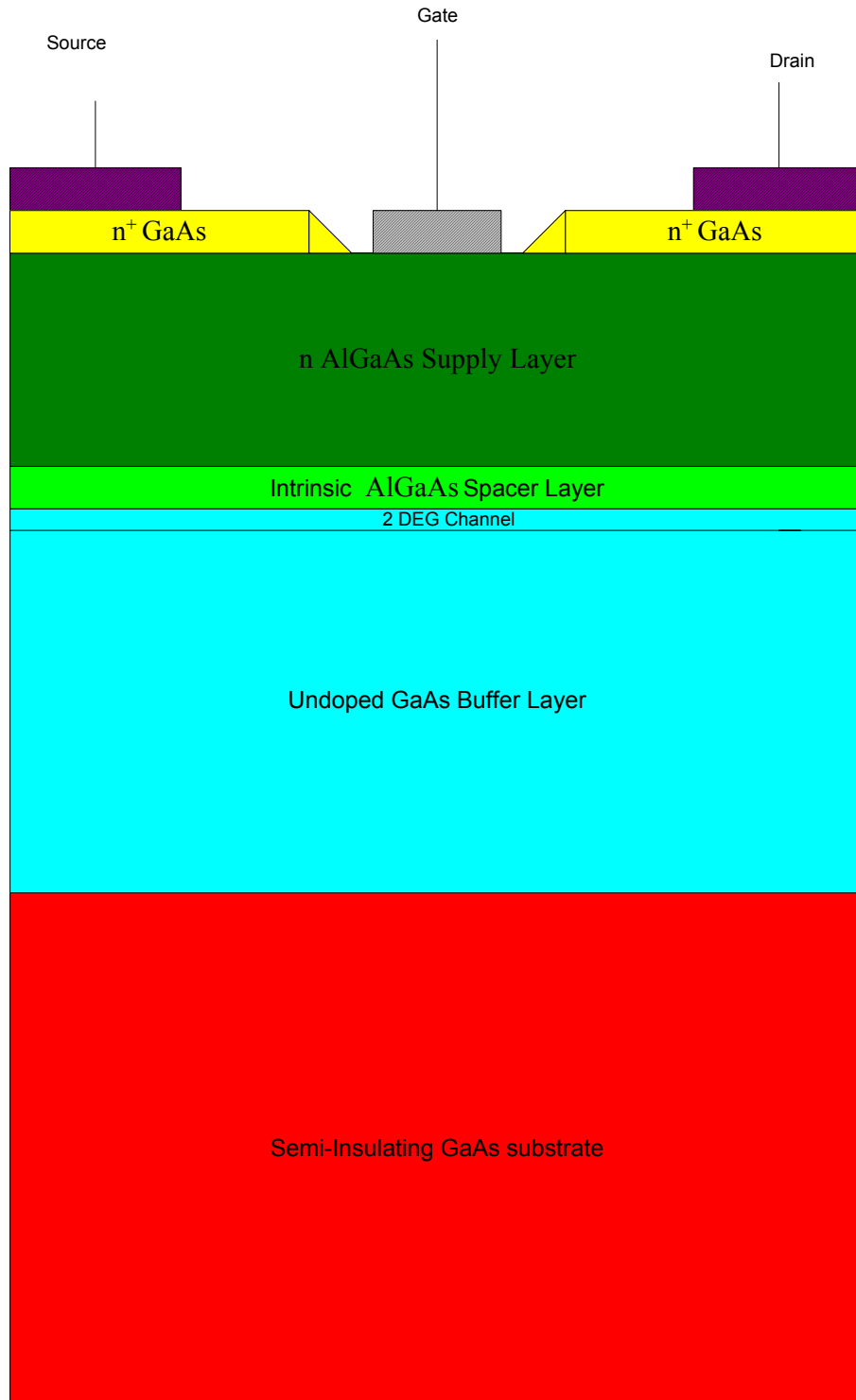
The first HEMT was fabricated using the compound semiconductors GaAs and AlGaAs [3]. Later, HEMTs have been fabricated using different material systems such as AlInAs/GaInAs [5], Si/SiGe [6], etc. AlGaAs has almost perfect lattice match with GaAs for all the possible mole fraction of Al. Thus, a high quality epitaxial layer of AlGaAs can be grown on GaAs substrate.

Figure 2.1 shows a typical structure of an n-channel GaAs/AlGaAs HEMT. There exists discontinuity in both the conduction band and the valence band at the GaAs/AlGaAs heterointerface. Electrons diffuse from the highly doped AlGaAs region to the undoped GaAs region and they are trapped in the almost triangular shaped quantum well formed in the interface at the GaAs side. The motions of these electrons are restricted to two dimensions as they are not free to move in the direction normal to the heterointerface. The widths of the quantum well being very thin, the electron energies in the well are quantized. The two lowest subbands are mostly occupied and only they are included in the calculation of electron density.

As the electron motions are confined to only two directions, the mobility of the electrons is certainly higher than that of the bulk material. Another reason behind the mobility enhancement is the distance of the electrons in the channel from the ionized dopant impurities [7]. The electrons in the channel encounter much less Coulomb scattering than the electrons in a typical MOSFET channel. Although at room temperature, the mobility is limited by optical phonon scattering, it can attain very high value at low temperature. The electron mobility at 100 K can be as high as twenty times of the mobility at room temperature [8].

For normal operation, the supply layer is totally depleted due to the gate voltage and the depletion at the AlGaAs/GaAs heterostructure. Thus, when voltage is applied between drain and source, conduction can only take place through the 2DEG channel formed in the GaAs layer. There exist two limits of the applied gate bias: the threshold voltage  $V_{TH}$





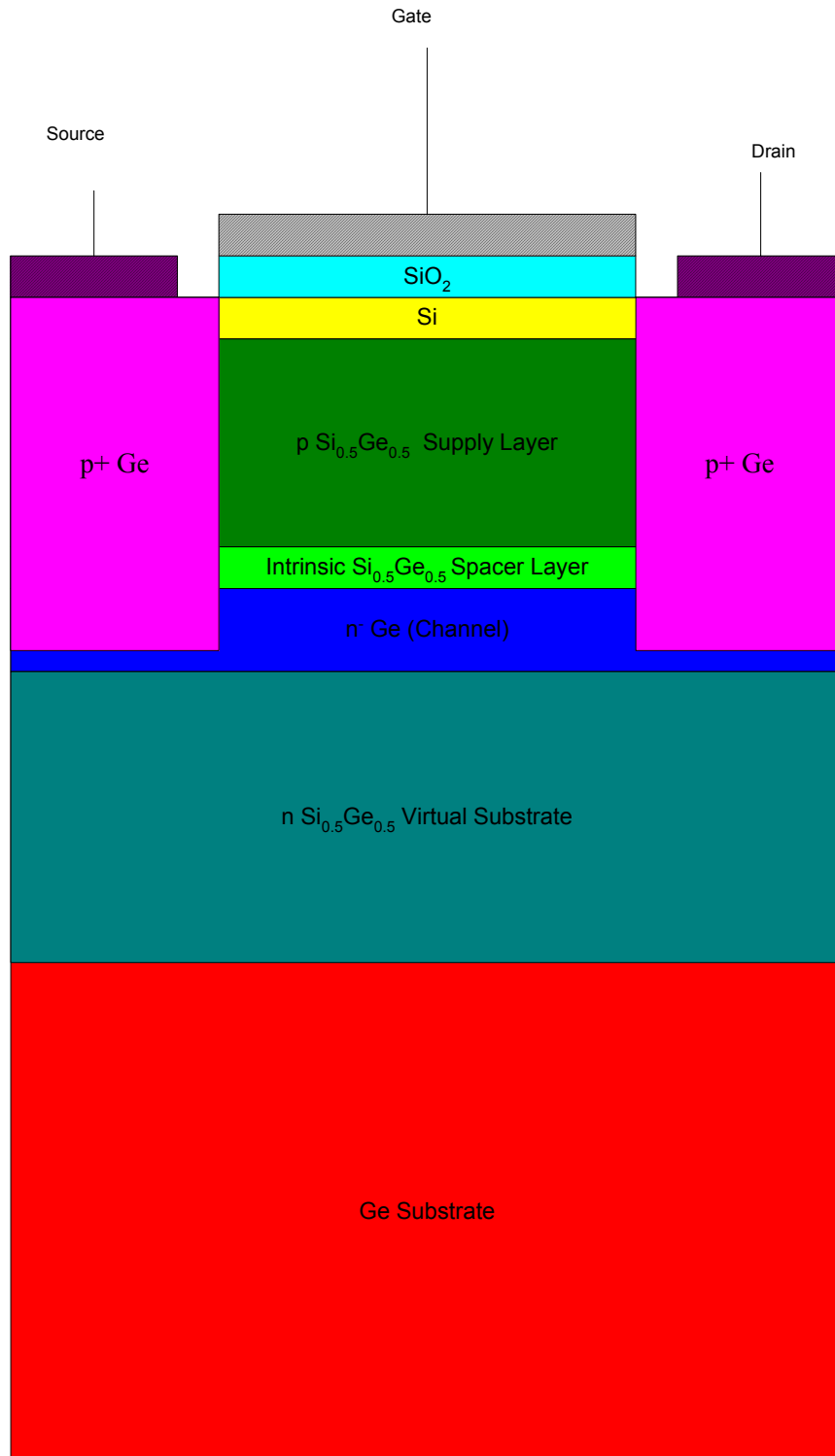
**Figure 2. 1: The cross-sectional view of a GaAs/AlGaAs n-channel HEMT.**

and the minimum gate voltage  $V_{Gmin}$  (for p-channel HEMT) or the maximum gate voltage  $V_{Gmax}$  (for n-channel HEMT). The threshold voltage is defined as the gate voltage, which causes total depletion in the channel. Thus, above (for p-channel HEMT) or below (for n-channel HEMT) the gate voltage value of  $V_{TH}$ , the HEMT is turned off. Again, at the gate voltage value of  $V_{Gmax}$  or  $V_{Gmin}$ , the supply layer is not anymore fully depleted. As a result, conduction parallel to the channel takes place in the AlGaAs region. This parallel conduction reduces the gate transconductance. For normal operation, the gate bias of the HEMT is kept within the range:  $V_{Gmin} < V_G < V_{TH}$  (for p-channel HEMT) or  $V_{TH} < V_G < V_{Gmax}$  (for n-channel HEMT).

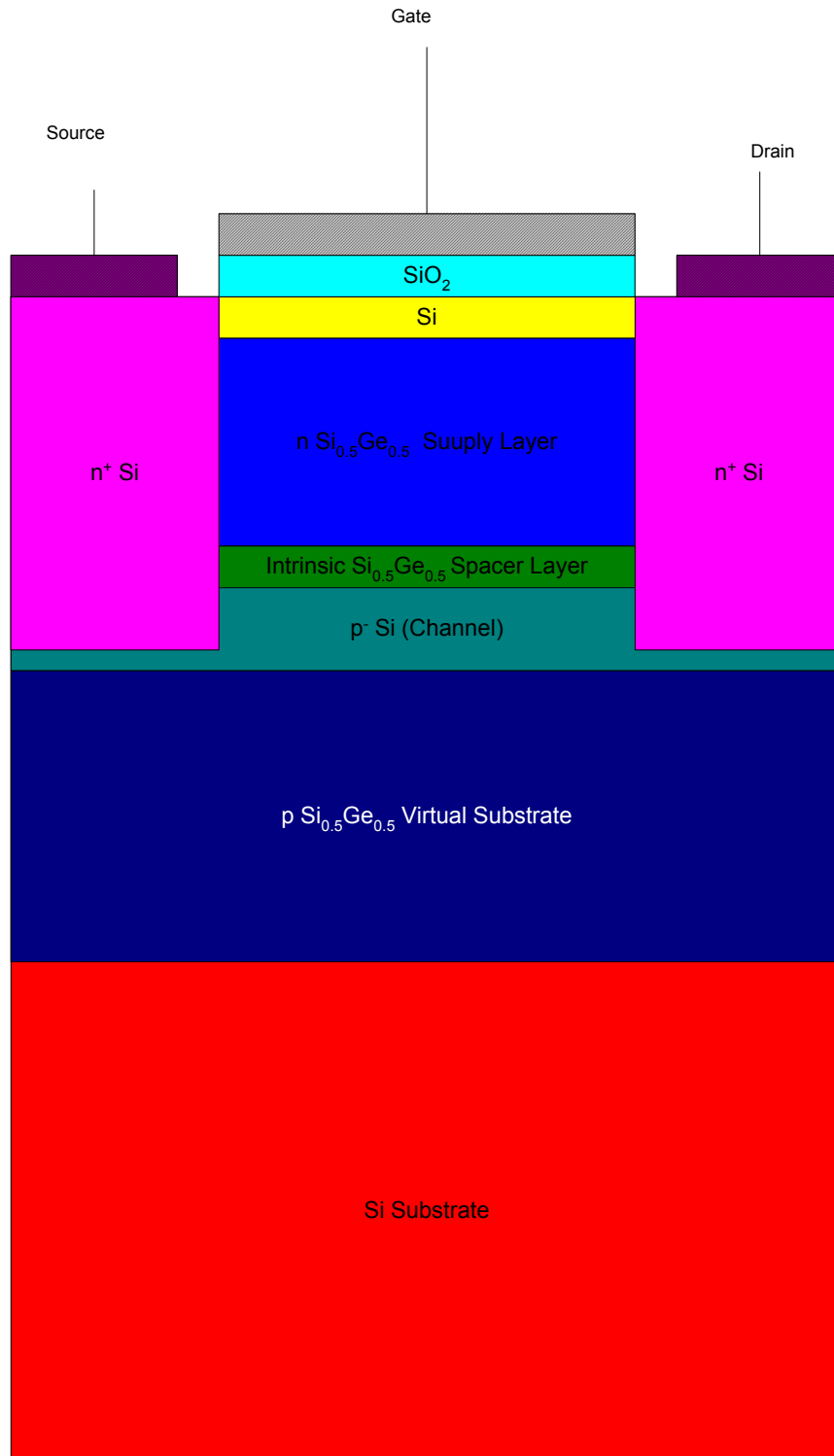
### ***2.1.3 SiGe MOS- gate HEMT***

As discussed in the previous chapter, the realization of the MOS-gate HEMT is a significant leap towards the integration of HEMT into mainstream CMOS monolithic integrated circuits.  $SiO_2$ , being a tested oxide in integrated circuits, has naturally become the choice for the gate oxide of the MOS-gate HEMT. As  $SiO_2$  is the native oxide of silicon, the MOS gate HEMT has been realized in the SiGe material system [4].

Figure 2.2 shows a p-channel MOS-gate HEMT while Figure 2.3 shows an n-channel MOS-gate HEMT. The operation of the MOS-gate HEMT is very similar to that of the Schottky-gate (metal-gate) HEMT. The silicon layer at the top of the SiGe supply layer is needed for growing  $SiO_2$  on the top. The SiGe buffer layer between the substrate and the channel is called the virtual substrate.



**Figure 2. 2: The cross-sectional view of a p-channel SiGe MOS-gate HEMT.**



**Figure 2. 3: The cross-sectional view of an n-channel SiGe MOS-gate HEMT.**

The virtual substrate plays a very important role in the strained SiGe material system. The thick and strain relaxed layer of SiGe virtual substrate is grown on the substrate (Si or Ge). Then, (for p-channel HEMT shown in figure 2.2) thin strained layers of Ge and  $\text{Si}_{0.5}\text{Ge}_{0.05}$  is grown commensurately on top of the buffer layer [4]. The strain on the Ge and  $\text{Si}_{0.5}\text{Ge}_{0.05}$  layers and most of the material properties of the strained Ge and  $\text{Si}_{0.5}\text{Ge}_{0.05}$  layers depend on the x value of the  $\text{Si}_{1-x}\text{Ge}_x$  virtual substrate. Thus, composition of the virtual substrate controls the size of the band discontinuity and the quantum well formed in the heterointerface. Also, the virtual substrate helps better confinement of the carriers in the quantum well.

## **2.2 Properties of SiGe and Si/SiGe Heterostructure**

SiGe material properties and the behavior of Si/SiGe heterostructure play a very important role in the performance of the SiGe MOS-gate HEMT. In this section, some of the important material properties of bulk and strained SiGe, and Si/SiGe heterostructure will be briefly discussed.

The band structure of  $\text{Si}_{1-x}\text{Ge}_x$  is similar to that of Si for  $x < 0.85$ . For  $x > 0.85$ , the material demonstrates Ge-like character with a conduction band L minima [9]. Thus, the bandgap (the distance between the minimum of the conduction band and the maximum of the valence band) of the  $\text{Si}_{1-x}\text{Ge}_x$  varies with composition. Also, when the heterostructure between SiGe and Si or Ge is formed, the bandgap is changed due to strain.

The conduction band or the valence band offset is an important parameter to be considered in a heterostructure. In the p-channel HEMT, large valence band offset is expected. On the other hand, large conduction band offset is required in an n-channel device. Not many results are available for the Si/SiGe conduction band offset. But, lots of work has been reported on theoretical and experimental studies of the valence band offset in this system [10] [11]. Obviously, the band structures and thus the band offsets are crystallographic orientation dependent. For <100> SiGe heterostructure, in the case of the strained  $\text{Si}_{1-x}\text{Ge}_x$  grown on the relaxed  $\text{Si}_{1-y}\text{Ge}_y$  virtual substrate, an average valence band offset expression proposed by Rieger and Vogl [10] is given by,

$$\Delta E_{v,av} = (0.47 - 0.06y)(x - y) \dots\dots\dots 2.1$$

This valence band offset is calculated considering only the hydrostatic strain. Consideration of the effect of the uniaxial strain components will provide more accurate results.

As mentioned before, the bandgap of SiGe depends on the strain resulted from the pseudomorphic growth. Also, the bandgap is a function of temperature. For unstrained  $\text{Si}_{1-y}\text{Ge}_y$ , the bandgap at 4.2 K is given by [12],

$$E_g(y, 4.2K) = 1.115 - 0.43y + 0.206y^2, y < 0.85 \dots\dots\dots 2.2$$

To predict the bandgap of the  $\text{Si}_{1-y}\text{Ge}_y$  at higher temperature, Si-like bandgap-temperature relation is used [13],

$$E_g(y,T) = E_g(y,0K) - \frac{4.73 \times 10^{-4} T^2}{T + 636} \dots\dots\dots 2.3$$

Assuming that, the bandgap at 0 K is almost equal to that at 4.2 K,

$$E_g(y,T) = E_g(y,4.2K) - \frac{4.73 \times 10^{-4} T^2}{T + 636} \dots\dots\dots 2.4$$

Equation 2.4 can be used to estimate the bandgap of the unstrained Si<sub>1-y</sub>Ge<sub>y</sub> for any composition smaller than 0.85 and at any temperature.

For the strained Si<sub>1-x</sub>Ge<sub>x</sub>, the bandgap can be estimated [14] using the following equation,

$$E_g(x,4.2K) = 1.17 - 0.896x + 0.396x^2 \dots\dots\dots 2.5$$

To estimate the temperature dependence of the bandgap of the strained Si<sub>1-x</sub>Ge<sub>x</sub>, equation 2.4 (y replaced by x) can be used. Table 2.1 shows some important parameters of bulk Si<sub>1-y</sub>Ge<sub>y</sub> material at 300 K [15].

### **2.3 Development of SiGe MOS-Gate HEMT**

Although there still exists some difficulty in the fabrication process of SiGe MOS-gate HEMT, due to its attractive features compared to the Schottky-gate HEMT, quite a few research groups around the world are working on it. Some of the research results reported in recent years will be discussed in this section.

**Table2.1: Basic parameters of bulk Si<sub>1-y</sub>Ge<sub>y</sub>, at 300 K.**

Parameter Name	Value
Dielectric Constant	11.7+4.5y
Effective Electron Mass (in units of m <sub>0</sub> )	~0.92 for y<0.85, ~1.59 for y>0.85
Electron Affinity (eV)	4.05-0.05y
Lattice Constant (Å)	5.431+0.2y+0.027y <sup>2</sup>
Electron Mobility (cm <sup>2</sup> /V-s)	1450-4325y, 0 ≤ y < 0.3
Hole Mobility (cm <sup>2</sup> /V-s)	450-865y, 0 ≤ y < 0.3
Electron Diffusion Coefficient (cm <sup>2</sup> /s)	36-112y, 0 ≤ y < 0.3
Hole Diffusion Coefficient (cm <sup>2</sup> /s)	12-22y, 0 ≤ y < 0.3
Electron Thermal Velocity (cm/s)	2.4X10 <sup>7</sup> , y<0.85 3.1X10 <sup>7</sup> , y>0.85
Hole Thermal Velocity (cm/s)	1.65+0.25y



In 1991, Murakami et al [4] reported the fabrication and characterization of strain-controlled SiGe delta-doped MOS-gate HEMT. Very high hole mobility has been obtained in the 2DHG formed in the strain-controlled Ge channel. Field effect mobility as high as  $9500 \text{ cm}^2/\text{V}\cdot\text{s}$  is estimated from the measurements conducted at 77 K.

In 1992, Jain et al [16] proposed an analytical model for the SiGe MOS-gate HEMT. In this work, a threshold voltage expression for the MOS-gate HEMT has been derived and the threshold voltage has been calculated for a p-channel SiGe MOS-gate HEMT. Current-voltage characteristics, transconductance and cutoff frequency for the HEMT are also calculated using this model along with Chang-Fetterman's extended model [17].

In a work published in 2000, Lu et al [18] have reported the fabrication and characterization of a  $0.1 \mu\text{m}$  gate length p-type SiGe Schottky-gate HEMT and a MOS-gate HEMT. In their work, they have pointed out two important problems in the fabrication of SiGe MOS-gate HEMT: (1) high density of interface states of oxides formed on SiGe and (2) Ge segregation caused by the high temperature oxide processing. They have compared two SiGe HEMTs of similar dimensions: one with MOS gate and the other with Schottky gate. The comparison shows that the MOS-gate HEMT has a wider gate voltage swing and lower leakage current than its counterpart.

V. Gaspari et al [19] have investigated the effect of temperature on the transfer characteristics of an n-channel Si/SiGe MOS-gate HEMT. They have experimentally measured the extrinsic transconductance for different gate voltages at different

temperature ranging from 180 K to 300 K. It has been found that at low temperature the off current is reduced and the subthreshold slope becomes steeper. Their experimental results have been compared with *Medici*<sup>TM</sup> simulation results. This work was published in 2004.

Velázquez et al [20] have reported the “design of nearly body effect free” Si/SiGe n-channel HEMT. They have numerically studied the effect of doping of the setback layer and designed the doping profile in such a way that the effect of the substrate bias is substantially reduced. They have also used *Medici*<sup>TM</sup> and compared the simulation results with results obtained from the experiments.

## Chapter 3

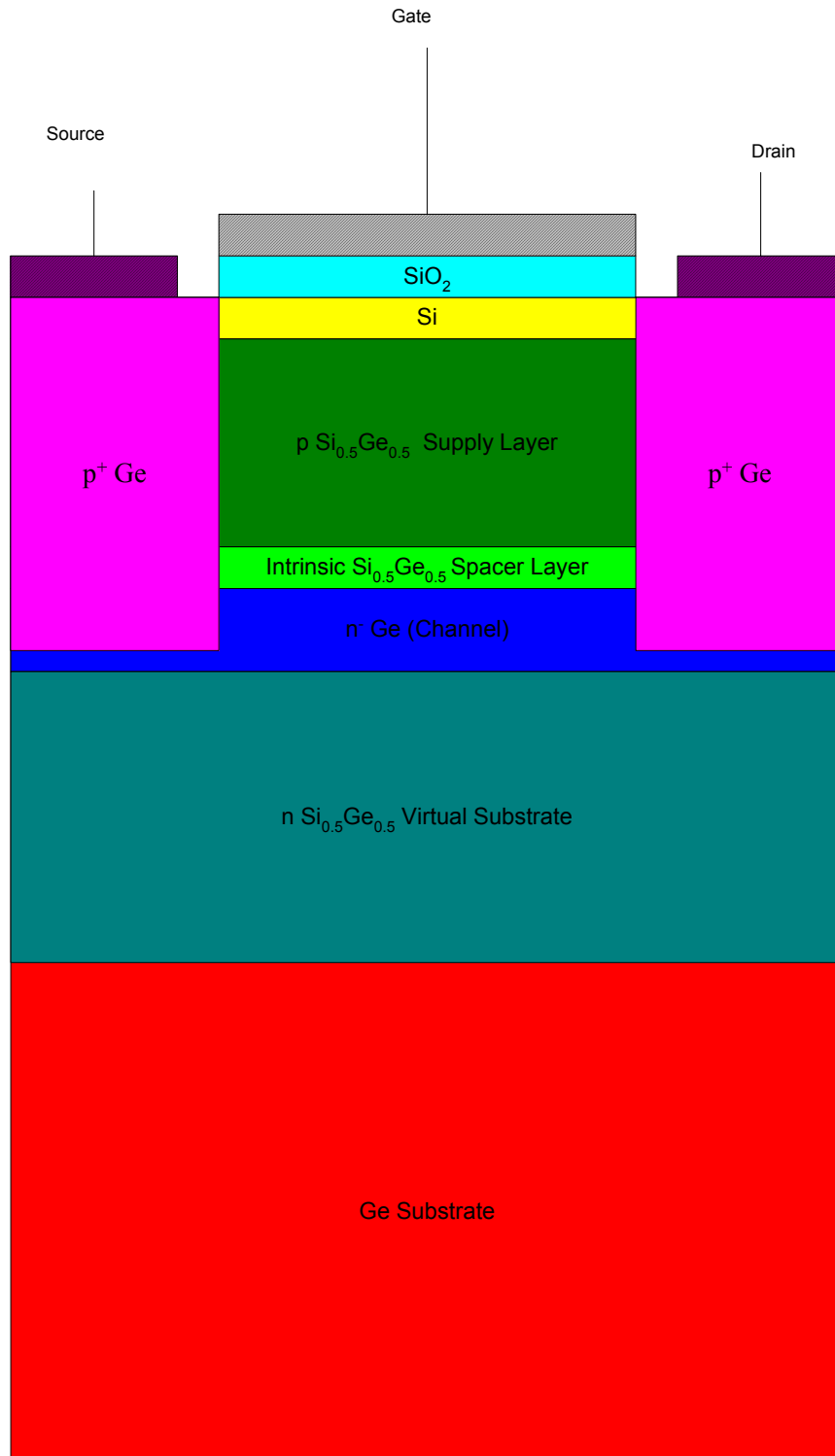
### *Modified Model for MOS-Gate SiGe HEMT*

In this chapter, different aspects of the analytical modeling of the SiGe MOS-gate HEMT will be discussed. Mostly, the analyses and discussions will be limited to the p-channel MOS-gate HEMT. The analysis of the n-channel MOS-gate HEMT can be performed in a similar fashion. At first, the analytical model proposed by Jain et al [16] will be discussed. Then, the modified model including the effect of the silicon cap layer will be proposed and the results obtained from the two models will be compared. Last part of this chapter consists of the simulation results and analyses of the effects of the change of different device and material parameters using the modified model.

### **3.1 Existing Model for the MOS-Gate HEMT**

#### *3.1.1 The threshold voltage expression*

A threshold voltage expression for the MOS-gate HEMT has been reported in [16]. In this work, a p-channel SiGe MOS-gate HEMT has been used to derive the threshold voltage equation. The structure of the device is shown in Figure 3.1. This structure combines a conventional MOSFET with the HEMT structure. The p-channel SiGe MOS-gate HEMT consists of a  $\text{Si}_{0.5}\text{Ge}_{0.5}$  (p-type) supply layer, an intrinsic  $\text{Si}_{0.5}\text{Ge}_{0.5}$  spacer



**Figure 3. 1: Cross-sectional schematic of a p-Channel SiGe MOS-gate HEMT.**

layer, an n<sup>-</sup>-Ge channel, a Si<sub>0.25</sub>Ge<sub>0.75</sub> virtual substrate and a Ge substrate. Also, a thin layer of silicon is used on the top of the supply layer, which is called silicon cap. The purpose of this layer is to grow the SiO<sub>2</sub> layer on the top. On the top of the gate oxide, the gate metal is deposited, which is Aluminum in this case.

The threshold voltage expression in [16] has been derived without considering the effect of the silicon cap layer. The device structure, charge distribution and energy band diagram used in the derivation is shown in Figure 3.2. In this derivation, d<sub>d</sub>, the width of the supply layer is defined as the distance from the oxide/silicon interface to the supply layer/spacer layer interface. The charge accumulated in the metal gate due to the applied gate voltage V<sub>G</sub> is compensated by part of the charge in the depletion layer of the Si<sub>0.5</sub>Ge<sub>0.5</sub> supply layer. This charge is termed as Q<sub>d</sub>. The rest of the charge in the depletion layer is compensated by the charge in the two dimensional hole gas (2DEG) and a small charge due to the depletion layer formed in the Ge channel.

The derivation starts with the equation,

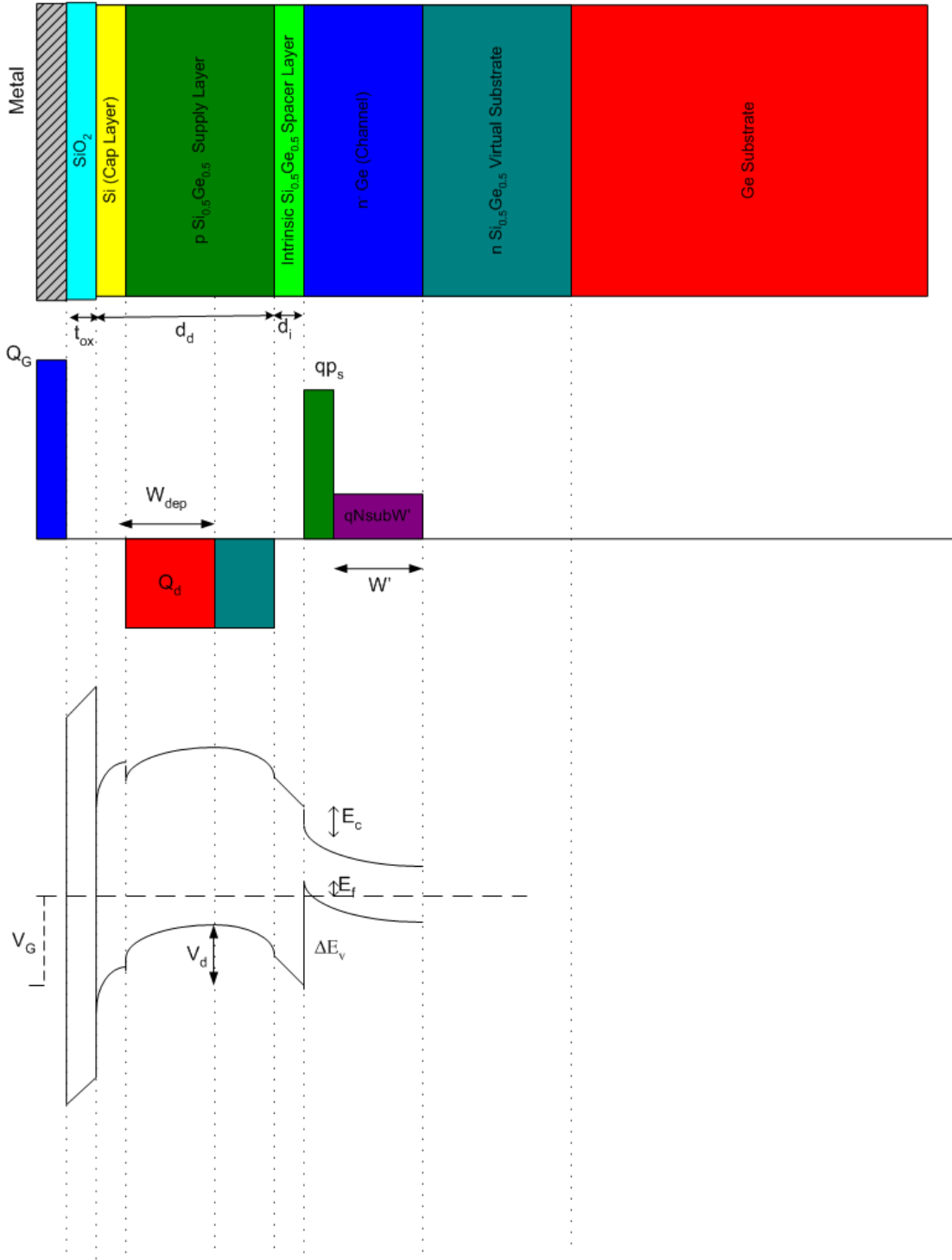
$$V_G = V_{FB} + \frac{Q_D}{C_{ox}} + \psi_s \dots\dots\dots 3.1$$

where, V<sub>G</sub> is the applied gate voltage,

V<sub>FB</sub> is the flatband voltage

ψ<sub>s</sub> is the surface potential,

C<sub>ox</sub> is the oxide capacitance.



**Figure 3. 2: Device schematic, charge distribution and energy band diagram of the p-channel MOS-gate HEMT.**

Using the depletion approximation, the expressions for  $\psi_s$  and  $Q_d$  are found as,

$$\psi_s = \frac{qN_2}{2\epsilon_2} W_{dep}^2 \dots\dots\dots 3.2$$

$$Q_d = qN_2 W_{dep} \dots\dots\dots 3.3$$

where,  $N_2$  is the doping density in the  $Si_{0.5}Ge_{0.5}$  supply layer,

$\epsilon_2$  is the permittivity of the  $Si_{0.5}Ge_{0.5}$  supply layer = 13.95  $\epsilon_0$ ,

$\epsilon_0$  is the permittivity of the free space.

The expression for  $V_{FB}$  is given by,

$$V_{FB} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}} \dots\dots\dots 3.4$$

$\phi_{ms}$  is the difference between the metal and the semiconductor ( $Si_{0.5}Ge_{0.5}$ ) work function, which is given by,

$$\phi_{ms} = \phi_m - [\chi_2 + \frac{E_{g2}}{q} - (\frac{\Delta E_v}{q} - V_d - \frac{E_f}{q})] \dots\dots\dots 3.5$$

where,  $\chi_2$  is the electron affinity of the semiconductor,

$\Phi_m$  is the metal work function,

$\Delta E_v$  is the valence band discontinuity at the  $Si_{0.5}Ge_{0.5}/Ge$  Interface,

$V_d$  is the potential difference between the maximum of the valence band and the bottom of the valence band discontinuity,

$E_{g2}$  is the band gap of  $Si_{0.5}Ge_{0.5}$ ,

$E_f$  is the Fermi level measured for the top of the valence band discontinuity.

Again,  $V_d$  is expressed in terms of  $\rho_s$  as,

$$V_d = \frac{q\rho_s^2}{2\varepsilon_2 N_2} + \frac{q\rho_s d_i}{\varepsilon_2} \dots\dots\dots 3.6$$

Two other useful relations used in the derivation are,

$$x_m = \frac{\rho_s}{N_2} + d_i \dots\dots\dots 3.7$$

$$\text{and, } W_{dep} = (d_d + d_i) - x_m \dots\dots\dots 3.8$$

Using equations 3.1 through 3.8, the final charge control equation can be derived. The charge control equation is given by,

$$\rho_s = -\frac{C_{eq}}{q} [V_G - V_{THp}] \dots\dots\dots 3.9$$

$$\text{where, } \frac{1}{C_{eq}} = \frac{d_d + d_i + \Delta d}{\varepsilon_2},$$

$$\Delta d = \frac{a\varepsilon_2}{q}.$$

$V_{THp}$  is the threshold voltage. The expression of  $V_{THp}$  is given by,

$$V_{THp} = \phi_m - \chi_2 - \frac{E_{g2}}{q} + \frac{\Delta E_v}{q} - \frac{\Delta E_{f_0}}{q} - \frac{Q_{ox}}{C_{ox}} + \frac{qN_2 d_d}{C_{ox}} + \frac{qN_2 d_d^2}{2\varepsilon_2} \dots\dots\dots 3.10$$

The expression for the n-channel MOS-gate HEMT can be derived in similar fashion and is given by,



$$V_{THn} = \phi_m - \chi_2 - \frac{\Delta E_c}{q} + \frac{\Delta E_{f_0}}{q} - \frac{Q_{ox}}{C_{ox}} - \frac{qN_2d_d}{C_{ox}} - \frac{qN_2d_d^2}{2\epsilon_2} \dots\dots\dots 3.11$$

### 3.1.2 Calculation of $V_{THp}$

The threshold voltage for the MOS-gate HEMT shown in figure 3.1 will be calculated now. The device and material parameters used to calculate the threshold voltage is listed in table 3.1. All the parameters are for 300 K. Some of the parameter values are not same as the ones used in the work of Jain et al [16]. One of the reasons behind the differences is the fact that the calculations performed in [16] were for 77 K instead of 300 K.

The electron affinity of  $Si_{0.5}Ge_{0.5}$  is calculated using the following relation [15],

$$\chi_2 = 4.05 - 0.05x \dots\dots\dots 3.12$$

where, x is the mole fraction in  $Si_{1-x}Ge_x$ .

The bandgap of the strained  $Si_{0.5}Ge_{0.5}$  at 300 K is calculated using the following equations [12]

$$E_{g_2}(x, 4.2K) = 1.17 - 0.896x + 0.396x^2 \dots\dots\dots 3.13$$

$$E_{g_2}(x, T) = E_{g_2}(x, 0K) - \frac{4.73 \times 10^{-4} T^2}{T + 636} \dots\dots\dots 3.14$$

Here, it is assumed that the band gap at 0 K is almost same as the bandgap at 4 K.

**Table 3. 1: Device and material parameters used to calculate  $V_{THP}$  at 300 K.**

<b>Parameter</b>	<b>Value</b>	<b>Unit</b>
$\Phi_m$	4.10	eV
$\chi_2$	4.025	eV
q	$1.6 \times 10^{-19}$	Coulomb
$E_{g2}$	0.7755	eV
$\Delta E_v$	0.2212	eV
$\Delta E_{f_0}$	0.00	eV
$Q_{ox}$	$1 \times 10^{11}$	Coulomb/cm <sup>2</sup>
$t_{ox}$	$50 \times 10^{-7}$	cm
a	$0.125 \times 10^{-12}$	V-cm <sup>-2</sup>
$d_d$	$30 \times 10^{-7}$	cm
$d_i$	$4 \times 10^{-7}$	cm
$\epsilon_2$	13.95	$\epsilon_0$
$\epsilon_0$	$8.854 \times 10^{-14}$	F/cm
$\epsilon_{oxide}$	3.90	$\epsilon_0$
$N_2$	$5 \times 10^{17}$	cm <sup>-3</sup>

$\Delta E_{f_0}$  is zero at 300 K. The value of  $\varepsilon_2$  is determined using the following relation,

$$\varepsilon_2 = 11.07 + 4.5x \dots\dots\dots 3.15$$

The calculation of the valence band discontinuity requires special attention. One might be tempted to use the Andersons model [21] to calculate  $\Delta E_v$  using following equations,

$$\Delta E_v = \Delta E_g - \Delta E_c \dots\dots\dots 3.16$$

$$\Delta E_c = \chi_1 - \chi_2 \dots\dots\dots 3.17$$

$$\Delta E_g = E_{g1} - E_{g2} \dots\dots\dots 3.18$$

But the Anderson model is oversimplified and it often fails to match the experimental data, mainly because it does not include the effect of the surface states, which is pretty dominant in most heterostructures. The device under investigation in this thesis consist of a strained SiGe/Ge interface pseudomorphically grown on a relaxed SiGe buffer, the use of the Anderson model would be inappropriate. Instead, the following relation derived by People and Bean [11] can be used,

$$\Delta E_v = x(0.84 - 0.53y) \dots\dots\dots 3.19$$

where,  $y$  is the mole fraction of the virtual substrate  $\text{Si}_{1-y}\text{Ge}_y$ .  $y$  is 0.75 for the p-channel MOS-gate HEMT structure used in the thesis.

Using the parameters specified, the threshold voltage value is found as,

<b><math>V_{\text{THp}} = 3.0573 \text{ V}</math></b>
---

It will be shown later that this threshold voltage value is an overestimation.

### 3.1.3 Calculation of $V_{Gmin}$

The minimum gate voltage  $V_{Gmin}$  is another important quantity of the HEMT. Unlike the MOSFET, the HEMT has two boundaries for its gate bias. For p-channel HEMT, the gate voltage must be less than the threshold voltage  $V_{THp}$  to keep it ‘ON’. For gate voltage equal to or greater than  $V_{THp}$ , the total channel is depleted and thus, there is no free carrier to conduct current flow from the source to the drain. Again, the gate voltage has to be greater than the minimum gate voltage  $V_{Gmin}$  for normal operation. At gate voltage equal to or lower than  $V_{Gmin}$ , the SiGe spacer layer is not fully depleted. Thus, there exists a conducting path in the SiGe supply layer parallel to the Ge channel. The device transconductance goes down due to this parallel conduction. Thus, this parallel conduction is not expected for the normal HEMT operation. As a result, HEMT operation is usually restricted within the gate voltage range:  $V_{Gmin} < V_G < V_{THp}$ .

The  $V_{Gmin}$  value can be calculated using the following relation,

$$V_{Gmin} = -\frac{q\rho_{so}}{C_{eq}} + V_{THp} \dots\dots\dots 3.20$$

where,  $\rho_{so}$  is the equilibrium channel charge

In the work of Jain et al [16], the value of  $\rho_{so}$  has been assumed to be  $10^{12} \text{ cm}^{-2}$ . Using this value the minimum gate voltage  $V_{Gmin}$  is calculated as,

<b><math>V_{Gmin} = 0.1738 \text{ V}</math></b>
---

In the later part of this chapter, a way to calculate more accurate value of  $\rho_{so}$  will be discussed. Accurate estimation of  $\rho_{so}$  helps to get a better estimate of the value of  $V_{Gmin}$ .

### 3.1.4 The current-voltage characteristics

The basic analytical model developed by Chang and Fetterman [22] has been used to calculate the current-voltage characteristics of the HEMT. There are several models available for calculating the current-voltage characteristics of the HEMT. The Chang-Fetterman model [22] has been used as it has been shown to be effective to match the experimental data.

The basic Chang-Fetterman model has been derived for the n-channel HEMT. Thus, a set of modified equations will be used here, which are valid for p-channel HEMT. The drain current  $I_D$  is given by,

$$I_D = -G_0[V_G - V_{THp} - V(x)][1 - \exp(-\frac{\mu\xi_x}{v_s})] \dots\dots\dots 3.21$$

where,  $G_0 = C_{eq}v_sZ$ ,

$\mu$  = The hole mobility in the strained Ge channel,

$v_s$  = the hole saturation velocity in the Ge channel,

$\xi_x$  = The electric field in the direction from source to drain,

$Z$  = the gate-width of the HEMT.

Now, considering the fact that  $\xi_x = \frac{dV(x)}{dx}$ , equation 3.21 can be written as,

$$I_D \int_{t_0}^{t_L} \frac{dt}{t^2 \ln(1+t)} = -\frac{v_s L G_0}{\mu} \dots\dots\dots 3.22$$

where,  $t(x) = \frac{I_D}{G_0(V_G - V_{THP} - V(x))}$ ,

$$t_0 = \frac{I_D}{G_0(V_G - V_{THP} - I_D R_s)}$$

$$t_L = \frac{I_D}{G_0(V_G - V_{THP} - V_D + I_D R_d)}$$

$R_s$  = Source Resistance,

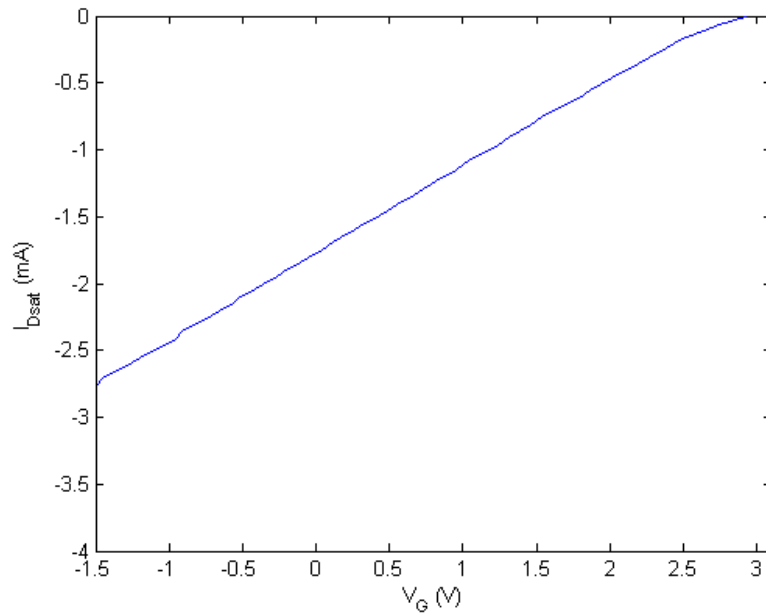
$R_d$  = Drain Resistance.

Again, Saturation current  $I_{Dsat}$  is given by,

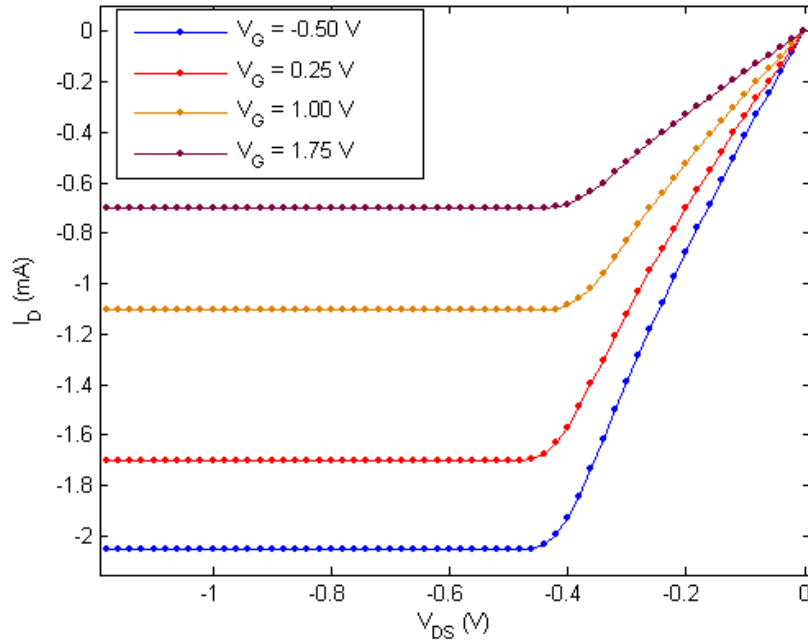
$$I_{Dsat} \int_{t_{os}}^1 \frac{dt}{t^2 \ln(1+t)} = -\frac{v_s L G_0}{\mu} \dots\dots\dots 3.23$$

where,  $t_{os} = \frac{I_{Dsat}}{G_0(V_G - V_{THP} - I_{Dsat} R_s)}$ .

Using Equation 3.23, the  $I_{Dsat}$  vs.  $V_G$  plot is obtained which is shown in Figure 3.3 (a). As expected, the saturation current varies almost linearly with the gate voltage. As the gate voltage approaches the threshold voltage (3.0573 volt in this case), the current goes to zero. Obviously, any parallel conduction or leakage current is neglected in this simple model. The entire current is assumed to be only due to the channel charge.



(a)



(b)

**Figure 3. 3: (a) The  $I_{Dsat}$ - $V_G$  and (b) the  $I_D$ - $V_D$  characteristics of the p-channel SiGe MOS-gate HEMT, using the analytical model of Jain et al [16].**

The  $I_D$ - $V_D$  plot is obtained using equation 3.22 and the  $I_{Dsat}$ - $V_G$  plot. This plot is shown in Figure 3.3(b). It should be noted that in this model, the variation of saturation current with drain to source voltage ( $V_{DS}$ ) is ignored. Thus, the current in the saturation region is constant for a fixed gate voltage. A hole mobility value of  $500 \text{ cm}^2/\text{V}\cdot\text{s}$  is used in the calculation of current voltage characteristics. This value is estimated using [8]. In [8], the hole mobility value is almost  $1000 \text{ cm}^2/\text{V}$ , which is obtained experimentally for a delta-doped HEMT device that consists of a strained Ge channel grown on a cubic  $\text{Si}_{0.3}\text{Ge}_{0.7}$  buffer. A delta-doped HEMT has higher mobility than a regular HEMT. Thus, it has been assumed that for the regular-doped HEMT an approximate mobility value of  $500 \text{ cm}^2/\text{V}\cdot\text{s}$  can be used.

The hole saturation velocity of  $3 \times 10^7 \text{ cm/s}$  is used in the calculation of Jain et al [16]. This value is definitely an overestimation. A hole saturation velocity of  $4 \times 10^6 \text{ cm/s}$  has been used in this thesis. Use of this value provides a closer agreement between the current-voltage characteristics calculated from the analytical model and that obtained by the *Medici*<sup>TM</sup> simulations.

### ***3.1.5 The transconductance ( $g_{ms}$ ) and cutoff frequency ( $f_T$ )***

The transconductance  $g_{ms}$  is an important parameter of any transistor, which determines its small signal (ac) performance. The expression that has been used to calculate  $g_{ms}$  is

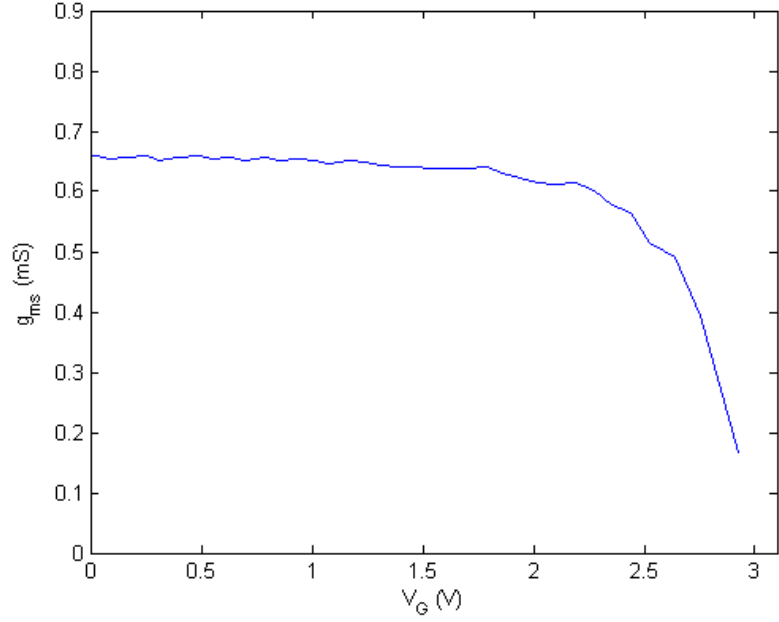


given below:

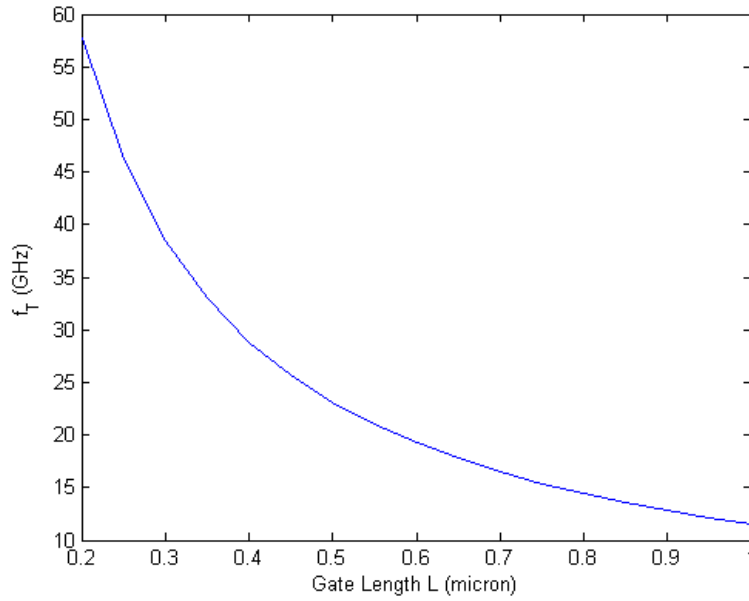
$$g_{ms} = \frac{I_{Dsat}}{V_G - V_{THp} + \left(\frac{v_s L}{\mu}\right) \ln(1 - t_{os})} \dots\dots\dots 3.24$$

Using this relation,  $g_{ms}$  has been calculated for different gate voltages. The  $g_{ms}$  vs.  $V_G$  plot is shown in Figure 3.4(a). It is clear that as the gate voltage goes down from the threshold voltage, the saturation transconductance goes up abruptly. At around a gate voltage value of 2 volts, the value of  $g_{ms}$  starts to saturate and it remains basically constant over the rest of the gate voltage range. It should be noted that in practical cases,  $g_{ms}$  value saturates and then starts going down for gate voltage less than  $V_{Gmin}$ . The current-voltage model used in this thesis considers current due to channel conductance only and thereby ignores any parallel conduction path such as the spacer layer. As mentioned before, for a gate voltage value less than  $V_{Gmin}$ , parallel conduction takes place in the spacer layer. Thus, the  $g_{ms}$  calculated here is basically the saturation transconductance due to the channel current only. But, for normal operation, gate bias is usually limited within the range:  $V_{Gmin} < V_G < V_{THp}$ . Thus, although,  $g_{ms}$  value calculated here is not very accurate for  $V_G < V_{Gmin}$ , it is not a big concern.

The cutoff frequency is another important figure of merit. Due to its high mobility, the HEMT has quite high cutoff frequency. The use of MOS gate in HEMT, further enhances



(a)



(b)

**Figure 3. 4: (a) The  $g_{ms}$  vs.  $V_G$  and (b) the  $f_T$  vs.  $L$  plot of the p-channel SiGe MOS-gate HEMT, using the analytical model of Jain et al [16].**

gate length, thus higher  $f_T$  value can be obtained.

## 3.2 The Modified Model

### 3.2.1 The threshold voltage expression

In the existing model, the threshold voltage expression has been derived completely ignoring the effect of silicon cap layer. A modified model for threshold voltage will be proposed, which will include the effect of the silicon cap layer and thus provides a more accurate estimation of the threshold voltage.

Figure 3.5 shows the device schematic, charge distribution and band diagram for the modified model. The derivation starts by considering the charge neutrality condition,

$$q(x_m - d_i) = q\rho_s + qN_{Ge}W_{Ge} \dots\dots\dots 3.25$$

As the Ge layer is unintentionally doped,  $\rho_s \gg N_{Ge}W_{Ge}$ . Thus, equation 3.25 can be written as,

$$q(x_m - d_i) = q\rho_s$$

$$\Rightarrow x_m = \frac{\rho_s}{N_2} + d_i \dots\dots\dots 3.26$$

Again,

$$W_{dep} = d_d + d_s + d_i - x_m \dots\dots\dots 3.27$$

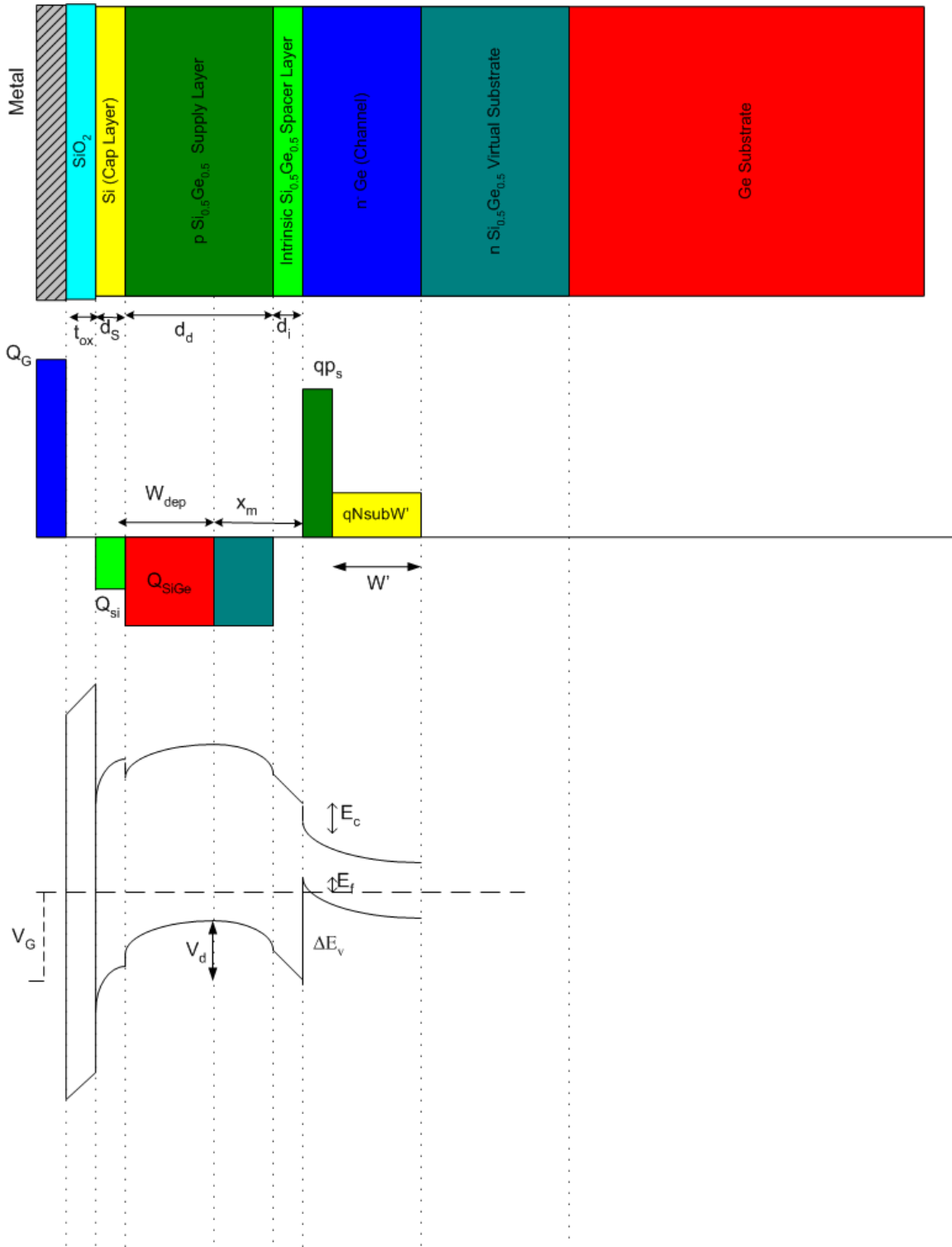


Figure 3. 5: Device schematic, charge distribution and energy band diagram of the p-channel MOS-gate HEMT, used in the modified model.

Using equation 3.24,

$$W_{dep} = d_d + d_s - \frac{\rho_s}{N_2} \dots\dots\dots 3.28$$

Again, the gate voltage is given by equation 3.1 as,

$$V_G = V_{FB} + \frac{Q_D}{C_{ox}} + \psi_s \dots\dots\dots 3.29$$

**Finding  $\psi_s$ :**

Considering the electric field and potential in the direction normal to the gate oxide/Si interface and using Gauss's law,

$$\frac{d\xi}{dx} = -\frac{qN_{si}}{\epsilon_{si}}, 0 < x < d_s$$

$$\frac{d\xi}{dx} = -\frac{qN_2}{\epsilon_2}, d_s < x < W_{dep} \dots\dots\dots 3.30$$

In the region,  $d_s < x < W_{dep}$ ,

$$\xi(x) = -\frac{qN_2}{\epsilon_2} x + A \dots\dots\dots 3.31$$

where, A is the constant of integration

At,  $x=W_{dep}$ ,  $\xi(x) = 0$ . Using this boundary condition in 3.27 yields,

$$A = \frac{qN_2}{\epsilon_2} W_{dep} \dots\dots\dots 3.32$$

Substituting the value of A in equation 3.27 ,

$$\xi(x) = \frac{qN_2}{\epsilon_2} (W_{dep} - x) \dots\dots\dots 3.33$$

At  $x = d_s^+$  ,

$$\xi(x = d_s^+) = \frac{qN_2}{\epsilon_2} (W_{dep} - d_s^+) \dots\dots\dots 3.34$$

Now, for  $0 < x < d_s$ ,

$$\xi(x) = -\frac{qN_2}{\epsilon_2} x + B \dots\dots\dots 3.35$$

where, B is the constant of integration.

At  $x = d_s$ , the electric flux D has to be continuous,

$$D(d_s^+) = D(d_s^-)$$

$$\Rightarrow \epsilon_{si} \xi(d_s^-) = \epsilon_2 \xi(d_s^+)$$

$$\Rightarrow \xi(d_s^-) = \frac{\epsilon_2}{\epsilon_{si}} \xi(d_s^+)$$

$$\Rightarrow \xi(d_s^-) = \frac{qN_2}{\epsilon_{si}} (W_{dep} - d_s^+) \dots\dots\dots 3.36$$

Substituting this value in equation 3.31 yields,

$$B = \frac{qN_2}{\epsilon_{si}}(W_{dep} - d_s) + \frac{qN_{si}}{\epsilon_{si}}d_s \dots\dots\dots 3.37$$

Thus, the electric field can be expressed as,

$$\xi(x) = \frac{qN_2}{\epsilon_{si}}(W_{dep} - d_s) + \frac{qN_{si}}{\epsilon_{si}}(d_s - x), 0 < x < d_s \dots\dots\dots 3.38$$

$$\text{and, } \xi(x) = \frac{qN_2}{\epsilon_2}(W_{dep} - x), d_s < x < W_{dep} \dots\dots\dots 3.39$$

The potential functions can be found by integration of equations 3.38 and 3.39,

$$\psi(x) = -\frac{qN_2}{\epsilon_{si}}(W_{dep} - d_s)x - \frac{qN_{si}}{\epsilon_{si}}(d_s x - x^2) + K_1, 0 < x < d_s \dots\dots\dots 3.40$$

$$\psi(x) = -\frac{qN_2}{\epsilon_2}(W_{dep}x - \frac{x^2}{2}) + K_2, d_s < x < W_{dep} \dots\dots\dots 3.41$$

where,  $K_1$  and  $K_2$  are the constants of integration.

At  $x=W_{dep}$ , the potential becomes zero,

$$\psi(W_{dep}) = 0 \dots\dots\dots 3.42$$

Using equation 3.42 with equation 3.41 yields,

$$K_2 = \frac{qN_2}{2\epsilon_2}W_{dep}^2 \dots\dots\dots 3.43$$

Thus, in the range,  $d_s < x < W_{dep}$ ,

$$\psi(x) = -\frac{qN_2}{\epsilon_2} \left( W_{dep}x - \frac{x^2}{2} \right) + \frac{qN_2}{2\epsilon_2} W_{dep}^2 \dots\dots\dots 3.44$$

At  $x=d_s$ ,

$$\psi(d_s) = -\frac{qN_2}{\epsilon_2} \left( W_{dep}d_s - \frac{d_s^2}{2} \right) + \frac{qN_2}{2\epsilon_2} W_{dep}^2 \dots\dots\dots 3.45$$

Now, potential has to be continuous across the Si/SiGe interface. Thus, substituting the value of  $\psi(d_s)$  in equation 3.36 and performing some algebraic manipulations, the following expression is obtained,

$$K_2 = \frac{qN_2}{2\epsilon_2} (W_{dep} - d_s)^2 + \frac{qN_{si}}{2\epsilon_{si}} d_s^2 + \frac{qN_2}{2\epsilon_{si}} (W_{dep} - d_s)d_s \dots\dots\dots 3.46$$

It is clear from Figure 3.5 that,

$$K_2 = \psi(0) = \psi_s \dots\dots\dots 3.47$$

Combining equation 3.46 and equation 3.47, the expression for  $\psi_s$  is found as,

$$\psi_s = \frac{qN_2}{2\epsilon_2} (W_{dep} - d_s)^2 + \frac{qN_{si}}{2\epsilon_{si}} d_s^2 + \frac{qN_2}{2\epsilon_{si}} (W_{dep} - d_s)d_s \dots\dots\dots 3.48$$

**Finding  $V_{FB}$ :**

The expression for the flat band voltage  $V_{FB}$  is given by equation 3.4 as,



$$V_{FB} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}}.$$

Again, the difference between the metal and the semiconductor work function is given by,

$$\phi_{ms} = \phi_m - \phi_{si} \dots\dots\dots 3.49$$

where,  $\phi_{si}$  is the work function of silicon.

The silicon used in the silicon cap layer is normally lightly doped p-type material. It can be shown with the help of the band diagram that the work function of the p-type  $\text{Si}_{0.5}\text{Ge}_{0.5}$  is almost equal to the work function of the lightly doped silicon layer. Thus  $\phi_{ms}$  can be expressed as,

$$\phi_{ms} \approx \phi_m - \phi_2 \dots\dots\dots 3.50$$

where,  $\phi_2$  is the work function of  $\text{Si}_{0.5}\text{Ge}_{0.5}$ .

Thus, using equation 3.5,

$$\phi_{ms} \approx \phi_m - \left[ \chi_2 + \frac{E_{g2}}{q} - \left( \frac{\Delta E_v}{q} - V_d - \frac{E_f}{q} \right) \right] \dots\dots\dots 3.51$$

The flatband voltage can be written as,

$$V_{FB} = \phi_m - \left[ \chi_2 + \frac{E_{g2}}{q} - \left( \frac{\Delta E_v}{q} - V_d - \frac{E_f}{q} \right) \right] - \frac{Q_{ox}}{C_{ox}} \dots\dots\dots 3.52$$

**Finding Q<sub>d</sub>:**

From Figure 3.5, it is clear that the depletion charge due to the gate voltage, Q<sub>d</sub> is given by,

$$Q_d = qN_{si}d_s + qN_2(W_{dep} - d_s) \dots\dots\dots 3.53$$

**The Threshold Voltage:**

Substituting the values of Ψ<sub>s</sub>, V<sub>FB</sub> and Q<sub>d</sub> from equation 3.48,3.52,3.53 into equation 3.1 yields,

$$V_G = \frac{qN_2}{2\epsilon_2}(W_{dep} - d_s)^2 + \frac{qN_{si}}{2\epsilon_{si}}d_s^2 + \frac{qN_2}{2\epsilon_{si}}(W_{dep} - d_s)d_s + \phi_m - \chi_2 - \frac{E_{g2}}{q} + \left(\frac{\Delta E_v}{q} - V_d - \frac{E_f}{q}\right) - \frac{Q_{ox}}{C_{ox}} + \frac{qN_{si}d_s + qN_2(W_{dep} - d_s)}{C_{ox}} \dots\dots\dots 3.54$$

Now, using depletion approximation, it can be shown that,

$$V_d = \frac{q\rho_s^2}{2\epsilon_2N_2} + \frac{q\rho_s d_i}{\epsilon_2} \dots\dots\dots 3.55$$

Using the value of V<sub>d</sub> in equation 3.54 yields,

$$V_G = \frac{qN_2}{2\epsilon_2}(W_{dep} - d_s)^2 + \frac{qN_{si}}{2\epsilon_{si}}d_s^2 + \frac{qN_2}{2\epsilon_{si}}(W_{dep} - d_s)d_s + \phi_m - \chi_2 - \frac{E_{g2}}{q} + \frac{\Delta E_v}{q} - \left(\frac{q\rho_s^2}{2\epsilon_2N_2} + \frac{q\rho_s d_i}{\epsilon_2} - \frac{E_f}{q} - \frac{Q_{ox}}{C_{ox}}\right) + \frac{qN_{si}d_s + qN_2(W_{dep} - d_s)}{C_{ox}} \dots\dots\dots 3.56$$

Using the linear approximation, E<sub>f</sub> can be expressed as,

$$E_f = \Delta E_{fo} + aq\rho_s \dots\dots\dots 3.57$$

where,  $\Delta E_{fo}$  is the y-axis intercept of the  $E_f$  vs.  $\rho_s$  plot.

$a$  is the slope of the plot.

Substituting this value of  $E_f$  in equation 3.56 and performing some algebraic manipulations, the final charge control expression is obtained,

$$\rho_s = -\frac{C_{eq}}{q}[V_G - V_{THp}] \dots\dots\dots 3.58$$

The equivalent or total capacitance  $C_{eq}$  is given by,

$$\frac{1}{C_{eq}} = \frac{d_d + d_i + \Delta d}{\epsilon_2} + \frac{d_s}{\epsilon_{si}} + \frac{1}{C_{ox}} \dots\dots\dots 3.59$$

$$\text{where, } \Delta d = \frac{a\epsilon_2}{q}.$$

The modified expression for threshold voltage  $V_{THp}$  is given by,

$$\begin{aligned} V_{THp} = & \phi_m - \chi_2 - \frac{E_{g2}}{q} + \frac{\Delta E_v}{q} - \frac{\Delta E_{fo}}{q} - \frac{Q_{ox}}{C_{ox}} + \frac{qN_2}{2\epsilon_2}d_d^2 + \frac{qN_{si}}{2\epsilon_{si}}d_s^2 \\ & + \frac{qN_2d_d d_s}{\epsilon_{si}} + \frac{qN_{si}}{C_{ox}}d_s + \frac{qN_2}{C_{ox}}d_d \dots\dots\dots 3.60 \end{aligned}$$

### ***3.2.2 Calculation of threshold voltage using modified model***

Now, the threshold voltage for the p-channel HEMT shown in Figure 3.1 will be calculated, using the modified threshold voltage expression. The device and material parameters used to calculate  $V_{THp}$  is shown in Table 3.2. It should be noted that, in this case, a  $d_d$  value of 25 nm is used instead of 30 nm. Actual value of the width of the SiGe

**Table 3. 2: Device and material parameters for the calculation of  $V_{THP}$  using modified model.**

Parameter	Value	Unit
$\Phi_m$	4.1	eV
$\chi_2$	4.025	eV
q	$1.6 \times 10^{-17}$	Coulomb
$E_{g2}$	.7755	eV
$\Delta E_v$	.2212	eV
$\Delta E_{f_0}$	0	eV
$Q_{ox}$	$1 \times 10^{11}$	Coulomb/cm <sup>2</sup>
$t_{ox}$	$50 \times 10^{-7}$	cm
a	$0.125 \times 10^{-12}$	V-cm <sup>-2</sup>
$d_d$	$25 \times 10^{-7}$	cm
$d_s$	$5 \times 10^{-7}$	cm
$d_i$	$4 \times 10^{-7}$	cm
$\epsilon_2$	13.95	$\epsilon_0$
$\epsilon_0$	$8.854 \times 10^{-14}$	F/cm
$\epsilon_{oxide}$	3.90	$\epsilon_0$
$\epsilon_{si}$	11.7	$\epsilon_0$
$N_2$	$5 \times 10^{17}$	cm <sup>-3</sup>
$N_{si}$	$5 \times 10^8$	cm <sup>-3</sup>

layer is 25 nm in both cases. But, in the Jain model, as the effect of the silicon layer have been ignored, the width of the silicon layer (5 nm in this case) had to be included, in the  $d_d$  value. In the modified model, as the width of the SiGe spacer layer and the silicon layer have been defined by the terms  $d_d$  and  $d_s$  respectively, the  $d_d$  value of 25 nm can be used. The addition of  $d_d$  and  $d_s$  ( $d_d+d_s$ ), specifies the total distance from the gate oxide to the supply/spacer interface.

In section 3.1.2, the methods of calculating parameters like  $\chi_2$ ,  $\Delta E_v$ ,  $\Delta E_{f_0}$  etc have already been discussed. As mentioned before, the p-type silicon-cap layer is usually very lightly doped. Here, a doping concentration value of  $5 \times 10^8 \text{ cm}^{-3}$  has been selected for the silicon layer. The width of the silicon layer is 5 nm. The main reason of the use of the silicon layer is to grow the gate oxide ( $\text{SiO}_2$ ). Thus, it is expected that most of the silicon layer originally grown on the spacer layer is consumed in growing  $\text{SiO}_2$ . Still, there exists a definite layer of silicon (few nanometers) that have been taken into account and termed its width as  $d_s$ . Later, it will be shown that the threshold voltage changes with the variation in the value of  $d_s$ .

Using the parameters specified in Table 3.2, the threshold voltage has been calculated as,

$$\mathbf{V_{THp} = 2.4839 \text{ V}}$$

As it will be shown later, this value is very close to the threshold voltage value obtained from *Medici*<sup>TM</sup> simulation.

### 3.2.3 Calculation of $V_{Gmin}$

The value of  $V_{Gmin}$  can be calculated using equation 3.20,

$$V_{Gmin} = -\frac{q\rho_{so}}{C_{eq}} + V_{THP}$$

An expression will be derived that can help to predict  $\rho_{so}$  accurately. From equation 3.55

$V_d$  can be expressed as,

$$V_d = \frac{q\rho_s^2}{2\varepsilon_2 N_2} + \frac{q\rho_s d_i}{\varepsilon_2}$$

$$\Rightarrow A\rho_s^2 + B\rho_s - V_d = 0 \dots\dots\dots 3.61$$

where,  $A = \frac{q}{2\varepsilon_2 N_2}$ ,

$$B = \frac{qd_i}{\varepsilon_2} .$$

Now, from Figure 3.5, it is clear that,  $V_d$  can be expressed as,

$$V_d = \Delta E_v - E_f - (E_f - E_v) \dots\dots\dots 3.62$$

$E_f - E_v$  is the difference between the Fermi level and the maximum point of the valence band in SiGe. This difference is calculated using the following relation,

$$E_f - E_v = -kT \ln\left(\frac{N_2}{N_v}\right) \dots\dots\dots 3.63$$

From equation 3.57,  $E_f$  can be expressed as,

$$E_f = \Delta E_{f_0} + aq\rho_s .$$

Using equation 3.57, 3.62 and 3.63 in equation 3.61 and performing some algebraic manipulations, the expression for  $\rho_s$  is found as,

$$\rho_s = \sqrt{\frac{2\epsilon_2 N_2}{q} [\Delta E_v - \Delta E_{fo} + kT \ln(\frac{N_2}{N_v})] + N_2^2 (d_i + \Delta d)^2 - N_2 (d_i + \Delta d)} \dots\dots 3.64$$

Again, from equation 3.9 ,

$$\rho_s = -\frac{C_{eq}}{q} [V_G - V_{THp}].$$

$V_{Gmin}$  is the gate bias at which the gate depletion and the channel depletion of the SiGe spacer layer just touch each other, but they do not interpenetrate. For this condition, the equilibrium channel charge  $\rho_{so}$  can be found using the simultaneous solution of equation 3.9 and 3.64. Thus, the value of  $\rho_{so}$  can be found using equation 3.64 and the  $V_{Gmin}$  value can be found using equation 3.55,

$$V_{Gmin} = -\frac{q\rho_{so}}{C_{eq}} + V_{THp}$$

The  $\rho_{so}$  value has been calculated using equation 3.64. The calculated value is  $6.6067 \times 10^{11} \text{ cm}^{-2}$ . Using this value in equation 3.55 yields a  $V_{Gmin}$  value of,

<b><math>V_{Gmin} = 0.5715 \text{ V.}</math></b>
--

### ***3.2.4 Current-voltage characteristics***

The current-voltage characteristics for the modified model are calculated using [22] as before. The same equations and parameters are used; except the value of threshold voltage  $V_{THp}$  is different here.

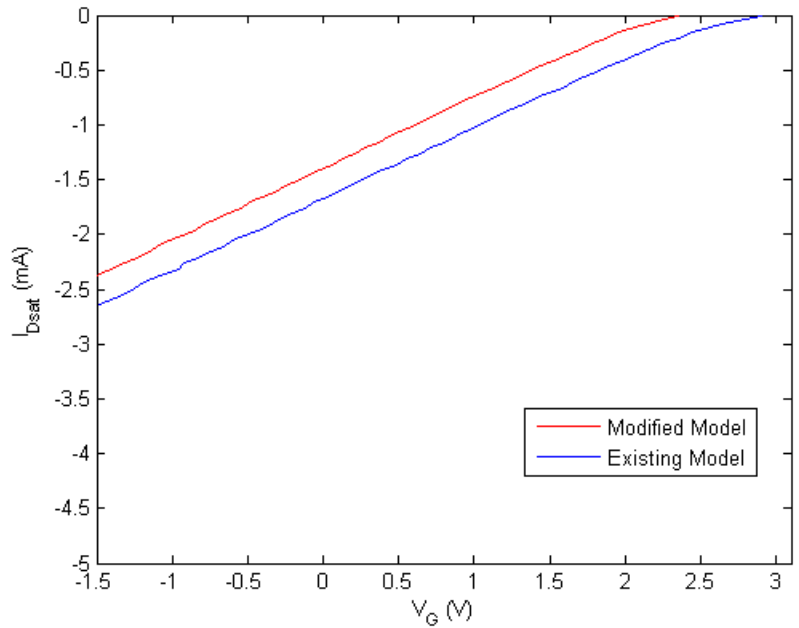
The  $I_{Dsat}$  vs.  $V_G$  plot is shown in Figure 3.6(a). The same plot for the previous model is also shown in the same figure. Comparison of these two plots shows that, the existing model overestimated the current values.

The  $I_D$ - $V_D$  plots for different  $V_G$  values, for both models are shown in Figure 3.6(b). Again, it is evident from the comparison that the existing model overestimated the current values.

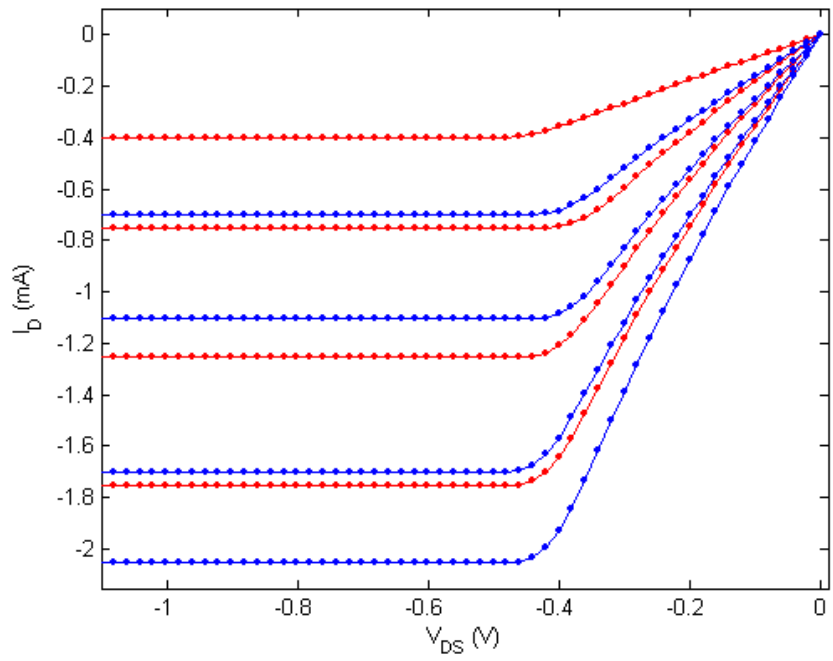
### ***3.2.5 Transconductance ( $g_{ms}$ ) and cutoff frequency ( $f_T$ )***

The  $g_{ms}$  vs.  $V_G$  plots using both models are shown in Figure 3.7(a). For gate voltage close to the threshold voltage, the value of  $g_{ms}$  using existing model is higher than the modified model. But for lower voltages, where  $g_{ms}$  value saturates, both model yields almost same



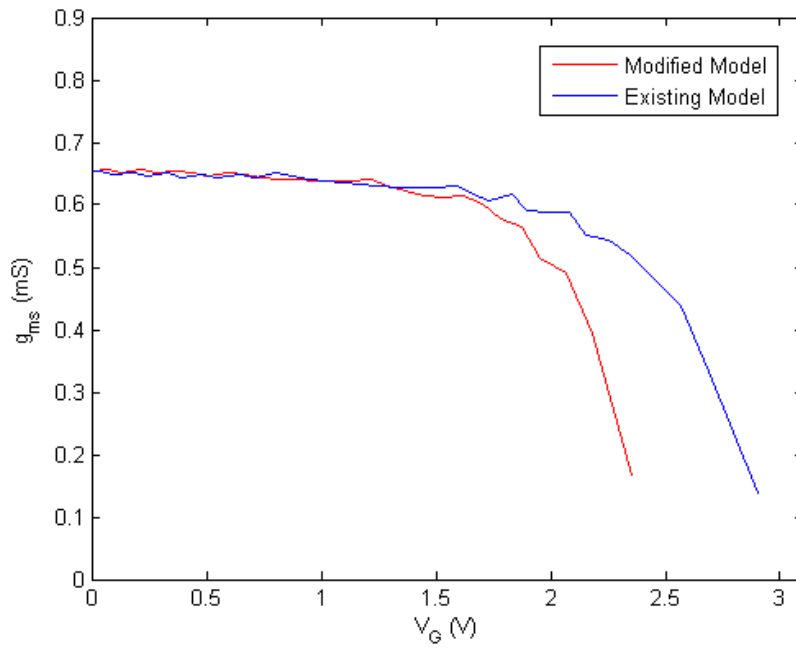


(a)

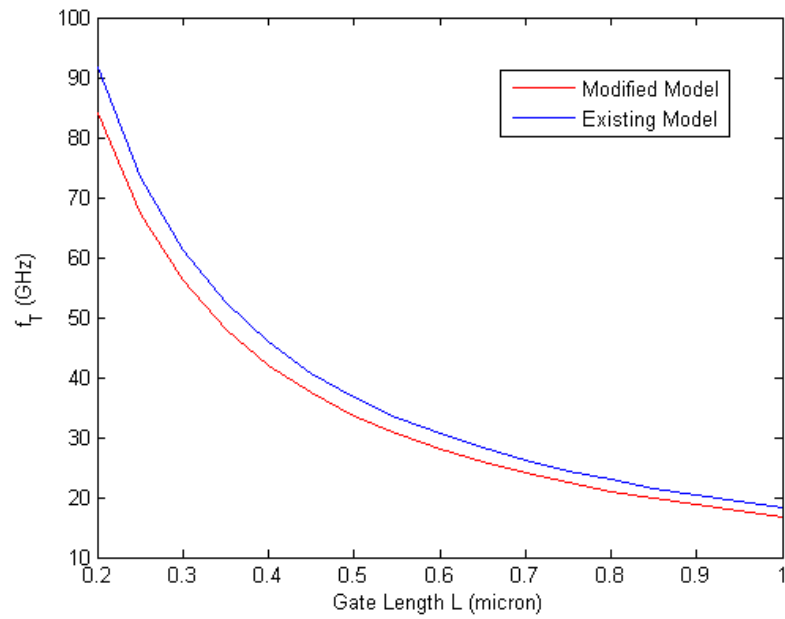


(b)

**Figure 3. 6: (a) The  $I_{Dsat}$ - $V_G$  and (b) the  $I_D$ - $V_D$  characteristics, using existing and modified model.**



(a)



(b)

**Figure 3. 7: (a) The  $g_{ms}$  vs.  $V_G$  and (b) The  $f_T$  vs.  $L$  plot, using existing and modified model.**

value. It is evident that in this region,  $g_m$  value is not very sensitive to the threshold voltage value.

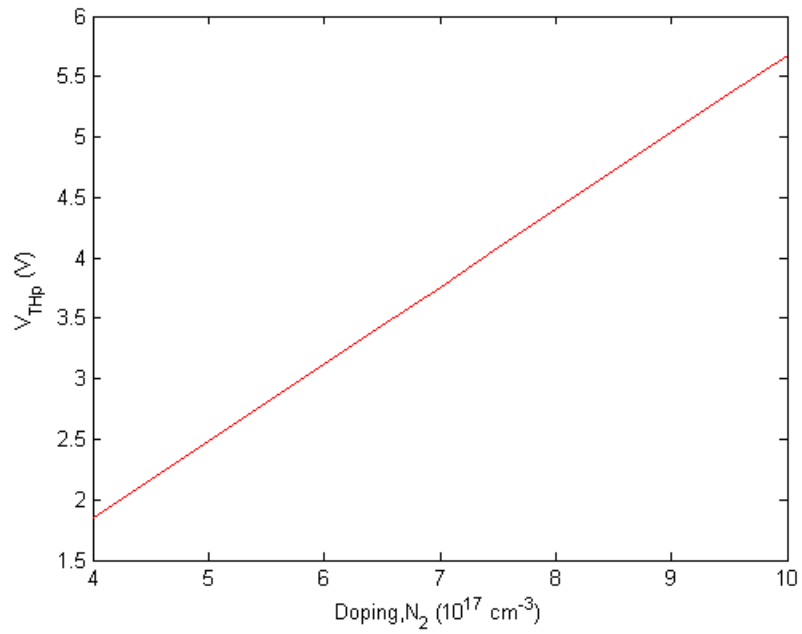
The plots of  $f_T$  vs.  $L$  for both models are shown in Figure 3.7 (b). It is clear from the plots that the existing model slightly overestimates the value of the cutoff frequency for all gate lengths.

### **3.3 Effect of Device and Material Parameters on $V_{THp}$ and $V_{Gmin}$**

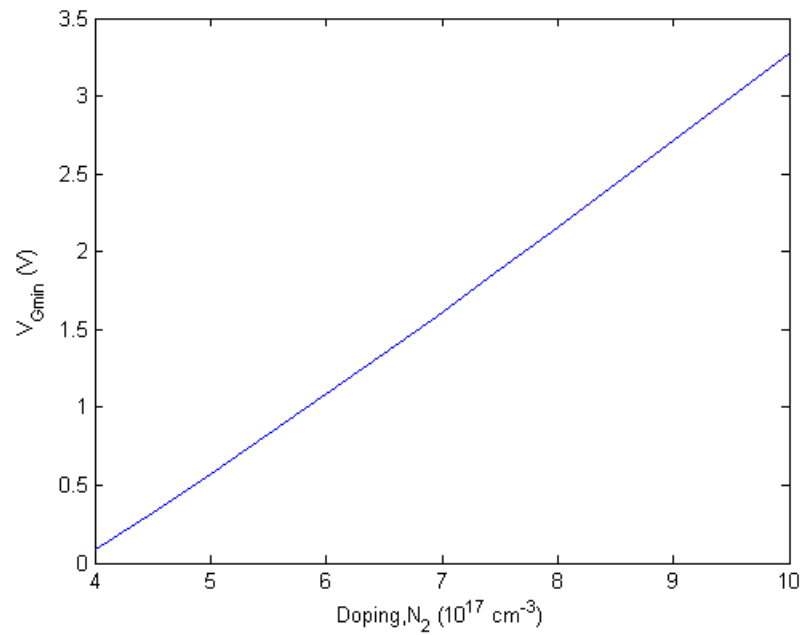
In this section, the effects of some device parameters such as doping concentration ( $N_2$ ), silicon cap layer width ( $d_s$ ), spacer layer width ( $d_i$ ) and oxide thickness on the value of threshold voltage  $V_{THp}$  and minimum gate voltage  $V_{Gmin}$  will be analyzed. Also, the effect of the mole fraction value  $x$  of  $Si_{1-x}Ge_x$  on  $V_{THp}$  and  $V_{Gmin}$  will be investigated. All analyses will be performed using the modified model.

#### ***3.3.1 Effect of doping concentration***

The threshold voltage and the minimum gate voltage can be changed by varying the doping of the SiGe spacer layer. Figure 3.8(a) shows the  $N_2$  vs.  $V_{THp}$  plot. The threshold voltage increases almost linearly with the increase in the doping concentration. The linear variation can be expected by looking at the expression of  $V_{THp}$ , which contains only first order terms of  $N_2$ . For a doping density variation from  $4 \times 10^{17} \text{ cm}^{-3}$  to  $1 \times 10^{18} \text{ cm}^{-3}$ , the



(a)



(b)

**Figure 3. 8: (a)  $N_2$  vs.  $V_{THp}$  plot and (b)  $N_2$  vs.  $V_{Gmin}$  plot of the p-channel SiGe MOS-gate HEMT.**

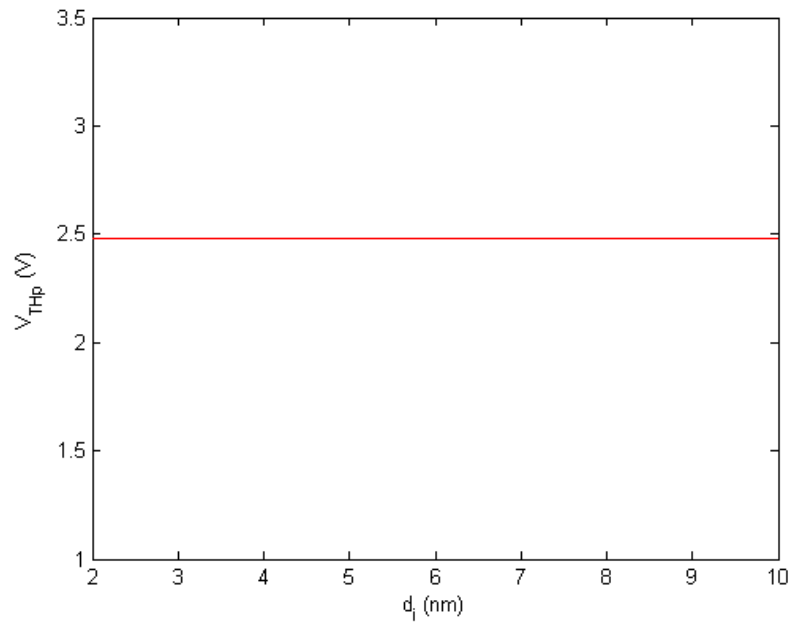
$V_{THp}$  value changes from 1.8 V to 5.6 V. Thus, it can be concluded that  $V_{THp}$  is strongly dependent on the doping density of the spacer layer.

The plot of  $N_2$  vs.  $V_{Gmin}$  is shown in figure 3.8(b). Similar to  $V_{THp}$ ,  $V_{Gmin}$  also varies linearly with doping density. The total change in  $V_{Gmin}$  is almost same as the total change in  $V_{THp}$ . Thus, the operating voltage range of the HEMT ( $V_{THp} \sim V_{Gmin}$ ) remains almost constant with the variation of the doping density.

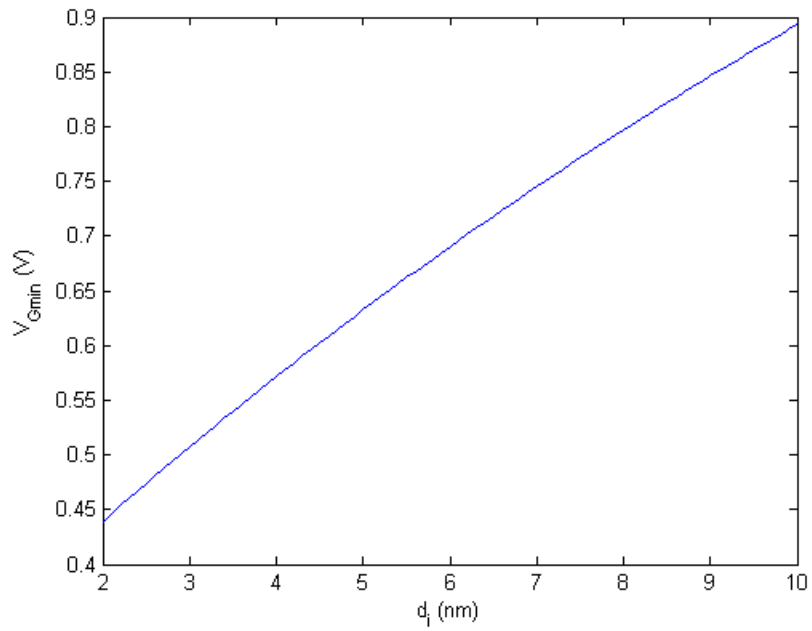
### ***3.3.2 Effect of spacer layer width***

The spacer layer width  $d_i$  vs.  $V_{THp}$  plot is shown in Figure 3.9(a). The expression of  $V_{THp}$  doesn't include any term consist of  $d_i$ . Thus, the threshold voltage remains practically indifferent to the change of the spacer layer width.

On the other hand, the plot of  $d_i$  vs.  $V_{Gmin}$  in Figure 3.9(b) shows that  $V_{Gmin}$  is weakly dependent on the value of  $d_i$ . The expression for  $V_{Gmin}$  contains the term  $C_{eq}$ .  $C_{eq}$  is dependent on  $d_i$ ; thus making the  $V_{Gmin}$  value dependent on  $d_i$ .



(a)



(b)

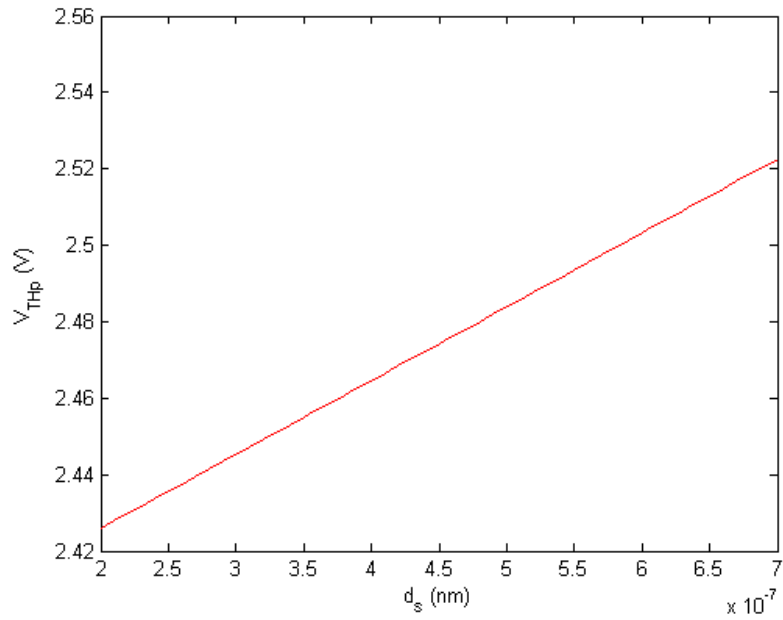
**Figure 3. 9: (a)  $d_i$  vs.  $V_{THp}$  plot and (b)  $d_i$  vs.  $V_{Gmin}$  plot of the p-channel SiGe MOS-gate HEMT.**

### ***3.3.3 Effect of silicon layer Width***

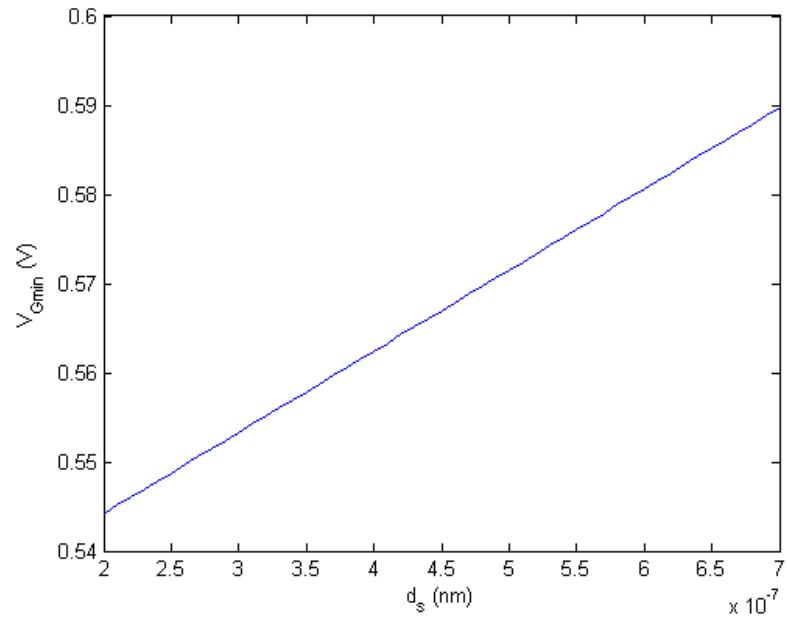
The inclusion of the effect of silicon cap layer in the expression of  $V_{THp}$  is the main goal of the modified model. As a result, using the modified model, the effect of the variation of the width of the silicon cap layer can be analyzed. As mentioned before, the main purpose of the silicon cap layer is to grow the  $SiO_2$  gate insulator, which is an inevitable part of the MOS structure. It is expected that, most of the silicon layer would be consumed in this oxidation process. In most cases, there remains a thin layer of silicon after the oxidation is done. Depending on the thickness of this layer it might have a significant or negligible effect on  $V_{THp}$  and  $V_{Gmin}$  value.

Figure 3.10 shows the  $d_s$  vs.  $V_{THp}$  plot. The variation is almost linear. The expression of  $V_{THp}$  includes second order term of  $d_s$ . But as the coefficient of the second order term is  $N_{si}$ , which is much smaller than  $N_2$ , the second order term has almost negligible effect in the variation of  $V_{THp}$ . It is evident from the plot that the variation of  $d_s$  moderately affects the value of  $V_{THp}$ . For a large doping density of the silicon layer, the variation would be larger.

The variation of  $V_{Gmin}$  shown in Figure 3.10(b) demonstrates a weak dependence of  $V_{Gmin}$  on the value of  $d_s$ . The operating voltage range is slightly varied with the variation of  $d_s$ .



(a)



(b)

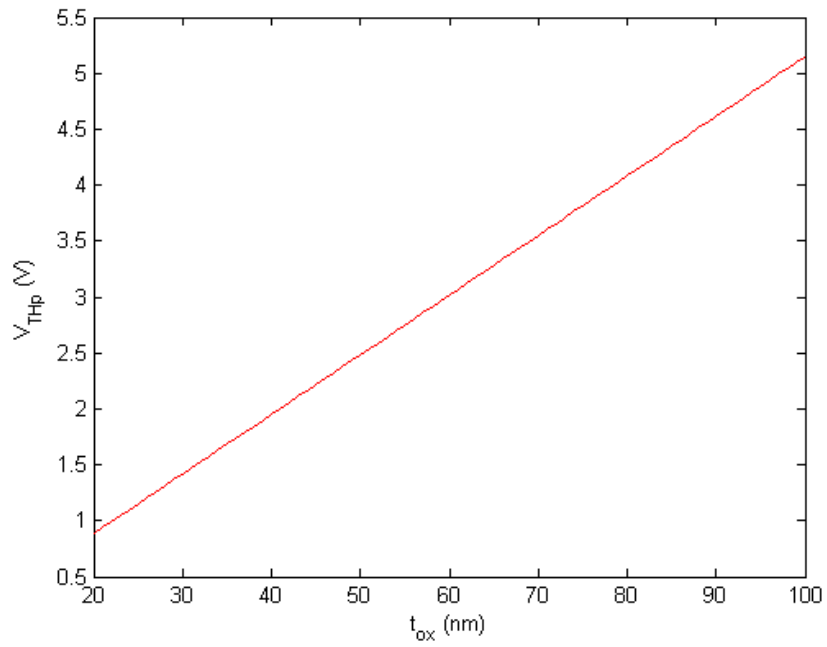
**Figure 3. 10: (a)  $d_s$  vs.  $V_{THp}$  plot and (b)  $d_s$  vs.  $V_{Gmin}$  plot of the p-channel SiGe MOS-gate HEMT.**



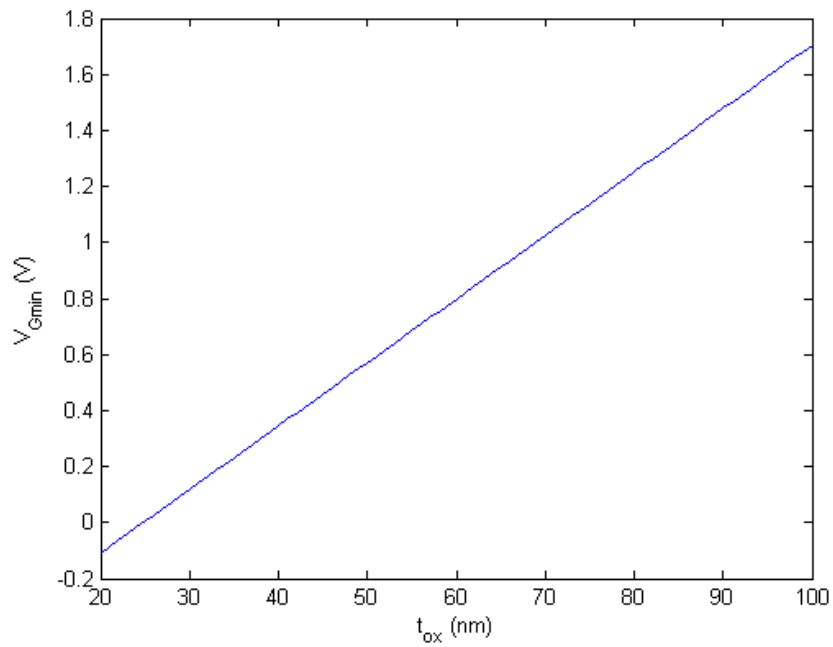
### ***3.3.4 Effect of oxide thickness***

The inclusion of the gate oxide makes the MOS-gate HEMT different from the Schottky-gate HEMT. The  $t_{ox}$  vs.  $V_{THp}$  plot is shown in Figure 3.11(a). The threshold voltage shows a strong dependence on the selection of the oxide thickness. The dependence is almost linear. The expression of  $V_{THp}$  does not contain any term of  $t_{ox}$ . But it contains terms with  $1/C_{ox}$ .  $1/C_{ox}$  is directly proportional to  $t_{ox}$ . This explains the linear dependence.

Figure 3.11(b) shows the  $t_{ox}$  vs.  $V_{Gmin}$  plot. It is evident that,  $V_{Gmin}$  is not so strongly dependent on  $t_{ox}$  as the threshold voltage. The  $V_{Gmin}$  expression consists of a term  $-1/C_{ox}$ . This term compensates part of the change that occurs due the change in  $V_{THp}$ . It is clear from the comparison of Figure 3.11(a) and (b) that increasing the oxide thickness can result in effective increase in the operating gate voltage range. On the other hand, excessive increase in  $t_{ox}$  results in poor transconductance value. Thus, an optimum value of  $t_{ox}$  should be selected while designing a MOS-gate HEMT, so that an wide operating voltage range, high cutoff frequency as well as reasonable gate transconductance can be achieved. One should also keep in mind that the minimum value of  $t_{ox}$  is determined by the breakdown electric field.



(a)



(b)

**Figure 3. 11: (a)  $t_{ox}$  vs.  $V_{THp}$  plot and (b)  $t_{ox}$  vs.  $V_{Gmin}$  plot of the p-channel SiGe MOS-gate HEMT.**

### ***3.3.5 Effect of mole fraction in $\text{Si}_x\text{Ge}_{1-x}$***

The p-channel MOS-gate HEMT device used in the simulations consists of  $\text{Si}_{0.5}\text{Ge}_{0.5}$  spacer and supply layer. The variation of the mole fraction  $x$  in  $\text{Si}_{1-x}\text{Ge}_x$  results in the change of bandgap, valence band discontinuity ( $\Delta E_v$ ) and other parameters. The effect of the choice of the mole fraction  $x$  on  $V_{\text{THP}}$  and  $V_{\text{Gmin}}$  will be investigated in this section.

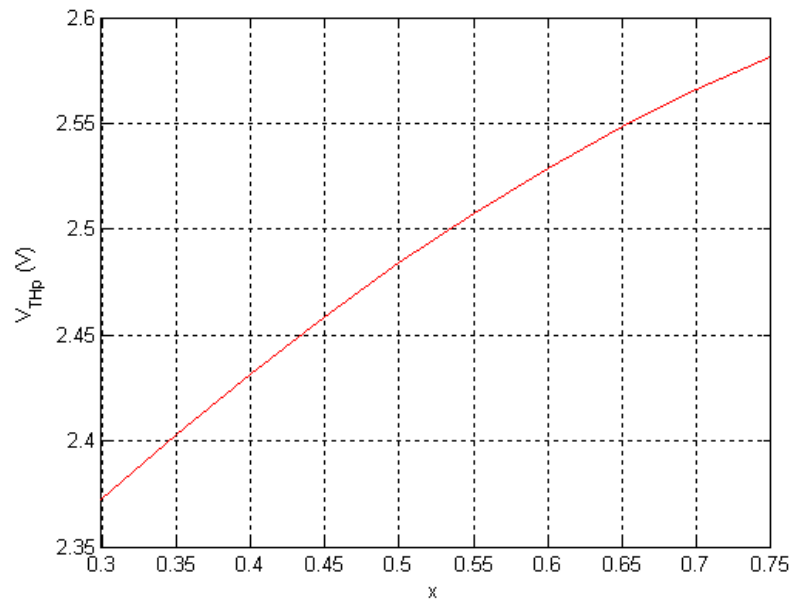
Figure 3.12(a) shows the dependence of the threshold voltage on the mole fraction.  $V_{\text{THP}}$  shows an almost linear and moderate dependence on  $x$ . As the spacer layer material approaches Ge (higher value of  $x$ ), the threshold voltage increases.

As it is evident from Figure 3.12(b),  $V_{\text{Gmin}}$  shows an opposite reaction to the increase in  $x$  value.  $V_{\text{Gmin}}$  value goes down as the  $x$  value is increased. Thus, for higher value of  $x$ , larger operating voltage range can be achieved.

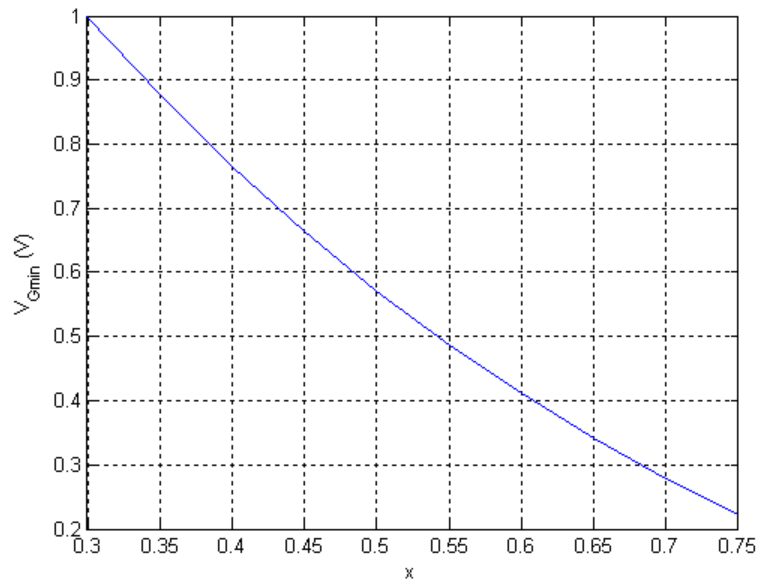
## **3.4 Conclusions**

In this chapter, the existing model, the modified model and the comparisons between them have been discussed. It is evident from the discussions that the modified model includes more device and material parameters and thus more accurately predicts device behavior. Using the modified model, the effect of some device and material parameters on the threshold voltage,  $V_{\text{Gmin}}$  and the operating voltage range have been shown.

These simulation results can be really handy to a device designer at the initial phase of



(a)



(b)

**Figure 3. 12: (a) Mole fraction  $x$  vs.  $V_{THp}$  plot and (b) mole fraction  $x$  vs.  $V_{Gmin}$  plot of the p-channel SiGe MOS-gate HEMT.**

the design. Certainly, to obtain a more accurate estimation of the threshold voltage and other parameters, some kind of numerical analysis software or device simulator (such as *Medici*<sup>TM</sup>, *Davinci*<sup>TM</sup>, *ATLAS*<sup>TM</sup>) has to be used.

# Chapter 4

## *The Temperature Model*

In the previous chapter, the p-channel MOS-gate HEMT behavior using the modified model has been discussed. All the analyses have been performed at room temperature (300 K). In this chapter, the effect of temperature variation on the behavior of the HEMT will be investigated. The HEMT has a wide range of applications that includes low temperature electronics as well as high temperature applications. Using the modified model, efforts will be made to theoretically predict the effects of temperature change on the threshold voltage, transconductance and current-voltage characteristics.

### 4.1 Effect of Temperature on Threshold Voltage

According to the modified model, the threshold voltage expression is given by,

$$V_{THp} = \phi_m - \chi_2 - \frac{E_{g2}}{q} + \frac{\Delta E_v}{q} - \frac{\Delta E_{fo}}{q} - \frac{Q_{ox}}{C_{ox}} + \frac{qN_2}{2\epsilon_2} d_d^2 + \frac{qN_{si}}{2\epsilon_{si}} d_s^2 + \frac{qN_2 d_d d_s}{\epsilon_{si}} + \frac{qN_{si}}{C_{ox}} d_s + \frac{qN_2}{C_{ox}} d_d \dots\dots\dots 4.1$$

The effect of the temperature variation on different terms in this expression will be investigated and combining the effects, the temperature dependence of the threshold voltage will be predicted.

### ***4.1.1 Temperature dependence of doping concentration***

The temperature range under consideration is from 100 K to 450 K. 100 K is much higher than the freeze out temperature of Si, Ge or SiGe. Thus, for the entire temperature range (100 K < T < 450 K), it can be assumed that the doping concentrations  $N_2$  and  $N_{Si}$  are almost constant.

### ***4.1.2 Temperature dependence of metal work function ( $\phi_m$ )***

Using the free electron model, it can be shown that the temperature dependence of the metal Fermi level can be expressed as [23],

$$E_{Fm}(T) = E_{Fmo} \left[ 1 - \frac{\pi^2}{12} \left( \frac{kT}{E_{Fmo}} \right)^2 \right] \dots\dots\dots 4.2$$

Here,  $E_{Fmo}$  is the metal Fermi level at 0 K, which can be evaluated using following relation,

$$E_{Fmo} = \left( \frac{h^2}{8m_e} \right) \left( \frac{3n}{\pi} \right)^{\frac{2}{3}} \dots\dots\dots 4.3$$

where,  $m_e$  is the mass of electron,

$h$  is Planck's constant,

$n$  is the total number of valence electrons in the metal/unit volume.

Normally, the value of  $E_{Fmo}$  is much larger than the value of  $kT$ . As a result, the metal Fermi level shows extremely weak temperature dependence.

Assuming the vacuum level being constant, it can be concluded that the change in the metal Fermi level is equal to the change in the metal work function. Obviously, the sign of the change is opposite. Thus, if the change in the metal Fermi level with temperature can be calculated, the change of the work function can be found.

Using the material parameters of Al, the change of the metal Fermi level has been calculated for a temperature change of 0 K to 300 K. The change is very small (few mV). Thus, in this present analysis, it can be easily assumed that the metal work function is essentially constant.

#### ***4.1.3 Temperature dependence of semiconductor electron affinity ( $\chi_2$ )***

The applied gate bias voltage  $V_G$  is independent of temperature. Two components of the gate voltage,  $\psi_s$  and  $Q_d$  are independent of temperature variation. As a result, the third component  $\phi_{ms}$  has to be constant also. It has been already proved that the metal work function is essentially constant. This makes  $\phi_s$  independent of temperature variation.

The temperature independence of  $\phi_s$  implies that the Fermi level of the semiconductors will be almost constant over the temperature range. Thus, it can be assumed that the change in the electron affinity of the SiGe supply layer is half of the change of its bandgap. Of course, the sign of the change is opposite. This relation can be expressed in an equation as,



$$\chi_2(300) - \chi_2(T) = \frac{1}{2}[E_{g2}(T) - E_{g2}(300)] \dots\dots\dots 4.4$$

The value of the electron affinity of the SiGe layer at 300 K is known. Thus, using equation 4.4, the temperature dependence of  $\chi_2$  can be calculated.

#### ***4.1.4 Temperature dependence of bandgap***

The temperature dependence of the bandgap of the strained  $\text{Si}_{1-x}\text{Ge}_x$  spacer layer is calculated using equations 3.13 and 3.14 [9] mentioned in the previous chapter,

$$E_{g2}(x, 4.2 \text{ K}) = 1.17 - 0.896x + 0.396x^2 \dots\dots\dots 4.5$$

$$E_{g2}(x, T) = E_{g2}(x, 0 \text{ K}) - \frac{4.73 \times 10^{-4} T^2}{T + 636} \dots\dots\dots 4.6$$

#### ***4.1.5 Temperature dependence of $\Delta E_v$***

As mentioned in the previous chapter, the valence band discontinuity  $\Delta E_v$  is calculated using the People and Bean's [11] equation. The model does not specify the temperature dependence of  $\Delta E_v$ . The other available models [10] to calculate  $\Delta E_v$  of a strained system also do not show any consideration of temperature variation. In the present analysis, it is assumed that  $\Delta E_v$  is temperature independent.

#### ***4.1.6 Temperature dependence of $\Delta E_{f_0}$***

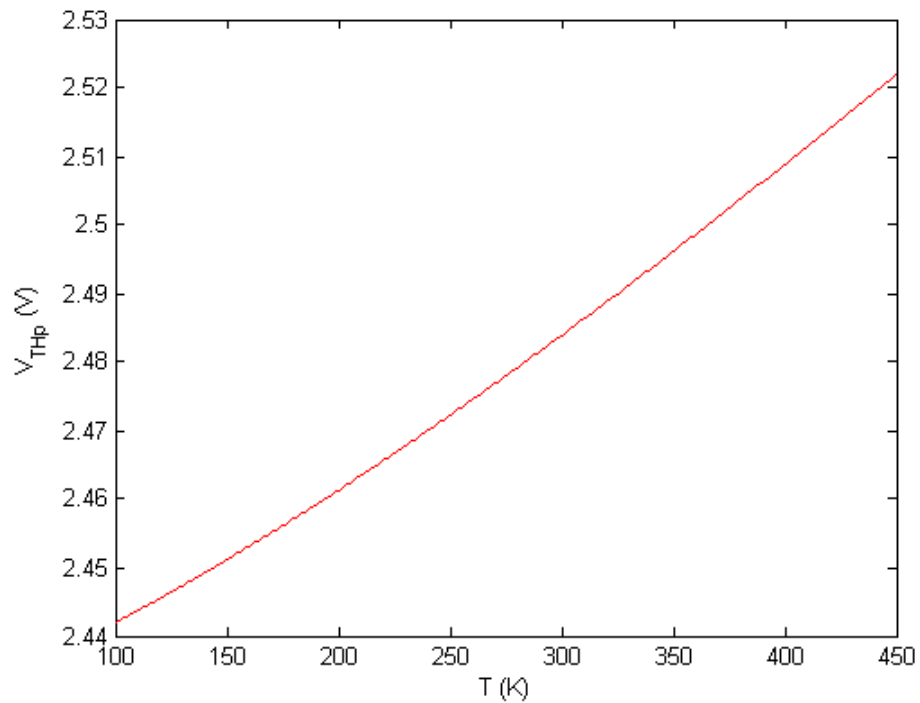
There is no accurate model available to predict the temperature variation of  $\Delta E_{f_0}$ . But it is known that at 300 K,  $\Delta E_{f_0}=0$  and at 77 k  $\Delta E_{f_0}=0.025$  eV. It have been assumed that a linear variation of  $\Delta E_{f_0}$  between these two temperatures. With this assumption,  $\Delta E_{f_0}(T)$  can be expressed as,

$$\Delta E_{f_0}(T) = -0.000112T + .0336 \dots\dots\dots 4.7$$

#### ***4.1.7 Calculation of temperature dependence of $V_{THP}$***

The other parameters in the threshold voltage equation can be assumed independent of the temperature variation. Thus, taking into consideration the temperature dependence of the parameters mentioned in the previous sections, the temperature dependence of the threshold voltage can be calculated. A MATLAB program has been used to calculate the temperature dependence of  $V_{THP}$ . Figure 4.1 shows the T vs.  $V_{THP}$  plot. A temperature range of 100 K to 450 K is considered which falls within the extrinsic temperature range of the semiconductors. As a result,  $n_0 \approx N_2$ .

It is evident from the plot that the threshold voltage shows weak dependence on temperature. The variation of  $V_{THP}$  is almost linear. Over a temperature change of 350 K



**Figure 4. 1: Temperature variation of the threshold voltage.**

(100K to 450 K), the threshold voltage changes only 8 mV. In practical cases, a little more variation might be observed, due to the variation of some other device and material parameters that have not been included in this analysis.

## 4.2 Effect of Temperature on Hole Mobility ( $\mu_h$ )

The hole mobility of the strained Ge channel varies with temperature. With increment in temperature, the mobility value goes down. At this point, no accurate analytical model is available to describe the temperature dependence of the hole mobility in the strained Ge

channel. The experimental data for temperature dependence of the hole hall mobility in the strained Ge channel reported in [8] will be used in this analysis. It should be noted that this data is obtained using strained Ge channel on cubic  $\text{Si}_{0.3}\text{Ge}_{0.7}$ . In the device under discussion, the virtual substrate is not  $\text{Si}_{0.3}\text{Ge}_{0.7}$ , but  $\text{Si}_{0.5}\text{Ge}_{0.5}$ . Still, it can be assumed that the temperature dependence of mobility can be approximated using the available data. Also, the data is for a delta-doped HEMT structure, which has higher mobility than the regular-doped HEMT. A mobility value of  $1000 \text{ cm}^2/\text{V-s}$  at 300 K is reported in [8]. In the present analysis, the mobility value at 300 K is  $500 \text{ cm}^2/\text{V-s}$ . Thus, the experimental mobility values at other temperatures can be scaled down by the factor of 2 to use in the present analysis.

The mobility values used in the calculation are shown in Table 4.1. It should be noted that the mobility value at 400 K was not available in the experimental data. It has been attempted to estimate the value using linear approximation.

**Table 4. 1: The hole hall mobility at different temperature as estimated from the experimental plot.**

Temperature (K)	Hole Hall Mobility ( $\text{cm}^2/\text{V-s}$ )
100	10000
200	1500
300	500
400	150

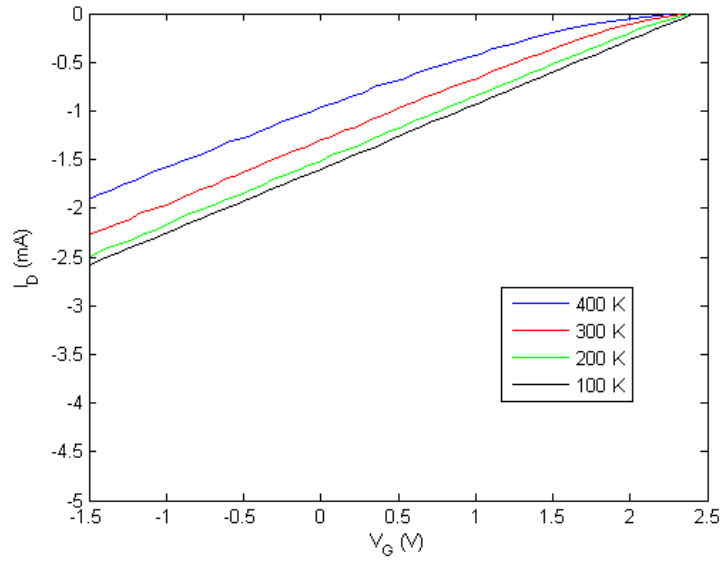
### 4.3 The Current-Voltage Characteristics

The current-voltage characteristics for different temperatures have been calculated using the Chang-Fetterman model [22]. It has been assumed that the only two temperature dependent parameters in the Chang-Fetterman current-voltage characteristics are the threshold voltage and hole mobility. Figure 4.2(a) shows the  $I_{Dsat}$  vs.  $V_G$  plot. It is evident that the saturation current decreases as the temperature goes up. The current values at 100 K and 200 K are very close. As the temperature goes up from 200 K to 300 K, bigger reductions in the current values are noticed. Again, in the temperature range of 300 K to 400 K, the changes in the current values are even larger.

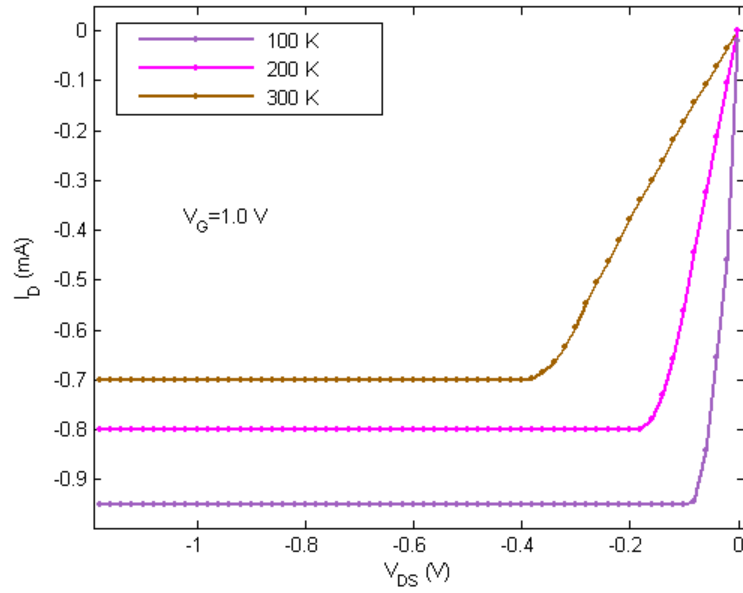
$I_D$ - $V_D$  characteristics for different temperatures at gate voltage 1 V are shown in Figure 4.2 (b). Due to the high mobility at low temperatures, the current increases very quickly with the increment of  $V_{DS}$  in the linear region. As the temperature goes up, the mobility decreases due to adverse effects such as optical phonon scattering. As a result, the current does not increase as fast as in the case of low temperatures. In the saturation region, the current value remains constant, as the channel length modulation effect has not been taken into consideration.

### 4.4 Transconductance

Figure 4.3 shows the  $g_{ms}$  vs.  $V_G$  plot for different temperatures. As the temperature goes up, transconductance goes down. For the gate bias values close to the threshold voltage,  $g_{ms}$  is sensitive to both temperature and threshold voltage. At lower gate voltages,  $g_{ms}$

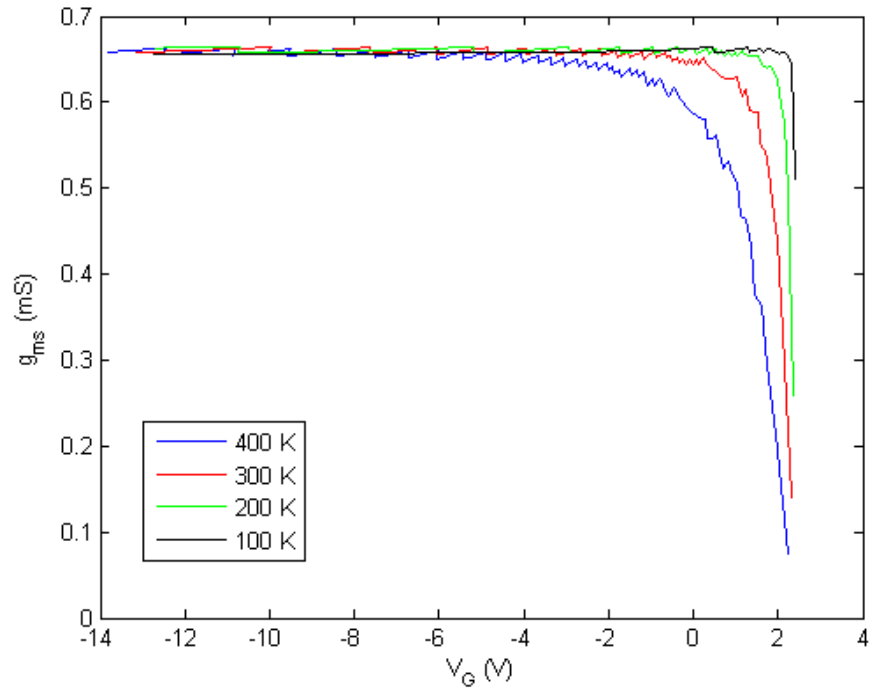


(a)



(b)

**Figure 4. 2: Temperature variation of (a) the  $I_{Dsat} - V_G$  and (b) the  $I_D - V_D$  characteristics.**



**Figure 4. 3:  $g_{ms}$  vs.  $V_G$  plot of different temperatures.**

becomes almost constant. For lower temperatures, this saturation occurs early. At high temperatures, saturation takes place slowly. As  $g_{ms}$  saturates, it becomes less sensitive to temperature.

## 4.5 Conclusions

In this chapter, a simple temperature model has been presented. Using this model, the temperature dependence of the threshold voltage, current voltage characteristics and transconductance have been predicted. It should be noted that the saturation velocity ( $v_s$ )

has been assumed to be independent of the temperature variation. This is definitely not true in practical cases. No accurate analytical model or experimental data is available that could help predicting the temperature variation of  $v_s$  in the strained Ge channel. If it is assumed that  $v_s$  is weakly temperature dependent, this temperature model should be able to give us a rough idea of the temperature dependency.



# Chapter 5

## *Analytical Modeling of Delta-Doped HEMT*

In a delta-doped HEMT, the whole supply layer is not doped. Instead, a very thin layer in the supply layer is doped. There are quite a few advantages of the delta-doped HEMT over the regular-doped HEMT that include increase in mobility and cutoff frequency. By varying the position and width of the doped layer, one can control the cutoff frequency, the threshold voltage, the minimum gate voltage and the transconductance. In the beginning of this chapter, the existing threshold voltage model for the delta-doped MOS-gate HEMT will be presented and its limitations will be discussed. Then, a modified model will be proposed that is valid for any width of the doped layer. Also, an expression for the minimum gate voltage  $V_{tl}$  will be derived. In the last part of this chapter, the effects of different material and device parameters on  $V_{THp}$  and  $V_{tl}$  are investigated.

### **5.1 The Existing Threshold Voltage Model**

#### *5.1.1 The threshold voltage expression*

An expression of the threshold voltage for the p-channel delta-doped SiGe MOS-gate HEMT has been proposed by Gokhale et al. [24]. The expression of  $V_{THp}$  is given by,

$$V_{THp} = \phi_m - \chi_2 - \frac{E_{g2}}{q} + \frac{\Delta E_v}{q} - \frac{E_{fo}}{q} - \frac{Q_{ox}}{C_{ox}} + \frac{qn_d}{C_{ox}} + \frac{qn_d d_1}{2\epsilon_2} \dots\dots\dots 5.1$$

where,  $\chi_2$  is the electron affinity of the semiconductor,

$\Phi_m$  is the metal work function,

$\Delta E_v$  is the valence band discontinuity at the  $\text{Si}_{0.5}\text{Ge}_{0.5}/\text{Ge}$  Interface,

$E_{g2}$  is the band gap of  $\text{Si}_{0.5}\text{Ge}_{0.5}$ ,

$n_d$  is the charge sheet density in the delta doping of the supply layer,

$d_1$  is the distance of the doped plane from the oxide/Si interface.

### ***5.1.2 Limitations of the existing model***

The existing model for the threshold voltage is applicable only when the width of the doped layer is extremely thin. In other words, the expression of the threshold voltage is derived with the assumption that the width of the doped layer (the width can be called  $\delta$ ) is negligible compared to the distance of the doped layer from the oxide/Si interface ( $d_1$ ). This assumption is definitely not valid when the delta-doped layer is placed very close to the oxide layer. Also, it is possible to tune the threshold voltage and the minimum gate bias by varying  $\delta$ . The existing model requires that the  $\delta$  value be quite thin and negligible compared to  $d_1$ . Thus, the existing model is fallible when the  $\delta$  value is varied freely and it becomes comparable to  $d_1$ .

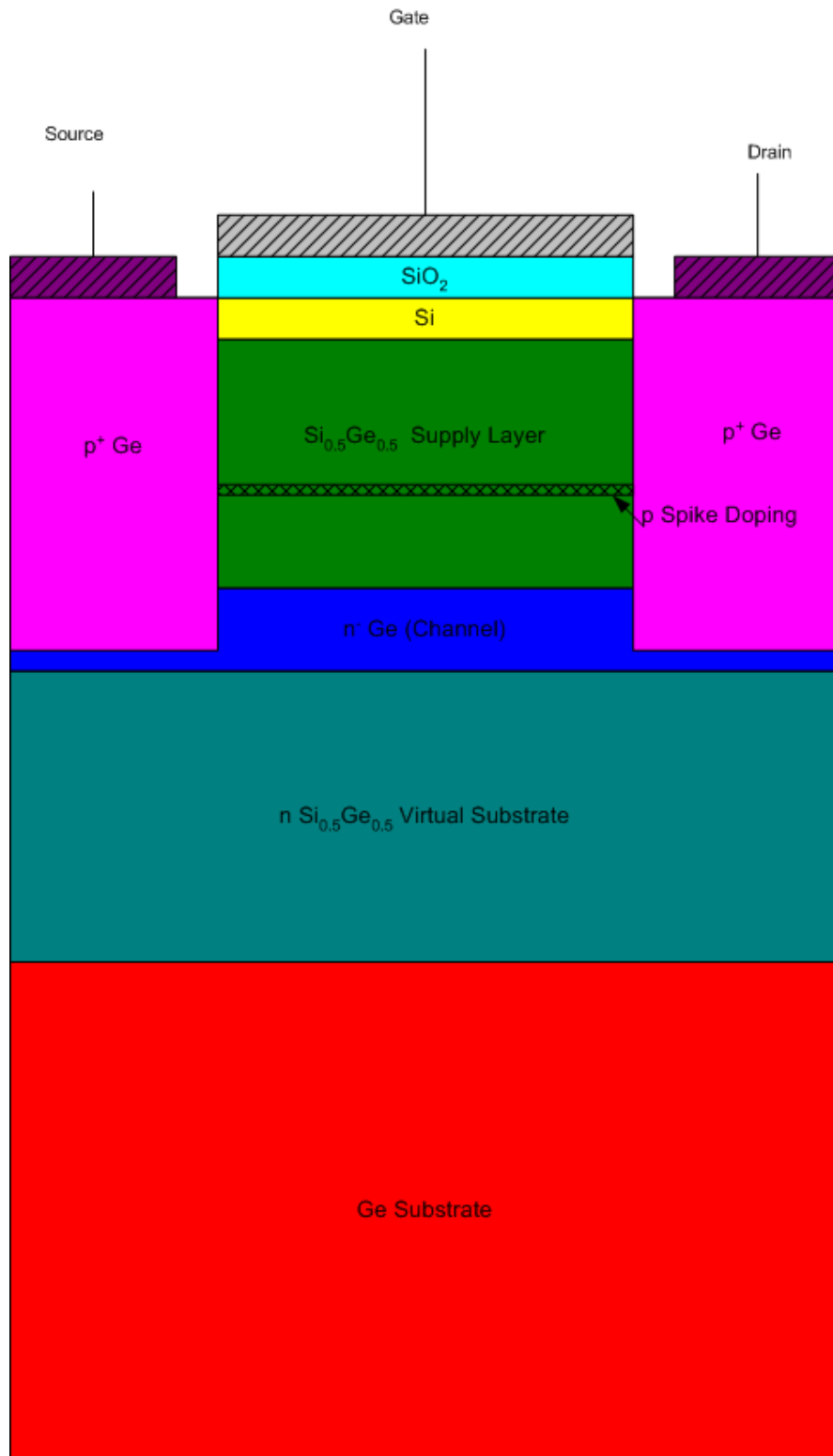
## **5.2 The Modified Threshold Voltage Model**

### ***5.2.1 Need for the modified model***

A threshold voltage model is required that can overcome the limitations of the existing model. This modified model should be valid for any value of  $\delta$ ; starting from almost negligible widths to the whole supply layer width (when  $\delta = d_d =$  width of the supply layer). As a result, the new model would enable us to include the effect of change in  $\delta$  on the threshold voltage and the minimum gate voltage. Thus, this model includes one more dimension to the existing model. A new model for the threshold voltage will be proposed, which is a modified version of the existing model.

### ***5.2.2 The threshold voltage expression***

Figure 5.1 shows the device structure used to derive the expression of the threshold voltage. This device is very similar to the one that has been used in chapter 3. In this case, the supply layer is delta doped and there is no spacer layer in this structure. Figure 5.2 shows the device schematic, band diagram and charge distribution diagram used in the derivation. The depletion charge in the supply layer is confined in a very narrow width. The part of the depletion charge is due to the gate voltage. The width of this charge layer is  $\delta_1$ . The width of the charge layer due to the channel charge is  $\delta_2$ . As there is no spacer layer present in this structure, the distance  $d_2$  should be equal or greater than the typical spacer layer width.



**Figure 5. 1: The device structure of the delta-doped MOS-gate SiGe HEMT.**

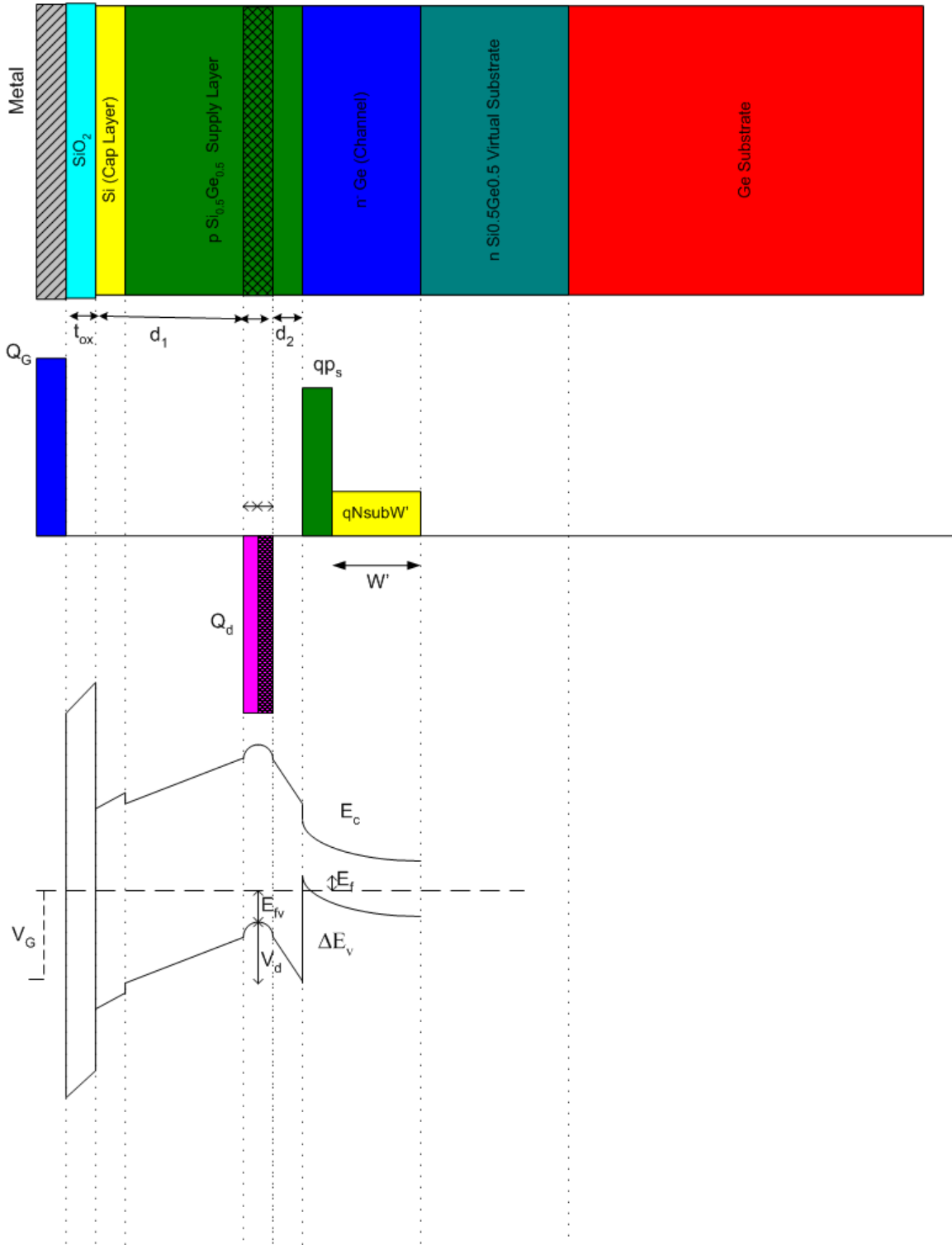


Figure 5. 2: The device schematic, charge distribution and band diagram used to derive  $V_{THP}$  expression.

The silicon cap layer used here is undoped. The expression of  $V_{THp}$  has been derived neglecting the effect of the silicon layer. It can be assumed that for the delta-doped structure and undoped silicon layer, the effect of silicon layer width is negligible. The derivation of the threshold voltage expression is similar to the derivation of the threshold voltage expression of the regular-doped MOS-gate HEMT. The threshold voltage expression is given by,

$$V_{THp} = \phi_m - \chi_2 - \frac{E_{g2}}{q} + \frac{\Delta E_v}{q} - \frac{E_{fo}}{q} - \frac{Q_{ox}}{C_{ox}} + \frac{qN_2\delta}{C_{ox}} + \frac{qN_2\delta^2}{2\epsilon_2} + \frac{qN_2d_1\delta}{\epsilon_2} \dots\dots\dots 5.2$$

Now, it can be shown that this equation converges to the existing expression for  $V_{THp}$  as  $\delta$  becomes very thin. For a thin doped layer,  $\frac{\delta}{2} \ll d_1$ . If it is defined that  $n_d =$  the charge sheet density in the delta doping of the supply layer  $= N_2\delta$ , equation 5.2 becomes,

$$V_{THp} = \phi_m - \chi_2 - \frac{E_{g2}}{q} + \frac{\Delta E_v}{q} - \frac{E_{fo}}{q} - \frac{Q_{ox}}{C_{ox}} + \frac{qn_d}{C_{ox}} + \frac{qn_d d_1}{2\epsilon_2},$$

which is basically equation 5.1.

### 5.2.3 Calculation of threshold voltage

The threshold voltage for the delta-doped MOS-gate HEMT shown in Figure 5.1 is calculated using the device and material parameters specified in Table 5.1. The calculated threshold voltage value is,

$V_{THp} = -0.4592 \text{ V.}$
--------------------------------

**Table 5. 1: Device and material parameters used to calculate  $V_{THP}$  of the delta-doped MOS-gate HEMT.**

Parameter	Value	Unit
$\Phi_m$	4.1	eV
$\chi_2$	4.025	eV
q	$1.6 \times 10^{-19}$	C
$E_{g2}$	0.7755	eV
$\Delta E_v$	0.2212	eV
$\Delta E_{f_0}$	0	eV
$Q_{ox}$	$1 \times 10^{11}$	C/cm <sup>2</sup>
$t_{ox}$	$50 \times 10^{-7}$	cm
a	$0.125 \times 10^{-12}$	V-cm <sup>-2</sup>
$d_1$	$15 \times 10^{-7}$	cm
$d_2$	$14 \times 10^{-7}$	cm
$\delta$	$1 \times 10^{-7}$	cm
$\epsilon_2$	13.95	$\epsilon_0$
$\epsilon_0$	$8.854 \times 10^{-14}$	F/cm
$\epsilon_{oxide}$	3.9	$\epsilon_0$
$N_2$	$1 \times 10^{18}$	cm <sup>-3</sup>

This result is very close to the experimental measurement of the threshold voltage of the delta-doped MOS-gate HEMT with similar structure, found in the work of Murakami et al. [4].

### 5.3 The Expression for $V_{tl}$

The term  $V_{tl}$  for a delta-doped HEMT is similar to the term  $V_{Gmin}$  for a regular-doped HEMT. The minimum gate bias  $V_{tl}$  of a p-channel delta-doped MOS-gate HEMT is the gate voltage at which the top of the valence band of the supply layer almost touches the Fermi level. As a result, real space hole transfer occurs in the supply layer. Thus, a channel parallel to the Ge channel is formed. The conduction due to this parallel channel sharply reduces the device transconductance. Thus, for normal operation of the delta-doped HEMT, the minimum gate voltage is restricted to equal or greater than  $V_{tl}$ . Thus, the normal operating gate-voltage range of a delta-doped HEMT is:  $V_{tl} < V_G < V_{THp}$ .

An expression for  $V_{tl}$  has been derived using its definition. At  $V_G = V_{tl}$ , the distance between the valence band maximum and the Fermi level,  $E_{FV}$  becomes almost zero. The expression for  $V_{tl}$  is given by,

$$V_{tl} = - \frac{q \left[ \sqrt{\frac{2 \epsilon_2 N_2}{q} [\Delta E_v - \Delta E_{fo} + kT \ln(\frac{N_2}{N_v})] + N_2^2 (d_i + \Delta d)^2 - N_2 (d_i + \Delta d)} \right]}{C_{eq}} + V_{THp} \dots \dots \dots 5.3$$



The expression for the total equivalent capacitance  $C_{eq}$  is given by,

$$C_{eq} = \frac{1}{\frac{d + \Delta d}{\epsilon_2} + \frac{1}{C_{ox}}} \dots\dots\dots 5.4$$

where,  $\Delta d = \frac{a \epsilon_2}{q}$ .

Using the parameters specified in Table 5.1, the value of  $V_{tl}$  has been calculated. The calculated value is,

$V_{tl} = -2.2608 \text{ V.}$
-------------------------------

The operating gate voltage range  $\Delta V_G$  is given by,

$$\begin{aligned} \Delta V_G &= V_{THp} - V_{tl} \\ &= (- 0.4592 + 2.2608 ) \text{ V} \\ &= 1.8016 \text{ V.} \end{aligned}$$

### 5.4 Effect of $d_1$ and $\delta$ on $V_{THp}$ and $V_{tl}$

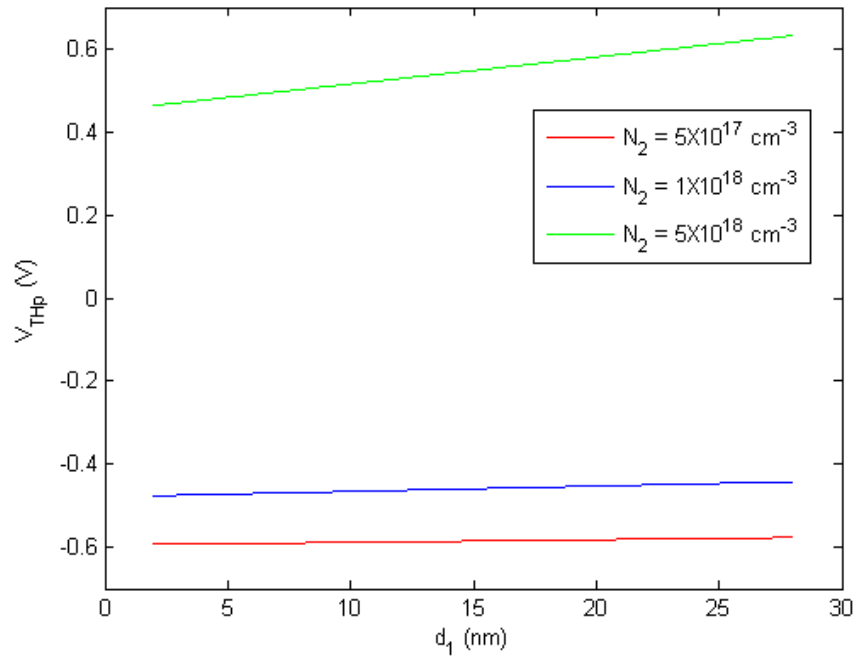
As discussed earlier, the value of the threshold voltage and the minimum gate bias can be tuned by varying the distance of the delta-doped layer from the oxide/Si interface and the width of the delta-doped layer. The effects of these two device parameters for different doping concentrations will be investigated in this section.

### ***5.4.1 Effect of $d_1$***

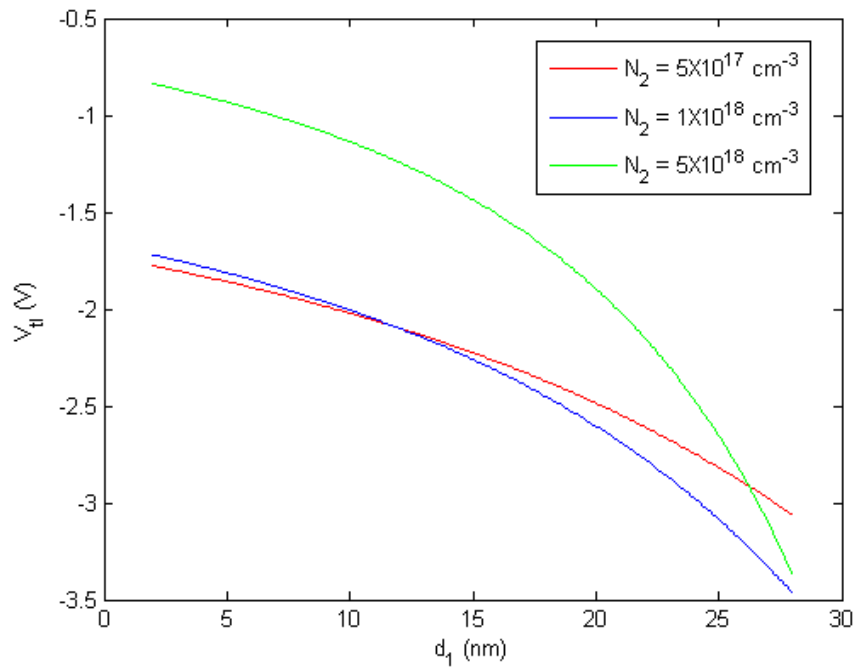
Figure 5.3(a) shows the  $d_1$  vs.  $V_{THp}$  plots for different doping concentrations. As expected by inspection of equation 5.2,  $V_{THp}$  varies linearly with the variation of  $d_1$ . For low doping concentration such as  $5 \times 10^{17} \text{ cm}^{-3}$ , the threshold voltage increases very slowly as the distance of the delta-doped layer from the oxide/Silicon interface is increased. At higher doping concentrations such as  $5 \times 10^{18} \text{ cm}^{-3}$ , the change of  $V_{THp}$  due to the change in  $d_1$  is steeper.

Figure 5.3(b) shows the  $d_1$  vs.  $V_{tl}$  plots for different doping concentration. As the delta-doped plane is moved away from the oxide/Silicon interface, the  $V_{tl}$  value goes down. The variation is nonlinear, as could be anticipated from equation 5.3. For low doping concentrations such as  $5 \times 10^{17} \text{ cm}^{-3}$ , the  $d_1$  vs.  $V_{tl}$  plot looks almost linear. On the other hand, at higher doping concentrations such as  $5 \times 10^{18} \text{ cm}^{-3}$ , the curvature of the plot become more dominant.

From the comparison of Figure 5.3 (a) and (b), it is evident that the operating voltage range  $\Delta V_G$  goes up as the delta-doped layer is moved away from the gate oxide. Also, for a fixed  $d_1$  value, the higher the doping concentration, the higher  $\Delta V_G$  is. On the other hand, if the delta-doped layer is placed very close to the channel, the mobility will be reduced. Thus, appropriate positioning of the delta-doped layer is very important.



(a)



(b)

**Figure 5. 3: (a)  $d_1$  vs.  $V_{THp}$  plot and (b)  $d_1$  vs.  $V_{th}$  plot of the p-channel delta-doped SiGe MOS-gate HEMT.**

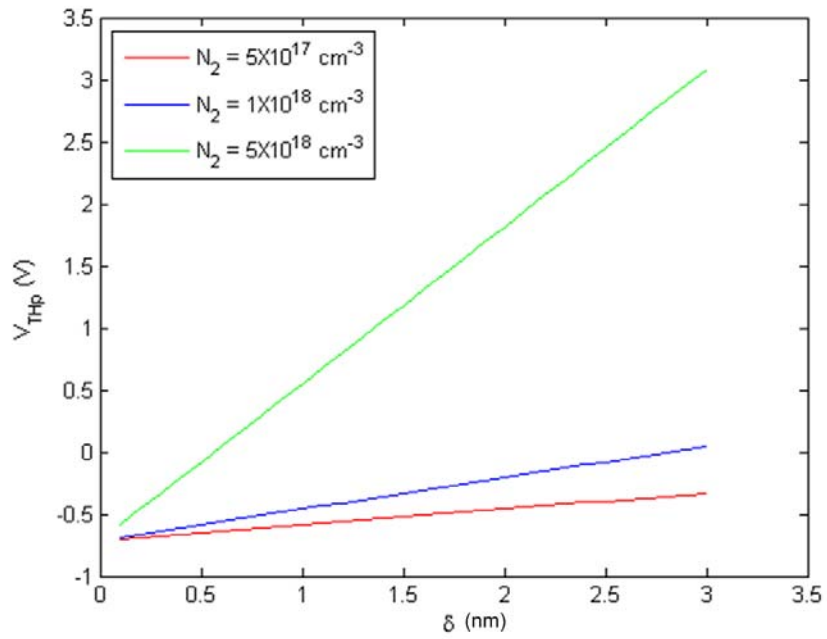
### ***5.4.2 Effect of $\delta$***

Figure 5.4 (a) shows the  $\delta$  vs.  $V_{THp}$  plots for three different doping concentrations. For low doping concentration,  $V_{THp}$  is weakly dependent on the  $\delta$  value. On the other hand, as the doping concentration increases, the threshold voltage shows significant sensitivity to the width of the delta-doped layer. Thus, for delta-doped MOS-gate HEMT with high doping,  $\delta$  is a very effective design parameter that can be used to control the threshold voltage value.

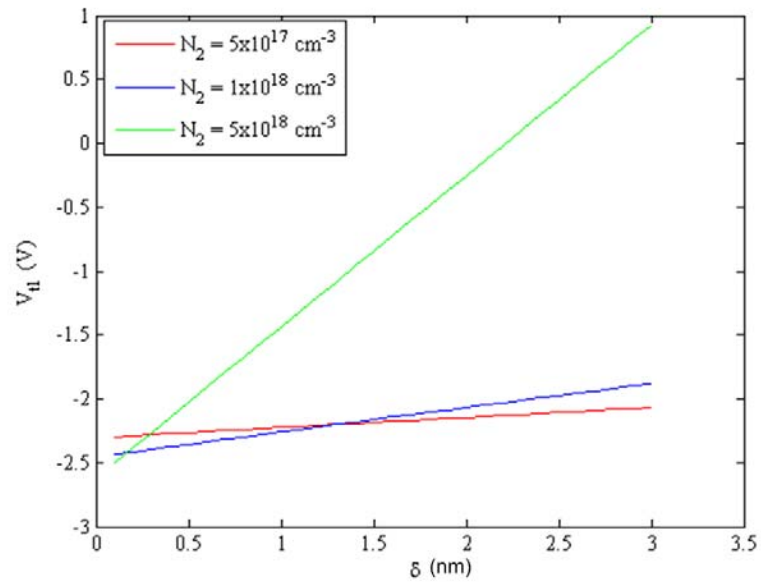
Figure 5.4 (b) shows the  $\delta$  vs.  $V_{tl}$  plots for different doping concentrations. The dependence of  $V_{tl}$  on  $\delta$  is similar to that of  $V_{THp}$ . For higher doping concentrations,  $V_{tl}$  becomes quite sensitive to the value of  $\delta$ . It should be noted that the nature of the  $\delta$  vs.  $V_{tl}$  plots differs from that of the  $\delta$  vs.  $V_{THp}$  plots as the  $\delta$  vs.  $V_{tl}$  plots for different doping concentrations intersect with each other which is not true for the  $\delta$  vs.  $V_{THp}$  plots.

## **5.5 Conclusions**

In Chapter 3, the dependence of  $V_{THp}$  and  $V_{Gmin}$  of the regular-doped HEMT on the device and material parameters has been discussed. In the case of a delta-doped HEMT, the device designer has two more parameters to play with:  $d_1$  and  $\delta$ . It is evident from the simulation results presented in this chapter that both  $d_1$  and  $\delta$  can be very helpful design



(a)



(b)

Figure 5. 4: (a)  $\delta$  vs.  $V_{THp}$  plot and (b)  $\delta$  vs.  $V_{d1}$  plot of the p-channel delta-doped SiGe MOS-gate HEMT.

parameters to achieve certain threshold voltage and operating voltage range for a delta-doped MOS-gate HEMT.

## Chapter 6

### *Medici<sup>TM</sup> Simulation of MOS-Gate HEMT*

In this chapter, the numerical simulations performed using the device simulator *Medici<sup>TM</sup>* will be discussed. Some of the simulation results will be directly compared to the results obtained from the analytical models presented in the previous chapters. The other simulations are used to investigate the device behavior and examine the dependence of device and material parameters on device performance.

#### **6.1 Brief Introduction To *Medici<sup>TM</sup>***

*Medici<sup>TM</sup>* is an industry-standard device simulator that can predict the electrical characteristics of arbitrary two-dimensional structures under user specified operating conditions. It is capable of simulating a broad range of devices including diode, BJT, MOSFET, JFET, MESFET, HBT, HEMT, IGBT, CCD and GTO.

*Medici<sup>TM</sup>* can help us to:

- Calculate and plot I-V characteristics, gain and speed of a device.
- Understand device physics and operation through calculating and plotting potential, field, band diagram, carrier concentration, mobility, etc.
- Calculate ionization rate and current density distributions.
- Analyze and understand breakdown mechanisms.

- Achieve optimal performance by refining device parameters.
- Study failure mechanisms, such as leakage paths and hot electron effects.
- Investigate transient radiation effects, such as single event and dose rate upset.

*Medici*<sup>TM</sup> is particularly suitable for devices that have structural variations in any two dimensions.

## 6.2 $V_{THp}$ and $V_{Gmin}$ for the MOS-gate HEMT

Figure 6.1 shows the gate voltage vs. drain current plot for small drain-source voltage ( $V_{DS}=-0.1V$ ). This simulation result has been obtained from *Medici*<sup>TM</sup> using a HEMT structure similar to the SiGe MOS-gate HEMT shown in Figure 3.1. From Figure 6.1, it is evident that the values of the threshold voltage and the minimum gate voltage are 2.45 V and 0.4 V, respectively. The threshold voltage and the minimum gate voltage obtained from the modified analytical model are 2.48 V and 0.57 V, respectively. Thus, the modified analytical model is capable of very closely predicting  $V_{THp}$  and  $V_{Gmin}$  at room temperature for MOS-gate HEMT.

## 6.3 Current Voltage Characteristics of the MOS-Gate HEMT

Figure 6.2 (a) shows the comparison between the  $V_G$  vs.  $I_{Dsat}$  plot obtained from *Medici* simulations and the one obtained using the modified analytical model. It is evident that



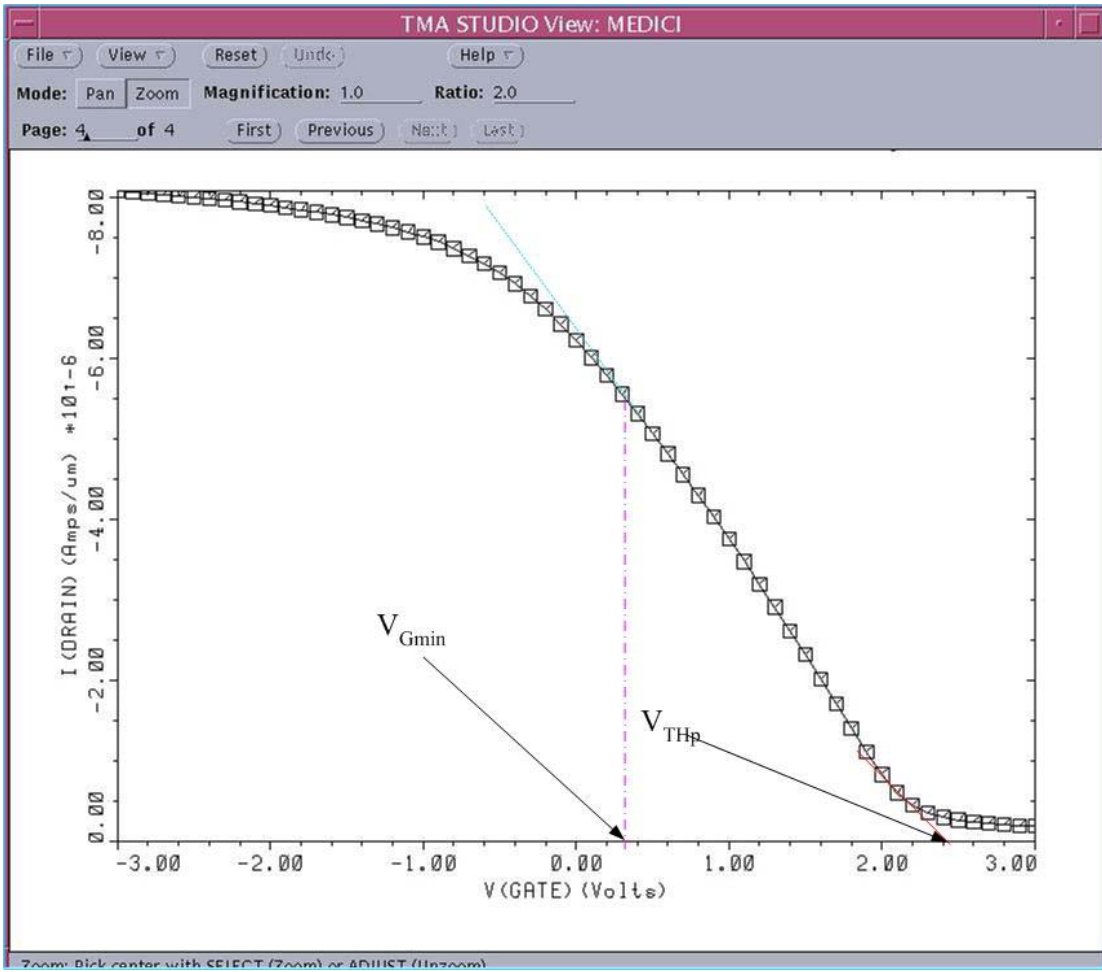
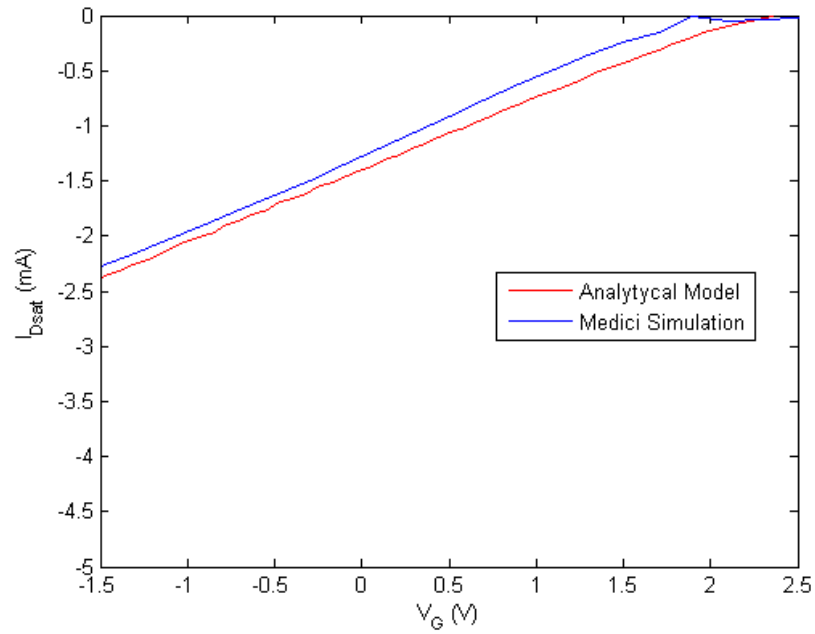
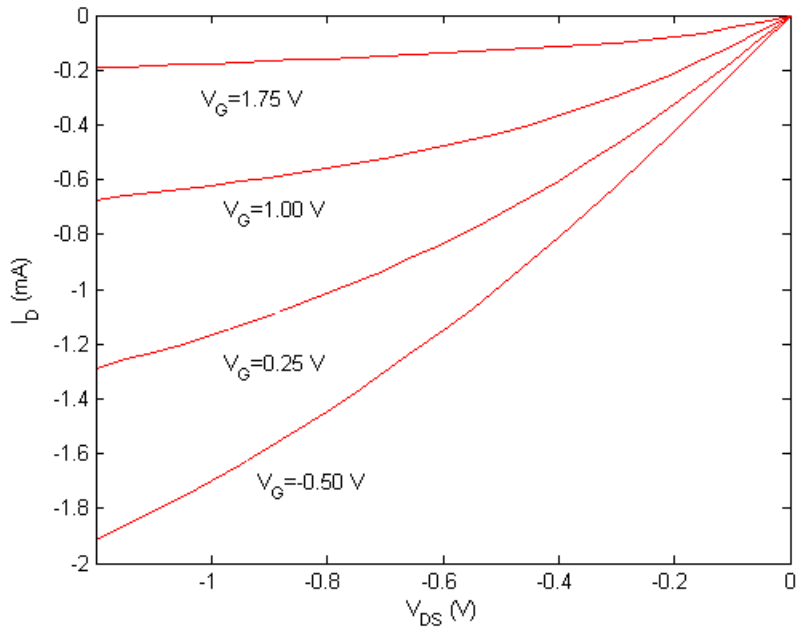


Figure 6. 1: *Medici*<sup>TM</sup> simulation result used to determine  $V_{\text{THp}}$  and  $V_{\text{Gmin}}$ .



(a)



(b)

**Figure 6. 2: (a) Comparison of  $I_{Dsat}$ - $V_G$  plot obtained from analytical model and Medici Simulation and (b)  $I_D$ - $V_D$  plot from *Medici*<sup>TM</sup>.**

the saturation currents estimated by the analytical model are very close to the currents estimated by *Medici*<sup>TM</sup> simulations. It should be noted that the current-voltage data obtained from *Medici*<sup>TM</sup> is used to plot the  $I_{Dsat}$ - $V_G$  characteristics in Matlab. It enables us to plot both results (analytical and Medici) on the same figure.

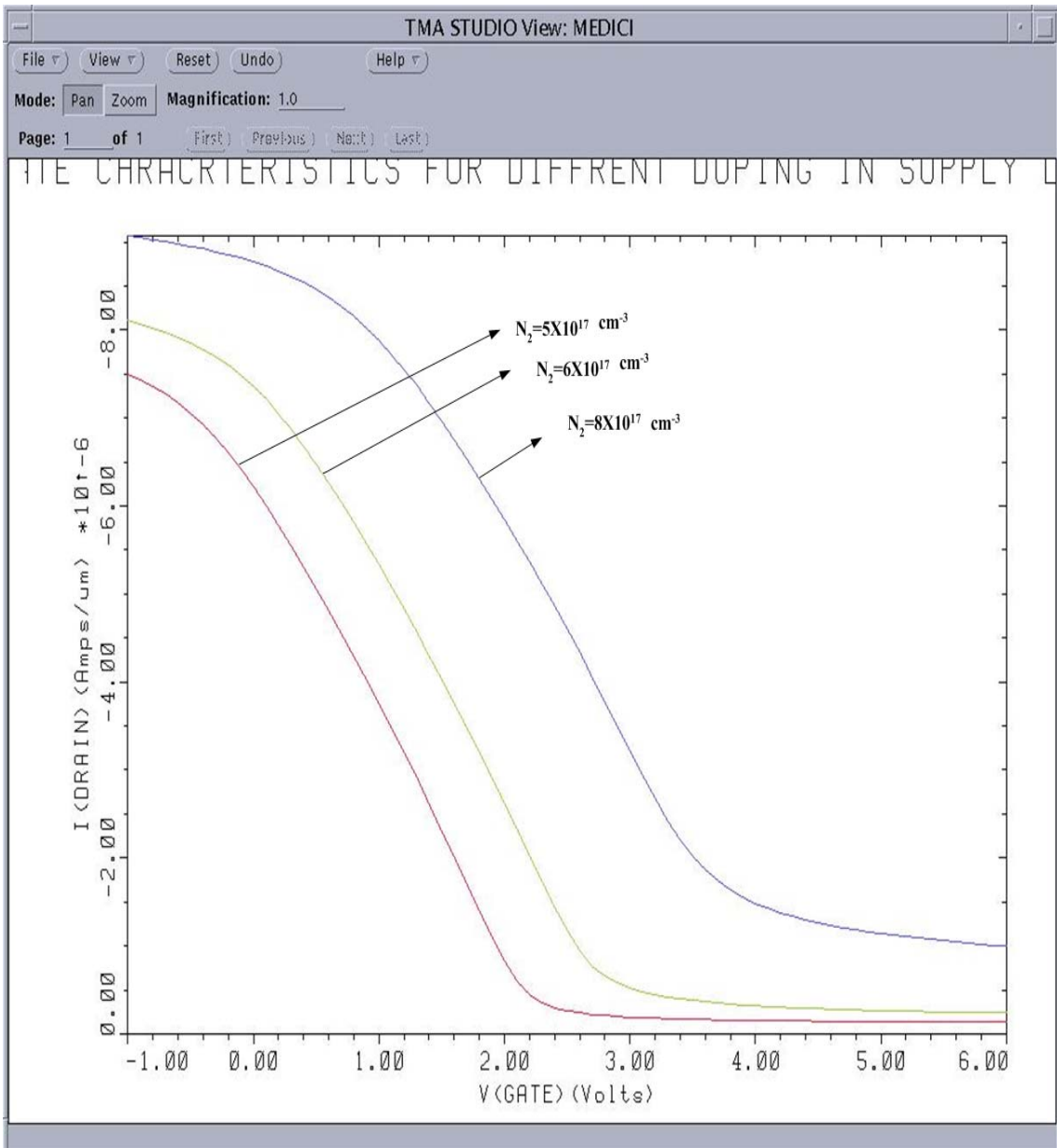
Figure 6.2 (b) shows the  $I_D$ - $V_D$  characteristics obtained from *Medici*<sup>TM</sup>. This  $I_D$ - $V_D$  characteristics differ from the  $I_D$ - $V_D$  characteristic found using analytical model by both shape and magnitude. As a result, they have not been plotted in the same figure. The differences between the  $I_D$ - $V_D$  characteristics might be explained by the following reasons:

- In the analytical model, a mobility value estimated from experimental result for strained-Ge channel has been used. On the other hand, while performing *Medici*<sup>TM</sup> simulations, bulk SiGe and Ge have been used to construct the device. The mobility value used by *Medici*<sup>TM</sup> has been examined and found to be lower than the value used in the calculations from analytical models.
- The saturation velocity value used in the calculations from analytical models is not very accurate. It is an estimated value. This estimated value has been used due to lack of a suitable analytical expression or experimental data for the saturation velocity in the strained-Ge channel.

- The Chang-Fetterman equation used in the analytical model considers only channel current. On the other hand, *Medici*<sup>TM</sup> is capable of calculating leakage currents besides the channel current.
- The basic Chang-Fetterman model has been used to calculate the current-voltage characteristics, which does not include the channel-length modulation effect.
- Also, the Chang-Fetterman equation does not include position-dependent mobility variation. Inclusion of the mobility variation along the direction normal to the heterointerface would improve the model.

## 6.4 Doping Concentration Dependence of $V_{THp}$

Figure 6.3 shows the  $I_D$ - $V_G$  characteristics (at low  $V_{DS}$ ) of the MOS-gate HEMT for different doping concentration of the supply layer. It is evident that with the increase in doping concentration, the threshold voltage shows significant increment. The  $V_{Gmin}$  value also increases almost the same amount. Thus, the operating voltage range ( $V_{THp} \sim V_{Gmin}$ ) remains almost constant with variation in the doping level. These results obtained from *Medici*<sup>TM</sup> simulations match quite closely with the results obtained from the analytical model. It should be noted that the subthreshold current becomes significant for high doping concentrations such as  $8 \times 10^{17} \text{ cm}^{-3}$ .



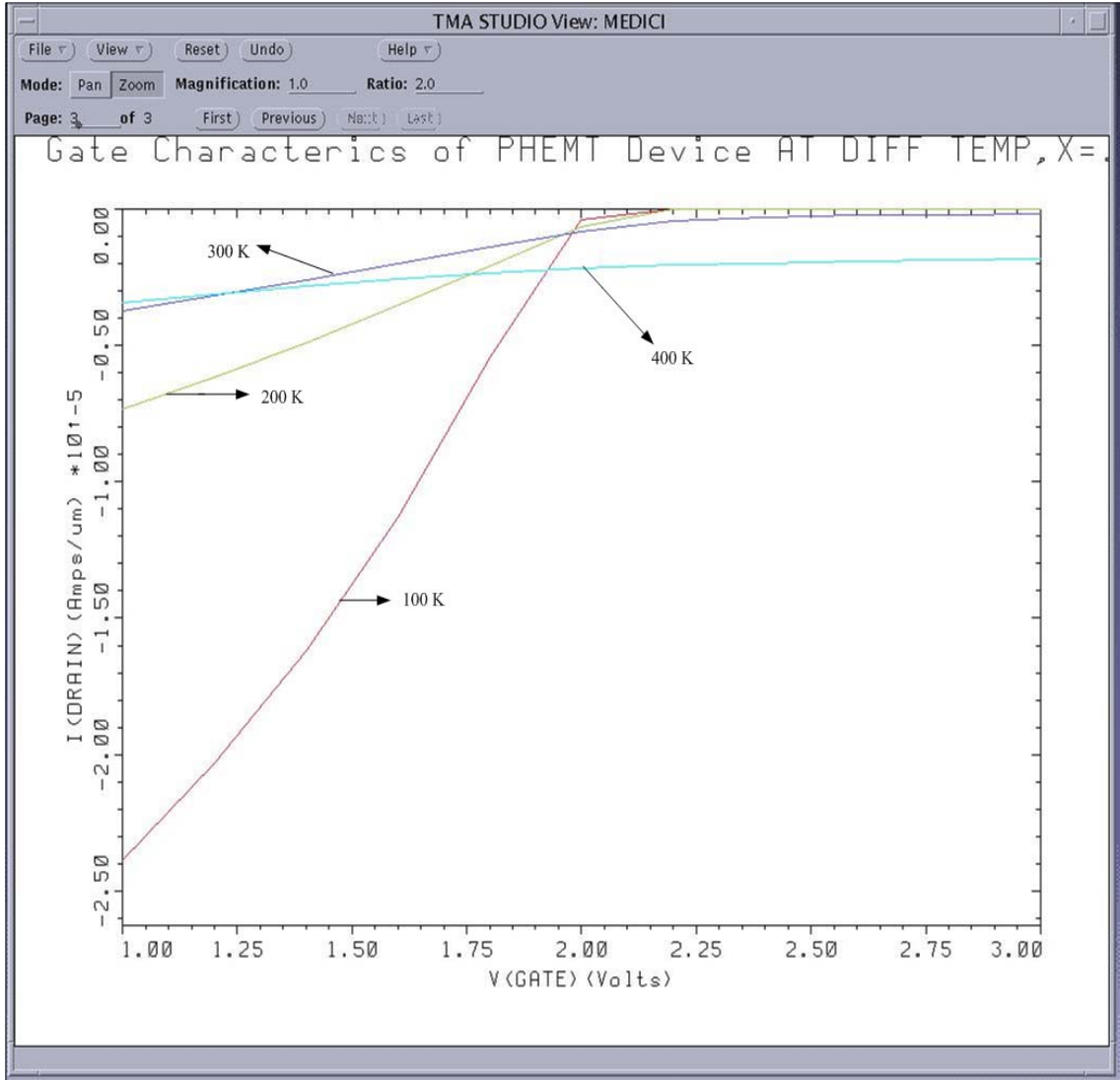
**Figure 6. 3:  $I_D$ - $V_G$  characteristics of the p-channel SiGe MOS-gate for different supply layer doping concentrations.**

## 6.5 The Temperature Variation of the Threshold Voltage

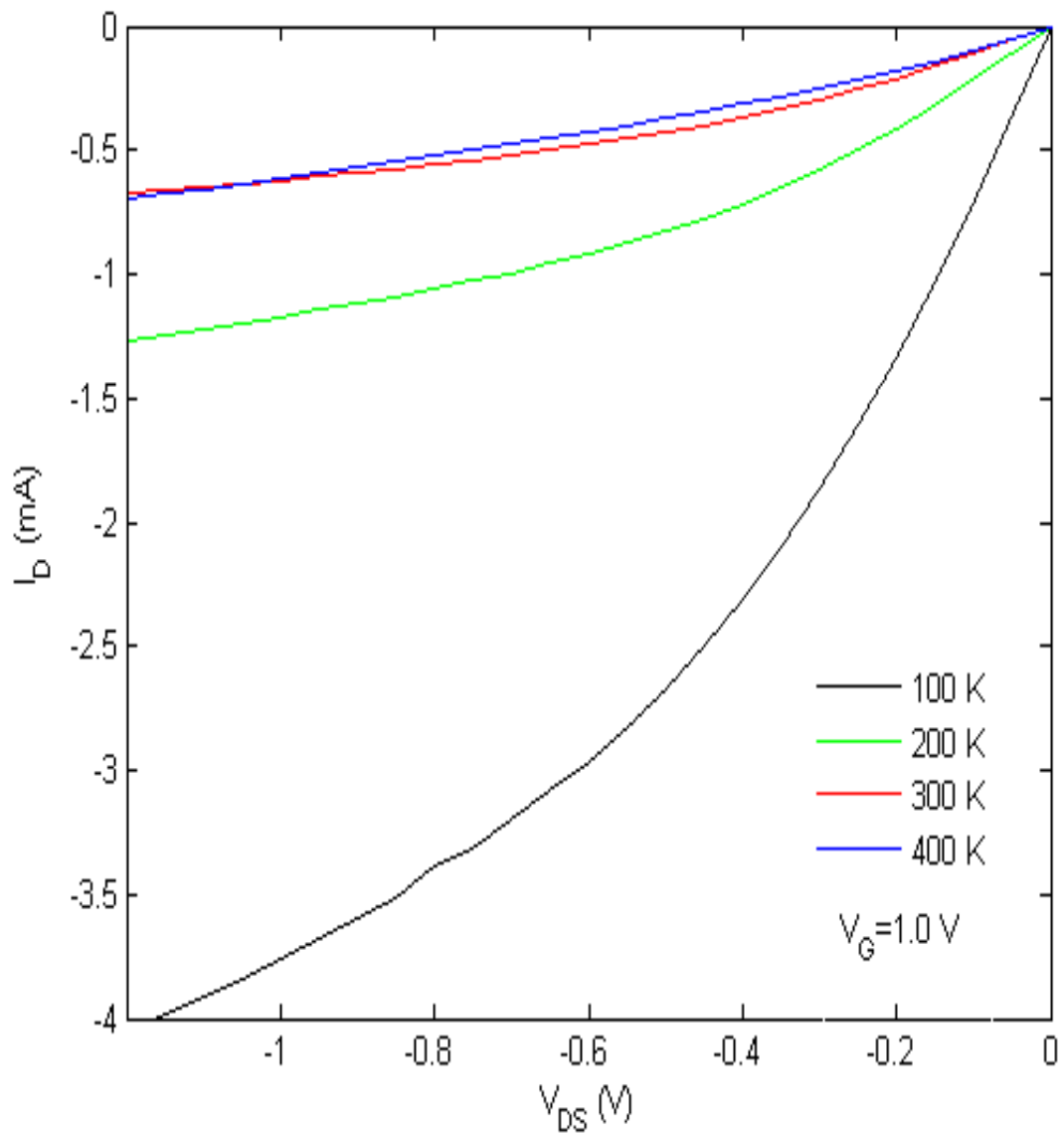
Figure 6.4 shows the  $V_G$  vs.  $I_D$  characteristics calculated by *Medici*<sup>TM</sup> at different temperatures. The threshold voltages at different temperatures can be determined from this plot. The  $V_{THp}$  values at 100 K, 200 K, 300 K and 400 K are 2.15 V, 2.25 V, 2.45 V and 2.6 V, respectively. Thus, *Medici*<sup>TM</sup> predicts a total of 450 mV variation in the threshold voltage as temperature changes from 100 K to 400 K, as opposed to only 90 mV change predicted by the analytical temperature model. This larger threshold voltage variation obtained from the *Medici*<sup>TM</sup> simulation might be the result of using bulk SiGe and Ge. The small threshold voltage variation predicted by the analytical model appears more realistic. Similar work on temperature behavior modeling of InGaAs HEMT [25] considers weak variation of threshold voltage with temperature.

## 6.6 The Temperature Dependence of the $I_D$ - $V_D$ Characteristics

Figure 6.5 shows the  $I_D$ - $V_D$  Characteristics at different temperature (at  $V_G=1.0$  V), obtained from the *Medici*<sup>TM</sup> simulation. Again, the  $I_D$ - $V_D$  Characteristics obtained from the *Medici*<sup>TM</sup> simulation differs significantly from the  $I_D$ - $V_D$  Characteristics obtained from the analytical temperature model. At very low temperature such as 100 K, *Medici*<sup>TM</sup> current values are substantially higher (almost 4 times) than the current values at 200 K, which is not true for the  $I_D$ - $V_D$  Characteristics of the analytical temperature model. It has been assumed in the analytical temperature model that the saturation velocity is



**Figure 6. 4: Temperature Variation of  $V_{THp}$  measured from  $I_D$ - $V_G$  plots at different temperatures.**



**Figure 6. 5: Comparison of  $I_D$ - $V_{DS}$  characteristics at different temperatures, obtained from *Medici*<sup>TM</sup> simulation.**

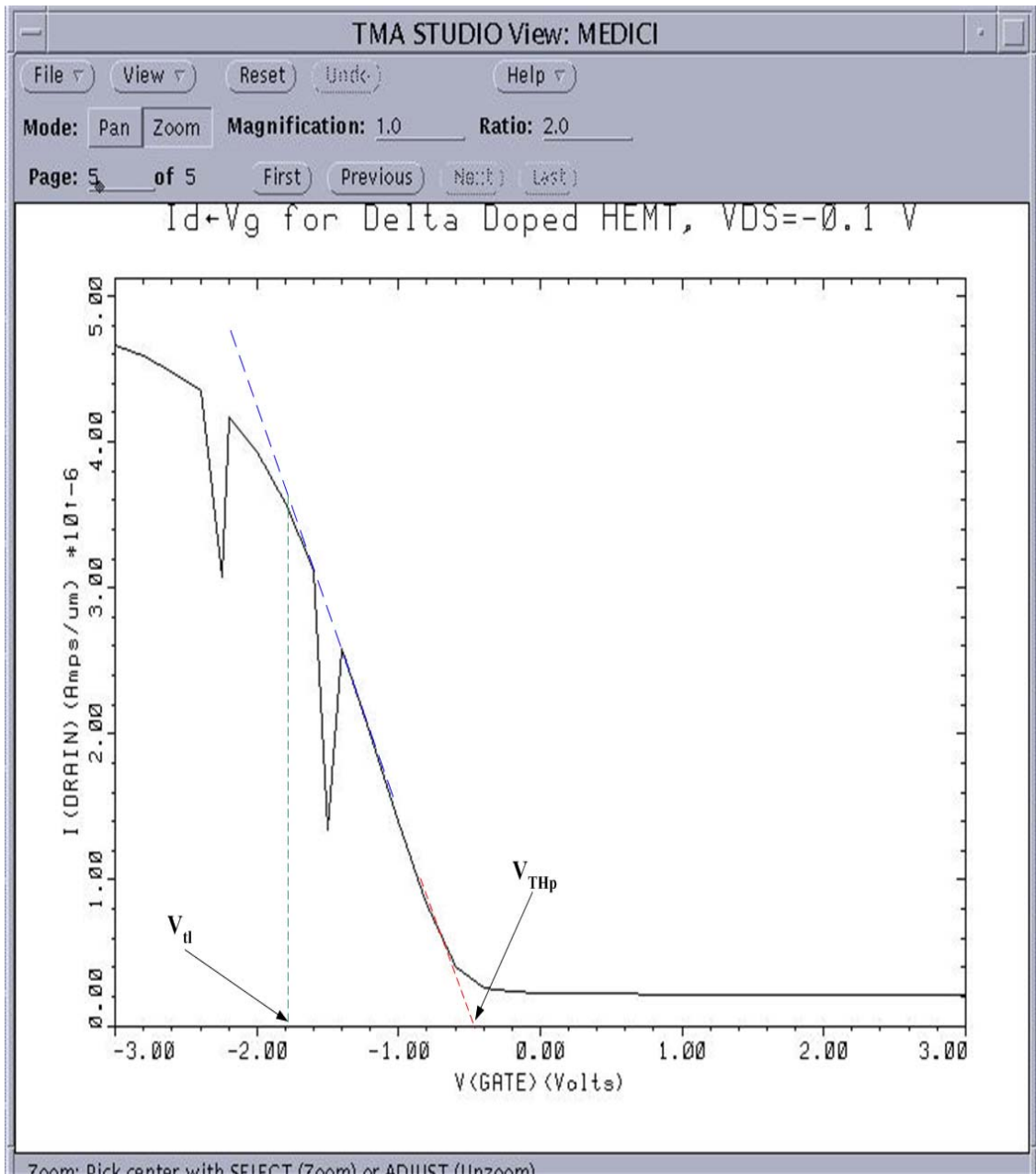


temperature independent, which is not true in practical cases. The saturation velocity normally goes up at low temperatures. The *Medici*<sup>TM</sup> simulations have certainly included the temperature dependence of the saturation velocity and thus, it calculated much higher current at low temperature. Also, *Medici*<sup>TM</sup> has used quite high mobility values at low temperatures.

## 6.7 $V_{THP}$ and $V_{tl}$ for Delta-Doped MOS-Gate HEMT

Figure 6.6 shows the  $V_G$  vs.  $I_D$  plot for small drain-source voltage ( $V_{DS}=-0.1V$ ) obtained from the *Medici*<sup>TM</sup> simulation for the delta-doped MOS-gate HEMT. The device structure is similar to the one used in the calculation from the analytical model. The threshold voltage value obtained from the figure is almost  $-0.5 V$ . This value is very close to the value ( $-0.46 V$ ) estimated by the analytical model calculation. On the other hand, the  $V_{tl}$  value extracted from the *Medici* plot is almost  $-1.8 V$ . The calculated value of the  $V_{tl}$  from the analytical model is  $-2.2 V$ . Thus, the  $V_{tl}$  value calculated from the analytical model is slightly overestimated.

In the derivation of the analytical expression of  $V_{tl}$ , it has been assumed that the real space hole transfer occurs when the maximum of the valence band touches the Fermi level. In practical cases, the hole transfer starts to occur when the distance between the maximum of the valence band and the Fermi level becomes comparable to the  $kT$  value. This is the reason for the difference between the minimum gate voltage value estimated by the analytical model and the *Medici*<sup>TM</sup> simulation. Although the prediction of the  $V_{tl}$



**Figure 6. 6:** *Medici*<sup>TM</sup> simulation results used to determine  $V_{THp}$  and  $V_{th}$  for the p-channel delta-doped SiGe MOS-gate HEMT.

value is not very close, the analytical model is able to provide us with a rough idea about the operating voltage range of the delta-doped MOS-gate HEMT.

## 6.8 Discussion

In this chapter, the results obtained from the analytical models and the *Medici*<sup>TM</sup> simulations have been shown. Usually, the analytical models are used in the first stage of the device design process or to get a rough idea of the behavior of an existing device. To get a more accurate idea, a numerical simulation software such as *Medici*<sup>TM</sup>, *Davinci*<sup>TM</sup>, etc. can be used. One has to be careful while using a complicated software such as *Medici*<sup>TM</sup> as it offers a wide variety of device parameter models and other simulation options. Careful selection of the models is the first step to obtain the realistic results from the simulations. One has to have an idea about the qualitative behavior and physics of the device under investigation.

As a whole, the comparison between the analytical model and *Medici* simulation is satisfactory. In cases where big differences between the results of the analytical model and the *Medici*<sup>TM</sup> simulations have been observed, the possible reasons behind the differences have been discussed.

# Chapter 7

## *Conclusions*

### 7.1 Summary of the Work

It is evident from the discussions in the previous chapters that the realization of the MOS-gate HEMT is a very important step toward the integration of the HEMT into CMOS circuits. Despite some fabrication difficulties, the MOS-gate HEMT demonstrates better performance than a metal-gate HEMT and holds great promise for high-frequency, low-noise circuits. For the design and analysis of the MOS-gate HEMT, an accurate analytical model is very important. In this work, an analytical model has been proposed which is better than the existing model and the results from the *Medici*<sup>TM</sup> simulations have been compared to those obtained from the analytical model. For some of the cases the results match closely, while in others there exists difference between the results. Efforts have been made to explain the possible reasons for the differences. The work achieved in this thesis is summarized below:

- A modified model for the threshold voltage and the minimum gate voltage of the SiGe MOS-gate HEMT has been proposed. The values of  $V_{THp}$  and  $V_{Gmin}$  have been calculated using the parameters of a 0.7- $\mu\text{m}$  gate length p-channel SiGe MOS-gate HEMT. The calculated results have shown excellent agreement with the  $V_{THp}$  and  $V_{Gmin}$  values calculated by the *Medici*<sup>TM</sup> simulations. The threshold

voltage value obtained from the analytical model differs only by 0.03 volts from the value obtained by the *Medici*<sup>TM</sup> simulation.

- The p-channel SiGe MOS-gate HEMT discussed in this thesis contains strained SiGe and Ge layers. As the properties of the strained material such as the bandgap, the band-discontinuity, etc. vary from the bulk material; care has been taken to include the strain-dependent material parameters in the calculations.
- The modified model, along with the Chang-Fetterman equation, has been used to calculate the current-voltage characteristics, transconductance and cutoff frequency. The comparison of the current-voltage characteristics calculated using the analytical model and those obtained from the *Medici*<sup>TM</sup> simulations revealed some difference between them. The reasons for the differences include the difference in the mobility values and the saturation velocity values used in the two methods (*Medici*<sup>TM</sup> and analytical model calculation).
- Using the modified model, the effects of different material and device parameters on the threshold voltage, the minimum gate voltage and the gate voltage swing have been investigated. Some of the results have been compared with the *Medici*<sup>TM</sup> simulations.
- An analytical model for predicting the temperature dependence of the MOS-gate HEMT has been presented. The threshold voltage variation due to the temperature

variation calculated from this model is smaller than the variation predicted by the Medici simulations. The total variation predicted by *Medici*<sup>TM</sup> is almost five times the total variation obtained from the analytical model. It has been justified that the result obtained from the analytical model appears more acceptable.

- The temperature variations of the current-voltage characteristics have been calculated using the temperature model and compared with the results of the *Medici*<sup>TM</sup> simulations. The differences between the results have been explained.
- A new model for the delta-doped MOS-gate HEMT has been proposed, which is valid for any width of the delta-doped layer and any distance of the delta-doped layer from the oxide interface. The threshold voltage  $V_{THp}$  and the minimum gate voltage  $V_{tl}$  of a delta-doped p-channel SiGe MOS-gate HEMT have been calculated using this model. The calculated values are very close to the values obtained from the *Medici*<sup>TM</sup> simulation results.
- The effects of doping concentration, width of the delta-doped layer, etc. on  $V_{THp}$  and  $V_{tl}$  of the delta-doped MOS-gate HEMT have been investigated using the new model.
- *Medici*<sup>TM</sup> simulations have been performed to compare the results obtained from the calculations using the analytical models. Also, the simulations have been used to explore the device behavior of the SiGe MOS-gate HEMT under investigation.

## 7.2 Future Work Directions

To improve the analytical models, the following works may be done in the future:

- The Chang-Fetterman equation [22] does not include the mobility variation along the direction normal to the heterointerface. Instead of using a constant mobility, if a mobility model is used, which includes the variation of mobility along the direction normal to the heterointerface, a better estimation of the current-voltage characteristics can be obtained.
- Better estimations of the mobility value and the saturation velocity are required to obtain better results from the analytical model. Use of the Monte Carlo method or other numerical simulation methods may help to calculate better mobility and saturation velocity values. The temperature dependence of the mobility and the saturation velocity should also be calculated using numerical simulation.
- The best way of getting realistic values of the mobility and saturation velocity of a strained Ge channel grown on cubic SiGe is to fabricate a SiGe p-channel MOS-gate HEMT, and determine the mobility and saturation velocity values from the experimental data. Once the data is obtained, it can be used later for any calculation from the analytical model of the p-channel SiGe MOS-gate HEMT.

- Also, if the experimental current-voltage characteristics are available, the current-voltage characteristics obtained from the analytical model can be fitted to the experimental data. The fitting parameters can be included as part of the analytical model. Thus, the analytical model can be ameliorated.
- The shape of the quantum well formed in the heterojunction depends on the width of the channel layer and also the composition and doping of the virtual substrate. Including the effects and solving the Schrödinger equation for the quantum well, a better and more realistic expression for the charge density in the channel can be obtained.



## References

1. H. Craig Casey, "Devices for Integrated Circuits.", John Wiley and Sons, Inc., 1999.
2. R. J. Baker et al., "CMOS Circuit Design, Layout, and Simulation", Prentice Hall of India, 2003.
3. [http://www.rpi.edu/~schubert/Educational%20resources/1982%20First%20HEMT%20\(Fujitsu%20Corp%20Japan\).jpg](http://www.rpi.edu/~schubert/Educational%20resources/1982%20First%20HEMT%20(Fujitsu%20Corp%20Japan).jpg).
4. E. Murakami et al, "Strain-controlled Si-Ge modulation-doped FET with ultrahigh hole mobility", IEEE Electron Device Letters, Vol. 12, No. 2, pp. 71-73, February 1991.
5. G. -W. Wang et al., "A 0.1 $\mu$ m Al<sub>0.5</sub>In<sub>0.5</sub>As/Ga<sub>0.5</sub>In<sub>0.5</sub>As MODFET fabricated on GaAs substrate," *IEEE Trans. Electron Devices*, vol. 35, pp. 818-823, 1988.
6. F. Aniel et al., "High performance 100 nm T-gate strained Si/Si<sub>0.6</sub>Ge<sub>0.4</sub> n-MODFET", *Solid-State Electronics*, Vol. 47, Issue 2, pp. 283- 289.
7. S. Hiyamizu et al., "High mobility of two-dimensional electrons at the GaAs/AlGaAs Heterojunction interface", *Applied Phys. Lett.*, vol. 37, Issue 9, pp. 805-807.
8. S. Madhavi et al., "High room-temperature hole mobility in Ge<sub>0.7</sub>Si<sub>0.3</sub>/Ge/Ge<sub>0.7</sub>Si<sub>0.3</sub> modulation doped heterostructure." *Journal of Applied Physics*, Vol. 89, Number 4, pp. 2497-2499.
9. Braunstein et al, " Intrinsic optical absorption in Germanium-Silicon alloys.", *Phys. Rev.*, Vol.109, Issue 3, pp. 695-710, 1958,
10. Rieger et al, "Electronic-band parameters in strained Si<sub>1-x</sub>Ge<sub>x</sub> alloys on Si<sub>1-y</sub>Ge<sub>y</sub> substrates.", *Phys. Rev. B*, 48, 14276-87, 1993.
11. R. People et al, "Band-alignments of coherently strained Ge<sub>x</sub>Si<sub>1-x</sub>/Si heterostructures on <001> Ge<sub>y</sub>Si<sub>1-y</sub> substrates", *Appl. Phys. Lett.*, vol 48, No. 8, pp. 538-540, 1986.
12. Weber et al, "Near-band-gap photoluminescence of Si-Ge alloys.", *Phys. Rev. B*, Vol. 40, Issue 8, pp.5683-93, 1989.
13. S M Sze, "Semiconductor Devices: Physics and Technology", John Wiley and sons, 1985.
14. D J Robbins et al, "Near-band-gap photoluminescence from pseudomorphic Si<sub>1-x</sub>Ge<sub>x</sub> single layers on Silicon.", *J. Appl. Phys.*, Vol. 71, Issue 3, pp. 1407-1414, 1992.
15. Michel E. Levinstein et al, "Properties of Advanced Semiconductor Materials", John Wiley and sons, 2001.
16. F. Jain et al, "Analysis of self-aligned MOSFETs with modulation-doped SiGe channels.", *Solid State Electronics*, Vol. 36, No. 11, pp.1613-18, 1993.
17. Chang et al., "An analytical model for HEMT's using new velocity field dependence.", *IEEE Transaction on Electron Devices*, Vol. 34 No. 7, pp. 1456-1462.

18. Wu Lu et al, "High performance 0.1 mm gate-length p-type SiGe MODFET's and MOS-MODFET's.", IEEE Transactions on Electron Devices, Vol. 47, No. 8, pp. 1645-1652, 2000.
19. Gaspari et al, "Effect of temperature on the transfer characteristics of a 0.5 mm-gate Si:SiGe depletion-mode n-MODFET.", Applied Surface Science, Vol. 224, Issues 1-4, pp. 390-393, 2004.
20. J E Velazquez et al., "Design of nearly body-effect free Si/SiGe MODFETs.", 8<sup>th</sup> IEEE International Symposium on High Performance Electron Devices for Microwave and Optoelectronic Applications, pp. 32-37, 2000.
21. Michael Shur, "GaAs Devices and Circuits", Plenum Press, 1986.
22. Chang et al, "An analytical model for high-electron-mobility transistors.", Solid State Electronics, Vol. 30, No. 5, pp. 485-491, 1987.
23. S O Kasap, "Principles of Electronic Materials and Devices", Tata McGraw-Hill Publishing Company Limited, 2002.
24. Gokhale et al, "Enhanced Performance of PMOS and CMOS Circuits Using Self-Aligned MOSFETs With Modulation Doped Si-Ge Channel", Proc. Tenth Biennial University Government Industry Microelectronics Symposium, pp219-222, May, 1993.
25. B González et al., "Characteristics of extrinsic resistances in temperature behaviour modelling of InGaAs MODFETs", Semicond. Sci. Technol., Vol.19, pp. 648-654, 2004.

## VITA

Mohammad Tanvir Alam was born in Mymensingh, Bangladesh, on November 20, 1977. In 2002, he received his Bachelor's degree in Electrical and Electronic Engineering from Bangladesh University of Engineering and Technology, Bangladesh. He was awarded the dean scholarship in junior and senior year of his undergraduate studies. Also, he got first prize in two inter-university electronic project competition.

In January 2003, he joined the University of Tennessee, Knoxville (UTK), as a Masters student in the Department of Electrical and Computer Engineering. Before joining UTK, he worked in Bangladesh University of Engineering and Technology as a research engineer. During his Masters studies, he has worked in different research projects including "Design and implementation of dose control circuits (DCC) for carbon nanofiber emitter-based massively parallel lithographic systems", Artificial retina project, etc. He has worked in Oak Ridge National Laboratory as a part of his Graduate Research Assistantship (GRA). He has also worked as a teaching assistant in the Department of Electrical and Computer Engineering and as a tutor in the Black Cultural Center, UTK.

### Publications:

- "Temperature Dependency of MOSFET Device Characteristics in 4H- and 6H-Silicon Carbide (SiC)", by Md. Hasanuzzaman, S.K. Islam, L. Tolbert and **M.T. Alam**, *Journal of Solid State Electronics*, 48(10-11), 2004, p.1877.
- "Temperature Dependency of MOSFET Device Characteristics in 4H- and 6H-Silicon Carbide (SiC)", by Md. Hasanuzzaman, S.K. Islam, L. Tolbert and **M.T.**

**Alam**, *Intl. Semiconductor Device Research Symposium (ISRDS)*, December 10-12, 2003, Washington DC, pp. 132.

- “Spin-Polarized Electron Injection into Semiconductor: Prospects, Problems and Possible Solutions”, by **Mohammad T. Alam**, Changgan Zeng, H.H. Weitering, Syed K. Islam and Md. Hasanuzzaman, *IEEE NTC Quantum Device Technology Workshop*, May 17-21, 2004, Clarkson University, Potsdam, NY.
- “ Multi-Channel Piezoresistive Micromechanical Sensor Readout System”, by Zhiyu Hu, Nazmul Islam, **Mohammad T. Alam**, Syed K. Islam and Thomas G. Thundat, *MRS 2004 Spring Meeting*, April 12 – 16, 2004, San Francisco, CA.
- “Miniature Multi-Channel High-sensitivity Implantable MEMS Pressure Sensor and CMOS Readout System” by Zhiyu Hu, Dechang Yi, Nazmul Islam, **Mohammad T. Alam**, Syed Islam, Arnab Choudhur and Thomas Thundat , 207<sup>th</sup> ECS meeting, May 15-20, 2005, Quebec City, Canada.
- “Design and Development of a Commercial Microcontroller based Solid State Prepayment Energy Meter”, by S.M.L. Kabir, S.M.S. Hasan, Touhidur Rahman, **M. T. Alam**, Abi A. Al Mamun and Md. Kamruzzaman., *BES Conference 2003*, April 25-27, 2003, Dhaka, Bangladesh.