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High-current integrated battery chargers for mobile applications

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To the Graduate Council:

I am submitting herewith a thesis written by Gabriel Alejo Gabian entitled "High-current integrated battery chargers for mobile applications." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Daniel Costinett, Major Professor

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High-current integrated battery chargers for mobile applications

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Al Nono. Sigamos creando...

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Abstract

Battery charging circuits for mobile applications, such as smart phones and tablets, require both small area and low losses. In addition, to reduce the charging time, high current is needed through the converter. In this work, exploration of the Buck, the 3-Level Buck and the Hybrid Buck converter is performed over the input voltage, the total FET area and the load current. An analytical loss model for each topology is constructed and constrated by experimental results. In addition, packaging and bond wire impact on on-chip losses is analyzed by 3D modeling. Finally, a comparison between the topologies is presented determining potential candidates for a maximum on-chip loss of 2 W at output voltage of 4 V and 10 A of output current.

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Chapter 1

Introduction

Every year, a new smartphone comes to market with a bigger screen, a faster processor, more radios, etc. This additional features requiere more power from the battery. However, battery capacity has not followed this trend over the last years. Figure 1.1 shows how for a generation of a specific smart phone, battery capacity has remained almoast flat. This implies that users have to charge their terminals more often. Industry is continusly trying to reduce the charging time of mobile terminals. Qualcomm has released the 4th generation of Quick Charge. A battery charger that reduces the charging time by a communication between the smart phone and the wall charger, where the input voltage for the charger can

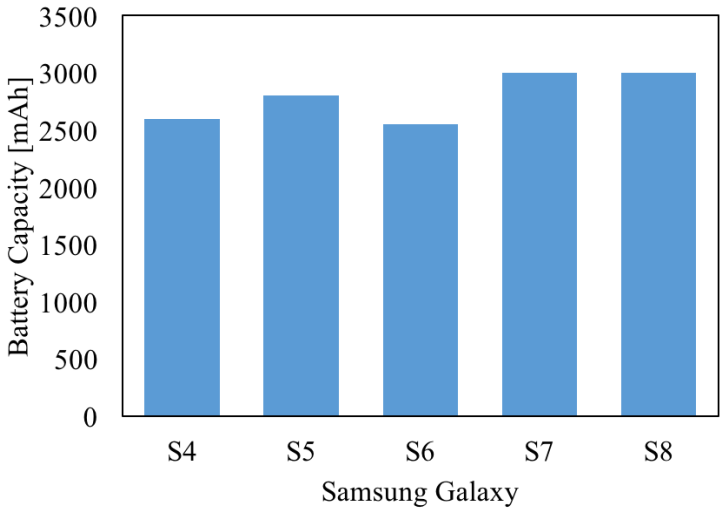


Figure 1.1: Battery capacity evolution for the Samsung Galsy S series.

be handshaked to achieve a more efficient power conversion.

Portable devices, such as smart phones, tablets and wearables have increased the use of Li-ion batteries due to their lower weight, lack of memory and higher power density when compared to other energy storage technologies such as Nickel Metal Hydride (NiMH) and Nickel-Cadmium (NiCd). However, Li-Ion batteries are more sensitive to over charge, over temperature and over current than other types of batteries. Thus, a specific charging profile must be followed in order to prevent battery damage and to extend battery life. Figure 1.2 shows the charging current and voltage for a Li-ion battery. There are three different states that must be met:

- Pre-charge: When the battery voltage is below a threshold (V_{TH}), a low current has to be applied (I_{pre-ch}). Normally, this state is never reached as the system will prevent a full discharge of the battery.
- Constant Current: When the battery voltage is between the threshold and the regulation voltage, the current is increased and held constant (I_{ch}) until the regulation voltage V_{reg} is detected (approximately 3.7 V).
- Constant Voltage: When the regulation voltage is reached, a constant voltage is applied.

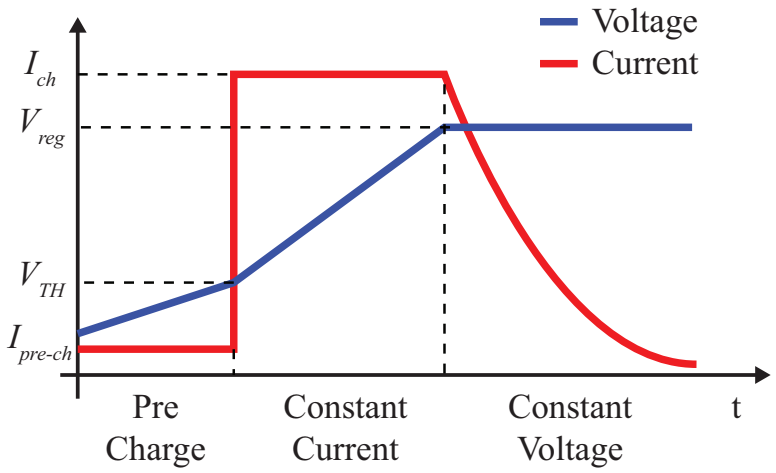


Figure 1.2: Li-Ion batteries charging profile.

Applying a higher current during the constant-current phase will decrease the total charging time. Li-Ion batteries maximum charge current is 1C, therefore, if the battery capacity is 3000 mAh the maximum current is 3 A. However, most recent batteries have increased ion mobility allowing higher charging currents which creates an opportunity for fast charging battery chargers [1]. Table 1.1 shows a list of the highest current commercial available battery chargers from three different manufacturers. These parts integrates the power stage along with control and gate driver circuitry. The maximum charging current is 5 A, meaning that the charging time for a 3000 mAh battery is 36 minutes. If the charging current is doubled, a mobile phone with this battery will be fully charged in less than 20 minutes.

A thermal limitation exists for the design of battery chargers for mobile applications. Portable devices can not include heat sinks due to dimension restrictions, in particular, thickness. Thus, losses are limited to the maximum temperature rise on the die inside the package. Junction to air thermal resistance, Θ_{JA}, represents the ability of a package to dissipate heat from the surface of the die to ambient. It is related to the power loss on the die as

$$\Theta_{JA} = \frac{T_J - T_A}{P_{loss}} \tag{1.1}$$

where T_J and T_A represents the temperature of the die and air respectively. As a consequence, for a given package, there is a maximum power loss that can be produced on chip in order to keep the die at a certain temperature. Commercial packages can have thermal resistance values of 30°C/W [2] and it is desirable to keep the temperature rise on the die below 60°C to prevent heating up the phone while charging. An easy solution would be to take the power switches out of the chip and use discrete devices. By doing this, better perfomance

Table 1.1: Commercial available battery charger ICs

Part Number	V_{in}	$I_{ch,max}$	f_s	η @ $I_{ch,max}$	P_{loss}	Size
BQ25890H	12 V	5 A	1.5 MHz	89%	2.1 W	4 mm x 4 mm
MAX8971	7.5 V	1.5 A	3 MHz	89%	0.65 W	1.62 m x 1.62 mm
RT9451	12 V	4 A	375 kHz	88%	1.44 W	4 mm x 4 mm

devices can be used at the expense of a larger footprint area. However, small size is also a requirement on mobile electronics.

1.1 Summary

In order to reduce the charging time of batteries on mobile applications, the charging current has to be increased while maintaining small footprint and high efficiency. Power dissipation is restricted to a maximum temperature rise of 60°C on the die. By adopting a package thermal resistance of 30°C/W, a maximum loss on-chip is set to 2 W. The following chapters will explore different topologies and their performance to double the charging current for mobile battery chargers. Each topology will be analyzed over an input voltage range from 5 V to 12 V, a maximum load current of 10 A and an output voltage of 4 V.

Chapter 2

Literature Review

2.1 Battery charger's topologies

Battery chargers are most commonly implemented as linear or switching DCDC converters (Figure 2.1). The choice of topology will depend on the final application, but a brief comparison is presented on Table 2.1. Linear converters use a pass transistor to drop the excess input voltage in order to achieve output regulation by modulating its resistance. The main advantage of this topology is the reduced size (for low to medium powers) and simplicity. However, losses depend on the voltage difference between the input voltage and the output voltage and the load current. Assuming an input voltage of 5 V and a charging current during the constant current phase of 1 A, this type of charger can exhibit up to 1 W of losses. LDO-based battery chargers are implemented in [3, 4, 5, 6], where constant currents ranging from

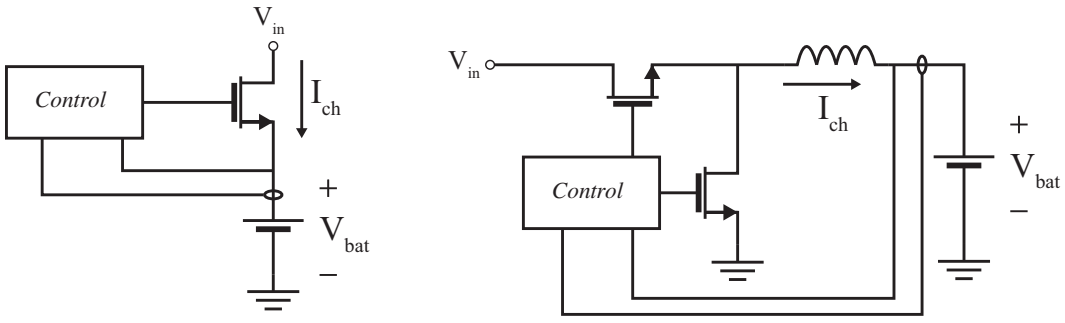


Figure 2.1: Commonly used topology for battery chargers for portable applications.

Table 2.1: Linear vs Switching

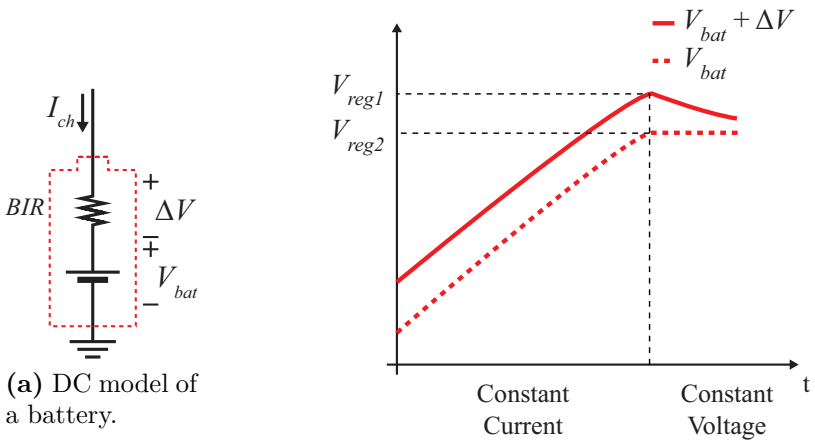
	Linear	Switching
Efficiency	Low	High
Complexity	Low	Medium
Size	Small-Medium	Lower at high power[†]
Input Voltage range	Low	Large

[†] Depends on switching frequency

350 mA to 1 A are used to charge Li-Ion batteries. Switching converters for battery chargers are most commonly implemented as buck converters. Using a switching power stage and a low pass filter to step down the input voltage lower losses than linear converters can be achieved. When comparing size, at low power linear converters are smaller, but at high powers buck converters tend to be smaller. However, this will depend on the switching frequency as it will be addressed further. Buck-based battery charger implementations are presented in [7, 8, 9, 10] with charging currents ranging from 300 mA to 2 A.

2.2 Fast charging

The charging process does not requiere a complex model for the battery. A Thevenin equivalent circuit including the open circuit voltage and a series resistance is shown in Figure 2.2a. The built-in resistance (BIR) adds an extra voltage drop when measuring the voltage while charging the battery. Recalling from Figure 1.2, the change to the constant voltage phase occurs when the measured voltage reaches a certain value. When this phase is reached, the only action of a charger is to sustain the regulation voltage while the current drops. The BIR produces a voltage measurement in excess, making the charger switch phases earlier. This ends in a longer charging time as the current during the constant voltage period is much smaller than in the previous stage. In [11, 12] a linear battery charger implements BIR correction by applying two different current values successively during the constant current phase while the battery voltage is measured. Then, with both pairs of measurements (V_1, I_1) and (V_2, I_2), the BIR is estimated continuously and the monitored voltage is compensated. In [8, 13], the slope of the inductor current in a buck-based charger



(a) DC model of a battery.

(b) BIR effect on measured battery voltage.

Figure 2.2: Built in resistance effect.

is used to derive an expression of the battery resistance. Li-ion batteries can not be charged at currents greater than 1 C to avoid overheating. However, today's batteries have increased ion mobility making possible to reduce the charging time by applying larger currents. Portable devices not only require small footprint converters but also high efficiency performance (as it is explained in Chapter 1) to avoid heating up the terminal while it's being charged.

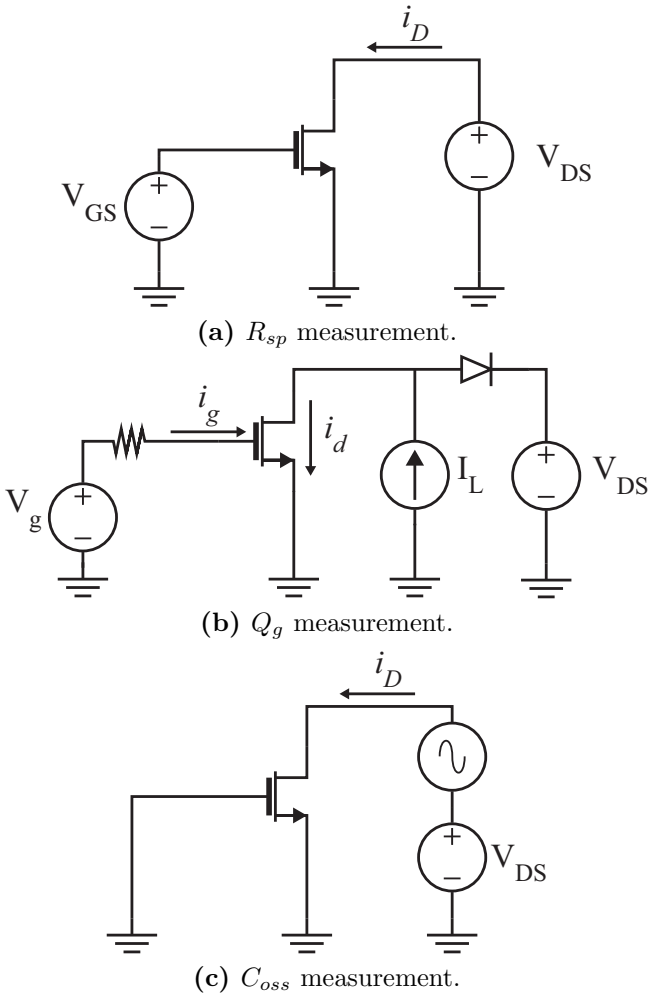
2.3 Integrated power converters

2.3.1 Modeling

Because IC FETs can be sized, loss models for integrated power converters utilize per area or per width parameters to specify MOSFET parasitics [14]. Doing this facilitates the design of converters by expressing its performance in terms of switch's dimensions [15, 16]. Table 2.2 shows parameters and units for each element. These parameters can be extracted using a test device with a given W/L ratio. Normally, for a power device the length is chosen to be the minimum allowable on the technology to minimize the device area. Circuits used to characterize the parameters of Table 2.2 are shown in Figure 2.3. The on-resistance of a

Table 2.2: MOSFET parasitic parameters

Symbol	Description	Units
R_{sp}	On-resistance per unit area	$\Omega \cdot mm^2$
$C_{oss,sp}$	Output capacitance per unit area	F/mm^2
$Q_{g,sp}$	Total gate charge per unit area	C/mm^2
$Q_{sw,sp}$	Switching charge per unit area	C/mm^2



(a) R_{sp} measurement.

(b) Q_g measurement.

(c) C_{oss} measurement.

Figure 2.3: Test circuits for parameter extraction

MOSFET in the linear region is defined by

$$r_{on} = \frac{dv_{ds}}{di_d} \tag{2.1}$$

$$= \frac{1}{k'(W/L)(V_{gs} - V_T)} \tag{2.2}$$

$$\tag{2.3}$$

Thus, to extract the specific on-resistance, the device must be fully turned on and a small V_{DS} has to be applied to keep the device into deep triode. A wider device has a wider channel, thus a lower on-resistance. However, it is more usefull to express the on-resistance of the FET in terms of the area of the device instead of the width. Then, a test device is used to calculate the specific on-resistance as

$$R_{sp} = r_{on}A \tag{2.4}$$

Gate charge, Q_g, and switching charge, Q_{sw}, can be extracted by switching the MOSFET with a clamped load as shown in Figure 2.3b. Then, the charge that flows into the gate is

$$Q_g = \int_0^{t_r} i_g dt \tag{2.5}$$

where t_r is the time it takes for v_{gs} to reach the maximum driving voltage. The gate charge is directly related to the gate-source and gate-drain capacitances, which are the result of the gate overlap to the source and drain contacts. As the width of the MOSFET increases, the overlap area increases, thus increasing the gate charge needed to fully turn on the device when it is switched. Thus,

$$Q_{g,sp} = \frac{Q_g}{W} \tag{2.6}$$

The switching charge Q_{sw} is the charge from $V_{gs} = V_{TH}$ to the end of the plateau V_m as shown in Figure 2.4. The output capacitance C_{oss} is the sum of the gate-drain and drain-source

capacitances

$$C_{oss} = C_{gd} + C_{ds} \tag{2.7}$$

To extract this parameter the circuit of Figure 2.3c can be used. The gate and source are connected to ground and a DC bias plus a small AC signal is applied to the drain terminal. The current flowing into the drain will charge C_{gd} and C_{ds}, resulting in

$$\hat{i} = C_{oss}\frac{d\hat{v}}{dt} \tag{2.8}$$

C_{oss} is dominated by C_{ds}. As shown in Figure 2.5, the drain-source capacitance is the result of the reversed biased junction between the drain doped n^+ region and the p-body of the MOSFET. As a consequence, this capacitance is dependent on the drain-source voltage and can be modeled as

$$C(V) = \frac{C_o}{(1+\frac{V}{\phi_B})^{mj}} \tag{2.9}$$

where C_o is the capacitance at $V = 0$, ϕ_B is the built-in potential and mj is the grading coefficient. Thus, this parameter can not be extracted as a simple value but as a curve as

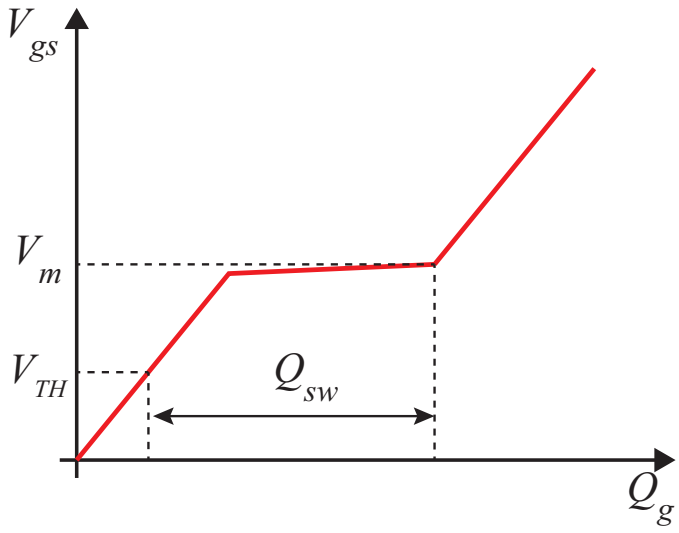


Figure 2.4: Gate charge plot.

a function of the drain voltage. C_{ds} is directly proportional to the MOSFET's width. To extract $C_{oss,sp}$ the curve obtained in Equation 2.9 has to be divided by area of the test device.

Due to the non-linear voltage dependence of C_{oss}, some error will be introduced when using this parasitic element to compute switching losses on power converters as a single value can not be chosen from the curve. In [17], an equivalent linear capacitor that stores the same energy ($C_{eq,E}$) or the same charge ($C_{eq,Q}$) that the non-linear model are calculated as

$$C_{eq,E} = \frac{2}{V_C^2}\int_0^{V_C} vC_x(v)dv \tag{2.10}$$

$$C_{eq,Q} = \frac{1}{V_C}\int_0^{V_C} C_x(v)dv \tag{2.11}$$

using the non-linear capacitance data. This capacitor is not dependent on voltage and can be used to compute switching losses more accurately.

With these parameters expressed in terms of the device size, exploration of power converters topologies over different conditions can be done once the analytical model is constructed.

2.3.2 Fully integrated buck

Converter size is important when designing for portable applications. Magnetics one of the bottle necks for switching converters when size matters. Fully integrated buck converters, where the power stage, control and passives are fabricated in the same die or package, have been implemented in [18, 19, 20, 21, 22] using metal layers in a spiral shape as inductors and

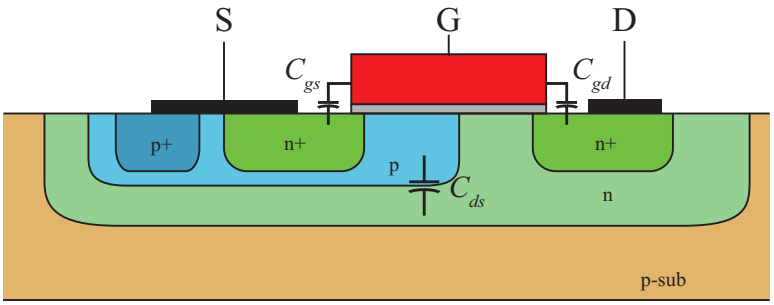
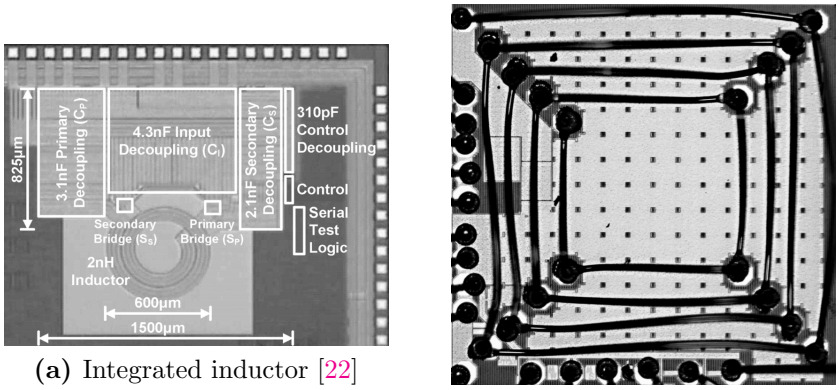


Figure 2.5: Cross section of a LDMOS

integrated capacitors for input decoupling and output filtering. Due to the low inductance value achieved with integrated inductors, high frequency operation is needed in order to reduce both current and output voltage ripple. Also, multi phasing is used to decrease the switching frequency while keeping low ripple. Metal routing layers used to construct integrated inductors are highly resistive (mΩ/square) due to the low thickness, producing DCR up to 250 mΩ/nH [21]. For this reason, high Q inductors are difficult to achieve. Other attempts to include inductors on chip use bond wires. A typical relationship between bond wire length and inductance is 1 nH/mm. In [23, 24] parasitic inductance due to the connection between the switching node on the die and the package is used as the power inductor. In [25] a non-standard packaging bond wire is used to build a spiral inductor on-chip. Different shapes for bond wire inductors are explored in [26] including triangle, square, pentagon, hexagon and octagon. The authors report that triangular geometry can achieve the highest inductance density and the lowest DCR for a given inductance value. All of these works use air core inductors in order to keep using standard processes. Building the inductor in an interposer[1] opens more possibilities. In [27] a coupled inductor that increases the current capability of previous works is implemented achieving output currents of 5 A. However, reported efficiency is 61 % at full load. Modified fabrication processes can include thick copper layers and deposition of magnetic materials. In [28] solenoid inductors are fabricated on chip for a multi phase integrated buck converter. In all cases, achieved inductance values do not exceed 30 nH. Thus, high switching frequency is needed in order to limit current ripple. In addition, reported output currents do not exceed 2 A. In order to increase the output current, switch area must be increased accordingly in order to reduce conduction losses. However, at high frequency operation, increasing the switch size to reduce conduction losses can also increase the total power loss due to switching losses. Moreover, gate driver design for moderate big power switches can be challenging at high frequency due to increased C_{gs}.

[1] interface between the die and the PCB. It is normally used to spread the pitch of the connections in the die.



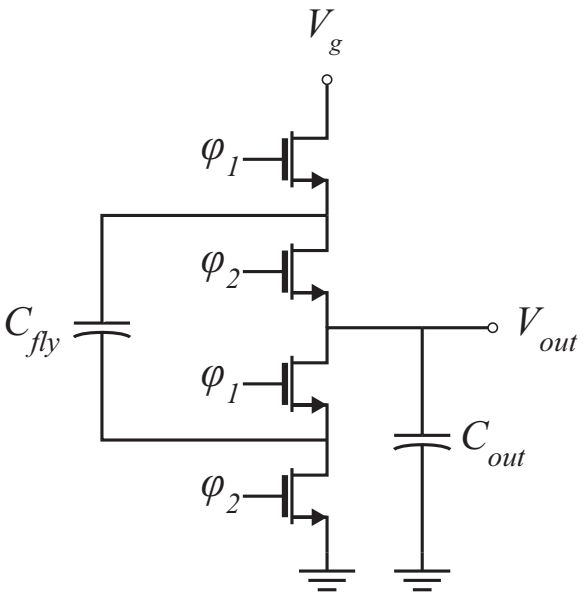
(a) Integrated inductor [22]

(b) Bond wire inductor [25]

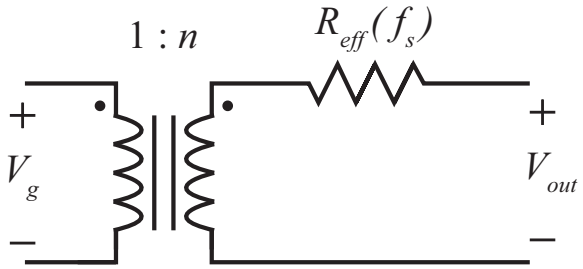
Figure 2.6: Inductors used for fully integrated converters.

2.3.3 Switched capacitors

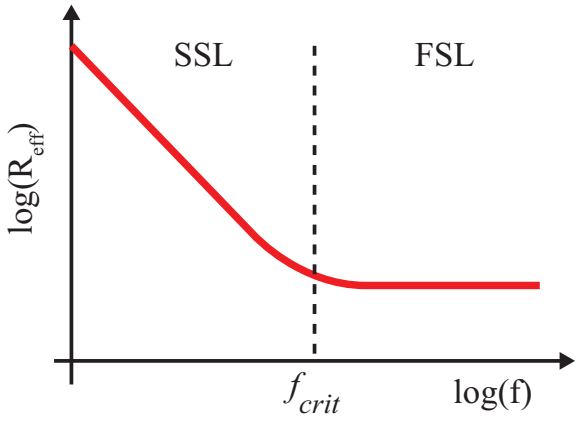
Switched capacitor converters (SCC) don't use inductors as the energy storage element. The power conversion is performed by charging and discharging a capacitor (or a set of capacitors) between the input and the load. In Figure 2.7a a 2 to 1 converter is shown as an example. During the first phase (ϕ_1 high), the flying capacitor is connected in series with the output, while during the second phase (ϕ_2 high) the capacitor is connected in parallel. If timing permits, the steady state voltage on the capacitor is half the input voltage and thus, $V_{out} = 0.5V_{in}$. The conversion ratio of a SCC is fixed defined by the topology. Figure 2.7b shows a general model for SCC where the transformer's turns ratio represents the conversion ratio and the resistor concentrate the losses of the converter [29]. The effective output resistance depends on the topology, the capacitance value and the switching frequency of the converter [15, 30]. Figure 2.7c shows a general output resistance for a SCC which shows two different region of operation: FSL (Fast Switching Limit) and SSL (Slow Switching Limit). At high switching frequencies ($f > f_{crit}$), the output impedance is dominated by the FETs on-resistance and the ESR of the capacitor. In this region, the impedance of the converter is independent of the frequency. For frequencies below f_{crit}, the output impedance is dominated by the charging and discharging of the capacitor. In this region, the impedance can not be reduced by lowering the FETs on-resistance. When two capacitors with different voltages are connected by a series resistance, a charge redistribution occurs. The associated loss for the charge sharing process depends only in the voltage difference and the value of



(a) 2-1 Switched capacitor converter.



(b) Switched capacitor converter model.



(c) Output impedance for a SCC.

Figure 2.7: Switched capacitors converter.

the capacitors. A expression for the resistance in both SSL and FSL are derived in [31],

$$R_{SSL} = \sum_i \frac{(a_{c,i})^2}{C_i f_{sw}} \tag{2.12}$$

$$R_{FSL} = 2\sum_i R_i (a_{r,i})^2 \tag{2.13}$$

Equation 2.13 represents the analytical expression for the output impedance of any SCC. In this equation $a_{c,i}$ is the relationship between the charge flow on the i^{th}-capacitor and the average charge flowing to the output in one period. While $a_{r,i}$ is the analogous for the FETs [31]. In the case of the 2:1 SCC of 2.7a, $a_{c,1} = a_{c,2} = a_{r,1} = a_{r,2} = 1/2$. It must be noted that this model does not include gate losses or C_{oss} losses. In the SSL region, a sort of linear regulation of the output voltage can be performed by modulation of the output resistance [32, 33, 34]. However, as in the case of linear converters, this is not an efficient control method as the difference between the input and the output voltage is dropped in the output resistance. SCCs are more suitable for integration than buck converters. Not only because of the absence of inductors but because device's stress is lower than the input voltage, i.e., the converter shown in Figure 2.7a, each device has to block $V_{in}/2$. As a consequence, lower voltage devices that have lower on-resistance can be used, decreasing on chip losses. As in the case of inductors for the buck converter, capacitor quality plays an important roll in SCC performance. Efficiency and power density is strictly related to the process used to fabricate the IC. Trench capacitors in SOI (Silicon-On-Insulator) technologies can achieve higher efficiencies [35, 36, 37] than standard CMOS processes [38, 39, 40].

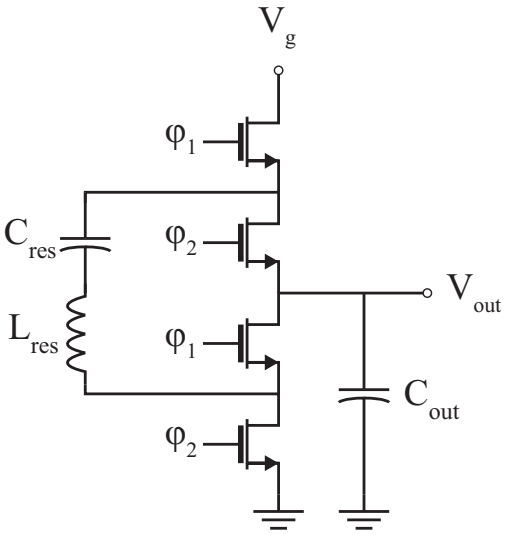
2.3.4 Multi-stage converters

Regulation of the output voltage on SCC is not possible as it only depends on the topology. Several works have presented switched capacitor converters followed by a regulation stage to overcome this drawback. However, cascading stages can increase conduction losses as the current path is shared among stages. In [41], a cascaded converter is implemented using a SCC as a voltage divider followed by a multiphase buck regulator stage. In [42] a SC step down is followed by a buck converter and the control scheme is such that charge sharing

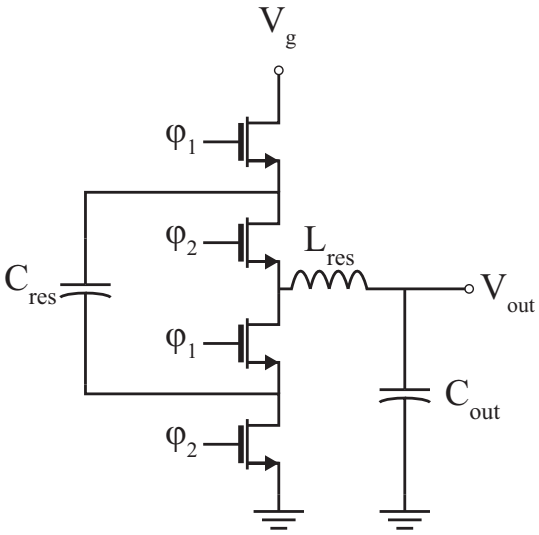
losses on the SC stage are reduced. Efficiency improvements are achieved when comparing with a single stage buck converter due to utilization of lower voltage devices on the last stage. In [43] a hybrid converter with merged voltage divider stage and regulation stage is implemented, achieving lower losses and smaller footprint than cascade converters.

2.3.5 Resonant switched capacitor

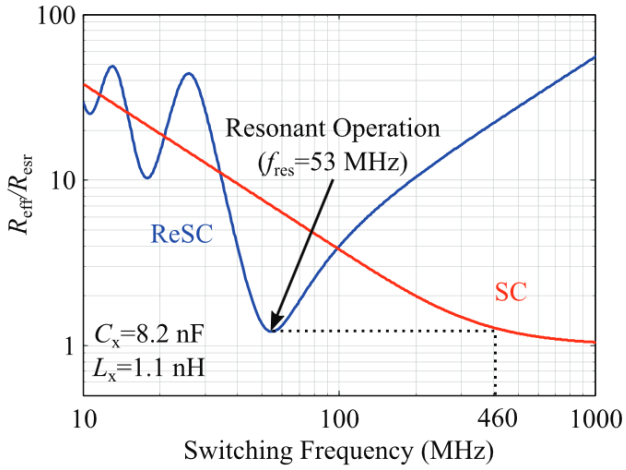
As shown in Figure 2.7c, there are two different regions for R_{eff}. The SSL (Slow Switching limit) region is dominated by the charge sharing losses due to voltage mismatches between capacitors. While the FSL (Fast Switching Limit) is the lower limit for R_{eff}, and is set by the on-resistance of the switches. To operate the converter in the FSL, high frequency operation is needed unless a big capacitor is used. Increasing the switching frequency will impact switching losses and make it difficult to drive large MOSFETs needed to reduce conduction loss, and big capacitance value will impact on the converter's size. Resonant Switched Capacitors Converters (ReSCC) overcome this drawback by placing an inductor in series with the capacitor (Figure 2.8a) [44]. When the converter is operated at its resonant frequency, charge sharing losses that are dominant at SSL are eliminated and a minimum value for the output resistance is achieved (Figure 2.8c). This value is related with the R_{eff} of its equivalent SCC: the impedance is reduced Q times for the same switching frequency, where Q is the quality factor of the tank. Also, to achieve this value on the equivalent SCC the switching frequency has to be Q times larger [15]. Thus a lower output impedance value is achieved while switching frequency is reduced. On the 2-to-1 resonant converter of Figure 2.8a, the inductor current is a pure sinusoid at the resonance frequency (Direct). Its energy is concentrated at a high frequency and can impact on losses of the inductor due to its AC resistance. In [46], the inductor is moved to the output node, producing a rectified sinusoid inductor current (Indirect) with frequency content located at DC and harmonics. By concentrating more power at DC, the ESR of the inductor can be reduced by lowering core losses and skin effect. Regulation of the output voltage can be achieved in the direct topology by duty cycle modulation. Whereas, in the indirect an extra state is added to the converter's operation, where the tank is disconnected from the output, maintaining capacitor's charge balance [45, 47].



(a) 2-1 Indirect Resonant Switched Capacitor converter.



(b) 2-1 Direct Resonant Switched Capacitor converter.



(c) ReSC effective resistance as a function of the frequency [45].

Figure 2.8: Resonant switched capacitor converter.

2.4 Summary

Figure 2.9 shows a graphical summary of the articles reviewed in this chapter. Most of the works related with the topic are concentrated at currents of 1 A with efficiencies below 90 %. Higher current implementations don't achieve high efficiency, which translates heating up the smart phone or tablet while charging at this current level. Our target is to achieve 96 % efficiency at a load current of 10 A, based on doubling the actual maximum charging current while maintaining losses on-chip below 2 W for an output voltage of 4 V.

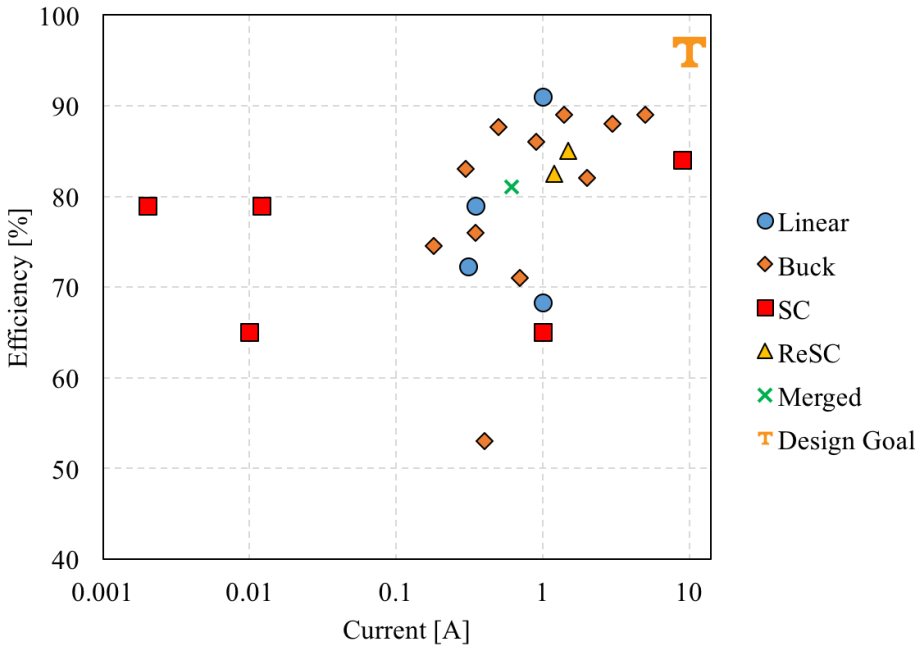


Figure 2.9: Efficiency summary at maximum currents.

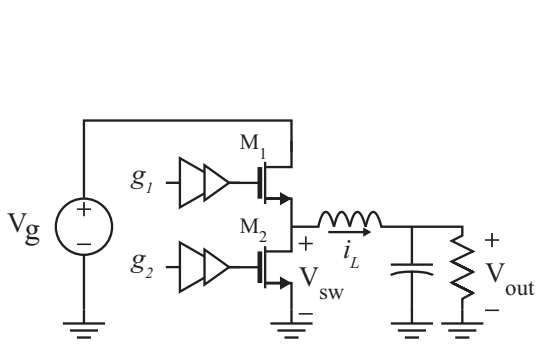
Chapter 3

Topology exploration

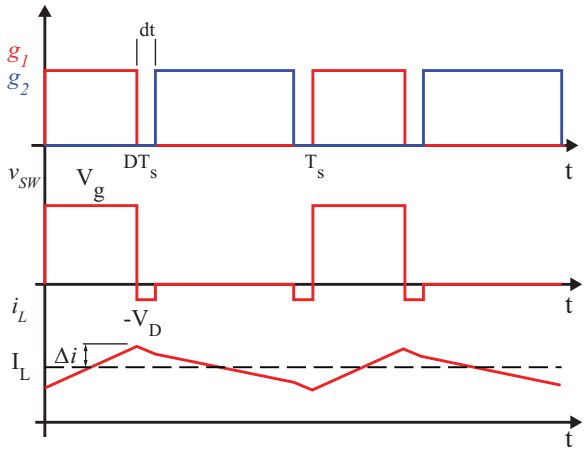
In order to find the best candidate for a low loss power stage, different topologies are explored in this chapter. The process that is used in this work has LDMOS (Laterally Diffused MOSFET) devices available on 7 V, 12 V and 20 V blocking voltage. An LDMOS is an asymetric device designed to achieve low on-resistance and high blocking voltage capability. Thus, this devices are suitable for integrated power converters. For each topology a loss model will be derived analyzing conduction and switching losses. Each loss mechanism is solved in terms of specific parameters (per area) of the devices. Then, in order to find the lower loss topology for different operating points, the input voltage, output current and total FET area are swept to make a comparison.

3.1 Buck

Buck converters are well known in power electronics. As shown in Figure 3.1a, a half bridge is used to generate a square wave at the switching node and a low pass filter composed of an LC network that eliminates the high frequency content. The output voltage is then the average of the switching node. Figure 3.1b shows the key waveforms for the converter.



(a) Buck converter schematic



(b) Key waveforms for buck converter

Figure 3.1: Buck converter.

3.1.1 Loss Model

Conduction Losses

RMS currents through M_1 and M_2 are

$$i_{rms,M1} = \sqrt{D} I_L \sqrt{1 + \frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2} \tag{3.1}$$

$$i_{rms,M2} = \sqrt{1-D} I_L \sqrt{1 + \frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2} \tag{3.2}$$

Thus, conduction losses in terms of the specific on-resistance are

$$P_{cond_1} = D I_L^2 \left(1 + \frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right) \frac{R_{sp}}{A_1} \tag{3.3}$$

$$P_{cond_2} = (1-D) I_L^2 \left(1 + \frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right) \frac{R_{sp}}{A_2} \tag{3.4}$$

During the dead times, the body diode of M_2 conducts the inductor current. This loss mechanism is computed as

$$P_{bd} = 2 V_f I_L t_d f_s \tag{3.5}$$

Switching Losses

During M_1 turn on/off, there is an overlap of current and voltage during the miller plateau. This loss can be modeled as shown in Figure 3.2b. When $v_{gs} = V_{TH}$, the drain current of M_1 starts to increase. However, because of the clamped inductive load, v_{ds} does not change and there is a voltage and current overlap. Then, overlap losses due to M_1 turn on and turn off are

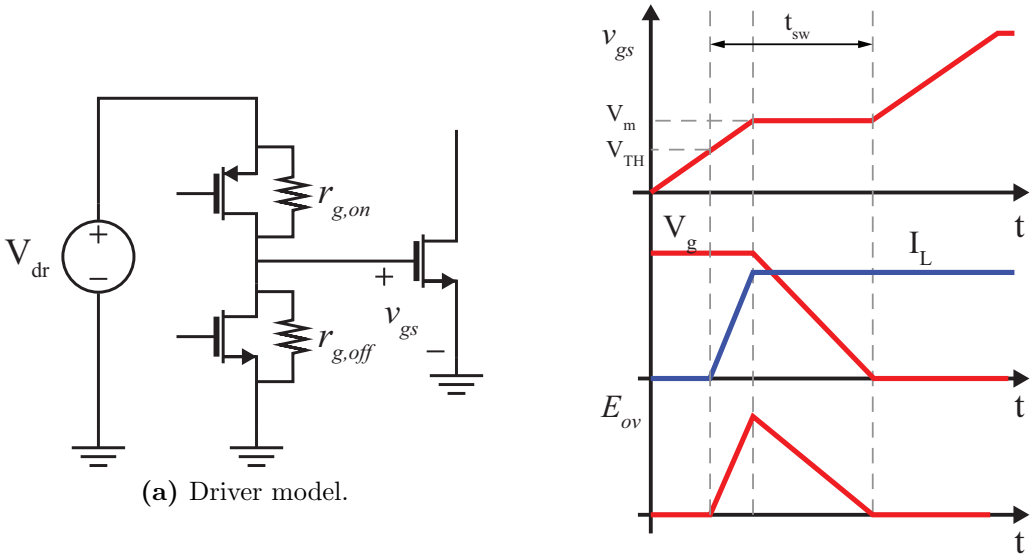
$$P_{overlap} = V_g I_L (t_{sw,on} + t_{sw,off}) f_s \tag{3.6}$$

Equation 3.6 can be rewritten by expressing t_{sw} in terms of the corresponding gate charge and the gate current during turn on/off. Using the model of Figure 3.2a, and assuming that the gate voltage is V_m during the overlap period,

$$P_{overlap} = \frac{1}{2} V_g I_L Q_{sw,sp} A_1 \left(\frac{1}{I_{g,on}} + \frac{1}{I_{g,off}} \right) f_s \tag{3.7}$$

$$I_{g,on} = \frac{V_{dr} - V_m}{R_{g,on}} \tag{3.8}$$

$$I_{g,off} = \frac{V_m}{R_{g,off}} \tag{3.9}$$



(a) Driver model.

(b) Overlap waveforms.

Figure 3.2: Overlap model.

When M_1 turns on, the charge that was stored in $C_{ds,1}$ is lost. However, there is also a loss on $r_{ds,on1}$ due to the charging of $C_{ds,2}$. The circuit of Figure 3.3 models the behaviour. There are two phenomena occurring on r_{ds1} at the same time when M_1 turns on: charging of C_{ds2} to V_g and discharging of C_{ds1}. The energy lost in the resistor can be calculated using equivalent energy and charge capacitances in order to account for the voltage dependence of C_{ds} [17]

$$E_R = \frac{1}{2}C_{eq1,E}V_g^2 + V_g^2 C_{eq2,Q} - \frac{1}{2}C_{eq2,E}V_g^2 \tag{3.10}$$

$$P_{oss} = \frac{1}{2}\left(C_{eq1,E,sp}A_1 + 2C_{eq2,Q,sp}A_2 - C_{eq2,E,sp}A_2\right)V_g^2 f_s \tag{3.11}$$

Gate charge is also lost when each device switches and is calculated as

$$P_{gate} = V_{dr}Q_{g,sp}(A_1 + A_2)f_s \tag{3.12}$$

Table 4.1 summarizes the loss model for a buck converter. In this loss model reverse recovery of the body diode of M_2 is neglected as for this specific process, Q_{rr} losses do not impact significantly on the performance of the converter if the dead time is short.

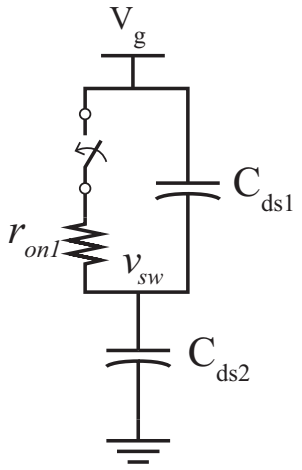


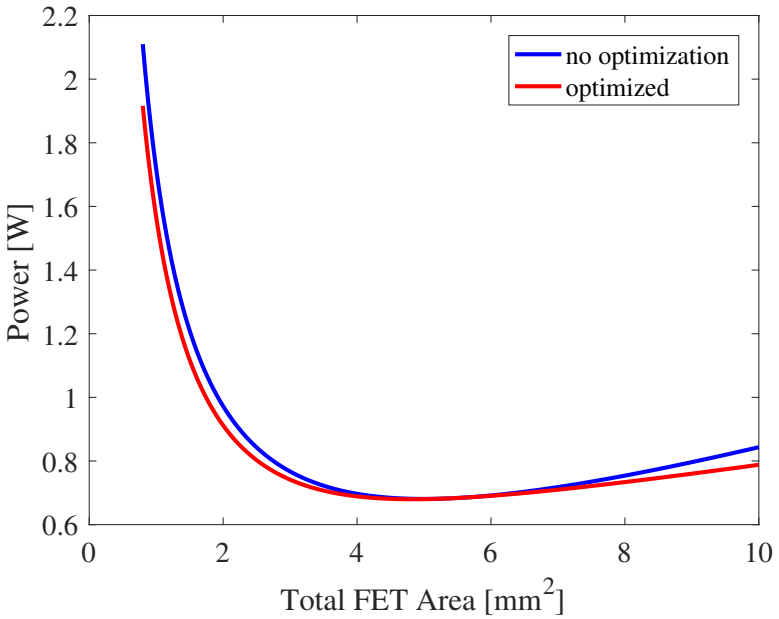
Figure 3.3: Model to calculate C_{oss} losses.

3.1.2 Design space

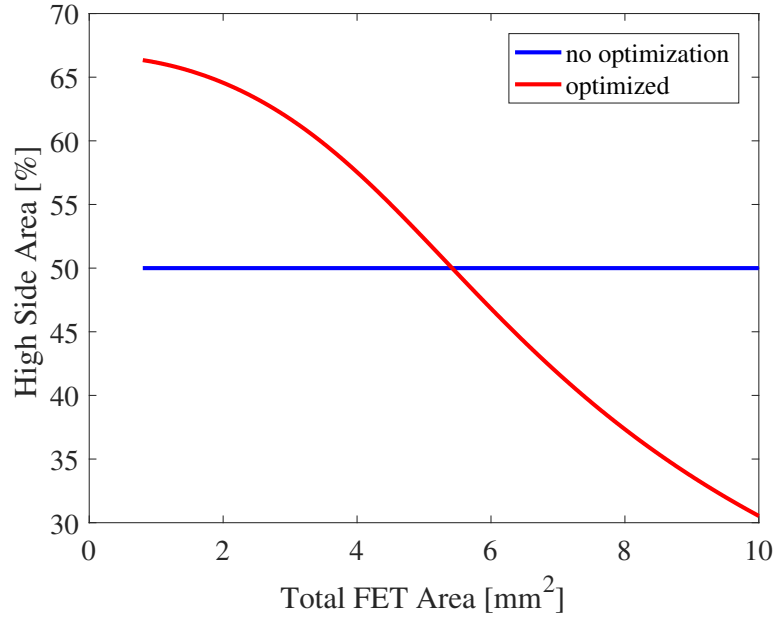
Depending on the input voltage, one of the devices will suffer more conduction losses than the other. For low conversion ratios ($D < 0.5$), M_2 will remain on more time than M_1. Then, $I_{rms,M2} > I_{rms,M1}$. If the area of the power stage is evenly distribute, $P_{cond2} > P_{cond1}$. An optimization can be made by sizing the switches properly by equating their losses. Figure 3.4, where the total FET area A ($A_1 + A_2$) is swept for a 5 V input - 4 V output buck converter at $I_{out} = 10$ A. At low areas, conduction loss dominates. As a consequence, in order to have equal losses on the FETs, M_1 area needs to be larger than M_2 (Figure 3.4b). On the other hand, at large areas, switching losses dominate and M_1 area has to be smaller than M_2.
In a buck converter, both devices must block the input voltage. In addition, ringing at the switching node occurs when M_1 turns on, increasing voltage stress on the devices. As a consequence, devices must be chosen with a safety margin. Any device must be used for an input voltage lower than $kV_{ds,max}$, where $k < 1$. Unless otherwise is stated, it will be adopted $k = 0.7$. Figure 3.5 shows the loss map over input voltage range from 5 V to 12 V with switch area optimization and over the total FET area. For each input voltage, the device is selected accordingly. For $I_{out} = 10$ A, 2 W of losses are achieved at a minimum area of 0.8 mm^2. As the input voltage increases, the change of LDMOS pushes the minimum area to 1.1 mm^2. Due to the switching node overshoot, 7 V devices can not be used.

Table 3.1: On-chip Loss model for a Buck converter

Loss Mechanism	Symbol	Model
M_1 Conduction Loss	P_{cond1}	$I_L^2 D\left(1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)\frac{R_{sp}}{A_1}$
M_2 Conduction Loss	P_{cond2}	$I_L^2 (1-D)\left(1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)\frac{R_{sp}}{A_2}$
Body Diode Loss	P_{bd}	$2V_f I_L t_d f_s$
Overlap Loss	P_{ov}	$\frac{1}{2}V_g I_L Q_{sw,sp} A_1 \left(\frac{1}{I_{g,on}}+\frac{1}{I_{g,off}}\right) f_s$
C_{oss} Loss	P_{oss}	$\frac{1}{2}\left(C_{eq1,E,sp}A_1 + 2C_{eq2,Q,sp}A_2 - C_{eq2,E,sp}A_2\right) V_g^2 fs$
Gate Loss	P_{gate}	$V_{dr} Q_{g,sp}(A_1 + A_2) f_s$

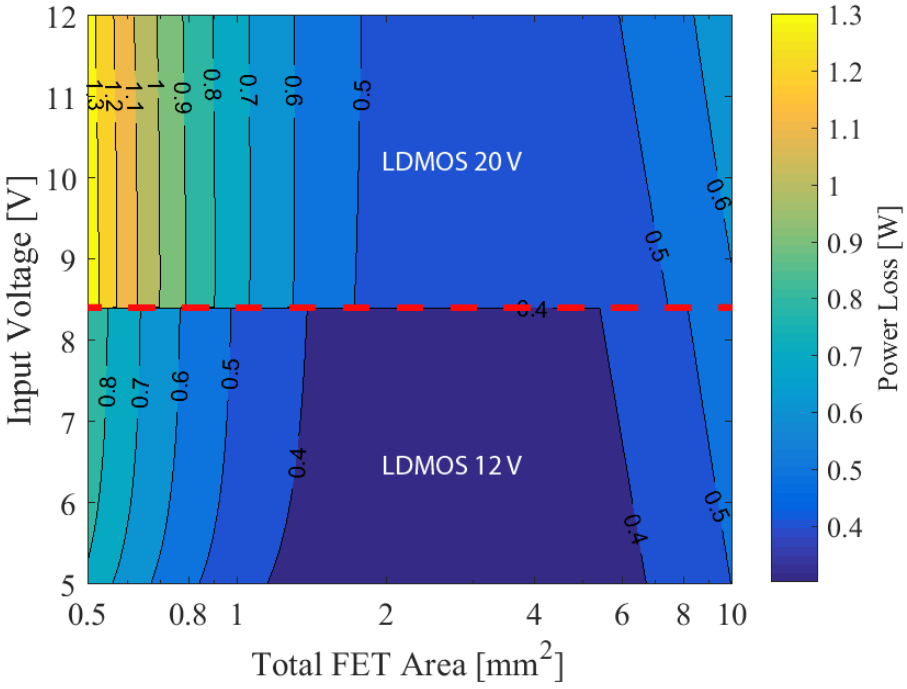


(a) Converter loss comparison with and without optimization of the FETs areas.

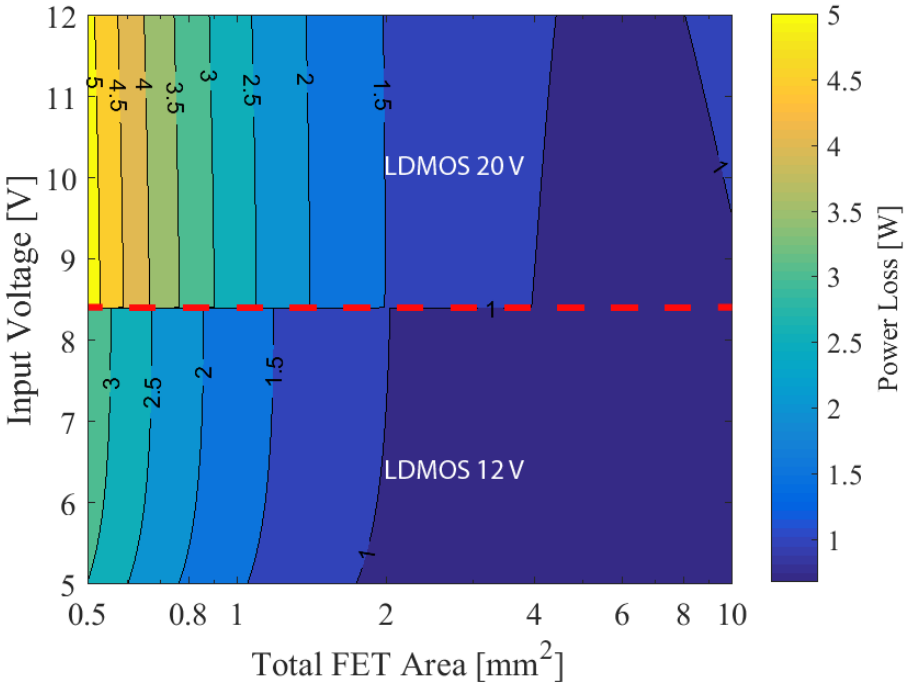


(b) Optimized high side area as a function of the total power switch area.

Figure 3.4: Area optimization for a buck converter.



(a) I_{out} =5 A



(b) I_{out} =10 A

Figure 3.5: Loss map with device size optimization for different load currents for a Buck converter.

The use of lower blocking voltage device reduce the losses R_{sp} is lower. This overshoot is produced by the fast turn on of M_1 which creates a high di/dt on the power loop inductance. This parasitic element is created by PCB traces and packaging connections. A decoupling capacitor must be placed as close as possible to the power stage in order to minimize the power loop as shown in Figure 3.6 Proper layout techniques can help to further reduce the power loop inductance as presented in [48]. However, some inductance is still remaining between the decoupling capacitor and the power stage that can't be mitigated by these methods. Bond wires contribute significant amount of inductance (canceling the effect of the decoupling capacitor) as was shown in [23, 24, 25]. Placing a capacitor between the bond wires and the power stage can move the parasitic inductance out of the power loop as shown in Figure 3.7 Capacitance density for integrated capacitors depends on the process. In a standard process, it is difficult to achieve capacitance values beyond 1 nF while leaving room for other circuits. SOI (Silicon on Insulator), trench capacitors that are the most area efficient capacitors, suffer from high ESR [49]. System in package (SiP) solutions for DCDC converters, where switches and control circuitry are integrated on different dies and attached on the same substrate, allow the chance to include the decoupling capacitor in the same package as shown in Figure 3.8, minimizing the power loop inductance. However, this solution increases the cost of the final product as three different IC have to be fabricated. However, if the size of a single IC containing the power stage and the control circuitry is

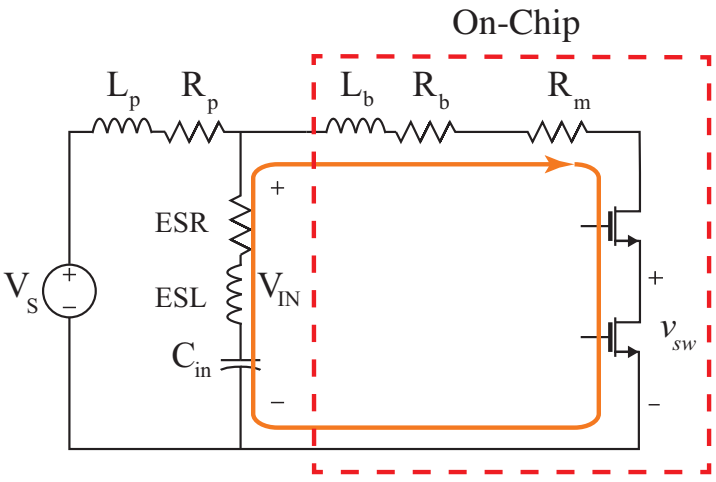


Figure 3.6: Equivalent circuit showing elements involved in the power loop

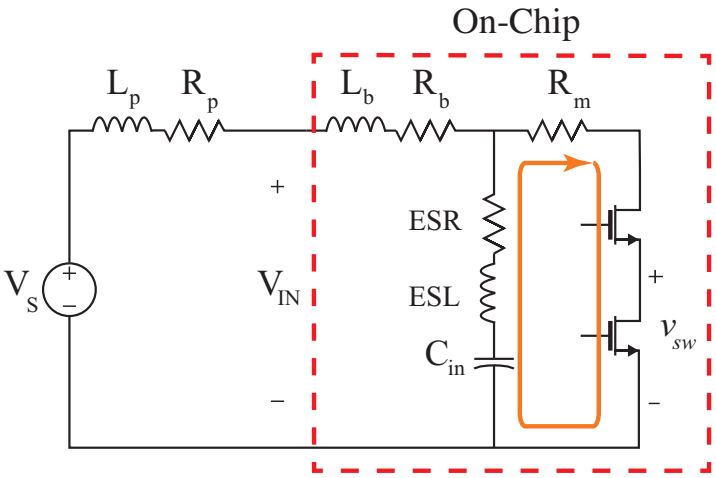


Figure 3.7: Bond wire inductance mitigation

large enough, 0201 or 0402 pads can be placed on the top metal layer to solder a discrete capacitor.In order to prevent the switching current to circulate through the bond wires, the impedance of the power loop of Figure 3.7 must be smaller than the outer loop of Figure 3.6. Both impedances can be modeled as:

$$Z_{off-chip} = \frac{1}{sC_{in}} + s(L_b + ESL) + (R_b + R_m + ESR) \tag{3.13}$$

$$Z_{on-chip} = \frac{1}{sC_{in}} + sESL + (R_m + ESR) \tag{3.14}$$

With these equations we can compare the three different approaches described so far. In Figure 3.9, an off-chip power loop with a 2 µF ceramic capacitor, an on-chip power loop with a 10 nF integrated capacitor and finally a SiP with a 2 µF ceramic capacitor. Typical values for ESR and ESL for the ceramic capacitor are taken from commercial parts and 5 Ω/square is used for the integrated capacitor, which is a typical value for a silicide poly. It can be seen how integrated capacitors will have a small effect on mitigating the switch node overshoot as they present a higher power loop impedance than using an off-chip capacitor for the same purpose over some range of frequencies. Thus, ringing due to the parasitic inductance of bond wires will still be present. However, if a SiP solution can be implemented with proper layout of the power stage, overshoot can be minimized. Then, the safety factor can be increased and for the same power stage area, lower losses can be achieved.

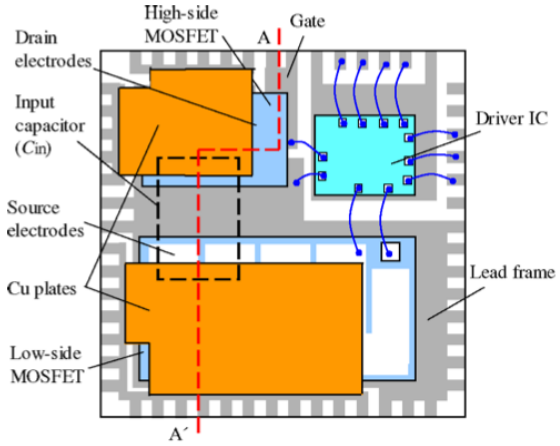


Figure 3.8: System-in-Package solution for minimizing the power loop inductance[50]

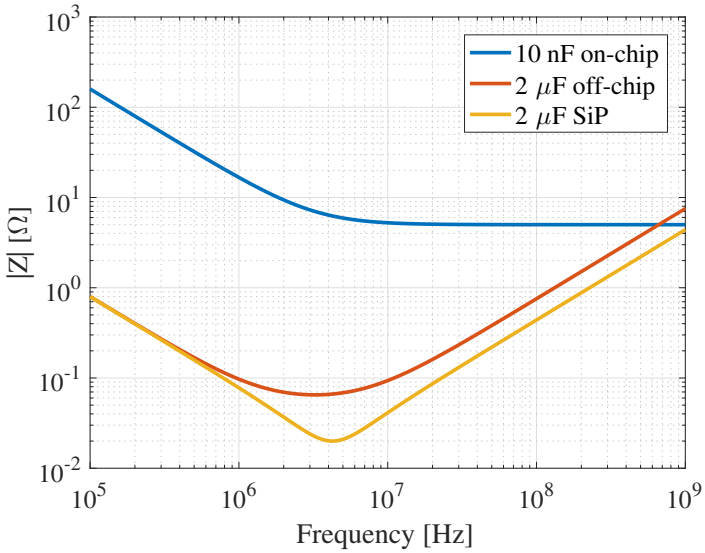
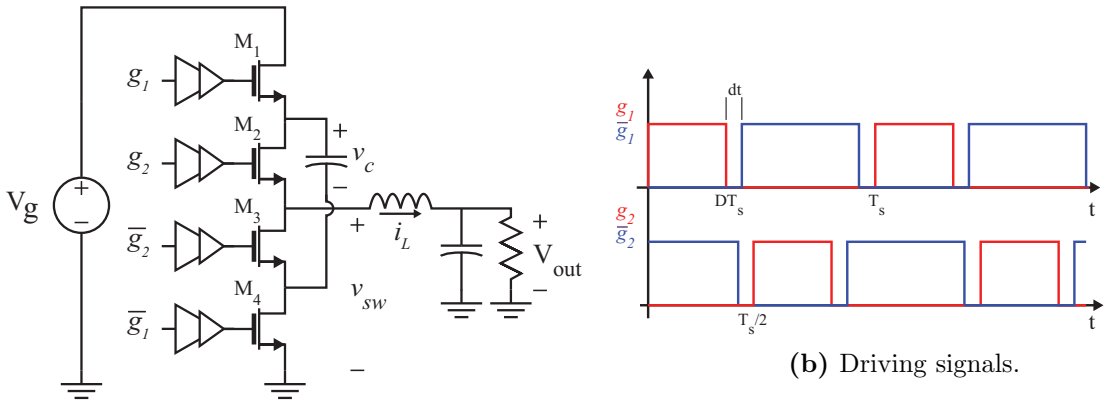


Figure 3.9: Power loop impedance comparison.

3.2 3-Level Buck

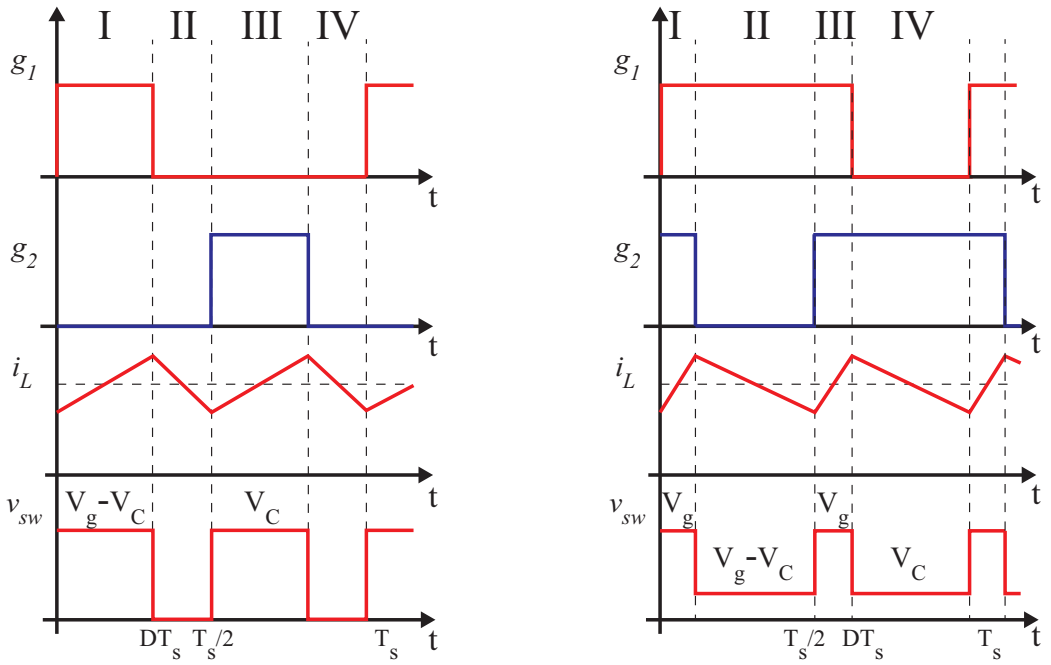
In order to achieve low losses at high currents, device area has to increase to reduce conduction loss that dominates at 10 A as shown in Figure 3.5. However, as switch's size increase, switching losses start to rise and there is a point where buck converter's performance becomes dominated by switching losses. The 3-Level Buck converter can potentially overcome this problem by reducing the switching frequency while keeping the same inductor current ripple. In addition, each FET has to block half the input voltage. Thus, lower voltage devices with lower R_{sp} can be used. Figure 3.10a shows the schematic of this converter. Switches $M_1 - M_3$ and $M_2 - M_4$ are driven with complementary signals and a phase shift of $T_s/2$ as shown in Figure 3.10b. As a consequence of this phase shift two different scenarios must be analyzed depending on the duty cycle. When D is less than 0.5, gate signals g_1 and g_2 do not overlap and the converter's operation is shown in Figure 3.11a. During interval I, M_1 and M_3 are on, connecting the flying capacitor in series with the input voltage. On interval II and VI M_3 and M_4 are on connecting the inductor to ground, and finally during interval III M_2 and M_4 connect the flying capacitor to the inductor and ground. For duty cycles greater than 0.5, there is an overlap of g_1 and g_2 as shown in Figure 3.11b. During interval I and II, M_1 and M_2 connect the inductor to the input voltage. On interval II, M_1 and M_3 connect the capacitor in series with the input voltage and the inductor. Finally, during interval IV, the flying capacitor is connected to ground by M_4 and to the inductor by M_2. As intervals I-III and II-IV have the same duration, $V_C = V_g/2$ to meet volt-sec balance



(a) Schematic.

(b) Driving signals.

Figure 3.10: 3-Level Buck converter.



(a) $D < 0.5$ **(b)** $D > 0.5$.

Figure 3.11: 3-Level Buck converter waveforms over duty cycle.

on the inductor. The same condition must be met if D >0.5. Thus, conversion ratio for the 3-Level Buck is the same as for the buck converter,

$$\frac{V}{V_g} = D \tag{3.15}$$

The applied voltage at the inductor is reduced, and as a consequence, current ripple is

$$\Delta i_L = \begin{cases} \frac{V_g(0.5-D)D}{2Lf_s} & D < 0.5 \\ \frac{V_g(0.5-D)(1-D)}{2Lf_s} & D > 0.5 \end{cases}$$

When operated at the same switching frequency, the 3-Level Buck has less current ripple than the Buck for the same inductance and conversion ratio. Thus, to achieve the same output characteristic, it can work at a smaller frequency, decreasing switching losses. In addition, due to the voltage on the flying capacitor, each switch has to block half the input voltage. This will not only reduce C_{oss} losses, but also lower voltage devices with lower R_{sp}

can be used, potentially compensating the fact that there are always two switches in series conducting current.

3.2.1 Loss model

Conduction losses

RMS current for $M_{1,2}$ and $M_{3,4}$ are the same as for the buck converter. Thus, conduction losses for this converter are

$$P_{cond_1} = DI_L^2\left(1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)\frac{R_{sp}}{A_1} \tag{3.16}$$

$$P_{cond_2} = DI_L^2\left(1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)\frac{R_{sp}}{A_2} \tag{3.17}$$

$$P_{cond_3} = (1-D)I_L^2\left(1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)\frac{R_{sp}}{A_3} \tag{3.18}$$

$$P_{cond_4} = (1-D)I_L^2\left(1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)\frac{R_{sp}}{A_4} \tag{3.19}$$

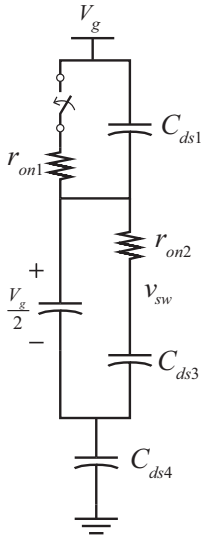
$$\tag{3.20}$$

Body diode conduction occurs through M_3 and M_4 during dead times,

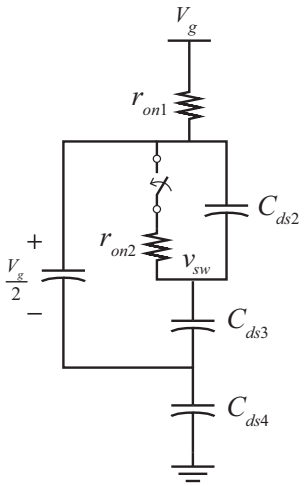
$$P_{bd} = 4V_f I_L t_d f_s \tag{3.21}$$

Switching losses

C_{oss} losses are calculated using the same approach in Section 3.1.1. When $M_{1,2}$ turn on, the same model of Figure 3.3 can be used with $V_g/2$ instead of V_g. Figure 3.12 shows the equivalent circuit models for a 3-Level Buck. For any switching action, there is always one switch that remains on while the other two are off. However, v_{ds} for one of these is clamped



(a) Equivalent circuit for M_1 turn on for $D > 0.5$.



(b) Equivalent circuit for M_2 turn on for $D > 0.5$.

Figure 3.12: C_{oss} circuit model for 3-Level Buck.

by the flying capacitor to $V_g/2$. Thus, C_{oss} losses can be computed as

$$P_{oss_1} = \frac{1}{2}\left(C_{eq1,E,sp}A_1 + 2C_{eq4,Q,sp}A_4 - C_{eq4,E,sp}A_4\right)\left(\frac{V_g}{2}\right)^2 fs \tag{3.22}$$

$$P_{oss_2} = \frac{1}{2}\left(C_{eq2,E,sp}A_2 + 2C_{eq3,Q,sp}A_3 - C_{eq3,E,sp}A_3\right)\left(\frac{V_g}{2}\right)^2 fs \tag{3.23}$$

Turn on and turn off losses occur on M_1 and M_2 also and can be modeled as

$$P_{overlap_1} = \frac{1}{4}V_g I_L Q_{sw,sp}A_1\left(\frac{1}{I_{g,on}} + \frac{1}{I_{g,off}}\right) f_s \tag{3.24}$$

$$P_{overlap_2} = \frac{1}{4}V_g I_L Q_{sw,sp}A_2\left(\frac{1}{I_{g,on}} + \frac{1}{I_{g,off}}\right) f_s \tag{3.25}$$

$$\tag{3.26}$$

assuming that M_1 and M_2 are driven with the same gate driver. Finally, gate losses are

$$P_{gate} = V_{dr}Q_{g,sp}(A_1 + A_2 + A_3 + A_4)f_s \tag{3.27}$$

To summarize the loss model for a 3-Level Buck, Table 3.2 presents the individual loss equations.

Table 3.2: On-chip Loss model for a 3-Level Buck converter

Loss Mechanism	Symbol	Model
M_1 Conduction Loss	P_{cond_1}	$I_L^2 D\left(1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)\frac{R_{sp}}{A_1}$
M_2 Conduction Loss	P_{cond_2}	$I_L^2 D\left(1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)\frac{R_{sp}}{A_2}$
M_3 Conduction Loss	P_{cond_3}	$I_L^2 (1-D)\left(1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)\frac{R_{sp}}{A_3}$
M_4 Conduction Loss	P_{cond_4}	$I_L^2 (1-D)\left(1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2\right)\frac{R_{sp}}{A_4}$
Body Diode Loss	P_{bd}	$4V_f I_L t_d f_s$
Overlap Loss	P_{ov}	$\frac{1}{4}V_g I_L Q_{sw,sp}(A_1+A_2)\left(\frac{1}{I_{g,on}}+\frac{1}{I_{g,off}}\right)f_s$
C_{oss_1} Loss	P_{oss}	$\frac{1}{2}\left(C_{eq1,E,sp}A_1+2C_{eq2,Q,sp}A_4-C_{eq2,E,sp}A_4\right)\left(\frac{V_g}{2}\right)^2 fs$
C_{oss_2} Loss	P_{oss}	$\frac{1}{2}\left(C_{eq2,E,sp}A_2+2C_{eq3,Q,sp}A_3-C_{eq3,E,sp}A_3\right)\left(\frac{V_g}{2}\right)^2 fs$
Gate Losses	P_{gate}	$V_{dr}Q_{g,sp}(A_1+A_2+A_3+A_4)f_s$

3.2.2 Design space

As the flying capacitor is charged to $V_g/2$, each device blocks half the input voltage. This will benefit the converter's performance as lower voltage devices with lower R_{sp} can be used for higher input voltages. In addition, current ripple is reduced when compared to the buck converter as shown in Figure 3.13 using same switching frequency and inductance. Lower ripple can still be achieved over the entire duty cycle even if the switching frequency or the inductance value is reduced. The former will impact core losses and on-chip losses, while the latter will only affect inductor size. A reduction of switching losses is desirable in high current integrated converters as switches tend to be wide for conduction loss minimization, making switching losses comparable in magnitude.

The same optimization process on Section 3.1.2 is applied to the 3-Level Buck converter. Looking at the waveforms of Figure 3.11, it can be seen that both M_1 and M_2 conduct the inductor current for DT_s while M_3 and M_4 do it for $(1-D)T_s$. As a consequence, the optimization is performed by sizing M_1-M_2 and M_3-M_4 together. Figure 3.14 shows the loss map for a 3-Level buck at 500 kHz over the input voltage and total power switch area. As in the case of the buck converter, device selection is based on the input voltage with a safety

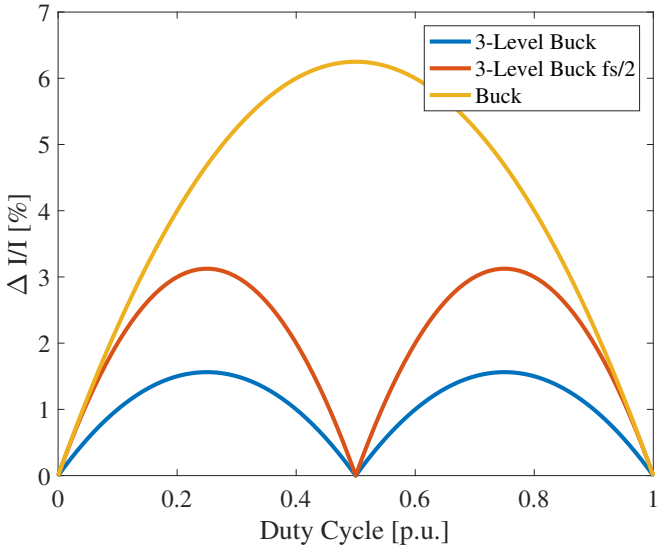
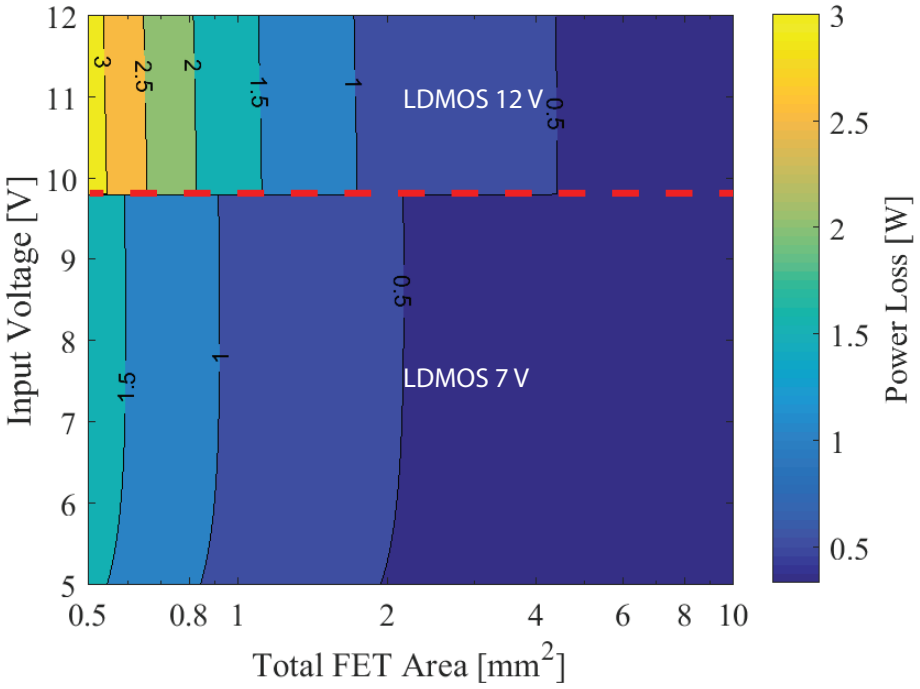
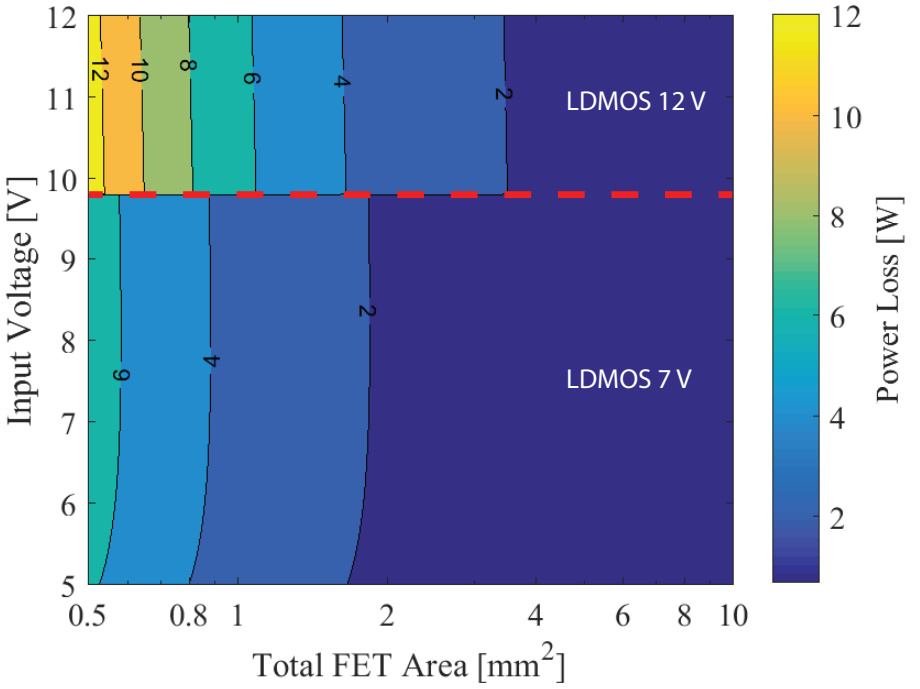


Figure 3.13: Current ripple as a function of the duty cycle for a Buck and a 3-Level Buck converter. I_L =10 A



(a) I_{out} =5 A



(b) I_{out} =10 A

Figure 3.14: Loss map with device size optimization for different load currents for a 3-Level Buck.

margin for switching node overshoot. Due to the fact that two devices are conducting in series on the 4 intervals, losses are higher for small areas.

3.3 Hybrid Buck

The buck converter is the most simple implementation of a switched DCDC converter. There is only one switch conducting per phase keeping conduction loss to a practical minimum. However, as each device has to block the input voltage, device selection has to go along with input voltage range. As the input voltage increases, higher voltage devices need to be used that have higher R_{sp}. In the 3-Level buck, this drawback is mitigated with the flying capacitor, reducing the voltage stress on each device to $0.5V_g$ but two devices conduct in series. The hybrid buck converter presented in this section has only one switch conducting the inductor current while the blocking voltage of each MOSFET is rated for the output voltage. In addition, the inductor is moved back to the input port, reducing conduction loss.

3.3.1 Operation

The Hybrid Buck converter schematic is shown in Figure 3.15. M_1 and M_3 are driven together for DT_s and M_2 for $(1-D)T_s$. The operation of this converter can be analyzed by two intervals.

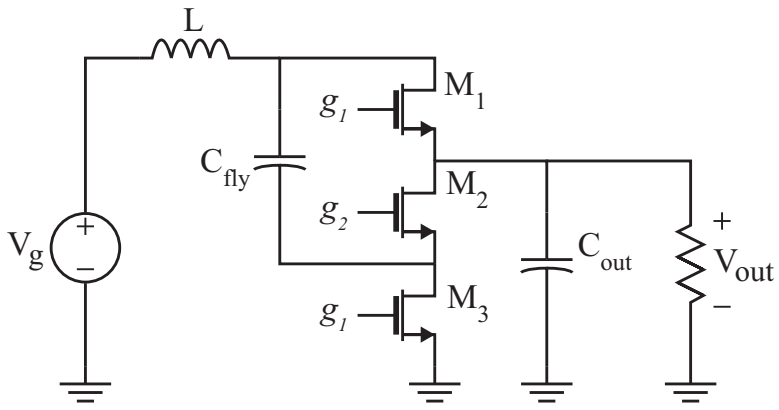


Figure 3.15: Hybrid buck converter schematic

Interval I - $0 < t < DT_s$

During the first interval, M_1 and M_3 are turn on simultaneously for DT_s. The inductor is connected to the output while the flying capacitor is grounded. The equivalent circuit for this interval is shown in Figure 3.16a. Solving for the voltages on the capacitors and the current on the inductor,

$$v_{C_{fly}} = v_{out} \tag{3.28}$$

$$L\frac{di_L}{dt} = V_g - v_{out} \tag{3.29}$$

$$(C_{fly} + C_{out})\frac{dv_{out}}{dt} = i_L - i_{out} \tag{3.30}$$

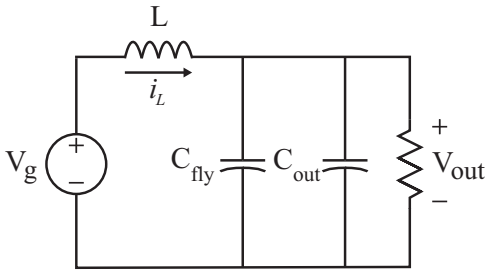
Interval II - $DT_s < t < T_s$

During phase II, switch M_2 is turned on and M_1 and M_3 are off. As shown in Figure 3.16b the flying capacitor is connected in series between the inductor and the output. Solving for the capacitor voltages and inductor current,

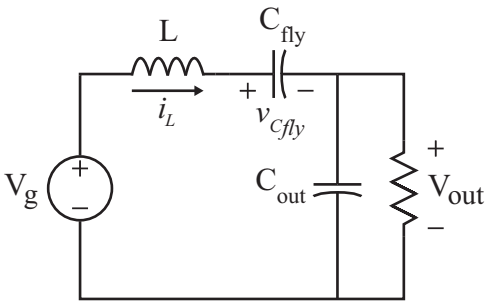
$$C_{fly}\frac{dv_{C_{fly}}}{dt} = i_L \tag{3.31}$$

$$L\frac{di_L}{dt} = V_g - v_{C_{fly}} - v_{out} \tag{3.32}$$

$$C_{out}\frac{dv_{out}}{dt} = i_L - i_{out} \tag{3.33}$$



(a) Phase I equivalent circuit for the hybrid buck converter



(b) Phase II equivalent circuit for the hybrid buck converter

Figure 3.16: Equivalent circuits for Hybrid Buck converter intervals.

For now, it will be assumed that capacitor C_{fly} is big and its voltage is held constant for the entire period and small ripple approximation is applied on the inductor. Thus, the conversion ratio of the hybrid buck converter can be found by

$$0 = (V_g - V_{out})D + (1-D)(V_g - 2V_{out}) \Rightarrow M(D) = \frac{V_{out}}{V_g} = \frac{1}{2-D} \tag{3.34}$$

Figure 3.17 shows the conversion ratio range of the hybrid buck converter. The hybrid buck converter can generate outputs that range from $0.5V_{in}$ to V_{in}. For the scope of this work, this is not critical as it can work at USB 5 V. In addition, high-end smart phones and tablets communicate with the wall charger to specify the required input voltage in order to work on the best efficiency point from an input voltage perspective [51]. As in the case of a boost converter, the input current is found by balancing the input and the output power.

$$V_g I_L = V_{out} I_{out} \Rightarrow I_L = \frac{I_{out}}{2-D} \tag{3.35}$$

And the inductor current ripple can be calculated using the equivalent circuit of Interval I

$$\Delta i_L = \frac{V_g D(1-M(D))}{2Lf_s} \tag{3.36}$$

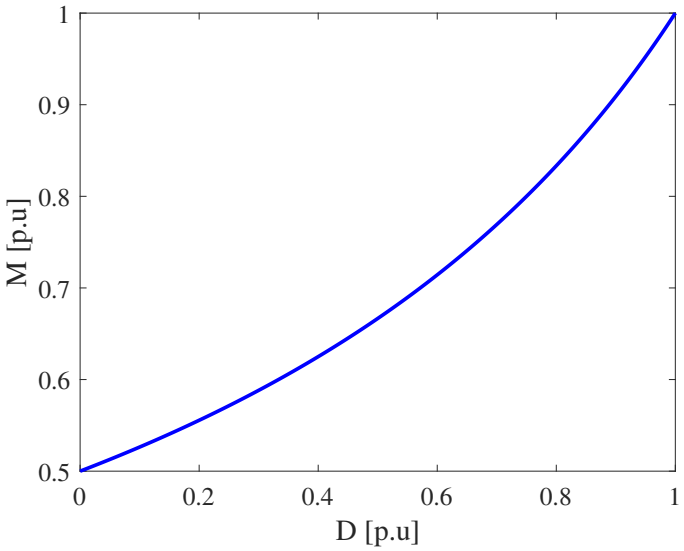


Figure 3.17: Conversion ratio for the Hybrid Buck converter

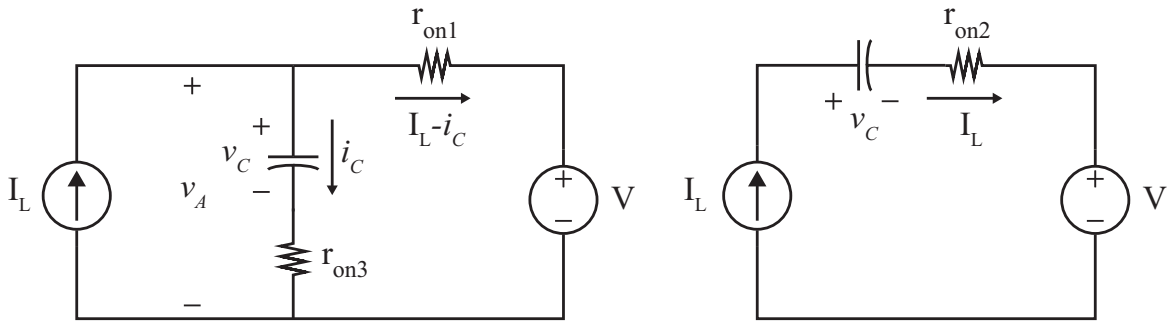
Thus, the inductor current is less than the output current. This is a major improvement over the buck and the 3-Level Buck converters. Although it does not affect on-chip losses, it impacts on the overall thermal dissipation. For an inductor with a 10 mΩ DCR, the power loss at 10 A will be 1 W on both Buck and 3-Level Buck converters. However, for the Hybrid Buck converter the power loss for the same inductor at the same output current will be 0.44 W, a 60 % loss reduction.

3.3.2 C_{fly} ripple effect

For the conversion ratio and inductor current expressions, it was assumed that the voltage on the flying capacitor C_{fly} was constant and equal to V_{out}. However, on Interval II, the capacitor is in series with the output. The inductor current flowing into C_{fly} will increase its voltage by

$$\Delta v_{fly} = \frac{I_L}{C_{fly}}(1-D)T_s \tag{3.37}$$

To examine the effect of the flying capacitor ripple, both intervals are analyzed using equivalent linear circuits (Figure 3.18) assuming small ripple on the inductor and on the output capacitor and including the on-resistances of the MOSFETS. By doing this, the inductor and the flying capacitor are replaced by DC current and voltage sources respectively. At the beginning of Interval I, the initial voltage on the flying capacitor is V_1. Then, $v_A(t)$



(a) Interval I equivalent circuit **(b)** Interval II equivalent circuit

Figure 3.18: Equivalent linear circuits used to analyze the effect of ripple on C_{fly}

can be written as

$$v_A(t) = V + (I_L - i_C(t))r_{on1} \tag{3.38}$$

$$v_A(t) = V_1 + \frac{1}{C}\int i_C dt + i_C r_{on3} \tag{3.39}$$

$$\tag{3.40}$$

Combining these equations, and transforming to Laplace's domain,

$$\frac{V}{s} + \left(\frac{I_L}{s} - I_C(s)\right) r_{on1} = \frac{V_1}{s} + I_C(s)\left(\frac{1}{sC} + r_{on3}\right) \tag{3.41}$$

Solving for $I_C(s)$

$$I_C(s) = \frac{\Delta V}{R_T}\frac{1}{s + \frac{1}{R_T C}} \Rightarrow i_C(t) = \frac{\Delta V}{R_T} e^{-\frac{t}{R_T C}} \tag{3.42}$$

$$\text{where } \Delta V = V + I_L r_{on1} - V_1 \tag{3.43}$$

$$R_T = r_{on1} + r_{on3} \tag{3.44}$$

As shown by Equation 3.42, there is a charge sharing phenomena during Interval I due to the difference between the initial voltage on the flying capacitor and the applied voltage when M_1 and M_3 turn on. To calculate V_1 and V_2, the voltages on C_{fly} at the end of Interval II and Interval I respectively the expression of $v_C(t)$ at the end of the intervals must be used.

$$\text{At the end of Interval I} \rightarrow V_2 = \frac{1}{C}\int_0^{DT_s} \frac{\Delta V}{R_T} e^{-\frac{t}{R_T C}} dt + V_1 \tag{3.45}$$

$$\text{At the end of Interval II} \rightarrow V_1 = \frac{I_L}{C}(1-D)T_s + V_2 \tag{3.46}$$

Plugging Equation 3.45 into Equation 3.46

$$V_2 = \left(V + I_L r_{on1} - \frac{I_L}{C}(1-D)T_s\right) + \frac{\frac{I_L}{C}(1-D)T_s}{1 - e^{-\frac{DT_s}{R_T C}}} \tag{3.47}$$

To corroborate these results a comparison between the equations and a SPICE simulation is performed. Figure 3.19 shows the flying capacitor voltage and current over a period of

operation. The mismatch in the flying capacitor voltage it is due to the output voltage difference between the model and simulation results. In simulation, the duty cycle is set by Equation 3.34. However, due to losses the output voltage is lower. Whereas in the model, the output voltage is set to the ideal case with no loss. Then, it is used to calculate the inductor current as shown in Equation 3.35, creating a different Δv_C during Interval II. However, there is less than 5 % difference and, as it is shown in further sections, there is no effect on the loss modeling while keeping the model simple.

3.3.3 Device stresses

The flying capacitor has a mean voltage close to the output voltage. During Interval I, M_2 is clamped by C_{fly} to V_{out}. M_1 conducts $I_L - i_c$. However, as cab be seen in Figure 3.19b, the capacitor current is negative, meaning that this current flows out of the flying capacitor. Then, both inductor current and capacitor current flow through M_1. The maximum current on these devices can be expressed as

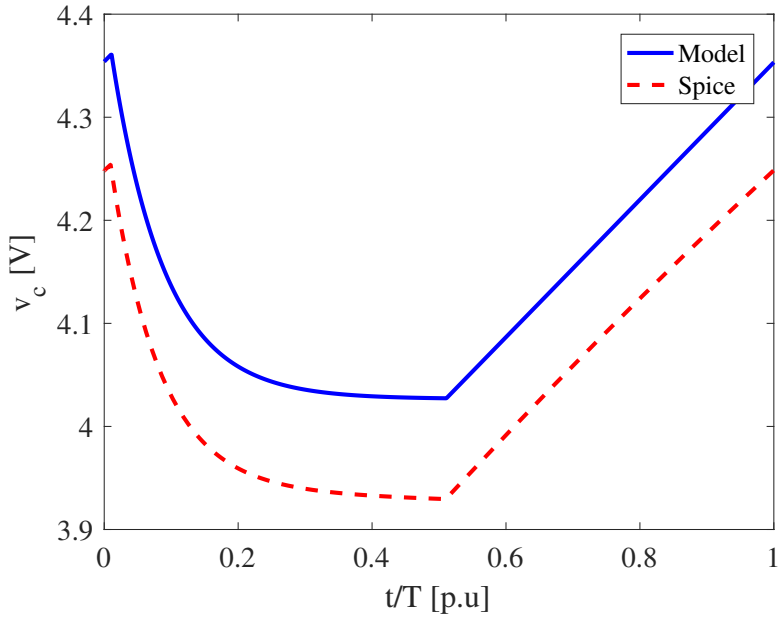
$$I_{M1,max} = I_L + \frac{\Delta V}{R_T} \tag{3.48}$$

$$I_{M3,max} = \frac{\Delta V}{R_T} \tag{3.49}$$

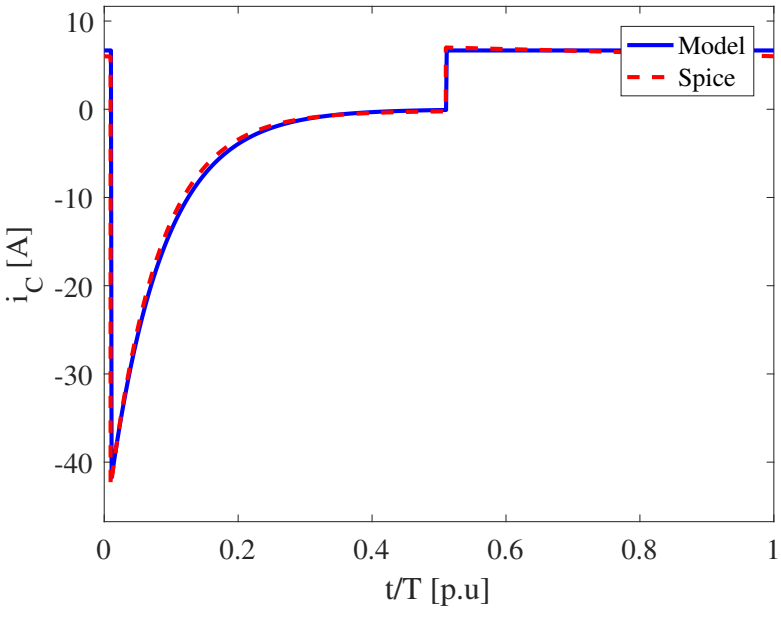
During Interval II, M_1 is clamped by C_{fly} and the drain of M_3 is connected to the output. As a consequence, the blocking voltage of M_1 and M_3 is also V_{out}, while M_2 is conducting the inductor current. Table 3.3 summarizes the stresses on each device. M_1 and M_2 have

Table 3.3: Device stress summary for the Hybrid Buck converter

Device	$V_{ds,max}$	$I_{d,max}$
M_1	V_{out}	$\frac{I_{\text{out}}}{2-D} + \frac{\Delta V}{r_{on1}+r_{on3}}$
M_2	V_{out}	$\frac{I_{\text{out}}}{2-D}$
M_3	V_{out}	$\frac{\Delta V}{r_{on1}+r_{on3}}$



(a) Capacitor voltage $v_{Cfly}(t)$



(b) Capacitor current $i_C(t)$

Figure 3.19: Comparison between the analytical model and spice simulation for the Hybrid Buck converter

higher current stress due to the charge sharing process. However, the peak current value of the capacitor during Interval I is dictated by the voltage difference ΔV and the resistance $r_{on1} + r_{on3}$. On the other hand, M_2 conducts only the inductor current. As a consequence, FETs area can be optimized to achieve lower losses.

3.3.4 Loss Model

In order to construct a loss model for the Hybrid Buck converter, RMS currents through devices have to be calculated. Figure 3.20 shows the current through the three MOSFETs over a full switching period. Current through M_2 is negative because of how it is connected, source to inductor and drain to the output, while M_3 current is the flying capacitor current that flows out to the output.

M_2 rms current is the same as the low-side switch of a Buck converter,

$$I_{2,rms} = I_L\sqrt{1-D}\sqrt{1+\frac{1}{3}\left(\frac{\Delta i_L}{I_L}\right)^2} \tag{3.50}$$

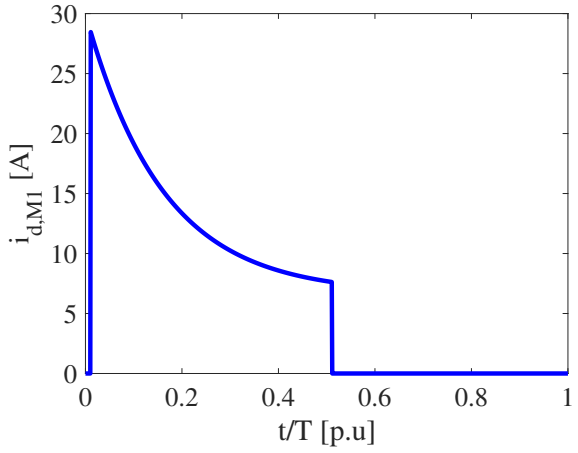
M_3 rms current has to be calculated using the definition of the rms value,

$$I_{3,rms} = \sqrt{\frac{1}{T_s}\int_0^{(1-D)T_s} i_c^2(t)d(t)} \tag{3.51}$$

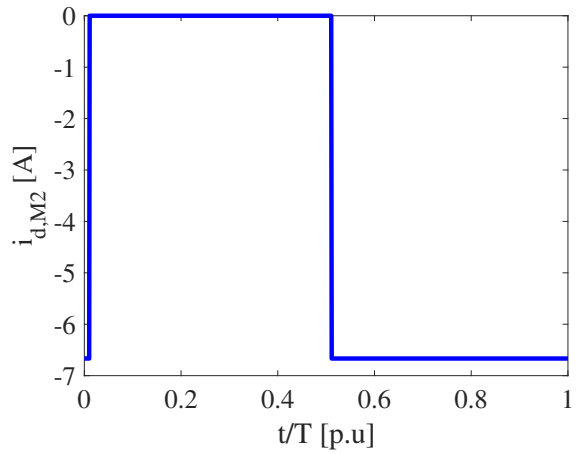
$$= \sqrt{\frac{1}{T_s}\int_0^{(1-D)T_s} \left(\frac{\Delta V}{R_T}e^{-t/\tau}\right)^2 d(t)} \tag{3.52}$$

where τ is $R_T C$. Solving Equation 3.52,

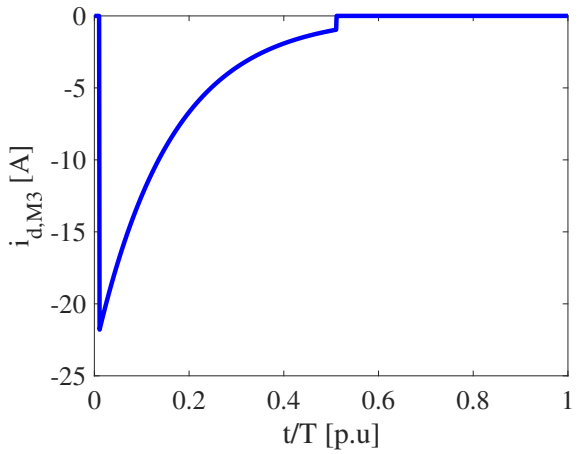
$$I_{3,rms} = \frac{\Delta V}{R_T}\sqrt{\frac{\tau}{2T_s}}\sqrt{1-\exp\left(-\frac{2DT_s}{\tau}\right)} \tag{3.53}$$



(a) i_{d1}



(b) i_{d2}



(c) i_{d3}

Figure 3.20: Current through each device over an entire switching period

To calculate the rms current through M_1,

$$I_{1,rms} = \sqrt{\frac{1}{T_s}\int_0^{DT_s}(i_L(dt) - i_c(t))^2 d(t)} \tag{3.54}$$

$$= \sqrt{A + B + C} \tag{3.55}$$

where: (3.56)

$$A = I_L^2 D \tag{3.57}$$

$$B = -\frac{2\tau I_L \Delta V}{R_T T_s}\left(1 - \exp\left(-\frac{DT_s}{\tau}\right)\right) \tag{3.58}$$

$$C = \left(\frac{\Delta V}{R_T}\right)^2 \frac{\tau}{2T_s}\left(1 - \exp\left(-\frac{2DT_s}{\tau}\right)\right) \tag{3.59}$$

Then, conduction losses are

$$P_{cond,M1} = I_{1,rms}^2 \frac{R_{sp}}{A_1} \tag{3.60}$$

$$P_{cond,M2} = I_{2,rms}^2 \frac{R_{sp}}{A_2} \tag{3.61}$$

$$P_{cond,M3} = I_{3,rms}^2 \frac{R_{sp}}{A_3} \tag{3.62}$$

During the dead time between g_1 and g_2 (Figure 3.15), the inductor current will flow through the body diode of M_2.

$$P_{bd} = 2V_f I_L t_d f_s \tag{3.63}$$

C_{oss} losses are modeled in the same manner that is done for the Buck and 3-Level Buck. When M_1 and M_3 turn on, the equivalent circuit of Figure 3.21 can be drawn. There are three simultaneous processes:

1. Charging C_{ds2} to V_{out} through r_{on3}
2. Discharging C_{ds1} through r_{on1}
3. Discharging C_{ds3} through r_{on3}

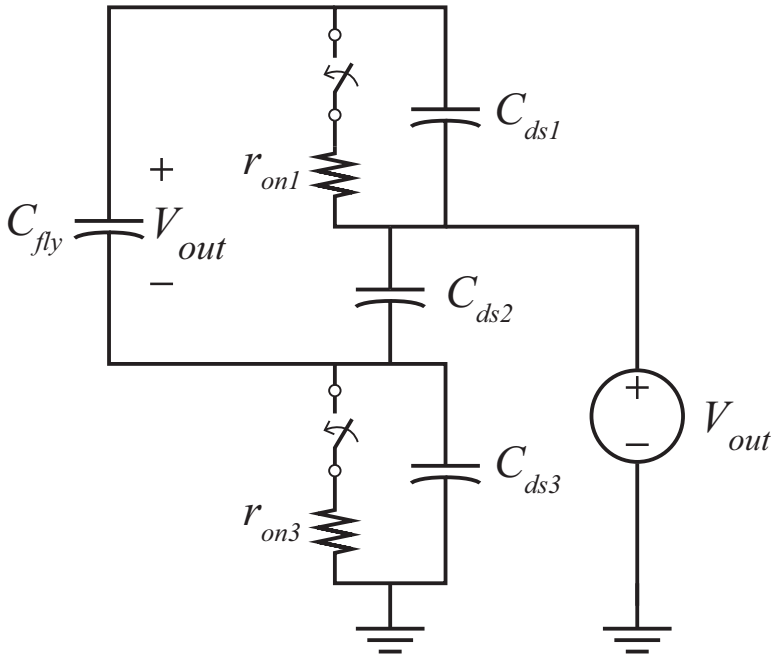


Figure 3.21: C_{oss} equivalent circuit.

Thus, losses associated to these three processes can be calculated using the equivalent charge and energy capacitances as

$$P_{Coss} = \frac{1}{2}\left(C_{eq,E,sp}A_1 - C_{eq,E,sp}A_2 + 2C_{eq,Q,sp}A_2 + C_{eq,E,sp}A_3\right)V^2 f_s \tag{3.64}$$

Overlap losses only occur on M_1, as M_2 will have soft turn on due to its body diode conduction and M_3 does not conduct the inductor current. Then,

$$P_{ov} = \frac{1}{2}V_{\text{out}}I_L Q_{sw,sp}A_1\left(\frac{1}{I_{g,on}} + \frac{1}{I_{g,off}}\right)f_s \tag{3.65}$$

And finally, gate losses are

$$P_{gate} = V_{dr}Q_{g,sp}(A_1 + A_2 + A_3)f_s \tag{3.66}$$

Table 3.4 summarizes the analytical loss model for the Hybrid Buck converter.

Table 3.4: On-chip Loss model for a Hybrid Buck converter

Loss Mechanism	Symbol	Model
M_1 Conduction Loss	P_{cond_1}	$(X+Y+Z)\frac{R_{sp}}{A_1}$
M_2 Conduction Loss	P_{cond_2}	$I_L^2(1-D)\frac{R_{sp}}{A_2}$
M_3 Conduction Loss	P_{cond_3}	$Z\frac{R_{sp}}{A_3}$
Overlap Loss	P_{ov}	$\frac{1}{2}V_{\text{out}}I_L Q_{sw,sp}A_1\left(\frac{1}{I_{g,on}}+\frac{1}{I_{g,off}}\right)f_s$
C_{oss} Loss	P_{Coss}	$\frac{1}{2}\left(C_{eq,E,sp}(A_1-A_2+A_3)+2C_{eq,Q,sp}A_2\right)V^2 f_s$
Gate Loss	P_{gate}	$V_{dr}Q_{g,sp}(A_1+A_2+A_3)f_s$
$X = I_L^2 D$ $Y = -\frac{2\tau I_L \Delta V}{R_T T_s}\left(1-\exp\left(-\frac{DT_s}{\tau}\right)\right)$ $Z = \left(\frac{\Delta V}{R_T}\right)^2 \frac{\tau}{2T_s}\left(1-\exp\left(-\frac{2DT_s}{\tau}\right)\right)$		

3.3.5 Design space

In order to explore the losses of the Hybrid Buck converter, it is analyzed over the input voltage and output current while varying the total switch area as performed for the previous converter's analysis. The fact that each switch conducts different currents, opens a window for FET area optimization. The device with highest conduction losses is M_1 as its current is composed of the inductor current and the flying capacitor current. It will be desirable then to maximize this MOSFET's area in order to compensate for the high current flow. M_2 conducts only the inductor current while M_3 the flying capacitor current. According to Equation 3.42, the peak current during the charge sharing process is

$$I_{\text{peak}} = \frac{\Delta V}{r_{on1}+r_{on3}} \tag{3.67}$$

Reducing this value will only reduce the losses on M_1; M_3 losses are not dependent on its on-resistance value as it is essentially the discharge of the flying capacitor through r_{on3}. ΔV can be reduced by decreasing the inductor current, which is not a design variable, or by increasing the flying capacitor value. Thus, it seems evident that increasing the area

of M_1 and decreasing the area for the other devices can benefit the performance of the converter. Figure 3.22 shows on-chip losses of the converter for optimized FETs area and for even distributed areas. The operating point is for $V_g = 5$ V, $V_{out} = 4$ V, $I_{out} = 10$ A and $f_{sw} = 1$ MHz. At moderate and low total FET areas, a loss reduction of 20 % is achieved by proper sizing. Optimization effect is reduced at large areas. Using the optimum sizing ratio, loss map plots for a 4 V output voltage Hybrid Buck converter are shown in Figure 3.23 where the input voltage is swept from 5 V to 8 V and the total FET area from 0.5 mm^2 to 10 mm^2. The combination of low blocking voltage devices with an optimized switch area contribute to low loss performance. These plots do not include inductor losses which is an important characteristic of this converter. Step down converters like the Buck, Cascaded SC-Buck converters has the inductor at the output conducting the load current, where the higher conduction loss takes place.

3.4 Topology comparison

The Buck converter is the simplest topology, using only two devices. However, both devices have to block the input voltage and conduct the output current. As the area of the switches increases, switching losses become dominant increasing the total power loss. The 3-Level

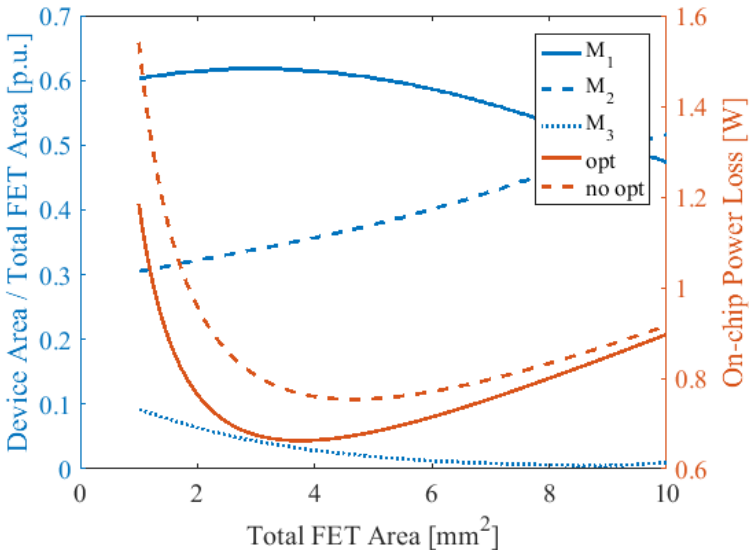
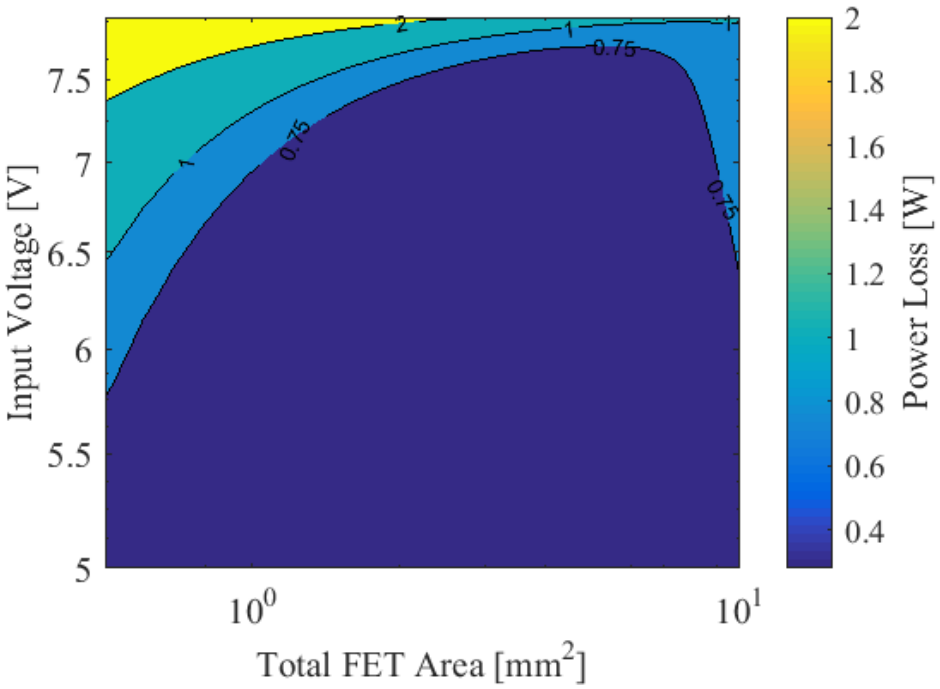
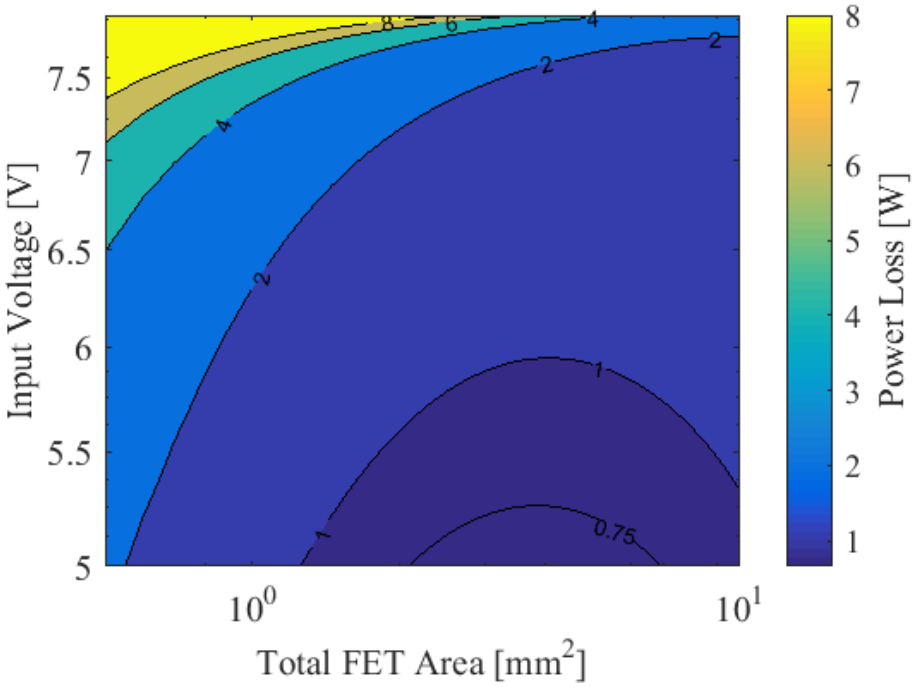


Figure 3.22: Optimizing the switch area for a Hybrid Buck converter.



(a) $I_{\text{out}} = 5\,A$



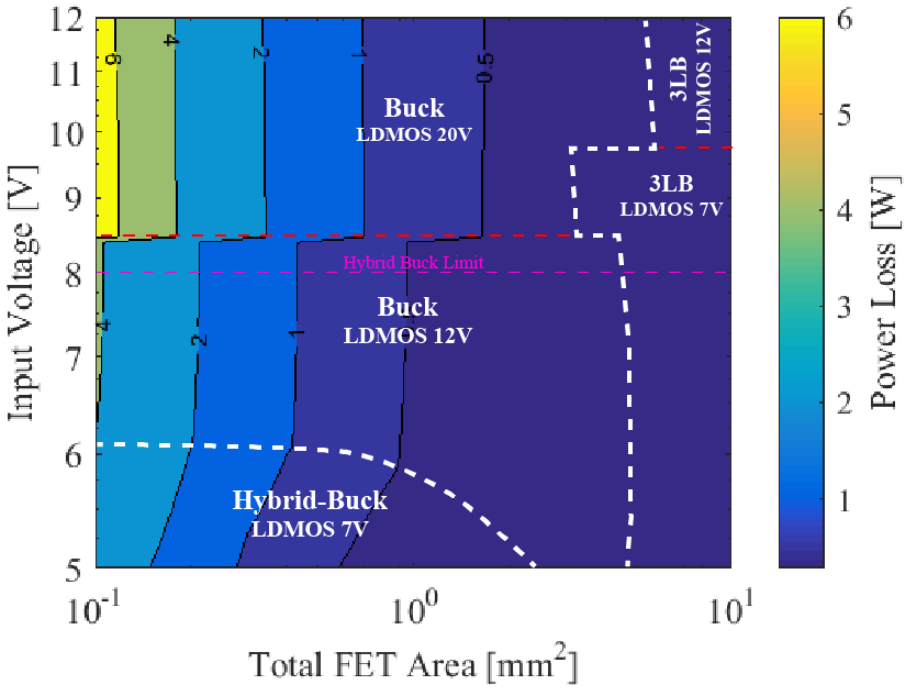
(b) $I_{\text{out}} = 10\,A$

Figure 3.23: On-chip loss map for a Hybrid Buck converter.

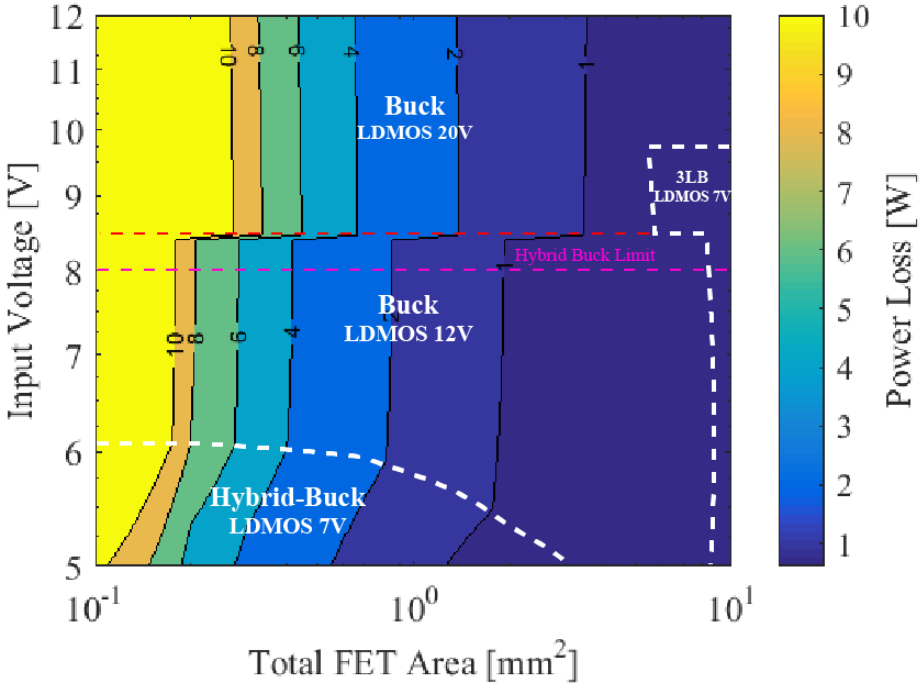
Buck overcomes this drawback. Each device has to block half the input voltage and due to the reduced volt-seconds applied to the inductor it can be operated at a lower frequency. Both characteristics contribute to potentially reduce total losses by using lower blocking voltage devices. However, the fact that there are two devices in series conducting the output current, creates a strong dependence on the process to mitigate conduction losses when compared with the Buck. The Hybrid Buck converter has output voltage rated devices, the inductor is at the input (lower current port for a step-down converter) and essentially only one switch is conducting at any interval. Table 3.5 summarizes the device stresses for each topology. To compare the performance of the three analyzed converters, the total power loss will be computed over the input voltage and the total power stage area for different currents. Device's size is optimized at each operating point. The inductor value is 1 μH and the operating frequency is 1 MHz for the Buck and the Hybrid Buck and 500 kHz for the 3-Level Buck in order to account for the advantage of this converter. Device selection is performed as a function of the input voltage. FETs area is optimized as shown in previous sections for the three converters. Figure 3.24 shows the the topology that has lowest on-chip losses at each design point for output currents of 5 A and 10 A. The Hybrid Buck converter losses over the Buck converter as the load current increases. However, one of the important characteristics of the Hybrid Buck converter is the reduction of the inductor current as it carries the input current. The same comparison is run in Figure 3.25 including a DCR of 10 mΩ to include the losses on the inductor. When computing the total power loss of the

Table 3.5: Device stress comparison for the Buck, the 3-Level Buck and the Hybrid Buck converters.

Topology	Device	Blocking Voltage	Max. Current
Buck	$M_{1,2}$	V_g	I_{out}
3-Level Buck	$M_{1,2,3,4}$	$V_g/2$	I_{out}
Hybrid Buck	M_1	V_{out}	$\frac{I_{\text{out}}}{2-D} + \frac{\Delta V}{r_{on1}+r_{on3}}$
	M_2		$\frac{I_{\text{out}}}{2-D}$
	M_3		$\frac{\Delta V}{r_{on1}+r_{on3}}$

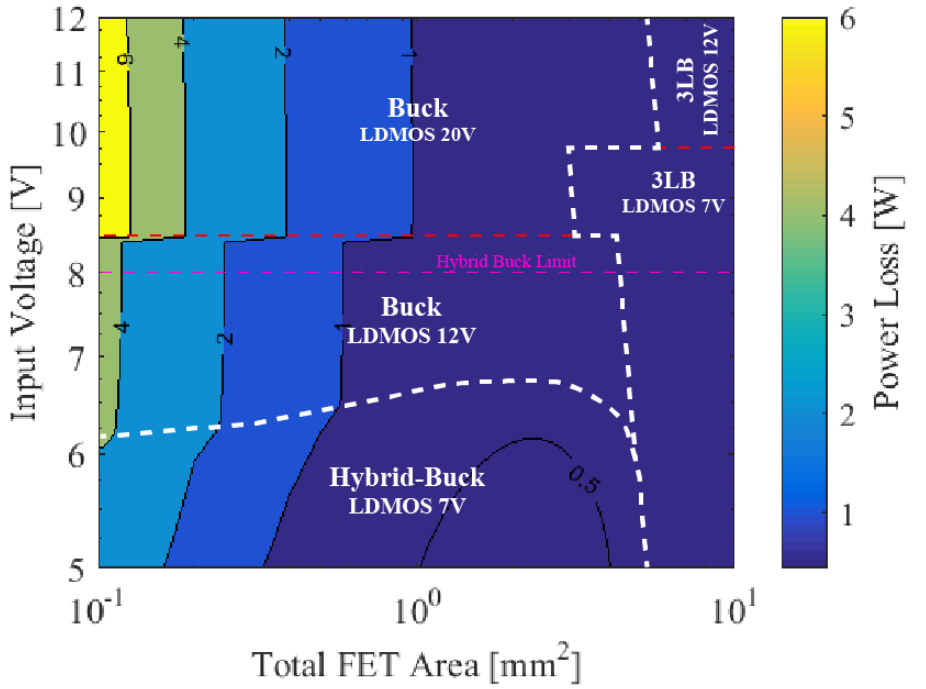


(a) $I_{\text{out}} = 5\,\text{A}$

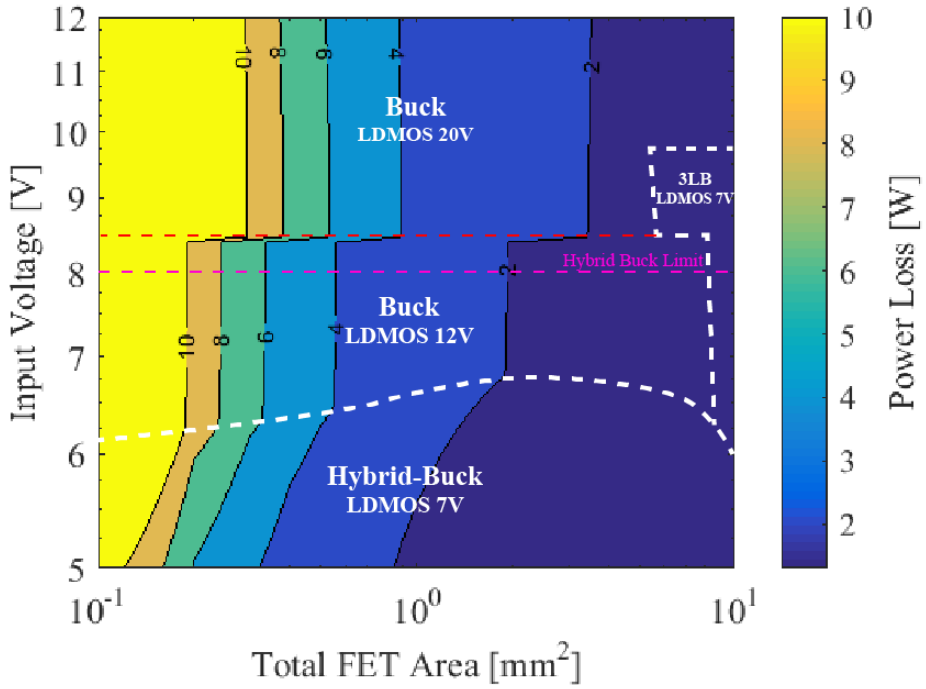


(b) $I_{\text{out}} = 10\,\text{A}$

Figure 3.24: Topology comparison over input voltage and total power switch area.



(a) $I_{\text{out}} = 5\,\text{A}$



(b) $I_{\text{out}} = 10\,\text{A}$

Figure 3.25: Topology comparison over input voltage and total power switch area including inductor losses.

converter, the Hybrid Buck extends the design area where it has lower losses because of lower inductor losses.

3.5 Summary

In this chapter, three topologies have been explored. For each of them, an analytical loss model has been constructed based on circuit parameters extracted from simple simulations. Losses on each converter are expressed in terms of device dimensions, making it easy to explore losses as a function of the converter's area. The Hybrid Buck converter has been presented with potential benefits that can help to reduce losses on an integrated battery charger under a range of input voltages. A comparison has been made showing the importance of optimizing the switch's size on the Hybrid Buck and the main advantage of having the inductor moved back to the input port.

Chapter 4

Implementations

In Chapter 3, analytical loss model for a Buck, a 3-Level Buck and a Hybrid Buck converter are built and used to compare the performance of the three topologies over the input voltage and total FET area. In this Chapter, validation of the loss models through experimental results is performed. In addition, analysis of parasitics and packaging is done for each implementation.

4.1 Integrated Buck converter

A buck converter is designed to meet the requirement of 2 W on-chip losses under the specifications of Table 4.1. Section 3.1.2 analyzes how switch area can be optimized to balance losses on each device. The optimization is performed on this design to size the

Table 4.1: Design parameters for Buck converter

Parameter	Value
V_g	5 V
V_{out}	4 V
I_{out}	10 A
f_s	1 MHz
L	1µH
$P_{loss,max}$	2 W

LDMOS individually to get the lowest power stage area for 2 W of losses on-chip as is shown in Figure 4.1. The on-resistances for the switches are $R_{on,1} = 17$ mΩ and $R_{on,2} = 26$ mΩ. The estimated power loss breakdown at full load is shown in Figure 4.2 The design is dominated by conduction losses due to its small power MOSFET area of 0.8 mm^2. The complete power stage (Figure 4.3a) includes the last stage of a gate driver (gate buffer) in order to minimize the gate loop inductance that can cause false turn on and to minimize the gate resistance to mitigate crosstalk conduction due to high dv/dt on the switching node. To achieve fast transitions on the switches, the driving stage can source and sink 3 A. Driving the gate buffer with NMOS and PMOS gates connected, will cause shoot-through current during the turn on/off transition of the gate driver signals. To avoid this, separate signals are fed into the NMOS and PMOS gates of each gate buffer (Figure 4.3c) adding a dead time between the signals. The power stage uses 12 V LDMOS devices and the gate buffers are 7 V isolated NMOS. The layout view is shown in Figure 4.3b. As the high-side device is larger than the low-side device, the former is broken into 4 devices in parallel while the latter is split into two devices in parallel in order to achieve a compact layout. The process used in this work to design and fabricate the ICs has 3 thin metal layer levels plus a top metal layer of thick

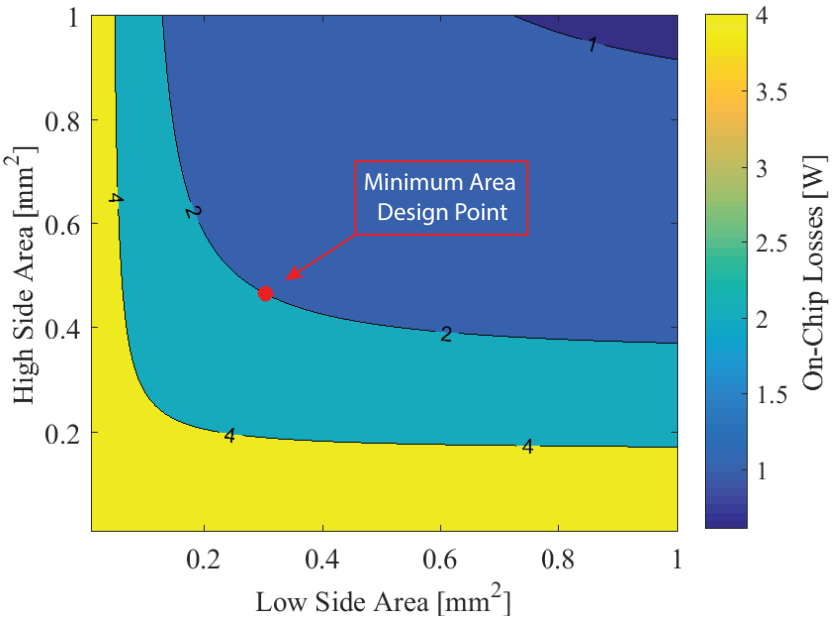


Figure 4.1: Design optimization at full load. The red dot indicates the minimum area design plot for 2 W of losses.

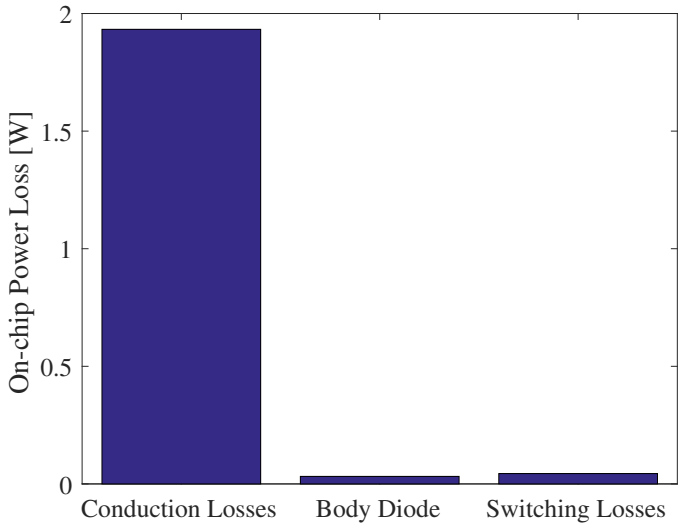
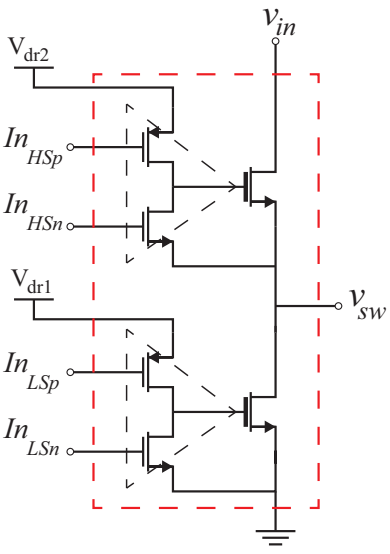


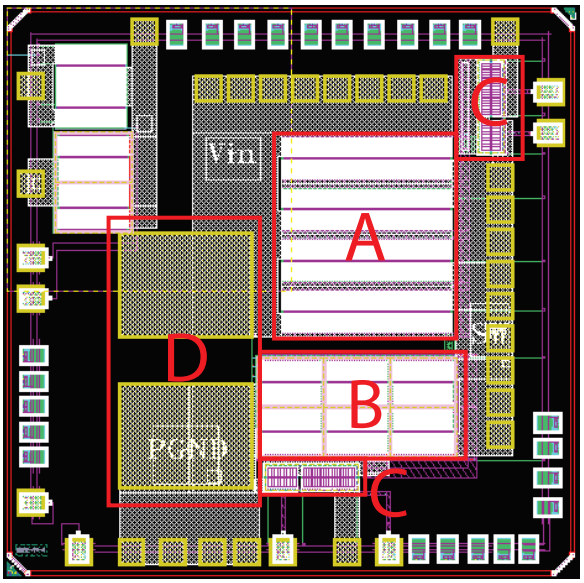
Figure 4.2: Power loss breakdown for the designed power stage at 10 A.

copper. For this reason, the metallization for each LDMOS device is designed to minimize the flow of current through the lower metal layers. Figure 4.4 shows one of the row LDMOS devices that forms the high-side switch. This row consists of multiple LDMOS in parallel placed in a multi-finger structure to minimize the total drain area that will determine the gate-drain capacitance of the device [52]. Drain and source run horizontally on the top copper layer. Figure 4.5 shows the two cross sections AA' and BB' of Figure 4.4 for a single finger. Connections to the drain and the source are made vertically by stacked vias minimizing metallization. Assuming there is a uniform current distribution, it will be split equally between the rows and each finger will conduct only a portion of that current.

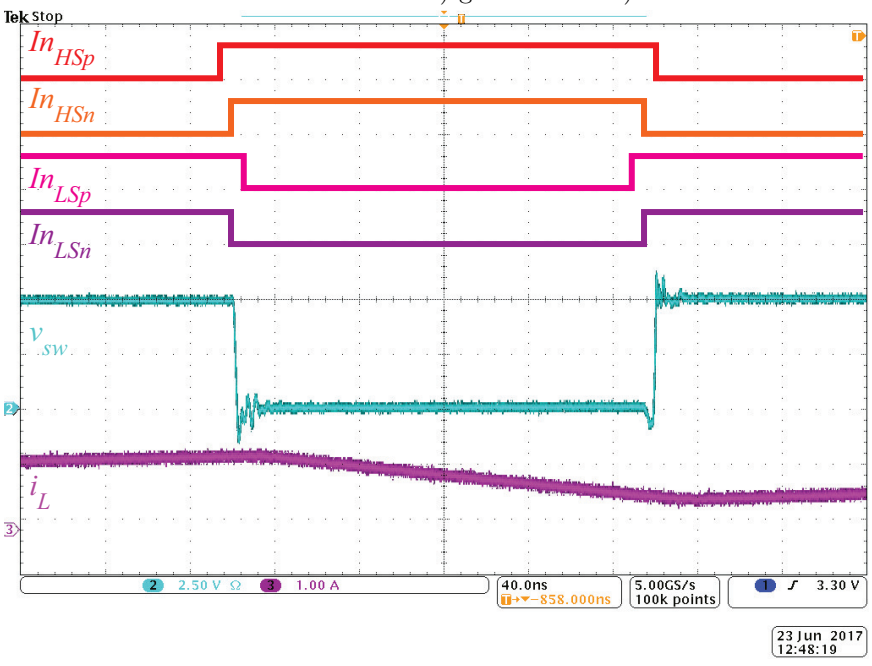
In section 3.1.2 is explained how power loop inductance impacts on the overshoot of the switching node, increasing voltage stress on the switches. In particular, bondwire inductance can not be mitigated by placing the decoupling capacitors outside of the chip. More over, integrated capacitors presents a higher power loop impedance than the outside loop, having little effect on reducing the power loop inductance because of ESR and capacitance density. However, a discrete ceramic capacitor placed as a SiP can reduce the overshoot as the bondwires are left outside of the loop and its impedance is smaller than the outer loop. 0402 pads were added to the layout on the exposed top copper layer for a ceramic decoupling capacitor. Figure 4.6 shows a photograph of the packaged design in a standard QFN 40 with



(a) Schematic



(b) Layout view. A) high-side device B) low-side device C) gate buffers D) 0402 Pads



(c) Operating waveforms.

Figure 4.3: Designed Buck converter.

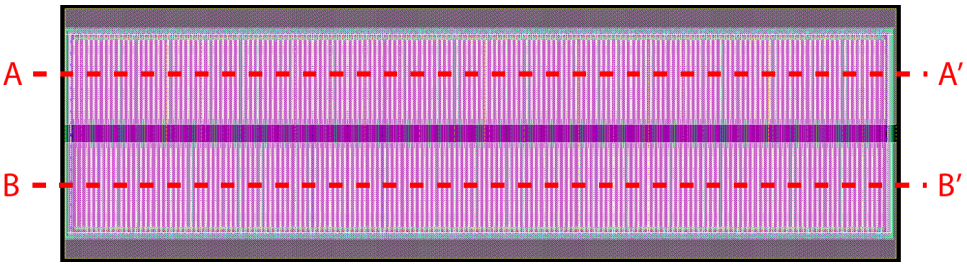
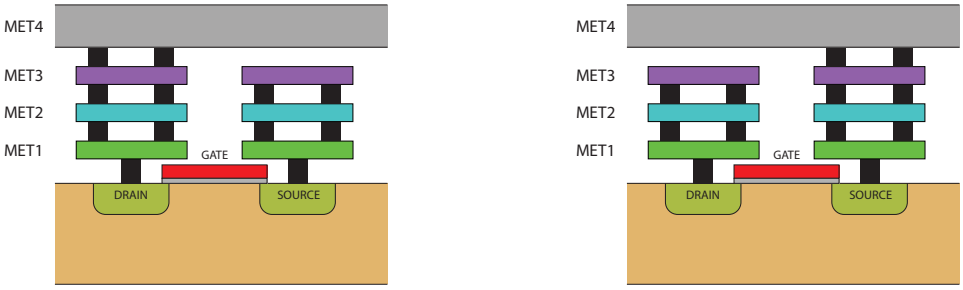


Figure 4.4: LDMOS layout view.



(a) AA' cross section of a single finger.

(b) BB' cross section of a single finger

Figure 4.5: Cross section views of Figure 4.4 for the same finger.

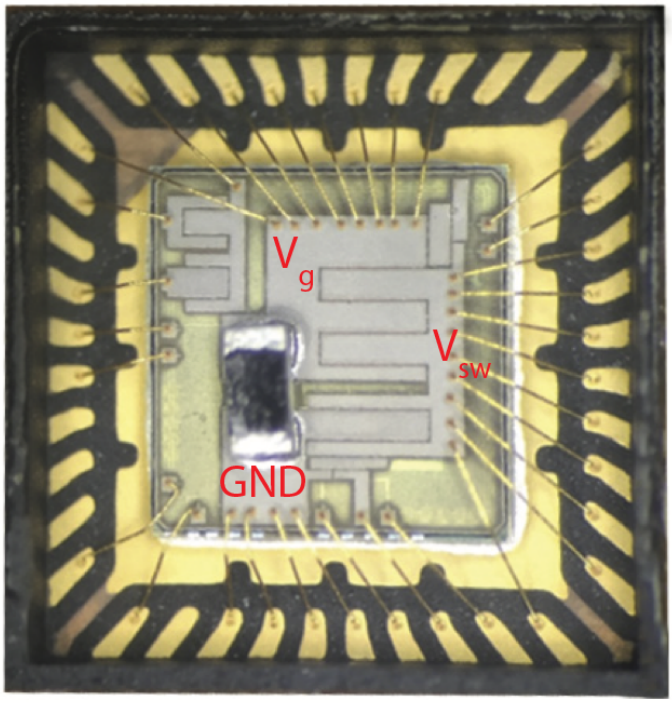


Figure 4.6: 0402 Decoupling capacitor soldered as a SiP over the power stage, minimizing the power loop inductance.

removable lid. The decoupling capacitor is soldered next to the power stage minimizing the power loop inductance. The value of the capacitor is 2.2 μF in a 0402 package in order to keep the inductance on the loop to a minimum.

To test the Buck converter 7 V power supplies (one isolated) are used for the gate buffer's driving voltage and a two channel isolated gate driver is used to drive the input signals for each switch (Figure 4.7). The decoupling capacitors for the outer loop are placed on the bottom layer.

4.1.1 Switching node overshoot mitigation

In order to verify the effect of the decoupling capacitor the switching node waveform is captured under the same testing conditions, i.e. dead time, frequency, load current, duty cycle and input voltage, for a testing board that has the SiP capacitor soldered and for another test board that only contains the outer decoupling capacitors. Figure 4.8 shows both waveforms the inductor current. When bondwires are part of the power loop (Figure 4.8a) the overshoot produced on the switching node increase the voltage stress beyond the input voltage by 7 V. For this reason, instead of using 7 V devices, with lower R_{sp} for a 5 V application, higher voltage devices may be required, requiring more area for the same target

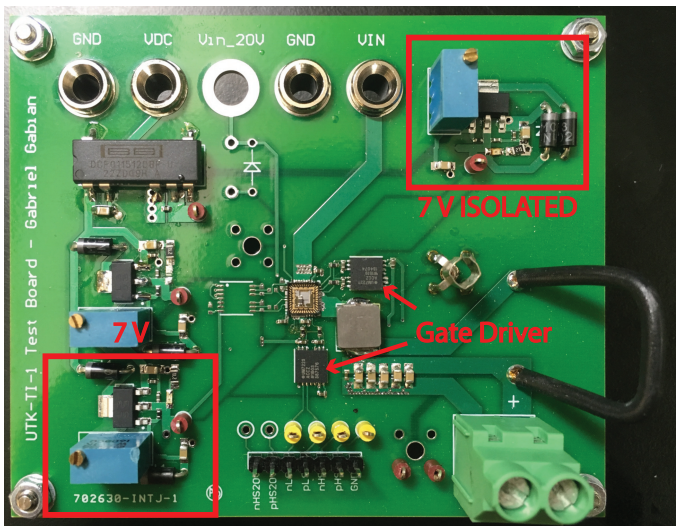
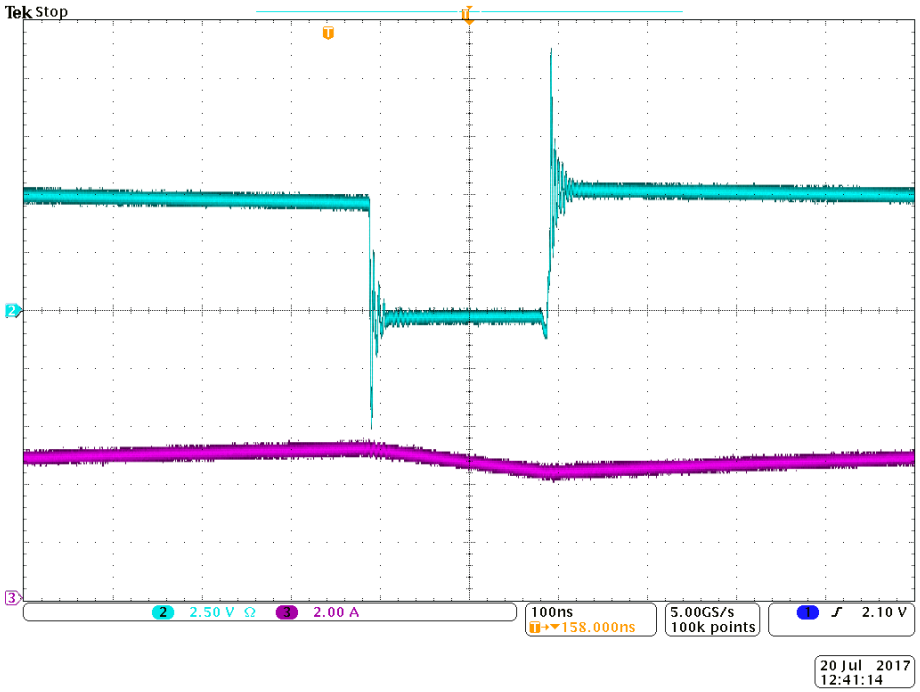
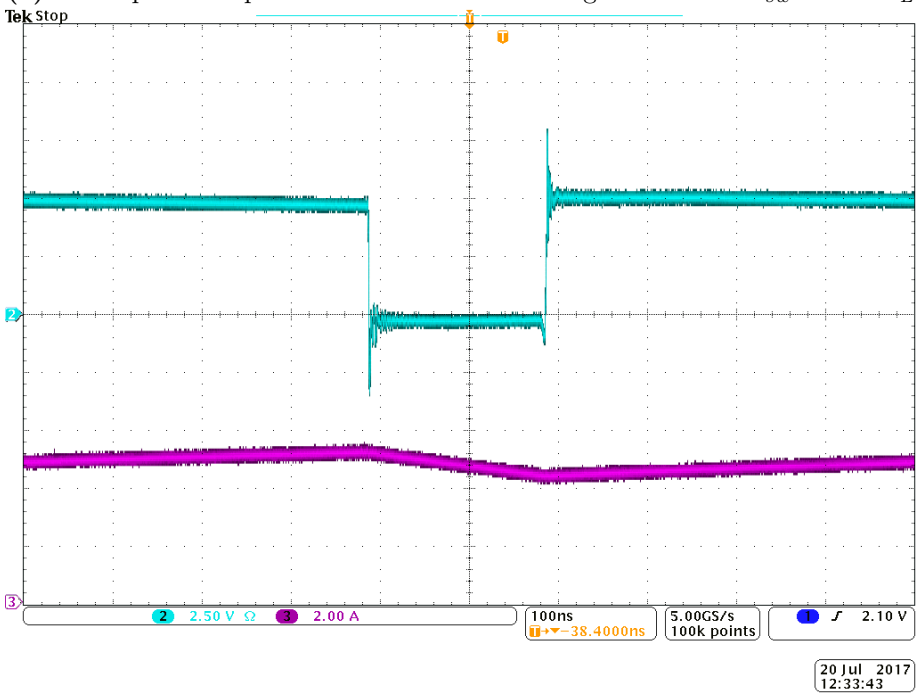


Figure 4.7: Test board for the implemented Buck converter with SiP decoupling capacitor.



(a) Outer power loop. Overshoot on the switching node. CH2: v_{sw} - CH3: i_L



(b) Power loop inductance is reduced with the SiP decoupling capacitor. CH2: v_{sw} - CH3: i_L

Figure 4.8: Switching node waveforms comparison.

power loss. However, the SiP capacitor significantly reduces the overshoot and the duration of the ringing.

4.1.2 Loss measurement

On-chip power loss is calculated by measuring parasitic resistances outside of the package and subtracting their losses to the total converter loss. Figure 4.9 shows the equivalent circuit of the converter including all the parasitic resistances involved in the power flow. R_{pcb1} and R_{pcb2} can be neglected as the voltage is measured using kelvin connections at the input port of the integrated power stage. The following parasitic resistances were measured:

$$R_{par1} = r_{bw1} + r_{met1} + r_{on1} + r_{bw} = 38\,m\Omega \tag{4.1}$$

$$R_{par2} = r_{bw2} + r_{met2} + r_{on2} + r_{bw} = 66.5\,m\Omega \tag{4.2}$$

$$R_{par3} = r_{dcr} + r_{pcb3} + r_{pcb4} = 15\,m\Omega \tag{4.3}$$

R_{par1} and R_{par3} are measured by turning on the high-side device while applying a DC current between the positive input port and the output node and measuring the voltage drop between the input and the switching node and between the switching node and the output. r_{pcb4} is measured by injecting a current between the negative input and output ports of the test board. R_{par2} is computed with the same technique, but with the low-side device turned on and measuring the voltage drop between the negative input and the switching node. Then,

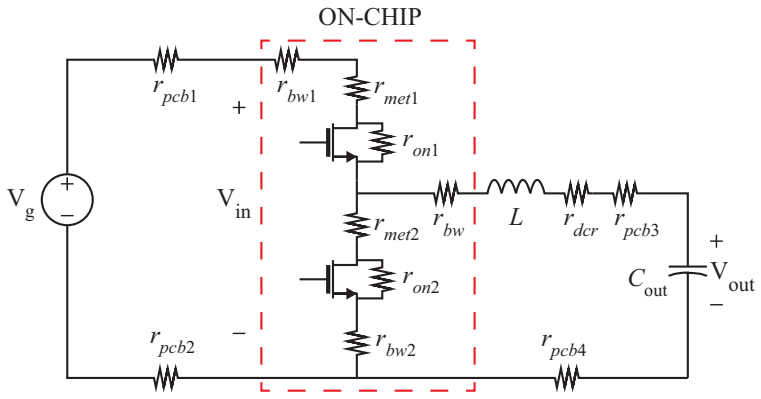


Figure 4.9: Parasitic resistance model for the Buck converter.

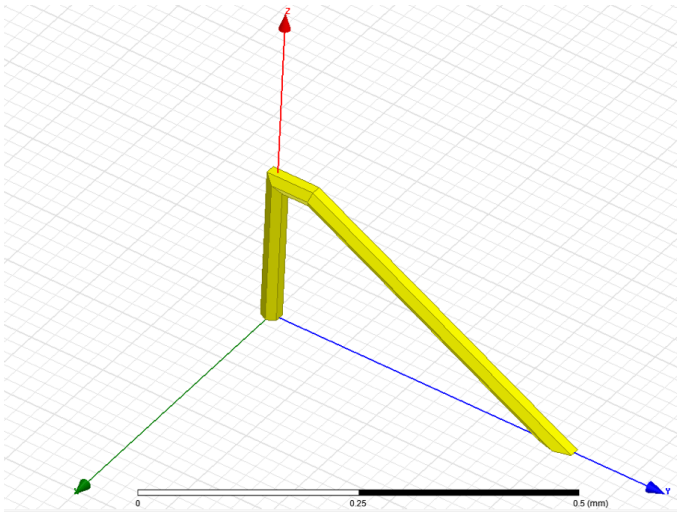
on-chip losses can be calculated as

$$P_{on-chip} = P_{in} - P_{out} - I_{L,rms}^2 R_{par3} \tag{4.4}$$

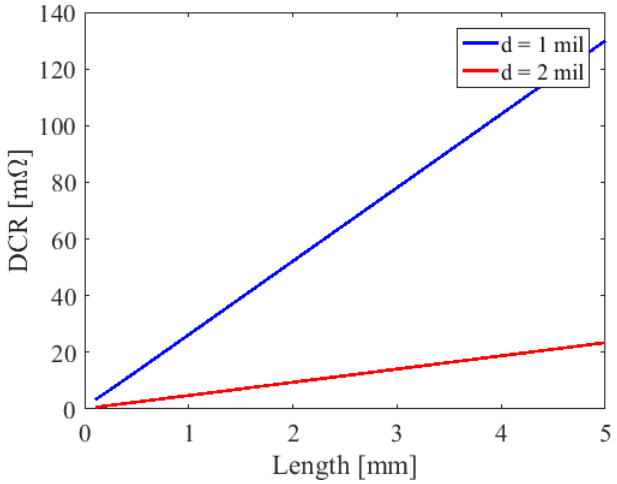
Values of R_{par1} and R_{par2} are much bigger than the designed on-resistance. In this design, bondwire and metallization resistances will dominate conduction losses. bondwire and metallization contribution to the parasitic resistances is analyzed using *Q3D*. The model to characterize the bondwire's parasitic resistance is shown in Figure 4.10a. The material assigned to the structure is gold with a thickness of 1 mil as it is in the implemented design. Skin depth for gold is 75 µm and 25 µm at 1 MHz and 10 MHz respectively. Then, for a 1 mil bondwire, there is a negligible change on the resistance over frequency. Then, the DC resistance is extracted as a function of the total length. Results for for the DC and AC resistance for thicknesses of 1 mil and 2 mil are shown in Figure 4.10. As is shown, contribution of bondwire to conduction losses can be as high as the power MOSFETs contribution. Doubling the thickness of the bondwires reduces the DC resistance by a factor of 4, as is expected due to the resistance of a cylindrical conductor,

$$R = \rho \frac{l}{\pi r^2} \tag{4.5}$$

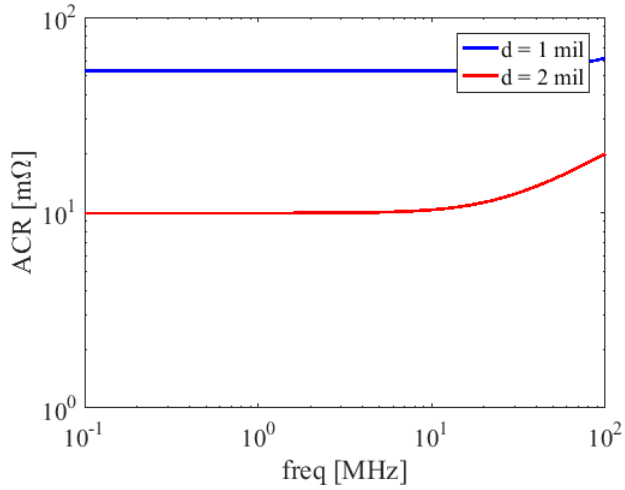
where l is the length of the conductor, r is the radii and ρ is the resistivity of the material. Thus, mitigation of the bondwires can be done by using thicker diameters. To verify this assumptions and to contrast the parasitic resistance measurements, a 3D model of the package along with the die and the bondwires is constructed (Figure 4.11a). MOSFETs are modeled as resistive blocks with equivalent resistivity per unit area. The resistance between the input node and the switching node (R_{par1}) and between ground and the switching node (R_{par2}) were extracted and compared with measurements (Table 4.2). Recalling that the designed on resistance for M_1 is 17mΩ and for M_2 is 26mΩ, metallization and bondwire resistance dominate the loss model of the converter. In Figure 4.11b the current flows along top metal fingers. Moreover, the beginning and the end of each metal runner, on the input and output respectively, carry more current than their opposite ends as current goes through the MOSFETs. Measured parasitic resistances are added to the model of Table 4.1



(a) Bondwire 3D model

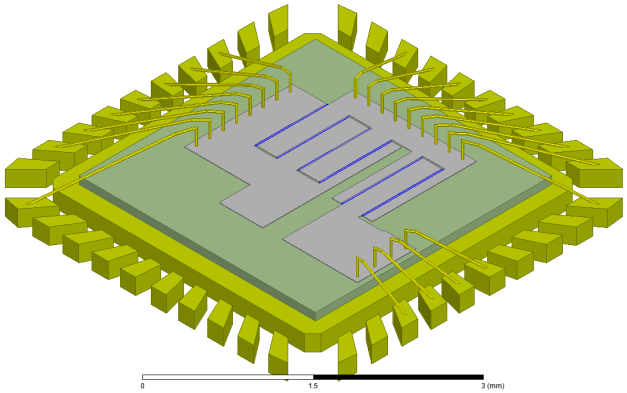


(b) DC Resistance for 1 mil and 2 mil bondwires

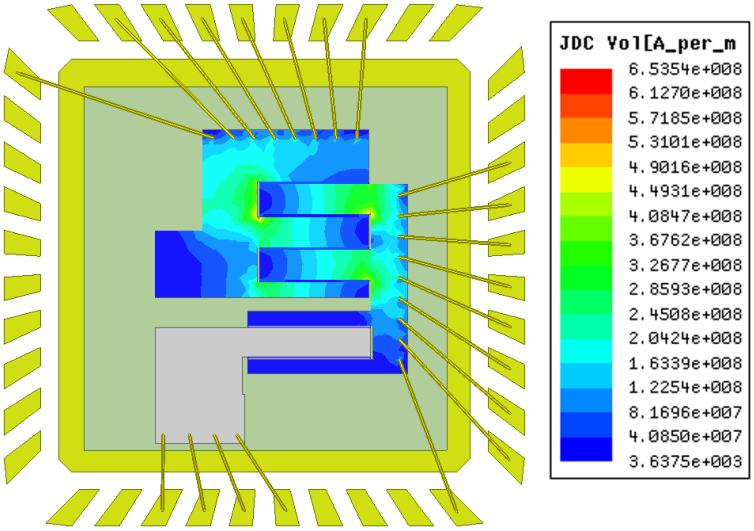


(c) AC Resistance for 1 mil and 2 mil bondwires for $l = 1$ mm

Figure 4.10: DC resistance of gold bondwires for 1 mil and 2 mil thickness.



(a) 3D model constructed to extract parasitic resistances



(b) Current distribution

Figure 4.11: 3D model

Table 4.2: Extracted parasitic resistances for a Buck converter

Parameter	Model	Measured
R_{par1}	40 mΩ	38 mΩ
R_{par2}	70 mΩ	66.5 mΩ

as conduction losses to calculate on-chip losses and compare to measurements (Figure 4.12). The analytical model matches with test results for currents lower than 3.5 A. However, for higher currents measured losses are larger than predicted. This behavior can be clearly seen at 5.5 A where the difference is more than 10%. A possible explanation for this trend is that power losses is rising the temperature of the die and bondwires increasing the resistance. At 5.5 A the temperature on the die rises to 60°C (Figure 4.13). There are three materials that conform on-chip parasitic resistances R_{par1} and R_{par2}: gold (r_{bw}), copper (r_{met}) and silicon (r_{on}). The on-resistance temperature coefficient is available in the data process manuals. Gold and copper are well known materials and have a similar temperature coefficient. Figure 4.14 shows the change of parasitics resistances over temperature. Including this effect on the model (Figure 4.15) results in a more accurate loss model.

4.1.3 Improvements

In this design, an integrated Buck power stage is implemented using 12 V LDMOS devices. The design point is a 5 V to 4 V converter with 2 W of losses at 40 W of output power. However, due to parasitics introduced by packaging, i.e. bondwires, and metallization, losses on-chip exceeded the 2 W design goal. A decoupling capacitor as a SiP is used to successfully

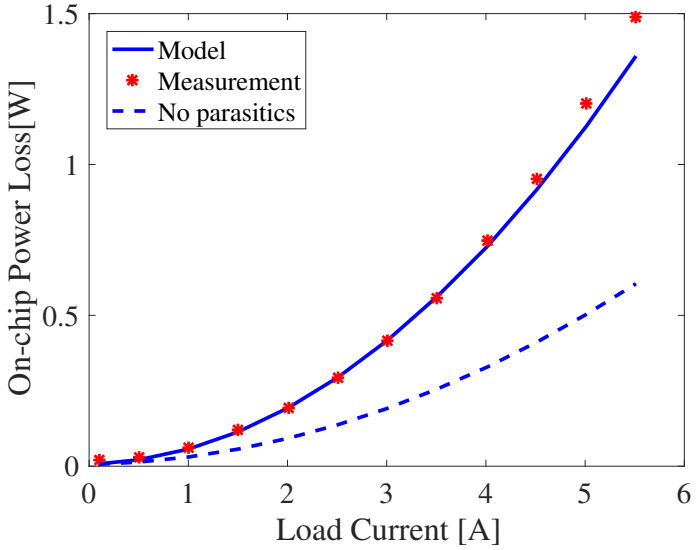


Figure 4.12: Loss measurement and analytical model for the implemented Buck converter with SiP capacitor.

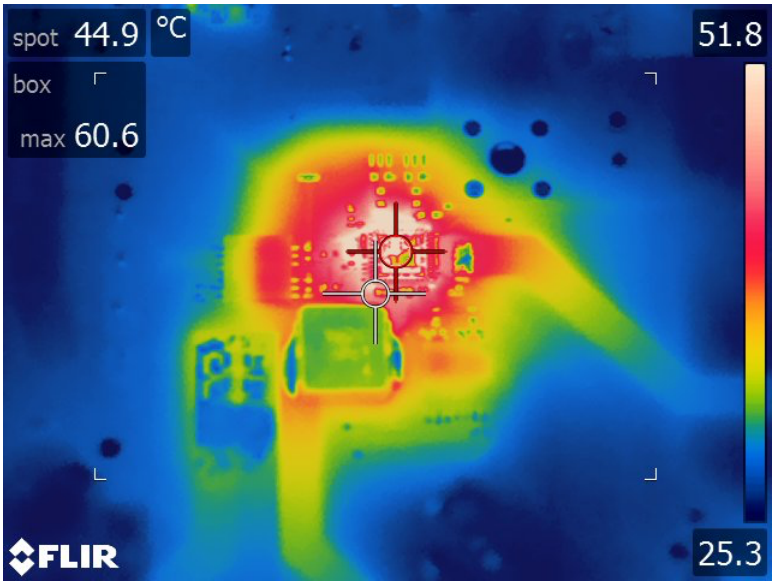


Figure 4.13: Thermal image of Buck converter's power stage at 5.5 A.

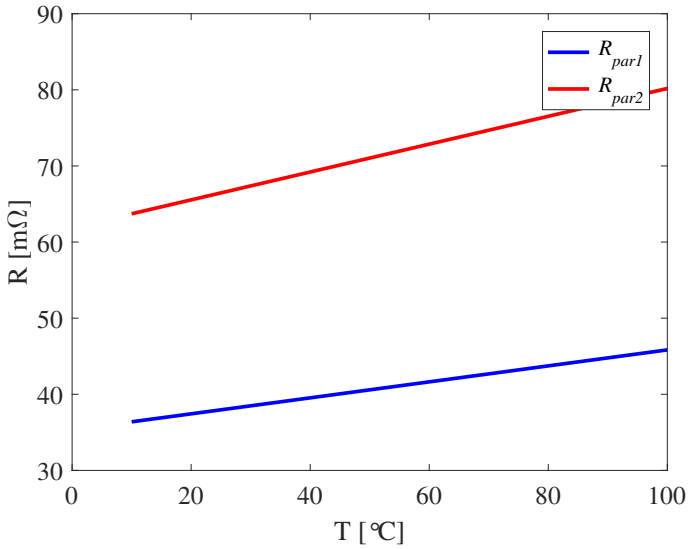


Figure 4.14: Variation of resistance over temperature for parasitic resistances R_{par1} and R_{par2}.

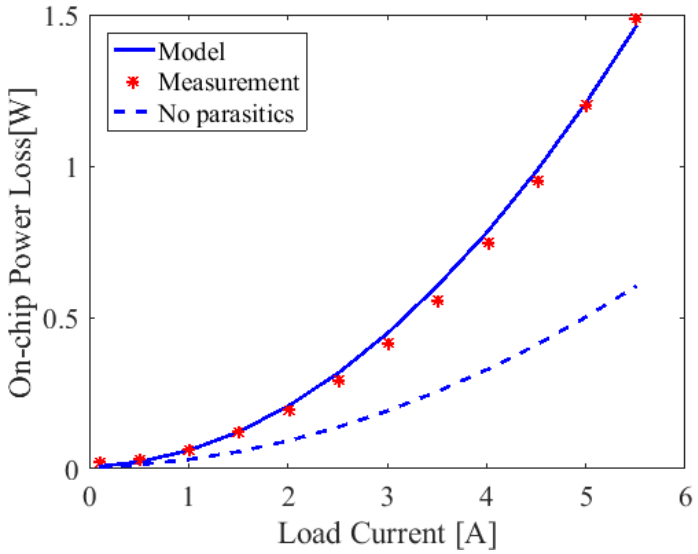


Figure 4.15: Adding temperature coefficient to parasitic resistances. Loss comparison between measured data and model with and without correction at 5.5 A.

reduce the overshoot on the switching node. As a consequence, assuming that a device can tolerate a small voltage in excess of its breakdown voltage for a short amount of time, lower voltage devices with lower R_{sp} can be used. In addition, thicker bondwires can be used to reduce the parasitic resistance. Redesigning the power stage using 7 V LDMOS devices, in the same area, the on-resistances are $R_{on1} = 7.2\,\text{m}\Omega$ and $R_{on2} = 13.6\,\text{m}\Omega$. Using 2 mil thick bondwires and the same metallization, a new parasitic resistance is extracted, $R_{par1} = 22.3\,\text{m}\Omega$ and $R_{par2} = 41.3\,\text{m}\Omega$. Predicted on-chip losses for the redesigned Buck converter are calculated using this values in the loss model (Figure 4.16). Even though losses are reduced by 60% at 10 A, it still exceeds 2 W which is the maximum on-chip loss budget. Bondwires are the biggest contribution to the parasitic resistance. However, as shown on Figure 4.11b, the uneven distribution of current along the device's rows can also increment the effective on-resistance as not all of the rows conducts the same current. In addition, current flowing through long metal lines increases the parasitics. A redesign of the power stage layout and the addition of more bondwires is presented in the following sections in order to minimize these effects.

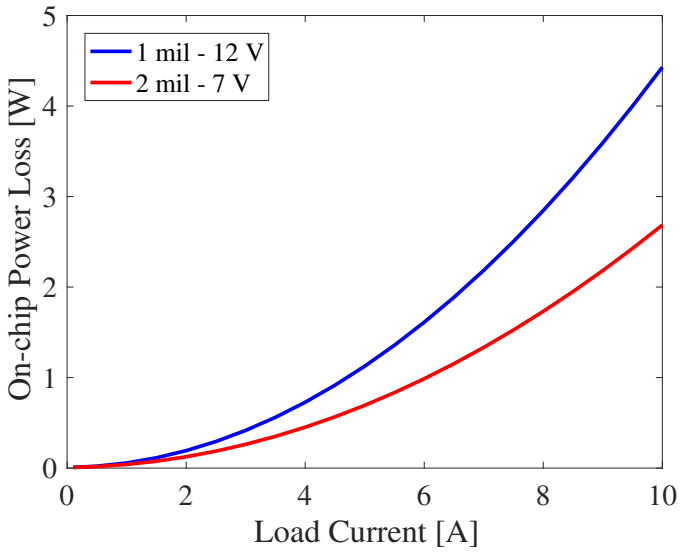


Figure 4.16: Predicted on-chip losses using 2 mil bondwires and 7 V LDMOS for the power stage

4.2 Bondwire analysis

Bondwire parasitic resistance and metallization can degrade the converter's performance. In the previous design current paths go along top metal layer from input/ground to the switching node increasing the parasitic resistance. Minimizing this path is important when low values of on-resistance are desired, as metallization resistance can be comparable to the MOSFET's resistance. On the design of Section 4.1, the top metal conducts current across long runners (Figure 4.11b). To minimize this effect, the layout of the MOSFETs should instead be done as single row devices. Doing this will require metal runners to connect drain and source terminals between them. By doing the layout of the high-side and low-side as single rows, current can flow through wide metal instead of long metal. This idea is shown in Figure 4.17. Each device is placed next to each other, allowing a single metal runner for the switching node. The current flows are from the input (drain of the high-side device) to the switching node (source of the high side device) and from ground (source of the low-side device) to the switching node (drain of the low-side device). This is the best scenario for the current flow, as it goes through wide top metal and down to the devices with the same stacked vias used in Figure 4.5. Bondwires can be placed breadth wise to the top metal runners, following the current flow. In addition, this layout is favorable for the power loop

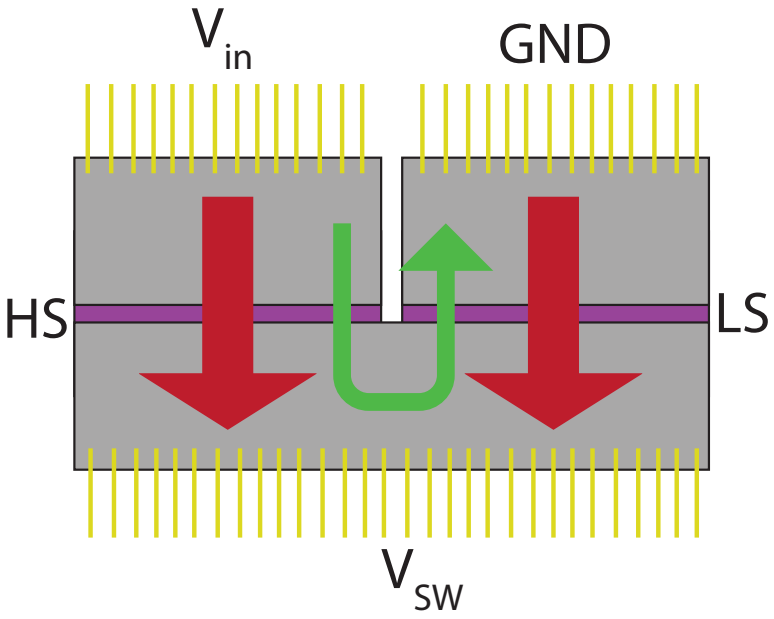


Figure 4.17: Layout view of a single row device Buck converter to minimize metallization resistance.

inductance as V_{in} and GND are next to each other and flux cancellation occurs due to the opposite flow of current. To evaluate this design, 3.5 mΩ and 4.75 mΩ switches are sized to occupy the maximum allowable dimension for a die (7 mm x 4 mm) placed next to each other as shown in Figure 4.17, using 7 V LDMOS devices. From the conclusions on bondwire's impact on additional conduction losses, a 3D model can be constructed in order to predict the parasitic resistance. It is important to use a package with a die attach pad accordingly to the dimensions of the design. Figure 4.18 shows the datasheet of a QFN 40 package with external dimensions of 5 mm x 5 mm. For this particular package, the die attach area is 3.4 mm x 3.4 mm. The smallest package that can be used with a 7 mm die, accordingly to the packaging vendor is a QFN 88, which is used to construct a 3D model. 2 mil gold bondwires, resistive blocks and copper metal sheets are used in Figure 4.19 to extract the total resistances R_{par1} and R_{par2}. Because of the dimensions of the design, the bondwire's length is increased. It is prioritized to reduce the length of the input terminals rather than the switching none, as adding more inductance to this node will only decrease the current ripple without affecting the performance of the converter. Thus, the silicon is placed closer to the leads of the input port. Current distribution when the high-side device is turned on

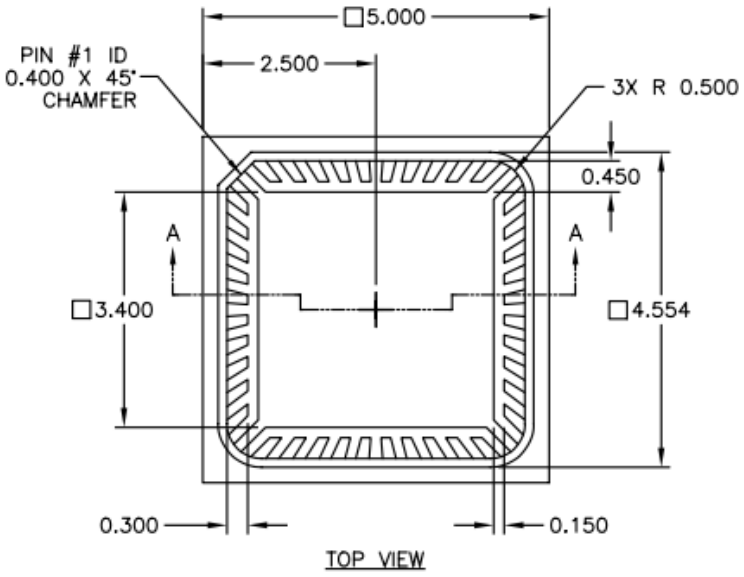


Figure 4.18: QFN package specifications[53]

and when the low-side device is turned on is shown in Figure 4.20. As can see in both cases, current flows into the MOSFETS evenly through the shortest path. This is an improvement from the design on Section 4.1. Extracted values for the parasitic resistances are shown in Table 4.3. Per the current distribution in Figure 4.20, it can be inferred that the additional resistance is produced by the bondwires, increasing the total on-resistance of the devices by 340%. This is verified by modeling the LDMOS and the bondwires as perfect conductors and repeating the simulation. The equivalent resistances were 0.5 mΩ and 0.6 mΩ. To graphically show how this can impact on the converter's losses, a comparison between the ideal design and the extracted model is shown in Figure 4.21. Although on-chip losses are below the target of 2 W, the size of the package is large compared to the size of the power stage. Commercial available battery chargers on Table 1.1 are packaged in 4mm x 4mm QFN. Thus, the converter of Figure 4.19 is bigger than two commercial 5 A available solutions.

4.3 Custom flip chip Buck converter

Based on the analysis of the previous section, for a high current application, losses due to bondwire parasitics dominate conduction losses of the converter. Flip chip is an alternative

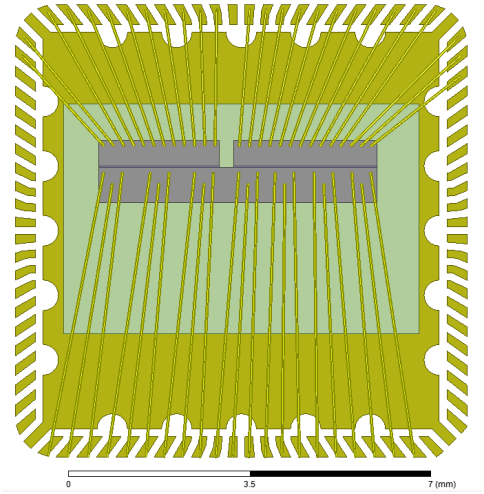
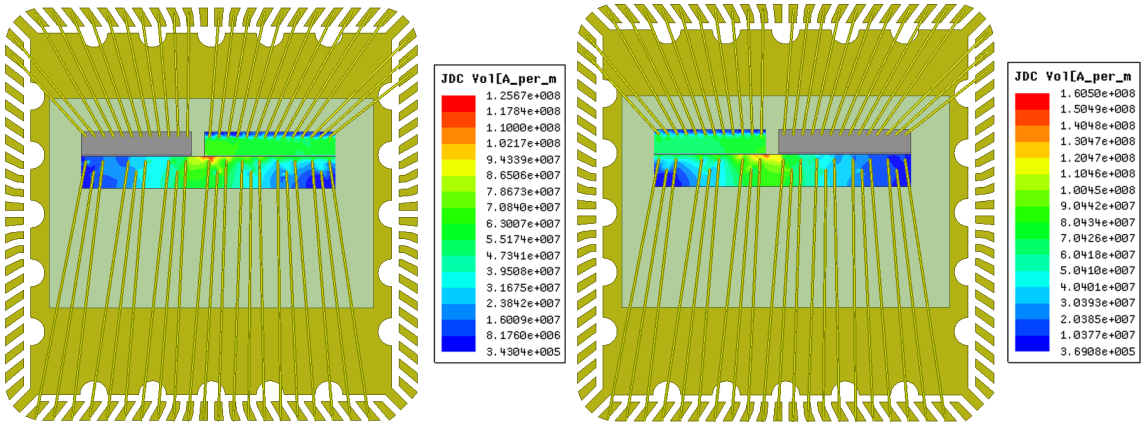


Figure 4.19: 3D model used to estimate the bondwire and metallization effect on a low on-resistance integrated Buck converter.



(a) V_{in} to V_{sw} current flow.

(b) P_{gnd} to V_{sw} current flow

Figure 4.20: On-chip current distribution for a low on-resistance Buck converter in a QFN package.

Table 4.3: Extracted parasitic resistances for a low on-resistance Buck with bondwires

Parameter	Model
R_{par1}	12 mΩ
R_{par2}	14.5 mΩ

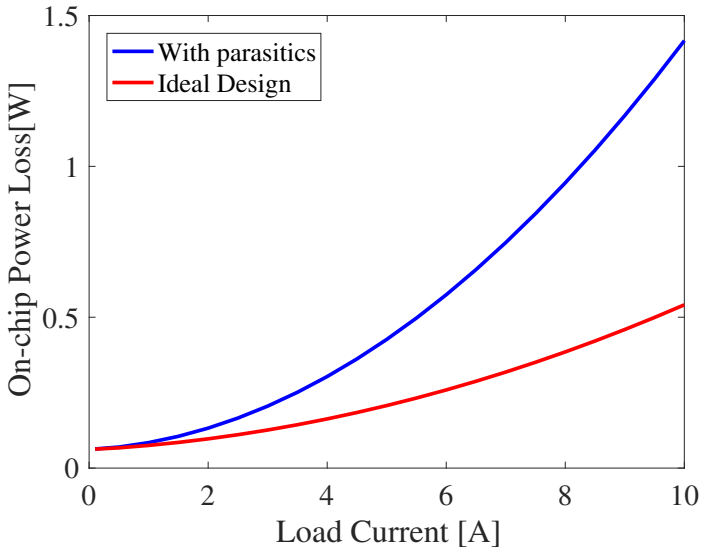
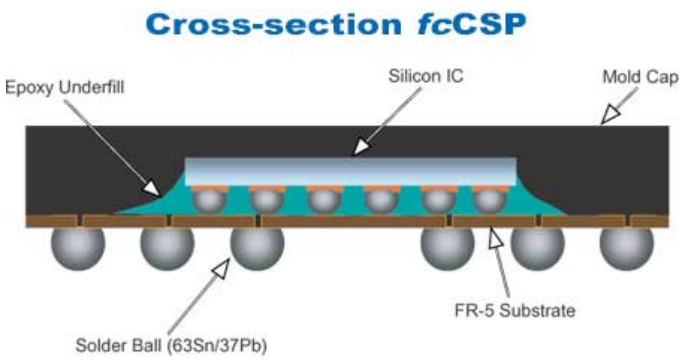
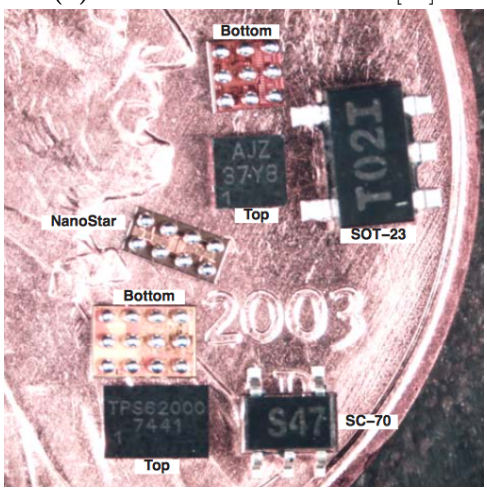


Figure 4.21: Increased losses due to bondwires.

technique to connect the die to the package. In the designs explored so far, the die is attached face up and connections are made through bondwires. Due to the high length-width ratio, additional resistance and inductance is added to the connections off-chip. On flip chip packaging, the die is populated with solder bumps on connection pads. Then, the bumped die is flipped over and placed down, so connections are made directly to the container package that will be soldered to the PCB [54]. Figure 4.22a shows a cross section of a flip chip CSP (Chip Scale Package). In this type of flip chip packaging, die bumps are routed inside the package to the solder bumps that are connected to the board. For a high current application, this is not suitable. Wafer Level Chip Scale Package is a flip chip technology that doesn't add any interface between the die and the PCB, the bumped die is directly soldered to the board. Figure 4.22b shows a WLCSP device. This package is the smallest possible form factor for an integrated circuit as the package is the dimension of the die itself [55]. However, this technology requires bumping the devices at wafer level before the dicing. For this project, dedicated wafers were not available for WLCSP. However, the advantage of the top thick copper metal layer exposed can be used to create a custom flip chip solution for the Buck converter analyzed in Section 4.2 with $R_{on1} = 3.5\,\mathrm{m\Omega}$ and $R_{on2} = 4.75\,\mathrm{m\Omega}$ for the high-side and low-side switch respectively. As a consequence, with no bondwires, the only parasitics are the metallization resistance and the solder joint resistance.



(a) Cross section of a fcCSP [54]



(b) Wafer Level Chip Scale Package [55]

Figure 4.22: Flip chip packaging technologies

4.3.1 Gate driver

A fully integrated gate driver is designed and implemented to drive the power switches. A gate driver is essentially a chain of inverters (buffer), driving a capacitive load (LDMOS gate). The buffer is built with N inverters in series, scaled with respect to the previous one by a factor f in order to reduce the propagation delay which can be calculated as [56]

$$t_p = N t_{p0}(1 + \frac{\sqrt[N]{F}}{\gamma}) \tag{4.6}$$

where t_{p0} is the delay of the minimum size inverter (the first stage) loaded by its own intrinsic capacitance, F is the effective fanout of the buffer $C_L/C_{g,1}$, with $C_{g,1}$ the input capacitance of the first inverter and γ is a technology factor that is close to 1. The optimum number of stages and scale factor is found by solving for the minimum propagation delay using numeric iteration as there is no closed form for $\delta t_p/\delta N = 0$. However, for a gate driver design, it is important to size the last stage in order to obtain the desired turn on and turn off resistances for the main power MOSFETs. Thus, the load capacitance of the buffer C_L, is the input capacitance of the last stage rather.

Gate charge losses are modeled considering the power MOSFET's gate charge and its driving voltage. However, this is only valid if gate driver losses are much smaller than P_{gate}. There are two types of losses in the buffer. Dynamic losses are produced by the charge and discharge of the intermediate gate capacitance of each stage in the chain. The other loss mechanism is related to the direct current path between the supply voltage and ground originated by

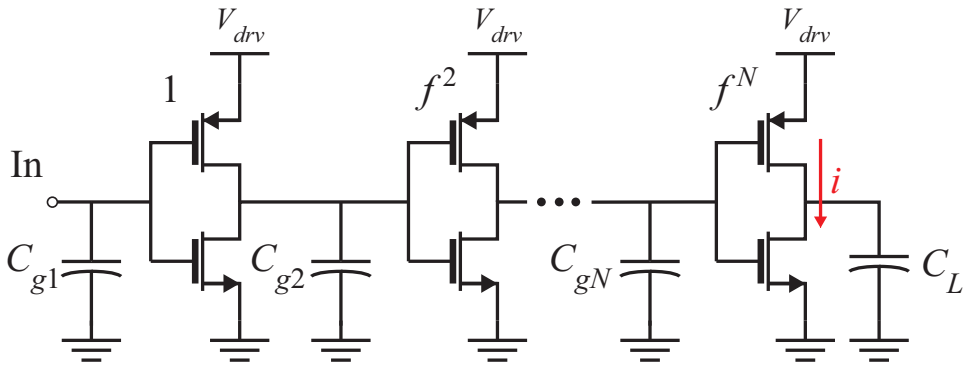
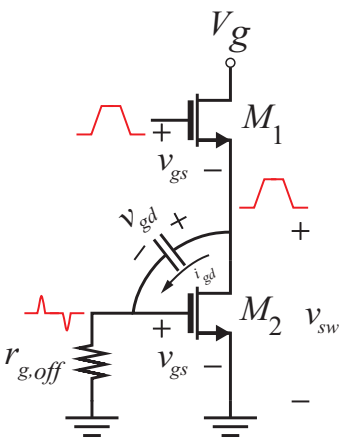


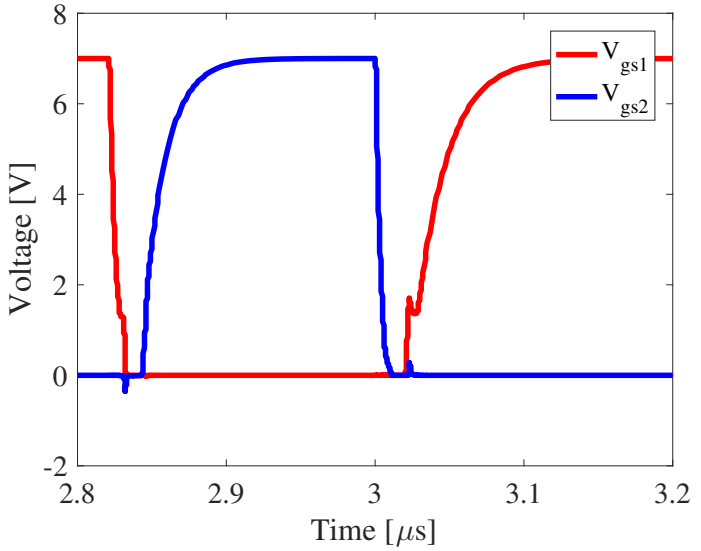
Figure 4.23: Inverter chain driving a capacitive load.

the simultaneous conduction of the PMOS and NMOS during the inverter's transition. As the size of the inverters scale up in the chain, the shoot-through current becomes larger. This is specially critical for the last stage of the gate driver as it is related with the turn on and turn off speed of the switches as it is explained in Section 3.1.1. By increasing the size of the power stage LDMOS to reduce its on-resistance, its total gate charge also increases. Thus, in order to reduce the turn on/off times, the driving resistances, i.e. the size of the last inverter in the chain, have to be sized appropriately. As a consequence it is desirable to drive the PMOS and the NMOS separately to prevent direct current flow.

The value of the turn on and turn off resistance not only depend on the desired driving speed of the power MOSFETs; high values of driver's resistance can degrade conduction loss by reducing the time during which the power MOSFET is fully turned on with its designed on-resistance value conducting the load current. On the other hand, excessively low driving resistance speeds up the switching node transition producing a high dv/dt on the low side gate-drain capacitance generating a current flow to the gate (Figure 4.29). This current will create a positive v_{gs} on M_2 and if its magnitude is big enough or if the off resistance of the gate driver is not low enough, the low side device can potentially turn on causing cross talk. This will cause extra losses to the converter as M_1 is already turned on. More over,



(a) Cross talk produced by fast turn on (off) of the high-side device.



(b) Simulated cross talk with a turn on resistance of 20 Ω

Figure 4.24: Cross talk produced by fast turn on (off) of the high-side device.

depending on the magnitude of the bump on the low-side's v_{gs}, it could be a destructive event if sufficient current flows from V_g to GND through the power stage. A similar effect occurs when the high-side device turns off. In this case, a negative v_{gs} will be generated. This will not create a shoot-through current on the power stage, but it increases the source drain voltage of the PMOS driver of the low side device. In Figure 4.25 the driver on resistance for the high side is swept for two different values of the off resistance, 300 mΩ and 700 mΩ, while the power stage has an input voltage of 5 V and an output current of 5 A. The peak value induced by the high dv/dt, increases as the turn on strength is higher. With a lower turn off resistance the curve is shifted down and can mitigate this effect.

The designed gate driver schematic is shown in Figure 4.26. It consists of a separate driving last stage, a non-shoot-through logic. As it is explained, a low turn off resistance is desirable to prevent cross talk on the power stage, while an excessively low turn off resistance can damage the PMOS of the gate driver. Therefore, a pull-down NMOS transistor is added to the gate driver to increase the turn off strength once the power stage LDMOS is turned off. To reuse the same design for the high-side device, all NMOS transistors (including those in inverters and gates) are isolated. Thus, the body terminal of the NMOS devices are connected to their source terminals preventing an increase of the threshold voltage, which will increase the turn off resistance. The signals for the PMOS and NMOS are generated through a

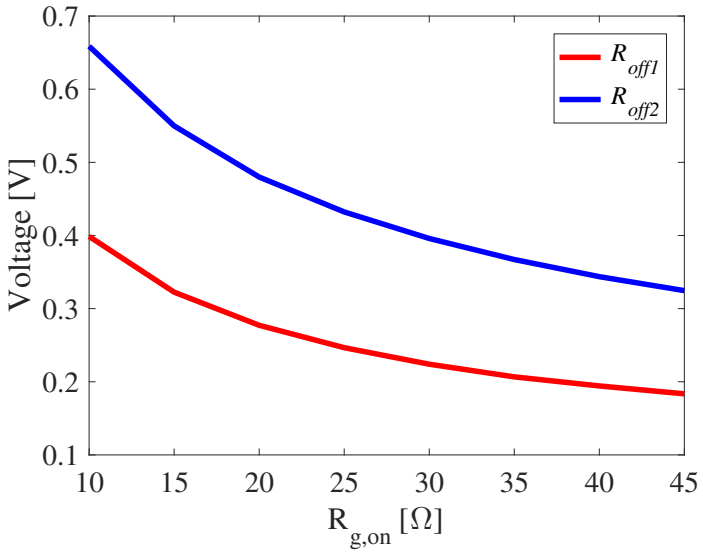


Figure 4.25: Peak v_{gs} on the low-side due to fast turn on off the high-side device

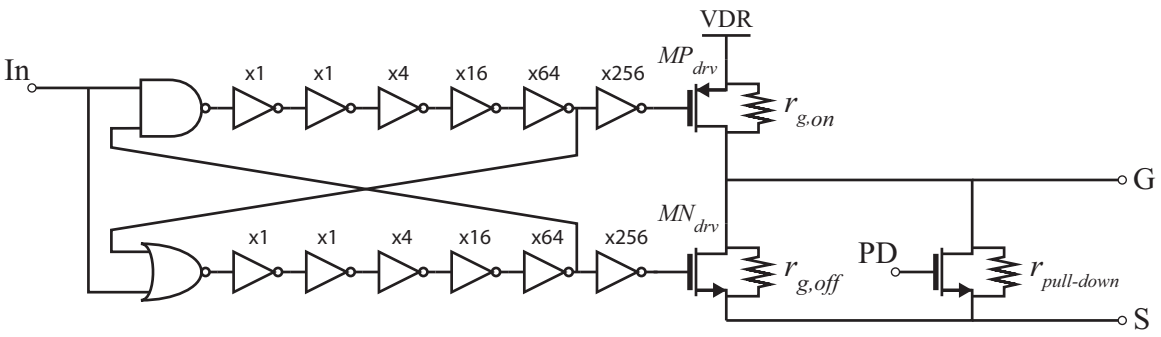


Figure 4.26: Gate driver with non-shoot-through last stage and pull down to further reduce the off resistance.

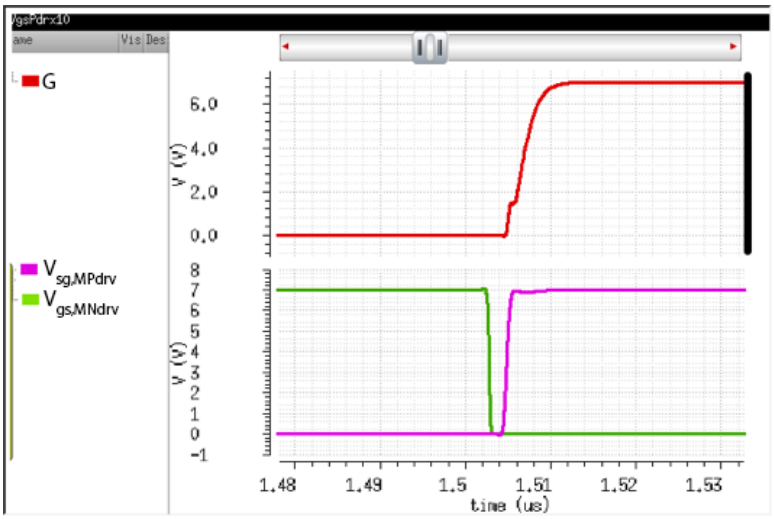
combination of the input and an intermediate signal of the buffers. As the second signal will have a delay, it will prevent M_{drp} and M_{drn} from conducting at the same time. The buffers are sized using the gate capacitance of the PMOS as the load according to Equation 4.6, which results in 5 stages with a scale factor of 4. Table 4.4 shows the sizing parameters of the design. The values of $R_{g,on}$, $R_{g,off}$ and $R_{pull-down}$ are selected by simulation, preventing cross talk on the power stage and excessive v_{sd} on the PMOS device of the gate driver. Figure 4.27 shows simulated performance of the gate driver driving a LDMOS of 3.5 mΩ on-resistance. Figure 4.27a shows the v_{gs} of the LDMOS and the v_{gs} and v_{sg} of the NMOS and PMOS transistors of the last stage. A corner simulation is used to check that enough delay is achieved for the feedback signals over process variations. In Figure 4.27b, the results are shown where no overlap occurs for any of the simulated cases.

4.3.2 Layout

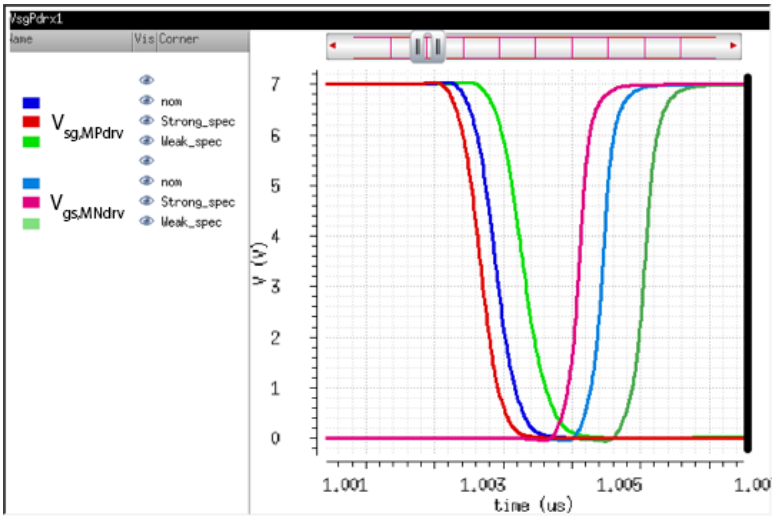
The same principles described in Section 4.2 to improve current distribution on the metal layer are used to implement the flip chip Buck converter. Figure 4.28a shows the top level layout view. The on-resistance for the high-side and the low-side MOSFETs is sized to 3.5 mΩ and 4.75 mΩ respectively. Connection to V_{in}, gnd and V_{sw} are extended to increase the solder area. Signal pads for the gate driver voltage, gate driver input, pull-down and power MOSFET gate are 300 µm x 500 µm. The gate driver layout used for both LDMOS is shown in Figure 4.28. The layout is symmetrical, both on the logic and the pull-down. The gate driver is placed at the center of the power MOSFET to equalize the gate path along

Table 4.4: Gate driver parameters

Parameter	Value
$r_{g,on}$	3.5 Ω
$r_{g,off}$	2 Ω
$r_{pull-down}$	160 mΩ
$(W_n/L_n)_{1-\text{stage}}$	2
$(W_p/L_p)_{1-\text{stage}}$	7

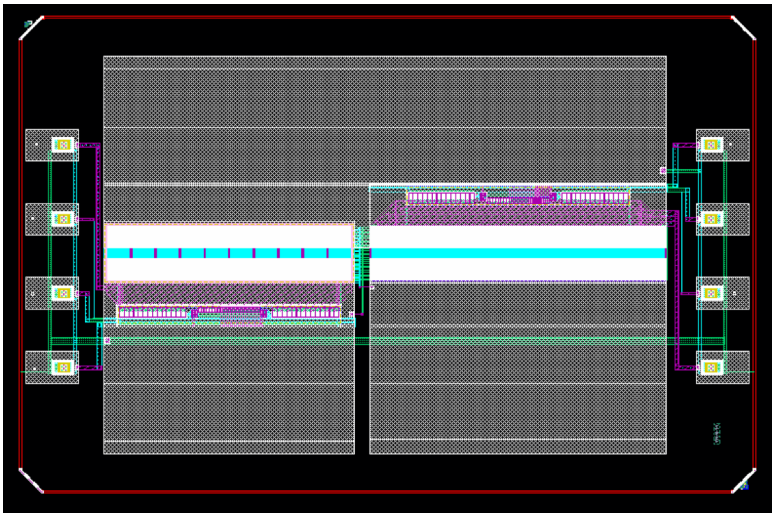


(a) Gate signal.

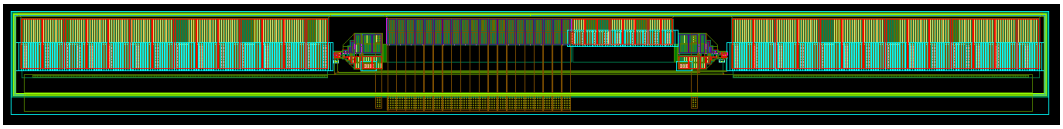


(b) Corner simulations of the non overlapping action. PMOS and NMOS v_{gs} signals.

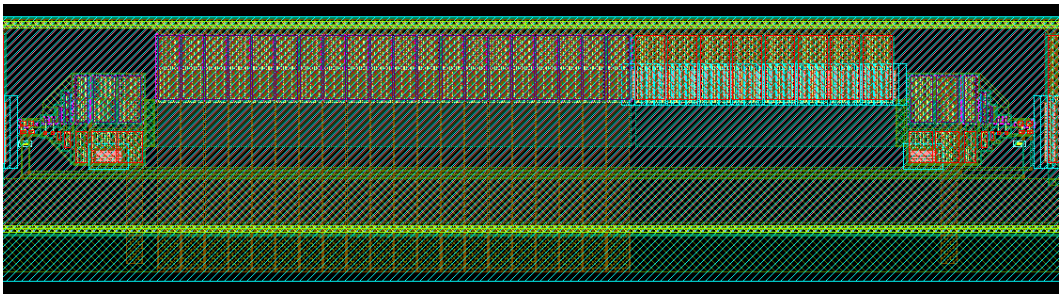
Figure 4.27: Gate driver simulation waveforms.



(a) Top level layout



(b) Gate driver and pull-down layout



(c) Gate driver layout. Non-overlap

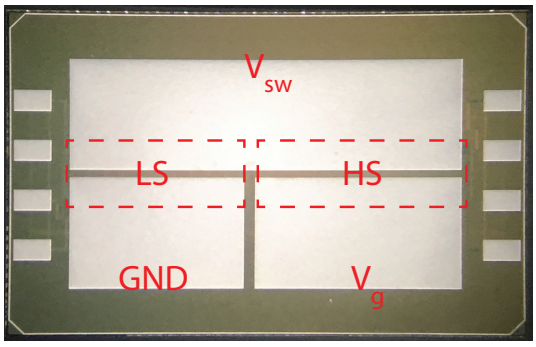
Figure 4.28: Gate driver layout.

the structure. Thus, the last stage of the driver is placed on the center as can be shown in Figure 4.28c. Each buffer is placed on the side of its driving MOSFET to equalize the path of the feedback signals needed for the non-overlapping logic.

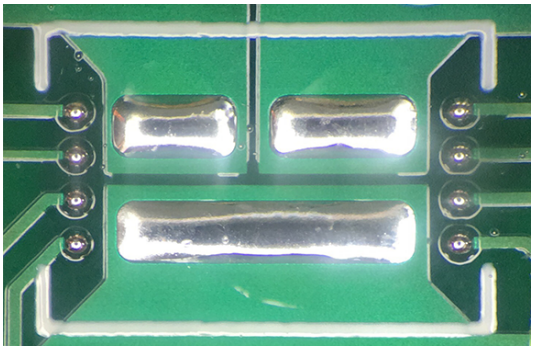
A picture of the fabricated IC is shown in Figure 4.29a. A commercial flip-chip package, like the ones mentioned in Section 4.3, will be bumped with solder balls to facilitate the integration of the device to the PCB board. In addition, there will be a passivation layer over the entire surface of the IC with openings on the pads to prevent that the solder balls extend beyond the pad. In this implementation the IC is not bumped. Instead, the bumping is made on the PCB board using the solder mask. Figure 4.29b shows the bumped footprint used to solder the Buck converter.

4.3.3 Loss measurement

In order to test this design, a mother-board with 4 isolated channels is designed (Figure 4.30). Each channel consists of an isolated DCDC, a 7 V regulator for the gate drivers and a 3-channel digital isolator. The input signals for each channel are fed from a FPGA with a time resolution on 3.33 ns. The PCB designed to test the flip chip Buck converter is shown in Figure 4.31. To drive the pull-down NMOS, dedicated gate drivers are included in the test board. The input and output voltage are measured by kelvin connections at the input and output ports. The inductance value is 1 µH. Figure 4.32 shows the operating waveforms of the implemented flip-chip Buck converter. In order to measure the on-chip losses, parasitic



(a) Picture of the solder side of the flip-chip Buck converter.



(b) Bumped PCB footprint used to solder the custom flip-chip Buck converter.

Figure 4.29: Implemented custom flip chip Buck converter.

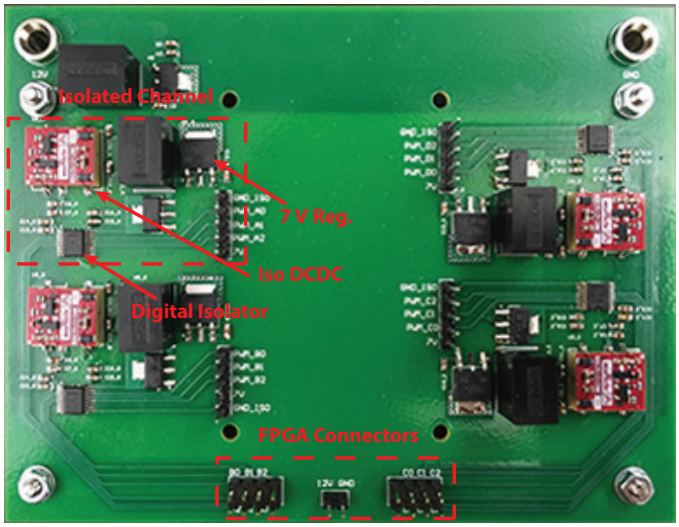


Figure 4.30: Motherboard with 4 isolated channels.

resistances from the switching node to the output and between the PGND output connector to the PGND of the flip chip were measured to estimate their loss contribution and subtract its value from the overall loss measurement. In addition, resistances in the current path, R_{par1} and R_{par2} (Figure 4.9), are also measured to include in the analytical model. These resistances are composed of

$$R_{par1} = R_{pcb1} + R_{met1} + R_{on1} \tag{4.7}$$

$$R_{par2} = R_{pcb2} + R_{met2} + R_{on2} \tag{4.8}$$

Table 4.5 summarizes the measured values. Even though these values are lower than the resistances predicted in Section 4.2, they are still not negligible. Possible reasons for this can be the solder joints and the metallization structure, taking into account the via stack and the uneven flow of current distribution through the MOSFET fingers. Figure 4.33 shows the top view of a single finger.

There are different paths for the current to flow with different resistances. However, those inside the red box represent the lowest resistance paths. With a bigger portion of the finger current flowing through this path, the effective on-resistance can be larger than designed. The result loss measurement for the flip chip Buck converter is shown in Figure 4.34.

To contrast the test results, the model of Table 4.1 is used adding the measured parasitic

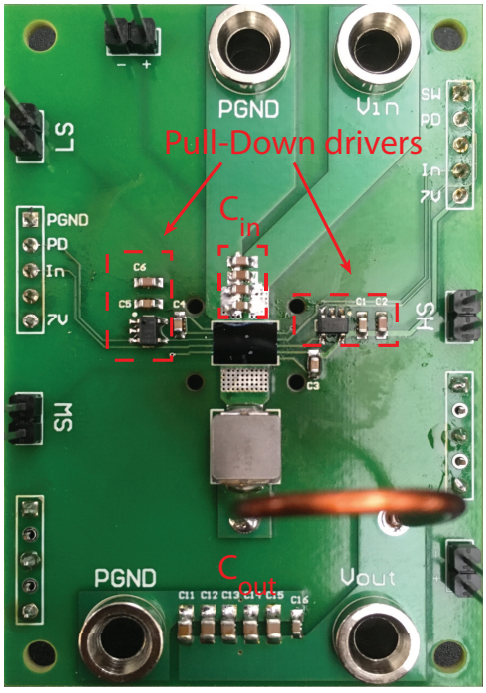


Figure 4.31: Flip chip Buck converter test board.

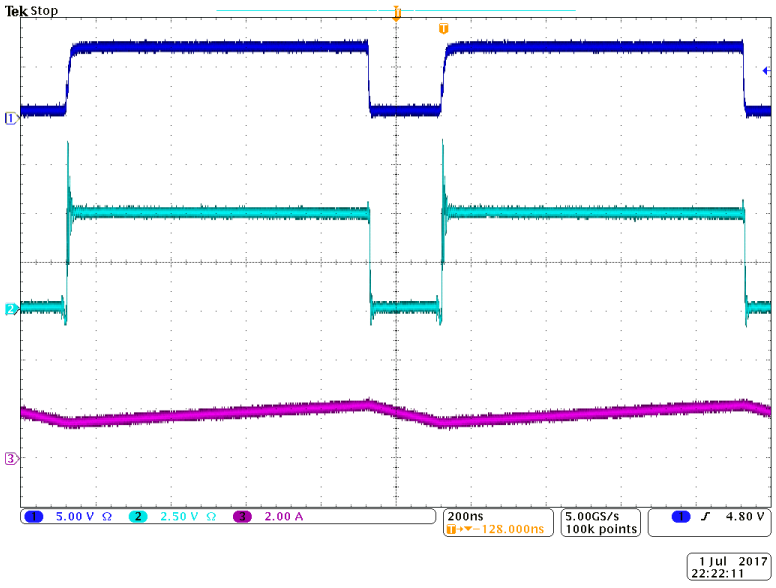


Figure 4.32: Flip chip Buck waveforms. CH1: $v_{gs,1}$ - CH2: v_{sw} - CH3: i_L

Table 4.5: Measured parasitic resistances for the flip chip Buck converter

Parameter	Measured
R_{par1}	7 mΩ
R_{par2}	8.5 mΩ

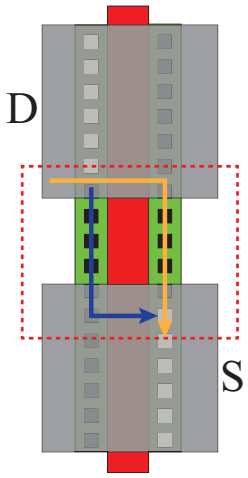


Figure 4.33: Current flow through a MOSFET's finger

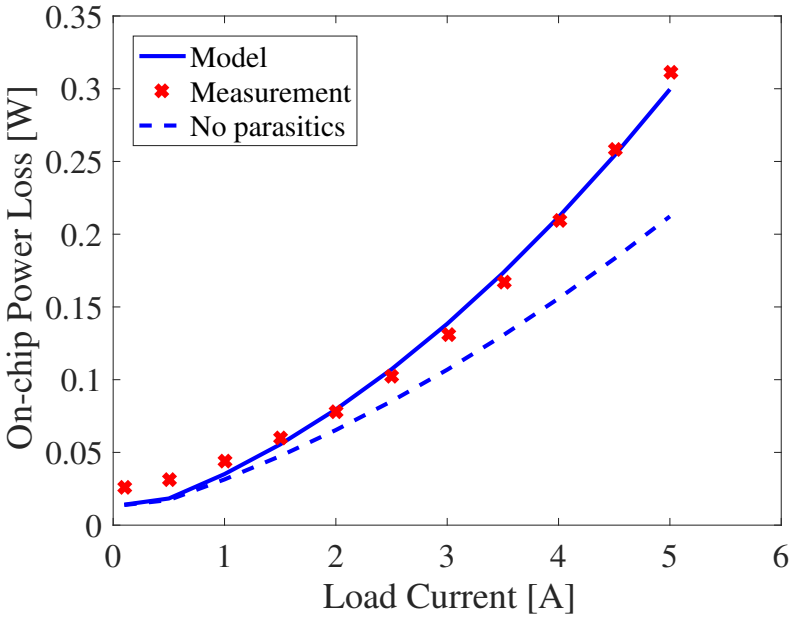


Figure 4.34: Loss measurement and analytical model for the flip chip Buck converter.

resistances. Using the results from the analytic model, an estimated loss breakdown is shown in Figure 4.35. Switching losses represent a considerable portion of the total losses due to the size of the devices. As the on-resistance is reduced, switching losses become a considerable factor, even at high currents.

4.4 3-Level Buck

The 3-Level Buck converter can exhibit lower switching losses than the Buck converter as the blocking voltage of each device is half the input voltage and it can be operated at lower frequency than a Buck converter while keeping the same current ripple if the same inductance is used. To evaluate the performance, a 3-Level Buck is constructed by connecting two flip-chip half-bridges in series from the previous Buck design. Figure 4.36 shows the implemented 3-Level Buck. The flying capacitor is comprised of three 10 µF capacitors in parallel with a 2.2 µF and 100 nF capacitor. The inductor is the same as used for the flip-chip Buck converter and the operating frequency is 500 kHz. In order to model the losses on the converter and to compare with measurements, the resistances in all the current paths are measured. Figure 4.36b shows a schematic of the 3-Level Buck converter with the parasitic resistances. For a 5 V to 4 V conversion ratio, from Figure 3.10b the following resistances will conduct

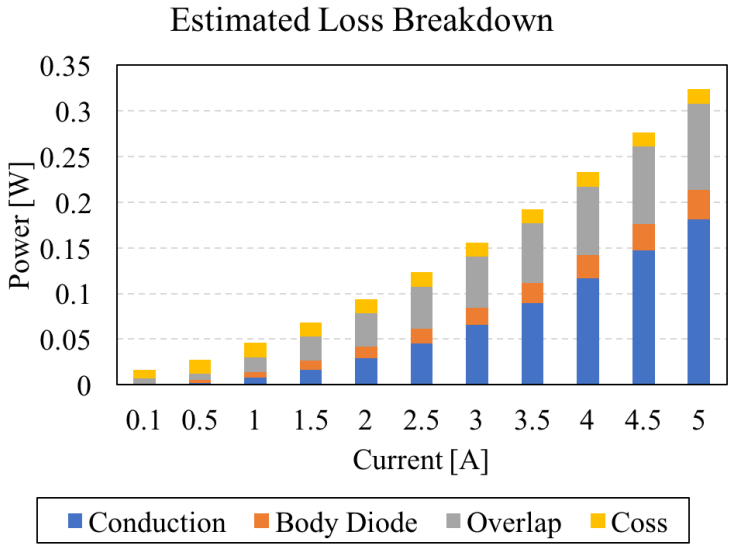
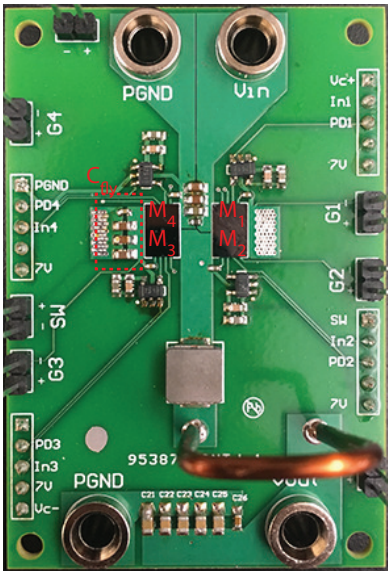
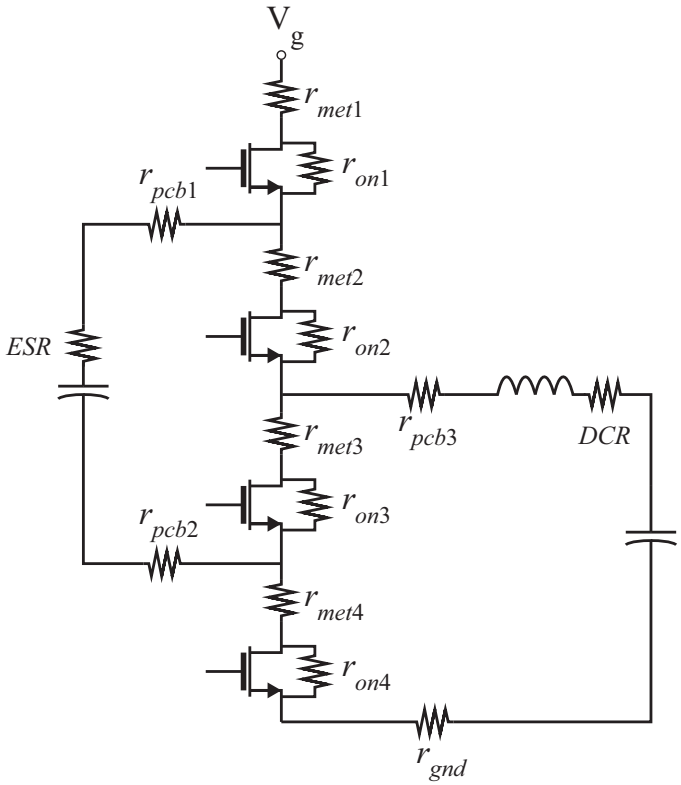


Figure 4.35: Estimated loss breakdown for the flip-chip Buck converter



(a) 3-Level Buck converter using two half bridges in series



(b) Parasitic resistances involved in the 3-Level Buck.

Figure 4.36: Implemented custom flip chip 3-Level Buck converter.

the load current on each phase (Table 4.6). Resistance $r_{met,i}$ includes the metallization and solder joint for the flip-chip interface. To calculate the ESR of the flying capacitor stack, the parallel network with the data provided by the manufacturer is computed. The resistance $r_{pcb3} + DCR + r_{gnd}$ is also measured in order to compute on-chip losses from measurements. Figure 4.37 shows the waveforms for the implemented converter operating at V_g =5 V, V_{out} =4 V, f_s =500 kHz and i_L =1 A. It can be noticed that there is a mismatch on the flying capacitor voltage during Phase II and Phase IV. The flying capacitor is charged and discharged by the load current. Thus, proper timing is needed to maintain its voltage at $0.5V_g$. As the test is run at open loop, this timing is tuned at each load current with a maximum resolution of 3.3 ns.

4.4.1 Loss measurement

A comparison between measured on-chip losses and the analytical model is shown in Figure 4.38a. The constructed model tracks the test results with sufficient accuracy. Compared with the losses measured for the Buck converter in Figure 4.34, total on-chip losses are almost doubled. This is expected, as predicted by analysis in Section 3.4. The 3-Level Buck converter only has lower losses than the Buck converter at large power stage areas, where conduction losses are much smaller than switching losses. However, the breaking area point is dependent on the specific technology parameters and the devices that are used. An estimated loss breakdown based on the analytical model is shown in Figure 4.38b. Compared with the breakdown calculated for the Buck converter in Figure 4.35, it can

Table 4.6: Resistances involved in each phase for the implemented 3-Level Buck for D >0.5 operation.

Phase	Devices	Total resistance	Value [mΩ]
I	M_1-M_2	$r_{met1} + r_{on1} + r_{met2} + r_{on2}$	18.6
II	M_1-M_3	$r_{met1} + r_{on1} + r_{pcb1} + ESR + r_{pcb2} + r_{on3} + r_{met3}$	20
III	M_1-M_2	$r_{met1} + r_{on1} + r_{met2} + r_{on2}$	18.6
IV	M_2-M_4	$r_{on4} + r_{met4} + r_{pcb2} + ESR + r_{pcb1} + r_{met2} + r_{on2}$	25

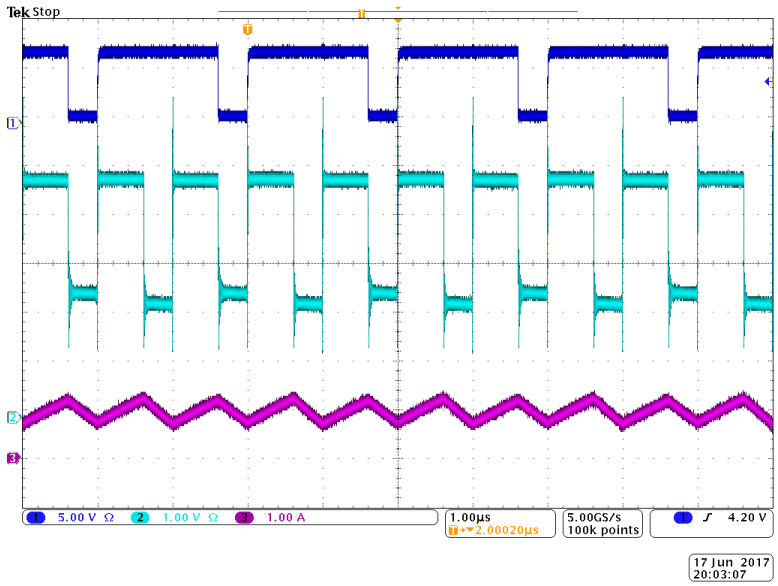
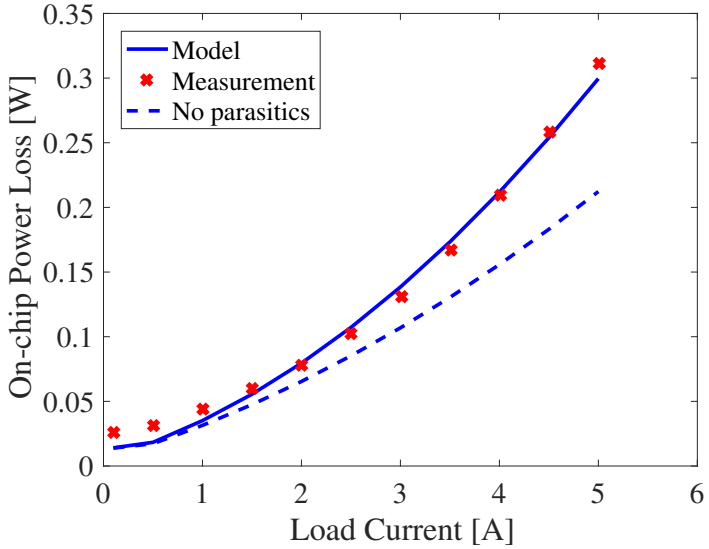


Figure 4.37: Operating waveforms for the 3-Level Buck converter. CH1: v_{gs1} - CH2: v_{Cfly} - CH3: i_L

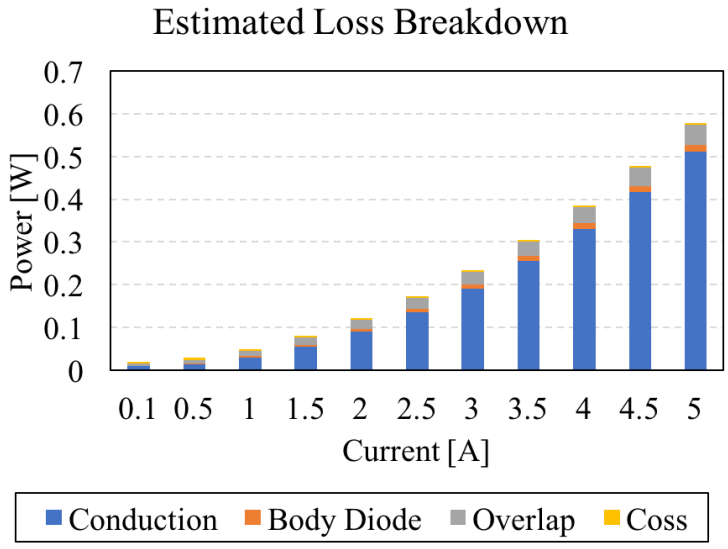
be seen that switching losses are reduced over the entire load current sweep, showing the important characteristic of the 3-Level Buck converter.

4.5 Hybrid Buck

A Hybrid Buck converter is built using the available custom flip-chip half bridges of Section 4.3. The half bridges were connected in series as is done for the 3-Level Buck, and the low side device of the lower half bridge is shorted circuited. There are two power loops that must be minimized, one between M_1 and M_2 and the other between M_2 and M_3. Figure 4.39 shows the schematic with these power loops highlighted. The first power loop is decoupled by the flying capacitor. While the second loop is decoupled by the output capacitor bank. As in the case of a Boost converter, it is important to add high frequency capacitors to obtain low impedance at high frequency. The implemented Hybrid Buck converter is shown in Figure 4.40. The decoupling capacitors are reversed geometry 0508 package, providing low inductance and low ESR to the power loops. The inductor is 1 µH, the flying capacitor is 10 µF and the output capacitor bank is 100 µF. The converter is tested at 6 V input voltage, 4 V output voltage at 1 MHz switching frequency. Figure 4.41 shows the operating



(a) Comparison between the loss model and test results for the 3-Level Buck converter.



(b) Estimated loss breakdown for the 3-Level Buck converter.

Figure 4.38: On-Chip losses for the 3-Level Buck converter.

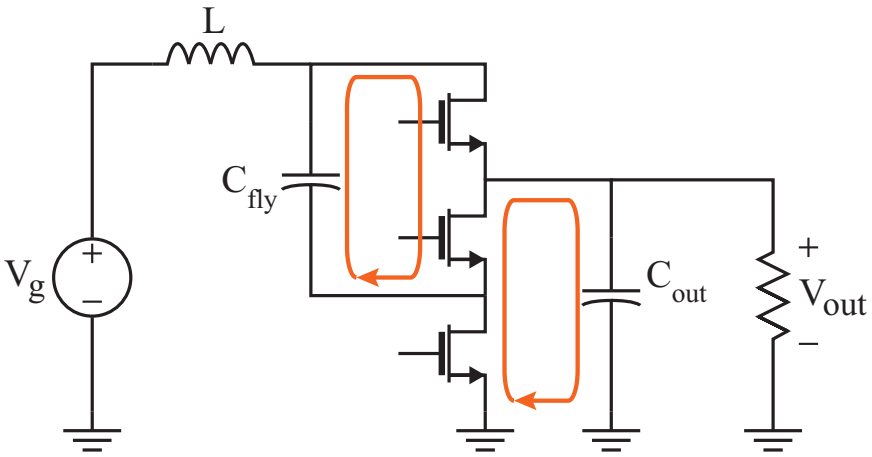


Figure 4.39: Power loops involved in the Hybrid Buck converter

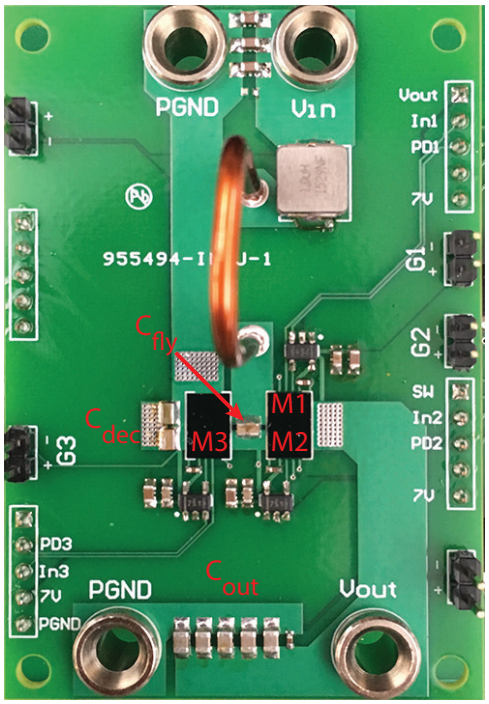


Figure 4.40: Implemented Hybrid Buck converter PCB board

waveforms of the implemented Hybrid Buck converter. It can be seen that the flying capacitor is charged to the output voltage, 4 V. The load current at which this waveform is captured is 2 A. Channel 3 shows the inductor current, which has an average value of approximately 1.3 A that corresponds to

$$I_L = \frac{I_{\text{out}}}{2 - D} \tag{4.9}$$

It is of interest to explore another characteristic of this converter: the charge sharing process. As is explained in Section 3.3, that when M_1 turns on, due to the charging of the flying capacitor during interval II, a voltage mismatch occurs giving place to a charge redistribution of the flying capacitor. Figure 4.42 shows the capacitor voltage with DC rejection. When M_1 is off, the voltage on the capacitor increases linearly. At the time M_1 turns on, there is an exponential decay that ends at the DC component, V_{out}.

4.5.1 Loss measurement

The resistances involved in the current path are shown in the schematic in Figure 4.43 Table 4.7 shows the resistances involved in each interval for the Hybrid Buck converter. Also $DCR + r_{pcb1} + r_{pcb3} + r_{gnd}$ is measured to calculate on-chip losses from measurements. Losses

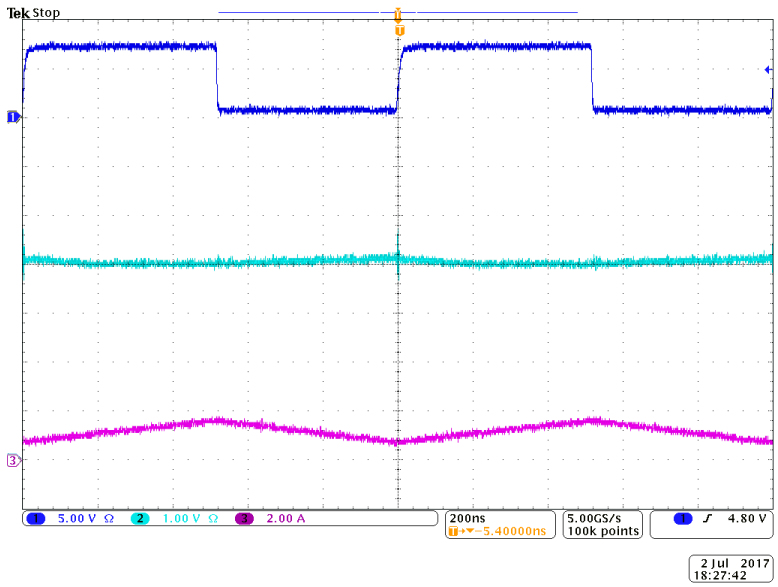


Figure 4.41: Hybrid Buck converter waveforms. CH1: v_{gs1} - CH2: v_{fly} - CH3: i_L

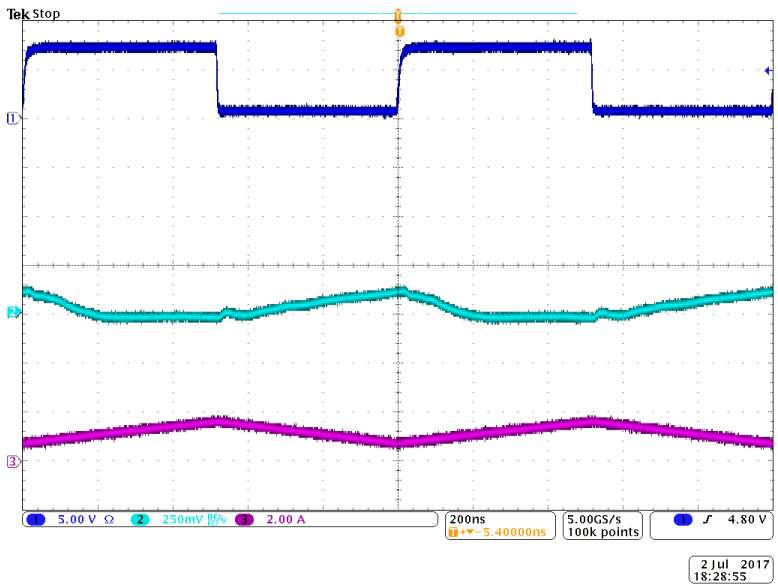


Figure 4.42: Hybrid Buck converter charge sharing process. CH1: v_{gs1} - CH2: v_{fly} (DC Rej.) - CH3: i_L

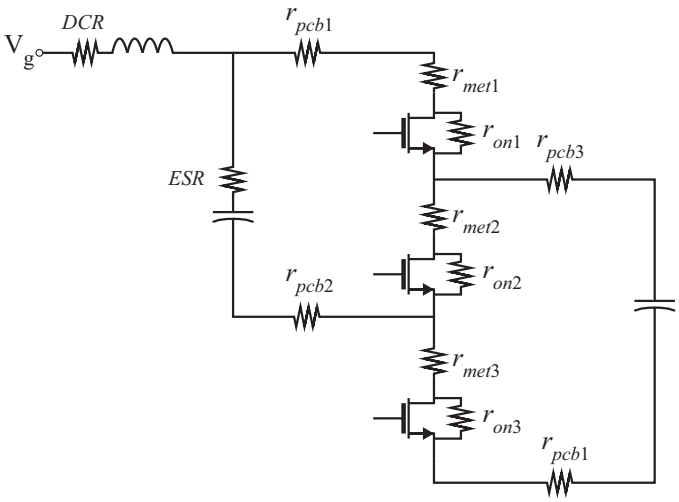


Figure 4.43: Parasitic resistances involved in the Hybrid Buck converter operation

Table 4.7: Resistances involved in each phase for the implemented Hybrid Buck converter.

Phase	Devices	Total resistance	Value [mΩ]
I	M_1	$r_{pcb1} + r_{met1} + r_{on1}$	5.4
	M_3	$ESR + r_{pcb2} + r_{met3} + r_{on3}$	11
II	M_2	$ESR + r_{pcb2} + r_{on2} + r_{met2}$	9.5

on the Hybrid Buck converter have a strong dependence on the charge sharing processes. A decreased value on the flying capacitor will create a larger ΔV during phase II, increasing the current on M_1 and M_3. Capacitance tolerance, DC bias and temperature can shift the effective value of a ceramic capacitor. The one that is used for this implementation has the parameters showed in Table 4.8. Taking these variations into consideration and including the parasitic resistances of Table 4.7 into the analytic model developed in Section 3.3, an on-chip loss comparison with test results is performed in Figure 4.44 for a 6 V to 4 V Hybrid Buck converter. Compared with measured losses for the Buck converter and the 3-Level Buck converter, these results are not encouraging. However, as it is explained, optimizing the FET area in the Hybrid Buck converter can reduce on-chip losses. Moreover, inductor loss is reduced in this converter. Then, a smaller size inductor with a higher DCR can be used achieving a smaller footprint for the converter.

4.6 Summary

In this chapter the analytical models constructed in Chapter 3 are validated with experimental results. The effect of bondwire, packaging and metallization of the power stage is analyzed. For a high-current integrated converter, bondwire can be a limitation on the maximum on-chip power loss. Flip-chip packaging can overcome this limitation. However, metallization and current distribution on the power MOSFETs can establish a practical limit when the on-resistance is taken to single digit mΩ values. The Hybrid Buck converter presented in Section 3.3 is fabricated and tested, validating the analytical model. It is shown how important is to optimize the on-resistances of the switches to overcome the charge sharing process.

Table 4.8: Capacitance tolerance value and shift due to DC bias.

Process	Variance [%]
Tolerance	+/-20
DC Bias (4 V)	-40

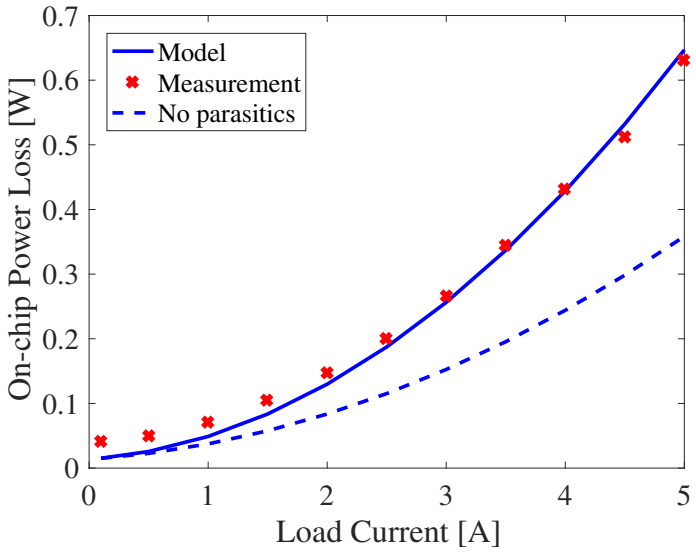


Figure 4.44: Loss comparison for the Hybrid Buck converter

Validated models accurately predicted the behavior of the three converters, forming a basis for further design comparison.

Chapter 5

Conclusions and future work

Bondwires sets a limit on the on-chip losses for a high current integrated converter. As the maximum load current for a design increases, it is needed to move to a flip chip package in order to reduce parasitics. Eventhough, metallization resistance and solder joint resistance are non negligible for low on-resistances.

The 3-Level Buck only has lower losses than the Buck converter for total FET areas where parasitics dominate the losses of the converter. For a low voltage application, the Hybrid Buck converter has lower losses than the Buck and the 3-Level Buck, even at small areas. As the input voltage increase, charge sharing losses become dominant and increase the total losses of the Hybrid Buck converter. However, the fact that the inductor is connected at the input port, decreases the total footprint of the converter as the inductor can be smaller by allowing a higher DCR.

Loss model validation through experimental results needs to be extended by comparing converters with different total FET area, different blocking voltage devices and with optimized sizing of the FETs.

Metallization resistance becomes dominant as the design on-resistance decreases. Current distribution from drain to source on large devices needs to be analyzed. Having a model for the impact of metallization will help to determine the maximum FET area that can be integrated before parasitics become larger than the desired on-resistance of the FETs.

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Vita

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