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Modeling and Control of Single Phase Grid-Tie Converters

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I am submitting herewith a thesis written by Bradford Christopher Trento entitled "Modeling and Control of Single Phase Grid-Tie Converters." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

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Modeling and Control of Single Phase Grid-Tie Converters

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Abstract

The penetration of renewable energy into the electric utility grid is growing worldwide. At the heart of these renewable sources is the power electronic systems used to convert the renewable source to an output that can be connected to the grid. In recent years, there has been a great deal of work in designing converters for grid-tie applications and is continuing to grow. With recent smart grid activities, it is not likely that this work will cease in the short term. Most of the recent research is in ancillary services that the converter can offer in addition to the normal energy transfer. With more advanced converters, the ability to provide reactive power and harmonic compensation has triggered many researchers to look at more advanced control schemes.

The work in this thesis focuses on modeling and control of single phase grid connected converters with an emphasis on grid interactions and ancillary services. While there has been a great deal of work in the modeling and control area for general converter operation, there has been little analysis in the converter's response to grid disturbances. There are very few resources that discuss the controller design as it relates to power quality. However, these are issues that must be considered in a real design and what separates the research and commercial level converters.

In addition to control and modeling work, the author suggests two new transformerless converter topologies for photovoltaic applications. In general, these converters can be viewed as a hybrid converter topology comprised of a two level and multilevel structure. Both converters show conducted emissions improvements over the standard commercial transformerless converters while also meeting leakage current requirements.

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Chapter 1.Introduction

1.1. Overview

The use of renewable energy has experienced a large growth in the last few years in the wind and solar area. For wind and solar systems, power electronics converters are at the heart of the conversion systems. With recent advances in power electronics, these renewable systems are now capable of supplying many ancillary services that traditional energy sources by themselves cannot. Some of the most notable services include [12]:

- Dynamic control of real and reactive power
- Voltage ride through
- Fault support
- Frequency control
- Harmonic compensation

Power electronic research in the wind and solar area is experiencing rapid growth, and with the recent smart grid activities will likely not slow down in the short term. While a great deal research has already been done in this area, there are still many areas that need more work and further development.

The work in this thesis focuses on modeling and control of single phase grid connected converters with an emphasis on grid interactions and ancillary services. While there has been a good deal of work in the modeling and control area for general converter operation, there has been little analysis in the converter's response to grid disturbances. There are very few resources that discuss the controller design as it relates to power quality. However, these are issues that must be considered in a real design and what separates research and commercial level converters. This thesis also addresses the steady state operating conditions for grid connected converters. For instance, chapter 4 is focused on leakage current and conducted emissions for transformerless connected converters. In solar installations, since there is a large amount of leakage capacitance, the emissions and leakage current are heavily affected by the renewable source. This has led researchers and manufacturers to look at different converter topologies and PWM schemes to minimize leakage current in transformerless connections. In the transformerless converter area, the author developed two new converter designs to meet leakage current requirements while also minimizing emissions.

1.2. Contributions

There has been a great deal of research in the last 10 years on leakage current in PV applications when using transformerless converter topologies. Most of the present work is focused on the converter topologies that can eliminate leakage current without the need for extra filtering. Unfortunately, in this area we are still missing a detailed study of how leakage current protection devices used in PV applications actually respond to high frequency leakage current. Most researchers in this area are using the rms current measurement and the rating of the protection device to evaluate their design. However, most leakage current being analyzed by researchers is outside the standards' operating frequency range, and studies like [23] show that the protection devices do not respond in the same way outside of this frequency range. One of the main contributions in this work was to reevaluate the standard full bridge topology and PWM schemes and try to correlate them to the protection standards used for residual protection devices. Using the surge standards, the author was able to show that one of the hybrid modulation schemes will most likely work for smaller PV systems as long as the cable connecting the converter and utility is not extremely long.

Using the results from the standard modulation schemes, a hybrid converter scheme was introduced that uses an active neutral point clamped phase leg and a traditional half bridge phase leg. A PWM scheme was designed for this converter based on the hybrid 1 PWM scheme for normal two level converters. As one would expect, this hybrid structure has lower emissions than its two level counterparts. After evaluating a few of the transformerless commercial products, a new converter called the H10 converter was introduced based on the hybrid active neural point clamped converter. Of course with a multilevel output, the emissions for this topology are less than the two level DC bypass designs, which also naturally result in smaller filtering.

On the controls side, the primary focus was on designing the system to work with various load and source configurations. In most work in this area, the interaction of the source and load with the converter is not addressed. This work was able to illustrate some of the worst case conditions for source and load configurations and show how to design the controls based around these conditions. Since there are different techniques for single phase dq transformation, the work also was able to illustrate how these techniques compare under various steady state and dynamic conditions.

1.3. Chapter Summaries

1.3.1. Chapter 2

The intent of chapter 2 is to give a brief overview of a few common techniques used for finding non-active power. Non-active power compensation is not the primary function of most grid-tie converters, so the compensation techniques in the chapter are compared in terms of ease of implementation and changes to the existing control structure. This chapter is not intended to be all-inclusive, but intended to illustrate a few of the common techniques. The techniques illustrated in this chapter can be divided into three categories: (1) those that provide instantaneous compensation; (2) those that provide compensation over an average interval; (3) those that can do any interval. In the later chapters, it will be assumed that these calculations do not impact the control system, so are of the instantaneous type; even though the results showed that the so called instantaneous results still took time to converge on the solution.

1.3.2. Chapter 3

In chapter 3, a few of the common single phase pulse width modulation techniques are discussed and compared. For all of the techniques, the vector and carrier implementation are illustrated with an example case. The vector approach for PWM is a much more elegant approach for the hybrid techniques because of the ease of dividing the switching times. After the vector analysis, it becomes apparent that the only difference between all of the discussed PWM techniques is how the timing is distributed within the switching cycle. From the timing diagrams for the hybrid methods, low frequency expressions for the duty cycles are found using Fourier analysis. The chapter also compares the different techniques in term of switching losses and differential and common mode noise.

The purpose of the chapter is to give an overview for the analysis needed in the subsequent chapters. In addition to standard topologies, chapter 4 also discusses a few of the commercial PV converters used in the field today. At the heart of the modulator for the commercial converters is one of the four techniques discussed in this chapter. Therefore, without an understanding of these techniques it is not possible to explain the commercial products. In chapter 5, filtering is discussed, so the harmonics and noise results of this chapter are also important for that analysis.

1.3.3. Chapter 4

The leakage current for the four modulation techniques discussed in chapter 3 are compared under symmetrical and asymmetrical filtering. For symmetrical filtering, only bipolar modulation is acceptable. For asymmetrical filtering, only the hybrid 1 approach is acceptable. The hybrid 1 modulation technique does however produce an oscillatory transient during polarity changes that limits its use. The oscillatory transient is a function of the utility cable impedance and array capacitance. The transient events are compared against the surge standards for leakage protection devices to try to determine whether the event would cause a nuisance trip for a residual protection device. For smaller grid-tie converters, the hybrid 1 modulation is compatible with residual current devices as long as the cable between the converter and utility is not extremely long.

The author introduced a new hybrid converter consisting of one phase leg in a two level structure and the other in a three level structure. This converter has lower noise than its two level counterparts and can also be used with the hybrid 1 modulation technique. A few of the commercially available transformerless converters are discussed to show how these products deal with leakage current. The author introduced a DC bypass converter based on the ANPC full bridge hybrid structure introduced earlier in the chapter. This has the advantages of the DC bypass circuitry found in commercial products and also has the lower switching ripple associated with a three level structure.

In addition to the leakage current, the conducted emissions of the different modulation and converter structures are compared. For PV applications, the hybrid 1 approach produces very low differential noise under asymmetrical filtering because of the modulation scheme and filter arrangement. The ANPC full bridge hybrid topology has half the differential noise under the same modulation sequencing because of the three level structure.

1.3.4. Chapter 5

In chapter 5, the dq and small signal models are developed for the single phase grid-tied converter. A few of the common techniques used for single phase dq transformations are discussed and compared. In the small signal analysis, the influence of the source and load impedance on stability is discussed. The filter design is addressed in this chapter using both the small signal model and switching model results of the previous chapter. The control system for the converter is designed to operate over a large range of source and load configurations using the small signal results. The average large signal model is used to validate the controller design over a large range of source and load conditions.

With the control system in place, the converter's response to voltage variations on DC side are compared for two of the dq transformation techniques. Since the quarter cycle delay approach results in lower gains and bandwidth, more of the signal passes through for this approach. However, both approaches have acceptable performance under low frequency DC variations. The dead time is also discussed in relation to the closed loop control. Although the distortion is fairly low, dead time compensation is still necessary for the converter in reactive power mode. Using the results from the small signal analysis, the converter response to voltage distortion and how it affects the converter current distortion was discussed for both the zero q-axis and quarter cycle delay approaches. Both converters have low current distortion under fairly distorted voltage waveforms. The control system's ability to provide harmonic compensation is also addressed in the chapter, which is directly related to the bandwidth of the controller.

1.3.5. Chapter 6

Sudden changes in voltage cause the current output of the converter to overshoot because of the filter frequency response being higher than the bandwidth of the controller. In order to prevent the current spike, if the voltage change is monitored and the real current is turned off before the filter has time to respond, then the current spike is minimized. An example case illustrated that two switching cycles is sufficient time to mitigate most of the current transient. An alternative would be to place the filter cut-off frequency lower than the crossover frequency of the control. The downside to this approach is that the filter will become larger than necessary. If no preventive action is taken in response to the voltage change, the converter will likely overload and shutdown during the event. There is also a risk that the damping resistor in the filter could be damaged because of the transient event. The control system has no problems with large inrush current events. A transformer inrush event is simulated to make sure the converter remains stable and does not overload because of the large energizing current. In conclusion, as long as the control system is able to minimize the current spike during voltage changes, the converter showed no other issues with power quality events.

Chapter 2.PQ Theories

Research into the calculation of non-active current started as early as 1930 [1] when Fryze introduced the concept of non-active power calculations in the time domain. Since then many different variations and techniques have been formulated to determine the non-active current under different loading and source configurations. Some methods work with periodic and non-periodic loading conditions and under non-sinusoidal conditions, while others are restricted to specific wiring configurations and sinusoidal conditions. For grid connected converters, the idea of compensating for the non-active current has been a research topic for many years and continues even in recent years. For compensation devices like STATCOMs and active filters, knowing the instantaneous non-active power is crucial to their operation since their sole purpose is to provide compensations for the non-active power.

For renewable and distributed energy systems, the concept of providing harmonic compensation and/or var support has been a hot topic in recent years because of recent smart grid activities. There has been much work among researchers and even some vendors to provide this type of compensation in grid connected converters. Europe and Asia have already adopted volt-var support in many of the commercial solar and wind converter systems. In the US, standards still prevent grid-tie converter from providing complete reactive power support, especially at the end use level. Since providing harmonic or var compensation is not the converter's primary purpose, these features do not have to be centered on this functionality; meaning that they do not need the fastest algorithms with the highest precision. In fact, the ideal solution is adding the capability to the existing platform with little changes. As a few of the different approaches are discussed, the reader should remember that the best approach for this type of application may not be the best technique available, but may be the one with the least amount of changes. In this chapter, an overview of a few of the techniques as well as their advantages and disadvantages will be discussed. Since in this work the focus is on single phase grid-tie converters, the use of the theory under this condition will be used for most of the example cases; although all of the theories presented are expandable to polyphase systems.

2.1. Fryze's Method

Fryze introduced the idea of calculating the non-active power for non-sinusoidal waveforms in the time domain as early as 1930 [1]. Since in the 1930s researchers did not have the tools to perform a Fourier analysis on the waveform, this was a very nice way of calculating the real and non-active power in the time domain. The approach is very simple and uses some basic power definitions, but is limited as will be shown shortly.

Fryze calculated the real current by determining the total conductance of the load, which he then multiplied by the instantaneous voltage. This relationship is given in (2-1). This requires only the real power and the rms voltage to be calculated from the voltage and current waveforms. For sinusoidal voltage conditions, this allows the real part of the current to be extracted from the waveforms. The main problem with the approach is the harmonics in the voltage waveform. In the calculation of the real power and rms voltage, the harmonics are included in the calculation, which means that the conductance will include the influence of the harmonics. When the voltage distortion is low and the power contributed by the harmonics is also low, this is not an issue for this method. To show how the harmonics influence the calculation, Table 2-1 shows the real and reactive power from a single phase rectifier load. The harmonic values in the table were obtained from a Fourier analysis. The voltage distortion caused by the current distortion was about 2.5% at the point of common coupling. The table illustrates that the power contribution from the harmonics is low even with a fairly distorted voltage.

$$i_r(t) = \frac{P}{V_{rms}^2} \cdot v(t) \tag{2-1}$$

Table 2-1: Harmonic real and reactive power for single phase diode bridge

Harmonic	Real Power	Reactive Power
1	8677.4	271.47
2	0	0
3	1.3	90.43
4	0	0
5	0.8	-75.72
6	0	0
7	0.4	-33.06
8	0	0
9	0.1	-6.08
10	0	0
11	-0.1	-1.04
12	0	0
13	-0.2	-2.10
14	0	0
15	-0.01	-1.26

It is clear from (2-1) that if the voltage is distorted that the real current calculation will have the same distortion scaled by the conductance. From the Fourier coefficients for the voltage and current, the conductance can be calculated at each of the frequencies, which is shown in Figure 2-1. The fundametal frequency is the most important since the power contributiion from the harmonics are low. The negative conductance means that the angle between the voltage and current is greater than 180°. Using Fryze's method the conductance of the waveform is 0.6370 S and with the Fourier series it is 0.6374 S, concluding that there is very little difference between the approaches even under non-sinusoidal condtions with moderate voltage disotortion. If the voltage distortion is low, which is typically the case, Fryze's method has very good agreement with the Fourier results. For the ideal case, meaning a sinusoidal voltage, Fryze's method produces the exact real current.

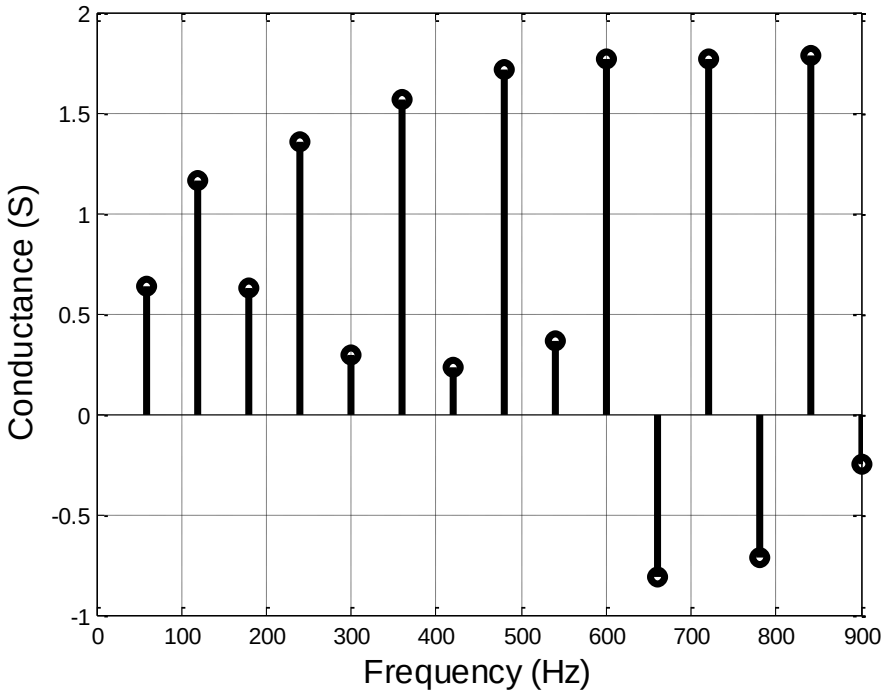


Figure 2-1: Frequency domain conductance for a single phase diode bridge

Since the converter needs the frequency to synchronize with the grid, the circuitry to determine the frequency should already be available in the converter. Therefore, calculating the real power and rms voltage to determine the conductance is easily added in the system with only a few additions. Most converters will already have the capability to calculate rms voltage and real power, so adding the real current calculation will probably require little addition to an existing system. The real issue with Fryze's approach is the integration procedures associated with the rms and real power calculation. These integration procedures become part of the control loop leading to smaller stability margins and slower response times. If the designer does not want to impact or redesign the existing control system, then the method needs to work instantaneously.

2.2. Generalized Non Active Power Theory

In [4-6], Xu et al. proposed a generalized non active power theory based on Fryze's approach but with a few subtle differences. First recognizing that the waveform may not be periodic or may contain interharmonics or subharmonics, averaging over the fundamental period does not necessarily generate the optimal non-active reference. The authors looked at different averaging intervals for different conditions. Also, proposed in the generalized non active power theory work is the idea of using a moving average for the power and rms calculations. From a control standpoint, this approach is better than Fryze's method because of the bandwidth constraint caused by integrating over a large time interval. Since the averages are being calculated, the authors proposed extracting the fundamental component of the voltage or using symmetrical components to extract the positive sequence value. Extracting the fundamental component can be done by calculating the first Fourier coefficients of the voltage. For three phase systems, the positive sequence voltage can be extracted using instantaneous symmetrical components. By extracting the fundamental or positive sequence fundamental value, the reference calculation can be forced to follow a sinusoidal reference even if the voltage is distorted. The bandwidth of the control system and margins of the control system will play an important role in the compensation capability, which will be discussed in a later chapter.

$$i_r(t) = \frac{P}{V_p^2} \cdot v(t) \;\; ; \;\; V_p \; can\; be\; the\; rms,\; fundamental, or\; positive\; sequence \tag{2-2}$$

$$i_q = i - i_r \tag{2-3}$$

$$P = \frac{1}{T_c} \int_{t-Tc}^{t} i(\tau) \cdot v(\tau) d\tau \tag{2-4}$$

$$V_{RMS} = \sqrt{\frac{1}{T_c}\int_{t-Tc}^{t} v(\tau)\cdot v(\tau)d\tau} \tag{2-5}$$

2.3. Generalized Instantaneous Reactive Power Theory

In [2-3], Peng and Lai proposed a generalized instantaneous reactive power theory for three phase systems. The generalized theory is independent of the reference frame and works under balanced or unbalanced conditions with three and four wire utility configurations and under non-sinusoidal conditions. A few of the equations that the authors arrive at are listed in (2-6)- (2-10), which are proved in the work. The main contribution of this work is the elegance of placing the results in a vector format. It should be noted that the dot in the equation represents the dot product of the vectors.

$$p = \vec{v}\cdot\vec{i} \tag{2-6}$$

$$\vec{i}_r = \frac{\vec{p}}{\vec{v}\cdot\vec{v}}\cdot\vec{v} \tag{2-7}$$

$$\vec{i}_q = \vec{i} - \vec{i}_r = \frac{\vec{q}\times\vec{v}}{\vec{v}\cdot\vec{v}} \tag{2-8}$$

$$s = \|v\|\|i\| \tag{2-9}$$

$$\|x\| = \sqrt{x_a^2 + x_b^2 + x_c^2} \tag{2-10}$$

When looking at the results in abc coordinate systems, the similarities to Fryze's theory are obvious, but how the authors are able to remove the averaging from Fryze's equation is not clearly defined. This ability to remove the averaging lies in the use of the dot product, but as we will see cannot produce a truly instantaneous response. Unfortunately, the authors do not describe their implementation of the dot product in the work. For instance, the work alludes to this calculation being a truly instantaneous calculation; meaning that the calculations are done on a point by point basis and no information is used from the previous calculation. However if this is the case, then the conductance from the diode bridge example would look like Figure 2-2. Obviously this is not the conductance, since if this waveform is multiplied by the voltage, which has very low distortion, then so called real power producing current will basically look like a scaled version of this conductance. This means that authors are using information from the previous measurements. The question is then how much previous information are they using or do you need? It is clear that the summation will become large very quickly with a fast sampling time, so there needs to be some type of limitation and procedure to reset the system.

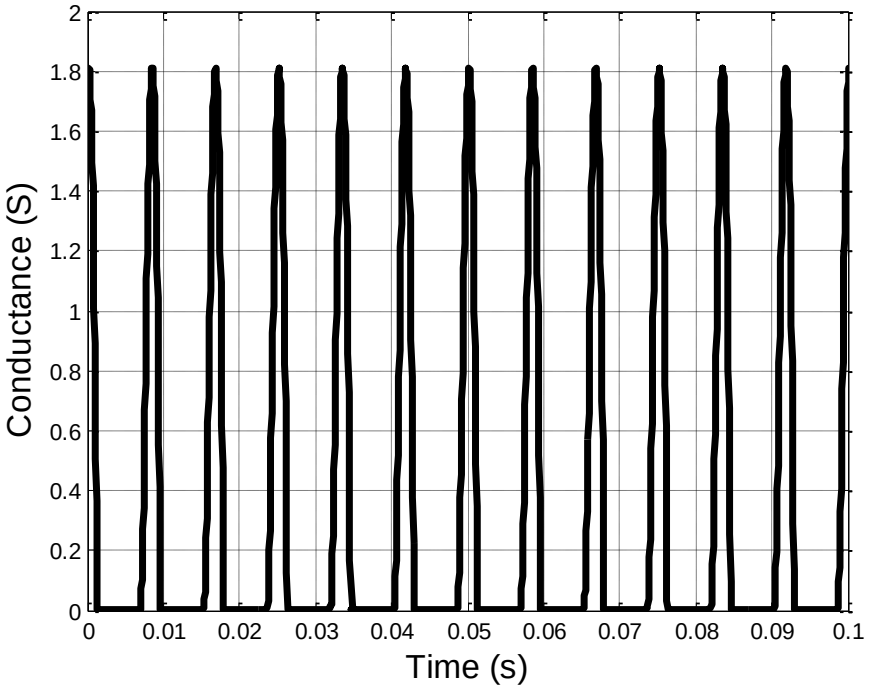


Figure 2-2: Instantaneous conductance diode bridge

To demonstrate how the conductance calculation converges, Figure 2-3 shows the calculation of the conductance as the lengths of the vectors grow in size. From the figure, it is clear that as the calculation is performed over larger intervals the conductance starts to converge on the same solution that Fryze's theory arrived at earlier. For this case, the system takes about 200 ms to converge. The sampling step size for this example was 50 μs. This behavior is fine for initialization and steady state waveforms but this is troublesome when the load is changing. In fact, Fryze's and Xu's approach are able to converge in half a period assuming half wave symmetry in the waveform. To illustrate this problem, Figure 2-4 shows the conductance during a step load condition. In the figure, the step load on the bridge rectifier occurs at 250 ms. The conductance is calculated at each time step using all of the previous calculations. With all of the previous information the system takes four seconds to reach the new steady state value. This is caused by the summation of the voltage and instantaneous power becoming large, which is analogous to anti-windup behavior seen when using integration in control feedback compensator. Therefore, it is clear that if the system wants to respond quickly then there needs to be some way to reset the control. There are techniques available for resetting; however, a study into the best methods is beyond the scope of this work. The author just wants to make the reader aware of the condition since it is not mentioned in the literature. In addition to resetting, it should also be pointed out that the sampling frequency does not need to be as high as the switching frequency.

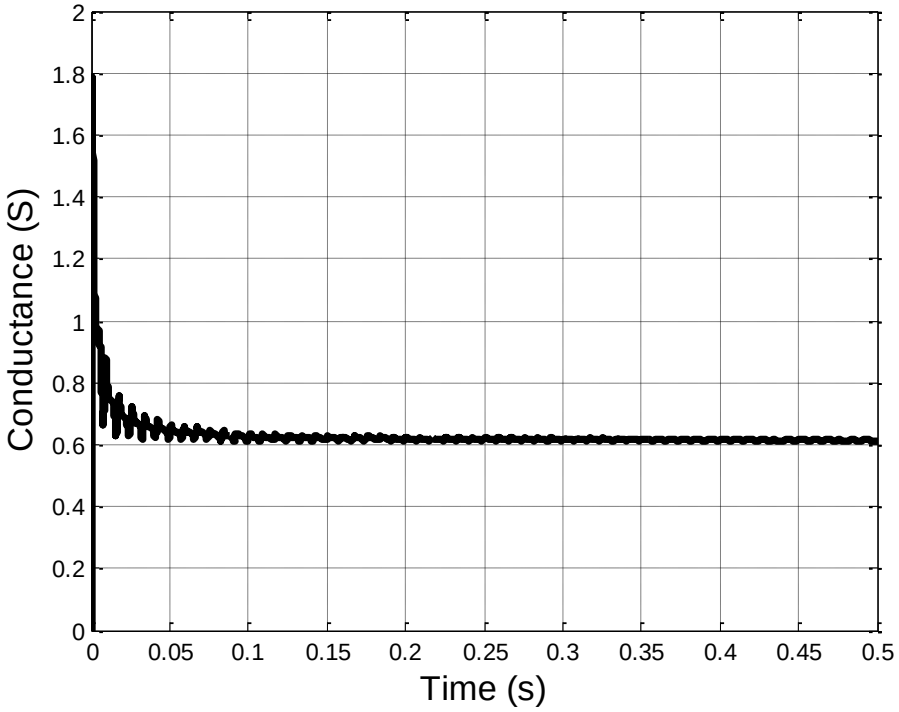


Figure 2-3: Conductance convergence

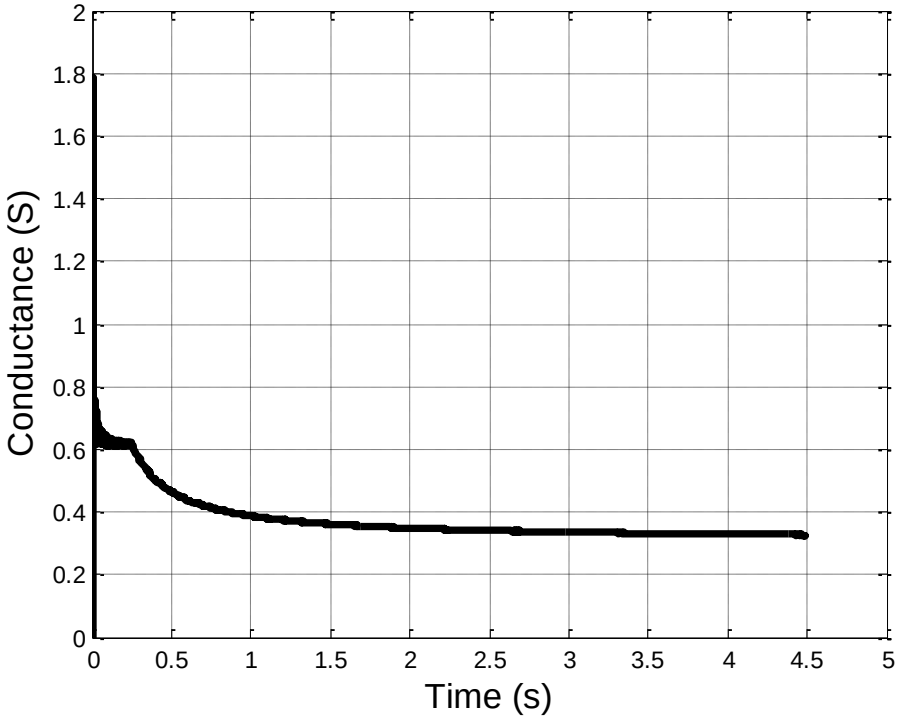


Figure 2-4: Conductance step load

2.4. Summary

A few of the different non-active power techniques were discussed and compared in this chapter. Since non-active power compensation is not the primary function of most grid-tie converters, the compensation techniques were compared in terms of ease of implementation and changes to the existing control structure. In chapter 5, harmonic compensation as a function of control system will be discussed, so in this chapter it will be assumed that the reference waveform is generated by using some type of non-active power technique. This chapter was not intended to be all-inclusive of all the techniques, but illustrated a few of the common techniques. The techniques illustrated in this chapter can be divided into three categories: (1) those that provide instantaneous compensation; (2) those that provide compensation over an average interval; (3) those that can do any interval. As we move forward with the analysis in later chapters, we will assume that these calculations do not impact the control system, so are of the instantaneous type; even though the results showed that the so called instantaneous results still took time to converge on the solution. It is also assumed that correction action has been taken to keep any summations from increasing as discussed in the previous section.

Chapter 3.Single Phase Grid-Tie Voltage Source Switching Models

One of the most widely used techniques for controlling the output voltage of a power converter is by the use of pulse width modulation (PWM). The technique involves varying the duty cycle of a switch or switches at high frequency to achieve a lower frequency or DC signal. In the case of AC applications, which will be the focus of the discussion, the duty cycle is varied to achieve a lower frequency signal. The principal idea is that the volt-second average of the switching waveform will have the same fundamental value as the target waveform [7]. One of the side effects of PWM is that the pulse trains create harmonics at the switching frequency and side band harmonics. These harmonics can be problematic to the load and source connected to the converter and can even cause interference issues with other loads in the system. In order to ensure that the converter will not cause problems with other equipment or the source, standards are in place to restrict the magnitude of the harmonics and noise that the converter can emit. To regulate the noise, filtering is required to attenuate the noise coming from the converter. For most designs, filtering is done with passive components which add additional losses, size, weight, and cost to the system. While all different AC PWM techniques share the common objective of creating a lower frequency waveform while minimizing unwanted harmonics and minimizing losses, there are advantages and disadvantages to the different approaches and applications where the different techniques are better than their counterparts. No modulation scheme is perfect for every application, so typically what defines the modulation scheme is the requirements of the application.

For grid-tie converter systems, which are the focus of this work, the requirements are for low losses, low harmonic distortion, small footprint, low leakage current, and EMI compatibility. Of course, minimizing one parameter could have an adverse effect on other parameters. Therefore, a balance between all of the requirements is essential, although an extremely challenging problem. The focus of this chapter is on the modulation schemes used for grid-tie converters, so the modulation techniques, losses, and noise will be analyzed for these types of systems. In chapter 4, the influence of the PWM methods on leakage current for PV applications will be examined while also expanding more on the emissions work from this chapter. In chapter 5, the filter design and controls will be discussed, which are also heavily influenced by the switching design. The intention of this chapter is to give a background for the remaining chapters. When discussing leakage current, emissions, and filtering, the switching schemes become very important and essential to understanding of the result. Therefore, the reader needs to have a basic understanding of these techniques to follow the results. This

chapter is not intended to discuss PWM in general and will only focus on techniques used for single phase grid-tie converters.

3.1. Two Level Converters

The single phase two level voltage source converter comes in two major forms, the half-bridge and full bridge topology. In the half bridge topology, the return path is connected to the midpoint of the bus as shown in Figure 3-1a. The voltage is bound between positive and negative ½ Vdc, which is determined by the selection of the two switches. Since the maximum absolute value of the voltage is ½ Vdc, the total DC bus needs to be at least twice the maximum output voltage. For grid-tie converters, the high DC voltage of the half bridge topology limits the application to lower voltage classes. For instance, a 480 V utility interconnect requires a DC voltage of nearly 800 V if connected phase to phase. This is often too high for standard low voltage applications. The converter does have some advantages over the full bridge topology. The most notable are small common mode voltage, low leakage current, and overall simplicity of the modulator [12]. These will be discussed in more detail in chapter 4.

The full bridge converter shown in Figure 3-1b is the most common topology found in single phase grid-tie application. The voltage on the output of the full bridge converter is bound to ± Vdc. The control of the switches depends on the application of the converter and requirements of the load. The switching can be as simple as square wave modulation or as complex as a hybrid type modulation scheme. For grid-tie converter applications, the goal of the switching is to minimize leakage current, emissions, losses, and reduced size and weight of the filter, so choosing a switching scheme that can reduce any of these issues is beneficial for the overall design. This chapter will primarily focus on the full bridge topology because of its popularity in grid-tie applications. However, the half and full bridge topology will be compared when applicable. This chapter is also a precursor to the next chapter which introduces some full bridge variations used to further improve the performance of the single phase converter in grid-tie applications.

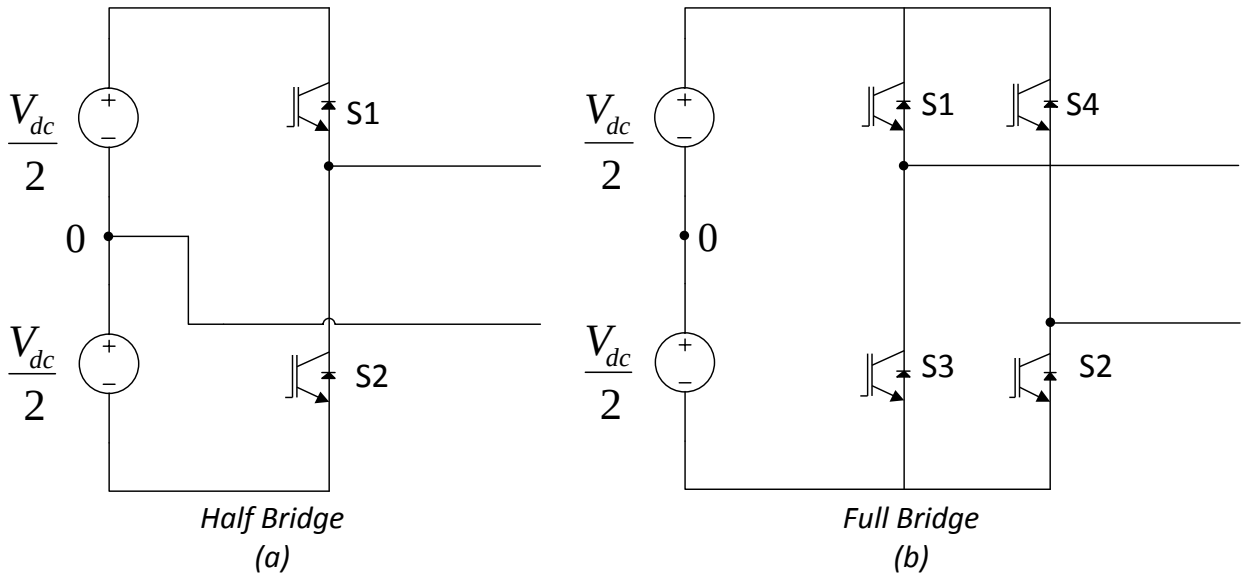


Figure 3-1 Two level single phase converters

3.1.1. Vector PWM Approach

Most people in the power electronic field are familiar with carrier based PWM techniques, so this chapter assumes that the reader has a basic understanding of PWM principles. If the reader is unfamiliar with the basic PWM principles, the work in [7] has a very thorough treatment of this subject. The vector PWM approach for single phase systems is not a new concept but is something that has become more popular for single phase applications because of grid-tie applications. With issues like high leakage current for PV applications, researchers started to readdress some of the less common PWM methods. Since in most inverter cases, unipolar modulation is easy to implement and produces low differential noise, there is often not much thought into the modulation choice for single phase converters. While some of this work may seem new to the reader, most of the work in this chapter is not original. The only work that is original is the low frequency derivations used to compare the carrier and vector PWM approaches.

The choice of the modulation scheme is one of most important aspects for designing a grid-tie converter since many of the design requirements are directly related to the modulation. By choosing a modulation scheme that can reduce switching losses, emissions, leakage current, and allow for smaller filtering, the overall requirements for the complete system become much easier to meet. It is therefore important to understand the advantages and disadvantages of the different PWM. This chapter will focus on the advantages and disadvantages of the methods as well as how they affect other system design parameters. The implementation of each method will be explained with both a carrier and vector approach.

The basic idea with the vector approach to PWM is to get the variables into a vector format and then divide the vector into sectors. Within the sectors the switching positions are determined and distributed according to the modulation technique the user wants to implement. This is the same approach used in space vector modulation (SVM) for three phase systems. The only difference is that for single phase systems the transformation is much simpler since there are only two sectors. As one might suspect, for single phase systems there is a positive sector and a negative sector. Figure 3-2 shows the vector diagram used for single phase systems. The reference vector is obtained by performing a pseudo dq transformation of the system, which will be discussed in detail in chapter 5. For now, let's assume that the d and q-axis references are a result of the control system. These variable can be transformed back to phase parameters by multiplying by the transformation matrix given in (3-1). From V_α and V_β, it follows that the magnitude and angle can be calculated by using (3-2) and (3-3) . The transformation is also easily transferred in the other direction since the transformation is an orthogonal matrix.

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} V_d \\ V_q \end{bmatrix} \cdot \begin{bmatrix} \cos\omega t & -\sin\omega t \\ -\sin\omega t & -\cos\omega t \end{bmatrix} \tag{3-1}$$

$$V_m = \sqrt{V_d^2 + V_q^2} \tag{3-2}$$

$$\theta = a\tan\left(\frac{V_\beta}{V_\alpha}\right) \tag{3-3}$$

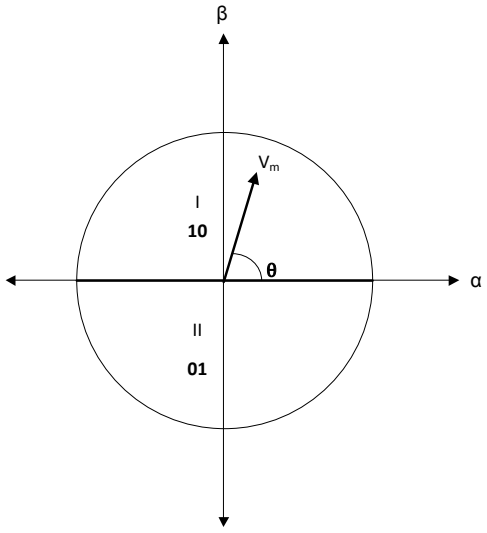


Figure 3-2: Vector PWM diagram

From the magnitude and angle, the duty cycle and sector can be determined. Between π/2 and 3π/2 the signal is negative since the system was aligned with cosine on the d-axis. The active and zero switching time can be calculated based on the DC link voltage assuming volt-sec balance over the switching cycle. The equations for calculating the switching times are given in (3-4) - (3-6). To distinguish between the two sectors, positive and negative timing are used corresponding to T_1 and T_2. This is only to make the sectors distinguishable to the reader. In the real implementation, only the absolute value of the timing is needed.

$$T_1 = T_s \frac{V_m}{V_{DC}} \cos\theta \tag{3-4}$$

$$T_2 = -T_s \frac{V_m}{V_{DC}} \cos\theta \tag{3-5}$$

$$\begin{aligned} T_0 &= T_s - T_1 \\ T_0 &= T_s - T_2 \end{aligned} \tag{3-6}$$

From the switching times and the sectors, PWM is easily implemented by controlling the switches in Figure 3-1b. If the voltage vector is in sector 1, then switches S_1 and S_2 in Figure 3-1b should be on. If the voltage vector is in sector 2, then switches S_3 and S_4 in Figure 3-1b should be on. The remainder of the switching period uses T_0 for unipolar modulation schemes and is divided between the two active states for bipolar modulation. Two zero vectors exist, both of the top switches on (PP) or both bottom switches on (NN). How the timing and use of the zero vectors are divided within the cycle is the only difference between the modulation schemes presented in this chapter.

3.2. Bipolar Modulation

The most traditional methods for pulse width modulation are unipolar and bipolar modulation, which are also referred to as three and two level modulation in some texts and references. The reason for the naming is evident when looking at the output voltage waveforms, but can be confusing since neutral point clamped converters are also referred to as three level converters in literature. To avoid confusion, the bipolar and unipolar naming will be used throughout the remainder of this chapter. In bipolar modulation, the two legs of the inverter are switched in complement to each other. This has the advantage of only requiring a single reference for carrier based pulse width modulation. The main disadvantage with this approach is that when the output is switched between $\pm V_{DC}$ the switching losses and switching ripple are lager compared to switching from 0 to V_{DC}. Figure 3-3 shows carrier and reference waveform for the two phase legs. Although both phase legs are shown in the figure, only a single leg is needed in the real design since the other leg is equal to the complement of the leg being controlled. Both phase legs are shown only for comparison purposes with waveforms in later discussions. Notice in the figure that both the references and carriers for the two phase legs are the negative of each other.

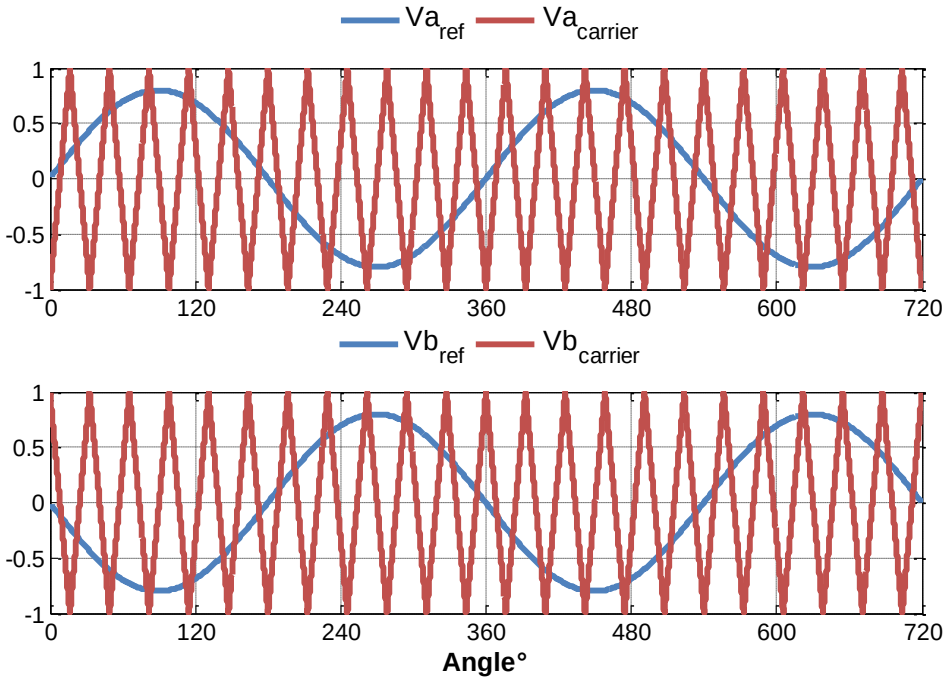


Figure 3-3: Bipolar PWM carrier approach

In addition to the simplistic implementation, another advantage of bipolar switching is that in the ideal case the technique does not generate common mode voltages. This can be explained by looking at the Double Fourier Integral as done in [7], or by simply looking at the phase leg waveforms in Figure 3-3. Since both the carrier and reference for the phase legs are negatives of each other, it is easy to see without any rigorous analysis that the addition of the phase legs would sum to zero. In a real design, the common mode voltage cannot be completely eliminated because of the need for a dead time between switching and asymmetries in the switching.

With the vector approach, bipolar modulation is implemented by dividing the zero time equally among the two active switching states. Figure 3-4 shows the two switching sectors with their equivalent duration at each of the states. Since V_1 and V_2 are negatives of each other and distributed equally among the switching cycle, the zero time does not contribute to the average of the waveform. This means that the average over sector 1 equals V_1 and that the average of sector 2 equals V_2. It is worth noting that for simulation and hardware implementation, the start and end point for the sectors should be the same as shown in Figure 3-4. For example, if d_a is high at the end of the switching period in sector 1, then d_a should start high in sector 2. Without this seamless transition it is possible to get unwanted switching transients between switching sectors. This technique of switching sectors in the same state will be used throughout this chapter but will not be addressed for every modulation technique; however, for each modulation method the same principles and reasoning apply.

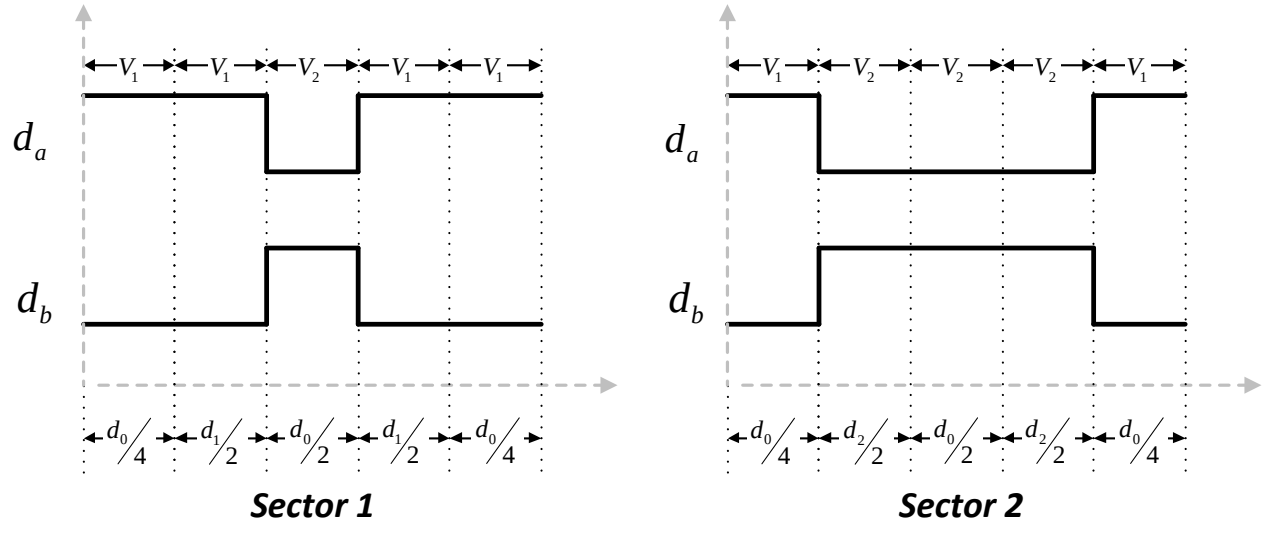


Figure 3-4: Bipolar PWM vector approach

3.3. Unipolar PWM

In unipolar modulation implemented with vector PWM, the zero states are used for the T_0 time period. For unipolar modulation, it is possible to use either of the zero states within the cycle and distribute them anywhere within the cycle. However, it is advantageous to distribute the zero vectors in a way that can minimize switching losses and reduce distortion. Minimizing switching losses is done by limiting the number of transitions within the cycle. This means that it is better to choose a zero pattern that has four switching events vs. six switching events. Reducing distortion is not as easy to see from the vector waveforms, but the distortion is related to the switching as well as the symmetry of the switching waveform. By making the waveform symmetrical within the switching period, the distortion caused by the high frequency switching is reduced vs. an asymmetrical waveform. For a carrier based implementation, this is equivalent to selecting a carrier waveform that is symmetrical. Figure 3-5 shows the two switching sectors for the vector approach for traditional unipolar modulation. Notice in the figure that the zero states are distributed within the switching period in order to reduce switching transitions and provide waveform symmetry.

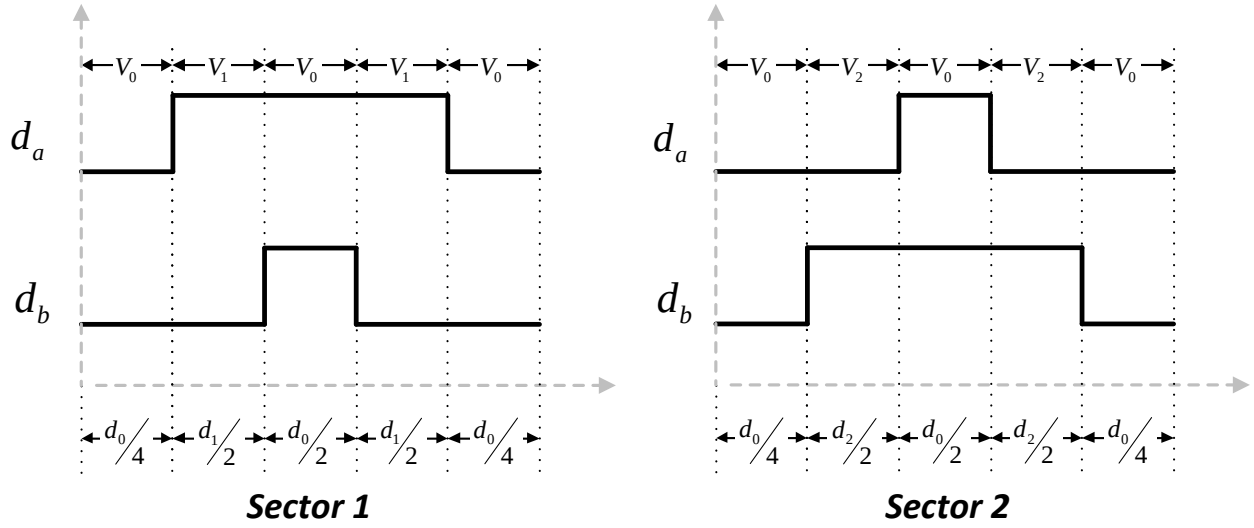


Figure 3-5: Traditional unipolar PWM vector approach

Unipolar modulation is also easily implemented with a carrier and reference waveform. With the carrier approach, unipolar modulation is accomplished by comparing a reference and the negative of the reference to a high frequency carrier waveform. Figure 3-6 shows the two phase legs using a triangle carrier. The carrier is typically a triangle wave for the symmetry and harmonic reasons discussed previously. Using a triangle wave for a carrier is equivalent to the vector approach shown in Figure 3-5. Notice that the difference between unipolar modulation and bipolar modulation is the carrier waveform. For unipolar modulation, the carrier is the same for both phase legs, but for bipolar modulation carriers are the negative of each other.

The most notable advantages of unipolar modulation are the reduction in switching losses and reduction in harmonic distortion. Both reductions are related to the use of the zero states. Improvement in the harmonic distortion is also contributed to the cancelation of the odd order switching harmonics between the phase legs. When the odd order harmonics are eliminated, this makes the phase to phase voltage appear as if the converter is being switched at twice the switching frequency. Another way to think about this is that the switching frequency can be reduced by half to produce the same harmonic frequencies as bipolar modulation. Of course, reducing the switching frequency by half also reduces the switching losses. Because of the use of the zero states, the harmonic magnitudes are also less for unipolar modulation than for an equivalent bipolar modulation. This means that even for the same switching harmonics, the magnitudes of the harmonics will be less for unipolar than bipolar modulation.

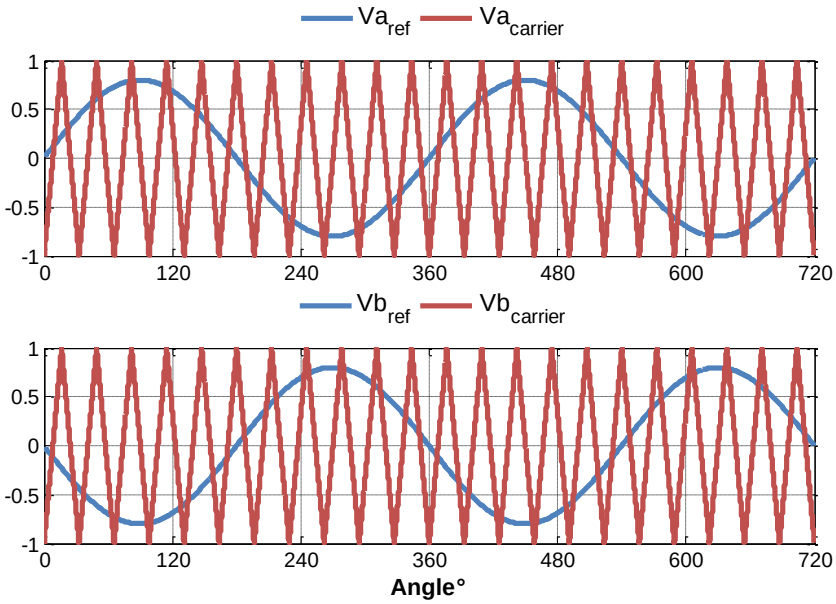


Figure 3-6: Traditional unipolar PWM carrier approach (M_i=0.8)

Unipolar modulation is not without its disadvantages though. Of course, for carrier implementation, it requires the reference and negative of the reference to be compared with a high frequency carrier waveform. This increases the complexity and number of components needed for modulator since the phase legs are now controlled separately. Also, the common mode voltage contains the odd order switching harmonics that cancel in the differential measurements. Remember that with bipolar modulation in the ideal case, the common mode is zero but the phase to phase (differential) harmonics are twice the individual phase cases. Figure 3-7 shows the common mode voltage under unipolar modulation to illustrate this result. The average of common mode voltage in the top waveform is calculated over the switching period, which in this example is 5 kHz. This is shown to emphasize that no low end harmonics are present in the common mode. The figure also shows the Fast Fourier Transform (FFT) of the common mode voltage cycle in the bottom graph. Notice that only the odd order switching harmonics are present in the common mode. Common mode voltage can be problematic when trying to meet emissions and leakage current requirement, and is therefore generally in the best interest of the designer to reduce the common mode noise. More will be discussed about the common mode emissions in the next chapter.

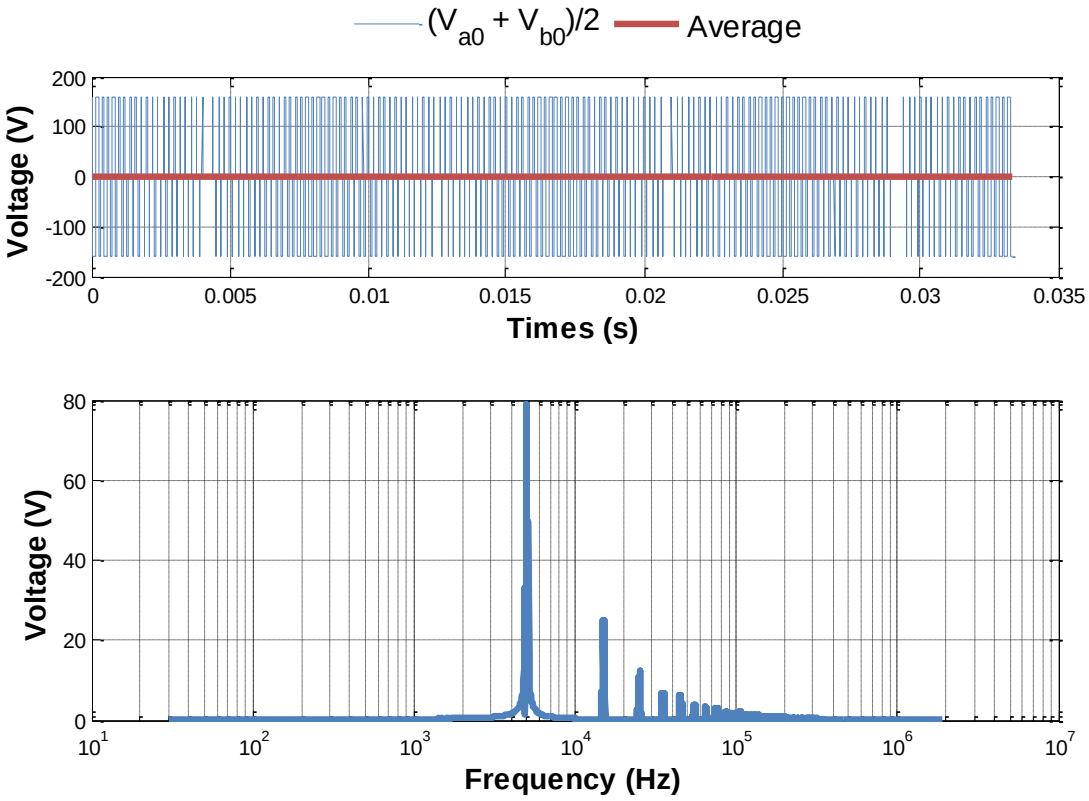


Figure 3-7: Unipolar common mode duty cycle (V_{dc} = 320V and M_i = 1)

3.4. Hybrid Modulation (Type 1)

With traditional unipolar and bipolar modulation, both phase legs are switched at high frequency. However, switching both phase legs is not a requirement for PWM synthesis. In fact, it is possible and even advantageous to switch the phase legs with both a low and high frequency modulation. This hybrid modulation, also called discontinuous in some literature, has been researched and is well understood from a fundamental modulation perspective. However, the grid-tie requirements, mainly the EMI and leakage current, warrant additional investigation from an application standpoint. Of course, with all modulation schemes there will be advantages and disadvantages, so these will be addressed in the discussion of the hybrid approach. Two different hybrid approaches will be discussed in this section, but it is easy to see that other variations are possible with this approach. From a switching loss and harmonic distortion standpoint, the two methods discussed offer the best performance.

The implementation of this hybrid approach is easy to see with the vector approach to PWM since the switching states are easily visible from the diagrams. Remember that the objective is for the average over the switching period to equal the target waveform. Therefore, the distribution of the switching states is the only difference between all the different modulation approaches presented. Figure 3-8 shows the switching vectors for one of the hybrid modulation scheme that will be discussed. Notice in the figure that one of the phase legs is switched at low frequency while the other is switched at high frequency, and that the average over the switching period is equivalent to standard unipolar and bipolar modulation. Although it is possible to switch either phase leg at low frequency, it will be shown later that if the neutral conductor of the utility voltage is grounded it is better to switch the neutral phase leg at low frequency for leakage current reasons.

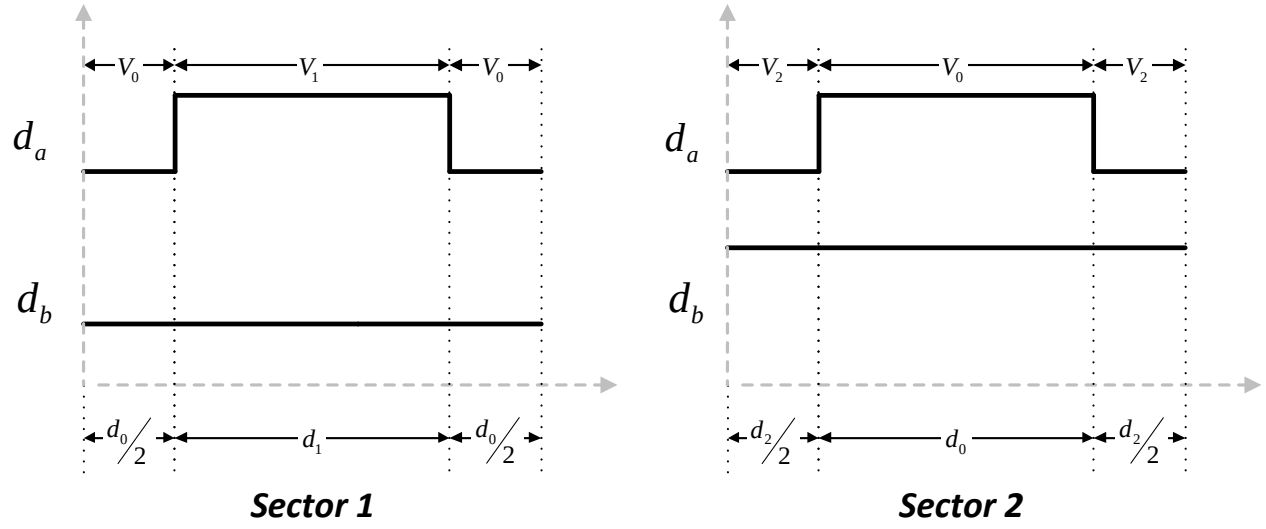


Figure 3-8: Hybrid 1 PWM vector approach

It is also possible to implement an equivalent hybrid modulation approach with a carrier and a reference waveform for each phase. The steps for performing the conversion to a carrier equivalent are given below:

1. Write out piecewise time domain equations for each phase's duty cycle
2. Calculate the Fourier series of the waveform
3. Choose a carrier waveform

As an example, let's look at Figure 3-8 and apply the steps outlined above. First, write out the equations for each of the phase duty cycles using the timing information and the definitions given for T_1 and T_0. After writing the equations, the two duty cycle equations that result are given by (3-7) and (3-8).

$$d_{a0} = \begin{cases} \frac{1}{2} \cdot \left[M_i \cdot 2 \cdot \sin\theta - 1 \right] & Sector\ 1 \\ \frac{1}{2} \cdot \left[M_i \cdot 2 \cdot \sin\theta + 1 \right] & Sector\ 2 \end{cases} \tag{3-7}$$

$$d_{b0} = \begin{cases} -\frac{1}{2} & Sector\ 1 \\ \frac{1}{2} & Sector\ 2 \end{cases} \tag{3-8}$$

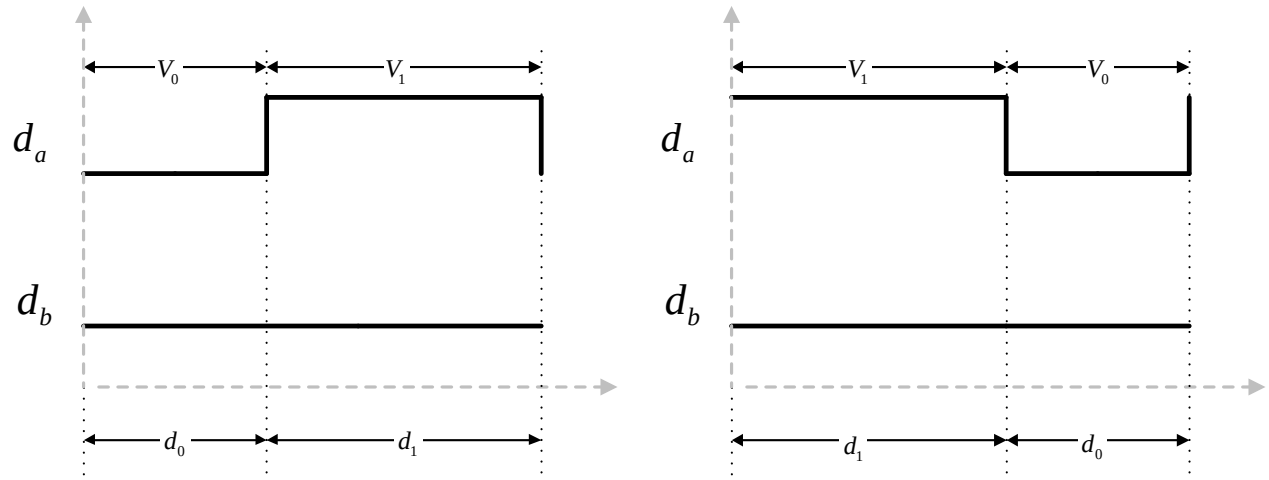
Next, write and solve the Fourier series using the duty cycles given in (3-7) and (3-8). Solving the Fourier series for the duty cycles results in (3-9) and (3-10) . Notice that the Fourier series for phase b duty cycle is equal to a square wave. This is expected since the duty cycle varies between two constant values over the fundamental frequency cycle. The results for phase a is not so easy to see from the time domain equations, but by using the Fourier series it is possible to easily solve for the analytical solution for the duty cycle. As a check to the solution for phase a, realize that the phase to phase duty cycle will be equal to a sinusoid scaled by the modulation index. If phase b duty cycle is subtracted from the phase a duty cycle, then the equation that results is (3-11), which verifies that the phase a duty cycle is correct. It is also possible to rearrange (3-11) and solve for the phase a duty cycle without needing to evaluate the Fourier integral. The solutions in (3-9)-(3-11) are only valid for a sinusoidal phase to phase duty cycle. Although, it easy to see that since the phase b duty cycle will always remain a square wave, the first term in the phase a duty cycle will be equal to the phase to phase duty cycle even under non-sinusoidal conditions.

$$d_{a0} = M_i \cdot \sin(\omega \cdot t) + \frac{1}{2} \cdot \left[-\frac{4}{\pi n} \sum_{n=1,3,5...}^{\infty} \sin(n \cdot \omega \cdot t) \right] \quad (3\text{-}9)$$

$$d_{b0} = \frac{1}{2} \cdot \left[-\frac{4}{\pi n} \sum_{n=1,3,5...}^{\infty} \sin(n \cdot \omega \cdot t) \right] \quad (3\text{-}10)$$

$$d_{a0} - d_{b0} = d_{ab} = M_i \cdot \sin(\omega \cdot t) \quad (3\text{-}11)$$

The last step involves choosing a carrier waveform to produce the same switching pattern as the vector waveform. Notice in Figure 3-8 that the timing of the switching cycles were chosen so that the waveform would be symmetric over the switching period. This is equivalent to using a triangle carrier waveform. It is also possible to align the waveform to the left or right as shown in Figure 3-9, which result in the same number of switching events but is no longer symmetric within the switching cycle. This is equivalent to using a sawtooth carrier aligned to the left or right. Since the number of switching events remains the same for the three cases, it makes sense to choose the triangle waveform if possible since the symmetry in the waveform produces lower distortion.



Sector 1- Left Aligned ***Sector 1-Right Aligned***

Figure 3-9: Vector alignment

At this point it may not be clear to the reader how to use the carrier and reference waveforms to generate the needed duty cycles. To illustrate this concept, Figure 3-10 shows the carrier waveform and the reference waveforms for each of the phases. Notice that the phase b reference waveform is a square wave given by (3-10) and that the phase a reference is the expression given in (3-9). Generating the reference waveform for the phase using only the modulation index is challenging even with sophisticated analog circuitry. Therefore, the more practical way to generate the phase a reference is to fix the phase b reference as a square wave and then add the phase to phase reference (control reference) to the phase b (square wave) reference. This approach forces phase b to switch at the fundamental frequency and phase a to switch at high frequency while also canceling out the low order harmonics of square wave modulation. This approach also works if the phase to phase control reference is non-sinusoidal.

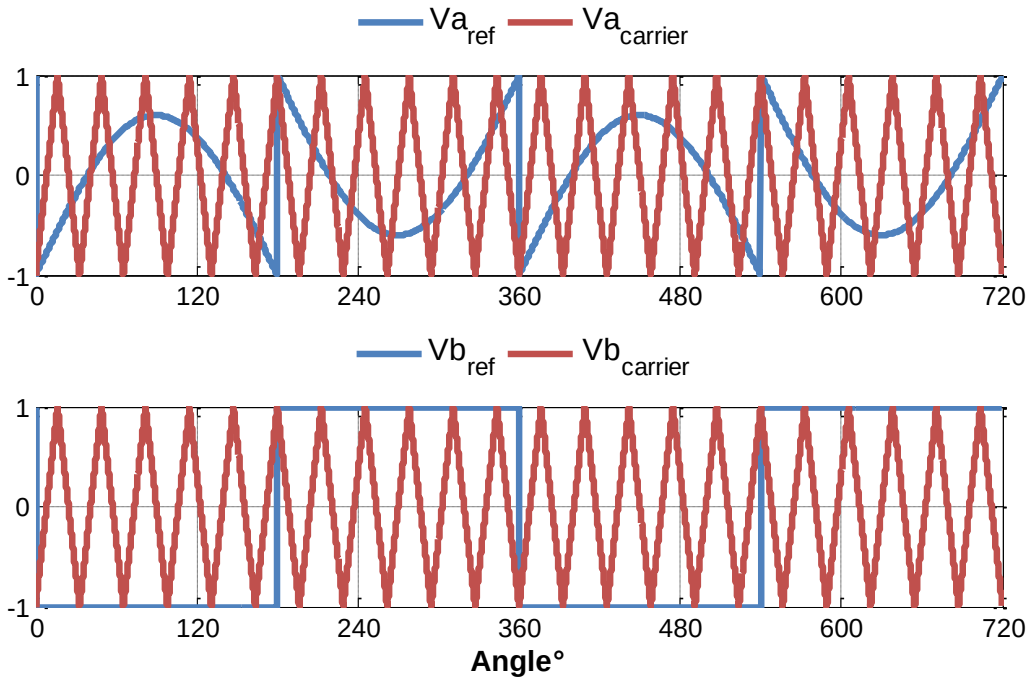


Figure 3-10: Hybrid 1 carrier approach (M_i=0.8)

The hybrid modulation scheme is obviously more difficult to implement with analog circuitry. Therefore, there has to be some advantages when compared to traditional bipolar and unipolar modulation. First, the amount of switching is reduced by half when compared to unipolar and bipolar modulation. This can be seen by comparing Figure 3-4 and Figure 3-8. Notice in Figure 3-4 that there are four switching events in each sector and in Figure 3-8 that there are two switching events. In addition to the amount of switching, the modulation scheme also uses the zero vectors resulting in a unipolar output voltage. The combination of both the switching amount and use of the zero states reduce the switching losses when compared to bipolar modulation. The use of zero states also reduces the harmonic distortion of the output voltage when compared to bipolar modulation.

Compared to unipolar modulation, this hybrid modulation scheme is actually equivalent from a switching loss and harmonic performance. This is because of the cancelation of the odd order switching harmonics achieved with unipolar modulation. Because of the harmonic cancelation, the switching frequency is "artificially" doubled in the phase to phase measurements for traditional unipolar modulation. Therefore, if the switching frequency is reduced by half for unipolar modulation to produce the same harmonic equivalent as the hybrid approach, then it is clear that the two methods would switch the same number of times. In [7], the double Fourier integral of both types is investigated and shown to be equivalent. The main advantage over unipolar modulation is that phase b duty cycle is varied at the line frequency. It will be shown later that for PV applications the leakage current is directly related to the neutral (phase b) duty cycle when the system is grounded and the output filtering is asymmetrical. This analysis is left for later in the work since all the methods are compared.

The hybrid modulation scheme does however have one major difference compared with unipolar and bipolar modulation, and that is the low frequency common mode voltage generated from the modulation. Remember that with bipolar modulation the common mode voltage is ideally zero for all frequencies, and with unipolar modulation only the odd order switching harmonics remain. For the hybrid modulation scheme, low frequency harmonics are present in the common mode voltage. Equation (3-12) gives the analytical expression for the low frequency common mode harmonics, which comes from the addition of (3-9) and (3-10). In addition to the low frequency harmonics, the modulation scheme also contains the switching frequency harmonics and sidebands from the phase leg that is switched at high frequency. Figure 3-11 shows the time and frequency domain characteristics of the common mode voltage for the hybrid modulation approach. The average in the waveform is the low frequency common mode carrier harmonics given in (3-12).

$$\frac{d_{a0}+d_{b0}}{2}=\frac{M_i\cdot}{2}\sin(\omega\cdot t)+\frac{1}{2}\cdot\left[-\frac{4}{\pi n}\sum_{n=1,3,5\ldots}^{\infty}\sin(n\cdot\omega\cdot t)\right] \tag{3-12}$$

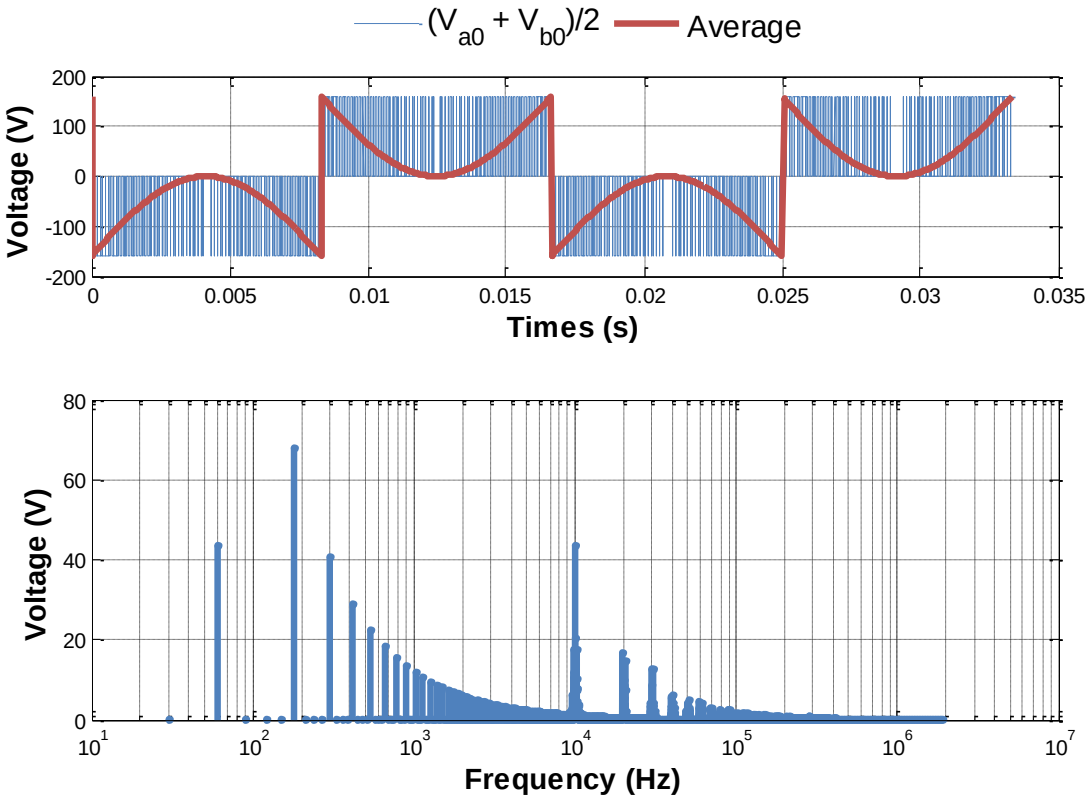


Figure 3-11: Hybrid 1 common mode duty cycle (V_{dc} = 320V and M_i = 1)

Since with the hybrid modulation approach a single phase leg is switched at high frequency, the switching frequency and sideband harmonics in the common mode are less for the hybrid modulation scheme than for unipolar modulation. Figure 3-12 shows a comparison of the common mode duty cycles for the hybrid modulation approach and traditional unipolar modulation. Notice in the figure that the switching frequency harmonics are less for the hybrid approach. The switching frequency for the unipolar case was chosen as 5 kHz so that the two methods would have equivalent phase to phase harmonic spectrum (10 kHz). Of course, since the odd order switching harmonics for the common mode duty cycle do not cancel for unipolar modulation, the common mode voltage contains the 5 kHz switching harmonics.

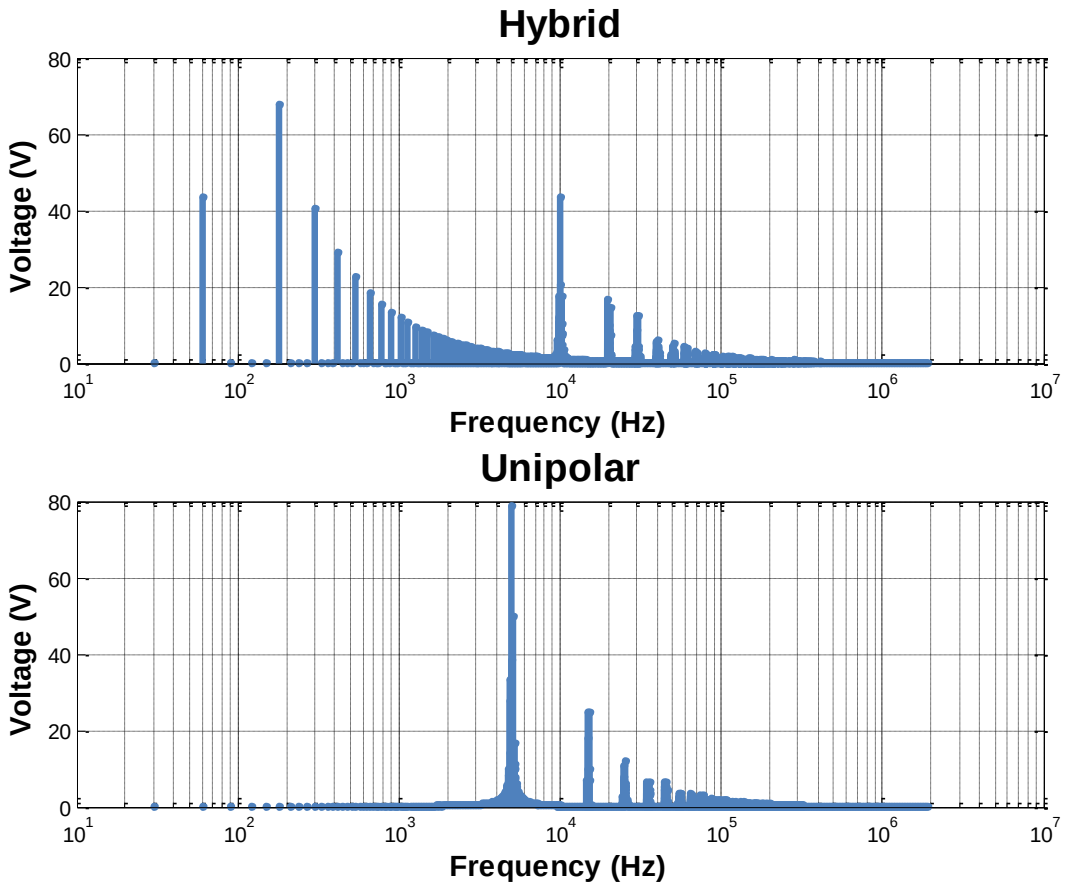


Figure 3-12: Comparison common mode duty cycles hybrid 1 (10 kHz) and unipolar (5 kHz)

Although the hybrid approach contains low end harmonics, the EMI and filter issues associated with the modulation are not necessarily more problematic than for unipolar modulation. In fact, unipolar modulation is worse for common mode. The common mode path in the converter for the most part is through the capacitance between the switching devices and the heat sink, which it typically fairly small and high impedance at the low frequency. Also, since most emissions standards do not address conducted emissions below 10 kHz, the low frequency emissions levels are not a problem from a compliance standpoint. The low frequency common mode voltage can however create low frequency leakage current. Since many converters have leakage current requirements for safety reasons, this can be an issue with this type of modulation for certain applications and topologies. Leakage current will be addressed in the next chapter.

3.5. Hybrid Modulation (Type 2)

Besides forcing one of the phase legs to switch at low frequency while the other is switched at high frequency, it is also possible to have each phase leg switch at the line frequency for half of the line cycle and at the switching frequency for the other half cycle. Figure 3-13 shows the switching vector diagrams for both sectors to illustrate the concept. Notice in the figure that each phase duty cycle is constant for one sector and switching for the other sector. This has the advantage of distributing the switching losses equally among the switches, which was not the case for the previous hybrid approach. Of course by holding one leg constant for half of the switching cycle, the total number of switching events is reduced by half vs. bipolar modulation and equivalent to unipolar modulation using an equivalent switching frequency.

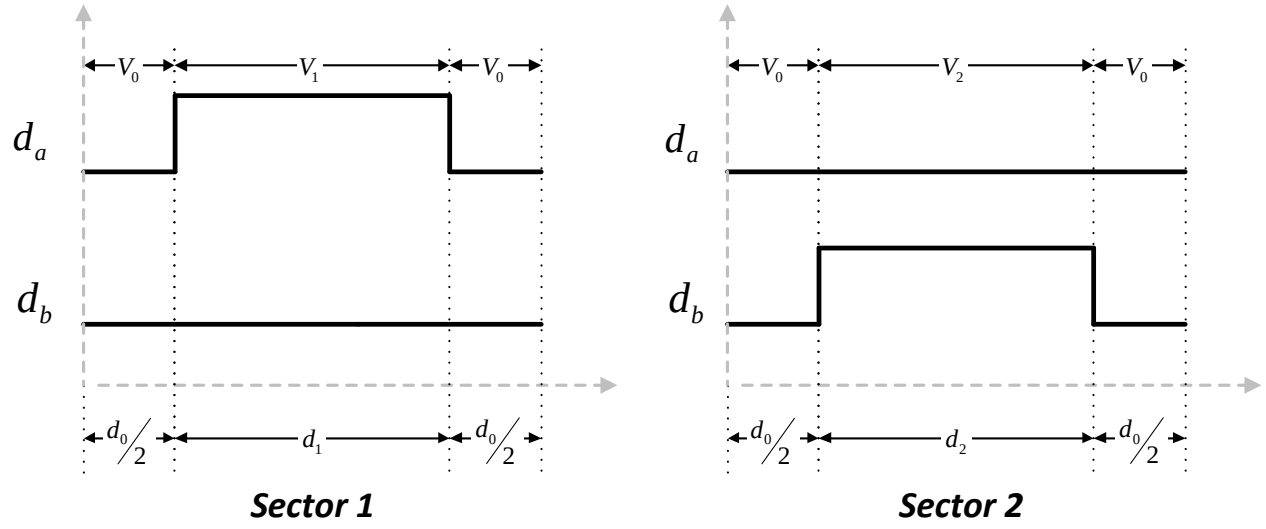


Figure 3-13: Hybrid 2 PWM vector approach

From the vector diagram in Figure 3-13, it is possible to develop a carrier equivalent using the same procedures outlined during the first hybrid approach. First, start by finding the piecewise time domain equations for each of the sectors, which are given in (3-13) and (3-14) and found by using the definitions for T_1, T_2, and T_0.

$$d_{a0} = \begin{cases} \frac{1}{2} \cdot \left[M_i \cdot 2 \cdot \sin\theta - 1 \right] & Sector\ 1 \\ -\frac{1}{2} & Sector\ 2 \end{cases} \tag{3-13}$$

$$d_{b0} = \begin{cases} -\frac{1}{2} & Sector\ 1 \\ -\frac{1}{2} \cdot \left[M_i \cdot 2 \cdot \sin\theta + 1 \right] & Sector\ 2 \end{cases} \tag{3-14}$$

Next, use the Fourier series to develop a continuous expression for the duty cycle. Although more involved than the previous hybrid method, these expressions are easily formulated with software such as Matlab or MapleSoft. The results of the Fourier series as a function of the modulation index are given in (3-15) and (3-16). From these expressions, there are a couple of interesting properties worth noting. First, is that both duty cycles have a DC component, which was not present with first hybrid approach. Second, is that the duty cycle contains only even harmonics. Finally, note that the harmonic magnitudes are less than previous hybrid method (i.e., n^2 vs. n), which is beneficial from a common mode standpoint. The carrier approach for this hybrid approach is illustrated in Figure 3-14 using a triangle wave for a carrier.

$$d_{a0} = \frac{M_i}{2} \cdot \left[\left(-2 + \frac{4}{\pi} \right) + \sin(\omega \cdot t) - \frac{4}{\left(n^2 - 1 \right) \cdot \pi} \sum_{n=2,4,6\ldots}^{\infty} \sin(n \cdot \omega \cdot t) \right] \tag{3-15}$$

$$d_{b0} = \frac{M_i}{2} \cdot \left[\left(-2 + \frac{4}{\pi} \right) - \sin(\omega \cdot t) - \frac{4}{\left(n^2 - 1 \right) \cdot \pi} \sum_{n=2,4,6\ldots}^{\infty} \sin(n \cdot \omega \cdot t) \right] \tag{3-16}$$

Since the harmonics and DC component are the same for both duty cycles, it follows that the difference between the duty cycles is equal to the fundamental frequency component, which is given in (3-17). While it was possible to develop the mathematical expressions for the reference waveforms, implementing this hybrid approach using analog circuitry is not simple. Therefore, implementation of this method is usually done using a DSP or FPGA by using the vector timing diagram given in Figure 3-13.

$$d_{a0} - d_{b0} = d_{ab} = M_i \cdot \sin(\omega \cdot t) \tag{3-17}$$

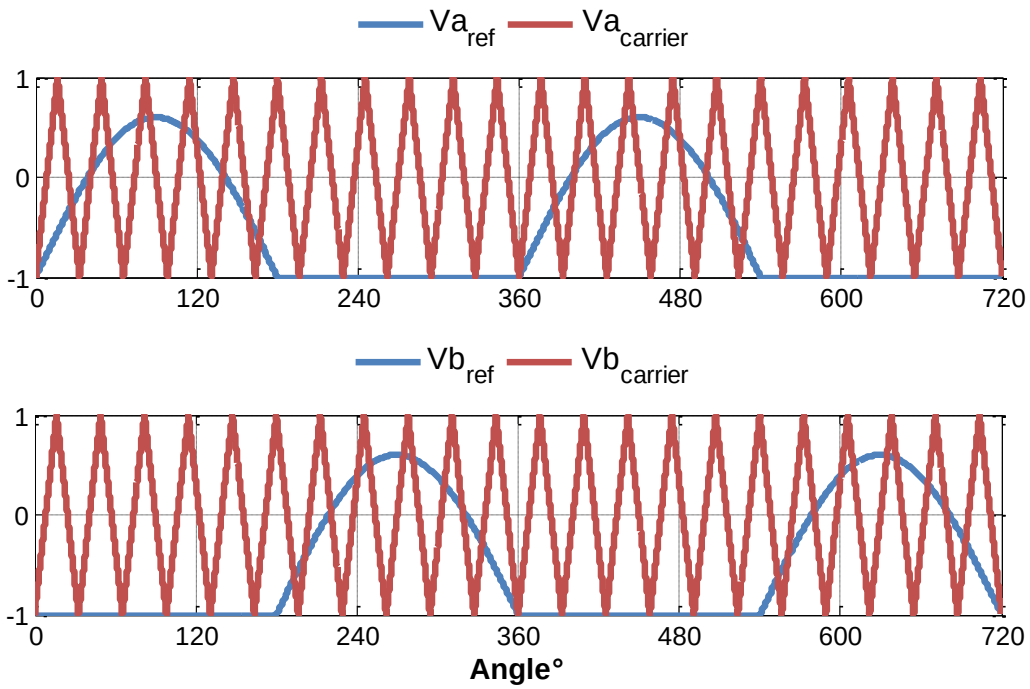


Figure 3-14: Hybrid 2 carrier approach

Similar to the first hybrid approach, this approach also produces low frequency common mode harmonics. Figure 3-15 shows the common mode voltage in the time and frequency domain. The average waveform in the figure is from the addition of the two reference waveforms and is given by (3-18). Notice that the average common mode voltage in Figure 3-15 only contains the DC and even harmonic components given by (3-18). From a low frequency common mode harmonics standpoint, this approach is better than the first hybrid approach because of the n^2 term in the harmonics. Since most of the common mode paths are through capacitance, the DC component is not a concern for leakage current or emissions.

$$\frac{d_{a0}+d_{b0}}{2}=\frac{M_i}{2}\cdot\left[\left(-2+\frac{4}{\pi}\right)-\frac{4}{\left(n^2-1\right)\cdot\pi}\sum_{n=2,4,6\ldots}^{\infty}\sin(n\cdot\omega\cdot t)\right] \qquad (3\text{-}18)$$

For the switching and side band frequencies, the two approaches are identical. Figure 3-16 shows a comparison of the two hybrid approaches. Notice that the switching frequency harmonics are the same for both approaches but that the low frequency harmonics are much lower for the second hybrid approach.

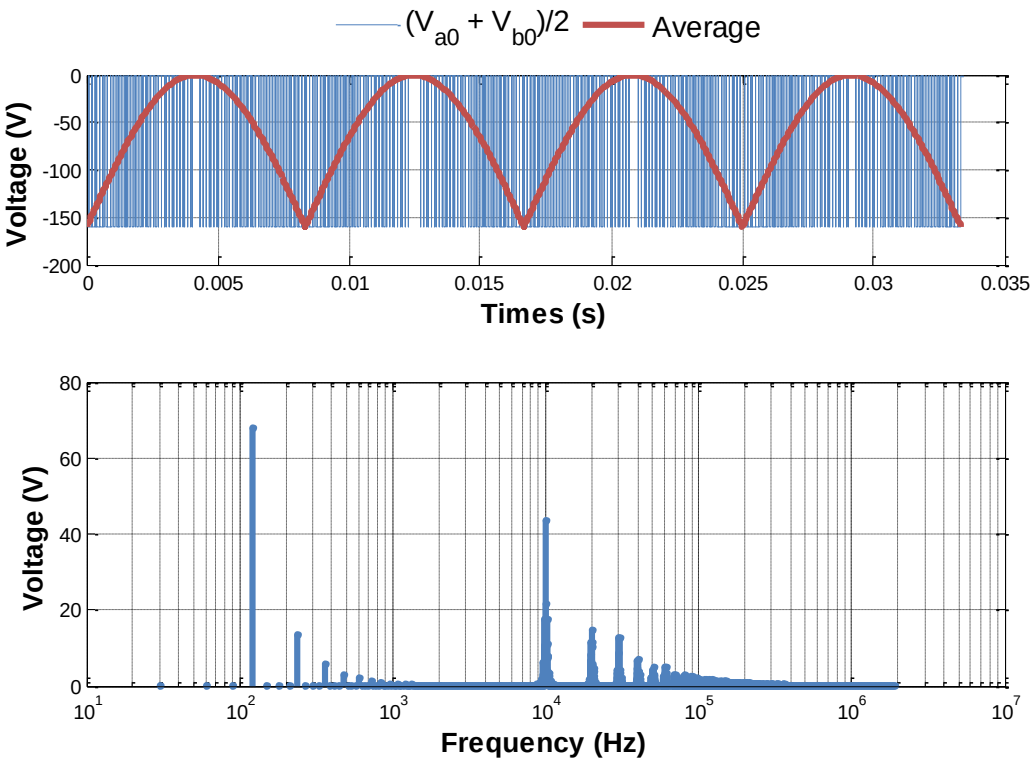


Figure 3-15: Hybrid 2 common mode duty cycle (V_{dc} = 320V and M_i = 1)

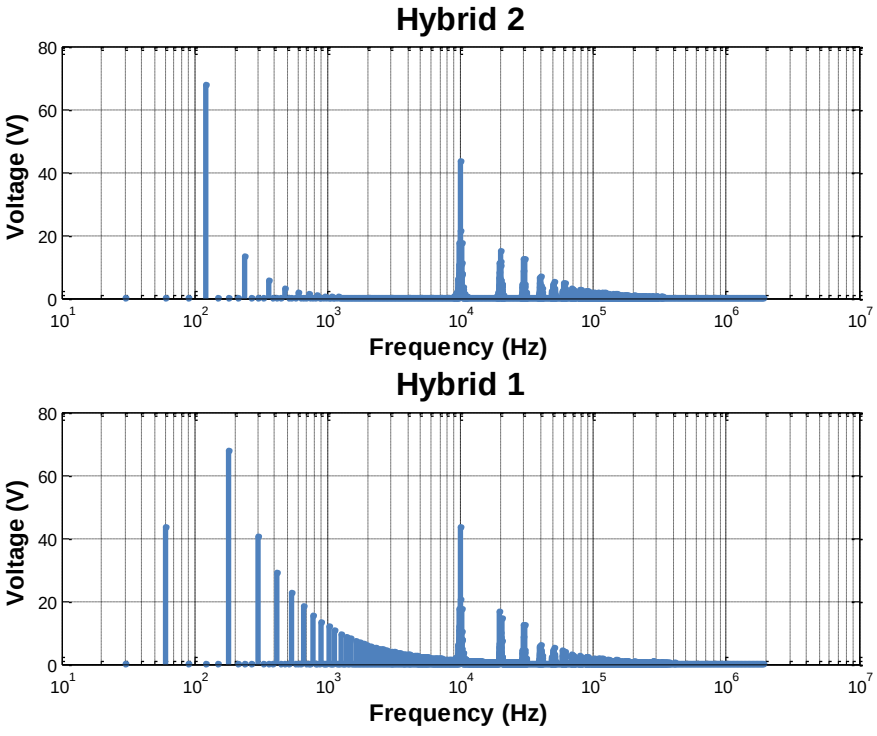


Figure 3-16: Comparison common mode duty cycles hybrid 1 and hybrid 2

3.6. Summary

In this chapter a few of the common single phase pulse width modulation techniques were discussed and compared. For all of the techniques, the vector and carrier implementation were illustrated with an example case. Overall, the vector approach is much more elegant approach for the hybrid techniques because of the ease of dividing the switching times. It became apparent in the analysis that the only difference between all of these techniques with the vector approach is how the timing is distributed within the cycle. For the hybrid approaches, low frequency expressions for the duty cycles were found using Fourier analysis. The chapter also discussed the different techniques in term of switching losses and differential and common mode noise.

In the next chapter, the conducted emissions and leakage current will be discussed in more detail, so it is important that the reader has a basic understanding of these four techniques since these will be used for the discussions. The purpose of the chapter was to give an overview for the analysis needed in the proceeding chapters. In addition to standard topologies, chapter 4 will also discuss some commercial PV converters used in the field today. At the heart of the modulator for these converters will be one of these four techniques. Therefore, without an understanding of these techniques it is not possible to explain the commercial products. In chapter 5, filtering will be discussed, so the switching harmonic and noise results of this chapter are important.

Chapter 4.Single Phase Leakage Current in PV Applications and Conducted Emissions

In photovoltaic (PV) applications, leakage current is a problem for grid-tie converters because of the large capacitance formed between the PV panel and ground. In the past, the solution for this problem has been to use a low frequency transformer between the inverter and utility to isolate the two sources and localize the leakage current to the inverter side of the transformer. Of course, even the transformer cannot provide complete isolation over all frequencies because of the inter-winding capacitance and other stray capacitances in the transformer. Therefore, even with the transformer in the circuit, it is possible to have high frequency components in the leakage current on the utility side. At the line frequency and low end line harmonics, which are the most concern, the line transformer is able to isolate the two sides very well. The problem with the line transformer is that it increases the size, cost, weight, and losses of the system. Therefore, it is not the ideal choice if only being used for leakage current issues.

Because of the size and weight of the line frequency transformer, the use of transformerless and high-frequency transformer grid-tie inverters are becoming popular in photovoltaic applications with several commercial products available in the U.S. and even more in Europe and Asia [12]. As one would expect, the designs for the transformerless converters are often more complex than the traditional full bridge topology because of the galvanic path between the two sources; often requiring extra switches or specific modulation techniques in order to reduce leakage current. In this section, a few of the major commercial products will be discussed to show how specific manufacturers deal with leakage current. The modulation methods used for all the converters discussed in the chapter will be based on one of the four methods discussed in the previous chapter. This is why in the previous chapter time was spent looking at the different approaches and deriving analytical expressions for each case.

4.1. Standard Full Bridge Topologies

As a starting point, the leakage current associated with the full bridge converter in its standard form will be discussed using the four different PWM methods from the previous chapter. A simple model will be used to formulate the problem, and then from the simple model the system complexity will be increased to account for more system variables. Figure 4-1 shows the PV system used for the simple model. Before proceeding there are a couple specific issues that should be pointed out about this model:

- The utility impedance is represented by a series RL circuit
- The neutral has a solid bond to earth
- The filter for the inverter is a simple 2nd order LC filter with a series resistor to account for the losses of the inductor
- The inductance and resistance in the filter are only on the line side of the utility feed
- The load is a simple resistance connected between the two sources
- The leakage path is modeled as a capacitance and small resistance in series

The amount of leakage capacitance and resistance will vary based on the size of the array and environmental conditions. In [19], the capacitance is approximated to be between 10-50 nF per kW, but is shown to vary substantially with environmental conditions. The value for the PV leakage impedance and passive elements used for this analysis are listed Table 4-1. The PV array and converter were based on a 4.5 kVA design. The utility was assumed to be 10 times larger than the PV system with 5% impedance and an X/R ratio of 5.

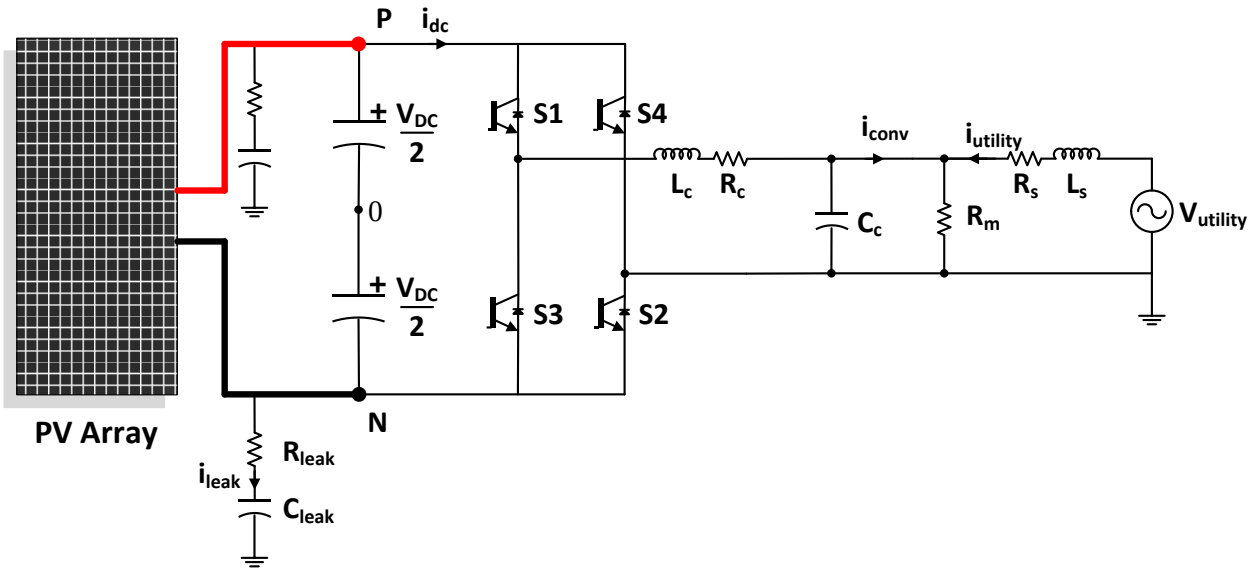


Figure 4-1: PV grid converter asymmetrical filtering ideal case

Table 4-1: Converter and utility impedances

Parameter	Value
C_{leak}	100nF
R_{leak}	0.5mΩ
L_c	100µH
R_c	15mΩ
C_c	15µF
L_s	40µH
R_s	3mΩ
R_m	2Ω

Using the model for the grid-tie converter shown in Figure 4-1, the leakage current can be determined for the four different PWM methods. Before deriving an expression for the leakage, first notice that the leakage voltage is directly related to the phase b duty cycle because of the utility grounding and filtering configuration. Therefore, the model for the leakage path can be simplified to the circuit shown in Figure 4-2, where the leakage source is the phase b voltage with respect to the midpoint of the converter including a DC offset. The leakage impedance is simply the impedance of the PV array and any impedance in the ground circuit. The leakage voltages equations are given by (4-1) and (4-2). From the leakage voltage, the leakage current can be found using the leakage impedance information.

$$V_{Leak} = -\frac{V_{dc}}{2} - V_{b0} \tag{4-1}$$

$$V_{b0} = S_b \cdot \frac{V_{dc}}{2} \tag{4-2}$$

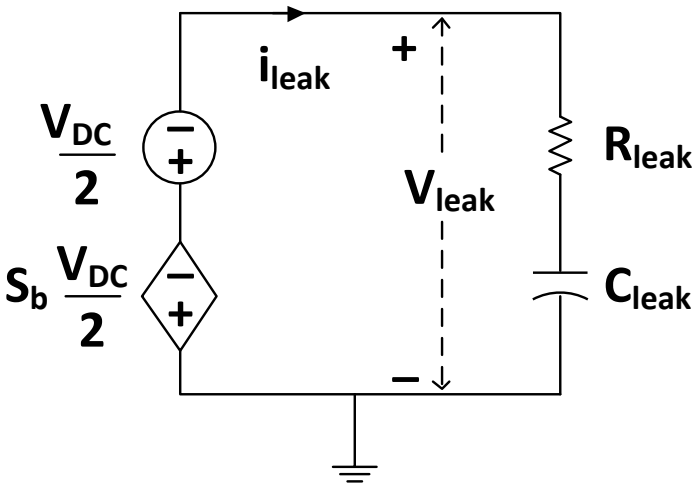
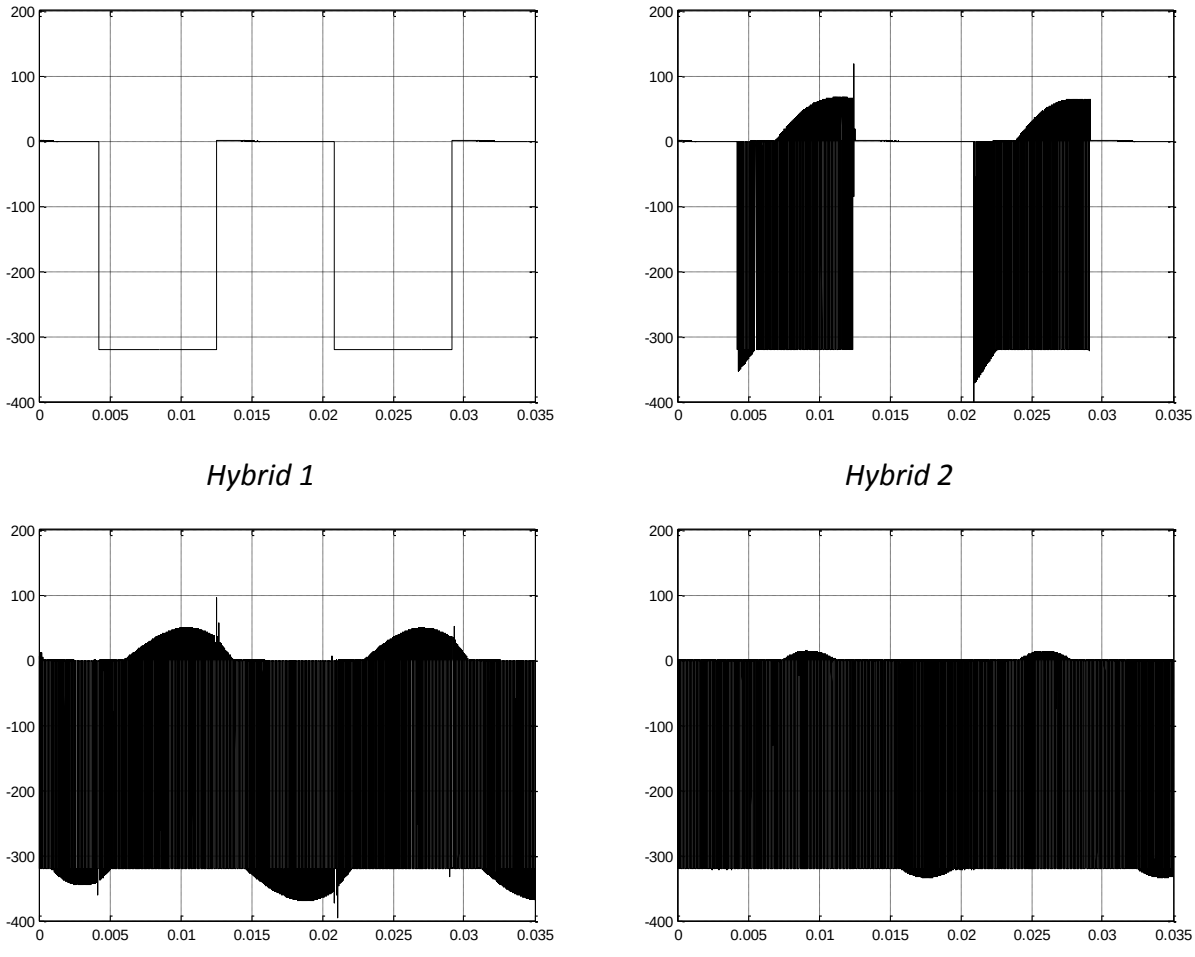


Figure 4-2: Leakage circuit with asymmetrical filtering

The leakage voltages for the four PWM methods discussed in the previous chapter are shown in Figure 4-3. All of the voltage waveforms in their ideal form can be obtained from the expressions for the phase b waveforms from the previous chapter. The waveforms shown in the figure were simulated using Saber. For the first hybrid method, if the phase leg that is switched at the line frequency is connected to the neutral of the utility, then the leakage voltage is simply a square wave. The second hybrid approach produces a waveform that is switched at high frequency for half of the line cycle and then constant for the other half cycle. This approach will of course cause low and high frequency components in the leakage current because of the two different switching sequences. The low frequency components are even harmonics and given in (3-16). For unipolar and bipolar modulation, the two cases have similar spectral waveforms, which is a sinusoidal component at the fundamental frequency in addition to the switching harmonics.

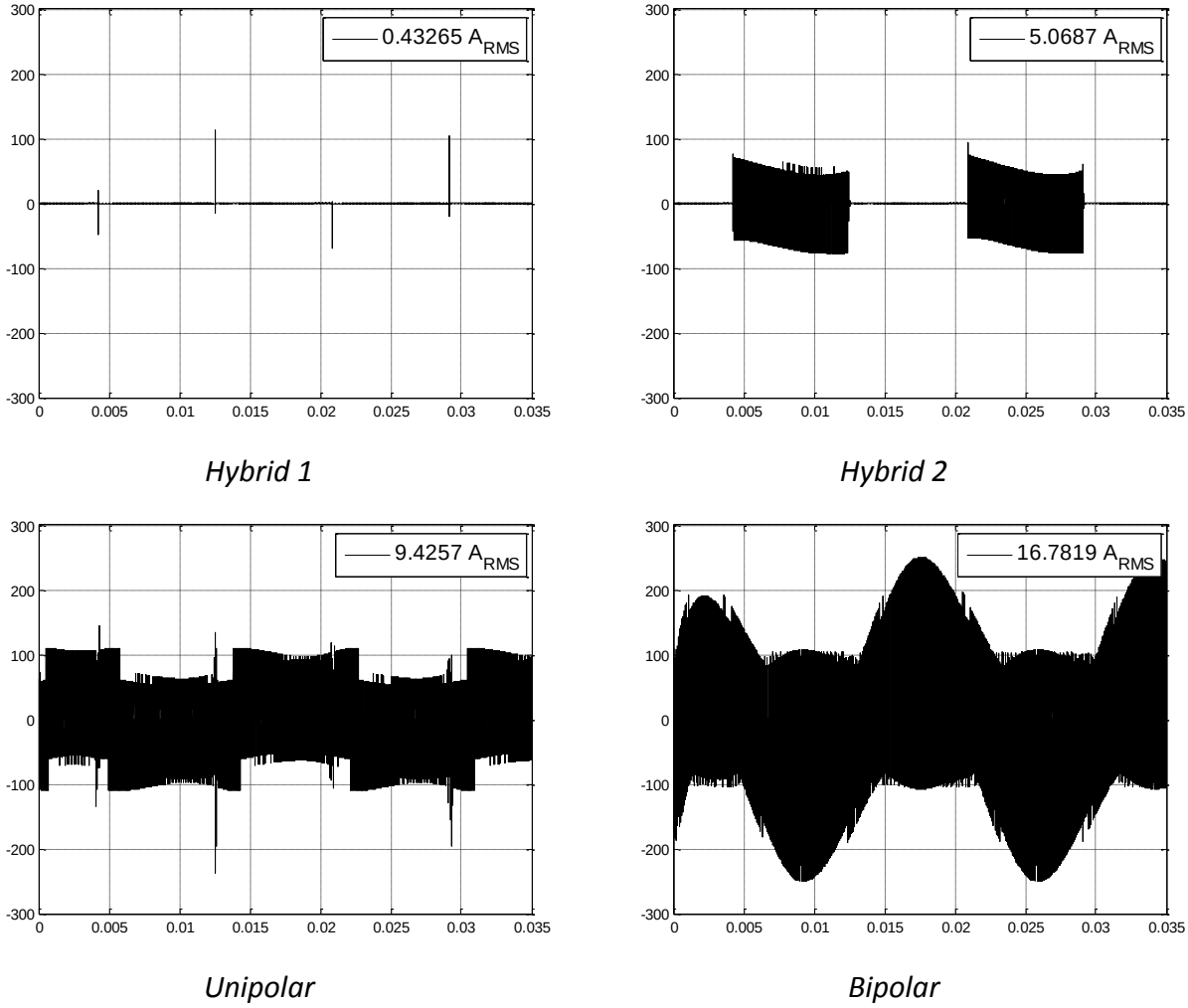


Hybrid 1 *Hybrid 2*

Unipolar *Bipolar*

Figure 4-3: Leakage voltage unsymmetrical filtering ideal case (switching frequency = 20 kHz, line frequency = 60 Hz, and Vdc = 320 V)

With expressions for the leakage voltage, it is possible to solve for the leakage current using the leakage voltage and impedance information. Since the capacitance dominates the leakage impedance, the leakage current is basically equal to the derivative of the leakage voltage. Figure 4-4 shows the leakage current results for the four PWM methods. The rms for each of the waveforms is shown at the top of each graph and is calculated over two line cycles using trapezoidal integration.



Hybrid 1 *Hybrid 2*

Unipolar *Bipolar*

Figure 4-4: Leakage current unsymmetrical filtering ideal case (switching frequency = 20 kHz, line frequency = 60 Hz, and Vdc = 320 V)

For the first hybrid method, the leakage current is zero when the voltage is constant and spikes during voltage transitions. The current spikes are directly related to the voltage magnitude and capacitance and will vary based on the DC bus voltage and PV array capacitance. A larger bus voltage or array capacitance will cause larger current spikes. Even though the rms is calculated for the waveform, rms is actually not the best metric to determine how a ground protection device might respond to this type of event. Although is difficult to know exactly how a leakage current device, such as a residual current device (RCD) or residual current circuit breaker (RCCB), would respond to this type of waveform, the peak current and the ring down is more important than the rms calculation for this waveform. Since most residual current devices use a current transformer around the phase and neutral wires to measure the ground current, it is possible that the transformer may not have the bandwidth to capture the fast current transition. Also, the control and measurement circuitry may have limited bandwidth to respond to this type of event. More will be discussed on this issue in the next section.

Hybrid approach two produces zero current for half of the line cycle and large amounts of leakage current for the remaining half cycle. Notice that because of the high frequency switching in the neutral phase, the difference between the two hybrid approaches is substantial under this source and filter configuration. The traditional unipolar and bipolar methods also have large amounts of the leakage current under this source and filter configuration. Because unipolar, bipolar, and hybrid 2 modulation schemes all have large amounts of leakage current, with large fundamental components, they are not suitable for transformerless PV applications in this configuration. Bipolar modulation has the worse leakage of the four types, with the rms current exceeding 15 A_{rms}.

For a more thorough evaluation of the PV leakage current, the trace and line impedance needed to be included in the analysis. In the real converter installation, the neutral leg of the inverter will be connected to the neutral of the utility through the impedance of the utility cable as shown in Figure 4-5. The impedance of this cable will vary based on the length, size, and configuration of the cabling as well as the environmental conditions. For this analysis, the cabling was assumed to be 25 ft. with the phase and neutral conductor in a bundled configuration. Since the impedance values of the cable will vary based on the installation and configuration, these values should not be viewed as typical but just as an example. The trace connecting the filter capacitor of the converter and the neutral phase leg will also have some impedance, which should also be included in the model. Assuming that the traces are thick and short and the phase leg is near the filter, which is typically the case, this inductance and resistance will be small in comparison to the cable and filter impedances. Figure 4-5 shows the equivalent circuit diagram with the additional impedances. Table 4-2 gives the values for the additional components. All other impedances in the circuit are the same as the previous case and can be found in Table 4-1.

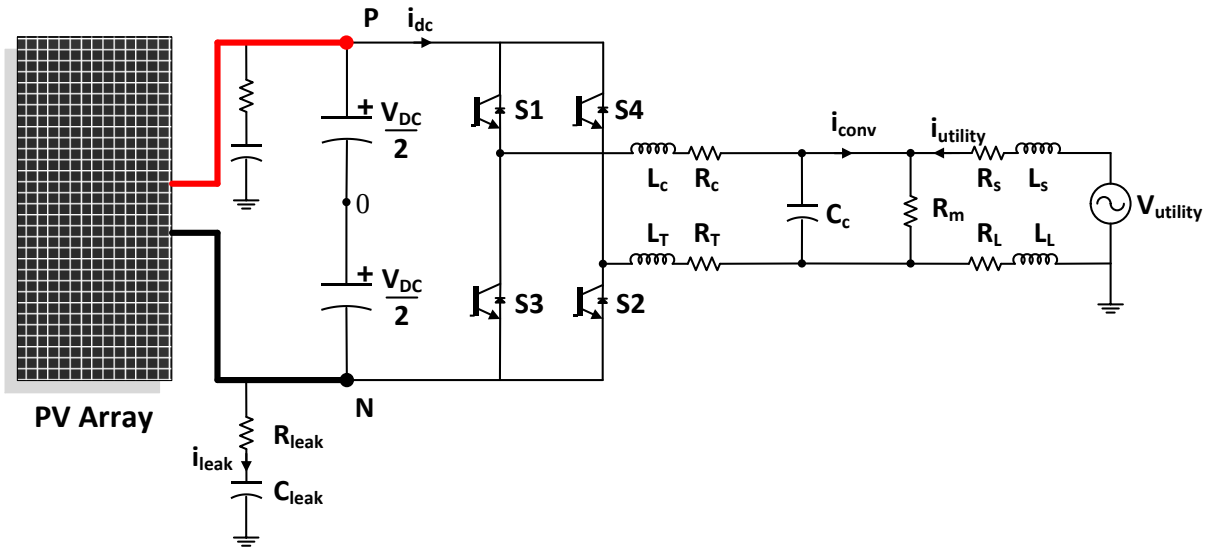
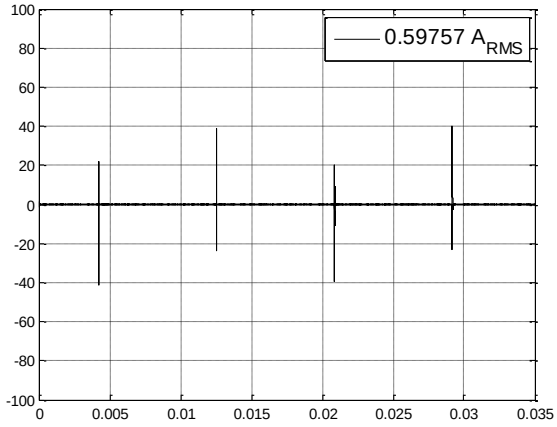


Figure 4-5: PV grid converter unsymmetrical filtering including trace and utility impedance

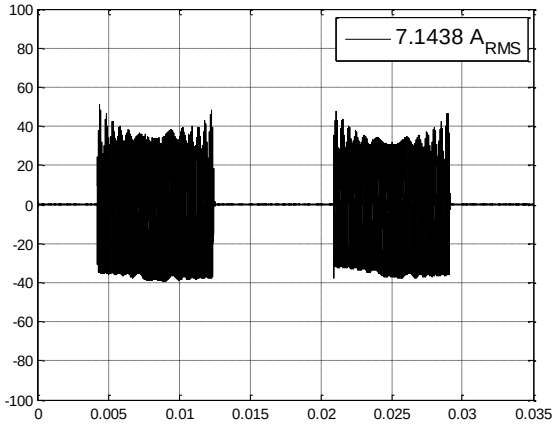
Table 4-2: Trace and line impedances

	Inductance	Resistance
Trace	100nH	1mΩ
Utility	3.5uH	10mΩ

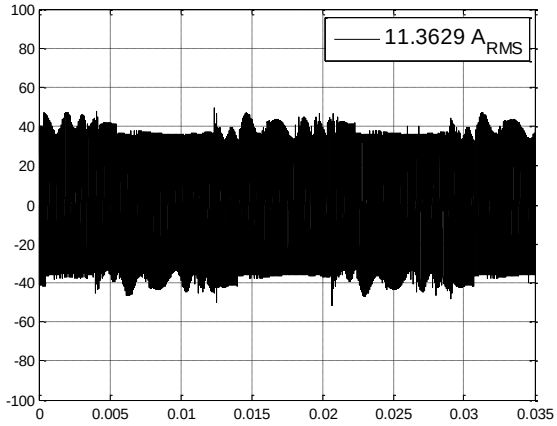
Figure 4-6 shows the leakage current simulations with the addition of the trace and utility conductor impedance. As can be seen in the figure, all of the rms currents increase except for bipolar modulation. Although it is evident when comparing Figure 4-4 and Figure 4-6 that the additional impedance does change leakage current, the waveforms and rms current are only slightly different than the ideal case.



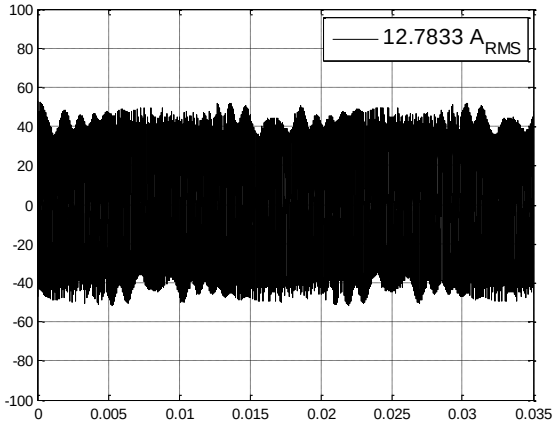
Hybrid 1



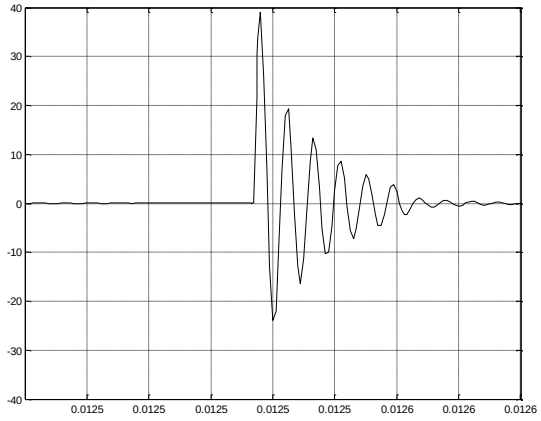
Hybrid 2



Unipolar



Bipolar



Switching transient

Figure 4-6: Leakage current unsymmetrical filtering ideal case (switching frequency = 20 kHz, line frequency = 60 Hz, and Vdc = 320 V)

The main difference between the two cases is the peak value of the current and the oscillatory transient that occurs during switching. Since the hybrid 1 approach is the only approach that produces reasonable leakage results under this source and filter configuration, it will be the only method discussed in more detail. Although the peak value was reduced by more than half when the line and trace impedance were included in the hybrid 1 approach, the total rms leakage current with the addition of the line and trace impedance is significantly higher. The reduction in the peak current is easily explained with the inclusion of the inductance in the neutral conductor. Since current cannot change instantaneously through the inductor, the peak current reduction is expected when compared to the case with no inductance. However, the current reduction does not explain why the rms current would increase. Further investigation of the waveform reveals that during the switching transition an oscillatory transient is created because of the RLC circuit formed between the line and trace impedance and the leakage capacitance of the panel. The transient frequency and peak current are given by (4-3) and (4-4). Since the trace impedance is typically much smaller than the cable impedance, the transient frequency can be further reduced accounting only for the array capacitance and line impedance. The response damping will depend on the resistance of the cable and trace.

$$f_{leak} = \frac{1}{2\pi}\sqrt{\frac{1}{L \cdot C} - \left(\frac{R}{2L}\right)^2} \approx \frac{1}{2\pi\sqrt{2 \bullet \left(L_L + L_T\right) \bullet C_{leak}}} \approx \frac{1}{2\pi\sqrt{2 \bullet L_L \bullet C_{leak}}} \tag{4-3}$$

$$i_{peak} = \frac{V_{DC}}{\omega \cdot L} \cdot e^{\frac{-R \cdot \pi}{L \cdot \omega}} \tag{4-4}$$

Unfortunately, the line impedance and leakage capacitance cannot be controlled by the inverter designer. The leakage capacitance will vary based on the size of the PV array and weather conditions, and the cable impedance will vary based on the length and configuration of the cable. Since these impedances are out of the designer's control, the best the designer can do is to understand how a ground fault protection device, such as an RCD or RCCB, might respond to this type of event and also look at different impedance scenarios.

4.1.1. Leakage and RCD Standards

While there has been a great deal of research on different inverter topologies and filtering techniques to minimize leakage current, the actual response of the RCD to PV leakage current has not been addressed much in literature. In fact, most of the literature on the subject only addresses the general rms operating specifications. The IEC 60755 standard that describes the general operating requirements for residual current devices only addresses frequencies below 1000 Hz and low frequency transient events like the ones seen in line commutated rectifiers. Since the transient behavior for the PV is much higher than the transients in IEC 60755, the general operating standards are not very useful for answering PV compatibility questions. The surge requirements for residual devices on the other hand, which are defined in IEC 61008, are similar enough to the leakage current waveforms that they can be used as a starting point for predicting the device behavior. It should be noted that while the surge requirements are a good starting point when trying to predict compatibility issues testing is still needed to validate speculations.

The surge requirements for residual current devices are in place to avoid nuisance trips during lightning strikes, and are tested using the standard combination and ring waveforms defined in IEEE C62.41. The IEEE combination wave is a unipolar surge wave characterized by its open and short circuit characteristics, with the magnitude of the voltage and current defined by the equipment exposure level to lightning events. IEC 61008 recommend testing RCDs to the 6 kV open circuit and 3 kA exposure level. At this level, the open circuit voltage has a 1.2 µs rise front and a 50 µs duration, and the short circuit current waveform has a 8 µs rise front and a 20 µs duration. The duration is defined as the time between the virtual origin and the 50% amplitude point on the tail. Since the waveform is unipolar, the correlation between the PV leakage current and the combination waveform is not very clear and therefore will not be used to try to predict possible nuisance tripping. The IEEE ring wave on the other hand, is a sinusoidal waveform with an exponential decay that is very similar to the PV leakage current waveforms seen with the hybrid approach. The ring wave used to test residual current devices has a 200 A peak current with a 100 kHz ring frequency. While the ring frequency and peak current are very important for this analysis, the decay rate of the waveform is equally as important. Unfortunately, the ring waveform decay rate in IEEE C62.41 is not defined as a ratio of the resistance and inductance in the circuit, which would be more convenient for this analysis, but is defined as range of acceptable decay percentages for the first three peaks of the current waveform. This requires the percentage information to be extracted from the waveforms. For this analysis, the decay rate was close enough to the accepted standard values that this was not an issue. However, this might not always be the case for all impedances and should be considered in the analysis.

Since in (4-3) and (4-4) the frequency and peak of the transient current are directly related to the resistance, capacitance, and inductance, the first step is to determine the boundary conditions for the line and leakage impedance. The authors in [19] showed that the array capacitance varied between 10-50 nF/kW based on the environmental condition, so as a starting point, the boundaries for the capacitance can be found based on the size of the PV system. Next the cable impedance can be varied to account for the different possible lengths of cable. In this study, the cable inductance and resistance were varied linearly accounting only for changes based on the length of the cable. Figure 4-7 show the maximum peak current vs. the maximum frequency for all of the different inductance and capacitance configurations.

It should be noted that for the case with no cable impedance, Figure 4-4, the current should be very large based on (4-3) and (4-4). The reason that this is not the case is because of simulation the step size. In (4-3) and (4-4), the calculations are for a continuous system and do not account for the simulation step size for discrete systems. For the case in Figure 4-4, the simulation step size was 500 ns, which is why the current was so low for the no impedance case. In conclusion, if the steps size is much less than the transient frequency, the simulations and closed form solutions should be in close agreement. Figure 4-8 shows the simulation response with the largest inductance, resistance, and capacitance case. The result is in agreement with Figure 4-7, which would be the first point on the first curve (teal waveform).

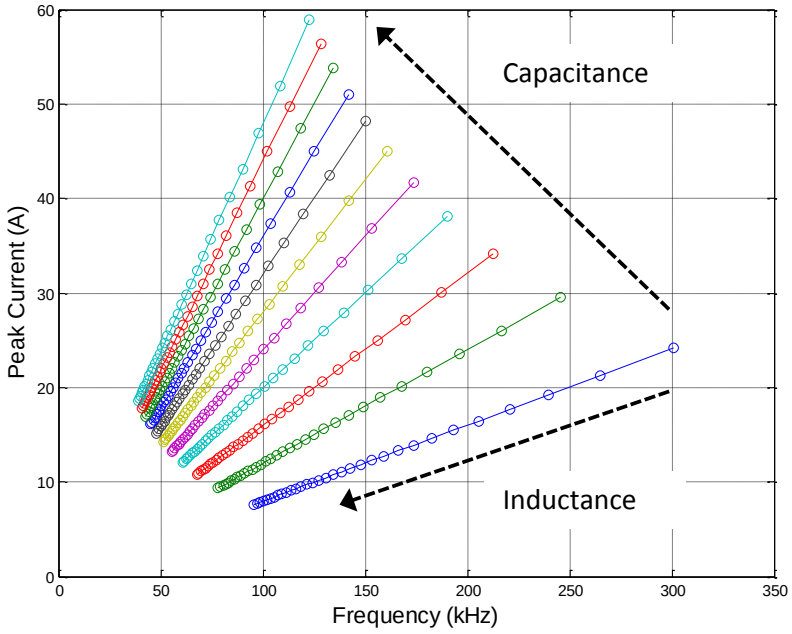


Figure 4-7: Peak current vs. ring frequency

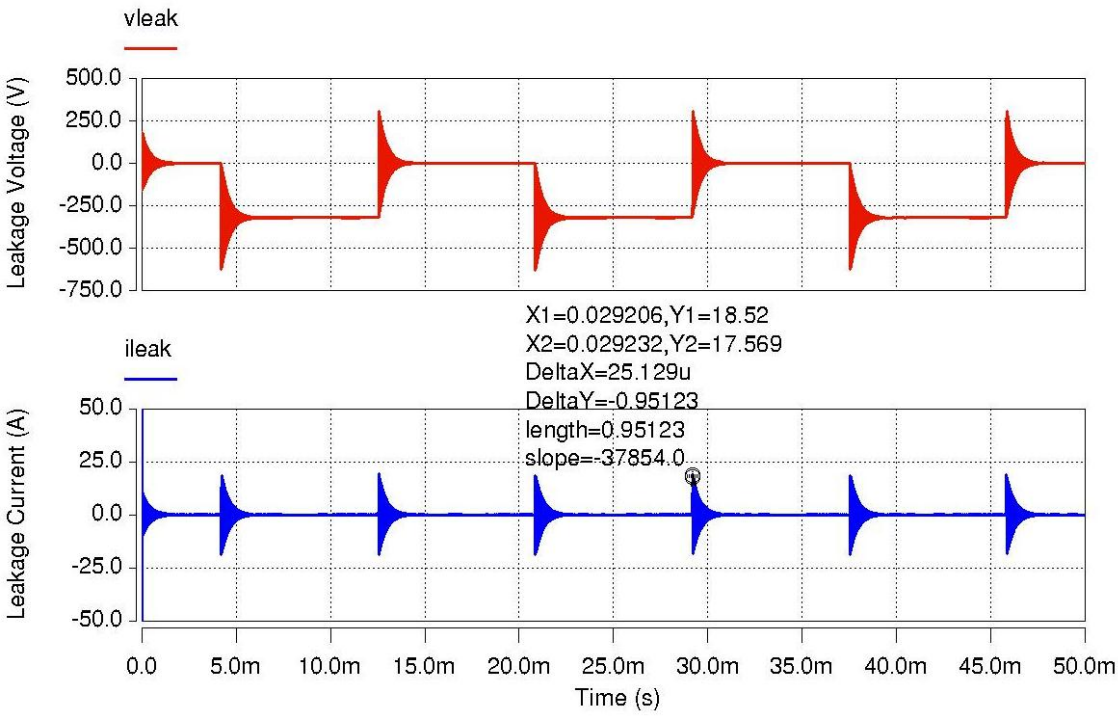


Figure 4-8: Simulation case L_L = 35uH R_L = 100m C_{Leak} = 240nF

Anything to the right of 100 kHz line in Figure 4-7 should not trip the RCD since the peak current is less than the standard 200 A test current, and since the event is greater than 100 kHz. Anything left of the curve is questionable since the duration is longer than the test waveform. In [23], the authors showed that for the surge combination waveform the duration has a significant impact on the tripping limit for the RCD. In fact, with a fall time duration increase of 250% the RCD tripped at 970 mA vs. the nominal 3000 A limit. If the RCD circuitry has a similar response to the ring wave, then anything left of the 100 kHz will more than likely cause the RCD to trip. In order to work around this issue, the inverter designers may wish to impose a limit on the cable length to the inverter so that any transients that occur are greater than 100 kHz. For our example, this would require keeping the cable inductance below about 5 µH assuming the worst case capacitance for a 4.5 kW array.

It is easy to determine the inductance requirement for different size arrays based on maximum capacitance of the array and the 100 kHz threshold frequency. From the inductance, the length of the cable can be calculated based on the installation, configuration, and geometry of the cable. Unfortunately, the installation is the one thing that the designer has very limited control over. However, if the designer is concerned that the installation will be problematic for a residual current protection device, then some installation requirements may be required to ensure proper operation. The sizes of the conductors are known by the designer based on the inverter size. In order to calculate the length of the cable for this analysis, equation (4-5) was

used, which is based on a two conductor model found in [11]. This approach assumes two equally sized round parallel conductors with one of the conductors acting as the return conductor. In the analysis, the spacing between the conductors was assumed to be four times the radius of the conductor.

$$L = 0.004 \cdot l \cdot \ln\left(\frac{d}{r} + \frac{1}{4} - \frac{d}{l}\right) \tag{4-5}$$

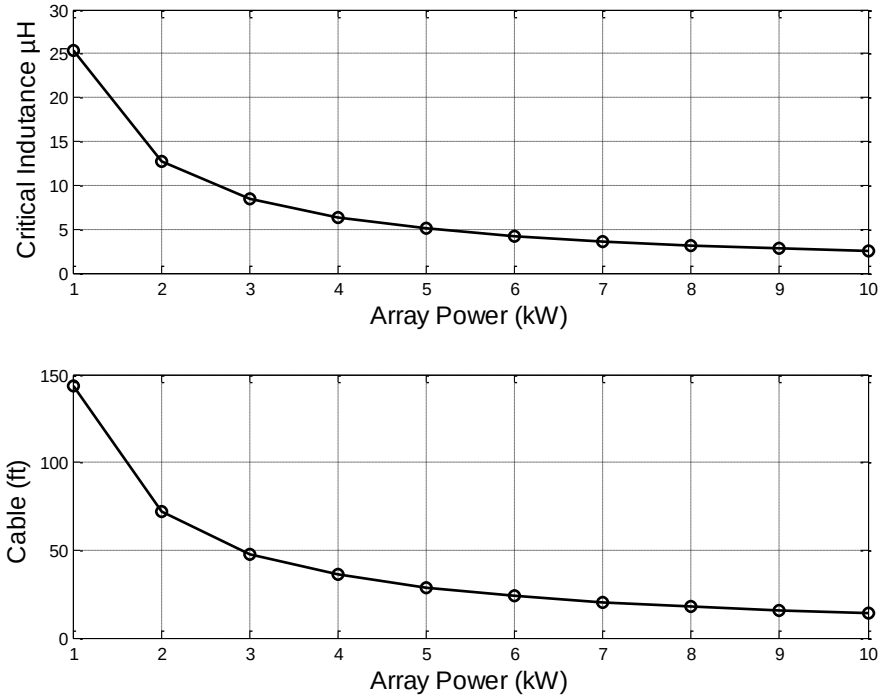


Figure 4-9: Critical inductance vs. power and length vs. power

Figure 4-9 shows the critical inductance and length for 1-10 kW power levels. Since above 10 kW the converters are more likely to be three phase, especially at lower voltages, the size range was kept below 10 kW for this analysis. The results clearly show that for systems smaller than 3 kW, the cable length should not be a problem because of the smaller leakage capacitance of the panel. For the larger systems, the designer may need to put restrictions on the cable length if this topology and switching scheme are to be used; although above 6 kW the restrictions on the length are not very practical. In conclusion, assuming that the length is less than critical lengths in Figure 4-9, the hybrid 1 modulation scheme with the standard full bridge topology could be used for transformerless grid-tie system.

From these results it is apparent that this topology and modulation scheme will not work for all installation schemes. For example, in a split-phase utility configuration, unless the size of the utility is much greater than the size of the inverter, the impedance of the utility will cause low frequency transients that will likely trip the RCD because of the large leakage inductance of the transformer. For the split-phase configuration, the leakage frequency can be calculated using (4-6). In (4-6), if the source impedance is assumed to be much larger than the wiring impedance between the source and converter, then the equation can be reduced to only include the leakage inductance of the source.

$$f_{leak} \approx \frac{1}{2\pi\sqrt{2\bullet\left(L_s + L_L \,||\, L_s + L_L\right)\bullet C_{leak}}} \approx \frac{1}{2\pi\sqrt{L_s \bullet C_{leak}}} \tag{4-6}$$

Figure 4-10 shows the case when the utility base is the same size as the converter rating with an X/R ratio of 5 and 5% impedance. The transient frequency in this case is approximately 16 kHz. This is much less than the 100 kHz ring frequency used in the surge standard and will likely cause the RCD to trip. In order to have a ring frequency greater than 100 kHz, the source would need to be almost thirty times the size of the converter. While this might be the case in some installations, it is not safe to assume that this will always be the case. Therefore, the hybrid 1 modulation scheme with the standard full bridge inverter is not suitable in split-phase utility configurations. These results also show that if the user decides to install a transformer between the inverter and utility that this modulation scheme might also have problems because of the additional leakage impedance of the transformer. While ideally the transformer would isolate the two sides, with transient frequencies in the 10-100 kHz range the coupling between the primary and secondary could become an issue. In fact, at these frequencies shielded transformers may need to be used to provide higher levels of isolation.

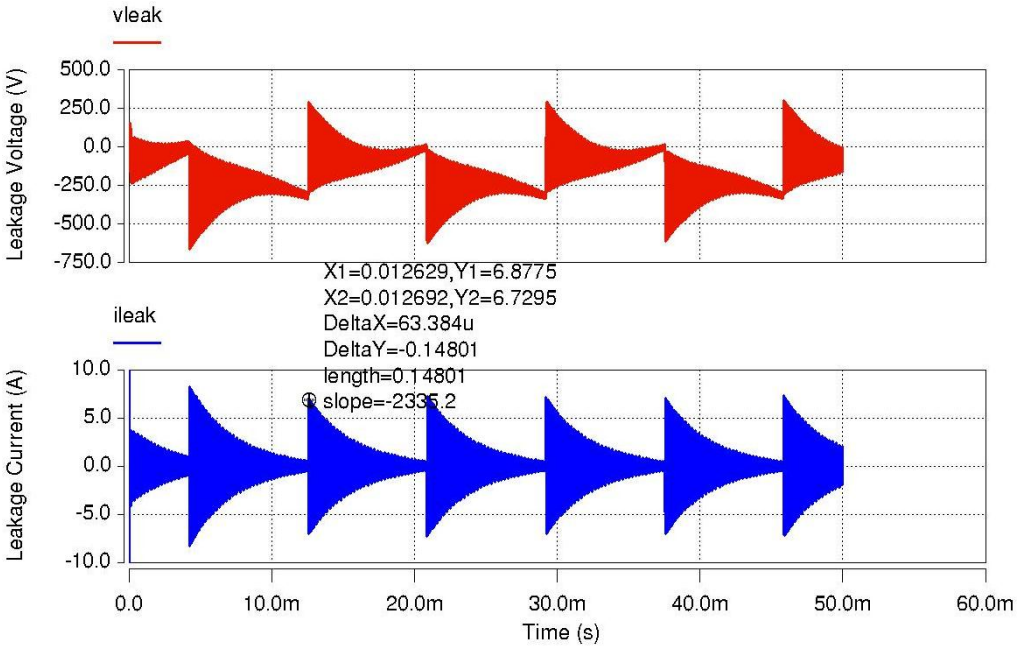


Figure 4-10: Simulation case L_s = 424.5uH R_s = 30mΩ C_{Leak} = 240nF

4.1.2. Distributed Filter Case

Until this point, the filter inductance was only on the phase conductor of the converter. However, distributing the inductance between the phase and neutral is a more common practice for single phase grid tie converters. By distributing the inductance, the voltage swings across the filter are divided among the two inductors. Also, the PV high frequency voltage between neutral and ground is reduced for some converter topologies and PWM schemes [16]. It should be noted that this was the case for the converter in [16] and some other designs. However, this is not necessarily true for all converters and modulation schemes as will be shown. Figure 4-11 shows the circuit for the split filtering configuration. The impedance of the trace from the previous analysis was excluded since it is miniscule when compared to half of the filter impedance. In most of the leakage current research that has been done for PV applications, the filter is distributed between the phase and neutral of the converter as shown in this figure. Accordingly, most of the leakage analysis is with the filter distributed in this way. Distributing the filter inductance in this way has a major advantage for bipolar modulation but a major disadvantage for hybrid 1 modulation. Therefore, it is not necessarily the ideal inductor configuration for all modulation schemes.

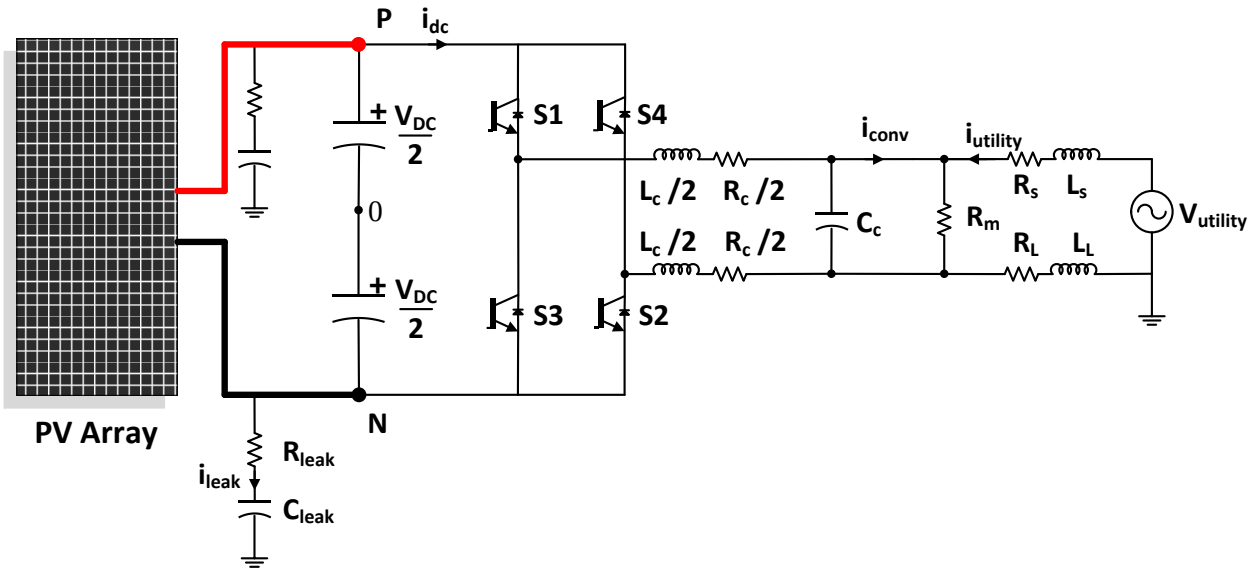
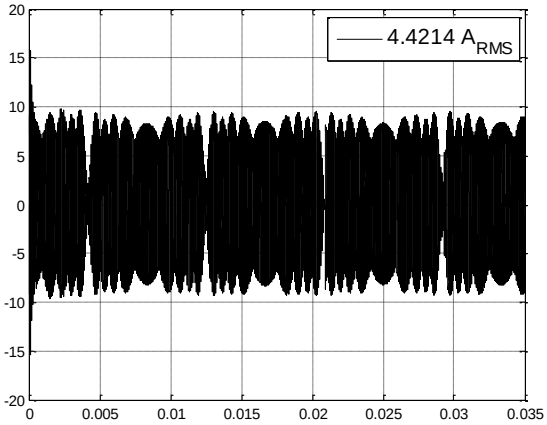


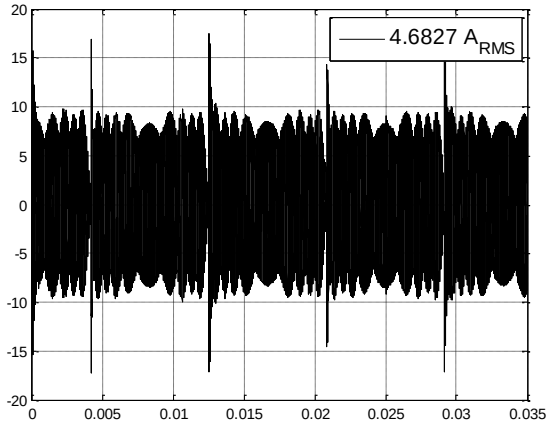
Figure 4-11: Full bridge distributed filter configuration

The bipolar and unipolar modulation results are typically what are shown in literature when discussing leakage current. To the author's knowledge, the two hybrid approaches have not been shown for leakage current comparisons purposes. In most literature on the subject, the leakage current in this configuration is shown to be attributed to the common mode path and common mode voltage of the PWM method. Since it was shown in the previous chapter that for bipolar modulation there is no common voltage, the results would suggest that leakage current is indeed a function of the common mode voltage and the common mode path in this configuration. In a similar manner, the unipolar modulation results, which had twice the common mode voltage for odd switching harmonics, would suggest that the common mode voltage is contributing to most of the leakage current in this configuration.

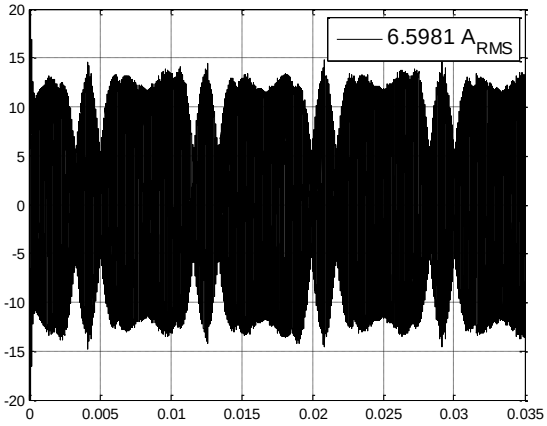
In conclusion, distributing the filter inductance only has a real advantage for bipolar modulation since the other PWM schemes have common mode voltage. In fact, this actually makes the first hybrid approach worse than when the inductor is only on a single leg of the filter. As discussed in the last chapter, bipolar modulation produces high losses and high ripple limiting its use for grid-tie converters. Therefore, even though the leakage current is low this is not the ideal choice for grid-tie converters.



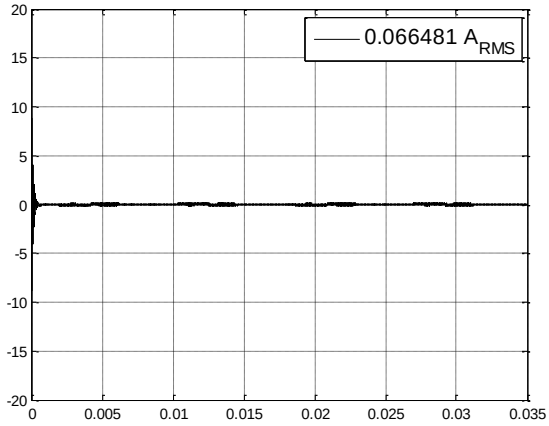
Hybrid 1



Hybrid 2



Unipolar



Bipolar

Figure 4-12: Leakage current symmetrical filtering ideal case (switching frequency = 20 kHz, line frequency = 60 Hz, and Vdc = 320 V)

4.1.3. NPC-Full Bridge Hybrid

The full bridge topology can be combined with the active neutral point clamped converter to form a hybrid converter as shown in Figure 4-13. To the author's knowledge, this converter has not been presented in literature on this subject. This converter has some of the benefits of both the active neutral point clamped and the full bridge topology. A few of the advantages and disadvantages are listed below:

Advantages

- Full utilization of DC bus
- THD improvements compared with full bridge topology
- Lower conducted emissions compared with full bridge topology
- Only one phase leg is clamped
- Four quadrant operation

Disadvantages

- Eight switches and anti-parallel diodes
- More complicated modulation
- More control and protection
- Higher conduction losses
- Difficult to implement with analog circuitry

All of the modulation schemes discussed in this chapter and the previous can be used with this converter using the vector approach by distributing the switching events accordingly. In the full bridge analysis, it was shown that if the filter inductance is only on the phase conductor, then hybrid 1 is the only scheme that produces acceptable leakage current, and when the filter is distributed between the phase and neutral conductor only bipolar modulation is acceptable. To further illustrate how this converter works; the hybrid 1 approach will be discussed in more detail under the asymmetrical filtering condition.

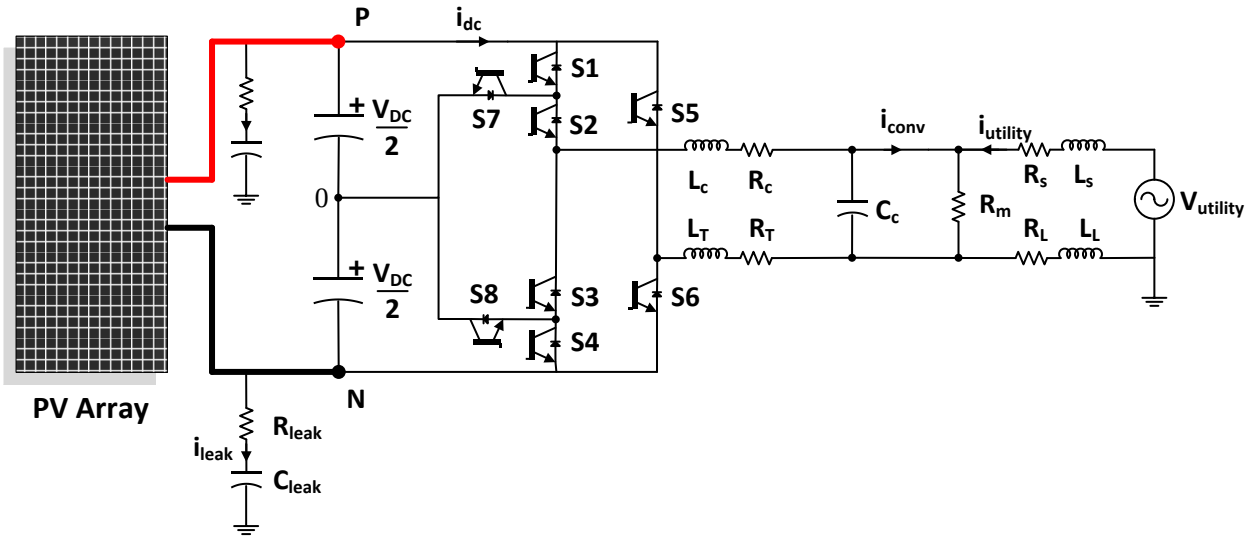


Figure 4-13: NPC-Full Bridge Hybrid

Instead of only having two sectors for the vector approach, the modulation sequencing is divided into four sectors, two positive and two negative. The two outer sectors are identical to the full bridge topology and are switched in the same manner as the hybrid 1 approach discussed in the full bridge section of the previous chapter. The two inner sectors take advantage of the midpoint connection, so switches S7 and S8 in Figure 4-13 are used. The selection of S7 and S8 depends on the polarity requirements for the output voltage and are used when the output voltage is less than the half of the total DC link voltage. Figure 4-14 and Figure 4-15 show the four switching patterns using the hybrid 1 modulation approach.

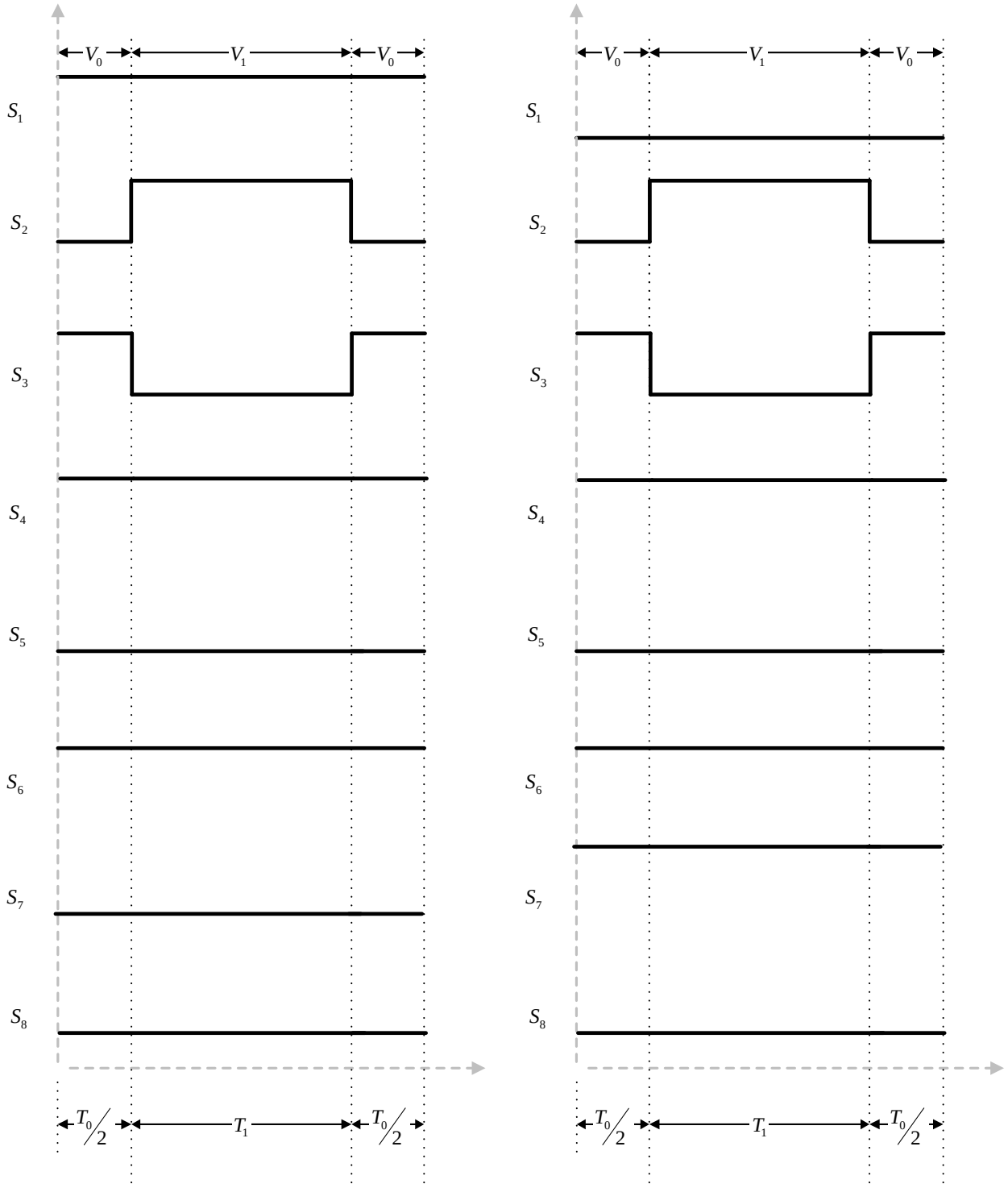
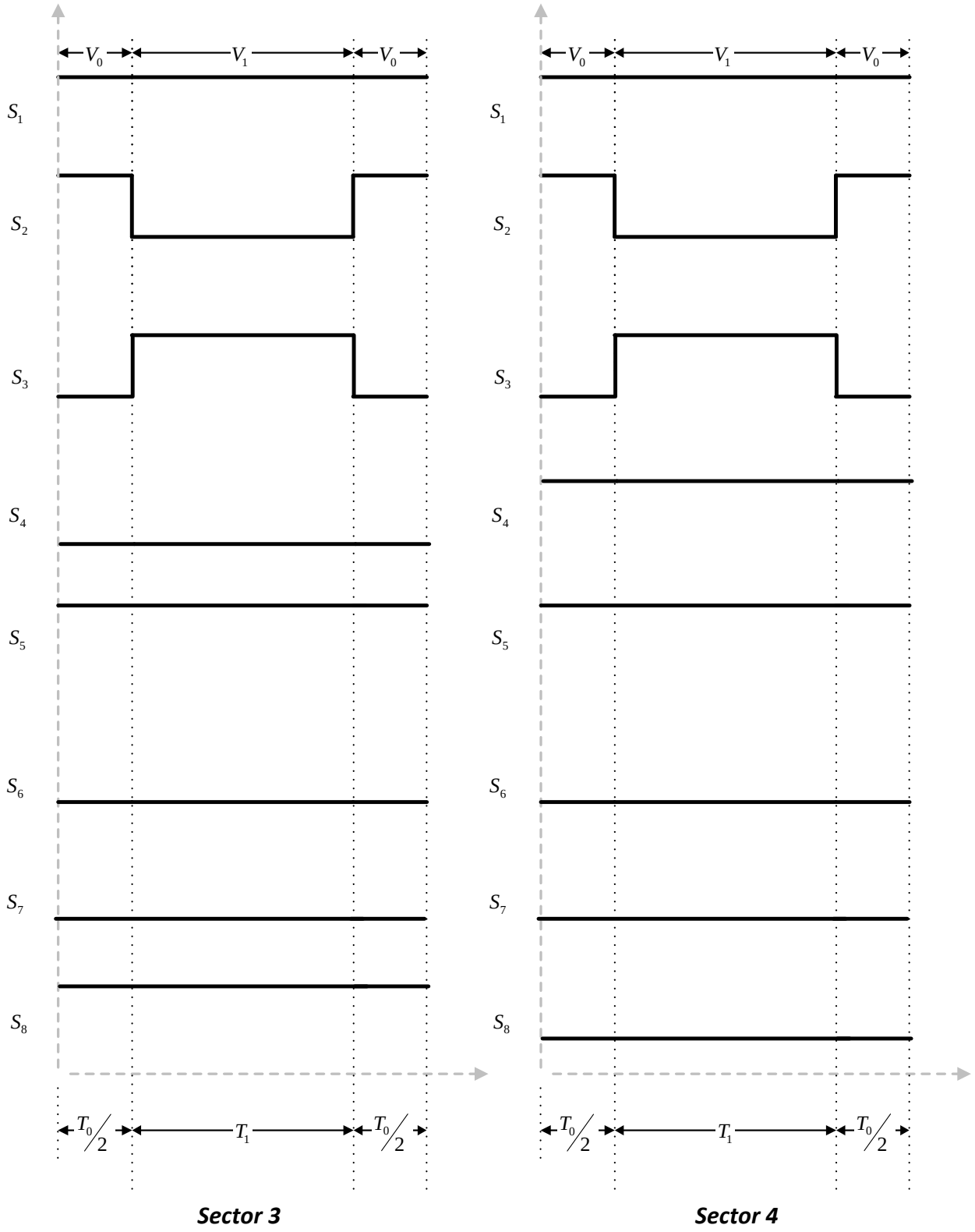


Figure 4-14: NPC full bridge hybrid sector 1 and 2 switching



Sector 3 ***Sector 4***

Figure 4-15: NPC full bridge hybrid sector 3 and 4 switching

During sectors 1 and 4, switches S2 and S3 are switched to produce the required zero and active vector while the remainder of the switches remain in a constant state. In sector 1, since the active vector is PN switch S6 is on while switch S2 is modulated to produce the required active and zero vector. The zero vector in sector 1 is NN, so S3 is complemented to switch S2 to avoid shoot-through and also allow for bi-directional current flow during the zero state. In sector 4, the active vector is NP so S5 is on while switch S3 is modulated to produce the required active and zero vector. Again, in order to avoid shoot-through and provide bi-directional current flow during the zero state (PP), switch S2 is switched in complement of switch three. It should be noted that during sectors 1 and 4, since S7 and S8 are a combination of a switch diode, they must be off to avoid shorting the DC bus. The user may decide to replace switches S7 and S8 with diodes if they are not concerned with four quadrant PQ operation. During sectors 2 and 4, switches S2 and S3 are also switched at high frequency to produce the required active and zero vectors. In sectors 2 and 3, the midpoint voltages are used requiring switches S7 and S8 and S1 and S4 to be turned on and off accordingly. Figure 4-16 shows the switching events and the corresponding sectors over two line cycles. It should be noted that in the modulator used to generate Figure 4-16 the outer sector are 1 and 3 and the inner sectors are 2 and 4.

It is evident from the switching diagrams, that even though there are eight switches within the converter, six of the eight are switched at line frequency. Only switches S2 and S3 are switched at high frequency. This means that the switching losses are not distributed equally among the switches and that these devices will require more cooling than the remaining switches because of the additional switching losses. Also, it is clear that the loss requirements for the remaining six switches are different than switches S2 and S3. For the devices switching at line frequency, devices with low conduction losses are the optimal choice since the devices only switch at the fundamental frequency. For switches S2 and S3, the devices will need low switching losses as well.

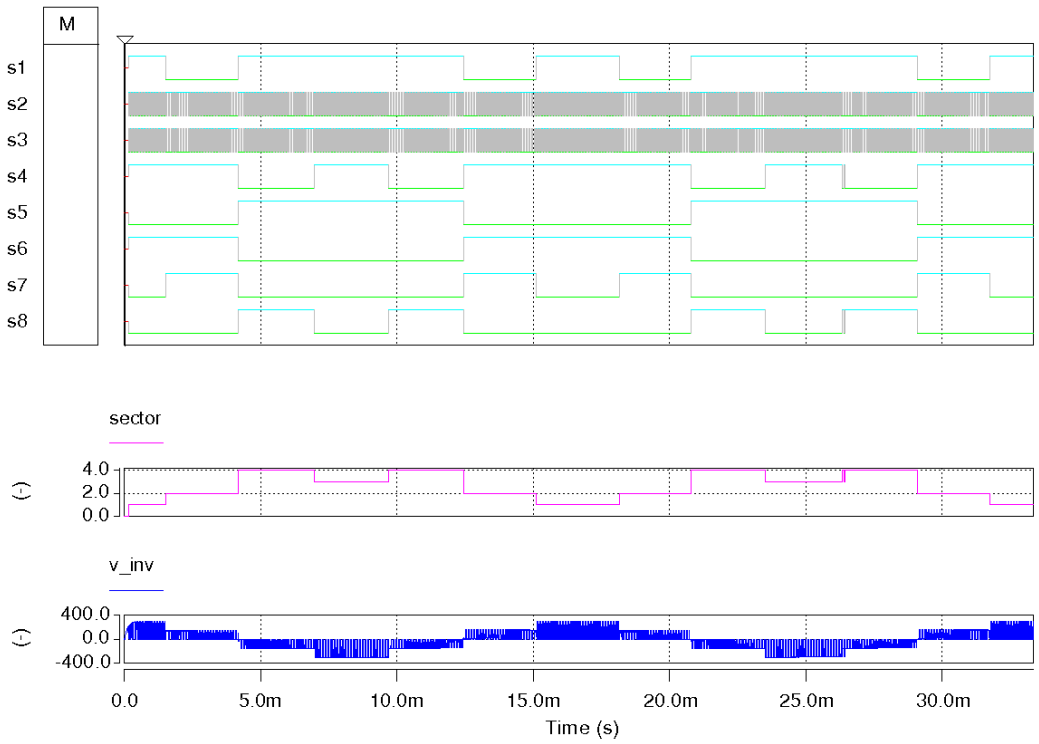


Figure 4-16: NPC full bridge hybrid two line cycles

The combination of the hybrid 1 modulation scheme with the ANPC-Full bridge converter is an output waveform that is a three level unipolar waveform. Since with the hybrid converter the output voltage is three levels, the THD and conducted emissions from the converter are lower than the two level cases, which means that smaller filtering can be used with this topology. The analysis relating the oscillatory transient during polarity reversal to the RCD nuisance tripping is also relevant with this converter configuration. In fact, the peak and frequency for this converter topology are exactly the same as the two level case. Therefore, all of the equations and relationships developed for the two level case are also applicable for this converter. This also means that the same inductance and cable requirements from the previous analysis apply to this converter. Since from the transient stand point this converter is the same as the full–bridge topology, it is clear from the previous analysis that the size range and utility configuration is limited for PV applications. Therefore, even if the additional cost or complexity is not considered, the converter with this modulation scheme is still limited for PV applications. However, in non PV applications, the initial analysis of the converter shows that this could have some major benefits for standard inverter applications. One such case would be in dual conversion uninterruptible power supplies (UPS) used for data centers. Although not implemented by the author, it also might be worth looking at a bipolar scheme with a distributed filter configuration for this topology in PV applications.

4.2. Commercial Products

4.2.1. Full Bridge

It was mentioned at the beginning of this chapter that commercial transformerless converters are available, so it is important to mention how these commercial products deal with leakage current. Transformerless converters are mainly found in Europe and Asia and only recently have manufacturers extended their product line into the U.S. [12]. The U.S. has been a little slower to adopt the transformerless topology since old NEC standards require galvanic isolation. All transformerless converters are designed to work with leakage protection devices, so this section will only focus on topologies and switching techniques used in these converters. Of course, with all the techniques mentioned so far, the leakage current could be reduced with additional filtering. However, additional filtering increases the size, weight, cost, and losses of the converter, so this approach to reducing leakage current is not the ideal solution. In fact, the trend is to try to reduce the leakage current with the topology and switching rather than with filtering. While there are many different variations of grid-tie converters on the market, the full and half bridge topology are the basic foundation for all the variations. The full bridge topology was the focus of previous discussions, so this will be the starting point for this discussion. Next, the half bridge topology and variants of it will be addressed. For all the different converters, the advantages and disadvantage will be discussed.

SMA Solar Technology's H5 converter is an extension of the full bridge topology that uses an extra switch on the positive connection of the DC link [13]. Figure 4-17 shows the H5 topology with an LC filter connected to the utility. The H5 converter is controlled using the hybrid 2 PWM scheme and opening the dc link switch during the zero state. Opening the switch during the zero states isolates the converter and forces the leakage voltage from the converter to float during the transition. Since the voltage is floating when the converter is in the zero state, there are topologies like FB-DCP [24] that add additional switches and diodes to force the voltage to zero during the zero states. The advantages and disadvantages for the H5 topology are listed below:

Advantages

- Ideally zero leakage current from the converter
- High efficiency
- Unipolar PWM scheme
- No reactive power exchange during zero transitions

Disadvantages

- Extra switch increases complexity of design
- Extra switch increases switching and conduction losses
- Difficult to implement with analog circuitry

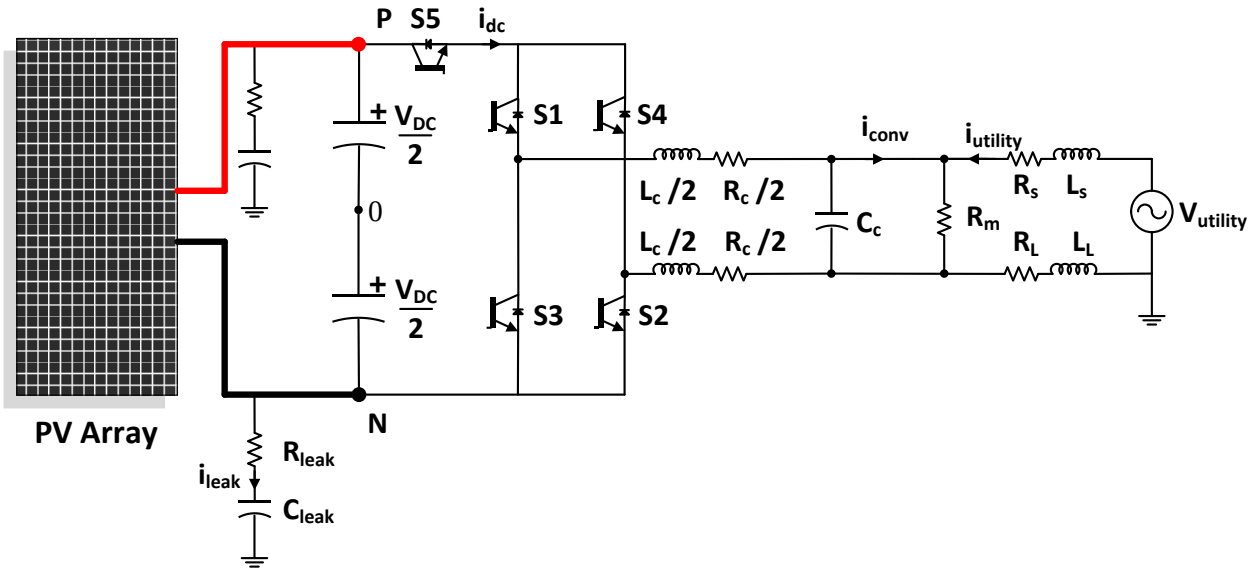


Figure 4-17: SMA H5 converter

The vector diagram for the H5 switching is shown in Figure 4-18. Notice that the zero state for both sectors is always S1 and S4 high and that S5 is always off during the zero state conditions. Since S5 is open during the zero states, this removes the DC Bus from the leakage path. It should be noted that in order for the converter to work in this configuration, the zero states must be chosen in this manner (PP). It is clear from the diagrams that S5 switches at high frequency in both sectors and is the complement of the phase leg that is being switched during each sector. Since S5 is operating in both sectors and current must travel through the switch or diode, it should not be surprising that this scheme has higher switching and conductions losses than the traditional full bridge converter.

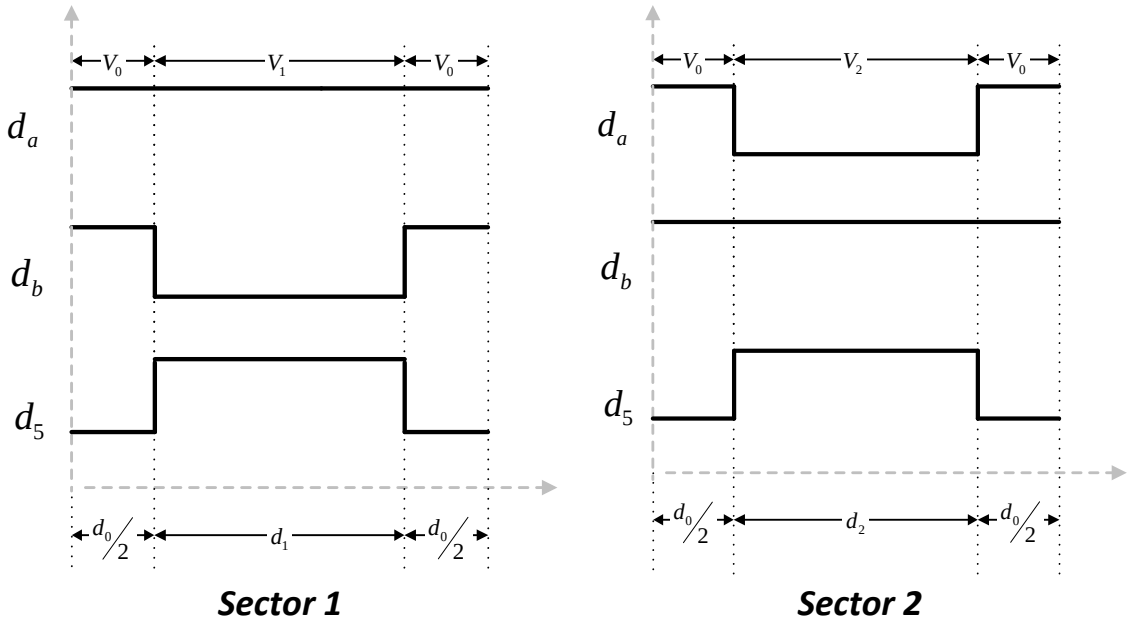
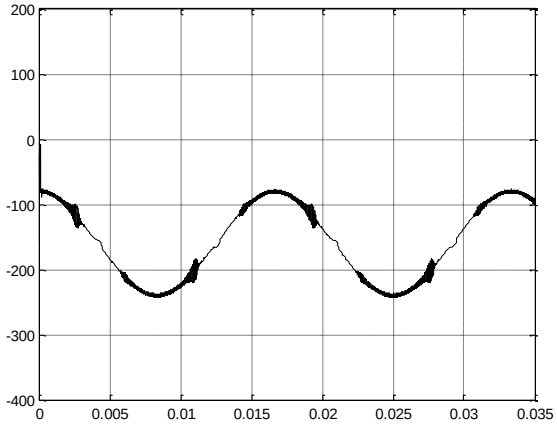


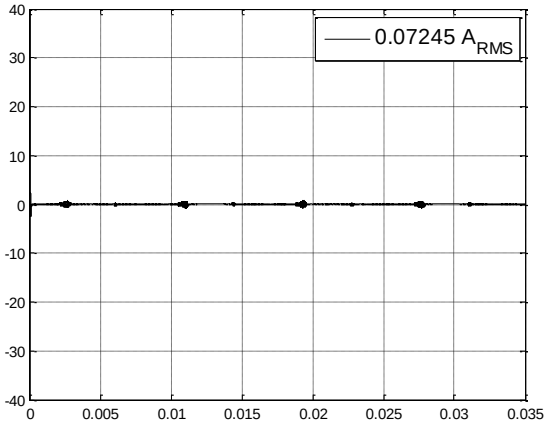
Figure 4-18: H5 switching diagram

The leakage results for two cases were simulated and are shown in Figure 4-19. The symmetrical case is when the filter inductance is distributed equally among the phase and neutral of the converter, which is shown in Figure 4-17. In this case the leakage voltage is for the most part a sinusoid at the fundamental frequency. This sinusoidal leakage voltage is contributed to the common mode voltage of the utility. Since the neutral of the utility is solidly grounded, the common mode voltage of the utility is equal to half of the differential voltage. [15]. The high frequency ripple in the waveforms is mostly contributed to the unbalance in the utility impedances on the phase and neutral of the utility. Since the utility is solidly grounded in the test case, the leakage reactance and series resistance of the utility transformer is only on the phase of the utility, which is why there is an impedance mismatch between the phase and neutral. It is worth noting that if the converter is connected line to line on a split-phase utility, that the fundamental leakage voltage is ideally zero since the utility common mode voltage is zero for this case. Figure 4-20 shows the spit-phase leakage current and voltage when the filter inductance is distributed between the phase and neutral conductor.

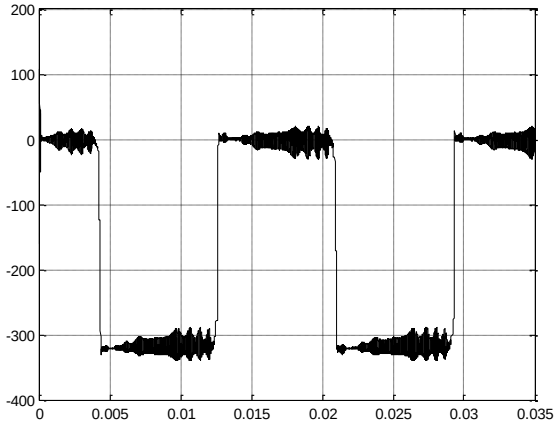
Since the converter filter configuration is not mentioned in the literature for the H5, the converter was also simulated with the filter inductance only on the phase leg of the converter to show how the converter responds to this type of filter arrangement. With the filter inductance only on the phase leg, the leakage voltage is a square wave and has a much higher switching ripple. The rms current is calculated for both filter configurations to show the difference between the two configurations. The results clearly show that distributing the filter inductance is ideal for this topology of converter.



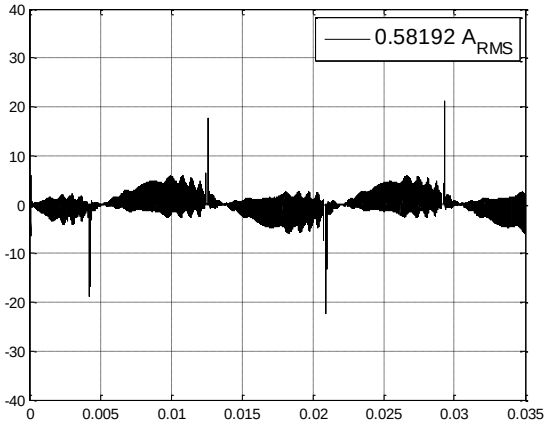
Voltage Filter Symmetrical



Current Filter Symmetrical

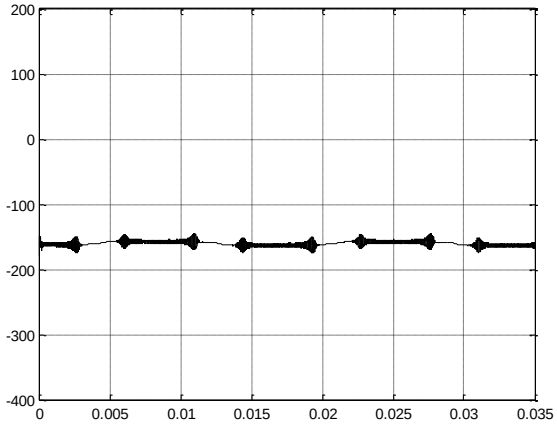


Voltage Filter Assymetrical

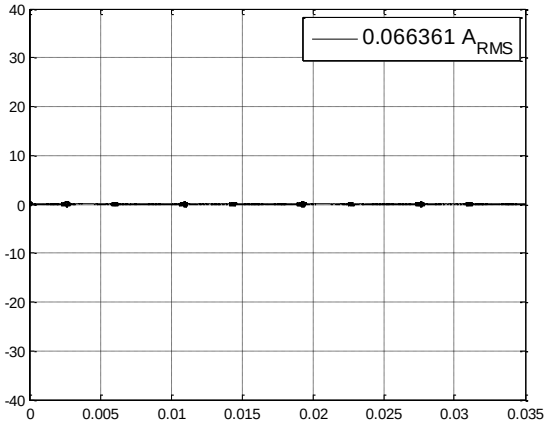


Current Filter Assymetrical

Figure 4-19: H5 leakage voltage and current filter comparison



Voltage Filter Symmetrical



Current Filter Symmetrical

Figure 4-20: Split Phase leakage voltage and current

The H5 converter shown in Figure 4-17 has one issue that is often not discussed in the literature on this topology but must be considered when designing a real converter. Unfortunately, SMA does not address this issue in their patent, but obviously has something in place to prevent this from being a problem. One of the first circuits that power electronics students learn is the buck converter. As such, students learn the importance of the diode in the circuit, and how without the diode in the circuit the switch would be damaged during turn-off since the current in an inductor cannot change instantaneously. In Figure 4-17, it is clear that the circuit is a buck type converter and that any stray inductance in series with the DC switch will cause a high voltage across the series switch when the device is opened. In order to prevent the high voltage from damaging the switch, a diode can be added as shown in Figure 4-21 or by using a large snubber circuit across the DC switch. If the stray inductance is small, the snubber circuit may be enough protection for the switch. Unfortunately, a H5 converter was not available to investigate this type of protection; although the simulation shows that without protection the voltage would reach values that would likely cause switch failure.

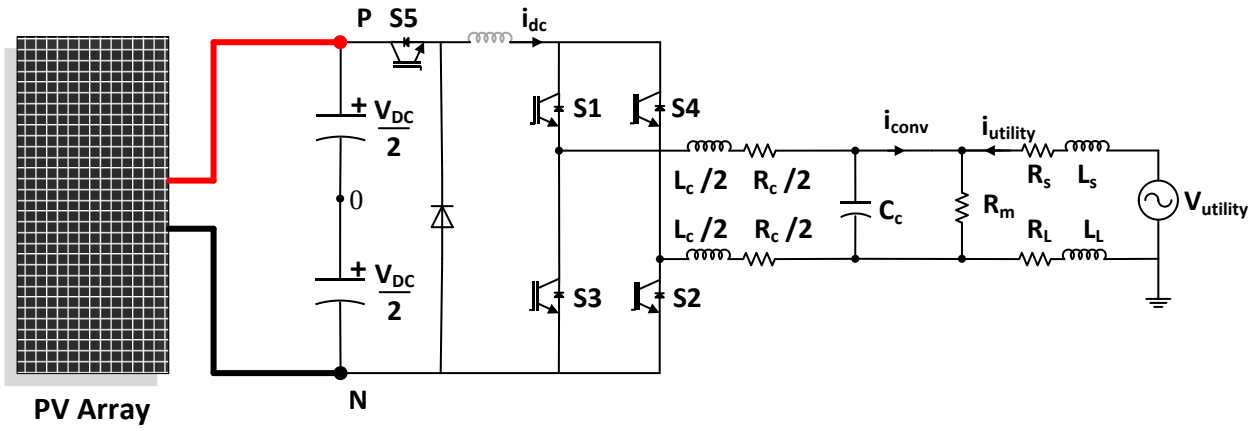


Figure 4-21: H5 DC switch protection

The H5 converter is classified as a DC bypass converter because switch S5 is on the DC bus and is used to isolate the DC bus during zero states. Another common form of isolation is the AC bypass converter, which isolates the converter on the AC side. Sunways has a patent for the high efficient and reliable converter (HERIC) converter, which uses two IGBT with anti-parallel diodes in series to form a four quadrant switch to isolate the AC side during zero states [14]. Figure 4-22 shows the HERIC converter with an LC filter connected to utility. Switching of the HERIC converter is done with unipolar PWM on the full bridge converter and at the utility frequency for the AC bypass switch. The advantages and disadvantages for the HERIC topology are listed below:

Advantages

- Ideally zero leakage current caused from the converter
- High efficiency
- Unipolar PWM scheme
- No reactive power exchange during zero transitions

Disadvantages

- More complex design
- Increased conduction losses
- Difficult to implement with analog circuitry
- Requires additional switches and diodes

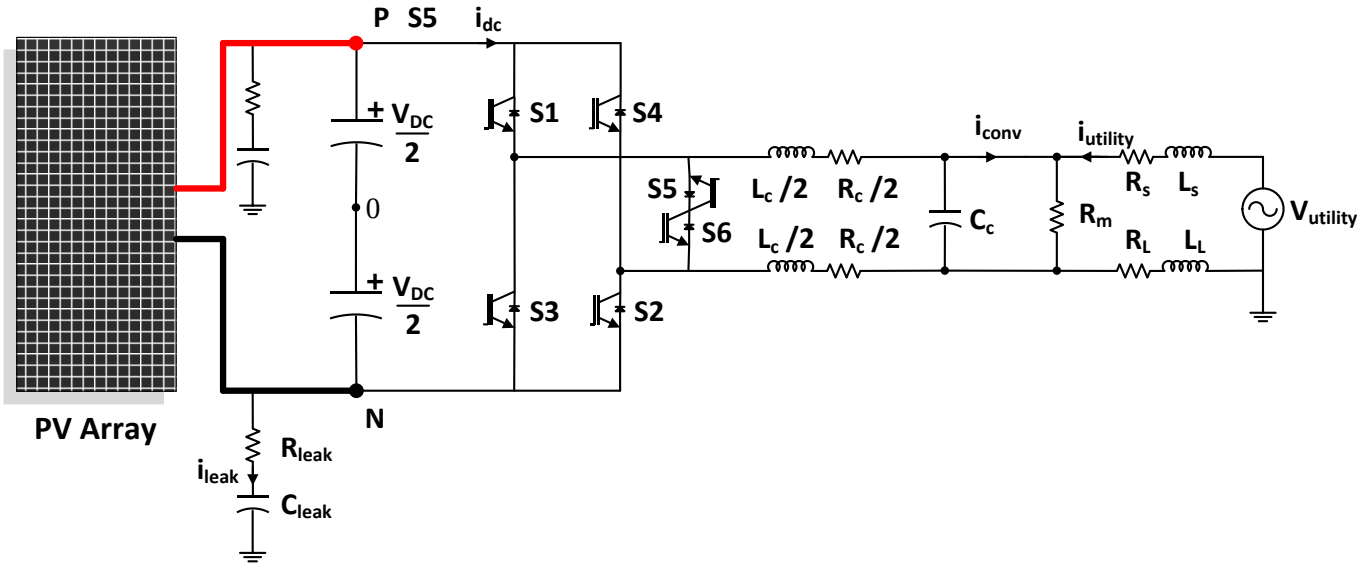


Figure 4-22: HERIC converter

4.2.2. Half Bridge

Until this point, the focus has been on the full bridge topology and variants of this topology for leakage current analysis. However, the half bridge converter in the ideal configuration does not have the same leakage current problems associated with the full bridge topology. This is because the leakage voltage is a constant because of the split dc bus configuration. In a real converter, the neutral impedance and unbalance between the split DC voltages allows for leakage current to flow in the circuit. Therefore, for this topology to work effectively, both the unbalance and neutral impedance should be minimized. Because of the influence of the neutral impedance on leakage current, the filter inductance is only placed on the phase leg of the converter in the half bridge topology.

The two most common forms of the half bridge topology are the standard two switch topology and the neutral point clamped (NPC) topology. Figure 4-23 shows the two half bridge topologies. Both topologies are used in commercial PV inverters. The advantages and disadvantages of the half bridge topology are listed below:

Advantages

- Vleak is equal to ½ Vdc in ideal case
- High efficiency
- No reactive power exchange during zero transitions

Disadvantages

- Need twice the dc link voltage
- Any neutral impedance creates high frequency leakage current
- NPC requires two extra switches and two diodes.
- NPC does not distribute losses equally among the four switches
- Large DC bus capacitors to prevent unbalance

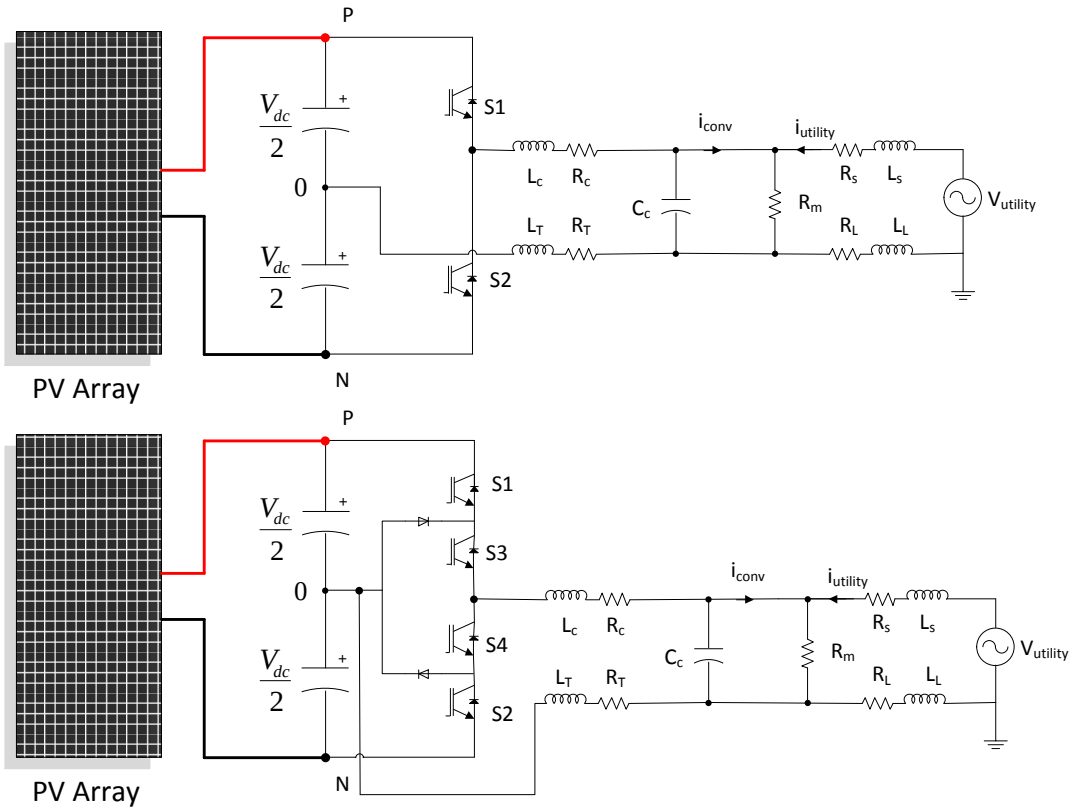


Figure 4-23: Half bridge topologies

The main limiting factor for the half bridge topology is the requirement for twice the DC link voltage. If the PV output voltage is not twice the utility voltage, then a step-up converter between the PV and inverter is needed. Unless this change is small, the DC/DC converter will likely be a step-up converter with a high frequency transformer. Therefore, using the half bridge toplogy to reduce the leakage current is redundant since the transformer already isolates the two sides. The extra DC/DC converter stage also creates additional losses and reduces the overall efficiency of the system. With today's PV market being driven by efficiency, adding extra power stages is not the optimal solution. In fact, the most efficient commercial products available today do not have an intermediate DC/DC converter stage and are transformerless topologies at all levels. Because of the voltage requirements of the DC bus, the half bridge toplogy is mostly found in low voltage applications in single phase converters.

4.2.3. H10 Converter

The ANPC full bridge hybrid converter in the previous section can be expanded upon to make a DC bypass converter similar to the H5 topology as shown in Figure 4-24. To the author's knowledge, this converter topology has not been presented in literature. Similar to the H5 topology, the converter is switched using the hybrid 2 modulation approach and using the PP zero vector for the two outer sectors. For the midpoint sectors, the modulation technique is the same as the previous NPC full bridge converter. During the zero state for all sectors, the DC bypass switches are opened to remove the DC source. Similar to the previous approach, only two of the eight main switches are switched at high frequency. The timing diagrams are shown in Figure 4-26 and Figure 4-27. During the outer sectors, switch S10 can stay on for the entire sectors only requiring switch S9 to switch at high frequency. During the midpoint sectors, switch S9 is used when the voltage is negative and switch S10 is used when the voltage is positive. The H10 has all the advantages of the NPC full bridge hybrid converter with the added benefits of a DC bypass circuitry. Of course, the major disadvantages of the converter would be the cost and added complexity because of the number of switches. In a future study, it might be possible to rearrange the switching events so that only one DC bypass switch is required. Also, if the operation does not require all four PQ quadrants, then switches S7 and S8 can be replaced by diodes. Figure 4-25 shows the leakage current in the time and frequency domain.

4.2.4. Extended Multilevel Topologies

The concepts used with the neutral point clamped converter can be expanded to include a more general class of multilevel converters that operate with one of the phase legs as a standard two level converter while the other is operated as multilevel clamped converter. Again, the major limiting factor for this design will be the cost and added complexity of the converter. Since multilevel converters are often used when the voltage requirements are too large for a single semiconductor device, the author wants to clarify that this topology will not work under these cases because of the modulation techniques and two level phase leg. In fact, it is easy to see from the two level structure and the switching diagrams, that some of the switches will have to block the full voltage potential. In future studies on this subject, the capacitive clamped arrangements for PV application might be interesting to study since the number of switches is reduced.

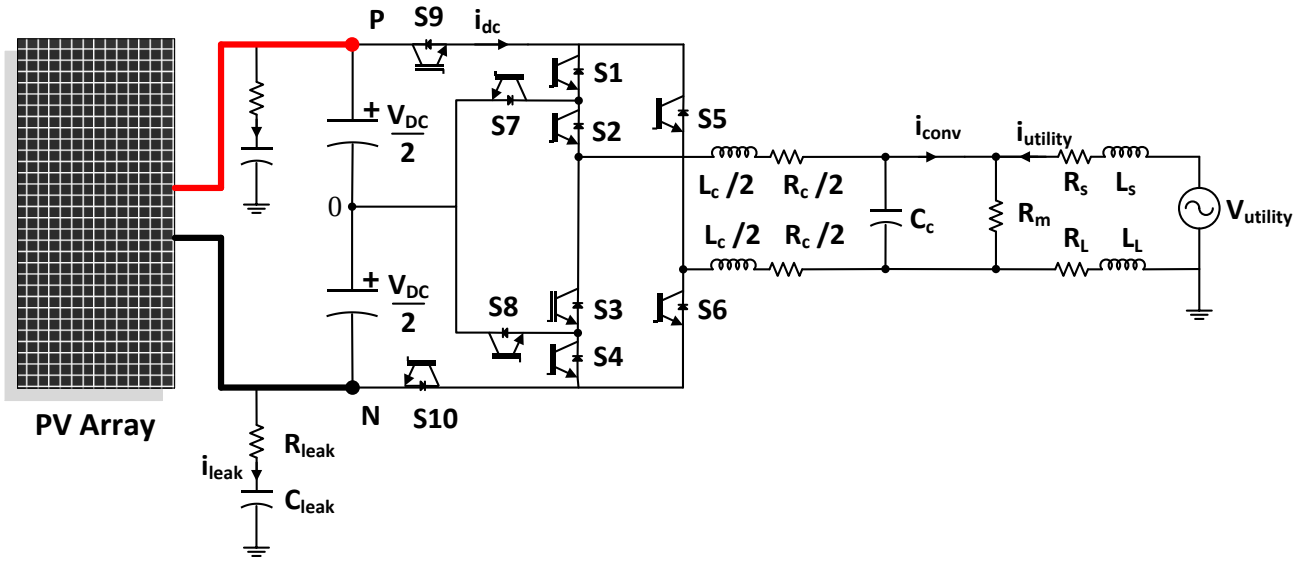


Figure 4-24: H10 converter

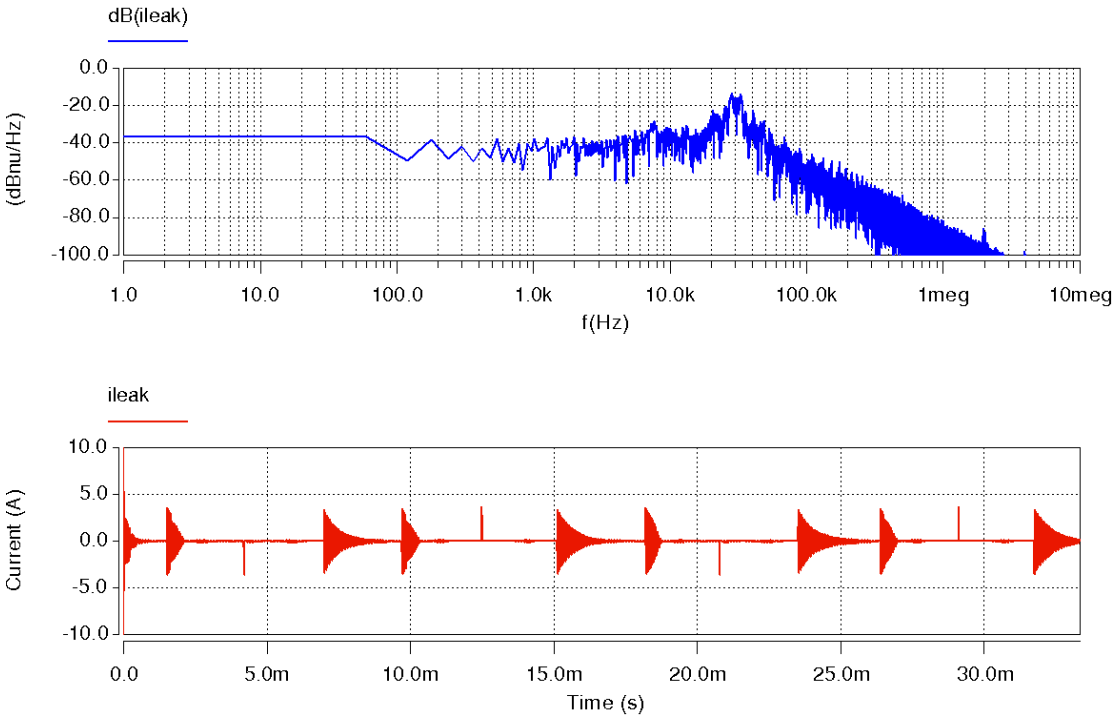


Figure 4-25: H10 Leakage current

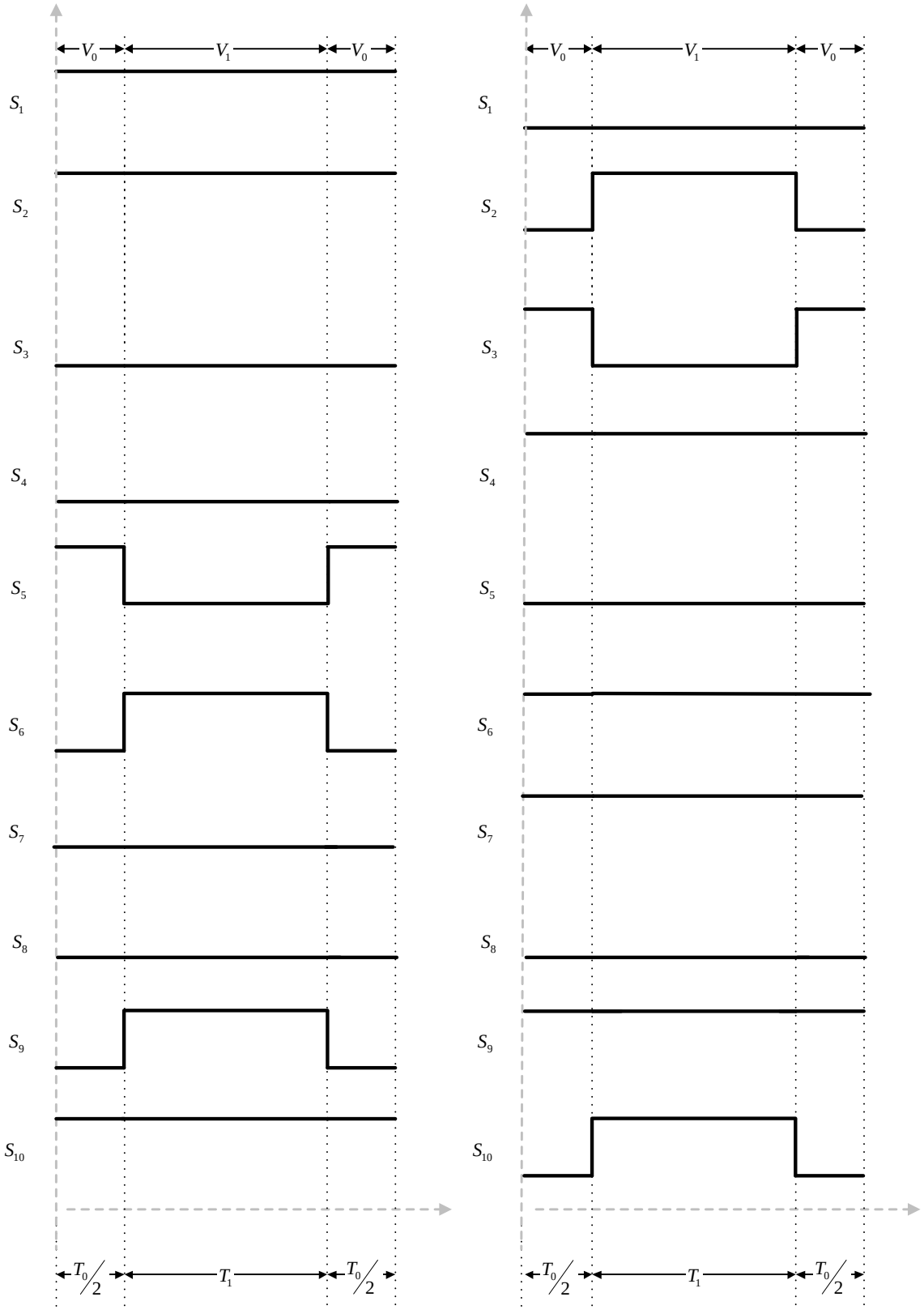


Figure 4-26: H10 sector 1 and 2 timing diagram

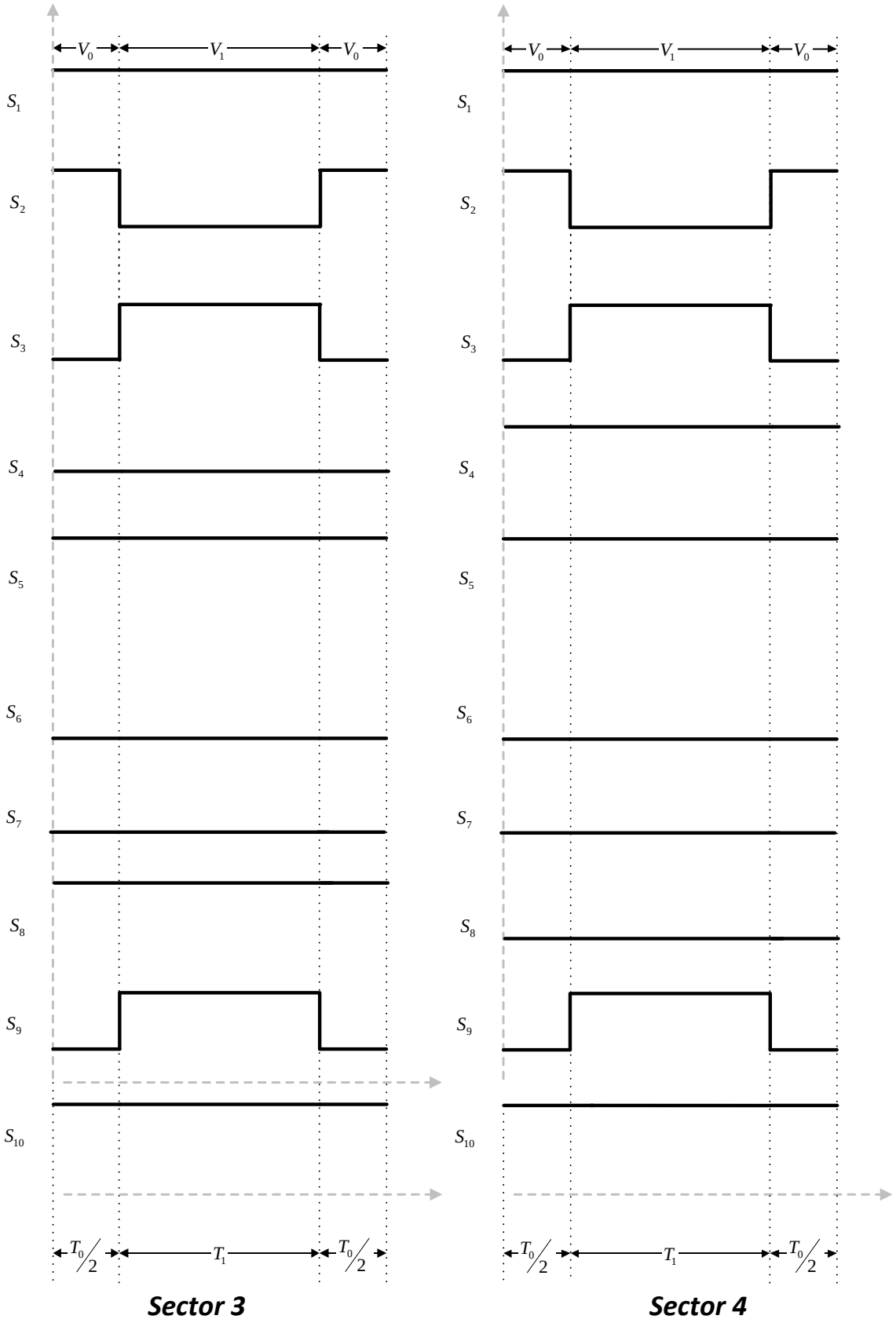


Figure 4-27: H10 sector 3 and 4 timing diagram

4.3. Conducted Emissions

Although a complete conducted emissions study is beyond the scope of this work, the leakage results warrant at least a preliminary investigation to see how the different modulation schemes compare in terms of conducted emission. To the author's knowledge, a comparison of the different modulation schemes has not been addressed in the literature for PV applications. To compare the different techniques, Saber is used with an ideal piecewise linear switch to model the transistor. The model includes the parasitic capacitances between the semiconductors and the heat sink and collector emitter capacitance. While this model is simple, the authors in [8] showed that this approach is fairly accurate below 10 MHz. In future studies, more details can be added to the models to increase the accuracy of the simulation. However, this model is more than sufficient for the comparison type analysis presented hereafter. In [8], the authors validate the model experimentally and showed very good agreement between the model and laboratory measurements. Any changes or additions in future work to improve the simulation accuracy should be validated with further experimental measurements as was done in [8].

Since the power distribution network is a large collection of devices interconnected through cabling, the emissions of one device can have an unintentional adverse effect on other equipment in the system. Because of these possible interference problems, there are regulatory standards that limit the amount of the acceptable emissions that can leave the power cable of a device. The purpose of the conducted emissions test is to measure the noise currents leaving through the power cables of the device under test (DUT) and ensure that the emissions are below the proper regulatory limitations. As one would expect, since the power distribution network varies across the world, a set of standard test procedures and test apparatuses are needed to ensure that tests are repeatable and that the test methods are consistent. One such device that helps to ensure repeatability and consistency is the line impedance stabilization network (LISN). The LISN has three main functions: (1) present constant impedance to the noise over the specified test range; (2) prevent noise on the AC power lines from contaminating the emission measurements; (3) provide a mechanism to measure the noise current with standard laboratory equipment. Figure 4-28 shows the electrical components that internally make up the LISN. The 50Ω load in the schematic represents the impedance of the spectrum analyzer used to measure conducted emissions. As the figure illustrates, the LISN is simply a filter that is designed to have a certain frequency characteristic over a defined test range. Hereafter, the electrical model of the LISN will be used to measure the conducted emissions of the converter. In this study, the military standard 461-E is used for establishing compliance limitations for conducted emissions; although the intention of the analysis is not to design a system that meets MIL 461-E, but only to use the standard as a metric to compare the modulation techniques. In the first part of the analysis, the conducted

emissions were measured using the four standard modulation techniques and only including the capacitance of the semiconductor in the model. This analysis was expanded to include the leakage capacitance of the PV panel to show the impact of the leakage capacitance on the emissions. In the final analysis, the emissions of the multilevel and two level converters were compared to show the reduction with a multilevel structure.

Figure 4-28 shows the emissions test setup with the converter and LISN connected to the utility in a standard grid-tie configuration. Table 4-3 gives the capacitance values used to model the semiconductors. It should be noted that these values are based on the authors' work in [8] for a three phase IGBT based converter, so they should not be viewed as typical or standard values for grid-tie converter applications. However, since this analysis is focused on comparing the different techniques, the most important part is the consistency of the values. These values are sufficient for a comparison type analysis. In the initial analysis, the PV leakage capacitance was not included, and the filter inductance was distributed equally among the phase and neutral conductor as shown in Figure 4-28. This was done to baseline the four PWM techniques before specifically looking at PV applications. Figure 4-29 shows the emissions results for the four PWM methods. When the filter inductance is distributed between the phase and neutral, the two hybrid methods produce similar emissions results. For unipolar modulation, the emissions at the even order switching harmonics are dominant since the odd order harmonics cancel in the differential noise. For bipolar modulation, the differential signals are twice the unipolar techniques, which would explain the increase in the switching harmonics. Comparing bipolar modulation with hybrid 1 or 2 shows a 6 dB difference at the switching frequency. This is expected since the switching ripple is twice the unipolar case and is dominated by the differential noise at these frequencies. These results also show that the common mode emissions for bipolar switching are small in comparison to unipolar switching. Since in the ideal switching case, the common mode component for bipolar modulation is zero this is expected. However, since bipolar modulation has high losses and ripple, unipolar modulation is the preferred method even when considering the high common mode emissions. It should be noted that the bipolar common mode noise is only small when the filter inductance is distributed between the phase and neutral. Addition of common mode filtering can improve the common mode performance of the unipolar methods while also keeping the efficiency high.

Table 4-3: Semiconductor Parameters

Parameter	Value
Csp	270pF
Csg	10pF
Rss	160mΩ
Cgb	32pF

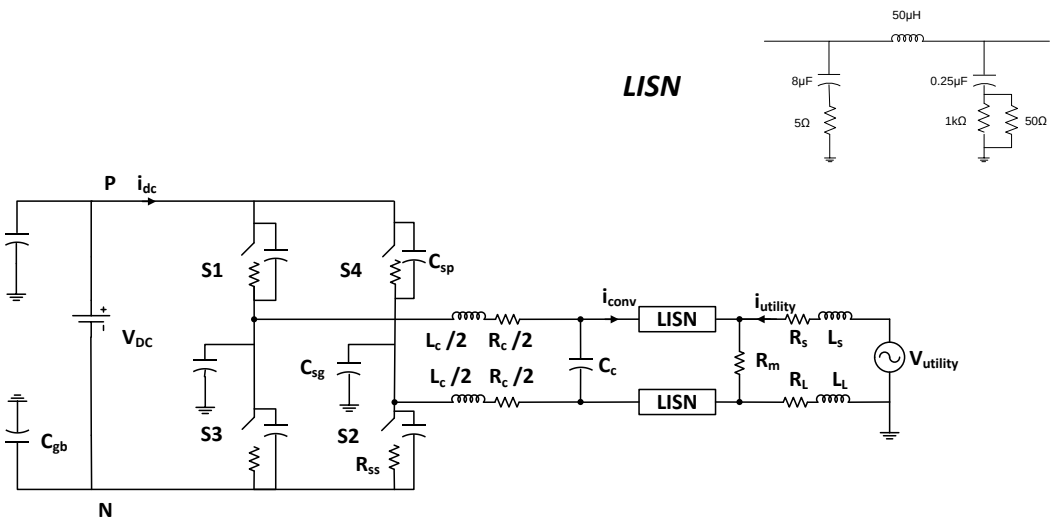
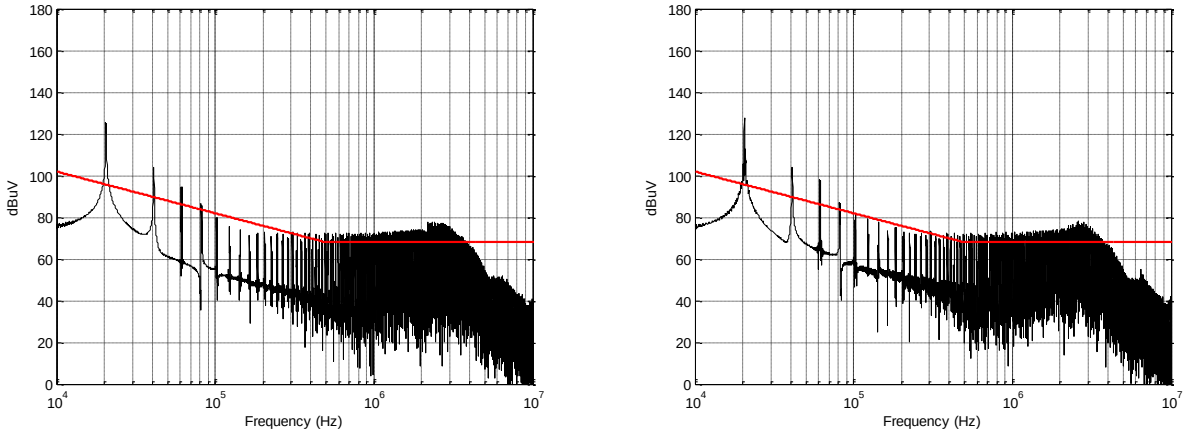
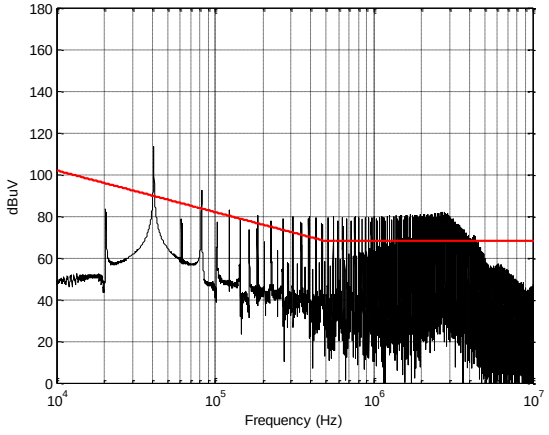


Figure 4-28: Full bridge emissions test

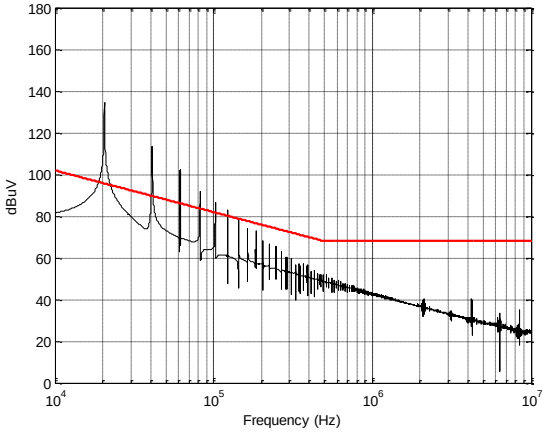


Hybrid 1

Hybrid 2



Unipolar



Bipolar

Figure 4-29: Standard full bridge comparison

In PV applications, efficiency, size, and weight are some of the main factors driving the converter market, so anything that the designer can do on the modulation side to keep the losses low while also reducing the filtering requirements is an additional benefit. In the previous discussion on leakage current for PV systems, the impact of the leakage capacitance on the ground current was discussed for several modulation schemes and converter topologies. It was concluded that the amount of capacitance and inductance in the circuit are limiting factors for some modulation and filtering schemes. Given the leakage results, it is not surprising that the leakage capacitance also has a profound effect on the conducted emissions. With the capacitance of the panel included in the model, the emissions results are much higher than the standard case. Since in the leakage analysis it was shown that distributing the filter was only beneficial to the bipolar modulation scheme with the standard full bridge inverter, the PV case was only compared with filter inductance distributed asymmetrically. Figure 4-31 shows the emissions results for the two level converters when the filter inductance is only on one phase leg of the converter, as shown in Figure 4-30. The values for the capacitances were the same as the base line case and can be found in Table 4-1.

From the results it is clear that the hybrid 1 approach only has switching noise at the switching frequency and that the noise is much lower than its unipolar counterparts. For bipolar modulation, since the filter inductance is not distributed symmetrically, the common mode noise is a large component of the total noise signal. Therefore, just as was shown in the leakage analysis, bipolar modulation also only has benefits for common mode when the filter inductance is distributed between the phase and neutral conductors.

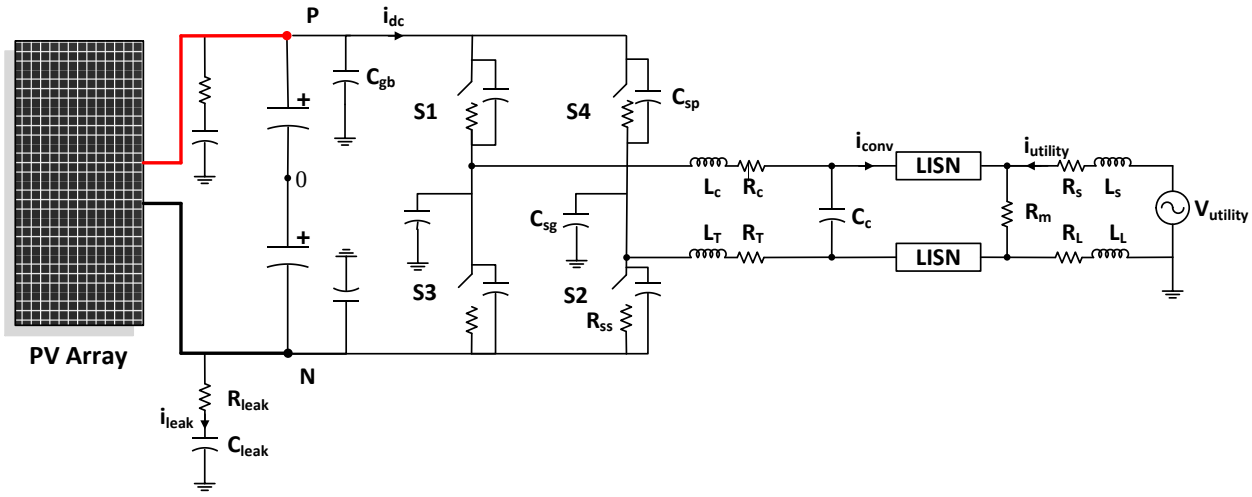


Figure 4-30: PV system emissions test

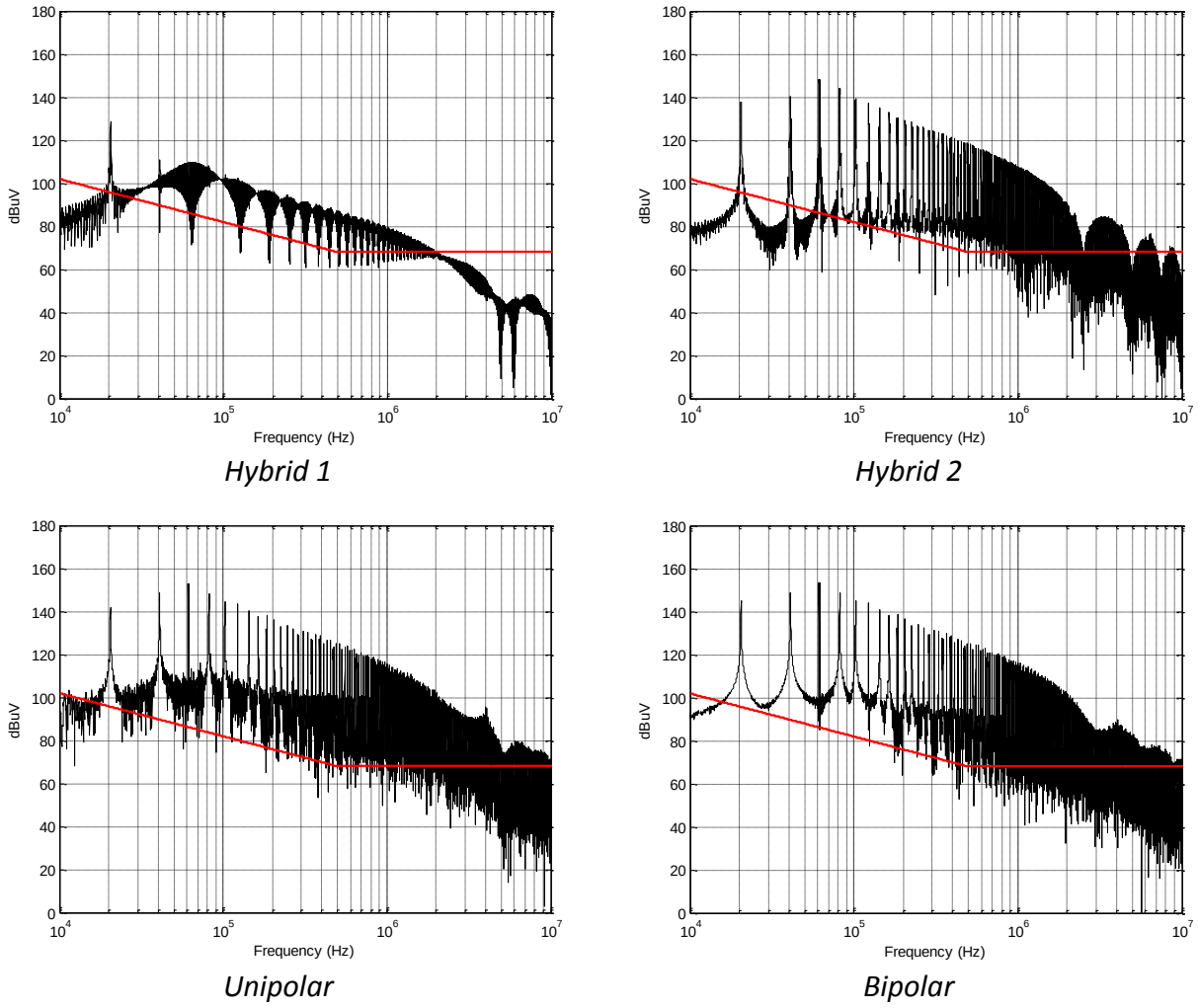
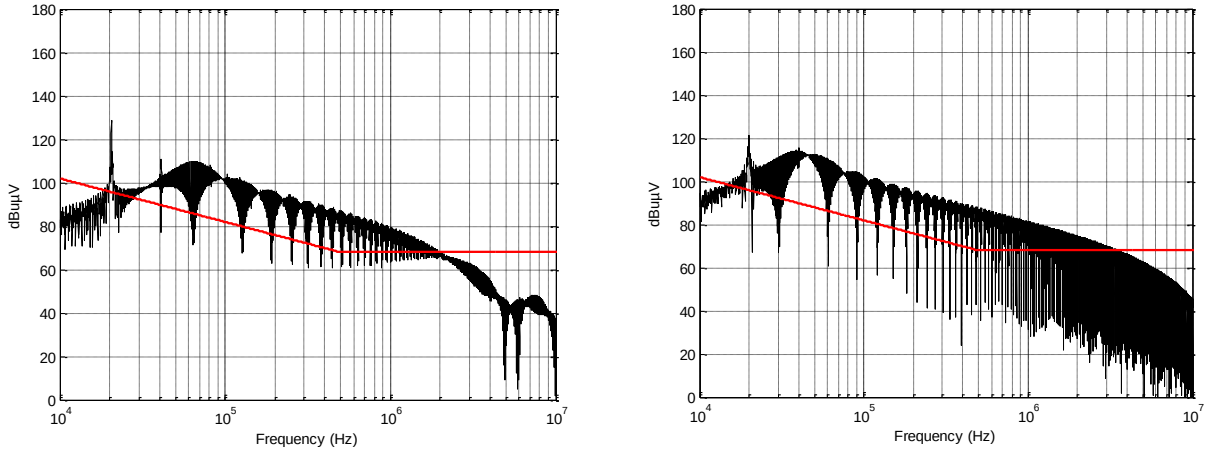


Figure 4-31: Filter undistributed including leakage capacitance

The time domain waveform for the hybrid 1 shows that the emissions current is very similar to the leakage current waveforms seen in previous analysis. In fact, the current transient that was discussed in the earlier sections is also present in the emissions waveforms. The main difference between the two cases is that the LISN filters much of the low frequency content from the waveforms. While filtering is still needed for the hybrid 1 topology, it is obvious that much less is needed than the other cases. The hybrid 1 method can also be used in the NPC full bridge hybrid converter to further reduce the emissions. Since the switching ripple is lower for the three level converter, the differential mode emissions at the switching frequency is much lower than the standard two level converter. Figure 4-32 shows a comparison of the two and three level converter conducted emissions results. The ANPC has 6 dB less of noise at the switching frequency than the two level converters. More levels can be added to the converter to reduce the noise further. However, with more levels comes the increase in complexity and cost.



Two Level *Three Level*

Figure 4-32: Two and three level comparison

4.4. Summary

In summary, the leakage current for the four modulation techniques discussed in the previous chapter were compared under symmetrical and asymmetrical filtering. For symmetrical filtering, only bipolar modulation is acceptable. For asymmetrical filtering, the hybrid 1 modulation technique produces an oscillatory transient during polarity changes. The oscillatory transient is a function of the utility cable impedance and array capacitance. The transient events were compared against existing surge standards for leakage protection devices to try to determine whether the event would cause a nuisance trip. It appears that for smaller grid-tie converters the hybrid 1 modulation is compatible with residual current devices. The author introduced a new hybrid converter consisting of one phase leg in a two level structure and the other in a three level structure. This converter has lower noise than its two level counterparts and can also be used with the hybrid 1 modulation technique. A few of the commercially available transformerless converters were discussed to show how these products deal with leakage current. The author introduced DC bypass converter based on the ANPC full bridge hybrid structure introduce earlier. This has the advantages of the DC bypass circuitry but has the lower switching ripple associated with a three level structure.

In addition to the leakage current, the conducted emissions of the different modulation and converter structures were compared. For PV applications, the hybrid 1 approach produces very low differential noise because of the modulation scheme. The NPC full bridge hybrid topology produces ½ the differential noise under the same modulation sequencing because of the three level structure. The emissions results need further investigation with hardware verification.

Chapter 5.Single Phase Grid-Tie Average and DQ Models

In the previous chapter, the focus was on the converter characteristics as a function of the modulation scheme, switching characteristics, and the arrangement of the passive components. While these are very important aspects of the overall converter design and something that must be considered when designing converters for grid–tie applications, these issues are often not important for developing the average models and designing the closed loop control. Therefore as we move forward, all of the issues associated with the switching characteristics and the passive placement in the previous chapters will only be discussed when relevant for the average and closed loop designs.

The focus of this chapter is on developing the average and dq models for the single phase converter in order to design the closed loop control for the converter. In order to develop the average model, the first step is averaging over the switching frequency in order to make the system continuous. Once the system is continuous, a fictitious dq transformation for single phase systems will be used so that the system can be switched to a dc equivalent circuit. With the system in a dc form, linearizing the system around an operating point allows the control system to be designed using classic linear time-invariant control techniques. Figure 5-1 shows a single phase grid-tie converter with an LC output filter and an equivalent load between the converter and utility. This will be the starting point of the discussion. From this simple LC case, the model complexity will be increased to more sophisticated filter topologies and load arrangements. As will be shown later in the chapter, the filtering, load level, and load type influence the closed loop design of the converter. Since the load and source impedances are unknown, the converter must be able to operate over a wide range of conditions while remaining stable and tracking a reference.

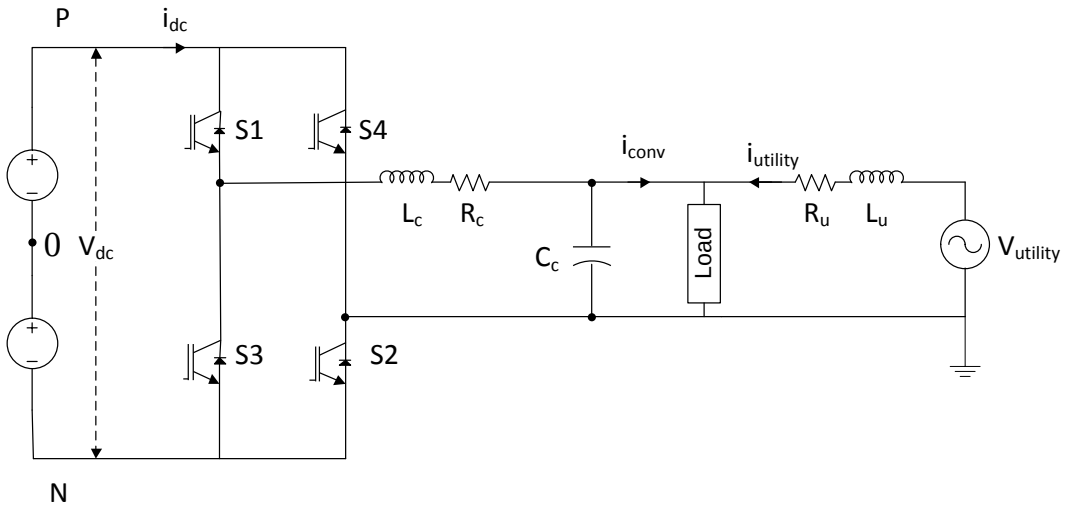


Figure 5-1: Single phase VSI

5.1. Average Model

Assuming ideal switching behavior for the voltage source converter, allows the switches in Figure 5-1 to be replaced by two single pole double throw switches (SPDT) resulting in Figure 5-2. In this new circuit model it is clear that each switch can be in one of two possible states. Next, it is possible to write out the switching states for the two phases in terms of each of the switch positions, which are given in Table 5-1. For the single phase voltage source converter, there are four possible switching positions, two active positions and two zero states. From the line to line switching function, the voltage relationship can be developed based on the switching positions. When the switches are in the active states, the voltage is equal to the DC link voltage. When the switches are in the zero states, the voltage is equal to zero.

While the switching technique will not be considered in the average model, it should be noted that these results are consistent with the analysis in chapter 3. In that analysis, it was shown that for unipolar modulation the only difference between the modulation techniques is how the active and zero vector are distributed within the switching cycle. From this table it is easy to see how the zero and active vectors are used to for a particular modulation scheme. Remember from the previous chapter that for bipolar modulation the zero time is divided equally between the two active states since the zero states are not used.

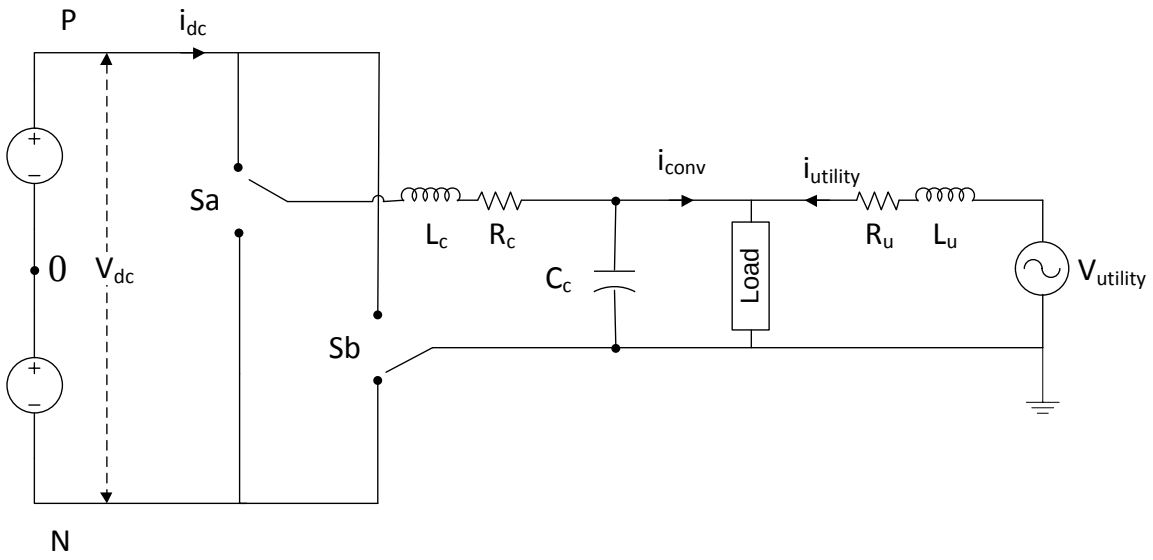


Figure 5-2: SPDT equivalent circuit

Table 5-1: Switching states

Sa	Sb	Sab	Voltage
0	0	0	0
0	1	-1	-Vdc
1	0	1	Vdc
1	1	0	0

With the switching functions established, it is possible to write the system equations in terms of the state variable. As a first case, to show how to formulate the expressions, let's assume that the load is a simple resistor shared between the converter and the utility. For the resistive load case, (5-1)-(5-4) can be used to describe the circuit.

$$\frac{di_c}{dt} = \frac{1}{L_c} \cdot \left[s_{ab} V_{DC} - R_c \cdot i_c - V_{pcc} \right] \tag{5-1}$$

$$\frac{di_u}{dt} = \frac{1}{L_u} \cdot \left[V_u - R_u \cdot i_u - V_{pcc} \right] \tag{5-2}$$

$$\frac{dV_{pcc}}{dt} = \frac{1}{C_c} \cdot \left[i_c - \frac{V_{pcc}}{R_L} + i_u \right] \tag{5-3}$$

$$i_{dc} = s_{ab} \cdot i_c \tag{5-4}$$

The next step is to average over the switching frequency to make the system continuous. We will assume that the switching frequency is much larger than the fundamental and any perturbation in the system so that the switching functions in (5-1)-(5-4) can be replaced by their equivalent duty cycles. After applying the averaging operator, (5-5)-(5-8) result.

$$\frac{di_c}{dt} = \frac{1}{L_c} \cdot \left[d_{ab} V_{DC} - R_c \cdot i_c - V_{pcc} \right] \tag{5-5}$$

$$\frac{di_u}{dt} = \frac{1}{L_u} \cdot \left[V_u - R_u \cdot i_u - V_{pcc} \right] \tag{5-6}$$

$$\frac{dV_{pcc}}{dt} = \frac{1}{C_c} \cdot \left[i_c - \frac{V_{pcc}}{R_L} + i_u \right] \tag{5-7}$$

$$i_{dc} = d_{ab} \cdot i_c \tag{5-8}$$

When the circuit is redrawn using the duty cycle and DC bus voltage, Figure 5-3, it is easy to see that the circuit is equivalent to a two bus system. From basic power transfer theory, if the impedance of the grid and converter are mainly inductive, then the reactive power will mostly be a function of voltage magnitudes and the real power will mostly be a function of the phase angle difference between the two sources. The voltage angle and magnitude of the inverter can be calculated using standard power flow techniques assuming the utility voltage reference is known. Of course, in a closed loop system the phase angle and voltage magnitude are a product of the control system.

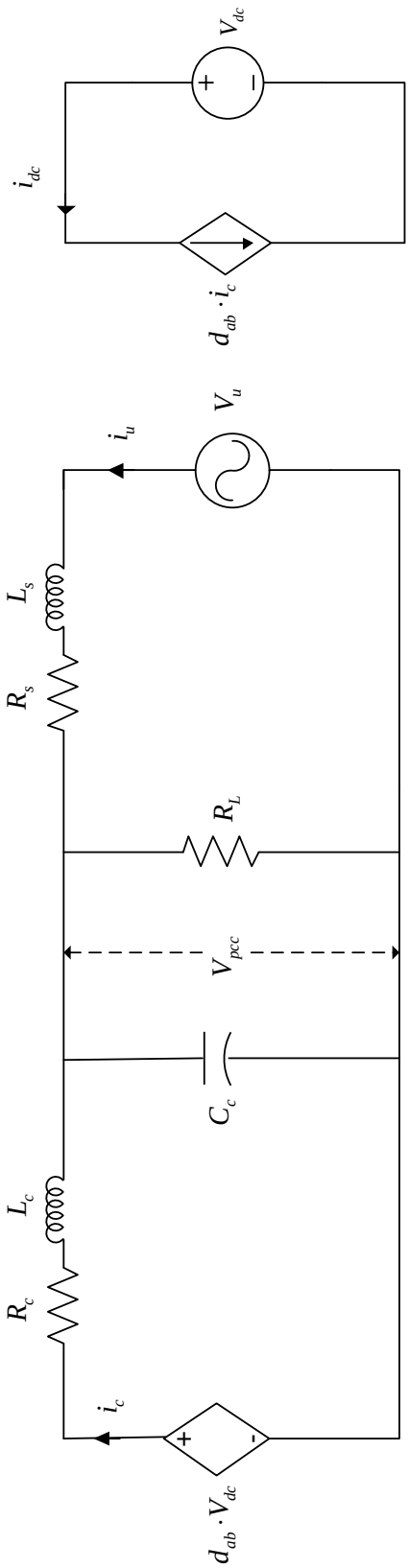


Figure 5-3: Average model resistive load

5.2. DQ Model

Since the system is AC, defining an operating point to linearize around in this configuration is not straightforward. Also, once the control system is in place, steady state error is higher when controlling AC variables using standard control schemes such as PI and PID since the gain at the fundamental frequency is finite. Therefore, transforming the variables to DC quantities is common practice in power electronics. The question is then how to transform the circuit into DC quantities? Unfortunately, this is not simple for single phase systems since the variables are single phase quantities. While there have been several proposed techniques in the literature on this subject, there is still ongoing research in this area. As a starting point, the present methods will be described, focusing on their implementation, advantages, and disadvantages.

In three phase systems, as long as the system is balanced and free of harmonics, the three phase variables can be transformed into DC quantities by using Park's transformation. For single phase systems, it is not possible to transform the quantities with a single variable and transformation matrix, so a component that is normal to the signal is introduced. With the addition of the normal component, equations (5-9)-(5-12) can be used to transform the signal between AC and DC quantities. Note that the single phase transformation is an orthogonal matrix.

$$T = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \tag{5-9}$$

$$T^{-1} = T^{T} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \tag{5-10}$$

$$X_{dq} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \cdot \begin{bmatrix} X \\ X_N \end{bmatrix} \tag{5-11}$$

$$where\ X_N\ is\ normal\ to\ X$$

$$X_{\alpha\beta} = T^{-1} \cdot X_{dq} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \cdot \begin{bmatrix} X_d \\ X_q \end{bmatrix} \tag{5-12}$$

5.2.1. Normal Component

The two most common ways of obtaining the normal component are differentiation and phase delay. Each method is briefly discussed below with a focus on their implementation, advantages, and disadvantages. During the small signal analysis and controller design, the

delay approach will be analyzed in a closed loop system. In addition to using these methods for closed loop control, they are also commonly used in phase-locked loop circuitry used to synchronize with the utility.

5.2.1.1 Derivative Approach

In the derivative approach, the signal is differentiated and then scaled by the fundamental frequency. Scaling ensures that the fundamental components are equal in magnitude while also normal to one another.

Advantages

- Simple implementation in analog circuitry
- Simple implementation in digital circuitry
- Better dynamic performance than phase delay

Disadvantages

- Susceptible to noise
- Does not work well with harmonics
- Difficult in closed form control

5.2.1.2 Phase Delay

In the phase delay approach, the control signal is delayed by 90°. The objective is to shift the fundamental frequency signal by 90° while leaving harmonics in the signal unchanged.

Advantages

- Simple implementation in digital circuitry
- Works better than derivative approach when harmonics are present
- Noise is not amplified

Disadvantages

- Delay results in low bandwidth
- Slow closed loop performance because of bandwidth
- Phase margin limits stability

5.2.2. Zero q-axis

Another method is to use zero for the normal component. In (5-11), if Xn is chosen to be zero then it is clear that when the signal X is a sinusoidal waveform that the transformation contains a dc component as well as a double frequency term. This double frequency term

behaves like a perturbation on the steady state DC terms. The advantages and disadvantages of the method are listed below.

Advantages

- Simple implementation in analog or digital circuitry
- Higher bandwidth in closed loop control than with phase delay or derivative
- Low steady state error compared to pure ac approach
- Easy to design control

Disadvantages

- Not a true dq representation
- Double frequency term for sinusoidal case

5.2.3. Single Phase DQ Transformation

Using the dq transformation matrix, it is possible to transform the AC system to a DC system. The equations for carrying out this transformation for the resistive load case are shown in (5-13)-(5-15). Multiplying (5-13)-(5-15) by the transformation matrix and carrying out the derivative results in (5-18)-(5-21). It is clear from (5-17) that the derivative causes cross coupling between the d and q axis. Since the cross coupling increases the overall complexity of the design, there are methods available to decouple the two axes to simplify the analysis.

$$\frac{d\left(T^{-1}\cdot i_{c\_dq}\right)}{dt}=\frac{1}{L_c}\cdot\left[T^{-1}\cdot d_{ab\_dq}\cdot V_{DC}-R_c\cdot T^{-1}\cdot i_{c\_dq}-T^{-1}\cdot V_{pcc\_dq}\right] \tag{5-13}$$

$$\frac{d\left(T^{-1}\cdot i_{u\_dq}\right)}{dt}=\frac{1}{L_u}\cdot\left[T^{-1}\cdot d_{ab\_dq}\cdot V_{DC}-R_u\cdot T^{-1}\cdot i_{u\_dq}-T^{-1}\cdot V_{pcc\_dq}\right] \tag{5-14}$$

$$\frac{d\left(T^{-1}\cdot V_{pcc\_dq}\right)}{dt}=\frac{1}{C_c}\cdot\left[T^{-1}\cdot i_{c\_dq}-\frac{T^{-1}\cdot V_{pcc\_dq}}{R_L}+T^{-1}\cdot i_{u\_dq}\right] \tag{5-15}$$

$$\frac{d\left(T^{-1}\cdot X_{dq}\right)}{dt}=\frac{dT^{-1}}{dt}\cdot X_{dq}+T^{-1}\cdot\frac{dX_{dq}}{dt} \tag{5-16}$$

$$T\cdot\frac{dT^{-1}}{dt}=\begin{bmatrix}0 & -\omega\\ \omega & 0\end{bmatrix}\cdot\begin{bmatrix}X_d\\ X_q\end{bmatrix} \tag{5-17}$$

$$\frac{di_{c\_dq}}{dt}=\frac{1}{L_c}\cdot\left[d_{ab\_dq}\cdot V_{DC}-R_c\cdot i_{c\_dq}-V_{pcc\_dq}\right]-\begin{bmatrix}0 & -\omega\\ \omega & 0\end{bmatrix}\cdot i_{c\_dq} \tag{5-18}$$

$$\frac{di_{u\_dq}}{dt} = \frac{1}{L_u} \cdot \left[V_{u\_dq} - R_u \cdot i_{c\_dq} - V_{pcc\_dq} \right] - \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \cdot i_{u\_dq} \tag{5-19}$$

$$\frac{dV_{pcc\_dq}}{dt} = \frac{1}{C_c} \cdot \left[i_{c\_dq} - \frac{V_{pcc\_dq}}{R_L} + i_{u\_dq} \right] - \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \cdot V_{pcc\_dq} \tag{5-20}$$

$$i_{dc} = d_{dq} \cdot i_{c\_dq} \tag{5-21}$$

The dq circuit for the resistive load case is shown in Figure 5-4. From the figure it is clear that there is cross coupling between the dq axis because of the derivative terms in the equations. Before designing the closed loop control, the dq model needs to be validated against the switching model to verify that the two models are in agreement. Figure 5-5 shows a comparison of the switching model and dq model under a step load condition. During the step load change at 250 ms, the voltage at the point of common coupling has a transient before settling to its new value. It is clear from the figure that the two models are in agreement during steady state and during transient conditions. The only difference between the two models is the switching ripple caused by the switching. In fact, if the average operator is applied to the switching waveform the two results are almost identical. The switching ripple will vary based on the modulation scheme. In Figure 5-5, the modulation scheme was chosen to be bipolar modulation in order the make the switching waveform and dq waveforms more distinguishable. With unipolar modulation techniques discussed in the earlier chapters, the switching ripple is much less than what is presented in Figure 5-5.

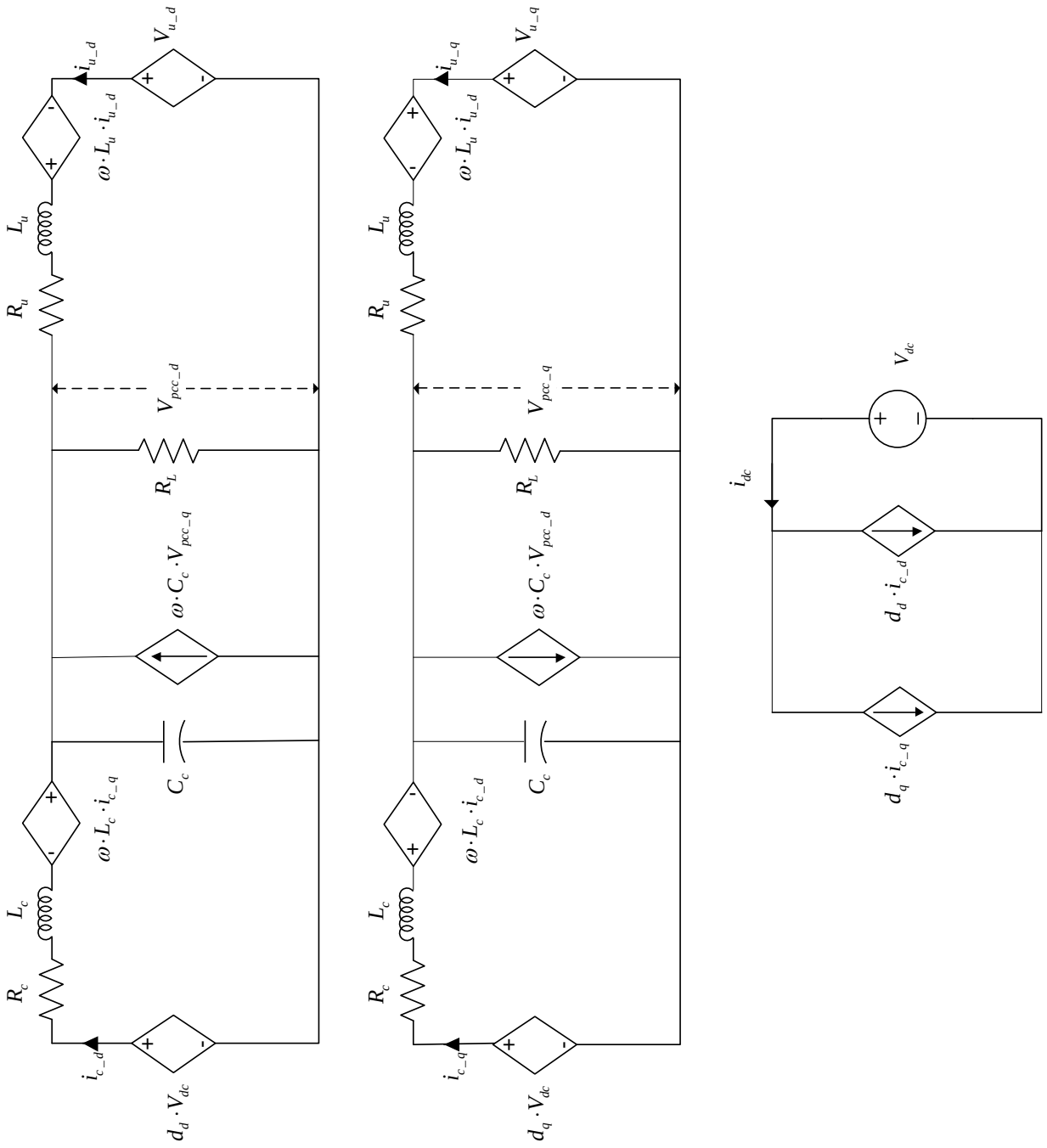


Figure 5-4: DQ resistive load

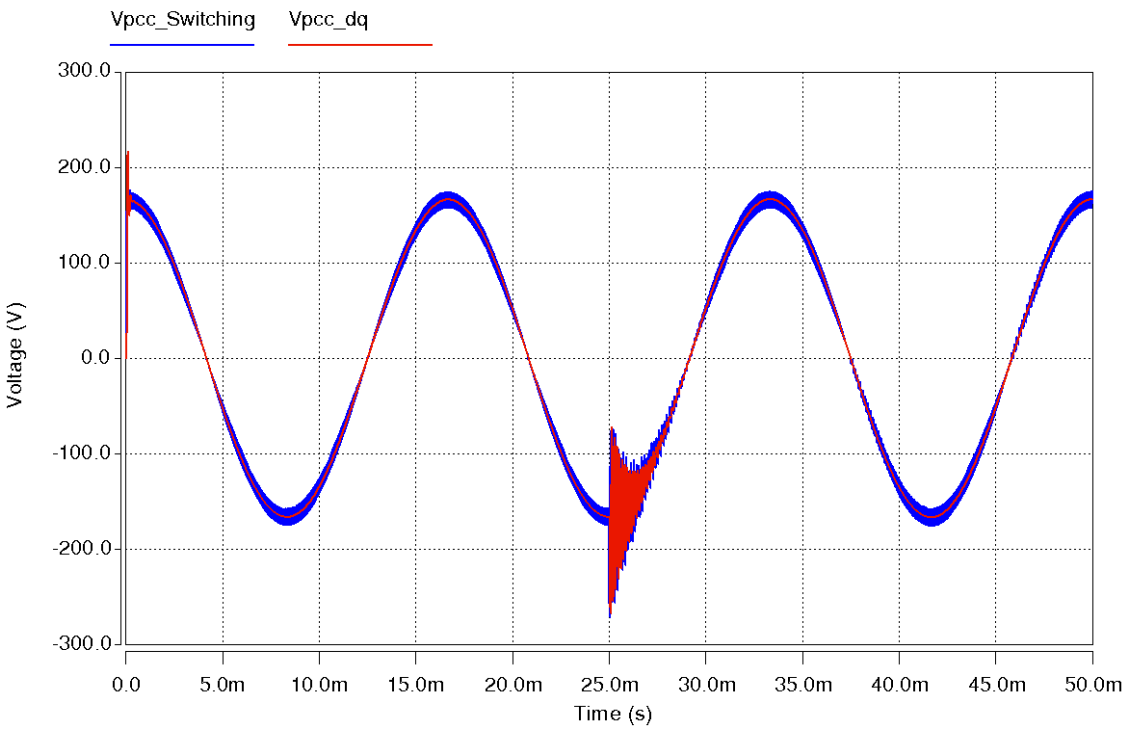


Figure 5-5: Switching and DQ model comparison

5.3. Small Signal Model & Control

From the dq model, the small signal model can be obtained by linearizing around a steady state operating point. In order to linearize the system, a perturbation is applied to the system, resulting in the system variables being equal to their steady state value plus a perturbation. Since the voltage output of the inverter is equal to the duty cycle multiplied by the DC voltage, after perturbing, the duty cycle multiplied by the DC voltage results in non-linear terms. In order to have a linear system, these 2^{nd} order terms have to be neglected. The 2^{nd} order terms are typically small in comparison to the first order terms under small perturbations and can be neglected, which is the assumption for small signal analysis.

Figure 5-6 shows the small signal equivalent circuit after linearizing the system. Notice that the inverter output has a duty cycle perturbation as well as a DC link perturbation. The closed loop control should have very high rejection to DC perturbations at the low frequency to ensure that variations in DC voltage are not significant on the inverter output. For PV applications with the panels directly connected to the inverter this is important since the PV voltage will vary based on weather conditions. The duty cycle perturbation is also important when looking at dead time, dropped pulses, and switching inconsistencies. If the gain is too low, these can create low end harmonics in the output voltage and may even lead to instability. More will be discussed on these topics later in the chapter. Other than duty cycle and DC link variations, the utility variations are also important since they can create unwanted harmonics in the control and output variables.

5.3.1. Passive Selection

Selecting the right passive components is important for both steady state and closed loop control of the converter. From an attenuation standpoint, the cut-off frequency of the filter needs to be low enough that the switching harmonics from the inverter are attenuated and distortion levels are in compliance, but high enough that the filter is not sinking any of the power line harmonics. On the control side, the filter inductance needs to be large enough that the utility inductance does not impact the closed loop performance, but low enough that the system response is not sluggish. Since the impedance of the utility is unknown to the designer, this is one of the more challenging issues to work around. Often leading the designer to determine a worst case scenario and design based around this condition.

Even if the converter does not need a transformer to interconnect, such as the ones discussed in the previous chapter, there will always be end users that will put a transformer between the inverter output and utility. In these cases, it is very likely that this transformer will be the same size or only slightly larger than converter. Therefore, the converter must be able to work when the utility impedance has a base value near or at the converter size. On the other extreme, it is possible that the utility size could be much larger than the converter. In

fact, for smaller converters connecting directly to the distribution system this is likely the case. In most literature on this subject, the utility is typically assumed to be much larger than the converter to simplify the analysis. However, in order to have a thorough analysis, a range of utility impedances needs to be considered as the smaller utility feed is often the worst case. Table 5-2 gives the values of the passive components used in the small signal analysis. The filter for the converter was designed to have a cut-off frequency of approximately 3 kHz with 40 dB/decade of attenuation. The utility impedance was assumed to have an X/R ratio of 3.5 with 5% impedance over a 7.2 -72 kVA base at 120 Vrms. Since the converter in the analysis was 7.2 kVA, it works out that the utility is less than ten times the size of the converter.

The passive selections also need to be able to work over a large range of load conditions. As will be shown later, the load level and type heavily influence the stability of the converter. In fact, the local load problem is one of the more challenging problems to deal with when designing the closed loop control for grid-tied converters. Often the best that the designer can do is to try to formulate a worst case scenario and then try to design around this condition. Unfortunately, this method can lead to suboptimal control for many of the loading conditions. In most literature on the subject, the local load case is not addressed, but in the real system this is always a limiting factor. Since there are many commercially available grid-tie converters, it is obvious that the control can be designed to work over a large range of loads. However, the question is whether the control has a desirable response time and can meet other control objectives with minimal changes to other design parameter. For instance, if the control bandwidth is decreased to work with a capacitive load, then the ability of the control system to attenuate harmonics from the utility and from the switching will be reduced as a consequence. This may result in the designer having to use multiple synchronous reference frames or PR control with harmonics to deal with utility harmonic, which may have not been required if the bandwidth and attenuation were high.

Table 5-2 : Passive component values

Parameter	Value
L_c	200 µH
C_c	15 µH
R_c	15 mΩ
L_u	26 - 260 µH
R_u	3-30 mΩ

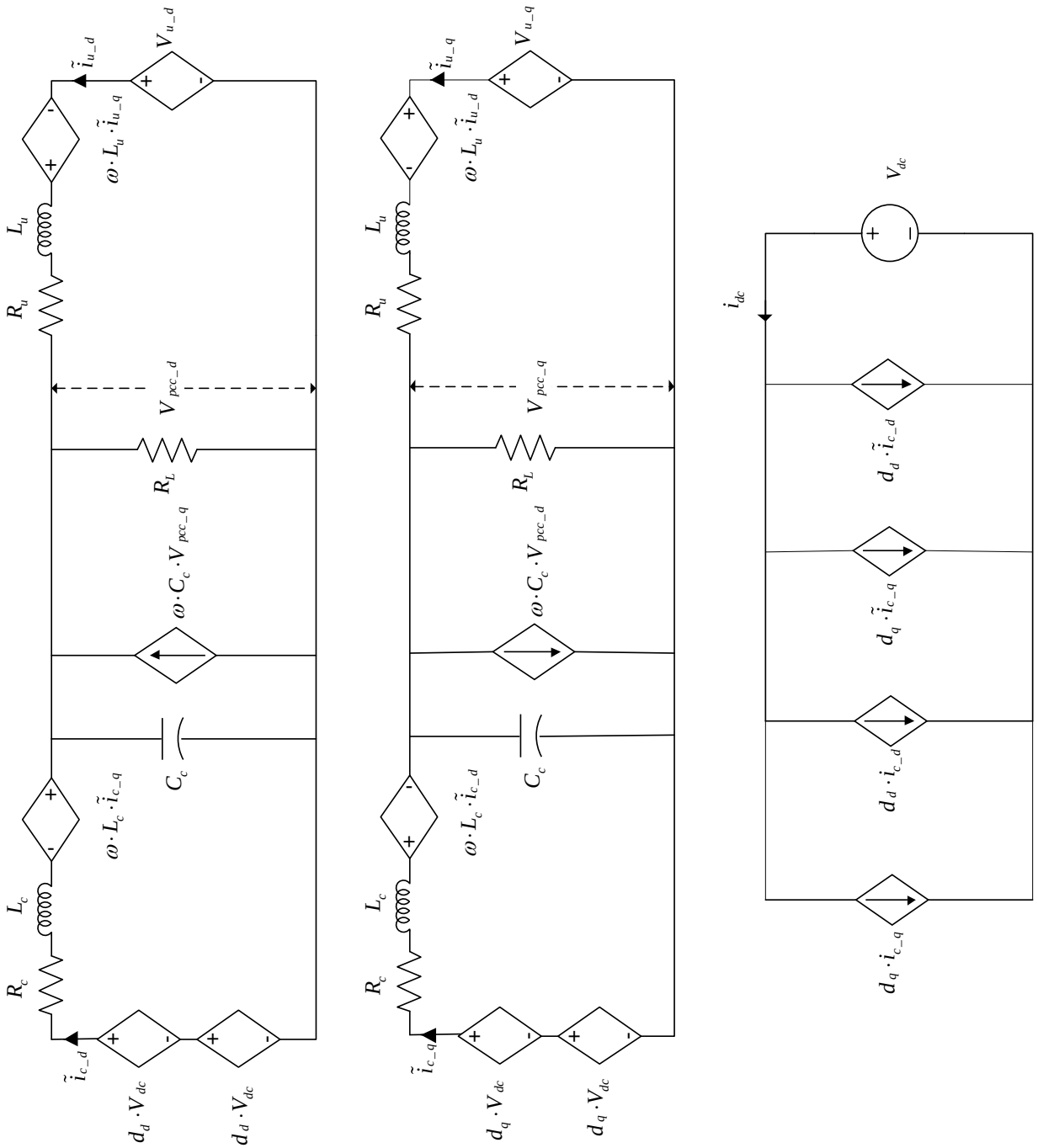


Figure 5-6: Small signal model resistive load

Given the small signal model for the converter with resistive load, the first order of action is to determine the influence of the resistance on the closed loop control. Since the resistance influences the damping at the resonant conditions and has very little influence elsewhere, the worst case scenario is when the resistance is not present. Therefore, when designing the closed loop control for the resistive load case, the no-load case should be the basis for the design. It should be noted that the resonances at the no-load case are damped by the ESR of the filter capacitor, so this should be included in the model for accurate damping. Excluding the ESR results in an over conservative design.

The transfer function of direct current vs. the direct duty cycle is shown in Figure 5-7. From the transfer function, it is clear that the controller will need to increase the roll-off rate in order to get a cut-off frequency below the switching frequency, which we will assume to be in the 10s of kHz for this example. Assuming that the switching frequency is in the 10s of kHz, the target crossover should be about 1 kHz (1/10th of the switching frequency). It is also clear from the figure that the phase is -90° for most of the high frequency range, excluding the resonance. Addition of a proportional integral control will increase the roll off rate at the expense of decreasing the phase. Addition of the PI compensator in the design results in a 900 Hz crossover frequency and a phase margin of 40°. Figure 5-8 shows the loop gain after applying the compensator. The constants for the compensator are given in the caption below the figure. Although the compensator could be pushed slightly higher to increase the bandwidth, the limiting factor is the digital delay which will be discussed in the next section. From the loop gain, the closed loop response is given in Figure 5-9.

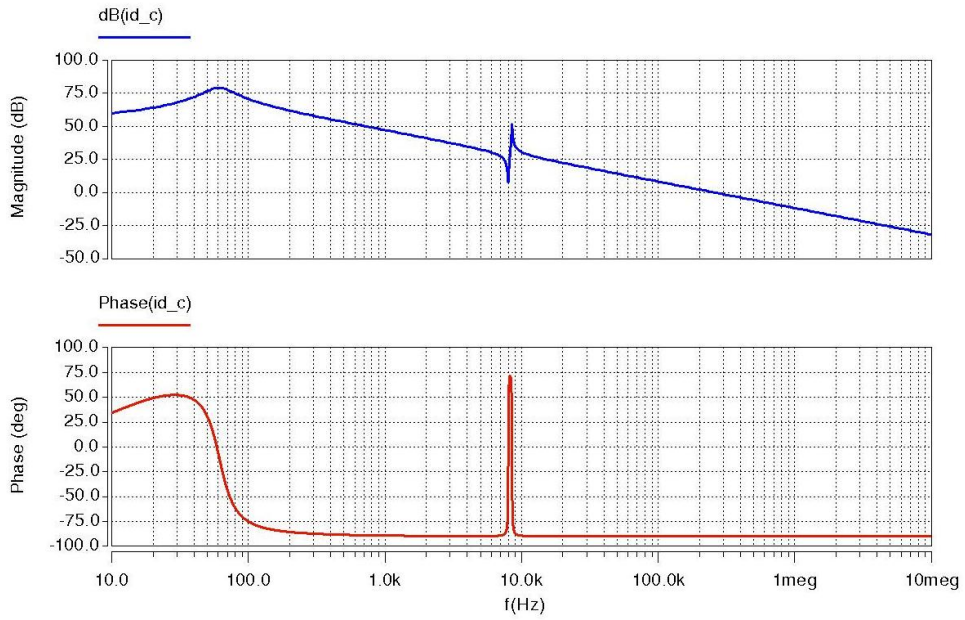


Figure 5-7: i_d/d_d transfer function

$$k_p + \frac{k_i}{s} \tag{5-22}$$

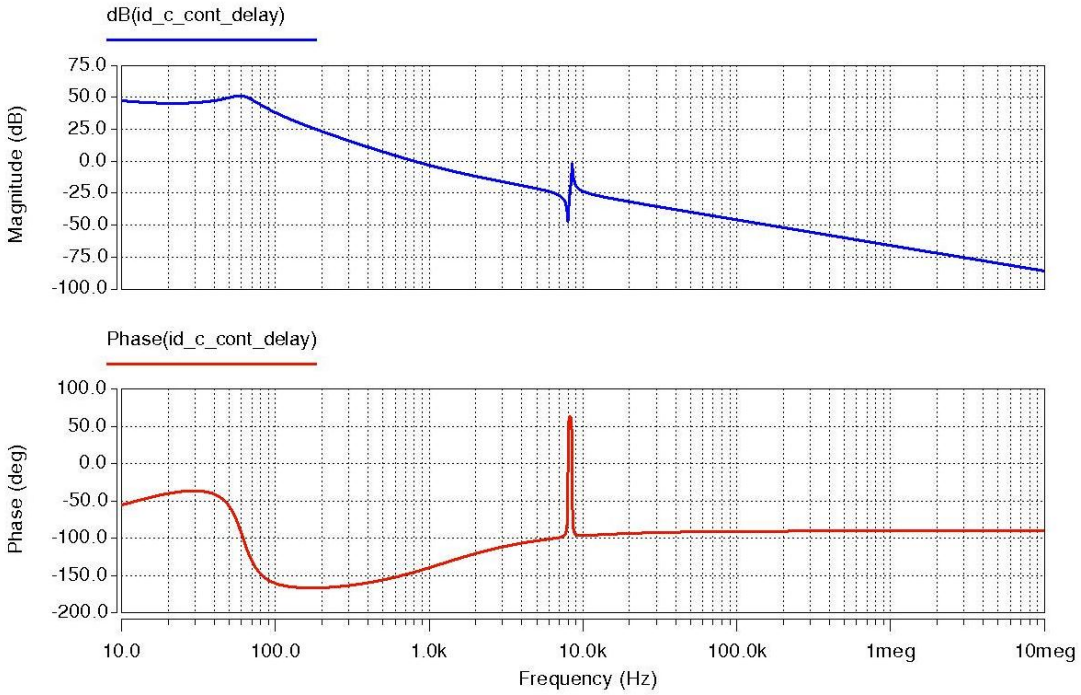


Figure 5-8: Loop gain i_d/d_d PI control $K_p = 0.002$ $K_i = 15$

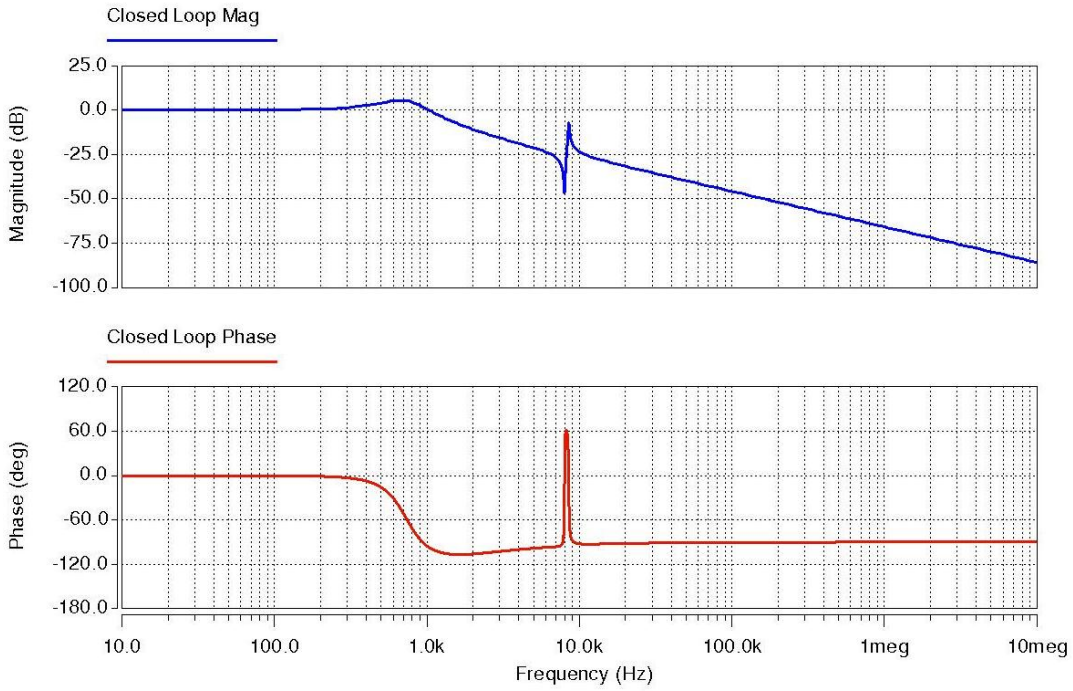


Figure 5-9: Closed loop i_d/d_d PI control $K_p = 0.002$ $K_i = 15$

5.3.2. Digital Delay

In a system using digital control, a time delay is inherent in the system because of the sampling and the time required for the signal processing. Depending on the sampling and processing time, this delay can be as much as two switching cycles. Of course, the time delay will have a huge impact on the phase margin, requiring the crossover frequency to be adjusted accordingly. In terms of control response, this typically means that the bandwidth has to be lowered to ensure adequate phase margin at the crossover frequency. Since there has been a good deal of research in this area, only the main take away and an illustration of the results will be presented here. Figure 5-10 shows the phase margin of loop gain without the delay and with a time delay of 50 µs. It is clear from the figure that the crossover frequency will be limited because of the delay. The key take away is that the time delay must be included in the model. Designing the control without considering the delay may result in the real system not working. In fact, in looking at the response without the delay, the phase never goes below 180° at any frequency; leaving the designer to believe that the crossover frequency can be much higher than actually possible.

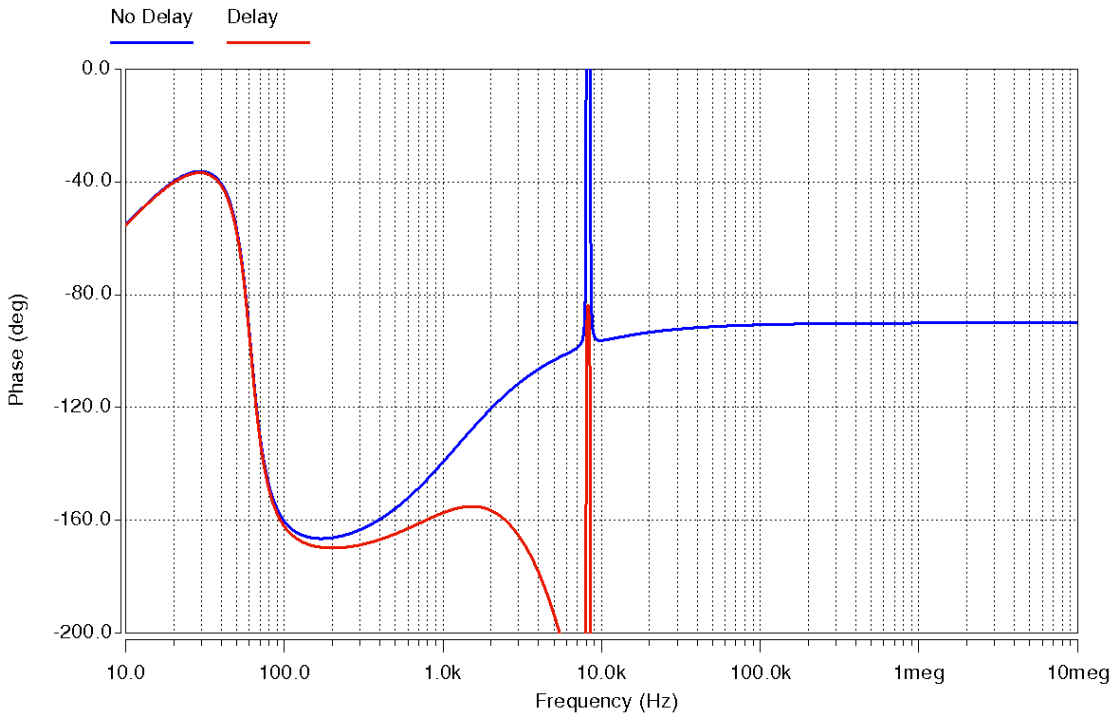


Figure 5-10: Phase margin comparison with and without delay

5.3.3. RL Load Case

The RL load is a very common load found in residential, commercial, and industrial applications. Therefore, any grid-tied converter system must be able to work with this load type. Fortunately, this load has little influence on the converter stability when controlling the converter current assuming that the grid impedance is much smaller than the load impedance. Similar to the resistive load case, the equations for the RL load can be found in abc and dq coordinates following the same procedures given earlier. These equations are given in (5-23)-(5-32). Figure 5-11 shows the equivalent circuit for the RL load condition in abc and dq components.

$$\frac{di_c}{dt} = \frac{1}{L_c} \cdot \left[d_{ab} V_{DC} - R_c \cdot i_c - V_{pcc} \right] \tag{5-23}$$

$$\frac{di_u}{dt} = \frac{1}{L_u} \cdot \left[V_u - R_u \cdot i_u - V_{pcc} \right] \tag{5-24}$$

$$\frac{dV_{pcc}}{dt} = \frac{1}{C_c} \cdot \left[i_c - \frac{V_{pcc}}{R_M} - i_L + i_u \right] \tag{5-25}$$

$$\frac{di_L}{dt} = \frac{1}{L_L} \cdot \left[V_{pcc} - R_L \cdot i_L \right] \tag{5-26}$$

$$i_{dc} = d_{ab} \cdot i_c \tag{5-27}$$

$$\frac{di_{c\_dq}}{dt} = \frac{1}{L_c} \cdot \left[d_{ab\_dq} \cdot V_{DC} - R_c \cdot i_{c\_dq} - V_{pcc\_dq} \right] - \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \cdot i_{c\_dq} \tag{5-28}$$

$$\frac{di_{u\_dq}}{dt} = \frac{1}{L_u} \cdot \left[V_{u\_dq} - R_u \cdot i_{c\_dq} - V_{pcc\_dq} \right] - \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \cdot i_{u\_dq} \tag{5-29}$$

$$\frac{dV_{pcc\_dq}}{dt} = \frac{1}{C_c} \cdot \left[i_{c\_dq} - \frac{V_{pcc\_dq}}{R_M} - i_{L\_dq} + i_{u\_dq} \right] - \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \cdot V_{pcc\_dq} \tag{5-30}$$

$$\frac{di_{L\_dq}}{dt} = \frac{1}{L_L} \cdot \left[V_{pcc\_dq} - R_L \cdot i_{L\_dq} \right] - \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \cdot i_{L\_dq} \tag{5-31}$$

$$i_{dc} = d_{dq} \cdot i_{c\_dq} \tag{5-32}$$

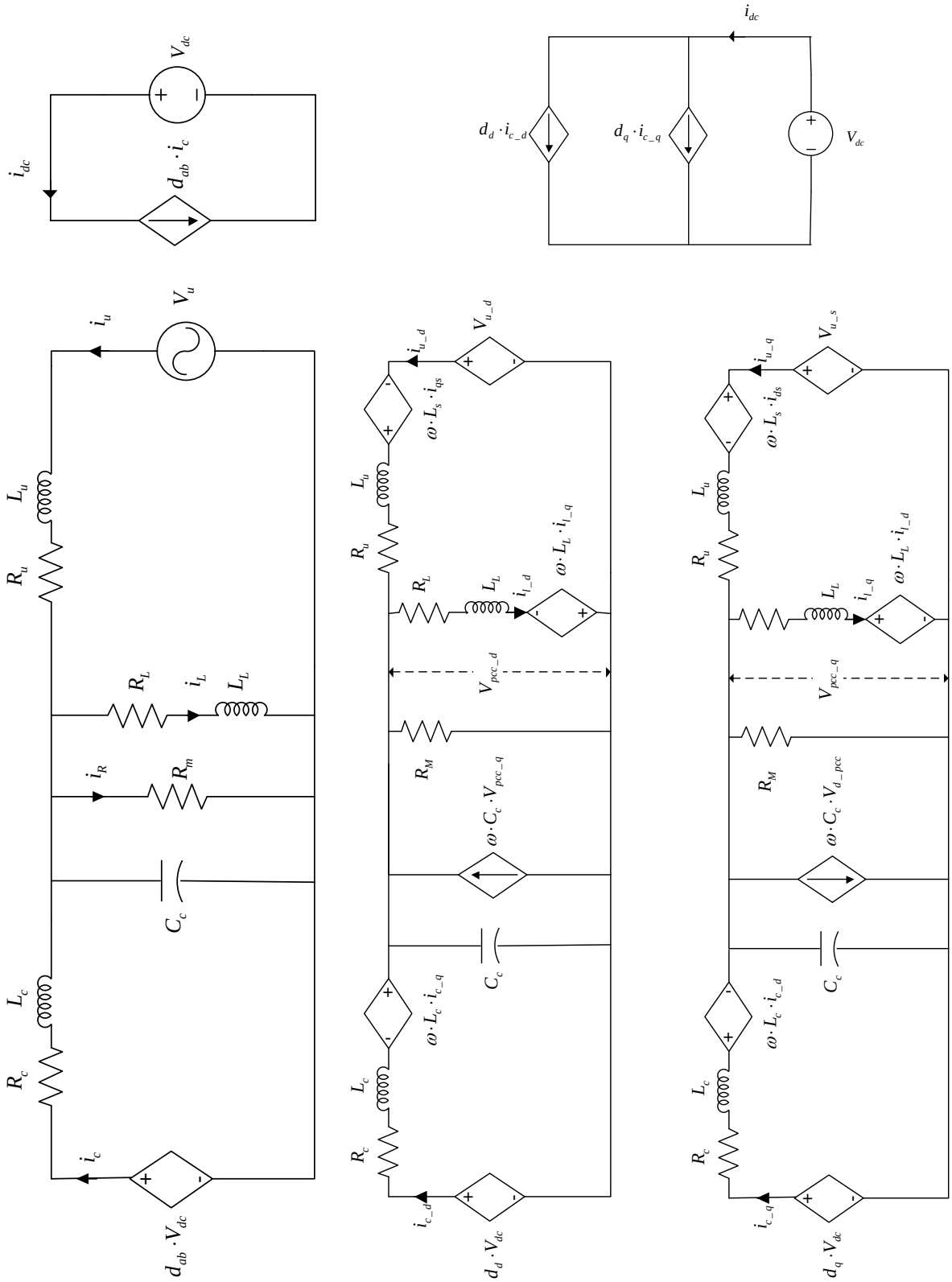


Figure 5-11: RL load abc and dq model

Figure 5-12 shows the loop gain at 10% and 100% load. It is clear that the gain and phase margin are not influenced by the load. For both cases the displacement power factor was 0.9. Since the impedance of the source is much smaller than the load, the load impedance has very little influence on the gain and phase margin under these cases. This means that from a control standpoint, the control parameters for the resistive load case will also work with the RL case. The results in Figure 5-12 can also be compared to Figure 5-8 to show the influence of the inductance.

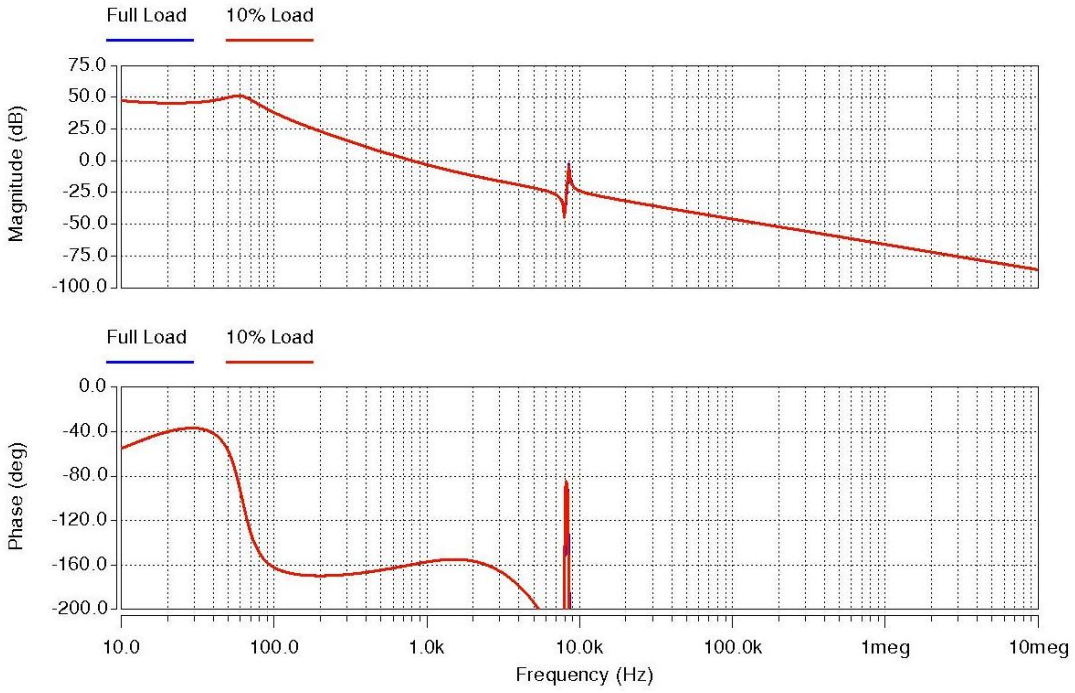


Figure 5-12: RL load comparison

5.3.4. Grid Impedance

The grid impedance has a much stronger influence on stability than the load. In the analysis that was done previously, the impedance of the grid was 10 times larger than converter, but this is not always the case. In fact, if the end user puts a transformer on the output of the converter, the transformer will most likely be close in size to the converter. Figure 5-13 shows a comparison of loop gain of the d-axis current vs. d-axis duty cycle for two cases; one when the grid is 10 times the size of the converter base and the other when they are equal. In both cases the grid impedance and base rating are the same as those given earlier in the chapter. From the figure, it is clear that when utility is the same size as the converter the system is unstable given the same values of PI parameters. Tuning the PI parameters is possible and something that can be done when initializing the system, but is not the ideal solution especially since the utility impedance is an unknown and requires circuitry to measure or predict. In order to make this system stable with a PI controller, the crossover frequency would need to be much lower resulting in a system that would be much slower to respond. Adding a resistance in series with the capacitor will increase the margins under this configuration but will increase the losses. In the next section the LCL filtering scheme will be discussed, which will describe the damping influence in more detail.

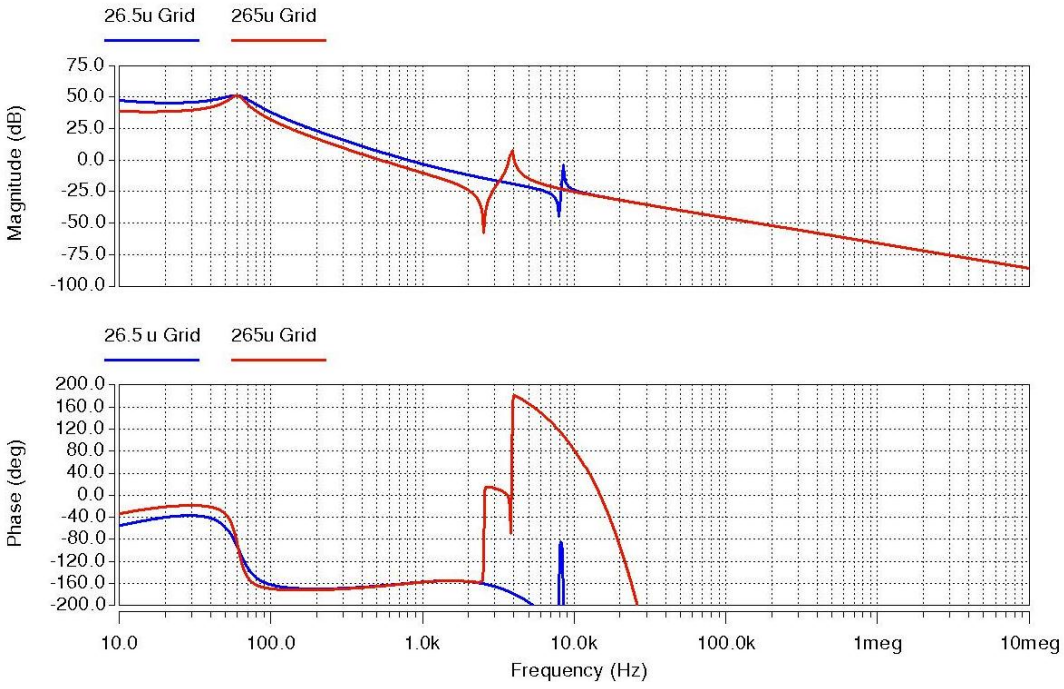


Figure 5-13 : Grid impedance comparison

5.3.5. LCL Filter

The LCL filter is a more common filter topology for grid-tie converters because of distortion requirements and variability of the load and source impedance. It is easy to see that the additional inductance would improve the output current ripple and point of common coupling voltage. However, its ability to work with a larger variety of loads and source impedances compared to the LC filter is what really makes it a better filtering choice. Of course, the additional inductance causes an increase in cost, losses, size, and weight of the filter. However, the ability to work with a larger range of load and source conditions outweighs the disadvantages in this case.

As mentioned previously, passive damping can help improve the filter's closed loop response. In this analysis, only passive filter damping will be addressed, although active damping is also possible. Damping the LCL filter comes in two variations: (1) is placing a resistor in series with the filter capacitor; (2) placing a resistor in parallel with the output inductor. Only the output inductor case will be considered in this analysis but the two methods are similar. When choosing the damping resistor for the inductor, there are three main conditions that must be addressed: (1) is the steady state losses in the resistor; (2) is the losses during transient events; (3) is the control. The steady state losses in the resistor consist of fundamental frequency and switching ripple. The fundamental frequency component can be calculated using current division given a known reference. If the control system is accurately tracking its reference, then the current entering the node of the output inductor resistor combination should be very close to this reference value since the filter capacitance is high impedance at the fundamental frequency. With a simple current division, the current flowing through the resistor can be approximated by (5-33). Although this is an approximation, this shows good agreement with simulation results in all tested cases. The real current in all cases was slightly higher than the approximation; therefore some extra headroom is advisable.

$$i_f \approx i_{\max} \cdot \frac{X_{c2}}{R_{c3} + X_{c2}} \tag{5-33}$$

In most cases, the switching ripple is small and has little influence on the total losses in the resistor. However, if the switching frequency is low or the filter cut-off frequency is high, then these losses could be a greater portion of the total losses. In these cases, the losses contributed from switching may need to be included in the calculation. Assuming that the ripple is small, (5-33) can be used to approximate losses, which shows that as resistance increases the power losses in the resistor decrease. Therefore, the resistance needs to be large enough that the power losses are not to excessive. Figure 5-14 shows a graph of the power vs. the resistance to illustrate the losses contributed by fundamental component. For this case, both filter inductors were 200 μH.

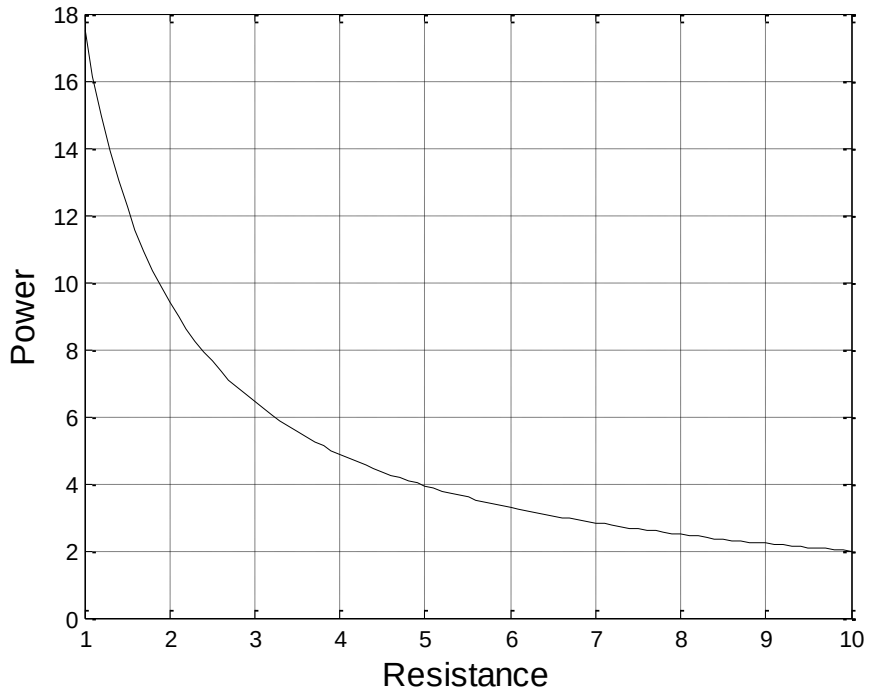


Figure 5-14: Damping resistor fundamental losses (i_{max} = 60A)

Other than the steady state losses, it is also important to size the resistance to handle transient conditions. In chapter 6, the transient behavior of the converter during typical power quality events will be discussed. During transient conditions, the current spikes through the resistor can be much larger than the maximum steady state conditions. If the resistor is only designed for steady state conditions, then it may be damaged during these transient events. If the resistor has a peak current rating or pulse power rating this should be incorporated in the selection process. Most resistors have a pulse power rating associated with them, although it may not be available in the data sheet. The designer will need to work with the resistor manufacturer to make sure the transient does not damage the resistor. In most power quality cases, the event will be related to the filter's response, which can be used to determine the peak and duration of the event. However, the designer should also consider faster events like lightning strikes.

The resistance also influences the gain and phase margin for the closed loop response. Figure 5-16 shows the equivalent circuit for the LCL filter case with a resistive load. The transformation from the abc to dq can be carried out using the same procedures as the LC filter case. After obtaining the dq equivalent circuit, the system can be linearized to perform a small signal analysis. Figure 5-15 shows a graph of the gain and phase margin of the d-axis current vs. d-axis duty cycle for different damping resistance values for two utility source configurations. It is clear from the figure that the phase and gain margins are higher at the lower resistances. Therefore, it becomes clear that choosing the resistance is a trade-off between the gain and phase margins and power losses. If the resistance is too low, the losses will be high, but if the resistance is too high, the margins are too low. The figure also illustrates the impact of the grid impedance on the gain and phase margin. Unlike the LC filter case, the LCL filter case is stable under both source conditions; although when the utility impedance is the same size as the converter, the gain margins are very low. In both source configurations, the crossover frequency was above 700 Hz given the same set of PI parameters. The crossover frequency is higher when the impedance is smaller. For this case, the system is unstable when the grid inductance goes above 350 µH. Under most conditions this should not be an issue. However, if the cable length connecting the converter to the utility is very long, the inductance may exceed this threshold. The crossover frequency would need to be decreased in order to work with a larger range of utility impedances.

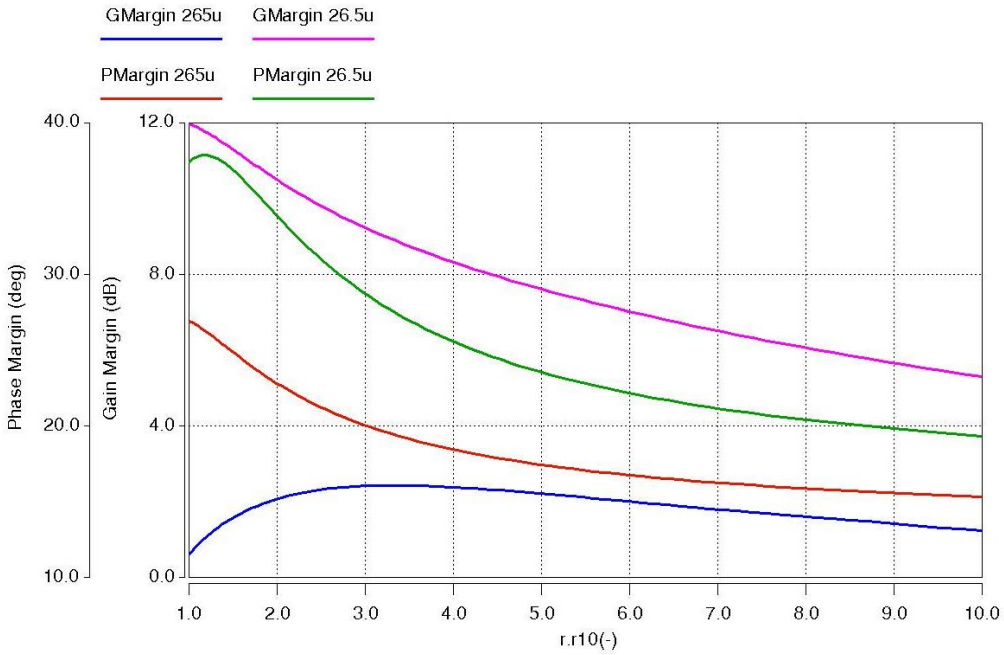


Figure 5-15: Gain and phase margin vs. damping resistance

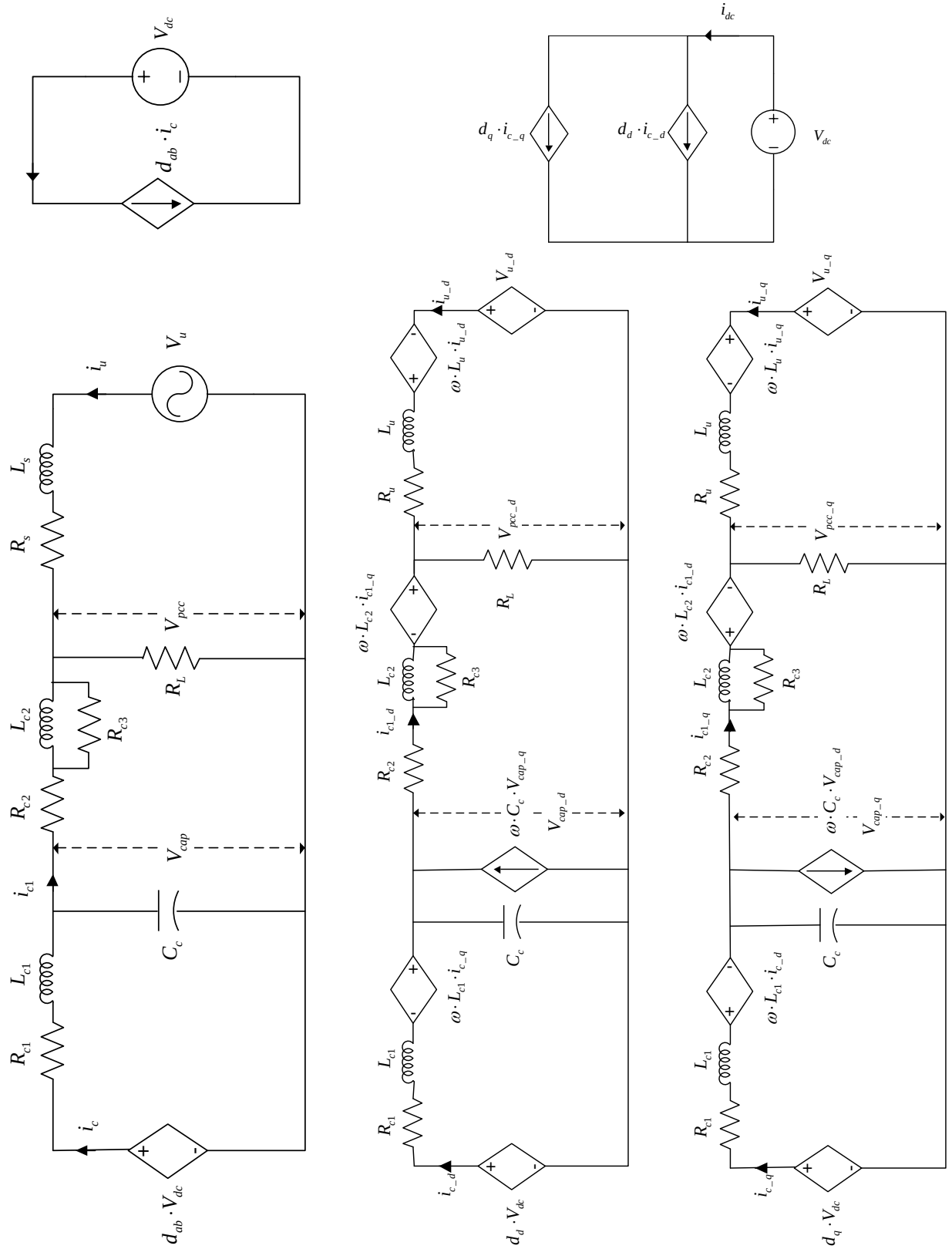


Figure 5-16: LCL resistive load

5.3.6. LCL Filter RLC load

The RL load analysis for the LCL filter case can be carried out in the same way as the LC filter case. Just as was the case with the LC filtering, the load inductance and resistance have little influence on the stability when the utility impedance is much smaller than the load, which is most often the case. While the RL load is a very common load, a combination of RLC load is actually a much more realistic scenario. The capacitance in the circuit can be contributed to the cabling, transformer winding capacitance, and any power factor correction capacitors installed on the distribution system. If the cabling is long or installed underground, the capacitance can be significant, especially when looking at stability for closed loop control. Capacitance in the system may also result from power factor correction capacitors being installed on the distribution system. Even though most converters will probably not be installed near power factor correction capacitors, the designer still needs to make sure that the converter remains stable just in case. Unlike the RL load case, the capacitance in the load does influence the stability. Therefore, the capacitance must be considered when designing the control. Unfortunately, this is not discussed much in the literature for this subject; although some have pointed out its influence [12].

Even with the capacitance, it is still possible to have a stable control system with high bandwidth and gain and phase margins. However, obtaining a single set of control parameters that works under all cases requires an iterative process where the filtering, source, and load parameters are varied and analyzed at the different conditions. Even though there are many variables in the system, it is possible to define a range for many of the variables to simplify the problem. First, assuming that the utility is at least the same size of the converter, the worst case source impedance can be determined assuming an X/R ratio and percent impedance. The utility impedance in the analysis was assumed to have an X/R ratio of 3.5 with 5% impedance over a 7.2 -72 kVA base at 120 V_{rms}. Therefore, the worst case source impedance would be the 7.2 kVA case. It should be noted that the source inductance is the main concern for stability; although if the X/R ratio is less than one, the resistance starts to have more of an influence on stability because of the damping. Second, assuming that the inductance and capacitance of the load are less than the size of the converter, then the load range can also be determined. With the load and source ranges defined, it is possible to design the filter to ensure stability and meet harmonic requirements. Designing the filter is an iterative process, although there are a few requirements that govern the design: attenuation of switching harmonics and resonances; inductance voltage drop and losses; and damping losses.

While it is possible to derive the transfer functions using Maple or Matlab for the converter, with large order systems like this it is often challenging to get meaningful information from the equations because of the high system order. Therefore, using simulations with a parametric type analysis can be more helpful when designing the closed loop control. This will be the approach taken hereafter.

The attenuation of the switching harmonics and resonances are mostly a function of the filter capacitance and inductance of the filter. As an initial step, the inductance and capacitance can be chosen based on a simple LC filter approach. This often leads to more than enough attenuation to meet the harmonic requirements under all loading and source condition and can be adjusted accordingly by the designer if not. Also, most of the resonance will occur in this region, with the exception of large capacitive loads which will also have a resonance at the lower frequencies. The filtering used in this analysis was designed based on this approach. The next question is then how to choose the inductance and capacitance in the filter? The inductance needs to be small so that the size and losses in the inductor are small, but large enough that the grid impedance does not dominate the filter response. Often, the ability to work with a large range of utility impedances overshadows the loss benefits of having a small inductance. Of course, making the inductance too large results in large voltage drops across the inductors in addition to the losses. For PV converters, the inductance should be less than 10% impedance of the converter base. It should be noted that this is not the case for all grid-tie converters. For wind turbines, the inductance is usually much larger than the grid impedance and can be as high as 20% impedance [12]. If the inductance is too small, the damping resistance required to meet the stability requirement will have high losses. In fact, originally the system was designed with 100 µH inductances for the filter, but the losses in the resistance to ensure adequate crossover and gain and phase margin where high.

Table 5-3: LCL system parameters

Parameter	Value
L_{c1}	200 µH
L_{c2}	200 µH
C_c	15 µH
R_{c3}	5 Ω
L_u	26 - 260 µH
R_u	3-30 mΩ
C_L	0.13 – 1.3 mF
L_L	5.3 – 53 mH
R_L	2 Ω-1 MΩ

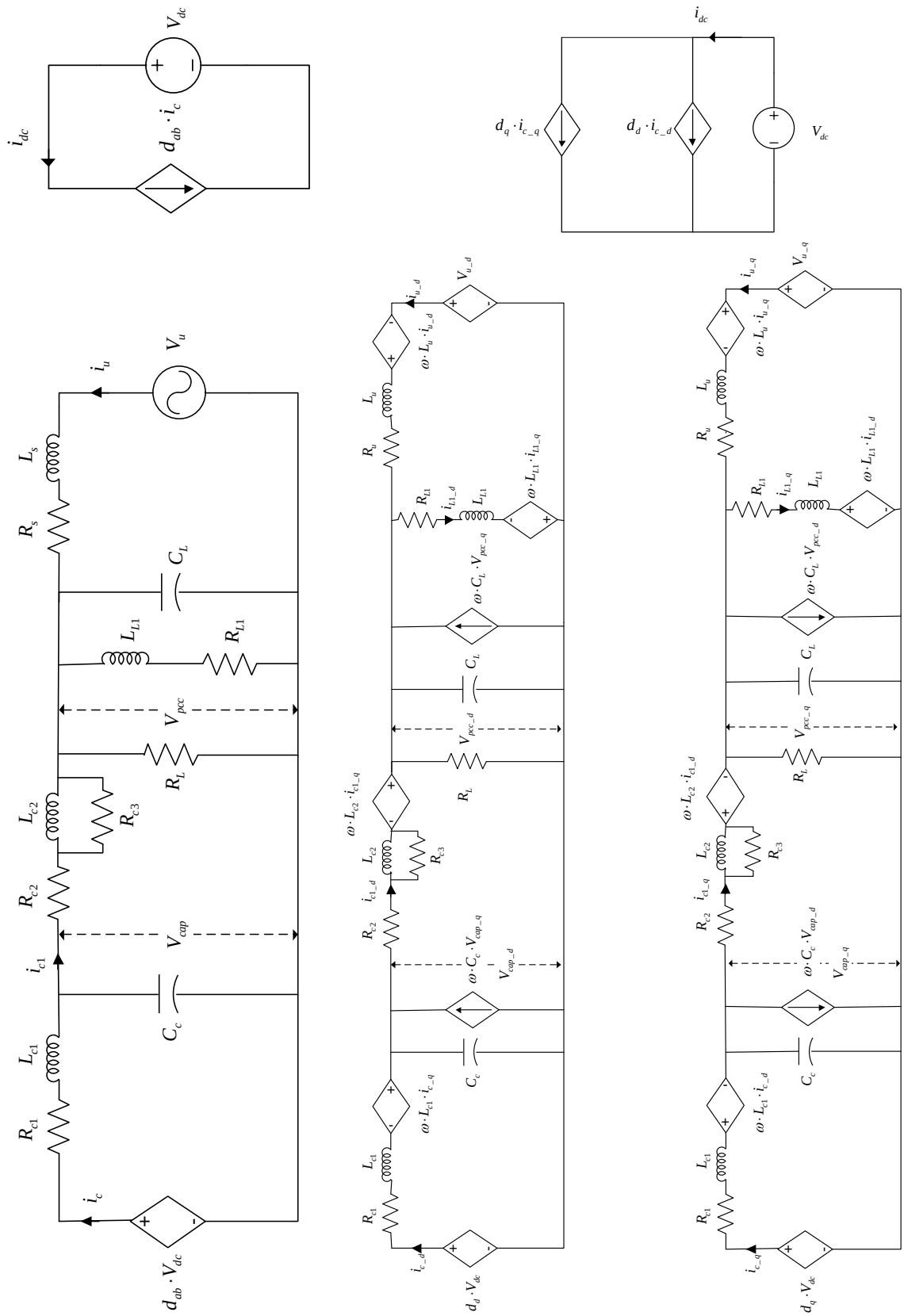


Figure 5-17: LCL RLC load

When designing the controls for the converter, the approach used to obtain the dq quantities has a significant influence on the closed loop performance. Since it was shown earlier that the time delay has a significant impact on the phase margin, it is not surprising that the ¼ cycle delay approach results in a system design with a lower crossover frequency. This is one of the primary disadvantages to this approach. By choosing the q-axis to be zero, the system is only restricted by the switching delay in the system, which allows for much more bandwidth in the control. However, this approach results in double frequency terms after the transformation and is not a true dq transformation. With both approaches it is possible to design the control system to work under all of the source and load configurations given in Table 5-3. The d-axis current vs. d-axis duty cycle loop gain and close loop response were simulated for all of the cases using a parameter sweep. For this system, the d and q axis responses are the same. Therefore, the controls for d-axis also work for the q-axis. Table 5-4 gives the control coefficients for the PI controller used for the two approaches. From the table, it is clear that the delay approach has to be tuned much lower than the zero approach because of the delay.

Since only a finite number of simulations were used in the small signal analysis, it cannot be said with absolute certainty that the converter will work over the entire range. However, generally if the step size between parameter sweeps is small enough instability conditions are noticeable in the results. The author did not notice any conditions that indicated instability in the system. After the small signal analysis, each approach was simulated for all of the possible load conditions. Since the load resistance only changes the damping, only the worst case resistive load was used. Figure 5-18 shows the delay approach with 100 different load inductance and capacitance configurations. For this particular case, the source impedance was assumed to be $1/10^{th}$ of the converter base impedance. However, the entire range of the source impedances was simulated in the analysis. For each of the load parameters, ten values were chosen within the range of values given in Table 5-3. It is clear from Figure 5-18 that the converter is able to work with all the different load configurations. In Figure 5-18, a voltage sag of 3 cycles is applied to the system at 33.3 ms. The behavior of the converter during voltage sags will be discussed in the next chapter. The voltage sag was only used to ensure proper settling and overshoot.

Table 5-4: LCL control coefficients

Parameter	Value	
	Zero-Q-axis	**¼ Cycle Delay**
kp	0.005	0.01
ki	50	1

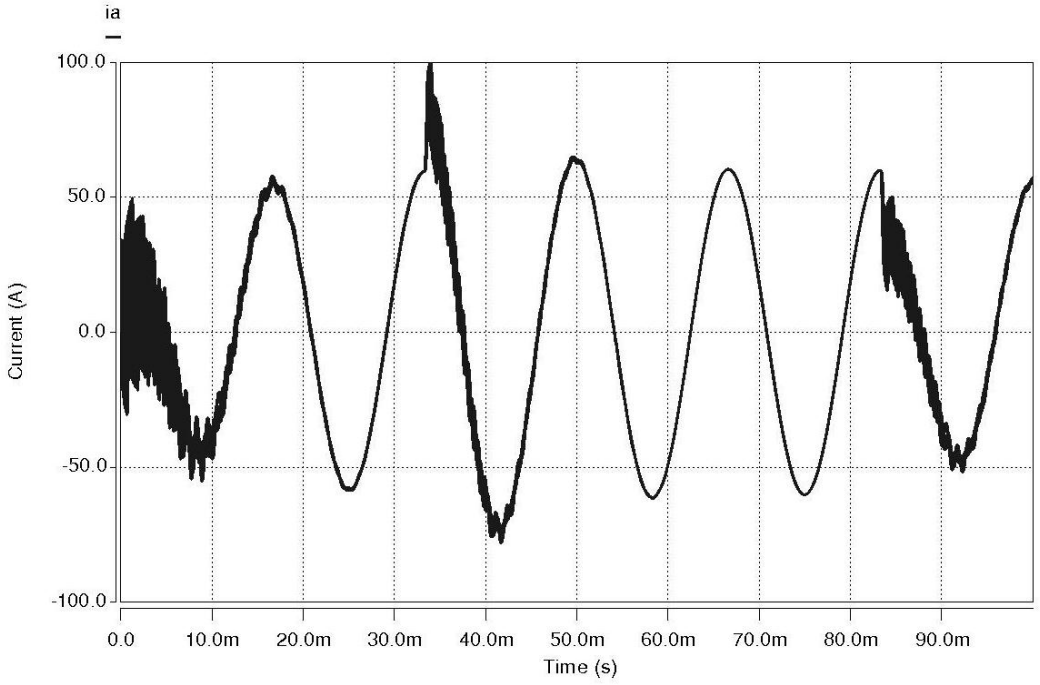


Figure 5-18: LCL voltage sag event

5.4. DC Bus Variation

Since the most efficient transformerless PV inverters on the market today connect the PV array directly to the DC bus, there is no intermediate DC/DC converter between the array and inverter to smooth out DC variations of the PV array caused by changing weather conditions; meaning that the inverter must be able to attenuate any low end harmonics to avoid them from showing up on the output of the inverter. Since the DC perturbations caused by weather conditions are slow, typically the inverter control has enough gain at the low frequency to attenuate any low frequency variations on the DC bus voltage. However, if the gain is low or the variation is quick, these DC variations can show up on the output of the inverter. To illustrate this concept, a 10 Hz 100 V variation was placed on the DC side of the inverter. While 100 V and 10 Hz is a very extreme variation for these types of events, this is used to illustrate the concept and show the difference between the two different dq approaches. Figure 5-19 shows the output current of the converter using the two different approaches. It is clear that the delay approach has much more of the 10 Hz signal pass through to the DC side, contributed by the lower gain and crossover frequency required to make the system stable. At 10 Hz, the delay approach has ~20 dB of attenuation and the zero q-axis approach has ~40dB. Even though this is an extreme case, the designer needs to be aware of this to make sure that control has enough gain at the low frequencies to ensure that the inverter does not pass these low frequencies variations to the utility. While Figure 5-19 makes it appear as if the delay has unacceptable performance, both designs provide adequate

attention for low frequency variations on the DC input. Of course, with more gain at the lower frequencies, the zero q-axis approach has much better performance. Most variations caused by weather conditions in PV applications will be much less than 10 Hz, so with properly designed control this should not be an issue.

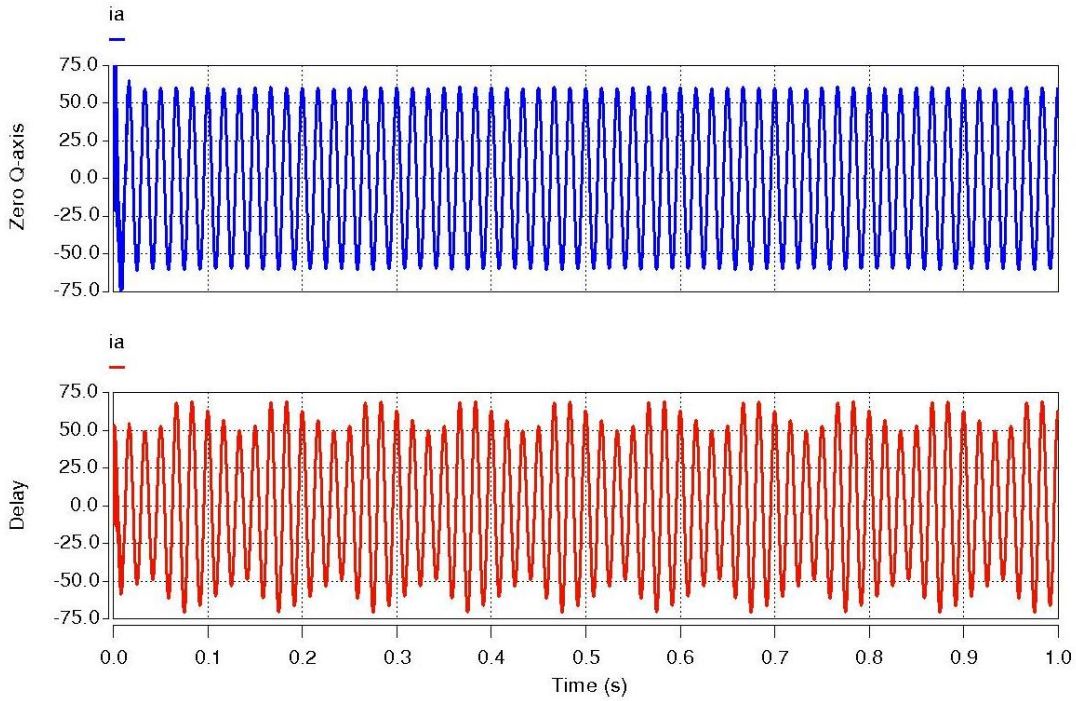


Figure 5-19: DC bus variation comparison

5.5. Dead Time

While the main focus of this chapter is on average models and controller design, it is important to briefly discuss dead time and other switching inconsistencies that occur in the real converter and how they are affected by the controller design. It is well understood in the power electronics field that low frequency harmonics result from dead time and other switching inconsistencies and that these harmonics cause an increase in total distortion and can even lead to instability. In order to deal with this, there have been many compensation techniques proposed in literature over the years to provide volt/sec balancing. Most of these techniques require the polarity of the current to determine whether there is an increase or decrease in the volt/sec during the dead time, which may require additional hardware and software functionality. In an open loop system, this is extremely important since without feedback this unbalance can lead to highly distorted waveforms. In a closed loop system, the dead time compensation is often not needed because of the control. In order to determine if the dead time is a problem, during the controller design it is very important that the designer investigates the output behavior. Ideally, the designer would prefer not to have to provide dead time compensation since it requires additional hardware and code, but this might be unavoidable.

For grid-tie converters, the reactive power cases are the most important conditions to investigate since they result in the most distorted waveforms. To illustrate the importance of this, Figure 5-20 shows the inverter output current in real and reactive mode. In both cases the dead time was 2 μs with a switching frequency of 20 kHz. It is clear from the figure that the reactive current is much more distorted than the real current. Therefore, if the converter is only designed by investigating the real power case, the reactive current condition may not meet distortion requirements. Since in most PV applications in the U.S. the converters only provide real power, the reactive case is not presently an issue. However, as the utilities start to use more renewable sources and allow for converters to provide voltage support, this issue will need to be addressed by the system designer. In many cases, this is not just a simple firmware upgrade to allow for the converter to provide reactive power. Of course, if the converter is designed in the beginning with dead time compensation this should not be an issue. However, adding the compensation increases the complexity of the software and in some cases requires additional hardware.

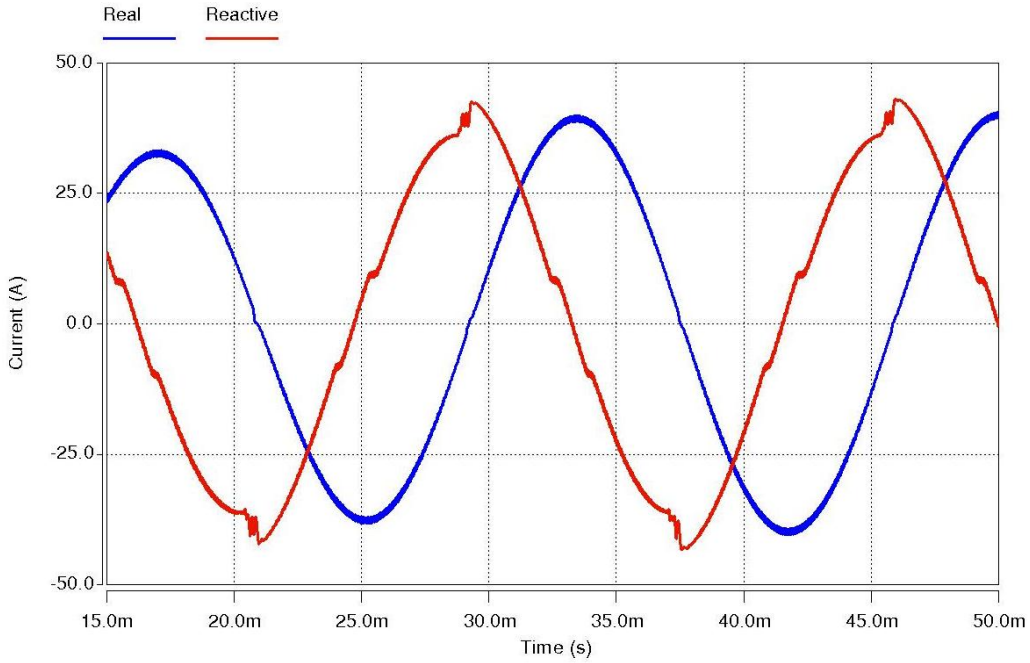


Figure 5-20: Dead time comparison

5.6. Harmonic Injection

When designing a grid-connected converter for harmonic compensation, the bandwidth of the control system determines the capability of the converter. The more bandwidth the controller has, the more harmonic compensation is available. Of course, increasing the bandwidth of the controller generally comes at the expense of decreasing phase and gain margin. Therefore, if the bandwidth is increased to provide more compensation capability, then the transient behavior of the system may no longer be acceptable. There will always be this tradeoff between harmonic capability and transient performance for this type of compensation. Often, the transient response takes precedence since the transient nature can lead to degradation and even failure of the semiconductor devices. To determine the harmonic compensation capability of the system, the closed loop response for the current vs. duty cycle relationships are used. Since the d and q axis are similar for this type of converter, only the d-axis will be shown. Figure 5-21 shows the closed loop response for the d-axis current vs. d-axis duty cycle for the LCL filtering case. The parameters for the filtering can be found in Table 5-3. When looking at the figure, if the magnitude is close to 0 dB then the converter will accurately track the reference at this frequency. If the magnitude is greater than 0 dB, then the current output will be larger than the reference. If the magnitude is less than 0 dB, then the current will be smaller than the reference. To illustrate the compensation capability, Figure 5-22 show the average model simulation results when trying to track the current of a single phase diode bridge rectifier. At the low frequencies, the controller is able to track the reference value very

well, which is in agreement with the results of Figure 5-21. The frequencies between 400 – 1000 Hz are higher than the reference current, which looking at Figure 5-21 shows gain in these regions.

These results illustrate the importance of the bandwidth of the controller when trying to provide harmonic compensation. It should be noted that these results are with the zero q-axis dq approach. With the ¼ cycle delay approach, the frequency range of compensation for the converter will be lower because of the bandwidth limitation caused by the delay. When trying to provide harmonic compensation, the zero q-axis is a better choice for the dq transformation because of the higher crossover frequency.

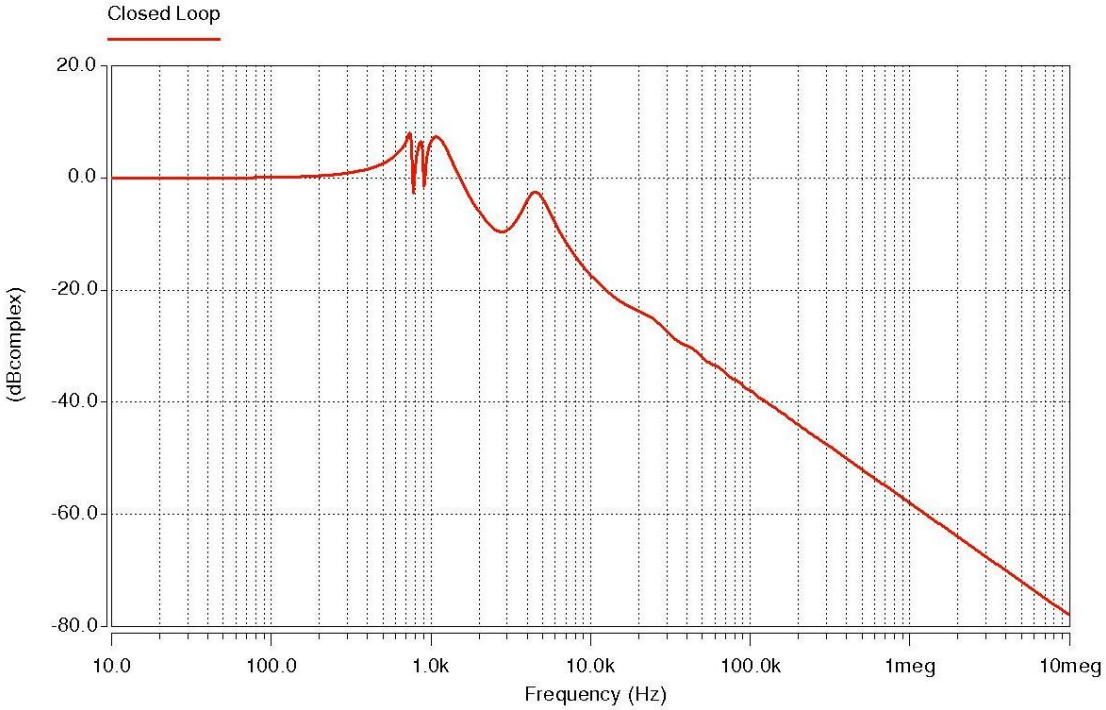


Figure 5-21: i_d/d_d closed loop response

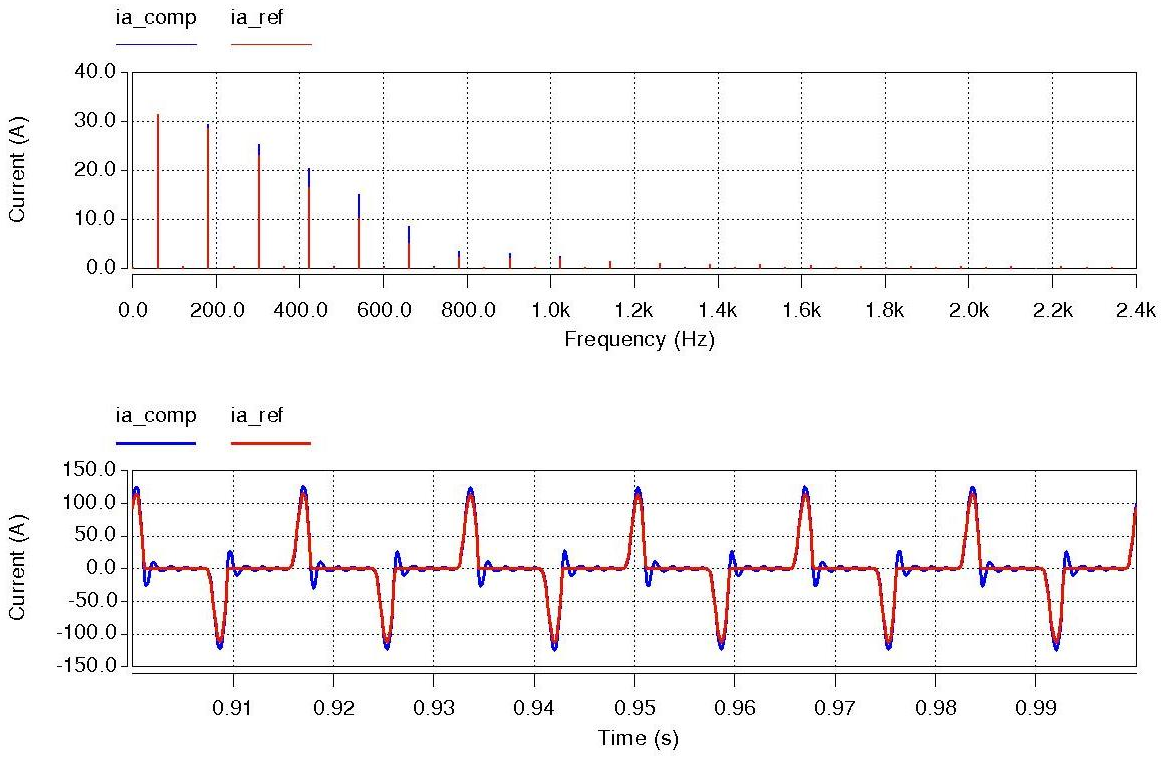


Figure 5-22: Harmonic current compensation

Other than the bandwidth, the area around the cross over frequency is extremely important since as we saw in the previous graphs that it leads to the output being higher than the reference value. These conditions are a function of the load, source impedance, filter, and controller parameters. In the previous sections, the source and load were discussed in terms of stability, but now it is clear that the load and source will also influence the controller's ability to track a non-sinusoidal reference. This is one of the reasons why most STATCOM and active filtering solutions are custom. Without knowing information about the source and load impedance, harmonic current compensation can be a very challenging problem. It should be noted that the conditions that go below 0 dB are not necessarily problematic since the output is less than the reference value. To illustrate the load on the controller's compensation capability, Figure 5-23 shows the response under two different capacitive load conditions. The first case is when load is 1.4 mF and the second case is when the load is 0.14 mF. The changes for the inductive case are small for the reasons discussed in the previous section which is why they are not shown. The source impedance for both cases in the figure was $1/10^{th}$ of the converter base impedance. While the two case have overall similar responses, the resonance around the crossover are distinctly different. For harmonic compensation, the smaller capacitance has a worse response because of the closer interaction with the converter filter. For both cases, the frequency range between 400 Hz and 1050 Hz is not very good. In order to increase the frequency range of compensation, the bandwidth of the controller needs to be

increased. For both load cases, the crossover frequency is ~1 kHz, which corresponds to the peak in the closed loop response. The easiest way to increase the crossover frequency is to raise the cut-off frequency of the filter. However, if the cut-off of the filter is too high the output will contain high amounts of switching ripple which may not be acceptable for grid-tie connection. The other option is to increase the switching frequency in conjunction with the filter cut-off frequency, which will increase switching losses but allow for the switching ripple to remain low and crossover to be raised. These results show that in order to track the single phase rectifier reference current, the converter crossover frequency should be in the 5-6 kHz range, which would most likely require the switching frequency to be in the 60-100 kHz range using simple PI compensation. Although not shown in the graphs, the phase of the compensation is also important for harmonic compensation. In a real converter designed for harmonic compensation, the converter would more than likely be injecting frequencies that are 180° out of phase with the diode current harmonics to compensate for the current. Therefore, the phase changes are also important for this type of compensation.

The source impedance also affects the frequency range of the compensator. For Figure 5-21-Figure 5-23, the source impedance was 1/10th of the converter base impedance assuming 5% impedance and a 3.5 X/R ratio. When the impedance of the utility is the same size as the converter, the crossover frequency is lower and has a larger peak in the closed loop response. This creates larger differences between the reference and actual current. It is worth noting that in both cases neither ESR or load resistance were included in the model. With the addition of the resistance, the harmonic compensation would be better for both cases. These results show worst case.

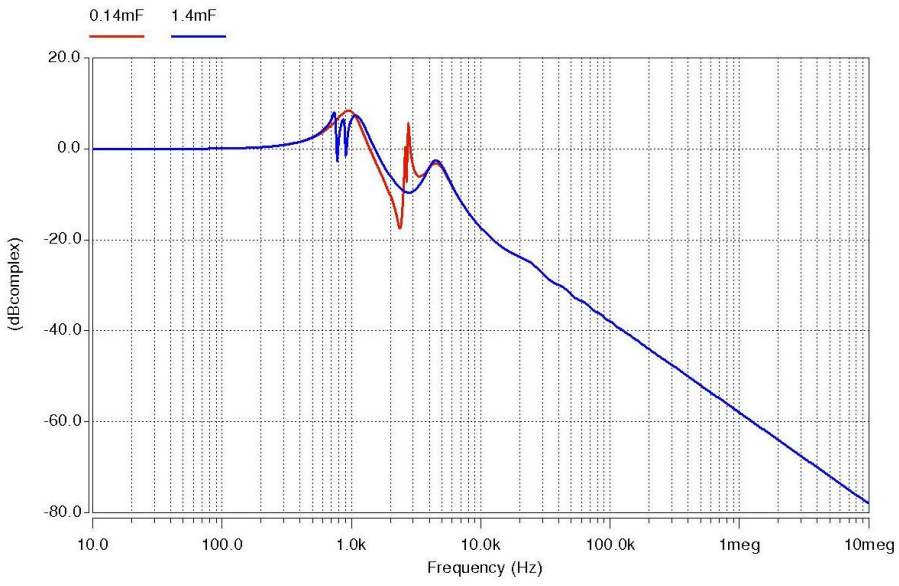


Figure 5-23: Load influence on compensation capability

5.7. Source Distortion

In the previous sections, the effect of the dead time on the output distortion was discussed and shown to be influenced by the real and reactive power. This analysis will address how the converter responds to grid input voltage distortion. Although in a real system, the distortion is a combination of the converter distortion and utility distortion, we will assume that the distortion caused by the converter is negligible. This is typically the case if the pf of the converter is unity or dead time compensation is added to the control. For an ideal converter, the output current of the converter would be not be changed by the grid distortion. However, in a real converter this is rarely the case. In fact, maintaining low harmonic current distortion levels is a very challenging design problem leading designers to use sophisticated control techniques such as multiple synchronous reference frames or PR controller tuned to harmonic frequencies to minimize the distortion. While these approaches are very effective at lowering the distortion, they increase the complexity of the control system and are much more difficult to implement. As we will see, depending on the current distortion requirements, these techniques might not be needed if the control system is properly designed.

To illustrate how the converter responds to distortion on the utility input voltage, a single phase rectifier was used to create a distorted harmonic voltage waveform at the utility input to the converter. Figure 5-24 shows the voltage harmonics seen at the PCC between the utility and single phase rectifier load. The THD of the waveform is given at the top of the graph. From the figure, it is clear that the 3^{rd}, 5^{th}, and 7^{th} harmonics are the dominant harmonics in the voltage. Therefore, for this type of distortion it is clear that the converter needs to be able to attenuate the low end harmonic frequencies in order to have low current distortion. It should be noted that in most utility cases the low end harmonics are dominant in the utility supply voltage. Therefore, for multiple synchronous reference frames or PR with harmonic compensation the 3^{rd}, 5^{th}, and 7^{th} are the target frequencies because of their dominance in the power system. Figure 5-25 shows the grid current distortion when the voltage is applied at the input using the zero q-axis dq transformation with a single reference frame. Since the harmonics are only marginally affected by the fundamental output current of the converter, as the load level is decreased the harmonic distortion becomes higher. At 33% load, the current is still less than 5% THD, which with no additional compensation techniques is good for a grid tie connection. When comparing the harmonic spectrums of the input voltage and current, it becomes clear that the 3^{rd} and 5^{th} harmonics are being attenuated by the control in the converter. Beyond the 5^{th}, the harmonic distribution of the current and voltage are almost the same. To show why this is occurring, Figure 5-26 shows the d-axis admittance loop response from the dq small signal model.

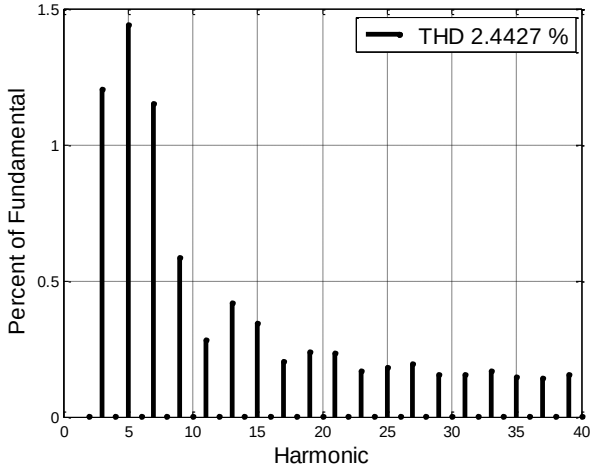
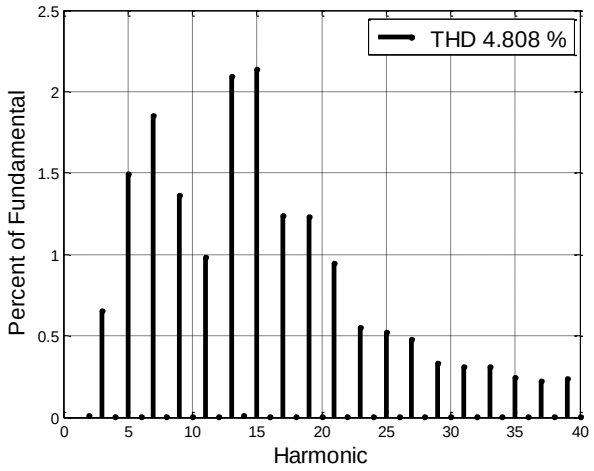
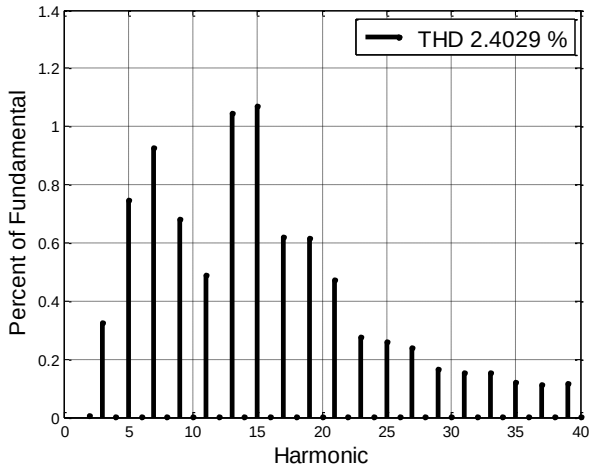


Figure 5-24: Voltage distortion PCC



33 % Load



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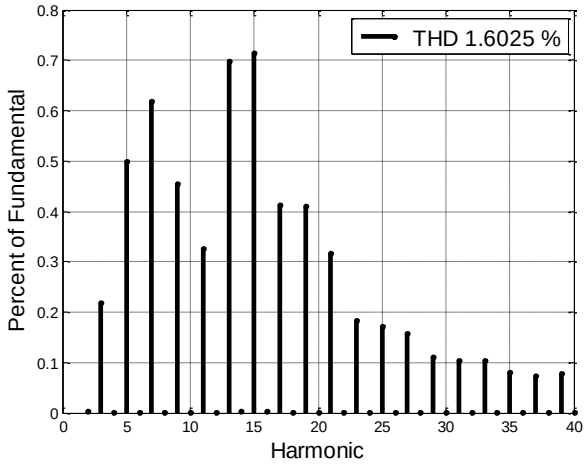


100% Load

Figure 5-25: Zero q-axis current distortion

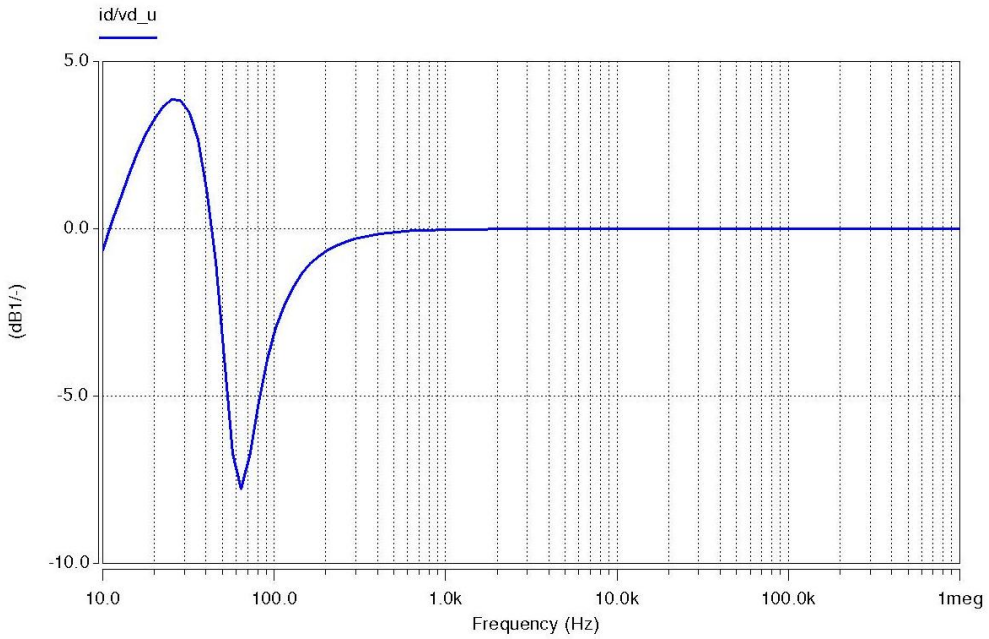
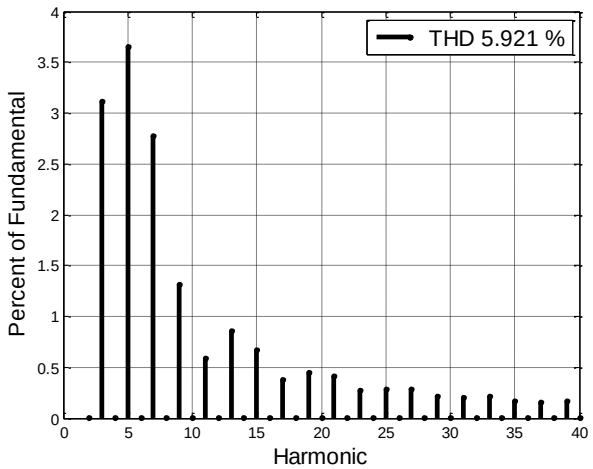


Figure 5-26: D-axis admittance

When the ¼ delay approach is used for the dq transformation, the distortion is slightly higher than the zero q-axis approach. This is a result of the controller being tuned to such a low crossover frequency as described in the previous chapter. Figure 5-27 shows the current distortion for the ¼ cycle delay approach. Comparing the current harmonic distribution with voltage harmonic distribution, it is clear that the harmonics have the same harmonic distribution indicating a flat transfer response. While the THD is slightly higher than the zero q-axis approach, the amount of distortion is still reasonable with a single reference frame approach.



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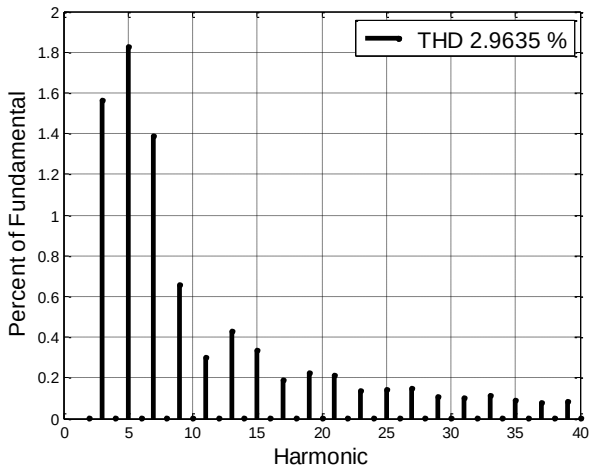
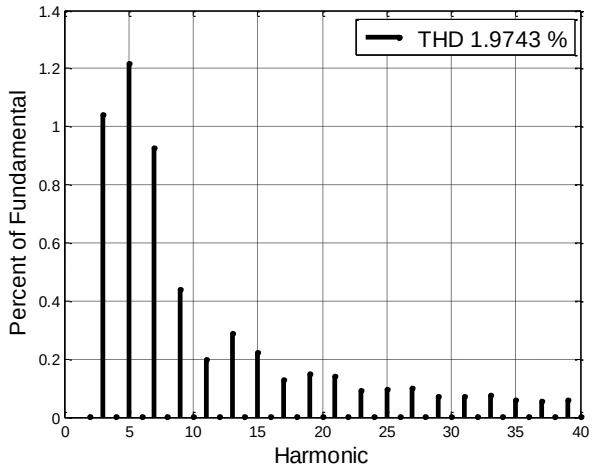


66 % Load



100% Load

Figure 5-27: ¼ delay current distortion

5.8. Summary

In this chapter, the dq and small signal models were developed for the single phase grid-tied converter. The chapter started by deriving the average models for the system and then used a pseudo dq transformation to transform the system to DC quantities. A few of the common techniques used for single phase dq transformations were discussed and compared. In the small signal analysis, the influence of the source and load impedance on the stability margins was discussed. The importance of the damping in the filter was also discussed. The control system was designed over a large range of source and load configurations from the small signal results using a simple PI controller. The average large signal model was used to validate the results over a large range of load and source conditions.

With the control system in place, the converter's response to voltage variations on DC side were compared for two of the dq transformation techniques. Since the ¼ cycle delay approach results in lower gains, more of the signal passes through for this approach. However, both approaches have acceptable performance under low frequency DC variations. The dead time was also discussed in relation to the closed loop control. Although the distortion was fairly low, dead time compensation is still probably needed for the converter in reactive power mode. Using the results from the small signal analysis, the converter response to voltage distortion and its effect on the converter current was discussed for both the zero q-axis and ¼ delay approaches. Both converters have low current distortion under fairly distorted voltage waveforms. Of course, under lighter loading conditions the current distortion is higher but is still acceptable. The control system's ability to provide harmonic compensation was also addressed in the chapter. As one would expect, the bandwidth of the control system determines the frequency range in this mode of operation.

Chapter 6.Grid-Tie Converter Dynamic Response

For grid-tie converters, the behavior of the system during dynamic conditions is an essential part of the design. Since the system is grid connected, the transient behavior of the grid as well as steady state condition both influence the converter performance. In the previous chapter, harmonics and steady state conditions were addressed. In this chapter, the tranisent behavior of the system converter will be addressed. The transient behavior is mostly contributed to the load and source voltage. Often, the impedance of the utility does not change dynamically. Therefore, modeling the transformer and cable feeding the transformer as a constant is sufficient for most cases. The load and the voltage on the other hand are constantly changing.

The grid connected converter transient behavior is different than traditional DC/DC converter transient design because the load cannot be modeled as a simple passive network. The load exhibits transient behavior that must be incorportated into the design. For instance, when a motor starts or a transformer is energized, the control needs to ensure that the converter does not overload because of the large current demands. In fact, in most cases, it is preferred that the converter not participate in transient conditions at all. Unfortunately, this is not possible in all cases because of how the control system reponds. As a final note, this chapter does not include all of the power quality problems. However, the author did try to address the more common issues.

6.1. Capacitor Switching

When a capacitor bank is switched on in the utility system, a switching transient can occur because of the interaction with the utility inductance. This transient can cause a voltage overshoot which can cause loads downstream to trip off-line. In industrial environments, capacitor transients are a common cause of motor drive tripping off-line [10]. Since the voltage cannot change instantaneously across the capacitor, if there is a difference between the utility voltage and the capacitor's initial voltage an inrush current will result during the event. If the voltage difference between the capacitor and the utility happens to be large, then this event can lead to large inrush currents. The damping of the transient will depend on the resistance in the system. With little damping in the system, the transients can lead to fairly long oscillatory transients. It is also possible for the one capacitor switching event to interact with other capacitor banks and amplify the event even further [10].

For grid connected converters, we want to make sure that the overvoltage event does not cause any overload or instability issues. Using the single phase grid tie converter with LCL filtering, the converter's behavior during a range of capacitor switching transients was simulated. For this case, the capacitor was the only load on the system to simulate a worst case scenario. Of course, any load resistance will damp this response. Figure 6-1 shows voltage at the point of common coupling voltage and the converter current over a range of capacitor switching condition. In each case, the capacitor is switched on at 500 ms and is initially discharged. The source impedance and capacitor range are given in the caption of the figure. When the voltage at the point of common coupling has a change, the converter current will overshoot because this causes the voltage at filter capacitor to also change. It is worth noting that the oscillator behavior of the event is not the problem. It is the initial change in voltage that causes the current overshoot. Later in the chapter, voltage sags and swells will be shown to cause the same type of current overshoot.

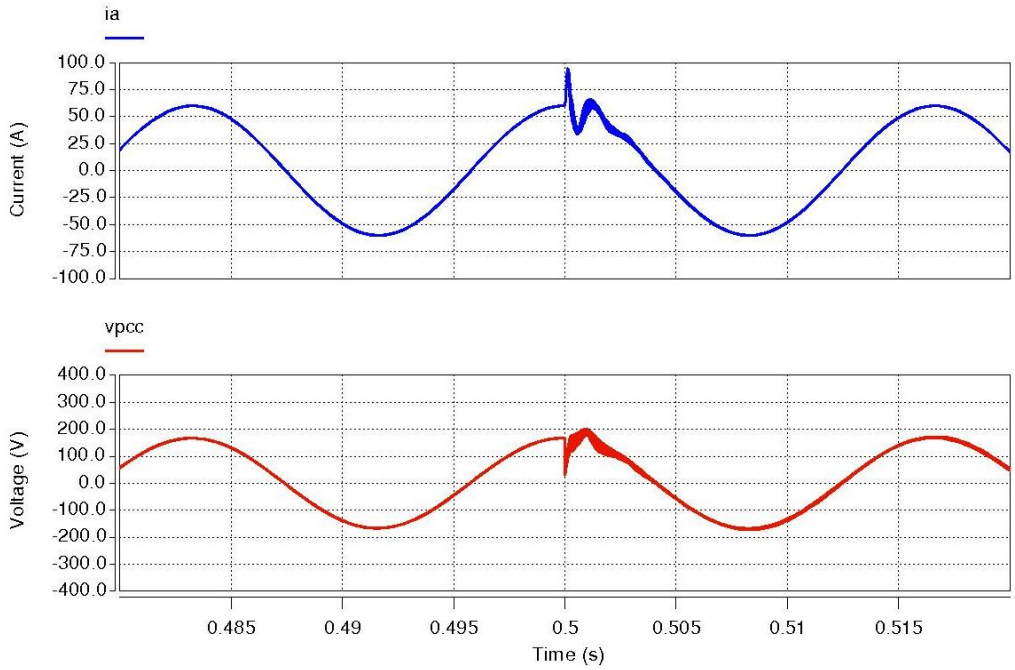


Figure 6-1: Capacitor switching response 0.14-1.4 mF (10 steps)

When looking at Figure 6-1, it is clear that the system has a lot of damping. However, since the capacitor is the only load in the system, this means that the damping is coming from the utility and converter. With a little investigation, we see that most of the damping during the event is coming from the resistor in parallel with the output inductor. This is why in the previous chapter the importance of sizing the resistance based on transient behavior was stressed. If this is not considered, the large amounts of energy during transient events can lead to failure of this damping resistance. Figure 6-2 shows the current through the damping resistor during the event. The nominal rms current through the resistor is less than one ampere but during the transient event the peak current reaches almost 30 A. As a designer we cannot rely on utility damping. Therefore, when designing the converter for transient events, it is crucial to understand the transient capabilities of the passives as well as their steady state capabilities.

Since there are so many different transients that can occur on the power system, trying to determine a worst case condition to design around can be very challenging. For capacitor switching events, excluding interactions from other capacitor banks, the worst case capacitor voltage is typically when the capacitor bank is initially charged at the opposite polarity of the utility voltage during the event. Most often this happens during reclosures when trying to clear a fault. Although this case was simulated, the author did not feel that the results were accurate since the current spikes were above 2 pu without including saturation of the inductor. Unless the inductors were designed with a lot of extra headroom, a 2 pu current spike would cause the inductors to saturate. This would lead to the current being even higher than 2 pu. Overall, this is a challenging problem to design around because of the large amounts of current. However, if the overload protection is designed properly, the converter should at least turn off if the current is high enough to damage the switches. Even though the switches will likely be protected, the author wants to reiterate that the passives, such as the damping resistor, may still be damaged during the event if not properly sized. During the voltage sag and swell discussions, a method for minimizing this transient will be discussed.

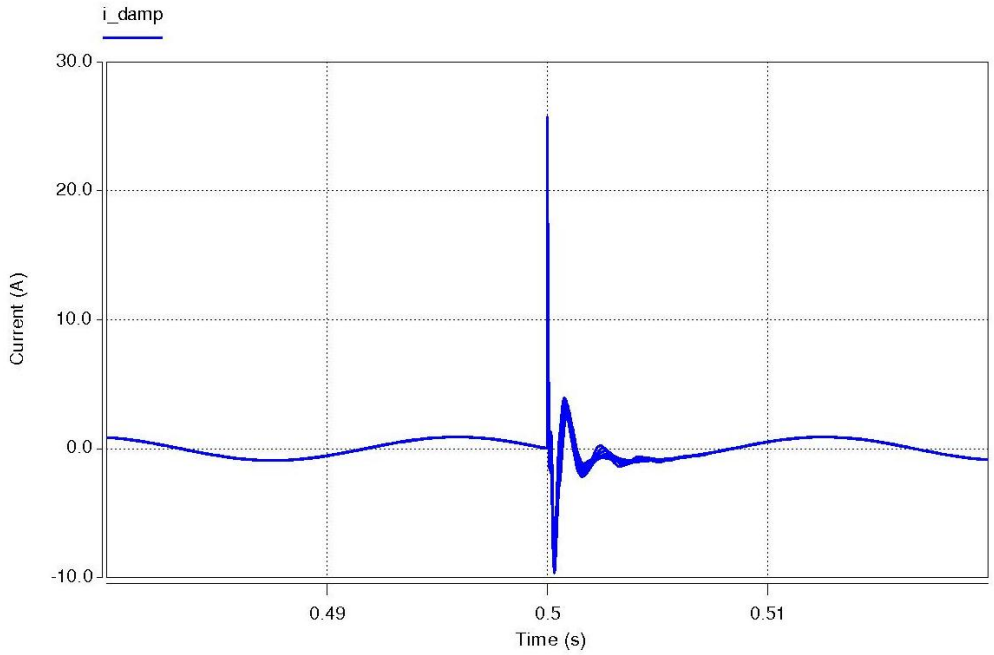


Figure 6-2: Damping resistor current during capacitor switching

6.2. Inrush Current

Energizing magnetic loads such as transformers and motors can cause large amounts of inrush current. To determine how the converter responds to this type of event, a simple model was developed to imitate transformer inrush current. The model tries to capture the non-linear magnetic properties of the transformer and saturation by using a 3rd harmonic and exponential function. Since the third harmonic is dominant in the magnetizing current for most single phase transformers, this was the only harmonic included in the analysis. Other harmonics can be included if a more accurate waveform is desired. Equation (6-1) gives the mathematical expression used to model the inrush current. Table 6-1 gives the values used in the model, and Figure 6-3 shows a graph of the inrush current using the expression in (6-1) and values from Table 6-1. It should be noted that the purpose of this analysis was to capture the overall shape of the current. This was not intended to be an extremely accurate model for the inrush current. If the reader is interested in more accurate models for transformer inrush, the works in [20-22] have very detailed models which accurately capture the harmonics and saturation. For this case study, the harmonics in the current are of little concern. Harmonics typically are a steady state issue, and since the magnetizing current is usually less than a few percent of the full load current, the voltage distortion caused by the magnetizing current is small under steady state conditions. Also, it was already shown that the low frequency voltage harmonics result in little current distortion under even light loading conditions with the current control system. Since the magnetization current is such a small percentage of the load current, the amount of voltage distortion at the PCC during steady state conditions from transformer magnetizing current is

negligible. During the actual inrush event, since the current is rich in harmonics this can create overvoltage conditions if there happens to be a parallel resonance condition at one of harmonics [10]. For this analysis, no capacitors other than the filter capacitor were included, and parallel resonance with the filter was not an issue.

$$i_{inrush} = \left[i_{\max} \cdot \sin(2\pi f \cdot t) + i_3 \cdot \sin(6\pi f \cdot t + \frac{\pi}{2}) \right] \cdot e^{-t \cdot \tau} + i_{\max} \cdot e^{\frac{-t}{\tau}} \quad (6\text{-}1)$$

Table 6-1: Insrush parameters

Parameter	Value
I_{max}	600
I_3	150
τ	10

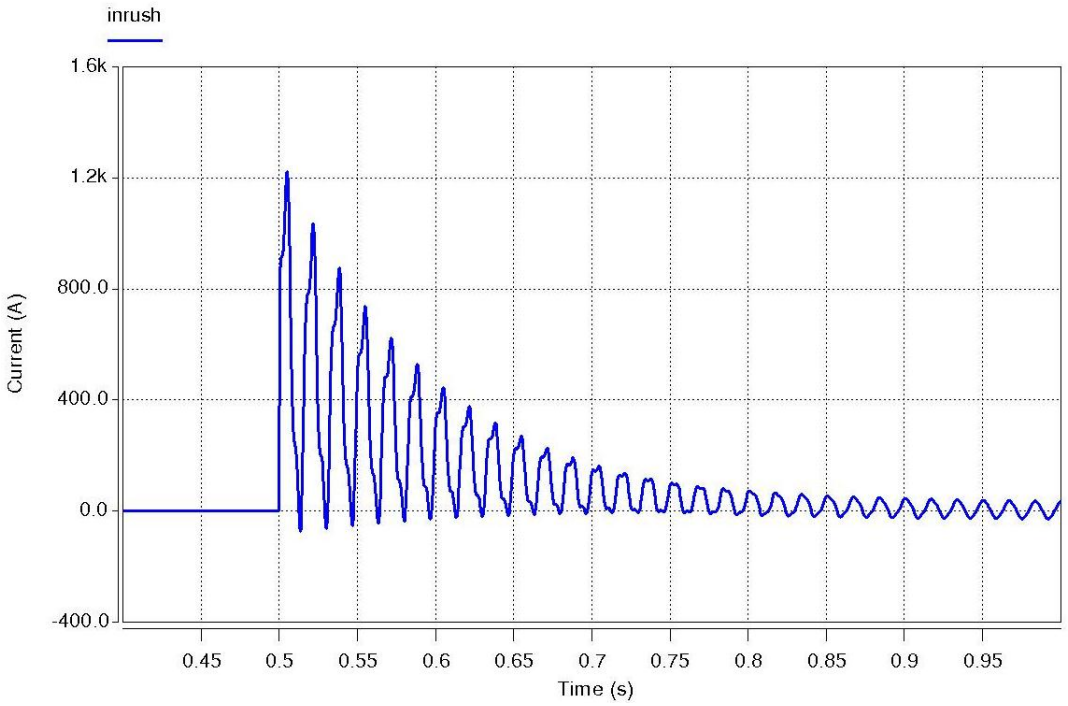


Figure 6-3: Transformer inrush

From an operational standpoint, during the inrush event we want to make sure that the converter does not overload. Because of the substantial amount of inrush current being drawn from the load, the control needs to ensure that the utility is supplying the current. Since the converter is controlling the current, the control system is able to regulate the current, leaving only the utility to supply the inrush current. Figure 6-4 shows the utility and converter current during the inrush event. It is evident from the figure that the utility is supplying the inrush current. The transient in the converter current during the initial event is caused by the voltage transient at the PCC. Since the voltage drops during the inrush current, the converter response is similar to what was shown during the capacitor switching analysis in the previous section. It should be noted that the voltage transient is a function of the utility and will be worse for weaker sources. For the case shown in Figure 6-4, the utility was 10 times the size of the converter base. With a smaller utility, the event would be worse. Of course with a smaller utility, the load transformer is not likely to be as large as the one used for this analysis; meaning that the inrush current would be smaller. The worst case would be when the utility transformer and load transformer are similar in size. In this case, the voltage transient would probably cause a current overshoot that would overload the inverter unless corrective action is taken during the voltage change.

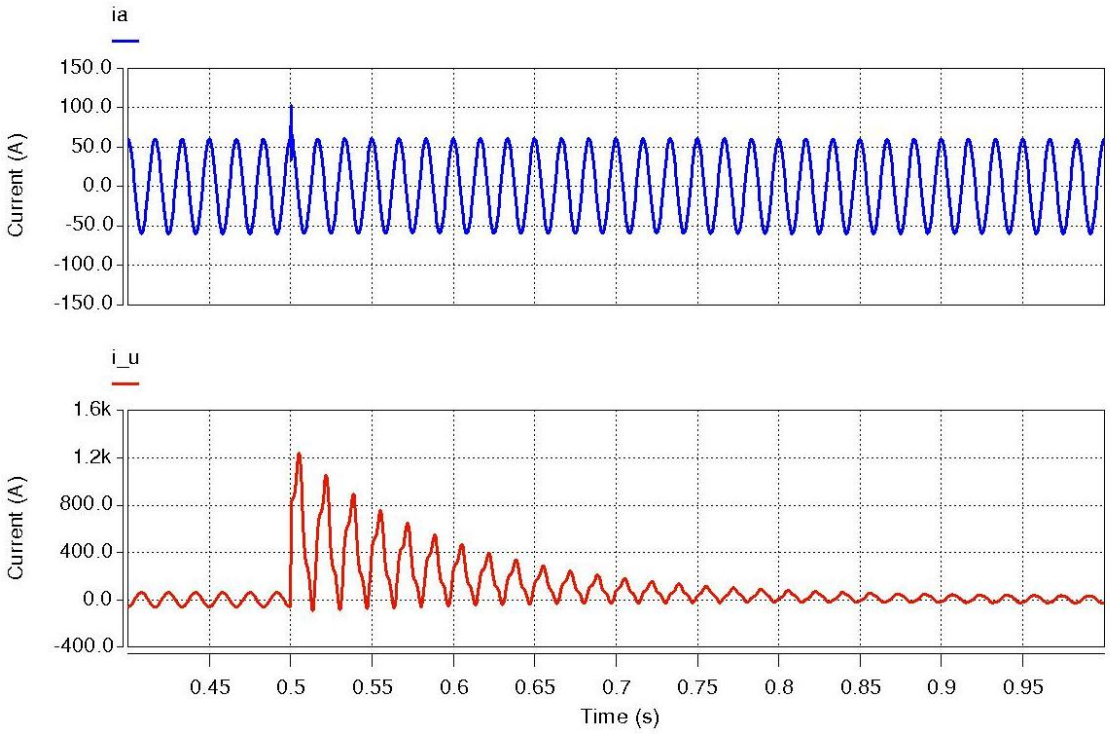


Figure 6-4: Converter response to transformer inrush

6.3. Voltage Sags and Swells

Voltage sags are among the most common utility disturbance and are contributed mostly to faults in the utility system. Depending on the depth and duration of the sag, loads may trip off-line as a result of the event. For the grid-tie converter, the voltage variation is of most concern since it causes a current transient on the output of the converter. If high enough, this current transient can lead to the overload or short circuit protection tripping within the converter. Therefore, it is crucial to the designer to remain operational during common utility disturbances. For voltage sags, only the depth of the initial transitions is important. After the initial change in voltage, the duration of the event has no influence on the converter output current. To illustrate the converter's response to a voltage sag, Figure 6-5 show the voltage at the PCC and converter output current during a volt sag to 0.05 pu. It is clear that because of the voltage change, the converter experiences an overshoot in the output current, which was also illustrated during the capacitor switching and inrush analysis. The current spike is dependent on the change in voltage. If the voltage change is large, the current spike will be large. The question is then how to prevent the converter from shutting down? A simple approach is to turn the converter off momentarily when it sees a voltage change greater than a certain percentage. For this converter design, when the voltage change is 0.05 pu the current spike is approximately 2 pu. If a 2 pu current spike is the limit for the protection, then the converter would need to turn-off momentarily during a detection of a 95% voltage change.

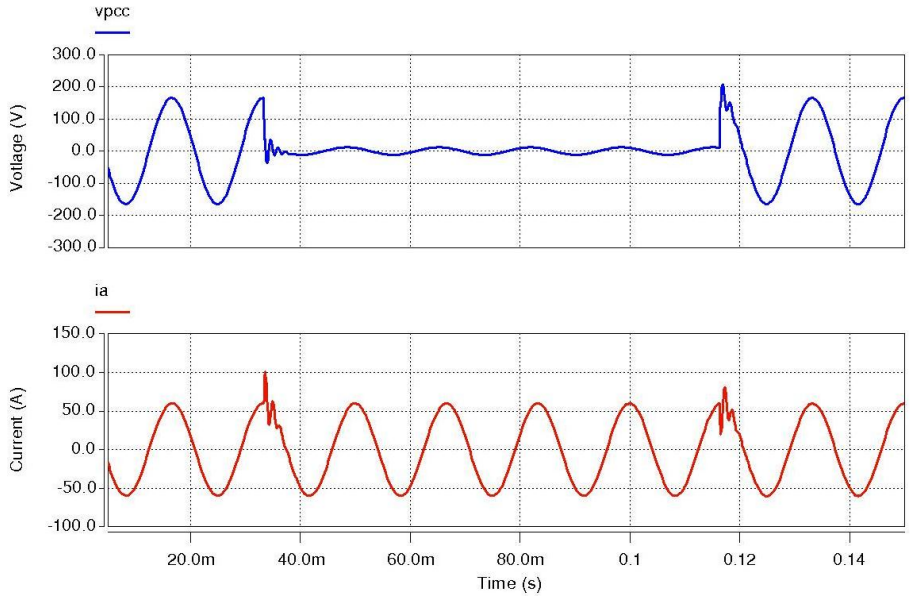


Figure 6-5: Voltage sag converter response before voltage change control

Since the voltage is mostly a reactive power issue, remaining on-line is not much benefit during the sag. If the utility allows for the converter to provide voltage support, then during the event the converter can inject vars to help support the grid; although this support is minimal in most cases. To illustrate this concept, Figure 6-7 shows the converter d and q-axis reference current during the event. The figure shows that as the converter detects an instantaneous voltage change greater than a set value the d-axis current turns off momentarily in order to avoid the initial current transient condition. How quickly the converter needs to shutdown depends on the filter. The transient is related to the LCL filter, so to avoid the event the system must operate quicker than the filter response.

In most cases, the filter's response can be approximated by simply looking at the natural resonant frequency of the LC portion of the filter. If the converter turns off quicker than this response, then the current overshoot should be minimized. For this particular scenario, the LC part of the filter is tuned to about 3 kHz, so the transition time was simulated based on a 100 µs delay, which for a 20 kHz switching frequency is 2 switching cycles. Two switching cycles is enough time to process the change in voltage and change the reference value. Figure 6-7 shows the voltage at the point of common coupling and the converter current during the event after applying the voltage monitoring. The q-axis is monitored for a cycle after turning off and then ramped over 1 ms to inject vars into the system. The converter does not necessarily have to wait for a cycle. Waiting for a cycle is solely for diagnostic purposes. In fact, as soon as the d-axis gets near zero, the q-axis current can start ramping.

For this case, the q-axis was ramped over 1 ms, which is 6% of one cycle, and produces only a very small transient in the voltage and current. During the event, the converter can raise the voltage caused by the sag by injecting vars into the system. However contrary to what some believe, the voltage change is minimal unless the converter is very large and the utility is also very weak. To give an example, if the utility transformer is the same size as the converter, the amount of voltage change is about 6 V assuming 5% impedance and an X/R ratio of 3.5 for the utility transformer. When the utility is 10 times the size of the converter with the same transformer characteristics, the voltage is about 0.6 V. Therefore, it is clear that if the utility is much larger than the converter the amount of change is going to be minimal. The idea of using a voltage source converter in parallel with the load to provide voltage ride through capability is not very practical since in most cases the utility will be at least the same size as the converter.

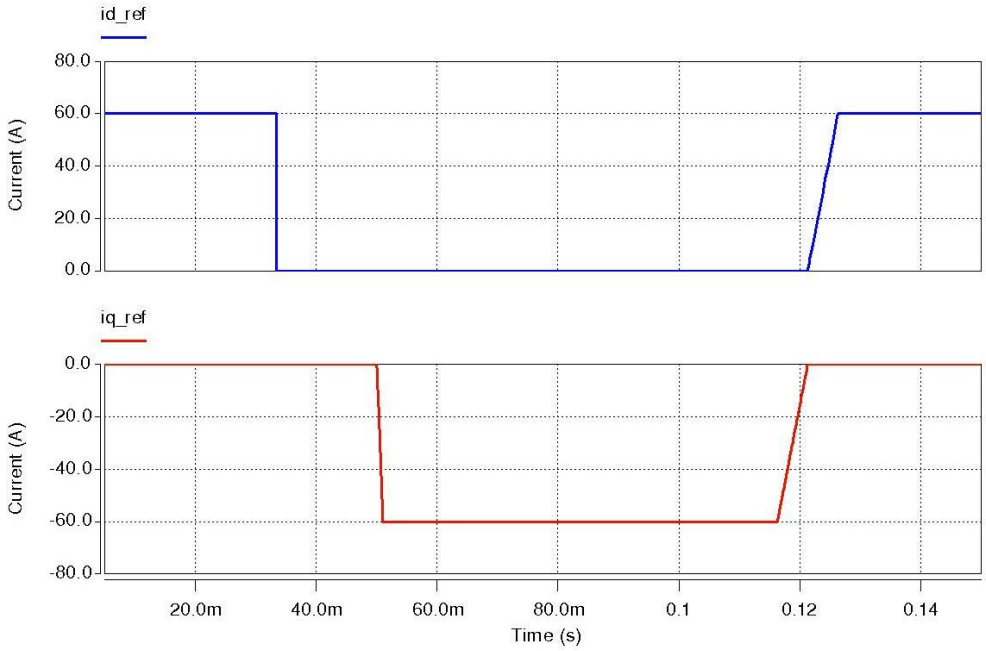


Figure 6-6: Reference current including voltage change compensation

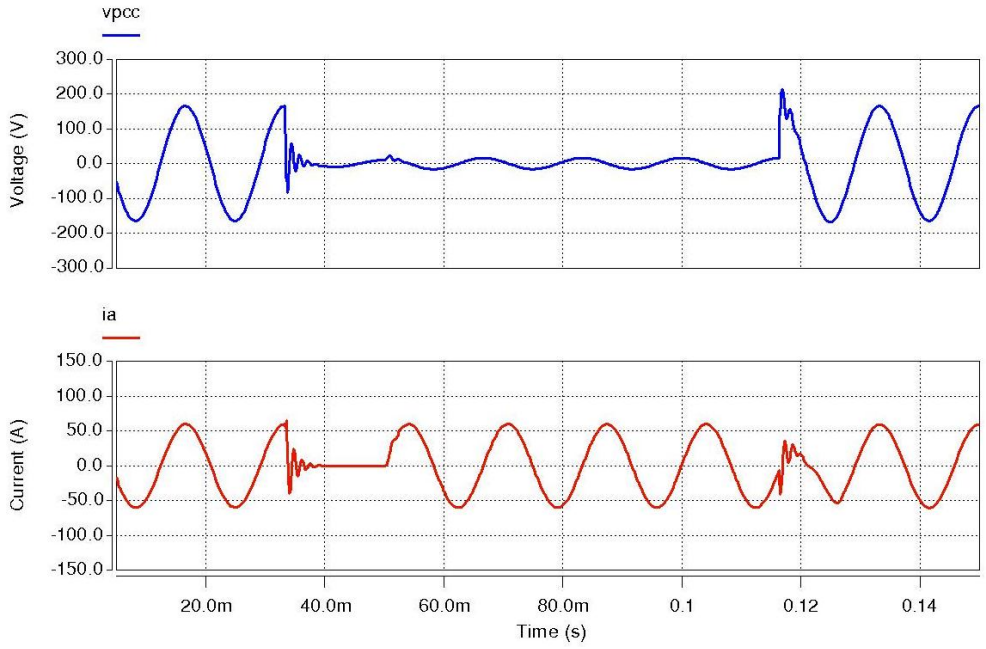


Figure 6-7: Voltage sag converter response after voltage change control

Voltage swells can be handled in the same way as sags, the only difference is that the converter would want to absorb vars instead of inject. The main difference between sags and swell is the operation window. For sags, the converter is not limited to disturbance magnitude, but for voltage swells when the utility voltage becomes greater than the DC bus voltage the anti-parallel diode are going to conduct regardless of switch state. Since the modulation index is often high for efficiency reasons, this leaves little head room for voltage swell events. On the positive side, voltage swells are rare in low impedance grounded utility systems. It should be noted that for capacitor switching and inrush transients, the same principles can be applied to mitigate the current spike.

Other than preventing the converter from turning off, this type of monitoring also helps to minimize transients seen on the passive components. In the capacitor switching discussion, the impact of the transient behavior on the damping resistor was shown to be fairly large. However, by turning off the d-axis current within a few switching cycles, the peak value of the transient is reduced by nearly 1/3. Figure 6-8 shows the damping current during a voltage sag to 0.05 pu. Notice that the peak current during the transient is now only 10 A compared to 30 A seen for the capacitor switching analysis.

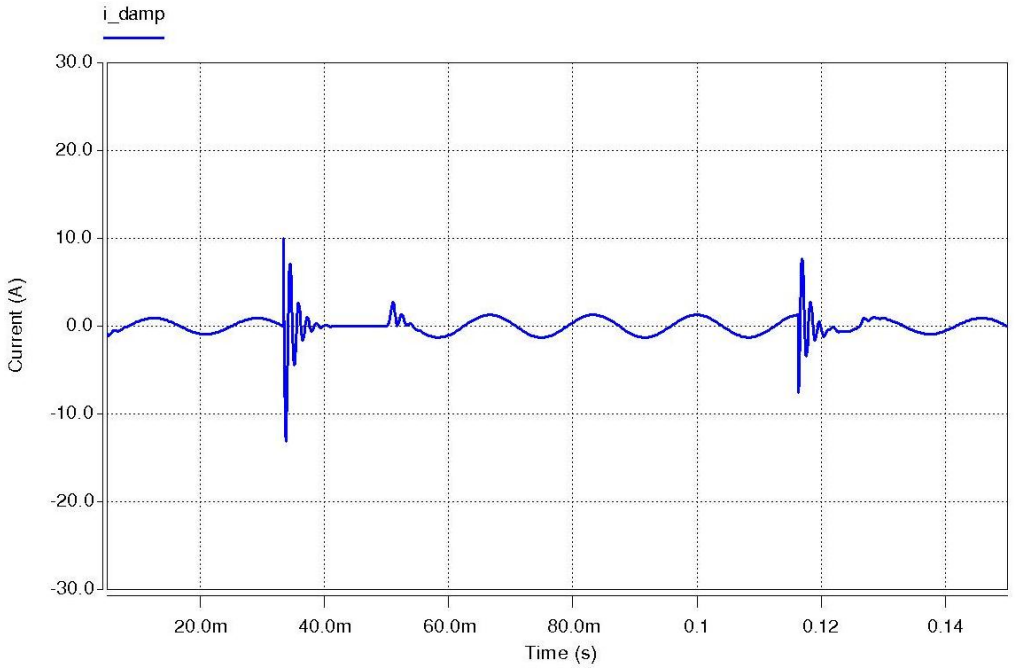


Figure 6-8: Damping resistor current after voltage change control

6.4. Summary

When there is a sudden change in voltage, the current output of the converter overshoots because of the filter response being higher than the bandwidth of the controller. In order to prevent the current spike, if the voltage change is monitored and the real current is turned off before the filter has time to respond, then the current spike is minimized. An example case illustrated that two switching cycles was sufficient time to mitigate most of the current transient. An alternative would be to place the filter cut-off frequency lower than the crossover frequency of the control. The downside to this approach is that the filter will become large. If no preventive action is taken for the voltage change conditions, the converter will likely overload and shutdown during large voltage changes. There is also a risk that the damping resistor in the filter could be damaged because of the transient event. The control system designed in the previous chapter has no problems with large inrush current events. A transformer inrush event was simulated to make sure the converter did not go unstable or overload because of the large energizing current.

In conclusion, as long as the control system is able to minimize the current spike during voltage changes, the converter showed no other issues with power quality events. However, it should be noted that not all of the power quality events were included in this analysis. Nevertheless, the author feels that the ones simulated are the most likely to be influenced by the control system. Generally, there is no reason to test the controls under events like lightning strike or EFT bursts since these events are much faster than the controls.

Chapter 7.Conclusion and Future Work

7.1. Conclusion

In chapter two, a few of the common methods for determining the real and reactive components of a current waveform were discussed with a focus on their implementation for single phase converters. Chapter 3 discussed a few different single phase PWM schemes and their use in single phase converter applications. For each scheme, a carrier and vector implementation were described. In chapter 4, the leakage current and conducted emissions were compared using the PWM techniques discussed in chapter 3. It was found that using a hybrid modulation schemes with a traditional bridge converter is only a problem when the cable between the converter and utility is long. The chapter also discussed how a few of the commercial transformerless converters use the PWM schemes developed in chapter 3 with additional circuitry to deal with leakage current issues. In addition to comparing existing topologies, two new converter topologies for grid connected converters were introduced. These topologies are based on a hybrid topology where one phase leg of the converter is a normal two level structure and the other is a multilevel structure. The multilevel output voltage helps to reduce the emissions and ripple compared to the two level structures.

On the controls side, the work focused on how both steady state and dynamic conditions affect the control system design. For steady state conditions, the small signal model was found by using an average dq model. From the small signal model, the influence of the PV source and utility were discussed and how they impact the closed loop response. Two different approaches for creating a fictitious dq transformation were compared under utility and PV disturbances. The work also illustrated how the bandwidth of the control system affects the compensation capabilities of the converter when used to provide harmonic compensation as described in chapter 2. The load and source impedance also heavily influence the control system, which was discussed in detail in chapter 5. On the dynamics side, when there is a sudden change in voltage, the current output of the converter overshoots because of the filter response being higher than the bandwidth of the controller. In order to prevent the current spike, if the voltage change is monitored and the real current is turned off before the filter has time to respond, then the current spike is minimized. An alternative would be to place the filter cut-off frequency lower than the crossover frequency of the control. The downside to this approach is that the filter becomes large. If no preventive action is taken for the voltage change conditions, the converter will likely overload and shutdown during the event.

7.2. Future Work

For PQ theory, the author feels that current work does not take advantage of the fact that the power contributed by the harmonics is low. By neglecting the power contributed by the harmonics, the real current and conductance can be found by using a simple perturb and observe approach, similar to what is being done for some MPPT tracking systems. In fact, the error that results from neglecting the power contributed by the harmonics is probably less than the error with the current approaches. The main advantage of this approach is that it would not limit the bandwidth of the control system. Since PQ theory was not the focus of this thesis, this was not researched in this work. However, in the future work it might beneficial to looking at using a perturb and observe type approach.

The two new hybrid converter topologies introduced in chapter 4 need further investigation. This work only addressed the emissions, filtering, and leakage current for these designs. The next step would be to look at a very thorough loss evaluation. This would need to go beyond the typical switching and conduction loss calculations, which could have easily been added in this work. The loss evaluation needs to consider the different types of semiconductors because of the different switching patterns. Since most of the switches are switching at line frequency, it makes sense to use something with very low conduction losses and that is inexpensive. Depending on the device, it may make the converter cost competitive with existing systems. Other than losses, the reduction in size and weight also need to be discussed. It was shown that the output filtering can be smaller with this type of converter because of the multilevel output structure, but a true comparison needs to be done in this area.

In chapter 4, a great deal of work was done trying to predict how a residual current device might respond during an oscillatory event caused by the hybrid PWM scheme. The author tried to correlate the event to the surge compliance standards, but this needs to be further investigated with laboratory measurements. Actually, there has been very little work published on leakage protection devices behavior to transients and high frequency noise. The majority of the work has been on designing filtering and converters to minimize the leakage current without regard for devices response to the conditions.

In terms of control, the system was designed to work over a large range of load and source conditions and showed satisfactory performance. The steady state conditions such as utility harmonics and DC variations are not a problem for the control system. The response of the control system to power quality events needs further work. One technique was proposed in this work but there may be better approaches.

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Vita

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