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The Characterization of a CMOS Radiation Hardened-by-Design Circuit Technique

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I am submitting herewith a thesis written by Austin James Womac entitled "The Characterization of a CMOS Radiation Hardened-by-Design Circuit Technique." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

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THE CHARACTERIZATION OF A CMOS RADIATION HARDENED-BY-DESIGN CIRCUIT TECHNIQUE

A Thesis Presented for the

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Austin James Womac

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I dedicate this thesis to my parents,
Alvin and Eleanore Womac, and my friends
for their unwavering support and love.

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ABSTRACT

This thesis presents the analysis, implementation and testing of a circuit-level radiation hardened-by-design (RHBD) technique first presented in [1]. Radiation effects heavily influence the cost and design of electronics bound for radiation-rich environments such as in nuclear reactors or space. The circuit-level RHBD technique is presented as a cost-effective way to mitigate total-ionizing dose (TID) radiation in digital complementary metal-oxide-semiconductor (CMOS) transistor circuits. These claims are analyzed and experimentally tested.

Devices from a relatively old and a newer semiconductor fabrication process are tested to investigate the impact of device scaling on the effectiveness of the RHBD technique. A rad-tolerant frequency synthesizer that implements this technique is discussed. Challenges in the project included implementing efficient testing procedures at the radiation test facilities. Testing time was limited and *in-situ* test methodologies utilizing LabVIEW programs were used effectively.

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CHAPTER 1: INTRODUCTION

1.1 Motivation

Electronic devices now pervade our society. From our smartphones to control and entertainment systems in our cars, to industrial process control systems, electronic devices perform vital functions in a multitude of applications that we may or may not realize. Their prevalence is in part due to their continuously increasing performance and decreasing cost. They have been increasingly called upon to perform in new, niche applications. Many of these applications include radiation-rich environments such as space, nuclear reactors and military applications.

Radiation can damage electronics causing performance degradation or malfunctions. NASA, along with Jet Propulsion Laboratory (JPL), launched the Mars Science Laboratory (MSL) mission in 2011 to determine whether the Martian environment was ever habitable for life [2]. This mission included a small car-sized, autonomous rover dubbed *Curiosity* with a full suite of science sensors and instrumentation. In February of 2013, after roaming the Martian surface for seven months, *Curiosity* experienced failure of its primary onboard computer [3]. The problem was traced to the computer's memory bank. The cause of the problem is believed to be a recent solar storm; charged particles from the storm may have reached *Curiosity's* primary memory bank and corrupted some of the digital data bits [4]. This example illustrates the worst-case effect radiation can have on an electronic device: complete device failure.

MSL represents a 2.5 billion dollar investment by the American public. For the entire program to be halted by a relatively common solar storm would have been a catastrophic blow to the space program. Fortunately, a redundant computer system was able to take over when the failure occurred. Normal operation of *Curiosity* was resumed thanks to radiation mitigation techniques in use aboard the rover.

Radiation mitigation techniques are more commonly called radiation-hardening techniques or simply rad-hard techniques. The rad-hard technique that saved *Curiosity* is a system-level technique. These techniques usually involve system redundancy,

majority-voting circuits and digital parity checking. They are suited for mitigating single-event effects (SEE). SEE include both single event upsets (SEU) and single event transients (SET) [5]. SEU occur when charged particles, such as high-energy photons or protons, change the state of a storage element such as a flip-flop, latch or memory bit [6]. A SET is a temporary voltage glitch in combinational logic caused by excessive charge deposited on a node from a large ion or proton [5]. By incorporating system-level mitigation techniques, SEE logic upsets can be detected and corrected.

Total-ionizing-dose (TID) effects are also important to consider when hardening electronic devices. SEE logic upsets are due to single ion strikes on vulnerable electrical nodes; TID quantifies the total radiative energy imparted to an electronic device. It is useful for understanding the degradation of device performance in the presence of radiation. These degradations are especially important in complementary metal-oxide-semiconductor (CMOS) transistors. Devices fabricated in older CMOS processes exhibit large changes in transistor threshold voltage. Newer CMOS processes tend to suffer more from subthreshold current leakage [7]. System-level rad-hard techniques are not suited for mitigating these degradations.

One form of radiation hardening for TID is termed hardened-by-process (HBP). HBP requires special "rad-hard" foundries to manufacture inherently rad-hard electronics. In his paper "Improving integrated circuit performance through the application of hardness-by-design methodology" [6], Lacoe describes these special foundries as boutique, expensive foundries lagging the latest commercial foundries by around three CMOS generations (about eight years). This gap is primarily due to the small demand for rad-hard electronics. It is desirable to avoid these foundries and harden higher performing, less expensive commercial processes directly [6].

Hardened-by-design (HBD) techniques provide superior cost-to-performance ratio than hardened-by-process techniques. These techniques involve combining the intrinsic radiation hardness of current generation CMOS processes and special design techniques to create rad-hard electronics [6]. These special design techniques can include layout-level techniques and circuit-level techniques. Many of the layout techniques involve novel transistor designs, such as annular-gate transistors or enclosed-source transistors.

These novel transistor designs are extremely tolerant of TID; however, they incur layout area, speed and power penalties. They are also much more difficult to model than standard transistors [8]. These drawbacks motivate the investigation of HBD techniques that do not use novel transistor-layout designs.

Dong Pan *et al.* have proposed a novel HBD circuit-level technique [1]. This technique uses process-standard transistors in a novel circuit configuration dubbed the "inverted-source" configuration. They show simulation data indicating that the technique is effective at mitigating threshold voltage variation under TID. However, no experimental data is provided to quantify this. In addition, this paper was published in 2003 when state-of-the-art CMOS devices were more susceptible to threshold voltage variation. There is no data indicating whether this novel technique is capable of mitigating subthreshold current leakage dominant in today's CMOS devices exposed to TID radiation. These shortcomings motivate this thesis.

1.2 Thesis Scope and Organization

Radiation effects and hardening techniques to mitigate them constitute a very wide field-of-study. It is necessary to narrow the scope of this work. The primary focus of this thesis is the testing methodology used to determine the effectiveness of the inverted-source TID radiation hardening technique. This includes choosing the processes for testing, designing the circuits in these processes that characterize the performance of the technique and the radiation test setup used at the testing facilities. The goals of this thesis are to experimentally characterize the TID immunity and assess the layout area, speed and power penalty of this novel HBD circuit-level technique in both an old and new CMOS process.

Chapter 2 provides background information on TID radiation effects in MOSFET devices and the common layout HBD techniques used to mitigate them. Chapter 3 analyzes the viability of the inverted-source HBD technique, describes the HBD circuits designed and discusses the tests and test setup. Chapter 4 presents and analyzes the results of the radiation testing. Chapter 5 concludes the thesis and presents some of the possible future directions of this research.

CHAPTER 2: BACKGROUND

2.1 TID Radiation and the Space Environment

Radiation-rich environments include space, nuclear reactors, nuclear material processing, nuclear weapons, and controlled fusion [9]. The space environment contains a broad range of energetic particles that can have various deleterious effects on microelectronics including TID effects, SEE, and displacement of atoms. A discussion of the radiation in space encompasses many of the types of radiation harmful to microelectronics that are seen in other radiation-rich environments. Therefore, for the purposes of covering TID radiation and its effect on MOSFETs, it is suitable to provide a brief discussion of radiation in the space environment.

The largest sources of TID-inducing radiation around the Earth are the van Allen belts. These belts consist of electrons and protons trapped in the Earth's magnetosphere [8]. Figure 1 shows the magnetic field lines of the Earth that contain the trapped particles. The trapped particle flux depends on the distance from the Earth and the latitude. Electrons tend to be found further from the earth and can have energies up to 7 MeV, while heavier protons are found closer and can have energies of several hundred MeV [9]. The typical altitudes of many space satellites are within the van Allen belts making it important that microelectronics aboard are tolerant of TID radiation.

Flux lines emanating from the sun shown in Figure 1 depict a continuous solar wind from the sun. Solar wind is plasma consisting of 96% protons and 4% hydrogen, heavy ions and electrons [8]. The Earth's magnetic field deflects most of this solar wind and creates a wake zone behind the Earth. However, if particles have energy higher than a certain threshold, dubbed the geomagnetic cutoff, they may penetrate the Earth's magnetic field [9]. Another source of radiation includes galactic cosmic rays (GCRs). GCRs originate outside of the solar system and primarily consist of heavy bursts of protons [9]. Solar flares are moments of intense activity on the sun. They eject large bursts of electromagnetic radiation ranging from gamma rays to radio waves along with heavy ions, protons and electrons [8]. Solar flares also interact with the Earth's magnetic field and may temporarily reduce the geomagnetic cutoff allowing increased radiation

exposure [9]. While the bulk of TID effects are primarily attributed to the van Allen belts, these other sources of radiation in space contribute to TID as well.

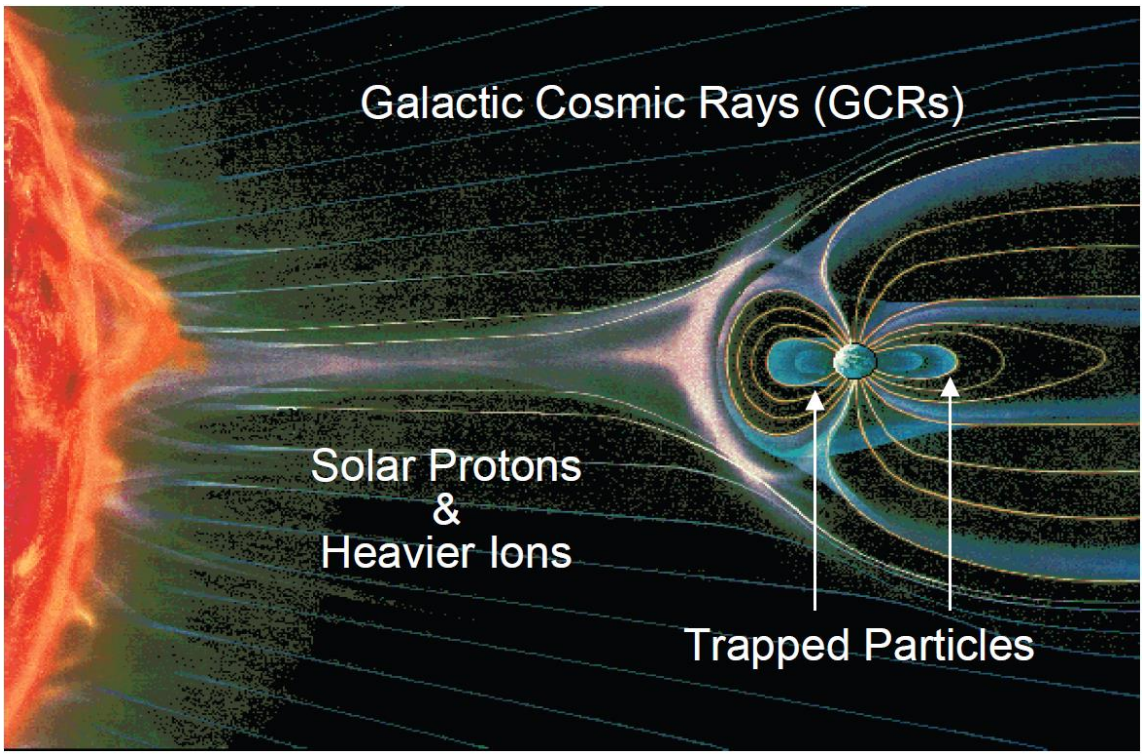

Figure 1 - The major sources of radiation to Earth [8].

2.2 Interaction of Radiation with Solids

When energetic particles such as protons, electrons or heavy ions impact a solid, they deposit energy in the solid. The rad is the most common measure of the total energy deposited in a material. A rad is absorbed when 100 ergs per gram is deposited where an erg is 100 nJ. The gray is the SI unit of total energy deposited. A gray is defined as 1 joule per kilogram. There are therefore 100 rads in one gray. More commonly, the rad is simply equated with one centigray (cGy). Because the rad is still the most common unit in use, it is used in this thesis. The amount of energy deposited by an energetic particle depends on the energy and size of the impinging particle and the material under irradiation [10]. When performing radiation testing, it is very important to note for what material the dose rate is measured. All dose rates and total dosages in this thesis are for silicon dioxide. The energy is lost at nearly a constant rate per distance traveled in the solid. When normalized by the density of the solid, the energy loss rate is defined as the linear energy transfer (LET). The units of LET are usually given in $\frac{MeV}{cm} \div \frac{g}{cm^3} = \frac{MeV-cm^2}{g}$ [8].

The process of energy transfer from an impinging particle and a solid is a complicated process; the next few paragraphs introduce the subject. The primary loss of energy for a charged particle such as a proton or electron occurs through Coulomb scattering where the charged particle ejects an outer shell electron from an atom in the solid [8]. This is the creation of an electron-hole pair (ehp). Charged particles with enough energy to create electron-hole pairs (ehps) are called ionizing radiation. A single charged particle may create many ehps along its trajectory. Charged particles may also directly displace atoms if they collide with them. However, it is much more probable that a charged particle will lose its energy through Coulomb scattering [11].

According to F. McLean and T. Oldham [11], uncharged particles, such as neutrons, primarily lose their energy in solids by colliding with an atom. A struck atom may recoil from its original lattice site and come to rest at an interstitial site damaging the material. This is termed displacement damage. The struck atom, which has a positive

charge, may also impart its energy to additional atoms causing further displacement damage or create ehps [11]. Thus, neutrons can be indirectly ionizing.

X-rays and gamma rays may also ionize semiconductor solids primarily through Compton scattering [8]. Compton scattering occurs when a photon collides with an atom and an electron is energized. It is then capable of creating more ehps through the Coulomb scattering process. Cobalt-60 is commonly used to produce ionizing gamma rays in test chambers. It produces gamma rays with an average energy of 1.25 MeV [9]. The LET in SiO_2 of gamma rays is shown along with that of protons and electrons in Figure 2. The LET is plotted versus the energy of the particles. The gamma ray's LET is equivocated to an electron of about 300 keV. As a general explanation of the plot's trends, the more energy a charge particle has, the faster it is traveling and the less probability it has of interacting with the solid; therefore, the LET drops as the particle's energy increases. The graph also indicates the number of ehps created per cm as horizontal dashed lines.

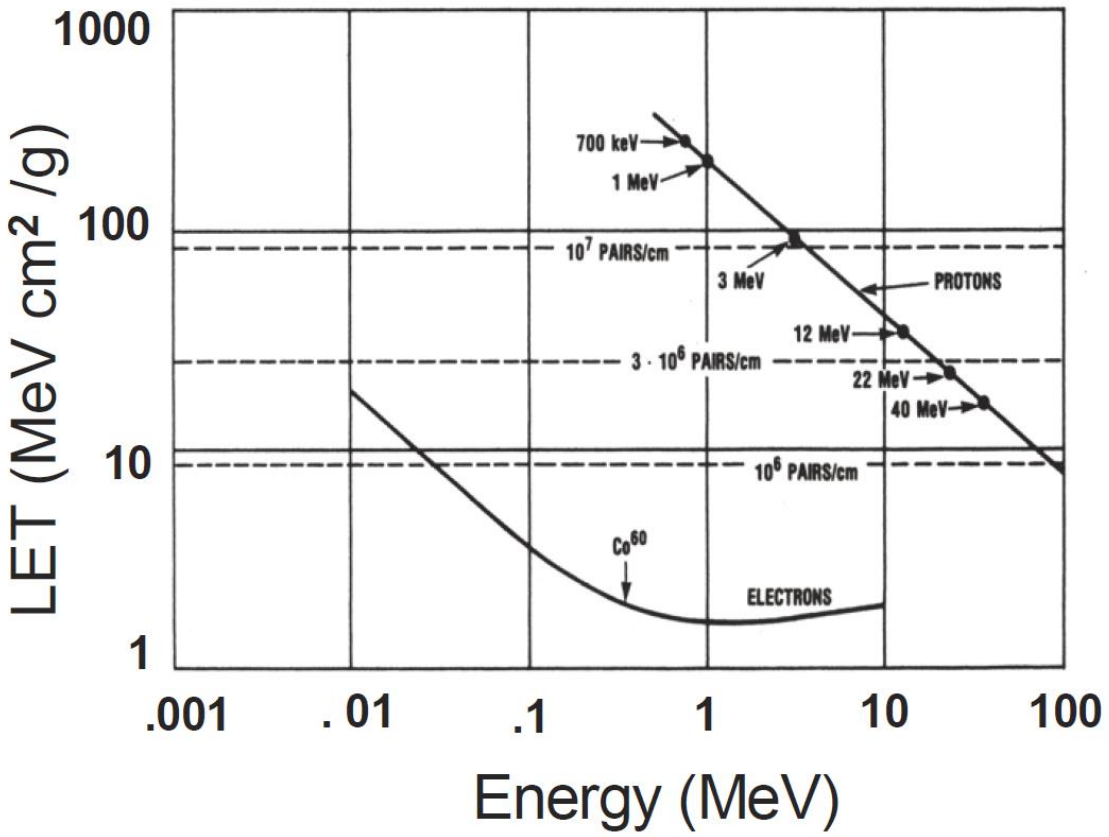

Figure 2 - The LET of protons and electrons in SiO_2 versus the particle's energy. "The effective LET of Co-60 is indicated in terms of an equivalent energetic electron" [8].

2.3 TID in MOSFET Devices

Radiation that strikes silicon may ionize it, creating ehps. However, the mobility of electrons and holes in silicon is 1350 cm^2/V-s and 480 cm^2/V-s respectively [12]. The ehps created from radiation recombine quickly. Silicon is still susceptible to displacement damage and SEEs. The most important electrical effect of displacement damage in MOSFETs is mobility degradation.

A far more potent form of TID damage in MOSFETs is charge trapping in SiO_2. Figure 3 illustrates the process of positive charge trapping in a band diagram of an example MOSFET gate dielectric. If an electric field is placed across the SiO_2, electrons and holes of ehps are pulled in opposite directions by the field. The mobility of electrons in SiO_2 is approximately 20 cm^2/V-s [13]. This level of mobility allows the electrons to be swept out of the oxide. This limits the time available for electrons and holes to recombine [8]. As an aside, this illustrates the importance of device biasing during radiation testing. Usually, a maximum V_{GS} voltage is used during irradiation [14]. This ensures a worst-case test condition, because the electrons and holes are strongly pulled in opposite directions limiting recombinations.

The holes in SiO_2 have a much lower mobility than electrons, in the range of 10^{-4} to 10^{-11} cm^2/V-s [15]. Therefore, the holes tend to become trapped at various energy levels and distances to the SiO_2/Si interface. Some are trapped deeply, greater than three electron volts away from the valence band, and others are less than one electron volt. The deep traps tend to remain immobile under normal operating conditions and may only be removed by annealing over a long period. The shallow-trapped holes tend to be more mobile and move toward the SiO_2/Si interface through polaron hopping transport ([8] and [10]).

The closer the holes are to the SiO_2/Si interface, the more easily they may induce an electron to tunnel into the oxide to recombine with it [10]. Holes within approximately five nanometers of the interface strongly interact with electrons in Si. They are called border traps. There are also traps (holes) located directly on the SiO_2/Si interface called interface traps. They are thought to be a byproduct of dangling bonds at this location (P_b) [10]. Because of their close proximity to the electrons in the Si, they

interact strongly with them and can have significant effect on MOSFET performance [10].

2.4 TID-Induced Performance Degradations in MOSFETs

SiO_2 is used as an insulating layer in integrated circuit (IC) fabrication. In bulk CMOS processes, it is used as the gate dielectric of a MOSFET (Figure 3) and as isolation between devices either LOCal Oxidation of Silicon (LOCOS) or Shallow Trench Oxide (STI). Figure 4 shows a cross-sectional view of a typical NFET using STI with the TID-vulnerable oxides highlighted.

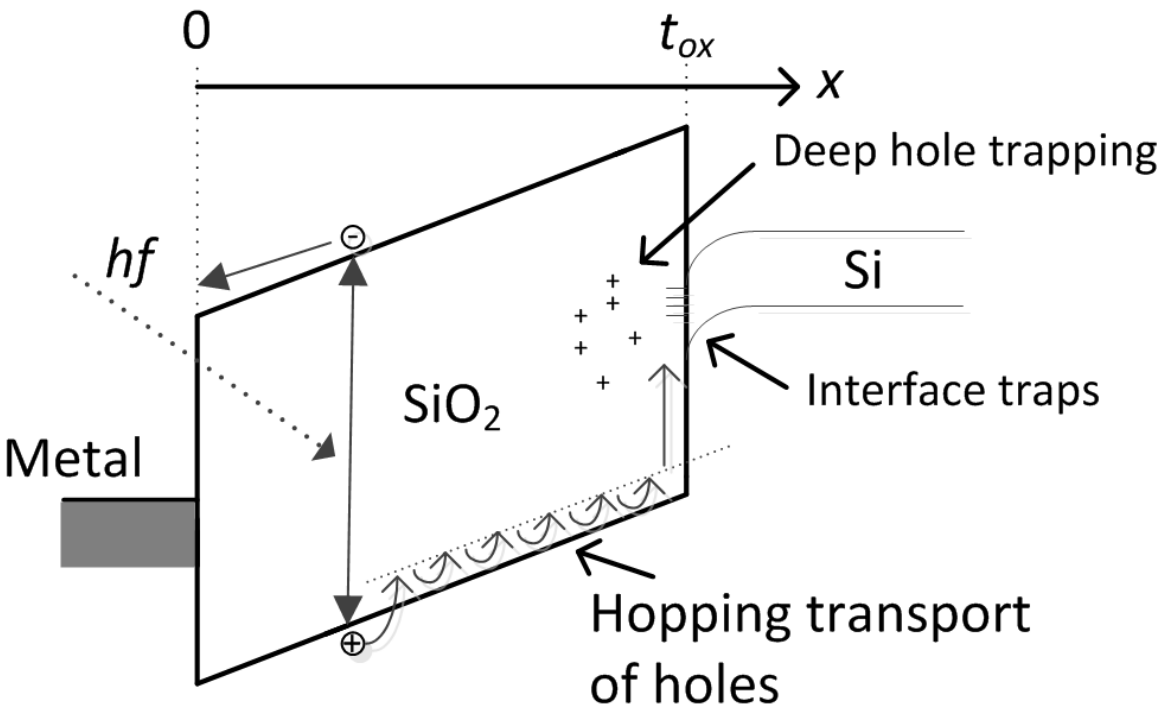

Figure 3 – Band diagram illustrating the trapping mechanisms in gate oxide with a positively biased gate node.

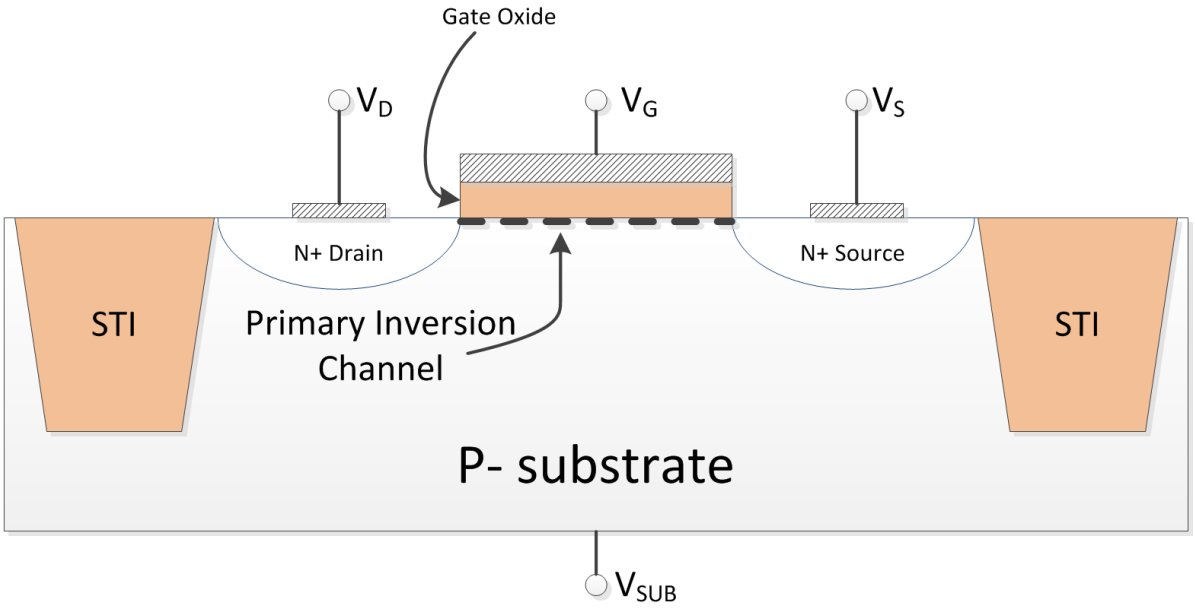

Figure 4 - Cross-sectional view of NFET in the channel length direction.

2.4.1 Thick-Gate Oxide Devices

MOSFETs that support a large V_{GS} voltage must have a gate oxide thick enough to prevent electric field breakdown. For older CMOS processes and high-voltage devices in newer processes, the gate oxide may be thicker than five nanometers to support the large V_{GS} voltages. There are regions in the gate oxides that may trap positive charges that do not have a high probability of tunneling out of the oxide because they are too far from the interface. The most significant effect of ionizing radiation in these "thick-gate oxide" MOSFETs is threshold voltage variation. As shown in Figure 5, the positive trapped charges decrease the threshold voltage of NFETs while increasing the threshold voltage of PMOS transistors by an amount of $-\Delta V_{ot}$. This may be calculated by,

$$\Delta V_{th} = -\Delta V_{ot} = \int_0^{t_{ox}} \frac{-t_{ox} q}{k_{ox} \varepsilon_0} \times N_{ot}(x) \times \left(\frac{x}{x + t_{ox}}\right) dx \quad (1)$$

where k_{ox} is the dielectric constant of the oxide, ε_0 is the permittivity of free space, x is the distance within the oxide, and $N_{ot}(x)$ is the trapped charge concentration at a certain depth, x. The most important failure mode of the MOSFETs in this case is the NMOS's transition from an enhancement-mode device to a depletion-mode device [12]. In other words, the NFET is not turned off when $V_{GS} = 0$ V. The effects on the PMOS transistor are not as dire. It becomes harder to turn on the PMOS, but not substantially if it can still reach saturation. For 5-V CMOS devices with a 1 V threshold voltage, the NFET will fail as a switch when $\Delta V_{ot} = 1$ V, but the PMOS will not fail until $\Delta V_{ot} = 4$ V, long after the NMOS has failed.

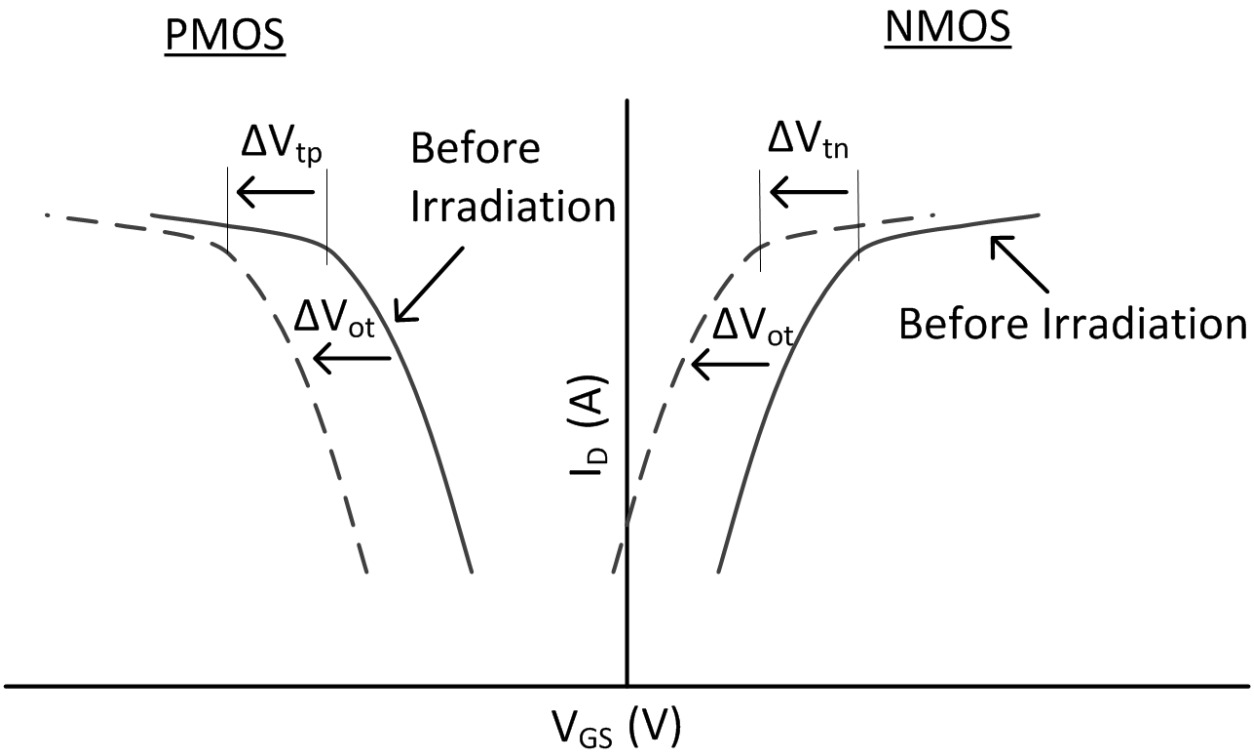

Figure 5 - Threshold voltage variation in PMOS and NMOS thick-gate oxide transistors via trapped charge.

There are many additional TID effects in thick-gate MOSFETs that do not contribute to device failure in digital CMOS applications. These secondary effects are primarily caused by the interface traps on the SiO_2/Si interface. These traps cause increased sub-threshold swing, decreased carrier mobility and increased 1/f noise above 1 kHz [8], [10]. Device annealing increases interface states, so these phenomena actually degrade further after annealing [8]. The 1/f noise above 1 kHz is increased because of interface traps, but 1/f noise below 100 Hz is increased as well but from border traps instead of interface traps [10]. Qualitatively, the border traps are further within the oxide and have a lower frequency of interacting with electrons than interface traps do.

2.4.2 Thin-Gate Oxide Devices

As process scaling has continued, the gate oxide thickness of MOSFETs has continued to decrease. From the equation above, the following relationship can be derived:

$$\Delta V_{th} \propto {t_{ox}}^2 \tag{2}$$

because N_{ot} is proportional to the gate oxide thickness, t_{ox}. As the gate oxide thickness shrinks below 5 nm, which is the characteristic tunneling length for holes within SiO_2, the threshold voltage shift in MOSFET devices, ΔV_{th}, becomes negligible (less than 5 mV at a 30 Mrad dose) [6]. MOSFETs with a gate oxide thickness of less than eight nanometers are dubbed "thin-gate oxide" devices. These devices are usually found in advanced submicron processes with a gate feature length of 0.35 μm or less. Under TID, subthreshold leakage current is the dominant performance degradation in these processes.

Figure 4 shows the STI on either side of the drain and source of the NFET. The STI, in fact, surrounds the entire transistor [16]. Figure 6 shows a cross-sectional view of the same transistor however rotated by 90°, so the current flow direction is perpendicular to the page. The cross-section is cut between the source and the drain. The STI oxide is much thicker than the gate oxide and can trap positive charges under TID. These trapped charges can invert the active area abutting the STI and create a parasitic sidewall transistor that causes leakage current to flow from source to drain [7].

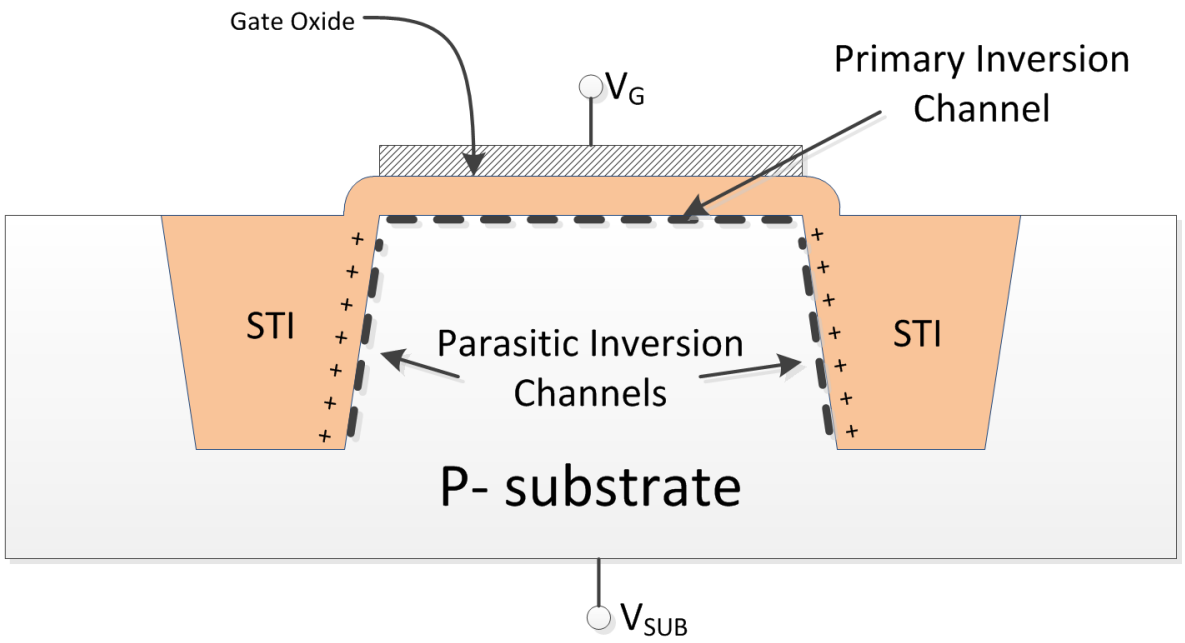

Figure 6 - Cross-sectional view of NFET in the channel-width direction.

The leakage current is a function of vertical location along the STI edge [16], [17]. As shown in Figure 7, the leakage current becomes worse further down in the STI. This is believed to be due to the positive gate bias during irradiation; the positive voltage repels the trapped holes pushing them further into the STI [17]. Because of the increased distance between the gate and the trapped charges, it is more difficult to control the transistor via the gate. Figure 8 shows a dramatic increase in sub-threshold current leakage for an NFET fabricated in a 0.18 μm process for increasing TID. Also, note there is no visible shift in the threshold voltage, because of the thin-gate oxide.

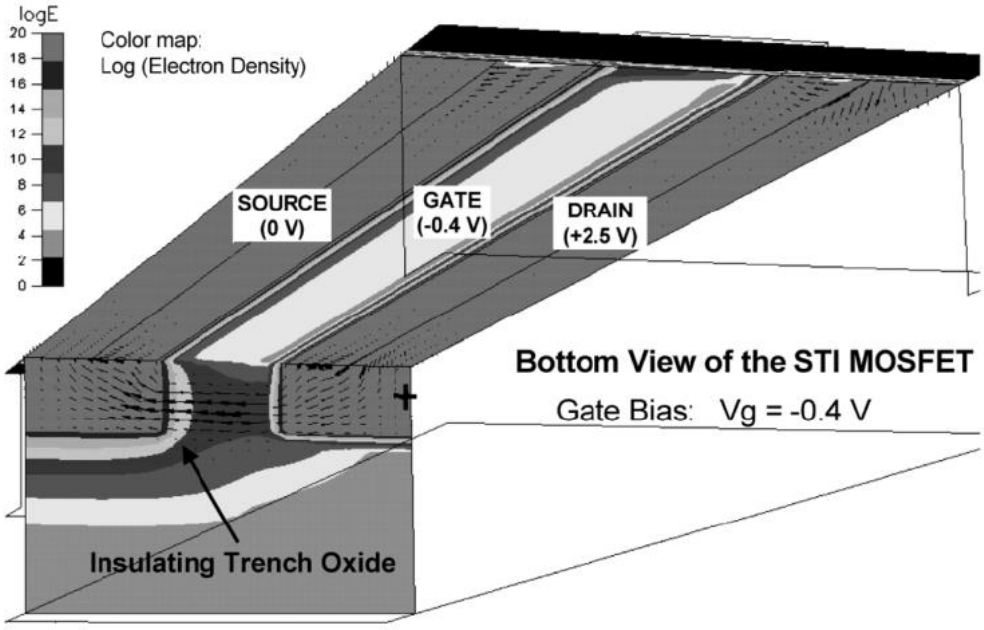

Figure 7 - 3D cross-section of 0.4 µm NMOS FET. Current density is calculated when a sheet charge is placed on the STI/Si interface. Results show leakage current density depends on depth in the channel with more current flowing deeper within the channel [17].

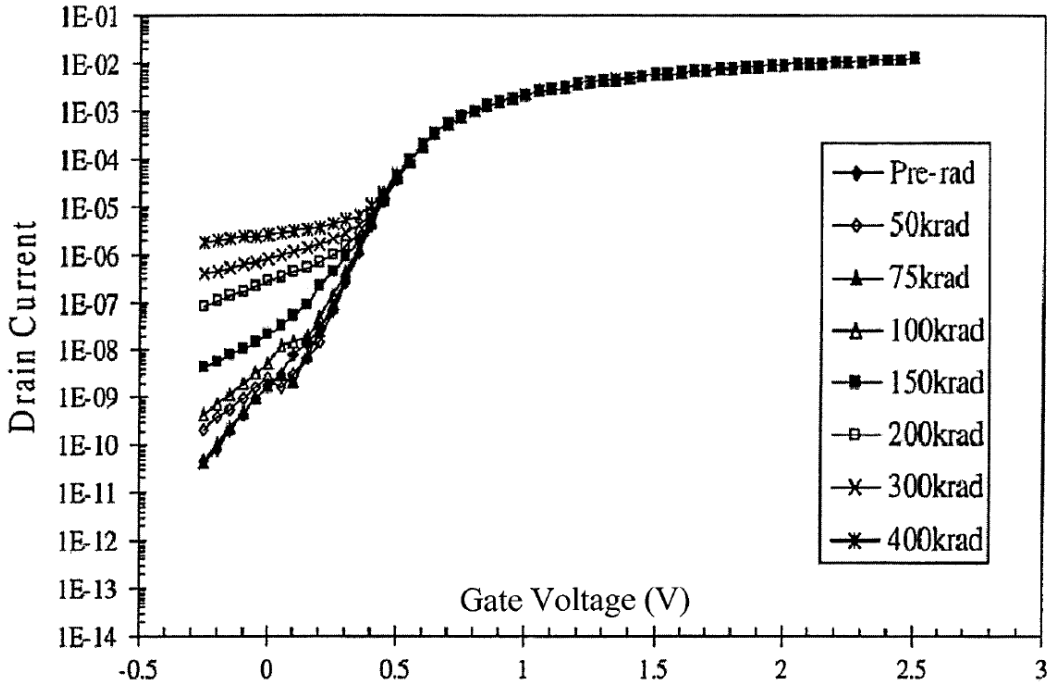

Figure 8 - Measured V_{GS} vs. I_D curve of an NFET fabricated in a 0.18 µm CMOS process for various TID [17].

Thin-gate oxide transistors isolated by STI exhibit another TID effect in addition to deep STI channel leakage. During initial TID exposure (up to 20 krad as described in [16]), the charges in the STI are located higher, near the STI corner. This means that the gate is able to exert some control over the parasitic sidewall transistors. This effect, dubbed the subthreshold hump effect, is shown in the contrasting pre-rad and 20 krad curves of Figure 9. However, as TID increases this effect is washed out by deep leakage within the STI.

It has been shown that the subthreshold hump effect is highly dependent on the MOSFETs structure. Hu *et al.* characterized a high-voltage (HV), an I/O, and a core NFET in a 0.18 μm process for various TID [18]. The HV NMOS shows the worst hump effect followed by the I/O NMOS, which is finally followed by the core NFET. The authors postulate that the oxide thickness at the STI corners plays an important role in this result. Figure 10 shows a cross-sectional diagram of the STI corner of the three different NMOS devices. The authors state that the thicker corner of the HV device allows more charge to be trapped, thereby pronouncing the subthreshold hump effect. The subthreshold hump, as shown in Figure 9, almost appears to be a shift in the threshold voltage of the device. As will be discussed later, high-voltage devices with thick STI corners could be an ideal candidate for the proposed HBD technique.

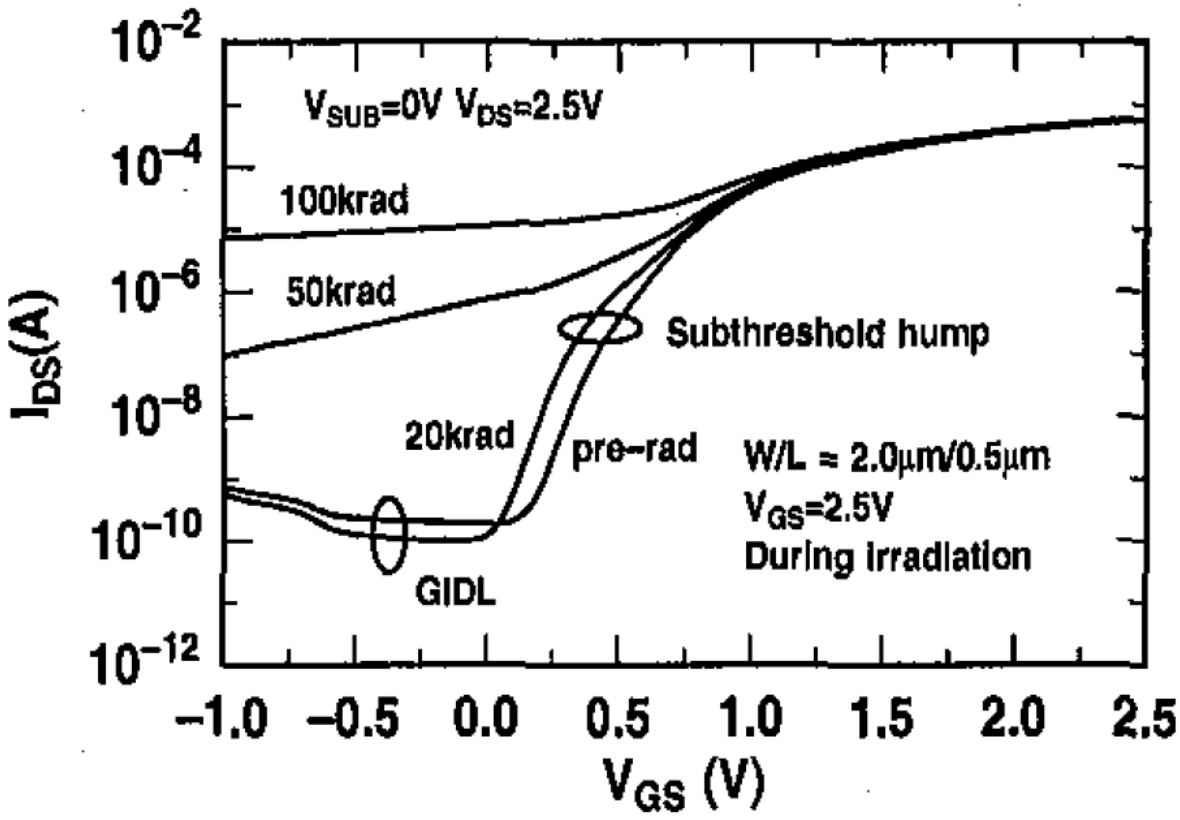

Figure 9 - Measured I_D vs. V_{GS} of NMOS in 0.35 μm BiCMOS process [16].

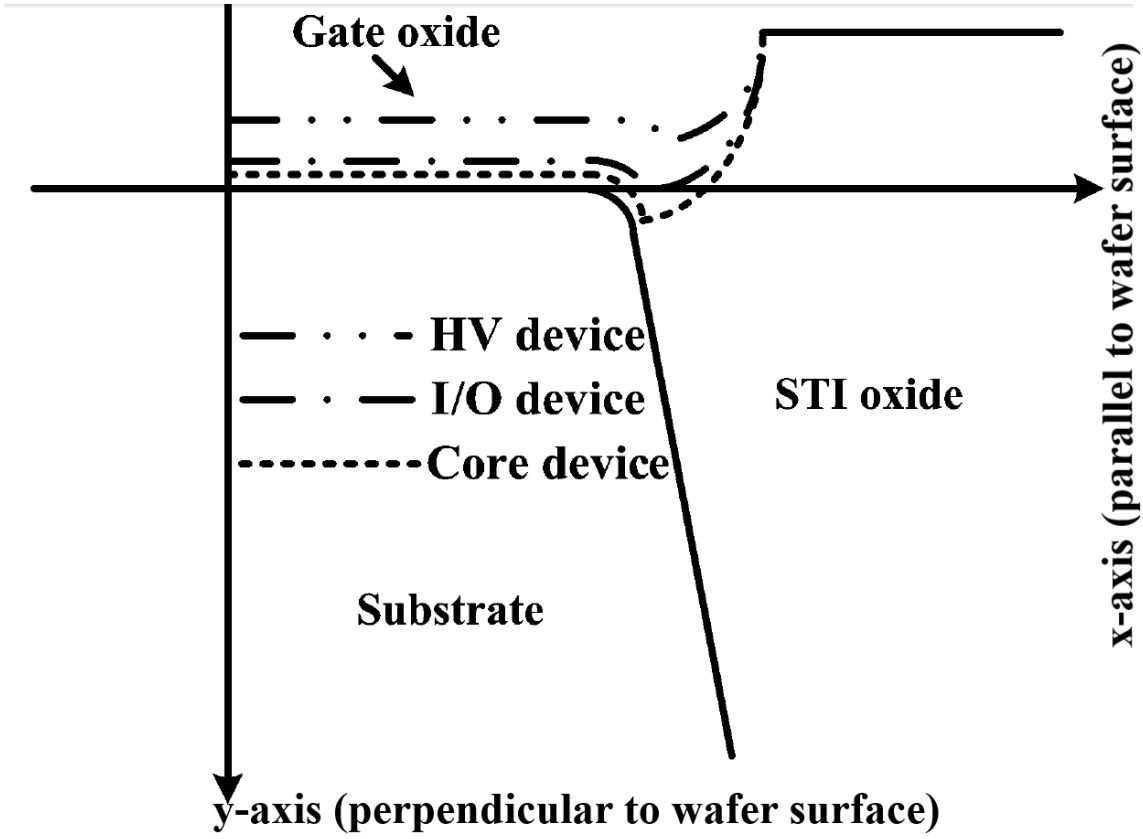

Figure 10 - Diagram of STI corner for three NMOS devices in a 0.18 µm CMOS process [18].

The subthreshold leakage current described previously is termed intra-device leakage. *Inter*-device leakage (leakage between neighboring devices) relies on charges trapped along the bottom of the STI. These trapped positive charges may invert n-type Si directly underneath them to form a leakage path between devices. However, recall that the electric field (i.e. proportional to the gate voltage placed across the gate oxide) plays a large role in the susceptibility of charge trapping in the oxide. As the electric field increases, the number of ehp recombinations decreases, because the electrons and holes are pulled in opposite directions. There is a very low electric field at the bottom of the STI; therefore, charge trapping (and inter-device leakage) has been shown to be not as important as intra-device leakage [18].

2.5 The Traditional, Straight-Gate Inverter's Shortcomings under TID

As discussed previously, TID has various deleterious effects on MOSFETs, especially NFETs. The most important of these effects limits the ability of the NFET to turn off. If the inverter has been exposed to a large amount of TID, when V_i is a logic 'low' or zero volts there will still be leakage current through NFET, N1, even though N1's V_{GS} is zero. This increases the static power dissipation of digital circuits.

In addition, further increasing TID may cause the logic gate to fail entirely. Figure 11 shows the standard CMOS inverter and its transfer function under TID. The output, V_o, should be a logic 'high' or nearly V_{DD} when the input is a logic 'low'. However as TID increases, the off-state resistance of the NFET decreases either through negative threshold voltage shift in thick-gate oxide NFETs or STI sidewall leakage in thin-gate oxide NFETs. Eventually, the output voltage will fall to a digitally indeterminate value and the digital circuit will fail.

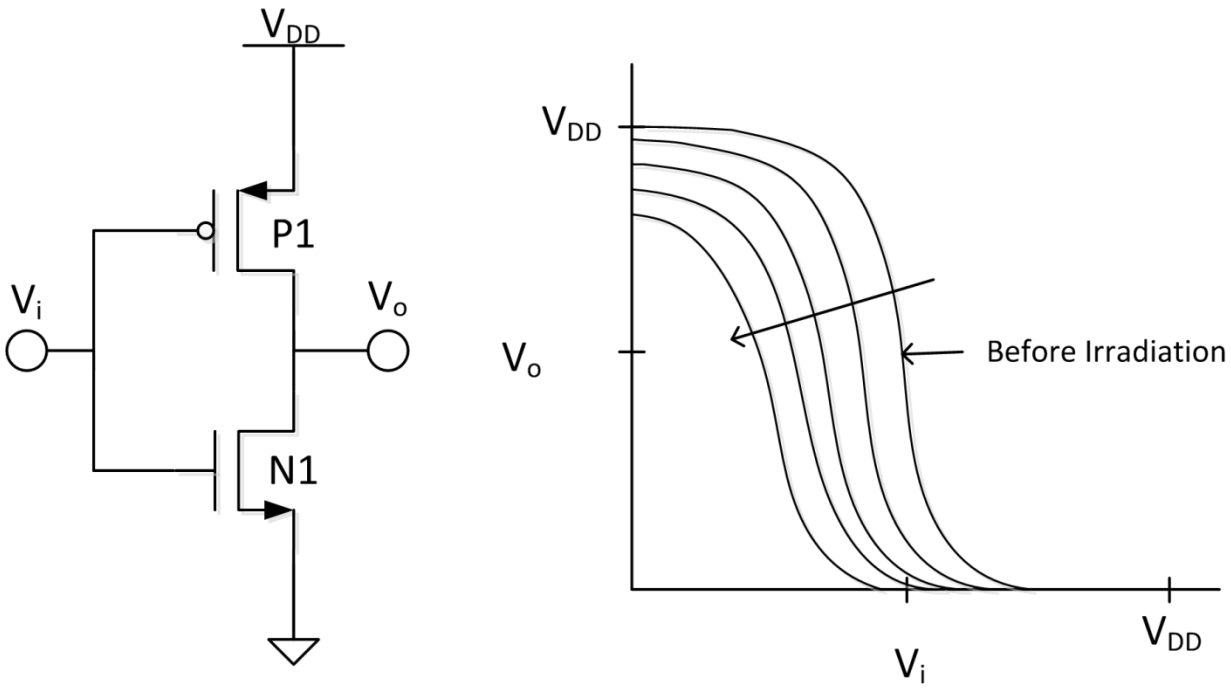

Figure 11 - An inverter and its DC transfer function showing output failure at high-TID levels.

2.6 Hardened-By-Design Layout Techniques

2.6.1 Annular Gate MOSFET

As discussed previously, the largest source of TID-induced leakage in new sub-micron, thin-gate oxide transistors is subthreshold leakage caused by the STI edge between the source and drain. The annular gate MOSFET (shown in Figure 12b) removes the STI edge between the source and the drain. This eliminates the possibility of inverting the channel along this edge. Annular gate MOSFET transistors are also known as edgeless transistors, re-entrant transistors, enclosed-layout transistors and closed-geometry transistors [8].

Figure 13 displays the I_D vs. V_G curves of an annular NFET in the TSMC 0.25 µm process up to 2 Mrad. The annular gate MOSFET exhibits exceptional TID performance. By comparing it with the straight-gate transistor's results (Figure 8), it is clear the annular NFET displays much better sub-threshold leakage performance. The straight-gate transistor displays at least four orders of magnitude increase in the off-state leakage at 400 krad, while the annular displays less than one order of magnitude increase at *2 Mrad*.

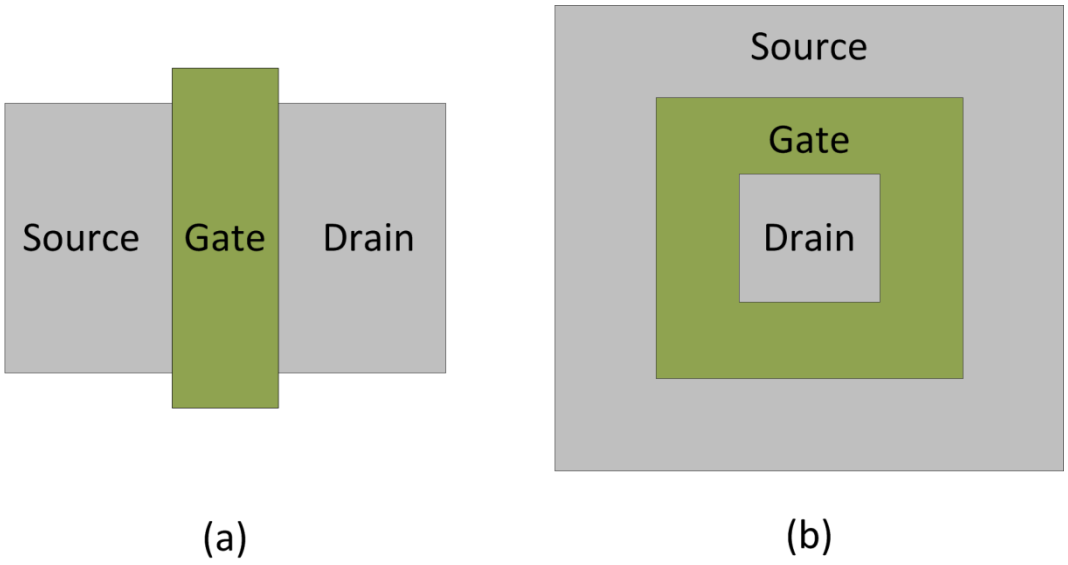

Figure 12 - Top-view layout structure of (a) traditional, straight-gate MOSFET and (b) annular gate MOSFET.

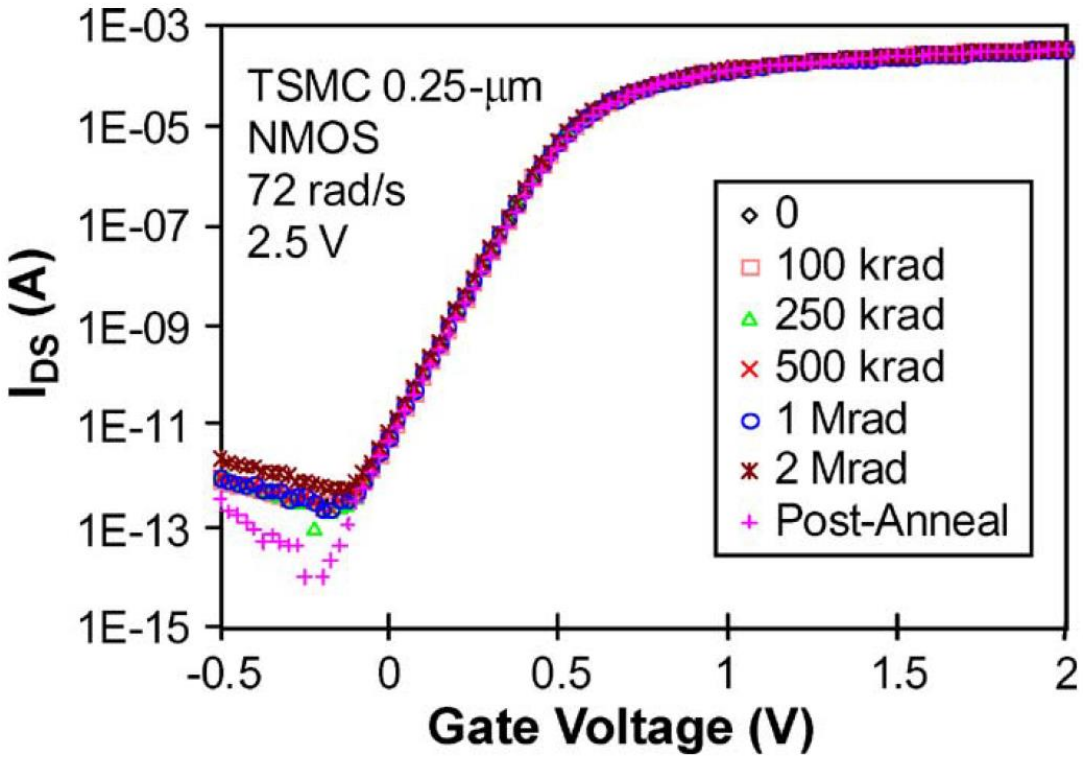

Figure 13 - I_D versus V_G curve for annular gate NFET fabricated in TSMC 0.25 µm process [6].

The annular gate transistor is not without its drawbacks, however. According to Lacoe, their implementation results in area, power and performance penalties. The minimum geometry size of the drain constrains the minimum W/L ratio [8]. For minimum-L devices, the minimum W/L ratio is 12 compared with two for standard edge transistors. In a two-input NOR gate fabricated in a 0.18 µm process, the area penalty for using annular NFETs was 1.25x. In addition, annular devices have increased gate and source/drain capacitances. They are also not symmetric; swapping the source and the drain changes the characteristics of the transistor. Generally, the drain connection is made to the inner ring of the device, because this has less capacitance to the substrate resulting in higher frequency performance. However, this configuration results in a device with higher output conductance than the reversed connection [8].

According to Lacoe, in the rectangular transistor shown in Figure 12b, the channel's length varies around the edges, as does the electric field. This makes modeling the annular gate transistor difficult [6]. Strained-Si substrates are sometimes used to increase carrier mobility in the strain direction. For full benefit of this, the channels of all the transistors on a chip must be fabricated in this direction. Annular gates have a channel in all cardinal directions making it impossible to optimize their performance in strained-Si processes [14]. In addition, many process-development kits (PDKs) do not support annular structures. Workarounds exist, but may require PDK modification and may not be supported by the foundry.

2.6.2 Enclosed-Source/Drain MOSFET

Figure 14 shows an enclosed-source transistor (the drain can be enclosed instead). These transistors have a channel that is nearly transverse like traditional, straight-gate transistors as opposed to the radial transistor [8]. These transistors do not eliminate the transistor edge associated with STI leakage; however, the polysilicon surrounding the source/drain inserts an insulator between the terminal and the leakage path [19].

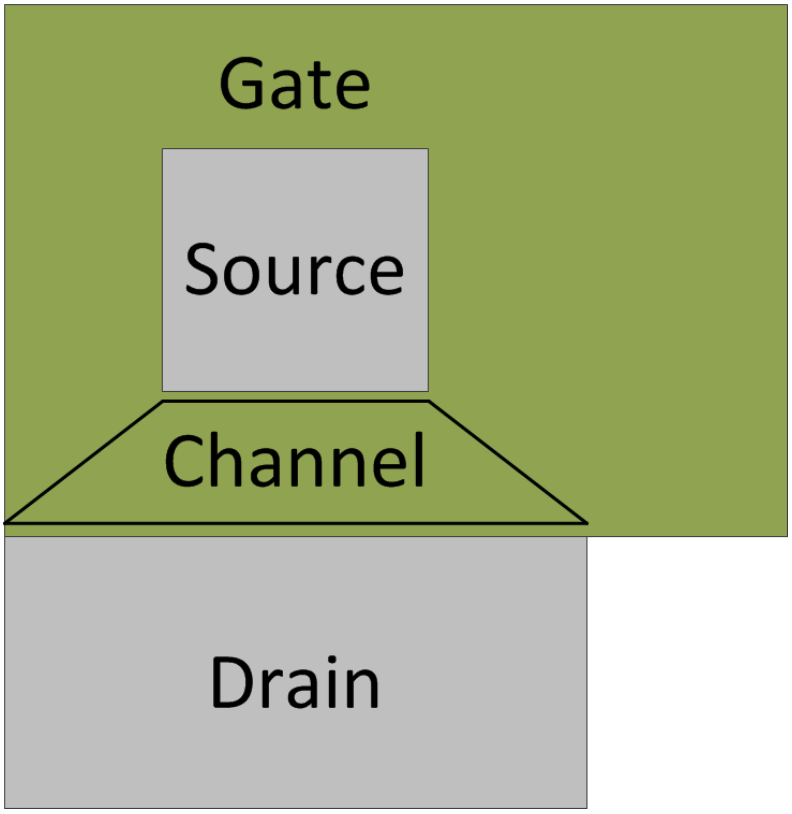

Figure 14 - Top level layout-view of enclosed-source transistor.

The enclosed-source/drain transistor exhibits exceptional TID performance like the annular gate transistors. Its advantage lies with its freedom from the large minimum W/L requirements imposed upon annular gate transistors [19]. In addition, its unidirectional channel lends itself to simpler modeling. However, enclosed-source/drain transistors have larger parasitic gate-to-source/gate-to-drain capacitance (whichever node is enclosed). This is because of the excess polysilicon used to enclose the source or drain. The long polysilicon runs also increase series-gate resistance. Like annular gate transistors, they are larger than straight-gate transistors and are not symmetric. Enclosed-drain transistors have higher Miller capacitance that can hamper device performance in amplifier and CMOS digital applications. Enclosed-source transistors offer better performance. However, to reduce the layout area in large designs, enclosed-source and enclosed-drain transistors may be alternated [19]. In addition, PDK modification may be required to complete layout-versus-schematic (LVS) checks successfully.

2.7 Summary

There are many different TID effects in MOSFET devices. By far the most important effects for digital CMOS circuits are the threshold voltage shifts seen in thick-gate oxide devices and the subthreshold leakage current in thin-gate oxide devices. Annular and enclosed-source transistors are layout techniques to mitigate subthreshold leakage. In general, the annular structure should be used if high W/L ratio is desired and enclosed-source structure if smaller W/L is required. These techniques are not without drawbacks such as increased layout area, reduced device performance, complex modeling and possible implementation difficulties.

CHAPTER 3: METHODOLOGY

3.1 The Inverted-Source Technique

The annular gate and enclosed-source/drain transistors are considered rad-hard layout design techniques because of their excellent TID performance under high TID and high dose rate. Many times circuits need only be radiation tolerant (lower TID and low dose rate). This is especially true for space applications where low dose rates mean devices have time to anneal under irradiation and may withstand a higher total TID [20]. For these applications, the rad-hard layout methods may not be necessary and the difficulties associated with implementing them, as well as the performance penalties, may outweigh any gains. A simpler solution would be to implement a circuit-level technique that uses traditional, straight-gate MOSFETs and provides adequate radiation tolerance.

3.1.1 How it Works

In their paper, "A Radiation-Hard Phase-Locked Loop," Pan, *et al.* presents a circuit-level HBD technique to counteract threshold variation in the NFET [1]. Figure 15 demonstrates this hardening technique for a simple inverter, but the approach extends to other logic functions as well [1]. Transistors P1 and N1 form the typical CMOS inverter. P2 and N2 form an additional inverter added as a hardening circuit. When V_i is a logic 'high', N1 and N2 drive the output to ground. However, when V_i is a logic 'low', the output of the additional hardening circuitry becomes 'high'. In this case, device N1 has a negative V_{GS}. This ensures the transistor is more fully turned-off, reducing the leakage current induced by ionizing radiation.

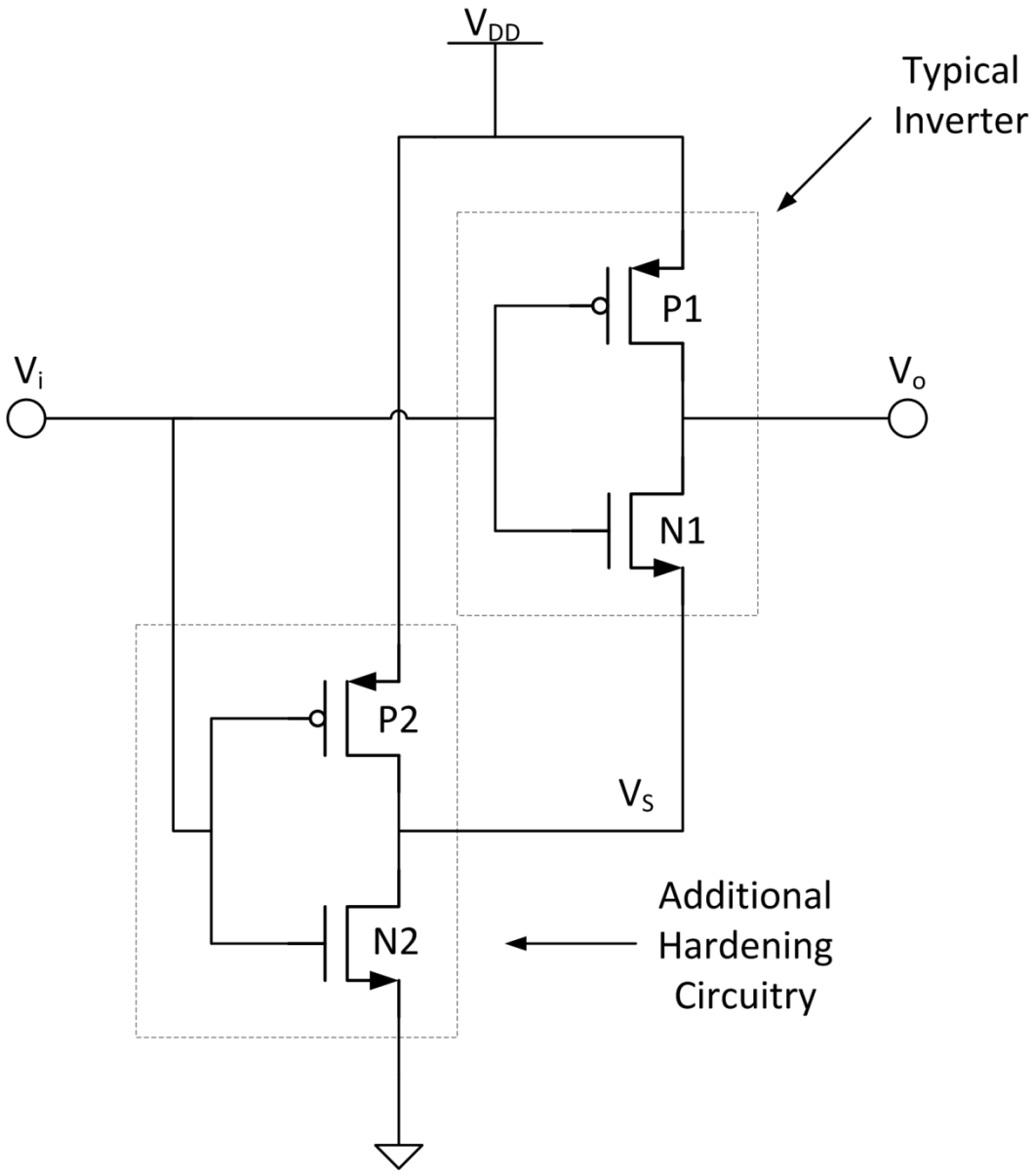

Figure 15 - Inverted-Source TID HBD technique applied to a CMOS inverter logic circuit.

A conceptual I_D vs. V_{GS} curve of an NFET under TID is shown in Figure 16 to help illustrate the hardening technique's advantage. When the input to a traditional CMOS inverter is 'low', it has a V_{GS} of zero , indicated by point A on the V_{GS} axis. Under high-TID, the negative threshold voltage shift of the NFET may cause high off-state currents and output voltage drop for $V_{GS} = 0$ V. N1 of the HBD inverter operates at a $V_{GS} = -V_{DD}$ (point B) when the input is logic 'low' for pre-irradiated devices. As TID increases, this operating point moves to the right to point C, because N2 starts to become leaky as well and the source voltage on N1 (V_S) begins to drop. However, this point C will always be below ground, because the N2 will always have a finite resistance. In addition, P2 is turned-on and supplies current to N2 to help maintain V_S. The HBD inverter maintains a negative V_{GS} across N1 that reduces the drain current helping to preserve digital signal integrity.

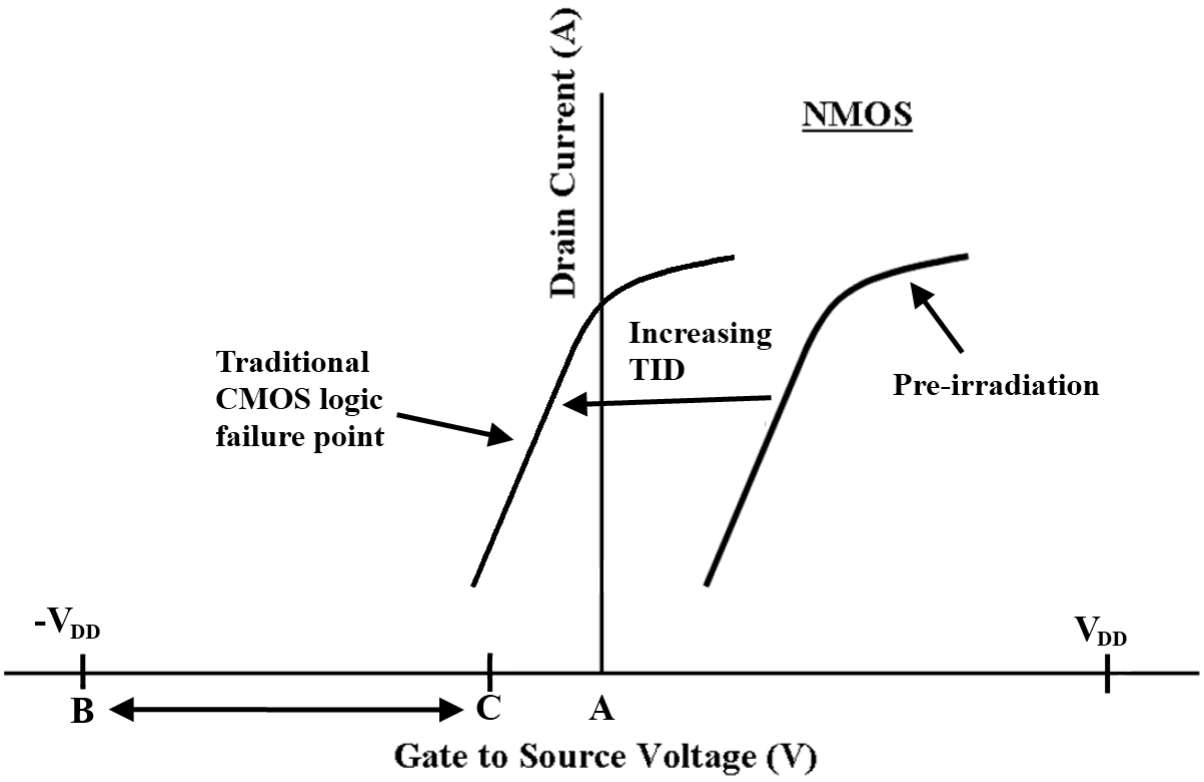

Figure 16 - Conceptual I_D vs. V_{GS} curves for thick-gate oxide NFET under TID. Point A shows the operating point of a traditional CMOS inverter, whereas the spectrum from B to C indicates the operating region of the HBD inverter over TID.

3.1.2 Potential TID Mitigation in Thin-Gate Oxide Devices

The question remains whether the HBD technique will provide any radiation hardening to thin-gate oxide transistors. Some thin-gate oxide NFETs exhibit better gate control over sub-threshold STI leakage than others do. This is believed to be a partial function of the STI corner thickness as discussed previously [18]. Figure 17 shows experimental I_D vs. V_{GS} curves for an NFET fabricated in an unnamed 0.18 µm process [17]. The 200-krad and 400-krad curves have been extrapolated to $-V_{DD}$. The positive slope indicates that the gate maintains some control over the current for $V_{GS} < 0$ V. It is impossible to pinpoint exactly where point C (from Figure 16) lies on this graph, because the characteristics of the PMOS transistor are not known. However, these preliminary results indicate that for this process at least, the thin-gate oxide NFETs sub-threshold leakage can be reduced through application of a negative gate voltage.

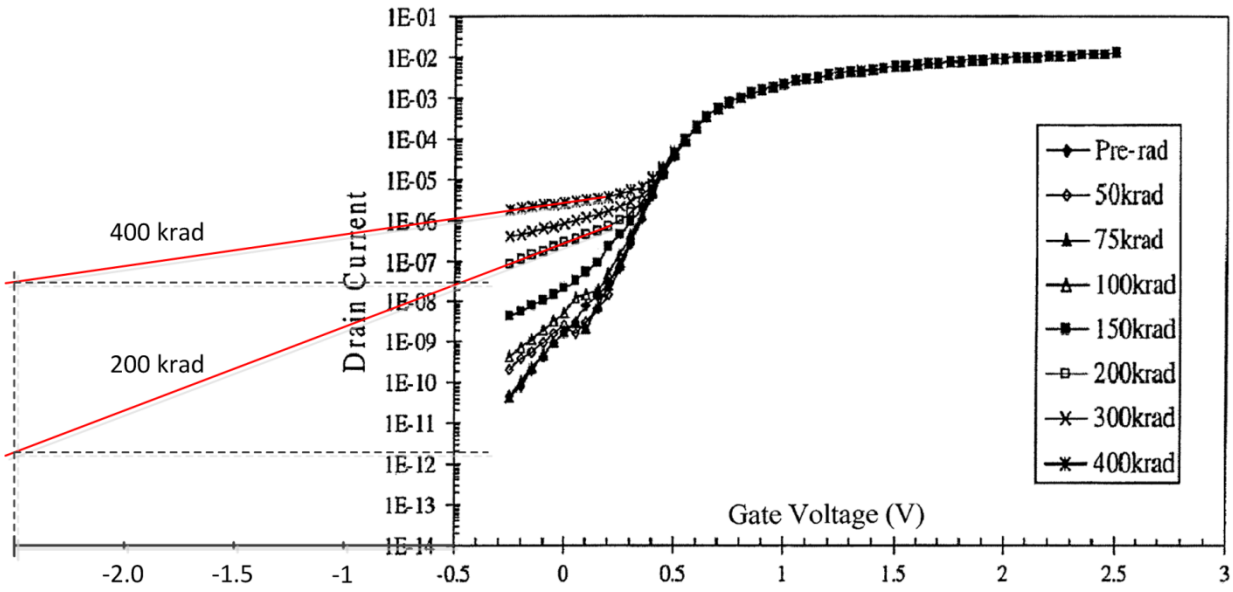

Figure 17 - V_{GS} vs. I_D curve for NMOS fabricated in a 0.18 µm CMOS technology [17]. Extrapolated curves indicate potential reduction in subthreshold leakage current if gate voltage is set below zero volts.

3.1.3 The Inverted-Source's Limitations

It is clear that the HBD technique can provide some TID immunity to NMOS devices that are still capable of providing some gate control for $V_{GS} < 0$ V. Figure 18 shows the V_{GS} vs. I_D curve for an NMOS in TSMC 0.18-µm CMOS process. Here, there is a smaller slope once the transistor is below its threshold voltage. Is there any advantage of using this technique in these devices that provide minimal control of the current for $V_{GS} < 0$ V?

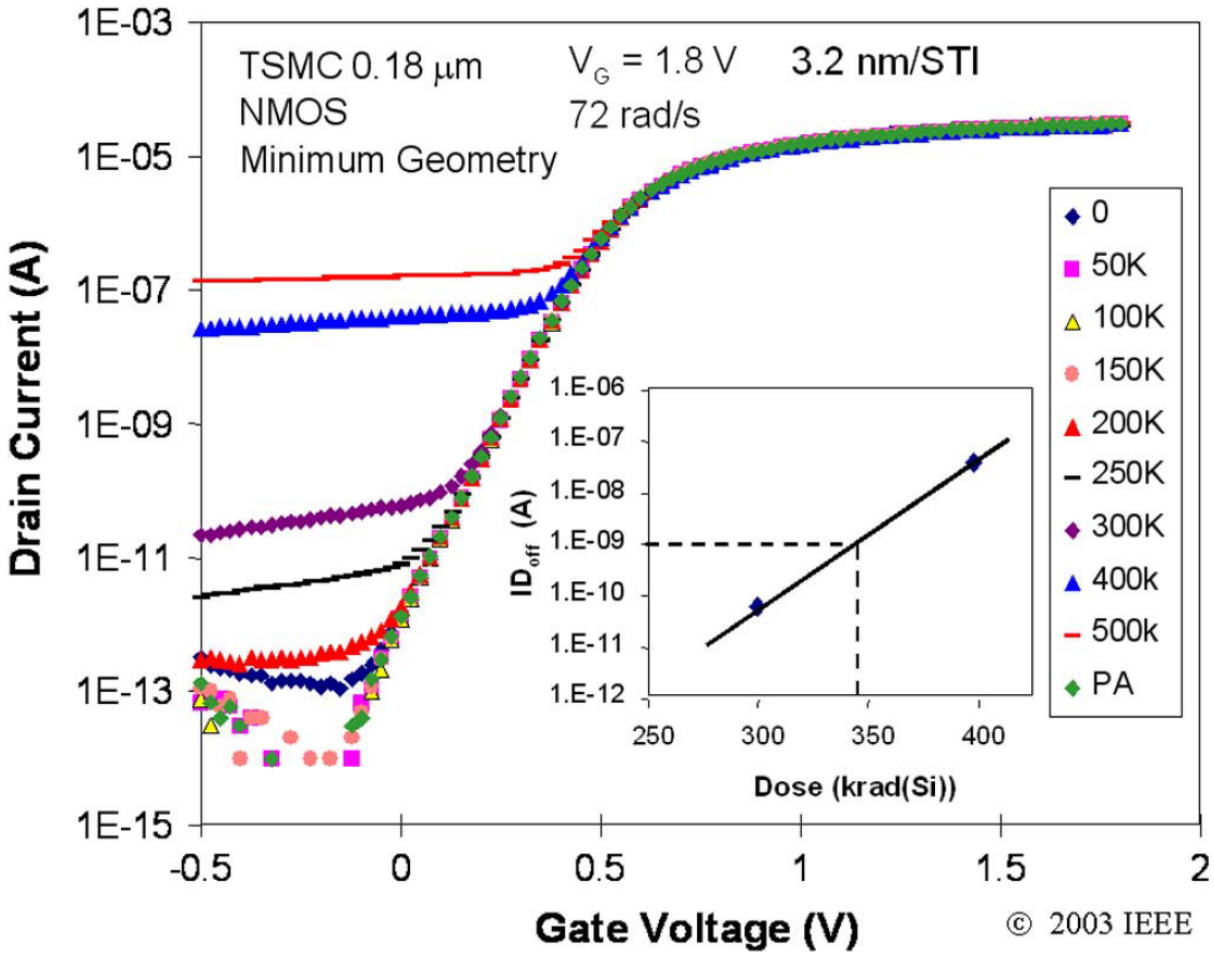

Figure 18 - Measured I_D vs. V_{GS} curves for various TID levels in the TSMC 0.18-µm process [8].

To help answer this question, a MATLAB simulation was performed comparing the output voltage of the DC-equivalent non-HBD inverter and DC-equivalent HBD inverter (Figure 19) if the input voltage is zero. The ratio of the NMOS off-resistance ($R_{off,n}$) to the PMOS on-resistance ($R_{on,p}$) was reduced to simulate increasing TID, since ionizing radiation increases off-state current leakage along the STI edges of the NMOS device (see Chapter 2 discussion). The HBD inverter's two NFETs, $R_{off,N1}$ and $R_{off,N2}$, are set equal to simulate the case where the NMOS devices cannot provide current control for $V_{GS} < 0$ V (N2's effective off-resistance will be the same as N1's off-resistance, even though $V_{GS,N2} = 0$ V and $V_{GS,N1} < 0$ V). This simulation result is shown in Figure 20. The results show that when $R_{off,n}/R_{on,p} = 10$, the HBD inverter is able to maintain an output voltage of 1.787 V while the non-HBD inverter has already fallen to 1.639 V. The results get better as the ratio of resistances continues to fall. For a 1:1 ratio, the HBD inverter has fallen to 1.448 V while the non-HBD inverter is at 0.9104 V or around mid-supply.

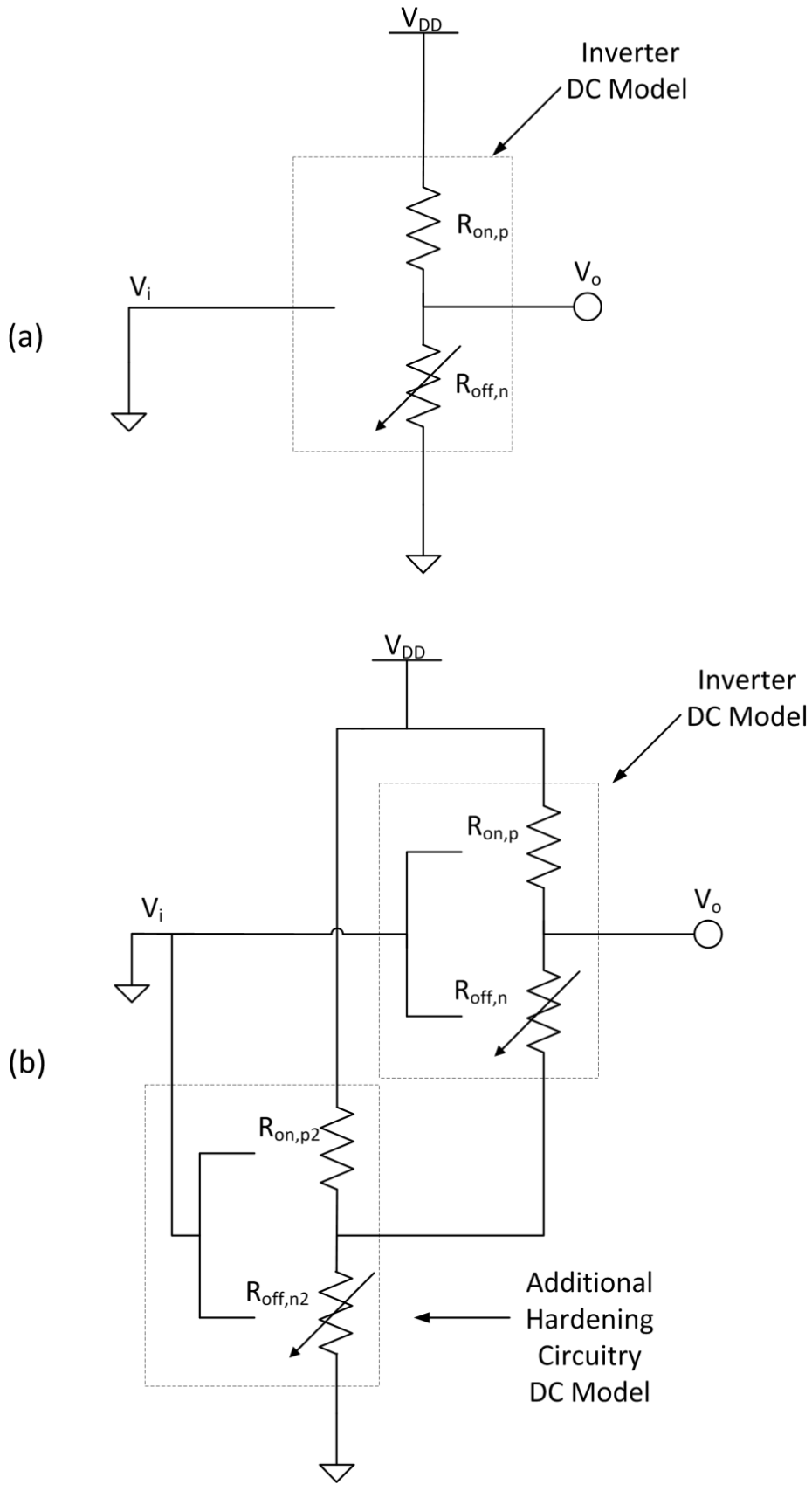

Figure 19 - DC-equivalent model of standard (a) and inverted-source (b) inverter with a logic 'low' input.

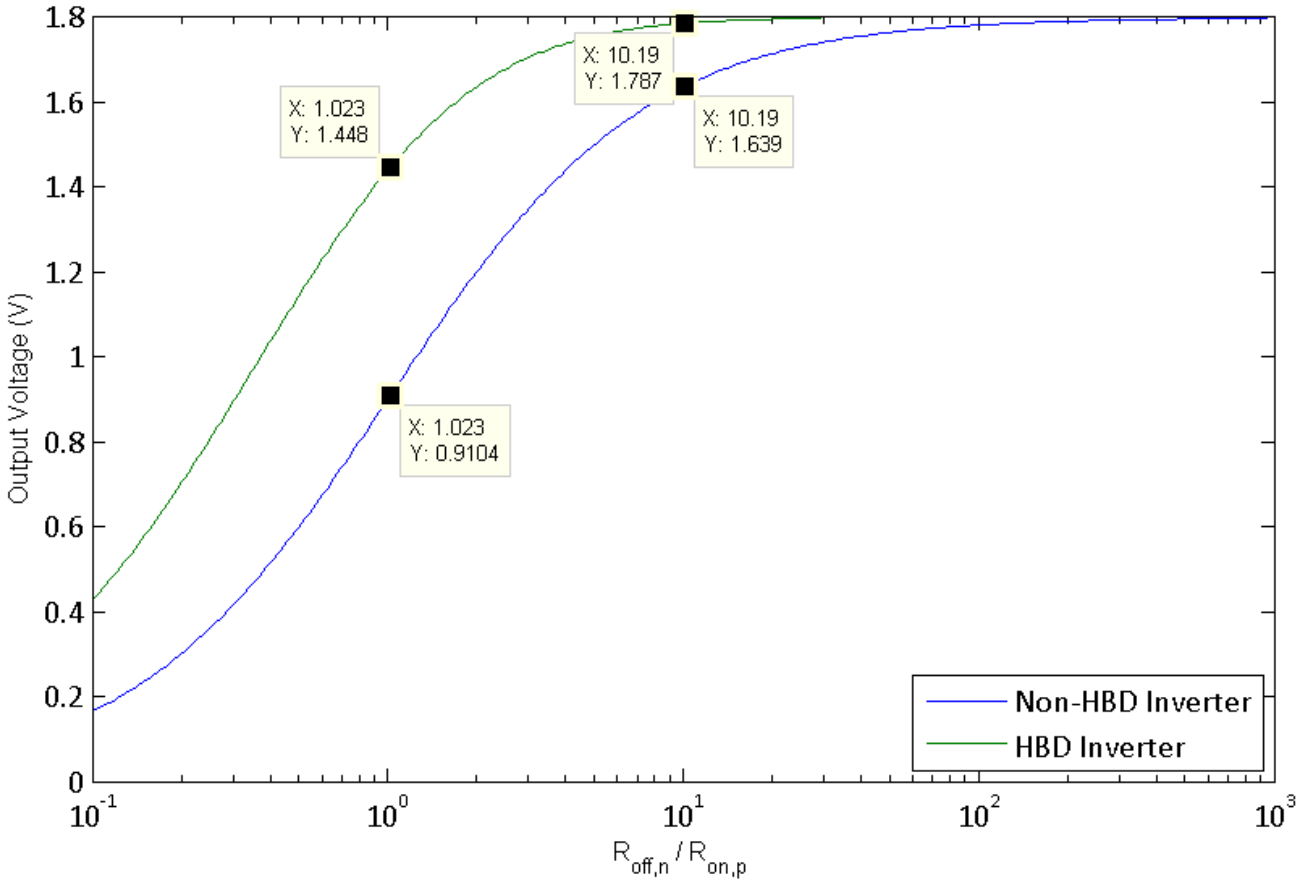

Figure 20 - MATLAB simulation of DC-equivalent models of the traditional, non-HBD inverter and the inverted-source HBD inverter (Figure 19) of NMOS devices that exhibit no current control for $V_{GS} < 0$ V (i.e. worst-case scenario). Y-axis is the output voltage of the inverter and x-axis is the ratio of the NMOS off-resistance to the PMOS on-resistance.

These results indicate the HBD technique hardens digital CMOS circuits even when the devices used have a thin-gate oxide and cannot exert gate control over the current for $V_{GS} < 0$ V. The reasons for this are two-fold. First, using two NFETs in series will double the effective off-resistance. Second, P2, the hardening PMOS transistor, is fully turned-on working to keep V_S close to V_{DD}. This reduces the V_{DS} voltage across N1, reducing leakage current. However, these results should be considered in the scope of a real system. For example in a 1.8-V process if the PMOS has a channel resistance of a few kilo-ohms and the $R_{off,n}/R_{on,p} = 10$, the static leakage current will be on the order of 10's of micro-amps for a single gate. In a digital system, the supply may not be able to handle the leakage currents from thousands of logic gates and it will collapse. This means that the leakage current and not an indeterminate output voltage results in system failure. For this reason, it is postulated that the HBD technique will *not* be effective at mitigating TID in devices where gate control becomes ineffective for $V_{GS} < 0$ V.

An additional and perhaps more fundamental concern with the inverted-source technique revolves around the difference between applying a negative V_{GS} and a negative V_{GB}. Applying a negative V_{GS} to a thick-gate oxide transistor will prevent it from exceeding its threshold voltage and turning on under TID. The primary mechanism of off-state leakage is different for thin-gate oxide transistors. The leakage stems from bulk inversion along the STI edge, because of the trapped positive charge in the STI. For this kind of leakage, will raising the source voltage of the transistor to create a negative V_{GS} aid in turning off the parasitic transistor? It may be that mitigation for this kind of device degradation instead requires a negative gate-to-bulk voltage.

A few performance drawbacks are expected with the HBD approach. First, there will be an approximate 2X speed penalty for using the inverted-source technique. This is because each NFET must have a hardening inverter and the effective gate capacitance of logic circuits will double. This will also increase the layout area, though not by 2X. The active area will double, but overhead from guard rings and metal routing will result in a less than 2X increase in layout area. The power consumption is expected to double as well.

3.1.4 Summary

When referring to HBD layout techniques, Lacoe asserts, "There is no easy way to design around gate-oxide threshold voltage shifts" [8]. However, the circuit-level HBD technique presents itself as a simple method to mitigate the issue. Thicker gate oxide transistors that are susceptible to TID-induced threshold voltage shift are still often used in modern processes on digital inputs and output buffers and high-voltage devices. The inverted source technique may be an ideal choice for these devices. In addition, this technique may provide TID mitigation for thin-gate oxide devices that are capable of exerting some gate control over sub-threshold current leakage for $V_{GS} < 0$ V.

3.2 Thick-Gate Oxide Device Testing

3.2.1 The ALD1106 and ALD1107 Devices

The ALD1106 and ALD1107 are complementary MOSFET arrays fabricated by Advanced Linear Devices, Inc. (ALD). They are packaged in 14-pin dual-inline pin (DIP) ICs. The ALD1106 is the NMOS part and the ALD1107 is the PMOS part. They each house 4 FET devices with drain, gate and source connections for each device and one body connection shared by all of the devices. These arrays represent a good candidate for testing the inverted-source technique. An approximation of the gate-oxide thickness may be calculated from [12]

$$t_{ox} \approx \frac{V_{GS,max} \times SM}{E_{BD,SiO_2}} \tag{3}$$

The devices have a $V_{GS,max}$ voltage of 13.2 V [21]. According to Neaman [15], the breakdown voltage of silicon dioxide (E_{BD,SiO_2}) is around $6 \times 10^6\ V/cm$. In addition, there is generally a 3X safety margin (SM) in gate-oxide thickness, because defects in the oxide lower the breakdown field [15]. Therefore, the oxide thickness of the ALD devices is estimated as

$$t_{ox} \approx \frac{13.2\ V \times 3}{6\ MV/cm} = 66\ nm \tag{4}$$

This thickness is much greater than the five nanometers quoted earlier as the distance at which electrons may easily tunnel into the oxide to cancel the trapped charge.

Therefore, it is expected the ALD devices will show significant threshold voltage shift under ionizing radiation, and they are a good candidate for experimentally verifying the inverted-source technique in a thick-gate oxide device. In addition, these devices are common and easily sourced from an electronics vendor. The V_{DD} voltage used for these devices was selected to be 5 V. The threshold voltage is around 1 V for both chips and a 5 V supply is adequate to switch the devices.

3.2.2 The Test Circuits

There are two test circuits designed to verify the inverted-source technique's TID mitigation capabilities experimentally. Figure 21 shows the first test circuit that is used to compute the V_{GS} vs. I_D curve of the NFET (ALD1106). This test shows the TID leakage mechanisms in the NMOS device, either threshold voltage shift or subthreshold leakage. The ammeter measures the drain current. The V_G and the V_S voltage sources are programmed to sweep V_{GS} from $-V_{DD}$ to V_{DD}. This technique of raising the source voltage above the body voltage emulates the inverted-source HBD technique.

The second test circuit is shown in Figure 22. This circuit utilizes both the ALD1106 and ALD1107 to create a standard CMOS inverter and an HBD inverter. These inverters share the input, V_{in}, that is swept from 0 V to V_{DD}. The output of each inverter is captured to create the DC transfer function of the inverters. This test enables the functionality of the CMOS inverters to be verified and compared.

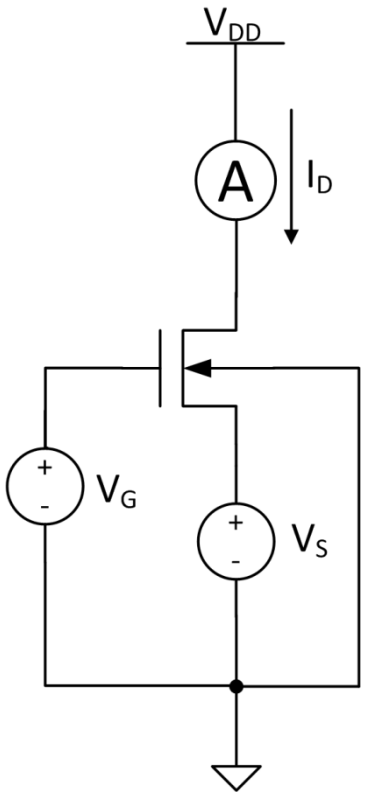

Figure 21 - V_{GS} vs. I_D test circuit.

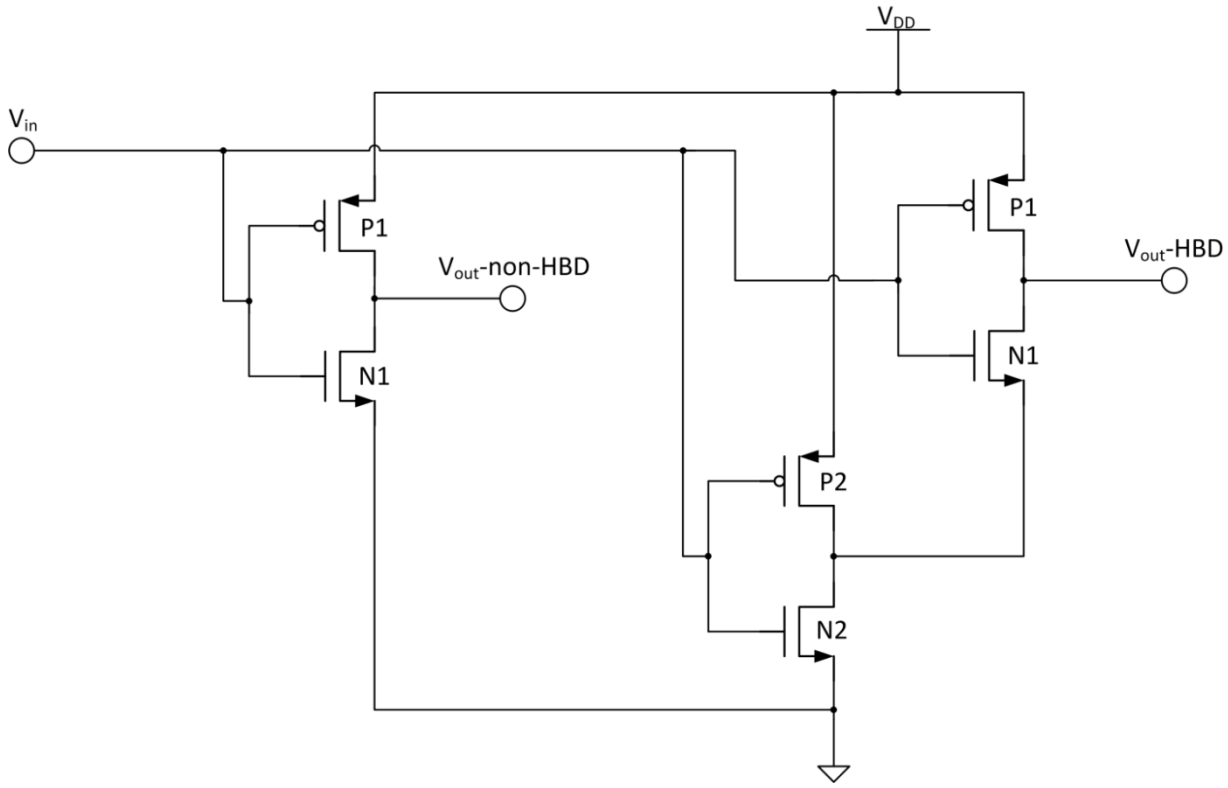

Figure 22 - Inverter DC transfer function test circuit.

3.2.3 *In Situ* Radiation Test Setup at Auburn

The thick-gate oxide test circuits were irradiated at the Auburn University radiation test facility. This facility has a Co-60 source. As it decays, Co-60 releases gamma ray photons with an average energy of 1.25 MeV [9]. These photons are energetic enough to pass through the ALD1106/1107's plastic packaging and ionize the IC wafer.

The source is safely stored at the bottom of a pool of heavy water in a designated room dubbed, "the vault". During irradiation, the source is raised, irradiating the entire vault. The vault is sealed by a large cement door a few feet thick. The entire process of raising and lowering the source and closing and opening the door takes at least 15 minutes to complete. *In situ* testing is desired in order to test the devices in a time efficient manner.

The premise of *in situ* testing consists of taking the measurements while the test boards remain in place requiring no physical human presence in the chamber. This is accomplished using a personal computer running LabVIEW software. The computer interfaces with the desired lab equipment through a USB-GPIB connection or an external PCI-express connection depending on the equipment. A LabVIEW Virtual Instrument (VI) program is written that enables control of this equipment. The VI is setup to perform the desired sweeps and display and store the results (Appendix A.2).

Because of the maximum allowable cable length, the computer must be located near the lab equipment taking the measurements. This means the computer is left inside the test chamber. To gain control and visibility of the computer, a long VGA cable and a USB cable with repeaters is routed through conduit outside the chamber to a monitor, keyboard and mouse. In this way, the test equipment can be controlled and the results viewed immediately without having to open the test chamber doors. Not only does the *in situ* test strategy speed up testing and experiment costs, it helps prevent errors in reading measurements. The VI program can be thoroughly tested and debugged before the actual radiation testing date; therefore, the possibility of human error during measurements is reduced.

A picture of the test setup is shown in Figure 23. The pool of heavy water where the source is stored is shown at the bottom of the image in the center. During irradiation, the source is raised by the elevator shown in the center of the picture. The test board sits 25 cm from the center of the source (as close as practical). At this distance, the boards received a dose rate of 9.219 rad/s. The wires from the test board (carrying only analog DC measurements) are routed to the test equipment at the right of the image. The test equipment is shielded by cinder blocks and lead bricks. The computer is also located here (not visible); the USB and VGA wires are strung up over the test setup and routed outside the chamber to the adjacent room with the monitor, keyboard and mouse.

Figure 23 – Auburn's Co-60 test room where the ALD1106 and ALD1107 chips were irradiated.

3.2.4 Test Methodology

During irradiation, the devices were biased in a worst-case scenario. For the discrete NMOS devices, the full gate voltage of 5 V was applied and the drain voltage was set to zero; the inverters' inputs had 5 V applied which biased the NFETs in a similar fashion. By applying a full gate voltage, the ehps created from the gamma rays are strongly pulled in opposite directions in the gate oxide. The electrons travel toward the gate electrode and escape the oxide, while the holes become trapped as described previously.

Radiation measurements were taken every 10 krad up to 60 krad. The dosage was measured by multiplying the dose rate by the time under irradiation (kept with a stopwatch). Radiation measurements were completed with two fresh sets of chips to verify repeatability. While not completely necessary, the source was raised and lowered each time before the radiation measurements were taken. This added a few minutes to each measurement, but provided security in case issues arose with the LabVIEW VI and the measurements could not be made immediately. Reaching 60 krad total dose with one set of chips took two hours and 42 minutes.

3.3 Thin-Gate Oxide Device Testing

3.3.1 A Rad-Tolerant Frequency Synthesizer in the IBM 7WL Process

A radiation-tolerant, extreme environment capable frequency synthesizer has been proposed and designed. Funded by a NASA SBIR, the frequency synthesizer is designed to operate in the space environment. The IBM 7WL 0.18-µm BiCMOS process was the selected fabrication process. The bulk CMOS devices in this process are susceptible to TID radiation. Figure 24 shows the block diagram of the frequency synthesizer. The highlighted blocks represent CMOS circuits. There are a large number of CMOS blocks; therefore, it is critical that these blocks be tolerant of TID radiation.

The 7WL process has a 1.8-V core voltage; the core CMOS devices have a gate oxide thickness of 3.5 nm [22]. Therefore, the primary TID concern is STI-edge leakage. The STI characteristics of these devices are not known; it is not known whether the gate of these devices will exert discernible current control over the parasitic STI-edge

transistors. Therefore, the inverted-source technique is applied to various CMOS circuits used in the frequency synthesizer. Radiation measurements are taken to compare the HBD circuits with unhardened designs.

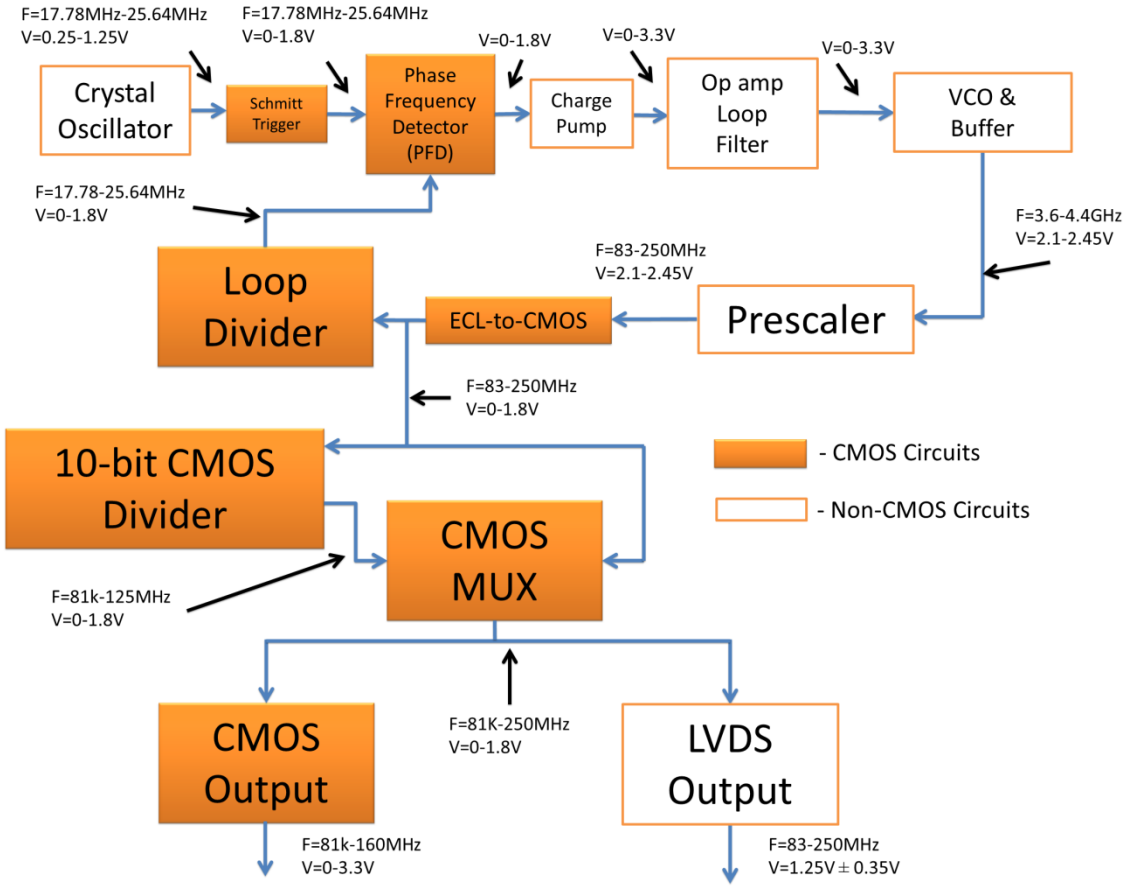

Figure 24 - Block diagram of frequency synthesizer.

3.3.2 The Test Circuits

The development of the frequency synthesizer was spread over two fabrication runs: the *Cappadocia* run and the *Archelais* run. On each of these runs, a couple of test circuits were implemented that test the inverted-source HBD method. The *Cappadocia* die contains non-HBD and HBD test inverters and ring oscillators. The *Archelais* die contains discrete NFETs and a non-HBD and HBD phase-frequency detector (PFD).

3.3.2.1 *Cappadocia* Die: The Test Inverters and Ring Oscillators

HBD and non-HBD test inverters were implemented on the *Cappadocia* fabrication run. The important design variables are the active devices' width and length. The devices' lengths were chosen to be 180 nm (minimum length) for maximum speed. The NMOS and the PMOS widths were chosen to give approximately equal rise and fall times. P+ guard rings surround both the PMOS and NMOS device for inter-device isolation. Figure 25 shows the layout of the test inverters. The HBD inverter is approximately 64% larger than the standard inverter.

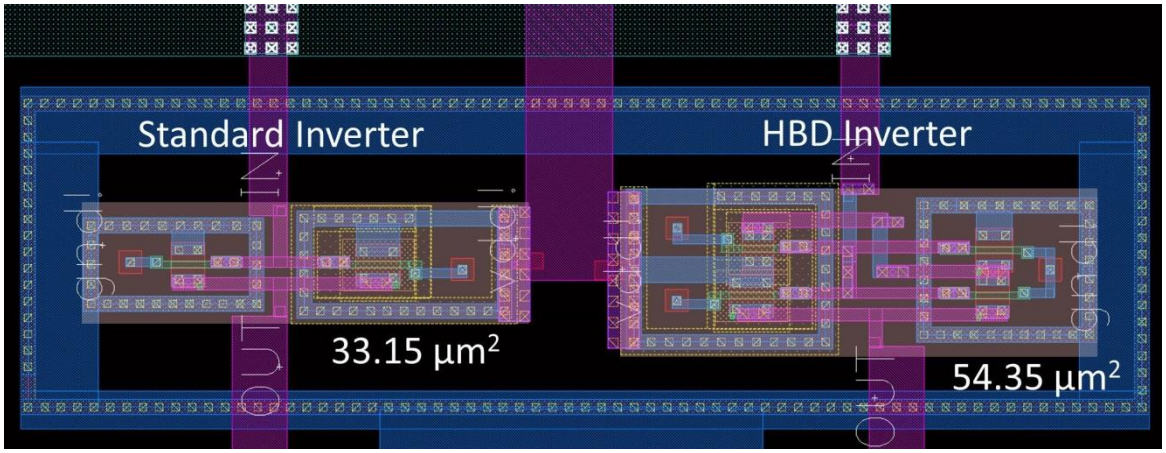

Figure 25 - Layout of 7WL test inverters.

Two thirty-one stage ring oscillators were designed from the test inverters. The ring oscillators are shown in Figure 26. The HBD ring oscillator is around 60% larger in area than the non-HBD inverter. The HBD oscillator is also slower than the non-HBD version. A simulation of the extracted-layout version of the oscillators showed the non-HBD version to oscillate at 160 MHz and the HBD version to oscillate at 74 MHz (room temperature and typical models). In addition to having twice the number of devices in the HBD technique versus standard CMOS, it is thought the longer trace lengths on the inverted source technique contribute to the greater than 2X speed penalty.

One of the inverters in each ring oscillator is actually a two-input NAND gate. One of these inputs is connected in the ring oscillator's loop while the other is padded out and acts an enable/disable bit for the ring oscillators. Both ring oscillators are powered on the same voltage supply, therefore these bits allow only one oscillator to be run at a time to reduce crosstalk interference. The ring oscillator waveforms collected were captured in this manner and resulted in a noticeably cleaner signal.

The ring oscillators' output frequency is divided by eight to make it easier to capture the waveform off-chip. This is accomplished through four HBD positive-edge-triggered D-flip-flops. A D-flip-flop can be used to divide a frequency by two by connecting the Q' output back to the input and driving the clock input with the input frequency signal. After the dividers, the signal is buffered by an HBD exponential horn driver.

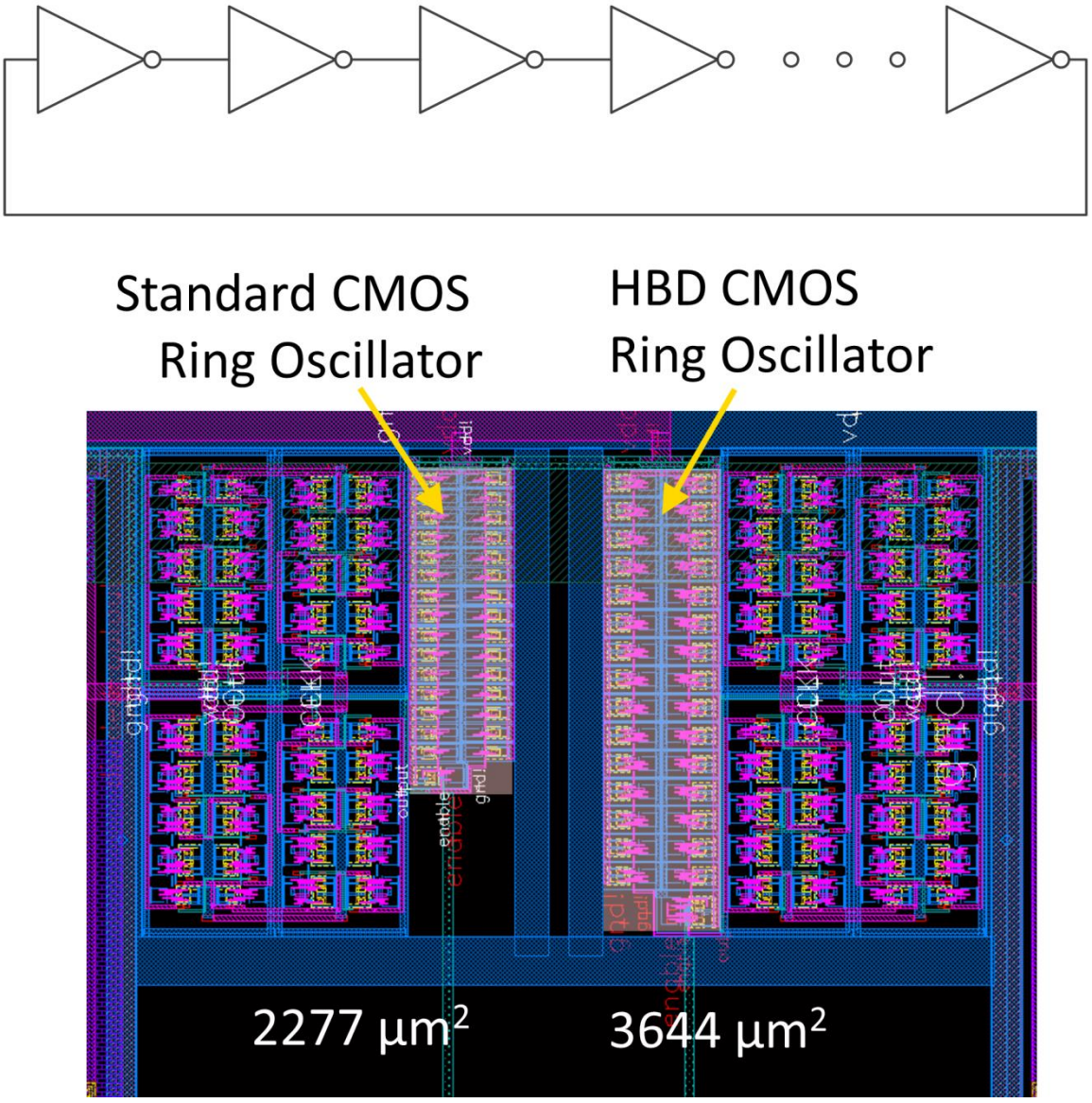

Figure 26 - Block diagram (top) and layout (bottom) of 31-stage test ring oscillators.

3.3.2.2 *Archelais* Die: The Discrete NFET and PFD

There are two radiation test circuits on the *Archelais* die. The first is a discrete NFET shown in Figure 27. The discrete NFET has a gate width of 2 µm, a gate length of 180 nm, and two gate fingers. This circuit is used to capture I_D versus V_{GS} curves to characterize the effects TID radiation has on the NFET. The gate, drain and source nodes are directly padded out with ESD protection. The second set of test circuits are two phase-frequency detectors (PFDs), one HBD and the other non-HBD shown in Figure 28. The two PFD circuits were fabricated to characterize any functional difference between the HBD and non-HBD PFDs.

The PFD is an important CMOS circuit in modern day phase lock loops (PLLs). A schematic of the basic topology is shown in Figure 29. It works by comparing two digital CMOS inputs: the reference clock and the feedback clock. It is desired for the feedback clock to be 'locked' in phase and frequency with the reference clock. The PFD finds the phase difference between the rising edges of the signals, and generates an output signal that has a pulse width proportional to this phase difference. The UP signal is asserted if the reference clock's rising edge is detected first. This signal is held 'high' until the feedback clock's signal is detected. Then the AND gate resets the PFD. The UP signal is used to increase the frequency of the feedback clock so it can 'catch-up' to the reference clock. The DOWN signal is asserted if the feedback clock's rising edge is detected before the reference clock. The delay in the feedback loop prevents what are called "deadzones" in the PFD's input range. These deadzones increase jitter when the clock signals are nearly in-phase. The delay decreases jitter in the PLL at the cost of some of the PFD range. The interested reader can learn more about the PFD and PLLs in general in [23].

The PMOS devices in the fabricated PFD used minimum gate length and the NMOS devices were twice the minimum gate length. The primary reason for slowing the NMOS instead of increasing the PMOS's drive was to decrease hot carrier effects in the NMOS at low temperatures (i.e. < 55°C) [24]. This should also help reduce subthreshold leakage, because the channel length is doubled, doubling the channel resistance. The delay built-in to the fabricated PFDs was created by having an even number of long

device length (1 μm) inverters in the feedback path. Because the HBD PFD already has more inherent delay, only two long-length inverters were used as opposed to the four used in the standard PFD. The HBD PFD is still 40% larger than the non-HBD PFD. However, there is a lot of empty space in the HBD PFD, because layout symmetry in the reference clock and feedback clock paths is more important than saving layout space.

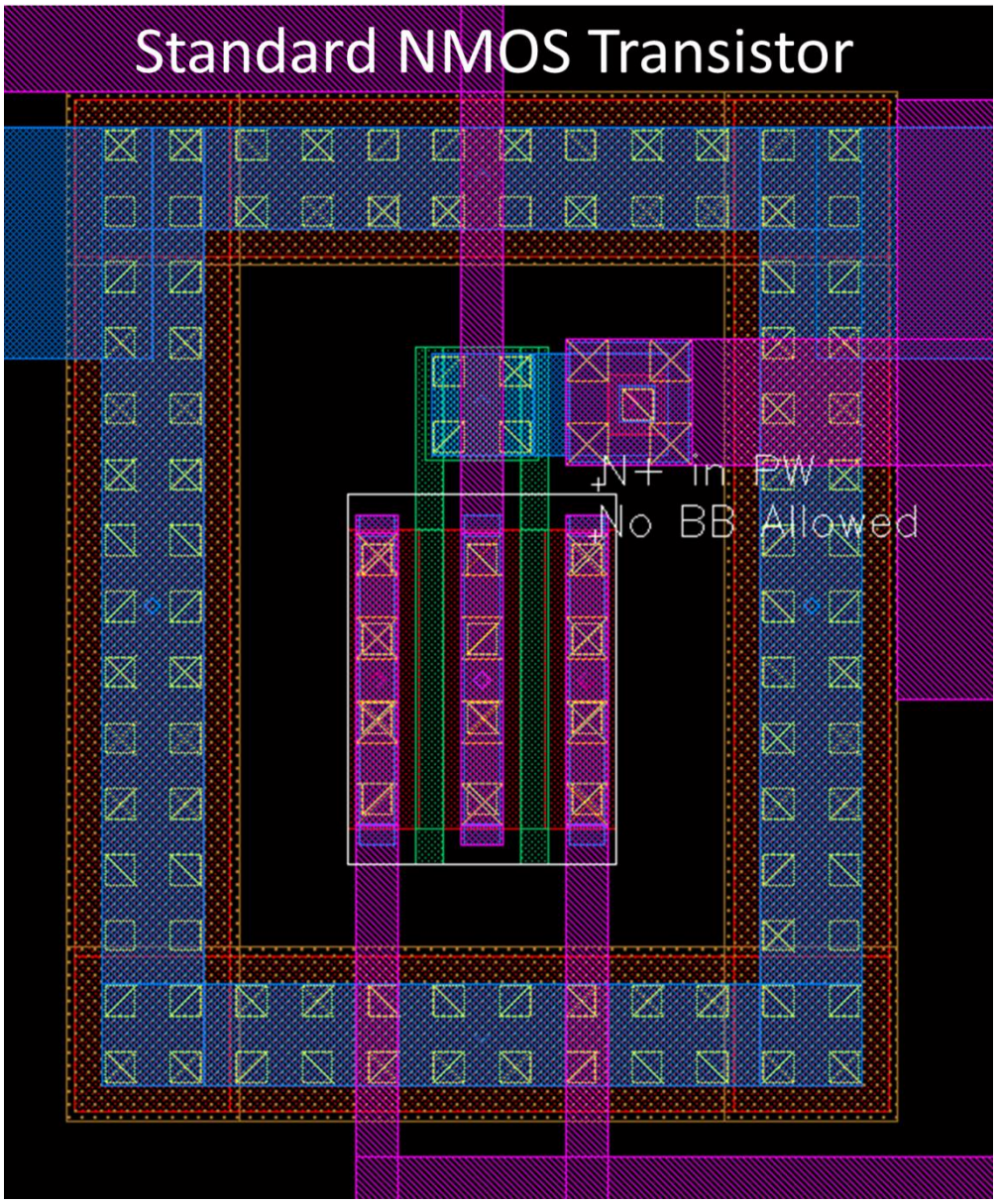

Figure 27 - Discrete NFET on Archelais die. Gate width = 2 µm. Gate length = 180 nm. Number of gate fingers = 2.

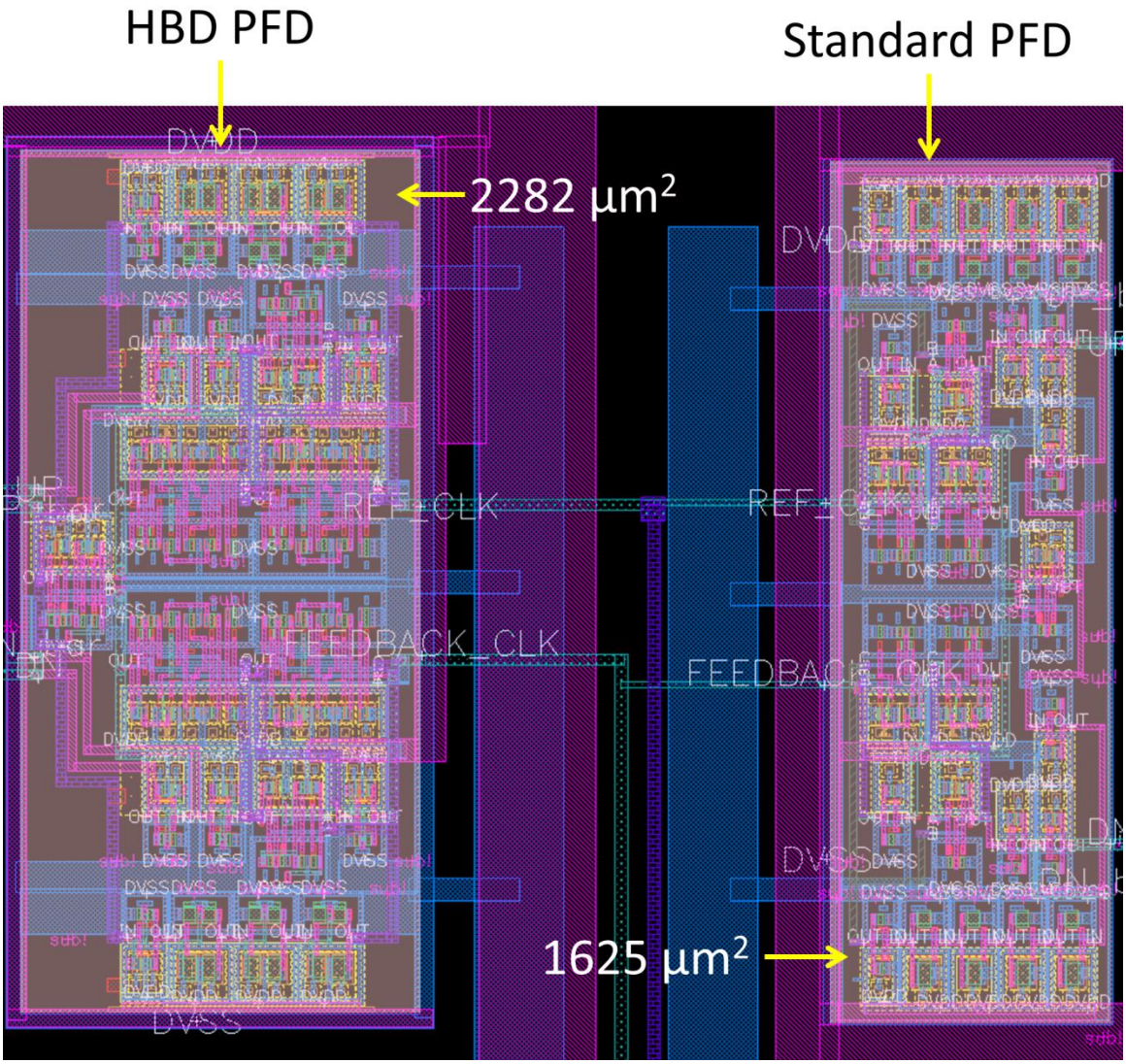

Figure 28 - Standard PFD and HBD PFD layout on Archelais.

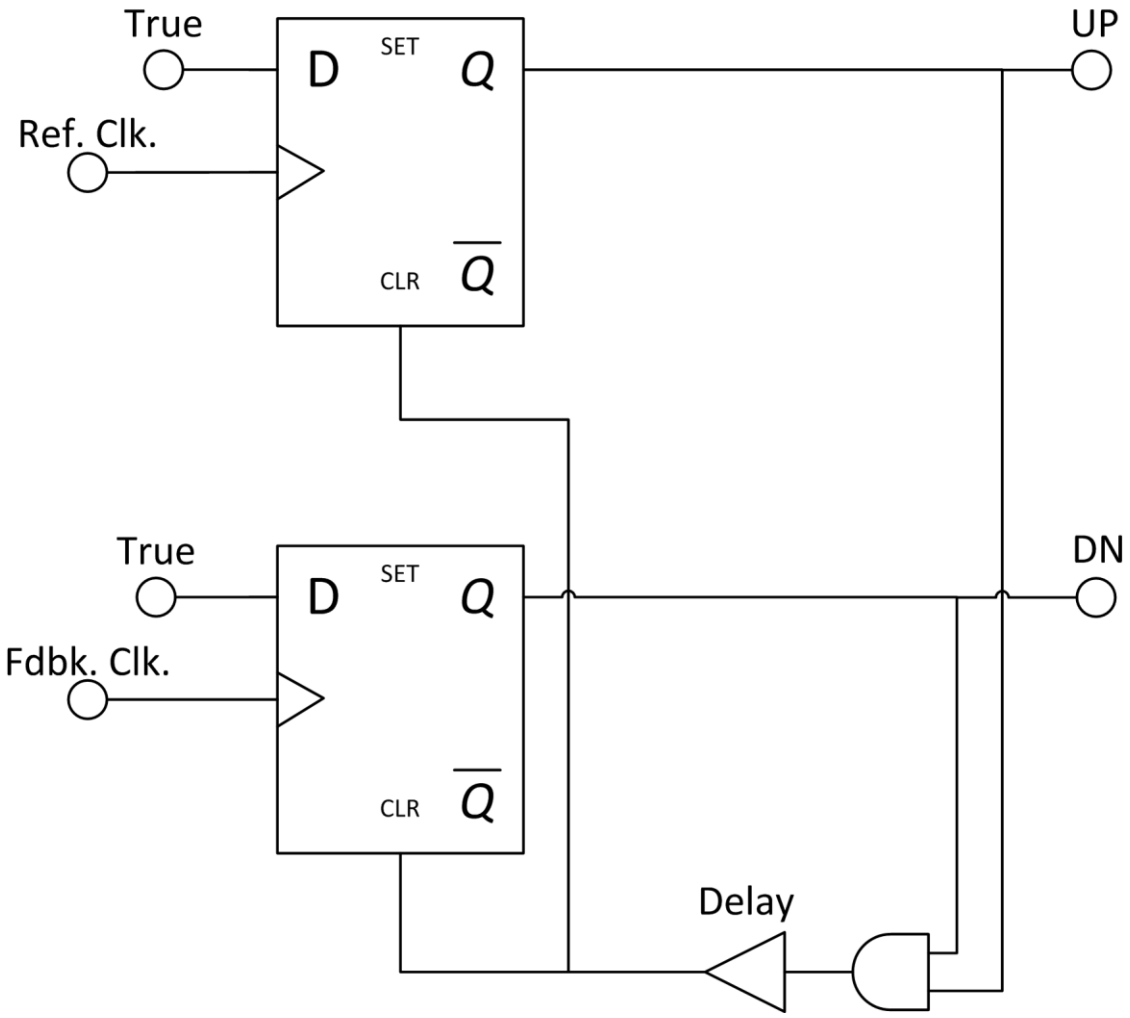

Figure 29 - Phase-frequency detector (PFD) schematic.

3.3.3 *In Situ* Radiation Testing

3.3.3.1 *Cappadocia* Die Test Setup and Methodology

The dose rate of the Co-60 source cannot be easily increased unless the source is replenished or the devices are moved closer to the source. Replenishing the source is not an option and the devices were as close as practical to the source. Thin-gate oxide transistors are largely immune to the catastrophic effects of the threshold voltage shift, so the circuit effects of TID may not be seen until many 100's of krad is reached. To reach 300 krad, the Auburn source would take over nine hours. To test multiple devices, the time commitment quickly rises into days of testing. A faster dose rate is desired.

It has been shown that irradiating MOSFET devices at higher dose rates decreases the annealing time available and therefore increases the TID damage for a certain dosage [20]. If the MOSFET devices are able to survive to a certain dose at a high dose rate, they will be able to survive the same dose at a lower dose rate such as the rates seen in space applications. Vanderbilt University has an ARACOR 10 keV X-ray machine available for use. The X-ray source is capable of any dose rate between 83 rad/s and 517 rad/s.

In contrast to Auburn's Co-60 source, the ARACOR machine (left side of Figure 30) does not require an entire room; the test setup does not need to be far from the machine. This eliminates the need for excessively long wires to control the PC; it and the rest of the test equipment are located beside the machine where they can be monitored and controlled directly.

The X-ray's photons are much less powerful than in the gamma ray source; the lid of the test die was removed to expose the die directly to the beam. Otherwise, the beam would be greatly attenuated.

Each *Cappadocia* test die contain one set of test inverters and ring oscillators. Two of the test die were irradiated quickly at 270 rad/s. This dose rate was calculated from a curve-fitting program with X-ray power supply's voltage and current as inputs. These values were selected as 35 kV and 15.5 mA to get the desired dose rate. The input to the inverters was set to 1.8 V and the ring oscillators were enabled during irradiation. The measurements were taken at certain dosage increments with the X-ray beam turned

off. The dies were irradiated to 300 krad. The increments were as follows: 10 krad, 25 krad, 50 krad, 100 krad, 150 krad, and 300 krad.

A third test die captured measurements of the ring oscillator during two different dose rates at a few dosages. Oscilloscope images of the output were captured for dose rates of 83.3 rad/s and 500 rad/s at pre-irradiation, 50 krad, 100 krad and 200 krad. The dose rate of 500 rad/s was used to get to the next dosage increment.

Figure 30 - Vanderbilt University's X-ray source (left) and the Cappadocia testing equipment (right).

3.3.3.2 *Archelais* Test Setup and Methodology

One discrete NFET device was available in a 14-pin DIP with a removable lid. The test setup consists of three Keithley 2400 SourceMeters controlling the gate, drain, and source voltages and measuring the drain current and the Agilent E3631A power supply powering the ESD pad ring of the chip. A custom LabVIEW VI was used to control these instruments and run the I_D vs. V_{GS} sweep. The X-ray testing was performed at Vanderbilt and was similar to the testing with *Cappadocia* chips.

It is always desired to show the repeatability of an experiment. Having access to only one de-lidded die containing the discrete NFET limits the repeatability of any radiation testing performed on it. There was the same part packaged in a permanently lidded 56-pin **Q**uad **F**lat-pack (**N**o-leads) (QFN). In addition to being lidded, this package is housed in a fully enclosed socket on the test board. These two obstructions will attenuate the X-rays that reach the die. A PIN diode detector that gives the dose rate of the X-rays was used to compensate for this attenuation. This was accomplished by measuring the dose rate without any obstructions in the path between the PIN diode detector and the X-ray source and then again with the top portion of the socket and a package lid in the path of the X-rays.

The dose rate given by the PIN diode was for silicon; however, the SiO_2 dose rate is more important in MOSFET devices as described in the Background chapter. The lab engineer overseeing the testing at Vanderbilt provided assistance with the conversion from dose rate (krad/min in Si) to dose rate (rad/s in SiO_2) (see equation (5) below) [25].

$$DR_{SiO_2}\left(\frac{rad}{s}\right) = \frac{DR_{Si}\left(\frac{krad}{\min}\right)}{1.8 \times 1.32} \times \frac{1000}{60} \tag{5}$$

The 1.8 term converts between the dose rate in Si and SiO_2 and the 1.32 term is a conversion needed specifically when a PIN diode detector is used [25].

The dose rate as calculated from the curve fit program was 270 rad/s (power supply set to 35 kV and 15.5 mA). The PIN diode detector gave a dose rate of 262 rad/s (error of about 3.1 %). When the top of the socket and the lid were placed in front of the diode, the dose rate dropped to 7.86 rad/s (3 % of the original dose rate). With this kind of dose rate, it would take a very long time to reach reasonable TID dosages. A small

metal support pin in the top of the socket was determined to attenuate the X-rays severely. The socket and lid were turned at an angle so the X-rays would miss this metal pin. With this angle, the dose rate jumped to 18 rad/s (6.9 % of the original dose rate). At this dose rate, it would still take over two hours to reach even 150 krad. The X-rays power was increased by about three times (40 kV and 39 mA). This new setting gave a dose rate of 60.6 rad/s through the socket and lid. This was the dose rate used to test the discrete NFET in the lidded-QFN packaged. The accuracy of this calibration method will be examined in the results. Figure 31 shows the *in situ* test setup. The X-ray source is the metallic tubular structure on the top of the image. The attachment at the end of this is a filter that helps filter some of the low power X-rays [25]. The board is tilted to avoid the metal support pin (visible in the center of the top portion of the socket). In addition, the chip is positioned at approximately the same distance from the source as the PIN detector diode (not visible) to ensure the same dose rate.

Unfortunately, the PFD was not able to be radiation tested. Time constraints limited its testing at the radiation test facility. However, it was still of interest to see whether there are any functional differences between the inverted-source technique and standard CMOS.

The PFDs were tested for functionality and performance at room temperature. The two inputs to the PFD (Ref. Clk. and Fdbk. Clk.) are provided by two waveform generators. The phase and frequency difference between these two inputs are what the PFD detects, so it is important to be able to control these parameters. To accomplish this, the waveform generators needed to be synchronized with the 10 MHz reference clock output of one connected to the 10 MHz reference clock input of the other with a BNC cable. With this connection, the waveform generators are synchronized and the phase and frequency difference between the two can be controlled to test the PFD properly. The outputs were captured with an Agilent 300 MHz oscilloscope and power was provided by the Agilent E3631A power supply.

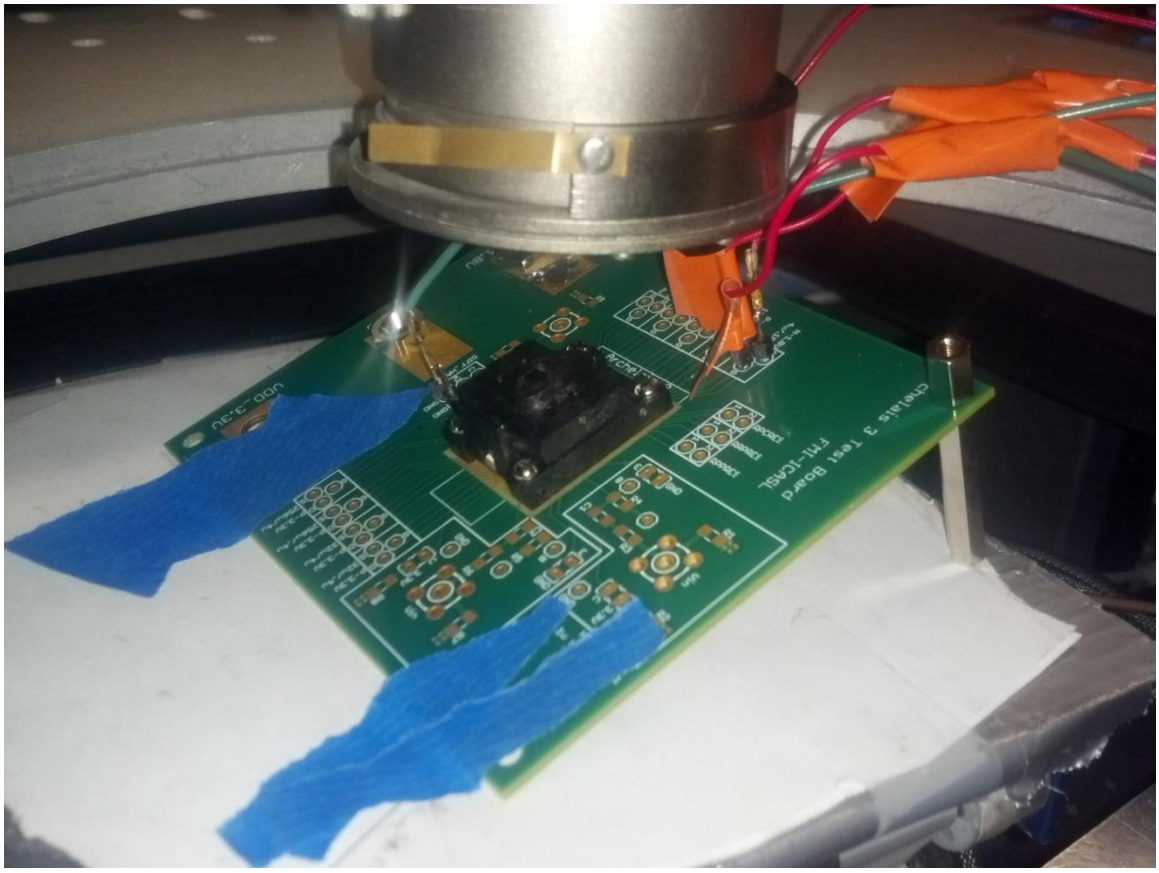

Figure 31 - TID testing of discrete NFET in lidded QFN (housed within a socket).

3.3.4 Summary

There were many different test devices used to characterize the HBD technique. The radiation-testing summary is provided in Table 1. In addition, recall the PFDs were not irradiated; though, they were tested and compared under nominal conditions.

Table 1 - The radiation-testing summary.

Test Devices	Test Circuits	Source	Dosage
ALD1106/1107	Inverter DC TF	Cobalt-60 – 9.219 rad/s	60 krad
	NMOS I_D vs. V_{GS}		
IBM 7WL BiCMOS	Inverter DC TF	10 keV X-ray – 270 rad/s and 83 rad/s	300 krad
	Ring Oscillator		
	NMOS I_D vs. V_{GS}	10 keV X-ray – 270 rad/s and 60.6 rad/s	300 krad
	Phase Frequency Detectors (PFDs)	N/A	N/A

CHAPTER 4: RESULTS AND DISCUSSION

4.1 Thick-Gate Oxide Device Test Results

4.1.1 Inverter Transfer Function

The ALD1106/1107 inverter transfer functions over TID are shown in Figure 32 (non-HBD inverter) and Figure 33 (inverted-source inverter). The trends seen agree well with Figures 4 and 5 in Dong Pan *et al.*'s paper [1]. Therefore, these results experimentally verify that paper's conclusion that the inverted-source technique is effective at mitigating TID in thick-gate oxide devices.

The non-HBD inverter's transfer function shows large variability with TID. The output voltage for a zero volt input begins to degrade at 30 krad. By 60 krad, the output voltage has dropped to around 4.4 V. Depending on the noise margins of the digital system, these circuits could be failing at 60 krad. The HBD inverter, on the other hand, has no visible degradation in output up to the tested 60 krad dose. The shift in switching point appears to be relatively linear over TID. By extrapolating the HBD inverter's data, it can be expected that the output will not start to degrade until around 90 krad, and it will not reach 4.4 V until around 120 krad. This indicates the HBD inverter increases the TID hardness of CMOS circuits implemented with thick-gate oxide (~66 nm in this case) transistors by around twice as much as unhardened designs.

The reasons for the inverted-source's effectiveness are two-fold. First, the pre-irradiation switching point of the HBD inverter is higher than that of non-HBD inverter (2.7 V vs. 2.1 V). The ALD1106 and ALD1107 are discrete components; the drive strength ratio of the PMOS and NMOS is set (unless multiple devices are used in parallel or series). The HBD technique effectively has two NFETs in series doubling the effective length of the pull-down transistor. This increases its switching point making the circuit more tolerant of ionizing radiation. This effect could be utilized in fabrication processes where the W/L length is adjustable at the cost of circuit performance.

Second, and more importantly, the HBD version shows smaller shifts in switching point for each TID increment. The switching point changed by 1.5 V in the standard

inverter and 1.2 V in the HBD inverter. This indicates that applying a negative V_{GS} is effective at reducing leakage current in these devices. These results were repeatable.

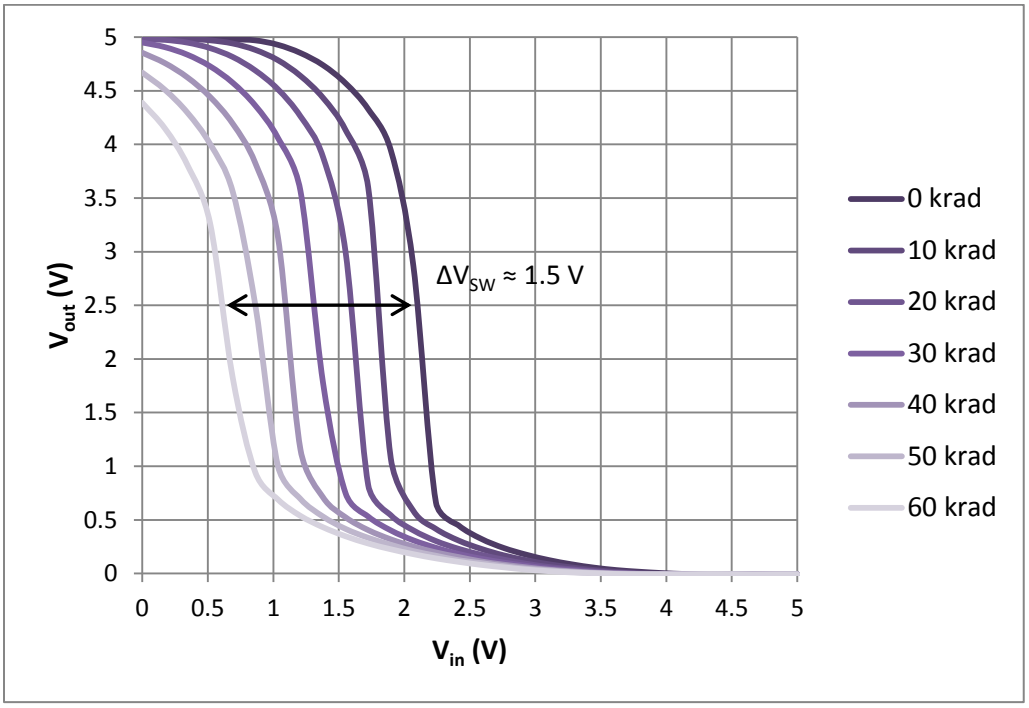

Figure 32 - ALD1106/1107 non-HBD inverter transfer function to 60 krad TID.

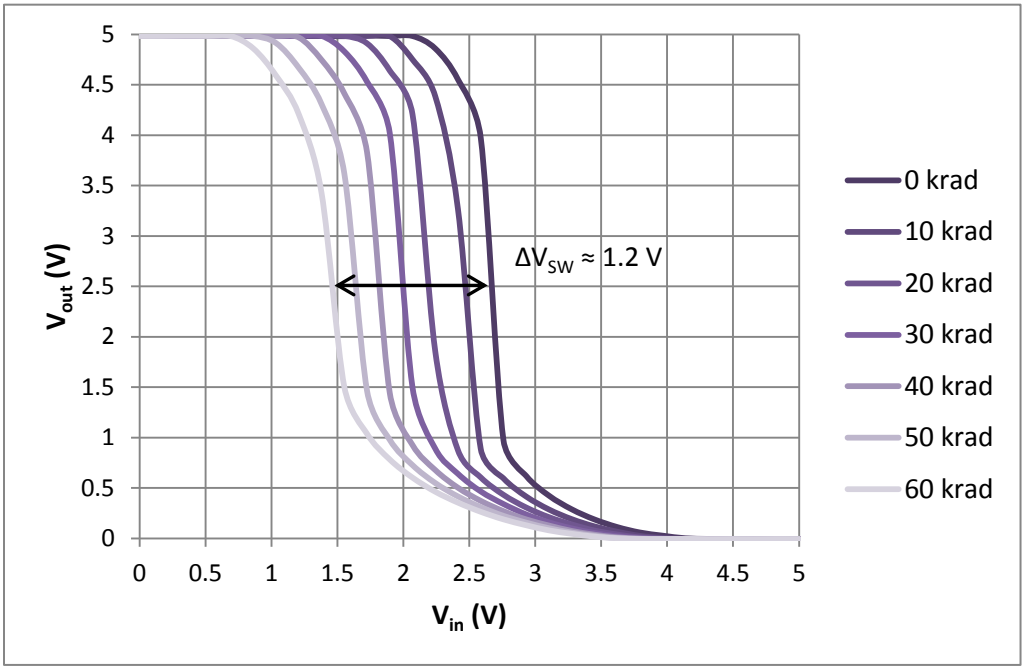

Figure 33 - ALD1106/1107 HBD inverter transfer function to 60 krad TID.

4.1.2 ALD1106 I_D vs. V_{GS}

Figure 34 shows the I_D versus V_{GS} curve for the ALD1106 (NMOS part) to 60 krad. The results show an approximate −0.3 V shift in threshold voltage for every 10 krad increment in total dose. The important points to observe are the leakage currents at zero V_{GS}. By 30 krad, the leakage current is approximately 10 µA. By 60 krad, the device switches from an enhancement mode to a depletion mode device in which a negative V_{GS} is needed to turn the device off. These results help confirm the inverter transfer function results.

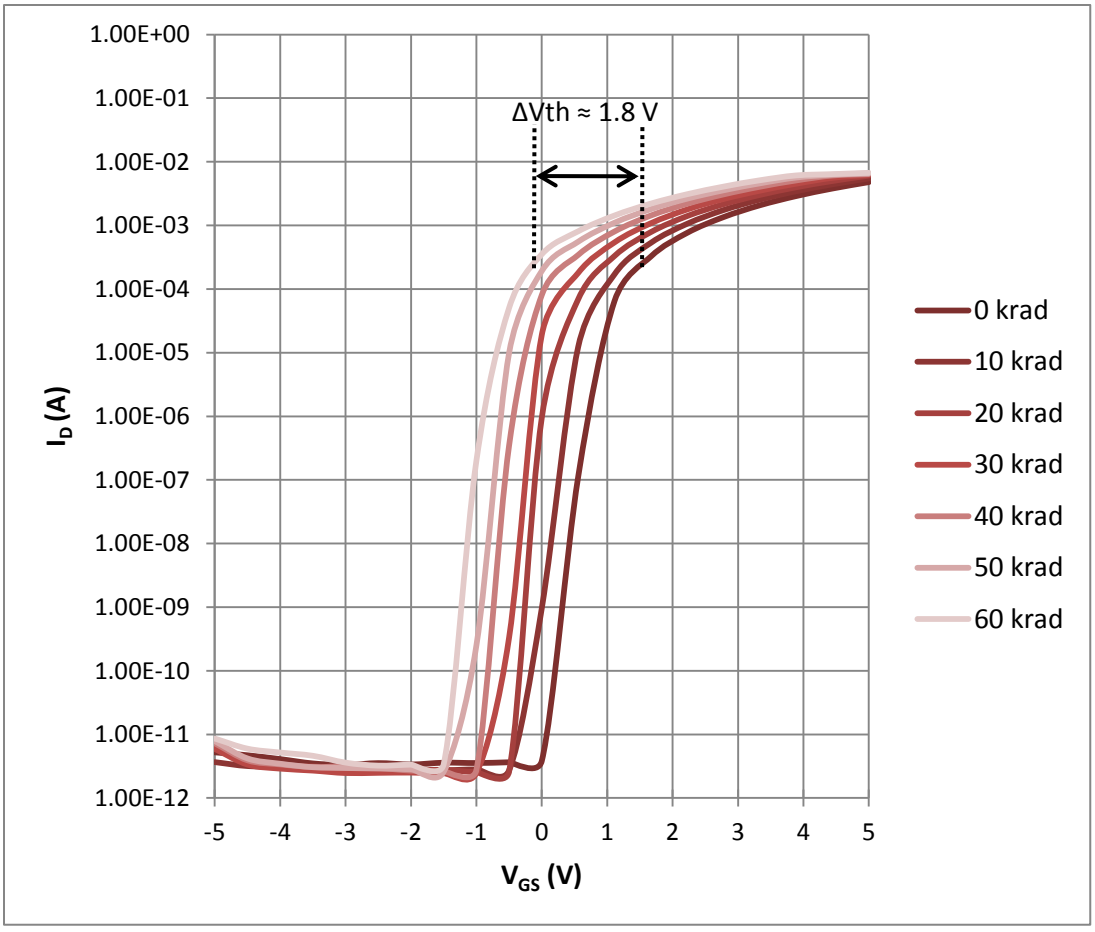

Figure 34 - ALD1106 I_D vs. V_{GS} curves to 60 krad.

4.2 Thin-Gate Oxide Device Test Results

4.2.1 The Inverter Transfer Function

The non-HBD and HBD versions of the 7WL inverters were both irradiated to 300 krad. These results are shown in Figure 35 and Figure 36 respectively. Both HBD and non-HBD show nearly negligible changes in the switching point. However, the non-HBD inverter shows a more dramatic change in its transfer function to the left of the switching point. This is the area where the NMOS is being turned off. Even with a zero volt input, the output cannot fully reach the 1.8 V rail in the non-HBD inverter (1.78 V). The HBD inverter's curve shows less change particularly in the area to the left of the switching point.

However, recall the inverted-source technique's circuit (Figure 15); N2 has a V_{GS} of zero volts and will leak as much current as a standard CMOS inverter. It is believed that the leakage current's burden on the voltage supply will play a more important role than the drop in output voltage in system failure from TID. That is, if TID becomes an issue at all. Most space applications need up to 300 krad at most and with a much lower dose rate than tested allowing for more annealing [14]. These results indicate the HBD technique *does* help maintain the output voltage of CMOS circuitry in thin-gate oxide devices, but these devices already display what may be considered adequate TID performance for many digital CMOS applications.

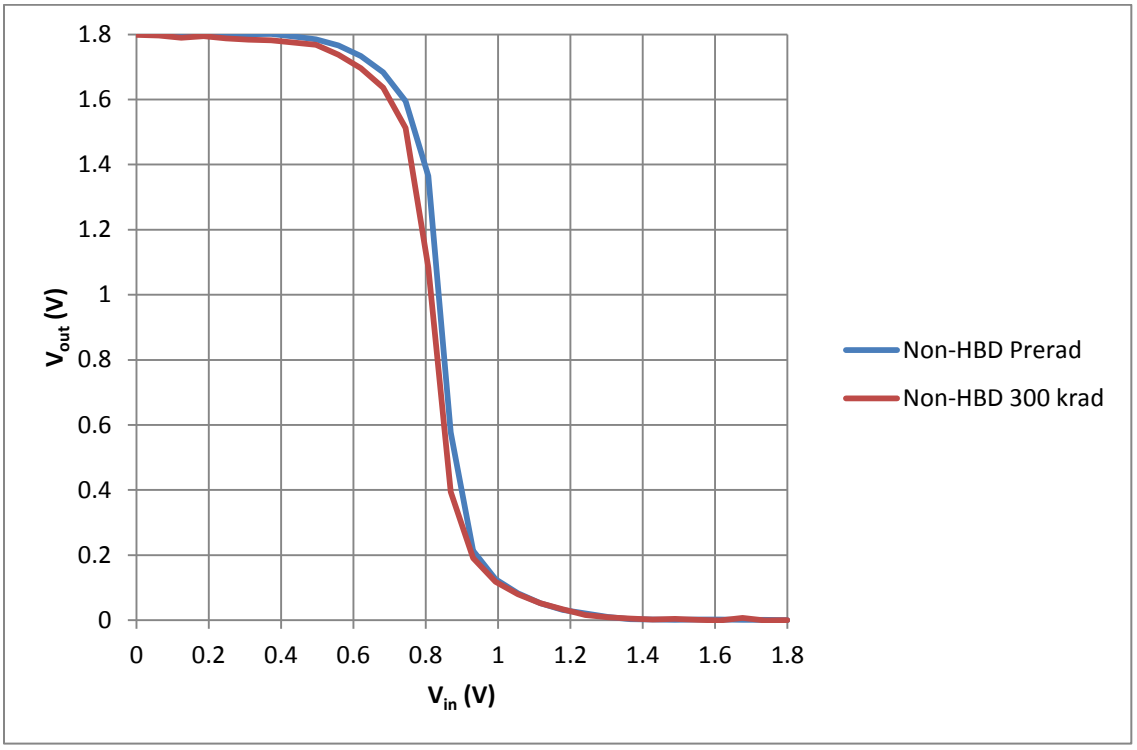

Figure 35 – TID effects on the non-HBD inverter transfer function.

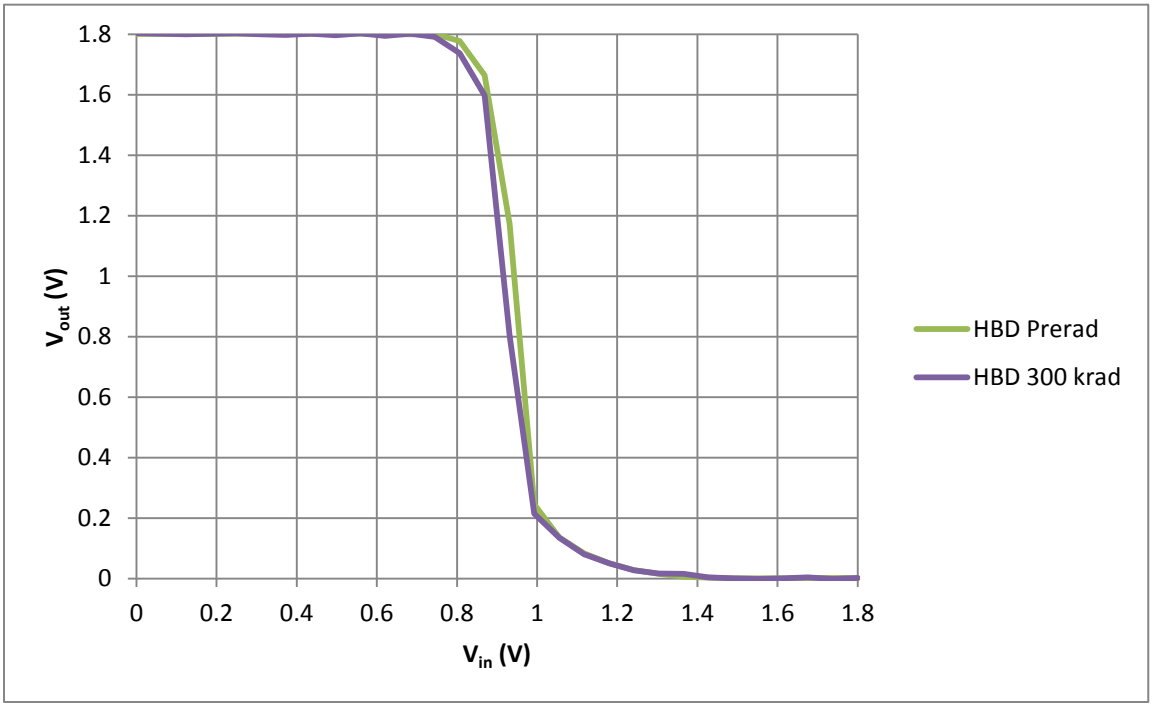

Figure 36 – TID effects on the HBD inverter transfer function.

4.2.2 The Discrete NFET V_{GS} vs. I_D Curves

The de-lidded discrete NFET curves over TID are shown in Figure 37. The V_D for these tests was 50 mV. The area of interest is the subthreshold leakage for $V_{GS} < 0$ V. As TID increases this leakage increases as the STI sidewall traps positive charge and begins to invert the parasitic leakage transistor. However, there appears to be a saturation point; above 150 krad, there is no substantial increase in leakage current. This is verified in Figure 38, where the leakage current at $V_{GS} = -1.8$ V is plotted over TID. The curve shape represents a crude transistor V_{GS} vs. I_D curve. The charge trapped in the STI sidewall is proportional to TID, so the effective gate voltage of the parasitic transistor is also proportional to TID.

This saturation effect is an important result. Even at 300 krad, there is less than 0.1 μA of leakage current. This may pose problems in large digital systems with a high number of gates. This would place a higher load than normal on any regulated supply and could cause system failure. However, this level of leakage current will not cause the output of a single gate to fail. The PMOS transistor in a CMOS circuit easily supplies the current necessary to maintain a logic 'high' output. This correlates with the small changes seen in the inverter transfer functions.

It is important to note that the tests performed above with a $V_D = 50$ mV do not accurately represent the NFET operating in a CMOS circuit. For this to be the case, $V_D = 1.8$ V. The lidded component was tested at both $V_D = 50$ mV and $V_D = 1.8$ V (Figure 39). One important result here is the *reduced* leakage current for $V_D = 1.8$ V at 150 krad for $V_{GS} = -1.8$ V versus for $V_{GS} = 0$ V. The subthreshold hump is clearly visible on this curve as seen previously in Figure 9. This indicates that applying a negative V_{GS} does aid in reducing leakage current in thin-gate oxide devices. It was unknown whether these thin-gate oxide devices would respond to a negative V_{GS} or if they would need a negative V_{GB} to more fully turn off. It should be noted that it is unknown why the initial, pre-irradiation leakage current is higher in the $V_D = 1.8$ V versus the $V_D = 50$ mV run. In addition, the lidded device was only tested to 150 krad, so results above this dosage are unknown.

Figure 40 shows a comparison of the de-lidded and lidded part. As shown, there is a difference in leakage current at 100 krad. This difference is likely due to inaccurate dose rate measurements of the lidded part. As mentioned in section 3.3.3.2, the socket needed to be tilted to achieve the highest dose rate. It is likely the angle set when calibrating was not the same as when the test board's actual measurements were being made.

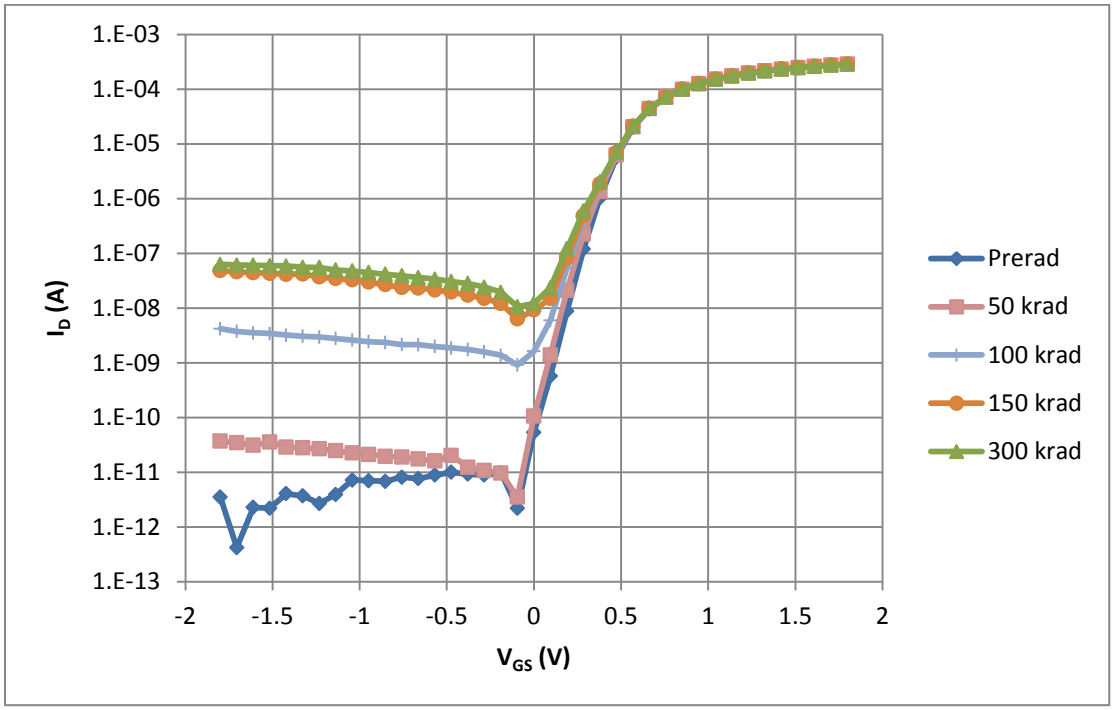

Figure 37 - I_D vs. V_{GS} curves over TID of IBM 7WL 180nm NFET.

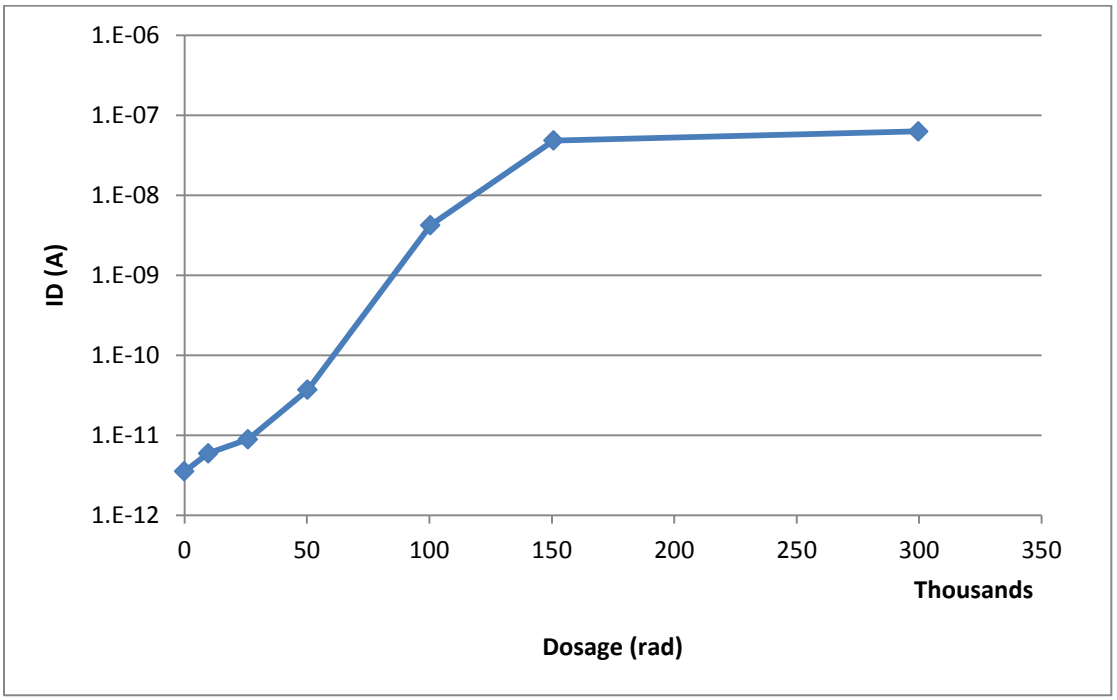

Figure 38 - Leakage current vs. dosage for Vs = 1.8 V.

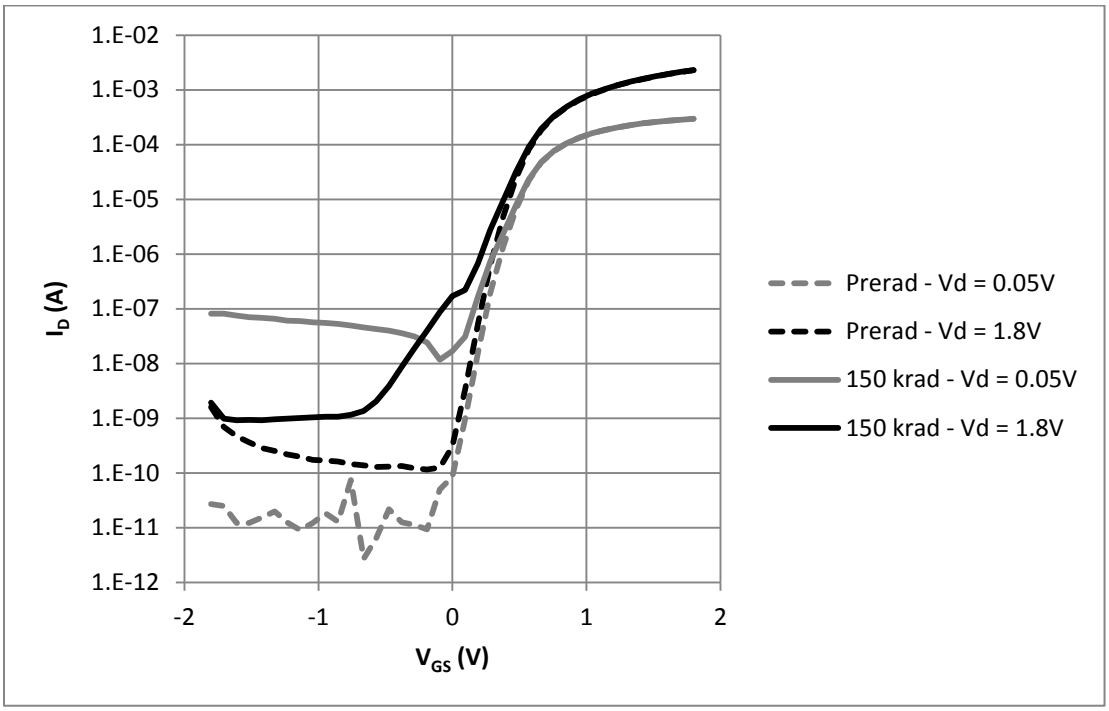

Figure 39 - I_D vs. V_{GS} curves comparing different V_D voltages at two TID levels.

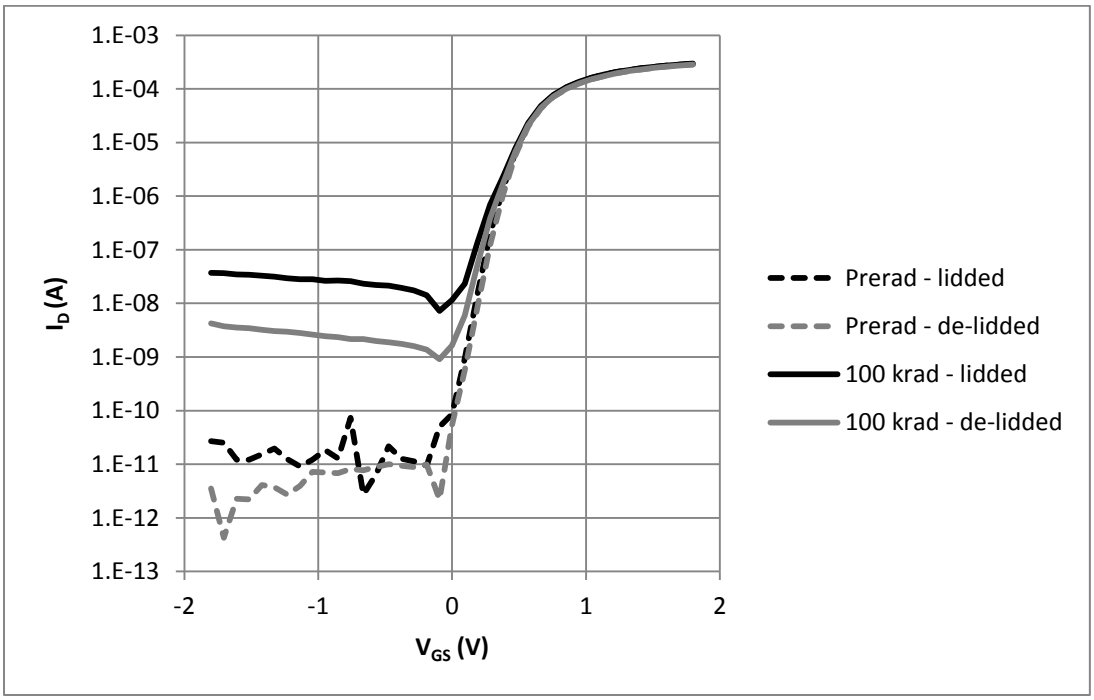

Figure 40 - I_D vs. V_{GS} curves comparing the lidded and de-lidded parts.

4.2.3 The Ring Oscillator's Total Dose and Dose Rate Performance

The ring oscillators were tested to 300 krad at approximately room temperature. The non-HBD and HBD ring oscillators' pre-irradiated and 300 krad oscilloscope waveforms are shown in Figure 41 and Figure 42. The pre-irradiated, non-HBD ring oscillator is oscillating at 19.041 MHz and the HBD is oscillating at 8.929 MHz. Recall, this frequency has been divided down from the actual ring oscillator's frequency. Extracted simulations showed the HBD ring oscillator to be approximately 53.8 % slower than the non-HBD version. These laboratory measurements indicate the HBD ring oscillator to be 53.1 % slower (very close to simulated values).

Upon initial inspection, there appears to be no difference between the pre- and post-irradiated ring oscillator waveforms for either the HBD or the non-HBD version. Closer inspection as indicated by the arrows shows there is a slight increase in oscillating frequency for the irradiated oscillators. These changes are slight; however, they were repeatable. The temperature of the room was not accurately measured throughout the testing, so changes in temperature could have had this effect on oscillating frequency. However, intuition says the chips would get hotter during irradiation from waste heat being generated in the room from the X-ray's power supply. The effect of this would be a decrease in oscillating frequency (the MOSFETs drive capability drops as temperature increases). The increase in frequency was measured to be 0.103 % in the non-HBD version and 0.0524 % in the HBD version. By normalizing these to the oscillating frequency, they become nearly equal. Thus, it is decided the HBD technique plays no role in hardening the ring oscillator from TID-induced frequency changes. The cause of these changes is unknown.

Figure 43 and Figure 44 display the pre-irradiated and the during-irradiation non-HBD and HBD ring oscillator waveforms. The dose rate for these tests was 5 krad/min with no dose accumulated. There are no apparent changes in operation of either the HBD or the non-HBD ring oscillator. These tests were also performed at 100 krad of accumulated dose and showed the expected increase in oscillating frequency. These tests show the TID effects on the thin-gate oxide devices are minimal.

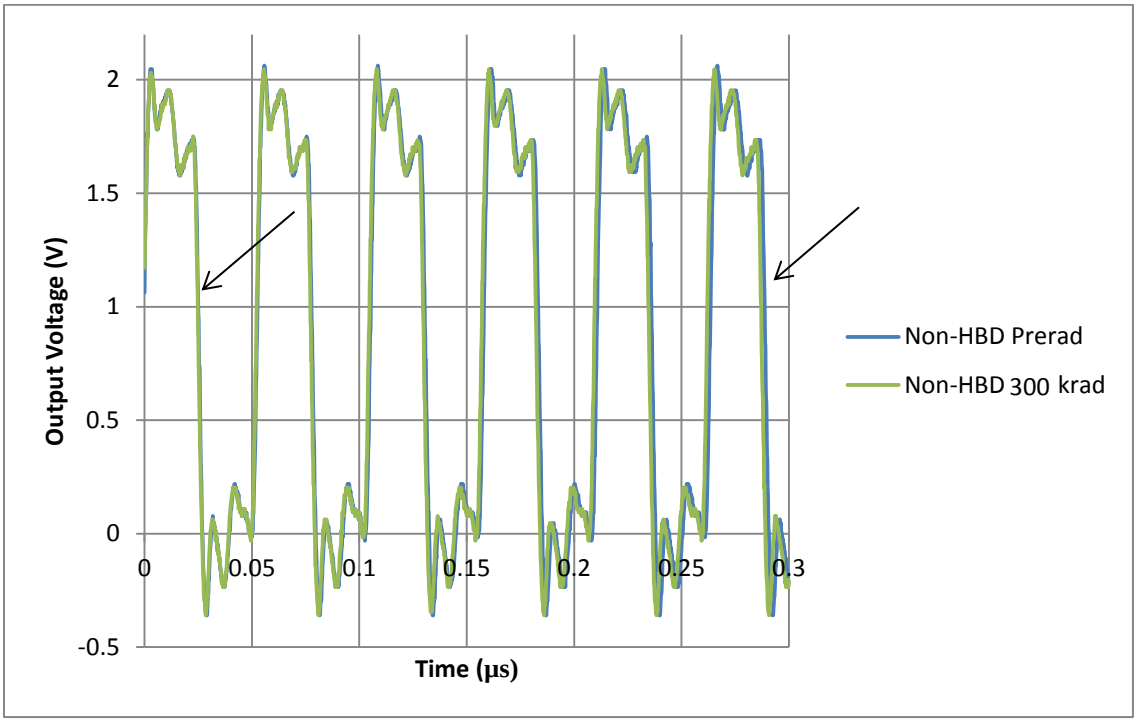

Figure 41 - Oscilloscope capture showing TID results for non-HBD ring oscillator.

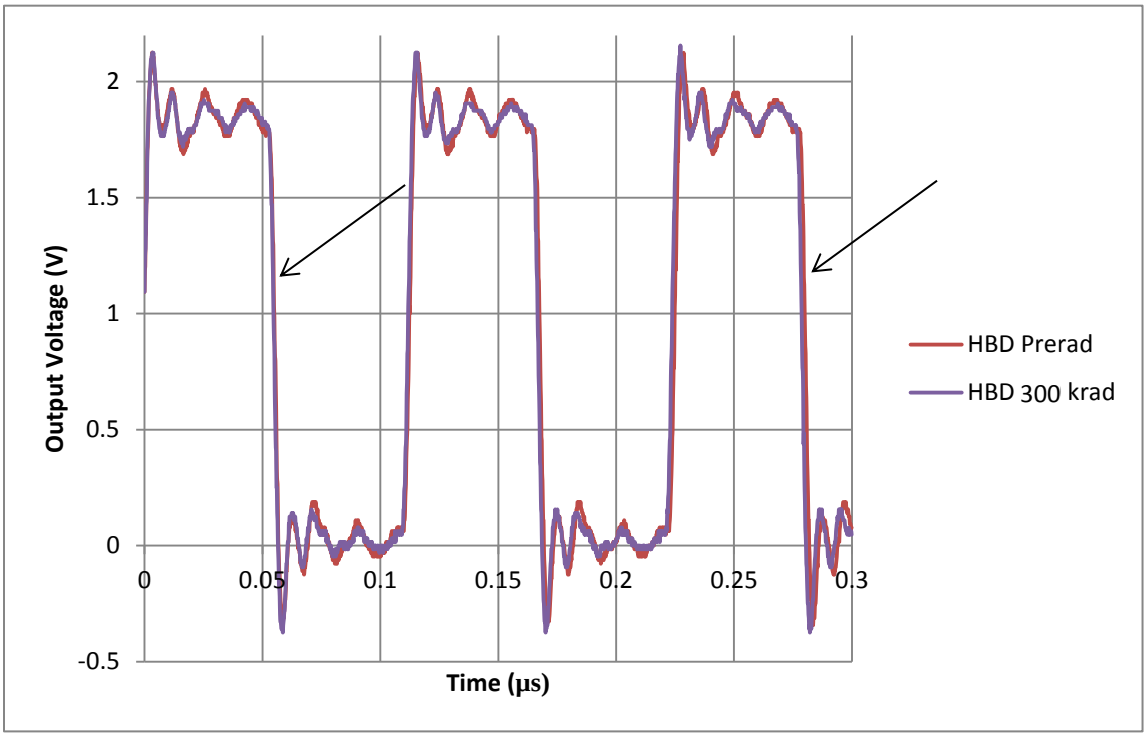

Figure 42 – Oscilloscope capture showing TID results for HBD ring oscillator.

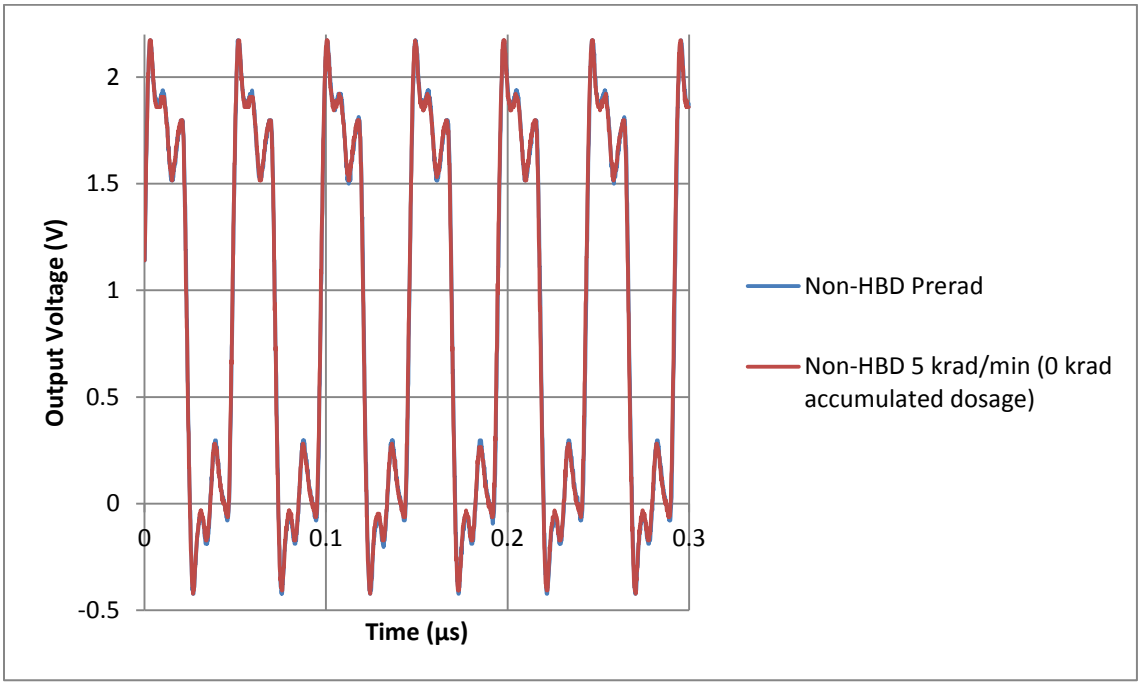

Figure 43 – Oscilloscope capture showing dose rate results for non-HBD ring oscillator.

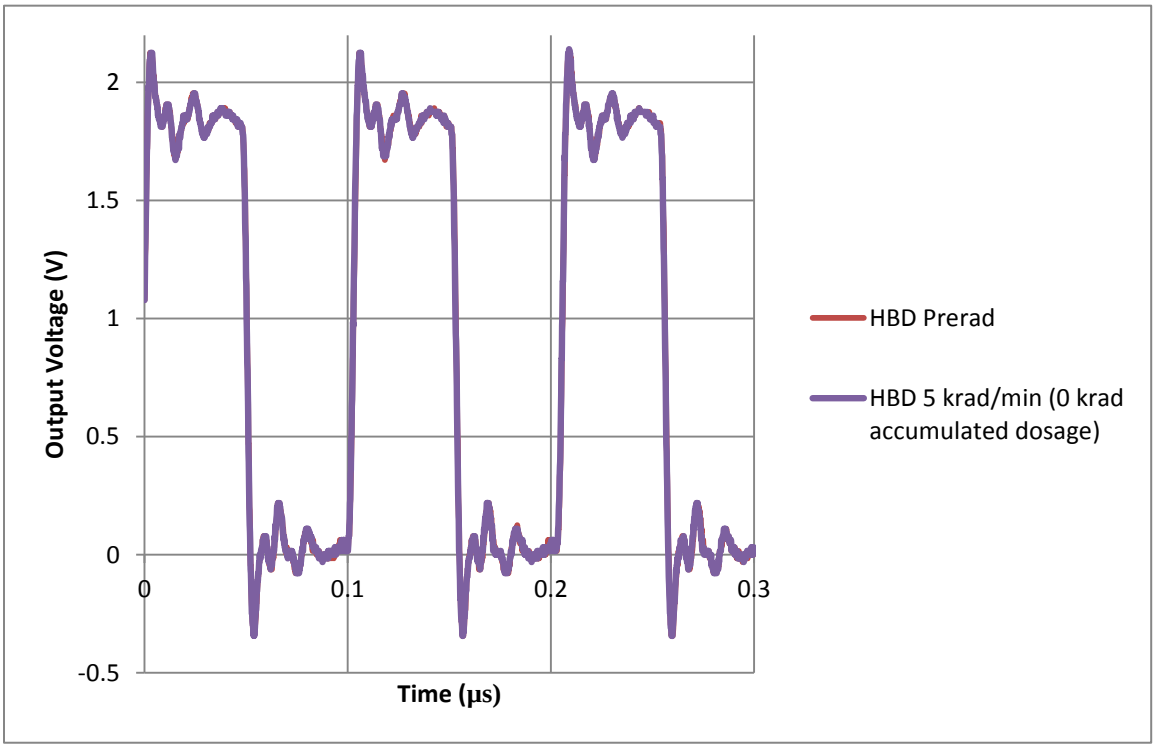

Figure 44 – Oscilloscope capture showing dose rate results for HBD ring oscillator.

4.2.4 The Non-HBD and HBD PFD Comparison

The PFDs were tested to observe any functional or speed differences while using the inverted-source technique under nominal (i.e. non-irradiated) conditions. Figure 45 shows an oscilloscope capture of the non-HBD and HBD in operation. The signals shown are the two UP signals. The input signals are at 20 MHz and in-phase. Recall, the output signals are proportional to the difference between the phases of the input signals. Since the phase of the input signals is zero, one might expect the output to be zero. However, this is a zero-deadzone PFD, so the PFD has a built-in delay in the feedback loop to reset itself. Even if the signals are in-phase, the outputs (both UP and DOWN) will be asserted for a short time while the signal propagates to the reset. This allows the PFD to distinguish effectively between small phase errors in the signal and reduces jitter in the PLL.

The PFD has a characteristic duty cycle when the signals are in-phase. The non-HBD PFD has a duty cycle of 3.8 % and the HBD PFD has one of 7.4 %. Recall, the non-HBD PFD's delay was created with four long device length inverters and the HBD's with two long device length inverters. The fact that the non-HBD PFD still has a smaller duty cycle indicates that there must be some other delay. It is thought the delay within the D-flip-flop itself (Figure 29) is large enough to significantly contribute to the added delay. This difference will reduce the detection range of the HBD PFD. Proper frequency detection will occur only for an input signal whose period is less than twice the delay [23]. The non-HBD PFD has a delay of 1.9 ns while the HBD PFD has a delay of 3.7 ns. Therefore, the maximum detectable frequencies are 263 MHz and 135 MHz respectively. The PLL loop itself was designed for a maximum reference frequency of 40 MHz, so this added delay should pose no functional issues for the PLL as a whole. In addition, the HBD PFD could be designed with even less feedback delay to bring its performance closer to the non-HBD PFD. Other than this, there are not any visible differences between the HBD and non-HBD PFD. The HBD PFD has been successfully implemented in the frequency synthesizer described earlier.

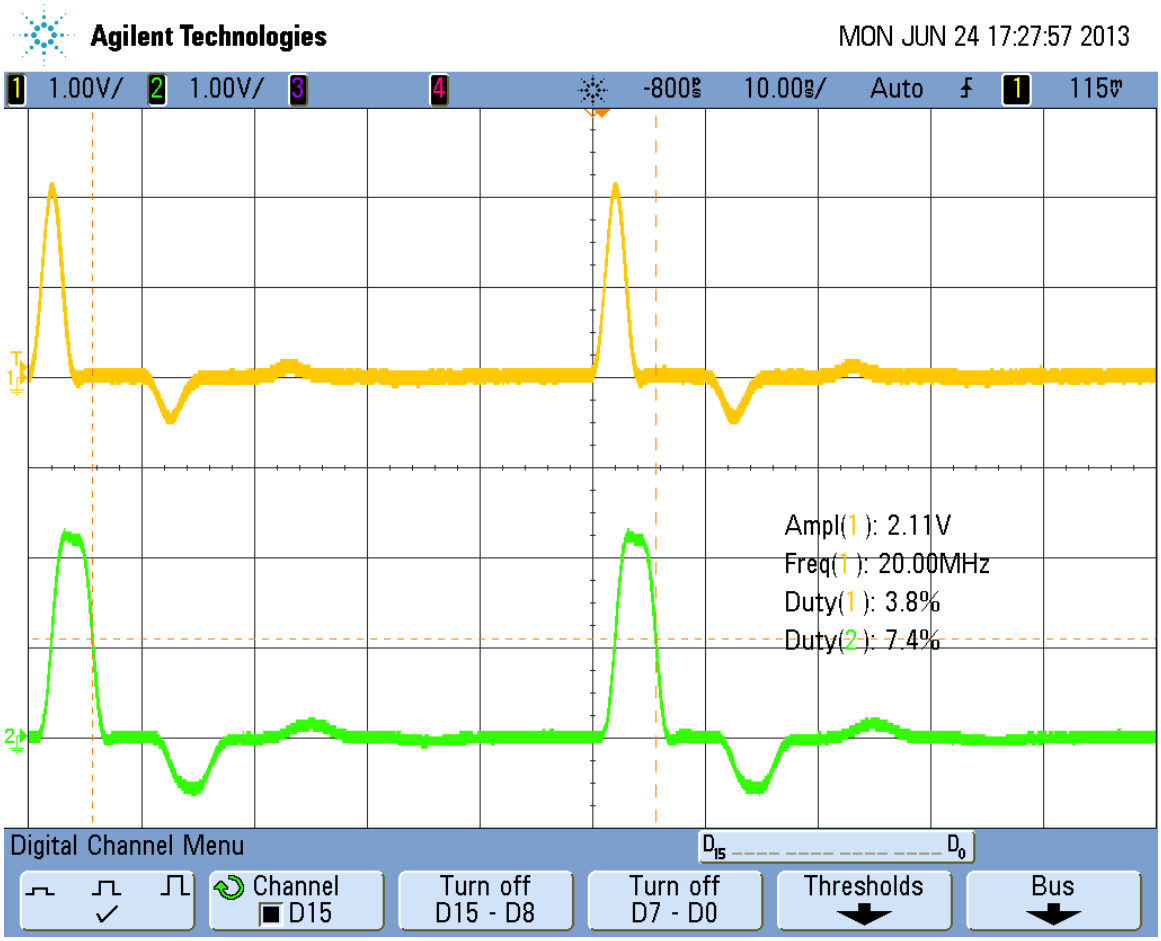

Figure 45 - Non-HBD (top) and HBD (bottom) PFD operating with zero phase difference between inputs.

4.3 Results Summary

Table 2 - CMOS inverters' results.

CMOS Inverters	Switch Point Change (ΔV_{SW})	Layout Area
Standard – ALD1106/1107	**1.5 V (60 krad)**	**1X**
HBD – ALD1106/1107	**1.2 V (−20%) (60 krad)**	**2X (+100%)**
Standard – 1.8 V 7WL	**0.4 V (300 krad)**	**33.15 µm^2**
HBD – 1.8 V 7WL	**0.3 V (~−20%) (300 krad)**	**54.35 µm^2 (+64.0%)**

Table 3 - Discrete NFETs' results.

		Leakage Current ($V_D = V_{DD}$)	
Device	Dosage (krad)	$V_{GS} = 0$ V	$V_{GS} = -V_{DD}$
ALD1106	**0**	**< 10 pA**	**< 10 pA**
	60	**0.352 mA**	**< 10 pA**
1.8 V NFET, W = 2 µm, L = 180 nm, gate fingers = 2	**0**	**200 pA**	**2 nA**
	150	**0.2 µA**	**2 nA**

Table 4 - Ring oscillators' results.

1.8 V 7WL Ring Oscillator	Dosage (krad)	Frequency (MHz)	Layout Area (μm^2)
Standard	**0**	**19.041**	**2277**
	300	**19.061 (+0.103%)**	
HBD	**0**	**8.929 (−53.1%)**	**3644 (+60%)**
	300	**8.934 (+0.0542%)**	

Table 5 - PFDs' results.

PFD	Max Frequency (MHz)	Layout Area (μm^2)
Standard	**263**	**1625**
HBD	**135 (−48.7%)**	**2282 (+40.4%)**

CHAPTER 5: CONCLUSIONS AND RECOMMENDATIONS

The inverted-source HBD technique (as presented in [1]) has been experimentally tested with thick-gate oxide MOSFET devices (ALD1106/ALD1107) and thin-gate oxide devices (1.8-V devices in the IBM 7WL BiCMOS process). The results indicate the HBD technique effectively doubles the radiation tolerance of thick-gate oxide devices with the cost of double the number of ICs and a slightly larger than 2X speed penalty.

The HBD technique provided some TID immunity to the tested thin-gate oxide devices, but it was shown to be unnecessary because of the inherent hardness of the devices in CMOS logic. This is believed to be because of the different TID leakage mechanism in thin-gate oxide NMOS devices (NFETs). Thick-gate oxide NFETs experience a negative threshold voltage shift because of trapped positive charge in the gate oxide. Thin-gate oxide NFETs do not trap as much charge in the gate oxide. They do trap charge in the shallow trench oxide (STI) abutting the channel between drain and source. This charge inverts the channel and causes leakage current. However, this leakage current must be about $1/10^{th}$ of the on-current of the PMOS device in a typical CMOS inverter for the noise margins of the digital circuit to be reduced. The leakage current in the tested NFET was shown to saturate around four orders of magnitude less than the NMOS on-current. Therefore, the 1.8-V CMOS digital circuits in the 7WL process are shown to be relatively immune to the leakage effects caused by TID, at least for the dose levels considered in this work.

There are a few different hardening mechanisms at work in the inverted-source HBD technique in the tested thin-gate oxide devices. Surprisingly, the NFET displayed some control over the drain current for $V_{GS} < 0$ V. By applying a negative V_{GS} the leakage current can be reduced. Another mechanism comes from simply having two NMOS devices in series to ground, which doubles the leakage resistance. Also, the PMOS of the hardening inverter supplies current to help maintain the source voltage on the output NMOS, reducing the voltage drop from drain to source in this transistor (further reducing leakage current). Table 6 summarizes the gains in TID hardness and

the performance degradations introduced by the HBD technique for the two processes with the annular gate NFET as a reference for comparison.

Table 6 - Inverted-source HBD technique performance comparison.

	TID Leakage Hardness	**Speed Penalty**	**Power Penalty**	**Layout Area Penalty**	**Implementation Difficulty**
Std. Thick-Gate Oxide	Bad	-	-	-	Easy
HBD Thick-Gate Oxide	Moderate	2X	2X	2X	Moderate
Std. Thin-Gate Oxide	Good	-	-	-	Easy
HBD Thin-Gate Oxide	Good	2.16X	2X	1.6X	Moderate
Annular Thin-Gate Oxide[1]	Excellent	1.25X	2X	1.7X	Difficult

[1] As described in Figure 17 of [6].

Finally, it is believed the inverted-source technique is a viable option for thick-gate oxide devices (>20 nm). In addition, it is concluded the IBM 7WL BiCMOS process is radiation-tolerant for CMOS circuits in standard, non-HBD configurations. If added leakage current will place a large strain on the voltage regulator due to excessive current draw, annular gate NFETs should be sought. Through the literature review, wide variation in MOSFET response to TID was seen. It is important to note that these conclusions do not apply to other processes, especially deep sub-micron processes where TID effects are different.

Seeing the HBD's hardening mechanism in thin-gate oxide devices did spur some other ideas for increasing the TID hardness of these kinds of devices. First, in CMOS device matching if a longer NMOS device can be used to slow the NMOS instead of using a wider PMOS, the leakage channel in the NMOS is increased in length. This increases the leakage resistance therefore reducing static power draw in CMOS circuits. In addition, NAND gates should be used in place of NOR logic gates. A two input NAND logic gate can potentially have four times less static power draw than a two input NOR gate. Therefore, to achieve power savings, the number of NAND gates replacing a single NOR gate should be less than four. For example, the PFD designed in this thesis implements NOR gate D flip-flops. By designing it with NAND gate D flip-flops static current draw in TID environments could be reduced.

Future work using the inverted-source technique could involve investigating the effect of substrate biasing on TID immunity as in [16]. In this same vein, analyzing both the I_D vs. V_{GS} and the I_D vs. V_{GB} curves for an NFET would be enlightening. In addition, the inverted-source technique could be investigated in 3.3 V or 5 V I/O devices. Finally, a thin-gate oxide NFET could be irradiated and then the TID effects could be fitted to simulation models in order to simulate TID effects on a digital system before fabrication. This evaluation could help determine the necessity of annular gate devices in these digital systems.

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APPENDICES

A.1 The Test Boards

Pictures of the test boards used in this thesis are shown in Figure 46 through Figure 50. Figure 46 shows the test board implementing the two test circuits for the ALD1106/1107 thick-gate oxide MOSFETs. The board is a four-layer FR4 printed circuit board (PCB) designed in the Eagle PCB CAD software. The inner layers are V_{DD} and ground; bypass capacitors are used between these two nodes to lower noise from the supply. Most of the connections to exterior devices are made through banana plugs, because the measurements are at DC frequency and banana plug cables are cheap and easy to make any custom length. The top half of the board allows the I_D vs. V_{GS} test to be performed, and the bottom portion enables the inverter DC transfer functions to be captured. The Co-60 source used during radiation testing can be physically approximated as a line source of radiation; therefore, to ensure even dosage the ALD1106 and ALD1107 are horizontally centered on the board.

The test boards for the 7WL *Cappadocia* chip are shown in Figure 47 and Figure 48. They are both four-layer FR4 boards designed with the KiCAD electronic design automation (EDA) software. KiCAD is free and open-source as opposed to the Eagle PCB software. The author found the KiCAD software to be slightly more intuitive than Eagle. However, back-annotation is allowed meaning connections/parts not found in the schematic may be added to the board view. This allows mistakes to crop up more easily in the board design. The adventurous designer is encouraged to investigate the KiCAD suite further, however the Eagle software is adequate and will not let the designer make some mistakes. A brief tutorial for KiCAD may be found in [26] and an excellent online component symbol generator may be found in [27].

The bias board for *Cappadocia* is shown in Figure 47. This board generates the voltage supplies, bias currents and control pins for the daughter card. Figure 48 shows the daughter card that houses the *Cappadocia* chip. This board accepts the inputs from the bias board and provides input and output capabilities for the signals on the chip. The outputs for the test inverters and ring oscillators are shown along the bottom of the board.

Figure 49 and Figure 50 show the bias board and one of the daughter cards for the *Archelais* chips, respectively. They are both four-layer FR4 boards designed in Eagle.

As with the *Cappadocia* bias board, the *Archelais* bias board provides voltage supplies, bias currents and DC control signals to the daughter card. The daughter card accepts these inputs and has inputs and outputs for the signals on-chip.

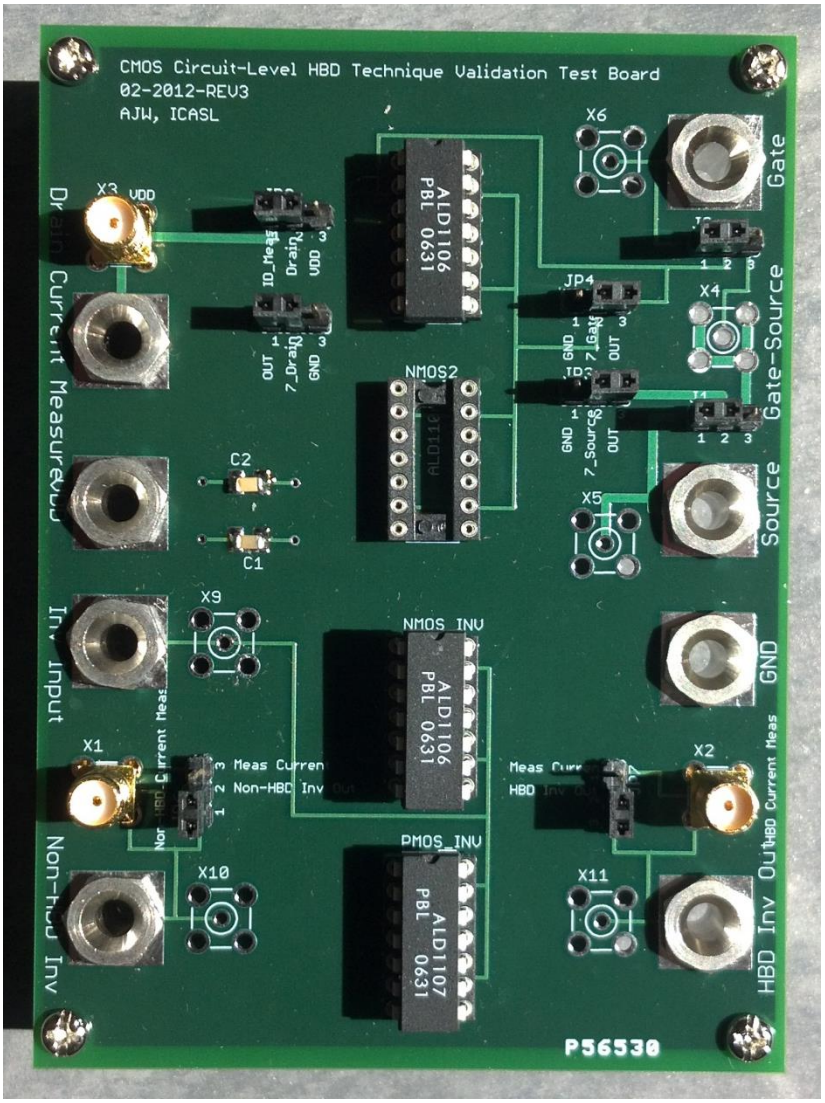

Figure 46 – Test board used for radiation testing of ALD1106 and ALD1107.

Figure 47 - Bias board for Cappadocia chips.

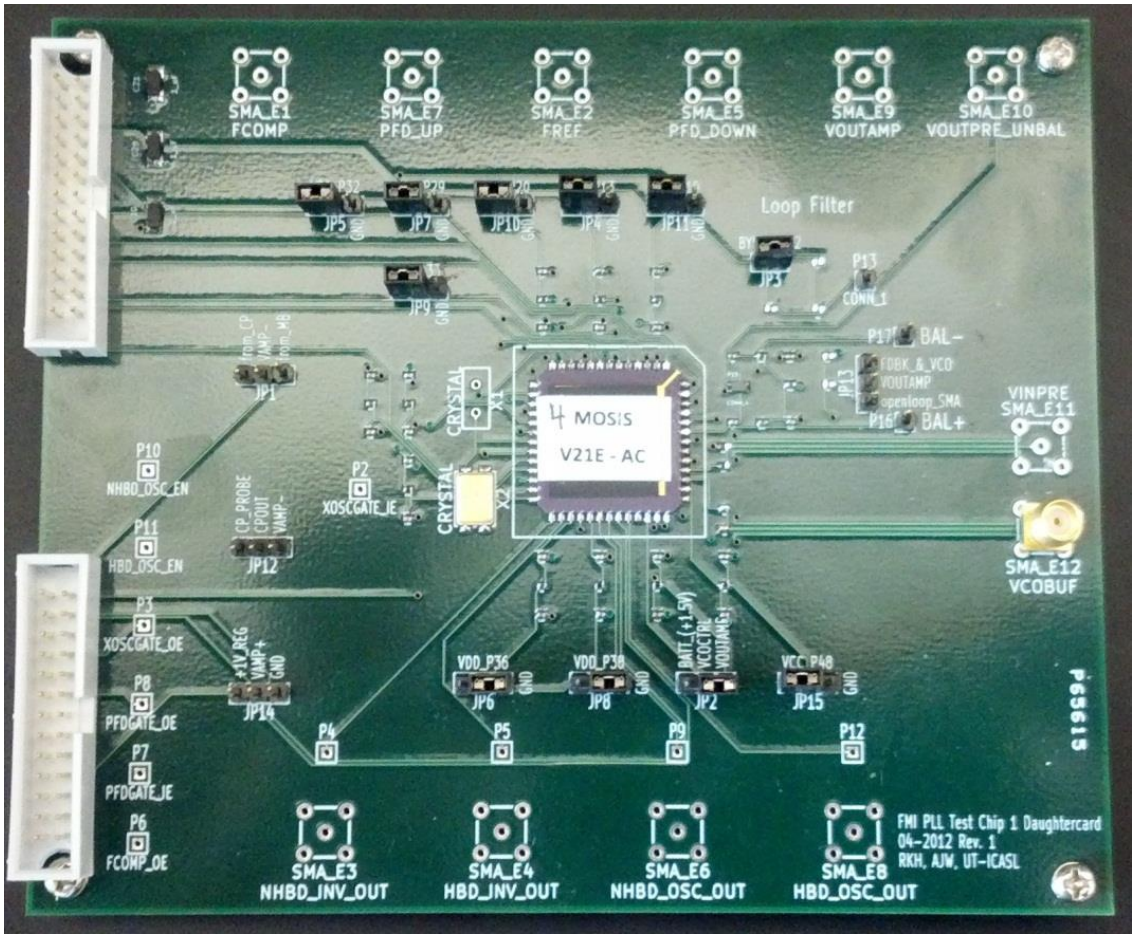

Figure 48 - Daughter card housing Cappadocia chips. Inverter and ring oscillator outputs are along the bottom of the board.

Figure 49 - Bias board for Archelais chips.

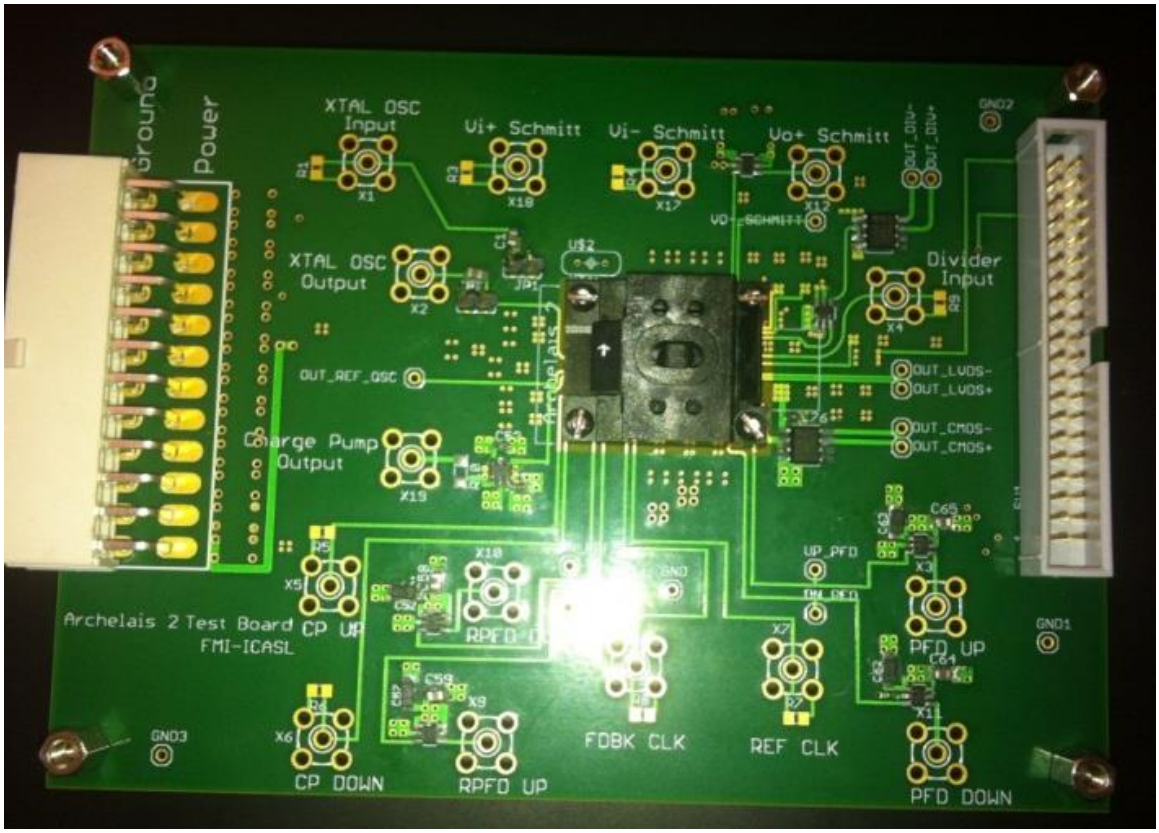

Figure 50 - Daughter card for Archelais chips.

A.2 The LabVIEW Virtual Instruments (VIs)

LabVIEW is a powerful, icon-based programming language developed for PCs by National Instruments (NI). It was used to collect the measurement data during irradiation. LabVIEW was chosen for a number of reasons over other data collection methods. First, the ICASL lab has LabVIEW licenses and instruments manufactured by NI (NI PXIe-1062Q) that are directly compatible with LabVIEW through prebuilt virtual instruments (VIs). Second, nearly all of the non-NI equipment available in the lab has a GPIB connection for the PC and have basic VIs already written to control them. These prebuilt VIs should not be underestimated; they function as building blocks for the users own VIs. Third, Jeremy Brantley, a recent ICASL graduate, has much LabVIEW experience and graciously provided assistance with debugging as needed. Fourth, there are numerous resources and tutorials available online for learning LabVIEW. In particular [28] introduces LabVIEW giving the reader a good grasp on the fundamental philosophy behind the icon-based programming language. In addition, Jeremy's thesis describes many of the basic building blocks commonly used in measurement sweep VIs [29]. In summary, there is great foundation made available in the lab to create functional programs in LabVIEW quickly.

A VI consists of the front panel or GUI interface that allows the user to control the VI and the block diagram that uses icons to define how the program works. The icons are connected together with wires that define how data flows between them. The VI for the *Cappadocia* chip testing is shown in Figure 51 (front panel) and Figure 52 (partial block diagram). In Figure 51, buttons and text fields allow the user to control the program. For example pressing the "Bias Board Input Voltage" button will turn on a power supply connected to the *Cappadocia* bias board. There are also various outputs; for example, once the bias board is powered, the voltage and current are monitored through a numeric indicator and real-time updating chart respectively.

In Figure 52, a partial view of the block diagram is shown. Program execution occurs from left to right in this VI. The instruments are defined on the left side: the power supply, two analog inputs and one analog output. The analog output is tied to the

inverter inputs and the analog inputs are tied to the same HBD and non-HBD inverter outputs.

The center of the image contains an event structure nested within a while loop. The event structure is similar to a case statement in that there are many different cases/events possible but only one is executed at a time. Its advantage over a case statement or an equivalent for loop is that it does not constantly need to poll the GUI interface for changes, saving CPU cycles. The event shown in the image is "'Bias for Irradiation': Value Change"; when the "Bias for Irradiation" button is pressed, the program executes the subVIs shown inside the event structure box. In this case, nothing occurs with the power supply so its data is passed through the event unchanged. The input to the inverters should be 1.8 V. To accomplish this, the "NewVal" Boolean for the event ('true' if the button is pressed and 'false' when it is pressed again) is used. It is converted to a binary number (either '1' or '0'), multiplied by 1.8 and then fed to the analog output's value.

SubVIs on the right side of the image ensure the instruments are properly closed and turned-off after program execution. However, the program would not be very useful if only one event was executed and the program closed. This is where the while loop comes into play; the event structure is continuously executed by the while loop until the while loop is closed by pressing the stop button (this button press represents another event and has its own event case to close the while loop).

It is hoped that this appendix has provided a clear picture of the testing automation methodology used in the thesis. As mentioned previously, [28] and [29] are both good resources for the novice LabVIEW programmer.

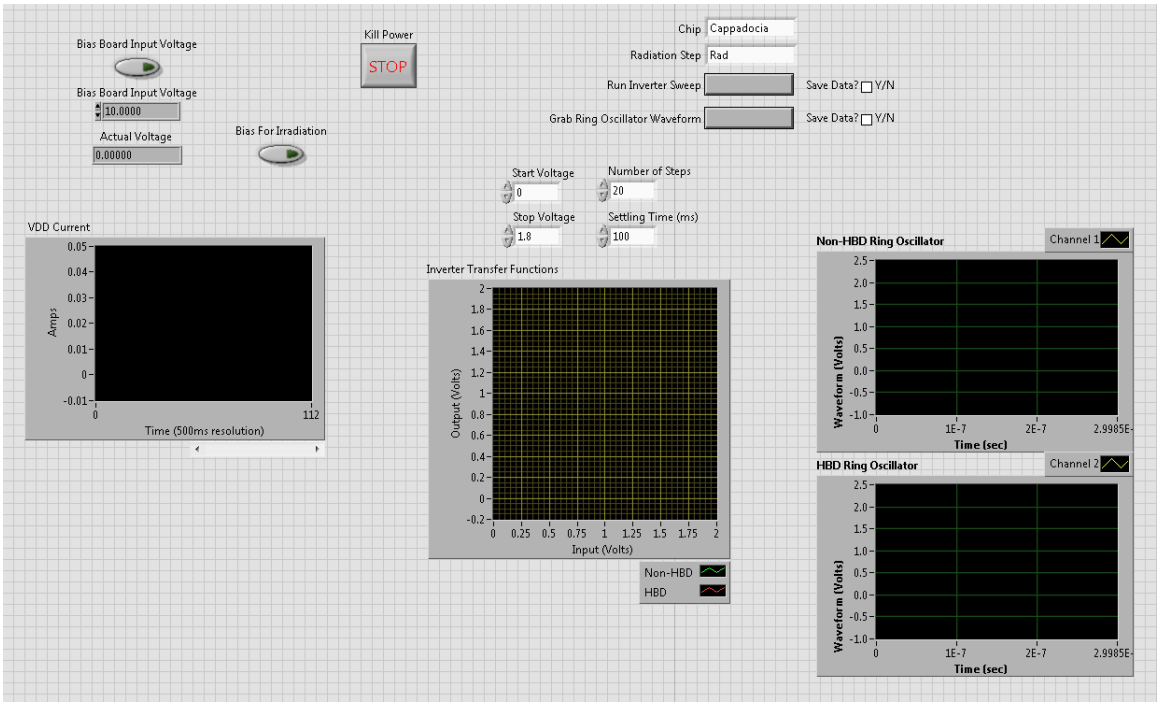

Figure 51 - LabVIEW front panel for Cappadocia testing.

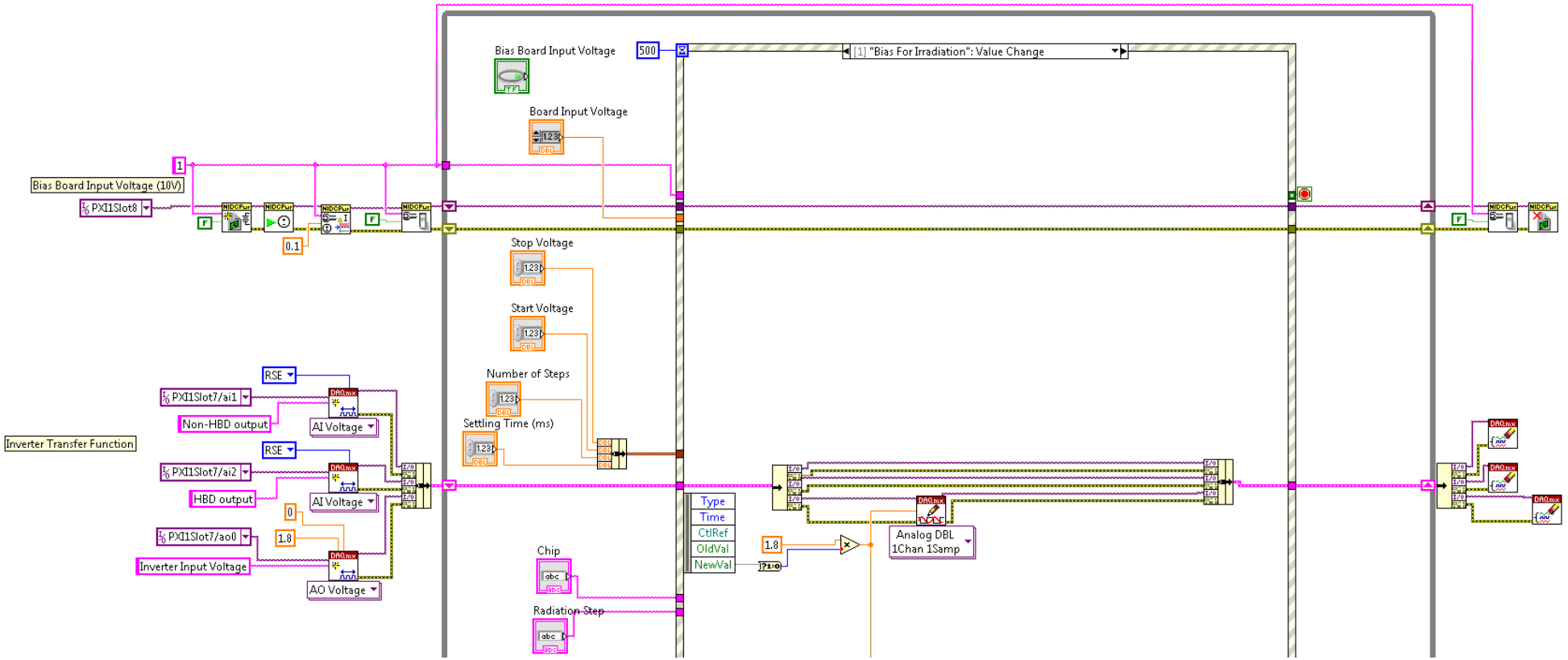

Figure 52 - Partial block diagram for Cappadocia testing in LabVIEW.

VITA

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