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Design of a 5-V Compatible Rail-to-Rail Input/Output Operational Amplifier in 3.3-V SOI CMOS for Wide Temperature Range Operation

Robert Lee Greenwell
University of Tennessee - Knoxville

To the Graduate Council:

I am submitting herewith a thesis written by Robert Lee Greenwell entitled "Design of a 5-V Compatible Rail-to-Rail Input/Output Operational Amplifier in 3.3-V SOI CMOS for Wide Temperature Range Operation." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Benjamin J. Blalock, Major Professor

We have read this thesis and recommend its acceptance:

Syed K. Islam, M. Nance Ericson

Accepted for the Council:
Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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Linda Painter
Interim Dean of the Graduate School

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DESIGN OF A 5-V COMPATIBLE RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIER IN 3.3-V SOI CMOS FOR WIDE TEMPERATURE RANGE OPERATION

A Thesis Presented for the

Master of Science Degree

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Robert Lee Greenwell II

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Finally, I would like to thank my family and friends who have been very supportive while I completed my master's degree. I would especially like to thank my father, who has always been there.

ABSTRACT

This thesis presents the design and implementation of a 5-V compatible operational amplifier in a 3.3-V technology capable of accepting rail-to-rail inputs, providing a rail-to-rail output swing and wide temperature range operation. The major system components consist of a fully-differential input (gain) stage and an output (driver) stage, with protection and bias circuitry components. The op amp is biased by a constant inversion coefficient current reference to optimize its performance over temperature. Measured results demonstrate the functionality of the design, which has been fabricated in a 0.35-μm, partially-depleted silicon-on-insulator (PDSOI) CMOS process.

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CHAPTER 1

INTRODUCTION AND OVERVIEW

Introduction

The exploration of our solar system has been largely accomplished through the use of probes sent into space and to the surface of our neighboring planets. Operating electronics in these environments requires components capable of functioning reliably in the extreme temperatures these locations present. The parts destined to operate in these conditions require extensive design review and operational testing. Therefore, multipurpose components designed to operate in a range of environments can save extensive amounts of time in the design and verification of systems destined for such environments.

Considerations for such designs include the lifespan of the component, in terms of operational lifespan as well as manufacturing lifespan. As CMOS device scaling continues and the benefits, such as increased speed and decreased chip area, are reaped, design concerns also arise. For example, decreases in supply voltage from device scaling can lead to new components that require interface circuitry to buffer their input/output signals if used in a system that operates at a higher voltage level than a given technology supports. Despite this additional design overhead, designs in a more recent, and consequently lower-voltage technology, may be considered more "future-proof" as older fabrication technologies are phased out.

Some of the chief limitations that restrict the voltage for a MOS device include gate oxide breakdown due to high V_{GS} and hot carrier effects brought about by excessive V_{DS} [1]. The breakdown of the gate oxide, which can be attributed to stresses placed on the gate owing to high gate voltages and inherent oxide defects, among other factors, manifests itself as a leakage path from the gate to the body of the transistor. Hot carrier effects are brought about by large V_{DS} voltage creating strong electric fields that accelerate carriers in the channel, which then collide with lattice atoms. The resulting electron-hole pairs are then swept away, some penetrating the gate oxide and becoming trapped. This can shift the threshold voltage and transconductance of the device, as well as increase the substrate (body) current.

There are several options available to combat these issues. One of the simplest is to have external circuitry, whether utilizing commercial off-the-shelf (COTS) components or another integrated circuit (IC), to serve as an appropriate voltage level shifting interface to the circuitry of a desired chip or technology. Drawbacks to this approach are the additional on-board space required for the components and increased power requirements, which is an obvious problem for applications where size and weight are an important factor. Other options include utilizing technology specific solutions, such as fabrication methods that can incorporate multiple oxide thicknesses, allowing for different performance and voltage tolerance characteristics on a single substrate. However, this obviously adds additional cost and time to the design and fabrication overhead of a project.

Another approach is to design components and systems that are capable of withstanding higher voltage levels by designing circuitry with built-in protection which

shields transistors and other susceptible components from excessive voltage levels. Benefits of this approach are that no special (added cost) fabrication steps are needed and no supplementary external components are necessary.

The wide temperature range that circuits in the extreme environments of space may be exposed to leads to additional design constraints. Over a large temperature range the performance characteristics of MOS devices vary considerably. This is magnified as the voltage protection circuitry must provide sufficient protection as transistor parameters, such V_{TH} and mobility, vary across temperature.

Overview

This thesis presents the design and implementation of a 5-V compatible operational amplifier in a 3.3-V PDSOI technology, designed to operate from −180˚C to 120˚C. The amplifier is comprised of a fully-differential input gain stage, single-ended output driver stage, and current reference for biasing. Wide temperature range operation is made possible with the use of a constant inversion coefficient current reference.

This thesis is divided into four sections. Chapter 2 contains a review of the challenges inherent in developing 5-V compatible circuits in a 3.3-V technology. These issues include V_{GS}, V_{DS}, and V_{GD} voltage limitations. Also included in this chapter is an overview of the top-level amplifier including design considerations, methodology, and topology.

Chapter 3 presents a comprehensive analysis of the design of the 5-V amplifier. Starting with the general architecture and circuit topology, the implementation of the

voltage protection devices is then demonstrated. Simulation results are also presented. Basic design equations are located in the Appendix.

Chapter 4 presents the measured results for the amplifier and describes the test systems used.

Chapter 5 presents conclusions for this work as well as a discussion on future work.

CHAPTER 2

DESIGN OVERVIEW

Design Constraints

The design of 5-V compatible circuitry in a 3.3-V process requires that precautions be taken to shield devices against excessive voltage levels. The 0.35-µm PDSOI process utilized for this amplifier stipulates that for long-term reliability no transistor can be exposed to a V_{DS} or V_{GS} greater than 3.6-V. The same constraints must also be applied to V_{GD} to maintain long-term reliability. The design specifications for this amplifier require that it be capable of safely functioning while utilizing a power rail voltage that may vary ±10% from a nominal 5-V supply. Thus, in an inappropriately designed circuit, an unprotected device could be exposed to voltages of 5.5 V, this translates to 1.9 V over the process voltage specification.

Excessive V_{GS} on any given transistor may lead to the breakdown of the gate oxide. This oxide breakdown is caused by excessive electric fields created by the potential difference between the gate and the source and body terminals of a transistor. To a lesser extent, a large potential difference between the gate and drain terminals can cause oxide breakdown where the gate oxide overlaps the drain. When the field's potential becomes large enough, electrons will begin burrowing through the gate oxide, particularly if there are already inherent defects in the structure, creating resistive

connections between the gate and channel. This event causes permanent damage to the device [1][2].

For a 3.3-V process, typically a V_{DS} above 3.6 V may cause a device to exhibit hot-carrier effects. In general, hot carriers occur when a high voltage potential is applied to the drain, which creates a large drain-to-source electric field. This electric field accelerates the carriers in the channel into the depletion region. Some of these hot carriers collide with atoms in the silicon lattice, depositing energy and causing electrons and holes to scatter. This is referred to as impact ionization. Occasionally, the energy deposited in the ejected electron or hole allows it to overcome the electric potential across the gate, and becomes embedded in the oxide, called hot-carrier injection. Over time, this effect can shift the threshold voltage and transconductance of the transistor, significantly affecting its performance. An illustration of the effect is shown below in Figure 2-1 [1]-

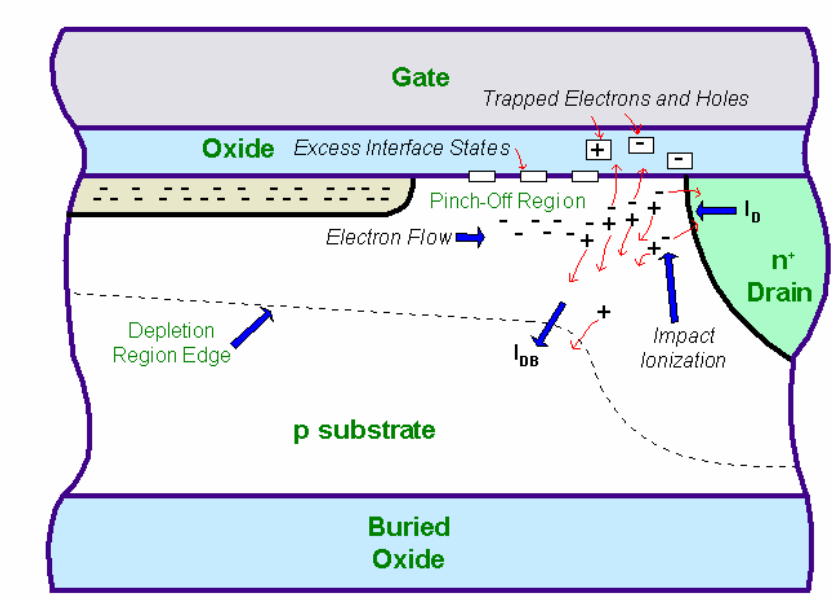


Figure 2-1: Diagram of hot-carrier effects.
The hot-carriers accelerated through the channel impact atoms in the silicon lattice, resulting in impact ionization. Some of these displaced electron-hole pairs overcome the gate potential and become embedded in the oxide [3].

[3].

An illustration of excessive V_{DS} within a simple circuit is shown in Figure 2-2. Methods for compensating for such a condition in a static circuit are often as straight forward as adding cascode devices, as illustrated below. Excessive V_{GS}, along with dynamic V_{DS} voltages, must be considered on a more case-by-case basis. This practice will be explained in-depth in Chapter 3, where a better understanding of the dynamic voltages, and the necessary voltage shielding, will be gained

The wide temperature range of operation can greatly affect the performance characteristics, and therefore the design, of the op amp. Across temperature, changes in the threshold voltage, mobility, etc., must be taken into account, with voltage headroom built into each circuit topology to account for changes in the operational parameters of the transistors.

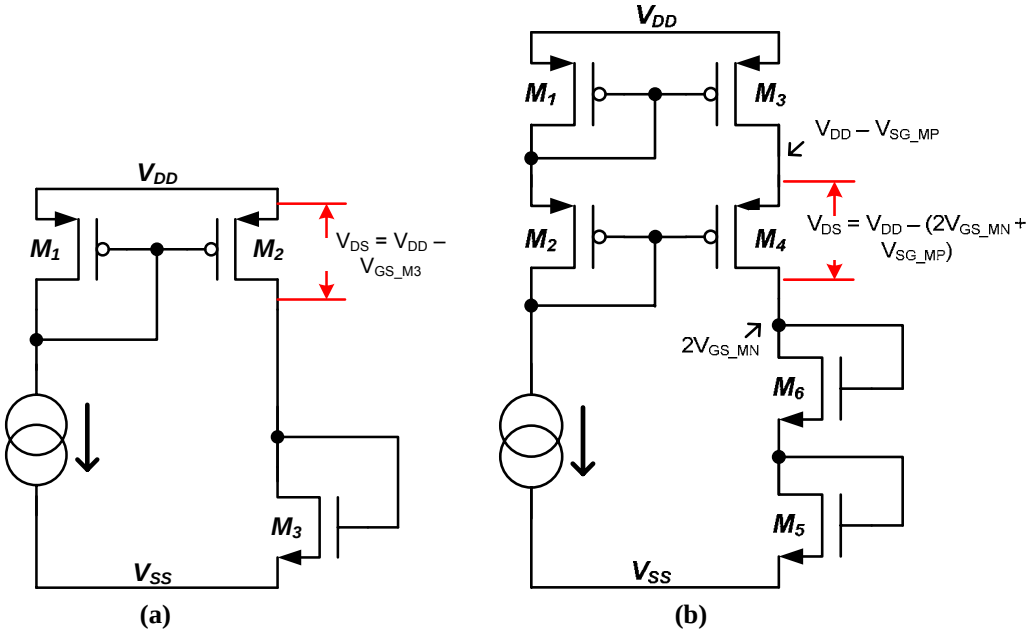


Figure 2-2: Excessive static V_{DS} voltage example.
(a) Simple example of a static device with excessive V_{DS}
(b) Possible solution, cascoding, to correct for excessive V_{DS} across the device

Design Methodology

To guard any given device from excessive voltage levels, several techniques may be utilized. Basic means of protection include adding diode-connected transistors or resistors in series with the device to reduce the voltage across its terminals, such as the cascoding shown in Figure 2-2. This method is generally all that is required for statically biased circuitry. A high V_{GS}, V_{GD}, or V_{DS} voltage may require bias circuitry that actively controls the gate voltage on a cascode device, especially in the case of dynamic voltages.

Obviously, shielding a device is only possible if it is understood that a certain device may experience a reliability condition, or an over-voltage level which places the reliability of the device at risk. The simulator used for the majority of this design, Mentor's ELDO SPICE tool, has the ability to run SOA (safe operating area) checks [4]. This utility allows the designer to enter the parameters at which a device is to be flagged, in this case any transistor with a V_{GS} or V_{DG} greater than 3.6 V, or a device with V_{DS} greater than 3.6 V that is not in cutoff. Once run, the simulator will record any SOA violations that occur during a DC or transient simulation. This allows for rapid detection and correction of design reliability concerns.

However, there are drawbacks to these methods. Extensive simulations must be completed not only to ensure that the devices are protected from oxide and hot carrier related effects, but that the circuit continues to function as desired across its intended operational range. For example, if there are too many devices being used in series to reduce the V_{DS} of a transistor, it may move out of saturation as process models, supply voltage, and temperature (PVT) are varied.

In the following section the top-level op amp design, as well as some of the circuitry used for voltage shielding, will be briefly discussed. A more in-depth view of the needs and required circuitry implementations will be presented in Chapter 3.

System Overview

The operational amplifier presented here is comprised of a fully-differential input stage, single-ended output stage, current reference, bias circuitry, power control circuitry, and compensation network. A top-level diagram of the op amp is given in Figure 2-3.

The first stage of the op amp is a fully-differential amplifier, using a regulated folded-cascode structure to provide high voltage gain. It uses complementary input pairs to provide for a rail-to-rail input common-mode range (ICMR). The use of complementary input pairs also allows a single input pair, for example the NMOS pair,

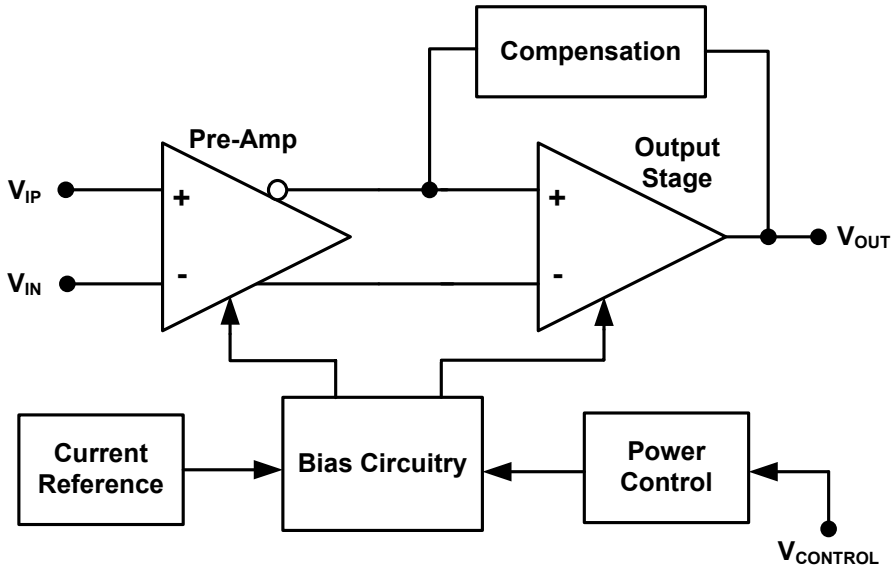


Figure 2-3: Operational amplifier top-level diagram

which would experience excessive V_{DS} voltages near the bottom of its common-mode input range, to be shut off. Figure 2.4 illustrates the dynamic V_{DS} concerns for a simple NMOS differential amplifier. Similarly, with a high common-mode input (V_{ICM}), the tail current device will experience a high V_{DS}. This can be improved by cascoding the tail current source.

The output stage is a class AB amplifier, which provides a large current driving capability and converts the differential signal from the input stage into a single-ended output. To shield the output devices, adaptively biased drive circuitry assures that the V_{GS} is maintained below 3.6-V, and an actively-biased cascode structure is utilized to limit the V_{DS} of the transistors.

Several bias structures are used to limit, clamp, and control node voltages within the output and input stages, which will be discussed in-depth in Chapter 3. There is also a switch used to move the amplifier between two modes of operation referred to as full power mode and half power mode. In half power mode, the bias current to the

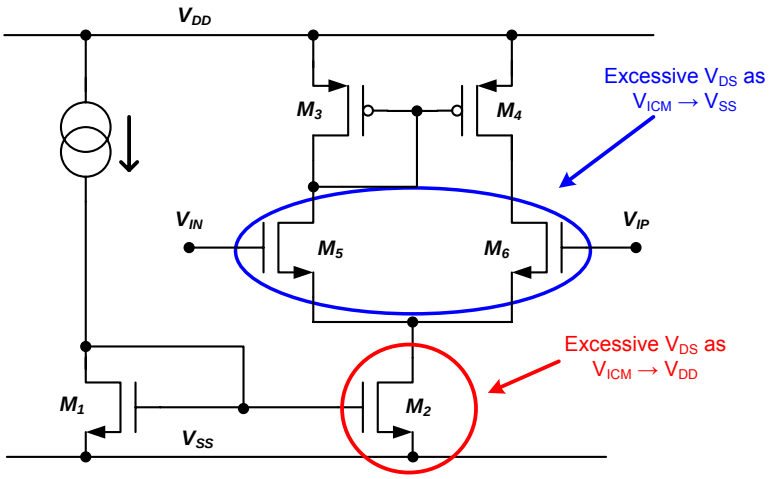


Figure 2-4: NMOS input differential amplifier and associated voltage concerns

amplifier's components are halved compared to full power mode operation, thus lowering the power consumption of the amplifier. Of course, this also affects several key performance parameters of the op amp, such as slew-rate, bandwidth, and phase margin.

The current reference is the most important component of the op amp in enabling a wide temperature range operation, −180˚C to 120˚C. Two common bias techniques for biasing op amps are constant g_m and constant current. Constant g_m current references maintain the small signal-performance parameters over temperature at the expense of large-signal parameters, while constant current references maintain the large-signal parameters at the expense of the small-signal op amp parameters. In order to provide the best possible small- and large-signal performance of this op amp over temperature, a constant inversion coefficient (IC) current reference is used [5]. This is a tradeoff, as the constant-IC reference allows for variations in both small- and large-signal parameters, but to a lesser degree than either the constant current or constant g_m references. The constant-IC current reference will be described in detail in Chapter 3.

CHAPTER 3

OPERATIONAL AMPLIFIER DESIGN

Input Stage

The primary design considerations for the input, or pre-amp, stage are a high gain amplifier with a rail-to-rail ICMR and the necessary protection circuitry. As stated previously it is a fully differential amplifier using a regulated folded-cascade structure with complementary input pairs. The basic organization of the differential input pairs and associated circuitry without the voltage protection devices is shown in Figure 3-1.

Transistors M9 and M10 steer the tail current bias of the NMOS and PMOS differential input pairs (M58, M59 and M56, M57, respectively) by comparing the signal at the amplifier's negative input terminal with a mid-supply reference voltage, V_{MID}. This in turn directs current to the mirror inputs M15 and M11, which control the bias on the input pairs' tail current devices. The source degeneration resistor, R1, is used to

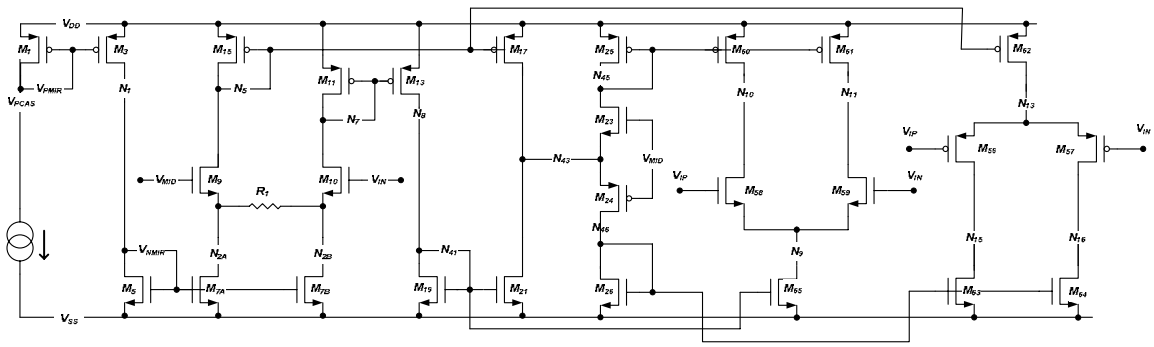


Figure 3-1: Input stage differential pairs without protection devices

linearise the output of M9 and M10, preventing an abrupt change in tail current across V_{ICM} [6]. This ensures that the input pairs are not exposed to excessive V_{DS} by shutting off the NMOS or PMOS pair when V_{ICM} goes low or high, with respect to the mid-supply voltage level.

Figure 3-2 shows the differential pairs and their tail current steering circuitry with the protection devices added. Static voltage protection is provided by the devices in blue, which is most often accomplished by adding cascode current mirror devices. Note that many of these supplementary devices have their gates tied to V_{MID} as opposed to their complementary cascode device. It was found that over PVT this biasing technique is more robust than standard cascode biasing at preventing SOA violations, and does not adversely affect the performance of the amplifier.

Dynamic protection is accomplished by the devices shown in red. This protection

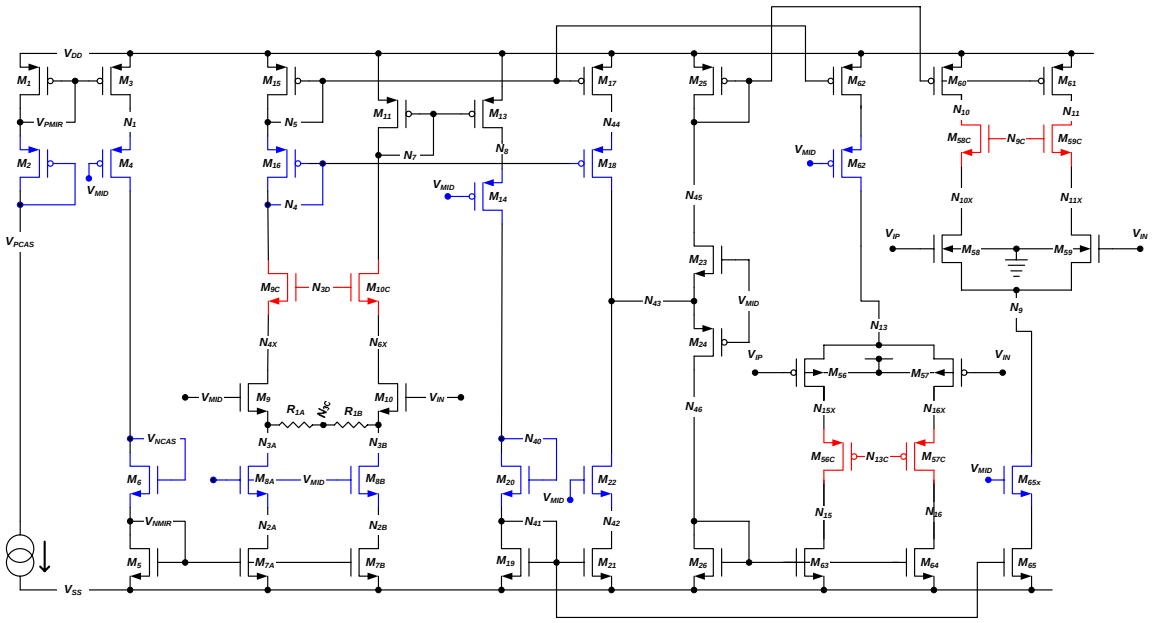


Figure 3-2: Input stage differential pairs with protection devices

is required to shield the input pairs, as well as the current steering devices. As the common-mode input voltage approaches V_{SS}, the V_{DG} on the NMOS input pair will approach roughly $V_{DD} - V_{SG,P}$. In the same way, if the common-mode level goes high, the PMOS input pair will experience excessive V_{GD}. Actively biased cascode devices are added to prevent this. However, they must be biased in such a way as not to clamp the amplifiers ICMR at high common-mode voltages, and must prevent low common-mode voltages from creating an SOA violation. Figure 3-3 contains the cascode bias circuit used to accomplish this.

The cascode bias cell creates a $V_{GS,N} + V_{DSAT,N}$ voltage that is placed across the NMOS input pair and tail-current steering input pair, and similarly a $V_{SG,P} + V_{DSAT,P}$ voltage across the PMOS input pair. This voltage tracks with temperature, maintaining the ICMR of the amplifier, while providing cascode protection to the input pairs. To illustrate, for the NMOS input pair a voltage equal to an NMOS V_{GS} plus an NMOS V_{DSAT} is created and placed across the source of the input pair to the shared gate of cascode devices M58C and M59C of Figure 3-2. This voltage maintains the NMOS

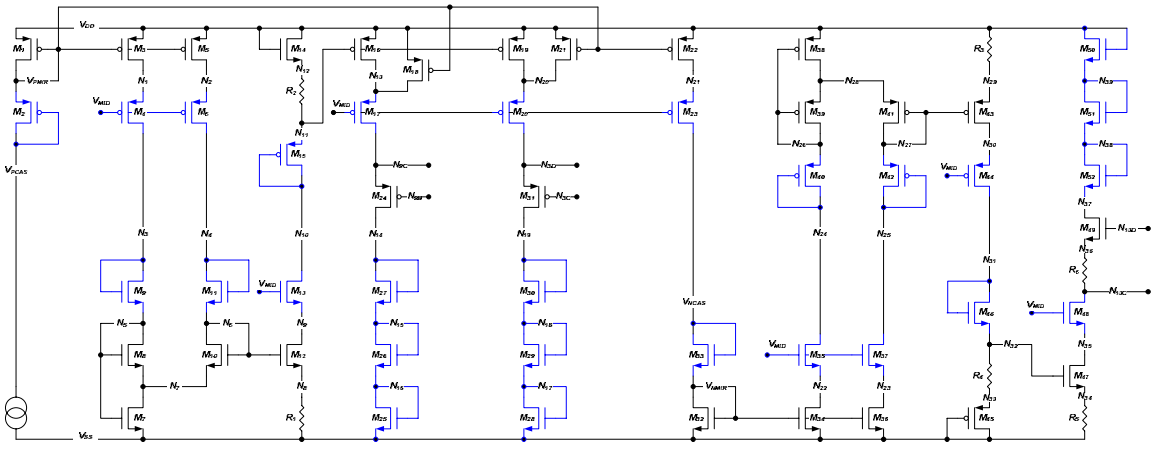
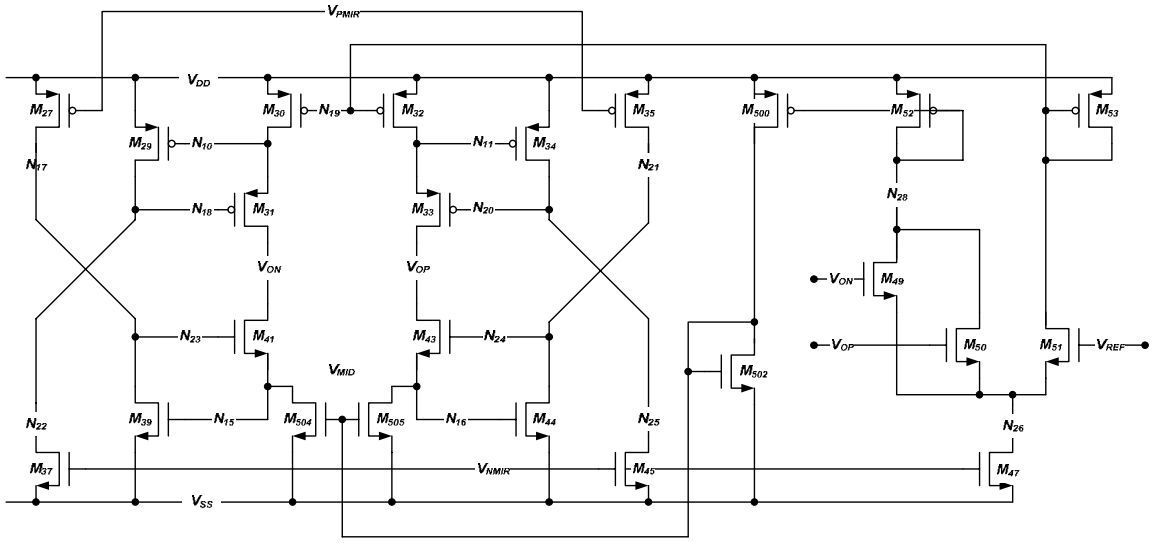


Figure 3-3: Cascode bias cell

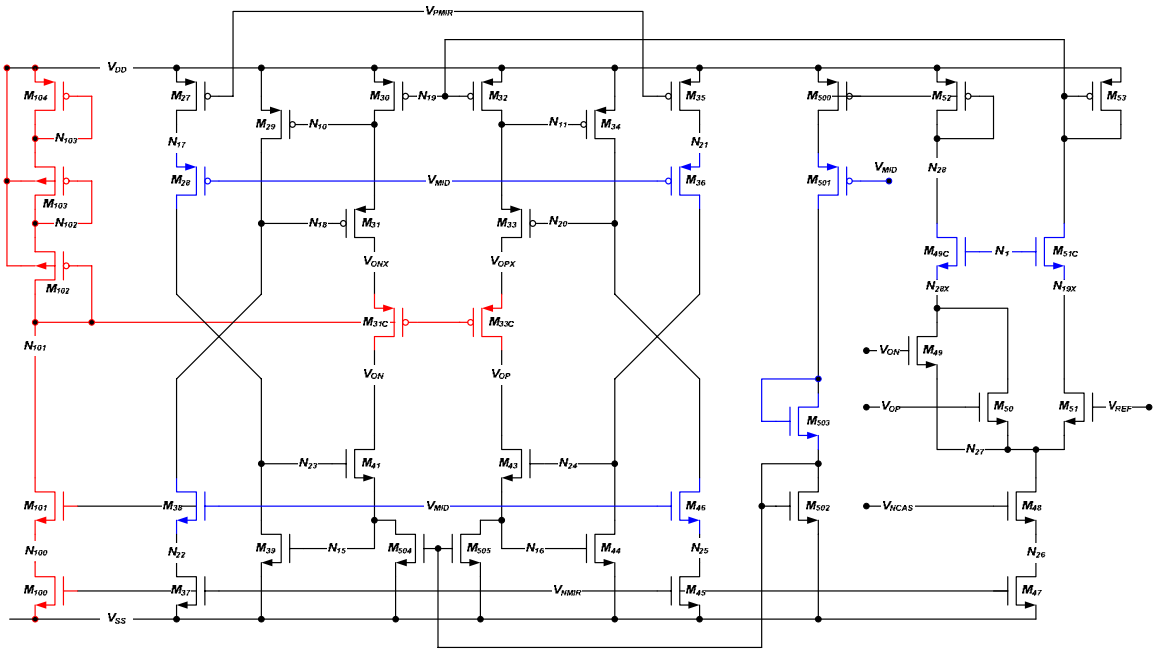
V_{DSAT} required to maintain the NMOS input pair in saturation, while protecting the devices from high V_{DG} voltages. This biasing is accomplished by creating the NMOS V_{GS} + V_{DSAT} voltage from the cascode bias cell. First, $V_{DSAT,N}$ is extracted from the Minch bias circuitry made up of M3, M5, M7, and M8 at node N7 [7][8]. An NMOS V_{GS} is then added at node N6, which is the gate to M12. M12 and R1 are matched to M14 and R2, thus providing $V_{DD} - (V_{GS,N} + V_{DSAT,N})$ at node N11. Using PDSOI, body effect may be eliminated in M14 to improve matching with M12. N11 is connected to the gate of M16, which therefore has a V_{SG} equal to $V_{GS,N} + V_{DSAT,N}$, and since M16 sets the current through this branch of the circuit, M24 also has a V_{SG} equal to $V_{GS,N}$ + $V_{DSAT,N}$, which is used to actively bias the NMOS input pair's cascode devices. This bias technique is copied and applied to the tail-current steering devices M9 and M10 (Figure 3-2), as well as the PMOS input pair.

The remaining components of first stage are the regulated folded-cascode and common-mode feedback (CMFB) circuitry, shown in Figure 3-4 [1][9]. The regulated folded-cascode structure provides high output resistance and therefore high gain for the first stage. Several cascode devices are added for static bias protection and M31C and M33C provide protection for M31 and M33, which would see excessive V_{DS} when the common-mode output voltage goes low. Additionally, devices MCL5, MCL6, MCL7, and MCL8, shown in the full schematic in Figure 3-5, provide voltage clamping for the source-follower amplifiers (M39, M44 and M29, M34) in the folded-cascode [6].

The CMFB circuitry maintains the common-mode output level of the first stage at V_{REF}. M49C and M51C are tied to node N1 (from Figure 3-2), which is biased at a

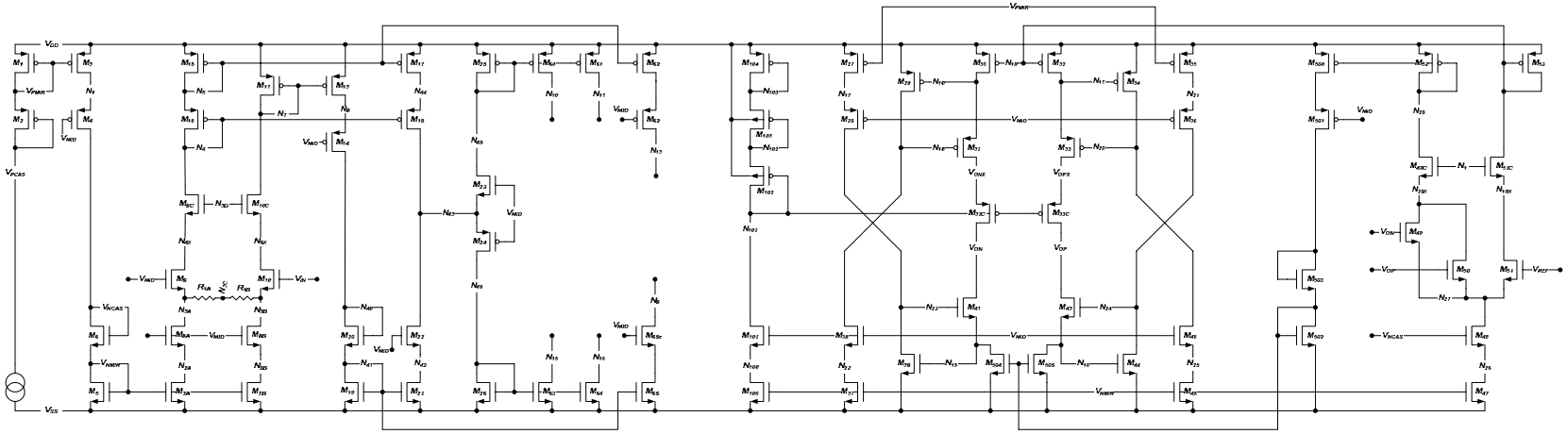


(a)

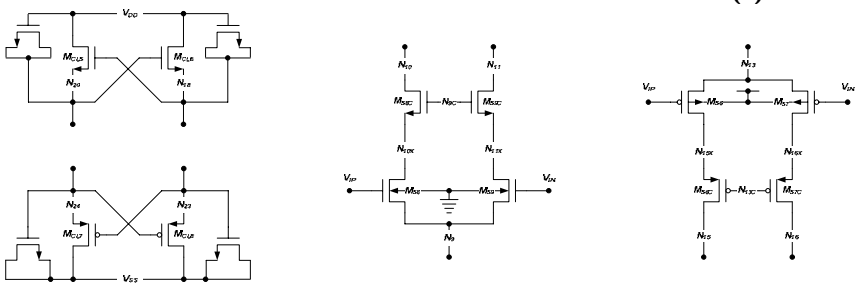


(b)

Figure 3-4: Regulated folded cascode and CMFB
(a) without protection devices
(b) with protection devices



(a)



(b) **(c)**

Figure 3-5: Complete input stage.
(a) bulk of input stage
(b) regulated cascode amplifier clamps
(c) complementary input pairs

PMOS V_{SG} above V_{MID}. This ensures M49, M50, and M51 have sufficient V_{DS} to stay in the saturation region. Also, the fully differential input stage allows for a relatively controlled output level for small-signal inputs, and a clamp-able output signal when slewing (large-signal). Clamping the output of the first stage prevents SOA's, as well as decreases the recovery time of the circuit from large slewing, or saturation, events.

Output Stage

The output stage is a class AB amplifier, for which a simplified schematic is shown in Figure 3-6. The design specifications required a power efficient stage capable of a rail-to-rail output swing that could drive capacitive and resistive loads, and provide large short-circuit current driving capability. The output stage also converts the differential signal from the input stage to a single-ended output [9].

In order to maintain power efficiency and still be capable of driving a heavy load when needed, an adaptive output driver is used [10]. For the first set of input devices, M16 and M17, under quiescent conditions, the current through M16 is equal to the input

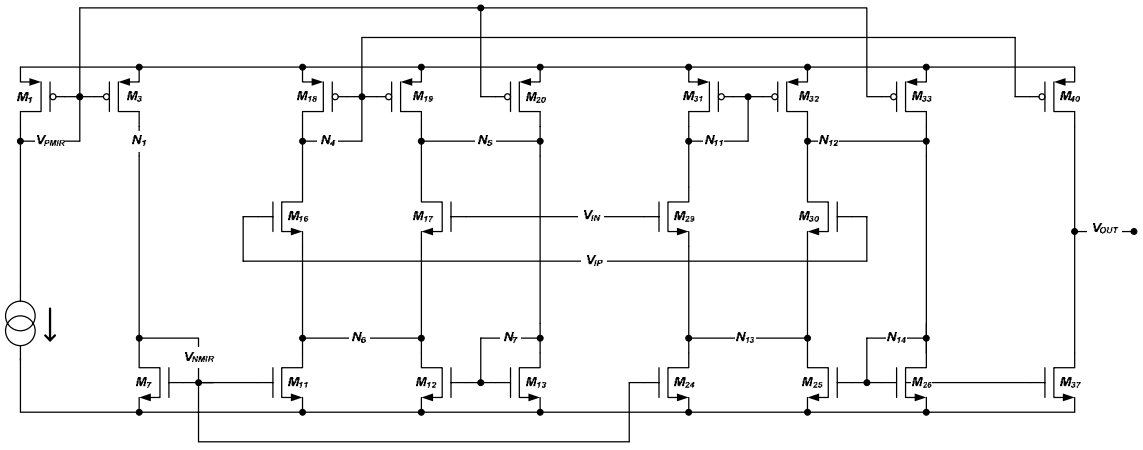


Figure 3-6: Output stage without protection devices

bias current *I*. The current mirror devices M18 and M20 are matched and generate current *I*, and have an aspect ratio of 1:1.5 with device M19. Therefore, under quiescent conditions the current through M12 and M13 equals $1.25 \times I$. When a slewing condition occurs and the V_{IP} signal goes high while V_{IN} goes low, M17 can be considered turned off. This increases the current through M16 since all of M12's current will now go to the M16 circuit branch, which in turn is amplified by 1.5 through transistor M19. This creates a positive feedback loop increasing the maximum output current, since the output device M40 mirrors M18's current. The current in this loop increases until there is no longer sufficient voltage to maintain M16 in saturation. In this fashion, large transient current is sourced into the load. The loop is broken when the input voltages return to the common-mode level. A complementary action sinks large transient current from the load when V_{IN} goes high and V_{IP} goes low.

Figure 3-7 illustrates the output stage with the required protection circuitry. The cascode protection devices on the input pairs have their gates biased at a PMOS V_{DSAT} below V_{DD} to ensure that the input pairs are in saturation. Since the output swing is nearly rail-to-rail, cascode devices are required to protect the output drivers, M37 and M40, from excessive V_{DS}. Actively biased ohmic cascode's are used to control the V_{DS} levels in the output driver branch [11]. This structure regulates the gate bias of the cascode devices by comparing the V_{DS} of the output devices M37 and M40 to a mid-supply voltage. As the V_{DS} across M37 and M40 varies with output voltage, the simple regulation amplifiers adjust the gate bias of the ohmic cascode transistors to maintain the voltage level and prevent an SOA violation. Additionally, $M_{CL1,2,3}$ and $M_{CL4,5,6}$ clamp the V_{GS} of M38 and V_{SG} of M39 to maintain a safe operating region.

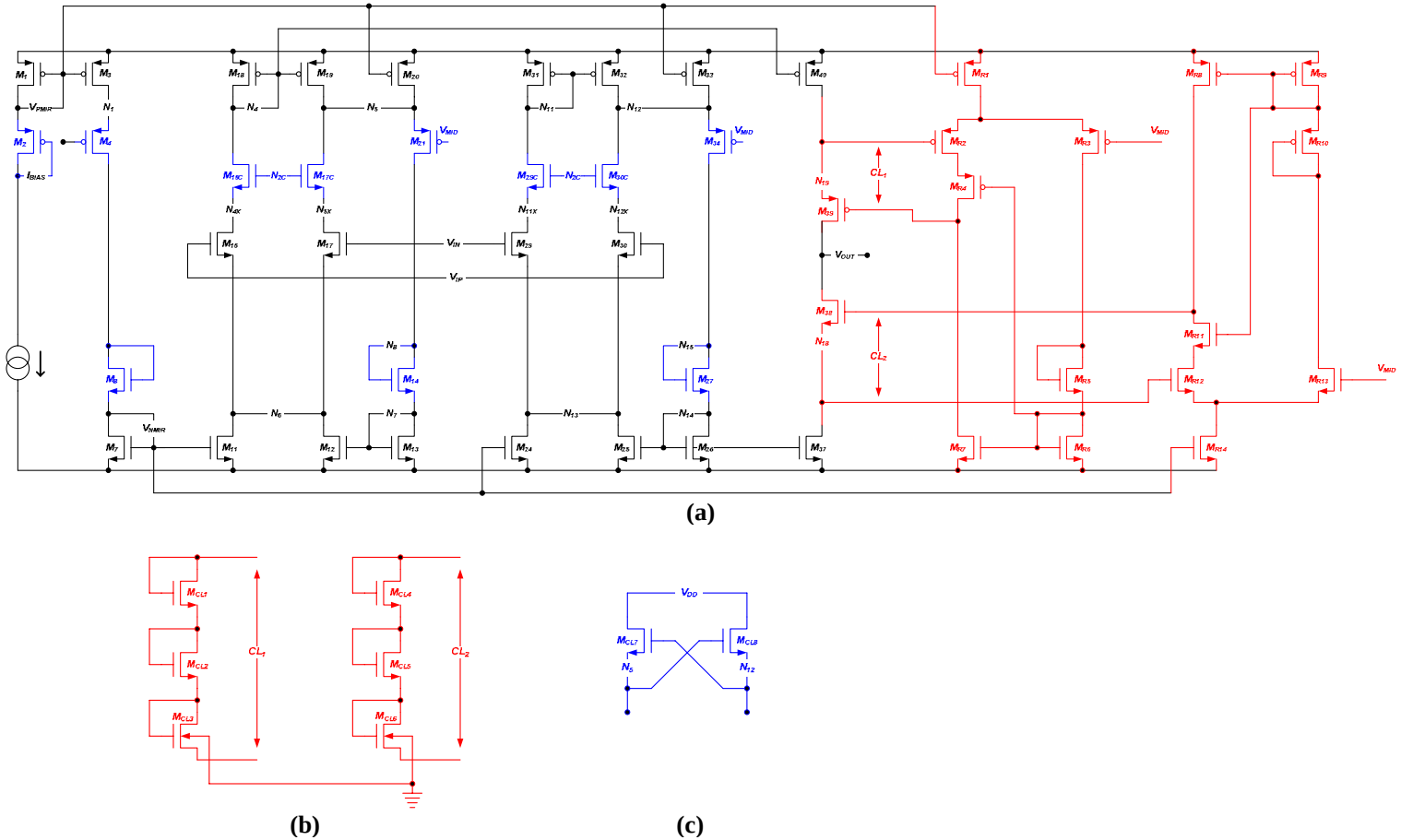


Figure 3-7: Complete output stage.
(a) bulk of output stage
(b) ohmic cascode V_{GS} clamps
(c) adaptive output driver clamps

Frequency compensation for the amplifier is provided by the compensation network shown in Figure 3-8 [9]. A 20 pF Miller capacitor and matching 10 pF capacitors, along with zero compensation resistors, are the major components of the network. V_{REF} provides the reference voltage for the input stage's common-mode level that is less susceptible to supply noise than $V_{MID.}$ $M_{CL7,8}$ and $M_{CL9,10}$ clamp V_{OP} and V_{ON} (the outputs of the input stage) to decrease the recovery time of the input stage from a large slewing (saturation) event.

Power Control

The design specifications for this op amp called for the ability to be able to run the circuit in a low power, or 'half power' mode. Switching to half power mode is accomplished by halving the bias current fed into the amplifier's components from the current reference. The circuit utilized to control the switching is shown in Figure 3-9.

If left floating, the input control signal $V_{CONTROL}$ is pulled low by resistor R_2. This causes M4, M5, and M6 to be shut off. In turn, M12 is activated, which pulls the

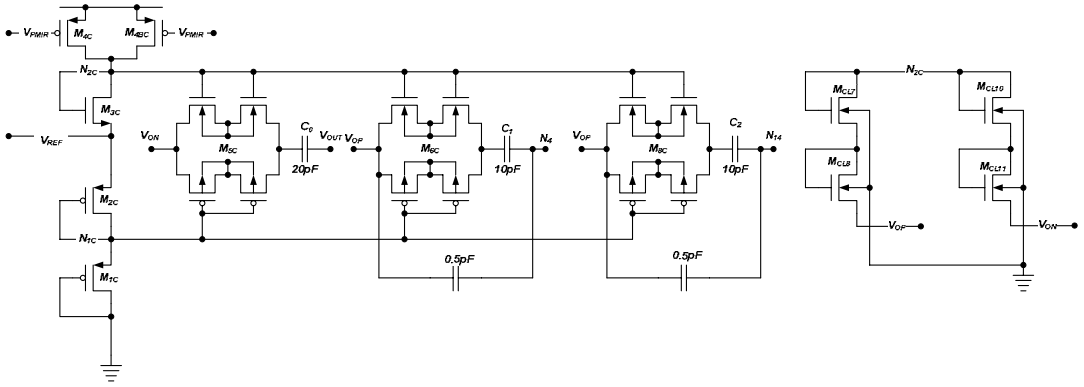


Figure 3-8: Compensation Network

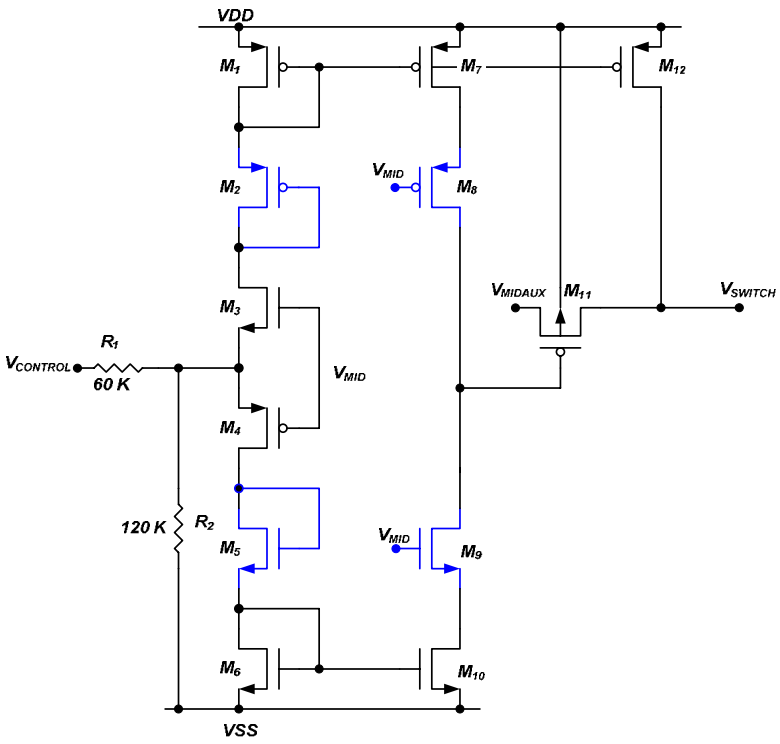


Figure 3-9: Power control circuitry

output V_{SWITCH} up to V_{DD}. This high output level is used to signal the half power mode. However, if $V_{CONTROL}$ is pulled high, M1, M2, and M3 are shut off, pulling down M11's gate such that M11 shorts the output V_{SWITCH} to V_{MIDAUX}. V_{MIDAUX} is a V_{MID} voltage generated by a duplicated V_{MID} cell. This was done in order to isolate V_{MIDAUX} from the system-wide V_{MID}. If the power mode were to be switched while the op amp is functioning, having a separate V_{MID} cell for this circuit prevents noise from the switching event from affecting other op amp components that utilize the reference voltage.

This output signal V_{SWITCH} is connected to a current bias circuit that splits the output of the current reference and feeds it into the necessary branches of the op amp. This circuitry is shown in Figure 3-10. V_{SWITCH}, coming from the power control circuitry, is either at a high voltage level, V_{DD}, or at V_{MID}. If it is high, M7 is turned off,

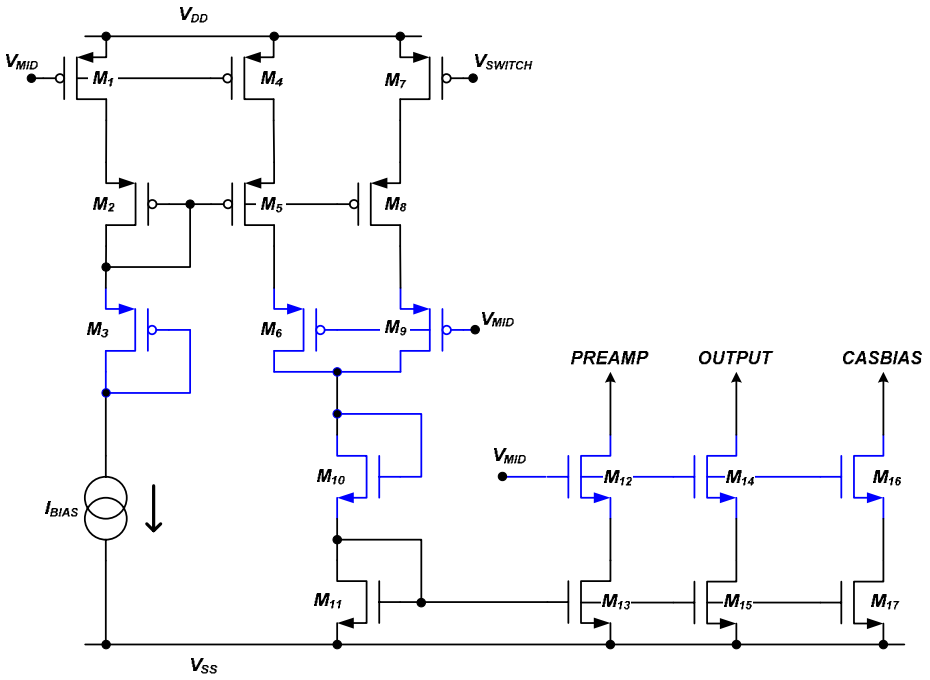


Figure 3-10: Current bias circuitry

in turn shutting off M8 and M9. This is considered 'half power' mode as only half of the 'full power' current is being fed into the amplifier. If V_{SWITCH} is at the V_{MID} voltage level, M7 is on, mirroring the current from the M1, M2, and M3 branch, placing the amplifier in 'full power' mode. The gates of the cascode current mirror devices M12, M14, and M16 are tied to V_{MID} to prevent SOA violations over PVT.

Current Reference

In selecting the circuit topology for the current reference the paramount concern is to minimize the performance variation of the op amp across the specified temperature range of operation, −180˚C to 120˚C. One well-established technique is to use a constant

g_m current reference biasing scheme which minimizes variations in small-signal performance, such as bandwidth, at the cost of large-signal performance variation, such as slew rate. Another technique is to use a constant current reference, which minimizes variations in large-signal performance over temperature at the expense of small-signal characteristics. However, in general, it is desirable to simultaneously minimize variations in both small-signal and large-signal performance. In order to achieve this, a constant inversion coefficient (IC) current reference was developed [5] [12].

The constant-IC concept can be demonstrated by plotting the magnitude of variation in transconductance and current for a MOSFET over the operating temperature range versus the temperature exponent of the bias current, as shown in Figure 3-11 (assuming a mobility temperature exponent of −1.5). In this plot the magnitude of change in strong- and weak-inversion transconductance and the inverse magnitude of

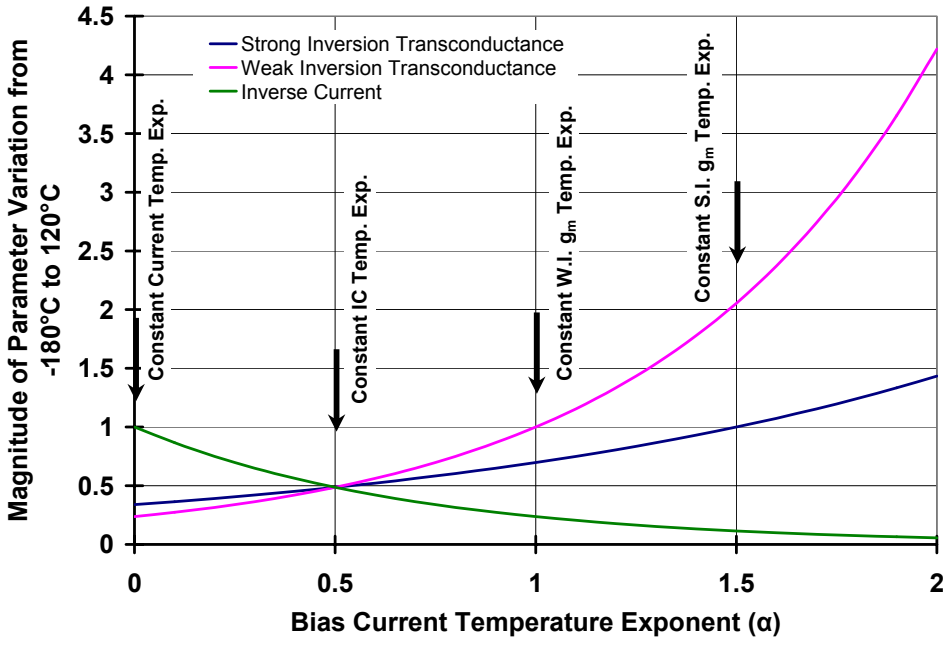


Figure 3-11: Magnitude of parameter variation vs. bias current temperature exponent

change in current are given. As shown in the plot, for a bias current temperature exponent of zero, the magnitude of change in current is 1, representing constant current over temperature. Constant weak- and strong-inversion transconductance are given at bias current temperature exponents of 1.0 and 1.5, respectively. From this plot it is evident that the least variation in all parameters occurs at a temperature exponent of 0.5, which happens to be the temperature exponent of the MOSFET inversion coefficient [13]. The magnitude of change of the large- and small-signal variations for the three types of current references being discussed is shown in Table 3-1. It is evident that the constant-IC current reference has lower overall variation in its large- and small-signal parameters than either constant transconductance or constant current references.

The constant IC current reference seeks to maintain a constant inversion coefficient for MOSFETs across temperature. MOSFET inversion coefficient is defined in [13]. Constant IC is a tradeoff between the large-signal stability provided by the constant current reference, and the small-signal stability provided by the constant g_m reference. A simplified schematic for the current reference is shown in Figure 3-12.

Table 3-1: Magnitude of parameter variation over temperature vs. temperature exponent

	Constant *I*	**Constant g_m**	**Constant *IC***
***SR* Variation (SR_{120}/SR_{-180})**	1	W.I.: 4.2 S.I.: 8.7	2.04
BW Variation (BW_{120}/BW_{-180})	W.I.: 0.24 S.I.: 0.34	1	0.49

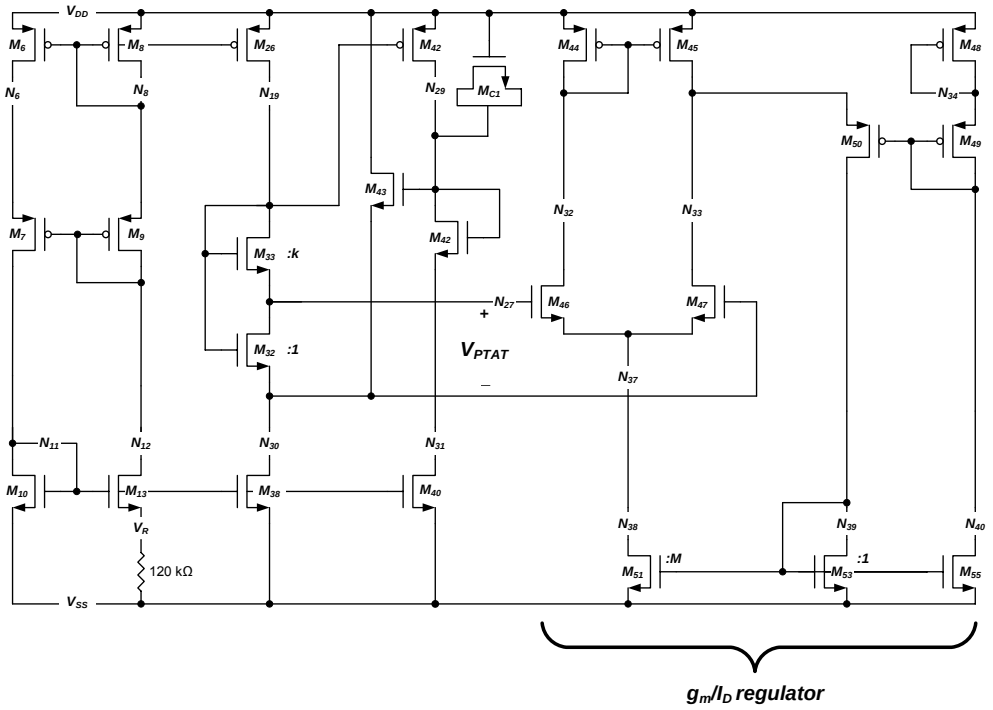


Figure 3-12: Simplified current reference without startup

The reference operates by creating a proportional to absolute temperature (PTAT) voltage that is fed into a g_m/I_D regulator circuit, the output current of which maintains the MOSFET g_m/I_D ratio, and therefore the inversion coefficient, across temperature. The first two (left most) branches of the current reference shown in Figure 3-12 make up a simple low-level (low current) current generator that biases M32 and M33. This small current ensures that M32 and M33 are biased in weak inversion, in order to create the PTAT voltage.

The drain current equation for a MOSFET in weak inversion is given as

$$I_D = I_S \exp\left(\frac{V_{GS} - V_T}{nU_T}\right), \tag{3.1}$$

where I_S is the saturation current, U_T the thermal voltage, V_T the threshold voltage, and n the subthreshold slope parameter. From this the expression for V_{GS} is derived as

$$V_{GS} = \ln\left(\frac{I_D}{I_S}\right) nU_T + V_T . \tag{3.2}$$

The PTAT voltage is measured from the source of M32 to the source of M33. Here again, thanks to PDSOI, body effect is eliminated in M32 and M33. M32 and M33 are also matched in layout. Taking the voltage from the source of M32 to source of M33 to be V_{REF} (not to be confused with V_{REF} of Figure 3-8), the PTAT voltage can be calculated as

$$\begin{aligned} V_{REF} &= V_{GS,M32} - V_{GS,M33} \\ V_{REF} &= \ln\left(\frac{I_D}{I_{S,M32}}\right) nU_T + V_T - \left[\ln\left(\frac{I_D}{I_{S,M33}}\right) nU_T + V_T\right] \\ V_{REF} &= nU_T \times \ln\left[\left(\frac{I_D}{I_{S,M32}}\right)\left(\frac{I_{S,M33}}{I_D}\right)\right] = nU_T \times \ln\left(\frac{I_{S,M33}}{I_{S,M32}}\right) \end{aligned} \tag{3.3}$$

Selecting M33 to have an aspect ratio k times greater than M32,

$$I_{S,M33} = kI_{S,M32} \tag{3.4}$$

$$V_{REF} = nU_T \ln(k). \tag{3.5}$$

Since thermal voltage (U_T) is equal to kT/q (where k is Boltzmann's constant), the only undefined variables are temperature and the subthreshold slope parameter, n. Neglecting the small variance in n, this makes the voltage V_{REF} dependent upon changes in temperature, and therefore a PTAT voltage.

V_{REF} becomes the input to the g_m/I_D regulator. A block diagram of which is given in Figure 3-13. The current I_{OUT} is defined as

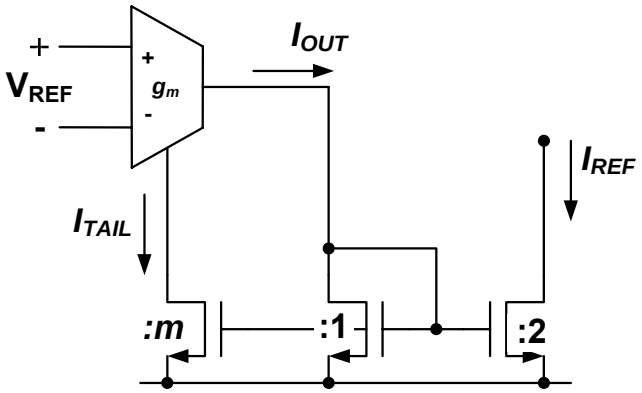


Figure 3-13: Block diagram of g_m/I_D regulator

$$I_{OUT} = g_m V_{REF} . \tag{3.6}$$

And I_{TAIL} and I_D are defined as

$$I_{TAIL} = mI_{OUT} , \tag{3.7}$$

$$I_D = \frac{I_{TAIL}}{2} , \tag{3.8}$$

where I_{TAIL} biases the transconductor block, implemented using an NMOS input pair (M46, M47 in Figure 3-12). Solving for g_m/I_D, during balanced (quiescent) operation,

$$\begin{aligned} &\Rightarrow I_{OUT} = I_D\left(\frac{2}{m}\right) \\ &\Rightarrow g_m V_{REF} = I_D\left(\frac{2}{m}\right) \\ &\Rightarrow \frac{g_m}{I_D} = \frac{1}{V_{REF}}\left(\frac{2}{m}\right) \end{aligned} \tag{3.9}$$

Taking the EKV [14] definition for g_m/I_D and equating it to the g_m/I_D from our circuit,

$$\frac{g_m}{I_D}(ckt.) = \frac{1}{V_{REF}}\left(\frac{2}{m}\right) \Leftrightarrow \frac{g_m}{I_D}(EKV) = \frac{1}{nU_T}\left[\frac{1}{\sqrt{IC + 0.25} + 0.5}\right]. \tag{3.10}$$

The inversion coefficient can then be found

$$\begin{aligned}
&\Rightarrow \frac{1}{V_{REF}}\left(\frac{2}{m}\right) = \frac{1}{nU_T}\left[\frac{1}{\sqrt{IC+0.25}+0.5}\right] \\
&\Rightarrow \sqrt{IC+0.25}+0.5 = \left(\frac{V_{REF}}{nU_T}\right)\left(\frac{m}{2}\right) \\
&\Rightarrow IC+0.25 = \left[\left(\frac{\alpha \times m}{2}\right)-0.5\right]^2, \quad \alpha = \frac{V_{REF}}{nU_T} \\
&\Rightarrow IC = \left(\frac{\alpha \times m}{2}\right)^2 - \left(\frac{\alpha \times m}{2}\right)
\end{aligned} \tag{3.11}$$

Now substituting

$$\begin{aligned}
&\alpha = \frac{V_{REF}}{nU_T} \Rightarrow \frac{nU_T \ln(k)}{nU_T} \Rightarrow \ln(k) \\
&\Rightarrow IC = \left(\frac{\ln(k) \times m}{2}\right)^2 - \left(\frac{\ln(k) \times m}{2}\right)
\end{aligned} \tag{3.12}$$

The inversion coefficient is therefore dependent on only the aspect ratio (k) of the PTAT voltage generator, M32 and M33, and the g_m/I_D current mirror ratio m set by devices M53 and M51. This shows that the reference generates a bias condition such that the MOSFET inversion coefficient is independent of temperature.

The complete current reference, including startup circuitry and protection devices, is shown in Figure 3-14. Numerous cascode devices are added for static voltage protection. Additional V_{PTAT} generating MOSFETs are placed in series to create a larger V_{REF} voltage for better accuracy. M43 and M43B form a feedback loop that prevents the reference voltage, V_{REF}, from floating toward the power rails and causing biasing problems within the g_m/I_D regulator.

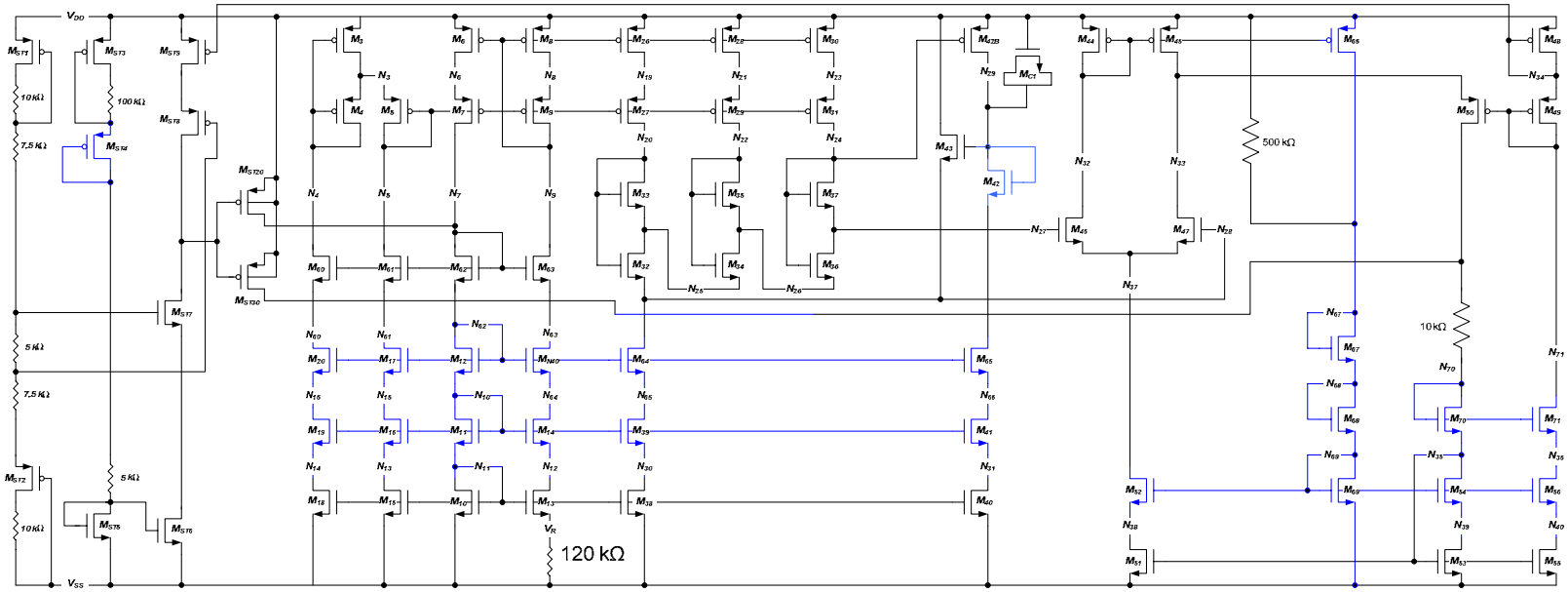


Figure 3-14: Complete current reference

The startup circuit operates by creating a small current, on the order of 1-2 μA, with devices M_{ST1-5}, and comparing it to the references output current fed back from M48. If the startup reference current is larger than the output current, which is approximately 20 μA when the reference is biased at its quiescent point, the gates of the two PMOS switches, M_{ST20} and M_{ST30}, are pulled low, injecting current into the low-level current bias and the output branches of the circuit. During fabrication it was discovered that the g_m/I_D regulator may not properly startup under certain conditions. Because of a this, a 500 kΩ resistor was added to inject current into the drain of M67 instead of a switch.

The simulated performance of the current reference over temperature is shown in Figure 3-15. Note that it was found the supplied BSIM3 models did not correctly model the V_{PTAT} performance across temperature. Because of this, simulations of the current

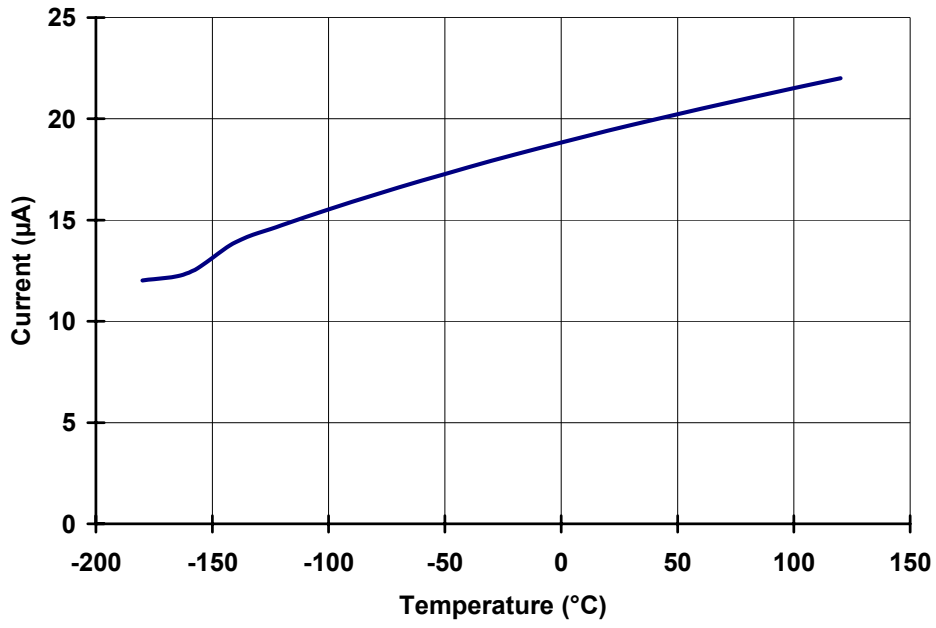


Figure 3-15: Simulated constant-IC current over temperature

reference were conducted using both the supplied BSIM3 model, and a custom-made EKV model. The performance has been verified with previously fabricated versions of the reference.

Simulated System Level Performance

To verify operation of the op amp across temperature, performance characterizing simulations were performed. This included open-loop gain and gain-bandwidth, small- and large-signal analysis with transient response characterization and other standard amplifier characteristics such as short circuit output current, CMRR, and PSRR. Unless otherwise stated, the simulations shown were performed using BSIM3 typical models with a 5-V V_{DD} across temperature. However, the V_{PTAT} voltage generator in the current reference was not properly modeled by the BSIM3 models. Because of this, EKV models were used to simulate the performance of the current reference. A model was then created to represent the performance of the current reference's output, which was used in the BSIM simulations of the op amps performance.

Confirmation of the models functionality across temperature was carried out through the comparison of the simulated values of the NMOS and PMOS mobility and threshold to the corresponding measure data [15]. Figure 3-16 and Figure 3-17 show the simulated and measured PMOS mobility and threshold information, while Figure 3-18 and Figure 3-19 show the NMOS data. In general, the simulated performance of these parameters matches relatively well with the measured values across temperature.

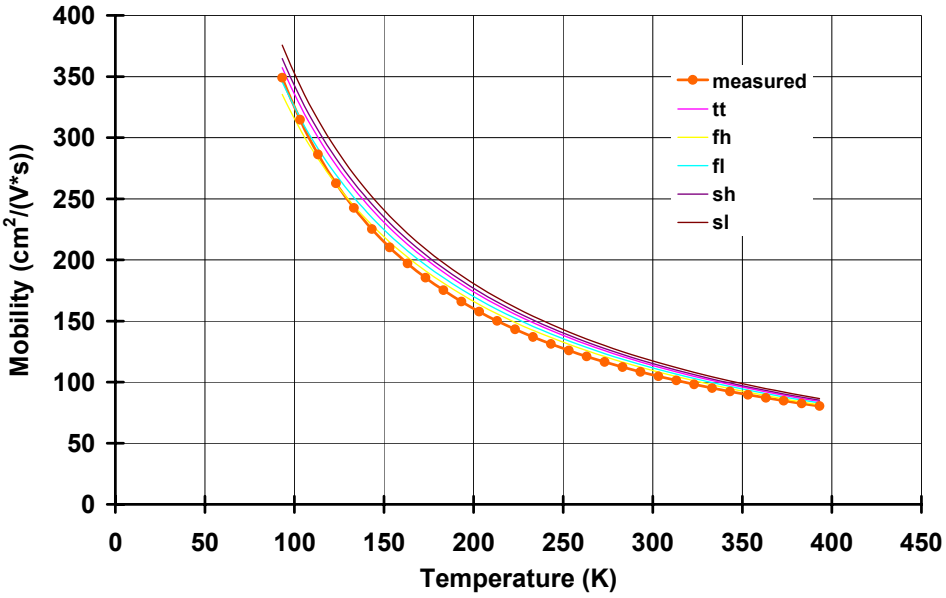


Figure 3-16: PMOS mobility vs. temperature

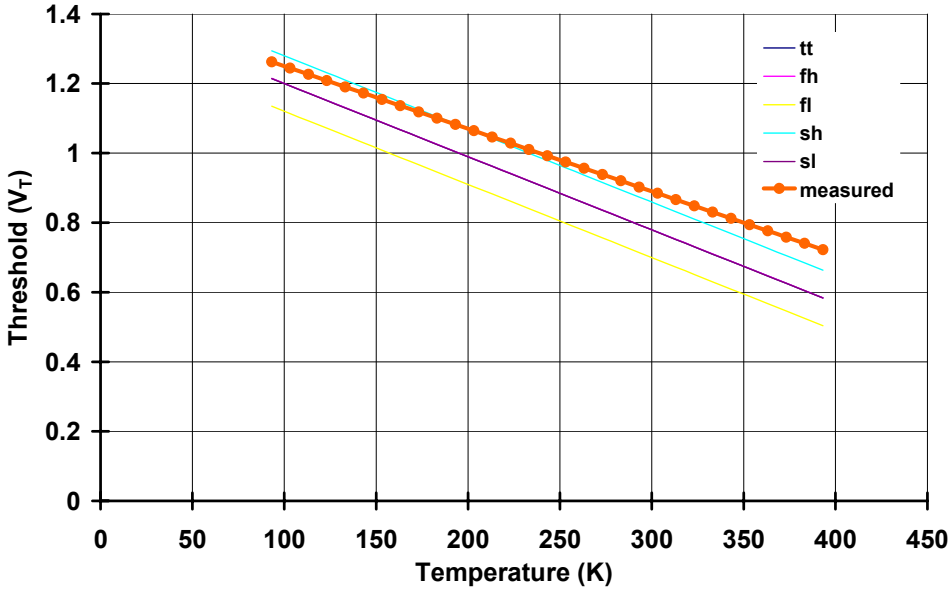


Figure 3-17: PMOS threshold vs. temperature, W/L=5/0.35

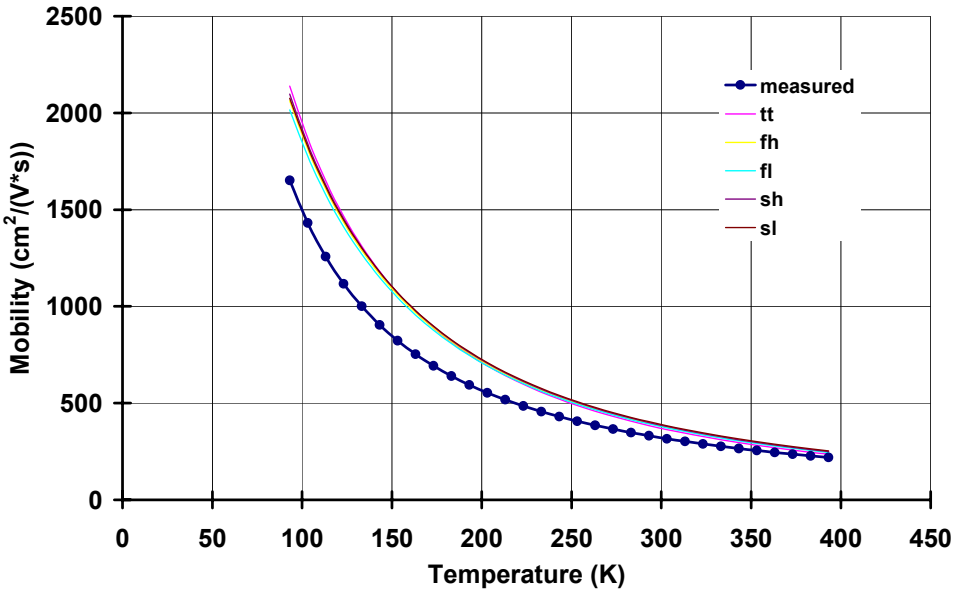


Figure 3-18: NMOS mobility vs. temperature

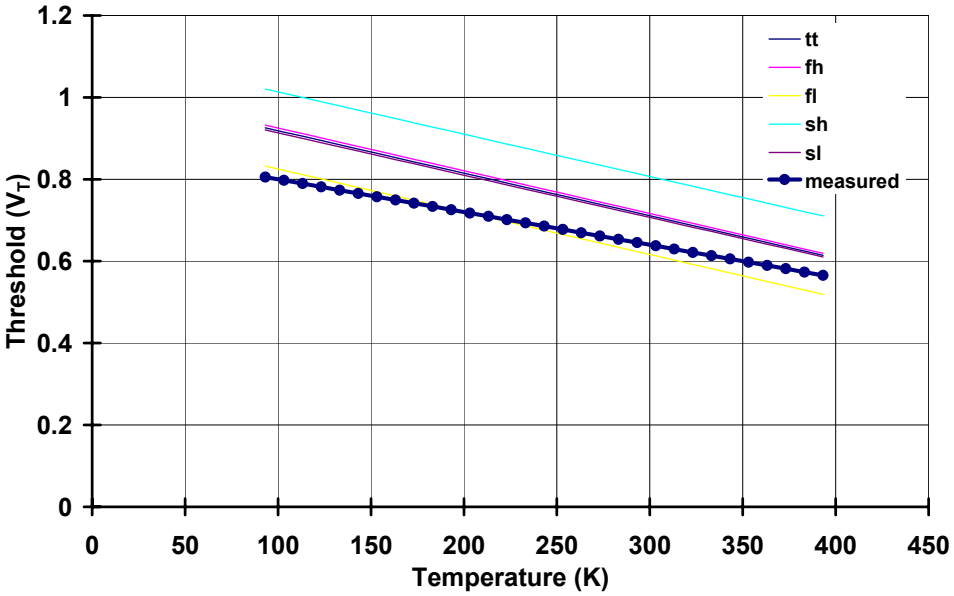


Figure 3-19: NMOS threshold vs. temperature, W/L=5/0.35

The operational amplifier configurations used for the simulations in this section reflect the configurations used for measurements, which will be discussed in-depth in Chapter 4. The complementary input pairs allow for a full swing ICMR, the simulated values for which are shown in Figure 3-20. Note that ICMR is not noticeably affected by changing to full or half power mode and is consistent across temperature (not shown). The simulated large-signal transient response is given in Figure 3-21 and Figure 3-22. Figure 3-23 shows the slew-rate vs. temperature for half and full power modes compiled from these simulations. Note that the slew-rate in half power mode is roughly half the slew rate of full power mode, which is consistent with the op amp receiving half of its full power bias current.

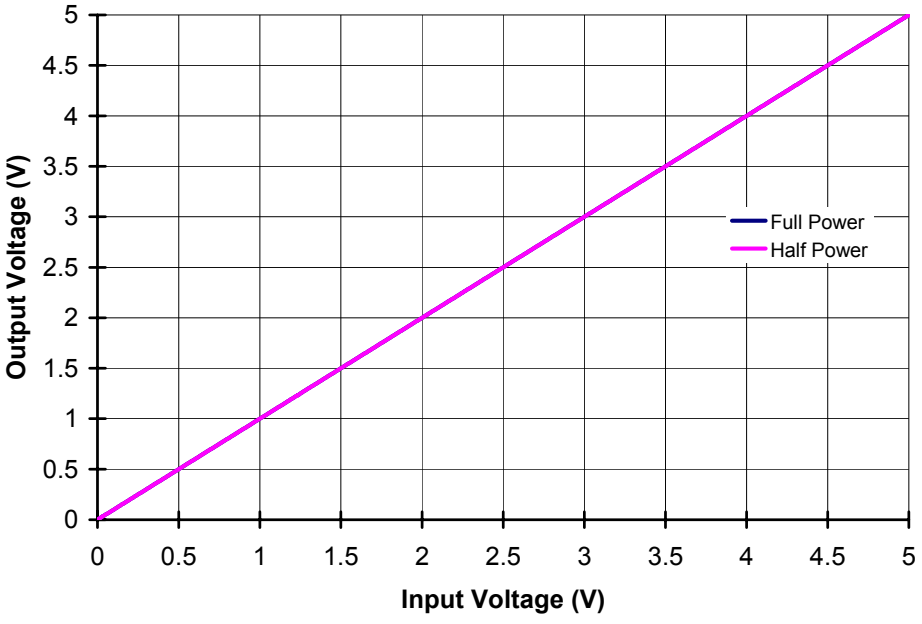


Figure 3-20: Simulated ICMR, 25°C

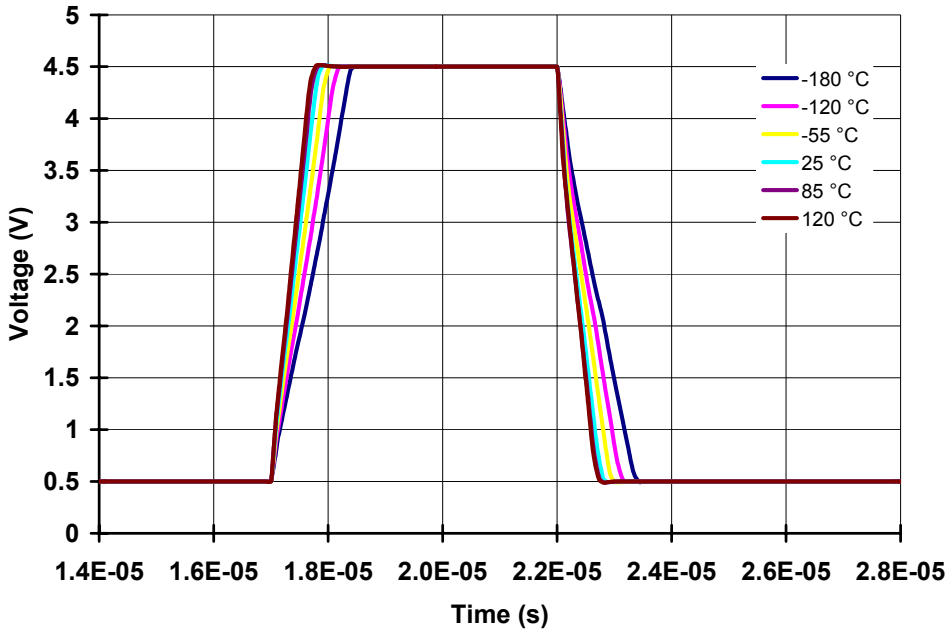


Figure 3-21: Simulated large-signal transient response, full power

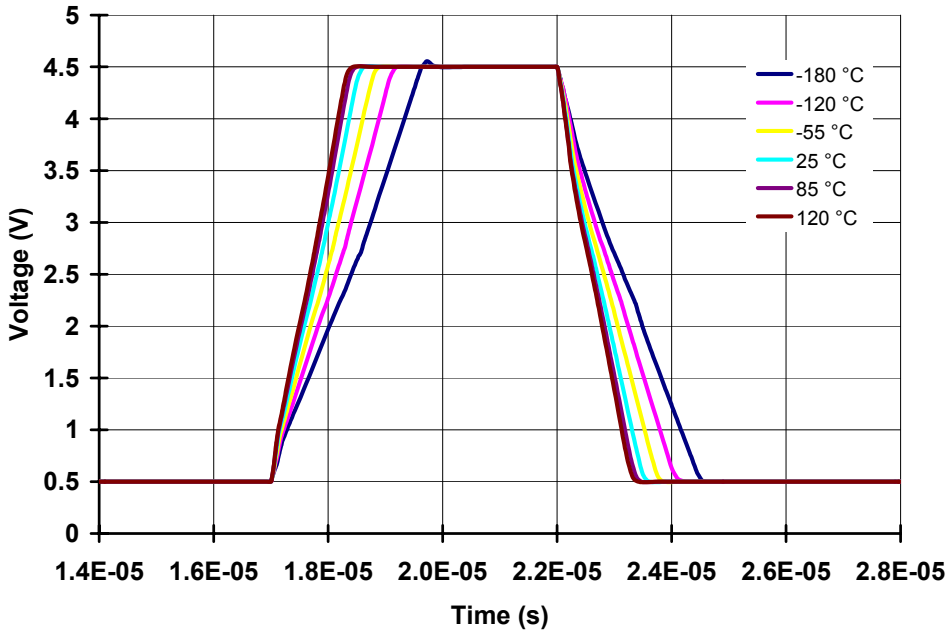


Figure 3-22: Simulated large-signal transient response, half power

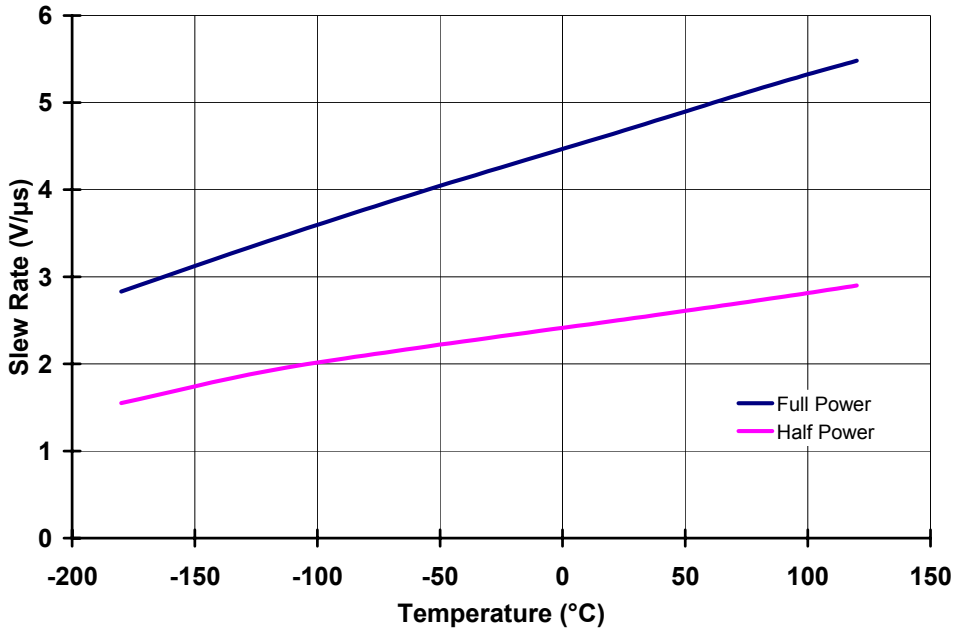


Figure 3-23: Simulated slew-rate vs. temperature

The simulated short-circuit current for the op amp in both modes of operation is given in Figure 3-24. Figure 3-25 gives the simulated quiescent supply current requirements for the op amp.

Figure 3-26 and Figure 3-27 show the simulated open-loop gain across temperature. The DC gain across temperature and operational mode is maintained at well above 120 dB.

It was found that the simulation results that best match the measurements of the amplifiers bandwidth and phase margin were made using the EKV models, as opposed to BSIM3 models. The EKV simulated unity-gain bandwidth and phase margin over temperature are given in Figure 3-28 and Figure 3-29.

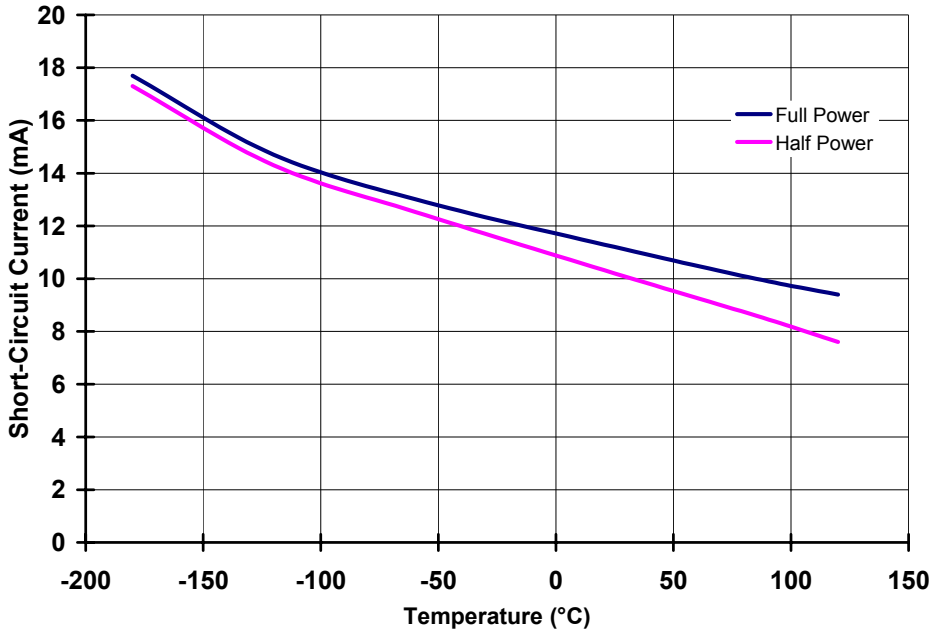


Figure 3-24: Simulated short-circuit current vs. temperature

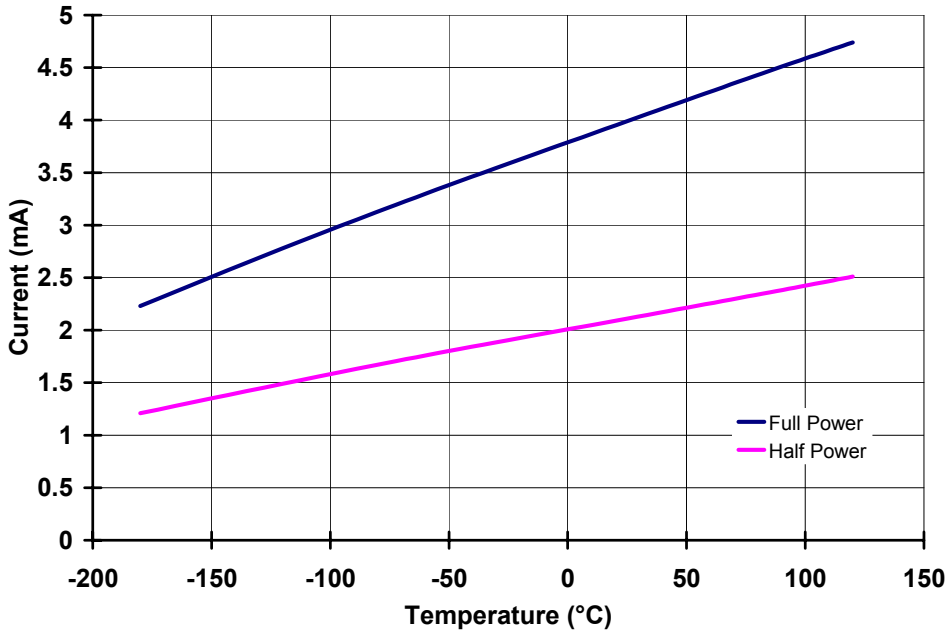


Figure 3-25: Simulated op amp supply current, 5-V V_{DD}

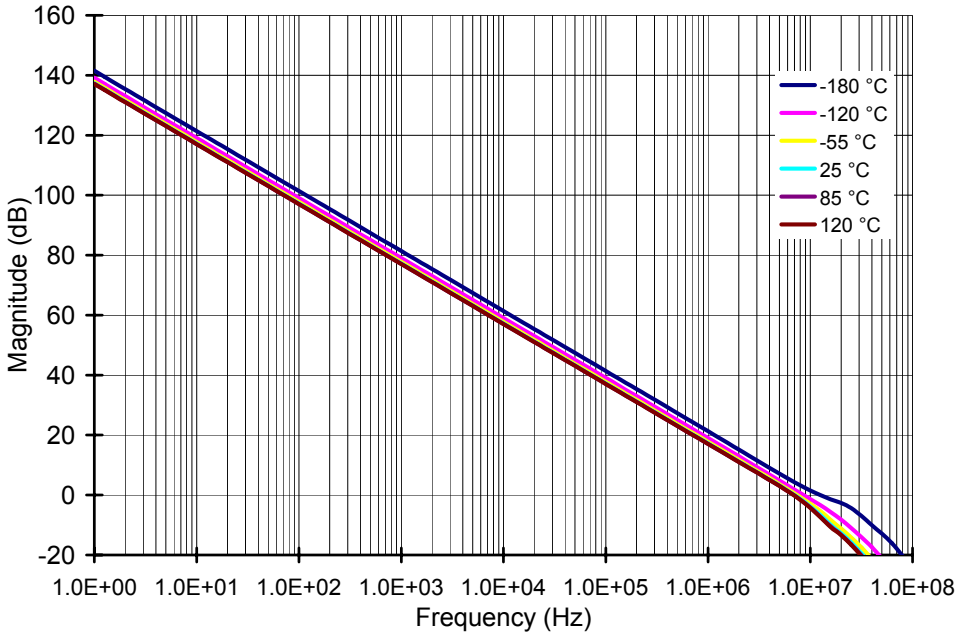


Figure 3-26: Simulated A_{OL}, full power

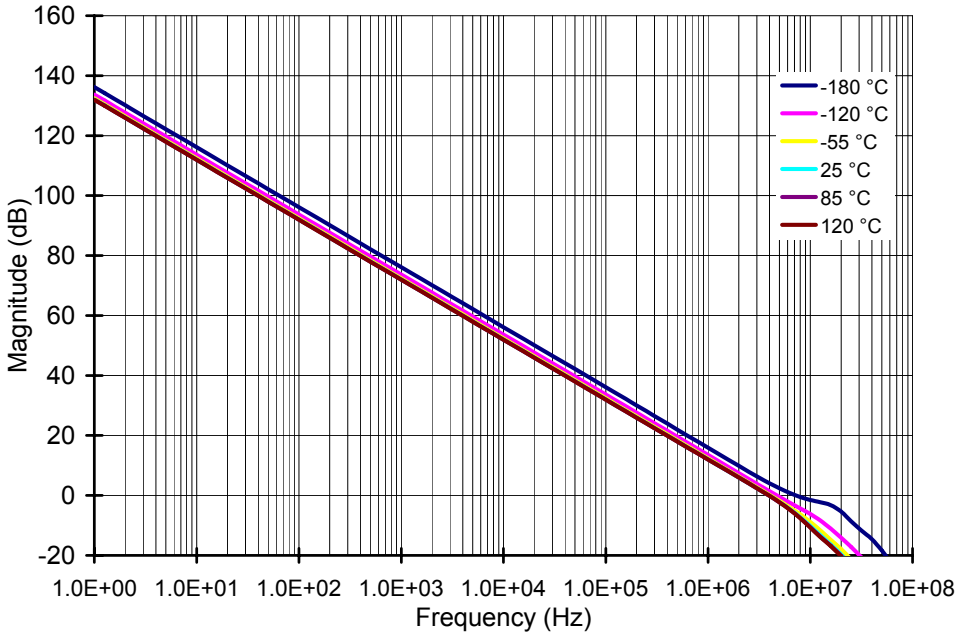


Figure 3-27: Simulated A_{OL}, half power

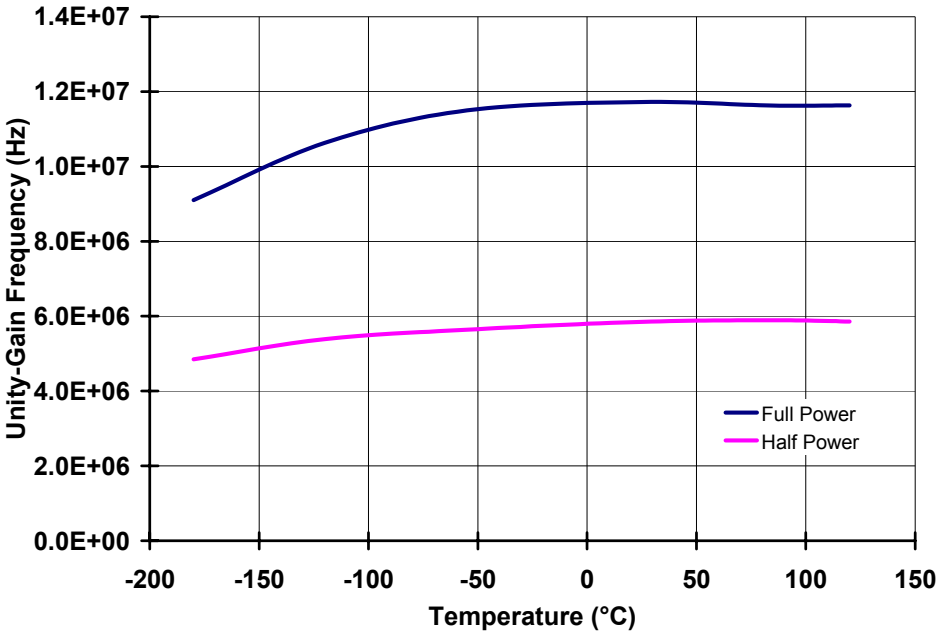


Figure 3-28: Simulated bandwidth

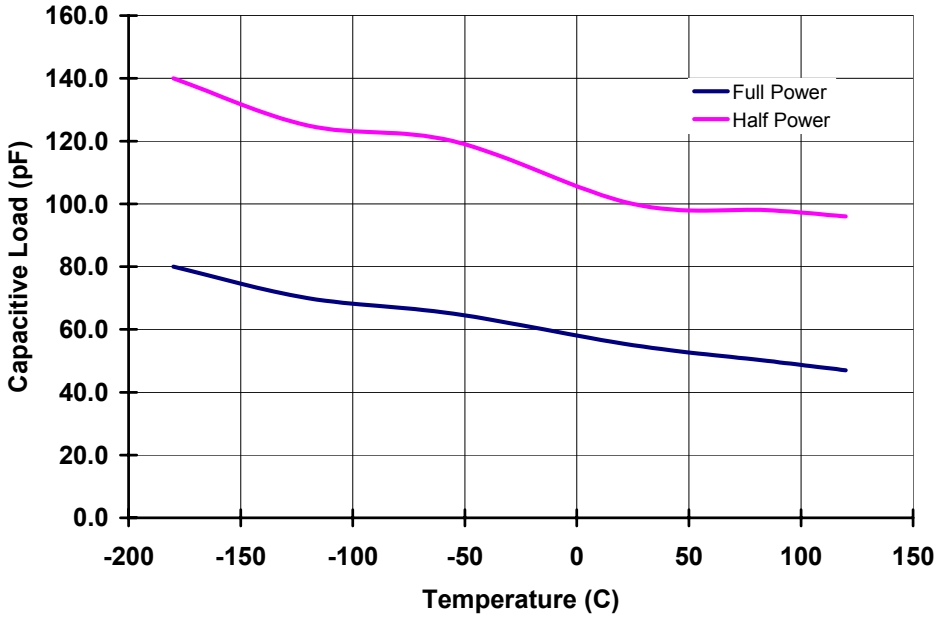


Figure 3-29: Simulated capacitive load for 45° phase margin

The values for the simulated DC power-supply rejection ratio (PSRR) are given in Table 3-2. Similarly, the simulated DC common-mode rejection ratio (CMRR) for both power modes is shown in Table 3-3.

These simulations will be compared to the measured results in the following Chapter.

Table 3-2: Simulated DC PSRR

	Full Power	**Half Power**
120°C	94.00 dB	96.72 dB
85°C	91.16 dB	93.89 dB
25°C	89.94 dB	91.69 dB
–55°C	86.82 dB	89.57 dB
–120°C	85.51 dB	88.23 dB
–180°C	84.82 dB	87.52 dB

Table 3-3: Simulated DC CMRR

	Full Power	**Half Power**
120°C	70.41 dB	70.78 dB
85°C	69.64 dB	69.52 dB
25°C	69.32 dB	69.02 dB
–55°C	69.01 dB	68.73 dB
–120°C	68.77 dB	68.45 dB
–180°C	68.23 dB	67.87 dB

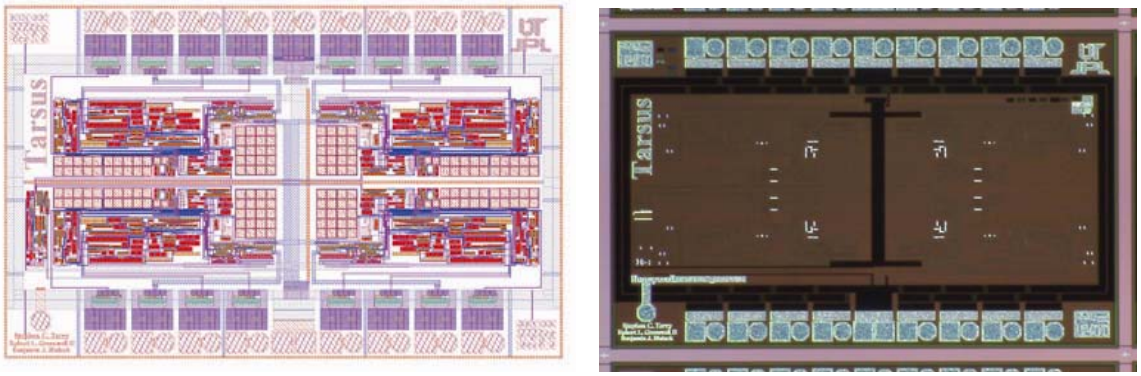
CHAPTER 4

MEASUREMENT RESULTS

Testing Procedures and Results

The fabricated op amp chip, named Tarsus, Figure 4-1, is made up of four identical op amps (a quad op amp chip, or QOA) and a single current reference with separate output current branches feeding each op amp. The op amps each have four input/outputs: V_{IP}, V_{IN}, V_{OUT}, and $V_{CONTROL}$. There are two universal power pads, V_{DD} and V_{SS}, for a total of 18 chip I/O's. Functional measurements performed to verify the performance of the op amp include ICMR, PSRR, offset, A_{OL}, large-signal transient, short-circuit current, and supply current.

Open-loop gain (A_{OL}) was measured with an HP3589 spectrum/network analyzer. The circuit used to make this measurement is shown in Figure 4-2 and an image of the



(a) **(b)**

Figure 4-1: Images of Tarsus QOA chip.
(a) layout overview
(b) fabricated chip

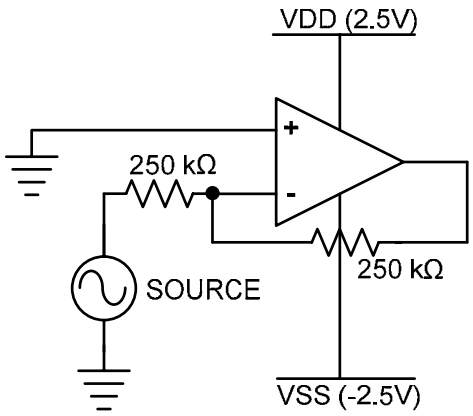


Figure 4-2: A_{OL} test configuration

test board is located in the Appendix, Figure A-1 [8]. The amplifier was placed in a unity-gain inverting configuration, with large feedback resistors in order to minimize loading on the output. A sine wave was created by the source of the HP3589 and is used as the input to the amplifier. The error voltage, V_e, was measured at the negative input terminal of the op amp, and the A_{OL} calculated by dividing the output voltage by the error voltage

$$A_{OL} = \frac{V_{OUT}}{V_e}. \qquad \textbf{(4.1)}$$

The measured open-loop gain in both full power and half power modes, from 50 Hz to 100 kHz, is plotted in Figure 4-3. Limiting the measurement bandwidth can help prevent higher frequency complications caused by capacitive loading on the V_e node by the measurement probe. The measured gain is slightly higher, but consistent, with the simulated performance of the amplifier.

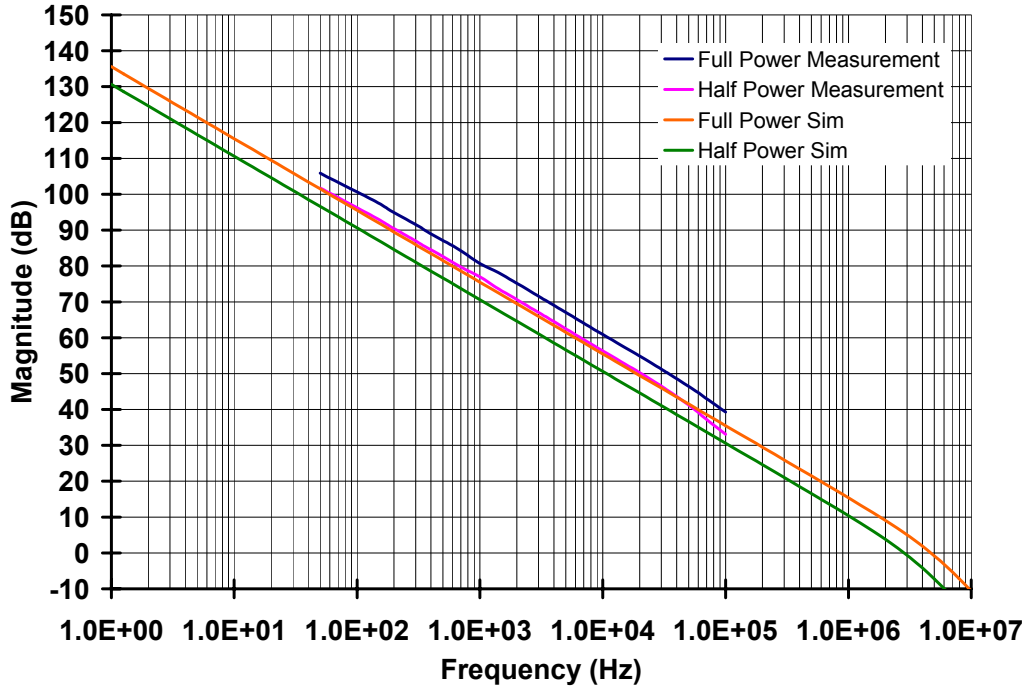


Figure 4-3: Measured A_{OL} vs. simulation, 25°C

The unity-gain bandwidth was measured by placing the op amp in a unity-gain non-inverting configuration, as shown in Figure 4-4. The test board for this configuration is shown in Figure A-2. The bandwidth was found by measuring the rise-time of the small-signal response and calculating bandwidth from the formula

$$GBW = \frac{f_n \tau_r}{small - signal\ risetime}, \tag{4.2}$$

where $f_n\tau_r$ are from [16]. The measurement and simulation results are shown in Figure 4-5. The measured bandwidth of the op amp varies less than 20% from the simulated results.

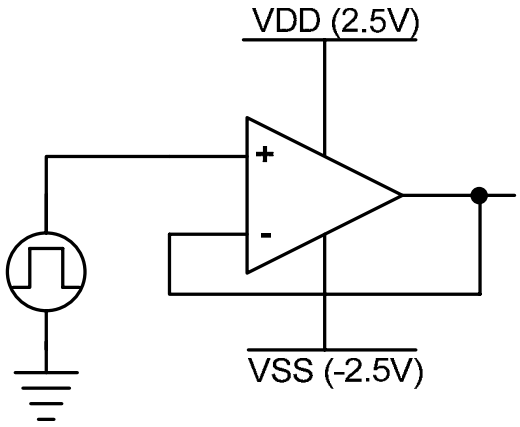


Figure 4-4: Unity-gain non-inverting measurement configuration

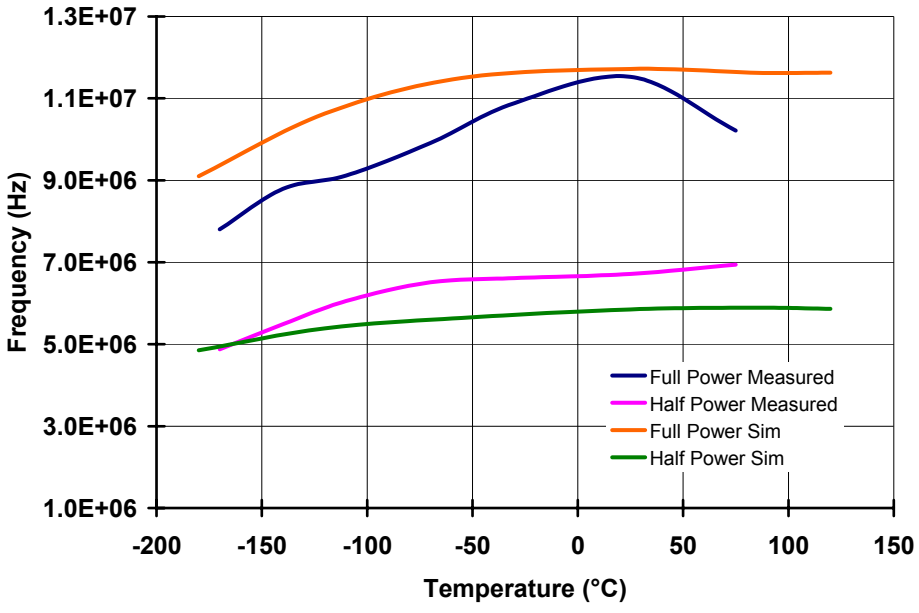


Figure 4-5: Measured GBW over temperature

The capacitive load for 45° phase margin was found by measuring the overshoot of the small-signal response and calculating the phase margin, again from [16]. The results are given in Figure 4-6. Here there is a maximum variation between the measured and simulated results of about 30%. This could be a caused by asymmetry and current mirror mismatch in the output drivers of the output stage (M18, M19, M33 and M25, M26, M27 from Figure 3-7) which could shift the transconductance of the output devices, and therefore the location of the non-dominant pole with respect to the zero, thus shifting the phase response of the amplifier. This effect is supported by the measured short-circuit current which will be discussed later in this section.

The offset of the amplifier was measured by placing the op amp in a unity-gain non-inverting configuration, as shown in Figure 4-4, with the positive input terminal tied

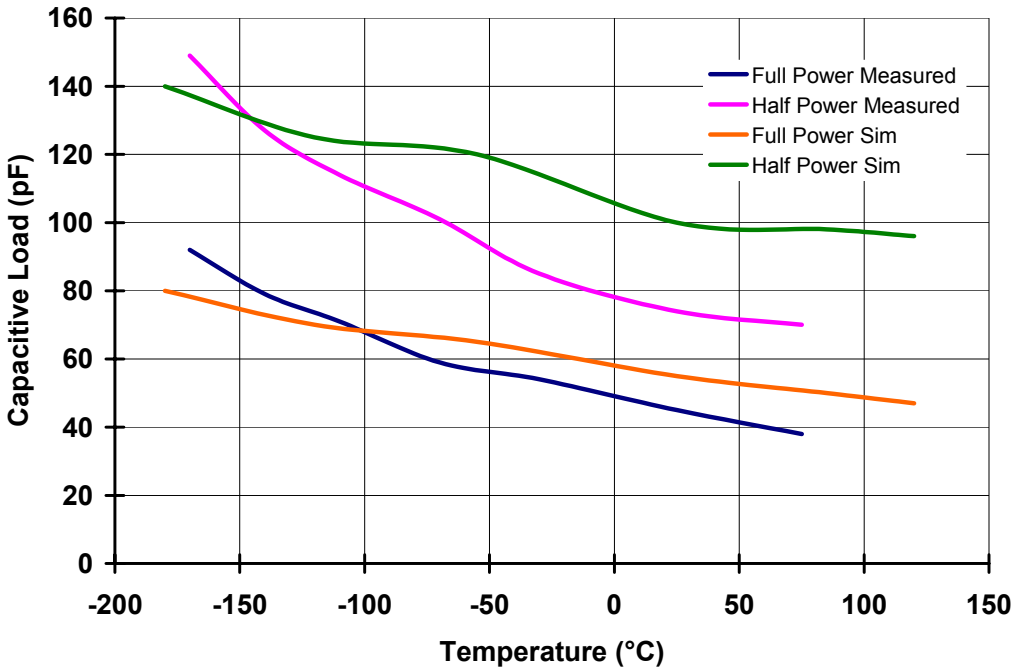


Figure 4-6: Measured capacitive load for 45° phase margin over temperature

to analog ground. The offset was then measured as the difference between the output voltage and analog ground over temperature. The measured offsets of the four op amps from two chips are given in Figure 4-7. Note that the average offset, from –180°C to 120°C, from these measurements is approximately 1.5 mV.

The ICMR was measured by again placing the amplifier in a unity-gain configuration and sweeping the input from rail-to-rail. The measurement results are shown in Figure 4-8, and correspond to a rail-to-rail input and output range. The ICMR does not change noticeably across temperature.

The rising edge of the large-signal transient response across temperature is shown in Figure 4-9 and Figure 4-10 for full and half power modes, respectively. For this measurement, the op amp was placed in a unity-gain configuration, with a 4-V_{P-P} input

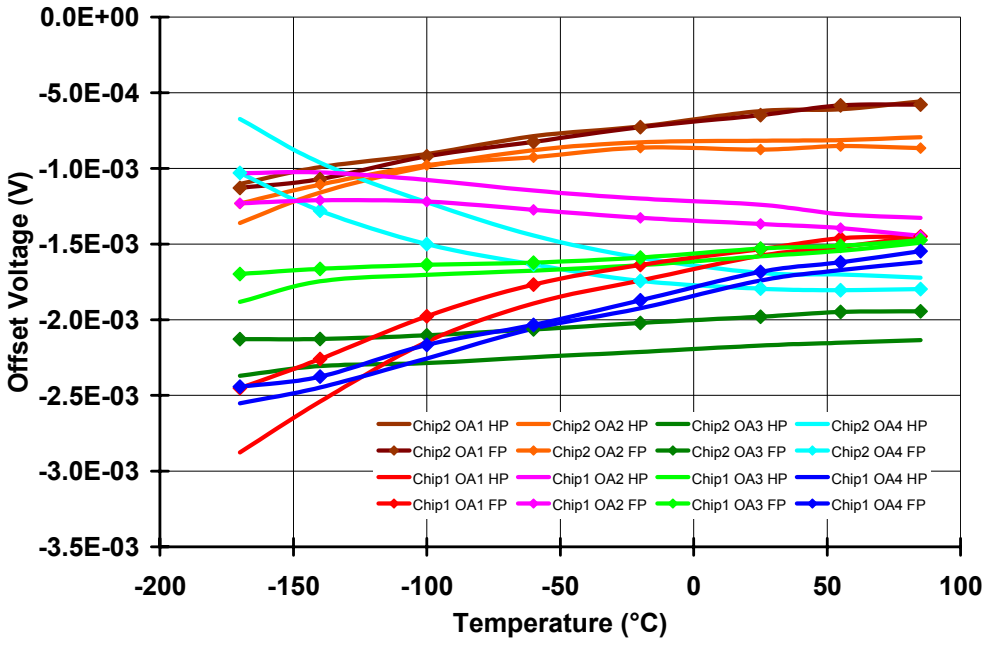


Figure 4-7: Measured offset vs. temperature

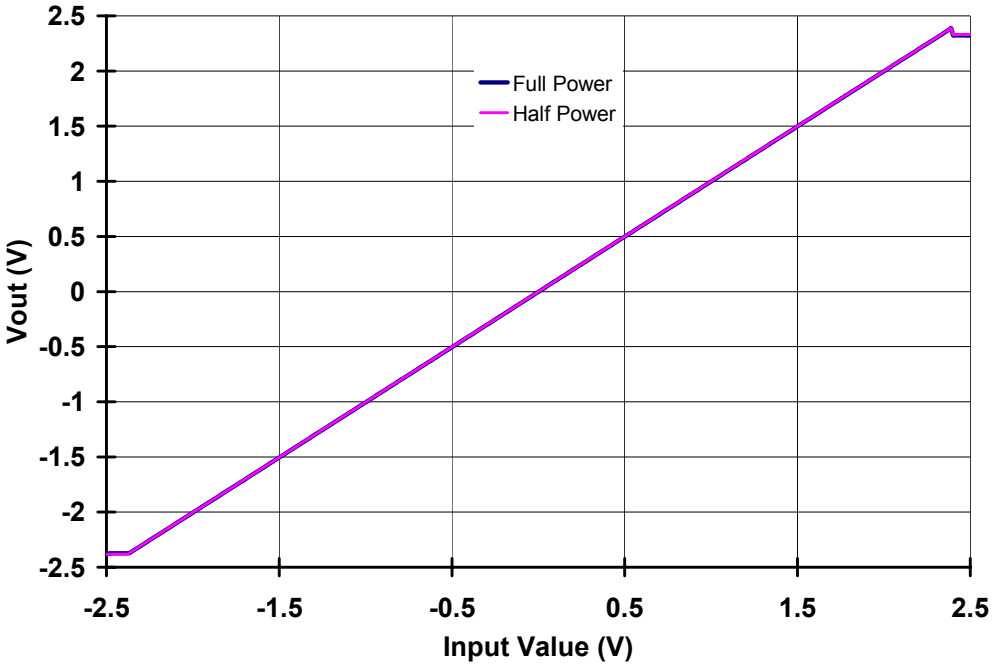


Figure 4-8: ICMR Measurement, 25°C

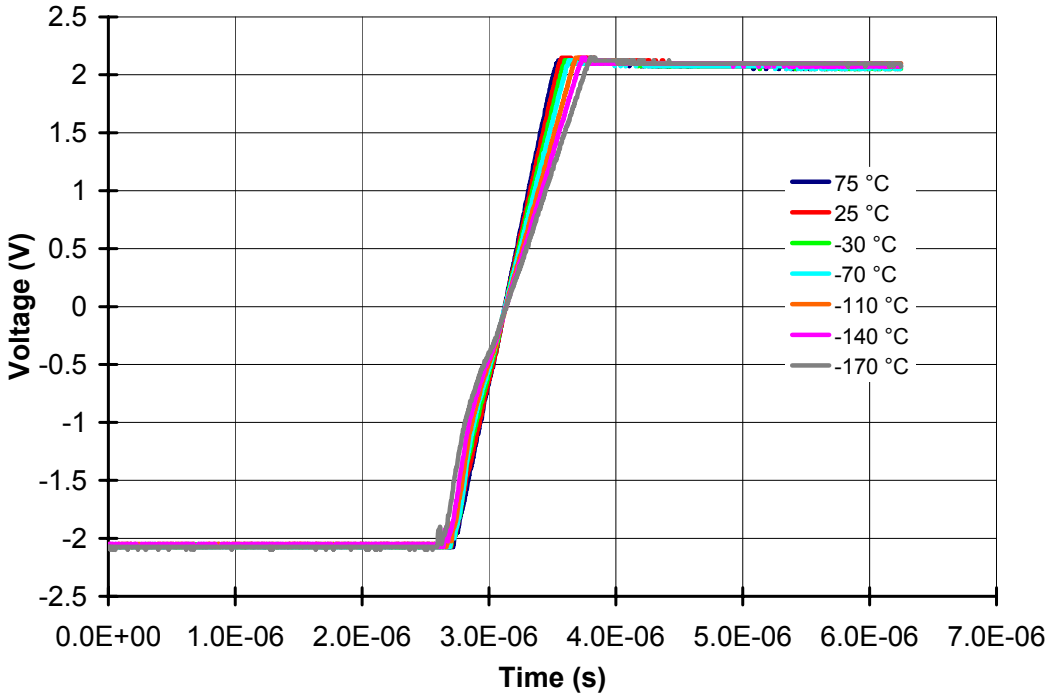


Figure 4-9: Measured large-signal transient response, full power

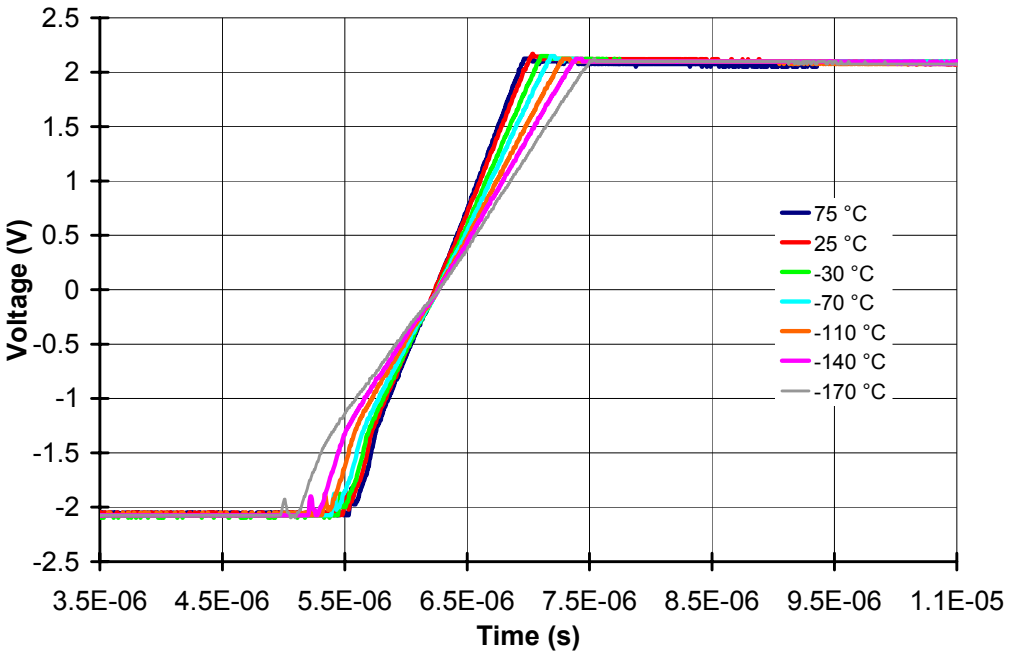


Figure 4-10: Measured large-signal transient response, half power

signal. Figure 4-11 shows the slew-rate vs. temperature and operating mode of the op amp for the large-signal response. This data agrees well with the simulated results presented in Chapter 3.

The short circuit output current was measured by placing the op amp in the configuration shown in Figure 4-4, and shorting the output to V_{SS}. The measured current is given in Figure 4-12. Similar to Figure 4-6, there is a noticeable discrepancy between measured and simulated results. The current mirror mismatch mentioned for the phase margin discrepancy would also apply here, especially given that any current or device mismatch would be accentuated during large-single events, such as short-circuit current drive.

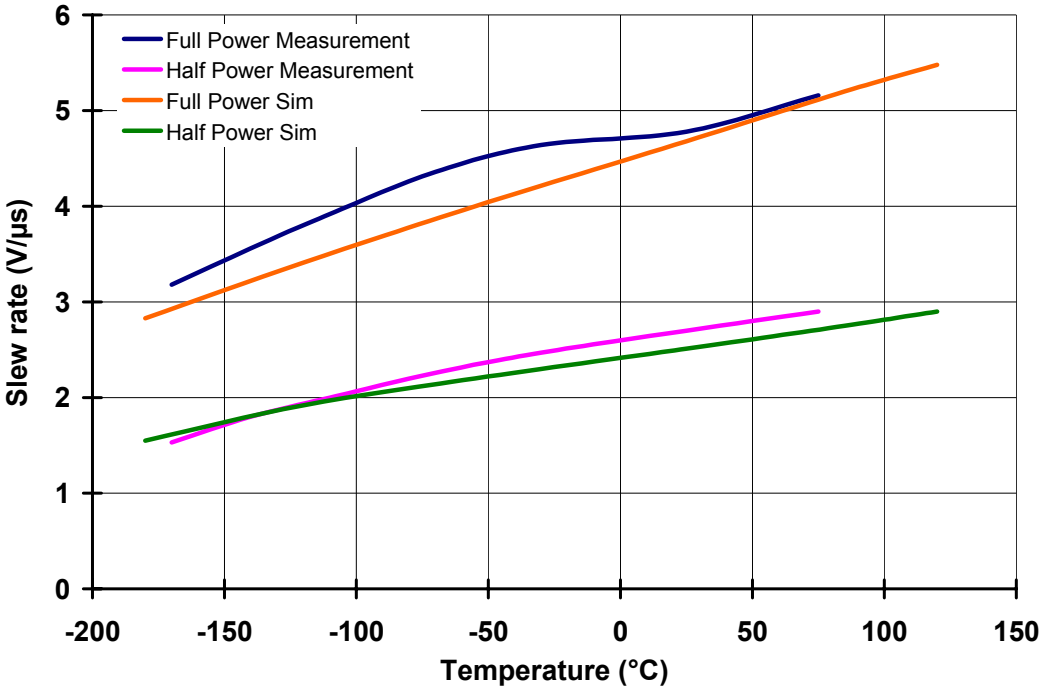


Figure 4-11: Measured slew rate vs. temperature

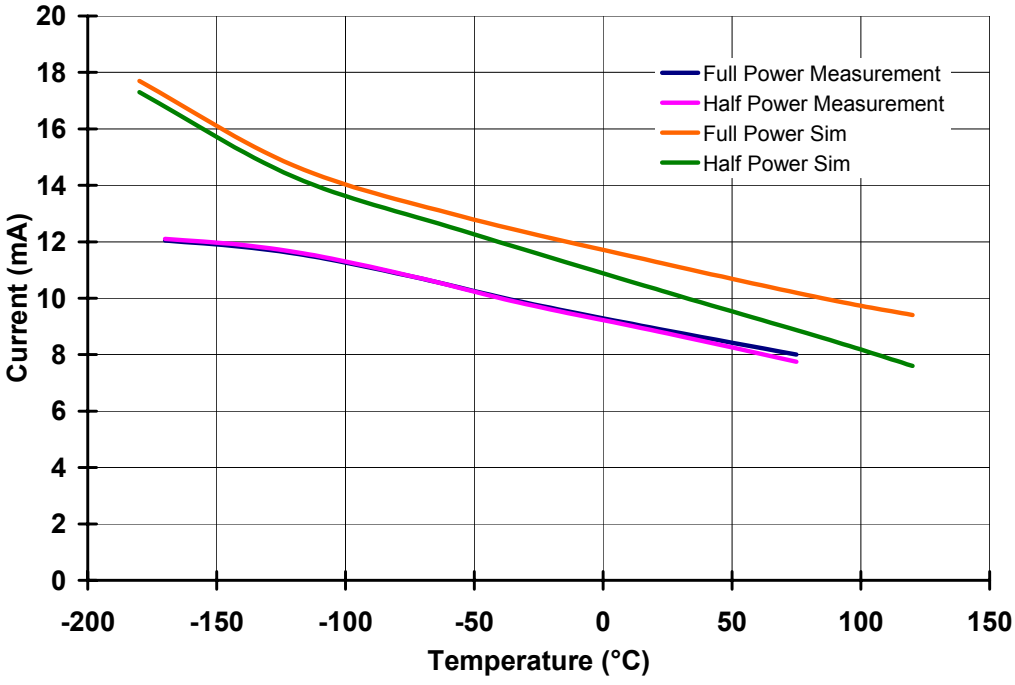


Figure 4-12: Measured short-circuit current vs. temperature

Figure 4-13 contains the current consumption of a QOA chip running with a 5-V supply. For this measurement, each of the four op amps are tied in a unity-gain non-inverting configuration, with their positive input terminals tied to analog ground, and no load on the output. Half and full power modes demonstrate the expected behavior in that half power mode utilizes nearly half the current of full power mode, which is consistent with other measurements and the fact that the current into each branch of each op amp is being halved.

PSRR is measured by placing an op amp in a unity-gain configuration as shown in Figure 4-14, and varying the power supply voltage while measuring the offset. Then, the DC PSRR can by calculated as

$$DC\_PSRR = \frac{dV_{POWER\_RAILS}}{dV_{OUT}}. \tag{4.3}$$

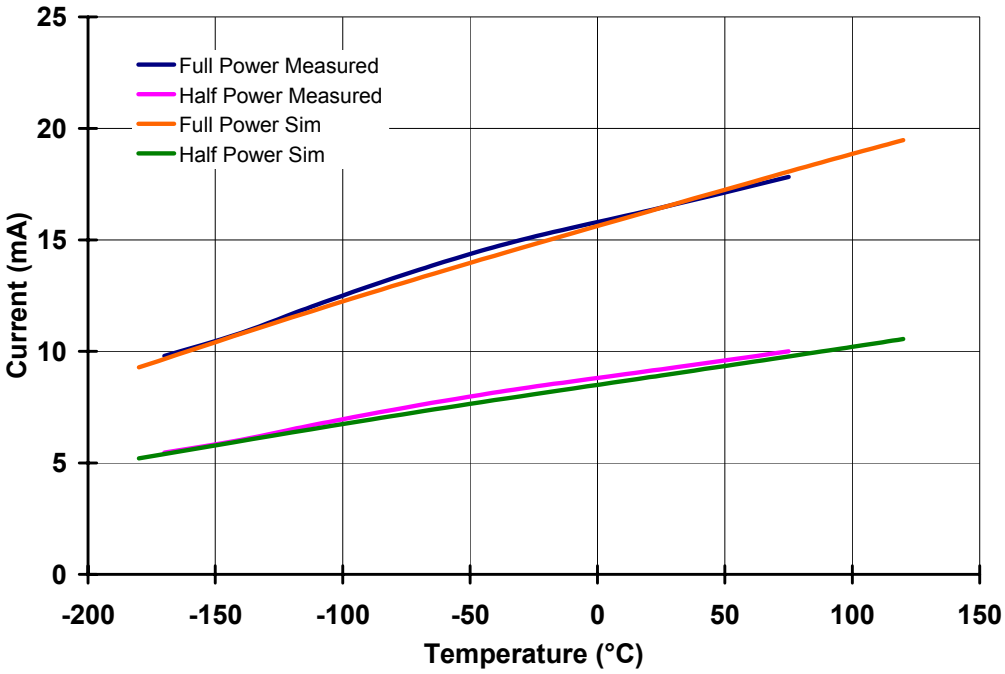


Figure 4-13: Measured QOA chip current consumption vs. temperature

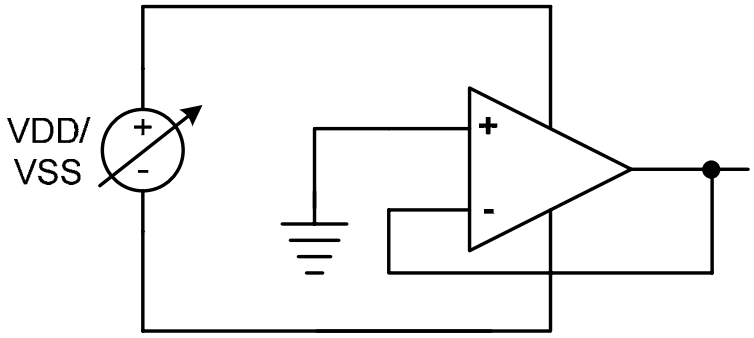


Figure 4-14: Circuit for measuring PSRR

The resulting measurements are given in Figure 4-15. These results compare well with the simulated values from Chapter 3, Table 3-2.

The circuit given in Figure 4-16 was utilized for measuring the CMRR [8]. This circuit allows the output of the DUT to be held at mid-supply, so that any change in the output voltage could be attributed to a change in the input offset voltage. However, during testing it was determined that it is more reliable to take the offset voltage measurement directly at the input terminals of the DUT. The equation to obtain the DC CMRR is

$$DC\_CMRR = \frac{dV_{CM}}{dV_{ID}} \tag{4.4}$$

where V_{ID} is the measured voltage between the DUT's input terminals. Figure 4-17 shows the measured DC CMRR. Again, these measurement results agree well with the simulated values given in Chapter 3.

Overall, the measurement results show an amplifier that operates as designed, across a wide temperature range, and whose results agree well with the simulations results.

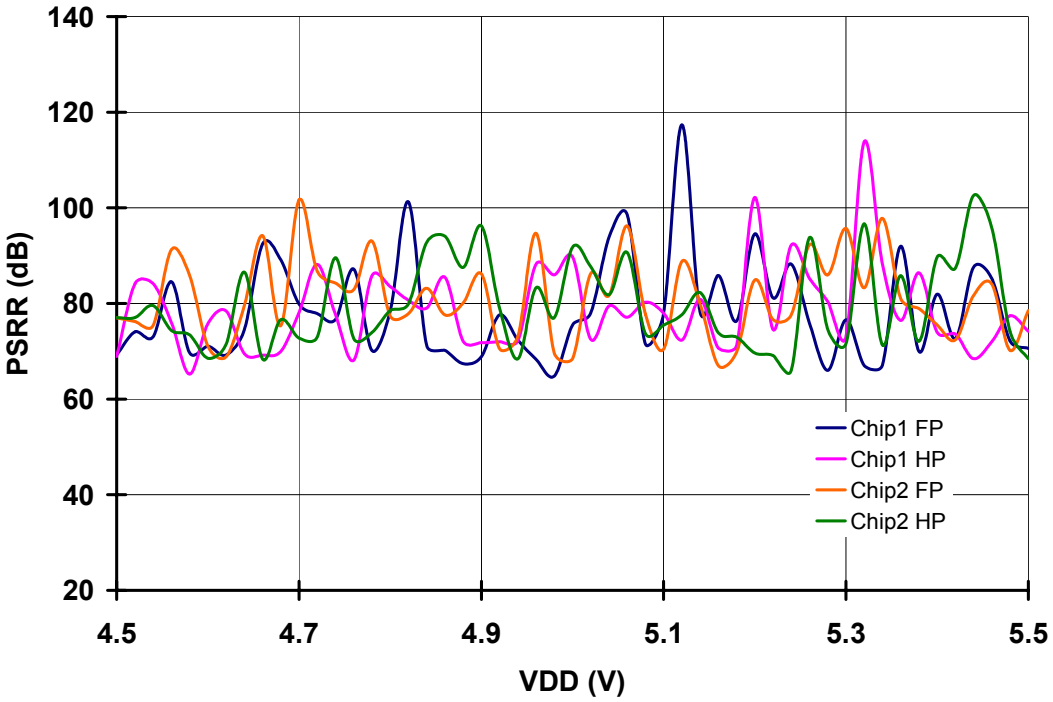


Figure 4-15: Measured DC PSRR, 25°C

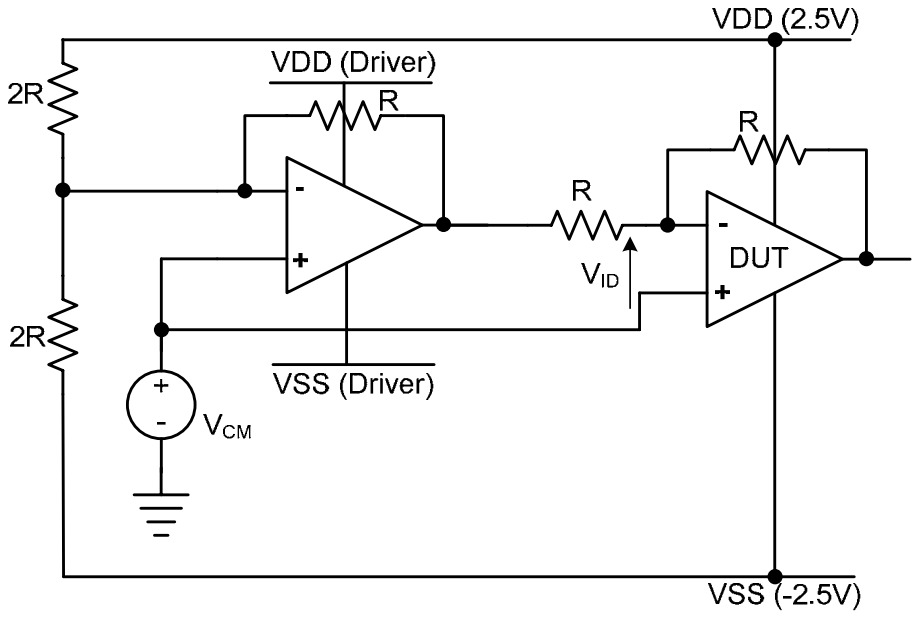


Figure 4-16: Circuit for measuring CMRR

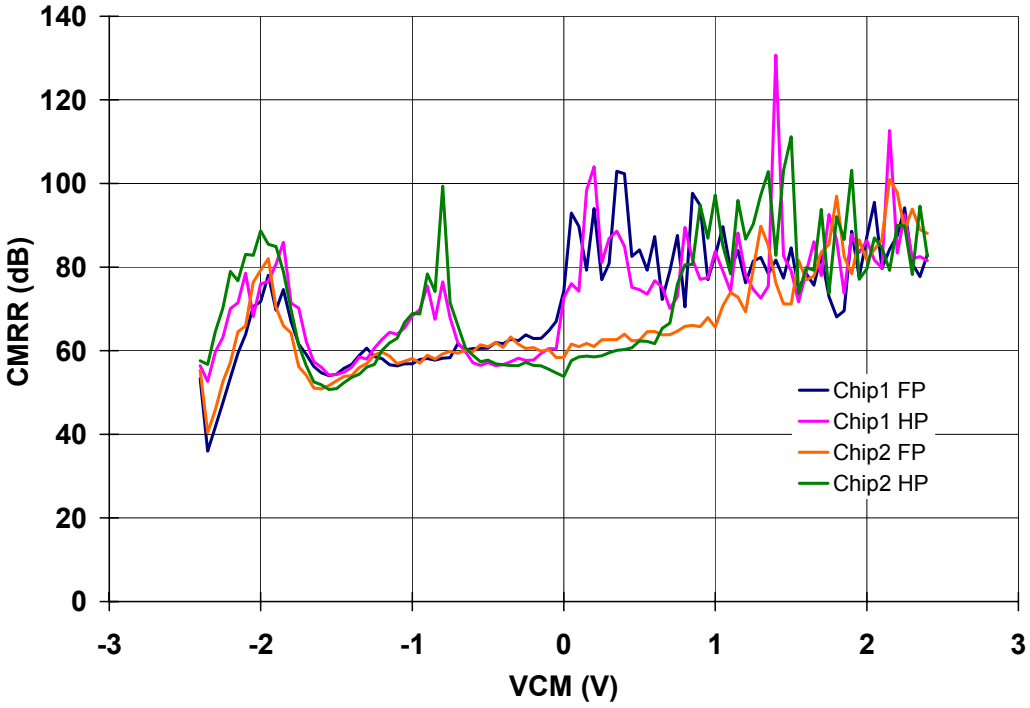


Figure 4-17: Measured DC CMRR, 25°C

CHAPTER 5

CONCLUSIONS

Conclusions

This thesis presented the design and analysis of a 5-V compatible op amp fabricated in a 3.3-V PDSOI process. The op amp has a rail-to-rail ICMR, a rail-to-rail output swing, high gain, and low offset. It is capable of sourcing relatively large currents, and can drive capacitive loads.

Temperature testing has shown that the op amp performs as expected across its intended range of operation, from −180°C to 120°C. Additionally, it is shown that the constant-IC current reference is capable of generating a constant MOSFET inversion coefficient current across this operating range, and that this type of current reference is well suited for biasing CMOS analog circuits operating across broad temperature ranges.

Future Work

Although it has been demonstrated that the op amp performance is very close to the target design parameters, further verification must be carried out before its long-term reliability can be assured. For example, oxide breakdown and hot carrier effects, as discussed in Chapter 2, have an accumulating effect. Although neither of these high voltage effects has been seen here, it does not ensure proper operation over the lifetime of the part. Consequently, additional testing will most likely take the form of burn-in and

flight qualification testing to be conducted at the Jet Propulsion Laboratory. This testing will help assure that, although great care was taken in the design to protect the devices in the op amp from excessive voltage levels, no breakdown effects are at work.

Additionally, there was a discrepancy observed between simulated and measured phase margin. It was found that simulating the op amp with EKV models, as opposed to BSIM3 models, gave results much closer to the measured values for the phase margin. Understanding why these two models provide different results, and why the phase margin did not match with BSIM3 simulation, may be important to further understanding the functionality of the op amp.

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APPENDIX

System Equations

The open-loop gain can be approximated as the gain of the input stage times the gain of the output stage

$$A_{OL} = A_{preamp} \times A_{output} \quad \textbf{(A.1)}$$

First, looking at the input stage, the gain is equal to the transconductance of the input pair times the output resistance

$$A_{preamp} = g_m \times r_o = g_{m,input\ pair} \times r_{output} \quad \textbf{(A.2)}$$

The transconductance of the input pair is (from Figure 3-5)

$$g_{m,input\ pair} = g_{m,M56} + g_{m,M58} \quad \textbf{(A.3)}$$

This is approximated by

$$g_{m,input\ pair} = \sqrt{2 \times \beta_{M56} \times I_D} + \sqrt{2 \times \beta_{M58} \times I_D} \quad \textbf{(A.4)}$$

$$g_{m,input\ pair} = \sqrt{2 \times KP_N \times \left(\frac{W}{L}\right)_{M56} \times I_D} + \sqrt{2 \times KP_P \times \left(\frac{W}{L}\right)_{M58} \times I_D}$$

$$g_{m,input\ pair} = \sqrt{2 \times 37.46 \times 10^{-6} \times \left(\frac{10}{2} \times 32\right)_{M56} \times 21 \times 10^{-6}} + \ldots$$

$$\ldots + \sqrt{2 \times 16.6 \times 10^{-6} \times \left(\frac{20}{2} \times 32\right)_{M56} \times 21 \times 10^{-6}}$$

$$g_{m,input\ pair} = 9.74 \times 10^{-4}\ \text{S}$$

The output resistance can be found as the parallel resistance seen looking into the regulated folded cascode output of the first stage. The resistance is made up of the upper and lower half of the regulated cascode.

$$r_{output} = R_{reg\_top} \| R_{reg\_bottom} \tag{A.5}$$

This becomes [6]

$$r_{output} = \left[\left(r_{o,M33}\left(1 + g_{m,M33} r_{o,M61}\right) + r_{o,M61}\right) \times A_{M34}\right] \| \ldots \tag{A.6}$$

$$\ldots \left[\left(r_{o,M43}\left(1 + g_{m,M43} r_{o,M64}\right) + r_{o,M64}\right) \times A_{M44}\right],$$

where A_{M34} and A_{M44} are the gains associated with the source follower amplifier M34 and M44 in the regulated cascode (see Figure 3-5). This equation can be simplified to

$$r_{output} = \left[\left(g_{m,M33} r_o^{\,2}\right)\left(g_{m,M34} r_{o,M34}\right)\right] \| \left[\left(g_{m,M43} r_o^{\,2}\right)\left(g_{m,M44} r_{o,M44}\right)\right] \tag{A.7}$$

Because the quiescent bias current is identical, the output resistance of each device can be assumed to be approximately equal. Also, M33 and M34 are matched devices, so the previous equation becomes

$$r_{output} = \left(g_{m,M33}^{\,2} r_o^{\,3}\right) \| \left(g_{m,M43}^{\,2} r_o^{\,3}\right) \tag{A.8}$$

Evaluating the result provides

$$r_{output} = \left(\sqrt{2 \times 16.6 \times 10^{-6} \times \left(\frac{20}{2} \times 8\right)_{56} \times 21 \times 10^{-6}}\right)^2 \times \left(\frac{1}{.06 \times 21 \times 10^{-6}}\right)^3 \Bigg\| \ldots \tag{A.9}$$

$$\ldots \left(\sqrt{2 \times 37.46 \times 10^{-6} \times \left(\frac{10}{2} \times 8\right)_{56} \times 21 \times 10^{-6}}\right)^2 \times \left(\frac{1}{.06 \times 21 \times 10^{-6}}\right)^3$$

$$r_{output} = \left(2.36\times10^{-4}\right)^2 \times \left(7.94\times10^{5}\right)^3 \left\| \left(2.51\times10^{-4}\right)^2 \times \left(7.94\times10^{5}\right)^3 \right.$$

$$r_{output} = 1.478\times10^{10}\ \ \Omega$$

Therefore, A_{preamp} is equal to

$$A_{preamp} = g_{m,input\ pair} \times r_{output} = 1.44\times10^{7}\ \text{V/V} \qquad \textbf{(A.10)}$$

The gain of the second stage is approximated as

$$A_{output} = g_{m,input} \times r_{output} \qquad \textbf{(A.11)}$$

$$A_{output} = g_{m,M16} \times r_{top} \left\| r_{bottom} \right.$$

Evaluating this formula yields

$$A_{output} = \left(\sqrt{2\times16.6\times10^{-6} \times \left(\frac{5}{1.2}\times8\right)_{56} \times 21\times10^{-6}} \right) \times \ldots \qquad \textbf{(A.12)}$$

$$\ldots \left[\left(\frac{1}{.06\times10\times10^{-3}} \right) \left\| \left(\frac{1}{.06\times10\times10^{-3}} \right) \right. \right]$$

$$A_{output} = 1.52\times10^{-4} \times 833 = 1.27\times10^{-1}\ \text{V/V}$$

And now the approximate open loop gain can be found

$$A_{OL} = A_{preamp} \times A_{output} = 1.44\times10^{7} \times 1.52\times10^{-4} \times 833\ \text{V/V} \qquad \textbf{(A.13)}$$

$$A_{OL} = 1.83\times10^{6} = 125\ \text{dB}.$$

Next, slew-rate may be described by [17]

$$SR = \frac{I_{SS}}{C_C} = \frac{2\times42\times10^{-6}}{20\,pF} = 4.2\ \text{V/µs}. \qquad \textbf{(A.14)}$$

And gain bandwidth is equal to

$$GBW = A_{OL} \times f_{-3dB}\,. \tag{A.15}$$

$$GBW = A_{OL} \times \frac{1}{2 \times \pi \times r_{out,preamp} \times C_{out,preamp}} \tag{A.16}$$

Substituting in the values

$$GBW = 1.83 \times 10^{6} \times \frac{1}{2 \times \pi \times 1.478 \times 10^{10} \times 2 \times 10^{-12}} \tag{A.17}$$

$$GBW = 9.85 \text{ MHz.}$$

The phase margin is estimated by first calculating the poles and zeros of the system. The first and second poles can be approximated by [17];

$$p_1 \cong \frac{1}{g_{m,M40} \times r_{o,preamp} \times r_{o,output} \times C_C} \tag{A.18}$$

$$p_1 \cong \frac{1}{3.99 \times 10^{-4} \times 1.47 \times 10^{10} \times 833 \times 20 \times 10^{-12}} \cong 10.2 \text{ Hz}$$

$$p_2 \cong \frac{g_{m,M40}}{C_L} \tag{A.19}$$

$$p_2 \cong \frac{3.99 \times 10^{-4}}{C_L}$$

And if we assume that the zero-compensation resistor R_Z is equal to $1/g_{m,M40}$ (Figure 3-7)

$$z_1 \cong \frac{1}{C_C\left(\frac{1}{g_{m,M40}} - R_Z\right)} \cong \infty \qquad \textbf{(A.20)}$$

And now phase margin can be approximated as

$$PM = 180 - \tan^{-1}\left(\frac{GBW}{p_1}\right) - \tan^{-1}\left(\frac{GBW}{p_2}\right) \qquad \textbf{(A.21)}$$

We may solve for C_L for 45° of phase margin

$$PM = 180 - \tan^{-1}\left(\frac{9.85\times10^6}{10.2}\right) - \tan^{-1}\left(\frac{9.85\times10^6}{3.99\times10^{-4}/C_L}\right) \qquad \textbf{(A.22)}$$

$$PM \cong 45^\circ \text{ for } C_L \cong 40 \text{ pF}$$

Test Boards

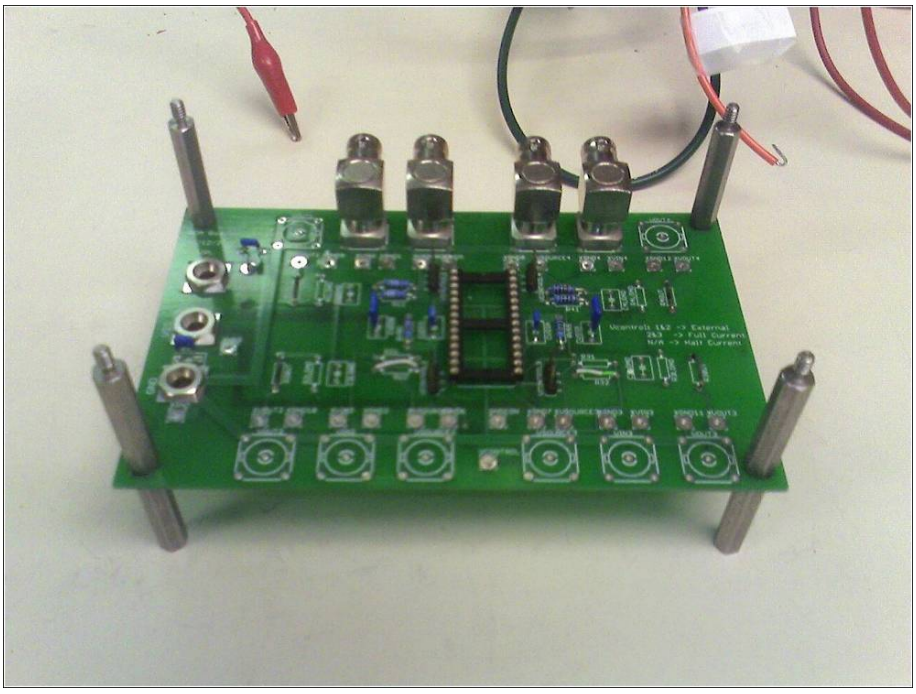

Figure A-1: A_{OL} test board

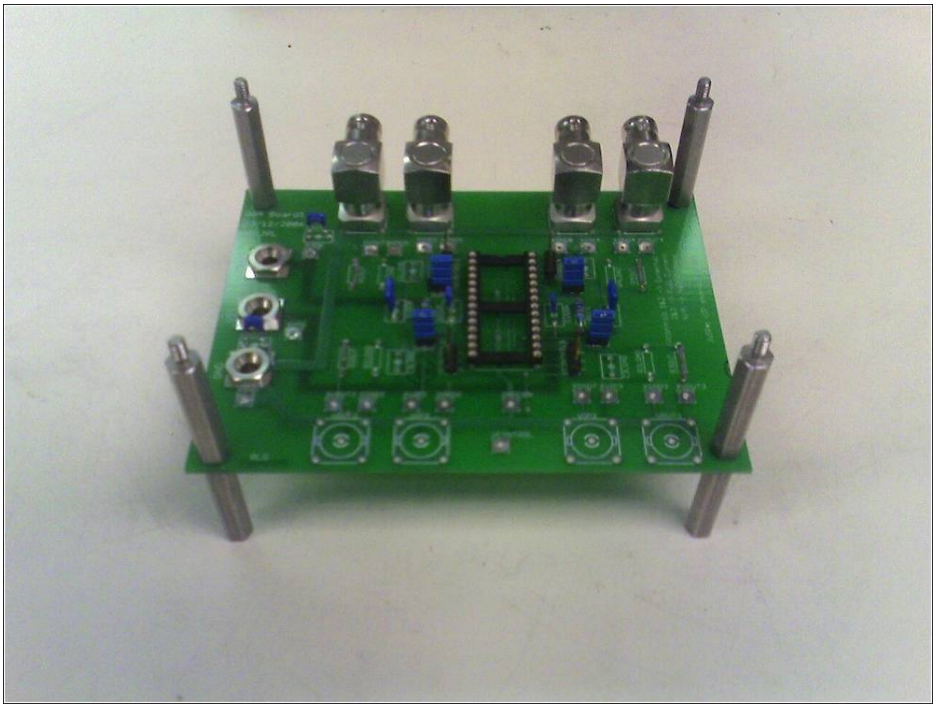

Figure A-2: Unity-gain test board

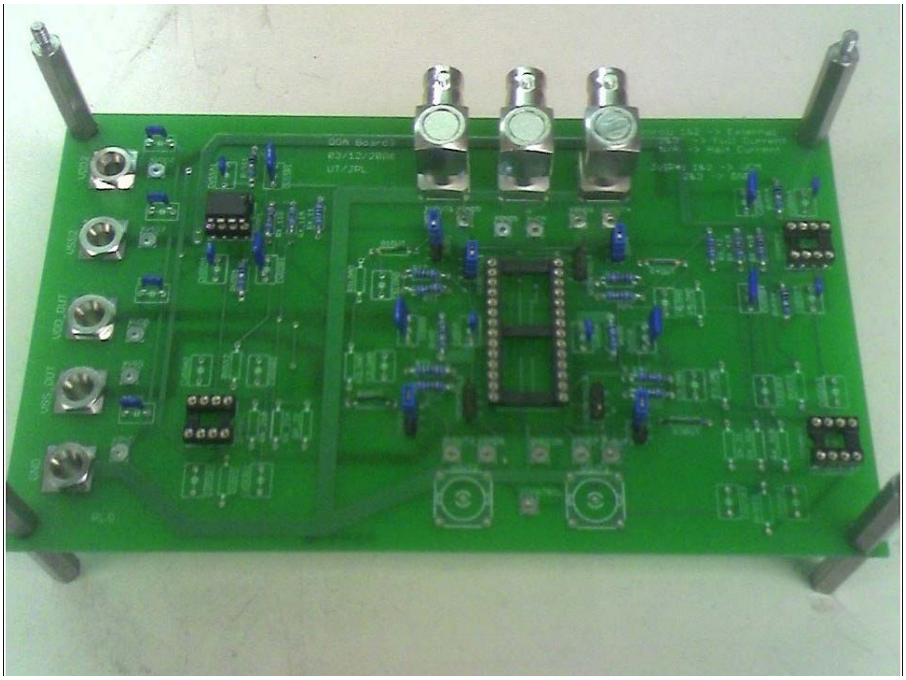

Figure A-3: CMRR test board

VITA

Robert Greenwell was born in Garden City, Michigan on October 29, 1980. He grew up in Dearborn Heights, Michigan before moving to Jonesborough, Tennessee, where he graduated from David Crockett High School in 1999. Robert then entered the University of Tennessee, and graduated with a Bachelor of Science in Electrical Engineering in 2003, Magna Cum Laude. During this time Robert worked as an undergraduate research assistant at the Oak Ridge National Laboratory, and at the Integrated Circuits and Systems Laboratory at the University of Tennessee.

After obtaining his undergraduate degree, Robert began work on his Masters of Science in Electrical Engineering at the University of Tennessee in the Integrated Circuits and Systems Laboratory under the direction of Dr. Benjamin Blalock.