12-2013

An On-Chip Transformer-Based Digital Isolator System

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To the Graduate Council:

I am submitting herewith a thesis written by Cory Lynn Fandrich entitled "An On-Chip Transformer-Based Digital Isolator System." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

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An On-Chip Transformer-Based Digital Isolator System

A Thesis Presented for the
Master of Science
Degree
The University of Tennessee, Knoxville

Cory Lynn Fandrich
December 2013

DEDICATION

I dedicate this work to my parents, David and Joy, and my wife, Abbie, for their constant love and encouragement.

ACKNOWLEDGEMENTS

I would like to thank my advisor Dr. Benjamin Blalock for the opportunity to pursue graduate school. His guidance and enthusiasm made my time as a research assistant a very positive experience. I would like to thank my other committee members Dr. Leon Tolbert and Dr. Jeremy Holleman for their support as I completed this research. The Integrated Circuits and Systems Laboratory research group has also been a huge source of knowledge and support during my time in graduate school.

I would also like to thank my family and friends. My parents, David and Joy Fandrich, have always supported my academic and other pursuits. My wife, Abbie, is my daily encouragement and inspiration.

ABSTRACT

An on-chip transformer-based digital isolator has been designed, fabricated, and tested. This isolation technique is designed to function between a low voltage microcontroller and a potentially high-voltage power control system. The isolator's isolation capability is determined by two factors, the RMS blocking voltage strength and common-mode transient immunity. The integrated circuit solution is designed in a high-temperature capable SOI process.

The on-chip transformer size is minimized by utilizing high frequency voltage pulses. A small transformer and overall small chip footprint of the design are favorable for integration into a larger system. The isolator is a two chip solution, an isolated transmitter and receiver. The transformer's primary and secondary coils are fabricated with chip metal interconnect. The transformer is located on the transmitter chip. The secondary coil of the transformer is electrically isolated from the transmitter circuitry by an insulating oxide layer and is wire bonded off the transmitter chip and onto the receiver chip.

The isolator chips have been fabricated and bonded directly to printed circuit boards. The isolator has been experimentally tested with an input frequency as high as 5 MHz, or 10 Mbps. The isolator functions up to 150°C. The isolation capability has been experimentally verified at 8 kV/μs common-mode rejection and at 700-V RMS voltage breakdown.

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CHAPTER I
INTRODUCTION AND MOTIVATION

Galvanic isolation is the insulation of electrical systems to deny direct current flow. This isolation is needed in many different applications to protect against dangerous voltages or currents. Power electronics in home appliances, vehicles, and industrial equipment present a wide need for isolators to protect people and adjacent electronics [1]. The motivation for this thesis is from research of a power control system for hybrid electric vehicles (HEVs).

Digital Isolator for Power Control Systems

An integrated power module for hybrid electric vehicle (HEV) motor drives is being researched to take advantage of wide-bandgap power switches. An example motor drive is shown in Figure 1. Each of the three phase legs contains two power switches that are controlled by a gate driver. When the high-side switch of a phase leg is turned ‘on’, the high-side gate driver’s low supply rail will swing from a low voltage to the DC bus voltage that is hundreds of volts. The microcontroller (MCU) operates with logic level voltages from zero to five volts. The MCU must be isolated from the potentially high-voltage domain of the gate driver.

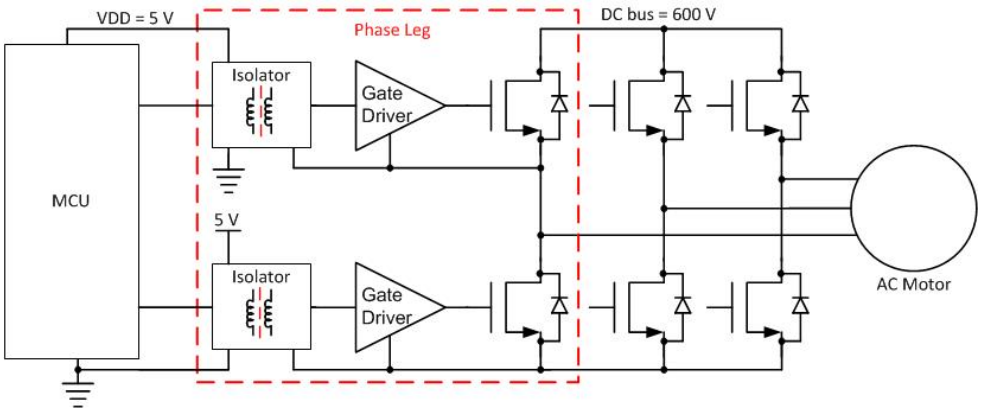

Figure 1. Three-phase inverter

The isolator must block the static voltage potential from the low-voltage domain up to the DC bus voltage when the high-side switch is turned 'on'. Also, the isolator must reject the dV/dt, or common-mode noise, of the node connecting the two transistors of a phase leg. This common-mode noise is on the order of tens of kV/μs. An isolator is also needed for the low-side power switch to completely isolate the microcontroller from any high-voltage feedback through parasitic capacitances in the system.

The integrated power module project is also pushing for high temperature operation. This high temperature refers to the temperature region found near the engine in automobiles; this location under the hood of a vehicle can be in excess of 175°C [2]. The electronics for the power module are targeting operation with the aid of the standard 105°C cooling loop. The isolator and gate driver for the power module are designed in a silicon-on-insulator (SOI) chip technology capable of operation in excess of 200°C. The chip technology is a bipolar-CMOS-DMOS or BCD process. The isolator design is almost exclusively CMOS, but there are a few bipolar transistors used also.

The remaining content of this thesis is separated into four chapters. Chapter II of this thesis is a survey of typical digital isolator systems. The survey covers the main types of isolators and reports the performance results of each type. Chapter III is a design review. This design review covers the circuit topology, on-chip transformer design, simulation results, and expected isolation capability. Chapter IV details the experimental test setup and results. Chapter V gives a conclusion, comparison to previous isolator systems, and the direction of future work.

CHAPTER II
ISOLATOR TECHNOLOGIES

Three of the main digital isolator techniques are optocouplers, capacitive isolators, and transformer-based isolators. Optocouplers use light-emitting diodes (LEDs) and photodetectors to send and receive information across an insulating barrier. Capacitive isolators block direct current (DC) from flowing across the dielectric between two conductors. Only alternating current (AC) signals may transfer across a capacitor. Galvanic isolation is also achieved from transformers. Insulation between two coils provides isolation, and the desired AC signal is transferred through inductive coupling.

The isolation strength of these techniques is tested independent of isolation mechanism. The isolators are treated as two terminal devices. All nodes on the input side are connected together, and all nodes on the output side are connected together. One standard test is a stress test that applies a high voltage across the insulating dielectric to determine the maximum operating RMS voltage and failure point [1].

Common-mode rejection (CMR), or common-mode transient immunity (CMTI), is a second benchmark for isolators. Transient immunity is needed to reject high frequency noise present in the system. This noise is transferred through capacitances across the isolation barrier in isolators [1]. The transferred noise can cause an incorrect output state. CMR is reported in units of kV/μs. Depending on the technology used, this noise is handled in different ways.

Optocoupler Isolation

Optocouplers are one type of digital isolators. An electrical signal is passed into a LED to generate a source of light. This light travels across an insulating barrier and contacts a photodetector. The photodetector and additional circuitry create an electrical output signal based on the incoming light. The LED and photodetector are insulated to block direct current.

An example of the construction of an optical isolator is shown in Figure 2 [3]. The physical construction of optical isolators enhances common-mode rejection. A Faraday shield at the photodetector enhances CMR by coupling high frequency noise to ground. Also, the LED junction capacitance of about 80 pF improves immunity to high frequency noise [4]. An Avago Technologies optocoupler with internal shield reports 3.75 kV RMS operation, 15 kV/μs CMR, and 10 Mbps [5].

Optical isolators have many advantages. The isolation benchmarks of RMS blocking voltage and common-mode rejection are generally high for optocouplers. Optocouplers are highly resistive to external electric and magnetic fields. However, there are a few disadvantages also. Speed limitations, high power dissipation, and LED degradation are drawbacks of optocouplers. LEDs typically require 10 mA of current at a high data rate. With long-term use, the same current level produces less light, and eventually the isolator may stop functioning [1]. Integration is another disadvantage of optocouplers. Semiconductor materials such as gallium arsenide (GaAs) are used to make LEDs. These materials cannot be directly integrated with a microcontroller or gate drive chip [6].

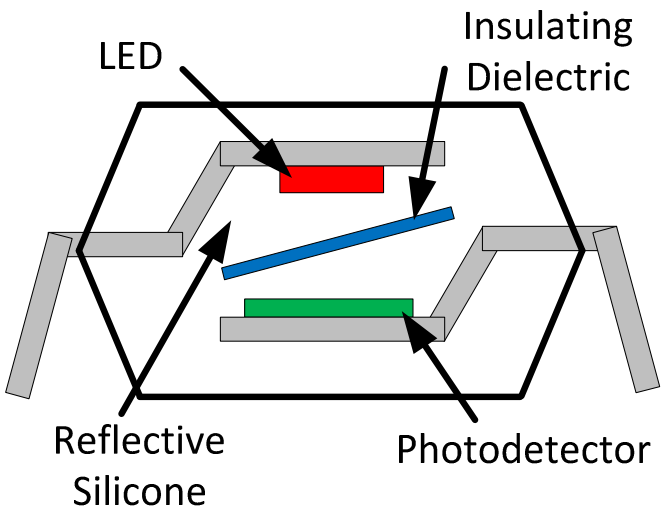

Figure 2. Optocoupler package diagram [3]

Capacitive Isolation

Capacitive isolation is another way to insulate high voltage systems. A fundamental aspect of capacitors is the ability to block direct current. The changing electric field from a high frequency signal allows the signal to be transferred across the insulating dielectric. The CMR of capacitive isolators is an issue because the common-mode noise and desired signal share the same signal path. Therefore, the desired signal must be at higher frequencies than the transient noise. Two benefits of capacitive isolators are efficiency and magnetic field immunity [1].

One advantage of capacitive isolation is speed. While optical isolators are typically rated below 50 Mbps, capacitive isolators have reported data speeds up to 640 Mbps [7]. However, this specific capacitive isolator gives no data on CMR. It claims 2.5 kV RMS isolation by implementing on-chip lateral high-voltage capacitors on a silicon-on-sapphire substrate. The capacitors use 5 μm separated interdigitated fingers on chip metal interconnect [7].

The Texas Instruments ISO72x family of isolators uses capacitors for isolation. The design uses two channels, a high signaling rate channel and a low signaling rate channel. The low signaling rate channel encodes the signal with a high frequency pulse-width modulated (PWM) carrier to transmit across the capacitor. Both channels provide differential signaling to achieve high common-mode rejection. The reported voltage isolation is 2.5 kV RMS, CMR is 25 kV/μs, and data rate is 150 Mbps [1].

Transformer-Based Isolation

Isolated transformers are also used for digital isolators. Two electrically isolated coils are able to pass information through inductive coupling. A primary winding is driven with a changing current to produce a varying magnetic field. A voltage proportional to the rate of change of the current is produced on the secondary coil. Circuitry detects the secondary winding voltage and converts the signal to a digital output. Transformers have limited bandwidth; therefore, signal

processing must be used to convert the input signal to the usable frequency range. A main advantage of transformer-based isolators is power consumption. A concern with these isolators is magnetic field interference [1].

Traditional transformers used for isolators have large occupied areas. Analog Devices has a chip-scale transformer for digital isolation, ADuM1100. The isolator places multiple chip dies in a single package. The dies are a typical CMOS die and a CMOS die with an elevated transformer on polyimide layers, shown in Figure 3. The design uses signal edges to transmit across the isolation barrier. This isolator has a data speed of 100 Mbps, isolation voltage of 2.5 kV RMS, and CMR of 25 kV/μs. This isolation technology also claims high DC magnetic field immunity from the lack of a magnetic core. The small area of the design allows high AC magnetic field immunity, and the immunity is mainly limited by the printed circuit board (PCB) design [8].

Isolators using transformers in standard CMOS technologies have also been researched with promising results. One such work implements a “small” transformer that has a diameter of 230 μm. This design achieves 2.5 kV isolation voltage, 35 kV/μs CMR, and 250 Mbps data rate. The isolation voltage is

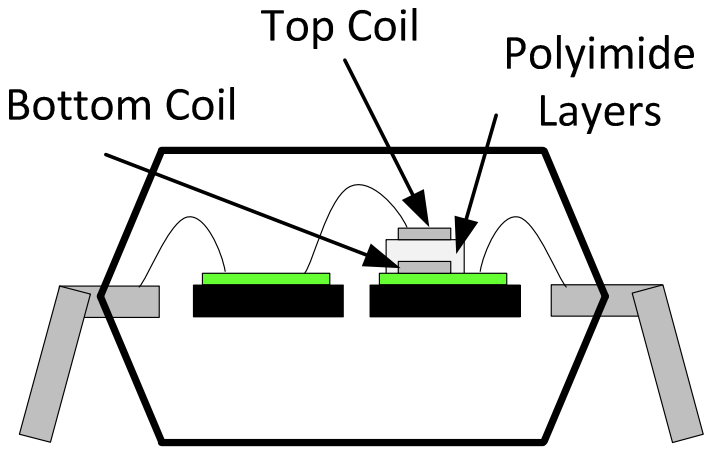

Figure 3. ADuM1100 cross-sectional view [8]

achieved by the silicon dioxide (SiO_2) dielectric between chip metal interconnect. This SiO_2 layer separates two stacked transformer coils. Low coupling capacitance from a small transformer size and a high-pass filter (HPF) in the receiver circuitry helps improve this design's CMR [6].

CHAPTER III
ISOLATOR DESIGN REVIEW

Isolator Topology

The design goals for this thesis are based on an isolator design to best meet the needs of the integrated power module for motor drive applications. For this application an on-chip transformer-based isolator was chosen. A transformer-based isolator may be integrated with CMOS chip technologies. This isolator type may achieve significant isolation voltage and CMR. The design was implemented in a SOI chip technology capable of handling the high temperature requirements of the integrated power module.

There have been many transformer-based isolator designs in CMOS technologies. The architectures include set/reset, amplitude modulation, pulse count, and pulse polarity. The most straightforward architecture is a set/reset design with a dual transformer. The dual transformer implementation takes up twice the amount of chip area compared to single transformer designs. The amplitude modulation scheme is a single transformer architecture but has high power dissipation. The pulse count architecture improves upon the previous designs when considering area and power consumption. The pulse count design has speed limitations from the finite time it takes to determine the pulse count. The pulse polarity architecture uses a single transformer and only uses signal edges to transmit data across the transformer. The improvements of a pulse polarity design lead to small area, low power, and high data rates. Inductor-coupled isolator architectures are compared in Table 1 [6]. This table normalizes the parameters for comparison. The circuit design for the chip-level isolator presented in this thesis is based on a pulse polarity scheme in [6].

Table 1. Comparison of inductor-coupled isolator architectures [6]

	Set/Reset	Amplitude Modulation	Pulse Count	Pulse Polarity
Area	2	1	1	1
Power	1	>>2	1.5	1
Delay	1	>1	>2	1

On-Chip Transformer Model

An on-chip transformer model is needed for chip technologies. The SOI chip fabrication process used for this design does not include any inductor or transformer models. Modeling and design of on-chip inductors and transformers is presented in [9]. Each inductor is constructed with one metal spiral or coil. On-chip transformers, consisting of multiple coils, may be designed in different ways. The transformer configurations include tapped, interleaved, and stacked transformers. The stacked transformer design is chosen for multiple reasons. This configuration has the highest self-inductance and best coupling coefficient. It also has the best area efficiency. A main disadvantage of the stacked transformer is a lower resonant frequency resulting from higher spiral-to-spiral capacitance [9]. Also, a stacked transformer limits the insulating dielectric thickness between coils that results in lower voltage strength of the isolator.

The lateral parameters of a spiral are shown in Figure 4 [9]. The main parameters are the number of turns (n), the metal width (w), the spacing between adjacent turns (s), the number of sides of the coil (N), the inner and outer diameters (d_{in} and d_{out}), and the average diameter (d_{avg}). The fill ratio (ρ) is given by either of the following expressions [9]

$$\rho = \frac{d_{out}-d_{in}}{d_{out}+d_{in}} = \frac{n(w+s)-s}{d_{avg}} \qquad (3.1)$$

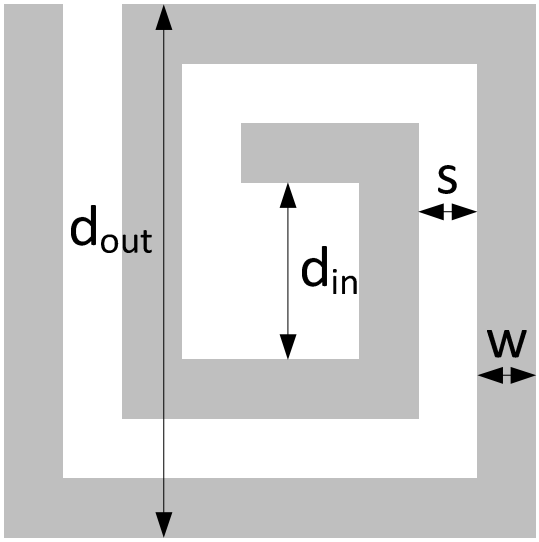

Figure 4. Parameters of a lateral coil with n=2 and N=4

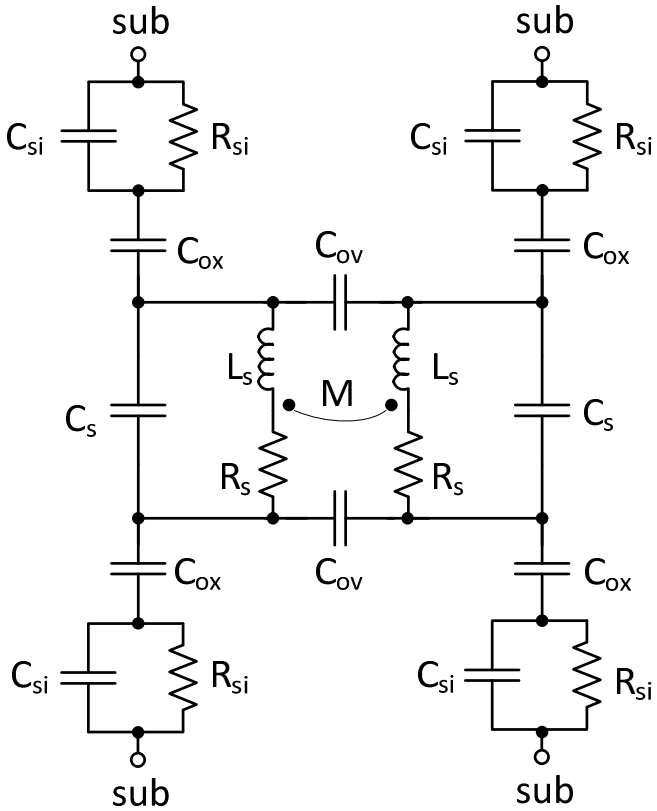

Figure 5. Nonideal transformer circuit model [9]

The model for a nonideal transformer is shown in Figure 5. This model includes two spiral π models, one for each coil. The spiral π model includes the series inductance (L_s), the series resistance (R_s), the feed-forward capacitance (C_s), the inductor to substrate capacitance (C_{ox}), and the substrate resistance (R_{si}) and capacitance (C_{si}). The transformer model also includes the spiral-to-spiral capacitances (C_{ov}) and the mutual inductance (M). The substrate coupling elements R_{si} and C_{si} are neglected from the use of a patterned ground shield [9].

The inductance (L_s) calculation of each coil is determined by approximate expressions derived in [9]. The expressions include electromagnetic principles using current sheet approximations obtained for discrete inductors. Compared to field solvers, these expressions typically present 2-3 % error [9]. The equation for the series inductance is [9]

$$L_s = \frac{2\mu n^2 d_{avg}}{\pi}\left[ln\left(\frac{2.067}{\rho}\right) + 0.178\cdot\rho + 0.125\rho^2\right] \qquad (3.2)$$

where μ is the magnetic permeability of free space ($\mu = 4\pi\cdot 10^{-7}$ H/m), n is the number of turns of the coil, d_{avg} is the average diameter of the turns, and ρ is the fill ratio [9].

The series resistance is calculated by the following equation [9]

$$R_s = \frac{l}{\sigma\delta w\left(1-e^{\frac{-t}{\delta}}\right)} \qquad (3.3)$$

where l and w are the length and width of the spiral, σ is the metal conductivity, t is the metal thickness, and δ is the skin length given by [9]

$$\delta = \sqrt{\frac{2}{(2\pi f)\mu\sigma}} \qquad (3.4)$$

where f is the frequency. The series resistance expression models the increase of resistance at higher frequencies due to the skin effect [9].

For a stacked transformer, the dominant capacitances are the coil to coil capacitances and the bottom coil to substrate capacitance, modeled by parallel plate capacitances C_{ov} and C_{ox}. These capacitances are given by [9]

$$C = \frac{1}{2} \frac{\varepsilon_{ox}}{t_{ox}} lw \tag{3.5}$$

where ε_{ox} is the oxide permittivity ($3.45 \cdot 10^{-13}$ F/cm), and t_{ox} is the oxide thickness [9].

The mutual inductance is calculated from the coupling coefficient (k) and the primary and secondary coil inductances [9]

$$M = k\sqrt{L_1 L_2} \tag{3.6}$$

The coupling coefficient varies depending on the type of transformer. A stacked transformer has the highest coupling coefficient about 0.9 with no lateral spacing between the coils [9].

Transmitter Design

The isolator system is composed of one transmitter die and one receiver die. The schematic design is similar to [6]. The block diagram of the transmitter is shown in Figure 6. The transmitter includes the isolated transformer coils. The transmitter and receiver dies are connected through the node V_2. The input signal to the transmitter is a pulse-width modulated (PWM) 5 V logic signal. The transmitter circuitry converts this logic signal to a current through the primary coil that is inductively coupled to the second coil by creating a voltage pulse at V_2.

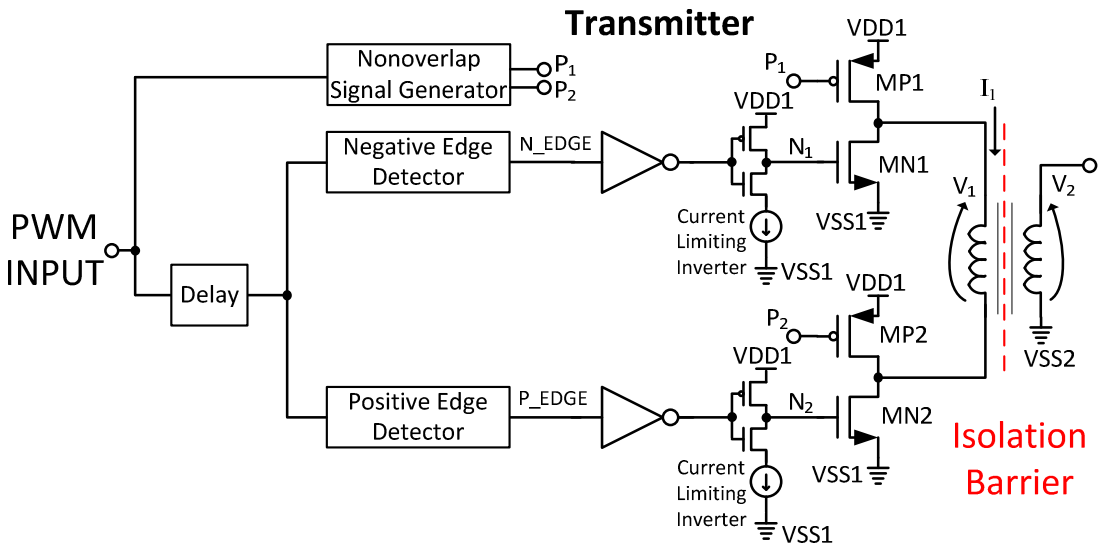

Figure 6. Transmitter schematic

The nonoverlap signal generator is developed from [10] and shown in Figure 7. A nonoverlap signal generator converts the logic signal to complementary outputs at P_1 and P_2. The complementary signals control MP1 and MP2 in the transmitter circuit allowing only one PMOS to turn on at a time. The circuit uses delay between the NAND gate and inverters to induce a delay between the negative transitions at nodes A and B. The A and B nodes are then given to an inverter string buffer to drive the large PMOS switches MP1 and MP2. Simulation waveforms are shown in Figure 8.

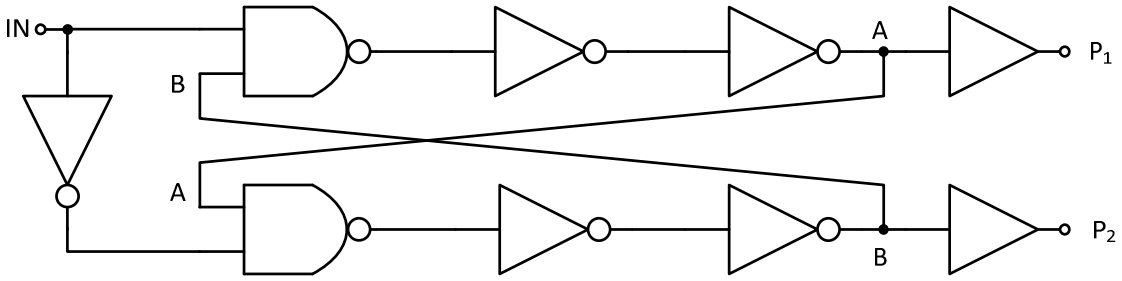

Figure 7. Nonoverlap signal circuit

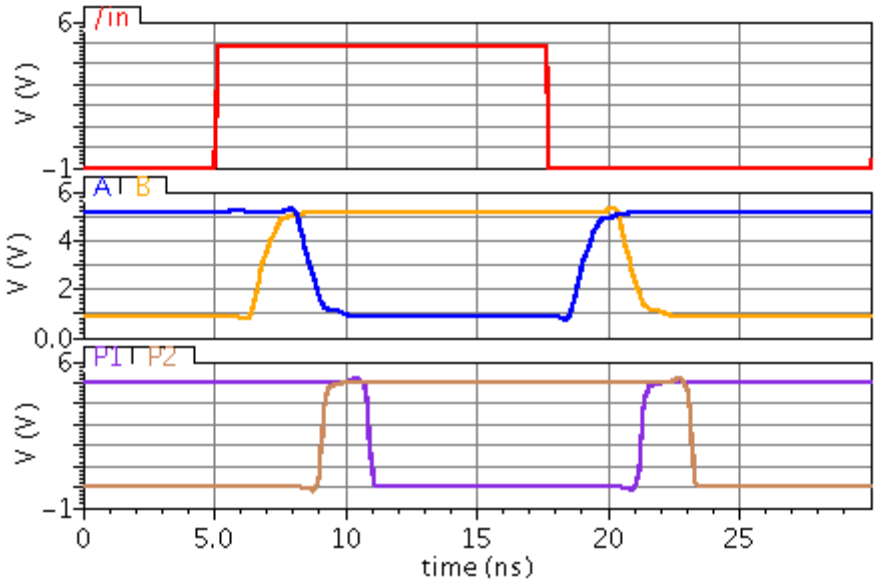

Figure 8. Nonoverlap circuit simulation

The NMOS drive transistors MN1 and MN2 in Figure 6 set the desired current signal through the transformer. MN1 and MN2 are controlled by a delay, edge detectors, inverted buffers, and current limiting inverters. The delay is a simple string of inverters that introduces about 6 ns of delay. The purpose of this delay is to allow the correct PMOS drive transistor to turn 'on' fully before the correct NMOS drive transistor turns 'on.' No more than one PMOS and one NMOS drive transistors are 'on' at the same time.

The edge detectors, based on the block diagram in [6], are shown in Figure 9. A negative edge detector is the circuit used in the control circuitry for MN1. A positive edge detector is the circuit used in the control circuitry for MN2. Both edge detectors use two inverters to buffer the input signal to the B_IN nodes. A string of inverters is used to generate an inverted input signal at the INV_DEL nodes that has been delayed by 9 ns. The outputs N_EDGE and P_EDGE switch to high for 9 ns on a negative and positive input edge, respectively. The simulation results are shown in Figure 10.

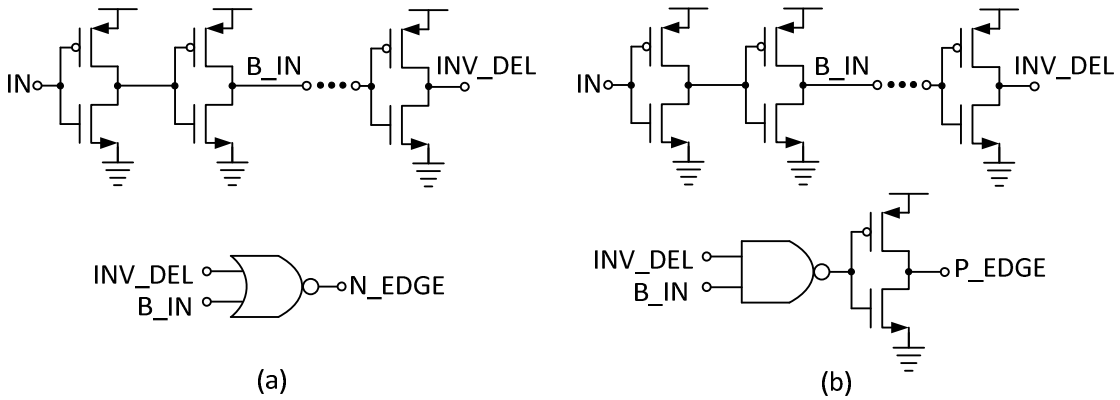

Figure 9. (a) Negative edge detector and (b) positive edge detector

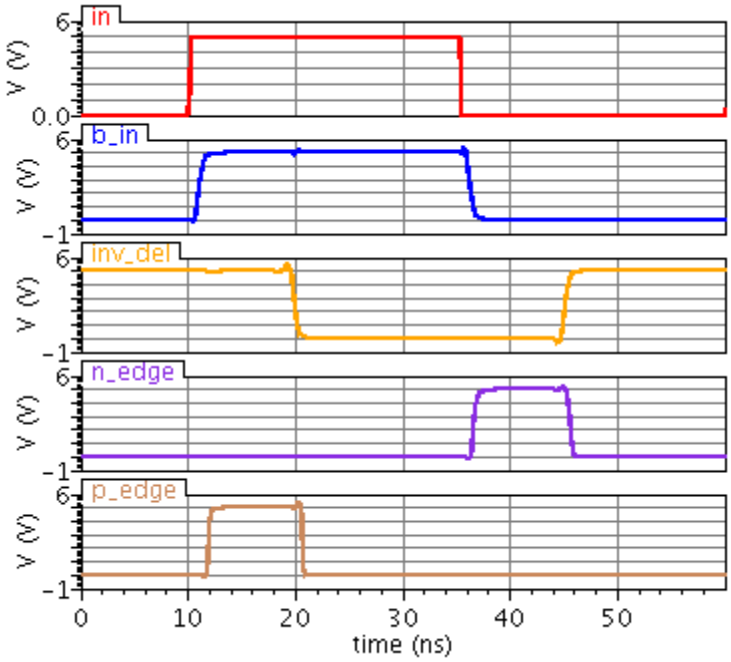

Figure 10. Edge detector simulation

The edge detectors' outputs are given to the inverted buffers to drive the current limiting inverters. The current limiting inverters allow a fast rise time and slow fall time for the voltage on N_1 and N_2 in Figure 6. The current limiting inverter in Figure 11 shows a basic CMOS inverter with an extra NMOS

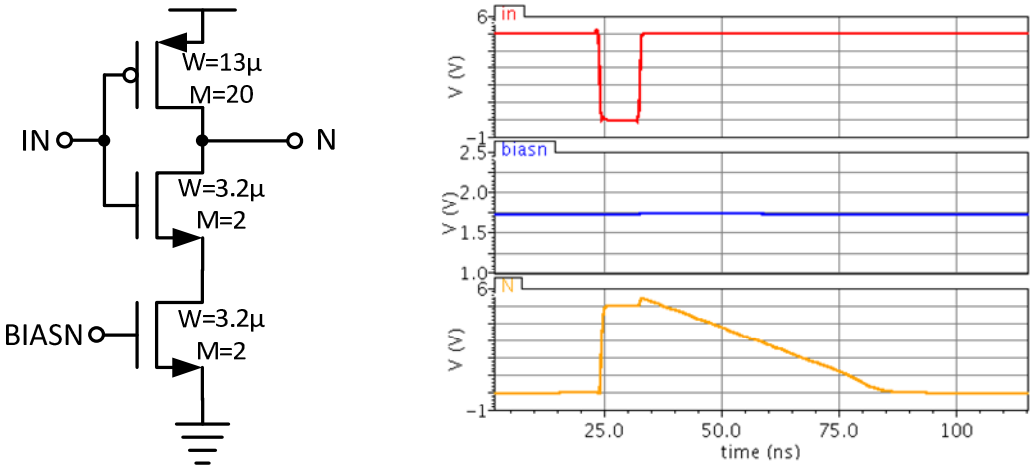

Figure 11. Current limiting inverter schematic and simulation

transistor. The PMOS transistor is large for sufficient current drive of the high capacitive load of MN1 and MN2. The desired rise time of node N in Figure 11 is on the order of 1 ns. The extra NMOS transistor is given a low bias voltage; this limits the current to increase the pull-down time on N. The BIASN voltage is generated with a Beta-multiplier current mirror from [10]. The simulation of the current limiting inverter is also shown in Figure 11. The simulations show a rise time around 1 ns and fall time around 50 ns at node N.

The simulation results of the drive stage are shown in Figure 12. The voltages for the PMOS gates (VP1 and VP2) are from the nonoverlap signal generator. The voltages for the NMOS gates (VN1 and VN2) are from the current limiting inverters. The input logic signal is the top signal shown in the simulation. After the logic signal changes to HIGH, VP1 switches LOW turning MP1 ‘on.’ After a short delay, VN2 sharply rises, holds HIGH for a small time, and then slowly falls. The corresponding current in the primary coil (I1) has a similar shape to VN2. The current sharply rises to around 80 mA and then slowly falls to zero mA after a short delay. The voltage pulse (V2) is the bottom signal on the waveform. This pulse is proportional to the voltage across the inductance of the primary coil given by

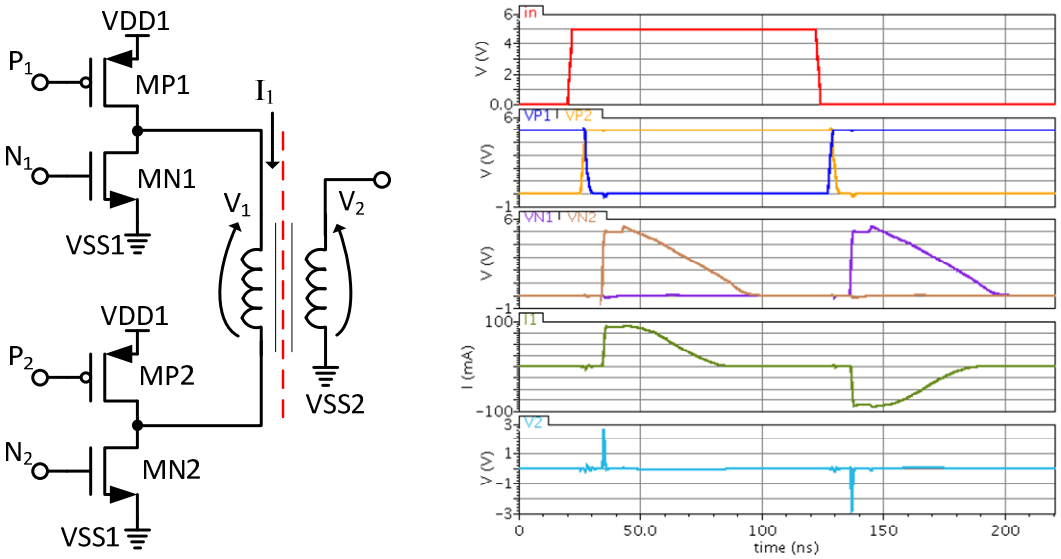

Figure 12. Drive stage schematic and simulation

$$V = L\frac{dI}{dt} \qquad (3.7)$$

where L is the inductance, and *dI/dt* is the derivative of the current in the coil. The pulse polarity description of this topology is demonstrated by the voltage pulse polarity generated after the switching of the input signal. The fast positive current is produced after the input PWM signal switches HIGH, and a fast negative current is produced when the input PWM signal switches LOW. A high voltage pulse about 2.5 V occurs during the fast rise time of the current. A much smaller voltage of about 60 mV results from the slow fall time of the current. This smaller voltage is called the counter-pulse in [6]. The receiver circuit must detect the high voltage pulse and reject the counter-pulse.

An on-chip transformer is designed to interface between the transmitter and receiver circuitry. The transformer layout and schematic model used in the chip design are shown in Figure 13. The transformer has a n of 10, w of 6 μm, s of 2 μm, N of 4, d_{out} of 224 μm, and d_{in} of 60 μm. The d_{avg} is 142 μm, and ρ is

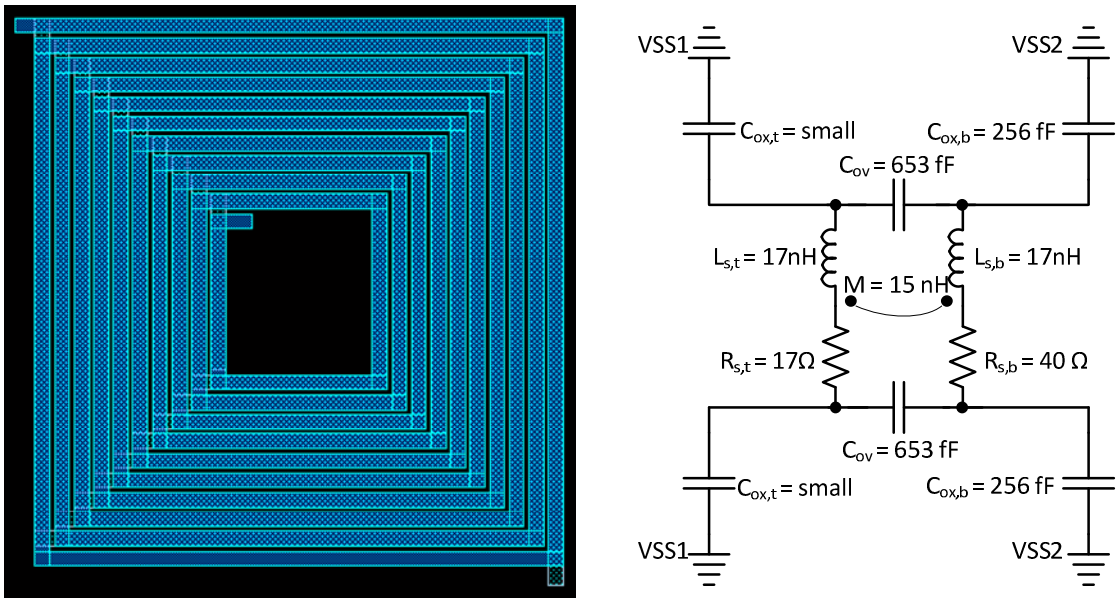

Figure 13. Transformer chip layout and circuit model

0.55. The primary coil is constructed on chip metal 3, or top metal, and the secondary coil is constructed on chip metal 2. The circuit model uses 't' to label the top, or primary, coil and 'b' to label the bottom, or secondary, coil. Top metal is the thickest metal interconnect on the chip. Top metal has a sheet resistance of 14.6 mΩ/square; metal two has a sheet resistance of 38 mΩ/square. The primary coil constructed from top metal is best suited to carry the relatively large current around 80 mA. The series inductances (L_s), the series resistances (R_s), and the capacitances from coil to coil and coil to substrate (C_{ov} and C_{ox}) are calculated from the equations presented with the transformer model. The circuit model shows a small $C_{ox,t}$ for the capacitance from the top coil down to the substrate. Since the top and bottom coil are overlapped, the capacitance from the top coil to the substrate is much smaller than the capacitance from the bottom coil to the substrate, $C_{ox,b}$. The mutual inductance is estimated with a coupling coefficient of 0.9. The nodes VSS1 and VSS2 represent the isolated grounds of the transmitter and receiver circuits. The only paths for signal transfer between the primary and secondary coils are the mutual inductance and the parasitic capacitances. The desired voltage pulse of the transmitter circuitry is

inductively coupled to the receiver circuitry. The common-mode noise is coupled through the coil to coil capacitances.

A main advantage of the pulse polarity architecture is reduced transformer area. Utilizing the higher frequency components of the input signal, the transformer diameter is small [6]. The area taken up by the transformer is roughly 0.05 mm^2. From this small area, the transformer takes up only a small portion of the chip.

Receiver Design

The receiver circuit is designed to detect the voltage pulse on the secondary coil and convert the pulse into an output logic signal that matches the input PWM signal to the transmitter. The schematic for the receiver circuit is shown in Figure 14. The input signal for the receiver is the voltage pulse V_2 from the transformer secondary coil. The main elements of the receiver are a diode-based pulse detector [6], an amplifier, and a comparator.

The pulse detector is the circuitry from node V_2 to the differential amplifier (DA in Figure 14). A high-pass filter is implemented at the input of the receiver with a capacitance set by C_1 and C_2 and resistance set by R_1, R_2, and the impedance looking into the voltage reference output. This filter is a circuit to help block transient noise coupled from the transmitter. The voltage pulse produced from the transmitter circuitry is higher frequency than the common-mode noise. Therefore, the high pass filter is designed to allow the designed voltage pulse to pass and block the common-mode noise [6].

Two lateral npn BJTs are diode connected to introduce the diode thresholds. The diodes D_1 and D_2 detect the positive voltage pulse and negative voltage pulse, respectively. The capacitors C_3 and C_4 are charged through the diodes during the correct pulse polarity. The voltage on the capacitor decays slowly from the sufficiently large time constant introduced at the nodes V_{PEAK} and

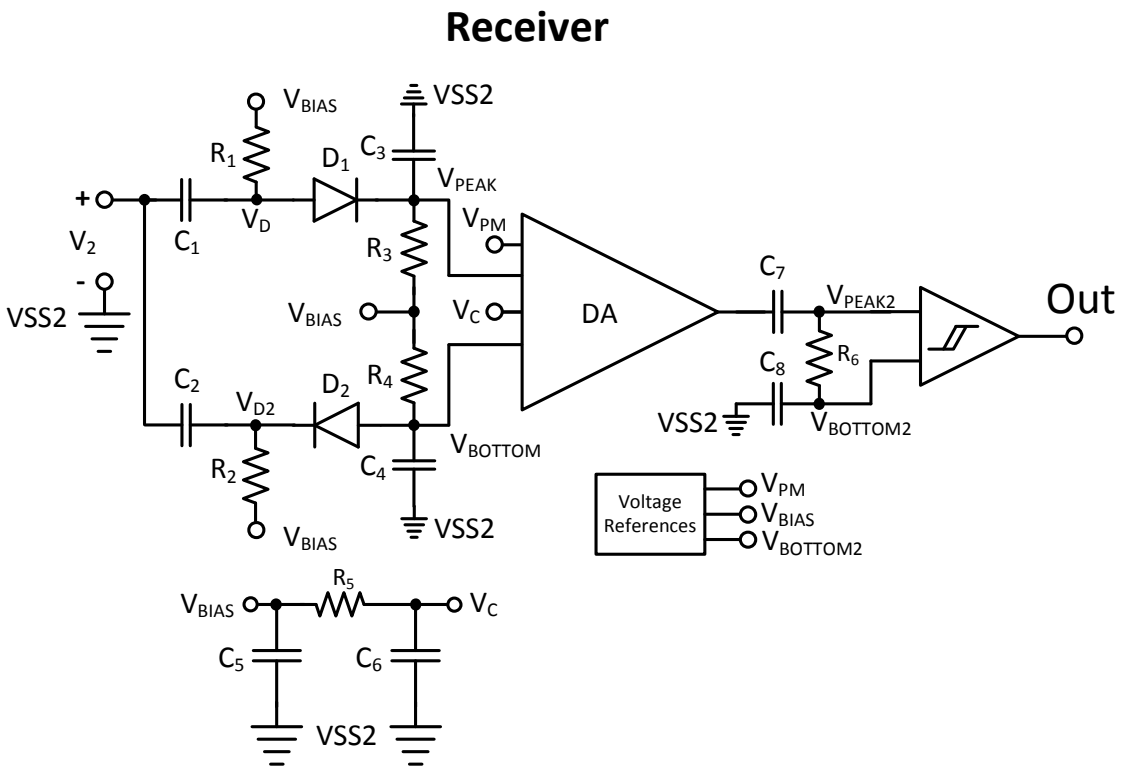

Figure 14. Receiver schematic

V_{BOTTOM}. The simulation results in Figure 15 show the voltages V_2, V_D, and V_{PEAK} during normal operation. The simulation represents one period of the input PWM signal. A positive voltage pulse at V_2 is around 2.5 V. A large portion of that voltage pulse shows up at V_D. The voltage at V_D is high enough to pass the voltage threshold of D_1. The voltage at node V_{PEAK} shows the signal that crosses the threshold level of D_1. Node V_{PEAK} holds about 200-300 mV for 50 ns. This signal is slow enough for the differential amplifier to process. The negative pulse at V_2 does not show up at V_{PEAK}.

A bandgap reference (BGR) voltage, based on a design in [10], sets the DC operating point of the pulse detection circuitry and the input to the differential amplifier. Node V_{BIAS} in Figure 14 is the BGR output voltage. This voltage is relatively constant across a wide temperature range. A BGR combines the

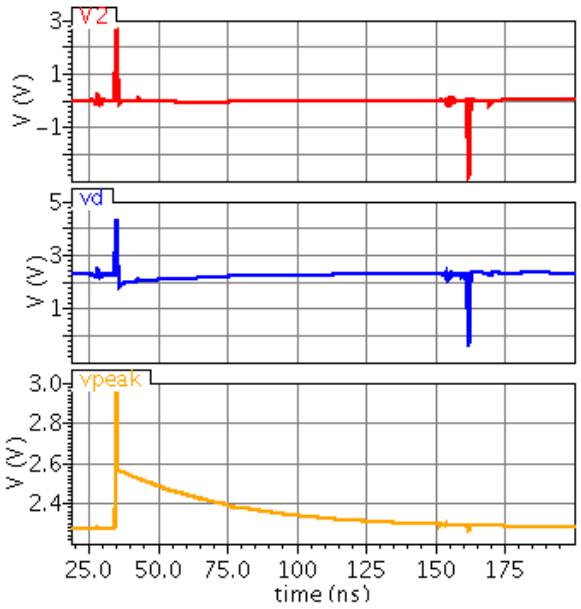

Figure 15. Diode threshold simulation

elements of a circuit that are proportional to absolute temperature (PTAT) and complementary to absolute temperature (CTAT). The schematic of the BGR circuit is shown in Figure 16.

The schematic is split in two main parts. The first part is the PTAT current generator. In this circuit the cascode structure forces the same current through each side of the circuit. The size of D_2 must be larger than the size of D_1 in this circuit for nonzero current to flow. Figure 16 shows D_2 to be a factor of K times larger than D_1. The voltage drop across D_2 will be smaller than the voltage drop across D_1 with an equivalent current flowing through both. The diode currents (I_{D1} and I_{D2}) and diode voltages (V_{D1} and V_{D2}) are related as given in the following equations [10]

$$I_{D1} = I_S e^{\frac{V_{D1}}{nV_T}} \tag{3.8}$$

$$I_{D2} = K \cdot I_S e^{\frac{V_{D2}}{nV_T}} \tag{3.9}$$

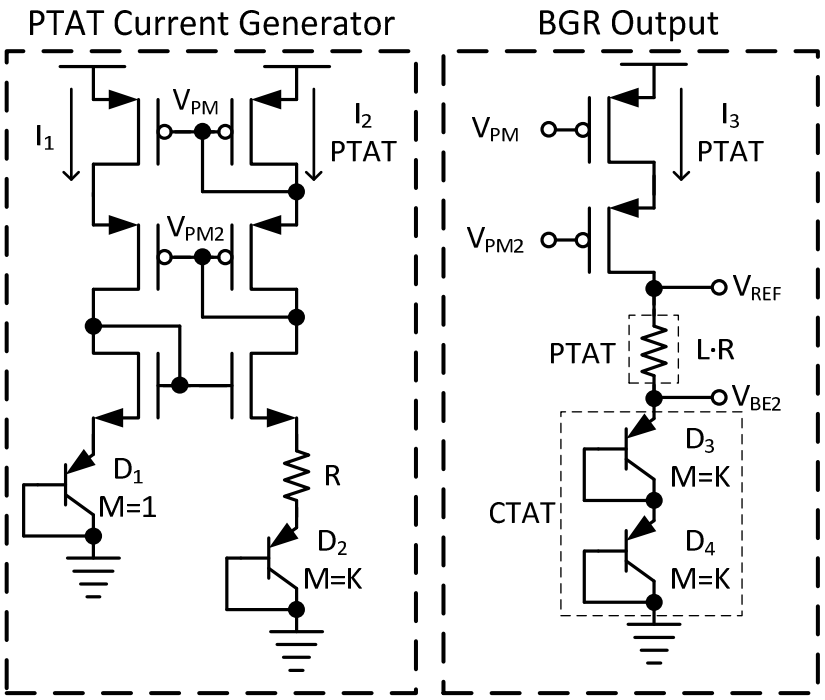

Figure 16. Bandgap reference schematic

$$V_{D1} = nV_T ln\left(\frac{I_{D1}}{I_S}\right) \tag{3.10}$$

$$V_{D2} = nV_T ln\left(\frac{I_{D2}}{K \cdot I_S}\right) \tag{3.11}$$

where I_S is the scale (or saturation) current, n is the emission coefficient, and V_T is the thermal voltage. In this schematic the voltage across D_1 is equal to the sum of the voltage across D_2 and the resistor R [10]

$$V_{D1} = V_{D2} + I_{D2}R \tag{3.12}$$

Since the currents I_{D1} and I_{D2} ($I_{D1} = I_{D2} = I$) are equivalent, this equation may be solved for R or I [10]

$$R = \frac{nV_T ln(K)}{I} \text{ or } I = \frac{nV_T \cdot ln(K)}{R} \tag{3.13}$$

Ignoring the temperature coefficient of the resistor, the current's temperature dependence, set by V_T, is PTAT.

The next part of the schematic generates the BGR output voltage (V_{REF}). This part of the circuit is connected to the PTAT current generator through the PMOS gate voltages V_{PM} and V_{PM2} in Figure 16. This produces a current through the BGR output circuit that is PTAT. This PTAT current flows through a resistor and two diodes in series. The voltage drop, V_{BE2} in Figure 16, across diodes D_3 and D_4 is CTAT. However, the voltage at node V_{REF} shows small variance with temperature. The voltage V_{REF} is given by

$$V_{REF} = V_{D3}+V_{D4}+I_3 \cdot L \cdot R$$

$$V_{REF} = V_{D3}+V_{D4}+nV_T \cdot L \cdot ln(K) \qquad (3.14)$$

where L is a multiplication factor, and R is the resistor in the PTAT current generator. Using the multiplication factor allows the temperature behavior of the resistor to fall out of the equation. The derivative with respect to temperature of Eq. (3.14) is

$$\frac{dV_{REF}}{dT} = \frac{dV_{D3}}{dT} + \frac{dV_{D4}}{dT} + n \cdot L \cdot ln(K) \cdot \frac{dV_T}{dT} \qquad (3.15)$$

This equation shows the change in the reference voltage with temperature. The changes with temperature are about –1.6 mV/℃ for the diode voltages and 0.085 mV/℃ for the thermal voltage. To produce a reference voltage with (theoretically) no temperature change, Eq. (3.15) is set to zero and solved for L

$$L = \frac{-\left(\frac{dV_{D3}}{dT}\right)-\left(\frac{dV_{D4}}{dT}\right)}{n \cdot ln(K) \cdot \frac{dV_T}{dT}} \qquad (3.16)$$

The simulation in Figure 17 shows a temperature sweep while plotting V_{REF}, V_{BE2}, and I_3. V_{REF} varies only about 10 mV, V_{BE2} is CTAT, and I_3 is PTAT.

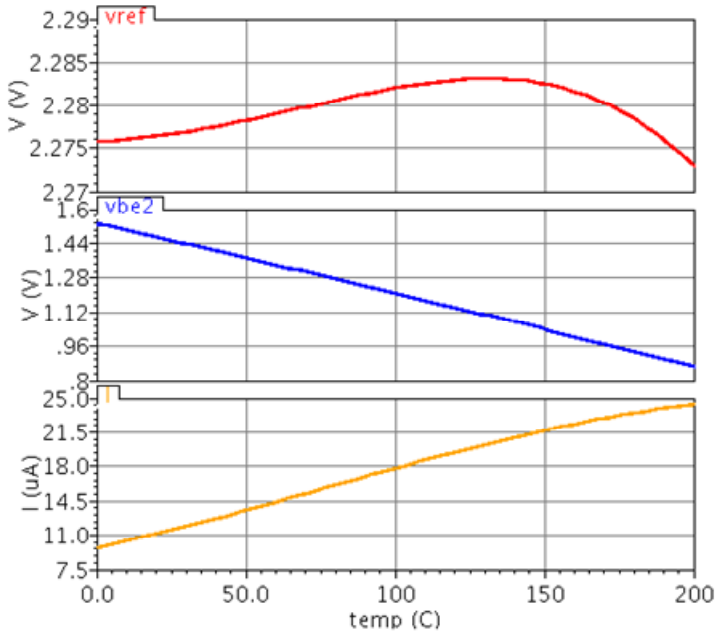

Figure 17. Bandgap reference simulation

The differential amplifier (DA) amplifies the voltages that pass either of the diode thresholds. The DA schematic, based on a differential difference amplifier from [11], is shown in Figure 18. The current in the DA is established from a current mirror by V_{PM}. This voltage for the gate of M13 is connected to the V_{PM} node of the BGR. The differential amplifier's input common-mode voltage is also set by the BGR. The BGR output of about 2.275 V is the voltage V_{BIAS} in the receiver circuit. This sets the DC voltage of V_{NN}, V_C, and V_{PP} in the DA. For the DA to be functioning correctly, all transistors must be operating in the saturation region. Therefore, the bias point of the input NMOS transistors set by V_{BIAS} must be within a specific range for the transistors to be in saturation. The maximum and minimum common-mode voltage (V_{CMMAX} and V_{CMMIN}) are given by [10]

$$V_{CMMAX} = V_{DD} - V_{SG} + V_{THN} \tag{3.17}$$

$$V_{CMMIN} = V_{DS,SAT} + 2V_{GS} \tag{3.18}$$

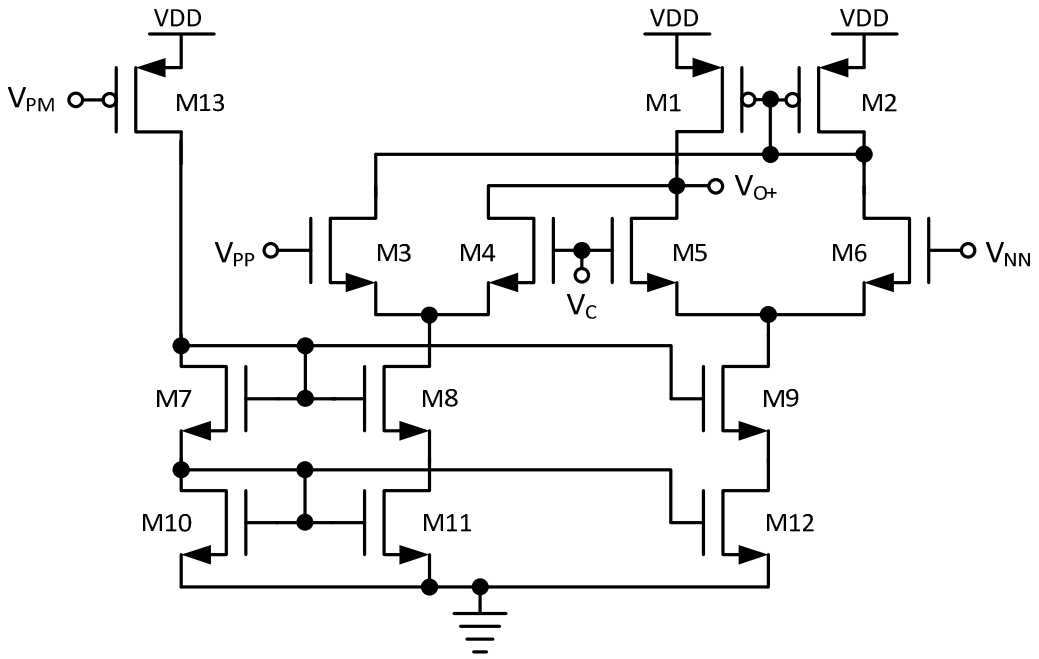

Figure 18. Differential amplifier schematic

where V_{SG} is the source-to-gate voltage of the PMOS transistors M1 and M2, V_{THN} is the NMOS threshold voltage, $V_{DS,SAT}$ is the drain-to-source saturation voltage of the NMOS transistors M8, M9, M11, and M12, and V_{GS} is the gate-to-source voltage of the NMOS transistors. The voltage $V_{DS,SAT}$ is the minimum drain-to-source voltage that meets the definition of the saturation region ($V_{DS} \geq V_{GS} - V_{TH}$). $V_{DS,SAT}$ is approximately 250 mV for strong-inversion operation. The saturation voltage is equivalent to the excess gate voltage or amount of gate voltage exceeding the threshold voltage.

The differential amplifier is a single stage gain circuit with two positive inputs (V_{PP} and V_{NN}) and one negative input (V_C). The circuit simultaneously compares V_{PP} to V_C and V_{NN} to V_C. The small signal differential mode gain of the amplifier (A_d) at the output V_{O+} is given by [10]

$$A_d = g_m \cdot (r_{on} || r_{op}) \qquad (3.19)$$

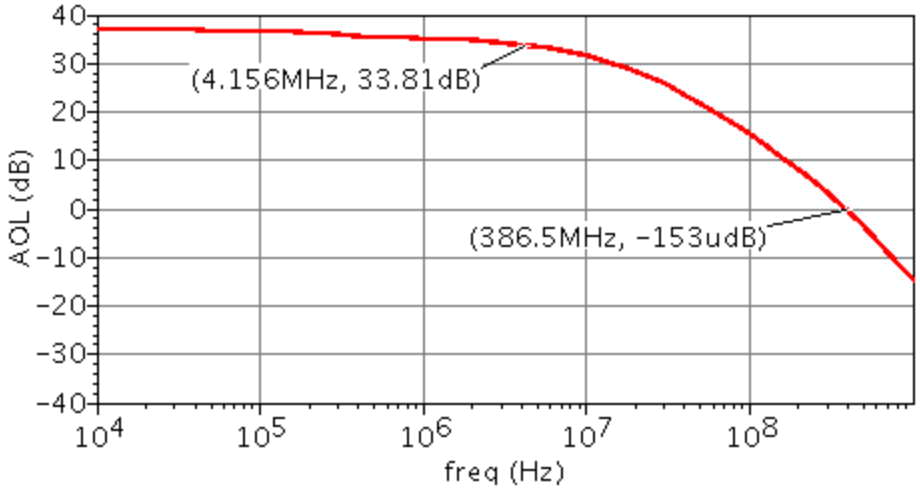

Figure 19. Differential amplifier A_{OL} simulation

where g_m is the transconductance of the input NMOS transistors, r_{on} is the output resistance of the input CMOS transistors connected to V_C, and r_{op} is the output resistance of the PMOS transistor M1. The AC simulation response of the open loop gain (A_{OL}) is shown in Figure 19. The low frequency gain around 36 dB is sufficient to convert the inputs to a detectable signal by the comparator. The 3 dB frequency is about 4.2 MHz and the unity frequency is about 387 MHz. This plot further explains the need for the capacitors C_3 and C_4 and the resistors R_3 and R_4 in the receiver circuit. The time constant introduced by these elements produces a lower frequency signal that can be sufficiently amplified by the DA.

The output of the differential amplifier is capacitively coupled to the positive input of the comparator. This output of the DA is capacitively coupled because simulations show a large DC voltage variance of node V_{O+} when applying device mismatch variations. Therefore, only the AC component of V_{O+} reaches the comparator. The inputs to the comparator are V_{PEAK2} and $V_{BOTTOM2}$. The DC level of these signals is produced from $V_{BOTTOM2}$; $V_{BOTTOM2}$ is a BGR voltage similar to V_{BIAS} in the receiver circuit. The connection between the DA and comparator is shown in Figure 20.

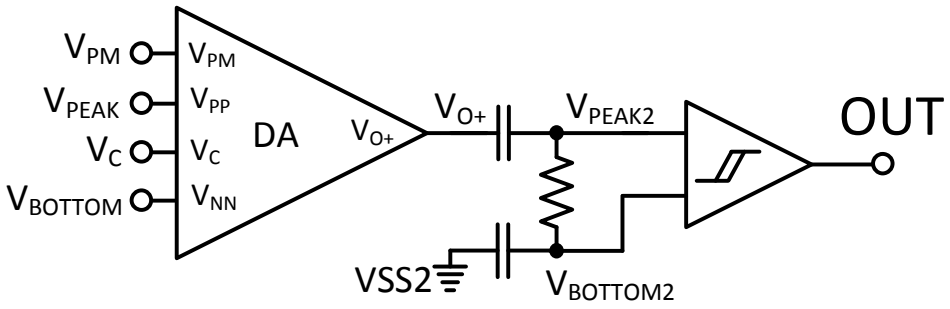

Figure 20. Differential amplifier and comparator connection

The simulation of the DA signals and the comparator input signals are shown in Figure 21 for one period of the PWM input signal. The positive voltage pulse from the transformer is detected at V_{PEAK}, and the negative pulse is detected at V_{BOTTOM}. The amplified signal V_{O+} is capacitively coupled to V_{PEAK2}. The amplitude of V_{PEAK2} is about 1.5 V in the positive direction and –2 V in the negative direction.

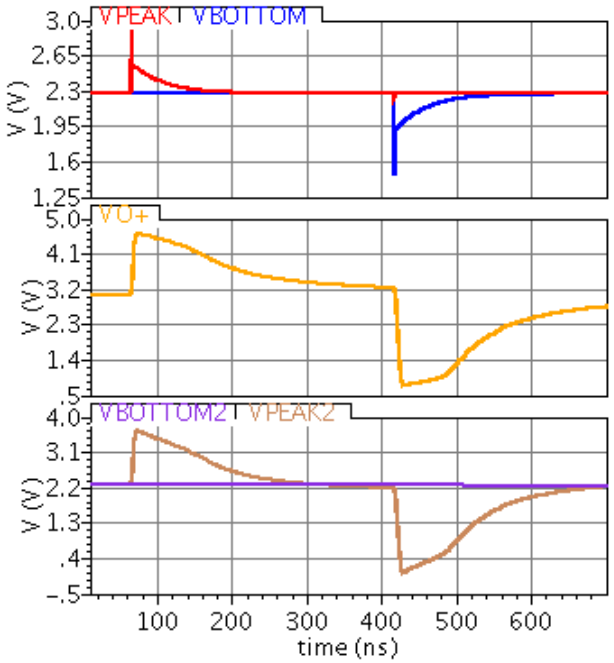

Figure 21. Differential amplifier and comparator input simulation

The comparator design is similar to an architecture provided in [10]. The comparator's positive and negative inputs are connected to V_{PEAK2} and $V_{BOTTOM2}$, respectively. The comparator is a nonlinear analog circuit. This description is because the output signal of the circuit is not linearly related to the input of the circuit [10]. The comparator shown in Figure 22 has a differential input pair, a decision stage, and an output buffer.

The differential stage inputs of the comparator are the positive input V_P and the negative input V_M. The decision stage utilizes positive feedback from the cross-gate connection of M4 and M5. If the PMOS transistors M3, M4, M5, and M6 of the decision stage are the same size, the switching point of the comparator is when V_P and V_M are equivalent. Hysteresis is present in the comparator when $B_{p4,5}$ are larger than $B_{p3,6}$ [10]. The parameter B_p is defined as [10]

$$B_p = \mu_p C_{ox}' \frac{W}{L} \tag{3.20}$$

where μ_p is the hole mobility, C_{ox}' is the oxide capacitance, W is the device gate width, and L is the device gate length. An equation for the positive and negative

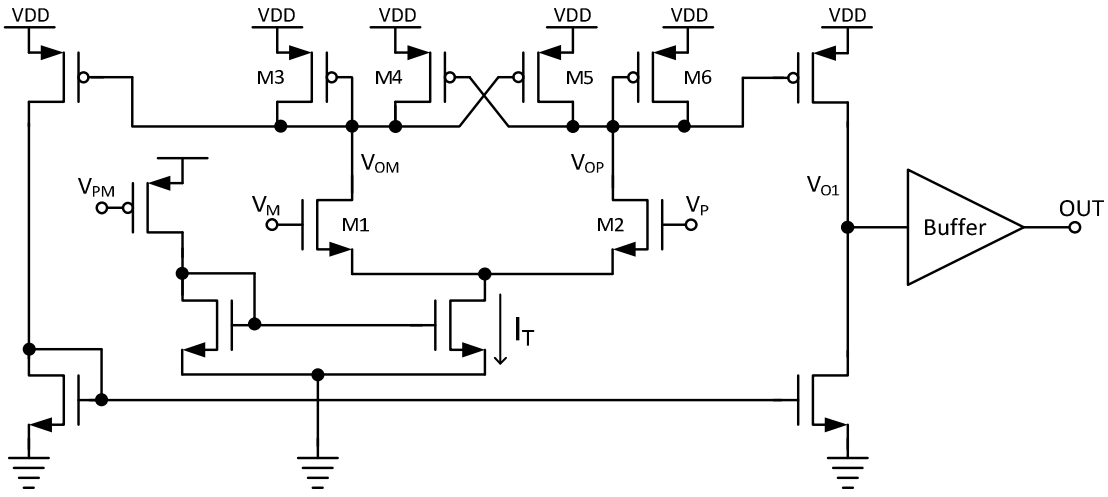

Figure 22. Comparator schematic

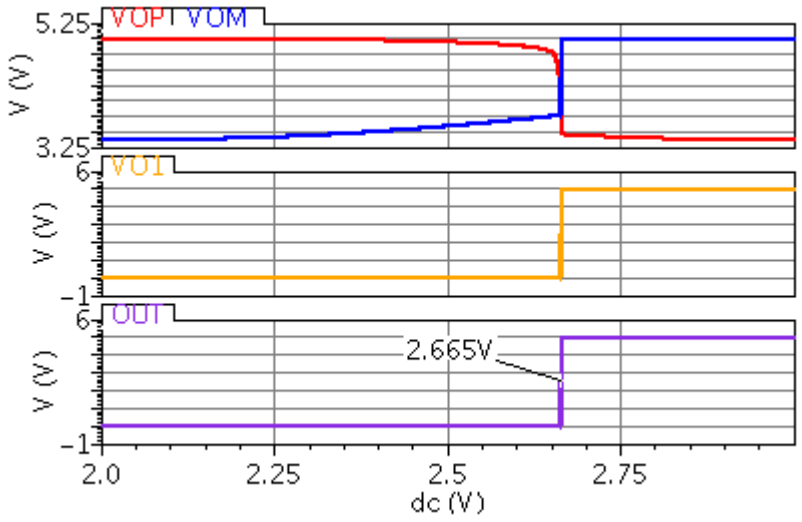

Figure 23. Comparator DC simulation of V_P sweep

switching points V_{SPH} and V_{SPL} is given by [10]

$$V_{SPH} = -V_{SPL} = \frac{I_T}{g_m} \cdot \frac{\frac{B_B}{B_A}-1}{\frac{B_B}{B_A}+1} \qquad (3.21)$$

where I_T is the tail current, B_B is B_p of M4 and M5, and B_A is B_p of M3 and M6. The switching point simulation is shown in Figure 23. This DC simulation sweeps V_P from 2 to 3 V and keeps V_M at 2.5 V. The plotted signals are the decision stage voltages V_{OP} and V_{OM}, the first logic output V_{O1}, and the final buffered output OUT. The simulation displays a switching point of 165 mV. The output of the comparator is the final output signal of the digital isolator system.

Chip Layout and Simulations

The isolator design is implemented in a three metal SOI chip technology. A cross section of the chip layout detailing layer thicknesses and placements is shown in Figure 24. The p-type handling wafer is isolated from devices in the n-well and p-well through a 500 nm thick buried oxide. Each n-well and p-well is isolated horizontally by 0.8 µm thick trench isolation. The metal thicknesses are

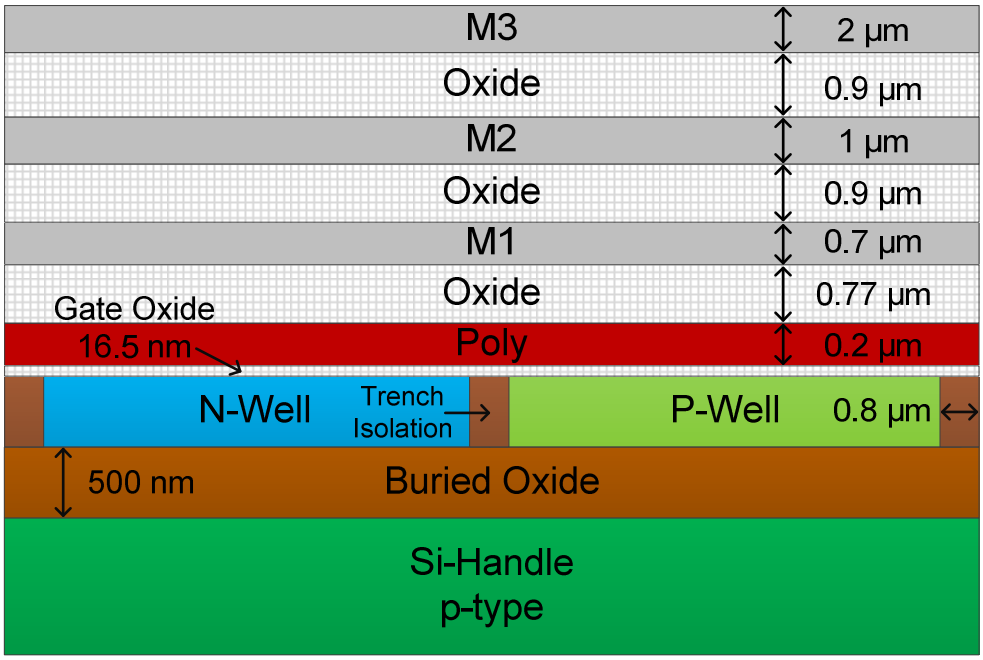

Figure 24. Chip layers cross-sectional view

0.7 µm of metal 1 (M1), 1 µm of metal 2 (M2), and 2 µm of metal 3 (M3). This allows metal 3 to have a smaller sheet resistance than metal 1 or metal 2.

Chip layout introduces parasitics that affect the operation of the circuit design. These parasitics are from metal interconnect, metal and substrate contacts, adjacent circuits, etc. One main place where parasitics affect the performance of the circuit is at the transformer drive stage that uses high dI/dt to create a detectable voltage pulse at V_2. Parasitics lead to a significant drop in the magnitude of the voltage pulse. The transmitter circuitry including the inverted buffers, current limiting inverters, and drive stage are impacted by increased parasitics. The capacitive loads at these stages become larger and require higher current drive to maintain the rise time and fall times of the signals.

Figure 25 shows waveforms for the drive stage simulations. The signals plotted are the voltage at N_2, the primary coil current I_1, and the voltage pulse V_2. The left plot of a simulation without parasitics shows a rise time of N_2 about 1.1

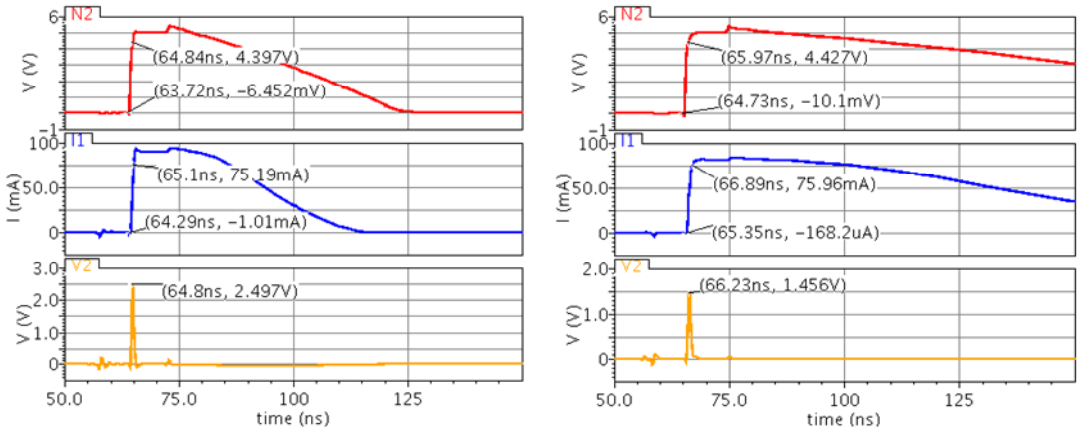

Figure 25. Drive stage simulations (a) parasitics not included and (b) parasitics included

ns, the rise time of the current about 0.8 ns, and the voltage pulse magnitude almost 2.5 V. The right plot of a simulation with parasitics shows a rise time of N_2 about 1.3 ns, the rise time of the current about 1.5 ns, and the voltage pulse magnitude almost 1.5 V. The reduced pulse magnitude from 2.5 V to 1.5 V is much harder for the receiver circuitry to detect.

Layout techniques are used to improve device matching of the analog circuits on the chip. MOSFET process parameters that affect device matching include gate-oxide thickness, lateral diffusion, oxide encroachment, and oxide charge density [10]. The analog circuits include the voltage references, the differential amplifier, and the comparator. These circuits use long gate length MOSFETs, common-centroid layout, and dummy MOSFETs to improve matching. Also, parasitic capacitances and resistances are minimized using multiple gate fingers and multiple substrate contacts.

A common-centroid layout example of NMOS transistors in a current mirror is shown in Figure 26. The layout contains 14 NMOS transistors. Eight of

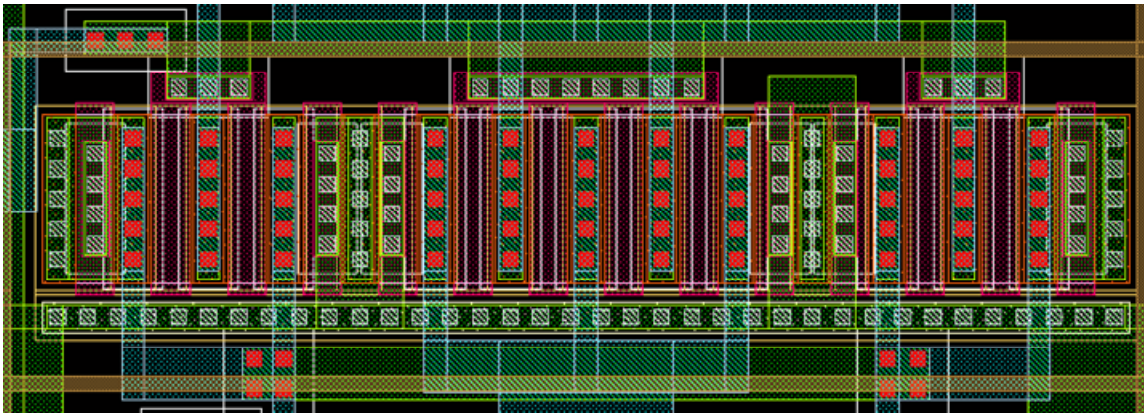

Figure 26. Common-centroid layout

the transistors are actually two devices with four gate fingers apiece. The first NMOS has two gates on the left and two gates on the right. The second NMOS has four gates in between the left and right gates of the first NMOS. The common-centroid layout evenly distributes process gradients in the x and y directions [10]. Six of these transistors in the layout are dummy transistors. The dummy transistors are connected together to ensure the device is ‘off’ and do not affect the normal circuit operation. The dummy devices minimize polysilicon patterning effects. The outermost gate of a multi-fingered device would otherwise be mismatched due to undercutting of the polysilicon [10]. The layout uses multiple contacts for all connections between metal layers and substrate layers. The gate length of these devices is 2 μm, 2.5 times the minimum gate length. This minimizes the effects of channel length modulation.

The final chip schematic and layout with I/O pads are shown in Figure 27. The whole chip layout is actually fabricated on each isolator chip. The isolator system then consists of two chips, utilizing an isolated transmitter and receiver. The isolator layout dimensions are 1.986 mm by 0.563 mm. This layout easily fits on the footprint of the 3.4 mm by 3.4 mm chips.

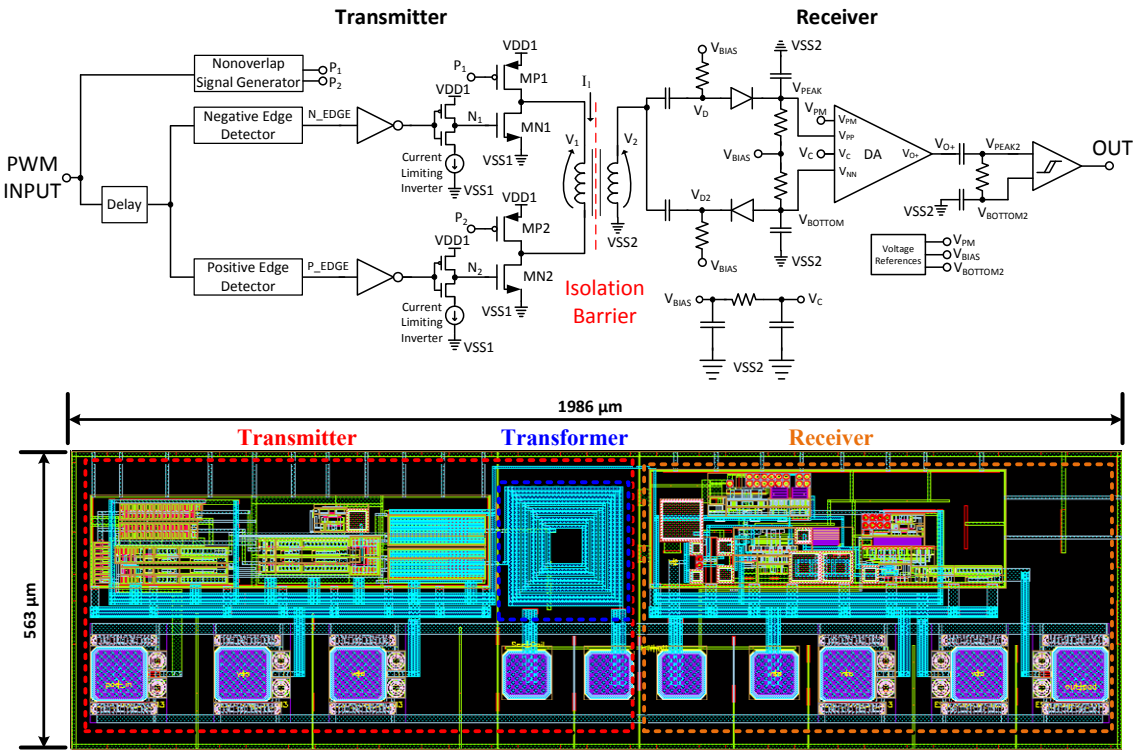

Figure 27. Final chip schematic and layout

Final Chip Simulations and Temperature Limitation

The final chip layout simulation results with parasitics show a functioning isolator design in Figure 28 at room temperature or 27℃. This simulation shows the input signal (IN), the voltage pulse (V_2), the input to the comparator (V_{PEAK2}), and the output signal (OUT). The voltage pulse is just below 1.5 V. The amplitude of V_{PEAK2} is sufficient to switch the output of the comparator. The output signal correctly matches the input PWM with a delay (latency) of 54 ns. The same simulation is shown in Figure 29 and Figure 30, but the temperature is set to 140℃ and 145℃, respectively. Figure 29 shows correct operation with increased delay. The simulation in Figure 30 shows the temperature that results in an incorrect output signal. The voltage pulse is less than 1 V, and the input to the comparator is not high enough to switch the output. The simulations predict the highest operating temperature of the isolator to be near 140℃.

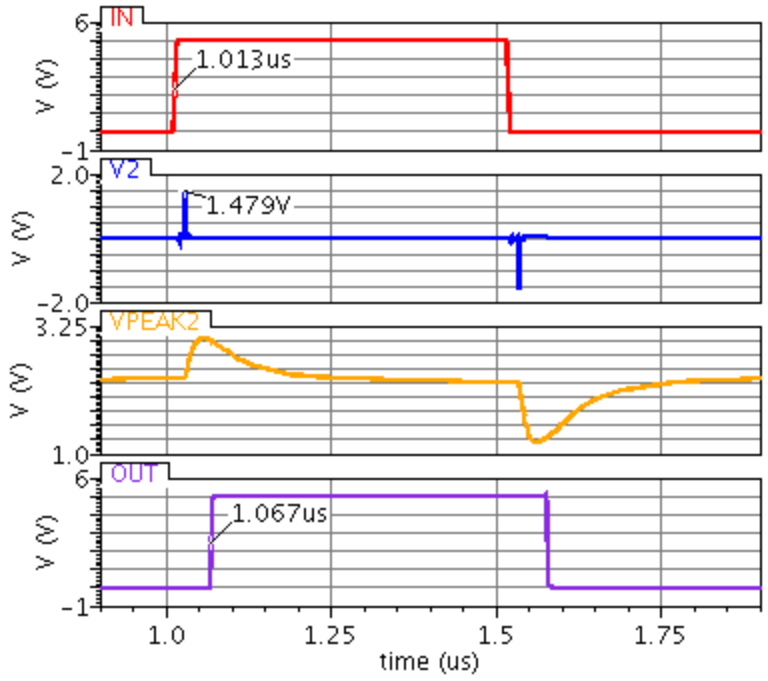

Figure 28. Final design simulation at 27℃

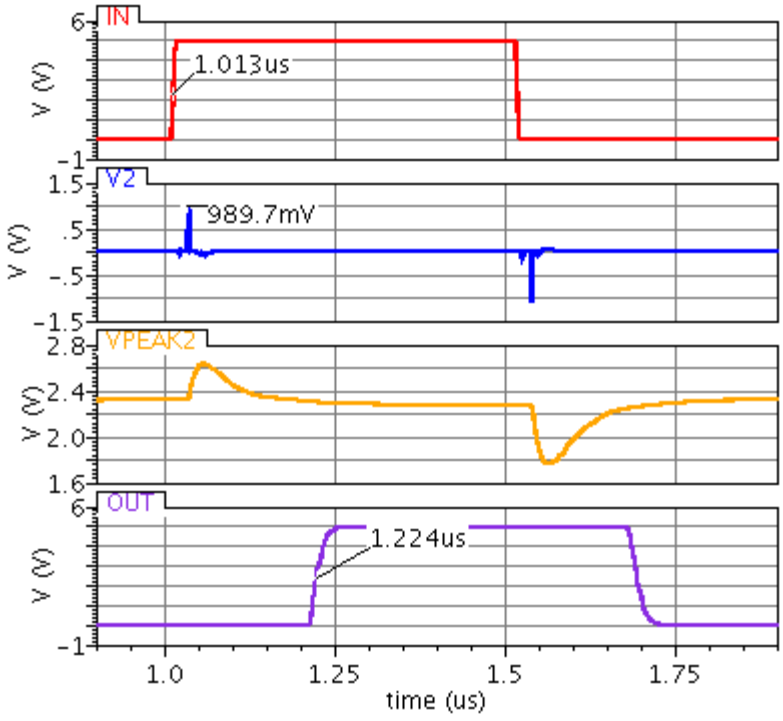

Figure 29. Final design simulation at 140℃

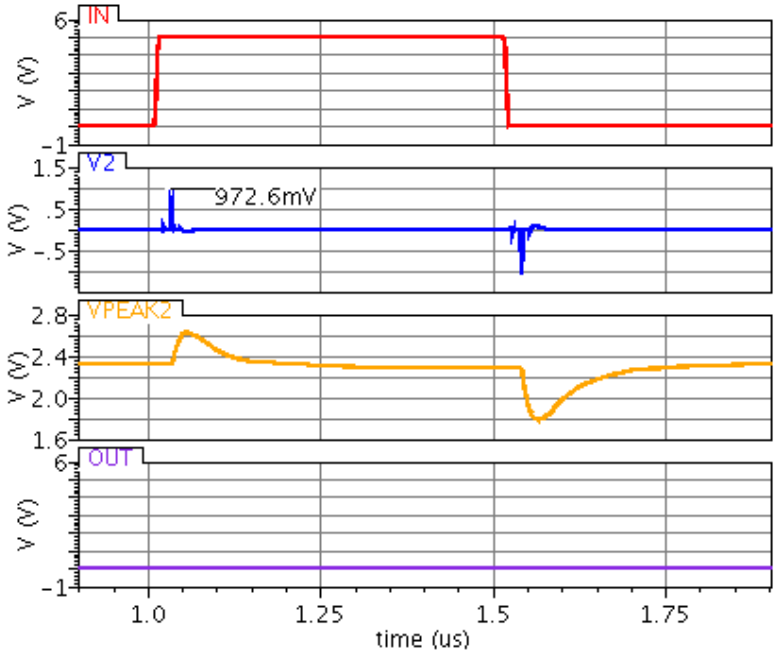

Figure 30. Final design simulation at 145℃

The reduction of the voltage pulse V_2 is the most important factor in high temperature operation. The magnitude of the pulse is established by the current flowing through the primary coil. The magnitude of the current is reduced and the rise time of the current is increased as temperature is increased. The current supplied by the drive transistors is reduced from the lowering of the devices' mobility at higher temperatures. The reduction of the current in stages preceding the drive stage at higher temperatures diminishes the rise time of the current.

Also, the simulations of the final chip layout show a large difference in total propagation delay. The delay of Figure 28 at 27℃ is around 50 ns. The delay of Figure 29 at 140℃ is over 200 ns. The node V_{PEAK2} is plotted in both simulations. This is the node at the input to the comparator, the last circuit component of the isolator system. There is some increase in delay of this signal (V_{PEAK2}) but no more than 25 ns. Therefore, the overall increase of delay is introduced mainly by the comparator. The comparator would need to be biased with more current to

improve speed performance. The current biasing has a significant effect on the switching points of the comparator. Speed and hysteresis must both be considered with the comparator design.

Isolation Capability

The RMS voltage blocking capability of the isolator is limited by the SiO_2 strength (breakdown voltage) between the transformer coils. The dielectric breakdown is lowest at the minimum thickness of SiO_2. The minimum thickness is at two places. The first is the dielectric between the overlapped coils of the primary coil on metal 3 and the secondary coil on metal 2. The second is the distance from metal 1 and metal 2 where the primary coil middle connection is routed down from metal 3 to metal 1 and out to the transmitter circuitry. Both of the minimum dielectric thicknesses are estimated to be 0.9 µm by the chip design manual. The SiO_2 dielectric is estimated to have an electric field breakdown of larger than 700 V/µm [2]. Therefore, the expected voltage limit of the isolator is no less than 630 V. This is the maximum voltage available using this chip technology and a stacked transformer design. This maximum voltage is much less than the previously reported isolators, but this design shows a proof of concept that may be applied to other chip technologies to improve the RMS blocking voltage. The main limitation of this chip technology is the availability of only three metal interconnect layers. A higher number of metal layers allows transformer coils to be separated by thicker oxide and reach higher breakdown voltages.

The CMR of the isolator design is simulated by the schematic in Figure 31. This simulation test injects a high dV/dt common-mode voltage (V_{CM}) between VSS1 and VSS2. This common-mode noise is coupled through capacitances of the transformer to the receiver side circuitry. This test demonstrates the common-mode noise injected during the phase leg operation of the motor drive application.

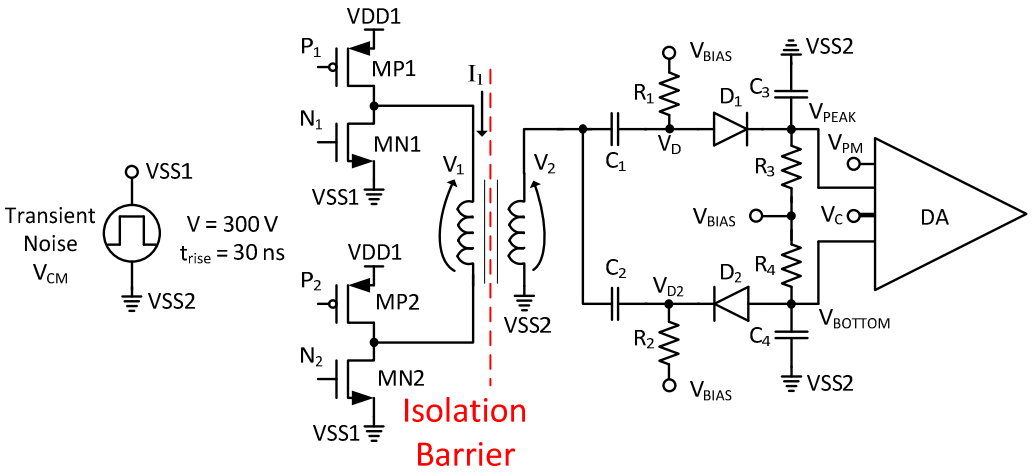

Figure 31. CMR test schematic

The simulation results of the CMR test are shown in Figure 32. The simulation measures the CMR during regular functionality, the input signal to the isolator is switching. The simulation shows the input signal (IN), the common-mode voltage rate of change (dV_{CM}/dt), the voltage pulse (V_2), nodes internal to the receiver (V_D and V_{BIAS}), and the output signal (OUT). The measured maximum common-mode voltage rate of change (dV_{CM}/dt) in the simulation is 15.7 kV/µs. The signal at V_D shows the signal after the high-pass filter in the receiver circuitry. The voltage at V_{BIAS} is an important waveform for this simulation. This voltage is the bias voltage for the pulse detection and input to the DA. While V_{BIAS} should be a DC signal, it has an amplitude of nearly 65 mV during the common-mode voltage transient. The BGR does not have a sufficiently low output impedance to correctly regulate the bias voltage during the common-mode transient. The simulation shows an output signal correctly detecting the input signal after switching HIGH, but the output is incorrectly switched LOW due to the high common-mode transient voltage before the input signal changes. From the simulation results, the estimated CMR of the isolator system is around 15 kV/µs.

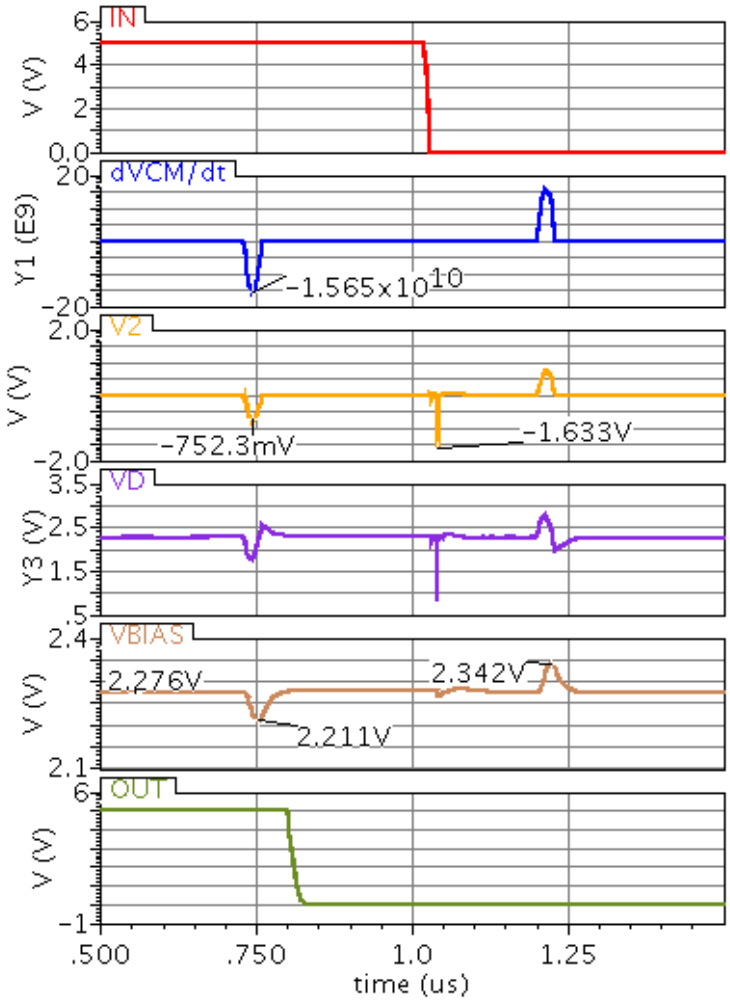

Figure 32. CMR detailed simulation

CHAPTER IV
RESULTS AND DISCUSSION

This chapter presents the measurement results of the on-chip transformer-based digital isolator system. The isolator system has been tested for functionality with various data rates, temperature operation, common-mode rejection, and high-voltage breakdown. The isolator chips are bonded directly to polyimide test boards. The test boards are shown in Figure 33. The test setup uses four isolator chips or two isolator systems in series. There are two transmitter chips labeled Tx1 and Tx2 and two receiver chips labeled Rx1 and Rx2. This setup uses two isolator systems to have two isolated ground potentials, a low voltage domain referenced from VSS1 and a high voltage domain referenced from VSS2. Tx1 and Rx2 are in the low voltage domain. Rx1 and Tx2 are in the high voltage domain. An input PWM signal can be given to either Tx1 or Tx2. The output of both Rx1 and Rx2 can be measured separately. During CMR testing, the input of Tx1 and output of Rx2 are measured in the low voltage domain; two isolators in series are measured during CMR testing.

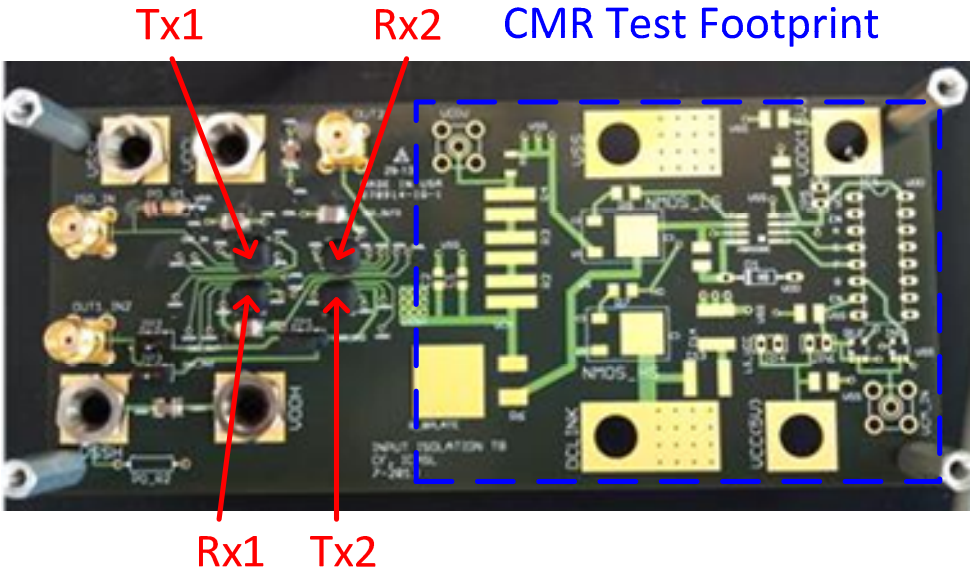

Figure 33. Isolator test board

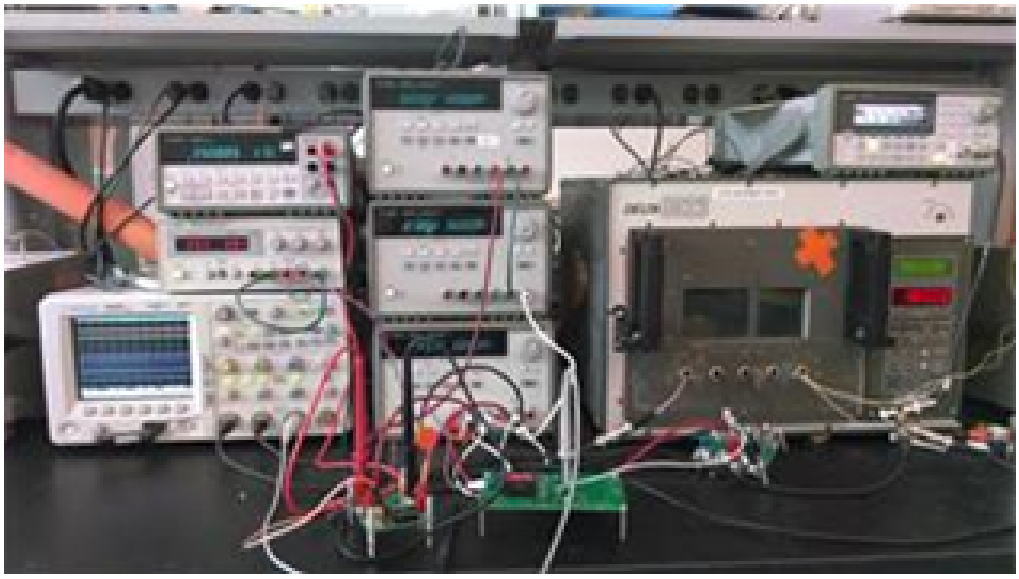

Figure 34. Isolator system test setup

The isolator test setup is shown in Figure 34. This test setup is used for the basic functionality testing, CMR testing, and high temperature testing. The basic functionality testing requires a power supply, a signal generator, and an oscilloscope. The CMR testing requires additional power supplies including an isolated 5 V power supply to reject common-mode noise. The temperature testing is performed in the temperature chamber. The polyimide isolation test board is inserted into the temperature chamber and connected out through high temperature cabling. The CMR test board sits outside the temperature chamber.

Functionality

The basic functionality testing is measured with the isolator test board. The correct functionality of the isolator is simply defined by an output signal that matches the input PWM signal. The isolator functionality is shown in Figure 35. This experiment measures the input PWM signal and the output PWM signal of the isolator. The input frequency of this test is 1 MHz. This frequency is well beyond the maximum frequency needed for the integrated power module.

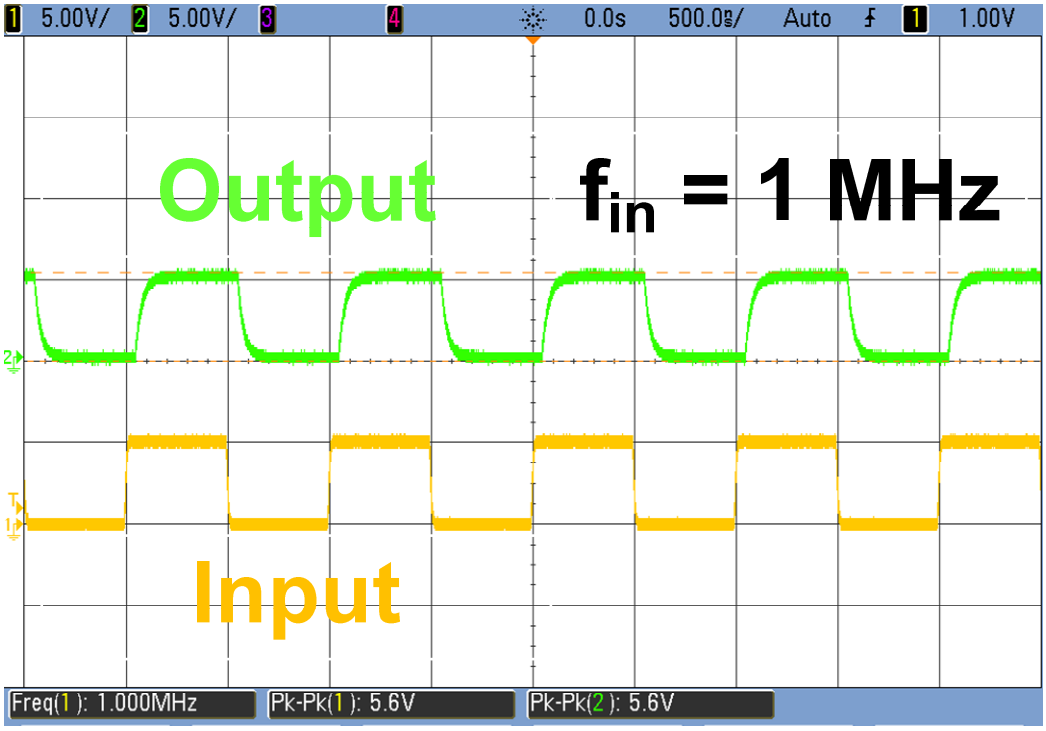

Figure 35. Functionality measurement at 1 MHz

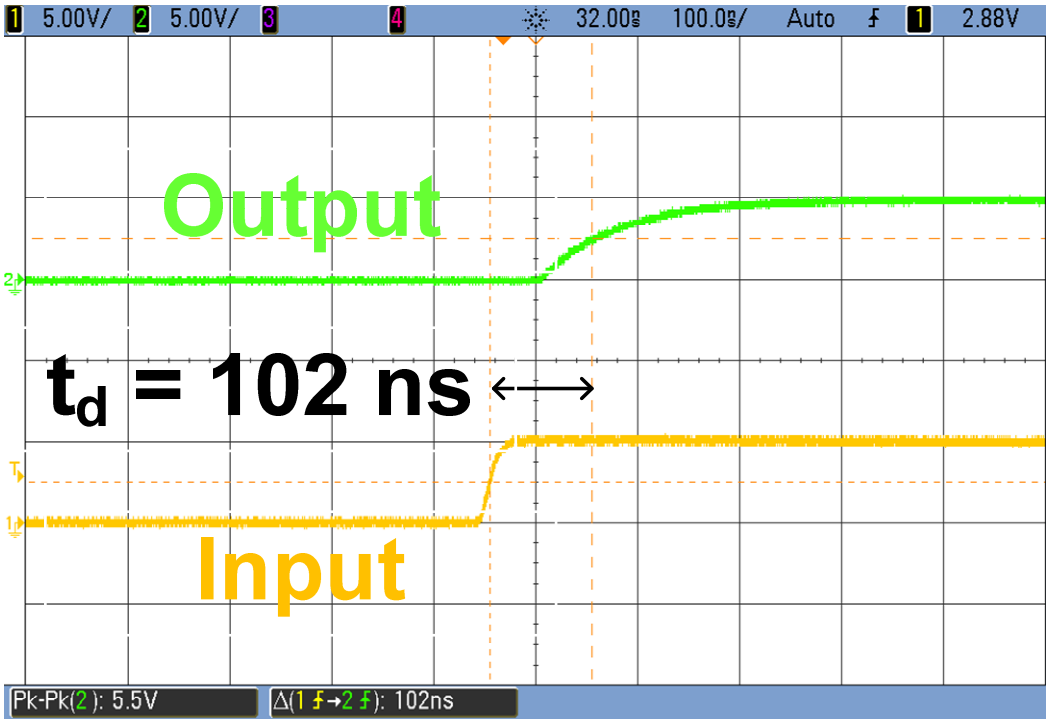

Figure 36. Propagation delay measurement at 27℃

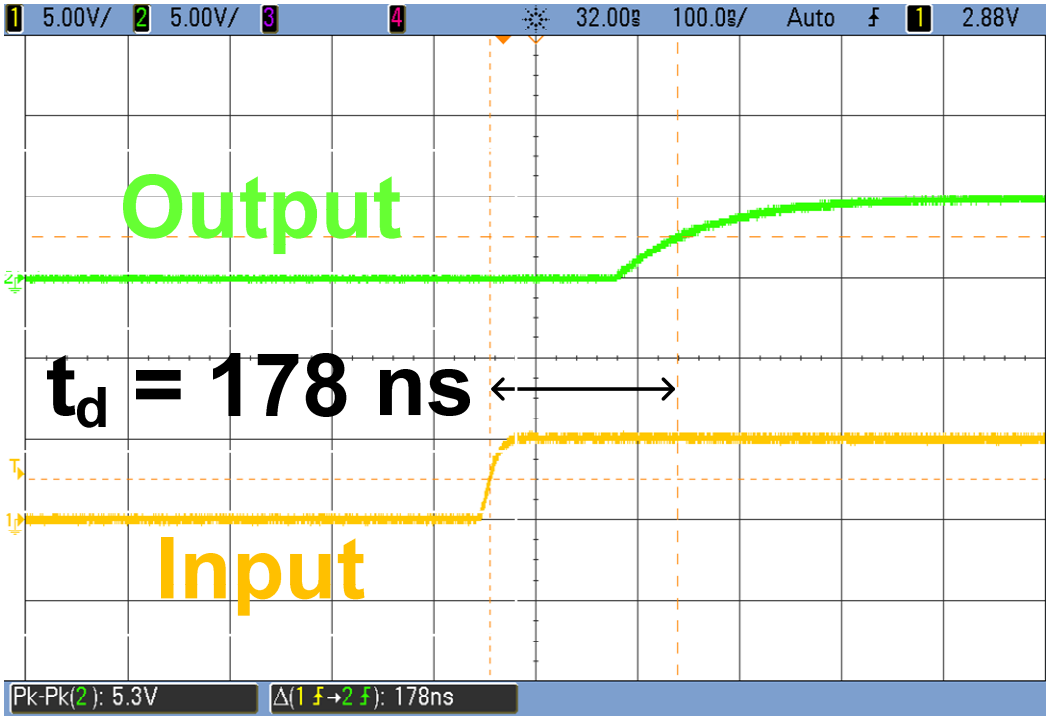

Figure 37. Propagation delay measurement at 140℃

Figure 36 is a measurement that has zoomed in on the rising edge to measure the propagation delay (t_d) from input switching to output switching. Figure 36 is measured at room temperature or 27℃. The delay demonstrated is 102 ns. Figure 37 is the same measurement but measured at 140℃. This measures the propagation delay at 140℃ to be 178 ns.

The isolator chip functionality has been demonstrated up to 150℃. Figure 38 and Figure 39 show functionality tests at high temperatures. Figure 38 shows a test at 150℃. The input and output signals are measured. The output correctly matches the input PWM signal. Figure 39 shows a test at 152℃. This test shows the high temperature operation limit of the isolator chips. The output signal is only able to detect a percentage of the input PWM transitions. When the temperature was increased a couple more degrees, the output stops detecting any of the input PWM transitions.

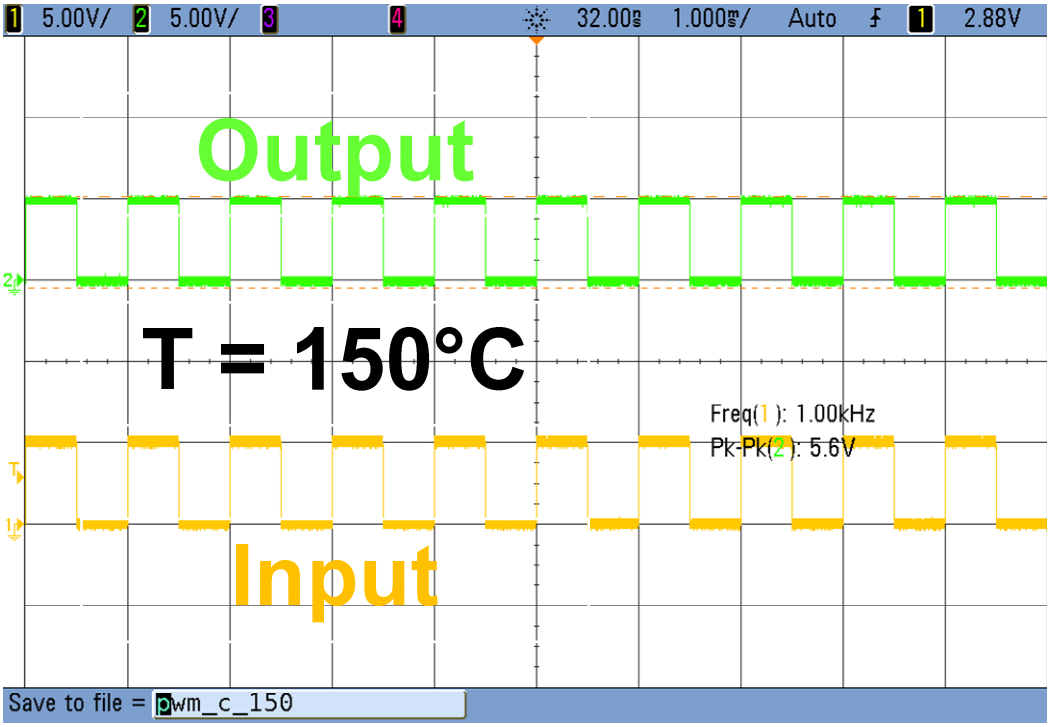

Figure 38. Temperature functionality correct at 150℃

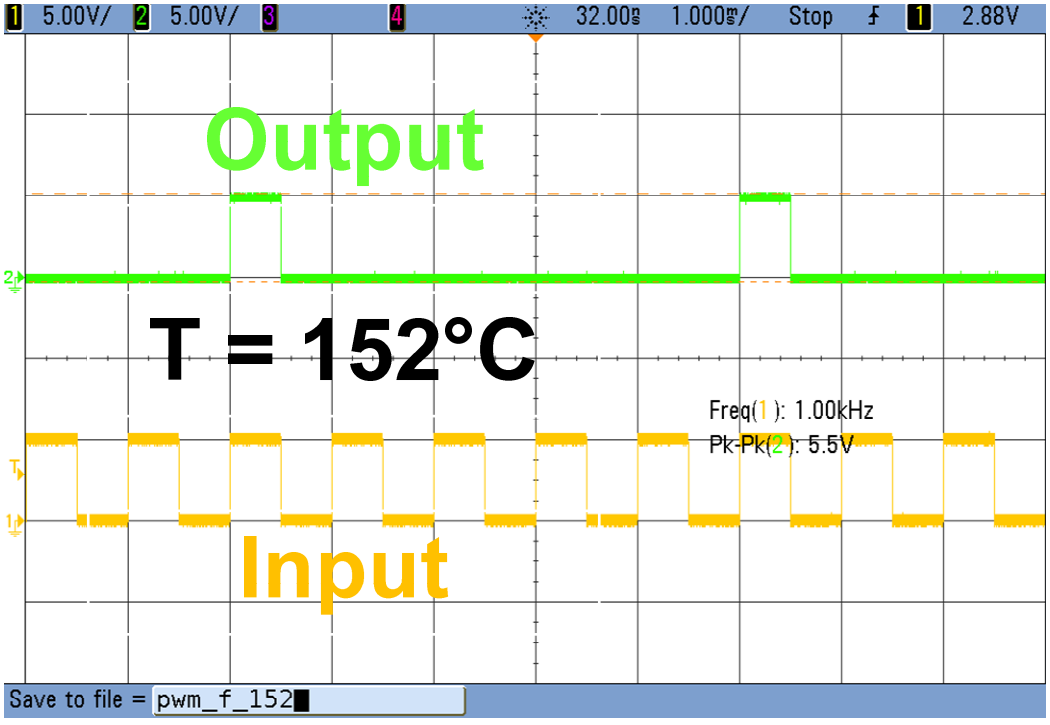

Figure 39. Temperature functionality incorrect at 152℃

Common-Mode Rejection

The common-mode rejection testing requires an additional circuit to inject a high dV/dt noise signal. The design of the CMR test is similar to the CMR test setup in [6]. The CMR test design is implemented on a separate test board as well as on the isolator test board. The separate test board is shown in Figure 40. The CMR test schematic is shown in Figure 41. The input is a PWM signal. This input is split into two complementary PWM signals. A level shifter (CD40109B) converts the 5 V complementary signals to 15 V signals. A half-bridge gate driver (FAN7380) is used to drive two 600 V NMOS transistors. The high-side of the half-bridge circuit uses a floating supply rail with its reference point connected to the potential between the half-bridge transistors. The floating potential voltage between the half-bridge transistors is connected to the node V_{CM} through an RC network. The alternating switching of the high-side and low-side transistors causes V_{CM} to switch between zero V and the HVBUS voltage. The RC network is used to adjust the dV/dt of V_{CM}. The output of the CMR test design (V_{CM}) is connected to VSS2 on the isolator test board. This injects a potential difference between VSS1 and VSS2 of the isolator test board.

Figure 40. CMR test board

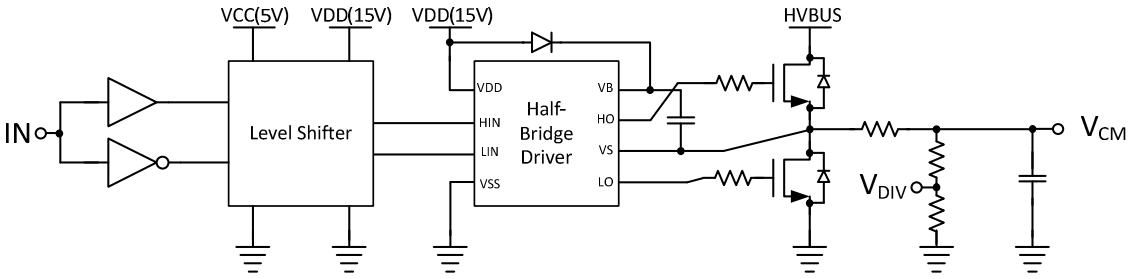

Figure 41. CMR test schematic

The next six figures show the CMR test results at 27℃. All of these waveforms measure the input PWM signal, the common-mode voltage (V_{CM}) injected into VSS2, and the output signal. Figure 42, Figure 43, and Figure 44 demonstrate a functioning isolator. Figure 42 shows multiple periods of a 1 kHz PWM input signal, a 70 V_{PP} V_{CM}, and the output PWM signal that matches the input. Figure 43 zooms in showing the positive edges of the input signal, V_{CM},

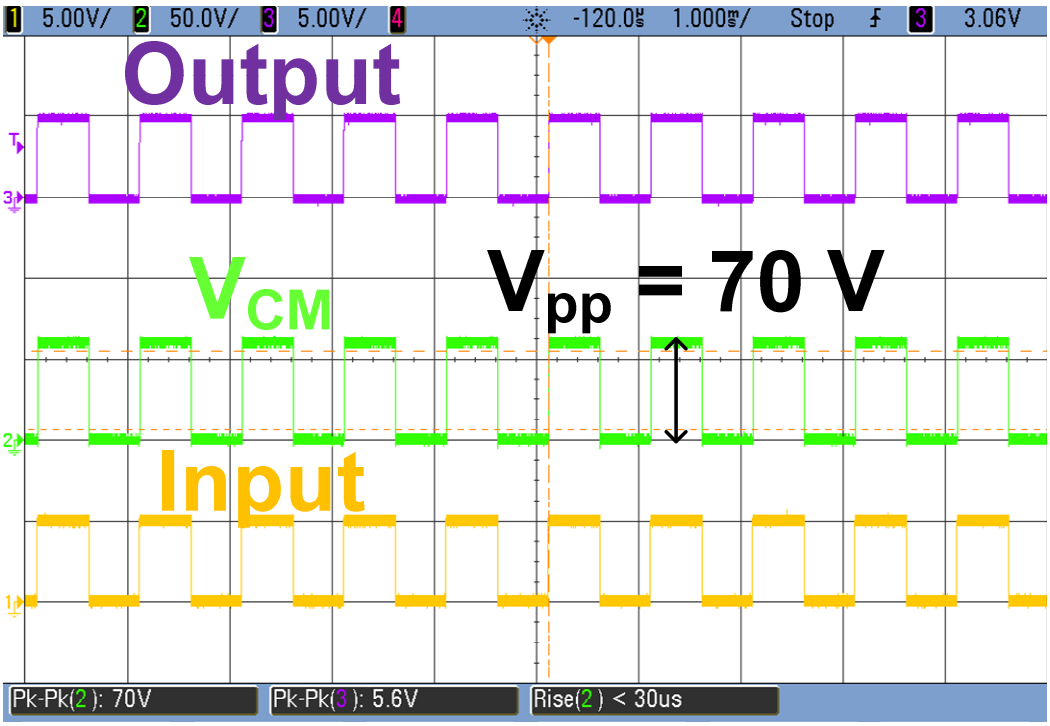

Figure 42. CMR successful test PWM functionality

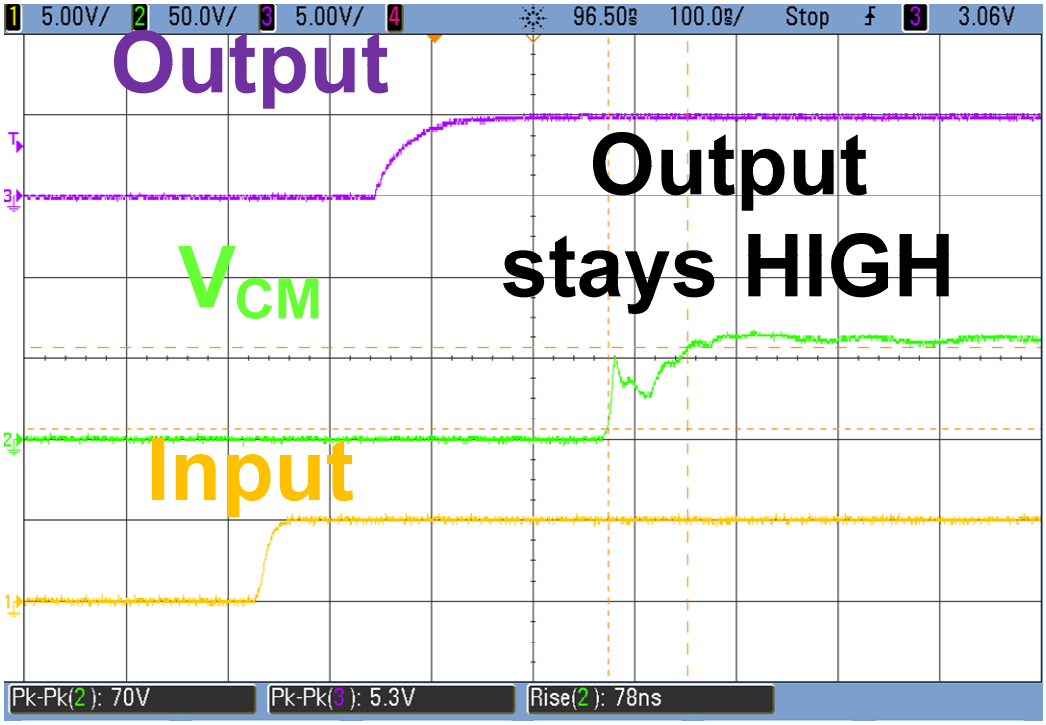

Figure 43. CMR successful test edge zoom in

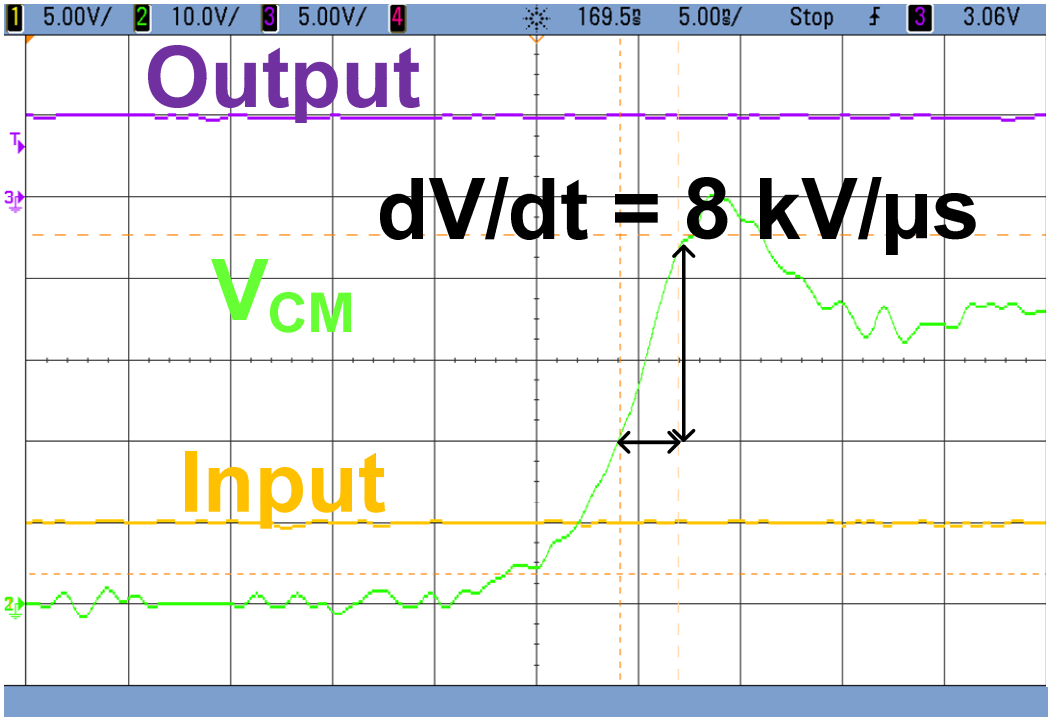

Figure 44. CMR successful test dV/dt measurement

and the output signal. After the high dV/dt noise signal is injected, the output signal continues to match the input signal. Figure 44 zooms in further to measure the dV/dt of V_{CM}. The measured dV/dt is 8 kV/µs.

Figure 45, Figure 46, and Figure 47 demonstrate a failed CMR test. Figure 45 shows multiple periods of a 1 kHz PWM input signal, a 74 V_{PP} V_{CM}, and the output PWM signal that does not detect each period of the input signal. Figure 46 zooms in to the failure point showing the positive edges of the input signal, V_{CM}, and the output signal. After the high dV/dt noise signal is injected, the output signal fails to match the input signal. Figure 47 zooms in further to measure the dV/dt of V_{CM}. The measured dV/dt is 9 kV/µs. The simulated CMR failure point of the isolator system is about 15 kV/µs. The isolator does not quite reach this level of common-mode noise rejection.

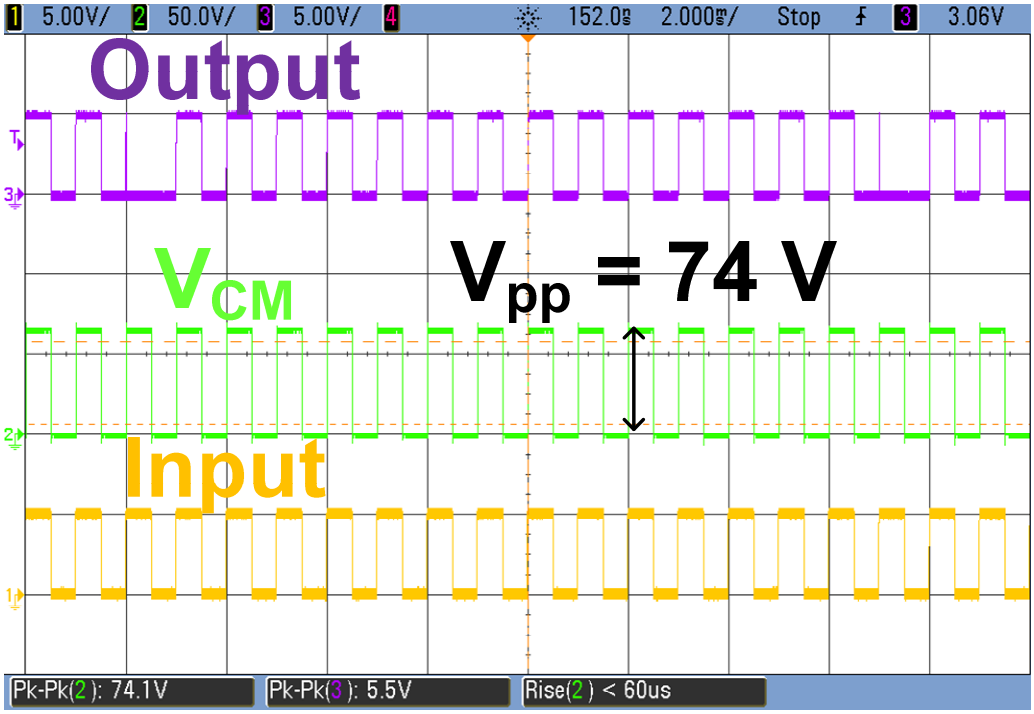

Figure 45. CMR failed test PWM functionality

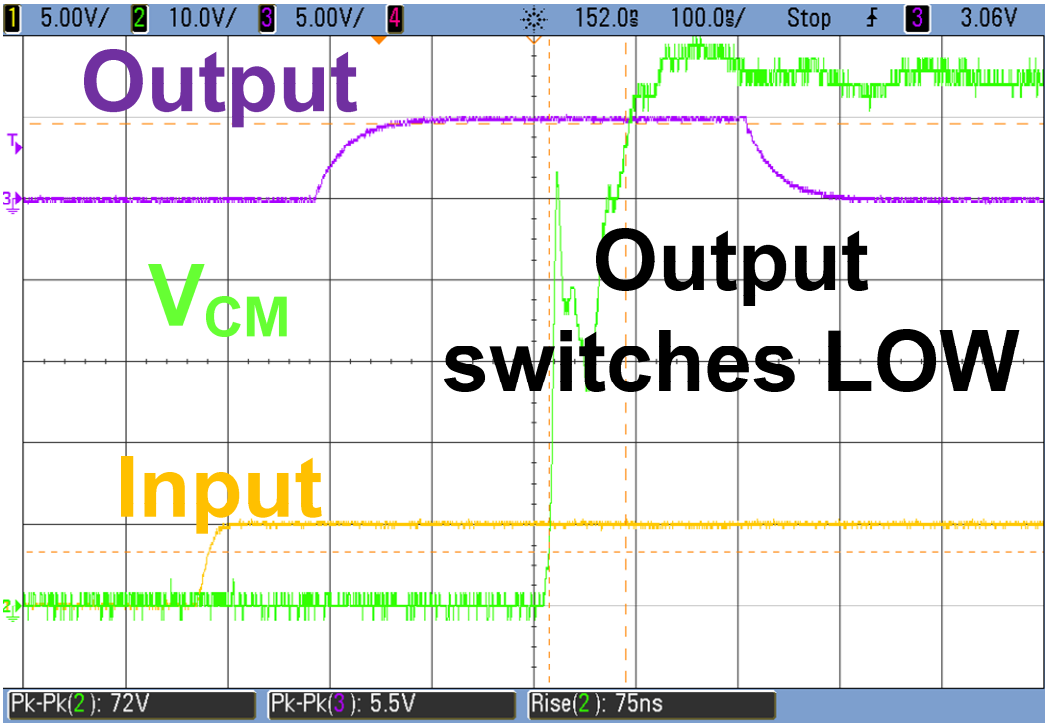

Figure 46. CMR failed test edge zoom in

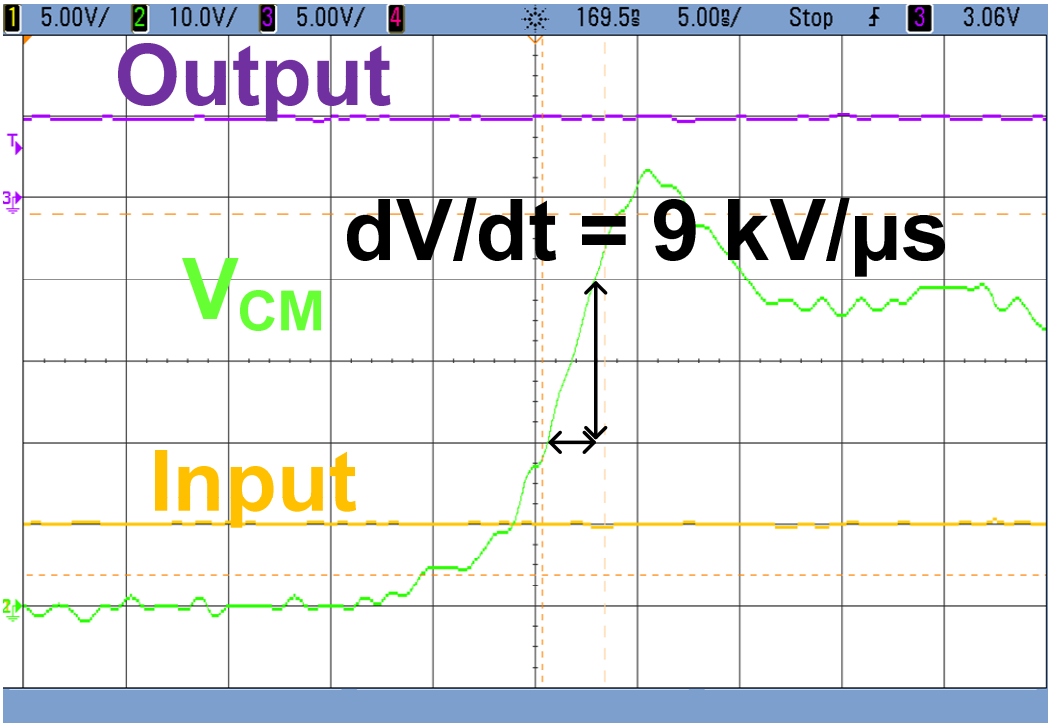

Figure 47. CMR failed test dV/dt measurement

The CMR of the isolator has also been tested at 140℃. The isolator rejects higher dV/dt at higher temperatures. Figure 48 and Figure 49 demonstrate a functioning isolator at 140℃. Figure 48 shows multiple periods of a 10 kHz PWM input signal, a 109 V_{PP} V_{CM}, and the output PWM signal that matches the input. Figure 49 zooms in further to measure the dV/dt of V_{CM}. The measured dV/dt is 12 kV/μs. The DC level at 100 V of V_{CM} used in this test is near the maximum allowable voltage of the power supplies in the test setup.

High-Voltage Breakdown

The high-voltage test is conducted with the isolator test board. The isolators are treated as two terminal devices to test the high-voltage breakdown. All nodes on the low-voltage side are connected together, and all nodes on the high-voltage side are connected together. A high voltage is applied across the insulating dielectric to determine the maximum operating RMS voltage and failure point. The high-voltage experiment tests two isolators on the test board simultaneously. The first one to fail gives the breakdown voltage.

The high-voltage test was conducted by slowly raising the DC voltage across the chips until a failure occurred. The isolator system failed at 700-V RMS. This voltage is near the SiO_2 breakdown of 700 V/μm. The estimated SiO_2 thickness is 0.9 μm. The test board after the high-voltage test is shown in Figure 50. The image clearly shows that the isolator consisting of Tx2 and Rx2 failed. There is visible damage of these two chips.

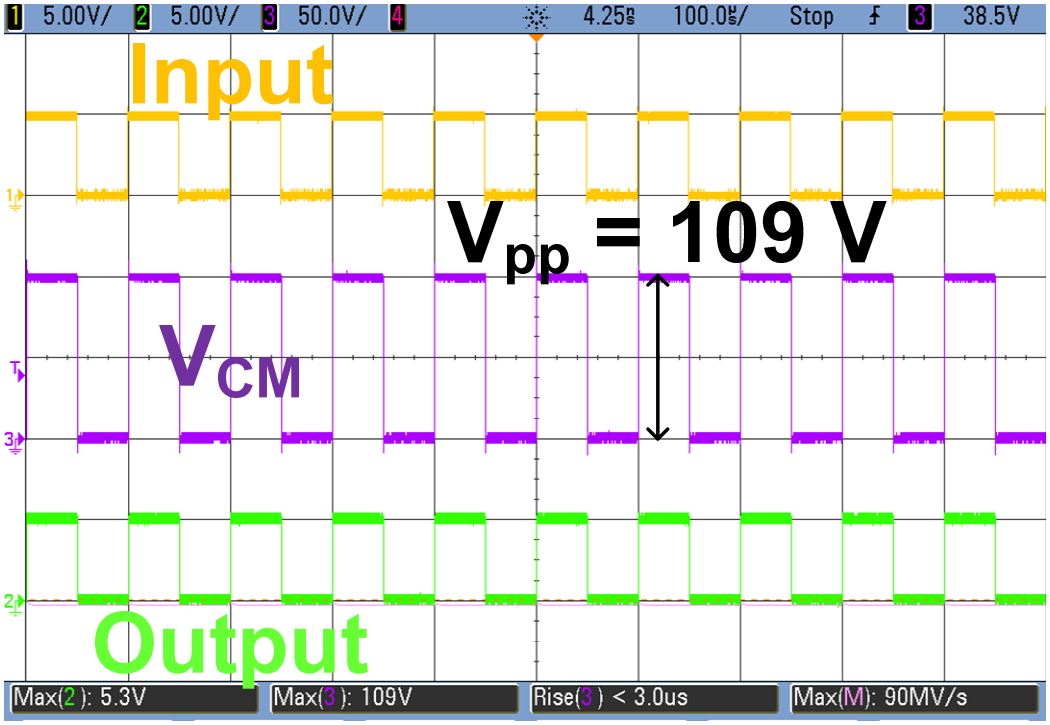

Figure 48. CMR successful test PWM functionality at 140℃

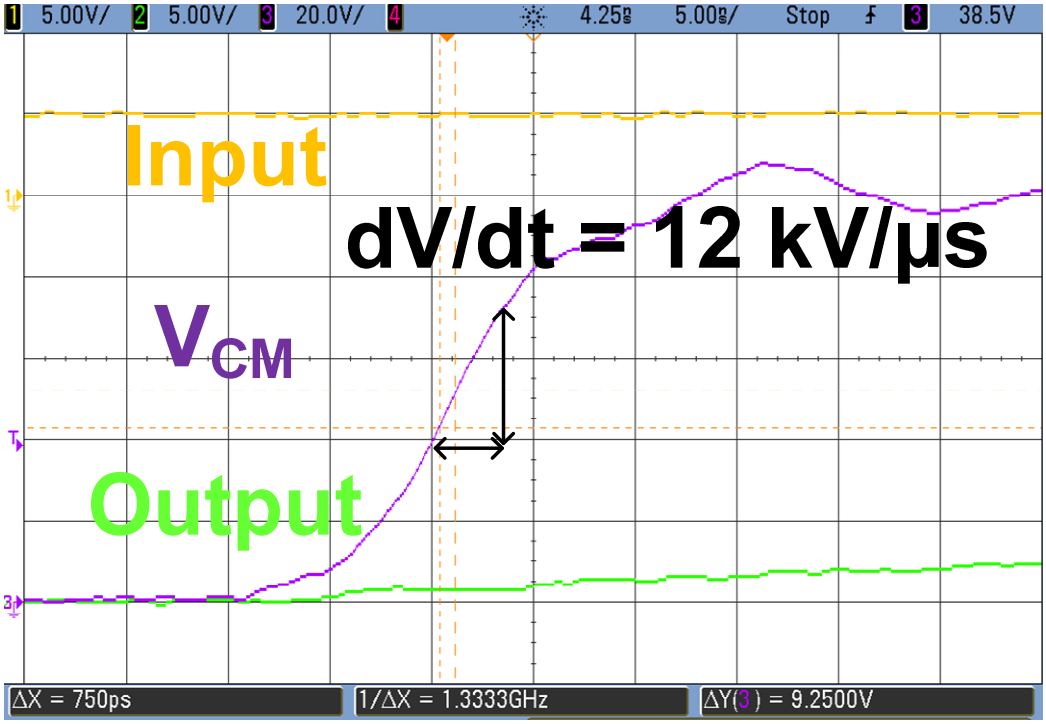

Figure 49. CMR successful test dV/dt measurement at 140℃

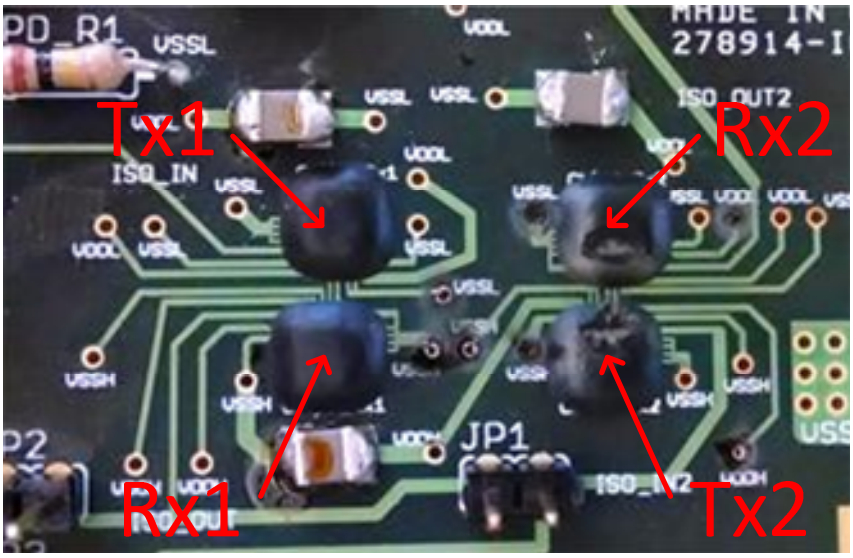

Figure 50. Isolator test board after high-voltage test

CHAPTER V
CONCLUSIONS

Conclusions

This thesis presents an on-chip transformer-based digital isolator system. The chip design is fabricated in a 0.8 μm SOI chip technology. The isolator system consists of two isolated chips, a transmitter and receiver. An on-chip transformer model has been investigated and implemented. The total chip area of the transmitter and receiver is about 1.1 mm^2.

The chips have been fabricated and bonded directly on polyimide test boards. The isolator has been tested for functionality, temperature operation, CMR, and high-voltage breakdown. At room temperature, the output of the isolator correctly matches the input signal up to 5 MHz, or 10 Mbps, with a propagation delay around 100 ns. The isolator stops functioning just over 150°C. The CMR capability measured is 8 kV/μs. The breakdown voltage has been tested and measured at 700-V RMS. The performance of the presented isolator is compared with other technologies in Table 2. The future work row in the table is the second isolator prototype being fabricated during the publication of this document. This second prototype is discussed in the future work section. The transformer comparison column data is mostly from [6].

Future Work

The fabricated SOI isolator has verified many elements of the design. Simulations and experimental results have verified the transformer model and signaling scheme. With the experience and knowledge from the chip design, fabrication, and testing, many improvements may be made to the operation of the isolator.

A second isolator design with the same topology is being fabricated in a process that has more metal layers. This design will have a much higher breakdown voltage, estimated to be 2.4-kV RMS. The circuit design has also

Table 2. Isolator performance comparison

	Isolator Type	Relative Transformer Area	Data Rate (Mbps)	Voltage Blocking (kV RMS)	Common-Mode Rejection (kV/µs)
6N137 [5]	Optocoupler	-	10	3.75	15
ISO72x [1]	Capacitive	-	150	2.5	25
ADuM1100 [8]	Transformer	8	100	2.5	25
CMOS [6]	Transformer	1	250	2.5	35
This Work	Transformer	1	10	0.7	8
Future Work	Transformer	1	10	2.4	>50

been improved to reject higher common-mode noise. Simulations show a functioning isolator with a common-mode noise transient of at least 50 kV/µs. The main circuit change is a voltage regulator for the receiver circuitry. The regulator introduces lower output impedance for the bias voltages in the receiver circuit. The regulated voltage is less susceptible to common-mode noise.

A future SOI chip fabrication could also be used to improve the isolator. The isolation voltage will still be limited by the number of metal layers and a stacked transformer design. However, the circuitry could be altered to reject higher common-mode transients and operate at higher temperatures. The higher CMR could be achieved from the addition of a voltage regulator in the receiver circuitry. The main limitation at high temperatures is the reduced voltage pulse input to the receiver. The drive stage circuitry could be investigated more to reduce the rise time of the current in the primary coil. Also, the transformer could be further investigated to increase the voltage pulse. A higher inductance of the coils could result in a larger magnitude of the voltage pulse; however, the increased parasitics from a larger coil could result in diminishing returns as the transformer size is increased. The receiver circuitry could also be adjusted. The

high-pass filter, diode threshold, and comparator hysteresis are circuit elements that could be investigated to improve the temperature performance.

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VITA

Cory Fandrich was born on September, 11 1987 in Winchester, TN. He grew up in Franklin County and graduated from Franklin County High School in 2006. He graduated with a Bachelor of Science in Electrical Engineering from the University of Tennessee in 2011. After graduating, he began pursuing a master's degree in electrical engineering. He worked as a graduate research assistant in the Integrated Circuits and Systems Laboratory under the advisement of Dr. Benjamin Blalock.