



12-2003

## Silicon Carbide GTO Thyristor Loss Model for HVDC Application

Madhu Sudhan Chinthavali  
*University of Tennessee - Knoxville*

Follow this and additional works at: [https://trace.tennessee.edu/utk\\_gradthes](https://trace.tennessee.edu/utk_gradthes)



Part of the [Electrical and Computer Engineering Commons](#)

---

### Recommended Citation

Chinthavali, Madhu Sudhan, "Silicon Carbide GTO Thyristor Loss Model for HVDC Application. " Master's Thesis, University of Tennessee, 2003.  
[https://trace.tennessee.edu/utk\\_gradthes/1915](https://trace.tennessee.edu/utk_gradthes/1915)

This Thesis is brought to you for free and open access by the Graduate School at TRACE: Tennessee Research and Creative Exchange. It has been accepted for inclusion in Masters Theses by an authorized administrator of TRACE: Tennessee Research and Creative Exchange. For more information, please contact [trace@utk.edu](mailto:trace@utk.edu).

To the Graduate Council:

I am submitting herewith a thesis written by Madhu Sudhan Chinthavali entitled "Silicon Carbide GTO Thyristor Loss Model for HVDC Application." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Leon M. Tolbert, Major Professor

We have read this thesis and recommend its acceptance:

J. S. Lawler, Syed K. Islam

Accepted for the Council:

Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

To the Graduate Council:

I am submitting herewith a thesis written by Madhu Sudhan Chinthavali entitled "Silicon carbide GTO thyristor loss model for HVDC application." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Leon M. Tolbert  
Major Professor

We have read this thesis  
and recommend its acceptance:

J. S. Lawler

Syed K. Islam

Accepted for the Council:

Anne Mayhew

Vice Provost and Dean  
of Graduate Studies

(Original signatures are on file with official student records)

**SILICON CARBIDE GTO THYRISTOR LOSS MODEL  
FOR HVDC APPLICATION**

A Thesis Presented for the  
Master of Science  
Degree  
The University of Tennessee, Knoxville

Madhu Sudhan Chinthavali  
December 2003

## **Dedication**

This thesis is dedicated to my parents

Varalakshmi Chinthavali

and

Kedharinath Chinthavali

## **Acknowledgements**

I am thankful to everyone who has helped me finish my thesis. I am grateful to my advisor Dr. Leon M. Tolbert for having supported me financially and academically in my master's degree program.

I would like to thank my committee faculty members Dr. Islam and Dr. Lawler for guiding me with valuable advices during my thesis.

I am also thankful to my lab mates for supporting me in my program, especially Jianqing Chen for his moral support and for the discussions.

I am really thankful to all my friends at UTK who have made my stay at Knoxville a memorable one.

## **Abstract**

With the increase in use of power electronics in transmission and distribution applications there is a growing demand for cost effective and highly efficient converters. Most of the utility applications have power electronics integrated in the system to improve the efficiency and functionality of the existing system. The development of semiconductor devices is vital for the growth of power electronic systems. Modern technologies like voltage source converter (VSC) based HVDC transmission has been made possible with the advent of power semiconductor devices like IGBT and GTO thyristor with their high power handling capability.

Various material limitations of silicon power semiconductor devices have led to the development of wide bandgap semiconductors such as SiC, GaN, and diamond. Silicon carbide is the most advanced amongst the available wide bandgap semiconductors and is currently in the transition from research to manufacturing phase. This project presents the modeling and design of a loss model of 4H-SiC GTO thyristor device, and the effect of device benefits at system level are studied. The device loss model has been developed based on the device physics and device operation, and simulations have been conducted for various operating conditions. The thesis focuses on the study of a comparison between silicon and silicon carbide devices in terms of efficiency and system cost savings for HVDC transmission system.

## Table of Contents

Chapter	Page
<b>1.High Voltage DC Transmission .....</b>	<b>1</b>
1.1 Objective .....	1
1.2 Outline of Thesis.....	1
1.3 Introduction.....	2
1.4 Why HVDC?.....	3
1.5 HVDC Constraints.....	4
1.6 Basic HVDC System Configurations .....	5
1.7 Components of an HVDC Transmission System.....	8
1.7.1 The converter station.....	8
1.7.2 Converter Transformer.....	10
1.7.3 Converter.....	10
1.7.4 Smoothing Reactors.....	14
1.7.5 AC Filters.....	14
1.7.6 DC Filters.....	14
1.7.7 Transmission Medium .....	15
1.8 HVDC Technology .....	15
1.8.1 Selection of Converter Configuration.....	15
1.8.2 HVDC Operation .....	19
1.8.3 Control and Protection .....	23
1.9 Areas for Development in HVDC Converters.....	25
<b>2. Silicon Carbide Technology .....</b>	<b>27</b>



2.1	Silicon Carbide.....	30
2.2	Silicon Carbide Lattice Structure.....	31
2.3	Properties of Silicon Carbide.....	33
2.4	Silicon Carbide Power Devices .....	41
<b>3.</b>	<b>Silicon Carbide Gate Turn-off Thyristor .....</b>	<b>46</b>
3.1	GTO Structure.....	48
3.2	Static Characteristics of GTO .....	50
3.2.1	On-State Characteristics and Turn-on Process .....	50
3.2.2	GTO Turn-off Process .....	55
3.3	GTO Switching.....	56
3.3.1	Turn-on Process .....	57
3.3.2	Turn-off process.....	59
3.4	Device Model.....	60
3.4.1	Device Structure.....	61
3.4.2	Conduction Losses.....	62
3.4.3	Switching Losses .....	66
3.5	Simulations .....	71
<b>4.</b>	<b>System .....</b>	<b>83</b>
4.1	VSC Technology.....	83
4.1.1	Basic Structure.....	85
4.1.2	Operating principle .....	87
4.2	Converter Rating Improvement .....	89
4.3	HVDC System .....	91

4.3.1 System Specifications .....	92
4.3.2 Control System .....	92
4.4 System Simulations.....	97
4.5 Results.....	100
4.5.1 Efficiency Calculation .....	107
4.5.2 System Cost .....	116
<b>5. Conclusion .....</b>	<b>119</b>
<b>6. Future Research Work.....</b>	<b>123</b>
<b>References.....</b>	<b>124</b>
<b>Vita .....</b>	<b>128</b>

## List of Tables

Table 2.1. List of Electrical and Physical Properties of Some Semiconductors.....	41
Table 3.1 List of terms used in the equations .....	65
Table 3.2 Simulation Data .....	70
Table 3.3 Data for Mobility Calculation.....	75
Table 4.1 Efficiency of Si GTO Converter's Controlled Switches .....	110
Table 4.2 Efficiency of SiC GTO Converter's Controlled Switches.....	110
Table 4.3 Efficiency of SiC GTO Converter's Controlled Switches.....	113
Table 4.4 Efficiency of SiC GTO Converter's Controlled Switches.....	114
Table 4.5 SiC Converter's Controlled Switches Cost Savings compared to Si-based Converter.....	116

## List of Figures

<b>Figure</b>	<b>Page</b>
1-1 Five basic configurations of HVDC transmission.....	6
1-2 HVDC substation configuration .....	9
1-3 Components of thyristor valve .....	12
1-4 Current converter.....	17
1-5 Voltage converter .....	17
1-6 HVDC operation.....	20
1-7 Steady state $U_d$ - $I_d$ characteristics for a two terminal HVDC system.....	24
2-1 Tetrahedral silicon carbide structure .....	32
2-2 Planar stacking sequence.....	33
2-3 Stacking sequences of the polytypes .....	34
2-4 Bandgap variation with temperature.....	36
2-5 Electron mobility vs. doping concentration.....	39
2-6 Hole mobility vs. doping concentration .....	39
3-1 GTO symbol .....	47
3-2 Two-transistor model of GTO .....	47
3-3 Ideal characteristics of a gate turn-off thyristor.....	47
3-4 (a), (b) Four layer structure of GTO .....	48
3-5 Concentric layout structure.....	49
3-6 Involute layout structure.....	49

3-7 Complementary asymmetric SiC GTO thyristor structure .....	51
3-8 V-I characteristics of GTO thyristor.....	51
3-9 Complementary asymmetric GTO thyristor .....	52
3-10 Open base breakdown characteristics vs. current gains npn and pnp transistors .....	54
3-11 Maximum turn-off gain vs. transistor gains for top and bottom transistors .....	57
3-12 Turn-on characteristics of 4H-SiC GTO switching process .....	58
3-13 Turn-off characteristics of 4H-SiC GTO switching process .....	59
3-14 Device structure of SiC GTO thyristor used in simulations.....	61
3-15 Conduction losses of Si and SiC GTO thyristor.....	64
3-16 Switching losses of Si and SiC GTO thyristor .....	67
3-17 Comparison waveforms for Si and SiC switching.....	68
3-18 Simulink device model .....	69
3-19 Device simulation for $J = 100 \text{ A/cm}^2$ , $T = 300\text{K}$ .....	72
3-20 Device simulation for $J = 500 \text{ A/cm}^2$ , $T = 300\text{K}$ .....	73
3-21 Device simulation for $J = 300 \text{ A/cm}^2$ , $V = 10000\text{V}$ .....	74
3-22 Mobility calculations of electrons and holes for Si and SiC .....	76
3-23 Device simulation for $J = 200 \text{ A/cm}^2$ , $V = 5000 \text{ V}$ .....	78
3-24 Device simulation for $J = 400 \text{ A/cm}^2$ , $V = 10000 \text{ V}$ .....	79
3-25 Device simulation for $J = 200 \text{ A/cm}^2$ , $V = 10000\text{V}$ .....	80
3-26 Switching losses of SiC GTO thyristor .....	82
3-27 Switching losses of SiC GTO thyristor .....	82
4-1 Basic configuration of VSC transmission .....	85
4-2 Equivalent circuit of VSC transmission .....	87

4-3	Phasor diagram .....	<b>88</b>
4-4	Series connection and protection for voltage rating .....	<b>90</b>
4-5	Parallel connection for current rating .....	<b>90</b>
4-6	3-Phase full-bridge six-valve converter.....	<b>91</b>
4-7	Overview of the HVDC control system .....	<b>94</b>
4-8	Reactive power controller at the sending end.....	<b>95</b>
4-9	Power flow controller .....	<b>96</b>
4-10	Voltage controller at the receiving end.....	<b>98</b>
4-11	dc voltage controller at the receiving end.....	<b>98</b>
4-12	SIMULINK interface with PSCAD/EMTDC.....	<b>98</b>
4-13	SIMULINK interface block.....	<b>100</b>
4-14	Voltage and current profiles from PSCAD/EMTDC .....	<b>101</b>
4-15	Voltage and current profiles from PSCAD/EMTDC (zoomed).....	<b>102</b>
4-16	Loss profile and diode current for SiC GTO (373 K).....	<b>102</b>
4-17	Loss profile for SiC GTO (300 K).....	<b>103</b>
4-18	Loss profile for SiC GTO (423 K).....	<b>103</b>
4-19	Loss profile for SiC GTO (473 K).....	<b>104</b>
4-20	Loss profile for Si GTO (373 K) .....	<b>104</b>
4-21	Loss profile for Si GTO (300 K) .....	<b>105</b>
4-22	Loss profile for Si GTO (423 K) .....	<b>105</b>
4-23	Loss profile for Si GTO (473K) .....	<b>106</b>
4-24	Cyclic power loss plots for Si 5kV, 200 A/cm <sup>2</sup> GTO.....	<b>108</b>
4-25	Cyclic power loss plots for SiC 20 kV, 200 A/cm <sup>2</sup> GTO .....	<b>109</b>

4-26 Converter's controlled switches efficiency plot .....	111
4-27 Cyclic power loss plots for Si 5kV, 400A/cm <sup>2</sup> GTO .....	112
4-28 Converter's controlled switches efficiency plot .....	113
4-29 Cyclic power loss plots for 5kV, 200A/cm <sup>2</sup> SiC GTO.....	115
4-30 Converter's controlled switches efficiency plot .....	115

# **1.High Voltage DC Transmission**

## **1.1 Objective**

The main objective of the thesis is twofold

- To develop the loss models for Si and SiC GTO thyristors to study the impact of these devices on the HVDC system.
- Compare the performance of the HVDC system with Si and SiC GTO in terms of
  - (i) Efficiency
  - (ii) System cost savings

## **1.2 Outline of Thesis**

The basics of HVDC transmission to be discussed in this chapter will be used to develop a HVDC system model in the later chapters. The following chapters discuss the effect of replacing Si GTO thyristor with a SiC thyristor in a HVDC converter.

Chapter 2 presents the structural properties and physical characteristics of SiC material. The advantages of SiC power devices and their applications in power systems are also discussed.

In Chapter 3, the GTO thyristor structure and its operation will be discussed briefly, and the various structural properties and physical characteristics of SiC material discussed in chapter 2 will be used to develop a GTO thyristor loss model. The individual Si and SiC device simulations will be presented and discussed.



In chapter 4, the HVDC system model based on VSC technology will be presented, and the system simulations obtained using the Si and SiC GTO thyristor loss models are discussed to study the impact of SiC GTO on the system.

Chapter 5 summarizes the advantages of using SiC GTO thyristor instead of its Si counterpart and discusses the future of SiC devices.

### **1.3 Introduction**

The history of electric power transmission reveals that transmission was originally developed with dc. However, dc power at low voltage could not be transmitted over long distances, thus it led to the development of alternating current (ac) electrical systems. Also the availability of transformers and improvement in ac machines led to the greater usage of ac transmission. The advent of the mercury arc valve for high power and voltage proved to be a vital breakthrough for High Voltage Direct Current (HVDC) transmission. These mercury valves were the key elements in the converter stations, and the filtering was done using oil immersed components. The control was analog and most of the operations were left to the operator. After enough experiments were conducted on mercury valves, the first HVDC line was built in 1954 and was a 100 km submarine cable with ground return between the island of Gotland and the Swedish mainland.

The development of thyristors is another milestone in the development of HVDC technology. The first solid-state semiconductor valves were commissioned in 1970. The mercury arc valves in the primitive projects were replaced by thyristor valves. The semiconductor devices like thyristors, IGBTs and GTOs, in conjunction with microcomputers and digital signal processors have proved to be very effective compared

to older mercury valves. The wider usage of semiconductor technology in present day HVDC systems has initiated great leaps in the research of power electronics. With increased demand for high quality power, application of power electronics in the field of power distribution and transmission systems is attracting wide attention throughout the world.

#### 1.4 Why HVDC?

There are many different reasons as to why HVDC is chosen instead of ac transmission. A few of them are listed below.

- Cost effective

HVDC transmission requires only two conductors compared to the three wire ac transmission system. One-third less wire is used, thus readily reducing the cost of the conductors. This corresponds to reduced tower and insulation cost, thereby resulting in cheaper construction. However, the ac converters stations involve high cost for installation; thus, the earlier advantage is offset by the increase in cost. If the transmission distance is long, a **break-even distance** is reached above which total cost of HVDC transmission is less than the ac.

- Asynchronous tie

HVDC transmission has the ability to connect ac systems of different frequencies. Thus it can be used for intercontinental asynchronous ties. For example, in Japan HVDC could be used to connect an ac system operating at 60 Hz with one operating at 50 Hz.

- Lower line losses

Similar to ac transmission, HVDC transmission has  $I^2R$  losses too. However, for the same amount of power transfer, dc losses are less due to the lower resistance of the conductors because of only two-thirds of the conductor length. The main losses are converter losses.

- Offers better stability and control
- Ensures low environmental impact and reduces construction time.

### **1.5 HVDC Constraints**

Even though HVDC has many advantages, the whole power system cannot be made dc, because of the fact that generation and distribution of power is ac. So HVDC technology is restricted to transmission. As no system is perfect, even HVDC transmission has some disadvantages and drawbacks. A few of them are listed below,

- Converter station costs

The power electronic converters involve high installation and maintenance costs. This expenditure offsets the cost savings mentioned as one of the advantages; for this reason, short overhead HVDC lines are more expensive compared to ac.

- Reactive power requirement

Both the rectifier and inverter in converter stations consume large amounts of reactive power (VARs). Even though the capacitors used in the converters supply reactive power to some extent, the rest should be supplied by additional capacitors or taken from the ac system.

- Harmonics

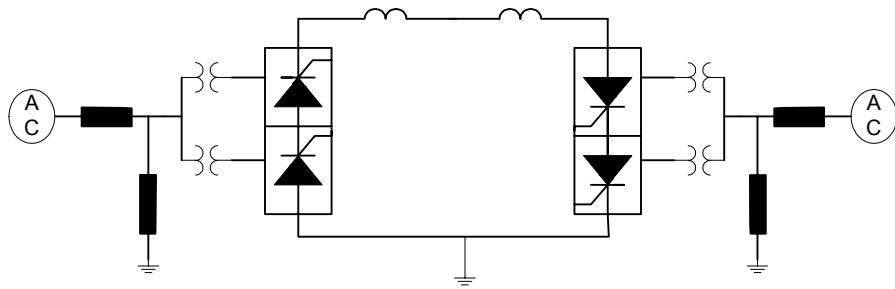
- Converters at both ends of an HVDC system inject a certain amount of harmonics into the ac system. These harmonics may cause interference to the nearby telecommunication network, and hence need to be filtered. The harmonic frequencies can be suppressed using capacitors and reactors; however, these increase the cost and complexity of the system.

- **Difficulty in maintenance**

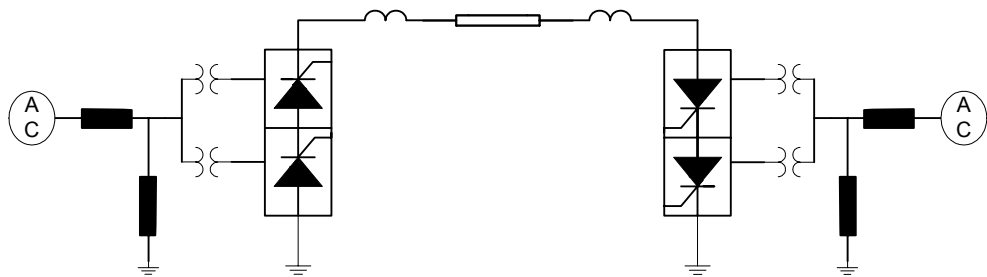
Unlike ac, there are no zero magnitude points in dc transmission, since the voltage stays constant. The zero crossings help to extinguish the arc within the breaker when contacts are separated, however in dc transmission; the voltage stays at a constant level. Faults on the dc line are handled by blocking the faulted pole, and blocking the pole is the same as shutting it off. Thus maintenance of the lines is difficult, and a transmission grid is not practically feasible [1].

## **1.6 Basic HVDC System Configurations**

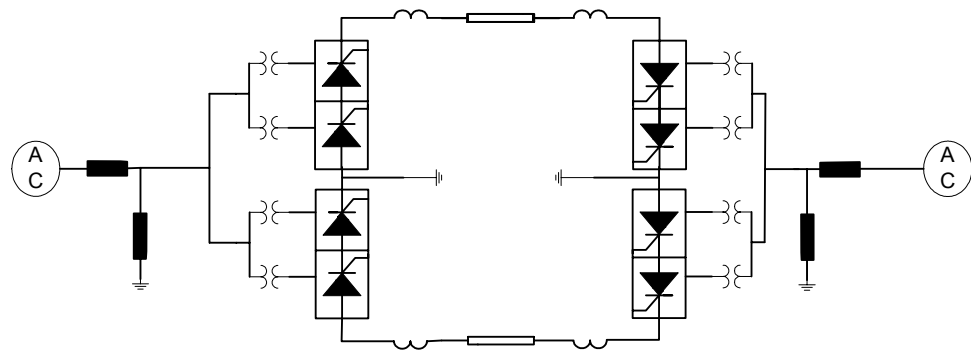
There are many different configurations of HVDC based on the cost and operational requirements. Five basic configurations are shown in Figure 1-1. The back-to-back interconnection has two converters on the same site, and there is no transmission line. This type of connection is generally designed for low ratings, and is more economical than the long distance transmission. The converters at both the ends are identical and can be operated either in rectification or inversion mode based on the control. The monopolar link has only one conductor, and the return path is through the earth. Generally the use of ground as the return path is restricted to prevent the underground metallic equipment from being damaged.



**Figure 1-1a: Back-to-back interconnection**

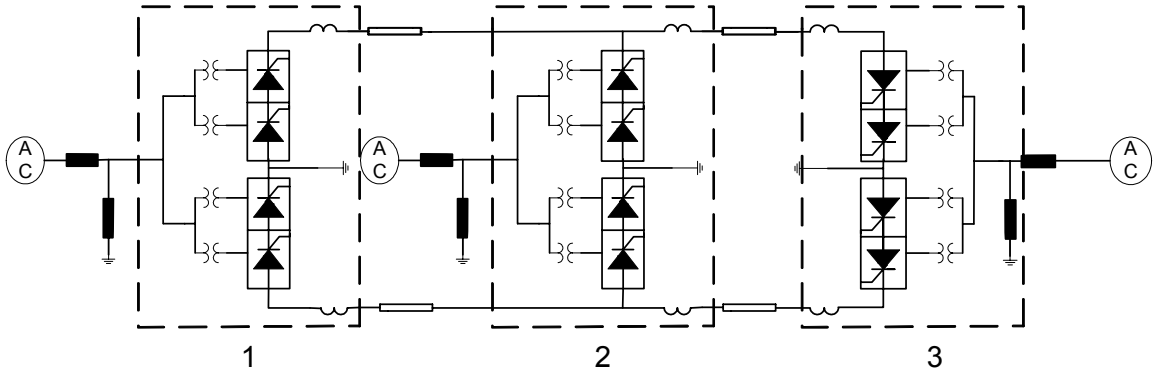


**Figure 1-1b: Monopolar link**

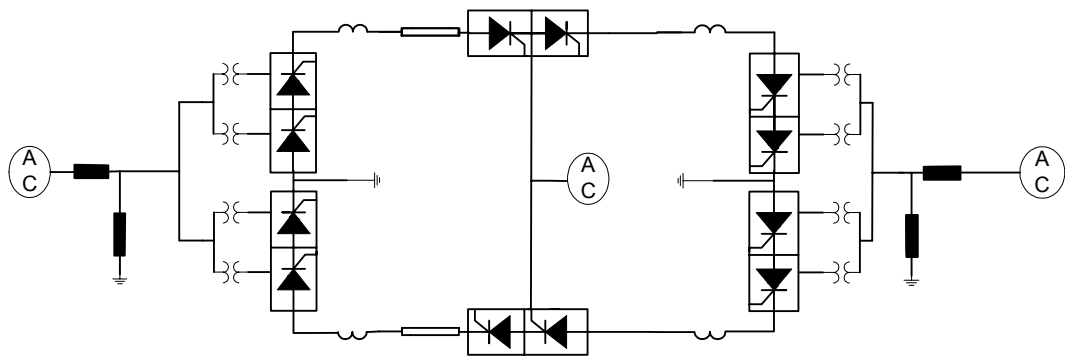


**Figure 1-1c: Bipolar link**

**Figure 1-1: Five basic configurations of HVDC transmission**



**Figure 1-1d: Parallel 3-terminal**



**Figure 1-1e: Series connection**

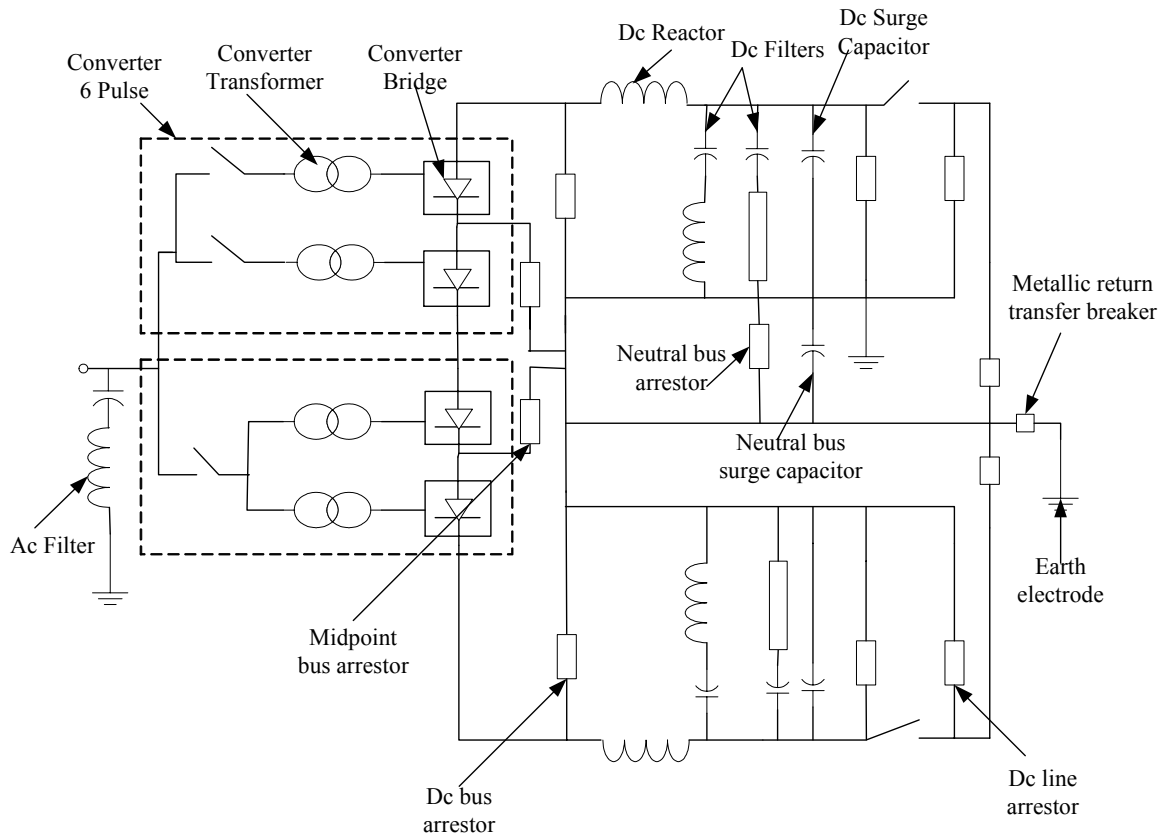
**Figure 1-1 (Continued)**

The bipolar link is the most common configuration and has two conductors or poles. One of the conductors or pole is positive with respect to the other. The current from the rectifier flows through the positive pole, and from the inverter flows through the negative pole. However, the return path is through the ground, and hence the opposite currents cancel each other, and the ground current is practically zero. In the parallel-connected three-terminal configuration, converters 1 and 2 operate as rectifiers, and converter 3 operates as an inverter. However, by changing the firing angle control and the polarity of voltage, converters 1 and 2 operate as inverters and 3 as a rectifier. The series connection, although still unused, is an attractive proposition for small taps because of comparatively high cost of the full voltage parallel tapping alternative [1].

## **1.7 Components of an HVDC Transmission System**

### **1.7.1 The converter station**

The converter stations at each end are identical and can be operated either as an inverter or rectifier based on the control. Hence, each converter is equipped to convert ac to dc and vice versa. One of the main components of a converter substation is the thyristor converter, which is usually housed in a valve hall. As seen from Figure 1-2, the substation also essentially consists of converter transformers. These transformers transform the ac system voltage based on the dc voltage required by the converter. The secondary or dc side of the converter transformers is connected to the converter bridges. The transformer is placed outside the thyristor valve hall, and the connection has to be made through the hall wall. This is accomplished in two ways: 1) with phase isolated bus



**Figure 1-2:** HVDC substation configuration ([1])

bars where the bus conductors are housed within insulated bus ducts with oil or SF<sub>6</sub> as the insulating medium, or 2) with wall bushings, and these require care to avoid external or internal breakdown [1]. Filters are required on both ac and dc sides since the converters generate harmonics. The filters are tuned based on the converter operation (6 or 12 pulse). DC reactors are included in each pole of the converter station. These reactors assist the dc filters in filtering harmonics and mainly smooth the dc side current ensuring continuous mode of operation. Surge arrestors are provided across each valve in the



converter bridge, across each converter bridge, and in the dc and ac switches to protect the equipment from overvoltages.

### **1.7.2 Converter Transformer**

The arrangement of the transformer windings depends on the converter configuration. For example, the 12-pulse converter configuration can be obtained with any of the following transformer arrangements [2]:

- Six single-phase, two winding
- Three single-phase, three winding
- Two three-phase, two winding

Star or delta connections are chosen for different configurations. The entire winding of the converter transformer is fully insulated, since the potentials across its connections are determined by the combination of valves conducting at any particular instant. As a result, the radial leakage fluxes at the end of the windings increase [2]. Because the converter transformer impedance determines the fault current across each valve, the converter transformer's leakage reactance is larger than that of the conventional one. A tap changer is most critical in HVDC as it reduces the reactive power requirement, and the tap-change range varies from scheme to scheme.

### **1.7.3 Converter**

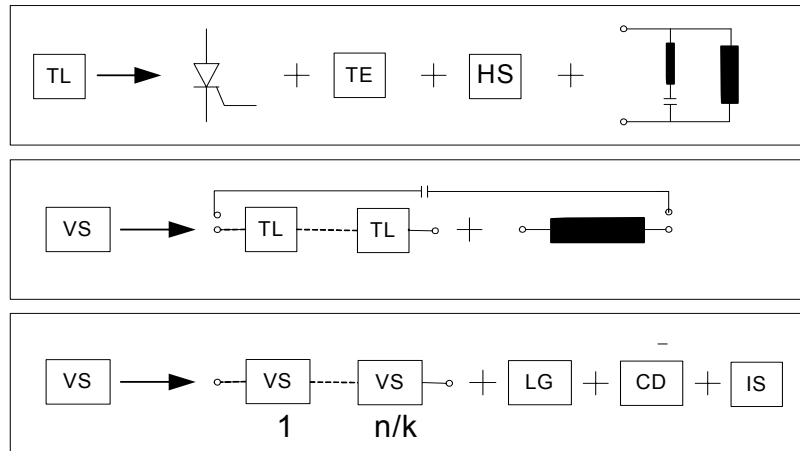
The role of power electronics in power systems has become highly significant and had power electronics not been developed, utility applications like HVDC and flexible ac

transmission systems (FACTS) would not be possible at all. The increasing demand in the quality of power systems necessitates further development of power electronics, which in turn induces more research in power electronics itself. The integration of semiconductor devices into the power system has brought improvement in the system level performance in terms of better voltage control, stability, power quality, reliability, and efficiency. Converters form the core of the substation, and the entire operation depends on the performance of the converters. Hence, the choice of the semiconductor power device used in the converter is vital, and care should be taken in designing the circuitry. For HVDC applications, the thyristor has been the choice of device ever since it was invented in the 1960's. However, devices like IGBTs and GTOs have been developed and are being studied for use in HVDC.

Thyristors replaced the mercury arc valves, and more predictable performance, reduced maintenance, and no aging were realized. However, it was not available for high blocking voltages and current ratings required for HVDC applications. The solution was a series connection of thyristors, and this series connection along with the protective and triggering circuitry is known as a thyristor level. The thyristor level forms the basic building block of a thyristor valve. A high voltage thyristor valve is a modular composition of single components in a series string as shown in Figure 1-3.

The module consists of several components and subsystems such as,

- Thyristors
- Voltage grading and damping circuits
- Cooling system
- Mechanical and insulating structure



**TL** - Thyristor Level

**TE** - Thyristor Electronic

**HS** – Heatsink

**IS** – Ins. Structure

**VS** – Valve Section

**LG** –Light guide

**CD** – Valve Coolant Distribution

**Figure 1-3:** Components of thyristor valve

- Thyristor control and monitoring system

Almost all the HVDC systems to date use line commutated thyristors made from high purity, monocrystalline silicon. For higher current ratings, the thyristors are connected in parallel, and for higher voltage ratings thyristors are connected in series.

Over the past few decades more sophisticated technologies were developed, and the device ratings were pushed to higher limits. In the last few years, silicon carbide has emerged as a promising material for improved semiconductor devices. The use of SiC is restricted by the material defects and immature technology; however, in the long term, thyristors with a blocking voltage of several tens of kV may be feasible. Apart from voltage and current rating, the control of the thyristor is important. Gate pulse generation

is important for it determines the working of the thyristor, and accuracy is a key factor as it may affect the performance of the whole system.

The various auxiliary circuits required in a high voltage thyristor valve are schematically illustrated in Figure 1-3. All thyristors require a snubber circuit connected in parallel to dampen the voltage overshoot at turn off; this circuit also serves as a means to linearize the voltage distribution along the series string. Various types of circuits have been suggested in the past; however, a simple RC connection has evolved as the industry standard.

The major challenge is to find suitable components that support the high voltage withstand capability of modern thyristors and handle the power losses. A combination of components would be an immediate solution to this, but this leads to an increase in the number of components, and the thyristor valve would become more susceptible to failure. So a resistor and a capacitor per thyristor is more safe and efficient. To protect the thyristors from the high inrush currents when the snubber circuits and external stray capacitances are discharged at turn on, a nonlinear reactor is connected in series with the thyristors.

The heat losses generated in thyristors, snubber resistors, and nonlinear reactors have a magnitude that requires forced cooling. Deionized water has evolved as the standard cooling medium because of its superior characteristics. In order to avoid electrolytic corrosion of metallic parts in the circuit, the cooling circuit is designed such that the metallic components are made independent of the leakage currents caused by high voltage stress.

The various components included in a high voltage thyristor valve need to be mechanically arranged in an insulating structure. In order to avoid damage due to seismic stresses, suspended design is widely used, especially for high rating HVDC where the structures are tall. The insulating material used is flame retardant to avoid the risk of fire due to high voltage across the thyristor valves.

#### **1.7.4 Smoothing Reactors**

The main purpose of a smoothing reactor is to reduce the rate of rise of the direct current following disturbances on either side of the converter [2]. Thus the peak current during the dc line short circuits and ac commutation failure is limited. The reactor blocks the non- harmonic frequencies from being transferred between two ac systems, and also reduces the harmonics in the dc line.

#### **1.7.5 AC Filters**

Filters are used to control the harmonics in the network. The reactive power consumed by the converters at both the ends is compensated by the filter banks. For example, in CCC (capacitor commutated converter) reactive power is compensated by the series capacitors installed between the converter transformer and the thyristor valves.

#### **1.7.6 DC Filters**

The harmonics created by the converter can cause disturbances in telecommunication systems, and specially designed dc filters are used in order to reduce the disturbances. Generally, filters are not used for submarine or underground cable

transmission, but used when HVDC has an overhead line or if it is part of an interconnecting system. The modern filters are active dc filters, and these filters use power electronics for measuring, inverting and re-injecting the harmonics, thus providing effective filtering.

### **1.7.7 Transmission Medium**

HVDC cables are generally used for submarine transmission and overheads lines are used for bulk power transmission over the land. The most common types of cables are solid and the oil-filled ones. The development of new power cable technologies has accelerated in recent years, and the latest HVDC cable available is made of extruded polyethylene [3]

## **1.8 HVDC Technology**

The fundamental process that occurs in an HVDC is the conversion of electrical current from ac to dc (rectifier) at the transmitting end and from dc to ac at the receiving end. There are different ways of achieving conversion with different converter configurations.

### **1.8.1 Selection of Converter Configuration**

A dc system can be operated with constant voltage or with constant current. However, it would be a disadvantage to use a constant current system in terms of additional components required because the supply is taken from a constant alternating system. The process of instantaneous matching of ac and dc side voltages and currents is

a basic consideration for power conversion. If an impedance free ac network is connected to a dc network, as the dc voltage is constant, time varying ac voltages will cause infinite current-level transients. The devices used for switching are capable of matching the mean values of two voltages and not instantaneous values. Hence, series impedance should be added to the network so that there would be voltage differences. Now this impedance can be connected in two different ways, and there is again a choice to be made.

As seen in the Figure 1-4, a series impedance  $Z$  is connected on the dc side. The reactance is large enough to make the current coming out of the converter direct current. This dc current flows as a result of either of the transformer phases that are connected, and the transformer transfers the currents simultaneously to the primary phases of the ac side. The currents on ac side are directly proportional to the direct currents. This arrangement is called a **current converter**.

The proportionality of the fundamental ac side current  $I_{N1}$  to direct current  $I$  is given as [4],

$$1.732 * I_{N1} / I = k \quad (1.1)$$

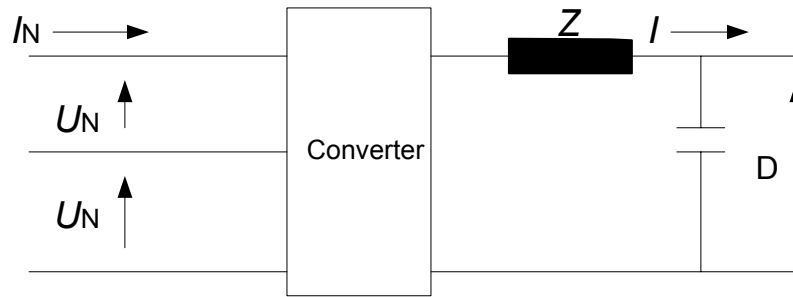
The power on dc and ac side is

$$P = DI = 1.732 * U_N * I_{N1} * \cos(\Phi) \quad (1.2)$$

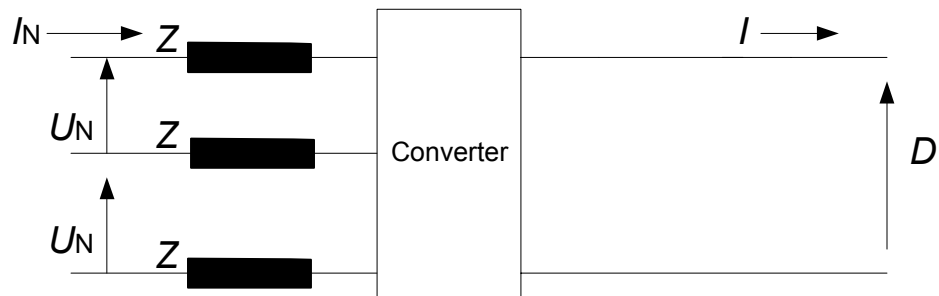
Where  $U_N$  is the rms value of the alternating line-line voltage,  $D$  is the direct voltage,  $I$  is the direct current,  $I_{N1}$  is the fundamental current,  $\Phi$  is the angle between  $I_{N1}$  and  $U_N$  and  $\cos(\Phi)$  is the power factor. From (1.1) and (1.2), it is seen that

$$D = k * U_N * \cos(\Phi)$$

So for a given transformer ratio, the current converter thus has a definite ratio  $k$  between the currents on ac and dc sides, and the voltage is dependent on the power factor.



**Figure 1-4:** Current converter



**Figure 1-5:** Voltage converter

The voltage can still be regulated using the devices, and the current ratio remains unaltered.

The converter configuration as seen in Figure 1-5, has an impedance  $Z$  connected across each phase of the ac network. These impedances along with the transformer, control the voltage through the converter and hence the voltage on dc side. This voltage is transferred across the converter onto the ac side. This type of arrangement is called a **voltage converter**.



The fundamental voltage  $U_{NI}$  is proportional to the direct voltage and differs in phase angle from the network voltage by an angle  $d$  [4]. Thus

$$U_{NI}/D = k \quad (1.3)$$

And

$$P=DI = (U_N * U_{NI}/X) * \sin (d) \quad (1.4)$$

From (1.3) and (1.4) it is seen that

$$I = k * U_N/X * \sin (d)$$

$X$  is the reactance on the ac side. For a given transformer ratio the voltage converter thus has a definite ratio  $k$  between the voltages on ac and dc sides, and the current is dependent on the network voltage and the phase angle between the fundamental components of the voltages on either side of the reactance. The switches can control the voltages, and thus the phase angle and the direct current can be determined.

Again there are three different combinations of voltage and current source converters.

- a) Voltage source converters on both ends
- b) Voltage source converter on one end and current source on other end
- c) Current source converters on both ends.

There are different configurations for the converters used in HVDC and the conversion process can be done using the following

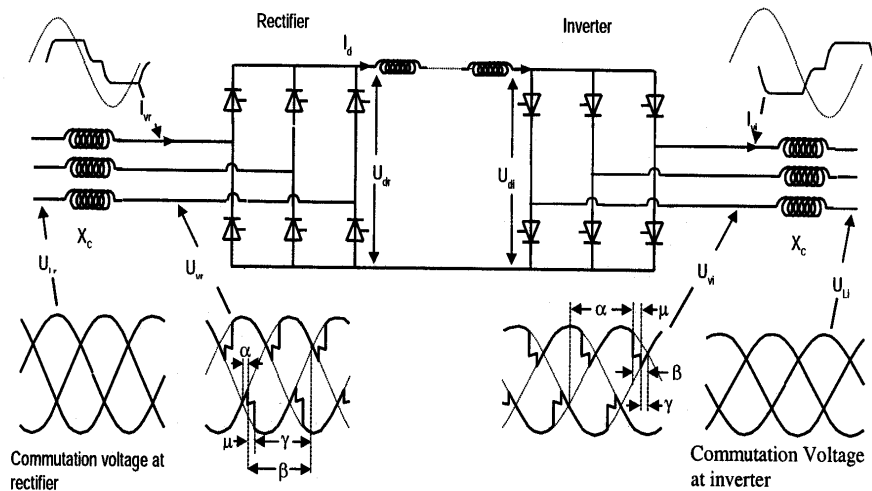
- **Natural Commutated Converters:** These are most used in the HVDC systems as of today. The component that enables this conversion process is the thyristor. The high voltage for HVDC is realized by connecting the thyristors in series, and these form a thyristor valve. The dc voltage of the bridge is varied by controlling the firing angle

of the thyristor and operated at system frequency (50 Hz or 60 Hz). The control is very rapid and efficient using natural commutated converters.

- **Capacitor Commutated Converters:** The capacitors are connected in series between the converter transformer and the thyristor valves. These capacitors prevent the converters from commutation failure, especially when connected to weak networks. The more rigid the ac network is, the less likely there will be commutation failures.
- **Forced Commutated Converters:** This type of converters is advantageous in many ways. For the control of active and reactive power, high power quality etc., the semiconductor devices used in these converters has the ability to both turn-on and turn-off. GTO and IGBT are the normally used devices. These types of converters are also known as voltage source converters (VSC). The operation of the converter is through PWM, and hence changing the PWM pattern can create any amplitude and phase. Since independent control of both active and reactive power is achieved, VSC is viewed as a motor or a generator controlling the power transfer in a transmission network.

### 1.8.2 HVDC Operation

The six-pulse converter bridge shown in the Figure 1-6 is used as the basic converter unit of HVDC transmission rectification where electric power flows from the ac side to the dc side, and inversion where the power flow is vice versa. Thyristor valves conduct current on receiving a gate pulse in the forward biased mode. The thyristor has unidirectional current conduction control, and can be turned off only if the current goes to zero in the reverse bias. This process is known as line commutation. Inadvertent turn-on of a thyristor valve may occur once its conducting current falls to zero when it is reverse



**Figure 1-6: HVDC operation ([1])**

biased, and the gate pulse is removed. Too rapid an increase in the magnitude of the forward biased voltage will cause the thyristor to inadvertently turn on and conduct [1]. The design of the thyristor valve and converter bridge must ensure such a condition is avoided for useful inverter operation.

### **Commutation**

Commutation is the process of transfer of current between any two-converter valves with both valves carrying current simultaneously during this process [1]. HVDC converters operate through line or natural commutation process both for rectification and inversion. The converter operation is defined by the voltage crossings of the ac network connected at both the ends. The ac network connected should be relatively free of

harmonics. The commutation (transfer of current) takes place when one valve starts conducting, and the current in the other valve begins to fall to zero. The valve starts conducting only when its forward biased voltage becomes more positive than the forward bias voltage of the other conducting valve, and on receiving a gate pulse.

As no system is ideal, the impedance of the system is not zero, and during commutation the current does not change instantaneously from one valve to another due to the reactance of the system. The leakage reactance of the transformer windings is also the commutation reactance as long as the ac filters are located on the primary or ac side of the converter transformer [1]. The equivalent reactance at the rectifier and inverter is known as the commutation reactance,  $X_c$ . In a practical HVDC transmission system, this commutation reactance accounts for sub transient reactance of the generator and motors, and the primary, secondary and tertiary leakage reactances of the transformers. The dc reactor and converter transformer make the dc current smooth and flat. The principle of operation for both the converters at both the ends is the same; however, the firing angle is varied for rectification and inversion. If the firing angle is greater than  $90^\circ$  the converter acts as an inverter, and if it is less than  $90^\circ$  it acts a rectifier.  $I_{vr}$  and  $I_{vi}$  are the non-sinusoidal currents at rectifier and inverter ends respectively, and both are lagging currents.

The higher order harmonics of these currents are filtered, and hence the voltages  $U_{lr}$  and  $U_{li}$  are relatively free from harmonics. Since the thyristors are unidirectional, power flow reversal is not possible by reversing the direction of current. So, power reversal is achieved by changing the polarity of the dc voltage.

## Converter Bridge Angles

The electrical angles, which describe the converter bridge operation, are shown in Figure 1-6. Both the converters have these angles, which are measured in the steady state conditions. These are defined in [1] as:

**Delay angle alpha ( $\alpha$ ):** The time expressed in electrical angular measure from the zero crossing of the idealized sinusoidal commutating voltage to the starting instant of forward current conduction. This angle is controlled by the gate firing pulse and if less than 90 degrees, the converter bridge is a rectifier and if greater than 90 degrees, it is an inverter. This angle is often referred to as the firing angle.

**Advance angle beta ( $\beta$ ):** The time expressed in electrical angular measure from the starting instant of forward current conduction to the next zero crossing of the idealized sinusoidal commutating voltage. The angle of advance  $\beta$  is related in degrees to the angle of delay ' $\alpha$ ' by:

$$\beta = 180 - \alpha$$

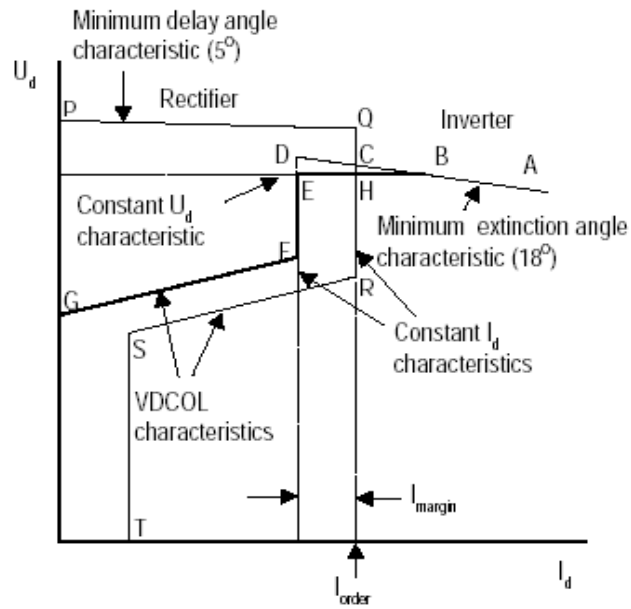
**Overlap angle ( $\mu$ ):** The duration of commutation between two converter valves expressed in electrical angular measure.

**Extinction angle gamma ( $\gamma$ ):** The time expressed in electrical angular measure from the end of current conduction to the next zero crossing of the idealized sinusoidal commutating voltage. Gamma ( $\gamma$ ) depends on the angle of advance  $\beta$  and the angle of overlap  $\mu$  and is determined by the relation

$$\gamma = \beta - \mu$$

### 1.8.3 Control and Protection

HVDC transmission systems involve (must transport) very large amounts of electric power and the desired power transfer is achieved by precisely controlled dc current and voltage across the system. Also, in dc transmission the power-flow direction is determined by the relative voltage magnitudes at the converter terminals, which can be controlled by adopting a firing-angle control scheme. Therefore, it is very important, and necessary to continuously and precisely measure system quantities which include at each converter bridge, the dc current, its dc side voltage, the delay angle  $\alpha$ , and for an inverter, its extinction angle  $\gamma$ . Each converter station is assumed to be provided with constant current and constant extinction-angle controls, for equidistant firing angle control. The choice of assigning current control, either to the rectifier or to inverter station, is made considering the investment cost for reactive- power compensation, minimization of the losses, and total running cost. Normally, the line utilization is the best with minimum reactive-power compensation if the inverter operates on minimum extinction-angle control while the rectifier operates on constant-current control. The inverter station maintains a constant extinction angle  $\gamma$  which causes the dc voltage  $U_d$  to droop with increasing dc current  $I_d$ , as shown in the minimum constant extinction angle  $\gamma$  characteristic A-B-C-D in Figure 1-7 [1]. If the inverter is operating in a minimum constant  $\gamma$  or constant  $U_d$  characteristic, then the rectifier must control the dc current  $I_d$ . This it can do as long as the delay angle  $\alpha$  is not at its minimum limit (usually  $5^\circ$ ). The steady state constant current characteristic of the rectifier is shown in Figure 1-7 as the vertical section Q-C-H-R. Where the rectifier and inverter characteristic intersect, either



**Figure 1-7:** Steady state  $U_d$ - $I_d$  characteristics for a two terminal HVDC system ([1])

at points C or H, is the operating point of the HVDC system. The operating point is reached by action of the on-line tap changers of the converter transformers. The inverter must establish the dc voltage  $U_d$ , by adjusting its on-line tap changer, to achieve the desired operating level if it is in constant minimum  $\gamma$  control. If in constant  $U_d$  control, the on-line tap changer must adjust its tap to allow the controlled level of  $U_d$  be achieved with an extinction angle equal to or slightly larger than its minimum setting of  $18^\circ$  in this case. The on-line tap changers on the converter transformers of the rectifier are controlled to adjust their tap settings so as to minimize the reactive-power consumption subject to a minimum  $\gamma$  limit for maintaining the constant current setting  $I_{order}$  (see Figure 1-7).

At the inverter end, constant extinction angle minimizes the reactive power, and hence, the tap changer will provide the dc voltage control. During some disturbances, like

ac-system faults, the ac voltage at the rectifier or inverter is depressed, and a sag in ac voltage at either end will result in a lowered dc voltage too. If the disturbance is large, the converter may not be capable of recovering by itself, and it becomes important to reduce the stress on the converter valves. This is achieved by the controller, which reduces the maximum current order, and is known as a voltage dependent current order limit (**VDCOL**). The VDCOL control will keep the dc current  $I_d$  to the lowered limit during recovery, and only when dc voltage  $U_d$  has recovered sufficiently, will the dc current return to its original  $I_{order}$  level. There are a number of special purpose controllers, which can be added to HVDC controls to take advantage of the fast response of a dc link and help the performance of the ac system. These include ac system damping controls, ac system frequency control, step change power adjustment, sub synchronous oscillation damping, and ac under voltage compensation.

### **1.9 Areas for Development in HVDC Converters**

The thyristor is the key component of a converter bridge, and improvements in thyristor ratings and characteristics highly influence the costs of the valves, and other equipment in a converter substation. GTO, a device with turn off capability in the thyristor family, is making a significant impact in power-electronic design. The turn-off capability feature has evolved new circuit concepts such as self-commutated, pulse-width modulated (PWM), voltage-driven and multi-step converters, and enables the circuits to operate at higher switching frequencies. These, in turn, reduce harmonic content and allow operation at leading power factors.



GTOs are attractive for dc power conversion into ac systems, which have little or no voltage support and hence are gaining wider attention in their application to HVDC transmission. The voltage source converter configuration VSC is being applied in the latest developments, and it requires GTOs. Its special properties include the ability to independently control real and reactive power supplied to the ac system, and it does not require an active ac voltage source to commutate unlike the conventional line commutated converter. There is considerable flexibility in the configuration of the VSC converter bridges, and a suitable control system can enhance the system performance.

Before GTOs can be implemented in dc transmission, the series and parallel stacking of the devices and their losses are of major concern in implementing the GTOs for HVDC transmission. At present, however, the GTO ratings are much lower, and their cost and losses are higher compared to a thyristor. With the advent of SiC devices, the three factors mentioned above can be greatly improved, for they have superior material qualities than the Si devices. It is expected that continued research and developments in power electronics would provide exciting new configurations and applications for HVDC converters.

## **2. Silicon Carbide Technology**

Before analyzing the devices and the systems that utilize silicon carbide material, it is important to know about silicon carbide material structure, properties and the device benefits because of these properties. In this chapter, a brief introduction about SiC material will be presented followed by its structural properties and characteristics. Also, a brief description of SiC devices and their applications will be given.

Power electronic applications in the field of power distribution and transmission systems are gaining wide attention because of their anticipated large-scale application in the near future. At the consumer end, much of the electrical power undergoes some form of electronic conversion, and it is estimated to be 15% of the electric power produced. For the past few decades power electronics devices have enabled HVDC transmission, which is mostly line-commutated electronics. However, it is in the 1990s that the improvisation took place, when self-commutated power electronics at the transmission level was implemented. It is predicted that with further developments in semiconductors and their packaging technology, power electronic applications will be extended into distribution applications as device efficiency and reliability increases and also as the cost per megawatt falls. The above discussion illustrates that; in the past cost-effective implementation of control at the user level has been the driving force behind research in power electronics. Even though the transmission and distribution industry has its problems to solve, there are no cost-effective solutions. The role of power electronics is very limited in generation industry since it involves high powers in the range of 250 MW.

Worldwide utility market restructuring and environmental and efficiency regulations have impacted the electricity market, which led to further innovation in power electronics for electrical power systems. Utility market restructuring and new regulations are aimed at improving the existing generation capacity, increase in efficiency, better use of existing plants, and providing environmentally acceptable ways of power transmission. This has initiated huge research interests and has benefited the power semiconductor applications and technology industry.

Silicon-based power semiconductor devices, ranging from diodes, thyristors, gate turn-off thyristors, metal-oxide-semiconductor field-effect transistors and more recently insulated bipolar gate bipolar transistors and metal-oxide-semiconductor turn-off thyristors are the most widely used in the power electronic circuits and systems.

The need for improved performance of the electronic systems in many applications has brought about much advancement in Si technology. Despite these advances, Si devices are limited to operation at low junction temperatures and low blocking voltages, by virtue of the physical properties of silicon. Hence, in megawatt power applications, which require efficient, lightweight, high-density power converters operating at high temperatures, the use of silicon devices is restricted. The various limitations in the use of Si devices has led to the development of wide band-gap semiconductors such as SiC, GaN, and diamond, which have better performance characteristics than Si devices.

Silicon carbide has some exceptional physical properties that make it a potential material to overcome the limitations of silicon. The wide band gap makes the device operate at high electric fields, and the reduction in intrinsic carrier concentration with

increase in band gap enables the device to operate at high temperatures. Wide band-gap semiconductors, such as silicon carbide (SiC) and gallium nitride (GaN), provide larger band-gaps, higher breakdown electric field and higher thermal conductivity than silicon devices. Amongst the available wide band gap materials, SiC is by far the most advanced material and, hence, is of great interest at present for many power electronics, device, and system engineers.

Silicon carbide has the following advantages over silicon:

- Low resistance – silicon carbide has reduced drift region widths due to high band gap and hence less on state resistance. Hence, silicon carbide devices have lower conduction losses compared to silicon.
- High switching frequency – the high velocity saturation and thinner drift region associated with the high band gap make the device switch faster.
- Smaller heat sinks – thermal conductivity of silicon carbide is three times greater than silicon and hence better heat dissipation. This results in reduced thermal management system.
- Radiation tolerance and minimal shielding – the electrical characteristics of a silicon carbide device do not vary with temperature.
- Higher breakdown voltages – due to the high electric breakdown field (five times that of silicon), silicon carbide can block higher voltages.
- Higher junction operating temperature ranges – the device temperature increase is slower.

- Silicon carbide bipolar devices have excellent reverse recovery characteristics. With the less recovery current switching losses, EMI is reduced, and hence there is less need for snubbers.
- Smaller die sizes – reduced size and weight of the system results in high system efficiency.

However, silicon carbide devices have several defects that degrade their performance, and also most of the results are theoretical. Fabrication is one of the issues, and hence wafers as big as one inch were available only a decade before. So, the study of silicon carbide material was limited to small area devices and hence could not be extended to devices with higher ratings. The major manufacturing defects identified in silicon carbide devices is micropipes and screw dislocations. These defects have an adverse effect on the performance of the devices and hence result in detrimental usage of the device. These defects restrict the development of large area devices, as the performance of the devices deteriorate with increase in the device size. SiC technology is an emerging technology and requires significant improvements to the material, device characterization, and modeling. Silicon carbide technology is considered immature and still in the primitive stages of development. With continued research in the material processing and fabrication technology, silicon carbide would revolutionize the power electronics industry.

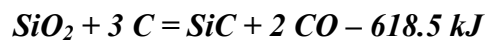
## **2.1 Silicon Carbide**

Before analyzing the devices and the systems that utilize silicon carbide material, it is important to know about silicon carbide material structure, properties and the device benefits because of these properties.

What is silicon carbide?

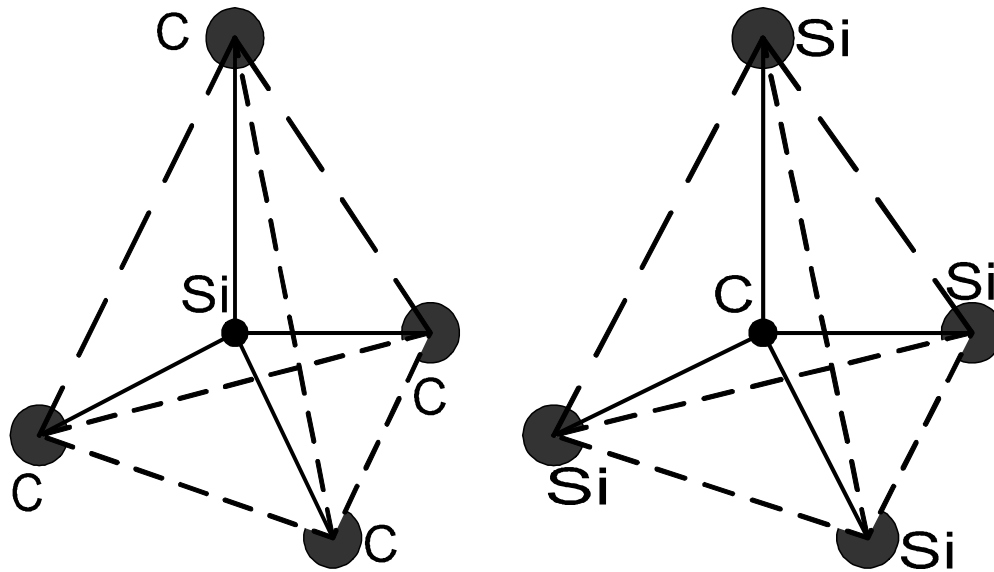
**Silicon carbide** is a wide band gap semiconductor with high thermal conductivity, high breakdown electric field strength, high-saturated drift velocity, and high thermal stability. Silicon carbide is extremely durable and useful for many high power, high frequency, and high temperature applications.

SiC was discovered by E.G. Acheson and was first produced by the Acheson process in the 1890s. SiC is produced in electrical resistance furnaces with a mixture of a carbon material, normally petroleum coke, and silica sand. The mixture is reacted chemically at high temperatures in the range of 1700°C-2500°C to form silicon carbide. The chemical reaction is given as [6]:



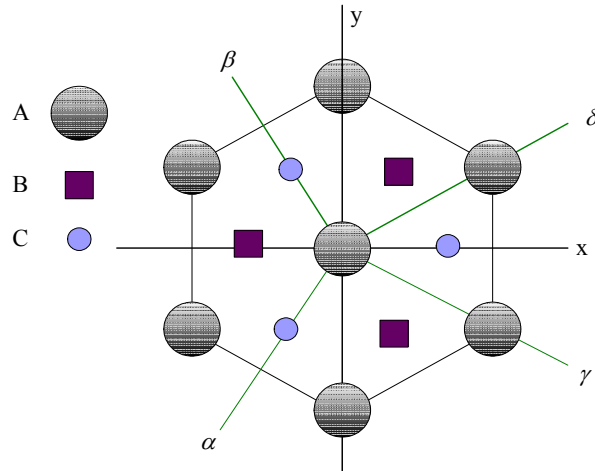
## 2.2 Silicon Carbide Lattice Structure

SiC molecules are made by arrangement of covalently bonded tetrahedral Si and C atoms with either a carbon atom bonded to four Si atoms or a Si atom bonded to four carbon atoms as shown in Figure 2-1. Silicon carbide occurs in more than 170 polytypes, and each has a different physical property. Polytype refers to a family of material, which has common stoichiometric composition but not common crystal structure. A silicon carbide molecule has a layer of silicon atoms bonded with a layer of carbon atoms forming a double layer of Si-C also called a Si-C bilayer. The plane formed by the bilayer is called the basal plane, and the c-axis direction perpendicular to this plane is known as the stacking direction.



**Figure 2-1:** Tetrahedral silicon carbide structure

As shown in the Figure 2-2, if the stacking sequence of the Si-C bilayer in the three different planes A, B, C are designated as Aa, Bb, and Cc then there are several different possible sequences [7]. The most common polytypes are 3C-SiC, 6H-SiC, and 4H-SiC. 15R-SiC and 2H-SiC have also been identified, but are not widely used. All other polytypes are combinations of these basic sequences. 3C-SiC, also referred to as  $\beta$ -SiC, is the only form of SiC with a cubic crystal structure. The non-cubic polytypes of SiC are sometimes referred to as  $\alpha$ -SiC. 4H-SiC and 6H-SiC are only two of many possible SiC polytypes with a hexagonal crystal structure [8]. Similarly, 15R-SiC is the most common of many possible SiC polytypes with a rhombohedral crystal structure.



AB - hcp  
 ABC - fcc  
 AaBbAaBb - Wurzite  
 AaBbCcAa - Zinblende  
 Other ordered sequences - Polytypes

**Figure 2-2:** Planar stacking sequence ([7])

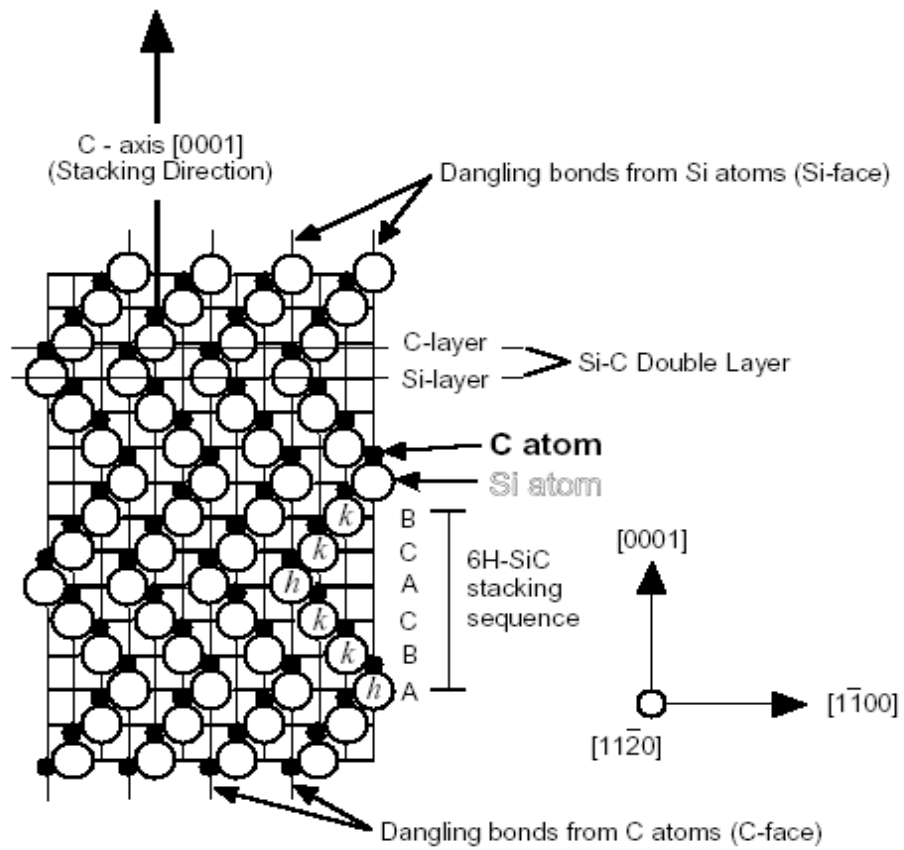
Figure 2-3 shows the stacking sequences of the polytypes of major interest to current research and development. Each polytype has different electrical properties due to the difference in their physical properties. **4H-SiC**: Hexagonal close packed, ABCBACB; **3C-SiC**: Cubic structure, Zinc-blend, ABCABC; **6H-SiC**: Hexagonal close packed, ABCACB [7].

## 2.3 Properties of Silicon Carbide

### 1). Wide Bandgap

Silicon carbide is classified as a wide band gap material because it has a large band gap ( $E_g = E_c - E_v$ ).  $E_c$  – conduction band energy,  $E_v$  – valence band energy,  $E_g$  – band gap. Each polytype has a different bandgap ranging from 2.39 eV for 3C-SiC to 3.33 eV for 2H-SiC [11]; whereas Si has a much less bandgap of 1.12 eV. Silicon carbide





**Figure 2-3a:** 6H – silicon carbide ([8])

**Figure 2-3:** Stacking sequences of the polytypes

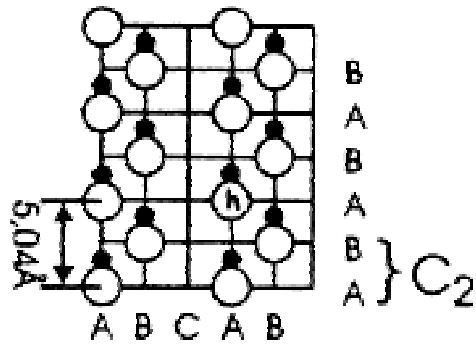


Figure 2-3b: 2H- silicon carbide

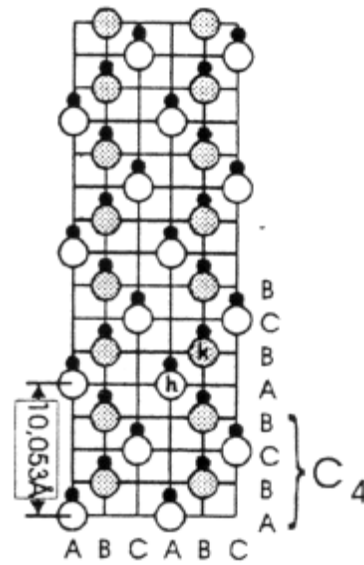


Figure 2-3c: 4H- silicon carbide

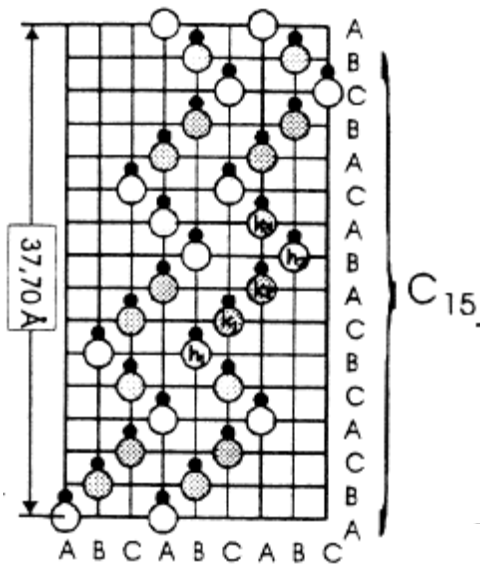


Figure 2-3d: 15R- silicon carbide

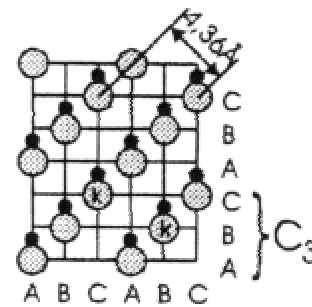
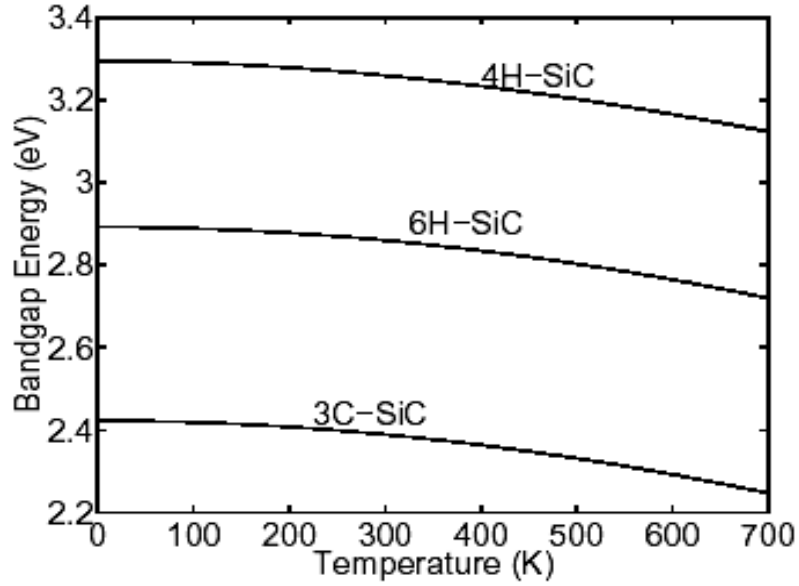


Figure 2-3e: 3C- silicon carbide

Figure 2-3b, Figure 2-3c, Figure 2-3d, Figure 2-3e ([14])

Figure 2-3: Continued



**Figure 2-4:** Bandgap variation with temperature ([10])

has an indirect band gap like silicon; also the temperature dependence of band gap energy is similar to silicon with the bandgap energy decreasing with increase in temperature.

(2.1) gives the empirical relation of this temperature dependence [10].

$$E_g(T) = E_g(T_o) + \alpha \left( \frac{T_o^2}{T_o + \beta} - \frac{T^2}{T + \beta} \right) \quad (2.1)$$

T is the temperature in Kelvin and  $E_g(T_o)$  is the band gap energy at a temperature  $T_o(K)$ .  $\alpha$  and  $\beta$  are empirical constants. Figure 2-4 shows the variation in band gap with the temperature for different SiC polytypes. Silicon carbide has higher maximum operating temperature compared to silicon, due to the low intrinsic carrier concentration and wider band gap. For a doping density of  $1e14$ , silicon has an intrinsic temperature of

200°C while silicon carbide has 900°C. Thus silicon carbide, with large bandgap, is radiation hard and hence can withstand higher temperatures making it suitable for operating in extreme conditions.

## 2). High Electric Breakdown Field

Silicon carbide has higher breakdown field than silicon because of the wide band-gap. The electron hole pair generation due to ionization impact is difficult because of the wide band gap, and hence silicon carbide can withstand higher electric fields compared to silicon. 4H-SiC has approximately seven times higher critical electric field than silicon. The high electric breakdown field allows the device to have less thick layers compared to silicon and hence less drift region resistance reducing the on-state losses.

## 3). Carrier Mobility

Carrier mobility depends on various factors like temperature, doping concentration, applied electric field, and the lattice structure. At low electric fields lattice scattering is the dominant factor, and the low field mobility is given by the empirical relation known as Caughey-Thomas low field mobility model [12].

$$\mu_o = \mu_{\min} + \frac{\mu_{\max} - \mu_{\min}}{1 + \left( \frac{N_D + N_A}{N_{ref}} \right)^\alpha} \quad (2.2)$$

Where  $(N_A + N_D)$  is the total doping concentration,  $\mu_{\max}$  and  $\mu_{\min}$  are the minimum and maximum mobilities of electrons and holes,  $N_{ref}$  is the doping concentration for p-

type and n-type material calculated empirically and  $\alpha$  is the curve fitting parameter, a measure of how quickly the mobility changes from  $\mu_{\min}$  to  $\mu_{\max}$ .

The temperature dependence of the mobility model can be calculated as,

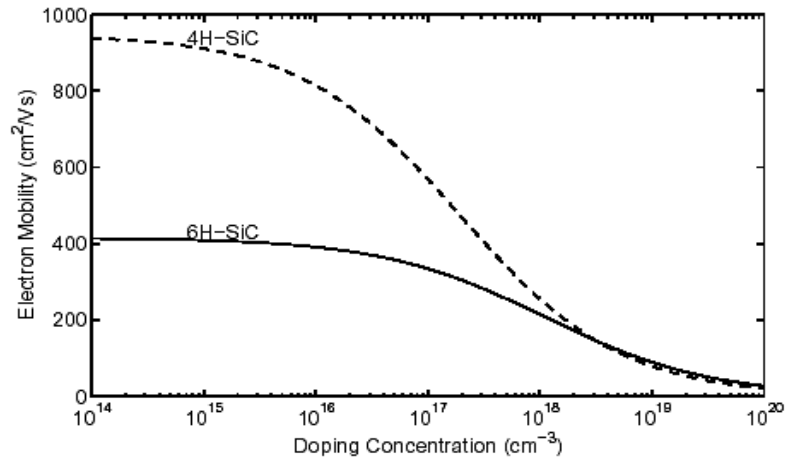
$$\mu = \mu_0 * \left( \frac{T}{T_0} \right)^\gamma \quad (2.3)$$

Where  $\mu_0$  is the value at room temperature  $T_0$ .  $\gamma$  is a constant and varies from -1.8 to -2.5 for n-type and p-type SiC materials [12]. Using the parameters in the mobility model equation, the mobilities for electrons and holes, in 4H-SiC and 6H-SiC, have been calculated and plotted as shown in Figure 2-5 and Figure 2-6 [5].

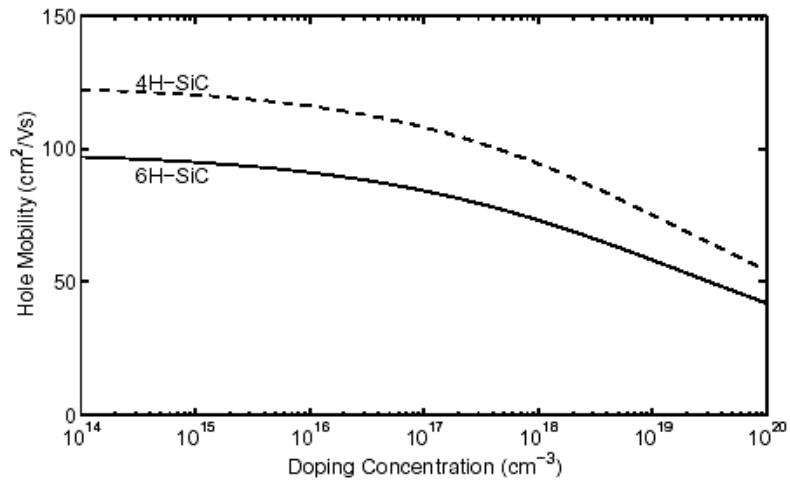
At high electric fields the electron velocity saturates due to increased scattering, and the mobility becomes proportional to the field. As a result of velocity saturation, the mobility becomes low at very high fields, and a field dependent model can be given as,

$$\mu^E(E) = \mu \left( \frac{1}{1 + \left| \frac{\mu E}{v_s} \right|^\beta} \right)^{\frac{1}{\beta}} \quad (2.4)$$

$E$  is the applied electric field,  $v_s$  is the saturation velocity, and  $\beta$  is a constant, which determines how abruptly the velocity goes to saturation [12]. The mobility along the c-axis is higher in 4H-SiC compared to the 6H-SiC and hence the former is preferred for many applications.



**Figure 2-5:** Electron mobility vs. doping concentration ([10])



**Figure 2-6:** Hole mobility vs. doping concentration ([10])

#### 4). Saturated Drift Velocity

The saturation velocity also depends on the temperature and can be expressed as [12],

$$v(T) = \frac{v_{\max, 600 K}}{1 + 0.6 \exp\left(\frac{T}{600 K}\right)} \quad (2.5)$$

The saturation velocity for SiC is  $2e7$  cm/s compared to  $1e7$  cm/s for silicon. This high saturation velocity enables the silicon carbide devices to switch faster than silicon devices, because the drift velocity determines the frequency of operation.

#### 5). High Thermal Stability

Silicon carbide can be operated at high temperatures because of the wide band gap. Also silicon carbide has high thermal conductivity, more than three times greater than silicon. Therefore, the junction-to-case thermal resistance  $R_{th-jc}$  of SiC polytype is at least three times less than silicon. This feature enables easy transfer of heat generated in the device to the ambient through the case and heat sink.

$$R_{th-jc} = \frac{d}{\lambda \cdot A} \quad (2.6)$$

$\lambda$  – thermal conductivity,  $d$ - is the length, and  $A$  is the cross-sectional area.

List of electrical and physical properties of some semiconductors are shown in Table 2.1.

**Table 2.1. List of Electrical and Physical Properties of Some Semiconductors**

Property	Si	GaAs	6H-SiC	4H-SiC	GaN	Diamond
<b>Bandgap, <math>E_g</math> (eV)</b>	1.12	1.43	3.03	3.26	3.45	5.45
<b>Dielectric constant, <math>\epsilon_r</math></b>	11.9	13.1	9.66	10.1	9	5.5
<b>Electric Breakdown Field, <math>E_c</math> (kV/cm)</b>	300	400	2500	2200	2000	10000
<b>Electron Mobility, <math>\mu_n</math> (<math>\text{cm}^2/\text{V}\cdot\text{s}</math>)</b>	1500	8500	500	1000	1250	2200
<b>Hole Mobility, <math>\mu_p</math> (<math>\text{cm}^2/\text{V}\cdot\text{s}</math>)</b>	600	400	101	115	850	850
<b>Thermal Conductivity, <math>\lambda</math> (W/cm·K)</b>	1.5	0.46	4.9	4.9	1.3	22
<b>Saturated Electron Drift Velocity, <math>v_{\text{sat}}</math> (<math>1\text{e}7</math> cm/s)</b>	1	1	2	2	2.2	2.7

## 2.4 Silicon Carbide Power Devices

The electrical properties and their advantages, compared to silicon, discussed in the previous section have been utilized by the device manufacturers and have transformed those material benefits to device benefits at the system level. One of the basic building blocks of a power circuit is the half-bridge circuit in which two modules are connected in series and each module is composed of a three terminal switch and a two-terminal diode connected in anti-parallel. There are basically two families of two- and three- terminal power semiconductor-switching devices – the Schottky rectifier and the power FET representing the unipolar family and the BJT and thyristor belonging to the bipolar family. The three terminal devices can further be classified based on the control signal used (either voltage or current). Traditional power devices like BJT, SCR, and GTO use



current for control and modern devices like MOSFET, IGBT and MCT use voltage control for reduced control circuit complexities.

There are several different bipolar, unipolar, controlled, uncontrolled and metal-oxide-semiconductor (MOS) - gated devices that are widely used by the power electronics and power system designers. IGBTs offer low switching losses, high switching frequency operation and a simplified gate circuit. GTOs and thyristors, on the other hand, are still used for high power applications, such as power system conditioning equipment and large direct-current (dc) rectifiers. Low switching losses of power MOSFETs make them perfect for high frequency applications. However, their high on-state resistance makes it a less attractive device for high voltage application. The need for faster devices with high voltage and high switching frequency capability is growing, especially for advanced power conversion.

Silicon-based power devices have long dominated the power electronics and power system applications. The primary limitation of the silicon is the small energy band-gap, which leads to low intrinsic breakdown voltage. In order to overcome this limitation, the active layers were made thick to have greater voltage drop across the device and stacking packaged devices in series was adopted. However, series stacking is expensive from a packaging standpoint and requires complicated control. Hence, there is a strong incentive to develop high voltage blocking capability semiconductor devices particularly from wide bandgap semiconductors like SiC. Due to the wide band gap, silicon carbide can block high voltages with increased doping and thinner drift regions. Silicon devices are limited to 5000 V [13], and silicon carbide devices can block voltages up to 19.2kV

[14]. Silicon carbide devices are highly reliable because, the static and dynamic characteristics do not vary much with the variation in temperature.

Of the many device benefits, the most striking one is the ability to meet the system conditions with one device instead of several silicon devices. Of the many possible system benefits, the reduction in size or complexity of the circuit is a substantial one. For example, there is a potential reduction in the size and cost of thermal management hardware can be realized by operating the active devices at high junction temperatures. SiC has the inherent ability to operate at higher temperatures compared to other material devices and exhibit the same electrical characteristics as at room temperature. Silicon carbide has higher thermal conductivity and also low intrinsic carrier concentration, which enables them to operate at high junction temperatures. The maximum junction temperature that silicon operates is 150°C whereas; silicon carbide can operate at 650°C [15]. However, packaging and high temperature contacts are a problem for the SiC devices. The two important facts about higher operating temperatures are: (i) the higher temperature will result in smaller heat-sink area for the same packaging technology, (ii) higher operating temperature allows a complete change in the thermal management approach for a given packaging area.

Because of higher electron saturation velocity and reduced drift region widths, SiC has low switching losses compared to Si and hence is suitable for high frequency operation. Increase in the device speed results in many system benefits, one of which is a reduction in volume and weight associated with passive components, which can be simply achieved by increasing the frequency. For example,  $X=1/wC$ ,  $X$  is the capacitive reactance,  $w$  is the frequency in rad/s,  $C$  is the capacitance, and hence the capacitance

required varies inversely with frequency. But increasing frequency should not cause substantial increase in system losses, EMI generation etc. The power is dissipated during turn-on and turn-off times, the latter being longer. In SiC devices the turn-off time is less than Si devices because of the fact that SiC devices can block faster. Hence, reduced  $t_{off}$  leads to increase frequency of operation.

### **Power System Applications:**

Power devices such as thyristors, GTOs, and diodes have been widely used in many power system applications such as static volt ampere reactive compensators, static transfer switches, dynamic restorers/regulators, electronic tap changers, high-voltage DC transmission systems, and flexible AC transmission lines [16]. The Si thyristor ratings are limited to 6-10 kV and currents up to 5000 A [16], whereas the system requirements are as high as 500 kV and 5000 A [16]. Series and parallel stacking is an immediate solution to this; however this results in an increase in the volume and weight of the system. SiC devices with high voltage and current ratings reduce the number of devices, and also the high temperature operation characteristic reduces the size of cooling system. Prototype high-voltage SiC thyristors and GTOs are rated up to 3 kV BV, 10 A [16], and although these devices are still small compared to Si counterparts, SiC GTOs will likely remain faster at higher ratings because of the intrinsic properties of SiC. With steady progress in material growth, it can be easily predicted that SiC GTOs will be commercially revolutionize the power electronics industry in less than a decade.

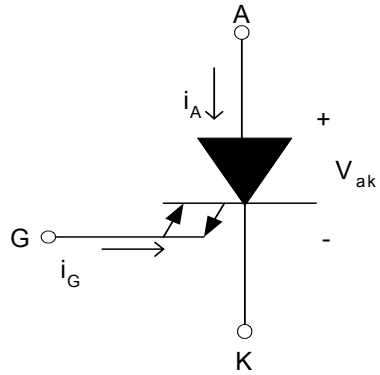
The structural and electrical properties of silicon carbide were presented in this chapter. A comparison of silicon and silicon carbide, and the advantages of silicon

carbide devices were also discussed. These properties will be used to develop the loss models in the next chapter.

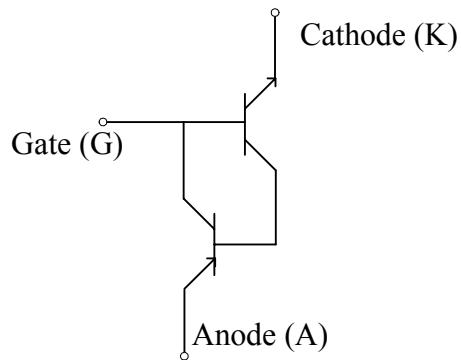
### 3. Silicon Carbide Gate Turn-off Thyristor

In this chapter the GTO thyristor structure and its operation will be discussed briefly, and the various structural properties and physical characteristics of SiC material discussed in the previous chapter will be used to develop a GTO thyristor loss model. The individual Si and SiC device simulations will be presented, and discussed.

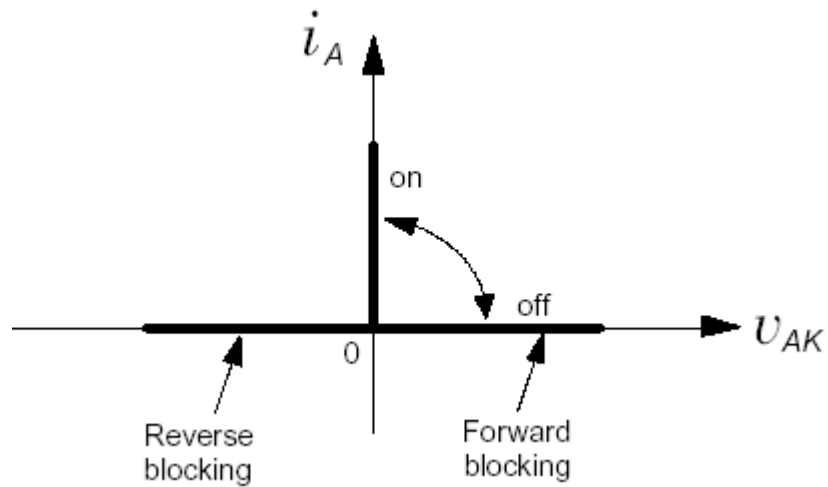
Gate turn-off thyristor (GTO) is a power semiconductor device with three junctions and three terminals, has a four-layered structure, and belongs to the thyristor family. The gate turn-off thyristor has the ability to turn-on and turn-off through the gate terminal control. The turn-on process is similar to the conventional thyristor; however, the GTO is designed to turn-off by applying a complementary gate signal. The three terminals in a GTO are anode (A), cathode (K), and gate (G) as shown in Figure 3-1. The GTO can be viewed as a bipolar junction transistor pair connected as shown in Figure 3-2. The working of a GTO can be explained with this npn and pnp transistor equivalent, which will be discussed later in this chapter. The ideal characteristic curve of a gate turn-off thyristor is shown in Figure 3-3. The graph has three sections: the reverse blocking characteristic, the off state or the forward blocking characteristic, and the on-state characteristic. The reverse blocking characteristic resembles a power diode, and it can block voltages up to a few kV with only minor leakage. As long as there is no gate signal applied, the GTO blocks voltage for positive voltages across anode and cathode, and it is still in the off state or the forward blocking state. If a GTO with forward bias voltage is triggered, by means of a current signal at the gate terminal, the region of operation shifts from forward blocking to the on-state characteristic.



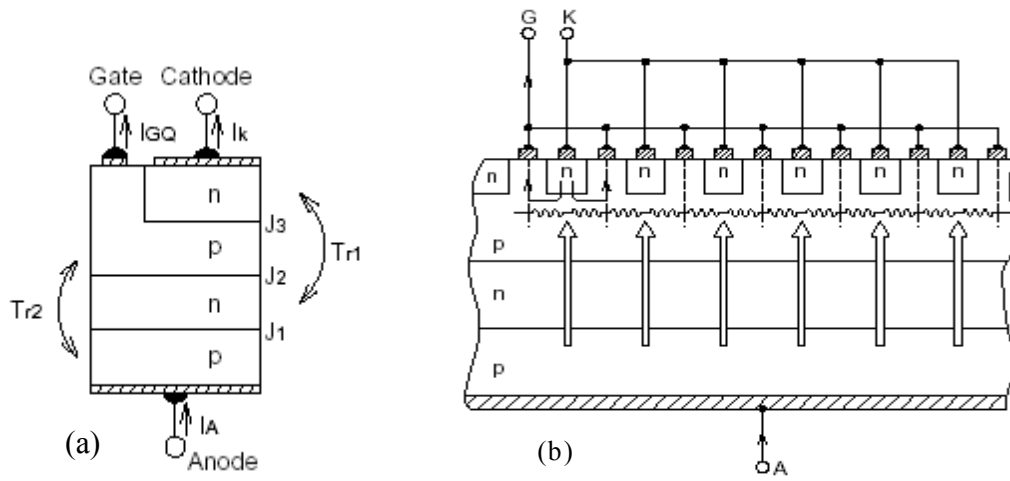
**Figure 3-1:** GTO symbol



**Figure 3-2:** Two-transistor model of GTO



**Figure 3-3:** Ideal characteristics of a gate turn-off thyristor

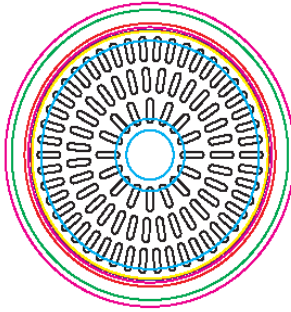


**Figure 3-4 (a), (b):** Four layer structure of GTO ([18])

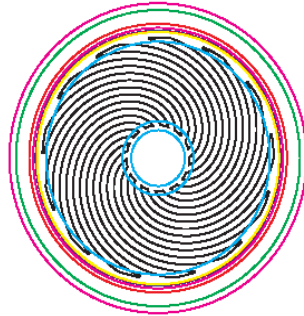
### 3.1 GTO Structure

The basic structure of a GTO is similar in construction to the conventional thyristor; however, it has several design features that allow turn-on and turn-off operations through gate signal control. The GTO also has a four layer p-n-p-n structure as shown in Figure 3-4, and there are a few significant differences between a GTO thyristor and a conventional thyristor. The gate and cathode are highly interdigitated to reduce the resistance of the gate-cathode region. There are various types of geometric forms used for gate-cathode layout. The most common design has the cathode region split into fingers, and arranged in concentric rings around the device as shown in Figure 3-5. Different structures used are shown in Figure 3-5 and Figure 3-6.

Based on the anode layer formation, the GTO thyristor can further be classified as:



**Figure 3-5:** Concentric layout structure ([10])



**Figure 3-6:** Involute layout structure ([10])

Asymmetrical structure – this is the most common structure and has unidirectional blocking capability. This type of device has a diode integrated in the structure and hence cannot block reverse voltages. Turn-off operation of asymmetric GTO is easier compared to the symmetric device, and it can also block high voltages as it is less susceptible to the open base transistor breakdown. The devices with this structure are generally used in dc switching applications.



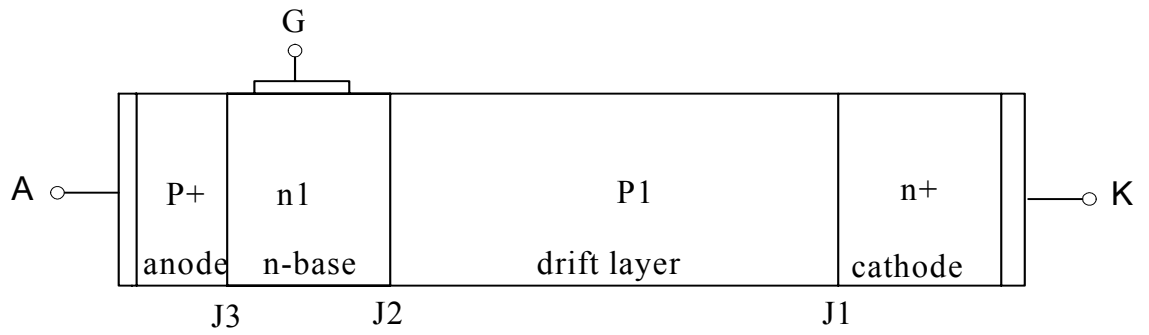
Symmetrical structure – the devices with this structure can block forward and reverse voltages, similar to the conventional thyristor. These devices with bi-directional blocking capability are used in ac circuits.

There are a few structural differences between silicon and silicon carbide GTO thyristors. The material limitation of silicon carbide has forced a different structure, unlike the silicon device, known as the complementary structure. The p-type SiC substrate has very high resistivity, because of the partial ionization of the p-type acceptor impurities. Hence, it is difficult to obtain a highly conductive p-type substrate. This structure has n-p-n-p configuration, complementary to the p-n-p-n configuration of the silicon device as shown in Figure 3-7.

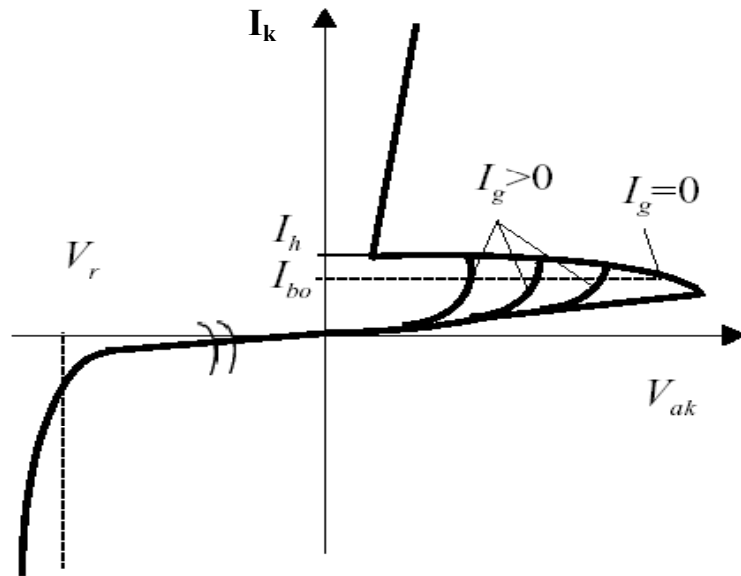
## **3.2 Static Characteristics of GTO**

### **3.2.1. On-State Characteristics and Turn-on Process**

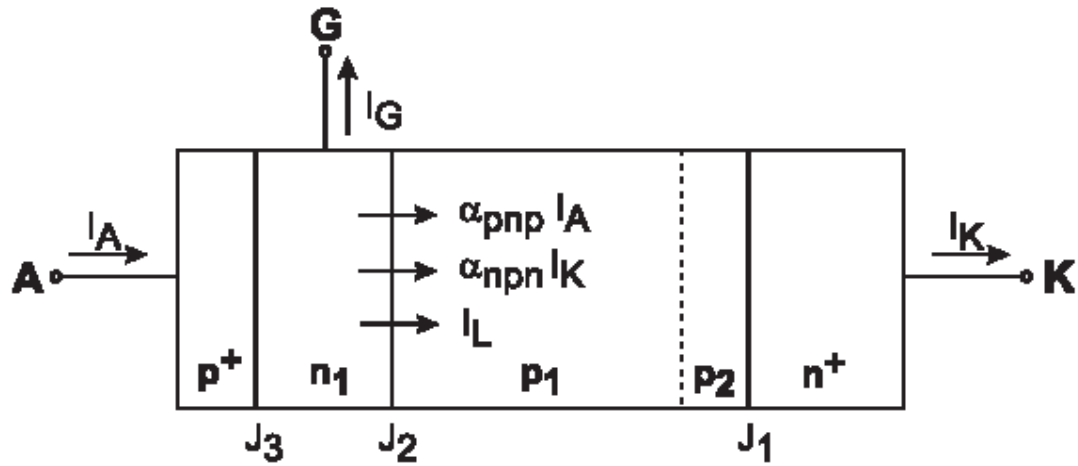
The V-I characteristics of a GTO are shown in Figure 3-8. The characteristic curve shows the anode current  $I_K$  as a function of the anode to cathode voltage  $V_{ak}$  for different values of gate current,  $I_g$ . The on-state characteristic of the GTO is similar to that of the conventional thyristor. The gate signal is applied until the current reaches a specific value, known as the holding current, after which the GTO will remain in the conduction state. The holding current value of a GTO is more than the standard thyristor, due to reduced gain of the lower transistor to achieve the turn-off capability. The negative slope in the forward characteristic is due to reduced breakover voltage,  $V_{bo}$ , at higher values of gate current.



**Figure 3-7:** Complementary asymmetric SiC GTO thyristor structure



**Figure 3-8:** V-I characteristics of GTO thyristor ([24])



**Figure 3-9:** Complementary asymmetric GTO thyristor ([10])

This characteristic is due to the interdigitated gate-anode structure of the GTO, used to make gate controlled turn-on, turn-off operations, and voltage blocking. This can be explained better with the two-transistor model of a GTO, with the characteristics of the bipolar junction transistors influence on the GTO.

In the forward blocking mode of operation, the junctions  $J_1$  and  $J_3$  are forward biased, and  $J_2$  is reverse biased. As shown in Figure 3-9, the various currents at the junction  $J_2$  include cathode current, anode current, and leakage current, which are a sum of the space charge, generated current, and the diffusion current. So the cathode current can be represented as [10]:

$$I_K = \alpha_{pnp} I_A + \alpha_{npn} I_k + I_L \quad (3.1)$$

where  $\alpha_{pnp}$  and  $\alpha_{npn}$  are the common-base current gains of the pnp and npn transistors, respectively. The anode current can be represented as,  $I_A = I_G + I_K$  and hence the cathode current can be written as,

$$I_k = \frac{(\alpha_{pnp} I_G + I_L)}{1 - \alpha_{pnp} - \alpha_{npn}} \quad (3.2)$$

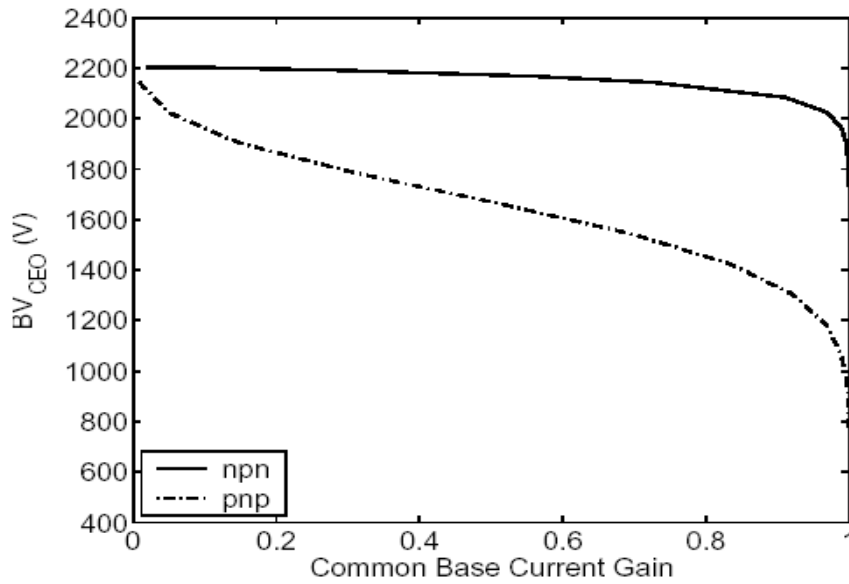
The above expression gives the relation between the cathode current and gate current as a function of the common base gains of the npn and pnp transistors. Hence, for the gate controlled turn-on and turn-off operations, these transistor gains are significant. The GTO can start conducting even without applying the gate signal when a large forward anode-cathode voltage is applied across the device. The GTO loses its blocking capability at a particular voltage known as the forward breakover voltage.

If the gate current is zero, cathode current  $I_K$  can be expressed as

$$I_k = \frac{I_L}{1 - (\alpha_{pnp} + \alpha_{npn})} \quad (3.3)$$

As the anode-cathode voltage increases, the current gains of the transistors increase due to increase in the leakage and diffusion current and also because of the avalanche multiplication process. The GTO continues to block until the sum of gains

$$\alpha_{npn} + \alpha_{pnp} = 1 \quad (3.4)$$



**Figure 3-10:** Open base breakdown characteristics vs. current gains npn and pnp transistors ([10])

When the sum equals unity, the GTO switches to the conduction state, and this defines the point of breakover voltage. The above expression can also be expressed as a function of avalanche multiplication co-efficient  $M$ , base transport  $\alpha_T$ , and the emitter injection efficiency  $\gamma$  as [10],

$$(M\gamma\alpha_T)_{pnp} + (M\gamma\alpha_T)_{npn} = 1 \quad (3.5)$$

Hence by controlling the emitter injection efficiency and the base transport factor and by varying the base thickness, the gains of the transistors can be adjusted. The open base breakdown voltage can be calculated for both the npn and pnp transistors as a function of the common base current gains. Figure 3-10 shows the variation in open base breakdown voltage as a function of the gains for a 12  $\mu\text{m}$  drift region [10].

As shown in Figure 3-10, the npn silicon carbide transistor has a better open-base breakdown voltage range, compared to the pnp transistor, due to the low avalanche multiplication co-efficient value [10]. Hence GTOs made with open-base npn transistors can block higher voltages than the pnp transistors. Hence, for the GTOs with complementary structure, some structural modifications have to be made for higher blocking voltages. For silicon devices, the open-base breakdown of a pnp transistor would be higher than npn because of the low ionization co-efficient of the holes [20]. Also, the silicon GTO structure has a different structure compared to the silicon carbide GTO. The gate triggering current  $I_g$  is the minimum gate current required by the GTO to switch to the conducting state. The gate current causes an increase in the anode current and hence the common base gains of the transistors. As stated earlier, if the sum of the gains becomes unity, the GTO starts conducting and latches on due to the regenerative action of the two transistors. Holding current  $I_h$ , is the minimum anode current required to hold on to the conduction state. If the anode current drops below the threshold value, the sum of the gains drops below unity and the GTO turns off.

### 3.2.2 GTO Turn-off Process

The GTO thyristor can be turned off by applying a reverse gate current. The maximum cathode current that can be turned off is given as [10]

$$I_{KM} = \beta_{off} I_{GM} \quad (3.6)$$

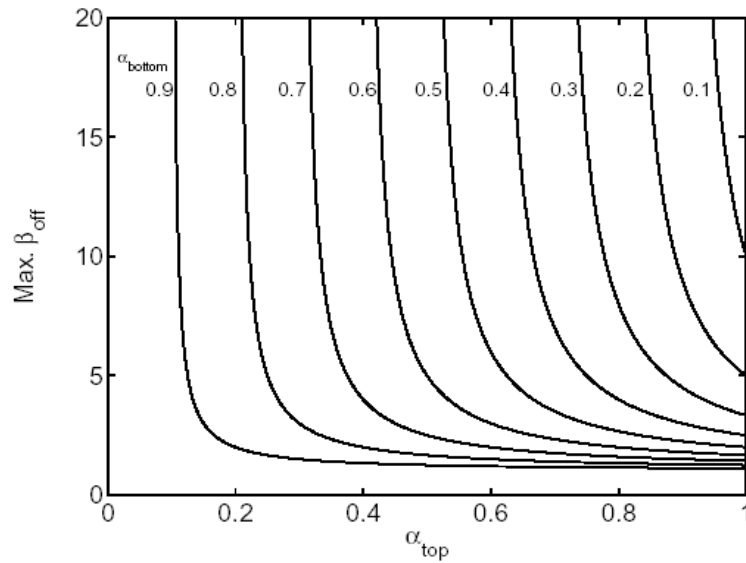
The maximum controllable cathode current determines the maximum cathode current at which the device can be operated and also limits the gate-controlled turn-off of the device. Using the equations for base and collector currents from the transistor equivalent circuit, the expression for the maximum turn-off gain, which is a ratio of the gate current to the cathode current, can be derived in terms of common base current gains as,

$$\beta_{off} = \frac{\alpha_{top}}{\alpha_{top} + \alpha_{bottom} - 1} \quad (3.7)$$

The gains of the transistors determine the turn-off gain of the GTO, and hence it is important to design the GTO such that gate current is dominant in determining the turn off of the device. To achieve an effective gate control device turn-off, the gain of the bottom transistor, npn, should be low so that the range of control over the gain of the top transistor is more. Figure 3-11 shows the variation in the turn-off gain with the common base transistor gains. The gains are generally adjusted by making structural modifications in the device layout.

### 3.3 GTO Switching

The switching characteristics of a GTO thyristor are influenced by design of the device and the material properties. The lifetime and mobility of holes and electrons, in the p-base and n-base regions of the transistors, have a significant effect on the switching characteristics of the device. Doping and the layout design also influence the switching characteristics. The switching processes can be divided into different segments in turn-on



**Figure 3-11:** Maximum turn-off gain vs. transistor gains for top and bottom transistors ([10])

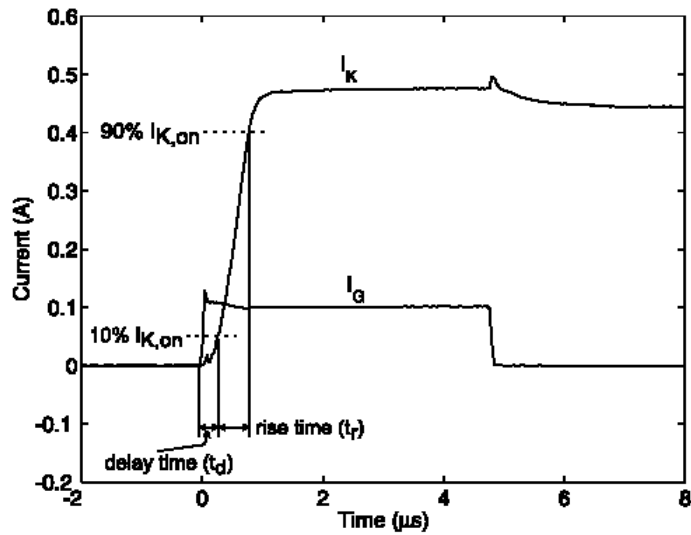
and turn-off characteristics irrespective of the design and material used.

### 3.3.1 Turn-on Process

The turn-on characteristics can be divided into three phases as shown in Figure 3-12.

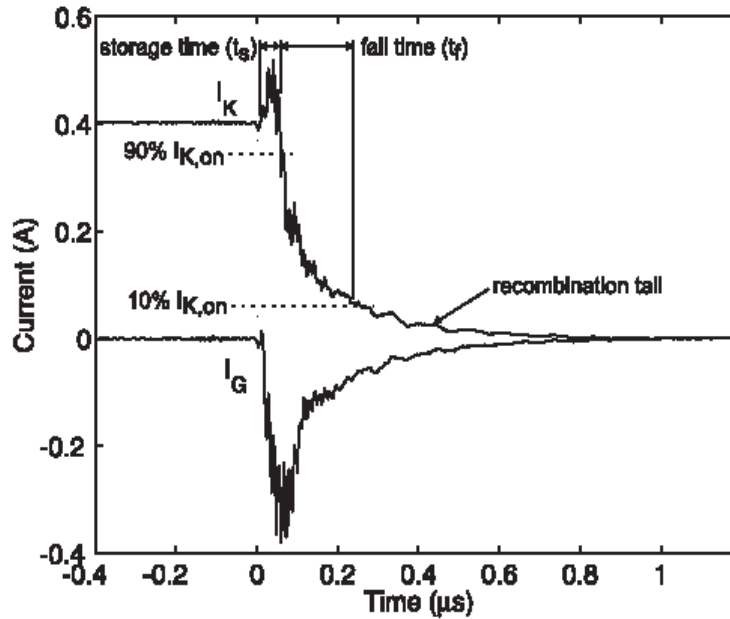
- Delay time phase – delay time is the time taken for the cathode current to reach 10% of the on-state current after the gate signal is applied.
- Rise time phase – rise time is the time taken for the cathode to increase from 10% to 90% of the on-state current.
- Conduction phase





**Figure 3-12:** Turn-on characteristics of 4H-SiC GTO switching process ([10])

The delay time is the measure of time required for charge build up in n-base and p-base. The gate current and the common base current gains of the npn and pnp transistors influence the charging of the base regions. The sum of the transistor gains,  $\alpha_{npn} + \alpha_{pnp}$ , is less than unity during the charge build up and thus cause a delay in the rate of rise of cathode current. Once the sum exceeds unity, the rise-time begins and the cathode current rises rapidly due to the regenerative action of the transistors. The conduction-spreading phase or the current spreading phase starts after the rise-time phase, and there can be a significant delay before the device starts conducting uniformly. However, for GTO thyristor the delay is very less or insignificant because of the highly interdigitated anode structure.



**Figure 3-13:** Turn-off characteristics of 4H-SiC GTO switching process ([10])

### 3.3.2 Turn-off process

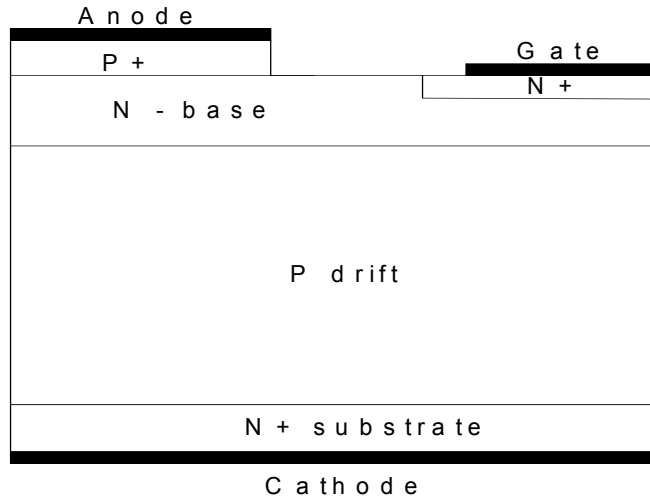
The turn-off process can also be divided into three phases as shown in Figure 3-13:

- Storage time phase – is the measure of time delay between the application of the reverse gate current and a decrease in the cathode current indicating the device turn-off.
- Fall-time phase – is the time required for the expansion of depletion layer in the drift region and the corresponding build up of anode-cathode voltage.
- Recombination tail phase – corresponds to the time taken for elimination of excess charge carriers during the final recombination tail phase.

During the storage phase, the junction  $J_2$  is forward biased. Storage time corresponds to the removal of excess charge carriers in the n- base of the upper transistor by applying the reverse gate current and lateral hole diffusion current [10]. The stored charge in the n-base region is extracted until the junction  $J_2$  becomes reverse biased. So by the end of storage phase, the junction  $J_2$  will be completely reverse biased across its entire region. During the fall time phase, the anode current decreases and the cathode voltage increases to the supply voltage. During this time, the depletion layer across the junction expands into the drift region, and the excess minority charge carriers are swept out. In the recombination tail phase, the remaining charge in the p-base region is removed by recombination. This produces a tail current in the cathode current waveform, as shown in Figure 3-13.

### **3.4 Device Model**

To study the impact of a device at the system level and to realize the benefits of using the device, a good device model is required. Based on the V-I characteristics and switching characteristics described in the previous sections of this chapter, a model of a GTO thyristor has been developed for the purpose of loss analysis during conduction and switching. There is some degree of approximation in the model, and it is primarily modeled as loss model. The model is based on the equations derived for power loss in the conduction state and the energy loss during switching on and switching off periods of the GTO thyristor. The developed model has been studied for both silicon and silicon carbide materials and for different ratings of voltages and currents. A description of the device



**Figure 3-14:** Device structure of SiC GTO thyristor used in simulations

model is presented, followed by simulations to evaluate the switching and conduction losses.

### 3.4.1 Device Structure

The equations for conduction losses and switching losses are derived in [19], based on a specific device structure, as shown in Figure 3-14. The structure is similar to what has been described in section 3.2 except for few modifications and has the following features:

- The material used is 4H-SiC polytype.
- The structure has five layers including the 4H-SiC n+ substrate. The second layer is the lightly doped p-type drift layer, followed by lightly doped n-type layer, a heavily doped n-type layer, and finally the heavily doped p-type layer,

which carries the metal anode contact. The device has interdigitated anode structure for effective gate control. The N+ doped layer, which forms the base of the upper pnp transistor, has a metal gate contact.

- Asymmetrical structure – the device can block in only one direction because of the cathode short.
- Complementary pnpn configuration – is complementary to the silicon npnp configuration as explained in the earlier section.
- Heavily doped N+ substrate – due to low resistivity of the p-type SiC
- The lower base thickness is 1.5 times the maximum depletion region width – to accommodate the open base transistor voltage ( $BV_{ceo}$ ) blocking characteristic of the GTO thyristor. The increase in layer thickness is because of the lower blocking capability of the upper pnp transistor as described in section 3.2.1.

### 3.4.2 Conduction Losses

The on-state power loss is mainly due to conduction losses, and the on-state power loss for a GTO thyristor is similar to that of the power diode given as [17],

$$V \cdot I = V_j \cdot I + R_{on} \cdot I^2 \quad (3.8)$$

where  $V_j$  is the voltage across the junction,  $V_d$  is the voltage drop across the drift region,  $I$  is the on-state current,  $R_{on}$  is on-state resistance, and  $V$  is the on-state voltage drop. The on-state power loss equation is derived in [19] as,

$$P_{on-state} = J \cdot (E_g / q) + J \cdot (3\pi / 8) \cdot (kT / q) \cdot \exp(3V_B / 2L_a E_c) \quad (3.9)$$

In (3.9) the first term in the sum corresponds to the loss due to the voltage drop across the junction and the second term corresponds to the voltage drop due to on-state specific resistance in the lower base region. This equation can further be simplified and reduced to an expression that is dependent on few parameters. The list of expressions used is [17], [19],

$$V_B = \varepsilon(N_a + N_d) \cdot E_c^2 / (2q \cdot N_a \cdot N_d)$$

$$\tau_a = \tau_n + \tau_p ; L_a = (D_a \cdot \tau_a)^{0.5}$$

$$D_a = 2 \cdot D_n \cdot D_p / (D_n + D_p)$$

$$D_n = (kT / q) \cdot \mu_n$$

$$D_p = (kT / q) \cdot \mu_p$$

Then the final expression for conduction losses can be given as,

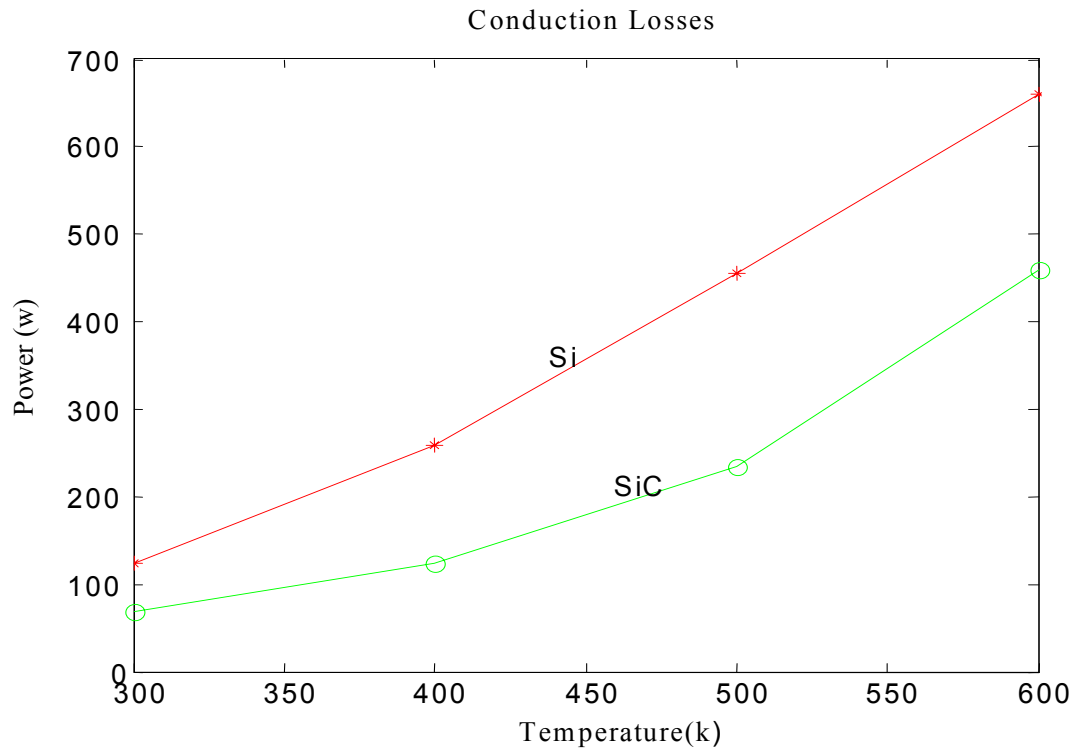
$$P_{on-state} = J \cdot (E_g / q) + J \cdot (3\pi / 8) \cdot (kT / q) \cdot \exp(D)$$

$$D = (\varepsilon(N_a + N_d) \cdot E_{bd} \cdot 1.5) / (2 \cdot q \cdot N_a \cdot N_d \cdot \sqrt{(kT / q) (\mu_n \cdot \mu_p)} \cdot \tau_a / (\mu_n + \mu_p)) \quad (3.10)$$

This equation is dependent on doping densities, mobilities, temperature, and applied voltage and current. For a given operating voltage and current, the model behavior varies with temperature, with the doping density fixed for a desired rating of the device. Figure 3-15 shows the variation in conduction losses as the temperature increases. It should be noted that the silicon GTO thyristor losses are more than the silicon carbide conduction losses, because of the difference in the on-state specific resistance.

The expression for specific on-state resistance is given as [22],

$$R_{sp} = \frac{4BV^2}{\varepsilon_s \mu_n E_c^3} \quad (3.11)$$



**Figure 3-15:** Conduction losses of Si and SiC GTO thyristor

Since the electric field for SiC is higher than silicon, which is the dominant factor in the expression, it can be seen that the specific resistance for a silicon device is higher than for a silicon carbide device. Also, for a given operating current, conduction losses vary with the second term in the (3.9), which is a function of the specific resistance. Hence, the conduction losses are an order higher for the silicon GTO thyristor. Conduction losses for an applied voltage of  $V = 5000 \text{ V}$  and a current density of  $J = 100 \text{ A/cm}^2$  is shown in Figure 3-14. The list of terms used is given in Table 3.1.

**Table 3.1 List of terms used in the equations**

<p><math>k</math>, Boltzmann constant (J/K)</p> <p><math>v_s</math>, electron saturation velocity (cm/s)</p> <p><math>V_B</math>, breakdown voltage (V)</p> <p><math>D_a</math>, ambipolar diffusion coefficient (cm<sup>2</sup>/s)</p> <p><math>D_n, D_p</math>, electron and hole diffusion coefficients (cm<sup>2</sup>/s)</p> <p><math>N</math>, electron concentration (cm<sup>-3</sup>)</p> <p><math>q</math>, electron charge (C)</p> <p><math>E</math>, electric field (V/cm)</p> <p><math>E_c</math>, avalanche breakdown electric field(V/ cm)</p> <p><math>E_{on}, E_{off}</math> turn-on and turn-off losses (J/cm<sup>2</sup>)</p> <p><math>J</math>, current density (A/cm<sup>2</sup>)</p> <p><math>L_a, L_n</math>, ambipolar and electron diffusion lengths (cm)</p> <p><math>P_{on-state}</math>, on-state losses (w.cm<sup>-2</sup>)</p> <p><math>V</math>, applied voltage (V)</p>	<p><math>\alpha_{npn}</math>, average current gain during voltage rise</p> <p><math>R_{sp}</math>, ideal specific on-state resistance (ohm.cm<sup>2</sup>)</p> <p><math>N_A, N_D</math>, acceptor and donor concentrations (cm<sup>-3</sup>)</p> <p><math>\alpha_{npn,max}</math> maximum common-base current gain for a given applied voltage</p> <p><math>\alpha_{npn}</math>, average common-base current gain during applied voltage varies from 0 to <math>V</math></p> <p><math>\epsilon_s</math>, permittivity of the semiconductor (F/cm)</p> <p><math>\mu_n, \mu_p</math> electron and hole mobility (cm<sup>2</sup>/V·s)</p> <p><math>\tau_a</math>, ambipolar carrier lifetime(s)</p> <p><math>\tau_n, \tau_p</math> electron and hole lifetimes(s)</p>
--	--



### 3.4.3 Switching Losses

The equations for energy losses, during turn-on and turn-off operations, are derived in [19]. During turn-on, it is assumed that the turn-on gain is very high,

$$E_{off} = 1/2 \cdot (\epsilon_s \cdot E_c V / (1 - \alpha_{npn})) \sqrt{V/V_B} + J \alpha_{npn, \max} \cdot \tau_a \quad (3.12)$$

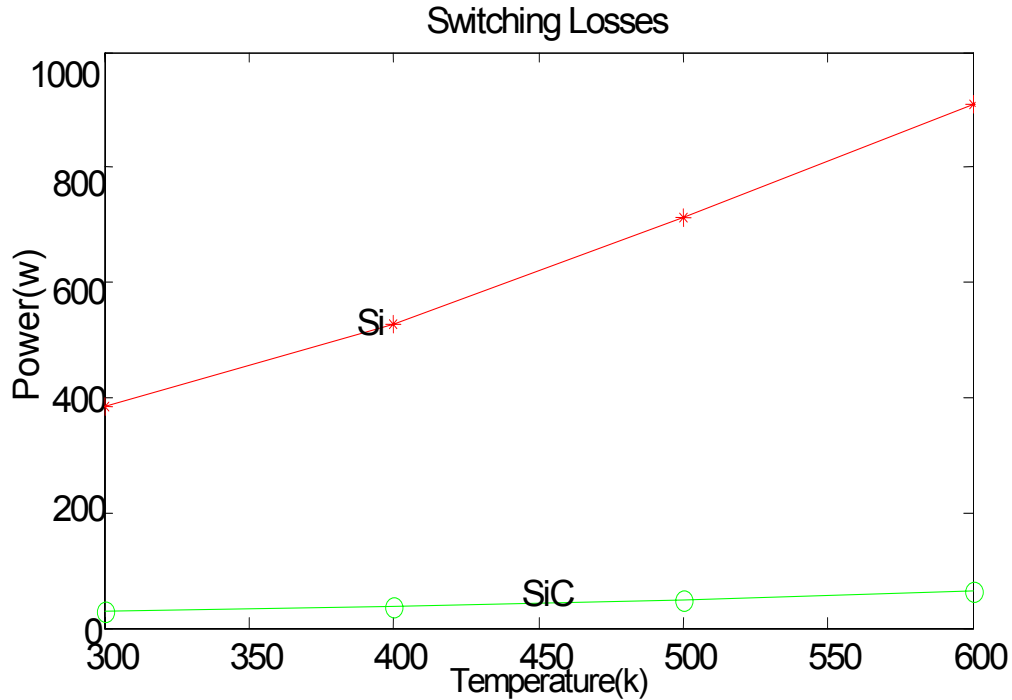
$$E_{on} = 1/3 \cdot \epsilon_s \cdot E_c V \sqrt{V/V_B} + J^2 \cdot (3\tau_a \cdot V_B^2) / (\epsilon_s \cdot \mu_n \cdot E_c^3) + (E_g / 2q) \cdot J \tau_a \quad (3.13)$$

hence it can be assumed that the current rise is very fast. During the turn-off period, assuming unity gain turn-off, the energy loss equation is derived as an open base NPN transistor turn-off and also assuming that entire anode current flows to the gate terminal.

The switching power losses can be calculated using the total energy loss equation as,

$$P_{switching} = (E_{on} + E_{off}) \cdot f_s$$

Figure 3-16 shows the comparison of silicon and silicon carbide devices as the temperature increases for  $V = 5000 \text{ V}$ ,  $J = 200 \text{ A/cm}^2$ , and a switching frequency of 1 kHz. There is a noticeable difference between the switching losses of silicon and silicon carbide devices. For the same blocking voltage, thickness of the blocking layer in a silicon device is more than the thickness of blocking layer in a silicon carbide device. The reduction in the blocking layer thickness in silicon carbide devices is because of the high electric breakdown strength of silicon carbide material due to wide bandgap.

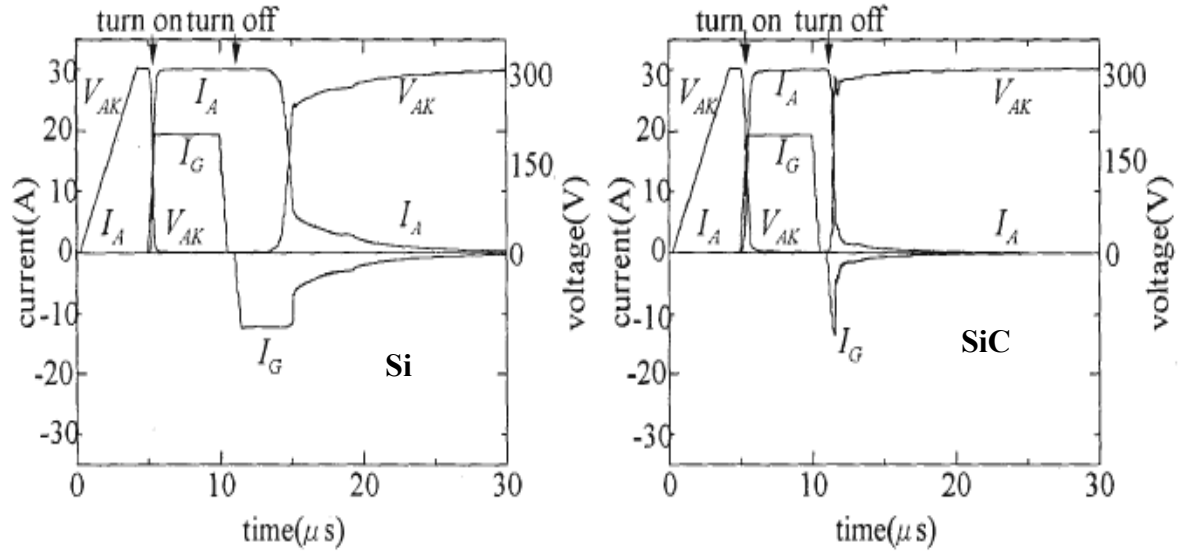


**Figure 3-16:** Switching losses of Si and SiC GTO thyristor

Thus, the charge stored in the drift region is less, which results in faster switching. Also, the ambipolar diffusion length  $L_a$ , which is a function of ambipolar lifetime, and the electron and hole mobilities for silicon is greater than silicon carbide due to high carrier mobilities and greater lifetimes. These result in higher switching losses. The additional tail current due to the recombination of residual minority carriers in the base region causes additional power loss during switching. Since there is no additional tail current in a silicon carbide device, the losses are less. Figure 3-17 shows a comparison in the switching of the physical silicon and silicon carbide GTO thyristor devices.

The total power loss in the device is given as,

$$\text{Total losses} = \text{Conduction losses} + \text{Switching losses}$$



**Figure 3-17:** Comparison waveforms for Si and SiC switching ([21])

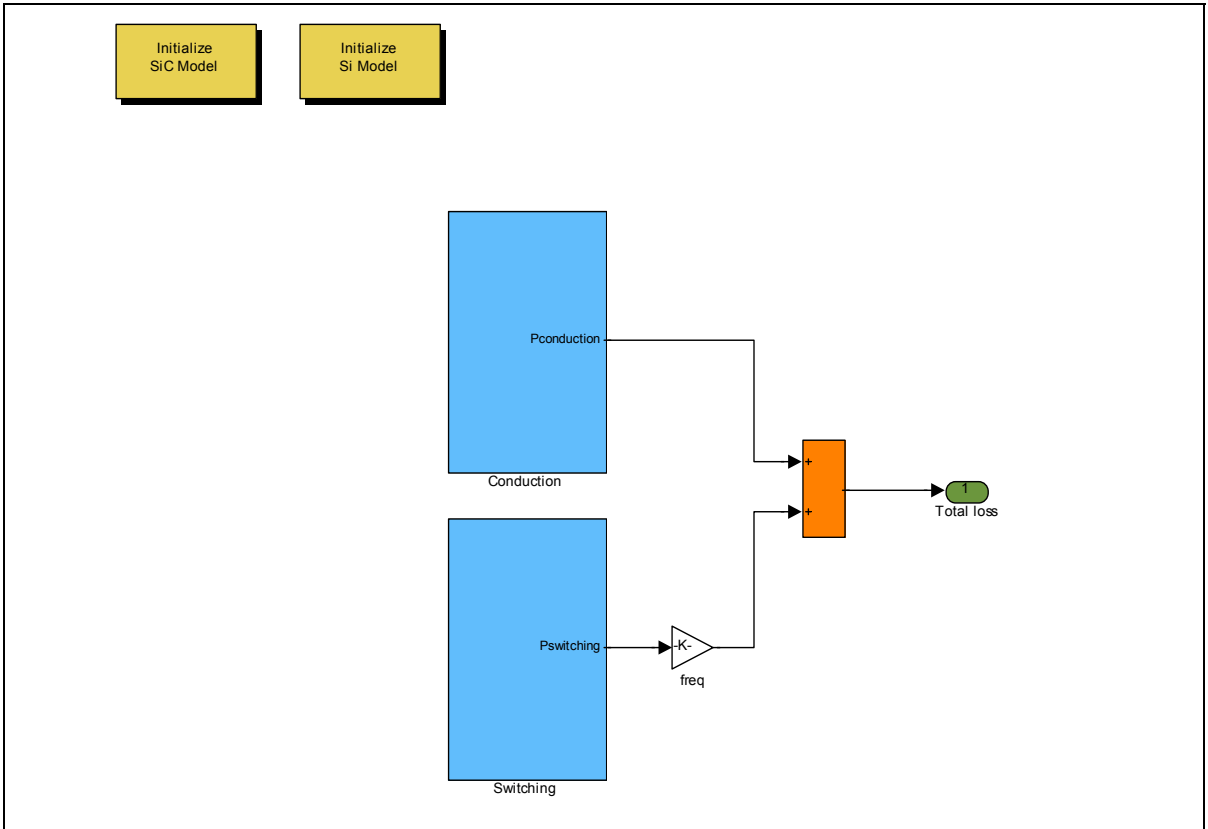
$$P_{total} = P_{conduction} + P_{switching}$$

The equations described in this section have been modeled using Matlab/Simulink. The model is, as shown in Figure 3-18. The following are details and assumptions made in the development of the model:

- The mobilities and lifetimes of holes and electrons are assumed to be constant
- The device is doped for a desired breakdown voltage

$$V_B = \varepsilon(N_a + N_d) \cdot E_c^2 / (2q \cdot N_a \cdot N_d)$$

- SiC GTO is rated at 20 kV, Si GTO is rated at 5000V, and for comparison, Si devices are assumed to be connected in series for voltage rating.



**Figure 3-18:** Simulink device model

- The model is studied for variation in temperature for different current and voltage ratings.
- The frequency of operation is 1 kHz.
- The temperature range is 300 K – 600 K. It should be noted that the silicon GTO cannot withstand more than 423 K; however, the model is tested for comparison purposes.
- The devices are subjected to a current density range of 100 A/cm<sup>2</sup> – 500 A/cm<sup>2</sup>.

The data used in the simulation is presented in Table 3.2.

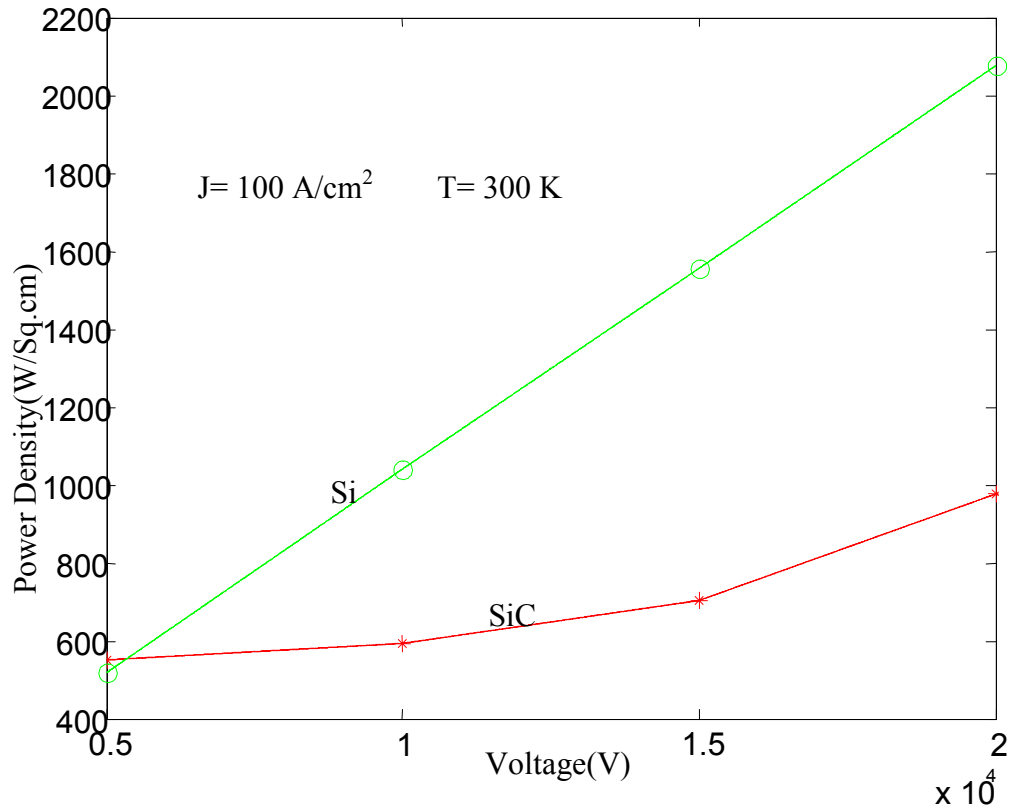
**Table 3.2 Simulation Data [23]**

Parameter	4H-SiC	Si
(E <sub>g</sub> ), Energy gap (eV)	3.2	1.1
ε <sub>r</sub> , relative permittivity	9.7	11.7
τ <sub>p</sub> , hole lifetime (s)	575e-09	575e-09
E <sub>c</sub> , critical electric field (V/cm)	2.3 e06	0.3 e06
τ <sub>n</sub> , electron lifetime (s)	1150e-09	1150e-09
μ <sub>n</sub> , electron mobility(cm <sup>-3</sup> /V·s)	800	1360
μ <sub>p</sub> , hole mobility(cm <sup>-3</sup> /V·s)	120	453
V <sub>sat</sub> , saturation velocity (cm/s)	2e07	1e07

### 3.5 Simulations

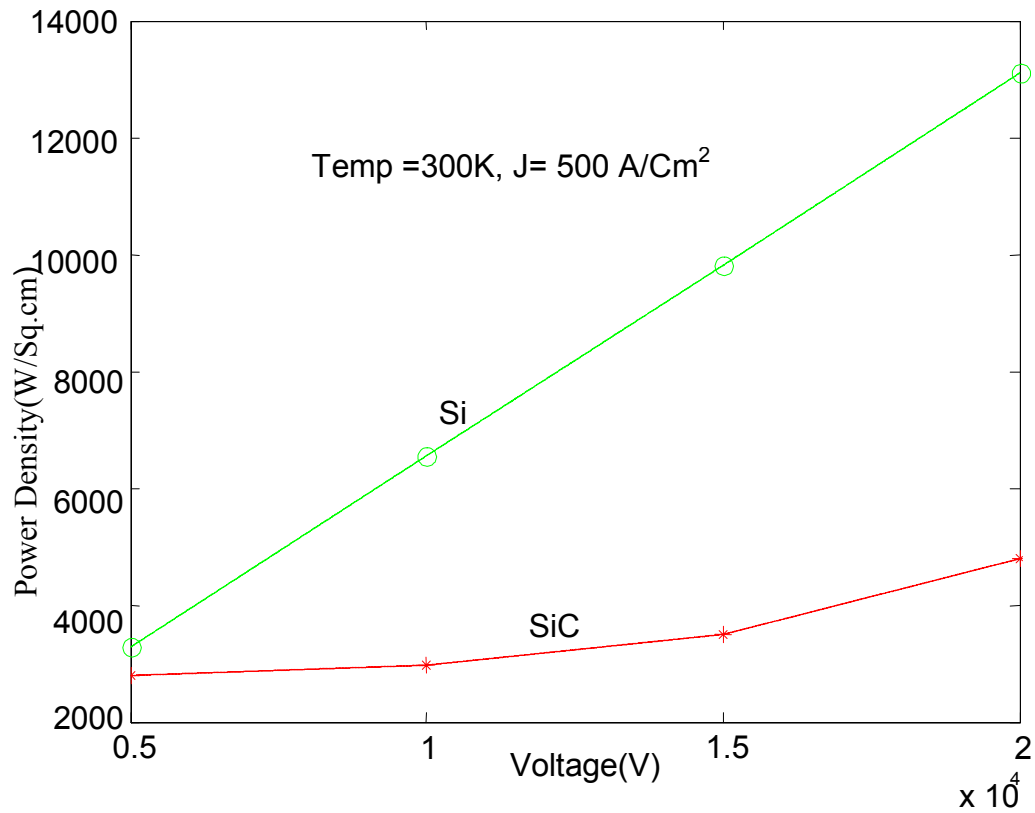
The simulations are shown in Figure 3-19, Figure 3-20, and Figure 3-21. These are few of the many cases simulated and shown for different voltage and current ratings and for different temperatures. The total power loss for the silicon GTO thyristor is more than silicon carbide GTO thyristor for the reasons stated earlier. The trend in the simulation plots is the same for different voltages, currents, and different temperatures. However, there are a few simulations with some ambiguities, which could not be accounted for. The total loss for SiC GTO was increasing with increase in temperature for most of the simulations; however, for certain operating voltage and currents a decrease in loss was observed at certain temperatures as shown in Figure 3-19. Further analysis of the simulation plots and data reveal that, the model dependency on the parameters such as voltage, current and temperature is split between the conduction and switching loss models. The conduction model is a function of current and temperature, and the switching model is a function of voltage and temperature. Hence, for a change in the operating voltage of the device, there is an increase in the switching losses only and the conduction losses would stay the same. Introduction of a temperature dependent mobility model, which has been discussed in the section 2.3 of chapter 2, solved the problem. The equations used in the mobility model are given as,

$$\mu_o = \mu_{\min} + \frac{\mu_{\max} - \mu_{\min}}{1 + \left( \frac{N_D + N_A}{N_{ref}} \right)^\alpha} \quad (3.12)$$



Volts, V	$P_{\text{cond}}$ (W) Si	$P_{\text{cond}}$ (W) SiC	$P_{\text{sw}}$ (W) Si	$P_{\text{sw}}$ (W) SiC	$P_{\text{total}}$ (W) Si	$P_{\text{total}}$ (W) SiC
5000	400	538	118	12.5	518.5	550.5
10000	800	538	236	52.5	1037	590
15000	1200	538	354	165	1555.5	702.5
20000	1600	538	472	437.5	2074	975.5

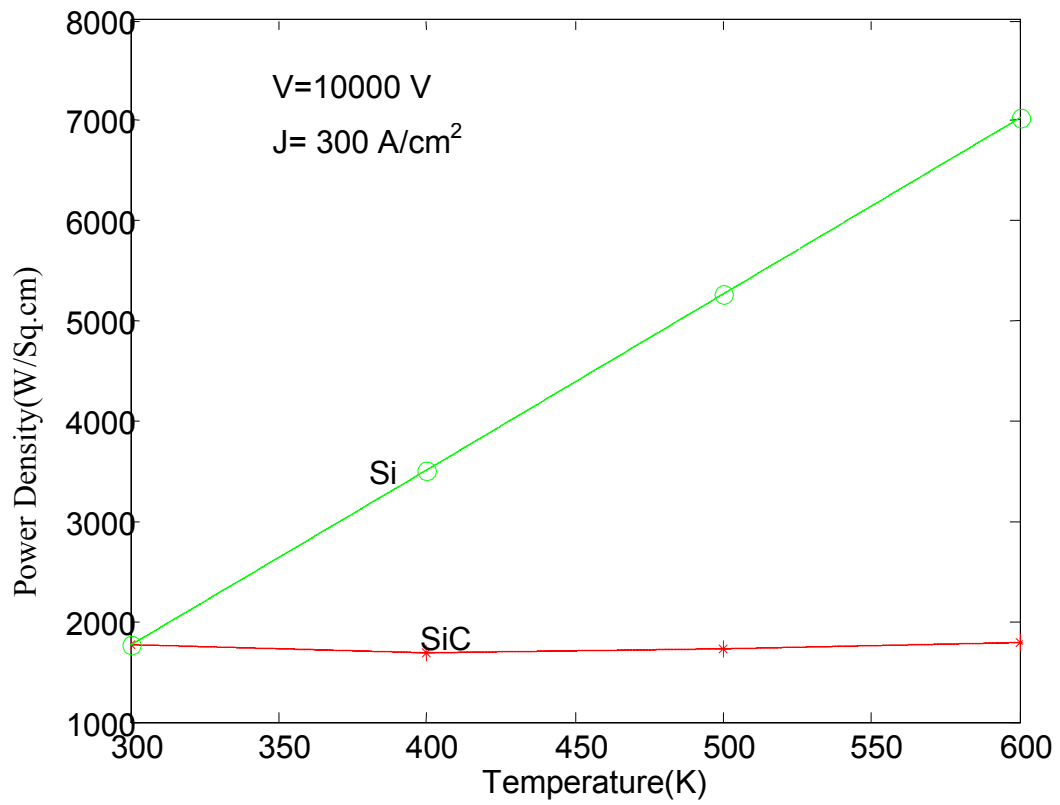
**Figure 3-19:** Device simulation for  $J = 100 \text{ A/cm}^2$ ,  $T = 300\text{K}$



Volts, V	P <sub>cond</sub> (W)	P <sub>cond</sub> (W)	P <sub>sw</sub> (W)	P <sub>sw</sub> (W)	P <sub>total</sub> (W)	P <sub>total</sub> (W)
	Si	SiC	Si	SiC	Si	SiC
5000	2000.5	2151.5	1271.5	96.5	3272	2785.5
10000	4001	2151.5	2543	264	6544	2953.5
15000	6001.5	2151.5	3814.5	787	9816	3476
20000	8002	2151.4	5086	2100	13058	4789

**Figure 3-20:** Device simulation for J = 500 A/cm<sup>2</sup>, T = 300K





Temp (K)	P <sub>tot</sub> (w)	P <sub>tot</sub> (w)
	SiC	Si
300	1762	3516
400	1694.5	3282
500	1725	3394
600	1794.5	3299

**Figure 3-21:** Device simulation for  $J = 300 \text{ A/cm}^2$ ,  $V = 10000\text{V}$

Where  $N_A+N_D$  is the total doping concentration,  $\mu_{max}$  and  $\mu_{min}$  are the minimum and maximum mobilities of electrons and holes,  $N_{ref}$  is the doping concentration for p-type and n-type material calculated empirically and  $\alpha$  is the curve fitting parameter, measure of how quickly the mobility changes from  $\mu_{min}$  to  $\mu_{max}$ .

The temperature dependence of the mobility model can be calculated as,

$$\mu = \mu_o * \left( \frac{T}{T_o} \right)^\gamma \quad (3.13)$$

where  $\mu_o$  is the value at room temperature  $T_o$ .  $\gamma$  is a constant and varies from -1.8 to -2.5 for n-type and p-type SiC materials.

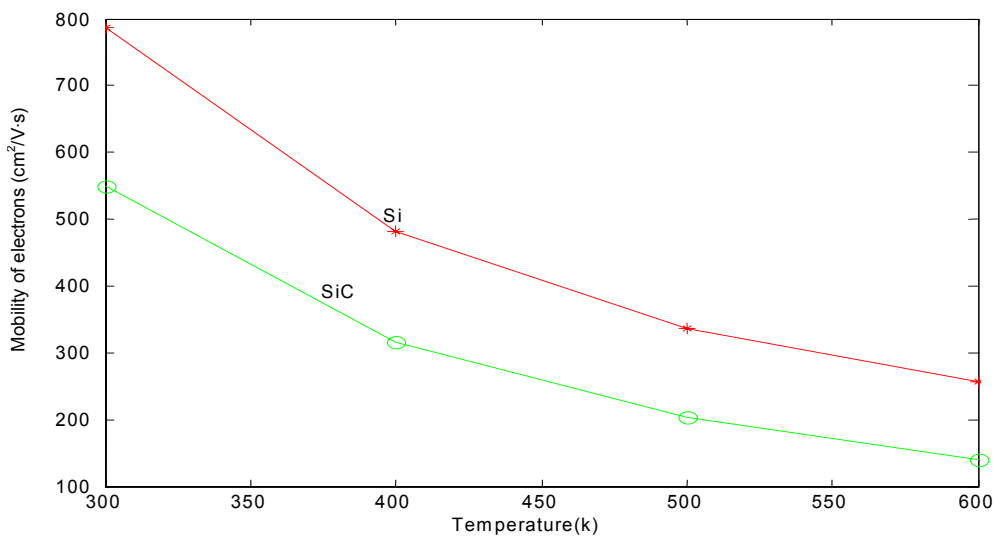
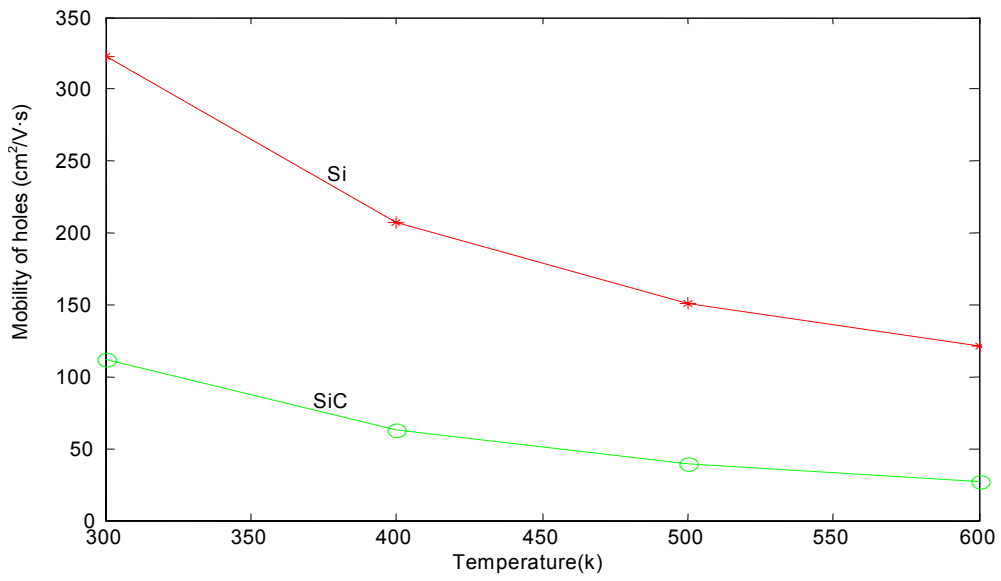
$$\mu^E(E) = \mu \left( \frac{1}{1 + \left| \frac{\mu E}{v_s} \right|^\beta} \right)^{\frac{1}{\beta}} \quad (3.14)$$

$E$  is the applied electric field,  $V_s$  is the saturation velocity, and  $\beta$  is a constant.

The data used to calculate the mobilities is given in the Table 3.3. Figure 3-22 shows the variation in the mobility of the electrons and holes as a function temperature. The temperature dependent mobility model would affect the device model because the diffusion length, which is a function of lifetime, and mobility of electron and holes will

**Table 3.3 Data for Mobility Calculation [21]**

	Si	4H-SiC
Minimum and maximum electron mobility, $\mu_{min}, \mu_{max}, [cm^2/V \cdot s]$	65, 1360	50, 950
Minimum and maximum hole mobility, $\mu_{minp}, \mu_{maxp} [cm^2/V \cdot s]$	50, 505	10, 180
Electron and hole ionization coefficients, $\alpha_n, \alpha_p$	0.91, 0.63	0.76, 0.56
Reference electron and hole concentrations, $N_{refn}, N_{refp} [cm^{-3}]$	8.5e16, 6.3e16	2.2e17, 2.35e17



**Figure 3-22:** Mobility calculations of electrons and holes for Si and SiC

vary with temperature. The expression for ambipolar diffusion length is given as,

$$L_a = (D_a \cdot \tau_a)^{0.5} \quad (3.15)$$

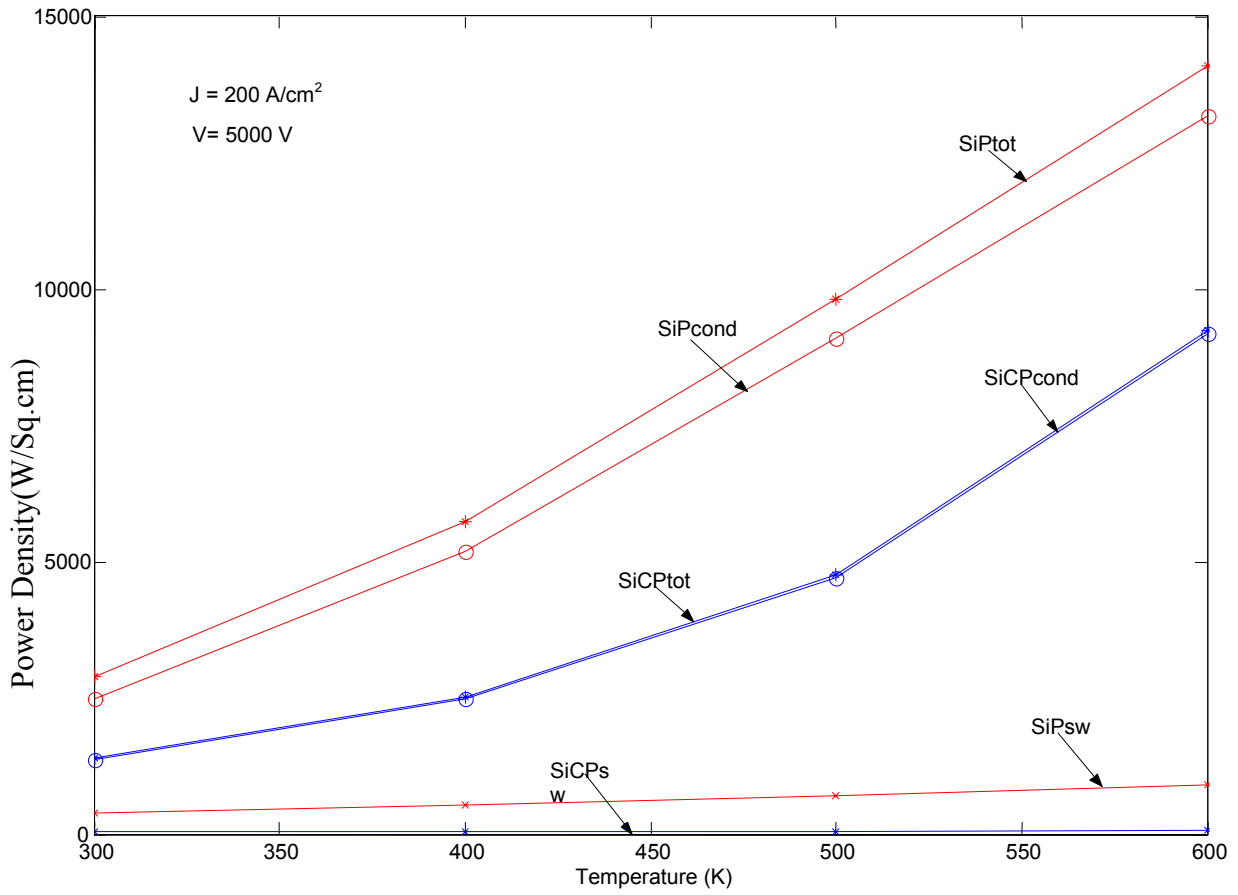
$$D_a = 2 \cdot D_n \cdot D_p / (D_n + D_p) ;$$

$$D_n = (kT/q) \cdot \mu_n ; D_p = (kT/q) \cdot \mu_p$$

Where  $D_a$  is the ambipolar diffusion constant,  $D_n$  and  $D_p$  are the diffusion constants for electrons and holes,  $\mu_n$  and  $\mu_p$  are the mobilities for electrons and holes. For low-level injection, the lifetimes are assumed to be constant and hence, the diffusion length is proportional to the mobilities. As discussed earlier, the diffusion length affects the switching losses and conduction losses, which is evident from (3.3) and (3.4). The simulations are redone using the mobility model, and the effect of the model is immediately realized. Figure 3-23, Figure 3-24, and Figure 3-25 show the total power losses of the silicon and silicon carbide GTO thyristor for 1 kHz switching.

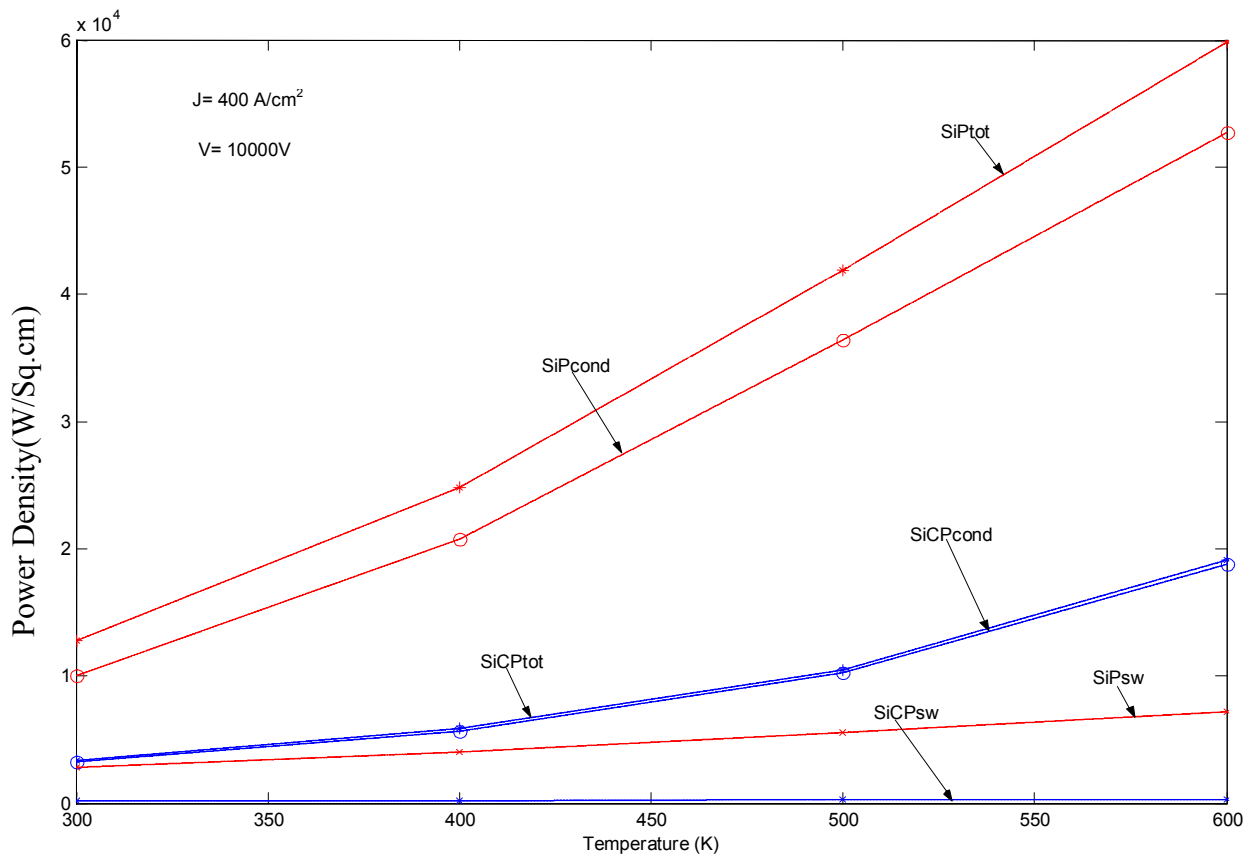
The simulations produced give an insight of the GTO thyristor loss model and losses for different ratings of the device. There are a few inferences made from the simulations, which are listed below.

- The turn-on loss is dominant at low voltage and low temperature
- Drastic increase in turn-off losses at high voltage ratings
- Turn-on losses increased with increase in temperature while the switch-off losses decreased due to the effect of mobility, which decreases with decrease in temperature.



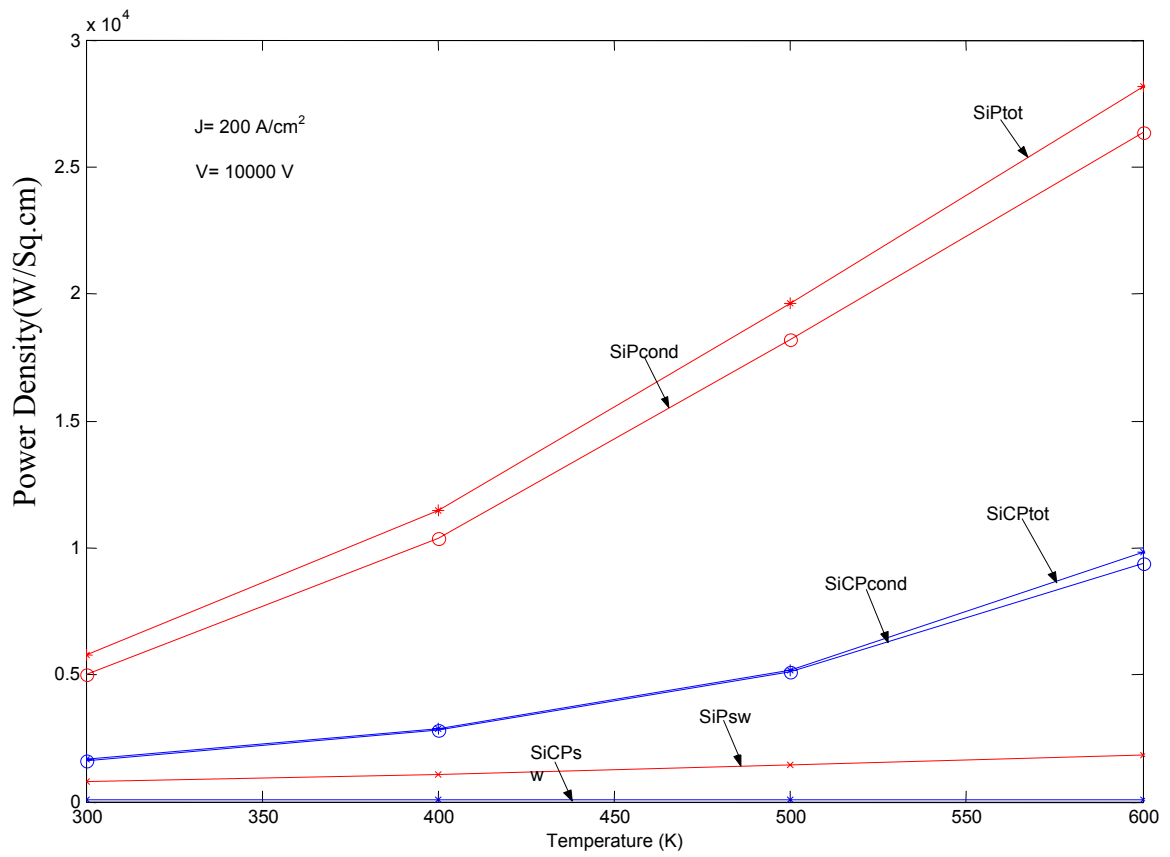
T (K)	$P_{\text{cond}}$ (W) Si	$P_{\text{cond}}$ (W) SiC	$P_{\text{sw}}$ (W) Si	$P_{\text{sw}}$ (W) SiC	$P_{\text{total}}$ (W) Si	$P_{\text{total}}$ (W) SiC
300	2491.5	1375.5	383.5	29.5	2875	2785.5
400	5194.4	2476.5	527.5	37.5	5722	2953.5
500	9093.5	4704	713.5	48	9807	3476
600	1.381e	9184	910	63	1.409e	4789

**Figure 3-23:** Device simulation for  $J = 200 \text{ A/cm}^2$ ,  $V = 5000 \text{ V}$



T (K)	$P_{\text{cond}}$ (W)		$P_{\text{sw}}$ (W)		$P_{\text{total}}$ (W)	
	Si	SiC	Si	SiC	Si	SiC
300	9966	3193	2792	172	1.27E+04	3366
400	2.08E+04	5699	4020	188.5	2.48E+04	5856.5
500	3.37E+04	1.02E+04	5550	221.5	4.19E+04	1.05E+04
600	5.24E+04	1.88E+04	7137	265.5	5.98E+04	1.91E+04

**Figure 3-24:** Device simulation for  $J = 400 \text{ A/cm}^2$ ,  $V = 10000 \text{ V}$



T (K)	$P_{\text{cond}}$ (W) Si	$P_{\text{cond}}$ (W) SiC	$P_{\text{sw}}$ (W) Si	$P_{\text{sw}}$ (W) SiC	$P_{\text{total}}$ (W) Si	$P_{\text{total}}$ (W) SiC
300	4983	2596.6	767	68.5	5.75E+03	1665
400	1.04E+04	2843	105	65	1.14E+04	2899
500	1.82E+04	5.12E+03	1427	69.5	1.96E+04	5.19E+03
600	2.64E+04	4.40E+03	1820	78.5	2.89E+04	9.84E+03

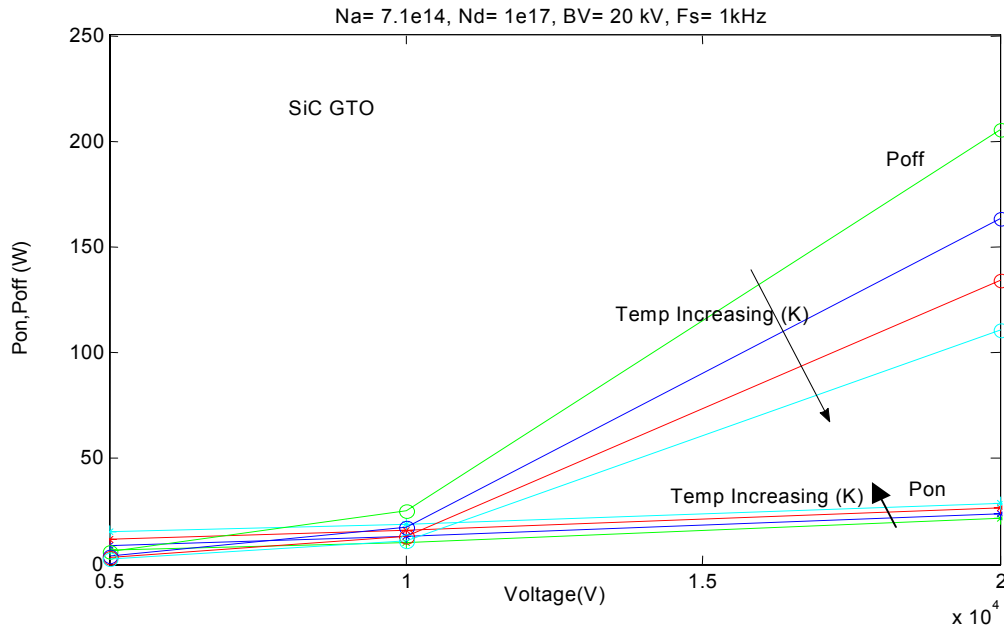
**Figure 3-25:** Device simulation for  $J = 200 \text{ A/cm}^2$ ,  $V = 10000 \text{ V}$

These inferences are obtained after an in depth analysis of the data obtained from the simulations. The data obtained from different simulations is plotted as shown in Figure 3-26 and Figure 3-27.

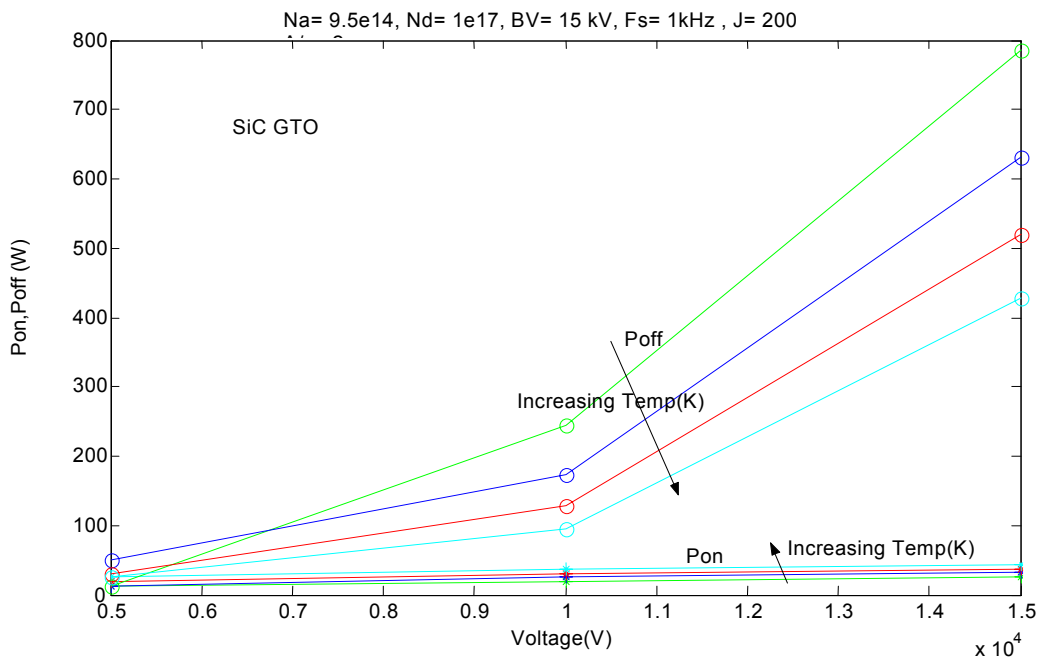
However, the turn-on and turn-off losses are increasing with increase in voltage and current, which further substantiates the normal behavior of the model.

The silicon and silicon carbide GTO thyristors have been modeled and studied in this chapter. It is found that the conduction losses of a silicon GTO thyristor are at least twice more than silicon carbide device. The switching losses of silicon carbide GTO thyristor are at least 12 times less than the silicon device. The various simulation studies made on the device models in this chapter will be used to study and analyze the system model behavior in the next chapter.





**Figure 3-26:** Switching losses of SiC GTO thyristor



**Figure 3-27:** Switching losses of SiC GTO thyristor

## **4.System**

In the previous chapter the individual device modules were discussed and the simulations results were presented to study the comparison between Si and SiC GTOs for various operating conditions. In this chapter, the system model of the HVDC transmission system will be presented, and the loss model will be integrated in the system to study the effect of the Si and SiC devices on the system.

HVDC system has many different configurations as discussed in chapter 1. A specific configuration is chosen for the study, and more emphasis is placed on the converter performance results. A simple 6-pulse converter configuration is chosen. EMTDC simulation software is used to develop the system model, and the model is interfaced with SIMULINK device loss model for the purpose of loss analysis for a specific system rating.

The simulation results are investigated to study the efficiency, reduction in device cost by using SiC GTO, and also the possible advantages of SiC GTO over the Si GTO are also discussed based on the devices' loss model developed.

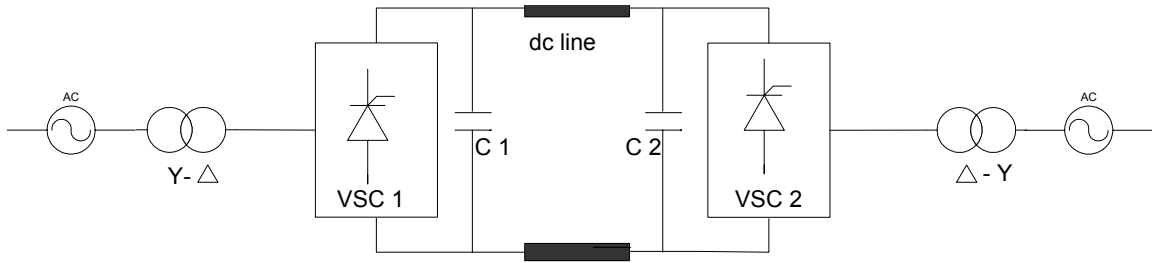
### **4.1 VSC Technology**

The line commutated thyristor current source converters used in the present HVDC system have a few problems like commutation failure and reactive power compensation requirement, which affect the overall system performance. Modern HVDC systems employ voltage source converters, and using this technology provides an

improvement in the system performance technically and from an economic standpoint. As discussed in chapter 1, the voltage source converter technology requires devices with turn-off capability like IGBT and GTO. The rapid progress in the development of these devices has improved the performance of voltage source converter technology and is gaining wide attention for high voltage applications. The voltage source converter has the following advantages [25]:

- No commutation failure, and there is no need for ac source for commutation – due to use of self commutated device
- Reduced filter sizes – due to reduced low-order harmonics
- No additional reactive power supply is required – since there is no reactive power consumption on the ac side, unlike the conventional thyristor converter
- Independent control of active power and reactive power
- Can supply to an isolated remote load with no local power generation
- Improved system stability – ability to control reactive power in the ac system maintains the ac bus voltage.
- Improved dynamic response characteristics – increased switching frequency using pulse width modulation (PWM) technique.

Figure 4-1 shows the basic configuration of the voltage source HVDC transmission system. The main components of the system are converters, transformers and the dc circuit.



**Figure 4-1:** Basic configuration of VSC transmission

### 4.1.1 Basic Structure

#### DC Circuit:

The DC circuit is comprised of storage capacitors and the DC cable or overhead line. The DC voltage provided by the capacitor is fixed in polarity, and the reversal of power flow is achieved by changing the direction of DC current, unlike the conventional HVDC system where the power flow reversal is through change in voltage polarity. Since the voltage is fixed, the cables do not require special insulation designs as in ac systems. The length of the cable is not a constraint as in ac systems, which requires reactive power management.

#### Transformers:

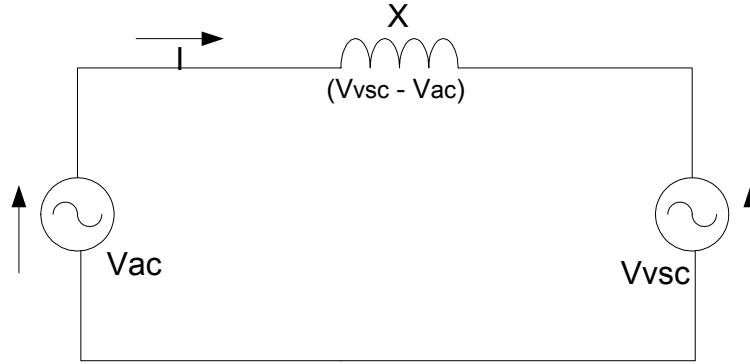
The most important functions of a transformer are [26]:

- To provide a reactance between converter AC terminals and AC system.
- To transform the AC system voltage to the converter voltage ratings and currents
- To connect two single pulse converters to form a 12 pulse group and provide isolation.

### **Voltage Sourced Converters (VSC):**

Converters can be divided into two major groups based on their operation principle (i) Line or natural commutated converters, and (ii) self or forced commutated converters. Further, the self-commutated converters can be classified as voltage source and current source converters based on the design of the DC circuit. CSC operates with a large inductor, and VSC operates with a storage capacitor.

The VSC can be classified based on pole topology and also converter topology. The switches can be arranged for different levels, each level consisting of a turn-off device and diode. The possible configurations are two level, three level and multi-level. The increase in the number levels increases the cost and size of the valve; however, the power losses will be less, and the quality of the voltage output will be good. Also, the increase in the levels increases the voltage handling capacity of each phase leg or the pole. Based on the converter topology, the possible configurations are 6-pulse, 12-pulse, 24-pulse, 48-pulse, and n-pulse. Each configuration has multiple six-pulse converters according to the pulse-order. As the order of the pulse increases, the harmonics of the converter output will be reduced, and the converter rating can also be increased. The selection of converter topology is based on factors such as complexity, installation costs, harmonic issues and control issues [27].

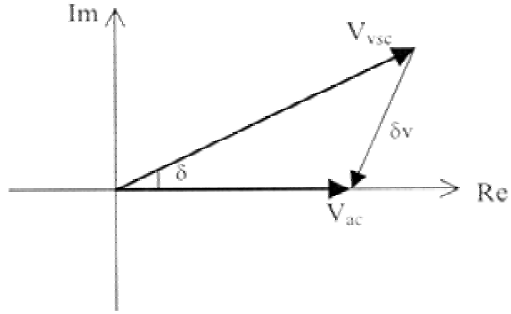


**Figure 4-2:** Equivalent circuit of VSC transmission

#### 4.1.2 Operating principle

The equivalent circuit of one end of a VSC transmission system is shown in Figure 4-2.  $V_{ac}$  and  $V_{vsc}$  are the magnitudes of the ac system voltage and VSC respectively.  $X$  is the inductive impedance of the system, and the capacitance and resistance of the line are neglected. The voltage difference between these voltages determines the power flow, and is effectively the voltage drop across the line,  $\delta V$ .  $\delta$  is the angle between  $V_{ac}$  and  $V_{vsc}$  determined by the voltage drop and is generally small. The phasor diagram is shown in Figure 4-3. The active power can be controlled by adjusting the phase of the  $V_{vsc}$ . If the  $V_{vsc}$  is phase advanced, the active power flows from the converter to the ac system, and vice versa if the phase is delayed. The expression for active power flow is given as

$$P = V_{vsc} \cdot V_{ac} \cdot \sin \delta / X$$



**Figure 4-3:** Phasor diagram

The reactive power flow can be controlled by regulating the output voltage of the converter. If the converter voltage  $V_{vsc}$  is less than the ac system voltage the reactive power flows from the system to the converter, and vice versa if the voltage  $V_{sc}$  is greater. The reactive power can be expressed as,

$$Q = (V_{vsc} \cdot \cos \delta - V_{ac}) \cdot V_{vsc} / X$$

The voltage source technology has several applications due to the advantages it offers [26].

- Interconnecting lower and middle power range, and isolated or weak ac systems.
- Connecting two different distributed energy source plants
- Multi- terminal HVDC systems
- Serves as auxiliary power supply in a plant when there is a failure
- Provide reactive power support with voltage magnitude and frequency control

The voltage source converter technology is realized as a potential technology to replace the existing conventional thyristor based HVDC systems. However, the voltage source converter transmission technology has high capital costs, and also high converter losses compared to the conventional HVDC system, due to the high power losses in the switching devices like IGBT and GTO thyristor. With continued development in the power semiconductor devices, the installation cost and the performance of the converter can be improved. There have been many developments, and this study focuses on silicon carbide GTO thyristor impact on the converter performance.

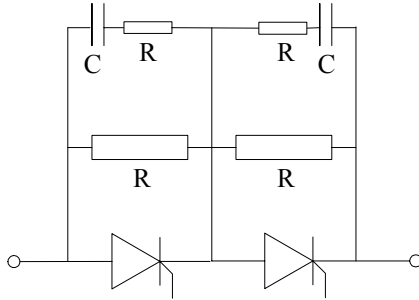
#### **4.2 Converter Rating Improvement**

Most of the power applications involve converters with a rating that a single device per valve per leg cannot operate at. There are several different methods to design the converter to withstand the high power ratings, and a few of them are presented below:

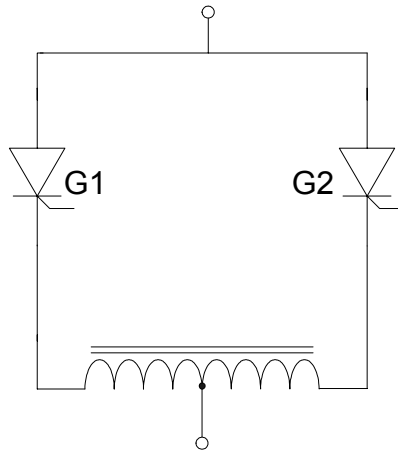
- 1). The converter pulse-order can be increased so that the harmonics are reduced and the rating can be increased with still one device per valve.
- 2). Increasing the number of levels so that the voltage can be increased, and hence the capacity of the single device.
- 3). By paralleling the phase legs so that power rating can be increased.
- 4). Series connection

Connecting the devices in series for high voltage rating is the most commonly used design technique. However the equal voltage sharing is problematic and has to be forced using a resistor in the steady state. A low non-inductive resistor and capacitor in.





**Figure 4-4:** Series connection and protection for voltage rating

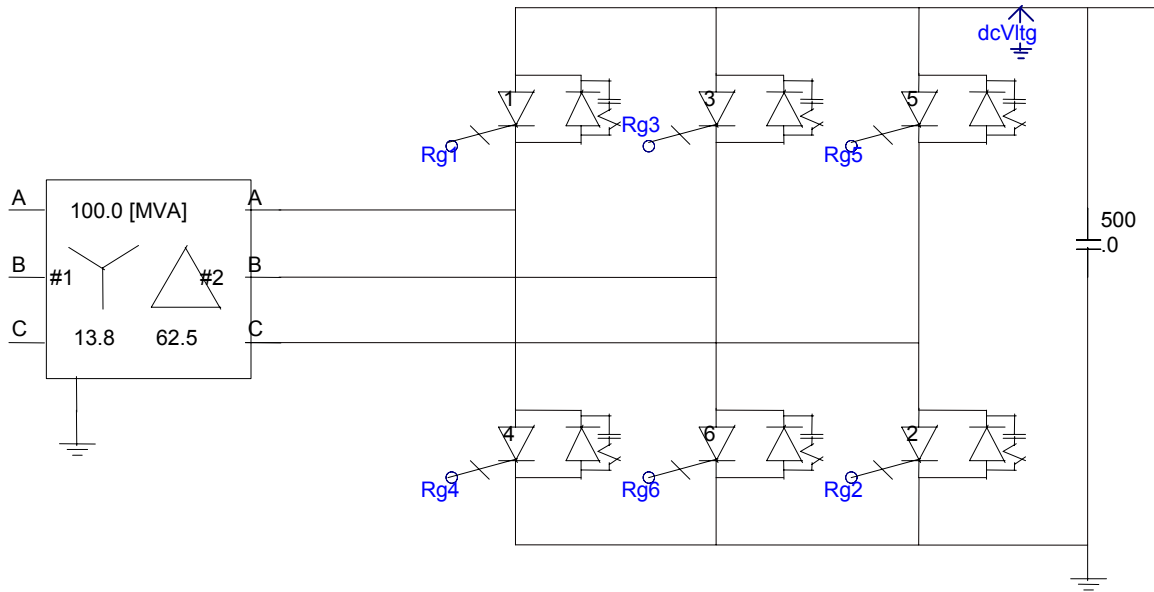


**Figure 4-5:** Parallel connection for current rating

series are placed in parallel to control the transient response. The series connection is shown in Figure 4-4.

#### 5). Parallel connection

Several groups can be connected in parallel to handle the high current rating. However, if the devices are not matched, then the current division may differ from device to device. Using external reactors, equal current sharing can be achieved. Generally, when the load current is greater than the device current rating, operation is parallel. The arrangement for current sharing is shown in Figure 4-5.



**Figure 4-6: 3-Phase full-bridge six-valve converter**

### 4.3 HVDC System

The configuration chosen for the study is a simple monopolar configuration as described in section 1.3. The transmission system is based on voltage source converter technology, unlike the one discussed in chapter 1. The converter at both ends is a voltage source converter also known as a forced commutated converter. The structure is the same as the basic structure described in the previous section. The system model is designed to emulate the ac characteristics as discussed in chapter 1. The main assumption made in the model is that one substation is the sending end and the other is the receiving end. The converter arrangement is as shown in Figure 4-6. The converter configuration is a two-level, six-pulse 3-phase full bridge converter.

### 4.3.1 System Specifications

- Transformers

Rectifier end : 3 phase 2 winding transformer

100MVA, 60 Hz, Y-Delta, 13.8 kV – 62.5 kV

Inverter end : 3 phase 2 winding transformer

100MVA, 60 Hz, Delta-Y, 62.5 kV – 115 kV

- Filters

Inverter end: RC filter bank - 139  $\mu$ F, 0.5 ohm each

Rectifier end: Capacitor bank – 2  $\mu$ F each

- Cable: The cable modeled represents two coaxial cables buried 1m underground and separated by 40 cm. It is 100 km long.
- Synchronous generator: 75MVA
- Three voltage source: 115kV (line-line base voltage), 60 Hz, 100MVA base(3 phase)

### 4.3.2 Control System

As discussed in section 4.1.2 the active power transfer in a system is given as,

$$P = V_1 \cdot V_2 \cdot \sin \delta / X$$

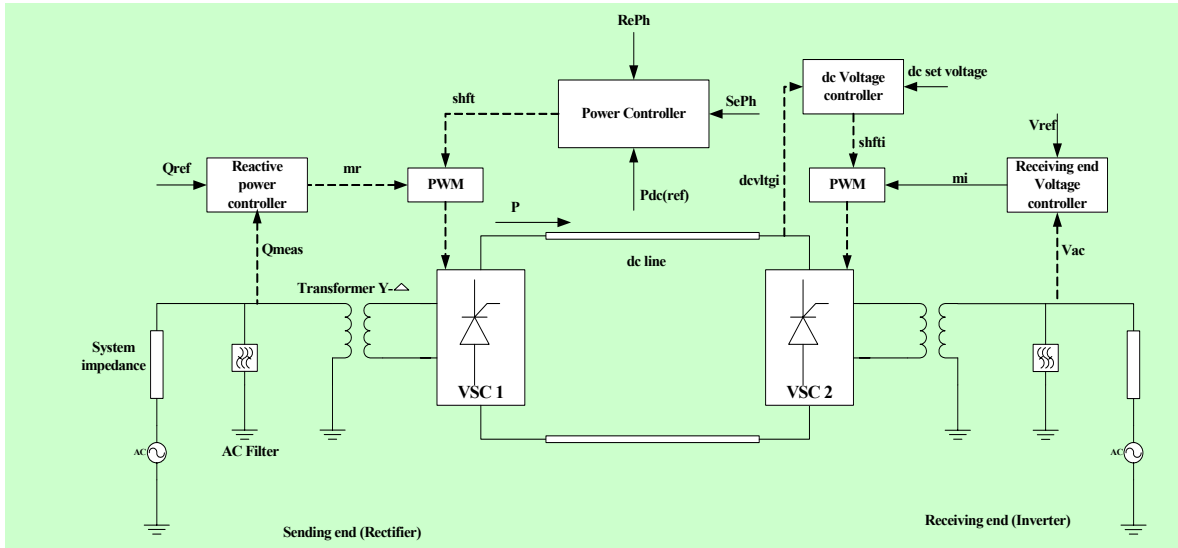
Where  $V_1$  and  $V_2$  are the ac voltage magnitudes at the sending end and receiving end respectively.  $X$  is the inductive reactance of the dc cable and  $\delta$  is the angle between the sending and receiving end voltages. It is evident from the equation that there are three degrees of freedom that can be used to control the power flow. So for a constant dc

power in the system, the voltage at the dc link should be constant, and also the current through the overhead line or the cable should also be constant. So assuming the resistance to be constant, the line losses do not vary much and will be almost constant. If the magnitude of the ac voltages at sending, and receiving end is maintained to be constant, then the power flow can be controlled by adjusting the phase angle  $\delta$ . Figure 4-7 gives an overview of the control system implemented in the system.

Fixed controllers and several small controls are implemented at both ends to provide the required performance of the system. For simplicity, the left hand end is fixed as the sending end, and the right hand side end as the receiving end. The control system is designed such that the sending end (or the rectifier end) controls the amount and direction of power transferred across the dc link, and the receiving end (or the inverter end) controls the dc voltage. The rectifier controls the power as a function of the phase angle difference between sending and receiving end ac voltages, and also controls the reactive power at the sending end. A synchronous generator supplies the ac power at the sending end and controls the ac voltage at the sending end. The inverter controls the ac voltage magnitude, and the dc voltage. Pulse width modulation techniques are employed to control the operation of the converters at both ends.

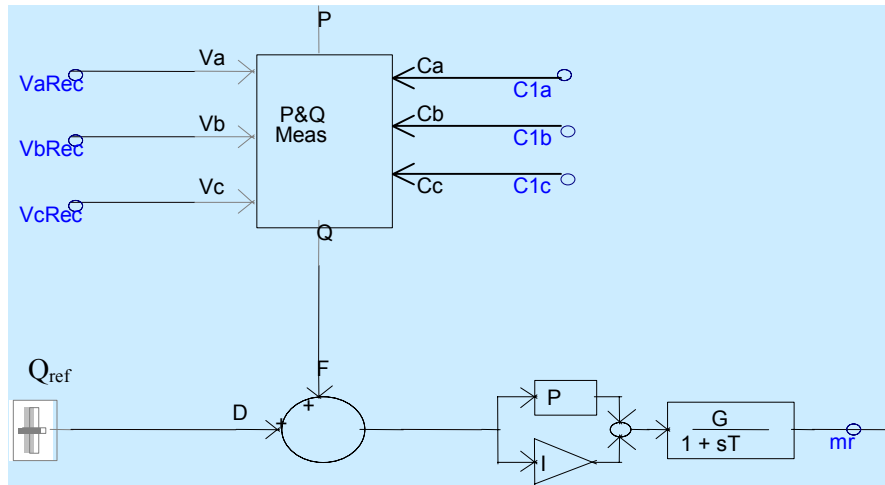
### **PWM Control at the Rectifier End**

Sine triangle PWM technique is implemented to control the sending end converter operation. The frequency of the carrier triangular wave is 33 times the fundamental frequency. As stated in [1],  $m_f$  is chosen to be a multiple of three in order to eliminate the even harmonics, and the high  $m_f$  reduces harmonics and hence filtering.



**Figure 4-7:** Overview of the HVDC control system

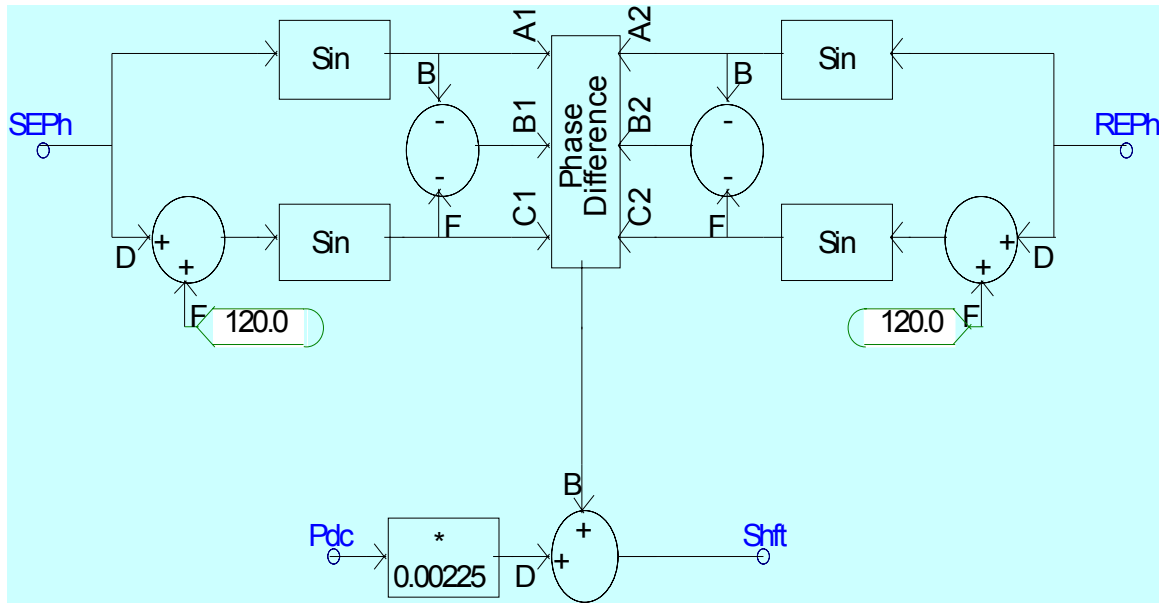
However, the high switching frequency causes more losses in the converter. A 3-phase, PI controlled phase locked loop (PLL) is used to synchronize pulses to the input voltage. The magnitude of the PWM sinusoidal reference signal arrays at fundamental frequency is controlled by signal  $mr$  and the phase is controlled by signal  $shft$ . Firing pulses are generated using a comparison of reference signals to triangular signals - two sets of signals (reference and triangular ones) are needed, one set for turning on and the second one (a negation of the first set of signals) for turning off. The two signals are sent to each switch, the first one tells to turn on or off; the second one determines an exact moment of switching. The two signals  $mr$  and  $shft$  are generated by the controllers to control the power flow through the system.  $mr$  is the modulation index for the PWM control at the rectifier end. The sending end reactive power controller generates



**Figure 4-8:** Reactive power controller at the sending end

the signal  $mr$ , and is controlled to achieve the desired reactive power at the sending end by setting the reactive power reference. The PI control used is shown in Figure 4-8.

$Shift$  is the phase angle order in degrees derived from the open loop power controller. It is the angle by which the voltage across the sending end transformer is phase shifted in order to control power flow. This signal is fed to the PWM control to phase shift the sine wave to control the power transfer. The power flow controller is shown in Figure 4-9. The  $shift$  signal is generated as function of the phase difference between the sending end and receiving end voltage phase angles. The measured phase difference is synthesized using the dc power reference signal ( $P_{dc}$ ). The synthesized phase angle across the transmission line is filtered then phase advanced to cause ac system damping if high frequency control oscillations are detected. This control causes the VSC



**Figure 4-9:** Power flow controller

transmission to emulate the characteristics of an ac line by controlling power using the synthesized ac voltage phase angle difference measured between each end.

### **PWM control at the inverter end**

The PWM control at the inverter end is the same as the rectifier end with the same specifications and the same design to generate the firing pulses. However, the control strategy at this end, as stated earlier, is to control the dc voltage of the dc link and ac voltage magnitude. Hence the control signals to control the PWM controller are different. The magnitude of the PWM sinusoidal reference signal arrays at fundamental frequency is controlled by signal *mi* and the phase is controlled by signal *Shfti*. *mi* is the modulation index for the PWM control at the inverter end. The receiving end voltage controller generates the signal *mi*. The output of the PI controller is used to control the voltage

magnitude. The modulation index is a function of the difference between the measured voltage and reference ac voltage. The controller is shown in Figure 4-10.

The *shfti* signal is generated from the dc voltage controller at the receiving end. It is function of the difference between measured dc volts *dcVltgl* and dc voltage set point at receiving end (in kV). The control acts to adjust the phase of the ac side of the receiving end converter. When dc volts are too high, the phase angle is adjusted to push power into the receiving end ac system. If more power is thus extracted from the dc system than is ordered by the sending end power controller, the dc voltage is lowered. The dc voltage controller is shown in Figure 4-11.

#### **4.4 System Simulations**

The system model and the various control systems described in earlier sections have been implemented using PSCAD/EMTDC software. PSCAD/EMTDC is a simulation tool for analyzing power systems. PSCAD is the graphical user interface and EMTDC is the simulation engine. This software is most suitable for simulating the electromagnetic transients of the electrical systems. This software also has an excellent feature of interfacing MATLAB/SIMULINK, and hence has the flexibility of interfacing various MATLAB/SIMULINK models. The device models, which were discussed in the previous chapter, have been interfaced with the HVDC system model. The system model has been developed from an example of the PSCAD and modified for the specifications listed in the previous sections. A program was written in FORTRAN 99 to interface the SIMULINK device models. Figure 4-12 shows an outline of the system interface.



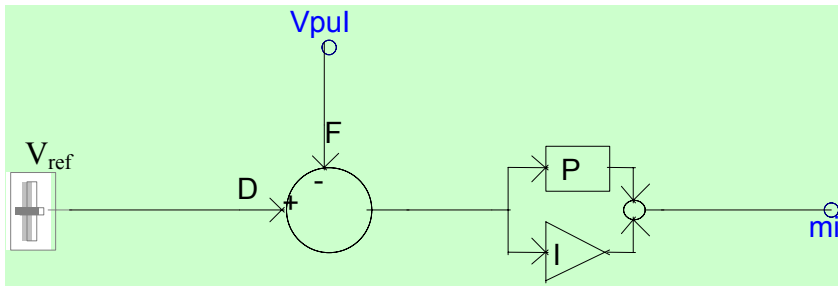


Figure 4-10: Voltage controller at the receiving end

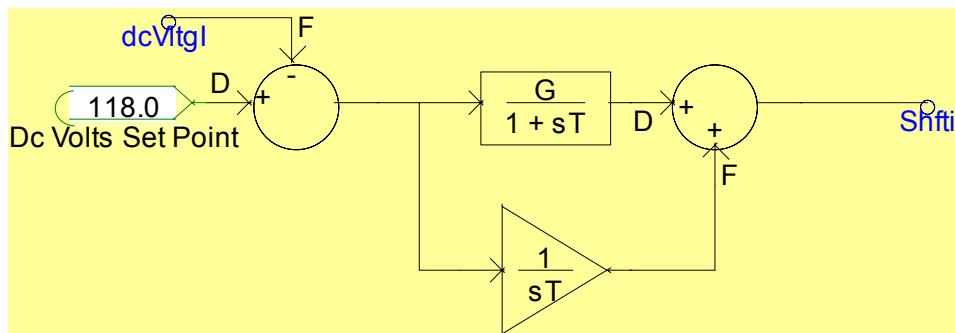


Figure 4-11: dc voltage controller at the receiving end

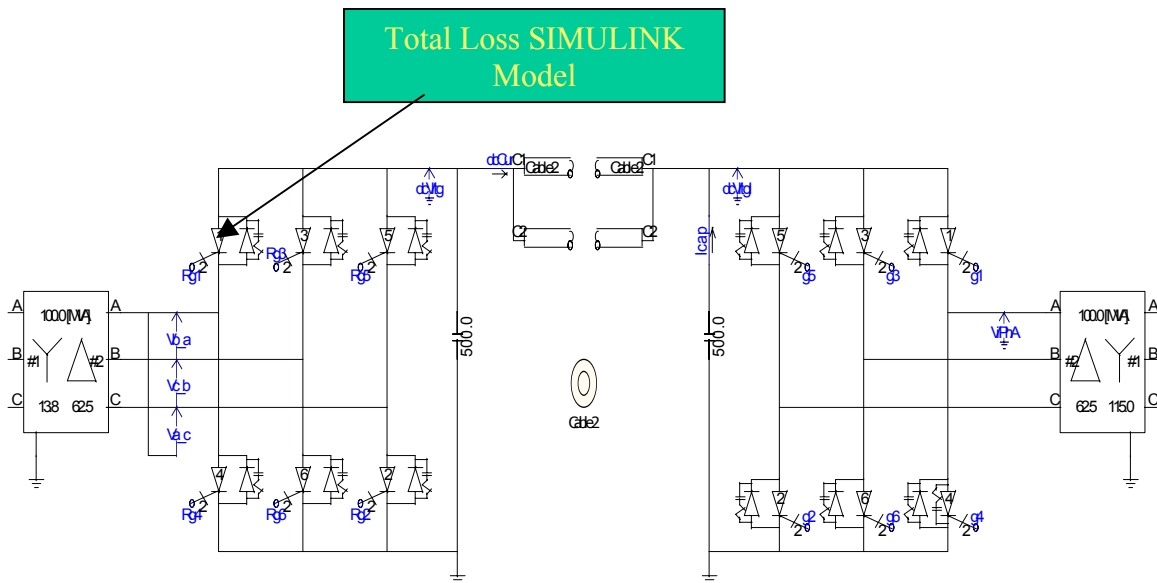


Figure 4-12: SIMULINK interface with PSCAD/EMTDC

## FORTRAN Subroutine for SIMULINK Interface

```
#STORAGE REAL:11
#LOCAL INTEGER I_CNT
!
! Transfer inputs to STOR? locations
STORF (NSTORF)= TIME
DO I_CNT = 1, $#DIM(sig_in)
STORF (NSTORF + I_CNT) = $sig_in( I_CNT )
ENDDO
! Call interface
CALL SIMULINK_INT("$Path","$simfile","R(3)")
! Output to STOR?
#IF $#DIM(sig_out) > 1
DO I_CNT = 1, $#DIM(sig_out)
$sig_out(I_CNT) = STORF( NSTORF + $#DIM(sig_in) + I_CNT)
ENDDO
#ELSE
$sig_out = STORF( NSTORF + $#DIM(sig_in)+ 1)
#ENDIF

! Update NSTOR?
NSTORF = NSTORF + 1 + $#DIM(sig_in) + $#DIM(sig_out)
```

Figure 4-13 shows the SIMULINK interface block.

### Simulation specifications

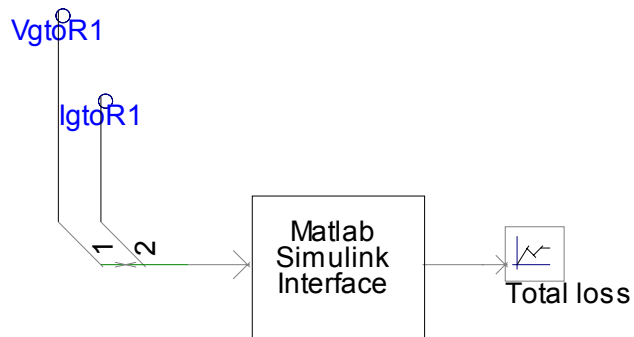
- System ratings: 120 kV dc link, upto 75 MW power delivered to the receiving end
- Device ratings: SiC - 20kV/ 5kV, 200 A/cm<sup>2</sup> , Si – 5kV, 200 A/cm<sup>2</sup> , 400 A/cm<sup>2</sup>
- Number of devices: As discussed earlier, by arranging the devices in series and parallel the converter can handle high voltages and currents. For a rating of 120kV, 1000 A, which is the maximum voltage and current, there are several possible arrangements based on the device rating.

SiC devices: 5 parallel strings of 6 devices in series (for 20kV, 200A device).

5 parallel strings of 24 devices in series (for 5kV, 200A device).

Si devices: 3 parallel strings of 24 devices in series (for 5kV, 400A device).

5 parallel strings of 24 devices in series (for 5kV, 200A device).

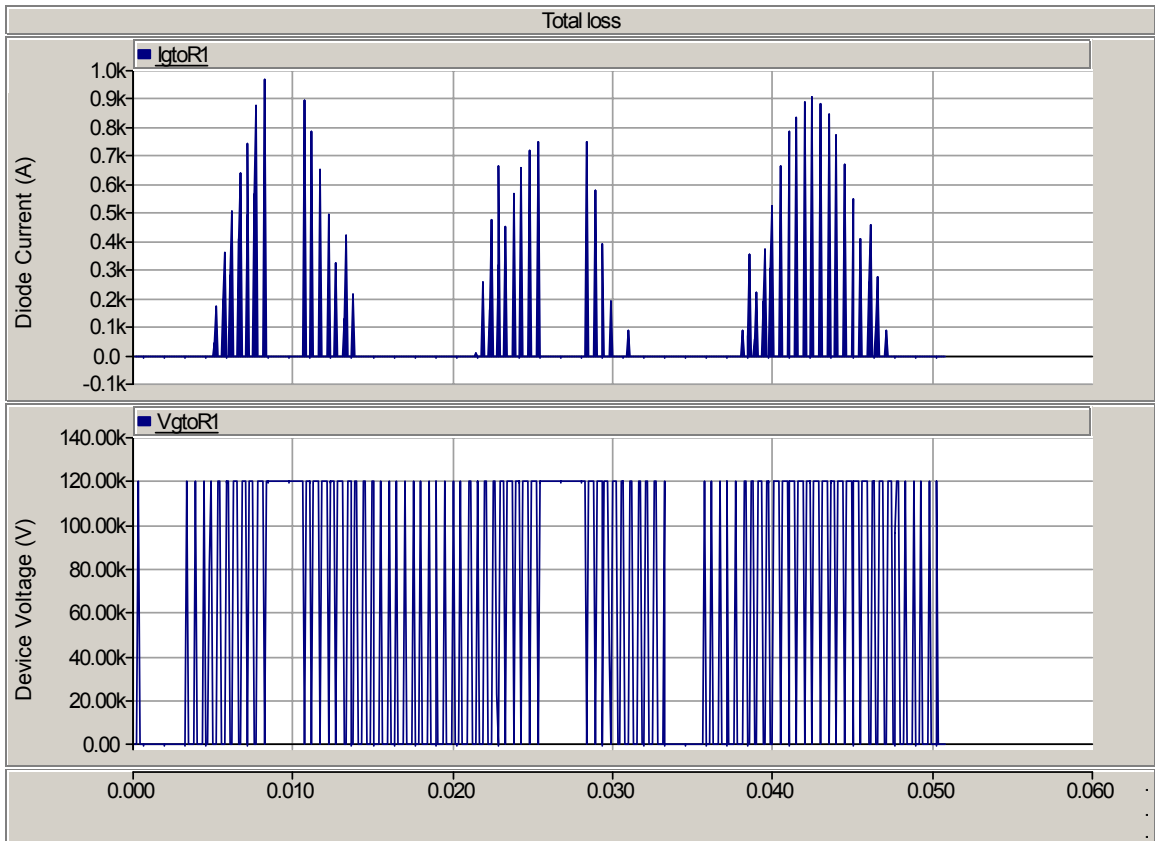


**Figure 4-13:** SIMULINK interface block

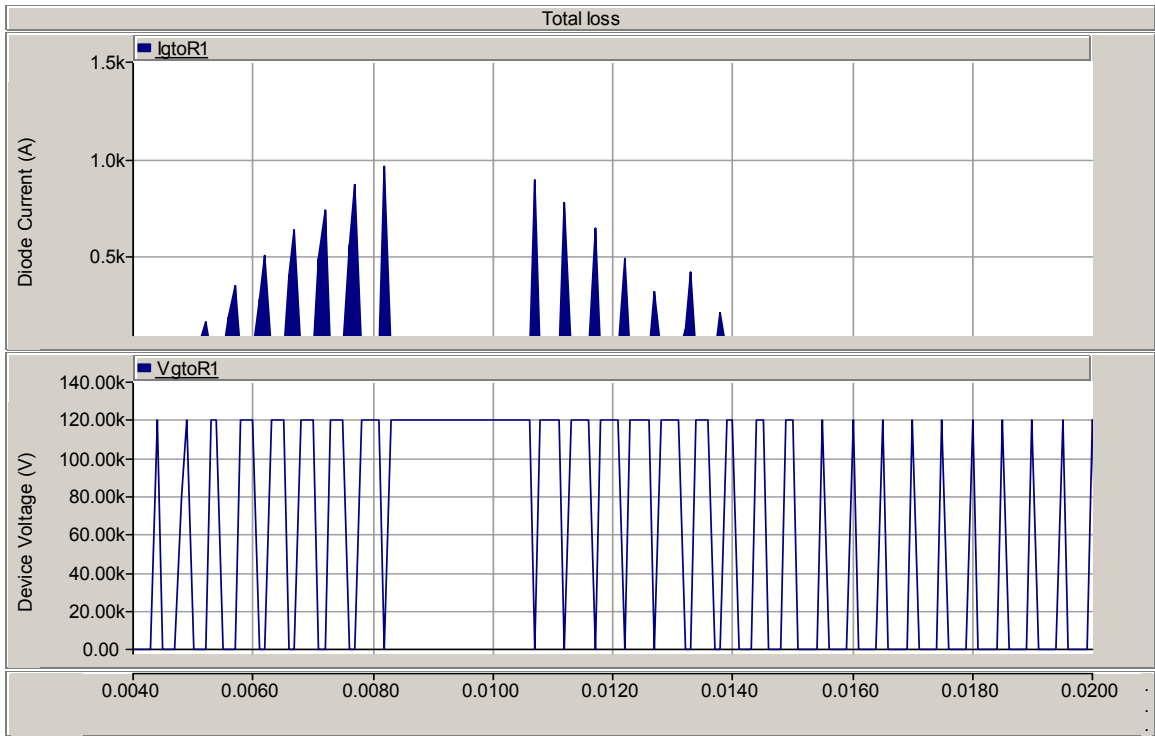
- The voltage and current profiles are obtained from the single GTO device valve of one phase leg in the converter.
- The model is tested for a temperature range of 27° C – 200 ° C.
- Simulation is started from a snapshot to initialize the steady state operating values.
- The switching frequency is 2 kHz – as the frequency modulation index is 33 times the fundamental, which is 60 Hz.

#### 4.5 Results

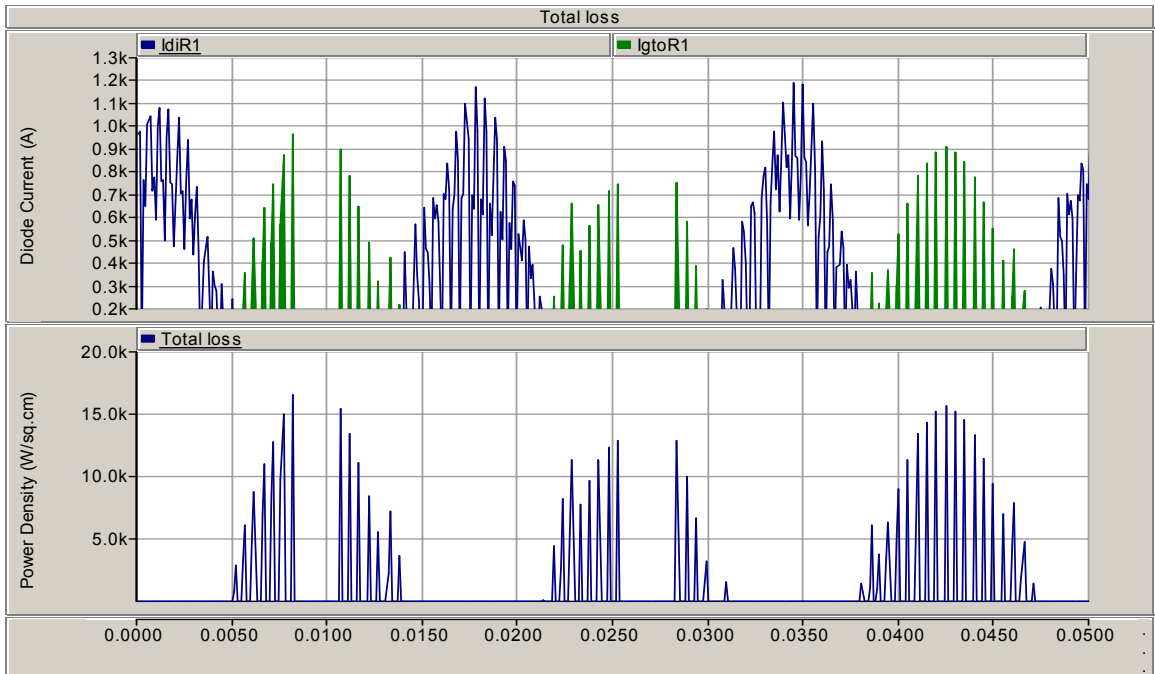
The simulation results for different operating conditions are presented in figures from Figure 4-14 to Figure 4-23. The graphs show device voltage and current profiles at 100°C, and the total device losses for a few cycles of the fundamental at different temperatures.



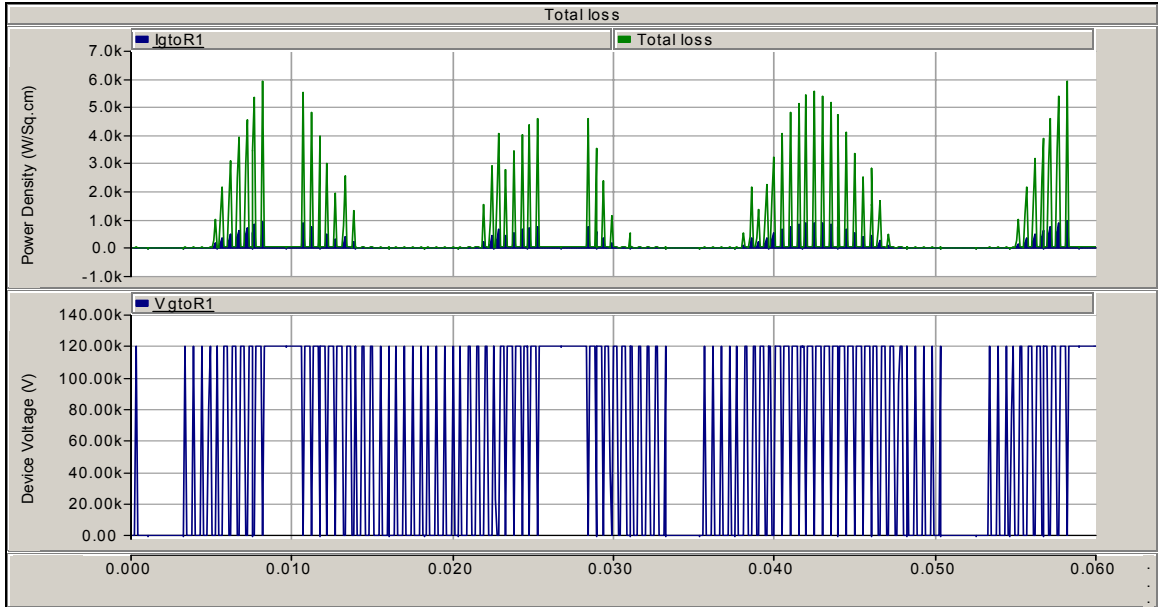
**Figure 4-14:** Voltage and current profiles from PSCAD/EMTDC



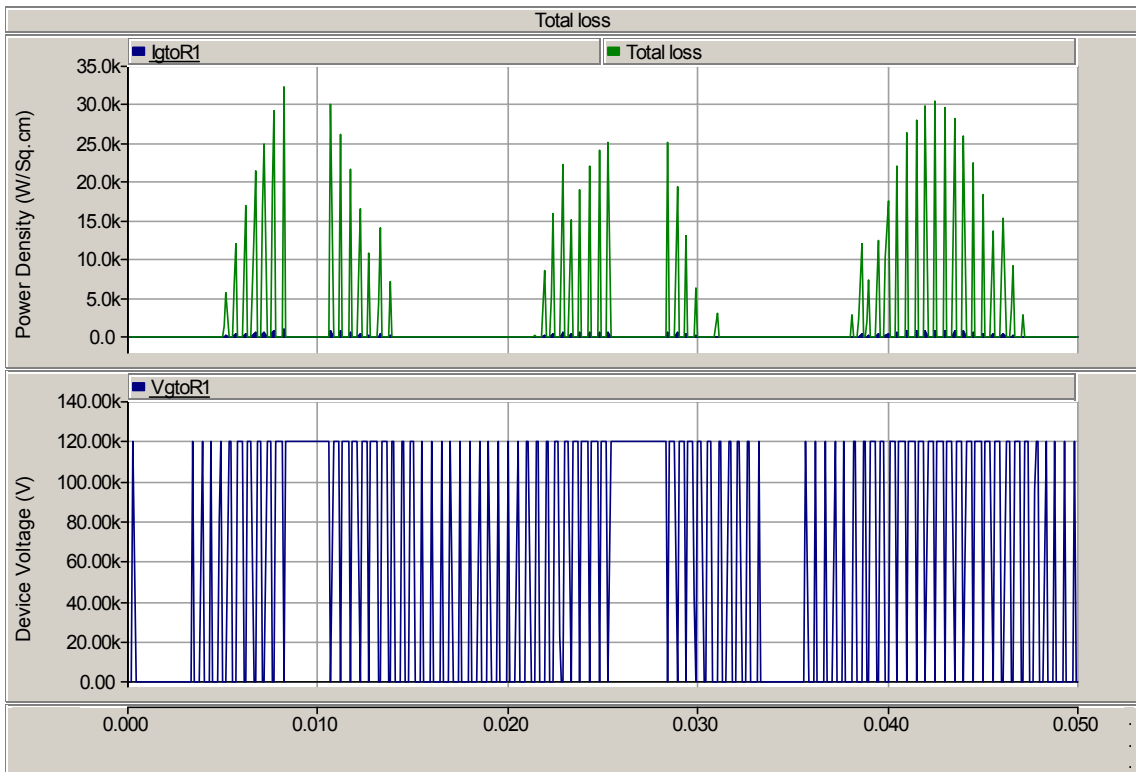
**Figure 4-15:** Voltage and current profiles from PSCAD/EMTDC (zoomed)



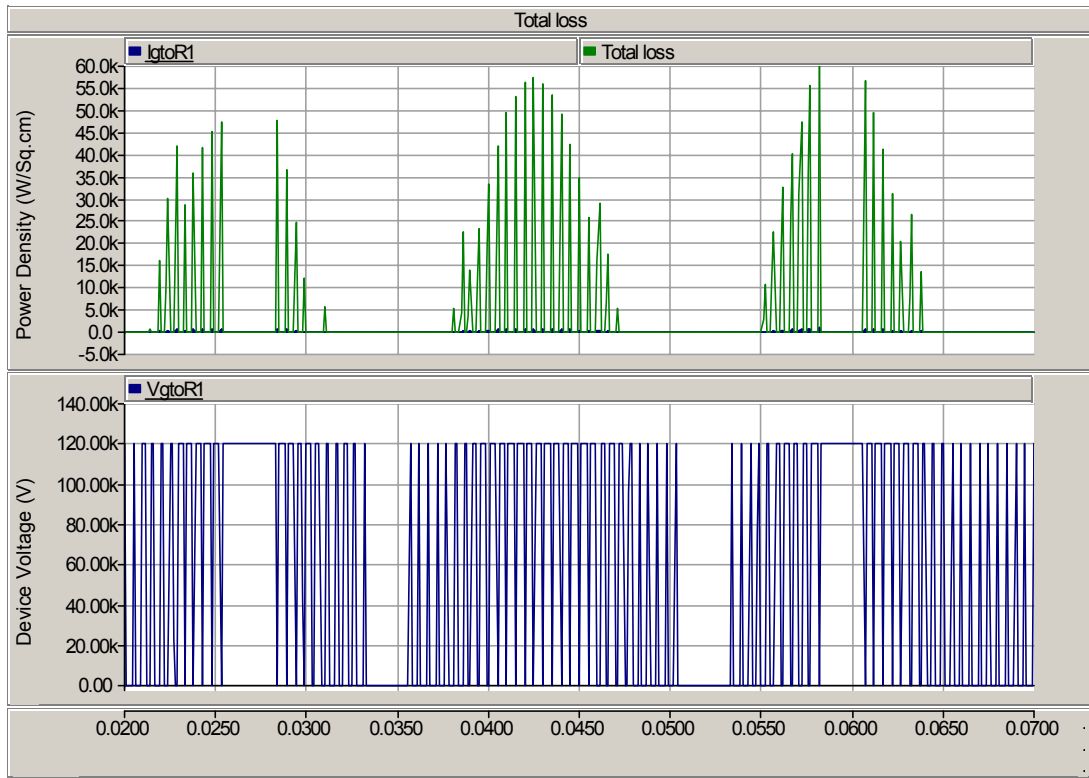
**Figure 4-16:** Loss profile and diode current for SiC GTO (373 K)



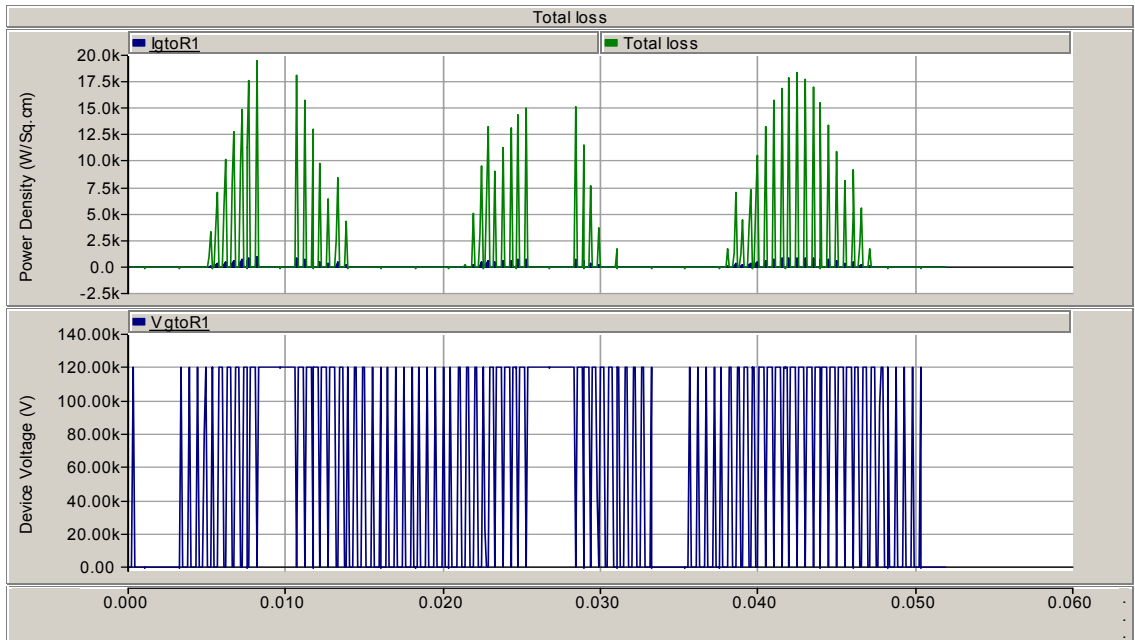
**Figure 4-17:** Loss profile for SiC GTO (300 K)



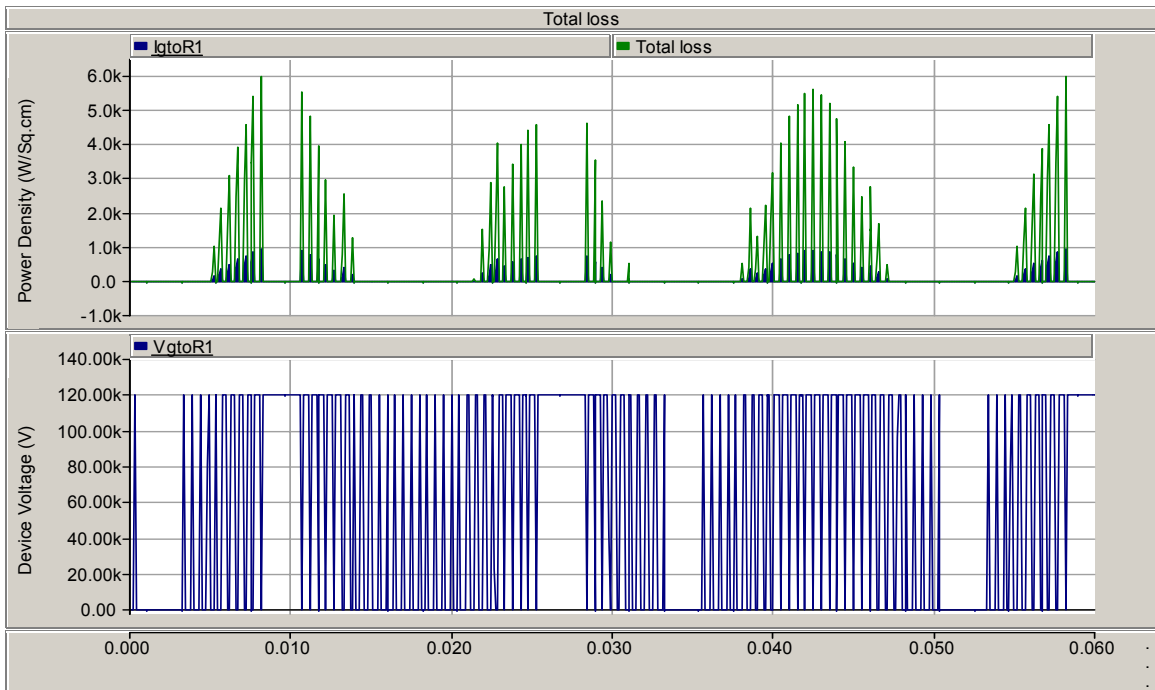
**Figure 4-18:** Loss profile for SiC GTO (423 K)



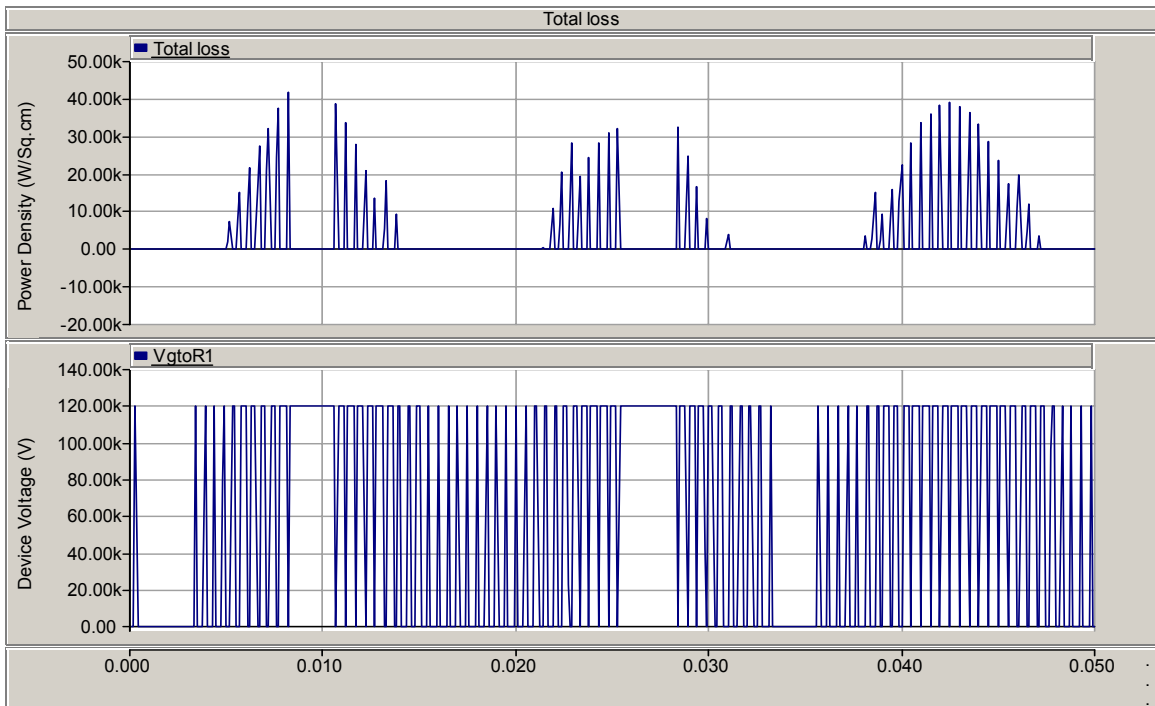
**Figure 4-19:** Loss profile for SiC GTO (473 K)



**Figure 4-20:** Loss profile for Si GTO (373 K)

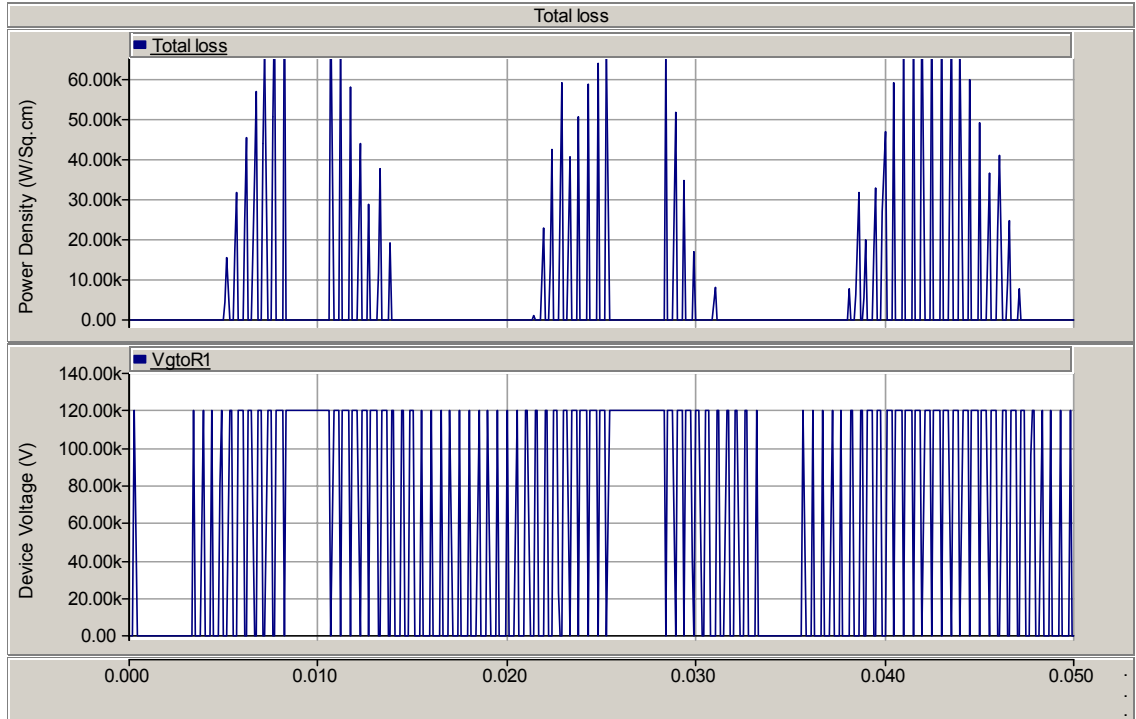


**Figure 4-21:** Loss profile for Si GTO (300 K)



**Figure 4-22:** Loss profile for Si GTO (423 K)





**Figure 4-23:** Loss profile for Si GTO (473K)

As shown in the graphs, the losses are a function of the conduction current and vary proportionally with the square of current. When the device is not conducting, it blocks the voltage across it and there is no loss in the device. The diode current is also shown in the graphs, and the current flows through the diode when there is power reversal and the current through the GTO is zero. The conduction losses are found dominant, similar to the device simulations discussed in the previous chapter. This is because, the switching frequency is low and thus the switching losses are less compared to conduction losses. However, for the same switching frequency, the losses are more for Si GTO than SiC GTO. The total loss of SiC GTO is less than Si GTO as expected, since the on-state resistance of silicon GTO is more than SiC GTO. The losses increase with

the increase in temperature due to increase in on-state resistance with temperature. However, the increase in loss, of Si GTO, is more than SiC GTO. These results are used to calculate the efficiency and system cost savings.

#### 4.5.1. Efficiency Calculation

The efficiency is calculated based on the power loss profile obtained for different operating conditions. It is the instantaneous loss as a function of the instantaneous current, which depends on the modulation index and the switching angles generated by the PWM. The average loss over few cycles of the fundamental is calculated to find the cyclic power loss (average power loss for each cycle of the output voltage). The plots of average power loss for Si GTO and SiC GTO are as shown in Figure 4-24 and Figure 4-25. The power loss is different for each cycle as the conduction current duty cycle varies. The maximum and minimum power loss for a single device over a few cycles is measured from the plots, and the corresponding converter controlled switches efficiency is calculated. The efficiency calculations are based on the dc power in the dc link, average loss in the devices, and the number of devices in the converter.

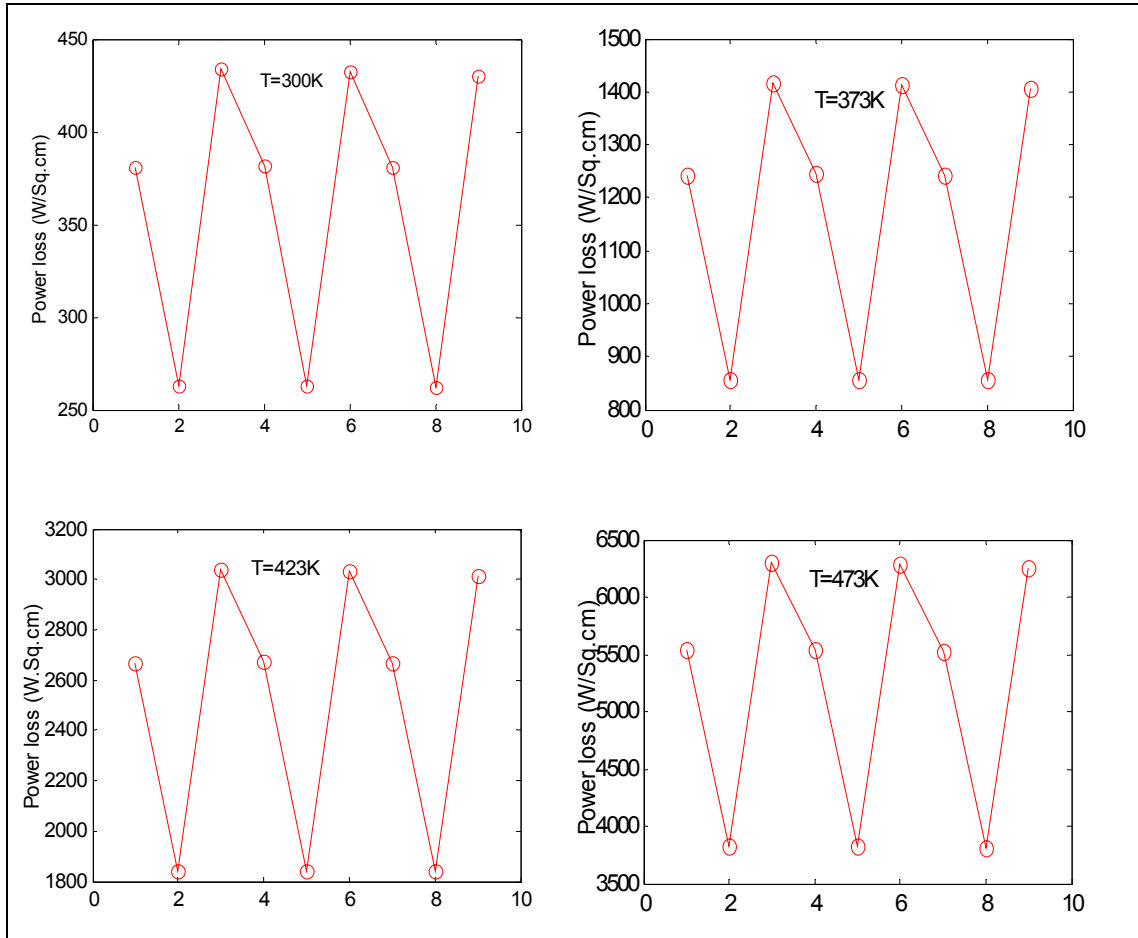
$$\text{Maximum efficiency} = (\text{dc power} - P_{\text{loss}(\text{min})})/\text{dc power}$$

$$P_{\text{loss}(\text{min})} = P_{\text{min}} \cdot (\text{no: of devices in the converter})$$

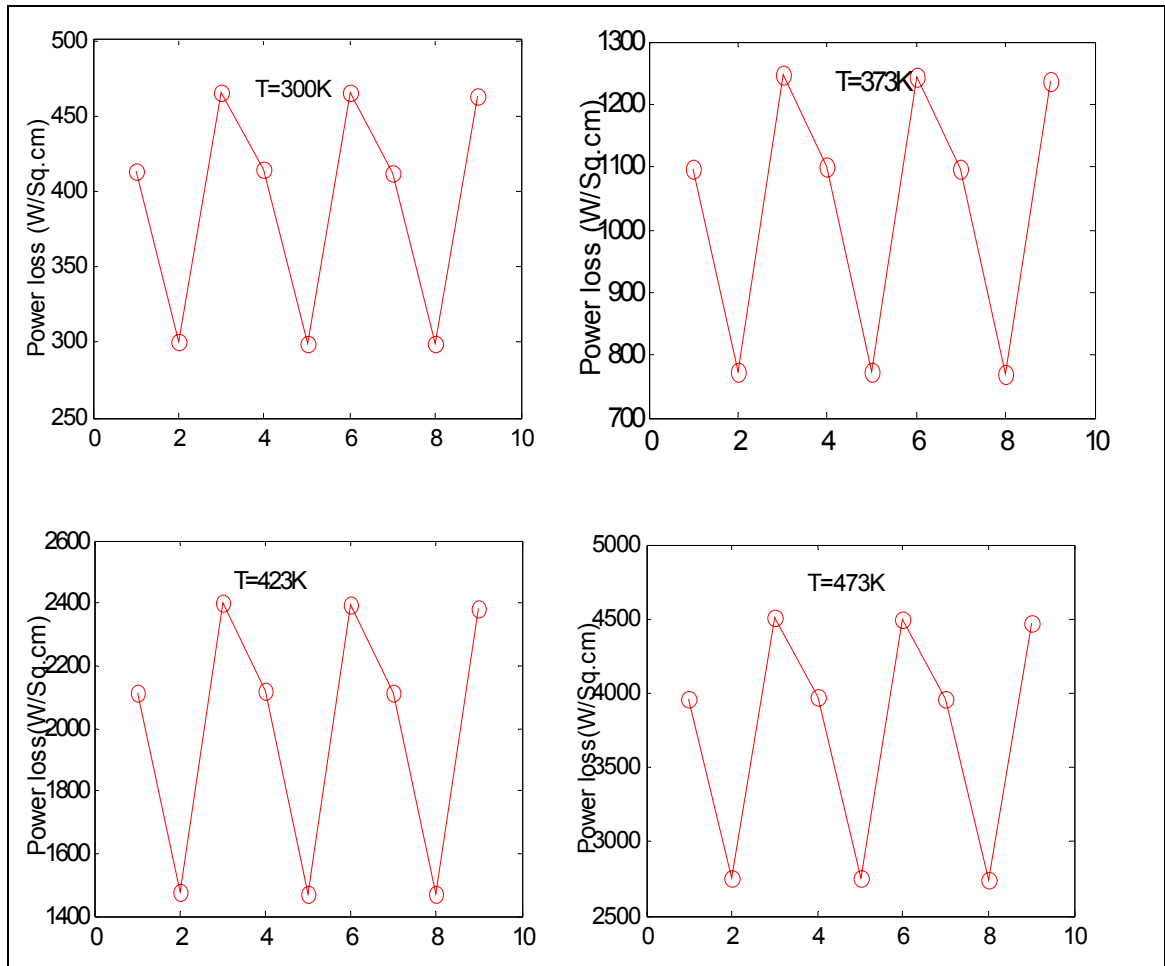
$$\text{Minimum efficiency} = (\text{dc power} - P_{\text{loss}(\text{max})})/\text{dc power}$$

$$P_{\text{loss}(\text{max})} = P_{\text{max}} \cdot (\text{no: of devices in the converter})$$

$$\text{No:of devices} = (\text{no:of devices for voltage sharing}) \cdot (\text{no:of devices for current dividing}) \cdot 6.$$



**Figure 4-24:** Cyclic power loss plots for Si 5kV, 200 A/cm<sup>2</sup> GTO



**Figure 4-25:** Cyclic power loss plots for SiC 20 kV, 200 A/cm<sup>2</sup> GTO

Tables 4.1 and 4.2 show the maximum and minimum efficiencies of Si GTO rated at 5kV, 200 A/cm<sup>2</sup> and SiC GTO rated at 20 kV, 200 A/cm<sup>2</sup>. Figure 4-26 shows the efficiency plot for Si GTO and SiC GTO converter's controlled switches. The range of efficiency for SiC converter is higher than Si converter, due to the lesser number of devices and also the average power loss per device is less for SiC GTO.

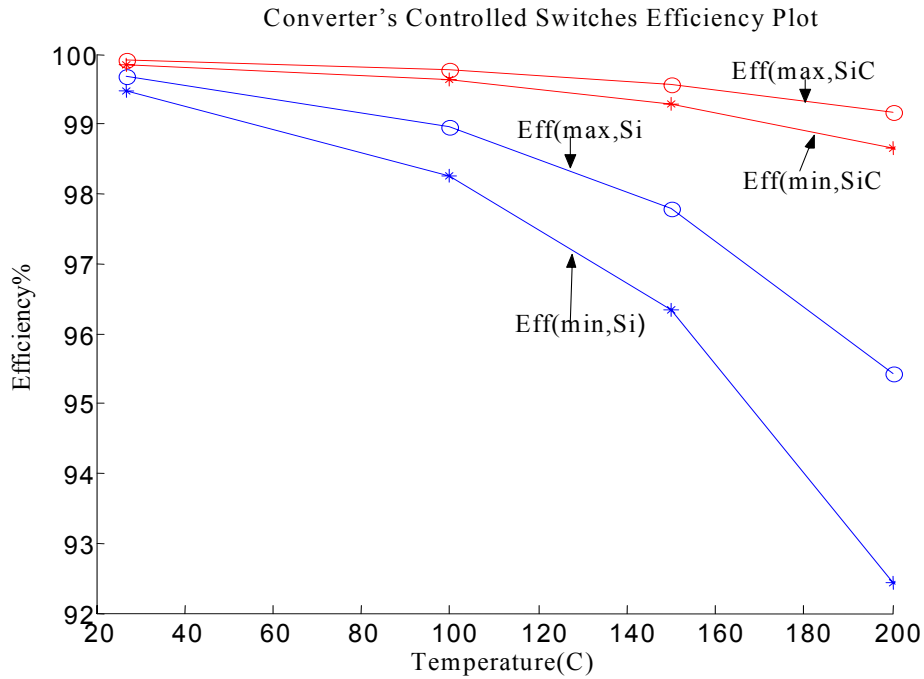
It can also be seen from the plot, that at 27°C, the efficiency is almost the same for the Si converter and SiC converter. However, at higher temperatures the efficiency of the Si converter's controlled switches drops down, but the efficiency of the SiC converter

**Table 4.1 Efficiency of Si GTO Converter's Controlled Switches**

Temp (K)	P <sub>max</sub>	P <sub>min</sub>	Max.eff %	Min.eff %
300	433.3	262.7	99.68	99.48
373	1443.1	873.7	98.75	98.26
423	3041.2	1842.4	97.78	96.35
473	6301.9	3818.9	95.41	92.43

**Table 4.2 Efficiency of SiC GTO Converter's Controlled Switches**

Temp (K)	P <sub>max</sub>	P <sub>min</sub>	Max.eff %	Min.eff %
300	475.2	300.6	99.9	99.85
373	1245.6	771.8	99.76	99.62
423	2402.1	1472.8	99.55	99.77
473	4506.9	2749.3	99.17	98.64

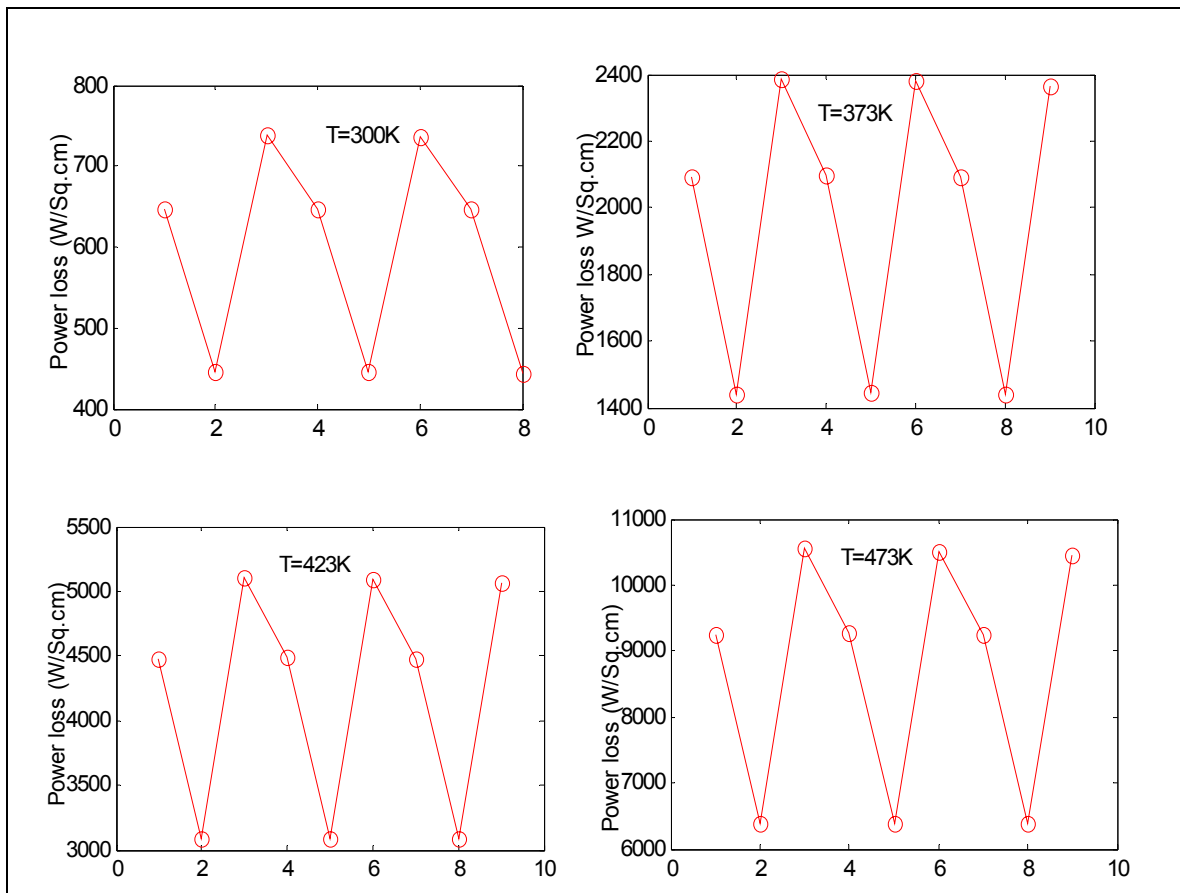


**Figure 4-26:** Converter's controlled switches efficiency plot

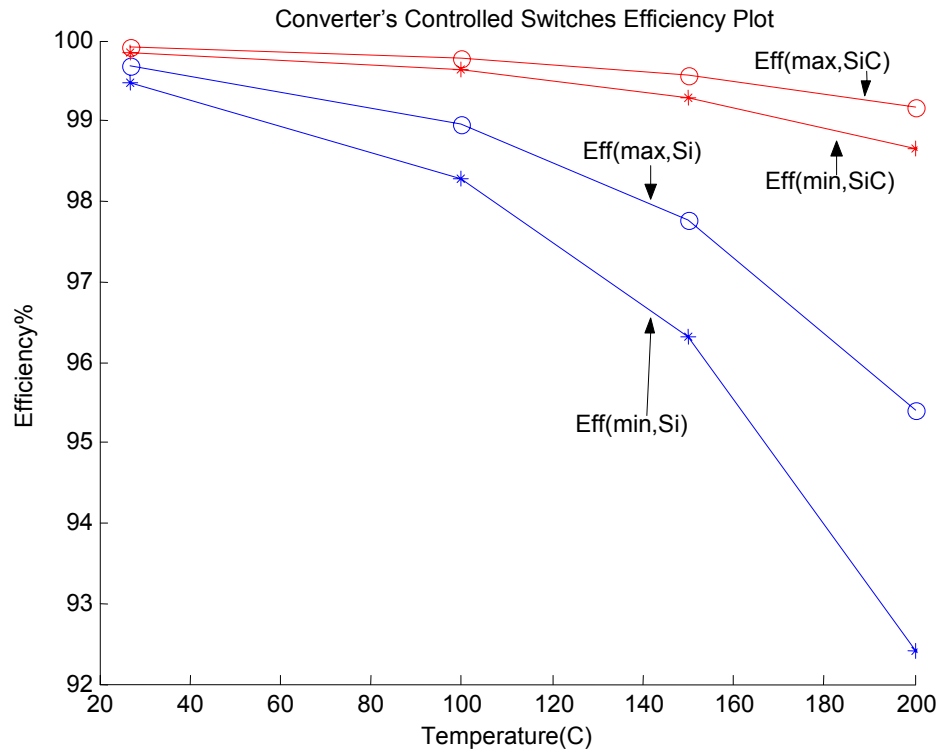
controlled switches is still high. This illustrates that SiC devices can operate efficiently at high temperature.

The rating of the Si GTO was changed to study the effect of reduction in number of devices on system performance. Figure. 4-27 shows the plots of average power for different temperatures. The average power loss per device is more than the Si device rated at  $400\text{A}/\text{cm}^2$ .

Figure 4-28 shows the efficiency plot for Si GTO and SiC GTO converter controlled switches, plotted from the values obtained for new rating of Si GTO. Table 4.3 shows the maximum and minimum efficiencies of Si GTO rated at  $5\text{kV}$ ,  $400\text{ A}/\text{cm}^2$ .



**Figure 4-27:** Cyclic power loss plots for Si 5kV, 400A/cm<sup>2</sup> GTO



**Figure 4-28:** Converter's controlled switches efficiency plot

**Table 4.3 Efficiency of SiC GTO Converter's Controlled Switches**

Temp (K)	$P_{max}$	$P_{min}$	Max.eff %	Min.eff %
300	737.6	445.1	99.67	99.46
373	2386.2	1442.8	98.96	98.28
423	5102.65	3088.3	97.77	96.32
473	10548	6388.4	95.4	92.43

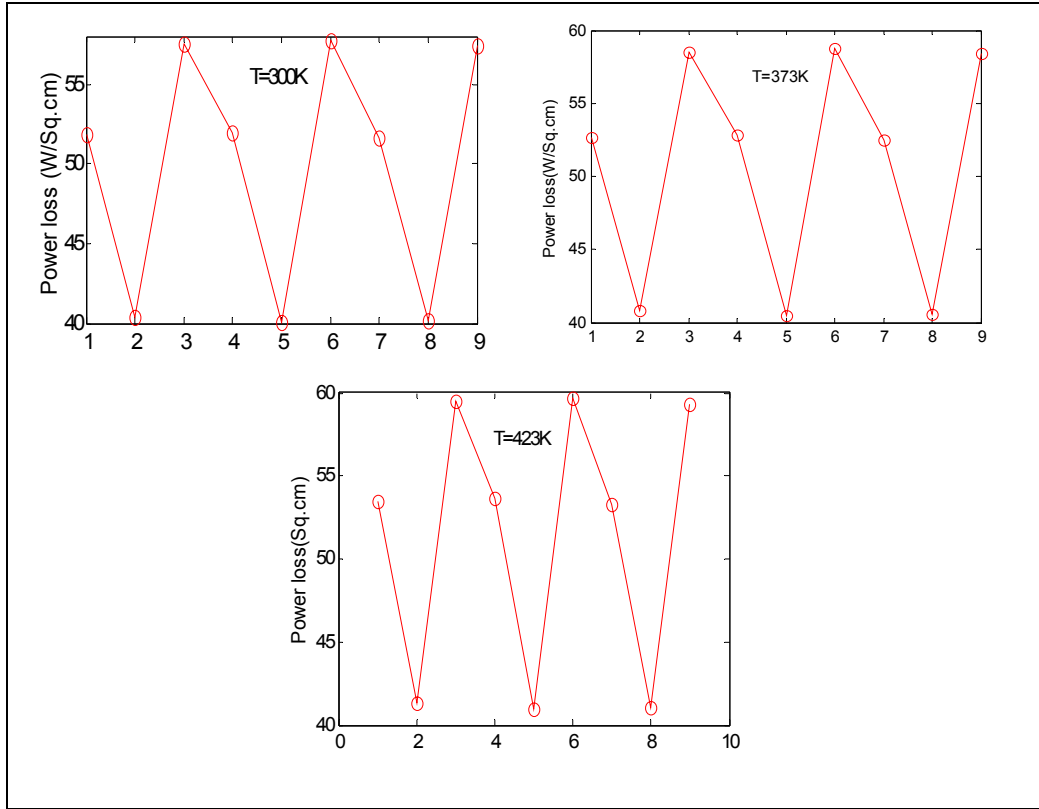


The range of efficiency for the Si converter is slightly higher but very insignificant compared to GTO rated at  $400\text{A}/\text{cm}^2$ . However, lesser number of devices has a substantial impact on the cost of the converter.

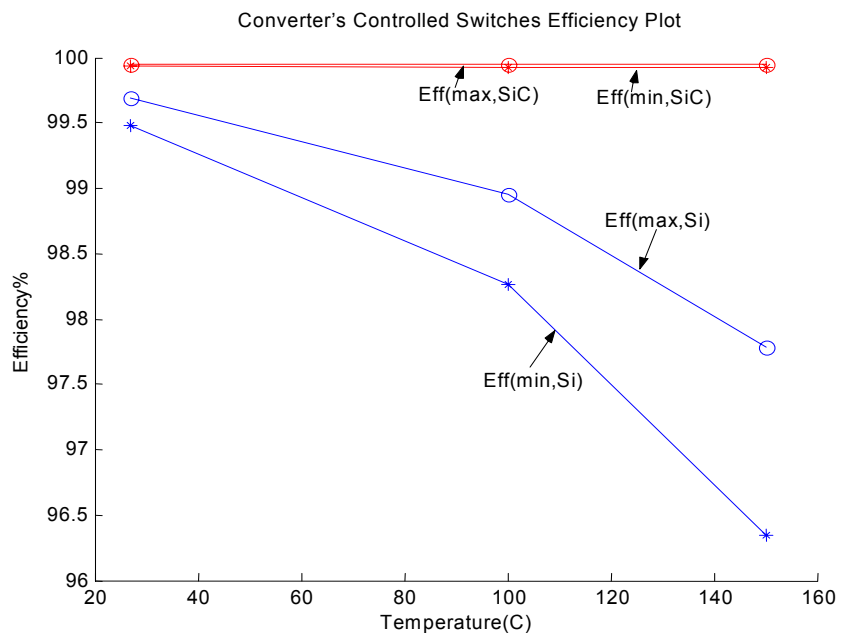
The voltage rating of the SiC GTO was changed to study the effect of one-to-one replacement of Si GTO with SiC GTO. The SiC GTO is rated at  $5\text{kV}$ ,  $200\text{A}/\text{cm}^2$ , so that the number of devices in the converter are equal. Figure 4-29 shows that the average power dissipated is much less than compared to  $20\text{ kV}$  SiC GTO. This reduction in power loss is because of the reduction in breakdown voltage corresponds to reduction in drift layer width. Hence, for a same diffusion length, the on-state losses are less. Figure 4-30 shows the efficiency plot for  $5\text{kV}$  SiC. Table 4.4 shows the efficiency calculation for  $5\text{kV}$  SiC GTO. Since the power losses are less, the converter's controlled switches efficiency of  $5\text{kV}$  SiC is higher. However, the increase in efficiency is marginal, and the key factor is the number of devices, which determines the installation and operating costs of a converter.

**Table 4.4 Efficiency of SiC GTO Converter's Controlled Switches**

Temp (K)	$P_{\max}$	$P_{\min}$	Max.eff %	Min.eff %
300	57.5	40.05	99.9519	99.93
373	58.5	40.5	99.9514	99.929
423	59.6	41.1	99.9507	99.928



**Figure 4-29:** Cyclic power loss plots for 5kV, 200A/cm<sup>2</sup> SiC GTO



**Figure 4-30:** Converter's controlled switches efficiency plot

### 4.5.2 System Cost

The system cost savings is calculated based on the power loss profile obtained for different operating conditions, similar to efficiency calculation. The cost savings was calculated for different ratings of the devices at 100°C.

Calculation:

Maximum savings

$$\text{Difference in losses, dl} = (P_{(\text{loss, Si})} \cdot (\text{no: of devices})) - (P_{(\text{loss, SiC})} \cdot (\text{no:of devices}))$$

The converter operates for 365 days and 24 hours

$$\text{Losses/year} = \text{dl} \cdot 365 \cdot 24$$

Assuming a rate of \$0.04/ kW·hr

$$\text{Savings} = (\text{losses/year}) \cdot (\$0.04)$$

Table 4.5 gives the maximum and minimum cost savings for a converter using a SiC-based converter with 20 kV, 200 A/cm<sup>2</sup> GTOs instead of 5 kV, 200 A/cm<sup>2</sup> Si GTOs.

**Table 4.5 SiC Converter’s Controlled Switches Cost Savings compared to Si-based Converter**

		dl	Losses/yr	(Losses/yr) · 0.04
	Max.savings	814.824 kW	7,137,858.24 kW	285,514.32 \$
Si 200 A/cm <sup>2</sup>				
	Min. savings	490.14 kW	4,293,626.4 kW	171,745.05 \$
	Max.savings	806.824 KW	7,066,082.3 kW	282,643.29 \$
Si 400 A/cm <sup>2</sup>				
	Min. savings	484.365	4,243,042.656	169,721.71 \$

As shown in Table 4.5, the system savings of converter's controlled switches with Si GTO rated at  $200 \text{ A/cm}^2$  is a little higher compared to  $400 \text{ A/cm}^2$  Si GTO converter controlled switches. However, the difference in savings is much less. So the advantage of lesser devices overrides the savings because, if the number of devices is less the auxiliary components required will be less and the overall system cost will be reduced. Also, the installation costs will be less and complexity of the system control is reduced to a great extent with the reduction in number of devices. It was also shown in the previous section that the efficiency of a converter with Si GTO rated at  $400 \text{ A/cm}^2$  is slightly higher. This illustrates that higher current and voltage rating of a device results in the better performance of the system.

### **Summary**

An HVDC transmission system model based on VSC transmission principle was discussed. The model was developed using PSCAD/EMTDC software and the SIMULINK device model was interfaced to study the effect of SiC and Si devices on the performance of the system. The model was simulated for different operating conditions, and the results obtained were used to calculate the converter efficiency and system cost savings for SiC GTO and Si GTO. It was shown that SiC GTO converter's controlled switches have a higher range of operating efficiency compared to Si GTO converter's controlled switches. The system cost savings was calculated based on the difference in loss, and it can be concluded that these savings can be used to pay more for SiC devices. The ratio of number of devices in a SiC converter compared to a Si converter is less because SiC GTOs have a higher voltage rating than their Si counterparts. Thus, the

reduction in number of devices results in cost savings, and hence one can afford to pay more for a SiC GTO.

## 5. Conclusion

The objective of this thesis was to compare the performance of SiC devices with Si devices for an utility application. The utility application chosen was HVDC transmission, and the choice of device was GTO thyristor. The silicon and silicon carbide GTO thyristors were modeled using SIMULINK. For a given operating voltage and current, the model behavior varies with temperature with the doping density fixed for a desired rating of the device. The model was studied for variation in temperature for different current and voltage ratings. The mobility and lifetime of the carriers were assumed to be constant. Analysis of the simulation plots revealed that the model dependency on the parameters such as voltage, current, and temperature is split between the conduction and switching loss models. The conduction model is a function of current and temperature, and the switching model is a function of voltage and temperature. Hence, for a change in the operating voltage of the device, there was an increase in the switching losses only and the conduction losses were the same. Introduction of a temperature dependent mobility model solved the problem. The effect of the temperature dependent mobility model was realized in the simulations, because the diffusion length, which is a function of lifetime, and mobility of electron and holes will vary with temperature, and hence, the conduction and switching losses also varied with temperature.

Conduction losses dominate because at lower switching frequency the switching losses are low, and the main power loss is a function of on-state resistance. Silicon GTO thyristor losses are more than the SiC conduction losses primarily because of the

difference in the on-state specific resistance. It was found that the conduction losses of silicon GTO thyristor are at least twice more than a comparable silicon carbide device. The turn-on and turn-off losses are increasing with increase in voltage and current. The switching losses of a silicon carbide GTO thyristor are at least 12 times less than the silicon device. This noticeable difference between the switching losses of silicon and silicon carbide devices is mainly because, for the same blocking voltage, thickness of the blocking layer in silicon device is more than the thickness of blocking layer in silicon carbide device. The reduction in the blocking layer thickness in silicon carbide devices is because of the high electric breakdown strength of silicon carbide material due to wide bandgap. Thus, the charge stored in the drift region is less, which results in faster switching. This difference in losses shows that SiC devices have high efficiency compared to silicon. The number of SiC devices per converter leg required is less, due to the higher voltage rating of the device.

A system model was developed using PSCAD and the EMTDC simulation tool. The device models were interfaced with the system model to study the comparison and analyze the impact of the device on the system performance. The Si GTO was rated at 5kV, 200 A/cm<sup>2</sup> and SiC GTO at 20kV, 200 A/cm<sup>2</sup>. The voltage and current profiles across a GTO, obtained from PSCAD, were used to calculate the losses. Losses of the Si GTO were found to be more than SiC GTO similar to the individual device simulation. The efficiencies of the converter's controlled switches were calculated based on the losses for different operating temperatures in the range of 27°C – 200°C. The range of efficiency for SiC GTO converter's controlled switches was higher than Si GTO converter's controlled switches. The system cost savings was also estimated using the

converter's controlled switches loss calculation. Since the losses in SiC converter are less, the operating cost of SiC converter is less and thereby results in system savings. These savings can be used to pay more for SiC devices. The ratio of number of devices in a SiC converter compared to a Si converter is less because SiC GTOs have a higher voltage rating than their Si counterparts. Thus, the reduction in number of devices results in cost savings, and hence one can afford to pay more for a SiC GTO.

Based on the results obtained, a few conclusions can be drawn. SiC devices can withstand high temperature, more than 150°C, and since the losses are also less, thermal management requirements, such as heat sink size, can be greatly reduced. Also, the device operating area (DOA) limits can be improved due to reduced losses, and hence, the maximum frequency can be increased for a given current density and operating voltage. Since the switching losses are less, the switching frequency of the device can be increased which results in improved dynamic characteristics of the system.

The use of VSC in high power transmission application is restricted mainly due to the high converter losses, which make the system highly inefficient. Even though advanced technologies like multilevel converters have been developed, the percentage increase in loss reduction is not high and results in increased complexity of the system. However, using SiC devices, overall losses can be reduced. Currently, system manufacturers face the challenge of reducing the operating cost of the system and hence demand devices with higher current and voltage rating. It was shown in the study that by using high rated SiC GTO the system savings are improved. Instead of several Si GTOs in series and parallel, fewer SiC devices can be employed for the same rating. Hence it



can be concluded that SiC devices close to commercialization can effectively replace the conventional Si based thyristor converters.

Even though SiC devices have been realized to have the potential to replace the existing Si devices in power applications, there are few issues to be resolved before SiC can be commercialized. The key issues include material defects like micropipes, ion implantation, SiO<sub>2</sub> interface, and cost of the material. Also, the increase in rating of auxiliary components and effective packaging techniques are important. Hence, the rate of commercialization depends on development of defect-less material and more importantly the cost of manufacture.

At present, however, the GTO ratings are much lower, and their cost and losses are higher compared to the thyristor. The three factors mentioned above can be greatly improved using SiC devices. It can be concluded that continued research and developments in power electronics and power semiconductor technology would provide exciting new configurations, and applications for HVDC converters.

## **6. Future Research Work**

The GTO thyristor loss model developed can be used to study different system applications like static var compensator (SVC), static synchronous compensator (STATCOM), or static synchronous series compensator (SSSC).

The focus of this thesis was on the main switches; the GTO thyristor and the results produced are based on the effect of these devices on the converter operation. However a diode loss model can be developed, and incorporated in the converter. Thus the impact of devices on the system can be studied with a complete converter.

A fault analysis can also be done on the system used in this thesis to study the dynamic response characteristics, which is one of the advantages of a VSC technology.

Also, a hybrid converter model with silicon and silicon carbide devices can be developed to study the cost savings compared to a total SiC device converter.

## References

- [1] D. A. Woodfrod, "HVDC Transmission," Manitoba Research Centre, March 1998.
- [2] J. Arillaga, *High Voltage Direct Current Transmission, 2<sup>nd</sup> edition, IEEE Power and Energy Series 29.*
- [3] [http://www.worldbank.org/html/fpd/em/transmission/technology\\_abb.pdf](http://www.worldbank.org/html/fpd/em/transmission/technology_abb.pdf)
- [4] E. Uhlmann, *Power Transmission by Direct Current*, 1975.
- [5] HVDC Transmission, WSCC Network Disturbances, session 3, pp. 1-29.
- [6] <http://www.ceramicmaterials.saint-gobain.com/products/basic.asp0>
- [7] W.J. Choyke, R. P. Devaty, "SiC- The Power Semiconductor for the 21st Century: A Materials Perspective," *Naval Research Reviews*, vol. 51, pp. 4-12, November 1999.
- [8] P. G. Neudeck, "SiC Technology," NASA Lewis Research Center, 1998
- [9] A. R. Powell, L. B. Rowland, "SiC Materials –Progress, Status, and Potential Roadblocks," *Proceedings of the IEEE*, vol. 90, no. 6, pp. 942-955, June 2002.
- [10] J. B. Fedison, "High Voltage Silicon Carbide Junction Rectifiers and GTO Thyristors," *Thesis Submitted to RPI New York*, May 2001
- [11] B. Ozpineci, "System Impact of Silicon Carbide Power Electronics on Hybrid Electric Vehicle Applications," *A Dissertation Presented to University of Tennessee, Knoxville*, August 2002.
- [12] M. Roschke, Frank Schwierz, "Electron Mobility Models for 4H, 6H, 3C SiC," *IEEE Transactions On Device Letters*, vol. 48, No. 7, pp. 1442-1447, July 2001.
- [13] [http://www.ecn.purdue.edu/WBG/Data\\_Bank/Best\\_Performance.html](http://www.ecn.purdue.edu/WBG/Data_Bank/Best_Performance.html)
- [14] Y. Sugawara, D. Takayama, K. Asano, R. Singh, J. Palmour, and T. Hayashi, "12-19kV 4H-SiC pin diodes with low power loss," *Proceedings of the IEEE International Symposium on Power Semiconductor Devices & Ics*, pp. 27-30, 2001.

- [15] M. Shanbag, T.P. Chow, M.S. Adler, "Reliability testing of SiC high voltage power devices," Proceedings of Center for Power Electronic Systems (CPES) Annual Seminar, pp. 487-490, 2001.
- [16] A. Elasser, T. P. Chow, "Silicon carbide benefits and advantages for power electronic Circuits and Systems," *Proceedings of the IEEE*, vol. 90, no. 6, pp. 969-985, June 2002.
- [17] N.Mohan, T.M. Undeland, and W.P. Robbins, *Power Electronics*, Second Edition, John Wiley & Sons Inc., New York, 1995.
- [18] *Feature And Application Of Gate Turn-off Thyristors*, Mitsubishi High Power Semiconductors.
- [19] Alex Q. Huang, Bo Zhang, " Comparing SiC Switching Power Devices: MOSFET, NPN Transistor and GTO thyristor," *Solid State Electronics*, 44, pp.325-340, 2000.
- [20] A.K.Agarwal, Jeffrey B. Casady, L.B. Rowland, S. Seshadri, R. R. Sierej, W. F. Valek, and C D. Brandt, "700-V Asymmetrical 4H-SiC Gate Turn-Off Thyristors," *IEEE Electron Device Letters*, vol. 18, no. 11, pp.518-520, November 1997.
- [21] Hiroshi Sakata, Muhamad Zahim, " Device Simulation of SiC-GTO," *IEEE*, pp. 220-225, 2002.
- [22] M.Bhatnagar, B. J. Baliga, " Comparison of 6H-SiC, 3c-SiC, and Si for power devices," *IEEE Transactions on Electron Devices*, vol. 40, no. 3, pp. 645-655, March 1993.
- [23] C.E. Weitzel, "Wide Bandgap Semiconductor Electronics," *Electron Devices Meeting, 1998. IEDM '98 Technical Digest, International*, pp. 51-54, Dec 1998.

- [24] <http://encon.fke.utm.my/notes/MSc%20notes-introduction-2002.pdf>
- [25] L. Xu, "VSC Transmission," Alstom, December 2001.
- [26] F. Schettler, H.Huang, N.Christl, " HVDC Trnasmission Systems Using Voltage Sourced Converters- Design and Application," *Power Engineering Society Summer Meeting, 2000. IEEE*, vol. 2 ,pp. 715 –720, July 2000.
- [27] R. Chokhawala, "Power Semiconductors in Transmission and Distribution Applications," *Proc. of the 2001 International Symposium on power Semiconductor Devices & ICs (ISPSD)*.

## **Vita**

Madhu Sudhan Chinthavali is a citizen of India and was born in 1979. He received his bachelor's degree in the year 1996 from Bharathidasan University, India. He was a co-author for two publications. His areas of interest are semiconductor power devices for power applications and digital VLSI.