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A Class-E Inductive Powering Link with Backward Data Communications for Implantable Sensor Systems

Mohammad Ahsanul Adeb
University of Tennessee - Knoxville

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To the Graduate Council:

I am submitting herewith a thesis written by Mohammad Ahsanul Adeeb entitled "A Class-E Inductive Powering Link with Backward Data Communications for Implantable Sensor Systems." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Syed K. Islam, Major Professor

We have read this thesis and recommend its acceptance:

Donald W. Bouldin, M. Nance Ericson, Jayne Wu

Accepted for the Council:

Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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Jayne Wu

Accepted for the Council:

Anne Mayhew
Vice Chancellor and
Dean of Graduate Studies

(Original signatures are on file with official student records.)

A Class-E Inductive Powering Link with Backward Data Communications for Implantable Sensor Systems

A Thesis
Presented for the
Master of Science
Degree

The University of Tennessee, Knoxville

Mohammad Ahsanul Adeeb
August 2006

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Abstract

The design and implementation of a wireless power and data transfer system based on inductive coupling, having the potential to be used in numerous implantable bio-medical sensors and systems, is presented. The system consists of an external (primary) unit and an internal (secondary) unit. The external unit incorporates a high-efficiency switch-mode Class-E amplifier operating at ~200 kHz for driving the primary coil. The secondary unit consists of a parallel resonant coil followed by the power recovery circuitry. Means for backward data communication from the internal to the external unit over the same pair of coils has been realized using a simple FSK-based modulation scheme incorporated into the internal unit. FSK demodulation and associated filtering are integrated with the base inductive powering system. Prototype system test results indicate the inductive link efficiency can exceed 80% under optimum operating conditions with the overall power transfer efficiency of approximately 30%. The communication system is capable of transmitting up to 10kbps of data with the FSK carrier frequency (i.e., middle-frequency) being only 120kHz. The complete system functions reliably over an inter-coil distances exceeding 2.5cm with a 5V dc supply.

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CHAPTER 1

Introduction

This thesis summarizes the design and testing of a system enabling external powering and data communication with implanted biomedical sensor systems. In this chapter an introduction of the work is presented with an emphasis on the motivation for the work, and the design goals and requirements. The primary design tradeoffs and considerations most relevant to practical implementation for use with implanted applications are discussed. A top-level view of the proposed system is presented. Finally, an overview of the organization of the thesis is provided.

1.1 The Implantable Perfusion Sensor System

A photonics-based sensor system that is well suited for real-time, continuous monitoring of organ perfusion following transplantation surgery has been developed and reported by Ericson *et al.* [1]. This newly developed sensor technology is suitable for miniaturization, and can be implanted for monitoring and assessment of regional tissue perfusion. Although the primary intended application of this minimally-invasive technique is blood flow monitoring following liver transplantation, many additional applications are possible as organ and tissue transplant procedures are becoming increasingly successful.

The perfusion sensing technique under discussion makes use of absorption spectroscopy for assessing microcirculation in tissue. The method is based on the varying absorption of visible and near-IR light by oxygenated and non-oxygenated hemoglobin in the blood [2].

The implantable perfusion sensor system developed in [1] uses light sources of three different wavelengths (660nm, 805nm and 940nm). Two wavelengths (660nm and 940nm) have been commonly employed in pulse oximetry, a similar technique that non-invasively determines the systemic oxygen saturation. These two wavelengths can be used to discriminate between oxygenated and non-oxygenated hemoglobin from the difference in absorption in them. The third wavelength was included for improving motion artifact rejection, a common problem in optical-based bio-sensing.

A conceptual view of the optical perfusion sensing technique is illustrated in Figure 1.1. As shown in this figure, the three co-mounted LED light sources were integrated into a single package with a lens, and used to illuminate the tissue. The reflected light was detected by a photodetector, and through appropriate processing of the received signal a measure of the relative tissue perfusion parameters and oxygen saturation was achieved.

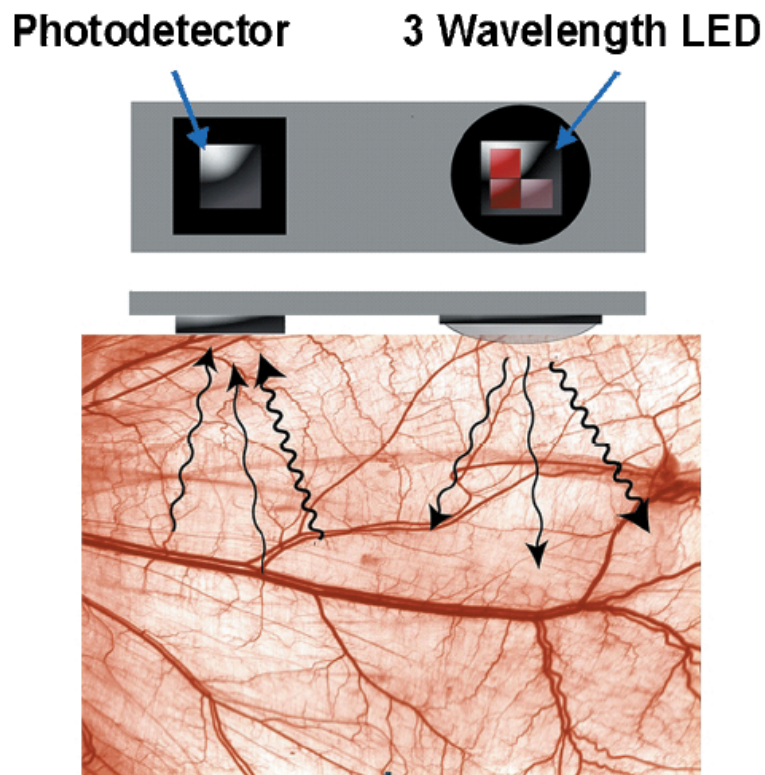


Figure 1.1 Photonics-based perfusion measurement technique [1]

The implant electronics for the perfusion monitoring system consists of several functional units – sensor interface electronics, a system controller, an LED driver, and the RF transmitter. A number of prototypes of the implanted system were fabricated and tested in different environments. One prototype of the implanted system and the optical sensor were sufficiently miniaturized and successfully tested in a laboratory environment (see Figure 1.2).

Multiple *in vitro* experiments using artificial blood perfusion model and a preliminary *in vivo* experiment using a porcine model demonstrated reasonable correlation between the measured data through this technique and that using a conventional standard clinical method.

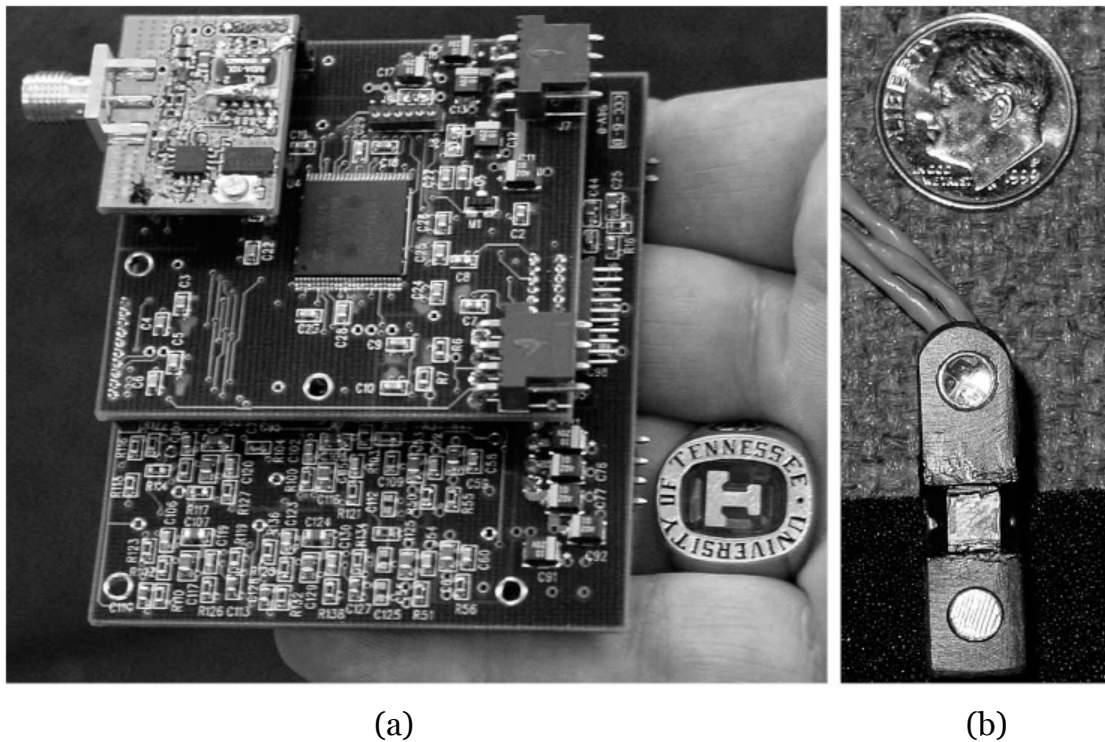


Figure 1.2 (a) Prototype implant system, (b) 3-wavelength optical sensor [1]

1.2 Implant System Powering and Communication Requirements

The implantable sensor system for blood flow monitoring described in the previous section was developed and tested by a joint collaboration between the Oak Ridge National Laboratory (TN, USA), the University of Pittsburgh (PA, USA) and Texas A&M University. As with any implantable system, this design faces two major challenges for practical and successful system application:

- A means for supplying electrical power to the implanted unit that is non-invasive, reliable, long lasting, efficient, miniaturized and inexpensive.
- A means for data communication between the implanted unit and an external unit that is robust, reliable and provides sensor data in real time.

Methods for powering implantable systems consists of tethered power cables, implanted batteries, inductive powering, and combinations of the later two methods. Tethered power cables (percutaneous plugs) have been employed in some clinical implantable applications, but they suffer from some serious drawbacks [3], such as,

- Creation of potential path for infection as they break the skin
- Physical safety risks to the patient and implant (tether pulling and implant dislocation and associated tissue damage).

These problems become increasingly serious as the period of implantation increases.

The use of integrated batteries is a popular implant powering method, but also has some associated limitations:

- Limited power density: Some applications require more ampere-hours than an implantable battery can provide, which necessitates frequent reimplantation or recharging of the battery.

- High Mass: Batteries can be considerably large and heavy, and usually account for a significant portion of the implant mass.
- Leakage: Though unlikely, hermetically sealed batteries may leak, causing hazard to body tissue.

Similarly, a wired data communication system is also not a feasible choice for the implantable systems for the reasons mentioned above.

A properly designed inductive link offers a very attractive solution for wireless powering and data communication of many implantable biomedical systems, by mitigating many of the problems associated with alternative powering methods.

1.3 Inductive Link: A Viable Solution

1.3.1 Advantages of Inductive Links

Inductive links, also known as RF links, are becoming increasingly popular as a means for providing power and data to and from state-of-the-art ‘smart’ implantable units. An inductive link-based powering and communication system offers the following benefits:

- Eliminates external cables, thus reducing the risk of infection, tether and implant dislocation, and associated patient discomfort;
- No periodic surgical maintenance is needed to replace or recharge batteries;
- Provides a durable and non-corrosive powering and communications method, thus increasing the implant robustness;
- Is suitable for long-term use;
- Sufficient miniaturization is possible.

- Power and data (unidirectional or bidirectional) can be transferred simultaneously or by time division multiplexing depending on the architecture used.

1.3.2 Basic Link Concepts

An inductive link is formed by a loosely coupled transformer consisting of a pair of coils that are usually placed in a coaxial arrangement. The external or primary coil is excited by an alternating current, and thus an electromagnetic field is produced with magnitude dependant on the dimensions of the coil, the drive current and the frequency of operation. A portion of the alternating flux lines generated this way link to the internal or secondary coil's turns, and the change in flux linkage produces a voltage in the secondary coil, which is proportional to the rate of flux change and the number of turns in the secondary coil (Faraday's Law of Electromagnetic Induction).

The induced voltage is then properly conditioned to suit the needs of the implant's signal processing circuitry and other electronics. The size and number of turns of each of the transformer coils are chosen based on the power requirements of the implantable unit and the geometric and physiological constraints associated with the particular application. Based on the required location the implanted system, the internal coil diameter can range from a few millimeters to several centimeters.

The implanted unit also consists of a data transmitter, receiver, or transceiver module depending on the nature of the implantable system's functionality. Usually a *forward* data link (data transmitted from the outside world to the implant) is established for microstimulators, while a *reverse* data link (data transmitted from the implant to the outside world) is necessary for sensing and

monitoring systems. In some cases, a bidirectional data link can be implemented as well.

The external RF unit consists of the power transmitter that provides the necessary current drive to the primary coil, and the configuration-dependant external half of the communication system (transmitter, receiver, or transceiver).

The simplified block diagram of a typical biomedical implant system involving an inductive power and data link has been illustrated in Figure 1.3.

1.3.3 Biocompatibility and Tissue Absorption Issues

A biocompatible coating and hermetic sealing is necessary for systems implanted inside the human body in order to minimize the immune response to the implanted device and to avoid possible contamination or safety hazards to the body tissue. Furthermore, standard electronics materials and packaging methods do not provide adequate protection against the harsh environment they face inside the body. A reliable hermetic seal helps protect the implanted electronics against the chemical aggression of body fluids.

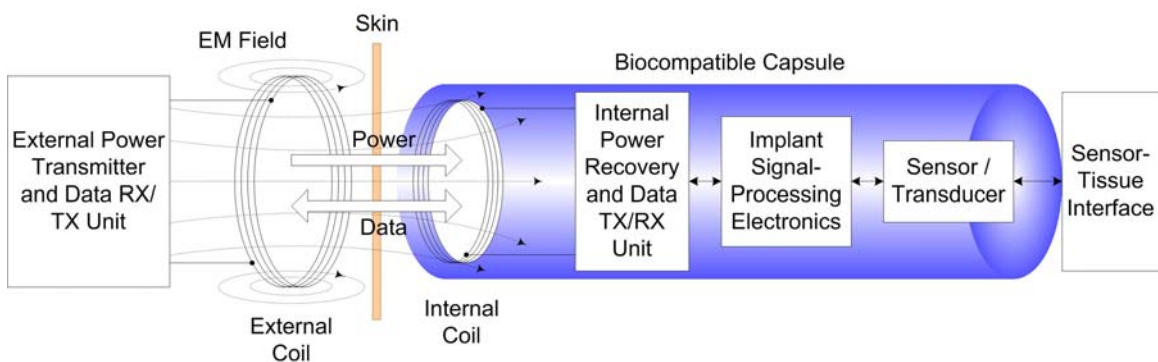


Figure 1.3 Schematic overview of a typical implant system using an inductive link

Several biocompatible encapsulation techniques and/or hermetically sealed packages have been reported in the literature, some of which includes:

- A ceramic hermetic package, where the power recovery and signal processing circuitry are placed on a thin film printed circuit over the package base [4]. The secondary coil may be placed inside the ceramic package or in a separate place under the skin.
- A glass capsule, which can be hermetically packaged using a technique based on glass-to-silicon electrostatic bonding [5, 6].
- Encapsulation by polymers or silicone-based materials [7].
- Encapsulation using two layers (particularly suitable for microstimulators, [8]). The circuitry is fabricated in a thick-film microelectronic form, and then mounted inside a hermetically sealed grade-II titanium capsule with multiple feedthroughs. After the circuit is connected to the feedthroughs, the lid is welded on. Finally, the whole assembly is encapsulated in a medical grade epoxy; however, the lid of the titanium capsule is left exposed and is used as the anodic reference electrode for monopolar stimulation. A Silicone elastomer strain relief for the leads is also provided. The packaging system has demonstrated suitability for long-term implantation in humans. [8]
- Encapsulation and insulation by laser welding a metal lid on the top of the specially constructed orthopedic cavity, where the strain sensor, its interface circuit and the RF data transmitter are housed together inside the implant cavity. The metal lid is provided with a biocompatible, ceramic, radio-transparent window for efficient data transmissions, because the antenna/internal coil is included inside the cavity. Laser welding of the stainless steel parts is performed under the inert argon atmosphere to guarantee a fully hermetic seal and corrosion free welds. Long-term reliability has been demonstrated using this technique [9, 10].

In addition to the materials biocompatibility issues, considerations must be given to the safe limits of exposure of the human body to electromagnetic radiation, while designing and implementing an inductive link-based implant system.

Safety considerations with respect to electromagnetic radiation require that the absorption of RF energy in body tissue be limited. It is known that tissue absorption varies approximately as the square of the frequency in the range of 1-100MHz [11]. Therefore, for a given energy density within the near field of the link coils and for a specified maximum allowable power absorption by the tissue, there is a frequency above which the power absorbed by tissue will be excessive. In fact, a higher power consumption device not only increases tissue temperature through power dissipation in the form of heat, but also implies higher electromagnetic field density in tissues, particularly in the RF 'hot spot' of the body (near field region of the coils), in the effort of transcutaneous powering of an implant system [12]. The following tables adapted from IEEE Standard C95.1 (1999 Edition) provide the necessary guidelines for determining the safe operating conditions/exposure limits for a given operating frequency. Adhering to these recommendations is very important in the design and development of an inductive powering and data communication system.

According to the IEEE Standard in discussion, exposure associated with an uncontrolled environment is the exposure of individuals who have no knowledge or control of their exposure. The exposure may occur in living quarters or workplaces where there are no expectations that the exposure levels may exceed those shown in Table 1.1, and where the induced currents do not exceed those in Table 1.1, Part B. However, it has been also mentioned in the standard that induced current measurements are not required if the spatially averaged electric field strength does not exceed the MPE at frequencies of 0.20 MHz or less.

Table 1.1 Maximum Permissible Exposure (MPE) for Uncontrolled Environments [13]

Part A: Electromagnetic Fields [†]					
Frequency range (MHz)	Electric field strength (E) (V/m)	Magnetic field strength (H) (A/m)	Power density (S) E-field, H-field (mW/cm ²)	Averaging time E ² , S or H ² (min)	
1	2	3	4	5	
0.003–0.1	614	163	(100, 1 000 000) [‡]	6	6
0.1–1.34	614	16.3 / <i>f</i>	(100, 10 000 / <i>f</i> ²) [‡]	6	6
1.34–3.0	823.8 / <i>f</i>	16.3 / <i>f</i>	(180 / <i>f</i> ² , 10 000 / <i>f</i> ²)	<i>f</i> ² / 0.3	6
3.0–30	823.8 / <i>f</i>	16.3 / <i>f</i>	(180 / <i>f</i> ² , 10 000 / <i>f</i> ²)	30	6
30–100	27.5	158.3 / <i>f</i> ^{1.668}	(0.2, 940 000 / <i>f</i> ^{3.336})	30	0.0636 <i>f</i> ^{1.337}
100–300	27.5	0.0729	0.2	30	30
300–3000	—	—	<i>f</i> / 1500	30	
3000–15 000	—	—	<i>f</i> / 1500	90 000 / <i>f</i>	
15 000–300 000			10	616 000 / <i>f</i> ^{1.2}	

NOTE—*f* is the frequency in MHz.

†The exposure values in terms of electric and magnetic field strengths are the mean values obtained by spatially averaging the squares of the fields over an area equivalent to the vertical cross section of the human body (projected area).

‡These plane-wave equivalent power density values, although not appropriate for near-field conditions, are commonly used as a convenient comparison with MPEs at higher frequencies and are displayed on some instruments in use.

Part B: Induced and contact radio frequency currents [*]			
Frequency range (MHz)	Maximum current (mA)		Contact
	Through both feet	Through each foot	
0.003–0.1	900 <i>f</i>	450 <i>f</i>	450 <i>f</i>
0.1–100	90	45	45

NOTE—*f* is the frequency in MHz.

*It should be noted that the current limits given above may not adequately protect against startle reactions and burns caused by transient discharges when contacting an energized object.

1.3.4 Inductive Link Applications

The clinical applications employing inductive powering and/or data communication fall in two major categories, and some of them, which have been recently investigated and have seen some success in practical implementation are mentioned here:

Implantable Sensing and Monitoring Systems:

- Detection and monitoring of hip prosthesis loosening [14]
- Cortical monitoring devices for simultaneous recording of large groups of cells located in specific areas of the cortex [12]
- Exploration of the brain and its physiological functions [19, 20]
- Peripheral neural recording system for understanding the organization and operation of individual neurons and signal processing techniques of biological neural networks [23]
- Dynamic measurement of implant strain and stress acting upon massive orthopedic implants [9, 24]

Implantable Microstimulator Systems:

- Neural stimulators (or cochlear implants) for auditory prosthesis of profoundly deaf persons [3, 17]
- Intracortical visual prosthesis (or visual cortical stimulator) for profoundly blind people [4, 12, 16]
- Bladder controllers for urine voiding and to prevent incontinence [12, 25]
- Pacemakers and defibrillators for combating cardiac irregularities [15]
- Brain stimulators for the treatment of obsessive-compulsive disorder and major depression [18]

- Neurostimulation for the treatment of degenerative disorders of the retina [21, 22]
- Multichannel neural stimulators for functional electrical stimulation (FES) to restore muscular control in disabled patients [7]
- Advanced functional neuromuscular stimulation (FNS) for patients with spinal cord and other nervous system injuries [8]

In addition to these biomedical devices, other fields of application can benefit from the use of power and data communication via inductive links, especially where the use of batteries is not desirable due to size, cost and lifetime requirements. Some example applications include radio-frequency identification (RFID), contactless smartcards, and wireless micro-electro-mechanical systems (MEMS) [26-29]. In addition to purely inductive-powered systems, some implant systems may benefit from a hybrid approach where an inductive link is used for battery recharging. High-power inductive links can find potential applications in micro-motors, high bandwidth data transmitters and other industrial and automotive systems.

1.3.5 Inductive Link Drawbacks

Despite many attractive features and applicability in many fields, inductive links suffer from some difficulties. The major limitations of a typical inductive link are:

- (i) considerably low power-transfer efficiency,
- (ii) mostly suited for narrowband applications,
- (iii) sensitivity to misalignments of the coils and coil spacing.

The maximum achieved efficiency for transdermal power transfer to biomedical implants, as reported by Djemouai and Sawan [30], is below 20%, and it could be as low as 0.25% [14] or even lower. However, higher efficiencies were reported in

some recent publications, for example, 28% in [4]. The low power transfer efficiencies associated with the inductive links are mostly due to poor coupling between the coils. The coupling coefficient between the transmitter and receiver coil of the link, which is a function of coil dimensions and relative position of the coils, plays a major role in determining the overall efficiency of power transfer. Since many biomedical applications impose rigid constraints on the size and spacing of the coils, a low power-transfer efficiency is quite obvious. Many system characteristics contribute to the overall efficiency of the power transfer link, such as the coupling factor, number of turns of the coils, frequency of operation, primary coil drive technique (power amplifier topology), and unloaded Q s of the reactive components.

Almost every inductive link reported to date works with a double-tuned resonant circuit, i.e., a combination of series/parallel resonance is used both in the primary (external) and secondary (internal) units. A resonant circuit basically acts like a bandpass filter, and therefore, an inductive link is typically a narrowband system. However, some wide-band links have been reported [3, 31].

The gain of an inductive link is a strong function of the spacing between the coils, and it is affected significantly by misalignments. For a small increase in spacing (in the near field), the coupling drops drastically, and hence the gain is also reduced.

Several efficiency and bandwidth enhancement techniques and gain desensitizing strategies were reported in the literature, and some of them will be explored in Chapter 2.

1.4 Scope of the Thesis

The purpose of this work is to design and develop a system prototype of an inductive powering and data communication link that –

- is capable of delivering at least 125mW of power at a 5V supply voltage to an implantable system with appreciable overall power transfer efficiency,
- is driven by an efficient, Class-E type, switching power amplifier (or driver),
- can reliably communicate digital data backward (i.e., from the implanted system to the outside world),
- operates at a frequency low enough to minimize the exposure of body tissue to electromagnetic fields and high enough to provide a good data rate to carrier frequency ratio,
- is sufficiently miniaturized so that it can be easily interfaced with an implant system's signal processing electronics.

The target application for this inductive powering and reverse telemetry link is an implantable perfusion sensor system that has been briefly described in section 1.1 (prototype shown in Figure 1.2.). The specific application to liver perfusion monitoring requires a high power transfer due to required optical power levels for successful measurements in optically-dense liver tissue. However, implantation into the human torso provides ample space allowing a larger implant unit than practical in many other applications. Adaptation of this unit to applications requiring less power transfer should be possible and will result in decreased implementation size.

The system components that are designed and implemented in this work are shown in Figure 1.4.

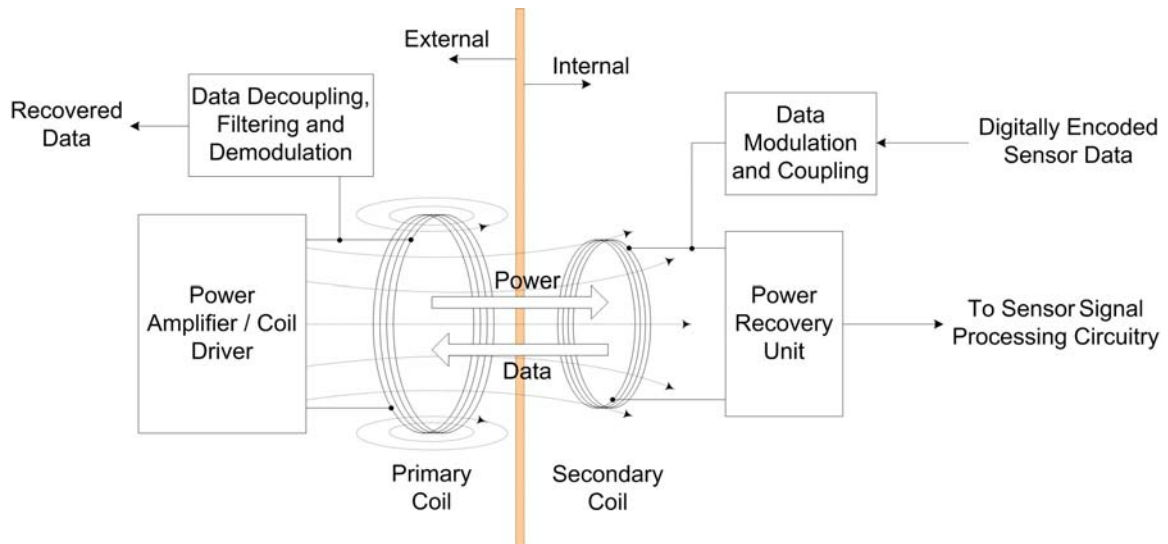


Figure 1.4 Simplified system block diagram

1.5 Thesis Organization

This thesis is organized into six chapters. Each of these chapters is summarized below.

Chapter 2. Literature Review and System Overview

A summary of the major prior works in this area is provided with comparison of their salient features, topologies, performances and limitations. This chapter also provides an overview of the proposed system through block diagrams of the major system units and their basic descriptions. This top-level view of the system facilitates the understanding of the details presented in the next chapters and the interrelation among the system components.

Chapter 3. Inductive Power System Design

The details of the system components that constitute the inductive powering system are provided in this chapter. Fundamental theory and design equations, a step-by-step design procedure, detailed schematic entries, hand calculations and simulation results (where applicable) are organized in a logical order. Some preliminary test results of the powering system are also provided.

Chapter 4. Communication System Design

Details of the system components that constitute the communication system are provided. Key modulation-demodulation concepts, schematic entries, hand calculations and simulation results (where applicable) are presented systematically. Preliminary test results of the communication system are also provided.

Chapter 5. System Integration

Issues related to overall system integration, PCB layouts and other considerations are discussed. Test results of the integrated system implemented as two printed circuit boards are provided. Discussion and analysis of the test data is also provided.

Chapter 6. Conclusion and Future Directions

The contributions in this thesis is summarized and suggestions given for future directions and enhancements of this work.

CHAPTER 2

Literature Review and System Overview

This chapter provides a brief literature review and overview of the major system blocks of this work. A number of significant prior works in the field of inductive powering and data transfer are summarized and some enhancement techniques are discussed. Then detailed block diagrams of the proposed telemetry system are provided along with a brief description of each functional unit.

2.1 Prior Work in Inductive Link Design

The earliest work in implantable biomedical systems involving an inductive link was reported in the early 1960's [32]. Since then, numerous works have been published investigating many theoretical and practical aspects, different link topologies, performance enhancement techniques, and numerous applications. Before presenting the important inductive link design and optimization concepts, a review of basic terminologies of coil geometry and magnetic circuits is presented including associated implications on the design.

2.1.1 Definition of Terms

Mutual Inductance and Inductive Coupling: Mutual inductance exists between two inductors when their relative position is such that the flux lines generated from one link with the other. In this condition, the two inductors are said to be inductively coupled.

Mutual inductance may be defined as the voltage induced in the second circuit when the current in the first circuit is changing at a unity rate with respect to

time. If the current in the first circuit is sinusoidal, the mutual inductance between the two coils can be expressed as,

$$M = -\frac{E_2}{j\omega I_1} . \quad (2.1)$$

Rearranging the above formula, the mutual impedance can be defined as,

$$Z_m = j\omega M = -\frac{E_2}{I_1} . \quad (2.2)$$

The negative sign indicates that the induced voltage lags the current by 90° .

Coupling Factor: The maximum value of mutual inductance that can exist between two coils of inductance L_1 and L_2 is $\sqrt{L_1 L_2}$, and this occurs when all the flux of one coil links with all the turns of the other.

The ratio of the mutual inductance actually present between two inductances to the maximum possible value is called the coupling factor or coefficient of coupling and is written as,

$$k = \frac{M}{\sqrt{L_1 L_2}} . \quad (2.3)$$

As can be seen from this expression, the coupling factor is a dimensionless quantity that has a maximum value of 1.

The major factors that affect the coefficient of coupling between two coils are –

- Coil separation,
- Coil diameters,
- Relative coil alignment.

Link Efficiency: The link efficiency is defined as the ratio of the power delivered to the load to the power supplied to the primary coil. For the derivation of link efficiency, a few assumptions are generally made: (i) either series or parallel resonance is used for the secondary coil, (ii) the primary loss mechanism is due to

the non-ideal (< 1) coupling factor between the coils, (iii) loss also occurs due to finite Q of the coils, (iv) and the load is purely resistive.

The total link efficiency for a parallel resonant secondary can be written as [44],

$$\eta = \frac{k^2 Q_1 Q_2}{\left(1 + \frac{Q_2}{\alpha} + k^2 Q_1 Q_2\right) \left(\alpha + \frac{1}{Q_2}\right)} . \quad (2.4)$$

For a series resonant secondary the expression becomes,

$$\eta = \frac{k^2 Q_1 \alpha}{\left(1 + k^2 Q_1 + \frac{1}{Q_2}\right) \left(\alpha + \frac{1}{Q_2}\right)} . \quad (2.5)$$

In both equations,

Q_1 = quality factor of the primary coil

Q_2 = quality factor of the secondary coil

k = coupling factor between the coils

α = unitless constant = $\omega C_2 R_L$

ω = angular operating frequency

C_2 = capacitance of the secondary resonant capacitor

R_L = load resistance

2.1.2 Factors Affecting Inductive Link Performance

Some of the factors that vastly influence the performance of an inductive link are qualitatively discussed here. It will be obvious from the discussions that most of these elements are greatly interdependent, and consequently, extensive trade-offs are associated with the design choices.

Coil Dimensions and Turns: The voltage transfer ratio or voltage gain of an inductive link varies in proportion with the square of the diameter of the receiver (secondary) coil, and inversely with the diameter of the transmitter (primary) coil

[33]. Since the self and mutual inductances of the coils also vary proportionally with their diameters, the coupling factor, and therefore the link efficiency, also increase with increasing diameters. In general, larger coil sizes result in increased power transfer and efficiency, although many applications impose limits on having large coils. Depending on the application, the practical coil diameters may range from a few millimeters to several centimeters. The limits on the receiver coil size are usually more stringent than that of the transmitter coil, as it is part of the implanted system.

Although the coupling factor between two coils is independent of their number of turns, the mutual inductance, and hence the voltage transfer ratio, is proportional to the product of the number of turns in the transmitter and receiver coils.

Coupling Factor and Mutual Inductance: Coupling factor or coupling coefficient between two inductively coupled coils is a function of the coil dimensions, relative coil positioning and coil spacing. The mutual inductance is directly proportional to coupling factor. Therefore, the voltage gain of the link varies proportionally with both of these quantities, while the link efficiency has an approximate square law relationship with the coupling. Using a magnetic core material inside the coils can considerably increase the self and mutual inductances of the coil pair, and hence the voltage gain. The factor of increment, or the multiplying factor (μ_f), depends on the relative length and cross-section of the magnetic (usually ferrite) material and typical values range from 4 to 15 [34].

Coil Spacing and Alignment: A small increase in the separation between the coils can significantly reduce the coupling between them, resulting in a proportional decrease in gain.

For a given size and separation of the coils, the mutual inductance increases to some extent as the coils are moved from the perfectly coaxial alignment, provided that the receiver coil is within the circumference of the transmitter coil. Both theoretical evaluation and experimental results suggest that the receiver coil will operate anywhere within the circumference of the transmitter coil with performance comparable or better than that with an exact coaxial alignment [33]. It should still be remembered that variation in coil alignment changes the mutual inductance and link gain, which may not be acceptable for many applications. However, if active line regulation is employed at the implanted unit, variation in coupling is not of serious concern, as long as the mutual inductance remains above a certain level.

Quality Factor: The link efficiency of a typical inductive link slowly varies with the product of the primary and secondary coil's unloaded quality factors (Q_s) [35, 36]. Therefore, reasonably high Q values for the coils at the frequency of operation are necessary in order to achieve satisfactory power transfer efficiency. In addition, if the Q is too low, the output voltage will be sensitive to load changes [3]. However, it is also known that the bandwidth of a circuit is inversely proportional to its quality factor, i.e., higher Q usually translates to narrowband performance. Consequently, care must be taken in choosing the equivalent or loaded quality factor of an inductive link, while realizing a communication scheme over the link.

Frequency of Operation: The operating frequency affects several aspects of an inductive link. The mutual impedance, and hence the voltage transfer ratio is better with higher frequency. Since the quality factor of a reactive element is, by definition, a function of frequency, the efficiency and bandwidth of the link are also impacted by the choice of frequency. Another very important consideration, particularly for biomedical applications, is the absorption of RF energy in body tissue. As discussed in section 1.3.3, the conductive losses associated with tissue

absorption increases approximately as the square of the frequency in the 1-100MHz range. Also, power is lost through electromagnetic radiation by the coils, which increases with increasing frequency. Thus, careful consideration must be given to the associated trade-offs before selecting the frequency of operation for a particular application. The frequency should be low enough to keep the tissue absorption at a minimum, and high enough to allow for a sufficient data transfer rate and voltage transfer ratio.

Link Driver Topology: The external or primary coil is usually driven by a low-loss switching amplifier. The overall power transfer efficiency of an inductive link is dependent on the primary coil driver efficiency. A desirable characteristic for high driver efficiency is that the drive transistor should only draw current when there is no voltage across it, and such a behavior can be achieved with a tuned amplifier load [10]. The correct operation of this type of amplifier is subject to the proper design of the loading network connected to the active device. The output power in a switch-mode power amplifier is determined only by the supply voltage, and the output power is proportional to the square of the supply voltage if the amplifier is operated properly.

Among all the switch-mode power amplifier types, Class-C [10, 35] or Class-E [4, 14, 38, 52-54] converters are the most commonly used topology for driving inductive links; however, Class-D [3, 37] and Class-C-E [36] types have also been reported in literature.

A Class-C amplifier conducts less than half of the RF period and can achieve very high efficiency. However, for this class of amplifier, as the efficiency moves towards unity, the output power approaches zero. This is evident from the analyses of the theoretical expressions for the maximum achievable efficiency and the output power corresponding to the maximum efficiency condition [39]:

$$\eta_{\max} = \frac{2y - \sin 2y}{4(\sin y - y \cos y)} \quad (2.6)$$

$$P_{\max} = \frac{2y - \sin 2y}{8\pi(1 - \cos y)} \quad (2.7)$$

where y is the conduction angle expressed as a percentage of the RF period.

Both Class-D and Class-E type switching amplifiers can theoretically achieve 100% efficiency if the switch is ideal, i.e., the switch has a zero switching time, zero on-resistance and infinite off-resistance. However, for a Class-D amplifier, these conditions are not guaranteed because of “hard-switching”, even if an ideal switch is used. An explanation for the terminologies “hard-switching” and “soft-switching” is provided in [40].

The Class-E amplifier, reported by Sokals in 1975 [41, 42], presents a clever method of guaranteeing soft-switching by shaping the drain voltage and current waveforms for the active device. This driver type exhibits an inherent insensitivity to small timing errors, as the transistor voltage and its derivative are ideally zero when the switch is turned on. It can be shown that for the same required primary coil voltage, an incidental mistiming in switch closure will cause lower losses in a properly designed Class-E driver, due to a lower voltage across the switch during turn-on time.

It is, therefore, not surprising that the Class-E drivers or power amplifiers are superior to most of the switching amplifiers in terms of efficiency. Nonetheless, Class-E amplifiers, like most other switch-mode amplifiers, are quite sensitive to variations in the impedance of the output network [43]. A variation in the internal load, either by a change in power demand or a change in coupling factor of the coils (k), will therefore result in a change in the equivalent series resistance of the primary circuit as seen by the driver. Thus for implanted applications,

changes in the physical configuration of the two coils and the surrounding materials will affect the overall link gain and efficiency.

2.1.3 Efficiency Enhancement Techniques

Several techniques for the enhancement and optimization of the inductive link efficiency are discussed in literature, and are generally summarized below:

- The most common technique for increasing the link efficiency is the use of resonant primary and/or secondary coils. Although four different combinations for the primary-secondary resonance are possible (series-series, series-parallel, parallel-series, parallel-parallel), a series-parallel combination is widely used with both the sides tuned to the same resonant frequency. A series-resonant primary circuit provides a low impedance path to the link driver, resulting in increased link power transfer. The secondary, on the other hand, is almost always implemented using a parallel tank circuit, enabling improved drive of a non-linear rectifier load [12]. In addition, parallel tuning of the secondary coil further improves the efficiency [44].
- Careful design of the system equivalent resistances is another important efficiency optimization technique. For the series-tuned primary and parallel-tuned secondary, the link efficiency can be expressed as the product of the efficiency of the primary circuit and the efficiency of the secondary circuit, given respectively by [44]:

$$\eta_{prim} = \frac{R_{eq}}{R_{eq} + R_{L_1}}, \text{ and} \quad (2.8)$$

$$\eta_{sec} = \frac{Q_{L_2}}{\alpha + Q_{L_2}} \quad (2.9)$$

where

$$R_{eq} = k^2 \omega L_1 \cdot \frac{\alpha Q_{L_2}}{\alpha + Q_{L_2}} = \text{equivalent resistance of the secondary circuit,}$$

$$\alpha = \omega R_{load} C_2, \quad Q_{L_1} = \frac{\omega L_1}{R_{L_1}}, \quad Q_{L_2} = \frac{\omega L_2}{R_{L_2}},$$

L_1, L_2 = inductances of the primary and secondary coils respectively, and
 R_{L_1}, R_{L_2} = equivalent series resistances of the coils.

Therefore, further optimization of the efficiency can be achieved by keeping R_{L_1} as small as possible (which is proportional to the number of coil turns) and by choosing an optimal value for α .

An interesting fact is that the variation of the primary coil inductance has virtually no influence on the total link efficiency as long as R_{eq} is considerably larger than R_{L_1} [14].

- A self-oscillating Class-E coil driver topology has reported link efficiency improvements [45], where the frequency of operation is not fixed, rather influenced by the relative position of the coils. This citation reports that the oscillation frequency offset due to coupling variations may be employed to significantly improve the power transfer performance. Specifically, the resulting frequency obtained through a feedback network tracks the frequency corresponding to the maximum transmission efficiency, whose spectral position is dependent on the coupling between the coils.

2.1.4 Coupling Enhancement Techniques

The coupling factor and hence the mutual inductance of an inductive link for implantable applications is usually variable in nature, mainly because the relative position and alignment of the coils are not well defined. However, the following techniques could be adopted for maximizing the coupling within certain geometrical constraints:

- Ko *et al.* [35] have shown that for a given internal coil diameter (d_2), coil spacing (D) and diameter to length ratios for the external and internal coils (d_1/l_1 and d_2/l_2 respectively), the primary or external coil diameter that provides the maximum coupling factor can be calculated from the following equation:

$$d_1 = \sqrt{d_2^2 + 4D^2} \quad . \quad (2.10)$$

This formula can be used as a first step to maximize the coupling factor, k .

- Zierhofer *et al.* [46] presented a geometric approach for enhancing the coupling between two inductively coupled coils. This enhancement was achieved by distributing the turns of each coil across the individual coil diameter instead of concentrating them at the outer circumference. Theoretically calculated values for identical primary and secondary coils showed an enhancement by 68.8% for a given coil size and a coil spacing of 40mm. The experimental results were in excellent agreement with the theoretical values. As an added advantage, the coupling of the distributed coils tends to be less sensitive to the inter-coil spacing.

However, the disadvantages of this technique are: 1) a moderate decrease of the unloaded quality factors of the coils due to increased wire length (typically the unloaded Q s are reduced by 20%), and 2) difficulty in winding the coil turns, particularly if the coils are hand-wound.

2.1.5 Gain Desensitizing Techniques

Two popular techniques, namely the geometric approach and the stagger-tuning approach, have been widely used in inductive link design to minimize gain sensitivity (usually a voltage gain) to changes in coupling. Many implantable applications require a stable, constant power supply, and therefore, a voltage regulator is usually employed in the internal power recovery circuitry. However, if the gain variation is too large, then a considerable fraction of the received

power will be wasted in the regulator. Therefore, at least a first degree of desensitization of the gain should be realized in a practical inductive link based system. The two techniques stated above are briefly discussed here:

- The most commonly used approach, known as the geometric approach, uses an external or transmitter coil that is larger than the internal coil [47-50]. In this way, the flux lines shared by both the coils remain nearly same, as long as the internal coil stays within the perimeter of the larger external coil. This technique ensures that the coupling factor between the coils remains fairly constant despite relative changes in lateral coil positioning (including tilt), thus minimizing the effect on the link gain.

Unfortunately, this approach is still sensitive to changes in the coil separation. The coupling factor and hence the link gain changes proportionally with the spacing between the coils (in the near field) [3].

- Galbraith *et al.* [3] proposed a new technique, known as the stagger tuning approach that desensitizes the link gain to coupling variations. This approach considerably reduces the effect of misalignment and coil separation on link gain. It has been reported that the stagger tuning approach can provide both an efficient power transfer performance and a wide bandwidth.

A doubly-tuned inductive link (both coils being either series- or parallel-resonant) acts like a narrowband passive bandpass filter with the two poles of its frequency response usually being located at the frequency of operation. In a stagger-tuned link, however, one pole is placed above the operating frequency, while the other one is placed below it. The poles move with the variations of the coupling factor, and by proper placement of the poles, it can be ensured that the resulting displacement in the location of the poles will compensate for the gain variation due to change

in coupling. The ultimate result of this scheme is minimal changes in link gain over a broad range of coupling variation.

2.1.6 Bandwidth Enhancement Techniques

Although inductive links are generally suited for narrowband applications due to its inherent characteristics, some methods have been reported that investigate means for increasing its bandwidth. A few such approaches are discussed in this section:

- The stagger tuning technique, that can be used for desensitizing the link gain as described in the previous section, also brings in the attractive feature of a wide bandwidth. In a stagger-tuned inductive link, the two poles of the primary and secondary resonant tanks are separated in frequency instead of being superimposed on each other. As the coupling changes, the poles move either toward or away from each other in such a way that a stable and nearly coupling-insensitive gain is provided over a relatively large frequency band around the frequency of operation. Thus, an increased bandwidth can be achieved without excessively loading the resonant circuits, which could otherwise reduce the power transfer efficiency [3].
- Two novel techniques, called MVS (Magnetic Vector Steering) and HCAM (Half-Cycle Amplitude Modulation) have been proposed by Mueller *et al.* [51] for enhancing wireless data collection from high-bandwidth biosensors. The two techniques are jointly expected to be useful in applications where multiple, arbitrary positioned implants need to be energized by and communicated with using external circuitry. Through MVS, an external coil assembly of special geometrical arrangements can be used to strategically maneuver the net magnetic field toward a particular implant of interest, thus conserving energy. Then by utilizing another new technique, named half-cycle amplitude modulation or HCAM, data bits

can be transmitted with every half-cycle of the power carrier signal, resulting in a significant increase in the data rate (up to twice the operating frequency). It should be made clear that this approach does not actually increase the bandwidth of the narrowband inductive link; rather it is a clever modulation scheme for achieving a high data rate over a typical link. However, the literature only summarizes a conceptual overview of the proposed scheme; a practical implementation of these techniques with test results have yet to be reported.

2.2 Summary of Published Research

In this section, two tables (Table 2.1 and 2.2) are provided which list and compare the published work associated with implemented inductive links for power and data transmission to implantable systems.

2.3 Proposed System Overview

The work presented in this thesis can be divided into two main functional modules, namely the wireless powering system and the backward data communication or telemetry system. The inductive link, which forms an air-core transformer, provides the handshaking between the external and internal circuitry. The powering system can again be subdivided into two units: the primary or the power transmitting unit, and the secondary or the power recovery unit. The telemetry module consists of the following components: the modulation unit, data coupling and decoupling units, and the demodulation unit.

The following sections provide the block diagrams and brief overview of the system components mentioned earlier.

Table 2.1 Literature Summary I: Inductive Power Links

(Legend: d=diameter, l=length or thickness, n=no. of turns, Q=quality factor, L=inductance, D=spacing between coils, k=coupling factor, η =efficiency)

Ref.	Output Power	Efficiency	Coil Parameters			Driver Type	Application
			Internal	External	Other		
[4]	50 mW @ 5 V or 3.3V	28%	d=3cm	d=3cm	D=1cm k=0.3	Class-E	Visual neuroprosthesis, cortical or nerve stimulations
[9]	20 mW @ 4 V, 1 MHz		d=20mm l=6mm	d=160 mm	D=70 mm	Colpitts transmitter	Strain monitoring in ortho-pedic implants
[10]	16 mW @ 4 V, 1 MHz	0.24%	d=20 mm l=6mm	d=160 mm	D=70 mm	Saturated Class-C	Strain sensing in femoral nail plates
[14]	25 mW @ 5 V (reg.), 750kHz	0.4% (link) 0.25% (overall)	d=1cm, Q = 100	d=30cm	k = 0.0043	Class-E η =90%	Detection of hip prosthesis loosening
[31]*	5 mW @ 5MHz & 10MHz	23% @ 10MHz, 30% @ 5MHz (link η)	d=12mm l=2mm L=7.36 μ H n=13	d=20mm L=1 μ H n=7	D=5mm	-- (function gen. used in testing)	Neural microstimulators
[52]*	250mW @ 15V, 1MHz	36.3% (with adaptive control)	d=22mm l=0.5mm	d=40mm l=5mm	D=15 mm	Class-E (closed-loop)	Retinal prosthesis
[53]*	6.6mW @ 3.3V, 4MHz	Less than 1%	d=2cm	d=5cm	D=25 mm	Class-E	Advanced neurological monitoring

* Some part or whole of the external drive and/or internal power recovery unit was implemented using integrated circuit technology.

Table 2.2 Literature Summary II: Inductive Data Links

Ref.	Forward Telemetry			Backward Telemetry			Application
	Modulation Type	Data Rate, Carrier	Data-rate /Carrier Ratio	Modulation Type	Data Rate, Carrier	Data-rate /Carrier Ratio	
[3]	FM	1Mbps, 20MHz	0.05	N/A	N/A	N/A	Neural Stimulators
[4]	FSK	100 kbps, 1MHz	0.1	DBPSK	15.625 kbps, 500kHz	0.03	Visual neuroprosthesis
[12]*	ASK-BPSK	1.507 Mbps, 13.56 MHz	0.11	LSK	1.13 Mbps, 13.56 MHz	0.08	Visual cortical stimulator
[21]*	Packet detect	-, 2.5MHz	-	Burst of RF energy	-, 2.5MHz	-	Neuro-stimulation
[23]*	ASK	-, 4MHz	-	PWM-ASK	125 kbps, 4MHz	0.03	Peripheral neural recording
[7]*	OOK	100 kbps, 5MHz	0.02	N/A	N/A	N/A	Neural stimulator
[8]*	OOK	-, 6.78 MHz	-	LSK-CCM	200 kbps, 6.78 MHz	0.03	Advanced functional neuromuscular stimulation
[24]	N/A	N/A	N/A	PIM	-, 418MHz	-	Stress monitoring in orthopedic implants

Table 2.2 Continued.

Ref.	Forward Telemetry			Backward Telemetry			Application
	Modulation Type	Data Rate, Carrier	Data-rate /Carrier Ratio	Modulation Type	Data Rate, Carrier	Data-rate /Carrier Ratio	
[31]*	FSK	2.5 Mbps, 5/10 Mhz	0.5/0.25 (0.33 on avg.)	N/A	N/A	N/A	Neural stimulation microsystem
[22]*	PWM-ASK	25~250 kbps, 1~10 MHz	0.025	N/A	N/A	N/A	Retinal prosthetic device
[52]*	N/A	N/A	N/A	LSK-pseudoP WM	3.3 kbps, 1MHz	0.0033	Retinal Prosthesis
[53]*	N/A	N/A	N/A	LSK	10kbps, 4MHz	0.0025	Advanced neurological monitoring

* Some part or whole of the communication unit was implemented using integrated circuit technology.

2.4 Inductive Link and the Powering System

At the heart of the whole scheme is the wireless powering system, which receives dc power from an external source, such as a battery, and then through proper amplification, transformer coupling, rectification, filtration and regulation stages, provides the required dc power to the internal (i.e. in the implanted system) components, such as the sensor electronics, signal processing and communication circuitry. As is apparent, this system will contain both a transmitter and a receiver part. To prevent confusion of these functions with the data communication system blocks, they will be referred to as the primary unit and the secondary unit.

2.4.1 The Primary Unit

The primary unit of the power system has three major building blocks as shown in Figure 2.1.

A description of each of these blocks is provided in the following paragraphs:

Power Amplifier & Loading Network: This is the principal building block of the primary unit. A switch-mode power amplifier of Class-E type has been chosen for this block. Its working principles are very similar to that of a switch-mode dc-dc power converter. The reason for choosing the Class-E topology is its high power

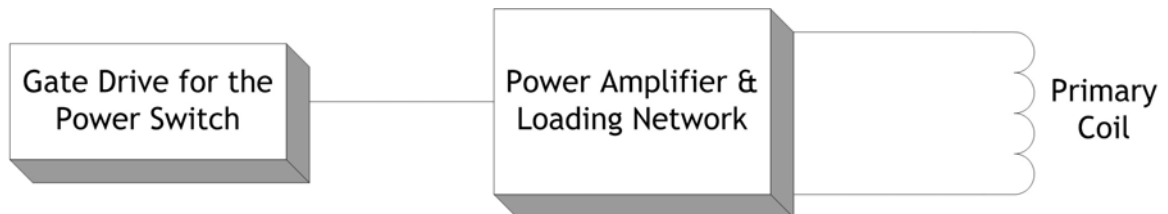


Figure 2.1 Block diagram of the primary unit

transfer efficiency, making it better suited for portable and wireless applications. The Class-E amplifier, also known as the Class-E driver, generates a sinusoidal current to its load whose magnitude is determined by the switching frequency of the power switch and the characteristics of its loading network.

Gate Drive for the Power Switch: A square-wave gate signal at the frequency of operation for the power-carrying signal must be generated to drive the gate of the MOSFET switching device inside the power amplifier block. A free-running oscillator can be used followed by a gate driver IC for the power device. A high-current driver is often needed for driving the high input capacitance that is usually associated with a low-impedance power switch.

Primary Coil: This is a hand-wound coil of suitable dimensions, wire thickness, number of turns and inductance, which comprises the primary winding of an air-core transformer. This coil is in series resonance with the loading network for the class E driver. The coils reactance, along with the reflected impedance from the secondary unit, appears as the load for the power amplifier.

2.4.2 The Secondary Unit

The secondary unit of the power system consists of typical power recovery and management blocks such as a rectifier, filters, a clamp and a voltage regulator (see Figure 2.2).

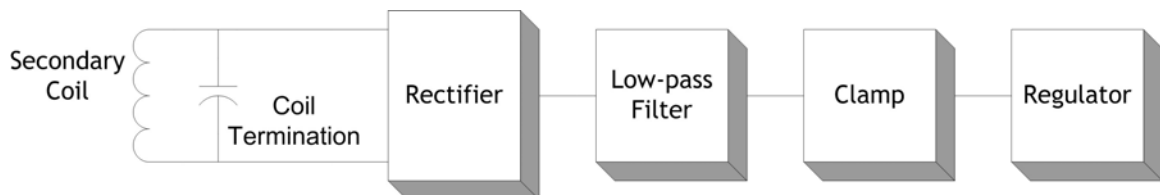


Figure 2.2 Block diagram of the secondary unit

The following descriptions are included to provide a brief idea of the secondary unit components.

Secondary Coil and Coil Termination: This is a hand-wound coil that comprises the other half of the air-core transformer between the primary and secondary units. The coil is terminated using a capacitor in parallel to form a resonant tank circuit.

Rectifier: A full-wave bridge rectifier topology is used to maximize power transfer. Schottky barrier diodes have been employed in the bridge to provide fast switching and increase efficiency.

Low-pass Filter: A filter composed of an L-C type pi-section and a high inductance ac-blocking choke that precedes the pi-section is used to reduce the ripple of the rectifier output voltage. Miniature conformal coated inductors and high-Q ceramic/tantalum capacitors have been used for this filter.

Clamp: A typical Zener diode based clamp circuit is used between the filter and regulator blocks to limit the voltage input to the voltage regulator. This limiting is required as changes in the relative positioning of the coils may produce large changes in the filtered rectifier output voltage.

Regulator: A low-power, low-dropout voltage regulator is used following the rectifier and first order filter stages to further reject ripple and provide a clean and stable dc signal to the output load.

The background theory, architecture and the detailed design procedure for the wireless powering system are discussed in Chapter 3.

2.5 Data Communication

The inductive link developed in this work is capable of transferring digital data from the secondary to the primary unit (i.e., from the implanted sensor to the outside world). Several modulation schemes were investigated before selecting the Frequency Shift Keying (FSK) technique.

As in any communication system, it consists of modulation/demodulation units and the mechanisms for coupling/decoupling with the transmission medium, the transformer coils in this case. The following sections illustrate the block diagrams of these units along with brief overviews of their constituents.

2.5.1 The Modulation Unit

Since the communication system is designed for transferring sensor data from the implanted part to the external part (reverse or backward telemetry), and is powered by the secondary unit of the power system, the modulation unit has the same ground as the secondary power unit. The block diagram of the modulation unit is shown in Figure 2.3.

As is understood from this figure, a voltage-controlled oscillator (VCO) is the major building block of the modulation unit that provides two different frequencies for the logic '0' and logic '1' level of the data. The digital data comes

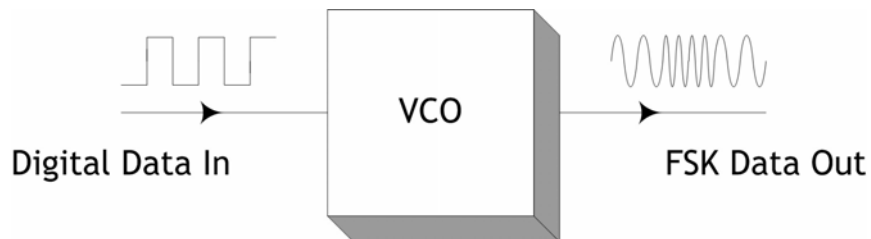


Figure 2.3 Block diagram of the modulation unit

from the implanted sensor signal-processing circuitry, for example, the one described in section 1.1. A low-power PLL chip has been chosen, where only the VCO block is used in an open-loop configuration for the FSK carrier generation.

2.5.2 The Coupling and Decoupling Units

A major challenge in designing the communication system was to effectively couple the FSK carriers to the secondary coil, and likewise, to decouple the induced FSK signals from the primary coil. Each of these functions has to be implemented having a minimal or acceptable impact on the power transfer over the same inductive link or the Class-E operation of the power amplifier. The coupling and decoupling circuit blocks are shown in the shaded region of Figure 2.4.

Traps: A special technique has been applied that uses proper combinations of series and parallel ‘trap’ networks at suitable locations of the data signal and power signal paths. These networks are series and parallel resonators respectively. The parallel trap in a circuit branch rejects or attenuates the signal of a particular frequency (frequency band, to be precise), while the series trap allows a certain frequency range to pass. Therefore, the parallel traps

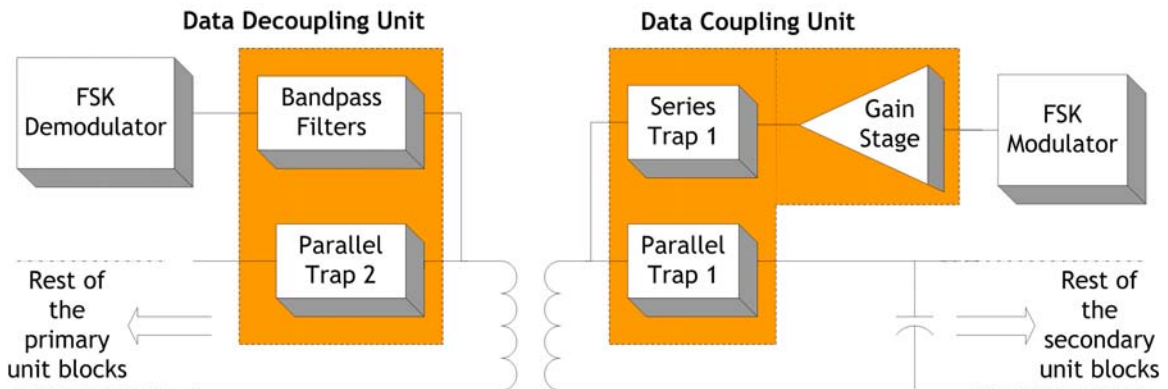


Figure 2.4 Block diagrams of the data coupling and decoupling units

approximate the operation of a band-rejection filter, and the series traps approximate that of a band-pass filter.

Gain Stage: A gain stage is included following the modulator unit that eliminates the effect of direct loading of the secondary coil at the modulator output, and thus helps couple sufficient amplitude of the FSK modulated data to the secondary coil. A simple common-source amplifier biased for low power dissipation is adequate for this requirement.

Bandpass Filters: Another challenging component of the implementation of the reverse communication scheme is the bandpass filters. Because the induced FSK signals at the primary coil are mixed with the power carrying signal and its associated harmonics, which have much higher signal power, a very careful design for the filtering stage is mandatory. In this design, a high order passive bandpass filter followed by an active bandpass filter were incorporated. The active bandpass filter provides additional gain needed before feeding the decoupled FSK modulated data to the demodulator input.

2.5.3 The Demodulation Unit

This demodulator unit, as shown in Figure 2.5 extracts the digital data from the filtered FSK carriers. A PLL can nicely perform this job provided that the VCO frequencies are set correctly and the loop filter is properly designed.

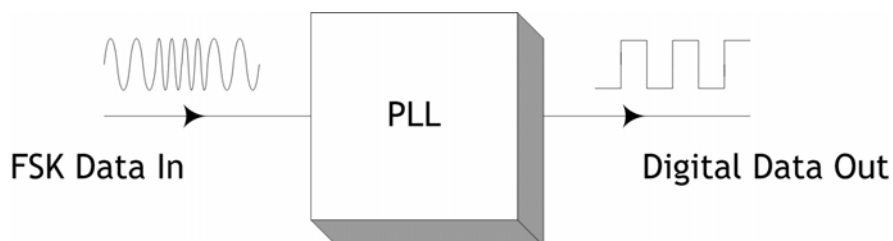


Figure 2.5 Block diagram of the demodulation unit

A low-power general-purpose PLL chip and a passive loop filter are used to implement the demodulator (the loop is not shown in the figure above). A comparator with hysteresis may also be used at the output of the demodulator to produce logic-level signals.

2.6 Complete System Block Diagram

Based on the discussions and the top-level views of the different units presented in the earlier sections, it is possible to construct an overall system level block diagram. The integrated system is illustrated in Figure 2.6. In this figure, all the system blocks described earlier are shown; however, the primary and secondary coils have been put together under the 'transformer' block, and thus have been excluded from the primary and secondary power units respectively.

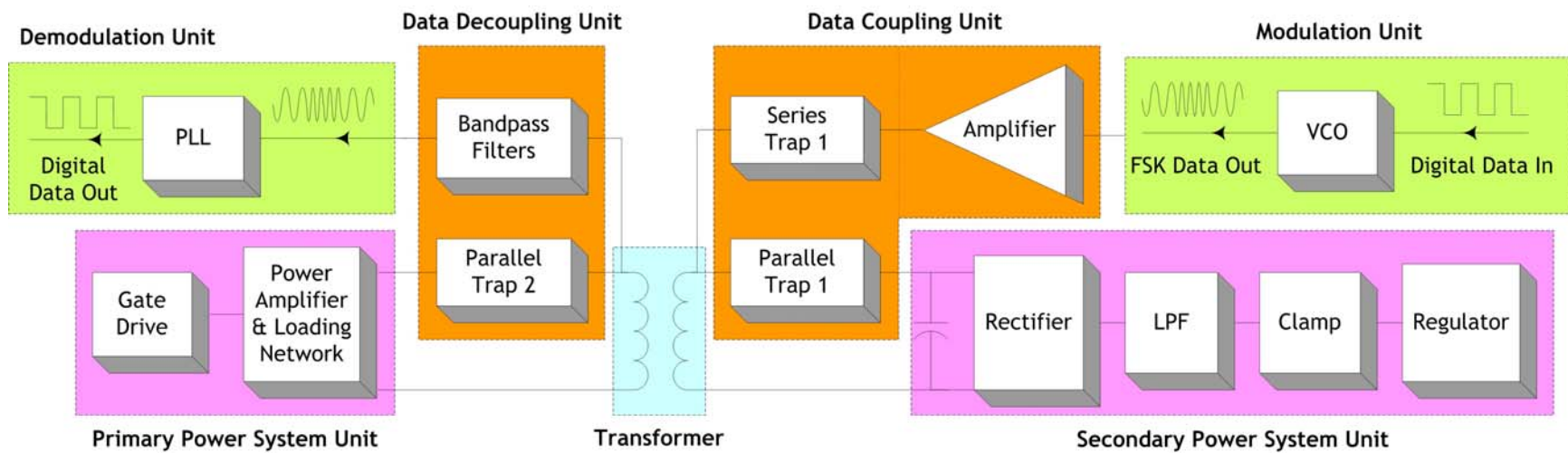


Figure 2.6 Detailed system block diagram

CHAPTER 3

Inductive Power System Design

This chapter provides the details of the design procedure adopted for different components of the wireless powering system. It also includes the relevant background theories, important design equations and discussion of several factors that affect the performance of the system and hence the applicable strategies in different stages of the design task. Detailed schematic diagrams, ample hand calculations, SPICE simulation results, and finally, test results are provided for the inductive power system.

3.1 The Coil System

The circular coil system acts as a weakly coupled air-core transformer between the external (primary) and internal (secondary) part of the system consisting of two hand-wound coils of suitable geometrical, magnetic and electric properties. The choices of different parameters were made based on physical constraints, performance and compatibility with other system elements. Before presenting the theory of the circular coil system and applicable formulas, the choice of resonance for the secondary coil is discussed.

3.1.1 Choice for Secondary Resonance

In an inductive link design, a capacitor is generally added either in series or in parallel with the secondary coil. The reason is two-fold:

- 1) The resonant capacitor cancels the reactance (in series resonance) or admittance (in parallel resonance) of the secondary coil; therefore, ideally the load seen by the primary driver is purely resistive.
- 2) It can be shown that using either series or parallel resonance achieves an optimal coupling efficiency [44].

By plotting the link efficiency against α (using equations 2.4 and 2.5) for a given set of coil Q 's and low coupling factor (hence low power links), it has been shown [36] that the series resonance case requires a very large secondary coil inductance for optimum link efficiency. These large inductance values can be practically impossible to attain, as there are size limitations for the internal/secondary coil in many applications (including implantable biomedical sensor applications). Therefore, low power links are usually utilized using secondary parallel resonance, making the L-C tank act as a voltage source.

For high power, high coupling applications, it has been shown [36] in a similar fashion that both resonance schemes are practically implementable and can be quite efficient as well. It is, however, noteworthy that parallel and series resonant configurations have different output characteristics; the parallel case provides a voltage source type output, while the series resonant coil acts like a current source.

3.1.2 Theory of the Inductively Powered Coils

The fundamental concepts that govern the design of an inductive link are described in this section, and follow the work presented by W.H. Ko *et al.* [34]. The theory and accompanying practical design equations were developed using the basic inductively coupled circuit and its equivalent secondary circuit as shown in Figures 3.1 and 3.2.

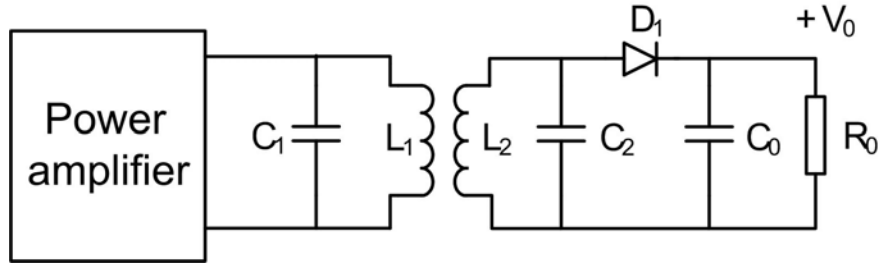


Figure 3.1 Basic inductively coupled circuit

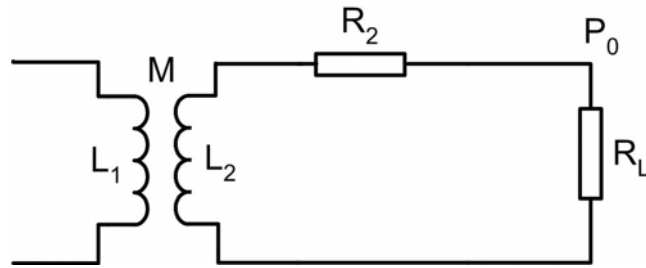


Figure 3.2 DC equivalent secondary circuit for Figure 3.1

It should be noted that although a parallel capacitor has been shown across the primary coil, both series and parallel resonance could be used.

The total equivalent series resistance in the secondary tank circuit (as shown in Fig. 2) is, $R_2 + R_L$, where R_2 is the series resistance of the unloaded secondary tank circuit and R_L is the load resistance.

The equivalent resistance R_e , reflected back into the primary coil is,

$$\begin{aligned}
 R_e &= \frac{(\omega M)^2}{R_2 + R_L} \\
 &= \frac{Rk^2 Q_1 Q_2}{R + Q_2^2 R_2} \cdot R_1
 \end{aligned}
 \tag{3.1}$$

where, $M = k\sqrt{L_1 L_2}$ = mutual inductance of the coils, and

$Q_1 = \omega L_1/R_1$, $Q_2 = \omega L_2/R_2$ are the unloaded Q s of the primary and secondary coils, respectively, and
 $R =$ equivalent ac load resistance.

Therefore, the equivalent circuit referred to the primary side can be found and is shown in Figure 3.3.

Overall Circuit Efficiency at Resonance:

From the primary equivalent circuit, shown in Figure 3.3, the circuit efficiency at resonance can be derived as,

$$\eta = \frac{P_o}{P_i} = \frac{k^2 Q_1 Q_2^3 R_2 R}{(R + Q_2^2 R_2) \left\{ (1 + k^2 Q_1 Q_2) R + Q_2^2 R_2 \right\}} \quad (3.2)$$

As can be seen, the overall efficiency has a strong dependence on coupling factor, k . However, the maximum value of k that is practically attainable is determined by coil size, spacing, and alignment.

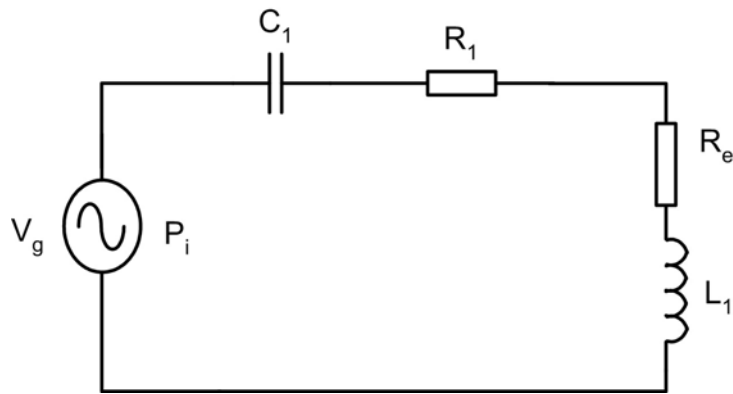


Figure 3.3 Primary-referred Equivalent Circuit

Optimum Efficiency:

If the derivative of the efficiency expressed in equation (3.2) is taken with respect to R_2 (for a given set of k , Q_1 and Q_2) and set to zero, then the optimum value of R_2 required for maximum efficiency is found to be,

$$\therefore R_{2opt} = \frac{R(1 + k^2 Q_1 Q_2)^{\frac{1}{2}}}{Q_2^2} . \quad (3.3)$$

Substituting this result into equation (3.2) yields the optimum efficiency of the circuit,

$$\therefore \eta_{opt} = \frac{k^2 Q_1 Q_2}{\left[1 + (1 + k^2 Q_1 Q_2)^{\frac{1}{2}} \right]^2} . \quad (3.4)$$

This equation once again confirms that the optimum efficiency increases as $k^2 Q_1 Q_2$ increases, and therefore the first and foremost design consideration in an inductive link design is the attainment of the highest possible unloaded Q and k . As will be seen shortly, these two vital parameters are functions of the shape, size and relative position of the coils.

Important Link Parameters for a Parallel Co-axial Coil Arrangement:

A typical co-axial coil arrangement used in inductive powering applications is shown in Figure 3.4.

- Let, n_1 = number of turns on the primary coil,
 n_2 = number of turns on the secondary coil,
 d_1 = diameter of the primary coil,
 d_2 = diameter of the secondary coil,
 D = spacing between the coils,
 M_0 = mutual inductance between two co-axial single-turn coils of same diameters and spacing

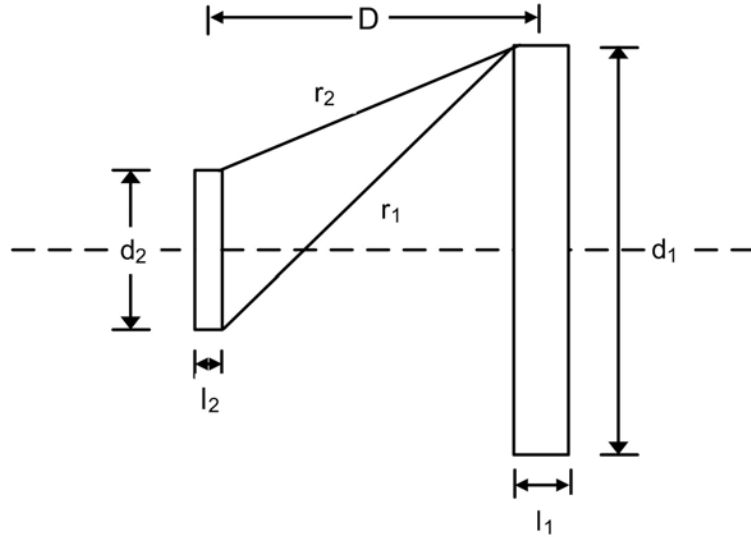


Figure 3.4 Co-axial coil arrangement

Therefore, the mutual inductance between the coils,

$$M = n_1 n_2 M_o . \quad (3.5)$$

Now, from the definition of M ,

$$k^2 = \frac{M^2}{L_1 L_2} = \frac{(n_1 n_2 M_o)^2}{L_1 L_2} . \quad (3.6)$$

The low frequency self-inductance of a single-layer solenoid is given by,

$$L = F n^2 d \text{ (in microhenrys)} \quad (3.7)$$

where, d = diameter of the coil,

F = shape factor, which is a function of the diameter and length of the coil.

This is a rearrangement of the well-known Nagaoka formula.

Again, M_o is given by,

$$M_o = 1.27 N (d_1 d_2)^{\frac{1}{2}} \quad (3.8)$$

where, N = a function of $\frac{r_2}{r_1}$.

From equations (3.6), (3.7) and (3.8),

$$k^2 = \frac{(1.27N)^2}{F_1 F_2} \quad (3.9)$$

where, F_1, F_2 = shape factors for the primary and secondary coils respectively.

It is important to note that k is independent of the number of turns of the coils,

and N increases as $\frac{r_2}{r_1}$ decreases. Values of F and N as a function of $\frac{r_2}{r_1}$ can be

found in Tables 12 and 17 of [55] respectively.

The ratio $\frac{r_2}{r_1}$ can be determined with the help of Figure 3.4 as,

$$\begin{aligned} r_2^2 &= D^2 + \frac{(d_1 - d_2)^2}{4} \Rightarrow 4r_2^2 = 4D^2 + (d_1 - d_2)^2 \\ r_1^2 &= D^2 + \left\{ \frac{d_1 - d_2}{2} + d_2 \right\}^2 \Rightarrow 4r_1^2 = 4D^2 + (d_1 + d_2)^2 \\ \therefore \frac{r_2}{r_1} &= \sqrt{\frac{4D^2 + (d_1 - d_2)^2}{4D^2 + (d_1 + d_2)^2}} \end{aligned} \quad (3.10)$$

Optimum Value of d_1 for Maximum Coupling Factor:

As can be seen from equation (3.9), maximum N and hence minimum $\frac{r_2}{r_1}$ is

desired for maximum k . By setting $\frac{d\left(\frac{r_2}{r_1}\right)}{d(d_1)} = 0$,

$$\begin{aligned} \left\{ (d_1 + d_2)^2 + 4D^2 \right\} \cdot 2(d_1 - d_2) - \left\{ (d_1 - d_2)^2 + 4D^2 \right\} \cdot 2(d_1 + d_2) &= 0 \\ \Rightarrow d_1(4d_1 d_2) &= d_2(2d_1^2 + 2d_2^2 + 8D^2) \\ \Rightarrow d_1^2 &= d_2^2 + 4D^2 \end{aligned}$$

Therefore, for a given d_2 and D , $\frac{r_2}{r_1}$ is minimum, when

$$d_1 = (d_2^2 + 4D^2)^{\frac{1}{2}}. \quad (3.11)$$

Equations (3.5) through (3.11) form the basis of the inductive link design. As mentioned earlier, the primary design objective is to achieve the maximum k possible under given geometric constraints. Keeping this in mind, a step-by-step design procedure is presented in the next section that facilitates the design.

3.1.3 Design Procedure for an Inductive Link

Based on the analyses presented in section 3.1.3, the following steps for designing the primary and secondary coils were presented in [35].

It is assumed that the following are known or derived conditions:

- (a) $V_o, I_o, R_o = V_o/I_o$ (i.e., dc output requirements),
- (b) the spacing D between coils,
- (c) the secondary coil diameter d_2 ,
- (d) the diameter-length ratio of the two coils d_1/l_1 and d_2/l_2 ,
- (e) frequency of operation.

The design procedure is outlined in the following steps:

- (i) Calculate d_1 by equation (3.11) to maximize k^2 .
- (ii) Calculate r_2/r_1 by equation (3.10), obtain the value for N and the values for F_1 and F_2 , calculate k^2 from equation (3.9).
- (iii) Calculate η_{opt} . In order to do this, the unloaded Q_1 and Q_2 must first be selected. Since it is very difficult to perform the theoretical calculation of the unloaded Q of the coils, experimental measurement of the Q values is preferred, and that yields a close approximation as well.
- (iv) Determine L_2 and C_2 . R_2 can be determined from equation (3.3) and is used to calculate L_2 and C_2 by:

$$L_2 = \frac{Q_2 R_2}{2\pi f} \text{ and } C_2 = \frac{1}{(2\pi f)^2 L_2} .$$

- (v) Calculate the approximate total resistance of the primary circuit.
- (vi) Determine L_1 and C_1 . In order for doing that the loaded Q of the primary circuit, Q_{L1} , must be determined.
- (vii) Calculate the number of turns of the two coils. Rearrangement of equation (3.7) yields the equations for the number of turns:

$$n_1 = \left(\frac{L_1}{F_1 d_1} \right)^{\frac{1}{2}} \text{ and } n_2 = \left(\frac{L_2}{F_2 d_2} \right)^{\frac{1}{2}} .$$

For the particular design presented in this thesis the steps (i) to (iii) have been almost exactly followed. In step (iv), L_2 has not been calculated first; rather a coil has been built with suitable number of turns and diameter based on some practical considerations and physical constraints. Then C_2 has been calculated. The determination of L_1 and C_1 in step (vi) was done with the design of the primary coil driver that is discussed in section 3.3.2.

3.1.4 The Designed Link

Known or Derived Conditions:

(a) DC Output Requirements: $V_o = 5V$, $I_o = 25mA$

$$\therefore R_o = \frac{V_o}{I_o} = 200\Omega .$$

These are found from an estimated load requirements, where the load is the implanted sensor signal processing electronics.

(b) Spacing between two coils, $D = 1cm$.

This is just an estimate of the distance between the implanted and external coil and serves as a starting point for the link design.

(c) Secondary coil diameter, $d_2 = 7.12\text{cm}$.

This size has been chosen considering the perimeter of the prototype board of the implantable electronics. It is understood that in a real life application, both the board containing the electronics and the coil will need to be miniaturized.

(d) Assuming $l_2 = 0.72\text{cm}$, the diameter-length ratio for the secondary coil is,

$$d_2/l_2 = 9.9.$$

d_1/l_1 will be found when the optimum d_1 is calculated.

As in the case for diameter, this coil length has been chosen considering the size (height) of the proto-board.

(e) The frequency of operation has been chosen to be 200kHz.

This has been tried to keep as low as possible in order to reduce the amount of electromagnetic radiation exposure to body-tissue, but high enough to provide a convenient bandwidth for the backward data communication.

Step 1:

Using equation (3.11) and the conditions stated above, $d_1 = 7.4\text{cm}$ is obtained.

This is an acceptable diameter for the primary coil, particularly because the size restrictions for the external unit are less stringent.

If the length for the primary coil is chosen to be 0.89cm, then $d_1/l_1 = 8.32$.

Step 2:

Substituting the values of d_1 , d_2 and D in equation (3.10) yields,

$$\frac{r_2}{r_1} = 0.1379.$$

Using Table 17 of [55], $N = 0.01762$, and

Using Table 12 of [55], $F_1 = 0.04806$, and $F_2 = 0.05088$ are found.

Therefore, the estimated coupling factor between the two coils by equation (3.9) is,

$$k = \sqrt{\frac{(1.27 \times 0.01762)^2}{0.04806 \times 0.05088}} = 0.453$$

Step 3 & 4:

After the initial theoretical estimate of the coupling factor, both the primary and secondary coils were built by winding several turns of AWG #18 and #30 wire that have physical dimensions very close to the ones mentioned above. The specifications of the coils are given in Table 3.1.

The electrical parameters of the coils presented in this table were measured using an HP 4192A LF Impedance Analyzer. The choice of inductance for the primary coil (L_1) was dictated by the design of the coil driver (power amplifier) that will be discussed in a later section.

Table 3.1 Primary and Secondary Coil Specifications

	Diameter (cm)	Length (cm)	Turns	Inductance (μH)	ESR (Ω)	Q	Test Frequency
Primary Coil	7.5	0.6	6	5.8	0.09	81	200kHz
Secondary Coil	7.2	0.8	45	267	5.5	61	200kHz

Now, substituting the values of measured Q_1 and Q_2 from Table 2.1 and the calculated k into equation (3.4) yields,

$$\eta_{opt} = 0.94 \text{ or, } 94\% .$$

This is a very high efficiency indeed. However, it must need to be noted that it is the link efficiency, and not the overall power transfer efficiency. This optimum efficiency corresponds to an optimum ESR of the unloaded secondary tank circuit as described by equation (3.3). In addition, several loss mechanisms present in the primary drive unit and in the secondary power management blocks have not been accounted for. So, in reality a much lower efficiency is expected (as discussed in the literature review section of Chapter 2), especially because the optimum R_2 cannot be guaranteed due to the complexity and nonlinearities of the secondary network. However, the above result at least ensures that the coil quality factors and coupling coefficient are good enough to start with, and a moderate overall efficiency for the whole inductive powering system can be expected.

3.2 Secondary-Side Power Conversion and Management

This section starts with the detailed schematics of the secondary unit (as shown in Figure 3.5), and then sequential description of each block's function and the design considerations for them follow.

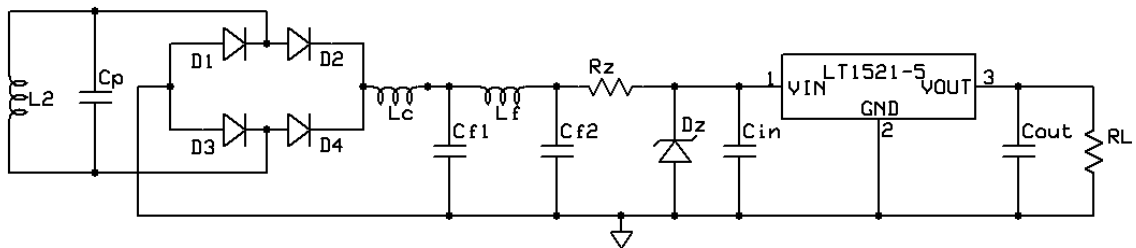


Figure 3.5 Schematic diagram of the inductive powering system's secondary unit

3.2.1 Resonant Tank

A capacitor (C_p) has been placed across the secondary coil (L_2) to form a tank circuit that resonates at the operating frequency of the primary coil drive. Due to the parallel resonance of the tank, it behaves as an ac voltage source to the rest of the secondary network. Since the resonant frequency for a parallel tank is given by, $f_r = \frac{1}{2\pi\sqrt{LC}}$, the value of the parallel capacitor is found as,

$$C_p = \frac{1}{4\pi^2 f^2 L_2} \quad (3.12)$$

where, f = frequency of operation for the primary drive.

For $f = 200\text{kHz}$ and $L_2 = 267\mu\text{H}$, the calculated $C_p = 2.37\text{nF}$.

3.2.2 Rectifier

A full-wave bridge rectifier has been used in this work for the rectification of the induced alternating voltage at the secondary tank. In Figure 3.5, the diodes D_1 through D_4 form the rectifier bridge. Schottky rectifier diodes (part number: 1N5819) have been chosen mainly for two reasons:

- (i) Fast recovery time,
- (ii) Low forward voltage drop (usually less than 0.5V).

3.2.3 Low-Pass Filter

A simple two-stage passive low-pass filter has been used for the filtration of the rectified signal to dc. In Figure 3.5, L_c , L_f , C_{f1} and C_{f2} combinedly form the LPF. In the first stage, a high-inductance conformal-coated inductor (L_c) has been used for blocking most of the ac components. This stage is followed by a Π -section L-C filter, comprised of L_f , C_{f1} and C_{f2} . The cutoff frequency of an L-C Π -section is given by

$$f_c = \frac{1}{\pi\sqrt{LC}} \quad (3.13)$$

where, L = inductance of the only inductor

$C/2$ = capacitance of each capacitor branch.

Now, if $L = 50\mu\text{H}$ and $C/2 = 1\mu\text{F}$ are chosen, for example, that gives a cutoff frequency of $f_c = 31.83\text{kHz}$, which should be good enough to reject most of the ripple content at 200kHz .

3.2.4 Clamp

A Zener diode based clamp circuit has been included between the low-pass filter output and the regulator input in order for providing protection of the regulator input pin against possible over voltage situations. A series resistor R_z and a 9.1V, 1W Zener diode, D_z (part number: 1N4739A) have been connected as shown in Figure 3.5 that makes the clamp circuit. When the voltage at the input of the regulator is less than 9.1V, the Zener diode does not conduct and the system operates normally. If the voltage at the regulator input reaches or exceeds 9.1V, which is the breakdown voltage for this device, then the diode starts conducting. The voltage at this node remains constant at 9.1V as long as the filter output minus the resistor drop is greater than the breakdown voltage, and the extra current flows through the Zener diode. A small resistance value, typically 50-100 Ω is usually chosen so that too much power dissipation at the resistor can be avoided.

3.2.5 Voltage Regulator

In order for providing a constant, stable voltage to the load a voltage regulator should be employed at the final stage of the powering system. For this purpose a

low power, low dropout voltage regulator has been chosen from Linear Technology (part number: LT1521-5). This chip provides a fixed 5V output voltage with a dropout voltage of only 0.5V and it draws only 12μA of quiescent current. A 1μF filter capacitor has been used at the input of the regulator and a 10μF tantalum capacitor at the output, which provides stability and good ripple rejection as well.

3.2.6 List of Secondary Power Unit Components

The actual parts and component values used in building a prototype secondary unit that operates with a 200kHz primary drive signal has been listed in Table 3.2.

3.3 Primary Coil Drive Unit

Since the transformer is an ac instrument the primary coil of the inductive link must be driven by an alternating current that will induce a voltage in the secondary coil through transformer action. As is seen in equation (2.1), the voltage induced in the secondary coil is a function of the primary current, mutual inductance between the coils and the operating frequency, i.e.,

$$E_2 = -j\omega MI_1 .$$

Therefore, by increasing the primary current, the mutual inductance or the operating frequency, the secondary induced voltage can be increased.

Again, the power supplied to the transmitter coil and the power delivered to the receiver coil are given respectively by,

$$P_1 = E_1 I_1 , \text{ and}$$

$$P_2 = E_2 I_2 = \frac{E_2^2}{R_{load}} \quad (\text{Assuming a resistive load network})$$

where, $E_1 = \omega L_1 I_1$ for sinusoidal signals.

Table 3.2 Secondary Powering Unit Component List

Component	Part No. / Value	Description	Features/Comments
Receiver/ Transformer Coil, L_2	267 μ H	Hand-wound coil	ESR = 5.5 Ω , Q = 61 @ 200kHz
Parallel Resonant Capacitor, C_p	2.225nF	Ceramic capacitor	-
Rectifier Diodes, D_1 - D_4	1N5819	Schottky rectifiers	40V, 1A, Maximum Forward Voltage = 0.6V
AC-blocking Choke/Inductor, L_c	1.11mH	Conformal-coated RF choke	ESR = 11.4 Ω
Filter Inductor, L_f	50 μ H	Conformal-coated inductor	ESR = 1.6 Ω
Filter Capacitors, C_{f1} & C_{f2}	1 μ F	Tantalum	-
Clamp Circuit Resistor, R_z	40 Ω	Carbon-film resistor	-
Clamp Diode, D_z	1N4739A	Zener diode	9.1V, 1W
Voltage Regulator	LT1521-5	Low-dropout regulator	5V, 300mA, Dropout Voltage = 0.5V
Regulator Input Capacitor, C_{in}	0.8 μ F	Ceramic capacitor	-
Regulator Output Capacitor, C_{out}	10 μ F	Tantulum capacitor	-

$$\begin{aligned} \therefore P_1 &= \omega L_1 I_1^2 \\ \text{and } P_2 &= \frac{\omega^2 M^2 I_1^2}{R_{load}} = \frac{\omega^2 k^2 L_1 L_2 I_1^2}{R_{load}} . \end{aligned} \quad (3.14)$$

[using the result from equation (2.3)]

It is clear from the above relationship that a high coupling factor and high primary current drive, as well as reasonable choice for the primary and secondary coil inductances are all key to maximizing the transmitted power to the implantable unit. In addition, it is known from equation (2.4) that coupling factor and the quality factors of the coils are important for achieving a high link efficiency.

The above discussion justifies the efforts to obtain a high coupling factor and a reasonably large product of the inductances. Now, in making the choice of the primary coil driver, the considerations are - to have a high current drive and an efficient converter topology so that the achieved link efficiency does not need to be compromised much. After careful considerations, a switching converter of Class-E type has been chosen for driving the primary coil.

3.3.1 The Class-E Driver

The Class-E driver is a special class of switching resonant converters (also known as power amplifiers), where the load is supplied through a sharply tuned series-resonant circuit. The schematic diagram of a low-order Class-E converter has been shown in Figure 3.6.

Principle of Operation:

The circuit configuration of Figure 3.6 results in a sinusoidal output current (i_o) in the coil L_1 and in the load as the loading network's Q_L (loaded Q) approaches infinity [56]. The input to the converter is through a large inductor, L_D (usually a

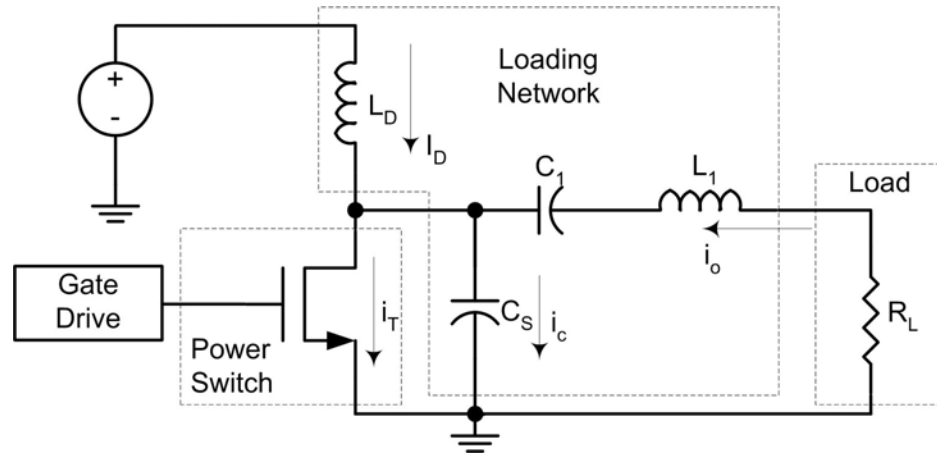


Figure 3.6 Class-E converter schematic

high-current choke) that provides an almost dc current input (I_D) to the converter at steady state, and the current magnitude depends on the power output. When the switch is on, the total current ($I_D + i_o$) flows through the switch. When the switch is turned off, the voltage across the switch builds up slowly due to the parallel capacitor C_0 . This allows ideally a zero-voltage turn-off the switch. The equivalent circuits of the Class-E converter for the switch-on and switch-off states have been shown in Figure 3.7 [57].

Principles for Achieving High Efficiency:

Class-E power amplifiers or converters are generally more efficient than conventional Class-B or Class-C amplifiers. Here, the switching transistor and the loading network combinedly shapes the voltage and current waveforms to prevent simultaneous high voltage and high current in the switch, thus minimizing the power dissipation. This strategy works because of the fact that in most RF and microwave power amplifiers, the largest power dissipation is in the power switch (usually a power BJT or MOSFET). Although it is necessary for the transistor to sustain high voltage and conduct high current during part of the RF period, the circuit can be arranged so that high voltage and high current do not exist at the same time. This ensures that the product of the transistor voltage and current will be low at all times during the RF period [55].

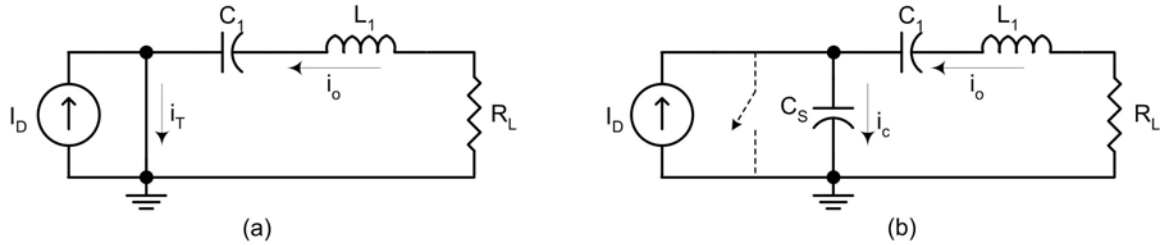


Figure 3.7 Equivalent circuits for the Class-E converter, (a) during ‘on’ state, (b) during ‘off’ state

The condition mentioned above is the key for a successful implementation of Class-E operation of a power amplifier. This can be achieved by realizing the following concepts:

- (i) *During Switch-On State:* The voltage across the switch is nearly zero when the switch is on and high current is flowing. Therefore, a transistor will be needed that acts as low-resistance closed switch during the on state.
- (ii) *During Switch-Off State:* The current through the switch is zero when the switch is off and a high voltage is present across it. Therefore, a transistor will be required that acts almost as an open switch during the off state.
- (iii) *During Switching Transitions:* The rise of the transistor voltage is delayed until after the current has reduced to zero. Similarly, the transistor voltage returns to zero before the current begins to rise. By following these strategies, a high voltage-current product (i.e., power dissipation) can be avoided during the switching transitions, even if the switching times are significant fractions of the RF period.

3.3.2 Driver Design

One of the leading design factors in a Class-E power amplifier or driver design is the loaded Q (Q_L) of the loading network. As already learned, the assumption of a sinusoidal current in L_1 and C_1 is exactly accurate only if Q_L is infinite. Also, the

output power increases as Q_L increases. In fact, the choice of Q_L involves a trade-off among the operating bandwidth (wider with lower Q_L), harmonic content of the output power (lower with higher Q_L) and power loss in the parasitic resistances of the load-network inductor L_1 and capacitor C_1 (lower with lower Q_L) [55]. As the purpose of the proposed inductive link is not only to provide power to the implantable electronics, but also to provide a means for data communication from the internal to the external unit, a high Q_L is not suitable anyway. Therefore, it has been decided to have a Q_L less than 5 as a primary design criterion.

In [55], Sokal presented some explicit design equations for choosing the loading network component values of a Class-E power amplifier for a given load resistance, R (including the equivalent series resistance of the reactive elements and effective resistance of the power device), loaded quality factor of the loading network, Q_L , and operating frequency. Total load resistance seen by the amplifier is calculated as:

$$R = R_L + ESR_{L_1} + ESR_{C_1} + 1.365R_{on} + 0.2116ESR_{C_s} \quad (3.20)$$

where,

R_{on} = On-resistance of the power transistor

ESR = Effective series resistance of a reactive component.

The design equations as presented in [55] are as follows:

$$C_s = \frac{1}{2\pi f R \left(\frac{\pi^2}{4} + 1 \right) \frac{\pi}{2}} \left(0.99866 + \frac{0.91424}{Q_L} - \frac{1.03175}{Q_L^2} \right) + \frac{0.6}{(2\pi f)^2 L_D} . \quad (3.21)$$

$$C_1 = \frac{1}{2\pi f R \left(\frac{1}{Q_L - 0.104823} \right)} \left(1.00121 + \frac{1.01468}{Q_L - 1.7879} \right) - \frac{0.2}{(2\pi f)^2 L_D} . \quad (3.22)$$

$$L_1 = \frac{Q_L R}{2\pi f} . \quad (3.23)$$

Usually, L_D is chosen such that X_{LD} is 30 or more times the unadjusted value of X_{CS} .

Now, in the work presented, the Class-E amplifier does not drive a simple resistive load, rather it drives a transformer loaded with some power management blocks, which are mostly non-linear in nature. However, in order to make use of the design equations mentioned above, an estimation of the load resistance (R_L) that is seen by the primary loading network is required. For estimating the load impedance reflected back to the primary unit, the equivalent secondary impedance has been calculated as a first thing by adopting the following procedure.

Estimation of Equivalent Secondary Impedance:

The equivalent circuit of the secondary unit of Figure 3.5 at dc, assuming negligible ESR for the filter capacitors and that the protection diode D_z is non-conducting, can be drawn as shown in Figure 3.8.

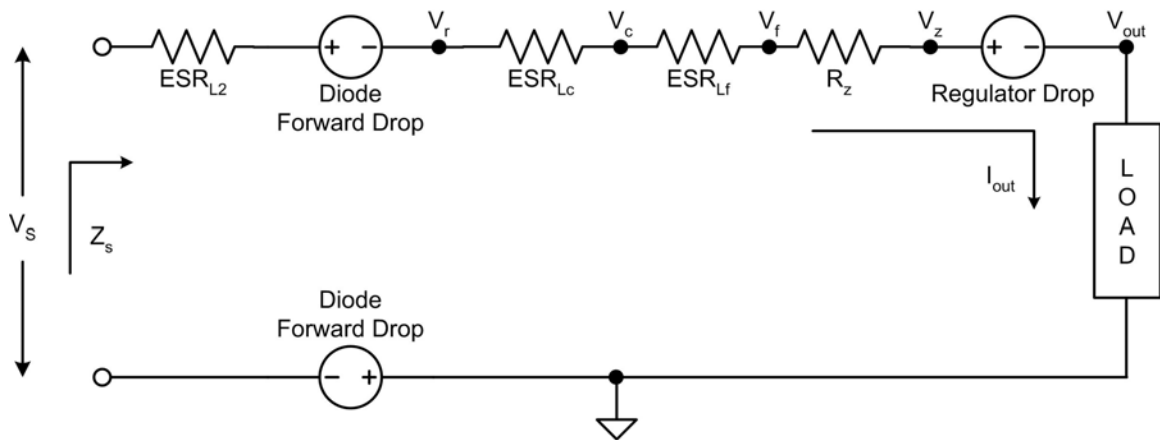


Figure 3.8 Equivalent Secondary Circuit for the Purpose of Primary-referred Load Estimation

The idea behind estimating the equivalent secondary resistance is - the calculation will be started at the output node with the dc output requirements for the intended application, and then the voltages at the previous nodes will be backtracked by considering the voltage drops associated between two consecutive nodes. In this way, the required minimum voltage to be induced at the secondary tank for a given operating condition will be found. Then by dividing that voltage by the current in the circuit will give an approximation of the secondary series resistance.

As might be recalled from section 3.1.5, the dc output requirement is $V_{\text{out}} = 5\text{V}$ at $I_{\text{out}} = 25\text{mA}$. Now the typical dropout voltage for an LT1521-5 regulator is 0.5V for the rated load current. However, to be operated effectively without being interrupted due to possible link parameter variations (such as, misalignment of the coils, change in distance between coils and other ambient environmental causes), an additional 1V drop has been allowed between the input and output of the regulator. This should provide sufficient safety margin at this point. Since the quiescent current of the regulator is very low (12 μA) compared to the load current, it can be assumed that the same load current flows in the series circuit. This should give

Therefore, $V_z = V_{\text{out}} + \text{dropout voltage of the regulator} + 1 = 6.5\text{V}$

$$\begin{aligned} V_f &= V_z + I_{\text{out}}R_z \\ &= 6.5 + 25\text{mA} \times 40\Omega && [R_z \text{ value found from Table 3.2}] \\ &= 7.5\text{V} \end{aligned}$$

Similarly, using the ESR values for L_f and L_c from Table 3.2, the following results are found:

$$V_c = 7.5 + 25\text{mA} \times 1.6\Omega = 7.54\text{V}$$

$$\text{And } V_r = 7.54 + 25\text{mA} \times 53\Omega = 8.87\text{V}.$$

Now, the maximum instantaneous forward voltage of the 1N5819 Schottky rectifier is 0.6V.

$$\therefore \text{Maximum drop across two diodes} = 2 \times 0.6 = 1.2\text{V}$$

Considering this and the voltage drop across the secondary coil's ESR, the minimum rms voltage required across the secondary tank is found to be,

$$V_s (\text{rms}) = 8.87 + 1.2 + 25\text{mA} \times 5.5\Omega = 10.21\text{V}$$

Therefore, the estimated load resistance seen by the secondary coil,

$$R_s = \frac{10.21}{25 \times 10^{-3}} = 408.4\Omega$$

Since the impedance of a parallel resonant circuit is very high, the equivalent impedance of the secondary circuit can be approximated to be,

$$Z_s \approx R_s = 408.4\Omega$$

Calculation of the Primary-referred Load Resistance and Primary Coil Inductance:

Applying transformer principle, the reflected secondary load to the primary side can be found using the following equations:

$$R_L = \frac{(\omega M)^2}{R_s} \quad (3.24)$$

$$\text{where, } M = k\sqrt{L_1 L_2} = \frac{V_s}{\omega I_1} \quad (3.25)$$

$$I_1 = \text{primary coil current (rms)}$$

As one can see from the above relations, equations (3.20) and (3.23), the effective secondary resistance reflected back to the primary side depends on the mutual inductance between the coils and hence on the self-inductance of the primary coil. Again, the choice of primary coil inductance is dependent upon the choice of Q_L and the total resistance seen by the driver (R), of which R_L is a part. There are also other considerations that affect the choice of primary coil inductance. To put

it briefly, designing the loading network for the Class-E amplifier is not a trivial task, and it requires careful considerations of the following issues:

- Q_L of the loading network should not be greater than 5 (as mentioned earlier), which puts some limit on the L_1/R ratio as seen from equation (3.23).
- R_L should take the major portion of R so that the drain efficiency of the amplifier and hence the power transfer efficiency is good. In other words, it prompts the need for a low on-resistance power device and low ESR of the reactive elements. Therefore, the number of turns in the primary coil should not be too many and the coil wire should not be too thin.
- The current in the primary drive circuit can be quite large (several hundred milliamps), so the current-carrying capability of the primary coil wire should also be taken into account. Again, a thicker wire addresses this issue.
- The product of the mutual inductance between the coils, the primary current and the operating frequency should be sufficiently large to provide the required induced voltage at the secondary tank.

It is therefore understandable that the selection of the coil inductance and loading network parameters is an iterative process, and judicious choices need to be made in every step.

One of the topmost priorities in the link design process was achieving a high coupling factor for the inductive link, as its importance is discussed in section 3.1.5. The next thing that has been done is putting a large number of turns in the secondary coil within the physical limits. This was comparatively easy, because the current in the secondary unit is much lower, and a thinner (AWG #30) wire has been used. The ESR of the secondary coil was also not a big issue. This allowed having ample self-inductance in the secondary coil (267 μ H) as well as the

provision of obtaining a high mutual inductance without being required to put too many turns in the primary coil.

Now, a starting Q_L of 5 is assumed for making the initial choice of L_1 . For an operating frequency of 200kHz, equation (3.23) yields,

$$\frac{R}{L_1} = \frac{2\pi f}{Q_L} = 251.33 \times 10^3 .$$

And choosing $R = 2\Omega$ yields $L_1 = 7.96\mu\text{H}$.

A primary coil was built using AWG #18 wire that provided an inductance of $5.8\mu\text{H}$; but to have an inductance closer to calculated L_1 , a conformal coated inductor of $1.6\mu\text{H}$ has been added, which resulted in a total inductance of $7.4\mu\text{H}$ and an ESR of 0.29Ω at 200kHz as already mentioned in Table 3.1. Substituting this value along with L_2 and k as found earlier in equation (3.25) gives,

$$M = 0.453\sqrt{7.4 \times 10^{-6} \times 267 \times 10^{-6}} = 20.14\mu\text{H} .$$

Using this result in equation (3.24) yields,

$$R_L = 1.57\Omega .$$

High-current, high Q polypropylene capacitors have been chosen for using in the primary circuit. These capacitors have ESRs on the order of 0.024Ω . If a low on-resistance power MOSFET with $R_{\text{on}} = 0.1\Omega$ is selected, then plugging these values into equation (3.20) provides,

$$R = 1.57 + 0.29 + 0.025 + 1.365 \times 0.1 + 0.2116 \times 0.025 = 2.03\Omega .$$

Now, using the adjusted values of R and L_1 , Q_L is calculated again by equation (3.23):

$$Q_L = \frac{2\pi f L_1}{R} = 4.58 ,$$

which is an acceptable value for the loaded Q .

Calculation of the Rest of the Loading Network Parameters:

A high-current high-inductance toroidal RF choke has been chosen as L_D . For this part, $L_D = 481\mu\text{H}$. Substituting this value and the calculated results for R and Q_L in equations (3.21) and (3.22) yield respectively,

$$C_S = 83.5\text{nF}$$

and $C_1 = 119.3\text{nF}$.

Now, $X_{CS} = 9.53\Omega$ and $X_{LD} = 604.44\Omega$ at the 200kHz operating frequency. This calculation verifies that the chosen value for L_D makes X_{LD} greater than X_{CS} by a factor well above 30, thus meeting one of the design requirements discussed earlier.

This completes the design of the Class-E primary coil driver and its loading network.

3.3.3 Gate Drive Circuit for the Power MOSFET

The only thing remaining towards the realization of a complete inductive powering system is the gate drive circuit for the active device switch; a power MOSFET in this case. A 200kHz square wave signal with sufficient amplitude and low rise and fall times is ideal for driving the gate of such a device that can quickly turn on and off the switch, and thus reducing the power dissipation during switching transitions. However, it may be recalled from the discussion in the previous section that a low on-resistance switching device is essential in order for achieving an efficient Class-E operation. Consequently, a larger device is needed, which means higher gate capacitance, higher charging current requirement for obtaining sharp rising and falling edges of the gate signal, and hence higher power dissipation. Following simple calculations will give an idea about the implications of high gate capacitance associated with larger devices.

It is known that, $Q = CV$ or, $I = \frac{CV}{t}$ for constant current charging.

If the rise or fall time is chosen to be 2% of the RF period, then

$$t = 0.02T = 100\text{ns}.$$

The typical on-resistance of the IRFD120 power MOSFET is 0.27Ω and the input capacitance is 360pF .

Therefore, for a target gate voltage of 5V and a rise time of 100ns the charging current required is

$$I = \frac{360\text{pF} \times 5\text{V}}{100\text{ns}} = 18\text{mA}$$

On the other hand, the on-resistance and input capacitance of IRF59N10D are 0.025Ω and 2450pF respectively. So, for the same gate voltage and rise time, this device requires

$$I = 122.5\text{mA!}$$

The increase in efficiency achieved through a lower on-resistance will probably not circumvent the power loss associated with this high gate drive current. Therefore, careful considerations should be given while choosing the switching device. As far as this particular work is concerned, the IRFD120 will most likely be the wiser choice between the two.

It is possible to infer from the foregoing discussions that a current buffer stage will be required anyway following the timing generator circuit because of the considerably high gate drive requirements.

The circuit arrangements shown in Figure 3.9 have been used to generate the gate drive signal for the power MOSFET.

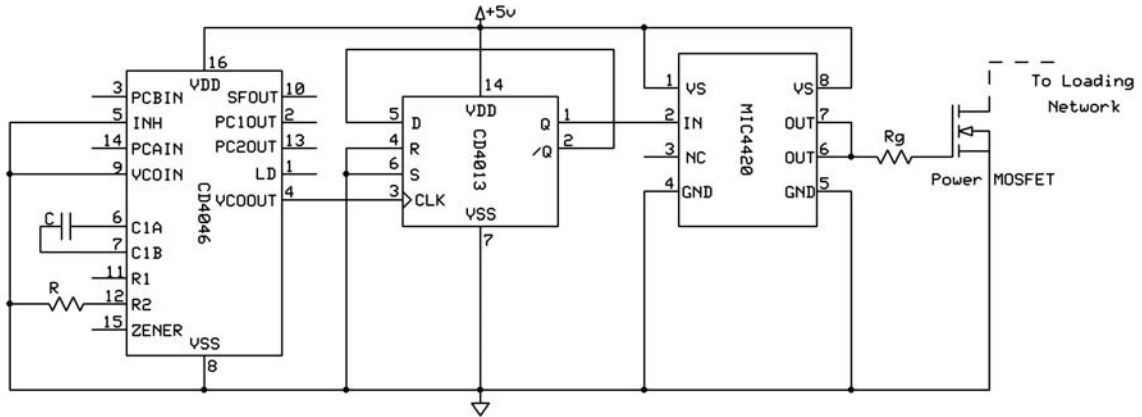


Figure 3.9 Schematic diagram of the gate drive circuit

The CD4046 phase-locked loop chip has been configured as a free-running voltage-controlled oscillator (VCO). The timing resistor (R) and capacitor (C) values have been chosen such that the VCO generates a 400kHz square wave signal with the VCOIN pin at 'low'. The following equation can be used as a design guide to choose the component values:

$$f = \frac{1}{R(C + 32\text{pF})} \quad [\text{when VCO input} = V_{\text{ss}}]$$

Where, the conditions $10\text{k}\Omega \leq R \leq 1\text{M}\Omega$ and $100\text{pF} \leq C \leq 0.01\mu\text{F}$ should be met for the proper operation of the device.

The output of the VCO has been connected to the 'CLK' input of a divide-by-2 ripple counter that gives a 200kHz square wave at its output. The reason for using the frequency divider is to obtain a duty cycle as close as 50%. Usually, the VCO cannot provide a 50% duty cycle, but this is a desirable feature for the gate drive signal. The frequency divider has been implemented by connecting the \bar{Q} to D of a CD4013 D-type flip-flop. Finally, a low-side non-inverting MOSFET driver (MIC4420) has been used to provide sufficient current with the gate drive signal to quickly charge the gate capacitance of the power MOSFET. A small resistance, R_g (usually $10\text{-}50\Omega$) has been used between the output of the MIC4420 and the gate of the MOSFET in order for minimizing the sharp current glitches in the

switching transients. This is particularly important for the performance of the data communication system, where the switching noises can greatly affect the reliability and even the workability of the system.

3.3.4 List of Primary Powering Unit Components

The actual component values and parts used in the implementation of the primary (external) unit of the inductive powering system have been listed in Table 3.3.

3.4 Simulation Results

SPICE simulations have been performed for the complete inductive powering system. For simulation purpose, the link has been modeled by a transformer using the calculated coupling factor and measured primary and secondary coil inductances. Manufacturer-supplied SPICE macromodels have been used for the parts IRFR3710Z (which is similar to IRF540Z), 1N4739A, 1N5819HW and LT1521 (output voltage is 3.75V instead of 5V of LT1521-5). The gate drive circuit has not been included; rather a pulse source has been used with comparable rise and fall times. All other component values were taken from Table 3.1 and 3.2. The external unit's supply voltage was fixed at 5V and the internal unit's regulated output was connected to a 200 Ω load resistance. The simulations have shown that the system becomes well tuned at 228.3kHz and produces near-perfect Class-E waveforms. Therefore, all simulation results presented in this section (Figures 3.10 through 3.16) correspond to an operating frequency of 228.3kHz.

Table 3.3 Primary Powering Unit Component List

Component	Part No. / Value	Description	Features/Comments
Transmitter / Transformer Coil, L_1	7.4 μ H	Hand-wound coil	ESR = 0.29 Ω , Q = 32 @ 200kHz
Series Resonant Capacitor, C_1	120nF	Polypropylene Capacitor	ESR = 0.025 Ω
Parallel Capacitor across the Switch, C_s	100nF	Polypropylene Capacitor	ESR = 0.025 Ω
High-Inductance Choke, L_D	481 μ H	Toroidal RF Choke	ESR = 7.1 Ω
Power Device Switch	IRFD120/ IRF540Z	N-Channel Power MOSFET	$R_{on} = 0.27\Omega/0.0265\Omega$, $V_{DSS} = 100V$, $I_D = 1.3A/36A$
Voltage-Controlled Oscillator	CD4046B	Micropower Phase-Locked Loop	$V_{DD} = 3V$ to 18V, Maximum VCO Frequency = 0.7 MHz with $V_{DD} = 5V$
D Flip-Flop	CD4013	Micropower D Flip-Flop	$V_{DD} = 3V$ to 18V
MOSFET Driver	MIC4420	Low-side MOSFET Driver	Peak O/P Current = 6A, Rise & Fall time = 25ns

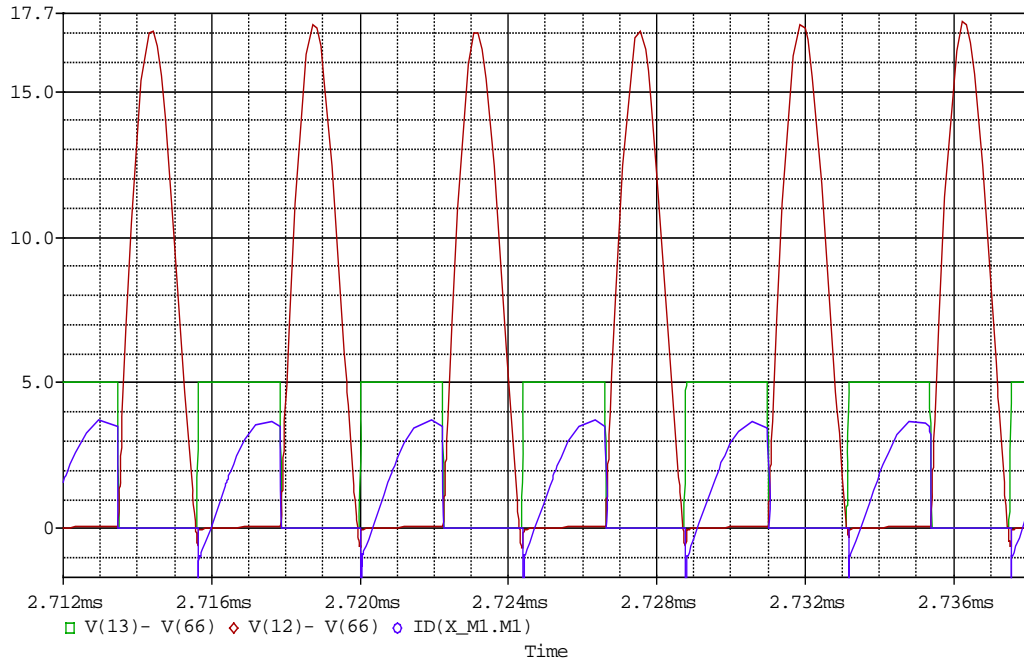


Figure 3.10 Gate voltage [V(13, 66)], drain voltage [V(12, 66)] and drain current [ID(X_M1)] of the power MOSFET

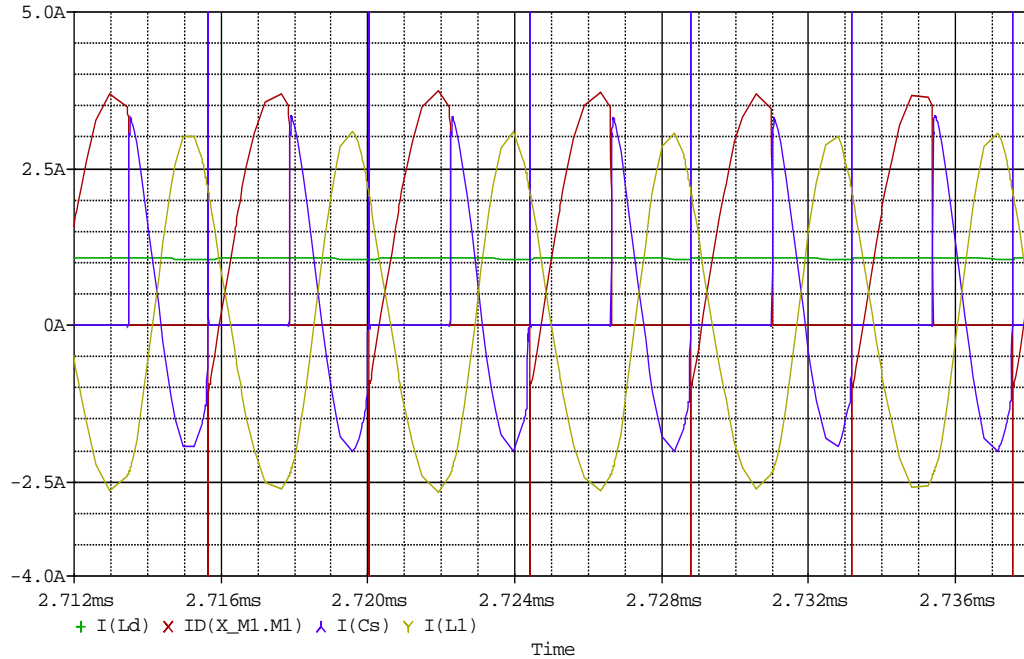


Figure 3.11 Currents through primary choke [I(Ld)], power MOSFET [ID(X_M1)], MOSFET's parallel capacitor [I(Cs)] and primary coil [I(L1)]

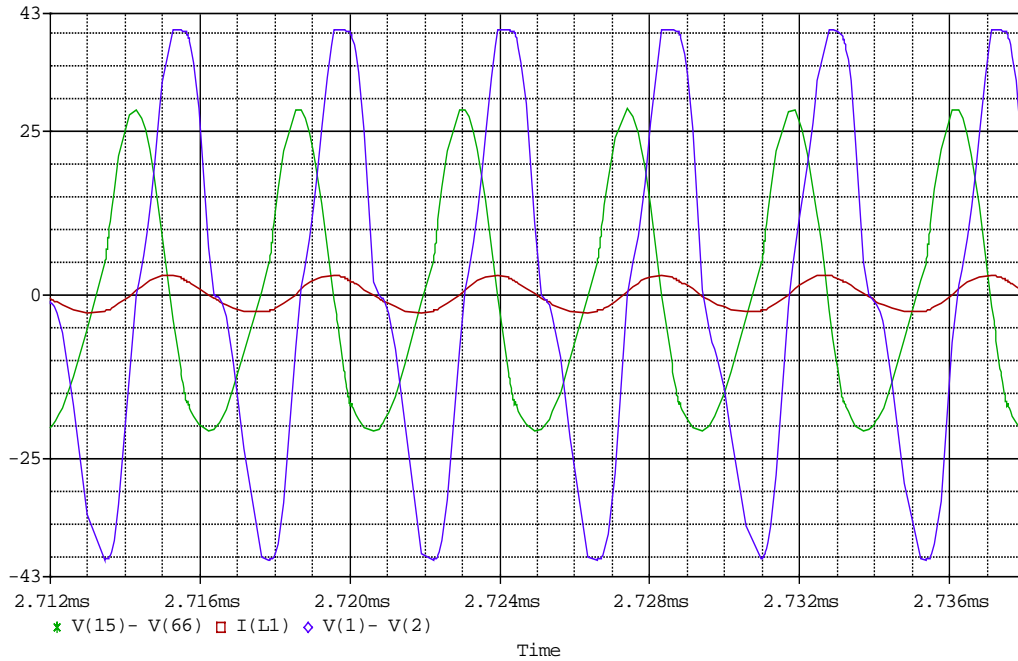


Figure 3.12 Primary coil voltage [V(15, 66)], primary coil current [I(L1)] and secondary coil's induced voltage [V(1, 2)]

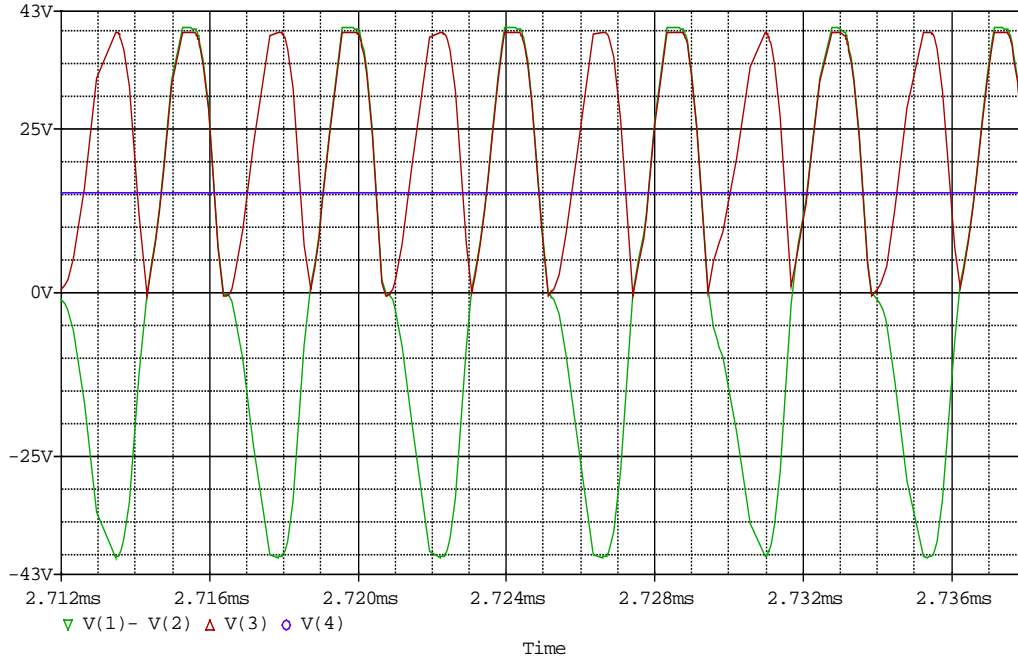


Figure 3.13 Secondary coil voltage [V(1, 2)], rectifier output voltage [V(3)] and secondary choke output voltage [V(4)]

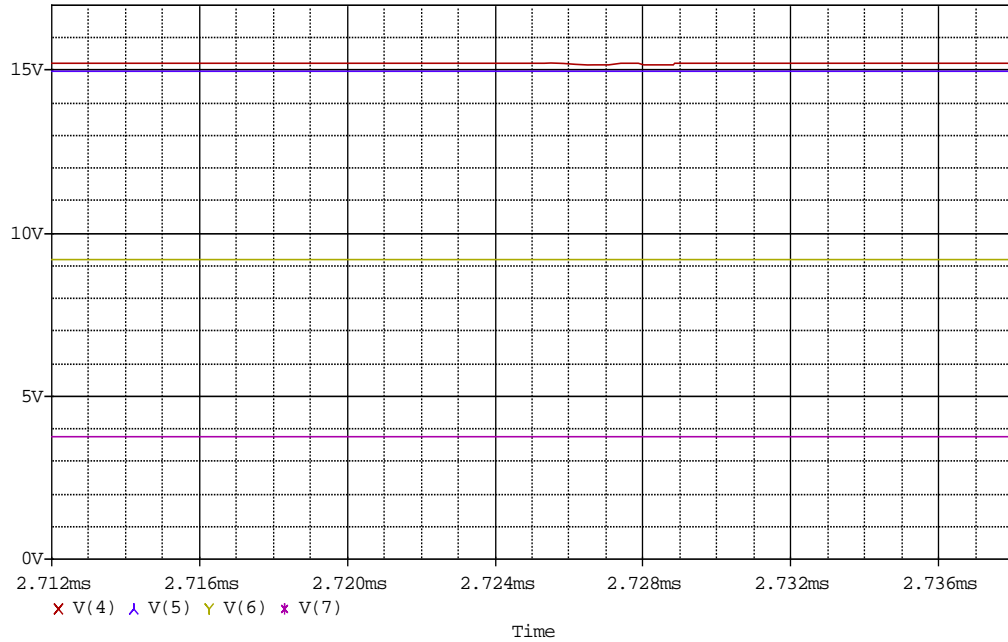


Figure 3.14 Voltages at the secondary choke output [V(4)], Π -Filter output [V(5)], Zener diode [V(6)] and the regulator output [V(7)]

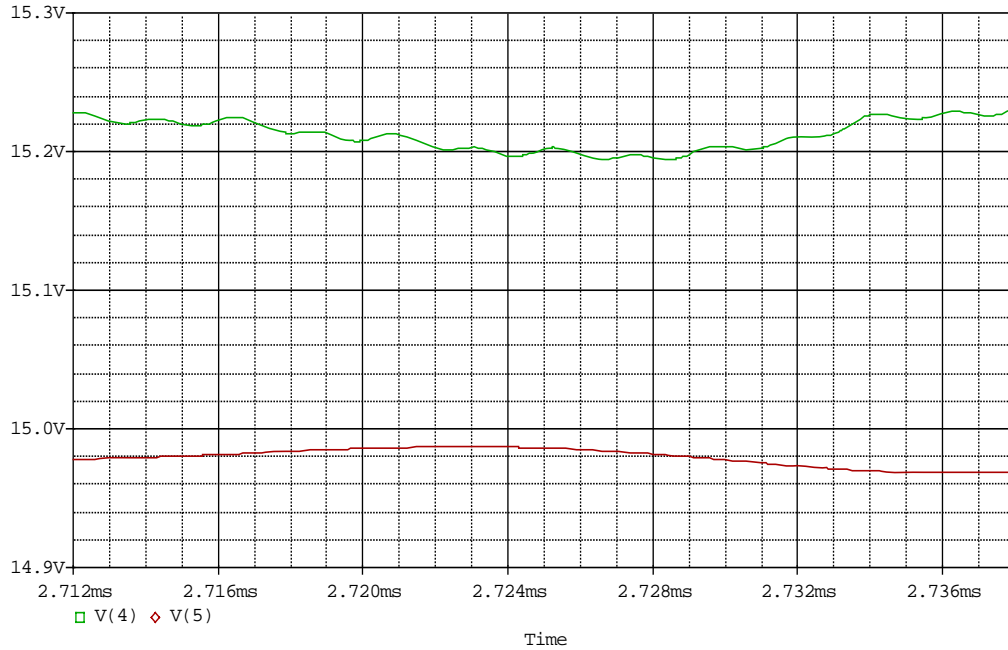


Figure 3.15 Ripple content at the secondary choke output [V(4)] and Π -Filter output [V(5)]

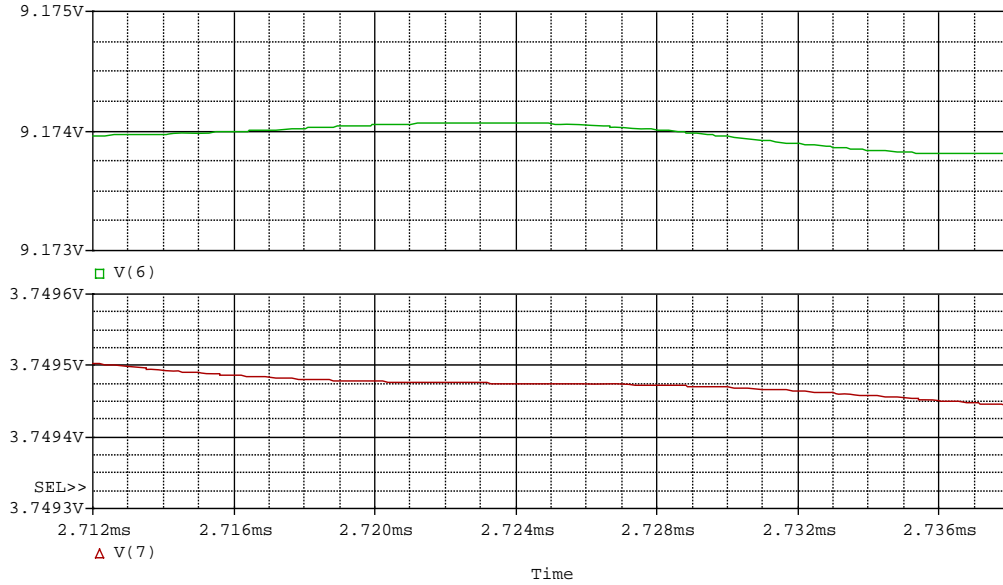
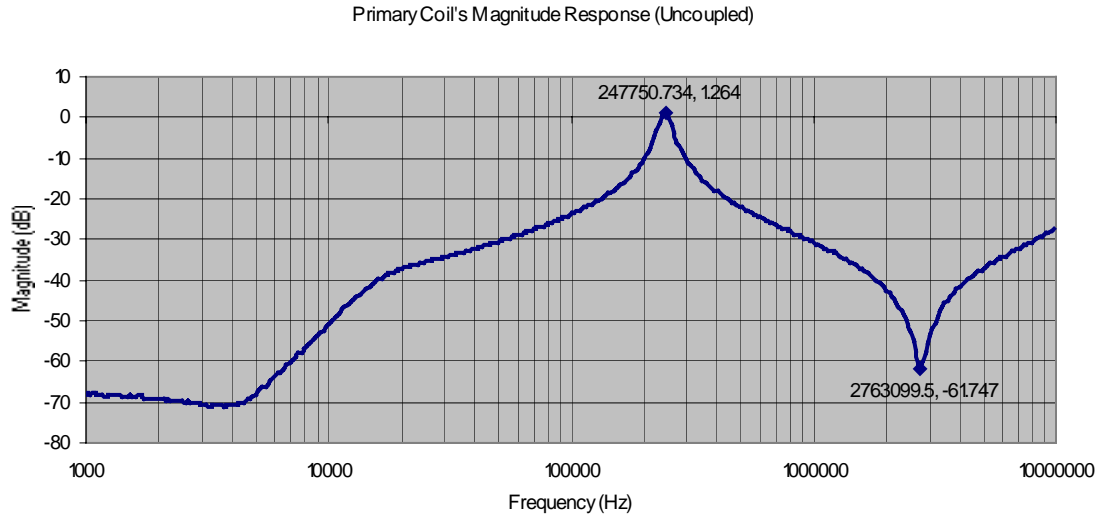


Figure 3.16 Ripple content at the clamp [V(4)] and final regulator output [V(5)]

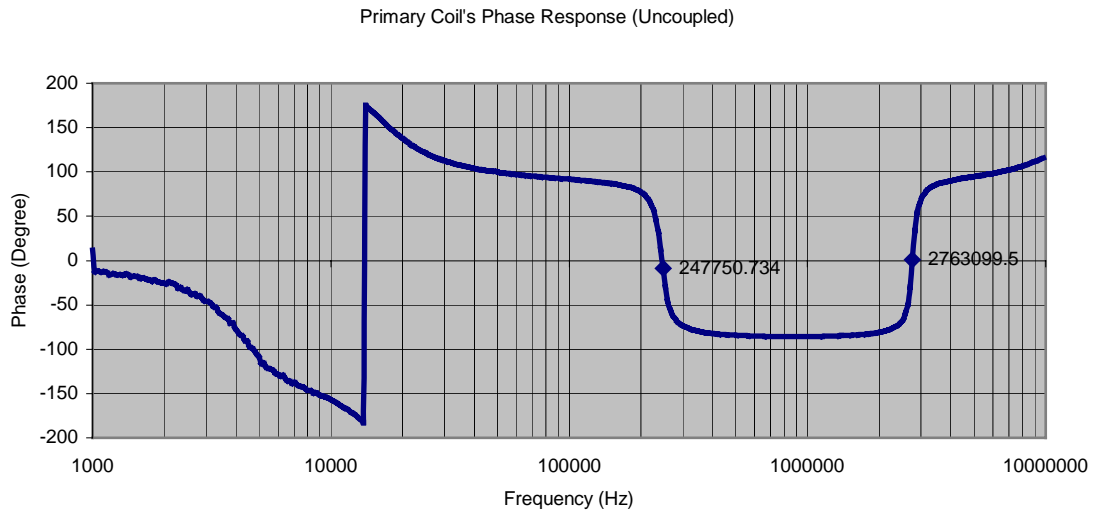
3.5 Test Results

3.5.1 Frequency Response Curves

Frequency response of the inductive powering system has been obtained using the HP3589A Network/Spectrum Analyzer. For the purpose of measurements, the active power switch of the Class-E amplifier has been taken off and the source of the network analyzer has been connected across C_s (refer to Figure 3.7). The source amplitude has been set such that it does not overload the analyzer. The dc power supply to the external unit has been replaced by a ground. Then a frequency sweep has been performed from 1kHz to 10MHz. Total number of data points was set to 400 by default. Several sets of data have been taken for the uncoupled and coupled primary coil, the secondary coil and the low-pass filter of the secondary power recovery unit. The data were then transferred to a PC through the GPIB ports and by a custom program written in LabVIEW. Finally, the measured data were plotted in Microsoft Excel to generate the corresponding Bode plots. Appropriate plots are presented in Figures 3.17 through 3.20.

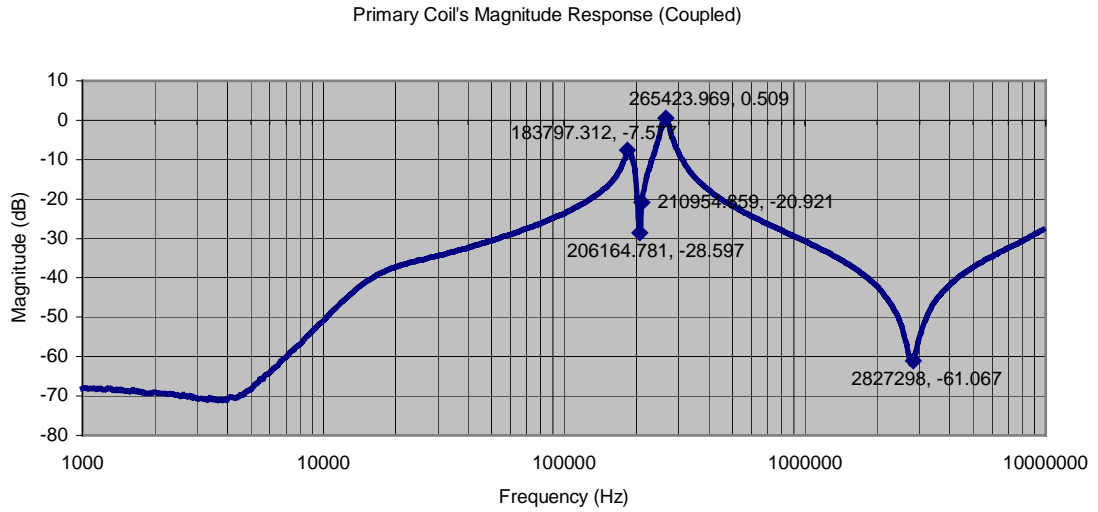


(a)

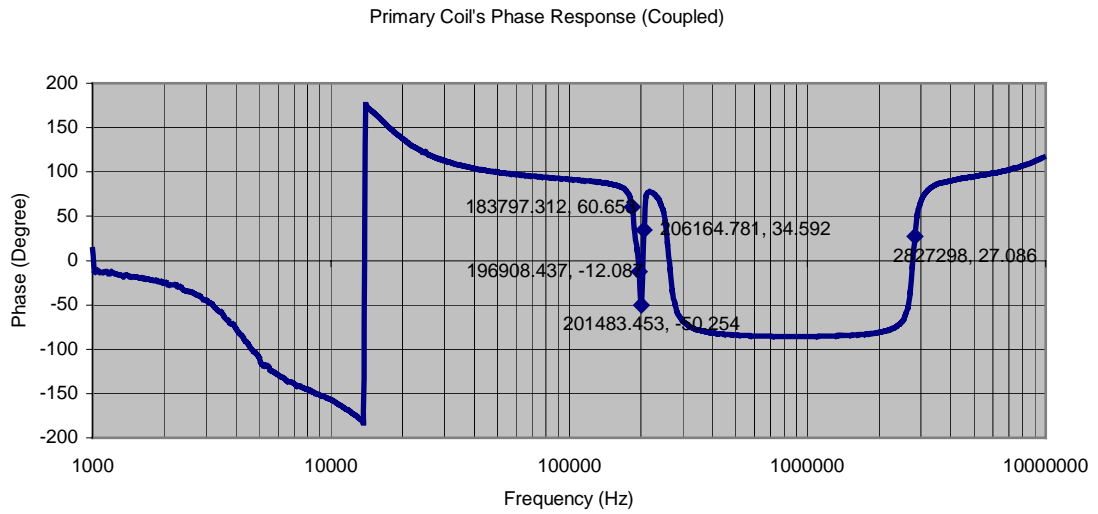


(b)

Figure 3.17 Bode plots for the uncoupled primary coil: (a) Magnitude response, (b) Phase response

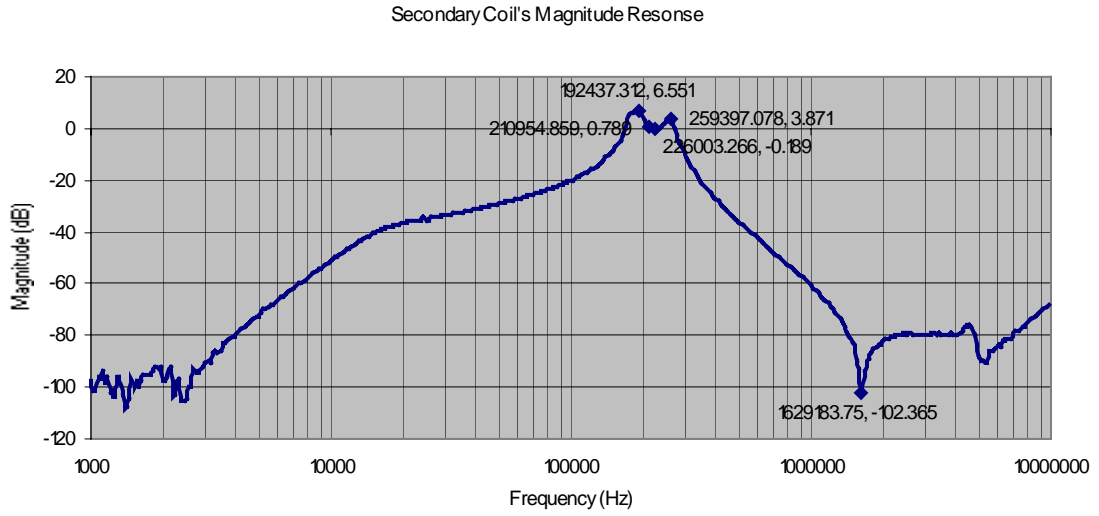


(a)

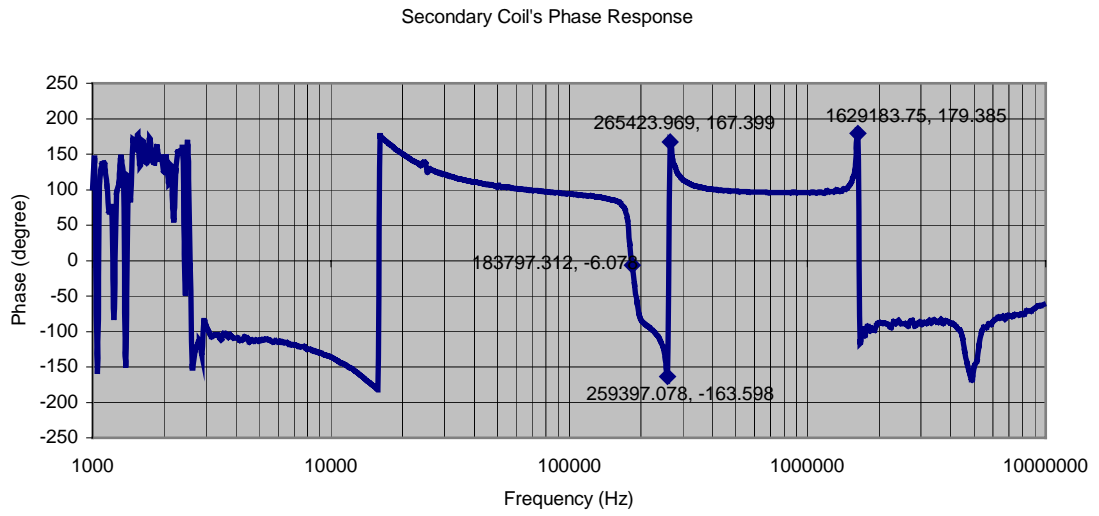


(b)

Figure 3.18 Bode plots for the coupled primary coil: (a) Magnitude response, (b) Phase response



(a)



(b)

Figure 3.19 Bode plots for the coupled secondary coil: (a) Magnitude response, (b) Phase response

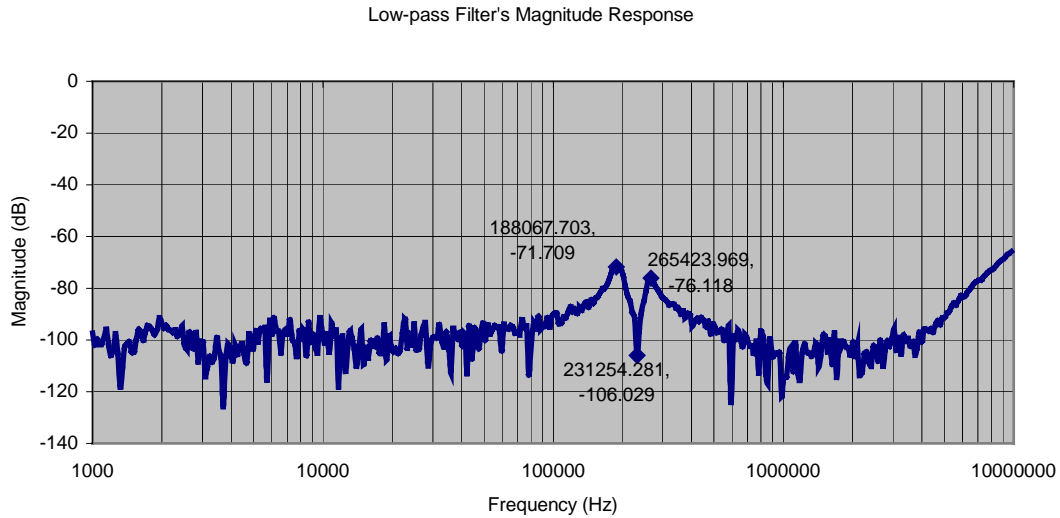


Figure 3.20 Magnitude plot for the secondary unit's low-pass filter

3.5.2 Transient Response Curves

Time domain measurements were performed using a Tektronix TDS 5054 Digital Phosphor Oscilloscope. Several sets of tests were performed by varying frequency, supply voltage and coupling. In this section, some captured waveforms at an operating frequency of 211.8kHz are presented. The first five screenshots (Figures 3.21 through 3.25) show the Class-E converter's waveforms, i.e. the voltages across the gate and drain of the active switch, at five different frequencies. These figures show the differences between the key voltage waveshapes of a perfectly tuned amplifier and those of a mistuned amplifier. As will be seen, the Class-E amplifier is considerably mistuned at frequencies 184kHz and 195.kHz, while they are operating in almost ideal condition at 206kHz and 208kHz, and it is, perhaps, very slightly deviated from the ideal Class-E mode at 212kHz. However, experiments showed that the whole system operates most efficiently for a given test condition at 212kHz, which is most likely due to the least amount of negative overshoot present in the drain voltage during switch-on time. All other waveforms presented in this section are obtained at 212kHz (Figures 3.26 through 3.29).

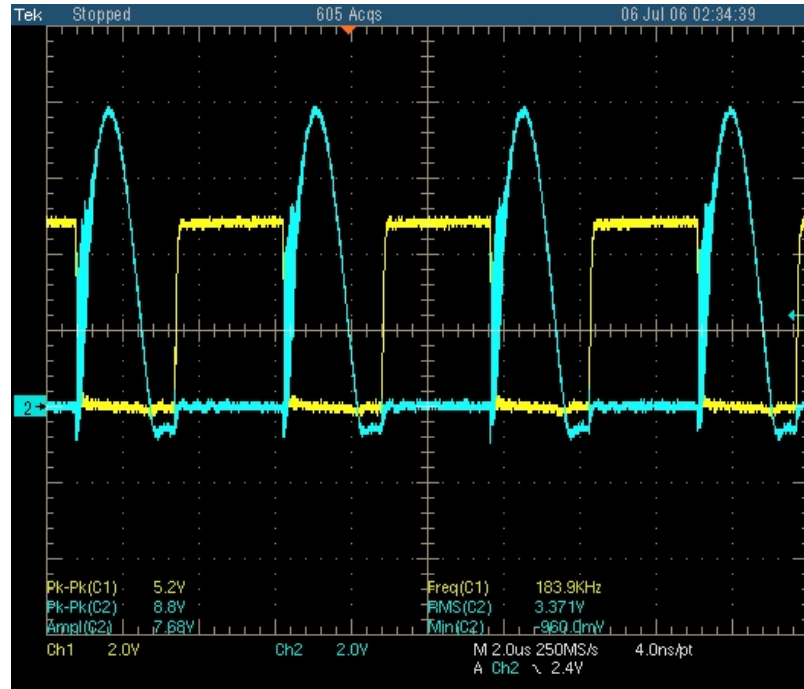


Figure 3.21 Class-E voltage waveforms of the power MOSFET at 184kHz: Gate voltage (yellow) and drain voltage (blue)

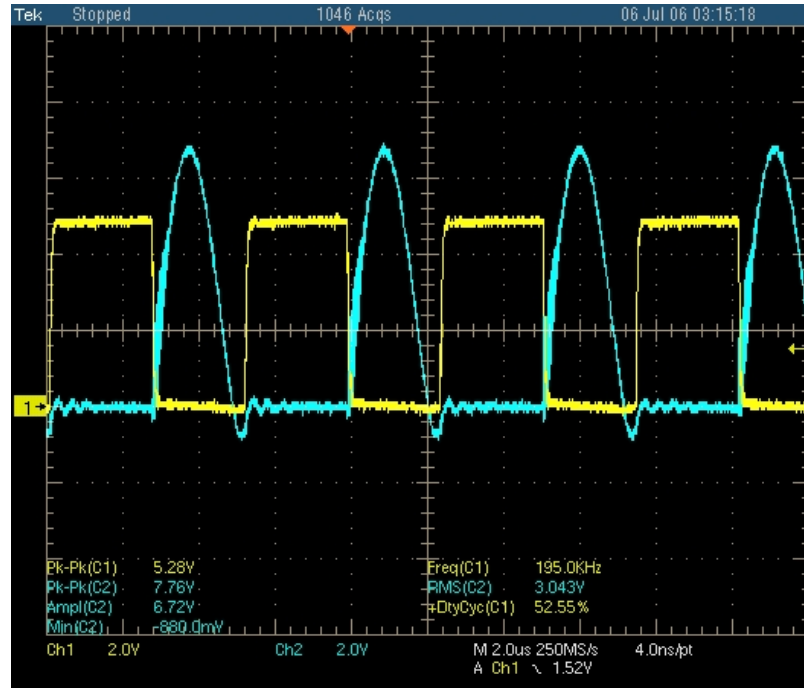


Figure 3.22 Class-E voltage waveforms of the power MOSFET at 195kHz: Gate voltage (yellow) and drain voltage (blue)

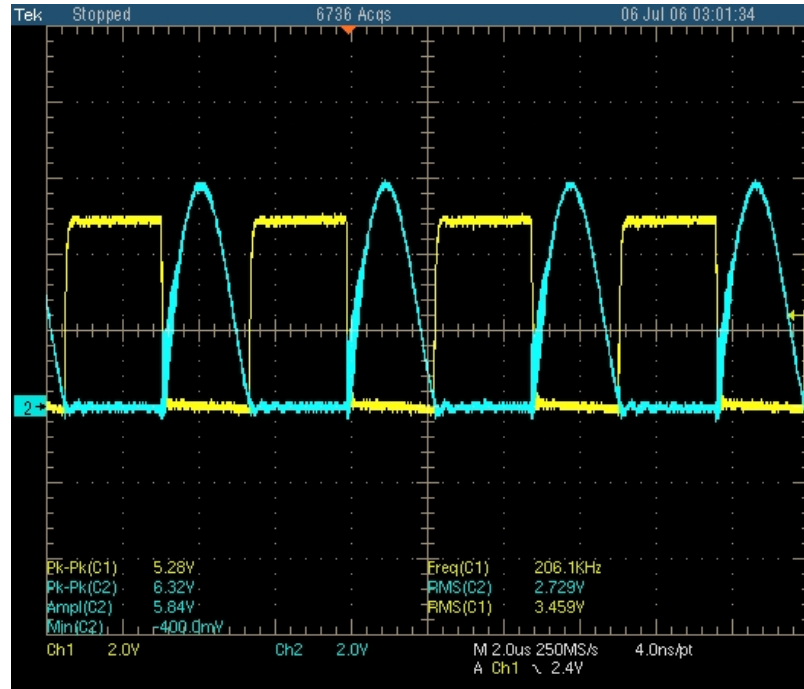


Figure 3.23 Class-E voltage waveforms of the power MOSFET at 206kHz: Gate voltage (yellow) and drain voltage (blue)

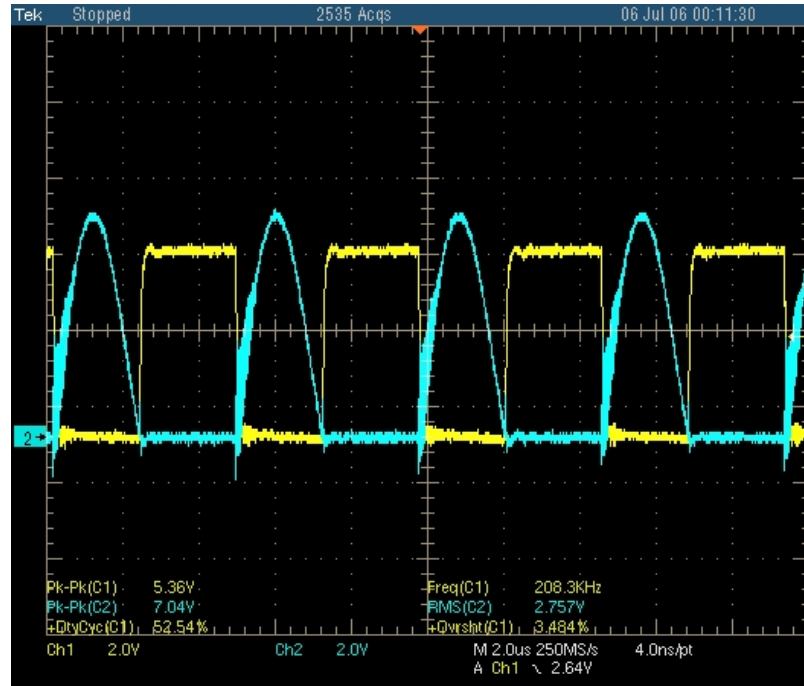


Figure 3.24 Class-E voltage waveforms of the power MOSFET at 208kHz: Gate voltage (yellow) and drain voltage (blue)

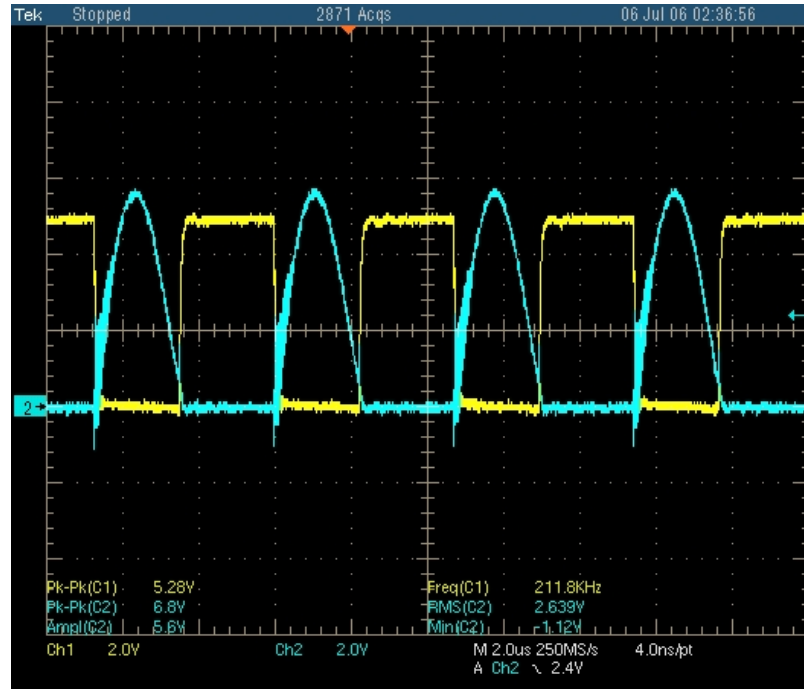


Figure 3.25 Class-E voltage waveforms of the power MOSFET at 212kHz: Gate voltage (yellow) and drain voltage (blue)

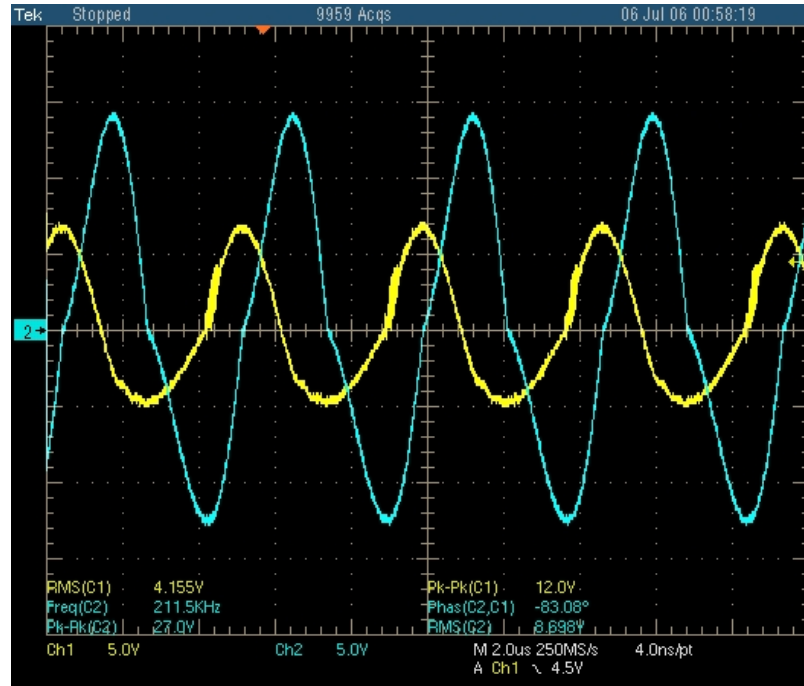


Figure 3.26 Voltages across the primary coil (yellow) and secondary coil (blue)

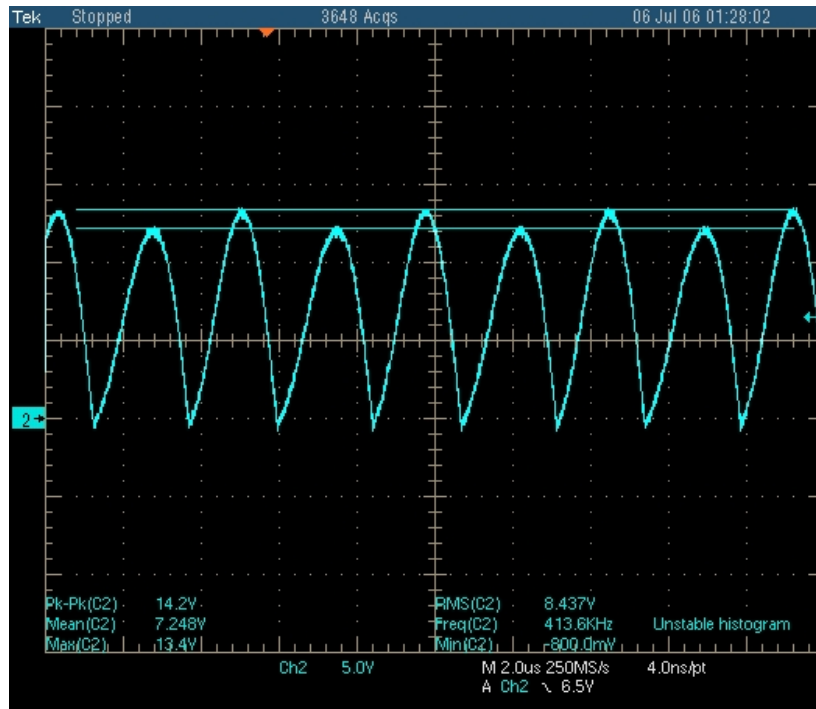


Figure 3.27 Rectifier output voltage

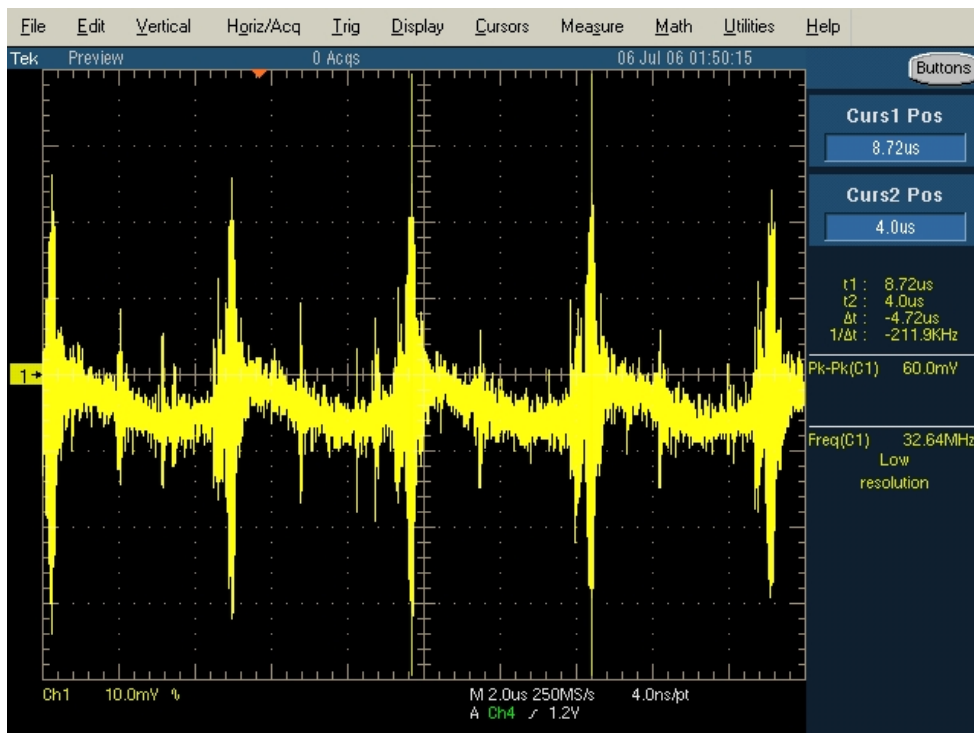


Figure 3.28 Low-pass filter output voltage (ac-coupled)

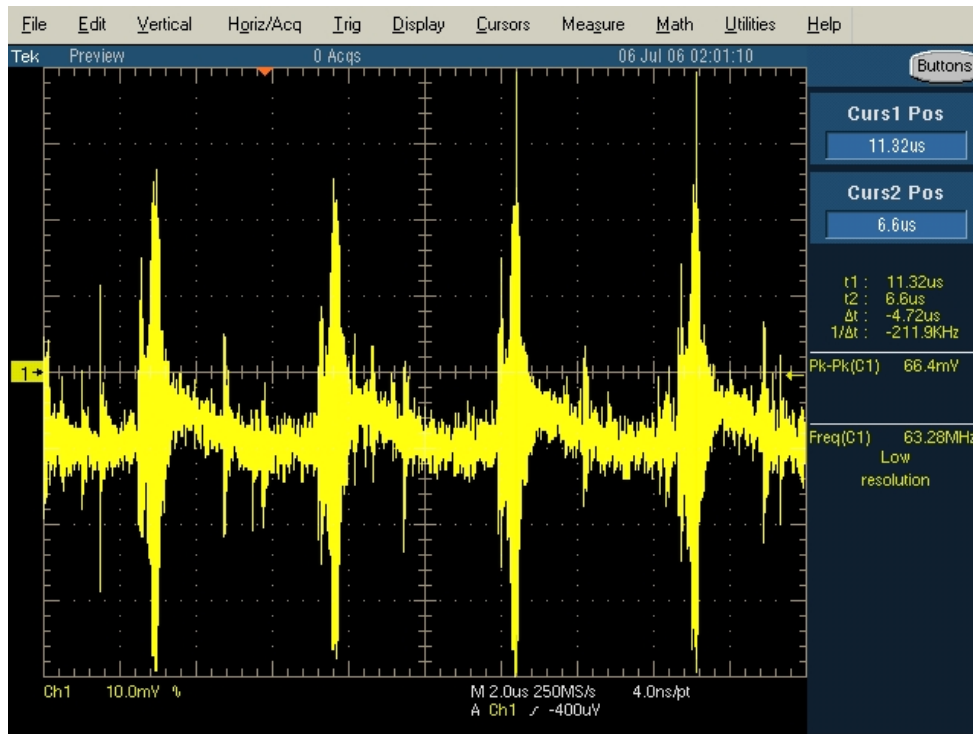


Figure 3.29 Regulator output voltage (ac-coupled)

Discussions: Some clarification is needed about Figures 3.28 and 3.29. These screenshots show the ac noise present in the output dc voltage. By careful observation of these figures, the frequency of the dominant ac component is found to be 212kHz, which is the frequency of operation. However, the rectifier output contains ripple of twice the operating frequency (i.e., 424kHz), which has certainly been diminished beyond the measurable limit, as the cutoff frequency of the low-pass L-C filter was set at only 12kHz. The regulator is supposed to further reject the ripple with its 10 μ F output capacitor. Therefore, a reasonable explanation is, this noisy behavior must have been resulted from the free-air radiation of the coils. It must be considered that the coils are quite large, and the secondary coil's inductance is 267 μ H that can easily induce voltages more than 50V_{p-p}. Fortunately, the magnitude of this interference is very low, around 10mV_{p-p} except for the spikes, and this is acceptable for most of the applications. However, if any need arises to eliminate the noise, suitable shielding techniques can be applied.

3.5.3 Measured Data and Analysis

Tests have been performed to measure inductive powering system data so that its performance can be analyzed. Following test conditions apply to these measurements:

- Separation between primary and secondary coil, $D = 1.16\text{cm}$.
This is close to the target distance of 1cm.
- Main supply voltage = 5V.
- A 1A low dropout adjustable voltage regulator (REG1117A from Burr-Brown/Texas Instruments) has been used in the final prototype PCB for the external unit, where its input has been connected to the main supply and the output serves as the V_{DD} for the Class-E driver circuit. However, the gate drive unit is directly connected to the main supply or battery, because the minimum voltage required for that unit is 4.5V. The use of the adjustable regulator provides the flexibility to manually adjust the primary coil current, and hence to optimize for gain, output power or efficiency. For these sets of tests, primary unit voltage regulator's output was set to 1.76V. This is the minimum voltage for which the system works within the test frequency range.
- Test frequency range: 184 to 212kHz.
Within these two limits, the Class-E amplifier works in either optimum or sub-optimum mode (as already discussed in the previous section) and delivers useful power to the internal unit. Although the experimental frequency response curves show another resonant frequency at around 265kHz, the Class-E amplifier was not originally designed to operate at that frequency. Naturally, the amplifier becomes completely mistuned (i.e., the switch turns on much before the drain voltage reaches zero), and too much loss occurs in switching transitions and even during the turn-on time. Therefore, the input voltage to the secondary unit's regulator falls below the minimum required voltage.

- Duty cycle of the gate drive signal = 52.5%.
Despite the efforts for achieving a 50% duty cycle, this slight discrepancy is observed, which is most likely due to the inaccuracy in the high-current MOSFET driver. However, this slight difference is not an issue for efficient power transfer.
- Switching device used: IRF540Z
- RMS voltage across the series resistance (R_g) at the MOSFET gate = 0.36V.
 $R_g = 10\Omega$
- Internal unit's load resistance, $R_L = 200\Omega$

The test results are presented in Table 3.4.

Calculations: Now, in order to determine various efficiencies, some calculations and estimations are required. First of all, the charging current to the input capacitance of the power MOSFET has been estimated as,

- $I_{\text{charge}} = \frac{0.36}{10} = 36\text{mA}$, which should be constant as long as the supply voltage to the gate drive unit is fixed.

The connection diagram used for adjusting the regulator output voltage has been shown in Figure 3.30 (as provided by the REG1117 datasheet).

Table 3.4 Test Data for the Inductive Powering System

Frequency of Operation (kHz)	Supply Current, DC (A)	Switch Voltage, Peak (V)	Primary Coil Voltage, RMS(V)	Secondary Coil Voltage, RMS (V)	Filter Output Voltage, DC (V)	Regulator* Input Voltage, DC (V)	Regulator* Output Voltage, DC (V)
183.8	0.70	7.8	8.63	16.2	10.6	8.6	5
195.0	0.47	6.8	5.90	13.6	10.4	8.8	5
206.1	0.28	5.8	4.38	12.2	8.0	6.7	5
211.9	0.20	5.6	4.16	8.7	7.3	6.3	5

* Secondary unit's regulator: LT1521-5

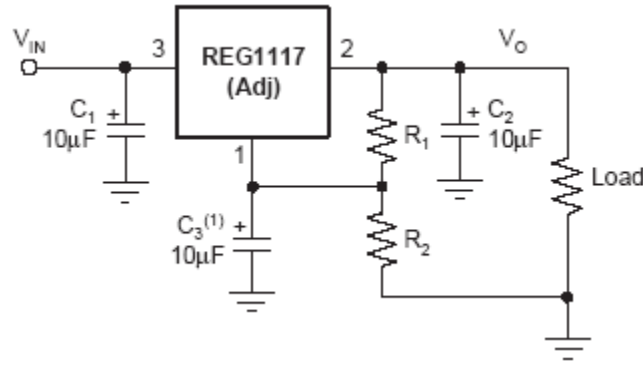


Figure 3.30 Basic connections for adjustable voltage

The typical reference voltage between pin 1 and 2 is 1.25V and the adjustable pin current for the load condition is 0.5µA (as found from the datasheet). $R_1 = 331 \Omega$ and a 1k potentiometer for R_2 have been used, so that the output voltage can be easily varied. Therefore, the current drawn by the regulator's output resistors is calculated as,

- $I_{\text{reg}} = \frac{1.25}{331} + 0.5\mu\text{A} = 3.78\text{mA}$, which satisfies the minimum load current required for the regulator.

Total quiescent/supply current to the power MOSFET driver (MIC4420), D flip-flop (CD4013) and VCO (CD4046) has been estimated as,

- $I_S = 3\text{mA} + 1\text{mA} + 1\text{mA} = 5\text{mA}$ (based on the datasheet values).

If I_{charge} , I_{reg} and I_S are subtracted from the total dc supply current, that gives the net current to the primary coil driver unit.

- For the internal RF unit regulator, the ground current is very small compared to the load current of $5\text{V}/200\Omega = 25\text{mA}$, so it is neglected. Therefore, the input and output currents of the regulator are assumed to be same to simplify the analysis.

- The current through the clamp resistor (R_z) can be found by taking the difference of filter output voltage and regulator input voltage (columns 6 and 7 of Table 3.4), and then dividing it by R_z . The value of R_z is 40Ω as found from Table 3.2. The difference between this current and the regulator current provides the current through the Zener diode, D_z .
- The same current flows through the filter inductors of L_c and L_f , neglecting the very little leakage current through the capacitors. Therefore, the voltage drop across these inductors can be found by the product of their current and the total ESR of the two filter inductors, which is 13Ω , as obtained from Table 3.2.
- The total current in the secondary unit is shared almost equally by the two rectification branches. Therefore, the current through each rectifier diode can be estimated by dividing the total current by 2. The maximum instantaneous voltage across each rectifier diode is $0.6V$, as found in the datasheet, and verified during experiments. The average voltage across each rectifier can thus be estimated as $0.6V/\pi = 0.19V$. Hence, the ac power dissipation in the rectifier diodes can be calculated by the product of their voltage and current.
- Finally, the resistive loss (ac) in the secondary coil can be approximated using the I^2R formula, where $R = \text{ESR of the secondary coil} = 5.5\Omega$.

The results obtained based on these calculations and associated assumptions are presented in Tables 3.5 and 3.6.

Now, several efficiency values have been computed. In order to estimate the link efficiency, the primary-to-secondary power conversion efficiency has been divided by the drain efficiency of the Class-E driver.

Table 3.5 Calculations of Currents and Powers for the Primary Unit

Frequency of operation (kHz)	Total supply current, I_{supply} (A)	Current to Class-E amplifier including gate drive current, $I_{\text{supply}} - I_{\text{reg}}$ (A)	Current to Class-E amplifier excluding gate drive current, $I_{\text{supply}} - I_{\text{reg}} - I_{\text{s}} - I_{\text{charge}}$ (A)	Total input power, P_{in} (W)	Net input power to Class-E amplifier including gate drive, P_{driver} (W)	Net input power to Class-E amplifier excluding gate drive, P_{amp} (W)
183.8	0.70	0.696	0.655	3.50	1.36	1.15
195.0	0.47	0.466	0.425	2.35	0.95	0.75
206.1	0.28	0.276	0.235	1.40	0.62	0.41
211.9	0.20	0.196	0.155	1.00	0.48	0.27

Table 3.6 Calculations of Currents and Powers for the Secondary Unit

Frequency of operation (kHz)	Load current, I_{L} (mA)	Current in R_{z} , I_{R} (mA)	Zener diode current, I_{D} (mA)	Secondary dc losses, $P_{\text{loss_dc}}$ (W)	Secondary ac losses, $P_{\text{loss_ac}}$ (W)	Power delivered to load, P_{load} (W)	Power converted to secondary coil, $P_{\text{secondary}}$ (W)
183.8	25	50.0	25.0	0.438	0.033	0.125	0.596
195.0	25	40.0	15.0	0.312	0.024	0.125	0.461
206.1	25	32.5	7.5	0.149	0.018	0.125	0.292
211.9	25	25.0	0.0	0.066	0.013	0.125	0.204

The approximate drain efficiency can be calculated using the following equation [56]:

$$n_D = \frac{R_L}{R} - \frac{(2\pi A)^2}{12} - 0.01 \quad (3.26)$$

where, $A = \left(1 + \frac{0.82}{Q_L}\right) \left(\frac{t_f}{T}\right)$,

t_f = 100% to 0% fall time of the drain current at transistor turn-off,

T = time period of the operating frequency,

and the last term of the equation is an approximation of the resistive power losses in the dc-feed choke, L_d .

R_L and R for equation (3.26) can be estimated with the help of equations (3.20), (3.24) and (3.25).

The calculated efficiencies are presented in Tables 3.7 and 3.8, and the voltage gains for the inductive link are presented in Table 3.9.

3.5.4 Plots of Calculated Results

Plots of efficiencies and link gain against frequency of operation are provided in Figures 3.31 and 3.32.

Table 3.7 Calculations of Power Conversion and Link Efficiencies

Frequency of operation (kHz)	Primary to secondary power conversion efficiency (through Class-E converter and link), $\eta_{\text{conv}} = P_{\text{secondary}} / P_{\text{amp}}$	Estimated drain efficiency, η_{drain}	Estimated link efficiency, $\eta_{\text{link}} = \eta_{\text{conv}} / \eta_{\text{drain}}$
183.8	51.8%	79.0%	65.6%
195.0	61.5%	85.4%	72.0%
206.1	71.2%	92.8%	76.7%
211.9	75.6%	94.0%	80.4%

Table 3.8 Calculation of Overall Power Transfer or Load Efficiencies

Frequency of operation (kHz)	Load efficiency excluding regulator and gate drive losses, $\eta_{\text{load_net}} = P_{\text{load}} / P_{\text{amp}}$	Load efficiency excluding regulator, but including gate drive losses, $\eta_{\text{load_driver}} = P_{\text{load}} / P_{\text{driver}}$	Overall system efficiency for the given condition, $\eta_{\text{system}} = P_{\text{load}} / P_{\text{in}}$
183.8	10.9%	9.2%	3.6%
195.0	16.7%	13.2%	5.3%
206.1	30.5%	20.2%	8.9%
211.9	46.3%	26.0%	12.5%

Table 3.9 Calculation of Link Gain

Frequency of Operation (kHz)	Primary Coil Voltage, RMS (V)	Secondary Coil Voltage, RMS (V)	Link Gain (dB)
183.8	8.63	16.2	5.47
195.0	5.90	13.6	7.25
206.1	4.38	12.2	8.90
211.9	4.16	8.7	6.41

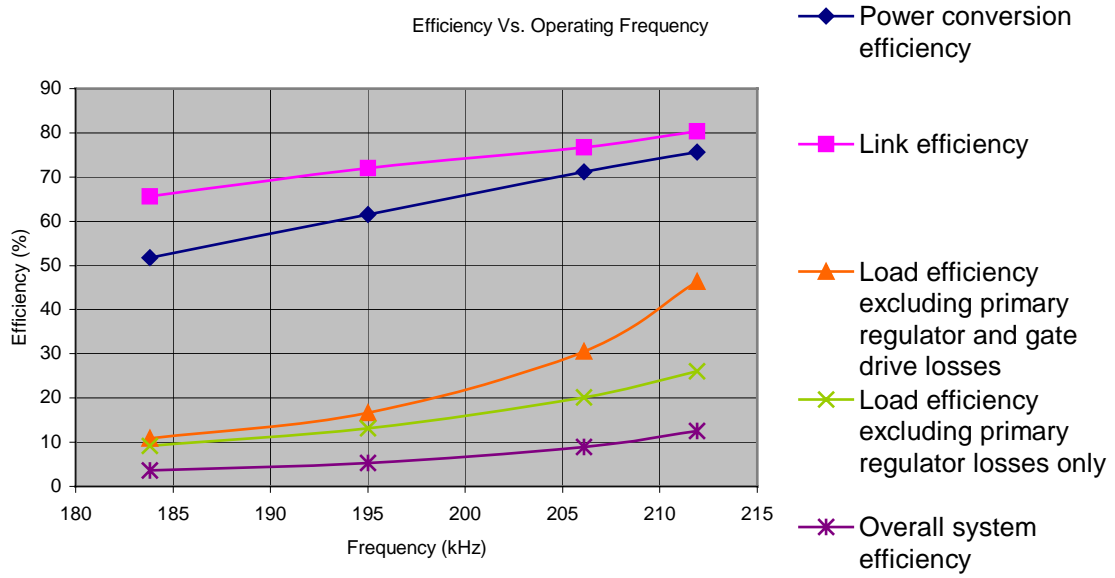


Figure 3.31 Efficiency vs operating frequency plots

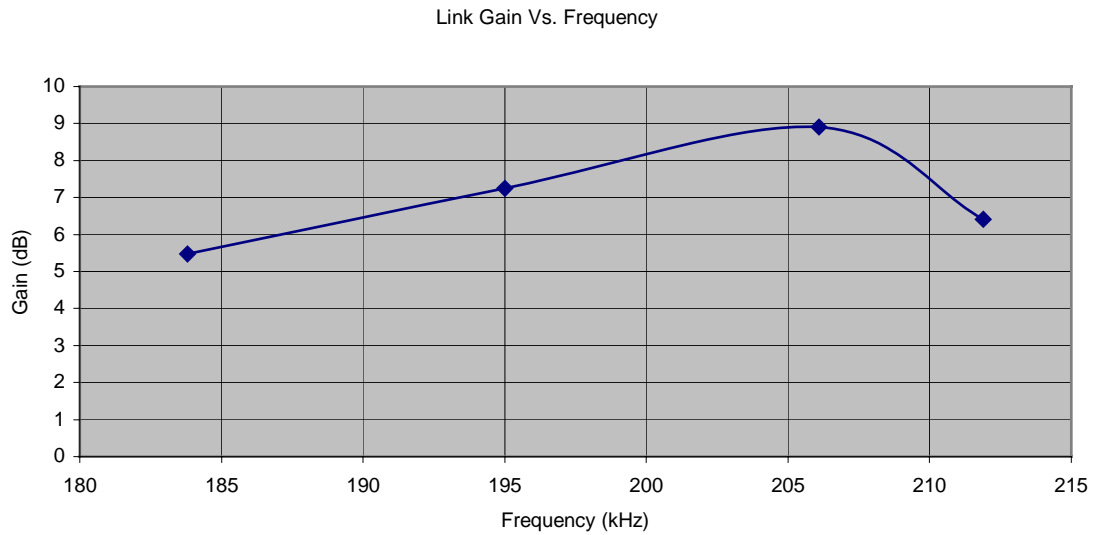


Figure 3.32 Link gain vs operating frequency plots

CHAPTER 4

Communication System Design

This chapter provides the details of the reverse communication scheme that has been designed and implemented over the same inductive link that was used for powering the implant electronics. It begins with determining the system requirements for backward communication and discussion about the selection of modulation scheme and key concepts. Then detailed schematic diagrams of different units of the communication system and design procedures are provided in an orderly fashion. Hand calculations and simulation results are included as necessary, and finally, test results regarding the data communication over the inductive link are presented.

4.1 Backward Data Communication

Implantable sensing and monitoring systems need a way of sending out the collected physiological data to outside world either in raw form or after proper processing of the analog electrical signals corresponding to biological variables. In many cases, the analog signals are converted to digital bit streams before transmitting transcutaneously. Sometimes encoding techniques are used for A/D conversion.

For the reasons mentioned in sections 1.2 and 1.3.1, inductive links have been evolved as the most popular and feasible solution for transdermal data communications to and from the implants. The backward telemetry, in particular, offers the attractive feature of real-time patient monitoring in clinical applications. If further processing and transmitting of the data is required, it can

be easily done externally, and thus without worrying about the power consumption at the implanted unit.

Several published work on data communication for implantable systems that utilized an inductive link are summarized in Table 2.2, which provides a first-hand idea of the different communication protocols used successfully, their performances, limitations and applications. In the following sections, the communication requirements will be determined for the intended application of this work. Then based on that and considerations of the available choices, a modulation scheme for the system will be selected.

4.1.1 System-Specific Requirements

The implantable perfusion sensor system described in section 1.1 is the first target application for the proposed inductive powering and data communication system. For standard operation, the perfusion sensor system digitizes raw sensor data from four analog signal channels. Each channel's signal is digitized at a rate of 150 samples per second using a 12-bit ADC.

Therefore, the required data rate = $4 \times (150 \times 12) = 7.2$ kbits/s [raw data only].

However, consideration of the packet overhead (i.e., start/stop bits for synchronization, time stamp, checksum etc.) yields the following figures –

For a maximum 100% overhead, required data rate = 14.4kbits/s

And For 50% packet overhead, required data rate = 10.8kbits/s

4.1.2 Choice for Modulation Scheme

From the summary of twelve publications presented in Table 2.2, it can be seen that the following modulation schemes were used for forward communication of digital data:

- FSK – Frequency Shift Keying
- OOK – On Off Keying
- ASK – Amplitude Shift Keying
- BPSK – Binary Phase Shift Keying
- PWM – Pulse Width Modulation
- Packet Detect

Among which the first three were the most popular.

On the other hand, for backward communication, the techniques used were:

- LSK – Load Shift Keying (also known as load modulation)
- ASK - Amplitude Shift Keying
- PWM – Pulse Width Modulation
- DBPSK – Differential Binary Phase Shift Keying
- Burst of RF energy,

where LSK was the most commonly used technique.

It is also noted that for backward telemetry, the reported maximum and minimum data rate-to-carrier frequency ratio were 0.08 and 0.0025, respectively; both of which were achieved using the LSK scheme. It is worth mentioning here that in relation to the target application and bandwidth requirement, the choice of frequency for transmitting the power signal (200kHz), and the measured self-resonant frequency of the coils (just above 1MHz for the

secondary coil), there is a certain practical limit in achievable data rate/carrier ratio.

In Table 4.1, some of the digital modulation schemes mostly used in inductive link-based communication are compared along with their advantage and disadvantage.

Based on the discussions presented in Table 4.1 and consideration of system specific requirements, FSK has been chosen as the modulation scheme for backward data communication from implantable sensor to the external unit. It was expected that with good power efficiency, decent error performance and bandwidth efficiency, FSK would be a good fit for this application. However, it is worth mentioning here that with simultaneous forward power signal and associated harmonic components of many times higher magnitude than the backward data, it becomes a challenge to properly couple, decouple and finally extract the data out from the primary coil. That is one reason why FSK has not ever been reported (in author's knowledge) as the modulation technique for reverse telemetry in implant systems.

4.1.3 FSK Terminologies

Some basic FSK concepts are discussed in this section based on [64].

Mark and Space: The two radio frequency FSK carriers corresponding to the binary logic level are called “Mark” and “Space”. For historic reasons, the higher frequency carrier is called Mark and the lower frequency is called Space.

Element Length: This term is used to define the minimum duration of a Mark or Space condition. Element lengths less than $1\mu\text{s}$ and greater than 1s have been successfully used.

Table 4.1 Comparison of Modulations Schemes*

ASK	OOK	LSK	FSK	BPSK/DBPSK
<ul style="list-style-type: none"> • Noncoherent • Simple • Inexpensive • Poor performance, as it is heavily affected by noise and interference • Low power efficiency • Should only be considered when the signal-to-noise ratio is very high 	<ul style="list-style-type: none"> • Non-coherent • Simple • A special form of ASK, where no line spectra are produced due to 100% modulation • Despite of reduced transmitter power than ASK, still inefficient in using power • Inferior error performance as ASK 	<ul style="list-style-type: none"> • Simple • Does not require a carrier • Utilizes the property of an inductive link that the load impedance seen by the secondary coil reflects back to the primary side and becomes a part of the primary coil's load • By modulating the load of the implanted circuit and detecting it by the voltage variations across the external coil, backward data transmission is achieved • The performance of this scheme highly depends on the coupling insensitivity of the link, and hence does not offer a robust communication choice 	<ul style="list-style-type: none"> • Can be noncoherent or coherent • Constant or nearly constant amplitude, and insensitive to amplitude variations • Better noise performance than amplitude modulation schemes • Moderate bandwidth efficiency • High power efficiency • Simple, low-cost implementation possible 	<ul style="list-style-type: none"> • BPSK is coherent, while DBPSK can be noncoherent as it compares the phase in one interval to the phase in the previous interval. • BPSK generally shows better error performance than ASK and FSK; but the error probabilities are double with DBPSK. • Bandwidth efficiency is similar to FSK. • Low power efficiency • Usually implementation is complex and more costly than other techniques

* Sources: [58], [59], [60], [61], [62], [63]

Keying Speed: The inverse of the element length in seconds is the keying speed. Its unit is baud. For many applications, such as the one in this work, the keying speed in baud is equivalent to the digital data rate in bits per second (bps).

Shift: It is the frequency difference between the Mark and Space frequencies. The nominal center frequency is halfway between the Mark and Space frequencies.

Occasionally, the frequency modulation term “deviation” is used, which is equal to the absolute value of the difference between the center frequency and the Mark or Space frequencies. In other words, $\text{Deviation} = (1/2) \times \text{Shift}$.

Coherent and Noncoherent Transmission: FSK signals can be transmitted coherently or noncoherently.

Coherent transmission means the phase of each Mark or Space signal has a fixed phase relationship with respect to a reference signal. This method is sometimes used, however, the condition that transitions from Mark to Space or vice versa must be phase-continuous requires that there be some specific relationship between the shift and keying speed. An FSK signal, which has a shift (in Hz) equal to an exact integer multiple ($n=1, 2, 3, \dots$ etc.) of the keying speed in bauds is called a synchronous FSK, and is the most common form of coherent FSK. Coherent FSK is capable of better error performance, but usually at the price of complexity and reduced design flexibility.

Noncoherent FSK signals do not have any special phase relationship between successive elements, and usually, the phase varies randomly. This type of FSK is simpler to generate and are most commonly used.

For the particular work presented in this thesis, a noncoherent transmission scheme has been chosen.

4.2 Modulation Unit

As discussed in section 2.5.1, the modulation unit consists of a VCO where the input to the VCO is the digital data from the implant electronics. As the VCO output frequency is ideally proportional to the magnitude of its signal input, it generates two different frequencies for the logic '0' and '1' levels, where the separation is separated by an amount depending on the VCO gain.

The CD4046B CMOS low-power PLL chip from Texas Instruments has been used as the FSK modulator for this work. This versatile IC consists of a linear VCO and two different phase comparators having a common signal-input amplifier and a common comparator input. Only the VCO unit of this chip has been used with proper timing resistors and capacitor to generate the FSK frequencies.

The block diagram of the generic 4046 PLL IC, provided by Motorola, Inc., is shown in Figure 4.1.

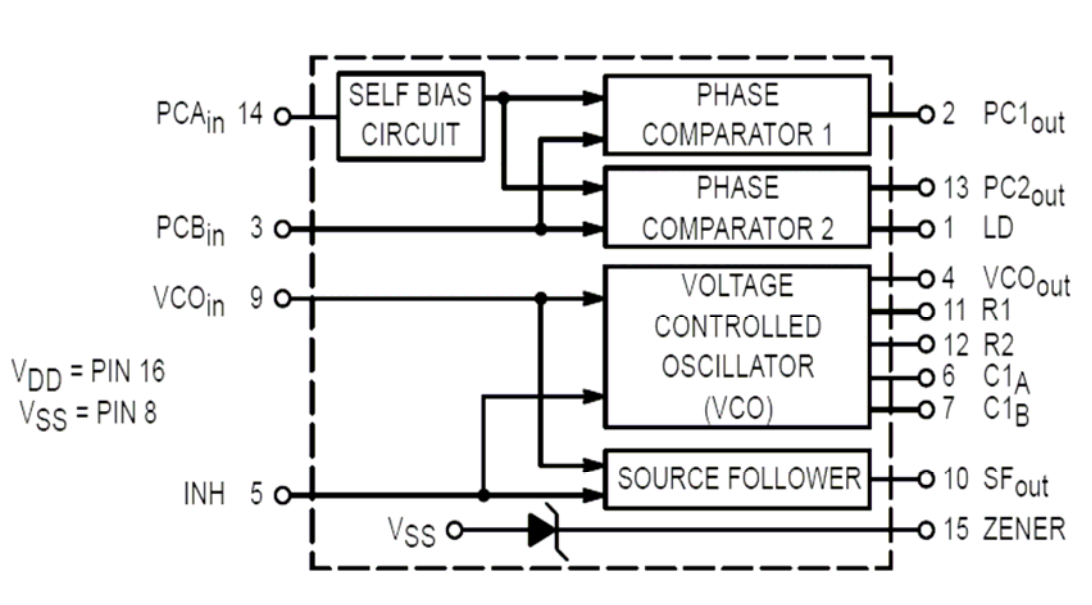


Figure 4.1 Block diagram of MC14046B (pin-to-pin equivalent for CD4046B)

The design equations to select the timing resistors R1, R2 and C1 (between pin 6 and 7) are given below:

$$f_{\min} = \frac{1}{R2(C1 + 32\text{pF})} \quad (4.1)$$

$$f_{\max} = \frac{1}{R1(C1 + 32\text{pF})} + f_{\min} \quad (4.2)$$

Where, f_{\min} and f_{\max} correspond to VCO inputs equal to VSS and VDD respectively, and

$$10\text{k}\Omega \leq R1 \leq 1\text{M}\Omega$$

$$10\text{k}\Omega \leq R2 \leq 1\text{M}\Omega$$

$$100\text{pF} \leq C1 \leq 0.01\mu\text{F}$$

The VCO gain can be estimated using the following equation:

$$K_{\text{VCO}} = \frac{2\pi \cdot \Delta f_{\text{VCO}}}{VDD - 2V} \quad (4.3)$$

Where, $\Delta f_{\text{VCO}} = f_{\max} - f_{\min}$.

It needs to be kept in mind that these equations are manufacturer provided approximate formula, and intended to be a design guide. Therefore, the equations are not very accurate; moreover, part-to-part VCO output frequency variation with identical passive components can be as large as $\pm 20\%$. So, potentiometers were used as the timing resistors for easy adjustment of the VCO frequencies. The value for C1 was chosen to be 820pF.

Selection of Mark and Space: The implementation of the FSK modulator was simple, however, the proper choice of the communication band was quite critical. As the power carrying frequency was chosen to be around 200kHz due to concerns about body exposure to electromagnetic radiation and tissue heating,

the initial approach was to select the two FSK frequencies between 200kHz and 400kHz, the fundamental and second harmonic of the power-carrying signal respectively. This is because Class-E amplifiers are usually reach in harmonics, as may be recalled from section 3.3.1 that the voltage and current waveforms at the coils are non-ideal sinusoids due to finite loaded Q of the link. While the loaded Q should be less than 5 in order to have a sufficient pass-band for data communication.

Unfortunately, due to low Q of the link, the power signal seemed to have very dominant 2nd, 3rd, 5th harmonics, and considerably large 4th, 7th and 9th harmonics in comparison to the induced data signal amplitude at the primary coil. On top of that the mixing among the Mark, Space and all these harmonic components in various combinations greatly corrupt the frequency spectrum over the link and makes the job of decoupling and filtering the data from the primary coil very difficult. Sometimes this meant a very complex filter configuration with unrealistic component demands. These effects were justified by simulations and experienced in practice.

Seemingly there were two ways to solve this problem: to set the communication band either well above the power carrying frequency or below the power carrying frequency, so that the fundamental and harmonics of the power signal interfere less with the communication signals. A few different frequency bands were tried. Based on these studies and experiments, and consideration of the self-resonant frequencies of the coils (which is just over 1MHz for the secondary coil), a feasible solution seemed to be placing the communication band near 100kHz. Fortunately, the filtering of data from power signal turned out to be easier and practicable in this range, which will be described more in the Data Decoupling and Filtration section.

Therefore, the center frequency for FSK modulation has been finally selected to be around 120kHz, and a frequency shift of 20kHz has been chosen as a starting point.

4.3 Data Coupling and Decoupling

4.3.1 Coupling with the secondary coil

The 4046 PLL chip is not capable of driving a low-impedance reactive load, also the data signal should not interfere with the secondary power management blocks. For these two considerations, a gain stage and suitable trapping networks were used in the implantable unit to facilitate data coupling with the secondary coil (see Figure 4.2).

Gain Stage: By recalling that a resonant tank circuit behaves as an inductor below the frequency of resonance and as a capacitor above the frequency of resonance, it has been found that the inductive reactance of the parallel secondary tank is less than 500Ω at the FSK center frequency. Therefore, a simple common-source gain stage has been added at the output of the modulator (VCO). The gain setting resistor was chosen to be $1k\Omega$, so that the current to the amplifier does not exceed 5mA with a 5V internal supply. An n-channel vertical MOSFET (ZVNO120A) has been used as the active device.

Traps: The output of the common-source amplifier has been connected to the secondary coil through a series resonant network, known as a series trap, so that it offers a low-impedance path for the FSK signals at their center frequency.

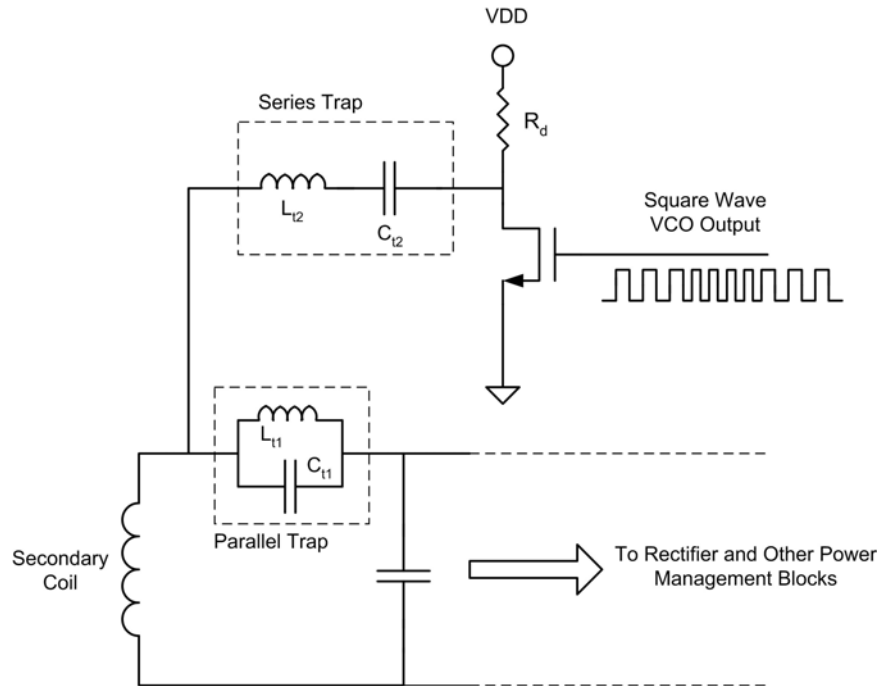


Figure 4.2 Gain stage and the trap networks

On the other hand, a parallel trap comprising of L_{t1} and C_{t1} has been used between the secondary coil and the parallel resonating capacitor by breaking the loop. This trap isolates the data signal from the rest of the power recovery circuitry by providing high impedance at the Mark and Space frequencies, and thus keeps the efficacy of the power recovery unit virtually unaffected. These techniques have been successfully used in RF broadcasting applications, and are proved effective in this project as well.

The proper choice of component values is important for correct operation of this scheme. The basic idea is the inductance and capacitance values for the traps should be selected such that the equivalent impedance of the parallel tank combination of the secondary coil remains nearly same, and thus the system provides very similar response to the power signal as the one without the traps. Of course, the transient response of the voltage at the primary coil will be

changed as it is modulated by data. Hand calculations, simulations and practical experiments – all were performed for deciding on the component values.

4.3.2 Decoupling from Primary Coil and Filtration

A similar trapping strategy has been utilized in the primary unit in order for preventing the FSK carriers to intervene in the Class-E driver operation. The primary coil voltage is then passed through two stages of passive and active filtering to extract the desired data carriers out of all other unwanted frequencies. The filtered FSK modulated signal is then fed into the demodulator input.

Passive Bandpass Filter: A fourth-order Butterworth bandpass filter has been used as the first filtering stage. Since higher-order filter design is a tedious task, and sometimes does not provide the optimum result, a filter design software (Filter Solutions 11.0.3 from Nuhertz Technologies, LLC) was used to do this job. The specifications provided to the software were:

Center frequency: 120kHz

Pass-band width : 23kHz

Stop-band zero : 218kHz

A zero at the power transfer frequency has been added to further improve its suppression. This is important because the magnitude of the power signal at the primary coil can easily be a few hundred times greater than that of the FSK carriers induced at the primary coil.

Filter Solutions generated the transfer function, frequency response, time response, input-output impedance plots, and even a possible circuit arrangement that approximates the ideal filter. The frequency response was verified by SPICE simulations and are both included in the Simulation Results section. The circuit

configuration with finite inductor Q s generated by the software is shown in Figure 4.3.

However, slightly different component values were used based on the existing inventory and requirements. The actual component values used in the PCB version of the prototype are shown in Figure 4.4.

Active Bandpass Filter with Gain: The induced FSK data signal at the primary coil is small, in the order of a few hundred millivolts, and it can be reduced due to coupling variations. Furthermore, as the signal passes through the passive filter network, it suffers from some attenuation, which is expected due to finite quality factors of the passive components, especially the inductors. Therefore, a gain stage is necessary to provide sufficiently large FSK signal that can be detected by the demodulator. Therefore, another stage of active bandpass filtering with voltage gain has been used. A single-opamp Sallen-Key filter has been designed and utilized for this purpose.

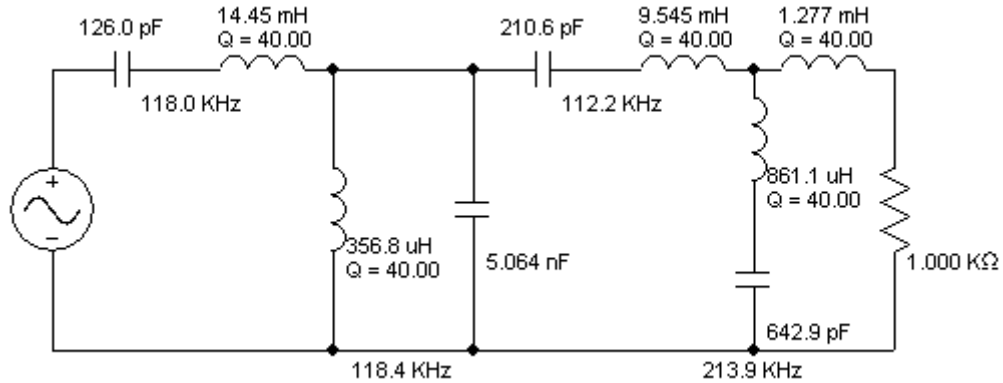


Figure 4.3 Schematic entry of the 4th order passive bandpass Butterworth filter

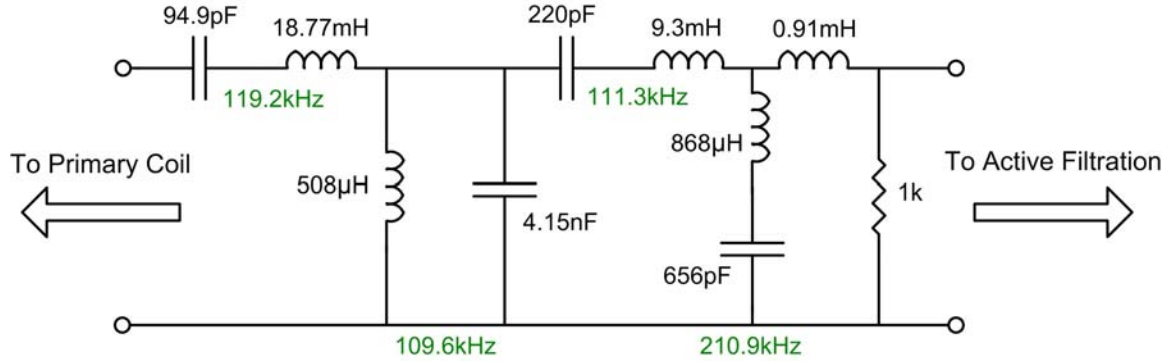


Figure 4.4 Component values actually used in the passive bandpass filter

The circuit arrangement for the single-stage Sallen-Key bandpass filter is shown in Figure 4.5. The OP27 low-noise precision opamp has been used as the active device in the implementation of the prototype. This is a dual-supply opamp, however, a single-supply device with similar characteristics can easily be substitute it.

The schematic shown in Figure 4.5 is a special case of Sallen-Key filter where all the resistors and capacitors have the same value, except for the two gain-setting resistors. This simplifies the design and implementation of the circuit. Following design equations [65] can be used to hand-calculate the resistances and capacitances:

$$\text{Center frequency, } f_c = \frac{\sqrt{2}}{2\pi RC} \quad (4.4)$$

$$\text{Non-inverting gain, } K = 1 + \frac{R_B}{R_A} \quad (4.5)$$

$$\text{Overall gain (at center frequency)} = \frac{K}{4 - K} \quad (4.6)$$

$$\text{Quality factor of the filter} = \frac{\sqrt{2}}{4 - K} \quad (4.7)$$

$$\text{Bandwidth} = \frac{f_c}{Q} \quad (4.8)$$

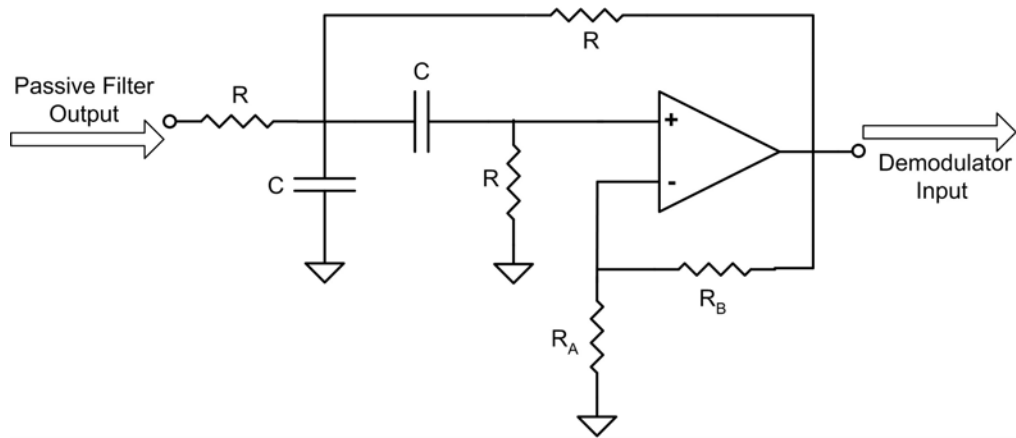


Figure 4.5 Schematic diagram of the Sallen-Key bandpass filter

The component values were first estimated using the above equations, then verified by simulations, and finally chosen through experiments. The components used in the final PCB version are:

- $R = 10\text{k}\Omega$, $C = 184\text{pF}$
- $R_A = 1\text{k}\Omega$, R_B : $100\text{k}\Omega$ potentiometer for manually adjusting the gain

4.4 Demodulation

The CD4046B PLL chip has been used to implement the FSK demodulator. The demodulator design involves the proper choice of timing resistors-capacitors and the loop-filter elements.

As can be seen from the schematic diagram of the demodulator as illustrated in Figure 4.6, the filtered FSK signal is ac-coupled to the signal input of the phase comparator. The VCO frequencies are set same as the ones of the modulator. VCO output is connected to the phase comparator. Between the output of the phase comparator (PC) and the VCO input, a passive R-C low-pass filter is used to reject the ripple at the PC output. The loop filter can be designed using equation (4.3) and (4.9)-4(11), as provided in the 4046 datasheet:

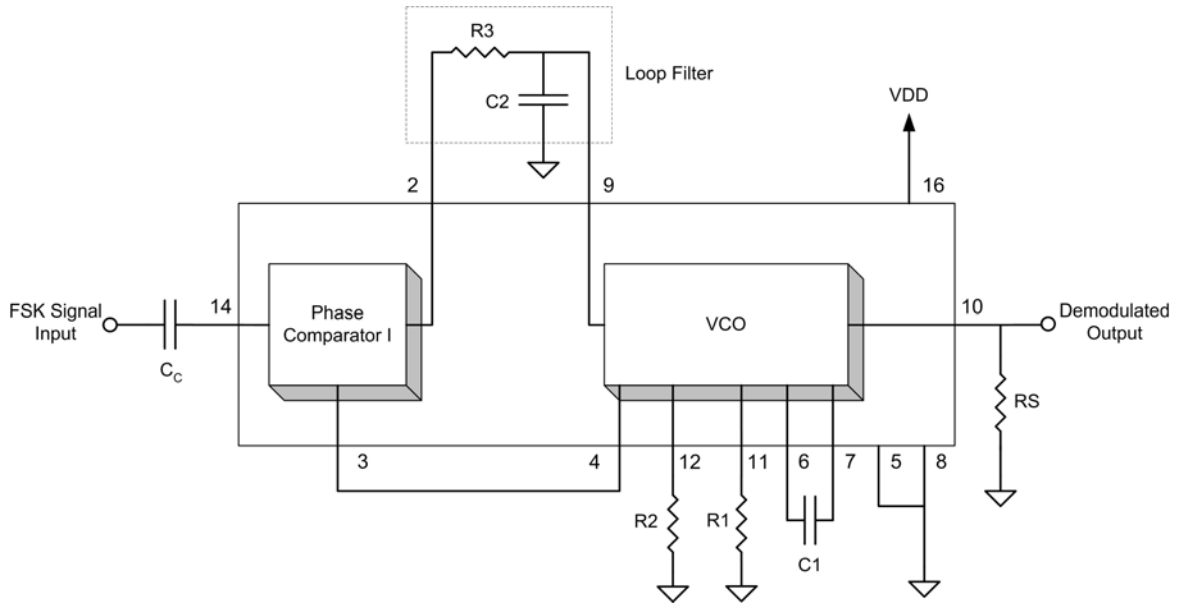


Figure 4.6 Schematic diagram of the demodulator

$$2f_c \approx \frac{1}{\pi} \sqrt{\frac{2\pi f_L}{R_3 C_2}} \quad (4.9)$$

where, $2f_c$ = capture frequency range

$2f_L$ = lock frequency range.

$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_3 C_2}}, \quad (4.10)$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}} \quad (4.11)$$

where,

the gain constant of the phase comparator, $K_\phi = \frac{VDD}{\pi}$ for Phase

Comparator 1,

N = total division ratio in feedback loop (1 in this case)

Loop damping factor, $\zeta = 0.7$ to 1.0 for a typical design

ω_n = natural frequency of oscillation.

Finally, the demodulated output (i.e., the VCO input) is obtained from the source-follower output so that the loop-filter is not loaded. A load resistor (R_S) of $10k\Omega$ or more needs to be connected from this node to ground.

Design of the Demodulator:

The design of the loop-filter and the choice for VCO gain are critical for the proper operation of the demodulator (i.e., PLL). Before presenting the design methodology for the loop filter, some fundamental concepts related to a phase-locked loop are briefly discussed here.

The block diagram of a simple feedback system is shown in Figure 4.7.

In this figure, $\theta_i(s)$ = phase input

$\theta_e(s)$ = phase error

$\theta_o(s)$ = output phase

$G(s)$ = product of the individual feed forward transfer functions

$H(s)$ = product of the individual feedback transfer functions

The following relationships can be easily obtained [67]:

$$\theta_e(s) = \frac{1}{1 + G(s)H(s)} \cdot \theta_i(s), \text{ and} \tag{4.12}$$

$$\theta_o(s) = \frac{G(s)}{1 + G(s)H(s)} \cdot \theta_i(s) . \tag{4.13}$$

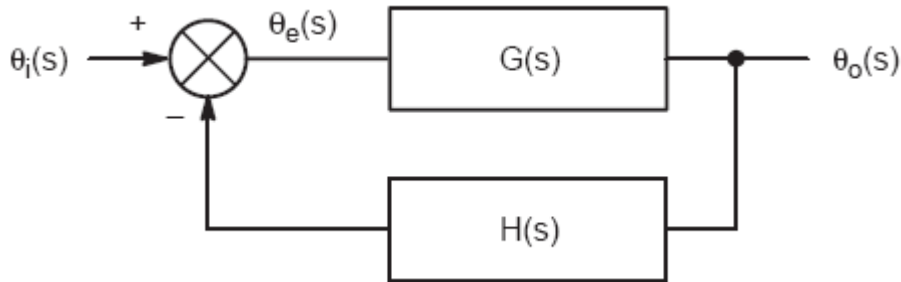


Figure 4.7 Feedback system [66]

These parameters of the feedback system relate to the PLL functions as shown in Figure 4.8.

The phase detector, filter and VCO/VCM (VCM – Voltage-Controlled Multivibrator) are the elements of the feed forward path, while the feedback path contains the programmable counter or divider. Removal of the counter results in a unity gain in the feedback path (i.e., $N = 1$), which means output frequency is then equal to the input frequency.

The expression $G(s)H(s)$ is called the *Loop Transfer Function* (LTF) and the following equation is termed the *Characteristic Equation* (CE) of the loop:

$$1 + G(s)H(s) = 0 \quad (4.14)$$

The roots of the CE are the closed loop poles of the overall transfer function.

Feedback loops of various types and orders can be constructed, where:

- The *type* of a system refers to the number of poles of the LTF located at origin, and
- The *order* of a system refers to the highest degree of CE.

As an example,

$$\text{the LTF} = G(s)H(s) = \frac{10}{s(s+5)},$$

$$\text{and corresponding CE: } s^2 + 5s + 10 = 0$$

refers to a Type 1 second order system.

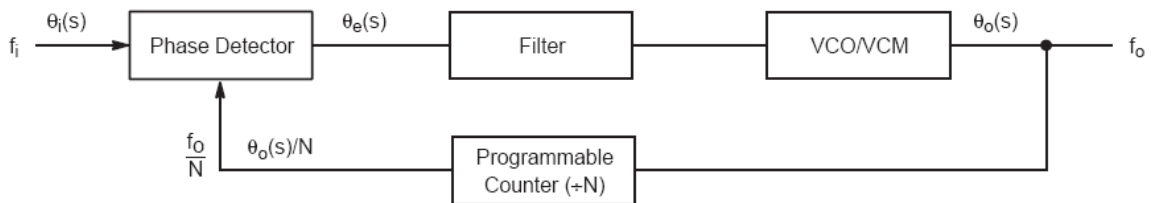


Figure 4.8 Block diagram of a phase-locked loop [66]

The steady-state evaluation of phase errors for different types of systems can be performed with the use of Final Value Theorem, and the results thus obtained for three major types of systems are shown in Table 4.2.

A zero phase error indicates phase coherence between the two input signals at the phase detector, while a constant phase error implies a phase differential between the input signals. The magnitude of the phase error is proportional to the loop gain and the magnitude of the input step function. A continually increasing phase error signifies a variable phase with respect to time. This is an unlocked condition for the PLL.

Since non-coherent FSK for data communication is used, it is needed for the PLL/demodulator to track the FSK frequencies (i.e., step velocity); however, a zero phase error is not required. Therefore, a constant phase difference, and hence a Type 1 system is sufficient for this purpose, which also simplifies the loop-filter design. A typical design procedure particular to the demodulator in discussion is presented here.

Let, some of the known conditions are –

VCO output frequencies: 115kHz and 125kHz

Frequency step, $\Delta f_{VCO} = 10\text{kHz}$

Dividing ratio, $N = 1$

Table 4.2 Steady-State Phase Errors for Various System Types [66]

	Type 1	Type 2	Type 3
Step Position	Zero	Zero	Zero
Step Velocity	Constant	Zero	Zero
Step Acceleration	Continually Increasing	Constant	Zero

Applying equations (4.3) yields,

$$K_{VCO} = 20.94 \times 10^3 \text{ rad/s/V.} \quad [\text{for } VDD = 5V]$$

In frequency domain,

$$K_{VCO}(s) = \frac{20.94 \times 10^3}{s}.$$

And,
$$K_{\phi}(s) = \frac{VDD}{\pi} = 1.59$$

For the loop-filter shown in Figure 4.6,

$$K_f(s) = \frac{1}{1 + sR_3C_2}$$

Therefore, by definition,

$$\begin{aligned} G(s)H(s) &= K_{\phi}(s) \cdot K_f(s) \cdot K_{VCO}(s) \cdot N \\ &= \frac{33.3 \times 10^3}{s(1 + sR_3C_2)}, \end{aligned}$$

which is the LTF of a Type 1 second order system.

Now, a rule of thumb for choosing the loop-filter's component values is to set the filter's time constant equal to or greater than 5 times the FSK carrier period. Thus, an effective ripple rejection from the phase comparator's output and an acceptable noise margin for the demodulator output can be achieved. Therefore, the time constant is set to be,

$$R_3C_2 = \frac{5}{120 \times 10^3} = 41.67 \mu\text{s}.$$

Choosing $C_2 = 670\text{pF}$ yields $R_3 = 62.2\text{k}\Omega$.

The natural frequency of oscillation and the damping ratio can be found from equations (4.10) and (4.11) respectively:

$$\omega_n = 28.27\text{krad/s}$$

$$\zeta = 0.424.$$

By the use of the Type 1 second order step response curves shown in [66], it can be estimated that the transient response settles down within 20% of the final

value for $\omega_n t \geq 4.5$. Therefore, the lock-up time or settling time can be approximated by,

$$t = \frac{4.5}{\omega_n} = 159.2 \mu\text{s}.$$

Certainly, this settling time is quite high compared to the fastest data rate of 10kbps, and this has been reflected in the experimental waveforms of the demodulator. However, through the analysis of the expressions for ω_n and ζ given by (4.10) and (4.11), it is observed that with the given configuration, the demodulator's transient response may not be significantly improved unless the PLL's bandwidth is decreased.

4.5 Simulation Results

Simulations were mainly performed for the passive and active filter stages. For other blocks of the communication system, simulations were not carried out due to unavailability of appropriate models. Rather they were directly built on the lab proto-board, tested, and hand calculations were done as necessary. The simulation results obtained using Filter Solutions and SPICE are included in this section (Figures 9 through 14). As will be observed, the SPICE simulation results for the 4th order Butterworth passive bandpass filter are very similar to the ones obtained using Filter Solutions, although different component values were used. For the simulation of active Sallen-Key bandpass filter in SPICE, the component values provided in section 4.3.2 and 3.22k Ω for R_B and the OP-27G opamp macromodel from Texas Instruments have been used.

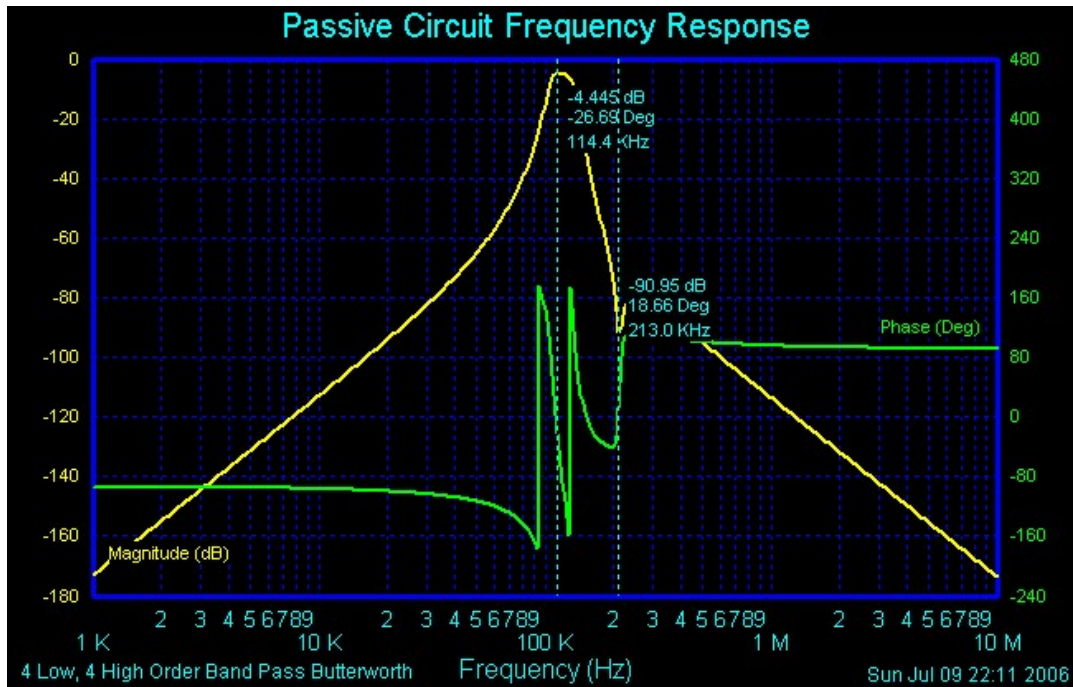


Figure 4.9 Frequency response of the 4th order passive bandpass Butterworth filter with center frequency=120kHz (circuit provided in Figure 4.3)

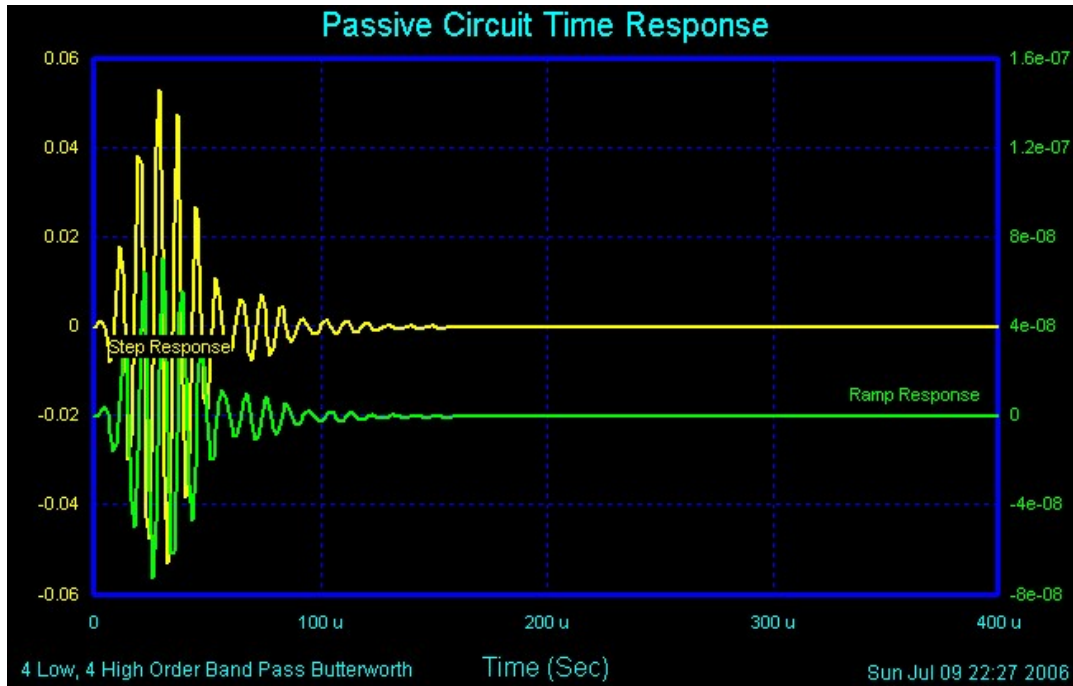


Figure 4.10 Time-domain response (for step and ramp functions) of the 4th order Butterworth filter shown in Figure 4.3

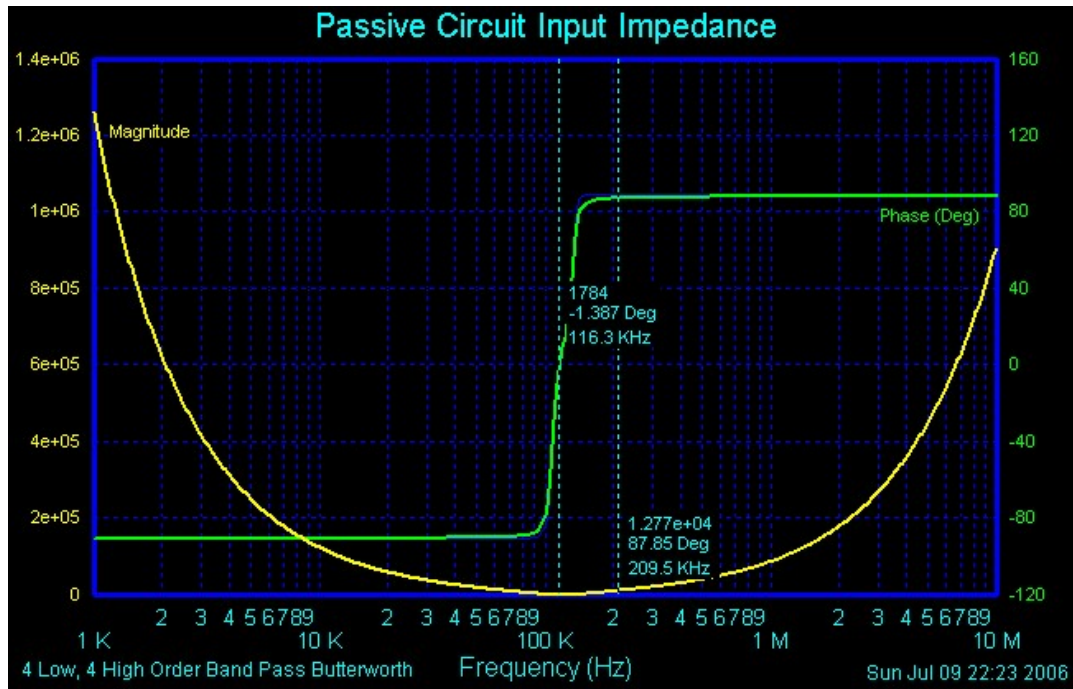


Figure 4.11 Input impedance characteristics of the filter shown in Figure 4.3

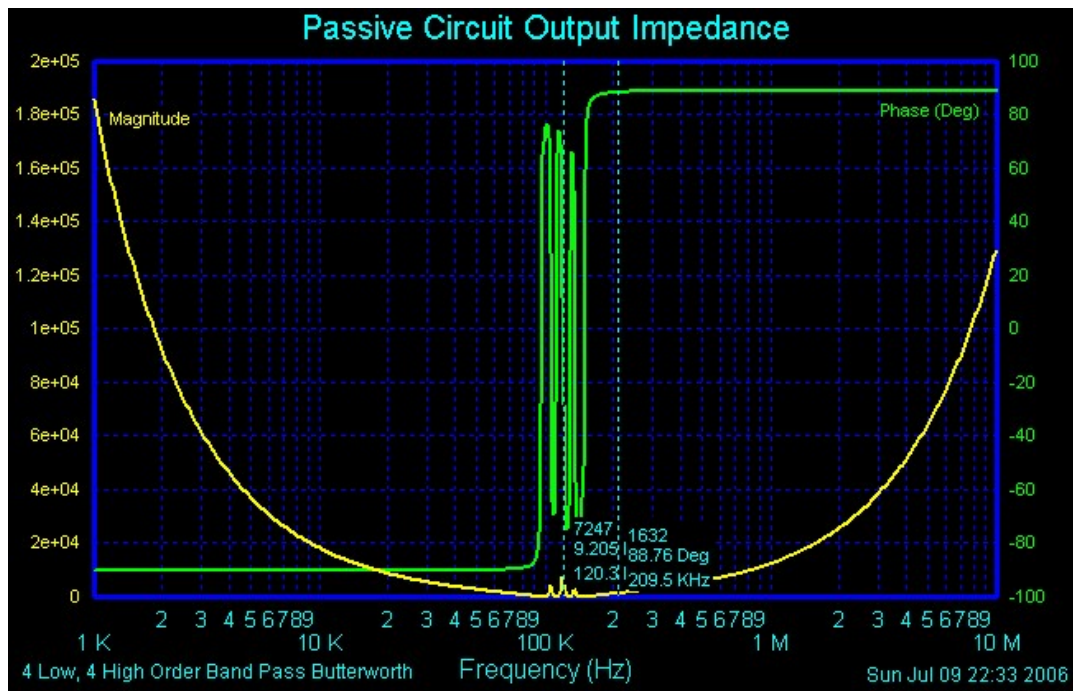


Figure 4.12 Output impedance characteristics of the filter shown in Figure 4.3

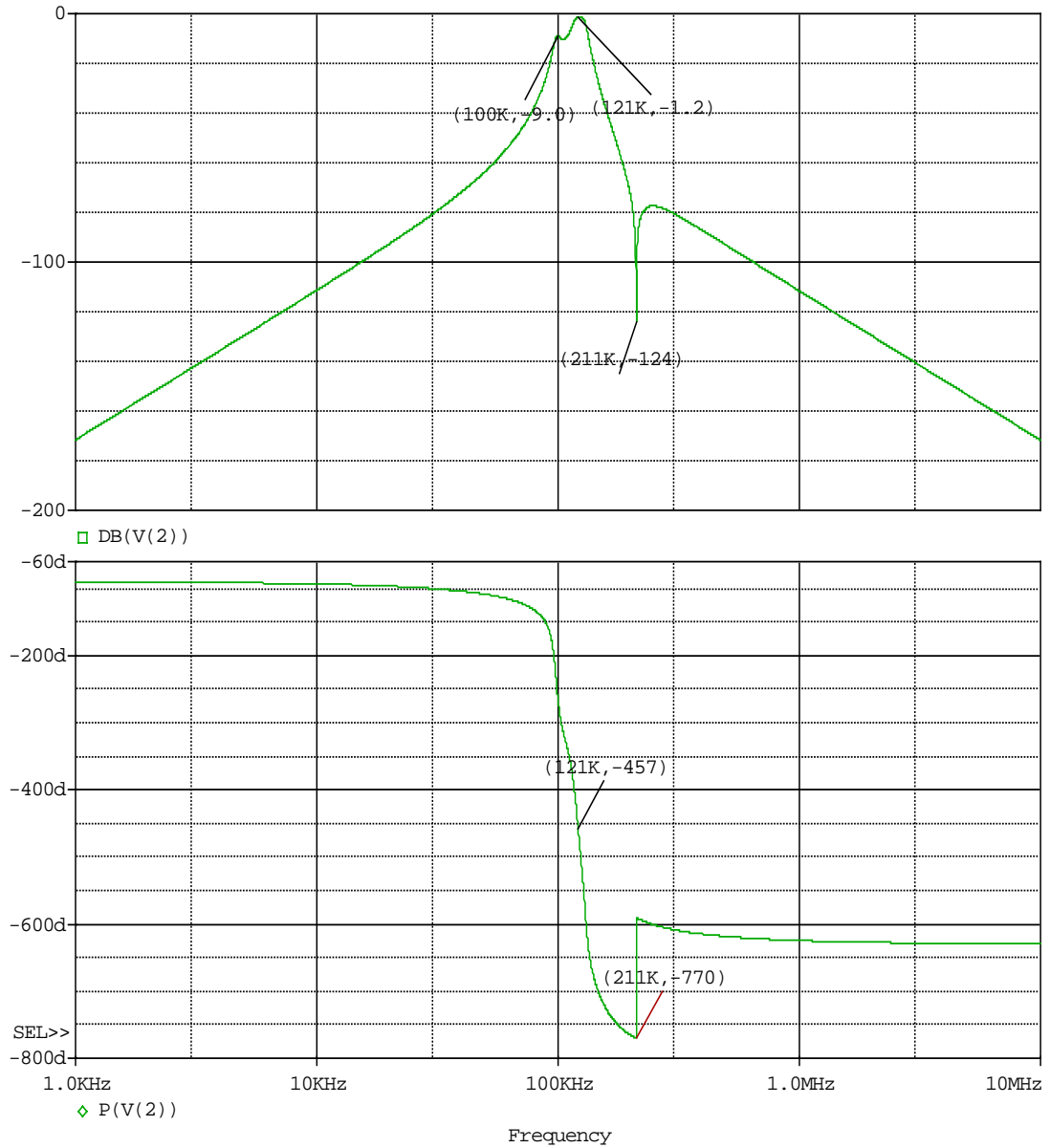


Figure 4.13 SPICE simulation of the frequency response for the 4th order passive bandpass filter (as shown in Figure 4.4): the top trace is the magnitude response and the bottom trace is the phase response

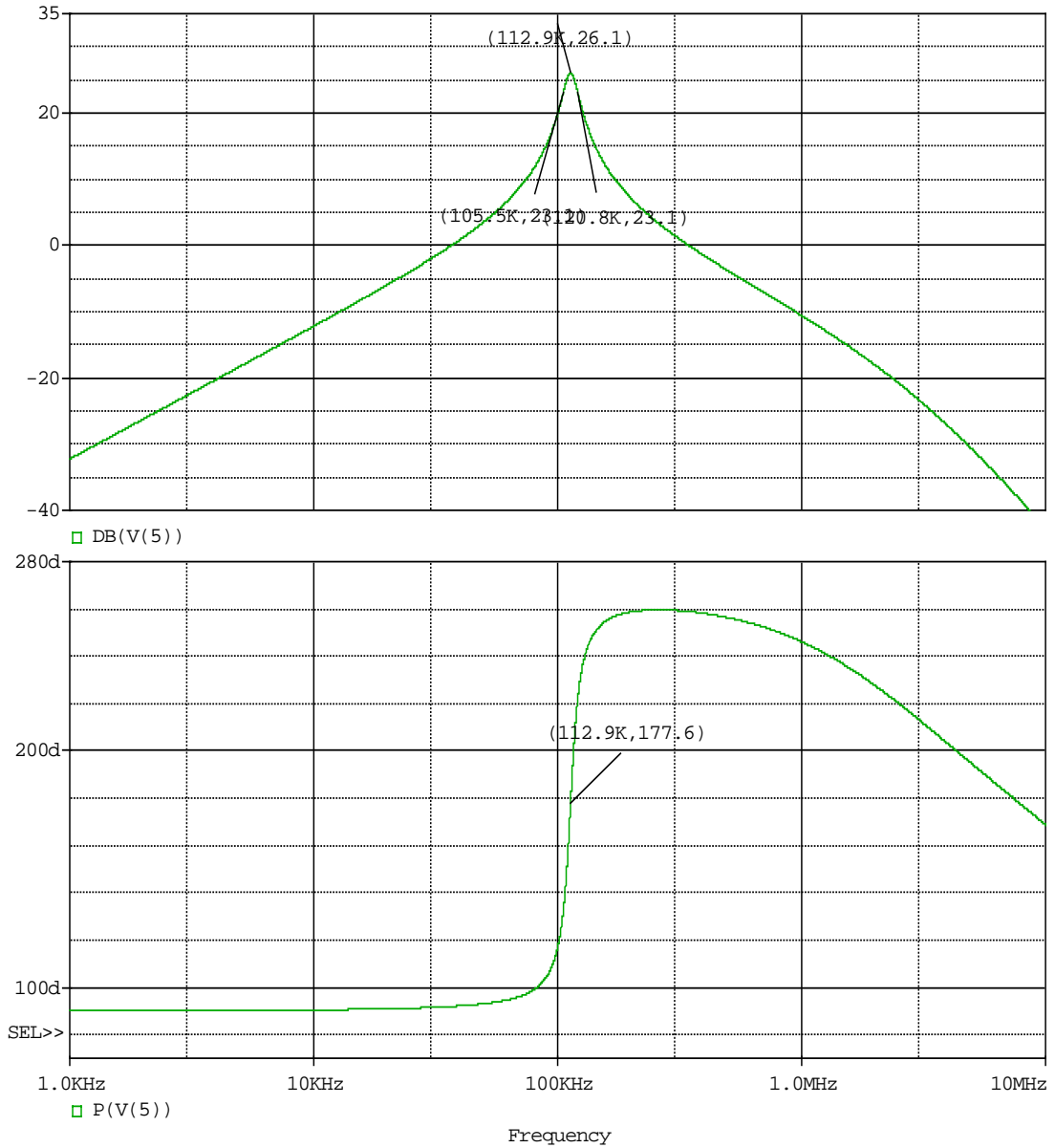


Figure 4.14 SPICE simulation of the frequency response for the active single-stage Sallen-Key bandpass filter (as shown in Figure 4.5): the top trace is the magnitude response and the bottom trace is the phase response

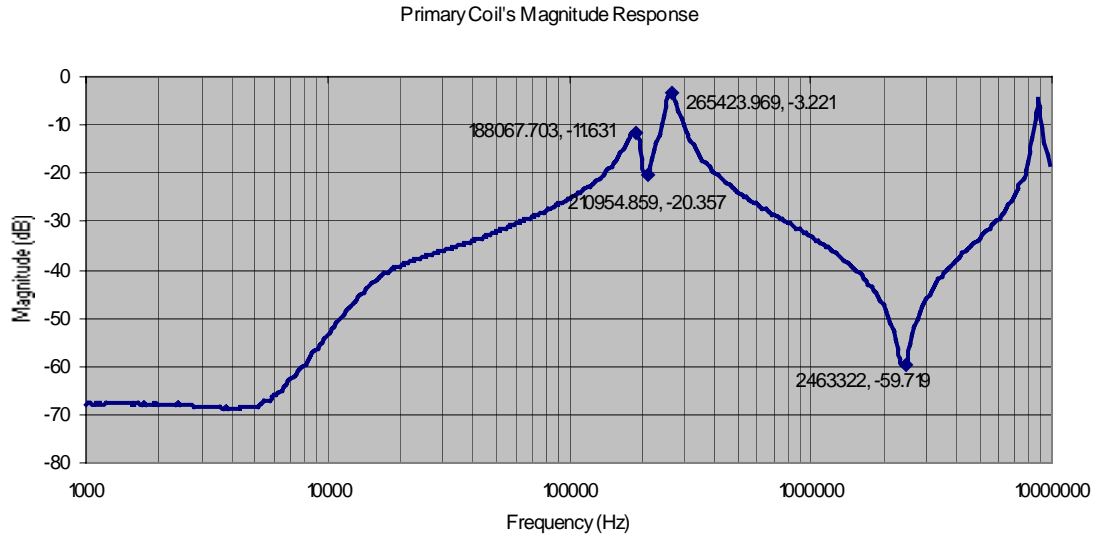
4.6 Test Results

4.6.1 Frequency Response Curves

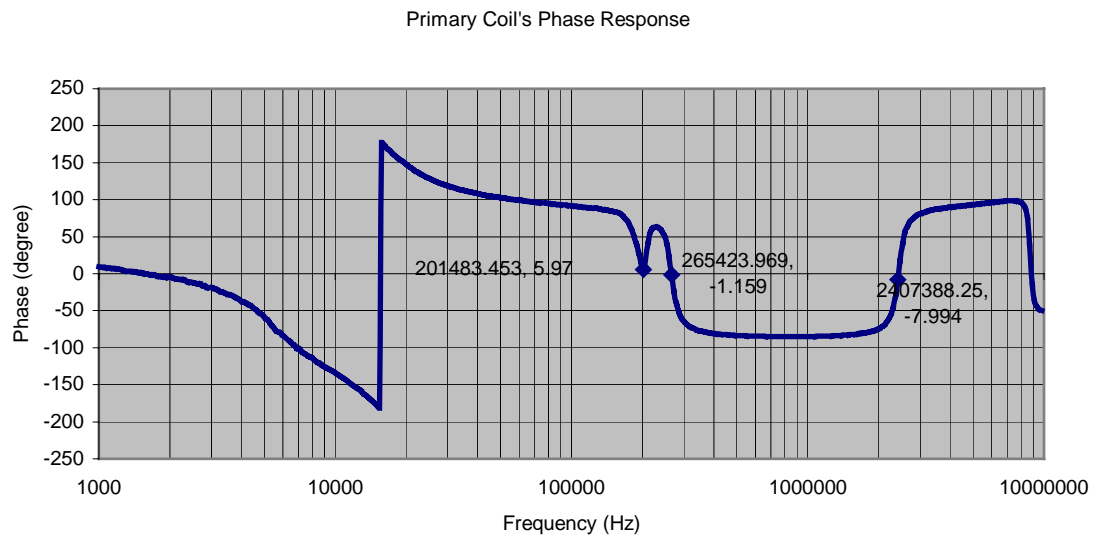
As was done earlier for the primary and secondary coils and other blocks of the powering system, several frequency domain analyses were performed after combining the communication modules with the powering units. The data have been transferred from the network analyzer to the PC through GPIB port and the use of a LabVIEW program, and then imported to Excel to generate nicer plots. The resulting Bode plots are shown in Figures 4.15 through 4.19. The primary and secondary coils' responses have been measured once again to see if there are any effects of the series and parallel traps and the filters, which were connected at different nodes of the inductive powering system. As will be seen shortly, the coil responses remain virtually the same, and that is what expected. The other frequency response curves presented in this section are the passive and active bandpass filters' individual responses, and their combined response when they are connected back to back. In order to obtain the active filter's response, the opamp (OP-27) was powered up, while for the passive filter, no supply was required, and the network analyzer's source was used as the input signal for both the cases.

4.6.2 Time-Domain Waveforms of the Communication System

Oscilloscope waveforms are provided in this section (Figures 4.20 through 4.38) to show the FSK modulation of baseband data, passive and active filtering with amplification of the FSK-modulated signal in the receiver or external side, and finally demodulation of the data. The digital data has been modeled by a square wave signal of 5V (p-p) with 2.5V offset, where 5V represents a logic '1' and 0V represents a logic '0'. The data rate (in bits/s) is equivalent to twice the frequency

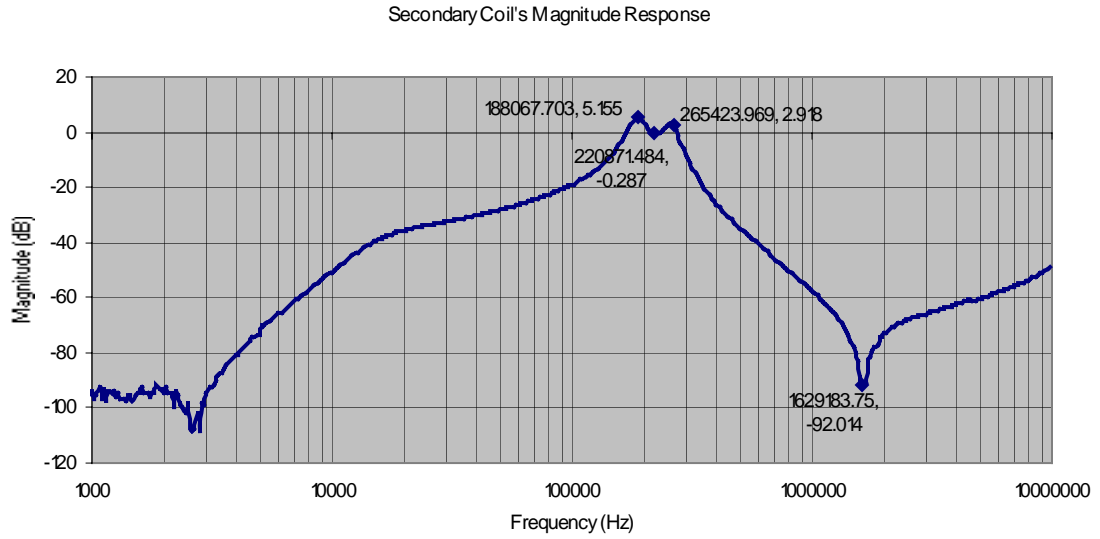


(a)



(b)

Figure 4.15 Bode plots for the primary coil with the communication system incorporated



(a)

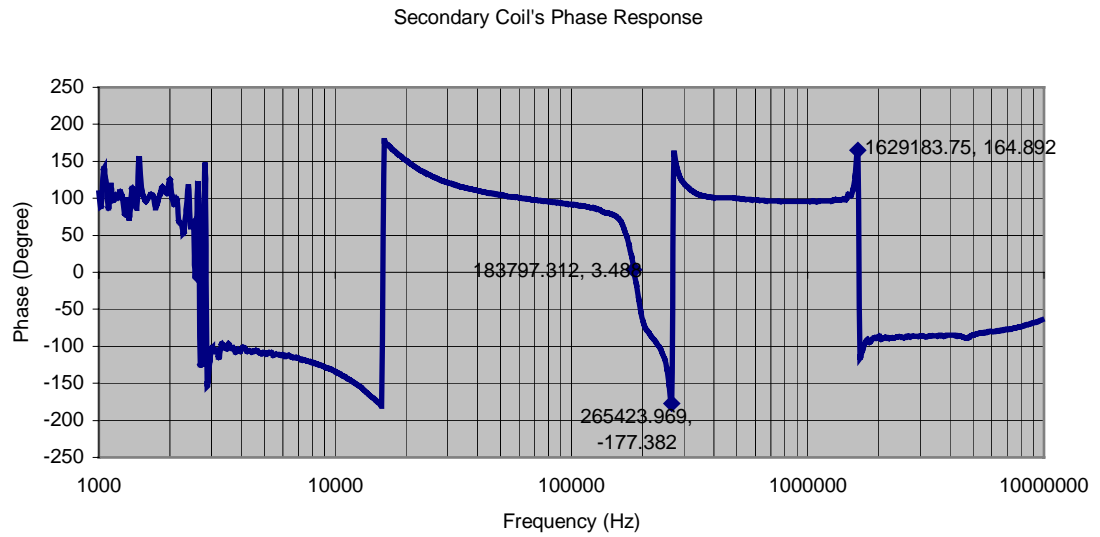
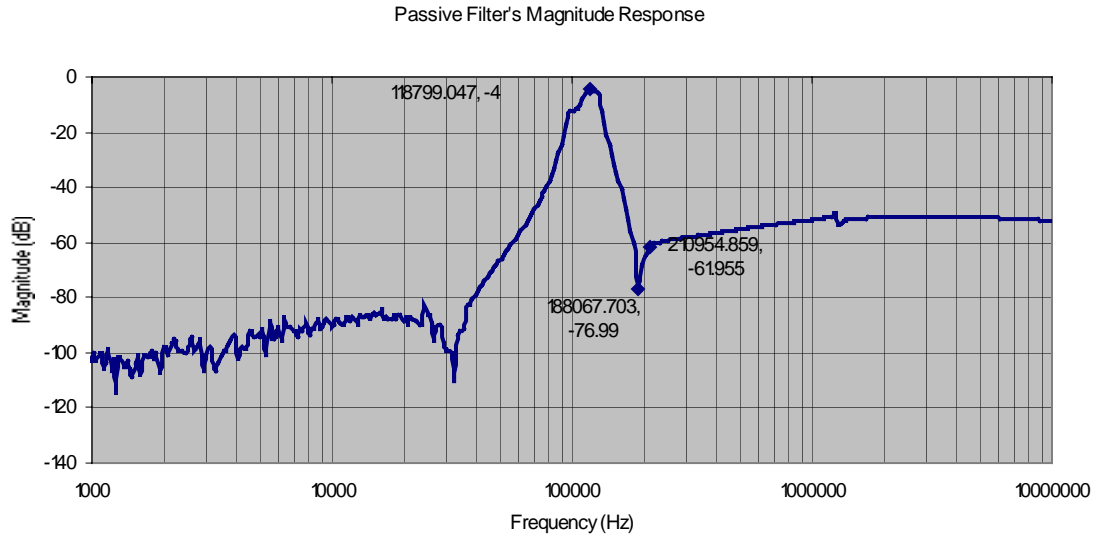
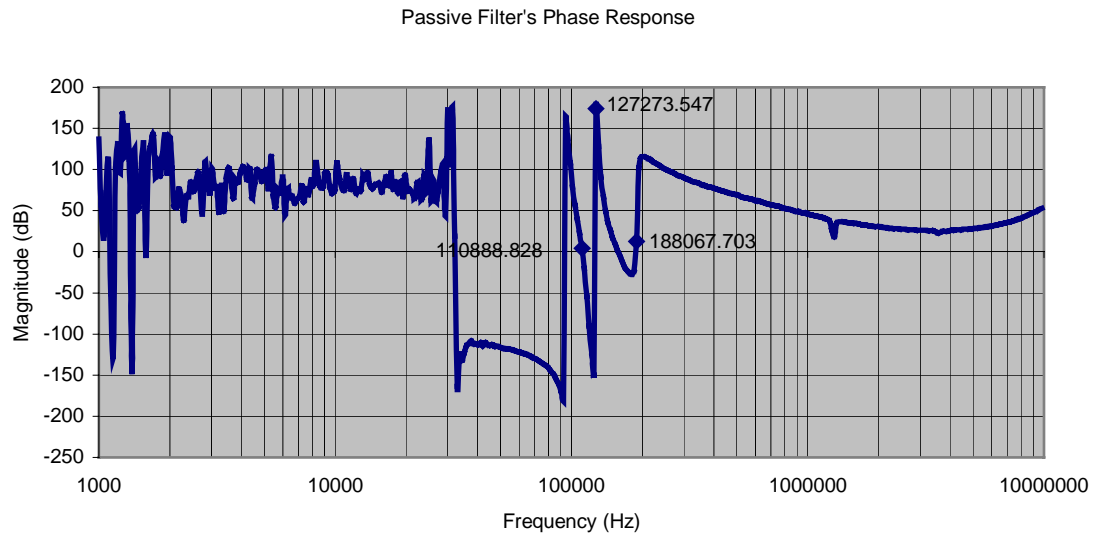


Figure 4.16 Bode plots for the secondary coil with the communication system incorporated

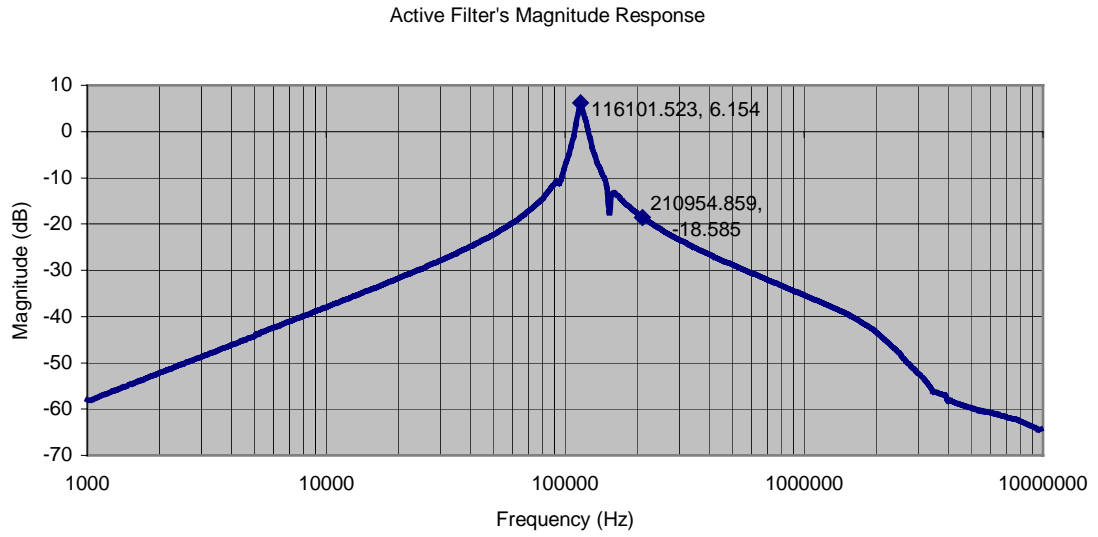


(a)

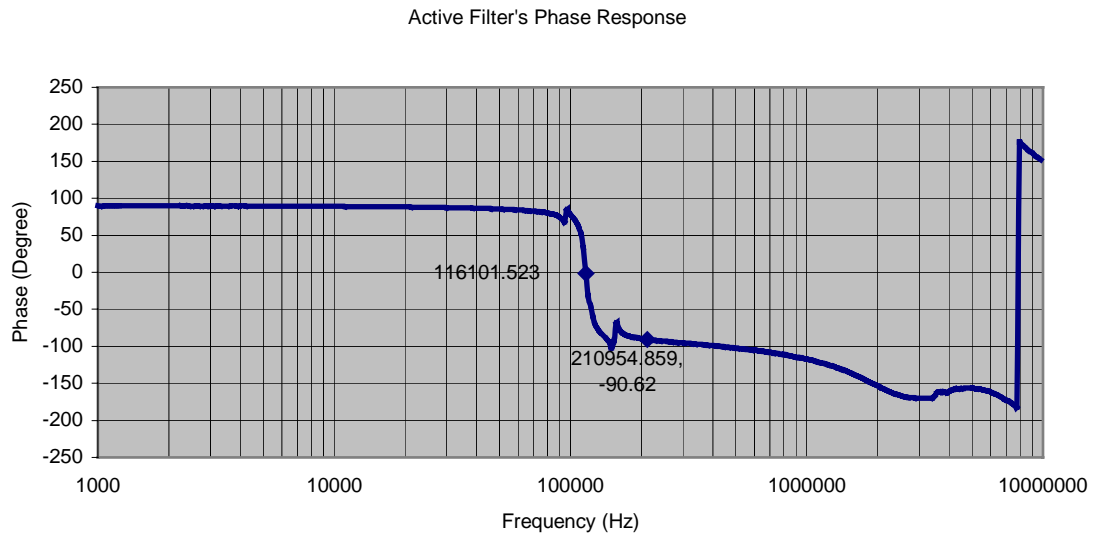


(b)

Figure 4.17 Bode plots for the 4th order Butterworth passive bandpass filter



(a)



(b)

Figure 4.18 Bode plots for the active Sallen-Key bandpass filter

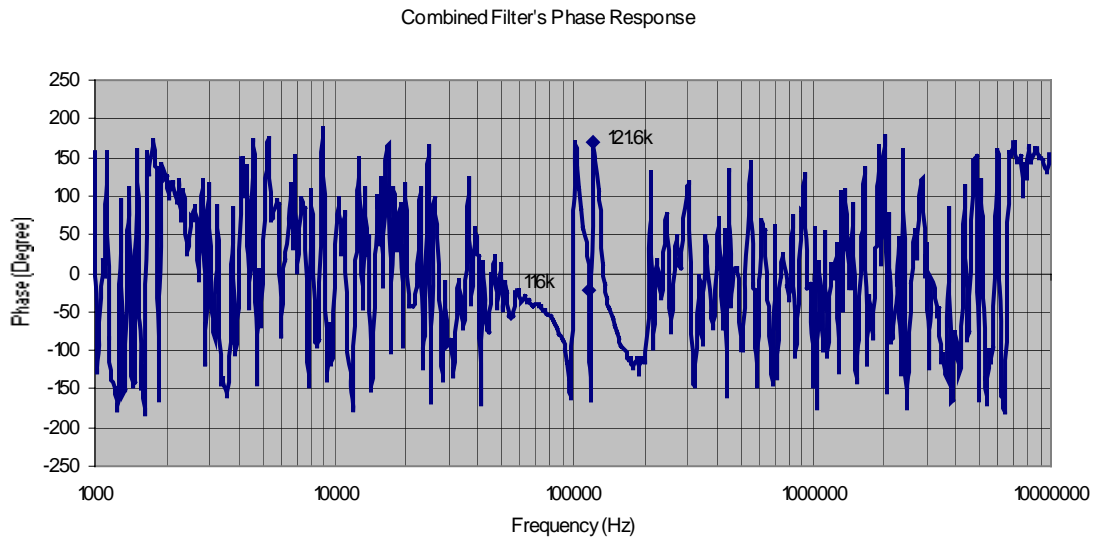
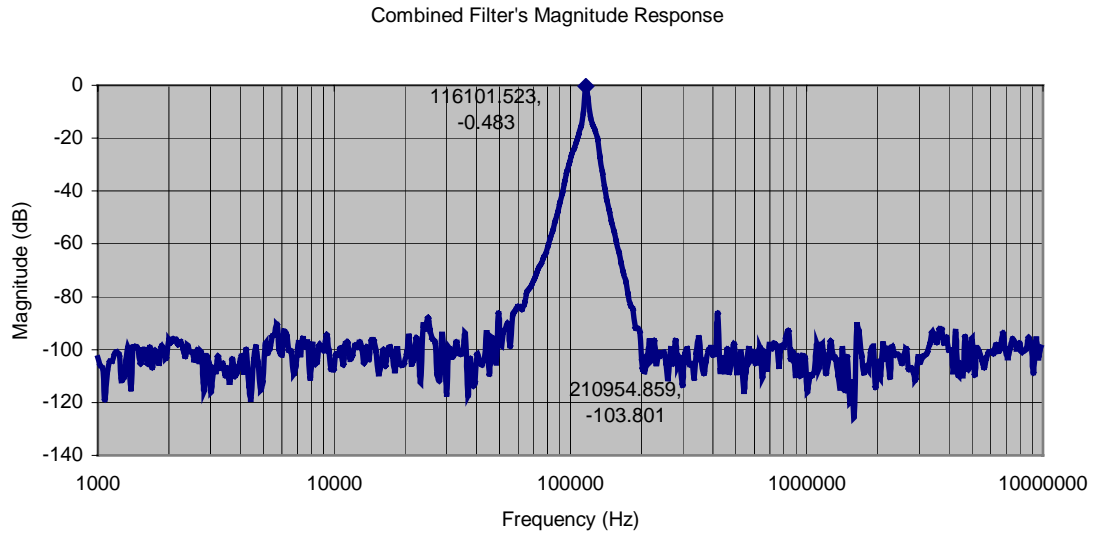


Figure 4.19 Bode plots for the passive-active combined bandpass filter

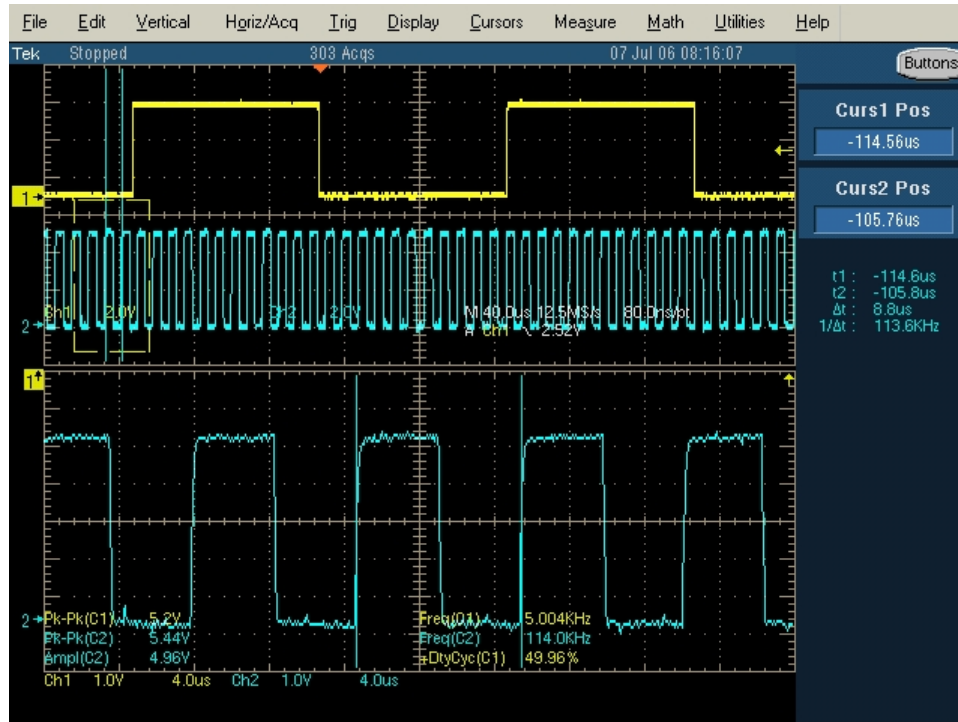


Figure 4.20 VCO input or digital data in (yellow trace); VCO output or FSK modulate signal (blue traces). The ‘Space’ frequency is zoomed.

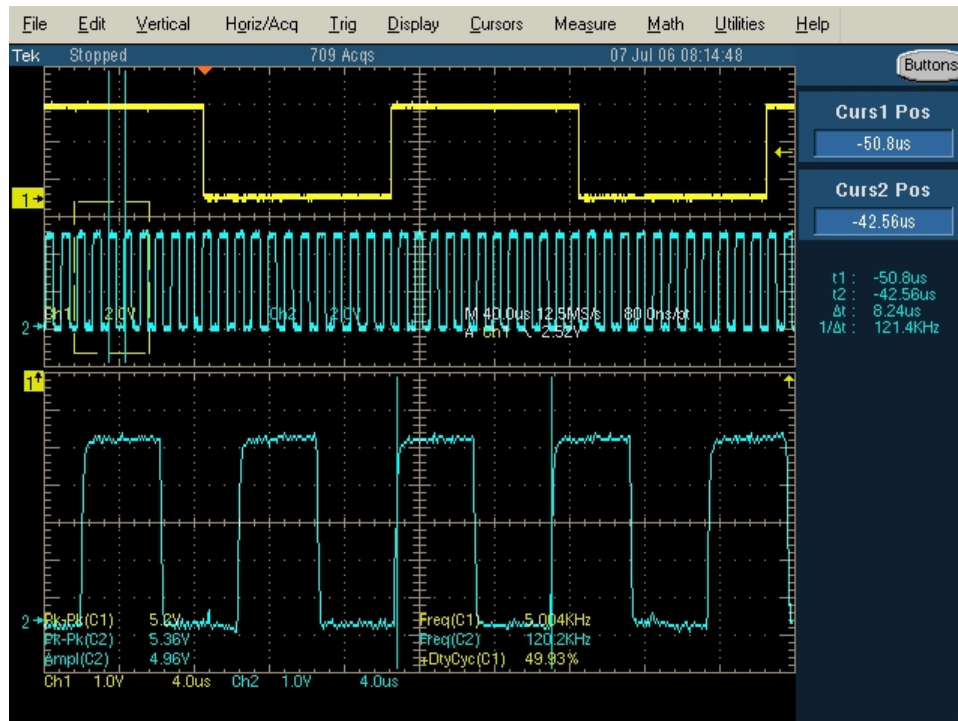


Figure 4.21 VCO input (yellow) and output (blue traces); ‘Mark’ is zoomed.

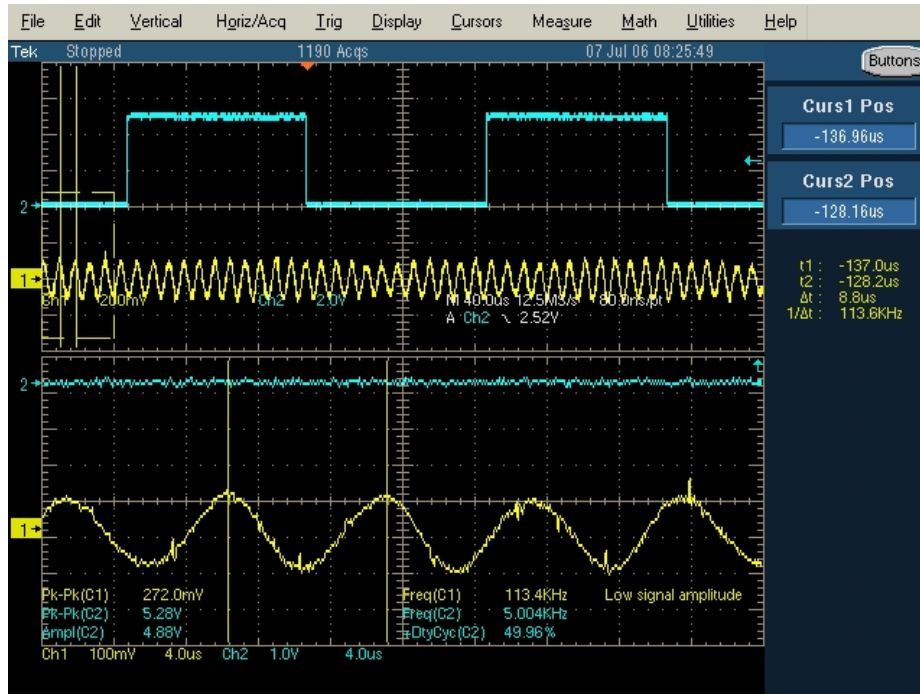


Figure 4.22 VCO input (blue) and the passive bandpass filter output (yellow).
‘Space’ in the filter output is zoomed.

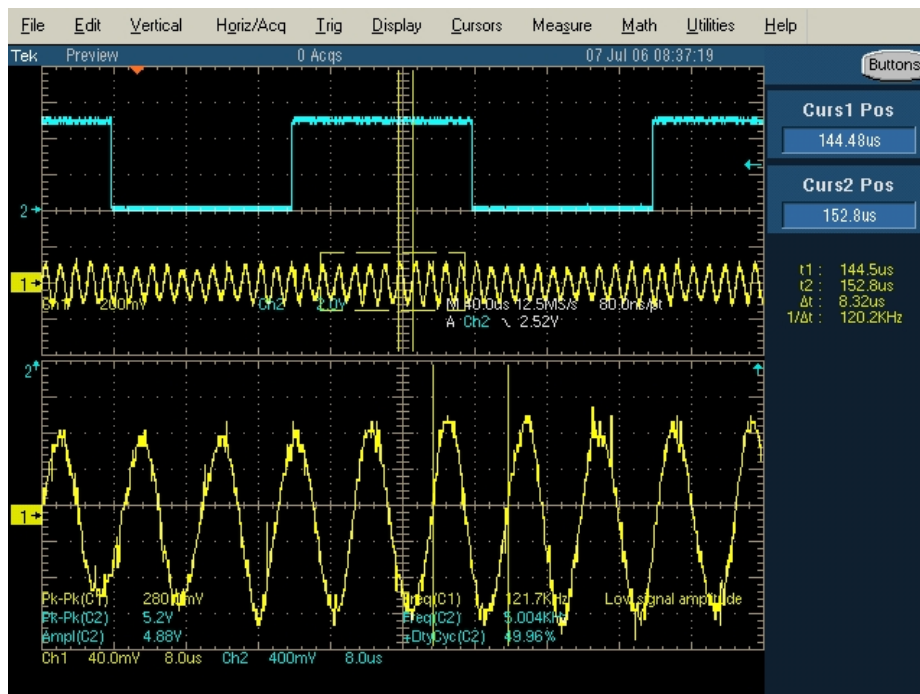


Figure 4.23 VCO input (blue) and the passive bandpass filter output (yellow).
‘Mark’ in the filter output is zoomed.

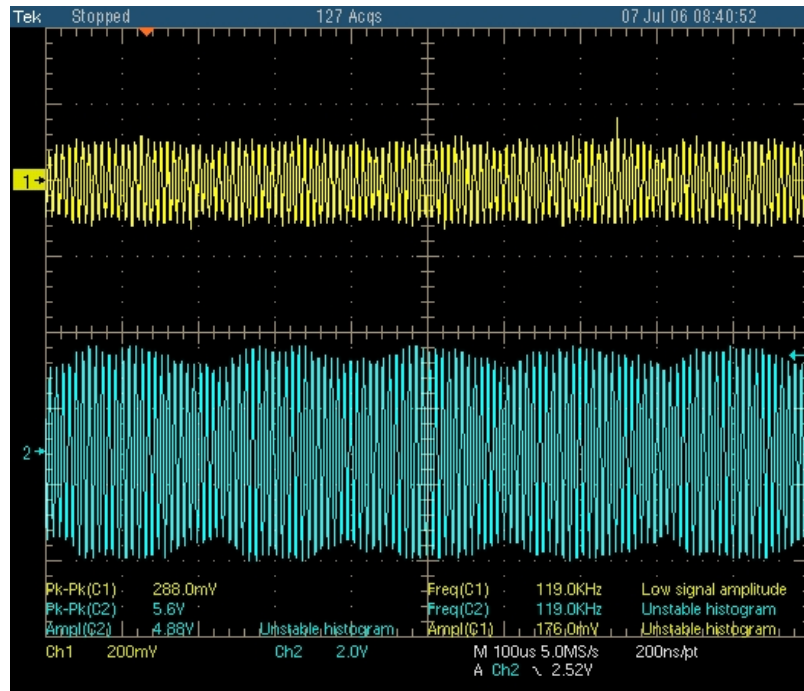


Figure 4.24 Passive bandpass filter and active filter's outputs (yellow and blue respectively)

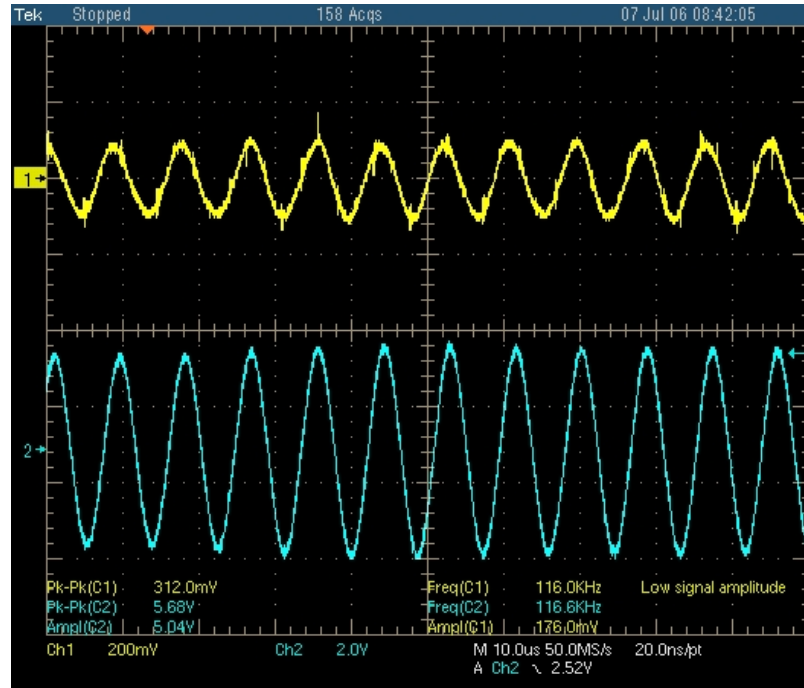


Figure 4.25 Passive bandpass filter and active filter's outputs zoomed. This figure demonstrates the amplification of passive filter output and improved SNR.

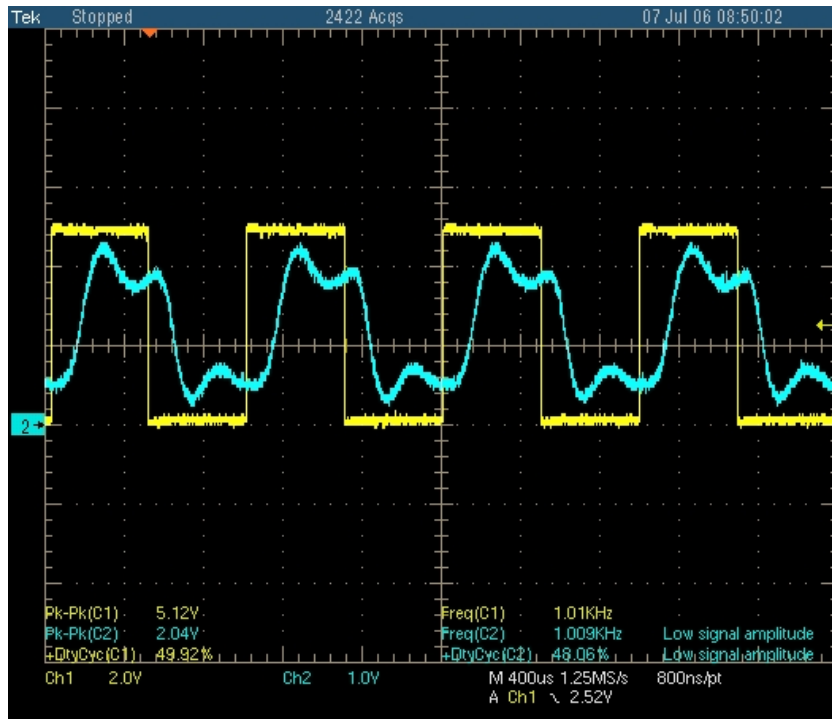


Figure 4.26 Demodulator output with 1kHz square wave signal (equivalent to a 2kbps data rate)

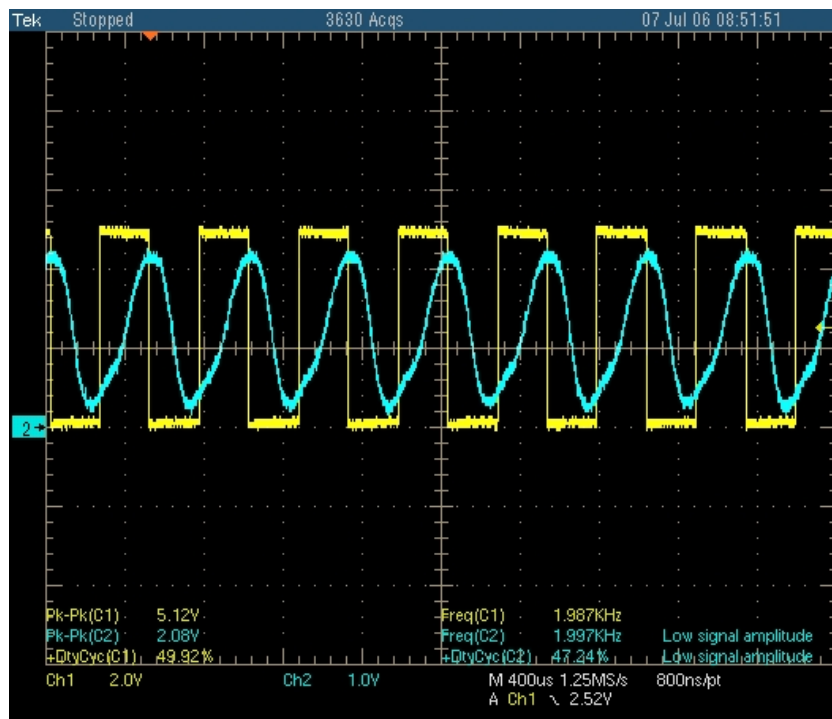


Figure 4.27 Demodulator output with 4kbps data rate

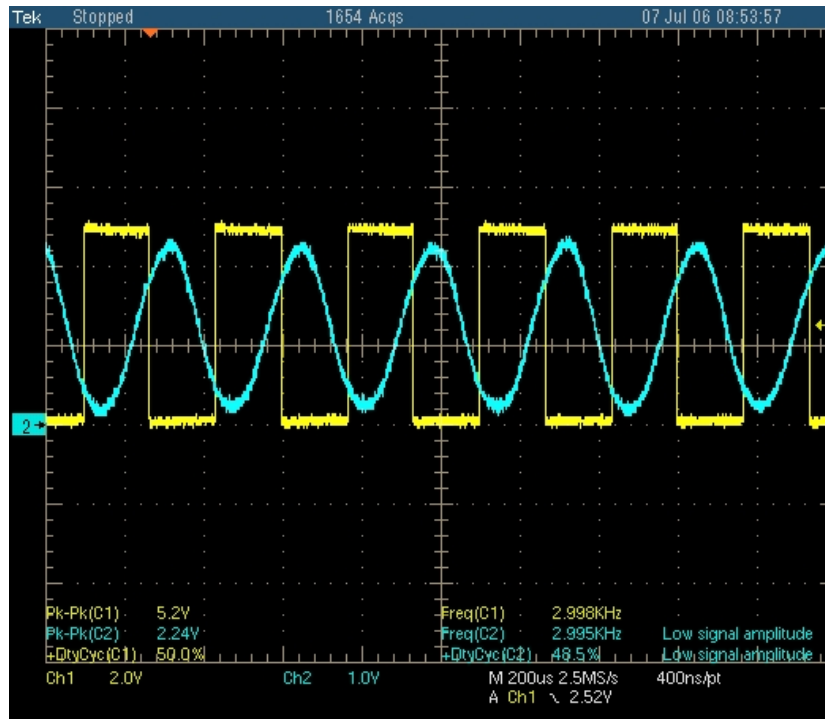


Figure 4.28 Demodulator output with 6kbps data rate

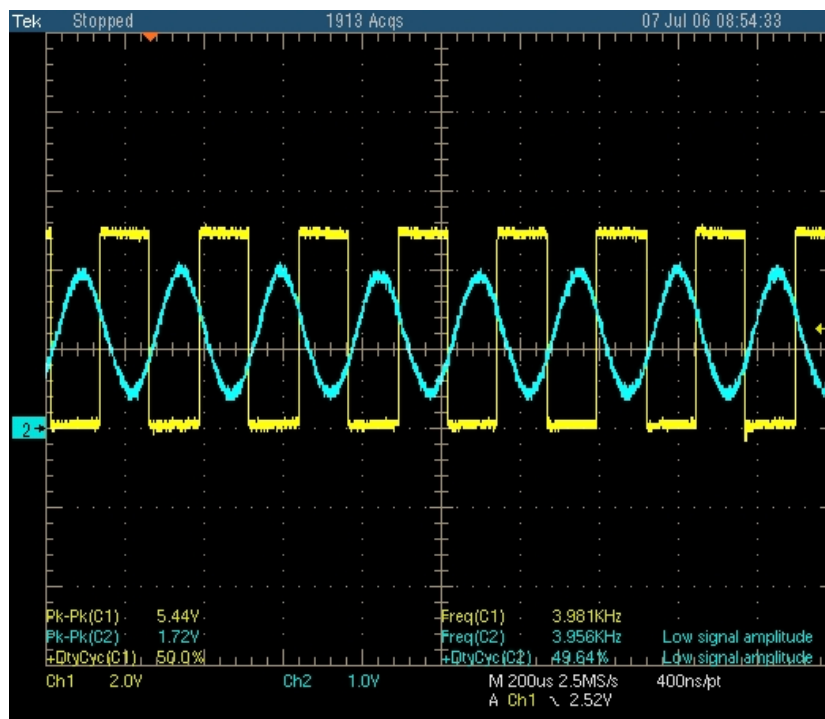


Figure 4.29 Demodulator output with 8kbps data rate

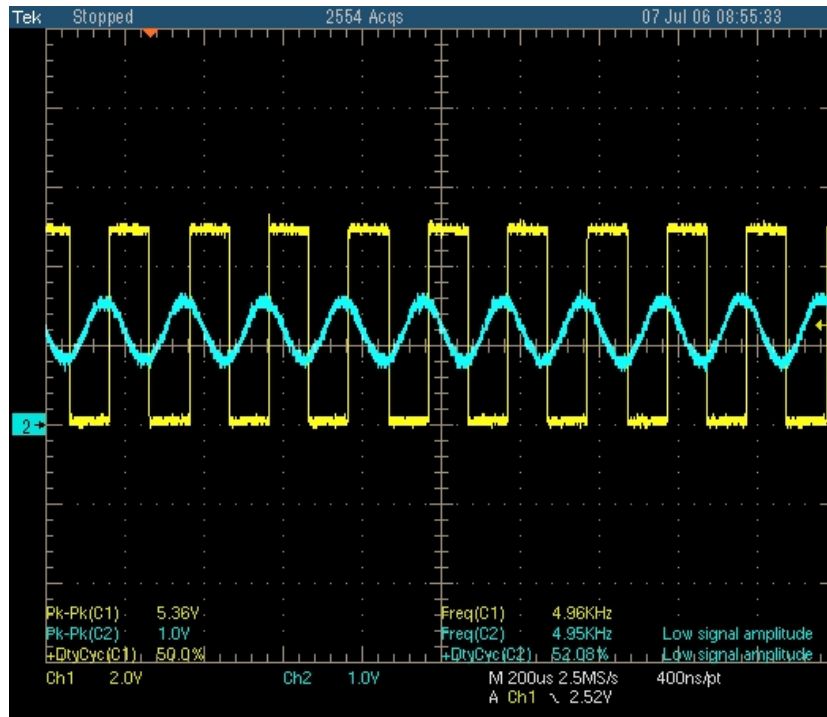


Figure 4.30 Demodulator output with 10kbps data rate

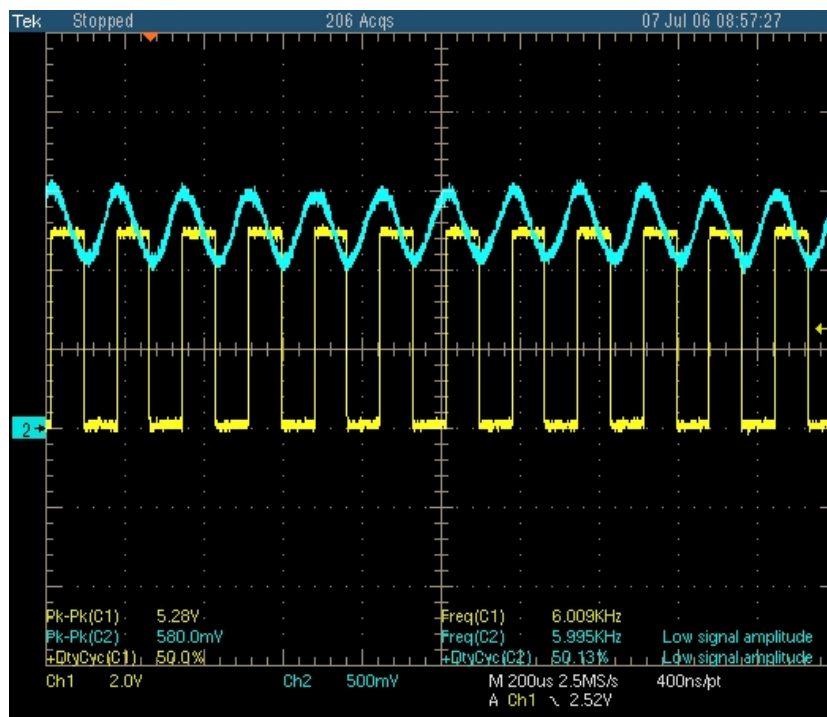


Figure 4.31 Demodulator output with 12kbps data rate

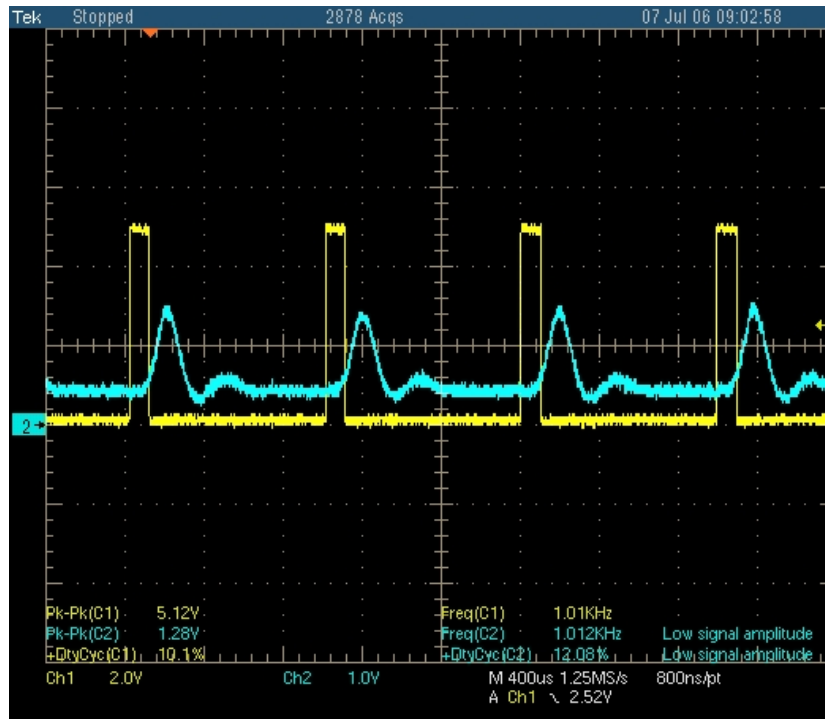


Figure 4.32 Demodulator output with 1kHz data signal of 10% duty cycle

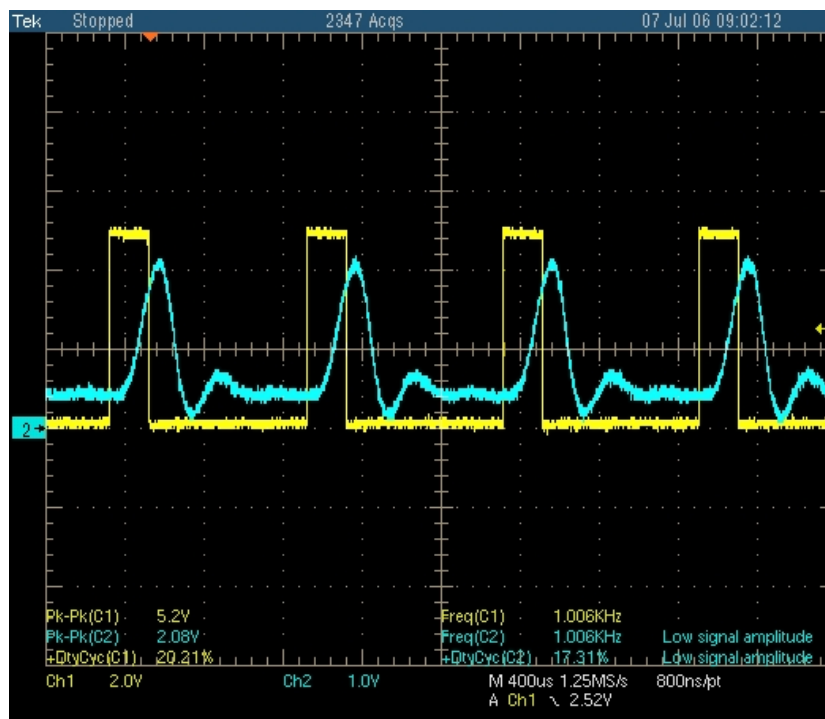


Figure 4.33 Demodulator output with 1kHz data signal of 20% duty cycle

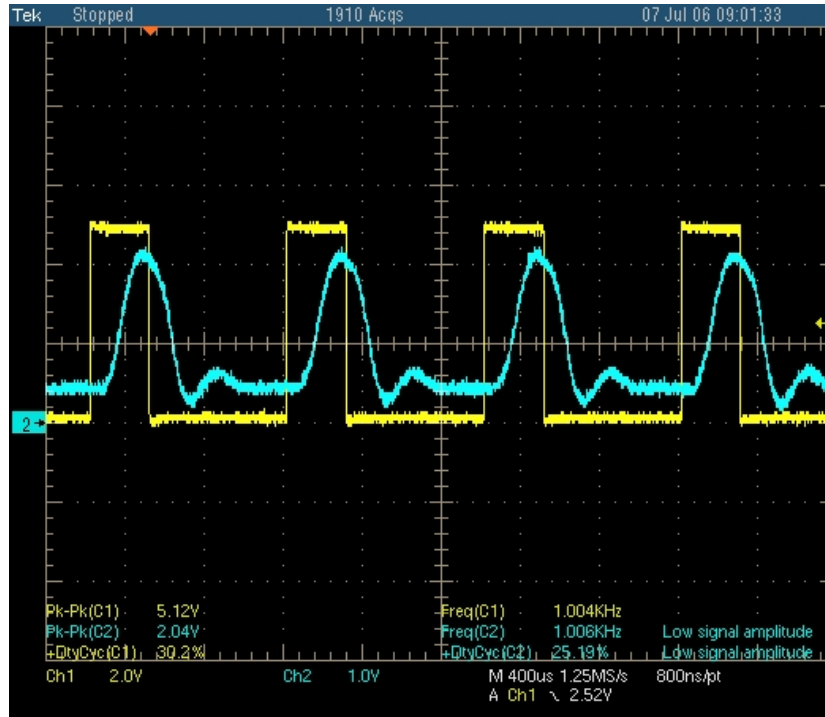


Figure 4.34 Demodulator output with 1kHz data signal of 30% duty cycle

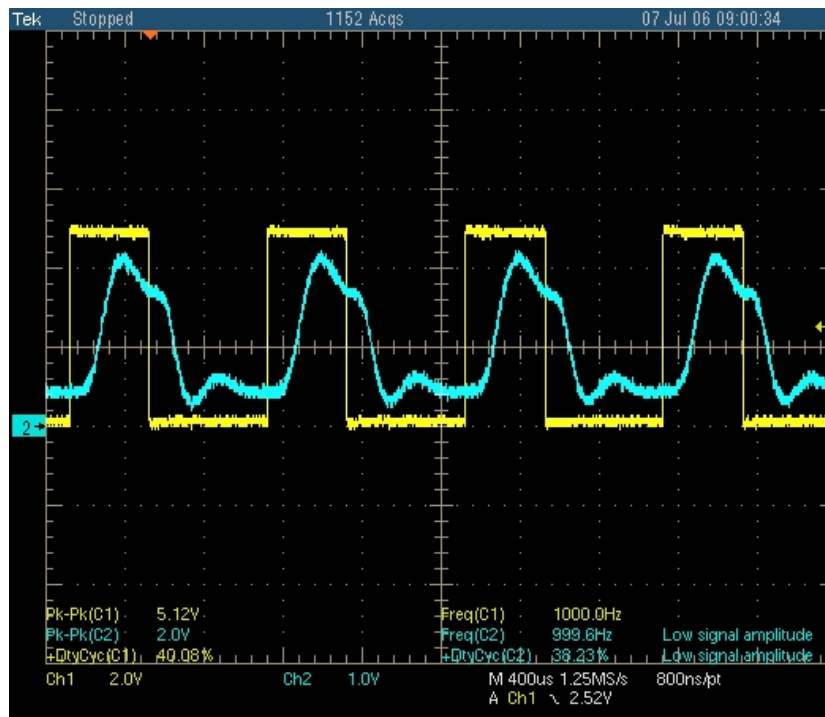


Figure 4.35 Demodulator output with 1kHz data signal of 40% duty cycle

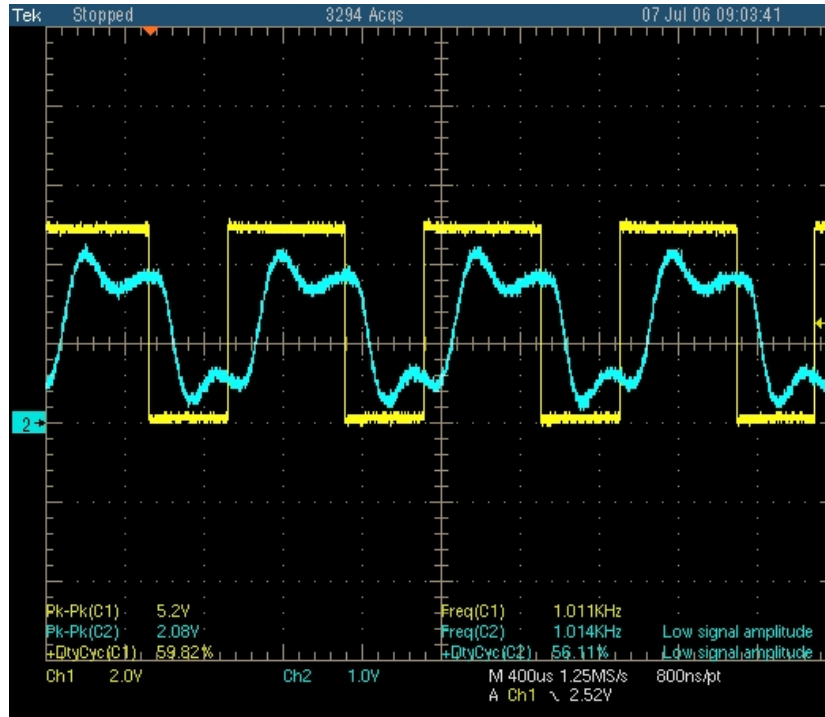


Figure 4.36 Demodulator output with 1kHz data signal of 60% duty cycle

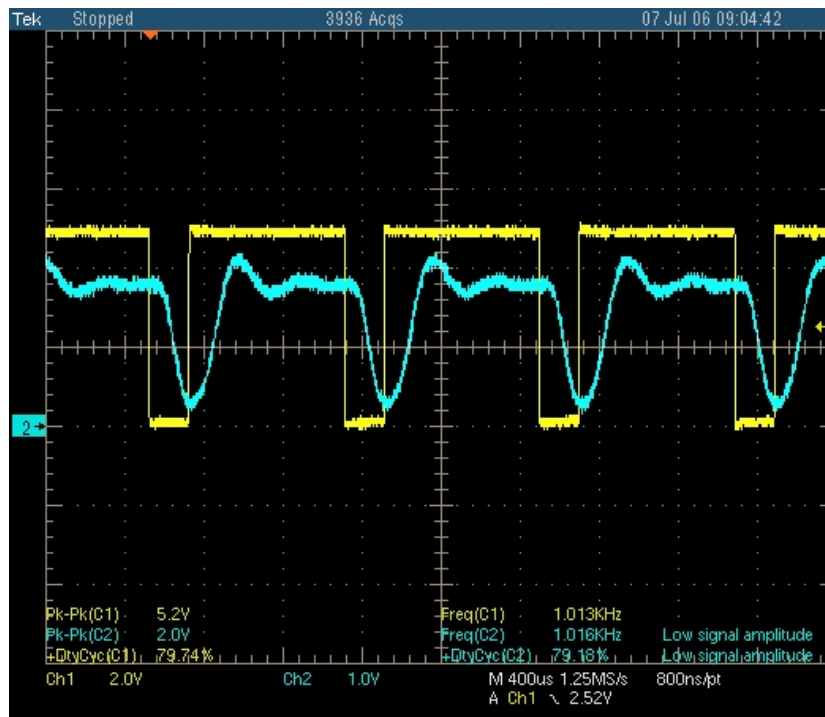


Figure 4.37 Demodulator output with 1kHz data signal of 80% duty cycle

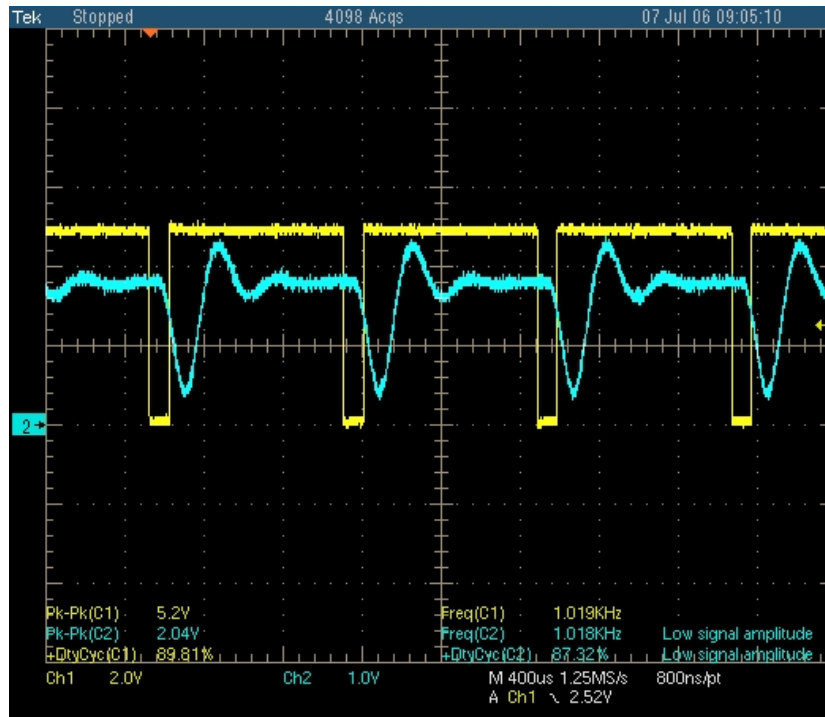


Figure 4.38 Demodulator output with 1kHz data signal of 90% duty cycle

wave signal contains two data bits, and therefore the 1kHz signal carries a total of 2000 bits in one second with equal number of ‘1’s and ‘0’s. This translates to a data rate of 2kbps. In this way, a 5kHz signal is equivalent to 10kbps of data. However, modeling of data in this way assumes that the data signal would have an equal share of ‘1’s and ‘0’s. In this case, it is completely justifiable because the target application’s (perfusion sensor system) sensor interface electronics generates digital data using the Manchester Encoding technique, which by principle produces equal number of ‘1’s and ‘0’s.

Nevertheless, in order to test the systems performance with unbalanced shares of ‘1’s and ‘0’s, a 1kHz square wave signal has been used with its duty cycle varied from 10% to 90% in steps. The 10% and 90% duty cycle conditions can be thought of as a single ‘1’ followed by nine ‘0’s and vice versa. Therefore, one cycle of the signal contains 10 data bits, which means a data rate equivalent to 10 times

the signal frequency. Similar analogies can be drawn for 20% and 80%, 40% and 60% duty cycles etc.

The system works well up to 10kbps of data rate using both data models. Beyond that, the performance becomes poor, mainly because, the system has been designed with a low PLL bandwidth. The demodulator PLL's bandwidth (capture range) can be increased to accommodate a higher data rate; however, there are certain practical limitations on that due to the low frequency carriers used for FSK transmission and limited performance of the CD4046 PLL chip. The reasons for using low frequency carriers are already discussed in section 4.2.

4.6.3 Summary of Results

The tests have been performed with the following operating conditions:

- Frequency of operation = 209.6kHz
- Supply voltage = 5V
- Primary regulator's output voltage = 1.975V
- Supply current = 0.32A
- Spacing between coils = 1.16cm

The demodulator PLL's bandwidth has been set almost equal to the modulator's (VCO) bandwidth, actually slightly higher than that. Therefore, a data rate has been achieved that is greater than the FSK bandwidth. Also, the data rate-to-carrier frequency ratio is quite high.

A summary of the results is provided in Table 4.3.

Table 4.3 Summary of Communication System Results

Mark frequency (kHz)	Space frequency (kHz)	FSK shift (kHz)	Maximum data rate (kbps)	FSK carrier (mid-frequency) (kHz)	Data rate - to-VCO bandwidth ratio	Data rate-to-carrier frequency ratio
121.4	113.6	7.8	10	117.5	1.28	0.085

The loop filter of the demodulator has been chosen such that there is a balance between the settling time and damping factor of the loop's transient response. There is always a trade off between these two parameters. If the settling time is low, a faster response is obtained, and hence the PLL locks quickly; however, it increases the overshoot present in the transient response, and thus decreases the noise margin. Therefore, the loop filter's transfer function (i.e., the pole location) has been adjusted by the use of a potentiometer for the filter resistor to obtain an optimum response.

CHAPTER 5

System Integration

Both the external and internal units of the proposed inductive powering and communication system were fabricated using printed circuit board technology to provide a robust prototype, and to enhance the ease of system measurement and testing. This chapter includes the complete schematics and layouts of the PCBs, photographs of the boards and test setup and some performance analysis of the complete system.

5.1 Complete Schematic Diagrams

Detailed schematics of the primary (or external) and secondary (or internal) units after integration of the powering and communication modules in both units were shown in Figure 5.1 and Figure 5.2 respectively. These schematics were used for laying out the prototype PCBs. In the final system prototype, some additional footprints have been incorporated that were not discussed in earlier chapters. For example, an LM339 comparator with hysteresis was added to the output of the demodulator to provide thresholding of the demodulator output. In addition, a low pass filter was added between the modulator (VCO) and the common-source amplifier in the internal unit to reduce the spectral lines introduced by the square wave FSK signals. During the final testing with the prototype PCBs, the additional components were not tested. However, it is generally a good practice to incorporate some degree of design flexibility during the prototyping stages of a circuit design work, so that future modifications and enhancements can be easily achieved.

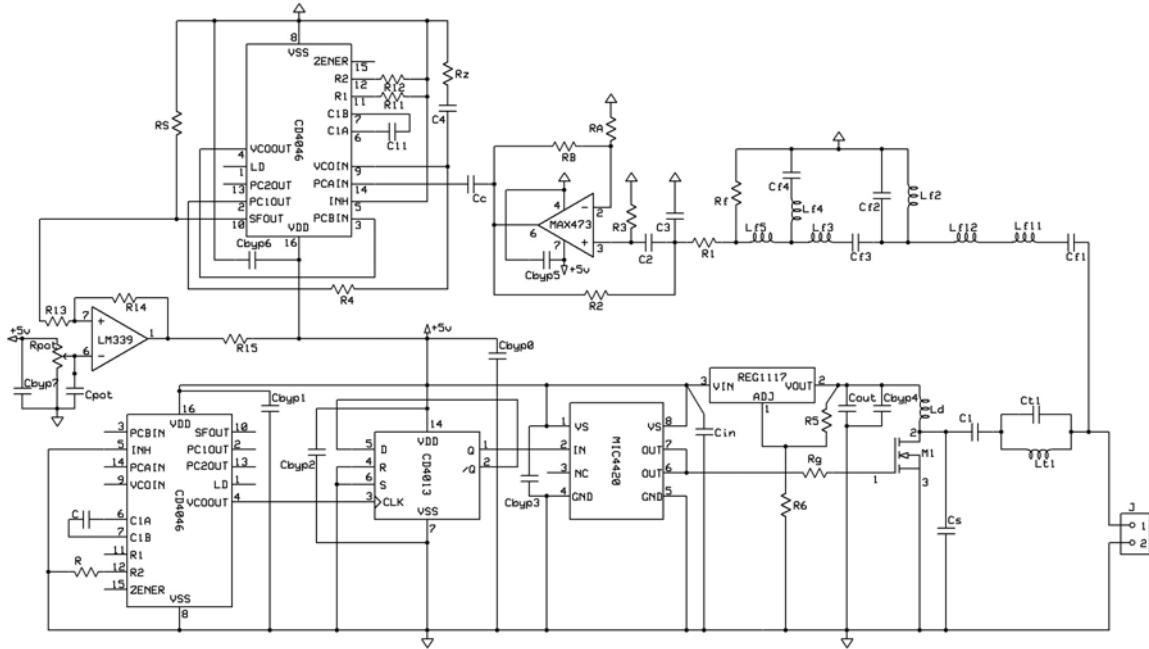


Figure 5.1 Schematic diagram of the PCB prototype external unit

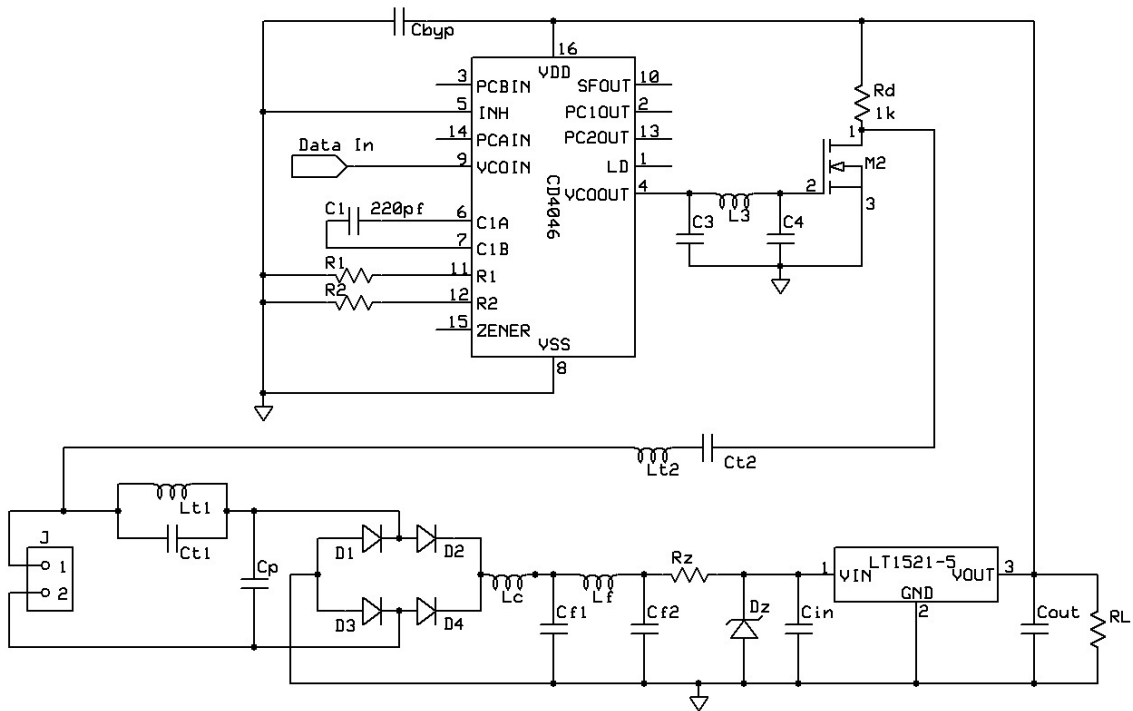


Figure 5.2 Schematic diagram of the PCB prototype internal unit

5.2 PCB Layouts

The PCBs were laid out using a simple vendor provided software, named ExpressPCB. Standard, two-layer PCBs were fabricated without a silkscreen or solder mask. Note that the Figures 5.3 and 5.4 include the silkscreen layer for better visual comprehension of the floor plan. The top-layer traces are colored red, while the bottom-layer traces are in green. Judicious grounding and routing techniques have been applied to minimize interferences. The original size of each of the boards was 3.8 inches \times 2.5 inches. However, the extra area of the internal unit's PCB was chopped off later.

5.3 Final Sets of Test Results

After integration of the powering system and communication system components in both the external and internal units, further experiments were performed to verify complete system performance and to determine the maximum link range. The complete system was operated with a fixed supply voltage and with a fixed primary drive frequency. Due to drift in the CD4046 chip used to generate the power-MOSFET's gate drive signal, some minor frequency variations were observed. However, in order to maintain consistent test conditions, the timing resistor (implemented by a potentiometer) of the VCO was adjusted periodically to compensate for VCO drift.

Keeping the main supply voltage constant, only two parameters were varied – the coil separation and the primary voltage regulator's output. The distance between the coils was varied using a combination of thin, plastic diskette cases and stacks of paper. As the distance varied, naturally the coupling and the delivered power changed. The primary regulator was then adjusted to provide the minimal input power to the Class-E driver required to maintain a constant voltage at the internal power recovery unit's regulator output. In this way, unnecessary wastage

of power was avoided in both external and internal units, and most importantly, almost identical test conditions were ensured for different sets of measurements.

The fixed test conditions were:

- Main supply voltage = 5V,
- Frequency of operation = 211.9kHz,
- Internal load voltage = 5V,
- Load: 200Ω resistive load, FSK modulator, and the gain stage,
- Approximate load current = 31mA (including the current drawn by modulator and gain stage), and
- Approximate load power = 0.155W

Measured data are provided in Table 5.1.

Using a similar approach to the one presented in section 3.4.3, the supply currents, power dissipations and efficiencies were calculated from the measured data, which are presented in Tables 5.2, 5.3 and 5.4.

Table 5.1 Test Results for the Complete System over Varying Distance

Distance (cm)	Supply current (A)	Primary regulator Output (V)	Primary Coil voltage, RMS (V)	Secondary coil voltage, RMS (V)	Secondary filter output, DC (V)	Secondary regulator input, DC (V)	Data rate (kbps)
0.56	0.32	1.49	3.80	9.6	6.9	5.6	Up to 10
1.15	0.28	2.00	4.95	10.6	7.5	6.2	Up to 10
1.72	0.28	2.77	6.70	9.0	6.5	5.2	Up to 10
2.30	0.30	3.66	8.67	9.1	6.6	5.3	Up to 10
2.50	0.31	4.00	9.40	5.8	6.6	5.3	Up to 10

Table 5.2 Secondary Unit Power Calculations Summary

Distance (cm)	Load current, I_L (mA)	Current in R_z , I_R (mA)	Secondary dc losses, P_{loss_dc} (W)	Secondary ac losses, P_{loss_ac} (W)	Power delivered to load, P_{load} (W)	Power converted to secondary coil, $P_{secondary}$ (W)
0.56	31	32.5	0.083	0.018	0.155	0.256
1.15	31	32.5	0.103	0.018	0.155	0.276
1.72	31	32.5	0.070	0.018	0.155	0.243
2.30	31	32.5	0.073	0.018	0.155	0.246
2.50	31	32.5	0.073	0.018	0.155	0.246

Table 5.3 Primary Unit Power Calculations Summary

Distance (cm)	Total supply current, I_{supply} (A)	Primary amplifier current including gate drive current, $I_{in,power}^*$ (A)	Primary amplifier current excluding gate drive current, $I_{in,amp}$ (A)	Total input power, P_{in} (W)	Net input power to Class-E amplifier including gate drive, P_{driver} (W)	Net input power to Class-E amplifier excluding gate drive, P_{amp} (W)
0.56	0.32	0.31	0.269	1.60	0.462	0.401
1.15	0.28	0.27	0.229	1.40	0.540	0.458
1.72	0.28	0.27	0.229	1.40	0.748	0.634
2.30	0.30	0.29	0.249	1.50	1.061	0.911
2.50	0.31	0.30	0.259	1.55	1.200	1.036

*This current is found by subtracting the primary regulator current and an estimated current drawn by the external communication system components from the total supply current.

Table 5.4 Efficiency Calculations Summary

Distance (cm)	Primary to secondary power conversion efficiency, $\eta_{\text{conv}} = P_{\text{secondary}} / P_{\text{amp}}$	Estimated link efficiency, $\eta_{\text{link}}^* = \eta_{\text{conv}} / \eta_{\text{drain}}$	Load efficiency excluding primary regulator & communication unit losses, $\eta_{\text{load_driver}} = P_{\text{load}} / P_{\text{driver}}$	Overall system efficiency for the given condition, $\eta_{\text{system}} = P_{\text{load}} / P_{\text{in}}$
0.56	63.8%	74.4%	33.5%	9.7%
1.15	60.3%	67.1%	28.7%	11.1%
1.72	38.3%	43.3%	20.7%	11.1%
2.30	27.0%	31.1 %	14.6%	10.3%
2.50	23.7%	29.6%	12.9%	10.0%

The plots of calculated efficiencies against distance are provided in Figure 5.5.

Discussions:

- It is known from the theory of inductive links that the link efficiency is a strong function of coupling factor (k) between the coils and hence of the coil spacing. This fact is revealed in the plots shown, as the efficiency drops drastically with increasing distance.
- Due to the inclusion of trapping networks both in the primary and secondary units, the drain efficiency and overall link response were somewhat reduced compared to the experiments involving only the powering system. Therefore, the calculated efficiencies decreased a small amount as expected.

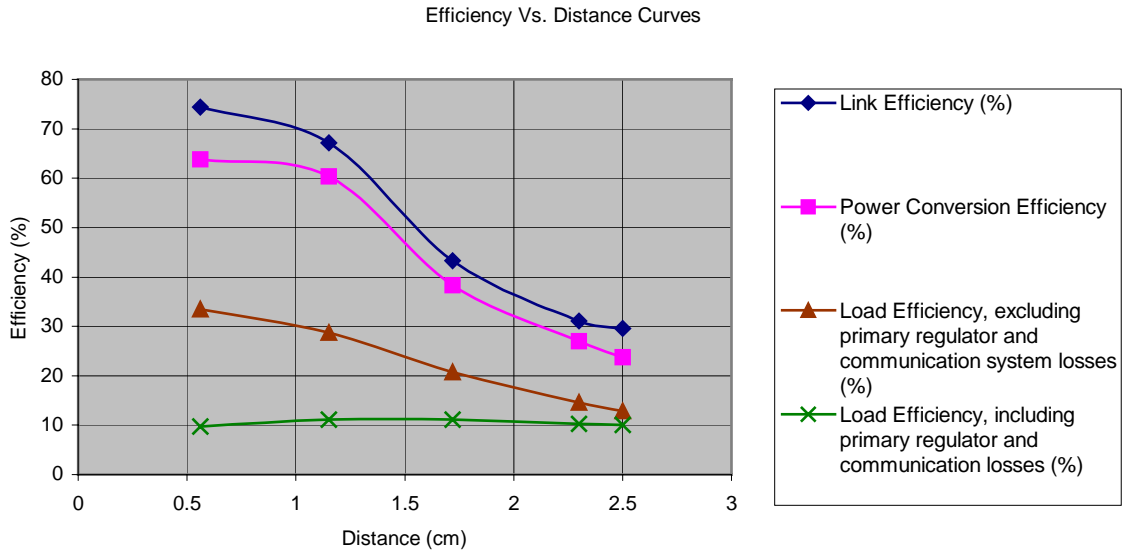


Figure 5.5 Efficiency vs. distance plots for the complete system

- The fourth (or lowermost) curve shows almost a constant efficiency irrespective of distance, because the link gain, and hence the power delivered to the system was manually adjusted by varying the primary unit's regulator every time the coil separation was varied. This indicates that the link can be optimized for efficiency and gain by manual or automatic gain control. However, this curve is not a true representation of the inductive powering system's efficiency, because it does not subtract the power dissipation in the external communication system blocks and the huge loss in the regulator itself. Therefore, it can be concluded that the primary unit's regulator or gain control block provides a means for optimizing the link over varying distances, but it can be quite wasteful when a large voltage difference between the input and output of the regulator is present, a condition that exists at short coil spacings.

5.4 Figures of Merit

Since inductive links are designed with various dimensions, and to meet a broad range of power conversion and data transmission requirements, it is not easy to compare one system to other just from one or two individual performance metrics. In order to compare the results of this work with other published works, two figures of merit were developed, one for the comparison of inductive powering system's performance, and the other one for backward telemetry. The figures of merit are as follows:

$$F.O.M_{power} = \frac{P_{out} \text{ (in mW)} \times D \text{ (in cm)}}{d_1 \text{ (in cm)} \times d_2 \text{ (in cm)}} \quad (5.1)$$

$$F.O.M_{backward_data} = \frac{\text{data rate (kbps)}}{\text{carrier frequency (kHz)}} \quad (5.2)$$

where, P_{out} = maximum power delivered to the load

D = maximum spacing between the coils

d_1 = diameter of the external coil

d_2 = diameter of the internal coil.

The calculated figures of merit for this work and the reported works summarized in Tables 2.1 and 2.2 are presented in Tables 5.5 and 5.6.

Table 5.5 Figure of Merit for Power Conversion

Reference No.	F.O.M _{power}
[4]	5.56
[9]	4.38
[10]	3.50
[31]	1.04
[52]	42.60
[53]	1.65
This Work	7.18

Table 5.6 Figure of Merit for Data Transmission

Reference No.	$F.O.M_{backward_data}$
[4]	0.0300
[12]	0.0800
[23]	0.0300
[8]	0.0300
[52]	0.0033
[53]	0.0025
This Work	0.0833

As can be seen, the proposed system performs very well in both power and data transfer over the inductive link. The system presented in [52] seems to be quite impressive in terms of power transfer; however, its figure of merit for backward data communication is very poor. In fact, if a combined figure of merit is defined by taking the products of the two, that is,

$$F.O.M_{combined} = F.O.M_{power} \times F.O.M_{backward_data} \quad , \quad (5.3)$$

it will be seen that the system presented in this work achieves the best figure.

The combined figures of merit of the aforementioned systems that implement a simultaneous power and backward data link are summarized in Table 5.7. This clearly demonstrates the effectiveness of the design presented in this work and associated implementation.

5.5 Photographs of Prototype Boards and Test Setup

In this section, photographs of the prototype boards and associated test system are provided. Figures 5.6-5.10 show the hardware components that make up the prototype design. Figures 5.11-5.13 provide views of the test setups associated with this work.

Table 5.7 Combined Figure of Merit

Reference No.	F.O.M _{combined}
[4]	0.167
[52]	0.141
[53]	0.004
This Work	0.598

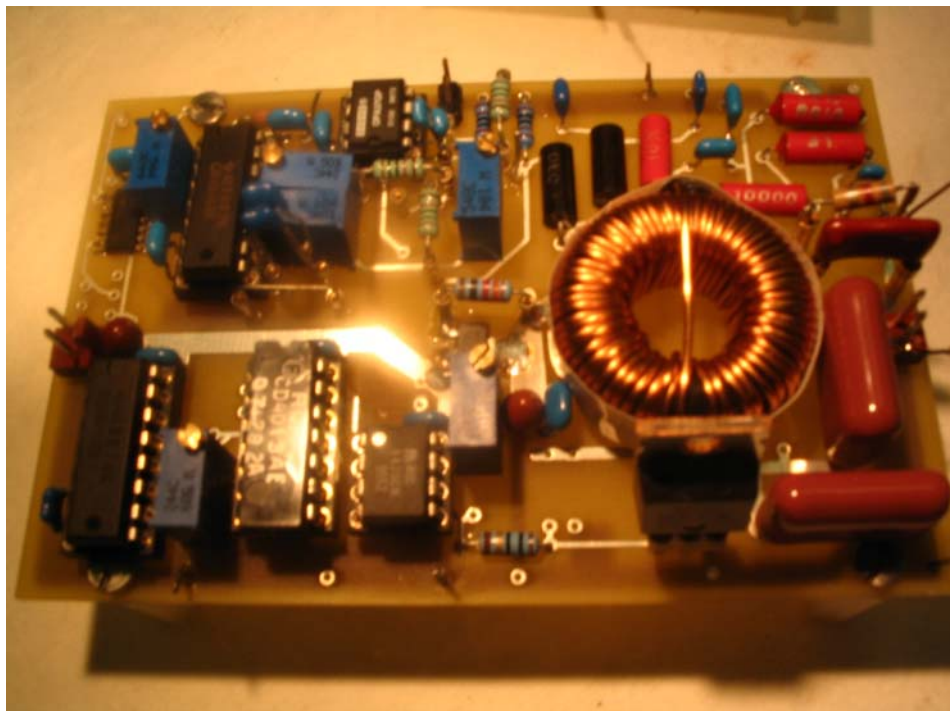


Figure 5.6 External unit on PCB

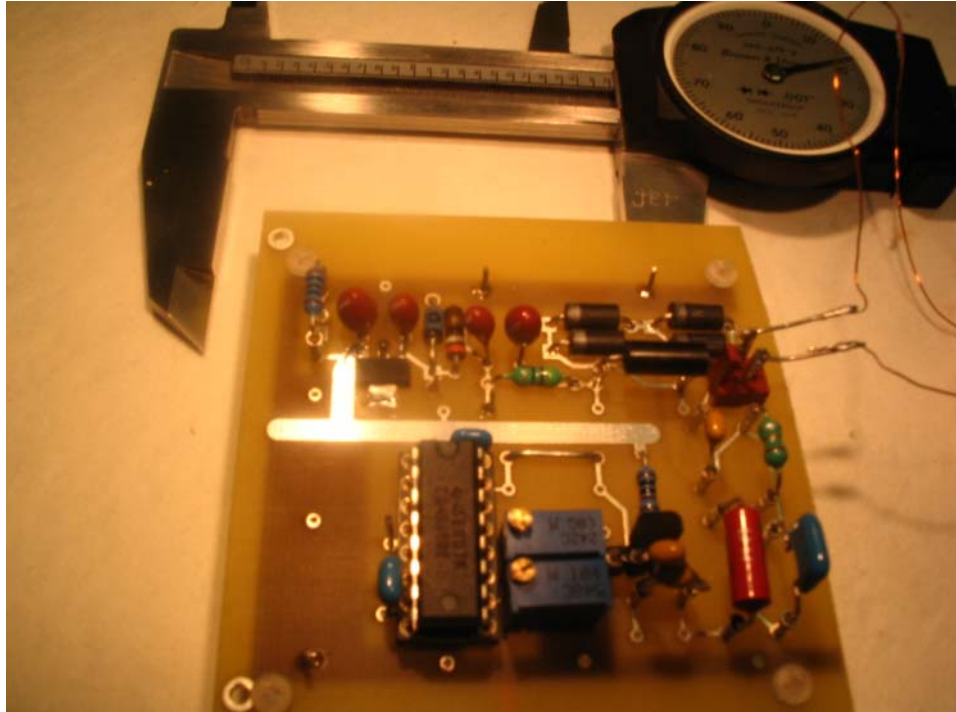


Figure 5.7 Internal unit on PCB



Figure 5.8 Primary (on the right) and secondary coils

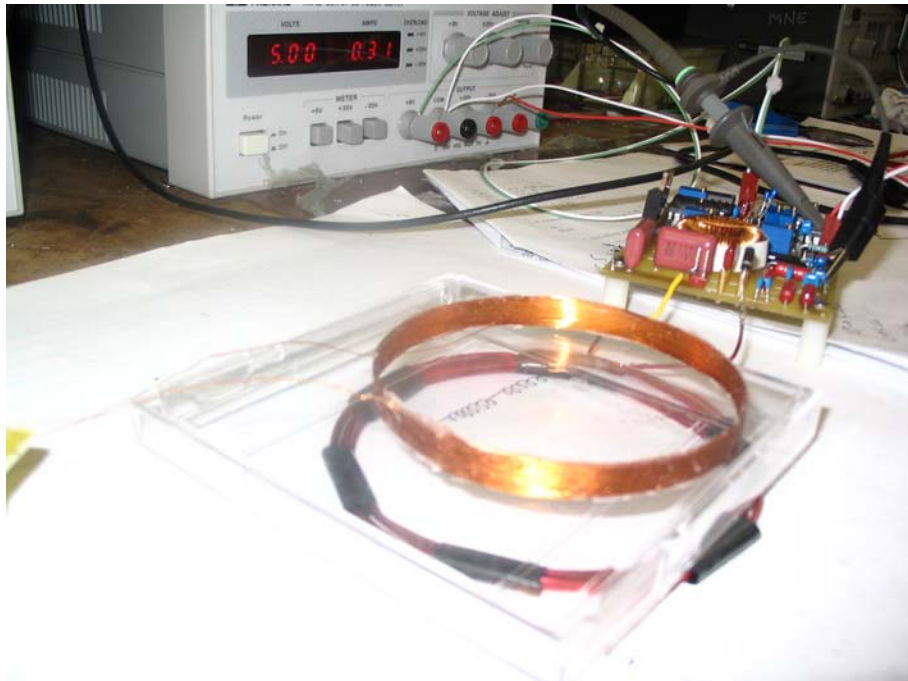


Figure 5.9 Secondary coil on top of the primary coil, separated by a plastic case



Figure 5.10 External and internal RF units, the inductive link (coils) and the perfusion sensor system's electronic interface (within the circumference of the secondary coil)

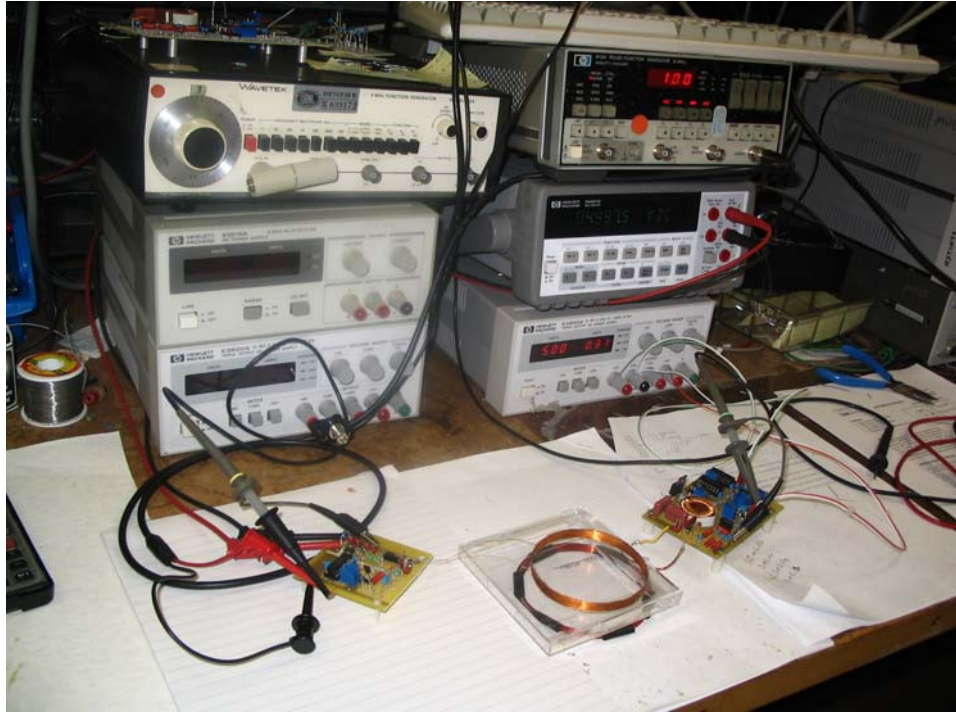


Figure 5.11 Typical lab setup: I



Figure 5.12 Lab setup: II

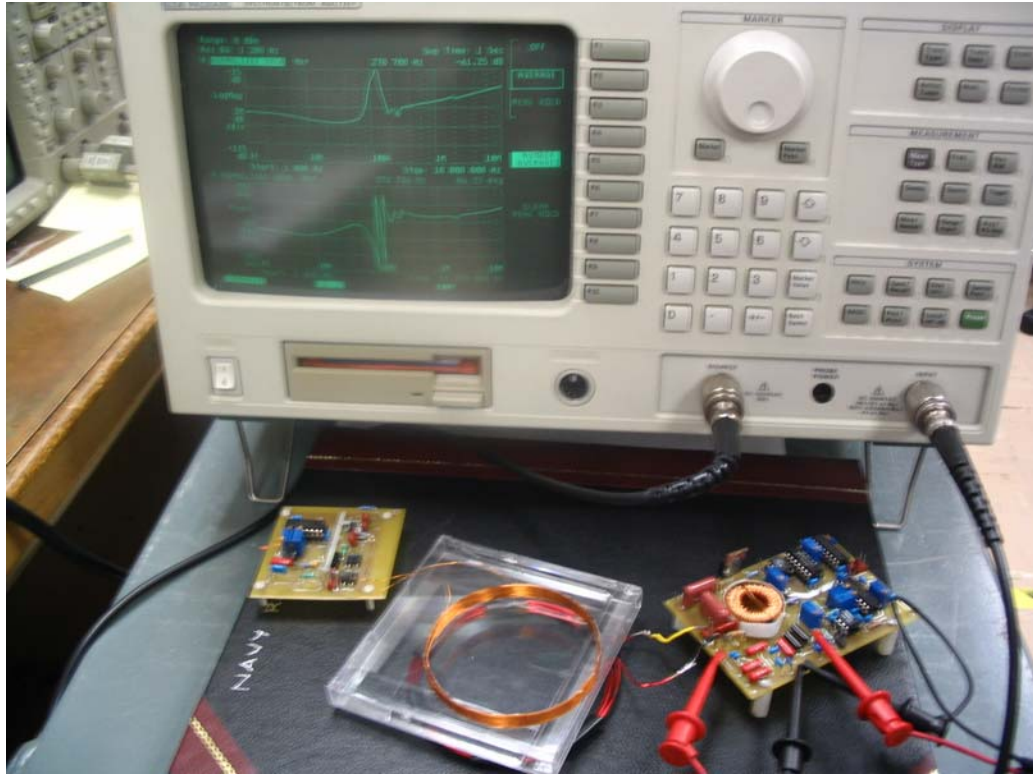


Figure 5.13 Network analyzer setup

CHAPTER 6

Conclusions and Future Directions

6.1 Thesis Conclusions

This thesis has presented an inductive link based remote powering and communication scheme for implantable sensor systems. The inductive link consists of two coaxially aligned circular coils, of which one coil is meant to reside inside human body, while the other one to be placed in an external unit located just outside of the body. Through transformer action, the link provides a means for transferring electrical power from the external to the internal unit that can be used by the implantable sensor interface electronics and communication module. The same link can be used for simultaneous transmission of digital data from the implant to the external unit, which is known as backward or reverse telemetry.

The external or primary coil is driven by a Class-E resonant power converter, which is one of the most efficient types in power amplification and conversion. The unit can deliver ample power to the implant system up to several hundred milliwatts over inter-coil distance ranging from 0 to 2.5cm, and with overall power transfer efficiency nearly 30% under optimum operating conditions. The range can be easily increased by increasing the supply voltage. An adjustable low-dropout voltage regulator with 1A output current capability has been incorporated in the prototype that offers the flexibility to the operator to adjust the system for maximum efficiency or maximum output power. With adjustable input power to the Class-E driver and variable operating frequency, a user can optimize the link performance for varying coupling conditions, up to a maximum coil spacing. The power transfer system was designed to operate at ~210kHz.

The backward communication scheme employs a power-efficient FSK modulation technique, and can support data rates of up to 10kbps. The mean carrier frequency for FSK is approximately 120kHz, which results in a 0.083 data rate-to-carrier ratio, which compares well with previously published work. In addition, a figure of merit incorporating both link power transmission performance and data rate-to-carrier ratio indicated better overall performance than previously published designs.

6.2 Future Work

The developed system showed promising performance in many areas. However, there are a number of enhancements that should be investigated to further improve the system and increase its application scope in the area of biomedical implants. Listed below are a number of focus areas that could lead to a much improved and more widely applicable system.

Automatic Gain Control and Automatic Tuning: An inductive link is inherently a coupling-sensitive system, which translates to gain variations with misalignment, spacing and lateral displacement. Even if some geometric and stagger-tuning approaches are employed, the system will still suffer from this problem due to variations in certain environmental conditions. Two approaches were implemented in the drive circuit to circumvent this problem: adjustable voltage and adjustable drive frequency. Proper selection of these parameters requires careful adjustment and monitoring. Therefore, an automatic gain control, and an automatic search for the optimum frequency of operation would be useful additions to the circuit.

Bandwidth Enhancement: Despite the generally narrowband characteristics of an inductive link, many works have been reported that accommodate quite high data transmission rates, some of which are in excess of 1Mbps. Obviously, the

data rate-to-carrier frequency ratio is a more important issue in the presented work than the data rate, since the frequency of operation was considerably lower; mainly due to concerns over EM exposure and tissue absorption. Nonetheless, the inductive links can easily be operated up to several tens of MHz and still be safe for most clinical applications, if proper attention is paid to these issues during the design stage. Moreover, there are several modulation techniques that are highly bandwidth efficient and can support very high data rates over a considerably narrowband link. Aside from that there are techniques that can be used to increase the bandwidth for a given modulation scheme and for the link itself. These possibilities can be investigated, and if successful, will make the link better suited for many applications requiring high data rate.

ASIC-level Integration and On-chip Inductors: Using ASIC technology, particularly for the complete implantable unit, the size of the system, and hence its applicability can be greatly reduced. On-chip inductors and sub-miniature microcoils are being investigated for specific tasks nowadays. Although the coupling performance of on-chip inductors is extremely poor, they have been used for certain low-power applications, including RFID transponders and biomedical Microsystems [68, 69, 70]. The work presented in [69] reports an inductive link with an on-chip receiver coil, which is capable of transferring 12mW of power at a link distance of up to 3cm. Investigations can be carried out to assess the feasibility of using on-chip inductors for moderate-power inductive links, and if their use can be proved successful in implantable system powering, that will undoubtedly commence a new era in implant systems.

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Appendix

A.1 : SPICE Simulation Netlists

A.1.1 Netlist for Powering System Simulation

* Primary Netlist *

```
VDC 11 66 1.76V
X_M1 12 13 66 irfr_u3710z
Ld 11 12 481uH ic=0
VP 13 66 PULSE 0 5 0 0.03u 0.03u 2.36u 4.72u
*VAC 12 66 AC 1
Cs 12 66 100n ic=0
Rs 12 14 0.315
C1 14 15 120n ic=0
L1 15 66 7.4uH ic=0
*L1 15 66 5.8uH ic=0
```

* Secondary Netlist *

```
L2 8 2 267uH ic=0
R_L2 8 1 5.5
C2 1 2 2.225n ic=0

D_D6 0 1 DI_1N5819HW
D_D8 0 2 DI_1N5819HW
D_D7 1 3 DI_1N5819HW
D_D9 2 3 DI_1N5819HW
L_Lc 3 33 760uH ic=0
R_Lc 33 4 11.4
C_Cf1 0 4 1u ic=0
C_Cf2 0 5 1u ic=0
L_Lf 4 44 45uH ic=0
R_Lf 44 5 1.6
R_Rz 5 6 40
X_D11 0 6 DI_1N4739A
X_Reg 7 7 0 9 6 LT1521
Cin 0 6 0.8u ic=0
Cout 0 7 10u ic=0
R_R2 7 0 200
```

* Transformer Netlist *

```
K1 L1 L2 0.453
Riso 2 66 9e10
```

* Including model files *

```
.INC "..\Spice Models\IRF\irfr_u3710z.spi"
.INC "..\Spice Models\Diodes Inc\1N4739A.txt"
.INC "..\Spice Models\Diodes Inc\1N5819HW.txt"
.INC "..\Spice Models\LT\LT1521.txt"
```

```

** Analysis setup **

.TRAN 50ns 3000us
*.AC DEC 10000 1k 10meg
.OP

.PROBE
.END

```

A.1.2 Netlist for 4th Order Butterworth Passive BPF Simulation

```

* Passive Bandpass Filter Netlist *

.SUBCKT BP_BUTTER4_120K 1 12 100

* Dummy Resistors Required For Spice Have Been Added to Net List.

C1      1      2      94.9pF
R1      1      2      1E+11
L2      2      3      18.77mH
R2      3      4      0.002269*F
L3      4      5      508uH
R3      5      0      5.604E-05*F
C4      4      0      4.15nF
R4      4      0      1E+11
C5      4      6      220pF
R5      4      6      1E+11
L6      6      7      9.3mH
R6      7      8      0.001499*F
L7      8      9      868uH
R7l     9      1      0 0.0001353*F
C7      10     0      656pF
R7c     10     0      1E+11
L8      8      11     0.91mH
R8      11     12     0.0002006*F
Rl      12     0      1000

.ENDS

X1      1      2      0      BP_BUTTER4_120K

*Xf     1      10     FSK
V1      1      0      AC      1
*VIN    1      10     SIN 0 0.2 130k 0 0 0
*VN1    10     20     AC      1      SIN 0 9.8 200k 0 0 0
*VN2    20     30     SIN 0 2.13 400k 0 0 0
*VN3    30     40     SIN 0 0.858 600k 0 0 0
*VN4    40     50     SIN 0 0.114 800k 0 0 0
*VN5    50     60     SIN 0 0.288 1000k 0 0 0
*VN6    60     61     SIN 0 0.040 1200k 0 0 0

```

```

*VN7  60    62          SIN 0 0.156 1400k 0 0 0
*VN8  62    63          SIN 0 0.102 1800k 0 0 0
*VN9  63    64          SIN 0 0.068 2200k 0 0 0
*VN10 64    65          SIN 0 0.079 80k   0 0 0
*VN11 65    66          SIN 0 0.174 120k  0 0 0
*VN12 66    67          SIN 0 0.053 160k  0 0 0
*VN13 67    68          SIN 0 0.048 240k  0 0 0
*VN14 68    69          SIN 0 0.065 320k  0 0 0
*VN15 69    70          SIN 0 0.028 360k  0 0 0
*VN16 70    71          SIN 0 0.109 480k  0 0 0
*VN17 71    72          SIN 0 0.024 520k  0 0 0
*VN18 72    73          SIN 0 0.026 680k  0 0 0
*VN19 73    0           SIN 0 0.018 720k  0 0 0

```

```

*.INC "..\Partial Data\switch_fsk.cir"

```

```

.AC DEC 1000 1000 10MEG
*.TRAN 50ns 1ms
.PROBE
.END

```

A.1.3 Netlist for Single-Stage Sallen-Key Active BPF Simulation

```

* Sallen-Key Bandpass Filter Netlist *

```

```

.SUBCKT SKBP280_1 6 5 10
X1  1  2  3  4  5  OP-27G
*X1  1  2  3  4  5  60 AD844A

R1  6  7  10k
R2  7  5  10k
R3  1  10 10k

*R1  6  7  20k
*R2  7  5  20k
*R3  1  10 20k

RA  2  10 1k
RB  2  5  3.22k

*C1  7  10 78p ic=0
*C2  7  1  78p ic=0

C1  7  10 184p ic=0
C2  7  1  184p ic=0

VDD 3  10 5
VEE 4  10 -5

```



```
*VDD 3      10      15
*VEE 4      10     -15

.ENDS

X2    6      5      0      SKBP280_1
VIN   6      10     AC      1      SIN 0 0.1 282k 0 0 0
VN    10     0      SIN 0 0.01 200k 0 0 0

.INC "..\Spice Models\TI\OP-27G.inc"
*.INC "..\Spice Models\AD\ad844a.cir"

*Analysis Setup

.OP
.TRAN 50ns 1ms
.AC DEC 10000 1k 10meg
.PROBE
.END
```

Vita

Mohammad Ahsanul Adeeb was born in Dhaka, Bangladesh. He did his secondary and higher secondary level schooling in Govt. Laboratory High School and Dhaka College, Dhaka. Being interested in electronics, he then pursued a degree in Electrical Engineering at Bangladesh University of Engineering and Technology (BUET), Dhaka, and graduated with a Bachelor's degree in March 2002. He then worked as an Engineer in Telekom Malaysia International, Bangladesh (TMIB) Limited for a few months and as an Instructor in Southeast University, Dhaka for about a year.

M. Adeeb entered the University of Tennessee, Knoxville in Fall 2003 and worked as a graduate research and teaching assistant during his pursuit of a Master of Science degree in Electrical Engineering. As a graduate research assistant, he worked in a few funded projects of the Analog VLSI and Devices Laboratory. He started his MS research in November 2005 through a joint collaboration between the University of Tennessee and Oak Ridge National Laboratory.

After completing his Master's degree, he will start his career as an Analog Design Engineer at RF Micro Devices, Greensboro, North Carolina. M. Adeeb's professional interests include analog/mixed-signal IC design, RF circuits and systems, and solid-state devices.