5-2010

A Fully Integrated High-Temperature, High-Voltage, BCD-on-SOI Voltage Regulator

Benjamin Matthew McCue
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To the Graduate Council:

I am submitting herewith a thesis written by Benjamin Matthew McCue entitled "A Fully Integrated High-Temperature, High-Voltage, BCD-on-SOI Voltage Regulator." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Benjamin J. Blalock, Major Professor

We have read this thesis and recommend its acceptance:

Benjamin J. Blalock, Leon M. Tolbert, Syed K. Islam

Accepted for the Council:
Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

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A Thesis
Presented for the
Master of Science Degree
The University of Tennessee Knoxville

Benjamin Matthew McCue
May 2010

Acknowledgments

I would like to acknowledge my graduate committee Dr. Leon Tolbert, Dr. Syed Islam, and Dr. Benjamin Blalock for their insight, support, and dedication to educating future engineers. Having the knowledge and support of a very strong faculty greatly enhances the ability to prepare oneself for a career in electrical engineering.

I would also like to recognize the peer support of the entire Integrated Circuits and System Laboratory (ICASL) team. Their continued assistance with course work and research made pursuing post-graduate education a rewarding experience. A special thanks to ICASL members Robert Greenwell and Ross Chun.

Also, I would like to reiterate the support I received from my major professor Dr. Blalock. Without his support, financially and intellectually, reaching this point in my education would not have been possible. Dr. Blalock prepares his students for engineering careers as well as any student could hope.

Lastly, I would like to thank my family for their unconditional support. My wife, Jenna, followed me every step of the way through this demanding process. I would like to thank my late father, David, for his inspiration to choose a career in electrical engineering, and while he is not here now, I know he is proud.

Abstract

Developments in automotive (particularly hybrid electric vehicles), aerospace, and energy production industries over the recent years have led to expanding research interest in integrated circuit (IC) design toward high-temperature applications. A high-voltage, high-temperature SOI process allows for circuit design to expand into these extreme environment applications. Nearly all electronic devices require a reliable supply voltage capable of operating under various input voltages and load currents. These input voltages and load currents can be either DC or time-varying signals. In this work, a stable supply voltage for embedded circuit functions is generated on chip via a voltage regulator circuit producing a stable 5-V output voltage. Although applications of this voltage regulator are not limited to gate driver circuits, this regulator was developed to meet the demands of a gate driver IC. The voltage regulator must provide reliable output voltage over an input range from 10 V to 30 V, a temperature range of −50 ºC to 200 ºC, and output loads from 0 mA to 200 mA. Additionally, low power stand-by operation is provided to help reduce heat generation and thus lower operating junction temperature. This regulator is based on the LM723 Zener reference voltage regulator which allows stable performance over temperature (provided proper design of the temperature compensation scheme). This circuit topology and the SOI silicon process allow for reliable operation under all application demands. The designed voltage regulator has been successfully tested from −50 ºC to 200 ºC while demonstrating an output voltage variation of less than 25 mV under the full range of input voltage. Line regulation tests from 10 V to 35 V show a 3.7-ppm/V supply sensitivity. With the use of a high-temperature ceramic output capacitor, a 5-nsec edge, 0 to 220 mA, 1-µsec pulse width load current induced only a 55 mV drop in regulator output voltage. In the targeted application, load current pulse widths will be much shorter, thereby improving the load transient performance. Full temperature and input voltage range tests reveal the no-load supply current draw is within 330 µA while still providing an excess of 200 mA of load current upon demand.

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1. Introduction

1.1 – Motivation

Research centered around hybrid-electric vehicles continues to expand as the need to reduce dependence on fossil fuels increases. The electric motors in these vehicles show drastic increases in automotive fuel efficiency when compared to standard combustion engines. The extreme environment presented by these hybrid-electric engines can produce temperatures approaching 200 °C [1]. Of the many electrical components required in the implementation of these vehicles, high power DC-DC converters and DC-AC inverters are the cornerstone of generating drive-capable energy from battery power [1]. These energy converters require large drive currents to efficiently operate. The gate driver is a device that provides transient currents to the gates of these power devices [2]. Central to the implementation of the gate driver is the need for a stable voltage supply for its switching circuits [2]. Load current and input voltage variations create a demand for a voltage regulator capable of operating effectively over a variety of conditions. Current high-temperature voltage regulators capable of this operation do not yet effectively meet the demands of the gate driver circuits, which has led to the development of a LM-723 Zener reference-based voltage regulator in a high-temperature, high-voltage silicon-on-insulator (SOI) process (a commercially-available 0.8 micron SOI, BJT-CMOS-DMOS (BCD) process). In addition to the automotive application, the designed high-temperature voltage regulator has a wide range of potential applications which include aerospace and energy production industries. The uniqueness of this design stems from the wide operating temperature and wide input voltage range.

1.2 – Thesis Organization

This thesis illustrates the design process for the implemented voltage regulator. The details of the LM723 voltage regulator (on which this design is based) are examined as well as design steps of the voltage regulator developed for the specific application. Simulation verification of the post-extraction design illustrates the design concepts in practice. Post-fabrication functionality testing over the entire range of operating conditions demonstrates properly functioning design

implementation. A design review highlights the performance capabilities of the voltage regulator while exploring potential design improvements.

2. Background and Literature Review

2.1 – Voltage Regulator Background

The general term "voltage regulator" simply describes a device that maintains a constant output voltage level regardless of outside influence (input voltage, load condition, temperature) [3]. Linear voltage regulator topologies (non-switching technology) are broken down into two main categories: series and shunt regulators. In general, series regulators provide better temperature performance than shunt regulators; the wide operating temperature for this voltage regulator project directs the choice of regulator topology to employ a series configuration [3]. The series regulator also allows for a greater input voltage to output voltage differential than the shunt regulator, and therefore, proves to be the obvious choice for the high input voltage used in this system [3]. The main components used in a series regulator consist of a reference voltage generator and an operational amplifier [4]. Figure 2.1 illustrates the implementation of a reference voltage generator and an operational amplifier to form a series voltage regulator. Resistors R_1 and R_2 are used to set the output voltage in relation to the reference voltage. The output voltage (V_{OUT}) is related to the reference voltage (V_{REF}) through the non-inverting, ideal op-amp equation (Equation 2.1) [4].

$$V_{OUT} = V_{REF} \cdot \frac{R_1 + R_2}{R_2} \quad \text{(Equation 2.1)}$$

In general, the reference voltage in series voltage regulators can be generated from several circuits including bandgap voltage references and Zener voltage references [4]. To allow V_{OUT} to provide a stable, reliable output voltage, the op-amp used in the series voltage regulator must possess the typical qualities of a well-designed op-amp. Low op-amp drift and offset voltage are essential qualities for an op-amp to accurately regulate V_{OUT} according to Equation 2.1 [5]. The negative feedback loop (with attentive op-amp design) imposes a high impedance node at the input of the op-amp. Large op-amp input impedance is essential in minimizing loading effects presented on the reference generator.

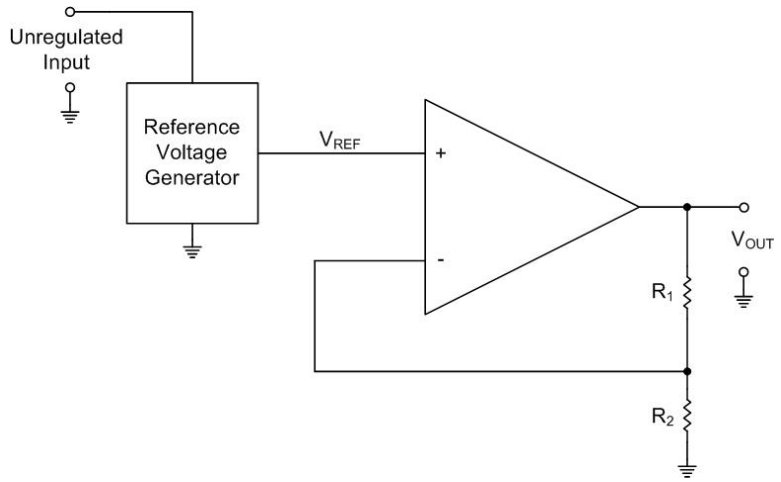

Figure 2.1 – Series Voltage Regulator

Similarly, the output of the op-amp must present a low impedance node. As with any op-amp, lowering output impedance increases op-amp current drive capability. Current drive capability is essential in any voltage regulator design due to the use of these circuits as voltage sources for variable load currents [4]. Equations 2.2 and 2.3 illustrate op-amp input impedance and output impedance, respectively.

$$R_{in} = r_i \cdot (1 + T_0) \quad \text{(Equation 2.2)}$$

$$R_{out} = \frac{r_o}{(1+T_0)} \quad \text{(Equation 2.3)} \qquad \text{where} \quad T_0 = A_{OL} \cdot \frac{R_2}{R_1+R_2}$$

In Equations 2.2 and 2.3, A_{OL} is the mid-band, open-loop gain of the op-amp, and T_0 is the mid-band loop transmission. Similarly, r_i and r_o are the mid-band, open-loop input and output resistances, respectively. As with most op-amp circuits, a large loop transmission allows negative feedback to drastically improve the performance of the op-amp. Exploring the relationship between V_{OUT} and R_{OUT} reveals that R_{OUT} is a function V_{OUT} as shown in Equation 2.4 (assuming A_{OL}, V_{REF}, and r_o are constant) [4].

$$R_{OUT} = \frac{r_o}{A_{OL} V_{REF}} \cdot V_{OUT} \quad \text{(Equation 2.4)}$$

Change in output current can be related to change in output voltage by Equation 2.5 [4].

$$\Delta V_{OUT} = R_{OUT} \cdot \Delta I_{OUT} \quad \text{(Equation 2.5)}$$

Combining Equation 2.4 and Equation 2.5, illustrates the relationship between output voltage and output current (Equation 2.6).

$$\frac{\Delta V_{OUT}}{V_{OUT}} = \frac{r_o}{A_{OL}\, V_{REF}} \cdot \Delta I_{OUT} \quad \text{(Equation 2.6)}$$

Equation 2.6 allows for load regulation calculations of a series regulator. A large open-loop gain improves load regulation and is essential in developing a voltage regulator capable providing an accurate voltage source under variable loads. Line regulation for a given series regulator is dependent on the reference generator circuit and will be examined in following sections [4].

2.2 – LM723 Voltage Regulator Topology

See reference [4] regarding section 2.2 discussion. The LM723 is a linear, series voltage regulator, which utilizes Zener diodes for reference voltage generation. This design utilizes BJT transistors throughout the topology. To better understand the LM723 design, each circuit section is examined at the transistor level.

2.2.1 – LM723 Reference Generator Circuit

The circuit used to generate the reference voltage in the LM723 regulator design is shown in Figure 2.2. The current sink I_1 is generated using a base-emitter referenced current source. The Zener diode D_1 induces a relatively constant Zener breakdown voltage across R_1, Q_1, and R_2 of approximately 6.2 V. The bias current through Q_1 is set by sizing resistors R_1 and R_2 according to Equation 2.7.

$$I_{C1} = -\frac{6.2 - V_{EB1}}{R_1 + R_2} \quad \text{(Equation 2.7)}$$

Therefore, the magnitude of I_{C1} is approximately equal to 5.6 V divided by the total resistance in series with Q_1. The main advantage of this current biasing scheme is the independence of the generated bias current to input voltage. Current I_{C2} is mirrored from Q_1 according to Equation 2.8 (assuming V_{EB} matching between devices).

$$I_{C2} = I_{C1}\frac{R_2}{R_3} \quad \text{(Equation 2.8)}$$

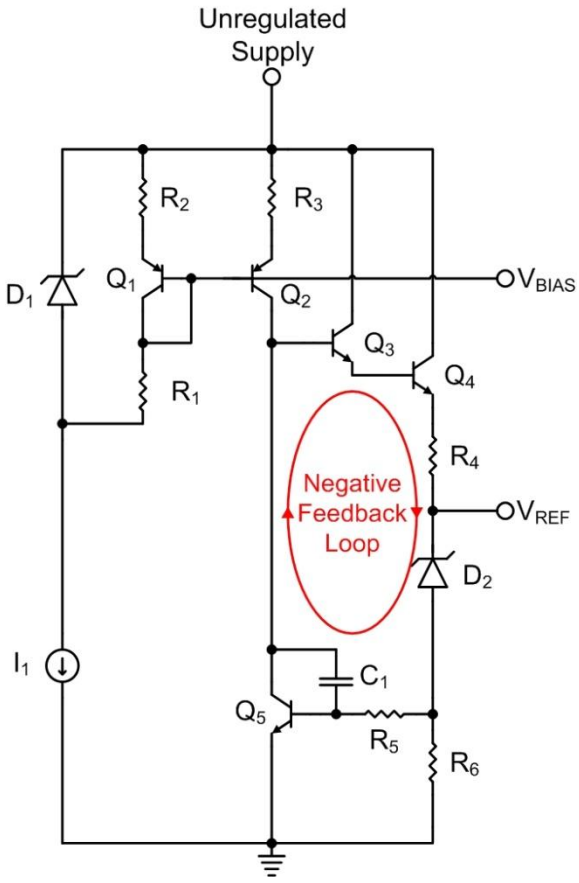

Figure 2.2 – LM723 Reference Voltage Generator Circuit

The current I_{C2} establishes the operating current for the voltage reference circuit composed of Q_3-Q_5. I_{C5} is forced to match I_{C2} through the negative feedback loop. The current through D_2 is set by resistor R_6 according to Equation 2.9 (assuming negligible base currents).

$$I_{D2} = \frac{V_{BE5}}{R_6} \quad \text{(Equation 2.9)}$$

The reference voltage, V_{REF}, is then equal to the sum of the Zener breakdown voltage of D_2 and V_{BE5} (about 6.8 V). Q_3 and Q_4 form a Darlington pair to boost the loop gain, lowering the impedance at the reference voltage node. Reducing the impedance at the reference voltage node increases the drive capability of the reference generator circuit. Resistor R_4 acts as a current limiter to protect the reference generator circuit from short circuit damage. R_5 and C_1 form a high frequency compensation network to reduce the bandwidth around the loop, which prevents oscillations in the feedback loop. The negative feedback loop provides output tracking and

allows changes at the reference voltage node to be referred to the current through D_2; this feedback action corrects changes in reference voltage due to loading effects.

2.2.2 – LM723 Operational Amplifier Circuit

Following the voltage reference generator in the LM723 design, the operational amplifier sets and regulates the output voltage as a function of the reference voltage. Figure 2.3 shows the operational amplifier used in the LM723 design. This op-amp is a simple, two-stage feedback amplifier. A differential input pair (Q_{11}, Q_{12}) provides the gain stage for the op-amp, while the Darlington pair, common-collector stage (Q_{13}, Q_{14}) provides the low output impedance stage. V_{BIAS} in Figure 2.3 is generated from the base voltage of the current reference transistor (Q_1) in the reference generator circuit. Resistors R_7 and R_8 set the ratios between the reference current through Q_1 and the biasing currents used in the op-amp circuit. Currents I_{C6}, I_{C7}, and I_{C8} match as long as $R_7 = R_8$ and the emitter areas of Q_6 and Q_7 are equal.

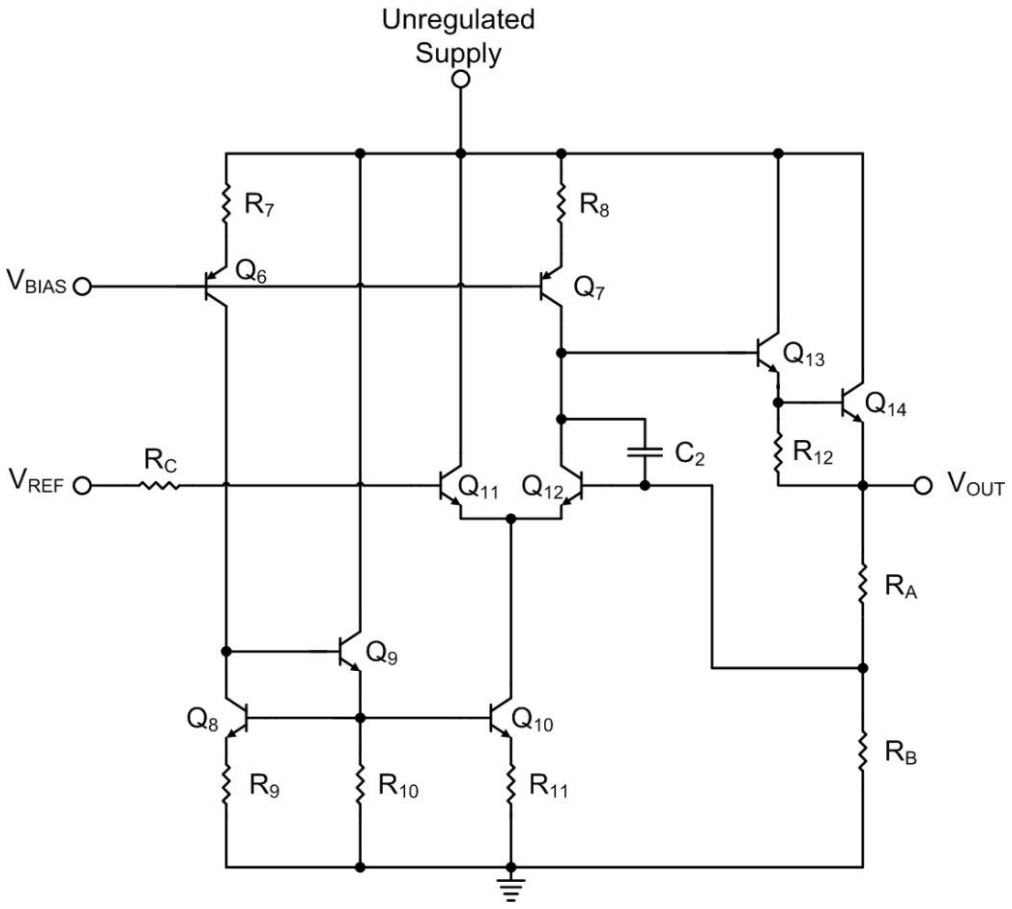

Figure 2.3 – LM723 Operational Amplifier Circuit

Q_{10} is set to have twice the emitter area of Q_8, and R_{11} is sized at half the value of R_9. This device sizing sets I_{C10} to be twice the magnitude of I_{C8}. Setting the bias currents to these values allows I_{C11} to equal I_{C12}. Q_9 provides current gain to minimize current mismatch due to base currents. This technique allows for better current matching and therefore, reduces offset error at the op-amp output. The load placed at V_{OUT} determines the current flowing through the Darlington pair Q_{14} and Q_{13}. R_{12} provides a constant current path through Q_{13}, so the output voltage will always be regulated. Capacitor C_2 provides dominant pole compensation for the op-amp in the form of Miller capacitance. The induced pole reduces the bandwidth and improves stability. The AC equivalent circuit for the op-amp in Figure 2.3 is shown in Figure 2.4. R_{LEQ12} is calculated from Equation 2.10 and represents the load seen by Q_{12}.

$$R_{LEQ12} = r_{o7} \cdot (1 + g_{m7} R_8) \quad \text{(Equation 2.10)}$$

The output impedance of the gain transistor, Q_{12}, is calculated assuming $g_{m11} = g_{m12}$ through matching.

$$R_{o12} = (1 + g_{m12} \frac{1}{g_{m11}}) \cdot r_{o12} \qquad \text{(Equation 2.11)}$$

Using Equations 2.10 and 2.11, the open-loop gain is derived as demonstrated in Equation 2.12.

$$A_{OL} = \frac{|v_o|}{|v_i|} = \frac{|v_1|}{|v_i|} = \frac{g_{m12}}{2} \cdot (R_{o12} || R_{LEQ12}) \qquad \text{(Equation 2.12)}$$

The output resistance for the op-amp is determined by the impedance looking into the emitter of the Darlington pair.

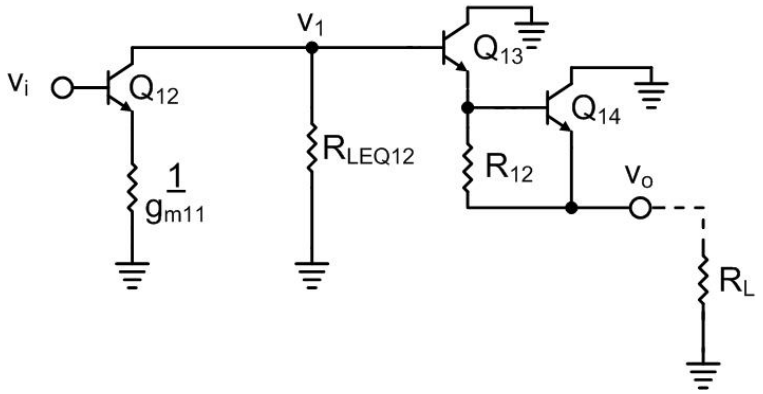

Figure 2.4 – LM723 Operational Amplifier Circuit – AC Equivalent

Equation 2.13 shows the calculation of this impedance (assuming $R_{12} >> r_{\pi 14}$).

$$r_o = \frac{1}{g_{m14}} + \frac{1}{\beta_{o14}} \cdot \left(\frac{1}{g_{m13}} + \frac{R_{o12} || R_{LEQ12}}{\beta_{o13}} \right) \quad \text{(Equation 2.13)}$$

Using Equations 2.12 and 2.13 in Equation 2.6 reveals the load regulation of the LM723 topology voltage regulator. Typical values for load regulation are on the order of 0.01-0.04 %; in other words, a 50-mA change in load current for a nominal 5-V output voltage results in an output voltage change of only 1-4 mV. The low output impedance of the op-amp allows the LM723 to exhibit this impressive resistance to loading conditions. The Miller compensation capacitor C_2 sets the dominant pole and allows a 2-pole loop transmission approximation to be used (Equation 2.14).

$$T(s) = T_0 \left(\frac{1}{1 + \frac{s}{T_{mid} \cdot R_{LEQ12} || R_{o12} . C_2}} \cdot \frac{1}{1 + \frac{s}{R_{in12} || R_A || R_B (C_2 + C_{be12} + C_{bc12})}} \right) \quad \text{(Equation 2.14)}$$

The single high-gain stage allows for pole splitting which ensures stability. The higher order poles and zeros are neglected, as they occur at frequencies much high than the unity gain frequency (f_{un}) of the op-amp.

2.3 – LM723 Design Review

The LM723 is a well designed, reliable voltage regulator that has been in industrial use for many years [6]. Several LM723 design features must be considered to ensure the designed voltage regulator meets the demand of the gate driver circuits. First, the LM723 is designed to withstand temperatures up to 125 ºC [6]. While its performance will most likely not degrade for temperatures marginally exceeding the rated operating temperature, the use of the gate driver voltage regulator in environments approaching 200 ºC imposes significant strain on the classic LM723 design. In addition to the temperature requirements, the gate driver voltage regulator is subject to input voltage ($V_{DDH} - V_{SSH}$) changes ranging from 10-30 V [2]. While the LM723 performs well under varying input voltage, the input conditions the gate driver project presents would result in an output voltage variation of 50-80 mV [6]. While this output voltage change may be acceptable for some applications, the design can be improved to perform more consistently over input voltage changes. Perhaps the most significant challenge to the LM723 design in the gate driver application is the transient load current imposed by the switching

circuits it is required to power. Essentially, the gate driver circuit impose large, switched-capacitor loads [2]. A slow voltage regulator response to a sudden load current demand results in a large deviation in regulator output voltage. Deviations in regulator output voltage can cause instability and gate driver error [2]. The transient current response of the classic LM723 design is not sufficient to supply the gate driver during a transient load [6]. Additionally, the required operating temperature of the gate driver project leads to an increased concern of on-chip heat generation. Also, the low β and g_m values (especially for the PNP devices) in the commercially-available, 0.8-micron process significantly reduce the attainable DC loop gain [5]. In summary, the LM723 provides a strong example for the design of the gate driver voltage regulator, but several significant design modifications are needed to ensure successful on-chip implementation.

3. Voltage Regulator Design and Simulation

3.1 – Voltage Regulator Design

The voltage regulator designed for the gate driver project consists of four stages: pre-regulator circuit, reference generator circuit, operational amplifier circuit, and output stage. The pre-regulator is supplied by V_{DDH} (10.0 V to 30.0 V) and outputs the pre-regulator voltage, V_{PRE}. The reference generator closely resembles the topology seen in Chapter 2, but several design alterations are implemented to improve regulator performance for the gate driver application. The generated reference voltage (V_{REF}) is the most critical voltage for establishing a constant regulator output voltage (V_{DD}). The operational amplifier is based on the design described Chapter 2 but with several significant design modifications to the LM723 design. The output of the operational amplifier is designated as $V_{DD'}$. The feedback signal from the voltage regulator output is input to the differential pair in the operational amplifier. The output stage of the voltage regulator is technically part of the operational amplifier, but the drastic changes from the topology seen in Chapter 2 warrant special consideration for this stage. The output stage receives the $V_{DD'}$ signal from the operational amplifier. The output of this stage (and output of the overall voltage regulator) is designated as the output voltage, V_{DD}. The block diagram in Figure 3.1 illustrates the 4-stage voltage regulator topology as a fully-functional unit with important signals labeled..

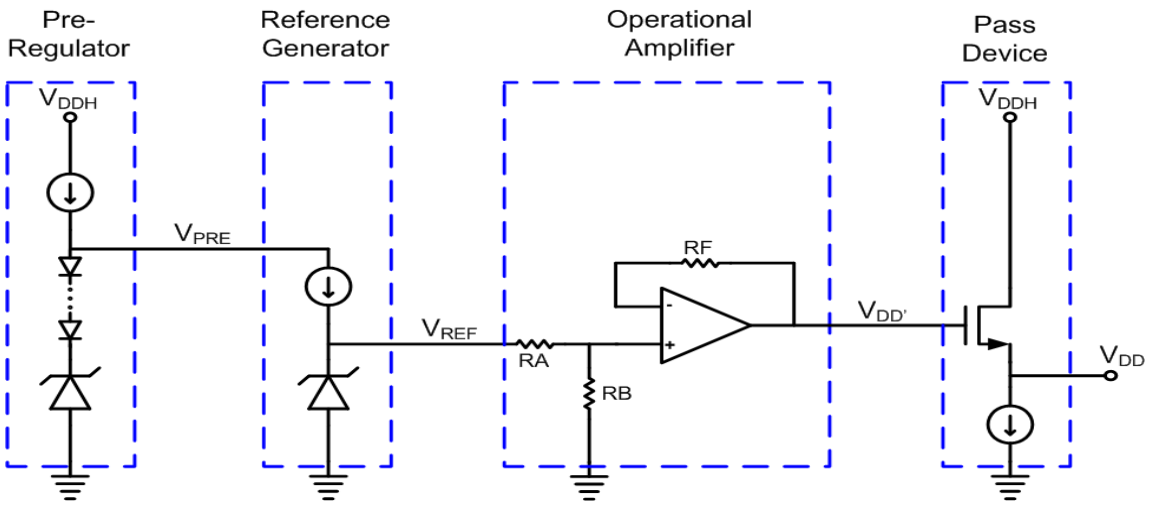

Figure 3.1 – 4-Stage Voltage Regulator Topology

3.1.1 – Pre-Regulator

The V_{DDH} input voltage supplied to the gate driver chip varies from 10 - 30 V; however, the commercially-available, 0.8-micron process offers BJT devices with an open-base, collector-emitter breakdown voltage of 15 V. To implement the BJT based LM723 design, a pre-regulator circuit is implemented to limit the voltage supplied to the remaining regulator stages. A Zener shunt regulator is used as a crude voltage regulator to generate V_{PRE}. Using this concept, the design of a pre-regulator is realized as seen in Figure 3.2. A threshold referenced current source (*M1-M6*, *R1*) generates the bias current for the pre-regulator circuit. This current is set by the threshold of *M1* and the resistor *R1* as illustrated in Equation 3.1 [4].

$$I_{D2} = I_{D1} = \frac{V_{TH1}}{R_1} \quad \text{(Equation 3.1)}$$

This reference current, I_{D2}, is mirrored through the cascode current mirror, *M3-M6*, creating I_{D1}. $M1_{SU}$-$M9_{SU}$ provide start-up for the current source to prevent the stable zero-current state [7]. *M7-M10* mirror I_{D2} so that $I_{D11} = I_{D12} = I_{D1}$. *M13*, *M14* are set to 10x the width of *M11*, *M12*, so that I_{D13}, I_{D14} are 10x the generated bias current. *M11-M14* are arranged in a wide-swing cascode configuration to allow V_{PRE} to swing very close to V_{DDH} [7]. In the wide-swing cascode configuration, *M12* is set to 5x the length of *M11* [7]. Equations 3.2a and 3.2b illustrate the required voltage difference between V_{DDH} and V_{PRE} for *M13* and *M14* to remain "on" [7].

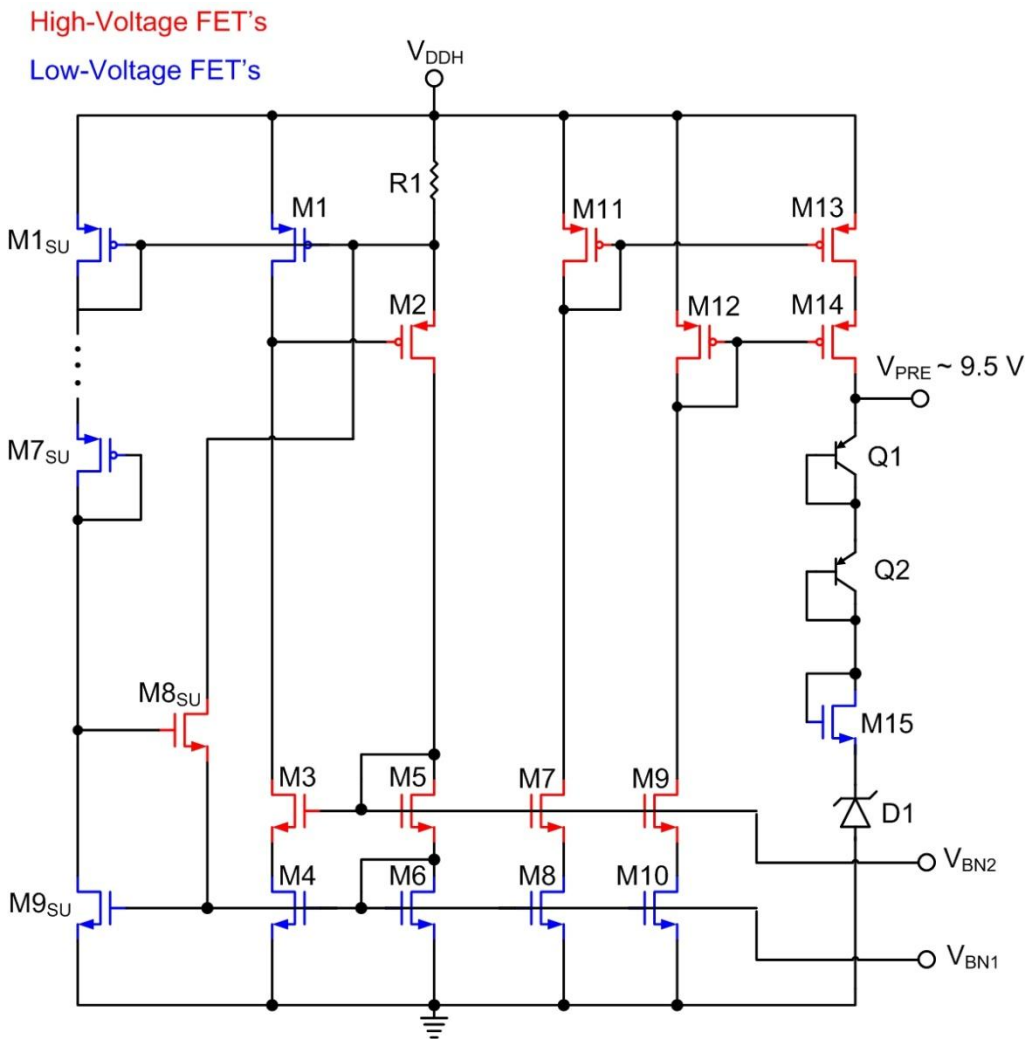

Figure 3.2 – Pre-Regulator Circuit

$$V_{DDH} - V_{PRE} \geq 2 \cdot V_{SD,sat\ 13,14} + |V_{TH13}| \quad \text{(Equation 3.2a, typical cascode)}$$

$$V_{DDH} - V_{PRE} \geq 2 \cdot V_{SD,sat\ 13,14} \quad \text{(Equation 3.2b, wide-swing cascode)}$$

When compared to a wide-swing cascode, a typical cascode configuration requires an additional threshold voltage to remain turned "on". The additional voltage swing generated by the use of the wide-swing cascode is required for low V_{DDH} voltages because the regulator circuits require a supply voltage of at least 8.5 V (set to 9.5 V to account for model inaccuracy, process variation, and mismatch). The current source (*M13*, *M14*) shunts current into the Zener diode, NMOS and PNP series configuration (*Q1*, *Q2*, *M15*, *D1*). The breakdown voltage of *D1* in the

commercially-available, 0.8-micron process is about 6.2 V. *Q1*, *Q2*, and *M15* add two V_{EB}, one V_{THN}, and one $V_{DS,SAT}$ to the generated pre-regulated voltage as shown in Equation 3.3.

$$V_{PRE} = V_{D1,BD} + V_{THN15} + V_{DS,SAT15} + V_{EB1} + V_{EB2} \quad \text{(Equation 3.3)}$$

The series configuration of *Q1*, *Q2*, *M15*, and *D1* provides the temperature-compensated voltage V_{PRE}. The high V_{DDH} voltage (up to 30 V) requires high-breakdown voltage devices to be used for the cascode devices. The remaining devices, however, do not have a large, induced drain-source voltage and are implemented using standard devices which provide better matching. Table 3.1 summarizes the devices used in the pre-regulator design.

Table 3.1 – Pre-Regulator Device Specifications

Device	Device Type	Device Property
M1	Low-Voltage PMOS	$\frac{80.0\ \mu}{1.6\ \mu}$
M2, M11	45-V P-Channel LDMOS	$\frac{20.0\ \mu}{3.2\ \mu}$
M12	45-V P-Channel LDMOS	$\frac{20.0\ \mu}{16.0\ \mu}$
M13, M14	45-V P-Channel LDMOS	$\frac{200.0\ \mu}{3.2\ \mu}$
M3, M5, M7, M9	45-V N-Channel LDMOS	$\frac{20.0\ \mu}{3.2\ \mu}$
M4, M6, M8, M10	Low-Voltage NMOS	$\frac{12.8\ \mu}{1.6\ \mu}$
M15	Low-Voltage NMOS	$\frac{80.0\ \mu}{4.0\ \mu}$
$M1_{SU}$-$M7_{SU}$	Low-Voltage PMOS	$\frac{1.6\ \mu}{16.0\ \mu}$
$M8_{SU}$	45-V N-Channel LDMOS	$\frac{20.0\ \mu}{3.2\ \mu}$
$M9_{SU}$	Low-Voltage NMOS	$\frac{12.8\ \mu}{1.6\ \mu}$
R1	Poly2	50 kΩ
D1	Zener	6.2 V

Using the devices in Table 3.1 and the device properties from the commercially-available, 0.8-micron process documentation, the nominal bias currents are set as follows: $I_{D4} = I_{D6} = I_{D8} = I_{D10} = I_{D9SU} = 20$ µA, $I_{D13} = 200$ µA. I_{D13} is mainly sourced to supply the remaining voltage regulator stages; however, 20-40 µA of current remains to bias *D1*, *Q1*, *Q2*, and *M15*. V_{PRE} is established at 9.5 V, but varies slightly with changes in current draw from the remaining stages, temperature, and process variations.

3.1.2 – Reference Generator

The reference generator circuit (Figure 3.3) used in the voltage regulator design is powered from the pre-regulator circuit described in Section 3.1.1. In the reference generator circuit, current bias is generated by the base-emitter referenced current source composed of *Q3*-*Q6* and *R2* while $Q1_{SU}$-$Q5_{SU}$ and *M16*-*M17* provide start-up [4]. *Q7* sinks the bias current through the parallel combination of *D2* and *Q8*.

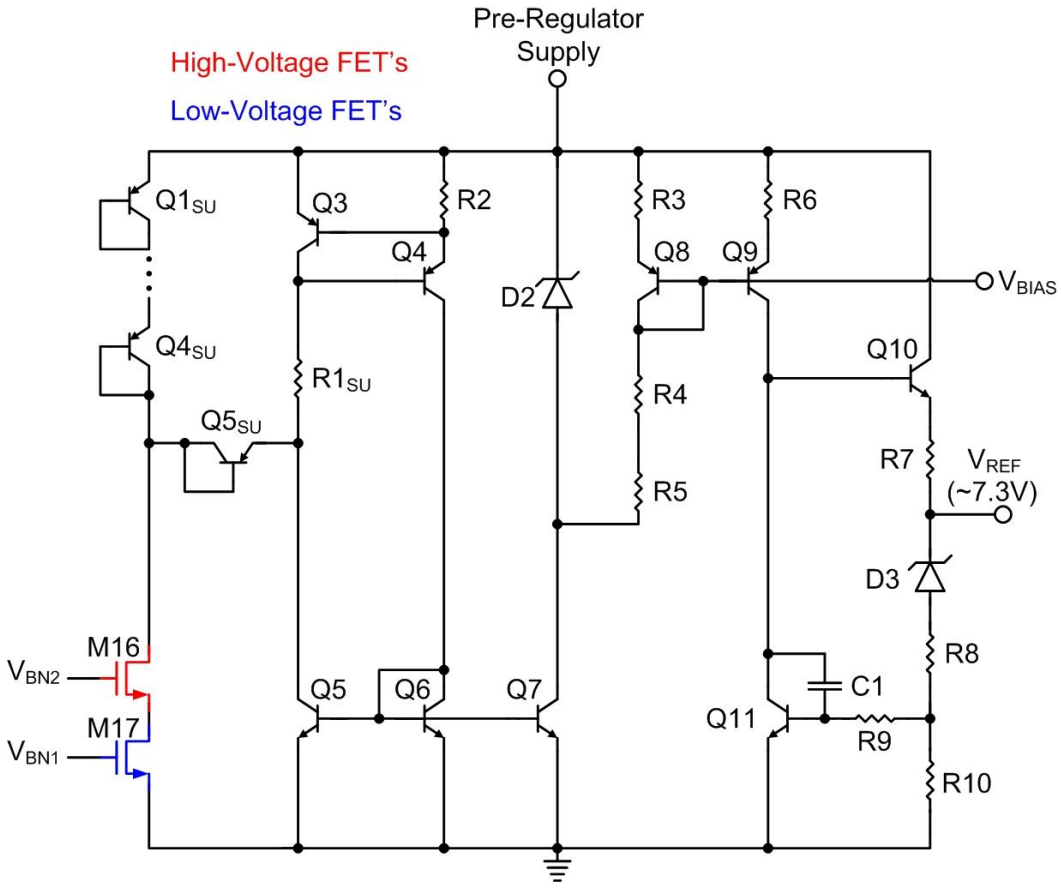

Figure 3.3 – Reference Generator Circuit

D2 establishes a reference voltage drop across *R3-R5* and *Q8*, resulting in a bias current in *Q8* governed by Equation 3.4 [4].

$$I_{C8} = \frac{V_{D2,BD}}{R3+R4+R5} \quad \text{(Equation 3.4)}$$

R3 and *R4* possess complementary temperature coefficients and are used compensate the temperature dependence of V_{EB8}. The bias current through Q_8 is mirrored throughout the reference generator and op-amp circuits. As seen in the LM723 discussion, Q_{10} provides current bias through *D3*. *D3* in series with *R8* and *R10* establish the temperature-compensated reference voltage V_{REF}. *R8* is sized to provide additional compensation to the inherent temperature compensation of *D3*. The Darlington pair in the LM723 reference generator is removed because a V_{DDH} of 10 V does not allow enough headroom between the reference voltage to the pre-regulator voltage. Loading effects on the output of the reference generator are carefully considered due to the removal of the Darlington pair common collector stage [8]. Table 3.2 summarizes the devices used in the reference generator circuit. These device sizes imply a bias current through *Q3-Q6* of about 10 µA based on Equation 3.5 and the technology parameters given in the commercially-available, 0.8-micron process documentation.

$$I_{C3} = \frac{V_{EB3}}{R2} \quad \text{(Equation 3.5)}$$

The bias current through *Q7* is set 2x the current through *Q5-Q6* by doubling the emitter area of *Q7*. The current through *Q8* is established at about 10 µA. *R10* establishes a bias current through *D3* of approximately 10 µA (Equation 3.6).

$$I_{D3} = \frac{V_{BE11}}{R10} \quad \text{(Equation 3.6)}$$

The temperature-dependent reference voltage is described by Equation 3.7.

$$V_{REF}(T) = V_{D3,BD}(T) + V_{BE11}(T) + R8(T) \cdot I_{D3}(T) \quad \text{(Equation 3.7)}$$

Substituting Equation 3.6 into Equation 3.7 yields Equation 3.8. The first-order temperature coefficients are estimated by taking the first derivative of Equation 3.8.

Table 3.2 – Reference Generator Device Specifications

Device	Device Type	Device Property
M16	45-V N-Channel LDMOS	$\frac{20\ \mu}{3.2\ \mu}$
M17	Low-Voltage NMOS	$\frac{3.2\ \mu}{1.6\ \mu}$
$Q1_{SU}$-$Q5_{SU}$	Lateral PNP	1x (unit transistor)
Q3-Q4, Q8-Q9	Lateral PNP	4x
Q5-Q6, Q11	Lateral NPN	4x
Q7, Q10	Lateral NPN	8x
D2, D3	Zener	8x
$R1_{SU}$	Poly2	110 kΩ
R2	Poly2	68 kΩ
R3, R6	Poly2	2 kΩ
R4	Poly2	380 kΩ
R5	PWell	170 kΩ
R7	N+	160 Ω
R8	Poly2	18 kΩ
R9	Poly2	32 kΩ
R10	Poly2	42 kΩ
C1	MOSCAP	4 pF

$$V_{REF}(T) = V_{D3,BD}(T) + V_{BE11}(T) + V_{BE11}(T) \cdot \frac{R8(T)}{R10(T)} \quad \text{(Equation 3.8)}$$

Equation 3.9 defines the first-order temperature coefficient of the reference voltage as a function of device temperature coefficients.

$$\frac{\partial}{\partial T}V_{REF}(T) = \frac{\partial}{\partial T}V_{D3,BD}(T) + \frac{\partial}{\partial T}V_{BE11}(T) + \frac{\partial}{\partial T}V_{BE11}(T) \cdot \frac{R8_o}{R10_o} \quad \text{(Equation 3.9)}$$

R8, *R10* temperature coefficients cancel yielding Equation 3.10, where the nominal resistor values ($R8_o$, $R10_o$) are chosen to minimize the reference voltage temperature coefficients.

$$\frac{R8_o}{R10_o} = \frac{-\left(\frac{\partial}{\partial T}V_{D3,BD}(T)+\frac{\partial}{\partial T}V_{BE11}(T)\right)}{\frac{\partial}{\partial T}V_{BE11}(T)} \qquad \text{(Equation 3.10)}$$

Equation 3.10 serves as a first order approximation; therefore, second order temperature effects are still present in the generated reference voltage [5]. Using the devices shown in Table 3.2 and device information provided with the commercially-available, 0.8-micron process PDK, a nominal reference voltage of ~7.3 V is established by the reference generator. Using Equation 3.10, the *R8*/*R10* ratio is set to 0.4 based on a $V_{D3,BD}$ temperature coefficient of 2.8 mV/ºC and a V_{BE} temperature coefficient of −2 mV/ºC [5].

3.1.3 – Operational Amplifier

In order to properly regulate the output voltage under a load condition, the reference voltage is fed to an error amplifier [4]. To combat the inherently low β values for the BJT devices (~ 50 for NPN, ~ 10 for PNP at room temperature) this amplifier is composed of three stages as opposed to the two used in the LM723 topology. This topology provides a high DC gain, which reduces offset error and improves regulation [8]. Because the op-amp for this regulator has narrow bandwidth requirements (due to use of an external output capacitor), the compensation scheme reduces the bandwidth quite low to accommodate phase margin concerns (the affects of this compensation scheme on transient response are addressed in later sections). Reducing the bandwidth of the feedback loop allows the three-stage amplifier to remain stable [8]. Figure 3.4 shows the implemented three-stage operational amplifier. The compensation node has moved from the differential pair (as in the LM723) to the common-emitter stage. Another modification to the operational amplifier is that the reference voltage is resistively divided before being fed to the operational amplifier input. The 7.3-V reference voltage used to generate V_{DD} must be resistively divided to approximately 5 V, which requires the operational amplifier to operate in unity gain. Figure 3.4 demonstrates this configuration with the feedback resistor R_F used to reduce mismatch offset related to the input bias currents. All bias currents in the op-amp are set to I_{C8} (of the reference generator) except for I_{C16} and I_{C22} which are double I_{C8}.

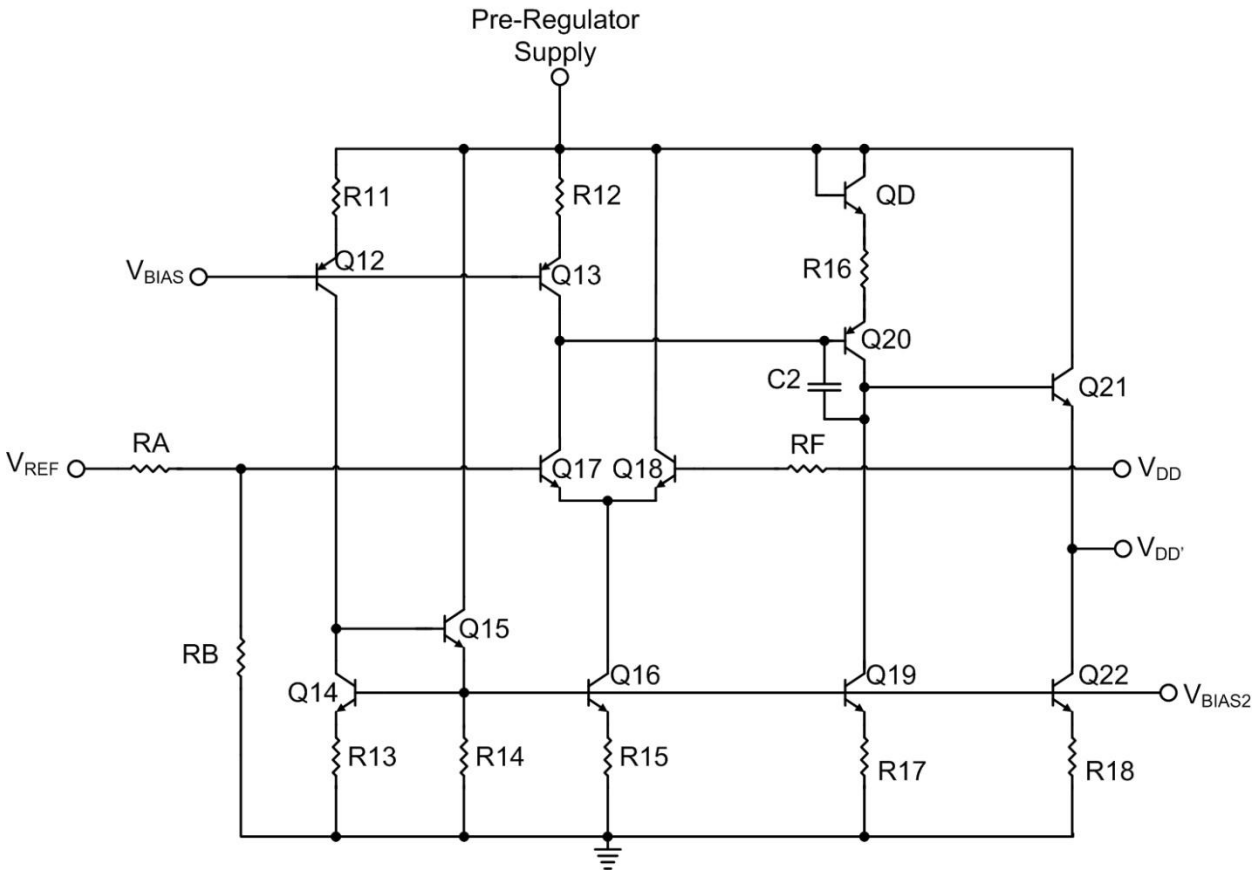

Figure 3.4 – Operational Amplifier Circuit

I_{C16} is doubled to provide current bias for *Q17* and *Q18*, while I_{C22} is doubled to increase the drive capability of the common collector stage. *QD* and *R16* are added to allow *Q13* to remain in forward-active mode by pulling the emitter voltage of *Q20* down from the pre-regulator voltage rail. The resistance seen in the emitter of *Q20* (*R16* and r_{eD}) is sized to allow *Q20* to remain the dominant gain stage. The DC loop transmission is found to be approximately 85 dB using Equation 3.11 (A_{diff} ~ 25 dB, A_{CE} ~ 60 dB using defined device values).

$$T_o = \frac{|v_o|}{|v_i|} = A_{diff} \cdot A_{CE} = \frac{g_{m17}}{2}\left(R_{o17} \middle|\middle| R_{LEQ17}\right) \cdot -g_{m20} \cdot \frac{R_{LEQ20}}{R16} \qquad \text{(Equation 3.11)}$$

The Miller capacitor *C2* provides loop stability by pole splitting [7]. The pole created at the common-emitter stage (*Q20*) is compensated to take advantage of the 60 dB gain at that stage. The expression for the loop transmission can be seen in Equation 3.12. Assuming *C2* dominates parasitic capacitances, τ_1 in Equation 3.12 is established by the gain of the common emitter stage, *C2*, and the equivalent load seen by *Q17*.

$$T(s) = T_o \left(\frac{1}{1+\frac{s}{\tau_1}}\right)\left(\frac{1}{1+\frac{s}{\tau_2}}\right) \quad \text{(Equation 3.12)}$$

Similarly, τ_2 is established by the capacitance at the base of *Q18* and the equivalent resistance at the base of *Q18*. Both poles in the two-pole approximation are subject to the Miller effect. The gain of the common-emitter amplifier is set to dominate the gain of the differential input pair, which allows pole-splitting to ensure stability.

$$\tau_1 = \left(R_{in,20} \left|\left| R_{out,17} \right|\right| R_{out,13}\right) \cdot C_2 \cdot A_{CE} \quad \text{(Equation 3.13a)}$$

$$\tau_2 = (R_{in,18}||(RF + (R_{out,21} + R_{out,22}))) \cdot C_{in,18} \cdot A_{diff} \quad \text{(Equation 3.13b)}$$

The resulting phase margin is over 70° which allows for stable operation. Table 3.3 lists the devices used in the operational amplifier circuit. This simple op-amp design provides stable voltage regulation over the full range of operating conditions.

Table 3.3 – Operational Amplifier Device Specifications

Device	Device Type	Device Property
Q12-Q13, Q20	Lateral PNP	4x
Q14-Q15,Q17-19, QD	Lateral NPN	4x
Q16, Q21-Q22	Lateral NPN	8x
R11-R13, R16-R17	Poly2	2 kΩ
R14	Poly2	58 kΩ
R15, R18	Poly2	1 kΩ
RA	Poly2	200 kΩ
RB	Poly2	440 kΩ
RF	Poly2	140 kΩ
C2	MOSCAP	100 pF

3.1.4 – Output Stage

In addition to the common-collector stage at the output of the op-amp, an output device capable of driving large currents and regulating large input/output voltage differentials is required at the last stage of the voltage regulator. To prevent load current from being drawn from the pre-regulator (increasing the no load supply current), this pass device draws its current directly from the input voltage (V_{DDH}). The insufficient open-base collector-emitter breakdown voltage of the BJT devices necessitates the use of a high-voltage NMOS device for the output device. The schematic for the output stage is depicted in Figure 3.5. *Q23* provides a small bias current to allow *M18* to regulate the output voltage under no load conditions. Using an NMOS transistor as the pass device allows the load current to be drawn from V_{DDH}, but the "on" resistance associated with this device degrades the load regulation this voltage regulator could potentially demonstrate [5]. Due to the high drain voltage imposed on *M18*, this device is always saturated; and therefore, the output voltage is a function of the load current [8]. To decrease this effect as much as possible, the width of *M18* is set quite large. Table 3.4 lists the devices used in the output stage of the voltage regulator design.

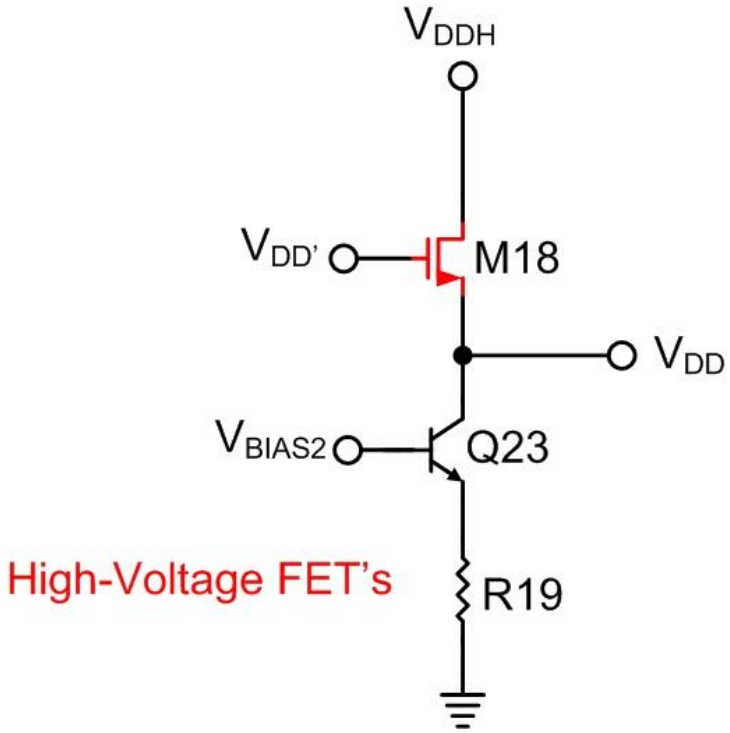

Figure 3.5 – Output Stage

Table 3.4 – Output Stage Device Specifications

Device	Device Type	Device Property
M18	45-V N-Channel LDMOS	$\frac{3000\ \mu}{3.2\ \mu}$
Q23	Lateral NPN	4x
R19	Poly2	2 kΩ

3.2 – Voltage Regulator Simulation

3.2.1 – Operational Amplifier

For the operation amplifier loop transmission simulation, $V_{DD'}$ is connected directly to V_{DD}, which allows the op-amp performance to be isolated. Loop transmission simulations for the operational amplifier closely match the predicted loop transmission as evident in Figure 3.6. The simulated DC loop gain of the op-amp is over 86 dB. The op-amp loop transmission is dominated by a two-pole response (f_1 ~ 10 Hz, f_2 ~ 500 kHz) with a gain-bandwidth product of about 200 kHz. Some higher order effects are visible but occur well past f_{un} and have minimal effect on the op-amp operation. Stable op-amp operation is ensured due to the ample phase and gain margins (*P.M.* ~ 72, *G.M.* ~ 10 dB). The operational amplifier provides stable operation, low offset, and accurate regulation due to the high gain and phase margin. The transient response of the operational amplifier is limited due to the low bandwidth of the design. The use of an external output capacitor reduces the bandwidth requirement of the voltage regulator by providing charge storage to respond to a load transient. The settling time of the regulated output voltage will be slow, but the total deviation from nominal V_{DD} will be minimal. The load transients presented by the gate driver have very narrow pulse widths, and therefore, the total charge required during a transient will be small. A relatively small output capacitor can supply the charge required during these events effectively reducing the load presented to the voltage regulator. Using this design, the operational amplifier is able to exhibit high DC gain while remaining stable for all operating conditions.

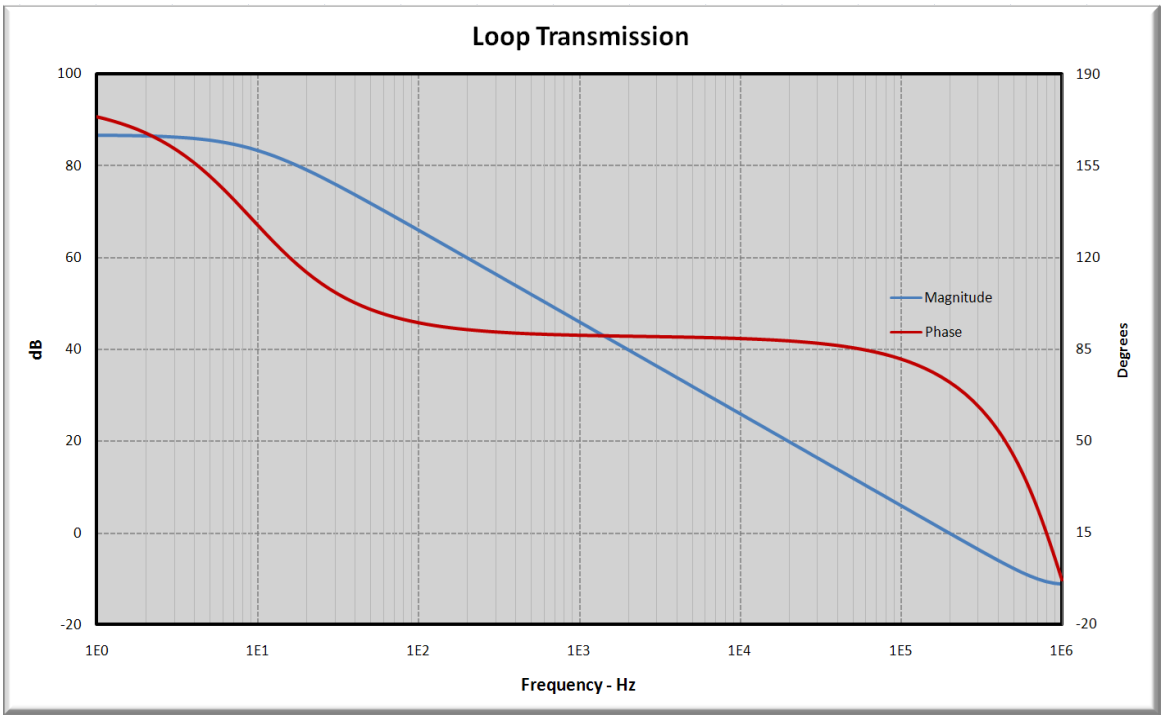

Figure 3.6 – Operational Amplifier Loop Transmission

3.2.2 – Input Voltage Start-Up

Voltage regulator start-up occurs when the Zener diode, *D3*, reaches its breakdown voltage, and the reference voltage is properly regulated. This start-up voltage is one of the fundamental limits of the LM723 topology. Historically, silicon Zener diodes with a breakdown voltage of about 5.6 V have been shown to offer minimized temperature coefficients (the voltaget at which the Zener effect and the avalanche effect cancel). In the commercially-available 0.8 micron process, a 6.3 V Zener diode is available. In order for the designed voltage regulator to start-up, Equation 3.14 must be satisfied (R7 is negligible).

$$V_{PRE} \geq V_{D3,BD} + 2V_{BE} + I_{D3} * (R7 + R8) \qquad \text{(Equation 3.14)}$$

The input voltage must be greater than the sum of the breakdown voltage of the Zener diode and all voltage drops in series with the Zener diode. Typically, the LM723 topology has a higher start-up voltage than other series linear regulator designs. The large start-up voltage of LM723-based voltage regulator designs is a significant design trade-off that must be considered. For the gate driver project, input voltages are always above 10 V allowing the use of the LM723 topology. Input start-up simulation shows a start-up voltage around 8.3 V (Figure 3.7).

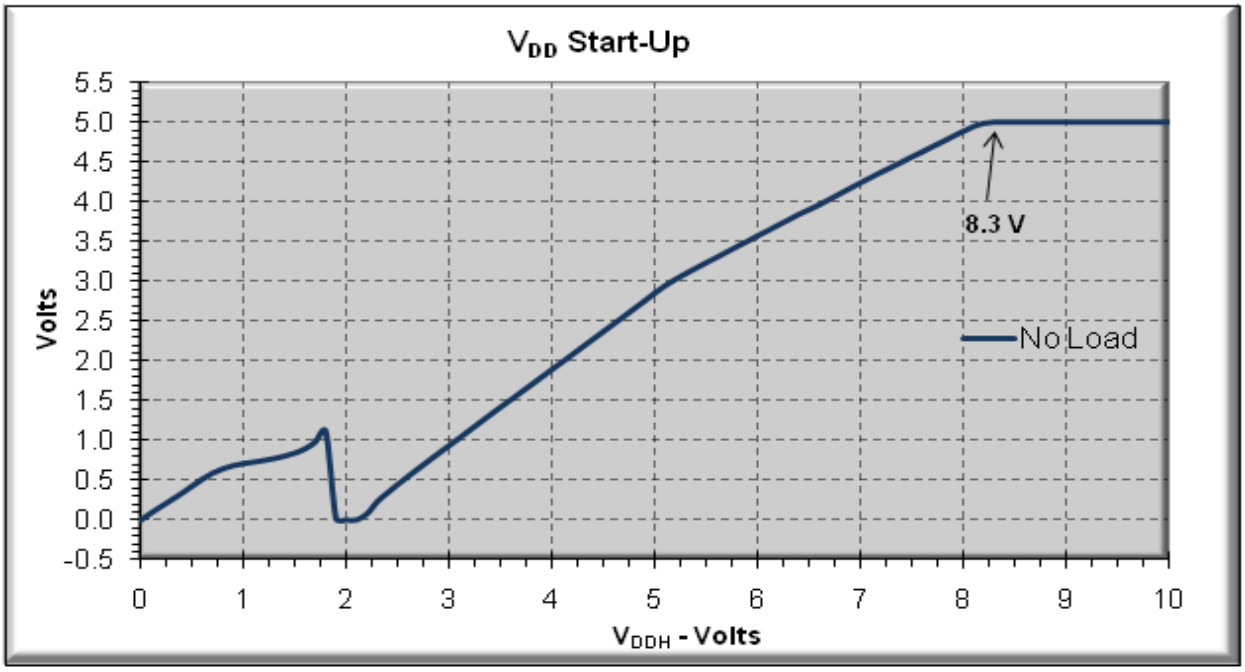

Figure 3.7 – Simulated Voltage Regulator Start-Up

3.2.3 – Line Regulation

Line regulation is a very important consideration for any voltage regulator design due to the variability of input voltages. Line regulation is simulated at room temperature for both the no load condition and a 10-mA load condition over a V_{DDH} range of 10 V – 35 V. Figures 3.8 - 3.11 illustrate line sweep simulation results for V_{DD}, V_{PRE}, V_{REF}, and I_{REG}, respectively. As Figure 3.8 demonstrates, the line regulation of V_{DD} is extremely small for either load condition; the inherent supply rejection of the LM723 topology and the use a pre-regulator circuit account for this simulated line regulation. This line regulation (on the order of ppb/V) far exceeds any foreseeable application demand. Adding a 10-mA load current to the output of the voltage regulator induces a slight increase in the input sensitivity of V_{DD} most likely arising from the "on" resistance of the pass device. Figure 3.9 shows the pre-regulator voltage in response to the input voltage sweep. The line regulation of V_{PRE} is not on the order of V_{DD} (an expected result), but the pre-regulator still regulates V_{DDH} on the order of ppm/V. Loading the voltage regulator exhibits virtually no change in the line regulation of V_{PRE}. The observed proportionality of V_{PRE} to V_{DDH} is related to channel length modulation of the MOSFET devices used in the pre-regulator circuit. Figure 3.10 examines the reference voltage as a function of input voltage. The reference

voltage (ideally independent of input voltage) is found to have a very small, proportional relationship to input voltage (ppb/V). This proportionality comes from the relationship of Zener breakdown voltage Zener diode current. Generating both the reference voltage and bias current with Zener diodes (as is done in this voltage regulator topology) reduces this effect. This, seemingly simple concept of the LM723 topology, allows for very predictable reference voltages to be generated over a wide range of input voltages. The line regulation of the output voltage, V_{DD}, is limited by the line regulation of V_{REF}, so design choices in the reference generator circuit are carefully considered in the overall voltage regulator design. Generating a reference voltage with a line regulation on the order of ppb/V is the main reason that the output voltage demonstrates extreme resistance to input variation. Load current variation reveals virtually no change in the line regulation of V_{REF} (due to the low output impedance of the op-amp). The regulator bias current generated from the Zener reference current source is indirectly related to input voltage (through V_{PRE}) due to the Early effect (Figure 3.11), but the coefficient of this relationship is on the order of pA/V and has little effect on regulator performance. Load current variation has no discernable effect on I_{REG} line sensitivity.

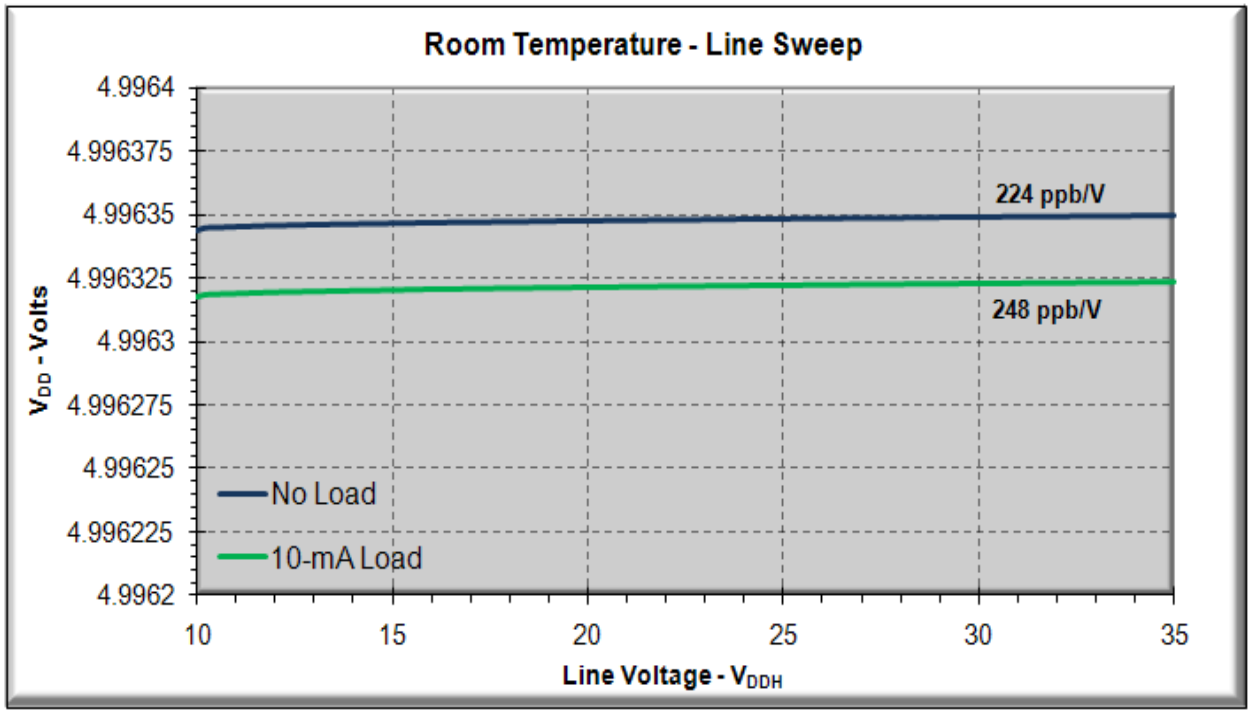

Figure 3.8 – Simulated V_{DD} Line Regulation

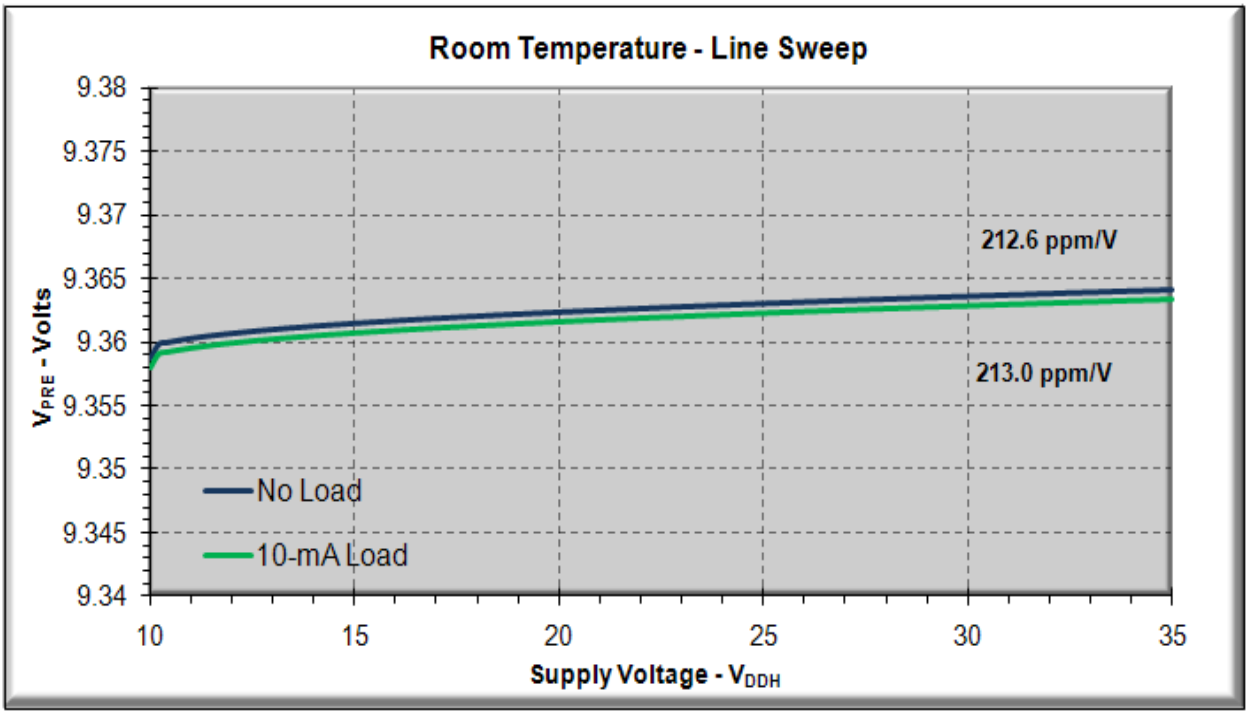

Figure 3.9 – Simulated V_{PRE} Line Regulation

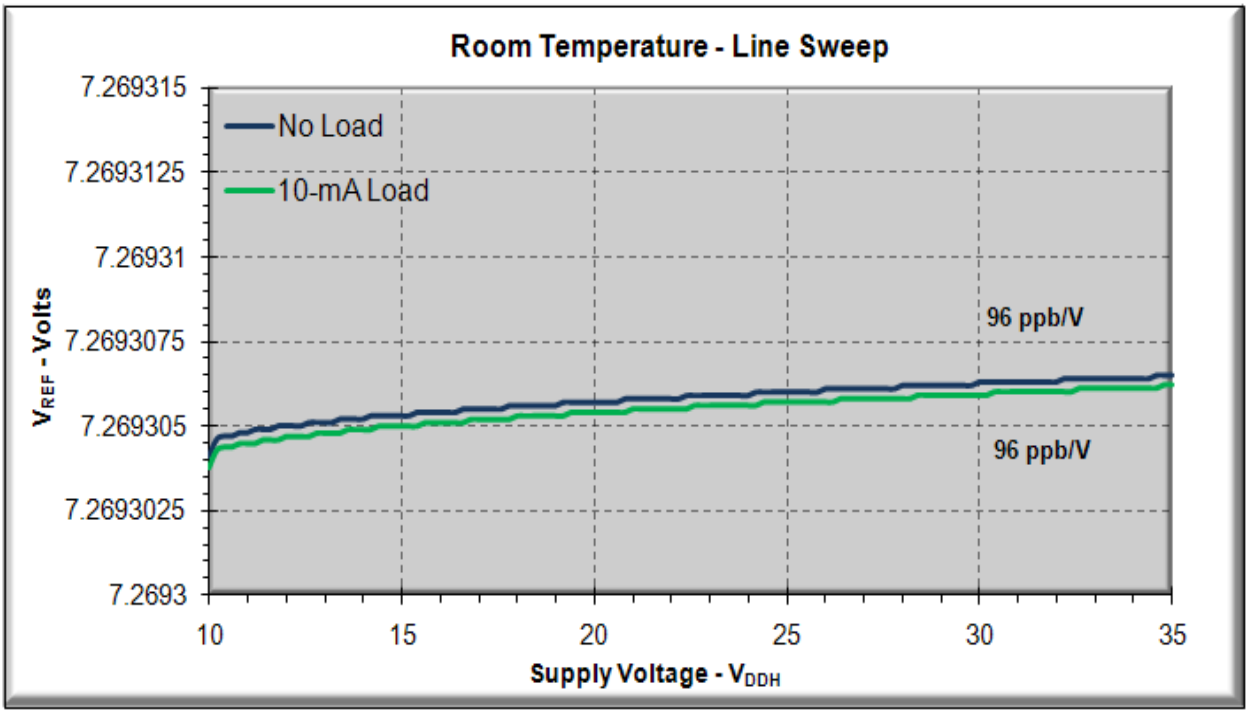

Figure 3.10 – Simulated V_{REF} Line Regulation

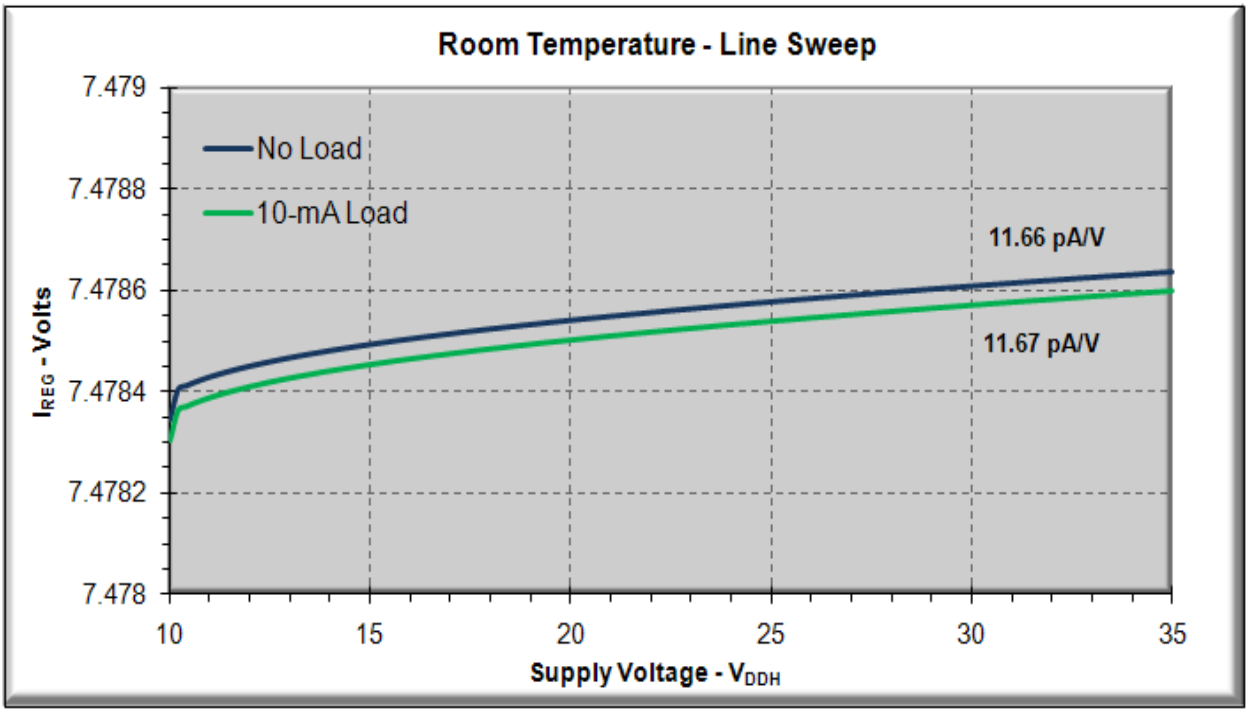

Figure 3.11 – Simulated I_{REG} Line Regulation

3.2.4 – Load Regulation

Load regulation is another critical parameter on which voltage regulators are evaluated. The ability to supply a wide range of load currents without a minimal change in output voltage allows the voltage regulator to be implemented in a myriad of applications. Some circuits (especially analog circuits) have very strict supply voltage constraints and demand the ability to draw current linearly with virtually no change in supply voltage. Digital circuits (such as the circuits in the gate driver application) are less sensitive to changes in supply voltage but impose very fast load transients on the voltage regulator. Analog and digital circuits present their own unique challenges when design voltage supplies for these circuits. This voltage regulator is designed to accommodate both types of electronic devices. DC load regulation simulations are performed at room temperature for input voltages of 10 V, 20 V, and 30 V. Figures 3.12 - 3.16 display load sweep simulation results for V_{DD}, V_{PRE}, V_{REF}, I_{PRE}, and I_{REG}, respectively. Over a load current range of 0 to 10 mA, V_{DD} is found to vary only a few µV/mA for all V_{DDH} voltages (Figure 3.12). The complementary dependence of V_{DD} on load current is due to the "on" resistance of the pass device, but this coefficient is quite small and allows for undisturbed performance over a wide

range of load currents. This load current vs. V_{DD} relationship is linear, and can be extrapolated for load currents exceeding 200 mA. For all input voltages, V_{PRE} has an inverse, linear proportionality to V_{DDH} (Figure 3.13). This relationship results from the increasing I_{D13} current required by the regulator circuits. The complementary relationship between V_{DDH} and V_{REF} (Figure 3.14) arises from the Early effect imposed on the regulator devices from the pre-regulator voltage load sensitivity. However, V_{REF} is nearly independent of load current through the use of an operational amplifier in the LM723 topology. The operational amplifier prevents loading effects from being referred to the reference voltage node. No measurable correlation between I_{PRE} and load current is discernable for any V_{DDH} voltage (Figure 3.15). This result is expected as I_{PRE} is generated using a threshold referenced current source. The Early effect on the BJT devices (as mentioned in reference to V_{REF} load regulation results) results in a complementary relationship between I_{REG} and load current (Figure 3.16). Overall, the voltage regulator shows excellent load regulation at each stage of the design. The load current can be increased up to 300 mA without risk of circuit damage.

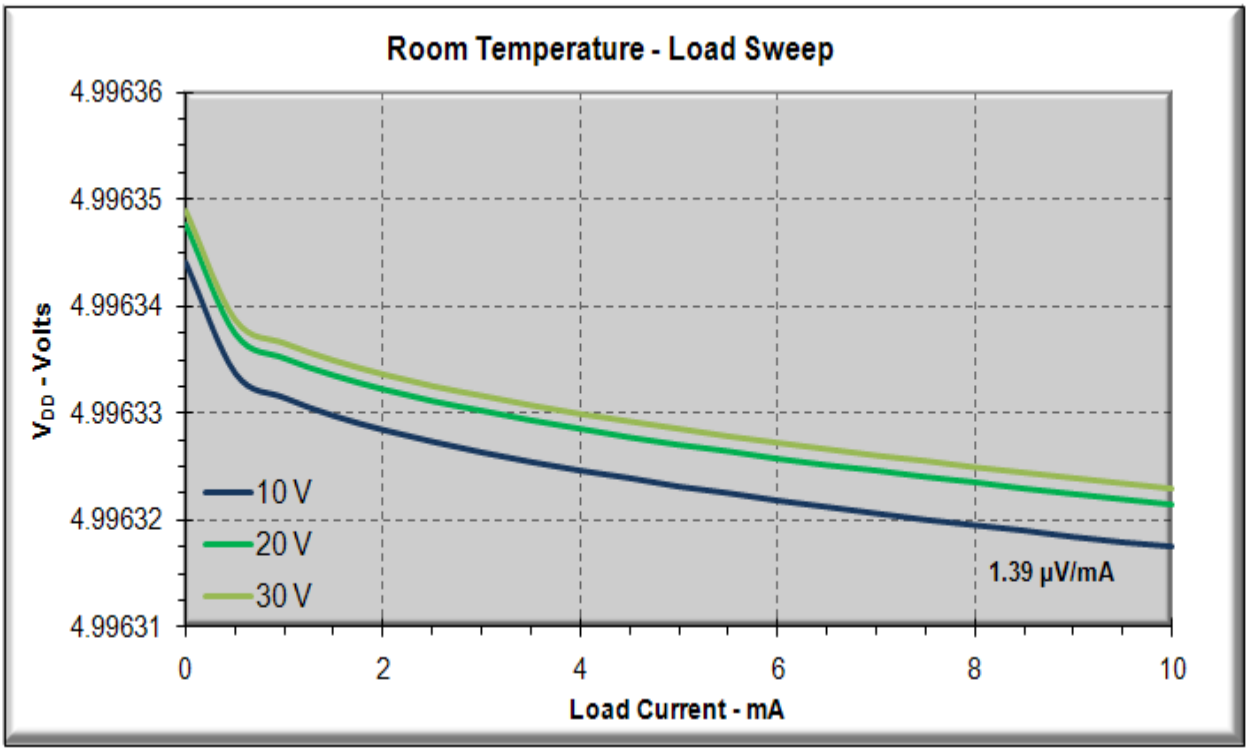

Figure 3.12 – Simulated V_{DD} Load Regulation

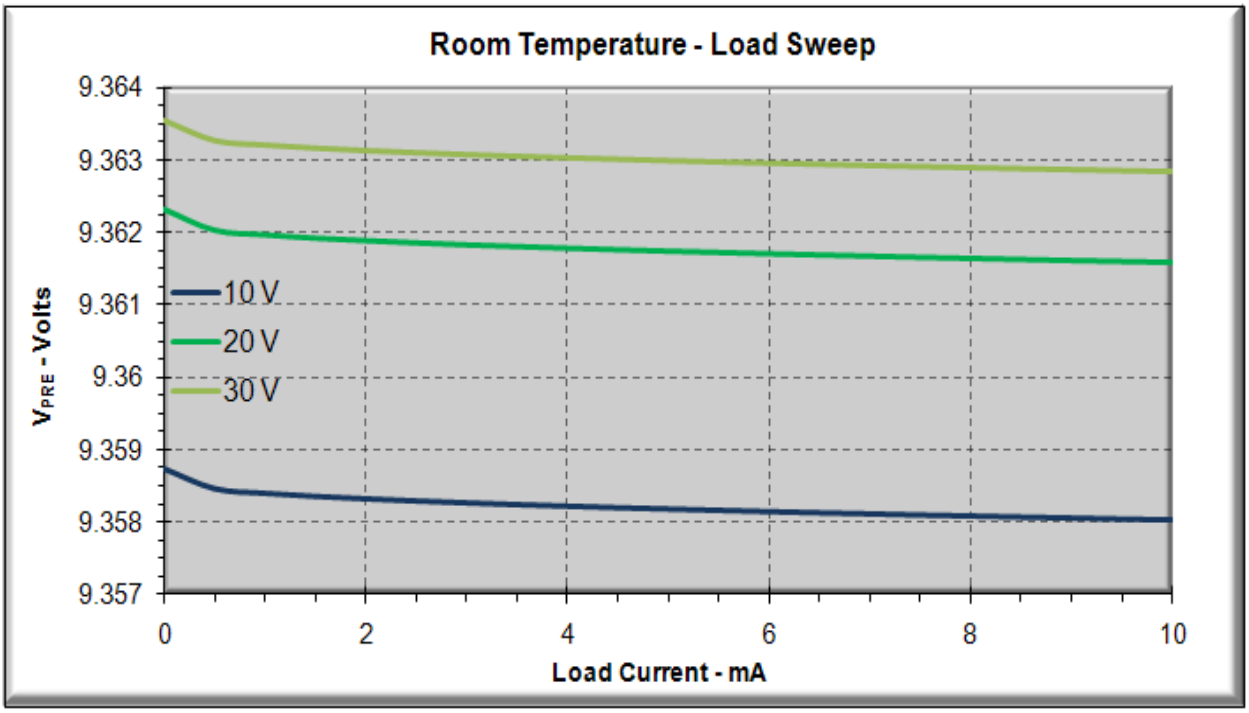

Figure 3.13 – Simulated V_{PRE} Load Regulation

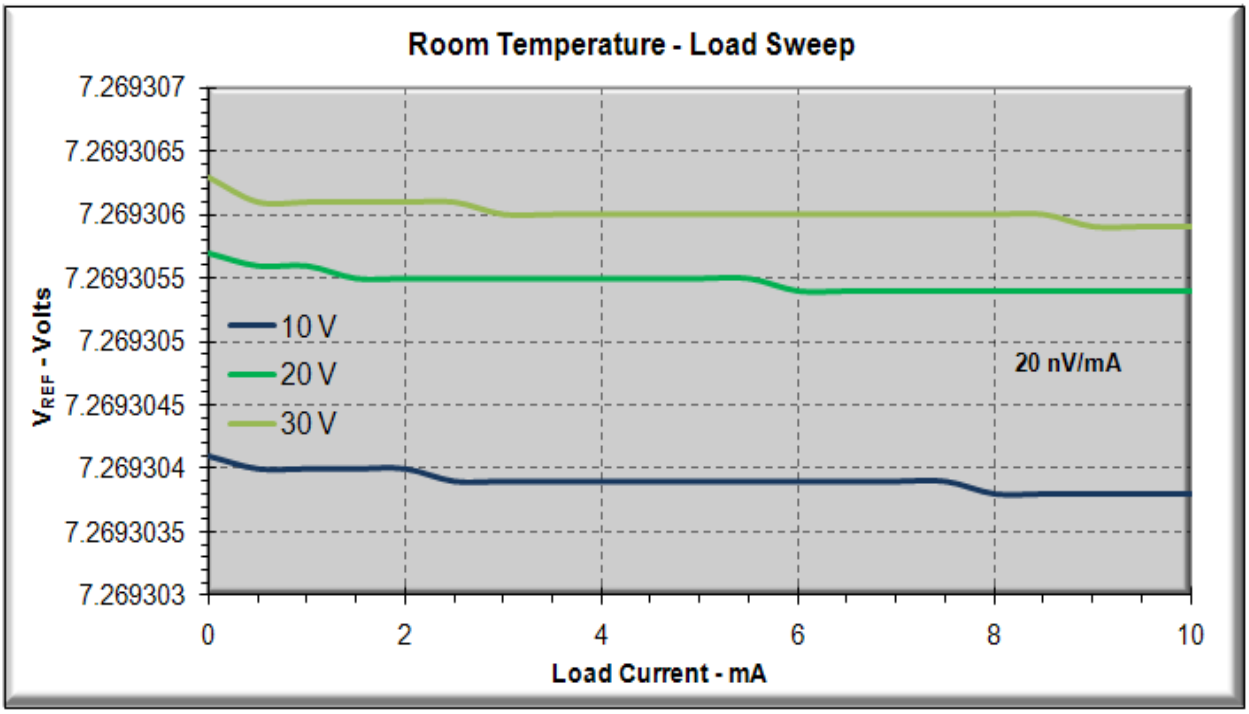

Figure 3.14 – Simulated V_{REF} Load Regulation

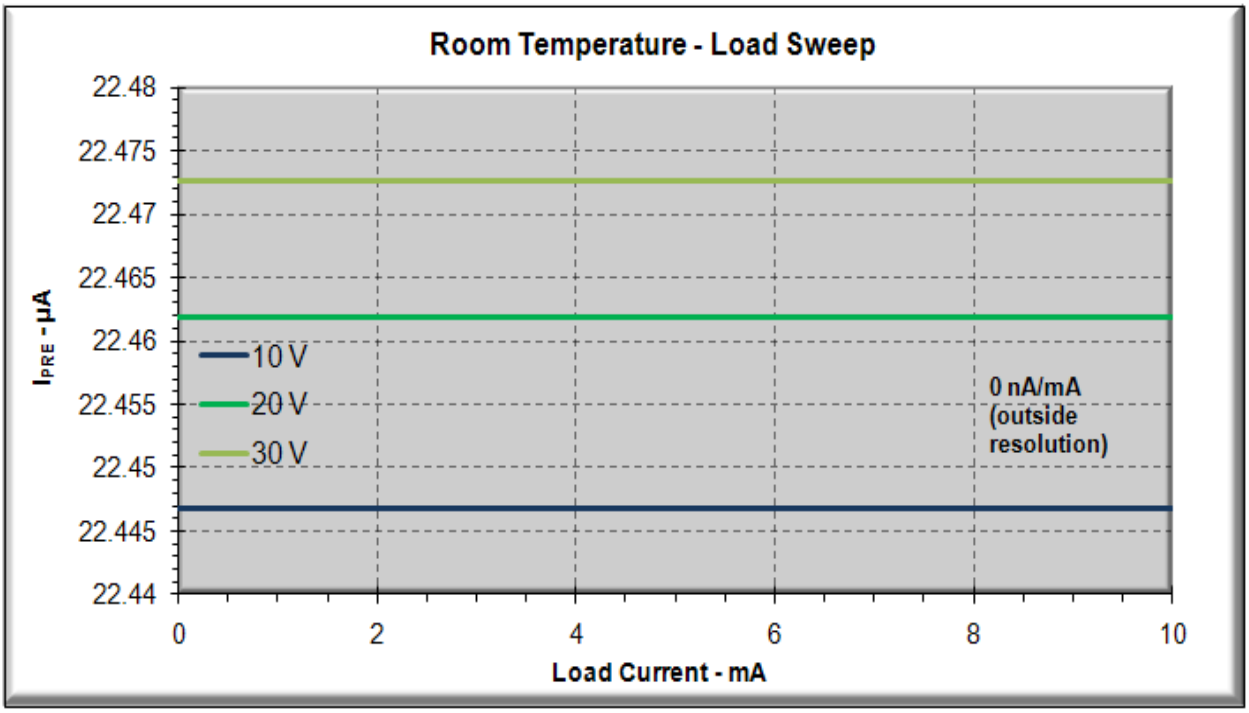

Figure 3.15 – Simulated I_{PRE} Load Regulation

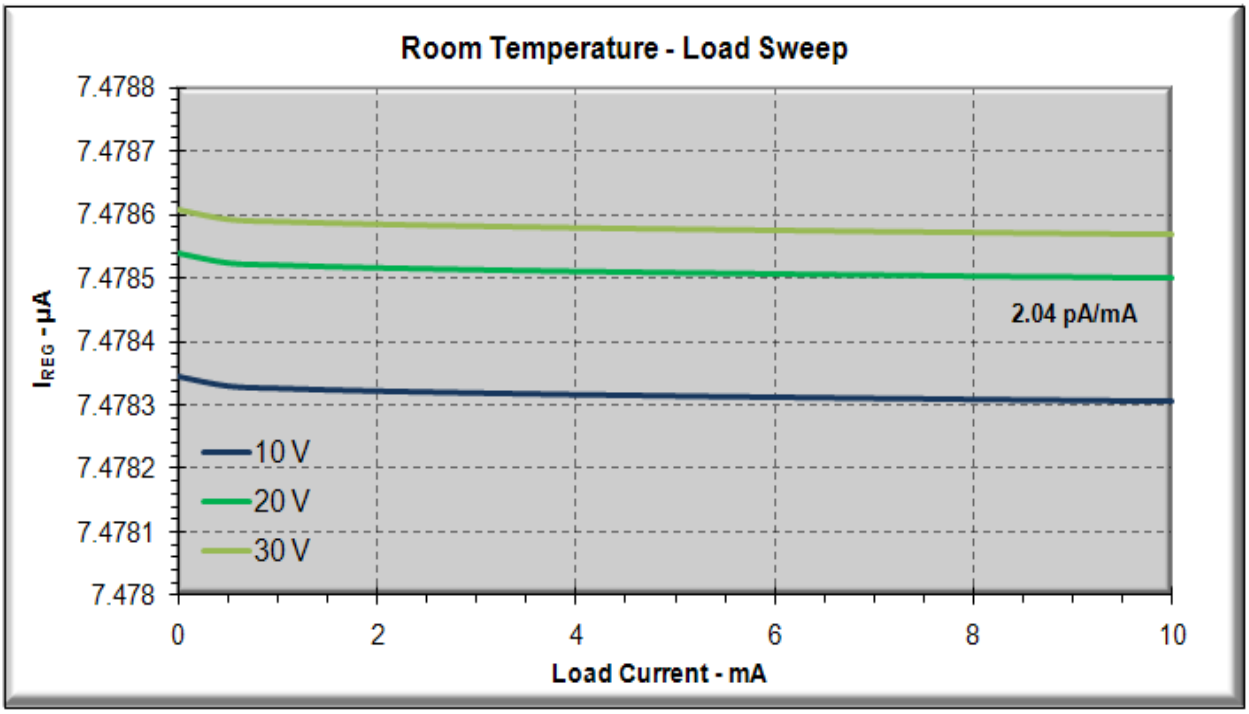

Figure 3.16 – Simulated I_{REG} Load Regulation

3.2.5 – Temperature Characteristic

One of the main initiatives in developing this gate driver project is the requirement for all circuits to operate up to 200 °C. Current LM723 designs offer temperature ratings up to 125 °C, which is substantially less than the environment imposed by hybrid electric engines. This voltage regulator design is simulated over a wide temperature range (−50 °C to 200 °C) to ensure all environmental conditions have been examined. Figures 3.17 - 3.22 demonstrate temperature sweep simulation results for V_{DD}, V_{PRE}, V_{REF}, I_{PRE}, I_{REG}, and I_{SUPPLY}, respectively. As Figure 3.17 illustrates, V_{DD} varies less than 7 mV over the full 250 °C temperature range (regardless of changes in V_{DDH} or load current). The Zener reference topology along with the additional temperature compensation described in section 3.1.2 allow for the small temperature dependence observed. The temperature compensation resistor *R8* in Figure 3.3 takes advantage of temperature coefficient of the current through *D3* by providing a voltage drop with a temperature coefficient complementary to that of the Zener diode breakdown voltage. In addition to the small temperature dependence of V_{DD}, the consistency of the temperature characteristic of V_{DD} for all V_{DDH} voltages and load currents allows for predictable operation in nearly any application. The temperature characteristic of V_{PRE} shows a significant dependence on V_{DDH} while load condition has an insignificant effect. V_{DDH} variation demonstrates an alteration of the temperature characteristic for V_{DDH} values close to V_{PRE}. For V_{DDH} voltages greater than ~11 V, the supply voltage has an insignificant effect on temperature characteristic. The combination of the temperature coefficients of V_{PRE} and $V_{DS,SAT}$ of the p-channel LDMOS devices *M13* and *M14* result in the observed temperature curves (Figure 3.18). Just as was the case with V_{DD}, the temperature characteristic of V_{REF} illustrates virtually no dependence on V_{DDH} or load current (see Figure 3.19). V_{REF} exhibits only a 17 mV variation over the full 250 °C simulation. Figure 3.20 reveals that V_{DDH} and load current have an insignificant effect on temperature characteristics for I_{PRE}. This bias current varies about 5 µA over the full temperature sweep. This variation is due to the temperature dependence of V_{TH} and the temperature dependence of the resistivity of the poly2 layer. Changes in pre-regulator bias current do not affect the remaining regulator stages as long as the current demand of the regulator circuits on the pre-regulator does not exceed I_{D13}. In the event that regulator current demand exceeds the current available from *M13*-*M14*, *D1* will not have a bias current to establish V_{PRE}. Under this condition, the regulator circuits would be subject to unpredictable line voltages and circuit operation would be erratic.

To avoid this potential pitfall, $I_{D13,14}$ is set well above the worst case current draw of the regulator circuit. The regulator bias current temperature characteristic also exhibits little variability with V_{DDH} and load current changes (Figure 3.21). The I_{REG} temperature coefficient is a result of the temperature dependence of V_{BE}, poly2 resistivity, and p-well resistivity. The temperature coefficient of I_{REG} is actually advantageous, as the I_{REG} curve cancels the inherent temperature curve of the Zener diode. This complementary behavior illustrates the advantage of using Zener diodes to establish both the bias currents and reference voltage. The supply current draw visible in Figure 3.22 is the summation of the bias currents of all four voltage regulator stages. The maximum supply current draw is 324 µA at 100 °C, for a 30-V input. The voltage regulator is designed so that I_{SUPPLY} is parabolic with respect to temperature. The parabolic temperature characteristic results in the lowest possible variability in current draw over temperature. The power requirements of this voltage regulator are, therefore, very predictable. Figure 3.22 also shows that supply current is proportional to supply voltage. For a load condition, total supply current is the direct sum of the no load supply current and the load current.

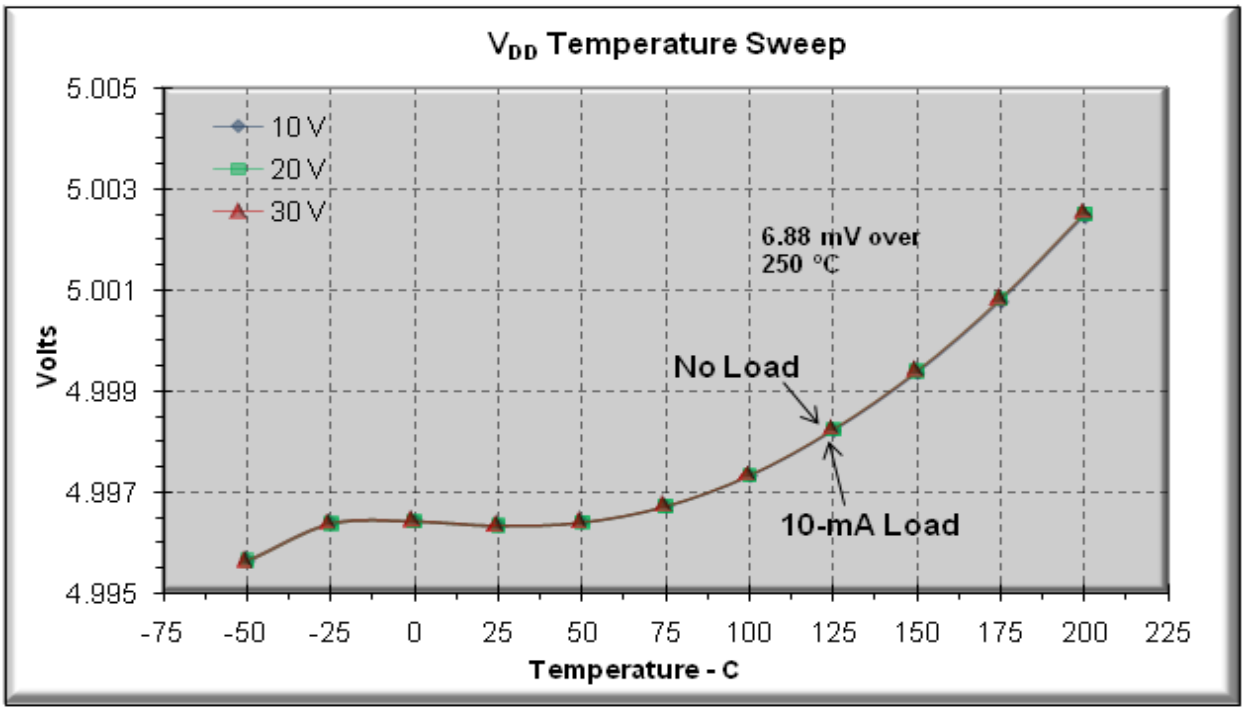

Figure 3.17 – Simulated V_{DD} Temperature Characteristic

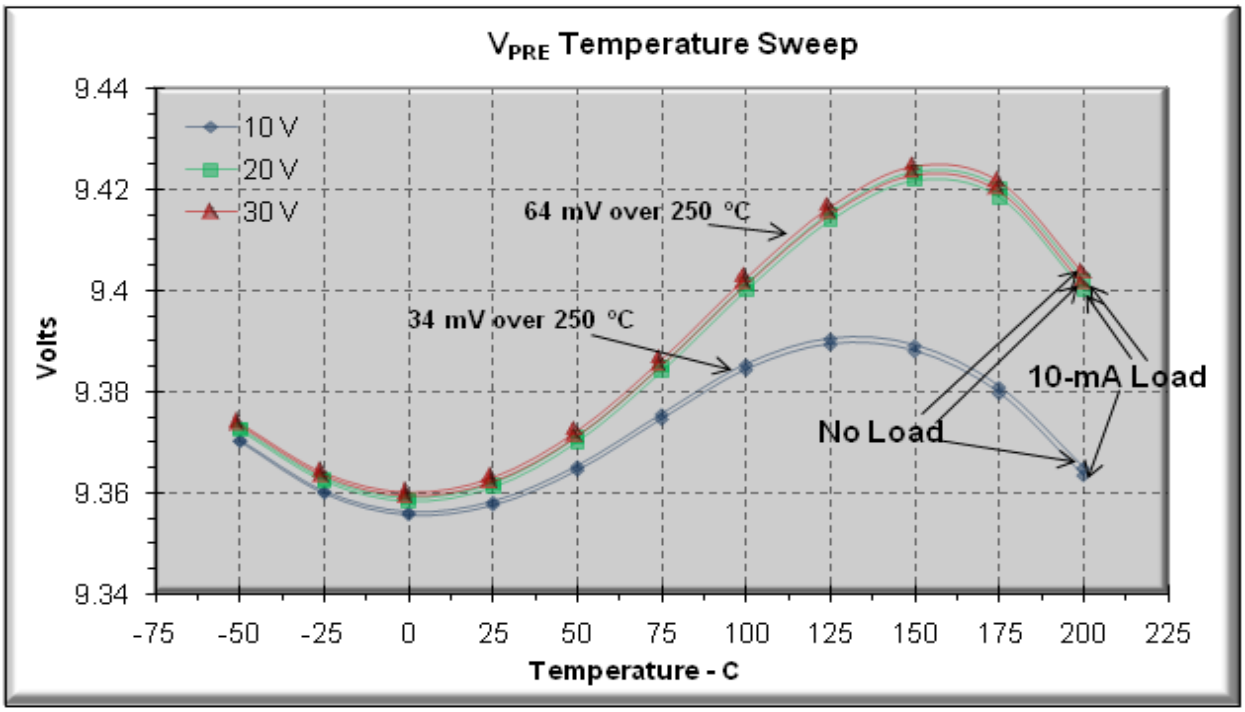

Figure 3.18 – Simulated V_{PRE} Temperature Characteristic

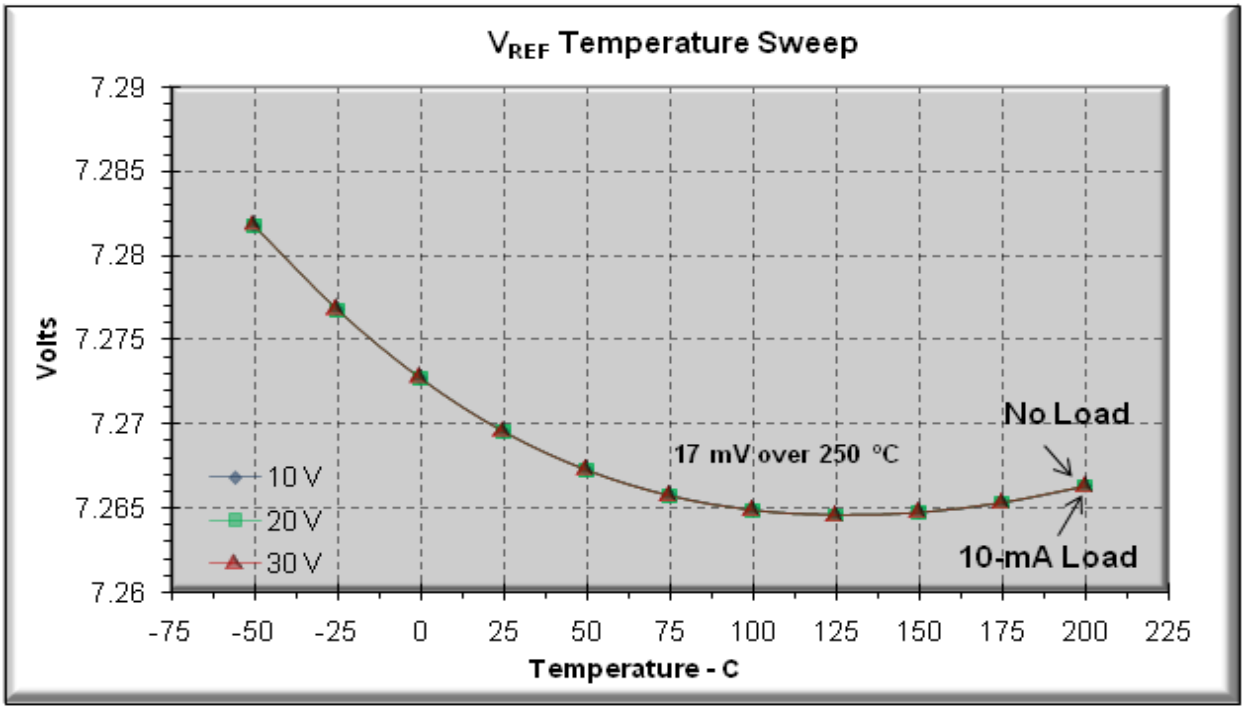

Figure 3.19 – Simulated V_{REF} Temperature Characteristic

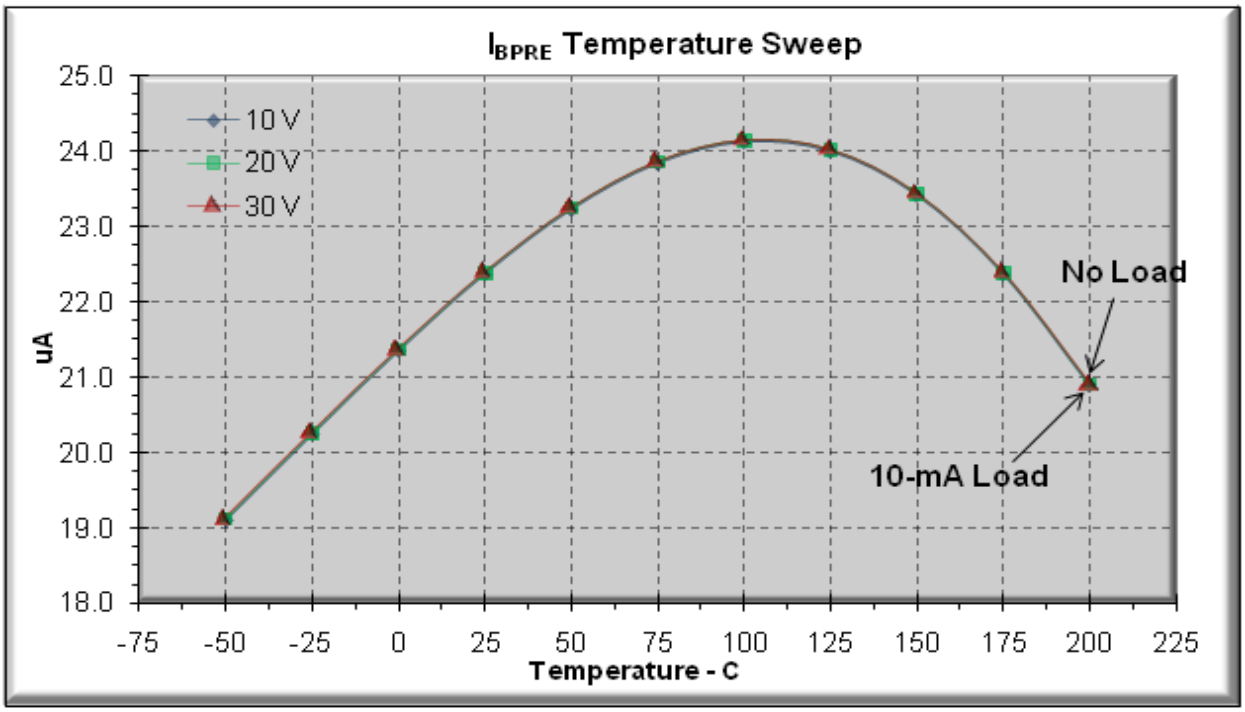

Figure 3.20 – Simulated I_{PRE} Temperature Characteristic

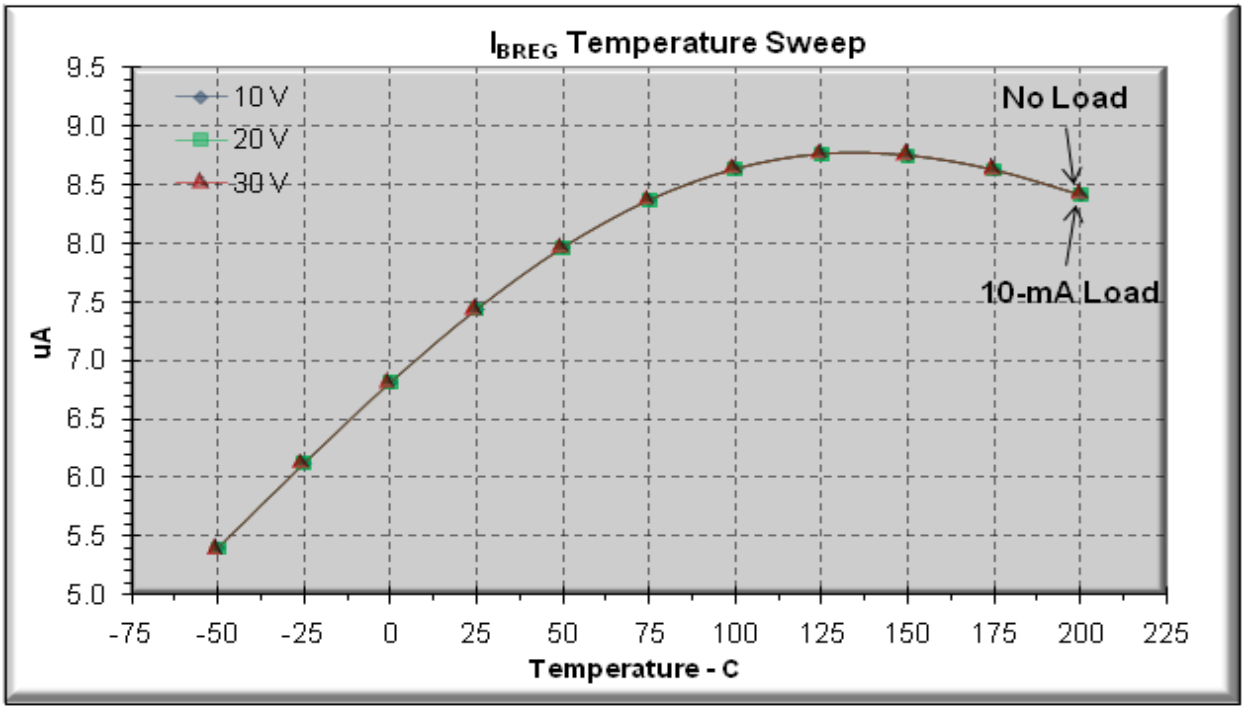

Figure 3.21 – Simulated I_{REG} Temperature Characteristic

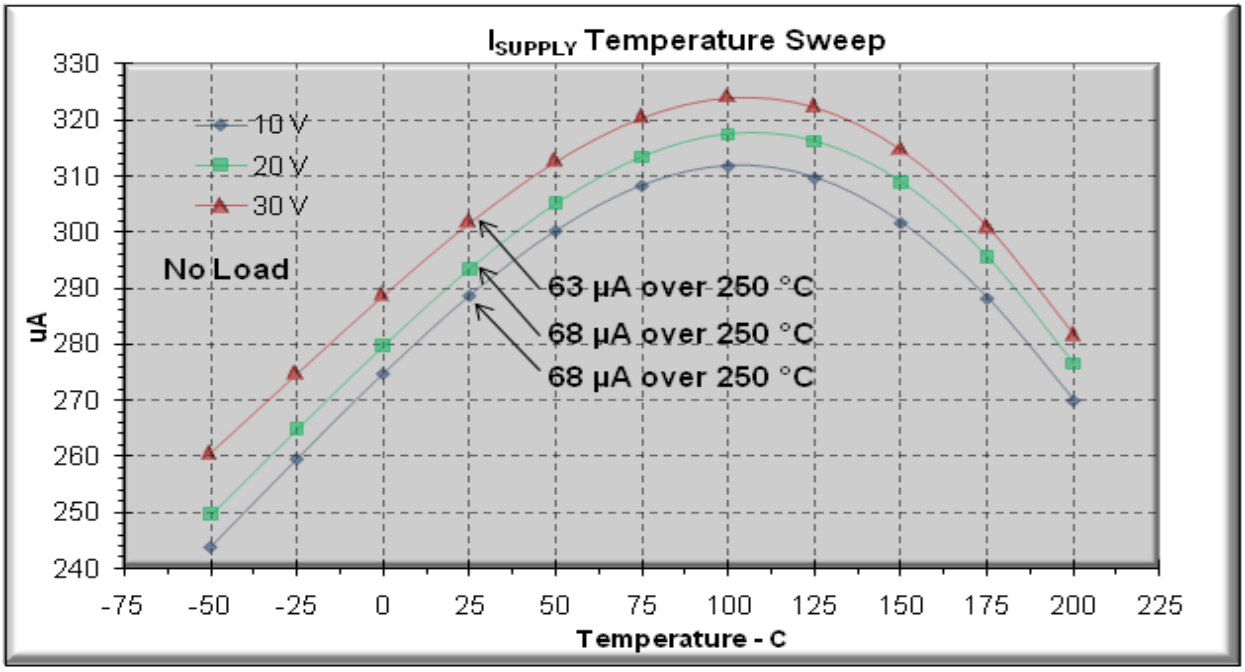

Figure 3.22 – Simulated I_{SUPPLY} Temperature Characteristic

3.2.6 – Load Transient

Figures 3.23-3.25 are the simultaion results of the voltage regulator in response to a 220-mA load transient at −50 °C, 25 °C, 200 °C, respectively. V_{DDH} is set to 20 V, and an output capacitor of 3.8 µF is used as a charge storage device. V_{DD} and V_{PRE} drop linearly during the 220-mA current draw as the load capacitor discharges and current demands on V_{DD} increase. In the gate driver application, the transient loads have a much shorter pulse width than demonstrated in these simulations (several orders of magnitude shorter). The shorter pulse widths remove the linear drop of V_{DD} and V_{PRE} seen in these simulations. V_{REF} exhibits extreme resistance to load transients, which is consequential to the use of the operational amplifier (essentially a buffer). Throughout the load transient, the regulator is able to restrict the output voltage to within 99.6 % of nominal V_{DD}. The load transient effect on V_{DD} is nearly independent of temperature. The load transient effect on V_{PRE} is pronounced at the extreme ends of the temperature range; however, the worst-case effect is still limited to under a mV total displacement. The response observed on V_{REF} to a load transient increases with temperature; the worst case for the load transient reponse of V_{REF} is under 100-µV total displacement.

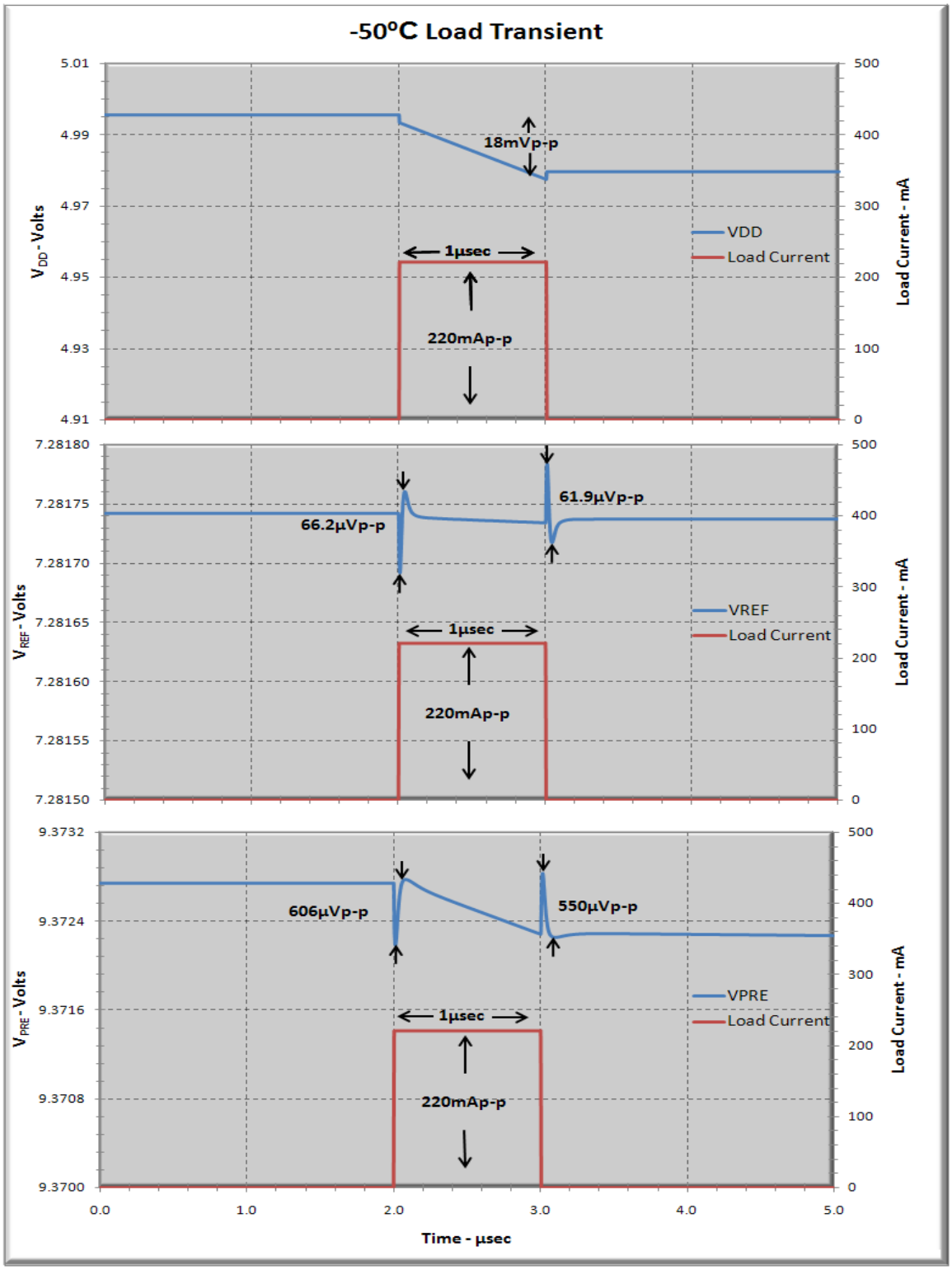

Figure 3.23 – Simulated −50 °C Load Transient

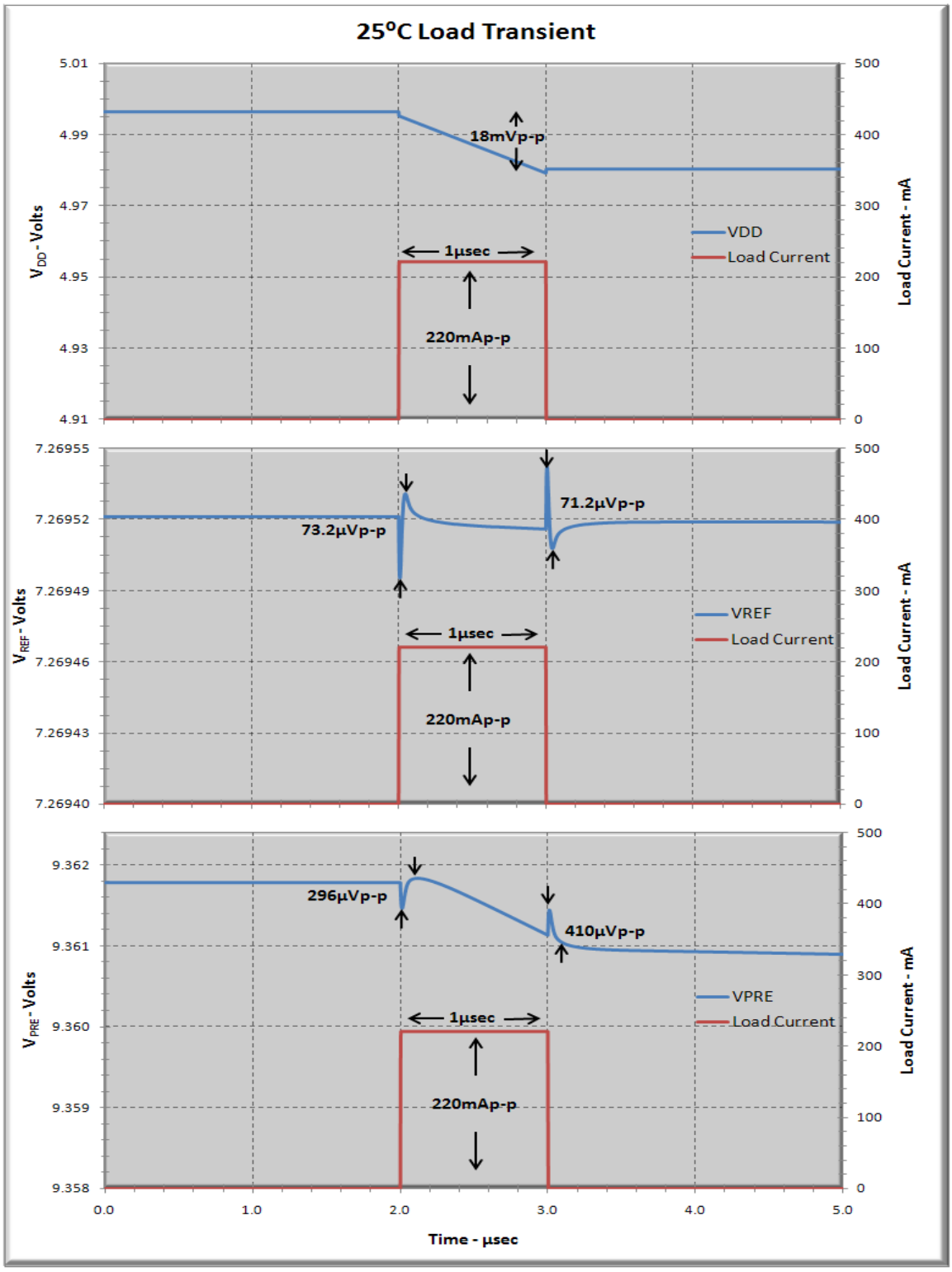

Figure 3.24 – Simulated 25 °C Load Transient

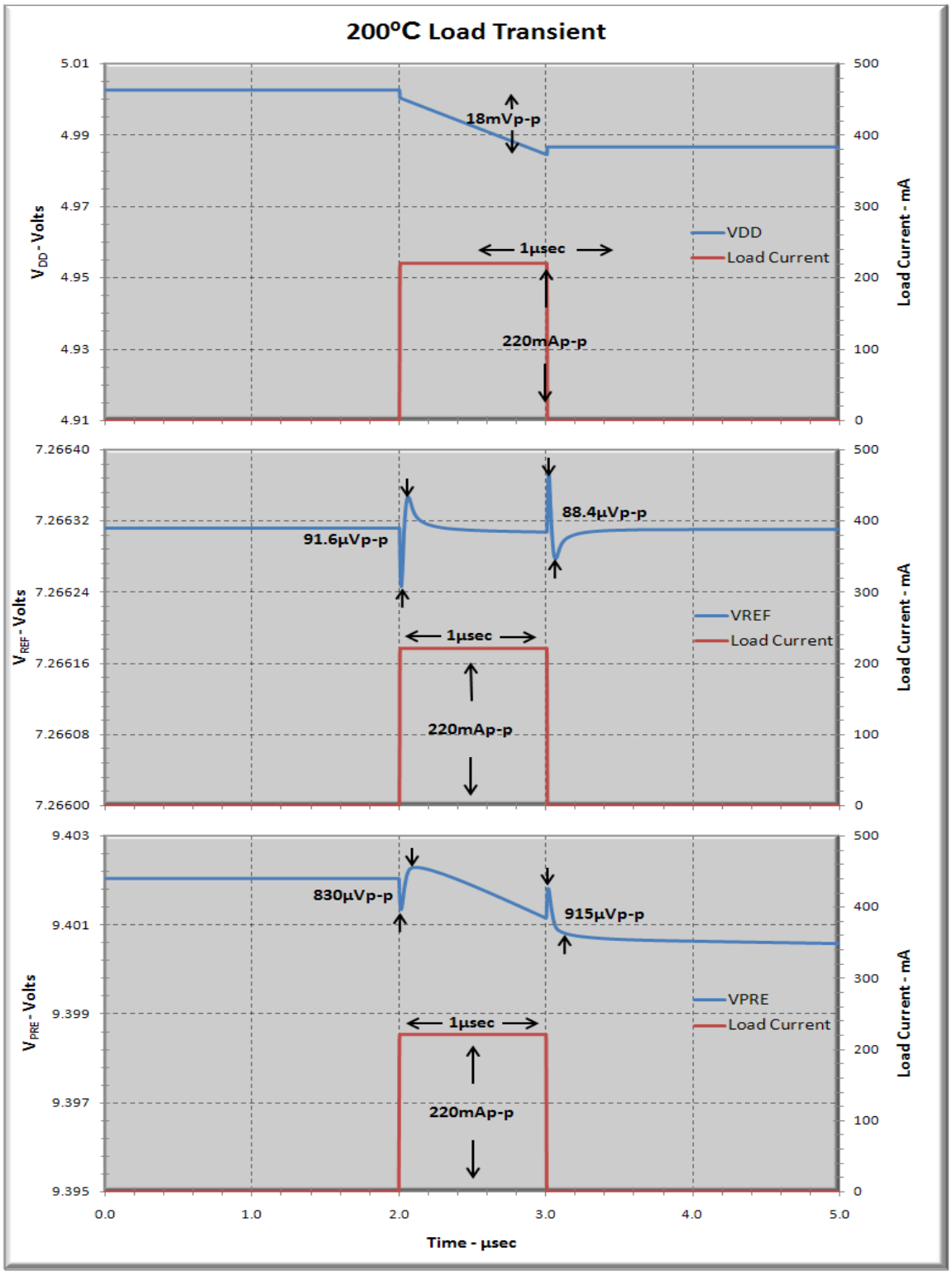

Figure 3.25 – Simulated 200 °C Load Transient

3.2.7 – Line Transient

Figures 3.26-3.28 examine the simulated voltage regulator response to a line transient of 5 V_{p-p} at −50 °C, 25 °C, 200 °C respectively. In this simulation, V_{DDH} switches between 20 V and 25 V with fast edges as demonstrated in the figures. The line transisent simulation reveals small transient pulses in both the pre-regulator voltage and the reference voltage at both rising and falling edges of a line transient. The amplitude of these pulses is greatest in the first stage of the circuit and is attenuated throughout the remaining voltage regulator stages. V_{DD} exhibits no suceptibility to a falling edge line transient (due to the class-A output stage) and shows only a modest change in output voltage in response to a rising edge transient. The amplitudes of V_{DD} during a line transient are inversely proportional to temperature. V_{DD} is regulated to within 99.97 % of nominal V_{DD} even under the worst case (−50 °C) line transient. V_{PRE} exhibits a significant line transient response (on the order of Vp-p) with a complementary relationship to temperature. This result is expected, as V_{PRE} is directly connected to V_{DDH}. The resistance to line transients in the remaining voltage regulator stages is attributeable in part to the resistance to line transients found in V_{PRE}. The line transient response of V_{REF} is directly related to the response of V_{PRE}. An attenuated effect of V_{PRE} is visble in V_{REF}, resulting in a similar temperature dependence. The ability of the voltage regulator to perform well in the presence of line transients allows the voltage regulator to be implemented in applications where reliable power supplies may not be avaliable (almost any embedded application). Reducing the restrictions on supply voltage required by a regulator widens the potential applications for the voltage regulator, and therefore, improves the marketability of the voltage regulator.

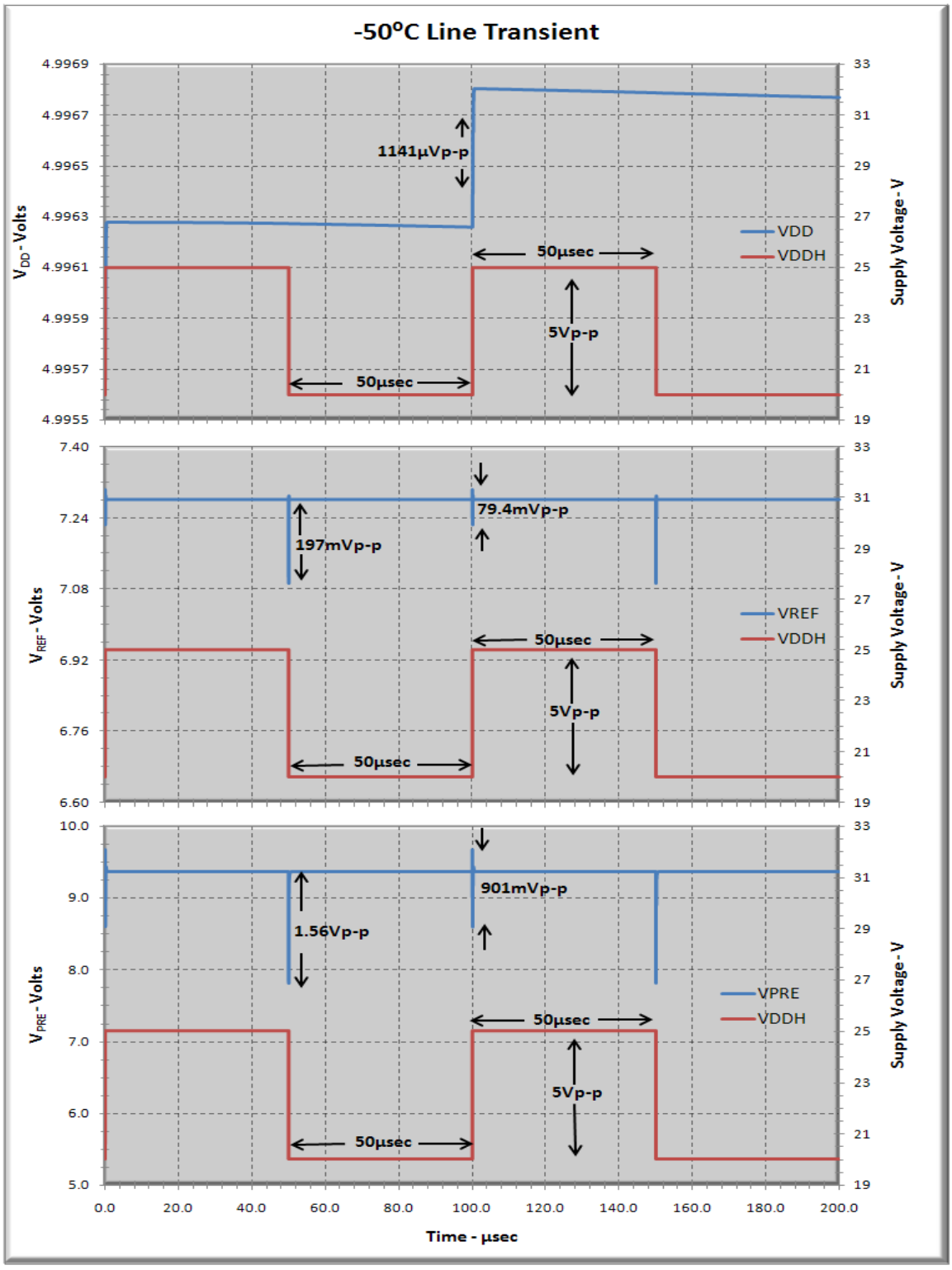

Figure 3.26 – Simulated −50 °C Line Transient

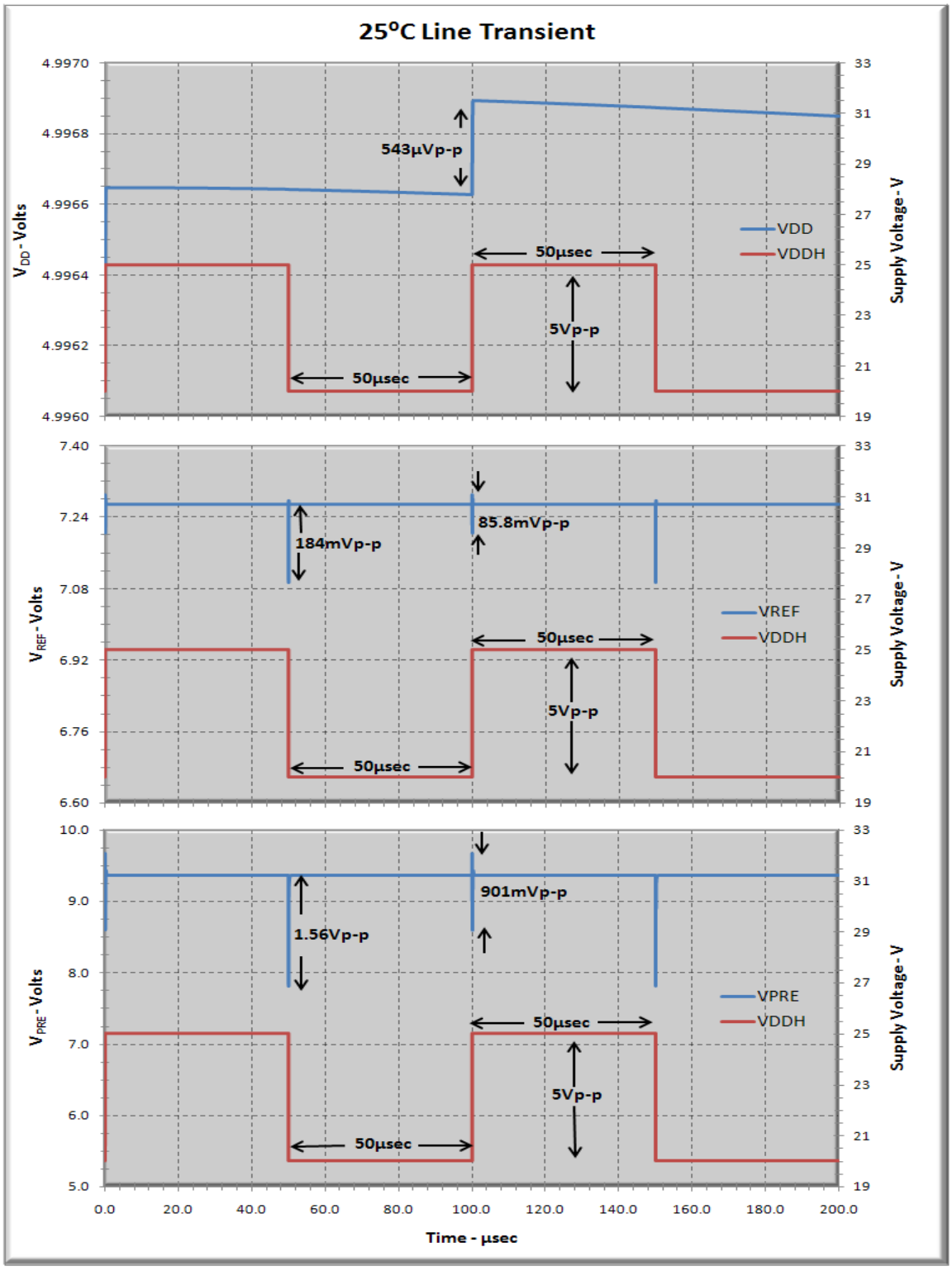

Figure 3.27 – Simulated 25 °C Line Transient

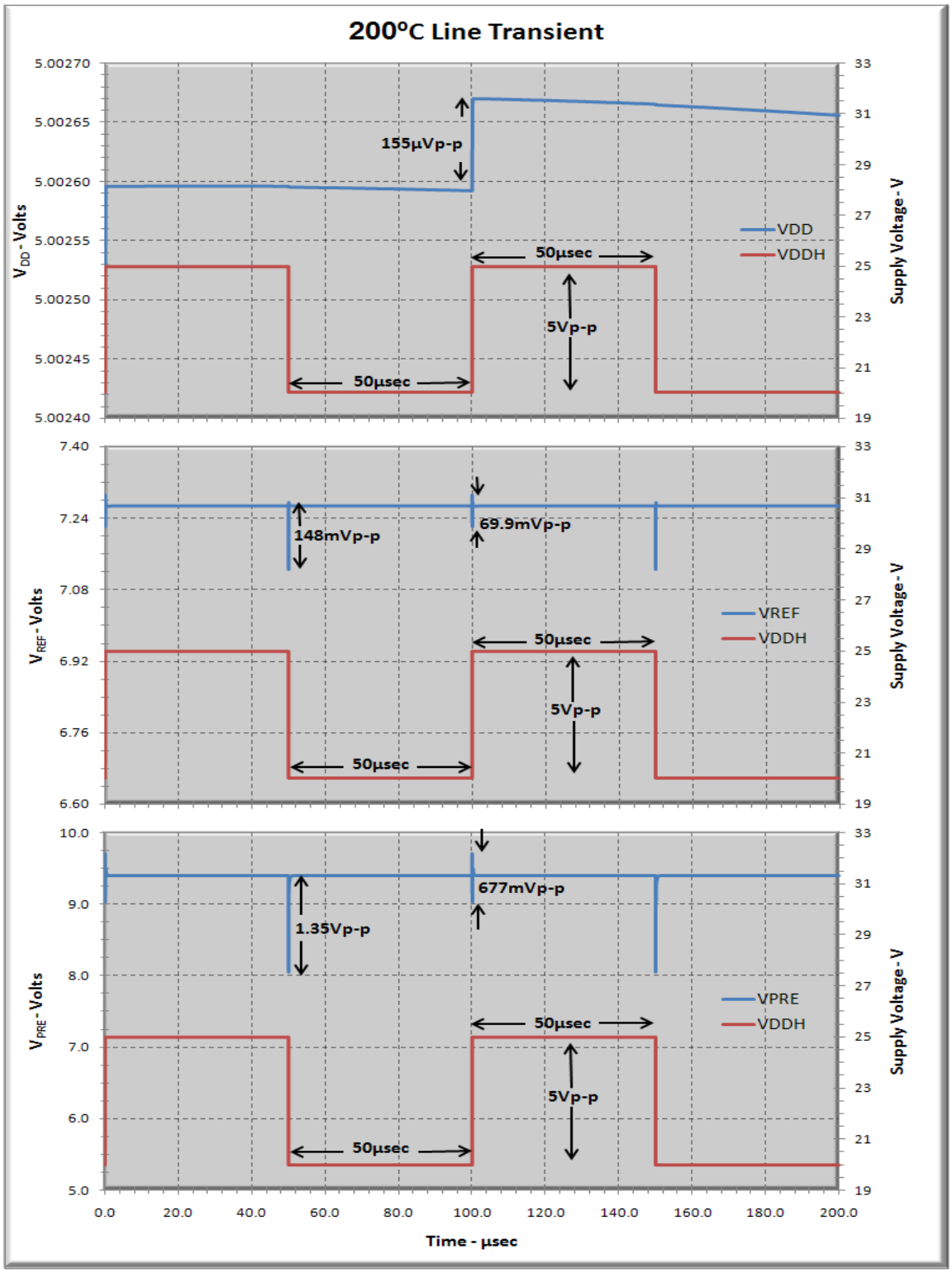

Figure 3.28 – Simulated 200 °C Line Transient

4. Post-Fabrication Verification

4.1 – Voltage Regulator Testing Set-Up

The voltage regulator layout in Figure 4.1 segregates each circuit stage in the voltage regulator design. Device matching is impossible for all BJT, LDMOS, and MOSCAP devices due to the non-self aligned nature in this SOI-process. The overall layout is compact which minimizes chip area and process variation. Figure 4.2 shows the fabricated chip in contrast to the layout image. The total device area for the voltage regulator design is less than 0.5 mm^2. A large portion of this chip area is used for on-chip capacitors. This capacitor area can be greatly reduced to accommodate smaller die areas in future fabrications. High-voltage ESD for pins exceeding 5 V is implemented using a gate-source connected, high-voltage LDMOS. Low voltage ESD for pins within 5 V is implemented using standard Zener diode ESD pads. Measurement data is obtained through a printed-circuit board (PCB) test set-up, using high-temperature components. Figure 4.3 shows the complete test board. The 4-layer PCB is fabricated with polyimide dielectric, immersion gold contact finish, and PSR-9000 FXT solder resist for optimal high-temperature performance.

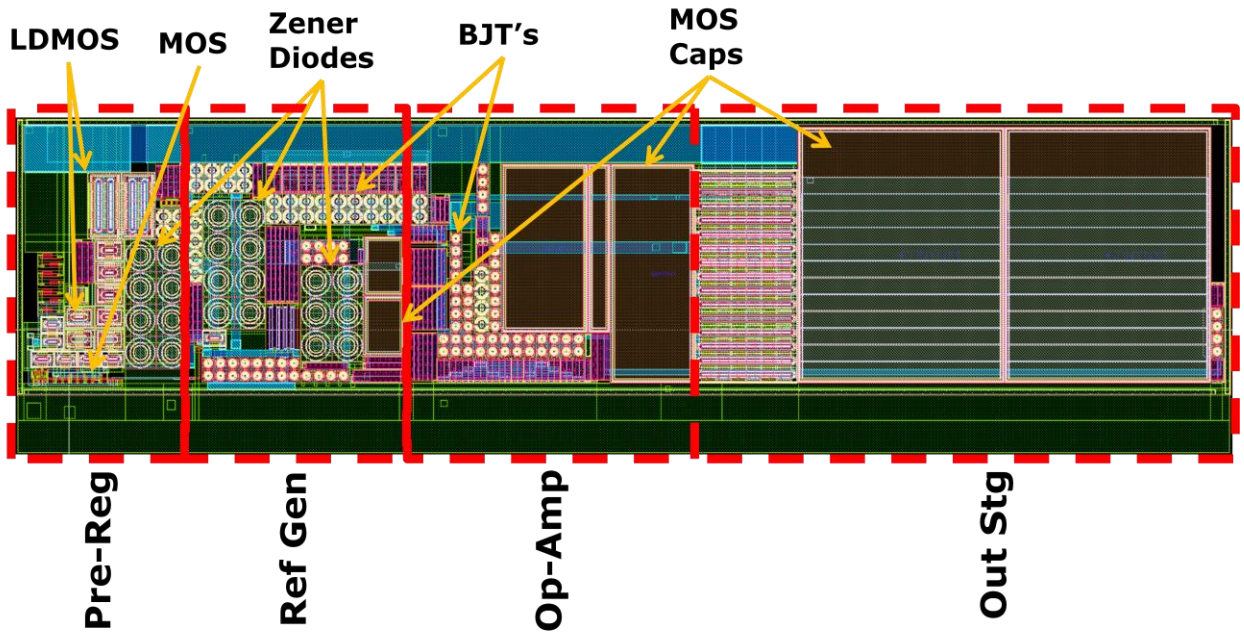

Figure 4.1 – Voltage Regulator Layout

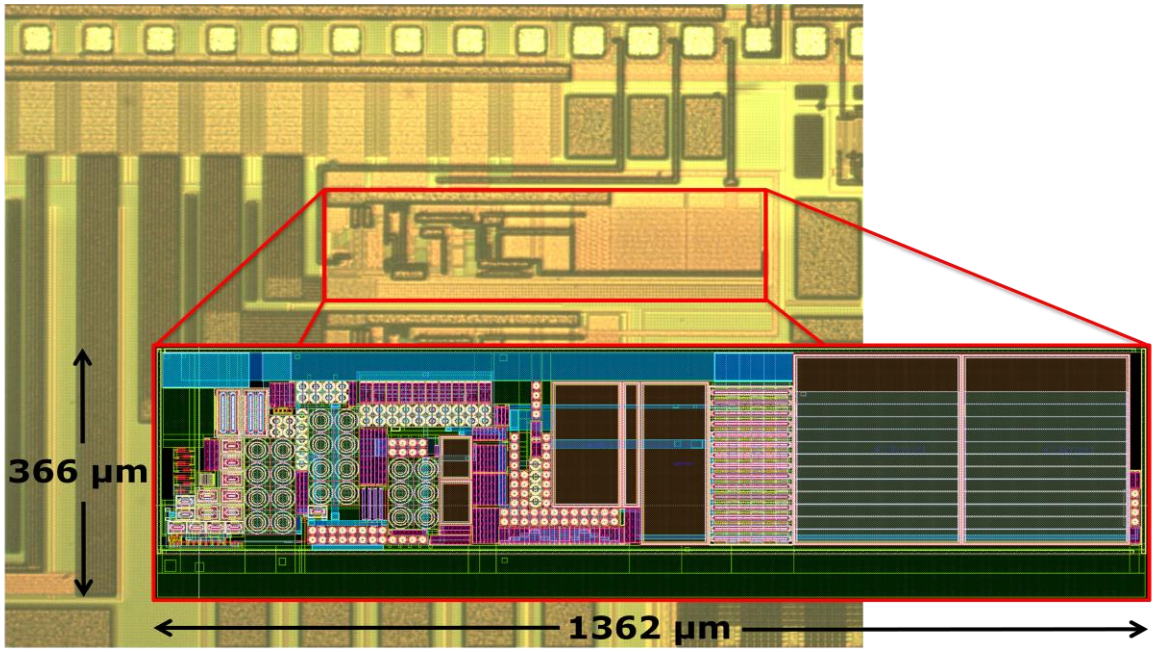

Figure 4.2 – Voltage Regulator Post-Fabrication

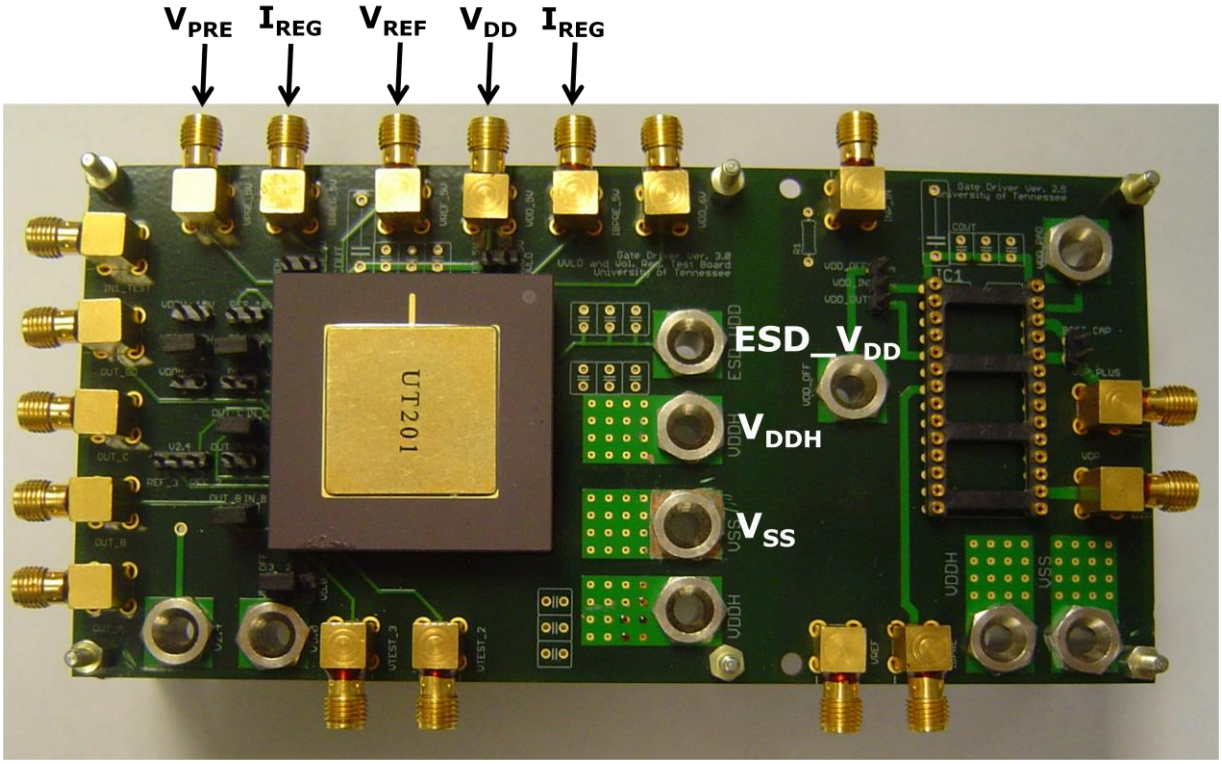

Figure 4.3 – Voltage Regulator Test Board

High-temperature, Teflon-insulated, gold-plated SMA connectors are used to route signals to and from the test board. Power is supplied via banana plugs and high-temperature, Teflon wire. On-board capacitance is provided by NPO ceramic capacitors, which provide a stable capacitance over temperature. This test board is designed to support independent or collaborative testing of the voltage regulator and the under voltage lock out circuits (a sub-circuit on the gate driver project). The DC testing (input start-up, line regulation, load regulation, and temperature testing) is performed using Labview 8.5-controlled Hewlett-Packard E3631A power supplies, Agilent 34401A multimeters, and Keithley 2400 ammeters. During each iteration of a test, the Labview code sets the independent variable for the specific test (load current or supply voltage), measures each instrument, writes the data to arrays, and increments the independent variable. After the final iteration, the arrays of each measurement are compiled and written to a text file.

4.2 – Input Voltage Start-Up

Figure 4.4 illustrates the voltage regulator performance during start-up. Results similar to simulations are observed, as the voltage regulator is functional for V_{DDH} voltages greater than 8.3 V. This result is consistent with predicted and simulated start-up values. The 8.3 V start-up voltage verifies voltage regulator functionality for a V_{DDH} voltage of 10 V (the lower limit).

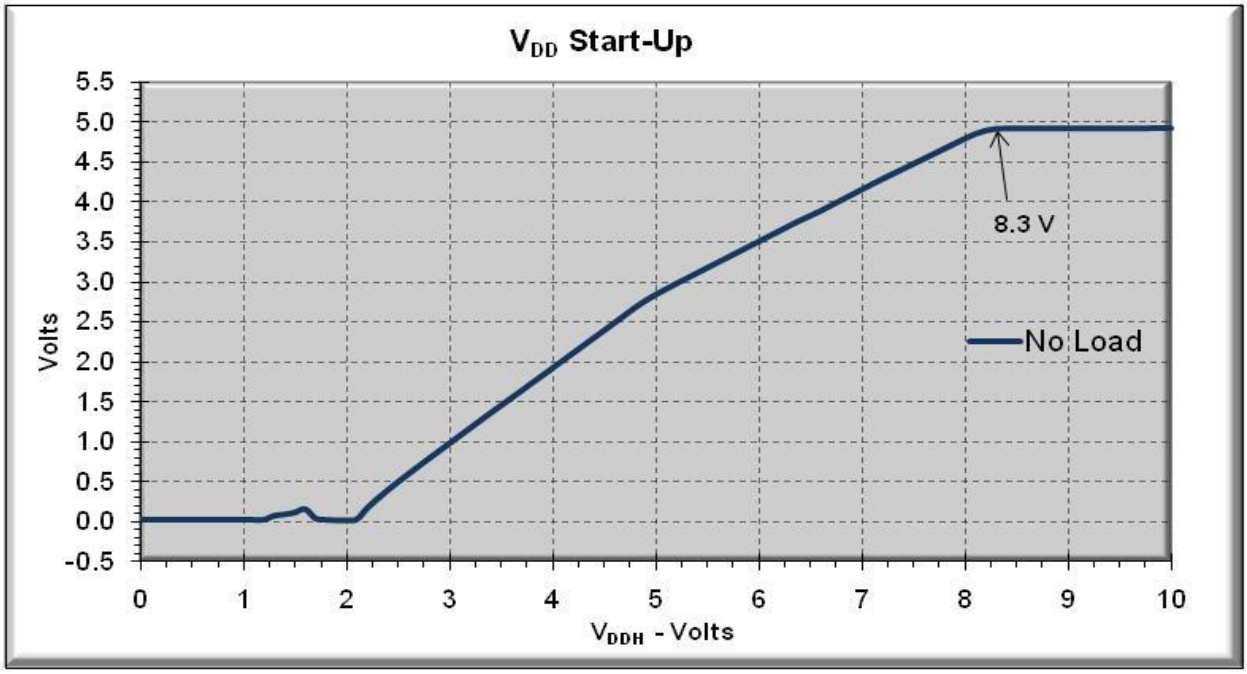

Figure 4.4 – Measured Voltage Regulator Start-Up

4.3 – Line Regulation

The designed voltage regulator is functional on a V_{DDH} range of 8.3 V to 35+ V. Figures 4.5-4.8 reveal the voltage regulator response to a V_{DDH} voltage sweep under no load and 10-mA load conditions. As seen in simulation results, V_{DD} possesses a proportional relationship with V_{DDH} for both loading conditions. Comparing measured results to simulations, a significant decrease in calculated line regulation is observable; however, noise limits the measurable resolution of V_{DD} to well above the order of ppb found in simulation results. The actual line regulation for the voltage regulator is not accurately measureable using the equipment described in section 4.1. The relationship between V_{DD} and V_{DDH} is emphasized with a 10-mA load present, but still well within design constraints. As predicted in simulations, the "on" resistance of the pass transistor causes V_{DD} line sensitivity, but self-heating of the voltage regulator under a load condition increases this effect. Noise renders accurate readings of V_{PRE} difficult (Figure 4.6), but the general trend of V_{PRE} as a function of V_{DDH} is visible as a proportional relationship (due to channel length modulation). Self-heating of the voltage regulator under a load condition affects V_{PRE} in a manner similar to V_{DD}. The measured line regulation of V_{PRE} matches the simulated line regulation fairly well with only small, constant deviations. V_{REF} is almost independent of supply voltage under the no load condition; however, an inversely proportional relationship is demonstrated during a DC load condition (Figure 4.7). Self-heating is again responsible for the decrease in line regulation V_{REF} shows in the presence of a load. V_{REF} still exhibits a line regulation on the order of ppm/V, and has minimal effect on the voltage regulator operation. The simulated vs. measured results of V_{DD}, V_{PRE}, and V_{REF} correlate well, which implies a robust design. I_{REG} exhibits similar line regulation characteristics to V_{REF} during an input voltage sweep (Figure 4.8). The regulator bias current is essentially independent of V_{DDH} under a no load condition, but the bias current increases proportionally to supply voltage in the presence of a DC load due to self-heating. As with V_{REF}, the small line sensitivity of I_{REG} will have a negligible effect on the voltage regulator performance. Overall, the voltage regulator demonstrates remarkable line regulation (for both no load and DC load current) at all circuit stages.

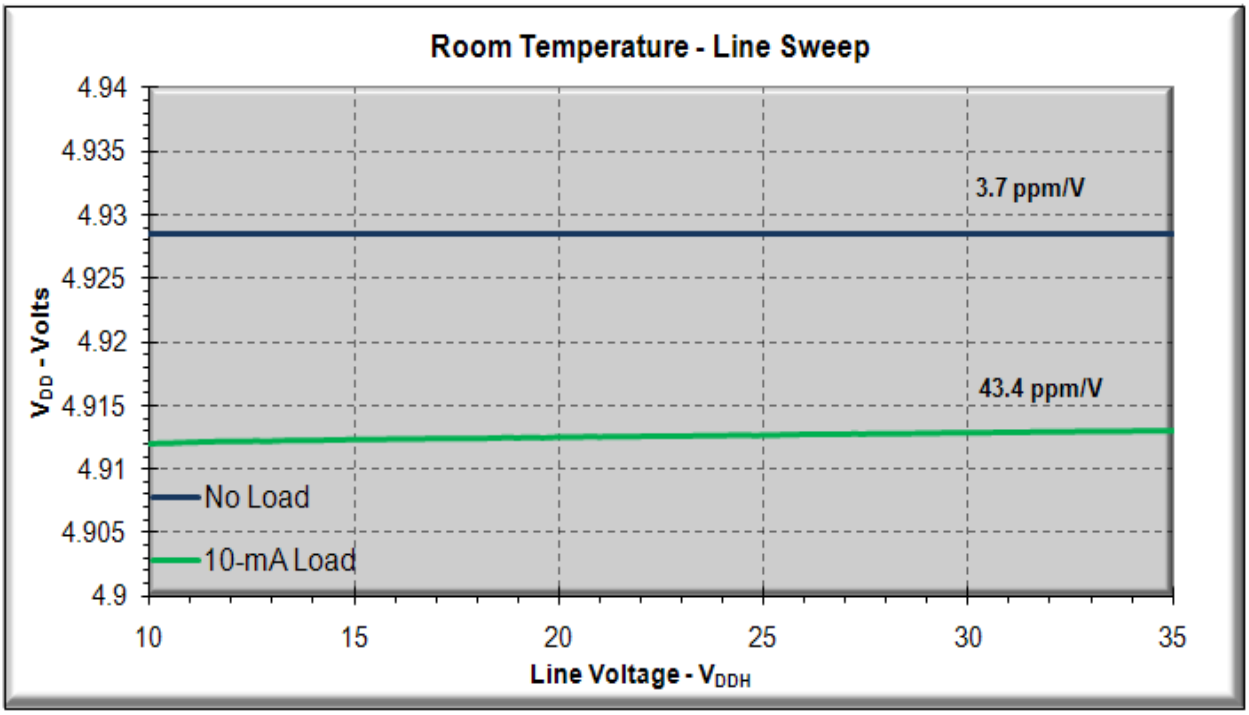

Figure 4.5 – Measured V_{DD} Line Regulation

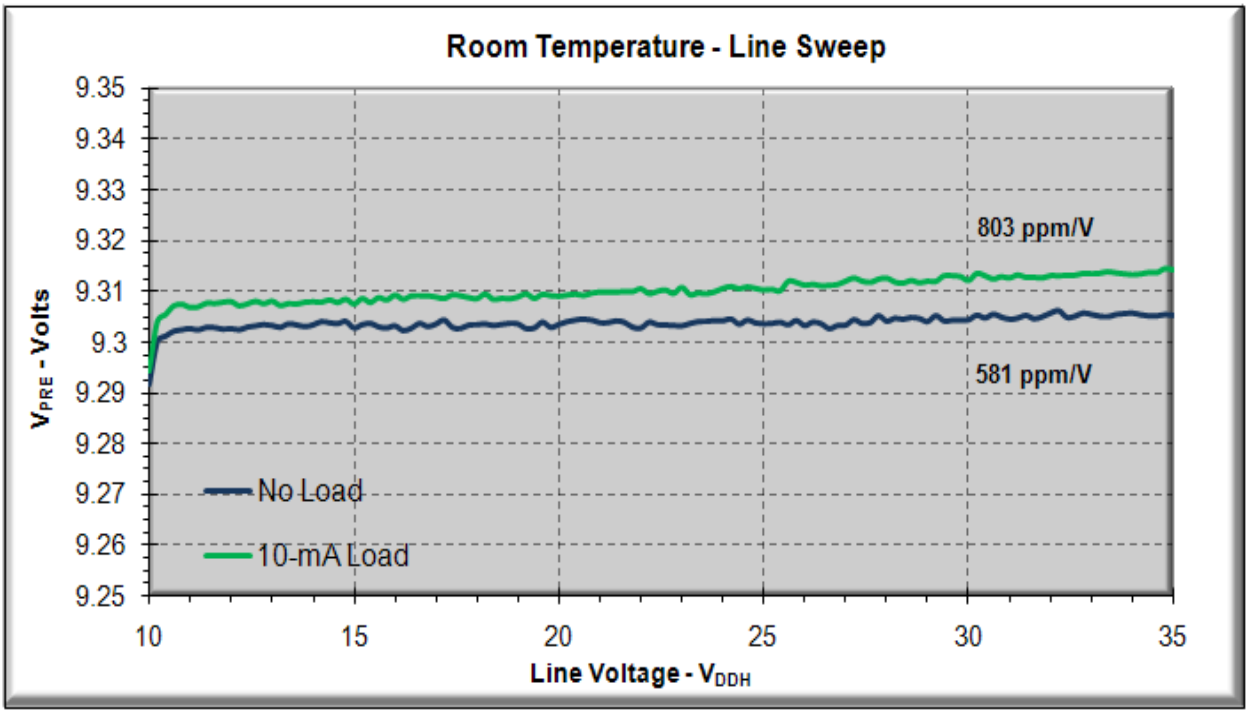

Figure 4.6 – Measured V_{PRE} Line Regulation

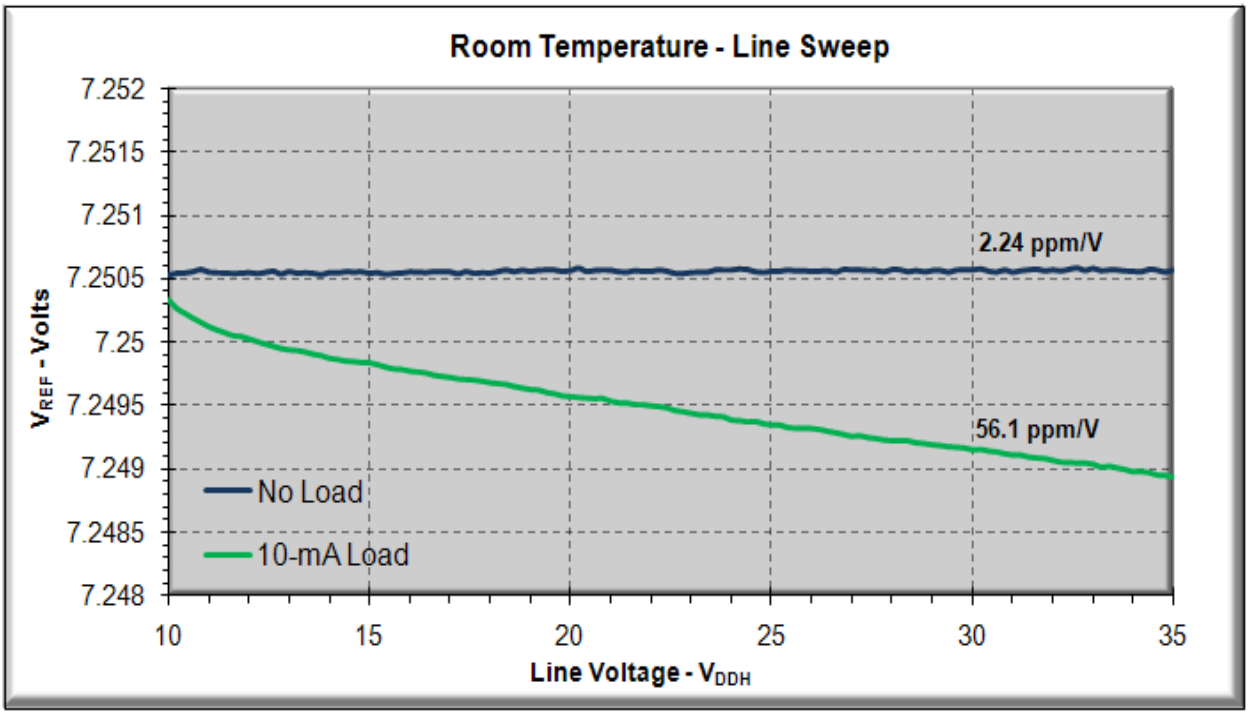

Figure 4.7 – Measured V_{REF} Line Regulation

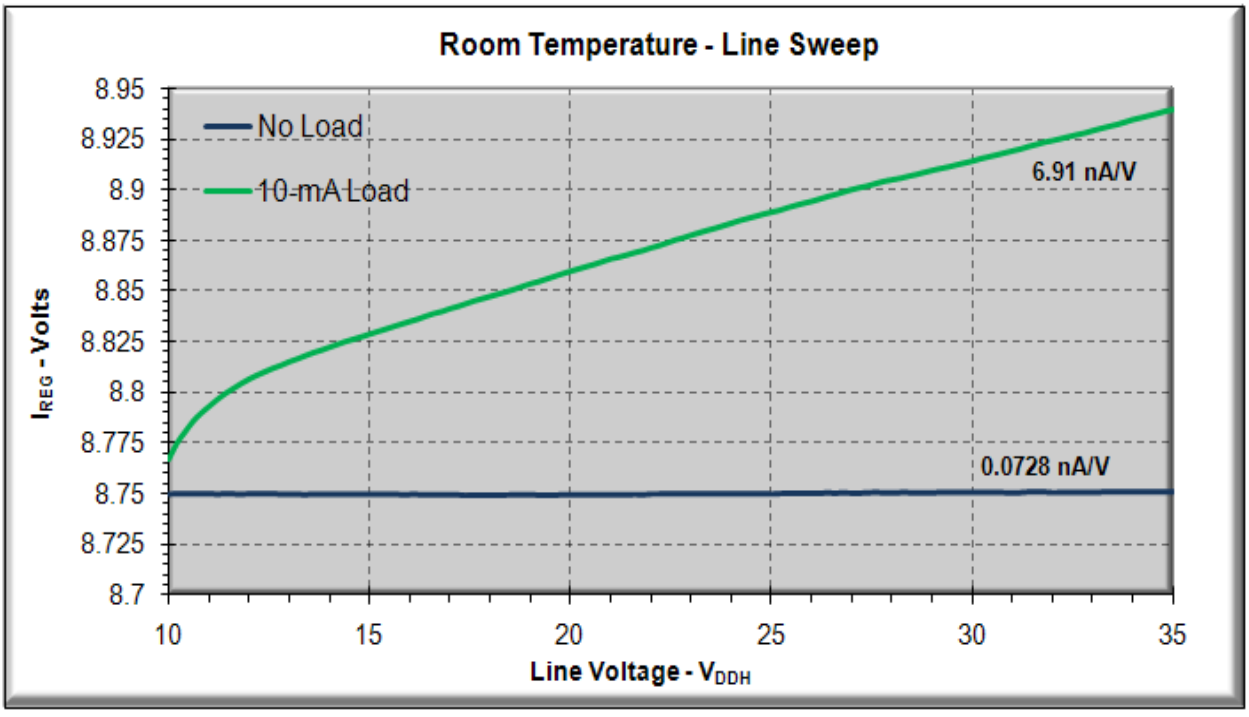

Figure 4.8 – Measured I_{REG} Line Regulation

4.4 – Load Regulation

The gate driver specifications for this voltage regulator require only about 250-µA DC current capability; however, the output is subject to transient load currents of 200 mA. To ensure reliable operation, the voltage regulator is capable of safely supplying over 300 mA of DC current. For testing purposes, the load regulation measurements are only performed to 10 mA, which is well below the capability of the regulator but well above the design requirements. Figures 4.9-4.13 illustrate the voltage regulator response to the load current sweep for 10-V, 20-V, and 30-V input voltages. In Figure 4.9, V_{DD} displays a linear relationship to load current indicating a linearly decaying R_{DS} of the pass transistor. This resistance is inversely proportional to load current and induces a small voltage drop, which reduces the overall output voltage. V_{DD} decays as load current increases at the rate much higher than simulations predicted. This rate of change decreases very slightly as V_{DDH} increases. The discrepancy between measured and simulated load regulation most likely arises from model inaccuracies of the high-voltage NMOS device (used as the pass device). The annular gate used in these devices is difficult to accurately model for simulation. The R_{DS} resistance can be decreased by increasing the width of the pass device, or by increasing gate overdrive. For this project, the DC current requirements do not require a strict DC load regulation; the measured load regulation is acceptable for most applications. A small, proportional relationship between V_{PRE} and load current is illustrated in Figure 4.10. This relationship is predominantly due to the effects described in simulation results, but self-heating as load current increases also contributes to the observed response. V_{REF} (Figure 4.11) possesses an extreme resistance to load current which is consistent with simulation results. The observable effects of V_{DDH} on the load regulation of V_{REF} (Figure 4.11) stem from increased power dissipation at higher V_{DDH} voltages. Figure 4.12 reveals a linear relationship between pre-regulator bias current and load current. In this case, the heat generated from load current lowers the threshold voltage of the NMOS devices in the threshold referenced current source of the pre-regulator and increases the generated bias current. Figure 4.13 examines the relationship between the regulator bias current and load current which is found to be similar to the relationship found in the pre-regulator bias current. Neglecting self-heating, measured load regulation results match simulated load regulation results at all voltage regulator stages, save V_{DD}. Overall, the regulator performs well under a wide range of load conditions.

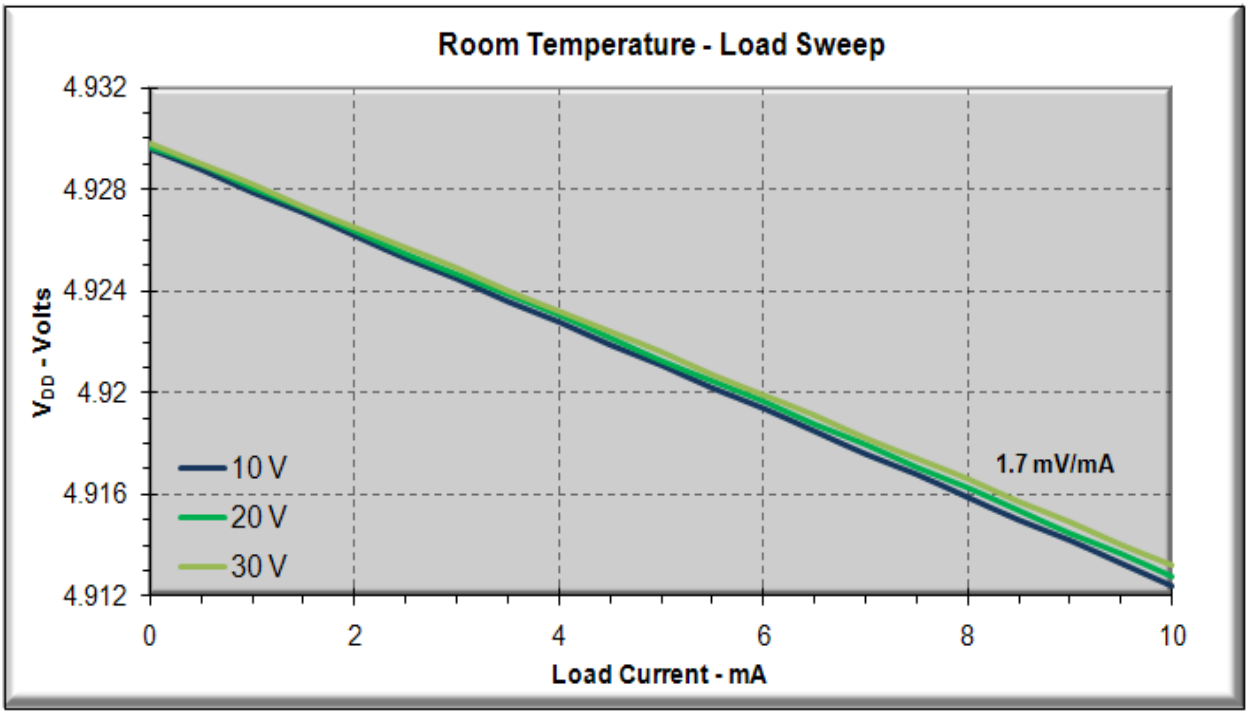

Figure 4.9 – Measured V_{DD} Load Regulation

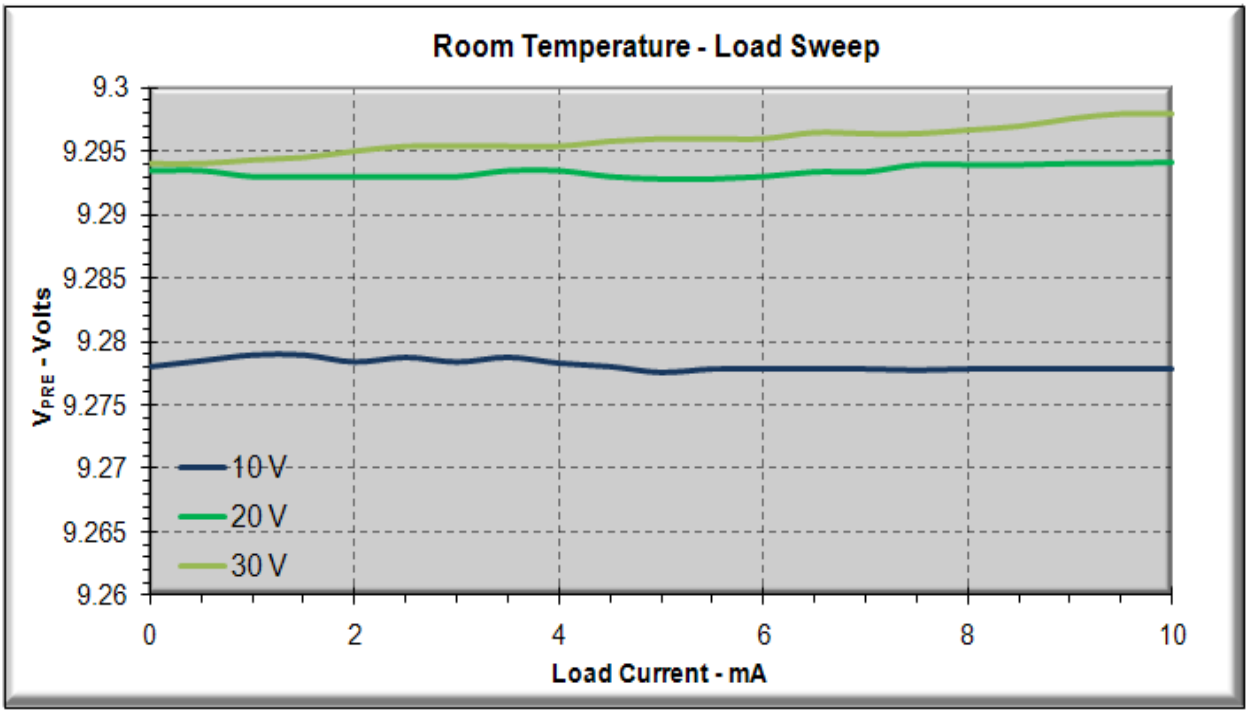

Figure 4.10 – Measured V_{PRE} Load Regulation

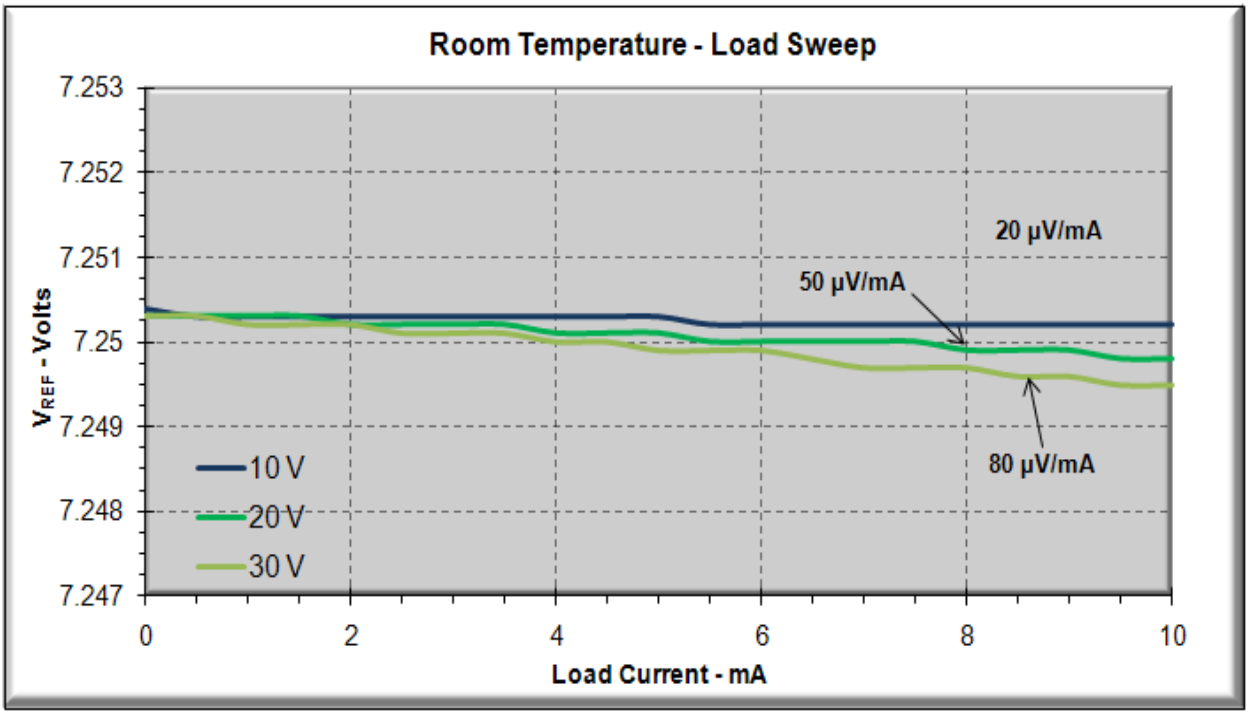

Figure 4.11 – Measured V_{REF} Load Regulation

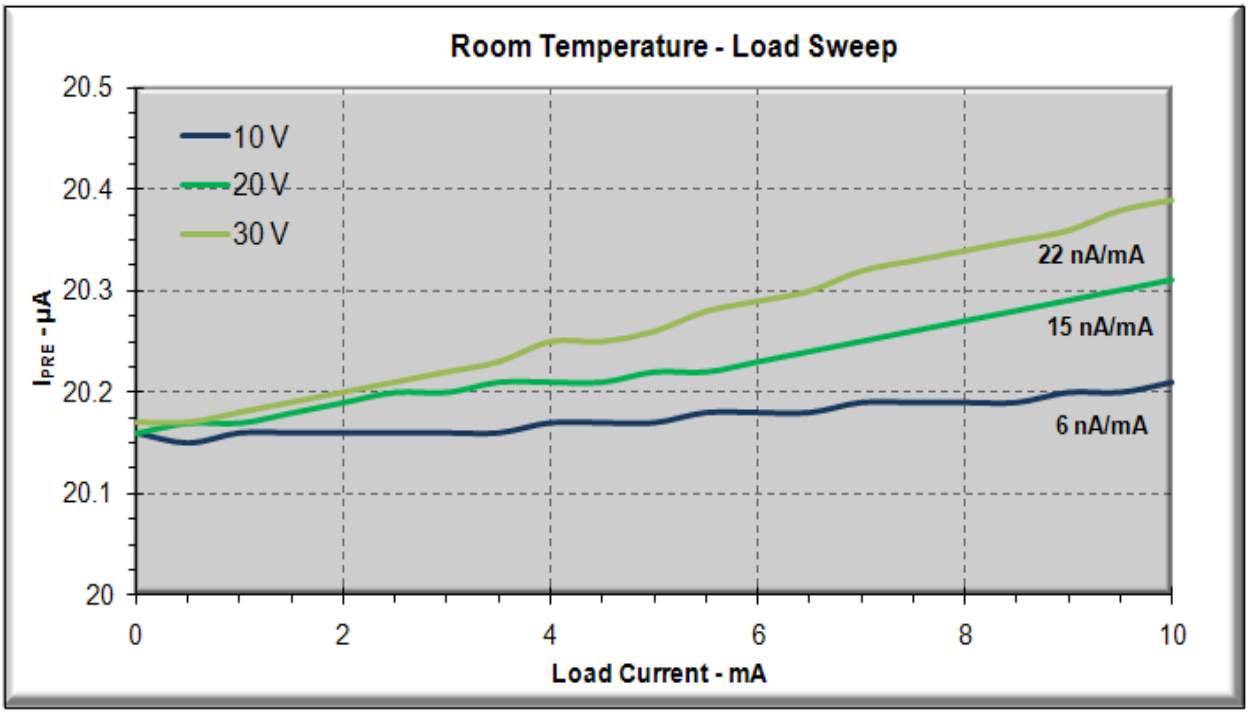

Figure 4.12 – Measured I_{PRE} Load Regulation

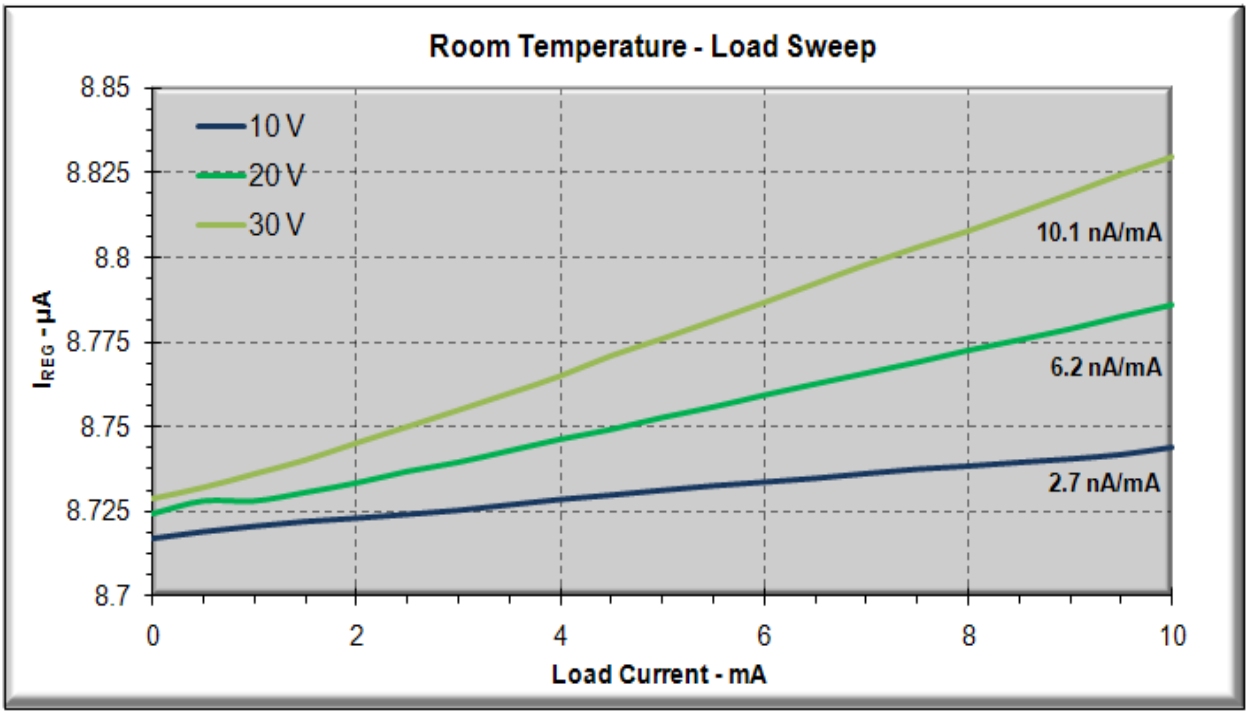

Figure 4.13 – Measured I_{REG} Load Regulation

4.5 – Temperature Characteristic

The voltage regulator is tested in a Delta Design 9023 Environments Chamber over a temperature range of −50 ºC to 200 ºC with a sample taken every 25 ºC. Figures 4.14-4.19 show the temperature characteristics of V_{DD}, V_{PRE}, V_{REF}, I_{PRE}, I_{REG}, and I_{SUPPLY} with 10-V, 20-V and 30-V input voltages and no load and 10-mA load conditions. Under no load, the output voltage exhibits a nearly uniform, parabolic relationship to temperature while varying only a few mV over the 250 ºC range (Figure 4.14). Supply voltage variation from 10-30 V reveals no discernable effect on the temperature characteristic of V_{DD}. Under a 10-mA load condition, a similar parabolic relationship is observable but with a less uniform correlation. The effects of temperature on R_{DS} cause an increased drop in V_{DD} as temperature increases. This effect is due to the proportional relationship of R_{DS} to temperature. In spite of the temperature effect on R_{DS}, the total variation of V_{DD} over a 250 ºC temperature sweep remains modest for either load condition. Supply voltage variation effects on V_{DD} with a 10-mA load display an inverse relationship to temperature; however, the effect is small. V_{PRE} relationship to temperature is demonstrated in Figure 4.15. The temperature coefficients of MOSFET threshold voltages and

poly2 resistivity combine to form this temperature dependence. A load condition results in a very small decrease in pre-regulator voltage, which is consistent across temperature. The proximity effect as V_{DDH} approaches V_{PRE} observed in simulations presents in measurement results as well. The temperature characteristic exhibited in Figure 4.15 differs from the simulation results due to modeling inaccuracies (likely the high-voltage LDMOS devices). At all temperatures, supply conditions, and load conditions the pre-regulator voltage remains well above the turn-on voltage required by the regulator circuits. Figure 4.16 reveals a decaying reference voltage in response to increasing temperature. The magnitude of the simulated V_{REF} temperature coefficient differs from the temperature characteristic found in measurement results. Once again, model inaccuracies are the most probable cause of the discrepancy. Load condition and supply voltage have minimal effects on V_{REF} temperature characteristic. Despite deviation from simulated results, V_{REF} is well-bounded over temperature and will allow for accurate voltage regulation. I_{PRE} and I_{REG} (Figures 4.16 and 4.17, respectively) respond to temperature changes as predicted by the simulations. The voltage regulator provides an overall temperature characteristic that out performs most comparable commercially-available voltage regulators.

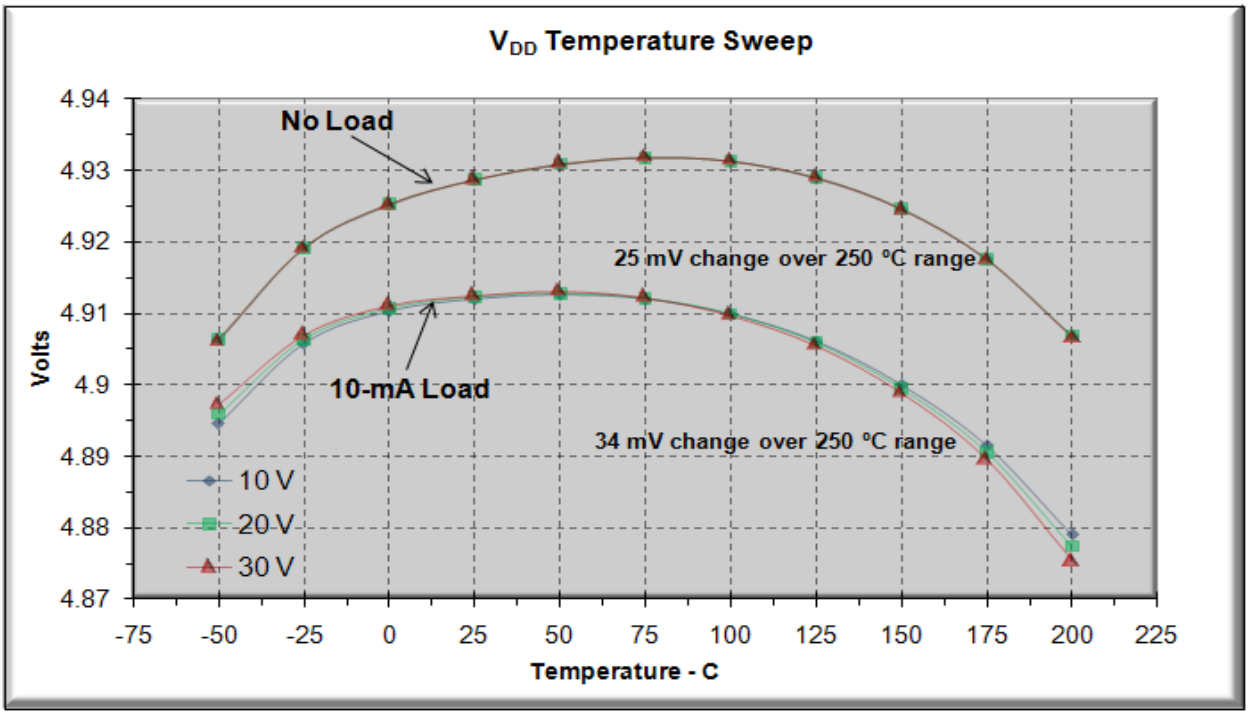

Figure 4.14 – Measured V_{DD} Temperature Characteristic

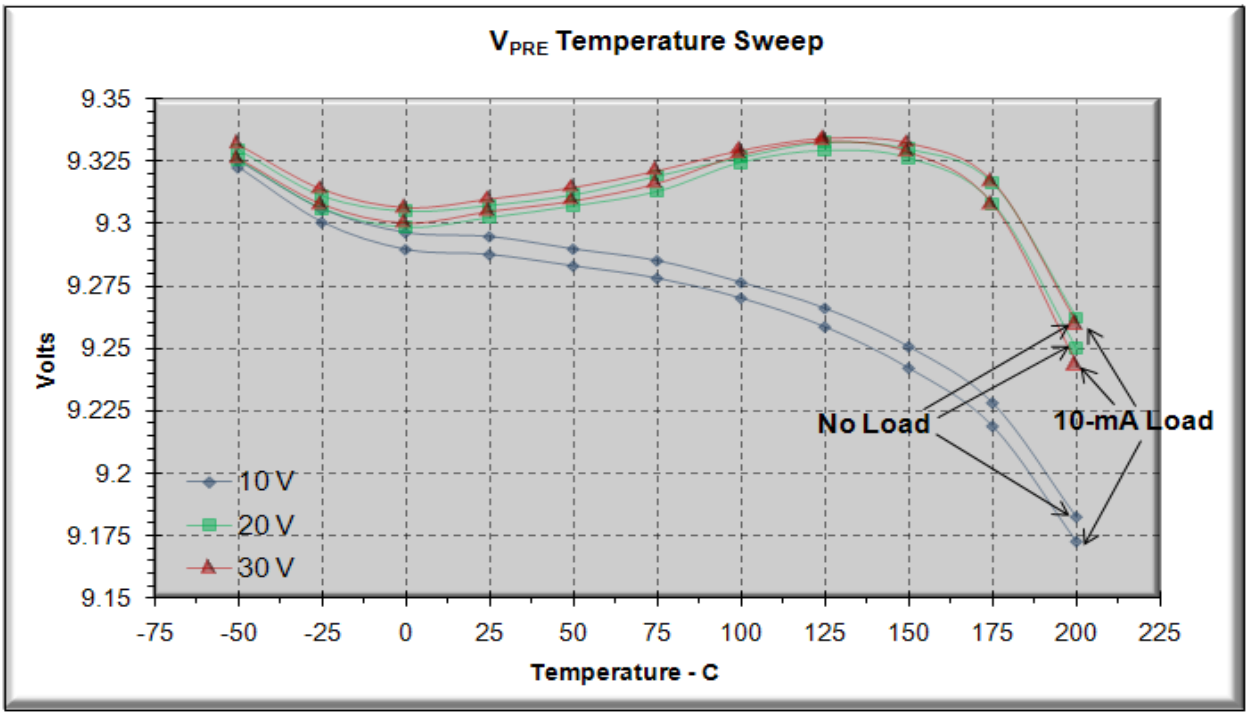

Figure 4.15 – Measured V_{PRE} Temperature Characteristic

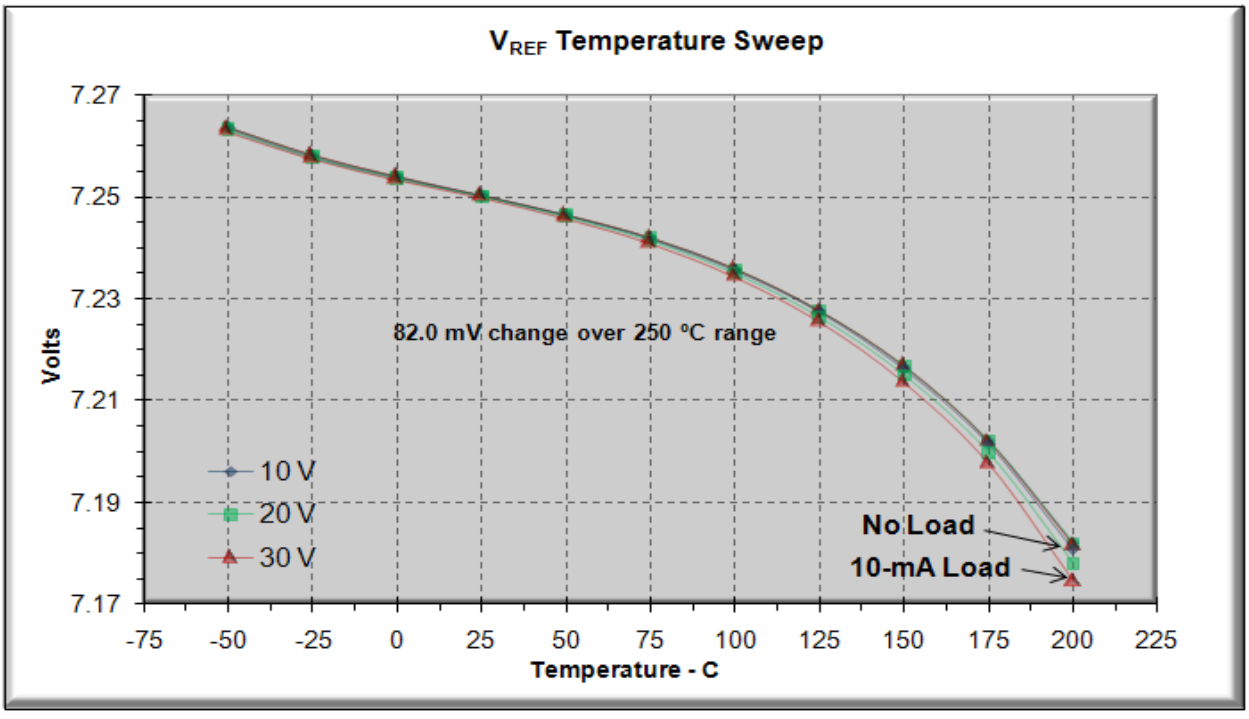

Figure 4.16 – Measured V_{REF} Temperature Characteristic

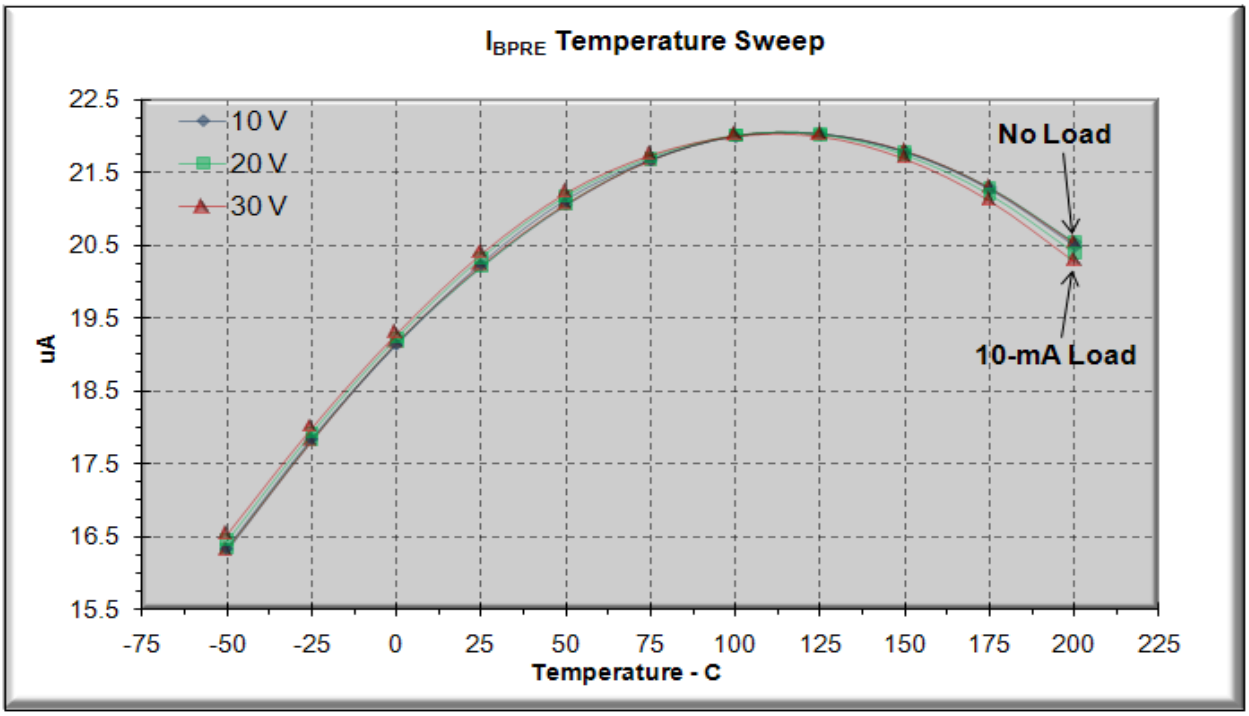

Figure 4.17 – Measured I_{PRE} Temperature Characteristic

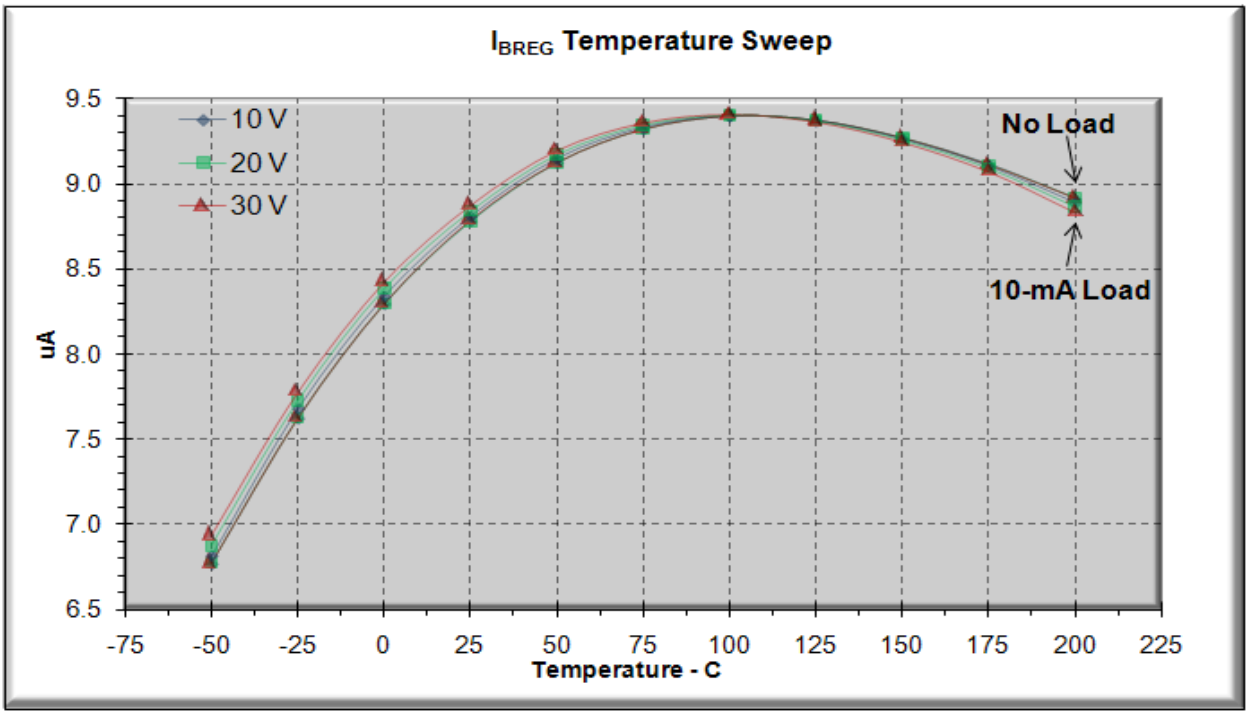

Figure 4.18 – Measured I_{REG} Temperature Characteristic

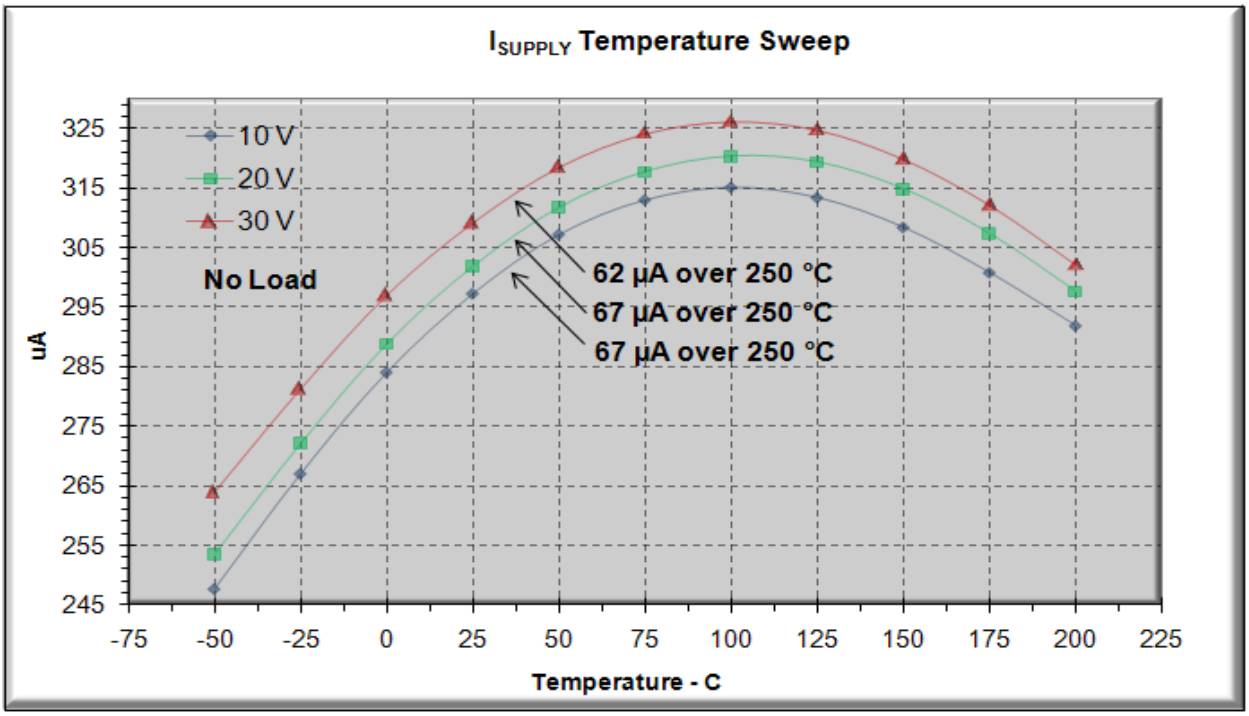

Figure 4.19 – Measured I_{SUPPLY} Temperature Characteristic

4.6 – Load Transient

Load transient tests are performed at −50 °C, 25 °C, and 200 °C with a supply voltage of 20 V. The test set-up for the load transient tests can be seen in Figure 4.20. The load current is obtained by measuring the voltage across the 5-Ω resistor and using Ohm's law. The switching signal v_{pulse} is sourced using an Agilent 33250A waveform generator. An Aglient 54624A oscilloscope is used to capture the various signals. Using the pulse signal described, the load current generated exhibits a 70-nsec rise time and a 60-nsec fall time. These transient times are limited by the speed of the 2N3904 current sink device. As in load transient simulations, a ceramic NP0 load capacitor of 3.8 µF is used as a charge storage device. Parasitic inductance and resistance present in the signal path from the signal routing on chip to the instruments inputs degrade the measureable transient response. Signals probed at different points along the signal path displayed drastic differences in transient response. The transient data obtained best represents the actual transient response; however, improved data may be attainable with packaging, PCB board, and test set-up modifications.

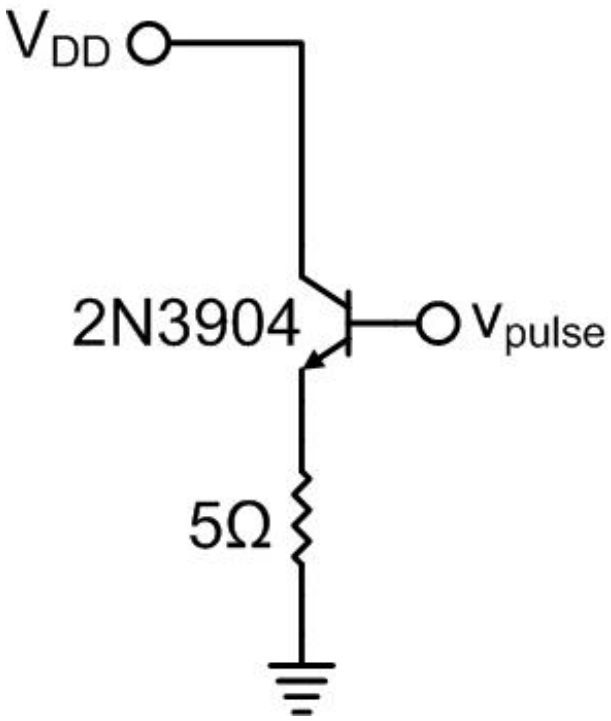

Figure 4.20 – Load Transient Test Set-Up

The results of the load transient test for −50 °C, 25 °C, and 200 °C are illustrated in Figures 4.21-4.23, respectively. For all temperatures, the total displacement of V_{DD} is about 50 mV during the load transient. The peak-to-peak V_{DD} load transient response decreases as temperature increases (consistent with simulation). V_{DD} settles to its nominal value within 2.5 µsec. This observed settling time decreases with temperature. Small ripple voltages are visible on V_{PRE} and V_{REF} at the edges of the transient load. These ripple voltages are on the order of a few $mV_{p\text{-}p}$ and have settling times of a few µsec as exhibited in the respective figures. These disturbances settle relatively quickly and do not cause voltage regulator stability issues. The transient load is coupled through various devices within the voltage regulator, but the main coupling path is through the NMOS pass device. The large width of this device implies large parasitic capacitances, which couple AC signals through the voltage regulator. These effects are not detrimental to the voltage regulator performance and are expected in reaction to such a large load transient. Subtle changes in the load transient responses of V_{PRE} and V_{REF} can be seen for different temperatures. The measured load transient results differ slightly from the simulation results due to model inaccuracies (mainly the high-voltage LDMOS devices). In spite of this short coming, the voltage regulator performs admirably in the presence of a load transient.

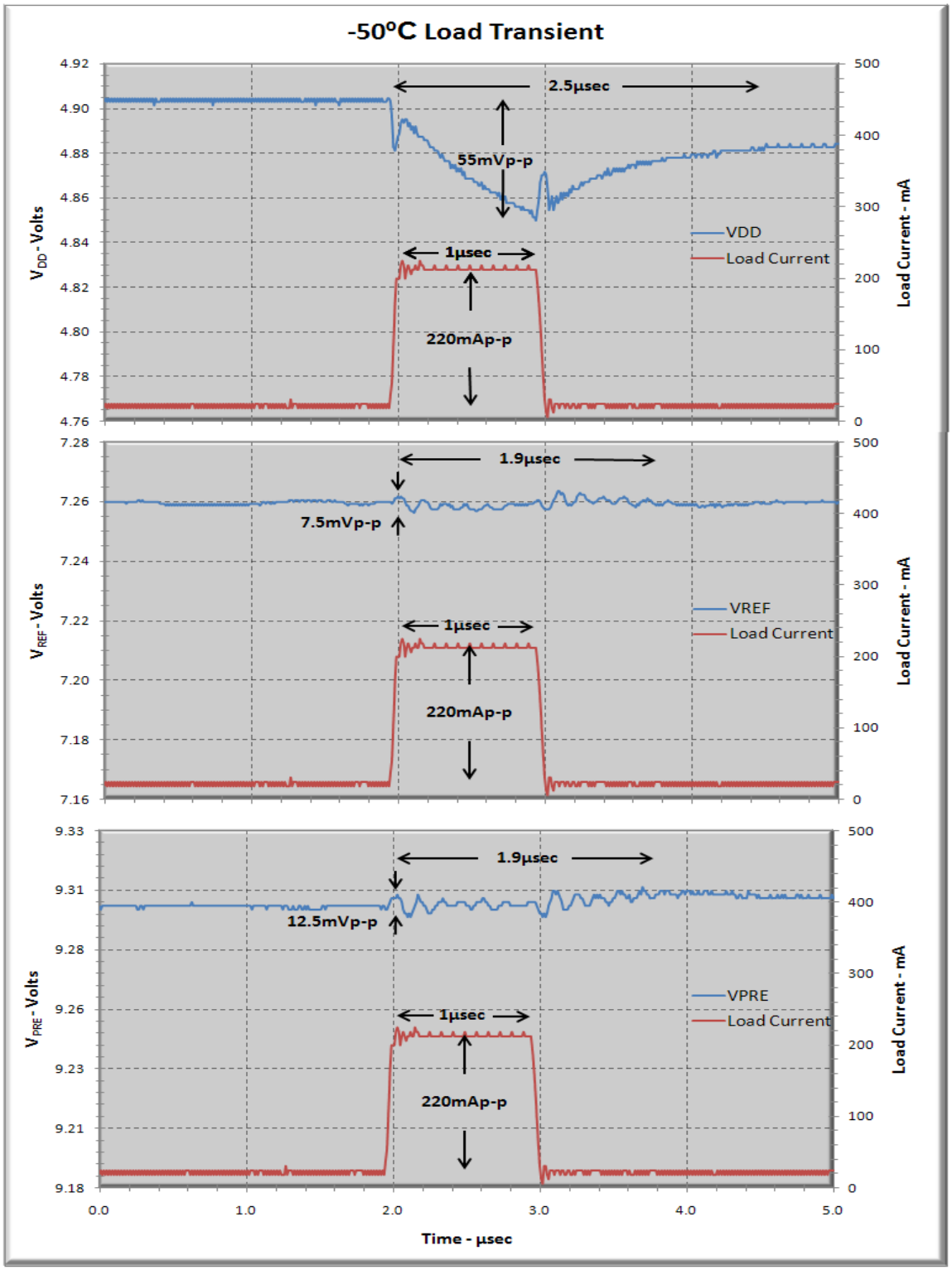

Figure 4.21 – Measured −50 °C Load Transient

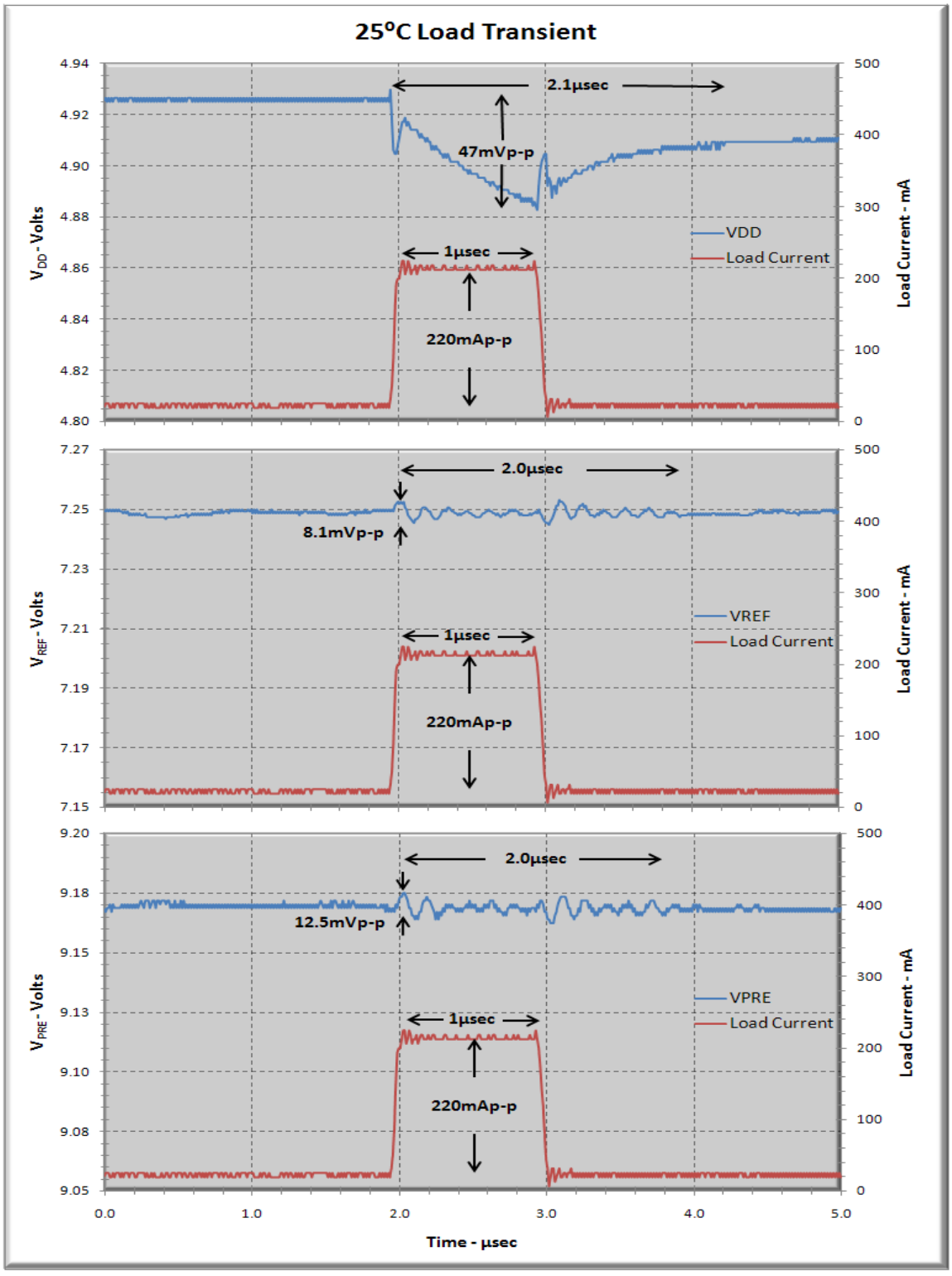

Figure 4.22 – Measured 25 °C Load Transient

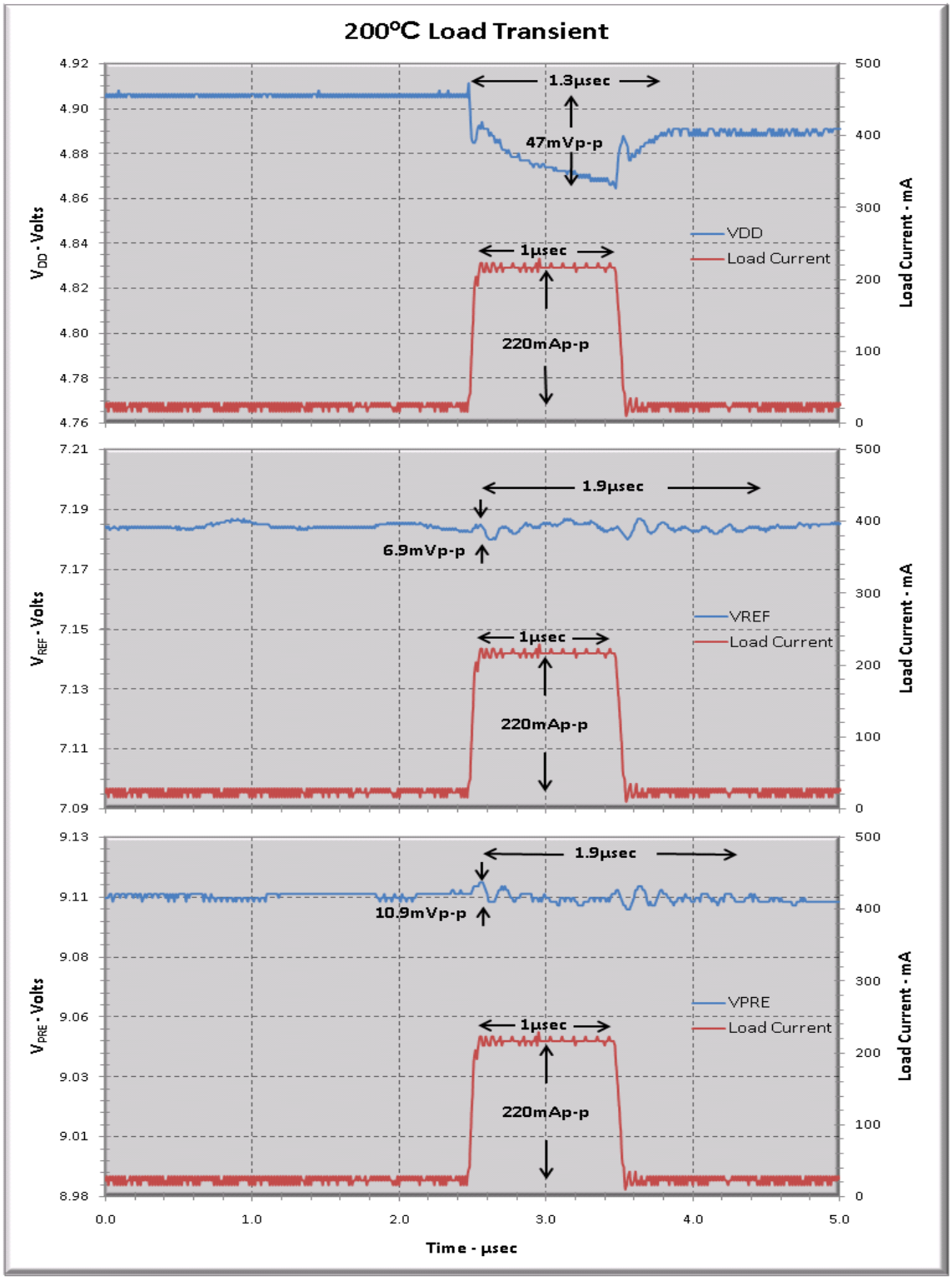

Figure 4.23 – Measured 200 °C Load Transient

4.7 – Line Transient

Measured line transient testing is performed using a DC voltage source in series with an AC pulse generator (Figure 4.24). An Agilent 33250A is used to provide the pulse voltage, while an Aglient 54624A oscilloscope is used to capture the various signals. The pulse voltage (v_{pulse}) is displayed in Figure 4.25. The pulse voltage is set to 5 Vp-p with a 5-nsec rise time. This test condition greatly exceeds input voltage transients encountered in the gate driver application. This transient supply voltage injects high frequency signals (the edges of the pulse signal) into the voltage regulator. These high frequency signals are coupled through various parasitic capacitors throughout the voltage regulator and are examined at each node in the voltage regulator. The pre-regulator greatly attenuates the line transient imposed on the subsequent voltage regulator circuits (another advantage to implementing the voltage regulator with a pre-regulator circuit). The output capacitor also attenuates the propagated transient signal. As with the load transient test, the accuracy of the measured line transient responses is limited by the parasitic inductance and resistance presented at various points along the signal path.

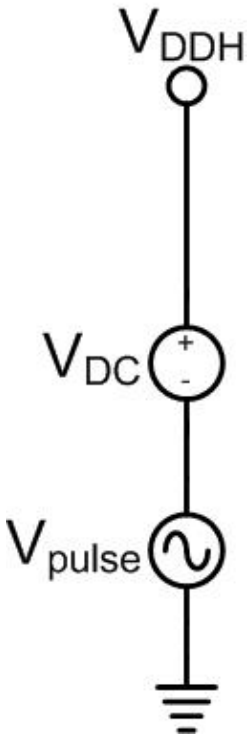

Figure 4.24 – Line Transient Test Set-Up

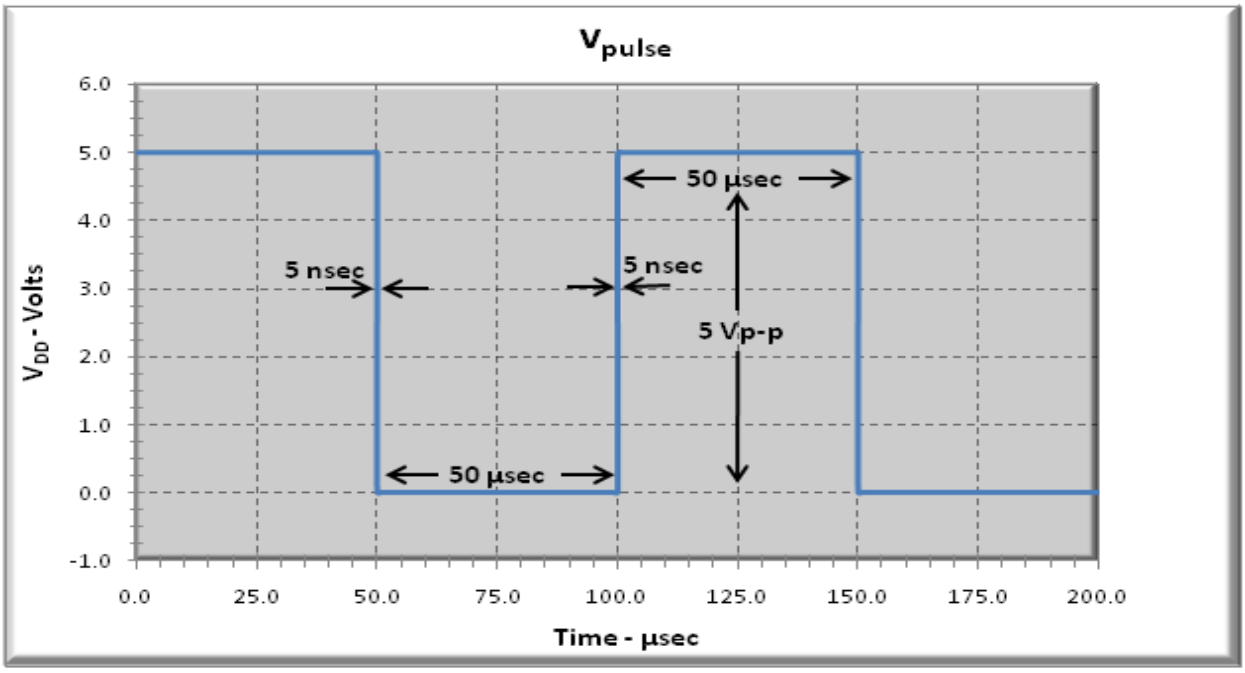

Figure 4.25 – v_{pulse} Line Transient Signal

The voltage regulator line transient responses can be observed in Figures 4.26-4.28. V_{DD} varies less than 1 mV during a rising edge transient and does not respond to a falling edge transient (consistent with simulation results). The observed displacement in V_{DD} increases with temperature but remains quite low even for a large line transient. V_{REF} shows a transient response at both rising and falling edges of the line transient, but the rising edge response is more pronounced. This transient response in V_{REF} exhibits narrow pulse widths due to the feedback loop in the reference generator circuit. The amplitude of the V_{REF} transient response has a parabolic relationship as function of temperature, but only minor differences arise at different temperatures. V_{PRE} responds to line transients with a proportional voltage step followed by an exponential decay back to the nominal voltage level. The amplitudes and settling times of V_{PRE} transient response is proportional to temperature. The exponential decay found in V_{PRE} is attributed to the parasitic capacitances of the two large current source PMOS devices (*M13* and *M14*). The pre-regulator greatly improves the voltage regulators ability to reject line transients. Even large line transients do not pose a significant threat to voltage regulator performance as long as the line voltage remains within the input voltage range of the voltage regulator. Measurement results correlate well to simulation results with only small amplitude and time constant variations.

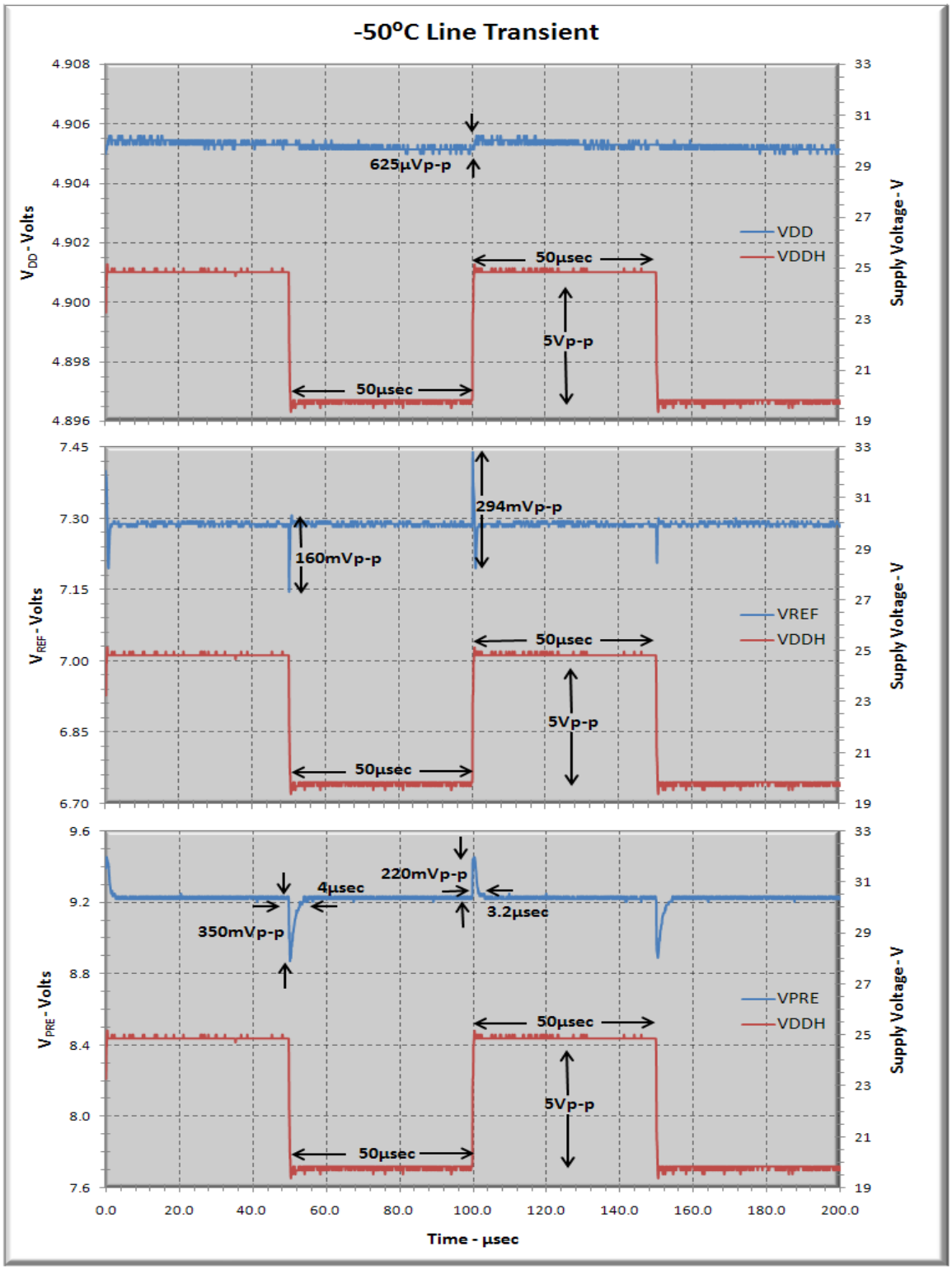

Figure 4.26 – Measured −50 °C Line Transient

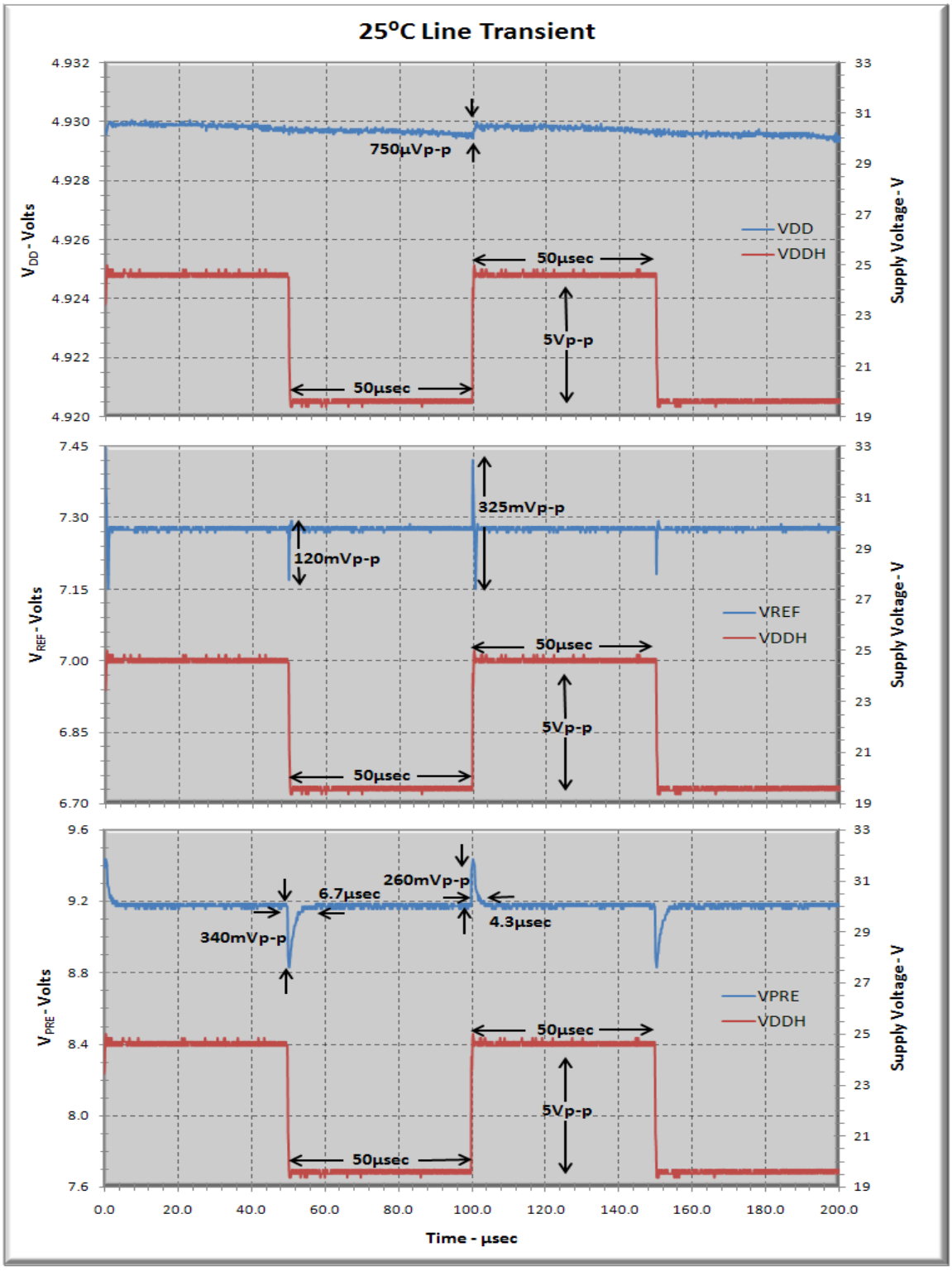

Figure 4.27 – Measured 25 °C Line Transient

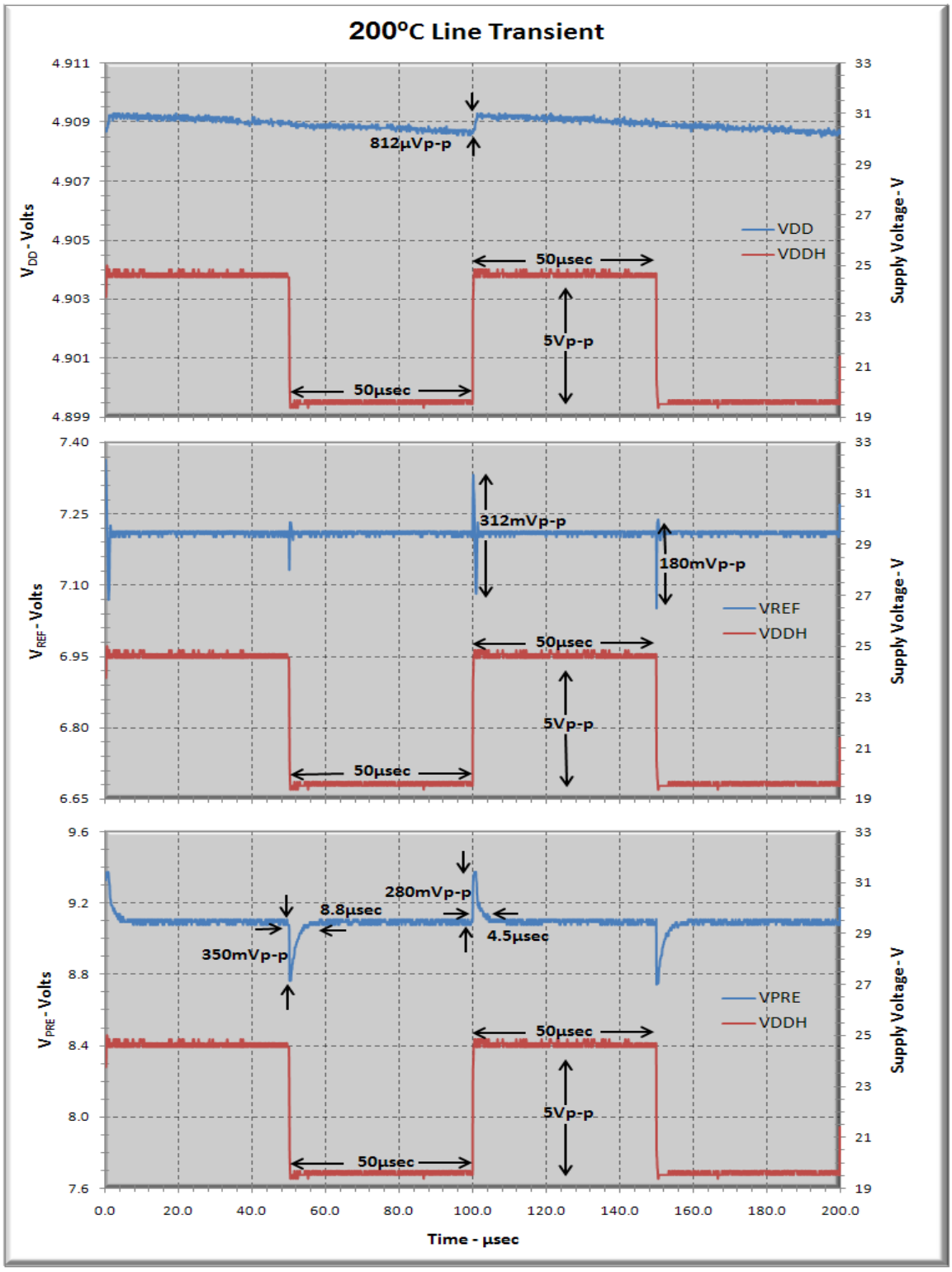

Figure 4.28 – Measured 200 °C Line Transient

5. Conclusion

5.1– Thesis Summary

All of the design challenges associated with the high-voltage, high-temperature gate driver project are met by modifying the existing LM723 design. The LM723 is a well-designed, well-tested topology that serves as a strong base for voltage regulator design. The commercially-available, 0.8-micron SOI process greatly enhances the robustness of the design, but the trench isolation of individual devices produces its own unique design challenges (mainly device matching). Device modeling inaccuracies in this process result in simulation vs. measurement discrepancies. By over-designing the voltage regulator, these discrepancies did not significantly detract from the voltage regulator functionality. Overall, the designed voltage regulator performs well over all specified operating conditions. The most pronounced inaccuracy of the voltage regulator is the nominal 70-mV deviation from simulated V_{DD} voltage. Offset voltage imposed by the inability to match trench isolated devices contributes to this offset. Also, BJT base currents can result in offset as these currents induce voltage drops on the input and feedback voltages of the op-amp differential pair. In spite of these model inconsistencies, the overall performance of the voltage regulator meets or exceeds the demands of gate driver and many other high-temperature applications. The temperature performance of the designed voltage regulator exceeds that of other LM723 based designs. Also, largely due to the implementation of the pre-regulator, the line rejection of the designed voltage regulator (both DC and transient conditions) greatly exceeds most commercial voltage regulators. Load regulation is adequate for most applications (up to 200 mA) but can be improved in future designs.

5.2– Future Work

Future design revisions of this voltage regulator will take advantage of the model information discovered in testing this regulator design and testing of individual devices. One potential modification to this votlage regulator is implementing a BJT-based output stage as opposed to the current LDMOS output stage. The BJT output stage could significantly improve the load regulation and temperature performance. To successfully implement the BJT output stage, the closed-base breakdown voltages of the BJT devices will need to be tested to unsure long term reliability. Modifying the output stage could also result in increased load current capabilities

which would expand the applications of this voltage regulator. An effort will also be made to remove the need for an external output capacitor. Increasing the bandwidth (at the expense of DC gain) and modifying compensation techniques could potentially reduce the need for an output capacitor. Temperature compensation may also be modified as device testing improves simulation accuracy. Due to the limited pin count available and the high demand for pins in this gate driver generation, test points for the voltage regulator are limited. Additional voltage regulator information would be available if future design were capable of allocating more pins for the voltage regulator circuit.

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Vita

Benjamin Matthew McCue was born in Oak Ridge, TN on September 6th, 1983. He graduated from Karns High School in Knoxville, TN in 2001. Benjamin entered the Engineering School at the University of Tennessee in August of 2002 with a goal of obtaining a B.S. in Electrical Engineering. During his junior year in the electrical engineering program, he interned at the Electric Power Research Institute in Knoxville, Tennessee. As a senior, Benjamin began working for Dr. Benjamin Blalock as a research assistant for the Integrated Circuits and Systems Laboratory (ICASL) research group at the University of Tennessee. It was during this time that he realized he wanted to pursue graduate school to enhance his understanding of his field and widen future career possibilities. In the summer of 2007, Benjamin entered the Masters of Science program at the University of Tennessee. During his work toward achieving a Master's of Science degree, he continued work as a research assistant in the ICASL research group under the instruction of Dr. Blalock. During this time, he worked on several projects including the gate driver project funded by the Oak Ridge National Laboratories (ORNL). After conferral of his Master's degree, Benjamin will continue his education in the pursuit of a Ph.D. degree at the University of Tennessee. During this endeavor, he will continue work as a research assistant for Dr. Blalock in the ICASL research group.