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# Design of A Low-power Precision Op Amp with Ping-pong Autozero Architecture

Pengfei Xi

*University of Tennessee - Knoxville*

To the Graduate Council:

I am submitting herewith a thesis written by Pengfei Xi entitled "Design of A Low-power Precision Op Amp with Ping-pong Autozero Architecture." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Benjamin Blalock, Major Professor

We have read this thesis and recommend its acceptance:

Syed Islam, Ethan Farquhar

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# DESIGN OF A LOW-POWER PRECISION OP AMP WITH PING-PONG AUTOZERO ARCHITECTURE

A Thesis

Presented for the

Master of Science

Degree

The University of Tennessee, Knoxville

Pengfei Xi

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Finally, I would like to thank my family and friends who have been always supportive.

# ABSTRACT

Precision op amps are widely used in instrumentation, automotive, and industrial applications. This thesis presents the design and characterization of a low-power precision operational amplifier that uses “ping-pong” autozero architecture for automatic offset correction. The op amp is designed for extreme environment applications, operating across a wide temperature range (minus 180 degree Celsius to plus 120 degree Celsius) with low offset, low drift and low power consumption. This design has been fabricated in a SiGe BiCMOS 0.5-micron process and the measured results demonstrate that the op amp is fully functional and achieves less than 40 microvolt input-referred offset voltage with 0.1 microvolt per degree offset voltage drift and 1 microwatt power consumption.

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# CHAPTER 1 INTRODUCTION

## 1.1 Introduction

The operational amplifier (op amp) fills a fundamental role in analog and mixed-signal integrated circuits and systems. Precision op amps are typically defined as op amps with low offset voltage and low offset voltage drift across temperature. Originally precision op amps were used in instrumentation applications where test circuits and systems needed much more precision than conventional ones. Nowadays, they are widely used in automotive and industrial applications as well.

## 1.2 Motivation

In National Aeronautics and Space Administration (NASA) Cryogenic project, a precision op amp is needed for sensor interface application in extreme environments. The wide temperature range that the circuit in the extreme environments of space may be exposed to requires this design operate consistently over temperature. The highlighted target design parameters are less than 50 μV offset voltage, 0.1 μV/°C offset voltage drift, and 1 mW power consumption.

In real life, circuits are not perfect. There are a few of causes of offset voltage, including input transistor mismatch, current mirror inaccuracies, resistor mismatch, differences in the doping of the input pair, and radiation. Usually offset voltage values of regular CMOS op amps are in the range of ±10 mV to ±30 mV. Moreover, regular op amps are

not able to work consistently over wide temperature range because transistor parameters change over temperature.

As a result, it is very difficult to design a general op amp to fit extreme environment applications. This thesis presents the design and characterization of a precision operational amplifier that uses ping-pong autozero architecture [1] [2] for automatic offset correction.

## 1.3 Organization of thesis

Chapter 2 outlines circuits techniques used to reduce offset voltage. In Chapter 3, detailed circuit design of the ping-pong autozero op amp is presented. Chapter 4 gives the measured results for the op amp and Chapter 5 presents conclusions as well as discussion on future work.

# CHAPTER 2 TECHNIQUES TO REDUCE OP AMP OFFSET

For precision op amp design, generally there are two major techniques used to reduce the offset and low-frequency noise, namely the chopper and the autozero techniques.

## 2.1 Chopper Technique

Chopper amplifiers [1] were introduced decades ago to eliminate op amp's imperfections. The basic idea of choppering is to apply modulation to or low-frequency input signals, thus frequency translating them to higher-frequency for amplification, and then down-converting them back to low-frequency after amplification, hence offset is reduced in baseband. First amplifiers using choppering had limited bandwidth. To solve the bandwidth problem, then chopper-stabilized technique was invented by using the chopper amplifier to stabilize a conventional wideband amplifier that remained in the signal path. One disadvantage of it is it could only do inverting signal gain amplifying. Nowadays chopper amplifiers employ autozero technique [1], and the stabilizing amplifier signals are connected to the main amplifier through an additional input for autozeroing use, not one of the differential inputs as in previous implementations. This change makes chopper amplifiers not limited to low-frequency applications.

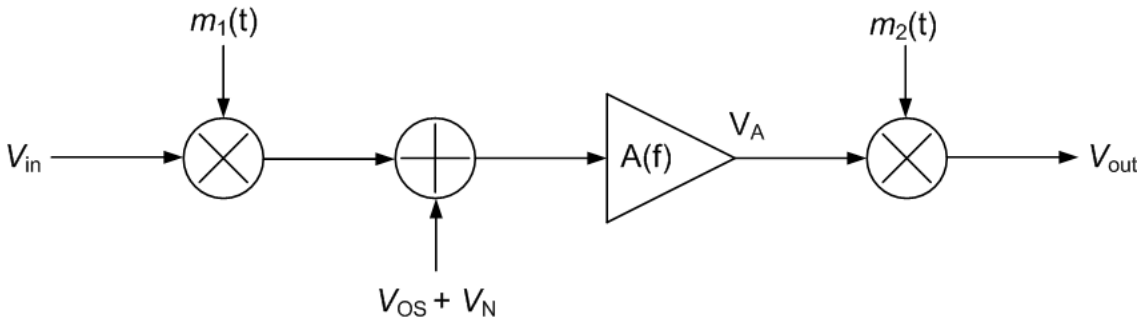


Figure 2.1 Principle of chopper stabilization technique [1]

The principle is illustrated in Fig. 2.1. It modulates the input signal to a higher frequency where there is no 1/f noise and dc offset and then demodulates it back to the baseband after amplification [1].

In the discrete time system shown in Fig. 2.1, $V_{in}$ is the input signal, which will be modulated by the square-wave carrier signal $m_1(t)$. $V_{OS}$ is offset voltage, and $V_n$ is noise of the op amp. Here assume the amplifier itself is ideal without any offset or noise. After being amplified, the modulated signal will be demodulated back to low frequency, and ideally it is $A_oV_{in}$. To achieve this, the amplifier needs to have infinite bandwidth with no delay. Moreover, the phase shift between the modulator and demodulator needs to match the phase shift of the amplifier in the chopper system. Also note that the input signal frequency should be less than half of the chopper frequency to avoid signal aliasing, thus limiting the applications of chopper op amps.

## 2.2 Autozero Technique

The autozero technique samples the offset at the output and then uses a negative feedback network to an auxiliary input port to cancel the original offset [1]. As shown in Fig. 2.2, by shorting two positive and negative inputs we have $V_{out} = A_o V_{os}$, where $V_{os}$ is input-referred offset voltage, $V_{out}$ is the output voltage, and $A_o$ is the dc open-loop gain of the op amp. Then, the sample-and-hold circuit samples the output voltage and feeds back this value to the input port for cancellation.

Since autozero technique needs to feed back offset voltage at output to reduce the input offset voltage and noise, usually there are two phases to realize: sampling and amplifying. In sampling phase, the input terminals are shorted, so the amplifier is disconnected from the signals and not for amplification use. The input differential voltage is just the dc offset voltage, $V_{os}$, and the amplifier will amplify this value, so the output voltage will be set to $A_o V_{os}$. The sample-and-hold block samples this voltage, and then stores it on a capacitor. In amplifying phase, input terminals of the amplifier are connected to signals for signal processing, and the stored voltage $A_o V_{os}$ on the capacitor is put into the amplifier's auxiliary input pair to cancel the offset voltage. As a result, the amplifier works as an ideal amplifier without offset if it is under the same conditions as during sampling phase.

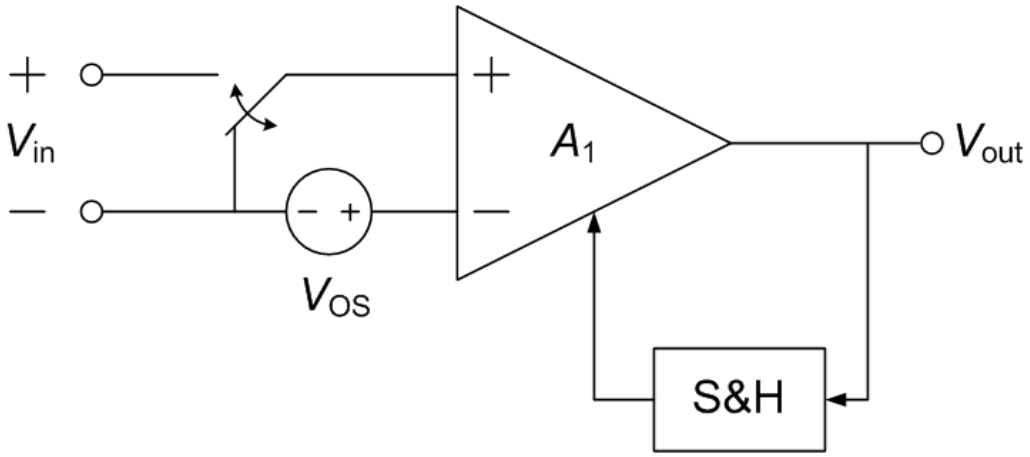


Figure 2.2 Basic principle of autozero technique [1]

## 2.3 Autozero with Ping-Pong Architecture

Generally an autozero amplifier is a discrete-time system as the one shown in Fig. 2.2 because the amplifier is unavailable for processing signals during the sampling phase. This prohibits that type of autozero amplifier from being used in continuous-time applications.

To solve this problem, the ping-pong autozero op amp was proposed, which consists of two identical amplifiers in parallel and switch networks for controlling their use in the signal path, as shown in Fig 2.3 [2] [3]. When $A_1$ is amplifying signals, $A_2$ is autozeroing. The two amplifiers switch back and forth, so the op amp as a whole can work continuously, hence the name 'ping-pong.'

During offset sampling period as shown in Fig. 2.4, two input terminals are shorted and there is a sampled voltage fed back to the auxiliary input while the other auxiliary input terminal is connected to a reference voltage. Applying Kirchhoff's voltage law,

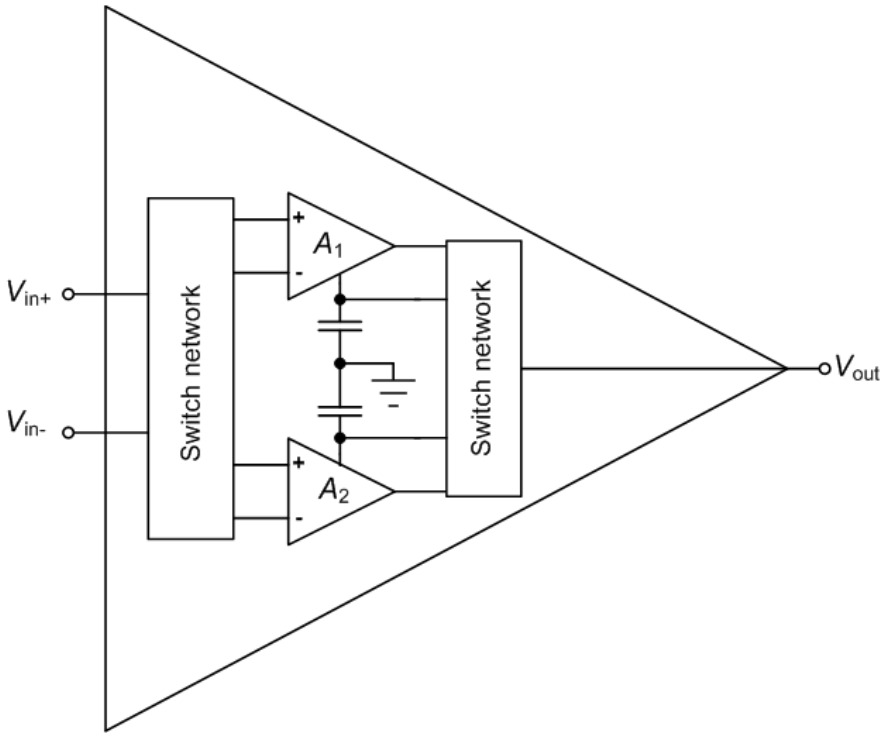


Figure 2.3 Block diagram of ping-pong autozero amplifier [3]

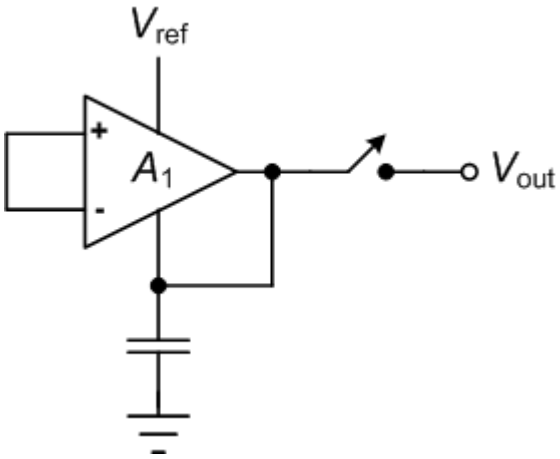


Figure 2.4 Amplifier configuration during sampling phase

$$V_{os1} \times A_1 + (V_{ref} + V_{os2} - V_o) \times A_2 = V_o \tag{2.1}$$

So we have

$$V_o = A_1 V_{in} \tag{2.1}$$

$$V_o = V_{os1} \frac{A_1}{A_2 + 1} + V_{ref} \frac{A_2}{A_2 + 1} + V_{os2} \frac{A_2}{A_2 + 1} \tag{2.3}$$

$A_2$ is the open-loop gain for auxiliary inputs, and usually much greater than 1, so

$$V_o = V_{os1} \frac{A_1}{A_2} + V_{ref} + V_{os2} \tag{2.4}$$

This is the voltage value sampled by the sample-and-hold block and stored on a capacitor for next phase use to cancel the offset. The above equation shows the output voltage consists of $V_{os1}$ and $V_{os2}$ parts, indicating that both the main input pair's and the auxiliary input pair's offset voltage affect this feedback voltage value.

During amplifying phase as shown in Fig. 2.5, the feedback switch is off and the amplifier works as a standard one. By Kirchhoff's voltage law, we have

$$(V_{in} + V_{os1}) \times A_1 + (V_{ref} + V_{os2} - V_{os1} \frac{A_1}{A_2} - V_{ref} - V_{os2}) \times A_2 = V_o \tag{2.5}$$

After simplifying,

$$V_o = A_1 V_{in} \tag{2.6}$$

Equation 2.6 shows the feedback voltage to the negative auxiliary input is put in to cancel the offset, and now $V_o$ is no longer related to $V_{os1}$. From the mathematics, the amplifier works as an offset-free op amp when operating, but it must be under the same conditions

as during sampling phase, which means the feedback value needs to be accurate and maintained over time (as through continued ping-pong action).

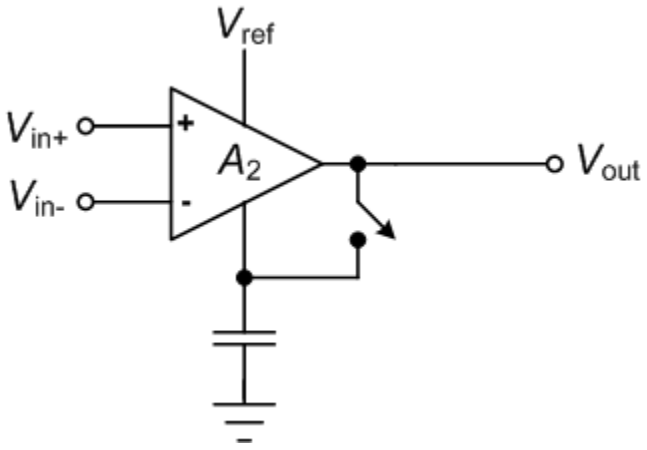


Figure 2.5 Amplifier configuration during signal-processing phase

# CHAPTER 3 CIRCUIT DESIGN OF PING-PONG AUTOZERO OP AMP

## 3.1 Topology of Ping-Pong Autozero Op Amp

A ping-pong autozero op amp mainly includes two identical amplifiers, switch networks, sample-and-hold circuits, a clock generator and switch drivers [2]. Controlled by a two-phase clock, one amplifier is processing signals while the other is canceling its offset.

As shown in Fig. 3.1, the input switch network is controlled by two-phase clock signals and they choose inputs for one amplifier to process. While one amplifier is operating to amplify signals, the other one is cancelling its own offset voltage. The two work back and forth continuously, hence called ‘ping-pong’.

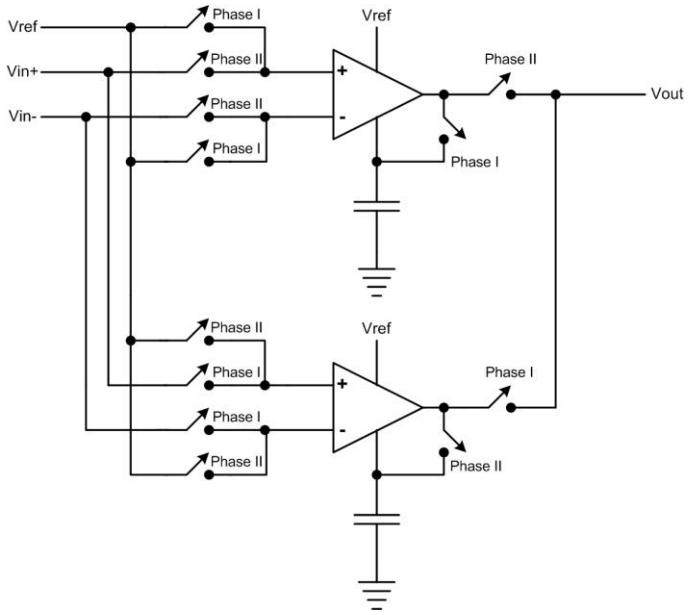


Figure 3.1 Topology of ping-pong antozero op amp

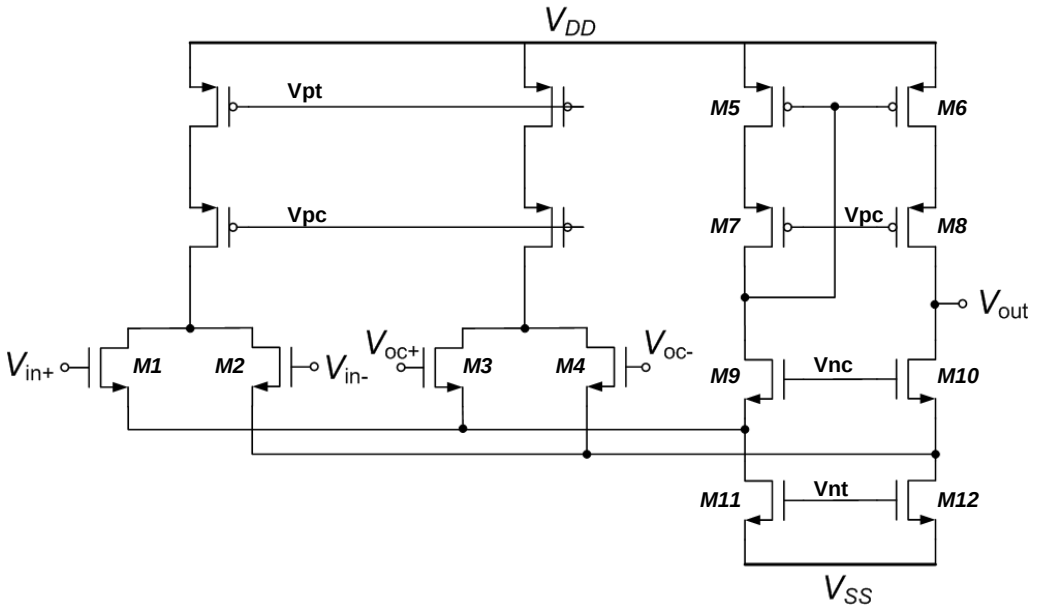


Figure 3.2 First stage schematic

## 3.2 Dual Input Pair Input Stage

For the input stage, a folded-cascode topology is used with PMOS input pair to provide ground sensing capability for the op amp's input common-mode range [2] [4]. As stated in Chapter 2, another input pair is required to amplify the sampled voltage for offset cancellation. In Fig 3.2, the left input pair is the main input pair which is used for signal processing, and the right auxiliary pair is for offset cancellation.

As stated previously, the mathematic equations show the cancellation results do not depend on the offset introduced by the auxiliary input pair. However, in practice the sampling switches are not ideal, so the sampled voltage value is not completely accurate and cannot be maintained with perfect consistency, causing the cancellation to be non-ideal. As a result, the sampled voltage at the output consists partially of $V_{os2}$, the offset

voltage of the second input pair. To minimize the error from $V_{os2}$, the auxiliary input pair must be designed carefully to reduce its input offset. Compared with the main input pair, longer transistor length and width have been chosen in this design to obtain better matching so that the offset is relatively smaller.

## 3.3 Class AB Output Stage

The output stage is a very important part of a two-stage op amp. The design specifications require wide output swing and good power efficiency, so a class AB output stage is chosen to used with the folded-cascode first stage. As shown in Fig. 3.2 it mainly consists of two parts: class-AB output stage, its biasing circuit and compensation capacitors. This class-AB output stage is based on [5], and each amplifier has one this output stage. As shown in Fig. 3.3, $M_{11}$ and $M_{12}$ are two common-source connected transistors forming class AB push-pull output stage, which are biased by $M_1$ and $M_2$ that form a "floating current source." $M_5$ and $M_6$ bias the gate of $M_1$, and $M_9$ and $M_{10}$ bias the gate of $M_2$. $M_1 - M_2$, $M_5 - M_6$, $M_9 - M_{10}$, and the output transistors $M_{11} - M_{12}$ establish two loops: $M_1$, $M_5$, $M_6$, $M_{11}$, and $M_2$, $M_9$, $M_{10}$, $M_{12}$ [5]. These two loops set the quiescent current for the output transistors. The voltage between the gates of output transistors, $M_{11}$ and $M_{12,}$ are kept constant. $C_1$ and $C_2$ are Miller capacitors for frequency compensation.

## 3.4 Current Reference Circuit

An on-chip current reference as in Fig. 3.4 is used to provide bias current for amplifiers in this design. Since this design is intended for wide temperature operation, a well-established bias current is critical to guarantee the performance over temperature.

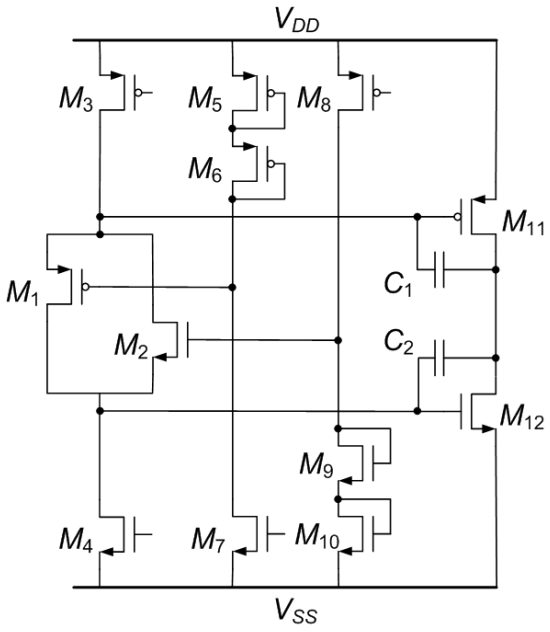


Figure 3.3 Floating control class-AB output stage

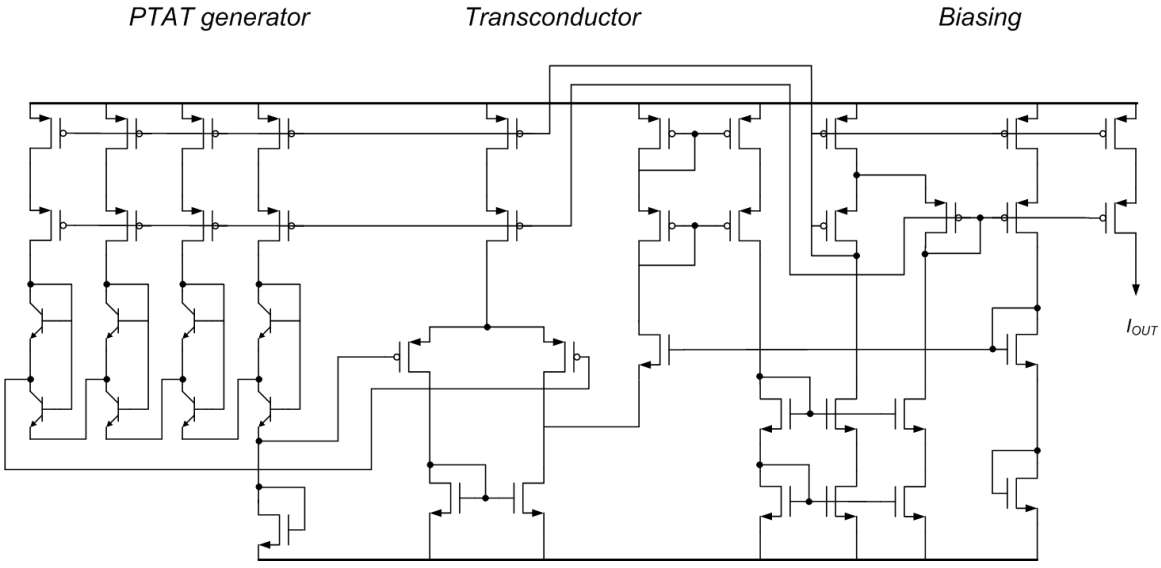


Figure 3.4 Schematic of current reference circuit [6]

There are three parts: a proportional-to-absolute temperature (PTAT) voltage generator, a transconductor and biasing circuit [6]. The transconductor converts the PTAT voltage into an output current that is replicated, providing a current copy that is fed back to bias the transconductor itself. Using this feedback scheme, the reference circuit's output current temperature exponent is around 0.5. Consequently, a constant level of inversion can maintained *over temperature* in critical MOSFET devices of the amplifiers biased by this unique circuit. This is important since analog CMOS design optimization requires careful selection of MOSFET level of inversion [7]. In addition, using this type of current reference circuit for biasing the op amp provides an optimal tradeoff between small-signal and large-signal amplifier performance over temperature [8].

## 3.5 Voltage Bias Circuit

A bias circuit was developed based on the Minch cascode circuit [9]. As shown in Fig. 3.5, $V_{nt}$ and $V_{nc}$ bias the NMOS cascode of the input stage, and $V_{pc}$ and $V_{pt}$ bias the PMOS cascode.

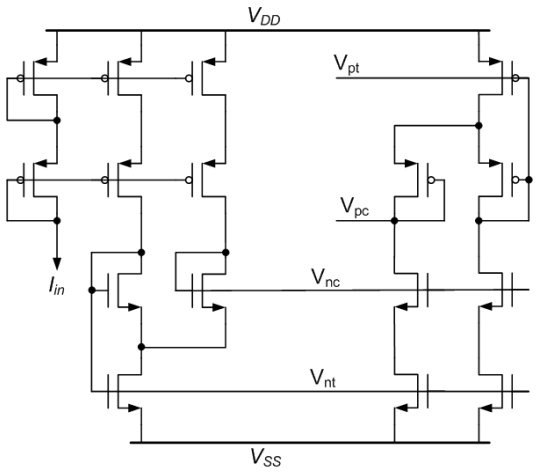


Figure 3.5 Biasing circuit

## 3.6 Two-phase Non-overlapping Clock Generator

The ping-pong autozero op amp operates on a two-phase, non-overlapping clock. Fig. 3.6 shows a clock generator circuit modified from a conventional version [10] to provide the clocks needed. An external 50% duty cycle clock drives the input of this clock generator.

Fig. 3.7 shows the timing diagrams of the two-phase non-overlapping clock used for switches that control the operation of the two amplifiers inside the ping-pong architecture to work back and forth.

## 3.7 Sampling Switches

As mentioned in previous chapter, in the signal-processing phase the amplifier works as offset-free if under the same conditions as during sampling. This makes sampling switches very critical for precision op amp design to approach ideal offset cancellation. Assume that the amplifier has an offset $V_{os1}$, and the canceling algorithm will reduce this offset value close to zero. However, when the sampling has completed, the voltage on the capacitor is stored. Since the switches are not ideal, they will introduce some error due to undesirable effects that will now be discussed.

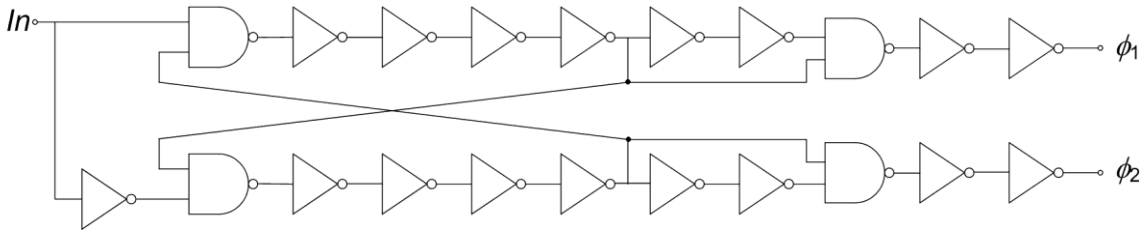


Figure 3.6 Non-overlapping clock generator block diagram [10]

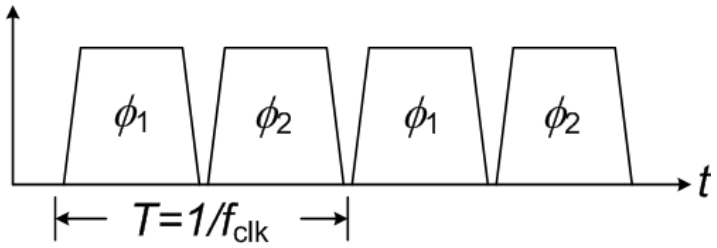


Figure 3.7 Timing diagram

In CMOS technology, the simplest sampling circuit consists of a single MOS device switch and a capacitor as in Fig. 3.8 [11]. While $V_{clk}$ is high the NMOS transistor is on and works as an active resistor, so output $V_{out}$ tracks the input signal $V_{in}$. While clock signal is low the transistor is off, so the output is disconnected from input signal and the signal $V_{out}$ is held on capacitor $C_h$.

There are precision considerations to this simple sampling circuit. One is charge injection effect [11] [12]. When the MOS switch is on, there is a channel at the oxide-silicon interface, and the total channel charge in the inversion layer is given by [11]

$$Q_{ch} = WLC_{ox}(V_{DD} - V_{in} - V_{th}) \tag{3.1}$$

As shown in Fig. 3.9, when the transistor turns off, $Q_{ch}$ is injected onto the capacitor and into $V_{in}$, this effect is called “charge injection” [11].

The charge injected to the input causes no error because a low-impedance voltage source is assumed to be used. However, the other portion of charge is injected onto the capacitor, thus resulting in an error voltage across it.

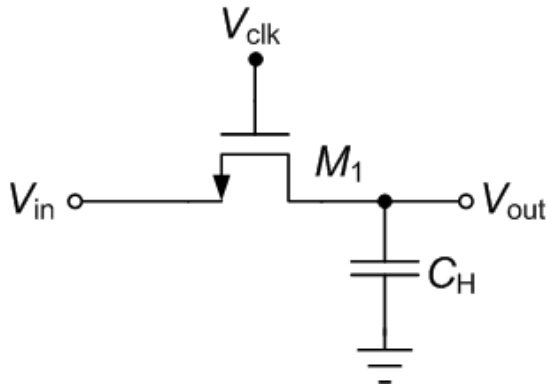


Figure 3.8 Simple sampling circuit schematic

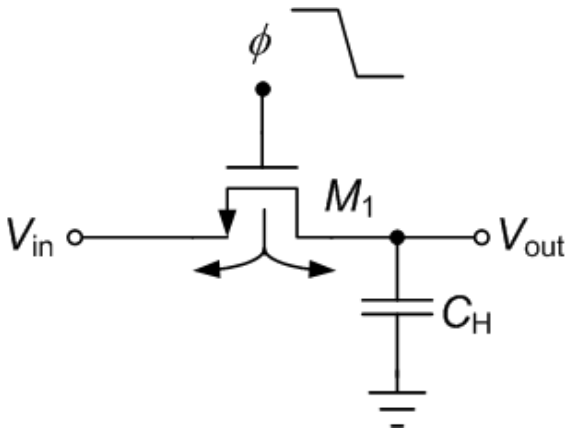


Figure 3.9 Charge injection effect

Usually we assume half of the charge is injected onto the capacitor. In this case, the resulting error is [11]

$$Vclk' \Delta V = \frac{WLV_{ox}(V_{DD} - V_{in} - V_{th})}{C_h} \tag{3.2}$$

The equation illustrates that decreasing *WL* or increasing $C_h$ can reduce this effect.

In addition, there is another undesirable effect called “clock feedthrough” [9]. Consider Fig. 3.10, when the clock signal $V_{clk}$ is high, the NMOS switch is on and $C_h$ is charged to input voltage $V_{in}$. However, when $V_{clk}$ goes from high to low, the switch turns off and the overlap capacitance, $V_{ov}$, and $C_h$ form a voltage divider connecting $V_{clk}$ to ground.

The portion of voltage on $C_h$ is

$$\Delta V = V_{clk} \frac{C_{ov}}{C_{ov} + C_h} \tag{3.3}$$

The equation shows that increasing $C_h$ can reduce this effect.

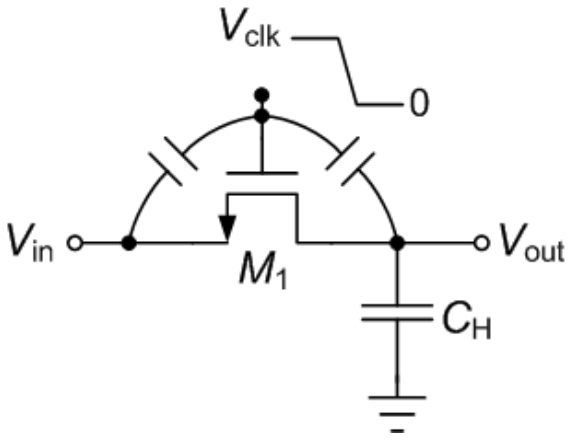


Figure 3.10 Clock feedthrough effect

Numerous methods have been developed to reduce the errors caused by charge injection and clock feedthrough. One widely used approach to reduce the charge injection is to use one NMOS and one PMOS together as a switch shown in Fig. 3.11, called complementary switches or transmission gate [11]. Consider that the charge injected by the NMOS switch is from electrons and that by the PMOS switch is from holes, so theoretically they can cancel each other. However, this is based on an assumption that the two charges are equal, but in reality the gate-drain overlap capacitance of the NMOS is not the same as that of the PMOS, so this method cannot cancel the charge completely. In addition, complementary switches can lower overall on-resistance compared with using a single NMOS or PMOS switch.

Another method is to add a dummy device after the switch [11]. As shown in Fig. 3.12, $M_2$ is placed after $M_1$ with the drain and source of $M_2$ shorted. When $M_1$ turns off, it injects charge to the right side, if half-sized $M_2$ turns on at the same time and absorbs the charge to form a channel. If the two are the same amount, then the dummy device helps cancel the charge caused by $M_1$. When $M_1$ is on and $M_2$ is off, $M_2$ also injects its own charge. However, all the charge from it will go through $M_1$ to low-impedance voltage source, resulting in the charge injected by dummy switch $M_2$ does not affect the voltage across $C_h$.

In this design, complementary switches with dummy switches as in Fig. 3.13 have been chosen for precision consideration.

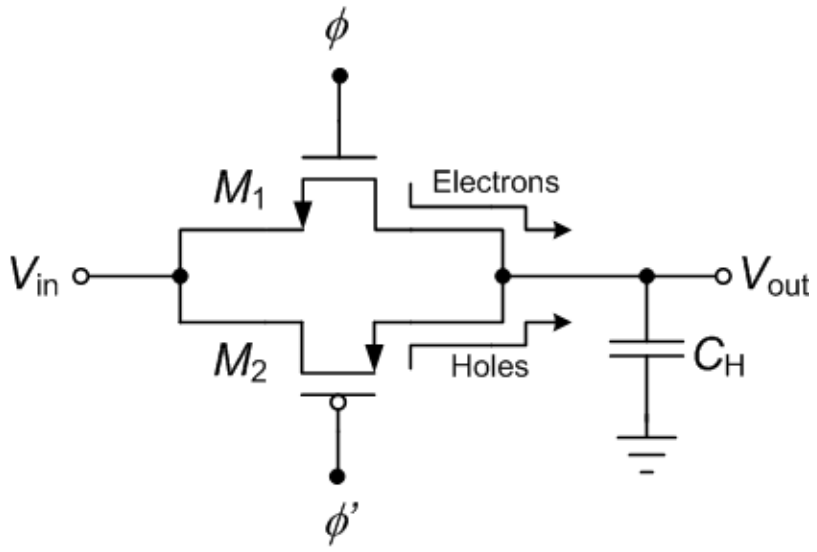


Figure 3.11 Complementary switches to reduce charge injection effect

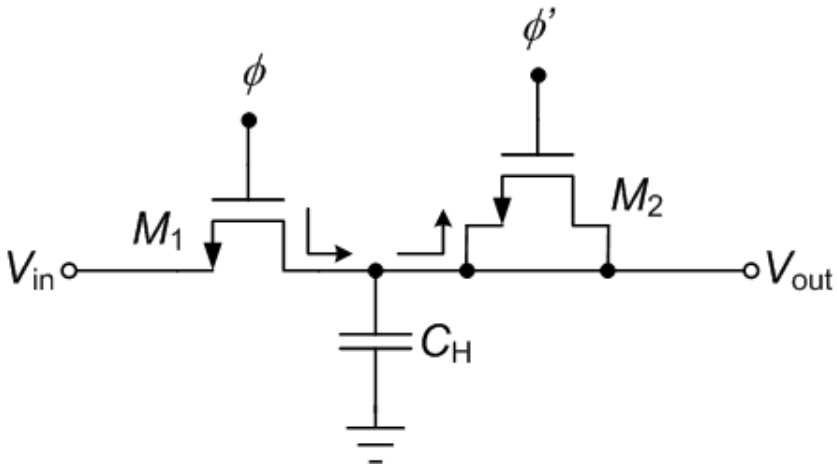


Figure 3.12 Addition of dummy device

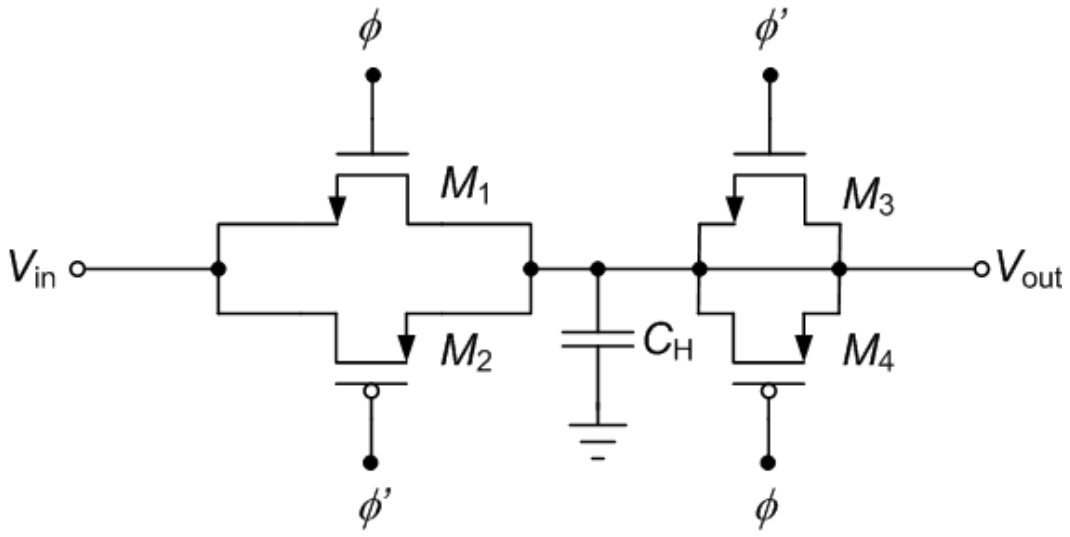


Figure 3.13 Complementary switches with dummy switches

As stated before, smaller transistor area and larger hold capacitors can improve the accuracy of sampling circuits, so smaller *W* and *L* and larger value storage capacitors are chosen. In this design, *W/L*=10/1 for $M_1$, *W/L*=4/1 for $M_2$, $M_3$ and $M_4$ are half sized, and the capacitor is 100 pF.

## 3.8 Pseudodifferential Switch Driver

Complementary switches require low-skew overlapping gate drive signals to control the NMOS and PMOS switches. Simple using an inverter to get clock' would causes relatively large skew between clock and clock'. However, it is very important when $M_1$ and $M_2$ turns off, $M_3$ and $M_4$ turns on simultaneously so that it does not cause distortion. To solve this problem, the pseudodifferential CMOS switch driver circuit as in Fig. 3.14 is used as the switch driver for complementary switches [2]. It generates two overlapping signals and can effectively reduce clock skew between the two signals.

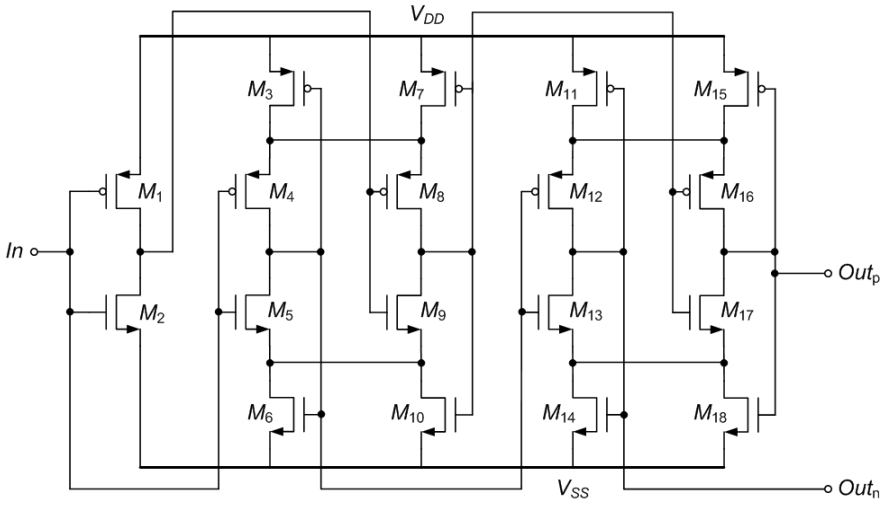


Figure 3.14 Schematic of pseudodifferential switch driver [2]

## 3.9 Layout Issues

To design analog and/or mixed-signal circuits successfully, careful attention must be paid to layout. In Fig. 3.15, the part in red box is the layout of the ping-pong autozero op amp, with area 1140 μm by 790 μm. Two copies of identical amplifiers were placed symmetrically, and the two green areas are two 100 pF capacitors storing offset voltage. Common-centroid layout was used for all differential pairs and current mirrors. In addition, every Vdd was padded out separately for power measurement.

## 3.10 Simulation Results

### 3.10.1 Simulated Offset Voltage

After design, characterizing simulations have been performed to verify the design. A key parameter of this op amp is input offset voltage, which is defined as the differential input voltage required to zero output voltage. However, there is no matching or process

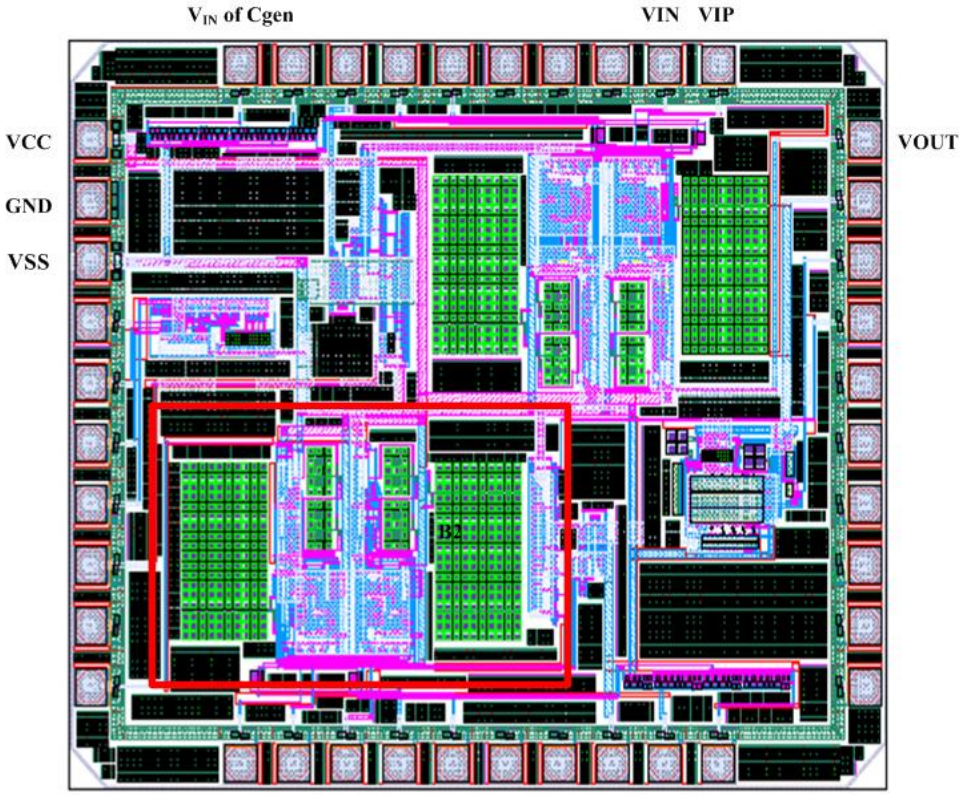


Figure 3.15 Full chip layout (0.5-micron SiGe BiCMOS)

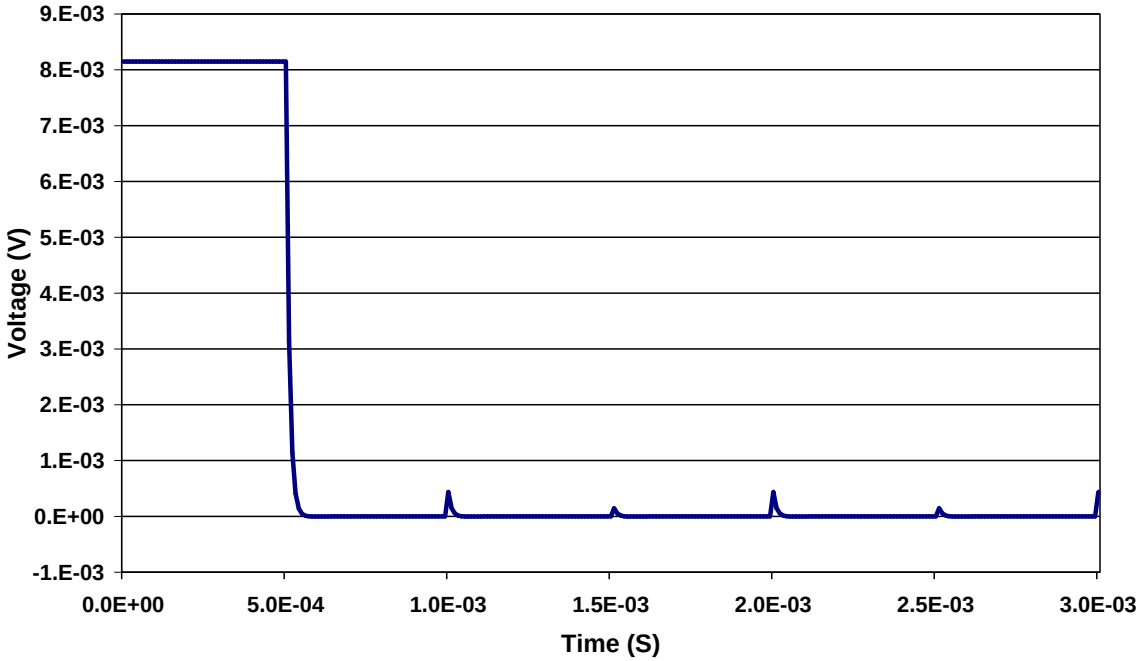


Figure 3.16 Simulated offset cancellation process

variation in the initial simulation. To check the functionality of offset correction, a 10-mV offset voltage was injected manually to one input terminal, so the offset was set to around 10 mV. Running transient simulation, one should expect to see the ping-pong op amp autozero its offset to around 0 V.

Fig. 3.16 shows that the initial offset value is over 8 mV, and then is successfully cancelled to close to 0 V through the op amp's autozero operation. What also can be seen are glitches due to switching at 1.0 ms, 1.5 ms, 2.0 ms, 2.5 ms and 3.0 ms in the figure. These time intervals correspond to the ping-pong controlling clock frequency of the op amp.

### 3.10.2 Monte Carlo Simulation of Offset Voltage

To simulate the worst-case performance, Monte Carlo simulation was performed with process variations and mismatch across temperature, without the additional 10 mV injected offset voltage.

At −180°C, the simulation results in Fig. 3.17 show that offset voltages are between −25 μV and +20 μV. For this Monte Carlo simulation more than 30 runs out of 40 have offset voltage between −5 μV and + 10μV. At room temperature (25°C) as shown in Fig. 3.18, the offset voltages are between −5 μV and +10 μV, better than the offset at −180°C. Except one 10 μV run, all other are located between −4 μV and +4 μV. Fig. 3.19 shows at +120°C offset voltage range is between −6 μV and +2 μV.

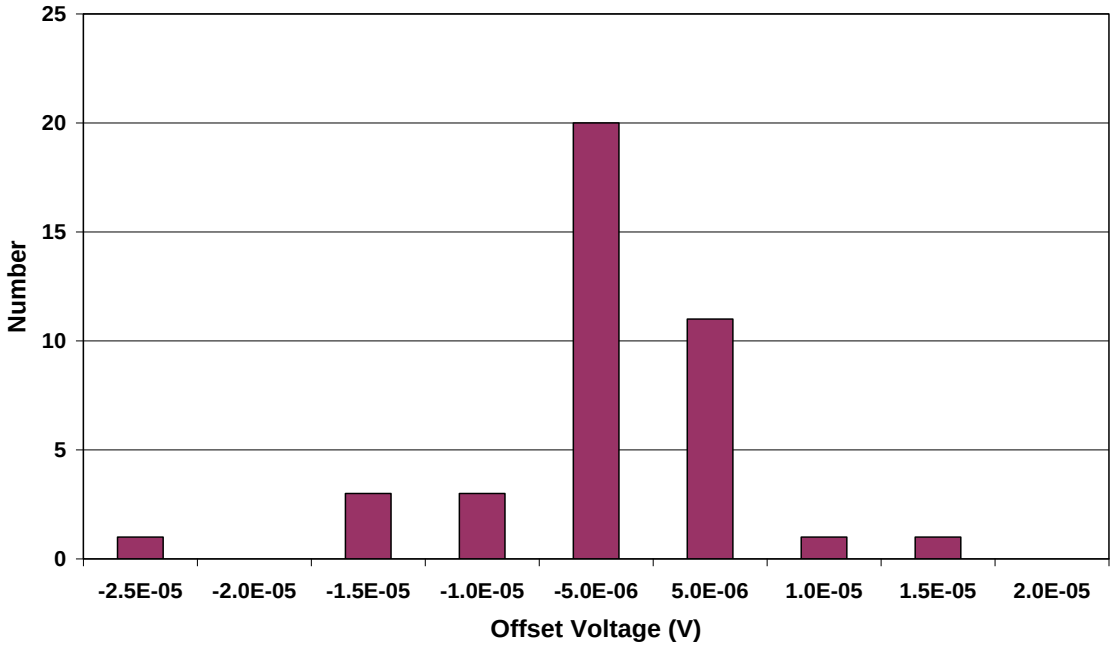


Figure 3.17 Monte Carlo simulation results at −180°C

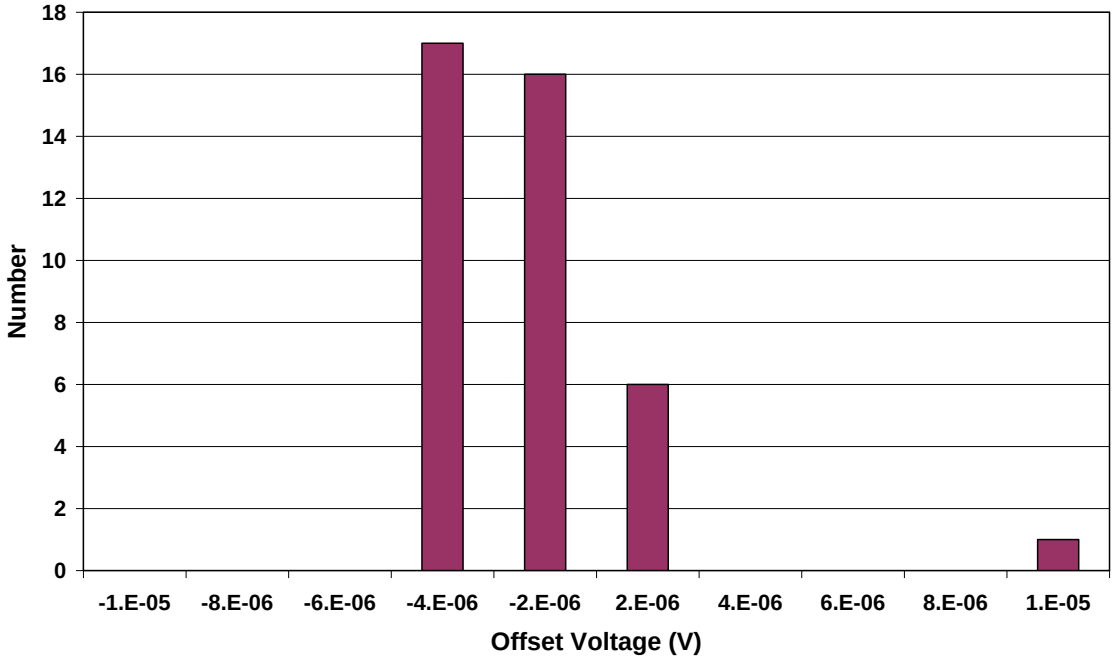


Figure 3.18 Monte Carlo simulation results at 25°C

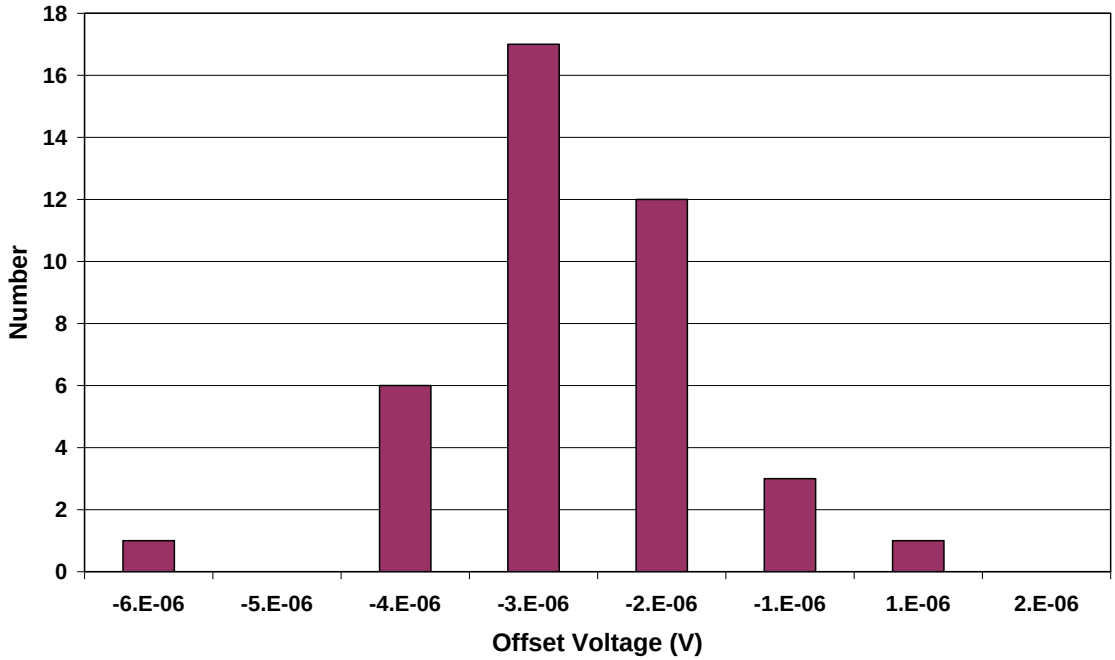


Figure 3.19 Monte Carlo simulation results at 120°C

### 3.10.3 Simulated Open-loop Gain

Open-loop gain is the output voltage over the differential input voltage when the op amp is open-loop. It is an important parameter that influences other parameters like common mode rejection ratio and power supply rejection ratio. Fig. 3.20 shows simulated dc open-loop gain at room temperature is 116 dB using typical corner models.

### 3.10.4 Input Common Mode Range

Input common mode range is defined as the range of common-mode voltage to keep all the transistors in the first stage in the desired saturation region. In simulation, the op amp was in non-inverting unity-gain configuration, simulated result shows the suitable input range is from –1.65 V to +1.2 V at room temperature as in Fig. 3.21.

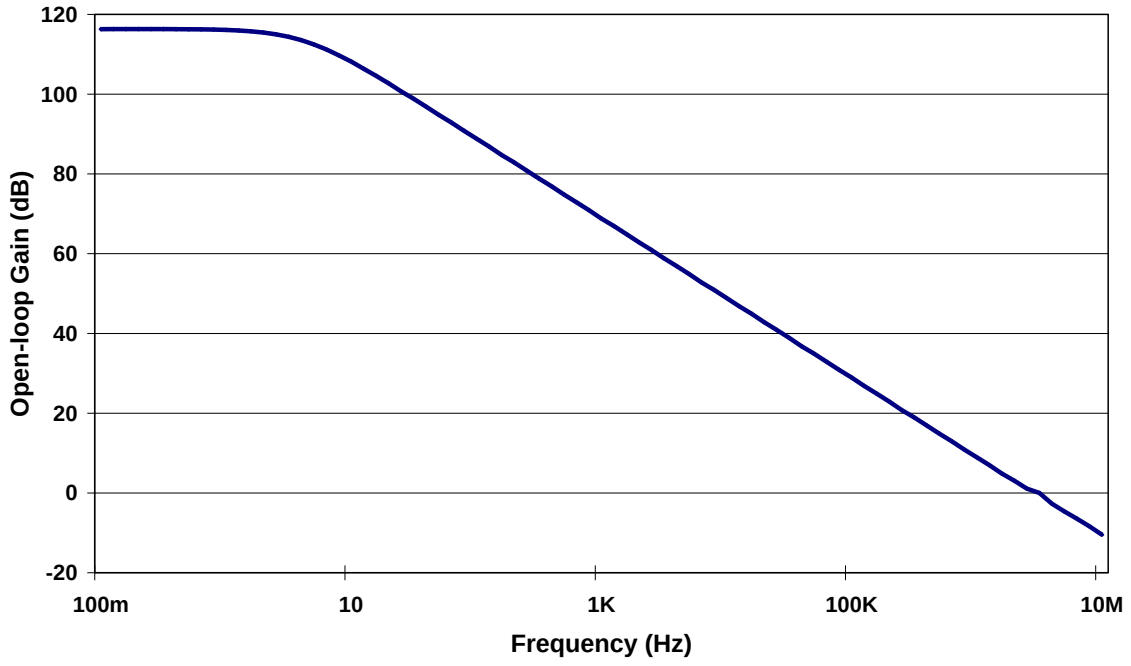


Figure 3.20 Simulated open-loop gain

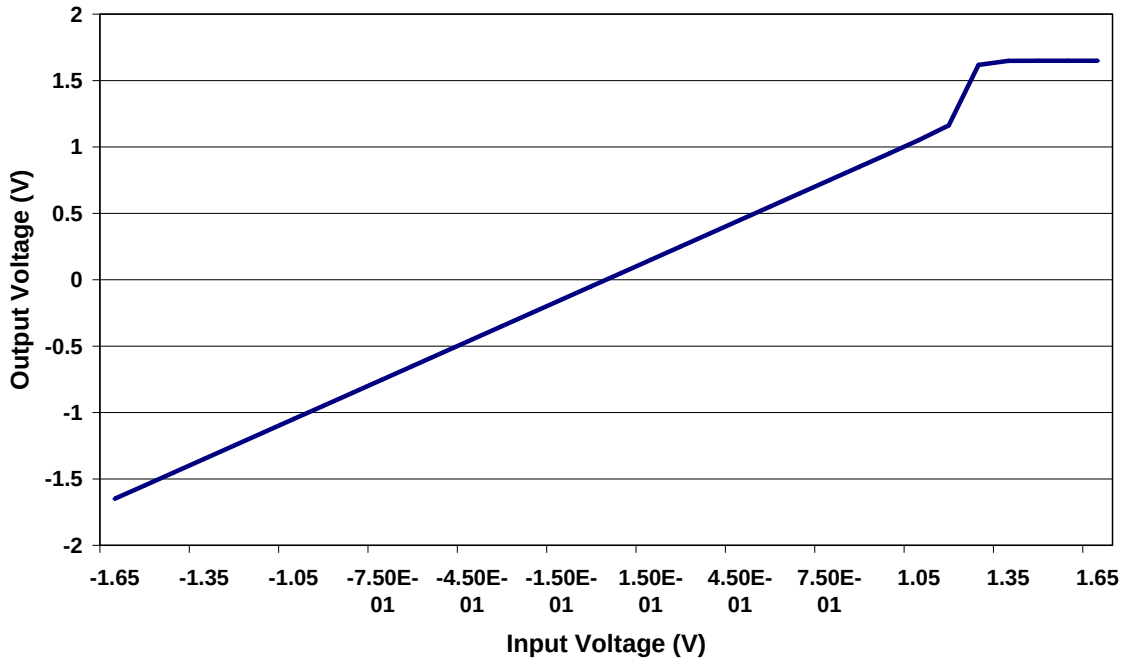


Figure 3.21 Simulated input common mode range

If not mentioned, the op amp's supply voltage rails are always ±1.65 V, or 3.3 V total across the op amp in the simulations.

### 3.10.5 Slew-Rate

The op amp was configured non-inverting unity-gain. The simulation results in Fig. 3.22 show that the rising slew-rate is 2.0 V/μs and falling slew-rate is –2.1 V/μs at room temperature.

### 3.10.6 Common Mode Rejection Ratio

Common mode rejection ratio is defined as the differential gain divided by the common-mode gain. For this design, the CMRR is the CMRR of the first stage because the second stage is single-ended to single-ended stage that does not provide more differential gain to

the op amp. The simulated CMRR is 136 dB at low frequency at room temperature as in Fig. 3.23.

### 3.10.7 Power Supply Rejection Ratio

Power supply rejection ratio is a parameter to measure how well an op amp rejects variation on the positive and negative power supply rails. Shown in Fig. 3.24 and Fig. 3.25 at room temperature the low frequency PSRR+ is 118 dB and PSRR− is 112 dB, respectively.

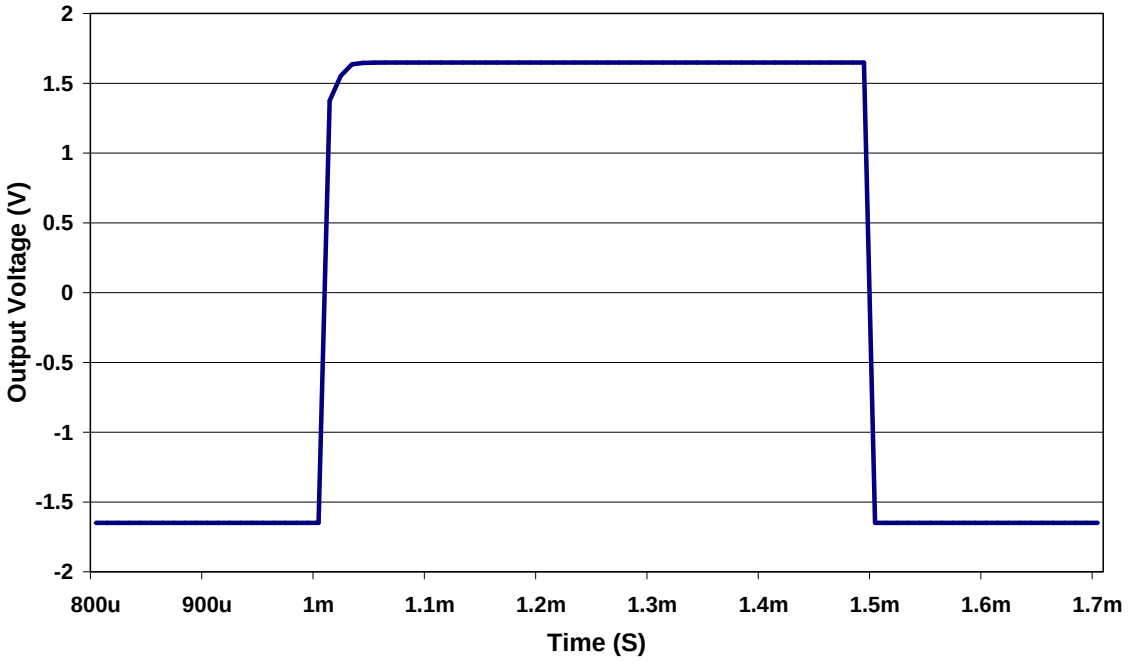


Figure 3.22 Simulated large signal response for slew rate

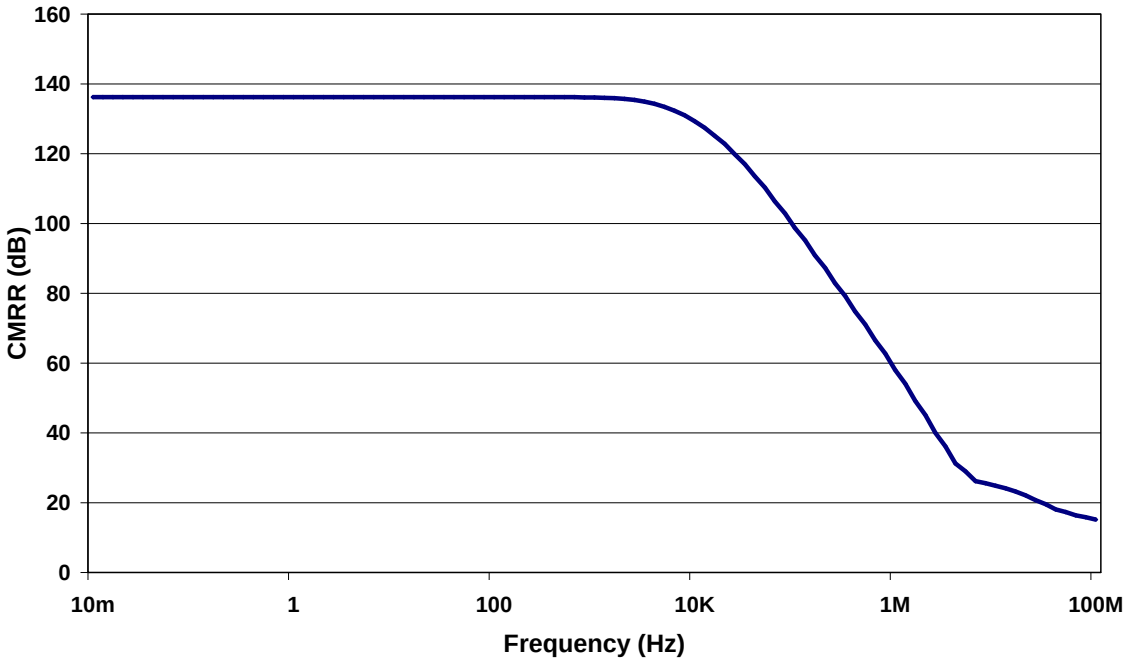


Figure 3.23 Simulated common mode rejection ratio

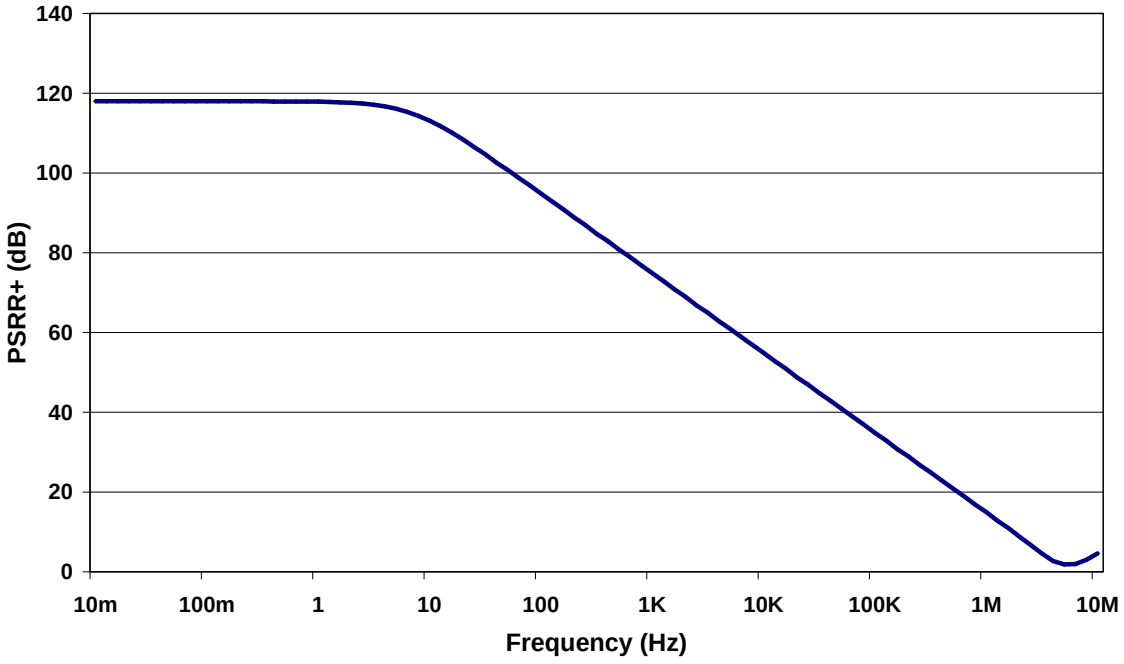


Figure 3.24 Simulated positive power supply rejection ratio

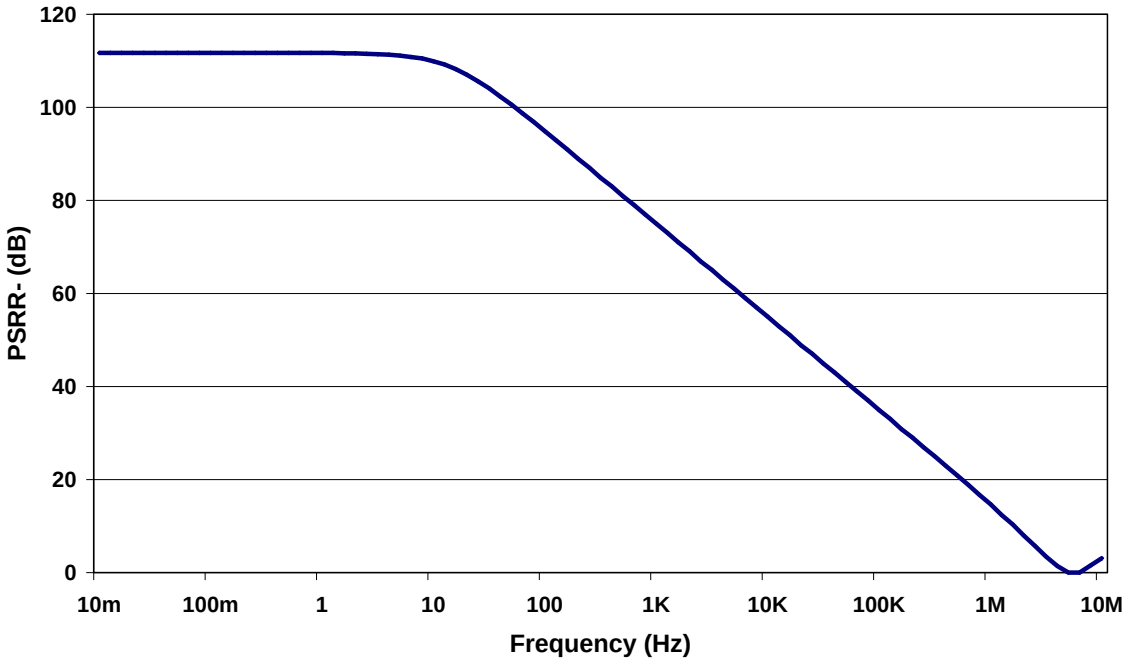


Figure 3.25 Simulated negative power supply rejection ratio

# CHAPTER 4 MEASUREMENT RESULTS

This chapter presents the test setup to characterizing the op amp and measured results.

## 4.1 Open-Loop Gain

To measure open-loop gain, the op amp was put in the inverting unity-gain configuration with two 250 kΩ resistors as shown in Fig. 4.1 [13] [14]. The HP3589A spectrum/network analyzer was used to measure the open-loop gain. The $V_{ref}$ was connected to the non-inverting input terminal and a sine wave generated by the HP 3589A was input to the inverting input terminal through a 250 kΩ resistor. To get the open-loop gain, the error voltage between the two input terminals and the output voltage were measured.

$$A_{ol} = \frac{V_{out}}{V_e} \tag{4.1}$$

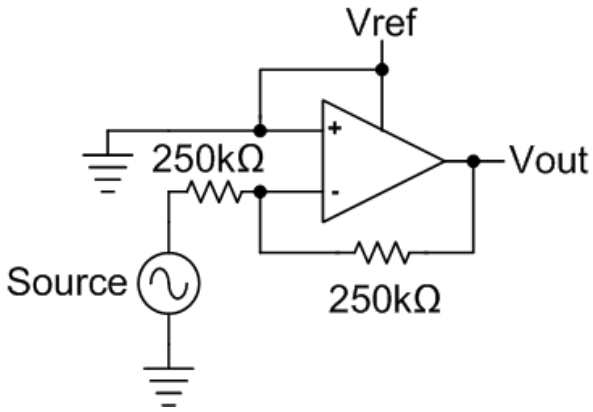


Figure 4.1 Simplified open-loop gain measurement configuration for the ping-pong op amp

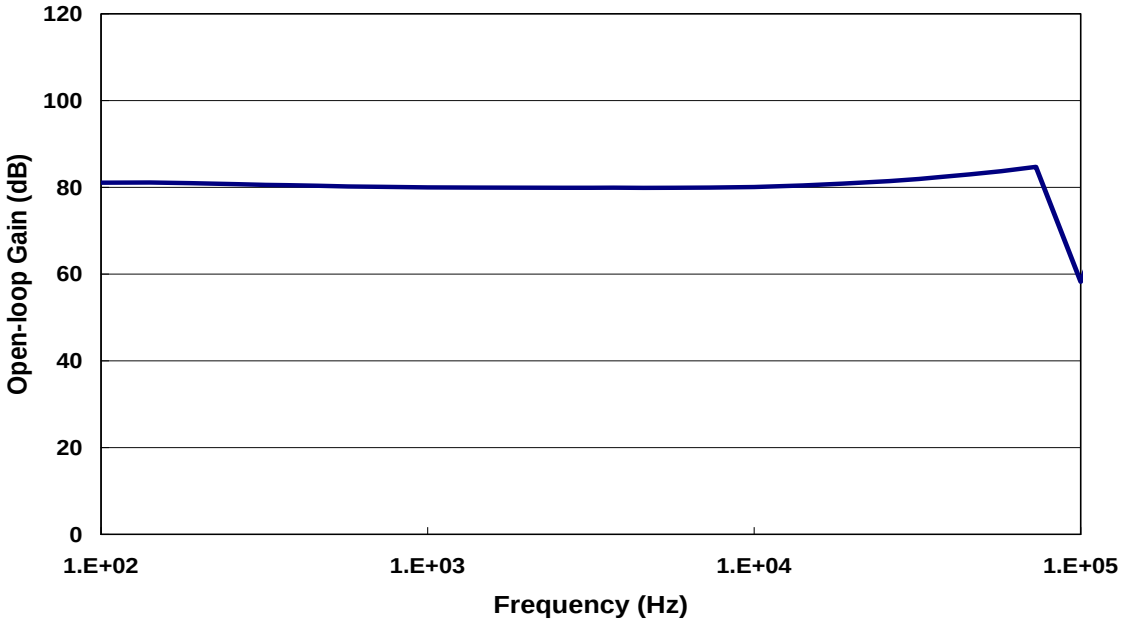


Figure 4.2 Measured open-loop gain

Fig. 4.2 shows that the dc open-loop gain measured is 81 dB. Because the testing instruments have problems at high frequency, the result only covers the range from 100 Hz to 100 kHz.

Moreover, the gain value is limited by measurement resolution, so here the 81 dB gain is less than 116 dB in simulation. Gain bandwidth product was measured as 750 kHz.

## 4.2 Offset Voltage

Usually unity-gain configuration can be used to test offset voltage of an op amp. However, this design's main purpose is to achieve low-offset, so a more accurate testing setup is preferred that amplifies the offset voltage to improve the measurement accuracy.

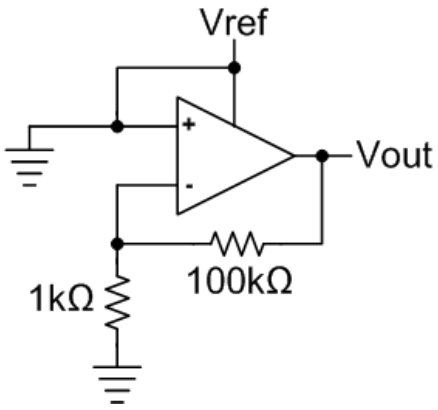


Figure 4.3 Circuit configuration for offset measurement

A feedback configuration in Fig. 4.3 was used for offset measurement, and offset value is

$$V_{os} = \frac{V_{out}}{100} \tag{4.2}$$

## 4.3 Offset Drift over Temperature

To be used in extreme environment, the op amp should not only have a low offset voltage at room temperature, but also provide low drift in offset over wide temperature range. Offset voltage variation of four chips was measured from −100°C to +80°C. The results are shown in Fig. 4.4, indicating the op amp has very low offset drift (0.1 μV/°C is the worst case of four measured chips) over the measurement temperature range.

## 4.4 Slew-Rate

Configured in the unity-gain feedback configuration shown in Fig. 4.5, the HP33250A function generator provided large-signal steps to measure slew rate. The slew-rates measured shown in Fig. 4.6 and Fig. 4.7 are +2.1 V/μs and –2.5 V/μs.

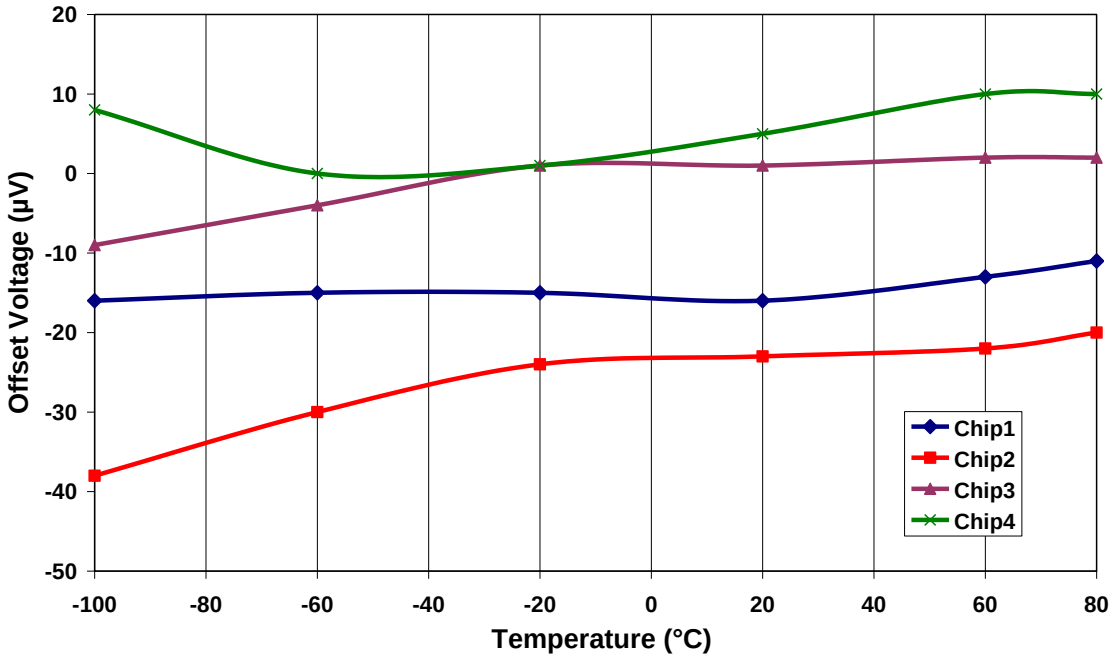


Figure 4.4 Measured offset voltage over temperature

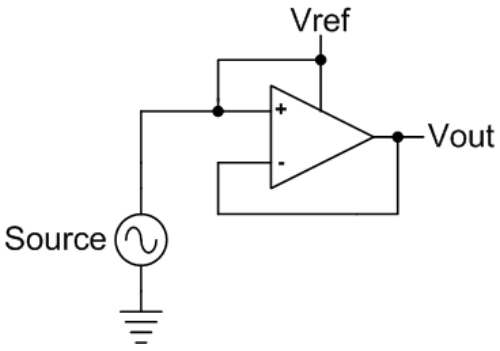


Figure 4.5 Unity-gain configuration test setup for the ping-pong op amp

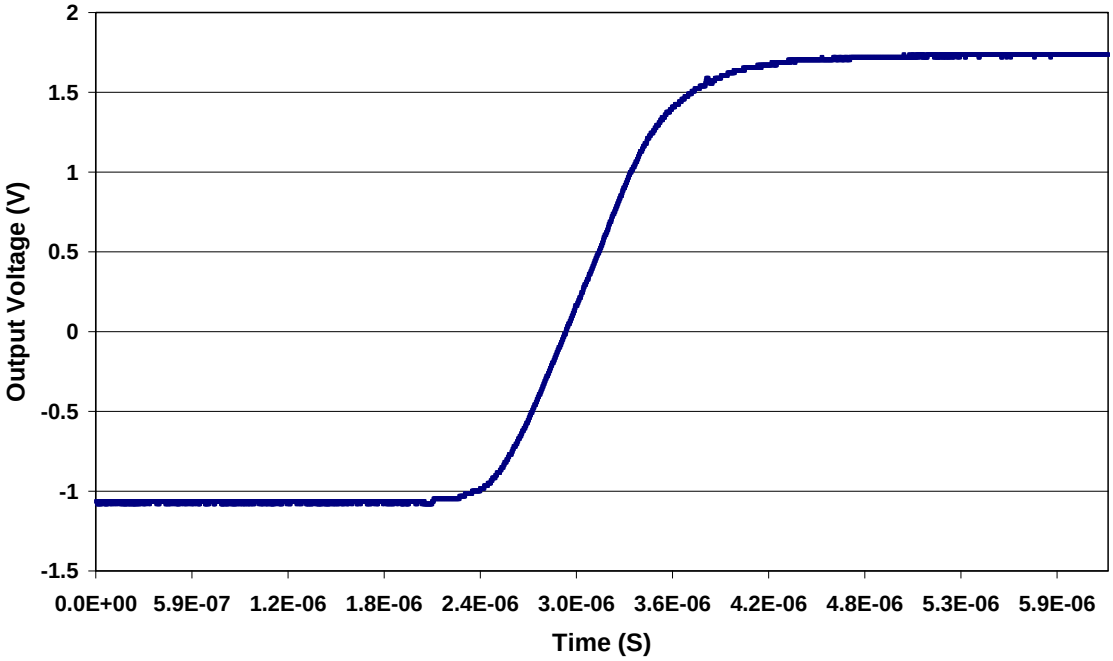


Figure 4.6 Measured slewing during low-to-high transition

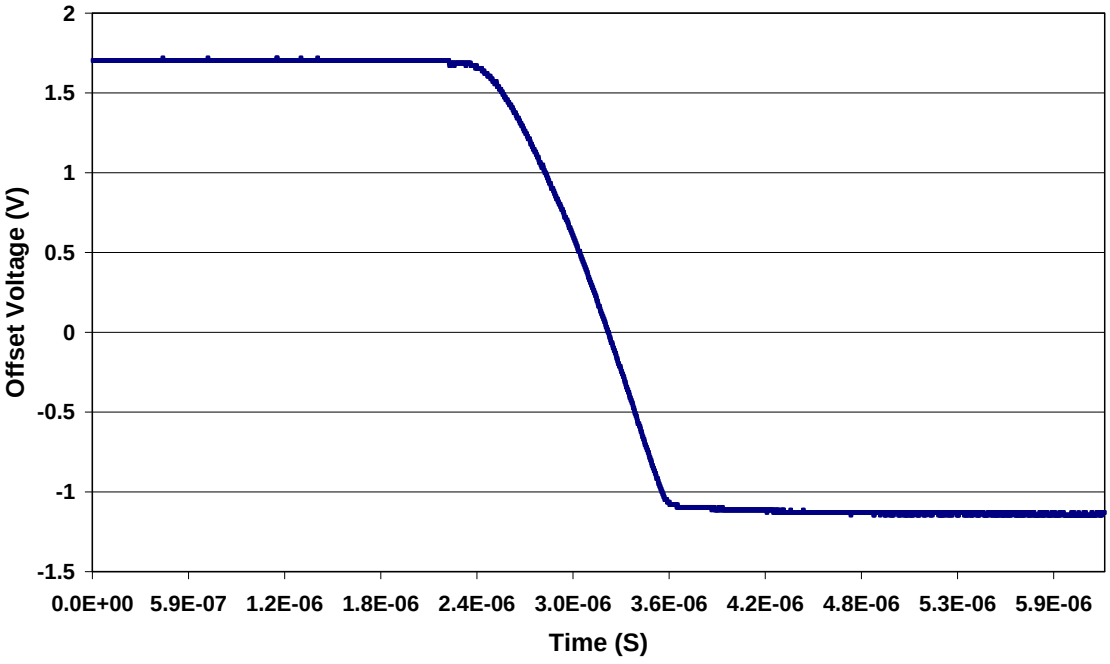


Figure 4.7 Measured slewing during high-to-low transition

## 4.5 Input Common Mode Range

The op amp was configured as non-inverting unity-gain as in Fig. 4.5, and the measured results are shown in Fig. 4.8. The dark blue line is the input voltage, and the red one is the output voltage. The range in which the red line follows the dark blue one provides an optimistic estimate of the input common mode range for the ping-pong op amp: –1.65 V to +1.2 V.

## 4.6 Power Consumption

Approximate 0.3 mA was shown on the power supply, resulting in a power consumption of about 1 mW.

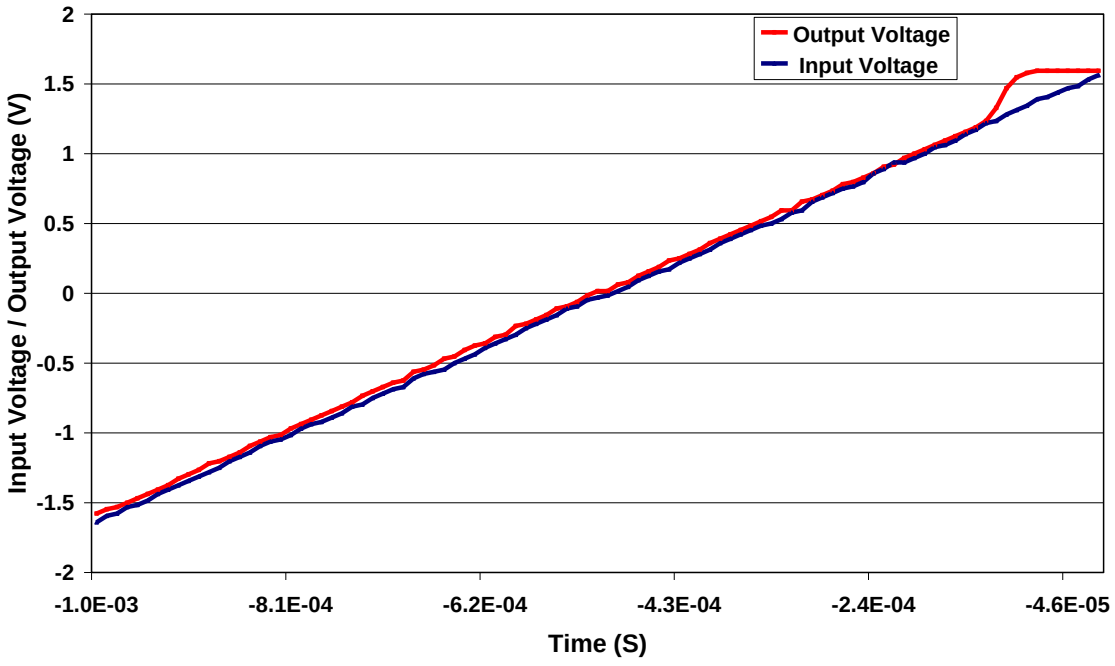


Figure 4.8 Measured input and output voltages

# CHAPTER 5 CONCLUSIONS AND FUTURE WORK

## 5.1 Conclusions

A low-power precision op amp using ping-pong autozero architecture was designed and fabricated in a commercially available 0.5-μm SiGe BiCMOS process. The measurement results show the op amp achieves less than 40 μV offset voltage and ≤ 0.1 μV/°C offset drift from −100°C to +80°C, and 1 mW power consumption.

## 5.2 Future Work

Although this design has demonstrated that the ping-pong autozero op amp is capable of operating over wide temperature range, there are a few verifications and optimizations can be done in the future:

- better setup for open-loop gain measurement,

- development of more precision sampling switches to reduce errors caused by switches,

- noise measurement can be performed to verify that the autozero process also cancels the flicker noise [2] so that the op amp has lower noise at low frequency,

- modify this design to fit specific system level requirements of a target application.

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# APPENDIX

Test Boards

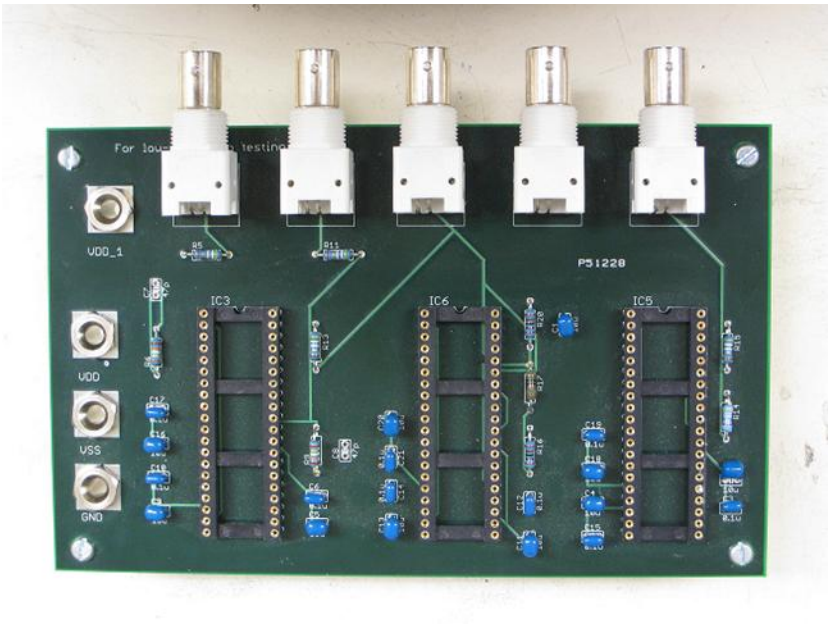


Figure A-1 Main test board

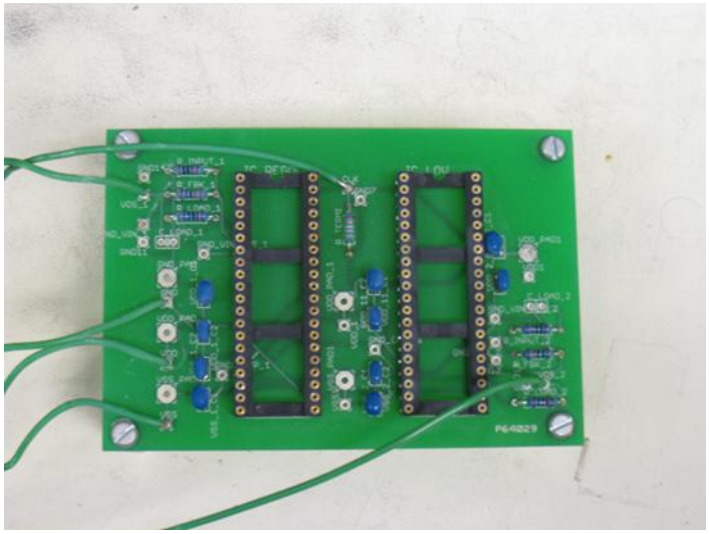

Figure A-2 Temperature test board

# VITA

Pengfei Xi was born in Anhui, China in 1982. He entered Anhui University majoring Electronic Engineering in 2000. Pengfei graduated with a Bachelor's degree in July 2004, and came to the University of Tennessee that fall to further his study. During this time he was a graduate teaching assistant in the Electrical Engineering department, and then worked for Dr. Blalock as a graduate research assistant on analog IC design. During the spring and summer of 2008, he was with power management group at Texas Instruments, as a design intern.