8-2012

Analog Testing, Characterization, and Low-Order Model Extraction using LabVIEW Automation

Jeremy Brantley
jbrantl9@utk.edu

To the Graduate Council:

I am submitting herewith a thesis written by Jeremy Brantley entitled "Analog Testing, Characterization, and Low-Order Model Extraction using LabVIEW Automation." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Benjamin J. Blalock, Major Professor

We have read this thesis and recommend its acceptance:

Kamrul Islam, Charles Britton

Accepted for the Council:
Dixie L. Thompson

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

Analog Testing, Characterization, and Low-Order Model Extraction using LabVIEW Automation

A Thesis Presented for the
Master of Science
Degree
The University of Tennessee, Knoxville

Jeremy Brantley
August 2012

DEDICATION

.

To my mom and dad, Lynda and Chris, I guess all of those dinner table conversations about work at the lab kinda rubbed off…

ACKNOWLEDGEMENTS

I would like to thank my committee: Dr. Blalock, Dr. Islam, and Dr. Britton. You have all given me so much guidance over the years, not all of it circuit related, it has been very much appreciated.

And to my fiancée, Jenn, thank you for reading this and inserting commas where necessary. I'm sure you had much better things to do.

ABSTRACT

Testing circuits is a hands-on, time intensive process; it is also one of the most important steps in a design cycle. The most well designed circuit is only an academic exercise if it does not work in real life. The time and cost associated with bench level testing pales in comparison to testing for extreme environments. Testing in extreme heat, cold or radiation introduces a large set of challenges that are rarely encountered in standard bench level testing. The two most pronounced problems are the inaccessibility of the devices under test and time constraints, both short and protracted. Due to the physical properties of devices and circuits there is a short window in which all testing must be conducted for each incremental step during extreme environment tests. This time requirement does not present a significant challenge when testing a single circuit or device, but the cost associated with this testing is enough to encourage a more efficient method.

The primary goal of this work is to reduce the time required to perform tests through the use of automation and parallel test schemes. The automation software chosen for this project was LabVIEW. LabVIEW is a graphical based programming language with an extensive library of functions for interfacing with test instrumentation. Due to the graphical nature of this language, display of measurement data is essentially a byproduct of the program. This allowed for confirmation of proper operation and immediate rectification if a problem was discovered.

This paper will cover the key parameters of common devices and circuits, methods for extracting these parameters from other prevailing effect, and methods for automating these tests through the use of computer based tools such as LabVIEW.

TABLE OF CONTENTS

LIST OF TABLES

Table Page

LIST OF FIGURES

CHAPTER I
INTRODUCTION AND GENERAL INFORMATION

Integrated Circuits and Extreme Environments

Integrated circuits (ICs) have a significant impact in everyday life. For decades ICs have been getting smaller and more powerful. Instrumentation and processors that used to be the size of a toaster oven can now be contained on a single IC measuring no more than a few square millimeters. This skyrocketing capability has led to the proliferation of ICs in every facet of life. As a simple comparison, the current iPhone could replace the Apollo 11 computer thousands of times over. Clearly, computational power is no longer the premium it once was and as this paradigm has shifted, the design of automobiles, spaceships, satellites, and numerous other “smart” tools has followed suite. The priority now is minimizing size and weight and replacing mechanical parts with the more reliable electronic versions.

Shifting from mechanical to electrical systems offers numerous advantages, but it places more of a burden on the circuits. As ICs make their way into more critical applications in aviation, automotive and space exploration it becomes more important to properly characterize these circuits in environments comparable to their intended operating condition. These operating conditions could be the high heat of an automobile engine compartment or if the intended application is of the extra-terrestrial type, it may be a combination of frigid cold and cosmic radiation. Any of these scenarios can lead to unexpected failure on silicon.

Years of study have gone into characterizing ICs at these extreme temperatures and many advances have been made into understanding the various phenomena that lead to these changes. Even after all of these advances, though, there is no documentation or simulations that can compare to testing actual circuits in real-life conditions. There are fairly inexpensive methods for approximating harsh environments (think: toaster oven or ice chest). But to really take it to the extreme, large facilities with an equally sized price tag are involved. The expense involved in conducting experiments at these environmental simulation systems necessitates quick data recovery.

This paper will cover Devices, Circuits and Characterization in Chapter II, Data Collection and Programming in Chapter III, Results and Discussion in Chapter IV, and Conclusions and Recommendations in Chapter V. To maintain the flow of this paper without excluding too much detail, a more extensive treatment will be given to the programming methods and suggestions in the appendices.

CHAPTER II
DEVICES, CIRCUITS AND CHARACTERIZATION

During the process of designing circuits and systems, engineers will use simulations and hand calculations to predict and estimate the behavior of circuit topologies. It is impossible, though, to fully capture the interactions between silicon and metal in the semiconductor jungle of an integrated circuit. Therefore, testing and characterization is a necessary step to confirm the validity of simulations.

Even the most fundamental component of the modern active circuit, the MOSFET, requires a multistep approach to build even the most basic model. Developing these models requires techniques that will suppress the influence of some parameters while making desired parameters dominate. In this chapter the details for characterizing transistors and operational amplifiers (op-amps) are covered.

Transistors

Transistors are one of the main components that make up active circuits. Without accurate models for these basic devices, it follows that it is not possible to accurately model the operation of these more complex circuits. A basic characterization of these devices is detailed below.

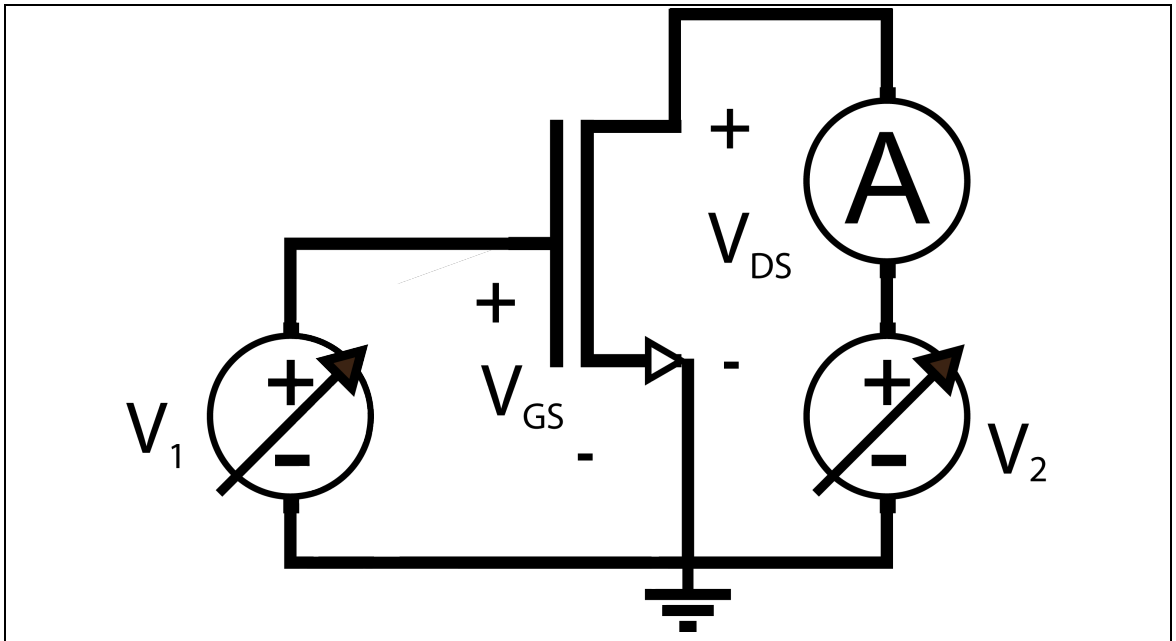

Figure 1 Basic Transistor Characterization

There are a few key parameters that can, at least to a first order, define the operation of transistors. The threshold voltage (V_{TN}) and transconductance (K_n) show up in both the saturation and linear region equations [1][3][6], (1) and (**2**). The threshold voltage defines, quite simply, the point at which a device turns on. Transconductance relates the drain current to a given bias condition. A third parameter that is important in the context of circuit design is the output resistance (r_o). This is most directly related to the channel length modulation parameter (λ) in the saturation equation **(**1**)**. These parameters can be extracted with a few simple tests.

$$i_D = \frac{K_n'}{2}\frac{W}{L}(v_{GS} - V_{TN})^2(1 + \lambda V_{DS}) \qquad \textbf{1}$$

$$i_D = K_n'\frac{W}{L}\left((v_{GS} - V_{TN})V_{DS} - \frac{V_{DS}^2}{2}\right) \qquad \textbf{2}$$

Threshold Voltage

Characterization of transistors generally involves performing voltage sweeps to obtain current versus voltage data (or I-V curves). From these sweeps key parameters of transistors can be derived. The classic circuit configuration for these sweeps, shown in Figure 1, uses one voltage source on the gate of the device to sweep the gate-to-source voltage and a second voltage source is used to hold the drain-to-source voltage constant. While sweeping the gate voltage, the drain current is measured. That data can be used to produce I-V curves such as Figure 2 and Figure 3.

Sweeping the gate voltage of transistors can illustrate many characteristics. To emphasize the threshold voltage, though, it is helpful to plot the data as the square root of the drain current versus the gate voltage as in Figure 2 [3]. It may be necessary to zoom into the point at which the transistor transitions from negligible current conduction ($I_{leakage}$) to the beginning of linear operation (Figure 3). That transition should be the point of the maximum slope of the curve. With the threshold voltage determined, the next step is to find the transconductance.

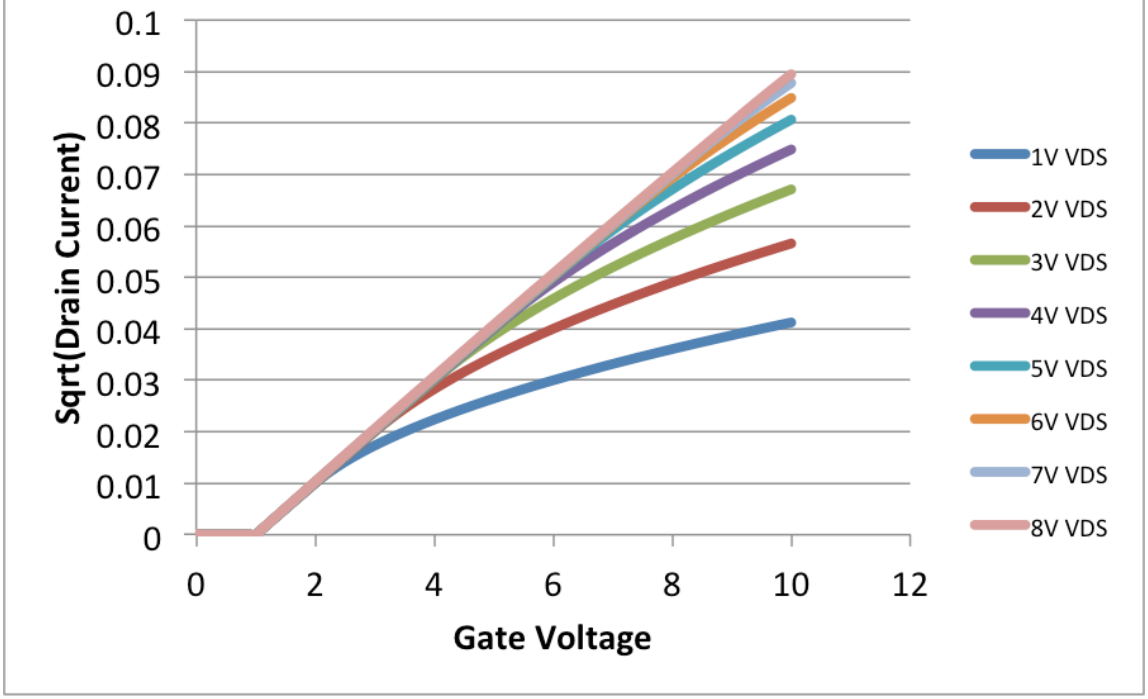

Figure 2 I-V Curve of transistor gate sweep with a constant drain voltage

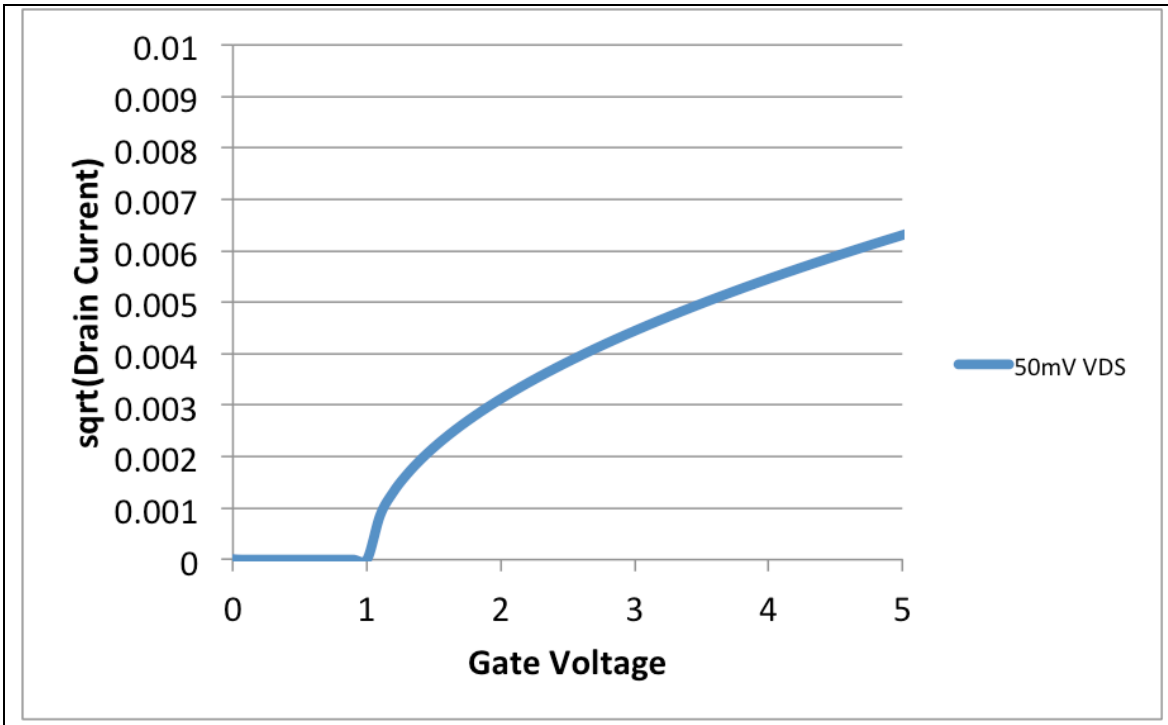

Figure 3 I-V Curve of transistor gate sweep with low V_{DS} to reveal the threshold voltage

Transconductance

Transconductance is the gain factor in a transistor. In the case of MOSFETs, it is the measure of drain current for a given gate voltage. To determine the transconductance parameter of a transistor, I-V curves need to be plotted. The circuit in Figure 1 is used, but this time the gate voltage (V1) is held constant while the drain voltage (V2) is swept. This should produce a plot similar to Figure 4. With this data it is possible to derive transconductance using **(**3**)** and **(**4**)** at multiple points to average out error.

For $\boldsymbol{V_{DS} < v_{GS} - V_{TN}}$

$$K_n = \frac{i_D}{(v_{gs} - V_{TN})V_{DS} - \frac{V_{DS}^2}{2}} \qquad \textbf{3}$$

For $\boldsymbol{V_{DS} > v_{GS} - V_{TN}}$

$$K_n = \frac{2i_D}{(v_{gs} - V_{TN})^2} \qquad \textbf{4}$$

Output Resistance

Output resistance relates to the small change in drain current versus drain voltage. This relationship is just like that of a resistor, an increase in the voltage

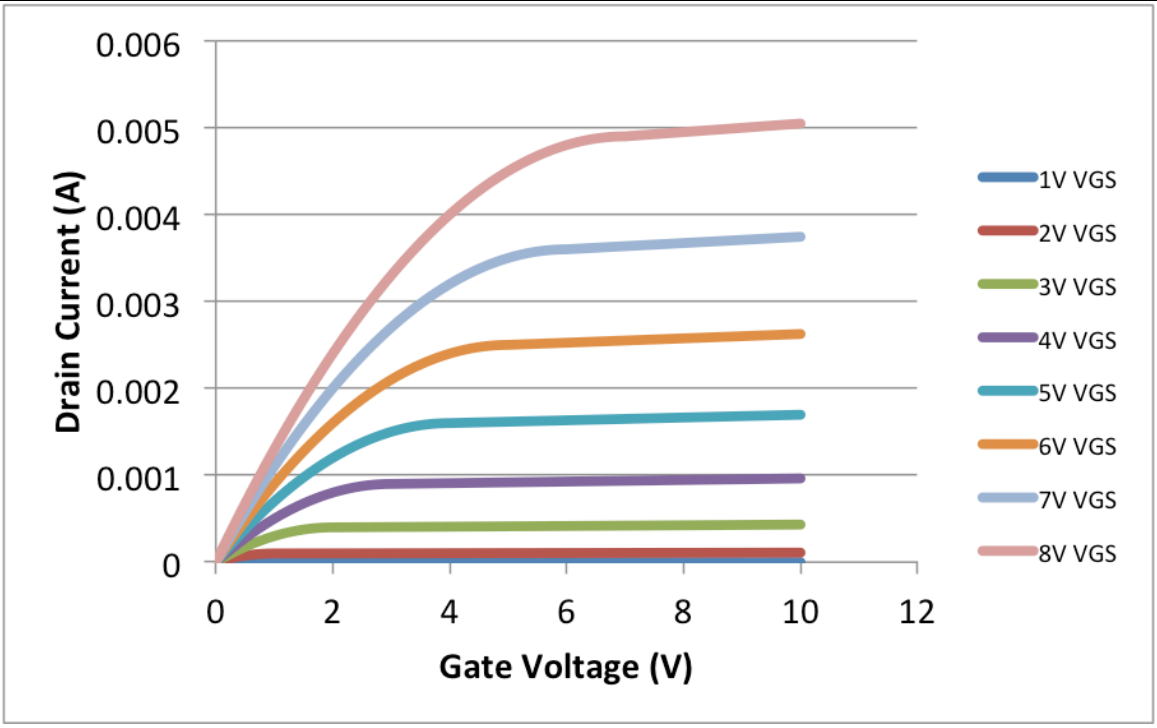

Figure 4 I-V Curve of transistor drain sweep

across the device results in an increase in the current through the device. This effect is clearly visible in Figure 4 when the current ramps up slowly, but linearly, with the increasing drain voltage. To find the output resistance, the transistor must be biased in the saturation region. A small voltage step must be applied and the corresponding drain current measured. The size of the voltage step will be divided by the difference of the drain current before and after the step. The output resistance is

$$r_o = \frac{v_2 - v_1}{i_2 - i_1} \qquad \textbf{5}$$

Op-Amps

Operational Amplifiers (Op-Amps) are one of the cornerstone functional blocks in integrated circuits. As their name suggests, they can be used to amplify signals, but they can also be used to regulate signals or buffer outputs. Because op-amps tend to be used as stand alone circuit blocks it is often necessary to perform a wide number of tests on them to confirm stability over a wide range of operation conditions. These tests cover a wide set of parameters and require many different modes of operation.

In a more complex block like an Op-Amp there are many different factors that can affect the transfer characteristics. Ideally, each of these parameters can be characterized individually. In order to achieve this goal, in turn, each parameter must be made to dominate the output signal. Much of the characterization is done along the logical signal path (I.E. gain, stability) , but some of the parameters include the power supplies as well. In order to best characterize the op-amp it is helpful to have access to all of the terminals. The complete characterization of an op-amp requires a battery of tests. These tests generally have to be altered from the ideal calculations to take into account the limitations of non-ideal circuits and tests equipment. Open loop gain is a prime example of an op-amp parameter that cannot fit into real test constraints. Op-Amps generally have open-loop gain on the order of 80 to 120 dB. In order to have the output within the voltage supply range of the op-amp, the input would have to be on the order of 1 millionth that of the output voltage. In practice it is very difficult to generate clean signals at such low amplitude. To overcome limitations such as this, unique circuit configurations must be used. This section will detail a variety of these configurations and the parameters they test.

Gain Error

Gain error is the result of finite open-loop gain in op-amps. Amplifier voltage gain **(**6**)** is a function of the open-loop gain (A) and the feedback factor

(β). When the open loop gain is infinite, the voltage gain simplifies and becomes the reciprocal of the feedback factor **(**7**)**.

$$A_v = \frac{A}{1 + A\beta} \quad \textbf{6}$$

$$A_{ideal} = \frac{1}{\beta} = 1 + \frac{R_2}{R_1} \quad \textbf{7}$$

Gain error can be measured directly by inputting a known signal and measuring the output. The difference of the expected gain and the measured gain is the gain error [1][3][5]. Fractional gain error **(**9**)** is the gain error divided by the ideal gain.

$$FGE = \frac{ideal\ gain - measured\ gain}{ideal\ gain} \quad \textbf{8}$$

$$FGE = \frac{1}{1 + A\beta} \quad \textbf{9}$$

This is a simple metric that can be used to roughly validate an amplifiers open-loop gain. It is a rough approximation because there are a few sources of error that can corrupt this measurement. Resistor tolerance can contribute a significant deviation from the open loop gain error. Even using 1% metal film resistor can result in approximately 2% error in the expected β.

$$\beta = \frac{R_1}{R_1 + R_2} \quad \textbf{10}$$

$$\Delta\beta = \frac{R_1 \pm 1\%}{R_1 \pm 1\% + R_2 \pm 1\%} = 1 + \frac{R_1 \pm 1\%}{R_2 \pm 1\%}$$

for $R_2 \gg R_1$ and worst case deviation

$$\beta\ \%error \approx 2\%$$

$$Gain\ Error = \frac{1}{\beta(1 + A\beta)} \quad \textbf{11}$$

$$\frac{\Delta GE}{GE} = \frac{\frac{1}{\Delta\beta(1+A\Delta\beta)}}{\frac{1}{\beta(1+A\beta)}} = \frac{\beta(1+A\beta)}{\Delta\beta(1+A\Delta\beta)}$$

$$\frac{\Delta GE}{GE} = \frac{\beta + A\beta^2}{\Delta\beta + A(\Delta\beta)^2}$$

$A \gg \beta$ therefore β and $\Delta\beta$ are negligible

$$\frac{\Delta GE}{GE} = \frac{A\beta^2}{A(\Delta\beta)^2} = \left(\frac{\beta}{\Delta\beta}\right)^2 = \left(\frac{1}{1.02}\right)^2 = 0.96 \qquad \textbf{12}$$

Equation 12 shows that even using 1% tolerance resistors can result in a 4% error in the gain error. The error contributed by resistor mismatch can dominate this measurement if the gain ratio is not measured precisely. For this test measuring the resistor when possible will result in a more accurate gain error measurement.

Input Offset Voltage

In ideal op-amps, the output of the amplifier is identical to the input multiplied by the gain factor of the feedback network. This means that an input signal at zero should also be zero on the output; this is not the case in real op-amps. Due to mismatch from process variation the output will not perfectly track the input. The op-amp will behave as if there is a small voltage applied to the input. This input referred offset voltage is usually between a few millivolts and a few hundred microvolts. The amplifier gain will be applied to this offset voltage and can result in substantial offsets in high gain configurations.

While some offset is expected, it can also be a symptom of bad design or inaccurate device models [3]. For this reason, testing Offset voltage is an important step in evaluating the strength and stability of an op-amp.

The standard configuration for measuring the input referred offset voltage is the traditional feedback network. This circuit can amplify the offset voltage several orders of magnitude to make it clearly distinguishable from the other non-idealities in the op-amp. One related effect that can interfere with this test is the bias current. It is important to choose the resistors such that the input offset current is not amplified along with the offset voltage. Due to this interaction, these two tests need to be considered together [5].

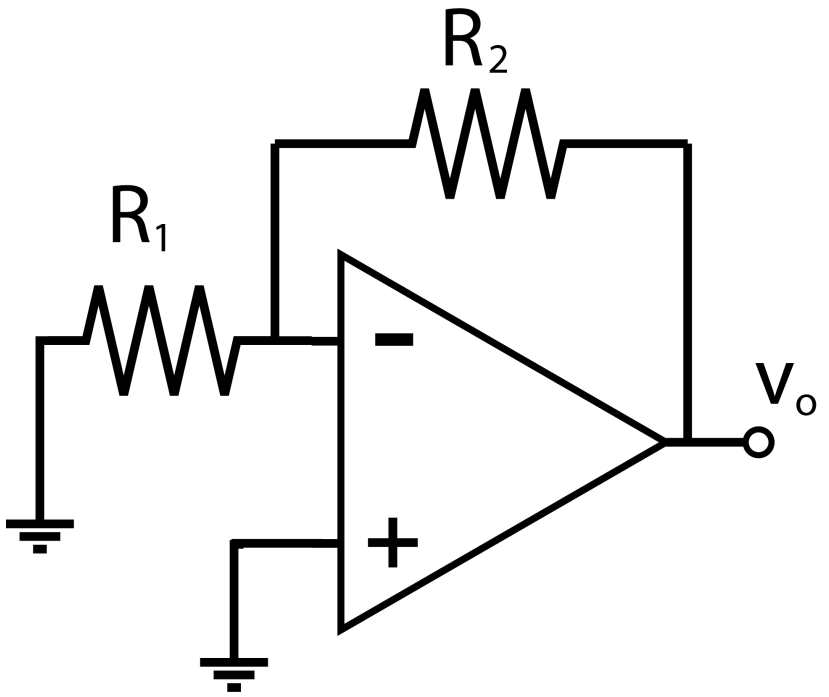

Figure 5 Offset Voltage Measurement Circuit Configuration

Input Bias Current and Input Offset Current

The Input Offset and Bias currents are generally negligible in MOSFET based amplifiers, but can make a noticeable contribution in op-amps with BJTs on the inputs. Input currents can range from microamps in BJTs down to femtoamps in FETs. Both the input bias current and input voltage offset will manifest as a voltage on the output. While testing the input bias current and input voltage offset the feedback network can be sized to have one effect dominate over the other.

The output voltage that results from the bias current is a product of the feedback resistor and the bias current $I_B R_2$. The input referred offset voltage is a product of the gain on the amplifier $A_v V_{OS}$. The combined output voltage due to offset voltage and bias current is given in **(**13**)** [1][5]. To maximize the effect of the bias current while minimizing the effect of the offset voltage, the feedback resistor should be large (1MΩ), but the amplifier gain should be small.

$$V_o = I_B R_2 \pm V_{OS}\left(1 + \frac{R_2}{R_1}\right) \qquad \textbf{13}$$

Conversely, to maximize the effect of the offset voltage while minimizing the interaction from the bias current, the gain should be large (10~100) and the feedback resistors should be small (100Ω~1kΩ). Following these guidelines the

bias current should come directly from **(**14**)** and the offset voltage can be calculated with **(**15**)**.

$$I_B = \frac{V_o}{R_2} \quad \textbf{14}$$

$$V_{OS} = \frac{V_o}{A_v} \quad \textbf{15}$$

The input offset current, like the offset voltage, can come from mismatch, both systematic and random, in the amplifier. In the previous circuit configuration (Figure 5) the effect of the positive terminal bias current is nulled by the direct ground connection. To measure the input current offset, both currents must be acting on the amplifier. The circuit configuration in Figure 6 achieves this by introducing a resistor on the positive terminal to generate a voltage due to the bias current. The voltage on this terminal will be subject to the gain of the amplifier. The output voltage from the bias currents will be

$$V_o = I_{B-}R_2 - I_{B+}R_B\left(1 + \frac{R_2}{R_1}\right) \quad \textbf{16}$$

if R_B is sized to be the parallel combination of R_1 and R_2 then the equation simplifies to

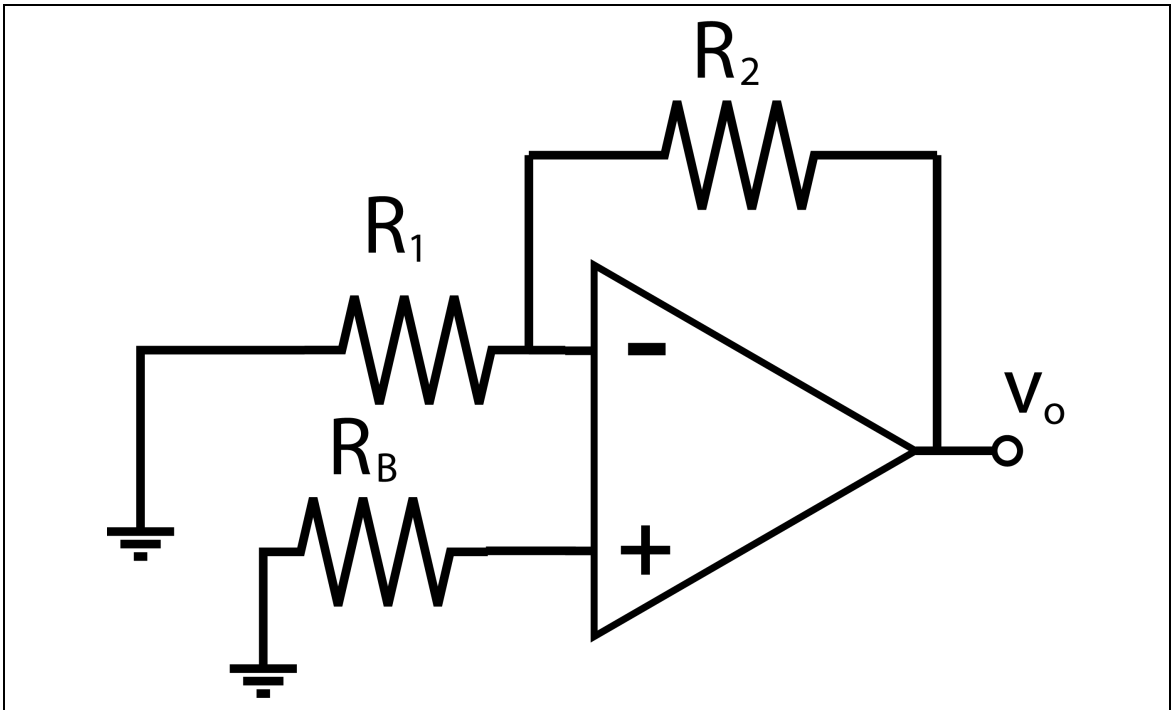

Figure 6 Input Bias Current Offset Measurement Circuit Configuration

$$V_o = (I_{B-} - I_{B+})R_2 \quad \textbf{17}$$

the offset current (I_{OS}) is then the difference of the bias currents [5].

Open-Loop Gain

There are many different methods for measuring open-loop gain. This measurement is challenging because most amplifiers are not designed to operate in the open loop configuration. Even when the inputs are tied together, the open-loop gain of modern amplifiers is large enough to cause the op-amp output to hit a supply rail due to the offset voltage on the input. One circuit configuration (Figure 7) tries to measure the components of the gain equation directly.

$$V_o = A_{OL} v_e \quad \textbf{18}$$

$$A_{OL} = \frac{V_O}{v_e}$$

It follows that the gain on the output will also appear across the error voltage (this is where the gain comes from after all). It is important to size the resistors to minimize loading, but this method is plagued by the difficulty of measuring the error voltage accurately. Another circuit that can be used to approximate a direct measure of open-loop gain is shown in Figure 8 [6]. At DC this is a unity gain configuration that provides feedback to bias the circuit. At higher frequency the

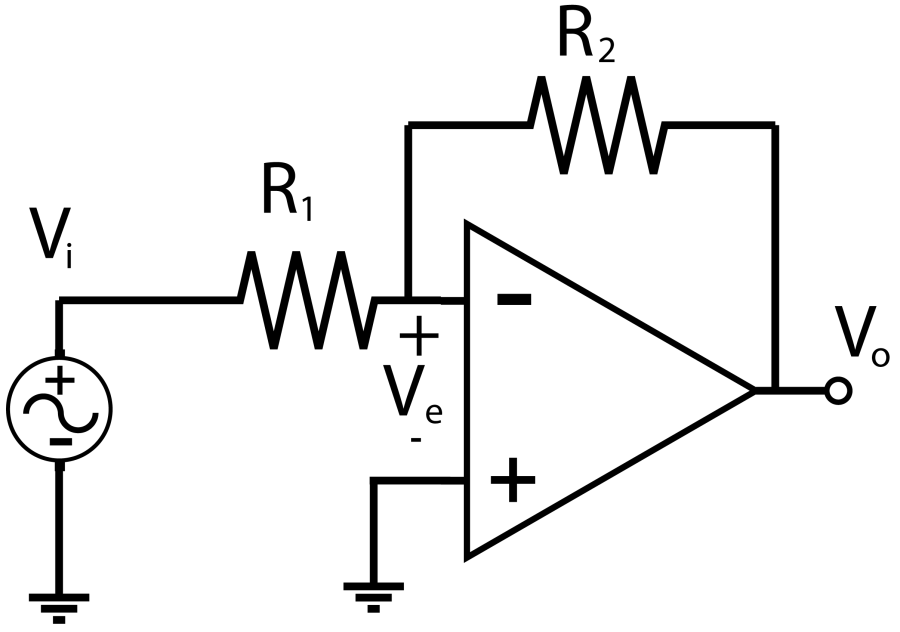

Figure 7 Simple Open-Loop Gain Measurement Circuit

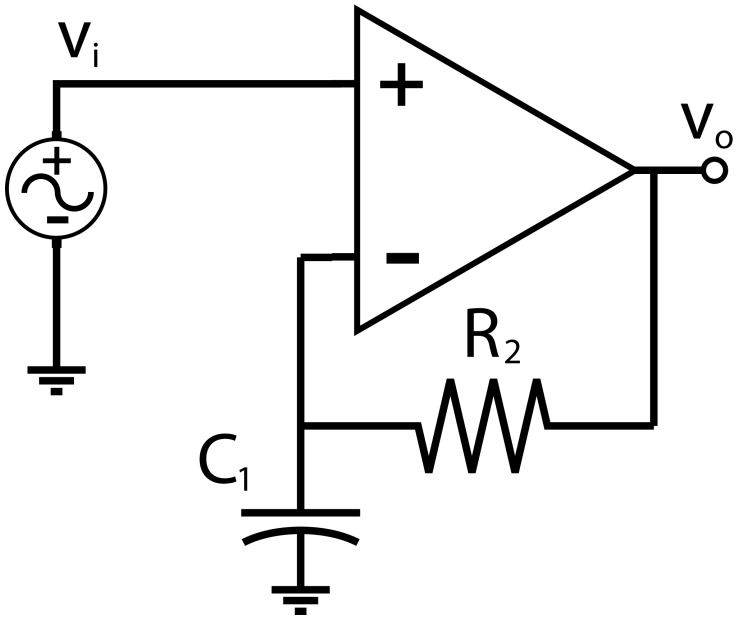

Figure 8 Open-Loop Measurement Circuit with RC Feedback

gain ramps up at 20dB/decade until it intersects the open-loop gain.

An important data point to capture in the open-loop gain measurement is the dominant pole frequency. If the RC network is not sized properly, the transition from the RC network dominating the gain to the amplifier will occur after the dominant pole. In order to properly size the RC feedback network for this circuit (Figure 8) a rough idea of the open-loop gain of the op-amp is required. The open loop gain with a single pole is represented as

$$A_{OL}(j\omega) = \frac{A_0\omega_0}{j\omega + \omega_0} \quad \textbf{19}$$

The RC network will add a pole to the op-amp transfer function of the form

$$A_v(j\omega) = 1 - j\omega RC \quad \textbf{20}$$

The closed-loop gain of the amplifier incorporates the frequency dependent open-loop gain and the feedback factor β

$$A_v(j\omega) = \frac{A_{OL}(j\omega)}{1 + A_{OL}(j\omega)\beta} = \frac{A_0\omega_0}{j\omega + \omega_0(1 + A_0\beta)} \quad \textbf{21}$$

The feedback factor (β) of the RC network

$$\beta = \frac{\frac{1}{j\omega C_1}}{\frac{1}{j\omega C_1} + R_2} = \frac{\frac{1}{j\omega C_1}}{\frac{1 + j\omega R_2 C_1}{j\omega C_1}} = \frac{1}{1 + j\omega R_2 C_1} \qquad \textbf{22}$$

Substituting (22) in to (21) yields

$$A_v(j\omega) = \frac{A_0 \omega_0 (1 + j\omega R_2 C_1)}{\omega_0 (A_0 + 1) + j\omega (1 + R_2 C_1 \omega_0) - \omega^2 R_2 C_1} \qquad \textbf{23}$$

In order to maintain stability and avoid masking the dominant pole, the gain RC ratio should be less than the dominant pole

$$\omega_0 > \frac{A_0}{R_2 C_1} \qquad \textbf{24}$$

Or as frequency

$$f_0 > \frac{A_v(DC)}{2\pi R_2 C_1} \qquad \textbf{25}$$

The resulting Bode plot of the op-amp and the RC network should resemble Figure 9. In this example the RC network has a frequency of 10 Hz and the first pole of the op-amp is at 10 kHz. That leaves one decade between the open-loop gain / RC transition and the first pole of the op-amp. There are a few of requirements for successful testing with this circuit. All of them revolve around the interaction between the feedback network and the dominant pole.

The op-amp must have sufficiently *low* gain so that there is no interaction between the RC network and the dominant pole [6]. This circuit can oscillate if that condition is not met. In conjunction, it is necessary to size the RC network so that the amplifier open-loop gain is dominating before the low frequency pole.

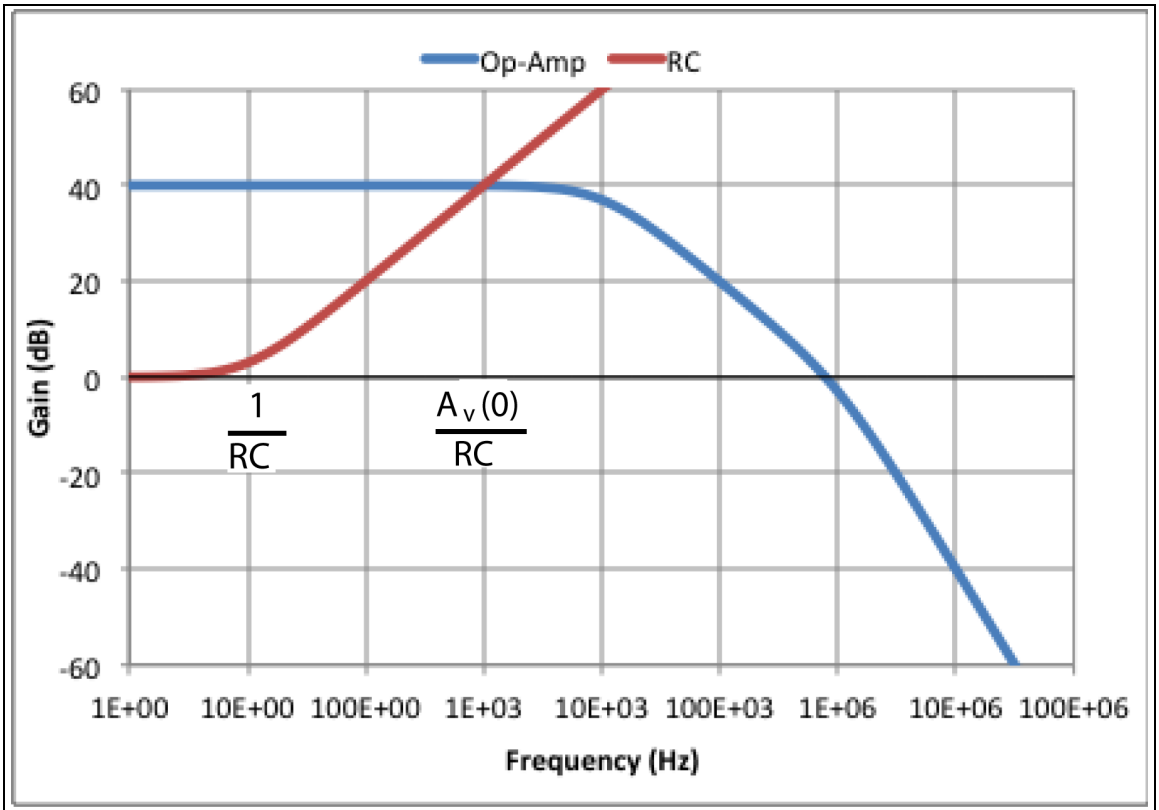

Figure 9 Op-Amp Bode Plot with RC Transfer Function Overlaid

A more robust circuit for measuring open-loop gain uses a buffer in the feedback path, a resistive divider on the input of the DUT and applies the input signal to the output of the DUT (Figure 10) [6]. This circuit overcomes the difficulty of measuring the error voltage by applying a 1000x gain factor to it. V_{test} is applied to the output of the DUT which is the input of the buffer. The output of the buffer drives the input of the DUT through a resistive divider. The DUT will stabilize the loop by matching the V_{test} signal on the output. The open-loop gain can be found by measuring V_{OS} and performing the calculation

$$A_{OL} = \frac{1000 v_{test}}{V_{OS}} \qquad \textbf{26}$$

An AC signal can be used for V_{test}. This can be swept to find the open-loop gain as a function of frequency.

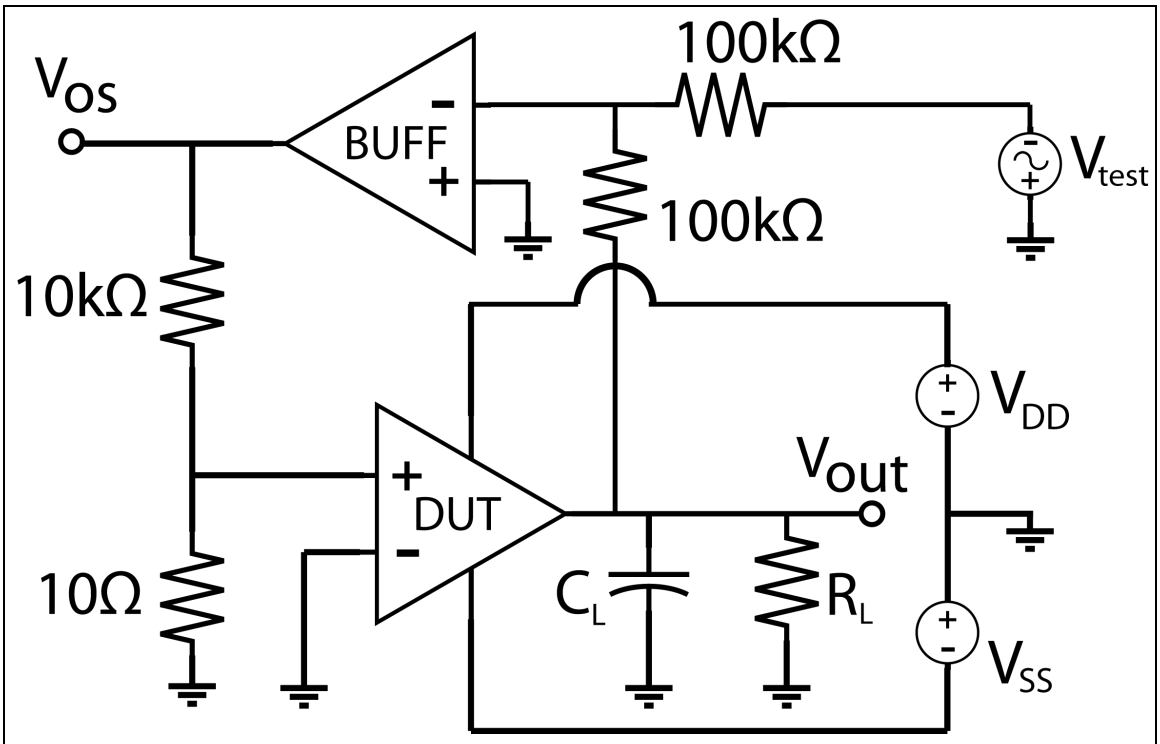

Figure 10 Buffered Open-Loop Gain Measurement Circuit

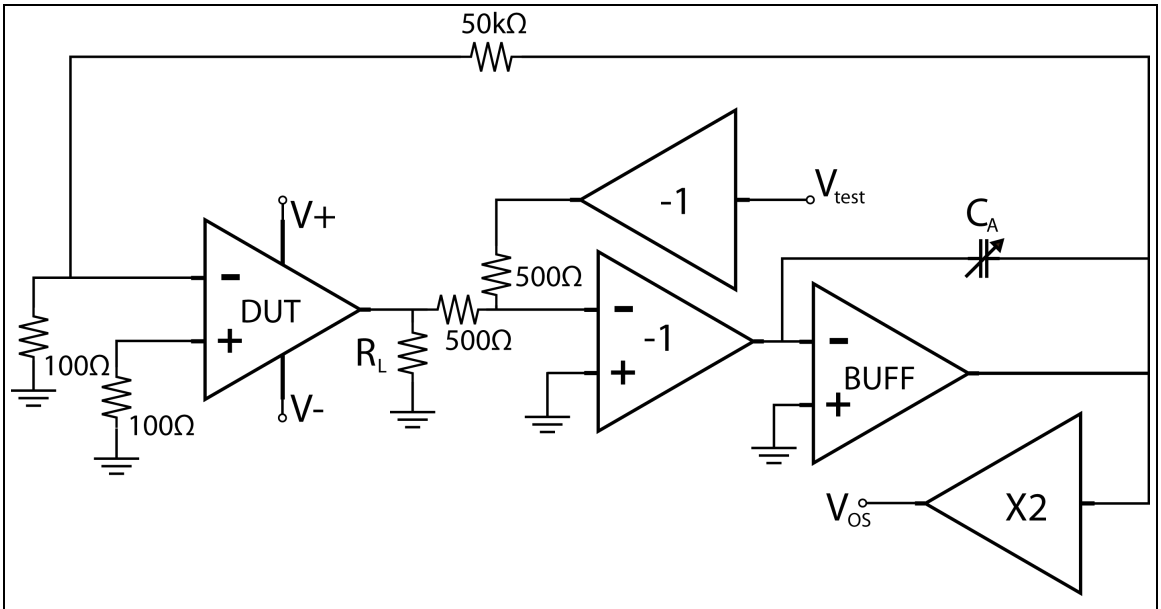

Figure 11 Buffered DUT Output, Feedback and Stabilization for Open-Loop Testing

While the open-loop test configuration in Figure 10 can be a good compromise of accuracy and complexity, this configuration can still be limited by the non-negligible output resistance in the DUT. A third option for testing is shown in Figure 11 [7]. Functionally this configuration is very similar; an inverting buffer is driving a voltage divider on the input of the DUT. This configuration is more robust due to the addition of buffers for the input signal, the output measurement signal and the stability loop. The formula for deriving open-loop gain is, again, very similar to that of the previous test configuration.

$$A_{OL} = \frac{1000 v_{test}}{V_{OS}} \qquad \textbf{27}$$

Common Mode Rejection Ratio (CMRR)

The Common Mode Rejection Ratio (CMRR) is closely tied to the open loop gain. CMRR is the ability of an op-amp to reject a signal that is common on the inputs. Op-amps are often used in differential signaling systems where they have to be able to pull a small differential signal from a sea of electrical noise.

Because the CMRR is tied to the open loop gain this test also requires a more involved test circuit. The circuit shown in Figure 12, like the A_{OL} test, uses a second op-amp in the feedback path to drive a resistive divider on the input of the device under test (DUT) [6]. The V_{OS} node on this circuit gives a 1000x view of the differential input voltage. During the test procedure the V_{test} sources are all changed by the same amount simultaneously to force a common-mode voltage on the op-amp. If the output of the DUT shifts due to non-zero common-mode gain, then that voltage will be summed with the V_{test} signal going to the buffer. The difference will be buffered and fed back through the resistive divider. Due to the divider the V_{OS} voltage will be 1000 times greater than the voltage on the input of the DUT thus allowing an (approximately) direct measurement of the v_{iD} voltage.

$$CMRR = \frac{1000 v_{test}}{V_{OS}} \qquad \textbf{28}$$

The v_{test} signal can be implemented with either a positive and negative DC step of an arbitrary value or it can be a swept AC signal and CMRR across frequency can be characterized.

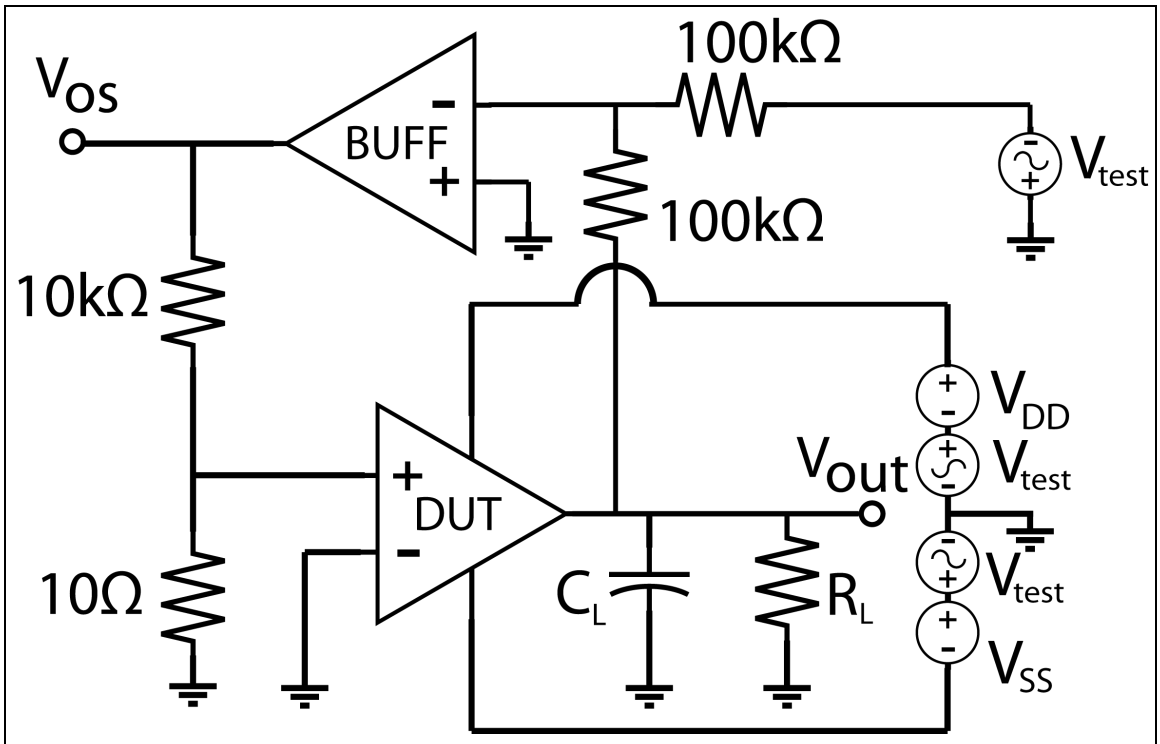

Figure 12 CMRR and PSRR Test Circuit Configuration

Power Supply Rejection Ratio (PSRR)

The Power Supply Rejection Ratio is similar to the Common Mode Rejection Ratio in that it is a ratio of unintended signal amplification versus the total open-loop gain of the op-amp. While functionally this is measuring a different mechanism for corrupting the output, the test circuit that was used for CMRR (Figure 12) can be reused for this test. To measure PSRR just step up the voltage on one of the power supply rails and measure the V_{OS} node. Then step it down by the same amount. The PSRR can be calculated using

$$PSRR = \frac{2000}{|V_{OS-} - V_{OS+}|} \qquad \textbf{29}$$

the same equation can be used when finding the negative PSRR. It is also possible to use an AC source and sweep the frequency on the on the power supply rails to characterize PSRR over frequency. That is similar to the CMRR equation.

$$PSRR = \frac{1000v_{test}}{V_{OS}} \qquad \textbf{30}$$

Input and Output Common-Mode Range

The input and output common-mode ranges correspond to the voltage levels on the input and output of the amplifier that can be passed without distortion. Input common-mode range can be measured with a simple unity-gain configured op-amp. The input voltage is swept linearly from the negative rail to the positive rail while the output voltage is recorded. The input common-mode range will be the span of the sweep where the output matches the input. In the example (Figure 14) the ICMR would be -3.8V to 4V.

The test for the output common-mode range is similar, but requires a gain of around 10. Without a gain factor the input common-mode range would dominate this test. Again the test procedure is sweeping the input voltage and recording the output. The input voltage sweep range should be within the rails divided by the gain factor [6]. Figure 13 shows a typical output voltage range measurement.

Transient Response

The transient response of an op-amp is one of the most realistic tests that are used to characterize an amplifier. The transient response will reveal the rise time, fall time, overshoot, and settling time or possible oscillation. These tests are fairly simple to execute as long as the op-amp can be measured with an oscilloscope.

To characterize the worst-case scenario for an op-amp, a non-inverting unity gain configuration should be used [1][3]. In this configuration the op-amp has maximum bandwidth and maximum feedback. The full feedback from the output can expose stability issues in the amplifier. There are certain high-performance amplifiers that are designed to operate exclusively in high gain configurations and will become unstable if used in a unity gain mode. For these op-amps, the lowest stable non-inverting gain configuration is the one to use.

Most contemporary oscilloscopes will automatically capture all of the key features of the step response, but being able to verify results is always important. Figure 15 is a standard step response plot. The four parameters to extract from this measurement are the rise time (τ_r), overshoot (M_{pt}), settling time (T_s) and the time of the first overshoot peak (t_p).

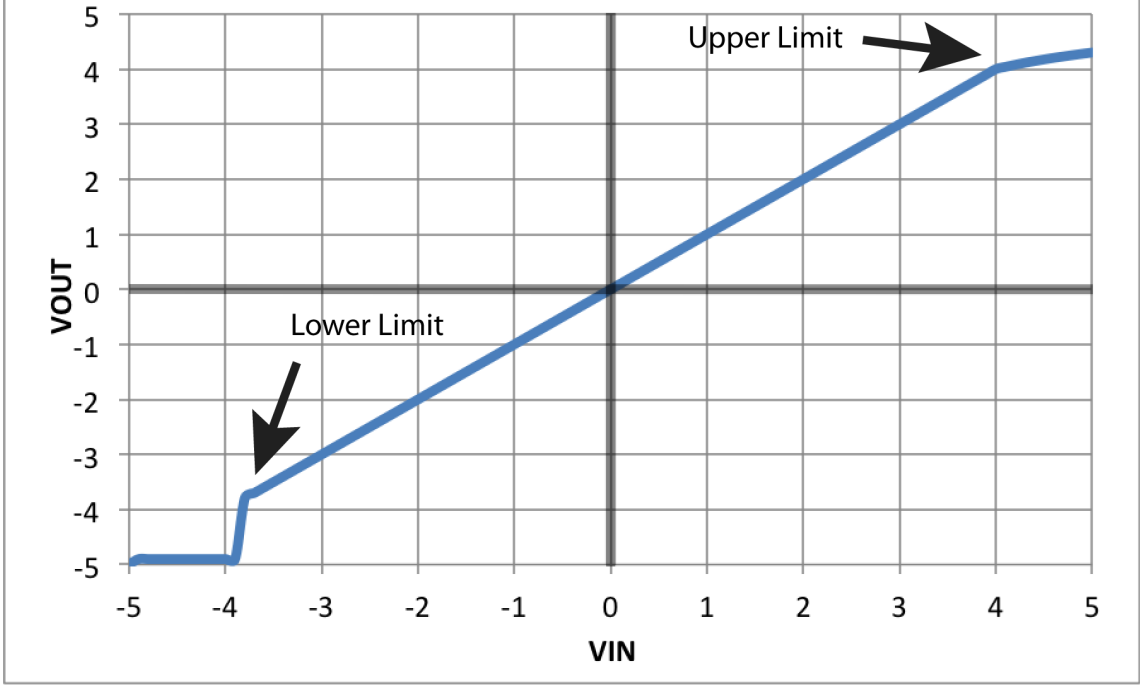

Figure 14 Typical ICMR Measurement

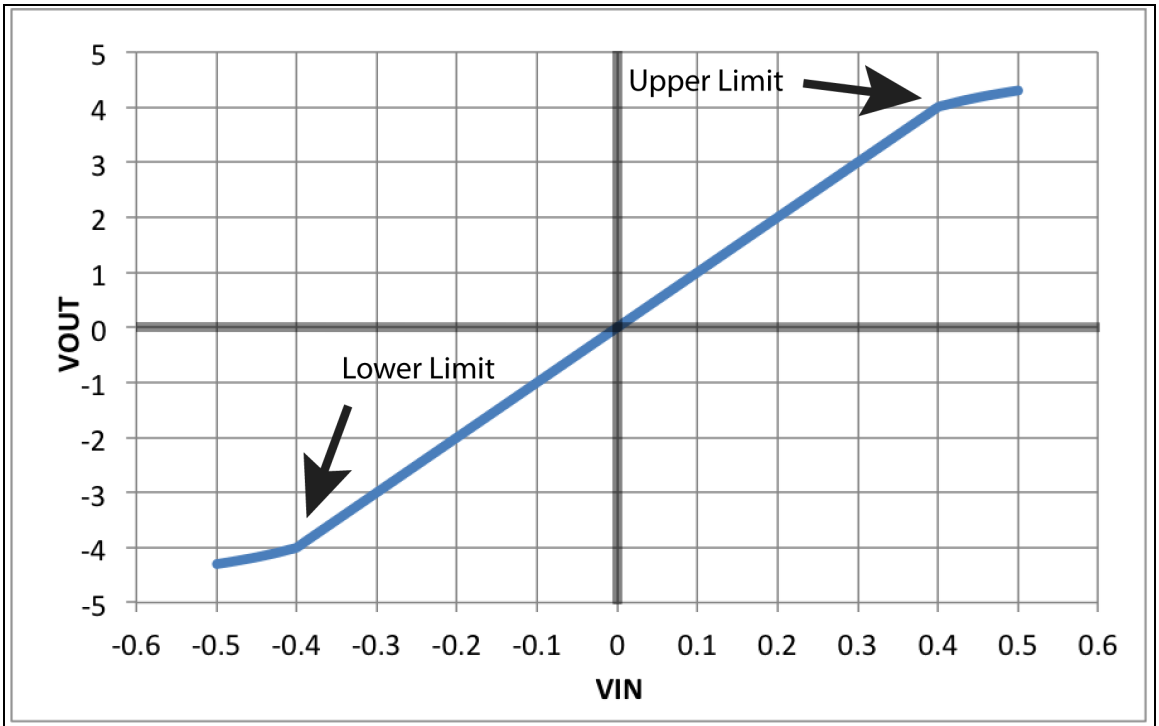

Figure 13 Typical Output Voltage Range Measurement

These data points can be related to the frequency domain response of the op-amp. The first step is to fit these parameters to the Laplace Transform step response. The time domain form of the transform is

$$L(t) = 1 - \frac{e^{-2\pi\zeta f_0 t}}{\sqrt{1-\zeta^2}} \sin\left[\left(2\pi f_0\sqrt{1-\zeta^2}\right)t + \cos^{-1}\zeta\right] \qquad \textbf{31}$$

All four of the measured parameters can relate to the two variables in the step response. The overshoot relates to the damping ratio (ζ) through

$$M_{pt} = 100e^{-\left(\frac{\pi\zeta}{\sqrt{1-\zeta^2}}\right)} \qquad \textbf{32}$$

The peak overshoot time is related to the damping ratio (ζ) and the corner frequency (f_0) through

$$t_p = \frac{1}{\left(2f_0\sqrt{1-\zeta^2}\right)} \qquad \textbf{33}$$

The settling time (T_s) is defined as the time required to reach 2 percent of the final value this relates to the damping ratio (ζ) and the corner frequency (f_0) through

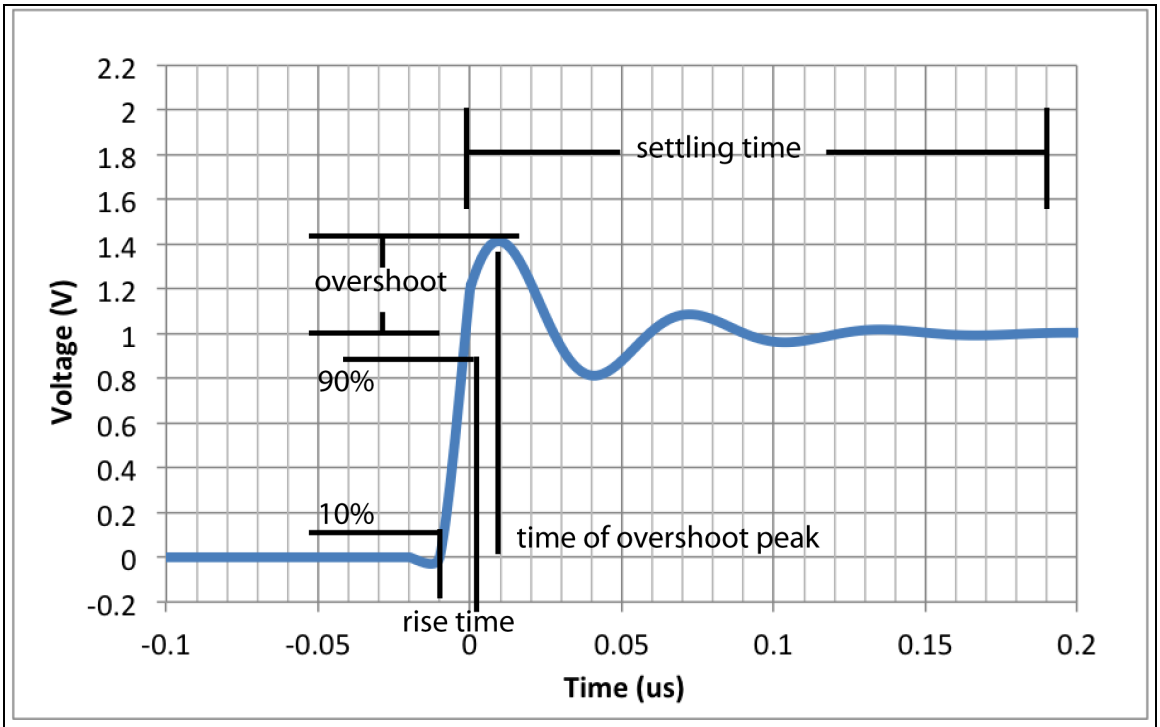

Figure 15 Step Response with key features annotated

Table 1 Time Domain - Frequency Domain Conversion Table

ζ	P.M.	$f_c t_p$	$f_{hi(f)}\tau_r$	$f_c \tau_r$	M_{pt}	$T_s f_c$
0	0°	0.5				∞
0.1	11.4°	0.49	0.28	0.18	73%	6.30
0.2	22.6°	0.47	0.29	0.18	53%	3.06
0.3	33.4°	0.44	0.29	0.19	37%	1.94
0.4	43.3°	0.4	0.32	0.2	25%	1.36
0.5	52°	0.36	0.34	0.21	16%	1.00
0.6	59°	0.32	0.35	0.22	9%	0.76
0.7	65°	0.29	0.36	0.23	5%	0.59
0.8	70°	0.29	0.34	0.23	2%	0.47
0.9	74°	0.33	0.34	0.24	0.2%	0.38
1.0	77°				0%	0.31

$$T_s = \frac{2}{(\pi \zeta f_0)} \qquad \textbf{34}$$

The rise time (τ_r) is defined as the time required to go from 10% to 90% of the final value. It relates to the corner frequency (f_0) through

$$f_0 \tau_r = f_0(t_2 - t_1) \qquad \textbf{35}$$

this equation **(**35**)** is used to confirm the accuracy of the previous equations **(**32**-**34**)**. The validity of the other data points can be confirmed by plotting **(**31**)** and using $f_0 t_2$ and $f_0 t_1$ as test points. At those points the step function should equal 0.9 and 0.1, respectively.

For a more complete explanation on relating measured parameters in one domain (time or frequency) to characteristics of the other refer to [2].

Input Common Mode Range using Transient Analysis

The aforementioned ICMR test is a simple method for determining the limits of input signal swing. It does not address variations in bandwidth and stability that correspond with the shifted common mode voltage. To account for these changes, a test combining the ICMR and step response methods can be used. This test consists of applying a small signal square wave to the input of the op-amp similar to the Transient Response test, the difference is that the common mode voltage is swept and the transient response data is recorded at a range of common mode voltages. Through this test it will be clear that the gain and

bandwidth of the amplifier is not constant through the entire input common-mode range.

Slew Rate

Slew rate is a measure of the large signal response of the output stage of the amplifier. When measuring the slew rate of the op-amp it is advisable to use gain (approx. 10V/V) to drive the output into large signal operation without pushing the input stage out or small signal operation [3][5]. In order to keep the output drivers from shutting off, it is wise to leave a little headroom for the output devices. Keeping a few hundred millivolts to one volt from the rails should prevent this from happening.

The slew rate calculation is a simple linear slope equation **(**36**)**

$$SR = \frac{V_2 - V_1}{t_2 - t_1} \qquad \textbf{36}$$

Generally slew rate is expressed as Volts per microsecond $(V/\mu s)$.

Full Power Bandwidth

Full Power Bandwidth is the highest frequency that an amplifier can drive full scale [1]. This is directly related to the slew rate of the amplifier. It is generally hard to detect when a sine wave starts slewing because it will start as a small linear stretch around the zero crossing. By the time the slewing is visible on a sine wave it will have severely corrupted the signal. For that reason it is best to calculate the full power bandwidth from the slew rate. The slew rate (SR), full power bandwidth (f_M), and full-scale voltage (V_{FS}) are related through **(**37**)**

$$f_M \leq \frac{SR}{2\pi V_{FS}} \qquad \textbf{37}$$

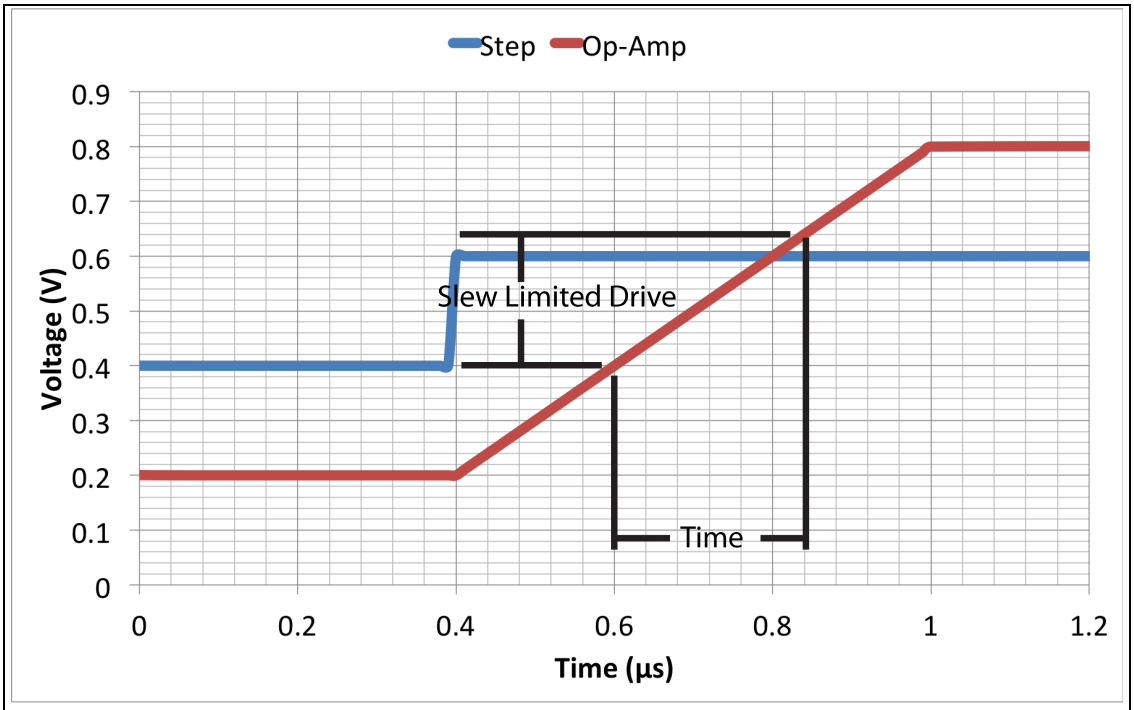

Figure 16 Slew Rate Limited Op-Amp Response

CHAPTER III
DATA COLLECTION AND PROGRAMMING

An Introduction to LabVIEW

A brief overview of the LabVIEW programming environment will be instrumental in streamlining the rest of this paper. The LabVIEW environment consists of two views or windows. There is the Front Panel and the Block Diagram (Figure 17). The Front Panel is the user interface. This window will display data and provides an interface for the user to manipulate program variables. The Block Diagram is the programming side. As the name implies, this is supposed to emulate simple block diagrams or flow charts. In this language the programs are read from left to right with lines or "wires" representing data flow. The individual programs are called virtual instruments (VIs).

In the block diagram there are various blocks, icons and patterns. These symbols can be classified as:

- Controls - visible to the user on the Front Panel, controlled or altered while the program is running
- Constants - these are hard-coded values that do not change while the program is running
- Operators - simple to moderately complex functional blocks, such as multiplication or array sorting
- Structures - conditional statements, switches, loops, event driven selections
- Sub VIs - equivalent to a function in traditional languages
- Indicator - visible to the user on the Front Panel, can display data as an individual value, table of values, or a graph

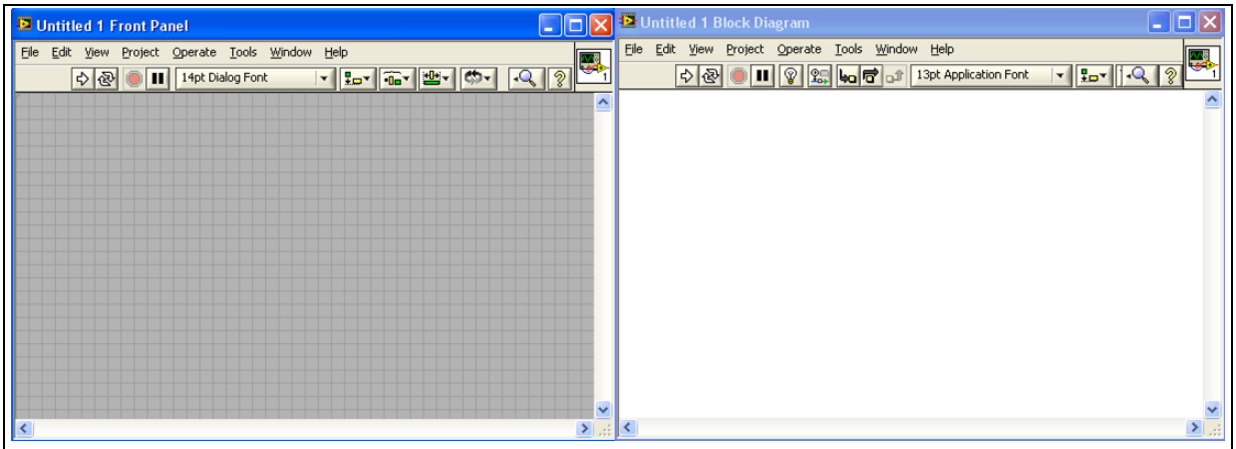

Figure 17 Front Panel and Block Diagram

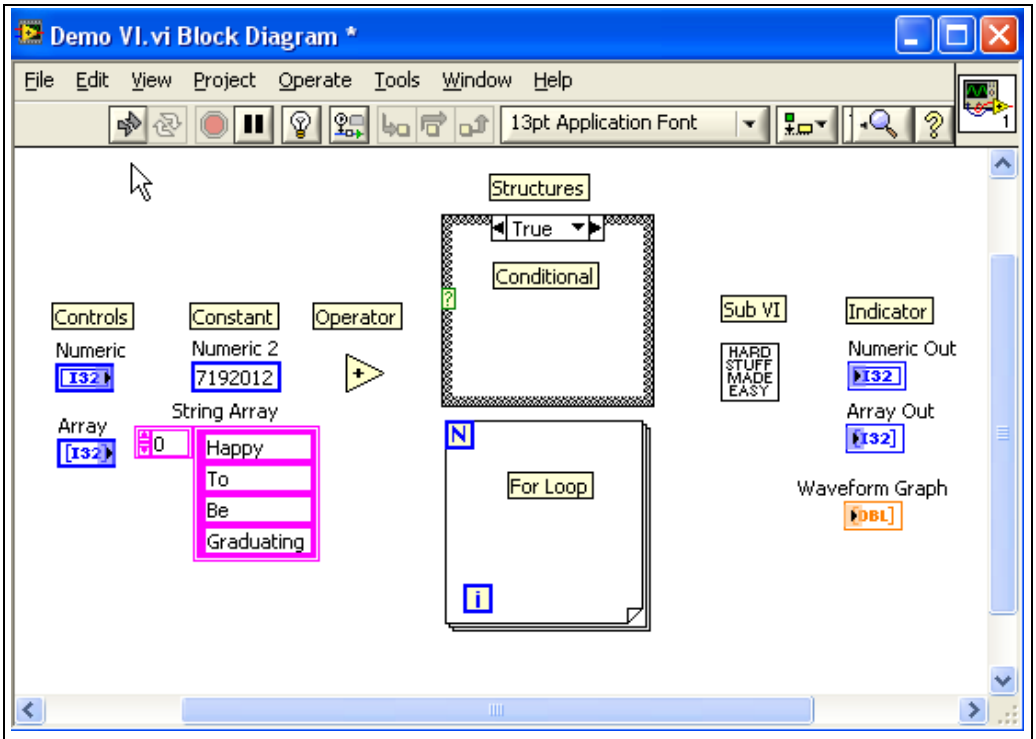

Figure 18 Controls, Constants, Operators, Structures, Sub VIs, and Indicators

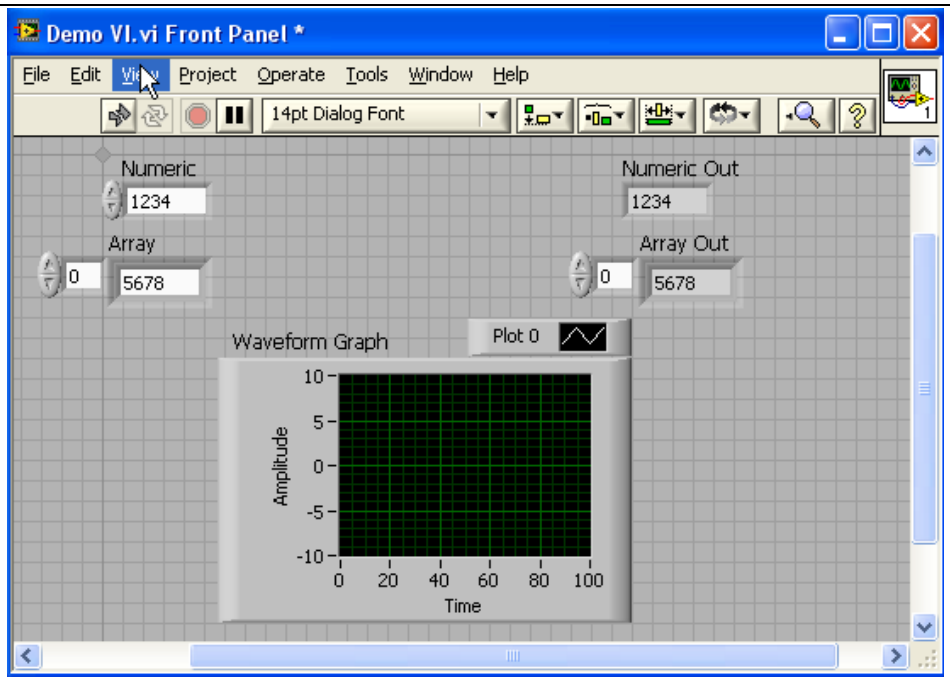

Figure 19 Front Panel Controls and Indicators

The appearance of most of these symbols is standardized by type and function. The various colors are used to differentiate data types: blue for integers, pink for strings, orange for double precision numbers. Figure 18 shows the various symbols and Figure 19 shows the Front Panel with the corresponding controls and indicators.

LabVIEW's strength, in terms of testing, is the immense library of test instrument functions. A program can be written in 12 mouse clicks to capture data from a multimeter or oscilloscope. Part of the simplicity is that the user interface is created as a byproduct of writing the program instead of being an extra step performed after the programming is finished.

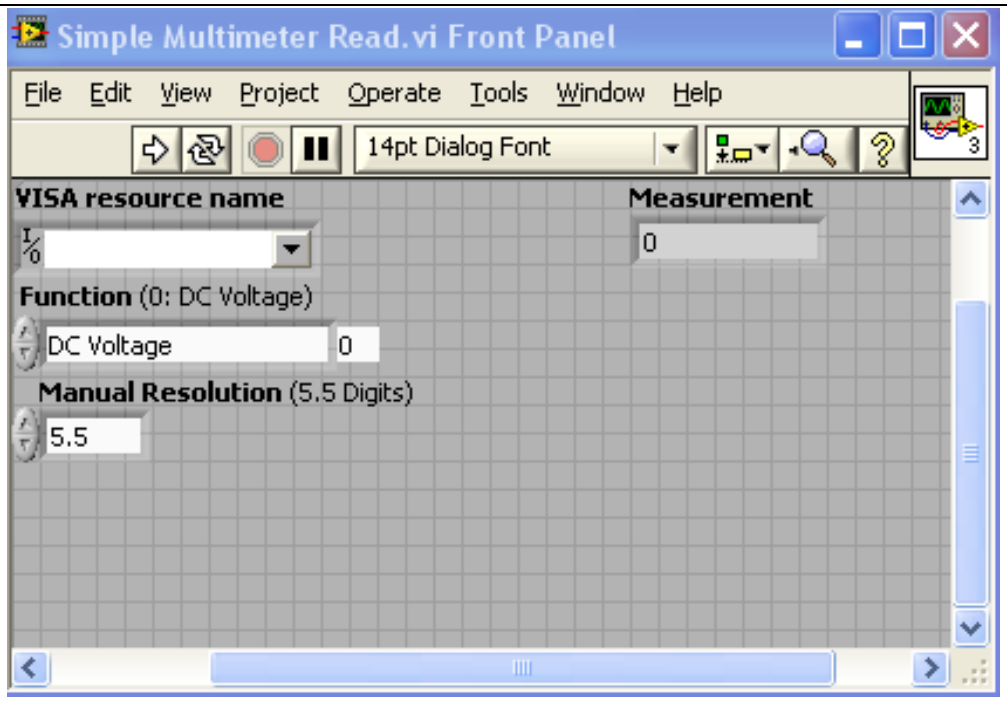

Figure 20 Simple multimeter data collection user interface

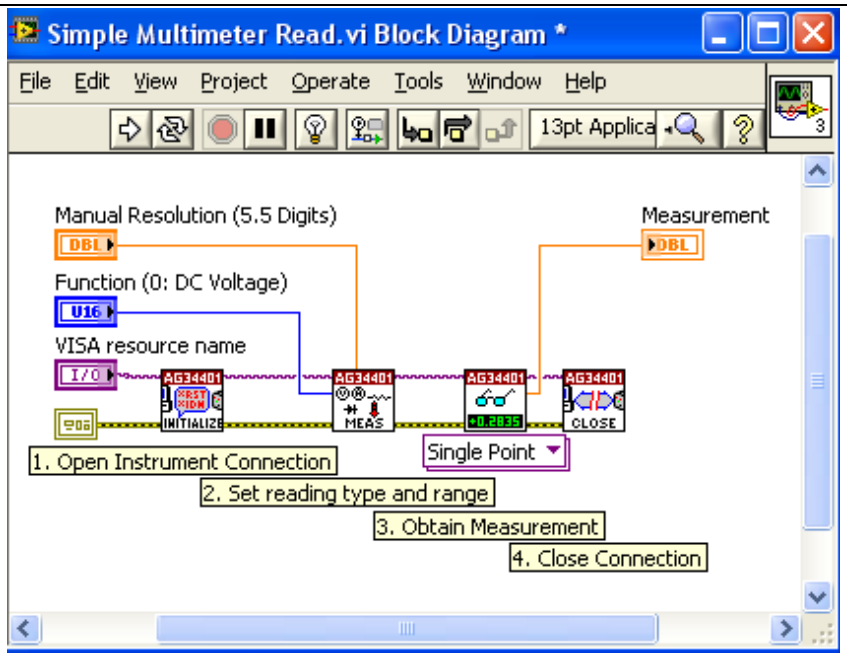

Figure 21 Simple multimeter data collection program

Data Collection Basics

Linear Devices and Simple Sweeps

A common exercise for the novice electrical engineer is to measure and observe the linear relationship between voltage and current on a resistor. This exercise is a good starting point for collecting data through an automated system. Using a voltage source, an ammeter, and a resistor, LabVIEW can be programmed to set a voltage on the source and then read back the current measurement on the ammeter. By putting this in an iterative loop, a range of voltages can be swept and the corresponding currents recorded.

Figure 22 is an example of the automated resistor sweep. In this VI there are three distinct functional paths. The top path is the multimeter functions; below that, the power supply; and on the bottom, in orange, the controls for the starting voltage, stopping voltage and the number of points to collect. On the right side of Figure 22 are the output arrays: current measurement and the programmed voltage. Figure 23 is the front panel setting for sweeping a 1 kΩ resistor. On the front panel, the GPIB addresses for the test instruments and the sweep parameters must be set. Then after the program finishes the data is output in the arrays on the right side of the figure. While displaying data in an array is functional it does not always reveal trends as readily as a plot would. And since graphs are an engineer's best friend an easy way to improve this program is to wire the data into a scatter plot (XY graph in LabVIEW).

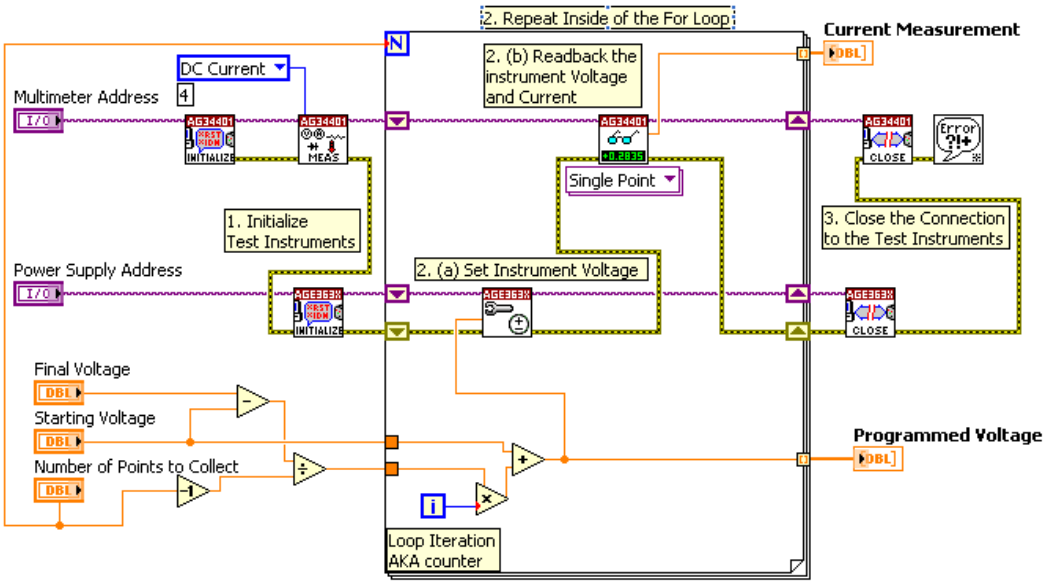

Figure 22 Basic Resistor Sweep I-V Curve

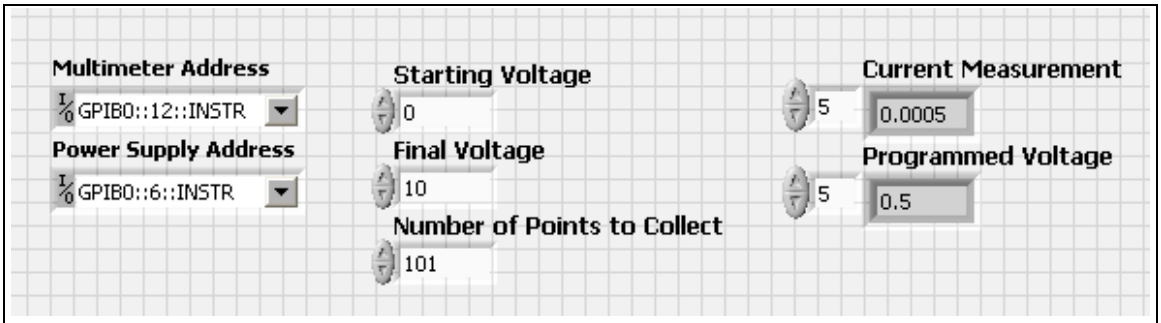

Figure 23 Results of sweeping a 1k resistor

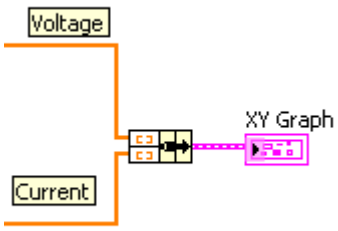

Figure 24 Bundling to data wires into a cluster and sending it to a graph

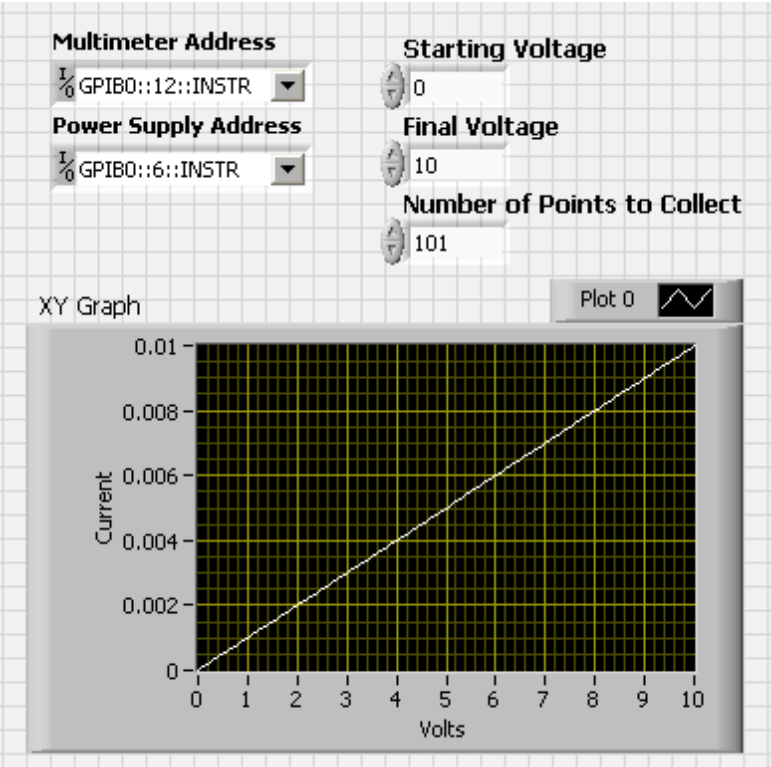

Figure 25 Resistor Sweep with Graph

Active Devices and Nested Loops

In three terminal devices, like transistors, there is an extra degree of control required. The potential of the drain and gate must be set with respect to the source of the transistor. Generally testing of these devices will involve holding one terminal constant while sweeping the other. The sweep is then repeated as the holding terminal is stepped through a range of values. This will produce a family of curves, similar to a curve tracer. To achieve this programmatically requires the use of nested loops

A multi-sweep program can be coded up with only a few minor tweaks to the resistor sweep program. First, an outer loop must be drawn around the existing For Loop to account for the extra variable. Secondly, because there is a second variable to sweep, another set of start, stop, step number controls and the associated step iterator must be created (or copied). Third, another voltage source must be added. Because the instrument used in this example has multiple channels, the same instrument can be used. In this example channel 1 controls v_{DS} and channel 2 controls v_{GS}. Fourth, due to the extra dimension of data that comes from a nested sweep, the data should be bundled on the output of the inner loop, so that each curve in the family is distinct from the other.

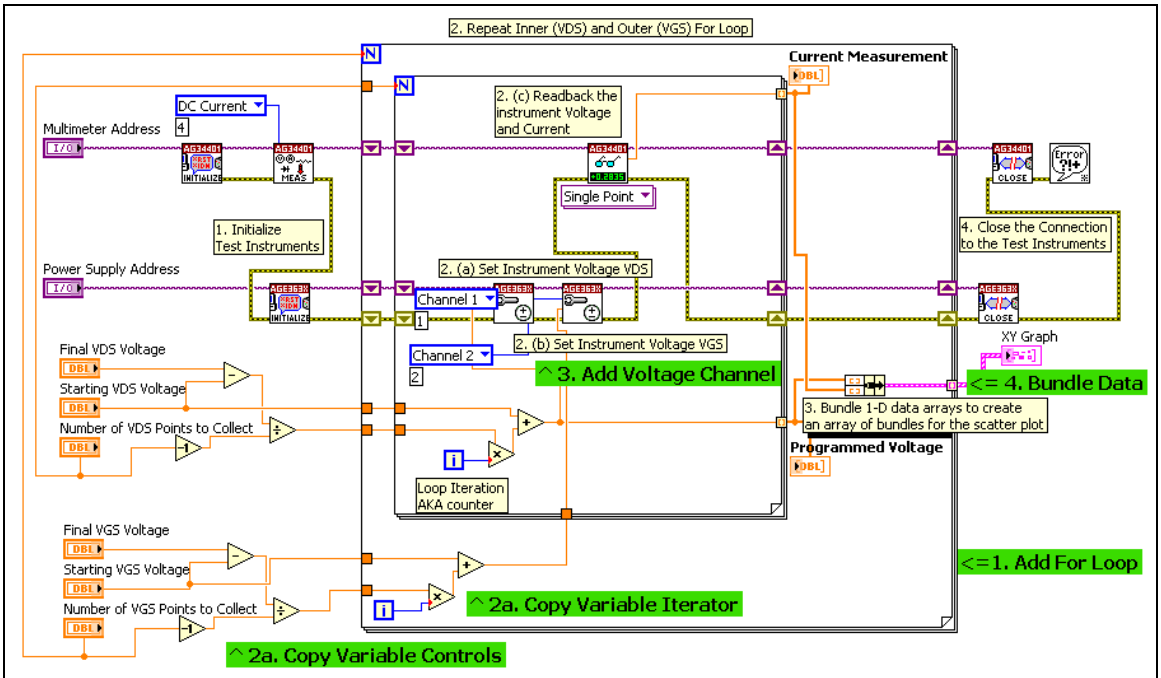

Figure 27 Transistor Curve Tracer using a nested sweep

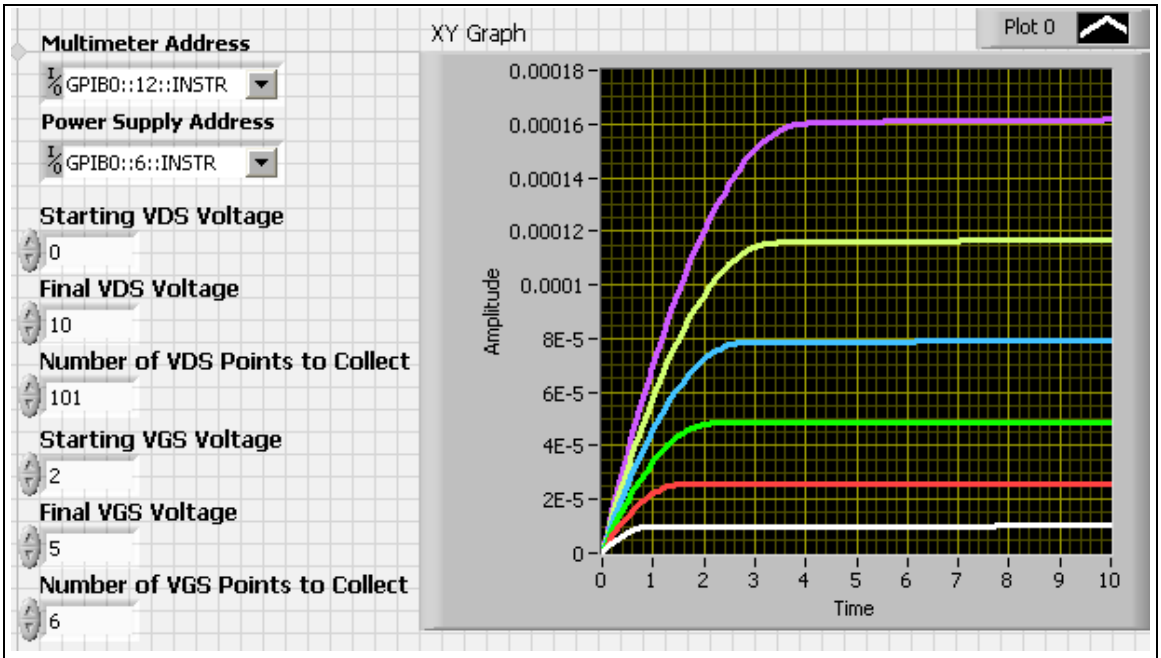

Figure 26 Transistor I-V Curve VDS Sweep

With these changes the basic sweeping program has been converted into a curve tracer like program. Figure 26 shows the resulting I-V curves. This preceding program will perform one of the tests necessary for characterizing a transistor. The second test is the V_{gs} sweep. The program from Figure 27 Transistor Curve Tracer using a nested sweep can be converted into a V_{gs} sweeper by switching channels 1 and 2 on the voltage source and, accordingly, switching the names on the VDS and VGS controls. After making those changes the program would produce results similar to Figure 29. By zooming in near the x-axis an approximate value of threshold voltage can be found (Figure 28).

Once an approximate value for the threshold voltage is found, the transconductance parameter can be solved for. The accuracy of these data points can be verified by comparing the measured transistor I-V curves to ideal transistor I-V curves with the extracted parameters. LabVIEW does not have a transistor model built in, so one must be programmed.

To build a mathematical transistor model in LabVIEW, the saturation (1) and linear region (**2**) equations will be used. The "formula" express VI block can be used to enter arbitrary algebraic expression. Figure 30 is one view of the mathematical transistor model. The conditional statements are used to decide the region of operation. The outer case structure evaluates $V_{DS} > V_{gs} - V_{TN}$ for saturation or linear region. The inner case structure evaluates $V_{gs} > V_{TN}$ to verify that the device is not in cutoff. If the transistor model is in cutoff then the drain current is set to 0. This transistor VI can be made into a subVI and used as a baseline comparison in the I-V Curve program.

Figure 32 shows the full testing program for MOSFETs. This program will capture a family of I-V curves and then plot the mathematical transistor model for the selected parameters. While the program is running the user can vary the threshold voltage, transconductance and channel length modulation (λ) to fine-tune the match with the measured data. While this can be a great tool for learning the interaction of various mechanisms in transistors, the program presented here still requires the user to manually determine the threshold voltage and calculate the transconductance.

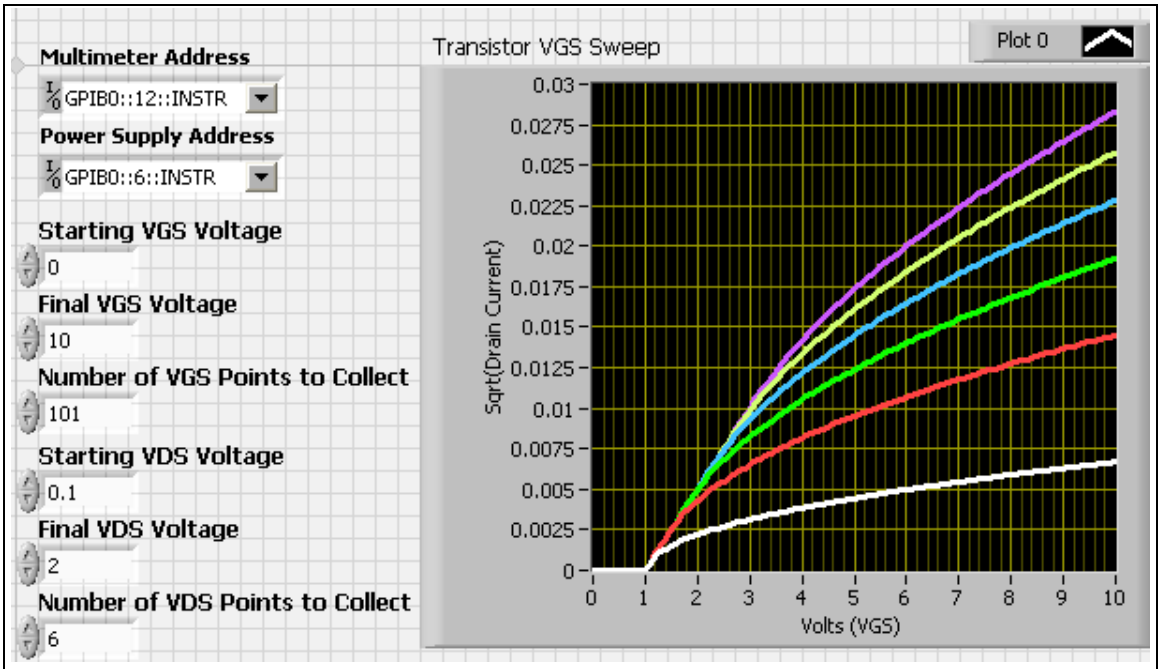

Figure 29 Transistor I-V Curves VGS Sweep

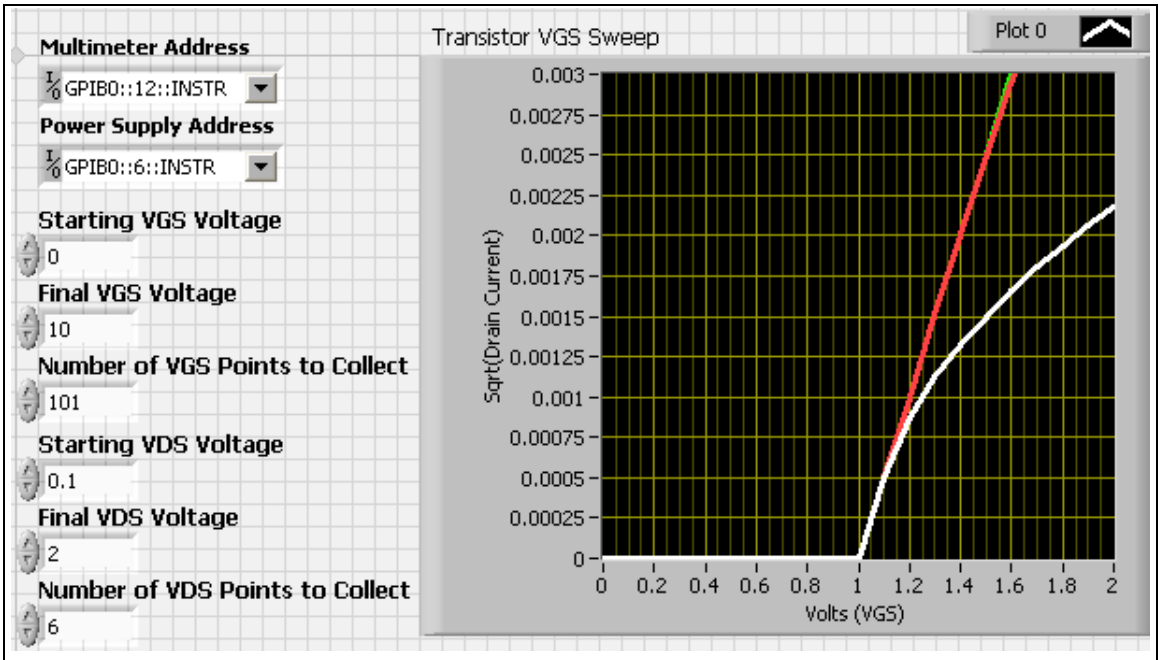

Figure 28 Transistor I-V Curves Zoomed In On Threshold Voltage

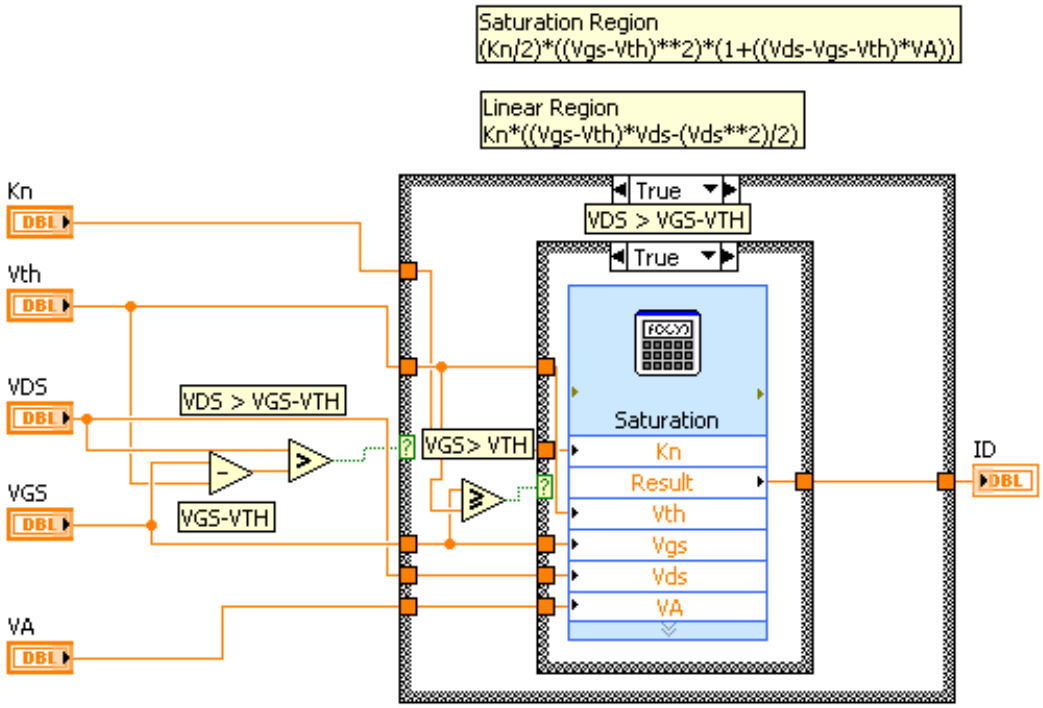

Figure 30 LabVIEW based mathematical transistor model

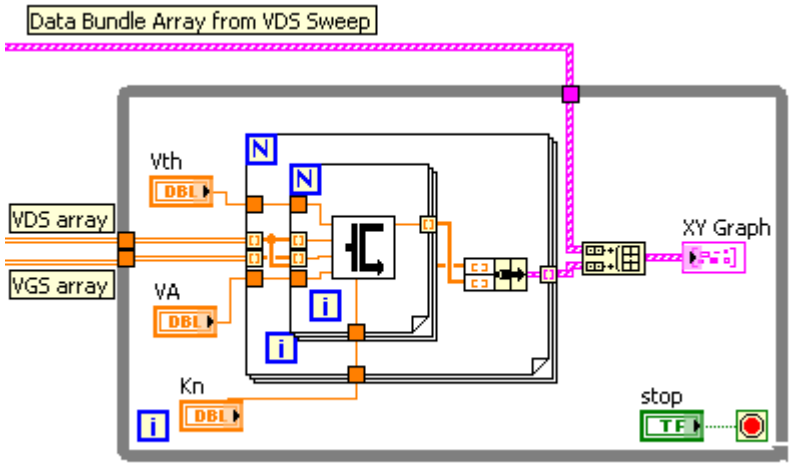

Figure 31 Transistor model in nested loop on the output of VDS Sweep

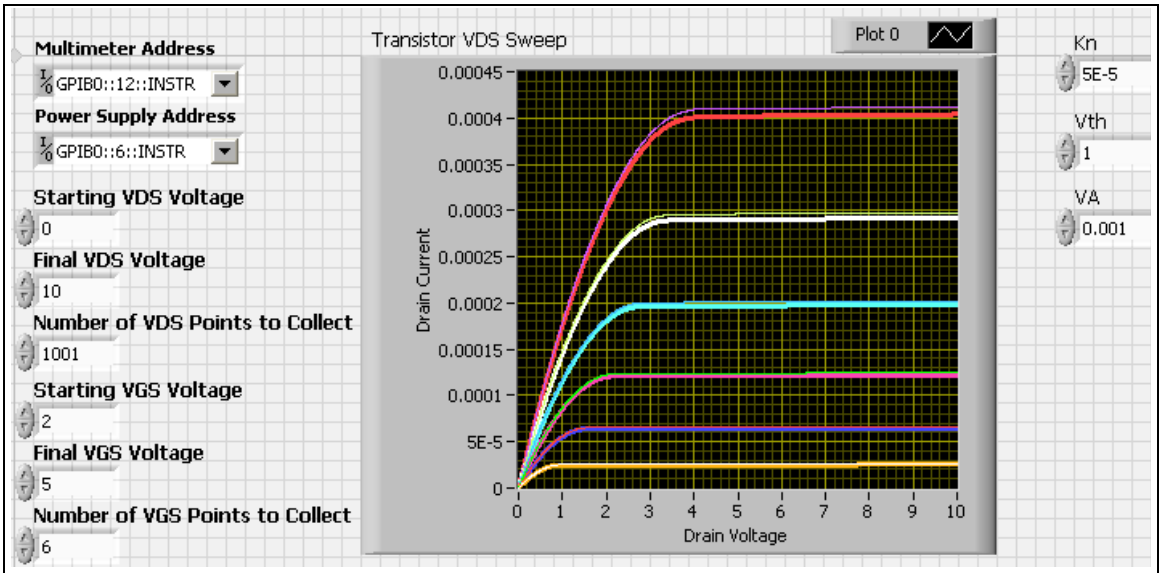

Figure 32 VDS Sweep with transistor model plotted to compare measure parameters

Automatic Data Processing

The goals of these programs are to collect data quickly and accurately, display it in a way that is immediately useful, and extract the desired information from the data. Thus far, these programs have succeeded at satisfying the first two points, but have required human interaction to do anything beyond data collection. To demonstrate the third point, the previous example will be further developed.

Extracting Intuition from Information

Adding a data processing component to the transistor sweep program does not present a significant hurdle. The three parameters, (V_{TN}, K_n, λ) can be found in order. First, the threshold voltage can be found by performing a V_{gs} sweep. V_{TN} will be equal to the gate voltage at which the drain current exceeds I_{off} or the noise floor.

$$V_{TN} = v_{gs}\ where\ i_d > i_{off} \quad \textbf{38}$$

This can be represented programmatically through a simple conditional statement. There are two requirements for this to yield accurate results: the i_{off} or i_{noise} threshold level needs to be correct within a few orders of magnitude and

there must be a sufficient number of data points around the threshold voltage. The returned threshold voltage will be equal to the first gate voltage that corresponds to a current above the noise threshold. This means that the first recorded point above the current threshold will be considered the transistor threshold voltage. There error can be as large as the step size.

Figure 33 shows the LabVIEW implementation of the threshold voltage solving routine. This program is slightly more complex than suggested above. Two functions were added to make this subroutine more robust and improve the accuracy. The first part is for glitch checking, this confirms that a stray measurement above I_{off} doesn't set the threshold voltage erroneously. If the measured current is above I_{off}, the corresponding v_{GS} will be set as V_{TN}. If, however, the current measurement falls below I_{off}, the early value will be considered an error and the threshold voltage will be reset to 0, so that V_{TN} can be set by the next value that is above I_{off}.

The other change is designed to produce a more accurate value for V_{TN}. Originally the value chosen for V_{TN} was the first v_{GS} over the threshold. This will inevitably result in errors because when the transistor first turns on it will still not be conducting much current. The solution for this is to define V_{TN} as the value of v_{GS} prior to crossing the I_{off} threshold.

The second value that can be calculated is the transconductance. Using

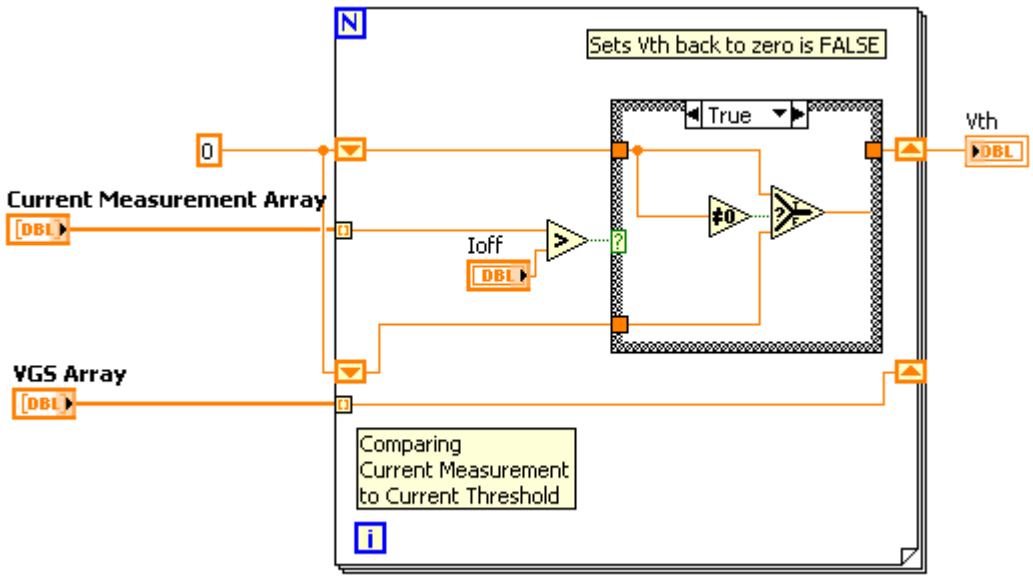

Figure 33 Threshold Voltage Solving Function

the threshold voltage from the first step all of the variables are known for **(**39**)** and **(**40**)**.

For $\boldsymbol{V_{DS} < v_{GS} - V_{TN}}$ $$K_n = \frac{i_D}{(v_{gs} - V_{TN})V_{DS} - \frac{V_{DS}^2}{2}}$$ **39**

For $\boldsymbol{V_{DS} = v_{GS} - V_{TN}}$ $$K_n = \frac{2i_D}{(v_{gs} - V_{TN})^2}$$ **40**

It is worth noting that in order to avoid adding extra unknowns (channel length modulation), **(**40**)** is defined specifically at $V_{DS} = v_{GS} - V_{TN}$. It is highly unlikely, though, that the condition for **(**40**)** will be met, since V_{TN} is an experimentally derived value. Some margin must be included in the condition for evaluating this equation.

Figure 34 shows the actual implementation of the transconductance parameter-solving program. A linear points counter was added to this program to keep track of the point at which the calculations switch from assuming linear region to saturation region. This is clearer on the following plot.

The third parameter to calculate is channel length modulation. This will be

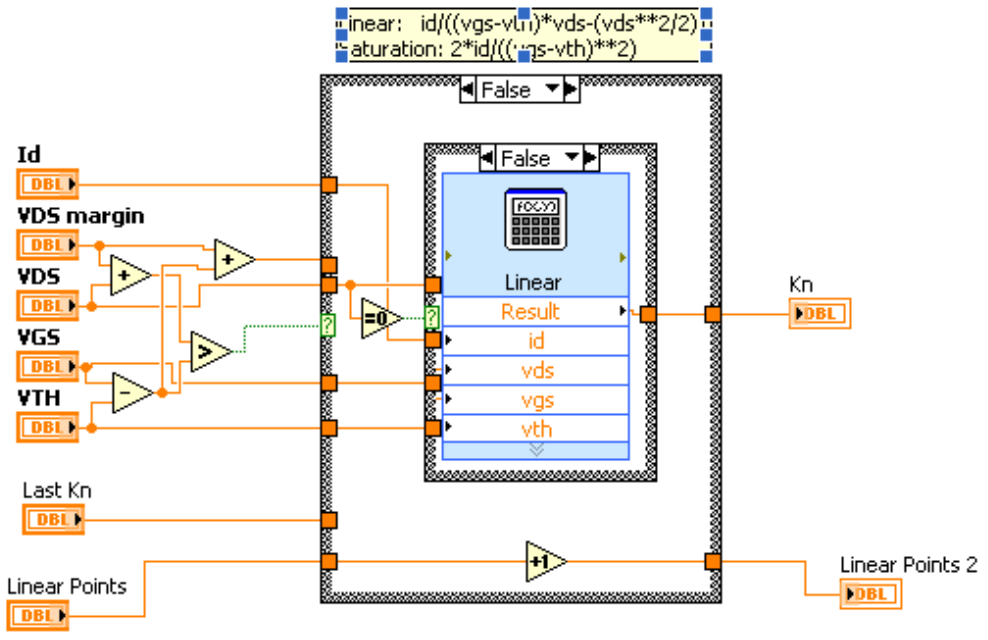

Figure 34 Transconductance Parameter Solving Function

calculated on the data where the transistor is deep in the saturation region.

For $\boldsymbol{V_{DS} > v_{GS} - V_{TN}}$ $$\lambda = \frac{2i_D - K_n\left(v_{DS,sat}\right)^2}{K_n v_{DS,sat}^2 V_{DS}} \quad \textbf{41}$$

The Channel Length Modulation solver (Figure 35) is implemented directly from **(**41**)**. To prevent a divide by zero error, K_n, $v_{DS,sat}$, and V_{DS} are checked before performing the calculation. If any of those parameters are zero, the function returns a zero, which is filtered out after the function.

The original program with the new parameter solving functions is shown in Figure 36. Test data was used for a transistor with $V_{TN} = 1\,V$, $K_n = 50\,\mu S/V$, and $\gamma = 0.001\,V^{-1}$. The outputs of the calculations are on the right side of the graph. They match perfectly to the test data used. There is also an additional white line on the graph delineating the transition from linear to saturation region.

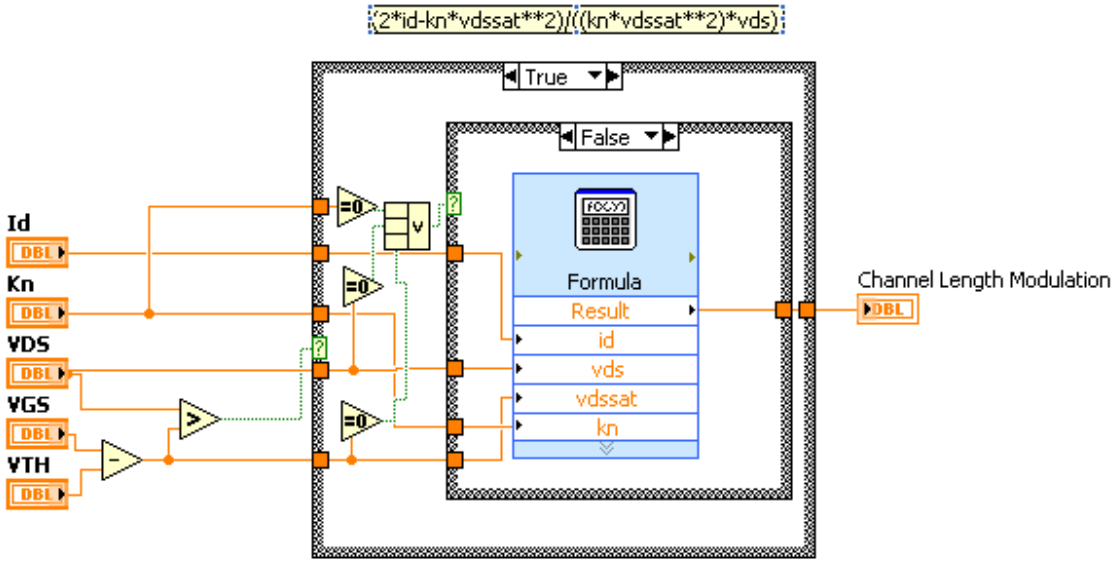

Figure 35 Channel Length Modulation Solver

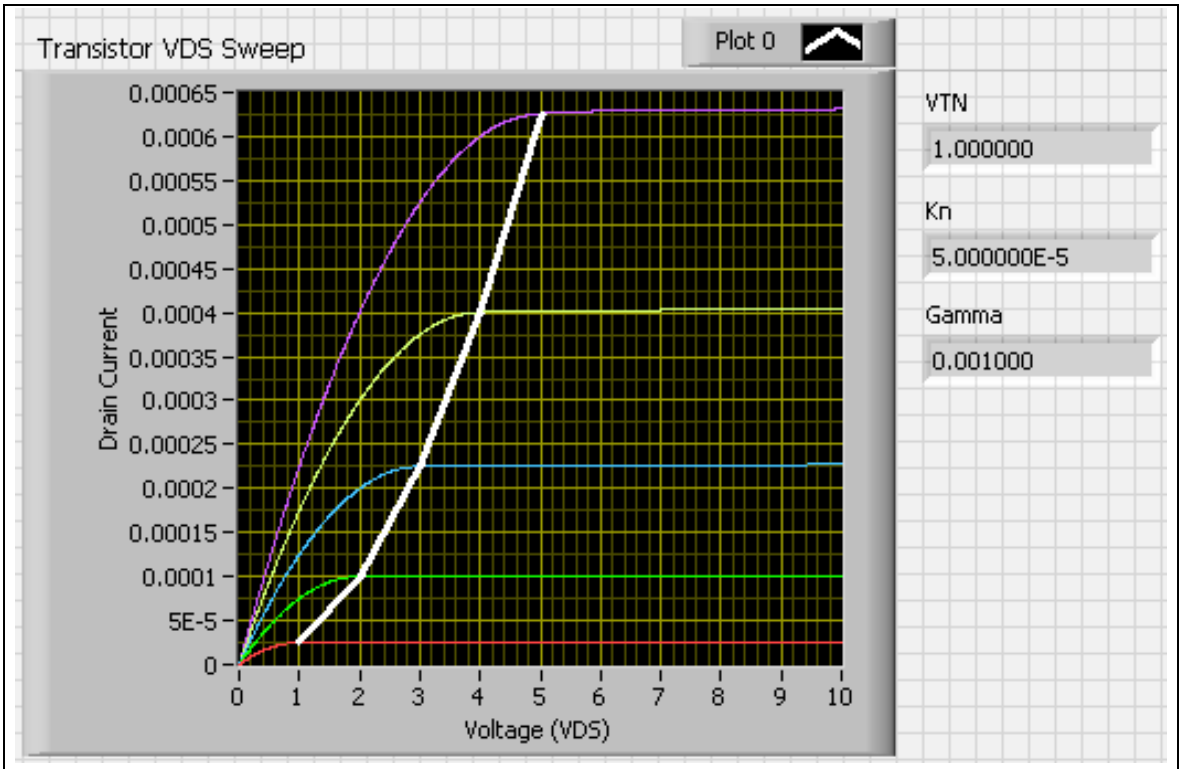

Figure 36 Transistor Sweeper with Parameter Solver

Complex Circuits and Data Organization

Op-amps may not qualify as a complex circuit, per se, but full characterization of an op-amp does require a large number of tests and many different circuit configurations. When testing is more involved than is the case with the transistors, it is important to look for overlap between test circuit configurations as well as the programs used to test different circuit configurations. For instance, the circuits used to test an op-amp's open-loop gain, CMRR and PSRR (Figure 10 and Figure 12) have a similar configuration. One program can test all three of those parameters. The most equipment-intensive of those tests is the CMRR, which requires a complementary power supply, an oscilloscope and three function generators. The PSRR and open-loop gain test represent a more standard test configuration and only require one function generator. The majority of the characterization tests can be run with this instrument lineup.

Two tests that reveal significant information about an op-amp are the closed-loop frequency sweep and the step response. Both of these tests use a waveform generator for the input signal and an oscilloscope to measure the output. Figure 37 shows an example of a simple program for sweeping the frequency of an input signal to an op-amp and measuring the amplitude on the output with an oscilloscope. This program is very similar to the previous examples with a few minor changes. Obviously, the instrument functions have to be replaced to call the appropriate test instrument. One change that is easy to overlook is in the frequency control section on the bottom of the program. The start, stop, and # of points controls are all the same, but the values are scaled by a $\log(x)$ function to calculate the range and step size. Then when calculating the frequency step, after the iteration step, a 10^x function is used. This scaling provides value sweeps that are more congruent with logarithmic frequency scale of Bode plots. The gain calculation is performed on the output with an expression block similar to the $\log(x)$ function at the beginning of the program.

Using this program to test an op-amp would yield results similar to those shown in Figure 38. From this data the unity-gain crossover frequency (f_c), peaking frequency (M_{pf}), -3dB frequency (f_{-3dB}), and approximate Gain-Bandwidth Product can be found. Much like the equations for transistors, the

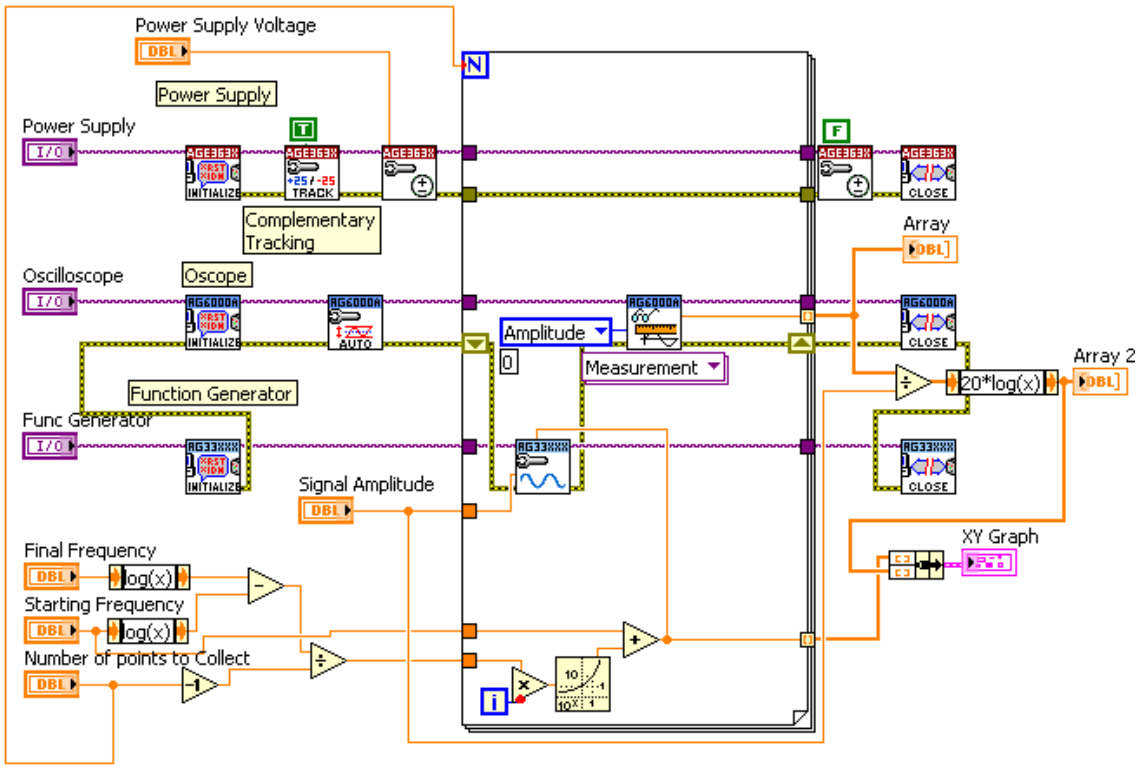

Figure 37 Op-Amp Frequency Sweep Program

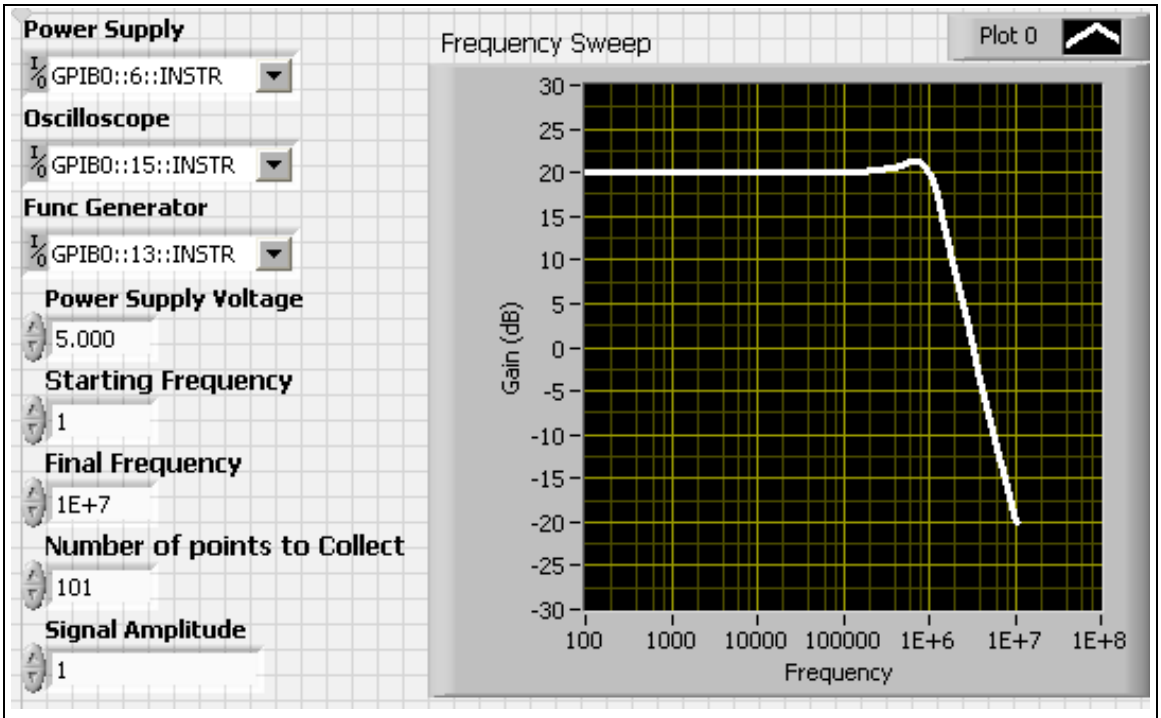

Figure 38 Results of a frequency sweep on an op-amp with 10V/V gain

equations for op-amps can be used to extract these various parameters automatically while the data is being collected. Likewise, this program can easily be configured to record transient response data.

To convert from a frequency sweep to a step response measurement, the function generator must be set to a square wave instead of sinusoid and the data collection functions on the oscilloscope must be programmed collect the rise time, overshoot and settling time. The actual waveform can be recorded as well (Figure 39).

Like the transistor model that was made to provide a first-order comparison of calculated parameters to the measured data, it is possible to make a single pole transfer function and a time domain step response that share parameters. It is possible to extract the natural frequency (f_n) and damping ratio (ζ) from the step response measurements. Those parameters are used in the models and can be compared to the measured data. The step response from **(**31**)** is translated into a LabVIEW model in Figure 40.

the op-amp characterization If it is possible to recreate all of the test circuits in the suggested forms then characterization can be a straight forward process. LabVIEW can expedite the process of collecting, processing, and organizing the data.

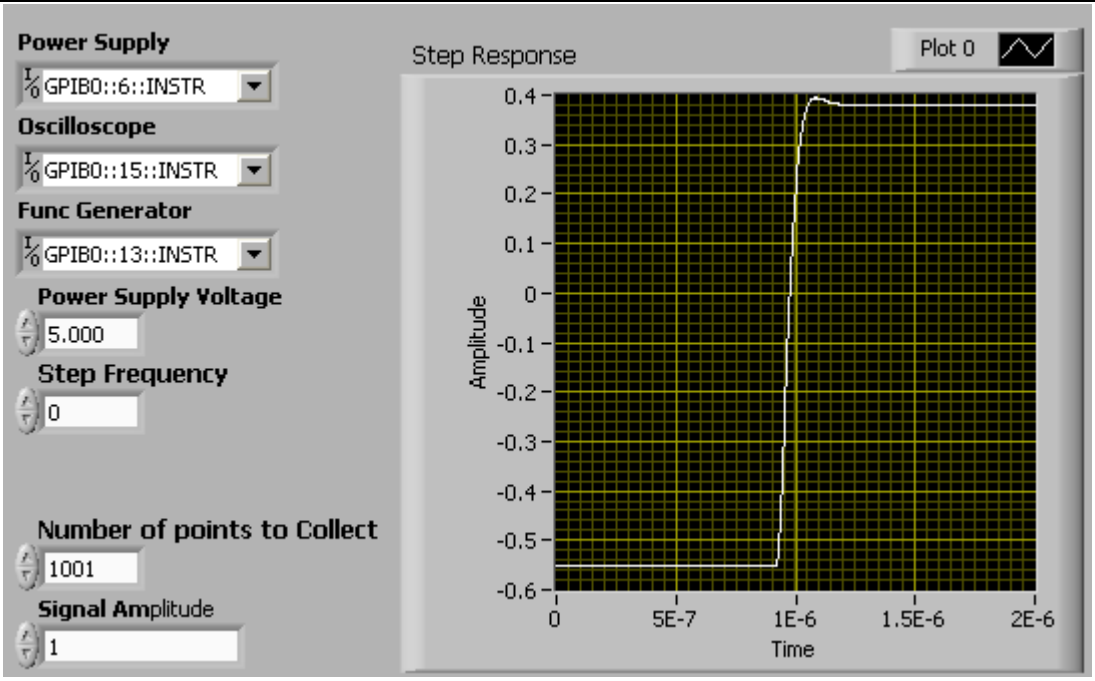

Figure 39 Results of a Step Response measurement

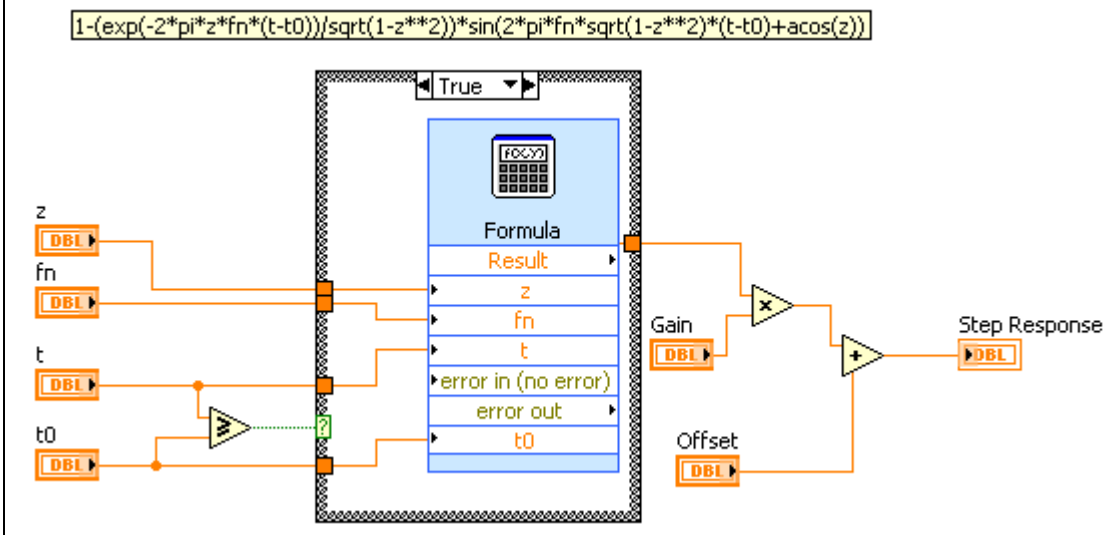

Figure 40 Step Response Function

There are instances when the testing will be limited out of necessity. It is possible that due to parasitics introduced by the bond wires an op-amp will not be stable if the feedback network is connected off chip. In that situation a feedback network must be connected on the IC. For a real life example, an op-amp was required to use on-chip feedback network with a gain of 10V/V (Figure 42). This configuration limited the number of tests that could be performed. There was still some flexibility in the circuit because none of the terminals were hard wired. The amplifier could operate as an inverting amplifier with a gain of 9V/V, a non-inverting amplifier with a gain of 10V/V, or, by connecting the negative terminal resistor back to the output, the amp could act as a voltage follower.

The large number of tests required to characterize an op-amp have already been enumerated

Automated Testing for Oddly Made Tests

All of the examples up to this point have assumed ideal controlled laboratory conditions with devices that can be accessed individually and reconfigured as needed for each test. When testing for extreme environments the DUT is not usually accessible during the test. This can limit the number of circuit configurations and variety of tests performed. In order to get the most data from each test, compromises must be made and alternate topologies used. The first example is a seemingly trivial measurement, transistor I-V curves. This trivial exercise becomes a challenge when instead of testing a single transistor, there are 16 transistors that must be tested and it must be done in less than a minute. The most direct solution, of course, would be to scale up the test equipment by 16x and run all of the tests in parallel. This solution would only work in the most well endowed labs; 32 sources and 16 multimeters is generally more equipment than any lab would own. The final solution was to use a slightly altered topology.

Testing with Limited Resources

The chosen solution to the transistor array was to use a common-gate voltage source and a common-drain voltage source. To bypass the lack of ammeters, current sense resistors were placed on the drain of the transistors. Figure 41 shows the arrangement of the transistors, resistors, control sources, and the voltage sense nodes. This configuration reduces the voltage sources to 2 and the solution for measuring drain current was to use a 16-channel data acquisition card (DAQ). The DAQ actually contained voltage sources as well as differential voltage ADCs, so the entire circuit only required the connection of a single ribbon cable. The addition of the resistors does add a voltage drop that will cause a deviation in the transistors' V_{DS} voltage. To account for this offset the characterization program had to calculate the actual transistor V_{DS} for each

device based off of the programmed V_{DS} and the measured sense resistor voltage drop.

$$V_{DS}^{i^{th}} = V_{DS} - V_{sense+}^{i^{th}} - V_{sense-}^{i^{th}} \quad \textbf{42}$$

$$i_D^{i^{th}} = \frac{\left(V_{sense+}^{i^{th}} - V_{sense-}^{i^{th}}\right)}{R^{i^{th}}} \quad \textbf{43}$$

In addition to the calculations required to get the true V_{DS} and i_D, feedback was required so that the program could sweep the full user defined range. For example, if the V_{sense} drop was 2 V and the programmed V_{DS} was 5 V, the voltage appearing across the transistor would be just 3 V. The fastest and most straightforward solution to this problem is to have the V_{DS} sweep loop continue iterating the voltage higher until the measured voltage across the transistor matches the set stopping point. This will of course add more points than originally specified, but it ensures a complete sweep of the DUTs.

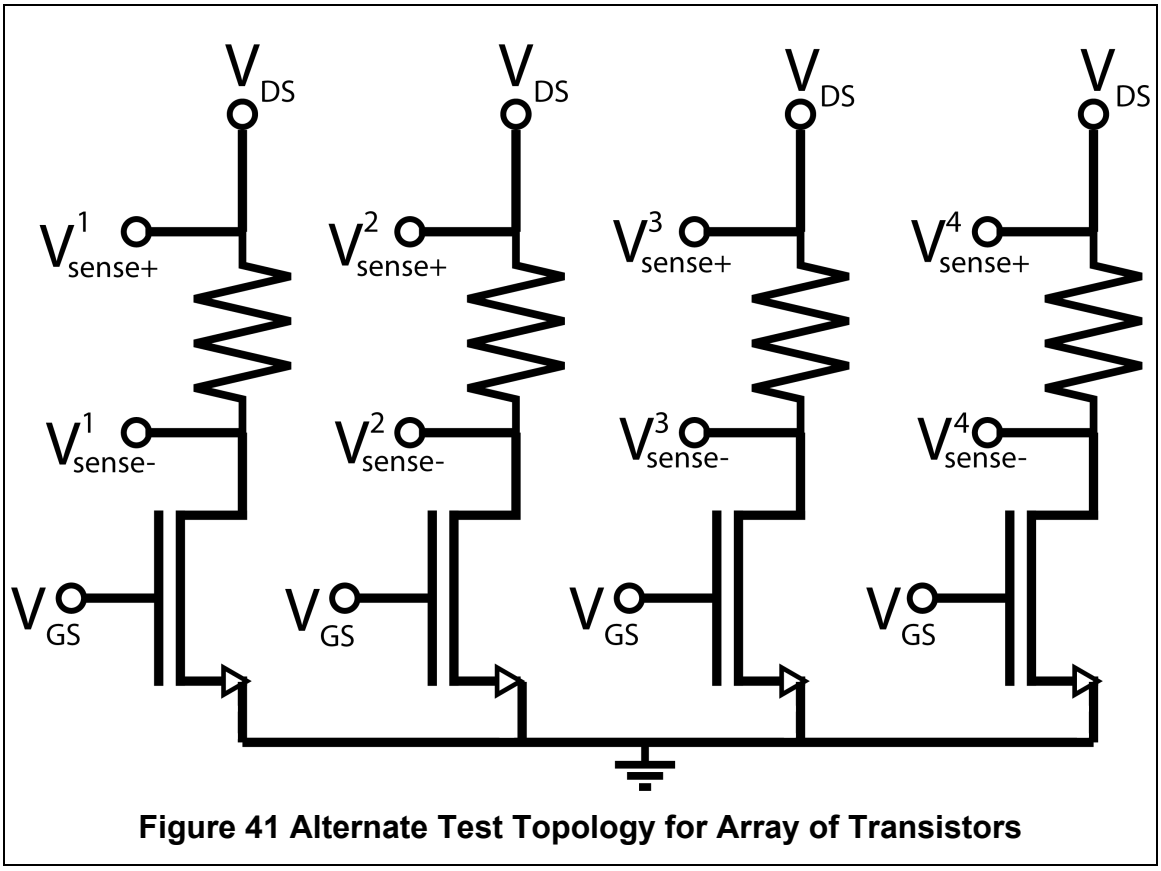

Figure 41 Alternate Test Topology for Array of Transistors

Characterization from a Pre-Defined Configuration

There are cases when it is not possible to have complete access to all of the terminals of a device, such as the case of an op-amp that is not stable without on-chip feedback. Figure 42 is an example of such a pre-defined circuit configuration. This was used for an experiment where time was a major constraint. A compromise had to be made between the time required to run a test and the importance of the parameters that are characterized by the test. Ultimately, the tests chosen were the frequency sweep (Bode plot) and the step response.

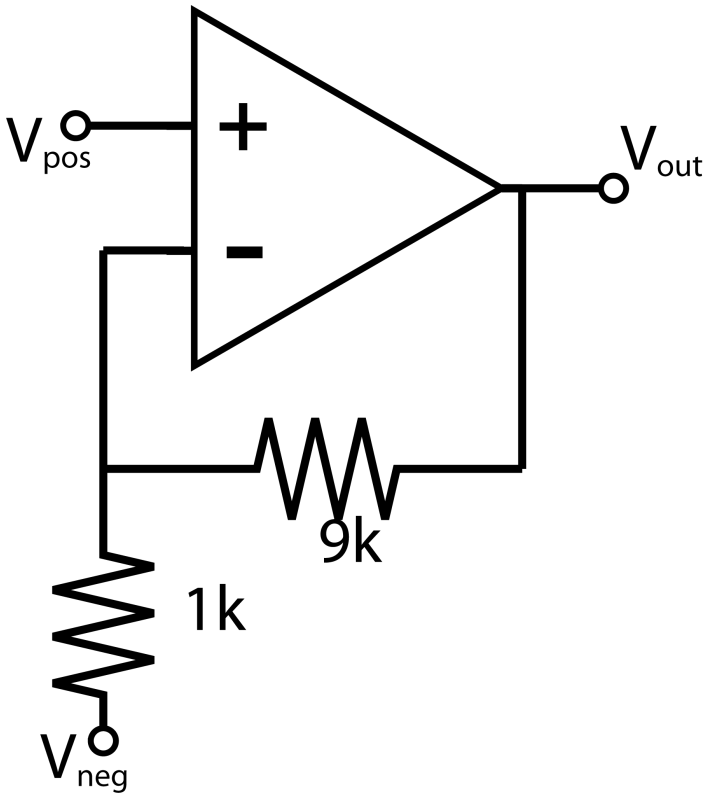

Figure 42 Limited Op-Amp Configuration

CHAPTER IV
RESULTS AND DISCUSSION

The data presented here was gathered using LabVIEW during extreme environment tests. The data was post-processed using the algorithms presented above. The actual LabVIEW display is shown with measured data (thin lines) and ideal model (thick lines) overlaid. The calculated parameters are shown to the right side of the plots. The parameters are calculated from the measured data and then those parameters are used to generate the ideal model plots.

To provide a figure of merit for the measured and modeled data matching, the percent difference **(**44**)** and RMS percent difference **(**45**)** is calculated as follows

$$\%\text{Diff} = \text{Avg}\left(\frac{Model\ Data - Measured\ Data}{\frac{Model\ Data + Measured\ Data}{2}}\right) \quad \textbf{44}$$

$$\%\text{Diff} = \sqrt{\text{Avg}\left(\left(\frac{Model\ Data - Measured\ Data}{\frac{Model\ Data + Measured\ Data}{2}}\right)^2\right)} \quad \textbf{45}$$

Tables with the measured parameters and matching difference percentage are presented after each section.

Measured and Parameterized Model Data

Transistor Array

The arrays of transistors presented in Figure 41 were subjected to a number of extreme environment tests. Data collected from those tests was processed as previously discussed. The parameters obtained from the data and the corresponding I-V curves are shown in Figure 43 through Figure 46.

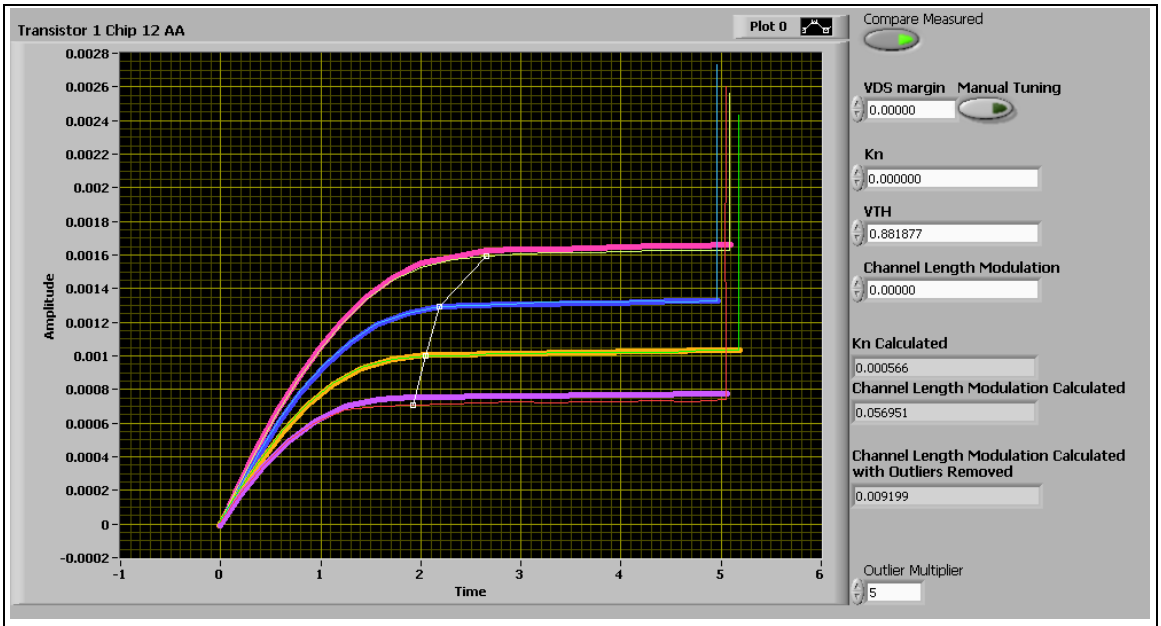

Figure 43 Transistor Evaluated and Curve Matched, K_n=566mS/V, γ= 0.009199 V^{-1}, V_{TN}= 0.882 V

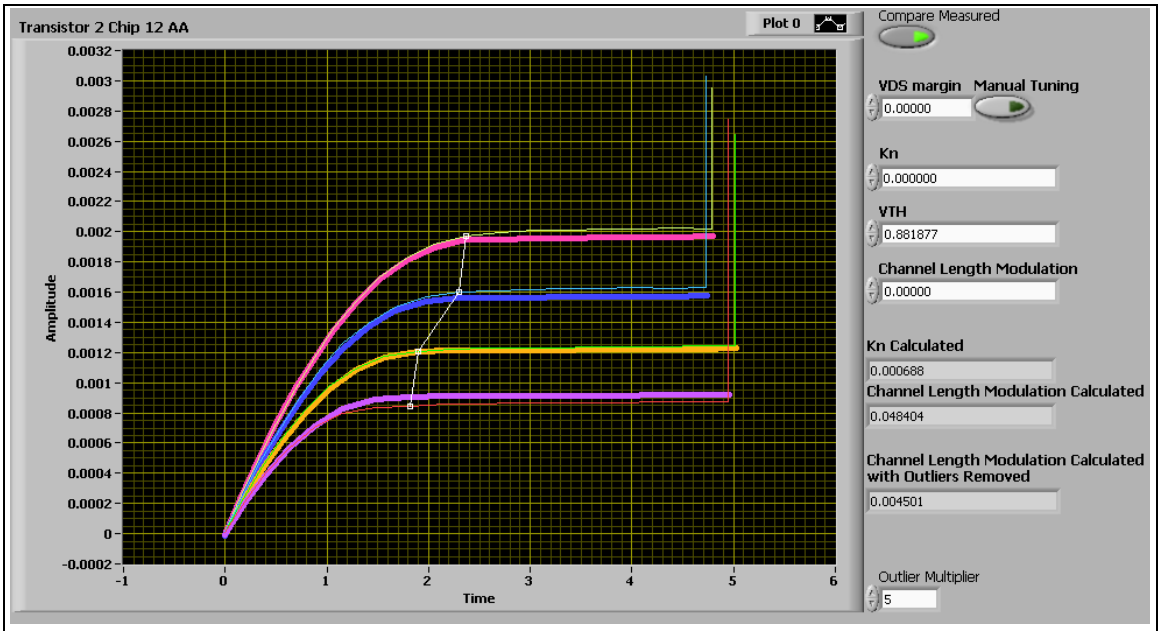

Figure 44 Transistor Evaluated and Curve Matched, K_n=688mS/V, γ= 0.004501a V^{-1}, V_{TN}= 0.882 V

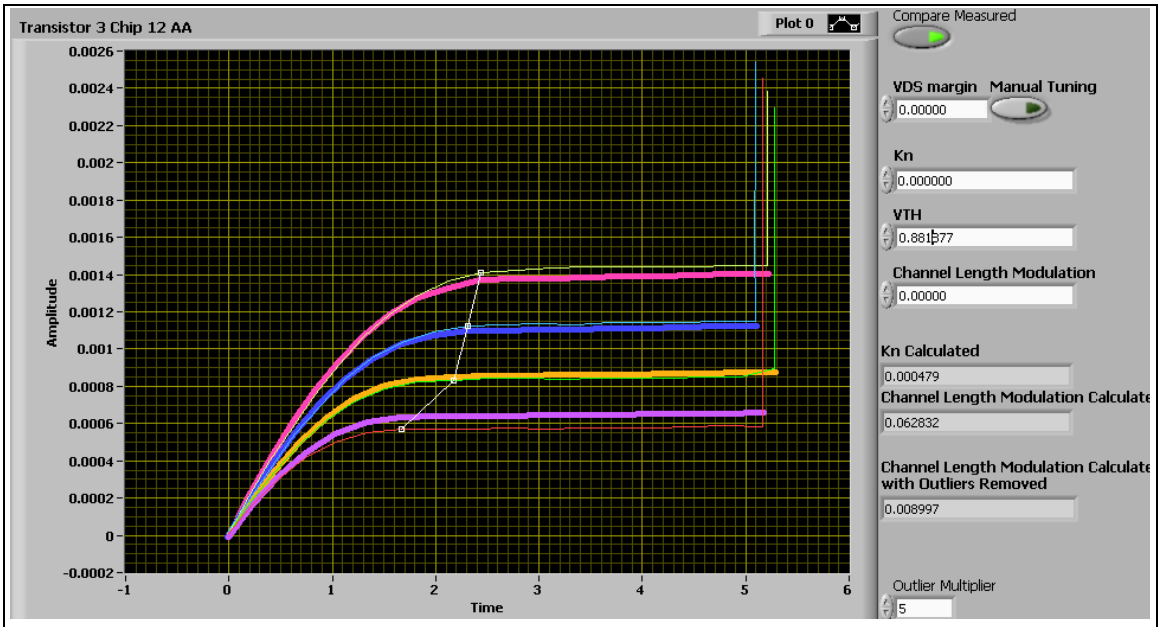

Figure 45 Transistor Evaluated and Curve Matched, K_n=479mS/V, γ= 0.000997 V^{-1}, V_{TN}= 0.882 V

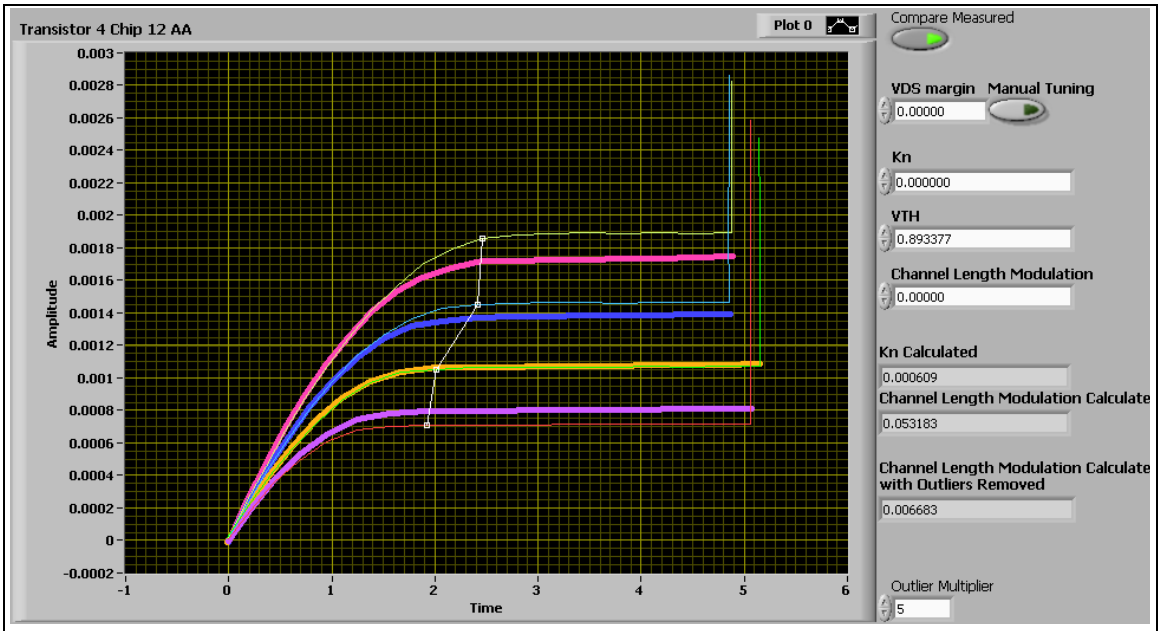

Figure 46 Transistor Evaluated and Curve Matched, K_n=609mS/V, γ= 0.006683V^{-1}, V_{TN}= 0.893 V

Table 2 Results from Transistor Parameter Matching

	FET 1	FET 2	FET 3	FET 4
Threshold Voltage (V)	0.7865	0.9037	0.8185	0.8386
Transconductance Parameter (μS/V)	525	700	455	582
Channel Length Modulation (1/V)	0.006878	0.007963	0.008038	0.005722
Root Mean Squared Error	========	========	========	========
Average Difference	1.616%	2.432%	0.6932%	1.6090%
RMS Difference	9.416%	8.455%	11.493%	10.954%

This data was collected from transistors with a variety of sizes. All of the transistors that were tested are below what is considered the threshold for long-channel devices [1][3]. The ideal model that is used for matching purposes defines the operation of long-channel devices. Given this fact, the measured data from the transistors matches the parameterized ideal models surprisingly well.

Op-Amp Characterization

The op-amps were characterized using the frequency sweeps and step response transient analysis. The natural frequency and damping ratio were extracted from these measurements and entered into the ideal models. The measured data and modeled data were compared to provide an RMS difference percentage.

The data collected from the tests is in Table 3. Much like the transistor tests, the ideal models are based on first-order systems that neglect all of the higher order effects. In op-amps with multiple poles and zeros this difference can be quite pronounced [2][5]. Based on simulations, it can safely be concluded that the wider bandwidth, audio band, op-amps have multiple pole interactions. This is reflected in the matching error. Op-amps 1 and 2 are the lower bandwidth op-amps. On both of these low bandwidth op-amps the RMS percent difference is approximately 6%. On the higher bandwidth op-amps, 3 and 4, the RMS percent difference is 15.8% and 11.8%, respectively. The degree of matching obtained through these tests is sufficient to provide a baseline for comparing topologies and monitoring parameter variation across environmental changes.

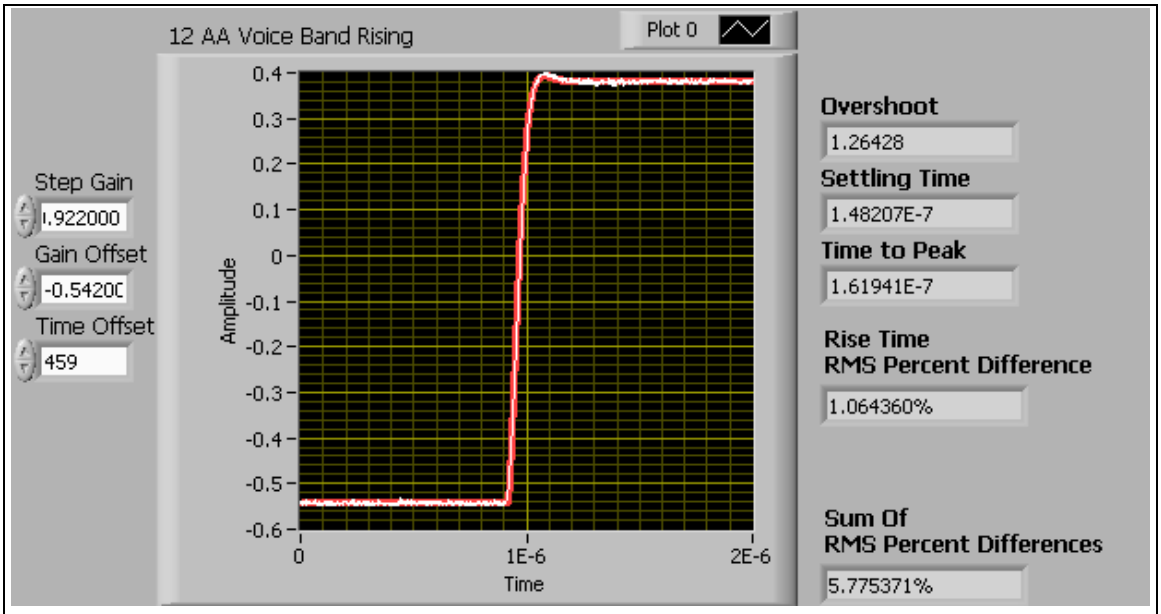

Figure 48 Step Response of Op-Amp 1, Overshoot 1.26, Settling Time 148ns, Time to Peak 162ns,

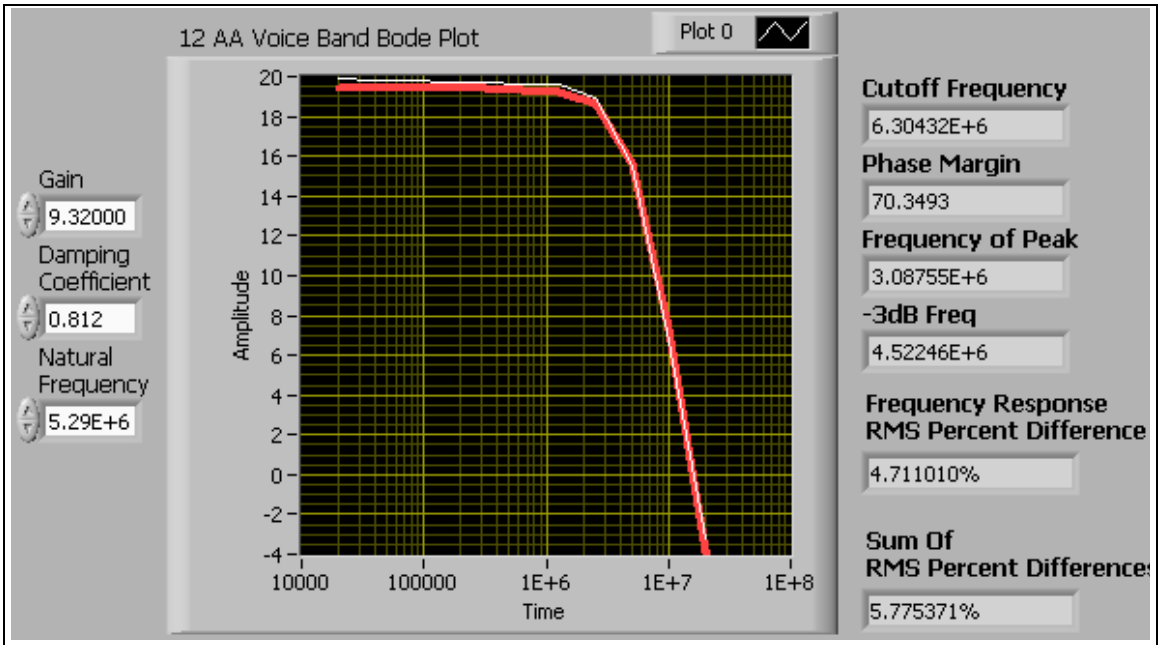

Figure 47 Frequency Response of Op-Amp 1, Cutoff Frequency 6.3 MHz, Phase Margin 70, -3dB Frequency 4.5 MHz

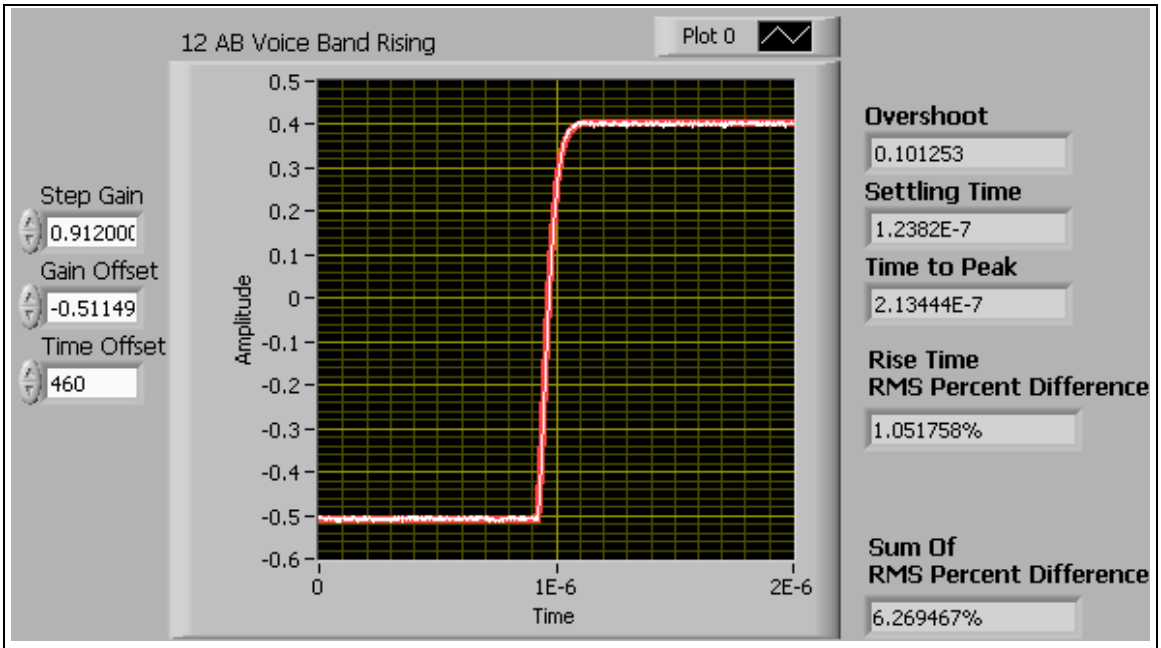

Figure 49 Step Response of Op-Amp 2; Overshoot 0.1, Settling Time 124 ns, Time to Peak, 213 ns

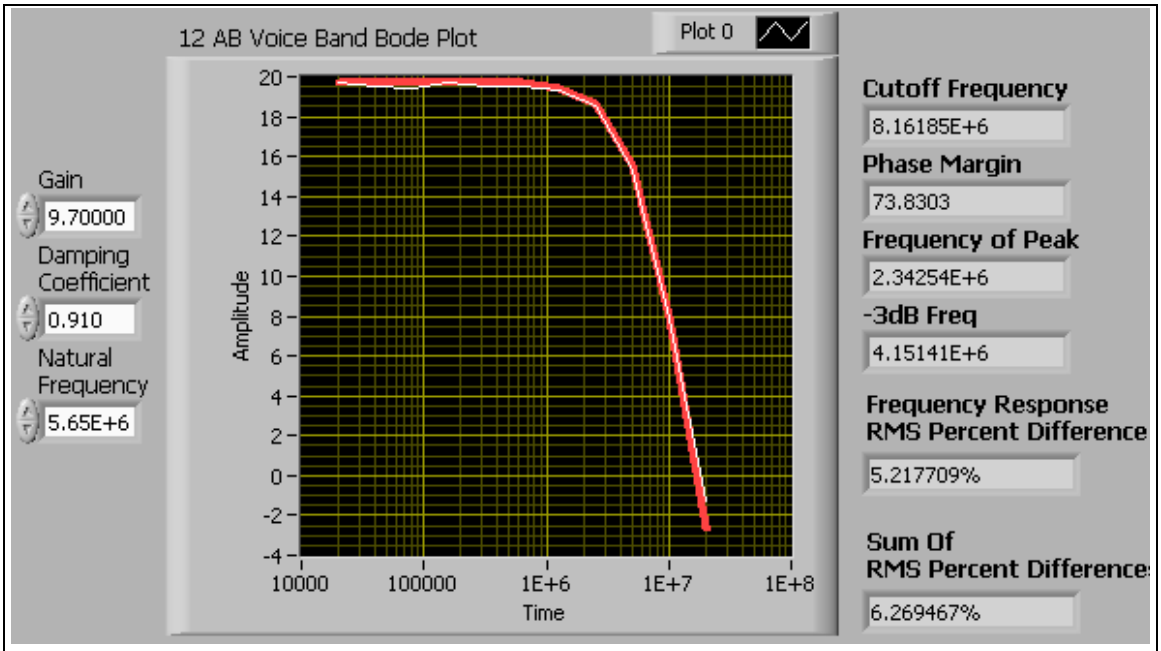

Figure 50 Frequency Response of Op-Amp 2; Cutoff Frequency 8.2 MHz, Phase Margin 73.8, -3dB Frequency 4.2 MHz

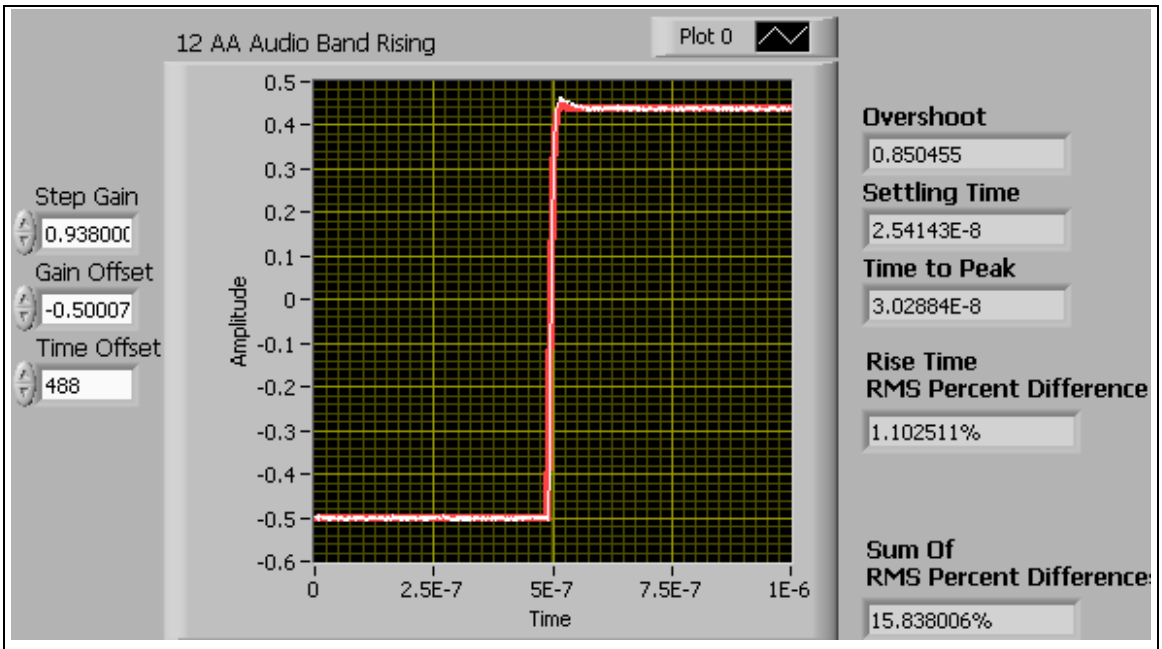

Figure 51 Step Response of Op-Amp 3; Overshoot 0.85%, Setting Time 25 ns, Time to Peak 30 ns

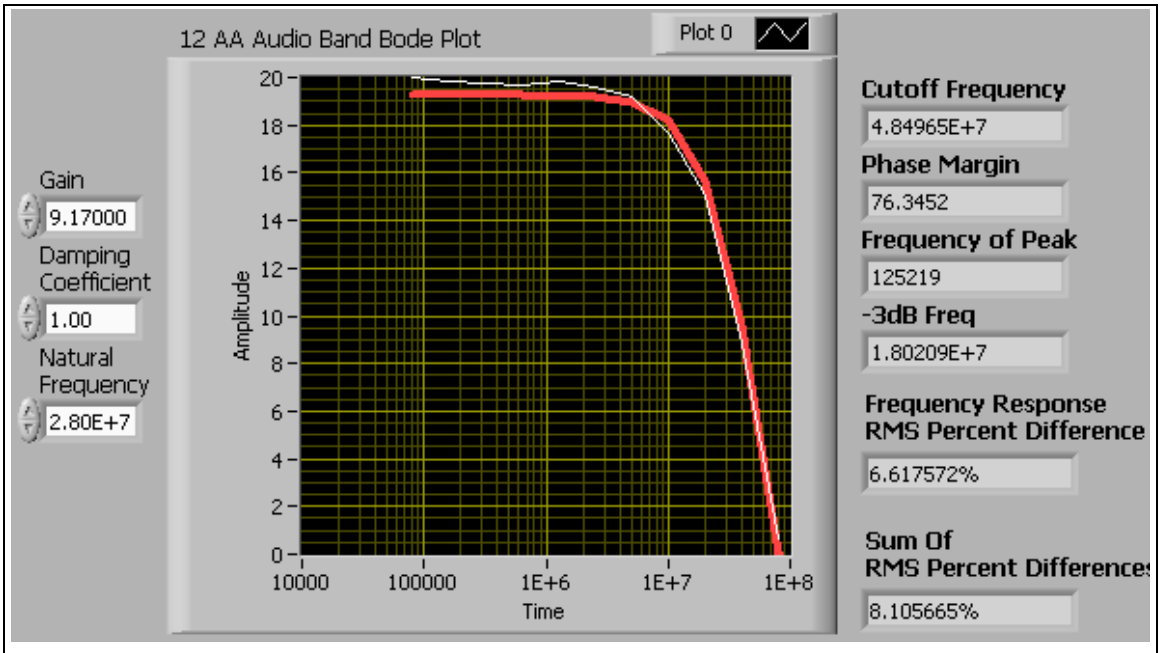

Figure 52 Frequency Response of Op-Amp 3; Cutoff Frequency 48.5 MHz, Phase Margin 76, -3dB Frequency 18 MHz

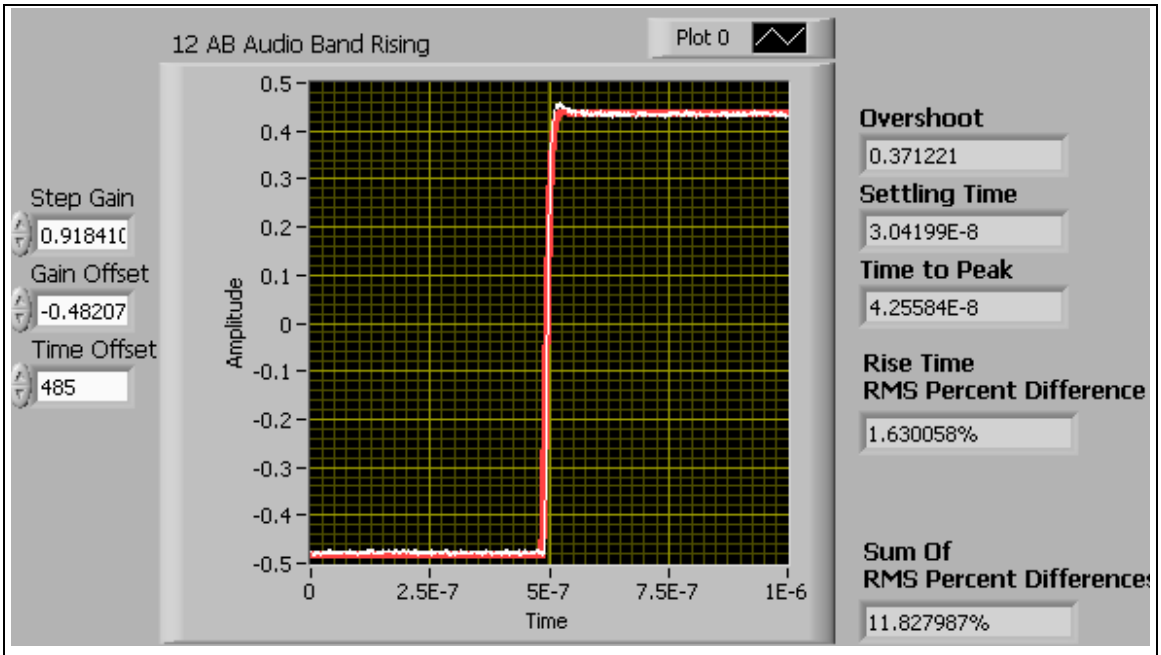

Figure 53 Step Response of Op-Amp 4; Overshoot 0.37%, Settling Time 30.4 ns, Time to Peak 42.6 ns

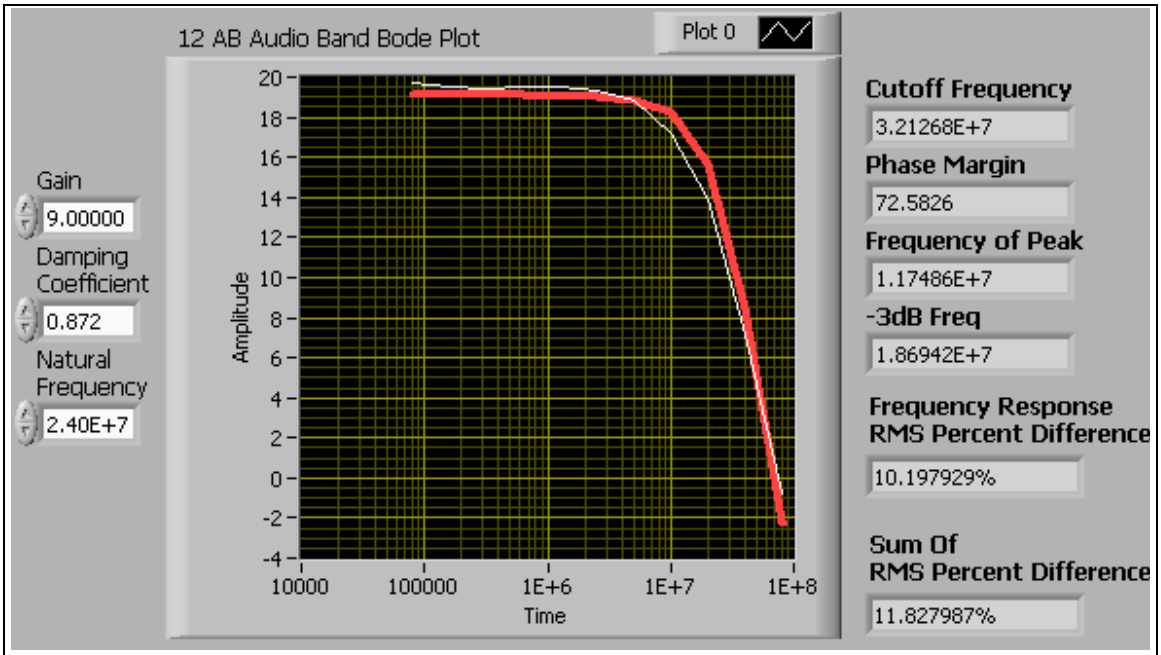

Figure 54 Frequency Response of Op-Amp 4; Cutoff Frequency 32.1 MHz, Phase Margin 72.6, -3dB Frequency 18.7 MHz

Table 3 Results from Op-Amp Parameter Matching

	Op Amp 1	**Op Amp 2**	**Op Amp 3**	**Op Amp 4**
Cutoff Frequency (MHz)	6.304	8.162	37.35	32.13
Phase Margin (degrees)	70.35	73.80	71.25	72.58
Peak Frequency (MHz)	3.088	2.343	16.50	11.74
-3dB Frequency (MHz)	4.522	4.151	24.75	18.69
Root Mean Squared Error	======	======	======	======
Step Response	1.064%	1.052%	1.103%	1.630%
Frequency Response	4.711%	5.218%	14.735%	10.128%
TOTAL	5.775%	6.2695%	15.838%	11.828%

CHAPTER V
CONCLUSIONS AND RECOMMENDATIONS

It has been shown that LabVIEW has a wide range of applications. In this project alone it served as a data collection system and an automated characterization system. The automated data collection was able to perform sweeps and record data hundreds if not thousands of times faster than could be achieved manually. This automation was the enabling factor in an extremely time constrained experiment.

In addition the program analyzed the data that was recorded and turned that into first order models or parameters for the transistors and op-amps that were tested.

The RMS percent differences were kept below 12%. This is respectable given that neither the transistors nor the op-amps were first-order systems. The transistors were not long channel devices. It is well known that sub-micron transistors do not adhere to the long-channel transistor equations (1) and (**2**). Unfortunately, due to the interaction of various phenomenon in short-channel transistors, they cannot be model as elegantly as the long-channel devices. The long-channel equations can provide a good approximation to the operation of these devices. For this experiment the measured and model data supports that conclusion.

Similarly, the op-amp models used were for a single pole system. Even with these imperfect models, the extracted parameters provide approximate results that can be used as a baseline when monitoring the health of these amplifiers during a testing or variation between amplifiers in a batch.

Further development of this system could include, addition of curve fitting to the transistor modeling. This would lose the physics based approach to modeling these devices, but it could obtain an even lower match error, which could be worthwhile when monitoring devices for environmental tests. The op-amp models for multiple poles and zeros could be added to more precisely model the step response and frequency response for these types of op-amps. The automated characterization and modeling system could also be expanded to other types of circuit blocks, such as data converters. The appendices contain more documentation on the program as well as suggestions for developing future programs.

LIST OF REFERENCES

[1] R. C. Jaeger, T. N. Blalock, “Microelectronic Circuit Design”, 3rd Ed. McGraw Hill 2006, ISBN 978-0-07-319163-8
[2] J. F Pierce, T. J. Paulus, “Applied Electronics” CBLS Publisher & Book Distributor 1992, ISBN 1-878907-42-5
[3] R. J. Baker, “CMOS Circuit Design, Layout, and Simulation”, Wiley-Interscience IEEE Press 2005 ISBN 0-471-70055-X
[4] M. J. Roberts, “Fundamentals of Signals and Systems”, 1st Ed. McGraw Hill 2008 ISBN 978-0-07-340454-3
[5] E.J. Kennedy, “Operational Amplifier Circuits: Theory and Applications”, 1st Ed. Holt, Rinehart and Winston, Inc. 1987 ISBN 0-03-001948-6
[6] P.E. Allen, D.R. Holberg, “CMOS Analog Circuit Design”, 3rd Ed. Oxford University Press 2012, ISBN 978-0-19-976507-2
[7] Harris Semiconductor, “Recommended Test Procedures for Operational Amplifiers”, Application Note November 1996 AN551.1

APPENDIX

LabVIEW Basics

In Figure 55 the error wire (yellow) is being used to control execution order. For comparison, Figure 56 is an example of the same program, but it will suffer from a race condition. All blocks in LabVIEW execute as soon as they have received the data on all of their inputs. The example in Figure 55 will program the voltage source first and then read the multimeter measurement. The example in Figure 56 can potentially read the multimeter data *before* the source is set to the new value. This would, of course, result in invalid data.

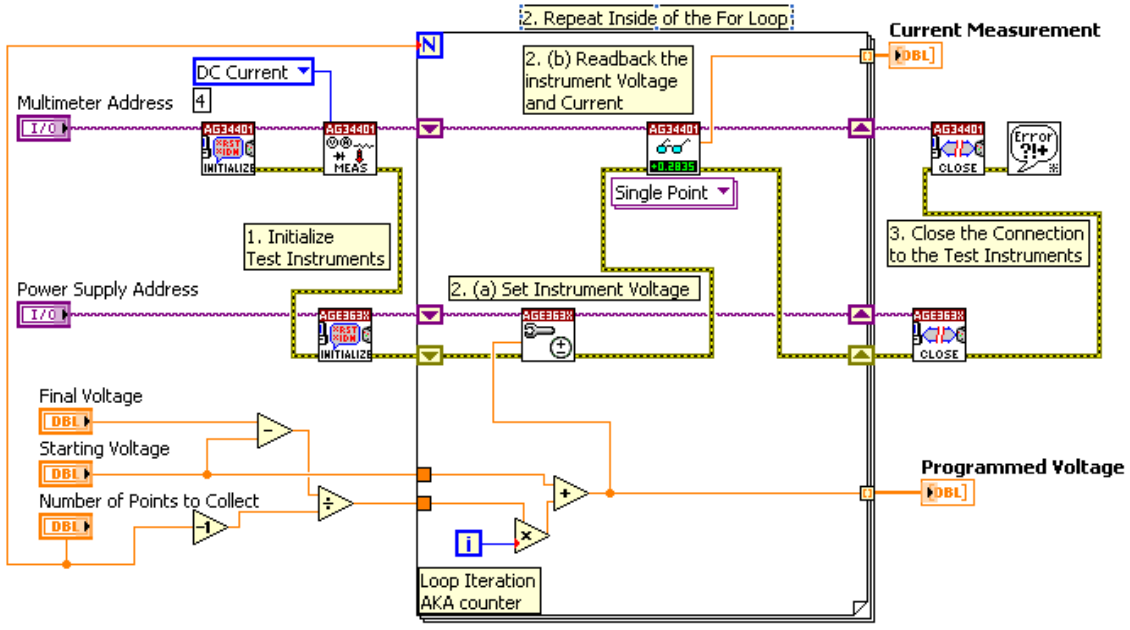

Figure 55 Resistor Sweep Program with dependent data paths

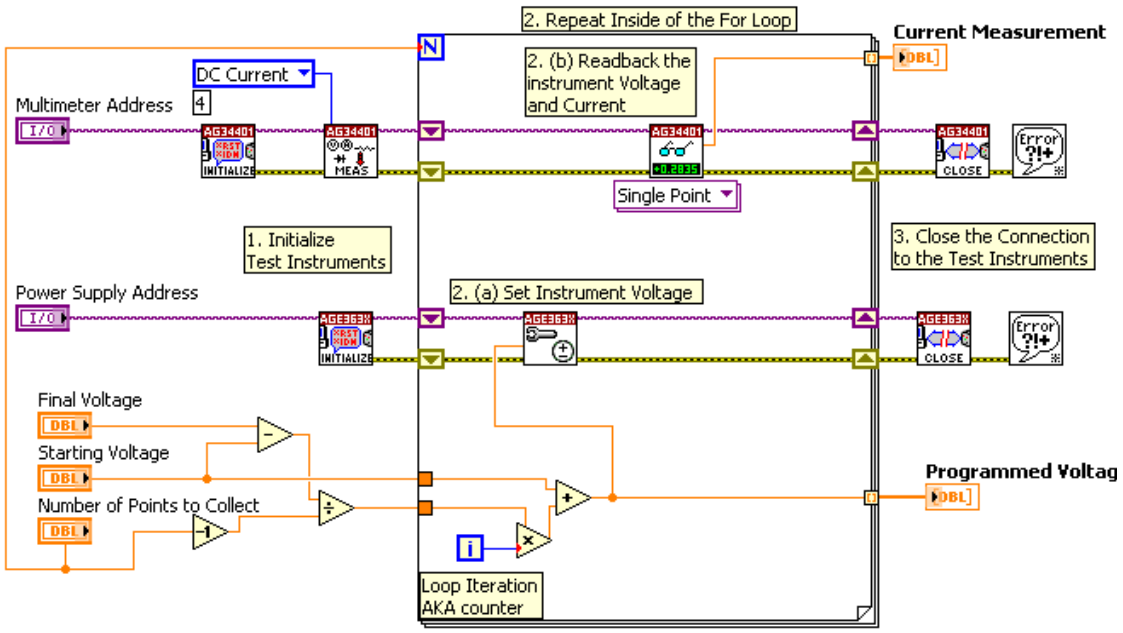

Figure 56 Resistor Sweep Program with race condition

Common Blocks

Figure 57 demonstrates a common functional block for sweep based tests.

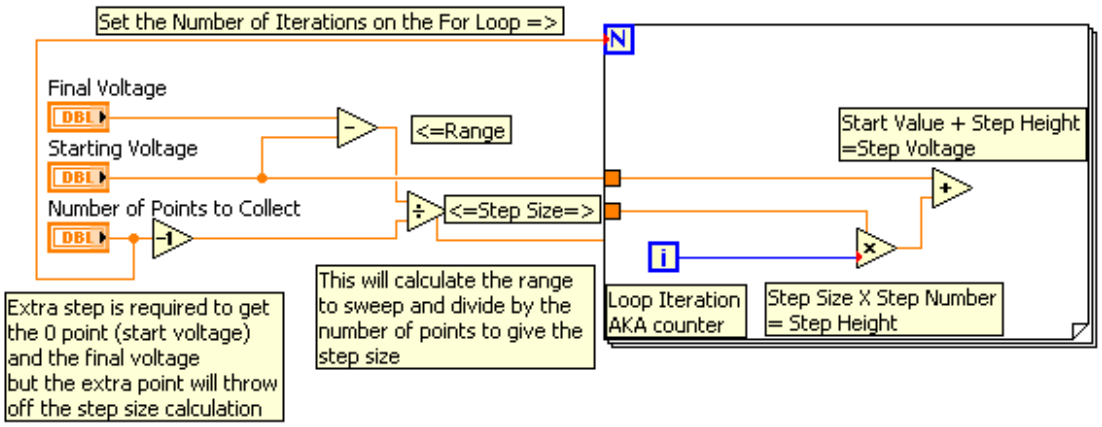

Figure 57 Creating a Sweep Range, Step Size and Increment Step based on the Number of Points in a Sweep

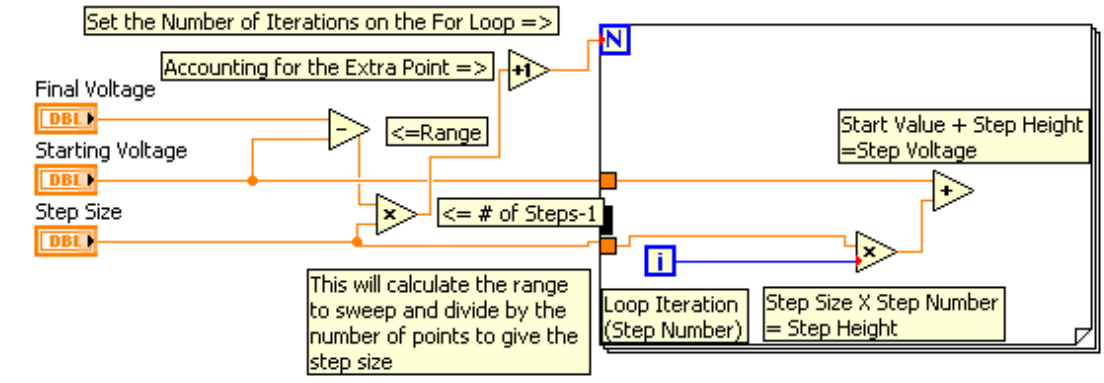

Figure 58 Creating a Sweep Range, Step Size and Increment Step based on the Step Size

A more extensive tutorial and list of commonly used blocks is available on the ICASL website. The website is:

https://icasl.eecs.utk.edu

There are also many resources available online. The National Instruments sponsored forums are very active and usually can resolve any questions that a programmer may have. Their website is:

http://forums.ni.com

The instrument drivers for lab equipment can be found through the LabVIEW programming environment, but more in depth descriptions for drivers can be found at:

http://www.ni.com/downloads/instrument-drivers/

VITA

Jeremy D. Brantley was born in Russleville, AR. He grew up in Knoxville, TN. He completed his Bachelors Degree at the University of Tennessee in 2009. While still an undergraduate he began working with Dr. Benjamin Blalock. After graduating, Jeremy continued performing research with Dr. Blalock while working towards a Master's Degree. Over the course of 5 years working with Dr. Blalock, Jeremy made contributions on projects with NASA/JPL, Large Synaptic Survey Telescope, and Triad Semiconductor.