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Design of an Integrated Silicon Carbide Nonlinear-carrier PWM Controller for Boost Converter Applications

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Design of an Integrated Silicon Carbide Nonlinear-carrier PWM Controller for Boost Converter Applications

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Abstract

Power electronics consisting of a switch mode power supply with feedback control have a great number of applications, including many that require extreme environment capability, such as the aerospace and automotive industries.

Silicon carbide (SiC) is a common material in which power devices are created for use in switch mode power supplies, such as boost converters, giving those power supplies extremely high temperature capabilities. To truly realize the temperature capabilities of SiC in power supplies, an integrated SiC converter has been designed that is also high-temperature capable.

Herein, the properties of SiC integrate circuit (IC) processes are discussed and nonlinear-carrier (NLC) control is proposed as a controller topology that can work within the design challenges presented by SiC. A boost converter with an NLC controller is demonstrated in simulation with circuit blocks built entirely from SiC IC models.

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Chapter 1

Introduction, Motivation, and Background

1.1 Power Electronics Controllers

Power Electronics is one of the most important fields in Electrical Engineering research, and within power electronics, switch mode power supplies (SMPS) can be found in a wide variety of applications—electric vehicles, portable electronics, spacecraft, etc. These SMPS typically consist of circuits like DC-DC converters or AC-DC rectifiers plus a control circuit that keeps the output voltage and power dissipation well regulated. The output voltage of a DC-DC converter or AC-DC rectifier is meant to be kept at a constant value $v_o(t) = V$ despite disturbances to the input voltage, load current, or nonidealities within the circuit elements. So while the output voltage of a typical converter circuit is related to the input voltage by the duty cycle, $d(t)$, it is not enough to simply set a constant duty cycle and trust that the output voltage will stay constant. It is preferable to employ feedback control to dynamically adjust the duty cycle to obtain a specific output voltage regardless of variation in input voltage, load current, or variance in component values. This is known as pulse-width modulation (PWM) control.

Typical feedback loop regulation is pictured in Figure 1.1 [6].

Figure 1.1(a) shows an example DC-DC converter, the boost converter, along with a power input, a load resistance, and control network. Output voltage, V_{out}, is multiplied by

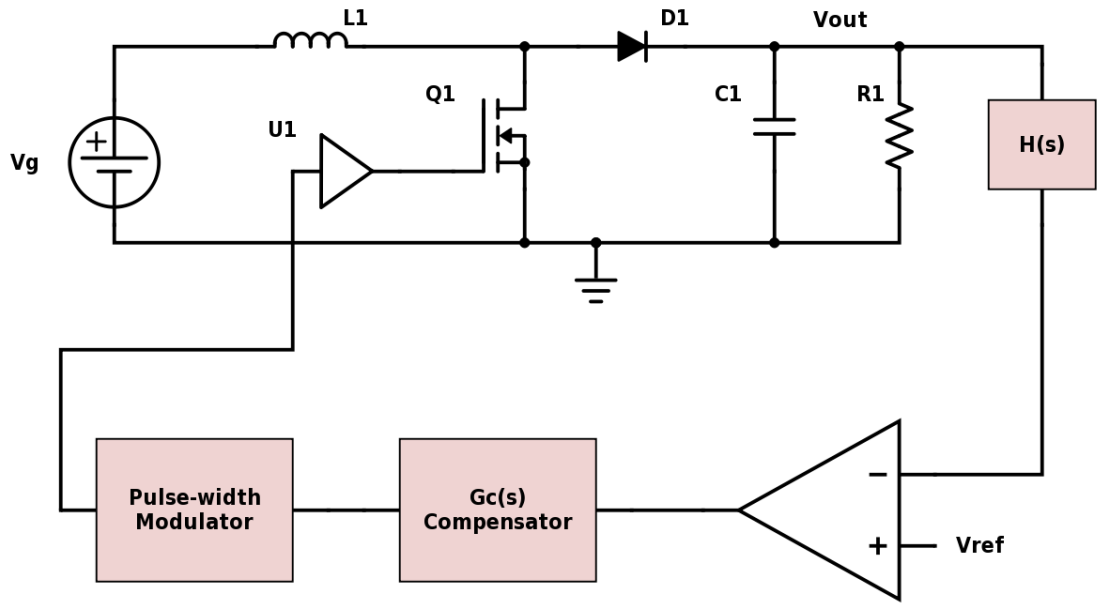

Figure 1.1: Example boost converter with feedback loop for regulation of the system output voltage

sensor gain $H(s)$, typically a voltage divider, and compared to a reference input V_{ref}. The difference between the two values generates an error voltage. Ideally feedback of the system would adjust v so that $v \times H(s) = V_{\text{ref}}$ and error voltage, $v_e = 0$, but practically speaking, the error voltage will never be exactly zero. The compensator, $Gc(s)$, amplifies the error voltage by a large gain so that even a small error can be used as a control signal, v_c, to set the duty cycle of the pulse-width modulator, ultimately setting the output voltage.

Error amplifiers, compensators, and other control signals needed within specific implementations of controllers are typically generated with op-amps, so the reliability of the controllers to properly regulate the output voltage of a SMPS can depend on the performance and the reliability of the op-amps themselves. Assuming a narrow temperature range around room temperature and terrestrial environments with low radiation, Silicon (Si)-based op-amps can be considered to be reliable for controller applications. But if those assumptions are violated, impact on op-amp performance must be considered.

1.2 High Temperature Power Electronics

Power Electronics circuits are important in a wide variety of applications, and different applications can present different environments in which the circuits must be functional and reliable. For example, electric/hybrid cars and space flight can present extremely high temperatures for power electronics to withstand. One example space flight application is the power processing unit for solar electric propulsion presented by NASA JPL [2].

In the above PPU, the benefits of SiC in the converter are discussed, but no high temperature solution for the support electronics such as PWM feedback control or gate driver are discussed. Chapter 2 will demonstrate that this is a common theme. High temperature capable converter circuits utilizing SiC power devices are common, but in order to see the full benefits of this high temperature capability, support electronics must also be high temperature capable, or else they will become the system weak link.

1.3 Thesis Organization

This thesis is organized as follows. Chapter 2 is a literature review covering the present state of the art in SiC integrated circuits, present state of the art in high temperature power converters, and an overview of NLC literature. Chapter 3 is a problem statement which details mathematically the problems presented by the conventional PWM controller topology when using SiC building blocks. Chapter 4 details the Nonlinear-carrier controller, providing a novel mathematical model describing it, simulation results verifying the model, and an example boost converter with NLC control created with entirely SiC IC subcircuits. Chapter 5 contains concluding remarks and future work.

Chapter 2

Literature Review

2.1 SiC Integrated Circuits

Due to the intrinsic material properties, SiC has been shown to have advantages over silicon based devices, including higher temperature capability and higher voltage operation [3]. SiC power devices provide an opportunity to create very high temperature power electronics circuits such as DC-DC converters. This high temperature capability allows for functionality in extreme environments such as space exploration, high temperature electric motor sensors and control, down-hole instrumentation, etc. However, the high temperature functionality of these power electronics circuits can be limited by the high temperature capability of their support electronics, such as PWM controllers and gate drivers. SiC IC technology that can provide highly integrated systems but still maintain the high temperature capability inherent to SiC could be impactful toward the advancement of highly integrated high temperature power electronics systems.

SiC IC design has properties that are both advantageous and disadvantageous in terms of designing high temperature integrated circuits for power electronics applications compared to silicon. GE reports that their SiC integrated analog and digital circuits can operate reliably in a 300°C environment [8]. Though high temperature operation is the primary advantage, GE goes on to describe the primary disadvantages of their SiC MOSFETs: low mobility, negative temperature coefficient of resistance, and no mature PMOS device [8]. Op-amps designed with SiC NMOS devices demonstrated just over 40 dB of gain at low frequencies at

both room temperature and 300C with a 3 dB frequency of about 1 kHz at room temperature and 10 kHz at 300°C [8]. GE demonstrates higher gain op-amps at high temperature, but they require supply voltages of 30 or 40 V [14].

Raytheon has demonstrated SiC CMOS circuits (including PMOS devices) up to 350°C [4] [12], but note that SiC MOS work has primarily focused on NMOS technology because bulk electron mobility is 8 to 9.5 times higher than hole mobility [4]. Aside from low hole mobility, another limitation of Raytheons process is SiC MOSFET threshold instability, which they have mitigated with auto-zeroing switched capacitor approaches in their analog circuit designs [12] [9].

Other researchers using Raytheons technology have presented CMOS circuits [11]. They demonstrate current references, a voltage reference, a miller compensated two stage OTA, a folded cascode OTA, and a Schmitt trigger [11]. In simulation, the Miller compensated OTA had 61.3 dB of gain at room temperature dropping to 40.8 dB at 300°C. The folded cascode OTA only varied from 61.5 dB to 65.7 dB over that temperature range. These op-amps were fabricated and tested over temperature and seem to perform well, though at the time of publication they had not finished the temperature testing and seemingly omitted a table which was meant to be included in their test results.

Also using the Raytheon CMOS process, a SiC IC gate driver was presented [1]. In this paper, functionality driving a SiC power MOSFET at over 500°C was demonstrated.

So, while SiC IC design technologies offer extended high temperature capability compared to Si, circuits designed with SiC MOSFETs are very low performance. As Chapter 3 will discuss, low performance analog circuits can negatively impact PWM feedback control.

2.2 High Temperature Power Electronics Converters

A SiC based Three-Phase AC-DC rectifier was designed for > 100°C ambient temperatures [15]. In this work, a three phase AC-DC boost rectifier was designed with a SiC power module capable of operating up to 250°C. This work correctly points out that not only does the rectifier circuit need to be high temperature capable, but so do the gate driver and control electronics. In this case, they selected voltage control electronics built with

Silicon-on-Insulator (SOI) technology, giving the controller some inherent high temperature capability by process. The end result was a system capable of achieving greater than 100°C operation. The drawback of the control scheme used is that there was no attempt to program input current. Additionally, SOI processes are more expensive than comparable standard CMOS processes.

High temperature capable SiC based MOSFET power modules with integrated SOI gate drivers have also been demonstrated [16]-[17]. While these power modules would eventually be a good candidate for high temperature capable control, currently they are demonstrated in open loop. In both cases, they demonstrate junction temperatures that exceed 225°C.

A high temperature capable SiC power factor correction (PFC) rectifier is presented [5]. The authors test their circuit up to 150°C and use a Texas Instruments TMS320LF2407A DSP IC as their controller, but give no insight into the specific controller topology. They also do not specify a gate driver. The authors dont explicitly detail how they dealt with high temperatures regarding the support electronics nor do they specifically state that those support electronics were heated along with the PFC rectifier.

Another publication showing power conversion in extremely high ambient temperatures demonstrates SMPSs at 400°C, but not only are the converters operated in open loop, but they also isolated the SiC power devices and only heated those, leaving out the passive components [7].

Finally, a high temperature SiC DC-DC boost converter is presented [20]. This research specifically measures the junction temperature of SiC power switches when operated at ambient temperature in boost converter configuration. Again, no feedback control was used in in this implementation.

It can be observed that the primary method of making a power converter high temperature capable is by using SiC power devices. However, in these publications little information about controller solutions is offered. In one case, the controller was designed in an SOI process [15], but its temperature capabilities arent as high as can be achieved by the SiC power devices. In other examples, no feedback control was presented. If SiC IC processes can be used to design the gate drivers and controllers to support SiC converters, small, lightweight, extremely high temperature power electronics could be achieved.

2.3 Nonlinear-carrier Control

Nonlinear-carrier (NLC) control is a form of current programming that uses a nonlinear current control signal. In most applications, the inductor or switch current is integrated for comparison to the nonlinear control signal, making it charge nonlinear-carrier control.

NLC control is first introduced for high-power-factor boost rectifiers [10]. In this implementation, the switch current is integrated into a capacitor, and the capacitor is reset once enough charge is stored to match the nonlinear control signal. The nonlinear control signal is derived and generated with two op-amp integrators and reset switches. Due to the low performance of SiC op-amps presented in Chapter 1 and 2, the op-amp dependence could lead to reliability concerns.

However, NLC is refined and presented for flyback, cuk, and sepic converters [18] and up-down switching converters [19]. In this iteration of NLC control, an exponential carrier waveform is introduced to be used in place of the ideal nonlinear carrier waveform. The two op amp integrators are replaced with a switch and an RC network, making generation of the carrier passive. Passive generation of this critical signal is the key attribute of NLC that makes PWM control with low performance analog possible. Details of the Nonlinear-carrier Controller are presented in Chapter 4.

Chapter 3

Problem Statement

3.1 Linear-carrier Controller and Model

Chapter 1 discusses Switch Mode Power Supplies (SMPS) at a high level, but provides no insight into how control signals might be generated within specific control topologies. Generally, voltage and current signals from a SMPS are used as control signals, so those signals typically interface to the controller via op-amps. Op-amps can either directly replicate a signal or provide signal conditioning—gain, attenuation, integration, etc. The underlying assumption is that there will be available an op-amp that can perfectly replicate the needed SMPS signals or perform whatever conditioning may be needed effectively and reliably. In fact, in most controller derivations, the underlying assumption is that op-amps are ideal, and little or no attention is paid to the role that op-amps play. Wit high performance Si in typical operating conditions, this assumption is valid. But in low performance analog situations, such as when designing in SiC IC processes, nonidealities must be accounted for.

In particular, the generic controller in Figure 1.1 is often implemented as a current-programmed controller, or as it will be referred to herein, a linear-carrier (LC) controller. In LC controllers, the controller relies on the comparison of linear waveforms. One waveform is a duplication of the inductor current, and another linear waveform must be generated internally in order to achieve stability when the duty cycle is above 50% [6].

Figure 3.1 is a boost converter with an LC controller. The output of the boost converter is scaled down with a voltage divider and compared to a reference voltage. The op-amp

integrator works both as a difference circuit and a high gain compensator. Above that op-amp is a current mirror used to generate the linear compensation ramp. A DC current is driven onto a capacitor, creating a linear voltage waveform, then at every narrow pulse clock signal, the capacitor is discharged and reset to ground. For stability, that linear compensating ramp must be subtracted from the DC value at the output of the op-amp comparing the output to the reference. A second op-amp accomplishes generation of this control signal and sends the output to the inverting terminal of a comparator. This control signal must be compared to the inductor current, or in this example, the rising edge of the switch current. In order to generate the comparison signal, a small sense resistor is placed in series with the switch so that a voltage signal can be compared to the control signal. The output of this comparison drives the reset of an SR latch to reset the system and turn the switch off. The switch is then automatically turned back on by a narrow pulse clock signal driving the set side of the SR latch. Once a clock pulse turns the switch on, it stays on until enough current has flowed through the inductor and therefore the switch to match the control signal generated by the op-amp network. Once V_{sense} is greater than the control signal, the comparator switches high and Q switches low, turning off the switch.

The inductor current, i_L, and control current, i_c, are pictured in Figure 3.2. Inductor current rising edge slope is defined as m_1 and falling edge slope is defined as m_2. The compensation ramp slope is defined as m_a.

In the example from Figures 3.1 and 3.2, the compensation ramp is generated by op-amps. Therefore, we must consider how any op-amp imperfections may impact overall system performance. First, we consider the importance of the assumed linearity of the compensation ramp.

For LC controllers with ideal control waveforms, a unified modulator (or controller) model has been established [13]. The current-loop gain transfer function relating inductor current to the control current is derived to be

$$\frac{i_L(s)}{i_c(s)} = \frac{1}{1 + \frac{1}{Q_s}(\frac{s}{\frac{\omega_s}{2}}) + (\frac{s}{\frac{\omega_s}{2}})^2} \tag{3.1}$$

where the converter stability parameter, Q_s, is defined as

$$Q_s \equiv \frac{2}{\pi(\frac{D'}{D'_{\min}-1})} \tag{3.2}$$

and

$$D'_{\min} \equiv \frac{0.5}{(1+\frac{M_a}{M_1})} \tag{3.3}$$

and D is the portion of a switching cycle where the power switch in the SMPS is turned off, or $1-D$, where D is the duty cycle. Because the current transfer function fits a standard low-pass quadratic with Q-factor Q_s, the stability of the system is controlled by the compensation ramp slope, M_a. As Q_s approaches infinity, the system becomes less stable and will eventually oscillate. It can be observed that as M_a decreases, $D'_{\min}$ increases and approaches D'. A s$D'_{\min}$ approaches D', the system becomes less stable, eventually oscillating if the condition $D > D'_{\min}$ is violated. It is a well-known conclusion [6] that if the compensating ramp is flat ($M_a = 0$), then the system will oscillate at $D > 0.5$, and in order to achieve stability across all values of D, $M_a \geq 0.5 \times M_2$ must remain true.

Therefore, the stability of converters that use LC current-programmed controllers depends on the assumption that a linear compensating ramp with a known slope is available. But as op-amp performance deteriorates, linearity can be compromised, and it can no longer be assumed that M_a is perfectly linear. If the slope varies, so does stability of the system.

3.2 Linear-carrier Controller Simulations

In the boost converter from Figure 3.1, a system simulation was constructed where $V_G = 24V$, $V_{\text{out}} = 100V$, switching frequency $f_s = 100kHz$, and the inductor $L = 300\mu H$.

First, the required compensation ramp for stability across all duty cycles was generated in simulation with op-amp macromodels, varying gain and gain-bandwidth-product. Next, the slopes of the resulting compensation ramps were extracted, and those values were plugged into a Matlab model of the LC system.

Figure 3.3 shows how the compensation ramp deteriorates as open loop gain of the op-amps deteriorate. At the highest gain, 120 dB, the slope is ideal: $M_a = 0.5 \times M_2$. However,

as gain decreases, so does the linearity and slope of M_a. And as Chapter 3.1 demonstrates, this decrease in slope predicts that the system current transfer function will become unstable.

Using Matlab, the values for slope obtained in 3.3 were plugged into the model described in Section 3.1. Bode plots were generated, and phase margin is observed for stability.

Figures 3.3 to 3.7 taken together show that as op-amp open loop gain decreases from 120 dB to 80 dB, the compensation ramp slope decreases from the expected $0.5 \times M_2$ to $0.19 \times M_2$. This change in slope results in the phase margin decreasing until it becomes negative, implying that the overall system is now unstable. These simulations show a direct connection from op-amp performance to system stability when using an LC controller.

3.3 SiC Op-amp Design

The Integrated Circuits and Systems Laboratory (ICASL) at UT designed all the required components for an LC controller, including an op-amp, comparator, SR latch, and oscillator circuits in GE's SiC IC process.

Schematics and performance specifications for each of these circuits can be found in the Appendix. However, because it has been shown that op-amp performance is critical to stability of the LC controller, it is worth paying particular attention to the design of the op-amp.

Designing in GE's SiC process presented several challenges. The process offers only enhancement and depletion NMOS transistors, no PMOS transistors. The NMOS devices, particularly the enhancement NMOS, have poor transconductance compared to Si. The minimum feature size, $3\mu m$, is generations behind Si. Additionally, the only routing layers were a poly-Si and one metal layer. Finally, the models were very immature.

As a result, SiC circuits designed in GE's process tend to have large layouts and be very low performance.

The SiC op-amp schematic is seen in Figure 3.8. The op-amp is a self-biased design that provides bias-point temperature tracking. By utilizing a depletion-mode NMOS input stage, an input common-mode range of 0 to $7.6V$ is achieved. No resistors are used in this design; all loads in this op-amp are depletion mode devices.

The low-gain differential input pair feeds a floating voltage source cascode structure. The input stage is followed by a temperature-tracking, high-gain common source stage. A low-gain, low-impedance output stage buffers the op-amp output and restricts the bias point movement of the high-gain, common-source stage. Temperature-tracking compensation ensures stable operation over temperature.

Table 3.1 below shows performance at both high temperature and room temperature.

Table 3.1: SiC Op-amp Simulation Results

Temperature	300°C	25°C
DC Gain	64 dB	50 dB
3-dB Frequency	70 Hz	230 Hz
Unity Gain Bandwidth	100 kHz	100 kHz
Phase Margin	80°	64°
Input Common Mode Range	0 - 7.6 V	0 - 9.14 V
Offset Voltage	1.03 mV	19.6 mV
Supply Current @ 24V	2.47 mA	5.21 mA

3.4 Conclusion

Taking the results from Sections 3.2 and 3.3 together, it can be concluded that the SiC-op amp is not high performance enough to produce a stable LC controller. In fact, the op-amps are so low performance, UT never properly generated anything close enough to a linear compensation ramp with a controllable slope to even attempt system level simulations. The output waveforms looked flat on a cycle-by-cycle basis. The LC controller was a non-starter, as it was sure to be unstable.

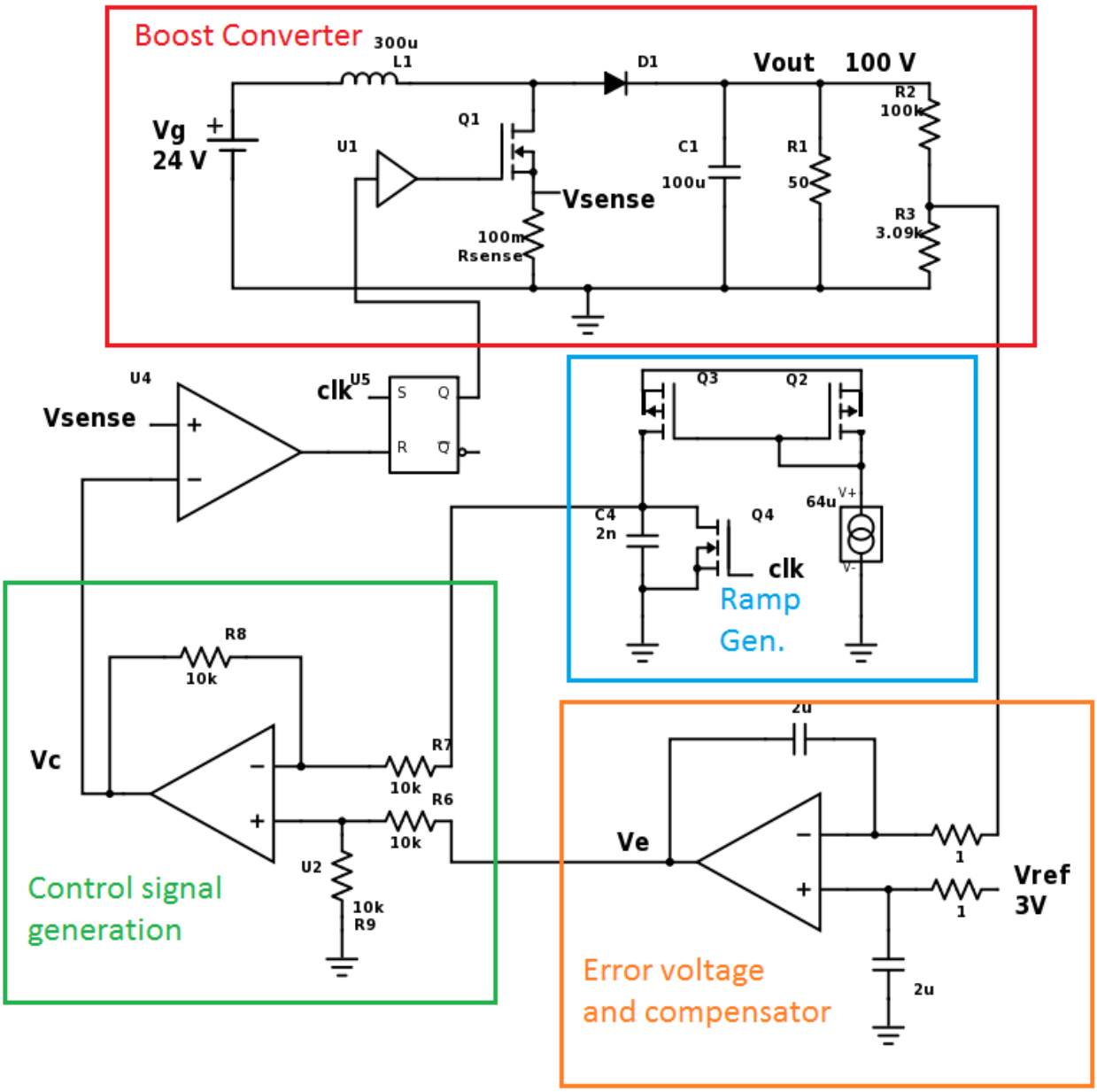

Figure 3.1: Example boost converter with linear carrier controller

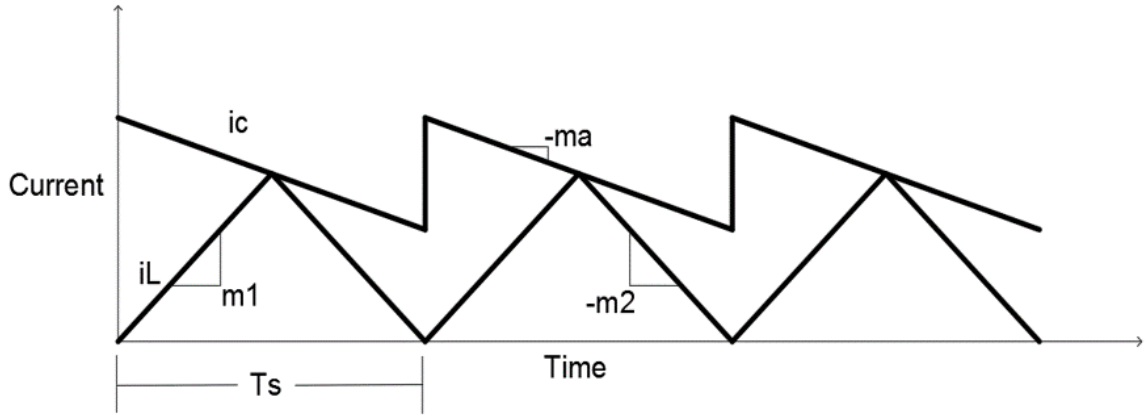

Figure 3.2: Inductor current (i_L) with slopes m_1 and m_2, control current (i_c) with slope m_a

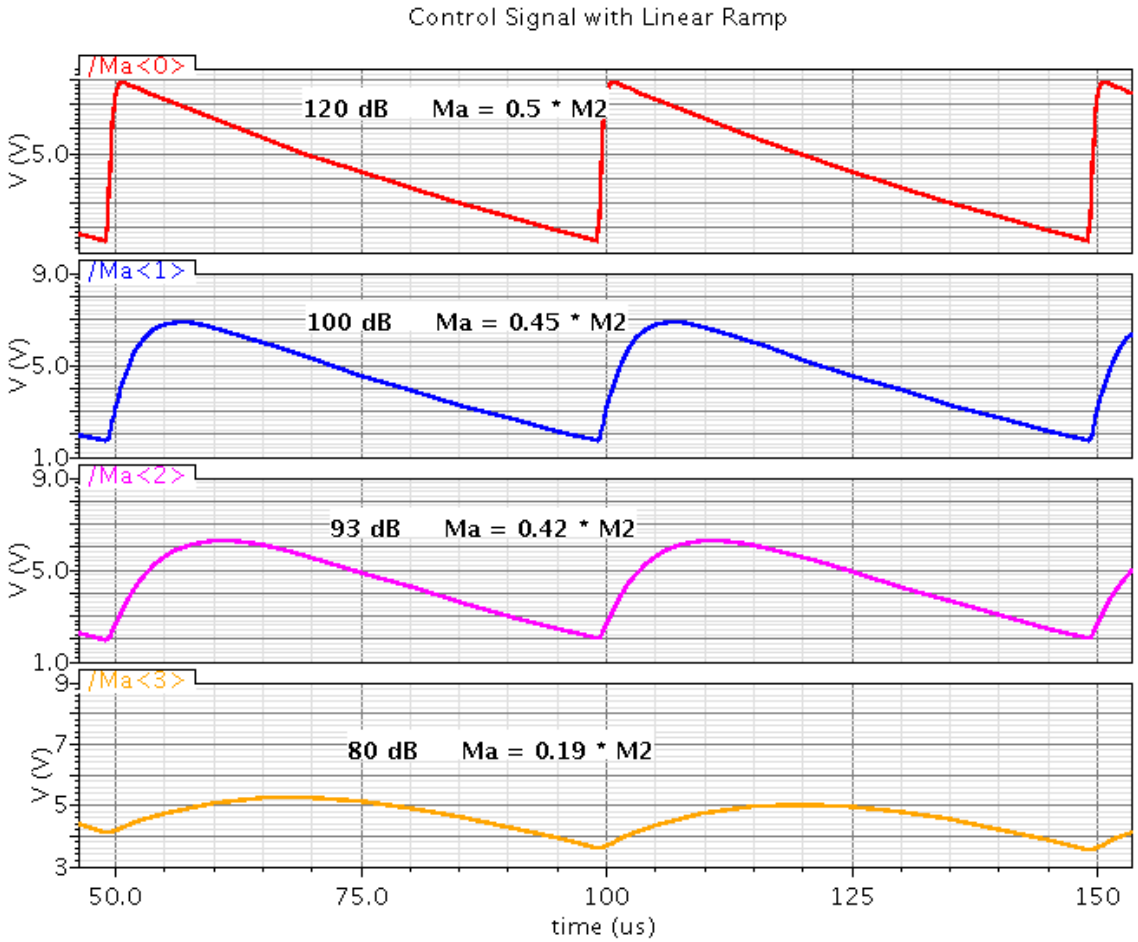

Figure 3.3: Compensation Ramp Simulation Across Op-amp Open Loop Gain

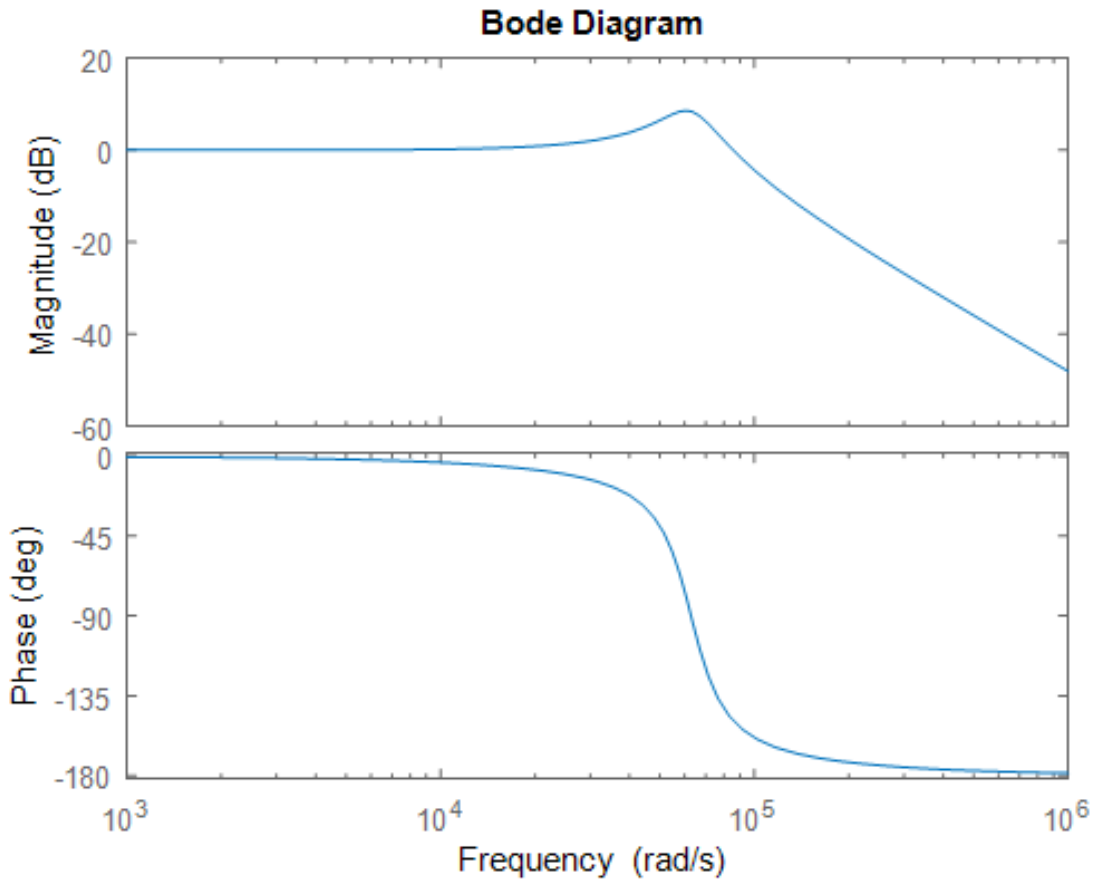

Figure 3.4: Bode Plot of Current Transfer Function with Ideal $M_a = 0.5 \times M_2$. Phase Margin is 31°

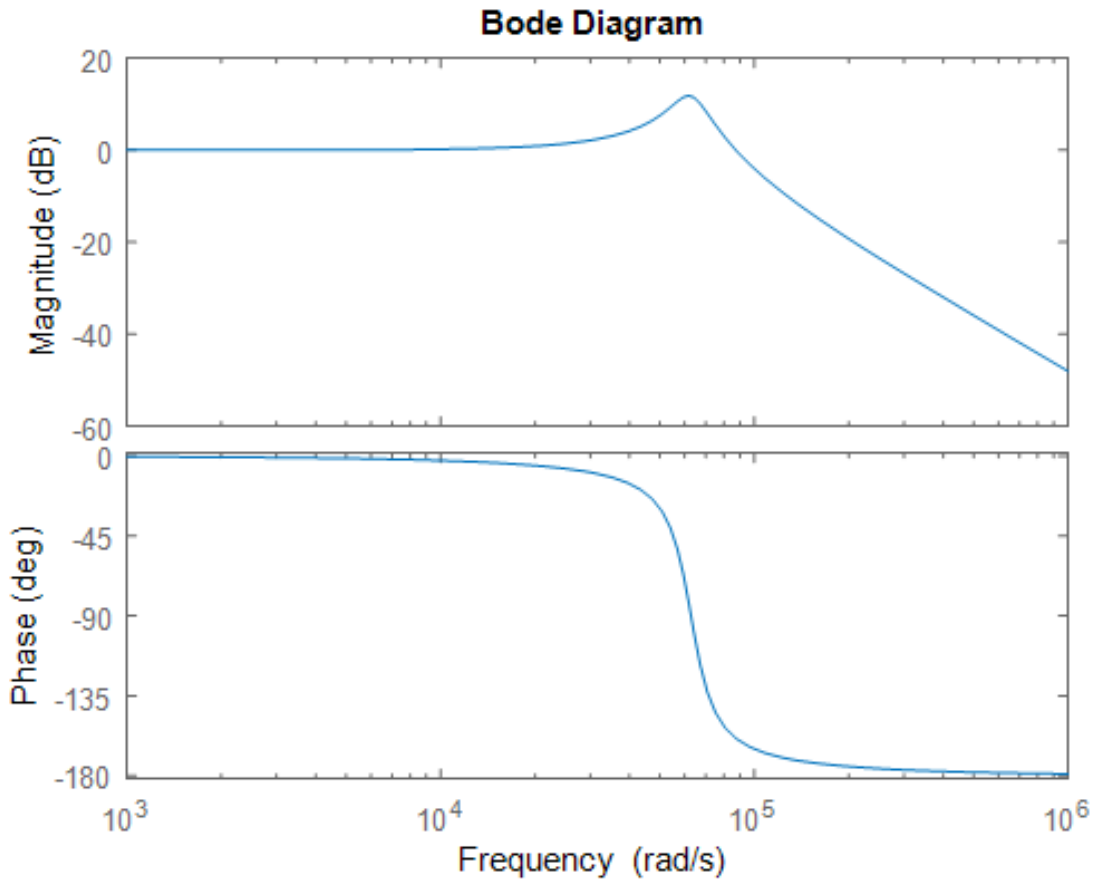

Figure 3.5: Bode Plot of Current Transfer Function with $M_a = 0.45 \times M_2$. Phase Margin is 21°

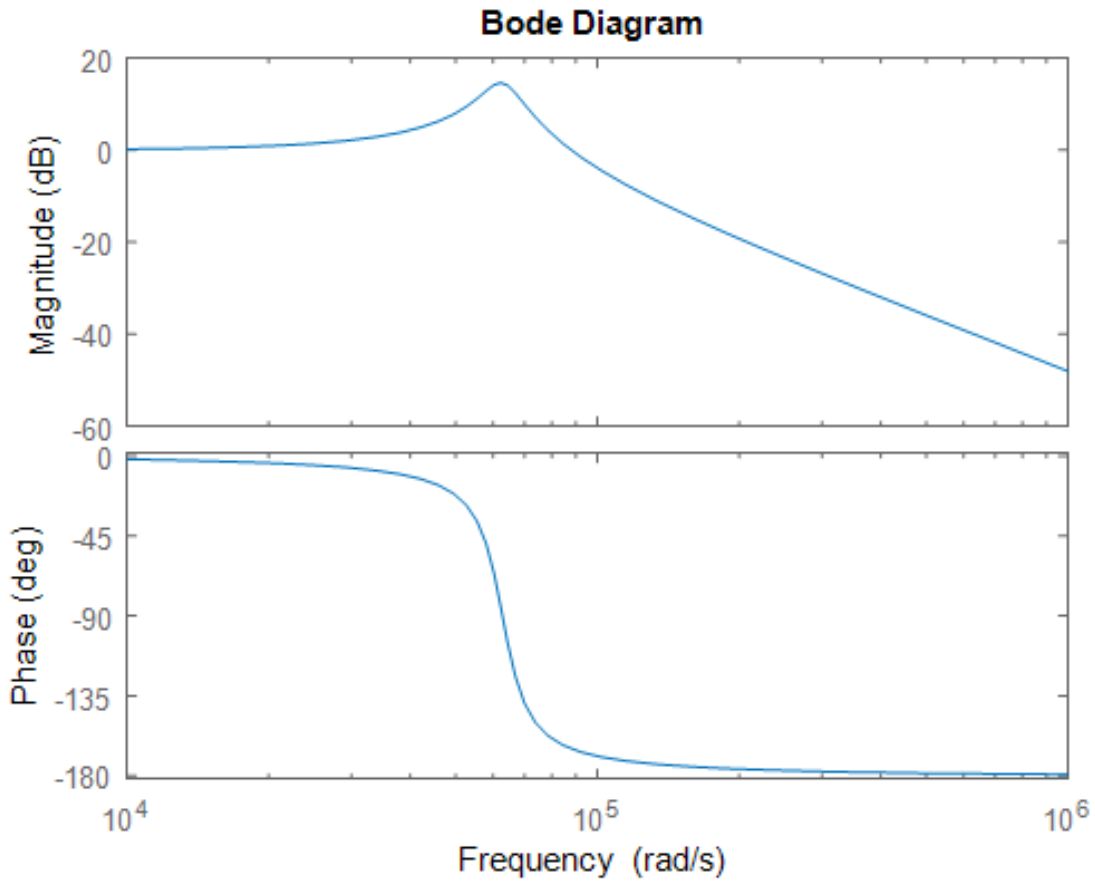

Figure 3.6: Bode Plot of Current Transfer Function with $M_a = 0.42 \times M_2$. Phase Margin is 15°

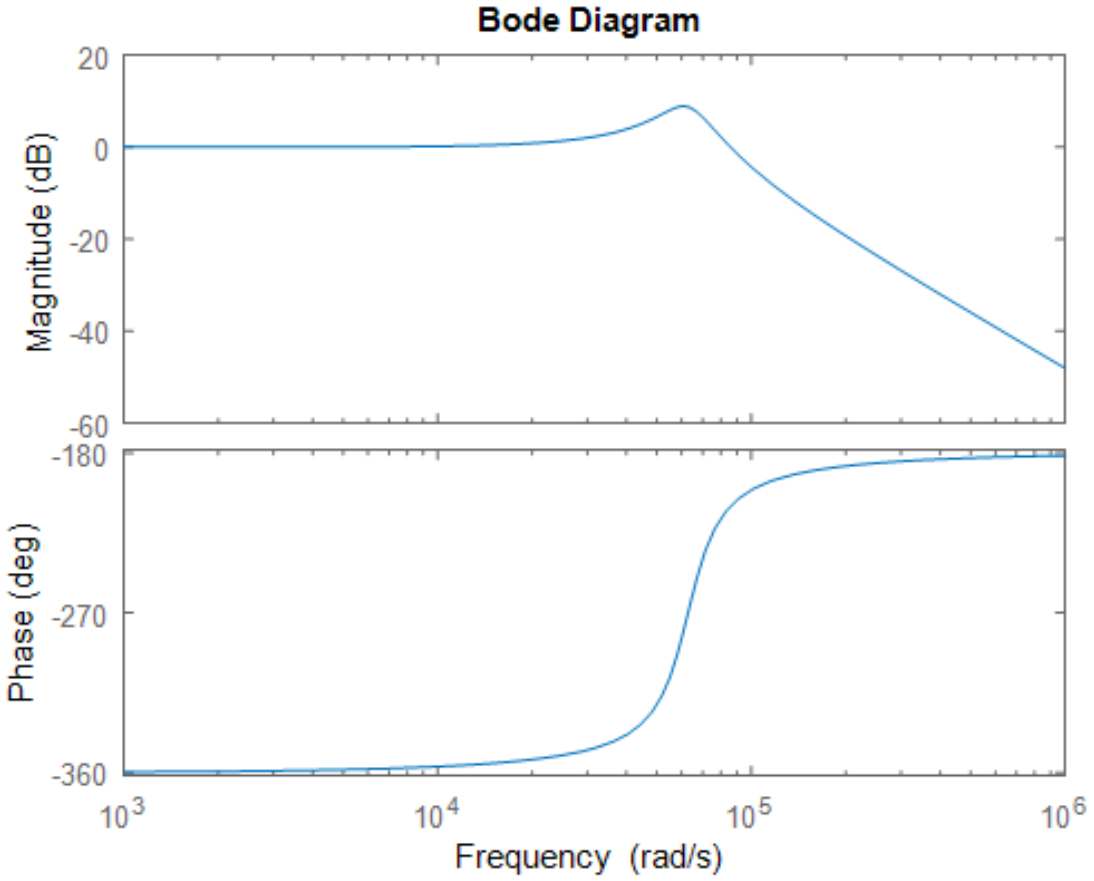

Figure 3.7: Bode Plot of Current Transfer Function with $M_a = 0.19 \times M_2$. Phase Margin is $-30°$

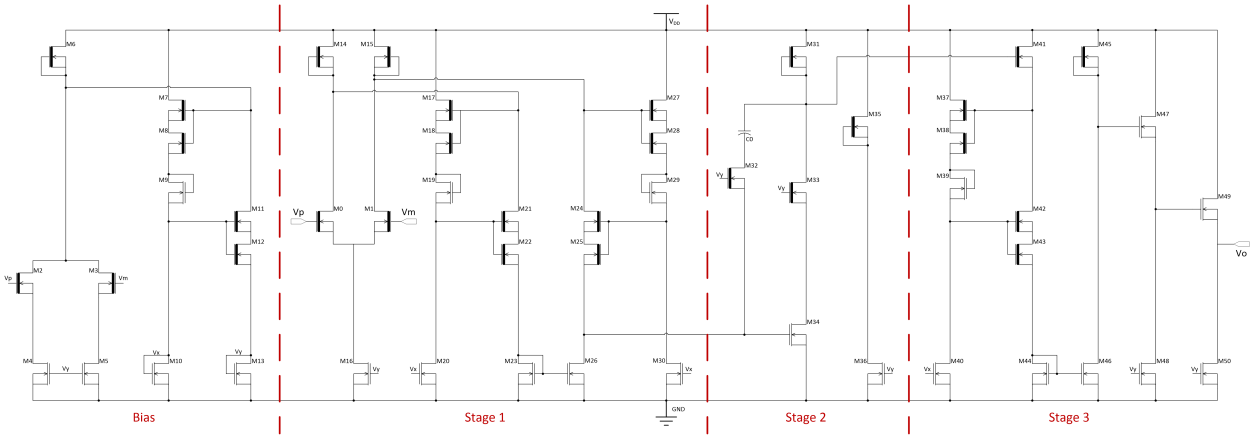

Figure 3.8: Three Stage SiC Op-amp designed with Enhancement and Depletion NMOS Transistors

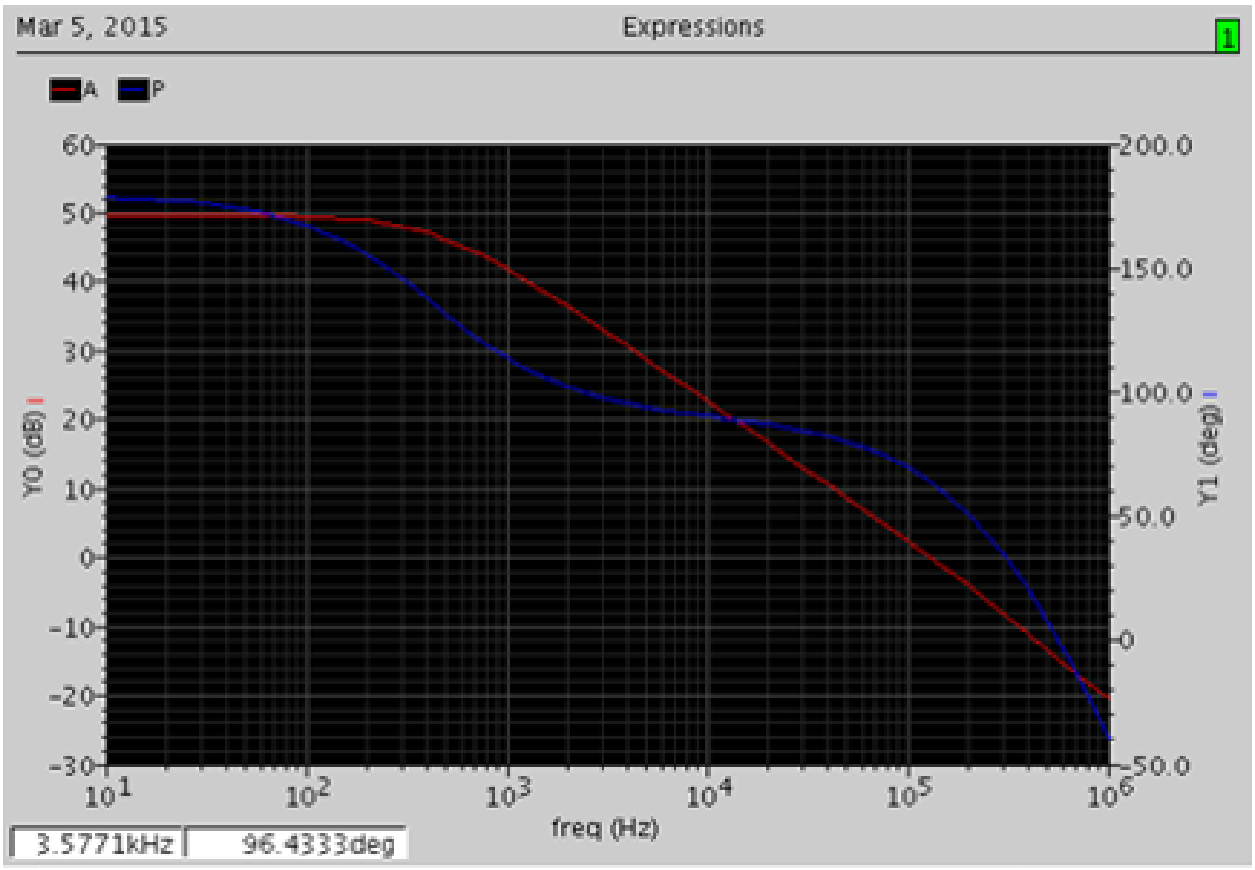

Figure 3.9: Bode Plot of the SiC Op-amp at Room Temperature

Chapter 4

Nonlinear-carrier Control for a SiC Boost Converter

4.1 Nonlinear-carrier Controller and Model

Due to the fact that SiC op-amps are not suitable to generate highly linear waveforms reliably, a topology that does not rely on linear waveforms must be chosen. As reviewed in the Literature Review in Chapter 2, Nonlinear-carrier (NLC) control is a version of current programmed control that uses a nonlinear carrier waveform rather than a linear compensation ramp.

Topologically, it is quite similar to LC control, but instead of using a DC current driving a capacitor to generate a line, then subtracting that line from the DC compensator voltage, the DC compensator voltage is simply discharged through an RC, generating an exponential waveform.

At present state of the art, it is presented strictly as an AC-DC rectifier used for power factor correction, where shaping the exponential carrier to closely match the input voltage provides for a well controlled power factor. It has never been presented for DC-DC conversion, and therefore the existing models are lacking in that application.

Presented in this section is a novel model based on the LC controller model, but modified to replace the linear compensation slope with a nonlinear exponential.

Figure 4.1 is the same boost converter as seen in 3.1, but with an NLC controller in place of the LC controller. The op-amp here performs the same task as the op-amp in the LC controller. It acts as a difference amplifier and integrator providing high gain compensation at low frequencies to generate a control signal. In the LC controller, there needed to be a current mirror and capacitor generating a linear waveform plus another difference amplifier to subtract this linear waveform from the DC control signal. In the NLC controller, the output of the op-amp simply has to charge the RC network, R_C and C_C, on the narrow pulse clock, then allow those passive components to discharge, creating the compensation waveform, v_c. Then, like in the LC controller, this waveform is used for comparison to the rising edge of the switch current which is identical to the rising edge of the inductor current, and when inductor current becomes greater than the control signal, the power switch in the boost converter is turned off until the next clock cycle.

Figure 4.2 shows v_c and v_{sense} in steady state operation. When the power switch in the boost converter is on, current flows through the inductor, switch, and sense resistor generating the blue waveform. Meanwhile, the control signal (green waveform) is set to a DC value during the narrow pulse clock and allowed to decay. When the sense voltage matches the control voltage, the comparator flips, turning off power switch, setting current through the power device and sense resistor back to zero until the next clock cycle.

This is similar to the waveforms for the LC controller in Figure 3.2, but the line with slope M_a has been replaced with the exponential decay waveform.

In practice, this is the same type of control seen in the LC controller, but rather than a compensation ramp with a steady slope, the compensation ramp slope varies with duty cycle, as seen in Figures 4.3 - 4.5. In those figures, the blue line represents the exponential decay, and the red line represents an equivalent linear compensator for a given duty cycle. If the duty cycle is 25%, the slope is large in magnitude. As the duty cycle increases, the slope magnitude decreases.

Mathematically, v_c can be defined as a system of equations:

$$v_c = V_M \text{ if } 0 \leq t \leq D_{\min} T_s \tag{4.1}$$

$$v_c = V_M e^{\frac{-(t-D_{\min}T_s)}{R_C C_C}} \text{ if } D_{\min}T_s < t \leq DT_s \tag{4.2}$$

where V_M is the starting DC value to which the RC network is charged during the time when the clock pulse is high. This is the minimum duty cycle, $D_{\min}$, multiplied by the switching period, T_s. After this minimum duty cycle portion of the switching period where the clock is high, the clock goes low, the switch in series with the op-amp and RC network is turned off, and the charge in the RC network decays exponentially until T_s, the full length of the switching period. As can be observed in equation 4.2, the value of v_c depends on the duty cycle, D. So depending on the duty cycle, the value of the equivalent slope at a given point in time can be defined as

$$M_a = -\frac{V_M - V_M e^{\frac{-(DT_s - D_{\min}T_s)}{R_C C_C}}}{DT_s} \text{ for } t = DT_s \tag{4.3}$$

Then M_a can be substituted into the definition for $D'_{\min}$, which is substituted into Q_s, to obtain the transfer function ils/ics, duplicated here:

$$\frac{i_L(s)}{i_c(s)} = \frac{1}{1 + \frac{1}{Q_s}(\frac{s}{\frac{\omega_s}{2}}) + (\frac{s}{\frac{\omega_s}{2}})^2} \tag{4.4}$$

$$Q_s \equiv \frac{2}{\pi(\frac{D'}{D'_{\min}-1})} \tag{4.5}$$

$$D'_{\min} \equiv \frac{0.5}{(1 + \frac{M_a}{M_1})} \tag{4.6}$$

As in Chapter 2, Ma still impacts the stability of the system, but now instead of being a single value, it varies with duty cycle. However, considering that V_M and T_s are set by the system, insuring stability across all duty cycles can be accomplished simply by sizing R_C and C_C appropriately.

$D \geq 0.5$ is the condition for risk of instability. M_a gets small as D increases from 0.5 to 1, increasing risk of instability. Therefore, the worst case scenario for stability is at $D = 1$. Therefore, to ensure stability across all duty cycles, M_a can be rewritten:

$$M_a = \frac{1}{2}M_2 = -\frac{V_M - V_M e^{\frac{-(T_s - D_{\min}T_s)}{R_C C_C}}}{T_s} \tag{4.7}$$

Solving for $R_C C_C$ gives

$$R_C C_C = \frac{-T_s + D_{\min}T_s}{ln(1 + \frac{M_2 T_s}{2V_M})} \tag{4.8}$$

M_2 can be defined entirely by the size of the inductor in the boost converter, the boost converter input voltage, and the boost converter output voltage [6].

$$M_2 = \frac{-V_g + V_{\text{out}}}{L} \tag{4.9}$$

Plugging that definition for M_2 back into the equation for $R_C C_C$ provides a formula to size for $R_C C_C$ that is entirely defined by system parameters and will ensure stability over all duty cycles:

$$R_C C_C = \frac{-T_s + D_{\min}T_s}{ln(1 + \frac{(\frac{-V_g + V_{\text{out}}}{L})T_s}{2V_M})} \tag{4.10}$$

4.2 Linear-carrier Controller Simulations

The same boost converter from the LC simulations was simulated with NLC and op-amp performance was similarly degraded. NLC control waveforms were simulated with op-amp macromodels. A matlab simulation of the system was generated based on the model previously presented for comparison to LC. Next, macromodel and device level system simulations were performed to verify model.

As seen in Figure 4.6, the exponential decay NLC carrier waveform shows no signs of degradation across op-amp gain. Using the same macromodel op-amps degraded in the same way, the LC compensation ramp slope changed significantly in Chapter 3.

The waveforms generated in Figure 4.6 were then plugged into a Matlab system simulation, and as expected, because the NLC waveforms don't change, we see no change in

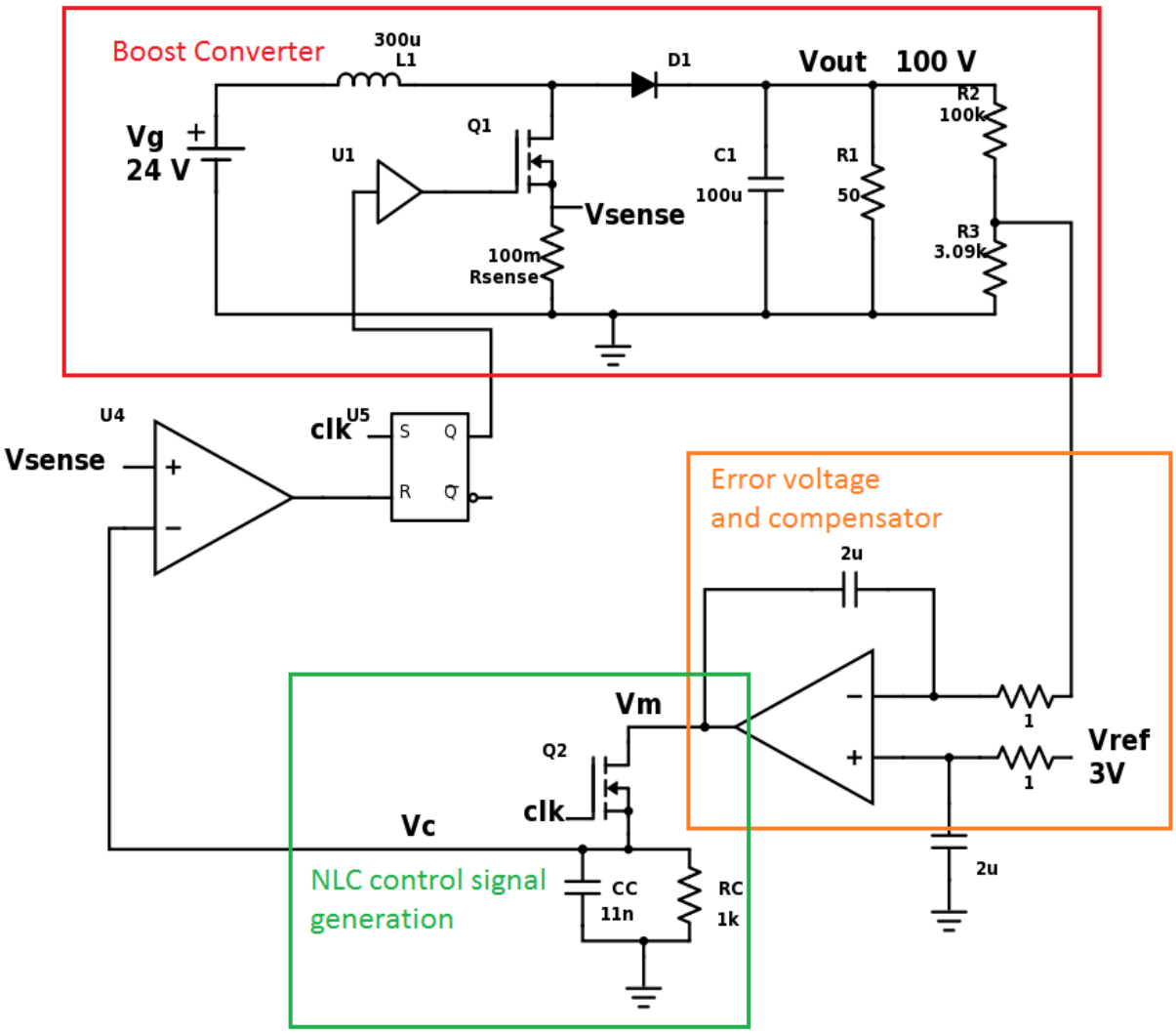

Figure 4.1: Example Boost Converter with Nonlinear-carrier Controller

the bode plots in Figures 4.7 - 4.10. Despite gain deterioration in the op-amp, stability is not sacrificed.

And in order to verify the system level functionality predicted in Matlab, LTSpice macromodel based simulations results are given in Figures 4.11 and 4.12. In these figures, a transient startup simulation is run, and the output voltage is plotted. The systems are identical, but in Figure 4.11, the op-amp open loop gain is 120 dB, and in Figure 4.12 the op-amp open loop gain is 80 dB. In both cases, there is an initial overshoot expected with a phase margin of 30°, and both systems settle to a steady state output of 100 V, as

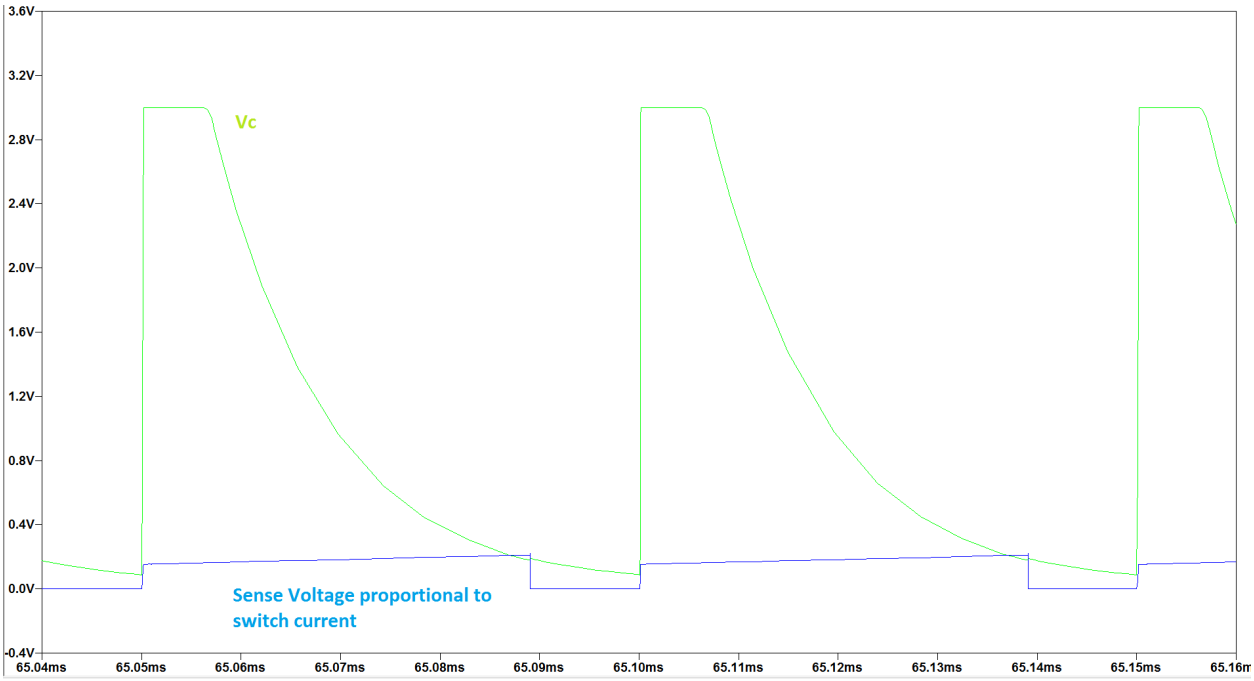

Figure 4.2: Steady-state v_c and v_{sense} waveforms

expected. Functionally, there is very little difference between the two systems across op-amp performance.

4.3 SiC Boost Converter with SiC Integrated NLC Controller

As the culmination of a NASA SBIR under grant NNX14CL20C with Frequency Management Inc., ICASL designed in simulation a NLC PWM controller for a DC-DC boost converter. Every necessary subcircuit for the PWM controller was designed using GE's SiC IC fabrication process design kit, and they were sent to GE for fabrication. Though the fabrication was attempted twice, it failed both times, so hardware was never tested.

However, the successful design of a functional system in simulation using only SiC MOSFETs is a promising result, and the simulations showed functionality at 300°C.

In the NASA SiC simulations, we designed a boost converter meant to boost an input of 24 V up to 48 V. The boost converter and controller topology are shown in Figure 4.13. The controller topology is the same as seen in Figure 4.1, but the Vsense value that tracks with

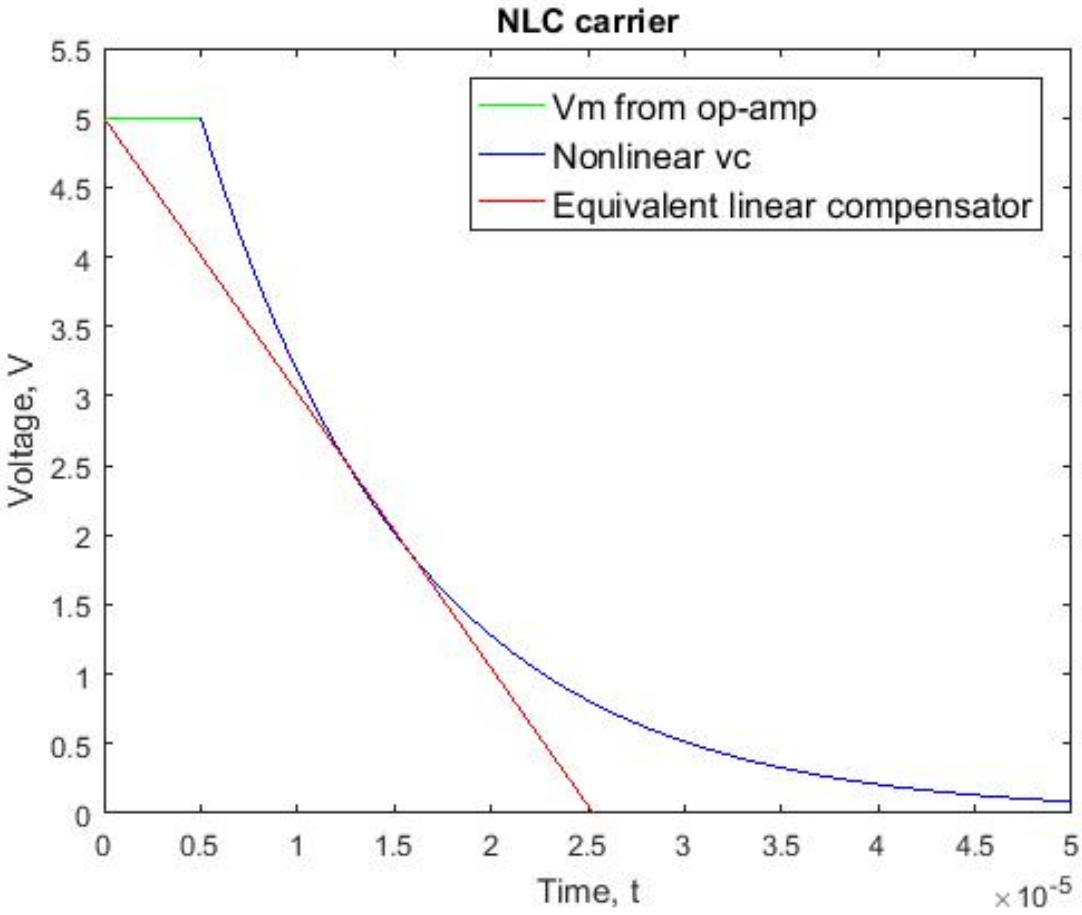

Figure 4.3: NLC Equivalent Slope for Duty Cycle, $D = 0.25$

inductor current is integrated before comparison to the nonlinear-carrier in order to protect against switching noise. This is a common technique seen in many implementations of NLC control.

Figures 4.14 and 4.15 show the steady state and step response results of the system. The expected output is 48 V, so the obtained output of 47 V represents about 2% error. The step response shows the output overshoot and settle to the steady state output voltage.

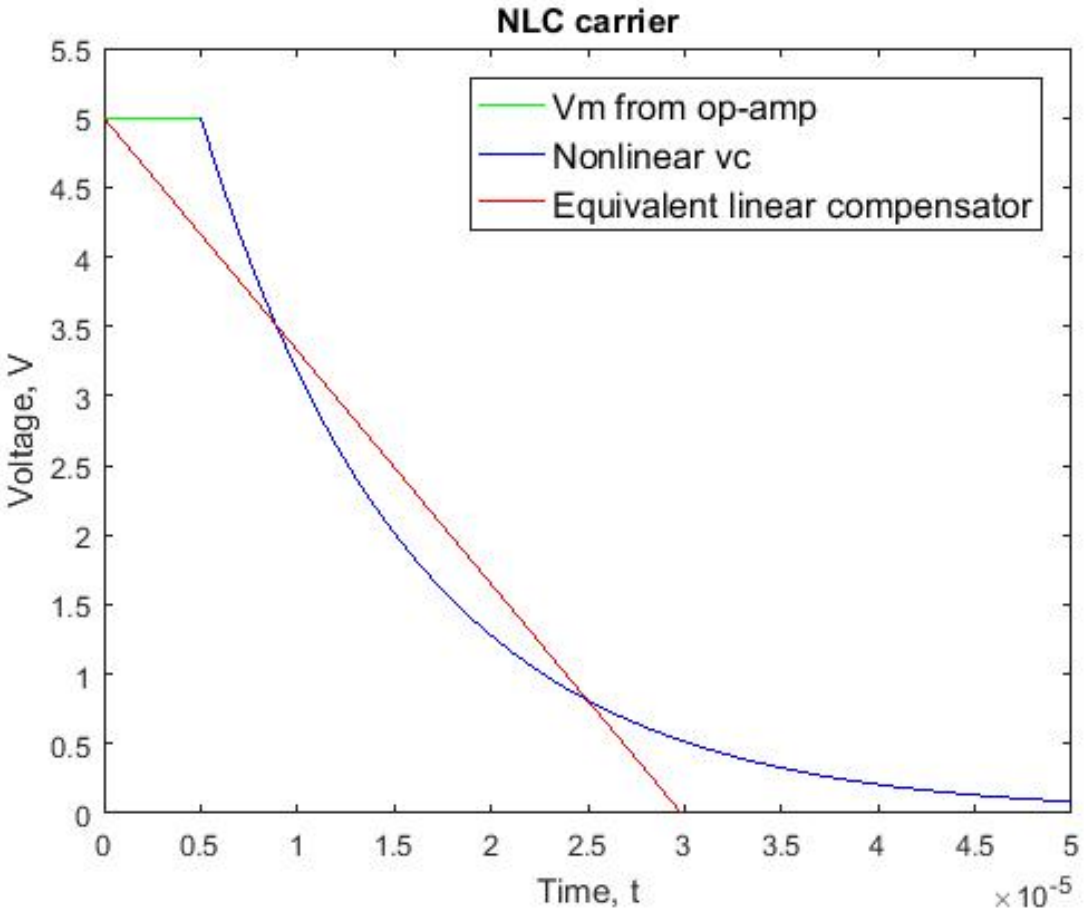

Figure 4.4: NLC Equivalent Slope for Duty Cycle, $D = 0.5$

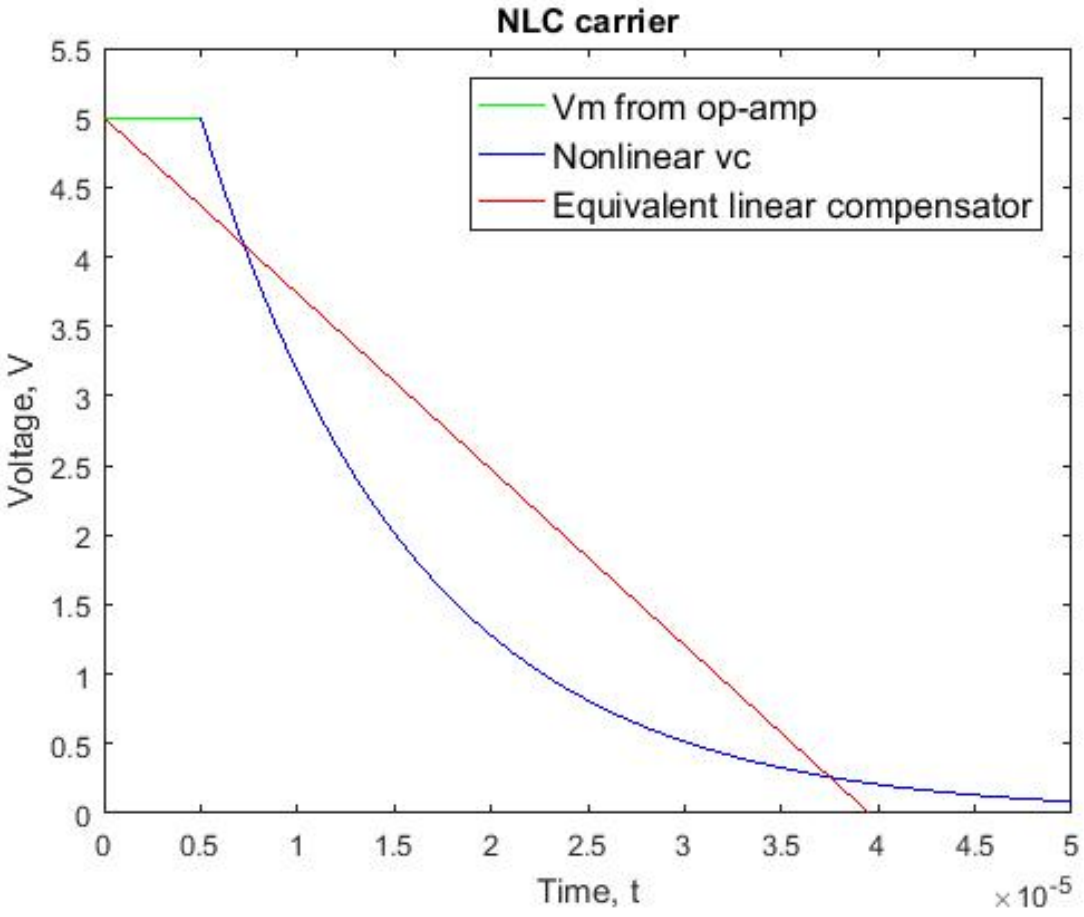

Figure 4.5: NLC Equivalent Slope for Duty Cycle, $D = 0.75$

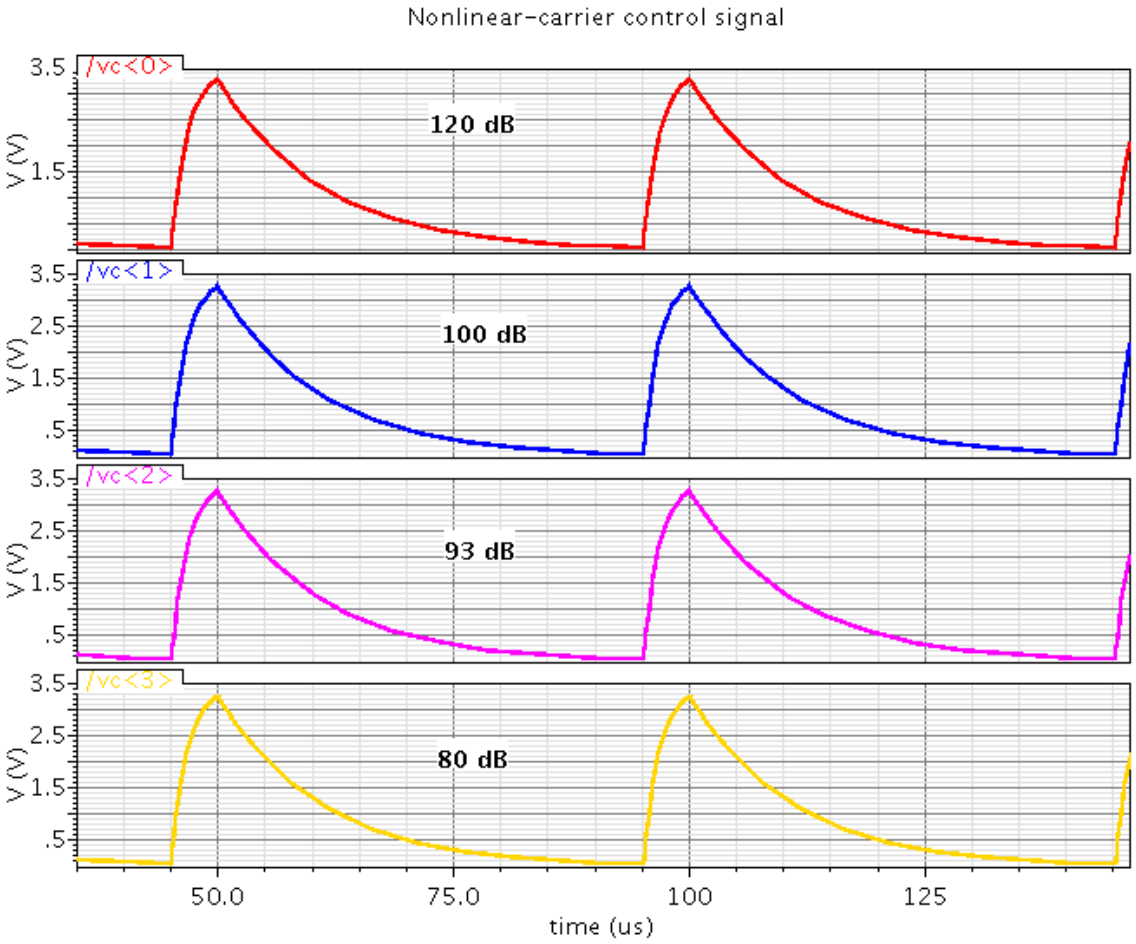

Figure 4.6: Nonlinear-carrier Control Signal Simulation Across Op-amp Open Loop Gain

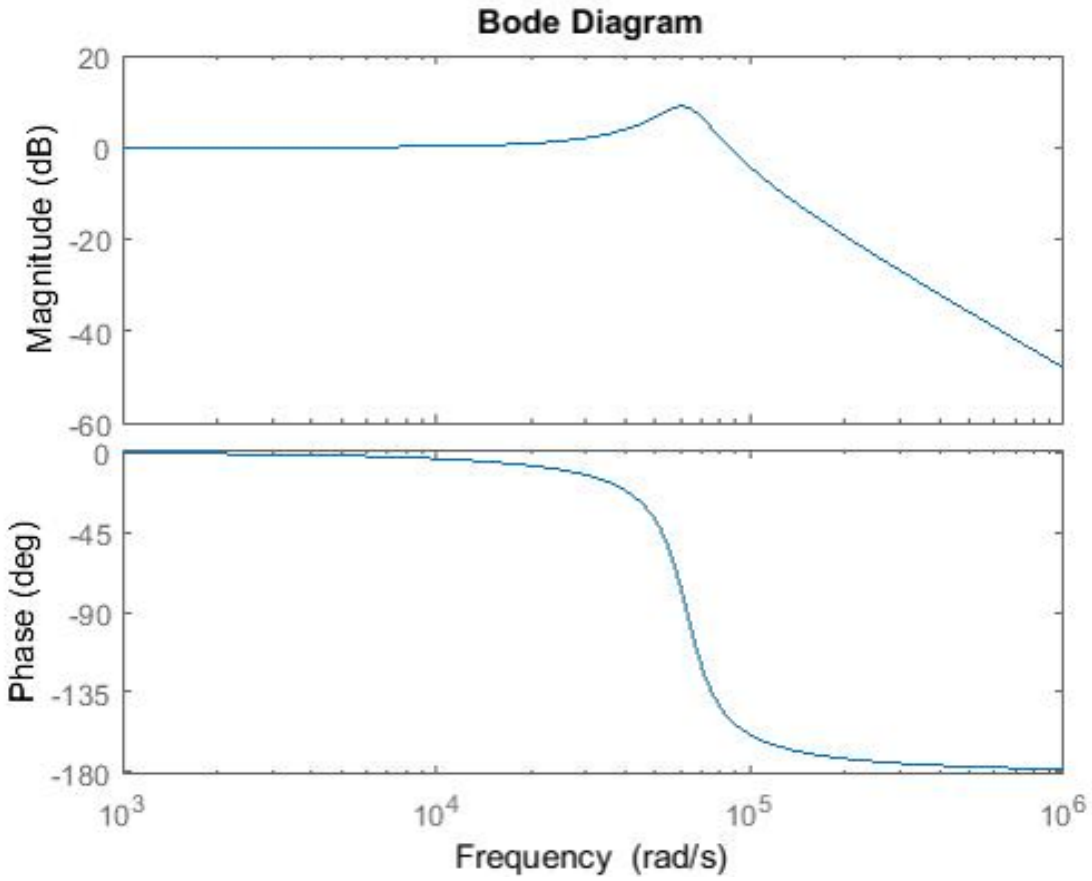

Figure 4.7: Bode Plot of Current Transfer Function with NLC Control Signal when Op-amp Open Loop Gain is 120 dB. Phase Margin is 30°

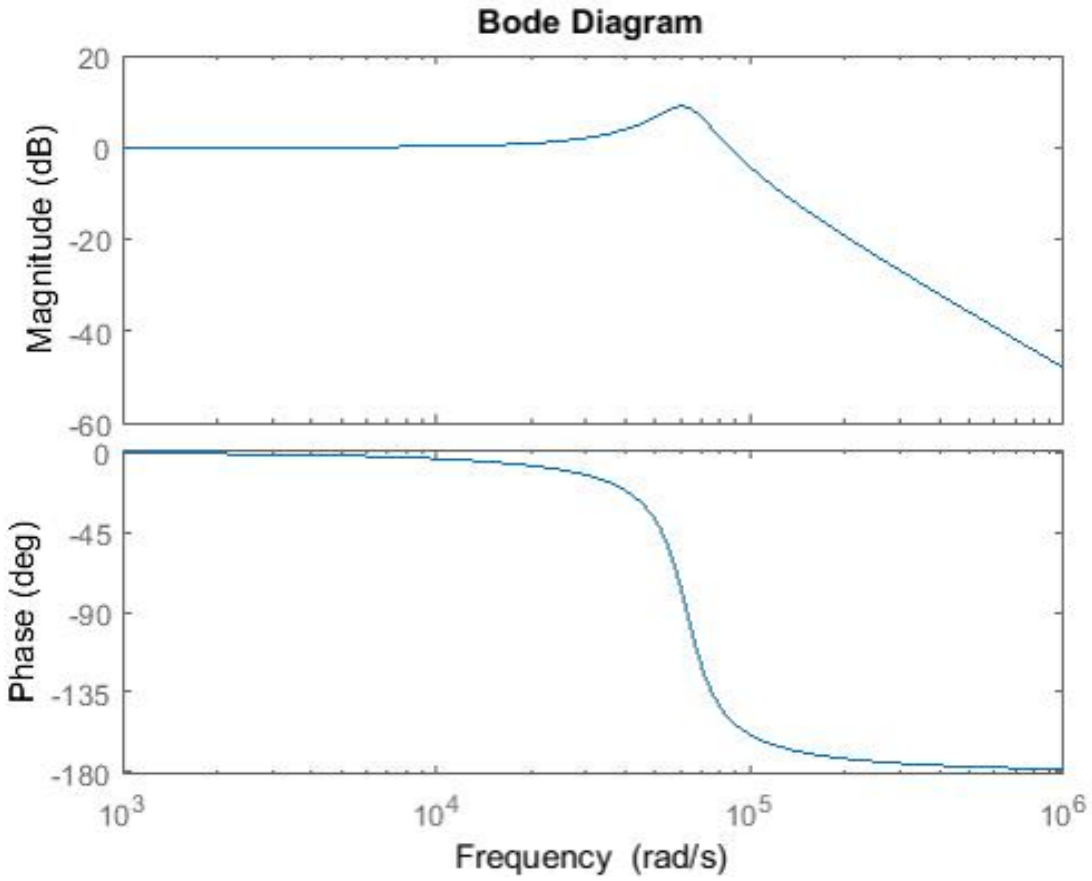

Figure 4.8: Bode Plot of Current Transfer Function with NLC Control Signal when Op-amp Open Loop Gain is 100 dB. Phase Margin is 30°

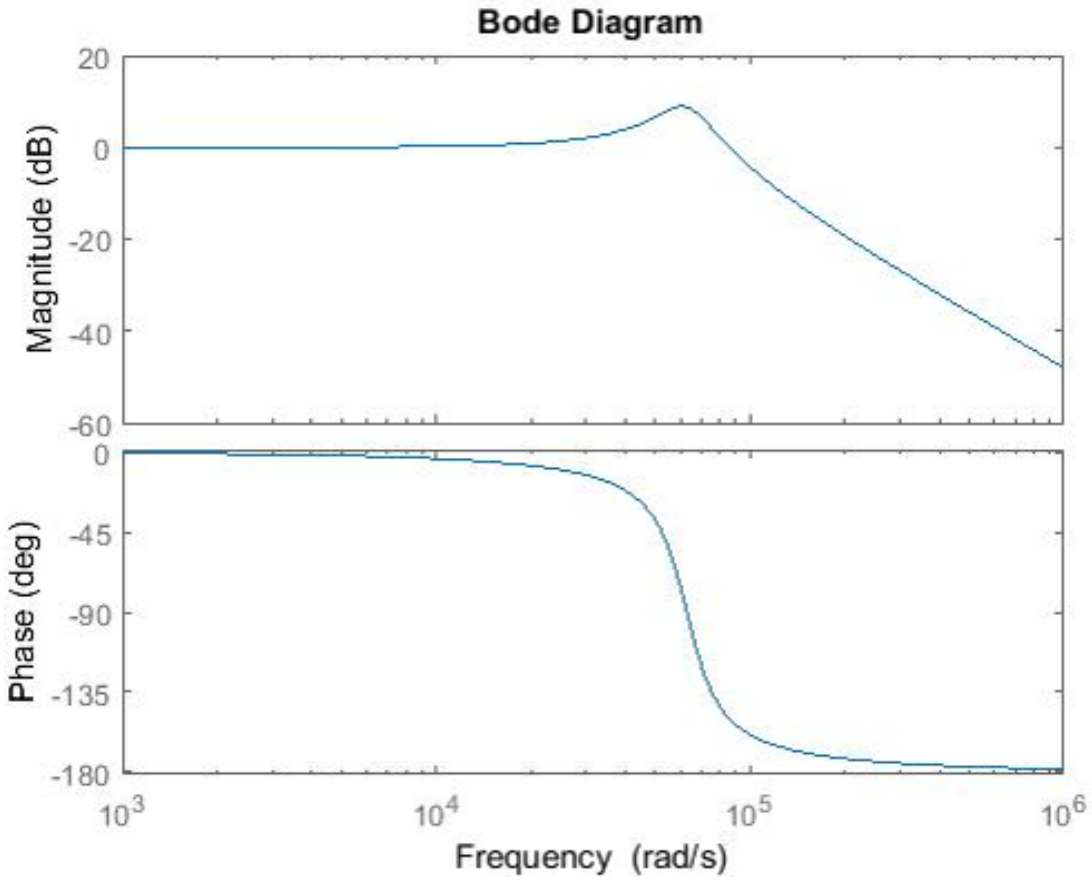

Figure 4.9: Bode Plot of Current Transfer Function with NLC Control Signal when Op-amp Open Loop Gain is 93 dB. Phase Margin is 30°

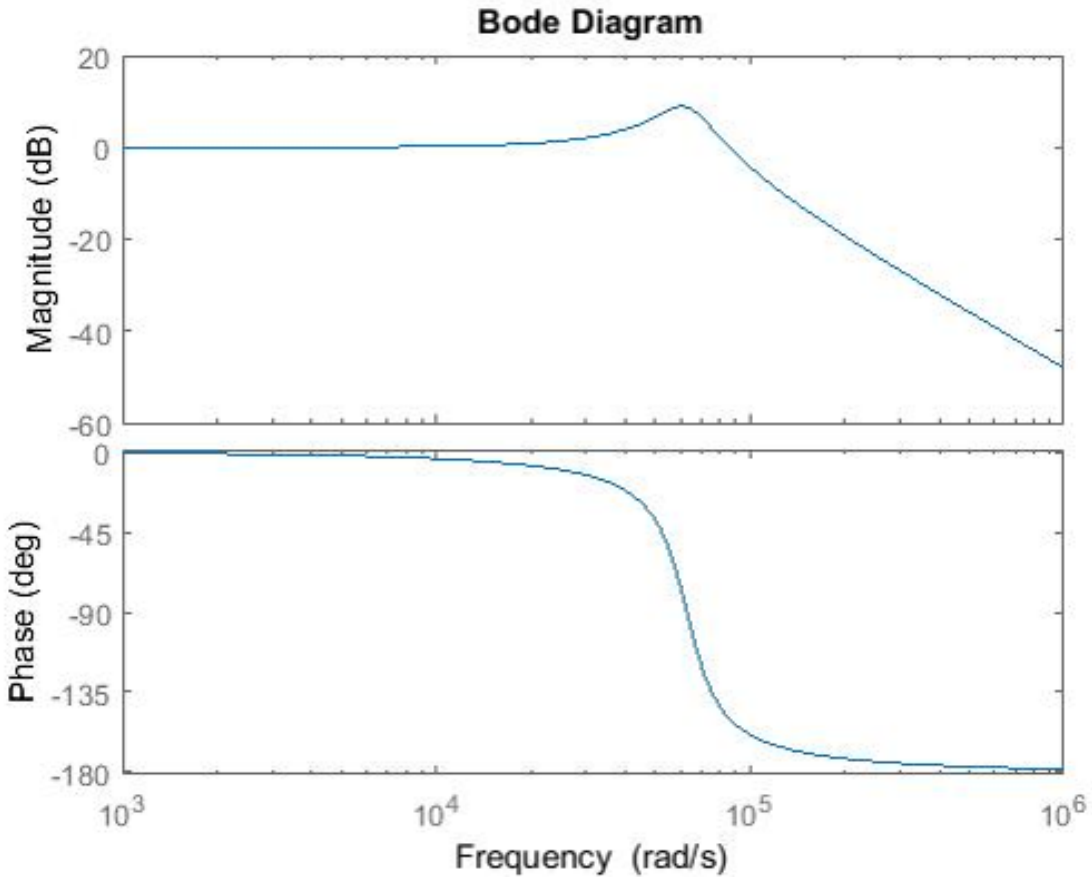

Figure 4.10: Bode Plot of Current Transfer Function with NLC Control Signal when Op-amp Open Loop Gain is 80 dB. Phase Margin is 30°

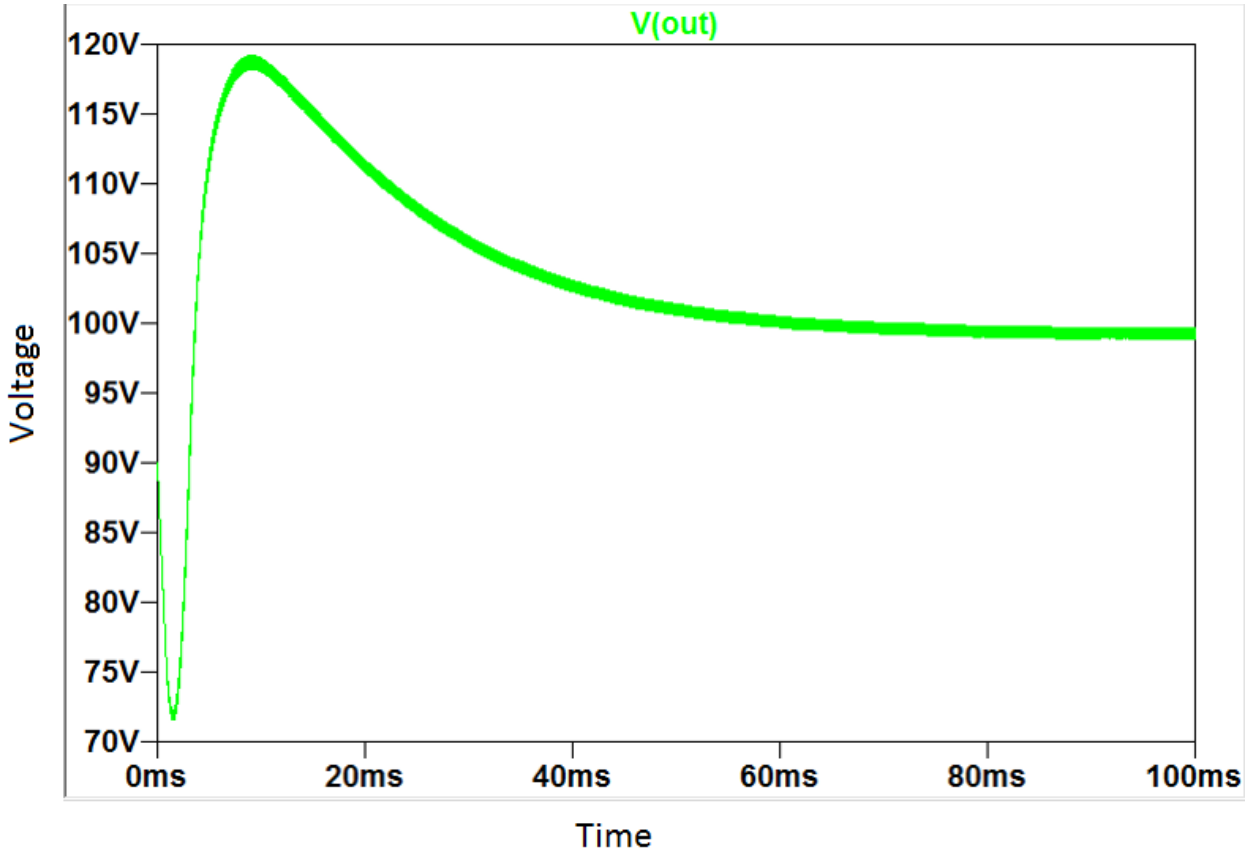

Figure 4.11: Transient Startup Simulation of Boost Converter with NLC Controller where Op-amp Open Loop Gain is 120 dB

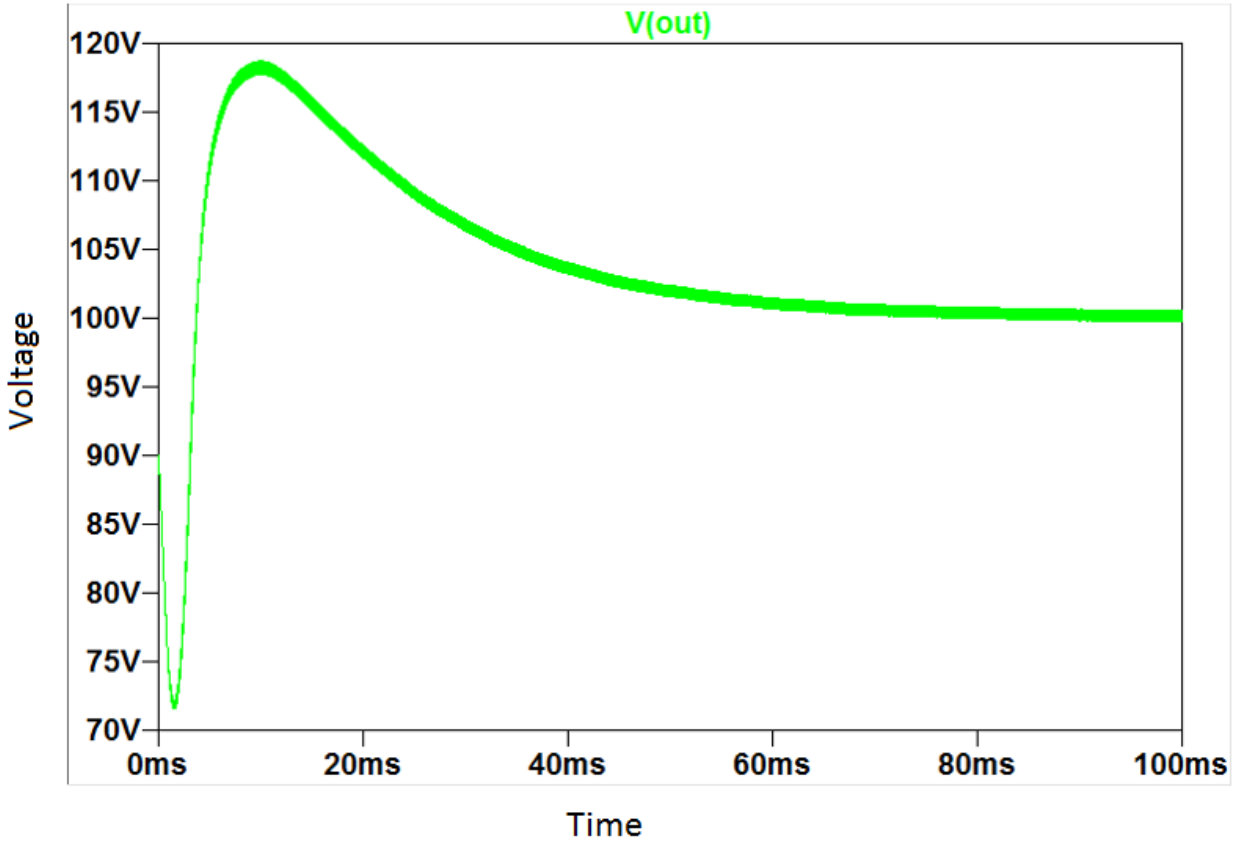

Figure 4.12: Transient Startup Simulation of Boost Converter with NLC Controller where Op-amp Open Loop Gain is 80 dB

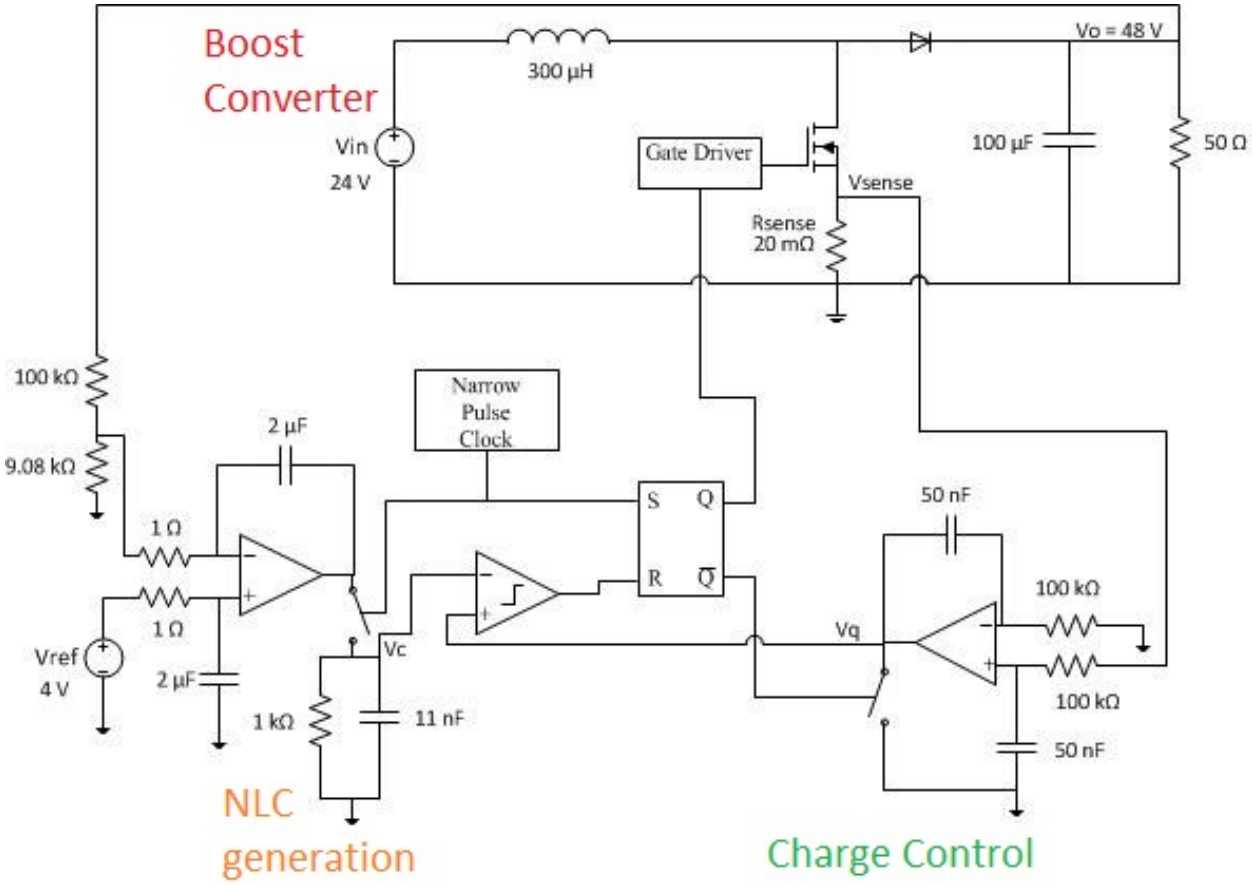

Figure 4.13: NASA Boost Converter with NLC Charge Control

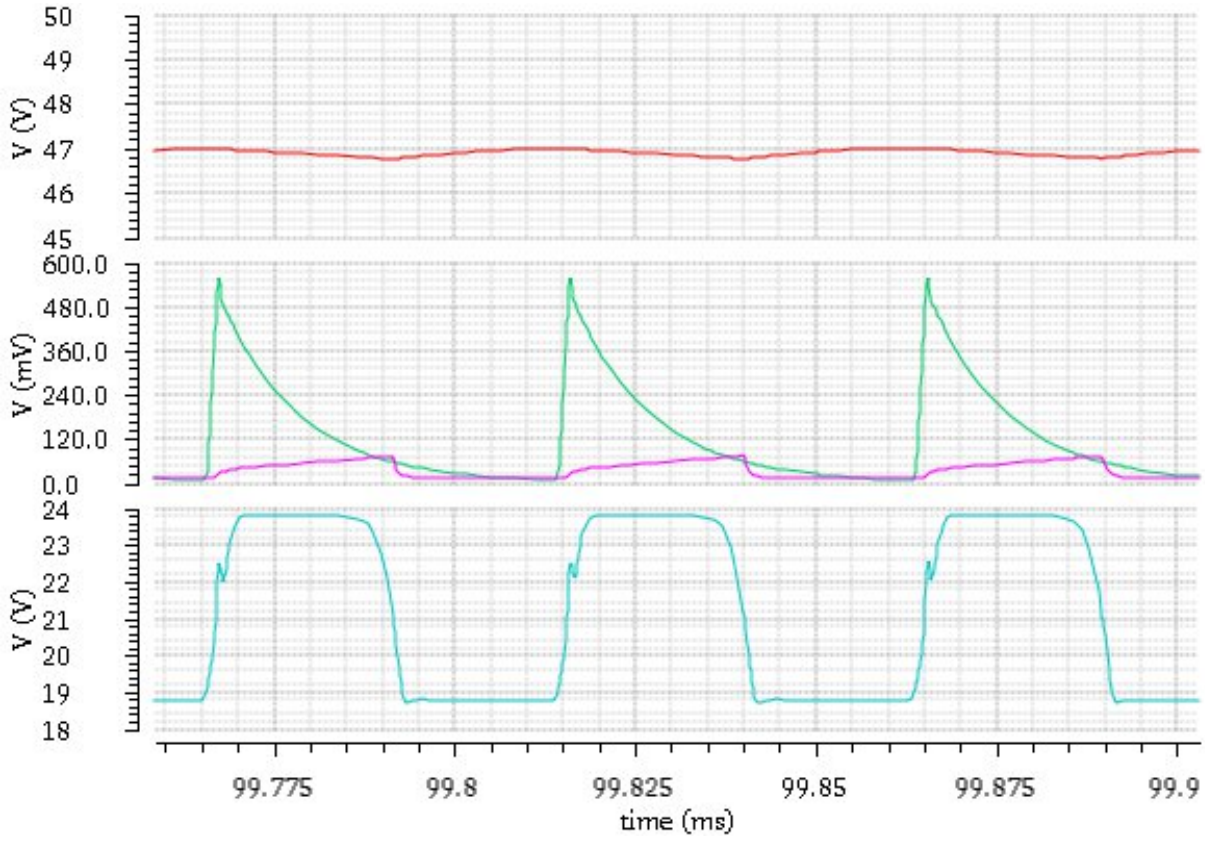

Figure 4.14: Boost Converter and NLC controller steady state waveforms from top to bottom: V_{out}, v_q and v_c, and Q

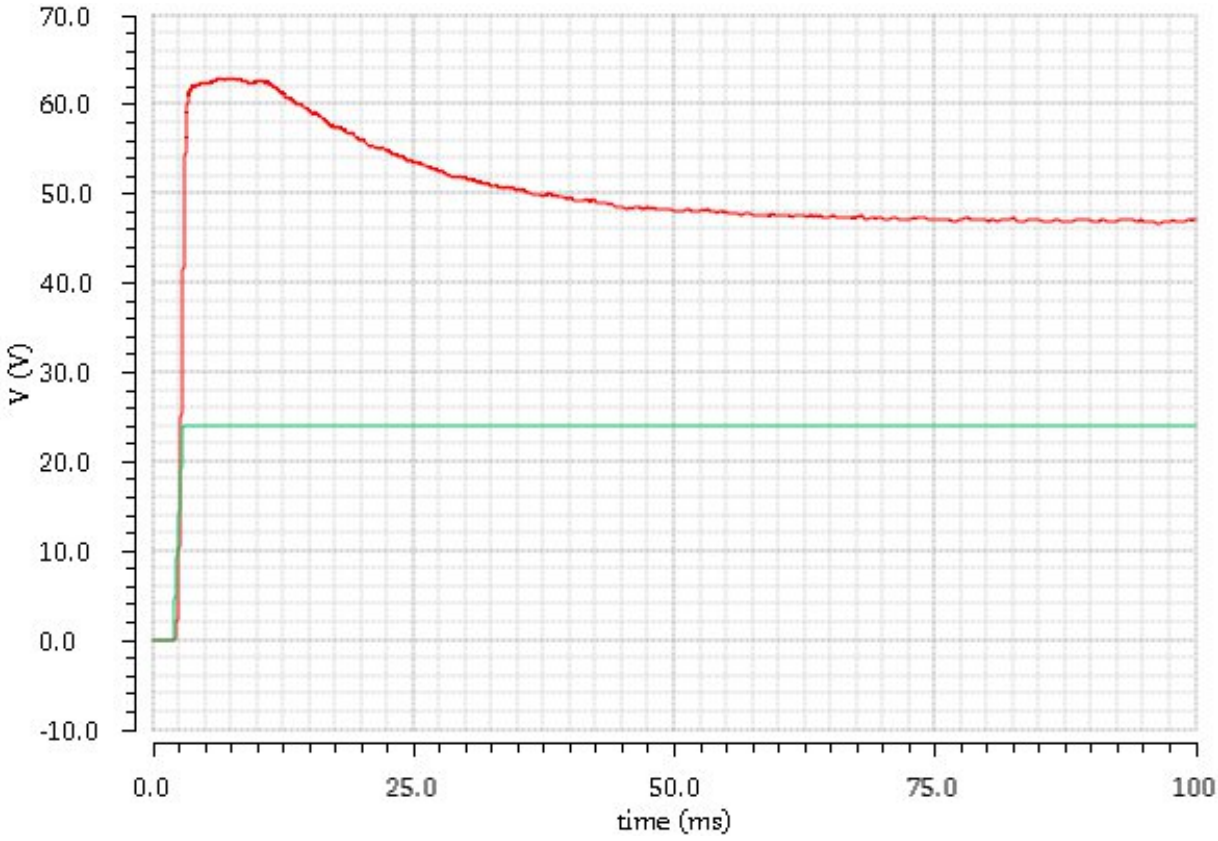

Figure 4.15: Boost Converter V_{out} Step Response

Chapter 5

Conclusion

This work presents the justification for using SiC IC processes to create integrated PWM controllers, it details the problems with conventional linear-carrier control, and it proposes nonlinear-carrier control as a solution. A model for NLC is presented, and mathematical and circuit level simulations are used to compare LC to NLC as justification of the technique. Finally, simulation results from a SiC boost converter with a SiC integrated NLC controller are presented. This work was published at APEC 2016 [citation needed].

Demonstration of an integrated SiC IC PWM controller, even in simulation, is an original contribution. Additionally, demonstration of NLC control for a DC-DC converter, the model describing NLC, and the direct comparison of NLC and LC models are original contributions.

If GE's IC fabrication had been successful, this work would have been supported with hardware test results. The greatest potential for future work would be verifying this technique on the bench with functional SiC ICs. Additional future work could be applying this circuit design technique to other low performance analog applications like silicon-based electronics exposed to high temperature and ionizing radiation.

Bibliography

[1] Barlow, M., Ahmed, S., Mantooth, H. A., and Francis, A. M. (2016). An integrated sic cmos gate driver. In *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 1646–1649. 5

[2] Carr, G. A., Iannello, C. J., Chen, Y., Hunter, D. J., Castillo, L. D., Bradley, A. T., Stell, C., and Mojarradi, M. M. (2013). Extreme environment capable, modular and scalable power processing unit for solar electric propulsion. In *2013 IEEE Aerospace Conference*, pages 1–9. 3

[3] Casady, J. and Johnson, R. (1996). Status of silicon carbide (sic) as a wide-bandgap semiconductor for high-temperature applications: A review. *Solid-State Electronics*, 39(10):1409 – 1422. 4

[4] Clark, D. T., Ramsay, E. P., Murphy, A., Smith, D. A., Thompson, R. F., Young, R., Cormack, J. D., Zhu, C., Finney, S., and Fletcher, J. (2011). High temperature silicon carbide cmos integrated circuits. In *Silicon Carbide and Related Materials 2010*, volume 679 of *Materials Science Forum*, pages 726–729. Trans Tech Publications. 5

[5] Durrani, Y., Aeloiza, E., Palma, L., and Enjeti, P. (2005). An integrated silicon carbide (sic) based single phase rectifier with power factor correction. In *2005 IEEE 36th Power Electronics Specialists Conference*, pages 2810–2816. 6

[6] Erickson, R. and Maksimovic, D. (2001). *Fundamentals of Power Electronics*. Springer Science+Business Media, LLC, New York, New York. 1, 8, 10, 23

[7] Funaki, T., Balda, J. C., Junghans, J., Kashyap, A. S., Mantooth, H. A., Barlow, F., Kimoto, T., and Hikihara, T. (2007). Power conversion with sic devices at extremely high ambient temperatures. *IEEE Transactions on Power Electronics*, 22(4):1321–1329. 6

[8] Kashyap, A. S., Chen, C. P., Ghandi, R., Patil, A., Andarawis, E., Yin, L., Shaddock, D., Sandvik, P., Fang, K., Shen, Z., and Johnson, W. (2013). Silicon carbide integrated circuits for extreme environments. In *The 1st IEEE Workshop on Wide Bandgap Power Devices and Applications*, pages 60–63. 4, 5

[9] Lelis, A., Green, R., and Habersat, D. (2011). (invited) effect of threshold-voltage instability on sic power mosfet high-temperature reliability. *ECS Transactions*, 41(8):203–214. 5

[10] Maksimovic, D., Jang, Y., and Erickson, R. W. (1996). Nonlinear-carrier control for high-power-factor boost rectifiers. *IEEE Transactions on Power Electronics*, 11(4):578–584. 7

[11] Rahman, A., Shepherd, P. D., Bhuyan, S. A., Ahmed, S., Akula, S. K., Caley, L., Mantooth, H. A., Di, J., Francis, A. M., and Holmes, J. A. (2015). A family of cmos analog and mixed signal circuits in sic for high temperature electronics. In *2015 IEEE Aerospace Conference*, pages 1–10. 5

[12] Ramsay, E., Clark, D., Cormack, J., Murphy, A., Smith, D., Thompson, R., Young, R., and Finney, S. (2012). Digital and analogue integrated circuits in silicon carbide for high temperature operation. *Additional Conferences (Device Packaging, HiTEC, HiTEN, & CICMT)*, 2012(HITEC):000373–000377. 5

[13] Tan, F. D. and Middlebrook, R. D. (1995). A unified model for current-programmed converters. *IEEE Transactions on Power Electronics*, 10(4):397–408. 9

[14] Vert, A., Chen, C.-P., Patil, A., Saia, R., Andarawis, E., Kashyap, A., Zhang, T., Shaddock, D., Shen, Z., Johnson, R. W., and Normann, R. (2012). Silicon carbide high temperature operational amplifier. *Additional Conferences (Device Packaging, HiTEC, HiTEN, & CICMT)*, 2012(HITEC):000378–000383. 5

[15] Wang, R., Boroyevich, D., Ning, P., Wang, Z., Wang, F., Mattavelli, P., Ngo, K. D. T., and Rajashekara, K. (2013). A high-temperature sic three-phase ac - dc converter design for greater than 100/spl deg/c ambient temperature. *IEEE Transactions on Power Electronics*, 28(1):555–572. 5, 6

[16] Wang, Z., Shi, X., Tolbert, L. M., Wang, F. ., Liang, Z., Costinett, D., and Blalock, B. J. (2015a). A high temperature silicon carbide mosfet power module with integrated silicon-on-insulator-based gate drive. *IEEE Transactions on Power Electronics*, 30(3):1432–1445. 6

[17] Wang, Z., Shi, X., Tolbert, L. M., Wang, F. F., Liang, Z., Costinett, D. J., and Blalock, B. J. (2015b). Development of a board-level integrated silicon carbide mosfet power module for high temperature application. In *2015 IEEE International Workshop on Integrated Power Packaging (IWIPP)*, pages 123–126. 6

[18] Zane, R. and Maksimovic, D. (1996). Nonlinear-carrier control for high-power-factor rectifiers based on flyback, cuk or sepic converters. In *Applied Power Electronics Conference and Exposition, 1996. APEC '96. Conference Proceedings 1996., Eleventh Annual*, volume 2, pages 814–820 vol.2. 7

[19] Zane, R. and Maksimovic, D. (1998). Nonlinear-carrier control for high-power-factor rectifiers based on up-down switching converters. *IEEE Transactions on Power Electronics*, 13(2):213–221. 7

[20] Zhong, X., Wu, X., Zhou, W., and Sheng, K. (2014). An all-sic high-frequency boost dc dc converter operating at 320 degree c junction temperature. *IEEE Transactions on Power Electronics*, 29(10):5091–5096. 6

Appendices

Appendix A

SiC Integrated Circuit Schematics

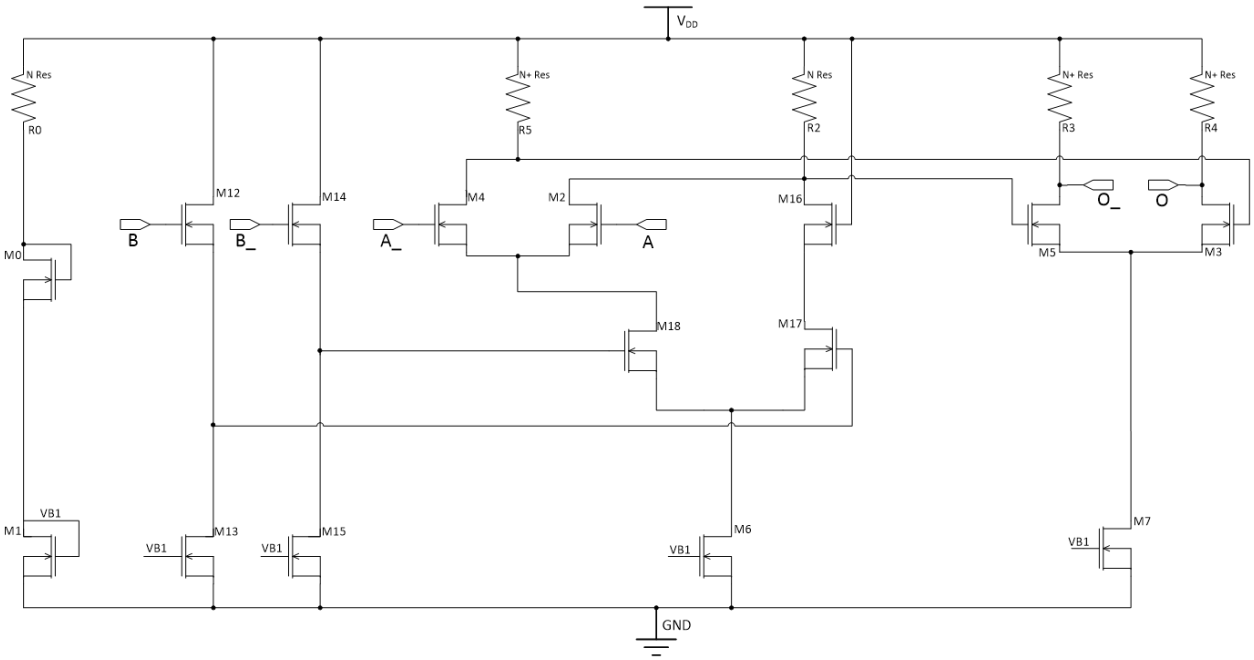

Figure A.1: SiC Current Mode Logic NOR Gate

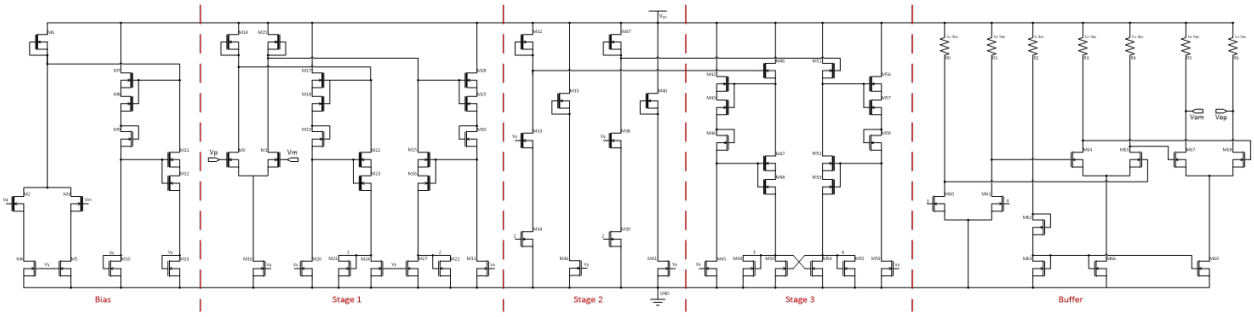

Figure A.2: SiC Comparator with Op-Amp Input and CML Logic Output

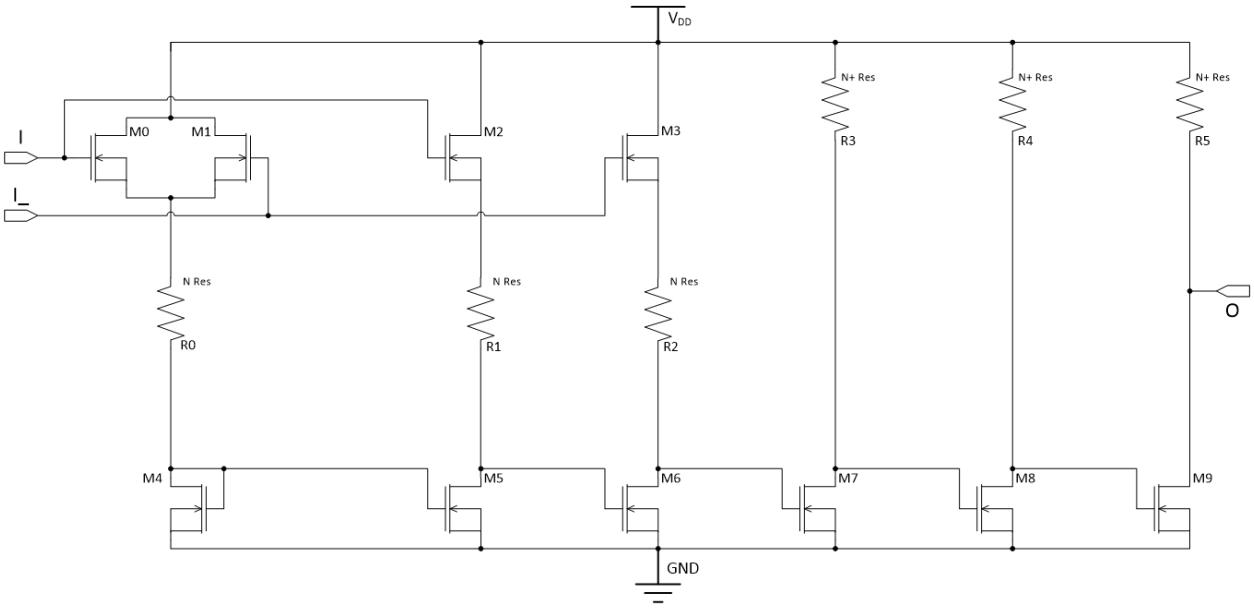

Figure A.3: SiC Switch Driver to drive large gate capactiance of SiC NMOS Switch

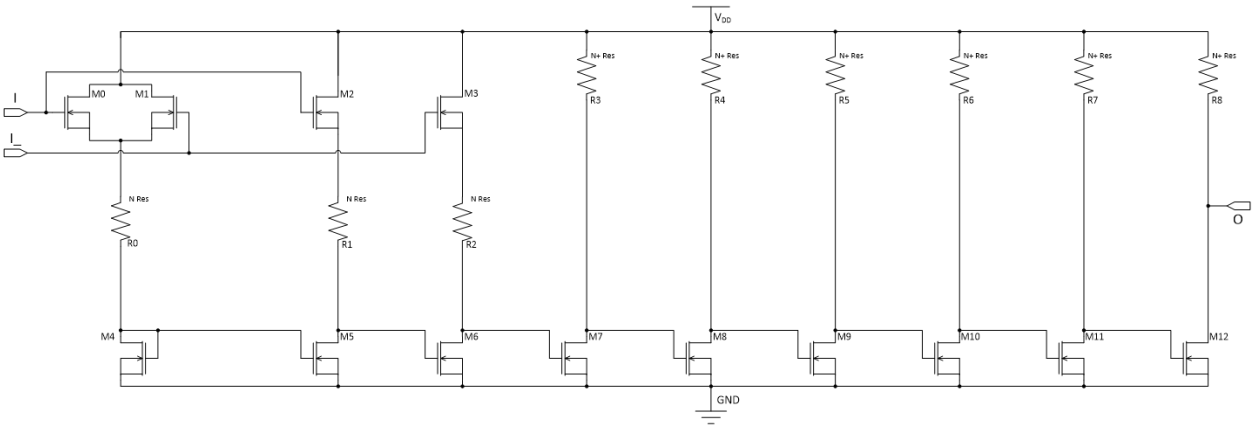

Figure A.4: Simple SiC Gate Driver to drive SMPS Power Switch

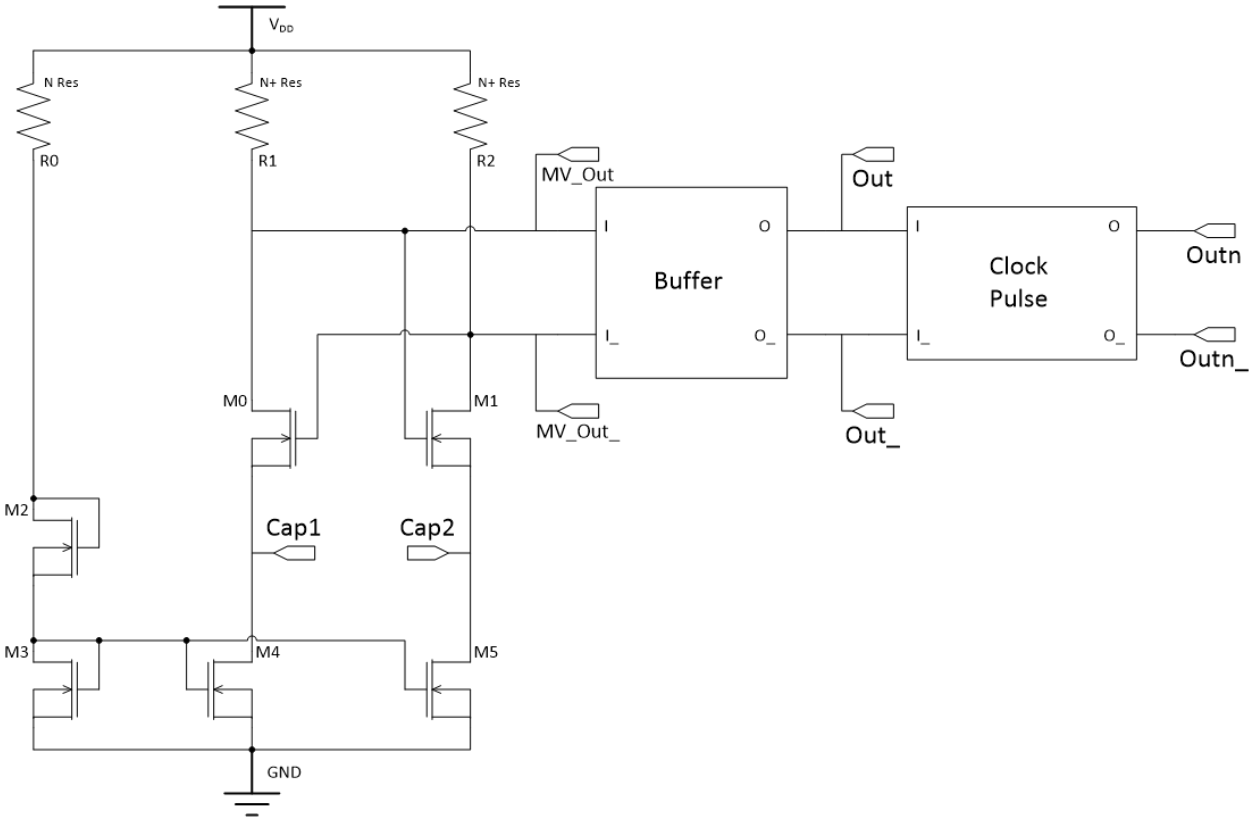

Figure A.5: SiC Multivibrator to be used as low frequency clock

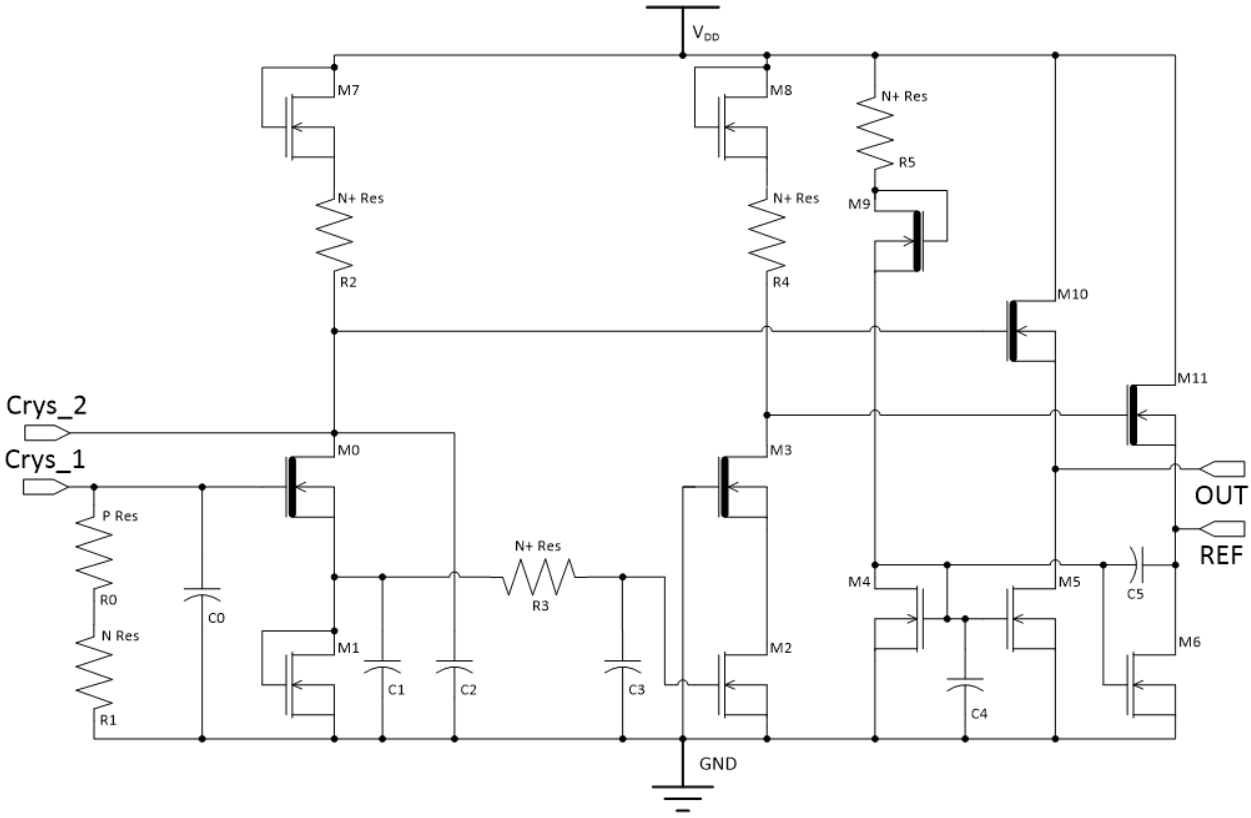

Figure A.6: SiC Crystal Oscillator to be used as high frequency clock

Vita

Richard Kyle Harris was born in Henderson, Tennessee, and attended Union University where he received a Bachelors of Science in Engineering degree in 2011.

After graduating from Union University, he started graduate school at the University of Tennessee studying in the Integrated Circuits and Systems Laboratory. His research interests are analog and mixed signal integrated circuit design, integrated power electronics, and very low power integrated circuit design.