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A 64-Channel Mixed-Signal Data Acquisition System for a Solid-State High Efficiency Neutron Detector Array

Anthony Gene Antonacci
University of Tennessee - Knoxville

To the Graduate Council:

I am submitting herewith a thesis written by Anthony Gene Antonacci entitled "A 64-Channel Mixed-Signal Data Acquisition System for a Solid-State High Efficiency Neutron Detector Array." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Benjamin J. Blalock, Major Professor

We have read this thesis and recommend its acceptance:

Charles L. Britton, Jr., M. Nance Ericson

Accepted for the Council:
Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

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A 64-Channel Mixed-Signal Data Acquisition System for a Solid-State High Efficiency Neutron Detector Array

A Thesis Presented for the

Master of Science Degree

The University of Tennessee, Knoxville

Anthony Gene Antonacci

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ABSTRACT

This thesis presents the design of multiple analog and digital blocks required to implement a desired solid-state data acquisition system for the High Efficiency Neutron Detector Array (HENDA) project under the Spallation Neutron Source (SNS) at Oak Ridge National Laboratory (ORNL). This system encloses and is an extension of prior work described in [1] and [2]. The first prototype chip, named *Patara*, contained a charge sensitive front-end amplifier [2], and a semi-Gaussian shaper with baseline restore circuitry [1]. *Patara III*, described in this thesis, involved the addition of the following system components; two comparators, a selectable synchronous/asynchronous digital backend, priority and binary encoders, nine LVDS drivers/receivers, three 8-bit current driven calibration DAC's, two BGR's, and a 99-bit serial shift register with channel test-mode circuitry. The design approach for all major blocks will be discussed along with overall system simulations. In addition, the testing procedure and associated measured results will be summarized illustrating a successful system design. This ASIC was fabricated using the Taiwan Semiconductor Manufacturing Company (TSMC) 0.35-µm process available through MOSIS.

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CHAPTER 1

INTRODUCTION AND OVERVIEW

1.1 Introduction

The continuous and systematic increase in transistor density and performance, guided by CMOS scaling theory and described in "Moore's Law" [3], has lead to the capability of high density and high functionality application specific integrated circuits (ASICs). The world today is revolutionized by this increasing effort in many sectors, consequently yielding higher functionality products in a more compact trend.

In the sector of radiation detector systems, the need for high resolution channel counts can be achieved on a single microchip. In addition, a system on chip (SoC) can yield a much smaller footprint than the alternative printed circuit board (PCB) system. This can result in a high density product capable of very large channel counts and high functionality. These sorts of product results are particularly beneficial in the science of neutron imaging where large channel counts are a necessity for highly pixilated imaging and high overall system efficiencies.

This work is an expansion of the foundational work reported in [1] and [2]. From a systems perspective, their work consisted of the analog front-end electronics needed in this design. The contributed work in this thesis implements the bridge between the analog and digital domains, resulting in the capability of a fully integrated, 64-channel data acquisition system for neutron imaging.

1.2 Motivation

The world today sees the advancement of technology as an inevitable fate. What lies beyond this veil are the scientists and engineers who habitually seek greater capability and a place for innovative ideas to be expressed. This project is part of a collaboration who seeks these same principles in the field of radiation detection systems, or more specifically neutron detection systems. Although this is not a consumer-recognized sector, advancements in this field can have an impact on applications for homeland security, treaty verification, personnel neutron dosimetry, and neutron counting and survey instrumentation [4].

The Spallation Neutron Source (SNS) at the Oak Ridge National Laboratory (ORNL) in Oak Ridge, Tennessee, is the world's most intense pulsed accelerator-based neutron source [6]. This capability has opened an avenue of innovative research and development, and a need for increased capability in the specific field of neutron imaging. This neutron source will require many supporting data acquisition instruments that utilize position sensitive neutron detectors [4]. In particular, the SNS will require a data acquisition system capable of operating a detector array with high spatial resolutions (pixel widths) of 100 μm to 500 μm, and obtain a response time of less than 10 μsec—a system with these specifications is not presently commercially available [4].

These high spatial resolutions result in a vast array of neutron detectors, and consequently dictate the need for a high channel count system with a small footprint. With the ability of current ASIC technology, this is readily achieved. This work utilizes

the benefits of integrating such a highly complex system and readily pushes the state-of-the-art for neutron imaging to new levels.

1.3 Overview

As a result of the need for greater capability in the science of neutron imaging, the High Efficiency Neutron Detector Array (HENDA) project was introduced and funded by the National Science Foundation (NSF) Grant Number 0412208. This project has been underway since 2004 and is centralized around a cutting-edge, silicon-based, linear thermal neutron detector.

1.3.1 Silicon-based linear thermal neutron detector

The solid-state neutron detector uses a novel approach which has been shown to yield a 50% thermal neutron detection efficiency [4]—much higher than the 13% efficiencies shown a half decade ago. Based on the alpha-n reaction

$$n + {}^{6}L \rightarrow {}^{4}He + {}^{3}H + 4.79\,MeV, \qquad \textbf{(1)}$$

the detector releases an alpha particle with an energy level of 4.79 MeV [5]. Utilizing an array of millions of microscopic holes etched directly into the silicon, the ^{6}LiF coating migrates to a depth of 170 μm and shows an increase in efficiency over non-etched surfaces [5]. This coating over a solid-state semiconductor detector shows a response time ranging from tens of nanoseconds down to hundreds of picoseconds leaving only the readout electronics, rather than the detector, to be the timing limitations for the neutron detection system [4]. This range of response times are superior to gas-based neutron

detectors due to low charge-carrier mobility in the detector gas, thereby making the gas-based detector the limiting factor rather than the electronics [4].

Due to the neutron reactive coating on the detector, an ionic reaction will occur under the presence of neutrons releasing an alpha particle. When this event occurs over a semiconductor, in this case silicon, the alpha particle hits the silicon lattice creating a charge proportional to the energy required to induce an electron-hole pair (or exciton). This charge can then be converted to a voltage potential and discriminated verses a DC threshold voltage to determine electronically that the event occurred.

1.3.2 16-channel analog front-end (Patara)

Prior to any discrimination, the collected charge must undergo analog signal processing (ASP) so that modern digital techniques can be utilized. Therefore, the front end of such a system must be analog and charge-sensitive. In addition, analog filtering and a DC baseline restore must be implemented to present a highly detectable signal at a known DC voltage level.

In 2006, an analog low-noise charge-sensitive readout channel for the coated neutron detector was developed [1][2]. This solid-state analog readout system, named *Patara*, consisted of 16 readout channels. Each channel is comprised of a charge-sensitive preamplifier with tracking pole-zero cancellation and digitally-adjustable leakage current compensation. The pole-zero section is followed by a voltage-amplifier based real pole, which serves as the first pole of the shaper section. The shaper has a five-pole, complex-conjugate semi-Gaussian shape with gated baseline restorer [5].

1.3.3 64-channel data acquisition system (Patara III)

After the successful development of *Patara*, the next step was to bridge the analog front-end and the needed digital circuitry so that this system is compliant with the SNS standard—this new microchip would then be called *Patara III*. The previously developed analog readout channel presents a semi-Gaussian response at a given DC voltage level allowing for an ideally detectable signal. Without the need for any amplitude information from the signal, a neutron occurrence is detected readily with a comparator (or discriminator) circuit—at this point, the event is now considered to have undergone a 1-bit flash analog-to-digital conversion.

With the neutron occurrence now digital, registering of the event on a rising-edge is needed until the SNS system has received the event data. Using a handshake protocol, the SNS system will receive a data flag when data is present, and send a reset command back to the data acquisition chip so that all registers are cleared. This can be performed synchronously or asynchronously with the SNS system. In this case, both protocols were implemented so that a system running without a clock on chip can be analyzed for noise concerns.

The time that has elapsed between data read and system reset is termed "dead-time." This term is derived from an error state that exists when an event occurs prior to properly resetting the system registers. When acquiring high throughput data, this can become problematic. The dead-time of this system was readily considered and optimized in this work as discussed in Chapter 3.

As described up to this point, the readout channel consists of a charge-sensitive front end, semi-Gaussian shaper with a DC baseline restore, a discriminator, system registers, and a synchronous/asynchronous handshake digital backend. The designed readout channel circuitry is then repeated 64 times to allow for data acquisition of 64 neutron detectors per chip. With each channel reading parallel detectors, priority encoding must be implemented under the event multiple channels are hit. Although this event is highly improbable, this state still needs to be handled electronically. In addition to priority encoding, binary encoding is implemented so that a 6-bit binary word is presented to the SNS system as to avoid 64-parallel data lines at the output.

Due to noise concerns, a low voltage differential signaling (LVDS) protocol is implemented using on-chip LVDS drivers/receivers for system inputs and outputs (I/O). In addition, three 8-bit DACs were designed so that the SNS system could calibrate the analog circuitry along with the neutron event discrimination level. To allow programming of the data acquisition system from the SNS system, a 99-bit serial shift register was implemented.

1.4 Thesis Organization

This thesis presents the design steps along with the testing results for a solid-state 64-channel data acquisition system used in the high efficiency neutron detector array (HENDA) project. The details of Chapter 2 covers the background of radiation detector systems, a block level overview of the previous work in [1] and [2], and a block level overview of the implemented data acquisition system performed in this work.

The details of Chapter 3 presents the design steps of all major blocks contributed in this work. Circuit analysis and device level designs are discussed along with simulation results.

The details of Chapter 4 presents the fabricated ASIC, and covers the block level of the testing and verification procedure of this system. Testing results will be shown and contrasted with the simulation results. The final chapter, Chapter 5, concludes on the work presented in this thesis and points out future work that will expand on this project.

CHAPTER 2

SYSTEM OVERVIEW AND PREVIOUS WORK

2.1 Fundamentals of Radiation Detection Systems

Radiation detection systems have had a large impact in many sectors of science and medicine. Such areas include Positron Emission Tomography (PET), Single Photon Emission Computed Tomography (SPECT), Magnetic Resonance Imaging (MRI), along with many others. The developments of such systems are relatively similar in concept (see Figure 2.1 below)—this work is fairly correlated to these similarities. All require a detector dedicated to conveying an annihilation event into an electronically decipherable signal, along with readout electronics. When this detector is implemented in the solid-state, it is electrically modeled as a reverse biased diode, and can be DC coupled or AC coupled with the front end of the readout electronics.

The front-end electronics of a typical readout channel consist of a charge sensitive

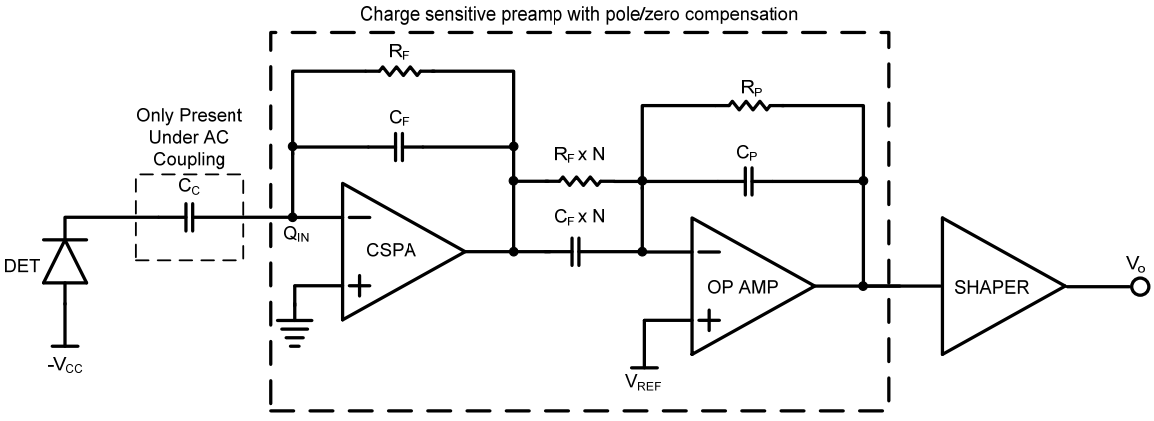


Figure 2.1 – Typical Radiation System Front End

preamplifier (CSPA) that converts the collected charge into a voltage. Generally, a pole/zero compensation technique is used in the design of the CSPA. This technique is used to avoid pulse pile up that can occur due to the large time constant, $\tau_F = 1/(R_F C_F)$, created by R_F and C_F in the feedback path, where generally $\tau_F >> T_{event\text{-}rate}$ [2]. If designed properly, the resulting frequency response of the CSPA will approximate a single-pole system determined by R_P and C_P. The output voltage from the CSPA is then amplified and suitably shaped by the shaper circuit for the measurement of the signal properties (generally peak value). An example of the detector signal propagation through the front-end electronics is shown below in Figure 2.2. The first stage of the detection system consisting of the detector and CSPA is the most important [7]. This stage should extract the charge from the detector with as little additive noise as possible.

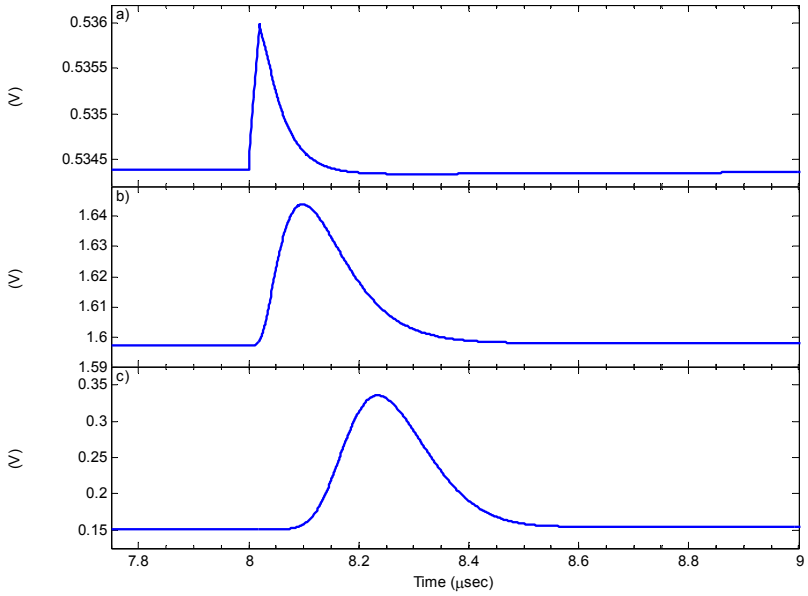


Figure 2.2 – a) Example of a detector output, b) The CSPA output after the first real pole with the given detector output, c) The shaper output with the given CSPA output

The resolution of the CSPA is designed to be limited by the input transistor, and is measured in terms of equivalent noise charge (ENC). The ENC corresponds to the charge that must be delivered to the front-end in order to achieve an output signal-to-noise ratio equal to unity [8]. In addition to the induced noise by the CSPA, proceeding electronics can consequently affect the ENC. In this work, the addition of digital circuitry and a system clock can greatly affect the ENC of the system if proper design techniques are not utilized.

One can make the argument that the CSPA can sufficiently make up the front end of a radiation detection system since it does provide the necessary amplitude information with a single pole response. However, a CSPA does present some non-ideal attributes to the detected signal. The major non-idealities are ballistic deficit, and baseline shift (see [9] for more detail regarding these two non-idealities). In a capacitively-coupled system any baseline shift will not present a problem since the DC offset will not be passed through the signal processing chain. Consequently, if a capacitively-coupled system is used, one could not implement any DC threshold levels with which to determine if an event occurs—this dramatically complicates the system requirements. Therefore, it is desirable to pass the output of the CSPA through a shaping filter that accommodates high pulse rates, retains amplitude information, and has low additive noise.

2.2 Previous Work

To adequately implement a radiation-detection ASIC dedicated to neutron imaging for the SNS, the front-end electronics are to have a charge sensitive preamplifier

capable of acquiring the signal from the solid-state sensor with as little noise as possible. In addition the pulse-pair resolution is to be 10 μsec; therefore a shaper with a response time less than 10 μsec is needed. It is also desired to have the noise of the overall system be dominated by the CSPA; therefore the shaper is to only contribute 10% of the noise power spectral density (NPSD) of the CSPA.

The above specifications for the analog front end was achieved by the *Patara* microchip [1][2]. Since the work presented in this thesis utilizes the front-end design in *Patara*, the following two sections will overview the CSPA and Shaper circuitry developed to provide a better understanding of the final system. Further detail can be found in references [1] and [2].

2.2.1 Patara: Charge Sensitive Preamplifier [2]

Since the CSPA directly interfaced the neutron detector, the design of the CSPA was based on the neutron detector specifications. The details of these specifications are:

- Low noise ≤ 1000 electrons for detector capacitance of 5 pF,
- Positive or Negative charge input,
- Detector leakage current compensation,
- Active pole/zero compensation network,
- Preamplifier gain adjustment.

The circuit topology chosen for the preamplifier is an NMOS regulated cascode amplifier for the low 1/f noise (flicker noise) feature. Since the design of this topology relies heavily on the input MOSFET to dominate the noise of the system, the design process when optimizing noise performance was based on [8]. A schematic of the final preamplifier without feedback is illustrated in Figure 2.3

This design also implemented a gain adjustment control. It can support a full gain (minimum feedback capacitance) and a half gain (maximum feedback capacitance) by using a digital switching interface in the feedback path. At higher charge gains, the output may be saturated and can cause ballistic deficit along with an overall higher level of noise when referred to the output of the system. Therefore, having the ability to adjust the charge gain can act as a benchmark to the overall performance of the CSPA.

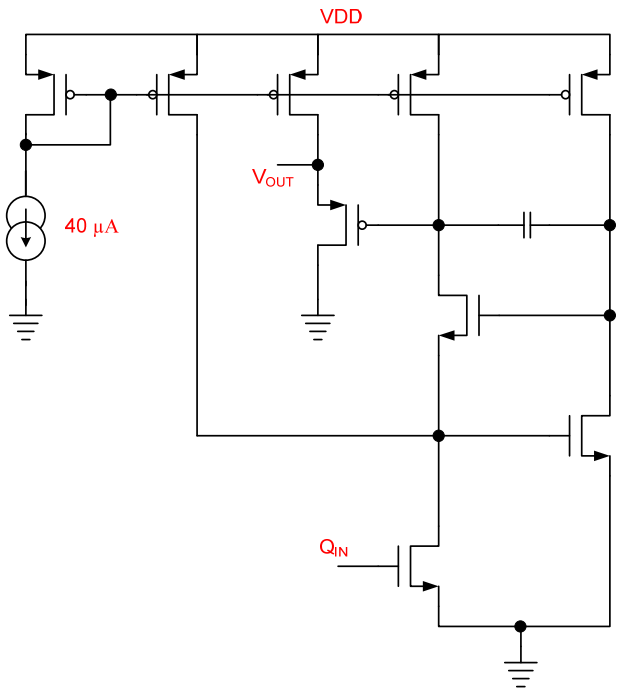


Figure 2.3 – CSPA topology without feedback [2]

The feedback network for the designed CSPA consists of a charge collecting capacitor and a resistive impedance to allow charge to bleed off of the feedback capacitor. One solution for the charge bleed off would be to apply a passive resistor in parallel with the feedback capacitor. Consequently a resistor adds thermal noise at the input MOSFET ultimately affecting the ENC. In order to reduce the noise contribution, the resistance value would have to be large (since this is a charge sensitive front end) which is not practical in terms of chip area. Therefore an active resistive element allows for a smaller footprint and is able to achieve very large impedances. Figure 2.4 illustrates the active resistor used in the feedback network.

In order to achieve a large effective resistance in the active feedback path, the

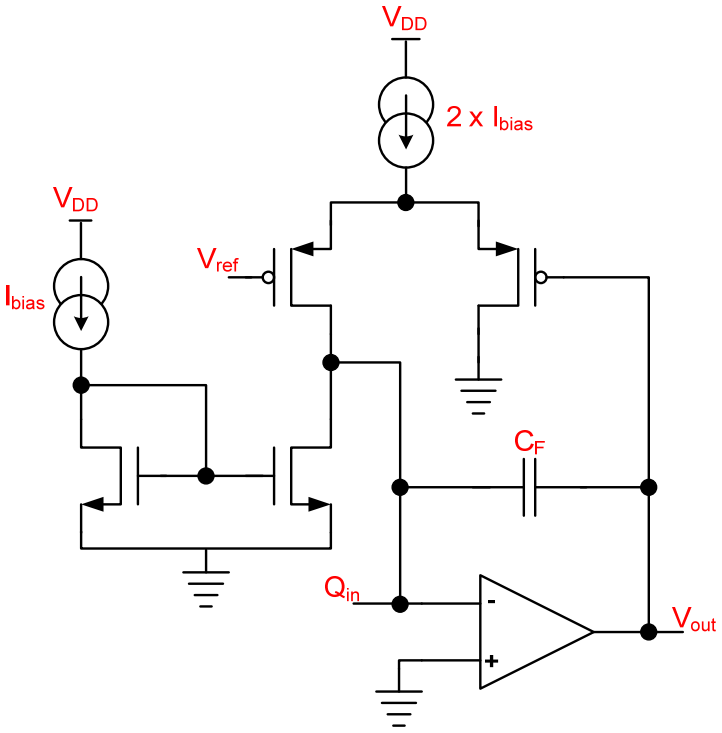


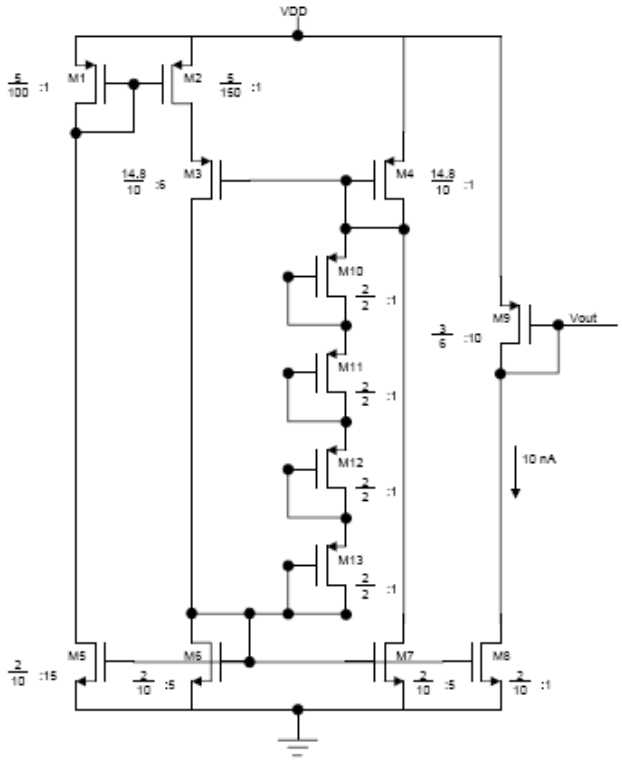
Figure 2.4 – Active feedback network [2]

active devices are to operate deeply in the linear region. This was implemented by biasing the feedback network with an on-chip nanoampere current source. In addition to this on-chip current source, a 4-bit digital-to-analog converter (DAC) was used to scale the bias current in order to change the effective resistance. This ultimately leads to compensation of the detector leakage current. Figure 2.5 shows the current source and DAC.

2.2.2 Patara: Semi-Gaussian Shaper and Base-line Restore [1]

The shaper implemented in *Patara* has a unipolar 4-pole complex conjugate semi-Gaussian response. A unipolar response was implemented versus the bipolar counterpart due to a superior signal-to-noise ratio (SNR), and due to the fact that the shaper can be set to maximize dynamic range. A semi-Gaussian shape was implemented in view of the fact that it would require an infinite shaping time (and a non-causal system) in order to realize a Gaussian response. The semi-Gaussian response was chosen as a compromise between maximum theoretical noise performance and return-to-baseline time (pulse rate) capability. Since it would require an infinite amount of poles to implement a true Gaussian response along with infinite chip area and power dissipation, it is unrealistic to design this sort of circuit. Along with the first real-pole from the CSPA, four poles can adequately approximate a semi-Gaussian response [10]. The block diagram of the designed shaper is illustrated in Figure 2.6.

a)



b)

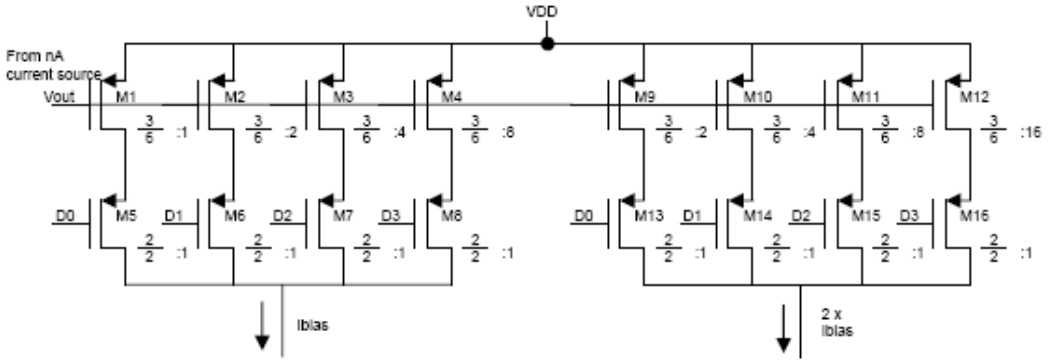


Figure 2.5 – a) Nanoampere current source for the CSPA feedback network, b) 4-bit DAC for bias current scaling [2]

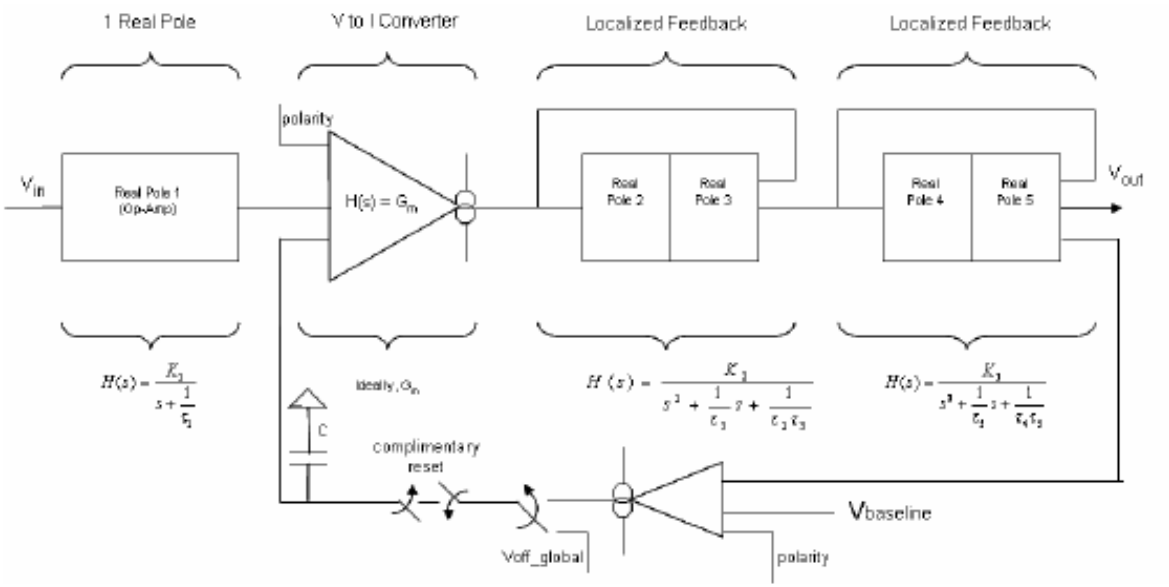


Figure 2.6 – Conceptual shaper block diagram [1]

From Figure 2.6, the output of the CSPA's first real pole is interfaced directly with an operational transconductance amplifier (OTA) that converts the voltage to a current. This was implemented to provide the filter topology with a current signal. The topology of the OTA shown in Figure 2.7 is a simple two stage amplifier, or equivalently an unbuffered operational amplifier (op amp). The OTA is unbuffered because it drives a very light load (or large resistance). The goal of this design was to obtain high linearity, therefore diode loads were implemented in the differential input stage. The input common mode range (ICMR) is not an important parameter in this application due to the active feedback elements around the CSPA. This provides zero DC current and therefore zero voltage drop from the input of the CSPA to the output (which is set to approximately mid-supply).

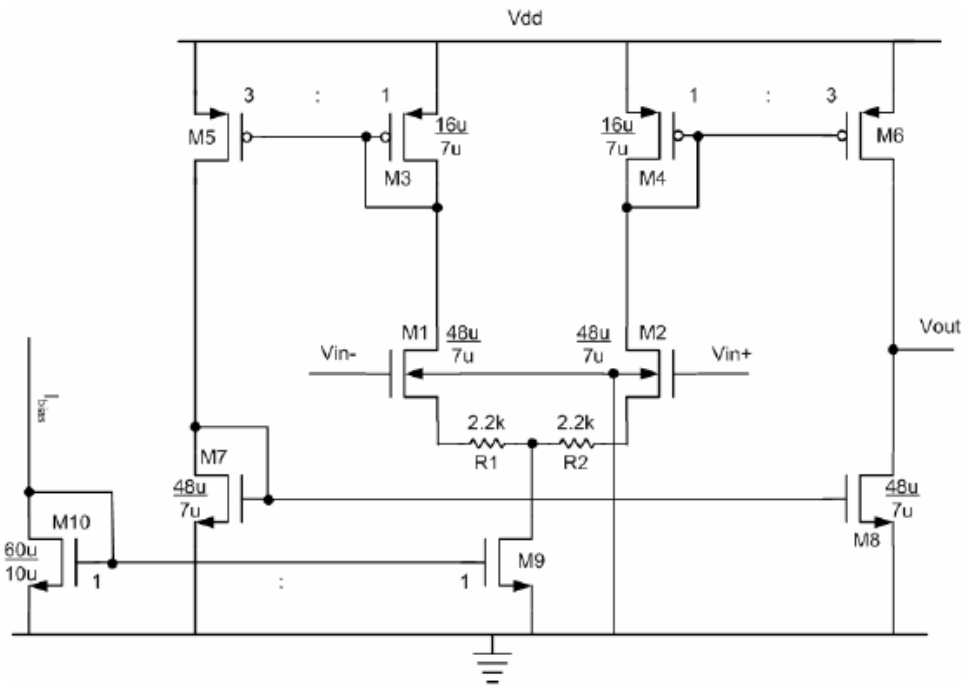


Figure 2.7 – Operational transconductance amplifier topology [1]

The circuit topology chosen to implement the four complex conjugate poles was a *free mode R-Lens filter*. This filter topology has the benefit of passing low frequencies relative to g_m-C filters, high linearity, voltage or current input, and a straight forward implementation with an even number of poles. The circuit topology is show in Figure 2.8. For further design steps and details, see reference [1].

As shown in Figure 2.6, a baseline restore amplifier completes a negative feedback loop so that the rest of the circuitry—the OTA (or V-to-I converter) and the four pole R-Lens low-pass filter—are its feedback elements. With the use of an off-chip reference, a DC threshold level is established for the signal processing chain allowing for an event to be readily discriminated for verification of occurrence. The baseline restore amplifier in this design is a ground-sensing OTA. The BLR OTA must be ground-

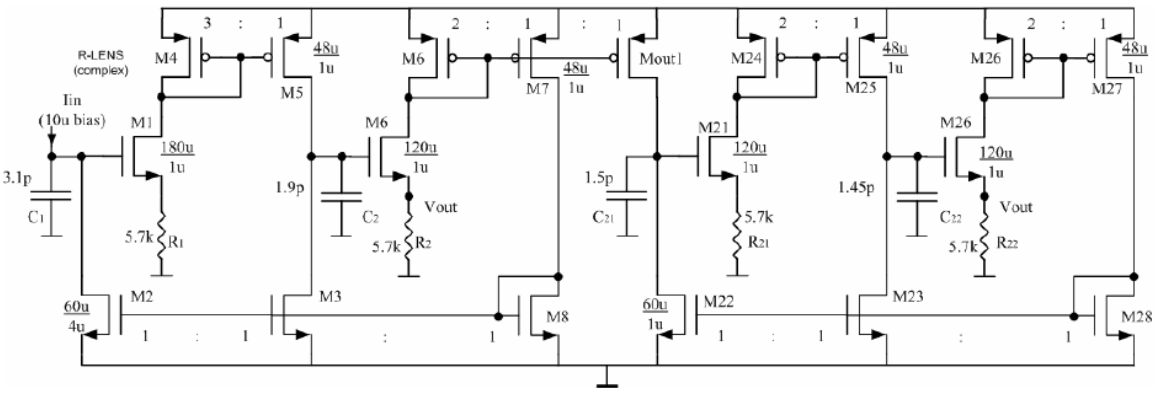


Figure 2.8 – Four-pole cascade complex conjugate R-Lens filter topology [1]

sensing capable since the output of the R-Lens filter will be nominally 100-mV when no signal is present. The circuit topology is show in Figure 2.9.

2.2.3 Patara Front End Block Diagram

With the previous work outlined, a block diagram of a single front-end channel in the microchip, *Patara*, is illustrated in Figure 2.10. The rest of the work presented in this thesis proceeds the output of the shaper.

2.3 System Requirements and Block Diagram

The SNS development has presented many new challenges with Data Acquisition Systems [6]. These cutting edge systems are pushing the limits of data handling as the produced data rates and intensities are expected to be among the highest and fastest of any current technology. Prior solutions to the analog signal processing (pre-amplification and shaping) were performed using PCB solutions with commercial-off-the-shelf

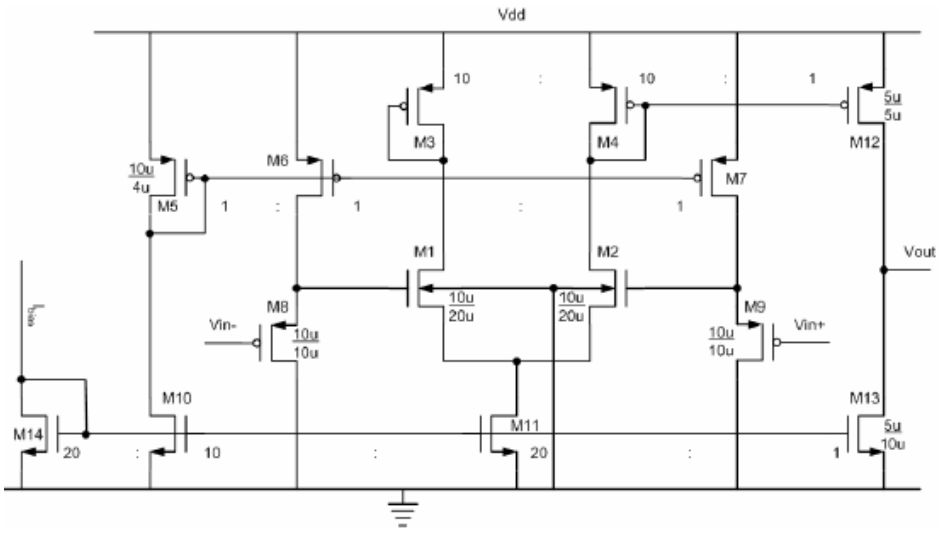


Figure 2.9 – Ground sensing baseline restore operational transconductance amplifier [1]

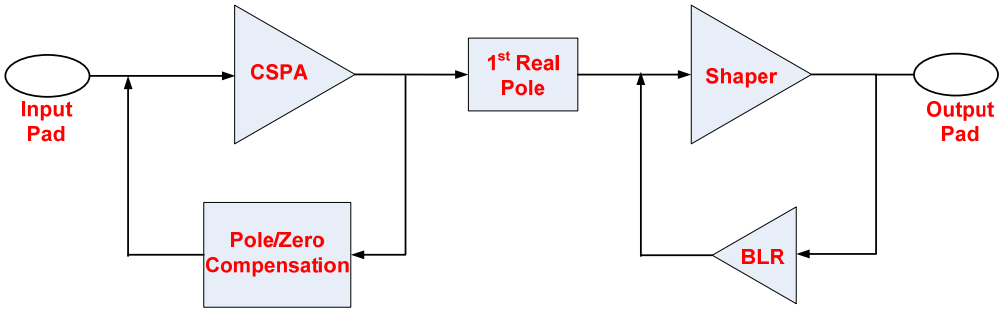


Figure 2.10 – Patara Channel Block Diagram

(COTS) components. This is acceptable for low density pixels (sensor resolutions greater than 1 millimeter). However, high channel counts can result for the analog signal processing when pixel resolutions undergo sub millimeter spacing. Consequently, this generates the need for a high density solution.

2.3.1 SNS Interface Requirements

To interface the SNS system, all input and outputs (I/O) must be digital—an interface standard for all SNS systems. The goal of this standard is to have a rear output card (ROC) that directly interfaces data acquisition software (DAS) on a CPU and the data acquisition system from the detector. The ROC acts as a buffer to the CPU, where the data acquisition system from the detector is not dependent on the DAS. This standard promotes design reuse and is intended to reduce software development time. Figure 2.11 illustrates a high level block diagram of an SNS system along with an example of a ROC.

Pertaining to this specific data acquisition system (*Patara III*), the ASIC is to

a) b)

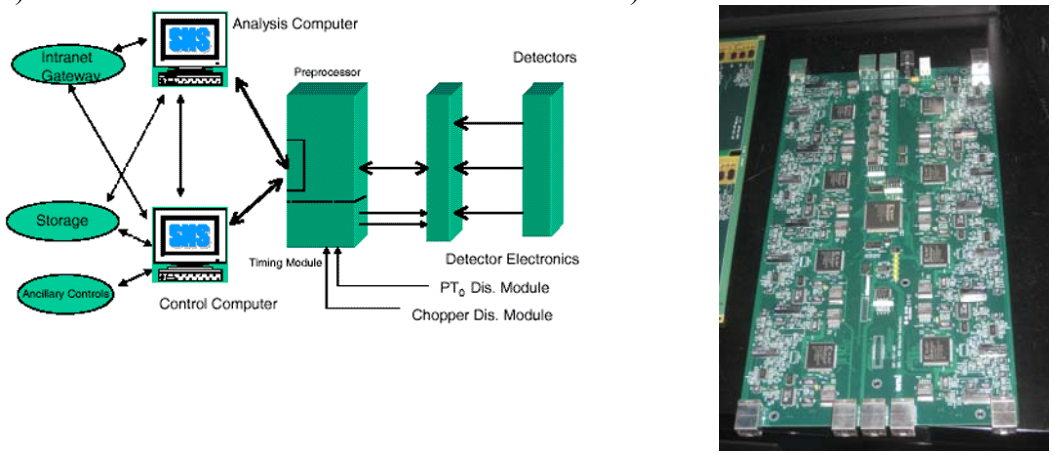


Figure 2.11 – a) Example of an SNS system [6], b) example of a rear output card (ROC)

provide a serial interface to the ROC for programming and calibration needs. This greatly reduces the amount of data lines and increases the ASIC functionality. The ASIC sends a parallel LVDS format data packet using a handshake protocol when active. This will allow high throughput, low noise, and an easily accessible data packet. The following two sections describe a block level of how this functionality is achieved.

2.3.2 Detector Readout Channel for Patara III

From the previously outlined work in *Patara*, a readout channel was designed having preamplification and shaping with DC baseline restoration (see Figure 2.9). To convey the event digitally, two comparators and a digital buffer were added after the shaper. The first comparator allows a DC threshold level to be established while the second comparator is present only to provide higher gain to the overall discriminator function (in other words, more gain for the 1-bit flash ADC). In addition, a digital buffer is added to the output of the discriminator in order to present a more ideal digital signal. Following the buffer, a synchronous/asynchronous digital backend is provided along with system registers so that a handshake protocol can be established between the ASIC and the ROC. A block level diagram of the discussed readout channel is shown in Figure 2.12. The previous work from *Patara* encompasses the *CSPA Front End* block, and the *Shaper* block.

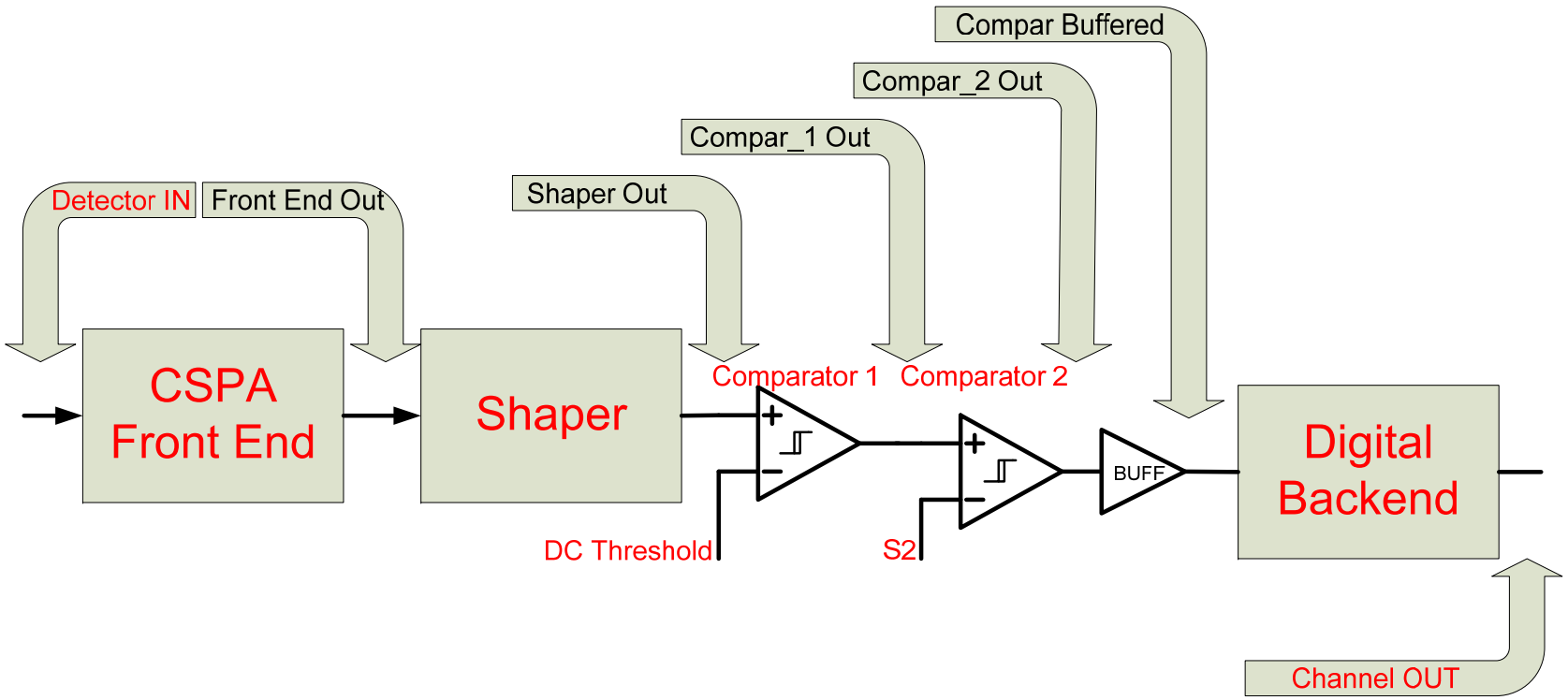


Figure 2.12 – Readout channel block diagram

Table 2.1 –System Select and Feedback Loop Rest truth table

System Select Truth Table	
Select	**f**
0	System A
1	System A Prime

Feedback Loop Reset		
Select	**feedback_rst**	**f**
0	0	active
0	1	reset
1	0	reset
1	1	reset

The digital backend is selectable between a synchronous or asynchronous state with the ROC. Therefore, this system will still operate using a handshake protocol but can also operate independently of the system clock. This is useful in the event charge injection into the substrate from the clock has become problematic. Since there are technically two systems, the synchronous system was dubbed *System A*, and the asynchronous system was labeled *System A Prime*. The ROC can select between the two systems with a *System Select* data line. *System A* does contain a feedback loop, and therefore is subject to instability or system latch up. If this is noticed by the ROC, a *Feedback Loop Reset* line will apply a reset. This feedback loop is not present in *System A Prime*. Therefore, when *System A Prime* is selected, this loop is always considered reset. These two lines are further accessible to the ROC and their truth tables are shown in Table 2.1.

2.3.3 64-Channel System Block Diagram for Patara III

With the channel design shown in Figure 2.12 having a physical height of 75 μm, a high density channel count can be accomplished. In this ASIC it was desired to be able

to readout 64 detectors, therefore the readout channel was repeated 64 times (resulting in an overall height of 4.8 mm) to form the *64-channel core*. This core would output event data from every detector channel in parallel. Due to the core's parallel nature, priority encoding must be implemented in the event of multiple hits. With the spatial resolutions of the 64 detectors being 100 μm, the chance of multiple hits occurring is highly improbable but must be considered. A binary encoder follows the priority encoder so that the event channel is presented to the ROC as a parallel 6-bit binary word. Since this system is highly concerned with noise, a Low Voltage Differential Signaling (LVDS) format was used via LVDS transmitters/receivers. When the data is ready to be sent to the ROC, a valid data flag is triggered. The ROC will then send back a reset command (hence the handshake protocol) to clear all system registers.

To set the DC level of the analog signal processing chain, an on-chip 8-bit current scaling calibration DAC was added. This DAC has a full-scale range of 600-mV and has an adjustable dynamic range. The same DAC design was repeated for the discriminator threshold level. In addition, a system test mode was implemented so that each of the 64 channels could be verified for proper operation. This was implemented by providing an on chip capacitance hosted by digital circuitry, and an additional 8-bit DAC so that a voltage could be placed across the capacitor resulting in a charge equal to the capacitance times the voltage ($Q=CV$).

To program the ASIC, a 99-bit serial shift register was implemented. The 99-bits are derived from the 64 enable bits for the channel test mode, the two 4-bit DACs used in

the CSPA feedback network, the three 8-bit DACs, and 1 bit for each of the three DACs offset control. The overall system block diagram is shown in Figure 2.13.

Due to the high integration demands on this system, two on-chip bandgap voltage references (BGRs) were designed for biasing of the DACs and the LVDS transmitters/receivers. All details of the design of the mixed-signal circuitry will be discussed in Chapter 3. Details on interfacing the programming circuitry and the dynamic data output are shown in Appendix A. In addition, Appendix A provides a pin-out diagram along with pin descriptions for the ASIC.

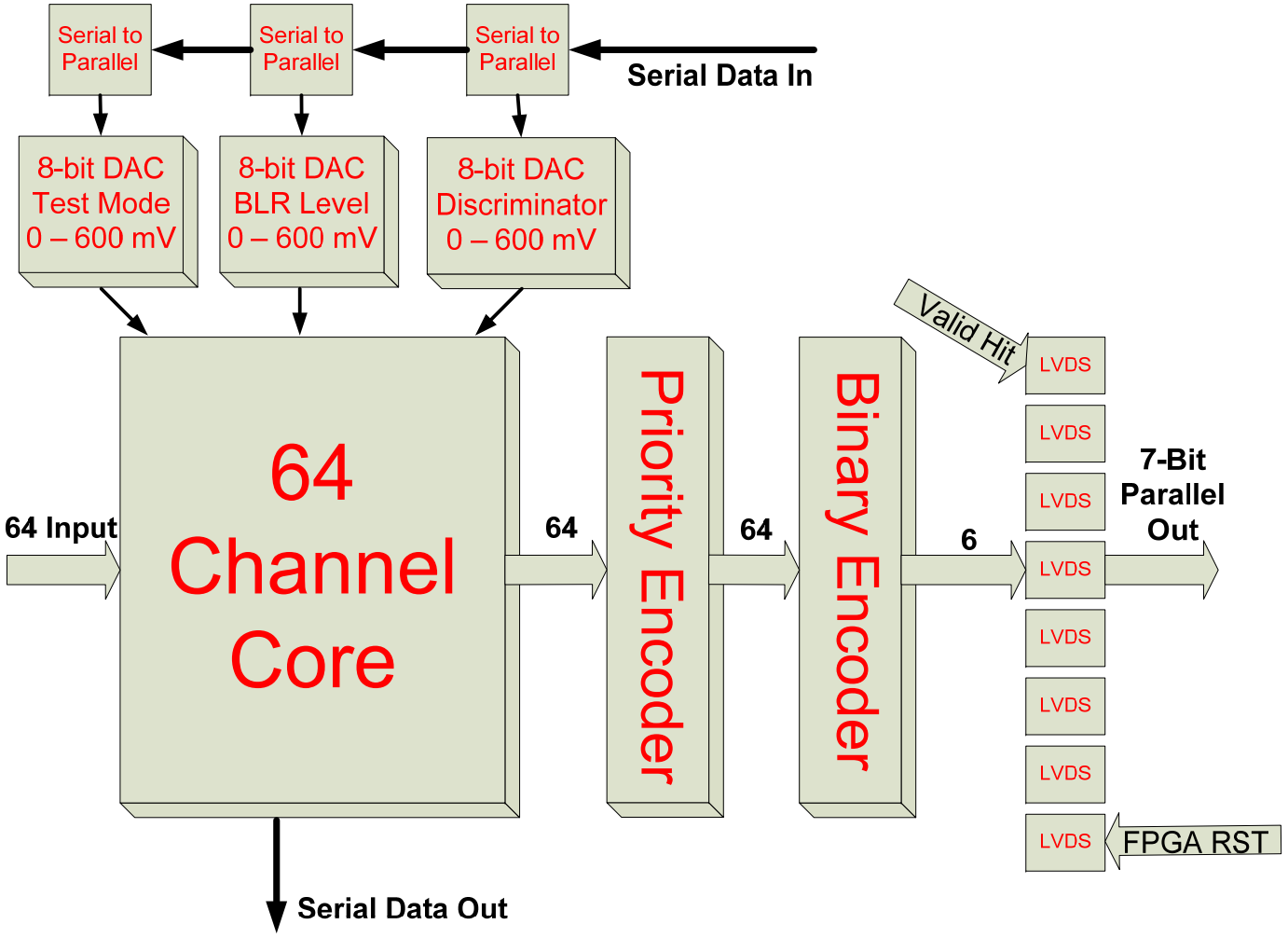


Figure 2.13 – Patara III ASIC block level overview

CHAPTER 3

DESIGN OF THE MIXED-SIGNAL COMPONENTS

3.1 Analog to Digital Conversion

The analog to digital conversion occurs when a hit propagates through the analog signal processing chain and has an amplitude greater than the set discrimination DC voltage level. To electronically implement this function, a ground sensing comparator circuit is used, similar to a 1-bit flash ADC. The BLR level of the analog circuitry is set nominally to 150-mV, consequently resulting in the need for the comparator to be ground sensing capable. The analog signal processing chain with the comparator is illustrated in Figure 3.1 along with example waveforms.

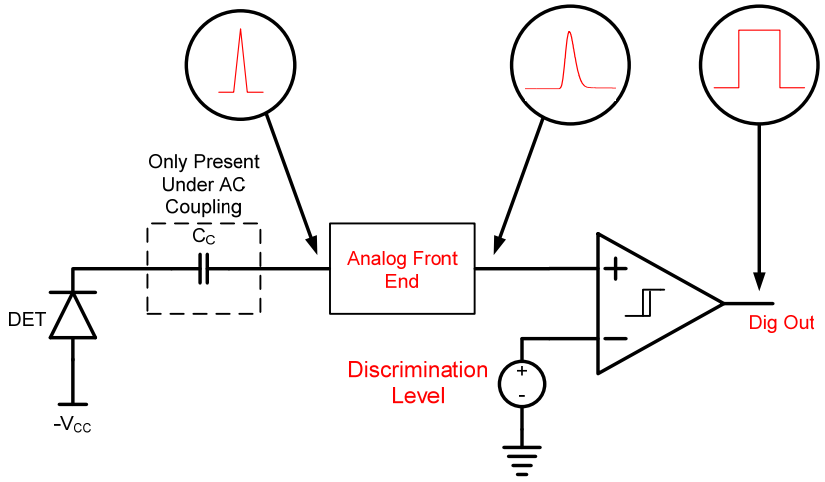


Figure 3.1 – Signal processing channel with comparator and example waveforms

3.1.1 Discrimination Level and Baseline Level Derivation

It was previously stated that the BLR level will be set to nominally 150-mV. This voltage level was chosen to ensure that the devices that make up the shaper stay in the saturation mode of operation. Keeping MOSFET devices in saturation increases their gain which ultimately leads to higher performance from the shaper.

With the BLR level set to a known DC potential, all incoming signals from the detector will have a DC offset equal to the BLR voltage. This is fundamental for discriminating the detector output signal under the occurrence of a neutron event. To accurately set the discrimination level, a general idea of the detector specifications must be understood.

Since the detector is based on alpha-n reactions in ^{10}B, charged particles are released with a reaction Q-value of 4.79 MeV [12]. The alpha particle will release the largest amount of energy creating an accumulated charge (electron-hole pairs) in the silicon substrate of the detector that can be collected by the CSPA. However, background gamma radiation will also create charge within the detectors substrate.

Simply reducing the low-level discriminator (LLD) setting (discriminator threshold) to lower values can increase the efficiency, yet the risk of including background radiation events, as from gamma rays, increases as the LLD is lowered [12]. The neutron reactive coating thickness does have an impact on the optimal LLD setting for the electronics. From Figure 3.2, it is readily discerned that the lower LLD has a higher detection efficiency. The compromise between background radiation, ^{10}B

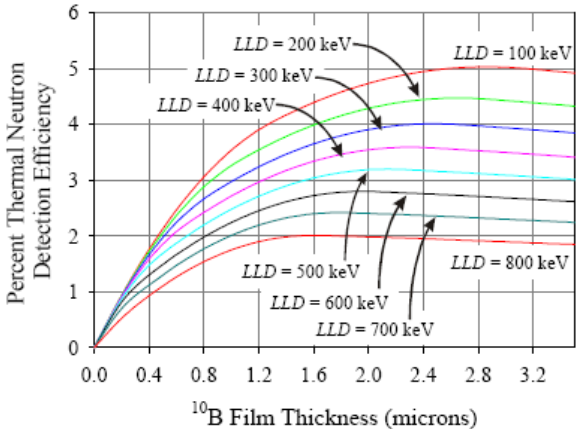


Figure 3.2 – Thermal neutron efficiency as a function of ^{10}B thickness and LLD setting from [12]

thickness, and detector efficiencies led to an LLD (discrimination level) of 300 keV above the baseline level of 150-mV.

The 300 keV LLD setting needs to be translated to a voltage so that an external bias level can be set. In silicon, it takes 3.6 eV to create an electron-hole pair (exciton). Therefore,

$$\frac{300\,keV}{3.6\,eV} = 83{,}333\,electron - hole\ pairs. \tag{3.1}$$

This will produce a charge of $1.6\times10^{-19}\ C$ that translates to

$$83{,}333\times1.6\times10^{-19} = 13\,fC. \tag{3.2}$$

The charge gain from the input of the CSPA to the output of the shaper is approximately

$$9.6\,\frac{mV}{fC}. \tag{3.3}$$

Therefore the voltage level above the baseline level is

$$9.6\frac{mV}{fC}\times 13\ fC = 125\ mV\,, \tag{3.4}$$

resulting in a discrimination level of,

$$BLR\ Level + LLD\ Level = 150\ mV + 125\ mV = 275\ mV. \tag{3.5}$$

3.1.2 Comparator Design and Schematic

PMOS input devices were used in the design of the comparator to enhance ground sensing capability. In many cases a PMOS differential pair can sufficiently make up the input stage to the comparator. In this design, PMOS source-followers (devices M_8 and M_{14} in Figure 3.3) were used to buffer the input to an NMOS differential pair (M_1 and M_2). This allowed for a below-ground sensing capability since the drains of the input buffers are common to ground, whereas a differential pair normally has active loading connected to the drains of the input devices.

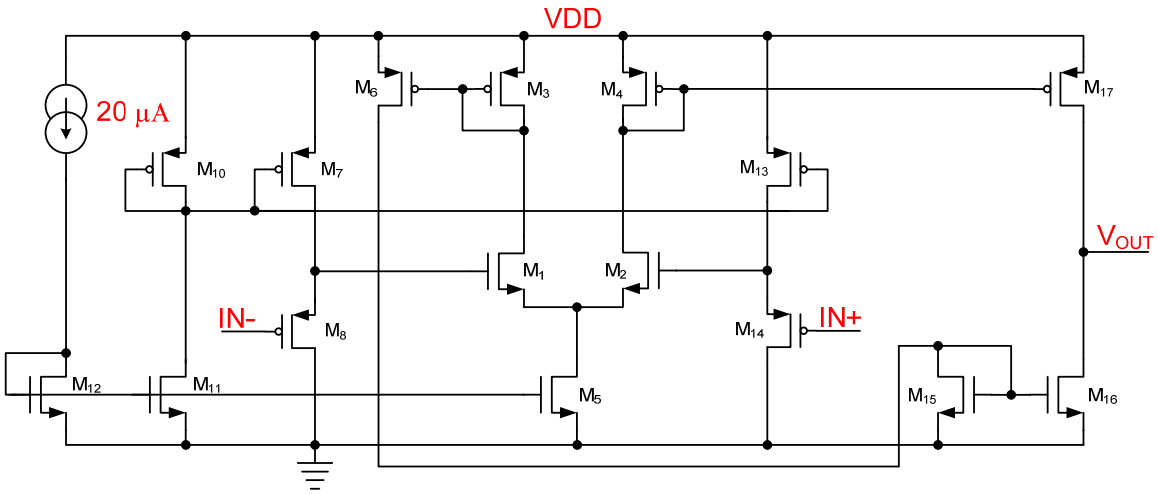


Figure 3.3 – Ground sensing comparator used for DC level discrimination

The design of a comparator is very similar to that of an uncompensated op amp. A comparator is optimized for large-signal conditions, whereas an op amp must be optimized for large-signal and small-signal conditions. Compensation of an op amp is generally performed to optimize small-signal performance, but it also contributes to large-signal effects such as slew rate (SR). Since this comparator is to switch to 3.3-V if the sensing terminal (*IN*+) is above the reference terminal (*IN*-), a large SR is needed to do this quickly. Consequently, SR is always maximized without the presence of any compensation capacitors. Another reason why a comparator does not need to be optimized for small-signal conditions is that there will never be negative feedback around the circuit—it is always in an open-loop configuration.

Figure 3.1 illustrates an ideal square wave at the output of a comparator. To output an ideal square wave, the comparator would need infinite gain and infinite SR. In reality a designer can never achieve these ideal characteristics, therefore certain techniques must be utilized to approximate ideality. Two techniques were used in this design to increase gain and provide high SR and will be discussed in the next section.

3.1.3 Simulation Results and Discussion

The gain of the comparator shown in Figure 3.3 will increase as the input overdrive increases. The input overdrive is defined as the positive differential voltage with respect to the reference terminal (*IN*-). This comparator also "walks" with higher input overdrives. "Walk" occurs due to the longer amount of time the input signal is

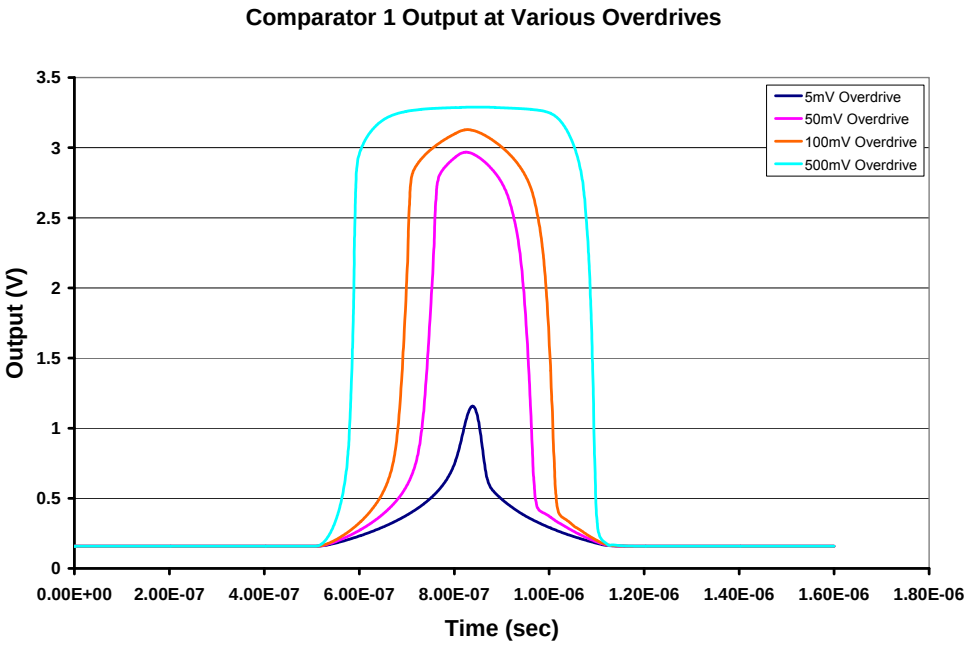


Figure 3.4 – Comparator output characteristics at different input overdrives

greater than the discrimination level at higher overdrives. Figure 3.4 illustrates the output characteristics of this comparator with a discrimination level of 175-mV.

It is easily assessed that the gain of this comparator is significantly low with an input overdrive of 5-mV. To increase the gain, a second sequential comparator is added to the channel. This technique is illustrated in Figure 3.5. Here the second comparator will discriminate a larger overdrive signal with a small input overdrive at the first comparator—hence the added gain. Figure 3.6 illustrates the output characteristics of the sequential comparator with the same input overdrive levels as shown in Figure 3.4.

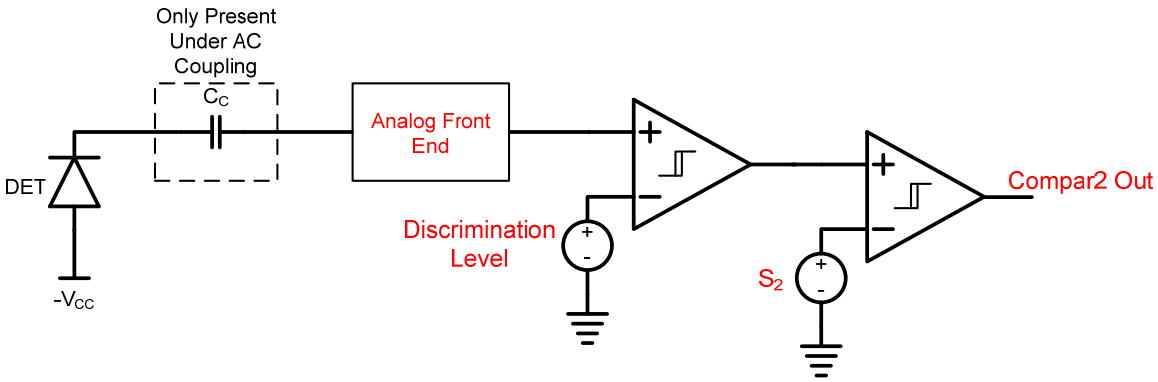


Figure 3.5 – Channel block diagram with sequential comparator configuration

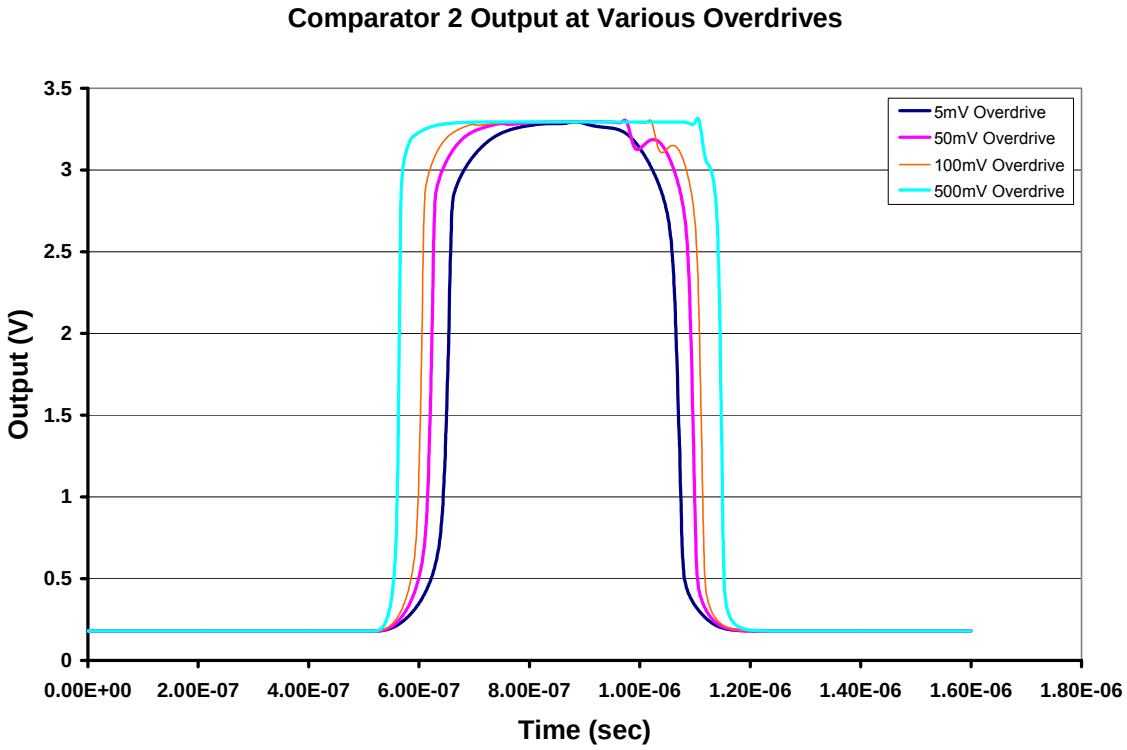


Figure 3.6 – Comparator 2 output at varying input overdrives to the first comparator

Digital buffering was used to present a more ideal digital square wave output from the sequential comparator. This buffer adds gain and increases SR to the comparator circuitry. The output of the digital buffer is shown in Figure 3.7 and results in a simulated rise time of τ_R = 0.73 nanoseconds with a 1 pF load. Notice that the output offset from the comparators do not propagate through digital buffering.

The circuitry of the digital buffer circuit used is a cascaded inverter. The aspect ratio of the second stage was designed to be 5 times that of the first stage. This aids in drive capability but results in a little larger delay. In addition, the aspect ratios of the PMOS devices are 2.5 times that of the NMOS devices. This is a general rule-of thumb to balance the drive strength between the PMOS and NMOS [13].

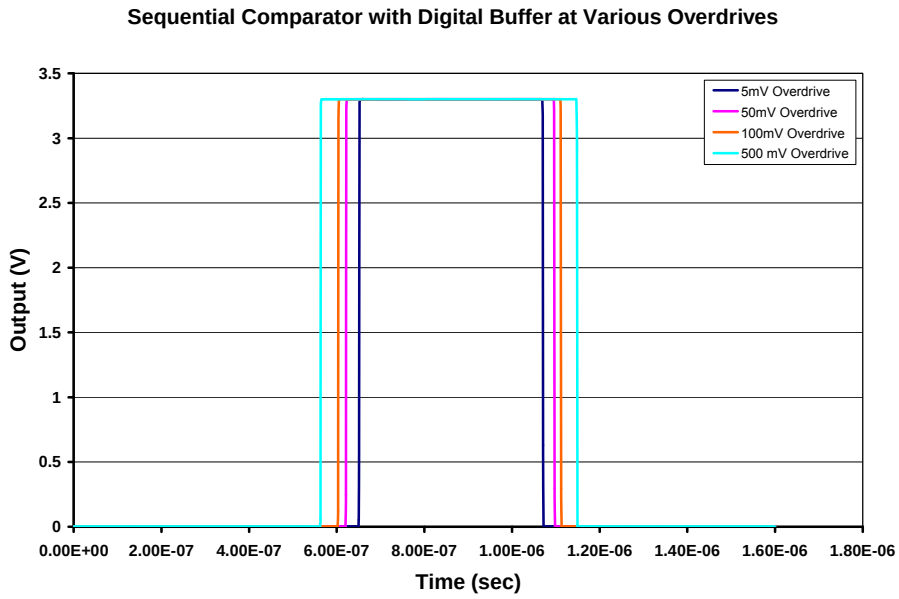


Figure 3.7 – Digitally buffered sequential comparator with different input overdrives

3.2 *Selectable Synchronous/Asynchronous Digital Backend*

With the comparator circuitry designed to output a TTL (transistor to transistor logic) compatible signal when a neutron event occurs, the next task is to digitally register the event and provide a handshake protocol that can be synchronous or asynchronous with the rear output card (ROC). This design utilizes bistable multivibrator circuitry (flip-flops) for the majority of the logic realization. The first part of the implementation provides edge detection of the comparator output signal. The second part implements registering that holds the event logic until the ROC provides a reset prompt. A digital multiplexer is provided at the output to enable selection between synchronous (*System A*), and an asynchronous mode (*System A Prime*).

3.2.1 Synchronous Edge Detection Logic and System Registers (*System A*)

The use of bistable multivibrator circuits allows for easy synchronization with a system clock. This design specifically utilizes D-Flip-Flops. To detect a digital edge, the sequence of events must be a logic '0' on the first clock, and a logic '1' on the second clock. Therefore only two D-Flip-Flops are necessary for memory. Figure 3.8 illustrates

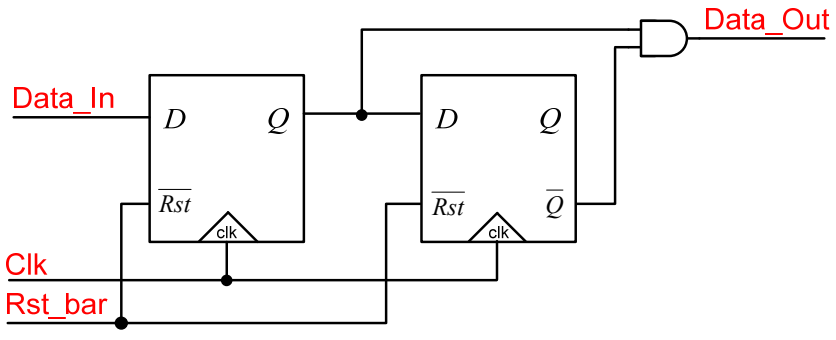


Figure 3.8 – Synchronous edge detection logic [14]

the implemented synchronous edge detection logic [14]. Here, the first D-Flip-Flop (DFF) stores a logic '0' on the first clock. On the second clock, the second DFF will register the logic '0' from the first DFF and output a logic '1' from the $\overline{Q}$ terminal while the first DFF will clock in a logic '1' and output a logic '1' from the Q terminal. Since the Q terminal from the first DFF and the $\overline{Q}$ terminal from the second DFF are connected to an AND gate, the AND gate will output a logic '1' under the presence of a rising edge. However, this detection will be cleared after one clock cycle. The timing description is shown in Figure 3.9 with a 10 MHz clock.

Since the signal from the comparator may have a short "walk" time, an input register is required. This will ensure detection any time the comparator trips high. In addition to an input register, an output register must be used to hold the edge detection

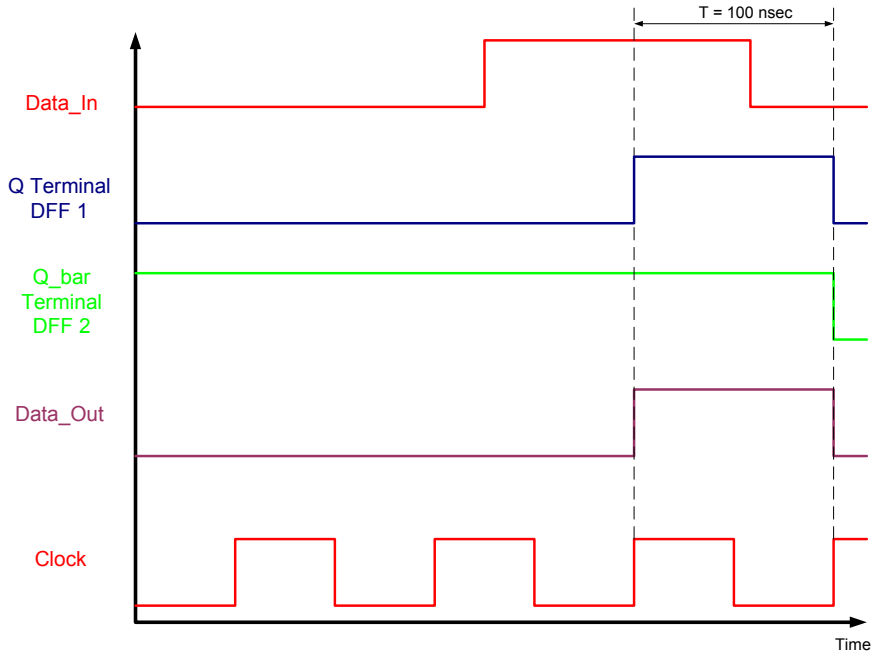


Figure 3.9 – Timing diagram for the synchronous edge detection circuitry

logic longer than a clock period if necessary. Registering the input and output of this circuitry allows the ROC to have control over when registers are cleared. This gives the ROC the "handshake" ability, meaning that it can give a reset command once it has received the event data. The register used was a simple DFF. Tying the *D* terminal of the DFF high and wiring the input signal to the *CLK* terminal allows the signal to be registered on a rising edge until a reset signal is sent. The DFF register configuration is show in Figure 3.10.

Since the input signal from the comparator is registered, the system can experience "dead-time." This means that an event can occur again prior to the input register being cleared which will be two full clock periods (200 nsec with a 10 MHz clock). To remedy this, a feedback path will clear *only* the input register in one clock period after an event has been registered at the output. This will allow the ROC to receive the event data while the input register is cleared for another event to be detected. In this system (*System A*), the ROC has no control over resetting the input register. In the case that a second event occurred while the ROC was processing the first event, the ROC

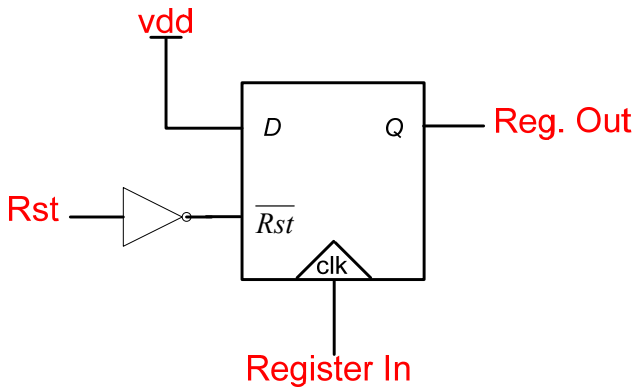


Figure 3.10 – DFF register configuration

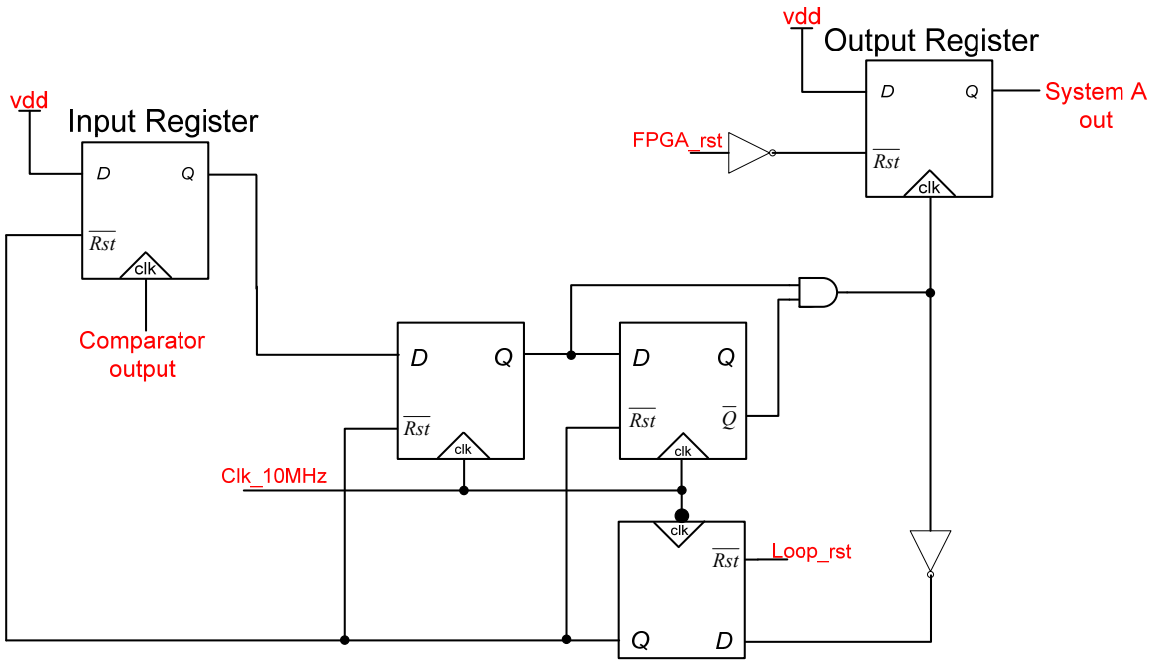


Figure 3.11 – System A with input and output registers

will apply a reset clearing the input register of the second event. This ultimately counter affects the use of the feedback circuitry and therefore the ROC is not granted access to the input registers reset terminal. Since a feedback loop is used, system latch up or metastability could occur. To release this state, a DFF element is used that is clocked off $\overline{clk}$. Therefore, the DFF can be reset to a known state if suspicious behavior is noticed. The final circuitry for *System A* is shown in Figure 3.11.

3.2.2 System Select Circuitry (*System A / System A Prime*)

To implement an asynchronous system mode (*System A Prime*), the signal path must bypass the edge detection circuitry. This can be performed by directly passing the input register's data line to the output register. This allows the ROC to provide a reset

prompt once the data is read asynchronously. However, both registers will be considered "dead" until the reset signal is applied 200 nsec later. Therefore if another event occurs on this channel, the ROC will miss the event.

With the two systems now designed, the next step is to provide both modes of operation with minimal control signals. Utilizing two port multiplexers allows for only one control line while providing the ability to operate both systems. This control line is called *select_dig* and will be provided to the ROC. The remaining control lines are the 10 MHz system clock, the system reset line (*Rst_FPGA*), and the feedback loop reset line (*Loop_rst*). This totals 4 control lines for the ROC to operate the digital backend. See Table 3.1 for a logic reference when interfacing the digital system. The final schematic including *System A* and *System A Prime* along with the input and output registers is shown in Figure 3.12.

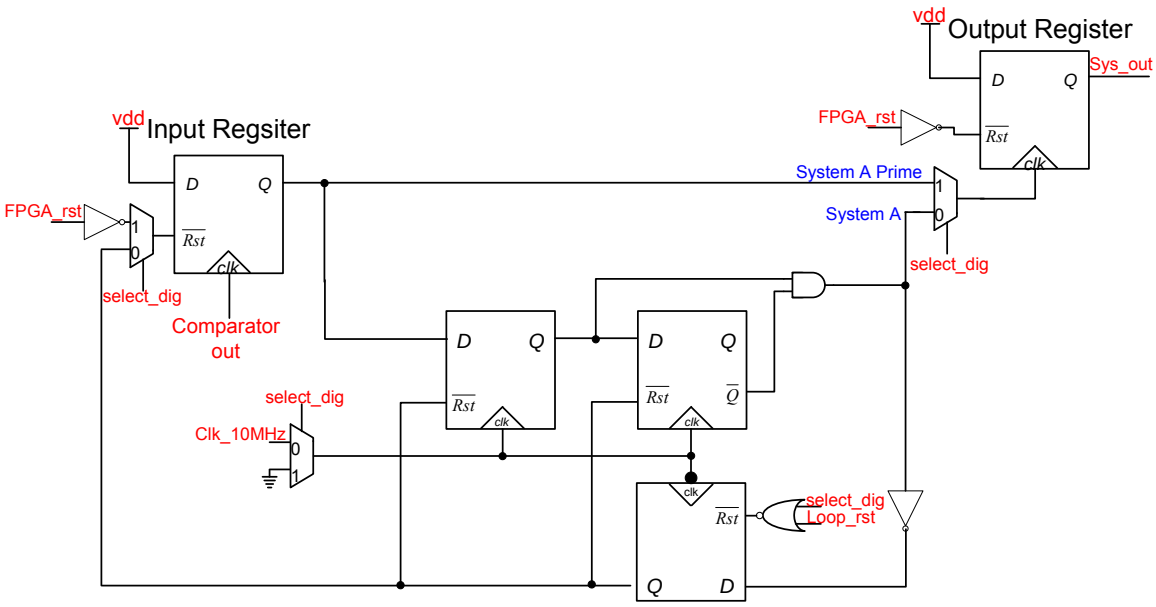


Figure 3.12 – *System A* and *System A Prime* schematic along with input and output registers

Table 3.1 – Digital system interface logic for the rear output card connectivity

Digital System Interface Logic

System Select		**System Reset**	
Select_dig	f	*Rst_FPGA*	f
0	System A	0	active
1	System A Prime	1	reset
System Clock		**Feedback Reset**	
Select_dig	f	*Loop_rst*	f
0	10 MHz	0	active
1	GND	1	reset

3.2.3 System Simulation and Timing Diagram

The key difference between *System A* and *System A Prime* is of course the presence of a system clock. However, another difference is how the two systems handle the input register. With *System A*, the input register is actively reset by a feedback delay element. *System A Prime*'s input register is passed directly to the output register. In the case of *System A Prime*, the input register will be "dead" for two full clock periods until the ROC prompts the system with a reset. *System A*'s post layout simulation illustrating timing characteristics and the pulse-pair resolution is shown in Figure 3.13. Figure 3.14 illustrates the simulation results and timing characteristics of *System A Prime*. Figure 3.15 and Figure 3.16 both illustrate the two systems and their "dead time" characteristics.

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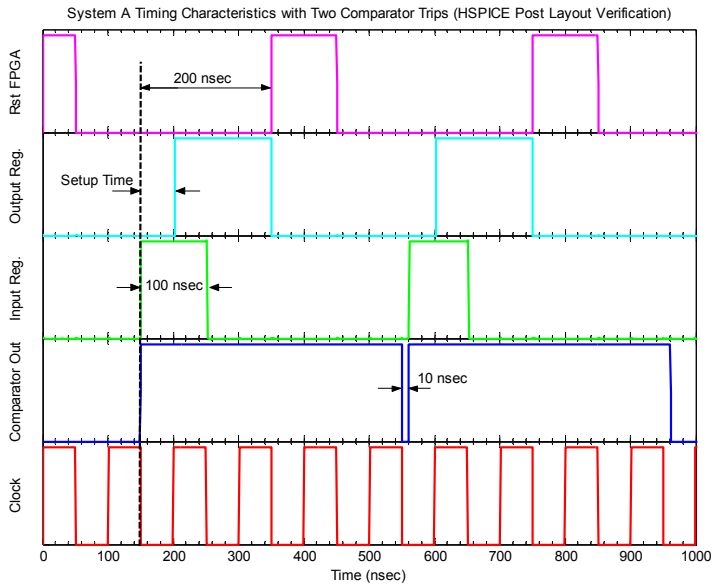

Figure 3.13 – *System A* post layout simulation results illustrating timing characteristics

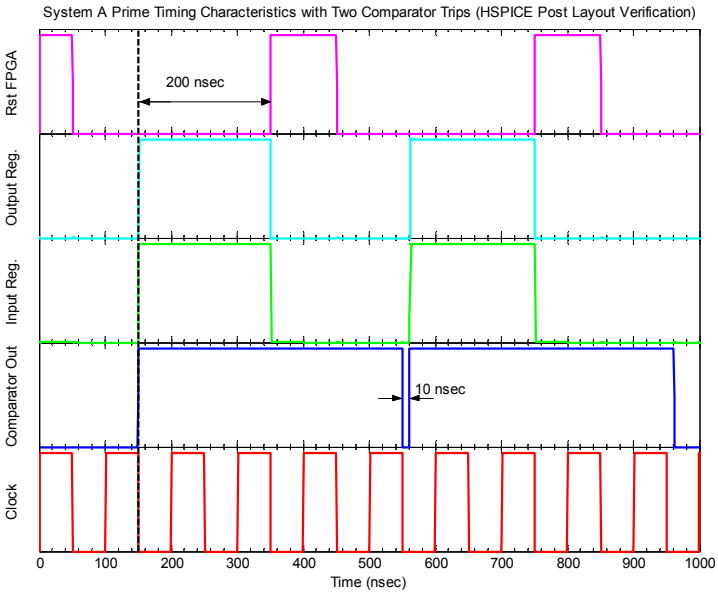

Figure 3.14 – *System A Prime* post layout simulation results illustrating timing characteristics

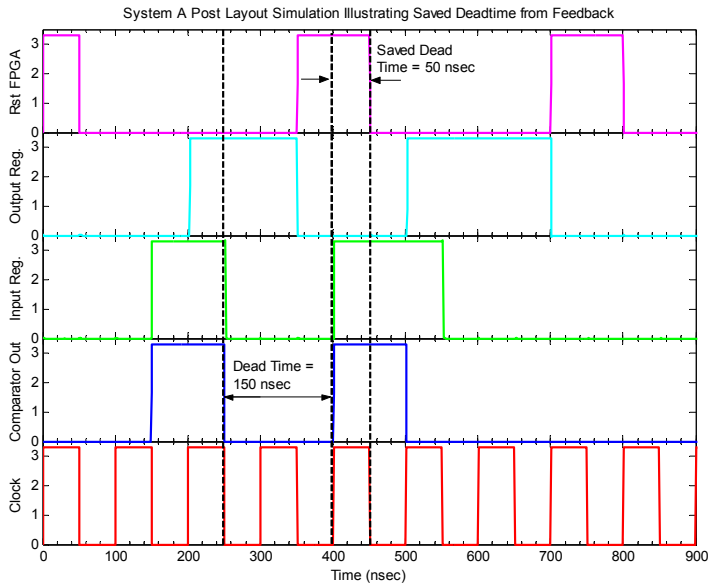

Figure 3.15 – *System A* simulation results illustrating system "dead time"

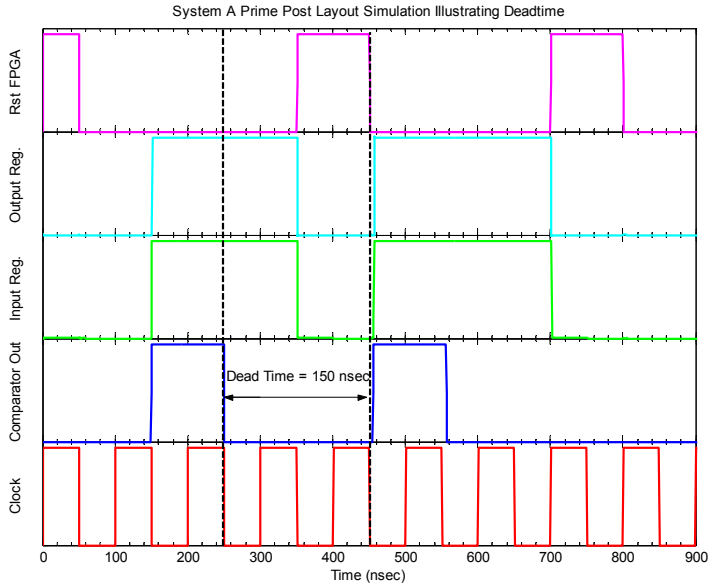

Figure 3.16 – *System A Prime* simulation result illustrating system "dead time"

3.3 64-to-64 Priority Encoder

The selectable synchronous/asynchronous digital backend system is repeated 64 times with one at the backend of each channel. Under the presence of a neutron event on a given channel, a 3.3-V TTL compatible signal will output. Since each channel is in parallel, multiple events may occur prior to the ROC reading an event. To handle multiple hits, priority encoding is implemented so that Channel 0 has the highest priority. This means that if a neutron event occurs on Channel 0 and on Channel 63, the ROC will read an event at Channel 0 and will not be notified of any event occurring at Channel 63.

This logic realization of the 64-bit priority encoder utilized logic blocks from a digital standard cell library provided by the Oklahoma State University (OSU) VLSI Computer Architecture Research group [15]. High Level Description Language (HDL) was not used to synthesize any logic realizations. This is desired so that a specific architecture could be used and could be fit to the exact physical pitch of the 64-channel core. Utilizing custom CAD tools (such as Cadence), even tracing between parallel logic gates allows for optimization of slack on any given signal path. This did take slightly more design time, but ultimately resulted in a highly robust and specific design.

The priority encoder is implemented entirely using static logic gates and a parallel priority look-ahead architecture. This architecture utilizes an optimized 8-bit priority encoder (PE) cell that is grouped in a bank of 8 total PE's resulting in 64 bits. This technique allows for parallel processing ultimately leading to minimal delay. The first topic discussed will be the design and derivation of the 8-bit PE cell.

3.3.1 8-Bit Priority Encoder Cell

In a multibit PE, the output of the *i*th bit is $EP_i = D_i \bullet P_i$, where D_i is the corresponding input data and P_i is the priority token passed into this bit [16]. When the input to the highest priority token bit is 0, the priority token is passed into the next priority bit: $P_i = \overline{D_{i-1}} \bullet P_{i-1}$. The general expression of EP_i is written as [16]:

$$EP_i = D_i \bullet \overline{D_{i-1}} \bullet \overline{D_{i-2}} \bullet \overline{D_{i-3}} \cdots \overline{D_1} \bullet \overline{D_0}. \quad \textbf{(3.6)}$$

By sharing common terms and adding a *look-ahead* token (*LA_in*) to enable the cell, the function of the 8-bit PE cell is written as [16]:

$$\begin{aligned}
EP0 &= LA_in \bullet D0 \\
EP1 &= LA_in \bullet \overline{D0} \bullet D1 \\
EP2 &= LA_in \bullet \overline{D0} \bullet \overline{D1} \bullet D2 \\
EP3 &= LA_in \bullet \overline{D0} \bullet \overline{D1} \bullet \overline{D2} \bullet D3 \\
EP4 &= LA_in \bullet \overline{D0} \bullet \overline{D1} \bullet \overline{D2} \bullet \overline{D3} \bullet D4 \\
EP5 &= LA_in \bullet \overline{D0} \bullet \overline{D1} \bullet \overline{D2} \bullet \overline{D3} \bullet \overline{D4} \bullet D5 \\
EP6 &= LA_in \bullet \overline{D0} \bullet \overline{D1} \bullet \overline{D2} \bullet \overline{D3} \bullet \overline{D4} \bullet \overline{D5} \bullet D6 \\
EP7 &= LA_in \bullet \overline{D0} \bullet \overline{D1} \bullet \overline{D2} \bullet \overline{D3} \bullet \overline{D4} \bullet \overline{D5} \bullet \overline{D6} \bullet D7
\end{aligned} \quad \textbf{(3.7)}$$

Notice that the total theoretical delay for each priority bit (EP_i) is one AND gate. This is reduced from multiple gate delays in previous designs [17] and [18].

Since the OSU standard library was used, the logic realization is limited to specific gates. Within this library, the largest quantity of inputs is provided by a 3-input NAND gate. Therefore a fan-in technique must be used for the priority bits containing

more than 3 inputs. In addition, an inverter at the output of the NAND gate must be used. This results in a maximum delay of two NAND gates and two inverters for priority bits EP_2 through EP_7.

Since this architecture is a parallel approach, some logic gates can end up driving a large number of gates. Driving a large number of gates can saturate the output of the driver and must be avoided. Therefore, a standard was set so that one logic gate would not drive more than four total gates. To do this, two buffers were used in parallel at the output of a gate that would be connected to four or more other gates resulting in a partitioned net. This conservatively reduced the risk of saturating the output of a driver on a given signal path. The resulting logic realization of the 8-bit PE is shown in Figure 3.17.

3.3.2 Parallel Priority Look-Ahead Architecture

The priority look-ahead scheme is used to reduce priority encoding delays associated with priority propagation [16]. Since 64 data lines are to be priority encoded, delays can become significant without this style of architecture. This architecture is based on parallel processing of *look-ahead* tokens. The token is used as a flag to enable a specific 8-bit PE cell in a bank of 8 total priority encoders, and ultimately addresses the processing chain so that the encoded output propagates through the least amount of logic gates necessary. In a 64-bit PE design, an 8-input OR gate cell can be used to examine if

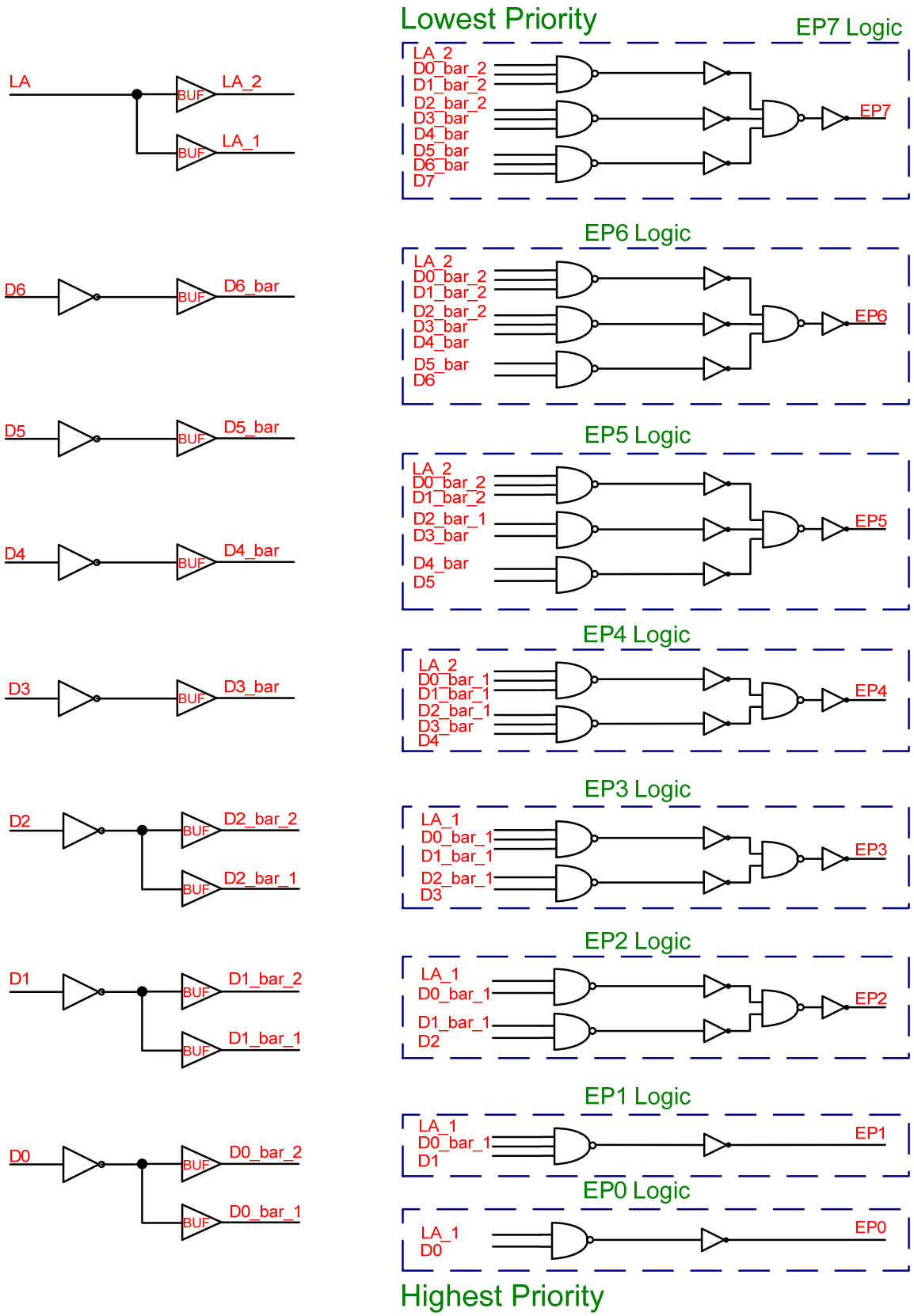

Figure 3.17 – 8-Bit Priority Encoder Cell

a logic ‘1’ exists in any of the inputs. This results in a bank of 8 total 8-input OR gate cells, with the first 8 bits being realized as [16],

$$OR0 = D0 + D1 + D2 + D3 + D4 + D5 + D6 + D7. \quad \textbf{(3.8)}$$

If all the inputs are a logic ‘0’ to the first set of bits, the output of OR_i is a logic ‘0’ and the priority token is passed to OR_{i+1}. The *look-ahead* tokens can then be expressed as [16],

$$\begin{aligned}
LA0 &= OR_0 \\
LA1 &= OR_1 \bullet \overline{OR_0} \\
LA2 &= OR_2 \bullet \overline{OR_1} \bullet \overline{OR_0} \\
LA3 &= OR_3 \bullet \overline{OR_2} \bullet \overline{OR_1} \bullet \overline{OR_0} \\
LA4 &= OR_4 \bullet \overline{OR_3} \bullet \overline{OR_2} \bullet \overline{OR_1} \bullet \overline{OR_0} \\
LA5 &= OR_5 \bullet \overline{OR_4} \bullet \overline{OR_3} \bullet \overline{OR_2} \bullet \overline{OR_1} \bullet \overline{OR_0} \\
LA6 &= OR_6 \bullet \overline{OR_5} \bullet \overline{OR_4} \bullet \overline{OR_3} \bullet \overline{OR_2} \bullet \overline{OR_1} \bullet \overline{OR_0} \\
LA7 &= OR_7 \bullet \overline{OR_6} \bullet \overline{OR_5} \bullet \overline{OR_4} \bullet \overline{OR_3} \bullet \overline{OR_2} \bullet \overline{OR_1} \bullet \overline{OR_0}
\end{aligned} \quad \textbf{(3.9)}$$

Notice the similarities between equation 3.9 and 3.7. It is evident that the 8-bit PE cell can be used to generate the *look-ahead* tokens with $OR_0 - OR_7$ as inputs. Therefore it will take a bank of 8 total 8-bit PE’s, plus one 8-bit PE for the *look-ahead* tokens, and a bank of 8 total 8-input OR gates to implement the 64-bit PE. The final 64-bit parallel priority look-ahead encoder is shown in Figure 3.18.

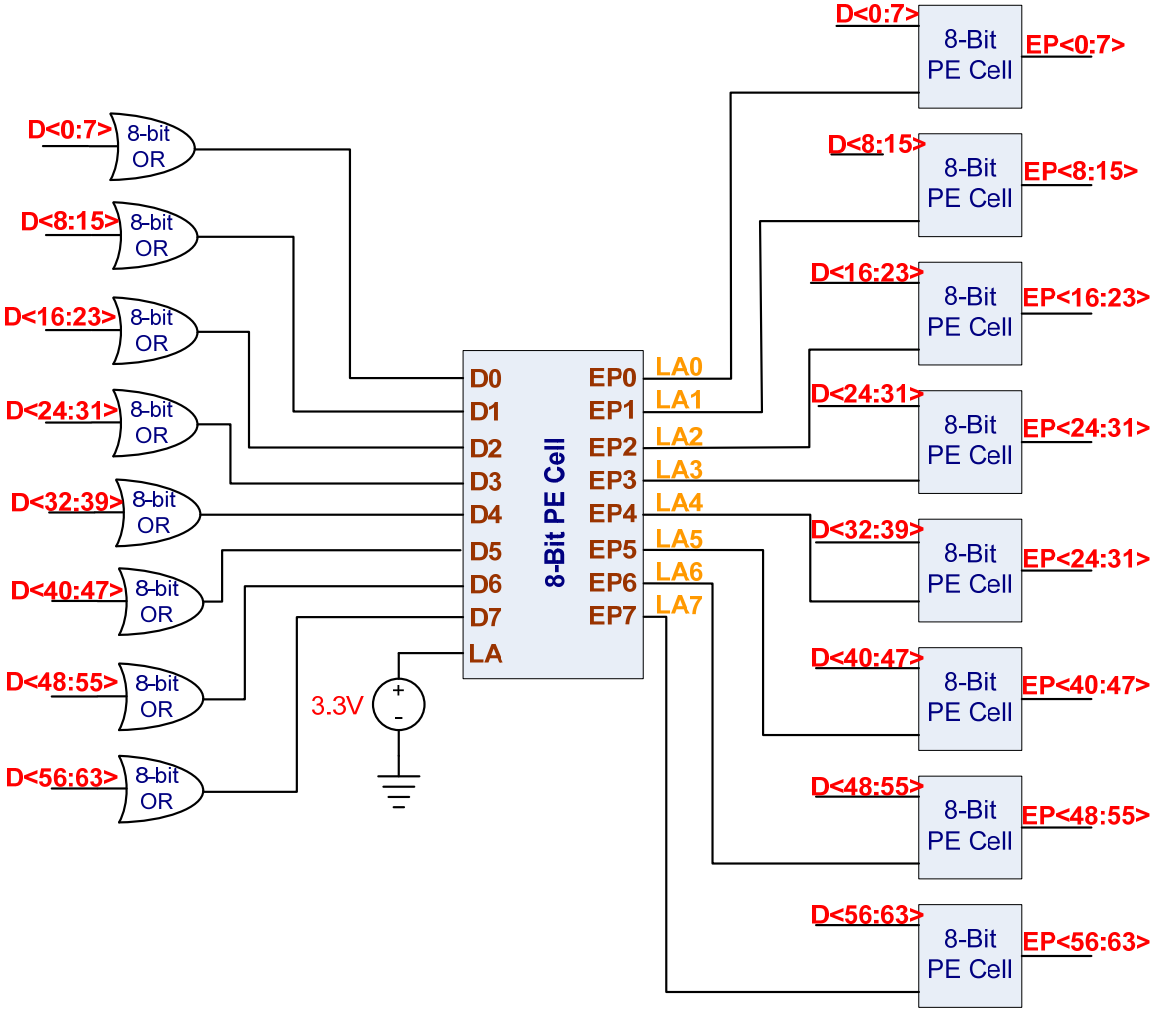

Figure 3.18 – 64-bit parallel priority look-head encoder

3.4 64-to-6 Binary Encoder

The ASIC and the ROC could theoretically interface each other after the 64-bit priority encoded output from the 64-channel detector readout core. However, it would require 64 parallel data lines just for the channel ID of the neutron event. This is highly undesirable since there is not an unlimited amount of pads on the ASIC. At this point it is evident that the binary encoder is needed. Since 64 data lines are to be converted to a binary word, it will take 6-bits to express this digitally ($2^6 = 64$). Again, this encoder was designed without the assistance of HDL. A custom static logic design was desired so that the physical pitch of this encoder could be matched to that of the priority encoder. All logic realization was implemented from the OSU standard cell library.

3.4.1 Basic 4-to-2 Binary Encoder

A binary encoder encodes information from 2^n inputs into an n-bit code, where exactly one of the n-input signals should have a logic value of '1' [19]. The outputs of the binary encoder presents the binary number that identifies which of the n-inputs is equal to a logic '1.' In this ASIC, the output will indicate which channel underwent a

a)

2-Bit Binary Encoder					
w3	**w2**	**w1**	**w0**	**Y1**	**Y0**
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

b)

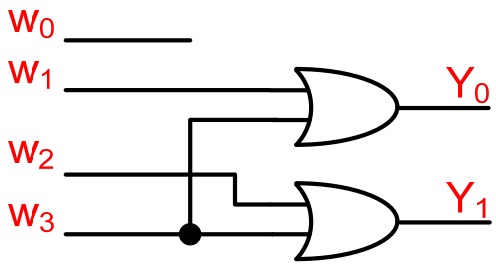

Figure 3.19 – a) truth table and b) logic realization for a 2-bit (4-to-2) binary encoder [19]

neutron occurrence. A truth table and logic realization for a simple 4-to-2 (2-bit) binary encoder is illustrated in Figure 3.19. The Boolean algebraic expression for each bit is,

$$Y_0 = w1 + w3$$
$$Y_1 = w2 + w3 \qquad \textbf{(3.10)}$$

Notice that the least significant bit (LSB) of the input is neglected. This signifies that a valid '00' state exists. This will be relevant in the next design topic when the Valid Data Flag is discussed.

3.4.2 64-to-6 Binary Encoder Realization

Translating the 2-bit concept to a 6-bit implementation is relatively straight forward. It should be noticed that only half the input data is needed to encode each output bit. However, each output bit has a unique sequence of inputs to evaluate. The logic implementation is shown in Figure 3.20. In this case, each bit will be evaluating 32

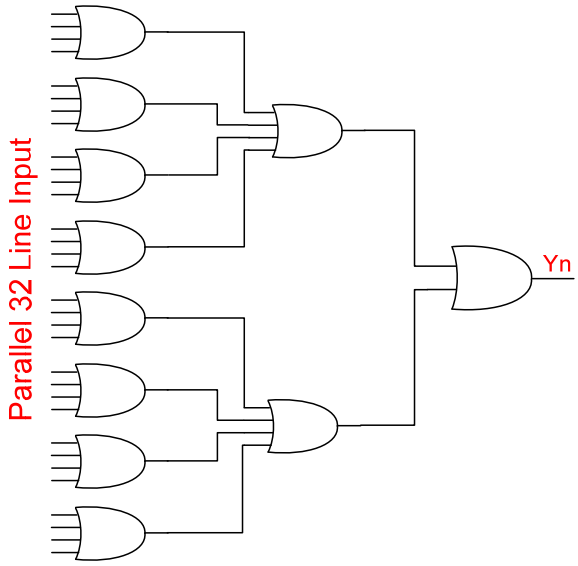

Figure 3.20 – 32-input OR gate fan-in

data lines. Therefore a 32-input OR gate is implemented. Due to the limited input size of the logic gates provided in the OSU standard cell library, a fan-in technique is used. This logic realization is then repeated 5 more times resulting in six 32-input OR gates.

To correctly encode a parallel 64-channel output, each 32-input slice is to have the correct sequence. The sequence changes from least significant bit to the most significant bit (*Y0 – Y5*). The corresponding sequence for each is as follows:

$$
\begin{aligned}
Y0 = {} & w1 + w3 + w5 + w7 + w9 + w11 + w13 + w15 + w17 + \\
& w19 + w21 + w23 + w25 + w27 + w29 + w31 + w33 + \\
& w35 + w37 + w39 + w41 + w43 + w45 + w47 + w49 + \\
& w51 + w53 + w55 + w57 + w59 + w61 + w63 \\
Y1 = {} & w2 + w3 + w6 + w7 + w10 + w11 + w14 + w15 + w18 + \\
& w19 + w22 + w23 + w26 + w27 + w30 + w31 + w34 + \\
& w35 + w38 + w39 + w42 + w43 + w46 + w47 + w50 + \\
& w51 + w54 + w55 + w58 + w59 + w62 + w63 \\
Y2 = {} & w4 + w5 + w6 + w7 + w12 + w13 + w14 + w15 + w20 + \\
& w21 + w22 + w23 + w28 + w29 + w30 + w31 + w36 + \\
& w37 + w38 + w39 + w44 + w45 + w46 + w47 + w52 + \\
& w53 + w54 + w55 + w60 + w61 + w62 + w63 \\
Y3 = {} & w8 + w9 + w10 + w11 + w12 + w13 + w14 + w15 + w24 + \\
& w25 + w26 + w27 + w28 + w29 + w30 + w31 + w40 + \\
& w41 + w42 + w43 + w44 + w45 + w46 + w47 + w56 + \\
& w57 + w58 + w59 + w60 + w61 + w62 + w63 \\
Y4 = {} & w16 + w17 + w18 + w19 + w20 + w21 + w22 + w23 + w24 + \\
& w25 + w26 + w27 + w28 + w29 + w30 + w31 + w48 + \\
& w49 + w50 + w51 + w52 + w53 + w54 + w55 + w56 + \\
& w57 + w58 + w59 + w60 + w61 + w62 + w63 \\
Y5 = {} & w32 + w33 + w34 + w35 + w36 + w37 + w38 + w39 + w40 + \\
& w41 + w42 + w43 + w44 + w45 + w46 + w47 + w48 + \\
& w49 + w50 + w51 + w52 + w53 + w54 + w55 + w56 + \\
& w57 + w58 + w59 + w60 + w61 + w62 + w63
\end{aligned}
\qquad \textbf{(3.11)}
$$

3.5 Valid Data Flag

The valid data flag is the ASIC's part of the designed "handshake" protocol with the ROC. This flag will present a logic '1' when data is ready for the ROC to read. Having this flag shows its importance when channel 0 undergoes a neutron event since all 6 bits of the binary encoder will be a logic '0.' This state also exists when the ASIC is in a steady state waiting for a neutron event to occur. Without the aid of a valid data flag, two states will exist for a binary '000000' output.

To derive the circuitry for the valid data flag, it is apparently understood that any bit of the binary encoder (*Y0-Y5*) will be tripped if Channel 1 – Channel 63 undergoes a neutron event. However, the valid data flag must also include an event at Channel 0 so that the ROC can decipher between the two valid '000000' states. Recalling that the priority encoder will output a logic '1' at *EP0* when Channel 0 undergoes an event, allows for the use of *EP0* in the valid data circuitry. Consequently, all that is needed is a 7-input OR gate that evaluates *EP0* from the priority encoder and *Y0 – Y5* from the binary encoder. The circuitry is shown in Figure 3.21.

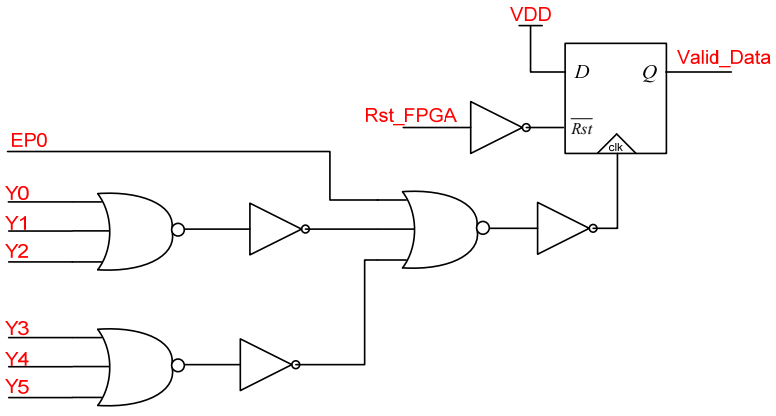

Figure 3.21 – Valid data flag circuitry along with output registering

3.6 Low Voltage Differential Signaling Driver and Receiver

Low voltage differential Signaling (LVDS) is a low swing, current-mode, differential signal standard [20]. Its qualities are ideal for noise suppression on any transmission line. This standard is ideal for the *Patara III* ASIC due to noise sensitivities. Two on-chip LVDS receivers were developed for the system clock, and the system reset provided by the ROC. In addition, seven on-chip LVDS drivers were developed for the channel ID (*Y0 – Y5*) and the valid data flag. Before discussing the topology of the driver and receiver, the LVDS standard will be discussed and outlined.

3.6.1 The LVDS Standard [20]

Figure 3.22 illustrates a typical point-to-point interface with an LVDS driver and receiver. LVDS standard outputs consist of a current source (nominally 3.5-mA) that drives a differential pair line. An LVDS receiver is designed to have high input impedance, so the majority of driver current flows across a 100Ω differential termination resistor generating ideally 350-mV across the receiver inputs. When the driver switches, it changes the direction of current flow across the resistor, thereby creating a valid "1" or "0" logic state. This signal swing occurs at a nominal common mode voltage of 1.25-V

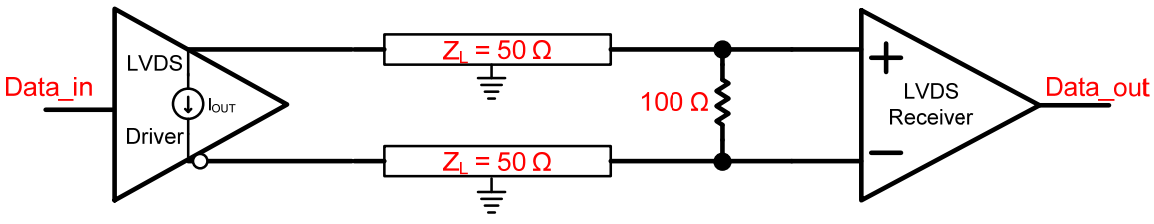

Figure 3.22 – LVDS point-to-point interface with transmission lines and termination impedance

Table 3.2 – ANSI/TIA/EIA-644-A standards for LVDS transmission [20]

Parameter	Description	Min.	Max.	Units
Vod	Differential output voltage	247	454	mV
Vos	Offset voltage	1.25	1.375	V
Vod	|Change to Vod|		50	|mV|
Vos	|Change to Vos|		50	|mV|
Isa, Isb	Short circuit current		24	|mV|
tr/tf	Output rise/fall times (200 Mbps)	0.26	1.5	ns
	Output rise/fall times (<200 Mbps)	0.26	30% of tui	ns
Iin	Input current		20	|μA|
Vth	Receive threshold voltage		+100	mV
Vin	Input voltage range	0	2.4	V

making a logic '1' state occur at approximately 1.425-V and a logic '0' state at 1.075-V. Table 3.2 shows the ANSI/TIA/EIA-644-A standards for LVDS transmission.

3.6.2 LVDS Driver Topology and Simulation

The developed LVDS driver utilizes a bridged-switched circuit. A bridge-switched based LVDS driver behaves as a current source with the capability of switched polarity [21]. The bias current to the bridge-switched circuit is switched through the termination resistors at the receiver according to the polarity of the data input, and thus produces the correct differential output signal swing [21]. This does require a bias current of 3.5-mA per the LVDS standard. To provide the common mode offset, a common-mode feedback (CMFB) network is added to the bridge-switched circuit. This allows for an external voltage reference to control the common mode of the output signal swing. For this work, an on-chip bandgap voltage reference (BGR) will be used to provide the 1.25-V offset. The overall LVDS driver topology is shown in Figure 3.23.

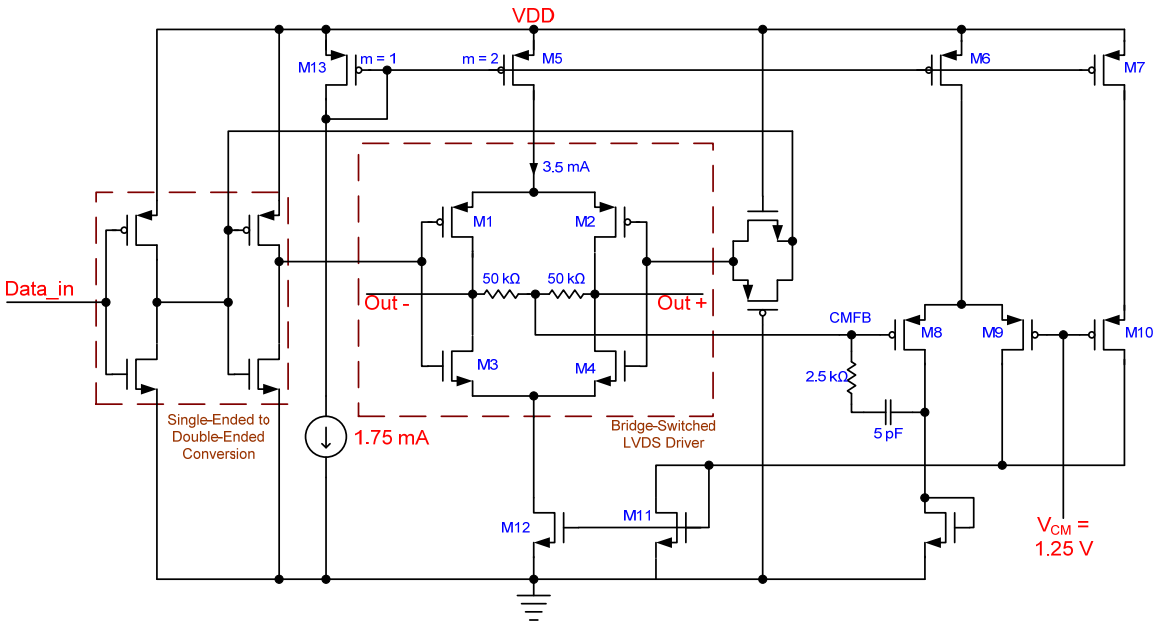

Figure 3.23 – Bridge-switched based LVDS driver

This driver accepts a 3.3-V digital signal and converts it directly to a fully differential LVDS standard signal. The single-ended data is converted to double-ended data by the cascaded inverter network shown in Figure 3.23. The bridge-switched circuitry consists of devices *M1-M4*. If switches *M1* and *M4* are on (*Data_In* = '0'), the polarity of the output current is positive with negative differential output voltage. On the contrary, if switches *M1* and *M4* are off (switches *M2* and *M3* are on), the polarity of the output current and voltage is reversed [21]. The common mode feedback (CMFB) network consists of devices *M5-M12*. Notice that the bias current to the LVDS driver is 1.75-mA rather than 3.5-mA. The only portion of the topology that is required to have a bias current of 3.5-mA is the bridge-switched circuit. Therefore, a current gain of 2 is provided between devices *M5* and *M13* providing 3.5-mA of bias current.

LVDS transmitters are primarily tested at higher data rates due to their general scope of applications. With this ASIC, the output data rates will saturate at the expected input pulse-pair resolution. The expected pulse-pair resolution is 10 µsec resulting in an expected data rate of 100 kbps (kilo-bits-per-second). The simulation was performed at 10 Mbps to ensure that this transmitter would function as expected. The eye diagram of the LVDS transmitter at a data rate of 10 Mbps is shown in Figure 3.24.

3.6.3 LVDS Receiver Topology and Simulation

An LVDS receiver is basically a comparator, except it discriminates differential voltages rather than single-ended voltages. From Table 3.2, an LVDS receiver is to have a switching threshold of 100-mV differential. This implies that when the positive input

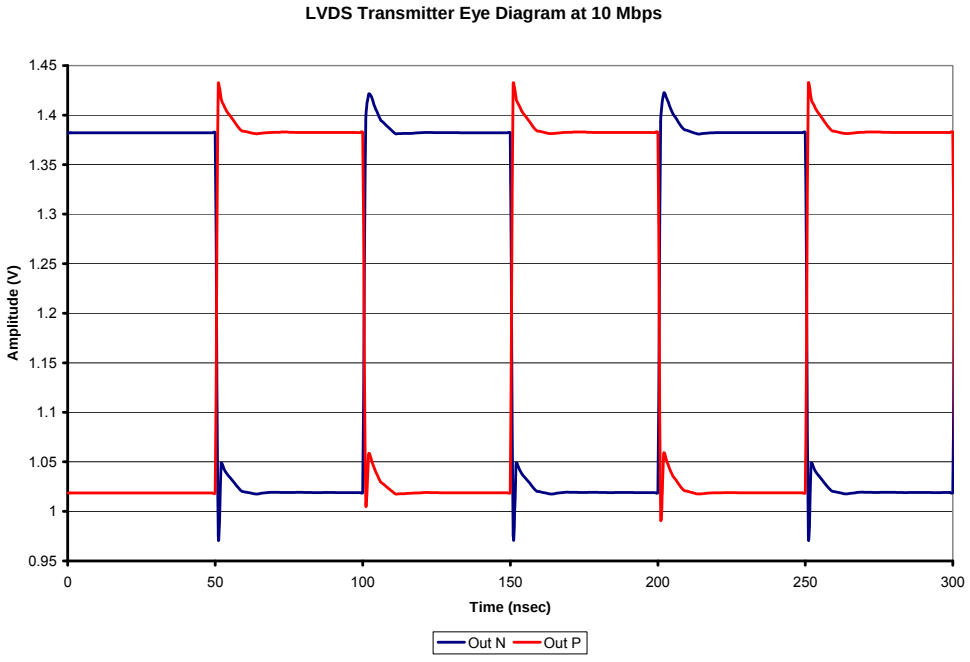

Figure 3.24 – Simulated LVDS transmitter eye diagram at a data rate of 10 Mbps

and negative input have a difference in potential greater than 100-mV, the receiver is to trip high or low (depending on the polarity of the difference). Since this receiver will not be operating at high data rates, the accompanying specifications are tailored to this application on this ASIC and not for general use. The developed LVDS receiver is shown in Figure 3.25.

Simulation results shows that when the output is approximately 90% of a logic '1' (2.97-V for 3.3-V logic), the differential input voltage is 99-mV. Also, the rise time of the LVDS receiver output with a 10 MHz clock input and a 10 pF load was 2.9 nsec. Figure 3.27 shows the simulation results for the transfer characteristic, and Figure 3.26 illustrates the output characteristic with a 10 MHz clock.

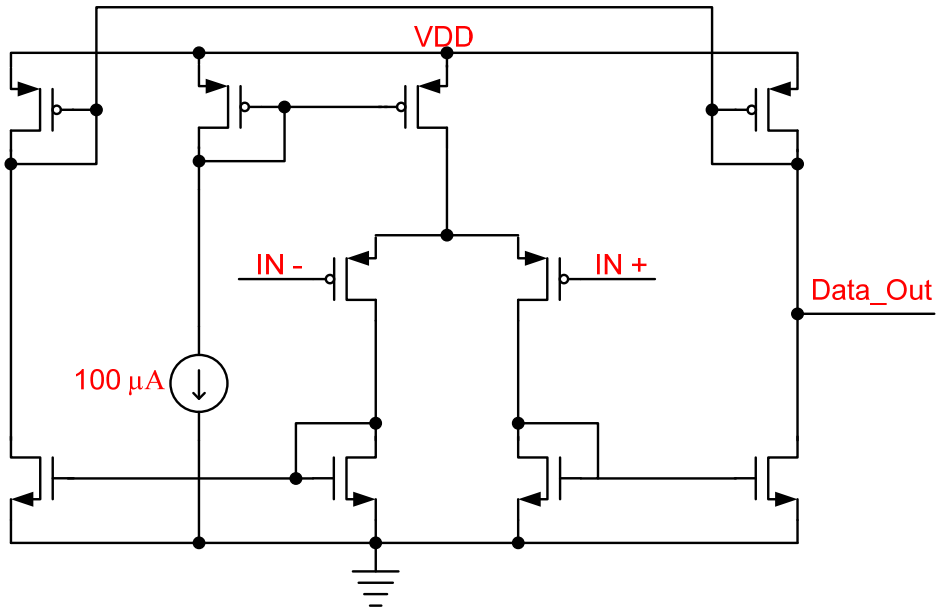

Figure 3.25 – LVDS receiver topology

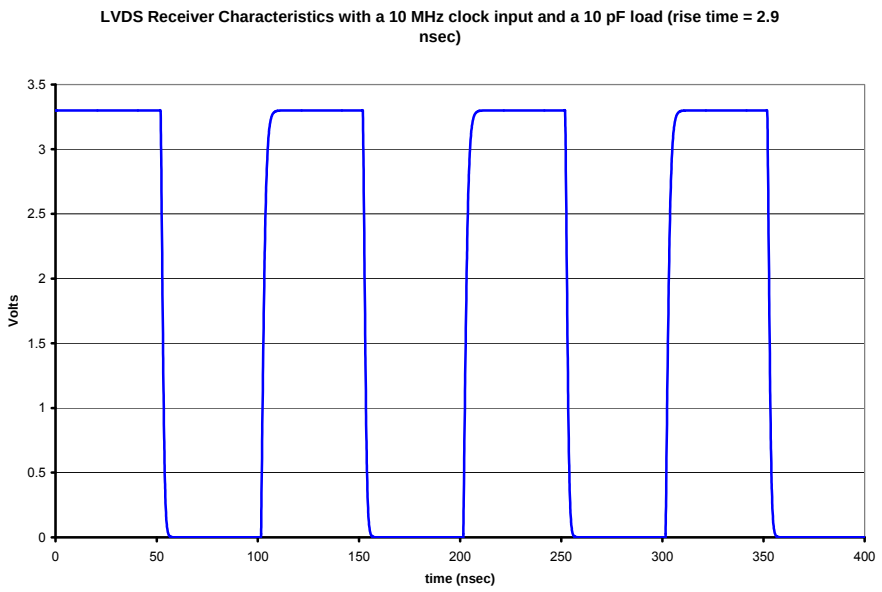

Figure 3.26 – SimulatedLVDS receiver output with a 10 MHz clock input and a 10 pF load

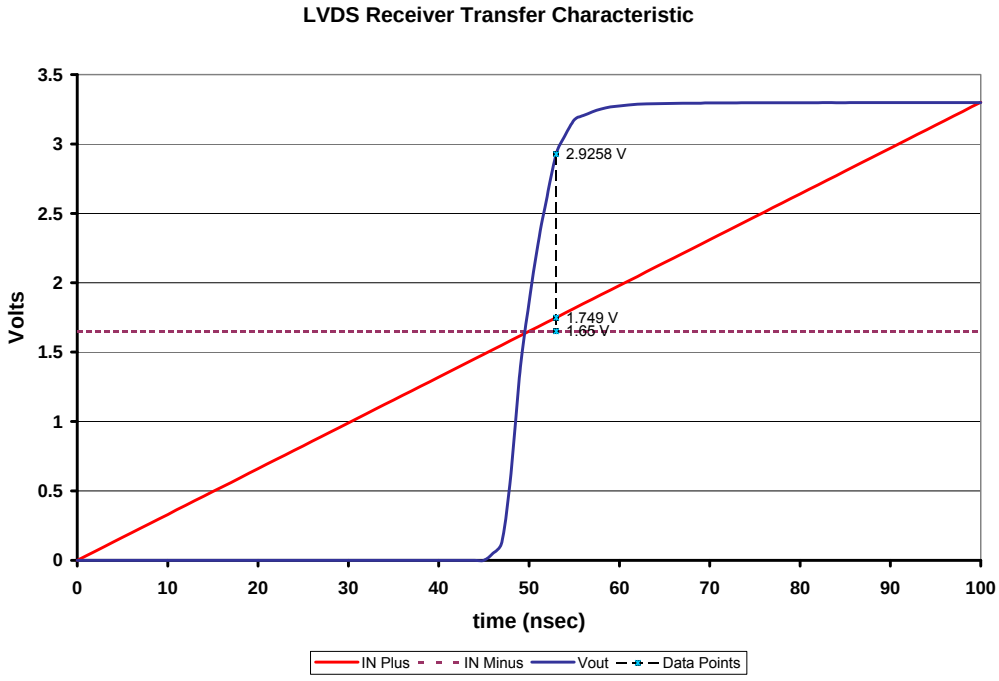

Figure 3.27 – Simulated LVDS receiver transfer characteristic illustrating differential input threshold

3.7 Enable/Disable Bandgap Reference

Two on-chip Bandgap Voltage References (BGR's) were designed for the purpose of biasing other on-chip circuits. The advantage of a BGR is that it is generally a very stable voltage reference and can be very robust. One use of the BGR in this application is to bias the common-mode voltage level of the LVDS transmitter. The other is to bias the DAC's LSB current. Having a steady voltage reference for these two applications is crucial to an accurate design of these circuits.

The basic idea of the BGR is to combine the complimentary to absolute temperature (CTAT) behavior of the bandgap energy of silicon (a diode's forward voltage drop) with the proportional to absolute temperature (PTAT) behavior of the thermal voltage ($V_T = kT/q$) to form a voltage reference that varies little with temperature [22]. The two steps listed above can be translated to electronics by first generating a thermal voltage referenced current and sourcing it into a diode. To convert the current into a voltage and zero out the temperature coefficient (temp. co.), a resister is added above the diode. This resistor above the diode is scaled up by a factor L with respect to the resistor in the thermal voltage current reference. This scaling is necessary due to the fact that the silicon energy bandgap temp. co. ($TV_{EG} = -1.6$ mV/°C) is greater than the thermal voltage temp. co. ($TV_T = 0.085$ mV/°C) [22]. Schematic details of this will be provided later.

3.7.1 BGR Fundamentals

In Silicon, the bandgap energy as a function of temperature is given by [22],

$$E_g = 1.16 - \left(702 \times 10^{-6}\right) \cdot \frac{T^2}{T + 1108} (eV), \qquad \textbf{(3.12)}$$

where T is absolute temperature. Notice that this equation verifies that the bandgap energy decreases with increasing temperature. If a diode is biased by a constant current source and the temperature is increased, the barrier height between the *n* and *p* sides of the diode is decreased and thus so does the diode's voltage drop (V_D). This creates the CTAT behavior utilized in a BGR.

To generate the PTAT current source, a thermal voltage ($V_T = kT/q$) referenced self-biasing topology is used. In this design, a cascode wide-swing current mirror amplifier is used to hold the source terminals of devices *M1* and *M2* at the same potential. The thermal voltage referenced (PTAT) current source is illustrated in Figure 3.28. To derive an expression for the PTAT current reference, the first-order diode equation must

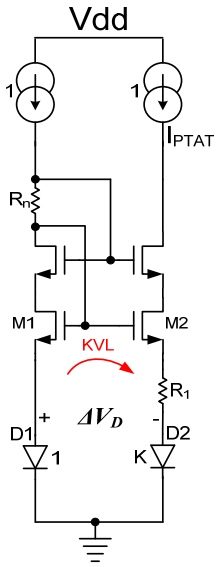

Figure 3.28 – Thermal voltage current reference

be understood:

$$V_{D1} = V_T \cdot \ln\left(\frac{I_{PTAT}}{I_S}\right). \quad \textbf{(3.13)}$$

Applying Kirchhoff's Voltage Law (KVL) around the loop show in Figure 3.28, and assuming devices *M1* and *M2* are ideally matched,

$$V_{D1} = V_{D2} + I_{PTAT} \cdot R_1 . \quad \textbf{(3.14)}$$

With the anode of diode *D2* scaled by the factor *K*,

$$V_{D2} = V_T \cdot \ln\left(\frac{I_{PTAT}}{K \cdot I_S}\right). \quad \textbf{(3.15)}$$

Substituting equations (3.15) and (3.13) into (3.14) leads to the following expression for the PTAT current reference,

$$I_{PTAT} = \frac{V_T \cdot \ln(K)}{R_1}. \quad \textbf{(3.16)}$$

An expression for the temperature coefficient may now be derived since the PTAT current source is readily dictated with a few design choices. The PTAT current reference will be directly sourced into a resistor and diode in series as shown in Figure 3.29. Therefore, the reference voltage can be written as,

$$V_{REF} = V_{D3} + x \cdot I_{PTAT} \cdot L \cdot R_1 . \quad \textbf{(3.17)}$$

Substituting the expression for the PTAT current reference (3.16) into equation (3.17),

$$V_{REF} = V_{D3} + x \cdot L \cdot \ln(K) \cdot V_T , \quad \textbf{(3.18)}$$

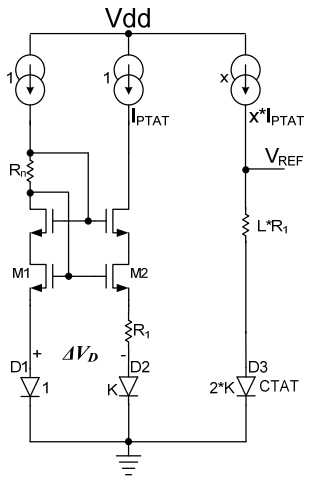

Figure 3.29 – Basic BGR topology

The temperature variation of the reference voltage is shown to be [22]

$$\frac{\partial V_{REF}}{\partial T} = \frac{\overbrace{\partial V_{D3}}^{-1.6\,mV/C}}{\partial T} + x \cdot L \cdot \ln(K) \cdot \frac{\overbrace{\partial V_T}^{-0.085\,mV/C}}{\partial T}. \qquad \textbf{(3.19)}$$

Setting equation (3.19) to zero and solving for the scaling factor L yields

$$L = \frac{1.6}{x \cdot \ln(K) \cdot 0.085}. \qquad \textbf{(3.20)}$$

The scaling factor, L, gives the designer control over where the zero temperature coefficient occurs (e.g., room temperature). To minimize this factor so that global variation between the two resistors (R_1 and $L*R_1$) is reduced, the current gain x is applied.

3.7.2 BGR Topology and Simulation

To fully implement the BGR, a wide-swing cascode PMOS current mirror is introduced to mirror the PTAT current to the output branch. This technique is used to preserve headroom and increase power supply rejection (PSR). In addition, a startup

circuit is used to sense the output for a 0-V state and bring the BGR back to normal operation. The startup circuit injects current at the high impedance node located between the NMOS and PMOS current mirrors within the thermal voltage referenced current generation circuit and turns itself off when normal operation occurs. The startup circuit is needed due to a zero current state that can exist in a self-biased reference resulting in zero voltage output. The developed BGR topology is shown in Figure 3.30.

Verifying the temperature performance and the PSR is of key interests when simulating. Desirable specifications of a BGR are generally to have temperature coefficients of less than 80 ppm over the operating temperature range and a PSR of more than 50 dB. The simulations verified that a temperature coefficient of −1.25 ppm at 25 °C and a PSR of 57 dB are achieved. Figure 3.31 and Figure 3.32 illustrate these results.

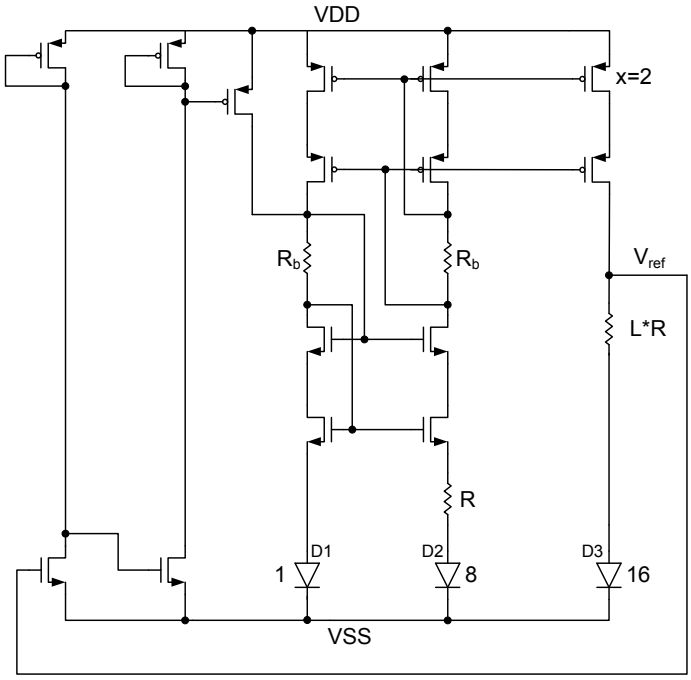

Figure 3.30 – On chip bandgap voltage reference

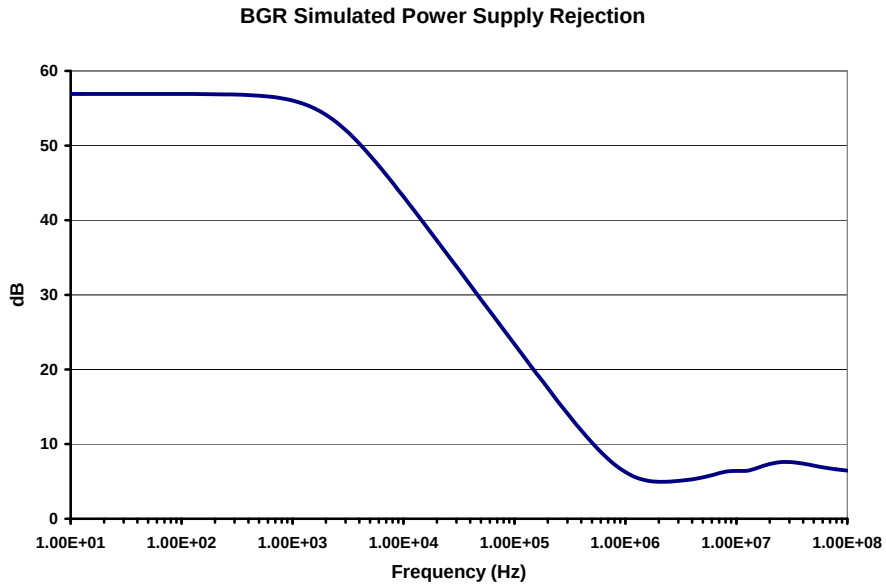

Figure 3.31 – BGR simulated PSR

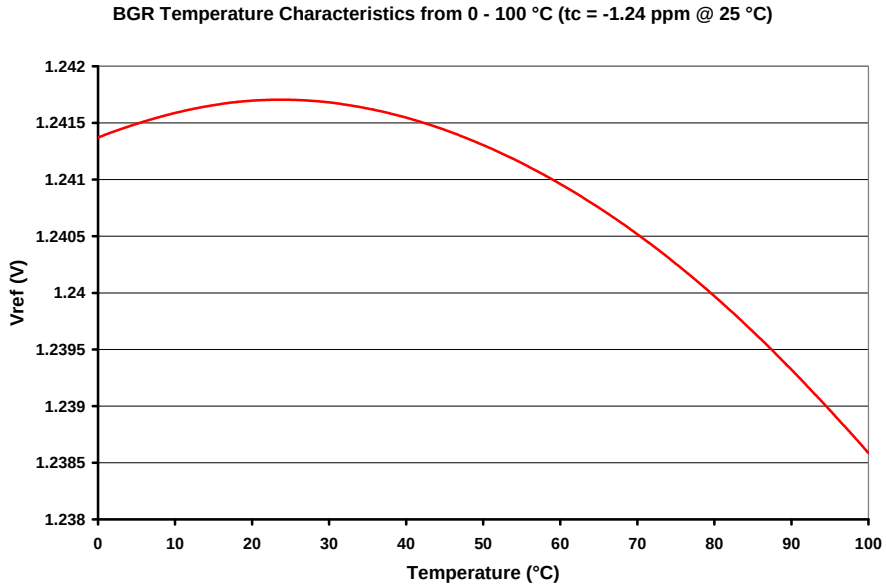

Figure 3.32 – BGR simulated temperature characteristic

3.7.3 BGR Programmability and Output Buffering

It is desired in this system to have the ability to turn the BGR on and off while the overall ASIC is powered on. To do so, a programmable master power supply switch is implemented. This switch must provide the user with a control line that can enable a clean power supply connection and have a low leakage off state. The circuitry used consisted of an inverter in series with a PMOS switch. This PMOS switch is sized to have a large aspect ratio to ensure a low impedance on state and a high impedance off state. The programmable switch along with the BGR is shown in Figure 3.33.

A bandgap voltage reference is a very robust circuit for on-chip biasing. However, the BGR has poor drive capability. Therefore, loading conditions could ultimately affect the performance of the reference. The poor drive capability stems from

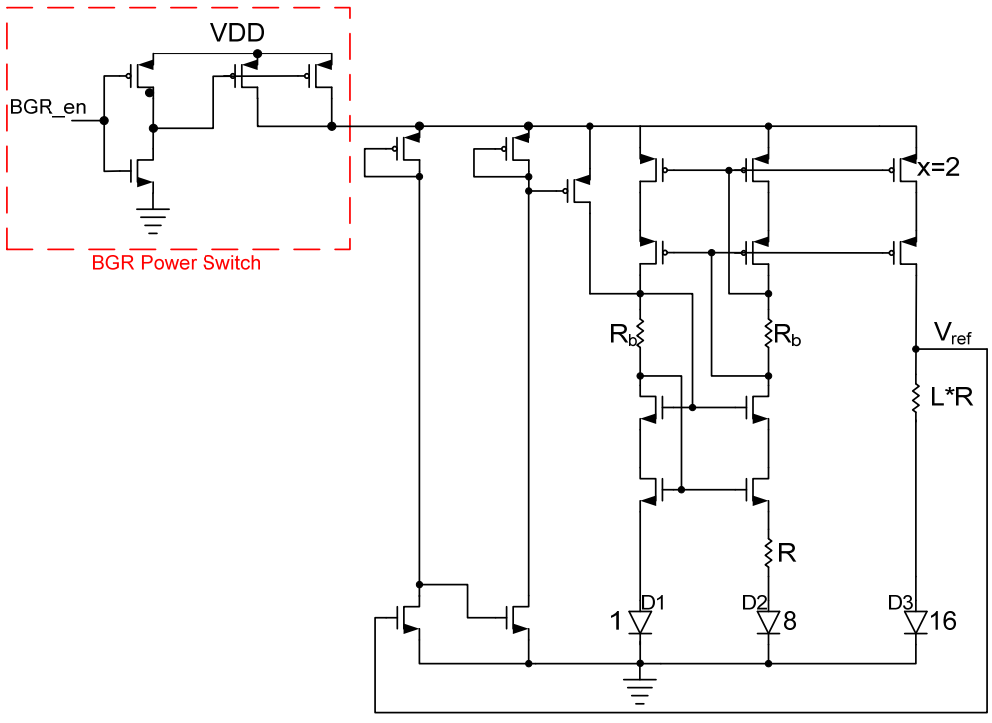

Figure 3.33 – Bandgap reference with programmable switch

the fact that the output impedance looking into V_{ref} is large. Buffering the output would provide a low output impedance and good drive capability.

A good voltage buffer for this application is an op amp in a non-inverting unity gain configuration. A non-inverting unity gain configuration takes advantage of maximum loop transmission in the negative feedback network. Therefore, an op amp with a large open-loop gain (A_{OL}) will have very low output impedance due to the benefits of negative feedback. This will ultimately result in a robust voltage reference with enhanced drive capability. Figure 3.34 illustrates the use of the voltage buffer in the developed BGR and Figure 3.35 provides a schematic of the op amp used for the voltage buffer.

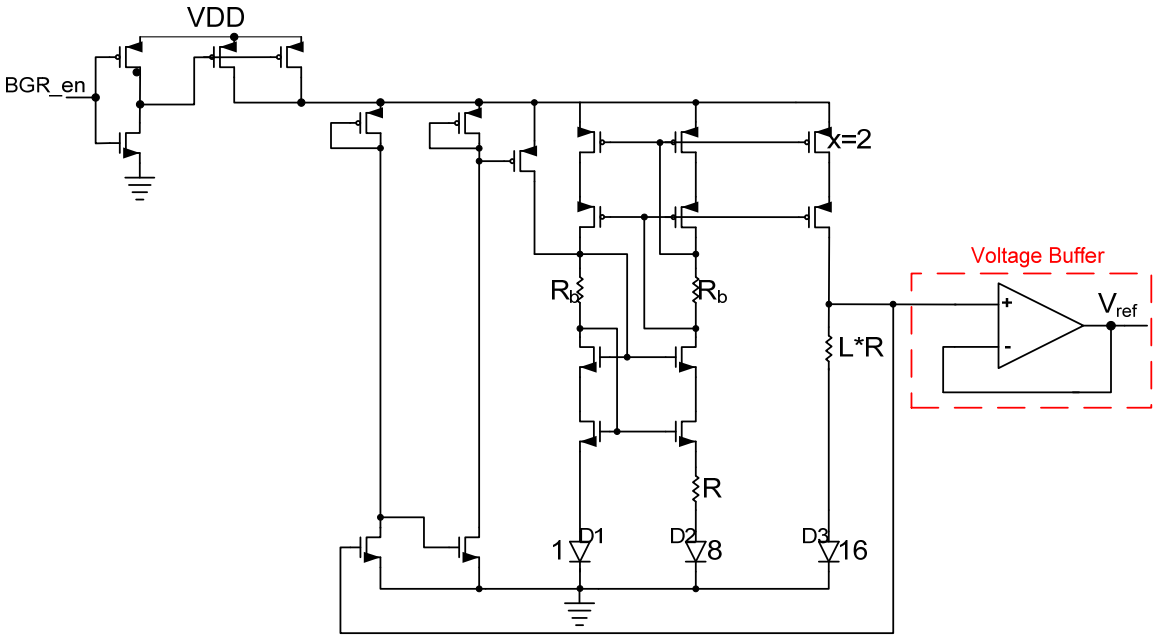

Figure 3.34 – Bandgap reference with voltage buffering

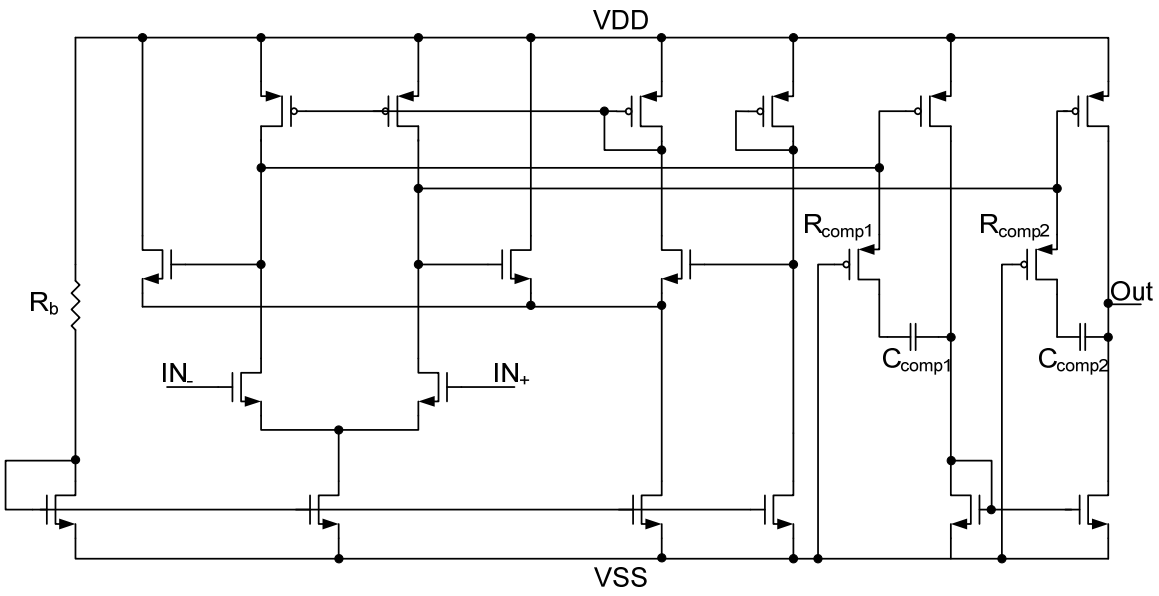

Figure 3.35 – RHIC4B op amp used for voltage buffering [23]

3.8 8-Bit Current Driven Digital to Analog Converter

To provide higher integration and functionality to the SNS system, 3 on-chip DACs were developed. Each DAC is of the same architecture, but each served different purposes. The major purpose is to provide the ROC with the ability to digitally select a discrimination threshold. The other two are used to set the baseline level of the readout electronics, and to provide a voltage reference for the built-in self-test (BIST) circuitry. The chosen topology allowed for a configurable range by selection of an external offset voltage and a programmable on-chip offset current reference. This provides a robust design for alternative voltage ranges if needed. However, the design approach was to meet a specification of 8-bits in resolution over a 600-mV to 0-V range.

3.8.1 DAC Architecture

Since the DAC is to be 8 bits in resolution, the number of input combinations will be $2^N = 256$ (where $N = 8$). To express the resolution in *least significant bits* (LSB),

$$1\,LSB = \frac{600mV}{2^N} = \frac{600mV}{256} = 2.34\,mV. \quad \textbf{(3.21)}$$

In other words, an iteration of the rightmost bit in the binary input word will result in a change of 2.34-mV at the analog output. For simplicity, a current summing DAC architecture is selected, thus 1 *LSB* must be translated to a current. The designer can dictate the value of the 1 *LSB* current so that the overall power consumption can be designated. However, the designer must hold this ratio true at the transimpedance stage of the design (current-to-voltage conversion). In this design, 1 *LSB* was set to 1-μA. Therefore the transimpedance gain at the output stage of the DAC is to be

$$\frac{V_{out}}{I_{in}} = \frac{2.34 \times 10^{-3}}{1 \times 10^{-6}} = 2.34 \times 10^{3}\ \Omega. \quad \textbf{(3.22)}$$

The DAC architecture is based on the topology shown in Figure 3.36 [24]. Here, binary weighted current sources are digitally switched and summed at the current summing node of the op amp. Ideally, the current summing node will be at the same voltage potential as V_{off}. Therefore, the analog output will be simply the offset voltage minus the current at the summing node times the feedback resistor R_F. The offset current is used to provide the ability to change the range of the DAC output. In this design, the offset current is a constant source and can be switched on or off. This results in two

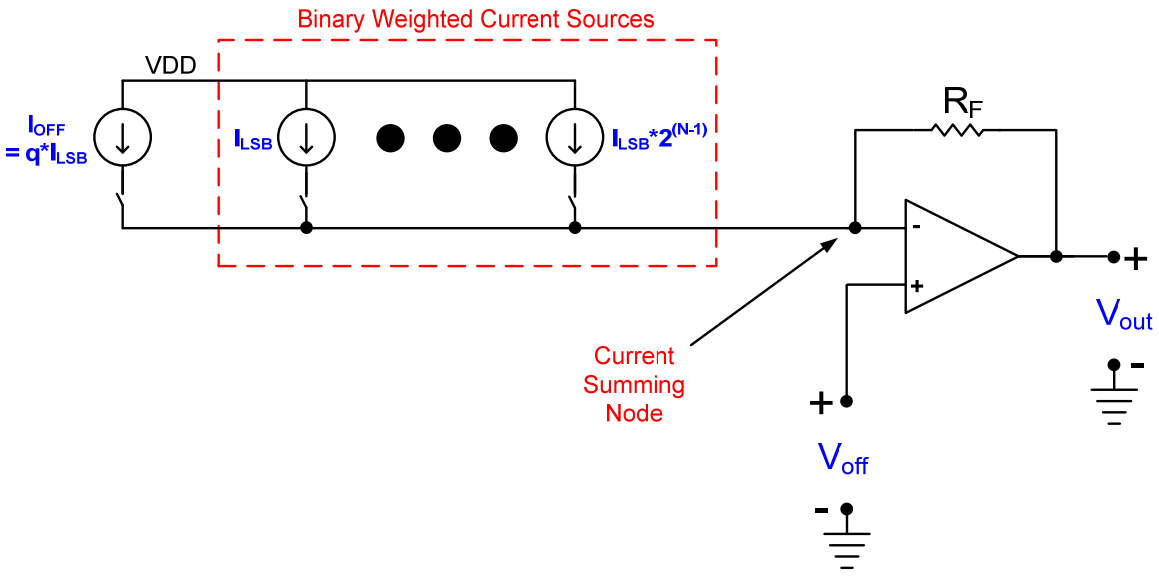

Figure 3.36 – Current driven DAC architecture overview

operating ranges if the offset voltage is fixed. The resultant transfer function is then given by

$$V_{out} = V_{off} - R_F \cdot I_{LSB}(m+q)$$
$$where, \quad 0 \le m \le (2^N - 1). \qquad \textbf{(3.23)}$$

The term q is the scaling factor for the offset current with respect to I_{LSB}, and N is the resolution of the DAC in bits.

To generate the 1 *LSB* current, the developed bandgap voltage reference output will be set across a bias resistor R_{bias}. This current reference will then bias a binary weighted current mirror bank to generate the binary weighted current sources in the DAC. Since the current mirror bank will be scaled from 2^1 through $2^{(8-1)}$ of the 1 *LSB* current, a design decision was made to have the 1 *LSB* current reference to be scaled by 16 (2^4). This will reduce systematic gain error in the binary weighted current mirror

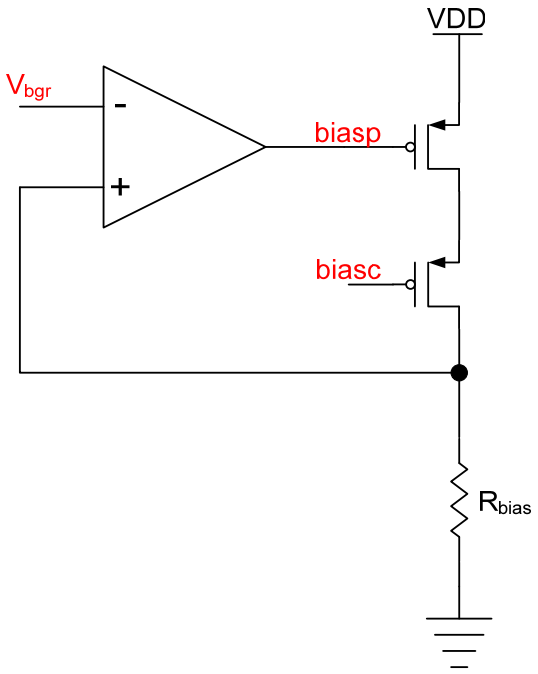

Figure 3.37 – 16x LSB bias circuit for the binary weighted current mirror bank

bank. The 16× *LSB* bias circuit for the binary weighted current mirrors is shown in Figure 3.37. The 1 *LSB* current can then be written as

$$I_{LSB} = \frac{V_{bgr}}{16 \cdot R_{bias}}. \tag{3.24}$$

Plugging equation 3.24 into 3.23 the DAC transfer function then becomes,

$$V_{out} = V_{off} - V_{bgr} \cdot \frac{(m+q)}{16} \cdot \left(\frac{R_F}{R_{bias}} \right). \tag{3.25}$$

Notice the resistor ratio in the transfer function. This ratiometric relationship compensates for any absolute resistance value changes introduced during fabrication [24]. If careful monolithic construction is engineered, the resistor values will track to ±2% [24].

Since a DAC transfer function is ideally linear, two important parameters can be derived from equation 3.25 by simply expressing it in slope-intercept form. The slope of the DAC is written as

$$slope = -\frac{V_{bgr} \cdot R_F}{16 \cdot R_{bias}}, \tag{3.26}$$

and the y-intercept is expressed as

$$y - \text{int.} = V_{off} - q\left(\frac{V_{bgr} \cdot R_F}{16 \cdot R_{bias}}\right). \tag{3.27}$$

From the above expressions, the slope of the DACs transfer curve is dictated by the ratio of R_F / R_{bias}, and the range of the DAC (y-intercept) is dictated by V_{off} and the offset current scalar q.

From Figure 3.36, the transimpedance conversion begins at the current summing node of the op amp. Recall from equation (3.22) that the transimpedance gain is to be 2.3529×10^3 Ω. From the topology of the DAC, R_F determines the transimpedance gain and is chosen to be 2.35 kΩ. Using equation (3.24) and a 1 *LSB* current value of 1 μA, R_{bias} is sized to 78.13 kΩ. Since the DAC is chosen to operate from 600-mV to 0-V, the y-intercept of the transfer function is 0.6-V. From equation (3.27), there are two variables left to be defined. At this point a design decision must be made. Setting V_{off} to 1.25-V (a BGR reference) for simplicity, the result for q is then 276. This implies that the aspect ratio for the offset current source is to be 276 times the 1 *LSB* device. Not only will this result in poor current matching, but it will require a substantial amount of chip

area and consume more power. However, setting V_{off} to 1-V results in a q scalar of 170—a reasonable design compromise.

With the design in Figure 3.37, the bias values (*baisp* and *biasc*) will be distributed to the binary weighted current mirrors in the DAC. The bias voltage *biasp* will be used to bias the current mirror device while *biasc* will bias the cascode device. The use of a cascode device will allow for better current matching among the binary weighted current mirror bank due to an increased output resistance of the current sources. Since the operating bias value for *biasc* is about 1.4-V, a BGR reference is used instead of any active biasing for simplicity. A detailed topology of the current driven DAC without the 16× *LSB* bias circuit is shown in Figure 3.38. It should be noted that the digital switches, *b0 – b7* are to be binary weighted with respect to their aspect ratios in the same fashion as the current mirror bank. If not binary scaled, the switch will not properly shunt the cascode device and it will not effectively disable the current source.

3.8.2 Simulation Results

The derived transfer function was simulated in Matlab to verify the output characteristics. A comparison of the theoretical Matlab transfer characteristics and the post layout simulated results are show in Figure 3.39. Notice the upward sloping towards the 0-V setting (decimal 256). This is ultimately due to the op amp used in the transimpedance stage. The output stage of the op amp is not ground-sensing capable, leaving it approximately one V_{dsat} (~50-mV) above ground. This was acceptable for this application since the DAC will not need to operate at voltages very near ground.

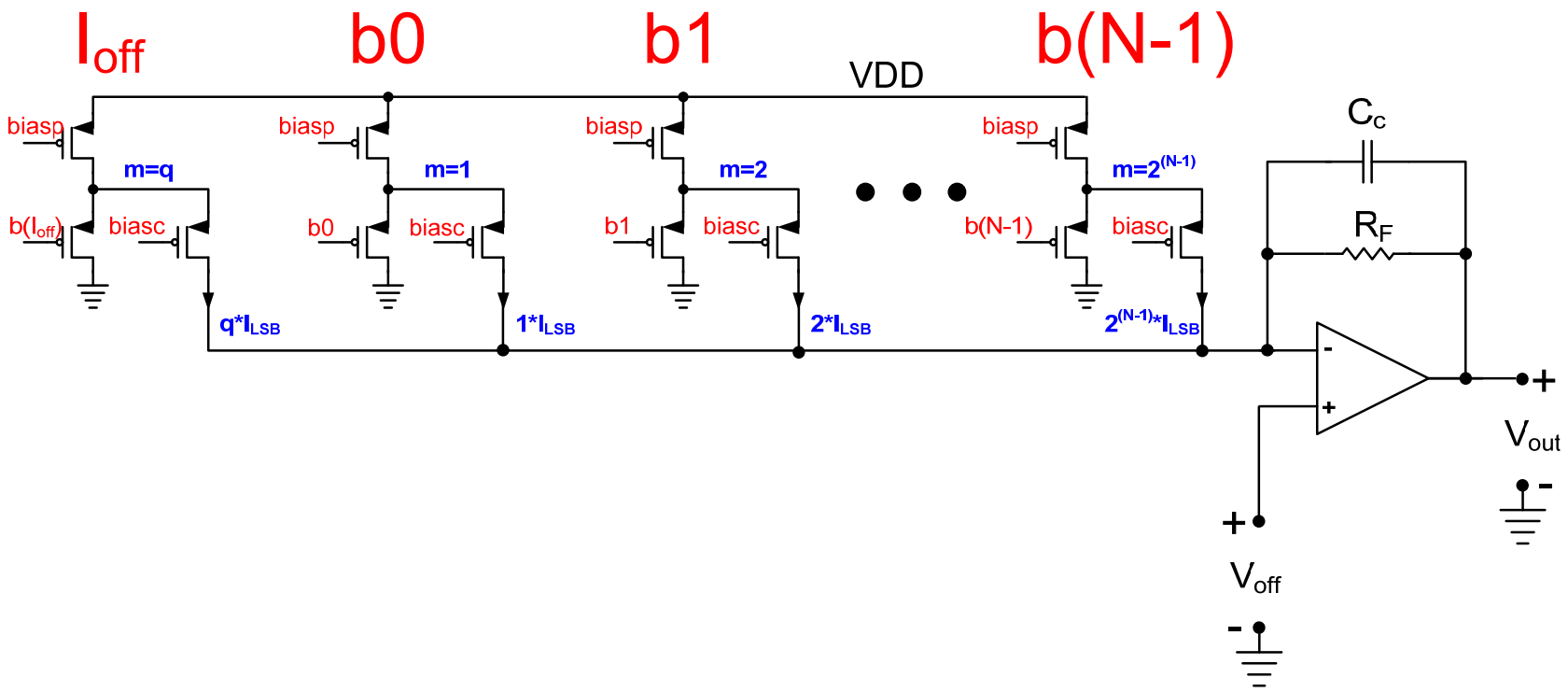

Figure 3.38 – Current driven DAC architecture without 16× *LSB* bias circuit

To examine the non idealities of a developed DAC, a specification known as *differential nonlinearity*, or DNL is calculated. DNL is defined as the difference between ideal and the actual increment value (1 *LSB*). Mathematically it is defined as

$$DNL_N = 1\,LSB - \frac{Actual\ Increment\ N}{1\,LSB}. \qquad \textbf{(3.28)}$$

The actual increment heights are labeled with respect to the ideal increment height, which is 1 *LSB* (2.34-mV for this DAC). Generally, a DAC will have less than ±1/2 *LSB* of DNL if it is to be *N*-bit accurate [22]. If the DNL magnitude for a DAC is greater than 1 *LSB*, then the DAC is said to be *nonmonotonic*, which means that the analog output voltage does not always increase/decrease as the digital input code is incremented [22]. The DNL plot in Figure 3.40 illustrates the DAC's DNL over the full output range of 600-mV to 0-V. The DAC sacrifices DNL at the lower range, but does stay *monotonic*.

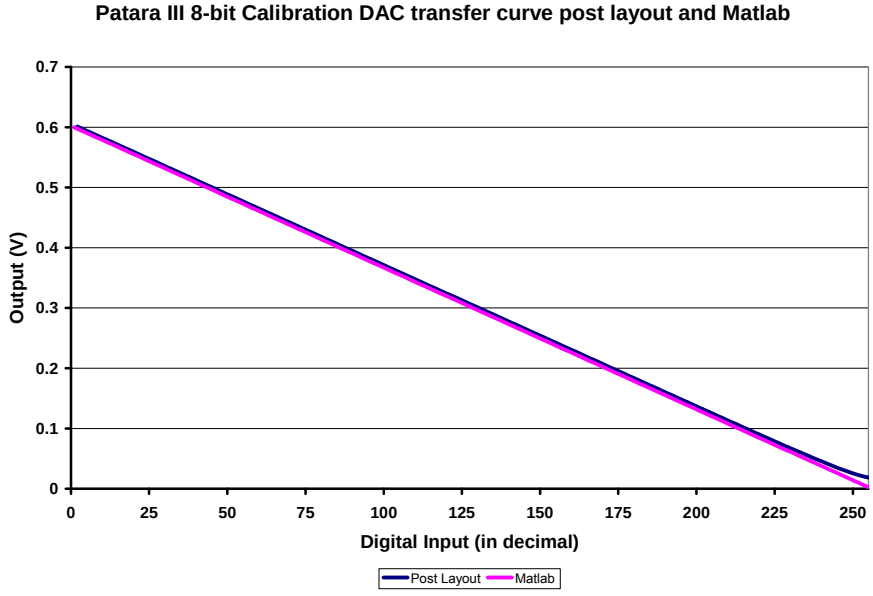

Figure 3.39 – Simulated 8-bit DAC transfer curve post layout and Matlab curve

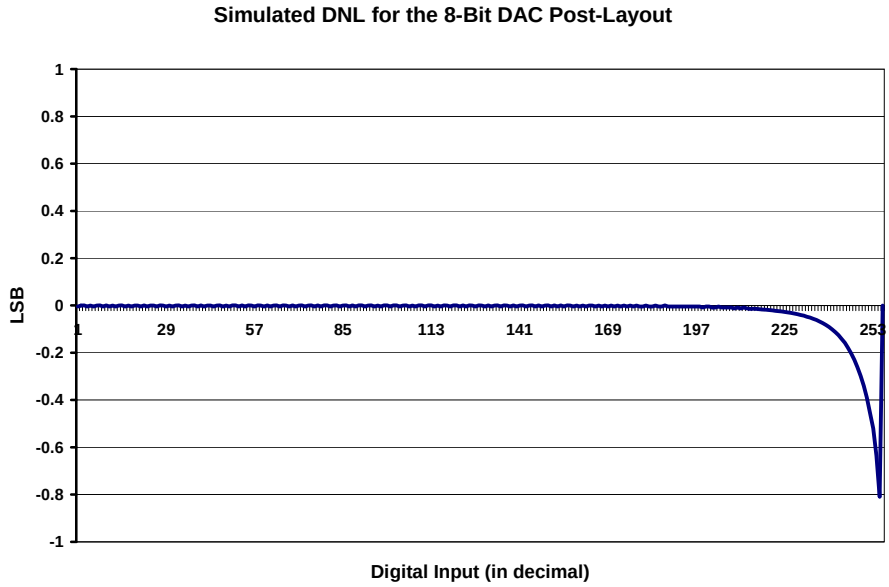

Figure 3.40 – Simulated 8-bit DAC DNL plot

3.9 99-Bit Serial Shift Register and Test Mode Circuitry

Due to the high integration and digital circuitry in this ASIC, a serial interface is used to reduce the amount of parallel I/O needed for system programming. For instance, each DAC is to be sent an 8-bit word along with a 1-bit control line for the offset current. This totals 27 parallel digital lines just to program the DACs alone. The serial interface implemented consists of a daisy-chained shift register with a non-destructive read-back line. The read-back mode is simply a mirrored register so that the serial line can be checked for programming errors. A two port multiplexer is used to select between system program mode and read-back mode. Figure 3.41 illustrates a 1-bit cell for the serial shift register. To make up the serial chain for multiple bits, the *Data_out* port is connected to the *Data_in* port of the next bit. With this configuration, the serial chain is

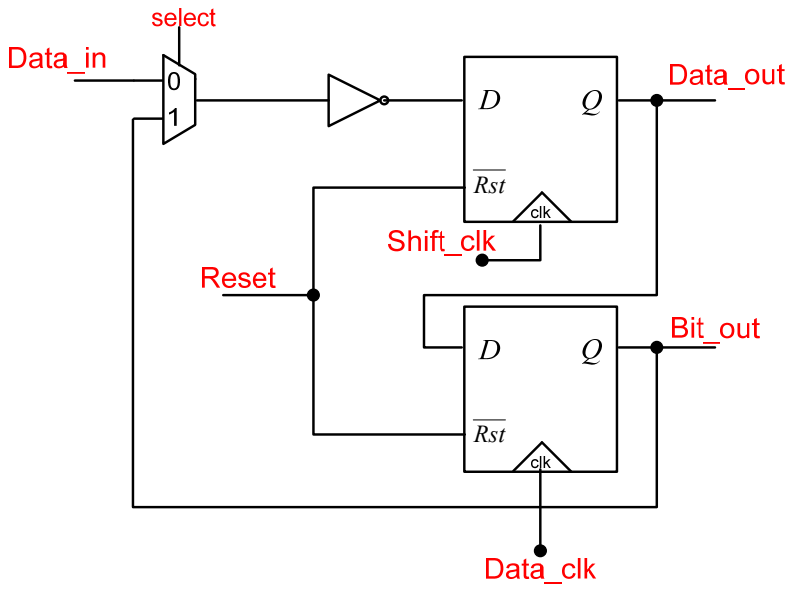

Figure 3.41 – Serial shift register 1-bit cell

configured as a first-in-first-out (FIFO) memory cell. For more detailed information regarding interfacing the serial data line, see APPENDIX A.

Since this ASIC will be integrating 64 total readout channels, it is necessary to provide an monolithic testing mode so that each fabricated chip can be verified for overall functionality and yield. To do so, a charge must be provided to the input of each channel in a non-destructive manner. This was performed by integrating a bank of 100 fF capacitors with a voltage DAC bussed across the bank. The shift register will select the desired channel to be tested by switching an ohmic connection with a single capacitor and discharging it into the input of the CSPA. The charge will be equal to the DAC voltage output times 100 fF. This circuitry is connected to the serial data string so that the BIST mode can be digitally selected. The schematic for the BIST cell is shown in Figure 3.42. See APPENDIX A for more detail on how to operate the BIST.

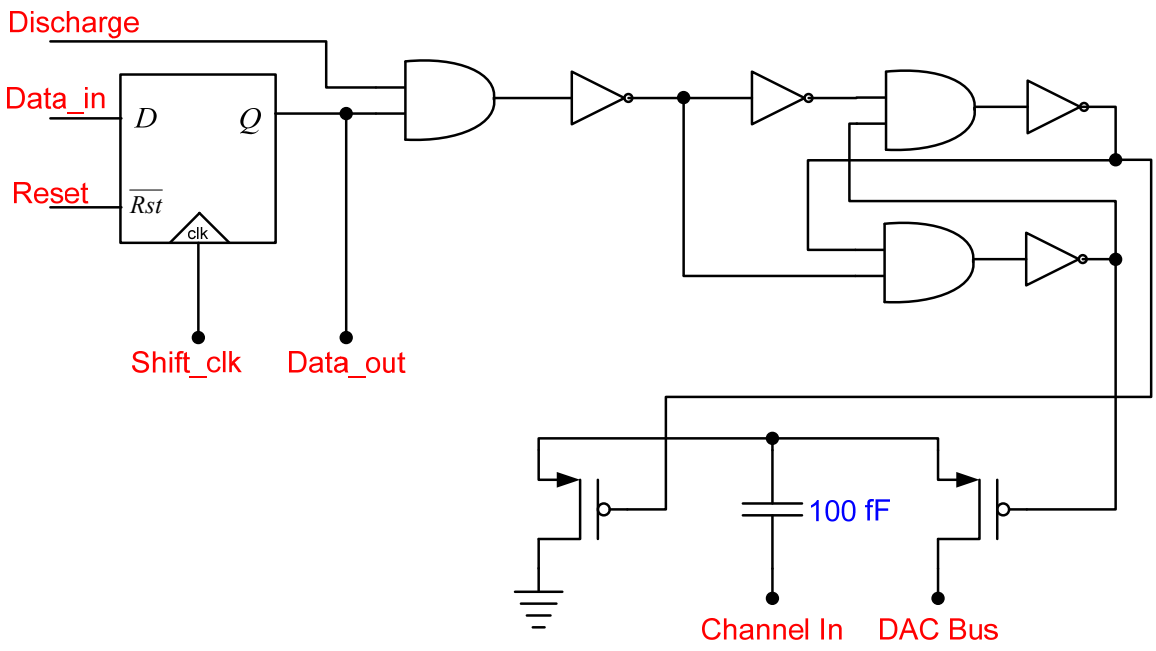

Figure 3.42 – Built in self test circuitry cell with serial register

3.10 System Simulation Results

To verify the system at the top level of the design, an analog simulation environment was used. The tool of choice was HSPICE. Due to the complexity of the system and the amount of digital circuitry, many techniques were used to enable the simulator to converge at an operating point. Since the environment is dedicated to analog, the digital I/O was verified in parallel bits. This makes illustration of the results complicated and non-intuitive. To illustrate simulation results, Figure 3.43 provides the outputs of major signals in the processing chain. Plots (c) through (h) in Figure 3.43 represents a neutron occurrence on channel 0 of the 64-channel core. Plots (a) and (b) in Figure 3.43 illustrate the handshake protocol of the digital system where plot (b) is the valid data flag and plot (a) is the reset provided by the ROC. With the simulated hit at channel 0, the 6-bit parallel channel ID lines from the binary encoder are all at a logic '0.' Therefore, these data bits were not shown. The HSPICE simulations verified the overall functionality of the ASIC, from the serial programming to the event channel ID digital output of the LVDS formatted binary encoder. The contents of Chapter 4 will contrast the pre-fabrication simulation results with the test bench results from the physical ASIC.

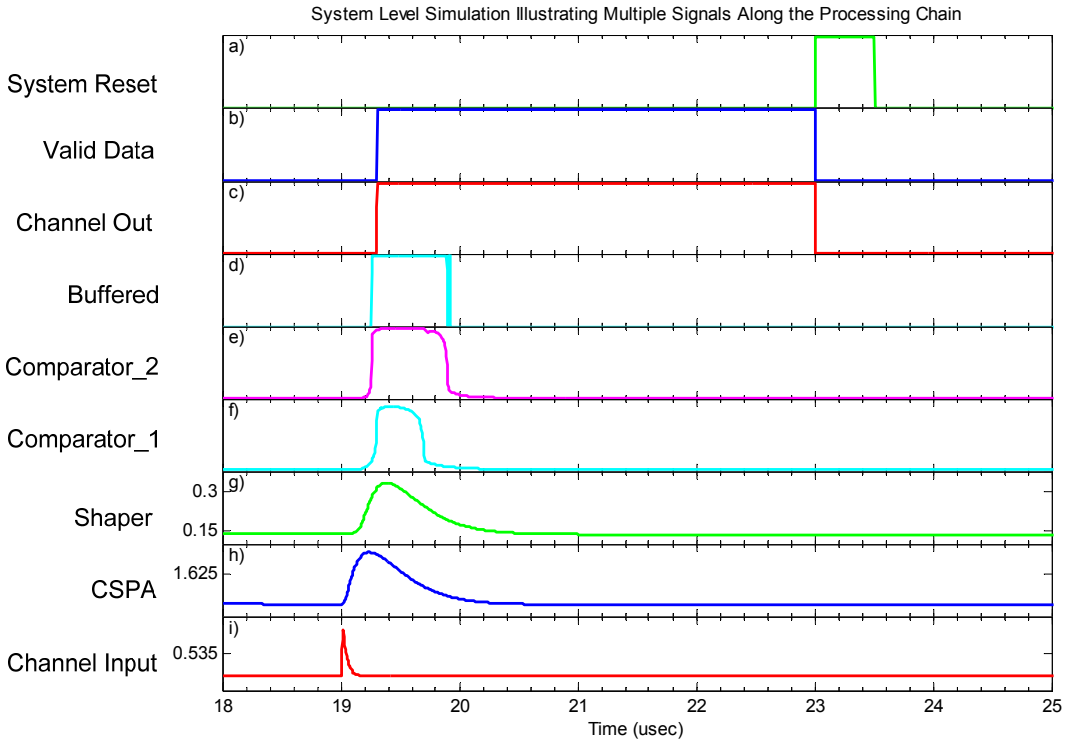

Figure 3.43 – a) System reset provided by the ROC, b) valid data flag provided by the ASIC, c) channel 0 register output from the 64-channel core, d) digital buffered output e) comparator 2 output, f) comparator 1 output, g) Shaper output, h) Preamp Output after first real pole, i) detector input

CHAPTER 4

SYSTEM TESTING AND VERIFICATION

4.1 Physical Design

The physical design of this ASIC was fabricated in the Taiwan Semiconductor Manufacturing Company's (TSMC) 0.35-µm bulk CMOS process available through a MOSIS shared project run. The overall physical dimensions of the die are 6.5 mm by 6.7 mm. The large amount of chip I/O resulted in 226 pads to be physically bonded out. This made hosting the ASIC a very challenging aspect of this work and will be revisited in the *Testing System Design and Configuration* section. A die photograph of the fabricated ASIC can be observed in Figure 4.1.

The TSMC 0.35-µm bulk CMOS process is economically advantageous, but presents many physical design challenges in a mixed-signal system. Since any given metal path is capacitively coupled to the substrate, high frequency edges from the digital circuitry can introduce charge injection (noise) to the substrate. Since this is a charge sensitive system, the analog circuitry's performance can be compromised with a large amount of substrate noise. Therefore, design techniques such as careful floor planning and shielding were employed in the physical implementation of this ASIC. An overview of the floor plan of this ASIC is illustrated in Figure 4.2.

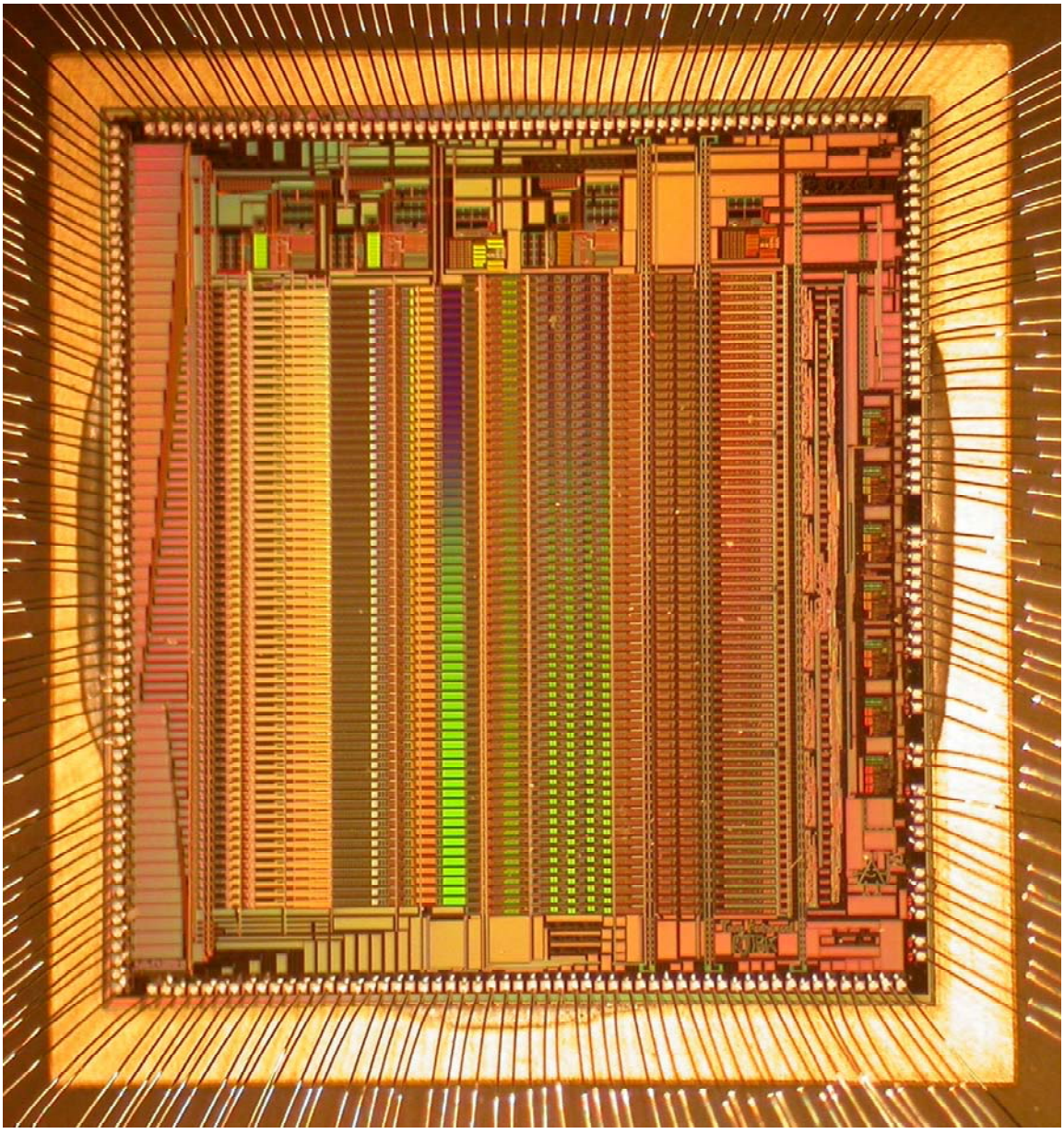

Figure 4.1 – Patara III ASIC micrograph

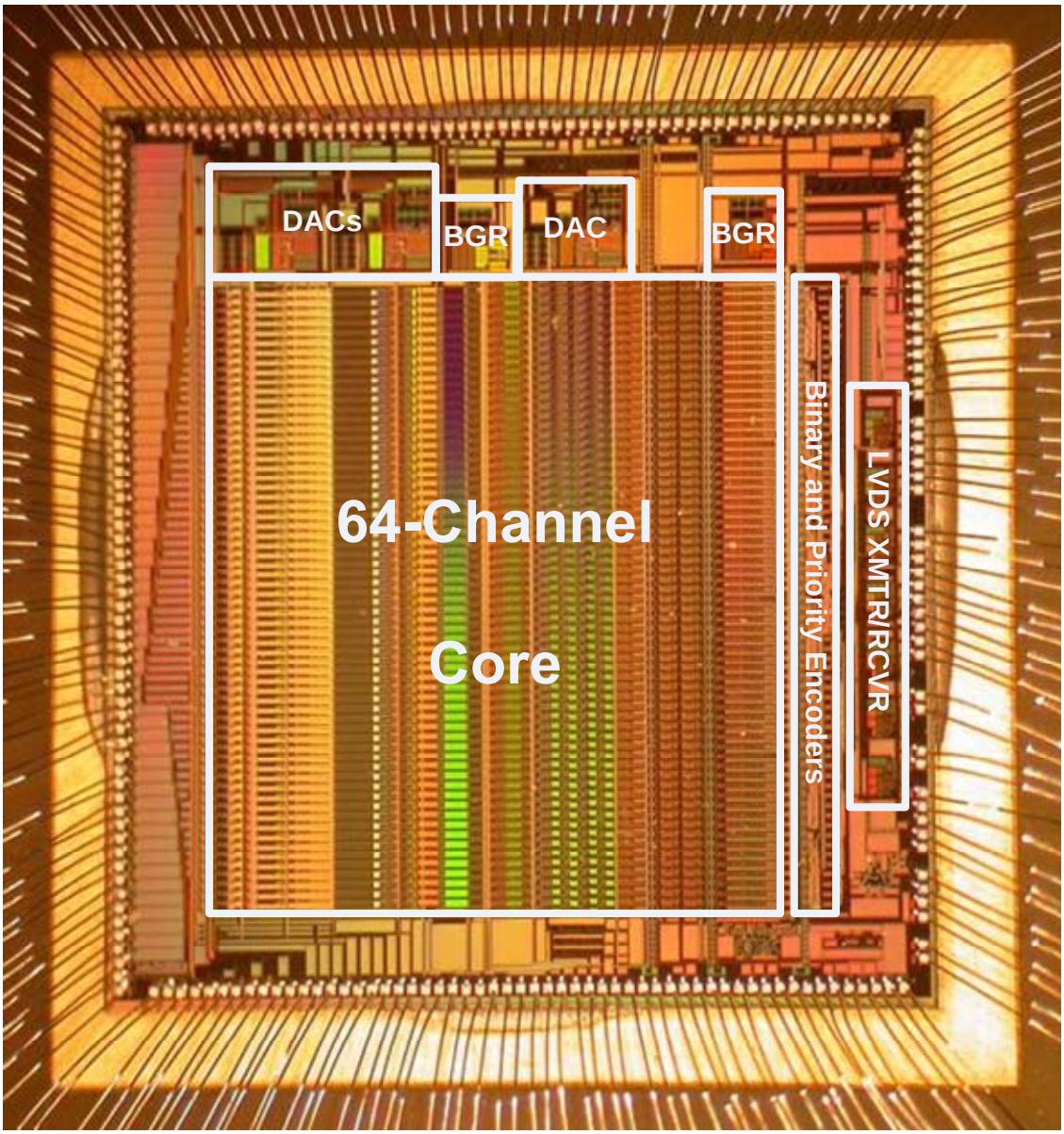

Figure 4.2 – Patara III ASIC micrograph with an overview of the floor plan

4.2 Testing System Design and Configuration

The testing interface for this ASIC must be able to handle a large amount of digital I/O and analog biasing while being able to synchronize with an external PC for user control. For efficient chip verification, it was desirable to not integrate directly with the SNS system. The implemented test configuration was designed to best emulate the SNS system and the readout card (ROC) for future implementations.

The two major functions of the testing system are to: 1) interface directly with the serial port on the ASIC along with providing user control over the static logic lines, and 2) provide a "handshake" protocol to the ASIC during data acquisition operation while applying a periodical base-line restore reset (analog reset). The synchronization and external digital circuitry is handled by a Xilinx Virtex-4 development board (part #DS-KIT-4VLX60MB-G) [25]. This board allows for 30 LVDS pairs of I/O and a P240 expansion slot along with many other peripherals. The synchronization with the CPU is handled by a National Instruments PXI express chassis hosting an NI-6536 digital I/O board [26]. The NI-6536 supports up to 32 digital I/O lines with a maximum speed of 25 MHz. The P240 expansion slot on the Virtex-4 board allows for a custom interface card to be designed that host's signal routing between the ASIC motherboard, the NI-6536 module, and the Virtex-4 FPGA. The operator is then presented with a developed LabVIEW front panel with supporting LabVIEW code for the data acquisition software. To efficiently verify the ASIC's functionality, the monolithic BIST is used to determine individual channel functionality and general system detection statistics. The statistical measurements will be discussed further in the *Testing Results* section.

4.2.1 Testing System Overview

The testing system block diagram is shown in Figure 4.3 illustrating major I/O between each block. The ASIC will be hosted on the motherboard while providing communication with the Virtex 4 FPGA. The Virtex 4 board complies with the ASICs "handshake" protocol by providing a reset prompt once the channel ID has been registered on the FPGA logic. However, the FPGA does not provide a system reset until the NI-6536 acknowledges registered data. Handshaking is then performed between the Virtex 4 FPGA and the NI-6536 to ensure proper data acquisition at the CPU. In general, the FPGA reads data when the *valid_data* flag is a logic '1' from the ASIC and provides a system reset once the NI-6536 provides a logic '1' via the *Data_Received* flag.

The Virtex 4 FPGA does provide a 10 MHz system clock via a phase divided 50

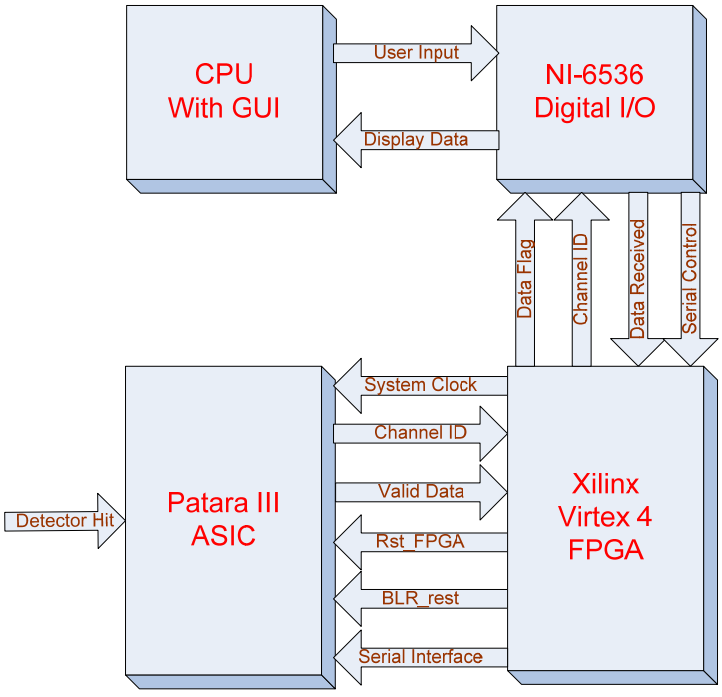

Figure 4.3 – Testing system block diagram

MHz oscillator. The clock output is effectively dictated by the user selection between the synchronous and the asynchronous system. If the user decides to run asynchronously, the clock does not leave the FPGA. This was desired to ultimately benchmark the noise contribution of clock throughout the entire testing system.

4.2.2 Patara III ASIC Motherboard and Daughter Card Design

A chip on board package is a more effective host for the ASIC due to the large number of bond pads (226 total). This package approach introduced the need for a daughter card and a high density connector between it and the motherboard. In the design of the daughter card, a high profile 17x2 connector was chosen. Repeating this connector 8 times allowed for 272 connections. To utilize all the available pins, the power and ground nets are connected to additional pins in parallel as to avoid "bottle necking" of the drawn current. In addition, separate pours for the ground planes were implemented so that the analog, digital and pad grounds would not introduce noise to each other. This technique ultimately preserves excess noise contribution from the digital circuitry to the analog circuitry. An image of the designed daughter card is shown in Figure B.2 in Appendix B.

The purpose of the motherboard in this testing system is to host the ASIC on the developed daughter card and provide all the peripheral biasing and I/O while avoiding additional noise contributions. The most important aspect of the design approach was to cleanly power and bias the ASIC. Specific power nets were kept separate on the ASIC and on the daughter card resulting in 8 nets at the motherboard. Each power net on the

motherboard was regulated by a fixed 3.3-V, 100-mA monolithic voltage regulator. The output of each regulator was then filtered by a passive lowpass RC filter with a −3 dB frequency of 160 kHz (R = 1 Ω and C = 1 μF). Having each power net isolated with a filter and a regulator effectively reduces the chance of any feed-through and noise contributions from peripheral nets. The input power to each regulator shared the same net so that each regulator powers up simultaneously.

The constructed motherboard hosts the external biasing for the ASIC, the static biasing, and adjustable biasing. The static biasing was implemented with pull-up or pull-down resistors and filtering capacitors at each bias node. The adjustable biasing and mode settings were constructed with 3 dip switches and 2 potentiometers. The potentiometers are used to allow user adjustment of the offset voltages for the DAC and the second comparator setting in the ADC separately. A description of the dip switches functionality on the motherboard can be found in Table B.1 of Appendix B.

In addition to the peripheral biasing and power inputs, the motherboard must comply with the serial I/O protocol from the Virtex 4 FPGA. Due to noise concerns, all I/O on the motherboard is presented in an LVDS format. Since the serial interface on the ASIC is formatted as standard CMOS logic, external LVDS receivers were added to the motherboard. This allowed for complementary twisted pair ribbon cables to be used between the motherboard and the Virtex-4 board. An image of the developed motherboard is shown in Figure B.1 of Appendix B, and an image of the motherboard hosting the daughter card is shown in Figure B.3 of Appendix B.

4.2.3 Interface Card

The purpose of the interface card is to provide clean signal routing between the Patara III ASIC, the Virtex-4 FPGA, and the NI-6536 module. The design of the interface card utilizes the P240 expansion slot on the Virtex-4 development board. Due to the large amount of I/O and noise sensitive LVDS nets, this board utilizes PCB layout techniques for low parasitic and clean signal transmission between the major pieces of hardware. An image of the interface card can be seen in Figure B.4 and Figure B.5 of Appendix B.

4.2.4 Virtex-4 VHDL Development

The first step during the development of the VHDL code for the Virtex-4 FPGA was to utilize the on-chip LVDS buffers to interface the I/O from the Patara III motherboard. This is implemented by instantiating the buffers by using the SelectIO Primitives *OBUFDS* and *IBUFDS*. To reduce reflection between the LVDS point-to-point transmission, the attribute *DIFF_TERM* is set to *TRUE* to enable 100 Ω differential termination on the FPGA.

With the LVDS buffers implemented on the FPGA, the next step was to coordinate serial communication from the LabVIEW environment to the ASIC. The LVDS buffers on the FPGA translate the logic to a standard 3.3-V TTL compatible signal allowing the serial lines to be directly routed to the digital I/O lines of the NI-6536 module. This direct connection promotes the ability for the developed LabVIEW code to handle the serial interface control while the FPGA is merely used as a translator from

LVDS formatting to 3.3-V CMOS formatting. Further details about the LabVIEW code will be discussed in the next section.

The serial interface allows for the user to program the ASIC and set it to a valid operating state. Once programmed, the ASIC is fully functional and able to provide dynamic data at the output of the system with a charge stimulus at the input. The ASIC output is formatted in the following manner: a 6-bit binary word packet for the channel ID, a 1-bit valid data flag, and a 1-bit reset. The FPGA is responsible to interface this output and handle "handshaking" with the ASIC. In addition to "handshaking" with the ASIC, the FPGA handles "handshaking" with the NI-6536 module so that the channel ID can be registered with the CPU prior to resetting the registers in the ASIC. This was implemented by using a coded state machine. The Virtex-4 state machine reads the valid data flag from the ASIC for a logic '1' and registers the channel ID. The FPGA then presents a valid data flag to the NI-6536 module and waits for an acknowledge (ACK) response. Once the ACK signal from the NI-6536 module is a logic '1,' the FPGA then resets the registers on the ASIC and goes back to the initial state.

For optimal operation of the ASIC, the baseline restore (BLR) loop must be reset on a periodical basis. During development it was determined that the optimal period is 3.3 msec. The BLR reset is held for 20 μsec of the total period allowing for system operation the remaining portion of the period. However, false events do occur during a BLR reset edge (rising and falling). To ensure that these false events are not read, a digital reset is held for the duration of the BLR reset. The analog circuitry does have a given decay time on a signal response, therefore the digital reset must overlap the

duration of the BLR reset. It was determined that a digital reset of 50 µsec was sufficient to avoid reading false events. The decay time of the analog circuitry occurred more significantly after the falling edge of the BLR reset signal, therefore the digital reset is held longer at the tail end of the BLR reset. A visual description of the timing specifics for the BLR and digital resets are shown in Figure 4.4.

The FPGA was given the responsibility to handle the timing specifics during the monolithic BIST. This is desired over the NI-6536 since the LabVIEW software is handled with interrupts and not real time. During a continuous discharge across the monolithic capacitor in the BIST, a 1 kHz clock signal is routed to the *discharge_bar* net from the FPGA. This will create a pulse-pair resolution of 1 kHz at the desired input channel. To handle the statistical analysis of the system, the FPGA creates a waveform triggered off the rising edges of the signal it sends to the ASIC. Routing this signal to the NI-6536 module allows for the number of events that has occurred at the input of the

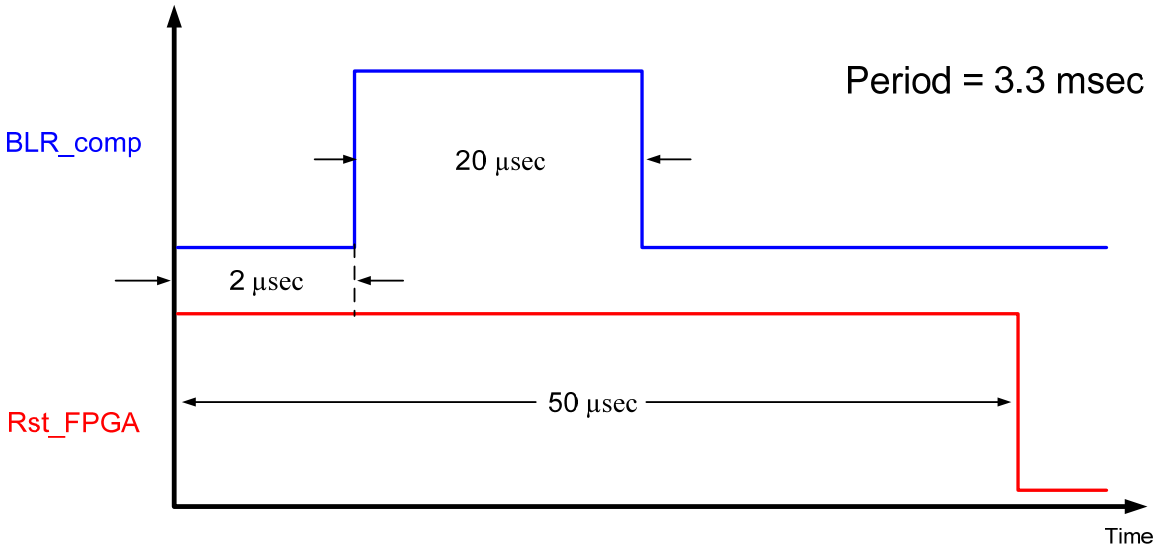

Figure 4.4 – Timing description for the BLR reset and the digital reset

ASIC to be calculated in software. Since the BLR reset and the digital reset occur periodically, an event should not be counted if it occurs during the reset window. Therefore this case is neglected and the NI-6536 does not account for it. In addition to the continuous discharge mode in the BIST, the FPGA allows for a single discharge mode. When the user selects this mode of operation, the FPGA routes a control line from the NI-6536 to the *discharge_bar* net allowing the user to create the events with a software switch at his/her own pace.

The interested reader can reference Table B.2 in Appendix B for the interface card I/O descriptions. This table also provides Virtex-4 and NI-6536 net locations from the ASIC to the Virtex-4 board and from the Virtex-4 board to the NI-6536 module.

4.2.5 Hardware Test Bench Illustration

A test bench view of the hardware configuration is illustrated below in Figure 4.5. The NI-6536 module is hosted by a high speed PXI chassis which interfaces the CPU with a PCI Express controller. This configuration for the NI-6536 is not always the case. The NI-6536 is offered in two platforms: a PXI platform, and a PCI express platform. The PCI express platform allows for the module to be installed directly into a PCI Express slot on a CPUs motherboard in place of the PCI Express controller. Both configurations are valid in this test bench. Accompanying the NI-6536 module is the Virtex-4 board and the ASIC motherboard. They are connected to each other via twisted pair ribbon cables for optimal noise suppression.

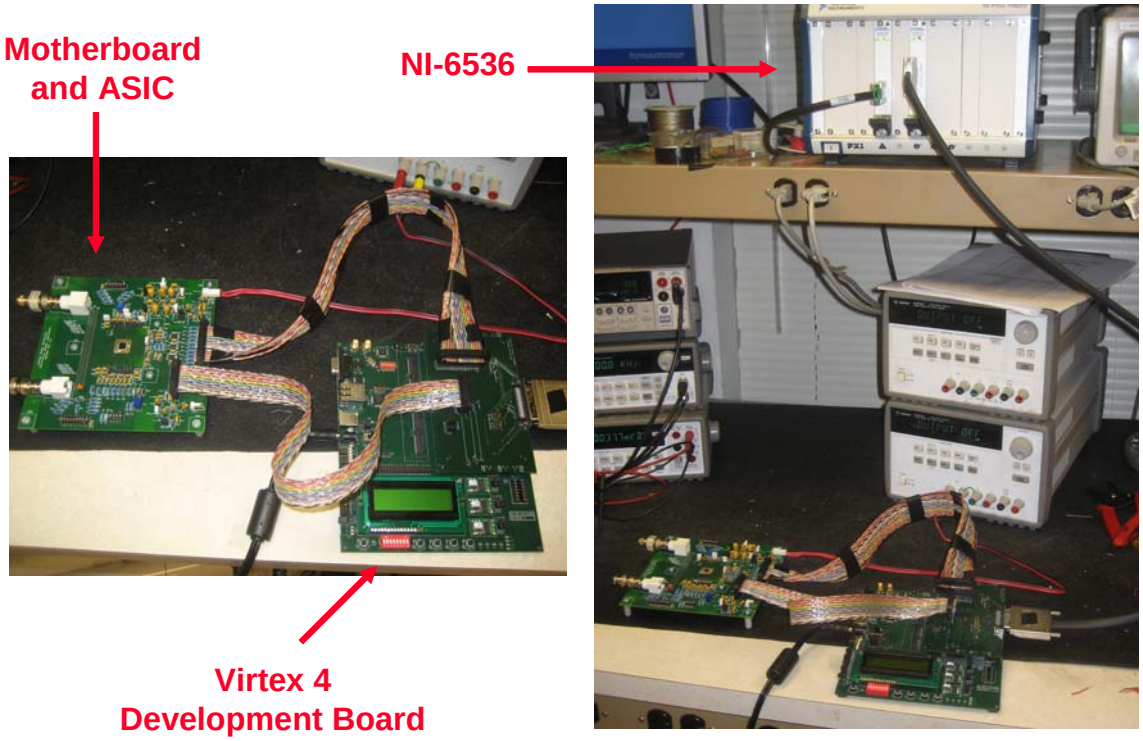

Figure 4.5 – Hardware test bench

4.2.6 LabVIEW Development

The data acquisition software for the ASIC was implemented through LabVIEW code development and integration with the NI-6536 module. The FPGA in this test system is responsible for the timing and communication between the Patara III motherboard and the NI-6536, whereas the NI-6536 is responsible for the digital interpretation. Since LabVIEW code is not intuitively interpreted from visual illustrations, the code development process will be merely discussed. The front panel for the developed software is shown in Figure 4.6 and is viewed as a reference to the functionality given to the user.

The first task when developing this software was to handle the serial interface. Software looping structures and a "bit-bang" approach was used to implement this; recalling that this functionality is directly passed to the LabVIEW environment while the FPGA simply translates the LVDS formatted logic to a 3.3-V standard logic. A 'for' loop structure toggles the shift clock line while presenting the serial data input for the duration of the serial packet. Once the serial packet is shifted into the registers, a program clock is set high, hence the "bit-bang" approach.

There are three total states to the software: 1) Continuous Charge BIST, 2) Single Charge BIST, and 3) Data Acquisition. The software limits the user to being in only one state at a time. When using the BIST states, the user can dictate which channel undergoes an emulated event. In addition, the user can apply multiple hits at two desired channels in order to verify functionality of the priority encoding. During the continuous charge event testing, the user is displayed simple statistics and event counting. The

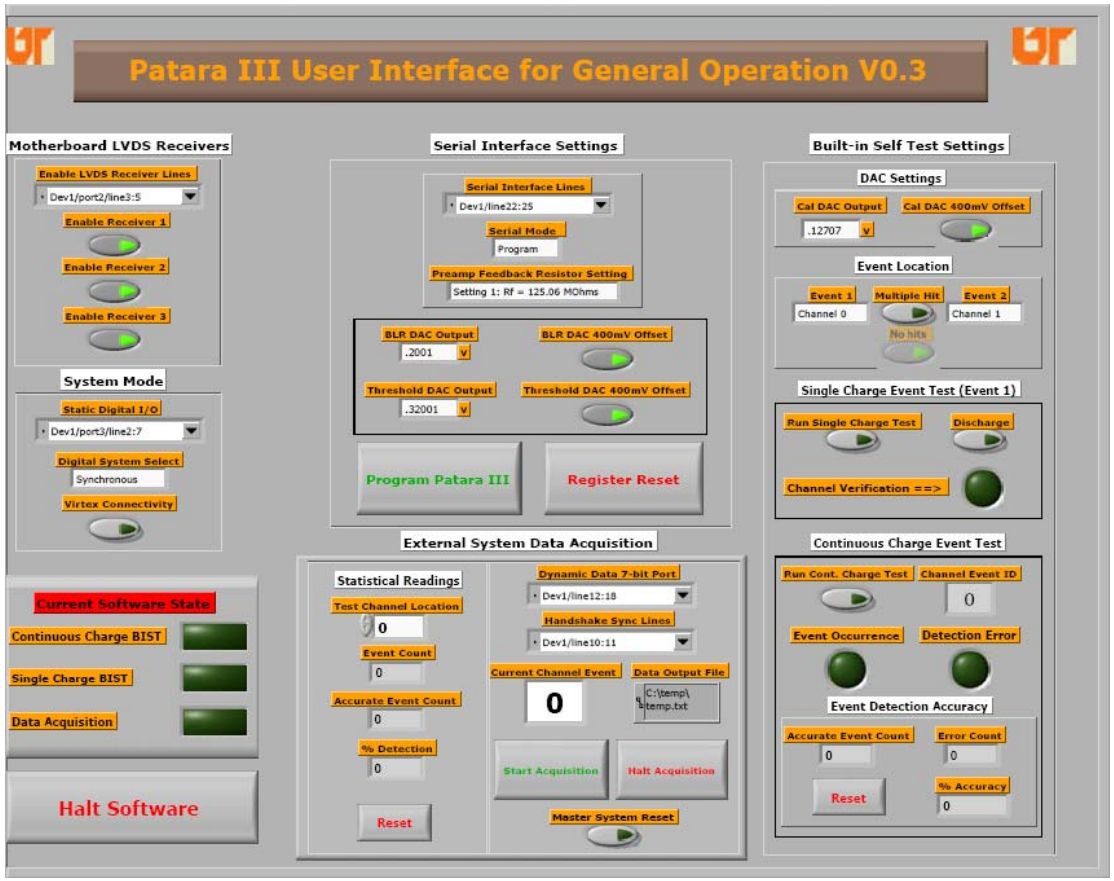

Figure 4.6 – User front panel of the developed LabVIEW software

calculated accuracy is defined as the correctly detected events divided by the total number of detected events. This is useful when determining the quality of the ASIC's programmed state during operation.

During single charge event testing, the user is given control of the applied discharge signal via a software switch. Therefore, the user can quickly verify functionality of a single monolithic channel. If the correct channel is detected, a software LED indicator is illuminated green and the digital display shows the channel that underwent an event.

The external data acquisition software state gives the user the ability to create an event at the input of the ASIC externally. For testing purposes, the user can input which channel is being tested to verify correct detection. In addition to the accuracy measurement, the % detection calculation is performed. The % detection is calculated by taking the total number of detected events divided by the total number of events presented at the input. However, the user must supply a synchronous parallel connection to the NI-6536 in order to quantify the number of events applied to the input.

4.3 Testing Results

The expected functionality of the ASIC was verified after the successful completion of the testing system. The following section will illustrate the results supporting a fully functional data acquisition system for the solid-state linear thermal neutron detector. The following sections will also aid in quantifying the ASIC specifications for the benefit of an operator.

4.3.1 Bandgap Voltage Reference

The developed monolithic BGR was designed to provide a voltage reference for the LVDS transmitters' common-mode level and the LSB current for the DACs. Having the reference on chip eliminates the need for any external biasing. The draw back to integrating a BGR is that it has been shown to suffer from process variations. Some sensitive points in the topology of the designed BGR in this ASIC are: 1) the output resistor matching with the thermal voltage referenced resistor, 2) the matching of the current mirror devices in the PTAT current source branch to the output leg current mirror devices, 3) the matching of the monolithic diodes, and 4) matching of the input devices to the current amplifier in the KVL loop. This ultimately raises the need for statistical measures to be made on the value of the output reference. Trimming can be used as a design approach to tighten the distribution of the output reference. However, this technique was not performed in this ASIC.

The two outputs of the bandgap voltage references were brought off chip in order to measure the discussed variations. The statistical quantifications were conducted separately for the two BGRs, and are presented with respect to their purpose. The LVDS BGR was statistically shown to have a standard deviation of 36.9-mV and a typical value of 1.21-V across five chips. The DAC BGR was shown to have a standard deviation of 38-mV and a typical value of 1.18-V across five chips. BGR measurements are shown in Figure 4.7 and Figure 4.8.

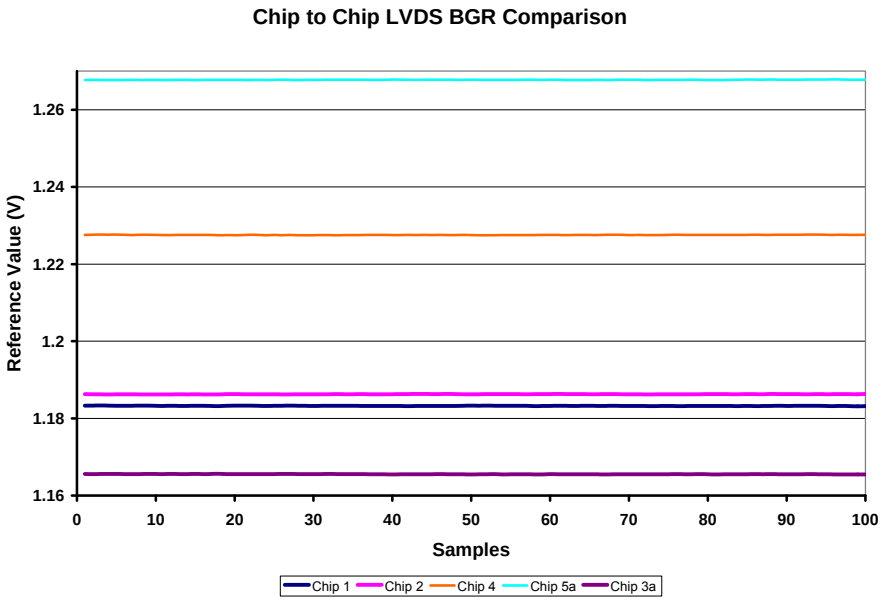

Figure 4.7 – LVDS BGR measurement across 5 chips

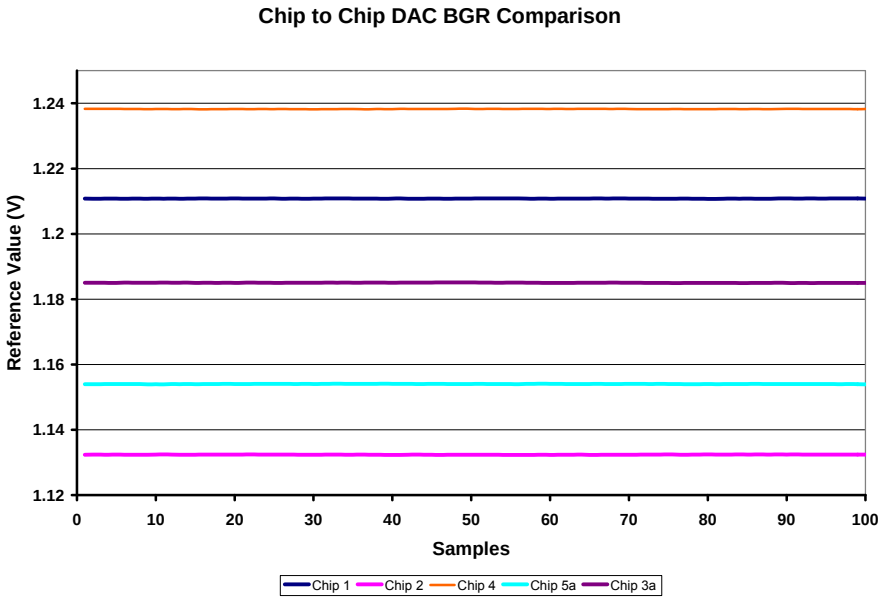

Figure 4.8 – DAC BGR measurement across 5 chips

4.3.2 Digital to Analog Converter

The DAC was found to operate very similar to theoretical and simulated results. However, the DAC output was expected to be able to operate very near ground. It can be observed in Figure 4.9 below that the measured response varies from the simulated and the theoretical responses near ground. It is apparent that the DAC loses monoticity from the decimal input words 245 to 255. This result is primarily due to the output stage of the op amp in the transimpedance stage of the DAC. The devices in the output stage are moving out of strong inversion operation leading to a decrease in functionality. Therefore more current is being dumped back through the feedback path into the current summing node (see Figure 3.38 for DAC topology) resulting in an increase in voltage at the DAC's output.

Fortunately the application of this DAC on the ASIC does not require an output

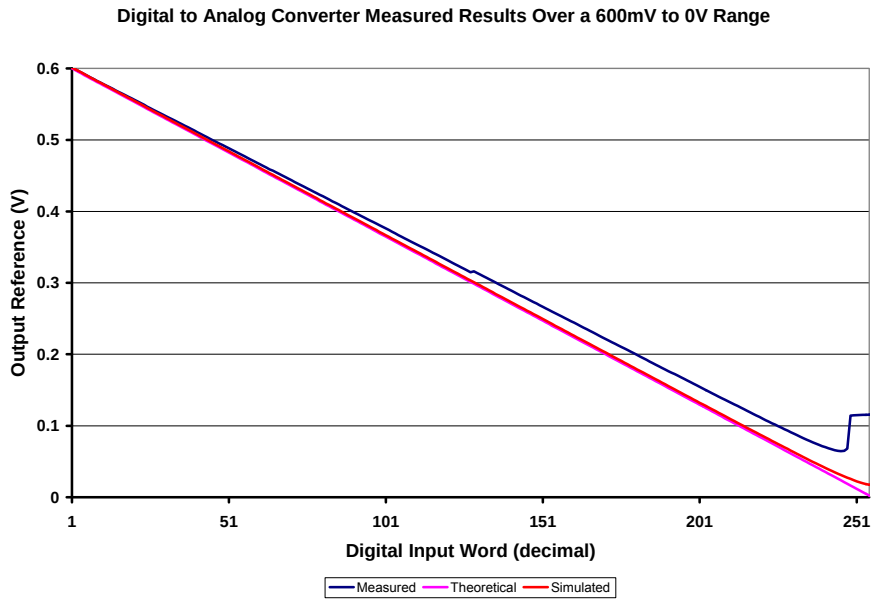

Figure 4.9 – Measured DAC transfer curve over the 600-mV to 0-V range

below 100-mV. Therefore an operation range of 700-mV to 100-mV is suggested. This can be implemented by adjusting the offset voltage (V_{off}) to 1.1-V rather than 1-V. The transfer curve for this operation mode is shown in Figure 4.10. Here it is observed that monoticity is maintained along with linearity. However, there is some gain (slope) error. This is actually a very reasonable result. Referencing equation (3.26), it is obvious that the value of V_{bgr} dictates the slope. In this DAC measurement, the output reference value for the BGR was 1.18-V. Since this value is less than the anticipated value of 1.25-V, the slope is less than expected. Therefore, any error in the bandgap reference results in gain (slope) error in the DAC. Since this can be predicted by the derived transfer equations, software can alter the expected output of the DAC by substituting the measured value of the bandgap reference into the transfer function of equation (3.25). A DAC transfer characteristic with a BGR output value of 1.24-V is shown in Figure 4.11. This verifies

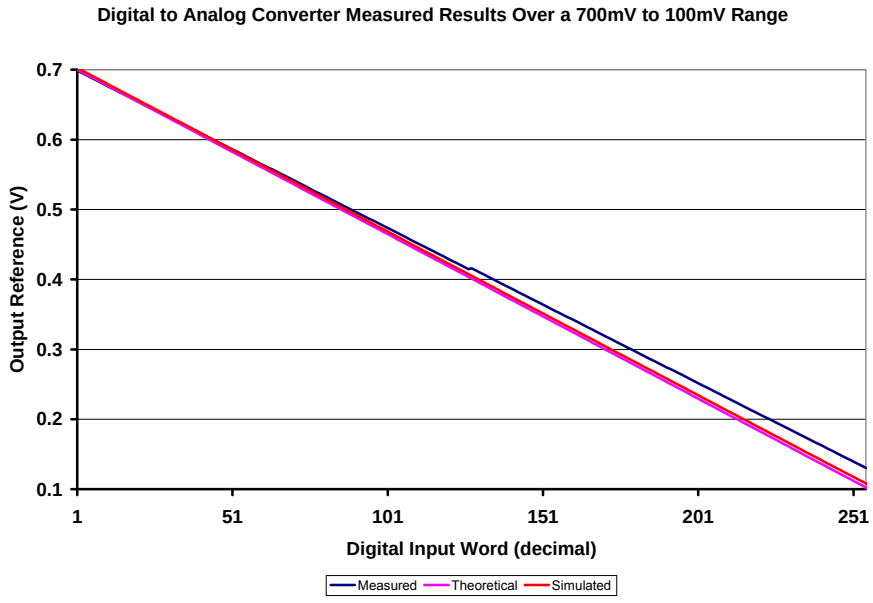

Figure 4.10 – Measured DAC transfer curve over the 700-mV to 100-mV range

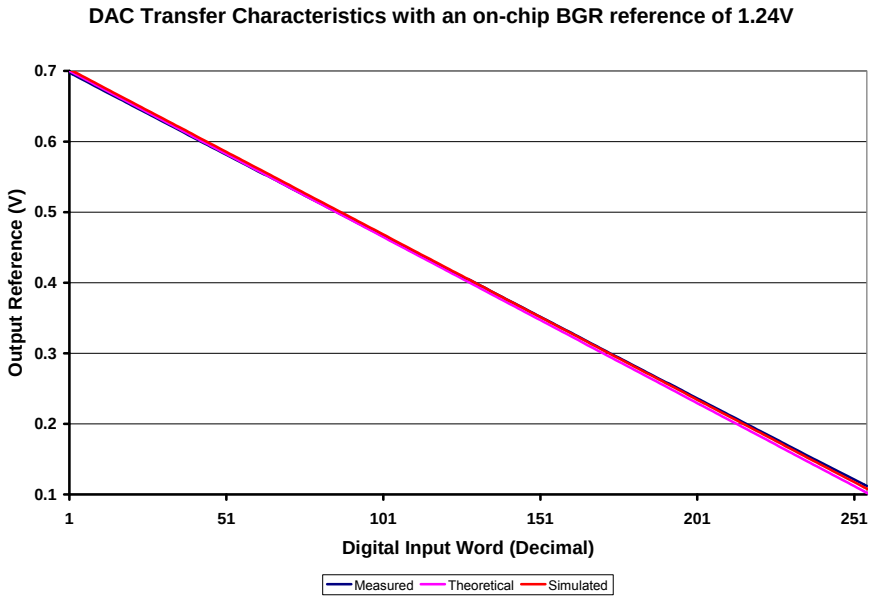

Figure 4.11 – Measured DAC transfer curve with a BGR output value of 1.24V

that the DAC does abide by the transfer function derived during the design process.

The on-chip transfer characteristic variation for the DAC is provided in Figure 4.12 along with the DNL in Figure 4.13. The DNL plot does show a significant spike at decimal input word 128. To understand why this is the worst case DNL, the binary word for decimal 128 is '10000000' and the binary word for decimal 127 is '01111111.' Observe that the MSB between decimal 127 and decimal 128 is switching high while all preceding bits in decimal 128 is switching low. Electronically, the MSB current source is showing a current mismatch between the other binary weighted current sources. The MSB current mirror device will have the most extreme variation due to its large aspect ratio. During the layout of the DAC, a common-centroid matrix of the current

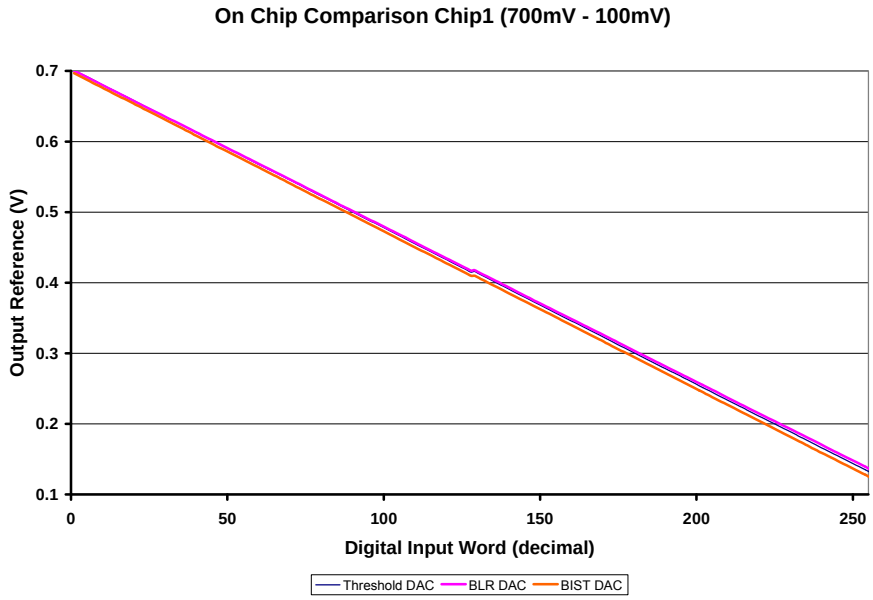

Figure 4.12 – Measured transfer characteristic variation on chip

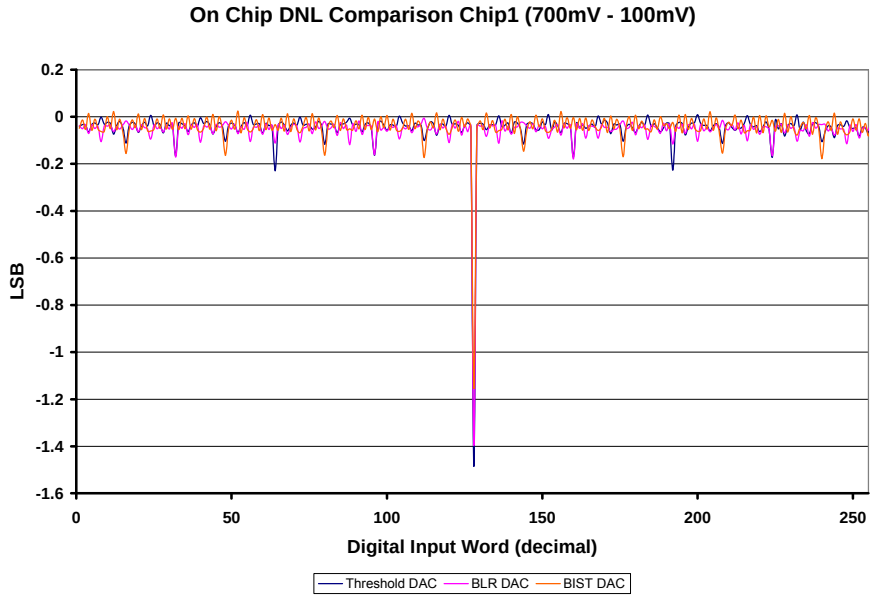

Figure 4.13 – Measured DNL variation on chip

mirrors were implemented to reduce the effect of device mismatch. If this design approach was not taken, a much worse DNL error would have been observed.

The next result illustrates the integral-non-linearity (INL) of the DAC. This measurement allows for a quantification of the DACs linear response. It is provided in both LSB and Percent Full Scale Error. Normalizing the measurement to the LSB value illustrates the variation with respect to the bit accuracy of the DAC. Normalizing the measurement to the full scale of the DAC illustrates the percent error at that given input word over the full scale. The INL in LSB is shown in Figure 4.14 and the INL in Percent Full Scale Error is shown in Figure 4.15.

The chip-to-chip variation of the transfer characteristic is shown in Figure 4.16 along with the DNL variation in Figure 4.17. It is apparent that the gain error is primarily due to the BGR output variation. The BGR value for chip 1 is 1.18-V, for chip 2 is 1.13-V, and for chip 3 is 1.24-V. Here it is observed intuitively that the chip with the lower BGR value yields the worst gain (slope) error. The DNL also shows the same results across multiple chips verifying that topology is the major concern with the current mirror mismatch. If this were skewed across multiple chips, the assumption can be made that process variation is the issue.

The chip-to-chip variation of INL in LSB is shown in Figure 4.18 and the variation of INL in Percent Full Scale Error is shown in Figure 4.19. The INL was also found to have its best performance when the BGR was closest to the anticipated value of 1.25-V.

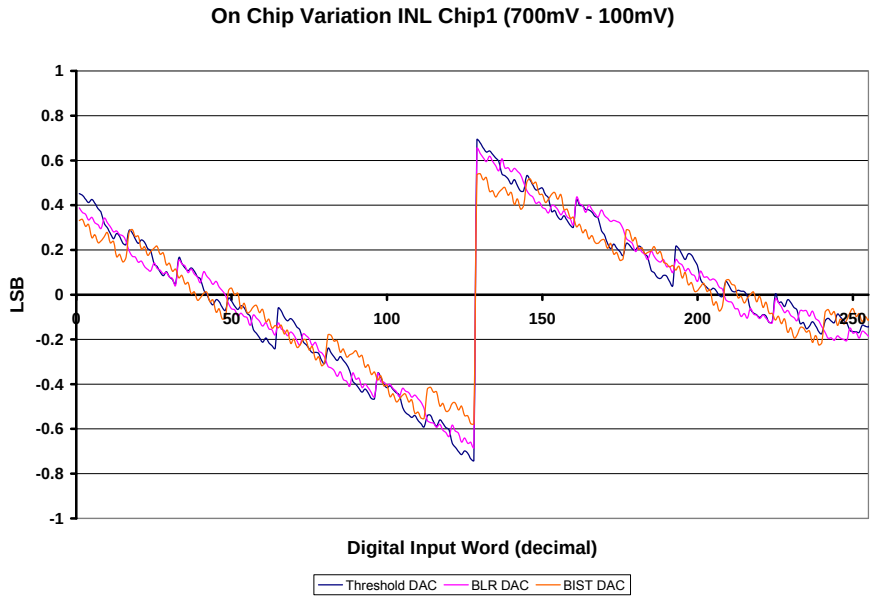

Figure 4.14 – Measured INL in LSB on chip

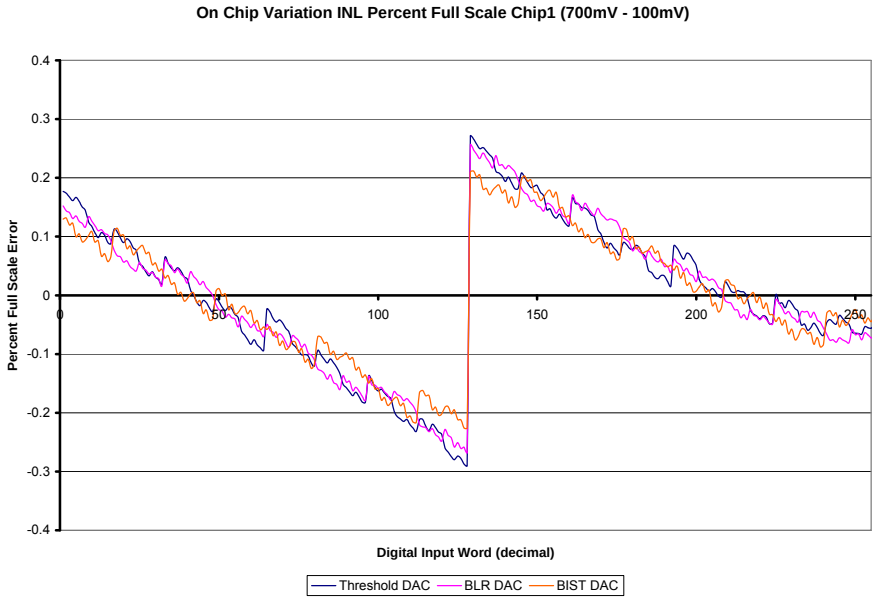

Figure 4.15 – Measured INL in Percent Full Scale Error on chip

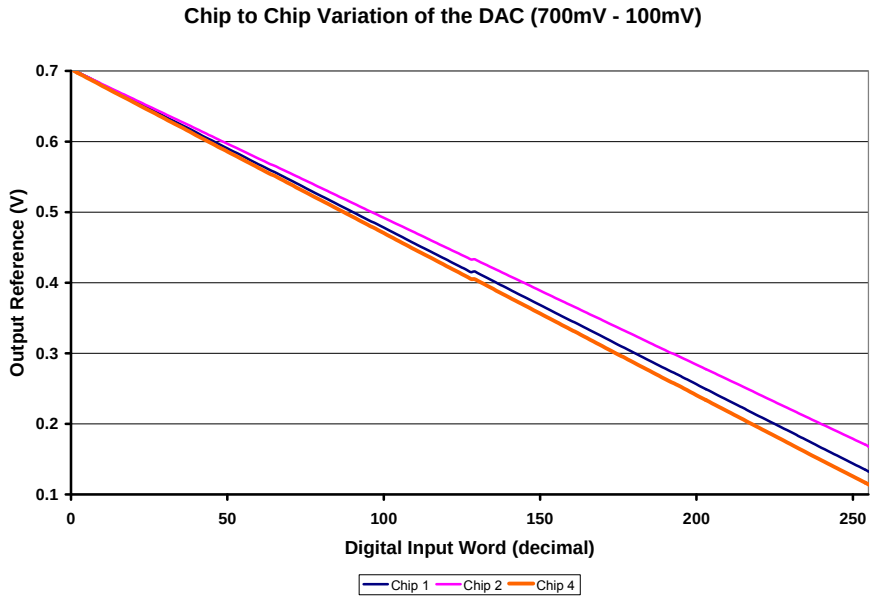

Figure 4.16 – Measured transfer characteristic variation chip-to-chip

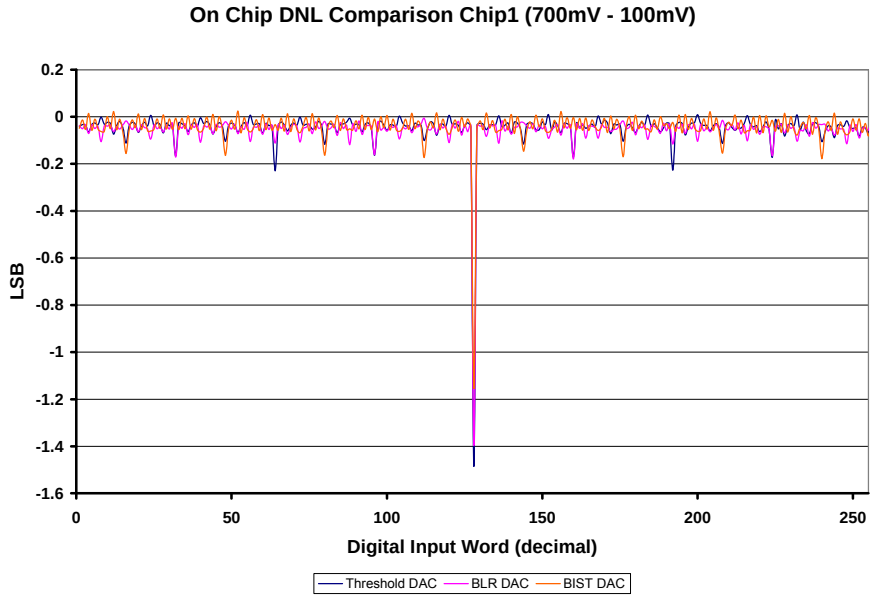

Figure 4.17 – Measured DNL variation chip-to-chip

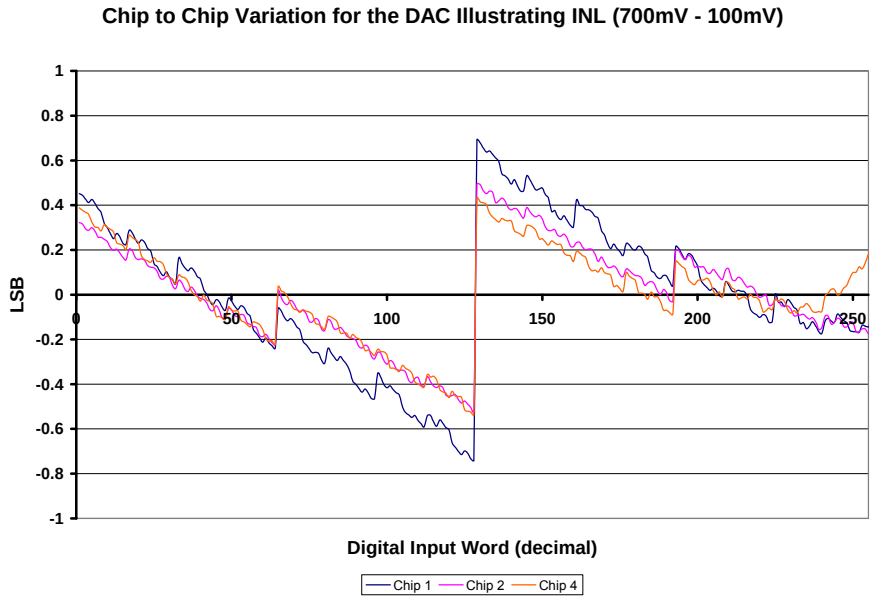

Figure 4.18 – Measured INL in LSB chip-to-chip

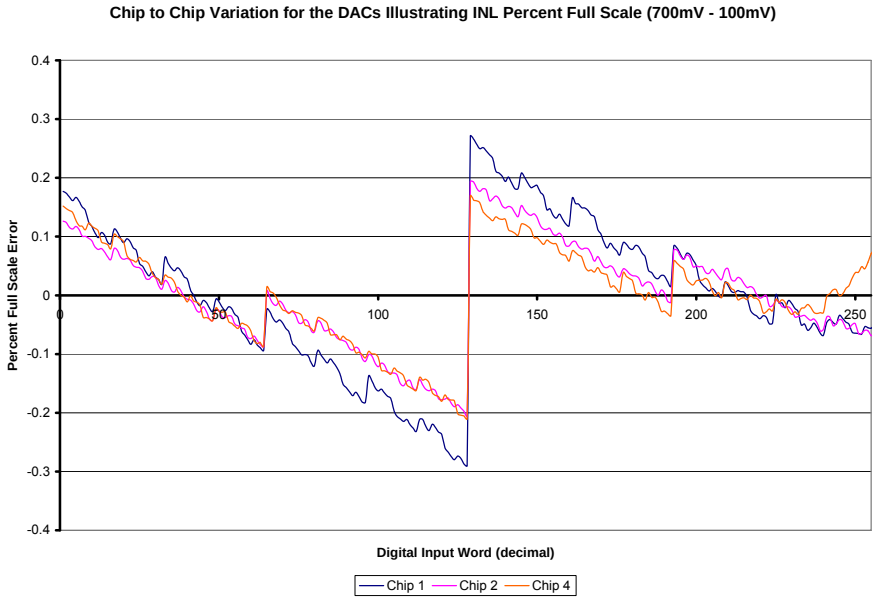

Figure 4.19 – Measured INL in Percent Full Scale Error chip-to-chip

4.3.3 Analog Processing Chain

A concern in this ASIC was preserving the functionality of the analog circuitry when adding the mixed-signal components on the same substrate. Other concerns were noise contributions due to the bulk substrate, and variation across a large die. The noise contributions were suppressed by isolating the digital components and nets from the substrate. This was implemented by adding n-well underneath the digital metal traces and by adding a significant amount of guard rings (active layers) around the digital and analog circuitry. The variation across chip could not be managed as well. With 64-channels it is inevitable that variation will occur.

The first stage of the analog processing chain is the charge sensitive preamplifier. Spy points were set up on channel 0 and channel 63 allowing for observation of the worst case variation. Figure 4.20 illustrates the observation made at these spy points. The next

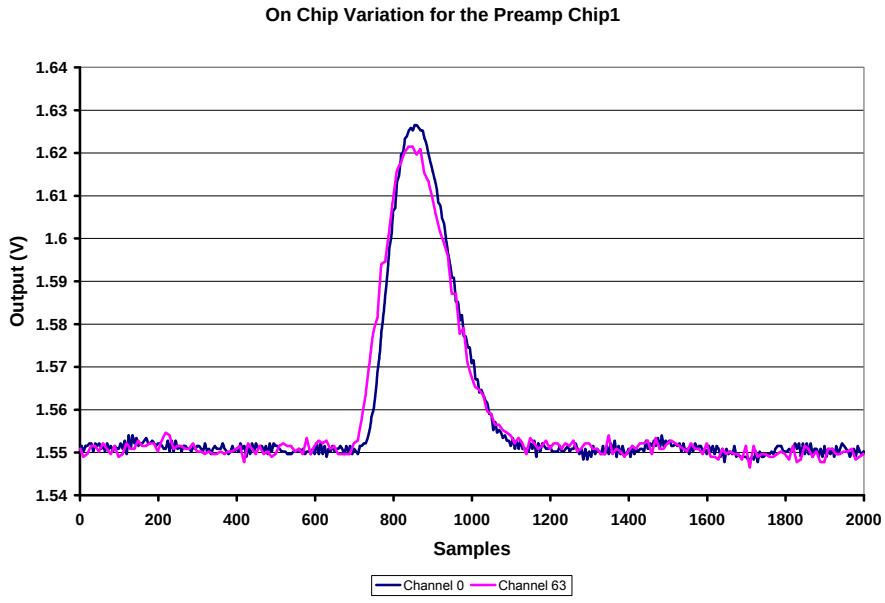

Figure 4.20 – Measured preamplifier variation across chip

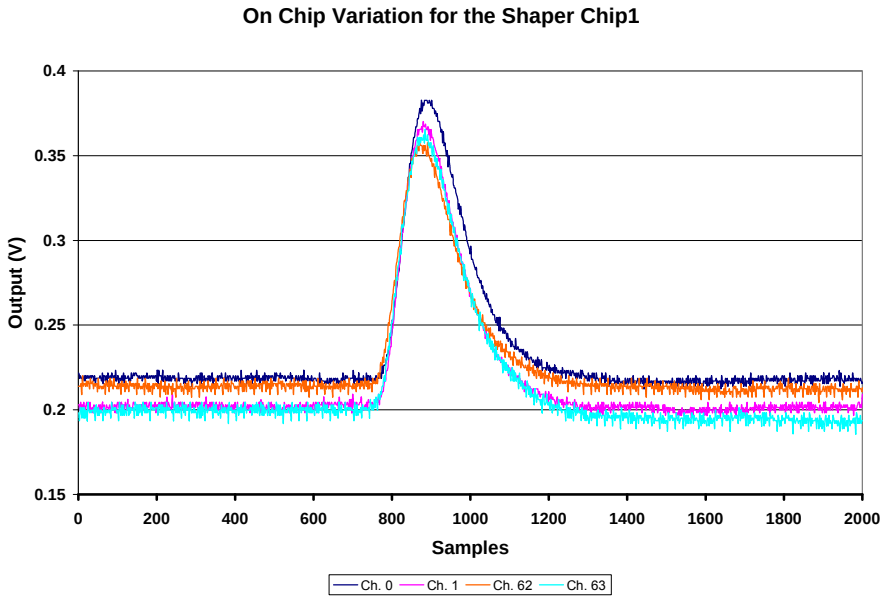

Figure 4.21 – Measured shaper variation across chip

stage of the analog signal processing chain is the shaper. Spy points were set up on channel 0, channel 1, channel 62, and channel 63. Figure 4.21 shows the observation at these spy points. The greatest concern during normal operation is the offset variation from the baseline. The shaper baseline offset was quantified across chip at a baseline of 200-mV and 300-mV. These measurements are shown in Figure 4.22 and Figure 4.23. The standard deviation for the baseline offset at a baseline level of 200-mV is 6.42-mV, and the standard deviation for the baseline offset at a baseline level of 300-mV is 6.53-mV. Here it is concluded that the baseline offset does not vary much with baseline level. However, the offset is random and will need to be quantified across a great number of samples (chips) for a better specification.

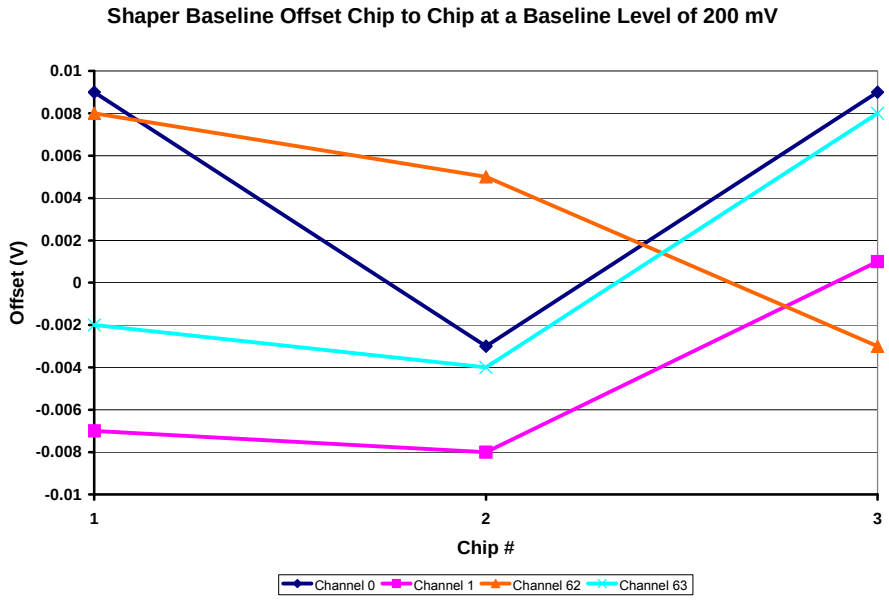

Figure 4.22 – Measured shaper baseline offset variation at a baseline of 200-mV

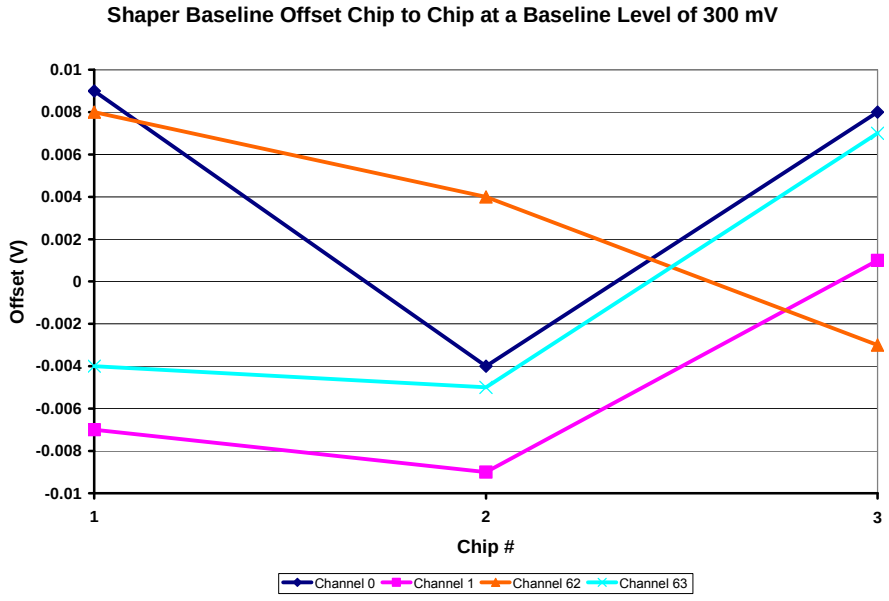

Figure 4.23 – Measured shaper baseline offset variation at a baseline of 300-mV

The noise contribution due the clock can be observed by running the system in synchronous (with clock) and asynchronous (without clock) mode. It was expected that some amount of noise would occur since the frequency of the system clock is 10 MHz. This would ultimately lead to a noise contribution in the 10 MHz band. Figure 4.24 illustrates the shaper response with and without a system clock. Note the small amount of additional noise present in synchronous mode.

The next important measurement is the probability of detection and the percent accuracy across multiple channels on the same chip. This was implemented by using the monolithic BIST. Note that the on-chip capacitors used for the input charge does have a ±20% variation. This will alter the results independent of the electronics. Recall that the probability of detection is determined by the total number of *accurate* events detected divided by the total number of events that have occurred. The percent accuracy is determined by the total number of *accurate* events detected divided by the total number

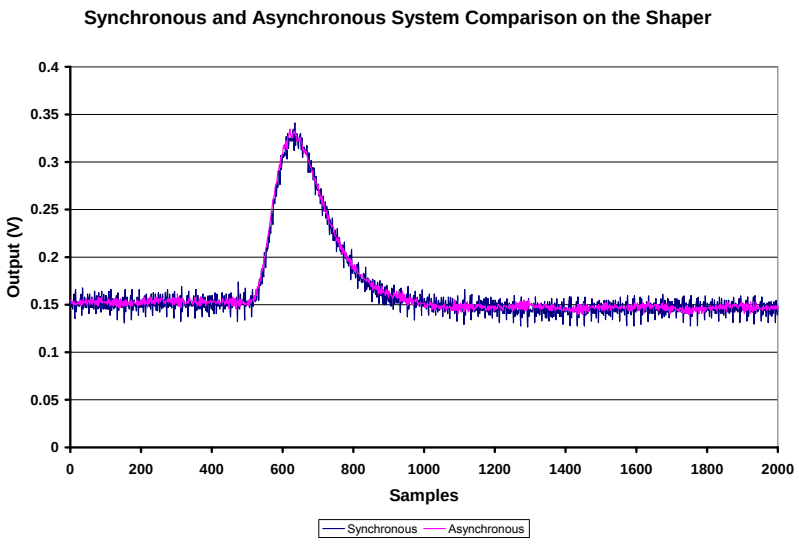

Figure 4.24 – Measured noise contribution observation on the shaper response

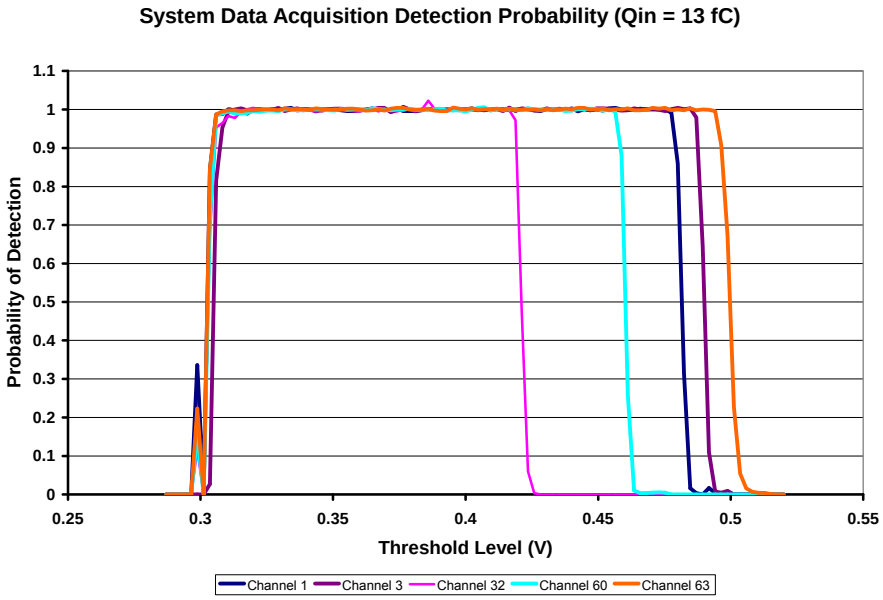

Figure 4.25 – Measured probability of detection across multiple channels

of events detected. Figure 4.25 and Figure 4.26 illustrate these two measurements.

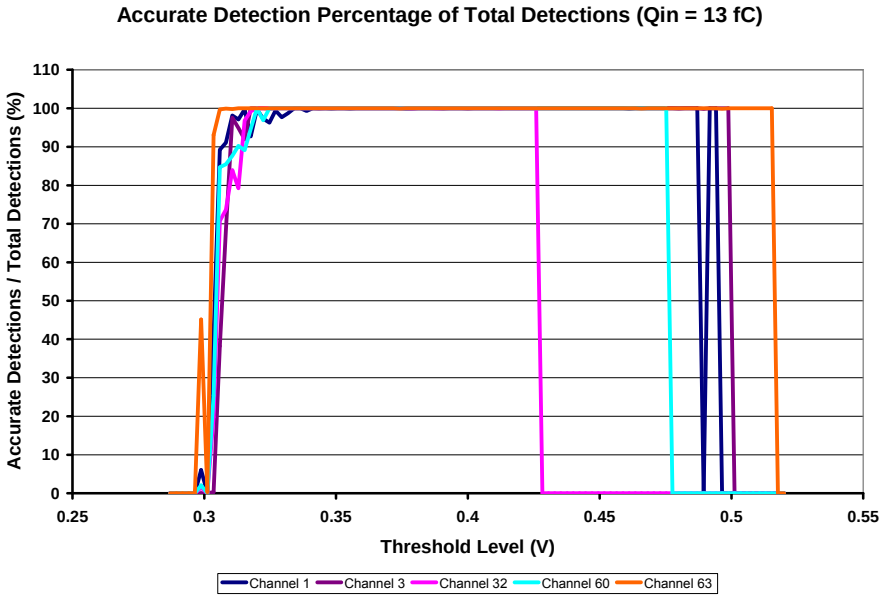

Figure 4.26 – Measured percent accuracy across multiple channels

The probability of detection and percent accuracy measurements allows for a statistical observation to be made on the hit threshold setting. From the above figures, a threshold level of 350-mV to 400-mV at a baseline level of 200-mV would statistically results in a 100% probable detection of a 13 fC input charge with an accuracy of approximately 100 % across 1,000 samples. The same measurement would have to be conducted across many chips to better quantify this statistical measurement for a global setting. This will ultimately lead to a global setting for all chips with an expected charge level from the sensor.

4.3.4 Measured Results Summary

A summary of the general results for the ASIC can be viewed in Table 4.1 below.

Table 4.1 – General results summary for the Patara III ASIC

Parameter	Conditions	Min	Typ	Max	Unit
LVDS BGR	T = 25 C	1.165	1.210	1.267	V
DAC BGR	T = 25 C	1.132	1.184	1.238	V
DAC DNL	BGR = 1.24V	−0.989		0.0395	LSB
DAC INL	BGR = 1.24V	−0.537		0.432	LSB
DAC INL Percent Full Scale	BGR = 1.24V	−0.210		0.169	%
BLR Offset	Baseline = 200-mV	−8	1.08	9	mV
Probability of Detection	LLD = 350-mV, Baseline = 200 mV, Qin = 13 fC	0.997	1	1	
Percent Accuracy	LLD = 350-mV, Baseline = 200 mV, Qin = 13 fC	100	100	100	%

CHAPTER 5

CONCLUSIONS

5.1 Conclusion

This thesis presented the design process from the previous work that led to the current ASIC design, *Patara III*. The ASIC design was fabricated in the TSMC 0.35-µm process and testing results verified a fully functional data acquisition system capable of operating 64 linear thermal solid-state neutron detectors. A testing system was developed to best emulate integration with the SNS system and was shown to fully exercise all the functionality of the ASIC. This ASIC takes full advantage of today's current semiconductor processes to integrate a high density, small footprint SoC. Resulting in a size of 6.5 mm by 6.7 mm, this solution to a high channel count data acquisition system proves to be superior over an alternative printed circuit board based system.

The ASIC was shown to achieve full functionality with all the designed on-chip components. This result allows for the full utilization of the ASICs functionality with no external components. In addition to this achievement, the analog circuitry did not show a decrease in functionality when the mixed-signal components were added to the same substrate. The only significant difference is the small amount of noise introduced when a system clock is present. If this result poises a concern, the ASIC can still operate without a synchronous clock.

With the robust design of the digital to analog converter (DAC), the user can adjust the full scale range of the DAC to avoid the non-monotonic transfer characteristic below 100-mV (with respect to ground). This result concludes that an operating range of 700-mV to 100-mV is recommended with an offset voltage (V_{off}) setting of 1.1-V. In addition, the DAC was shown to abide by the derived theoretical transfer function (shown in equation (3.25)). By having knowledge of the output potential of the monolithic bandgap reference (BGR), software can predict the gain error introduced by process variation in the BGR output.

5.2 Future Work

The scope of this work was to design, develop and verify an ASIC for the use as a linear thermal neutron detector data acquisition system. The statistical analysis of this system was not entirely explored across multiple ASICs. This will be coordinated following this work to fully characterize the system performance (throughput and latency), and the optimal event threshold setting (LLD setting). These types of measurements will be required prior to use in the SNS system.

Due to a small amount of noise introduced by the digital circuitry and the system clock, a noise measurement of the system will be conducted to quantify the noise present on the ASIC. The use of the synchronous and asynchronous modes of operation will allow for such a measurement to be obtained.

After the conclusion of the necessary measurements and quantifications of the ASIC, this chip is expected to be used at the Spallation Neutron Source (SNS) laboratory

in Oak Ridge Tennessee. The ASIC is expected to be in its preliminary operation by the latter part of 2008.

Once the additional measurements are conducted, a publication will be written to compile the results of this work for the general public. The publication will be submitted to the Nuclear Science Symposium or the Transactions on Nuclear Science.

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APPENDIX

APPENDIX A

A.1 Serial Programming Interface and System Test Mode

The serial programming interface takes a 99-bit packet—64 bits for the built-in-self-test (BIST) enable (one per channel), 27 bits for all three DACs, and 8 bits for the feedback resistance in the charge sensitive preamp. The first topic covered will be the method in which external digital circuitry can interface the serial input, and the second topic will cover the method in which to utilize the BIST for monolithic channel verification.

A.1.1 Serial Input Specifications

The serial interface is a first-in-first-out memory (FIFO) structure—the most significant bit will be programmed to the bottom register. In this case the bottom register is the BIST enable for channel 63, and therefore it is the first bit of the serial bit stream

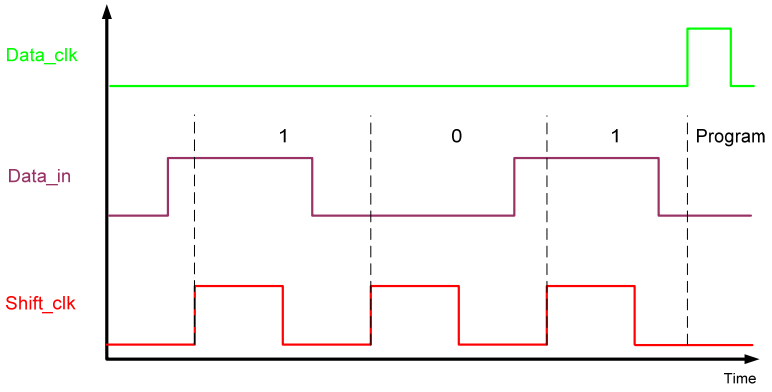
Table A.1 – Serial interface line description

Name	Type	Width	Description
Shift_clk	Input	1	Generic clock to shift bits through the serial registers
Data_in	Input	99	Serial bit stream
Select_data	Input	1	Serial line mode: 1 = Read back 0 = Program
Global_rst	Input	1	Serial register reset 1 = Reset 0 = Active
Data_clk	Input	1	Active program clock for parallel data output
Data_out	Output	1	Serial bit stream output for non-destructive read back

(*data_in*). To write to the serial registers, a clock must be provided (*shift_clk*). In addition, a reset line (*global_rst*) is provided to put the registers into a known state and to clear them of any previous programming. However, the registers will not have to be cleared every time the system is programmed. A non-destructive read back is provided to allow bit error notification. This mode is controlled by a two-port multiplexer, therefore a control line (*select_data*) is provided. After the serial stream is effectively clocked in, a data active clock (*data_clk*) is provided to output the parallel data to the system. A description of the interface lines are provided in Table A.1.

The timing constraints for the serial interface are that the serial data stream (*data_in*) must be stable prior to a rising edge of the serial clock (*shift_clk*). If not followed, bit errors may occur due to metastability in the serial registers. The timing diagram for the serial interface is illustrated in Figure A.1 along with the serial packet.

a)



b)

Figure A.1 – a) Serial interface timing diagram, b) serial bit stream packet order (first in on left)

A.1.2 BIST Operational Description

For rapid yield verification of each specific channel, a monolithic built-in-self-test can be conducted. The BIST mode for the channel under test is enabled through the serial interface by programming a logic '1' to the specific serial register (see Figure A.1 for the serial interface bit packet and section Appendix A.1.1 for writing to the serial interface). The BIST DAC should be programmed such that the channel under test will experience a charge expected from the detector. For this application, the charge expected is 12.8 fC. The BIST includes a monolithic 100 fF capacitor, therefore the voltage required from the DAC is,

$$V_{DAC} = \frac{Q}{C} = \frac{12.8 \times 10^{-15}}{100 \times 10^{-15}} = 128\ mV \qquad \textbf{(A.1)}$$

To discharge this charge into the channel, a control line is provided at the serial interface (*discharge_bar*). To provide a positive input charge, pulse this line from 0V to 3.3V. A negative input charge can be provided by pulsing *discharge_bar* from 3.3V to 0V. Table A.2 provides the theoretical DAC with a given binary word, provided the offset voltage (V_{off}) is set to 1V and the I_{off} bit is set to a logic '1'.

Table A.2 – Theoretical DAC output voltage with a given input word

NOTE: This table was calculated using a BGR voltage equal to 1.25V. For a more accurate table, recalculate using equation (3.25) with the measured BGR value and all constants discussed in chapter 3.

Dec.	Binary	Output (V)	Dec.	Binary	Output (V)	Dec.	Binary	Output (V)
0	0	0.60001	85	1010101	0.40001	171	10101011	0.19766
1	1	0.59765	86	1010110	0.39766	172	10101100	0.19531
2	10	0.5953	87	1010111	0.3953	173	10101101	0.19296
3	11	0.59295	88	1011000	0.39295	174	10101110	0.1906
4	100	0.5906	89	1011001	0.3906	175	10101111	0.18825
5	101	0.58824	90	1011010	0.38825	176	10110000	0.1859
6	110	0.58589	91	1011011	0.38589	177	10110001	0.18354
7	111	0.58354	92	1011100	0.38354	178	10110010	0.18119
8	1000	0.58118	93	1011101	0.38119	179	10110011	0.17884
9	1001	0.57883	94	1011110	0.37883	180	10110100	0.17649
10	1010	0.57648	95	1011111	0.37648	181	10110101	0.17413
11	1011	0.57413	96	1100000	0.37413	182	10110110	0.17178
12	1100	0.57177	97	1100001	0.37178	183	10110111	0.16943
13	1101	0.56942	98	1100010	0.36942	184	10111000	0.16707
14	1110	0.56707	99	1100011	0.36707	185	10111001	0.16472
15	1111	0.56471	100	1100100	0.36472	186	10111010	0.16237
16	10000	0.56236	101	1100101	0.36236	187	10111011	0.16001
17	10001	0.56001	102	1100110	0.36001	188	10111100	0.15766
18	10010	0.55765	103	1100111	0.35766	189	10111101	0.15531
19	10011	0.5553	104	1101000	0.35531	190	10111110	0.15296
20	10100	0.55295	105	1101001	0.35295	191	10111111	0.1506
21	10101	0.5506	106	1101010	0.3506	192	11000000	0.14825
22	10110	0.54824	107	1101011	0.34825	193	11000001	0.1459
23	10111	0.54589	108	1101100	0.34589	194	11000010	0.14354
24	11000	0.54354	109	1101101	0.34354	195	11000011	0.14119
25	11001	0.54118	110	1101110	0.34119	196	11000100	0.13884
26	11010	0.53883	111	1101111	0.33884	197	11000101	0.13649
27	11011	0.53648	112	1110000	0.33648	198	11000110	0.13413
28	11100	0.53413	113	1110001	0.33413	199	11000111	0.13178
29	11101	0.53177	114	1110010	0.33178	200	11001000	0.12943
30	11110	0.52942	115	1110011	0.32942	201	11001001	0.12707
31	11111	0.52707	116	1110100	0.32707	202	11001010	0.12472
32	100000	0.52471	117	1110101	0.32472	203	11001011	0.12237
33	100001	0.52236	118	1110110	0.32236	204	11001100	0.12002
34	100010	0.52001	119	1110111	0.32001	205	11001101	0.11766
35	100011	0.51766	120	1111000	0.31766	206	11001110	0.11531
36	100100	0.5153	121	1111001	0.31531	207	11001111	0.11296
37	100101	0.51295	122	1111010	0.31295	208	11010000	0.1106
38	100110	0.5106	123	1111011	0.3106	209	11010001	0.10825
39	100111	0.50824	124	1111100	0.30825	210	11010010	0.1059
40	101000	0.50589	125	1111101	0.30589	211	11010011	0.10355

Table A.2 - Continued

Dec.	Binary	Output (V)	Dec.	Binary	Output (V)	Dec.	Binary	Output (V)
41	101001	0.50354	126	1111110	0.30354	212	11010100	0.10119
42	101010	0.50119	127	1111111	0.30119	213	11010101	0.098839
43	101011	0.49883	128	10000000	0.29884	214	11010110	0.096486
44	101100	0.49648	129	10000001	0.29648	215	11010111	0.094133
45	101101	0.49413	130	10000010	0.29413	216	11011000	0.091781
46	101110	0.49177	131	10000011	0.29178	217	11011001	0.089428
47	101111	0.48942	132	10000100	0.28942	218	11011010	0.087075
48	110000	0.48707	133	10000101	0.28707	219	11011011	0.084722
49	110001	0.48471	134	10000110	0.28472	220	11011100	0.082369
50	110010	0.48236	135	10000111	0.28237	221	11011101	0.080016
51	110011	0.48001	136	10001000	0.28001	222	11011110	0.077663
52	110100	0.47766	137	10001001	0.27766	223	11011111	0.07531
53	110101	0.4753	138	10001010	0.27531	224	11100000	0.072957
54	110110	0.47295	139	10001011	0.27295	225	11100001	0.070604
55	110111	0.4706	140	10001100	0.2706	226	11100010	0.068252
56	111000	0.46824	141	10001101	0.26825	227	11100011	0.065899
57	111001	0.46589	142	10001110	0.2659	228	11100100	0.063546
58	111010	0.46354	143	10001111	0.26354	229	11100101	0.061193
59	111011	0.46119	144	10010000	0.26119	230	11100110	0.05884
60	111100	0.45883	145	10010001	0.25884	231	11100111	0.056487
61	111101	0.45648	146	10010010	0.25648	232	11101000	0.054134
62	111110	0.45413	147	10010011	0.25413	233	11101001	0.051781
63	111111	0.45177	148	10010100	0.25178	234	11101010	0.049428
64	1000000	0.44942	149	10010101	0.24942	235	11101011	0.047075
65	1000001	0.44707	150	10010110	0.24707	236	11101100	0.044723
66	1000010	0.44472	151	10010111	0.24472	237	11101101	0.04237
67	1000011	0.44236	152	10011000	0.24237	238	11101110	0.040017
68	1000100	0.44001	153	10011001	0.24001	239	11101111	0.037664
69	1000101	0.43766	154	10011010	0.23766	240	11110000	0.035311
70	1000110	0.4353	155	10011011	0.23531	241	11110001	0.032958
71	1000111	0.43295	156	10011100	0.23295	242	11110010	0.030605
72	1001000	0.4306	157	10011101	0.2306	243	11110011	0.028252
73	1001001	0.42825	158	10011110	0.22825	244	11110100	0.025899
74	1001010	0.42589	159	10011111	0.2259	245	11110101	0.023547
75	1001011	0.42354	160	10100000	0.22354	246	11110110	0.021194
76	1001100	0.42119	161	10100001	0.22119	247	11110111	0.018841
77	1001101	0.41883	162	10100010	0.21884	248	11111000	0.016488
78	1001110	0.41648	163	10100011	0.21648	249	11111001	0.014135
79	1001111	0.41413	164	10100100	0.21413	250	11111010	0.011782
80	1010000	0.41178	165	10100101	0.21178	251	11111011	0.0094291
81	1010001	0.40942	166	10100110	0.20943	252	11111100	0.0070762
82	1010010	0.40707	167	10100111	0.20707	253	11111101	0.0047233
83	1010011	0.40472	168	10101000	0.20472	254	11111110	0.0023704
84	1010100	0.40236	169	10101001	0.20237	255	11111111	1.75E-05
85	1010101	0.40001	170	10101010	0.20001			

A.2 Interfacing the Dynamic Digital Output

The timing diagram for the dynamic digital output is shown in Figure A.2. This interface is for normal data acquisition operation. The *Channel ID* will be an LVDS standard 6-bit output. This data must be registered externally prior to any system reset. The *HIT* line is a 1-bit valid data flag. Once received, the interface system must respond with a reset command in an LVDS standard at port *Rst_FPGA*. The clock is to be 10 MHz, and provided as an LVDS standard signal. This interface is classified as a simple "handshake" protocol.

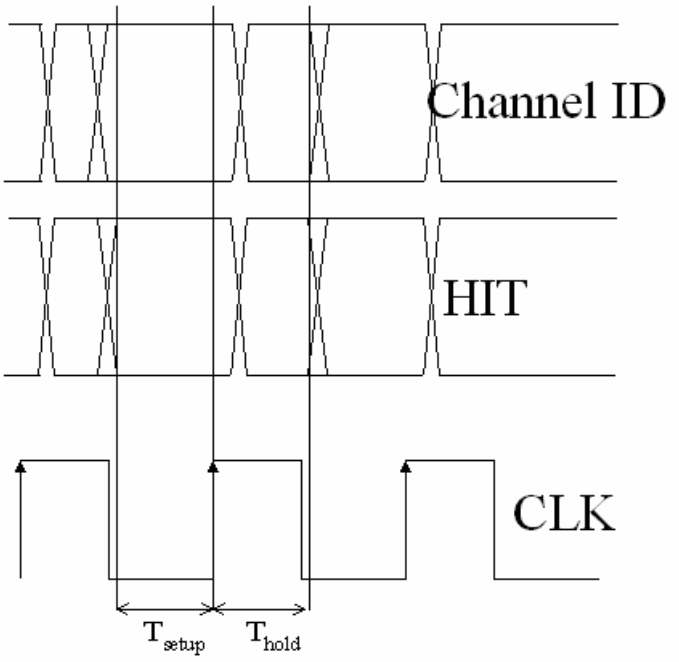


Figure A.2 – Timing diagram for the dynamic digital data output

A.3 Patara III Pin-Out Diagram and Description

Table A.3 – Patara III pin-out description

NOTE: Yellow highlighted pins are for the test structures.

Pin(s)	Function	Description
1-64	**Qin_1-64**	Charge inputs for all 64 channels where *channel 0 is of highest priority* and *channel 63 is of lowest priority*.
65,67,92, 120,172,174, 199,224,226	**PVDD_ANLG**	3.3V supply for the ANALOG pads and ESD protection
66,68,93,119, 173,175, 198, 223,225	**PGND_ANLG**	ANALOG ground for pad and ESD protection
69,70,221, 222	**VDD_cal**	3.3V supply for the Built-in-self-test circuitry
71,72,219, 220	**VSS_cal**	Ground connection for the Built-in-self-test circuitry
73,74,217, 218	**VDD_pre**	3.3V supply for the Preamp circuitry
75,76,100, 101,105,106, 185,186,215, 216	**VSS_anlg**	ANALOG ground for all internal analog circuitry
77	**Discharge_bar**	Event trigger for the BIST circuitry. Switch from 0V to 3.3V for a positive polarity charge on the input of the channel after system programming
78,168	**Data_out**	Serial register output.
79	**Global_rst**	Reset line for the serial registers. Switch to 3.3V for register reset
80	**Shift_clk**	Serial register clock input. Rising edge is the active edge for the registers
81	**Ibias_preamp**	Current bias for preamp input. Set to 20μA via a 47.5 kΩ pull down resistor
82	**Ibias_curs**	Test point for preamp current sources
83	**Vref**	Offset voltage for preamp input polarity selection. Set to 2V for charge pulse into the channel. Set to 1.5V for charge pulse out of the channel
84	**Vbias_op amp**	Positive op amp input voltage. Set to 1.6V
85	**Ibias_op amp**	Current bias for op amp input. Set to 20μA via a 115 kΩ pull down resistor
86	**Op amp_select_ch63**	Spy point enable line for the Op amp output in channel 63. Switch to 3.3V to allow signal transmission. Keep at 0V under normal system operation.
87	**Op amp_ch63**	Op amp output in channel 63. Must be enabled prior to observing any waveform.

Table A.3 - Continued

Pin(s)	Function	Description
88	**Preamp_select_ch63**	Spy point enable line for the preamp output in channel 63. Switch to 3.3V to allow signal transmission. Keep at 0V under normal system operation.
89	**Preamp_ch63**	Preamp output in channel 63. Must be enabled prior to observing any waveform.
90	**Comp_bar**	Baseline restorer reset. BLR loop is closed when $\overline{\textbf{RESET}}$ is 0V
91	**Comp**	Baseline restorer reset. BLR loop closed when **RESET** is 3.3V
94	**Blr_on**	Turns the BLR on or off. BLR is on when set to 3.3V
95	**Voff_gbl**	Shaper DC input voltage. Active when BLR is off, ignored when BLR is on. Always set to 1.6V.
96	**Pos_on**	Baseline restorer polarity. Set to 3.3V for positive input
97	**Ibi_1**	V-to-I converter bias current. Set to 100μA via 23.2 kΩ pull up resistor
98	**Ibi_2**	Complex conjugate filter bias current. Set to 10μA via a 243 kΩ pull down resistor
99	**Ibi_3**	Baseline restorer bias current. Set to 10μA via a 2.2 MΩ pull up resistor
102, 103, 188, 189	**VDD_Shape**	Shaper circuitry supply rail. Set to 3.3V
104	**Blr_pol**	Shaper input polarity. Set to 3.3V for positive input
107, 108, 183, 184	**VDD_compar**	Comparator circuitry supply rail. Set to 3.3V
109	**Shaper_select_ch63**	Spy point enable line for the Shaper output in channel 63. Switch to 3.3V to allow signal transmission. Keep at 0V under normal system operation.
110	**Shaper_ch63**	Shaper output in channel 63. Must be enabled prior to observing any waveform.
113, 114, 163, 164	**VDD_dig**	Digital circuitry supply rail. Set to 3.3V
112, 113, 165, 166	**VSS_dig**	Ground terminal for the digital circuitry
115	**Ibias_compar**	Bias current for the comparators. Set to 20 μA via a 120 kΩ pull up resistor
116	**Compar_S2**	Discrimination level for the second comparator. Set nominally to 100 mV or below the hit threshold level
117	**Compar2_select_ch63**	Spy point enable line for the second Comparator output in channel 63. Switch to 3.3V to allow signal transmission. Keep at 0V under normal system operation.
118	**Compar2_ch63**	Second comparator output in channel 63. Must be enabled prior to observing any waveform.
121	**Shaper_select_ch62**	Spy point enable line for the Shaper output in channel 62. Switch to 3.3V to allow signal transmission. Keep at 0V under normal system operation.

Table A.3 - Continued

Pin(s)	Function	Description
122	**Shaper_ch62**	Shaper output in channel 62. Must be enabled prior to observing any waveform.
125, 126	**VDD_clk**	Clock shielding well contract. Tie to 3.3V
127, 128, 138, 148	**VDD_LVDS**	LVDS transmitter/receiver supply rail. Set to 3.3V
129, 130, 139, 149	**VSS_LVDS**	Ground terminal for the LVDS circuitry
131	**Ibias_LVDS**	Bias current for the LVDS transmitters. Set to 1.75 mA via 1.24 kΩ pull down resistor
132	**Valid_hit_neg**	Negative output terminal of the LVDS standard valid data flag
133	**Valid_hit_pos**	Positive output terminal of the LVDS standard valid data flag
134	**Y5_neg**	Negative output terminal of the LVDS standard channel ID bit 5
135	**Y5_pos**	Positive output terminal of the LVDS standard channel ID bit 5
136	**Y4_neg**	Negative output terminal of the LVDS standard channel ID bit 4
137	**Y4_pos**	Positive output terminal of the LVDS standard channel ID bit 4
140	**Y3_neg**	Negative output terminal of the LVDS standard channel ID bit 3
141	**Y3_pos**	Positive output terminal of the LVDS standard channel ID bit 3
144	**Y2_neg**	Negative output terminal of the LVDS standard channel ID bit 2
145	**Y2_pos**	Positive output terminal of the LVDS standard channel ID bit 2
146	**Y1_neg**	Negative output terminal of the LVDS standard channel ID bit 1
147	**Y1_pos**	Positive output terminal of the LVDS standard channel ID bit 1
150	**Y0_neg**	Negative output terminal of the LVDS standard channel ID bit 0
151	**Y1_pos**	Positive output terminal of the LVDS standard channel ID bit 0
152	**BGR_in_LVDS**	Input terminal for the LVDS common mode level. Short to pin 153 if the BGR is functioning properly otherwise provide a 1.25V reference
153	**BGR_out_LVDS**	BGR output reference for the LVDS common mode level. Short to pin 152 if the reference is functioning properly, otherwise leave open
154	**BGR_en_LVDS**	Enable line for the BGR reference dedicated to the LVDS common mode level. Set to 3.3V to enable

Table A.3 - Continued

Pin(s)	Function	Description
155	**Bias_R4B_BGR_LVDS**	RHIC4B bias current for the BGR dedicated to the LVDS common mode level. There is an on-chip resistor so provide a 100 kΩ resistor to VDD to increase the bias current.
156	**Select_dig**	Control line for the synchronous and asynchronous digital systems. Set to 0V for the synchronous system.
157	**Loop_rst**	Feedback look reset signal for the synchronous system. Prove a 3.3V pulse if undesirable behavior is detected
158	**Ibias_rcvr**	LVDS receiver bias current. Set to 100 μA via a 22.6 kΩ pull down resistor
159	**Rst_FPGA_minus**	Negative input terminal for the LVDS standard system reset line
160	**Rst_FPGA_plus**	Positive input terminal for the LVDS standard system reset line
161	**Clk_minus**	Negative input terminal for the LVDS standard 10 MHz clock line
162	**Clk_plus**	Positive input terminal for the LVDS standard 10 MHz clock line
167	**Select_data**	Serial input mode select. Set to 0V for serial programming and 3.3V for serial readback
169	**Data_clk**	Serial input control line for outputting the parallel data. Pulse to 3.3V after serial data has been registered
176	**Data_in**	Serial data input. This line is similar to that of a FIFO. The first bit in will be programmed to the last register
177	**Ibias_R4B_DAC**	Current bias for the RHIC4B op amp in the DACs. Set to 12.5 μA via a 200 kΩ pull up resistor
178	**S1_DAC_sum**	Current summing node of the DAC dedicated to the event threshold. Can provide or steal current from the DAC to calibrate.
179	**S1_DAC_out**	Output of the DAC dedicated to the event threshold. Short to pin 180 if functioning properly, otherwise leave open
180	**S1_DAC_in**	Input terminal for the event threshold level. Short to pin 179 if DAC is operating properly, otherwise provide an external reference
181	**Compar2_select_ch0**	Spy point enable line for the second Comparator output in channel 0. Switch to 3.3V to allow signal transmission. Keep at 0V under normal system operation.
182	**Compar2_ch0**	Second comparator output in channel 0. Must be enabled prior to observing any waveform.
187	**Shaper_select_ch1**	Spy point enable line for the Shaper output in channel 1. Switch to 3.3V to allow signal transmission. Keep at 0V under normal system operation.
192	**Shaper_ch1**	Shaper output in channel 1. Must be enabled prior to observing any waveform.

Table A.3 - Continued

Pin(s)	Function	Description
193	**Shaper_select_ch0**	Spy point enable line for the Shaper output in channel 0. Switch to 3.3V to allow signal transmission. Keep at 0V under normal system operation.
194	**Shaper_ch0**	Shaper output in channel 0. Must be enabled prior to observing any waveform.
195	**BGR_in_DAC**	Input terminal for the DAC voltage bias. Short to pin 196 if the BGR is functioning properly otherwise provide a 1.25V reference
196	**BGR_out_DAC**	BGR output reference for the DAC voltage bias. Short to pin 195 if the reference is functioning properly, otherwise leave open
197	**BGR_en_DAC**	Enable line for the BGR reference dedicated to biasing the DAC. Set to 3.3V to enable
200	**Bias_R4B_BGR_DAC**	RHIC4B bias current for the BGR dedicated to the DAC voltage bias. There is an on-chip resistor so provide a 100 kΩ resistor to VDD to increase the bias current.
201	**Preamp_select_ch0**	Spy point enable line for the preamp output in channel 0. Switch to 3.3V to allow signal transmission. Keep at 0V under normal system operation.
202	**Preamp_ch0**	Preamp output in channel 0. Must be enabled prior to observing any waveform.
203	**Vblr_DAC_sum**	Current summing node of the DAC dedicated to the BLR level. Can provide or steal current from the DAC to calibrate.
204	**Vblr_DAC_out**	Output of the DAC dedicated to BLR level. Short to pin 180 if functioning properly, otherwise leave open
205	**Vblr_DAC_in**	Input terminal for the event threshold level. Short to pin 179 if DAC is operating properly, otherwise provide an external reference
206	**Op amp_select_ch0**	Spy point enable line for the Op amp output in channel 0. Switch to 3.3V to allow signal transmission. Keep at 0V under normal system operation.
207	**Op amp_ch0**	Op amp output in channel 0. Must be enabled prior to observing any waveform.
208	**Ibias_R4B_LSB**	RHIC4B current bias for the LSB current reference in the DAC. Set to 5 μA via a 536 kΩ pull down resistor
209	**Voff_DAC**	Offset voltage for all on-chip DACs. Provide a 1-V reference with trimming ability so the DAC can be calibrated
210	**Sw_ctrl**	Preamp gain selection switch. Set to 3.3V for normal gain. Set to 0V for ½ gain

Table A.3 - Continued

Pin(s)	Function	Description
211	**Startup**	Low level current source startup pin. Needed to ensure proper startup of current source circuit. Apply 3.3V pulse if evidence of improper operation when powered on.
212	**Cal_DAC_sum**	Current summing node of the DAC dedicated to the BIST voltage reference. Can provide or steal current from the DAC to calibrate.
213	**Cal_DAC_out**	Output of the DAC dedicated to the BIST voltage reference. Short to pin 214 if functioning properly, otherwise leave open
214	**Cal_DAC_in**	Input terminal for the BIST voltage reference. Short to pin 213 if DAC is operating properly, otherwise provide an external reference

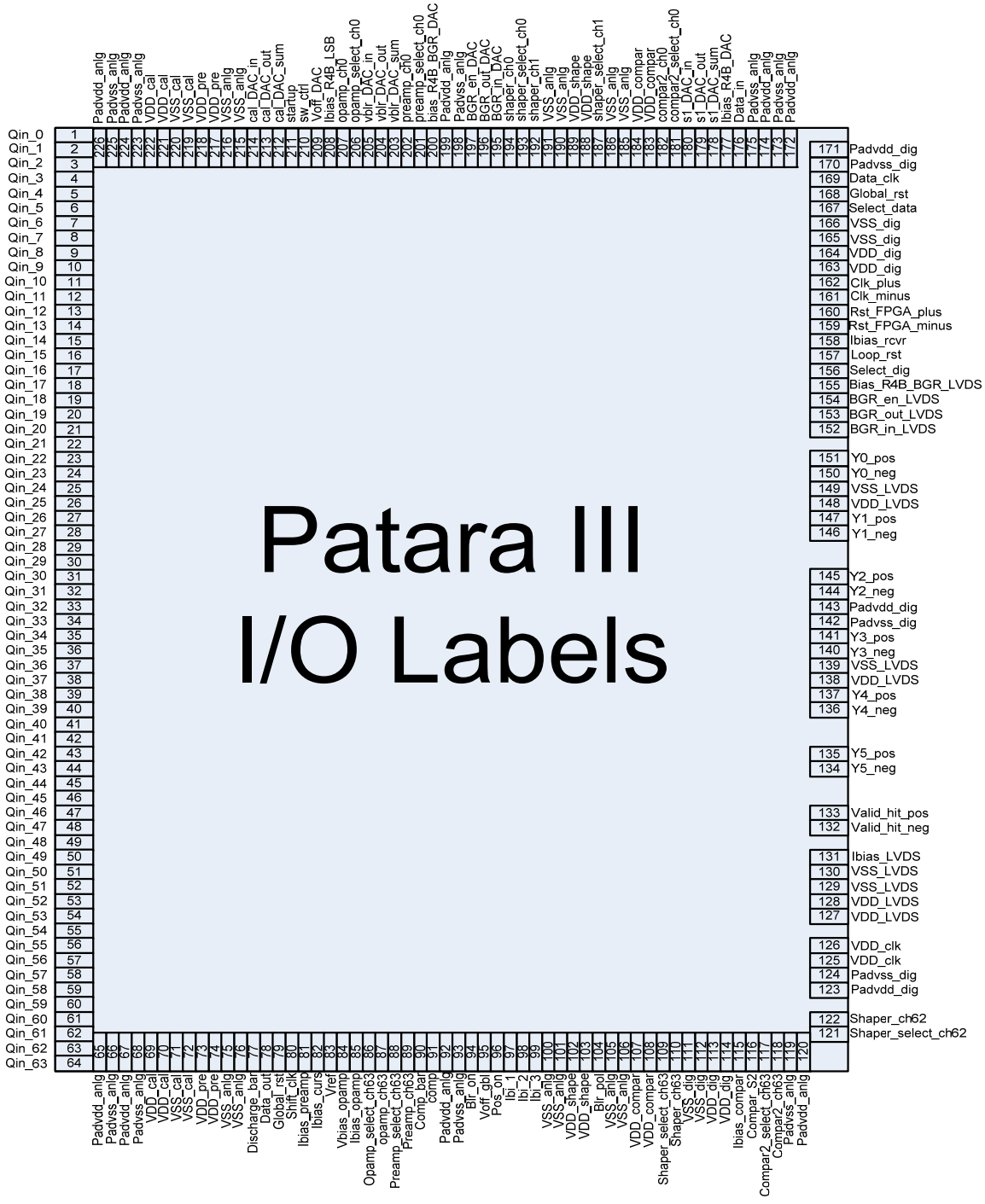


Figure A.3 – Patara III ASIC pinout diagram

APPENDIX B

B.1 Motherboard

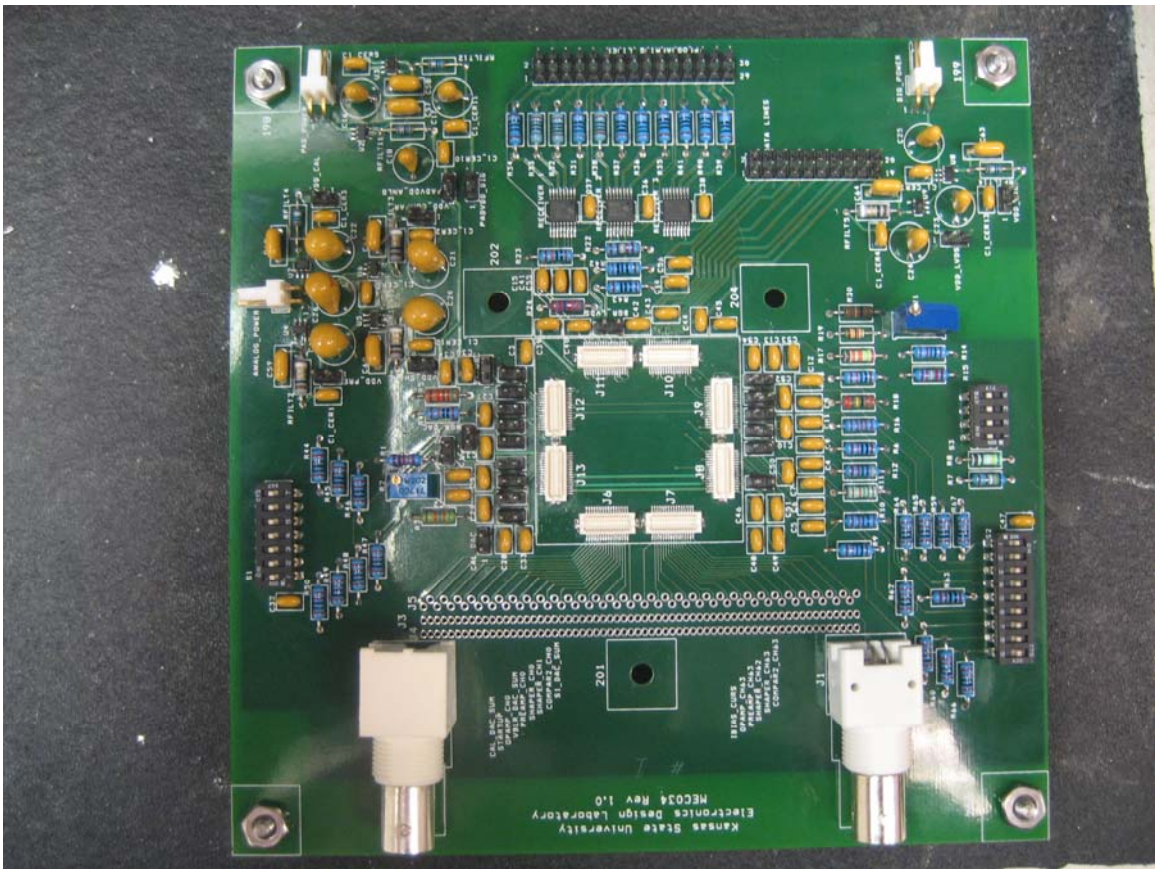


Figure B.1 – Motherboard used for system verification

Table B.1 – Motherboard dip switch descriptions

S1 Pin description and user settings

Pin Number	Description	Open	Closed
1	Spy point control for the second comparator in channel 0	Disabled	Enabled
2	Spy point control for the shaper in channel 1	Disabled	Enabled
3	Spy point control for the shaper in channel 0	Disabled	Enabled
4	BGR output control for the DACs	Disabled	Enabled
5	Spy point control for the preamp in channel 0	Disabled	Enabled
6	Spy point control for the op amp in channel 0	Disabled	Enabled
7	Preamp gain selection switch	1/2 gain	Full gain

S2 Pin description and user settings

Pin Number	Description	Open	Closed
1	BGR output control for the LVDS transmitters	Disabled	Enabled
2	Spy point control for the shaper in channel 62	Disabled	Enabled
3	Spy point control for the second comparator in channel 63	Disabled	Enabled
4	Spy point control for the shaper in channel 63	Disabled	Enabled
5	Shaper input polarity control	Negative Pol.	Positive Pol.
6	Baseline restorer polarity control	Negative Pol.	Positive Pol.
7	BLR enable/disable	Disabled	Enabled
8	Spy point control for the preamp in channel 63	1/2 gain	Full gain
9	Spy point control for the op amp in channel 63	1/2 gain	Full gain

Table B.1 - Continued

S3 Pin description and user settings

Pin Number	Description	Open	Closed
1	Offset voltage control for the preamp.	Negative Pol.	Positive Pol.
2	Shaper DC input voltage. Will reference 1.6V or 1V.	1 V	1.6 V
3	No Connect	X	X
4	No Connect	X	X

B.2 Daughter Card and ASIC

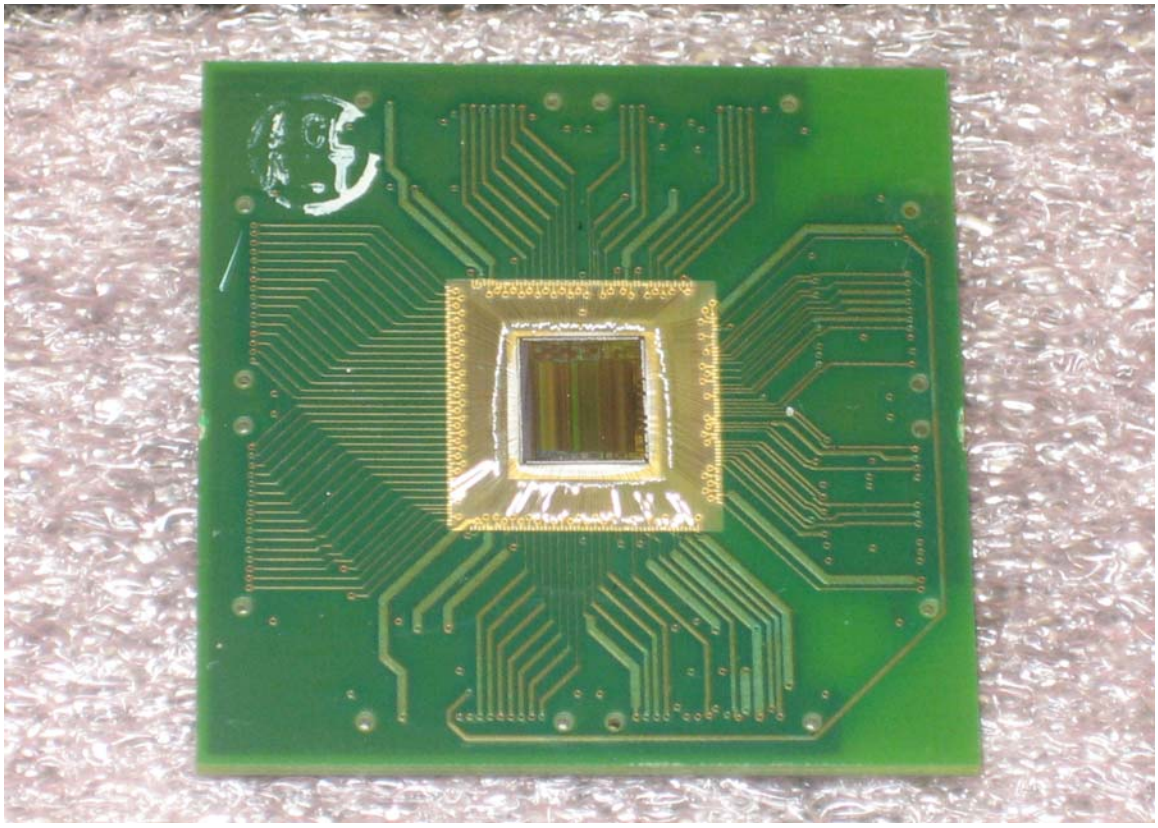


Figure B.2 – Developed daughter card and Patara III ASIC

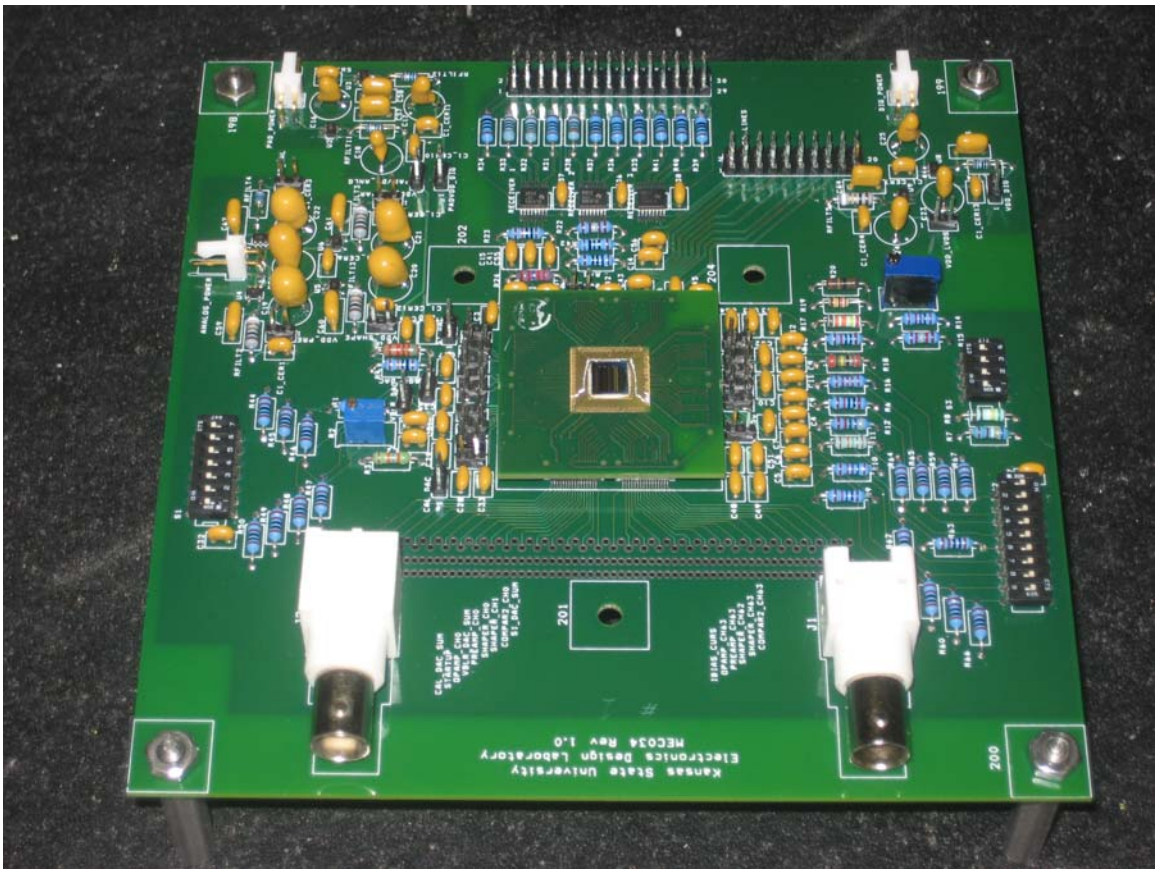


Figure B.3 – Daughter card and motherboard

B.3 Interface Card and Virtex 4 Board

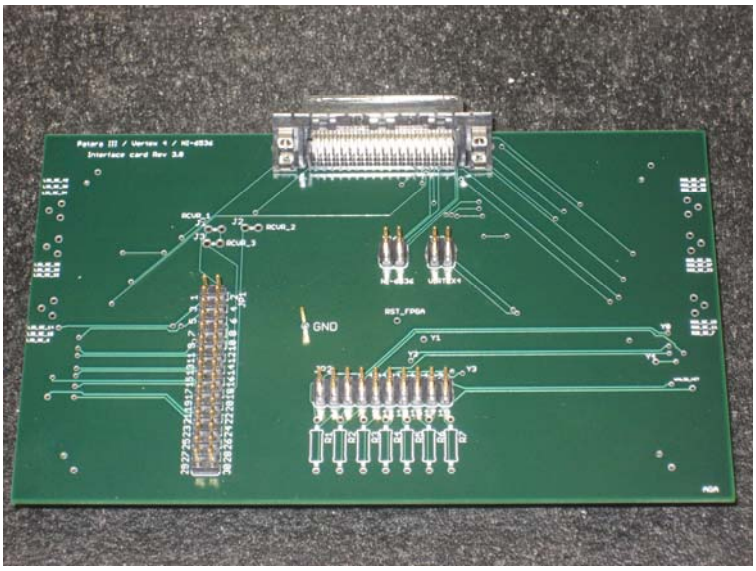


Figure B.4 – Interface card for the Motherboard/Virtext4/NI-6536 (top)

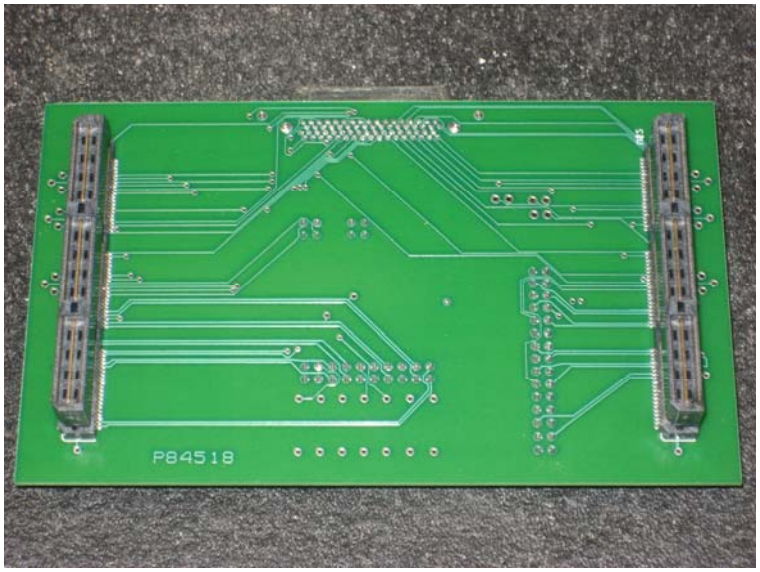


Figure B.5 – Interface card for the Motherboard/Virtext4/NI-6536 (bottom)

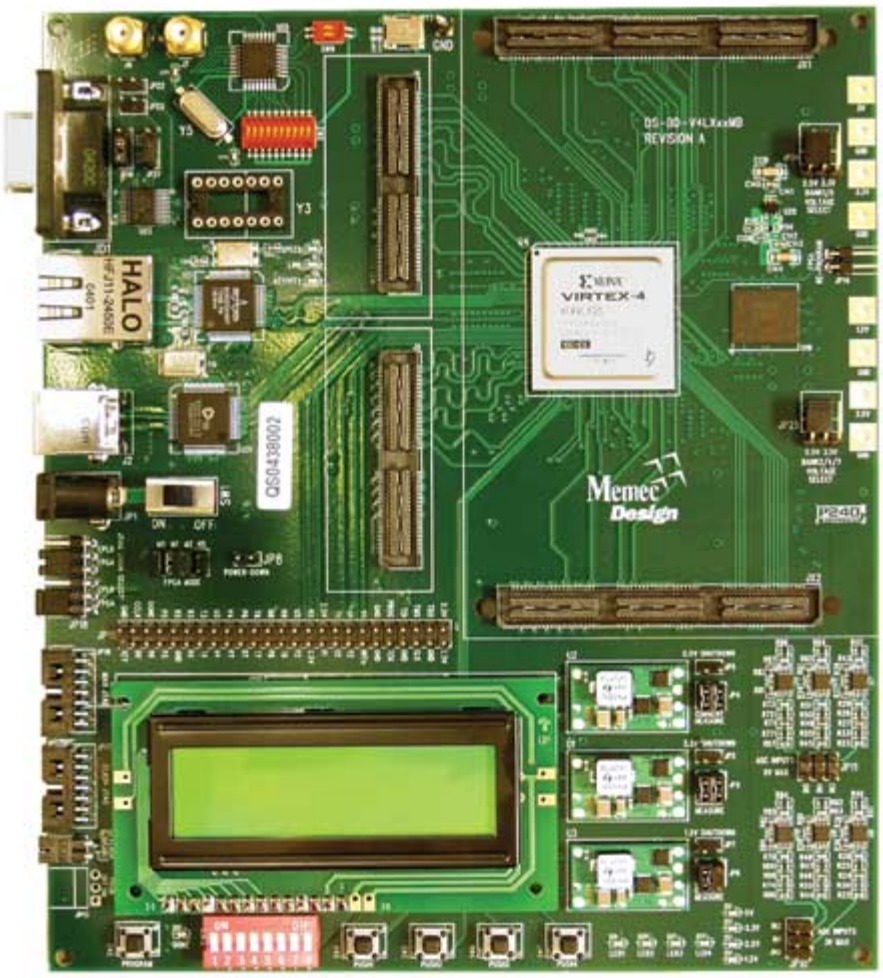


Figure B.6 – Virtex 4 development board (Part # DS-KIT-4VLX60MB-G)

Table B.2 – Interface card I/O details and Virtex-4/NI-6536 locations

Net	NI-6536 Location	Virtex-4 (To P3) Location	Virtex-4 (To NI) Location	Description
Select_Data	DIO_31	H22 (Pos) H21 (Neg)	H26	Selects between serial interface programming or non-destructive read-back.
Blr_comp_bar	No Interface	G19 (Pos) F19 (Neg)	No Interface	BLR loop negative reset switch.
Blr_comp	No Interface	E21 (Pos) D21 (Neg)	No Interface	BLR loop positive reset switch.
Select_dig	DIO_28	H20 (Pos) G20 (Neg)	G25	Selects between the synchronous and asynchronous system.
Sys_reset	DIO_27	C21 (Pos) B21 (Neg)	F26	Serial interface register reset.
NI_led	DIO_26	K26 (on board led)	E26	Connectivity LED indicator for the NI-6536 and the Virte-4 board.
Shift_clk	DIO_25	E17 (Pos) F17 (Neg)	E25	Serial interface register clock.
Data_in	DIO_24	F18 (Pos) E18 (Neg)	D26	Data input for the serial interface.
Data_clk	DIO_23	F20 (Pos) E20 (Neg)	D25	Program clock for the serial interface.
Discharge_bar	DIO_22	D22 (Pos) C22 (Neg)	C26	Discharge clock for the BIST.
EN_rcvr1	DIO_21	D16	C25	LVDS receiver 1 enable line for the P3 motherboard.
EN_rcvr2	DIO_20	D15	B24	LVDS receiver 2 enable line for the P3 motherboard.
EN_rcvr3	DIO_19	D14	A24	LVDS receiver 3 enable line for the P3 motherboard.
Y0	DIO_18	V21 (Pos) V22 (Neg)	B23	Bit 0 of the channel ID from P3
Y1	DIO_17	AA19 (Pos) AA20 (Neg)	W26	Bit 1 of the channel ID from P3
Y2	DIO_16	AC23 (Pos) AC24 (Neg)	W25	Bit 2 of the channel ID from P3
Y3	DIO_15	AA18 (Pos) Y18 (Neg)	Y26	Bit 3 of the channel ID from P3

Table B.2 - Continued

Net	NI-6536 Location	Virtex-4 (To P3) Location	Virtex-4 (To NI) Location	Description
Y4	DIO_14	AC22 (Pos) AB22 (Neg)	Y25	Bit 4 of the channel ID from P3
Y5	DIO_13	AF24 (Pos) AE24 (Neg)	AA26	Bit 5 of the channel ID from P3
Valid_hit	No Interface	AB20 (Pos) AC20 (Neg)	No Interface	Valid channel ID data from P3 to the virtex-4.
NI_read_data	DIO_12	No Interface	AB26	Data flag from the virtex-4 to the NI-6536.
NI_done	DIO_11	No Interface	AB25	Acknowledge handshake from the NI-6536 to the virtex-4.
Master_reset	DIO_10	Y20 (Pos) Y21 (Neg)	AC26	Will overide rst_fpga for a master reset of the P3 registers. Otherwise rst_fpga is dynamic.
NI_single	DIO_7	No Interface	AD26	Allows control of dicharge_bar for the BIST when high.
NI_cont	DIO_6	No Interface	W20	Outputs a 1kHz square wave on the discharge_bar line when high.
NI_BIST_count	DIO_5	No Interface	AD25	Counts the generated event signal for the BIST from the FPGA.
NI_sync	DIO_2	No Interface	NI-6536 Header Pin 2	External connection from the sync port of the signal generator to allow for edge counting.
clk	No Interface	Y17 (Pos) AA17 (Neg)	No Interface	10 MHz system clock.
data_led	No Interface	N25 (on board led)	No Interface	Active communication LED indicator between P3 and virtex-4.
led1	No Interface	V25 (on board led)	No Interface	Active communication LED indicator between NI-6536 and virtex-4.

VITA

Anthony Gene Antonacci (Tony) was born in San Diego, CA on April 28th, 1983. He was born and raised in Carlsbad and Del Mar, CA where he graduated from Torrey Pines High School in 2001. Tony then entered the University of Tennessee in August 2001 to pursue an Engineering degree. After his freshman year, he decided that Electrical Engineering would best fit his interests and career goals. During his undergraduate degree, he interned for National Instruments in Austin, TX in the Analog R&D department. It was here that he realized his passion for analog related design.

In the spring semester of 2006, Tony entered into the Master of Science program at the University of Tennessee emphasizing in mixed signal solid state electronics. During this time he held a position as a graduate research assistant to Dr. Benjamin Blalock in the Integrated Circuits and Systems Laboratory (ICASL). Within this research group, Tony was awarded the opportunity to work with Dr. Charles Britton, Jr. and Dr. Nance Ericson from the Oak Ridge National Laboratory on a project funded by the National Science Foundation (NSF) while fulfilling his research requirements for his master's degree.

After conferral of his Master's degree, he will be working with Texas Instruments in the Portable Power Management group in Dallas, TX.