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Design and Implementation of a High Temperature Fully-Integrated BCD-on-SOI Under Voltage Lock Out Circuit

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To the Graduate Council:

I am submitting herewith a thesis written by Nora Dianne Bull entitled "Design and Implementation of a High Temperature Fully-Integrated BCD-on-SOI Under Voltage Lock Out Circuit." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Syed Islam, Major Professor

We have read this thesis and recommend its acceptance:

Benjamin Blalock, Ethan Farquhar

Accepted for the Council:
Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

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Design and Implementation of a High Temperature Fully-Integrated BCD-on-SOI Under Voltage Lock Out Circuit

A Thesis
Presented for the
Master of Science
Degree
The University of Tennessee, Knoxville

Nora Dianne Bull
December 2009

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Dedication

This thesis is dedicated to Thomas and Beverly Bull, my parents. They have always supported and encouraged me in every way. I owe much of my success to them.

Acknowledgments

Several people were a large influence on my work and I would like to acknowledge these individuals.

First, I would like to acknowledge Dr. Syed Islam for his continuous support and guidance as both an undergraduate and graduate student. With a great deal of patience, he has helped me to grow professionally and personally.

Also, I would like to acknowledge Dr. Benjamin Blalock and Dr. Ethan Farquhar. They were exceptional mentors and contributed to me having a wonderful experience at the University of Tennessee.

Additionally, I would like to thank Dr. Charles Britton for his help with the design of this circuit. Without his guidance I would not be where I am today.

Also, I would like to thank the members of the Analog & Mixed Signal VLSI and Devices Laboratory and the members of the Integrated Circuits and Systems Laboratory. Their continuing support and assistance has allowed me to finish my masters work.

Finally, I would like to thank my family and friends for their support and love.

Abstract

As concern about the environment has grown in recent years, alternatives in the automotive industry have become an important topic for researchers. One alternative being considered is electric vehicles, which utilize electric motors. DC/AC inverters and DC/DC power converters control these electric motors. A logic circuit is needed to power these converters; however, the logic generators inherently operate at a voltage too low to power the motors. A device known as the gate driver is the interface between the logic generators (or microcontroller) and the power devices (power converter). The gate driver provides the power needed to drive the power devices. Circuits are susceptible to voltage and temperature changes though. For this reason, protection circuits must be implemented as an integral part of the gate driver circuits. The Under Voltage Lock Out (UVLO) circuit provides important detection of under voltage conditions in the power supply thus preventing malfunctions. There are multiple power supplies in the gate driver circuit, and it is important to monitor all of these supplies for both surges and reductions in power. If the power supply should drop below the threshold (nominally 80%) there could be issues in the gate driver's functionality. Since the gate driver will be located under the hood of a hybrid electric vehicles, operating temperatures can reach extremely high values. For this reason, circuit designs must provide reliable operation of the circuits in an extreme environment.

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Chapter 1

Introduction

1.1 Under Voltage Lock Out Circuits

Electric vehicles utilize battery sources and electric motors to decrease the need for petroleum-fueled transportation. They also need several electronic components to make the transition of energy from battery to drive system. An important design consideration for any electronic circuits powered by batteries is how the system behaves in conditions when the supply voltage dips to a level that may cause undesired operations for other critical circuits [1]. Control circuitry provides under voltage lock out (UVLO) to ensure protection against supply voltages that have not been stabilized [2]. Under voltage lock out circuits are used to monitor the power supply to circuits whose functionality is critically based on the supply voltage. Often times, a UVLO will use a reference voltage for comparison with the supply voltage. The environmental conditions of the UVLO are very important to consider. Since the gate driver is placed in close proximity to an automotive engine, the operating temperature of the circuit has a very large range. For this reason, a look at high temperature devices is important.

1.2 Outline of the Thesis

Relevant literature is reviewed including electric vehicles, gate driver circuits, high temperature electronics, and other UVLO circuits. Next, the overall UVLO circuit topology and the individual UVLO circuits are discussed. Also the comparators within each UVLO circuit are reviewed. Finally, simulations and test results prove that the UVLO is functional and meets the needed requirements.

Chapter 2

Literature Review

2.1 Electric Vehicles

Due to high demand and rising cost of petroleum, the demand for electric vehicles or vehicles with high-power electric motor drives will increase in the near future. The electronics within an electric car must be reliable at high temperatures and need to be low-cost. Three technologies are being considered for a greener automotive industry. First, the leading technology is the hybrid-electric vehicle (HEV) because of its better performance and fuel economy. HEVs use internal combustion engines (ICEs) along with electric motors to improve the performance of the vehicle. Figure 2-1 illustrates the topology of a HEV system. Next, plug-in-hybrids (PHEV) use rechargeable battery packs but can only travel short distances due to the lack of ICEs. Finally, fuel-cell vehicles (FCV) generate their own electricity and could someday completely replace ICEs [3].

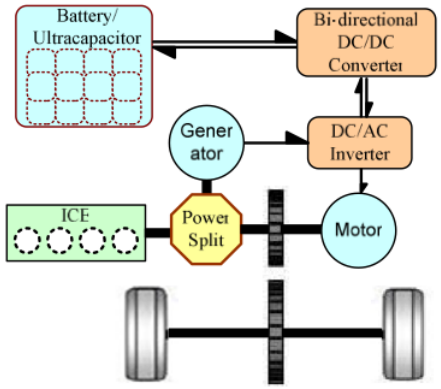

Figure 2-1: Typical Topological Arrangement of A Series/Parallel HEV [3]

2.2 Gate Drivers

Gate driver circuits can be used with microcontrollers in a HEV system. The ON and OFF operations of the power switch control the flow from the source to the load of the power converter. The ON/OFF efficiency directly impacts the performance of the system. Usually, these pulses are generated by a microcontroller, but it is unable to meet the power requirements needed to drive the gate of the power switch. This is due to the lack of current driving capability to charge and discharge the gate capacitance fast enough to minimize the switching losses. Previous research has not developed a gate driver circuit that can meet both the temperature needs as well as the drive needs for the power switch.

A block diagram of the gate driver circuit meeting both temperature and power requirements is displayed in Figure 2-2. This circuit has seven critical building blocks, namely a half-bridge high-voltage output stage (transistor pair M_H and M_L), low-side and high-side buffers, an on-chip bootstrap capacitor based charge pump, constant current bias low-side to high-side level shifters, a temperature independent dead-time controller, an edge detection circuit, and an input stage [4]. V_{DD} is a 5V source that comes from the output of a voltage regulator; it is actually a voltage swing of V_{SSH_LV} + 5V. V_{SSH_LV} is the lower rail for the low side of the gate driver and is connected on board to V_{SS_HV}. V_{OP_PLUS} is the output of the charge pump that powers the high side of the gate driver. V_{OP} is the output of the gate driver. Notice the UVLO input along with the other protection devices. The gate driver was implemented in a 0.8-micron, 2-poly, and 3-metal Bipolar-CMOS-DMOS (BCD) on Silicon-on-Insulator (SOI) process. Previous versions have been tested and were successful at the ambient temperature of 200°C.

The input stage of the gate driver uses a digital network to compare the logic input and the protection circuits (temperature sensor, UVLO, and short circuit detector). If any of these signals is zero (indicating a fault in the system), the output of the gate driver will be 'low' and the power switch will be turned OFF. On the high-side of the gate driver, there is a charge pump as well as an S/R latch and the buffer circuit. In the charge pump, there is a bootstrap capacitor (C_B) that establishes the voltage V_{OP_PLUS}. The input of the S/R latch comes from the bias level shifter. The output of the S/R latch feeds into the buffer circuit. This buffer circuit drives one input of the output stage.

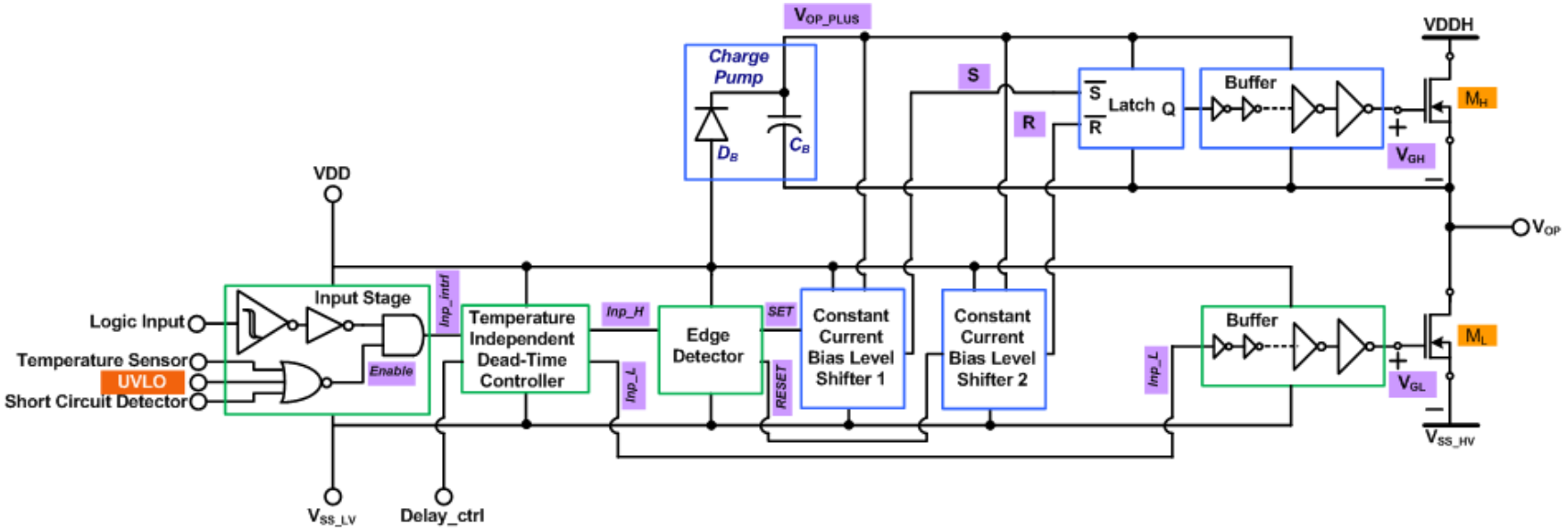

Figure 2-2: Gate Driver Circuit Topology[4]

On the low-side of the gate driver there is a dead-time controller, an edge detector, two bias level shifters, and a buffer. The dead-time controller ensures the complementary ON/OFF operation of the output stage through 'inp_L' and 'inp_H' with dead-time injection between them. The edge detector outputs a 'Set' and a 'Reset' signal depending on the input 'inp_H'. These 'Set' and 'Reset' signals then feed into the two bias level shifters. Bias Level Shifter 1 outputs a voltage level shifted copy of the 'inp_H' (S) signal, and Bias Level Shifter 2 outputs a voltage level shifted copy of 'inp_H' (R), both feeding to the S/R latch in the high-side. The output 'inp_L' is fed into a buffer that drives the output stage. The output stage is an all-NMOS transistor half-bridge that handles the large drive requirement of the driver circuit. In order to safely create a reliable output stage, many 45V devices are connected in parallel. The buffer circuits on the high-side and low-side of the gate driver drive the large capacitances at the gate terminals of the switch transistors.

Many devices depend on an accurate power supply for correct functionality. The gate driver of an electric car is one of the devices that need a dependable power source. For this reason, protection circuits like short circuit protection and under voltage lock out circuits are implemented as part of the gate driver circuit.

2.3 High Temperature Devices

Extreme environment devices have to withstand high temperatures. People are often surprised to hear about MOS circuits operating at temperatures exceeding 250°C. Devices operating in that range are not widely known because commercial vendors rarely provide information about components beyond the military range (125°C typically), a very small percentage of the IC market has a demand for high temperature circuits, and textbooks typically lack information about the behavior of MOSFET parameters at high temperatures [5].

Tests have been performed on standard circuit topologies at room temperature (25°C) and 250°C. Test results of the large signal parameter effects conclude that the magnitude of the threshold voltage decreases by approximately 0.5V as the temperature is increased. The average effective mobility is reduced by half. The leakage currents are increased by 5 orders of magnitude [5]. Test results of the small signal parameter effects conclude that the transconductance is reduced by half as the temperature is increased to 250°C. The body-effect conductance is also reduced by half. The leakage conductance increases by 5 orders of magnitude and the junction capacitance increases

anywhere from 5% to 50% [5].

While some applications work with commercial components, others have had to accomodate much larger temperature ranges. For space exploration, temperatures can range anywhere from -220°C to 470°C. The maximum working temperature for semiconductors can be estimated from their intrinsic carrier density, which depends on the bandgap of the material [6]. For high voltage devices on silicon (Si) with a voltage source below 100V, the theoretical limit is 250°C as discussed above. Silicon-on-Insulator (SOI) devices are capable of operating up to 300°C [6]. This temperature characteristic makes SOI a great option for the gate driver designers. The ability of the SOI chip to operate at such high temperatures is due to its inherently low leakage current and immunity to latch-up [3]. The low leakage current is an effect of the buried insulator layer. One option for circuits that need to operate across a large temperature range is to create a reconfigurable chip. Reconfigurable chips provide a platform for a large number of topologies to be programmed. When one topology deteriorates at high temperatures, the higher temperature topology takes over [6]. Reconfigurability was not an option for the gate driver's UVLO on account of space constraints.

One of the more crucial problems in electronics is the reliability of the devices at high temperatures. Operating at high temperature reduces the performance and greatly shortens the lifespan of the electronics [7]. Often times, high power electronics are needed in space exploration rovers, similar to the gate driver project's high power devices. High power devices usually operate at higher current densities and higher internal electric fields [7]. There are limited comprehensive high temperature studies, however there have been studies on the degradation of devices as a function of temperature. Usually, this will indicate the lifetime of the devices at normal operating conditions and predict high temperature results. Most of the high temperature studies have focused on compound semiconductors devices because of their higher bandgap. Compound devices such as Gallium Arsenide (GaAs) FETs, high electron mobility transistors (HEMT), pseudomophic HEMT, wide bandgap semiconductor devices such as SiC and GaN FETs, and hetero-junction bipolar transistors (HBTs) have replaced the standard Silicon devices for high temperature applications [7].

Power Electronics need to be able to operate at high temperatures, at high power levels, and in extreme environments [8]. Power devices will generate heat during the switch-mode. Wide bandgap devices will outperform Si and GaAs devices in switching performance by an order of magnitude at high temperatures. Devices fabricated with Si and GaAs technology will fail arising from hot spots generated by switching in the electronics. Si devices will fail when the junction temperature

exceeds 200C [8]. Wide bandgap semiconductors are excellent for these applications because of their excellent thermal conductivity and large breakdown fields. Some examples would be Silicon Carbide (SiC) and Gallium Nitride (GaN). Both of these materials are also known to have high breakdown field strength, and large energy bandgap while GaN possesses high carrier mobility [8]. These materials would be a better option if a designer wants higher temperature and higher power than Si technology. For these reasons the gate driver project and UVLO were fabricated using BCD-on-SOI.

2.4 Other UVLO Circuits

Since electronic circuits are becoming more and more dependent on battery powered sources, a need for power monitoring has become prevalent. The UVLO is not a new device, and several varied implementations exist. There are a few criteria that are important to consider when picking out the correct UVLO for a project. First, the supply voltage range and the threshold at which the UVLO triggers a fault is very important. Also, the temperature range of operation should be taken into account.

Several UVLO circuits were reviewed and considered in the initial design of the UVLO. First, consider the CMOS UVLO design shown in Figure 2-3. The circuit is fabricated in a 0.5μm n-well process. This UVLO concept consists of an inverter pair and a hysteresis controller. The hysteresis controller is simply a resistor voltage divider controlled by an NMOS switch. The hysteresis control output is the input to the first inverter. The inverter pair is powered from a pre-regulator [1]. This UVLO is able to monitor a 5V supply. The UVLO outputs a fault at 3.75V, which is a threshold of 75%. Since temperature was not mentioned it is assumed that the circuit operates at room temperature of 25°C.

Another UVLO reviewed is shown in Figure 2-4 and Figure 2-5. The UVLO is used in a Switch Mode Power Supply (SMPS) that provides low power consumption for multi-mode applications. This system was fabricated in 1.5μm BCD technology. The UVLO in this system monitors V_{DD} and prevents the system from turning ON until V_{DD} exceeds 10V. After the systems turns ON, it will turn OF again if V_{DD} drops below 7V. This UVLO uses a bandgap reference circuit with an output of 2.65V to supply the V_{REF} input [9]. This UVLO is designed to monitor a 10V supply. The UVLO outputs a fault at 7V, which is a threshold of 70%. Since temperature was not

mentioned, it is assumed that the circuit operates at room temperature (25°C). This is the second UVLO without a temperature range mentioned.

Finally, the UVLO in Figure 2-6 is reviewed. This circuit was only simulated; it was never fabricated. This UVLO is used in a system for DC-DC conversion. The UVLO monitors the voltage of the bandgap, thus reducing the temperature sensitivity to threshold voltage. However, the output of the UVLO will change as V_{DD} is altered. A sampling cell is formed from R3, R4, and R5. R3 is approximately equal to R5. For control of the sampling cell's ratio a transistor, M1 is used. A comparator cell is built using bipolar transistors and two resistors, R1 and R2. A current mirror is created from M2 and M3. Finally, two inverters are on the output for filtering. The zero temperature coefficient compensative point is set at room temperature (25°C). The threshold voltage decreases as the temperature deviates from 25°C. The threshold voltage has a negative temperature coefficient if the temperature is above 25°C [10]. The possible temperature range for the system to operate within is -40°C to +85°C. This UVLO is designed to monitor a 3.5V supply. The UVLO outputs a fault at 2.6V, which is a threshold of approximately 74%.

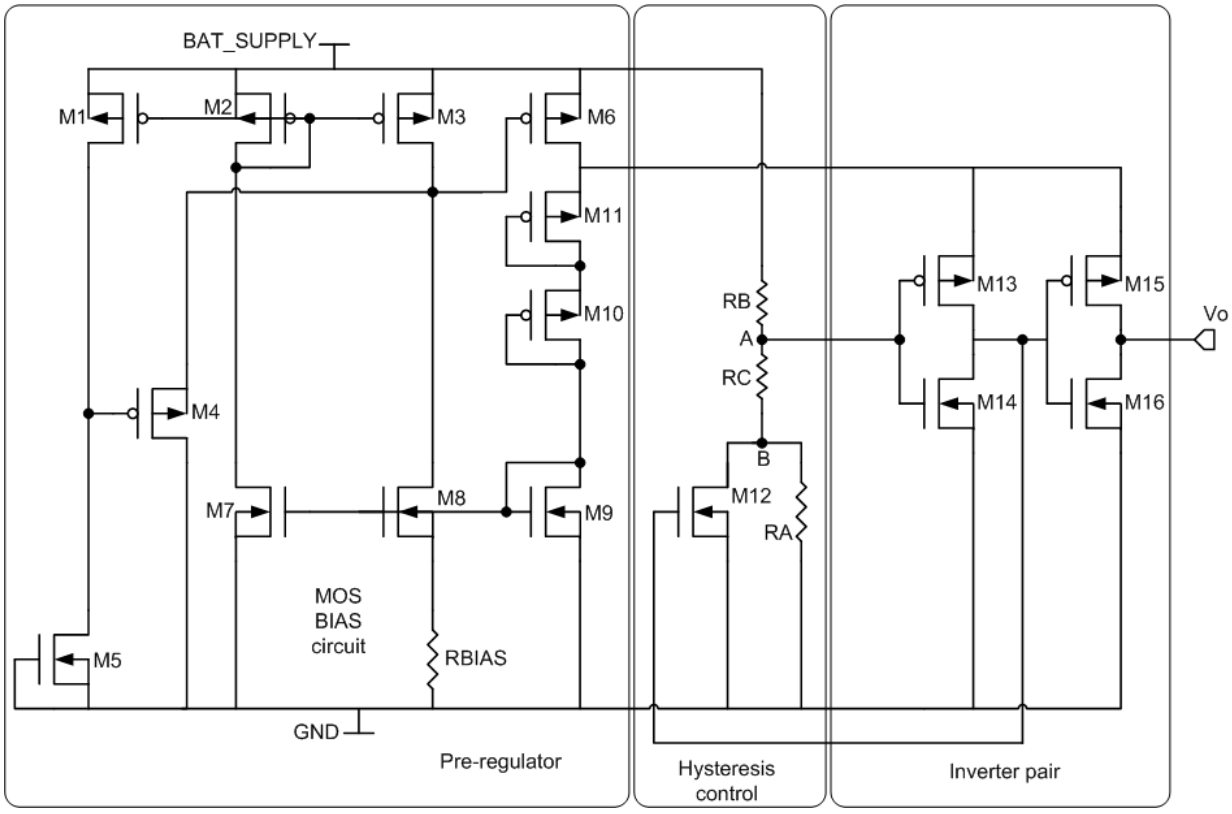

Figure 2-3: CMOS UVLO Circuit - Hoque [1]

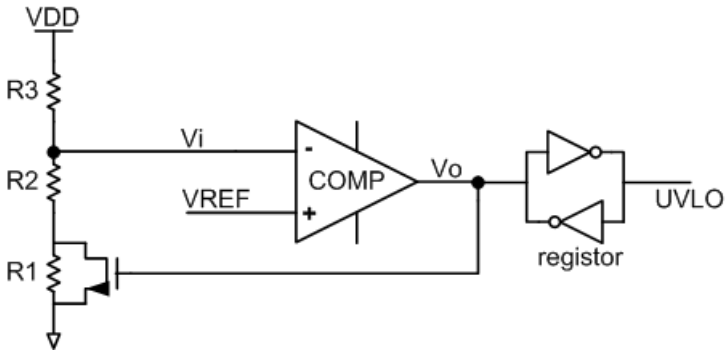

Figure 2-4: Diagram of UVLO System - Hong [9]

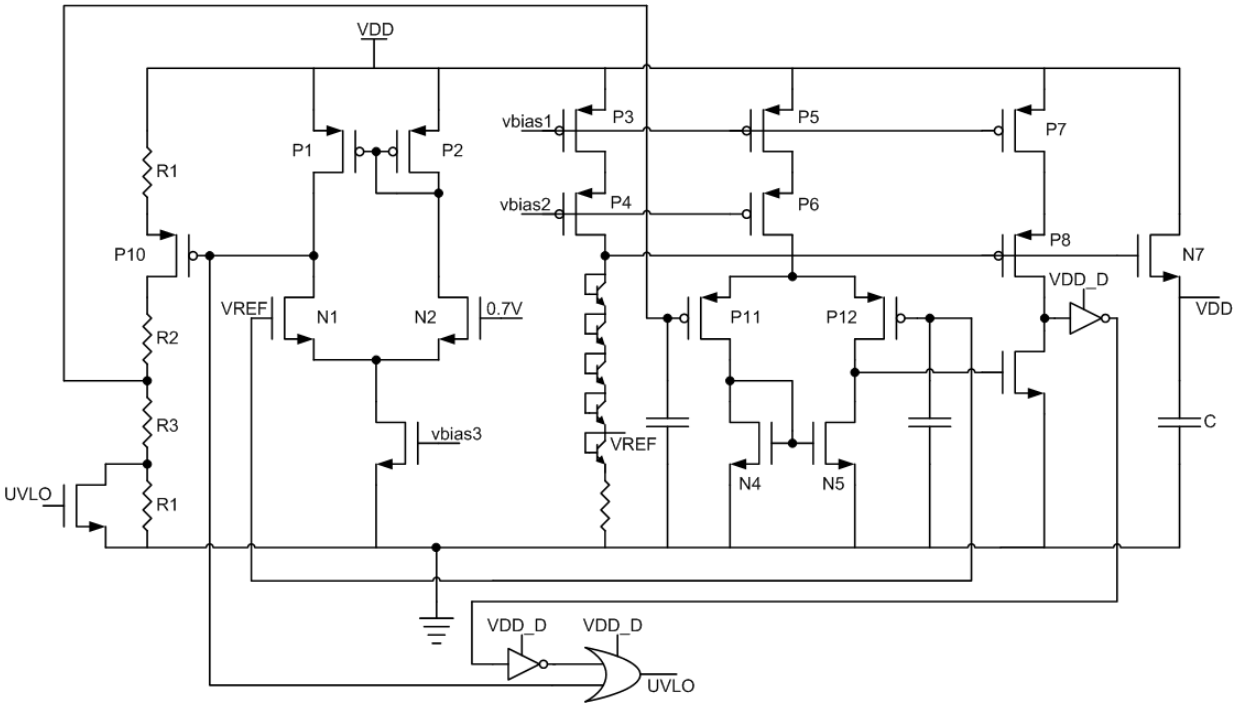

Figure 2-5: Detailed schematic of UVLO in UVLO System - Hong [9]

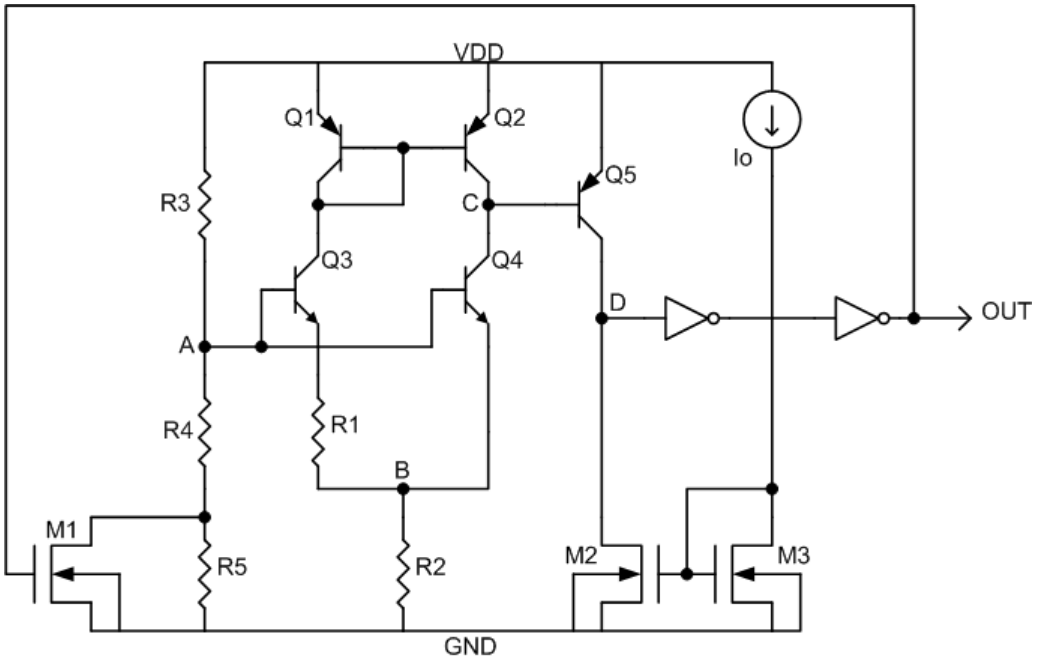

Figure 2-6: Diagram of UVLO - Fanglan [10]

Unfortunately, the next two UVLO circuits discussed do not have topology figures; however, their characteristics are very important for comparison. First, the UVLO was designed for a Dual In-Line Package transfer molded Intelligent Power Module (DIP-IPM) developed by Mitsubishi Electric for home appliance motor control. This UVLO was especially significant for comparison because its application is so close to the project being presented. The unit contains six insulated-gate bipolar transistors (IGBTs), free wheeling diodes for the three phase motor drive, a High Voltage Integrated Circuit (HVIC), and a Low Voltage Integrated Circuit (LVIC). When the control voltage supply drops below the under-voltage level, the IGBTs are turned OFF. Also, a fault is asserted to the system [11]. This UVLO is designed to monitor a 15V supply. The UVLO outputs a fault at 13.5V, which is a threshold of 90%. This is an impressive threshold percentage, well above most of the other UVLO. The gate driver UVLO did not need this large threshold, but was still capable of meeting this threshold. The temperature range of operation for this circuit is -20°C to +100°C. This range is not large enough to meet the requirements for the gate driver UVLO.

Lastly, a UVLO used for switched mode PWM based DC-DC converters for communications, automobile, computer and aerospace applications was reviewed. The UVLO for this system facilitated safe starts upon power up [12]. This UVLO is designed to monitor an 8V supply. The UVLO

outputs a fault at 7V, which is a threshold of 85%. However, the system is designed to monitor a 16.5V supply. The system outputs a fault at under voltage (UV) level 0f 10.5V, which represents a threshold of 65%. The temperature range of operation for this circuit is -25°C to +85°C. It was important to review this UVLO because the threshold was also a good standard for the gate driver UVLO. However, the temperature range is very small for the gate driver's design.

Reviewing these other UVLO circuits helped with design of the UVLO circuit used for the gate driver. The threshold voltage is typically around 80%. The temperature range depends on the application, but few if any met the needed temperature range for the gate driver. Also, few circuits were able to meet the voltage range needed for the gate driver (10V, 20V, and 30V).

Chapter 3

Design Approach

3.1 UVLO Circuits

Monitoring the supply voltage is not an easy task when observing and powering from the same voltage supply. As with most digital circuitry, the threshold or the operating point of the device will drop as the supply voltage drops. In cases such as Schmitt triggers, the output will change as the supply voltage drops. Developing or finding circuits that will operate within the threshold can be difficult.

The under voltage lock out system presented in Figure 3-1 displays three individual UVLO circuits with an OR gate to the outputs. The first UVLO is powered from V_{DDH} to V_{SSH} and monitors V_{DDH} to V_{SSH}. The second UVLO is powered from V_{DDH} to V_{SSH} and monitors V_{DD} to V_{SS}. The third UVLO is powered from V_{DD} to V_{SS} and monitors V_{DD} to V_{SS}. The first two under voltage lock out circuits use a comparator with hysteresis. The first UVLO circuit utilizes the circuit topology shown in Figure 3-2. The third UVLO circuit utilizes the circuit topology shown in Figure 3-3. The second UVLO circuit is a hybrid of the first and the third circuits. All of the outputs are OR-ed together as shown. The dotted blue lines represent off-chip connections or board-level connections. Having the outputs of each circuit come off-chip allows the user to have the option to monitor the individual supplies or both supplies simultaneously. Also, this option allows the designer to check the functionality of the individual UVLO circuits.

The UVLO 1 design shown in Figure 3-2 monitors V_{DDH} to V_{SSH} power voltages of 30V, 20V, or 10V. This circuit uses a comparator with hysteresis. The resistors (R1 and R2) are actually a

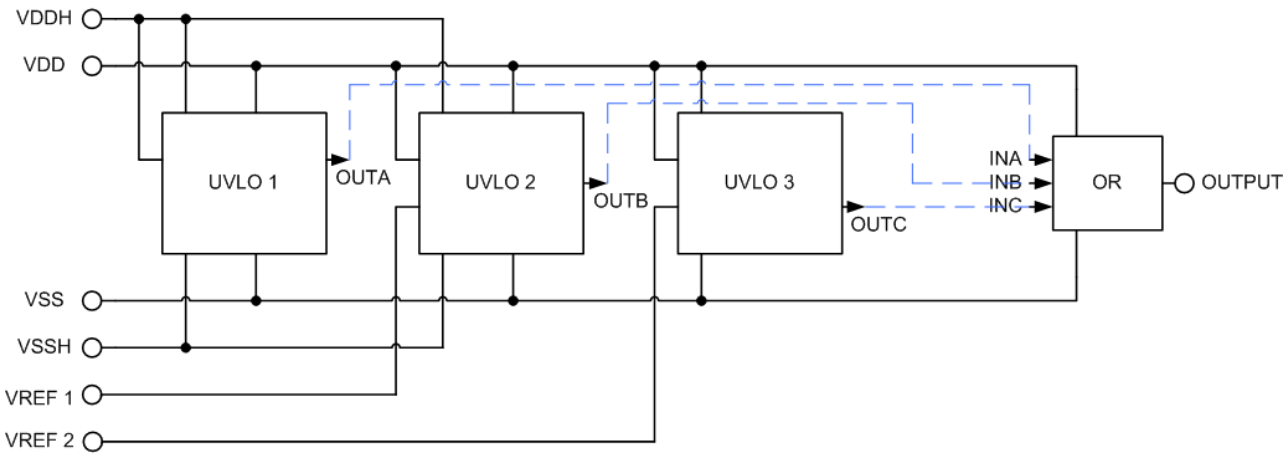

Figure 3-1: UVLO System Topology for Gate Driver

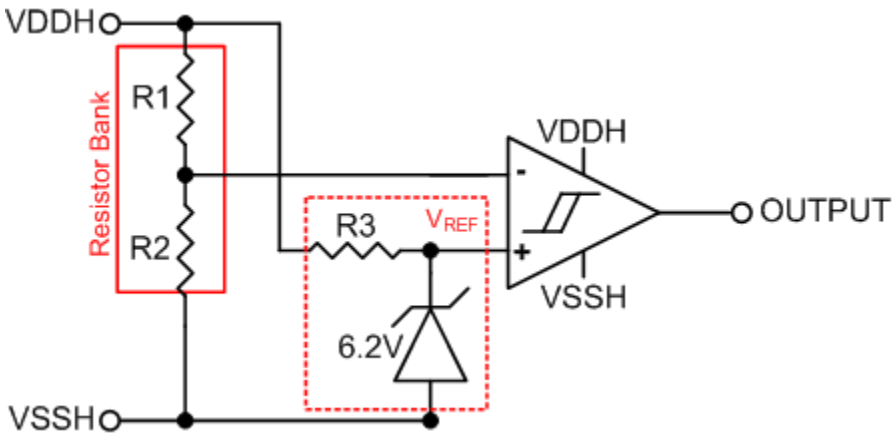

Figure 3-2: UVLO 1 : V_{DDH} to V_{SSH} Circuit Topology

network of resistors in a resistor bank. This gives the user the option to select a needed resistance from the bank depending on the magnitude of V_{DDH} to V_{SSH}. The voltage (V_{REF}) is set between 6-7 V by a resistor and a zener diode.

The UVLO 3 design shown in Figure 3-3 monitors the 5V swing from V_{SS} to V_{DD}. This 5V supply could come from a voltage regulator or be sourced off-chip. Also, the reference voltage ($V_{REF} = 2.4V$) can come from a bandgap reference (BGR) circuit on-chip or an off-chip source. The circuit contains a low-voltage comparator with hysteresis and an inverter. These circuits were designed to be as temperature independent as possible considering their natural circuit properties. Since the voltage source is always a 5V supply, a resistor bank is not needed for this circuit. This saves a lot of space on-chip. The resistors were set to 10KΩ. This resistance value was chosen because it met both the area and the current requirements.

UVLO 2 is a hybrid of UVLO 1 and UVLO 3. Figure 3-4 displays the circuit topology for UVLO 2. The high-voltage comparator from UVLO 1 is used, however the 5V swing is monitored. This allows for the circuit to be powered by a different source than the one it is monitoring. Since it is monitoring the 5V swing, the inputs for the comparator are the same as the inputs for UVLO 3. There are two resistors and a reference voltage ($V_{REF} = 2.4V$). Since UVLO 2 is powered from the high voltage supply but monitors the low voltage supply, it relies on UVLO 1 monitoring the high voltage supply. Through simulation, as the high voltage drops it has minimal effects on the functionality of UVLO 2, so minimal that it can be neglected.

3.2 UVLO 1 and UVLO 2 Comparator Circuit

Typically, comparators determine if an input voltage is above or below a reference voltage. The comparator has two inputs: a reference voltage and a measured voltage. If the measured voltage is larger than the reference voltage then the output will be 'high' (logic '1'). If the measured voltage is less than the reference voltage then the output will be 'low' (logic '0'). With the analog inputs and the digital output, the converter approximates the function of an analog-to-digital converter.

The comparator has internal hysteresis and a clamping circuit on the output to limit the output voltage swing (Figure 3-5). Comparators with hysteresis are needed if there is a noisy signal [13]. When using hysteresis, it is important to know that the input threshold changes as a function of the output. Hysteresis also prevents rapid switching in the circuit. The hysteresis for the comparator

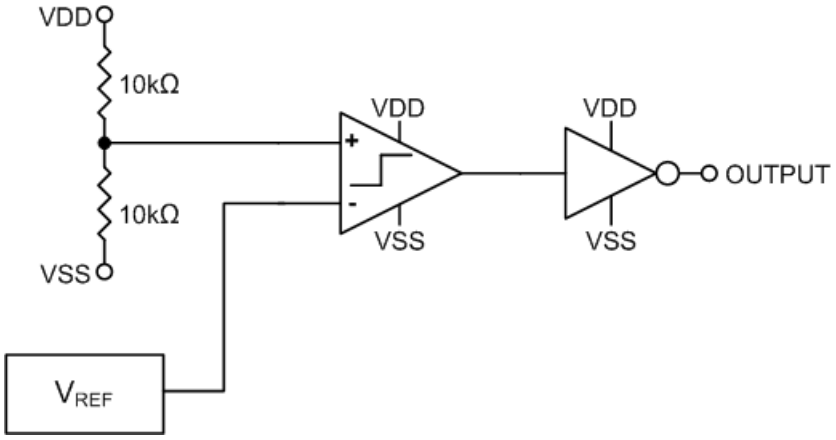

Figure 3-3: UVLO 3: V_{DD} to V_{SS} Circuit Topology

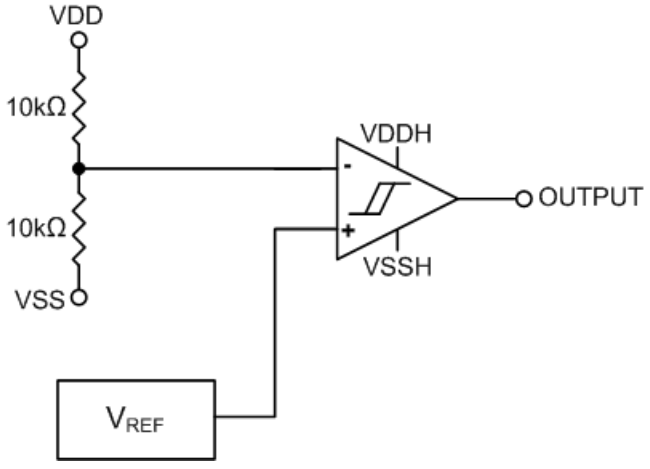

Figure 3-4: UVLO 2: V_{DD} to V_{SS} Circuit Topology

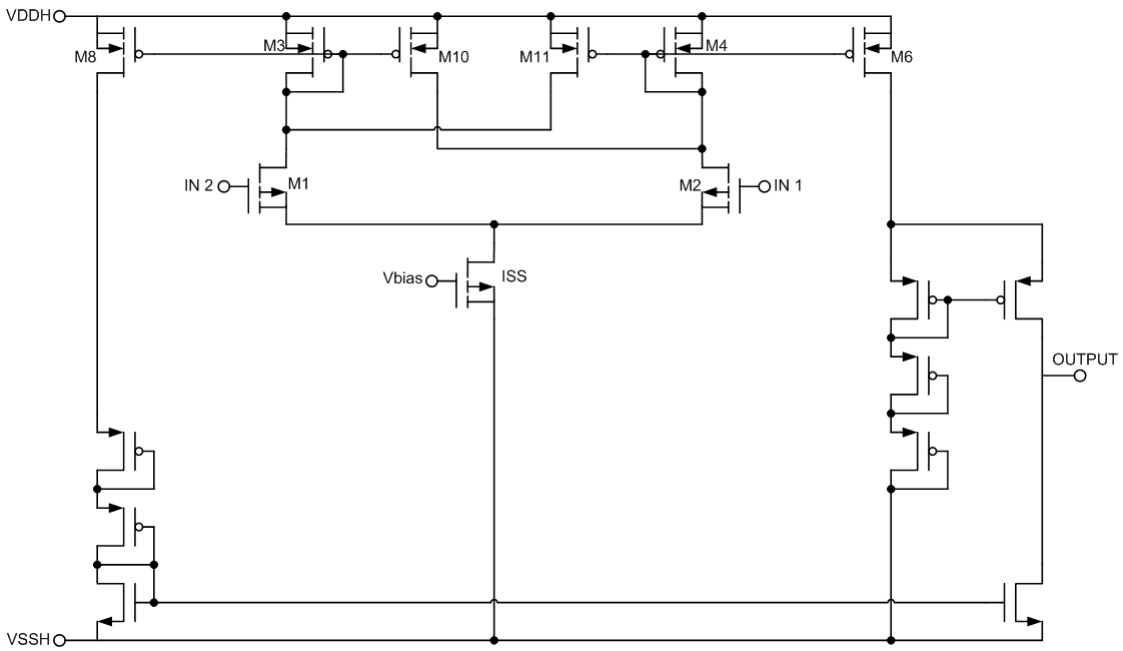

Figure 3-5: Comparator Circuit Topology

is shown in Figure 3-6

There are two types of feedback in this circuit. There is negative current-series feedback due to the common-source node connection of transistors M1 and M2. There is also positive voltage-shunt feedback from the gate-drain connections of transistors M10 and M11. Since there are two forms of feedback, the dominant feedback will dictate the feedback of the comparator. Hysteresis needs positive feedback. If $\frac{\beta_{10}}{\beta_3}$ <1, then negative feedback dominates and there is no hysteresis. If $\frac{\beta_{10}}{\beta_3} > 1$, then positive feedback dominates and hysteresis is present [13]. This makes the sizing of transistors in the input stage very important.

The hysteresis switching points($V_{TRP}{}^{+}$ and $V_{TRP}{}^{-}$) are calculated using the following method. If transistor M1's gate is tied to ground and transistor M2's gate input has a negative voltage applied; then M1, M3, M10 are ON and M2, M4, M11 are OFF. All the current (I_{SS}) will flow through M1 and M3 and the voltage at the output is 'high'. As the input voltage of M2 increases a part of the current (I_{SS}) will flow through M2. Continuing to increase the input voltage, the current i_2 will eventually be equal i_{10} [13].

$$i_{10} = \frac{(W/L)_{10}}{(W/L)_3} \cdot i_3 = i_2 \tag{3.1}$$

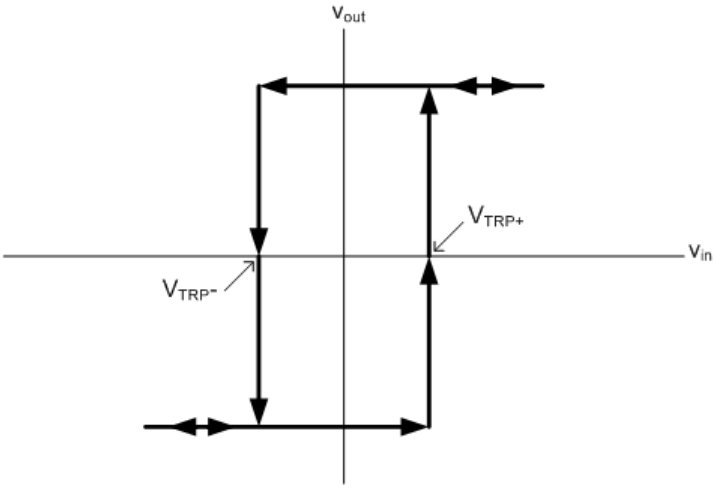

Figure 3-6: Comparator Hysteresis - Positive Switching Point ($V_{TRP}{}^{+}$), Negative Switching Point ($V_{TRP}{}^{-}$)

$$i_2 = I_{ss} - i_1 \qquad where\ \ (i_1 = i_3) \tag{3.2}$$

$$i_3 = \frac{I_{ss}}{1 + \frac{(W/L)_{10}}{(W/L)_3}} \tag{3.3}$$

$$V_{GS1} = \left(\frac{2i_1}{\beta_1}\right)^{1/2} + V_{T1} \tag{3.4}$$

$$V_{GS2} = \left(\frac{2i_2}{\beta_2}\right)^{1/2} + V_{T2} \tag{3.5}$$

$$V_{TRP}{}^{+} = V_{GS2} - V_{GS1} \qquad Positive\ \ Trip\ \ Point \tag{3.6}$$

Eventually, the increase of input current will cause the comparator to switch states, and the current through M2 eclipses the current through M10. With the majority of the current flowing through M2, the current then also flows through M4. This turns ON M11 and turns OFF M3, M10, and M1. The circuit then reaches the point where i_1 equals i_{11} and the negative trip point can be calculated [13].

$$i_{11} = \frac{(W/L)_{11}}{(W/L)_4} \cdot i_4 = i_1 \tag{3.7}$$

$$i_4 = \frac{i_5}{1 + \frac{(W/L)_{11}}{(W/L)_4}} = i_2 \tag{3.8}$$

$$i_1 = i_5 - i_2 \tag{3.9}$$

$$V_{TRP}{}^{-} = V_{GS2} - V_{GS1} \qquad Negative\ Trip\ Point \tag{3.10}$$

The differential input stage needs an output stage for reasonable voltage swing and output resistance. The circuit becomes a differential-to-single-ended converter because of the output stage design [13]. The output of the comparator is buffered before sending the signal to the padframe. Notice the high-voltage transistors at the input stage of the comparator.

3.2.1 Clamping of the Output

Since the output of the comparator will input into another gate, the output voltage is 0-5V. Without this clamping circuit, the output voltage would swing rail-to-rail [14]. The original network plays a game of balance. After altering one side of the output, the other leg of the comparator circuit is changed to balance the system again. (Figure 3-7)

The transistors on the output stage are sized in a 10-to-1-to-1 ratio to set the clamping. The other series transistors are level shifters 1-to-1-to-10 [14]. Notice the high-voltage devices used at the input stage. These devices are 45V devices and are needed because of the large voltage swing. The V_{gs} is approximately 5.5V so the output stage does not need to be composed of high-voltage devices.

3.3 High-Voltage Current Source

The current source shown in Figure 3-8 is used in the high-voltage comparator. This is a self-biasing current source. The current source I_{SS} has very little temperature dependence and is approximately 23 micro-Amperes (Figure 3-9). The start-up circuit consists of six PMOS transistors connected

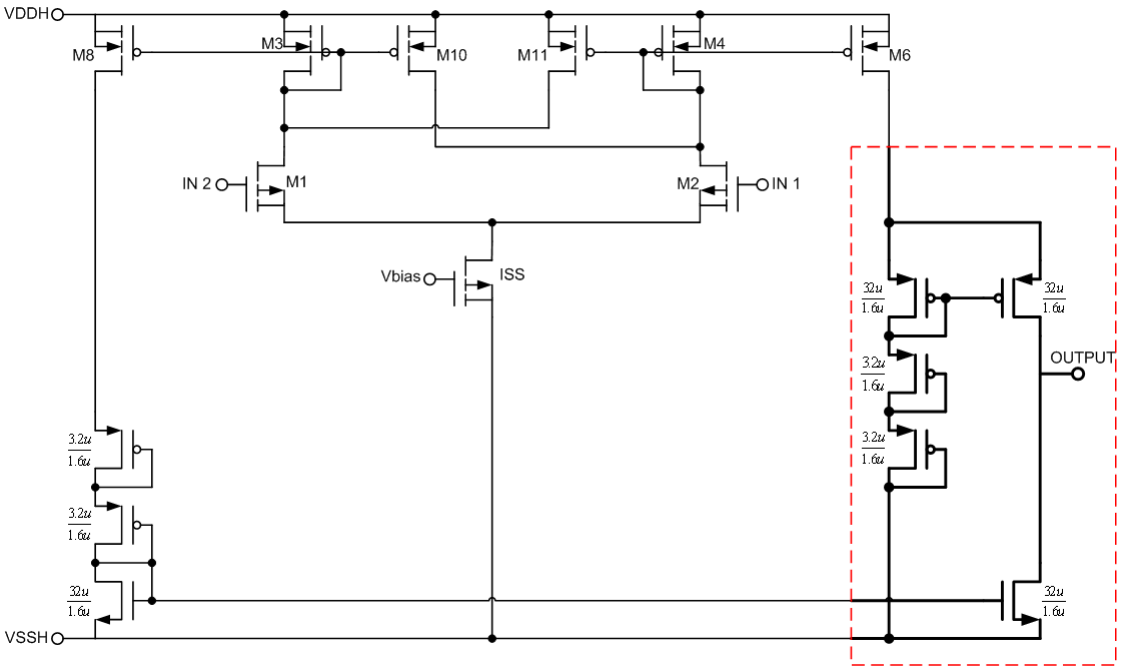

Figure 3-7: Clamping the Output of the Comparator [14]

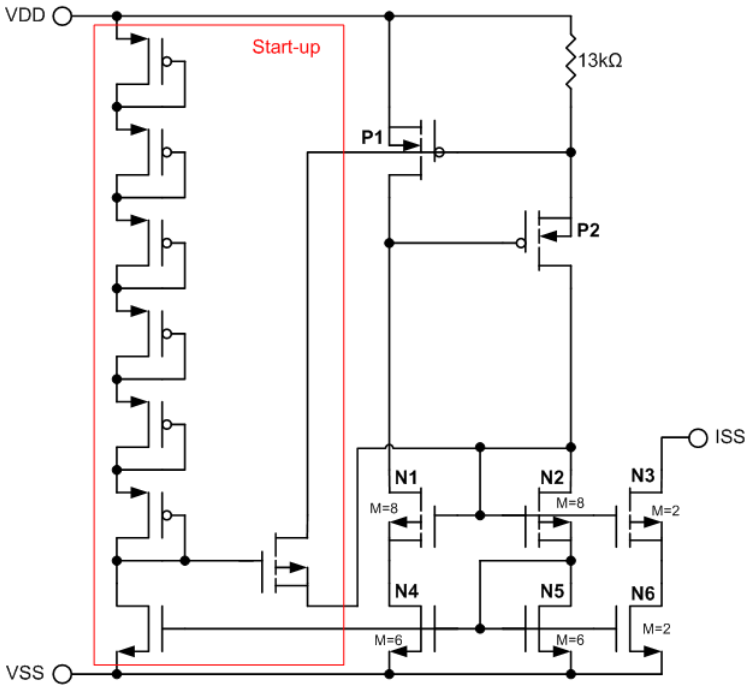

Figure 3-8: Current Source [15]

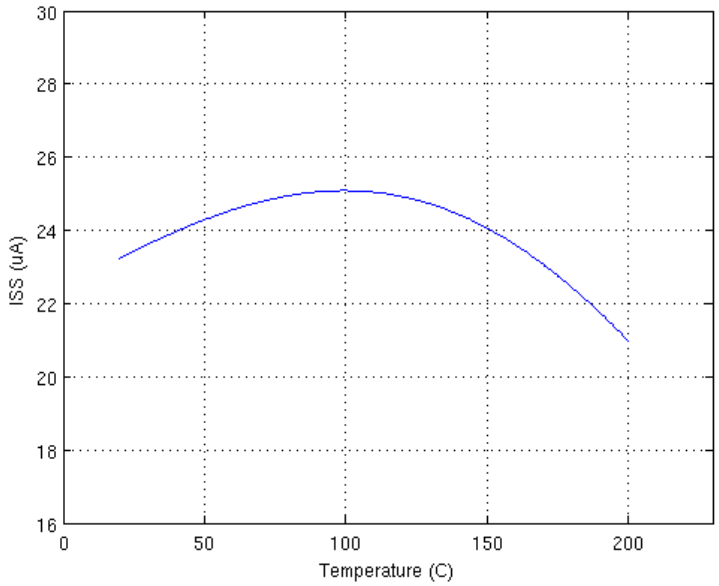

Figure 3-9: Comparator Current I_{SS} vs. Temperature

in series with a gate-to-drain connection to both a 5V NMOS and a 45V NMOS transistor. The resistor sets the current through P2, N2, and N5. The current is then mirrored through P1, N1, and N4. Notice the sizing of the NMOS transistors. Through sizing of these transistors and the value of the resistor, the current is set as needed [15]. This allows for a simple redesign of the current source and implementation in the low voltage comparator. The resistance is reduced and the multipliers of the transistors are also reduced to get approximately 10 micro-Amperes from the new current source.

3.4 UVLO 3 Low-Voltage Comparator Circuit

The comparator used in UVLO 3 is presented in Figure 3-10 [16]. The low-voltage comparator is powered from the V_{DD}-V_{SS} voltage swing. This comparator has internal hysteresis through the gate-drain connections of M3 and M4, similar to the high-voltage comparator. It also requires a current source (I_b=10uA).

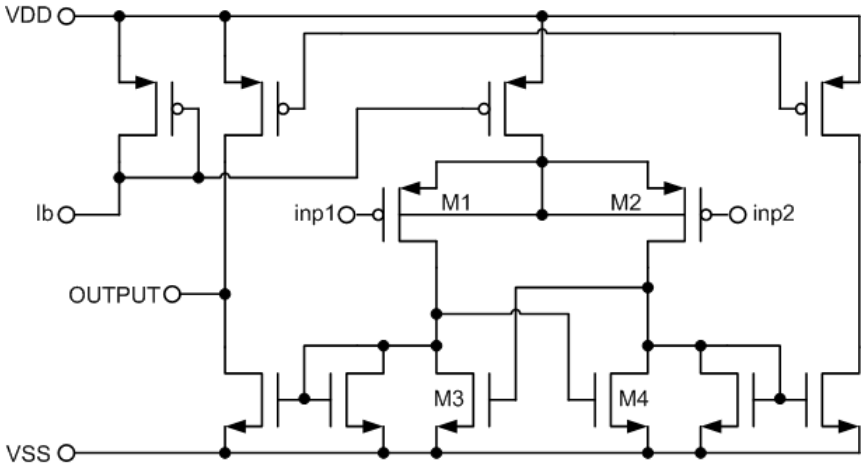

Figure 3-10: Low-Voltage Comparator Circuit Topology [16]

Chapter 4

Simulation and Test Results

4.1 Simulation Results - Schematics

It is important to keep a standard for measurement of the schematic simulation, layout simulation, and experimental testing. Figure 4-1 displays the standard of measurement used on the UVLO circuit. This measured point is the switching point where there is a fault in the system.

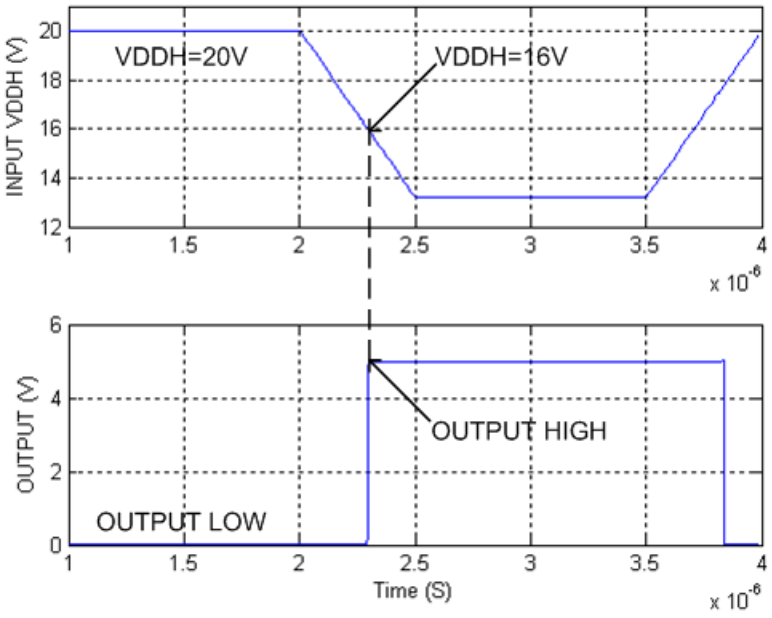

Figure 4-1: Measuring the Output of the UVLO

4.1.1 Simulating the UVLOs individually

Since the user has the option to utilize each of the UVLOs individually, it is important to simulate each UVLO and measure its output. This will also allow for the designer to determine the performance of each of the UVLO circuits work before sending the signals into the OR gate. Using the standard of measurement mentioned before, the following results were found for UVLO 1 (Table 4.1), UVLO 2 (Table 4.2), and UVLO 3 (Table 4.3). Displayed in these tables are the measured value of the switching point, the simulation temperature, and the percentage of the measured supply (input). The measured switching point is divided by the supply voltage to find this percentage (Equation 4.1).

$$\%\ efficiency = \frac{switching\ \ point}{supply\ \ voltage} \times 100 \tag{4.1}$$

The output from a transient sweep for UVLO 1 is seen in Figure 4-2. Figures 4-3 and 4-4 shows the output from a transient sweep for UVLO 2 and UVLO 3. These results display the fast switching times of the individual UVLO circuits. It is important to take the switching time into account. If the voltage drops quickly, the UVLO needs to react quickly. The UVLO operates and switches fast enough for the gate driver circuit. Notice the output signals in Figures 4-3 and 4-4 have spikes on either side of the "fault" or "high" state. This is due to the fact that the output signal wants to swing from 0-5V. However, the output signal can only swing as high as the power supply voltage. This would then raise the question about why UVLO 2 has this issue since it is powered from the high voltage supply. While UVLO 2's comparator circuit is powered from the high voltage supply and should give a clean 0-5V swing, the signal from the comparator is buffered before connecting to the pin. This buffer is a low-voltage buffer and will cause this spiking result for UVLO 2. This low-voltage buffer can be replaced with a high-voltage buffer and can eliminate the spiking effect. Since the gate driver circuit really only needs a signal to surpass 2.4V to be considered to be in a fault state, these spikes really do not effect the performance of the UVLO with the gate driver. Therefore, a low-voltage buffer is fine for this design.

4.1.2 Simulating the UVLOs with the OR Gate

The three UVLO circuits were OR-ed together in order to obtain a single output. Measurements need to be made at the output of this OR gate in case it adversely affects the signal. Effects on the

Table 4.1: Output from UVLO 1 - Schematic

VDDH	Output where V_{DDH} Faults		
30V	27°C	23.61	79%
	200°C	27.2	90%
20V	27°C	16.03	80%
	200°C	17.94	90%
10V	27°C	8.55	86%
	200°C	9.32	93%

Table 4.2: Output from UVLO 2 - Schematic

VDDH	Output where V_{DD} Faults		
30V	27°C	4.48	90%
	200°C	4.43	89%
20V	27°C	4.48	90%
	200°C	4.41	88%
10V	27°C	4.44	89%
	200°C	4.39	88%

Table 4.3: Output from UVLO 3 - Schematic

VDD	Output where V_{DD} Faults		
5V	27°C	4.42	88%
	200°C	4.34	87%

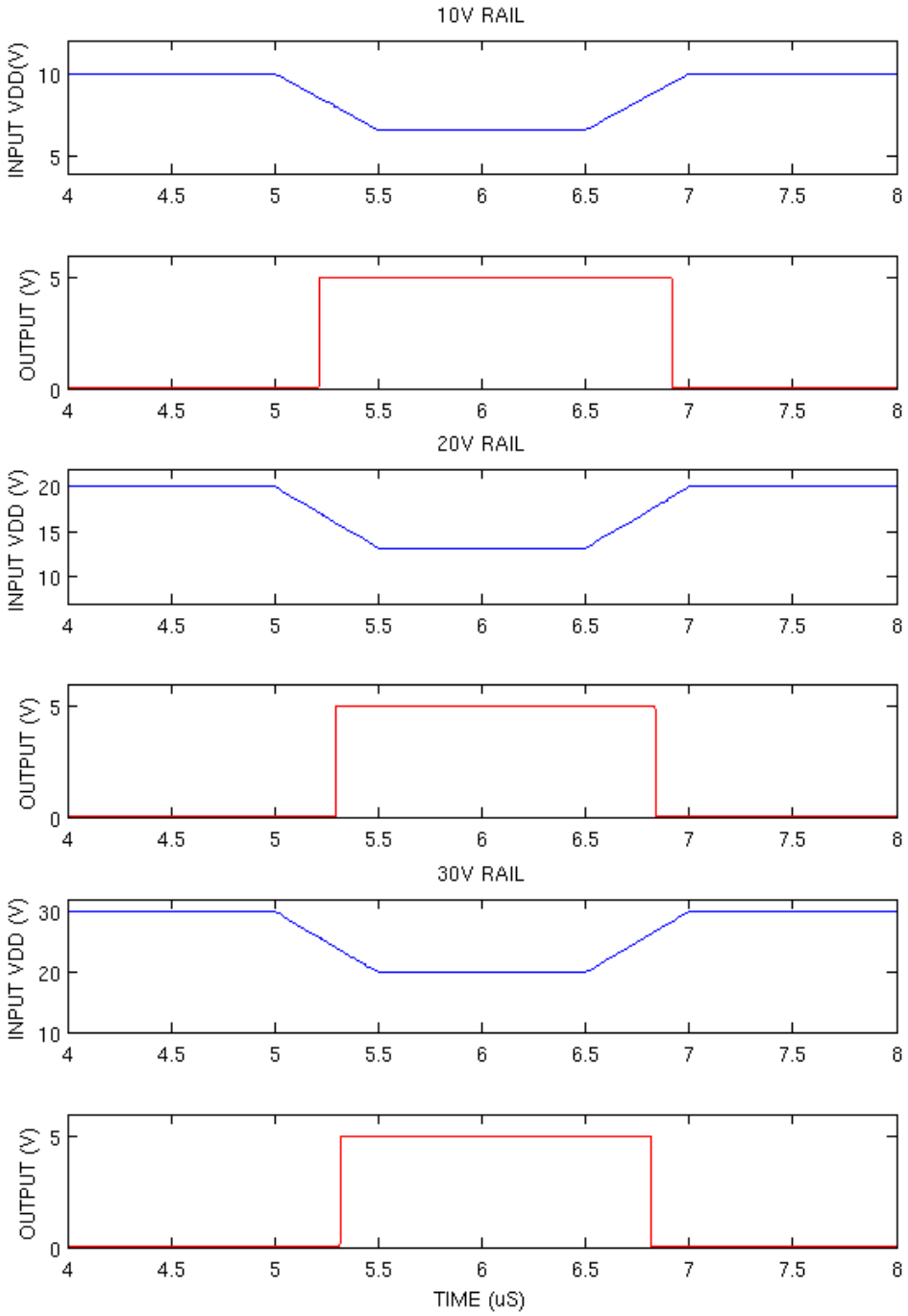

Figure 4-2: Output of UVLO 1 - Transient Simulation (Room Temperature)

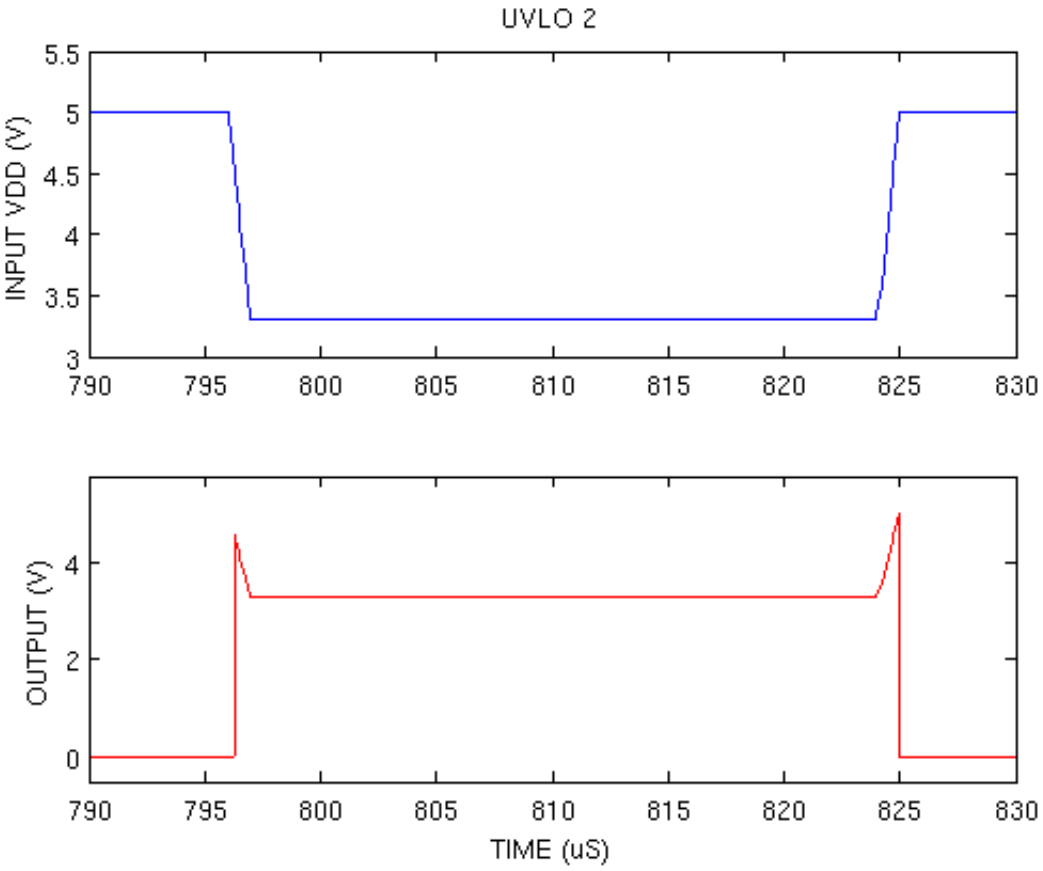

Figure 4-3: Output of UVLO 2 - Transient Simulation (Room Temperature)

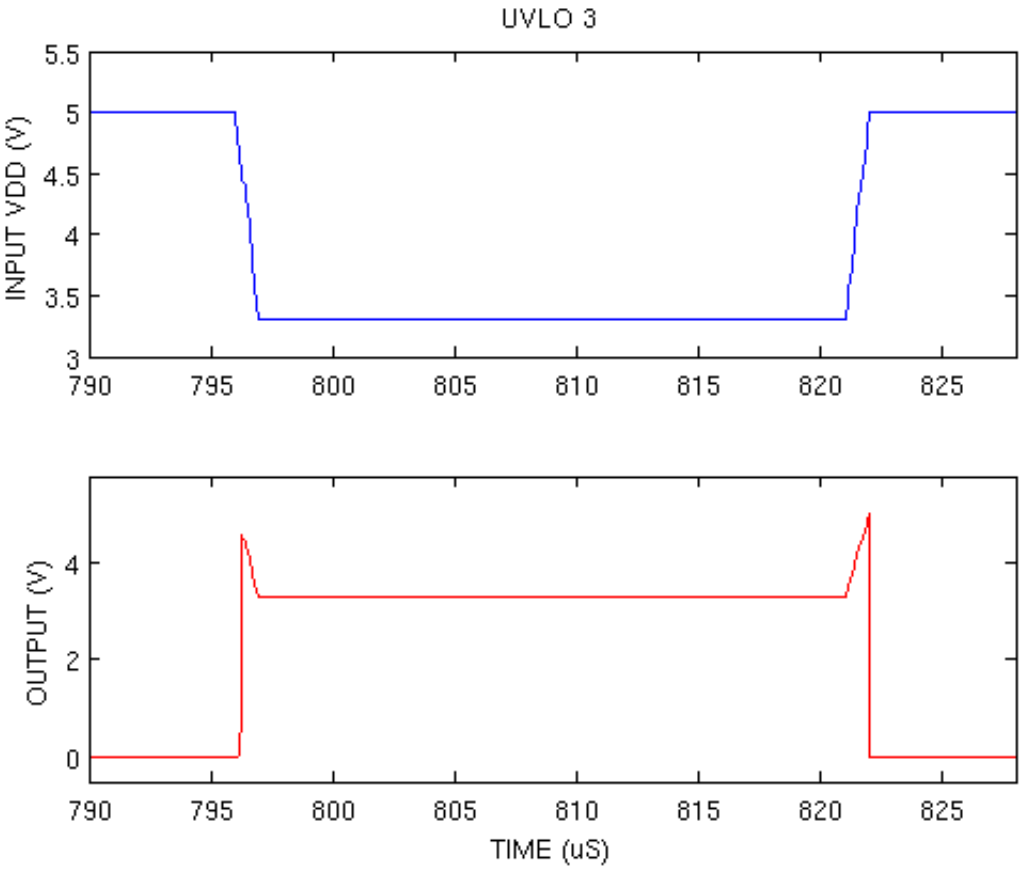

Figure 4-4: Output of UVLO 3 - Transient Simulation (Room Temperature)

signal could come from the OR gate's temperature dependance and speed of switching capabilities. Since the output of the UVLO circuit will travel off chip, to the board, then back on the chip to the input of the OR gate, there will be variations in the measured experimental data and simulated data. These results are compiled in Table 4.4. Figure 4-5 displays the transient output from the OR Gate.

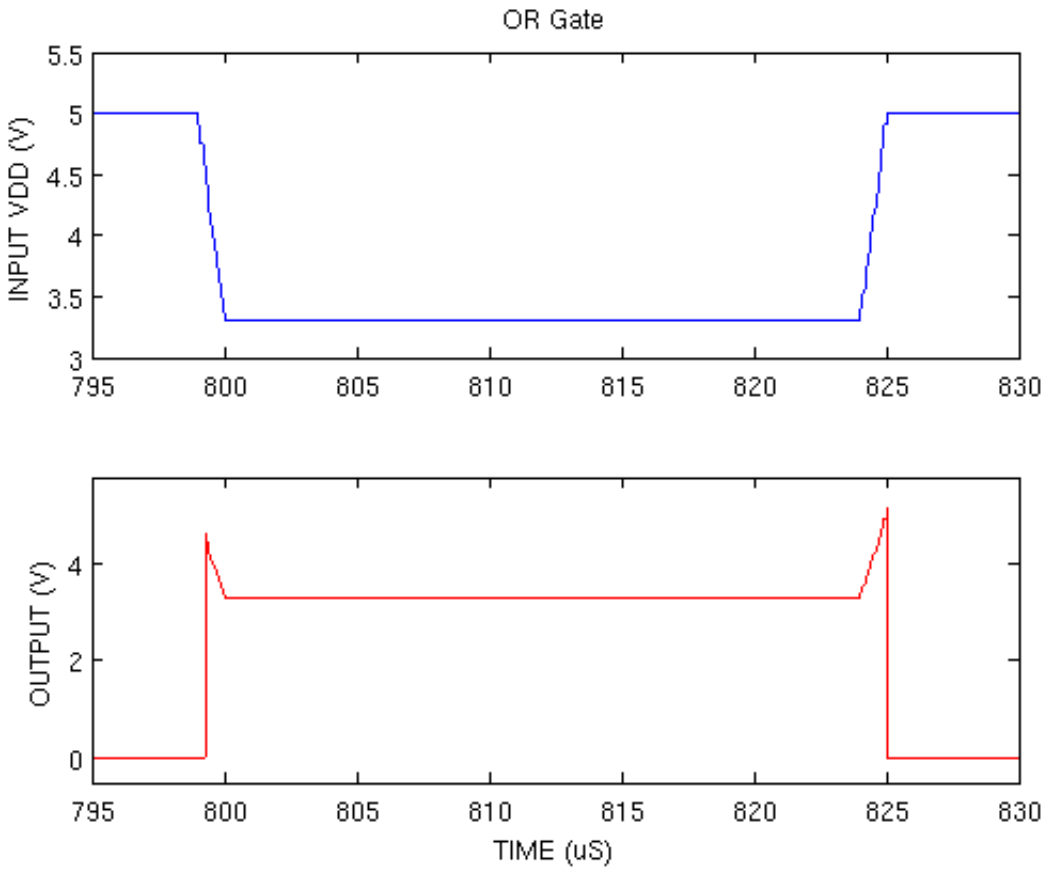

Figure 4-5: Output of OR Gate - Transient Simulation (Room Temperature)

Table 4.4: UVLO with OR Gate - Output of OR Gate - Schematic

V_{DDH}	Output where V_{DD} Faults			Output where V_{DDH} Faults			Output where V_{DD} and V_{DDH} Faults		
10V	27°C	4.61	92%	27°C	8.83	88%	27°C	4.64	93%
							27°C	9.2	92%
	200°C	4.59	92%	200°C	9.57	96%	200°C	4.68	94%
							200°C	9.39	94%
20V	27°C	4.52	90%	27°C	16.55	83%	27°C	4.52	90%
							27°C	18.3	92%
	200°C	4.53	91%	200°C	18.25	91%	200°C	4.65	93%
							200°C	18.3	92%
30V	27°C	4.59	92%	27°C	24.16	81%	27°C	4.57	91%
							27°C	27.43	91%
	200°C	4.53	91%	200°C	28.23	94%	200°C	4.6	92%
							200°C	27.04	90%

4.2 Simulation Results - Layout

Its important to simulate the layout of the circuits because these simulations take into account parasitics. The methods of measurement for the simulated layout were identical to that of of the schematics (Figure 4-1).

4.2.1 Simulating the UVLOs individually

The following tables were generated by measuring the outputs from each UVLO circuit layout. By comparing the layout results to the schematic results, the effects of the parasitics on the UVLO circuit become obvious. The trigger points are shifted causing the switching from the hysteresis to happen at lower voltages. This in turn lowers the efficiency of the UVLO's functionality. Notice the drop in percentages in the Tables 4.5, 4.6, and 4.7.

Table 4.5: Output from UVLO 1 - Layout

VDDH	Output where V_{DDH} Faults		
30V	27°C	23.22	77%
	200°C	26.94	90%
20V	27°C	15.73	79%
	200°C	17.69	88%
10V	27°C	8.51	85%
	200°C	9.24	92%

Table 4.6: Output from UVLO 2 - Layout

VDDH	Output where V_{DD} Faults		
30V	27°C	4.39	88%
	200°C	4.36	87%
20V	27°C	4.39	88%
	200°C	4.35	87%
10V	27°C	4.38	88%
	200°C	4.33	87%

Table 4.7: Output from UVLO 3 - Layout

VDD	Output where V_{DD} Faults		
5V	27°C	4.43	89%
	200°C	4.34	87%

4.2.2 Simulating the UVLOs with the OR Gate

The three UVLO circuits were OR-ed together in order to obtain a single output. Again, the measurements need to be made at the output of this OR gate in the case there is an effect on the signal due to the OR gate. Parasitics do have some effect on the results as shown in Table 4.8.

Table 4.8: UVLO with OR Gate - Output of OR Gate - Schematic

V_{DDH}	Output where V_{DD} Faults			Output where V_{DDH} Faults			Output where V_{DD} and V_{DDH} Faults		
10V	27°C	4.54	91%	27°C	8.67	87%	27°C	4.6	92%
							27°C	9.18	92%
	200°C	4.57	91%	200°C	9.44	94%	200°C	4.65	93%
							200°C	9.31	93%
20V	27°C	4.49	91%	27°C	16.49	82%	27°C	4.51	90%
							27°C	18.25	91%
	200°C	4.52	90%	200°C	18.19	91%	200°C	4.63	93%
							200°C	18.15	91%
30V	27°C	4.54	90%	27°C	24.29	81%	27°C	4.52	90%
							27°C	27.38	91%
	200°C	4.52	90%	200°C	28.18	94%	200°C	4.59	92%
							200°C	26.9	90%

4.3 Post Fabrication Test Results

Testing of the UVLO chip started with DC testing at room temperature. Figure 4-6 displays the test set-up. The test board was created out of polyimide, allowing for testing at temperatures greater than 300°C. High temperature wires with banana plugs were created to bring power supplies into the temperature chamber. Also, SMA connectors and cables were used to bring measurements off the board at both room temperature and higher temperatures.

It was very convenient that test points were brought off-chip, allowing for debugging of the circuit. First, the UVLO 1 V_{REF} TEST POINT measures the voltage produced by the resistor and zener diode connection in V_{REF} for UVLO 1 (Figure 3-2). The second test point, UVLO2 TEST POINT, measures the output from the voltage divider in UVLO 2 (Figure 3-4). The third test point, UVLO3 TEST POINT, measures the output from the voltage divider in UVLO 3 (Figure 3-3). Another convenience is the option to use an off-chip source for V_{REF} and V_{DD}. Through a board level selection these sources can either come from another circuit on the chip or from an external source.

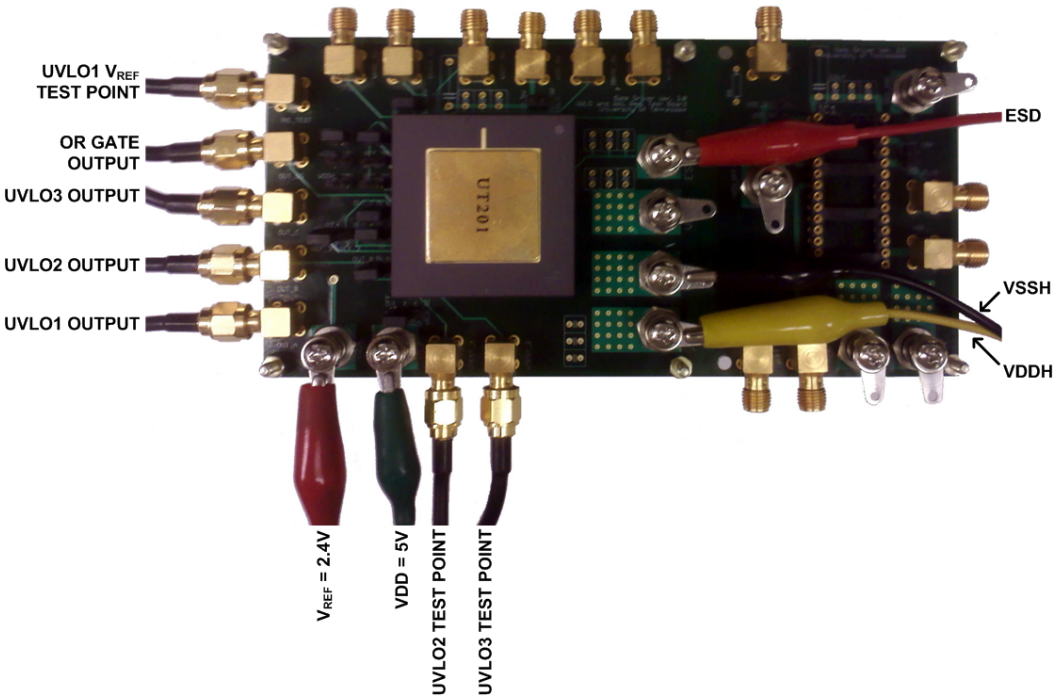

Figure 4-6: UVLO Test Set-up

4.3.1 Testing the UVLOs individually

Measurements were taken at the outputs of the individual UVLO circuits. Table 4.9 displays the output from UVLO 2 and Table 4.10 displays the output from UVLO3. These tables are similar to that of the simulated measurements. They show measured values at room temperature and at 200°C. By taking measurements at these points, it can be seen how temperature affects the overall stability and efficiency of the circuit.

Unfortunately the V_{REF} in UVLO 1 is not functioning properly, causing it to be impossible to obtain reasonable results from UVLO 1. V_{REF} is dependent on the resistor R3 and the zener diode. The zener diode is not correctly biased and therefore will not turn ON. Forcing current though the zener diode would force it to turn ON but could damage the rest of the chip. The input V_{REF} should be around 6-7 V, but is measured in the millivolt range. Since this input is so low, the output of the UVLO is always high. For this reason the UVLO is disconnected from the system for further measurements. Fortunately, the board level connections between the UVLOs and OR Gate allow for the UVLO to be taken out of the overall system.

Figures 4-7 and 4-8 show the output from a DC sweep of V_{DD} for UVLO 2 and UVLO 3. The input supply voltage V_{DD} is swept from 3V to 5V and back down to 3V. From the output results, the simulated and the measured hysteresis switching points (or trigger points) are found. This figure displays the results for both room temperature and elevated temperatures. These results were very encouraging. The simulated and measured results were very similar. Knowing that there would be some shifting in the hysteresis from simulation to post-fabrication testing, a conservative circuit was designed. Setting the hysteresis "high" allows for some shifting due to parasitics. The design goals were still met (80% threshold).

Figures 4-9 and 4-10 show the output from a transient sweep for UVLO 2 and UVLO 3 at

Table 4.9: Output from UVLO 2 - Post Fabrication

VDDH	Output where V_{DD} Faults		
30V	27°C	4.70	94%
	200°C	4.69	94%
20V	27°C	4.70	94%
	200°C	4.69	94%
10V	27°C	4.70	94%
	200°C	4.68	94%

Table 4.10: Output from UVLO 3 - Post Fabrication

VDD	Output where V_{DD} Faults		
5V	27°C	4.86	97%
	200°C	4.85	97%

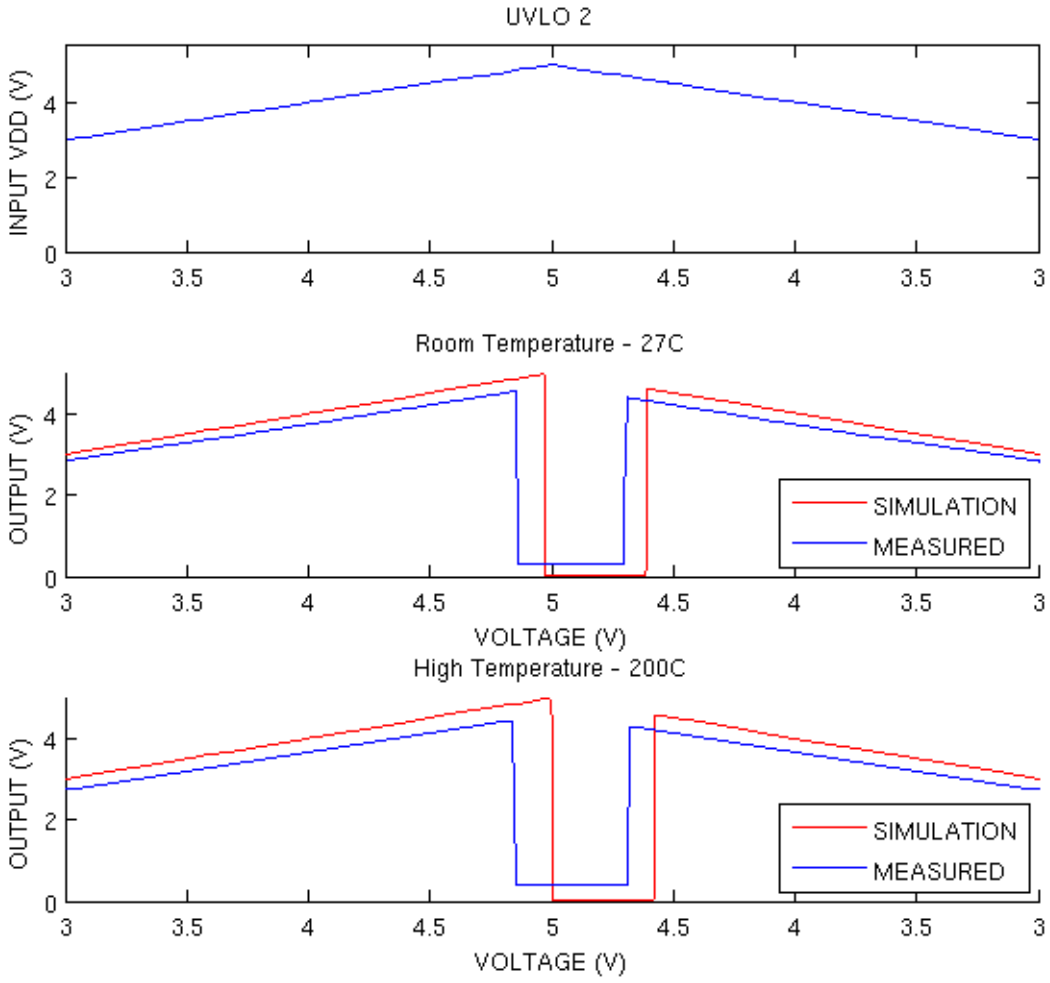

Figure 4-7: Output of UVLO 2 - Hysteresis Switching Points are Found from these Results

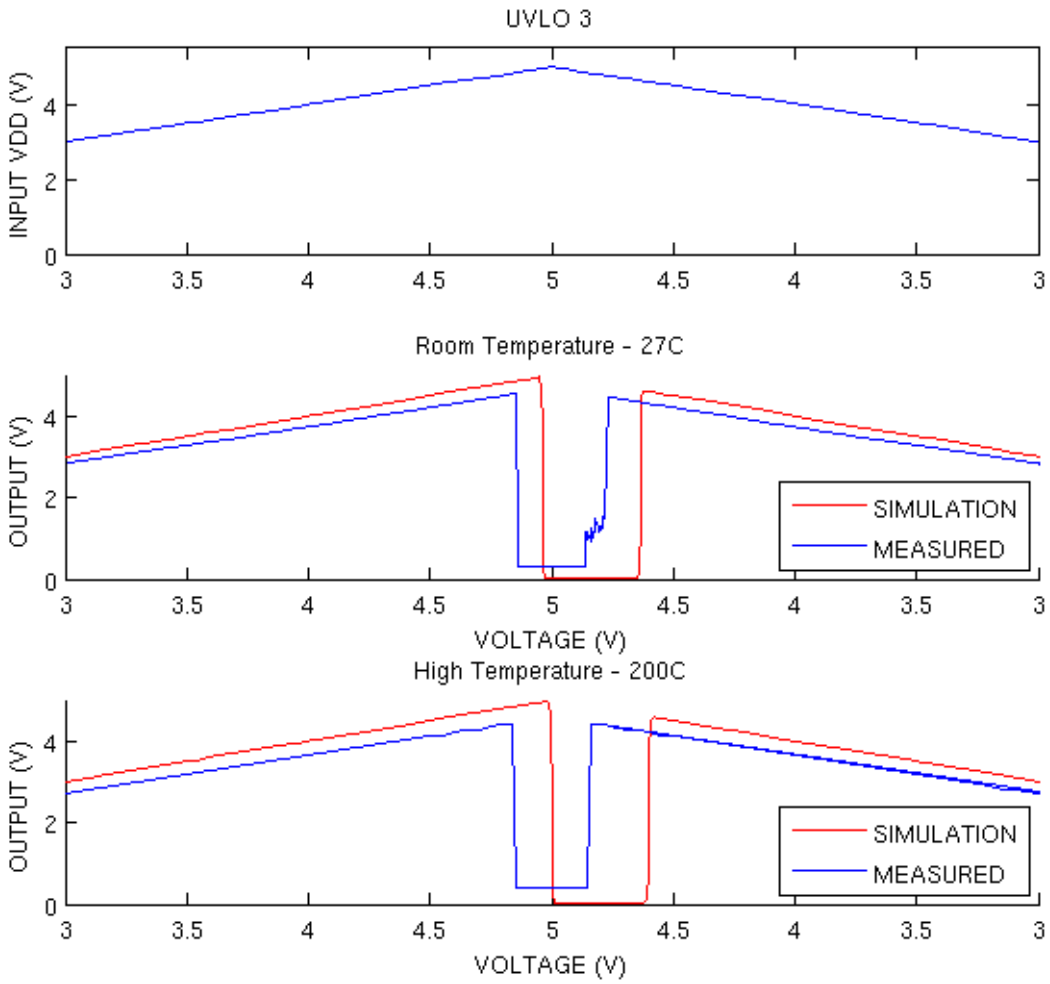

Figure 4-8: Output of UVLO 3 - Hysteresis Switching Points are Found from these Results

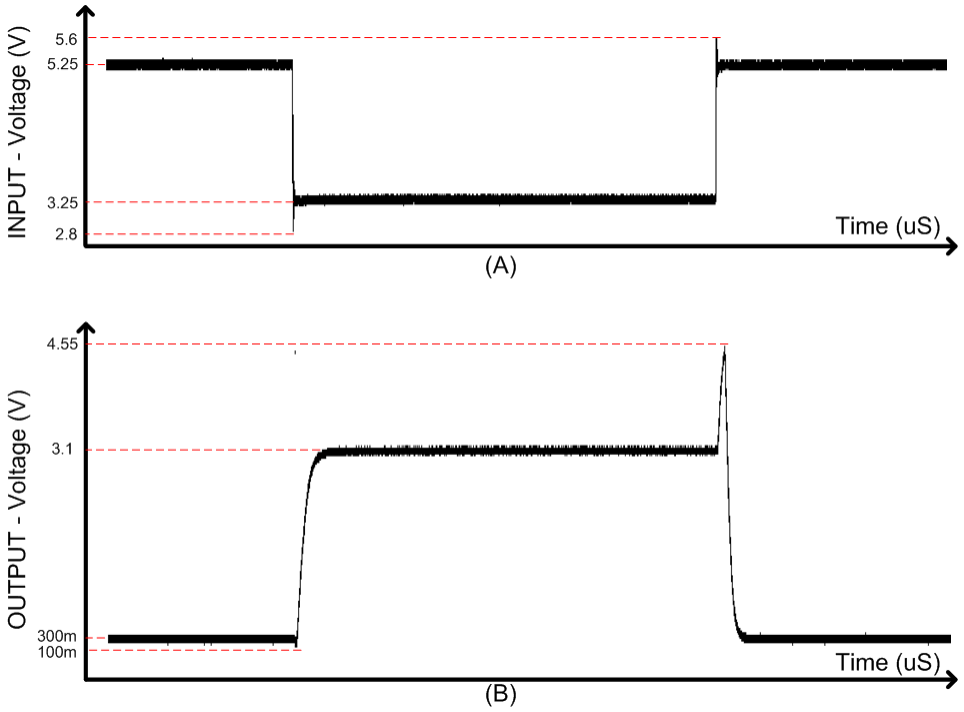

Figure 4-9: Output of UVLO 2 - Transient Measurement (A) Input Voltage, (B) Output Voltage

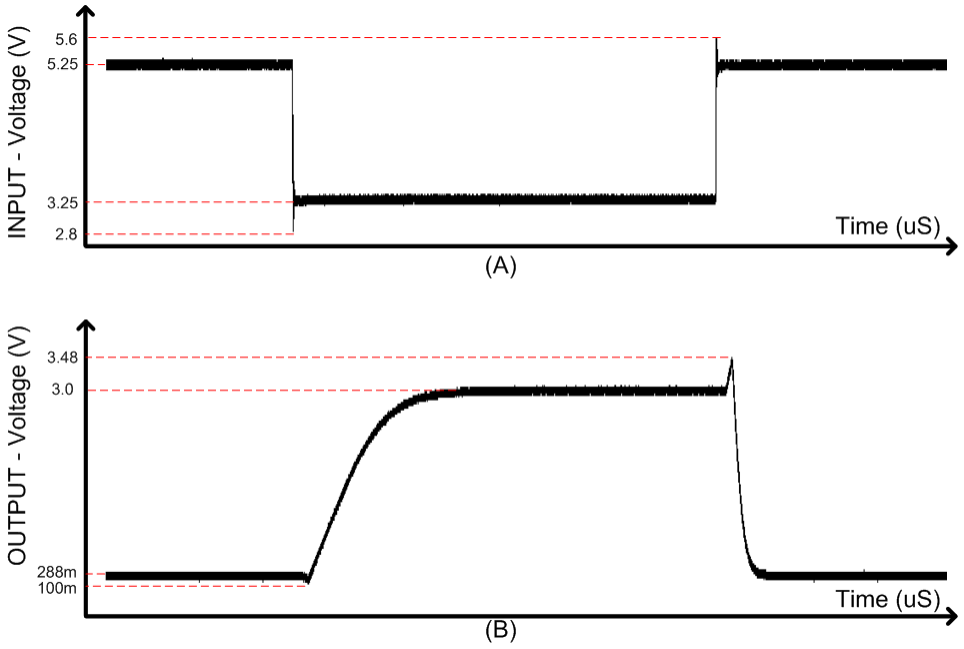

Figure 4-10: Output of UVLO 3 - Transient Measurement (A) Input Voltage, (B) Output Voltage

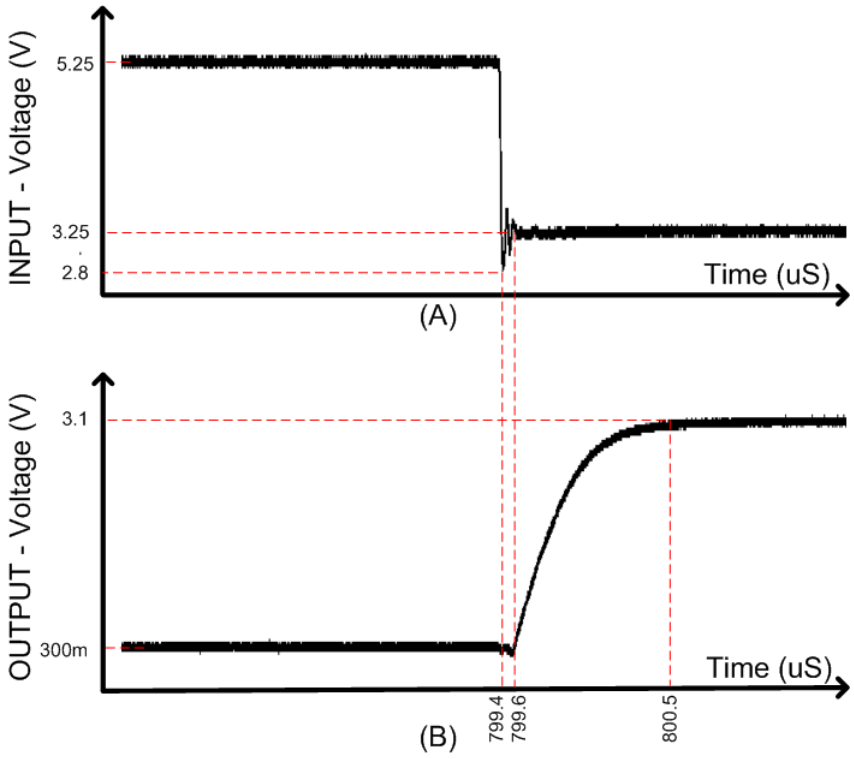

Figure 4-11: Output of UVLO 2 - Transient Measurement - Switching Point 1

room temperature. These results are comparable to the simulated results displayed in Figures 4-3 and 4-4. These results show how fast the individual UVLO circuits are able to switch states. It is important that the UVLO is able to react quickly to a drop in voltage before damage is caused to the circuit. Also, it is important for the UVLO to quickly switch states when the supply recovers. Figures 4-11 and 4-12 display a closer look at the measured times and voltages at the switching points for UVLO 2. Figures 4-13 and 4-14 display the measured times and voltages at the switching points for UVLO 3. These transient measurements were used to generate the values for Tables 4.9 and 4.10 at both room temperature and higher temperatures. The oscilloscope results at higher temperatures were not displayed because their switching point values were listed in the tables.

4.3.2 Testing the UVLOs with the OR Gate

After taking individual measurements, the two functioning UVLO circuits were connected to the input of the OR Gate and measurements were taken at the output of the OR Gate. Previously stated, the OR Gate is needed because the gate driver only accepts one signal from the under voltage protection circuit. The OR Gate allows for the monitoring of multiple supplies. The experimentally

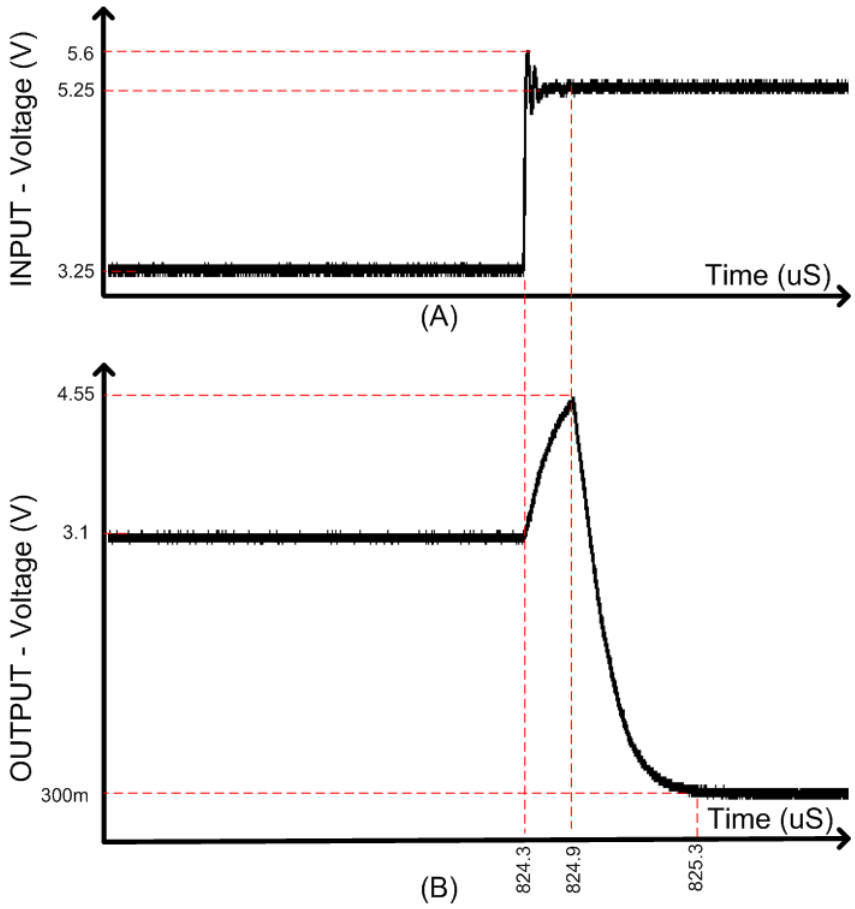

Figure 4-12: Output of UVLO 2 - Transient Measurement - Switching Point 2

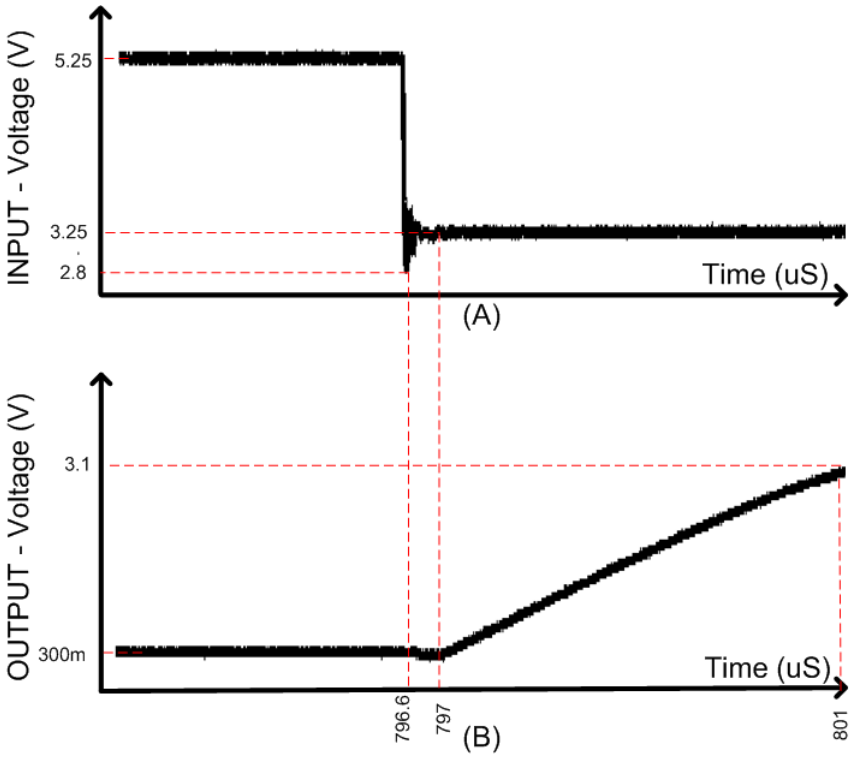

Figure 4-13: Output of UVLO 3 - Transient Measurement - Switching Point 1

measured output of the OR Gate is compiled in Table 4.11. Figure 4-15 displays the output from the OR gate.

These results should follow closely to the most restrictive inputs. For example, the output of UVLO 3 is more restrictive that the output of UVLO 2 meaning the switching points are at higher voltages. In this case, the OR Gate results should be very similar to UVLO 3 results. Notice the slight difference between the simulated and the measured results. These differences may be from the parasitics on chip and on the board. The output from the OR Gate is only dependent on the inputs from UVLO 2 and UVLO 3. Since the output of UVLO 1 is always 'high' (due to incorrect V_{REF}), UVLO 1's output is not connected into the OR Gate. Figure 4-16 displays the output from a transient sweep for the OR Gate. Figures 4-17 and 4-18 display a closer look at the switching points and the measured times and voltages at the switching points for the OR Gate. Notice the settling time for the output of the OR Gate is close to a micro-second, even with the noise in the input signal.

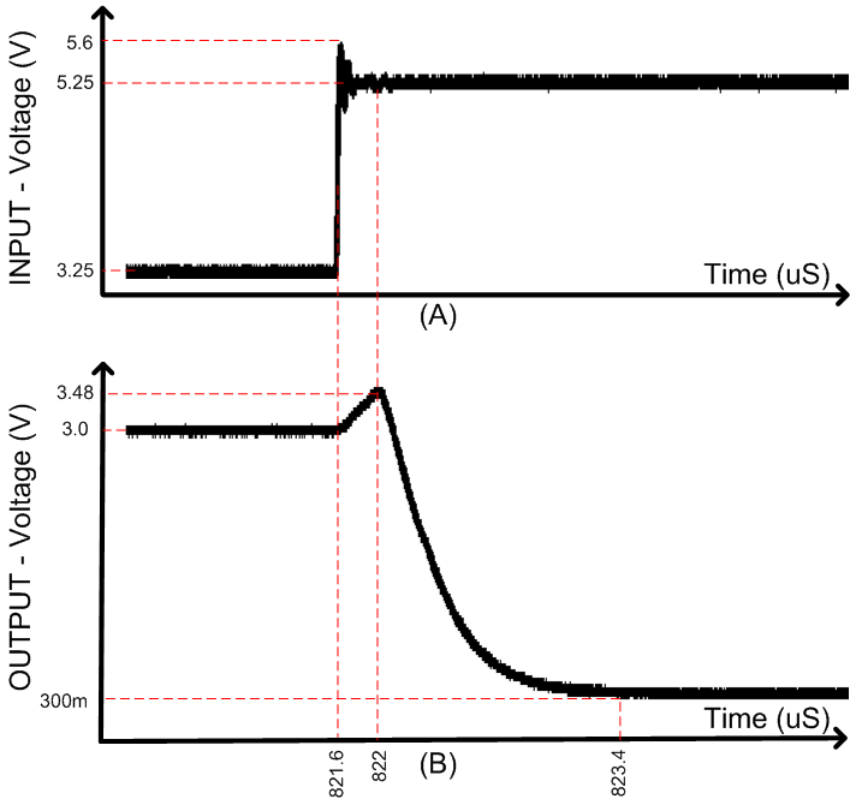

Figure 4-14: Output of UVLO 3 - Transient Measurement - Switching Point 2

Table 4.11: UVLO with OR Gate - Output of OR Gate - Post Fabrication

VDDH	Output where V_{DD} Faults		
30V	27°C	4.87V	97%
	200°C	4.85	97%
20V	27°C	4.87	97%
	200°C	4.84	97%
10V	27°C	4.86	97%
	200°C	4.84	97%

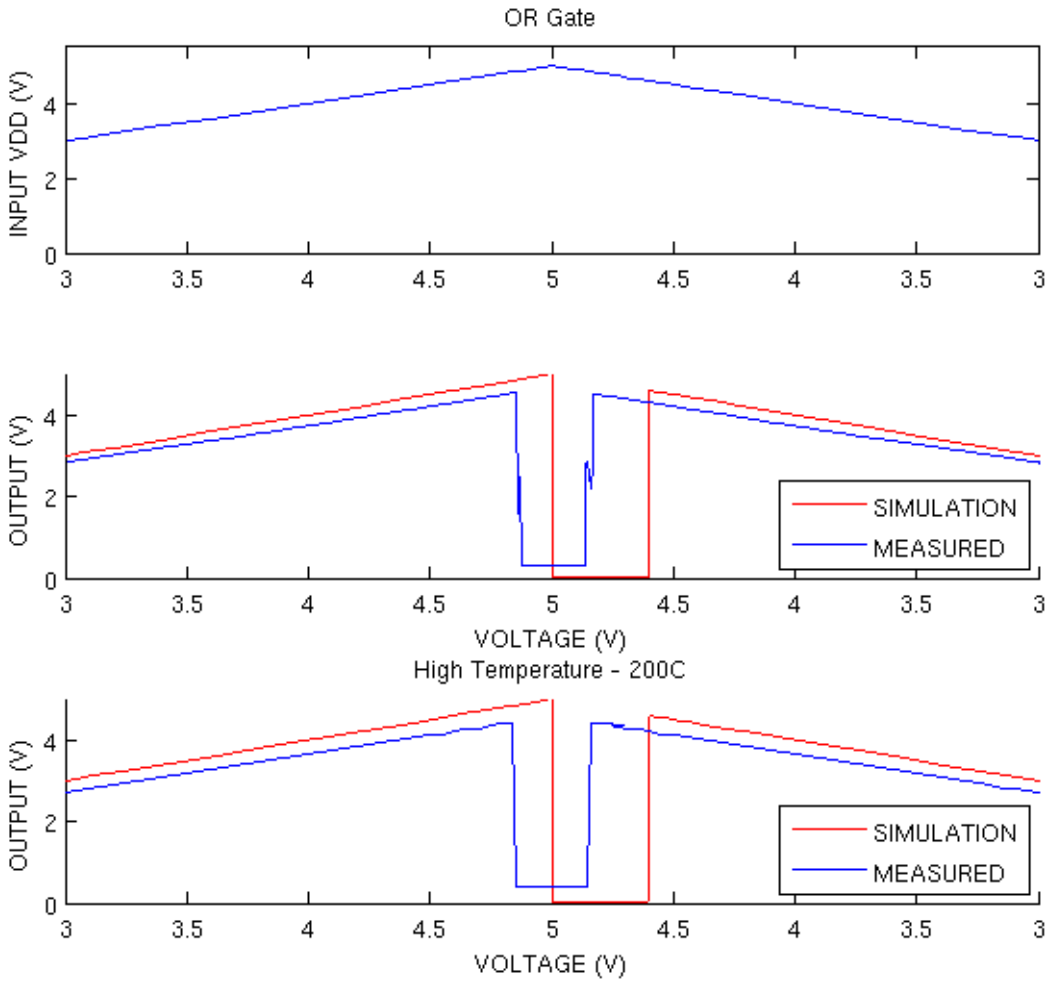

Figure 4-15: Output of OR Gate - Hysteresis Switching Points are Found from these Results

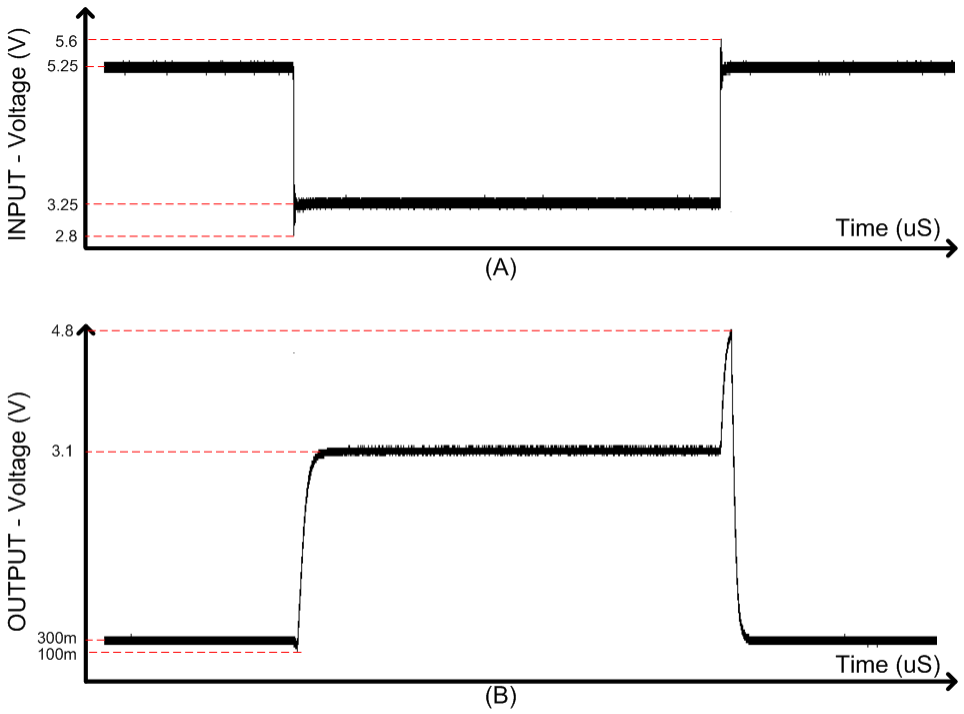

Figure 4-16: Output of OR Gate - Transient Measurement (A) Input Voltage, (B) Output Voltage

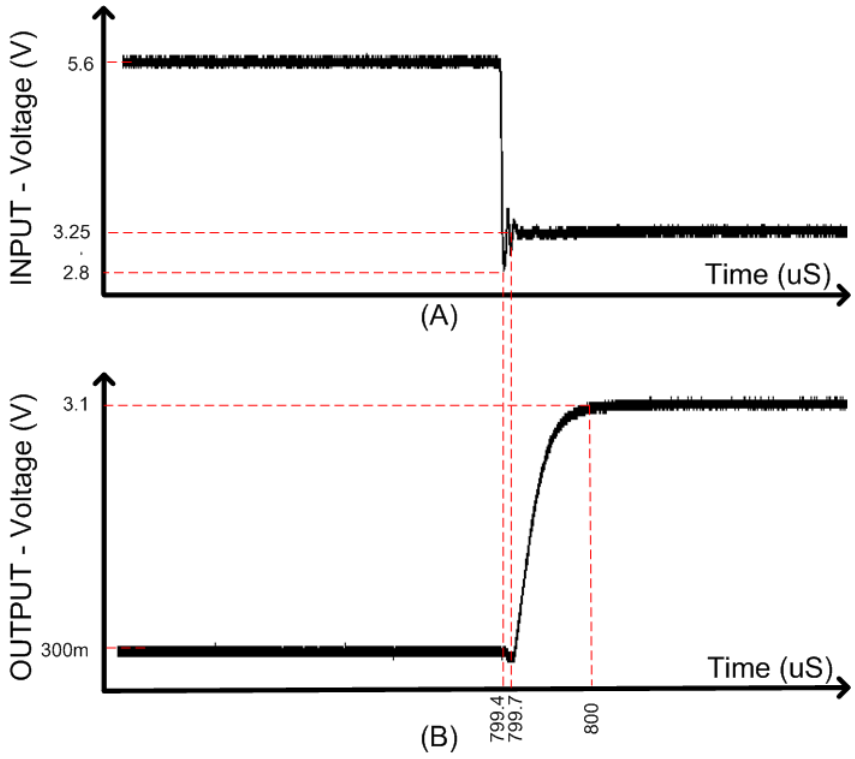

Figure 4-17: Output of OR Gate - Transient Measurement - Switching Point 1

Figure 4-19 displays the simulated DC sweep results from UVLO 1. These are only the simulated results. However, theoretically the measured results would have been very similar. It is possible to make this assumption due to the measured results from the other UVLO and OR Gate outputs. These results met the 80% threshold design goal. There is an obvious difference in room temperature and higher temperatures at the hysteresis switching points, but this is to be expected. If measured results were similar to these results they would have been very good.

4.3.3 Testing the UVLO with the Gate Driver

The under voltage lock out circuit needs to operate properly with the gate driver. For this reason, testing needs to be done to make sure the gate driver is receiving the UVLO's output and correctly reacting to it. Remember, if the UVLO detects a fault, namely a drop in the supply voltage below the threshold, it will output a high signal. The gate driver should then reset the system.

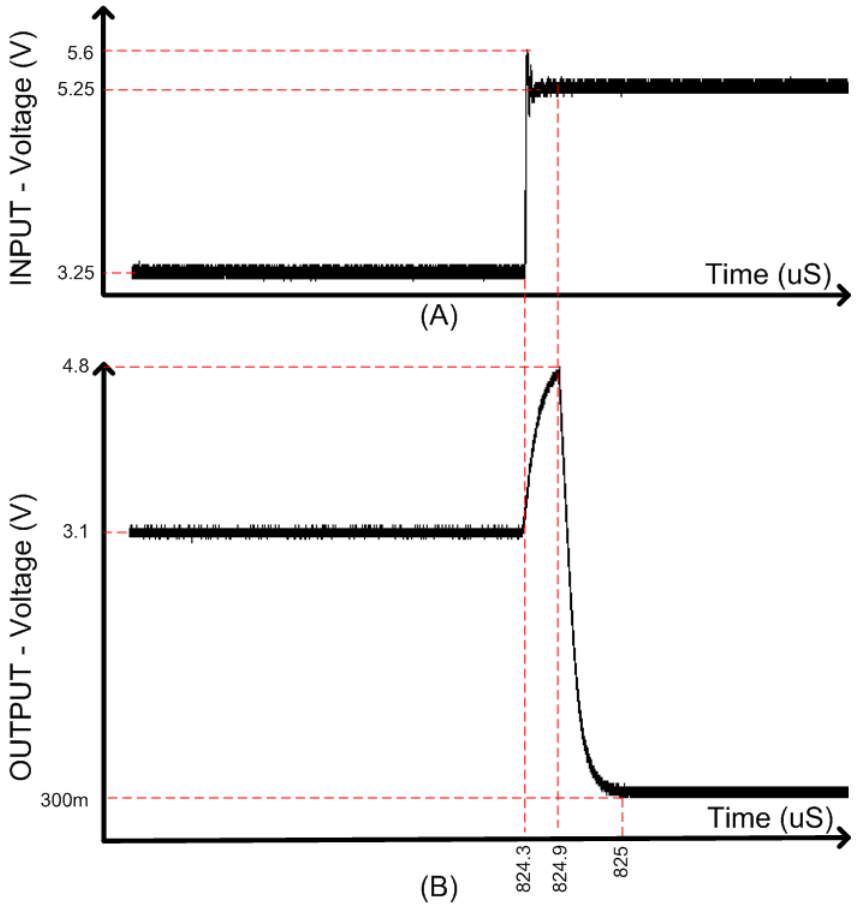

Figure 4-18: Output of OR Gate - Transient Measurement - Switching Point 2

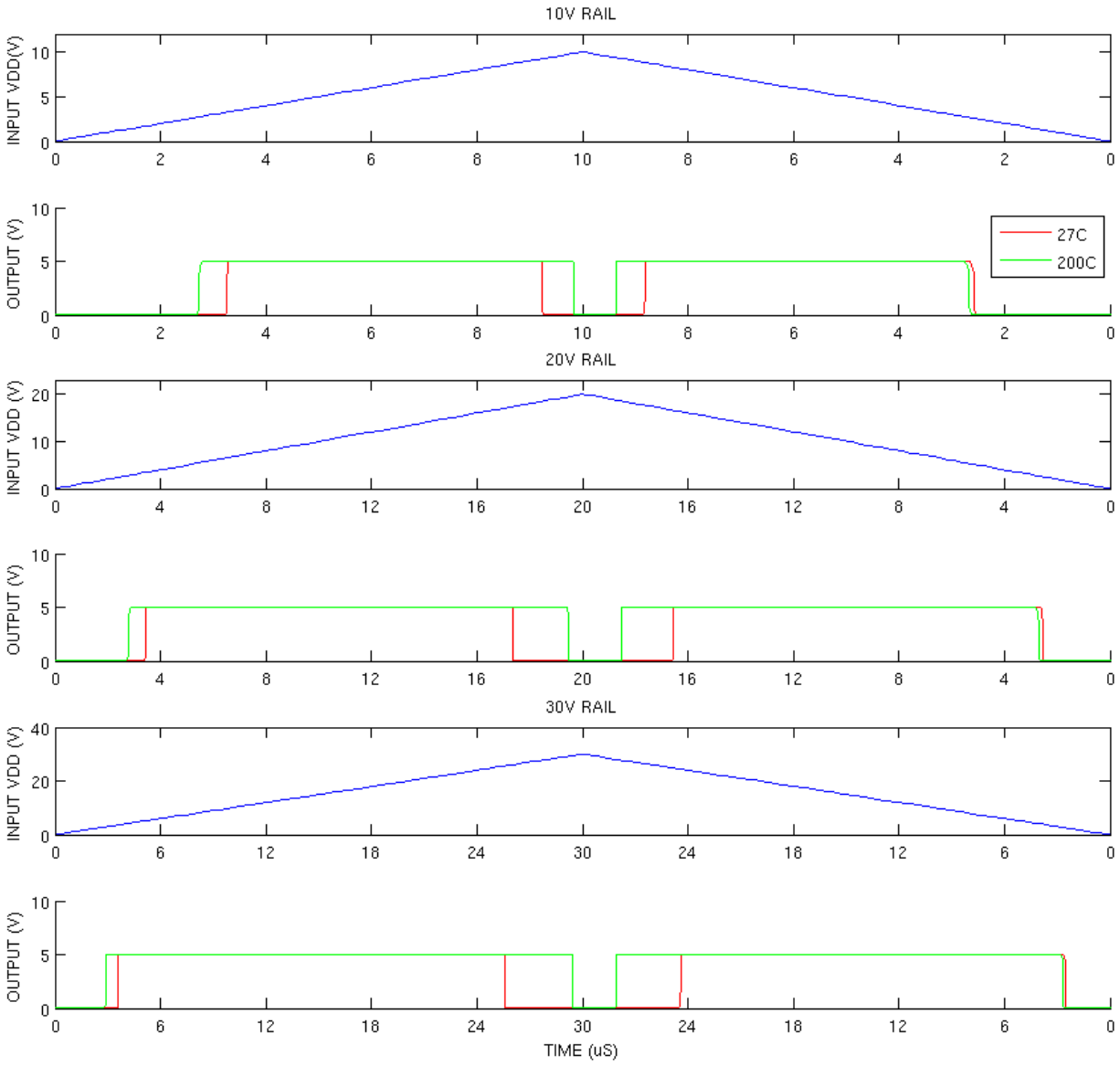

Figure 4-19: Output of UVLO 1 - Hysteresis Switching Points are Found from these Results

Chapter 5

Conclusion

5.1 Thesis Summary

The under voltage lock out circuit is very important for systems that depend on an unstable voltage supply such as batteries. This UVLO was designed to work as a protection circuit for a gate driver in a hybrid electric vehicle. Due to its location in the electric vehicle, the temperatures the electronics reach are beyond that of military grade electronics. This puts them in the extreme environment electronics group. For this reason, simulation and testing needed to be performed across a wide temperature range. After extensive testing of the under voltage lock out circuit, results were encouraging. There were some issues with the reference voltage in UVLO 1. This is due to the zener diode not turning on properly. However, UVLO 2 and UVLO 3 operated very well at room temperature and at high temperatures. Since the same comparator was used in UVLO 1 as UVLO 2 and the results from UVLO 2 were good, theoretically UVLO 1 should operate correctly. Correcting the issue with reference voltage would allow for future testing.

5.2 Future Work

The next logical steps would be to fully integrate the UVLO into the gate driver. Integration of the off-chip selection of resistance within the resistor bank in UVLO 1 would be another improvement to UVLO 1's layout. Instead of using jumpers on the board to select resistance values, a multiplexer could be added to the UVLO system forcing an on-chip selection. This would reduce the amount of pins needed as well as the parasitics. If satisfied with the results of the individual UVLO circuits,

the outputs of the individual UVLO circuits can be directly connected to the input of the OR gate without coming off-chip. Since this was the first revision for the UVLO, several test points were needed. These test points will not be needed on the next run of the UVLO circuit. Finally, the current the UVLO circuit is a very conservative design. The gate driver does not need such a conservative circuit. The switching points (or hysteresis points) can be moved according to better fit needs of the gate driver. This can be done through re-sizing the transistors on the input stage of the comparator.

There are a few options to resize the hysteresis of the comparator used in UVLO 1 and UVLO 2. Since the hysteresis depends on the ratio between M10 and M3 for the positive switching point, increasing the multiplier of M10 would move the switching point out. This means that the UVLO would send a fault at a lower voltage (lower percentage). The negative switching point depends on the ratio between M11 and M4. By reducing the multiplier of M4, the ratio would also shift the switching point. The means that the UVLO would fault at a lower voltage. If a more conservative design is needed, simply the opposite needs to be done and the UVLO will fault at a higher voltage (larger percentage).

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Vita

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