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Gate Drive Design for Paralleled SiC MOSFETs in High Power Voltage Source Converters

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I am submitting herewith a thesis written by Craig Timms entitled "Gate Drive Design for Paralleled SiC MOSFETs in High Power Voltage Source Converters." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

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Gate Drive Design for Paralleled SiC MOSFETs in High Power Voltage Source Converters

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ABSTRACT

High power voltage source converters (VSC) are vital in applications ranging from industrial motor drives to renewable energy systems and electrified transportation. In order to achieve high power the semiconductor devices used in a VSC need to be paralleled, making the gate drive design complicated. The silicon carbide (SiC) MOSFET brings much benefit over similarly rated silicon (Si) devices but further complicates the gate drive design in a parallel environment due to it's fast switching capability and limited short-circuit withstand time. A gate driver design with proper accommodation of key issues for paralleled 1.7 kV SiC MOSFETs in high power VSC applications is developed.

Three of the main issues are current imbalance, short-circuit protection, and cross-talk. By characterizing devices and supporting circuitry an understanding of constraints and sensitivities with regards to current balance between devices is developed for design optimization. A short-circuit detection scheme with adequate response time is employed and mitigation steps presented for issues arising from paralleling devices including large transient energy and instability. *Cdv/dt* induced gate voltage—cross-talk—is addressed by adapting a mitigation method to multiple devices. Finally, the gate driver is demonstrated in a full scale half-bridge using four devices per switch.

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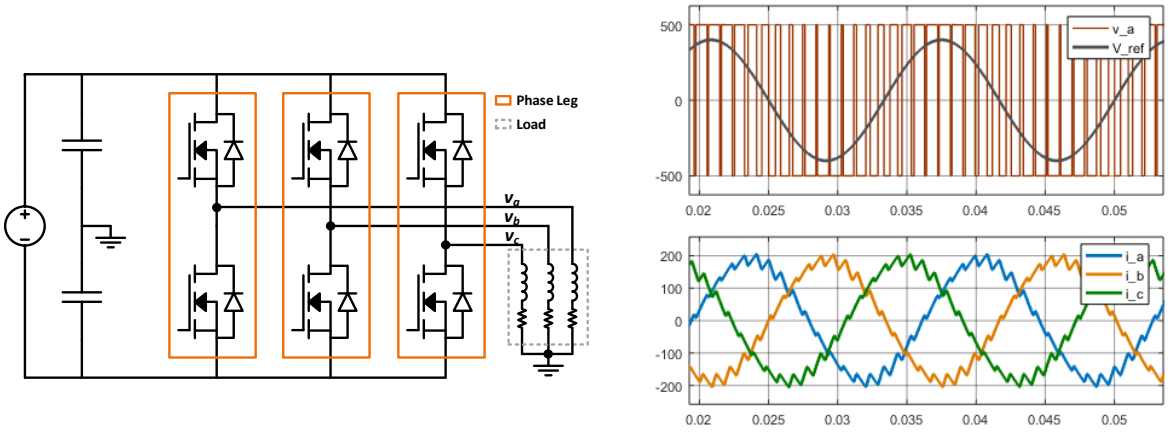
1 INTRODUCTION

In this section the voltage source converter (VSC) is introduced specifically as it is used for high power motor drives. The application in wind power generation will show the value of working towards more ideal switches as a building block for system level improvements. The SiC MOSFET is introduced as the most promising semiconductor switch for this application space. With this context, the motivation and objective of this thesis are presented. Finally, a general outline of the thesis is given.

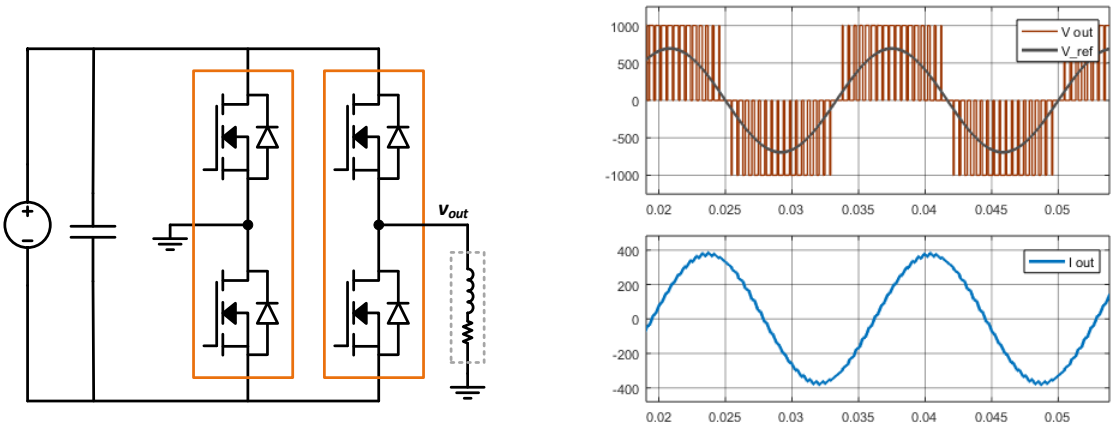
1.1 VOLTAGE SOURCE CONVERTERS IN HIGH POWER APPLICATIONS

AC motor drives are found in transportation (electric vehicles, trains, airplanes, and ships), industrial (pumps/compressors, paper and textile mills, rolling and cement mills), and power generation (wind, natural gas). The Electric Power Research Institute (EPRI) estimates that 60% of grid energy in the USA is consumed in electrical machine drives [1]. With a large majority of current applications using inefficient fixed-frequency drives, this area is ripe for progress.

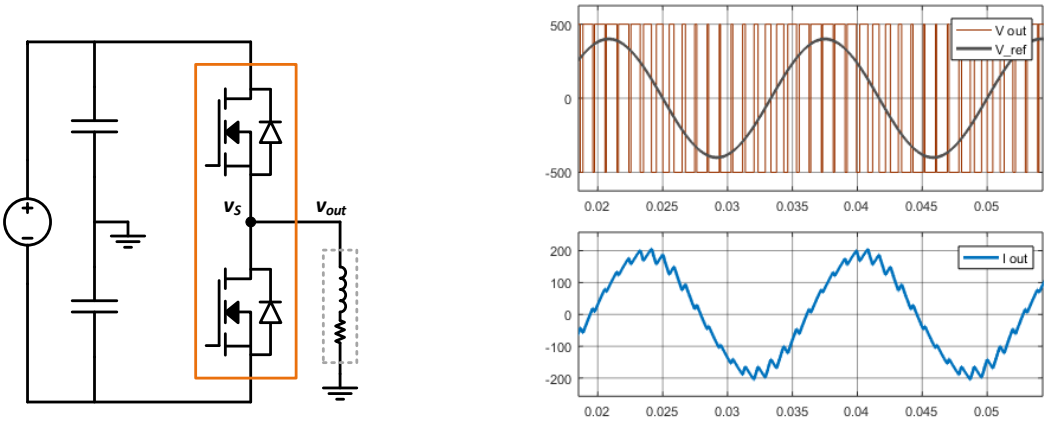
The voltage source converter is one of the most effective and mature means of controllable AC to DC conversion. By using switches to ‘chop’ a DC voltage across an inductive load—in this case a motor—behaves as an averaging filter creating AC current. Common applications require three phase current. A two-level three-phase VSC along with output waveforms are shown in Fig. 1 (a). The same principle is applied for a single phase AC current with a full-bridge (b) or a simple half-bridge (c). Variable frequency to better follow load and increase efficiency is accomplished using fully controllable switches—switchable regardless of current or voltage state.



(a) Three-phase



(b) Full-Bridge



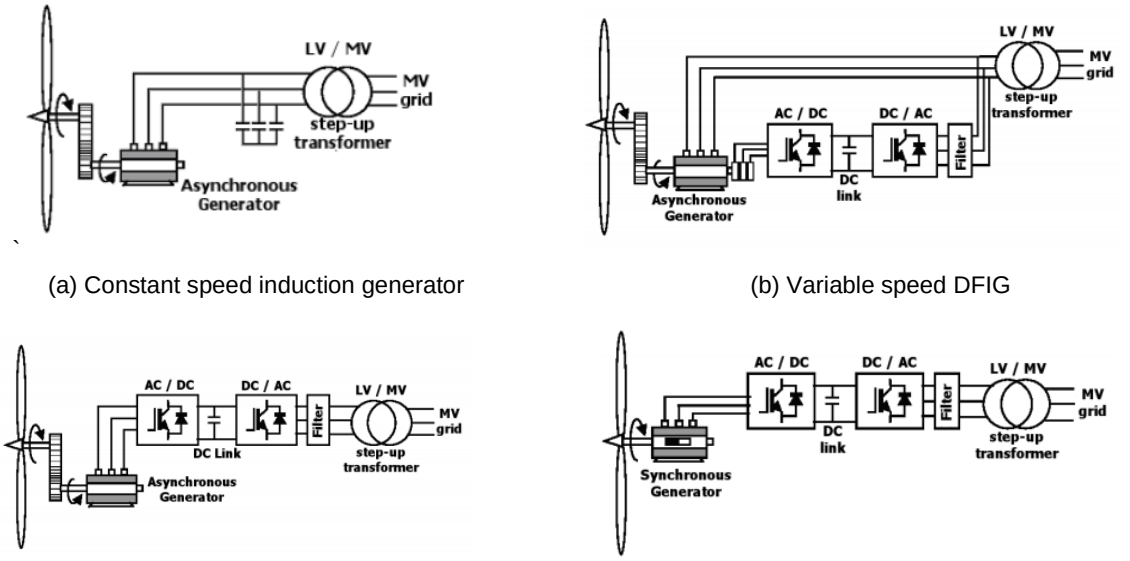
(c) Half-Bridge

Fig. 1. Phase-leg in VSC configurations

The four main configurations of wind power systems are shown in Fig. 2. The simplest configuration is the constant speed induction generator (IG) which directly couples the generator to the AC grid. Inefficiency occurs because maximum power output only occurs when the blade frequency is proportional to the grid frequency. The doubly-fed IG configuration improves efficiency by utilizing a VSC to transfer the extra power that would be lost in the previous case when the frequency of the blade does not match the grid. This is one of the most popular configurations because the VSC power rating only needs to be 30% of the overall system rating. Complete decoupling of the asynchronous machine and grid is accomplished using a VSC in the variable speed IG configuration. This allows full power transfer at any blade speed but requires a VSC rating equal to the system rating. Using the same VSC configuration as just mentioned but replacing the asynchronous generator with a synchronous generator utilizes higher speed VSC to remove the large mechanical gear box. Though more compact and potentially more efficient the permanent magnet generator is much more expensive and doesn't have the proven reliability of asynchronous induction machines [2].

The two level topologies in Fig. 1 are most popular to the relatively low voltage machines used in these applications. Switching frequencies of just a few thousand hertz are able to produce acceptable current waveforms for the machines. The progress in this space will come from increasing output and minimizing the size of the systems. From a system perspective, direct paralleling of devices is the simplest means to increase output power. Theoretically, output power can scale directly with number of devices in parallel—output power increases n times where n is the number of devices in parallel—due to the increased current carrying capability. Compared to placing multiple

converters in parallel there is no need for added control and other complexities like coupling inductors.



(a) Constant speed induction generator

(b) Variable speed DFIG

(c) Variable speed IG

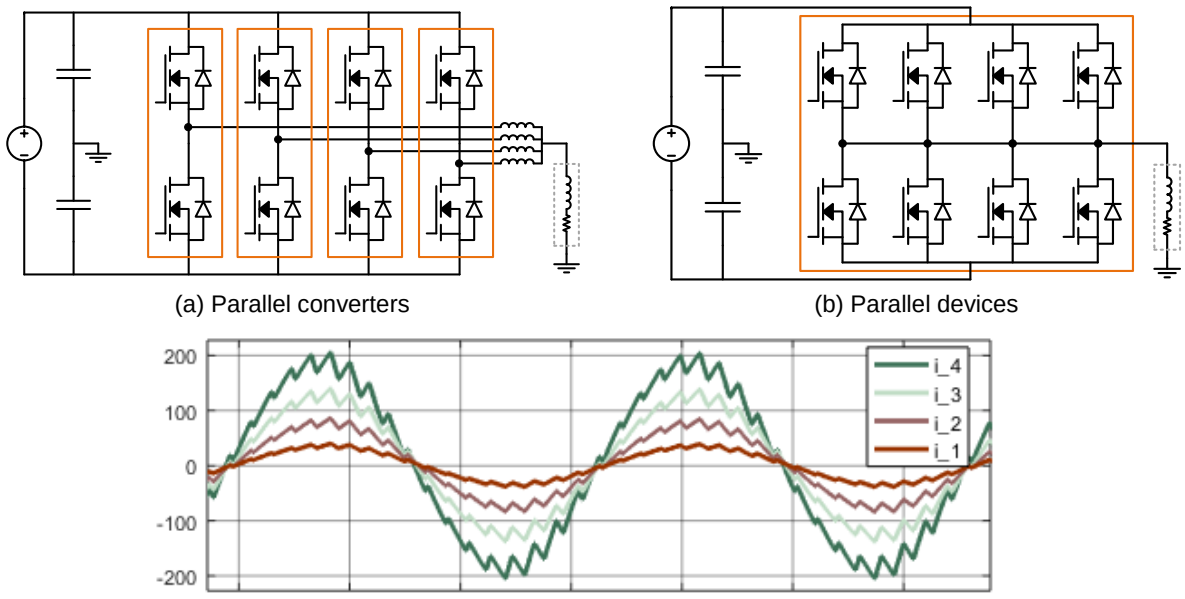
(d) Variable speed PM synchronous generator

Fig. 2. Wind turbine systems

These two option for increasing system output are shown in Fig. 3. In (a) four half-bridge phase legs are paralleled and in (b) four devices are directly paralleled to form one half-bridge phase leg. For a given voltage level—typically 690V for a wind generator—output power is a function of current capability. Fig. 3 (c) shows the output current increase as a function of paralleled legs or devices and is the same for either means. The main difference is that with paralleled converters, extra control may be required to keep the current balance. With parallel devices, the control can treat the setup as a single phase leg. Though there are complexities in obtaining an equivalent

switch from multiple devices, if done correctly, these complexities are controlled and kept in the switch itself without added load or processing for the system.

To understand what an ideal switch from multiple devices an ideal switch must first be defined. An ideal switch is one that turns on or off instantaneously or rather has a very short switching time. The downstream effects of non-ideal switching in a VSC are laid out in Fig. 4 (a) and the problems caused by sharp transitions in (b). The next section discuss why SiC MOSFETs are the best option for an ideal switch high power applications while the remaining thesis deals with mitigating the issues this causes.

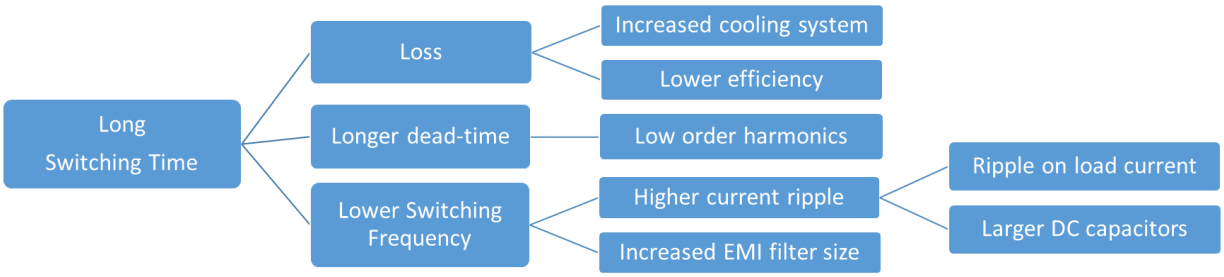


(a) Parallel converters

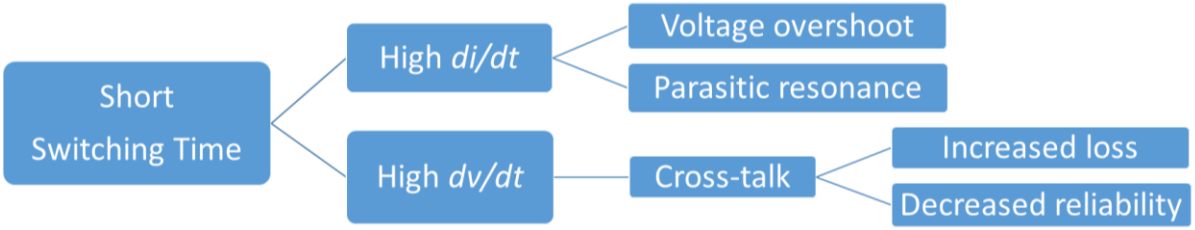
(b) Parallel devices

(c) Increasing output current

Fig. 3. Increasing output power of VSC



(a) Downstream effects of non-ideal switching

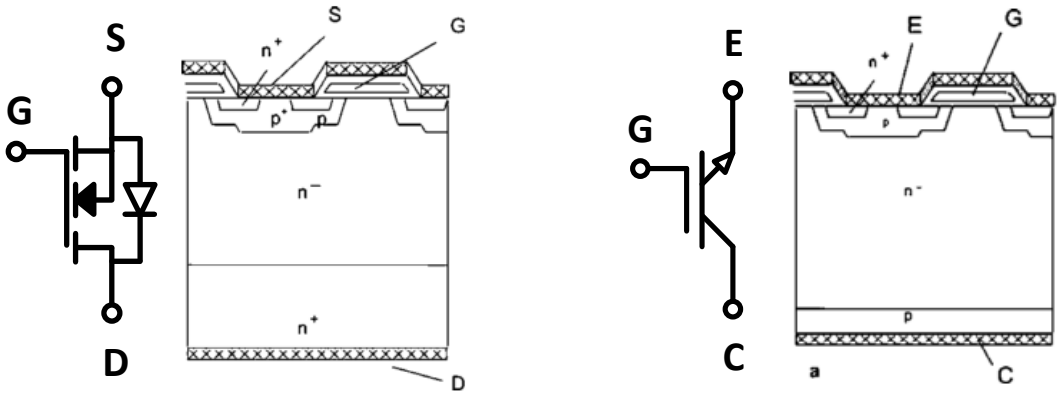


(b) Problems caused by more ideal switching

Fig. 4. Effects of increasing and decreasing switching times

1.2 SiC Wide Band Gap MOSFETs

Over the last few decades the silicon IGBT has driven the development in this application space. By combining the current carrying and high blocking voltage capability of a bipolar transistor and the simple MOS gate control a truly influential device was born. MOSFETs were not possible at significant voltage blocking levels due to the inverse relationship of blocking voltage to on-state resistance of middle n-layer. That is, the height of the epitaxial middle layer determines blocking voltage in the off state but the larger this layer the higher the resistance during conduction. The IGBT used the same gate principle of creating an n-channel by applying a gate voltage but the addition of the p-layer at the collector allows injection of holes into the n-layer during conduction increasing charge carrier density lowering the effective resistance. By mitigating the larger effective resistance with larger epitaxial layers, the IGBT enabled higher voltage blocking with silicon devices.



(a) MOSFET (b) IGBT

Fig. 5. Symbol and structure of power semiconductor devices

With the maturation of silicon carbide (SiC) process technology the MOSFET structure has been given new life in high voltage devices. SiC has nearly 3 times the critical electric field of silicon. This allows for a much thinner epitaxial n^- layer at higher blocking voltages enabling high current MOSFETs at blocking voltages previously only achievable with IGBTs. Before comparing the two devices, a more detailed description of the operation of semiconductor switches in the VSC will be discussed.

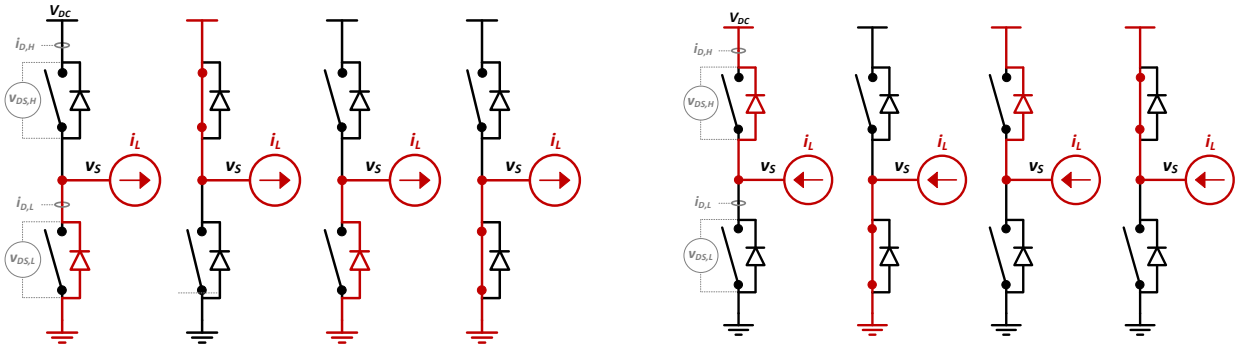
From the VSC waveforms in Fig. 2 there are two distinct conditions: when the load current is positive and when it is negative—flowing out of the switch node or into the switch node. In Fig. 6 a switching cycle is shown for each load current case in order to illustrate the current commutation between devices. In either case, current needs to conduct through a free-wheeling diode when both switches are off, the associated switch is considered the non-active or synchronous switch. The other switch is the active switch because it controls the current flow and consequently the switch node voltage. That is, when the active switch is off it is blocking voltage and not conducting current. When it is on, it is conducting current and the switch node is pulled high or low—high if the high side switch or low if the low side switch.

Three advantages of the SiC MOSFET in this structure are depicted in Fig. 7. First, in the on-state the MOSFET has a linear *VI* relationship whereas the IGBT has a similar relationship but after a 1-2V drop. Fig. 7(a) illustrates this and the larger light-load losses this will cause. Second, the MOSFET has an inherent internal body diode and can reverse conduct through the channel. This means that an external free-wheeling diode is required with an IGBT and conducting current through this during the

non-active switch state previously described creates more loss than conduction through the MOSFET channel. Silicon diodes tend to have reverse recovery current shown in Fig. 7(b) that adds loss at current commutation. The body diode of a SiC MOSFET has close to zero reverse recovery current. Finally, at turn-off of an IGBT the carriers injected into the n-layer do not exit immediately. This delay causes a tail current illustrated in as shown in Fig. 7(c). This extra current/voltage overlap increases switching losses and also increases switching time.

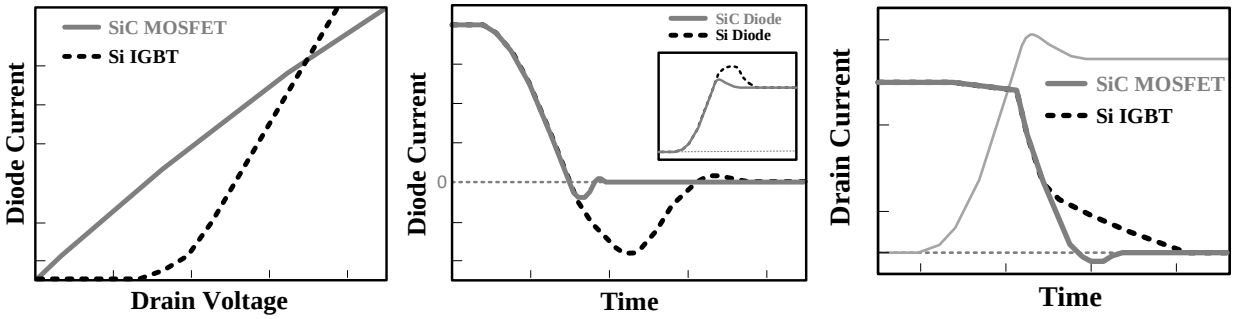
For many reasons the SiC MOSFET provides a great building block for a more ideal high power switch, but as listed in Fig. 4(b) there are many negative effects of shorter switching times. These negative effects steam from the *di/dt* and *dv/dt* inherent in switching high current and voltage in a short amount of time. Note the first switching transition in Fig. 6(a). SiC MOSFETs enable very large current commutation from the low-side to high-side in 10s of nanoseconds. Along with this, voltage across the switch can transition from >1kV to 0 in the same amount of time. Careful consideration needs to be taken when implementing this kind of performance.

The basic structure for controlling devices in this environment is shown in Fig. 8. Both signal and power input into the gate drive circuit must be isolated due to the source potential voltage swing. Some form of gate buffer will be required for high frequency and parallel devices. Gate regulation is needed to deal with the dv/dv induced cross-talk. Finally, SiC MOSFETs are much less robust in short-circuit events and require fast and adequate protection circuitry.



(a) Positive load current (b) Negative load current

Fig. 6. Current commutation between switches during switching transitions



(a) Output curve (b) Reverse recovery of diode (c) Turn-off tail current

Fig. 7. IGBT shortcomings

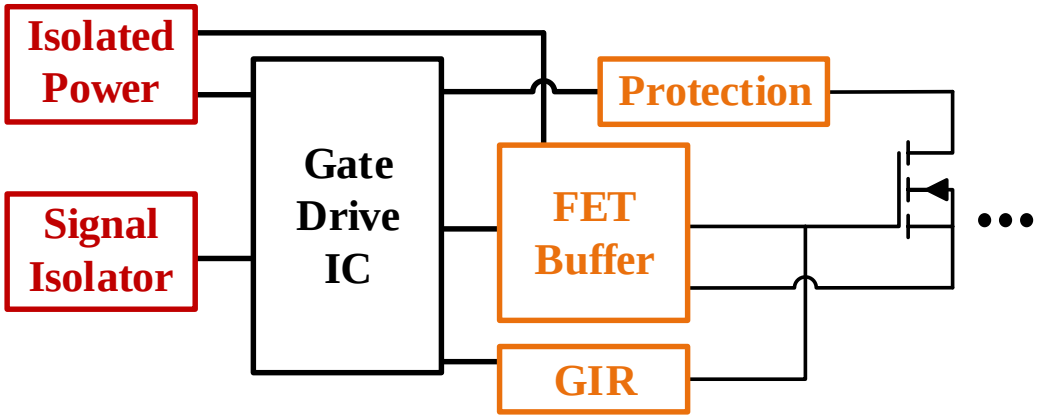


Fig. 8. Required functionalities for SiC gate drive

1.3 MOTIVATION AND OBJECTIVE

SiC devices—especially MOSFETs—are extremely promising for expanding technologies in the high power space like wind due to their high voltage blocking and current carrying capability. Many applications demand more power—100s of kWs to MWs—than single chips can deliver. There are many issues that arise paralleling SiC MOSFETs in high-performance applications that are not yet fully understood.

An issue with any parallel power devices is unequal current distribution that can lead to improper load balance, which limits performance and reduces reliability. It has been shown that non-uniformities between devices are significant and cause current imbalance [3]. Also, with fast switching SiC devices parasitic inductances caused by layout and high *di/dt* create feedback mechanisms that lead to current imbalance [4].

Second, known issues with SiC are compounded with devices in parallel. It is well established that parasitic elements in power and gate loops have significant performance impacts due to high *di/dt* and *dv/dt* of SiC devices [5, 6]. Oscillation during normal operation can occur in fast switching circuits causing self turn-on [7, 8]. Also spurious gate current from high *dv/dt* switching transients—cross-talk—can cause false turn-on and shoot-through current leading to extra loss and reduced reliability [9, 10]. These issues have been extensively studied with single devices but how exactly they extend to parallel devices has yet to receive much attention.

Third, gate stability issues arise due to parallel connection of devices. Low impedance loops are created with parallel gates and oscillation between gates has been observed under normal switching [11, 12]. Oscillations during short-circuit conditions

have also been observed in similar gated Si devices including IGBTs [13, 14]. Most of the work in this area is still just with Si devices.

Of the issues mentioned, unequal dynamic (switching transition) current distribution has received the most attention when looking at SiC devices in parallel. Passive solutions have been proposed [15, 16]. As well as active solutions with silicon devices [17-20]. An active current feedback approach with SiC has been demonstrated [21] as well as delay compensation based on temperature [22].

The motivation for this work is first, most of the solutions proposed are focused on individual switching transitions and do not address the system level perspective or other known issues with SiC. Second, very little has been done on short circuit considerations for parallel SiC devices which is critical considering time to failure is much shorter for SiC than similar Si devices. Furthermore, Si gated devices have shown destructive potential in parallel operation. Third, no published work has dealt with >1 kV environments and very few with more than a few amps per paralleled device.

This thesis proposes an integrated design approach to mitigate the drawbacks that come with SiC MOSFETs in parallel to provide solutions that ultimately increase power capability and performance of VSCs as well as add more design freedom at a lower cost. The main focus will be on the approach to gate drive design with parallel devices in order to realize SiC benefits in high power applications. By solving the issue of current scaling at the individual device level through paralleling devices the overall converter design is significantly simplified.

1.4 OUTLINE OF THESIS

This thesis presents a gate driver and single phase-leg power stage design using parallel SiC MOSFETs aimed at systems with DC bus voltages up to 1.5 kV and current up to 200A. This includes fast switching capability with cross-talk mitigation and fast short-circuit protection during fault events.

In Chapter 2, the state-of-the-art approaches to paralleling SiC power devices are presented. Then from the gate drive perspective the state-of-the-art approaches to mitigating cross talk and short-circuit failures are reviewed.

Chapter 3 provides a thorough analysis of datasheet parameters, how they vary between different chips and across temperature, and how this effects system level performance. Lab results will be used comparing 16 devices with the same manufacturer part number. Also, a short overview of power stage design for optimizing SiC MOSFETs in parallel will be given.

Chapter 4 shows simulation and experimental results for fast short-circuit protection then discusses instability that can occur as a result of paralleling devices and how to mitigate this potentially destructive side effect.

Chapter 5 presents the design methodology for achieving fast switching, anti-cross talk, and optimized parallel current sharing. Simulation and experimental results are presented both in a detailed setting through a double pulse setup and in a system level continuous phase leg setup.

Chapter 6 gives conclusions of the work detailing features that could further improve the integrated design of the gate drive circuit and parallel high power dies.

2 LITERATURE REVIEW

Though promising, achieving robust and reliable parallel operation of devices is extremely challenging, especially while maintaining the fast switching and low loss benefits of SiC devices. Three major issues that arise when paralleling SiC devices are: unequal current distribution, fast slew rates, and stability concerns. This section presents work done to understand the underlying mechanisms as well as proposed solutions to these three challenges to paralleling SiC MOSFETs.

2.1 CURRENT DISTRIBUTION IN PARALLEL DISCRETE DEVICES

Due to many factors in semiconductor manufacturing even chips from the same wafer will have some variation in many datasheet parameters. These discrepancies effect how current is distributed between parallel devices. Along with this, discrepancies in parasitic inductances within power and gate loops lead to di/dt induced feedback on the different gate voltages which also effects current distribution. The two significant losses in SiC MOSFETs come from conduction periods and switching periods, thus the mechanisms behind static current sharing and dynamic current sharing are presented before overviewing a proposed solutions.

2.1.1 Static Current Sharing

MOSFETs as power semiconductor switches behave as a small resistance during the conduction phase of operation. The benefit is clear that devices in parallel have a reduced equivalent $R_{DS(ON)}$. The drawback though is current will distribute unequally as modeled by parallel resistances. This leads to the lower resistance devices carrying the higher current and therefore incurring the more loss. The lowest resistance device is the

limiting factor for overall current which will be less than n times the max current of a single device.

When looking just at static current the worst case will be when one device has a very low $R_{DS(ON)}$ and all remaining devices have maximum $R_{DS(ON)}$. This case yields a simplified equation in [23] which allows for a starting point for how many devices are required for a given output current as well as an idea of the significance of $R_{DS(ON)}$ spread. When just looking at static current a down rating of at least 0.8 from n times single device current capability should be expected.

$$I_{max} = \frac{\left({R_{DS(ON)max}}/{(n-1)}\right)}{R_{DS(ON)min} + \left({R_{DS(ON)max}}/{(n-1)}\right)} \cdot I = \frac{1}{1 + \frac{R_{DS(ON)min}}{R_{DS(ON)max}}(n-1)} \cdot I \quad (1)$$

A beneficial feature of MOSFET devices is that $R_{DS(ON)}$ almost always has a positive temperature coefficient (PTC). This creates an inherent feedback loop for current sharing. That is, the hottest device—due to having the lowest $R_{DS(ON)}$ and conducting the most current—will naturally increase $R_{DS(ON)}$ reducing its share of current. This inherent feedback system is not as promising with SiC as was the case with Si MOSFETs. $R_{DS(ON)}$ at 150°C vs. 25°C for Si CoolMOS devices have been reported around 2.6 times whereas SiC at just 1.2-1.5 times[3]. Even though SiC $R_{DS(ON)}$ does have a PTC it is not as pronounced as Si MOSFETs.

2.1.2 Dynamic Current Sharing

SiC is desirable for high switching frequency switching potential. With this, switching losses are already a very important factor in design. With parallel devices another layer is added. Any difference in current distribution between parallel devices

during this period of current and voltage overlap can cause significant imbalance in losses between the devices. From the device perspective, transient current in MOSFETs is a function of transconductance (g_{fs}) and threshold voltage (V_{th}):

$$I_D = g_{fs} \cdot (v_{gs} - V_{th}). \tag{2}$$

The above equation clearly demonstrates the issue with unequal V_{th} between parallel devices. That is, devices with relatively low V_{th} or high g_{fs} carry more dynamic current and therefore incur greater switching loss. Threshold voltage can vary between devices as much as 25% [3]. Though this discrepancy should improve as SiC fabrication processes mature it is doubtful to be completely eliminated and no research exists on long term effects.

Another cause of current imbalance during switching transients is circuit layout. Even a very small parasitic common source inductance (L_{CS}) mismatch between parallel devices turns the high *di/dt* seen with SiC into a negative gate voltage feedback. This feedback is shown in the equation for v_{gs} and the effect is seen in current difference using Equation 2 and equal g_{fs} and v_{th}.

$$v_{gs} = V_{driver} - i_g R_g - L_{cs} \frac{di_s}{dt} \tag{3}$$

$$i_{d1} - i_{d2} = g_{fs}(L_{s2} - L_{s1}) \frac{di_L}{dt} \tag{4}$$

Accordingly, during turn-on a device with relatively large L_{cs} turns on slower and so carries less current causing switching loss imbalance. During turn-off relatively large L_{cs} causes a device to turn off faster and therefor has an opposite effect as turn-on by decreasing loss. This has been demonstrated experimentally in [4, 24]. These two

dynamic current imbalance mechanisms are illustrated in Fig. 9. Detailed models on design implications or approaches are still needed.

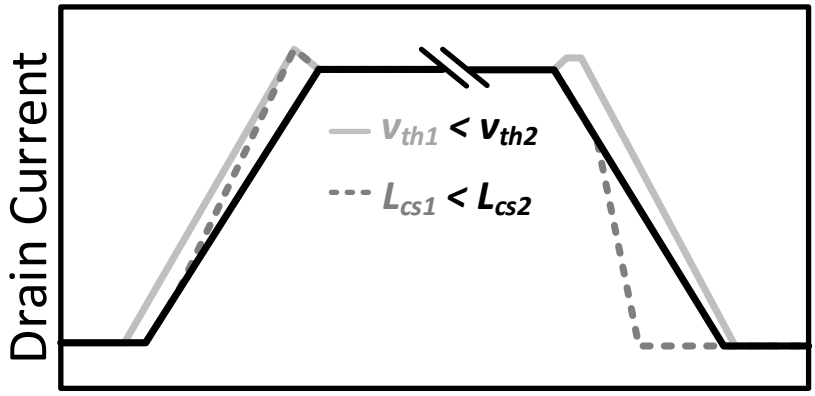


Fig. 9. Effects of V_{th} and L_{CS} variation on dynamic current sharing in parallel devices

2.1.3 Proposed Solutions for Parallel Current Imbalance

A few different solutions for current imbalance have been proposed. All of which have focused on dynamic current sharing. Broadly, they can be characterized as passive or active solutions. Passive solutions are presented first, followed by active.

2.1.3.1 Passive current imbalance mitigation schemes

The authors in [3] characterized the $R_{DS(ON)}$ and V_{th} of 30 1200V SiC MOSFETs. Paralleling two devices with significantly different V_{th} the effect of gate resistance was analyzed. Starting with a double pulse test (DPT), by reducing gate resistance from 41 Ω to 5 Ω switching loss difference between devices reduced from 20.3% of total current to just 7.3%. Furthermore, a continuous SEPIC converter validated the DPT results with a noticeable reduction in ΔT achieving a ΔT of just 9ºC at 100 kHz.

In [16] a number of SiC MOSFETs were also characterized to find their V_{th}. External gate resistors and extra source inductance was added to the standard double pulse test setup as shown in Fig. 10. With the two devices in parallel Eq. 5 was derived using Eq. 2. Setting the maximum allowable peak current difference R_k and L_s are solved for. By adding ~30nH to the DPT circuit, the authors were able to reduce dynamic current difference with nearly no additional total current loss.

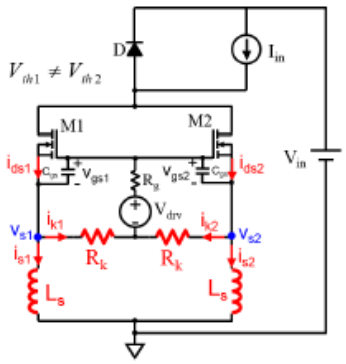


Fig. 10. DPT schematic for a proposed passive current compensation method

$$i_{ds1(pk)} - i_{ds2(pk)} = \frac{V_{th2} - V_{th1}}{R_k} + \frac{V_{th2} - V_{th1}}{L_s} \cdot t_r \tag{5}$$

In [4] a current coupling mitigation method is developed to mitigate asymmetries in modules that lead to L_{cs} induced dynamic current imbalance. The parasitic inductance that these asymmetries cause are depicted in Fig. 11. Like the previous reference, the authors start with Equation 2 to form a matrix equation for the various extra inductances that account for the selected four device module asymmetries.

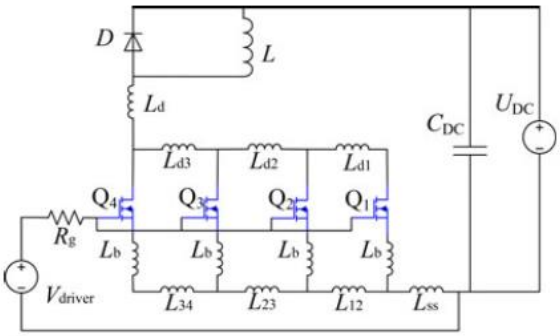


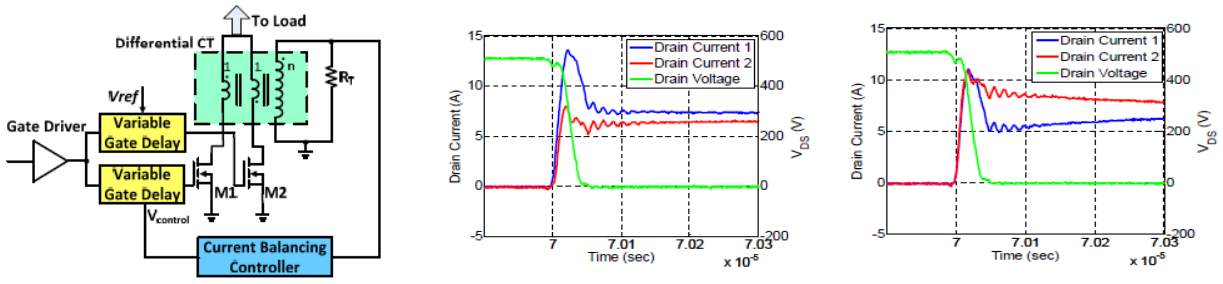
Fig. 11. DPT schematic for a proposed passive current compensation method

The first passive approach demonstrates the raw benefit of SiC to paralleling power MOSFETs. With fast switching capability, the time in which external factors have to effect dynamic current balance is reduced which ultimately limits the thermal difference experienced between devices compared to the much larger switching times of Si devices. The second approach requires detailed characterization of every devices V_{th} and then appropriately sizing external inductance to compensate. Both of these methods though only use two parallel devices and downstream effects are not presented. Finally, the last authors are able to mitigate effects of parasitic inductances added by asymmetries in a specific module but V_{th} is left unaddressed.

2.1.3.2 Active current imbalance mitigation schemes

An active transient gate control scheme for two parallel IGBTs is developed in [20]. By using a kelvin sense resistor to obtain dynamic current, gate resistance at one switch is reduced during the switching transient to compensate for the lowest current switch. Though the feedback and actuation are relatively simple the method is demonstrated with IGBTs with switching times of a few microseconds. A similar transient gate control for SiC MOSFETs with switching times approaching 10 ns is not feasible.

An active current balancing (ACB) scheme for 20A SiC MOSFETs is developed in [21]. Using a differential current transformer at the drains of the two devices, the gate drive is delayed accordingly. The current sensing is shown to be sufficient for very high *di/dt* of SiC MOSFETs. Switching energy imbalance is successfully demonstrated but system level effects are not expanded upon.



(a) Proposed ACB (b) Turn-on without ACB (c) Turn-on with ACB

Fig. 12. ACB schematic and experimental results

A high bandwidth, PCB based Rogowski coil current sensor is presented in [25]. The bandwidth is proven up to 100 MHz which is sufficient for SiC and provides a promising solution to the two device limitation of a differential transformer. Board space requirement for the sensor is significant though especially for multiple devices. A serious comparison of the effects of this added board space vs the benefits would take very detailed modeling.

From the above, transient gate control of any form would be very difficult with the very fast switching times of SiC. Differential current transformers can utilize high-bandwidth analog feedback but the method is needs further work to extend to more than two devices. Finally, there are high-bandwidth, board-level current sensing solutions but

they cause extra layout space leading to increased parasitics. Overall the objective is balancing power loss between devices which includes both switching and conduction loss. Focusing on dynamic current does not account for this.

2.2 CONSEQUENCES OF FAST SLEW RATES

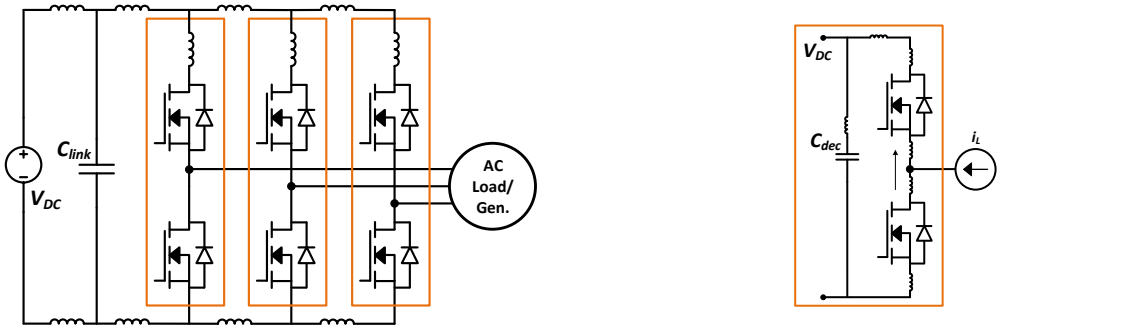
Issues already faced with fast switching single SiC MOSFETs compound when aiming at maintaining performance in parallel operation. Cross-talk which induces gate voltage through the Miller capacitance of off state devices potentially leading to shoot-through current and additional losses becomes more complex to mitigate in a parallel environment. Voltage overshoot is also a challenge with SiC in general due to high di/dt during switching transients. Just one additional device in parallel doubles this di/dt during switching transients that can lead to much larger overshoot voltages, not even accounting for the additional layout area and parasitic inductance that are hard to avoid.

2.2.1 Decoupling Capacitance Method

Some amount of parasitic inductance is inevitable in any circuit due to inherent inductance of copper. With the extremely high *di/dt* implicit of fast switching SiC MOSFETs voltage transients can occur with even small amount of inductance. An illustration of parasitic inductances caused by device packaging, circuit layout, and interconnects in a VSC is shown in Fig. 13(a).

Voltage transients in VSC caused by fast switching devices lead to conducted EMI and overvoltage on the device [26-28]. By placing a decoupling capacitor across the DC-link, as close as possible to each phase leg as shown in Fig. 13(b), these high *di/dt* switching events are decoupled from the larger interconnect inductances. The parasitic

inductances in this loop from device packaging, layout, and capacitor stray inductance are commonly referred to as loop inductance (L_D).



(a) VSC with associated parasitic inductances (b) Phase leg with decoupling capacitor

Fig. 13. Parasitic inductances inherent in VSC

Worst case overvoltage for the low side device occurs when load is flowing into the midpoint of the phase-leg and the lower switch is the active switch. When the active switch turns off, current must commutate from it to the upper diode. This di/dt is introduced into the drain loop as which also contains the output capacitance (C_{OSS}) of the now closed low side device. A small signal equivalent model of this circuit is shown in Fig. 14. The turn-off of the low side device is used as the stimulus and L_{dec} is added as the parasitic V_{DC} connection inductance.

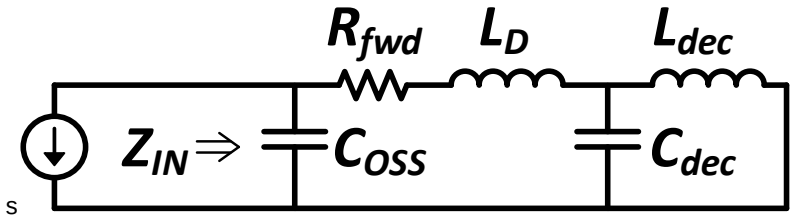


Fig. 14. Small signal equivalent circuit of power loop

Voltage overshoot on the device—which also generates EMI—comes from the *di/dt* of the switching event exciting an *LC* resonant circuit. Loop inductance should always be minimized as best as possible but is limited by packaging, capacitor parasitics, and other layout challenges. Shown in [29], the power loop is decoupled when Z_{IN} is composed mainly from the L_D/C_{OSS} loop. That is,

$$\left| j\omega_R L_{dec} // \frac{1}{j\omega_R C_{dec}} \right| \ll |j\omega_R L_{DS}|. \tag{6}$$

Where ω_R is the inner resonant frequency. Then by setting C_{dec} as a function of C_{OSS} and L_{dec} as a function of L_D, Z_{IN} merges with the impedance of the L_D/C_{OSS} loop when C_{dec} is just 50-200 times C_{OSS}—assuming L_{dec} is more than 2 times L_D. Therefore, C_{dec} severely reduces overshoot on the device—and associated EMI—when 50-100 times larger than C_{OSS} but has very minimum benefit when any larger. Similar conclusions were reached in [26] and [28] from a time domain approach.

2.2.2 Parasitic Inductances

Parasitic inductance outside of the power stage are possible to mitigate with proper sizing of a decoupling capacitor. The fast switching of SiC though creates issues with even the small inductances within this decoupled power loop. The parasitic inductances within a phase leg are characterized into three equivalent inductances: gate loop inductance (L_G), common source inductance (L_{CS}), and power loop inductance (L_D), shown in Fig. 15. L_{CS} was grouped with L_D in the previous section for simplification.

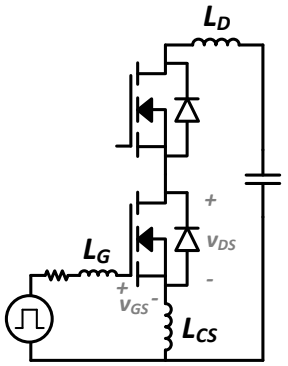


Fig. 15. Major parasitics in phase leg

The circuit level effects of each of these parasitic elements have been well studied [5, 6]. L_D as discussed before is responsible for overshoot voltage across the device which also creates higher switching losses. L_G has not been found to cause significant problems but will add ringing on the gate voltage and potentially increase turn-on delay if significant. L_{CS} has the most significant effect on performance. During switching transients when di/dt is high, L_{CS} creates a voltage feedback to gate drive. That is, during turn-on the di/dt is positive, creating a voltage source which lowers the actual gate to source voltage.

2.2.3 Cross-talk

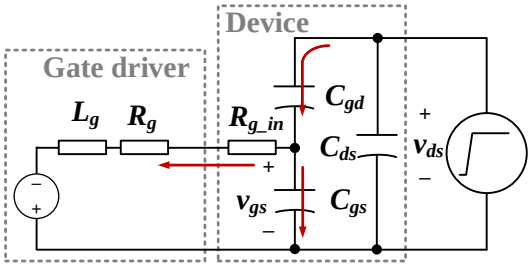
Cross-talk in a phase leg is ultimately when the switching action of one device induces gate voltage on the opposite—off-state—device. When load current is negative—flowing into the switch node—the lower switch is hard switching while the upper switch acts as a synchronous switch. Thus, the switch node voltage is dependent on the switching of the lower device. The opposite condition occurs when load current is

positive—flowing out of the switch node—but the effects are the exact same. Therefore, only the case with negative current needs to be introduced.

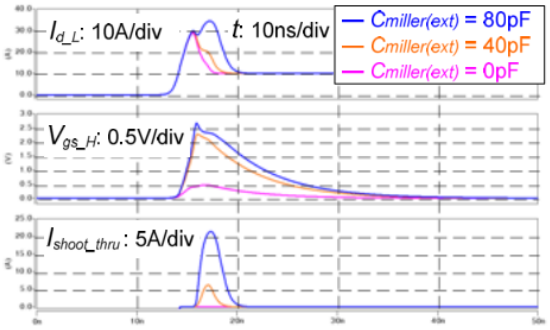
Let the upper switch acting as the synchronous switch in a hard switching phase leg be off. When the active (lower) switch turns on this will lower the switch node to ground and therefore induce a positive dv/dt across the synchronous switch. This *dv/dt* is seen by the gate to drain (C_{gd}) capacitance of the device which induces current into the gate of the device. This current through internal and external gate resistance creates voltage across the gate to source of the device. If this voltage exceeds the threshold voltage (V_{th}) of the device the channel turns on. This cross-turn-on is illustrated in Fig. 16(a) and has two adverse effects. First, the synchronous switch that should be off now conducts extra current under high drain to source voltage, this is commonly referred to as shoot through current—that is when both devices are on. Second, this current has to flow through the active switch adding to it's switching losses. These mechanisms are shown schematically in Fig. 16(a) and the effects in Fig. 16(b). This added loss and stress to each switch ultimately reduces reliability and efficiency.

The mechanism of cross-talk when the active switch turns off is similar but the effect is different. Again, the synchronous switch is ideally completely off while the active switch turns off which brings the switch node high. This means that the synchronous switch experiences a high negative *dv/dt*. This forces current flow away from the gate of the device which creates a negative gate to source bias. This is shown schematically in Fig. 16(c) with example waveforms in Fig. 16(d). If the gate voltage is

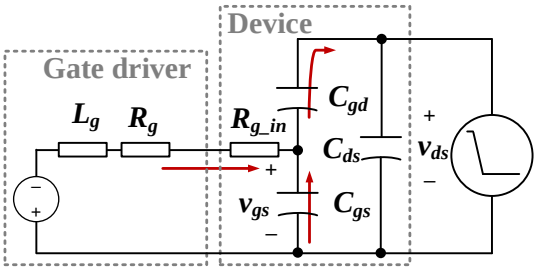
brought below the manufacture's recommended minimum v_{GS} failure or at least accelerated aging of the of the device can occur.



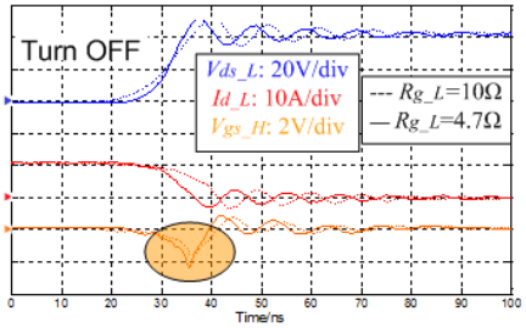
(a) Mechanisms causing cross-talk



(b) Effects of cross-talk [30]



(c) Mechanisms causing cross-talk



(d) Effects of cross-talk [30]

Fig. 16. Turn-off transient of lower switch

The reduction in reliability and efficiency makes cross-talk a critical problem to address with SiC MOSFETs. Much research has been produced to understand this phenomenon with discrete devices through characterizing the most important factors. The following equation can be derived from the circuit in Fig. 16(a):

$$\Delta v_{gs} = R_g C_{gd} \frac{dv_{ds}}{dt}\left(1 - e^{\frac{-t}{R_g C_{ISS}}}\right) \tag{7}$$

where $C_{ISS}=C_{gd}+C_{gs}$. With this equations a few relationships are drawn analytically. First, it is clear that the magnitude of induced gate voltage is directly proportional to C_{gd}. Second, the magnitude of the induced gate voltage is also directly proportional to both R_g and dv_{ds}/dt. Third, a maximum induced gate voltage occurs when t equals the rise time. Furthermore, [31] points out that di_d/dt also induces unintended gate voltage. The mechanism for this L_{cs} as follows

$$\Delta v_{gs} = L_{cs}\frac{di_d}{dt} + \left(L_g - L_{cs}\right)\frac{di_g}{dt}. \tag{8}$$

Simulation and experimental work has been conducted to verify and quantify the impact of contributing elements to cross-talk [31, 32]. The major contributing parasitic elements to cross-talk are summarized below along with the effect of each:

Table 1. Effects of parasitic elements on cross-talk

Parasitic Element	*Rg*	*Cgs*	*Cgd*	*Ld*	*Ls*	*Lg*	*Temp*
Effect	+	-	+	-	+	+	+

2.2.3.1 Mitigation

The simplest way to mitigate cross-talk is to decrease dv/dt the device sees. This can be accomplished two ways. First, the by increasing R_g of the active switch the turn-on time and therefore *dv/dt* across the synchronous switch will be decreased. Second, adding capacitance to the gate of the active switch has the same effect. Neither of these are practical for high performance VSC because switching loss and minimum dead-time will increase.

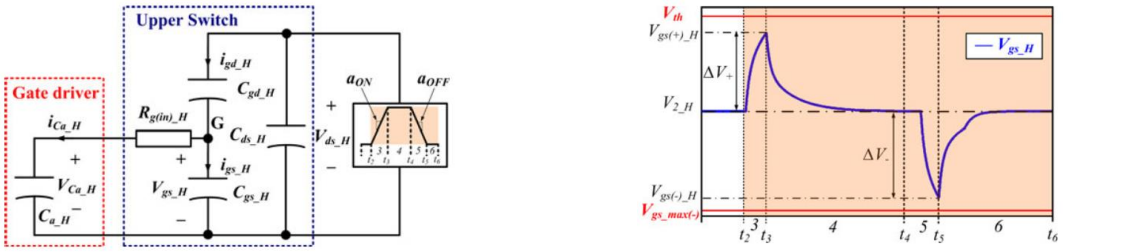
Asymmetric gate drive is a viable solution for a phase-leg used in a synchronous buck configuration [33]. That is simply using a schottky diode to bypass the gate resistance of the active switch during turn-off. This allows longer turn-on time without increasing turn-off time. With SiC FETs though this could cause current slew rates that the $L_{CS}di/dt$ effect actually create a larger induced gate voltage [31].

Another straightforward way to mitigate cross-talk is to simply provide a lower—negative—off-state gate voltage. Bipolar gate drives work well and are practical with Silicon devices for mitigating cross-talk. By using a negative off-state voltage, the peak of the induced voltage remains well below threshold voltage. This has been found to be insufficient for SiC [34]. SiC MOSFETs have much stricter negative gate voltage bias limits and typically lower threshold voltages.

Miller clamps provide an active means of mitigating induced gate voltage and are commercially available in IGBT gate drive chips [35, 36]. By using a small semiconductor switch to short the power devices gate during the off state, there is a much lower impedance for the Cdv/dt current to induce gate voltage. This technology has been shown experimentally to reduce cross-talk in SiC FET phase-legs [37, 38].

A limitation of the Miller clamp is the high internal gate resistance typical of SiC FETs and the lack of consideration for negative gate voltage and L_{CS} effects. To increase the effectiveness of the Miller clamp, a large capacitance can be added in series to the clamp to provide low impedance of the gate drive for both positive and negative induced current with consideration for L_{CS} [39]. Induced gate voltage using an auxiliary capacitor (C_a) is derived using the equivalent circuit in Fig. 17.

$$\Delta v_{gs} = \frac{C_{gd} V_{DC}}{C_a + C_{ISS}} + \frac{{C_{gd}}^2 R_{g(in)} (dv/dt)}{(C_a + C_{ISS})^2} \left(1 - e^{\frac{-(C_a + C_{ISS}) V_{DC}}{C_a (dv/dt) R_{g(in)} C_{ISS}}}\right) \quad (9)$$



(a) Simplified equivalent circuit of synchronous switch during switching of active switch

(b) Effect of induced gate current on synchronous gate voltage

Fig. 17. Equivalent circuit for gate impedance regulation design

2.2.3.2 Parallel considerations

While the effects and mitigation at the device level are well understood, few references exist for cross-talk with parallel devices. Work that has been done focuses on understanding cross-talk that exists within commercial modules and the route causes. Four modules were modeled and simulated in [40] to study the cross-talk that actually occurs within modules but gate voltage is not possible to measure experimentally due to packaging constraints. It was found that even though external waveforms appear normal, cross-talk induced cross turn-on occurs in all examined modules except for one which had inherently longer switching times and losses.

The main challenge with parallel dies is that the parasitic gate loop and power loop inductances are inherently larger. Authors in [41], found based on simulations that cross-talk induced current spikes simulated with and without packaging inductances differed by nearly 12 times. Furthermore, “the switching energy and cross-turn-on

current of the module increase with the number of paralleled dice regardless of different input voltages, gate resistances, and switching currents". Finally, only a significant turn-on gate resistance and negative drive voltage was found to be sufficient in reducing cross-talk induced current in SiC MOSFET modules[42]. This is far from ideal considering the associated switching loss increases

2.3 STABILITY

2.3.1 Short Circuit Behavior

Short-circuit situations are problematic for both devices and the system. There are generally considered to be three short-circuit cases for power devices [43]. Type I occurs when the power device turns on causing a short circuit. Type II occurs when the power device is conducting and a short occurs elsewhere. In the phase-leg configuration this typically occurs due to the opposite switch turning on. Finally, a type III occurs when the freewheeling diode is conducting and the load is shorted. This last type is not a concern with SiC phase legs. In either a type I or II, device current increases rapidly before gradually decreasing due to self heating and eventually leveling off as shown in Fig. 18. A type I fault is the worst case scenario for a device because it experiences this high short-circuit current under the full DC voltage.

During a short-circuit event there are four main regions where devices fail—as shown in Fig. 18. A power limit failure (a) occurs due to peak current limitation but have yet to be reported with SiC MOSFETs. After current begins to self limit due to heat from excessive current, the high die temperature causes the device to break down. This energy limit failure (b) is the most common in power devices. Then during turn-off of the

short-circuit current inhomogeneous operation from chips themselves or supporting circuitry can cause gate oscillation in multi-chip modules. This has been referred to as inhomogeneous operation failure (c) though the actual failure comes from gate oxide break down due to oscillation in gate voltage. Finally, thermal runaway (d) occurs after the device is turned off. After turn-off the temperature within the device is high enough for high temperature generated leakage current to cause thermal runaway failure.

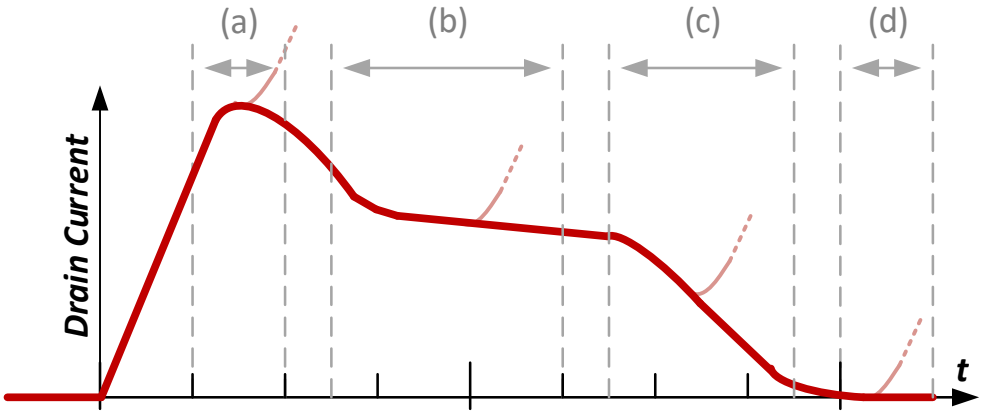
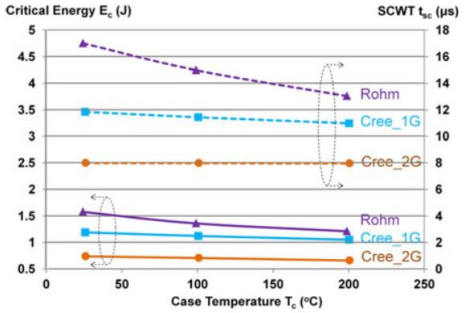


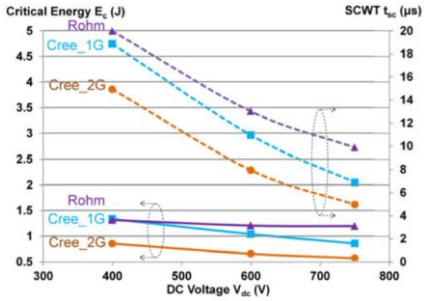
Fig. 18. Short-circuit current waveform and failure modes for both IGBTs and MOSFETs

Protection circuitry within the gate drive needs to detect and turn off short circuit current in enough time to prevent failure modes two and four. Therefore it is important to understand the allowable time in order to design protection properly. Fig. 19 shows critical energy (E_c) and short-circuit withstand time (SCWT) are a function of (a) temperature and (b) V_{DC} [44].

Similar results follow at the module level. Safe operating areas for two 1.2 kV modules are shown in Fig. 21(a), one rated at 180A and another at 300A [45]. Similar results were found for a 1.2 kV / 180 A module in [46] with the SOA shown in Fig. 21(b).

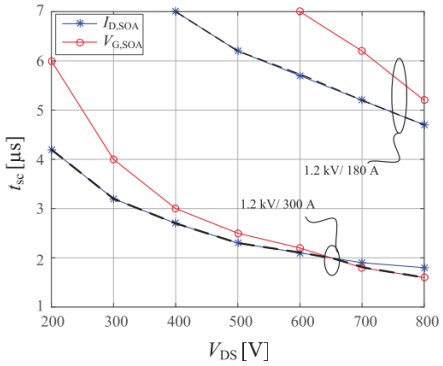


(a) Temperature dependency

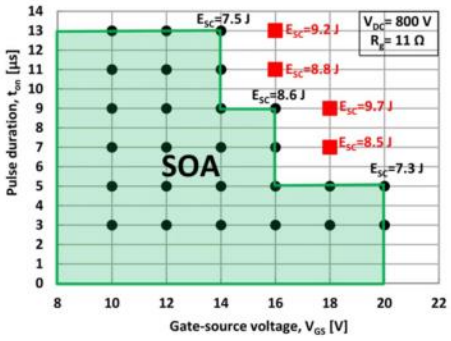


(b) DC bus voltage dependency

Fig. 19. SOA of discrete devices



(a) SCWT as a function of V_{DC}



(b) SCWT as a function of gate voltage

Fig. 20. SCWT for 1.2 kV modules

2.3.1.1 Detection Schemes

With a 1.7kV, 500A and claimed 14.5nH of loop inductance including decoupling capacitance achieved a total turn-off of 7.3 kA at a bus voltage of 1.1 kV in just 2.6 us using desat protection [47]. An improved desat protection scheme is proposed in [48] and a delay time of just 600ns is achieved. Desat utilizing a Schmitt-trigger was tested on two discrete devices and one 100A module—all rated at 1.2 kV—and achieved delay times under 300 ns for all cases [49].

2.3.2 Gate Oscillations with Parallel Devices

2.3.2.1 Turn-on Oscillation during Normal Switching

Paralleling MOSFETs creates an *LC* circuit through connection of gate terminals as shown in Fig. 21. Many manufactures have addressed this issue with silicon devices. Individual gate resistors [12, 50] as well as ferrite beads at each gate [11, 51] have been proposed to mitigate the issue. These are general recommendations though and a detailed, useful model does not exist.

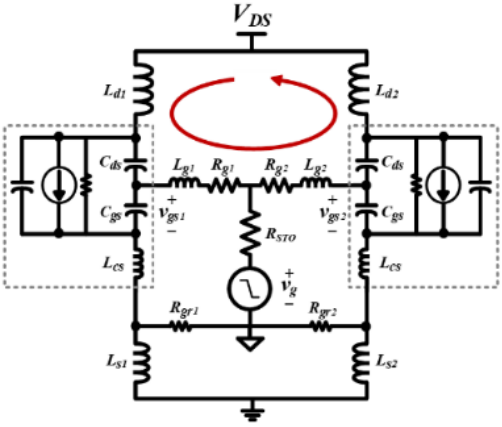


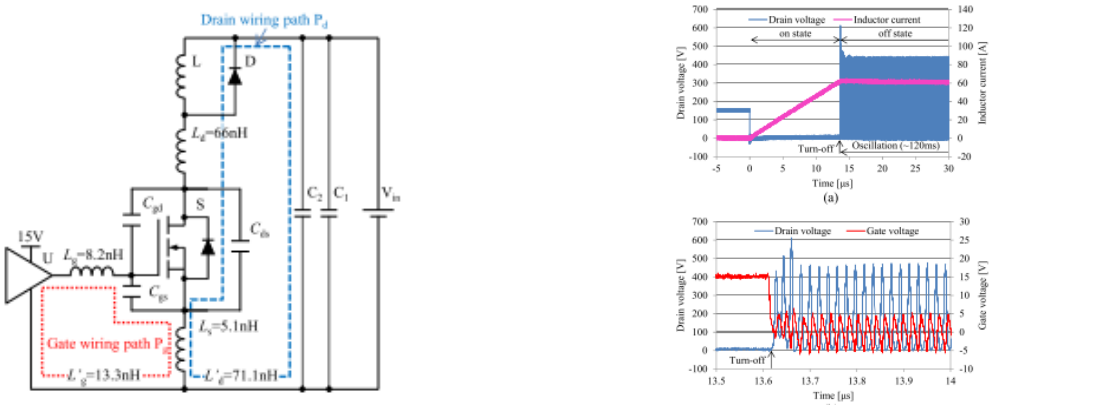
Fig. 21. LC loop created by paralleling MOSFETs

2.3.2.2 Oscillation During Short-circuit

The same *LC* loop as above has also been shown to cause gate and drain current oscillation in multi-die IGBT modules [13]. In severe cases this ultimately causes destruction of the devices. No concrete understanding of the underlying mechanism is yet agreed upon with both transconductance [52] and a negative gate phenomena [53] presented as possibilities. Though it is clearly dependent on collector-emitter voltage and the associated decrease in C_{GC} [14].

2.3.2.3 Self-Turn-On

Both SiC and GaN suffer from oscillatory false triggering. Stability due to the coupling off parasitic elements in high di/dt and dv/dt environments. Oscillatory false triggering of SiC MOSFETs caused by parasitics have been seen with just a single device [7, 8, 54]. Oscillation in gate and drain voltages as well as drain current occurs—Fig. 22 [8]—if parasitic inductances are not well controlled.



(a) Power stage and gate drive loops

(b) Sustained oscillatory false triggering in SiC MOSFETs

Fig. 22. Sustained oscillatory false triggering in SiC MOSFETs during normal turn-off

2.4 MODULE SOLUTIONS

Modules have become widely excepted as a means for higher current applications. With dies paralleled internally they are much easier from the designers perspective and treated as a single, high current device. For this reason it is worth also reviewing what SiC modules are available for such applications as a benchmark. The one commercially available 1.7 kV SiC MOSFET module as well as two from literature are shown in Table 2.

Table 2. Commercially available SiC MOSFET modules

Voltage	Rating	Manufacturer	Part Number	Dies	1200V / 200A	1000V / 200A	800V / 200A	
1700	8 mΩ	CREE	CAS300M17BM2	6	24 mJ		16 mJ (900V)	[55]
1700	3.4 mΩ	GE	Non-commercial	12	-	11 mJ	-	[47]
1700	5 mΩ	CREE	X12 next-gen Non-commercial	4	22 mJ		13 mJ	[56]

2.5 SUMMARY

This section presented the existing work on paralleling discrete SiC MOSFETs as well as single device or module level work that is important to consider in design. First, work addressing current distributing in parallel devices was reviewed. Next, various considerations for using SiC devices with fast switching was presented which includes power stage considerations, the effects of parasitic inductances, and cross-talk. Finally, existing work concerning stability and short-circuit protection was reviewed. The next section seeks to build on this work for a robust, high current phase leg for VSCs through paralleling of discrete SiC MOSFETs.

3 SiC MOSFET Characterization and Effects on Parallel Operation

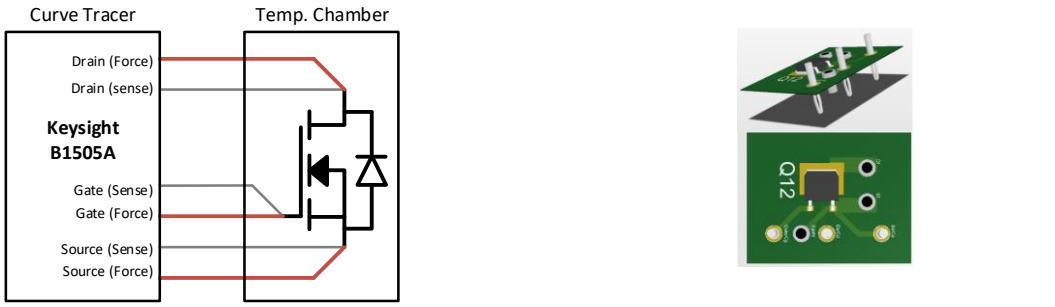
This chapter analyzes the main issues that lead to power imbalance between parallel MOSFETs. Building on the literature review the focus is on the characteristics of the devices themselves and the physical layout considerations. First, a lot of SiC MOSFETs are characterized to establish actual variation in datasheet parameters between devices of the same model. Then simulation and analysis is done to establish sensitivity to different mechanisms and establish priorities for design. Lastly, the sensitivity analysis is utilized to create a physical design which is evaluated with finite element analysis (FEA).

3.1 Characterization

Understanding characteristics of power devices are crucial for gate drive design. Key characteristics are included on the manufacture's provided data sheet but are not always sufficient for robust design. Detailed information over temperature and a number of test positions aid in design. Static characteristics include performance parameters like capacitances, on-state resistance, transfer function, etc.

As identified in literature, variation in device parameters play a significant role in parallel operation and performance. In this section the SiC MOSFET under consideration is characterized across temperature and discrepancies between different devices are analyzed. A curve tracer is a piece of test equipment that can precisely control and measure both voltage and current. This allows for the various V-I curves which characterized power devices to be measured. The Keysight B1505A machine

used is rated for over 3 kW which is important for power devices that can handle very high pulsed power. An oven with over 200°C capability is also utilized. The curve tracer setup is shown in Fig. 23. A force wire and sense wire are used at each connection to the device. These are continued all the way to the device pins using a PCB in order to minimize any measurement discrepancies between different devices. These Kelvin connections are vital considering many of the tests require over 100A so a small resistance will cause inaccurate voltage readings. This is especially vital when seeking accurate measurement of parameters like on-state resistance which is as low as 30mΩ.

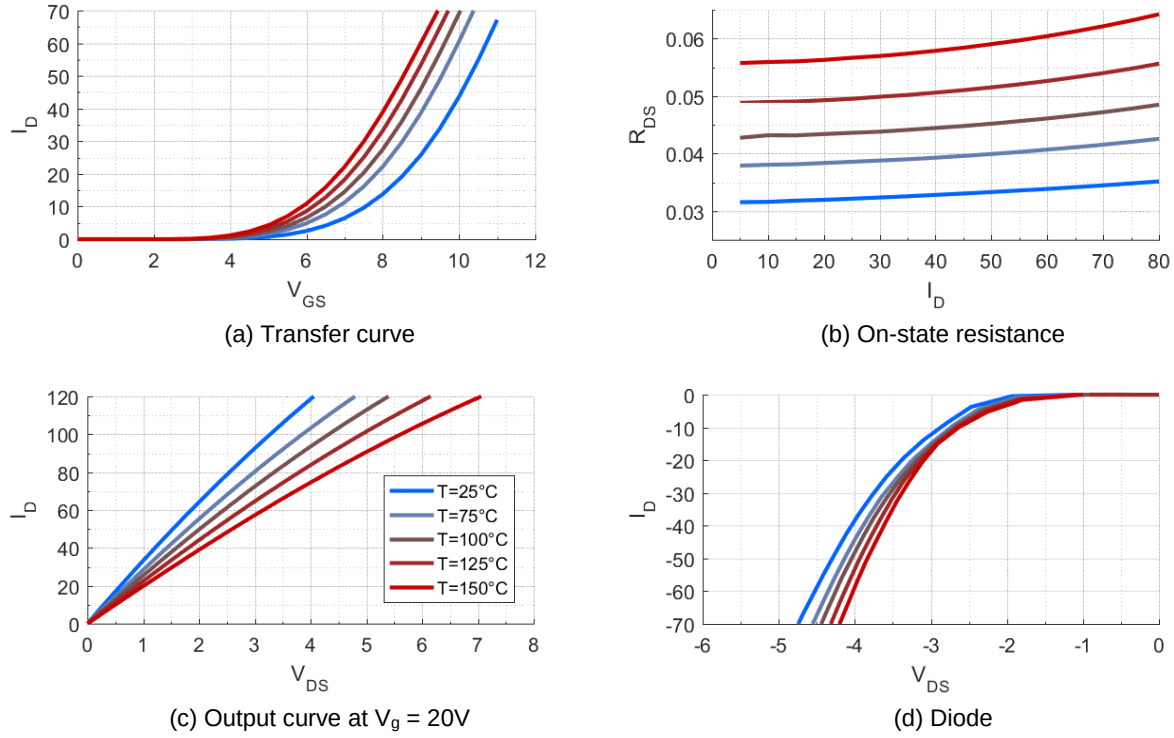


(a) Curve tracer setup (b) Kelvin connection testing platform

Fig. 23. Static characterization setup

With this setup key static characteristics are measured from 25°C to 150°C. Fig. 24 shows how these trend over temperature. The temperature trends are consistent with typical SiC results. In the transfer curve the threshold voltage decreases with temperature while the transconductance remains nearly constant. On-state resistance has the opposite effect in that it nearly doubles at 150°C compared to its room temperature value. It follows then that the output curve becomes less steep with

temperature. Finally, the voltage drop increases slightly across the body diode as device temperature increases.



(a) Transfer curve

(b) On-state resistance

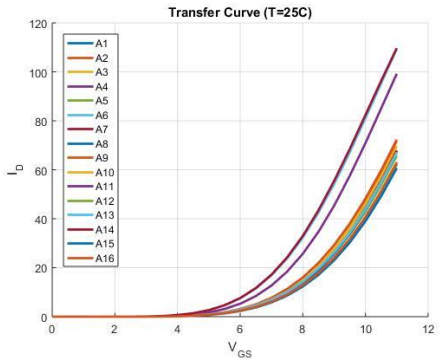
(c) Output curve at V_g = 20V

(d) Diode

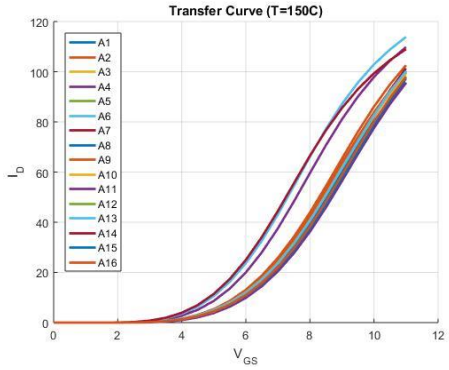
Fig. 24. Static parameters across temperature

These curves across temperature are measured for a lot of 16 devices. The two key figures for parallel current sharing—transfer curve and on-state resistance—are shown in Fig. 25. Looking first at the room temperature transfer curves there are clearly three outliers while the rest are not equal but are well grouped. This trend remains relatively consistent over temperature meaning that the change in V_{th} and g_{fs} over temperature is consistent between devices. Next, the on-state resistance has a spread of roughly 4mΩ across all currents at room temperature. This is consistent and slightly

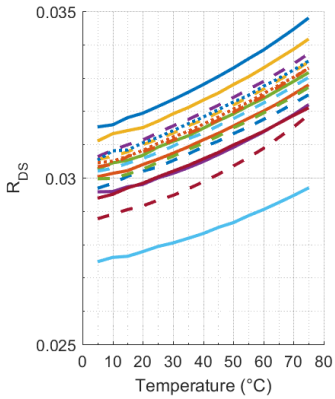
better than the 30mΩ typical value at 25°C with 25mΩ-35mΩ range given by the data sheet.



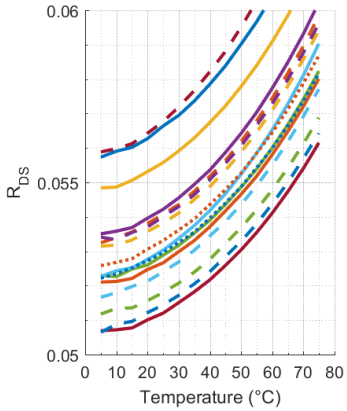
(a) Transfer curve of 16 devices at 25°C



(b) Transfer curve of 16 devices at 150°C



(c) R_{DS} of 16 devices at 25°C



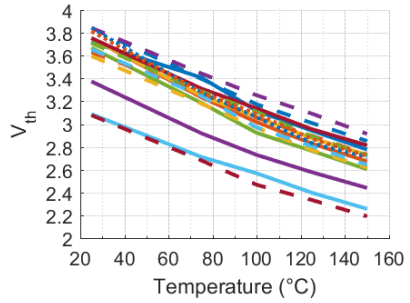
(d) R_{DS} of 16 devices at 150°C

Fig. 25. V_{th} and R_{DS} of multiple devices at minimum and maximum of temperature range

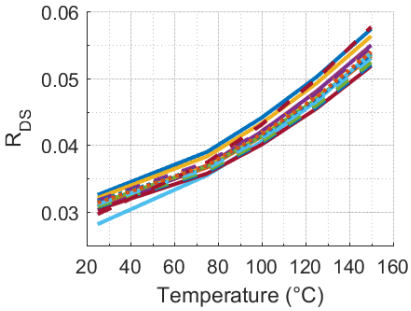
One important take aspect is that threshold voltage has a negative temperature coefficient (NTC) while on-state resistance has a positive temperature coefficient (PTC). These temperature trends are plotted in Fig. 26(a) and (b) for every device. This makes thermal runaway due to V_{th} possible with parallel devices. It has been shown that a device with the lowest V_{th} experiences the greatest switching loss which could

theoretically lead to an even lower V_{th} and even greater share of losses. Though possible, this type of runaway has yet to be reported. Adversely, the PTC of the $R_{DS(ON)}$ is potentially beneficial for parallel power sharing. That is, as a device heats up it's resistance increases which would naturally limit current in relatively hot devices.

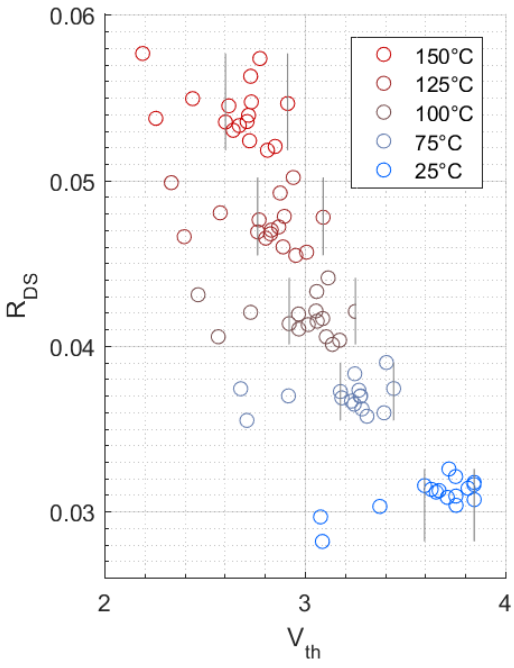
Additionally, there is no correlation between relative V_{th} and relative $R_{DS(ON)}$ within the sample. The two values are plotted together across temperature in Fig. 26(c). Additionally, there are clearly outliers with regards to V_{th} that occur across all temperatures. To numerically distinguish outliers the Thompson Tau Test is utilized due to nonuniform distribution. The bounds of this test are also plotted at each temperature in Fig. 26(c).



(a) V_{th} measured at 100mV



(b) R_{DS} at 35A



(c) Relationship between R_{DS} and V_{th}

Fig. 26. On-state resistance and threshold voltage relationships

3.2 Simulation and Understanding of Key Parameters

The focus in this section will be on current distribution between devices during switching transients—dynamic current sharing. As identified in the literature review, the two major contributors to dynamic current imbalance are the threshold voltage of the devices themselves (V_{th}) and the common source inductance (L_{CS}). There are other contributing factors though that are important to understand in order to prioritize design. There are three main categories of mechanisms leading to current imbalance which are illustrated in Fig. 27. These include the device characteristics, parasitics in the power loop, and gate drive characteristics.

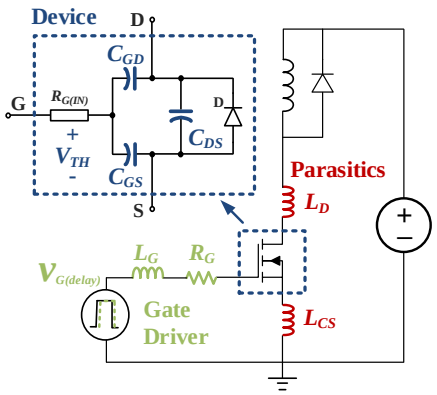


Fig. 27. Key parameters effecting current balance in parallel devices

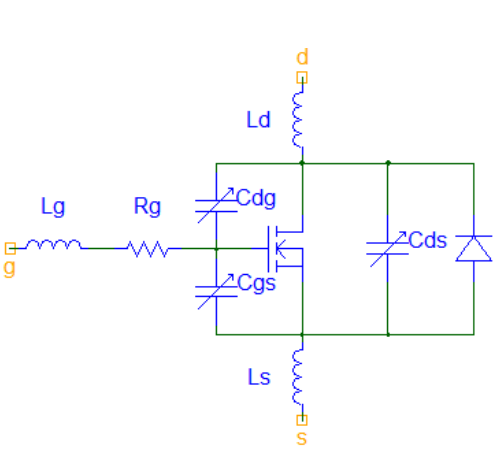
Using the physical device characterization results a simulation model is built in order to further understand the effects of each identified parameter. An accurate model of the physical devices is modelled using SaberRD's Power MOSFET tool. The equivalent model used in the software is shown in Fig. 28(a). The model is created from the following physical data discussed earlier: I_d-V_{ds}, I_d-V_{gs}, R_{ds}, I_d, *body diode I-V*, and

capacitances. This model is extended across temperature using the measured characteristics from 25°C to 150°C. Additionally, this allows for devices which exhibited significantly different characteristics to be modeled.

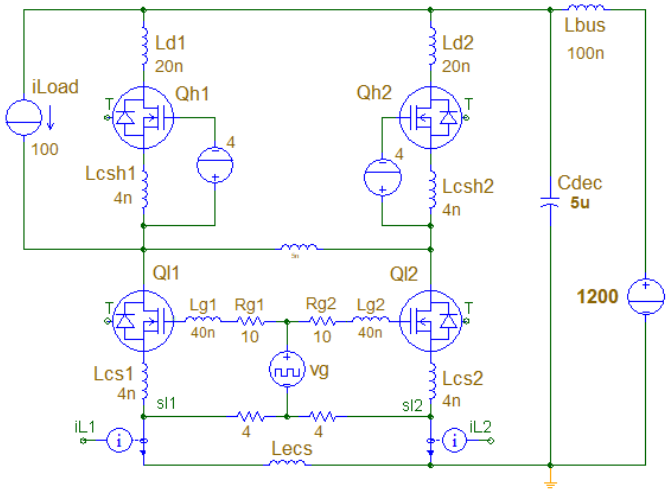
In design with a large number of parameters, optimization requires knowing the impacts of each in order to make proper trade offs. With this device model a phase leg consisting of two devices per switch—Fig 28(a)—is created to perform a sensitivity analysis. The simulation setup is shown in Fig. 28(b) with most of the parameters under evaluation and their base values shown. The parameters evaluated include threshold voltage (V_{th}), common source inductance (L_{cs}), equivalent common source inductance (L_{ecs}), power loop inductance (L_d), gate loop inductance (L_g), and gate signal delay ($t_{(delay)}$). L_{ecs} is separate from L_{cs} because it is not included in the gate loop but produces a similar effect through ground bounce because the high power stage current flowing through it. For testing $t_{(delay)}$ or jitter from a commercial buffer circuit in Fig. 28(b) is slightly modified to use two buffers. The actual effects of variation in the parameters under study on dynamic current are shown in Fig. 29. Drain to source voltage of each device remains relatively similar so it doesn't aid understanding to display. In general, variation in a parameter causes more dynamic current to be carried by one of the devices, ultimately leading to temperature imbalance from unequal switching loss (E_{SW}).

First, V_{th} of the two devices is varied and the device with the lowest V_{th} begins the turn-on transition first and carries more current. Similarly, at the turn-off transition, the device with the lowest V_{th} carries more current because but this time because it begins the turn-off transition last. The effect of variation in L_{cs} is similar at turn-on. During the

switching transient, di_d/dt through the inductance creates a negative feedback voltage to the gate-source voltage seen at the device terminals. The current imbalance does not begin until current starts to flow. As seen in Fig. 29(c) that means that the device with the lowest inductance carries the most switching current and therefore generates the most loss. The di_D/dt through the common source inductance is opposite polarity at turn-off though leading to a positive voltage feedback to the actual v_{gs} at the terminals. This means that the device with the lowest inductance still switches first but this time handles the smallest amount of current and therefore generates less loss. In summary, relatively low V_{th} or L_{cs} have the same effect on turn-on transient current but the opposite effect on turn-off transient current. This has a mild cancelation effect concerning loss for L_{cs} while a compounding effect for V_{th}. The effects of $t_{(delay)}$ and L_{ecs} are shown and follow similar reasoning.



(a) Equivalent circuit produced by SaberRD's Power MOSFET Tool

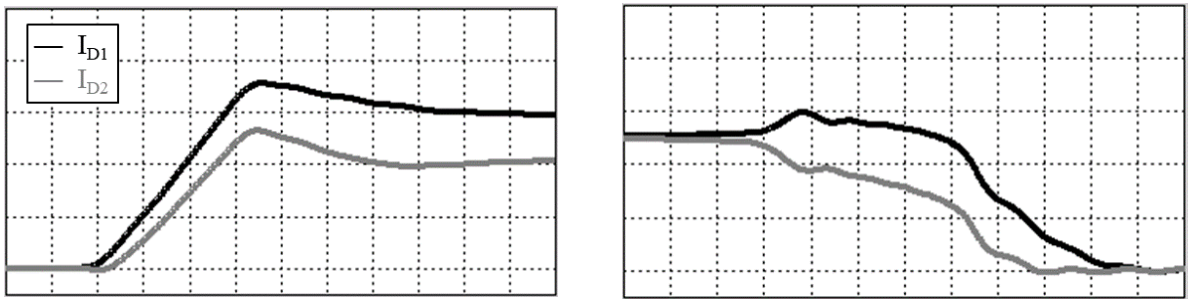


(b) Sensitivity analysis simulation circuit

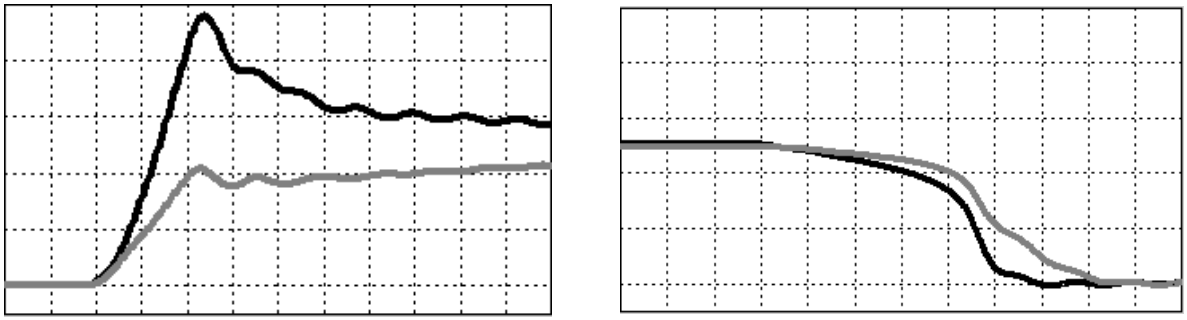
Fig. 28. Device modeling and simulation setup

With the underlying understanding of the current distribution issues caused by the various parameters is important to quantify each in order to properly utilize in design optimization. A sensitivity analysis is performed to quantify effects on dynamic current imbalance at turn-on and turn-off as well as the effects these have on switching loss by sweeping the parameters around a base case. The sensitivity is measured based on difference as a percentage of total. For example, the difference in switching loss between the two devices is divided by the total switching losses of the two combined. The sensitivity analysis for all parameters under study is shown in Fig. 30. For V_{th} the datasheet typical value is used as the baseline and the range listed on the data sheet swept. The compounding effect of turn-off loss (E_{off}) and turn-on loss (E_{on}) is evident. From the previous characterization, actual variation in V_{th} is not as severe as worst case datasheet values used in the sensitivity analysis. Thus, actual ΔE_{SW} from V_{th} will be 18%. By setting aside the <20% of devices that are outliers, this ΔE_{SW} can be reduced to just 5%. Binning of less than 20% of devices provides significant improvement.

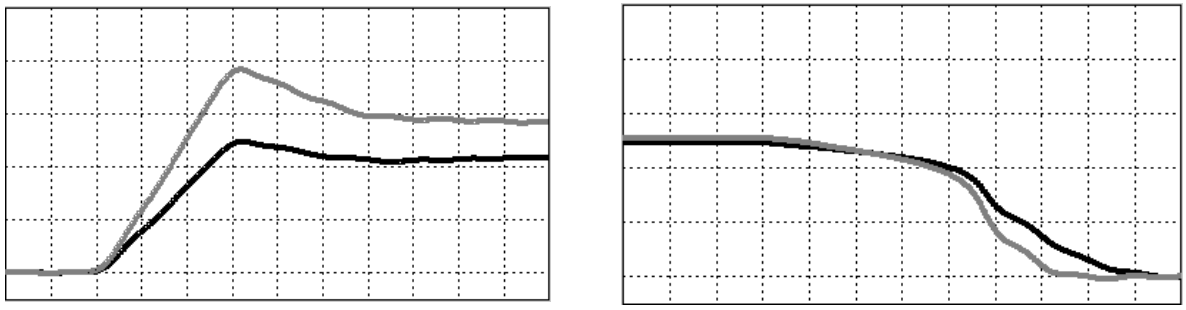
In contrast to the effects of V_{th}, E_{off} and E_{on} are in opposition for L_{cs} variation. L_{ecs} also has this counteracting effect since it is similar to L_{cs} but is less significant in magnitude. The effect of delay time ($t_{(delay)}$) or jitter if utilizing individual device buffers also has the same overall effect on current sharing and loss distribution. Lastly, both L_g and L_d are relatively insignificant. Of all the parameters available for optimization of parallel device utilization, these two parameters leave the most margin for tweaking. With V_{th} relatively mitigated, in the next section these design understandings are utilized in physical layout of the power devices to mitigate L_{CS} issues.



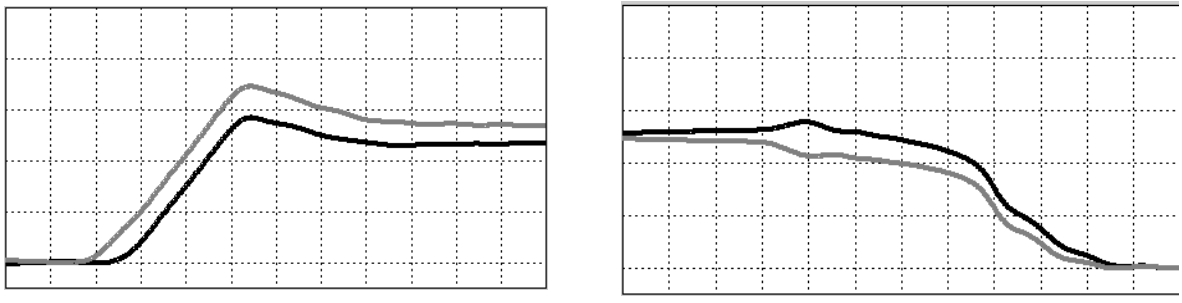
(a) $V_{th}(1) < V_{th}(2)$



(b) $L_{CS}(1) < L_{cs}(2)$

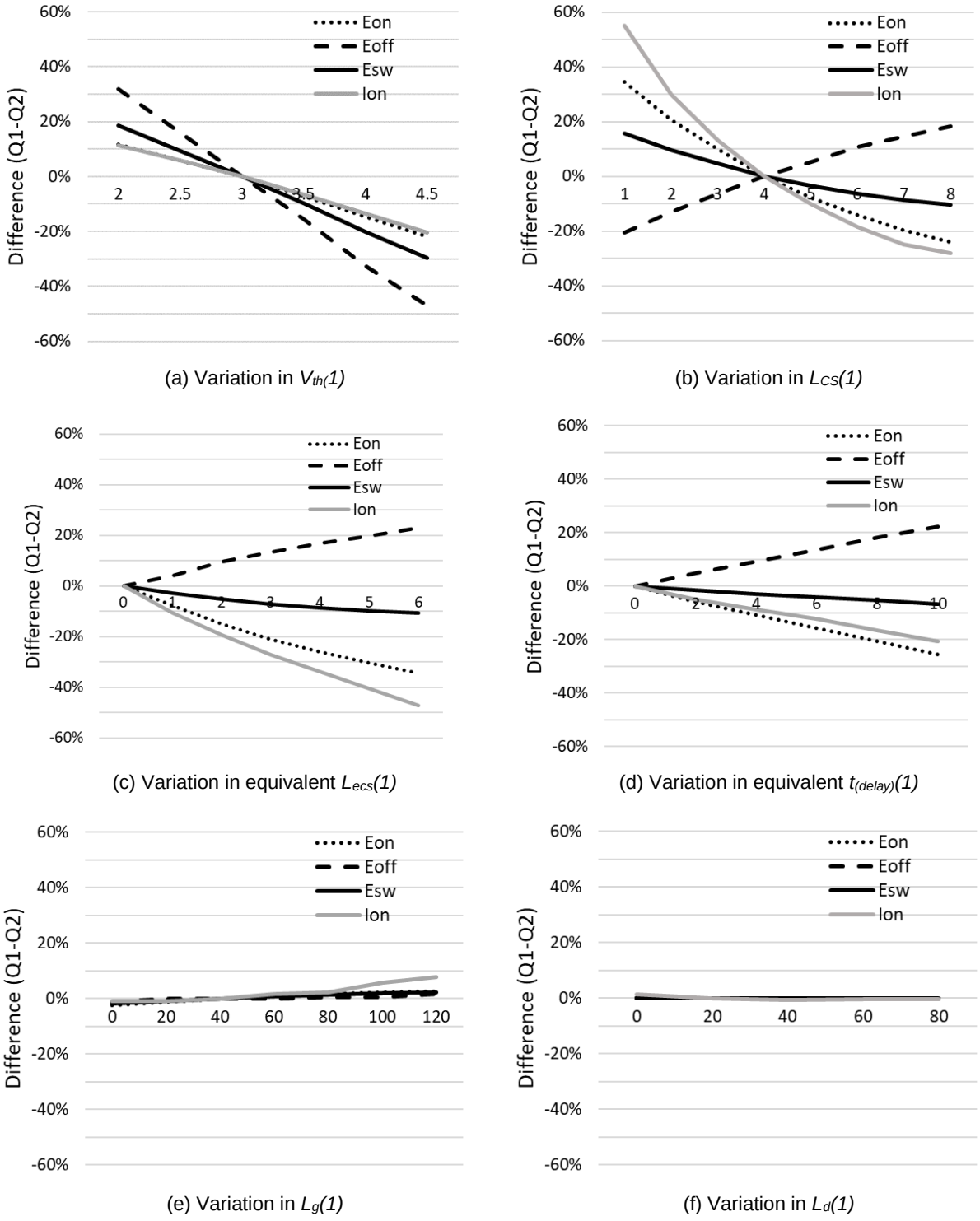


(c) $L_{ecs}(1) = 3$ nH



(d) $t_{(delay)}(1) = 6$ ns

Fig. 29. Dynamic current sharing between two devices with varying parameters (left) turn-on (right) turn-off



(a) Variation in $V_{th}(1)$

(b) Variation in $L_{CS}(1)$

(c) Variation in equivalent $L_{ecs}(1)$

(d) Variation in equivalent $t_{(delay)}(1)$

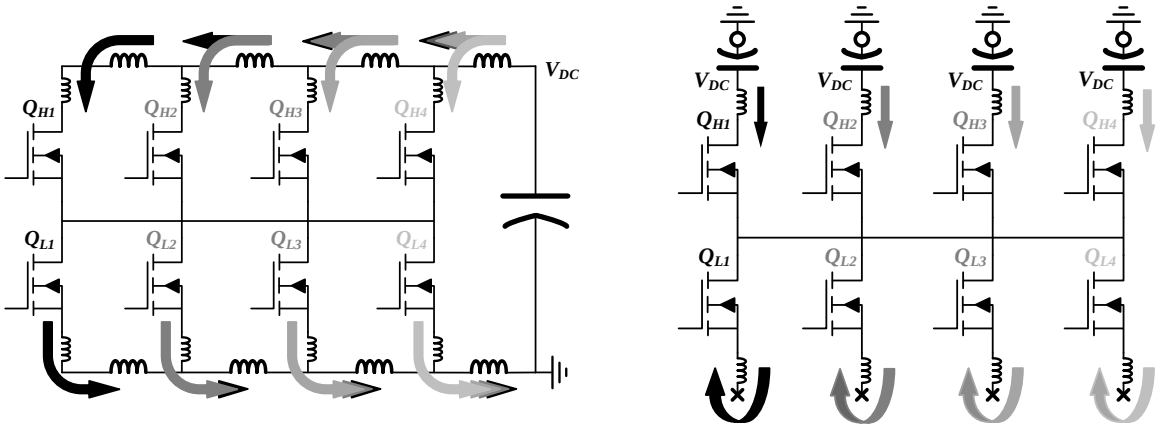
(e) Variation in $L_g(1)$

(f) Variation in $L_d(1)$

Fig. 30. Sensitivity of current imbalance and switching loss to key parameters

3.3 MITIGATION OF LAYOUT INDUCED IMBALANCE

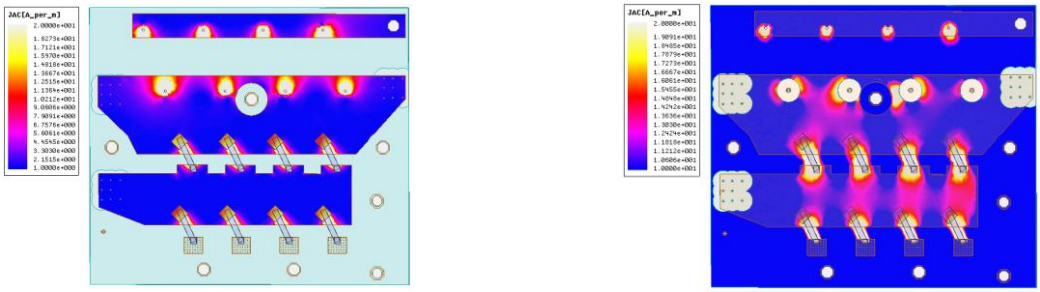
As shown in literature, the way in which devices are physically laid out plays a critical role in overall performance. With SiC MOSFETs *di/dt*'s well over 1 A/ns are achievable which means that even a small amount of inductance can create major issues. From the sensitivity analysis it is clear that the focus of laying out parallel SiC MOSFETs should be on matching common source inductance between devices, then minimizing L_{ecs} as much as possible, and finally minimizing the remaining inductances. With single chips simple Kelvin connection of the gate driver to the device can minimize L_{CS}. With parallel devices though, any current return path at the source become equivalent common source inductance. This is illustrated in Fig. 31(a) with the ideal situation shown in (b). Even with Kelvin connections at each source terminal ground bounce can occur that is worst at the device closest to the decoupling capacitance or true ground. This is an issue with both discrete and module level paralleling.



(a) Typical module (b) Discrete symmetric layout

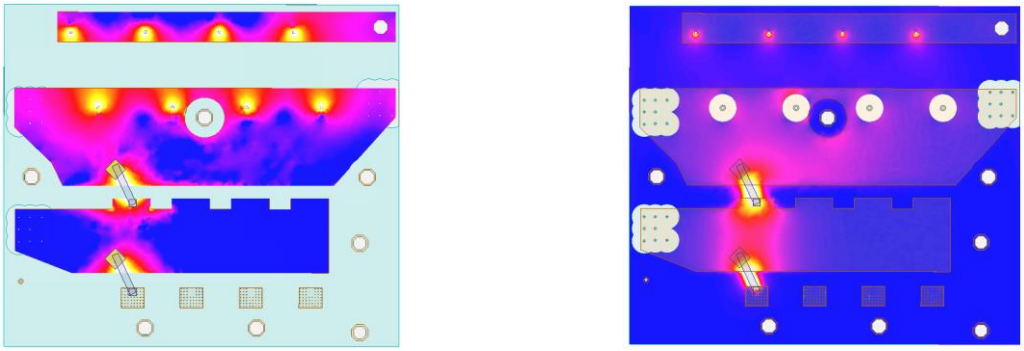
Fig. 31. Current flow

A vertical layout approach like what has been demonstrated for GaN devices offers a good approach to minimizing and matching parasitic inductances [57]. Essentially, by providing a current return path directly underneath the devices the effective inductance cancels out due to magnetic field cancellation. This can be seen in the finite element analysis (FEA) of the proposed physical design is shown in Fig. 32. The top layer of the board as well as the ground return layer are shown with a current density heatmap. The current in the ground plane flows directly underneath the current path on the top layer. With this configuration, an overall inductance from the decoupling capacitor terminals is found to be just 3.9 nH and is verified experimentally with an impedance analyzer. Again, the first objective with parallel devices is to match L_{CS}. In order to ensure this, the FEA software is also used to find the effective per device inductance. These results are shown in Fig. 33 for both the top layer and ground return layer for each position on the board. The parasitic inductance of each position is roughly *7 nH* with a maximum variation of just *0.13 nH*. This is vital for minimizing overshoot and dynamic current balance. Similar simulations can be done for through hole device layouts. These add complexity but reasonable results are achievable.

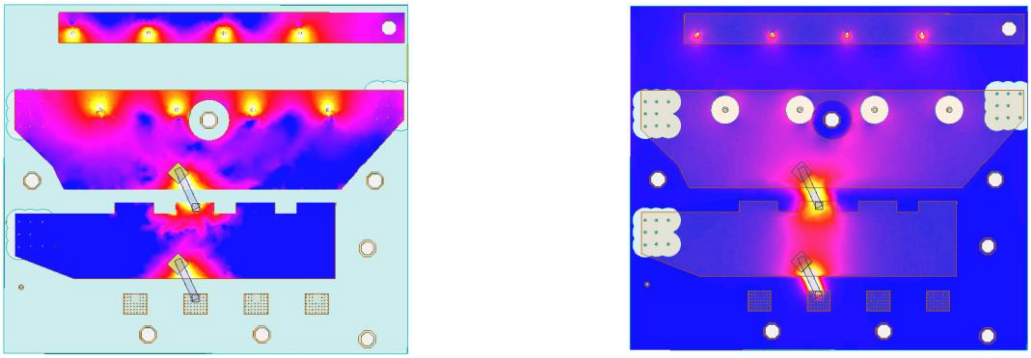


(a) Top board layer (b) Bottom layer (ground plane)

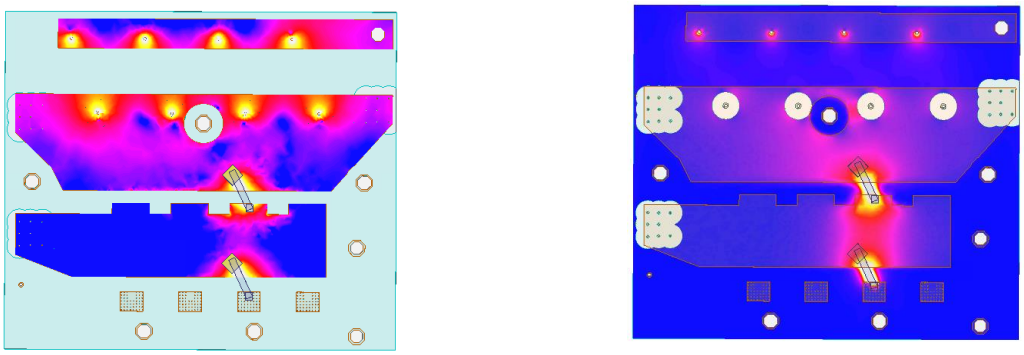
Fig. 32. Current distribution with 4 parallel dies



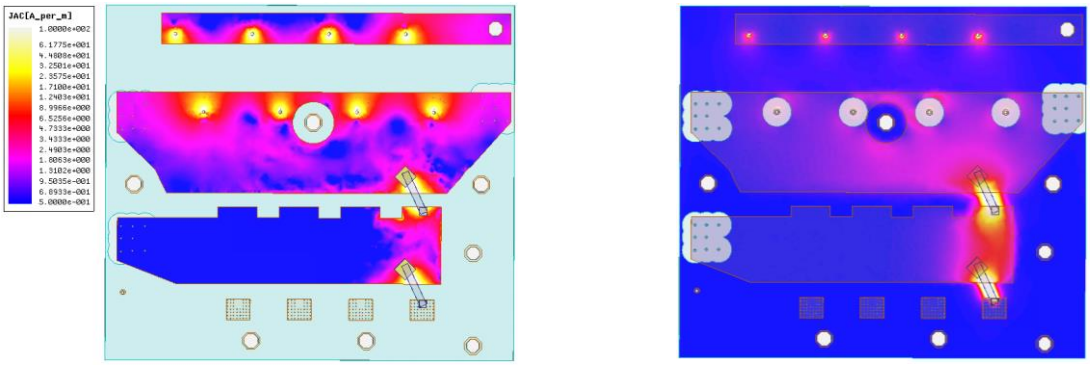
(a) Position 1 top (left) and bottom (right) current distribution with 6.93 nH



(b) Position 2 top (left) and bottom (right) current distribution with 6.96 nH



(c) Position 3 top (left) and bottom (right) current distribution with 6.91 nH



(d) Position 4 top (left) and bottom (right) current distribution with 7.04 nH

Fig. 33. Current distribution in IMS board per phase leg

3.4 SIMULATION RESULTS

The device model from physical characterization and FEA simulation of the physical power stage can be combined to validate the design and provide additional insight. The FEA software Q3d features a spice exporter for circuit simulation. This spice file contains an equivalent *RL* network with proper coupling parameters which allow simulation of the high frequency parasitic *RL* components which are critical to the parallel performance of MOSFETs

The two major considerations for dynamic current balancing are now able to be modeled—physical layout and actual device characteristic deviation. The SaberRD implementation of this is shown in Fig. 34. The importance of this model is to first validate that no additional issues for current sharing are added by physical design. Second, additional insight can be derived to understand key considerations for the gate driver design for high performance of parallel MOSFETS.

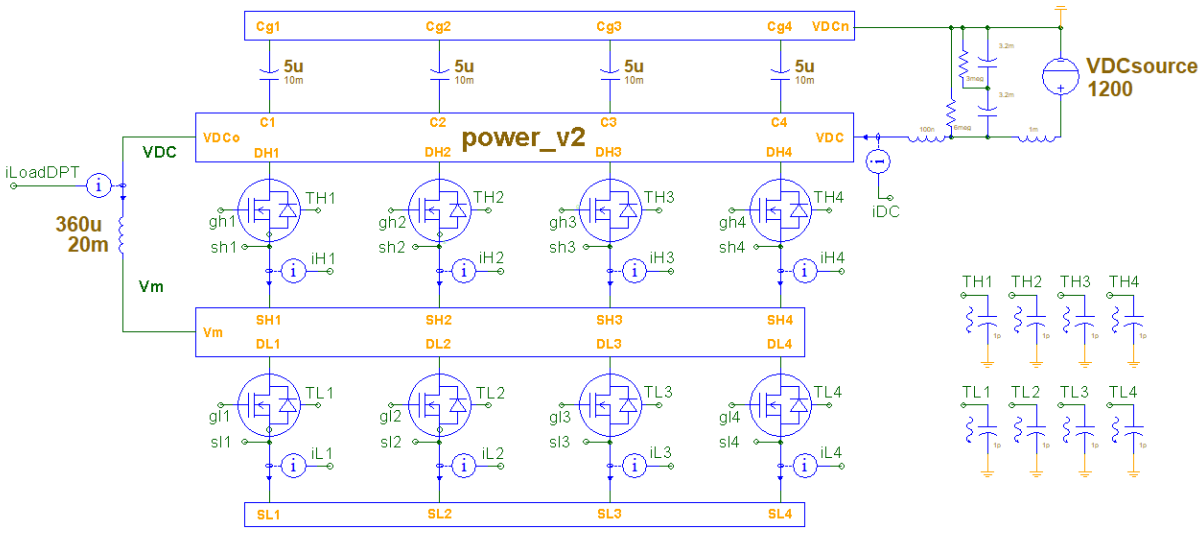
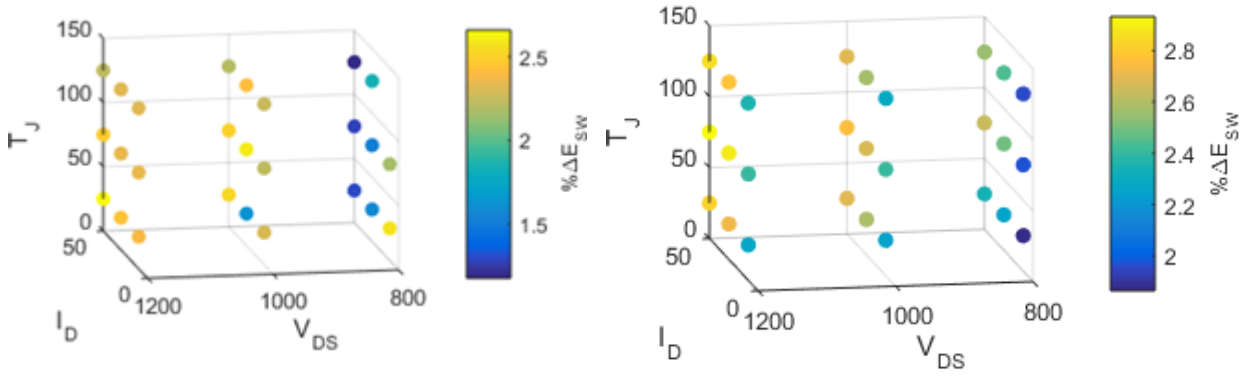


Fig. 34. Saber simulation with parasitic parameters from Q3d

First, the physical simulation model is used to validate the design objective of mitigating layout effects of dynamic current sharing. To do so the same MOSFET part number is used for all eight devices in the Fig. 34 schematic. This ensures that any dynamic current issues observed come from the layout and not discrepancies between devices. Simulating a DPT, various currents, drain voltages, and temperatures are swept. The maximum difference in switching loss as a percentage of the overall switching loss is plotted in Fig. 35. Drain current is for an individual device—overall output current is *4X* what is shown. Across a full spectrum of operating conditions the effect of the physical layout on switching energy distribution is under 3% of total switching energy. One of the two major causes of switching energy imbalance can be effectively mitigated with proper attention to physical design.



(a) R_g = 5 (b) R_g = 25

Fig. 35. Percent difference in switching energy loss caused by physical layout

Using the same simulation setup, the other important considerations for gate drive design previously discussed—cross-talk and slew-rates—are analyzed in the parallel environment. Fig 36. shows how severe of an issue cross-talk can be with 1.7 kV SiC

MOSFETs. The induced gate voltage can easily exceed +/- 10V on all the devices in parallel. This is enough to cause additional current to flow during switching transients and cause reliability issues exceeding negative gate voltage ratings of the devices. Cross-talk mitigation will be a design focus in Chapter 5.

3.5 SUMMARY

The two major concerns for current distribution discovered in literature—the devices themselves and supporting circuitry—as well as additional parameters critical for gate driver design have been studied with 1.7 kV SiC MOSFETs. Physical characterization is performed in order to establish discrepancies amongst the devices themselves. Simple binning of outlier devices based on V_{th} reduces ΔE_{SW} from this parameter to just 5%. Device models are developed and used for sensitivity analysis of all parameters relevant to design. Many of which have been well documented for design with a single SiC device but not as well for multiple in parallel. These design considerations are then utilized for layout of the parallel devices and FEA performed to validate the approach with L_{CS} contributing at most 3% to ΔE_{SW}.

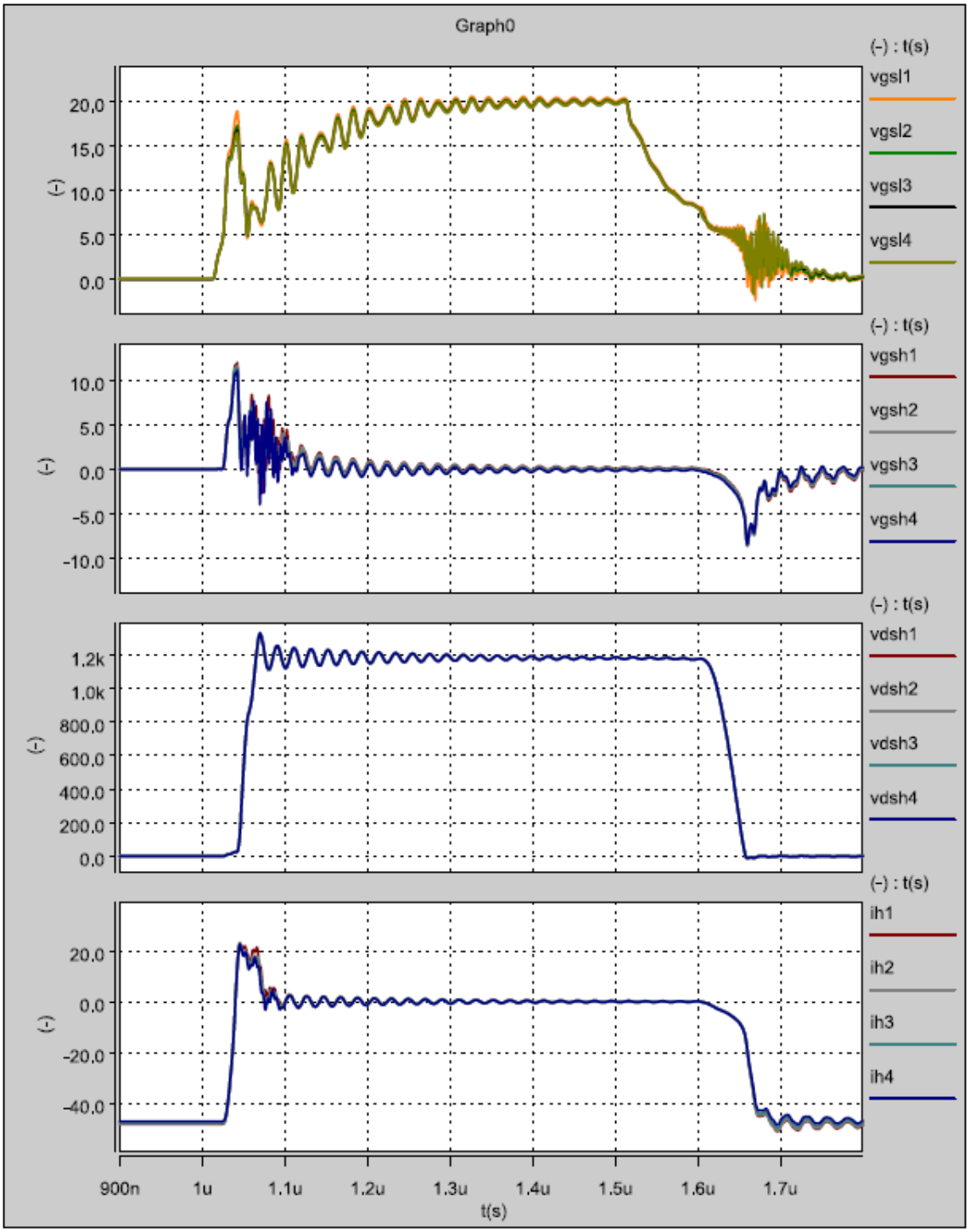
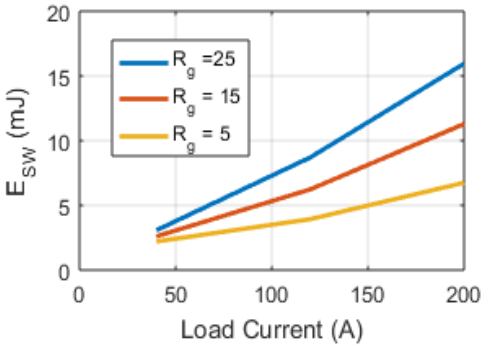
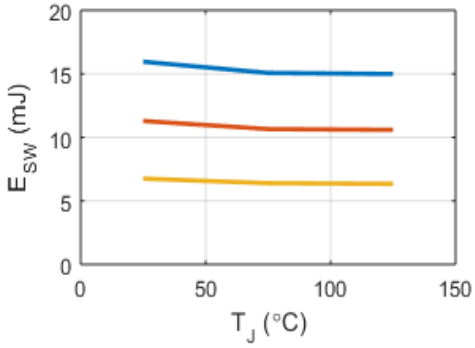


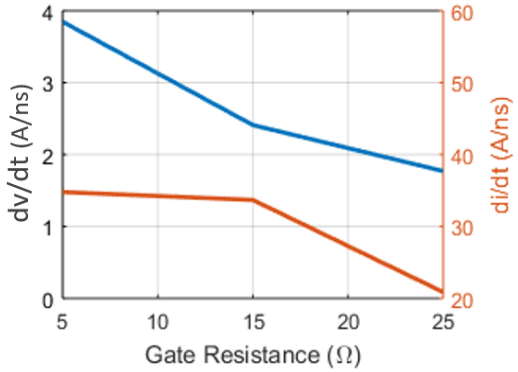
Fig. 36. Cross-talk occurrence with parallel SiC MOSFETs



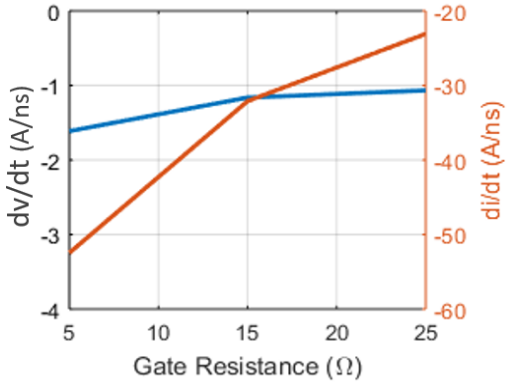
(a) Switching loss vs load current at 1200V



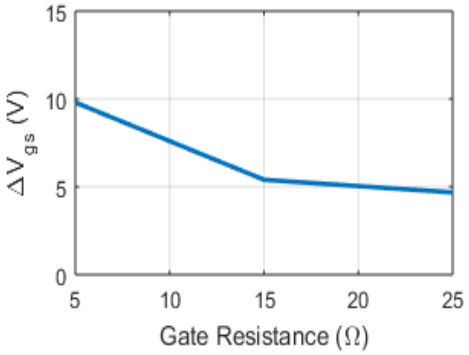
(b) Switching loss vs temperature at 1200V / 50A



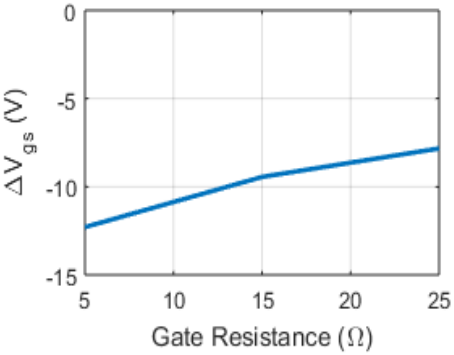
(c) Slew rates across off-device during turn-on of opposite



(d) Slew rates across off-device during turn-off of opposite



(e) Induced v_{gs} of off-device during turn-on of opposite



(f) Induced v_{gs} of off-device during turn-off of opposite

Fig. 37. Key switching characteristics

4 PROTECTION OF HIGH CURRENT SIC MOSFETS

Short-circuit survivability is even more critical of a threat to reliability than the longer term effects of current imbalance. It is especially a concern with the much larger short-circuit current that occurs with SiC MOSFETs relative to older technologies. This section presents the challenges with short-circuit protection of parallel SiC MOSFETs. Building on the literature review, a minimum protection time is set as the benchmark for design. Protection circuitry is designed, tested, and proven with a single device. Then considerations that need to be made for using devices in parallel are addressed before testing short-circuit protection with four parallel SiC MOSFETs.

4.1 DESATURATION AND SOFT TURN-OFF DESIGN

Desaturation detection is one of the most common short-circuit detection schemes utilized with high power Si power devices. The fundamental operation is to sense the devices drain current as a function of V_{DS}—illustrated by the devices output curve. An operational schematic is shown in Fig. 38.

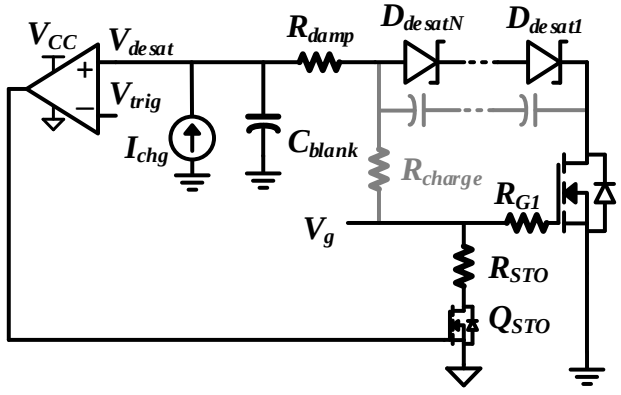


Fig. 38. Desaturation protection circuitry

Overall, the diodes must have equivalent blocking capability to the power device. Utilizing a current source at the desat node, the desat voltage—V_{desat}—then reflects the drain current minus the voltage drop across the diodes. That is,

$$V_{desat} = V_{DS} + N \cdot V_{fwd}. \tag{10}$$

During conduction periods of the power device, V_{ds} will raise with drain current which is reflected by V_{desat}. This voltage is compared with a threshold—V_{trig}—in order to identify unsafe current. When the comparator goes high a switch is enabled to bring the device gate low. This is in series with a soft turn-off resistor that turns off the large short circuit current in a larger time frame than much smaller current during normal operation. A blanking capacitor is needed to suppress noise and false triggering from transients. This makes the rise time of V_{desat} to V_{trig} during a fault condition

$$t_{blank} = \frac{C_{blank} \times V_{trig}}{I_{charge}}. \tag{11}$$

This time plus the time delay caused by the analog circuitry is the total response time of the protection circuit

$$t_{desat} = t_{blank} + t_{IC}. \tag{12}$$

Typical response times are not acceptable with SiC devices due to the much shorter short circuit withstand time. Another issue with using this scheme with SiC devices—especially higher voltage devices—is *dv/dt* noise sensitivity. With possible dv/dt's of 100 V/ns, significant current can be induces across the diodes' junction

capacitances which charges C_{blank}. This switching transient noise current is derived along with the induced voltage onto the desat pin it causes.

$$I_{induced} = nC_{Diode}\frac{dv_{DS}}{dt} \tag{13}$$

$$\Delta v_{desat} = n\frac{C_{Diode}}{C_{Diode}}V_{DS} \tag{14}$$

By significantly increasing the charging current, the blanking time can be reduced to an acceptable level. This also allows a larger C_{blank} which improves noise immunity. The new blanking time can now be approximated by

$$t_{blank} \approx R_{charge}C_{blank}\ln\frac{V_{CC}}{V_{CC}-V_{trig}}. \tag{15}$$

This approach is verified experimentally first with just a single SiC MOSFET. A HSF at a bus voltage of 1200 V is shown in Fig. 39. The blanking time is 600 ns and the analog delay an additional 150 ns for an overall response time of 750 ns which meets the 1 us benchmark.

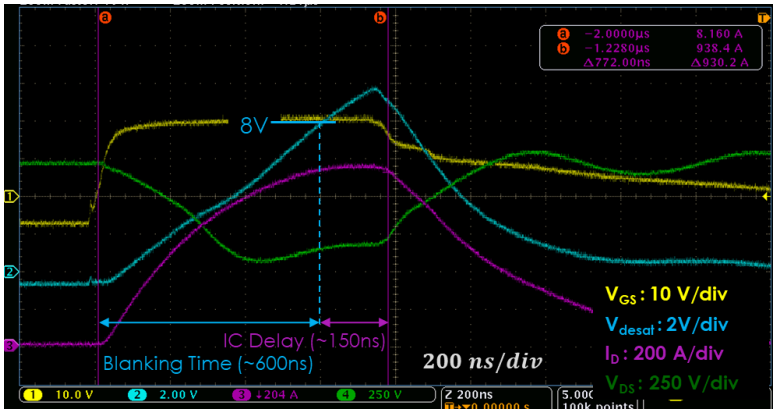
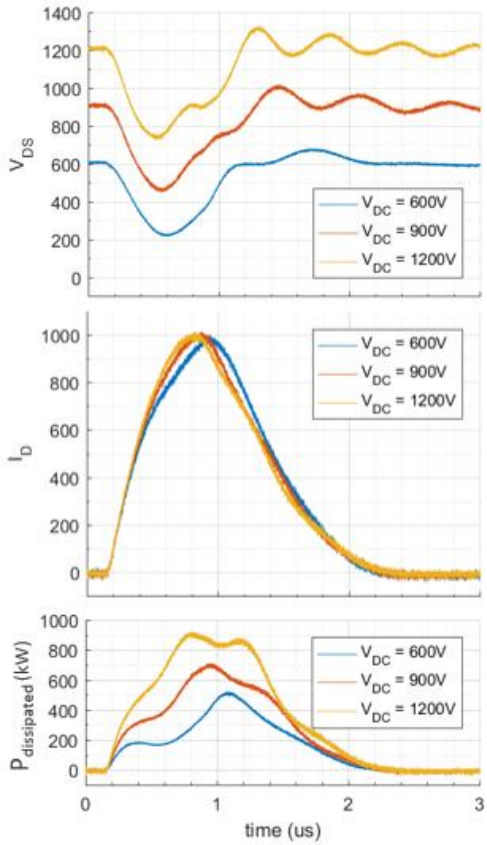


Fig. 39. Hard switching fault detection and turn off with single MOSFET

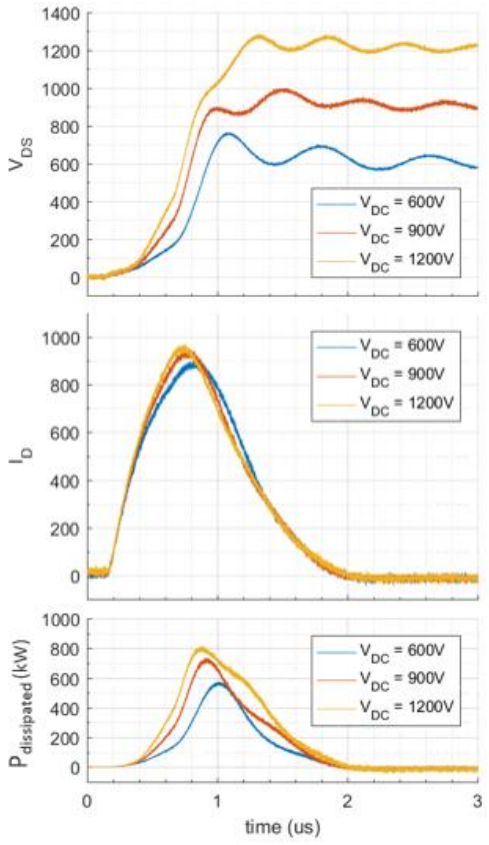
4.2 SHORT CIRCUIT CHARACTERIZATION

More short-circuit test samples are collected with a single device to understand behavior of both the device and protection before paralleling additional devices. This is a very practical design step because it has been shown that similarly rated devices—even from the same manufacturer—can exhibit different characteristics during short circuits [58]. Both HSFs and FULs are analyzed under various bus voltages. These are shown in Fig. 40 with the associated dissipated energy also shown.

The total energy from these short circuit tests at maximum desired operating voltage are calculated in Table 3. Due to experiencing the short-circuit current under initial presence of high blocking voltage, the HSF is the worst case fault. Also depicted in Fig. 41 is the dissipated power with a stable bus voltage under a HSF. This represents the absolute worst case situation, that is no voltage drop across V_{DS} during the short circuit event. The mechanisms behind the V_{DS} drop will be detailed next.



(a) Hard Switching Fault



(b) Fault Under Load

Fig. 40. Short-circuit waveforms with different bus voltages

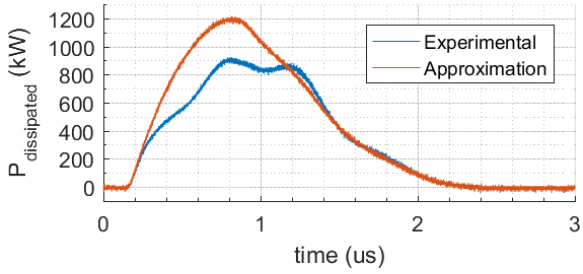


Fig. 41. Short-circuit energy worst case approximation using strict voltage bus

Table 3. Dissipated energy during short-circuit

	600V	900V	1200V
FUL	0.33 J	0.45 J	0.58 J
HSF	0.45 J	0.72 J	1.00 J
Worst Case			1.21 J

4.3 OVERVOLTAGE CONSIDERATIONS

The function of the decoupling capacitor is to provide transient energy. During normal switching transients, it was found that C_{dec} *>100X* C_{OSS} is sufficient to decouple the switching loop in effect limiting overvoltage to the value caused by transient current and the loop inductance (L_D). The transient energy required for this is equal to the switching loss, which is typically in the mJ range for this class of SiC MOSFETs. During short-circuit events though this energy can be in the range of joules—that is *1000X* normal conditions. Fig. 42(a) shows the equivalent circuit for the cause of V_{ds} overshoot during normal transients. Again, with C_{dec} sufficiently larger than C_{OSS} the two *LC* loops are sufficiently decoupled during transients. That is, C_{dec} is able to maintain voltage while supplying transient energy. During a short circuit event though this capacitance is not sufficient to supply the much larger transient energy and the energy is supplied from larger DC-link capacitors. This makes the energy draw on C_{dec} the new stimulus for overvoltage as opposed to the di_d/dt during normal switching.

This is evident in Fig. 40 with the single device short circuit where the V_{DS} ringing—and associated overshoot—is at the lower resonant frequency of the $L_{dec}C_{dec}$ loop as opposed to the L_DC_{OSS} resonant frequency seen during normal switching. Additionally, the oscillation on V_{DS} begins during peak di_D/dt also showing that di_D/dt is not the main concern for overvoltage during short circuits. The fact that the decoupling loop can potentially be the main short circuit energy source may not cause an issue with a single device, but the short circuit current—and therefore energy—scales with parallel devices and L_{dec} remains the same. Fig. 42 shows the small circuit equivalent circuit difference for both normal and short-circuit conditions. During normal switching Vdec is

held sufficiently steady and transient current causes a small peak voltage across the device from $L_D di_D/dt$. During a short circuit event though, the energy draw will be sufficient enough to deplete a normally sized C_{dec} forcing the large short-circuit current to be sourced through the larger L_{dec}. This creates a two-fold issue for overvoltage where in addition to the di_D/dt the depleted capacitor adds a step response.

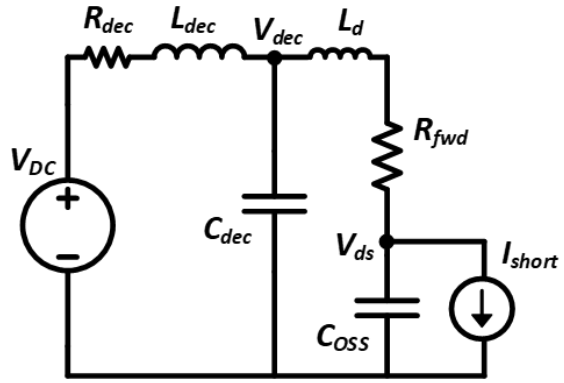


Fig. 42. Small-signal equivalent circuits for power loop

The energy draw during the short circuit can be equated to

$$\frac{1}{2}C_{dec}V_{DC}^2 - \frac{1}{2}C_{dec}(V_{DC} - \Delta V_{dec})^2 = E_{short}\,. \tag{16}$$

Assuming $\Delta V_{dec} < V_{DC}$ gives the voltage drop on the decoupling capacitor

$$\Delta V_{dec} \approx \frac{E_{short}}{V_{DC}C_{dec}}\,. \tag{17}$$

To illustrate this, simulated and experimental short-circuit results are shown in Fig. 43 using four devices in parallel. The extreme overvoltage that can occur without properly sized capacitances is clear. In the experimental results the smallest capacitance shown—*2 uF*—is 4X the value successfully tested with little overshoot in

the single device tests shown previously. Clearly simply scaling C_{dec} is not sufficient. Furthermore, the simulation results show that with four parallel devices, even *5000X* the combined C_{OSS} of the devices—*3 uF*—still leads to C_{dec} voltage drop and significant overvoltage. This value is far larger than the recommended *100X* found in literature.

Equation 17 is shown to be an accurate estimation in both simulation and experimentally as depicted in Table 4 with the waveforms in Fig. 43. The calculated ΔV_{dec} for the lowest C_{dec} in the experimental setup is greater than the actual bus voltage. This shows the worst case scenario where C_{dec} is fully depleted as evidenced by the dip in the current waveform. The severe overvoltage then follows.

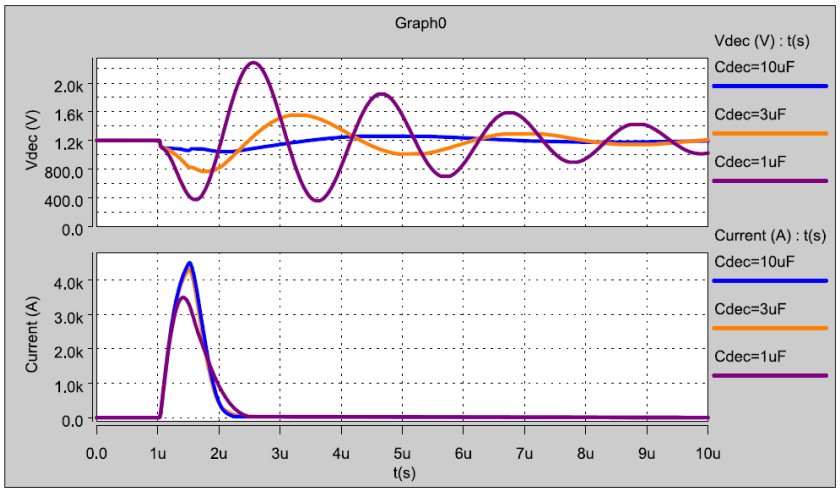
Table 4. Short-circuit Overvoltage

	Simulation ($1200V_{DC}$)			Experimental ($600V_{DC}$)			
	1uF	3uF	10uF	2uF	7uF	7uF	17uF
Calculated (ΔV)	1400	467	140	700	200	200	83
Actual (ΔV)	840	450	151	525	280	250	100

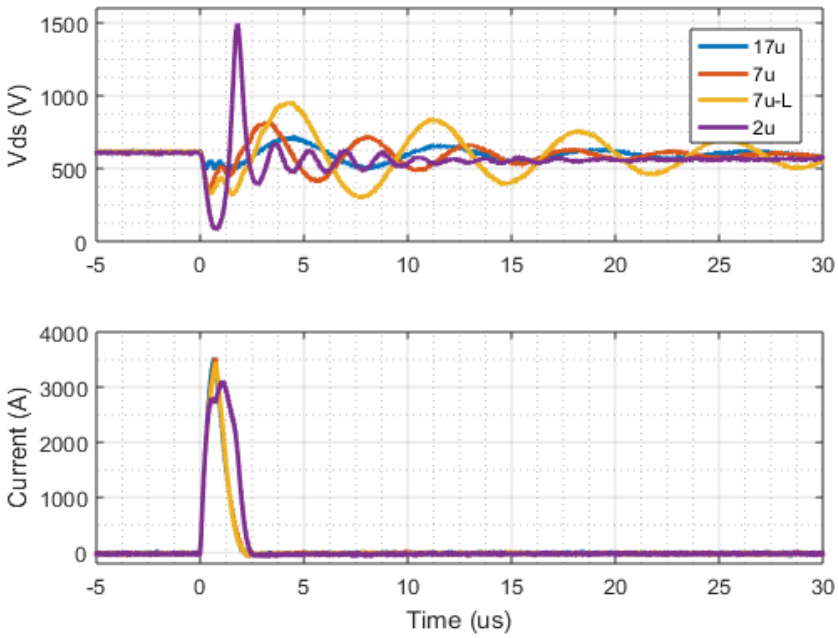
Rewriting Equation 17, C_{dec} can be appropriately sized in order to manage abnormal and potentially damaging overshoot during short-circuit events.

$$C_{dec} \geq \frac{E_{short}}{k_{\Delta VDC} V_{DC}^2} \tag{18}$$

Where $k_{\Delta VDC}$ is the percent change. Setting $k_{\Delta VDC}$ to 10% a final decoupling capacitance of *5 uF* per device is selected.



(a) Simulation at VDC = 1200V

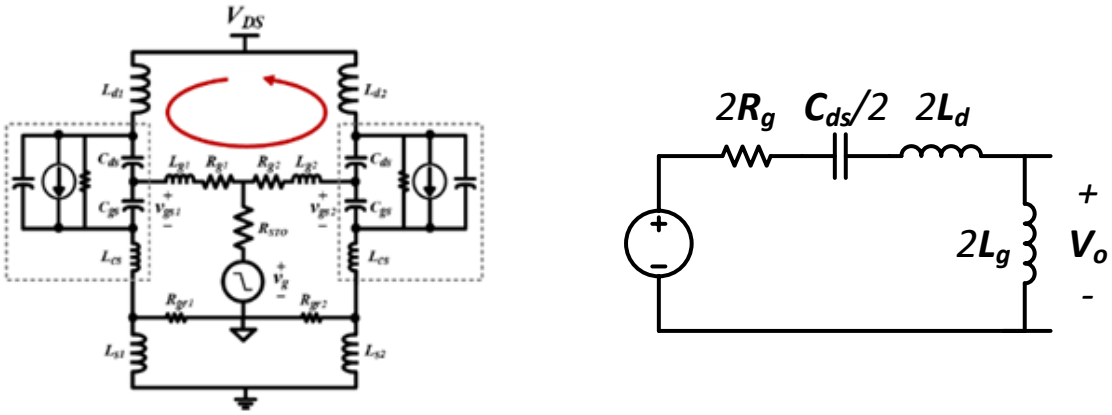


(b) Experimental results at V_{DC} = 600V

Fig. 43. Short-circuit induced overvoltage

4.4 GATE OSCILLATION

A large obstacle with parallel devices—module or discrete—is the unavoidable additional parasitic circuits. The most typical way of paralleling devices is to directly connect gates, drains, and sources in order to achieve a single equivalent switch. This creates a few inherent loops as shown in Fig. 44(a). The most significant of these is the *RLC* resonant tank consisting of L_d, C_{gd}, L_g, and R_g. The reduced small signal equivalent circuit for this is shown in Fig. 44(b).



(a) Complete schematic (b) Reduced resonant tank

Fig. 44. Small signal equivalent gate drive and power stage circuit for two parallel devices

The parasitic *RLC* circuit can potentially cause oscillation in the gate voltage if not properly accounted for. The resonant frequency for this is

$$\omega_o = \frac{1}{\sqrt{LC}} \tag{19}$$

which is typically in the 100MHz range for this type of setup. Furthermore, the damping factor is given by

$$\zeta = \frac{R}{2}\sqrt{\frac{C}{L}}. \tag{20}$$

and is critically damped when equal to one, overdamped when greater than one, and underdamped when less than one. So ideally this value would be less than one but this not in most practical designs.

During short-circuit events a number of less unfavorable conditions exist. These include high collector voltage, high operation temperature, and higher saturation current levels. This setting has been shown to cause a phenomena of negative gate capacitance which cause current redistribution between chips and lead to oscillation [53, 59]. This complex phenomena is inherent in most MOS-gated power devices so from the gate drive perspective, the only thing to do is mitigate the possibility of oscillation.

From the damping factor in Equation 20 it is clear that larger *R* and *C* values while smaller *L* values are desirable to mitigate oscillation. Practically though, this is difficult. Increasing *R*—gate resistance—too much will lead to loss, *C*—C_{gd}—is an inherent property of devices, and *L*—L_d+L_g—has to make trade-offs with other layout concerns. Two different gated devices are taken as a case study in order to understand this phenomena. First, the SiC MOSFET at the focus of this work and additionally a 600V / 50A Si Super Junction (SJ) MOSFET [60]. The reasoning for the second choice is because of the C_{gd} curve—C_{rss} on datasheets—of each device shown in Fig. 45. The SiC FET has a typical curve with C_{gd} monotonically decreasing with drain voltage. The Si SJ FET on the other hand has a unique, non-monotonic C_{gd} vs V_d relationship.

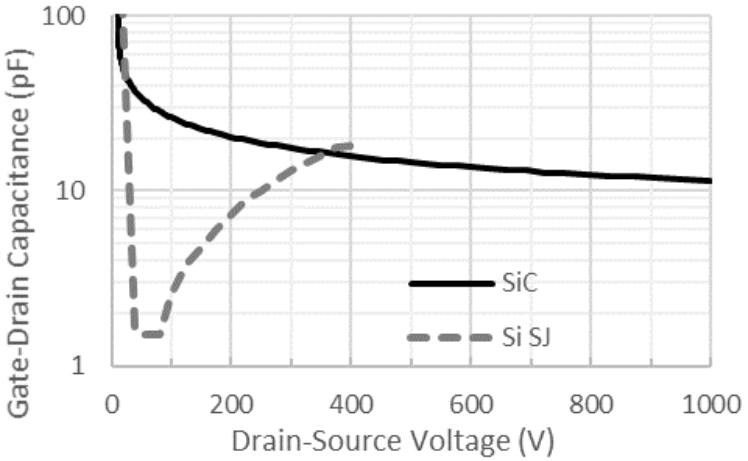
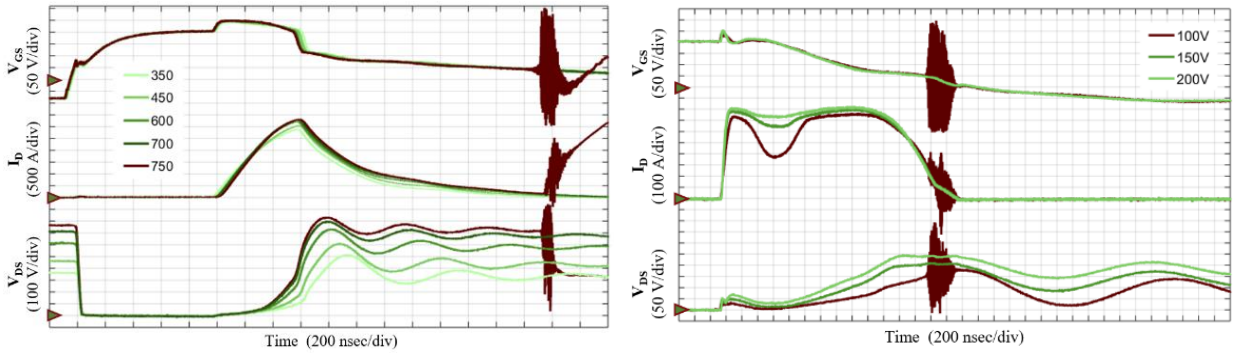


Fig. 45. Gate-drain capacitance curves as a function of drain voltage

The two distinct C_{gd} capacitance curves allow for a clear demonstration of possible oscillation in gate voltage under short-circuit conditions created by the introduced *RLC* resonant tank. In Fig. 46(a) short-circuit turn-off tests are performed with the SiC MOSFET under increasing drain voltage. Note that the current and gate voltage are identical with each test. As drain voltage increases, C_{gd} decreases which eventually leads to oscillation first in v_{gs} then elsewhere and eventually to failure of the devices. Next in Fig. 46(b) the same tests are shown for the Si SJ MOSFETs. Again the gate voltages and drain currents are nearly identical across tests at different drain voltages. In contrast to the SiC MOSFET though, oscillation in the gate voltages occur at low drain voltages and disappear as it increases. Again, this is due to the effect of the irregular C_{rss} vs V_{ds} curve as it effects the resonant tank in Fig. 44(b) and decreases the damping factor. Neither R_g, L_d, or L_g change keeping capacitance as the only dependent variable. This is a feature of devices themselves so the effect can only be mitigated. Furthermore, the parasitic layout inductances can only be limited so much.



(a) Oscillatory false turn-off with SiC MOSFETs under different drain voltages with R_g=10 per device

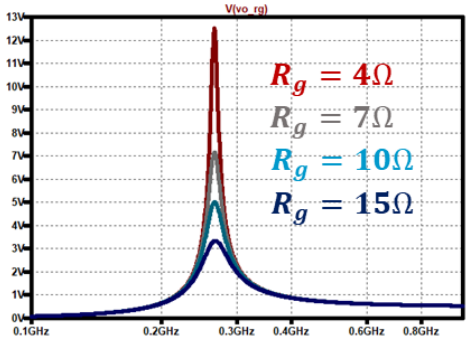
(b) Oscillatory false turn-off with Si SJ MOSFETs under different drain voltages with R_g=10 per device

Fig. 46. Oscillation as a function of gate-drain capacitance

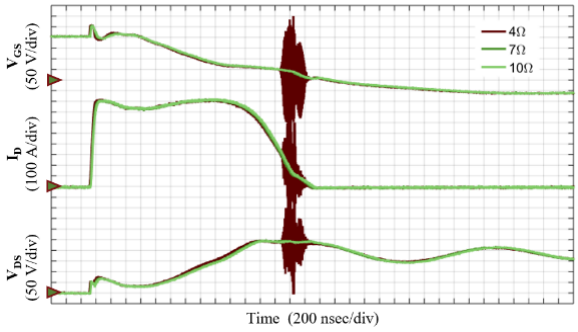
In order to address the gate voltage oscillation issue, the simplest solution is to increase the impedance between gates. This is shown clearly with the frequency response plot shown in Fig. 47(a) as a function of gate resistance. Then in Fig. 47(b) the experimental validation of this is shown. In these tests all waveforms—gate voltage, drain current, and drain voltage—are nearly identical with only oscillation at the lowest gate resistance the outlier with oscillation. Again, depending on switching loss demands increasing gate resistance may not be a valid option. Another solution is to use ferrite beads instead which have low DC resistance but larger high frequency impedance. Commercial ferrites of this variety are commonly rated by their impedance at 100MHz which is the range needed for this application. A few suitable commercial parts are listed in Table 5.

Table 5. Commercial ferrites for mitigating short-circuit gate oscillation

Impedance @ 100MHz (Ω)	DC Resistance (mΩ)	Current Rating (A)	Footprint	Part Number
60	10 m	6	1805	BLM41PG600SN1
60	25 m	3.5	0805	BLM21PG600SN1D
50	12.5 m	12	1206	BLM31SN500SN1L
22	10 m	6	0805	BLM21PG220SN1D



(a) Frequency response for Si SJ circuit with varied gate resistance

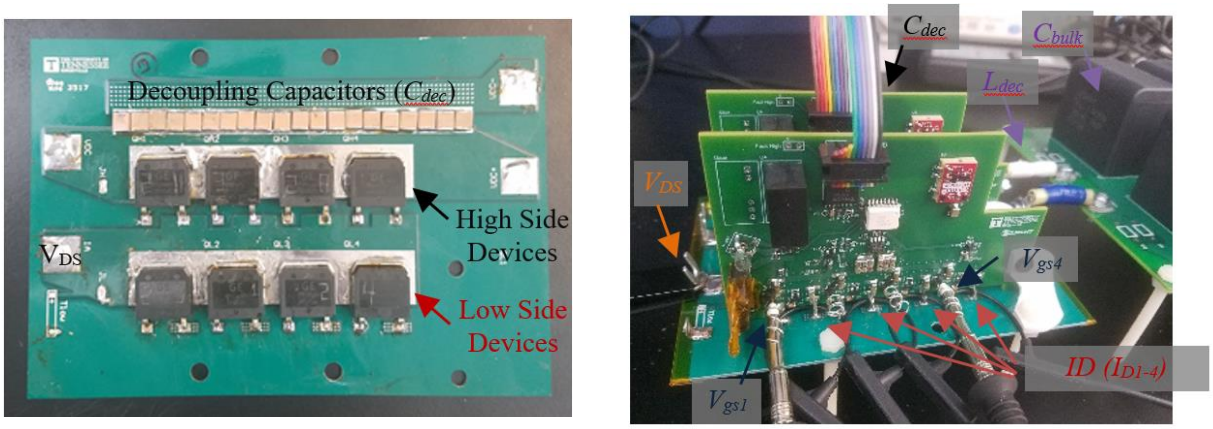


(b) Experimental short-circuit turn-off tests

Fig. 47. Effect of gate resistance on oscillation during short-circuit turn-off

4.5 EXPERIMENTAL RESULTS

With the protection time proven adequate, overvoltage concerns addressed, and oscillation abnormalities understood the overall protection is tested. The physical setup is shown in Fig. 48 with four devices in parallel. The accompanying gate drivers and current probes are highlighted. The short-circuit turn-off waveforms at a bus voltage of 1200V are shown in Fig. 49. Delay time is just 700ns with current completely shut off within 2us of the event. Additionally, overvoltage is just 120V or 10% due to proper design of decoupling capacitance.



Power stage board with 4 parallel devices

Gate driver and power stage

Fig. 48. Physical setup of parallel SiC

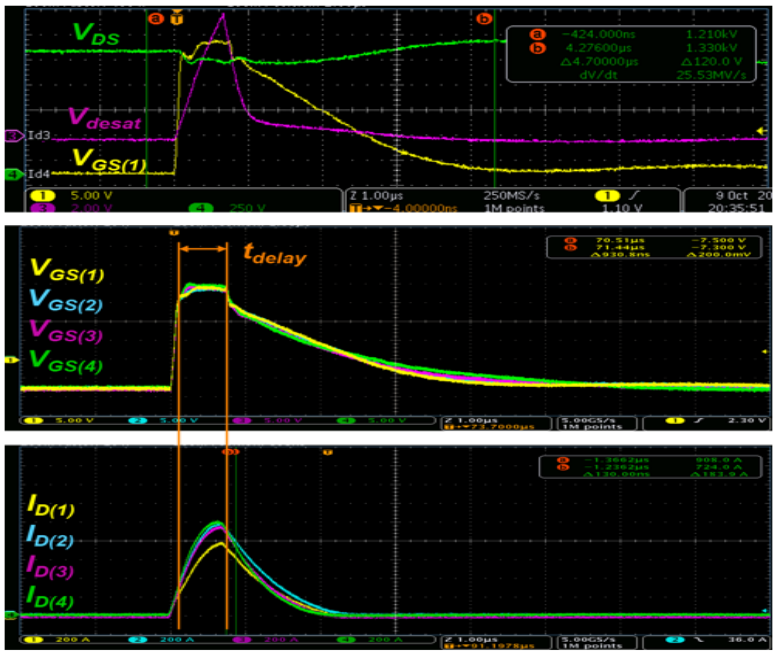


Fig. 49. Successful soft turn-off of short-circuit event with four parallel SiC MOSFETs at 1200V bus

4.6 SUMMARY

In this section, a modified desaturation detection scheme fast enough to meet the reduced withstand capability of SiC MOSFETs is implemented. Short-circuit tests are performed with a single device validating the approach with a detection time under 1 μs. A single SiC MOSFET is found to experience nearly 20X rated current during short-circuit conditions. Two major issues with parallel devices in short-circuit environments—voltage overshoot and v_{gs} oscillation—are studied and addressed. A new approach to decoupling capacitance design is presented to account for high transient energy caused by the very large short-circuit current of SiC MOSFETs. Proper gate decoupling is also applied in order to avoid failure during short-circuit turn-off caused by gate voltage oscillation. Finally, with these considerations the short-circuit protection of 4 parallel MOSFETs is demonstrated at 1200 V with current reaching 3.5 kA.

5 GATE DRIVE DESIGN FOR PARALLEL DEVICES

Achieving high efficiency and reliable performance out of power devices depends on capable gate drive circuitry. In this chapter the design space is first presented to establish design considerations. Basic driving considerations within this scope and considering multiple parallel devices are then presented. Achieving SiC's fast switching and low loss potential comes with drawbacks though of which *Cdv/dt* induced gate voltage or cross-talk is a main concern. This is analyzed and a mitigation scheme extended from single device applications. Overall loss of the phase-leg under test is experimentally verified before finally testing in a continuous half-bridge setup. This demonstrates the real power capability that can be extended to a variety of high power VSC applications.

5.1 DESIGN SPACE

First understanding the design space is critical for robust design. Almost all of the literature reviewed on parallel SiC or MOSFETs has been done at or for relatively low voltage and power levels. The application space of this work is high power VSCs with DC voltages in the 1 kV to 1.5 kV range. A key here is that for most applications 20 kHz is high frequency. For most line frequency applications Si devices are commonly used at 3-5kHz. The target switching frequency is a key parameter for adequately addressing parallel objectives.

As presented in the introduction, the phase leg configuration of power devices is the building block of most VSCs. A half-bridge continuous setup is the simplest way to test device and gate drive design in a way that extends to other VSC applications. This

configuration is ideal for lab testing because an almost purely reactive load can be utilized. A very large apparent power can be created to validate the power electronic design while drawing—in an ideal case—just the power loss from the grid. The half-bridge configuration for testing of the gate drive performance is shown in Fig. 52.

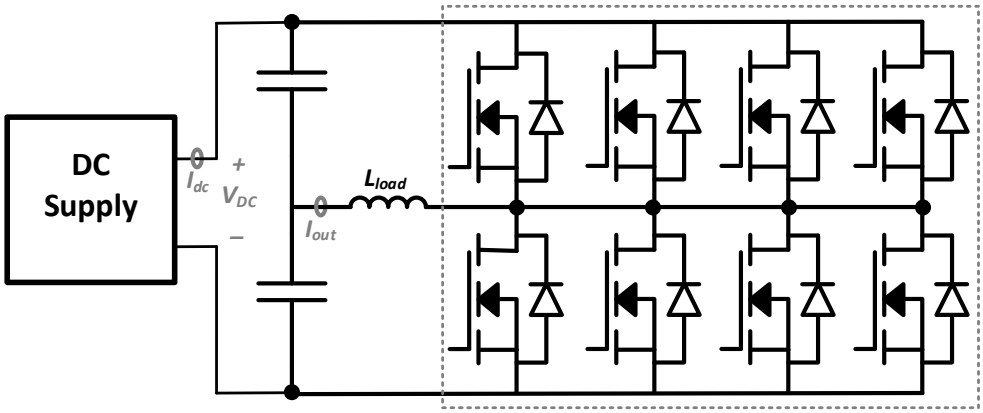


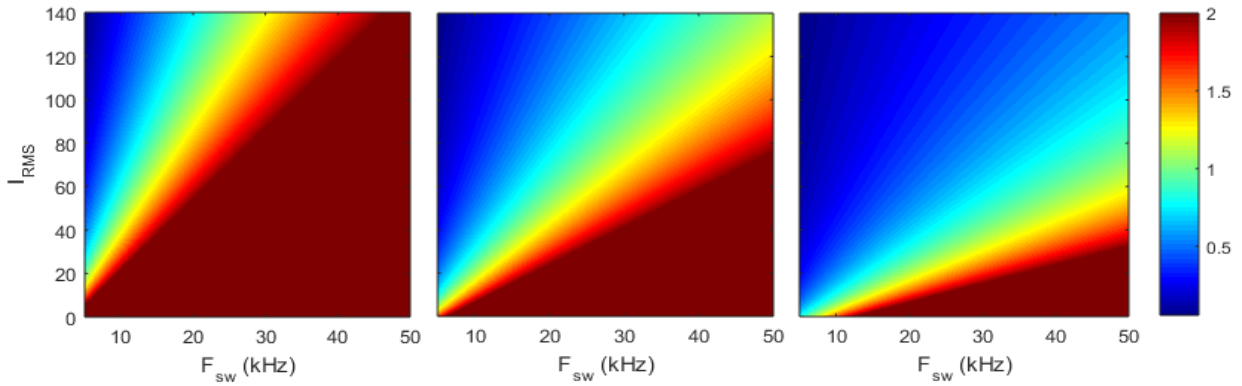
Fig. 50. Half-bridge configuration for continuous testing

The device losses in a VSC per switch location—four devices in Fig. 52—are

$$P_{device} = P_{cond} + P_{sw} = d \cdot R_{on} \cdot I_D^2 + f \cdot \left(E_{on} + E_{off}\right). \tag{21}$$

With this a key concern for utilizing parallel devices is the ratio of switching loss to conduction loss. If conduction loss dominates the effect of dynamic current imbalance is minimal. For the half-bridge configuration, the ratio of switching loss to conduction loss is shown in Fig. 51 at different operating points and switching loss values. The current imbalance issue is a multidimensional problem of which the focus on dynamic imbalance mitigation in literature. At a desired 20 kHz switching frequency, the impact of current imbalance caused by devices themselves can be minimized through minimizing

switching loss. Therefore, the active dynamic current balancing technics are not ideal for this application space as they do not take into account the conduction loss effects. The rest of this chapter will focus on minimizing overall parallel switching loss.



(a) P_{sw} = 30 mJ (b) P_{sw} = 16 mJ (c) P_{sw} = 8 mJ

Fig. 51. Ratio of conduction loss to switching loss at 1200V as function of switching frequency

5.2 Basic Driving Considerations for Parallel Devices

The gate driver is the power amplifier for the PWM signal to the voltage at the gate terminals and must be able to provide sufficient current. A first consideration for gate drive design is power requirement to turn on and turn off the device. The losses alone for switching the device are

$$P_{gate} = nQ_G(V_{CC} + V_{EE})f_s\,. \tag{22}$$

where n is the number of devices in parallel, V_{CC} is the on state voltage and V_{EE} is the off state voltage, Q_G is the gate charge, and f_s the switching frequency. Furthermore, this power consumption is only distributed at the turn-on and turn-off transitions. The transient current requirement for charging gate capacitance is

$$I_{gate} = n\frac{V_{CC}}{R_G}. \tag{23}$$

Driving multiple high current devices at high frequency requires substantial power and current. A survey of commercially available drivers are shown in Table 5 with key parameters listed. Additionally, commercial IC's cannot source or sink a significant amount of current—the highest is A current buffer is required in order overcome this limitation. A survey of commercially available current buffers is shown in Table 7. The two main approaches to obtaining the required high current gain are a totem pole BJT configuration or a MOSFET bridge. The totem pole is easier to control but the MOSFET pair allows for separate turn-on and turn-off resistances.

Table 6. Commercially available gate drive ICs

Manufacturer	Part Number	Max Vcc	DC Iso (kV)	CMR (kV/us)	Propagation Delay (ns)	Current Source	Current Sink	Soft Turnoff	Miller Clamp
Avago	ACPL-339J	30	5	25	300	-	-	Yes	
Avago	ACPL-333J	30	5	50	250	2.5	2.5	Yes	Yes
Fairchild	FOD8318	30	5	35	500	2.5	2.5		Yes
TI	ISO5852SDWR	30	5.7	100	76	2.5	5	Yes	Yes
TI	ISO5451	30	5.7	100	76	2.5	5		Yes
ST	STGAP1S	40	3	50	100	5	5	2-level	Yes

Table 7. Commercially available current buffers

Manufacturer	Part Number	Max Voltage	Current Source	Current Sink	Type	Configuration	Propagation Delay	Package
Vishay	Si4564DY	40	40	40	array	PN	20-50	SOIC-8
IXYS	IXDN630CI	35	30	30	driver	PN	46	TO-220
Vishay	SQJ500AEP	40	30	30	array	PN hi/low		SO-8L
ST	MJD44H11	80	16	16	array	BJT Totem Pole		TO-252
Microchip	TC4451	18	13	13	driver	PN hi/low	44	SOIC-8
IXYS	IXDN609SIA	35	9	9	driver	PN	42	SOIC-8
ST	STL40C30H3LL	30	8	10	array	PN hi/low		PowerFLAT
Zetex	ZXGD3003E6	40	5	1.5	driver	BJT Totem Pole	2	SOT-23
ON Semi	NCD5701C	36	4	6	driver	PN hi/low	70	SOIC-8
TI	UCC2753	35	2.5	2.5	driver	PN hi/low	17	SOT-23

Another important consideration is defining a good gate loop. This is crucial for minimizing ringing in the gate voltage. Like the power stage, this is done with a properly sized decoupling capacitor for the buffer stage. This capacitance is sized as a function of percent variation in V_{CC} and V_{EE}—k_{GS}—during the turn-on and turn-off transitions.

$$C > Q_g/(k_{GS} \times V) \tag{24}$$

For the devices used in this work the required C_{CC} is *0.830 uF* and C_{EE} is *3.320 uF* based on a gate charge of *166 nC* and a k_{GS} of *0.01*.

A kelvin source connection with a small resistor is necessary with this type of configuration. With parallel devices the sources of each device is connected through both the power stage and the gate driver. This resistance assures high power stage current does not flow through the gate driver.

5.3 CROSS-TALK MITIGATION

Realizing low loss from fast switching inherently means high voltage and current slew rates. These large transients can have detrimental effects on the normal operation of the device. When the off-state switch in the phase leg experiences high *dv/dt*, current is induced into the gate loop by means of C_{gd}. During a positive drain to source *dv/dt* the induced voltage is positive which can lead to unwanted channel conduction and additional loss. During a negative drain to source *dv/dt* the induced voltage (ΔV_{gs}) is negative which can potentially cause gate reliability issues. Little work exists on this phenomena in paralleled devices. Analysis starts with the developed simulation model in order to understand the any impacts or considerations. Initially, the parallel environment does not change any of the effects of cross-talk. That is, induced voltage can be found at each individual gate. The simulation results for induced voltage at individual gates is shown in Fig. 52 demonstrating the need for mitigation.

The gate impedance regulation approach is selected from the literature review [34]. Impedance regulation occurs by placing a relatively large capacitance at the gate terminals during the off-state in order to reduce the gate loop impedance. Therefore, the potential effects of the *Cdv/dt* current is reduced and cross-talk mitigated. A simplified schematic of this is shown in Fig. 53(a) which will be used at the gate terminal of each individual device. A small MOSFET is used to enable the capacitance while the device is off. The biggest challenge with this scheme is proper timing of the control FET. During normal turn-off of the device, if C_{gir} is activated too early the gate can be pulled low leading to very large *di/dt's* as depicted in Fig. 53(b). Additionally, at turn-on there is an

opposite effect of poor timing. If C_{gir}—which is much larger than C_{ISS}—is still active the turn-on speed will be severely limited.

In order to properly size C_{gir} Equation 9 is used where the induced voltage is a function of device capacitances, internal gate resistance, V_{ds}, slew rate, and C_{gir}. With these parameters ΔV_{gs} is plotted as a function of C_{gir} as shown in Fig. 55. The benefit of larger capacitance levels off around *200 nF* so this value is chosen. Again, this is much larger than the *3.3 nF* C_{ISS} or each device so proper control is critical.

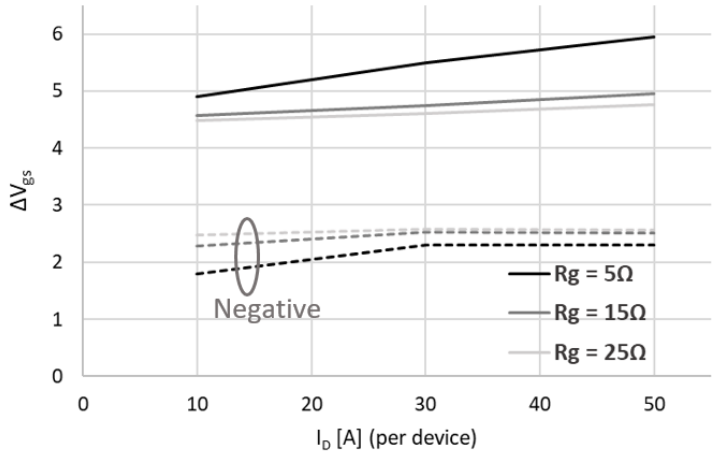
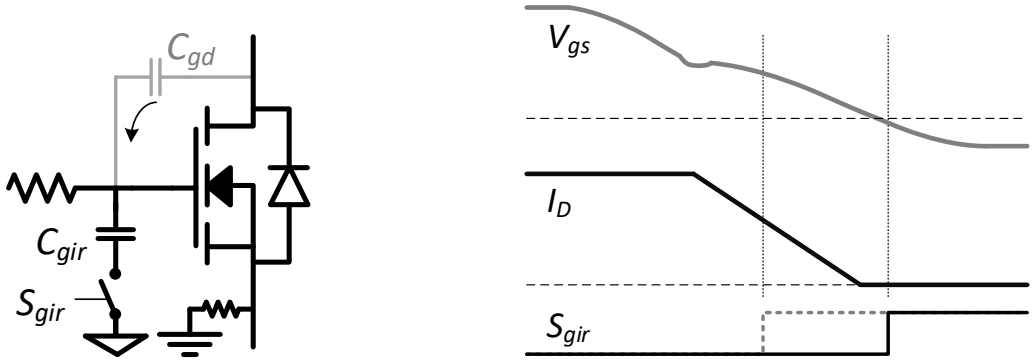


Fig. 52. Simulated cross-talk at 1200V



(a) Simplified schematic (b) Control limitation

Fig. 53. Cross-talk mitigation design

Fig. 54. Induced gate voltage as a function of C_{gir}

To test the cross-talk mitigation experimentally the phase leg is setup so that the top switch in the phase leg is the active switch—hard switching. The low side gates are at ground in this configuration allowing for much more accurate passive probes to be used for measurement. Passive probes allow the effect on the lower gates to be accurately measured as opposed to floating active probes on the high side devices. Experimental results for the difference in ΔV_{gs} with mitigation compared to without are shown in Fig. 55. The safety margin added by the gate impedance regulation scheme is

significant across a wide operating region. Waveforms for the worst recorded case are shown in Fig. 56 at a bus voltage of 1200V and load current of 120A—30A per device. Not all individual gate voltages are identical but they are similar and the impedance regulation works well with in a parallel setup. The first voltage spike in the waveforms is due to L_{cs}. That is, the current commutates through the body diode before the V_{ds} transient which means that a large part of the voltage seen is simply from inability to measure at the actual gate source internal to the packaging.

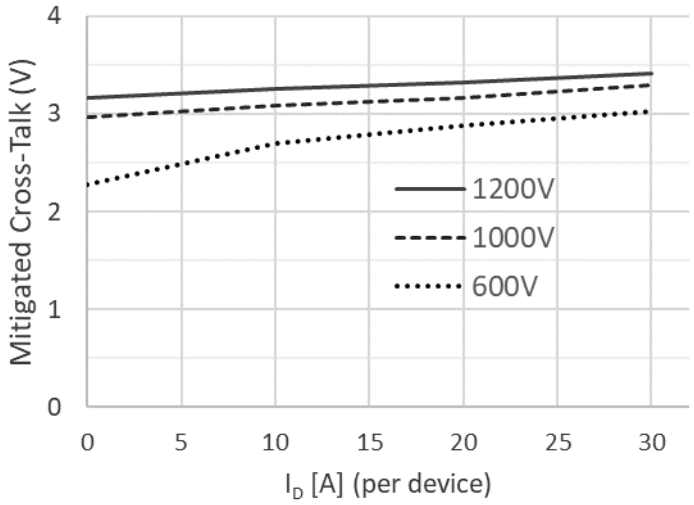


Fig. 55. Experimental results for cross-talk mitigation

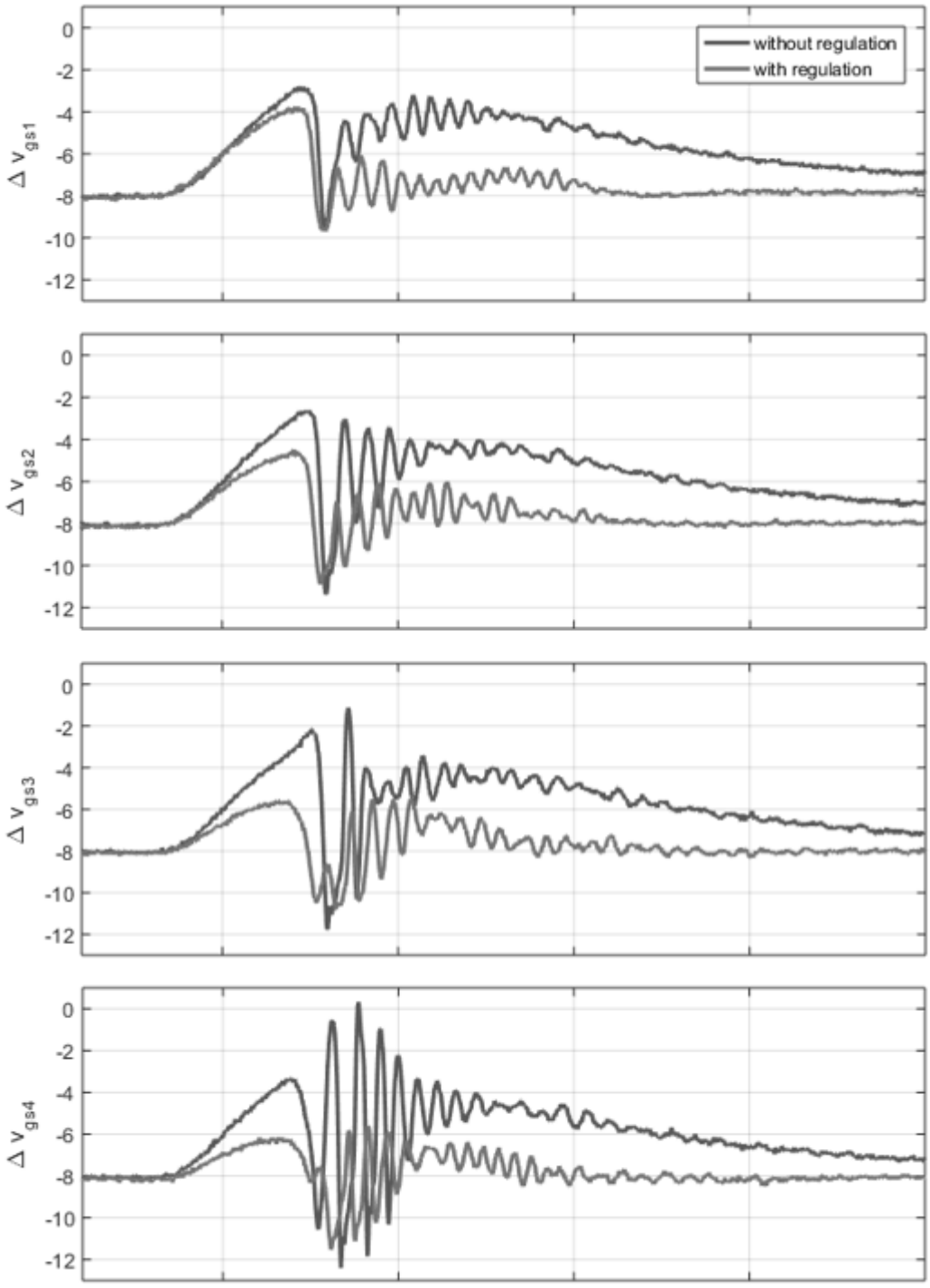


Fig. 56. Cross-talk reduction in parallel devices

5.4 LOSS RESULTS

The double pulse test (DPT) setup is used to characterize switching loss with a focus on four devices in parallel at each switch location. The high side devices' body diode is utilized as the freewheeling diode. In order to accurately measure losses with the fast slew rates of SiC high bandwidth probes are essential. The effective bandwidth of a ramp signal can be estimated by minimum rise time (t_r) and fall time (t_f)

$$f_{sw} = \frac{0.35}{\min(t_r, t_f)}. \tag{25}$$

Two of the most viable choices for current measurement are the coaxial shunt and the Rogowski coil. The coaxial shunt has much larger bandwidth but is extremely layout intrusive especially measuring multiple device currents in parallel. A Rogoski coil on the other hand allows for measurement through device leads. With a rated bandwidth of *30 MHz* the PEM CWT1 Ultra-mini Rogowski probe supports rise and fall times down to *12 ns* from Equation 25. This is sufficient based on simulation results. Furthermore, for accurate V_{ds} measurement the Tektronix TPP0850 passive probe is utilized with a more than sufficient *800 MHz* bandwidth rating.

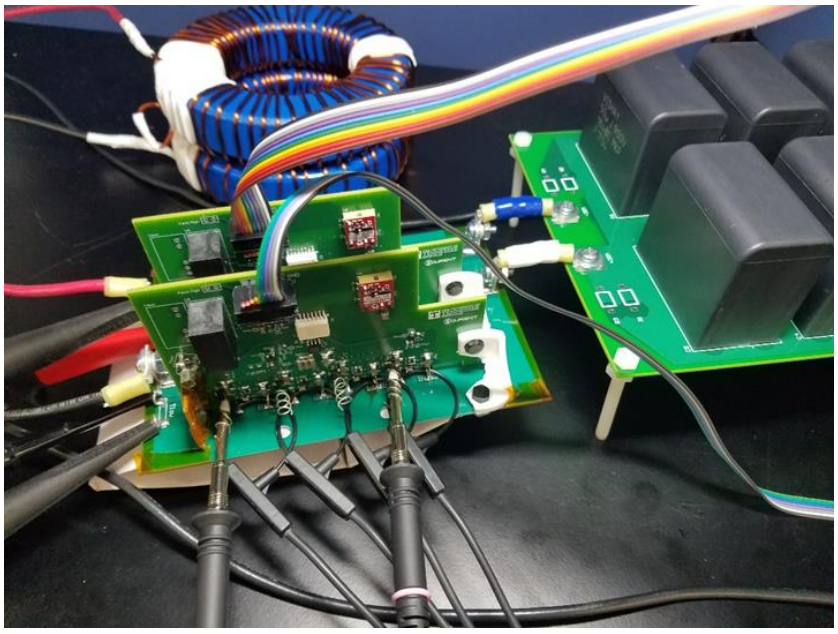
The physical test setup is shown in Fig. 57 with a Rogowski probe for each of the four devices under test. A load inductor of 360 μH is used in order to minimize current variation (ΔI_L) during switching transients based on the equation

$$L \geq \frac{V_{DC}}{\Delta I_L} t_{sw} = \frac{V_{DC}}{k_{\Delta I_L} \Delta I_L} t_{sw} \,. \tag{26}$$

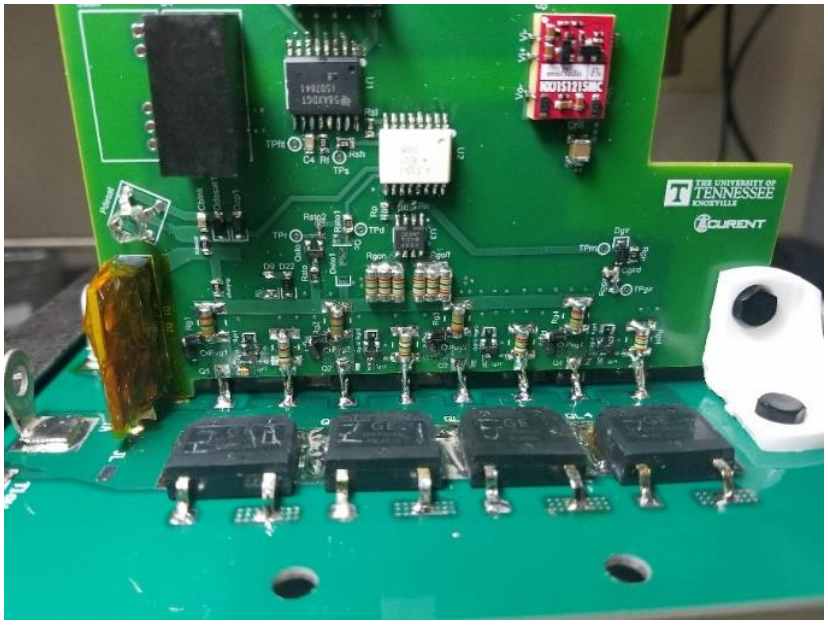
Similarly a sufficient capacitor bank (C_{bulk}) is required to minimize voltage variation due to load current draw. Based on the following equation a capacitor bank equivalent to 75 μF is used.

$$C_{bulk} \geq \frac{L I_L^2}{(2V_{DC} - \Delta V_{DC})} \approx \frac{L I_L^2}{k_{\Delta V_{DC}} V_{DC}^2} \tag{27}$$

Target characterization is full rated current through each device which is 50A or 200 A total. Waveforms at this condition with a 1200 V bus are shown in Fig. 58. The layout mitigation of L_{CS} is visible in that there is very little dynamic current imbalance. Devices with similar transconductance curves are used to illustrate this point. With this, current slew rates of over 1.5 A/ns through each device are achieved at both turn-on and turn-off. With four parallel devices this equates to over 6 A/ns with almost negligible overshoot. Overshoot across bus voltages is plotted in Fig. 59. This is a key performance marker due to up-stream EMI issues that excessive overshoot can cause. Voltage slew rates are 28 V/ns during turn-off and 20 V/ns during turn-on. Additionally there are no issue with oscillation between gate voltages. Note with a single device slew rates of 100 V/ns and 8 A/ns are achievable at both turn-on and turn-off. More so, all off this is done with a V_{DS} overshoot under 10% (112.8V at 1200V_{DC}). The limitation in gate resistance comes from the short-circuit oscillation issues presented earlier.

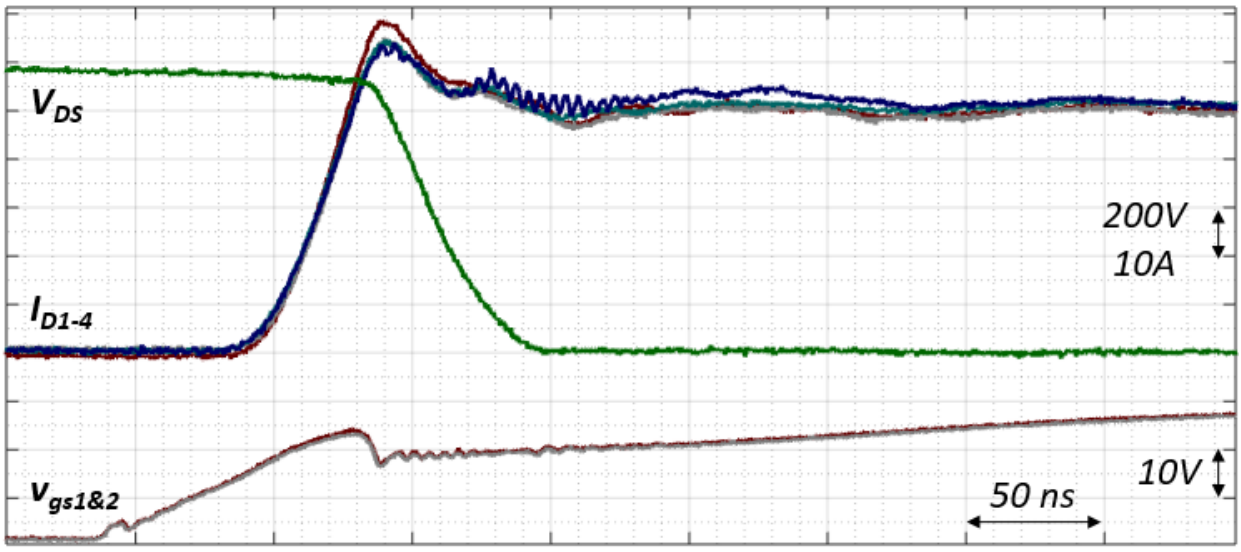


(a) complete setup

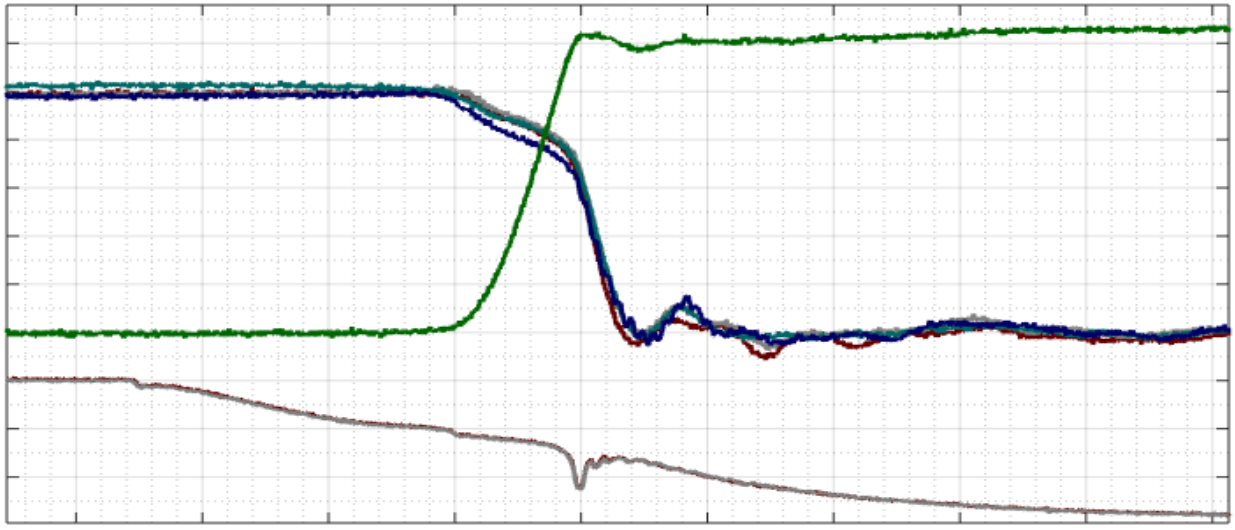


(b) connection of devices to power stage and gate driver

Fig. 57. DPT for parallel devices



(b) turn-on



(b) turn-off

Fig. 58. Switching transients with 4 parallel devices at 1200V and 200A

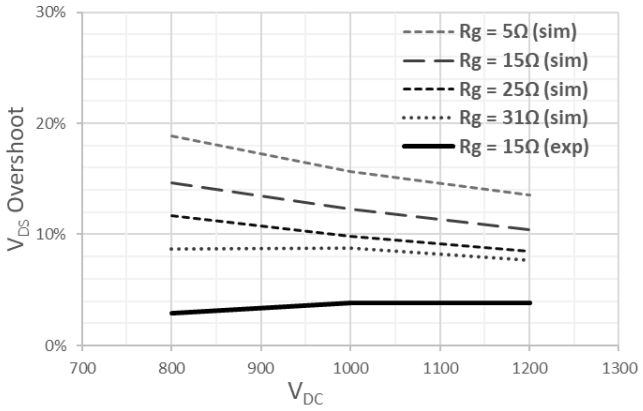
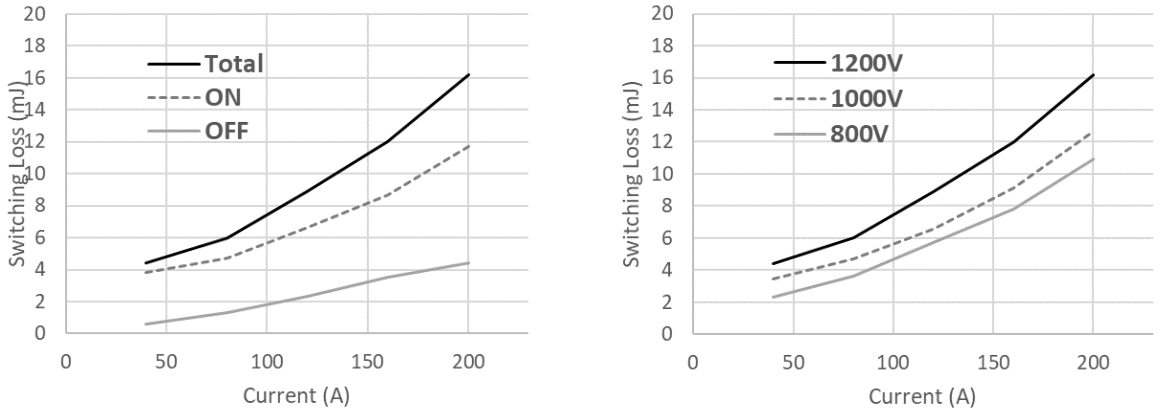


Fig. 59. Voltage overshoot with 200A load current

The room temperature switching losses for the four device per switch phase leg are shown in Fig. 60. Turn-on loss dominates switching losses as evident in Fig. 60(a). Using the survey of comparable modules in Table 3 as a bench mark, using discrete devices lower switching losses than commercial modules are achievable. The next section will extend the results from pulse tests to converter level implementation.



(a) turn-on and turn-off distribution

(b) at different bus voltages

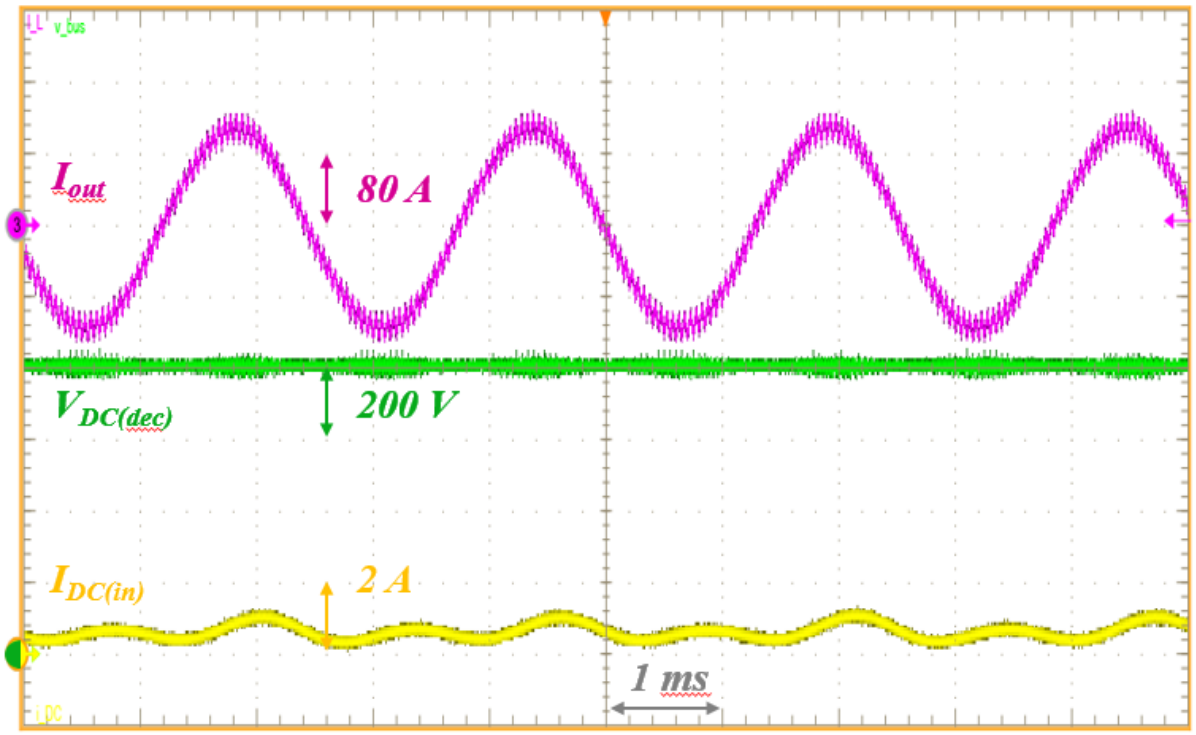
Fig. 60. Loss plots with rated 1200V bus

5.5 CONTINUOUS

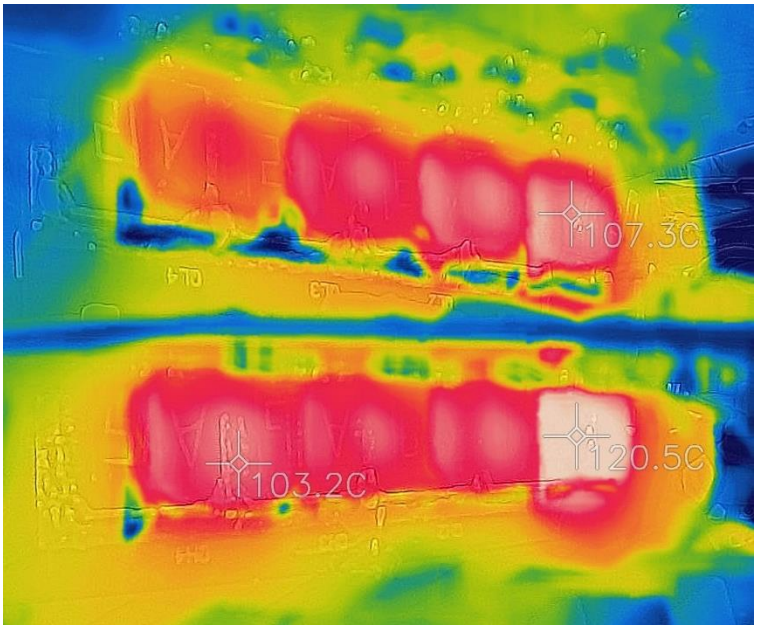
Using the half-bridge configuration shown in Fig. 50 the design approach is tested in an actual converter setup. Four MOSFETs are paralleled per switch. Waveforms at 800 V_{DC} and 80 A_{rms} output are shown in Fig. 61(a). This equates to 20 A_{rms} and 28 A_{peak} per device. The voltage at the decoupling capacitor demonstrates the small overshoot. In Fig. 61(b) the thermal and consequently power distribution between devices is shown. There is not major deviation between device temperatures. Also, the overall cooling setup was out of scope and not optimized.

5.6 SUMMARY

This chapter took standard approach to SiC MOSFET gate driver design and presented considerations needed for parallel devices. Additionally, a new approach to cross-talk mitigation is extended to the parallel setup and proven experimentally. The loss performance is proven in the DPT setup matching commercial module performance with similar voltage and $R_{DS(ON)}$ ratings. Finally, utilizing a half-bridge configuration the parallel gate drive design approach is proven in converter level operation.



(a) Bus voltage and input and output current waveforms



(b) Thermal image

Fig. 61. Half-bridge using four parallel SiC MOSFETs per switch at 800V / 80A_{rms}

6 CONCLUSIONS AND FUTURE WORK

6.1 CONCLUSION

Increasing power output of high power VSCs is a critical development direction due to the increasing demand for renewable energy, transportation, as well as many other applications. Using discrete SiC MOSFETs is an attractive solution due to the cost and design flexibility. These devices outperform current Si counterparts and parallel sufficiently well in hard switched, high power applications as long as proper measures are taken to address key issues. This work has presented these key issues along with insight and measures to address them in practical design.

The nonhomogeneity in commercial devices was characterized to find inherent limitations in parallel devices. Sensitivities for device and external circuit parameters were established and utilized in design to achieve module level parasitics with discrete devices. At which point current distribution becomes a factor of the devices themselves. Additionally it was shown how the design freedom can be used to reduce overvoltage through distributing power stage inductance. Next, concerns with parallel 1.7 kV SiC have not been documented. By addressing large transient energy concerns as well as gate stability, successful protection in under 1 μs of nearly 20X rated current at 1200V is demonstrated. Additionally, a mitigation technique for the effect of $C_{gs}dv/dt$ induced gate voltage was demonstrated with parallel devices. Loss results comparable to similar modules are achieved and system level performance demonstrated in an half-bridge setup. With key gate drive considerations addressed, SiC MOSFETs can be well paralleled to meet growing demands in high power VSC applications.

6.2 FUTURE WORK

Cross-talk mitigation was extended sufficiently well to parallel devices and less negative voltage margin could be used. In real budget cases, it may be feasible to use no negative voltage offset and still achieve the performance desired.

The cooling system was not analyzed in this work but would be an interesting study to see if the extra spacing allotted with discrete devices in parallel has any benefit with a good thermal management system. In theory, allowing for more heat spreading the hotter dies may be cooled better without the added coupling seen inside a module. This would take a detailed modeling approach.

The insulated metal substrate (IMS) power stage PCB used in this work allowed for a vertical layout leading to very low parasitics. Furthermore, much more thermally conductive core material is available than used here. A vertical layout is not currently possible with module packaging. There could be significant performance results utilizing this IMS approach with directly attached dies.

Finally, all of the current balancing approaches reviewed in literature dealt strictly with dynamic current balance. This may not actually address the objective of even power loss distribution. It was discussed that many applications in this space will actually depend more on steady-state current balance or at least a combination of both. It would be very interesting to utilize temperature information and control dynamic current—through delay of individual buffers—to mitigate effects of both dynamic and steady-state current imbalance.

REFERENCES

[1] B. K. Bose, "Power Electronics and Motor Drives Recent Progress and Perspective," *IEEE Transactions on Industrial Electronics,* vol. 56, pp. 581-588, 2009.
[2] A. Beainy, C. Maatouk, N. Moubayed, and F. Kaddah, "Comparison of different types of generator for wind energy conversion system topologies," in *2016 3rd International Conference on Renewable Energies for Developing Countries (REDEC)*, 2016, pp. 1-6.
[3] G. Wang, J. Mookken, J. Rice, and M. Schupbach, "Dynamic and Static Behavior of Packaged Silicon Carbide MOSFETs in Paralleled Applications," in *APEC*, 2014, pp. 1478-1483.
[4] H. Li, S. Munk-Nielsen, X. Wang, R. Maheshwari, S. Beczkowski, C. Uhrenfeldt*, et al.*, "Influences of Device and Circuit Mismatches on Paralleling Silicon Carbide MOSFETs," *IEEE Transactions on Power Electronics,* vol. 31, pp. 621-634, 2016.
[5] Z. Chen, D. Boroyevich, and R. Burgos, "Experimental Parametric Study of the Parasitic Inductance Influence on MOSFET Switching Characteristics," in *International Power Electronics Conference*, 2010, pp. 164-169.
[6] J. Wang, H. Shu-Hung, and R. Tin-ho Li, "Characterization and Experimental Assessment of the Effects of Parasitic Elements on the MOSFET Switching Performance," *Transactions on Power Electronics,* vol. 28, pp. 573-590, 2013.
[7] A. Lemmon, M. Mazzola, J. Gafford, and C. Parker, "Instability in Half-Bridge Circuits Switched With Wide Band-Gap Transistors," *Transactions on Power Electronics,* vol. 29, pp. 2380-2392, 2014.
[8] Y. Sugihara, K. Nanamori, S. Ishiwaki, Y. Hayashi, K. Aikawa, K. Umetani*, et al.*, "Analytical Investigation on Design Instruction to Avoid Oscillatory False Triggering of Fast Switching SiC-MOSFETs," in *ECCE*, 2017, pp. 5113-5118.
[9] Q. Zhao and G. Stojcic, "Characterization of Cdv/dt Induced Power Loss in Synchronous Buck DC-DC Converters," in *APEC*, 2004, pp. 292-297.
[10] J. Wang and H. S.-H. Chung, "New Insight into the Mechanism of the Spurious Triggering Pulse in the Bridge-leg Configuration," in *PESA*, 2013, pp. 1-6.
[11] J. Dodge, "Eliminating Parasitic Oscillation between Parallel MOSFETs," ed: Advanced Power Technology, 2003.
[12] A. O. Semiconductor, "Paralleling Power MOSFETs in Switching Applications," ed: Alpha & Omega Semiconductor, 2013.
[13] T. Ohi, A. Iwata, and K. Arai, "Investigation of Gate Voltage Oscillations in an IGBT Module under Short Circuit Conditions," presented at the IEEE Power Electronics Specialists, 2002.
[14] R. Diaz, W. Paula, R. Wu, F. Iannuzzo, and F. Blaabjerg, "Evidence of Gate Voltage Oscillations during Short Circuit of Commercial 1.7 kV/ 1 kA IGBT Power Modules," in *PCIM Europe*, Nuremberg, Germany, 2015, pp. 916-923.
[15] H. Li, S. Munk-Nielsen, S. Beczkowski, and X. Wang, "A Novel DBC Layout for Current Imbalance Mitigation in SiC MOSFET Multichip Power Modules," presented at the IEEE APEC, 2016.
[16] Y. Mao, Z. Miao, K. Ngo, and C. Wang, "Balancing of Peak Currents between Paralleled SiC MOSFETs by Source Impedances," in *APEC*, 2017, pp. 800-803.

[17] H. Wang and F. Wang, "Power MOSFETs Paralleling Operation for High Power High Density Converters," presented at the IEEE IAS, 2006.
[18] D. Bortis, J. Biela, and J. Kolar, "Active Gate Control for Current Balancing of Parallel-Connected IGBT Modules in Solid-State Modulators," *Transactions on Plasma Science,* vol. 36, pp. 2632-2637, 2008.
[19] R. Alvarez and S. Bernet, "A New Delay Time Compensation Principle for Parallel Connected IGBTs," in *ECCE*, 2011, pp. 3000-3007.
[20] M. Sasaki, H. Nishio, and W. T. Ng, "Dynamic Gate Resistance Control for Current Balancing in Parallel Connected IGBTs," in *APEC*, 2013, pp. 244-249.
[21] Y. Xue, J. Lu, Z. Wang, L. M. Tolbert, B. Blalock, and F. Wang, "Active Current Balancing for Parallel-Connected Silicon Carbide MOSFETs," in *ECCE*, 2013, pp. 1563-1569.
[22] J. Ewanchuk, J. Brandelero, and S. Mollov, "Lifetime Extension of a Multi-die SiC Power Module using Selective Gate Driving with Temperature Feedforward Compensation," in *ECCE*, 2017, pp. 2520-2526.
[23] D. Graovac, "Parallel Operation of Power MOSFETs," ed: Infineon, 2009.
[24] STMicroelectronics, "Paralleling of power MOSFETs in PFC topology," ed, 2009.
[25] Y. Xue, J. Lu, Z. Wang, L. M. Tolbert, B. J. Blalock, and F. Wang, "A compact planar Rogowski coil current sensor for active current balancing of parallel-connected Silicon Carbide MOSFETs," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 4685-4690.
[26] W. Teulings, J. L. Schanen, and J. Roudet, "MOSFET switching behaviour under influence of PCB stray inductance," in *Industry Applications Conference, 1996. Thirty-First IAS Annual Meeting, IAS '96., Conference Record of the 1996 IEEE*, 1996, pp. 1449-1453 vol.3.
[27] H. J. Beukes, J. H. R. Enslin, and R. Spee, "Busbar design considerations for high power IGBT converters," in *PESC97. Record 28th Annual IEEE Power Electronics Specialists Conference. Formerly Power Conditioning Specialists Conference 1970-71. Power Processing and Electronic Specialists Conference 1972*, 1997, pp. 847-853 vol.2.
[28] Q. Liu, S. Wang, A. C. Baisden, F. Wang, and D. Boroyevich, "EMI Suppression in Voltage Source Converters by Utilizing dc-link Decoupling Capacitors," *IEEE Transactions on Power Electronics,* vol. 22, pp. 1417-1428, 2007.
[29] Z. Chen, D. Boroyevich, P. Mattavelli, and K. Ngo, "A frequency-domain study on the effect of DC-link decoupling capacitors," in *2013 IEEE Energy Conversion Congress and Exposition*, 2013, pp. 1886-1893.
[30] Z. Zhang, W. Zhang, F. Wang, L. Tolbert, and B. Blalock, "Analysis of the Switching Speed Limitation of Wide Band-gap Devices in a Phase-leg Configuration," in *ECCE*, 2012, pp. 3950-3955.
[31] J. Wang and H. S.-H. Chung, "Impact of Parasitic Elements on the Spurious Triggering Pulse in Synchronous Buck Converter," *Transactions on Power Electronics,* vol. 29, pp. 6672-6685, 2014.
[32] S. Xu, W. Sun, and D. Sun, "Analysis and Design Optimization of Brushless DC Motor's Driving Circuit Considering the Cdv/dt Induced Effect," in *ECCE*, 2010, pp. 2091-2095.

[33] T. Wu, "Cdv/dt Incuced Turn-on in Synchronous Buck Regulators," ed: International Rectifier, 2007.
[34] Z. Zhang, F. Wang, L. Tolbert, and B. Blalock, "A Novel Gate Assist Circuit for Cross Talk Mitigation of SiC Power Devices in a Phase-leg Configuration," in *APEC*, 2013, pp. 1259-1265.
[35] Fairchild. (2013, Active Miller Clamp Technology. Available: https://www.fairchildsemi.com/application-notes/AN/AN-5073.pdf
[36] Avago. (2010, Active Miller Clamp.
[37] T. Funaki, "A study on self turn-on phenomenon in fast switching operation of high voltage power MOSFET," in *CPMT Japan*, 2013, pp. 1-4.
[38] Z. Chen, M. Danilovic, D. Boroyevich, and Z. Shen, "Modularized design consideration of a general-purpose, high-speed phase-leg PEBB based on SiC MOSFETs," in *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*, 2011, pp. 1-10.
[39] Z. Zhang, F. Wang, L. M. Tolbert, and B. Blalock, "Active Gate Driver for Crosstalk Suppression of SiC Devices in a Phase-Leg Configuration," *Transactions on Power Electronics,* vol. 29, pp. 1986-1997, 2014.
[40] Z. Miao, Y. Mao, K. Ngo, and W. Kim, "Package Influence on the Simulated Performance of 1.2 kV SiC Modules " in *WiPDA*, 2015, pp. 306-311.
[41] Z. Miao, C. M. Wang, and K. Ngo, "Simulation and Characterization of Cross-Turn-On Inside a Power Module of Paralleled SiC MOSFETs," *Transactions on Components, Packaging and Manufacturing Technology,* vol. 7, pp. 189-192, 2017.
[42] S. Jahdi, O. O. Alatise, and J. A. O. Gonzalez, "Temperature and Switching Rate Dependence of Crosstalk in Si-IGBT and SiC Power Modules," *Transactions on Industrial Electronics,* vol. 63, pp. 849-863, 2016.
[43] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. D. Doncker, *Semiconductor Power Devices*: Springer.
[44] Z. Wang, X. Shi, L. M. Tolbert, F. Wang, Z. Liang, D. Costinett*, et al.*, "Temperature-Dependent Short-Circuit Capability of Silicon Carbide Power MOSFETs," *IEEE Transactions on Power Electronics,* vol. 31, pp. 1555-1566, 2016.
[45] P. D. Reigosa, F. Iannuzzo, H. Luo, and F. Blaabjerg, "A Short-Circuit Safe Operation Area Identification Criterion for SiC MOSFET Power Modules," *IEEE Transactions on Industry Applications,* vol. 53, pp. 2880-2887, 2017.
[46] C. Ionita, M. Nawaz, K. Ilves, and F. Iannuzzo, "Short-circuit ruggedness assessment of a 1.2 kV/180 A SiC MOSFET power module," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 1982-1987.
[47] L. Stevanovic, B. Rowden, M. Harfman-Todorovic, P. Losee, and A. Bolotnikov, "High Performance SiC MOSFET Module for Industrial Applications," presented at the ISPSD, Praque, 2016.
[48] Y. Shi, R. Xie, L. Wang, Y. Shi, and H. Li, "Switching Characterization and Short-Circuit Protection of 1200 V SiC MOSFET T-Type Module in PV Inverter Application," *Transactions on Industrial Electronics,* vol. 64, pp. 9135-9143, 2017.

[49] D. P. Sadik, J. Colmenares, G. Tolstoy, D. Peftitsis, M. Bakowski, J. Rabkowski, *et al.*, "Short-Circuit Protection Circuits for Silicon-Carbide Power Transistors," *Transactions on Industrial Electronics,* vol. 63, pp. 1995-2004, 2016.
[50] I. Rectifier, "Paralleling Power MOSFETs."
[51] J. Hanckock, F. Stueckler, and E. Vecino, "CoolMOS™ C7: Mastering the Ar t of Quickness," ed: Infineon, 2013.
[52] R. Wu, P. Reigosa, F. Iannuzzo, L. Smirnova, H. Wang, and F. Blaabjerg, "Study on Oscillations During Short Circuit of MW-Scale IGBT Power Modules by Means of a 6-kA/1.1-kV Nondestructive Testing System," *Emerging and Selected Topics in Power Electronics,* vol. 3, pp. 756-765, 2015.
[53] H. Y. Long, M. Sweet, and E. Narayanan, "Investigation of Negative Gate Capacitance in MOS-Gated Power Devices," *Transactions on Electronic Devices,* vol. 59, pp. 3464-3469, 2012.
[54] W. Zhang, Z. Zhang, F. Wang, D. Costinett, L. Tolbert, and B. Blalock, "Common Source Inductance Introduced Self-turn-on in MOSFET Turn-off Transient," in *ECCE*, 2017, pp. 837-842.
[55] "CREE CAS300M17BM2," ed.
[56] J. Zhan, F. Rees, B. Hull, J. Casady, S. Allen, and J. Palmour, "Impact of next-generation 1700V SiC MOSFETs in a 125kW PV converter," presented at the ECCE, 2017.
[57] X. Zhang, Z. Shen, N. Haryani, D. Boroyevich, and R. Burgos, "Ultra-low inductance vertical phase leg design with EMI noise propagation control for enhancement mode GaN transistors," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 1561-1568.
[58] A. Maerz, T. Bertelshofer, R. Horff, and M. M. Bakran, "Requirements of short-circuit detection methods and turn-off for wide band gap semiconductors," in *CIPS 2016; 9th International Conference on Integrated Power Electronics Systems*, 2016, pp. 1-6.
[59] I. Omura, W. Fichtner, and H. Ohashi, "Oscillation Effects in IGBT's Related to Negative Capacitance Phenomena," *Transactions on Electronic Devices,* vol. 46, pp. 237-244, 1999.
[60] Infineon, "IPZ60R040C7," ed.

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