8-2018

Design Space Evaluation for Resonant and Hard-charged Switched Capacitor Converters

Jordan Alexander Gamble
University of Tennessee, jgamble6@vols.utk.edu

To the Graduate Council:

I am submitting herewith a thesis written by Jordan Alexander Gamble entitled "Design Space Evaluation for Resonant and Hard-charged Switched Capacitor Converters." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Daniel J. Costinett, Major Professor

We have read this thesis and recommend its acceptance:

Benjamin J. Blalock, Leon M. Tolbert

Accepted for the Council:
Dixie L. Thompson

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

Design Space Evaluation for Resonant and Hard-charged Switched Capacitor Converters

A Thesis Presented for the

Master of Science

Degree

The University of Tennessee, Knoxville

Jordan Alexander Gamble

August 2018

christo anesti

Acknowledgments

I would like to thank Dr. Costinett and Dr. Blalock for the opportunity to work on this research project and their guidance throughout. They've both enabled me to grow tremendously as a circuit designer. The generosity of both as well as the department for the DOE WBG Traineeship Fellowship made all of this possible.

I would also like to thank the team at Texas Instruments Knoxville for their valuable feedback and oversight on this project.

Additional gratitude to all of the students in Dr. Costinett's group and CURENT for their collaboration and advice, especially Gabriel who was very patient as I got up to speed on all the work he's done.

I would also like to thank my fiance Natalie for all of her love and support.

Abstract

USB Power Delivery enables a fixed ratio converter to operate over a wider range of output voltages by varying the input voltage. Of the DC/DC step-down converters powered from this type of USB, the hard-charged Switched Capacitor circuit is of interest to industry for its potential high power density. However implementation can be limited by circuit efficiency. In fully resonant mode, the efficiency can be improved while also enabling current regulation. This expands the possible applications into battery chargers and eliminates the need for a two-stage converter.

In this work, the trade-off in power loss and area between the hard-charged and fully resonant switched capacitor circuit is explored using a technique that remains agnostic to inductor technology. The loss model for each converter is presented as well as discussion on the restrained design space due to parasitics in the passive components. The results are validated experimentally using GaN-based prototype converters and the respective design spaces are analyzed.

Table of Contents

List of Tables

List of Figures

Chapter 1

Introduction

Moore's Law has led to continued scaling of digital integrated circuits and the growth of new applications. Handheld devices in particular are becoming increasingly prevalent and ubiquitous. So too, their capabilities are growing such that more power is required to realize their full functionality as shown in Table 1.1 [1]. Paralleled multi-core processors are also becoming the norm as a way of increasing computational power and maintaining constant power density [2]. Processor power is often limited by trade-offs in efficiency, size, and performance. Consumers demand longer lasting runtime and fast recharging of their devices as battery life is seen as the most important factor in their smartphone buying decision [1]. This problem can be addressed by improving the power efficiency and/or increasing the capacity of the batteries [3, 4, 5, 6, 7, 8].

Table 1.1: Power consumption changes for different functions over two years [1]

Function	2009	2011	% Change
Display	300 mW	900 mW	300%
Peripherals	400 mW	1500 mW	275%
Processor	800 mW	1620 mW	200%
Audio	300 mW	400 mW	30%
RF	1200 mW	1330 mW	11%
Total	3000 mW	5750 mW	92%

The former has been discussed by way of topology selection in [9, 10, 7, 11, 12]. One limitation of commonly used power converters is the inductor. In addition to longer runtime, users desire to reduce weight and size of their devices. In power electronics, the inductor is typically the largest component and can be a limiting factor on volume and form factor. This work looks to respond to the need of the consumer by analyzing the Switched-Capacitor (SC) power converter, which does not utilize an inductor.

A thermal limitation exists for mobile applications since the thickness of a heatsink will add undesirable bulk. To eliminate the need for a heatsink, the maximum temperature rise of the device junction or die in integrated circuits must be limited. It is common to integrate the power stage of silicon devices to reduce volume. Junction to air thermal resistance, Θ_{JA}, represents the ability of a package to dissipate heat from the surface of the die to ambient. It is related to the power loss on the die as

$$\Theta_{JA} = \frac{T_J - T_A}{P_{loss}} \tag{1.1}$$

where T_J and T_A represents the temperature of the die and air respectively. Commercial packages can have thermal resistance values of 30°C/W [13] and it is desirable to keep the temperature rise on the die below 60°C to reduce discomfort to the user while the phone is charging. An easy solution would be to take the power switches out of the chip and use discrete devices. By doing this, better performance devices can be used at the expense of a larger footprint area. However, small size is also a requirement on mobile electronics [14].

Applications for the SC are varied and it has historically been used in low power applications or as charge pumps for integrated circuits. While there is still on-going research for low power applications, higher current circuits have been developed recently in academia and industry [7, 15, 16]. Unlike a charge pump, the SC converter described here is a 2:1 configuration capable of 5 A or greater as shown in the Fig. 1.1. This is a step-down or divider topology whose nominal output voltage is half of the input.

In a 2:1 configuration, architectures such as the Dickson, Fibonacci, and series-parallel can be reduced to the same circuit topology [17].

General benefits of the SC include:

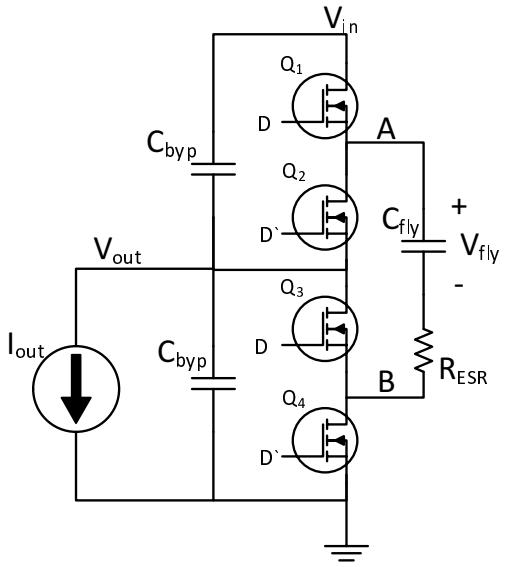
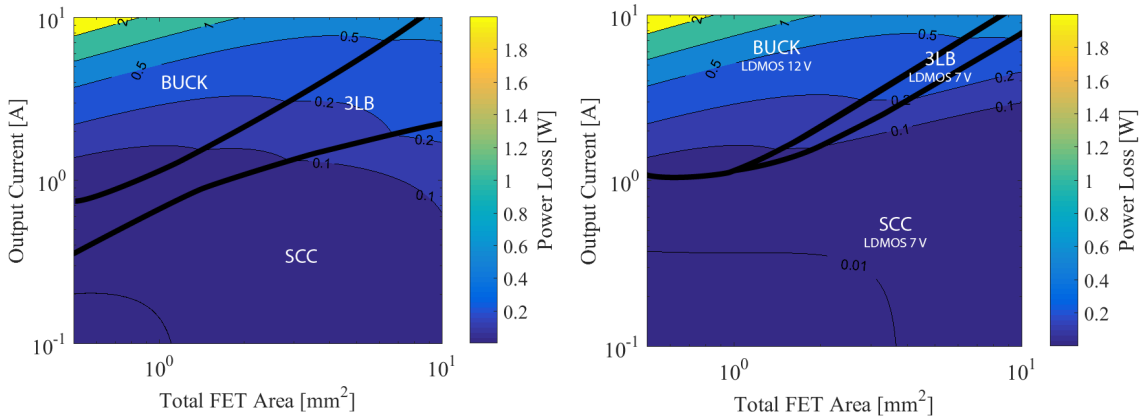


Figure 1.1: Switched capacitor 2:1 converter schematic

- No inductive element. This reduces EMI, bulk, and cost.
- Simple open-loop implementation for use in two-stage topologies
- Device voltage stress is scaled down in cascaded arrangements
- Soft switching and resonant operation with little modification
- Easily integrated with high efficiency
- Increased power density over inductive converter [18]

In [9], the SC is evaluated against the buck and 3-level buck for an integrated battery charger. Two modes of operation occur in relation to the resonant frequency due to parasitic inductance in the layout. Near f_{res} and far, but still in the slow-switching limit. Although lower power loss is achieved near resonant operation, the inductance and control of the resonant frequency is very difficult and not given well to mass production. It is far easier to increase the switching frequency for a more limited performance range. Fig. 1.2([9]) the performance of the SC in these two modes of operation is shown compared to the buck and 3-level buck for 2:1 operation.

Although only outperforming the other two converters at low current, the SC operated near the resonant frequency has a larger range where its power loss is lower than the



(a) SC (far resonance)

(b) SC (near resonance)

Figure 1.2: Comparison of buck, 3-level buck, and SC with 2:1 conversion ratio [14]

competitors. This trend motivates this work to look at the trade-off in hard-switching and resonant operations for the SC.

The buck converter requires switches rated at the input voltage and each conducts the full load current. The Volt-Ampere product serves as a Figure-of-Merit (FOM) and can be very large which results in low efficiency and power device utilization. In SC circuits, devices only block a fraction of the input voltage, depending on the number of levels, while also conducting a fraction of the output current. Not only do they have an improved utilization of switch devices and capacitors, but high efficiency can be maintained over a high conversion ratio [19].

Contemporary applications include voltage supplies for microprocessors, energy harvesting, and data center supplies. In order to improve efficiency over a wide range of input voltages, the SC can be used in a two stage converter, the second stage being either a boost or buck converter, depending on the application. Two stage converters are necessary to overcome the fixed conversion ratio in the SC, as explained in Chapter 2. The need for highly dense and efficient converters can be seen in datacenter energy usage, which in 2010 consumed 2 % of all US usage, which equates to about 80 TWh. As much as half of this is lost to inefficient power conversion, related cooling devices and distribution networks. Since so much money is spent on cooling, improving power loss will minimize cost. A large component of this loss (and volume) are magnetic components, which as stated previously, the SC lacks [20, 21].

Unregulated voltage supplies can experience a decrease in their output as load current increases. Regulation means that the voltage can remain constant under various loading conditions by changing a parameter in the circuit to compensate. This is especially needed where the performance of the load, such as an microprocessor, is affected by minute variations in its bus voltage. Constant current loads, such as battery chargers, allow the output voltage to change while maintaining a fixed current.

One limit of the SC is a lack of current regulation. This results from the SCs biggest advantage of no inductor. Numerous efforts have sought to overcome this limitation by incorporating a small inductor and operating at or near resonance. The inductor employed is typically smaller in value than similarly specified inductor in a buck converter. This variation of the SC is referred to as the Resonant Switched Capacitor (ReSC) converter. A look at how current regulation can be achieved by resonance is explored in further chapters. Voltage regulation of the SC is achieved by varying the switching frequency, which linearly varies the output impedance of the circuit, which is not very efficient.

With current regulation, additional applications can be evaluated such as battery charging and LED drivers. This function is inherent with the buck converter since the inductor is connected directly to the output and it can be operated as a current source.

In all of these cases, the criteria of efficiency and volume reduction inform the design decision, whether the topology be SC or not. There are many variables in designing the optimal SC converter. Previous works have focused on one component such as the flying capacitor, or the bypass capacitor, or the switching frequency. This thesis seeks to combine the many considerations an engineer must consider and distill them into a comprehensive design space, allowing trade-offs to be made as specified by the application. The design space is evaluated in hardware and compared to the derived loss model. The 2:1 SC is considered specifically in the context of a voltage source for integrated circuits, while the ReSC is discussed primarily as a current source for battery chargers.

1.1 Summary

The absence of an inductor and improved FOM compared to the buck converter make high-current step-down SC converters of great interest to research. Even with a small added inductor, the benefits of the SC can be further improved with the ReSC. However, it is not always clear when it makes the most sense to utilize one converter over the other. A review of the literature for applications of the SC and ReSC is presented in Chapter 2. Chapter 3 will detail various practical considerations when designing a discrete SC and ReSC converter. Chapter 4 reviews the literature for analyzing the SC, including developing the loss model. Chapter 5 does the same with the ReSC, with additional focus on current regulation. Chapter 6 presents the design spaces for both converters, quantifying the trade-off in efficiency and area for both converters. Finally, a summary and conclusion on this work is present in Chapter 7 with additional notes for future work.

Chapter 2

Literature Review

The SC circuit is selected for each of the outlined applications for its general benefits as discussed in Chapter 1. A brief overview of the SC and ReSC in the most common applications is presented with discussion on relevance to the analysis found in this thesis. Battery cell balancing and energy harvesting are two applications unlike the others discussed. They both tend to be low power and battery cell balancing uses the SC not as a voltage source, but as a voltage equalizer. However, both applications still design for high-efficiency and contribute to considerations for resonant and quasi-resonant operation. As discussed here, resonant operation of the SC will enable additional usage in areas that require current regulation, such as battery charging.

2.1 Battery Cell Balancing

When charging many battery cells in series, a voltage mismatch can occur between cells. This can be due to any number of reasons including variations in the cell, impedance mismatch in the charging path, age, and temperature affects. This mismatch can limit the charging current of the battery pack and cease charging while some cells have not been fully recharged. To address this problem, battery cell balancing can occur by either dissipating the higher voltage cells (very lossy) or charge shuttling. Redistributing the charge between cells can be an efficient method to equalize the battery pack.

Energy can be stored on a capacitor connected between adjacent cells and switched until the voltage across each cell is equalized. A simplified schematic of this is shown in Fig. 2.1[22]. The efficiency is determined by the ratio of cell voltages [23]. This application makes use of the SC being highly integrated since cell balancing is used in electric vehicles and laptops alike. These limitations, such as low efficiency outside of the 1:1 fixed conversion ratio is less of a concern due to lower power levels and where a popular alternative is resistively dissipating the extra charge.

This is similar to the SC discussed in Chapter 1 as energy is being stored in a flying capacitor and then redistributed. Instead of charge going from input to output as in a traditional voltage converter, the charge is going from cell to cell. The latest efforts for this application are in improving the balancing speed while maintaining high efficiency [24, 25, 26]. In a two-tiered topology, charge transport can be made independent of variations in the components [27]. Quasi-resonance can also be taken advantage of to further improve loss [28]. Operation similar to the ladder method is discussed in this work.

2.2 Energy Harvesting

Embedded and portable electronics continue to experience widespread adoption. While electronics become more complex, battery technology has lagged behind the performance requirements of the user. As a result, power management circuitry must be as efficient

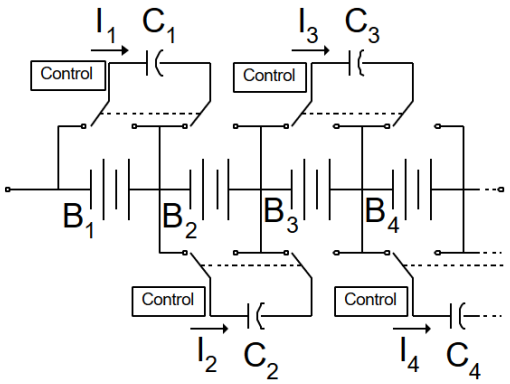


Figure 2.1: Multi cell charge shuttling [22]

as possible to increase usability between charges. So too, electronics such as sensors that can be made small and placed in non-serviceable locations, require battery lifespans of a decade or more. Energy harvesting circuits extract otherwise wasted energy either from the environment or other electronics (for example, RF energy) [29].

The switched capacitor topology used in these types of circuits are also called charge pumps and will be boosting on account of the low ambient energy they typically harvest [30, 31]. The power levels are quite low, tens of mili-Watts [32] at the most but even more frequently in the micro-Watt range [33, 34]. A typical schematic of a doubler charge pump is shown in Fig. 2.2 [29].

This is also known as a series-parallel converter. This is a second example of the SC being restricted to the low power domain due to its limitations. It also shows its advantages, namely no magnetic element, being exploited to make electronics more pervasive. This work seeks to minimize the limitations of the SC for high-current designs while still keeping the magnetic element minimal.

2.3 LED Drivers

Some commercial components using the SC are the LM2792 and LM3354. The LM3354 is for voltage regulation using a proprietary buck-boost architecture. The LM2792 is for current regulation and uses a doubler charge pump to supply a current mirror that performs the regulation [35].

Research efforts have also looked to improve upon the scheme of a charge pump with a regulated current mirror. The drive current in these circuits is low, on the order of tens of miliamps, and takes advantage of the integratability of the switched-capacitor. However,

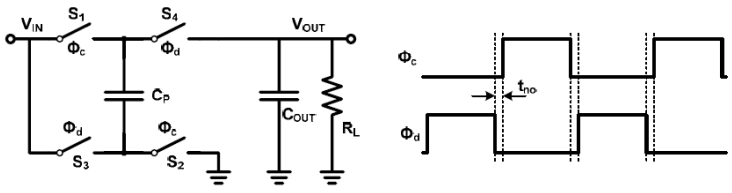


Figure 2.2: A voltage doubler charge pump [29]

.

regulation is achieved by varying the output impedance, by way of varying the switching frequency. This is similar to a linear regulator and the method suffers from the same inefficiency [36, 37].

Commercially, multi-gain charge pumps are used to improve efficiency, since the maximum efficiency occurs at a singular conversion ratio. Depending on the number of parallel LED's, the IC will select the optimum conversion ratio resulting in 90% efficiency and current regulation by way of switching in programmable current sources [38, 39]. These types of IC's provide output current in the tens of miliamps as well. In the market they compete with LDO converters. Since regulation is attained using current mirrors, the output current capability is limited. The commercial devices here show the need for a better solution for high current drivers.

2.4 Battery Charging

2.4.1 The Buck Converter

The buck converter is the most ubiquitous topology for battery charging and voltage supply applications. It is favored for its simplicity, low cost, controllability, and being well-known,. It can be configured to act as either a voltage source or a current source on account of the large output inductor. This is handy when attempting CC-CV charging as only the control scheme needs to change. Soft-switching is also possible in the buck converter and this helps reduce losses, with much research focused in this direction [40, 41].

Integrated solutions [42, 43, 44] tend to lower currents, just an amp or two and maintain efficiency in the low 90 % range. An overview of integrated solutions is covered in [14].

There are numerous guides for designing a buck-based battery charger, such as [45], and no shortage of integrated solutions, such as [46], so those details are not provided here.

2.4.2 Charging batteries with a sine wave

The output current of the ReSC is a rectified sine wave. Since the ReSC is looked at for the possibility of battery charging, the question of how much current ripple can a battery tolerate essential to determining if substantial output capacitance needs to be added.

In electric vehicle (EV) applications, the same question is asked in order to reduce the bulk and heavy electrolytic capacitors at the output of the DC/DC converter. If the battery can be charged with a sine wave, then the capacitors can be eliminated. High temperature is known cause of degradation in every battery chemistry. High ripple current with have a higher rms value than a DC current, even if both charging methods use the same average current. This increase in rms will result in more conduction loss, or I^2R loss in the battery, due to the batteries internal impedance.

It isn't clear if there is any significant degradation to the lifetime of the battery if the rms value for the DC and AC charging scheme are kept the same, especially at high frequency (tens and hundreds of kilohertz). However, for low frequency ripple (120 Hz) there seems to be no significant decrease in capacity (a measure of lifetime degradation), where temperature isn't similarly a cause. In [47] a 16 A average current is used for both DC charging and charging with a 120 Hz sine wave of $LiMn_2O_4$ batteries. The capacity of both batteries under test are degraded by the same factor. The test is performed at a higher than normal temperature as is common in accelerated life testing. Every 200 cycles one battery pack was idle while the other was charging. It is shown that the capacity degradation due to time spent sitting at an elevated temperature while idle, had a larger affect than the action of charging, whether DC or AC. A similar result is found in [48], [49], and in [50] for lead acid, and in [51] for $LiFePO_4$.

In [52] it is also shown based on the physics model of a lithium ion cell that "no effect on either efficiency or charge time should exist as the ac has negligible effect on the concentration of lithium in the electrode particles." This is for DC, Sine, and square wave charging.

There is additional research needed especially at high frequency. In [53] where the ripple frequency reached 14.5 kHz, there was shown a 7.5 % decrease in capacity compared to DC charging and that on the whole, higher frequencies were associated with wider variance in

capacity fade and resistance rise between cells, which can be problematic. Although the exterior temperature of the cells were controlled within two degrees, internal heating cannot be completely ruled out, considering the frequency dependence of the internal impedance. Unfortunately, it isn't shown how many years of performance will be lost with high frequency charging.

When using the ReSC as a battery charger with high ripple current, this gives a point of reference (although still inconclusive) as to whether that ripple will be detrimental. The output capacitance of the ReSC therefore need not be any more (in capacitance and area) than for the buck converter.

2.5 Voltage supplies

Since the highest efficiency for the SC occurs at a fixed conversion ratio, applications that require a single fixed voltage can make use of the SC both regulated and unregulated. An example of the variation in efficiency with output current is shown in Fig. 2.3 for an integrated 2:1 SC. The nominal output voltage is 1.5 V. As the input voltage increases and the conversion ratio is no longer 2:1, the efficiency decreases at a given current.

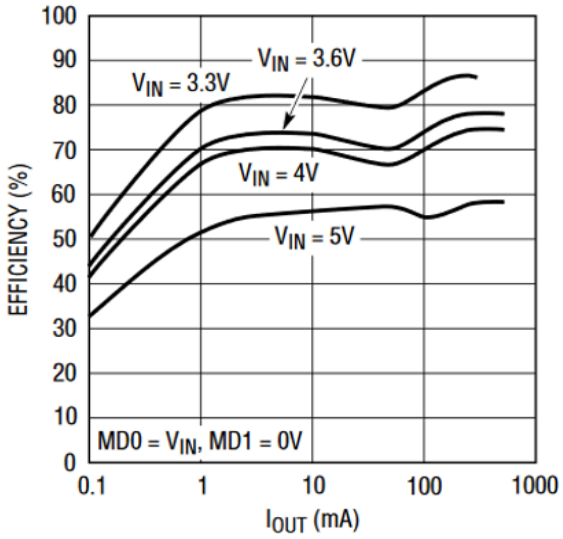


Figure 2.3: Example of the decrease in efficiency for variation in input voltage [54]

.

With commercially higher current capability compared to LED drivers, these also take the form of a automatically variable gain SC and maintain voltage regulation by using a variable current source. These currents are typically in the hundreds of miliamps, [55, 56].

Although there are some caveats to the SC as a voltage supply, the absence of an inductor is an overriding motivation for development of high-current converters. An 8-level Dickson SC is evaluated in [19], operated in FSL for a 12 V to 1.5 V point-of-load (PoL) application. The design uses 0.18μm CMOS and its performance is heavily limited by the bond wire and metalization that results from integration, similar to [9]. The PCB area is reduced by one-third compared to a similarly rated buck. The difficulty in obtaining highly efficient SC converters at high current in CMOS has motivated this work to use discrete components that can be later integrated as processes improve.

2.5.1 Variable Conversion Ratio

A fixed conversion ratio prevents the widespread adoption of the SC. One method of overcoming this limitations is by designing several fixed ratio converters and then switching them into the circuit to improve efficiency. With a gain stage of 1, 0.5, and 0.33, for example a SC converter can maintain decent efficiency over a wider range of input voltages. A block diagram is shown in Fig. 2.4 with the improvement in efficiency shown in Fig. 2.5.

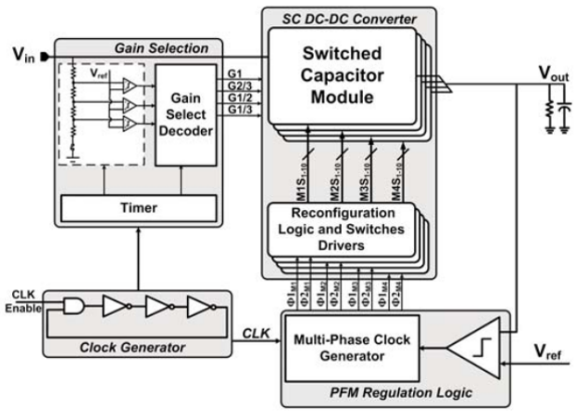


Figure 2.4: Example of multiple discrete conversions ratios used to improve efficiency [57]

.

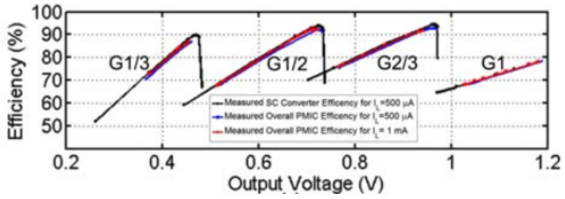


Figure 2.5: Efficiency improvement over output voltage with multi-gain converter [57]

.

A similar implementation can be made by reconfiguring the switches and flying capacitances to provide multiple gains. These will still be fixed gains, but there is more flexibility in optimizing the gain for efficiency [58]. Since multiple converters are still being implemented, the area reduction compared to a buck converter is limited as more area must be allocated for additional switches and capacitors that may not be used regularly. The ideal solution would be to have a single converter with multiple gains, or to move the output regulation to another pre-existent circuit in the system, as is discussed in subsection 2.6.

2.5.2 Two-stage converters

To compensate for the limitations of the unregulated SC, a second stage can be added in a merged or cascaded form as in [59, 60]. Losses will occur in both stages, decreasing overall efficiency and increasing converter size as both stages are rated for the same power. Fig. 2.6([59]) shows a typical example where a fixed ratio step-down SC operating in SSL is loaded with a high frequency buck converter. The step-down action of the SC reduces the conversion ratio of the buck, improving its efficiency, and the buck can provided traditional voltage and current regulation.

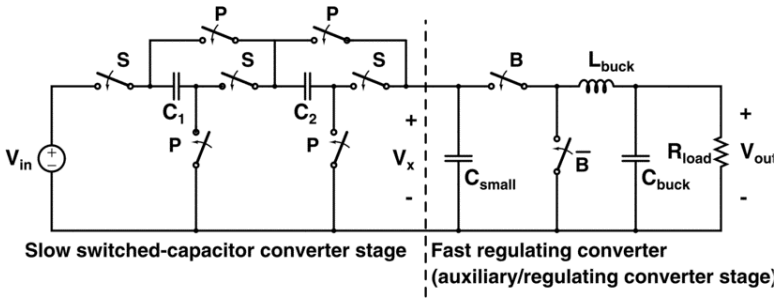


Figure 2.6: Example of a SC step-down stage with a secondary regulating stage [59]

.

The SC and buck converter can also be combined into a single stage, where the high-side device is shared between the two converters, as illustrated in Fig. 2.7([61]).

Here an additional input inductor is added to smooth the input current ripple due to the SC. Although there is improvement over the quadratic buck, the design still has limited regulation bandwidth. Additionally, compared to the 2:1 SC, there is one additional semiconductor device. Both of these techniques cascade the inefficiency and it is desired to have a single stage, single converter where regulation is possible. This is investigated in the ReSC in Chapter 5.

2.6 USB Power Delivery

Universal Serial Bus (USB) was originally optimized for fast data communications and the first specification for power delivery occurred as recently as 2010 when the standard was increased from 4.5 W to 7.5 W. Prior to this, USB power was only meant to power peripheral devices. In 2012 the USB Power Delivery (USB-PD) specification raised the maximum allowable power transfer to 100 W. Additionally power can be bidirectional and is managed intelligently at the system level for improved performance. The new specification divides power sources into profiles as outline in Table 2.1([62])

The default profile is selected and if the connected charger is compatible with higher input voltages and currents, a negotiation takes place and the best profile is selected for fast charging. The adapter side of the USB cable is typically the output of a flyback converter and high current is made possible by the addition of 18 pins compared to the previous 4

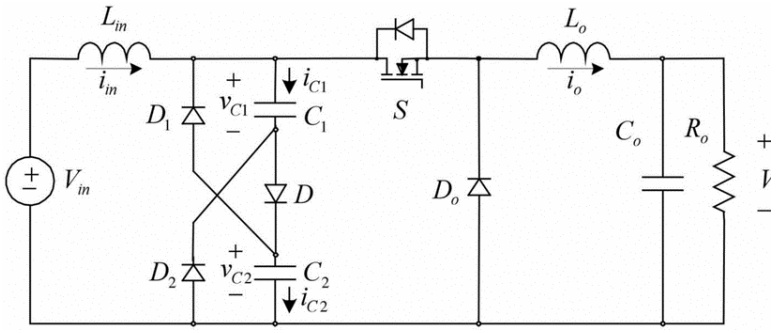


Figure 2.7: Example of a combined SC and buck converter into a single stage [61]

.

Table 2.1: Power source profiles for USB-PD [62]

Profile	Power Rating
1 (default)	10 W (5 V @ 2 A)
2	18 W (5 V @ 2 A → 12 V @ 1.5 A)
3	36 W (5 V @ 2 A → 12 V @ 3 A)
4	60 W (5 V @ 2 A → 20 V @ 3 A)
5	100 W (5 V @ 2 A → 20 V @ 5 A)

used in earlier USB models. The block diagram for this type of configuration is shown in Fig. 2.8([63]). The USB voltage and current is adjustable in a linear fashion as illustrated in Fig. 2.9([64]).

This adaptive power charging is made possible by the communication between the adapter, the charger proper, and the Power Management IC (PMIC). Completely programmable, this technique opens the possibility of adjustable input voltages for further design freedom in designing high-efficiency chargers, as explored in [9, 65]. The adapter will need finer resolution in regulating the input for the SC then it would for the ReSC. This is because the SC is fixed 2:1 and the efficiency deteriorates when the ratio is even 5 % off. The ReSC can use its own regulation such that a coarse-grain resolution is used on the adapter side and the finer resolution is from ReSC.

Detailed and complex battery models are not necessary for the charging process. An equivalent model of simply the open-circuit voltage and a series resistor is sufficient. The series resistance adds an extra voltage drop during charging. This will cause the charger to enter the constant-voltage (CV) phase earlier and as a result increase charging time. This can be compensated for by applying two different currents during constant-current charging to calculate the voltage drop using Ohm's Law [14].

One example of a commercially available high-current SC charger for USB-PD charging is the bq25970 from Texas Instruments. It uses a two-phase 2:1 ladder topology and is capable up to 8 A. It is typically used in conjunction with another integrated charger such as the bq25890 to perform the full charging cycle, specifically the trickle, precharge, taper charge, and termination. A typical set-up is shown in Fig. 2.10([66])

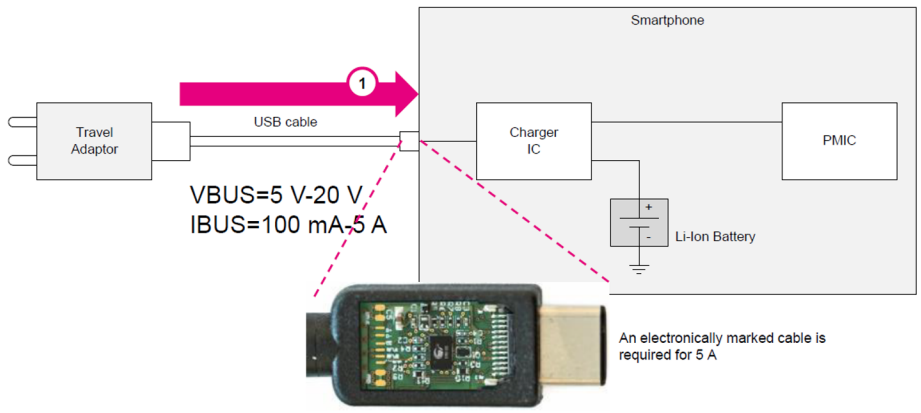


Figure 2.8: USB-PD typical block diagram [63]

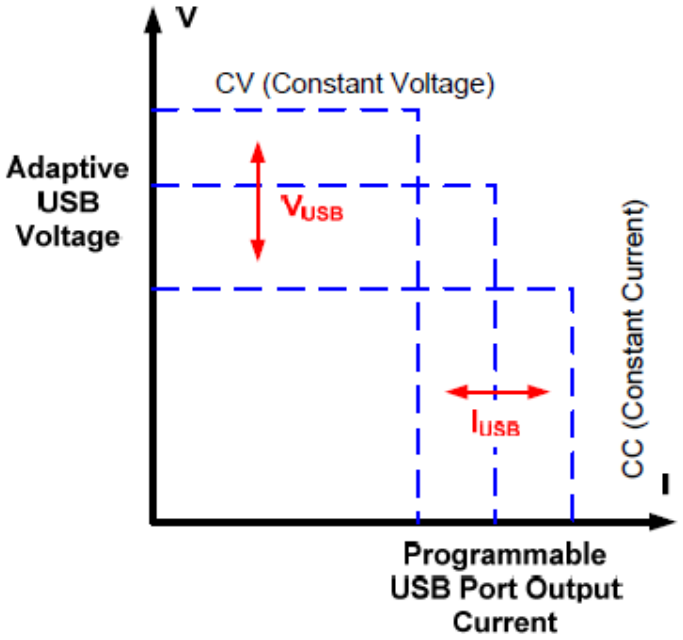


Figure 2.9: USB-PD adaptive voltage and current [64]

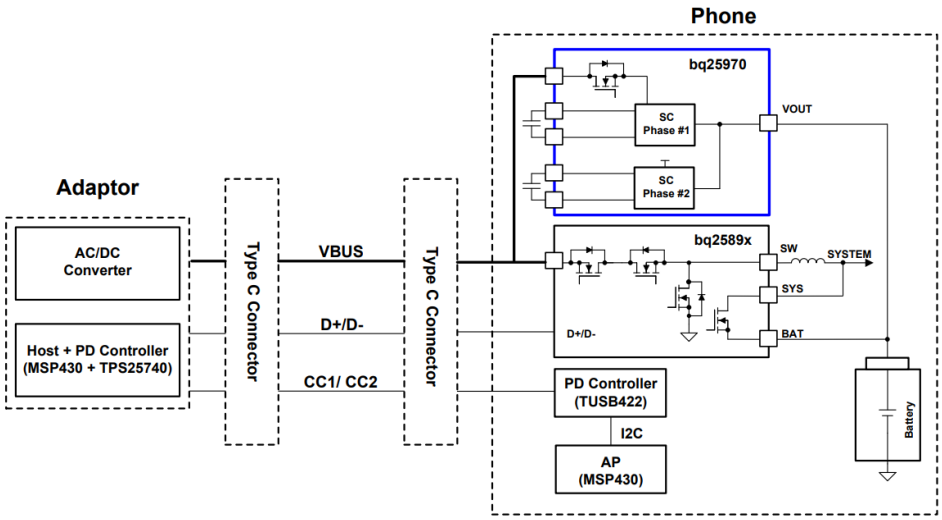


Figure 2.10: Application schematic for the bq25970 [66]

The bq2589x is a buck type regulator in parallel with the SC. It seems that both current and voltage regulation is possible, but the specific control scheme used is not detailed. Fig. 2.11([67]) specifies which device is the dominate active device during the various stages of charging.

It is interesting to note that the bq25970 is used in both CC and CV modes. At 8 A, the IC power loss is 1.4 W and capable of charging a 3200-mAh battery to 80 % in about 33 minutes. The efficiency curve for various charging currents is provided in Fig. 2.12 [66].

The efficiency of a SC will increase with switching frequency as the voltage difference between the capacitors decreases. The plot above shows the efficiency decreasing with switching frequency, and assuming slow-switching operation, indicates that the frequency dependent losses are from the FET's and not the topology being hard-charged, which it most certainly is. That is to say, the MOSFETs were optimized for low conduction loss. The flying capacitance used is 4x 22 μF.

A second commercially available SC voltage supply is the DA9313 from Dialog Semiconductor. It has a rated output current of 10 A and similarly uses the dual phase 2:1 interleaved ladder topology. Not marketed as a battery charger, it produces an unregulated output voltage using slow-switching operation with a default frequency at 500 kHz. The

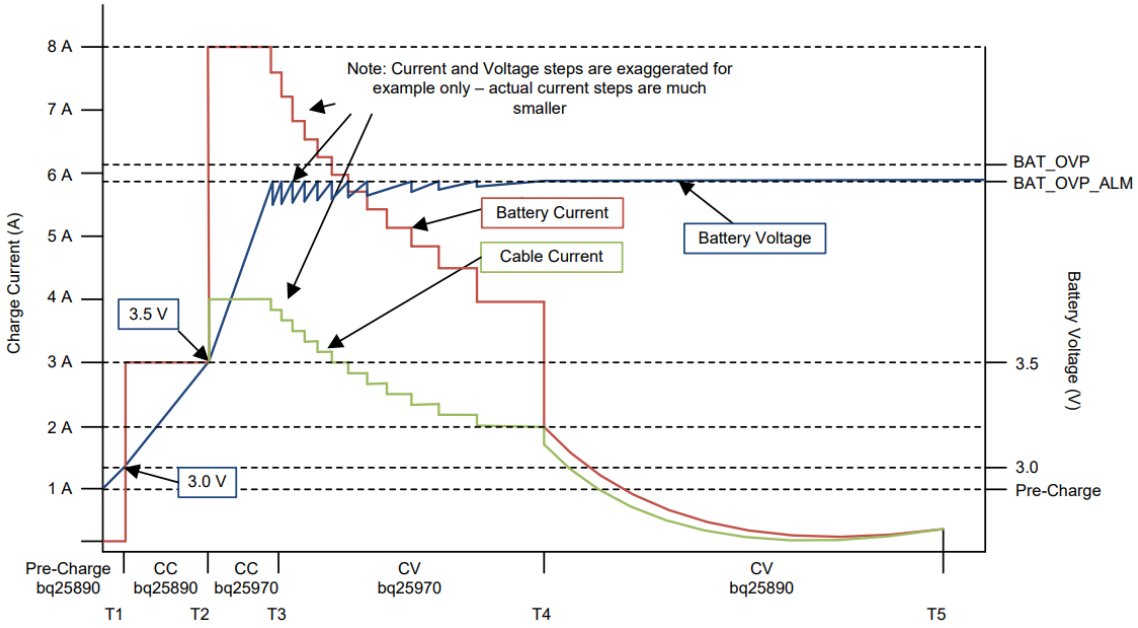


Figure 2.11: Ideal Charge Cycle Operation for a typical application of the bq25970 [67]

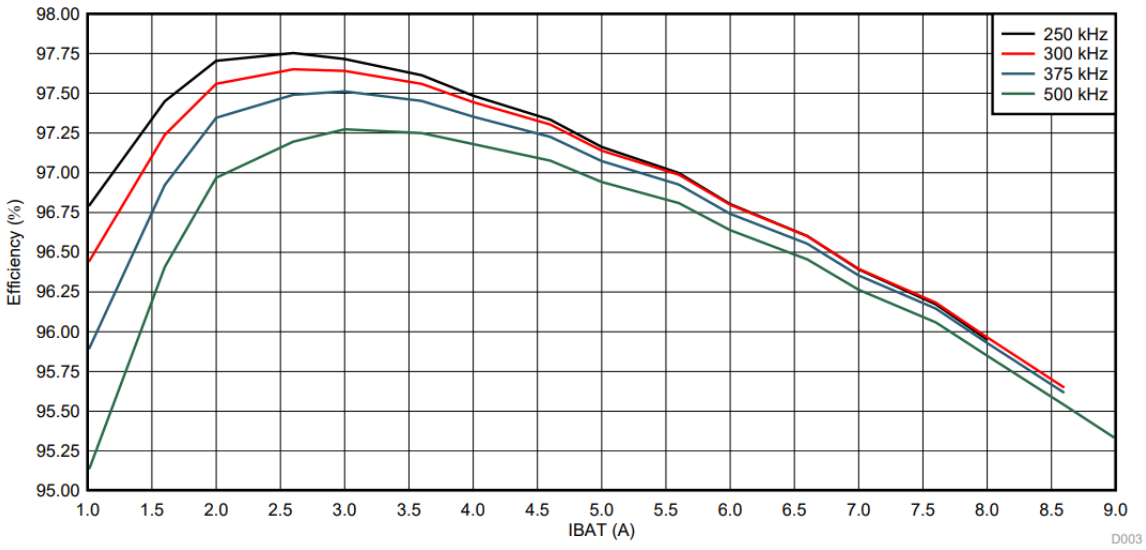


Figure 2.12: Efficiency curve of the bq25970 [66]

switching frequency is varied automatically to improve light load efficiency by entering what is termed discontinuous conduction mode but is really a pulse skipping scheme. The flying capacitance used is 2x 47 μF. The block diagram is shown in Fig. 2.13([15]), and the efficiency curve for various input voltages is shown in Fig. 2.14([15]).

Both the TI and dialog devices allow paralleling. Of note here are the two different design strategies for using the SC as a voltage supply. For TI, two converters are needed in parallel, in part to provide charging capability for incompatible USB protocols. This adds some redundancy which can be both a benefit and a hindrance. The Dialog strategy is to produce an unregulated output with very good performance, in the two-stage configuration discussed previously.

2.7 SC Optimization

Previous work on optimizing the SC converter has focused on area and efficiency optimization. This is typically taken as integrating the switches and the flying capacitor, but discrete capacitors have been considered as well [16]. Area optimization for the bypass capacitors is also considered in [68].

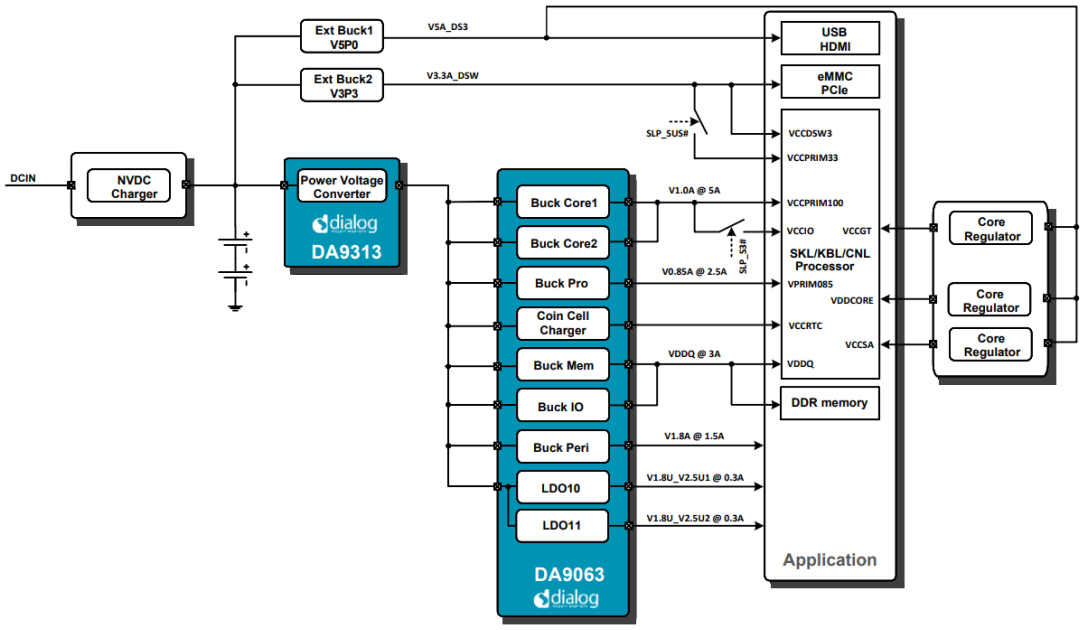


Figure 2.13: Block diagram of the DA9313 [15]

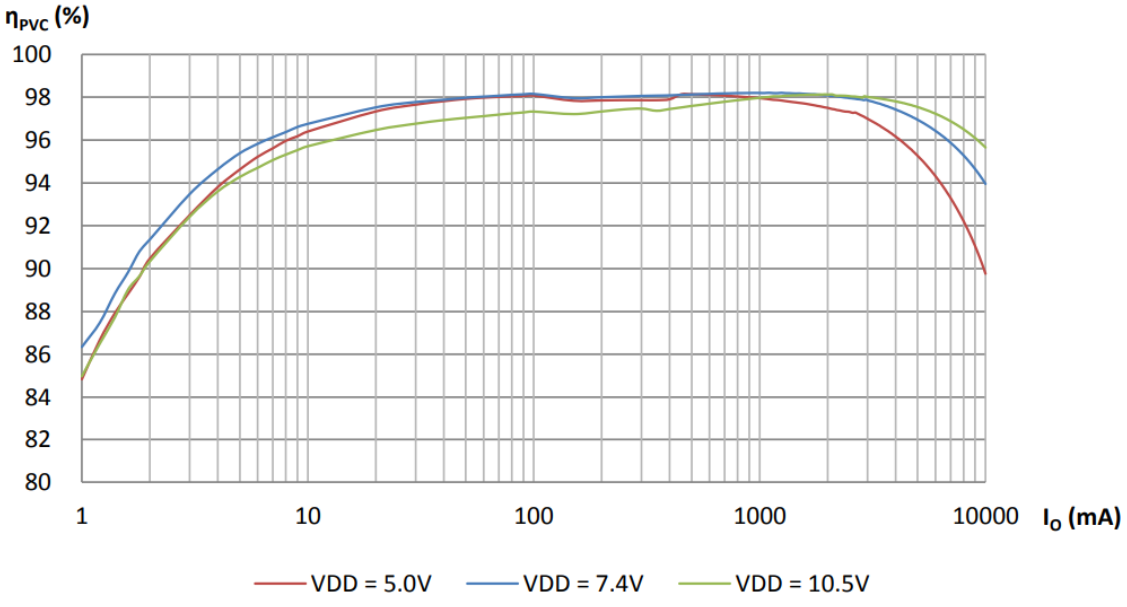


Figure 2.14: Efficiency curve of the DA9313 [15]

The standard approach is to independently optimize the area for the capacitor based on the energy density and then the area for the switches based on the on-resistance. Finally optimizing the entire system is done by finding the switching frequency that results in the highest efficiency [69, 70]. The power loss typically also contains the gate drive loss and bottom plate capacitance loss since the assumption is integration [71]. The optimal solution is found numerically and varies on the assumptions and loss mechanisms included.

The output impedance affects the amount of "droop" or IR loss that occurs. A higher output impedance will have a higher voltage drop for a given current. This voltage drop is subtracted from the nominal, unloaded output voltage. Since the IR drop is proportional to the current, at high load the voltage will "droop" or decrease. The energy lost as a result of droop is dissipated in the converter. This is illustrated in the LTC3251, an integrated 2:1 SC converter in Fig. 2.15.

Applications such as VRM power supplies have a restriction on the droop such that the processor does not go into under-voltage lockout. For the SC, voltage regulation focuses on compensating for the voltage droop, as the input voltage is considered constant. Optimization techniques include the effects and regulation of droop, including frequency and switch area modulation, which adds to their complexity [16, 72, 73, 74]. Table 2.2

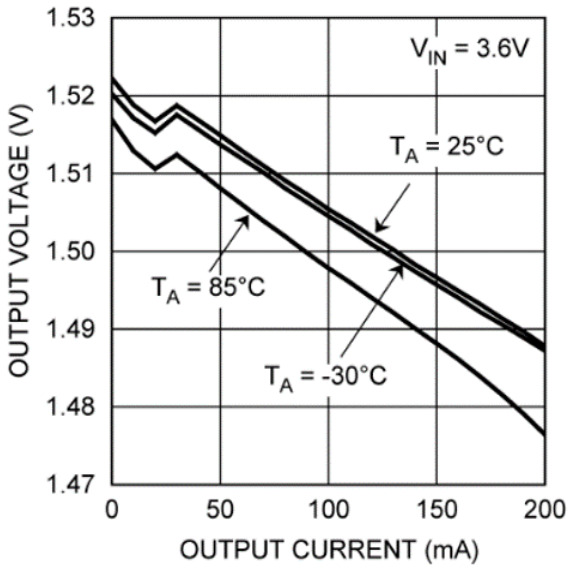


Figure 2.15: Example of droop in a SC circuit [54]

.

summarizes the optimization considerations discussed here. All sources use the three steps of optimization as explained previously, with specific techniques for droop control indicated.

As to the best of the author's knowledge their has not been an optimization that considers both discrete switches and capacitance. Similarly, paralleling flying capacitance to lower ESR has not been optimized against PCB area.

Soft-switching techniques for the SC capacitor has been extensively reviewed in [2] where an external inductor is placed at the output of the converter, either as a stand-alone or with a two-stage converter. Soft-charging essentially reduces the in-rush current spike due to charge-sharing while maintaining the same average current. This is accomplished by taking advantage of an inductors inability to conduct discontinuous current. This is in contrast to resonant operation, where the inductor current is sinusoidal, or a rectified sine wave. In the two-stage converter, more complex control is required to maintain a wide-range of stability. Since soft-charging requires that their be no mismatch between flying capacitors, for multi-level converters, the optimization technique in [2] looks at the feasibility of using soft-charging. Here we focus on the 2:1 ladder topology in either hard-charging or fully resonant.

2.8 ReSC Optimization

Optimization of ReSC circuits follow a similar approach as for the SC. The energy density of the flying capacitor is optimized for lowest loss along with the size of the FETs, assuming integrated devices. The inductor is evaluated with constant-volume scaling, deriving expressions that reduce power loss as a function of scaled loss mechanisms. Both analyses

Table 2.2: Summary of optimization techniques

Reference	Droop technique
[16, 68, 69, 70]	-
[16, 72]	FET conduction by varying gate voltage
[73, 74]	FET width selection

are then combined into a figure-of-merit (FOM) for comparison against variations of the SC for both energy and area constraints [75]. Area allotted for the flying and bypass capacitors is indirectly analyzed in [76] where minimum capacitance for minimum ripple is considered.

For power density optimization of the resonator, particle swarm optimization is performed on the total ESR of the capacitor and inductor, assuming a fixed volume. A resonator is also referred to as a "tank", which is an inductor and capacitor (either in series or parallel) operating at the resonant frequency. The capacitors evaluated have a high energy density, due in part to their high voltage rating, which is also associated with low ESR. The analysis did show that a low-loss resonator can be developed using commercial discrete capacitors, although since the power density is associated with the voltage rating, the application for low voltage converters is limited [77].

Interleaving phases in the ReSC can help reduce voltage ripple and reduce component size and count at the output, similar to a multi-phase buck. In this type of optimization, the size of the resonant components are evaluated with number of phases and it is shown that, for the same area, the interleaved ReSC can have an improved efficiency of 0.5 % [78, 79, 80].

Using the parasitic loop inductance has been investigated for the ReSC in very high power applications such as [81] where the connections between various components are long on account of voltage isolation. For low-voltage applications where every component can be very near to one another, the inductance due to layout will have insufficient quality factor, as explained in later chapters.

Modeling accurate inductor losses and size across various technologies is very difficult. This work will show that the analysis can be simplified to an equivalent resistance against which existing inductors can be evaluated to inform quick design choices.

The output voltage of the ReSC can be controlled in a similar fashion to that typically ascribed to the SC [82]. However, this method of changing the output impedance by varying the switching frequency results in a loss of ZCS and increased power loss. Many other control schemes have been proposed that incorporate additional switching states, including the two states discussed in this work. Typically, ZCS will be lost but ZVS will be gained; significant in higher voltage converters [83, 84, 85, 86]. An additional phase shift, which is either a phase shift between interleaved phases or a phase shift introduced by using more switching

states in the 2:1 ladder, can be used to control the charging current in the capacitor. Either the phase shift or the switching frequency can be modulated [87].

Here, two methods are analyzed, each with one additional switching state. The method of shorting the tank, which is included in [87, 83, 84, 85] is also the only additional switching state in [88]. The comparison between this work and [88] is not direct since the converters are topologically identical but behaviorally different. In [89] the dynamic off time modulation method (DOTM) is used to split the off-time between the charging phase of the flying capacitor and the discharging phase. For the direct ReSC, this is only appropriate at light load since the rms current will be larger [90], whereas for the indirect this is not case [78]. In [78] the method is used for improved light load ability and voltage regulation by modulating R_{eff}. No matter the method, the goal has been to regulate the output voltage over varying load conditions. This work investigates using a method similar to DOTM for regulating the output current, as the output voltage can be regulated by changing the input voltage in USB-PD systems.

Table 2.3 summarizes the combination of states used for voltage regulation with the numbered states in Fig. 2.16. The details of the first two states used for basic operation are detailed in Chapter 5 as well as states 3 and 4 as they relate to current regulation.

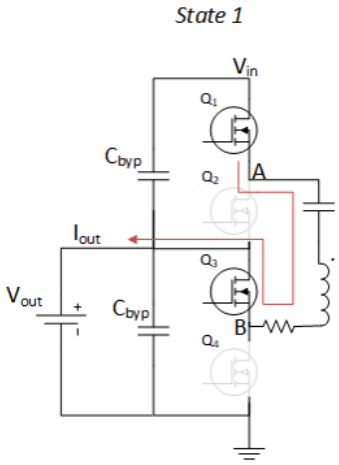
Table 2.3: Summary of regulation techniques

Reference	States	Objective
[83]	1,2	Lose ZCS, gain ZVS
[85]	1,2,3,4	Lose ZCS, gain ZVS
[84, 87]	1,2,3	Lose ZCS, gain ZVS
[88]	1,2,3	Lose ZCS, gain ZVS
[78]	1,2,4	Efficiency improvement at light load

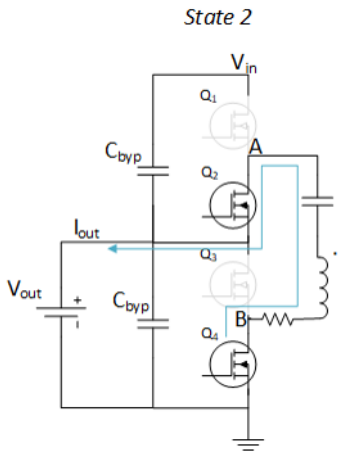
2.9 Summary

This literature review covers some selected applications of the SC and ReSC and the context in which they are considered in later chapters. The SC has been used for low-current applications and does not lend itself well to constant current methods used in LED drivers and battery chargers. When regulation is necessary, it is typically used in a two-stage converter with the second stage being a buck as the large output inductor can be used as a current source. However, for unregulated applications (as the efficiency of the voltage controlled SC can be very poor) it can be an improvement over the buck due to its high integrability and more effective utilization of passive components. The ReSC has the potential to provide current regulation with a comparatively smaller inductor than the buck. USB-PD also adds a new degree of freedom as the input voltage can be easily adjusted for fixed-ratio converters.

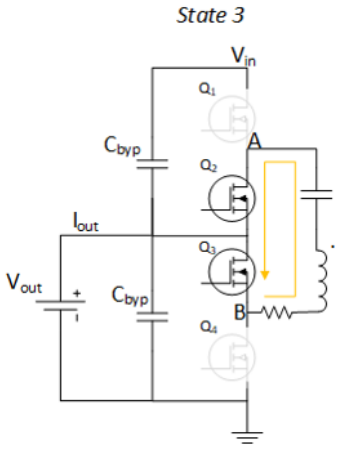
Due to their high integrability, the SC and ReSC have been optimized considering FET area and flying capacitor real estate. A simple analysis between the two converters for a discrete solution is presented in this work, focusing on when it makes sense to use one over the other.



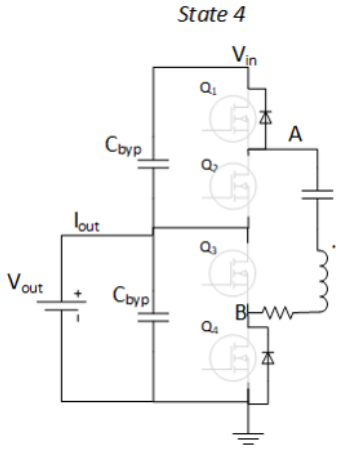
(a) First switching state of the ReSC in the first half resonant period



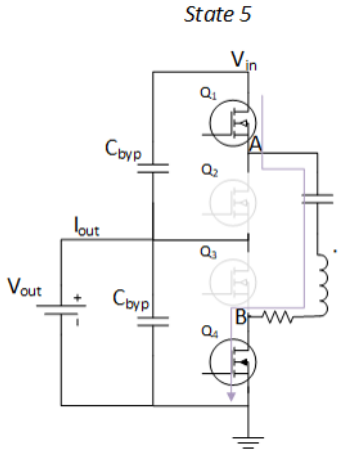
(b) Second switching state of the ReSC in the second half resonant period



(c) Additional switching state (3) by shorting the tank



(d) Additional switching state (4) by opening the tank



(e) Additional switching state (5) by turning on the top and bottom device

Figure 2.16: Basic and additional switching states to affect regulation in the ReSC

Chapter 3

Practical Limitations

The design of any power converter requires consideration of the real-world affects that are typically neglected in the design phase for the sake of simplicity. Some considerations and their affects on the converter are applications specific, while others tend to be universal. For the SC and ReSC, the flying capacitor is one of the central components that must be analyzed for predictable behavior. This chapter presents an analysis of the parasitic elements of capacitors and layout that can be a large influence on the operation of these two converters. It is crucial to cover these topics as they affect the design space later developed in this work. High-frequency operation and inductors are also covered in this chapter to make a case for the discrete design considered in this work. Complete optimization of the switching devices is not developed but a first order improvement is made by looking at Gallium Nitride (GaN) devices.

Although the design space is intended to be application agnostic, a specific use for the two topologies was considered, namely battery charging. The objective is to develop an integrated battery charger with higher current and efficiency than the BQ24190 (buck converter) from Texas Instruments. For this reason the output voltage is assumed to be 4 V and so for the 2:1 converter, the input voltage is 8 V.

3.1 GaN

Low voltage GaN devices will have a better figure of merit (FOM) (on-resistance * gate-source capacitance) than similarly rated silicon MOSFET devices [91]. This FOM captures the tradeoff that occurs in MOSFETs where a low on-state resistance is achieved by making the device wider, which in turn increases the capacitance due to the gate. Low on-resistance will provide low conduction loss, and low capacitance will provide low switching loss. Since a high current design will be limited by conduction loss, it may be advantageous to use lower R_{ds-on} devices. However, this will come at the cost of increased switching loss, and since the output impedance of the SC favors high frequency, GaN serves as a better alternative. The FOM for several commercially available 8 V and 12 V Si MOSFETS are shown compared to three devices from Efficient Power Conversion (EPC) in Fig. 3.1.

The GaN devices have a far superior FOM compared to the silicon devices. The conduction loss for the same devices are plotted in Fig. 3.2, in the range of interest for this work.

All but the EPC2040 outperform Si in conduction loss, but since the R_{ds-on} can be made arbitrarily lower than GaN while also increasing the switching loss due to the increased capacitance in widening the device, the gate drive and C_{oss} losses are plotted in Fig. 3.3. It is assumed that all devices are driven with 5 V and block 4 V. The C_{oss} is also known as the output capacitance that is charged and discharged as the device turns off and on,

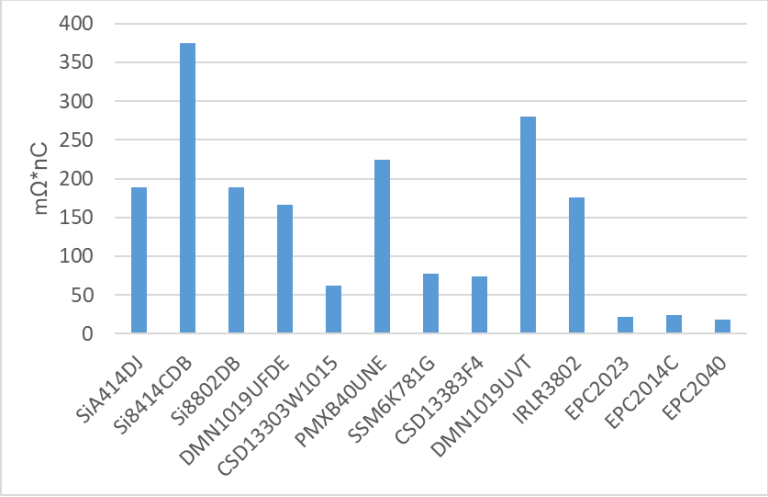


Figure 3.1: Figure of Merit for low voltage MOSFETS and EPC-GaN

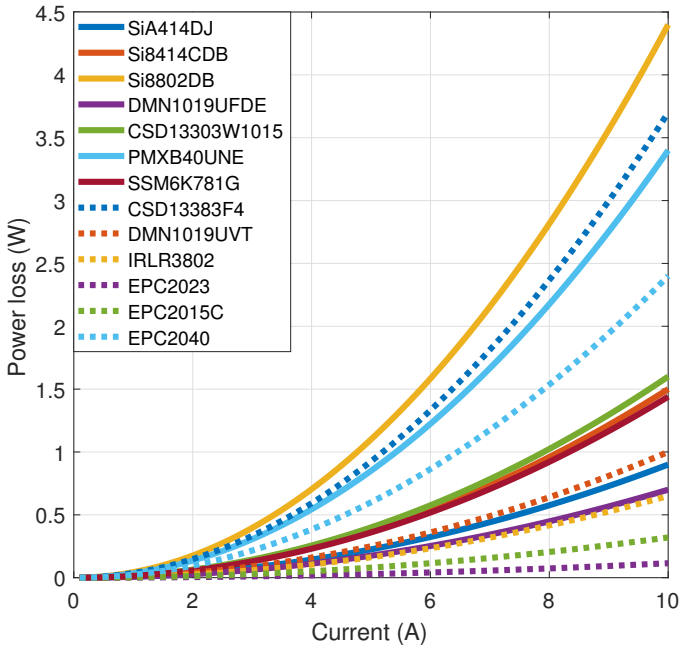


Figure 3.2: Conduction loss for low voltage MOSFETS and EPC-GaN. $V_{out} = 4$ V, $V_{GS} = 5$ V

respectively. The energy used to charge this capacitor is lost during hard-switching and can become dominant at very high frequency.

Here, all but the EPC2015C device outperform the Si devices. This does not indicate that this device is a poor choice, but rather, along with the EPC2040, demonstrates the tradeoff between achieving low on-state resistance and low input capacitance. This work is concerned with the high output impedance of the SC and ReSC and the on-resistance will certainly impact this. High switching frequency is also desired to lower this impedance. Physical size is also a concern. GaN offers an acceptable compromise as illustrated by the FOM and the reduction in physical size compared to a similarly rated silcon device is a materials property [92]. For this work the EPC2015C is chosen.

3.2 Integrated Inductors

A benefit of the SC is that it has no inductor to integrate and high quality capacitors can be implemented in todays CMOS technology. Efforts have been made to integrate inductors

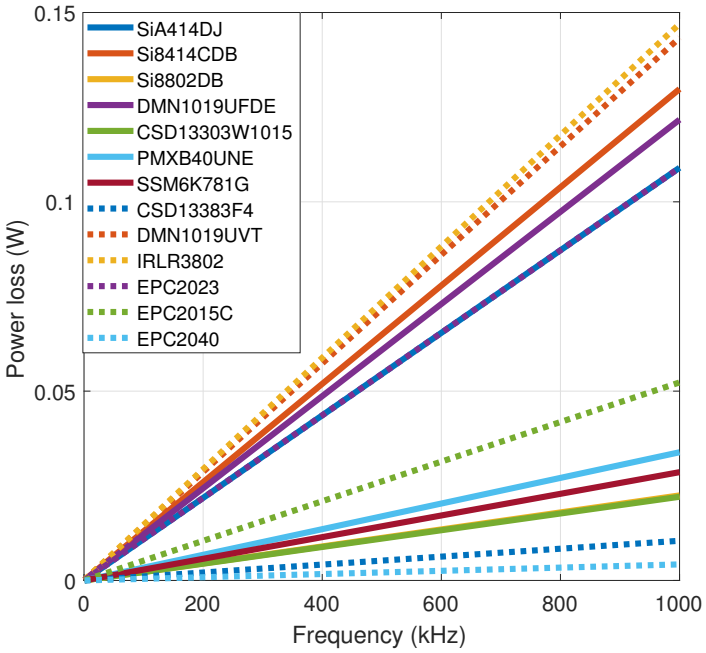


Figure 3.3: Switching loss for low voltage MOSFETS and EPC-GaN. V_{out} = 4 V, V_{DS-off} = 4 V

on chip, but their quality factors are quite poor unless using novel materials. The use of integrated inductors whether on chip or PCB can be prohibitive due to cost, access, and turn time [93, 94].

There has been some investigation into using air-core inductors, as they do not have any core loss and could be achieved with wire bonds, reducing complexity. The general approach to using wire bonds is first to reduce the inductance required, which means increasing the switching frequency. Inductance is proportional to the number of windings and the size of the core, which results in a physical size many times the size of the integrated switches and gate drivers. With an air-core inductor, even more windings are needed to achieve a modest inductance. These extra windings will increase the conduction loss.

Multi-phase converters such as the buck can also be used to reduce the output voltage ripple. By distributing the output current into many phases, the inductance of each phase can be further reduced. For the multiphase buck, the inductance can be reduced by n-times, where n is the number of phases [95]. Negatively-coupled, interleaved buck converters can also be used to realize reduced inductance requirements [96, 97].

Adding windings to an integrated air core inductor will also increase cost and complexity, as well as introducing a trade-off between high quality factor and area. It is non-trivial to bend a bond wire into a coil, so for windings greater than one, other geometric shapes are used to approximate a coil. Although an octagon more closely resembles a coil than an equilateral triangle, the latter will has fewer corners. The corners are the joints where two bond wires come together and are soldered to a copper pad the fewer the corners. the lower the ESR [98].

A bond-wire has been investigated for use as a single turn air core inductor. However, for a 1-mil diameter bond-wire, the rule of thumb for inductance is about 1 nH/mm. Increasing the diameter and using copper (which has a lower resistivity than less expensive aluminum) can help and a trade-off can be made.

For example, a 5-phase 10 A buck converter with 100% current ripple would require a per phase inductance of 0.85 nH at 120 MHz. According to Fig. 3.4 for a 4 mil copper bond wire, the $DCR = 3$ mΩ and the $ACR = 13$ mΩ resulting in 64 mW of loss. The *quality factor, Q* of an inductor is a measure of ratio of energy stored in the inductor to the energy lost per switching cycle. For this example, the Q is 40, which is very good, but the since the bond wire would be inside the package filled with epoxy, and the total loss due to the inductors is 320 mW, the heat could be damaging.

Switching losses are proportional to switching frequency. The gate drive losses are a function of the total gate charge of the MOSFET, which is made larger to reduce on-resistance. Power loss due to the gate drive current will also increase with input and miller capacitance. In the 120 MHz range these losses will violate the thermal requirement outlined in Chapter 1, as well as increase the die area for internal signal generation. External signal generation (pulses fed into the gate driver) will have propagation delays due to parasitics on the same order as the switching period.

Other attempts have looked at using a PCB trace just under the IC to implement the inductor as shown in Fig. 3.5 ([79]). It consists of three parallel inductors, each fabricated by two vias and a copper trace.

This has the benefit of keeping converter area small, but puts the burden on the PCB engineer in assuring the width, length and general placement is adequate. In [79], the

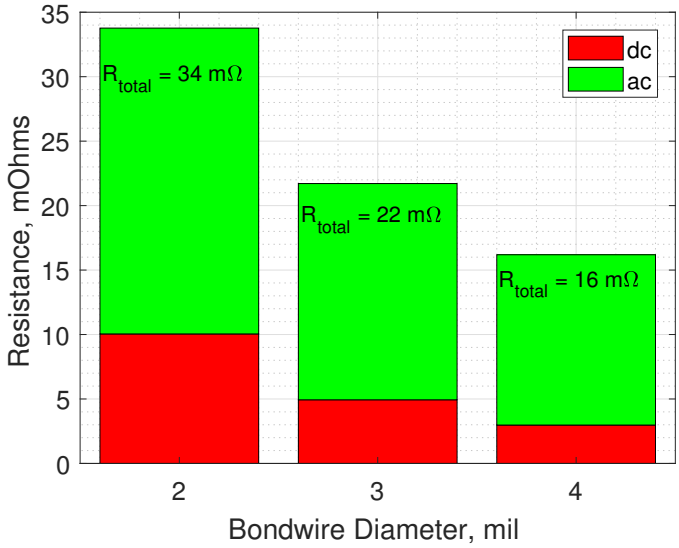


Figure 3.4: Total resistance in single turn bond wires of various diameter at 120 MHz

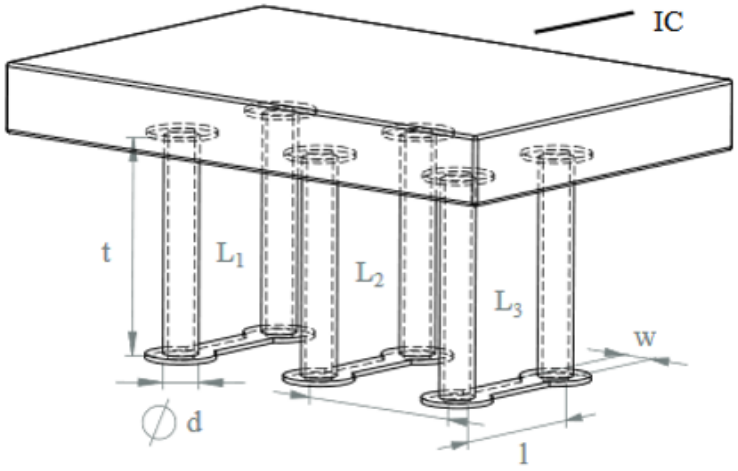


Figure 3.5: Drawing of a three-phase PCB inductor structure [79]

structure is used up to 1.2 A for an interleaved ReSC converter. As part of our own analysis, the inductance and resistance of several PCB traces are plotted in Fig. 3.6. A 5 mil trace is used as reference for the thinnest trace Advanced Circuits will make using their standard process. Widths of 55 mils and 85 mils are used for temperature rises of 50 °C and 25 °C, respectively at 10 A.

The inductance is still less than 10 nH which can make achieving the high-Q needed for the ReSC difficult. At 5 MHz (the frequency at which the inductance was determined using Q3D), the Q of the 55 mil trace (300 mil long) with a 25-mil via is 30, however considering the practical circuit in Table 5.1, the Q becomes 4.3. The resistance of the via should also be considered and is plotted with inductance in Fig. 3.7 using FEA software Q3D.

The via radius is swept for a 4-layer PCB. The parameters do not vary much but are comparable to the PCB trace, considering 2 vias are used. A 4-layer PCB was fabricated as shown in Fig. 3.8 to measure the DC resistance of the via-trace-via structure.

The DCR is determined by performing V-I measurements across the inductor . That is, a current source is applied and a kelvin voltage measured. This is performed three times at

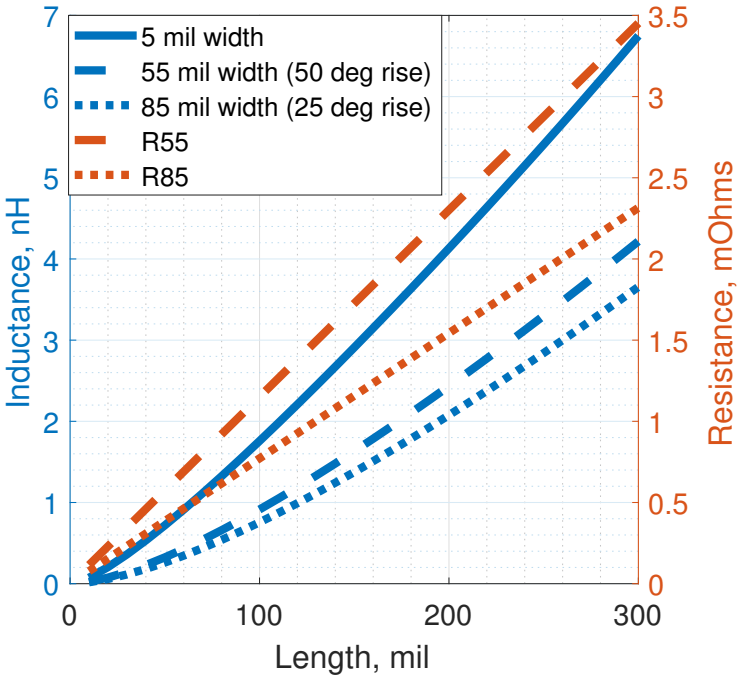


Figure 3.6: PCB trace resistance and inductance of 2 oz copper using 4PCB.com calculator.

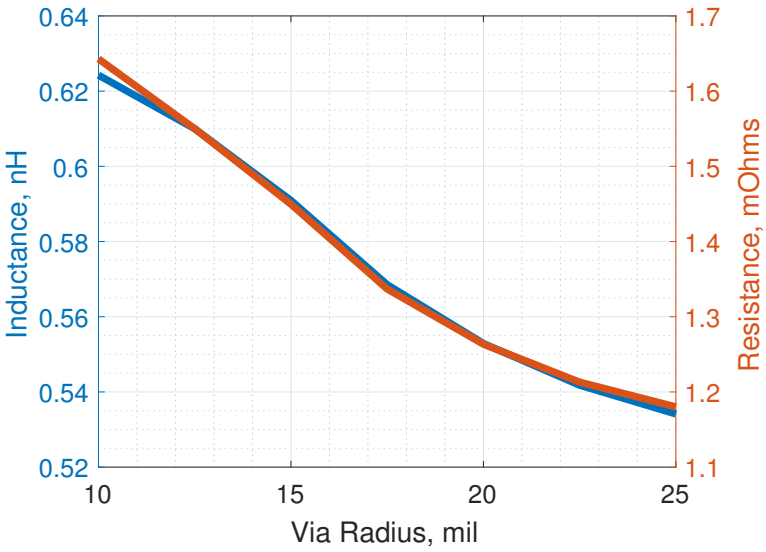


Figure 3.7: PCB via resistance and inductance of 2 oz copper using Q3D.

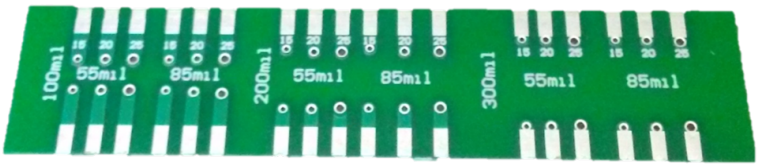


Figure 3.8: Several PCB inductors

three different currents, and than averaged. This is the DC resistance of the inductor. It was also desired to measure the AC resistance and inductance for validation of the Q3D model, however, a reliable measurement was not obtainable due to the small values involved. The results of the DC measurement are shown in Fig. 3.9. All linear dimensions are in mils, with each trend line representing a length-width pair (i.e "100,55" is 100 mils long and 55 mils wide). The data is plotted for three via radii, also in mils.

For the 55 mil trace (300 mil long) with a 25-mil via, the Q not considering the rest of the circuit is decreased from 30 to 19 with just 2.5 $m\Omega$ of added DCR. For the practical circuit, the Q is reduced from 4.3 to 0.68. Overall, using a PCB trace does have significant improvement over using bondwires, but they are not suitable for high-current designs due to low Q values and increased complexity. For this reason, and since fabrication of novel integrated inductors is not available, all of the design considerations in this work use a COTS inductor.

As a whole, inductors, even air-core, have a loss fraction that increases as size is reduced. A constant efficiency is not possible and power density will also decrease with size. The best analysis is then to maximize a given volume for the inductor and choose circuits that utilize the lease number of magnetics [99].

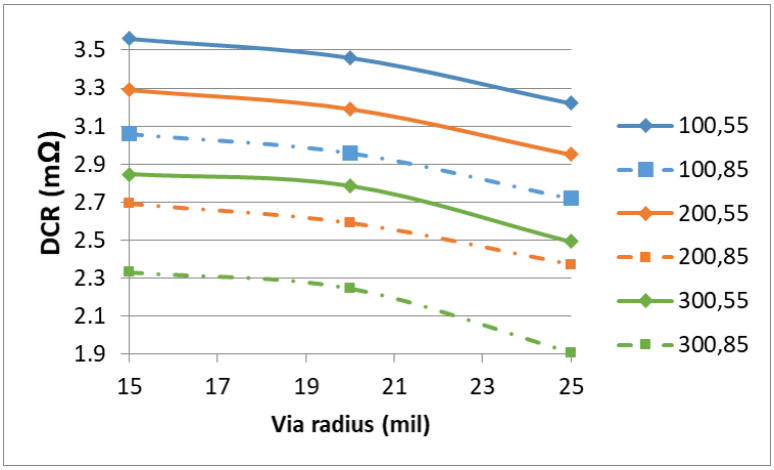


Figure 3.9: DC resistance measurements for various PCB inductors

3.3 COTS

Commercial-off-the-shelf, or COTS components are those that are ready made and commercially available to the general public. They are economical and in great supply, but are usually general for application use. As such, manufacturers attempt to optimize their components to meet a wide area of uses while also giving quality performance. This section looks at the real-world models of some components and how practical implementations inform the design of the SC and ReSC.

3.3.1 Capacitors

The simplified schematic for a real capacitor is shown in 3.10. It is comprised of an ideal capacitor, an inductor, and a resistance. In a multi-layer ceramic capacitor (MLCC) the inductance will depend on package geometry, whereas the resistance depends on the dielectric, its spacing, and interconnects.

The parasitic inductance causes the capacitor to have a self-resonant frequency defined as:

$$f = \frac{1}{2\pi\sqrt{LC_{fly}}} \tag{3.1}$$

And the *quality factor,* Q can also be defined as:

$$Q = \frac{1}{R_{ESR}}\sqrt{\frac{L}{C_{fly}}} \tag{3.2}$$

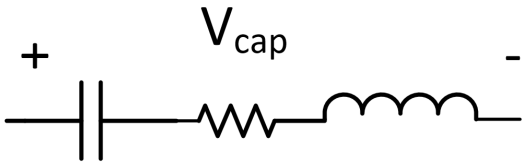


Figure 3.10: Parasitic elements within a real capacitor

At the resonant frequency the impedance is the parasitic resistance. Placing many identical capacitors in parallel will not alter the resonant frequency, since the inductance and capacitance decrease and increase by the same rate, respectively. Paralleling will reduce power loss from the resistance by a factor of n^2, where n is the number of parallel devices.

Surface mount MLCC's come in standard packages named for their dimensions in mils. Since the inductance is highly package dependent, a given package size will have the same parasitic inductance. Table 3.1 lists the parasitic inductance of several standard surface mount MLCC's as extracted from TDK's equivalent circuit models [100] as well as the inductance for their wide-body version (that is, the wide-body version of an 0805 is 0508).

Unsurprisingly, the larger the physical size of the capacitor, the more inductance it will have. Since a larger LC will have a lower resonant frequency, when operating the SC in SSL, we would like to place the resonant frequency as far from the switching frequency as possible. A large capacitance in a small package will help. Using wide-body capacitors will also help as the inductance is reduced by at least 75 %.

Unfortunately, smaller packages like 0201 are limited in available capacitance. For example, a quick search of Digikey for a 0201, 16 V, X5R capacitor yields a max capacitance of only 1 μF [101]. When selecting a capacitor, those with little to no variation with temperature are preferred since the ESR in the capacitor will cause heating that could shift the resonant frequency. C0G (Class I) is a dielectric with no temperature coefficient and no piezoelectric effects. It is commercially available in sub-microfarad values and will be disqualified from high power designs as per (4.3). Additionally, it is not as volumetrically efficient as Class II and Class III dielectrics. For high power applications, X5R and X7R

Table 3.1: Parasitic inductance for standard MLCC packages

Package	Inductance	Wide-body Inductance
0201	0.30 nH	-
0402	0.37 nH	-
0603	0.42 nH	0.1 nH
0805	0.48 nH	0.12 nH
1210	0.75 nH	0.187 nH

are generally considered acceptable (the higher available capacitance is worth the greater derating). Capacitor derating is when the capacitance under a specific operating condition is reduced relative to its nominal value. In circuits sensitive to the value of the capacitor, many may need to be put in parallel to compensate for the derating and attain an equivalent, effective capacitance.

Table 3.2 highlights the maximum capacitance found on Digikey for C0G, 16 V in a variety of packages. Since the values are so small compared to what is needed for higher current applications, paralleling many C0G capacitors would not be as power dense as a single X5R capacitor that is over-specified to compensate for the derating.

Table 3.3 ([102]) shows the letter and number codes used to classify Class II and Class III capacitors. Since these types do exhibit piezoelectric effects, they will literally expand and contract with applied voltage [102]. It is possible for this to cause an audible hum and for the vibrations to propagate to other areas of the circuit. However, there is no conclusive reliability issues associated with this effect [103].

Fig. 3.11 ([102]) plots variations of capacitors over different conditions based on Muratas web tool. Over various sizes and voltage ratings, a 4.7 μF capacitor is shown in both X5R and X7R [102].

A few key observations are made. First, as the physical size of the capacitor increases, the variation with DC bias will decrease. Second, for a given dielectric and package size, the lower rated capacitors will exhibit less derating. For example, the 1206 X5R with a rating of 6.3 V has less deviation than higher rated capacitors of the same type. Lastly, for a given package size, X7R will always be less sensitive to voltage bias than X5R, for

Table 3.2: Maximum capacitance for C0G capacitors in various packages

Package	Maximum Capacitance
0201	1000 pF
0402	2200 pF
0603	18 nF
0805	47 nF

Table 3.3: Capacitor Codes for Class II and Class III MLCC [102]

Low Temp	High Temp	Change over Temp (max)
Char, Temp (°C)	Num, Temp(°c)	Char, Change(%)
Z, +10	2, +45	A, ±1.0
Y, -30	4, +65	B, ±1.5
X, -55	5, +85	C, ±2.2
-,-	6, +105	D, ±3.3
-,-	7, +125	E, ±4.7
-,-	8, +150	F, ±7.5
-,-	9, +200	P, ±10.0
-,-	-,-	R, ±15.0
-,-	-,-	S, ±22.0
-,-	-,-	T, +22,-33
-,-	-,-	U, +22,-56
-,-	-,-	V, +22,-82

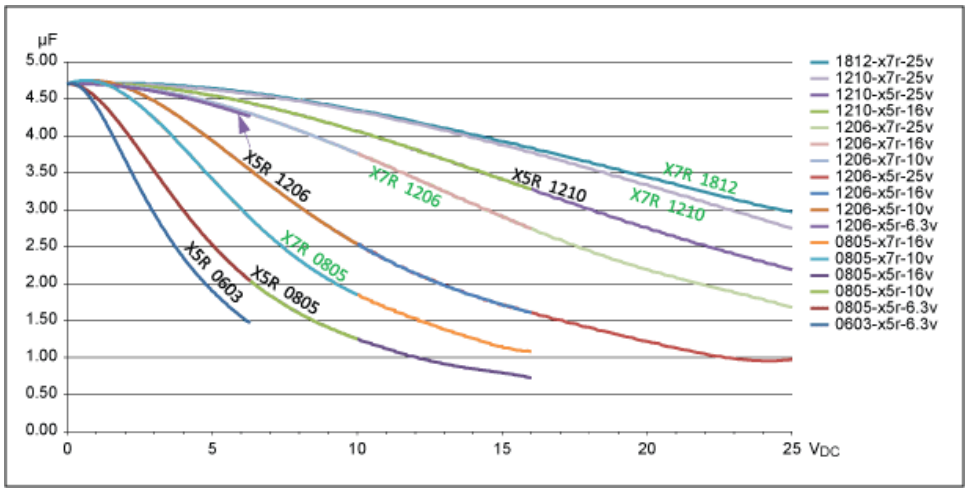


Figure 3.11: Capacitance variation vs. DC voltage for select 4.7 μF capacitors [102]

the data provided, although this might not be universal [102]. Table 3.4 ([102]) extracts capacitor variation of X7R with a 12 V bias. As the size increases, the derating approaches the nominal value, with little improvement beyond 1210.

This is useful to keep in mind since, to compensate for DC bias derating, it may be more geometrically advantageous to use a larger capacitor than to parallel two or more smaller capacitors. For example, two 0805 capacitors would minimally occupy 2*8*5 = 80 mil^2 and a single 1206 occupies 72 mil^2. Although any two capacitors may be classified as 'X7R', there are a variety of materials that can be used to get X7R performance. The classification and ratings are *only* assigned for variation over temperature, not DC bias. So any vendor with a ±15 % variation over the temperature range of -55°C to + 125°C can be called X7R, even if the voltage derating is over 50 %. Barium Titante is a ferroelectric material and most commonly used in Class II capacitors, with specific formulations that determine the voltage coefficient. For the purpose of this work, it is not necessary to go into much detail about the various materials used. It is sufficient to know that ferroelectric materials exhibit higher dielectric constants in a smaller physical size than Class I capacitors, as well as possessing the piezoelectric and pyroelectric (variation with temperature) properties. Smaller physical size for a given capacitance occurs when the dielectric thickness is reduced, increasing capacitance loss. Even Class I capacitors may exhibit DC bias derating, depending on the dielectric material used. Calcium Zirconate capacitors do not have this characteristic [102, 104].

Most manufacturers will include characterization data of their capacitors. This is needed for derating the DC voltage bias and other variations as the application requires. It also gives

Table 3.4: X7R capacitor variation with 12 V bias [102]

Size	Capacitance	% of Nominal value
0805	1.53 μF	32.6
1206	3.43 μF	73.0
1210	4.16 μF	88.5
1812	4.18 μF	88.9
Nominal	4.7 μF	100

the resonant frequency and ESR. Capacitors with a resonant frequency near the switching frequency can be problematic, as operating at the exact frequency over a wide range of loading conditions, with no variation in capacitance or inductance is not possible. This can be seen experimentally in Fig. 3.12 where a 2:1 SC is operating below, near, and above the resonant frequency. This is for a low-Q resonance.

The resonant frequency is approximately 530 kHz. In Fig. 3.12b, the current is nearly sinusoidal. As the converter is operated at a lower frequency, the current remains somewhat sinusoidal but with more distortion as hard-charging becomes more dominant. At 1 MHz, the current wave-shape more closely resembles hard-charging, although there is still some discrepancy due to resonance. As will be examined later on, the proximity to the resonant frequency greatly affects the operation of the SC and a rule-of-thumb of operating half a decade below f_{res} is developed for predictable behavior.

Discussed further on are PCB parasitics and for the SC, since the Q is so low and the package parasitic is less than 1 nH, then any additional stray inductance can change the resonant frequency by a significant percent. This may cause the converter to behave in an undesirable way.

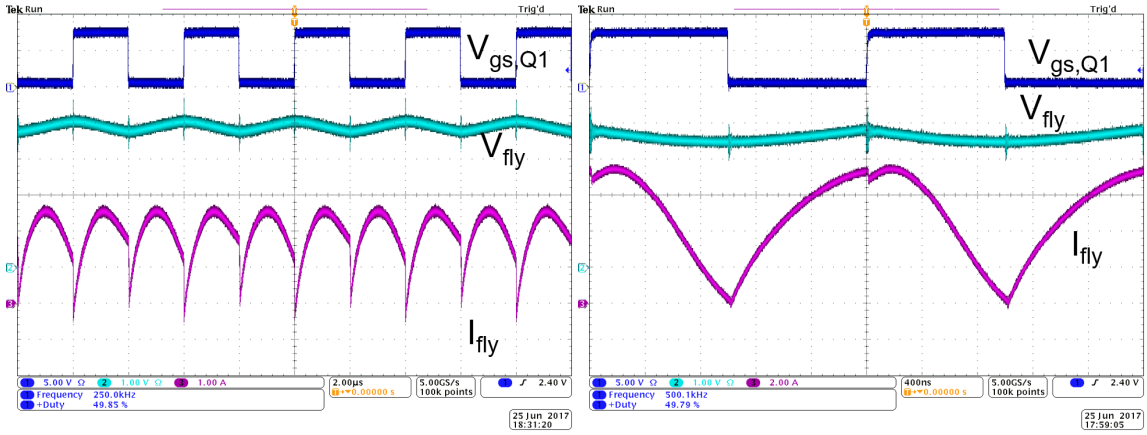
Paralleling Capacitors

As mentioned previously, paralleling capacitors can be beneficial in reducing loss attributed to the ESR and inductance in the main conduction path. The practical limit to paralleling capacitors and determining if the extra area needed justifies the improvement in circuit performance is addressed by developing the equivalent circuit model shown in Fig. 3.13.

The total capacitance of the parallel combination is [105]:

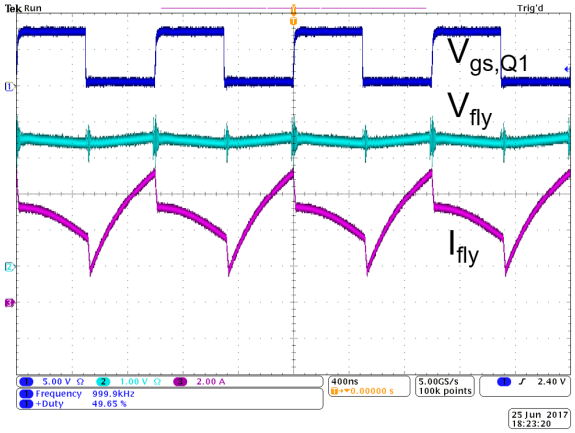
$$C_t = n \cdot C \tag{3.3}$$

where n is the number of parallel capacitors.



(a) A 2:1 SC operating at 250 kHz, 2 A

(b) A 2:1 SC operating at 500 kHz, 3.5 A



(c) A 2:1 SC operating at 1 MHz, 5A

Figure 3.12: Experimental observation of the capacitor current operating below, near, and above the resonant frequency with a low-Q.

Physicist Richard Feynman is credited for developing a formula for an infinite resistor ladder. This assumes an infinite number of parallel branches like that in Fig. 3.13 for shorted inductors and capacitors. The total impedance due to the parasitic resistors is [106]

$$R_t = \frac{R_B}{2} + \sqrt{\frac{R_B^2}{4} + R_B R_C} \tag{3.4}$$

Where R_b is the resistance added per branch, that is the resistance between two capacitors as a result of layout, and R_c is the resistance inherent in the capacitor. The total impedance due to only the parasitic inductances of layout and the capacitors can be found by shorting the resistors and capacitors

$$L_t = \frac{L_B}{2} + \sqrt{\frac{L_B^2}{4} + L_B L_C} \tag{3.5}$$

Where L_b is the inductance added per branch, that is the inductance between two capacitors as a result of layout, and L_c is the inductance inherent in the capacitor.

Assuming that several capacitors are evenly aligned in parallel, ESR and inductance will be introduced as a result of layout. If all of the current enters the circuit from the left, then the capacitors at the farthest end toward the right will experience a phase shift due to the PCB inductance and an increased time constant in charging and discharging. An LTSPICE implementation is constructed in Fig 3.13.

An off-the-shelf 0603 capacitor is selected with its parasitic inductance L inside the capacitor model. A parasitic inductance and resistance per branch of 1 nH and 1 $m\Omega$, respectively, is selected as an example of a layout to reduce resistance at the expense of slightly more inductance. The phase shift can be seen in Fig. 3.14 between the $C1$ and $C6$. The peak current in $C6$ is lower and the time to reach zero is longer, but the total area, that is the charge, is the same for all capacitors.

The equivalent model can be verified by calculating the total Q of the circuit and comparing it to the impedance of the circuit. The total impedance Z_T and Q are

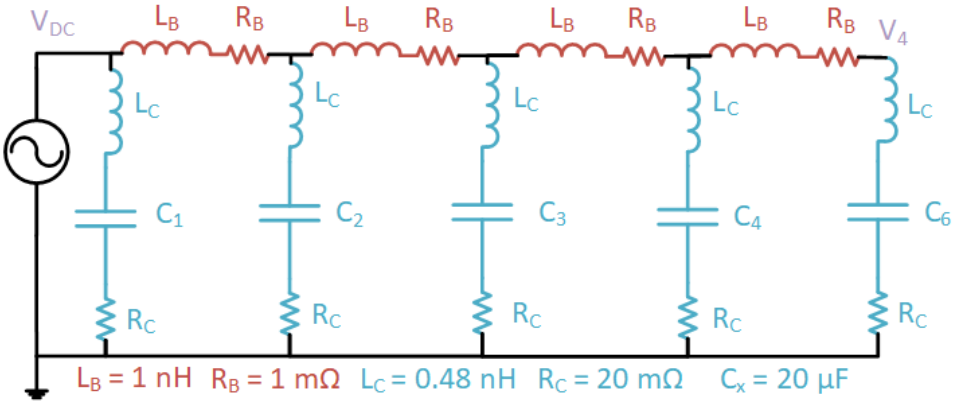


Figure 3.13: Schematic for the parallel capacitor model

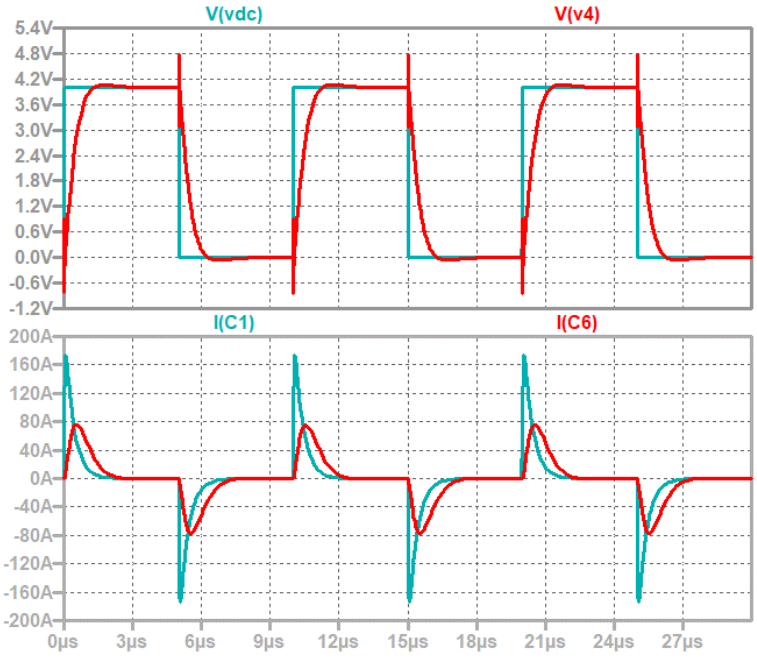


Figure 3.14: Waveforms of the parallel capacitor model

$$Z_t = \frac{1}{sC_T} + sL_T + R_T \tag{3.6}$$

$$Q_t = \sqrt{\frac{L_t}{C_t}}\frac{1}{R_t} \tag{3.7}$$

The bode plot for the parallel network is shown in Fig. 3.16. The Q is 0.3476. This Q is considered low and shouldn't impact the operation of the SC. At larger branch inductances, resonance within a capacitor can occur which may lead to higher losses as shown in Fig. 3.17.

Looking at how the Q changes paralleling capacitors for an unconstrained area as plotted in Fig 3.15, gives insight to the diminishing returns of paralleling. The blue curve is for the circuit in Fig. 3.13. Additionally there is the case where the branch inductance is doubled to 2 nH, and when with 1 nH of inductance, the capacitance is halved to 10 μF. A reference line indicating ten parallel capacitors is also added. Of note is that for all cases, the Q levels-out to a finite value for an infinite number of capacitors in parallel. It can be seen that the Q for all three scenarios is also nearly the same for 10 and fewer capacitors. This means that the capacitors and layout would have to be precisely selected such that soft-switching would occur for many paralleled capacitors, which in space constrained designs might not be worth the reduced power loss. This is examined in Chapter 6. Additionally, with modest layout techniques, unwanted resonance can avoided.

The overall improvement in efficiency will then also have diminishing returns for increased paralleled capacitors. Considering a design with 10 A output current, the number of parallel capacitors beyond ten will only add to increased area without improvement in overall efficiency. This is due to the R_t becoming less than the PCB resistance. It is important to include the Slow Switching Limit (SSL) in the analysis, as the optimal frequency must be constrained within the normal operating range. The SSL and an analysis of the efficiency impact of paralleled capacitors is detailed in Chapter 4.

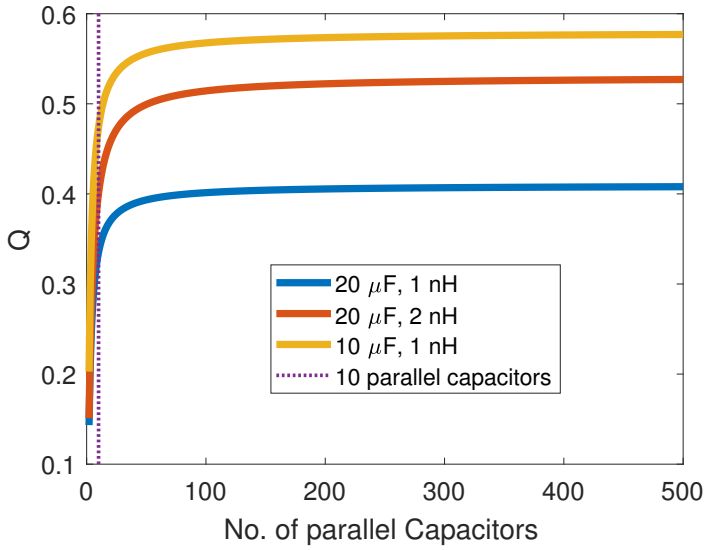


Figure 3.15: Q as a function of paralleled capacitors for the LTSPICE model

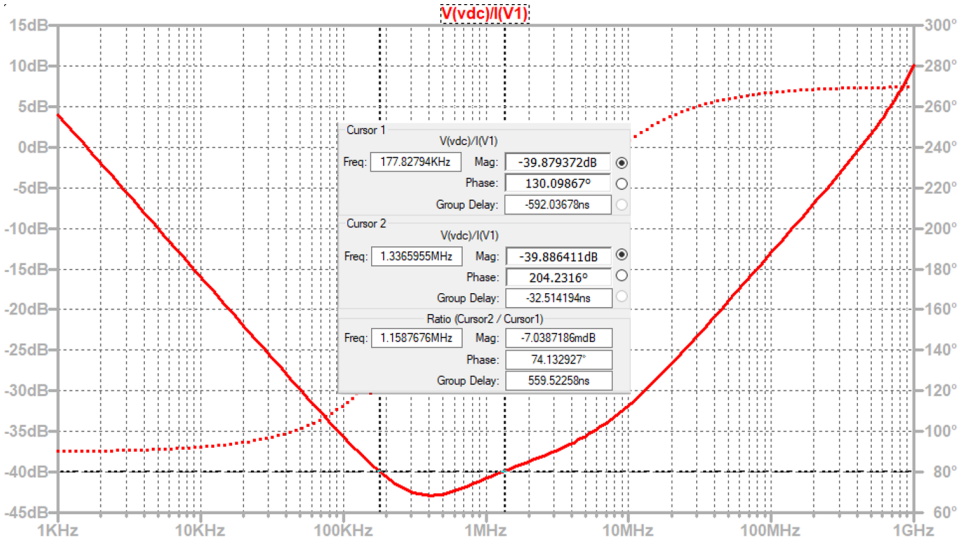


Figure 3.16: Bode plot of the parallel capacitor model

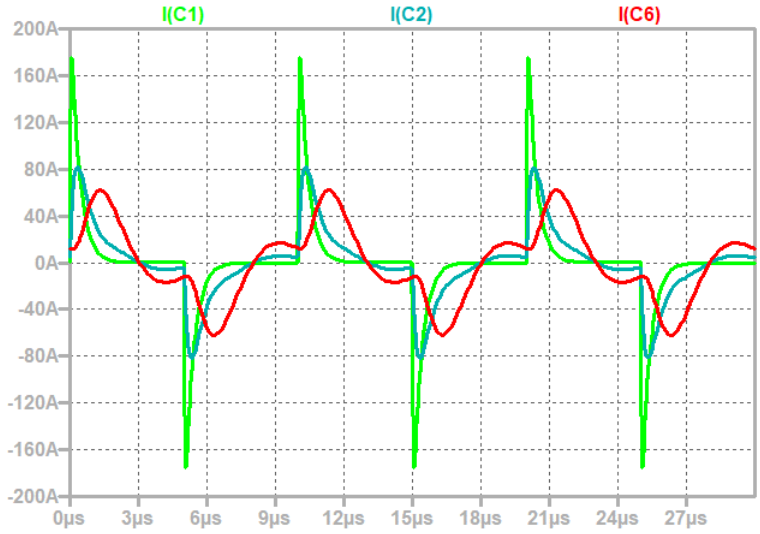


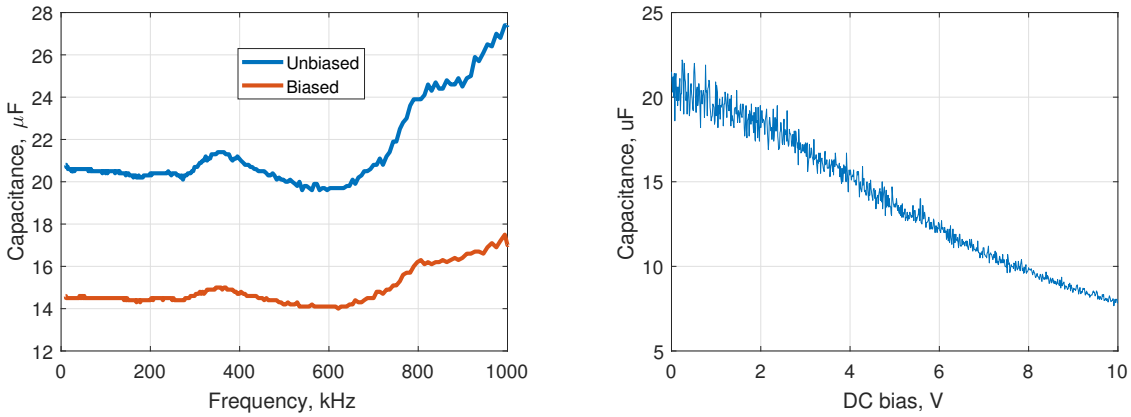
Figure 3.17: 5 nH branch inductance in the parallel capacitor model

As stated previously, the capacitance value can change significantly when a DC bias is applied. Five parallel 4.7 μF capacitors are measured with an impedance analyzer with and without bias. The nominal total capacitance should 23.5 μF. In Fig. 3.18a the unbiased total capacitance is swept over frequency and then again with a 4 V bias. Notice that even unbiased, the capacitance is less than the nominal value.

Under the bias condition, the capacitance is reduced by at least 25 %. The capacitance begins to increase near 800 kHz, as the resonant frequency of the measurement is about 1.5 MHz. The same paralleled capacitors are measured at 500 kHz across DC bias in Fig. 3.18b. As the bias increases, the total capacitance decreases, reaching 50 % of its unbiased value at only 8 V. It is impossible to generalize this trend as it can vary between manufacturers, capacitor series, and even individual capacitors in the same lot, as DC bias derating is not a controlled variable in manufacturing. Since this can easily alter the resonant frequency and current (or ripple) capability of the ReSC and SC, respectively, it is essential to characterize the capacitors used in the converter or develop other means to compensate.

3.3.2 PCB Layout

As already mentioned, the layout of the SC can be very sensitive to parasitic inductance. It is also desirable to parallel capacitors for reduced ESR. A layout like that shown in Fig. 3.19, can cause uneven current sharing in the capacitors as most of the current passes through the



(a) 4 V bias over frequency **(b)** Bias sweep at 500 kHz

Figure 3.18: Bias derating of five parallel 4.7μF capacitors

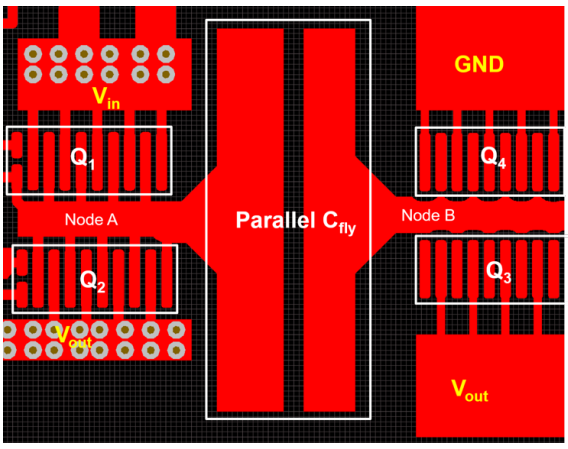
middle two, leaving the rest under-utilized, thus increasing the effective paralleled resistance. This is a "schematic" type layout where essentially the power stage mirrors the layout of the schematic in terms of each components orientation (see Fig. 5.3).

The current density is shown in Fig. (3.19b) using FEA in Q3D software. Several capacitors are placed in parallel as in a real layout. The capacitors themselves are just shorted with copper on either side with current entering node A and exiting node B. While this does not model the physical caps, it does show how layout geometry affects the current distribution.

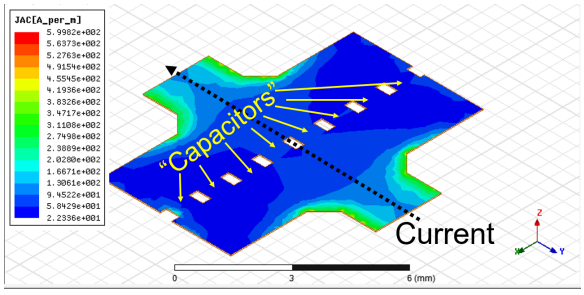
Most current crowding occurs where the two switches meet, which increases resistance while attempting to increase power density. Through the "capacitors" most of the current goes through the middle two, with less current for those on the outer edges. This means that adding an arbitrarily large number of capacitors will have diminishing returns as each added capacitor will contribute less to the reduction of voltage ripple. At 1 MHz, the inductance is 3.3 nH.

A similar layout is shown in Fig. 3.20 where, even with 10 paralleled paths, the current still goes through the path of least resistance. At 1 MHz, this inductance is 5 nH, the same as for just a single cap.

The layout shown in Fig. 3.21a is an improvement as it breaks the switches into half-bridges, placing each on either side of the capacitors. This reduces both parasitic inductance



(a) "Schematic" layout



(b) Current distribution of paralleled capacitors

Figure 3.19: A non-optimized layout technique

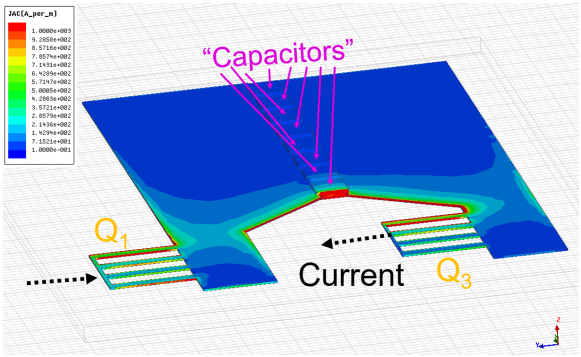
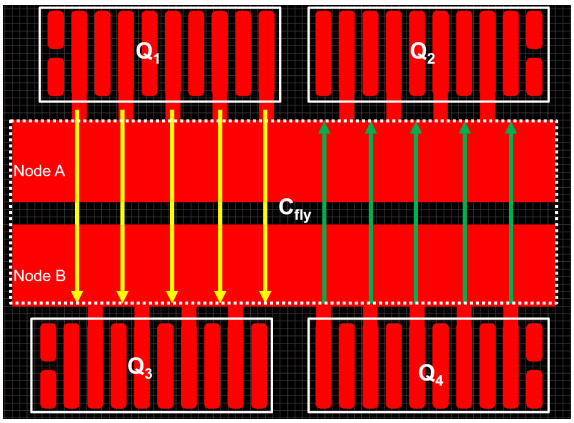
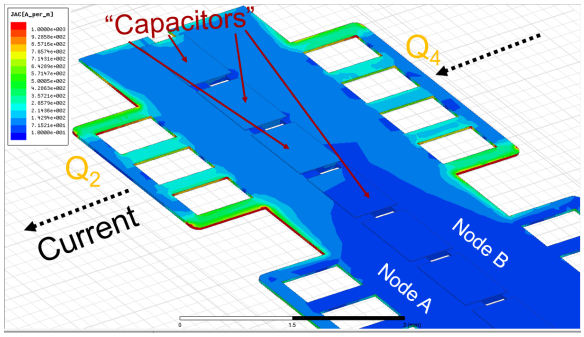


Figure 3.20: Current Distribution of the shortest path for paralleled capacitors



(a) Improved Layout



(b) Current distribution in second half-cycle

Figure 3.21: Improved layout for flying capacitor utilization

and resistance and improves power density. In Fig. (3.21b) the current distribution can be shown to be better shared between half of the capacitors for each half-cycle. At 1 MHz, the inductance is 1.8 nH. This layout out also improved current sharing in the GaN device as well.

Similarly, for the ReSC, although it is not space efficient to line everything up, since the inductor is rather long, the current sharing in the GaN devices can be improved by placing the switches at a 45 degree angle. This decreases the resistance in the pad area to only $1m\Omega$. This is shown in Fig. 3.22 and the current distribution is shown in 3.23. This is a more efficient use of space. Consider the layout in 3.19a. If one wanted to increase the width of node 'A' to be the same as long-edge of the switch (distance 'x'), Q_1 would need to be pushed up by 'x'. For the 45-degree layout, to get the same trace area, the top corner of Q_1 (and everything laid-out above it)is only pushed up by $\frac{x}{\sqrt{2}}$ or 0.707 times the distance.

Small alterations to layout can yield large improvements since the output impedance is in milli-ohms, so it doesn't take much to change it by 10 %. For the SC, this is seen in decreasing the slow-switching limit and for the ReSC increasing conduction loss. There are many well documented techniques for optimal layout and only a couple are looked at here. A good design will have minimal ESR, and for the SC, minimal inductance as well. When achieving high power density designs, the current distribution in the traces should be considered, as this can add more than expected impedance and under-utilize some components.

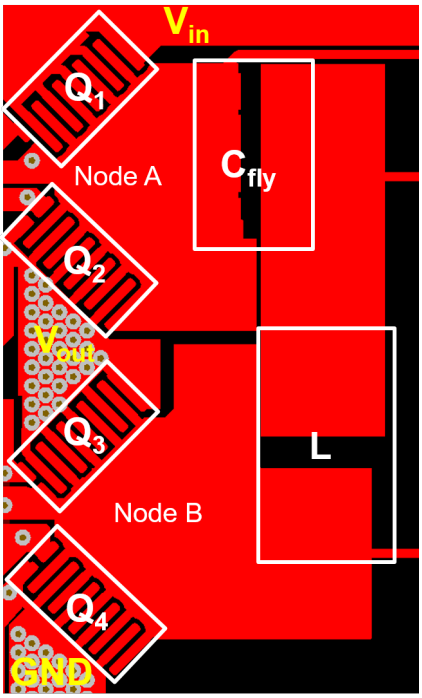


Figure 3.22: ReSC using the 45-degree orientation for the GaN switches

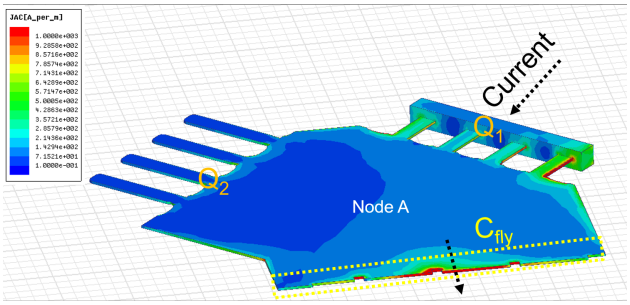


Figure 3.23: 45-degree current distribution for the node connecting two switches

3.4 Summary

The practical limitations of circuit design as they relate to designing the SC and ReSC are explored. This is necessary for the full topology analysis to follow as it sets some upper and lower boundaries under which the analysis is verifiable. The use of GaN is employed due to its improved FOM over Si, resulting in reduced power loss.

The use of integrated inductors is not feasible for this work due to the high current requirement and the difficulties associated with such designs is examined. Although there is potential for volume reduction, the current technology does not support high quality inductors at low cost for such reduction. Inductors by nature do not lend themselves well to miniaturization [79].

The biggest consideration for this work is the capacitor, as there are many factors to consider when anticipating their performance. The parasitic elements in the real capacitor model and the DC bias derating can have a severe effect on the operation of both the SC and ReSC if not properly considered. Reduction of the capacitor ESR can be done by paralleling, but doing so for an ESR below the parasitic resistance of layout will not improve circuit performance. As capacitors tend to have an ESR to surface area ratio higher than other components, paralleling some capacitors will be necessary for thermal management.

Layout as well can alter the loss model for both converters. Seemingly minor changes can improve the loss associated with layout considerably. It is desirable that every component in an area-constrained design be fully utilized, so as to justify its placement. The current distribution due to layout will not always be even and can result in even further diminished returns for paralleling capacitors.

Chapter 4

Switched Capacitor

4.1 Introduction

The 2:1 SC lends itself favorably to integration and high power density applications. However, it exhibits hard charging due to the flying capacitor being connected from the input capacitors to the output capacitors. This hard charging will limit the efficiency of the converter. For high current applications, the flying capacitance needs to be increased in order to deliver the needed energy every half-cycle. While soft charging techniques have been explored as outlined previously, this work will look at the hard-charged SC. The main benefit of the SC is the lack of inductor compared to other topologies, so a comparison of the inductorless SC with a resonant inductor SC in terms of power loss and area is later performed to evaluate the merit of this benefit. It thus examines the two extremes of no inductor and a discrete inductor. This chapter details the equivalent circuit model, loss model, and other considerations to establish the framework that will be investigated in Chapter 6. The ultimate goal is to compare the SC to its fully resonant cousin, the ReSC, in order to evaluate the application space for both.

4.2 Topology Description

As stated previously, SC converters do not use an inductor. Instead a capacitor is used to alternately connect the source to the load. This capacitor is known as the flying capacitor,

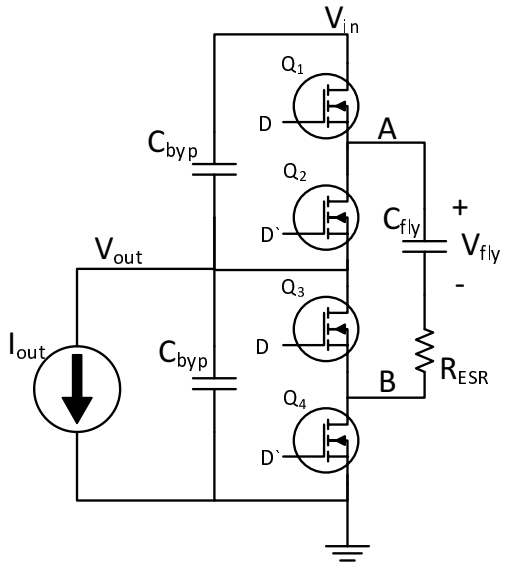


Figure 4.1: Schematic of a 2:1 SC

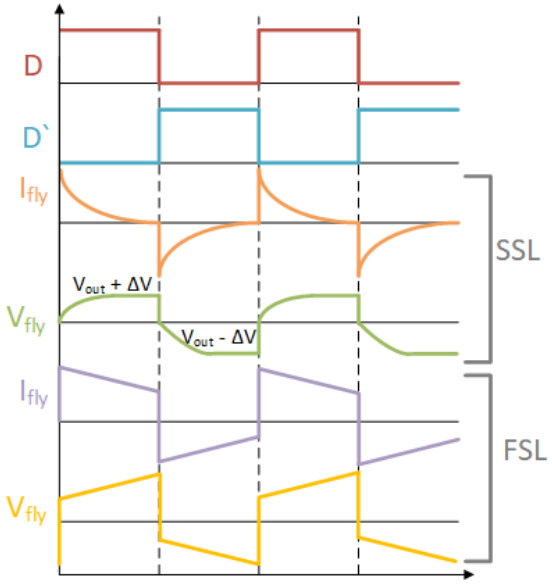


Figure 4.2: Switching waveforms for the SC

C_{fly}. The switched capacitor circuit is shown in Fig. (4.1) with its gate signals shown in Fig. (4.2).

During Phase I, Q_1 and Q_3 are turned on. The voltage across the capacitor is V_{in}–V_{out}, which simplifies to V_{out} for the 2:1 converter. During Phase II, Q_2 and Q_4 are turned on with Q_1 and Q_3 off. Node A of the capacitor is now connected to V_{out} and the voltage across the capacitor is V_{out}. In steady state, the voltage across C_{fly} is $V_{out} = 0.5\ V_{in}$. In SSL I_{fly} goes to zero and V_{fly} is equal to the output voltage. However, the output voltage will be less than $\frac{V_{in}}{2}$ due to losses. This is the voltage ripple, ΔV that is reduced with larger capacitor values. The large capacitor charging current spikes result from the inrush current of connecting two capacitors with different voltages together. The integral of this current is the charge transferred per period in and out of the capacitor. The energy lost during this transfer is termed the charge sharing loss. This is an inherent loss in any switching capacitor topology and is proportional to the voltage ripple across C_{fly}. Additionally, this uncontrolled current leads to efficiency reduction and EMI noise. Although the charge sharing loss is independent of series resistance, there will still be conduction loss resulting from the charging/discharging current.

The SC can be modeled as an ideal transformer with a series output impedance as shown in Fig. (4.3).

The transformer captures the step-down nature of the converter and the series impedance considers the voltage transients of the flying capacitor being charged and discharged between two voltage sources, as well as the total DC series resistance in the circuit [2, 69]. That is, the AC ripple resulting from switching will be energy lost to the series resistance elements. As a result there will be a voltage drop with non-zero current, reducing the output voltage from its ideal value [107].

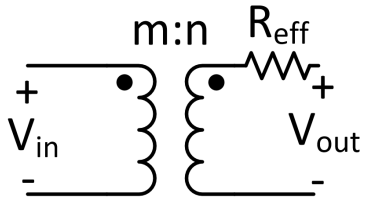


Figure 4.3: Output impedance model for the m:n SC

This output impedance gives rise to two modes of operation: the slow switching limit (SSL) and the fast switching limit (FSL). SSL is largely determined by the value of the flying capacitor and R_{eff} can be approximated by [78, 2]:

$$R_{eff} = \frac{1}{4C_{fly}f_s} \coth\left(\frac{1}{4f_sC_{fly}R_{ESR}}\right) \tag{4.1}$$

Here, the hyperbolic cotangent term captures the SSL/FSL transition and the factor of 4 captures the reflected output impedance for the 2:1 converter [17]. The series resistance is used because in the FSL, the output impedance converges to this value, and so their will be a transition from one operating area to the next. Reducing the on-state resistance of any of the components will have no affect on the output impedance. Since only charge redistribution occurs in SSL, these losses will only depend on the differential voltage and capacitance [14].

In FSL, the impedance of the flying capacitor is less than the total DC resistance, preventing charge equilibrium from being obtained. This occurs when the capacitor current becomes constant and the voltage of the flying capacitor can be modeled as constant. The output impedance is simplified to the total DC resistance, and the voltage across the flying capacitor is constant [69]. Past FSL, the impedance will increase and the circuit becomes inductive as the parasitic inductance in the circuit dominates the impedance model.

As the switching frequency approaches the SSL/FSL boundary, the converter will operate in a third state. As derived in [69] the output impedance is approximated as:

$$R_{eff} = \sqrt{(R_{SSL}^2 + R_{FSL}^2)} \tag{4.2}$$

Where $R_{SSL} = \frac{1}{4C_{fly}f_s}$ and R_{FSL} is the series resistance in the power path, including the FET channel resistance and resistances due to layout. The equation for the output ripple is given according to the charge balance across C_{fly} [70]:

$$\Delta V_o = \frac{I_{out}}{2C_{fly}f_s} \tag{4.3}$$

This is particularly useful as it relates the output current capability with switching frequency and capacitance. It can be seen that for 10% voltage ripple, 10 A designs, with 50 μF, the switching frequency will be 2.5 MHz, which may be too near the resonant frequency. Voltage ripple is a specification that is prominent in all power supplies acting as a voltage source and is very stringent for lithium ion batteries, as the ripple can cause additional heating, which in turn can be destructive. Since the ripple is proportional to the output current and inversely proportional to the flying capacitance, a trade off needs to be made with C_{fly} for area constrained designs.

Although operating in FSL results in lower output impedance, the converter is not well-behaved, suffers from increased switching loss, and its output impedance is not controllable, which is the most popular way to implement feedback. For this reason, and to also use simplified expressions that ease the analysis, the SC should be operated in the SSL. This limit can be determined by looking at R_{SSL} as it deviates from the full expression of (4.1). The amount of deviation is somewhat arbitrary and related to the level of error one can tolerate in predicting losses. For this work we use 2 %. In Fig. 4.4, these boundaries are shown for a SC circuit with $C_{fly} = 1\ \mu F$, and $ESR = 34\ m\Omega$.

The space in-between SSL and FSL can span a wide frequency range and always results in the R_{SSL} being substantially greater than R_{FSL}.

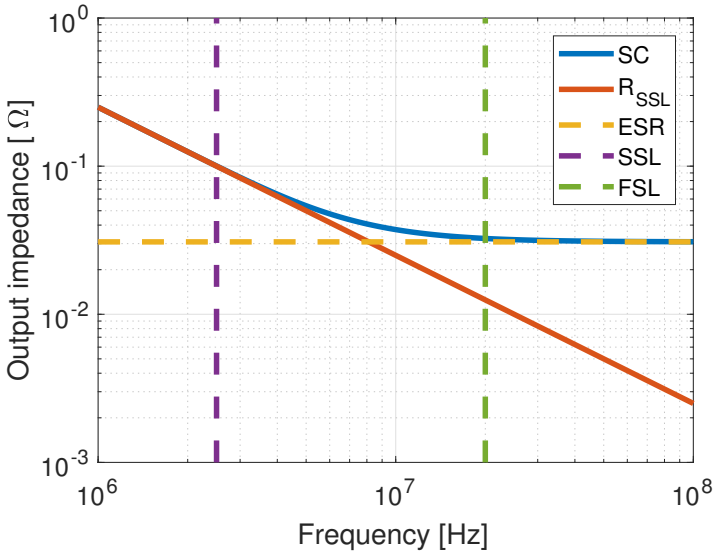


Figure 4.4: SSL and FSL boundaries for a given SC design

4.2.1 Maximum Switching Frequency

As discussed in Chapter 3, operating the SC near the self-resonant frequency of the circuit can lead to non-ideal waveforms. Fig. 4.4 shows the accuracy of limiting the switching frequency to about a 2 % deviation assuming the resonant frequency is deep into the FSL. For when this isn't the case, the effective output impedance for a low-Q capacitor is shown in Fig. 4.5 ($L_{parasitic} = 1.1\ nH$, $C_{fly} = 20\ \mu F$). The self-resonant frequency is shown as well as (4.1) and (5.5). With a Q of 0.185, the simplified expression of (4.1) is sufficient to find the SSL/FSL boundary. However, the resonant frequency will highly influences by parasitics in the layout as shown in Fig. 4.6.

This figure shows the resonant response of the same PCB for a SC circuit. Each curve is with a different parasitic inductance according to the path length between nodes A and B as in Fig. (4.1). With just a small adjustment to the loop inductance (7 mm), the resonant frequency decreases from 1.8 MHz to 0.75 MHz. If operating near the SSL boundary, this could severely alter the circuit behavior as shown in Fig. 3.12.

The same capacitor with 100x more parasitic inductance is shown in Fig. 4.7 ($Q = 3$). The resonant oscillations begin to become more prominent as the SSL boundary is approached. An upper bound on the switching frequency can than be set by calculating when the two models begin to diverge by more than a given amount. For frequencies below this, modeling can be simplified by using the expression of (4.1). Imposing this limit will guarantee the SC is operating in SSL and sufficiently far from the resonant frequency to ensure the ideal hard-charging waveforms. Since the bandwidth of this low-Q circuit is wide, the range of frequencies that impact the output impedance will also be wide. The limit is qualitatively set as half of a decade below the resonant frequency to ensure SSL operation.

4.2.2 Loss Model

The maximum theoretical efficiency of the SC is a function of the conversion ratio and is given as:

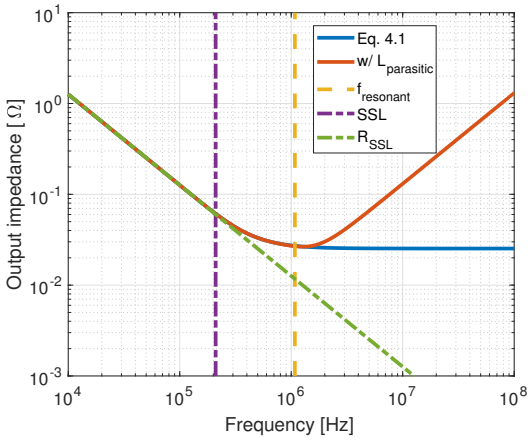


Figure 4.5: Effective output resistance of a low-Q capacitor

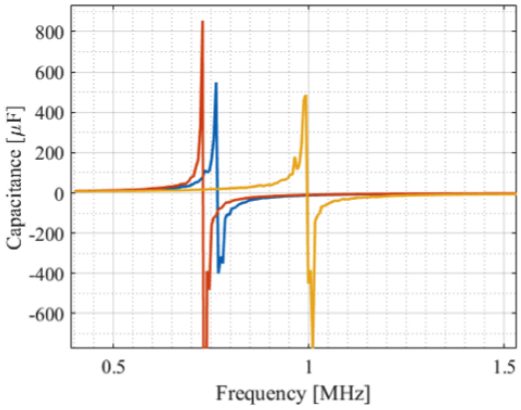


Figure 4.6: Resonant response of a SC PCB with 1.1 nH (red), 1.1 nH with 5 extra mΩ (blue) and 2 nH (yellow) of loop inductance

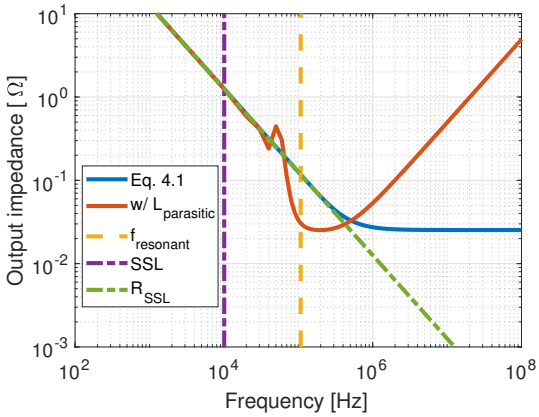


Figure 4.7: Effective output resistance of a high-Q capacitor

$$\eta = \frac{nV_{out}}{V_{in}} \tag{4.4}$$

Where n is the conversion ratio. When the SC is operating at its nominal conversion ratio (when $V_{in} = 2V_{out}$ for $n = 2$, for example) the maximum efficiency is 100 %. For intermediate conversions (attempting to perform a 3:1 conversion with a 2:1 SC, for example) the efficiency is severely degraded. This has been addressed in the past by switching in and out several discrete conversion levels [107]. For simplicity the nominal 2:1 is only considered.

Since the output impedance in Fig. (4.3) is in series with the output current and it captures the charge sharing and resistive loss, the conduction loss is simply [2, 78]:

$$P_{cond} = I^2 R_{eff} \tag{4.5}$$

And the switching loss now approximated to be the loss due only to C_{oss}. This is given by:

$$P_{sw} = (0.5)\,(4)\,C_{oss} V_{DS}^2 \tag{4.6}$$

Since each device blocks half the input voltage in the 2:1 converter, $V_{ds,off} = V_{out}$.

The drawback to the SC converter is in the direct charging/discharging that occurs between capacitors and voltage sources. This induces large transient current spikes which limit power density and stress the switching devices. This can be remedied by using larger capacitors and higher switching frequency but another alternative is placing an inductor either at the output (soft-charging) or in series with the flying capacitor (resonant operation)[2].

The loss model here is well established and introduced for further discussion on the trade-offs that will need to occur for an optimal design.

4.2.3 Model Validation

The loss models derived above are validated experimentally using EPC GaN. The design is summarized in the Table 4.1.

The input and output capacitances are over-designed for the PCB to allow verification across a wide-range of operating conditions. The input capacitance is split such that about half the capacitors are at the input terminal where the external supply connects to the PCB and the other half at the drain of the devices. There is a non-zero resistance between these two points and splitting the capacitance helps ensure a more stable voltage during high current operation. The capacitors nearer the input terminal clean up noise from the benchtop supply while those near the switches provide transient current. The PCB layout is shown in Fig. 4.8.

The converter has five capacitors in parallel to reduce the loss attributed to the flying capacitance. R_{PCB} is determined by performing V-I measurements for the main conduction path. That is, a current source is applied and a Kelvin voltage measured. This is performed three times at three different currents, and then averaged. This is the DC resistance of the PCB. The capacitor resistance, R_{fly} is determined from the datasheet of the capacitor. The objective is not to develop the most efficient and power dense prototype, but rather to verify the model and characterize the parasitic elements. The model is later used to make highly

Table 4.1: Design parameters for 5 A SC converter

Component	Value
Gate Driver	LM5113
Switch	EPC2015C
f_{sw}	100 kHz
V_{out}	4 V
ΔV_o	0.4 V
C_{fly}	5x 4.7 μF
C_{byp}	80 μF
R_{on}	3.2 $m\Omega$
R_{PCB}	8.8 $m\Omega$
R_{flying}	$\frac{4}{5}$ mΩ

accurate design choices in Chapter 6. For example, the GaN devices where not optimized for conduction loss, switching loss, or area.

The design is tested up to 5 A and fits the predictive model very well and can be seen in Fig. 4.9. Typical waveforms also conform to simulation as shown in Fig. 4.10. The current is measured with the I-Prober 520 by Aim-TTI which measures the magnetic field induced by a current. Since the amplitude is sensitive to the orientation of the probe, and the probe is oriented by hand, only the waveshape is the most reliable information from the probe. The maximum readable current is 10 A.

The output impedance can also be determined experimentally by plotting the decrease in output voltage for increased output current. The slope is the R_{eff}. Fig. 4.11 shows both the load line for the model and for the experimental results, with a best fit line used to determine the experimental output impedance (slope). The difference between the model and experimental is less than 5 %.

The model is also verified over several operating points and with several flying capacitance values as shown in Figs. 4.12, 4.13, and 4.14. Here, the converter is tested in both SSL and FSL and near the self-resonant point of the flying capacitors. As the switching frequency increases, and the converter enters FSL, the model is less accurate due to parasitic inductance in the PCB trace and the current becoming more sinusoidal near the resonant frequency.

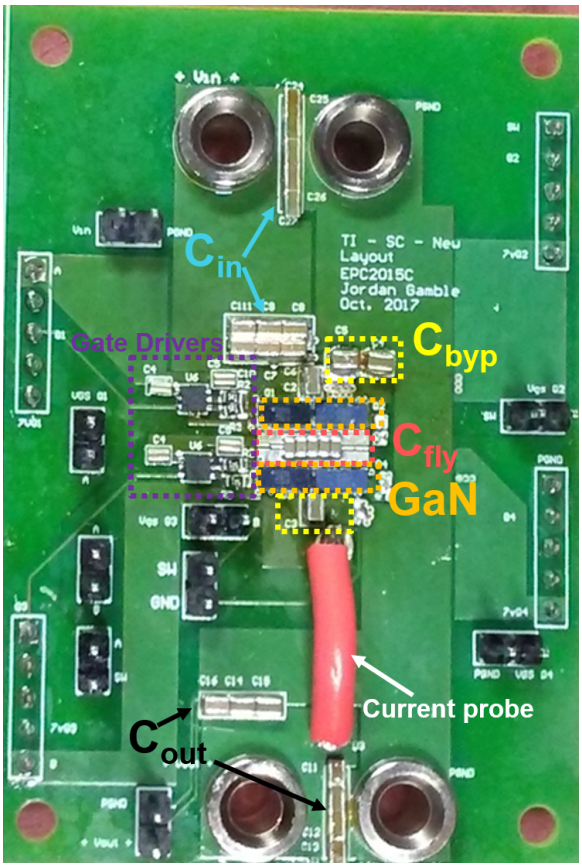


Figure 4.8: PCB for the 2:1 SC

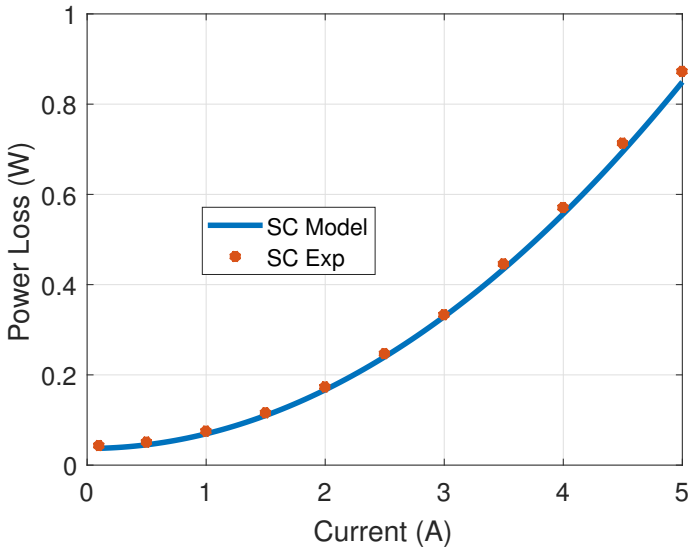
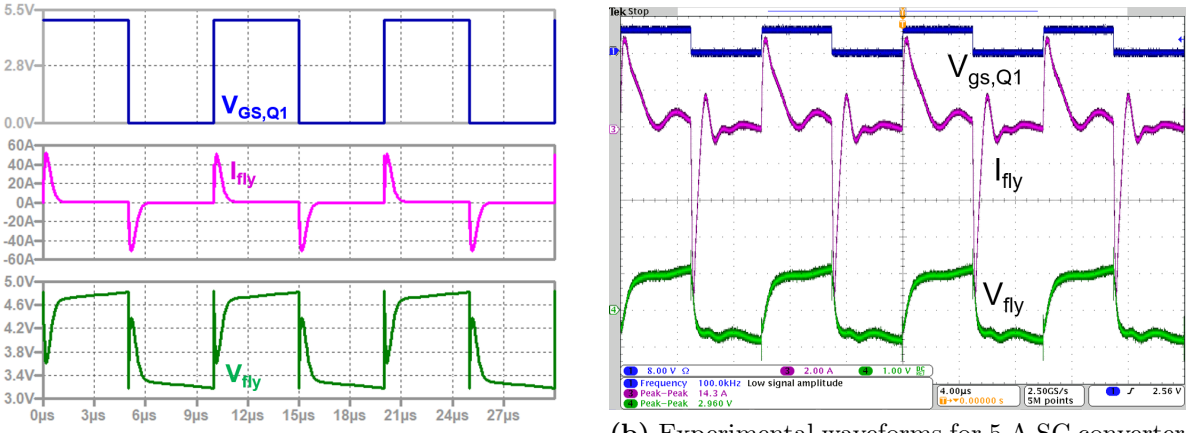


Figure 4.9: Power loss validation for the 2:1 SC



(a) Simulation of 5 A SC converter

(b) Experimental waveforms for 5 A SC converter

Figure 4.10: Simulation and experimental waveforms for the 5 A SC converter

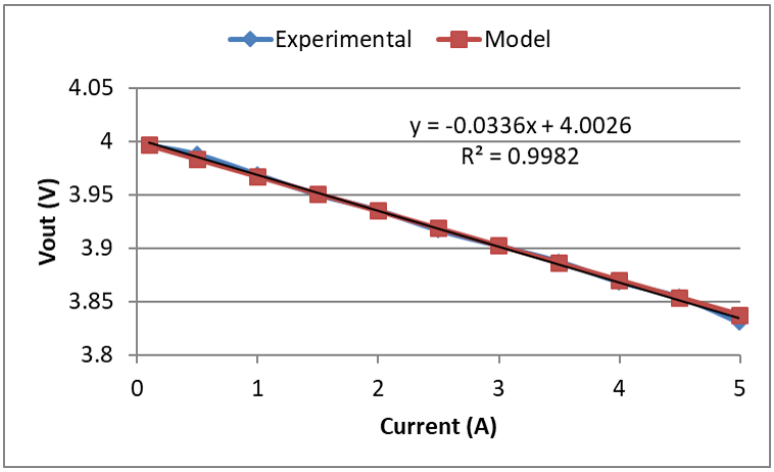


Figure 4.11: Experimental output impedance for the 2:1 SC

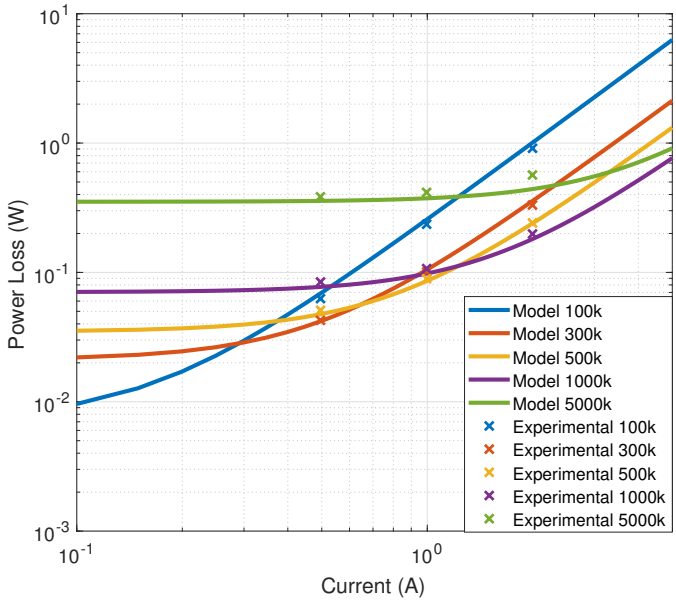


Figure 4.12: Loss model validation for 3 parallel capacitors at multiple frequencies. Resonant frequency 2.5 MHz

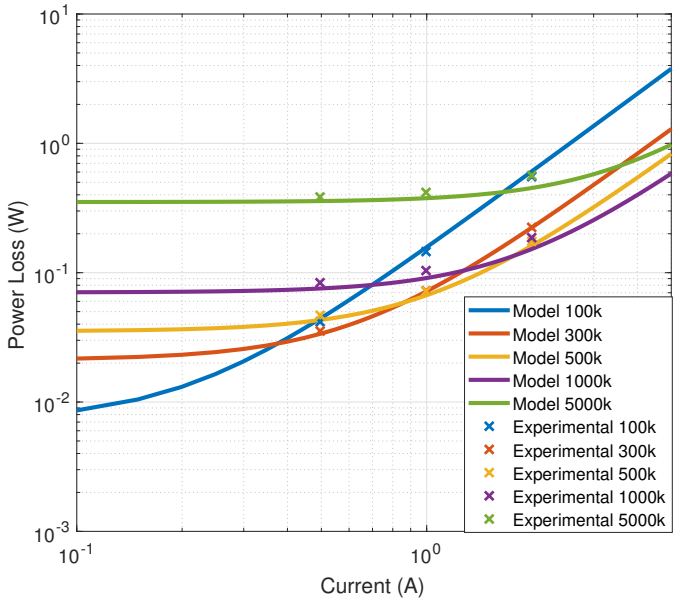


Figure 4.13: Loss model validation for 5 parallel capacitors at multiple frequencies. Resonant frequency 1.9 MHz

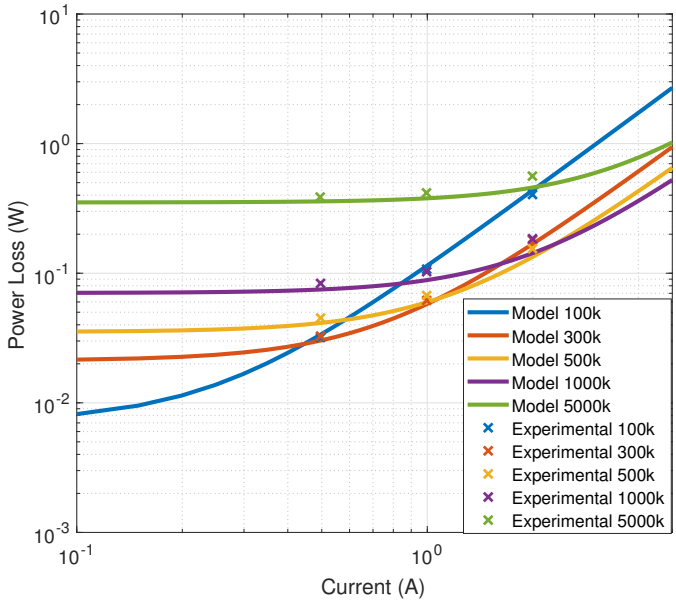


Figure 4.14: Loss model validation for 7 parallel capacitors at multiple frequencies. Resonant frequency 1.6 MHz

4.3 Impact of Paralleled C_{fly} on efficiency

The efficiency for a 10 A output is evaluated in both the ideal and derated case in Fig. 4.15. The solid lines are for a SC design that is optimized based on lowest loss and allowed to operate with impunity near the resonant frequency. The dashed lines are for the same design, except the 2 % deviation rule is in effect. In both cases, R_{eff} is recalculated for the paralleled capacitor, and the optimal frequency is such that the loss is minimized. The consequence of not considering the upper frequency limit can result in more than expected power loss. Although the two circuits have different constraints, the efficiency for both level-out at about ten parallel capacitors.

It might seem tempting to parallel as many capacitors as possible and increase the switching frequency until the lowest loss is obtained. However, by paralleling more capacitors, the slow-switching limit moves and the maximum frequency is reduced, as shown in Fig. 4.16. This assumes 14 $m\Omega$ of PCB resistance and sweeps the number of capacitors for a 10 A design. Higher efficiency is possible in the FSL if just looking at the equivalent lower R_{eff}, which could also be achieved with the ReSC, area permitting. The reason for the changing limit is seen in the next chapter, but suffice it to say, the ESR limit will be reached earlier (at lower frequency) as more capacitance shifts the SSL curve down.

4.4 Summary

The loss model for the 2:1 SC is presented as derived from literature. This model is then used to accurately predict the losses in an experimental set-up. A PCB is designed and characterized and incorporated into the model, as well the necessary parameters of the GaN devices used. The model is then experimentally verified over many operating points, using several values of C_{fly}. It is necessary to establish accurate models and understand their assumptions such that a design space over a wide range can be analyzed against the ReSC converter with confidence. A similar analysis is performed for the ReSC in the next chapter.

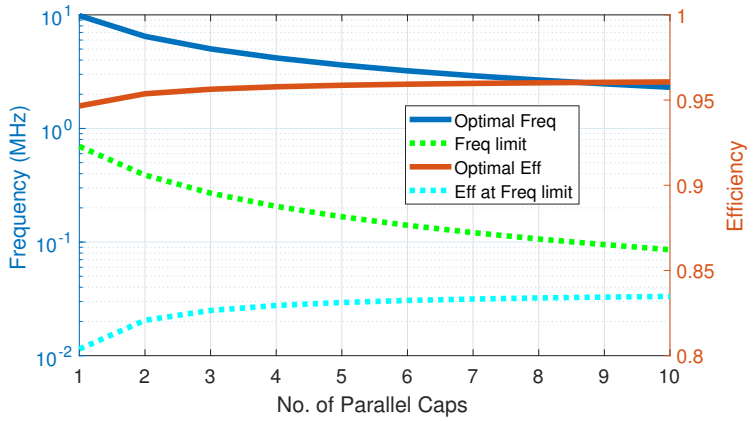


Figure 4.15: Efficiency and optimal switching frequency as a function of paralleled capacitors.

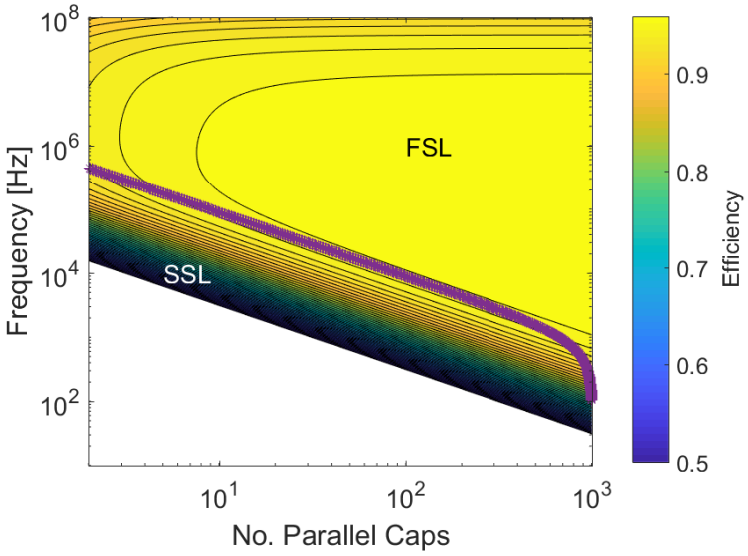


Figure 4.16: The SSL/FSL boundary for paralleling capacitors.

Chapter 5

Resonant Switched Capacitor

5.1 Introduction

In the FSL, the output impedance is at its minimum which improves efficiency but prevents the SC from being regulated by modulating the switching frequency. To reach this boundary, the switching frequency needs to be substantially increased from SSL operation, increasing switching losses due to C_{oss} as well as gate-drive losses. As mentioned earlier, the FSL may be unreachable if the parasitic elements cause the self-resonant frequency to occur before the SSL/FSL boundary. The Q from parasitics however will be too low for full resonant operation, as well being poorly controlled. A larger flying capacitor can also be used to decrease the output impedance, but the total area of the converter will increase. To assuage this detriment and operate with a lower R_{eff} at a lower frequency, an inductor can be placed in the path of the flying capacitor, and the converter operated at the resonant frequency. This is known as the Resonant Switched Capacitor [108]. The high energy density of capacitors can be better utilized in resonant mode and the inductor can be significantly reduced compared to the buck converter [86].

5.2 Topology Description

The quality factor, Q, will quantitatively determine the benefit of using the ReSC. As shown in Fig. 5.1 ([2]) R_{eff} can be reduced by Q times at a frequency Q times lower compared to a similar SC design.

The output impedance is normalized to the parasitic ESR, assuming equal ESR for both converters. The switching frequency is normalized to the SSL/FSL boundary. The same flying capacitance is also assumed. For the ESRs shown, the relative merit of the ReSC begins to take shape, as a function of quality factor.

The ReSC can either be indirect or direct as determined by inductor placement and is shown in Fig. 5.3 and Fig. 5.4 with their respective waveforms in Fig. 5.2 [80].

The current in the direct ReSC has a DC component. At high frequencies, inductor losses will be dominated by frequency dependent mechanisms such as skin-affect and core loss. If the spectral content of the current is concentrated at these frequencies, then greater loss occurs since the equivalent ac resistance is higher than the dc resistance. The benefit of the direct topology is that, since it has a dc component more of the power loss in the inductor will occur due to the DCR, while the other fraction is due to ACR. Since the DCR can be well-designed to be lower in magnitude than the ACR, the effective series resistance is reduced, even though there is still power loss due to harmonics. The indirect topology has

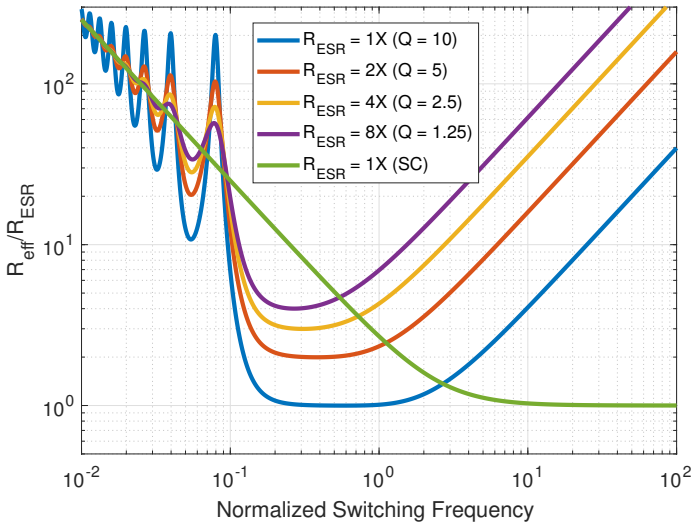


Figure 5.1: Effective Output impedance for the 2:1 SC and ReSC [2]

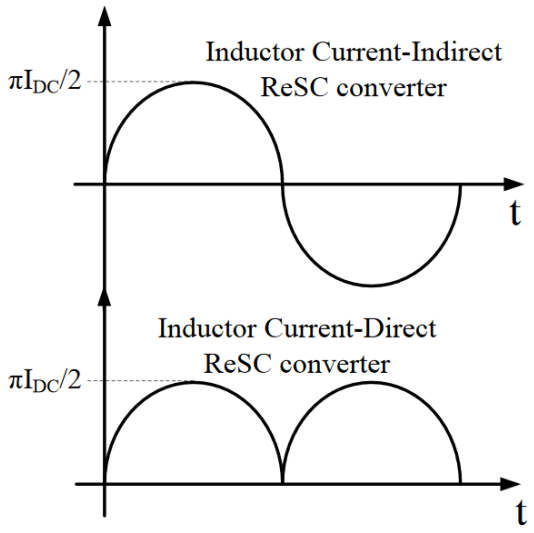


Figure 5.2: Inductor waveforms for the direct and indirect ReSC [80]

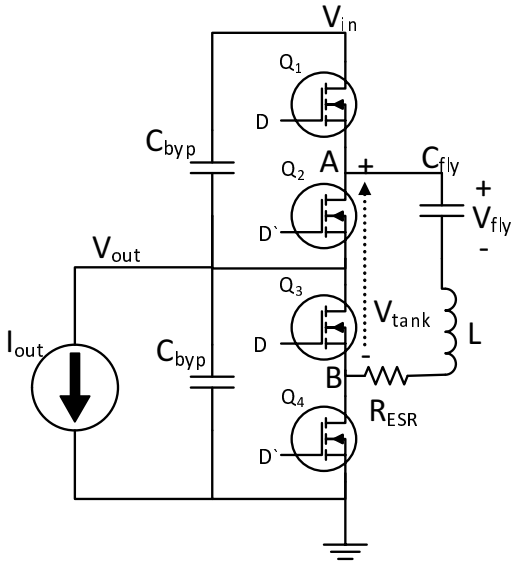


Figure 5.3: Indirect 2:1 ReSC circuit

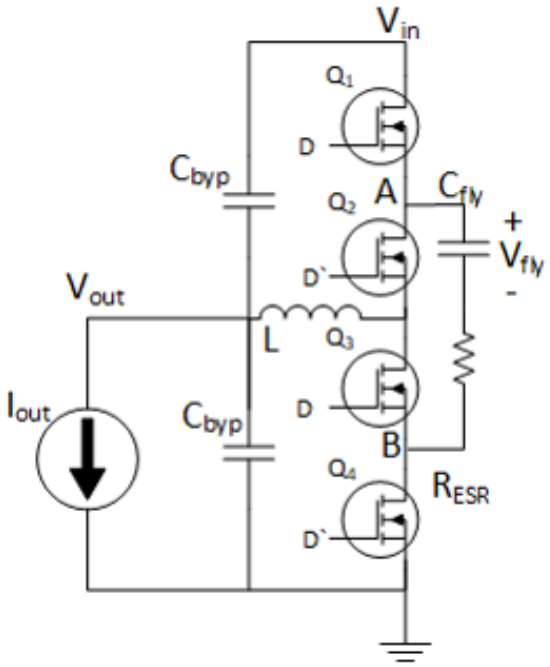


Figure 5.4: Direct 2:1 ReSC circuit

no dc component (or harmonics), which means that all of the current is concentrated at the resonant frequency, resulting in a larger effective resistance [80]. The power loss due to the inductor neglecting core loss is then:

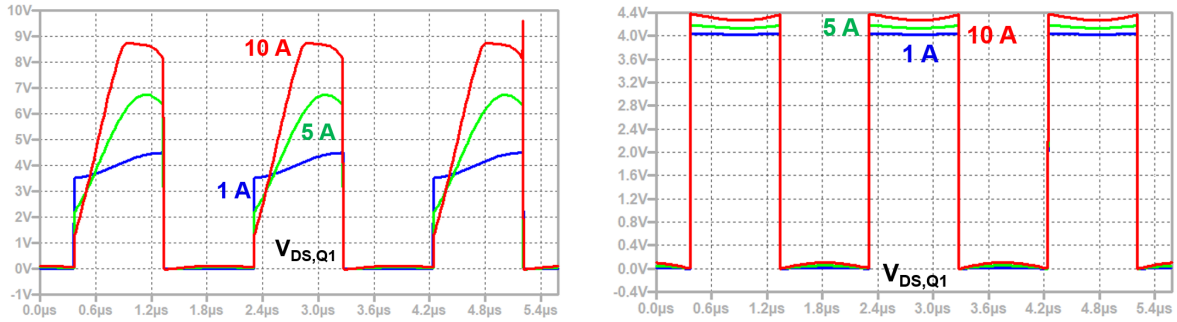
$$P_L = I_{DC}^2 DCR + ACR\left(\frac{\Delta I}{2\sqrt{2}}\right)^2 \tag{5.1}$$

An additional benefit to the direct topology is the variable duty cycle that can be utilized without a severe reduction in efficiency [109, 80]. For these reasons, the direct topology can also be seen as a merged two-stage topology (2:1 step-down of SC followed by variable duty cycle buck converter), or similar to the quasi-resonant 3-Level buck.

The main drawback of the direct ReSC is that the voltage blocking requirement of the devices increases with load current. This is especially problematic in integrated solutions where using the lowest rated MOSFET is desired to reduce the on-state resistance. This effect is shown by simulation for a $V_{out} = 4\ V$ converter in Fig. 5.5.

As the current increases from 1 A to 10 A, the voltage blocking requirement is over 2 times larger than the indirect. Calculating the C_{oss} loss is also increased due to the asymmetrical waveform reaching a higher peak voltage. In this way, the direct ReSC would not take advantage of the 0.5 V_{in} device rating in the 2:1 converter as the indirect ReSC can when compared to the buck.

The reason this occurs is shown in Fig. 5.6. For the indirect ReSC, the voltage across the flying capacitor and the voltage across the inductor are 180 degrees out of phase and so



(a) V_{ds} of the direct ReSC

(b) V_{ds} of the indirect ReSC

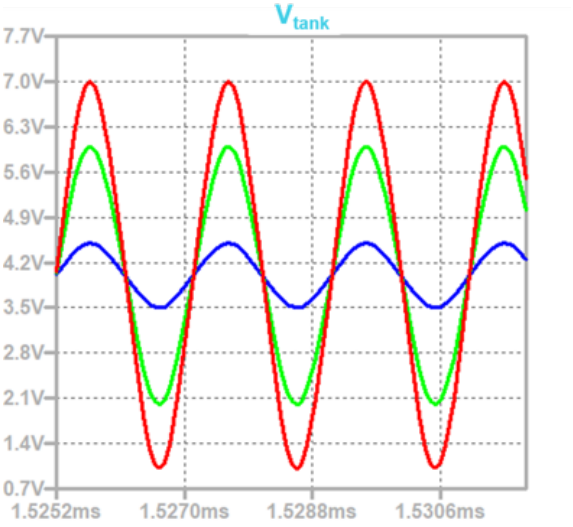
Figure 5.5: V_{ds} stress for 1 A, 5 A, 10 A, load current

cancel each other out, from the perspective of V_{tank}. The voltage across the tank is only the DC bias plus some ripple due to the ESR in the loop. For the direct ReSC, these two voltages do not cancel. The current through C_{fly} is sinusoidal and proportional to the output current. As the current increases, the voltages from node A to B increases. For these reasons, the indirect topology is considered for this analysis.

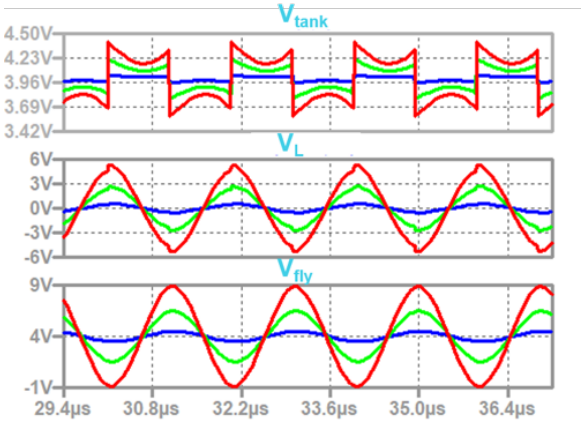
The ReSC has the same gate signals as the SC. However, to achieve zero-current switching (ZCS) the switching frequency must be that of the resonant frequency of the tank. It is well-known that the step-response to an under-damped RLC circuit is a sinewave that dampens over time around its DC operating point. The peak of this wave is in the first oscillation. By continuously stimulating the tank, the inductor current will be a sustained, purely sinusoidal waveform. Since the DC current in a series RLC circuit is zero, the oscillation will cross zero amps every half-period, with a period being defined as:

$$T = \frac{1}{f} \tag{5.2}$$

$$f = \frac{1}{2\pi\sqrt{LC_{fly}}} \tag{5.3}$$



(a) V_{tank} (node A to node B) of the direct ReSC



(b) V_{tank} of the indirect ReSC

Figure 5.6: V_{tank} variation for 1 A, 5 A, 10 A, load current

Or, the resonant frequency. The gate drive waveforms and inductor current are shown in Fig. 5.7 for the indirect ReSC.

In low voltage, high current applications ZCS is more beneficial than ZVS (zero-voltage switching), since the power loss due to C_{oss} is significantly smaller, especially if using GaN, and the circuit becomes conduction loss dominated, as discussed in Chapter 3. ZCS will reduce electromagnetic interference and maintain waveshape integrity, which is needed for loss reduction and regulation. ZCS is one innate advantage of the ReSC over the SC. However, complete integratability is not possible due to the inductor, although this inductor can be much smaller than in a traditional buck converter since it is not intended to filter but resonant. A more complex model for the output impedance of the circuit is required to account for the inductor.

The output impedance can be simplified at resonance in the case of Q >2, where the ReSC will be of most use [17].

$$R_{eff} = \frac{\pi^2 R_{ESR}}{8} \tag{5.4}$$

Where R_{ESR} is the sum total of the series resistances of every element in the current path. In [110] it is further expanded to include a wider-range of operating modes, that is, sub-harmonic frequencies.

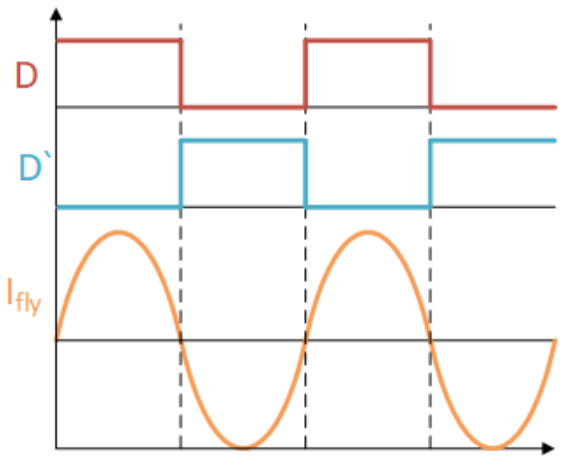


Figure 5.7: Gate and current waveform for the indirect ReSC

$$R_{eff} = \frac{1}{4C_{fly}f_s}\left(\frac{\sinh\left(\frac{R_{ESR}}{4Lf_s}\right)+\frac{R_{ESR}}{4\pi Lf_{res}}\sin\left(\frac{\pi f_{res}}{f_s}\right)}{\cosh\left(\frac{R_{ESR}}{4Lf_s}\right)-\cos\left(\frac{\pi f_{res}}{f_s}\right)}\right) \tag{5.5}$$

Since the ReSC is intended to be operated solely at the resonant frequency, (5.4) is sufficient for calculating conduction loss due to the output impedance. A high-Q circuit will have a narrow bandwidth which means that the output impedance will have a steep increase at frequencies near the resonant. When analytically determining the bandwidth (5.5) is of most use since it describes the output impedance at frequencies larger than the resonant. Additionally, this expression can also be used to capture behavior in the SC converter due to parasitic inductance. However, since the Q in the SC is typically below 0.5, it is sufficiently accurate to use (4.1) for simplicity.

The output impedance for the ReSC and SC is shown in Fig. 5.8. Included as well is the resonant frequency of the ReSC and the FSL boundary of the the SC. For the ReSC, R_{eff} will be $\frac{\pi^2}{8}$ times larger than the DC resistance since the current has a higher rms value than in the SC. Even so, the frequency reduction compared to the FSL will net significant savings in switching losses. It is also safer to push the operating frequency higher (in order to reduce the inductance) since the Q is large and any parasitic inductance in the layout will have minimal influence.

It is well known that the peak current in an underdamped series RLC circuit is:

$$I_{pk} = \frac{V_i}{\omega_o L}e^{\frac{-R\pi}{4L\omega_o}} \tag{5.6}$$

Where V_i is the initial voltage on the flying capacitor, R is the series resistance and ω_o is the radial frequency. For well designed, high-Q circuits where the series resistance is very small, the exponential factor will approach one as the resistance goes to zero. Further, simplifying the coefficient at the resonant frequency defined in (5.3), the equation can be simplified as:

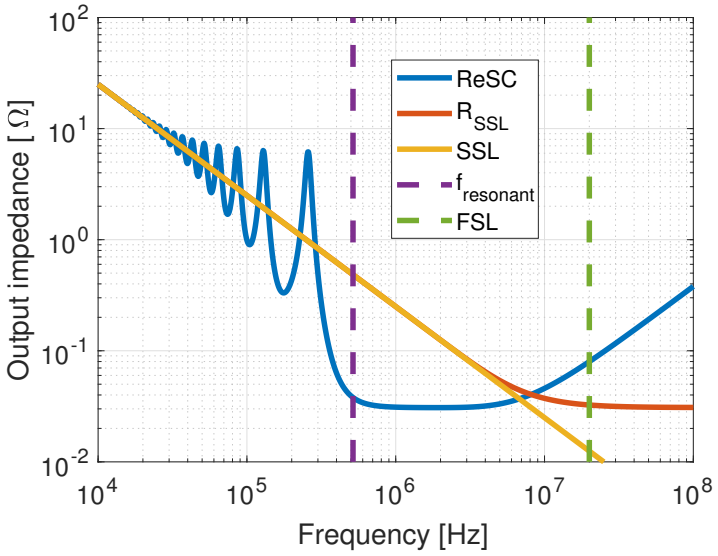


Figure 5.8: Effective output impedance for the SC, ReSC

$$I_{pk} \approx V_{out}\sqrt{\frac{C}{L}} \tag{5.7}$$

The maximum DC output current of the ReSC can also be determined from modifying the expression in [111] to include only operating at the resonant frequency.

$$I_{out} = \frac{V_{in}}{\pi}\sqrt{\frac{C}{L}} \tag{5.8}$$

Essentially (5.8) is a scaling the tank admittance, which is the inverse of the characteristic impedance designated r_o. The characteristic impedance needed for a given current can be calculated and is shown in Fig. 5.9 for a 95 nH inductor. As expected, more capacitance yields higher current capability which will also occur are lower frequencies, improving switching loss.

Off-the-shelf inductors can have varying tolerances and some derating for large DC currents. This will affect the ReSC in the same way as switching either slightly above or slightly below the resonant frequency. ZCS will be lost and impact the efficiency depending on the output current and by what margin the ZCS event is missed. For this reason it is

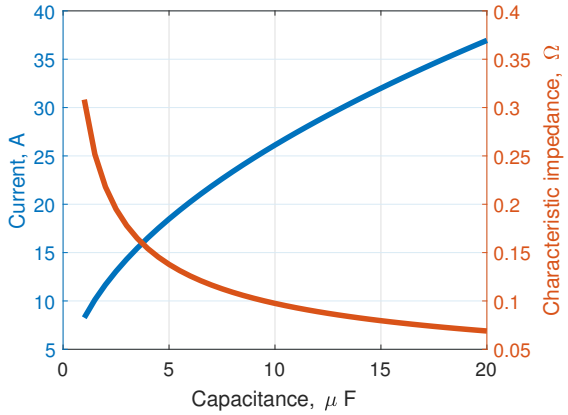


Figure 5.9: Current capability of the ReSC as a function of capacitance

very important to tune the switching frequency to achieve lowest loss, which needs to be done experimentally. Using an inductor with a Q that is lower will also be more forgiving, since the bandwidth will be wider, but the losses will be higher.

5.2.1 Inductor comparison to buck converter

Although not strictly a fair comparison as the inductors in both converters serve a different purpose (in the buck, the inductor is meant to filter), it can be shown that the standard equation for the output inductor of the buck can be evaluated for 2:1 operation with the same ripple as the ReSC and require 2.46 times larger inductance.

Starting from the inductor sizing equation in [112]

$$L_{buck} = \frac{V_{in} - V_{out}}{2\Delta I_L} D T_s \tag{5.9}$$

Assuming constant 2:1 operation, D = 0.5 and $V_{in} = 2V_{out}$.

$$L_{buck} = \frac{V_{in}}{8\Delta I_L} T_s \tag{5.10}$$

The current ripple in the ReSC is $\frac{\pi}{2} I_{dc}$ as shown in (5.3). Designing for equal ripple in the buck, yields

$$L_{buck} = \frac{V_{in} T_s}{4 I_{dc} \pi} \tag{5.11}$$

If the inductor in the buck operates with the same period of $T_s = 2\pi\sqrt{L_{buck}C}$ as in (5.3), (5.11) becomes

$$L_{buck} = \frac{V_{in}\sqrt{L_{buck}C}}{2 I_{dc}} \tag{5.12}$$

Finally, rearranging for L_{buck}:

$$L_{buck} = \frac{V_{in}^2 C}{4 I_{dc}^2} \tag{5.13}$$

Rearranging (5.8) for an expression of the inductance for the ReSC the ratio of two inductors is expressed as

$$\frac{L_{buck}}{L_{ReSC}} = \frac{\pi^2}{4} \tag{5.14}$$

The inductance for the buck is about 2.46 times larger than for the ReSC. Of course, operating a single-phase buck converter with the same inductor ripple as the ReSC is atypical since there will be harmonic content that needs filtering and so the inductance of the ReSC is an even smaller fraction of the conventionally-designed filter inductor of the buck. The output capacitor of the buck can also be designed to perform more of this filtering, but those details are beyond the scope of this work.

5.2.2 Bypass cap sizing

Optimizations previously highlighted study total area, trading off between the flying capacitance and the switches. But in a real circuit there will also be the bypass capacitors

and an input capacitor as well. For the structure shown in Fig. (5.3) where the input capacitor is referenced to ground and the bypass caps are from the output to ground and the input to the output, an area optimization can be found for dividing the area among the three capacitors. This is investigated in [76] in an integrated context. It is shown that the minimum output ripple occurs when the input capacitance is about 1.3 times larger than the bypass capacitors, assuming both bypass capacitors are equal.

The input and output ripple are given as:

$$\Delta V_{in} = 0.363 \frac{I_{out,dc}}{C_t f_{sw}} \tag{5.15}$$

$$\Delta V_{out} = 0.457 \frac{I_{out,dc}}{C_t f_{sw}} \tag{5.16}$$

Although for this work the area allocated to the input and output capacitor is not constrained since the converter is meant to operate over many conditions and configurations. In determining a final design for a given application, bypass capacitor sizing is needed to optimize power density.

5.2.3 Loss model

The conduction loss is the same as was calculated for the SC in (4.5) except that R_{eff} is calculated according to (5.4). The C_{oss} loss will also be the same as (4.6) since only ZCS is achieved, though the total loss is reduced. The ZCS benefit is manifested in the resonant valleys of the impedance as shown in Fig. (5.8). As the ReSC makes use of an inductor, both the core and AC losses need to be accounted for.

The ACR of the selected inductor is determined by connecting it to an impedance analyzer, out of circuit, and performing an AC frequency sweep as shown in Fig. 5.10. The resistance for the selected frequency is about 6.7 $m\Omega$, and the DCR according to the data sheet is 0.34 $m\Omega$, which is negligible.

The inductor is also a ferrite and so it will have core loss. As the current in the inductor is sinusoidal, the Steinmetz parameters should be very accurate. The parameters are extracted by selecting two points at the same frequency and different ΔB and then a third point at

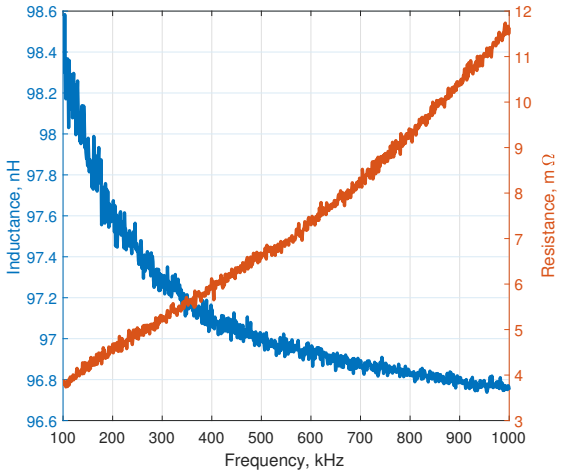


Figure 5.10: Inductance and AC resistance of the ICE inductor

the same ΔB as the first, but a different frequency. This forms a set of equations that are solved simultaneously yielding the Steinmetz coefficients. This are then used to find the core loss at each current.

With an extra component that typically suffers from either high DCR or ACR, the relative benefit of the ReSC is limited, as Q will be reduced proportionally. The benefit of using an inductor for a given loss parameter is analyzed in Chapter 6.

5.2.4 Model Validation

The loss models derived above are validated experimentally using EPC GaN. A single power stage is laid out with area allotted for paralleling capacitors. The design is summarized in the Table 5.1.

The inductor used is by ICE components, LP02-101-1. It has a saturation current of 40 A with a maximum current inductance drop of only 15 %, and a DCR of 0.34 $m\Omega$ [113]. The input and output capacitances are over-designed for the PCB to allow verification across a wide-range of operating conditions. The converter has three capacitors in parallel to reduce the loss attributed to the flying capacitance. R_{PCB} is determined by performing V-I measurements for the main conduction path as explained in Chapter 4. This is the DC resistance of the PCB. The model is later used to make highly accurate design choices in

Table 5.1: Design parameters for 5 A ReSC converter

Component	Value
Gate Driver	LM5113
Switch	EPC2001
f_{sw}	530 kHz
L	95nH
C_{fly}	3x 0.33 μF
C_{byp}	80 μF
R_{on}	3.2 $m\Omega$
R_{PCB}	14.5 $m\Omega$
R_{flying}	$\frac{20}{3}$ mΩ
$R_{L,AC}$	6.7 $m\Omega$

Chapter 6. For example, the GaN devices where not optimized for conduction loss, switching loss, or area.

The PCB layout is shown in Fig. 5.11.

The design is tested up to 5 A and fits the model very well and can be seen in Fig. 5.12. Typical waveforms also conform to simulation as shown in Fig. 5.13a and Fig. 5.13b.

The output impedance can also be determined experimentally by plotting the decrease in output voltage for increased output current. The slope is the R_{eff}. Fig. 5.14 shows both the load line for the model and for the experimental results, with a best fit line used to determine the experimental output impedance. The difference between the model and experimental is less than 5 %.

The model is also verified over several operating points and with several flying capacitance values as shown in Fig. 5.15. Here, the converter is tested at different resonant frequencies (by varying C_{fly}) and equivalent capacitor ESR as summarized in Table 5.2. The actual switching frequency is not exactly as calculated due to capacitor derating, slight variation in the inductor, and uncharacterized loop inductance. The resonant frequency is always determined experimentally by tuning the switching frequency until ZCS is achieved.

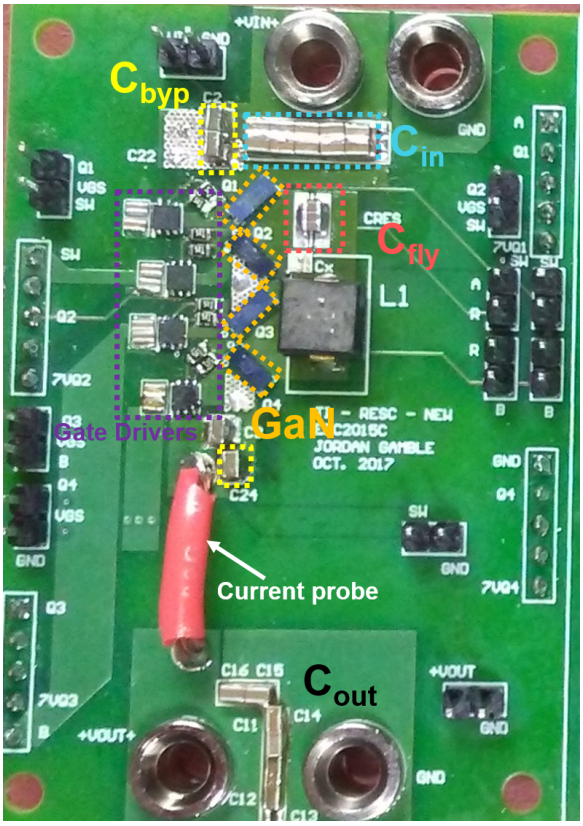


Figure 5.11: PCB for the 2:1 ReSC

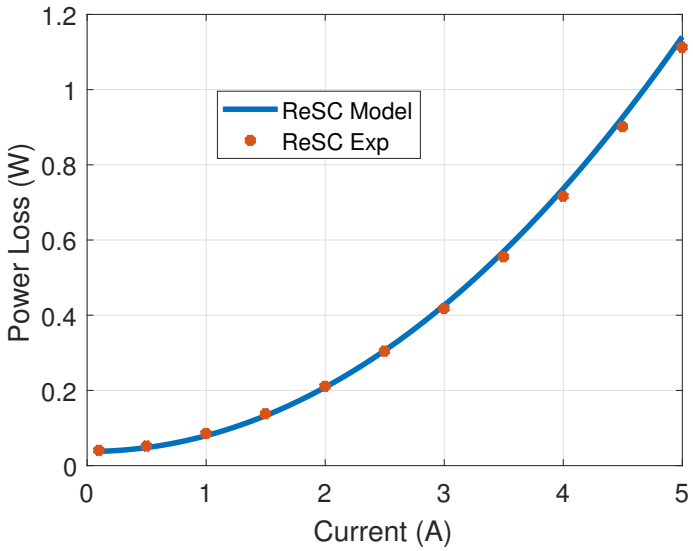
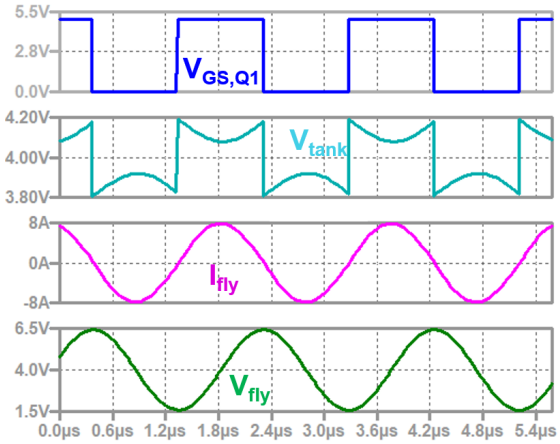
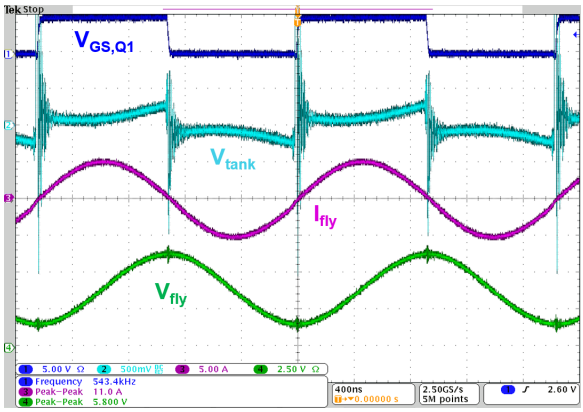


Figure 5.12: Power loss validation for the 2:1 ReSC



(a) Simulation waveforms for the ReSC



(b) Experimental waveforms of the ReSC at 5 A

Figure 5.13: Simulation and experimental waveforms

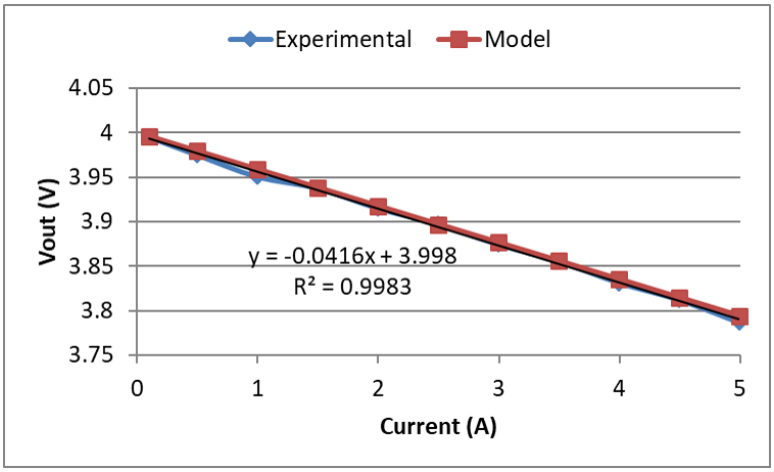


Figure 5.14: Experimental output impedance for the 2:1 ReSC

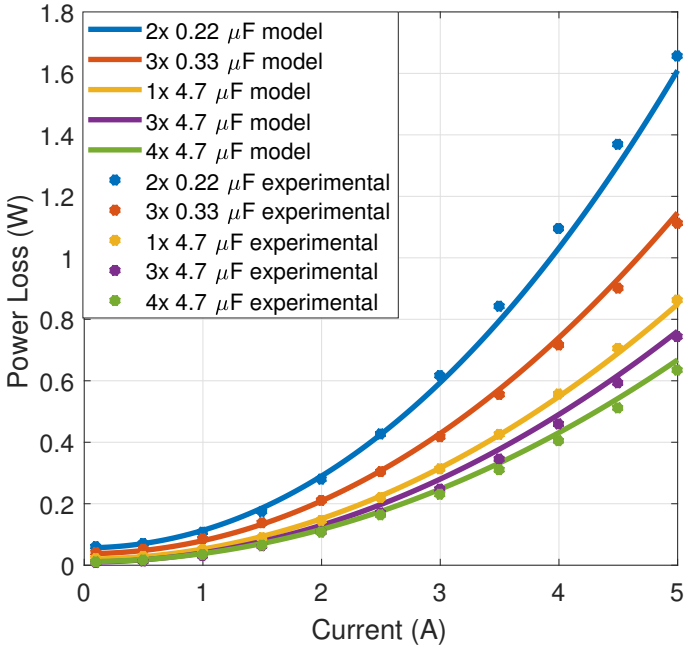


Figure 5.15: Loss model validation for 3 parallel capacitors at multiple frequencies

Table 5.2: Equivalent capacitor ESR and resonant frequency used to verify ReSC model

Capacitor	ESR	Resonant Frequency
2 x 0.22 μF	10 $m\Omega$	800 kHz
3 x 0.33 μF	6.6 $m\Omega$	533 kHz
1 x 4.7 μF	4.0 $m\Omega$	285 kHz
3 x 4.7 μF	1.3 $m\Omega$	166 kHz
4 x 4.7 μF	1.0 $m\Omega$	133 kHz

5.2.5 Current Regulation

Since the resonant frequency is fixed in the ReSC, typical PWM methods of voltage regulation are not possible. The technique described here is similar to pulse skipping or pulse density modulation, also called pulse frequency modulation. The technique is popularly implemented in so-called dual mode converters that use PWM for nominal operation and PFM for light load regulation in order to improve efficiency [114]. The resonant frequency remains unchanged, instead the switching frequency is modulated.

Regulation by tank cycling

For the first method a third period in which the tank is shorted out is added after Phase II, as shown in Fig. 5.16, with waveforms shown in Fig. 5.17.

A similar approach for variable output voltage was proposed in [86], except the switching order is Phase I, Phase III, Phase II, which suffers from hard switching transitions. The method here more closely resembles that in [88].

Phase I and Phase II are the typicaly resonant period used in the previous section. In Phase III, the tank is shorted by turning on Q_2 and Q_3 after the resonant period and until the end of the switching period. The duration of this short will determine the delivered output current. The switching period is now defined as the length of these three intervals. A shorter interval will deliver more resonant energy to the load per second, where a longer

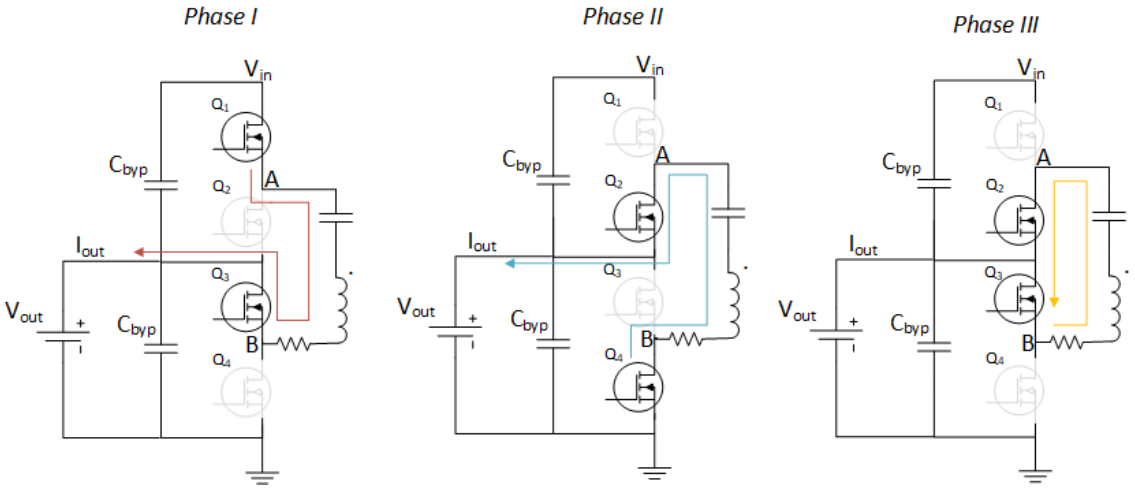


Figure 5.16: ReSC circuit configuration for current regulation by shorting the tank

third interval will decrease this energy per second and thus decrease the output current. This third period is here referred to as the cycling interval since the tank energy circulates, being lost only to parasitics.

The DC output current can be determined by the amount of energy per time in the resonant pulses. In a single pulse, the capacitor voltage oscillates from 0 to V_{in} every period, there are two pulses (one positive, the other negative) per period. The current in the typical ReSC, where the switching frequency is the resonant frequency, is a pure sine wave with an amplitude as shown in Fig. 5.2. The total charge per half-period is:

$$q = \int_0^{\pi} i(t)\,\mathrm{d}t \tag{5.17}$$

$$q = \int_0^{\pi\sqrt{LC}} I_{pk} \sin\left(\frac{t}{\sqrt{LC}}\right) \mathrm{d}t \tag{5.18}$$

$$q(t) = \left(-I_{pk}\sqrt{LC}\cos\left(\frac{t}{\sqrt{LC}}\right) + Const.\right)\Big|_0^{\pi\sqrt{LC}} \tag{5.19}$$

At $t = 0$, $q = 0$, and using the expression (5.7) for I_{pk}, the charge in one half-period is:

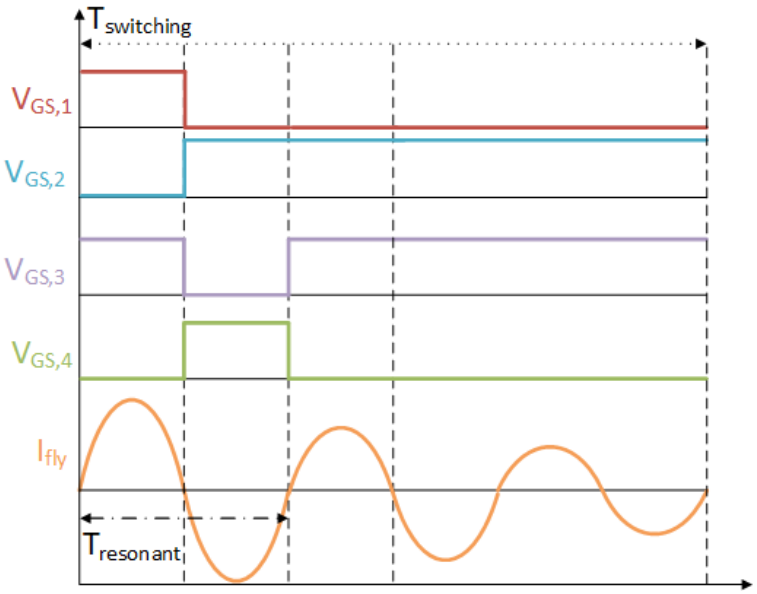


Figure 5.17: ReSC circuit waveforms for current regulation by shorting the tank

$$q = V_{in}C_{fly} \tag{5.20}$$

Multiplying (5.8) by $\frac{\pi}{2}$ to substitute for I_{pk} yields the same result. Setting $T = \frac{1}{f_{res}}$ and for two-half periods in the unregulated ReSC, (5.8) can be adapted for additional half-periods (D). When the switching frequency is longer than the resonant frequency, the total period with which to divide the charge, q, by is:

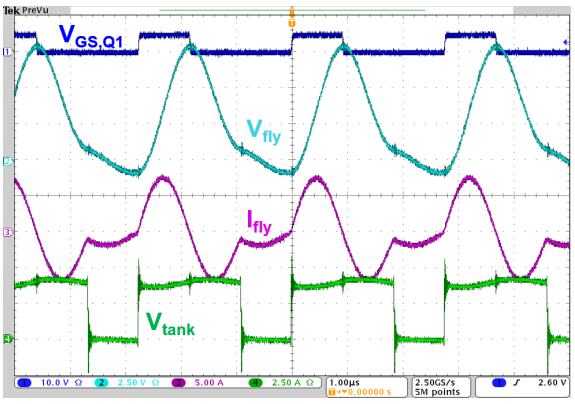
$$T_D = \frac{1}{f_{res}} + \frac{D}{2f_{res}} \tag{5.21}$$

So the output current is:

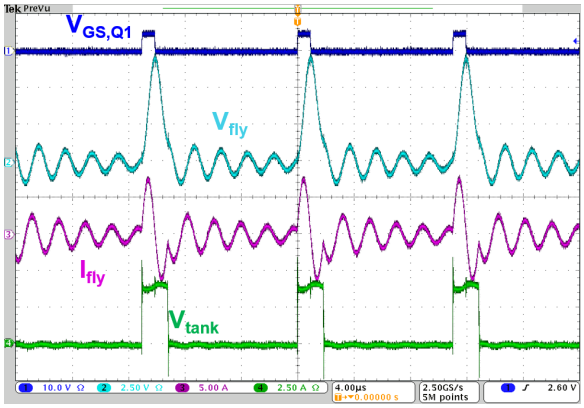
$$I_{reg} = \frac{2q}{T_D} \tag{5.22}$$

This is also used in [88]. The DC output current is then regulated by adjusting the total period, or, resonant half-cycles in the cycling interval. Since the output current is not a function of the ESR, the output current and efficiency should be independent of the series resistances, similar to the SC in SSL. As shown in Fig. , the inductor current will be negative for the first added half-cycle. This is because at the end of the discharge phase as the current becomes more negative and approaches zero the voltage across C_{fly} is positive. As Q_2 and Q_3 are turned on, C_{fly} is now in parallel with the inductor. The voltage across the inductor reverses polarity, opposing the voltage across C_{fly} such that the tank voltage is now zero. This reversal of polarity causes the inductor current to flow "out of the dot", that is, negative. In a similar way of thinking, since the capacitor is now DC shorted, the current will flow from the positive terminal (at the drain of Q_2) through the inductor to the negative terminal.

The tank current will now continue to ring out to zero as shown in 5.18b when the switching period is much longer than the resonant period. The power loss can be measured

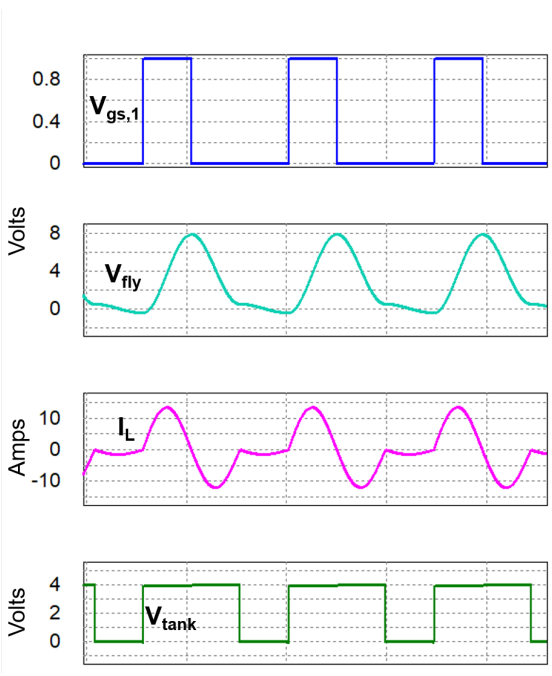


(a) Period extended to include one additional half-cycle

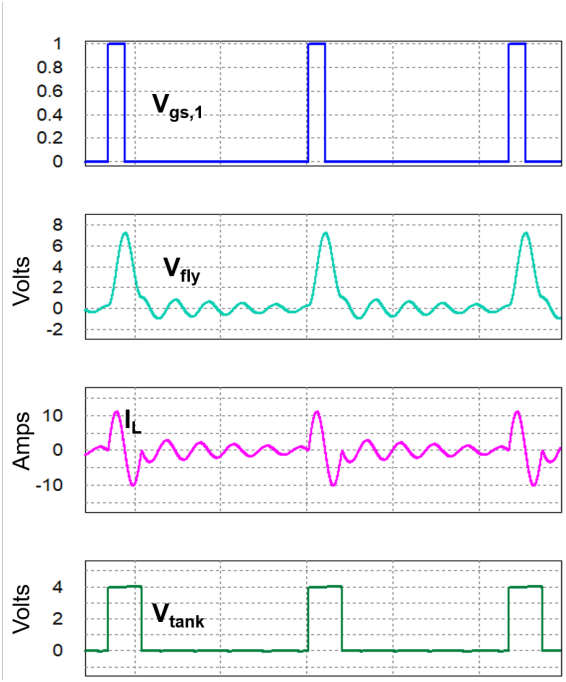


(b) Period extended to include ten additional half-cycles

Figure 5.18: Experimental current regulation using cycling half-periods



(a) Simulation of one additional half-cycle



(b) Simulation of ten additional half-cycles

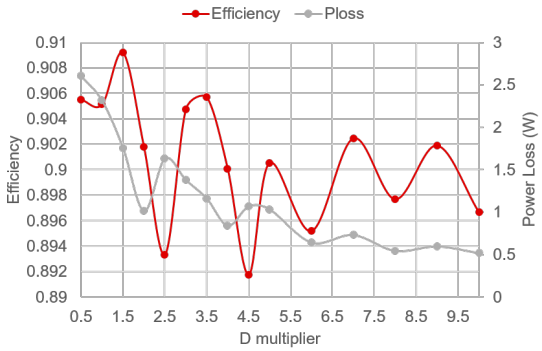
Figure 5.19: Simulation of current regulation using cycling half-periods

by connecting the output of the converter to a voltage source set to $\frac{V_{in}}{2}$, and making Kelvin measurements to the input and output power, subtracting the difference. The period is then increased in intervals of half D, that is, half-cycles. The results are plotted in Fig. 5.20a, with the calculated and measured output current in Fig. 5.20b.

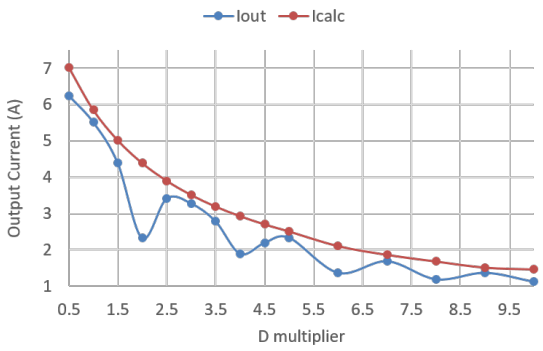
Most notable are the dips in efficiency that result in dips in output current for even multiples of D. This occurs when the inductor trajectory is decreasing and the zero-current crossing is missed. At the zero-current, the voltage across C_{fly} is phase-shifted by 90 degrees and is non-zero. When the resonant period begins again, the initial condition of the V_{fly} is no longer zero, and so a periodic error occurs which manifests itself as lost energy. This lost energy is than not transferred to the output, which decreases the current.

Also of note is that for a change in output current of 1 - 6 A, the efficiency varies by less than 1 %. There is however a general downward trend, although it does not affect the overall power loss much since the energy in the tank during these intervals is comparatively lower than in the charge and discharge cycle. This is further helped by low DC losses in the circulating path.

Constant power at the output can also be maintained by modulating the number of half-cycles with a variable input voltage. This can be useful for USB 3.0 Power delivery to maintain optimal operating efficiency by varying V_{in} as needed [5] [62] [115]. This effect is shown in Fig. 5.21a and Fig. 5.21b.

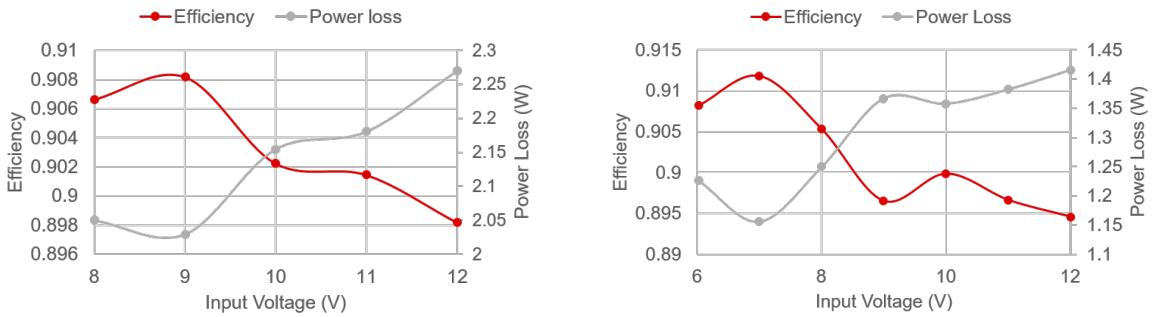


(a) Experimental Efficiency and Power loss



(b) Experimental output current

Figure 5.20: Experimental validation of cycling method



(a) 20 W output power **(b)** 12 W output power

Figure 5.21: Constant output power for variable input voltage, first method

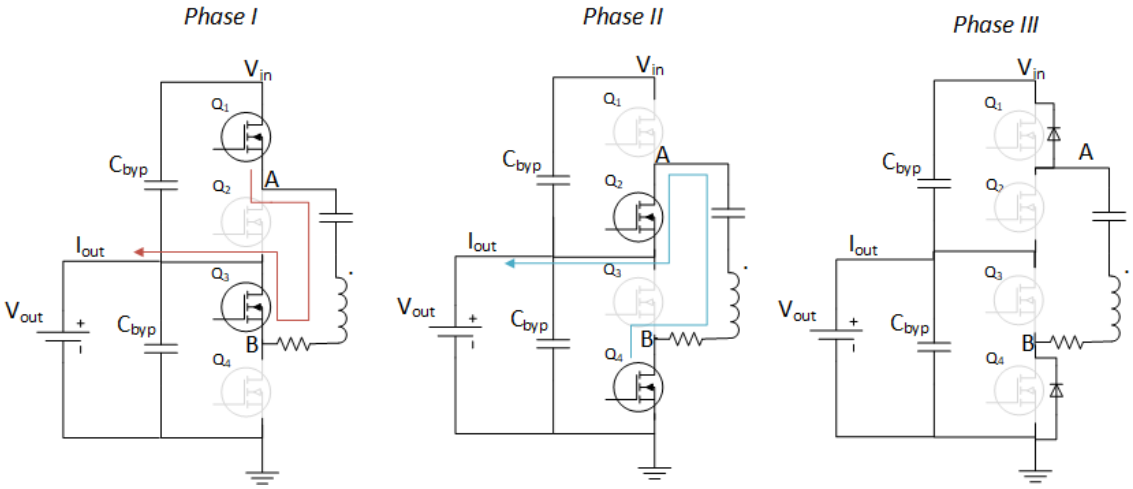


Figure 5.22: ReSC circuit configuration for current regulation by DOTM

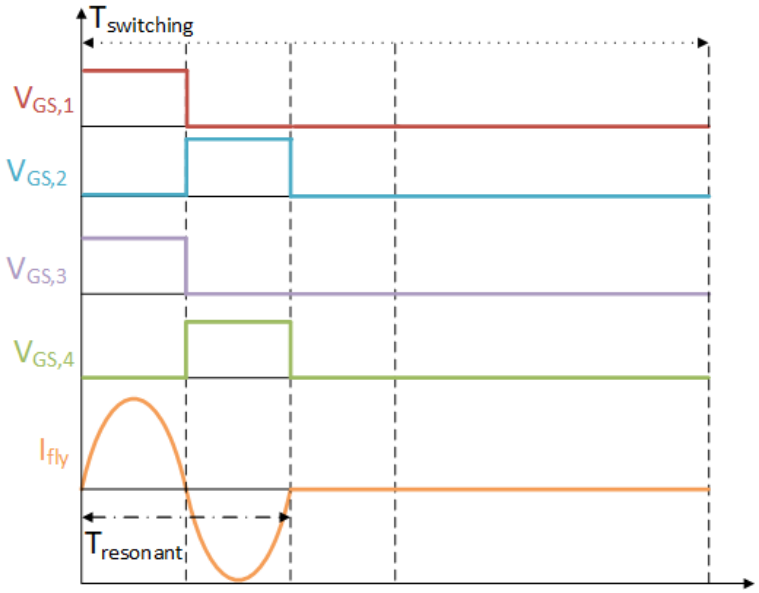


Figure 5.23: ReSC circuit waveforms for current regulation by DOTM

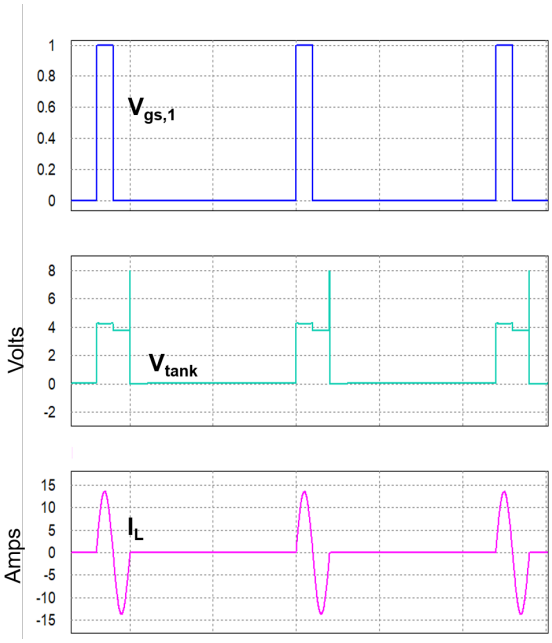
Regulation by opening the tank

This method is also known as dynamic off-time modulation (DOTM). The switches are in the off-state after the resonant period and the tank becomes an open circuit. This method is similar to Pulse-Density Modulation (PDM), except that, the envelope of pulses contains only a single pulse [116]. The off time is still adjusted to regulate the output. Instead circulating the tank current in the third phase in Fig. 5.16, all of the switches are turned off as shown in Fig. 5.22 with waveforms in Fig. 5.23. Analytically this is the same as the first method, so all of the same equations apply. A simulation of this is performed in Fig. 5.24a, with an experimental waveform in Fig. 5.24b zoomed into to show the inductor current. In both cases, the inductor current does not perfectly reach zero, and so some ringing occurs. The current path is completed by turning-on the equivalent body diode of Q_1, that in GaN is referred to as 'reverse conduction'. Although this is lossy, it proves to be less lossy than the first method. At the end of the resonant period, there is a non-zero voltage across the flying capacitor. The first method shorts the tank and the energy on the capacitor is dissipated in the series resistance. This method utilizes reverse conduction, which would have higher loss if conducting for the same time interval. The time spent in this phase is much shorter than the switching period and the energy (minus the reverse conduction loss) is recovered as the inductor current passes through Q_1 and into the input supply. In the cycling method, all of the extra tank energy is lost.

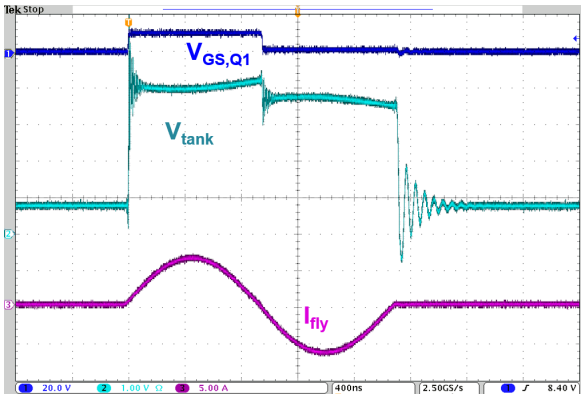
Here the electronic load can be set to a constant voltage equal to the nominal step-down minus the voltage drop at full output current due to the output impedance. That is:

$$V_{E-load} = V_{out} - I_{max} R_{eff,ReSC} \tag{5.23}$$

Where I_{max} is the full rated current with $D = 0$ from (5.8). Setting V_{E-load} to this constant then allows regulation by varying the period as in the cycling method. The experimental results are presented in Fig. 5.25. The same output current is used for these results as for the cycling method. The efficiency is relatively flat considering it varies only

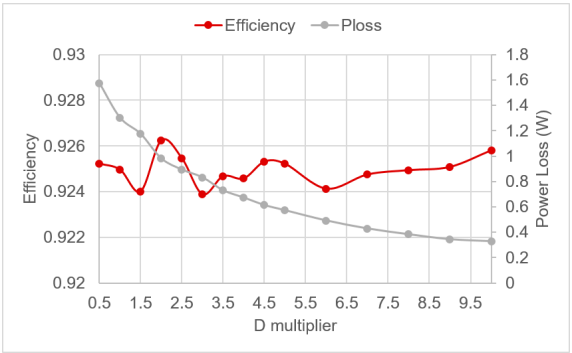


(a) Simulation

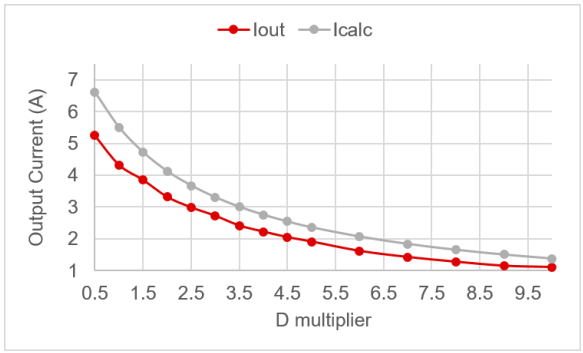


(b) Experimental

Figure 5.24: Current regulation by DOTM



(a) Experimental Efficiency and Power loss



(b) Experimental and calculated output current

Figure 5.25: Experimental Validation of DOTM

±0.1 %. It is also about 2 % more efficient than the cycling method. The output current does not experience any dips and is offset from the calculation by a constant.

Common to both methods is an increase in efficiency by increasing the output voltage. Since the configuration is 2:1, the input voltage must also increase, which is possibly with USB-PD. Since the switching loss of the GaN is so low, the output voltage can be increased with little regard to the C_{oss} loss. This is demonstrated in Fig. 5.26. Of course, if the load has a narrow window of voltages that it can safely operate with, a second stage is needed to maintain a constant output voltage.

The switching period can be regulated to maintain a constant output power for various input voltages as shown in Fig 5.27a for 20 W and Fig 5.27b for 12 W. The variation in efficiency is wider than for the cycling method, but the efficiency is also higher overall.

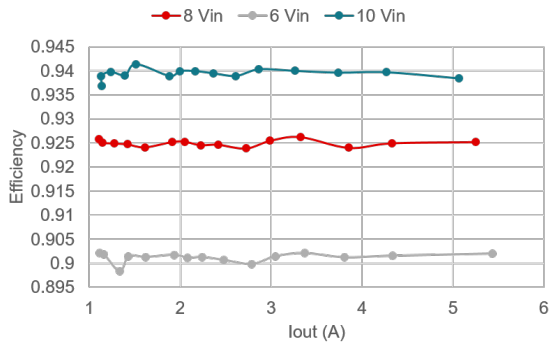
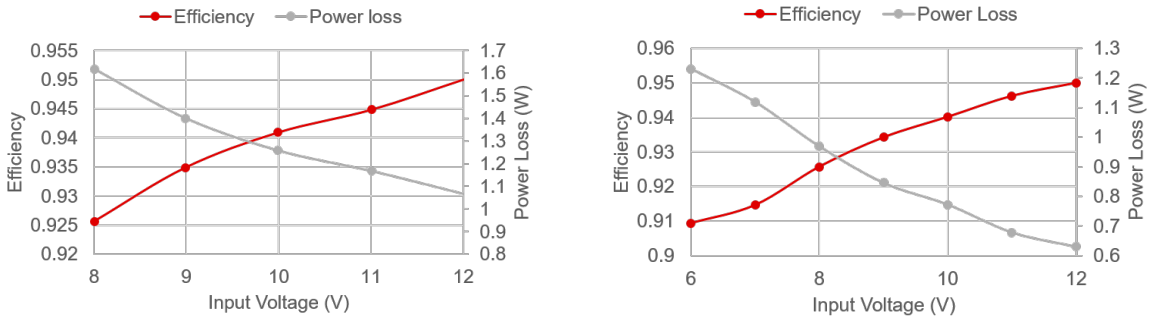


Figure 5.26: Efficiency improvement by increasing the input voltage



(a) 20 W output power

(b) 12 W output power

Figure 5.27: Constant output power for variable input voltage, DOTM

5.3 Summary

The loss model for the 2:1 ReSC is presented as derived from literature. This model is then used to accurately predict the losses in an experimental set-up. A PCB is designed and characterized and incorporated into the model, as well the necessary parameters of the GaN devices used. The model is then experimentally verified over many operating points, using several values of C_{fly}. It is necessary to establish accurate models and understand their assumptions such that a design space over a wide range can be analyzed against the ReSC converter with confidence.

The use of current regulation in the ReSC to enable such applications as battery charging is also explored. Two methods are explored, one where the energy is circulated in the tank and another where all of the devices are turned off. The first method exhibits an odd behavior where the current at even intervals of D dip below the expected value. The efficiency is flat at around 90 % up to 6 A. The second method improves the efficiency to about 92.5 % without any dips in the output current. In addition, the gate drive scheme is more forgiving since without the proper resolution for precise zero-current crossing at the end of the switching period, the inductor current and flying capacitor voltage always decay to zero. The power loss penalty due to missed zero-crossing is reduced as energy can be recovered. Both methods maintain their respective efficiency for constant output power, with an improvement in efficiency possible if the output power is increased for the same output current.

Chapter 6

Design Space

The previous chapters detailed the modeling techniques needed for predicting power loss of the SC and ReSC. The main circuit variables available for a discrete SC converter are the switching frequency, capacitance of C_{fly}, voltage ripple, output current, and when it makes sense to use the ReSC converter. These need to be balanced with area restrictions and efficiency targets. This chapter details a broad analysis of the converter that can be used by the design engineer to inform the trade-offs inherent in their application. For this reason, a design space is developed based on the converter modeling in the previous chapters. This methodology differs from others in that: 1), it looks only at discrete components, and 2), it examines the trade-off in inductor loss such that design can be evaluated based on any application.

6.1 Switched Capacitor Design Space

According to (4.3) a single output current is possible with fixed ripple, flying capacitance and frequency. Although not a specific requirement, in order to simplify our analysis, the ripple is set to be 10 % of the output voltage. Each capacitor has a derating that depends on a wide range of operating conditions such as the DC bias, AC ripple, temperature, frequency. The nominal capacitance also varies by 10 or 20 % (since there are so many factors, and it can be difficult to accurately predict how all of these influences will impact the final capacitance value). For this design space, only the derating due to DC bias is considered because it is

typically the most severe and, for the 2:1 SC, a bias of V_{out} is always applied across the flying capacitor.

The design space takes a derated standard value capacitance and determines its R_{eff} over a wide range of frequencies. Note that the parasitic inductance is not considered for this case. Each of these frequencies are then evaluated over a range of currents to calculate the efficiency of the converter. The circuit modeling is only valid for high efficiency designs, which is acceptable because all applications tend to desire high efficiency. The result is plotted in Fig. 6.3.

For this design, it is assumed that the converter will operate in SSL at any frequency. There are three trend lines to note. The pink dashed line represents the boundary at 0 % efficiency, where the output voltage is equal to the voltage drop due to the output impedance. The area below this line are invalid designs, where, R_{eff} is so large, and the output current so high, that no power can be delivered to the load. This is found by identifying two points along the boundary and applying the point-slope formula for logarithms.

The three dashed green lines are the asymptotes for a design that is at least 90 % efficient. The bottom green line operates in an area that is conduction loss dominated. The efficiency is then approximately

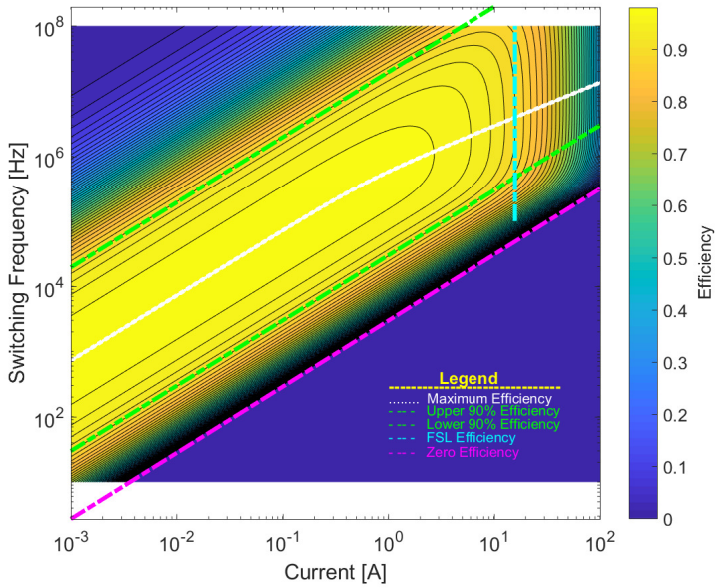


Figure 6.1: Switched Capacitor Design Space (0805, X5R, 15 μF)

$$\eta = \frac{V_{out}I_{out} - I_{out}^2 R_{eff}}{V_{out}I_{out}} \tag{6.1}$$

Using the SSL equation for the SC, the frequency that makes (6.1) is found for each current.

$$R_{eff} = \frac{1}{4C_{fly}f_s} \tag{6.2}$$

A similar approach is taken for the upper green dashed line. Here, conduction and C_{oss} losses are dominant. Equation (6.1) is augmented as:

$$\eta = \frac{V_{out}I_{out} - I_{out}^2 R_{eff}}{V_{out}I_{out} + P_{C_{oss}}} \tag{6.3}$$

The solution for the frequency becomes quadratic

$$f_s = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \tag{6.4}$$

$$a = \frac{4\eta C_{oss} V_{out}^2}{2} \tag{6.5}$$

$$b = V_{out}I_{out}\,(1-\eta) \tag{6.6}$$

$$c = \frac{I_{out}^2}{4 * C_{fly}} \tag{6.7}$$

The vertical dashed green line is representative of the converter in FSL, since the power loss becomes frequency invariant. Equation (6.1) can be used with the parasitic ESR of the circuit replacing R_{eff}, that is, R_{FSL} from (4.2).

The white dashed line represents the peak efficiency that can be obtained for each frequency and current pair. This trend line also accounts for conduction and switching loss, but unlike (6.3), SSL operation is not assumed. For this analysis (4.2) is used for R_{eff}. Regular hand analysis can render the equation into a 6^{th} order system by taking the

derivative of the losses and setting them equal to zero. Mathematica is used to determine the symbolic solution.

$$\frac{dP_{loss}}{df_{sw}} = \frac{d\left(I^2 R_{eff}\right)}{df_{sw}} + \frac{dP_{coss}}{df_{sw}} = 256p^2C^4R^2f_{sw}^6 + 16p^2C^2f_{sw}^4 - I_o^4 = 0 \tag{6.8}$$

Where p is the C_{oss} energy, R is the series resistance.

Selecting a point from Fig. 6.3, a numerical solution can be obtained. This solution can also be verified in Matlab by fixing the current and sweeping frequency. The solution is a parabolic curve whose peak is the maximum efficiency. As shown in Fig. 6.4 the results of both methods yield the same result.

If the design space is replotted limiting the R_{eff} to only the SSL, as explained previously using the 2 % deviation rule, the upper bound frequency becomes the SSL limit. This is plotted in Fig. 6.2. Since the flying capacitance is fixed, the SSL will be unchanged.

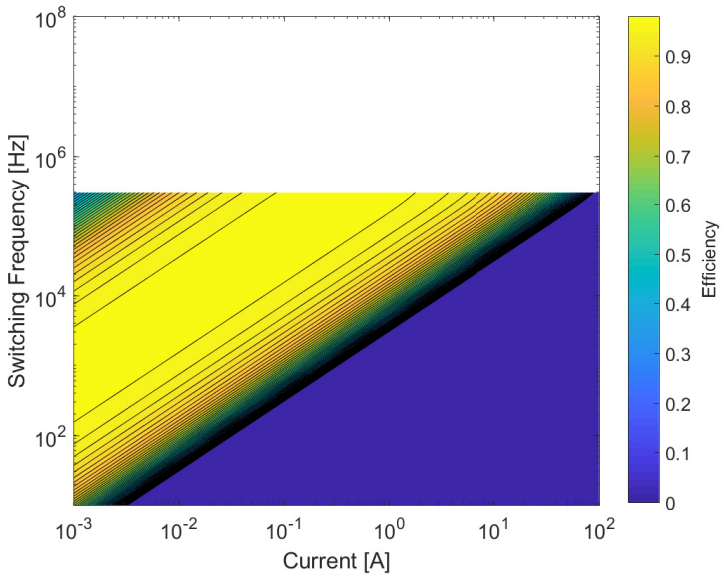


Figure 6.2: Switched Capacitor Design Space (0805, X5R, 15 μF), SSL

$$f_s = \frac{\sqrt{\left(\frac{-1}{C_{flyl}^2 R_{ESR}^2}\right) + \left(\frac{p^2}{R_{ESR}^2\left(-C_{flyl}^6 p^6 + 216C_{flyl}^8 I_{out}^4 p^4 R_{ESR}^4 + 12\sqrt{3}\sqrt{C_{flyl}^{14} I_{out}^4 p^8 R_{ESR}^4\left(-p^2 + 108C_{flyl}^2 I_{out}^4 R_{ESR}^4\right)}\right)^{\frac{1}{3}}}\right) + \frac{\left(-C_{flyl}^6 p^6 + 216C_{flyl}^8 I_{out}^4 p^4 R_{ESR}^4 + 12\sqrt{3}\sqrt{C_{flyl}^{14} I_{out}^4 p^8 R_{ESR}^4\left(-p^2 + 108C_{flyl}^2 I_{out}^4 R_{ESR}^4\right)}\right)^{\frac{1}{3}}}{C_{flyl}^4 p^2 R_{ESR}^2}}}{4\sqrt{3}}$$

Figure 6.3: Closed form expression for the frequency that corresponds to the highest efficiency for a given current

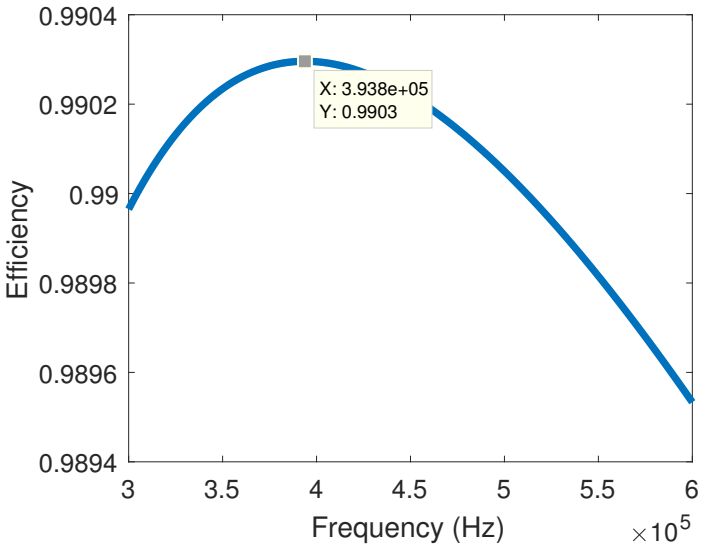


Figure 6.4: A particular Matlab Solution

6.2 ReSC

A similar approach is taken for the ReSC. For the same example capacitance used in the SC design space, the frequency and output current can be swept to obtain the efficiency. The frequency here is the resonant frequency and so also determines the inductance needed to achieve a given frequency. The output impedance uses (5.4) for Fig. 6.16a. This is the ideal design space for an inductor with no loss. An example of how the design space can change when including the AC resistance is given in Fig. 6.6b. The resonant frequencies for several inductors are indicated for reference.

A known 95 nH inductor was characterized with an impedance analyzer to obtain the AC resistance from 100 kHz to 1 MHz. The AC resistance is then normalized to the inductance. This is done because small inductors will tend to have less resistance in a given area, so this method assumes a constant Q. This data was plotted with a best fit line, and the resulting equation used to calculate the AC resistance at the frequencies in the design space. Although the resistance may not follow this trend for all inductors at all frequencies (especially for inductances far from 95 nH and for different materials), it gives a first order approximation to the upper frequency bound that restrains the ReSC design space. This plot is shown in Fig. 6.5.

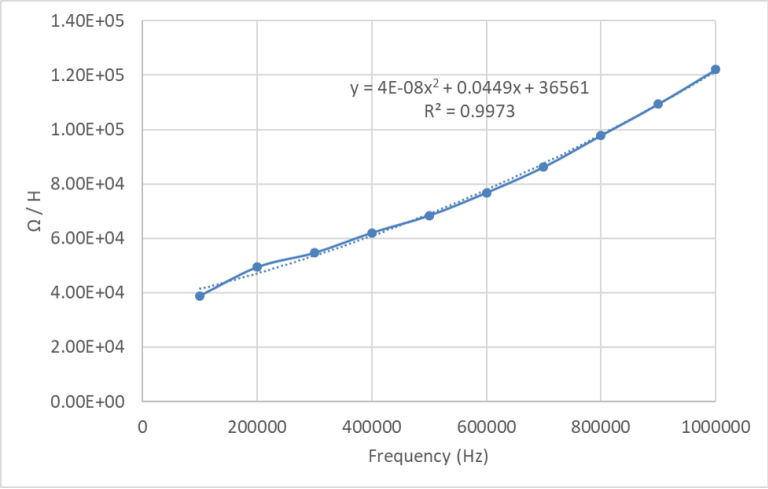
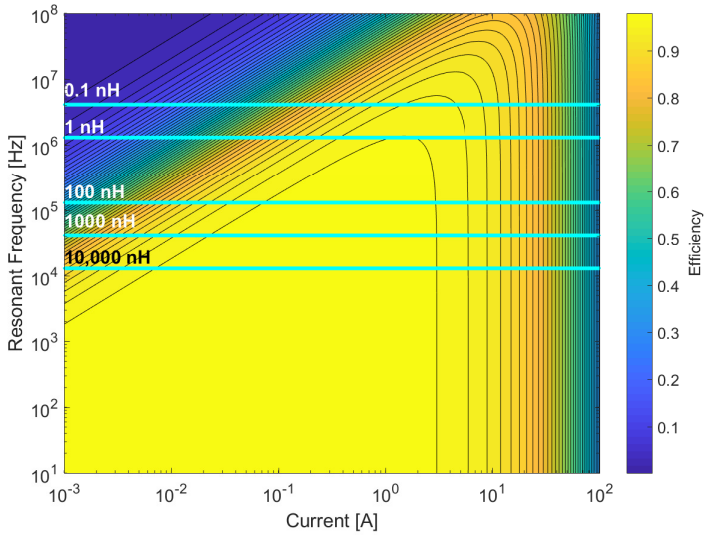
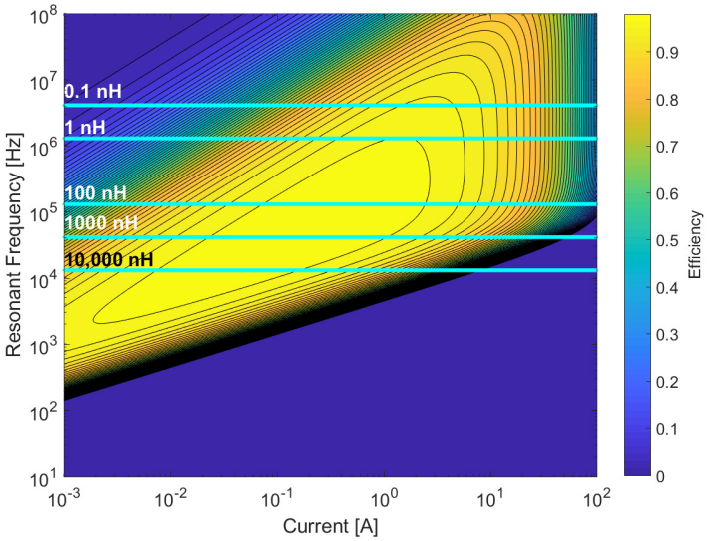


Figure 6.5: Normalized AC resistance for a particular inductor with best fit line



(a) Design space of the ReSC without inductor loss



(b) Design space of the ReSC with AC inductor loss

Figure 6.6: Design space of the ReSC (0805, X5R, 15 μF) with and without AC inductor loss

According to Fig. 6.6b there is a maximum inductance for a given output current that satisfies the high efficiency criteria. At low current and high resonant frequency, the switching losses will become dominate.

6.2.1 SC and ReSC Tradeoff

Now that the model has been validated experimentally as per Chapter 4 and Chapter 5 and a closed form expression for the maximum efficiency derived and validated for the design space, analytical techniques are employed to examine the tradeoff between the SC and the ReSC.

The typical motivation for high switching frequency is passive component reduction. High frequencies will require lower inductance for a given flying capacitor in the ReSC circuit. This trends with smaller footprint inductors. However, switching losses, including inductor-based losses will also increase. Lower frequencies will have comparatively larger magnetics, but lower switching losses. When constrained for a constant frequency, loss in the magnetics are also inversely proportional to the physical size, and so at lower frequencies, the inductor can be more efficiently utilized [99].

For the SC, lower frequencies result in higher R_{eff} and higher power loss assuming conduction loss domination. This can be mitigated at lower frequency by using larger C_{fly}, which proportionally reduces the R_{eff}. This comes at the cost of possible increase in footprint which is somewhat mitigated by standard packages. In Fig. 6.7 the output impedance of the SC is reduced for several capacitances and compared to the output impedance of the ReSC for a fixed inductor and increased capacitance.

Looking closer at the same plot where the flying capacitance of the ReSC and SC are the same, there is identified a ΔR_{eff} at the ReSC resonant frequency. This is the difference between the R_{eff} of the SC and the R_{eff} of the ReSC at that frequency. This is considered the typical improvement of the ReSC, where the output impedance is improved by Q times that of the SC at Q times lower frequency [17]. As the switching frequency increases for the SC, an improvement in conduction loss will erode the benefit of resonant operation. Since the ReSC will typically have higher resistance than the SC due to increased layout area for

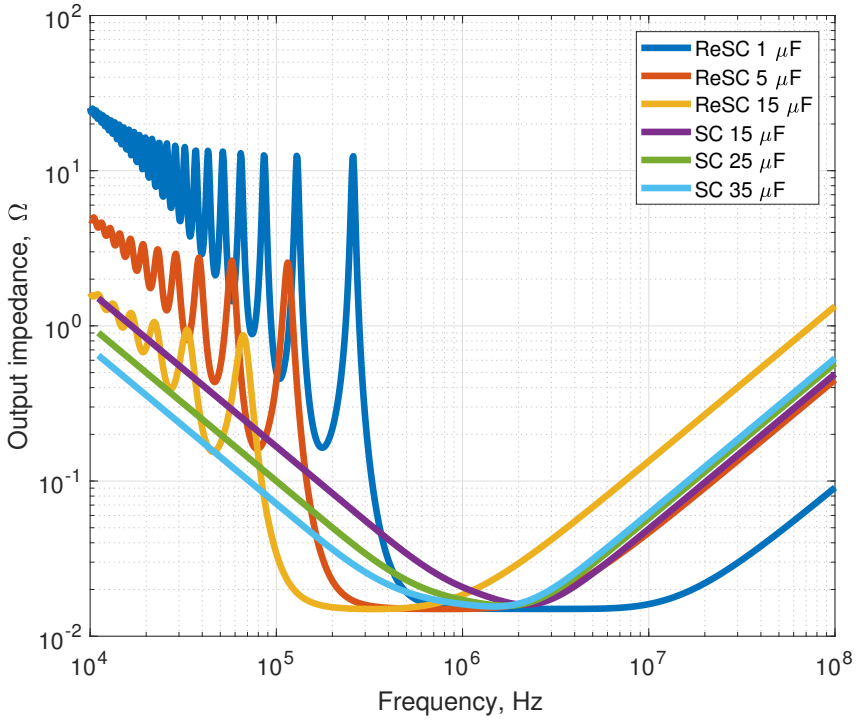


Figure 6.7: Overall improvement of operating in SSL with larger C_{fly}

the inductor and the AC resistance of the inductor, there will be a point where the R_{eff} will become lower than the ReSC before reaching the SSL. Where these two are equal, there is no benefit to the ReSC, as the loss will be the same but with more area allocated to the inductor. Conversely, increasing the flying capacitance of the SC at the resonant frequency, will also diminish the improvement in loss for the ReSC.

It is then useful for comparison to assign equal flying capacitance to both converters, since the area allocation for C_{fly} will be the same for both converters. In reality, the SC might need more physical capacitance to counteract the greater derating that will occur due to DC bias, whereas for the ReSC, the derating will be mostly to AC ripple amplitude shown in Fig. 6.9, which will increase the capacitance. This increase is then derated due to the temperature rise, with the net derating being near zero.

Further assuming that the same switches and gate drivers and other auxiliary components are used for both, any additional increase in area for the ReSC can be directly attributed to the inductor. Additional loss or improvement in loss will also be attributed to the inductor since extra PCB ESR for layout of the inductor and AC resistance can be lumped into the

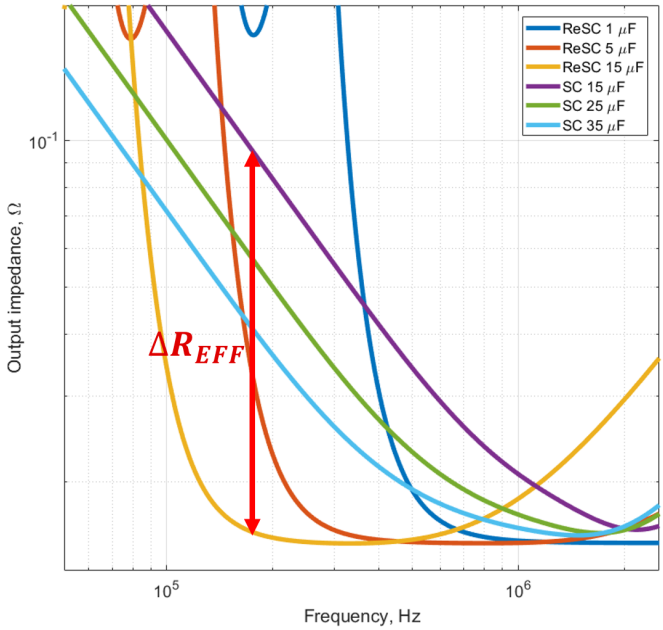
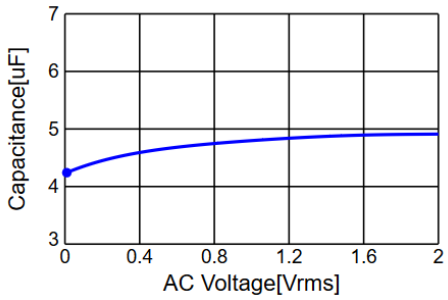
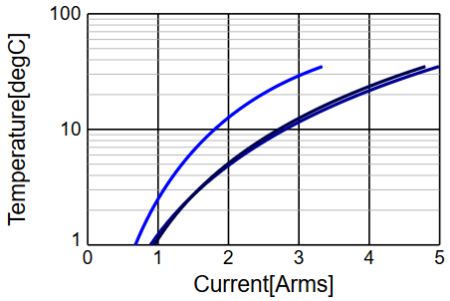


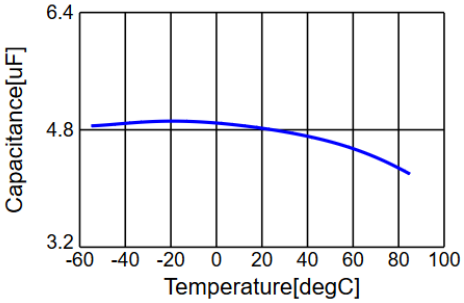
Figure 6.8: Overall improvement of operating in SSL



(a) AC voltage characteristics for a 0 DC bias



(b) Temperature rise from ripple characteristics



(c) Temperature derating

Figure 6.9: Characteristics of the 4.7 μF capacitor (GRM188R61C475kAAJ)

properties of the inductor. Core loss also need not be explicit since the total loss attributed to the inductor, whatever its source may be, will be seen in the difference in power loss between the two converters. The equivalent loss associated with inductor is modeled by a DC resistance and is denoted $R_{L,ESR}$. In [17] the following relationship is derived:

$$\frac{R_{eff,SC}}{R_{eff,ReSC}} = \frac{4Q_{ReSC}}{\pi} \tag{6.9}$$

Here we substitute (5.4) and (3.2) into (6.9) and obtain and an expression for the output impedance of the SC at the resonant frequency of the ReSC:

$$R_{eff,SC} = \frac{\pi}{2}\sqrt{\frac{L}{C_{fly}}} \tag{6.10}$$

We then define ΔR_{eff} as the difference between the output impedance of the SC and the output impedance of the ReSC, at the latter's resonant frequency.

$$\Delta R_{eff} = \frac{\pi}{2}\sqrt{\frac{L}{C_{fly}}} - \frac{\pi^2 R_{ESR}}{8} \tag{6.11}$$

Since the switching frequency for both converters is identical, and assuming identical switches and gate drivers, the switching losses not captured by R_{eff} will also be identical. The difference in power loss is then the difference in output impedance times the square of the current. In (6.11), the inductor is assumed to be lossless. In reality it will possess a DCR, ACR, and core loss. The core loss is determined use the Steinmetz parameters. This power loss is divided by the square of the current, yielding an equivalent resistance, R_{core}. The three resistance are then summed with any DCR resulting from PCB layout to give an equivalent resistance attributed to the inductor, R_L:

$$R_L = R_{PCB,L} + R_{DC,L} + R_{AC,L} + R_{core} \tag{6.12}$$

$$R_{core} = \frac{P_{core}}{I^2} \tag{6.13}$$

This method still requires characterizing the loss in any specific inductor but allows all of the complexities in inductor design to be reduced to one variable for analysis. ΔR_{eff} will be reduced by R_L as the inductor becomes less ideal. The maximum power loss due to the inductor is defined as the difference in power loss between the two converters being zero. This would mean that the non-ideal inductor is such that whatever benefit was targeted by using the ReSC to decrease output impedance has been canceled out due to the added component.

$$\Delta P = P_{SC} - P_{ReSC} \tag{6.14}$$

$$\Delta P = I^2 \Delta R_{eff} - P_L \tag{6.15}$$

$$P_{L,max} = I^2 \Delta R_{eff} \tag{6.16}$$

Equation (6.16) is the maximum loss that can occur in the inductor and still have the ReSC outperform the SC because any loss above this will result in the SC having lower conduction loss. When the inductor loss causes the ReSC and SC to have the same overall power loss, than any non-zero area the inductor occupies will dissuade the engineer from going resonant.

Equation (6.11) is verified experimentally. The flying capacitance for both converters is 15 μF and the inductor has been previous characterized. Operating both converters at the resonant frequency results in the model based R_{eff} shown in Fig. 6.10.

The power loss in both converters are then tested at 5 A, since the loss will be conduction-dominated. The power loss for each converter is calculated by subtracting the Kelvin-measured output power from the Kelvin-measured input power. So, substituting known values into 6.15 yields:

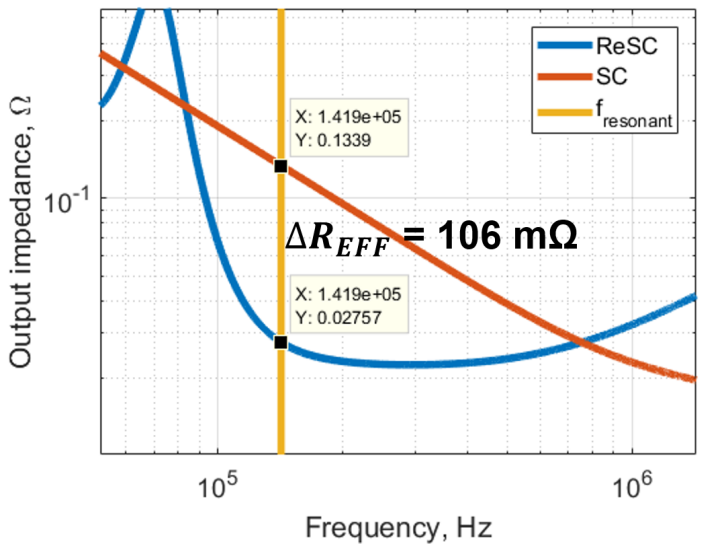


Figure 6.10: Model based output impedance for the SC and ReSC

$$2.6W = 5^2\Delta R_{eff} - \left(0.0032\ W + 5^2 3.7\ m\Omega\right) \tag{6.17}$$

$$\Delta R_{eff} = 104\ m\Omega \tag{6.18}$$

Where the difference in measured power loss is 2.6 W. The inductor loss is broken into core loss (0.0032 W) and the AC resistance (3.7 $m\Omega$) (the DCR for this particular inductor was negligible and R_{PCB} is already in the model from Chapter 5). The expected ΔR_{eff} based on the loss model is shown Fig. 6.10. The percent error is less than 1.8 %.

Revisiting (6.11), the ΔR_{eff} can be maximized for a minimum ESR in the ReSC. That is, well designed inductors and layout will lead to R_{ESR} being very small. For the experiment above, it constituted approximately 20 % of ΔR_{eff}.

A new design space for the inductor is developed that allows R_L to be evaluated in terms of efficiency improvement over the SC operating at the same frequency. This gives an easy way to determine if the extra area for an inductor can be justified from a power loss perspective. For a fixed capacitance, several resonant inductors are swept to find a series of resonant frequencies. Each of those frequencies will have a reference SC design; a reference R_{eff}. The output impedance of the ReSC is also determined from the values in Table 5.1 *plus*

the equivalent resistance attributed to the inductor, as discussed above. As this resistance increases, the efficiency of the ReSC will approach the SC. At large values of $R_{L,ESR}$, the efficiency of the SC is greater than the ReSC. This is modeled in Fig. 6.11 with the previous experimental operating point highlighted.

As described, $\Delta\eta$ is the difference in efficiency for the two converters at each operating point, where positive $\Delta\eta$ indicates the ReSC has lower loss and negative $\Delta\eta$ indicates the SC has lower loss. The highlighted operating point at $I_{out} = 5$ A, the efficiency of the ReSC will be about 13 *percentage points* higher than the SC operating at the same frequency. This is compared to the experimental result, found in Fig. 6.12, where $\Delta\eta = 13.5$ %.

The percent error is 1.5 %. This method is useful because it allows the designer to have total freedom over the inductors they can purchase or fabricate. Each inductor has an (L,R) point on Fig. 6.11 that can be used to inform if the added area is worth the improvement in efficiency for any general application. This method is further validated by investigating two additional operating conditions as highlighted in Fig 6.13.

Table 6.1 summarizes the results for all three inductors.

Another way of comparing the SC and ReSC is looking specifically at the power loss. Assuming the same number of parallel capacitors as before, an optimal SC converter is determined. This is done using the method discussed in Chapter 4 where the output impedance in the SSL deviates from (4.2) by 2 %. This is the greatest frequency and in turn the lowest output impedance for a fixed C_{fly}. For the circuit parasitics in Table 4.1 and four parallel capacitors, the switching frequency is 240 kHz. This optimal SC design is then compared to the power loss in the ReSC as a function of the inductor resistance in Fig 6.14.

The power loss of the ReSC is normalized to the loss in the optimized SC, which is noted by the white horizontal line. At low equivalent inductor resistances, the ReSC will have losses reduced by a factor of 70 %. At higher resistances, the loss associated with the inductor at 5 A will be too great and at 1 Ω the ReSC will have 15 times more loss than the optimized SC. This also includes the switching losses, namely just the loss due to C_{oss} since the converters are operating at different frequencies now. Several black lines highlighting different Q boundaries are shown for reference. These are determined by taking

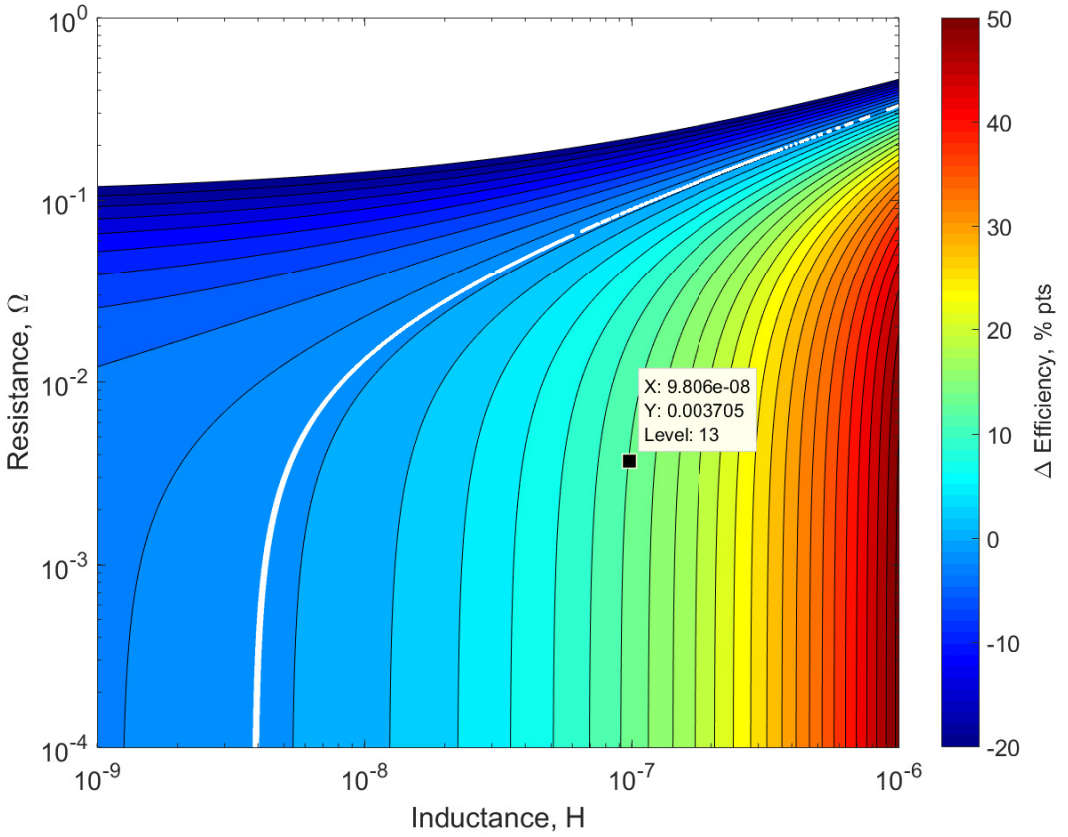


Figure 6.11: Evaluation of the efficiency tradeoff for various inductance

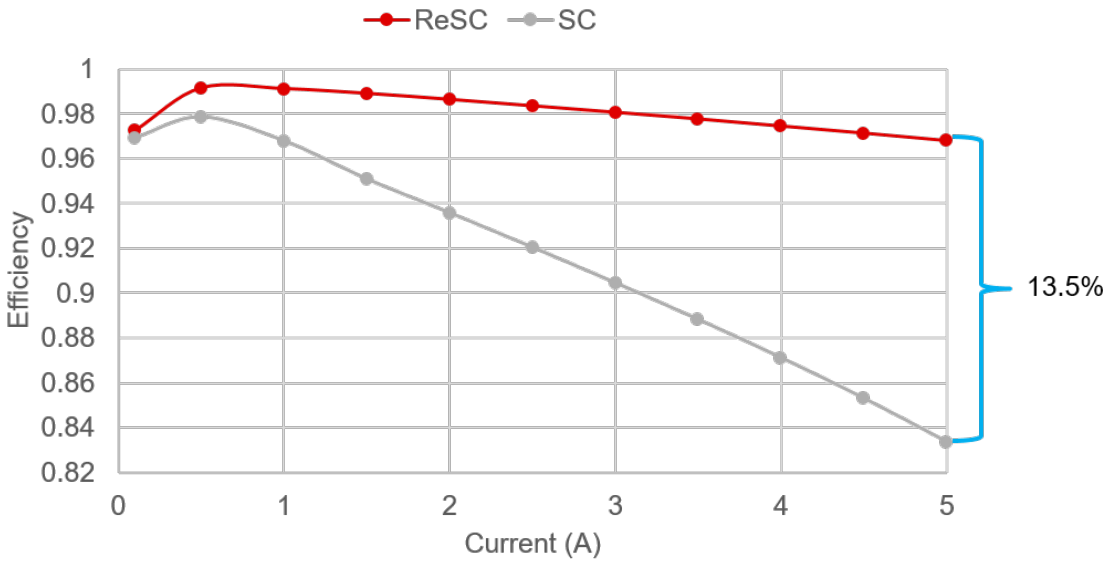


Figure 6.12: Experimental efficiency comparison for the SC and ReSC

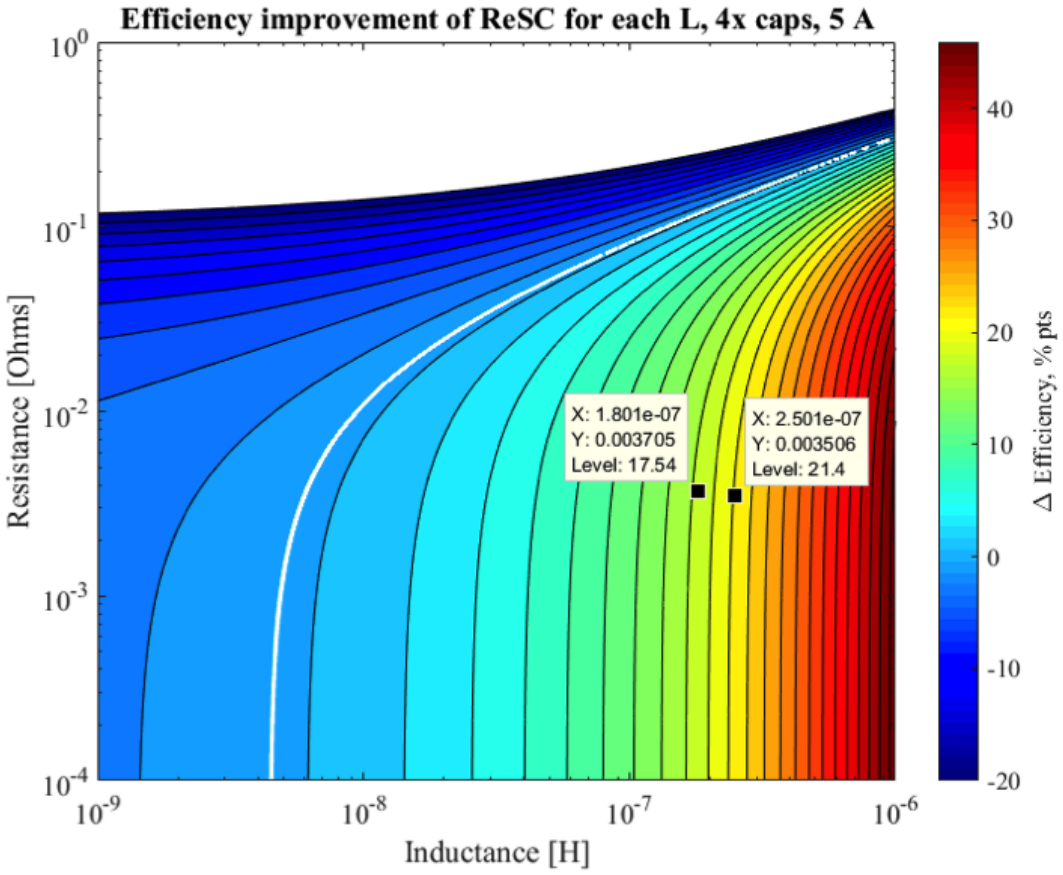


Figure 6.13: Evaluation of the efficiency tradeoff for two inductors

Table 6.1: Model and Experimental comparison for efficiency tradeoff

Inductance	$\eta_{SC_{experimental}}$	$\eta_{ReSC_{model}}$	$\eta_{ReSC_{experimental}}$	$\%_{Error}$
98 nH	83.3 %	96.3 %	96.8 %	1.5 %
180 nH	78.6 %	96.4 %	96.2 %	0.1 %
250 nH	75.1 %	96.5 %	96.1 %	0.4 %

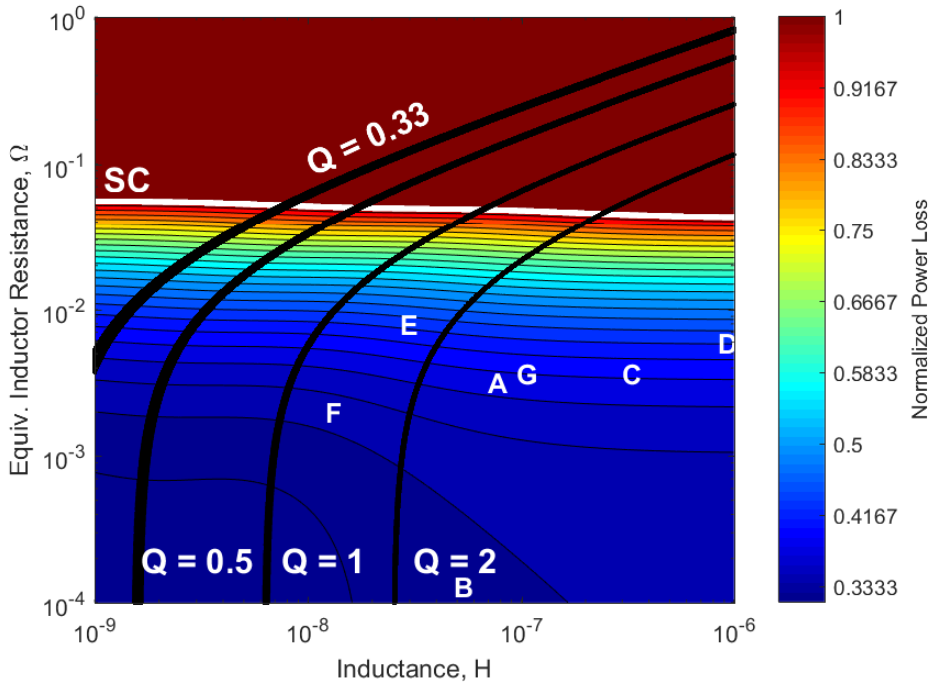


Figure 6.14: Relative power loss for the SC and ReSC for various inductor resistances

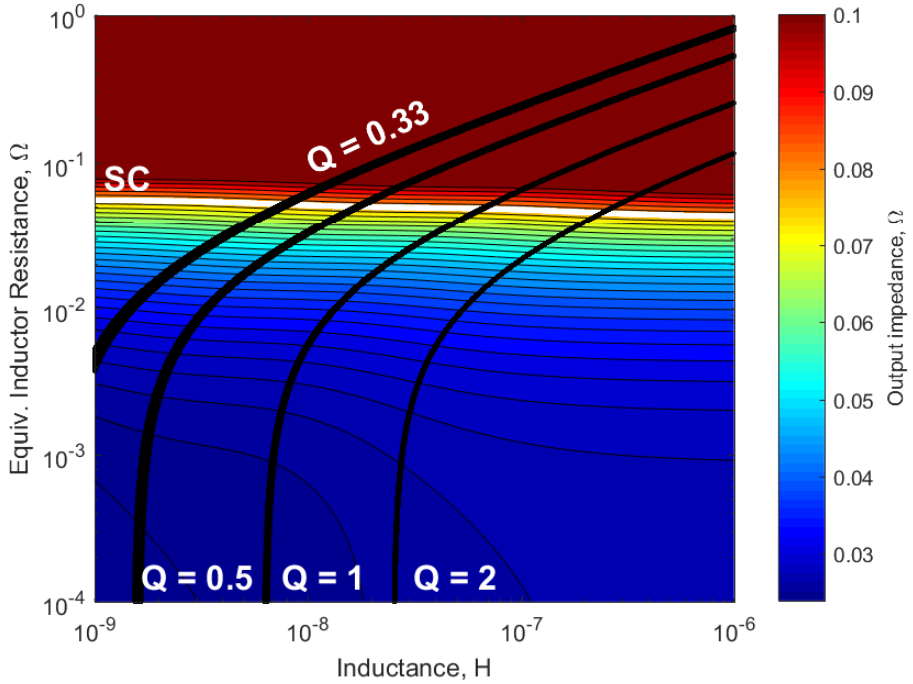


Figure 6.15: Output impedance for the SC and ReSC for various inductor resistances

Table 6.2: Selected off-the-shelf inductors

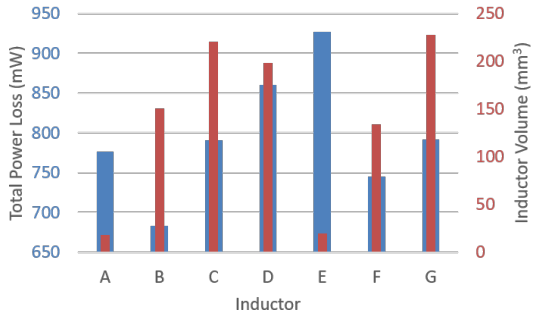
Letter	Mfg.	PN	L	l x w x h (mm)	V (mm^3)
A	Coilcraft	XEL3515-720	70 nH	3.65 x 3.35 x 1.5	18.3
B	Coilcraft	SLC7530S-500	48 nH	7.5 x 6.7 x 3	150.7
C	Coilcraft	MLC7542-311	300 nH	7.5 x 7 x 4.2	220.5
D	Coilcraft	XAL7030-102	842 nH	8 x 8 x 3.1	198.4
E	Coilcraft	1111SQ-27N	27 nH	2.67 x 2.67 x 2.79	19.8
F	Coilcraft	GA3094-AL	12 nH	5.46 x 4.95 x 4.96	134.0
G	ICE	LP02-101-1	95 nH	7 x 6.5 x 5	227.5

the characteristic impedance of the inductor and dividing by the sum of the equivalent inductor ESR and the layout ESR as in Chapter 5. As the Q increases, the R_{eff} becomes independent of inductance.

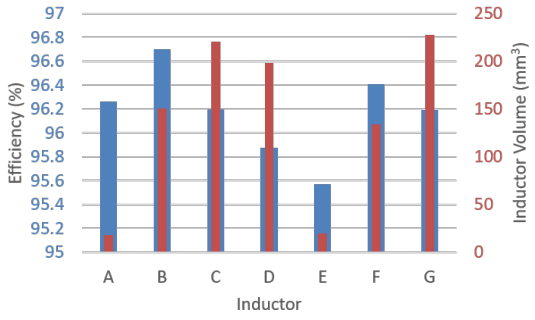
As shown by the $Q = 2$ line, the parasitic resistance in the complete circuit due to layout, capacitor ESR, and FET ESR, will diminish the inductors' efficiency substantially. For low inductance values, the parasitic ESR is so great that a Q of 2 is not achievable, even if the inductor itself is ideal. Inductors larger than about 25 nH for the specified circuit will be usable up to 1 μH, where the power loss in the ReSC is approximately 2.2 times larger than the SC.

Several commercial inductors are also plotted for reference with their specifications provided in Table 6.2. Coilcraft is over-represented because their website makes estimating the AC resistance and core loss quicker. These are still estimations however, each inductor will need to be characterized with an impedance analyzer for the most accurate results. Also included is the ICE inductor used in Chapter 5. Inductors 'E' and 'F' are air-core while the rest are ferrite. The ICE inductor is not the optimal for the highest efficiency or most power dense design. The design trade-off can be made in Fig. 6.16 where power loss and efficiency are shown with inductor volume. The smallest inductor 'E' for example has the highest loss and lowest efficiency. Since the efficiency is about 1 % lower than inductor 'B', the volume reduction of 86 % may be an acceptable exchange

For Q less than 2, the ReSC will be overdamped at the resonant frequency and the inductor current will be not purely sinusoidal. As Q decreases, the inductor current will



(a) Power loss and volume for the selected inductors at 5 A



(b) Efficiency and volume for the selected inductors at 5 A, 20 W

Figure 6.16: Relative performance of the selected inductors for design trade-off

more closely resemble the hard-charging current of the SC. The R_{eff} is reduced since the waveform is no longer sinusoidal and so has a lower rms value. In the FSL, the R_{eff} for the SC will be the PCB resistance. In the ReSC, the R_{eff} is the PCB resistance multiplied by $\frac{\pi^2}{8}$. For the overdamped ReSC (or equivalently, a SC approaching the FSL and near resonance), the effective output impedance will be scaled from $\frac{\pi^2}{8}$ to 1, as the resistance of the inductor increases. The output impedance of the ReSC for the same design space is shown in Fig. 6.15. The R_{eff} is lower in the low-Q zone, but this is not very significant.

The SC in or approaching the FSL has not been included in this work. This is due to the low-Q and low inductance inductors not being commercially available. So to implement this type of converter would require a PCB inductor as discussed in Chapter 3. This type of inductor is hard to control due to the inductance of the layout being comparable. Tuning for the resonant frequency is also more difficult as the frequency can easily change during operation (due to heating and other derating mechanisms). The actual power savings by operating in this mode is likely not worth the effort to tune the circuit, especially when the fully resonant SC has much better efficiency than the SC. For example, a 95 nH inductor with 300 $\mu\Omega$ of equivalent resistance will only dissipate 300 mW more power than a 1.3 nH inductor with the same resistance, at 10 A. This is a loss difference of less than 1 % for a 40 W converter.

Physically, operating in the FSL and low-Q resonant mode are quite different. While resonating, the voltage and current of C_{fly} will be a distorted sine wave, where for the FSL the voltage is constant. The distorted sinewave will produce more harmonics and can increase EMI noise. For the performance metrics considered in this work, the output impedance will slightly increased with low-Q resonant operation.

6.3 Summary

This chapter developed several design spaces for the SC and ReSC. A closed form expression for the maximum efficiency trajectory of the SC is presented to identify the most beneficial selection of flying capacitance, switching frequency, and output current. The design space of the ReSC is also developed but no closed for expression is possible for any Q due to it

being a transcendental equation. However, other design spaces are used to compare the loss of the ReSC against a SC operating at the same frequency, and at an optimal frequency. An equivalent resistance due to the inductance is defined to facilitate the trade-off of loss in the inductor and the added area compared to the SC.

Selection of the inductor is critical to the merits of the ReSC. The design is sensitive to the quality factor where every $m\Omega$ counts. The layout of the power stage and similarly the selection of the power switches are equally critical, as the parasitic resistance in the main conduction path can severely limit the range of acceptable inductors. However, it is also shown that for a SC circuit that has lower ESR in the conduction path, that in order to maintain SSL behavior, the output impedance will be larger than the total circuit resistance in the ReSC. Only in this situation is the ReSC able to outperform the SC, provided the inductor is of sufficient quality. The area tradeoff of the additional inductor, and any other complexities in design as in PCB integrated inductors, is left to the designer to discern.

The use of a PCB trace inductor to achieve slightly better efficiency when operating the ReSC in overdamped mode is also left for the designer to decide. High-Q inductors, while comparatively a little more lossy, will enable the designer to make analytical approximations that shorten design time and greater improve performance relative to the optimized SC.

Chapter 7

Conclusions and Future Work

The Switched-Capacitor circuit has a role to play in the development of high efficiency and high power density voltage supplies for applications such as VRMs, both as a stand alone converter and in a multi-stage implementation. The biggest benefit over the buck or other magnetic based converters is the SC lacks bulky magnetics and is easily integrated. But resonant topologies can also be used such that, while still utilizing a discrete inductor, benefit from volume reduction compared to the buck. For the engineer interested in the SC, it may be of interest to overcome some of the limitations of the conventional hard-charged SC by going fully resonant. This decision must balance efficiency with volume.

Limitations in off-the-shelf components restrict the usable range of the SC, due in part to parasitic inductance that can cause resonance. This resonance can be very difficult to control and measure, especially for dense layouts. The Resonant Switched Capacitor can attain a lower output impedance than a SC with a larger series loop resistance. High-Q circuits provide the most ease in design as many helpful approximations can be made in the analysis. However, the inductors required were discrete and so occupy more area than the pure SC. How much more area for a given power savings is determined on an application basis, as some designs constrain one parameter more than another. Presented here is a first-order approximation for evaluating the performance of an inductor and if that added area is indeed worth the increase in area. The method used in this work is shown to be a reasonable approximation in evaluating the trade-off between the power loss and area for hard-charging and fully resonant SC.

The ReSC also provides an added degree of freedom and possible use in applications over those of the SC. This is made possible by current regulation. The ReSC can have its switching period modulated such that CC-CV battery charging can be implemented. Two methods were explored with the most efficient allowing the tank voltage to reset. Although still a fixed 2:1 topology the ReSC can take advantage of the USB-PD standard, such that the input voltage is varied to provide the required output voltage. The granularity of the input control is relaxed with the ReSC since regulation can also occur by modulating the switching period.

More exploration in using PCB inductors to implement low-Q resonant circuits can be explored in order to provide lower losses compared to the two topologies discussed here. However, the design and implementation of these low and sub nanohenry inductors compound the design complexity to the point that the improvement in efficiency may not be worth it, especially considering the ReSC can achieve at least 93.8 % at 10 A. This can be further improved with layout techniques and optimized switch selection.

The design spaces developed here are for a fixed flying capacitance, and so iterations are required for additional capacitances. There may be a more efficient way of developing the design spaces that use an optimized capacitance or account for more design variables such as ripple. For the ReSC, this could be coupled with a design space comparison between other topologies such as the buck and hybrid buck converter.

Implementing closed-loop control for both the SC and ReSC to see if their is any benefit in using multi-mode operation for further efficiency improvement. Multi-mode operation has been shown to improve light-load conditions, so comparing this to a paralleled two-stage converter where the SC is typically used at light load could be beneficial. Similarly, the impact of high-frequency ripple in battery charging and the relative sizing of the output capacitors for the regulated ReSC can also further determine if the topology is appropriate for that application.

Finally, it would be interesting to compare the power density of the SC and ReSC in a state-of-the-art silicon process and integrated GaN process, identifying any obstacles that would prevent the circuit from being widely implemented.

Bibliography

[1] Q. R. Schwartz, "How to minimize the power consumption of your app," in *UPLINQ 2014*, Sept 2014. viii, 1

[2] R. P.-P. Y. Lei, "Circuit techniques for improving the power density of switched-capacitor converters," in *Power Management Integrated Circuits*, M. M. Hella, Ed. Boca Raton, FL: CRC Press, 2016, pp. 100–140. xi, 1, 23, 57, 58, 62, 72

[3] M. Brocanelli and X. Wang, "Making smartphone smart on demand for longer battery life," in *2017 IEEE 37th International Conference on Distributed Computing Systems (ICDCS)*, June 2017, pp. 2288–2293. 1

[4] (2015) In less than two years, a smartphone could be your only computer. [Online]. Available: https://www.wired.com/2015/02/smartphone-only-computer/ 1

[5] (2015) Fast-charging trends and challenges for single-cell batteries using high input voltage. [Online]. Available: https://goo.gl/EU6LNT 1, 92

[6] L. He, Y. Tung, and K. G. Shin, "icharge: User-interactive charging of mobile devices," in *Proc. ACM MobiSys '17*, Niagara Falls, NY, June 2017. 1

[7] G. G. J. Gamble, B. Blalock, and D. Costinett, "Hybrid buck converter optimization and comparison for smart phone integrated battery chargers," in *(In Press)2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2018. 1, 2

[8] (2016) The advantages of pulse frequency modulation for dcdc switching voltage converters. [Online]. Available: https://www.digikey.com/en/articles/techzone/2016/sep/a-designer-guide-fast-lithium-ion-battery-charging 1

[9] G. Gabian, J. Gamble, B. Blalock, and D. Costinett, "Modeling high current integrated power converters," in *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, July 2017, pp. 1–7. 2, 3, 13, 16

[10] G. Gabian, B. Blalock, and D. Costinett, "5v-to-4v integrated buck converter for battery charging applications with an on-chip decoupling capacitor," in *2017 IEEE*

Applied Power Electronics Conference and Exposition (APEC), March 2017, pp. 178–183. 2

[11] A. Abdulslam, S. H. Amer, A. S. Emara, and Y. Ismail, "Evaluation of multi-level buck converters for low-power applications," in *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2016, pp. 794–797. 2

[12] B. Choi and D. Maksimovic, "Loss modeling and optimization for monolithic implementation of the three-level buck converter," in *2013 IEEE Energy Conversion Congress and Exposition*, Sept 2013, pp. 5574–5579. 2

[13] T. Instruments. BQ24190. [Online]. Available: http://www.ti.com/product/bq24190?qgpn=bq24190 2

[14] G. A. Gabian, "High-current integrated battery chargers for mobile applications," Master's thesis, University of Tennessee, Knoxville, 2017. ix, 2, 4, 10, 16, 58

[15] "DA9313 data sheet," Dialog Semiconductor, United Kingdom. ix, 2, 20, 21

[16] V. Ng, "Switched capacitor dcdc converter: Superior where the buck converter has dominated," Ph.D. dissertation, Univ. of California, Berkeley, Berkeley, 2011. 2, 20, 22, 23

[17] J. Stauth, "Circuit techniques for improving the power density of switched-capacitor converters," in *Power Management Integrated Circuits*, M. M. Hella, Ed. Boca Raton, FL: CRC Press, 2016, pp. 145–167. 2, 58, 77, 106, 109

[18] "High Efficiency, High Density, Switched Capacitor Converter suitable for High Power Applications design note 1043," Linear Technologies, Milpitas, CA. 3

[19] V. W. Ng, M. D. Seeman, and S. R. Sanders, "Minimum pcb footprint point-of-load dc-dc converter realized with switched-capacitor architecture," in *2009 IEEE Energy Conversion Congress and Exposition*, Sept 2009, pp. 1575–1581. 4, 13

[20] *Growth in data center electricity use 2005 to 2010*. Analytics Press, 2011. 4

[21] A. Pratt, P. Kumar, and T. V. Aldridge, "Evaluation of 400v dc distribution in telco and data centers to improve energy efficiency," in *INTELEC 07 - 29th International Telecommunications Energy Conference*, Sept 2007, pp. 32–39. 4

[22] S. Moore and P. Schneider, "A review of cell equalization methods for lithium ion and lithium polymer battery systems," Society of Automotive Engineers, USA, Tech. Rep. 2001-01-0959, 2001. ix, 8

[23] G. A. Kobzev, "Switched-capacitor systems for battery equalization," in *Modern Techniques and Technology, 2000. MTT 2000. Proceedings of the VI International Scientific and Practical Conference of Students, Post-graduates and Young Scientists*, 2000, pp. 57–59. 8

[24] Y. Shang, N. Cui, B. Duan, and C. Zhang, "Analysis and optimization of star-structured switched-capacitor equalizers for series-connected battery strings," *IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1–1, 2017. 8

[25] R. Fukui and H. Koizumi, "Double-tiered switched capacitor battery charge equalizer with chain structure," in *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*, Nov 2013, pp. 6715–6720. 8

[26] Y. Wang, H. Yin, S. Han, A. Alsabbagh, and C. Ma, "A novel switched capacitor circuit for battery cell balancing speed improvement," in *2017 IEEE 26th International Symposium on Industrial Electronics (ISIE)*, June 2017, pp. 1977–1982. 8

[27] A. C. Baughman and M. Ferdowsi, "Double-tiered switched-capacitor battery charge equalization technique," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 6, pp. 2277–2285, June 2008. 8

[28] Y. Yuanmao, K. W. E. Cheng, and Y. P. B. Yeung, "Zero-current switching switched-capacitor zero-voltage-gap automatic equalization system for series battery string," *IEEE Transactions on Power Electronics*, vol. 27, no. 7, pp. 3234–3242, July 2012. 8

[29] I. chowdhury, "Efficient voltage regulation using switched capacitor dc/dc converter from battery and energy harvesting power sources," Ph.D. dissertation, Univ. of Arizona, Tucson, 2010. ix, 9

[30] F. Su and W. H. Ki, "Component-efficient multiphase switched-capacitor dc;dc converter with configurable conversion ratios for lcd driver applications," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, no. 8, pp. 753–757, Aug 2008. 9

[31] T. Ying, W.-H. Ki, and M. Chan, "Area-efficient cmos charge pumps for lcd drivers," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 10, pp. 1721–1725, Oct 2003. 9

[32] R. L. B. Zamparette, H. D. Klimach, and S. Bampi, "A 90switched capacitor dc;dc converter for photovoltaic energy harvesting aiming for iot applications," in *2017 IEEE 8th Latin American Symposium on Circuits Systems (LASCAS)*, Feb 2017, pp. 1–4. 9

[33] L. Intaschi, P. Bruschi, G. Iannaccone, and F. Dalena, "A 220-mv input, 8.6 step-up voltage conversion ratio, 10.45- uw output power, fully integrated switched-capacitor converter for energy harvesting," in *2017 IEEE Custom Integrated Circuits Conference (CICC)*, April 2017, pp. 1–4. 9

[34] S. Mondal and R. Paily, "An efficient on-chip switched-capacitor-based power converter for a microscale energy transducer," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, no. 3, pp. 254–258, March 2016. 9

[35] C. Jensen, "Application brief: Switched capacitor circuits provide efficient and functional white-led drive," Texas Instruments, Tx, Tech. Rep. SNVA521, 2011. 9

[36] L. Yin, X. Wu, and M. Zhao, "A highly efficient switched-capacitor led driver with switching frequency hopping technique," in *2010 10th IEEE International Conference on Solid-State and Integrated Circuit Technology*, Nov 2010, pp. 521–523. 10

[37] F. S. W. Feng, "A new switched-capacitor frequency modulated driver for light emitting diodes," in *Review of Scientific Instruments 78*, Nov 2007, pp. 521–523. 10

[38] "LTC3209 data sheet," Linear Technologies, Milpitas, CA. 10

[39] "ADM8843 data sheet," Analog Devices, Norwood, MA. 10

[40] M. Salem, A. Jusoh, and N. R. N. Idris, "Implementing buck converter for battery charger using soft switching techniques," in *2013 IEEE 7th International Power Engineering and Optimization Conference (PEOCO)*, June 2013, pp. 188–192. 10

[41] Y. C. Chuang, "High-efficiency zcs buck converter for rechargeable batteries," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2463–2472, July 2010. 10

[42] F. Haizoune, H. J. Bergveld, J. Popovic-Gerber, and J. A. Ferreira, "Topology comparison and design optimisation of the buck converter and the single-inductor dual-output converter for system-in-package in 65nm cmos," in *2009 IEEE 6th International Power Electronics and Motion Control Conference*, May 2009, pp. 295–301. 10

[43] M. G. Jeong, S. H. Kim, and C. Yoo, "Switching battery charger integrated circuit for mobile devices in a 130-nm bcdmos process," *IEEE Transactions on Power Electronics*, vol. 31, no. 11, pp. 7943–7952, Nov 2016. 10

[44] C. Shi, B. C. Walker, E. Zeisel, B. Hu, and G. H. McAllister, "A highly integrated power management ic for advanced mobile applications," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 8, pp. 1723–1731, Aug 2007. 10

[45] R. M. J. Formenti, "Design trade-offs for switch-mode battery chargers," Texas Instruments, Dallas, Tx. 10

[46] (Accessed 03/29) Lt- parametric search: switching battery chargers. [Online]. Available: http://www.linear.com/parametric/Switching_Battery_Chargers 10

[47] R. Prasad, C. Namuduri, and P. Kollmeyer, "Onboard unidirectional automotive g2v battery charger using sine charging and its effect on li-ion batteries," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2015, pp. 6299–6305. 11

[48] S. D. Breucker, K. Engelen, R. D'hulst, and J. Driesen, "Impact of current ripple on li-ion battery ageing," in *2013 World Electric Vehicle Symposium and Exhibition (EVS27)*, Nov 2013, pp. 1–9. 11

[49] S. Vadivelu, "Investigation of sinusoidal ripple current charging techniques for li-ion cells," Master's thesis, KTH Royal Institute of Technology, Stockholm, Sweden, 2016. 11

[50] F. Lacressonniere, B. Cassoret, and J. F. Brudny, "Influence of a charging current with a sinusoidal perturbation on the performance of a lead-acid battery," *IEE Proceedings - Electric Power Applications*, vol. 152, no. 5, pp. 1365–1370, Sept 2005. 11

[51] H. Z. Z. Beh, G. A. Covic, and J. T. Boys, "Effects of pulse and dc charging on lithium iron phosphate (lifepo4) batteries," in *2013 IEEE Energy Conversion Congress and Exposition*, Sept 2013, pp. 315–320. 11

[52] A. Bessman, R. Soares, S. Vadivelu, O. Wallmark, P. Svens, H. Ekstrm, and G. Lindbergh, "Challenging sinusoidal ripple-current charging of lithium-ion batteries," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 6, pp. 4750–4757, June 2018. 11

[53] K. Uddin, A. D. Moore, A. Barai, and J. Marco, "The effects of high frequency current ripple on electric vehicle battery performance," *Applied Energy*, vol. 178, pp. 142 – 154, 2016. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S030626191630808X 11

[54] L. Technologies. LTC3251. [Online]. Available: http://www.analog.com/en/products/power-management/inductorless-charge-pump-dc-dc-converters/regulated-step-down-charge-pumps/ltc3251.html ix, 12, 22

[55] "TPS6050x data sheet," Texas Instruments, Dallas, Tx. 13

[56] "LTC3251 data sheet," Linear Technologies, Milpitas, CA. 13

[57] D. El-Damak, S. Bandyopadhyay, and A. P. Chandrakasan, "A 93reconfigurable switched-capacitor dc-dc converter using on-chip ferroelectric capacitors," in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, Feb 2013, pp. 374–375. ix, 13, 14

[58] I. Vaisband, M. Saadat, and B. Murmann, "A closed-loop reconfigurable switched-capacitor dc-dc converter for sub-mw energy harvesting applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 2, pp. 385–394, Feb 2015. 14

[59] R. C. N. Pilawa-Podgurski, D. M. Giuliano, and D. J. Perreault, "Merged two-stage power converterarchitecture with softcharging switched-capacitor energy transfer," in *2008 IEEE Power Electronics Specialists Conference*, June 2008, pp. 4008–4015. ix, 14

[60] J. Sun, M. Xu, Y. Ying, and F. C. Lee, "High power density, high efficiency system two-stage power architecture for laptop computers," in *2006 37th IEEE Power Electronics Specialists Conference*, June 2006, pp. 1–7. 14

[61] B. Axelrod, Y. Berkovich, S. Tapuchi, and A. Ioinovici, "Single-stage single-switch switched-capacitor buck/buck-boost-type converter," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 45, no. 2, pp. 419–430, April 2009. ix, 15

[62] (2016) Introduction to usb power delivery. [Online]. Available: http://www.electronicdesign.com/interconnects/introduction-usb-power-delivery viii, 15, 16, 92

[63] D. S. L. Harju, "Solutions for fast charging," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2018. ix, 16, 17

[64] D. S. Y. Li, "Emerging application of usb pd for rapid charging in mobile devices," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2018. ix, 16, 17

[65] G. S. Seo and H. P. Le, "An inductor-less hybrid step-down dc-dc converter architecture for future smart power cable," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2017, pp. 247–253. 16

[66] T. Instruments. Switched-Cap Fast Charge Reference Design for USB Power Delivery Programmable Power Supply. [Online]. Available: http://www.ti.com/lit/ug/tidudl7/tidudl7.pdf ix, 16, 18, 19, 20

[67] T. Instruments. BQ25890. [Online]. Available: http://www.ti.com/lit/ds/symlink/bq25890.pdf ix, 19

[68] X. Mi, H. F. Moghadam, and J. s. Seo, "Flying and decoupling capacitance optimization for area-constrained on-chip switched-capacitor voltage regulators," in *Design, Automation Test in Europe Conference Exhibition (DATE), 2017*, March 2017, pp. 1269–1272. 20, 23

[69] M. Seeman, "A design methodology for switched-capacitor dc-dc converters," Ph.D. dissertation, Univ. of California, Berkley, Berkley, May 2000. [Online]. Available: http://www.ece.udel.edu/~qli 22, 23, 57, 58

[70] H. Le, "Design techniques for fully integrated switched- capacitor voltage regulators," Ph.D. dissertation, Univ. of California, Berkeley, Berkeley, May 2015. 22, 23, 58

[71] T. M. Andersen, F. Krismer, J. W. Kolar, T. Toifl, C. Menolfi, L. Kull, T. Morf, M. Kossel, M. Brndli, and P. A. Francese, "Modeling and pareto optimization of on-chip switched capacitor converters," *IEEE Transactions on Power Electronics*, vol. 32, no. 1, pp. 363–377, Jan 2017. 22

[72] P. Zhou, W. H. Choi, B. Kim, C. H. Kim, and S. S. Sapatnekar, "Optimization of on-chip switched-capacitor dc-dc converters for high-performance applications," in *2012 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Nov 2012, pp. 263–270. 22, 23

[73] S. Zhang, N. R. Shanbhag, and P. T. Krein, "System-level optimization of switched-capacitor vrm and core for sub/near- v_t computing," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 61, no. 9, pp. 726–730, Sept 2014. 22, 23

[74] V. S. Sathe and J. s. Seo, "Analysis and optimization of cmos switched-capacitor converters," in *2015 IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, July 2015, pp. 327–334. 22, 23

[75] M. H. Kiani and J. T. Stauth, "Optimization and comparison of hybrid-resonant switched capacitor dc-dc converter topologies," in *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, July 2017, pp. 1–8. 24

[76] J. S. Rentmeister and J. T. Stauth, "Bypass capacitance and voltage ripple considerations for resonant switched capacitor converters," in *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, July 2017, pp. 1–8. 24, 82

[77] P. A. Kyaw, A. L. F. Stein, and C. R. Sullivan, "Power density optimization of resonant tanks using standard capacitors," in *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, July 2017, pp. 1–7. 24

[78] K. Kesarwani, R. Sangwan, and J. T. Stauth, "Resonant-switched capacitor converters for chip-scale power delivery: Design and implementation," *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 6966–6977, Dec 2015. 24, 25, 58, 62

[79] C. Schaef, B. Reese, C. R. Sullivan, and J. T. Stauth, "Design aspects of multi-phase interleaved resonant switched-capacitor converters with mm-scale air-core inductors," in *2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL)*, July 2015, pp. 1–5. x, 24, 32, 33, 54

[80] K. Kesarwani and J. T. Stauth, "The direct-conversion resonant switched capacitor architecture with merged multiphase interleaving: Cost and performance comparison," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2015, pp. 952–959. xi, 24, 72, 73, 75

[81] D. Cao and F. Z. Peng, "A family of zero current switching switched-capacitor dc-dc converters," in *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Feb 2010, pp. 1365–1372. 24

[82] M. Shoyama and T. Ninomiya, "Output voltage control of resonant boost switched capacitor converter," in *2007 Power Conversion Conference - Nagoya*, April 2007, pp. 899–903. 24

[83] K. Zou, Y. Huang, and J. Wang, "A voltage regulation method for high power switched-capacitor circuits," in *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Feb 2012, pp. 1387–1391. 24, 25

[84] K. Sano and H. Fujita, "Performance of a high-efficiency switched-capacitor-based resonant converter with phase-shift control," *IEEE Transactions on Power Electronics*, vol. 26, no. 2, pp. 344–354, Feb 2011. 24, 25

[85] D. Qiu, B. Zhang, and C. Zheng, "Duty ratio control of resonant switched capacitor dc-dc converter," in *2005 International Conference on Electrical Machines and Systems*, vol. 2, Sept 2005, pp. 1138–1141 Vol. 2. 24, 25

[86] C. Schaef, K. Kesarwani, and J. T. Stauth, "20.2 a variable-conversion-ratio 3-phase resonant switched capacitor converter with 850.91w/mm2 using 1.1nh pcb-trace inductors," in *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, Feb 2015, pp. 1–3. 24, 71, 88

[87] Y. Li, J. Chen, M. John, R. Liou, and S. R. Sanders, "Resonant switched capacitor stacked topology enabling high dc-dc voltage conversion ratios and efficient wide range regulation," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2016, pp. 1–7. 25

[88] E. Abramov, A. Cervera, and M. M. Peretz, "Optimal design of a voltage regulator based on gyrator switched-resonator converter ic," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. PP, no. 99, pp. 1–1, 2017. 25, 88, 90

[89] K. Kesarwani, R. Sangwan, and J. T. Stauth, "4.5 a 2-phase resonant switched-capacitor converter delivering 4.3w at 0.6w/mm2 with 85efficiency," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, Feb 2014, pp. 86–87. 25

[90] K. Kesarwani and J. T. Stauth, "Resonant and multi-mode operation of flying capacitor multi-level dc-dc converters," in *2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL)*, July 2015, pp. 1–8. 25

[91] (2010) egan-silicon power shoot-out: Part 1 comparing figure of merit (fom). [Online]. Available: http://www.powerelectronics.com/discrete-power-semis/egantm-silicon-power-shoot-out-part-1-comparing-figure-merit-fom 29

[92] L. Culbertson. Wide Bandgap Semiconductors Go Beyond Silicon in Power, RF, LED Lighting, and Optoelectronics. [Online]. Available: https://www.mouser.com/applications/wide-bandgap-beyond-silicon/ 30

[93] D. S. Gardner, G. Schrom, F. Paillet, B. Jamieson, T. Karnik, and S. Borkar, "Review of on-chip inductor structures with magnetic films," *IEEE Transactions on Magnetics*, vol. 45, no. 10, pp. 4760–4766, Oct 2009. 31

[94] C. . Mathna, N. Wang, S. Kulkarni, and S. Roy, "Review of integrated magnetics for power supply on chip (pwrsoc)," *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4799–4816, Nov 2012. 31

[95] D. Baba, "Benefits of a multiphase buck converter," Texas Instruments, Tx, Tech. Rep. SLYT449, 2012. 31

[96] J. Wibben and R. Harjani, "A high-efficiency dc/dc converter using 2 nh integrated inductors," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 4, pp. 844–854, April 2008. 31

[97] P. R. Morrow, C. M. Park, H. W. Koertzen, and J. T. DiBene, "Design and fabrication of on-chip coupled inductors integrated with magnetic material for voltage regulators," *IEEE Transactions on Magnetics*, vol. 47, no. 6, pp. 1678–1686, June 2011. 31

[98] G. V. Pique and E. Alarcon, "Contributions on converter integrated components and detailed models," in *CMOS Integrated Switching Power Converters*. New York, NY: Springer, 2011, pp. 47–60. 32

[99] C. R. Sullivan, B. A. Reese, A. L. F. Stein, and P. A. Kyaw, "On size and magnetics: Why small efficient power inductors are rare," in *2016 International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM)*, June 2016, pp. 1–23. 36, 106

[100] (2018) Tdk multilayer ceremic chip capacitors. [Online]. Available: https://product.tdk.com/en/search/capacitor/ceramic/mlcc/characteristic/ 38

[101] (Accessed 03/18) Digikey ceramic capacitor search tool. [Online]. Available: https://www.digikey.com/products/en/capacitors/ceramic-capacitors/ 38

[102] M. Fortunato. (2012) Temperature and voltage variation of ceramic capacitors... [Online]. Available: https://www.maximintegrated.com/en/app-notes/index.mvp/id/5527 viii, x, 39, 40, 41

[103] Singing capacitors (piezoelectric effect), url =. 39

[104] J. Ngo. (2015) Here's what makes mlcc dielectrics different. [Online]. Available: https://ec.kemet.com/mlcc-dielectric-differences 41

[105] *Telephony: The American Telephone Journal ...* Telephony Publishing Company, 1921, no. v. 81. [Online]. Available: https://books.google.com/books?id=AP1FAQAAMAAJ 42

[106] J. T. Moody, "Efficient methods for calculating equivalent resistance between nodes of a highly symmetric resistor network," Master's thesis, Worcester Polytechnic Institute, Worcester, Ma, 2013. 44

[107] M. S. Makowski and D. Maksimovic, "Performance limits of switched-capacitor dc-dc converters," in *Power Electronics Specialists Conference, 1995. PESC '95 Record., 26th Annual IEEE*, vol. 2, Jun 1995, pp. 1215–1221 vol.2. 57, 62

[108] J. T. Stauth, M. D. Seeman, and K. Kesarwani, "A resonant switched-capacitor ic and embedded system for sub-module photovoltaic power management," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 3043–3054, Dec 2012. 71

[109] K. Kesarwani, R. Sangwan, and J. T. Stauth, "Resonant-switched capacitor converters for chip-scale power delivery: Design and implementation," *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 6966–6977, Dec 2015. 75

[110] S. Pasternak, C. Schaef, and J. Stauth, "Equivalent resistance approach to optimization, analysis and comparison of hybrid/resonant switched-capacitor converters," in *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, June 2016, pp. 1–8. 77

[111] A. Cervera, M. Evzelman, M. M. Peretz, and S. . Ben-Yaakov, "A high-efficiency resonant switched capacitor converter with continuous conversion ratio," *IEEE Transactions on Power Electronics*, vol. 30, no. 3, pp. 1373–1382, March 2015. 79

[112] D. M. R.W. Erickson, *Fundamentals of Power Electronics*. Norwell, MA: Kluwer Academic Publishers, 2001. 80

[113] "LP02-1 data sheet," ICE Components, Marietta, GA. 83

[114] (2014) The advantages of pulse frequency modulation for dcdc switching voltage converters. [Online]. Available: https://www.digikey.com/en/articles/techzone/2014/mar/the-advantages-of-pulse-frequency-modulation-for-dc-dc-switching-voltage-converters 88

[115] (2012) Usb power delivery specification 1.0. [Online]. Available: http://www.usb.org/developers/powerdelivery/ 92

[116] D. Pimentel, M. B. Slima, and A. Cheriti, "Power control for pulse-density modulation resonant converters," in *2006 IEEE International Symposium on Industrial Electronics*, vol. 2, July 2006, pp. 1259–1264. 94

Vita

Jordan Alexander Gamble earned a Bachelor of Science degree in Electrical Engineering Technology from Penn State University with a minor in Electronic and Photonic Materials in 2013. He worked for Arkansas Power Electronics International, later acquired by Cree, as a power electronics design engineer. He was awarded the DOE Wide-Bandgap Traineeship Fellowship from UTK in 2016 and joined Dr. Blalock and Dr. Costinett as an MS student in 2016 to research integrated battery chargers for mobile applications, as sponsored by Texas Instruments.