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Wireless Power System Design for Maximum Efficiency

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To the Graduate Council:

I am submitting herewith a thesis written by Jie Li entitled "Wireless Power System Design for Maximum Efficiency." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

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Wireless Power System Design for Maximum Efficiency

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Abstract

With the potential of cutting the last cord, wireless power transfer (WPT) using magnetic resonant coupling is gaining increasing popularity. Evolved from the inductive WPT techniques used in commercial products today, resonant WPT can transfer power over a longer distance with higher spatial freedom. Experimental prototypes have shown power transfer across a 2 m air gap [1], proving the viability of resonant WPT. Industrial consortia such as the AirFuel Alliance have standard specifications that enable wide application in consumer electronics.

Despite the promises of high efficiency and long transfer distance, resonant WPT has significant challenges to overcome before the broad adoption will occur. One of the critical challenges is the how to design the complicated system. A WPT system consists of multiple parts: the transmitter coil and the compensation capacitor, the receiver coil and the compensation capacitor, and the power stages which consists of the inverter in the transmitter side and rectifier in the receiver side. This thesis investigates the WPT system design for maximum efficiency. It explores modeling and design of individual stages as well as the entire system design method. From the careful literature review, it is found that current design method of coils is insufficient for consumer electronics applications due to the strict sensitivity of size. The current power stage design method is insufficient or inaccurate for WPT applications where wide loading situations need to be considered. The system-level design method is based on assumptions that are not generally true due to the neglect of ZVS requirement and diode rectifier reactance. Instead, previously established techniques in coil design are applied to invent a new coil structure for reduced ESR while achieving a compact size. Previous ZVS inverter and diode rectifier topology are combined with waveform and circuit analysis to develop new accurate modeling and design method for a wide load range.

From the resulting coil and converter models, an entire WPT system model and design methodology are proposed which highlights the design parameters selection and the design sequence. These techniques together contribute to a WPT system in terms of both high efficiency and compact size.

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Chapter 1

Introduction

With the promise of cutting the last cord, wireless power transfer has been adopted widely in everyday applications. The power level ranges from sub-watt medical implant device charging applications to watt level consumer electronics application, further to the kilo-watt level electric vehicle (EV) and rail-way charging. This thesis will address the watt level consumer electronics application with a focus on system design.

1.1 Wireless Power Transfer Overview

Wireless power transfer (WPT) refers to the transfer of power from a source to an electric load without any wired connection. Compared with traditional wired charging, WPT has several advantages that push this technology forward. WPT removes the need for plugging the charging cables. The eliminating of cable connection increases safety and is convenient because it increases ease of use. Furthermore, WPT has the potential to apply seamless charging, which means customers are capable to charge devices wherever near a charging pad. Seamless charging reduces charging intervals, therefore reducing the size and weight of the battery. The convenience and the promise of reducing the battery size boost the wide applications of WPT. Currently, the major application of WPT is in consumer electronics such as cell phones, laptops, tablets, and TVs. Other high-power applications of WPT are being researched such as EV charging [14] and railway seamless charging [15]. For some special applications such as implant devices [16], WPT is the only preferred solution.

Globally, WPT is being widely accepted, applied and researched by major industrial companies and research centers. The major industrial players in WPT market involves consumer electronics unicorns such as Intel, Apple, and Samsung, and EV unicorns such as BMW, Audi, and Nissan, and other important companies such as Texas Instruments, Efficient Power Conversion Corporation (EPC), WiTricity, and so on. The market for WPT technology is expected to be worth more than 11.3 billion by the year 2022 [17].

1.2 Inductive Wireless Power Transfer

The initial WPT system introduced to the public uses the similar operating principle to a transformer, where the primary coil and the secondary coil are placed closely and magnetically coupled through the air [18]. An induced voltage will be generated at the receiver coil when the transmitter coil conducts current, even though there is no wired connection between the two sides. This kind of wireless power transfer is called inductive wireless power transfer (IPT). The typical application involves low-power consumer

electronics such as WPT charging for the electric toothbrush, and WPT charging for the cell phone.

The maturity of IPT for consumer electronics was proven by the launch of the Qi standard from the Wireless Power Consortium in 2011 [19]. Similar to the aforementioned applications, Qi utilizes two tightly coupled coils and transfers power over millimeters range [19]. Qi standard sets the operating frequency range to be 110 kHz to 205 kHz for low power applications (5 W) [19]. For medium-power applications up to 120 W, the frequency range is set to be 80 - 300 kHz [19]. Qi targets the overall system efficiency to be higher than 70 % [19]. Afterward, Qi is widely applied by more than 100 companies in their wireless charger design.

A major drawback of IPT is the short transfer distance and the intolerance of position misalignment. This disadvantage comes from the working principle of IPT that the receiver side voltage is an induced voltage from the transmitter side magnetic field. When the receiver side is moved away from the transmitter, or a misalignment occurs from the designed position, the coupling between two sides decreases rapidly. The rapid decrease of coupling causes the drastic decrease of the induced voltage, reducing the output power [18]. A more complicated converter may be designed to use the low induced voltage to maintain the initial output power at the expense of power loss and cost [20], but is not preferred in consumer electronics applications. Methods of increasing the induced voltage include raising the transmitter (Tx) coil conducting current or working frequency, however, both at the expense of higher Tx coil loss [21]. Methods of preventing the coupling drop include designing larger coils [18]. But larger coil is not preferred in consumer electronics applications. Another method to maintain the initial power level is reducing the reactive power of the receiver side by adding a compensation capacitor to the receiver (Rx) coil, creating a resonant wireless power transfer [18].

1.3 Resonant Wireless Power Transfer

In a resonant WPT system, a compensation capacitor or tuning network is applied to have a resonance with the Rx coil at the fundamental operating frequency eliminating the reactive

power of the receiver. Assuming the Tx coil generates a constant magnetic field, the receiver with greatly reduced reactance is capable to provide higher output power and needs less Tx coil current to produce same output power, compared with IPT system with no receiver coil compensation. The Tx coil reactance is also compensated by a capacitor, increasing the achievable Tx current under restricted input voltage, enhancing the H-field generation ability and increasing transfer distance and power level.

The advantage of long distance, high efficiency, and high power level (under restricted input voltage) boosts the wide acceptance of resonant WPT. The commercial standard group Alliance for Wireless Power (A4WP) was launched in 2012 which involves more than 100 major companies including Intel, EPC, and so on. A4WP is indented to create a resonant WPT standard to compete with the existing Qi standard [22]. The standard they proposed is called "Rezence" or "Airfuel" which supports power transfer up to 50 watts over distances up to 5 cm. The transfer distance is one order of magnitude larger than the Qi standard. The working frequency is set to be 6.78 MHz, which is one of the modern ISM bands. The obviously magnified switching frequency reduces the size of coils and the compensation capacitors compared with Qi standard. In November 2015, A4WP merged with Power Matters Alliance (PMA) forming a new alliance called "AirFuel Alliance" [22].

1.4 Resonant WPT System Structure

Fig. 1.1 shows a basic structure of a resonant WPT system. The system consists of an inverter, a Tx coil and its compensation capacitor, an Rx coil and its compensation capacitor, and a rectifier with the load. The Rx coil is usually tuned to be resonant at the operating frequency for minimum reactive power for efficiency and power level considerations. The Tx coil is usually tuned to achieve greatly reduced reactive power for higher power level with restricted V_{in}, and slightly inductive for reducing inverter switching loss[18]. In practical applications, a DC-DC link may be used between the rectifier output and the battery [20], and impedance matching stages may be used between power stages and coils [23]. However, Fig. 1.1 only shows the structure necessary to form a complete WPT system as a basic example.

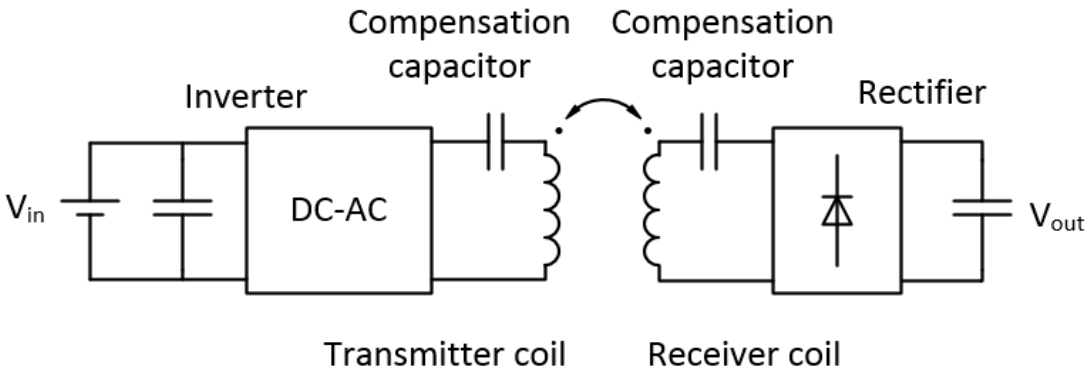


Figure 1.1: Basic structure of a resonant WPT system.

Despite the promises of high efficiency and long transfer distance, resonant WPT has significant challenges to overcome before the broad adoption will occur. The whole system design is one of the critical challenges due to the complexity of the system. This thesis will focus on resonant WPT whole system design. More specifically, the discussion will be focused on modeling and design of coils, converters, and further the entire system. This thesis aims at consumer electronics applications described by the Airfuel standard, meaning the power level is tens of watts and the working frequency is focused at 6.78 MHz.

1.5 Summary and Outline

WPT using magnetic coupling consists of two categories: IPT and resonant WPT. IPT uses tightly coupled coils to transfer power, therefore has limitations such as short charging distance, and intolerance to misalignment. Resonant WPT, on the other hand, compensates the coil inductance using capacitors, reducing the reactive power required from the inverter. Therefore, resonant WPT has longer charging distance and less sensitivity of misalignment. "Airfuel" standard sets the resonant WPT working frequency to be 6.78 MHz, presenting critical system design challenges.

The goal of this thesis is exploring resonant WPT system design method for maximum efficiency. To achieve this goal, both individual stage design method and the entire system design method will be explored. Following this introductory chapter, Chapter 2 is the

literature review addressing recent progress on WPT system design, including the state-of-art coil design, converter design and control, and system level design. Shortcomings of previous design methods will be summarized. A comprehensive system design methodology involving innovation in coil design, accurate converter modeling and design, and entire system design method will be proposed to solve the system design challenge.

Chapter 3 presents a novel self-resonant coil with series LC resonance, analyzes its structure and modeling method, and provides a geometric design method to achieve target LC with minimum ESR. The coil has small ESR and compact size. FEA assisted analysis and experimental coil test results are provided to support the coil modeling and working principle.

Chapter 4 presents the accurate modeling of power stages, discusses an analytical model of the 6.78 MHz diode rectifier, and propose ZVS inverter modeling and design. The rectifier model covers arbitrary output. The ZVS inverter design covers ZVS operation for arbitrary loading situations. LTSpice simulation is provided to support ZVS inverter modeling and design method.

Chapter 5 investigates the entire WPT system modeling and design. A comprehensive design method is proposed for minimum total loss while transferring a target amount of power. A 6.78 MHz WPT prototype test results are presented to support system modeling.

Chapter 6 provides a summary of the thesis, draws the conclusion, and discusses future work that expands the usage of the proposed system modeling and design method.

Chapter 2

Literature Review

The call for high efficiency and long transfer distance drives WPT system into 6.78 MHz operating frequency. Such high frequency raises great challenges to WPT system design. The challenges include individual stage design problems such as coil design and converter design problem. The challenges also include system-level design problems such as circuit operation design and control, and the whole system design considering co-design of circuit operation and hardware design of each stage. This chapter reviews recent progress in WPT system design and explores motivation for new work.

2.1 Coil Design

WPT systems consist of WPT converters and transmission coils. The modern soft switching techniques are capable to minimize power converter switching loss, leaving the coil conduction loss as the dominant component of the total WPT system loss [24, 18]. From references [24, 18, 4, 25], the maximum efficiency of a WPT system is limited by the coil quality factor for a given coupling application. Starting from the significance of coil designs, this section reviews the stage-of-art coil design method in WPT. The research into coil design is divided into three paths: design for reduced copper loss, design for reduced compensation capacitor loss, and design for better coupling.

2.1.1 State-of-art Coil Performance

The coil-to-coil maximum transfer efficiency over different coil designs, reproduced according to [24, 18, 4, 25], is shown in Fig. 2.1 under coupling of 0.1. Clearly, improving coil quality factor is of key importance to increase WPT efficiency.

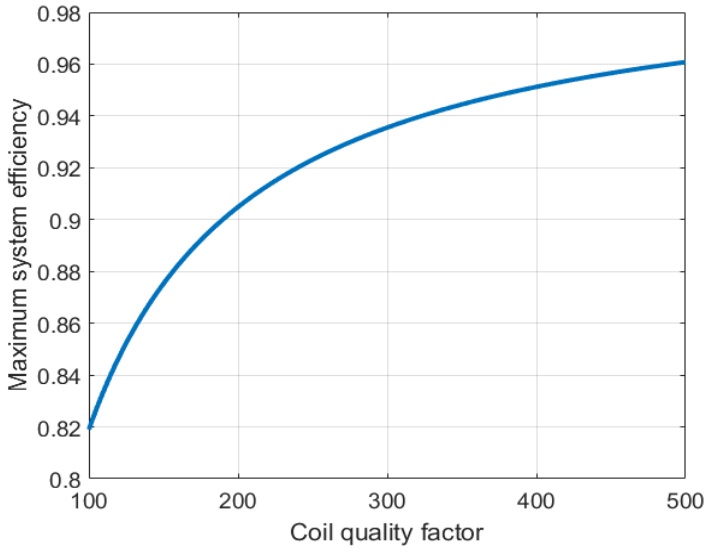


Figure 2.1: Coil quality factor vs. system efficiency.

Table. 2.1 summarizes the state-of-art coils in reported WPT systems. The key parameters, including the working frequency, coil wire, quality factor Q, diameter D, and inductance L are listed in the table. The self-resonant coil is termed as coils using the

parasitic capacitor of the coil itself as the resonant capacitor, instead of using the external lumped capacitor.

Table 2.1: Coil quality factor review.

Reference	Frequency [MHz]	Coil Wire	Self-resonant	Q	D [cm]	L [μH]
[26]	7.64	Solid wire	None	304	59	39
[27]	6.00	Solid wire	None	90	6.8	8.18
[28]	6.78	Foil	None	201	23.5	1.42
[29]	6.78	Foil	None	178	11.3	3.34
[30]	6.78	Foil	Parallel	45	3	0.09
[31]	7.08	Foil	Parallel	1177	6.6	0.16
[32]	7.73	Foil	Series	838	2.1	0.13

Among the reviewed coils, reference [31, 33] are multiple layer self-resonant coils and have high quality factor. However, the inductance values are significantly smaller than other non-self-resonant coils. Such small inductance requires a considerable amount of current to generate comparable magnetic field strength as the non-self-resonant coils, which may reduce system overall efficiency. Reference [26] has large inductance and high quality factor compared with other coils. However, the diameter is prohibitively large to be applied into consumer electronics applications. The achievable quality factor of such solid wire spiral coil drops significantly if made to be around 10 cm according to reference [31], as verified by the other solid wire coil in reference [27]. Reviewing all the coils, it is found a coil with large inductance, high quality factor, and compact is missing in literature.

2.1.2 Coil Design for Reduced Copper Loss

Compared with kHz WPT, 6.78 MHz WPT reduces the need for a ferrite core due to the reduced need for inductance. Air-cored coils are widely applied in many reported WPT systems [24, 29, 20]. The coil loss only consists of copper loss. In addition to DC copper resistivity, an increased copper loss incurs in the coil windings due to skin and proximity effect. The skin effect is current increasingly crowding to the surface of the conductor due to the presence of eddy current inside the copper, which is caused by the magnetic field inside

the copper. The effective conduction depth (termed as "skin depth") is reduced to

$$\delta = \sqrt{\frac{\rho_{copper}}{\mu \pi f_s}} \tag{2.1}$$

where ρ_{copper} is DC resistivity, μ is the absolute magnetic permeability of the conductor, and f_s is switching frequency. Fig. 2.2 shows the skin depth vs. frequency.

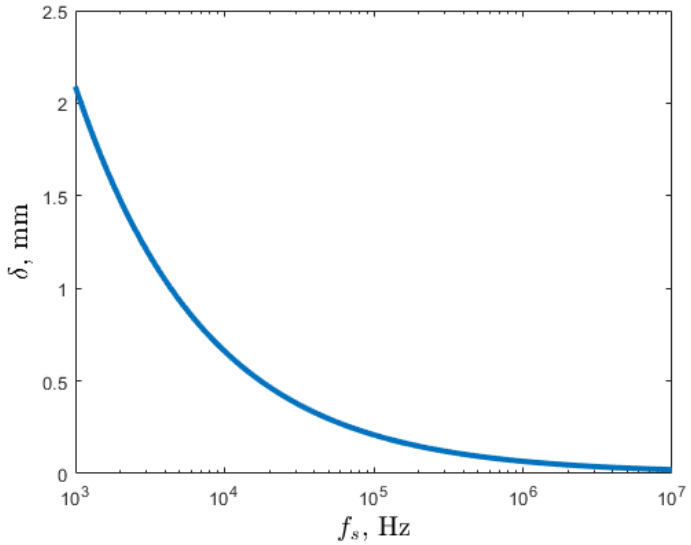


Figure 2.2: Skin depth vs. frequency.

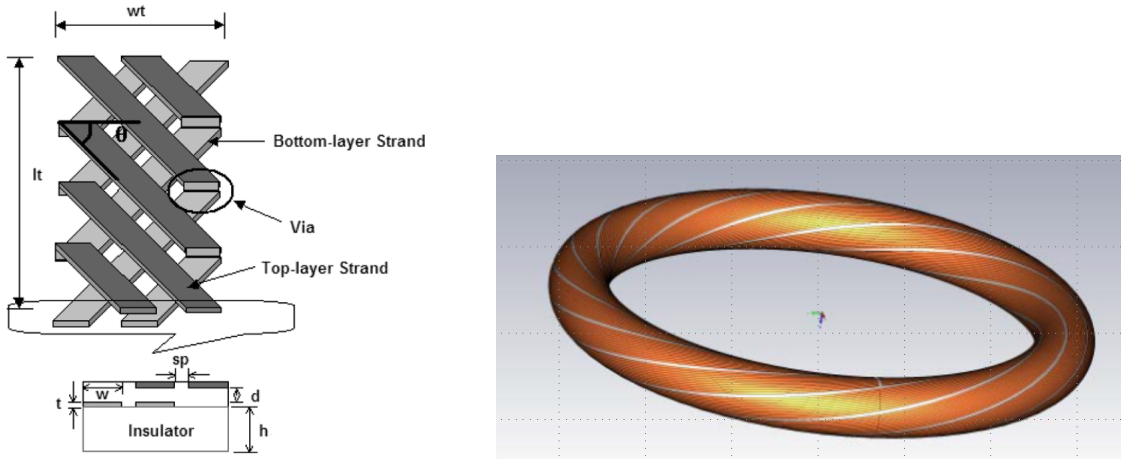
The current distribution becomes more crowding considering the additional eddy current incurred in the adjacent surfaces of neighboring turns, which is produced by the magnetic field of the neighboring turns. This effect is termed as "proximity effect". The skin and proximity effect in total is called "eddy current effect". The eddy current reduces effective conduction area and leads to an increased ESR.

One method of reducing coil ESR is changing wire structure to reduce eddy current effect and increase effective conduction area [4, 2, 33, 3]. Litz wire is fundamental to those new structures [4]. Litz wire maximizes effective conduction area by weaving together smaller, individually-insulated wires to form larger wires. Through making the individual strand thinner than a skin-depth, it does not suffer an appreciable skin effect. Furthermore, with the weaving of the wires, the magnetic coupling between adjacent wires are canceled. As a

result, each strand has a similar impedance and current sharing when conducting AC circuit, reducing the proximity effect.

Litz wire is widely used in applications with a frequency range from tens of kHz to hundreds of kHz, and exhibits reduced loss compared to solid wire [4, 24]. When the operating frequency increases to the MHz range, the requirement for the diameter of each strand becomes increasingly difficult to meet, as shown in Fig. 2.2, and the wire becomes prohibitively expensive [6].

The thin copper foil with a comparable thickness to the skin depth is widely used in MHz applications and suffers less current crowding [6]. For example, in 6.78 MHz applications where the skin depth is 25 µm, copper foil with comparable thickness is commercially available and not expensive. Further, foil coil is capable to be wound in a Litz wire structure to reduce proximity effect, as reported in references [2, 33]. Fig. 2.3a shows how the foil is weaved on a planar substrate forming a planar Litz [2]. Fig. 2.3b shows how the foil is weaved along a substrate tube forming a three-dimensional (3D) Litz called "surface spiral coil" (SSC) [3].



(a) **(b)**

Figure 2.3: Picture showing the schematic of the planar Litz (a) [2], and 3D Litz (b) [3].

Aside from changing wire structures to reduce eddy current effect, coil geometric optimization is another method reducing coil ESR [34, 35]. Coil geometric optimization involves coil modeling to bridge electric parameters with geometric parameters such as the number of turns, width, and pitch, and optimization design that specially designs the coil

geometry to reduce ESR under certain electric constants [34, 35]. Coil modeling method has been widely studied for solid copper wire [36], Litz wire [37], copper tube [21], and planar PCB coils [13]. The modeling method potentially can be used to develop geometric optimization design method for minimum ESR as in reference [34].

2.1.3 Coil Design for Reduced Compensation Capacitor Loss

The resonant WPT system uses capacitors to compensate coil reactance. Film and ceramic capacitors are commonly used [4, 38, 39, 40] because of their good thermal stability and the excellent loss characteristics [4]. However, the compensation capacitor loss may be comparable with the coils loss, especially in the application where the coil has been optimized for low loss [4].

One method to reduce the capacitor loss is using capacitor array that consists of multiple capacitors in series and parallels to obtain reduced ESR with the desired capacitance [4, 24, 20] at the expense of volume. Fig. 2.4 is a picture showing the capacitor arrays in a 100 W, 200 kHz WPT prototype [20]. Clearly, the array volume is prohibitively large to be applied in consumer electronics applications where size and cost are crucial concerns. The capacitor array in other frequencies and power-levels may have a different size than what is shown in this prototype. However, the size has been increased. Furthermore, the repeated connection terminals introduce extra ESR and may be lossy [3].

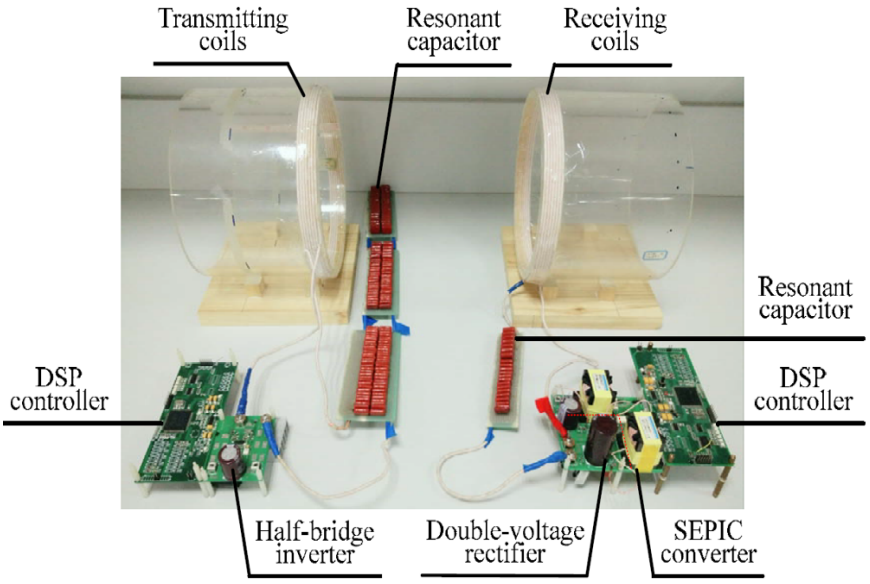


Figure 2.4: An array of capacitors in a 100 W, 200 kHz WPT system [4].

Another method to reduce the capacitor loss is using coil parasitic capacitance to compensate coil inductance, eliminating the external lumped capacitor [5, 6, 41, 37, 7, 21, 13, 36]. Coil parasitic capacitance widely exists in neighboring structures such as the adjacent turns of a tightly wounded coil [36], the adjacent strands in a Litz wire [37], and the neighboring conductor layers in a parallel-plate-shaped coil [5, 6, 7]. More specifically, reference [5] uses two copper layers of a PCB coil as the parallel-plate structure providing the parasitic capacitance. Reference [6] is a multiple layer ring-shaped planar inductor with the adjacent layers forming the parallel-plate structure and providing the parasitic capacitance. Reference [7] adds auxiliary conductor layer on top of the coaxial cable forming the parallel-plate structure and capacitance. The coil structures and connection methods are shown in Fig. 2.7 [7], Fig. 2.6 [6], and Fig. 2.5 [5].

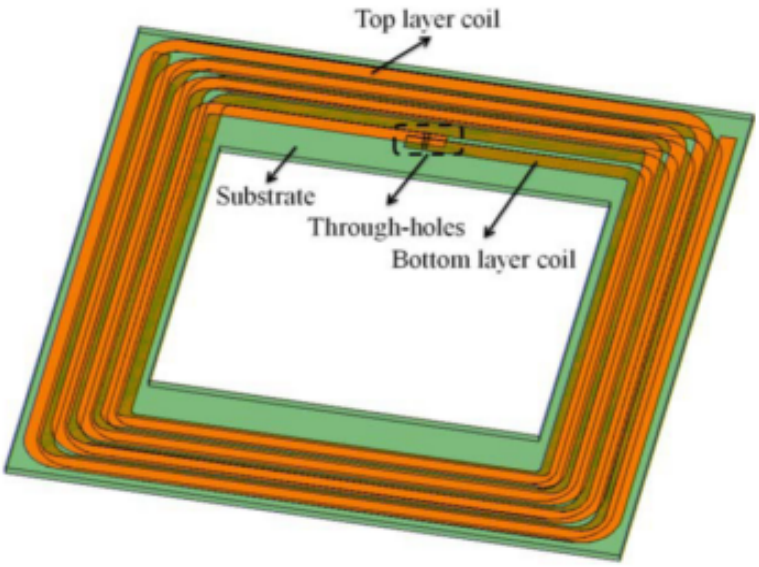


Figure 2.5: Coil structure and connection method of the double-layer PCB coil [5].

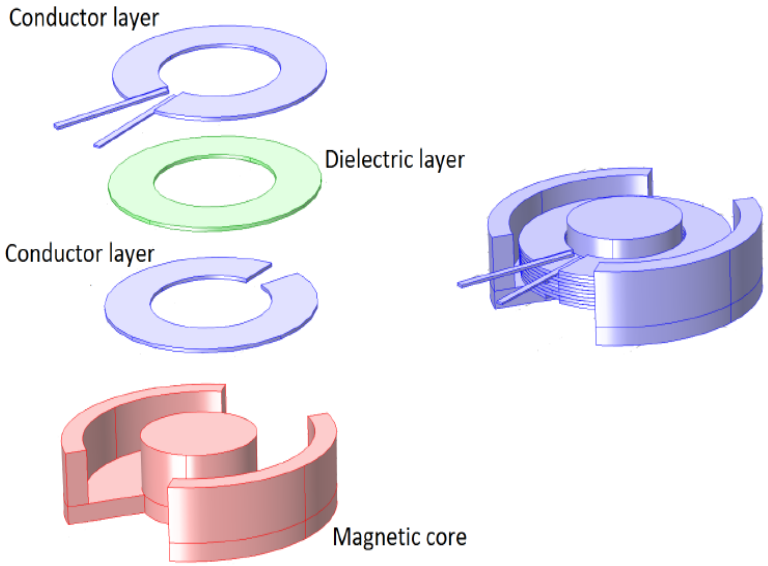


Figure 2.6: Coil structure and connection method of the ring-shaped multiple layer capacitor [6].

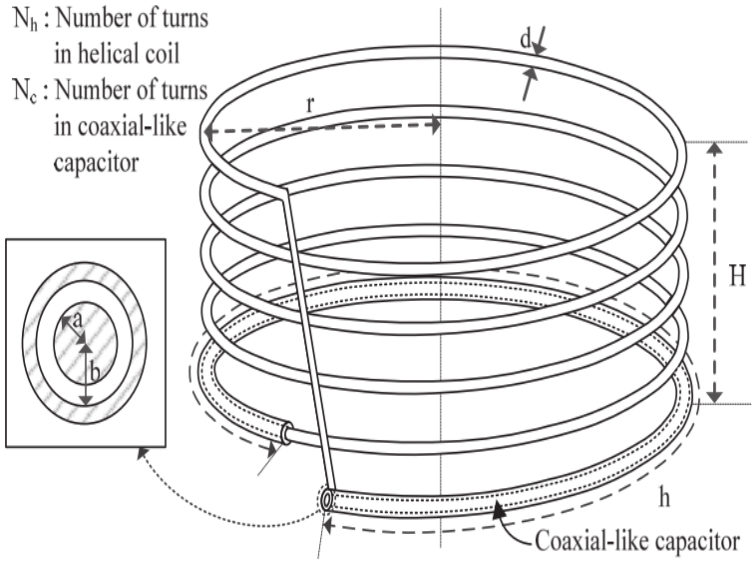


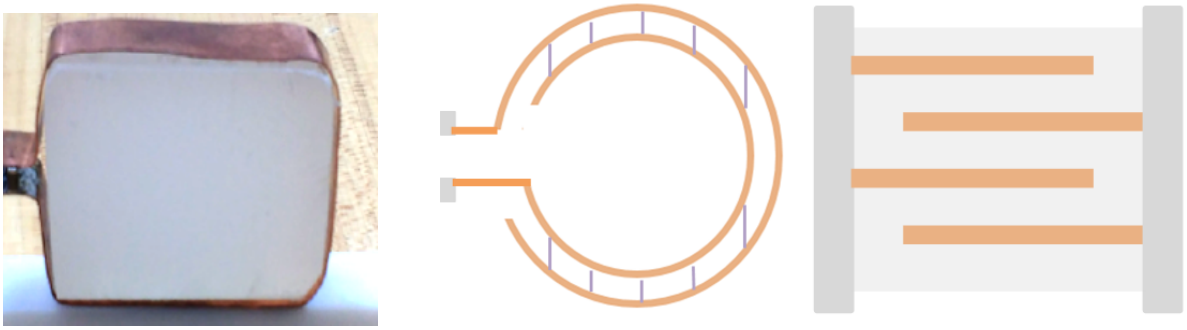
Figure 2.7: Coil structure and connection method of the coaxial cable coil with auxiliary conductor layer [7].

Due to the exposed electric field in the air, coils using the parasitic capacitance between adjacent turns [36, 37] have the potential to interfere with, or damage, nearby electronic components. In contrast, the parallel-plate-shaped coils use confined electric field between conduction layers inside a dielectric [5, 6, 32]. The confined field is non-sensitivity to neighboring objects, making the parallel-plate-shaped resonant coils safer and have a stable capacitance.

In the above-reviewed coils, the parasitic capacitance is in parallel with the coil inductance, forming a parallel LC resonance. Coil exhibits zero impedance to AC voltage sources due to the parallel capacitance, thus requiring additional impedance matching elements when connecting to voltage source inverter (VSI). The impedance matching elements increase loss, space, and cost. The majority of reported self-resonant WPT coils to date exhibit a parallel LC resonance and require impedance matching when connecting to VSI [5, 6, 37, 7, 21, 13, 36].

In [41], a self-resonant coil is reported with series LC impedance and is suitable to directly connect to a VSI without impedance matching. Coil prototype and structure are shown in Fig. 2.8a and Fig. 2.8b. This coil uses the multiple layer copper forming the parallel-plate capacitance. The copper layers are blended to force current flow in a circle, forming the

inductance. Due to the single turn inductor structure, this coil produces a limited amount of inductance. Sufficient capacitance is required to lower the resonant frequency, leading to a problematic height for consumer electronics application. Besides, this reference provides no ESR or inductance modeling or design method for the reader to explore the limit of coil performance.



(a) **(b)**

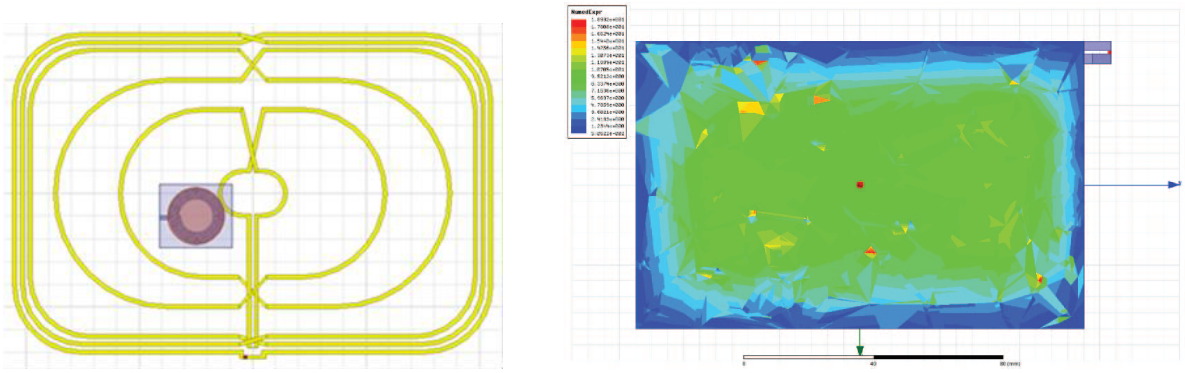
Figure 2.8: Coil prototype of the series LC impedance coil (a) [2], and coil structure similar to a multiple layer capacitor but with blended conductor layer (b).

2.1.4 Coil Design for Uniform or High Coupling

Coupling is an important factor that influences WPT system efficiency [24, 18, 4]. Coil design to shape the magnetic field (H-field) for better coupling is another research topic in coil design [9, 42, 10]. In this, the H-field modeling bridges the field distribution with coil geometry, providing the freedom of alerting field distribution (or equivalently, coupling) via designing coil geometry. The applications and design goals are divided into two paths: geometric design for uniform field distribution against misalignment in varying position applications [9, 10], and geometric design for maximum coupling in fixed position applications[42].

In varying position applications, reference [9] reports the geometric design of a planar coil to produce the minimum field variation near the coil surface. The pitch between each turn is specifically designed to achieve a minimum H-field variation under a set of constraints (i.e. maximum size). The optimized shape is shown in Fig. 2.9a [8]. The corresponding uniform H-field is shown in Fig. 2.9b [9]. It should be noted the two terminals of this coil 2.9a

are connected through the outer side. This purely-symmetric structure offers more evenly distributed H-field than traditional coils which are connected from inner side and outer side.



(a) **(b)**

Figure 2.9: Intel coil structure (a) [8] and the uniform surface H-field (b) [9].

Besides 2D coil design for uniform surface H-field, references [9, 10] report 3D bowl coil to produce uniform magnetic field perpendicularly to the side or the bottom. The uniform perpendicular field is required because the devices in a bowl are usually perpendicular to the surface [10]. In additional to geometric design, reference [10] uses multiple coils to form the 3D bowel with each coil conducts a specially modulated current to shape a uniform H-field perpendicular to surfaces. Multiple inverters are required to excite the coil array which increases cost, size and loss. The 3D bowel utilizing a single coil is shown in Fig. 2.10a. The 3D bowel implementing coil array is shown in Fig. 2.10b.

(a) **(b)**

Figure 2.10: Bowel coil consisting of single coil (a) [9] and bowel coil consisting of coil array (b) [10].

In fixed positions applications, reference [42] optimizes a set of spiral coils to have the highest coupling design various space between adjacent turns. Th similar method is applied that first modeling coil coupling with coil geometries then optimizing geometry for maximum coupling.

2.2 Converter Modeling, Design and Control

This section reviews the stage-of-art converter modeling, design and control for WPT. The function of the converter in WPT system is realizing power conversion with high efficiency.

Converter loss consists of device conduction loss, device switching loss, and passive component loss. In transitioning from kHz to 6.78 MHz, device switching loss increases by over one order of magnitude because switching loss scales with operating frequency. In consumer electronics applications where turn-off loss is small due to the low current low voltage application, turn-on loss dominants the switching loss and zero-voltage-switching (ZVS) operation of all devices is a primary concern [11]. Also, the obviously magnified switching frequency causes resonant transition times to constitute a significant portion of the switching period, leading to a more complicated characteristics of the diode rectifier.

2.2.1 Converter Design for ZVS

ZVS techniques are widely applied in reported WPT systems [38, 24, 39, 11, 43, 44]. The fundamental principle is designing a current that lags the turn-on of the device. The lagging current flows through and fully discharge the output capacitance C_{oss} before a gate-source voltage is applied to turn-on the device, eliminating turn-on loss. Reference [38, 24] use load current to discharge the C_{oss} energy, however, in WPT applications the load may change drastically due to position or power variations and may cause ZVS failure due to the change of current phase or amplitude. To ensure ZVS over wide load range, reference [39, 11] add an auxiliary inductive tank across the switch node to provide additional inductive current for the device ZVS. The topology, re-produced from reference [11], is shown in Fig. 2.11.

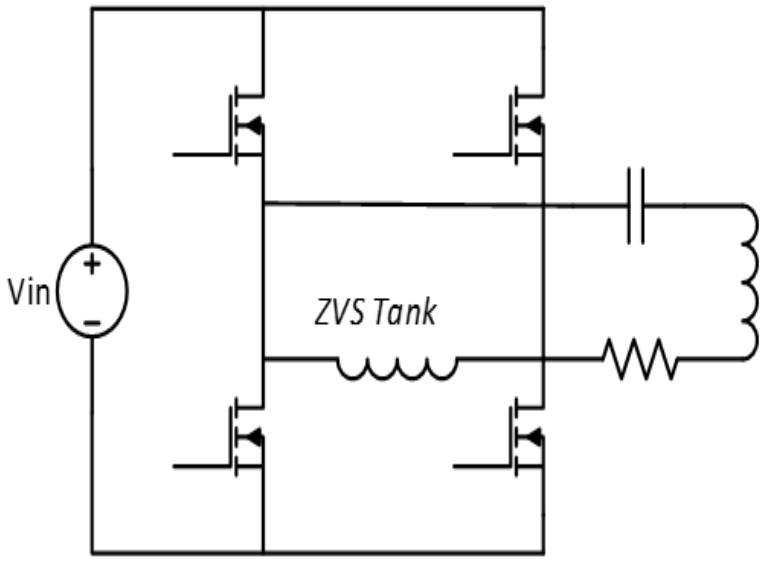


Figure 2.11: ZVS inverter with auxiliary tank [11].

The traditional modeling covers a simple situation that only the ZVS tank current transfers C_{oss} energy [39, 11]. When the load current is much smaller than the ZVS current [39], or the load is resistive [11], the load current has little contribution compared with ZVS current and thus is ignored when building the ZVS transient model. In WPT applications, however, the phase of load current may change from capacitive to the inductive, and the amplitude may be comparable with ZVS current, based on design. A ZVS inverter modeling considering the load current together with the ZVS tank current is missing in the literature.

2.2.2 Converter Design and Control for Voltage Regulation and Efficiency Control

As a special power source, WPT system is desired to efficiently transfer power with the regulated output voltage. In many reported WPT systems, the receiver side rectifier is connected to a DC-DC converter for output voltage regulation. And the inverter is connected to a DC-DC converter for input voltage regulation which is used to tune the equivalent load for minimum system loss, termed as "optimal load control" [39, 4]. Though the optimal load control maximize system efficiency for a given hardware implementation, the multiple stages structure may have a high accumulated total loss from each individual part.

Converter designs and control methods are proposed to reduce stages while still utilizing output voltage regulation and efficiency maximization [11, 38, 45, 46]. In references [11, 38, 45, 46], active rectifier using phase shift control [45, 46] or pulse modulation modulation (PDM) control [11, 38] are proposed to eliminate the DC-DC stage connected to the diode rectifier or inverter. The simplified converter structure has less number of component, which may lead to a lower total loss. However, the active bridge has some design problems that need to be considered. The phase shift control causes unbalanced current on each phase leg, leading to ZVS design problems [11, 39]. Reference [39] uses an auxiliary tank to solves the ZVS problem. However, the additional tank increases size and cost. PMD has identical current sharing on both phase legs. Thus, PMD bridge may eliminate the need for ZVS tank if the load current is designed inductive and large enough for device ZVS. However, the non-uniform pulse density causes current amplitude ripple in the coil and devices, which increases conduction loss.

Class-E rectifier [43] and inverter [44] are also reported to eliminate DC-DC stages, reducing system components and loss. However, class-E topology is only capable to efficiently operate over a narrow range of the load around the design optimal load. Beyond this range, the inefficiency of the converter may cause system failure or even damage the switch. In contrast, class-D topology with an auxiliary tank is capable to maintain ZVS over a wide range of loading situations.

2.2.3 Diode Rectifier Reactive Power

In relatively low frequency and high power applications, diode reactive power is generally ignored due to the negligibly small portion of the transient time. The diode rectifier is modeled as a resistive load and matches well with experiment results [11, 38, 45, 46, 24].

In transient from previous kHz WPT to the target 6.78 MHz WPT, the obviously magnified switching frequency causes resonant transition times to constitute a significant portion of the switching period. Because the resonant transition intervals are expected to be significant in the proposed application, the diode rectifier exhibits a strong capacitive impedance, as shown in Fig. 2.12a from an example WPT system [12]. The reactive power causes significantly efficiency drop when not compensated properly, as shown in Fig. 2.12b [12].

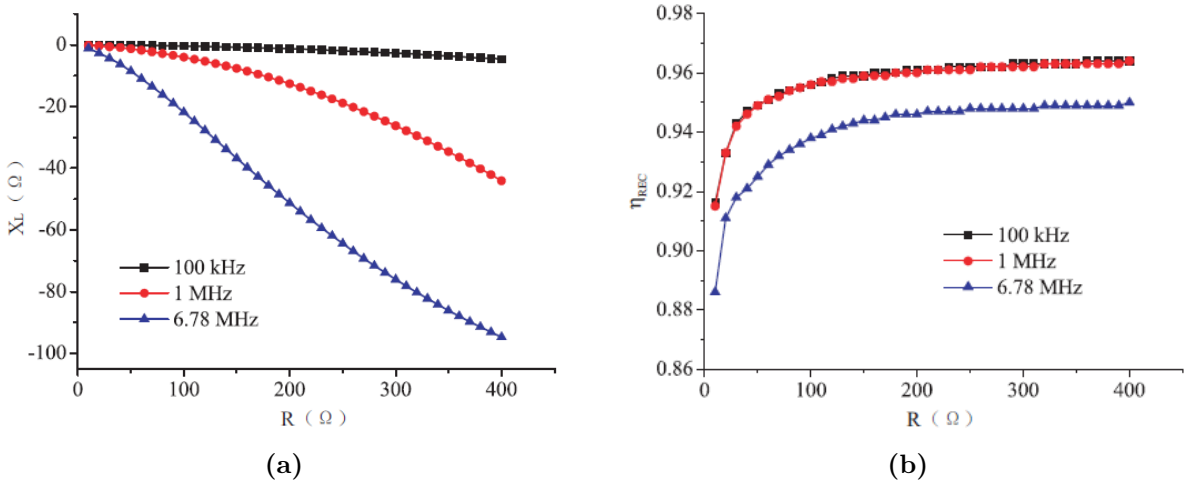


Figure 2.12: Diode reactance of a example WPT system (a) and system efficiency (b) at different frequencies [12] .

Wide research into diode reactance modeling and compensation are reported in reference [12, 47, 45, 40]. The diode rectifier reactance is modeled in [12, 47] where a couple of different output voltage and power are simulated and the reactance modeling is derived through curve fitting. However, the accuracy of the simulation-assisted curve fitting model depends on the number of simulated load. And it cannot cover arbitrary output accurately. A diode model that covers wide load range accurately is missing in literature.

To compensate diode bridge reactive power, a fixed capacitor [12] or a switched array with multiple capacitors and switches [47] may be used. The array has the ability to dynamically compensate the reactive power for different circuit operation, but cannot fully compensate due to the finite number of capacitors and steps. Moreover, the array takes larger space and add more cost. Another method to achieve reactive power cancellation is utilizing an active rectifier that has the ability to regulate the input impedance. The rectifier in [45, 40] replaces the diodes in a full bridge diode rectifier with GaN switches to form a synchronous full bridge rectifier. By means of detecting the current phase and controlling the time of switching, synchronous full-bridge rectification provides the ability to control the rectifier input phase and therefore input impedance. Furthermore, an active rectifier has the ability to almost continuously regulates the reactance. However, active bridges require special ZVS designs, and the additional driver and control circuit is not preferred in the receiver in consumer electronics applications.

2.3 System Design Method for High Efficiency

WPT system design is a large topic which includes the previously reviewed individual stage hardware design, and circuit operating (input and output voltage) control for fixed hardware implementations. It also includes system level design considering hardware and circuit operating together. The end-to-end efficiency of the state-of-art reported WPT systems are summarized in Table. 2.2. The key parameters, including operating frequency f_s, coil diameter D_c, power transfer distance d, coupling coefficient k, output power P_o, and overall efficiency η are listed in the table. The normalized distance is defined as d/D_c. The normalized distance is considered because it is related to the coupling which is a major limiting factor in the efficiency.

Table 2.2: WPT system end-to-end efficiency review.

#	Reference	f_s [MHz]	D_c [cm]	d	d/D_c	k	P_o [W]	η [%]
1	[26]	7.65	59 (28)	70	1.61	–	12	50
2	[28]	6.78	23.5	5	0.21	–	24	73
3	[29]	6.78	11.3	4	0.38	–	10	72
4	[48]	6.78	11.3	5	0.44	0.18	10	80
5	[49]	13.56	20	10	0.50	0.075	40	76
6	[11]	0.91	30	20	0.68	0.08	10	89
7	[11]	0.91	30	40	1.33	0.02	10	73

Generally, it is discovered that WPT system with tens of Watt power level has an efficiency lower than 90 %. And the efficiency tends to drop with increasing of d/D_c. Research into WPT system design for higher efficiency still has a long way to go.

In many relatively high-power and low-frequency applications, it is discovered that the coil conduction loss dominates the system loss, and the coil conduction loss can be minimized through optimal load control [24, 50, 4]. The highest achievable efficiency for a given WPT system hardware is determined by the product of coil quality factor and coupling coefficients [24, 50, 4]. Based on this analysis, traditional systems level design apply two principles to achieve high-efficiency design: increase coil quality and coupling to increase maximum achievable efficiency, and apply optimal load operation to achieve that efficiency.

Reference [4, 25] analyze the system level design for a 5 kW, 85 kHz range WPT application. In this, the optimal load operation is achieved by specially designing the ratio of Tx and Rx coil inductance. The maximum achievable efficiency is optimized by iteration of a wide range of Tx and Rx coil that has difference inductance and coupling but still satisfies the optimal ratio and are within geometrical constraints.

Aside from using coil inductance ratio to achieve optimal load operation, the previously reviewed references [24, 50] use dual-side voltage control to achieve optimal load operation. High quality factor coils are build to enhance maximum achievable efficiency.

However, the system-level design method for relatively high-power and low frequency applications is based on assumptions that are not generally true for 6.78 MHz consumer electronics applications due to the neglect of ZVS requirement and diode rectifier reactance. In 6.78 MHz WPT applications with wide load range, the inverter may lose ZVS and the reactance may cause significant efficiency drop. A comprehensive system design method considering device ZVS, diode rectifier reactance, coils and converter, and circuit operating is missing in literature.

2.4 Summary and Motivation

The call for high efficiency and long transfer distance drives WPT system into 6.78 MHz operating frequency presenting great challenges to WPT system designs. Motivated by the need for a WPT system which exhibits high efficiency and compact size, this chapter reviews the state-of-art coil design, converter design, and system design methods. Through careful review, it is discovered that series self-resonant coil is promising to reduce system loss, but current design method of series self-resonant coils is insufficient due to the limited inductance, prohibitively large thickness, and lack of modeling to explore the performance limit. The current power stage design method is insufficient or inaccurate for WPT applications and designs where wide loading situations need to be considered. The system-level design method is based on assumptions that are not generally true due to the neglect of ZVS requirement and diode rectifier reactance.

To solve these disadvantages, previously established techniques in coil design will be applied to invent a new series self-resonant coil structure for reduced ESR while achieving a compact size. Previous ZVS inverter and diode rectifier topology will be combined with accurate waveform and circuit analysis to develop new modeling and design method for a wide load range. From the resulting coil and converter models, a holistic system design considering the co-design of individual stages will be detailed. The necessary consideration of the interdependence among the ZVS design, rectifier reactive power, coil design, and circuit operation are highlighted.

Chapter 3

Analysis and Design of a Series Self-resonant Coil for Wireless Power Transfer

It is discovered from literature that series self-resonant coil is promising to reduce system loss. However, current design method of series self-resonant coils is insufficient due to the limited inductance, prohibitively large thickness, and lack of modeling to explore the performance limit. To solve these disadvantages, previously established techniques in coil design are applied to invent a new series self-resonant coil structure for reduced ESR while achieving a compact size. The coil structure, model and design method, will be detailed in this chapter.

3.1 Proposed Structure and Operation Principle

Fig. 3.1 shows the proposed coil structure. The coil consists of two identical planar spiral coils separated by one layer of dielectric material. The two copper spirals are designed to provide the resonant inductance. The inserted dielectric material is designed to form the resonant capacitor between the two copper layers while fixing their position. When implemented, there is no air gap between the three layers. Terminals a and b are connected to the ac source (e.g., WPT inverter) while the other two Terminals $a$re left open. Due to complete separation of the two conduction layers by the dielectric, the coil is an open circuit for a DC source. When an AC source is applied, current flows from one terminal to the other crossing through the dielectric, resulting in a series LC impedance.

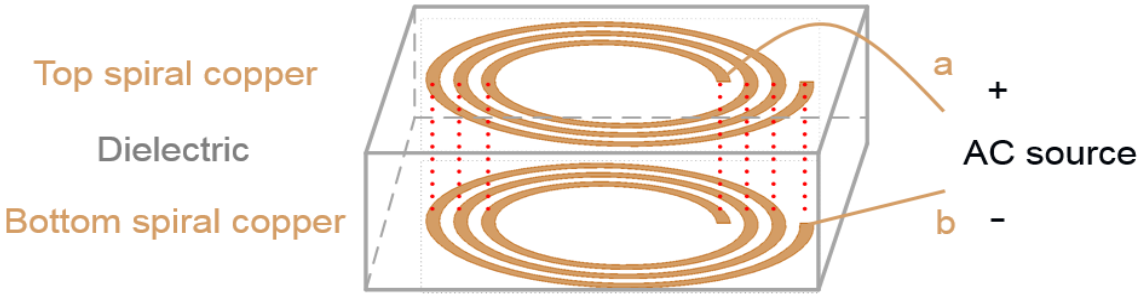
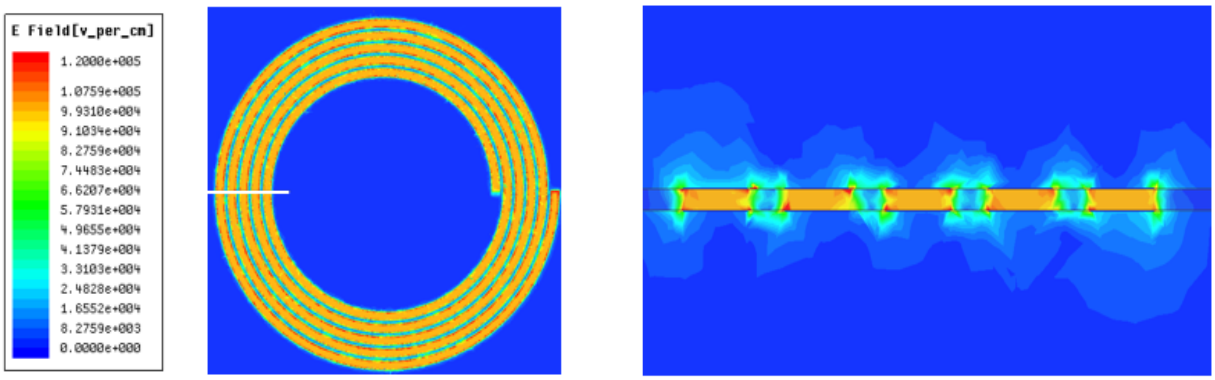


Figure 3.1: Diagram showing the structure of the proposed coil.

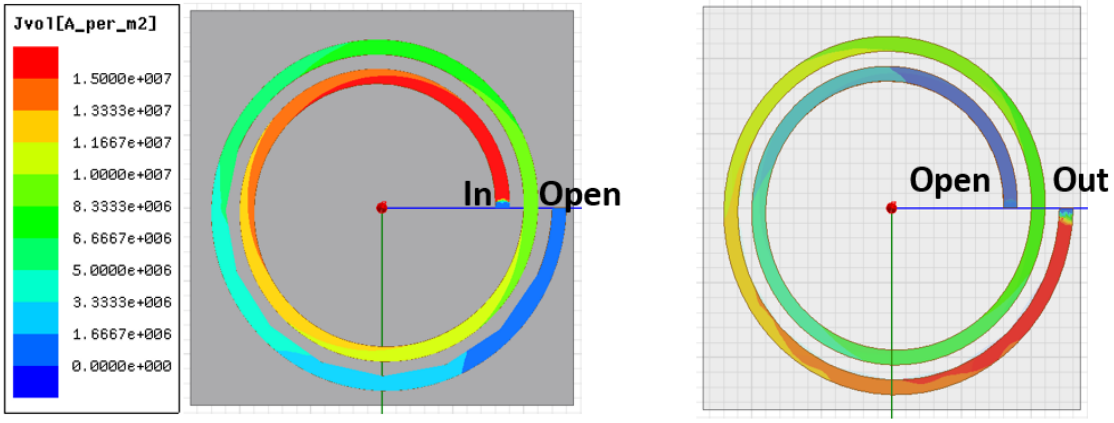
Similar to a parallel-plate capacitor, the current transients between two layers in the form of displacement current $J_d = \varepsilon_r \varepsilon_0 \partial E/\partial t$ where ε_r is the relative permittivity of the dielectric material. The uniform distribution of the electric field, as shown in Fig. 3.2, leads to the uniform distribution of J_d long the whole length and width of the coil in the dielectric.

Due to the uniform J_d, the input current linearly transitions from the input terminal a on the top spiral to the output Terminals b on the bottom spiral over the length of the coil. At the Terminals a and b, the entire coil current flows through one of the spiral conductors, with zero in the opposite conductor. The simulated current distribution pattern on the two copper spirals is shown in Fig. 3.3 which agrees with the analyzed current distribution.



(a) **(b)**

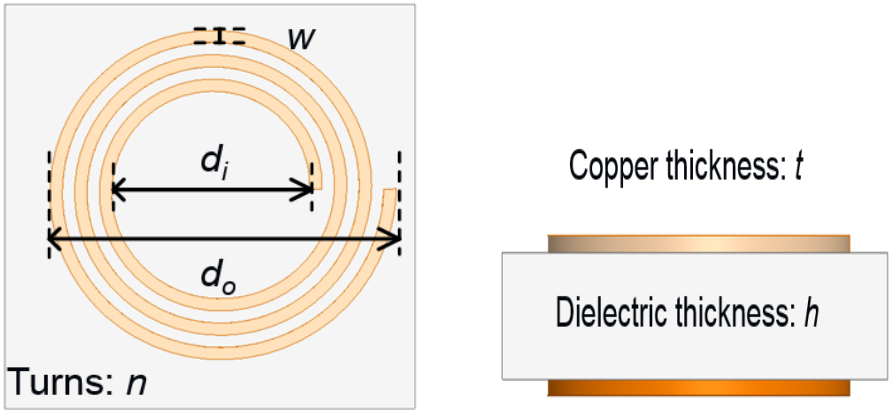
Figure 3.2: Simulated E-field (a) top view, and (b) cross-section view @ 6.78 MHz.



(a) **(b)**

Figure 3.3: Simulated current density distribution (a) top view, and (b) bottom view.

The geometric parameters of the spiral track are shown in Fig. 3.4. w is the width of each turn, s is the distance from the inner radius of one turn to the inner radius of the adjacent turn, d_i is the inner radius, and d_o is the outer radius. Additionally, n is the number of turns of one spiral layer, and h is the thickness of the dielectric layer. t is the copper thickness.



(a) **(b)**

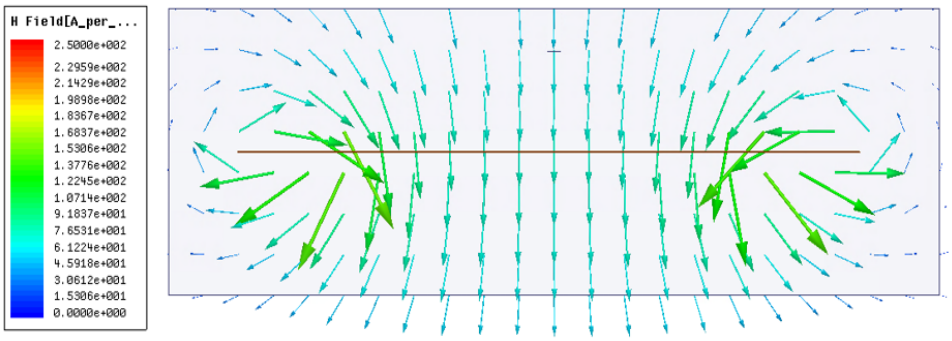
Figure 3.4: Geometry of the proposed coil (a) top view, and (b) cross-section view.

3.2 Analysis and Modeling

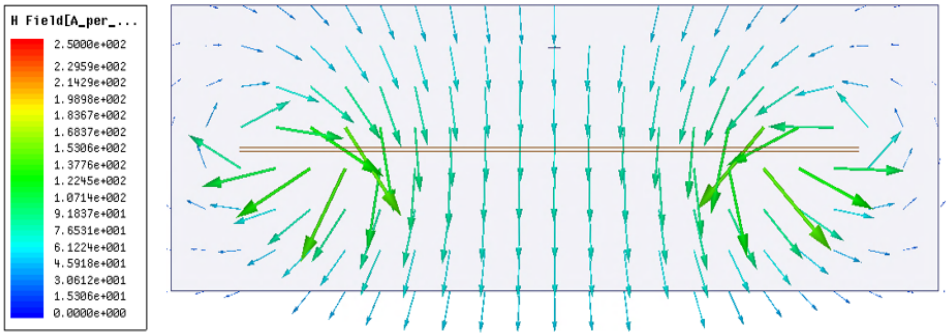
In order to examine the performance capabilities, analytical models for the inductance, capacitance, and resistance are developed based on results from the literature and FEA-assisted simulation. L is analyzed based on magnetic field simulation. C is analyzed based on electric field simulation. And R is analyzed based on current distribution.

3.2.1 Inductance

The top and bottom layer of the proposed coil have identical current flow directions (i.e. from input terminal towards output terminal). Compared to a single spiral coil, the current flow in the proposed coil differs only in that it crosses vertically through the dielectric layer (i.e. in the plane of the page in Fig. 3.4b). Both layers have identical current flow direction (When the dielectric thickness is thin relative to the w, the magnetic flux distribution of the proposed self-resonant coil and the traditional single layer spiral coil are nearly identical, shown in Fig. 3.5. Therefore the two coils have the same inductance.



(a)



(b)

Figure 3.5: Flux distribution of traditional coil (a), and the proposed self-resonant coil (b) when conducting 1 A, 6.78 MHz current .

As analyzed in [34], the inductance of a planar spiral coil is

$$L_{spiral} = \frac{\mu n^2 d_{avg}}{2}(\ln\frac{2.46}{k_u} + 0.2{k_u}^2) \tag{3.1}$$

where μ is the magnetic permeability, d_{avg} is the average diameter $d_{avg} = (d_o + d_i)/2$, $k_u = (d_o - d_i)/(d_o + d_i)$. Therefore the inductance equation for the proposed coil is

$$L_s = \frac{\mu n^2 (d_i + d_o)}{4}\left(\ln\frac{2.46(d_i + d_o)}{d_o - di} + 0.2\left(\frac{d_o - d_i}{d_o + d_i}\right)^2\right) \tag{3.2}$$

From reference [34], this expression exhibits a typical error of 3 % when compared to FEA analysis.

3.2.2 Capacitance

The simulated E-filed has been plotted in Fig. 3.2. The electric field of the proposed structure is similar to a parallel plate capacitor. The E-field is composed of two parts: the primary electric field located vertically between the two conductor layers and inside the dielectric, and the fringing field located between adjacent conductors. Fig. 3.6, reproduced from [13], shows the electric field of the double layer planar coil for an example geometry.

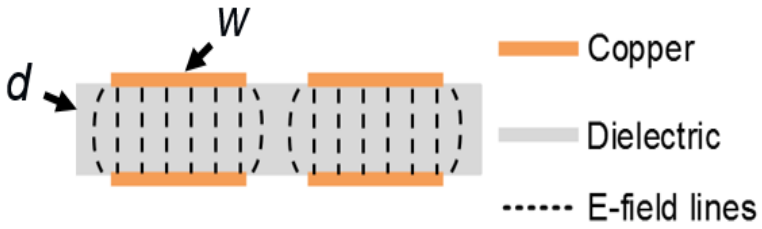


Figure 3.6: Schematic showing the electric field of a double-layer PCB coil [13].

The electric field with fringing effect has been widely researched in the literature [13, 51]. The work in [51] summarized various calculation formulae and verified them with simulation results, proposing an accurate model of the capacitance with less than 5 % error

$$C_s = \frac{\varepsilon_r \varepsilon_0 \pi w n (d_i + d_o)}{2h} \left[1 + \frac{h}{\pi w} \ln \frac{2h}{\pi w} + \frac{h}{\pi w} \ln \left(1 + \frac{2h}{\pi w} + 2\sqrt{\frac{t}{h} + \left(\frac{t}{h}\right)^2} \right) \right] \tag{3.3}$$

where $l_0 = \pi n (d_o + d_i)/2$ is the total length of one spiral copper foil.

3.2.3 Resistance

The total loss of the proposed self-resonant coil consists of copper loss and dielectric loss. The copper loss is modeled as skin-effect loss plus proximity effect loss [6]. The skin effect loss is calculated through the integration of the loss density over the whole coil. The proximity loss is through the calculation of the proximity field on each turn, and calculation the proximity loss afterward.

As has been discussed, the input current linearly transitions from the top to bottom spiral over the whole length of the coil. At the terminals, the entire coil current flows through one of the spiral conductors, with zero in the opposite conductor. In Fig. 3.7, the spiral coil has been unwound into straight tracks to better show the current distribution.

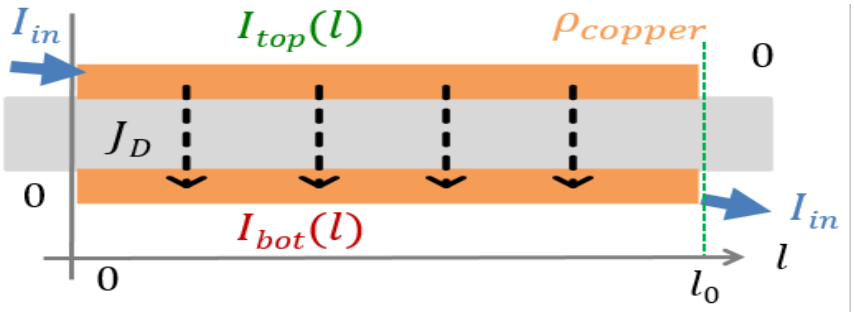


Figure 3.7: Current distribution along the whole length.

The bottom layer collects displacement current from top layer:

$$I_{bot}(l) = \int_0^l J_d w dl = \frac{l}{l_0} I_{in} \tag{3.4}$$

The top layer transfers current to bottom layer while both sides add up to I_{in}:

$$I_{top}(l) = I_{in} - I_{bot}(l) = (1 - \frac{l}{l_0}) I_{in} \tag{3.5}$$

Due to skin effect, the current inside the copper is increasingly crowing towards the dielectric and the effective conduction area is [52]

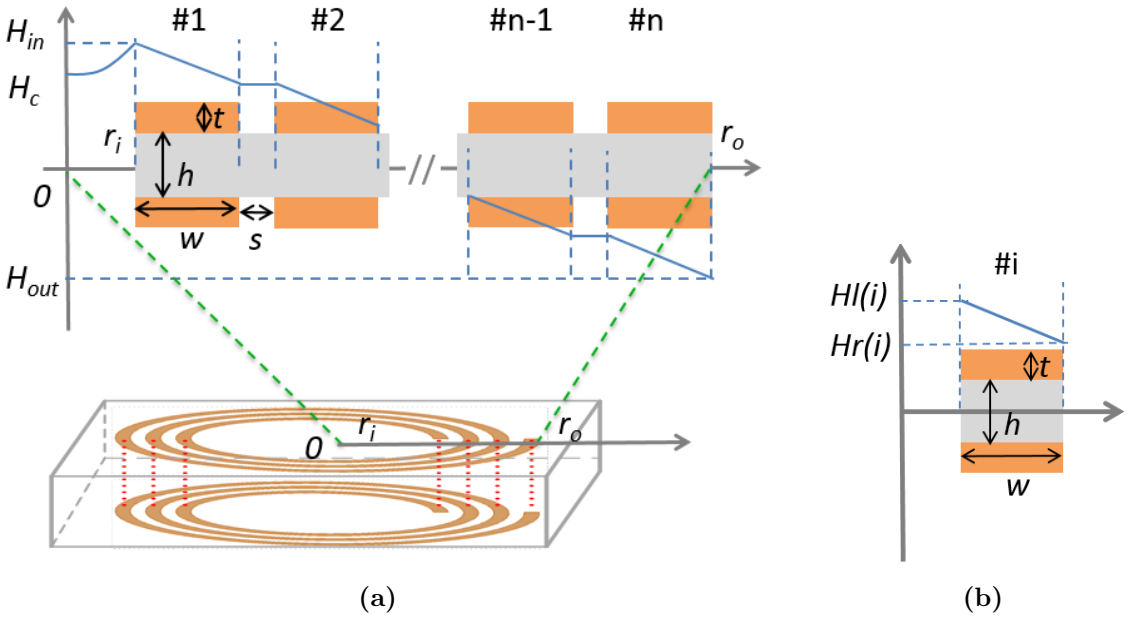
$$A_e = w\delta(1 - e^{-\frac{t}{\delta}}) \tag{3.6}$$

The skin effect ESR when conducting I_{in} is

$$R_{skin} = \frac{1}{I_{in}^2} \int_0^{l_0} \left(I_{top}(l)^2 + I_{bot}(l)^2\right) \frac{\rho_{copper}}{A_e} dl = \frac{2\rho_{copper}\pi n(d_i + w + n \cdot s)}{3w\delta(1 - e^{-\frac{t}{\delta}})} \tag{3.7}$$

In addition to skin effect, the time-varying H-field around the coil causes the eddy current loss in the copper foil. Since the H-field in the self-resonant coil has an almost identical H-field to a single spiral, the resonant coil H-field distribution can be calculated using the

H-field calculation from previous publication [53]. In this, the spiral shape is simplified to multiple concentric rings. Fig. 3.10 is a cross-section view showing the resonant coil H-field. the y-axis is H-field strength and the x-axis is the position from coil center to coil edge.



(a) (b)

Figure 3.8: Cross section view of the resonant coil H-field (a), and the zoom-in of ith turn (b).

H_c is the H-field strength at the center point. H_{in} is the H-field strength at the innermost point. H_{out} is the outermost field. The H-field strength drop on each turn $dH = H_{in} - H_{out})/n$. Using H-field calculation of spiral coil [53]

$$H_c = \frac{nI_{in}}{(d_o - d_i)} \ln \frac{\sqrt{d_o^2 + t^2} + d_o}{\sqrt{d_i^2 + h^2} + d_i} \tag{3.8}$$

$$H_{in} = H_c \exp^{\frac{d_i}{d_o}\left(0.4 + 0.15 \ln \frac{d_o}{4t+2h}\right)} \tag{3.9}$$

$$H_{out} = -H_c \left(0.4 + 0.08 \ln \frac{d_o}{4t + 2h}\right) \exp^{\frac{d_i}{d_o}\left(1 + 0.125 \ln \frac{d_o}{4t+2h}\right)} \tag{3.10}$$

For ith turn with inner radius $r_{i,i} = d_i/2 + (w + s)(i - 1)$ and outer radius $r_{o,i} = r_{i,i} + w$, Hl(i) is denoted as the H-field strength at the left side of foil and $Hr(i)$ is the H-field strength at the right side of foil, as shown in Fig. 3.8b. The proximity effect loss of is calculated using

the standard formula for eddy-currents in a lamination [6]

$$P_{prox,i} = \frac{B_{avg,i}^2 w_s^2 t^2}{24\rho} Vol_i \tag{3.11}$$

where Vol_i is the copper volume of the ith turn, and $B_{avg,i}^2$ is the average peak flux density square of the proximal H-field

$$Vol_i = \pi(r_{o,i}^2 - r_{i,i}^2)t \tag{3.12}$$

$$B_{avg,i}^2 = \int_0^w \frac{\mu(Hl(i) + dH/wdl))^2}{w} = \mu^2 \left(Hl(i)^2 + (Hl(i) - Hr(i))^2/3 + (Hl(i) - Hr(i))Hl(i)\right) \tag{3.13}$$

The resonant coil has two copper conductors exposed in the H-field. Practically, the eddy current in one layer reduces the H-field penetrated into the other layer. Therefore, the maximum proximity effect ESR is less than two times the sum of all $P_{prox,i}$. In the modeling, the maximum proximity effect ESR is used

$$R_{prox} = \frac{2\sum_{i=1}^{n} P_{prox,i}}{I_{in}^2/2} \tag{3.14}$$

The dielectric loss is calculated based on the loss tangent D_k of the dielectric material

$$R_c = \frac{D_k}{2\pi f C_s} \tag{3.15}$$

Finally, the total equivalent series resistance (ESR) of the coil is

$$R_s = R_{skin} + R_{prox} + R_c \tag{3.16}$$

3.3 Coil Design for Target LC with Minimum ESR

The inductance, capacitance and ESR design equations bound the coil geometry with electric parameters. Thus, it is feasible to examine how to design the coil geometry to achieve a target L_s and C_s while minimizing R_s for a given application.

The geometric design is studied for given dielectric laminate with specified h, ε, D_k, t. The geometric parameters to be designed are d_i, n, and w. d_o is usually constrained by size requirement.

3.3.1 Design Method

According to ESR equation (3.16), the dielectric loss is a constant when the laminate and target C_0 have been assigned. Therefore, the geometric design seeks the minimum copper ESR for the target L_0C_0 by designing d_i, n and w. The three parameters are constrained by the two LC design equations (3.2), (3.3), producing the possibility to design multiple combitions of d_i, n and w. Each combination determines a coil loss R_s (3.16). Therefore, the coil geometry design seeks the optimal combination that has the minimum ESR.

Analyzing the inductance equation, it is found the the designed n decreases monotonically with d_i for any target L_0. To show this relation, (3.2) is rewritten using a spiral fill factor $\alpha = d_i/d_o$, where $0 < \alpha < 1$, and normalized number of turns $n_0 = n/\sqrt{\frac{L_0}{d_0}}$.

$$n_0 = \frac{2}{\sqrt{\mu\left(\alpha+1\right)\left(\ln\frac{2.46(1+\alpha)}{1-\alpha}+0.2\left(\frac{1-\alpha}{1+\alpha}\right)^2\right)}} \tag{3.17}$$

The n_0 vs. α curve is plotted in Fig. 3.9

Clearly, n_0 decreases monotonically as α increases for all L_0. Because α is proportional to d_i and n_0 is proportional to n, the physical explanation of Fig. 3.9 is that multiple geometries can be used to achieve L_0 with different d_i and n, and n decreases with increased d_i.

Thus, the maximum n_{max} is achieved when d_i approaches zero

$$n_{max} = 2\sqrt{\frac{L_0}{\mu d_o\left(\ln 2.46+0.2\right)}} \tag{3.18}$$

The minimum n_{min} is achieved when d_i reaches the maximum $d_{i,max}$, which is calculated considering that the remaining copper area is just sufficient for the target capacitance C_0

$$d_{i,max} \approx \sqrt{\left(d_o^2-\frac{4hC_0}{\varepsilon\varepsilon_0\pi}\right)} \tag{3.19}$$

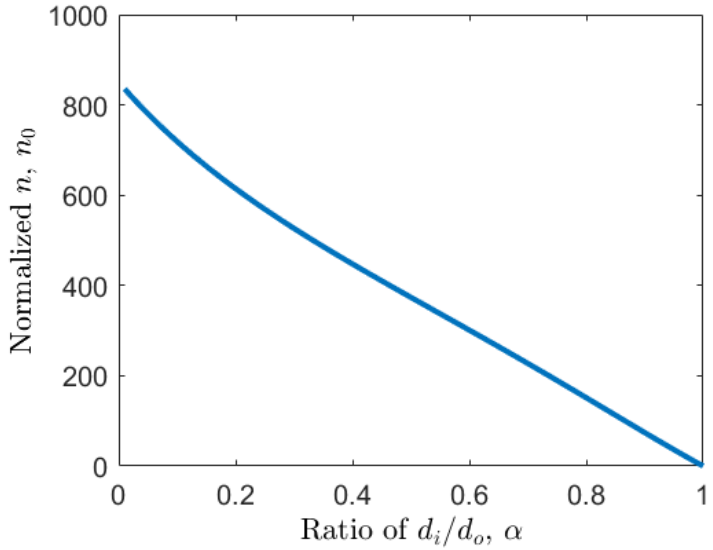


Figure 3.9: Relation of n_0 with α, with α ranging from 0 to 1.

$$n_{min} = 2\sqrt{\frac{L_0}{\mu\left(d_{i,max}+d_o\right)\left(\ln\frac{2.46}{k_{u,min}}+0.2k_{u,min}^2\right)}} \tag{3.20}$$

where $k_{u,min} = (d_o - d_{i,max})/(d_o + d_{i,max})$.

The maximum d_i design has the smallest number of turns. Intuitively, it also has the shortest total length of the copper trace. To maintain a constant C_0, the shortest trace design calls for the widest width to keep a roughly constant copper area. The shortest and widest trace ensures the smallest ESR.

However, the rough estimation of the relation that the shorter trace needs a wider width for constant C_0 is not true in some extreme situations. For example, when the copper width is much smaller than the dielectric thickness, the fringing field dominates over the main field. As shown in (3.3), narrowing the width increases fringing capacitance and may increase total capacitance, meaning the $d_{i,max}$ may not minimize $R_{s,copper}$. To maintain generality including the extreme case, an iterative approach that considers all feasible n and selects the minimum ESR design is proposed as the geometric design method for any target LC.

3.3.2 An Example of the Geometric Optimization Design

The design constraints for an example 6.78 MHz WPT coil are listed in Table 3.1. The dielectric is a commercial RO3003 Teflon-ceramic laminate that has low loss.

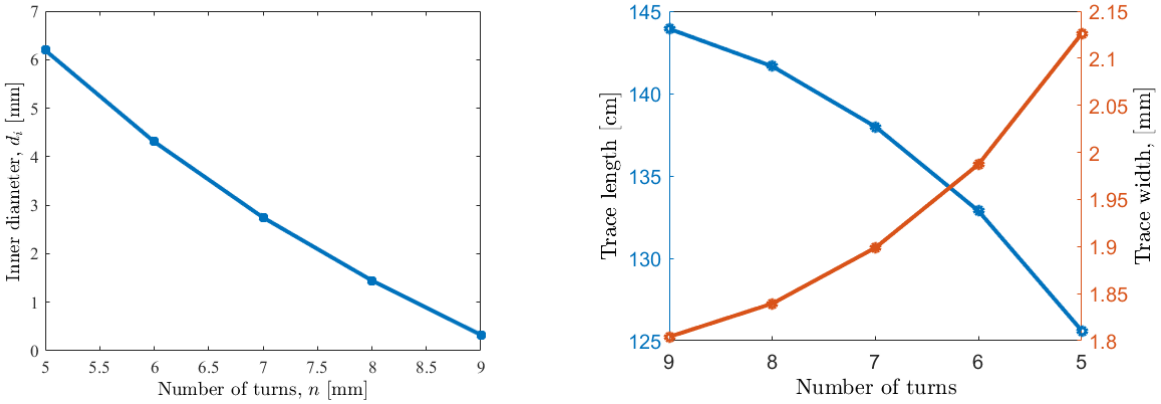
Table 3.1: Example Coil Design Constraints

Parameters	Value
L_0	3.12 µH
C_0	176.5 pF
d_0	10 cm
ε	3
h	0.508 mm
t_c	1 oz
D_k	0.0001

The calculated n_{max} and n_{min} are 9.5 and 4.4, respectively, meaning coils within the range $5 \leq n \leq 9$ can achieve the target L_0 and C_0 simultaneously. The inner diameter d_i with respect to n is shown in Fig. 3.10a. The monotonic increasing of d_i with the decreasing of n is as expected. The largest d_i design has the minimum number of turns. The length and width of a trace for different n are shown in Fig. 3.10b. The length decreases and the width increases with the increasing d_i, which also agrees with the previous analysis.

The ESR with different designs within the feasible n range is shown in Fig. 3.11. The design with the largest d_i has the minimum ESR, because this design has the shortest and widest trace.

The minimum ESR of the optimized geometry is 0.75 Ω with $n = 5$. In contrast, the ESR of the worst geometry is 1.03 Ω with $n = 9$. The ESR is reduced by 27 % compared with the worst design which still meets the target inductance and capacitance. A geometry comparison of the optimal geometry with $n = 5$ to a non-optimal design with $n = 8$ is shown in Fig. 3.12. Clearly, the trace of the optimal design is wider and shorter.



(a) **(b)**

Figure 3.10: Inner diameter (b) and length and width of trace with different n (b).

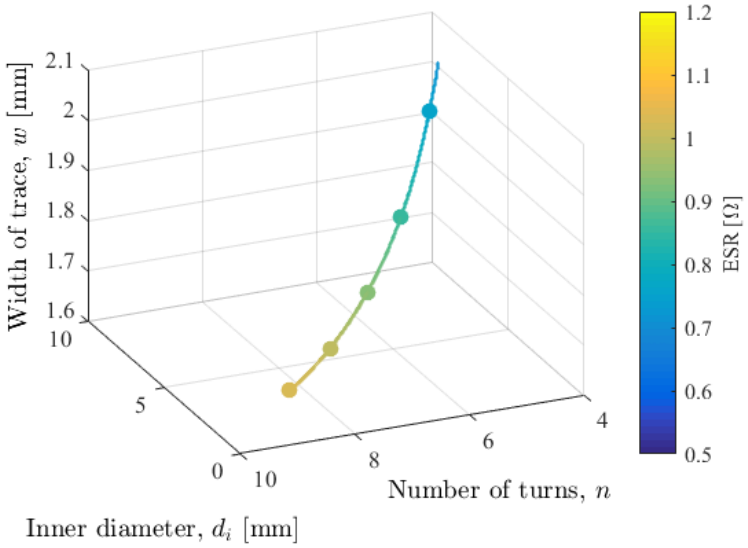
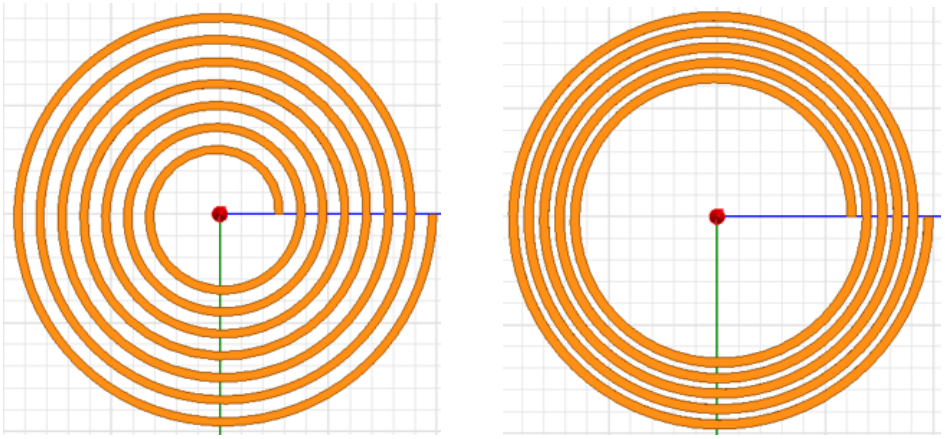


Figure 3.11: ESR with different n, w, d_i, the the dot on the curve is the iterated point with integer n.



(a) **(b)**

Figure 3.12: Images of the non-optimal coil with $n = 8$ (a) and optimal coil with $n = 5$ (b)

3.4 Prototype Testing and Verification

A set of coils with different shapes is built to verify the proposed coil and design equations. Coils use a standard four-layer FR4 PCB as both the substrate and dielectric material. Six different geometries and their parameters are listed in Table 3.2. Fig. 3.13 shows the picture of the experimental coils.

Table 3.2: Geometric parameters of the fabricated self-resonant coils with FR4

Coil	h [mm]	d_i [mm]	d_o [mm]	n	w [mm]
1	0.33	20	140	3	9.9
2	0.33	21.2	100	4	6.6
3	0.71	34.2	100	5	4.5
4	0.33	20	74	7	1.6
5	0.33	20	74	6	2.8
6	0.71	31	74	7	2.2

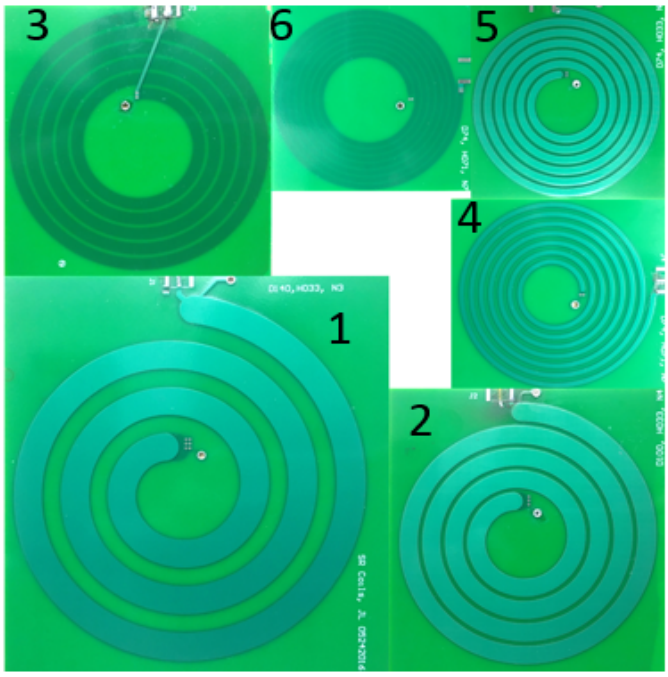


Figure 3.13: Picture showing the fabricated FR4 coils.

The coils are tested using an Agilent 4294A impedance analyzer and 42941A impedance probe kit. One example measurement curve is shown in Fig. 3.14. As shown, the coil is capacitive below 6.457 MHz and inductive above 6.457 MHz. At 6.457 MHz the impedance is minimized, and the phase is nearly zero, which means the coil exhibits a series LC resonance. All coils have the similar LC series resonance curves but differ in resonant frequency and ESR.

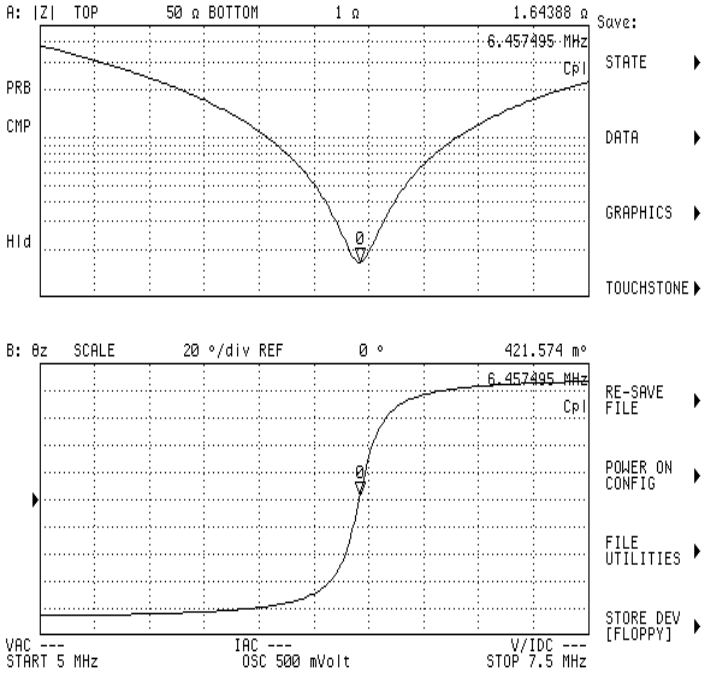


Figure 3.14: The impedance and phase curve of one fabricated coil.

The measured LCR parameters of each coil are compared with calculation values, which are shown in Fig. 3.15. The maximum errors for the LCR modeling are 4 %, 3 %, and 14 %, respectively, proving the accuracy of the design equations.

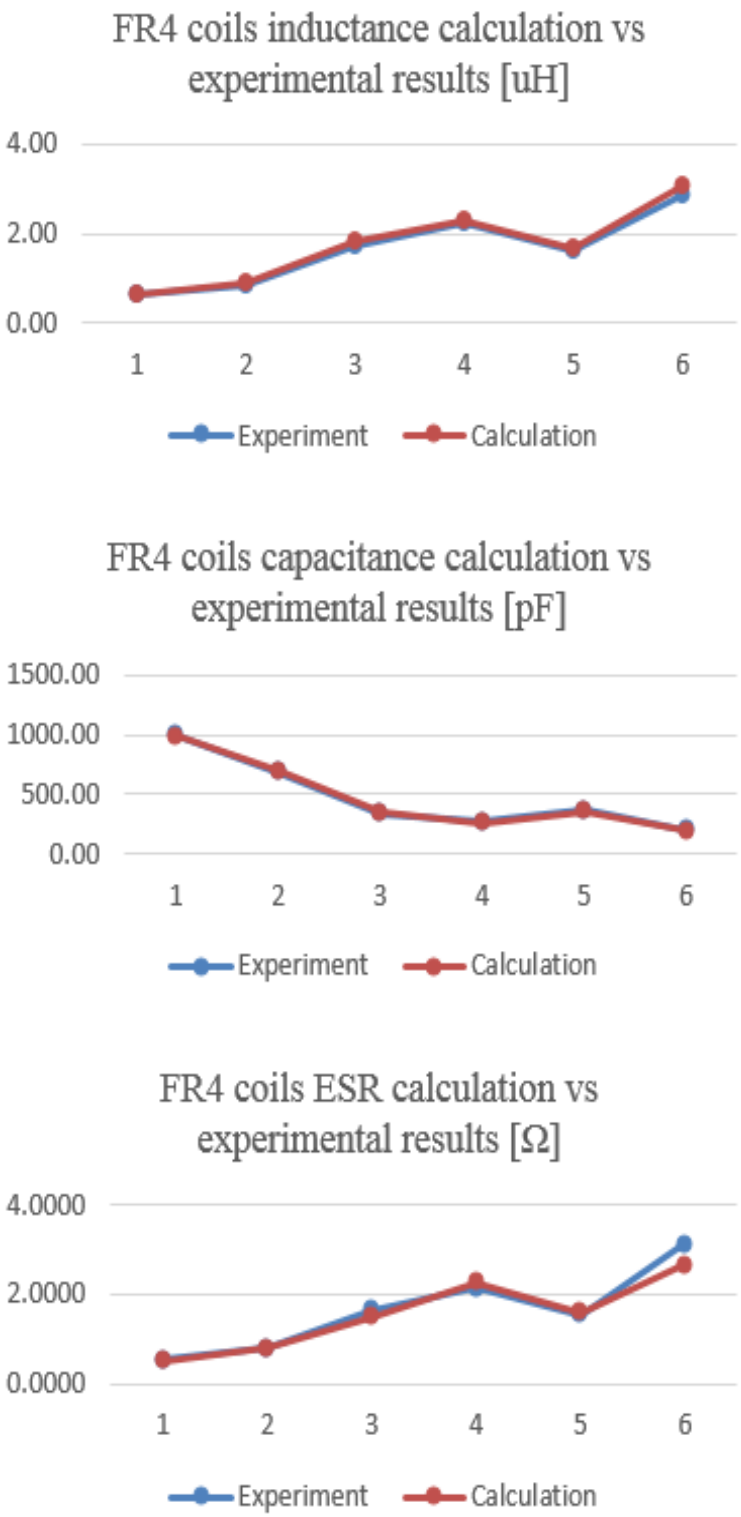


Figure 3.15: LCR parameters comparison of the tested results and the calculated results.

The quality factors of those coils are low (around 40), which is caused by the high dielectric loss of the FR4. To improve quality factor, RO3003 Teflon-ceramic laminate is used for an additional prototype. Fig. 3.16 shows the picture of the RO3003 coil.

Figure 3.16: Self-resonant coil built with RO3003 for further reduced loss.

The calculation and measurement values of the RO3003 coil are summarized in Table 3.3, showing good accuracy. Compared to the state-of-art none-self-resonant coils shown in Table 2.1, this coil has excellent Q. This coil has lower Q than the reported self-resonant coils [30, 31, 32]. But the fabricated coil has roughly twenty times higher inductance, which means much less current is needed to generate the same amount of induced voltage.

The series LC impedance is further verified by connecting the coil to a voltage source inverter (VSI) working at 6.78 MHz without impedance matching network. Fig. 3.17 shows the input voltage and current of the coil. I_{in} is the input current to the coil and output current of the inverter. V_{in} is the input voltage to the coil and output voltage of the inverter. Because of the LC filter, high order harmonics of V_{in} are filtered out and only the fundamental component is left, forming the sinusoidal shape of I_{in}. The current lags the output voltage because the working frequency is higher than the resonate frequency and the coil forms an inductive load to the inverter.

Table 3.3: RO3003 coil parameters.

Parameters	Calculated	Tested
Inductance, μH	3.00	3.13
Capacitance, pF	176.5	173.8
ESR, Ω	0.67	0.70
Q	191	189

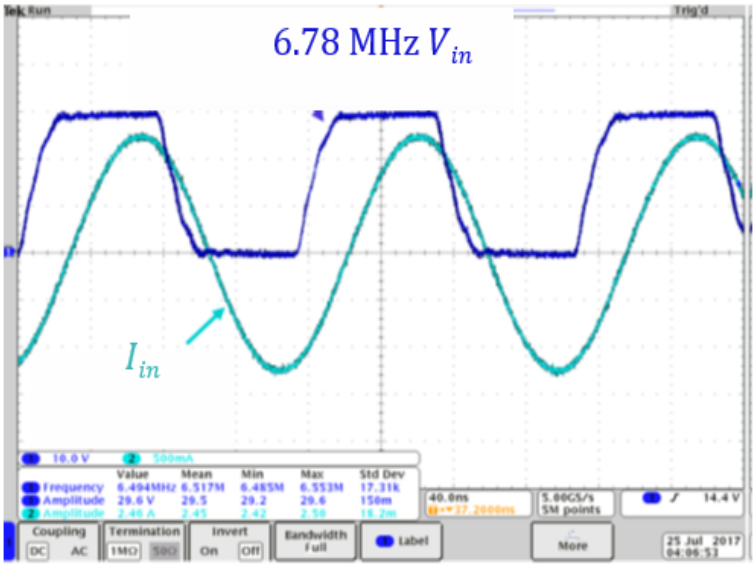


Figure 3.17: Input voltage and current of the fabricated coil when connected with a VSI working in a WPT system.

3.5 Summary

A new series self-resonate coil structure is proposed in this chapter. Detailed analysis of the coil structure and complete modeling of the coil LCR are provide based on FEA-assisted analysis and verified by prototypes. The resulting model is further developed into a geometric design method that minimizes ESR for target LC. The coil optimization design method is used in future system design considering a wide range of LC.

Multiple ESR reducing techniques are applied in the proposed coil: foil structure with reduced skin effect, multiple layers structure with better current sharing, a self-resonant structure with reduced compensation capacitor loss, and series LC impedance with no need for impedance matching when connecting to VSI. In given geometry constraints, this coil is capable to produce much larger inductance compared with other series self-resonant structures due to the multiple turns, while maintaining an extremely compact thickness. Compared with the state-of-art coils reported in the literature, a prototype coil with the proposed structure has an excellent quality factor which benefits system efficiency.

Chapter 4

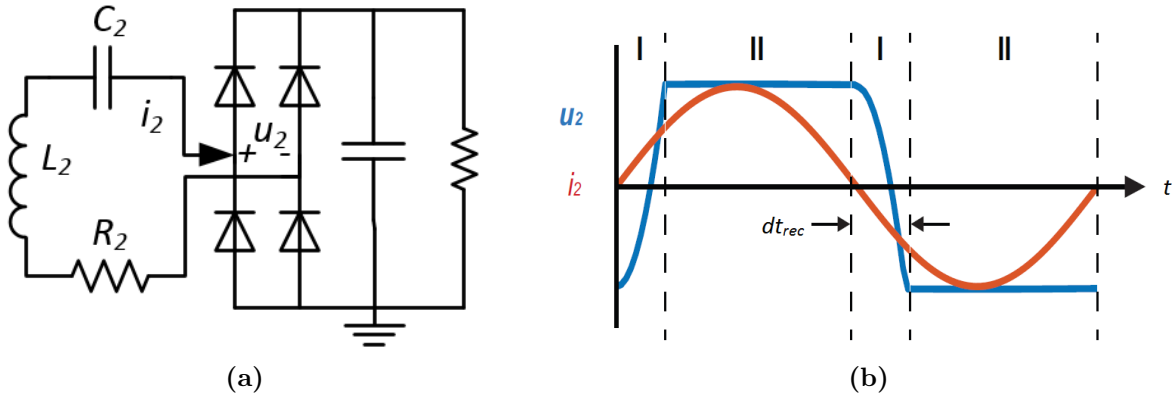
Modeling and Design of Power Electronics Converters

From literature review, traditionally diode rectifier modeling method and the ZVS inverter design are in accurate or insufficient for WPT system applications and designs where wide loading situations need to be considered. To solve these disadvantages, previous diode rectifier and ZVS inverter topology are combined with waveform and circuit analysis to develop new accurate modeling and design method for a wide load range. Detailed modeling will be shown in this chapter.

4.1 Accurate Rectifier Model

In low frequency (up to 1 MHz) WPT systems, the rectifier is usually modeled as a purely resistive load and shows good accuracy [38, 4, 24]. However, in 6.78 MHz applications, the transient of the charging and discharging of the diode output capacitance takes an appreciable part of the period, and the rectifier shows a strong capacitive input impedance. This reactance may cause a significant system efficiency drop [12] if not taken into consideration. Reference [12] uses simulation-based analysis to extract the input voltage and current for a given output at 6.78 MHz operation. However, simulations are not suitable to analyze a wide range of arbitrary designs. An accurate analytical model of the input characteristics including input voltage fundamental component V_{rect}, current I_2, and phase ϕ_{rect} for any arbitrary working point of V_o and P_o is proposed here.

The circuit schematic of a diode full-bridge rectifier is shown in Fig. 4.1a, where L_2, C_2, R_2 are the inductance, capacitance and ESR of the receiver coil, i_2 is the input current and u_2 is the input voltage. The working waveforms at a 6.78 MHz are shown in Fig. 4.1b.



(a) (b)

Figure 4.1: Diode rectifier schematic (a), and input voltage and current waveforms (b).

The red curve is i_2 . It is sinusoidal because the high-frequency components are filtered out by the connected series LC resonator working near the system switching frequency. The blue curve is u_2.

The total period is divided into two intervals. Interval I is the switching transition, where i_2 flows through the reverse-biased diode output capacitance

$$Q_{oss,leg} = \int_0^{dt_{rec}} I_2 \sin(\omega_s t) dt \tag{4.1}$$

where ω_s is the angular switching frequency, and dt_{rec} is the transient time. $Q_{oss,leg}$ equals two times the equivalent output capacitance of one device at V_o,

Interval II is the power delivery interval where i_2 flows through forward-biased diodes to the output.

$$P_o = \frac{2}{T} \int_{dt_{rec}}^{T/2} V_o I_2 \sin(\omega_s t) dt \tag{4.2}$$

with loss

$$P_{rect} = \frac{4}{T} \int_{dt_{rec}}^{T/2} V_f I_2 \sin(\omega_s t) dt \tag{4.3}$$

where V_f is the forward voltage drop on each channel. V_f is approximately determined by the junction barrier voltage v_0 and the equivalent diode resistance R_d, $V_f(t) = v_0 + R_d \cdot i_2(t)$. The total input power of the diode rectifier is $P_{total} = P_{rect} + P_o$.

The input current peak value I_2 is solved from (4.1) and (4.2)

$$I_2 = \frac{\pi P_o + V_o \omega_s Q_{oss}}{2V_o} \tag{4.4}$$

The analytical expression of the input voltage of the rectifier $u_{2(1)}(t)$ is

$$u_{2(1)}(t) = \begin{cases} -V_o + 2\int_0^t I_2 \sin(\omega_s t)/C_{oss,leg} dt, 0 < t < dt_{rect} \\ V_o + 2\left(v_0 + R_d \cdot I_2 \sin(\omega_s t)\right), dt < t < T/2 \\ V_o + 2\int_0^{t-T/2} I_2 \sin(\omega_s t)/C_{oss,leg} dt, T/2 < t < T/2 + dt_{rect} \\ -V_o - 2\left(v_0 + R_d \cdot I_2 \sin(\omega_s t)\right), T/2 + dt_{rect} < t < T \end{cases} \tag{4.5}$$

The fundamental component V_{rect} of $u_{2(1)}(t)$ is extracted using Fourier analysis

$$V_{rect} = \sqrt{\left(\frac{2}{T}\sqrt{\left(\int_0^T u_{2(1)}(t)\sin(\omega_s t)dt\right)^2 + \left(\int_0^T u_{2(1)}(t)\cos(\omega_s t)dt\right)^2}\right)} \tag{4.6}$$

The input phase ϕ_{rect} is calculated using the definition $P_{total} = V_{rect}\ I_2\ \cos\phi_{rect}$

$$\phi_{rect} = \arccos\left(\frac{2(P_o + P_{rect})}{I_2 V_{rect}}\right) \tag{4.7}$$

Thus, the equivalent impedance of the rectifier Z_{rec} is

$$Z_{rec} = \frac{2\,(P_o + P_{rect})}{I_2^2} \cdot (1 - j\tan(\phi_{rect})) \tag{4.8}$$

4.2 ZVS Inverter Design Using Auxiliary Tank

4.2.1 Structure

The function of the inverter is providing power to a target load $P_{load} = V_1\ I_1\ \sin\phi_1$. V_1 is the fundamental component of the switch node voltage, I_1 is the peak of the output current, and ϕ_1 is the phase between the output voltage and current. At 6.78 MHz, it is critical to ensure ZVS operation of inverter devices for safe operation. However, in the design stage, it is not clear which load will be connected to the inverter. The load current may be inductive and large enough to ensure the ZVS operation. It may be small or even capacitive, and the inverter cannot achieve ZVS with this load current.

To ensure ZVS, an auxiliary inductor tank is added to each phase leg for additional inductive current and ensured ZVS when the inverter cannot achieve ZVS with i_1. The tank is added to the switch node and the middle point of two capacitors that are in parallel with the DC bus, shown in Fig. 4.2.

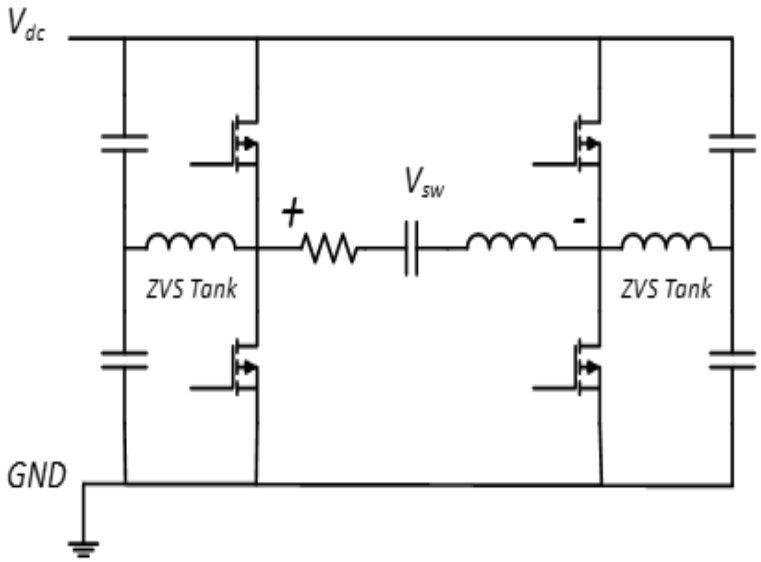


Figure 4.2: ZVS inverter with auxiliary tank.

4.2.2 Modeling

The focus of this section is finding the relation of the inverter design parameters with the target output parameters. The inverter design parameters are DC bus voltage V_{dc}, tank inductance L_{zvs} and dead time dt. The target output parameters are V_1, I_1 and ϕ_1.

The typical waveforms when i_1 is capacitive are shown in Fig. 4.3. The output current i_1 is shown by the blue curve. i_1 is sinusoidal due to the series LC filter which works around working frequency. The ZVS tank current i_{zvs} is shown by the red curve. The switch node voltage V_{sw} is shown by the grey curve. V_{gH} and V_{gL} are gate signals of the high side and low side devices, respectively.

v_{sw} is approximately trapezoidal:

$$v_{sw}(t) = \begin{cases} V_{dc}\left(-1 + 2/dt \cdot t\right), 0 < t < dt \\ V_{dc}, dt < t < T/2 \\ V_{dc}\left(1 - 2/dt \cdot (t - T/2)\right), T/2 < t < T/2 + dt_{rect} \\ V_{dc}, T/2 + dt_{rect} < t < T \end{cases} \tag{4.9}$$

where $t = 0$ is the starting point of ZVS transient.

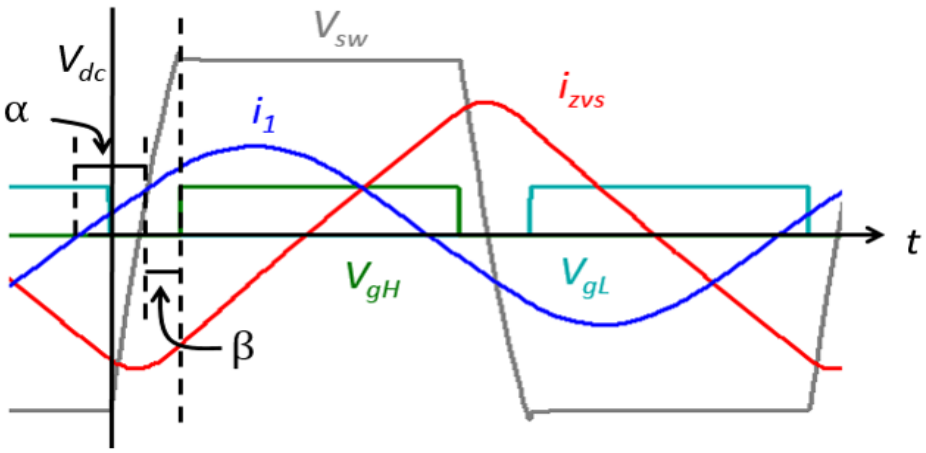


Figure 4.3: ZVS inverter output voltage and current.

To generate the target V_1, the inverter can be designed with multiple combination of V_{dc} and dt. Using Fourier analysis, the V_{dc} that provides V_1 is

$$V_{dc} = V_1 / \left(\frac{2}{T} \sqrt{\left(\int_0^T v_{sw}(t) \sin(\omega_s t) dt \right)^2 + \left(\int_0^T v_{sw}(t) \cos(\omega_s t) dt \right)^2} \right) \tag{4.10}$$

which gives the relation of V_{dc} and dt for target V_1.

During transient interval, both i_{zvs} and i_1 are involved in charging or discharging the switch node output capacitance Q_{oss}. The ZVS tank is designed to ensure the inverter has full ZVS without diode conduction. Thus,

$$Q_{oss} = \int_0^{dt} \left(i_{zvs}(t) + i_1(t) \right) dt \tag{4.11}$$

i_{zvs} during dead-time is calculated by [40]

$$\begin{aligned} i_{zvs}(t) = {} & I_0 \cos\left(\omega_z \left(t + \frac{\beta - \alpha}{\omega_s} \right) \right) + C_{oss} V_{dc} \omega_z \sin\left(\omega_z \left(t + \frac{\beta - \alpha}{\omega_s} \right) \right) + \\ & \frac{I_1}{\left(\frac{\omega_s^2}{\omega_z^2} - 1 \right)} \left[\cos\left(\omega_z \left(t + \frac{\beta - \alpha}{\omega_s} \right) \right) \sin(\alpha - \beta) + \right. \\ & \left. \frac{\omega_s}{\omega_z} \sin\left(\omega_z \left(t + \frac{\beta - \alpha}{\omega_s} \right) \right) \cos(\alpha - \beta) + \sin(\omega_s t) \right] \end{aligned} \tag{4.12}$$

where $\omega_z = 1/\sqrt{L_{zvs}C_{oss}}$, $I_0 = i_{zvs}(0)$, α and β are auxiliary parameters introduced to help model. Shown in Fig. 4.3, α is the phase difference between the zero phase of the resonant current and the center of the transient section. α is positive for leading the middle of the transient, and negative for lagging the center of the transient. α is the output phase angle of the inverter given by ϕ_1, assuming that the voltage during transient is linear. β is the phase representing half of the total transient time $\beta = dt/T\dot{\pi}$, where T is the time of a period.

After transient interval, $V_{dc}/2$ is applied to the tank, causing i_{zvs} to rise linearly from $t = dt$ to $t = T/2$.

$$i_{zvs}(dt) + i_{zvs}(T/2) = \frac{V_{dc}}{2L_{zvs}}(\frac{T}{2} - dt) \tag{4.13}$$

Due to symmetric operation, the ZVS current at $t = 0$ equals to $t = T/2$

$$i_{zvs}(T/2) = i_{zvsdt}(0) = I_0 \tag{4.14}$$

I_0 is solved by the above two equations (4.13) and (4.14)

$$\begin{aligned} I_0 = \frac{1}{1+\cos(\omega_z dt)}\Bigg[\frac{V_{dc}}{2L_{zvs}}(\frac{T}{2} - dt) - \frac{V_{dc}}{2}\sqrt{\frac{C_{oss}}{L_{zvs}}}\sin(\omega_z dt) + \\ \frac{I_1}{L_{zvs}C_{oss}\omega^2 - 1}\Bigg(\sin(\omega dt + \alpha - \beta) - \cos(\omega_z dt)\sin(\alpha - \beta) - \\ \frac{\omega}{\omega_z}\sin(\omega_z dt)\cos(\alpha - \beta)\Bigg)\Bigg] \end{aligned} \tag{4.15}$$

Further, L_{zvs} is solved by plugging I_0 into i_{zvs} and solve the transient equation (4.12). Therefore, both L_{zvs} and V_{dc} are solved based on a given dt for the target V_1, I_1 and ϕ_1. Changing dt results multiple inverter designs that provide the same output.

4.2.3 Inverter Design Method for Minimum Loss

Even though multiple inverter designs can provide the same target output, only the design with minimum loss is preferred. To find the best design, inverter loss modeling is necessary.

ZVS Inverter Loss Modeling

The inverter total loss consists of two parts: the loss on the devices and the loss on the auxiliary tanks. The loss on the device consists only of the conduction loss because the inverter is designed to have ZVS and no diode conduction. The conduction loss on the full bridge is

$$P_{ds} = 2I_{1,rms}^2 R_{ds} \tag{4.16}$$

where $I_{1,rms}$ is the RMS value of i_1, R_{ds} is the on-resistance of one device.

The loss on the auxiliary tank consists of copper loss $P_{zvs,copper}$ and core loss P_{core}. The inductor is designed using an iron powder toroid core with 1 cm diameter. Iron powder is commonly used in RF applications and has low core loss.

To achieve the target L_{zvs}, the number of turns N_z is calculated based on the empirical equation from the datasheet [54]

$$N_z = \sqrt{\frac{L_{zvs} \times 10^9}{k_z}} \tag{4.17}$$

where k_z is an empirical coefficient from the datasheet.

The wire length l_{ac} is calculated as

$$l_e = MLT \cdot N_z \tag{4.18}$$

where MLT is the mean length per turn.

The wire is implemented using AWG 28 with an outer radius of $r_{z,o}$. Considering the skin effect with skin depth δ, the effective conduction area A_{ac} is

$$A_{ac} = \pi[r_{zo}^2 - (r_{zo} - \delta)^2] \tag{4.19}$$

Copper ESR calculation is based on the the wire length l_{ac} and effective conduction area A_{ac}

$$R_{zvs,copper} = \frac{\rho_{copper} l_{ac}}{A_{ac}} \tag{4.20}$$

$$R_{zvs,copper} = \frac{mlt\rho_{copper}\sqrt{\frac{L_{zvs}\times 10^9}{k_z}}}{\left[r_{z,o}^2 - (r_{z,o}-\delta)^2\right]} \tag{4.21}$$

As in Fig. 4.3, i_{zvs} is approximated to be a triangular wave when calculating the copper loss. When V_{dc} is applied, the voltage across the ZVS tank is $V_{dc}/2$. The peak value I_{zvs} is

$$I_{zvs} = \frac{V_{dc}T}{8L_{zvs}} \tag{4.22}$$

The copper loss is calculated combing the copper ESR (4.21) and the current (4.23)

$$P_{zvs,copper} = \frac{1}{3}\cdot\left(\frac{V_{dc}}{8L_{zvs}f}\right)^2 \frac{\sqrt{2}\rho_{copper}H_t\sqrt{\frac{L_{zvs}\times 10^9}{k_z}}}{\left[r_{z,o}^2 - (r_{z,o}-\delta)^2\right]} \tag{4.23}$$

The core loss is calculated using an empirical equation from the datasheet [54]

$$P_{core} = \left(\frac{f}{\frac{4\times 10^9}{B^3} + \frac{3\times 10^8}{B^{2.3}} + \frac{2.7\times 10^6}{B^{1.65}}} + 3\times 10^{-15} f^2 B^2\right) V_{ol} \tag{4.24}$$

where $B = V_{1,rms}\cdot 10^8/4.44AN_z f$, V_{ol} is the core volume, f is the switching frequency, and A is the cross-section area of the core.

ZVS Inverter Design Method for Minimum Loss

The modeling section 4.2.2 illustrates that multiple inverter designs with different dt can achieve the same target output, and V_{dc} and L_{zvs} are calculated based on dt. The inverter loss modeling section presents the method to calculate the loss of each design. Thus, it is feasible to examine which dt gives the minimum loss.

In 6.78 MHz applications, when dt is iterated from a small value, for example, 5 ns, with a step of 10 % increment from last dt, it is found the change of V_{dc} compared with last V_{dc} is very small (less than 1.5 %), as shown in Fig 4.4.

Therefore, V_{dc} and Q_{oss} is approximated to be constant for each step of dt. To discharge a constant Q_{oss}, L_{zvs} must increase for every step of dt so that the average i_{zvs} during transient reduces. According to (4.23) and (4.24), the increased L_{zvs} leads to the drop of both core loss and copper. Consequently, the inverter loss decreases with dt until to a maximum dt

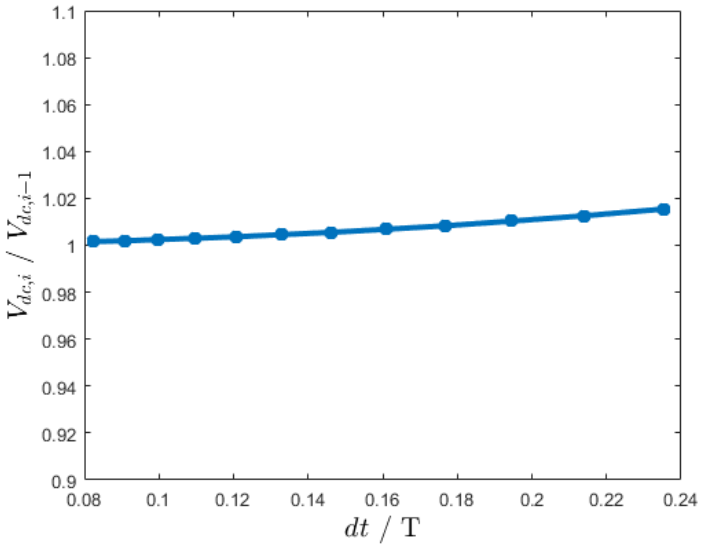


Figure 4.4: V_{dc} change with each step of dt. dt has a step of 10 % compared with the previous dt.

where further increasing dt will cause an insufficient amount of ZVS current which leads to inverter partial hard switching. Or in situations where the load current is sufficient for ZVS, the maximum dt is when the load current just have enough time to recycle the Q_{oss} energy and no diode conduction. Therefore, the optimal inverter can be designed by iteration of dt from a small value and find the maximum dt, then designing the V_{dc} and L_{zvs} accordingly.

An Example of the Inverter Design

An example inverter design specification is listed in Table 4.1. The load current is capacitive and therefore auxiliary tank is necessary. The resulting inverter loss and design parameters, and the total current at the end of the transient interval with an iteration of dt are shown in Fig. 4.5. Shown in Fig. 4.5a, L_{zvs} increases with dt reducing the average ZVS tank current. Accordingly, the inverter loss reduces with the increased L_{zvs}, shown in Fig. 4.5b. When dt increases to around 27 ns, the tank current reaches a minimum point that the total output current considering i_1 is zeros. Further increasing dt (or equivalently, increasing L_{zvs}) will lead to insufficient tank current, causing partial hard switching. This time point is dt_{max}. The designed V_{dc} and the associated Q_{oss} are shown in Fig. 4.5d, which are almost constant.

Table 4.1: Example Inverter Design Specifications

Parameters	Value
V_1	50 V
I_1	0.5 A
ϕ_1 in °	13 ° capacitive
f_s	6.78 MHz
GaN device	EPC2045

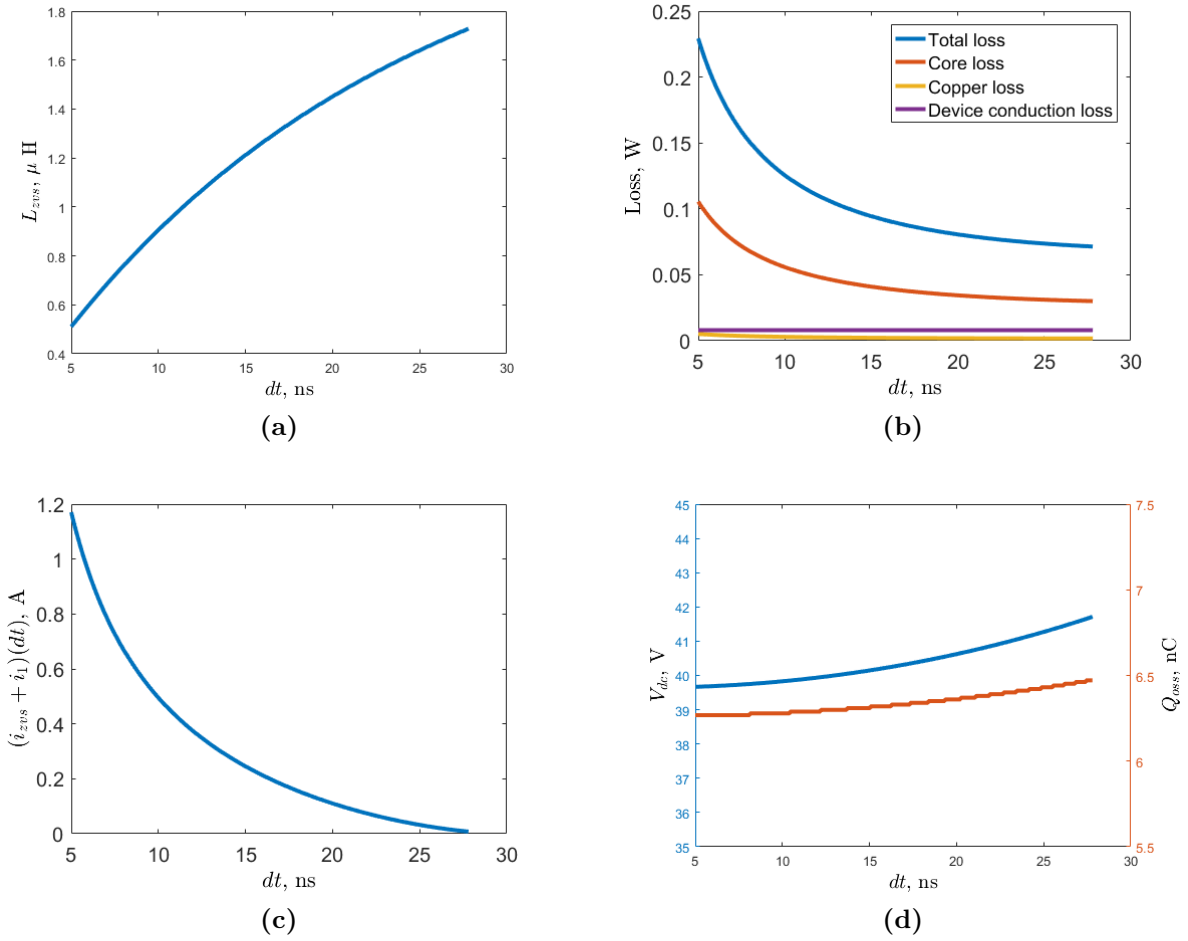


Figure 4.5: Inverter tank inductance (a), loss (b), total output current (c), and bus voltage and the output charge (d).

The calculated results show the power loss for the optimized inverter is 0.07 W at V_{dc} = 41.6 V, L_{zvs} = 1.70 μH and dt = 27 ns. In contrast, the power loss for dt = 5 ns is 0.23 W, which is 328 % of the optimal design.

LTSpice Simulation of the Example of the Inverter Design

An LTSpice simulation is provided to support the modeling method. The simulation uses the same device and inverter parameter as in the example case. As shown in Fig. 4.6, i_1 is represented by a 0.5 A constant sinusoidal source with a 5 ns (equivalently 13 °) capacitive phase shift. The current source is connected to a 100 Ω resistor forming the required V_1 = 50 V . The simulated waveforms are shown in Fig. 4.7.

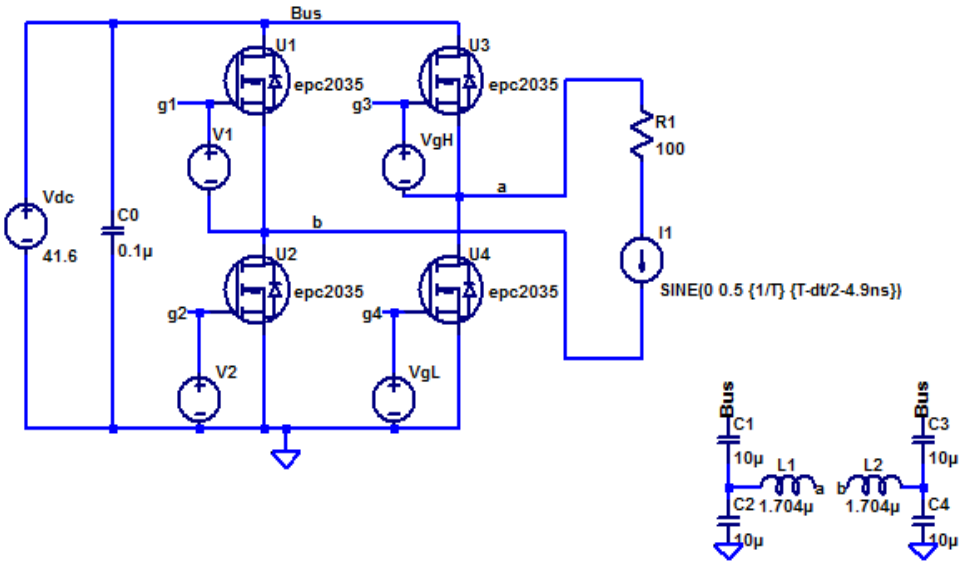


Figure 4.6: Schematic in LTSpice simulation for verification of the optimal ZVS design.

v_{sw} is the grey curve. i_1 is the red curve and i_{zvs} is the blue curve. V_{gH} and V_{gL} are the dark and light blue curves. Devices are turned on after the C_{oss} energy has been almost charged or discharged. ZVS is achieved with a slight partial hard switching (around 2 V). This discrepancy may be caused by the inaccurate approximation of V_{sw} to a trapezoidal waveform.

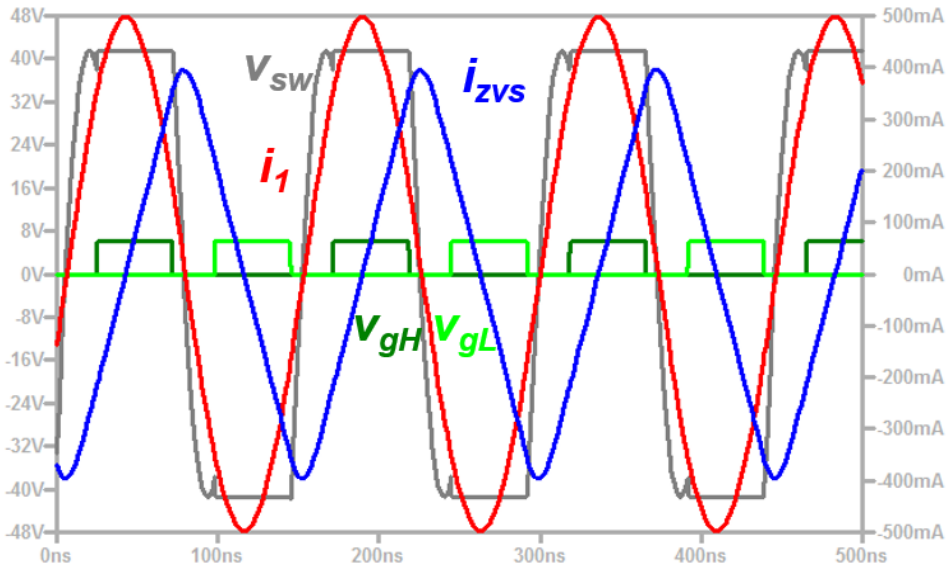


Figure 4.7: Simulated waveforms of the designed optimal ZVS inverter in LTSpice.

4.3 Summary

In transient from previous kHz WPT to the target 6.78 MHz WPT, the obviously magnified switching frequency causes resonant transition times to constitute a significant portion of the switching period. Because the resonant transition intervals are expected to be significant in the proposed application, traditionally diode rectifier resistive modeling in relatively low frequency and higher power applications is no longer true. Accurate working waveforms of the rectifier is described using analytical expressions, which further lead to an accurate diode rectifier model describing the input characteristics of the rectifier with an arbitrary load. The resulting analytical model covers wide loading situations thus suitable in WPT system design.

In 6.78 MHz WPT systems, the inverter is desired to provide target output power with ZVS operation for safe operation. Because inverter load may change drastically due to load/distance variations, the traditional ZVS class-D inverter topology with auxiliary tank is accurately modeled to cover arbitrary output load. Accurate working waveforms of the inverter is described using analytical expressions, which further lead to an accurate ZVS inverter model describing the inverter V_{dc}, L_{zvs}, and dt with an arbitrary load. Based on the design model, an inverter optimization that achieves minimum inverter loss for a arbitrary

load is detailed. The resulting inverter solution is a single optimal design for any required output, which is used in future system design considering wide load range.

Chapter 5

System Design Method Considering the Interdependence of Converters, Coils, and Circuit Operating

From literature review, traditional system-level design method is based on assumptions that are not generally true due to the neglect of ZVS requirement and diode rectifier reactance. Based on the resulting coil and converter models, this chapter presents an entire WPT system model and design methodology which highlights the co-design of individuals parts and the design sequence.

5.1 WPT System Model and the Interdependence of Losses of Each Part

As shown in Fig. 5.1, the analyzed WPT system includes a full bridge inverter, a self-resonant coil on the transmitter side, another self-resonant coil on the receiver side, and a rectifier on the receiver side. The two coils are coupled with a coupling factor k. The system is desired to transfer a constant output power of P_o.

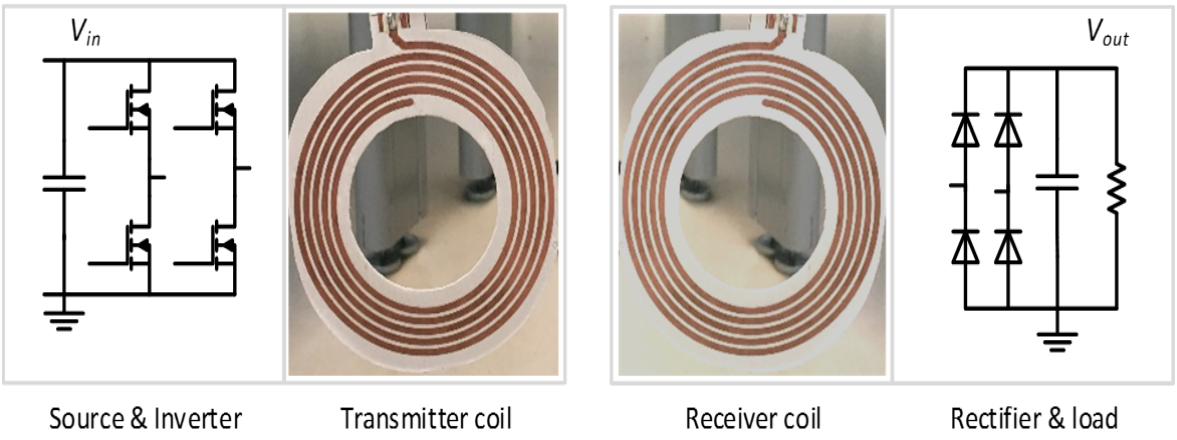


Figure 5.1: Blocked diagram of a WPT system employing self-resonant coils.

The equivalent circuit describing the above system is shown in Fig. 5.2. Z_{rec} is the equivalent impedance of the rectifier and load. (L_1, C_1, R_1) and (L_2, C_2, R_2) are the inductance, capacitance, and ESR of the transmitter coil and receiver coil, respectively. V_1 is the fundamental component of the inverter output voltage. i_1 is the output current of the inverter and i_2 is the input current of the rectifier. I_1 and I_2 are the amplitude of i_1 and i_2. ϕ_1 is the phase between V_1 and i_1. All the parameters have the same definition when they are first used in Chapter 3 and Chapter 4.

The previous chapters have addressed the individual stages modeling and design method, bridging the target electric parameters (shown in the equivalent circuit) with their design parameters. Chapter 3 presents a coil modeling which bridges coil geometry parameters with LCR. The geometry optimization design seeks to optimize coil geometry for each (LC), eliminating all non-optimal designs. After optimization, each (LC) is associated with one minimum ESR. The coil loss is determined by the conducting current I and ESR. Because

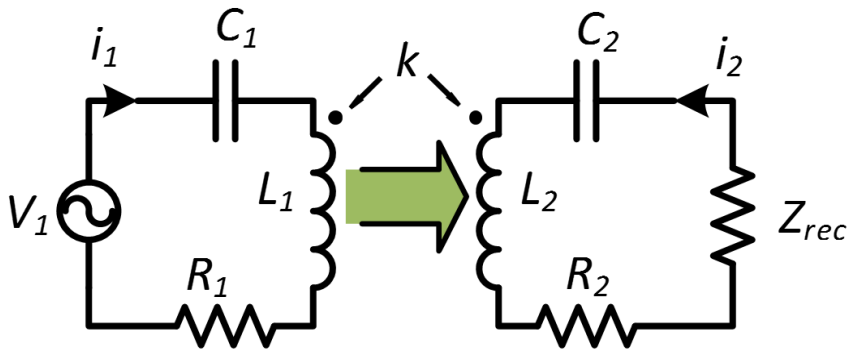


Figure 5.2: Equivalent circuit of the WPT system.

each (LC) is uniquely associated with one ESR, the coil loss is equivalently determined by (I, L, C) after optimization design.

Section 4.1 discussed the rectifier modeling which bridges the input impedance and current with arbitrary output. For constant P_o applications, the inverter loss P_{rect} is determined by V_o.

Section 4.2 analyzes ZVS inverter modeling which bridges the inverter design (V_{dc}, L_{zvs}, dt) with required output (V_1, I_1, ϕ_1). The inverter optimization design eliminates all non-optimal inverter design, leaving just one inverter design with minimum loss for each required output. The inverter power loss is determined by $(V_1, I_1, \phi_1, V_{dc}, L_{zvs}, dt)$. Because each (V_1, I_1, ϕ_1) is associated wiht one (V_{dc}, L_{zvs}, dt), the inverter loss is equivalently determined by (V_1, I_1, ϕ_1) after the optimization design.

The parameters concerning the losses on each individual part are summarized in Fig. 5.3.

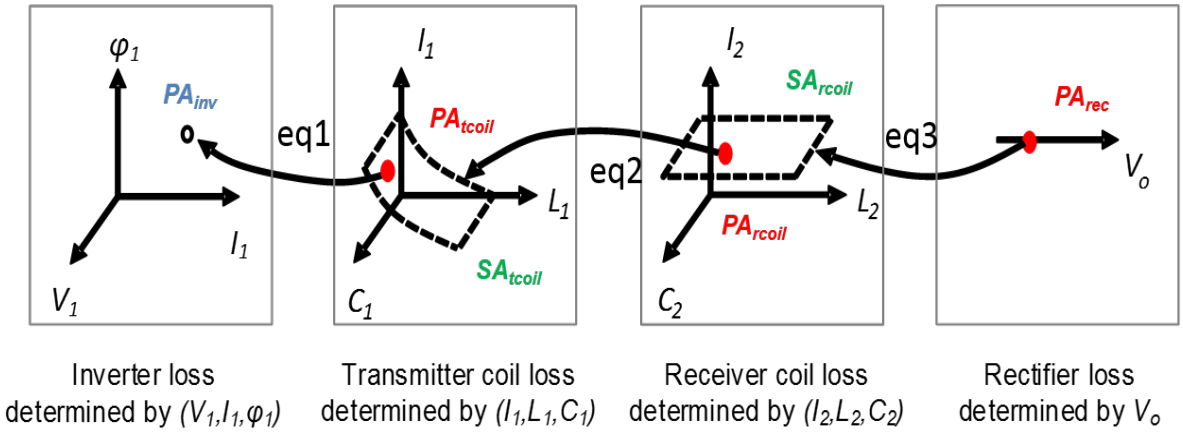


Figure 5.3: Design parameters concerning the loss of each part, and their inter-dependence.

As shown in Fig. 5.3, the losses on each part are strongly coupled. One arbitrary rectifier design (PA_{rec}) determines one unique I_2, linking to a plane (SA_{rcoil}) in the receiver coil loss design region. The linking equation eq3 has been discussed in (4.4) and is re-written

$$I_2 = \frac{\pi P_o + V_o \omega_s Q_{oss}}{2V_o} \tag{5.1}$$

Further, each arbitrary receiver coil loss design ($PA_{rcoil}(I_2, L_2, C_2)$), with the information from the rectifier V_o, constrains the transmitter coil loss design to one surface (SA_{tcoil}). The linking equation eq2 is

$$I_1 = \frac{j(\omega_s L_2 - \frac{1}{\omega_s C_2}) + R_2 + Z_{rec}}{\omega_s k \sqrt{(L_1 L_2)}} \tag{5.2}$$

Finally, each arbitrary transmitter coil design ($PA_{tcoil}(I_1, L_1, C_1)$), with the information from receiver design (V_o, L_2, C_2), defines one unique (V_1, I_1, ϕ_1), linking to one point in the inverter loss design. This link is described by eq1

$$V_1 = I_1 \cdot \left(\frac{\omega_s^2 k^2 L_1 L_2}{j(\omega_s L_2 - \frac{1}{\omega_s C_2}) + R_2 + Z_{rec}} + j(\omega_s L_1 - \frac{1}{\omega_s C_1}) + R_1 \right) \tag{5.3}$$

$$\phi_1 = Phase\left(\frac{V_1}{I_1}\right) \tag{5.4}$$

The coupled losses prevents separatly desining the lowest loss for single part. The lowest loss rectifier, which requires a high V_o, links with high transmitter coil loss. The loss inter-dependence calls for a comprehensive design method that considers co-design all parts together.

5.2 The Overall Design Method for Minimum Loss

This section proposes the overall design method aiming at minimizing total DC-to-DC power loss while transferring a constant amount of power P_o. Initially, design variables are: V_o of the rectifier, geometrical parameters of the coils (turn width w, number of turns n, inner diameter d_i, outer diameter d_o, thickness of the dielectric h), and V_{dc}, L_{zvs} and dt of the

inverter. The range of input and output voltages, and the size of the coils, are constrained within acceptable ranges for a consumer electronics application.

Because of the complicated design parameters, direct iteration of all possible designs, including physical geometry implementation of the coils, may be infeasible. To reduce computational burden, the first step of the proposed design method seeks to individually optimize each stage to the extent possible, leaving a reduced design space in which all independently suboptimal designs have been eliminated.

For the coils with given dielectric material, because LCR are the electric parameters that matter when analyzing the coils in the circuit, geometrical parameters w, n, d_i, h and d_o are used to first calculate the range of LC. Then, the minimum ESR for each feasible LC is designed using the coil geometrical optimization design method in Chapter 3 [35]. After optimization, all independently suboptimal designs have been eliminated and the coil design variables are converted from (w, n, d_i, d_o, h) to just (L, C), with R_{opt} is determined by (L, C). (L, C) and the associated R_{opt} are stored in a coil design look-up-table.

For the ZVS inverter, by designing the inverter to have ZVS operation and no diode conduction, and designing an optimal dt so the inverter achieves minimum loss while still providing the required output, all suboptimal inverter designs have been eliminated and the inverter design parameter reduces from (V_{dc}, L_{zvs}, dt) to a single optimal inverter design for any required output (V_1, I_1, ϕ_1). The inverter loss $P_{inv}(V_{dc}, L_{zvs}, dt, V_1, I_1, \phi_1)$ is reduced to be $P_{inv,opt}(V_1, I_1, \phi_1)$ and stored in an inverter design look-up-table. The inverter design variables are significantly reduced.

For the rectifier, to provide specified output power P_o, the rectifier loss and input characteristics are calculated with V_o using the accurate rectifier model in Chapter 4 and stored to a rectifier design look-up-table.

The elimination of suboptimal designs and the significant reduction of design variables makes iteration feasible. The design variables finally transfer to the parameters shown in Fig. 5.3.

The second step of the overall design method is the iteration of the design variables shown in Fig. 5.3. For fixed P_o applications, V_o is chosen as the first iteration parameter because V_o determines P_{rect} and I_2, linking one dot of the rectifier design plot to a plane of the receiver

coil design. Each point of this plane has a loss $P_{rcoil}(L_2, C_2, I_2)$ and confines the relation of I_1 and L_1, linking to a surface of the transmitter design. Any point of the surface has a loss of $P_{tcoil}(L_1, C_1, I_1)$ and requires a specified output (V_1, I_1,ϕ_1) from the inverter.

The total loss P_{sys} is the sum of the loss on each part $P_{rect} + P_{rcoil} + P_{tcoil} + P_{inv,opt}$. After iteration, the optimal system with complete design of the four parts is found by selection of the minimum P_{sys}.

5.3 An Example Overall Design

The example application is transferring 10 W power across a pair of coils with 0.1 coupling coefficient. The inverter switches are EPC2112, 200V GaN FETs. The rectifier diodes are CDBA240LL-HF, 40V Schottky diodes. The laminates for the two self-resonant coils are RO3003, a Teflon-ceramic laminate which has a low dielectric loss (1/20 of FR4 loss). Two commercial laminates are considered: 0.25 mm and 0.5 mm. The outer diameter is 10 cm for the transmitter coil and 7 cm for the receiver.

5.3.1 Individual Optimization

The first step is seeking individual optimization to reduce system design variables. Coil design parameters are converted from all geometrical parameters to just LC. Inverter design parameters are reduced from multiple V_{dc}, L_{zvs} and dt to one single optimal design.

Coil Geometry Optimization Result

The coil geometry is designed to achieve minimum ESR for a wide range of LC. Design results for the transmitter coil using the 0.5 mm thickness are shown in Fig. 5.4.

Fig. 5.4a shows the ESR vs. LC. The trend can be explained by the optimized geometry shown in Fig. 5.4c and Fig. 5.4b. When the capacitance is fixed and inductance increases, the optimized ESR generally increases as in Fig. 5.5a. This is because larger inductance calls for longer length as in Fig. 5.4c, resulting in a thinner width to keep a roughly constant copper area for the fixed capacitance, as in Fig. 5.4d. The longer and thinner trace leads to an increased ESR. When the inductance is fixed and capacitance increases, the optimized

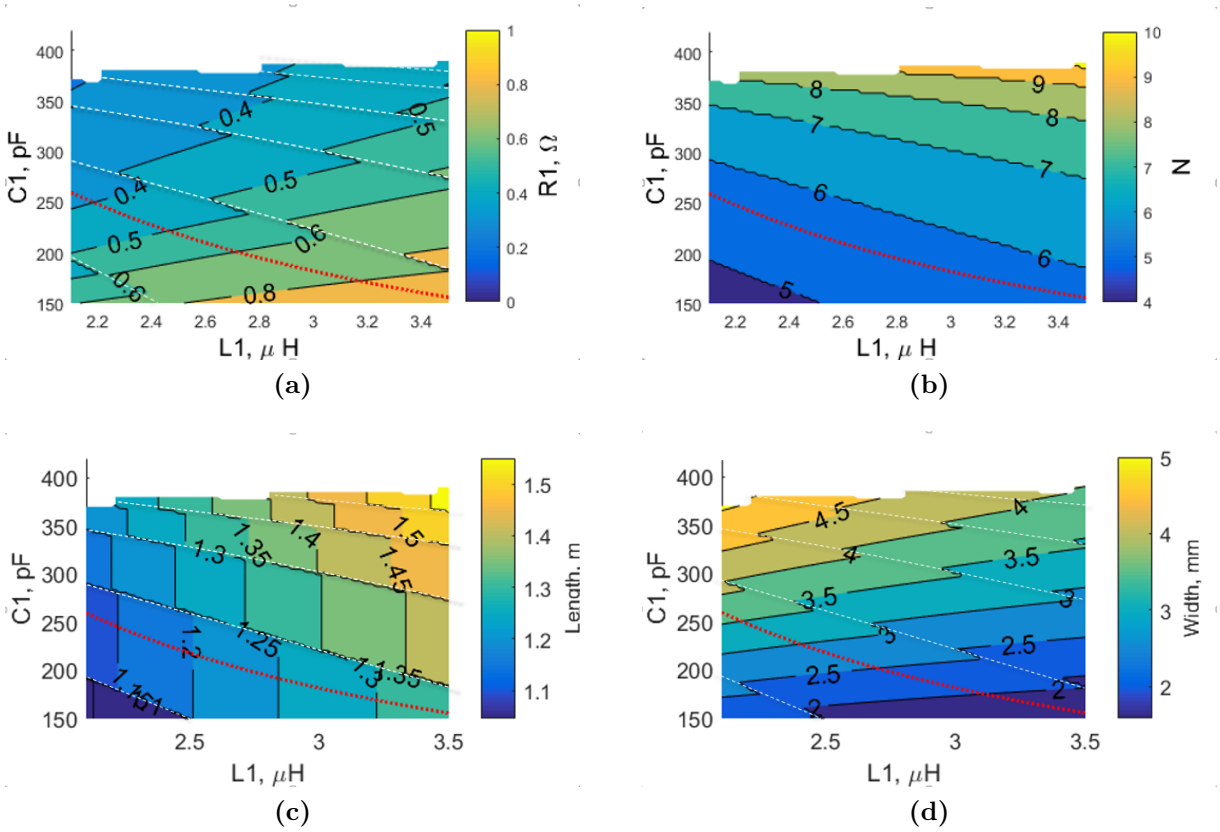


Figure 5.4: Coil design after optimization for $h = 0.5$ mm transmitter coil, ESR 5.4a, number of turns 5.4b, trace length 5.4b, and trace width 5.4d. The red curve is LC resonance at 6.78 MHz. The white curve is the optimized n contour from 5.4b.

ESR generally decreases because the fixed inductance almost determines the length of trace, as shown in 5.4c, and larger capacitance calls for wider width 5.4d to maintain the copper area. The wider trace leads to a reduced ESR. Additionally, the dielectric loss also reduces with increasing capacitance. The glitches in Fig. 5.4 are caused by the changing of integer number of turns, as shown in Fig. 5.4b.

The ESR vs. LC for $h = 0.25$ mm has the same shape and explanation as $h = 0.5$ mm. The difference is that a 0.25 mm dielectric has a wider capacitance range because of the thinner dielectric (3.3). Also, when designing the same LC, 0.25 mm dielectric needs less width and therefore has higher ESR than 0.5 mm dielectric. The final transmitter coil design region is the combination of the two thickness, picking the minimum ESR from Fig. 5.4a and Fig. 5.5a and forming Fig. 5.5b.

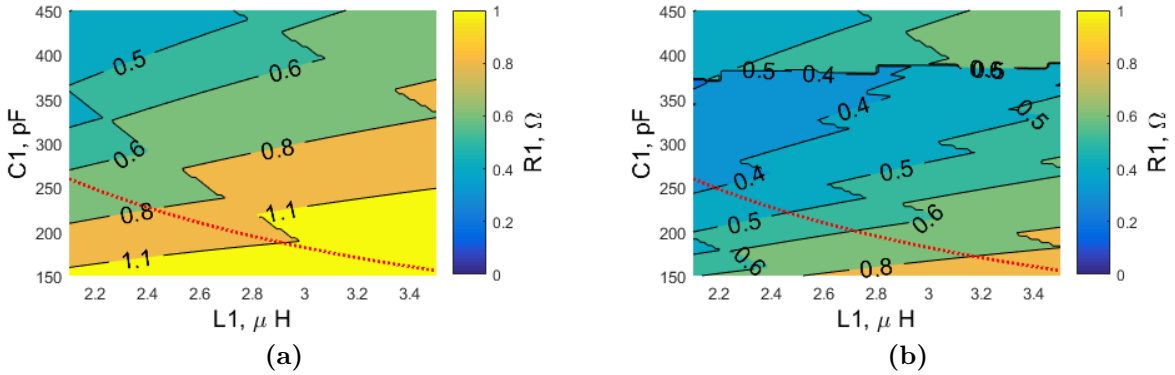


Figure 5.5: Coil design after optimization for minimum ESR for $h = 0.25$ mm dielectric 5.5a, and the final transmitter coil design 5.5b. The red curve is the 6.78 MHz LC resonance.

The receiver coil design for different dielectric thickness and the final receiver coil design are shown in Fig. 5.6. The receiver coil design follows a similar shape and explanation to a transmitter coil design. The difference is that the receiver coil has a smaller capacitance range compared with transmitter coil with the same thickness (i.e. Fig. 5.4a vs. Fig. 5.6a), due to the smaller maximum copper area. The optimized ESR over the wide LC range is stored in a coil design look-up table for future use in system optimization.

Inverter Optimization Results

The ZVS inverter optimization is designing the V_{dc}, L_{zvs} and dt to have minimum loss for a target load (V_1, I_1, ϕ_1). V_1 is iterated from 10 V to 120 V with a step of 1 V. I_1 is iterated from 0 A to 3 A with a step of 0.1 A. ϕ_1 is iterated from capacitive 25 ° (-10 ns) to inductive 75 ° (+30 ns) with a step of 1 ns. The range is subject to expand if the final system optimization reaches the limit. The optimized inverter design is shown in Fig. 5.7.

Fig. 5.7 is difficult to analyze clearly due to the 3D view. Additional plots with different 2D views are provided to supplement. Fig. 5.8 is a slice from Fig. 5.7 at $V_1 = 50$ V.

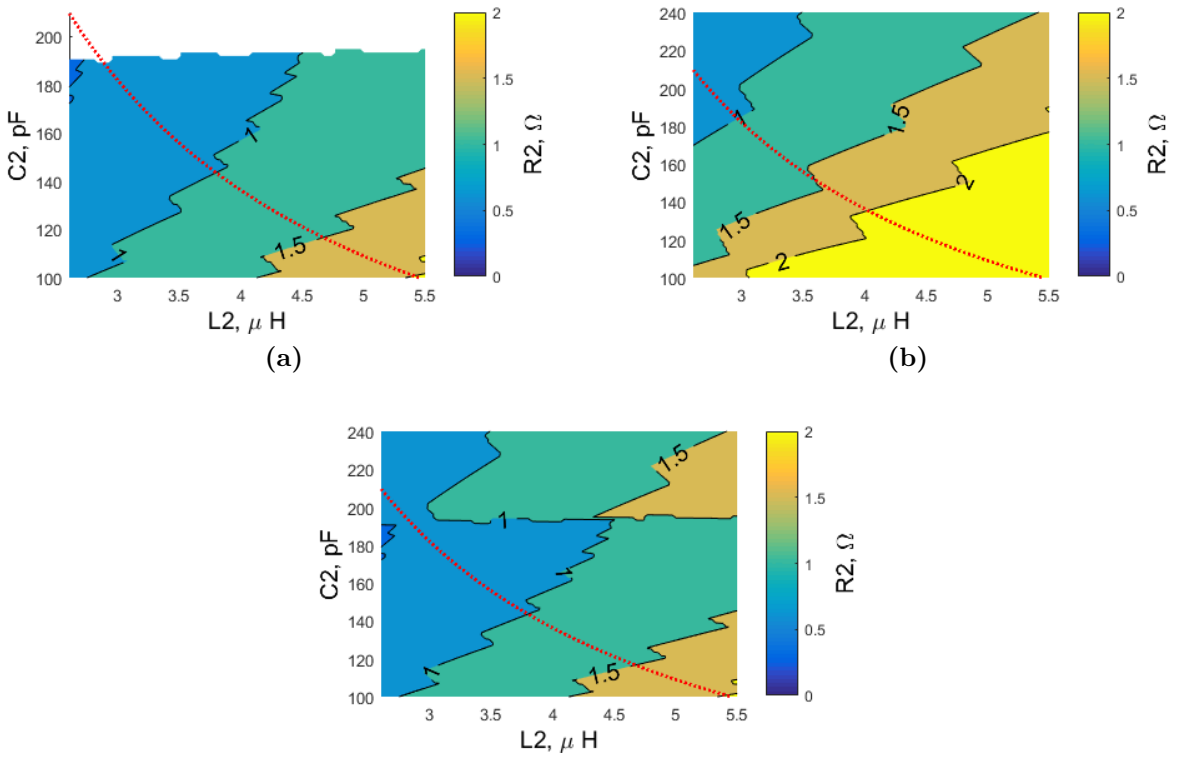


Figure 5.6: Receiver coil design after geometry optimization for minimum ESR for $h = 0.5$ mm dielectric 5.6a, for $h = 0.25$ mm dielectric 5.6b, and the final receiver coil design 5.6c. The red curve is the 6.78 MHz LC resonance.

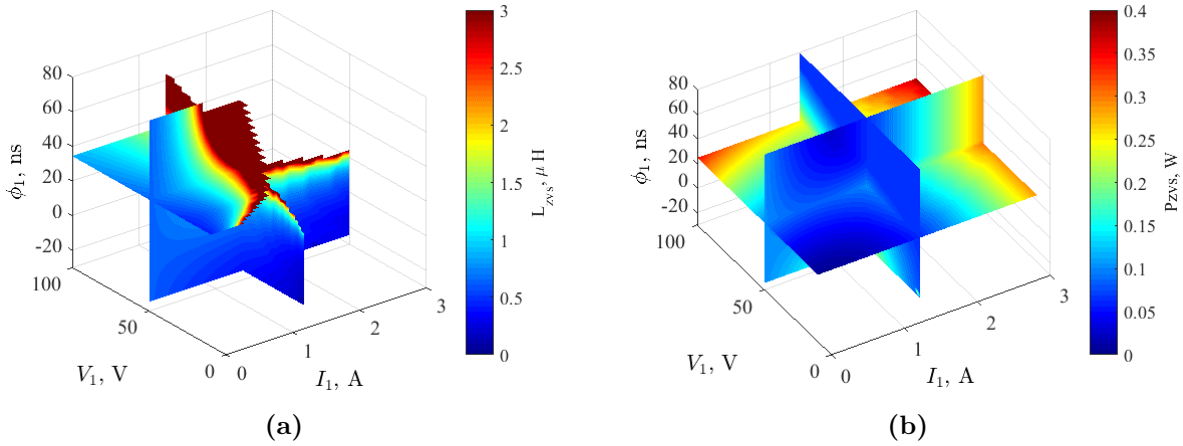


Figure 5.7: The ZVS inductance 5.9a, and the inverter loss 5.9b over wide load range.

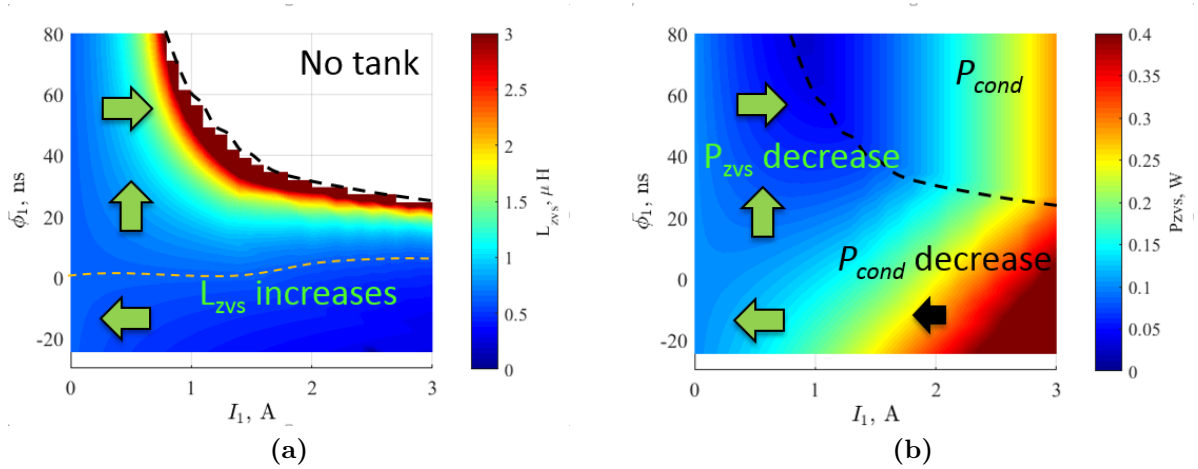


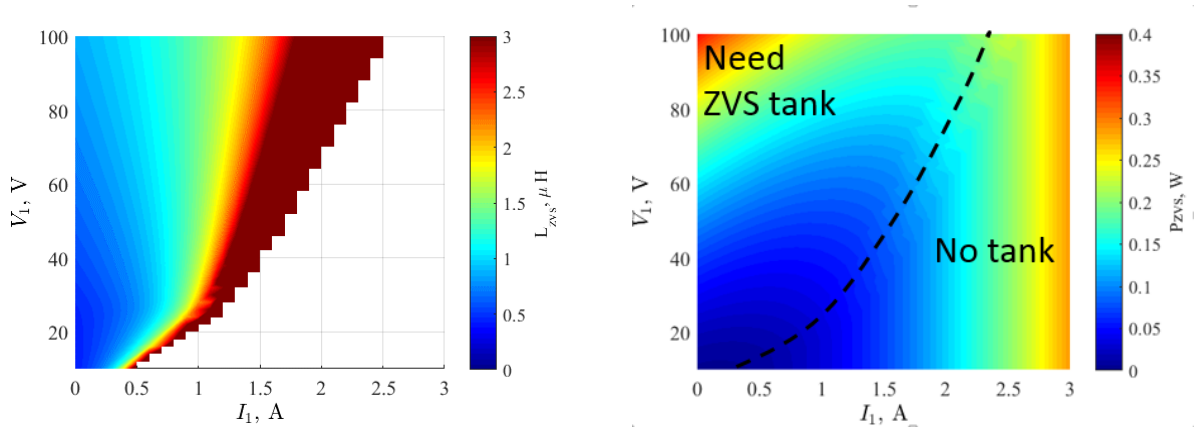
Figure 5.8: The ZVS inductance 5.9a, and the inverter loss 5.9b over wide load range with $V_1 = 50$ V.

Fig. 5.9a is the L_{zvs} vs. I_1 and V_1. L_{zvs} decreases along the green arrow. For all I_1, increasing ϕ_1 reduces the need for ZVS current, reducing L_{zvs}. When ϕ_1 is inductive, increasing I_1 reduce the need for ZVS current, leading to a increased L_{zvs} till finally eliminating the need for auxiliary tank. When ϕ_1 is resistive, decreasing I_1 reduce the need for ZVS current, leading to a increased L_{zvs} but cannot eliminate the need for L_{zvs}. When ϕ_1 is near resistive, I_1 contributes little discharge of the device C_{oss} energy therefore is almost independent to L_{zvs}, shown by the yellow curve which is $L_{zvs}(I_1 = 0)$ contour.

The inverter loss consists of device conduction loss and the ZVS tank loss. The conduction loss decreases with I_1 and is independent of ϕ_1. The inverter loss distribution follows the L_{zvs} distribution. The inverter loss always decreases with ϕ_1 for all I_1 and the decrease stops when loss on ZVS tank is eliminated. ZVS tank loss dominant over conduction loss for I_1 around 0. For inductive ϕ_1 when I_1 increases, inverter loss first decreases because L_{zvs} increases leading to a decreased ZVS tank loss which approaches zero zero, then increases because P_{cond} increases and dominates the loss. For capacitive ϕ_1 when I_1 increases, inverter loss always increases because both tank loss and device conduction loss increase with I_1.

Fig. 5.9 is a slice from Fig. 5.7 at $\phi_1 = 37$ °. Fig. 5.9a is the L_{zvs} and vs. I_1 and V_1 and Fig.5.9b is inverter loss vs. I_1 and V_1. The analysis method are the same as in Fig. 5.8.

The optimized losses over the wide (V_1, I_1, ϕ_1) range are stored in an inverter design look-up table for future use of system design.



(a) (b)

Figure 5.9: The ZVS inductance 5.9a, and the inverter loss 5.9b over wide load range with $\phi_1 = 37\ °$.

5.3.2 The Interdependence of Each Part

Based on the optimized individuals, the overall loss inter-dependence is shown in Fig. 5.10 and will be explained in detail.

The rectifier loss is coupled with the receiver coil loss when designing for a constant P_o. Fig. 5.11 shows this interdependence. PA_{rec} and PB_{rec} are arbitrary rectifier designs with different V_o and I_2. The different I_2 links the rectifier loss to different receiver coil loss shown by the two planes SA_{rcoil} and SB_{rcoil}. Every point on each plane has different loss. Choosing the higher loss receiver design (PA_{rec}) means at the same time choosing the higher loss receiver coil design plane SA_{rcol}. The loss on the receiver coil is coupled with the loss of the rectifier.

Further, the receiver coil loss links with the transmitter coil loss Fig. 5.12 shows this interdependence. PA_{rcoil} and PB_{rcoil} are arbitrary receiver designs on SA_{rcoil}. The two points contain rectifier design information PA_{rec} and link with the transmitter coil loss shown by the two surfaces SA_{tcoil} and SB_{tcoil}. Choosing the lower loss receiver coil, PA_{rcoil}, means at the same time choosing the high loss transmitter design SA_{tcoil}, and the rectifier design PA_{rec}. The loss on rectifier, receiver coil, and transmitter coil are coupled.

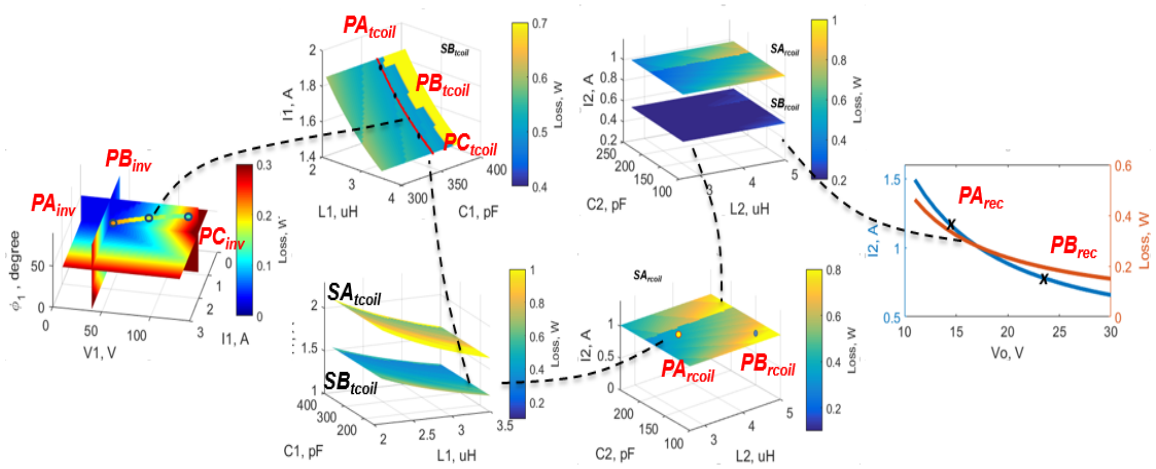


Figure 5.10: Diagram showing the interdependence of the loss from all parts.

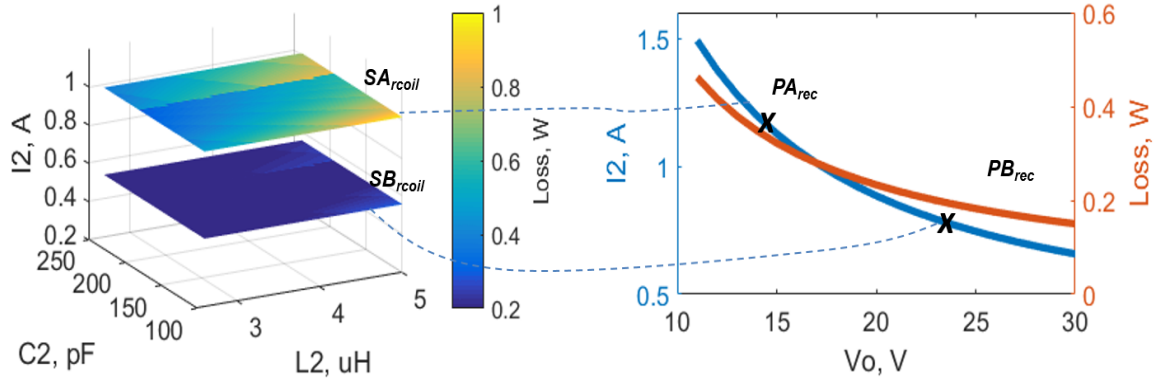


Figure 5.11: Diagram showing the link between the rectifier loss and the receiver coil loss.

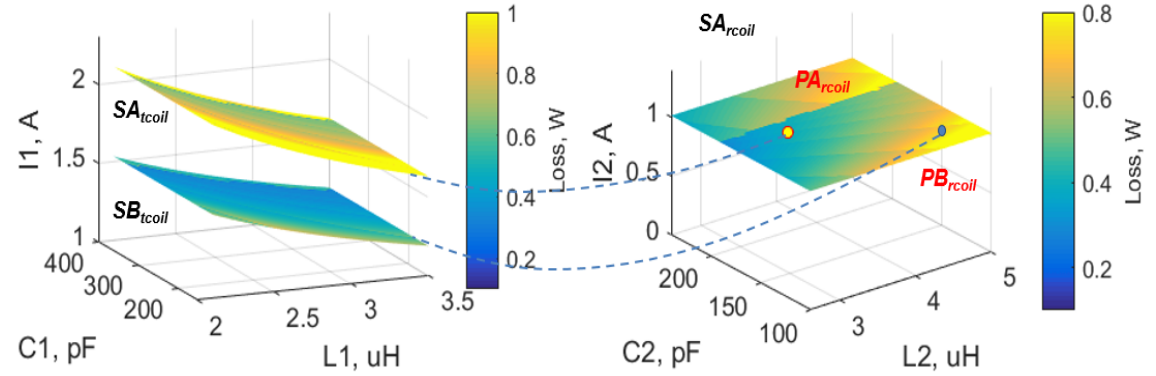


Figure 5.12: Diagram showing the link between the transmitter coil and the receiver coil loss.

Finally, the transmitter coil loss links with the inverter loss when the inverter is designed for minimum loss while still transferring P_o and V_o. Fig. 5.13 shows the link between the transmitter coil loss and the inverter loss.

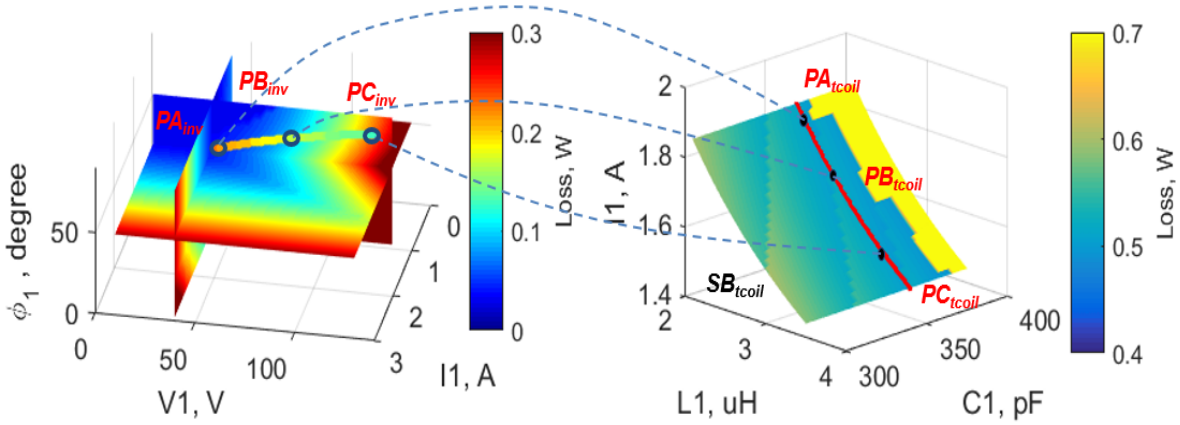


Figure 5.13: Diagram showing the link between the transmitter coil and loss the inverter loss.

PA_{tcoil}, PB_{tcoil} and PC_{tcoil} are three arbitrary transmitter designs on SB_{tcol} and they are all on the red curve. The three points contain information of the receiver design and links with the inverter design PA_{inv}, PB_{inv}, and PC_{inv}. The red line of the transmitter coil design links with the colored line in the inverter design. Tho the transmitter coil has similar loss along the red line, they link to inverter designs that have a different loss. The losses of all stages are inter-dependent.

With this loss independence, separate design of individual stages may lead to high loss design of other stages. For example,

5.3.3 Iteration of All Design Parameters

The second step of the overall design is iteration of V_o, L_2, C_2, L_1 and C_1 based on the overall design method. Among all iterated designs, the optimal design is found with the minimum loss of 1.26 W and the highest efficiency of 88.80 %. The loss breakdown is plotted in Fig. 5.14.

The optimized system variables are summarized in Table 5.1.

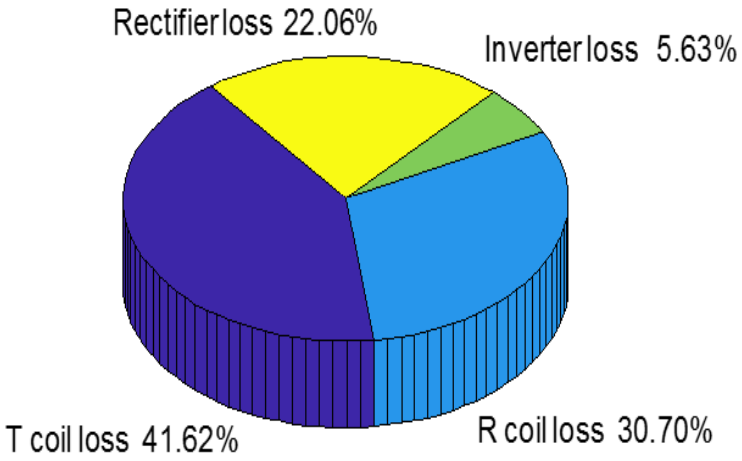


Figure 5.14: Optimized system loss breakdown.

Table 5.1: Parameters of the optimized system.

L_1	C_1	R_1	L_2	C_2	R_2	V_{dc}	L_{zvs}	dt	V_o
3.41 μH	386 pF	0.4 Ω	3.34 μH	175 pF	0.76 Ω	99 V	NO	37 ns	17 V

5.3.4 Discussion on the Optimal Result

In order to prove the designed system is optimal, other systems with sub-optimal designs are examined and compared with the proposed optimal system. First, the transmitter design, including the transmitter coil and inverter, is examined. In this step, the receiver coil keeps the previous optimal design parameters. The transmitter coil is varied along the constant $C_1 = 376$ pF curve which passes the optimal transmitter point. The inverter is co-designed accordingly to provide the constant V_o and P_o. The dashed red curve links to the doted colored curve in the inverter design, where the blue circle on the transmitter coil and the black circle on the inverter design mark the optimal design point. The inverter co-designed with changing transmitter design is shown in Fig. 5.15

The loss breakdown when varying the transmitter coil is shown in Fig. 5.16, where the blue circle marks the optimal design point.

When L_1 increases from 2.5 to 3.4, I_1 decreases leading to the decreased loss on both the transmitter coil and the device conduction loss. When L_1 further increases, the I_1 is

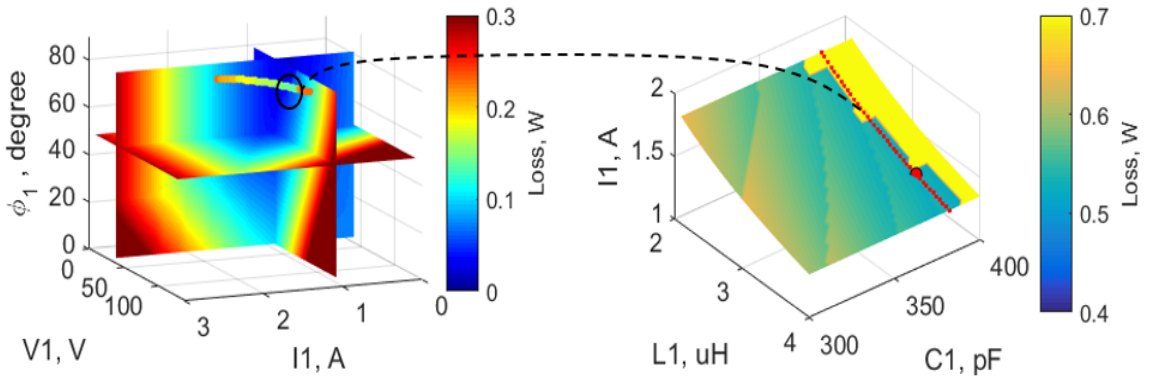


Figure 5.15: Inverter co-designed with changing transmitter design for the optimal receiver set-up.

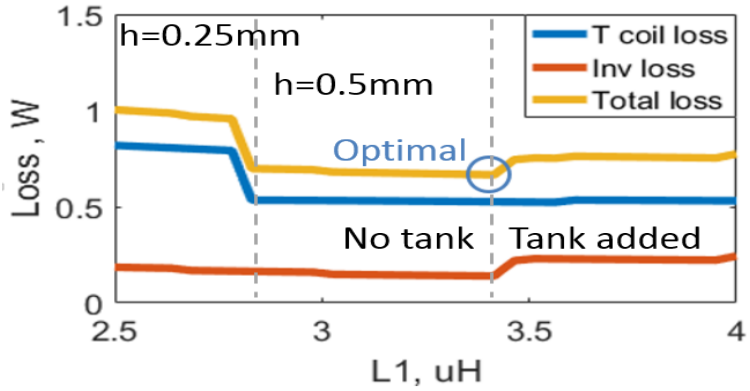


Figure 5.16: Optimized efficiency and loss bread down vs. iterated V_o.

insufficient to provide the required ZVS current and auxiliary tank is needed, leading to the increased inverter loss. At the optimal inductance value, the overall loss is minimized.

The second step is checking if the receiver coil has better designs than the iterated optimal design. In this check, the receiver coil is varied along the LC curve that cancels the rectifier reactance power, which passes the optimal receiver coil design point shown by the yellow dot. The transmitter coil keeps the same design as the iterated optimal design. The inverter is co-designed with receiver coil and transmitter coil provided P_o at the proposed optimal V_o. The plot showing the link of the loss on the coils and inverter when the receiver coil is varied is shown in Fig. 5.17.

The dashed red curve on the receiver coil design is the aforementioned reactance cancellation curve. The cancellation curve locates near the coil LC resonance curve. Any point on this curve links with one surface on the transmitter coil design. Because transmitter

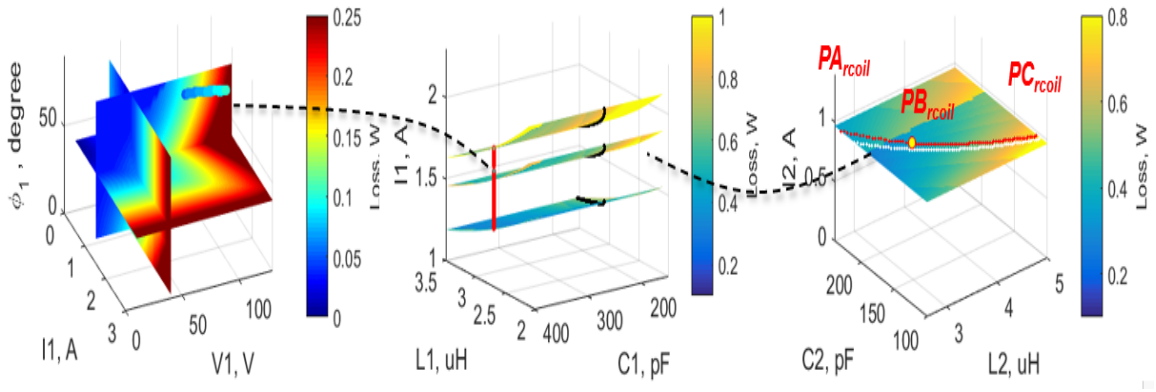


Figure 5.17: Inverter co-designed with changing transmitter design for the optimal receiver set-up.

LC uses the proposed optimal value, the linked multiple surfaces are reduced to one curve, shown by the red dot in the transmitter coil loss design region. Each point has a different loss. Further, each point links with one inverter design to provide the V_o and P_o and the red curve links with the colored curve in the inverter loss design region.

The loss breakdown vs. the varying receiver coil is shown in Fig. 5.18, where the blue circle marks the optimal receiver coil design.

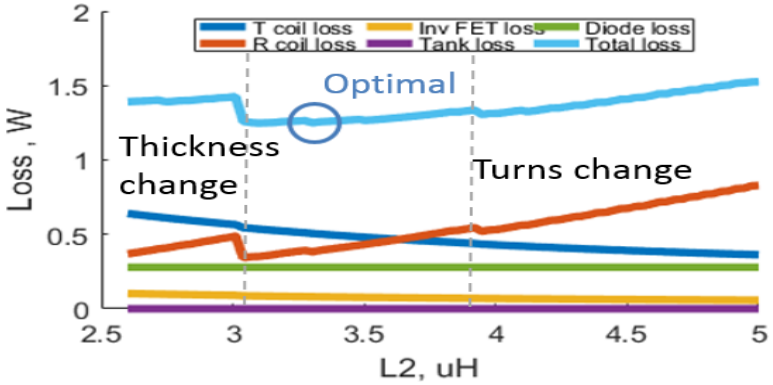


Figure 5.18: Optimized efficiency and loss bread down vs. iterated V_o.

The loss on the diode is constant because V_o is designed to be constant. Loss of transmitter coil and inverter conduction loss decreases with increasing L_2 because I_1 decreases with L_2. As I_2 is constant due to the constant V_o, the loss of receiver coil generally increases with L_2 as shown in the receiver coil design region. The glitches are caused by the change of the integral number of turns. The minimum total loss design agrees with the proposed optimal receiver coil design.

5.4 WPT System Efficiency Experimental Tests

5.4.1 WPT System Prototype

A WPT system prototype including GaN inverter, self-resonant transmitter and receiver coils, and Schottky diode rectifier is built to verify the system modeling at 6.78 MHz. The WPT system is required to transfer 10 W.

The inverter is a full bridge inverter connected to a DC power supply and controlled by an FPGA with adjustable dead-time control for ZVS. The switches are EPC2035, 60 V GaN switches. The rectifier is a full bridge diode rectifier connected to an electronic load. The diodes are SS2P4, 40V Schottky diodes. Both coils are series self-resonant coils built with 1oz copper foil and Teflon-based dielectric. The two coils have the same geometry and diameter of 10 cm. The LCR parameters are measured using Agilent 4294A impedance analyzer. A set of wooden bars is used to fix the positions of the two coils with a 5 cm air gap. Table 5.2 lists the measured coils parameters

Table 5.2: Specifications of the WPT coils.

Parameters	Symbol	Value
Transmitter coil inductance	L_1	3.354 μH
Transmitter coil capacitance	C_1	177.8 pF
Transmitter coil Resistance	R_1	0.884 Ω
Receiver coil inductance	L_2	3.547 μH
Receiver coil capacitance	C_2	176.3 pF
Receiver coil Resistance	R_2	0.885 Ω
Coupling	k	0.0887

Fig. 5.19 shows a picture of the prototype

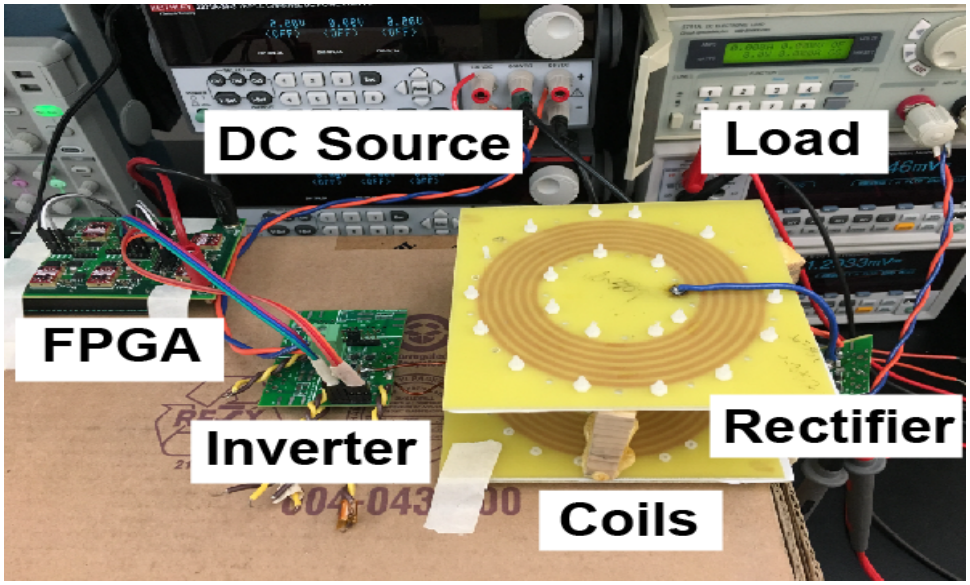


Figure 5.19: Picture showing the experimental WPT prototype.

5.4.2 Coupling Measurement

L_P is denoted as the total inductance of two coupled coil when connected in a positive coupled way. L_n is denoted as the total inductance of two coupled coil when connected in a negative coupled way. The mutual inductance M is constant with the fixed position.

$$L_p = L_1 + L_2 + M \tag{5.5}$$

$$L_n = L_1 + L_2 - M \tag{5.6}$$

From definition, $M = k\sqrt{L_1 L_2}$. Therefore k is calculated

$$k = \frac{L_p - L_n}{4\sqrt{L_1 L_2}} \tag{5.7}$$

Using this method, the coupling factor is measured to be 0.0887.

5.4.3 Working Waveforms

The working waveforms are shown in Fig. 5.20. The green curve is the output voltage of the diode rectifier V_o. The pink curve is the receiver side resonant current i_2. The light blue

curve is the transmitter side resonant i_1. The dark blue curve is the switched-node voltage of one phase leg.

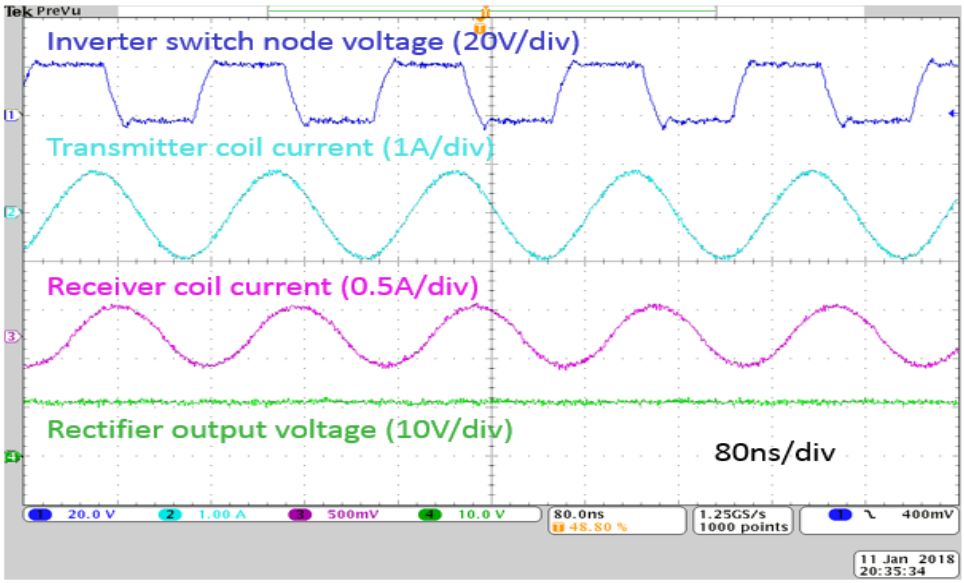


Figure 5.20: Switching voltage and resonant currents waveforms when the inverter operates in full bridge.

5.4.4 System Efficiency Tests Results

The DC to DC efficiency is measured by measuring the input DC voltage and current and the output voltage and current of the rectifier. Fig. 5.21 shows the measured and calculated efficiency of the 10 W WPT system with various load resistances ranging from 25 Ω to 60 Ω. Fig. 5.22 shows the loss comparison. The calculated efficiency matches well with experimental results. The typical error of loss calculations is within 3 %, proving the accuracy of the complete system model.

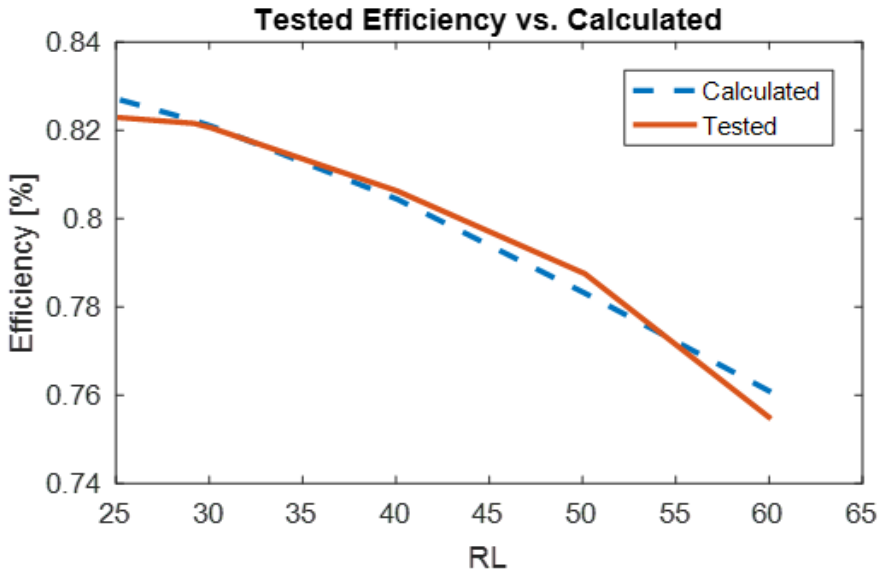


Figure 5.21: DC-DC efficiency test results with calculation results, with 10 W output power.

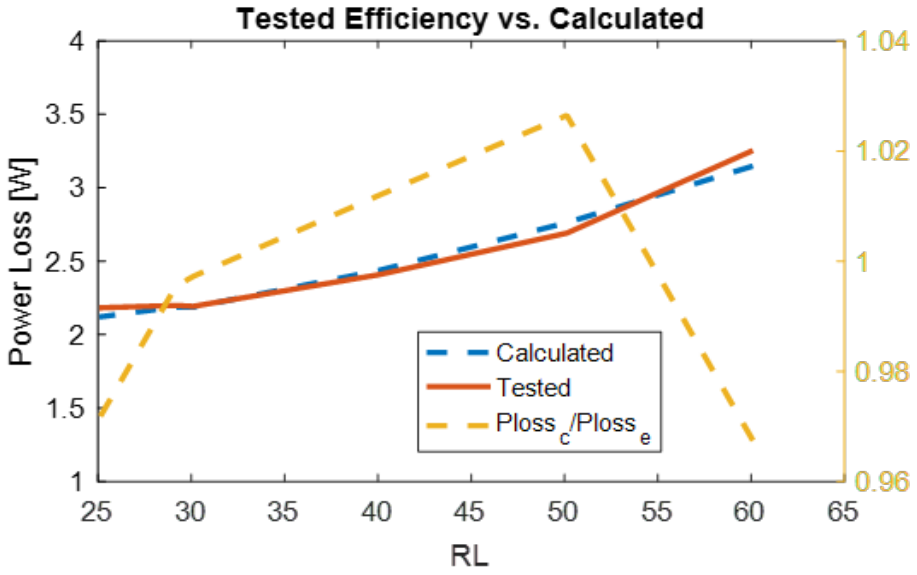


Figure 5.22: Total loss tests results with calculation results, with 10 W output power.

It should be noted that the system parameters are not the final optimized system parameters. The goal of this experiment is verifying the the modeling accuracy.

The calculated efficiency matches well with experimental results. The typical error of loss calculations is within 3 %, proving the accuracy of the complete system model. The calculated loss break-down is shown in Fig. 5.23. As RL increases, larger V_o is needed to transfer a constant power. The increase of V_o leads to a smaller I_2, which reduces the loss of receiver coil and diodes. More I_1 is needed to generate the higher induced voltage, increasing the loss of transmitter coil and GaN FET.

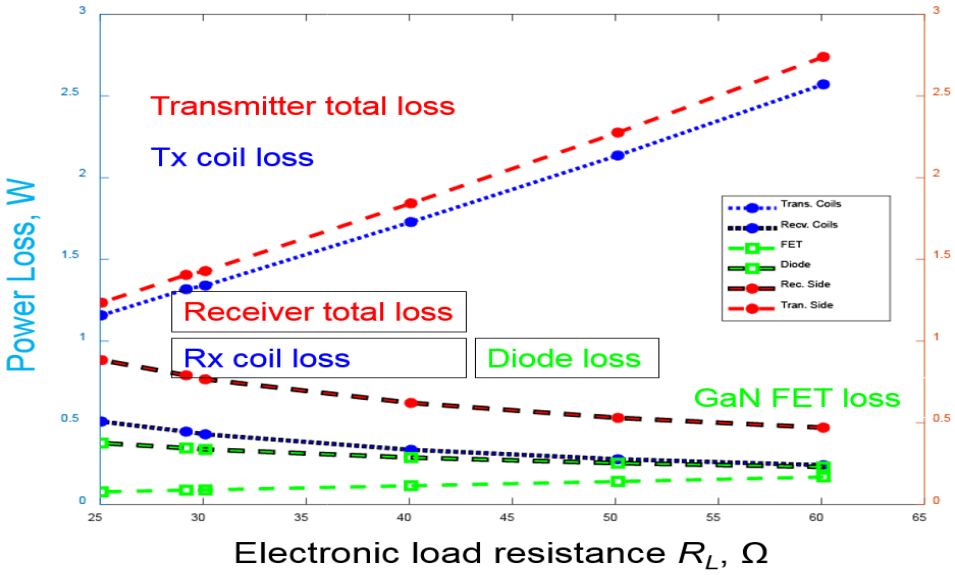


Figure 5.23: Loss breakdown based on calculation with 10 W output power.

5.4.5 Comparison to Existing WPT Systems

The state-of-art reported WPT systems working around 6.78 MHz and with similar power level have been summarized in Table 2.2. It is reproduced here as Table 5.3 including the thesis prototype and the proposed optimized WPT system. Fig. 5.24 visualize the comparison with a highlight on the efficiency with respect to the normalized distance. In comparison to other WPT systems, the thesis prototype #8 has excellent efficiency while the proposed system #9 is even better than the prototype. Prototype #6 in the literature also has excellent efficiency and large normalized transfer distance. Compared to the thesis's work, #6 uses a solenoid coil with large diameter and thickness for high-quality factor. The size is problematic for consumer electronics application where diameter and thickness are strictly limited. #6 uses an active rectifier with ZVS tank to reduce rectification loss. However, the active bridge needs additional driver circuit and the ZVS tank adds size and cost. The thesis's optimized work has a similar efficiency and normalized transfer distance compared with #6, and the thesis's optimized work has a much more compact size than #6.

Table 5.3: WPT system end-to-end efficiency review.

#	Reference	f_s [MHz]	D_c [cm]	d	d/D_c	k	P_o [W]	η [%]
1	[26]	7.65	59 (28)	70	1.61	–	12	50
2	[28]	6.78	23.5	5	0.21	–	24	73
3	[29]	6.78	11.3	4	0.38	–	10	72
4	[48]	6.78	11.3	5	0.44	0.18	10	80
5	[49]	13.56	20	10	0.50	0.075	40	76
6	[11]	0.91	30	20	0.68	0.08	10	89
7	[11]	0.91	30	40	1.33	0.02	10	73
8	This prototype	6.78	10	5	0.50	0.09	10	82.3
9	Optimized design	6.78	10	5	0.50	0.1	10	88.8

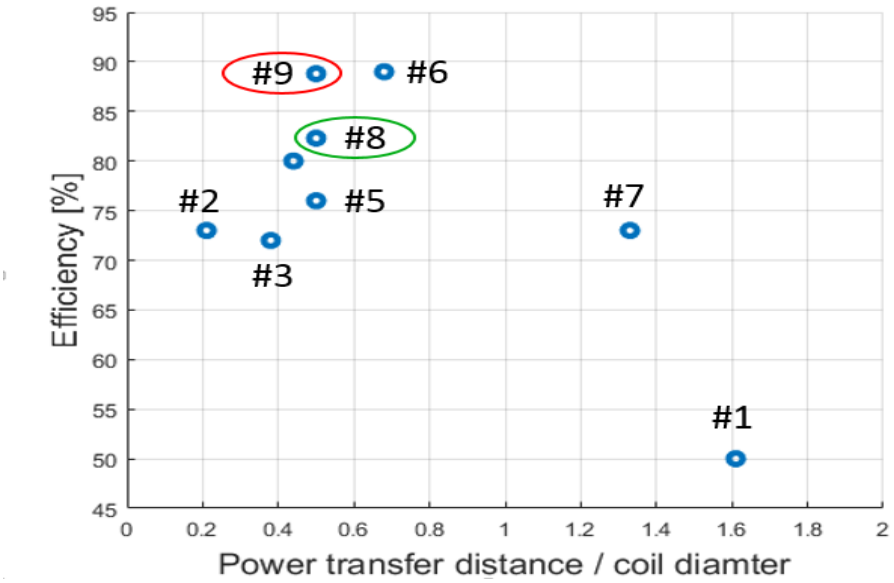


Figure 5.24: Efficiency comparison of the system listed in Table. 5.3. The red circle is the preliminary fabricated prototype and green circle is the proposed optimized design.

5.5 Summary

Based on the developed individual model, a WPT system equivalent circuit is used to bound the design of individual stages to form a complete system, of which the coils and the inverter have been optimized to the extent possible, leaving a reduced design space where all non-optimal designs have been eliminated. The coil optimization design transfers initial coil geometric design parameters to the system design parameters LCR with each LC associated with one ESR. The inverter optimization design transfers the inverter design from V_{dc}, L_{zvs}, dt to a single optimal inverter associated with the required output. The rectifier modeling bridges the circuit output voltage to the equivalent circuit model. Because output voltage is one of the design specification and because it starts the link with other parts, iteration that starts from the output voltage, then to Rx design, then to Tx coil design, and finally to inverter design is proposed as the design method. The selection of parameters and the design sequence is key of the proposed system design methodology. Compared with previous system design method, this new design includes ZVS operation and diode reactive power, resulting in a comprehensive design method for 6.78 MHz WPT systems. The system model has been verified by experiments.

Chapter 6

Conclusion and Future Work

6.1 Conclusions

The promise of higher power and larger spatial freedom has driven the operating frequency of consumer electronics WPT systems into the MHz range. Motivated by the need for a WPT system which exhibits high efficiency and compact size, this thesis details the analysis, design, and prototyping of a resonate WPT system. From the careful literature review, it is discovered that current design method of coils is insufficient for consumer electronics applications due to the strict sensitivity of size. The current power stage design method is insufficient or inaccurate for WPT applications where wide loading situations need to be considered. The system-level design method is based on assumptions that are not generally true due to the neglect of ZVS requirement and diode rectifier reactance. Instead, previously established techniques in coil design are applied to invent a new coil structure for reduced ESR while achieving a compact size. Previous ZVS inverter and diode rectifier topology are combined with waveform and circuit analysis to develop new accurate modeling and design method for a wide load range. From the resulting coil and converter models, an entire WPT system model and design methodology are proposed which highlights the design parameters selection and the design sequence. These techniques together contribute to a WPT system in terms of both high efficiency and compact size. Contributions of the thesis are summarized as follows.

6.1.1 Series self-resonant coil

Motivated by previous coil design methods, a new coil structure is proposed in Chapter 3. Applied to the coil are multiple ESR reducing techniques: foil structure with reduced skin effect, multiple layers structure with better current sharing, a self-resonant structure with reduced compensation capacitor loss, and series LC impedance with no need for impedance matching when connecting to VSI. In given geometry constraints, this coil is capable to produce much larger inductance compared with other series self-resonant structures due to the multiple turns, while maintaining extremely compact thickness. Compared with the state-of-art coils reported in the literature, a prototype coil with the proposed structure has an excellent normalized quality factor Q_d which benefits system efficiency. Complete modeling of the coil LCR are provide based on FEA-assisted analysis and verified by prototypes. The resulting model is further developed into a geometric design method that minimizes ESR for target LC. The single optimal ESR with LC is used in future system design considering a wide range of LC.

6.1.2 Accurate Converter Modeling Covering a Wide Load Range

In transient from previous kHz WPT to the target 6.78 MHz WPT, the obviously magnified switching frequency causes resonant transition times to constitute a significant portion of the switching period. Because the resonant transition intervals are expected to be significant in the proposed application, traditionally diode rectifier resistive modeling in relatively low frequency and higher power applications is no longer true. Accurate waveforms of the rectifier are analyzed using an analytical expression, which further is used to model the input characteristics of the rectifier with an arbitrary load. The resulting analytical model covers wide loading situations thus suitable in WPT system design.

In 6.78 MHz WPT systems, the inverter is desired to provide target output power with ZVS operation for safe operation. Because inverter load may change drastically due to load/distance variations, the traditional ZVS inverter utilizing auxiliary tank topology is accurately modeled to cover arbitrary output load. Analytical waveform modelings are used to further develop the inverter design model to achieve a required output. Based on the

design model, an inverter optimization that achieves minimum inverter loss is detailed. The resulting inverter solution is a single optimal design for any required output, which is used in future system design considering wide load range.

6.1.3 Entire WPT System Design Method

Based on the developed individual model, a WPT system equivalent circuit is used to bound the design of individual stages to form a complete system, of which the coils and the inverter have been optimized to the extent possible, leaving a reduced design space where all non-optimal designs have been eliminated. The coil optimization design transfers initial coil geometric design parameters to the system design parameters LCR with each LC associated with one ESR. The inverter optimization design transfers the inverter design from V_{dc}, L_{zvs}, dt to a single optimal inverter associated with the required output. The rectifier modeling bridges the circuit output voltage to the equivalent circuit model. Because output voltage is one of the design specification and because it starts the link with other parts, iteration method that starts from the output voltage, then to Rx design, then to Tx coil design, and finally to inverter design is proposed as the design sequence. The selection of parameters and the design sequence is key to the proposed system design methodology. Compared with previous system design method, this new design includes ZVS operation and diode reactive power, resulting in a comprehensive design method for 6.78 MHz WPT systems. The system model has been verified by experiments.

6.2 Future Work

In addition to the WPT system design under the current application constraints, further research directions have been identified in the process of completing this thesis. The proposed future work are summarized as follows.

6.2.1 WPT System Design and Component Selection

The proposed design method yields a WPT system exhibiting optimal efficiency with given switching devices and given coupling. In this, the optimization considers the ZVS requirement of inverter switching device, and rectifier reactive power; both are related to switching device selection. In order to explore which devices give the best overall efficiency, a wide device range is examined using the proposed WPT overall design method. The sample inverter switching devices are listed in Table 6.1 and the sample diodes are listed in Table 6.2. V_g is gate-source voltage.

Table 6.1: Sample switching device for inverter.

Part Number	Type	R_{ds} [mΩ]	C_{oss} at 50 V [pF]	Max V_{ds} [V]
EPC2022	GaN	2.4	1376	100
EPC2045	GaN	5.6	419	100
EPC2112	GaN	32	308	200
EPC8009	GaN	90	23	65
IPB027N10N5	Si	2.4 (V_g=10 V)	2817	100
BSC070N10NS5	Si	6 (V_g=10 V)	808	100

Table 6.2: Sample Schottky diode.

Part Number	R_{ds} [Ω]	C_{oss} at 20 V [pF]	V_f at 1 A [V]	V_f at 0.1 A [V]
VSKY20401608	0.14	77	0.44	0.3
SS2P4	0.11	89	0.42	0.31
CDBA240LL-HF	0.09	116	0.28	0.19
5xCDBA240LLHF	0.018	580	0.21	0.19

Using the same system design method and the same coil designs, the optimized system loss breakdown for each combination of devices are shown in Fig. 6.1 where 1-4 represents the first shown diode device to the last shown diode device. Detailed analysis if proposed as future work.

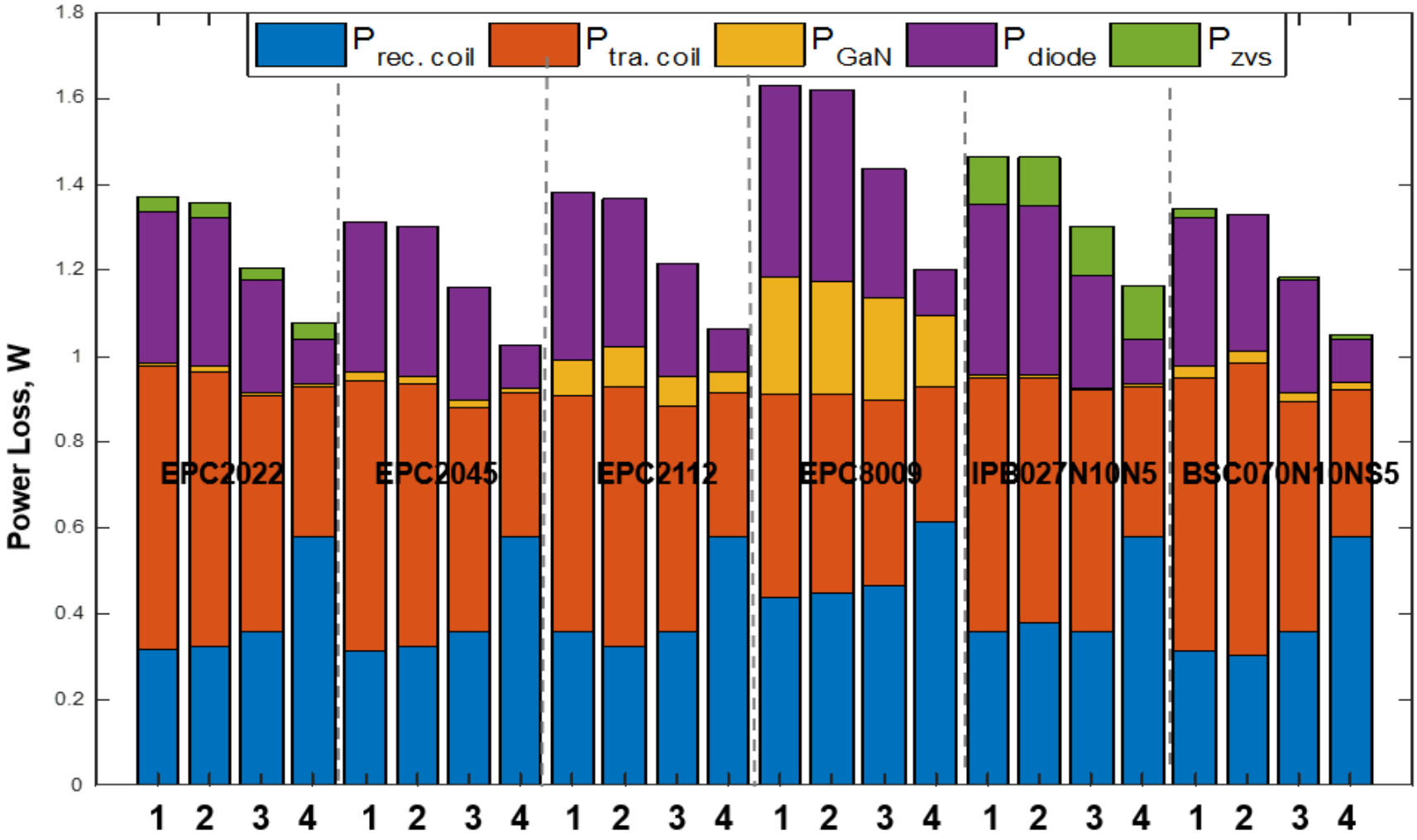


Figure 6.1: Loss breakdown of optimized system using various combination of devices.

6.2.2 Design Over Wide Devices Ranges

Analyzing the loss breakdown of the optimized system using various devices, it is discovered the coil loss still takes a major portion of the total loss. Thus, further optimization of coil design is proposed as the second future work.

A modified series self-resonant coil based on the proposed structure is plotted in Fig. 6.2, which is an unwound shape of the spiral shape. The current flowing inside from the inner layer is split into two directions as shown by the green arrow. The current flows out from both top layer and bottom layer. The skin effect ESR is expected to reduce by 50 %. Considering that the proximity effect causes current crowing on the surface layers, the H-field penetrated to the inner layer is reduced. Thus, the additional two copper layer in the center may have little proximity effect loss. The resulting total loss is reduced, which potentially leads to an increased loss on coils.

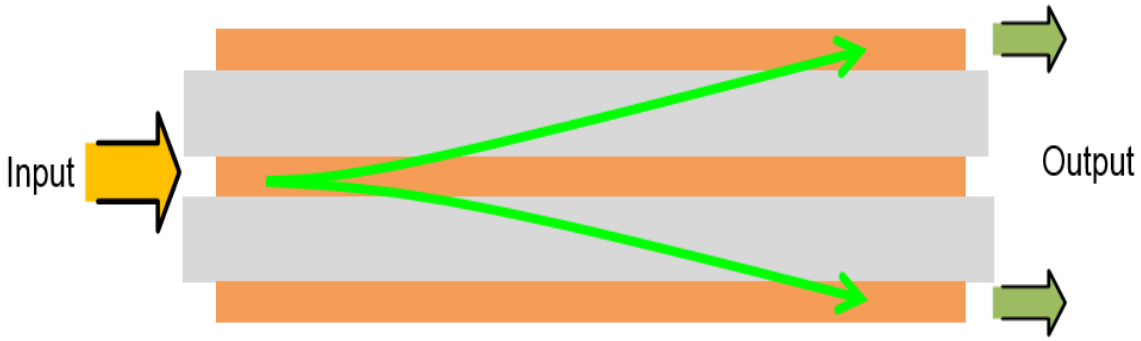


Figure 6.2: Revised structure of the series self-resonate coil with better current sharing for lower ESR.

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Vita

Jie Li was born in Henan, China, where he attended the Xian Jiaotong University as an undergraduate. He graduated in 2014 with a degree in electrical engineering. During his undergraduate studies he held multiple scholarships, participated in undergraduate power electronics research, helped build a wireless power transfer system for Haier Corporation, and co-authored one peer-reviewed journal paper and one conference paper. His undergraduate research evolved into a graduate research under Dr. Daniel Costinett in the University of Tennessee, Knoxville, USA, where he has been focusing on high frequency WPT system design and efficiency optimization.