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# Monolithic Perimeter Gated Single Photon Avalanche Diode Based Optical Detector in Standard CMOS

Md. Habib Ullah Habib
*University of Tennessee, Knoxville*, mhabib4@vols.utk.edu

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I am submitting herewith a dissertation written by Md. Habib Ullah Habib entitled "Monolithic Perimeter Gated Single Photon Avalanche Diode Based Optical Detector in Standard CMOS." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

Nicole McFarlane, Major Professor

We have read this dissertation and recommend its acceptance:

Benjamin J. Blalock, Syed K. Islam, Steven A. Ripp

Accepted for the Council:
Dixie L. Thompson

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

# Monolithic Perimeter Gated Single Photon Avalanche Diode Based Optical Detector in Standard CMOS

A Dissertation Presented for the

Doctor of Philosophy

Degree

The University of Tennessee, Knoxville

Md. Habib Ullah Habib

May 2017

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# Dedicated to

*My wife & son*

Shamsun Naher Islam

Aayaan Habib

*My Parents*

Md. Sanaullah

Diluara Begum

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# Abstract

Since the 1930's photomultiplier tubes (PMTs) have been used in single photon detection. Single photon avalanche diodes (SPADs) are p-n junctions operated in the Geiger mode. Unlike PMTs, CMOS based SPADs are smaller in size, insensitive to magnetic fields, less expensive, less temperature dependent, and have lower bias voltages. Using appropriate readout circuitry, they measure properties of single photons, such as energy, arrival time, and spatial path making them excellent candidates for single photon detection. CMOS SPADs suffer from premature breakdown due to the non-uniform distribution of the electric field. This prevents full volumetric breakdown of the device and reduces the detection efficiency by increasing the noise. A novel device known as the perimeter gated SPAD (PGSPAD) is adopted in this dissertation for mitigating the premature perimeter breakdown without compromising the fill-factor of the device. The novel contributions of this work are as follows.

A novel simulation model, including SPICE characteristics and the stochastic behavior, has been developed for the perimeter gated SPAD. This model has the ability to simulate the static current-voltage and dynamic response characteristics. It also simulates the noise and spectral response.

A perimeter gated silicon photomultiplier, with improved signal to noise ratio, is reported for the first time. The gate voltage reduces the dark current of the silicon photomultiplier by preventing the premature breakdown.

A digital SPAD with the tunable dynamic range and sensitivity is demonstrated for the first time. This pixel can be used for weak optical signal application when relatively higher sensitivity and lower input dynamic range is required. By making the sensitivity-dynamic range trade-off the same detector can be used for applications with relatively higher optical power.

Finally, an array has been developed using the digital silicon photomultiplier in which the dead time of the pixels have been reduced. This digital photomultiplier features noise variation compensation between the pixels.

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# Chapter 1
# Introduction and Motivation

## 1.1 Introduction

Single photon detectors have been rapidly increasing the possible application fields. The development of this technology is based on the principle of the photoelectric effect. Single photon detectors produce a measurable response in response to absorbing a photon. This concept is behind the invention of the photomultiplier tube (PMT) in the 1930's. Through relentless efforts for development, single photon detector technology is currently at a place that was unimaginable in 1930's. The journey from photomultiplier tube to complementary metal oxide semiconductor (CMOS) detector has been challenging and it will definitely move forward.

A single photon avalanche diode (SPAD), a single photon detector, is basically a p-n junction operated in the so-called Geiger mode. Using appropriate readout circuitry, properties of single photons, such as energy, arrival time, and spatial path can be measured [1–3]. SPADs are also excellent candidates for the sensing of the weak optical signals generated in some applications [4, 5]. Thus, SPADs are suitable candidates for image sensors and detectors, particularly where low light intensity levels may be an issue [6–9]. Researchers have been working on SPAD based nuclear imaging and detection devices for positron emission tomography (PET) and

neutron detection applications [10–12]. They are also good candidates for biological applications such as florescence detection and protein analysis. It can also be used in applications such as random number generation [13–15].

CMOS technology has been a dominating factor in various fields since its invention. The field of single photon detection is included. CMOS SPADs are capable of generating a current from a single incident photon. However, due to the planar nature of the technology, SPADs suffer from premature breakdown due to uneven electric field distribution [4,5,16–19]. This reduces the detection efficiency of these devices by increasing the noise. A large voltage, higher than the reverse breakdown voltage of the device, is applied across a SPAD for operation in Geiger-mode. The electric field distributions, caused by the applied voltage, are maximum at the periphery [18, 19]. Therefore, premature breakdown occurs around the edges of the device due to the presence of high electric field and it stops the device from going into full volumetric breakdown [4, 5, 17, 18].

There are a number of strategies to mitigate premature perimeter breakdown in avalanche diodes fabricated in CMOS processes. In a twin-well CMOS fabrication process, lateral diffusion of donor atoms creates a lighter n-doped region at the edge of the p-n junction. This increases the breakdown voltage around the perimeter and prevents premature breakdown [20]. Incorporation of a field-limiting guard ring at a distance from the implant and a gate placed on top of the gap has also proven effective in reducing premature breakdown [21]. However, use of a guard ring reduces the fill-factor, and is therefore not always an ideal option [18, 21]. Fill-factor is

the ratio between the optically active area and the total area of the detector. The combination of the lateral diffusion of n-wells and the depletion gate has also been shown to reduce premature edge breakdown [20, 22]. All of these techniques rely on the modulation of the dopant carrier concentration and modulation of the junction curvature on the breakdown voltage [16, 23]. In deep-submicron CMOS technologies, the use of shallow trench isolation (STI) to modify the junction geometry has been used to prevent edge breakdown [24]. Placement of a perimeter gate on top of the junction and application of the voltage on that gate is also an effective method of preventing premature breakdown while having a large fill-factor [18]. This dissertation fully characterizes, models, and develops a perimeter gated single photon avalanche diode (PGSPAD) with improved noise performance and develops monolithic detection systems using PGSPADs.

## 1.2 Motivation

Figure 1.1 [25] illustrates the diversity of applications supported by single photon detectors. Doing research on something that can create an impact on such a big and diverse field is the main motivation behind this dissertation. Moreover, the depth of the impact this work could create is another inspiration behind this research. In single photon detection the transition from photomultiplier tube to SPADs is a matter of overcoming the shortcomings of the photomultiplier tube.

SPADs are generally designed and fabricated in dedicated fabrication processes making the device expensive. Standard CMOS process can aid in that area. CMOS technology makes the device or system cheaper than commercially available SPAD based detectors fabricated in dedicated process, making this technology accessible to more users. One of the main challenges of a number of consumers of any technology is the cost. This scenario can be realized with the example of the evolution of personal computers or cell phones. A regular positron emission tomography (PET) machine or a radiation detector system is unreachable price-wise to many communities. However, a CMOS SPAD based tomography machine or radiation detector would be significantly lower cost.

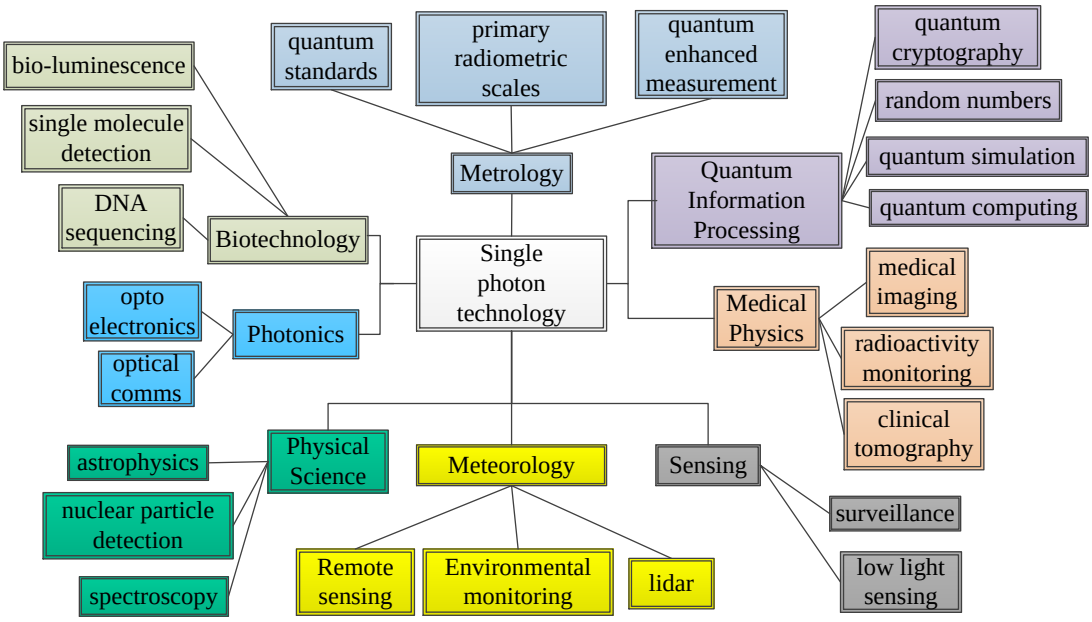



**Figure 1.1:** Application areas for single photon detectors [25].

However, this lower cost many times comes at the cost of a performance reduction. The main challenges of CMOS SPADs lie in the noise performance of the device. In this dissertation, a perimeter gated technique is used to enhance the noise performance. Necessary readout electronics based on the application, can be integrated with the PGSPAD on the same chip in CMOS technology. Integrating the detector with the needed on chip electronics results in a faster system, which is very useful in high speed detection applications.

Many research facilities purchase commercial SPADs and photomultipliers for their research. They are placing the detectors into 2-dimensional arrays. The dead-space between the detectors in these arrays is significantly large. It can be avoided by requesting the manufacturers to fabricate the 2-dimensional array as required on a single chip. Some manufacturers may comply and some may not. In either case, the cost will be very high and without any guaranty the device will operate as expected. In CMOS the whole array could be designed with significantly reduced dead-space through layout techniques and judicious placement of bonding pads or

**Table 1.1:** Advantages of perimeter gated SPADs compared with commercial off the shelf SPADs and regular CMOS SPADs.

| | **Commercial off the shelf SPAD** | **CMOS SPAD** | **CMOS Perimeter Gated SPAD** |
|---|---|---|---|
| **Cost** | $$$ | $ | $ |
| **Monolithic integration** | No | Yes | Yes |
| **Noise (DCR)** | Best | Worst | Better |
| **Breakdown variation control** | No | No | Yes |
| **Speed** | Slow | Fast | Fast |
| **Dead space in array** | Higher | Lower | Lower |

backside bonding. There will be very little dead-space for minimum distance design rules between layers used in design.

The motivation behind using CMOS based PGSPADs as detector could be summarized based on the technology available for detection application. The single photon detection can be done using quantum dots or superconducting detectors. But these processes are not mature enough for mass production at reasonable cost. Additionally, the yields for these techniques are very low. Active pixel sensors (APS) and electron multiplying charge coupled devices (EMCCDs) are not free-running. So, they have to be periodically enabled for a short time window with the aid of an external pulse generator or on chip electronics. SPAD based detectors have advantages over PMTs because they are smaller in size, insensitive to magnetic fields, less expensive, have lower temperature dependency, and moderate bias voltages requirement. Considering the effects of magnetic field, SPADs are the most viable option and CMOS PGSPADs adds the previously mentioned advantages with the option. Table 1.1 shows the advantages of CMOS perimeter gated SPADs over commercial off the shelf SPAD and regular CMOS SPADs.

## 1.3 Research Goals

The goal of this research is twofold. First, the noise performance of the CMOS SPAD is enhanced through the use of the perimeter gated technique. Secondly, perimeter gated single photon avalanche diode based detectors suitable for optical detection

are developed. Using standard CMOS makes the cost lower than commercially available detectors. Improving the noise performance of the detector using perimeter gated technique makes it suitable for relatively weak optical signal (e.g. bio-luminescence application. This perimeter gated technique helps control the noise variation between pixels in an array. The research is divided into the following major parts: (1) optimizing the perimeter gated SPADs for the application, (2) building a comprehensive model of perimeter gated SPADs for simulation before going into fabrication, (3) designing perimeter gated SPAD based optical detectors (e.g. silicon photomultiplier (SiPM), digital pixel), and (4) building compact array of pixel with readout as monolithic detector with noise variation compensation.

## 1.4 Dissertation Overview

The dissertation is organized as follows. A comprehensive literature review of avalanche diodes and readout electronics is presented in Chapter 2. Chapter 3 showcases the research on device characterization. Chapter 4 describes the novel modeling and simulation work in this research. Chapter 5 demonstrates the details of a perimeter gated SPAD based silicon photomultiplier with improved noise performance. Chapter 6 describes the performance of a digital perimeter gated SPAD pixel with tunable dynamic range. Chapter 7 describes the $3 \times 3$ array with a dead time minimization technique and the dissertation is concluded in Chapter 8.

# Chapter 2
# Literature Review

## 2.1 Single Photon Avalanche Diode

In single photon avalanche diodes, the p-n junction is biased beyond its breakdown voltage. This p-n junction device has three different region of operation, (1) forward region, (2) reverse region, and (3) reverse breakdown region. In the forward region of operation, the voltage applied between the anode and cathode of the diode is higher than the junction's inherent potential. The diode is 'on' in this region, allowing for current flow. In the reverse region, the diode is said to be 'off', and a negligible amount of current (the reverse saturation current) flows through the device. With the increase in applied voltage in the reverse region, the electric field magnitude at the junction increases. Past a critical applied voltage, the electrical field at the junction is so high that charge carriers will be accelerated and undergo impact ionization. This creates a sudden huge flow of current. This region is termed as the breakdown region. Geiger-mode avalanche devices (SPADs) are operated in this region. Avalanche photodiodes (APDs) are operated just below their breakdown voltage.

The diode is operated in the breakdown region with negligible leakage current for a very brief period of time before the injection of a charge carrier into the diodes depletion/ space charge region. Free charge carrier may be generated due to noise

processes such as thermal generation, band-to-band tunneling or it may be generated due to a photon providing enough energy to free a charge carrier. This free charge carrier, accelerated under the high electric field, can free other charge carriers through collisions. These new charge carriers are also accelerated under the high electric field and can free more charge carriers in a cascading process. Thus, the injection of the ionizing carrier into the depletion region creates a self-sustaining avalanche of carriers. Keeping the diode biased beyond breakdown and sustaining an every

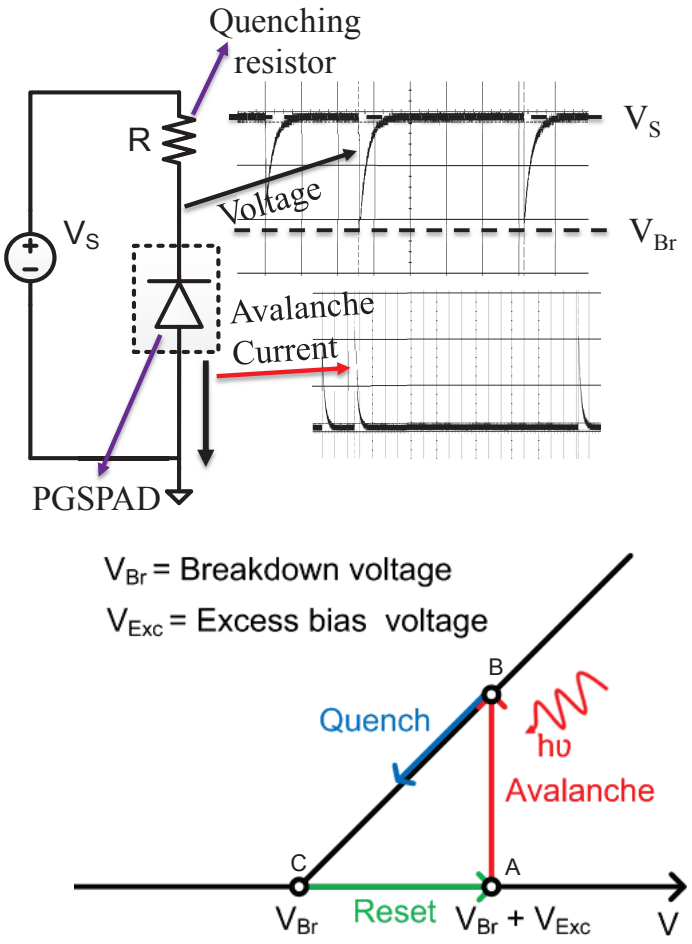



**Figure 2.1:** A PGSPAD in Geiger mode goes through avalanche, quench, and reset with the aid of the quenching resistor. The voltage and current response from the device through a complete cycle is seen as an avalanche of current, followed by a decrease in that current.

increasing current, will heat-up the diode and eventually it will be destroyed. The quenching circuit aids the diode in reducing the applied bias voltage across the diode to a value less than the breakdown voltage, and facilitates the release of free carriers from the diode before going into another avalanche. This mode of operation is known as the Geiger-mode. Properly biased Geiger-mode diodes probabilistically create a current spike that can be converted into a voltage spike (Figure 2.1) following the injection of a single carrier into the diode. The carrier generation process follows Poisson statistics. Single photon avalanche diodes are Geiger-mode avalanche diodes designed to sense carriers injected due to a single photon.

In order to be able to detect the subsequent photons by SPADs after each avalanche, the current must be quenched. This is accomplished by reducing the applied voltage to a voltage below the breakdown value. This process can be attained using a passive quenching arrangement or an active quenching arrangement to implement a large resistor. For each event the device starts from point 'A', goes to 'B' (avalanche), then 'C' (quench, and returns back to 'A' (reset), Figure 2.1. The time taken to quench the diode is given by the $RC$ time constant dictated by the resistors and capacitances at the output of the device. The device becomes non-responsive to other incident photons during this cycle. The time taken for a complete cycle is refereed to as the dead time of the SPAD [4]. Since the dead time is related to the $RC$ time constant, active quenching can significantly reduce the SPAD dead time compared to the passive quenching, and is important for applications in which high instant count rates must be monitored.

## 2.2 Impact Ionization in Silicon

Impact ionization is a charge generation mechanism in semiconductor devices. Depending on the application, it either determines the useful characteristic of the device or it causes an unwanted parasitic effect [26]. The breakdown voltage of a silicon p-n junction diode is caused by impact ionization if the breakdown voltage is relatively large and the temperature coefficient of the breakdown voltage is positive [26]. The doping concentration is relatively less and the depletion region width is relatively wider for devices capable of going to avalanche breakdown through impact ionization. In devices with relatively higher breakdown voltages, the breakdown is caused by tunneling and the temperature coefficient of the breakdown voltage is then negative [26]. This type of breakdown is known as Zener breakdown.

Therefore, impact ionization is essential for a SPAD to respond to incident photons. For impact ionization, relatively higher breakdown voltages is required since the electric field, $E$, generated by the breakdown voltage forces the free carriers to avalanche. Figure 2.2 presents a pictorial illustration of how number of free carriers is multiplied by impact ionization leading to a avalanche current.

### 2.2.1 Ionization Rate

The ionization rate ($\alpha$) is defined as the number of electron-hole pairs generated by a carrier per unit distance traveled [26]. The ionization rate for electrons ($\alpha_n$) and holes ($\alpha_p$) are not the same. For impact ionization, the ionizing carrier has to gain

at least the threshold energy from the electric field. Using the laws of conservation of energy and of momentum at a collision event, it can be derived that a minimum energy of $1.5 \times E_g$, where $E_g$ is the bandgap, is needed if the effective masses of both holes and electrons are assumed equal [26]. Generally, the ionization rates depends on the probability of the carriers to reach the threshold energy. This probability is a function of the local electric field and the previous states on the carrier.

The empirical expression of local avalanche generation reported in [26, 27] is the most commonly used model:

$$\alpha_{n,p} = a_{n,p} exp\Big( - \frac{b_{n,p}}{E} \Big) \tag{2.1}$$

where, $E$ is the electric field in the direction of current. The ionization coefficients, $a$ and $b$, are different for holes and electrons. $a$ is the maximum number of carriers that can be generated per unit distance at very high electrical fields.

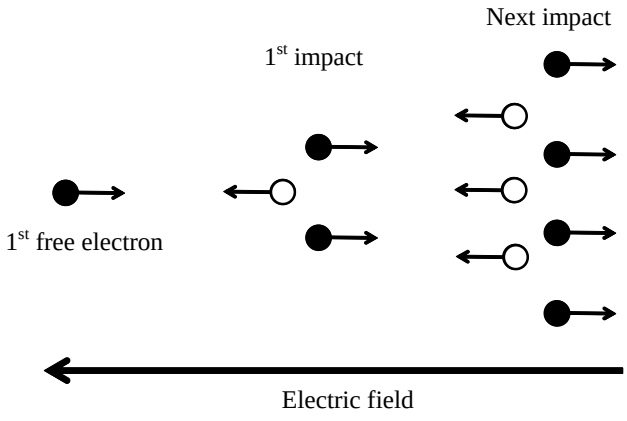



**Figure 2.2:** Impact ionization initiating avalanche current in presence of high electric field. Number of free carriers is multiplied in each step.

The avalanche generation term is used in the current continuity equations as [26]:

$$\Delta J_{n,p} = \pm(G_{n,p} - R_{n,p}) \tag{2.2}$$

where, $J_{n,p}$ is the current density for electrons and holes respectively,$G_{n,p}$ the generation, and $R_{n,p}$ is the recombination rate. The plus sign has to be used for holes and the minus sign for electrons. The generation term for avalanche generation can be written as [26]:

$$G_{n,p} = \frac{\alpha_n |j_n|}{q} + \frac{\alpha_p |j_p|}{q} \tag{2.3}$$

The theory of ionization rate is very important to understand how the applied voltage across the p-n junction in a SPAD affects its optical and noise characteristics.

## 2.3 CMOS Single Photon Avalanche Diode

From the beginning of 21st century, researchers have explored the possibilities of fabricating SPADs in standard CMOS. This facilitates the integration of the SPADs, quenching and sensing electronics, and digital processing blocks on the same chip. This monolithic integration for implementing smart photon-counting and photon-timing on-chip processing was one the main goals for fabricating SPADs in CMOS. Moreover, since standard CMOS is relatively cheaper, cost minimization was another reason to move towards CMOS technology.

### 2.3.1 Noise of CMOS SPAD

In CMOS SPADs, when biased beyond the breakdown voltage, the generated free carrier create an avalanche and produces a spike response with the help of a quenching resistor. Ideally, the device should generate free carrier by absorbing energy from the incident photon. So, in complete darkness (absence of photon) the SPADs should be idle and have no output.

However, carriers generated from other phenomena can also go through impact ionization and create an avalanche. Therefore, without any incident photon the device generates response or spikes due to thermally generated carriers, carriers due to band-to-band tunneling, and diffused carriers. This noise is known as the dark count rate (DCR). The number of unwanted response per unit time in complete darkness is defined as the dark count rate.

#### 2.3.1.1 Noise Due to Thermal Generation

The atoms in the crystal lattice of the semiconductor vibrate. With the increase in temperature, the electrons gain energy high enough to travel to the conduction band from the valance band, and thus a free carriers are generated. This is known as thermal generation in a semiconductor. The thermal generation rate can be calculated using the Shockley-Read-Hall theory. The total number of generated carriers is proportional to the area of the device and the thermal generation rate also increases

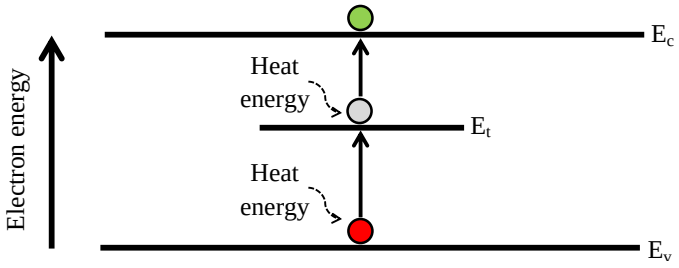



**Figure 2.3:** Thermal generation of free carriers. Vibration in atoms, due to temperature, creates free electron by releasing a valence electron from covalent bond. Forbidden/ trap states ($E_t$) helps in moving the electron from the valance band to conduction band.

with temperature. This determines how the device size and temperature affect the noise of SPADs. Figure 2.3 illustrates the thermal carrier generation process.

#### 2.3.1.2 Noise Due to Band-to-Band Tunneling

In CMOS technology, devices are becoming smaller very rapidly and the depletion layers are becoming extremely thin. With narrow depletion region and higher applied electric field, the potential barrier between the valance band and the conduction band ($E_c$-$E_v$) in the depletion region becomes small enough for electrons to quantum mechanically tunnel into the conduction band from the valance band (Figure 2.4). This phenomenon, known as band-to-band tunneling, creates free carrier and initiate

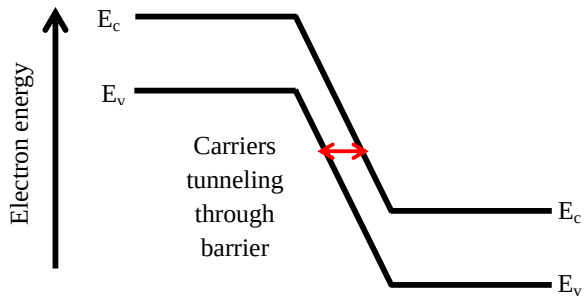



**Figure 2.4:** Carriers tunneling through narrow potential barrier in the depletion region.

the avalanche process. So, carriers generated from band-to-band tunneling are another source of noise in CMOS SPADs. This carrier generation phenomena has a dependency on the electric field in the depletion region. The number of generated carrier due to band-to-band tunneling also depends on the area and applied reverse bias voltage of the device. Therefore, the area and biasing have roles to play in the noise performance of the SPAD.

#### 2.3.1.3 Noise Due to Carrier Diffusion

The diffusion of minority carrier from neutral region to depletion region can also create free carriers which can initiate an avalanche. Prior study, presented in [28], shows the effect of this phenomena is negligible. The number of generated carrier in this process is 2-3 order of magnitude smaller than other carrier generation mechanisms.

## 2.4 CMOS SPAD Noise Minimization Techniques

Research groups, around the world, have been working on developing different SPAD structures at different CMOS technology nodes [29–52] for handling different issues such as premature edge breakdown, tunneling effects, electric field uniformity, sensing electronics complexity, and wide depleted region thickness.

The noise contribution from the thermally generated carrier can be minimized by cooling [53]. At relatively low temperatures, the rate of the thermally generated carriers becomes very low compared to carrier generation due to band-to-band

tunneling. The variation in dark count rates due to band-to-band tunneling is negligible over a broad temperature range. Therefore, operating the device at low temperatures reduces the dark count rate due to thermal generation. However, cooling does not help for the noise due to the tunneling phenomenon.

Since CMOS SPADs are planar device, the premature breakdown at the edges occurs due to the non-uniform distribution of the electric field. This worsens the noise contribution by the carriers generated due to band-to-band tunneling. Preventing the premature breakdown enables the device to go into full volumetric breakdown with a relatively more uniform distribution of the electric field. This also reduces the noise due to band-to-band tunneling.

The performance of CMOS SPADs fabricated in relatively older nodes have minor spread. This is because of fabricating almost standard structure devices with shallow p-diffusions in an n-well, with p-doped guard-ring. Different structures were proposed in [37], [38], and [39] implementing a standard structure device. A reverse $n^+$/p-well structure was designed in [40] and [49]. The fill-factor of these devices were not satisfactory. [24] presented an STI-bounded SPAD, where shallow trenches are used as guard-ring in place of low-doped diffusion regions, thus shrinking SPAD dimensions down to 2$\mu$m. This improved the fill-factor in the SPAD array. [87] reported a scalable $n^+$/p-well diode, with deep n-well insulation. All these designs had noise issues. This is primarily due to the high doping concentrations and consequently high electric fields boosting tunneling and field-enhanced carrier generation effects. Also, the presence of shallow trenches increases the density of deep-level carrier generation centers at the

$Si/SiO_2$ interface, and the limited duration and effectiveness of annealing and drive-in diffusion steps do not help in reducing impurities, traps, and defect concentrations [41, 42, 54].

To diminish the aforementioned effects, new structures (especially in 130nm and 90nm technologies) were proposed. The STI was moved away from the active area by laying out dummy polysilicon [41]. In [43, 46, 48–50] two different methods were adopted. One is use of a virtual guard-ring to spatially separate shallow tranches from the high-field region. This prevents the injection of undesired carriers into the avalanche zone. The other one uses proper implant layers to create junctions where the electric field is lower. A p-type passivation is used around the STI to prevent carrier injection in [42, 44, 47]. Additionally, a lower n-well doping is used to reduce tunneling contribution.

## 2.5 Perimeter Gated Single Photon Avalanche Diode

SPADs fabricated in custom processes has better performance than CMOS SPADs. One of the performance reducing aspects of CMOS SPADs is the premature breakdown around the junction. This can be minimized by adding a polysilicon gate around the junction and applying voltage on it. This topic is explained more in detail in the next chapter.

## 2.6 Silicon Photomultiplier

Silicon photomultiplier (SiPM) is another type of photon detector and it is used in medical imaging, radiation detection, and high energy physics application. This detector is basically a collection of SPADs operating in Geiger mode. Figure 2.5 [55] show a very basic structure of SiPM built with perimeter gated SPADs for improved noise performance. Each diode must have a dedicated quenching resistance to maintain the whole operation cycle described earlier in this chapter. In this structure all the anodes are connected. Each cathode is connected to one and of the quenching resistance and another ends of quenching resistances are connected together. In this configuration all the cathodes must be isolated from each other.

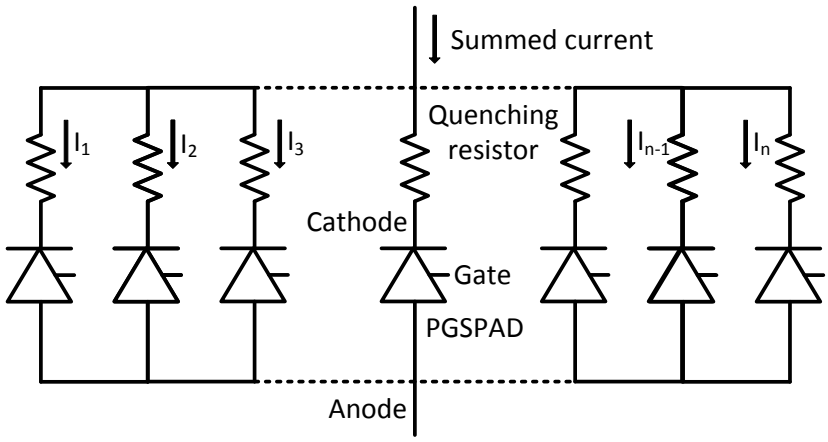



**Figure 2.5:** Basic structure of a silicon photomultiplier (SiPM). Each detector with quenching resistor can respond to an incoming photon. The summed current at the output is directly correlated with the light intensity.

The operating principle of this detector is based on current summing topology. If one photon creates avalanche in one diode, current flows through the branch having that diode for a short period of time. With the increase in number of photons, more SPADs go into avalanche and the value of the summed up current increases. So more photons mean more current. The total current gives a measurement of the properties of the incident light on the SiPM. For example, considering the neutron detection application, the incoming neutron can be converted to photons using a scintillation material. Then the photon can be measured using a SiPM. So, indirectly the neutron intensity can be measures using SiPM by knowing the conversion property of the scintillator. The SiPM has an analog current output whereas a SPADs output is more digital being an all or nothing signal.

## 2.7 Readout Techniques

Readout electronics is an indispensable part of the detection system whether a SPAD or an SiPM is used. The readout techniques varies with the detector and application. Integrating this essential part on the same chip is one of the main reasons why CMOS detectors are so popular. In this section different readout techniques are briefly discussed.

### 2.7.1 Photon Counting Based Readout

Using photon counting based readout, the number of avalanche events in each SPAD over a time span can be counted. If a single pixel has arrays of SPAD, only one counter can be used for all the arrays of a single pixel. An integrated timer can be added to measure the time of arrival. It is useful in various applications for detecting extremely weak light at the photon counting level. For SPAD arrays, different readout techniques have been proposed based on their application and limitation. Charbon proposed three different techniques in [56], (1) in-pixel, (2) in-column, and (3) on-chip counting or time of arrival (TOA) evaluation. In in-pixel architectures, operation are performed and stored locally. Random or sequential access techniques are used to read the values back. This is done in column-by-column basis on case for in column technique. On-chip counting or TOA is an extension of the in-column architecture. In this case the whole chip is a single cluster. Figures 2.6, 2.7 and 2.8 were proposed in [56].

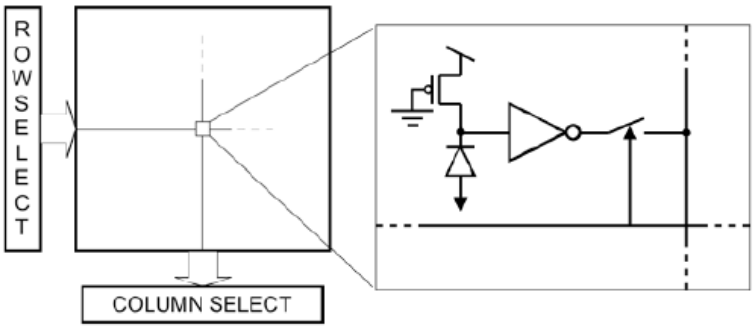



**Figure 2.6:** Block diagram and pixel schematic of a SPAD array with random access readout [58].

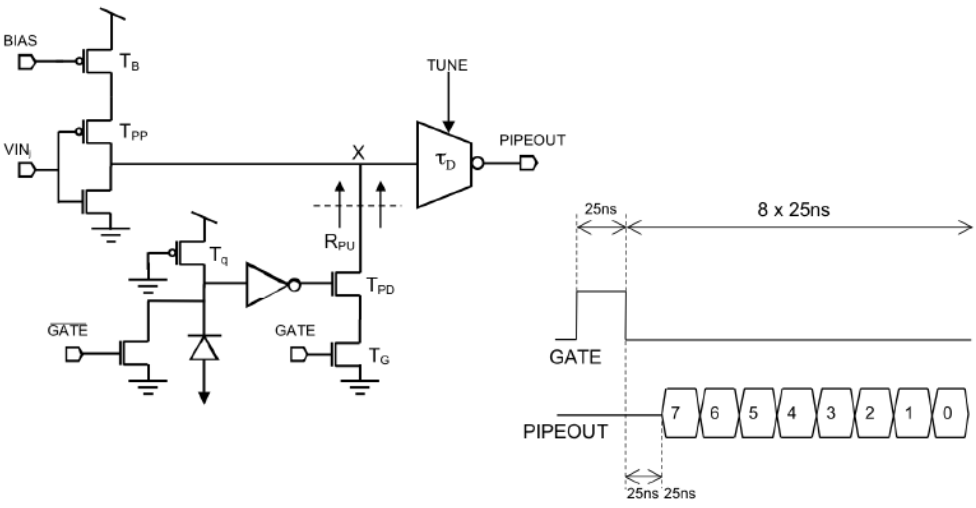



**Figure 2.7:** Schematic diagram of a latchless pipelined readout [58].

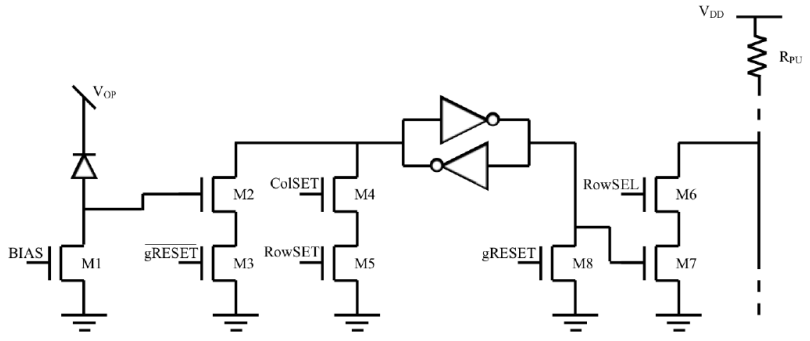



**Figure 2.8:** Schematic diagram of a pixel with embedded 1-bit counter [58].

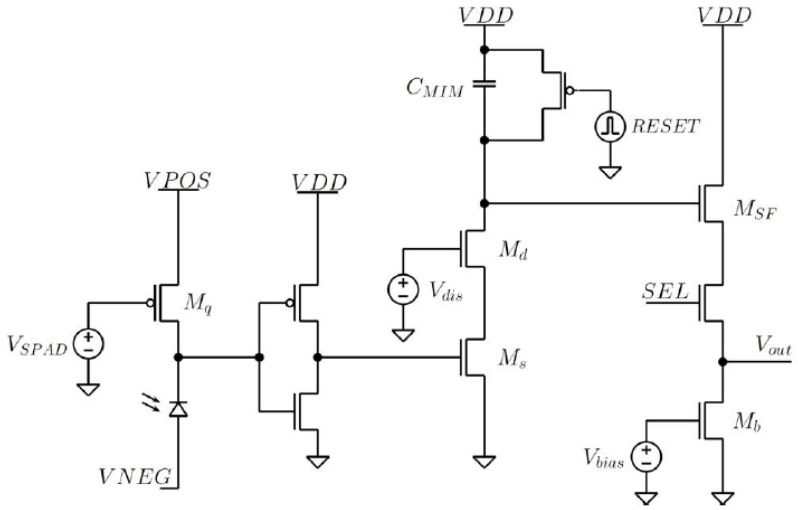



**Figure 2.9:** The pixel circuits that generate an output that is proportional to the number of detected photons [59].

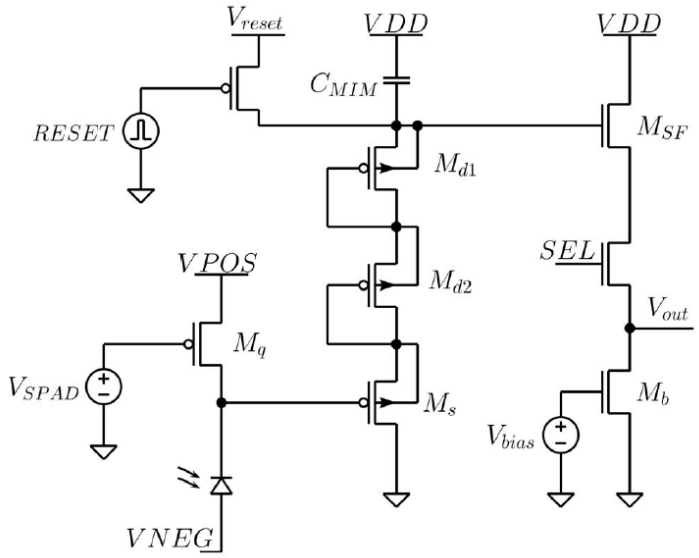



**Figure 2.10:** Logarithmic pixel circuit [59].

Chitnis *et al.* reported a few readout techniques for SPAD arrays [57]. The linear pixel technique shown in Figure 2.9 converts the number of pulses to an analog voltage. For increasing the dynamic range they also proposed a logarithmic pixel shown in Figure 2.10. Guerrieri *et al.* proposed a readout techniques using counter and latches for a two dimensional SPAD array [35]. After each photon ignition the avalanche is quenched swiftly. Readout electronics increment the 8-bit counter for each photon initiated event.

A counter technique is one of the most used readout techniques for SPAD arrays. Pancheri *et al.* and Panini *et al.* proposed almost similar counter techniques [58, 59]. Both of these techniques use a gating circuit block in the readout. Therefore, in these techniques the detectors are not free-running. The free-running detectors are always ready for detection while properly biased. But the non free-running (gated) detectors need 'enable' pulses for activating the detector for detection.

### 2.7.2 Current Sampling Based Readout

This technique is suitable when the light has a relatively steady level. The SiPM current is directly measured, and the readout circuit actually works as a picoammeter. SiPM readout using the continuous current method is preferable when a steady light signal is available for a long period. Brightness variations of the light are measured by sampling the SiPM's output current over a suitable interval. Averaging the samples reduces the low frequency noise.

### 2.7.3 TIA Based Readout

A transimpedance amplifier (TIA) can be used to transform the summed up current into voltage to better measurement. While determining the DC operating range of the amplifier, it is considered that all the pixels will be fired at the same time, and contribute to the summed current [55]. While designing the capacitance of the device have to considered since it can affect the bandwidth of the amplifier.

## 2.8 Figures of Merit

The application of the SPAD based detectors can be divided in there major groups: (1) photon- counting, (2) photon-timing and (3) photon imaging. The intensity of slowly varying ($\mu$s range) optical signal is measured in photon-counting applications, whereas very fast (ps range) optical waveforms are reconstructed in photon-timing applications [54]. For this two types of application one or few dozen detectors are user but for imaging application an array of hundreds of detectors are required and that is why the pixel pitch and fill-factor have huge importance in imaging application [54].

Signal-to-Noise Ratio (SNR) and Dynamic Range are commonly reported as the figure of merits for photon counting application. [60] reported SNR of SPAD as:

$$SNR = \frac{S}{\sqrt{S+N}} = \frac{PDE \,.\, \Phi_S \,.\, T_{INT}}{\sqrt{PDE \,.\, \Phi_S \,.\, T_{INT} + DCR \,.\, T_{INT}}} \tag{2.4}$$

where Photon Detection Efficiency ($PDE$) is defined as the ratio of the number of detected photons and the number of photons incident on the active area [54]. This ratio depends on absorption probability and on triggering efficiency [60], $\Phi_S$ is the signal photon-rate and $T_{INT}$ is the integration time employed to count photons. So equation 2.4 can also be represented as:

$$SNR = \frac{MCR - DCR}{\sqrt{MCR}} \tag{2.5}$$

where $MCR$ is total measured count rate and $T_{INT}$ =1s.

Dynamic range is defined as the ratio between maximum $S_{max}$ and minimum $S_{min}$ detectable signals [54]:

$$Dynamic\ range = \frac{S_{max}}{S_{min}} \tag{2.6}$$

Dynamic range is also reported in dB using the following equation:

$$Dynamic\ range = 20 \log_{10} \frac{S_{max}}{S_{min}} \tag{2.7}$$

A figure of merit ($\mathrm{FoM}_C$) is reported in [54] considering device parameters i.e. efficiency ($PDE$), noise ($DCR$), maximum achievable photon flux ($S_{max} = \Phi_{max} \times T_{INT}$), dead time ($T_{Dead}$) and active area ($A_{Active}$):

$$FoM_C = PDE \times \frac{\sqrt{A_{Active}}}{\sqrt{DCR}} \times \frac{1 - P_{AP}}{T_{Dead}} \tag{2.8}$$

where $T_{INT}$ =1s.

For photon-timing application the figure of merit is described as:

$$FoM_T = \frac{FoM_C}{FWHM} \tag{2.9}$$

where FWHM is Full-Width at Half Maximum of the distribution histogram of the statistical spread of output pulse on-set compared to the true photon arrival time [54].

SPADs are the building blocks of SiPMs. So, SiPM microcell could be treated as an individual SPAD. $\text{FoM}_C$ and $\text{FoM}_T$ defined earlier can be used when considering the performance of the individual microcell. The microcell PDE is obtained by dividing the SiPM PDE by fill-factor [54]. The geometrical losses are taken into account while reporting the PDE in the SiPM datasheets. The microcell area is computed by multiplying the total SiPM area by the fill-factor which gives the total active area and by dividing the result by the number of microcells [54]. The DCR of the SiPM can be divided by the number of microcell to calculate the DCR of the microcell. In large SiPMs the overall noise is affected by hot-pixels and crosstalk [60]. So, the median DCR of a SiPM microcell can be lower than the total DCR divided by the number of microcells [54].

Performance wise, custom SPADs are far ahead of CMOS SPAD. One of the main goal of this research is to make the gap narrower. But one of the advantages of CMOS SPADs is the monolithic integration of 2D array of SPADs with necessary readout electronics. This advantage helps in designing imager for either 2D, 3D imaging.

A figure of merit for SPAD based imagers ($\mathrm{FoM}_I$) was reported in [54] considering account efficiency, noise, fill-factor ($FF$), number of pixels ($N$), maximum frame-rate ($f_{max}$), and maximum count rate (considering $T_{INT} = 1\mathrm{s}$) [54]:

$$FoM_I = PDE \; . \; \frac{\Phi_{max}}{\sqrt{DCR}} \; . \; FF \; . \; N \; . \; f_{max} \tag{2.10}$$

These figures of merit helps in comparing SPADs fabricated in different technology nodes and provide ideas about how parameters affect the performance for different application.

# Chapter 3

# CMOS Perimeter Gated SPAD Characterization

** **Portions of this chapter were published in:**

M. H. U. Habib, F. Quaiyum, S. Islam, N. McFarlane, *"Optimization of Perimeter Gated SPADs in a Standard CMOS Process,"* IEEE Sensors Conference, 2-5 Nov. 2014.

## 3.1 Introduction

There are a number of strategies to mitigate premature perimeter breakdown in single photon avalanche diodes fabricated in CMOS processes. In a twin-well CMOS process, lateral diffusion of donor atoms following n-well oxidation creates a lighter n-doped region at the edge of the p-n junction. This increases the breakdown voltage around the perimeter and prevents premature breakdown [20]. Incorporation of a field-limiting guard ring at a distance from the implant and a gate placed on top of the gap have also proven effective in reducing premature breakdown [21]. However, use of a guard ring reduces the fill-factor, and is therefore not always an ideal option [18, 21]. The combination of lateral diffusion of n-wells and depletion gates have also been shown to reduce premature edge breakdown [20, 22]. All of these techniques are

based on modulation of dopant concentration and junction curvature effects on the breakdown voltage, and the effect of the gate on the high field regions [16, 23]. In deep-submicron CMOS technologies, use of shallow trench isolation (STI) to modify the junction geometry has been used to prevent edge breakdown [24]. Placement of a perimeter gate on top of the junction and application of the voltage on that gate are also effective ways of preventing premature breakdown while having a large fill-factor [18].

Perimeter gated single photon avalanche diodes (PGSPADs) with varying physical parameters were fabricated in a standard 0.5$\mu$m, 2-poly, 3-metal CMOS process, and the effect of gate voltage, excess bias, size of junction, junction shapes, and junction types on the device characteristics have been investigated. These characteristics include breakdown voltage and the optical response.

## 3.2 Theory

The current-voltage characteristic of a p-n junction diode contains three regions of operation, forward, reverse, and breakdown regions as discussed earlier. To operate in Geiger mode, the device is reverse biased at a voltage above the breakdown voltage. An incoming photon frees charge carriers by supplying enough energy.

The carriers are then accelerated due to the high reverse electric field. These carriers undergo impact ionization in the depletion region creating a self-sustaining

avalanche of carriers [61,62]. The avalanche gain, $M$, or the multiplication factor can be expressed as,

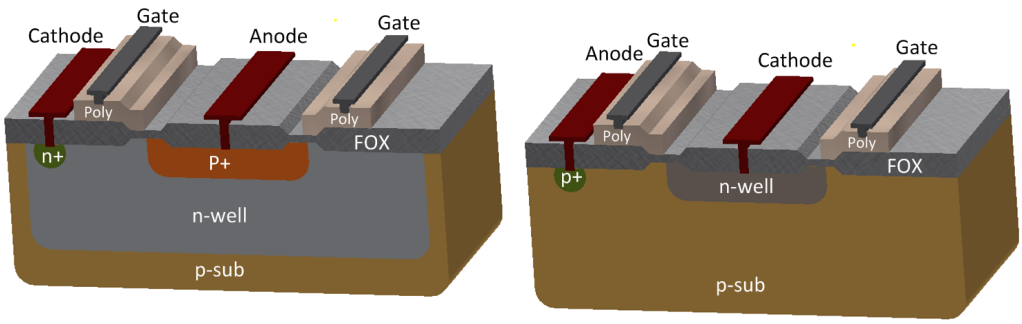
$$M = \{1 - \int_0^{W_D} \alpha_n e^{-\int_0^{W_D}(\alpha_n - \alpha_p)dx} dx\}^{-1} \tag{3.1}$$

where, $W_D$ is the depletion-layer width, and $\alpha_n$ and $\alpha_p$ are the electron and the hole ionization rates, respectively [62]. For $\alpha_n = \alpha_p = \alpha$ , the gain equation reduces to the simple form,

$$M = \frac{1}{1 - \alpha W_D}. \tag{3.2}$$

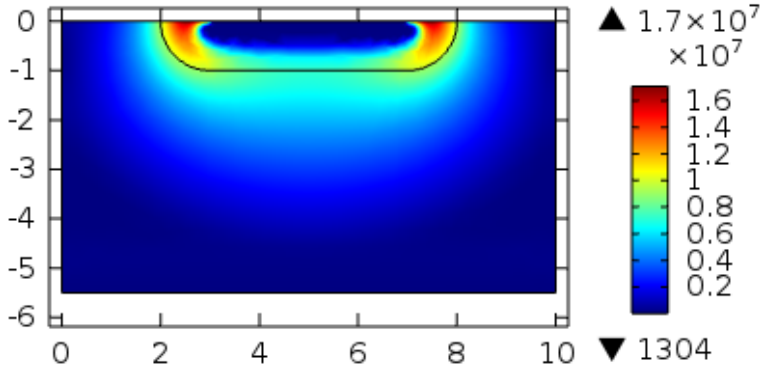
Breakdown corresponds to the situation when $\alpha W_D = 1$ [27].

Figure 3.1 shows the general cross-sectional views of the designed devices with an nwell-p$^+$ junction and a psub-nwell junction. In this figure, FOX is the field oxide and Poly is the polysilicon gate of the device. Application of a voltage to these gates prevent premature breakdown [4, 17, 18]. When a high electric field is applied across the device, the electric field around the junction edges are at a maximum,

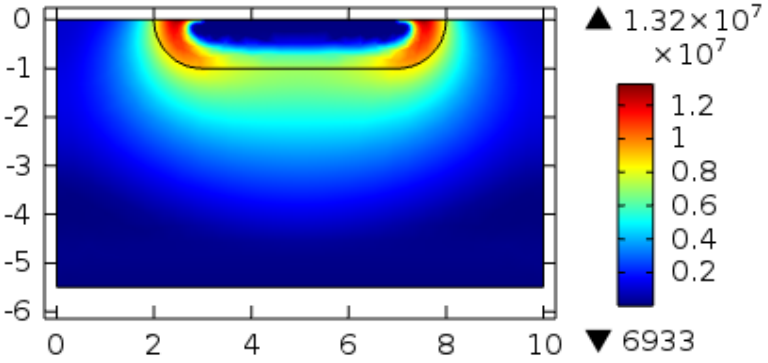



**(a)** **(b)**

**Figure 3.1:** Cross sections of (a) nwell-p$^+$ PGSPAD and (b) psub-nwell PGSPAD.




**(a)**

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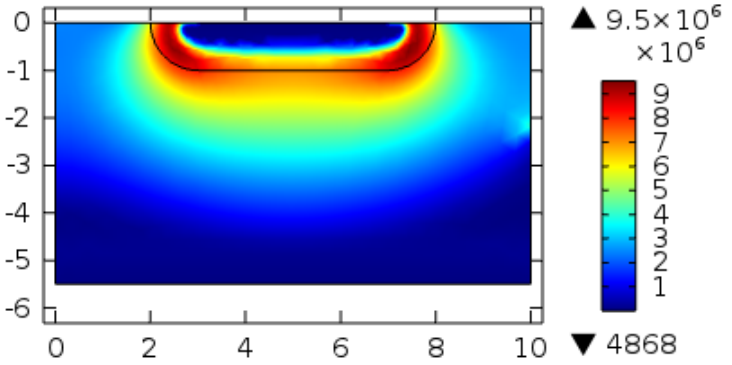



**(c)**

**Figure 3.2:** Simulation of electric field distribution modulation with a gate voltage magnitude of (a) 0V, (b) 5V, and (c) 10V. (x-axis and y-axis are in $\mu$m and colormap is in $Vm^{-1}$). The gate voltage makes the electric field more uniform around the junction and lowers the overall field.

thus reducing the active area of the device. Early breakdown can be suppressed. By applying a voltage on top of the junction through the polysilicon gate [4, 5, 18]. The breakdown voltage of the device is one of the key parameters in this study. Previous studies have shown that the breakdown voltage has a dependency on the doping concentration and impurity gradient [63–65]. The dependency of breakdown voltage on doping concentration can be expressed as [65],

$$V_{Br} = \frac{\epsilon_S E_{crit}^2}{2eN_B} \tag{3.3}$$

Where, $E_{crit}$ is the critical electric field at breakdown, $V_{Br}$ is the breakdown voltage, $e$ is the charge of an electron, $N_B$ is the doping concentration of the lightly doped region, and $\epsilon_S$ is permittivity. The addition of the perimeter gate and applying voltage on it increases the breakdown voltage by modulating the overall carrier concentration. Device simulation was performed to confirm the effect of the applied gate voltage on the electric field. Figure 3.2a shows the electric field distribution when 0V is applied at the gate terminal of a 2D model. The electric field distribution is maximum at the edges. Thus, this region will breakdown before the rest of the junction. Application of a gate voltage bias, (Figure 3.2b and Figure 3.2c), decreases the electric field at the edges, creating a more uniform electric field distribution. Thus, the entire region will breakdown at the same time.

## 3.3 Fabricated Devices

Eight PGSPADs were fabricated with varying size, shape and junction type in a standard 2-poly, 3-metal CMOS $0.5\mu m$ process. Devices were designed with areas of $22 \times 20\mu m^2, 70 \times 70\mu m^2$, and $110 \times 110\mu m^2$. Based on the active area, the sizes are referred as 'small', 'medium', and 'large'. The fabricated devices were square, octagonal and circular in shape. Two different junctions were used, psub-nwell junction and nwell-$p^+$ junction. For the psub-nwell devices, an nwell was created in the substrate. Necessary contacts were placed for connection. A gate of polysilicon was placed around the junction created by the nwell and substrate. The gate voltage was applied to this polysilicon gate to modulate the breakdown voltage. For nwell-$p^+$ devices, a p-diffusion was placed inside the nwell and the junction between the nwell and the diffusion was used as the junction of interest. A polysilicon gate was placed as described to modulate the breakdown voltage of this junction. Figure 3.3 shows the photomicrographs of the fabricated devices with three different shapes (square,

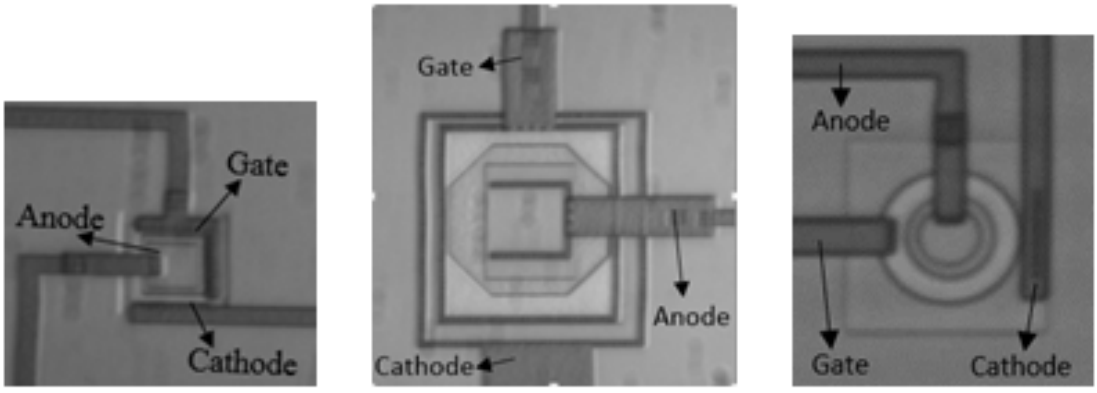



**Figure 3.3:** Photomicrographs of fabricated PGSPADs (square, octagonal and circular).

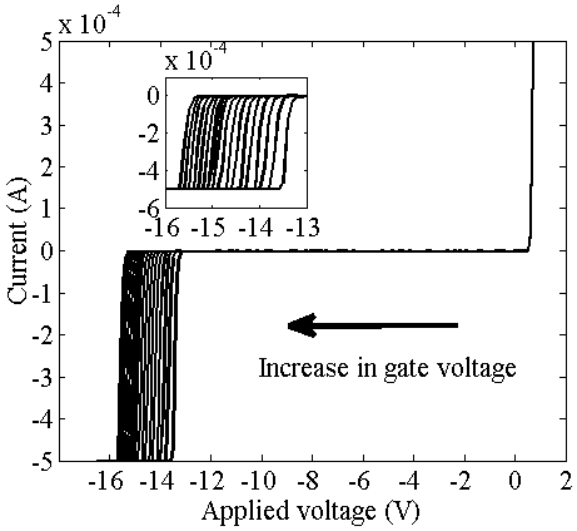
octagonal, and circular). The shapes are varied to explore the effect of the electric field distribution around the junctions. Different shapes having different electric field distributions show different breakdown voltage values and different noise responses.

## 3.4 Experimental Results

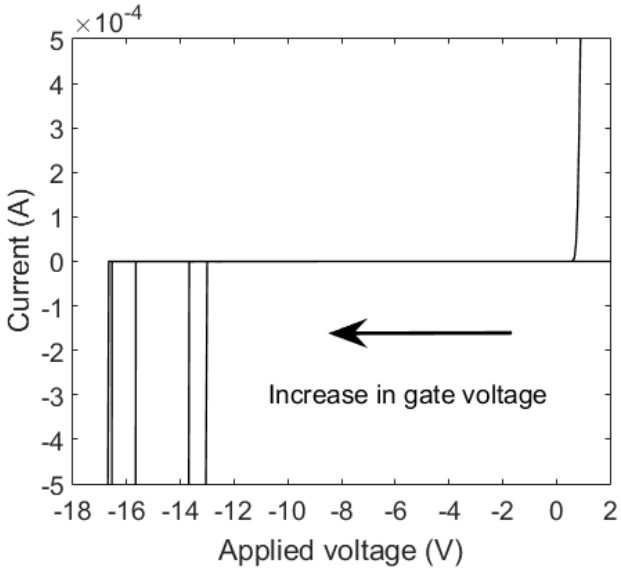
The current-voltage (I-V) characteristic was experimentally measured as a function of the excess bias voltage and the applied gate voltage for all fabricated PGSPADs. Additionally, devices were optically characterized under varying incident light power intensities to quantify the sensitivity and the effects of excess bias and the gate bias. Three chips are tested and the average response is reported here.

### 3.4.1 Breakdown Characteristics

The effect of the voltage applied to the polysilicon gate of the fabricated device was studied. From equation (5.3), it is seen that the breakdown voltage of the device depends on the electric field. This applied voltage at the polysilicon modulates the electric field (Figure 3.2), and the change in electric field distribution results in a change in breakdown voltage. The I-V characterization with a sweep of the gate voltage was performed for each PGSPAD. The gate voltage does not have any effect on the forward bias, but in the reverse bias the magnitude of the gate voltage shifts the breakdown voltage. Two Keithley 2400 source-measure-units (SMU) were used for the I-V characterization. The voltage between the anode and the cathode was swept




**(a)**




**(b)**

**Figure 3.4:** Experimental and simulated data showing the prevention of premature edge breakdown by increasing the voltage at the perimeter gate: (a) IV characteristic of one of the fabricated small nwell-$p^+$ square shaped PGSPAD. Inset shows the reverse bias region. (b) Sentaurus simulated IV characteristics showing the change in breakdown voltage with increase in applied gate voltage.

using one SMU and the voltage on the control gate was swept using another SMU. Figure 3.4 shows the I-V characteristics for one of the devices, and is typical of all devices measured. The change in breakdown voltage was simulated using Sentaurus device simulator. Figure 3.4b shows the results from the device simulation, and has good agreement with the experimentally measured data. The doping profile model of reference [4] was adopted in the simulation. The peak concentration in $p^+$ and $n^+$ regions used in the simulation is $\approx 1 \times 10^{22} cm^{-3}$ with a Gaussian distribution. $\approx 8 \times 10^{19} cm^{-3}$ and $\approx 1 \times 10^{17} cm^{-3}$ were used for the n-well and p-substrate respectively. The voltage at the knee of the I-V curve, in the reverse region, is the breakdown voltage. The knee is the point where the rate of change in current with respect to the applied voltage is at a maximum. The gate voltage was varied from 0V to -8V in steps of 0.25V. Tables 3.1, 3.2 and 3.3 show the breakdown voltages for the fabricated PGSPADs with zero gate bias. The effects of size, shape and, junction type on the breakdown voltage are discussed in the following sections.

**Table 3.1:** Fabricated octagonal devices with different sizes.

| Name | Diode Type | Size | Breakdown Voltage (V) |
|---|---|---|---|
| PGSPAD7 | nwell-octagonal $p^+$ | Medium | 13.6 |
| PGSPAD8 | nwell-octagonal $p^+$ | Large | 11.75 |
| PGSPAD3 | psub-octagonal nwell | Small | 22.3 |
| PGSPAD6 | psub-octagonal nwell | Medium | 20.3 |

#### 3.4.1.1 PGSPAD Characteristics as a Function of Size

Table 3.1 presents the effect of size on the breakdown voltage of the perimeter gated SPADs. Experimental results show that breakdown voltage decreases with increase in the device size. This is consistent with prior studies on the device size effect on the breakdown voltage and is included for completeness [66, 67]. Figure 3.5 shows the effect of the gate voltage on the breakdown voltages of the fabricated devices for varying sizes. Larger devices have lower breakdown voltage when 0V is applied to the gate. This is because of the non-uniform effect on a larger device due to relatively lower gettering efficiency for larger devices. However, increases in the gate voltage rapidly increase the breakdown voltage of the larger device close to the breakdown

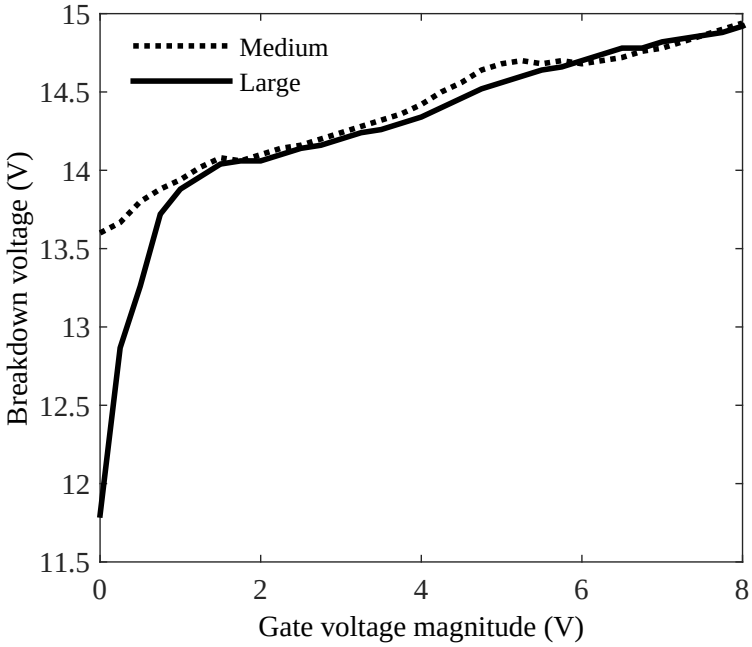



**Figure 3.5:** Gate voltage affecting the breakdown voltage of different sized devices.

voltage of a relatively smaller device. As shown in Figure 3.5, when the gate voltage is 0V, the difference in breakdown voltage of the medium and the large device is around 2V. But the gate voltage overwhelms the size effect when the magnitude is increased to 1V. Thus, the variation of breakdown voltage for different sizes can be corrected using a relatively smaller amount of gate voltage.

#### 3.4.1.2 PGSPAD Characteristics as a Function of Shape

The electric field is not uniformly distributed around the junction of the device. For this reason, the whole junction does not enter breakdown at the same time. The device will breakdown in the regions where the breakdown critical field is reached first. The electric field at the corners of the device reaches the breakdown value before other regions. This can be simply explained by corners of the edges having a higher concentration of electric field lines than straight edges. The chances of edge breakdown can be reduced by changing the shape of the device. Square, octagonal, and circular devices were fabricated to observe the variation in the breakdown voltage.

Table. 3.2 shows the breakdown voltage values for square, octagonal, and circular devices when the applied gate voltage is 0V. As the corner effect is stronger in a square

**Table 3.2:** Fabricated 'small' nwell-$p^+$ devices with different shapes.

| Name | Diode Type | Breakdown Voltage (V) |
|---|---|---|
| PGSPAD2 | nwell-square $p^+$ | 12.4 |
| PGSPAD4 | nwell-octagonal $p^+$ | 13.5 |
| PGSPAD10 | nwell-circular $p^+$ | 14.8 |

device, the electric field distribution is highly non-uniform. So the maximum value of electric field reached the critical value for breakdown at a relatively lower reverse voltage compared with the octagonal and the circular PGSPADs. So the breakdown voltage is less for the square device. But, as corner effect reduces for the octagonal device, it show a higher breakdown voltage than the square one. The electric flied distribution is more uniform than the other two shapes for the circular device. As a result of which it shows the highest breakdown voltage amongst these three differently shapes devices. Since the non-uniformity of electric field and premature breakdown phenomena are more prominent in square device, the perimeter gated technique should display stronger effect for square device than the circular device.

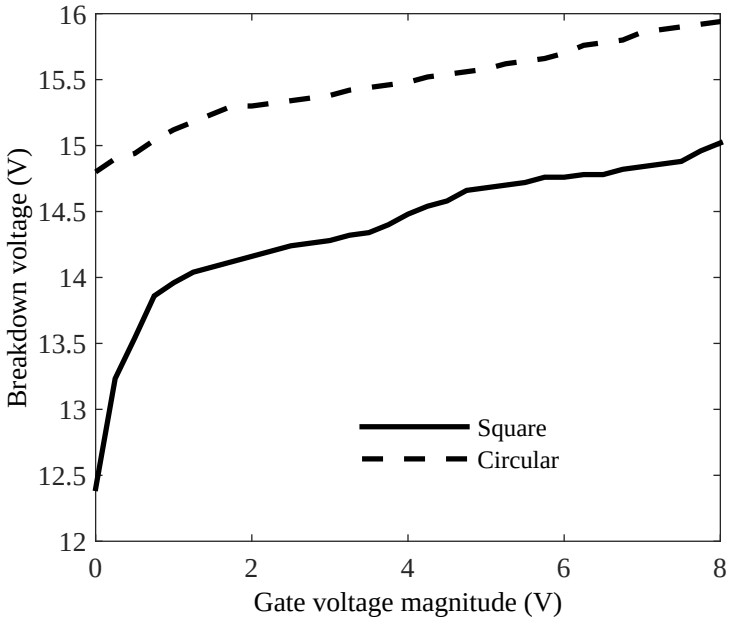



**Figure 3.6:** Breakdown voltage vs applied gate voltage for different shapes (small nwell-$p^+$ junction). The more dominant premature edge breakdown in the square shaped device is prevented by using the perimeter gated technique.

The experimental values in Figure 3.6 shows the expected change in the breakdown voltage with the change in applied gate voltage. For a gate voltage magnitude range of 0-8V, a change of 2.5V in breakdown voltage is seen, where the change for the circular device is around 1V. Most of the non-uniformity for the square device is corrected withing a gate voltage magnitude of 1V. Though the breakdown voltage of the square device increases it cannot fully reach the performance of circular device, and that is why even at higher gate voltages the circular device has higher breakdown voltage than the square one. Therefore, increasing the corner angles reduces the corner effects and a change in breakdown voltage is observed [61].

#### 3.4.1.3 PGSPAD Characrteristics as a Function of Junction Type

From Table. 3.3 and Figure 3.7, it is clear that the junction type plays a role in the breakdown voltage. This result is in accordance with equation's 5.3 well known results, due to the difference in doping concentrations of the layers. All devices with the psub-nwell junctions have relatively higher breakdown voltages, while devices with the nwell-$p^+$ junctions have relatively lower breakdown voltages. In Figure 3.7a, the breakdown voltage as a function of the gate voltage is increased from 13V to 23V for the (p-type bulk) psubnwell (PGSPAD3) junction instead of the $p^+$-nwell (PGSPAD4) junction. If the doping concentration of the relatively lightly doped region increases, the breakdown voltage decreases and vice versa. Figure 3.7b and Figure 3.7c show similar results for different shaped devices.

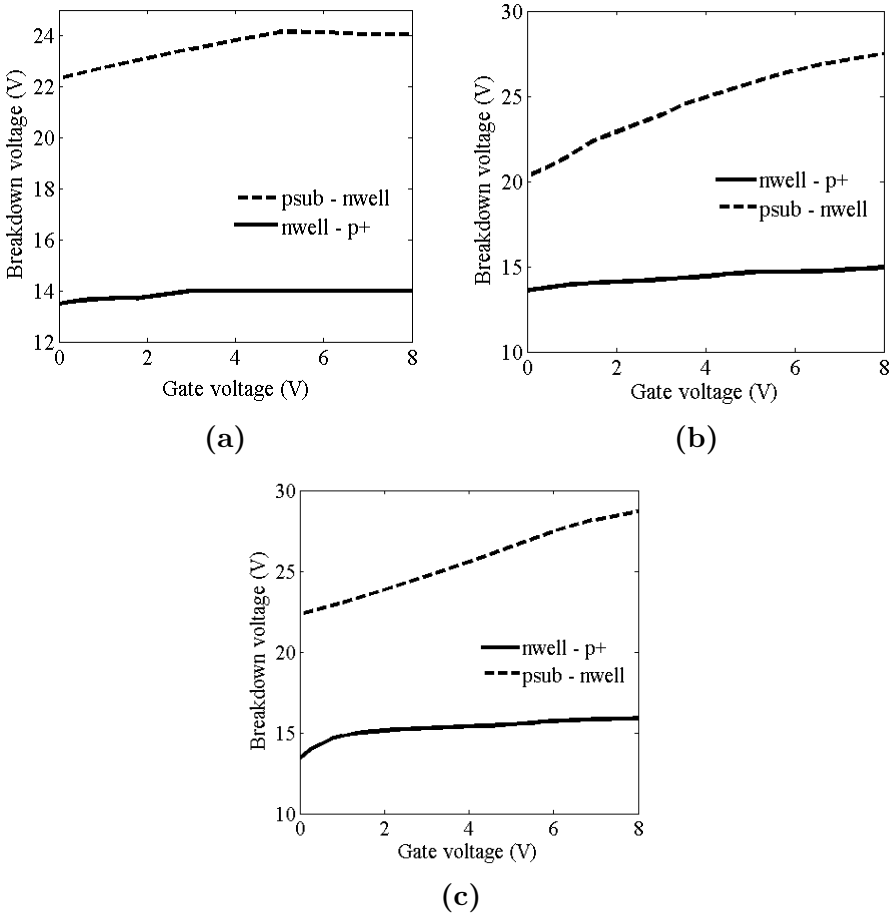



**Figure 3.7:** Breakdown voltage vs applied gate voltage for different junction type: (a) small octagonal junction, (b) medium octagonal junction, (c) small circular junction.

**Table 3.3:** Fabricated devices with different junction types.

| Name | Diode Type | Size | Breakdown Voltage (V) |
|---|---|---|---|
| PGSPAD3 | psub-octagonal nwell | Small | 22.3 |
| PGSPAD4 | nwell-octagonal $p^+$ | Small | 13.5 |
| PGSPAD6 | psub-octagonal nwel | Medium | 20.3 |
| PGSPAD7 | nwell-octagonal $p^+$ | Medium | 13.6 |
| PGSPAD9 | psub-circular nwell | Small | 22.3 |
| PGSPAD10 | nwell-circular $p^+$ | Small | 13.4 |

The rate of change of the breakdown voltage with the gate is less for the psub-nwell devices compared to the nwell-$p^+$ devices. Moreover, the change in breakdown voltage for different junction type is also visible from simulated IV characteristics presented in Figure 3.4b and Figure 3.6. From simulation, it is observed that the breakdown voltage is almost 6V higher for psubnwell devices compared to the nwell-$p^+$ devices.

### 3.4.2 PGPSAD Characterization: Optical Response

The optical sensitivity of the devices was experimentally measured by varying the optical power from $0.047\mu W/cm^2$ to $28.95\mu W/cm^2$. The optical power was measured using an optical power meter coupled with an integrating sphere. The optical power was varied in twelve steps using commercial optical filters. A monochromatic light source was used in the test setup. As the spectral response of silicon is well known, the overall count rate as a function of optical intensity is focused on rather than the usual photon detection probability. Optical testing results for two different PGSPADs (PGSPAD2 and PGSPAD8) are shown in Figure 3.8a and Figure 3.8b. PGSPAD2 is

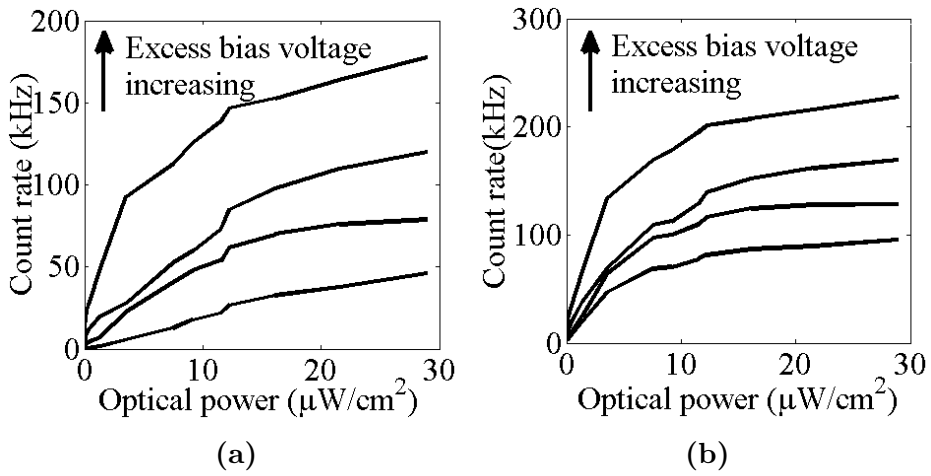



**Figure 3.8:** Count rate vs optical power for different excess bias: (a) small square nwell-$p^+$ junction, (b) large octagonal nwell-$p^+$ junction. Higher optical power means more photons and higher count rate. Excess bias increasing the count rate by increasing the avalanche probability.

a small device with square nwell-$p^+$ junction and PGSPAD8 is a large device with octagonal nwell-$p^+$ junction. In general, the count rate increases with optical power as expected. Increased optical power means more photon flux, resulting in more spikes (avalanche events followed by quenching). In all cases, the curves saturate at higher optical powers. This is most likely due to the finite dead time of the device, the time a PGSPAD takes to become ready to detect the next photon event after detection of a first photon as described in the previous chapter. The count rate increases with excess bias voltage (Figure 3.8). The noise floor also increases with excess bias. Since, the active area is higher for the larger device, the count rate values are higher for large device as expected.

Figure 3.9 shows the effect of the applied gate voltage on PGSPAD2 (nwell-square $p^+$, small) and PGSPAD8 (nwell-octagonal $p^+$, large). The gate voltage magnitude was varied from 0V to 6V in 1V increments. Increase in the gate voltage magnitude

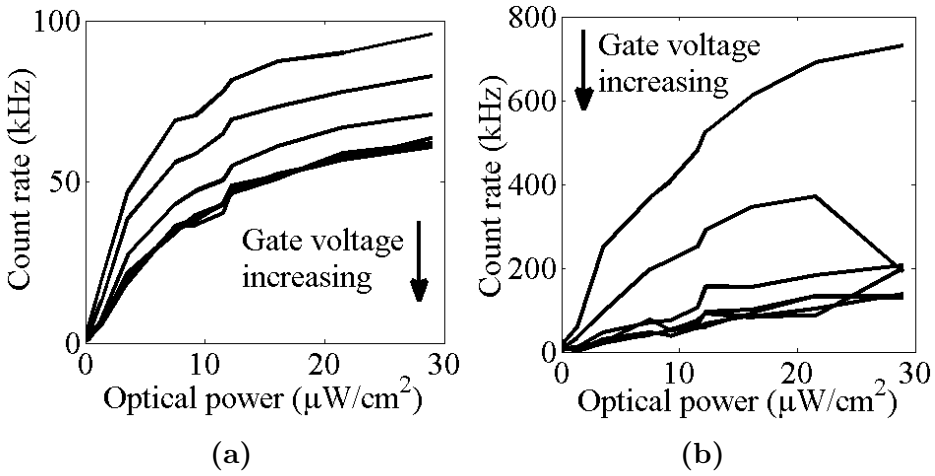



**Figure 3.9:** Count rate vs optical power for different gate voltages: (a) small square nwell-$p^+$ junction, (b) large octagonal nwell-$p^+$ junction. Increasing the gate voltage decreases the count rate by reducing the noise (DCR).

decreases the sensitivity of the device. The sensitivity of the device is defined as the rate of change in the count rate with respect to optical power of the incident light. In the optical power range of $0\mu W/cm^2$ - $3.5\mu W/cm^2$, PGSPAD2 has a sensitivity of $14.31kHz/\mu Wcm^{-2}$ for a gate voltage of 0V and $5.76kHz/\mu Wcm^{-2}$ for a gate voltage magnitude of 6V. PGSPAD8 has a sensitivity of $74.28kHz/\mu Wcm^{-2}$ for a gate voltage of 0V. The count rate for the same optical power also decreases with the increase in the gate voltage. However, the gate voltage decreases the noise floor which increases the overall signal to noise ratio. Beyond 3V, the change in the gate voltage has negligible effect on the count rate. The increase in count rate in the larger device is observed in this study as well.

## 3.5 Conclusion

Over the years, SPADs have shown significantly great promise for the detection of weak optical signals. PGSPADs enhance the performance of the SPADs by preventing premature perimeter breakdown. In this chapter, the breakdown voltage and optical response characteristics of PGSPADS with varying size, shape, and junction type as a function of applied gate bias and excess bias voltages were experimentally characterized. The exact choice of PGSPAD is dependent on the specific application. For instance, the intensity of the photon flux for detection of radiative particles, such as neutrons, is dependent on the scintillation material, which may be of varying efficiency. The experimental data and the physical device simulation results described in this work, offer guidelines for device structure and operating conditions for a given application. Although this study is performed in a relatively large process, the results should translate to submicron processes. STI in submicron processes results in poor performing SPADs and there are a few techniques to mitigate its effects in commercial processes [68]. Thus, the effects of applied gate voltages will have similar outcomes in smaller process.

# Chapter 4
# Modeling and Simulation

** **Portions of this chapter were published in:**

1. M. H. U. Habib, F. Quaiyum, K. A. A. Mamun, S. K. Islam, and N. McFarlane, *"Simulation and Modeling of Single Photon Avalanche Diodes,"* International Journal of High Speed Electronics and Systems, vol. 24, no. 03n04, 1520006-1-9, Oct. 2015.

2. M. H. U. Habib, K. A. Al Mamun, and N. McFarlane, *"A SPICE Model for Perimeter-Gated Single Photon Avalanche Diode,"* IEEE International Midwest Symposium on Circuits and Systems, 3-6 Aug. 2014.

3. M. Dandin, M. H. U. Habib, B. Nouri, P. Abshire, and N. McFarlane, *"Characterization of Single-Photon Avalanche Diodes in a 0.5μm Standard CMOS Process-Part 2: Equivalent Circuit Model and Geiger Mode Readout,"* IEEE Sensors Journal, vol. 16, no. 9, pp. 3075-3083, May, 2016.

## 4.1 Introduction

Simulation, one of most important steps in any design process, predicts the design's behavior, within some acceptable margin of error, if realized. SPICE Models predicting the static and dynamic behavior of a PGSPADs have been previously reported [69, 70]. These models simulated the current-voltage profile of the PGSPAD

and the Geiger mode avalanche current response to a photon. It also had the feature of simulating the effect of the gate voltage ($V_G$) on the breakdown voltage ($V_{Br}$) of the PGSPAD. However, the model is limited in predicting the effect of the gate voltage on the inherent randomness of the physical processes underlying the device operation.

The avalanche process in a SPAD is triggered by photons incident on the active area ($A_{Active}$) of the device. The photon energy generates free carriers. When properly biased, the applied electric field moves the free carrier with high velocity resulting in impact ionization, which leads to an avalanche of carriers flowing through the high field region (also known as the multiplication region). In complete darkness free carriers are generated through other phenomena such as, carrier diffusion, thermal generation, and band-to-band tunneling [11, 28, 71]. The total number of avalanches initiated per unit time because of these effects is termed as the dark count rate (DCR) and is considered to be the noise of the device. These phenomena and their noise contribution must be considered in developing a comprehensive model.

Behavioral modeling, including dark count rate (DCR) and spectral responsivity, have been developed for regular SPADs without the gate [71]. The model improved here to simulate the statistical behavior of the PGSPAD. The model predicts the effect of $V_G$ on the noise (DCR), and simulates the spectral profile of the device. The simulation of the DCR for different excess bias voltage, $V_{Exc}$, the difference between the applied reverse bias voltage ($V_R$) and the breakdown voltage ($V_{Br}$) of the PGSPAD is also included. The generation rate caused by diffusion, thermal generation, and band-to-band tunneling is included in the model. Additionally, empirical parameters

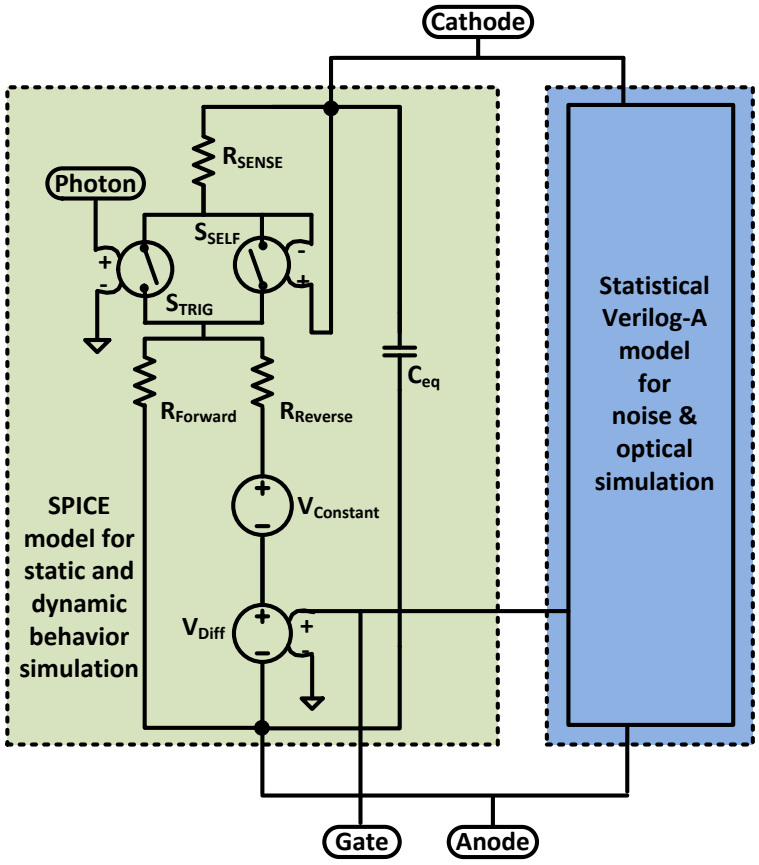



**Figure 4.1:** A complete model for PGSPAD simulation. PGSPAD has a gate terminal in addition to cathode and anode.

are extracted from experimental data to improve model accuracy. Figure 4.1 shows the block diagram of the complete model for simulating PGSPAD. The SPICE model block was reported in [70]. This statistical model completes the previous model and the model in Figure 4.1 simulates the static, dynamic, noise, and optical behavior of the PGSPAD.

## 4.2 SPICE Model for Static and Dynamic Simulation

Different modeling techniques for single photon avalanche diode have been reported over the years [12, 72–76]. Since SPAD is a diode the developed model is based on the model of a diode so it has a voltage source and resistor along with other devices [72, 73, 76]. The breakdown voltage modulation with gate voltage feature is added to this perimeter gated SPAD model.

As described earlier increasing the gate voltage magnitude increases the breakdown voltage. In the circuit representation of the model (Figure 4.1), there are two parallel branches for the device. One branch is for forward-biasing and the other is for reverse bias operation. The resistor values used in both the branches varies with the voltage between anode and cathode. The relationship between the resistors' values are empirically formulated from fabricated PGSPADs in 0.5$\mu$m standard CMOS process. In earlier literature, piece-wise linear models of the resistor were used, however we take a different approach in modeling this resistor [74]. The study of the relationship

from the collected data presents that an exponential function is best fitted to model the relation between the resistor value and the input voltages (Figure 4.2). The exponential fit, while not perfect, is an improvement over a piecewise linear fit reported earlier [70]. The exponential fit works with reasonable accuracy over the entire range, while the piecewise linear fit requires different segments for each gate voltage [70].

The effect of the gate voltage on the breakdown voltage is added by using voltage sources. The voltage sources are used only in reverse bias branch ,since the forward ON voltage is not affected by the gate. The empirical equation of the breakdown voltage, showing the relation between the breakdown voltage and the applied bias, has a constant term. An independent voltage source, $V_{Constant}$ (Figure 4.1), is introduced to represent this constant term. The non-constant portion of this equation is modeled with another voltage-controlled-voltage-source (VCVS) shown as $V_{Diff}$ in Figure 4.1. The incoming photon is simulated using a voltage-controlled-switch ($S_{TRIG}$) triggered with a pulsed voltage source [73]. Each single pulse represents a photon event in the model.

A current sustaining technique is used using a resistance ($R_{SENSE}$) and a a voltage controlled switch ($S_{SELF}$) [72, 73]. The quenching behavior of the PGSPAD is partly determined by the threshold value of this voltage controlled switch and the value of the sensing resistor. The equivalent capacitance ($C_{eq}$) of the device is extracted from the dynamic behavior of the device.

### 4.2.1 Parameter Extraction

Model parameters such as resistances, capacitance, voltage source, and threshold voltage of the voltage controlled switches are extracted using experimental data from PGSPADs fabricated in a 0.5$\mu$m CMOS process. The model parameters are different for devices with different sizes and shapes, however, the implemented models are identical in function type and circuit representation.

A dual DC I-V sweep analysis is used to determine the resistance values and breakdown voltages for different gate voltage. The voltage between anode and cathode is swept as primary and the gate voltage is swept as secondary. The exponential characteristic of resistance for one device is shown in Figure 4.2 is extracted from the

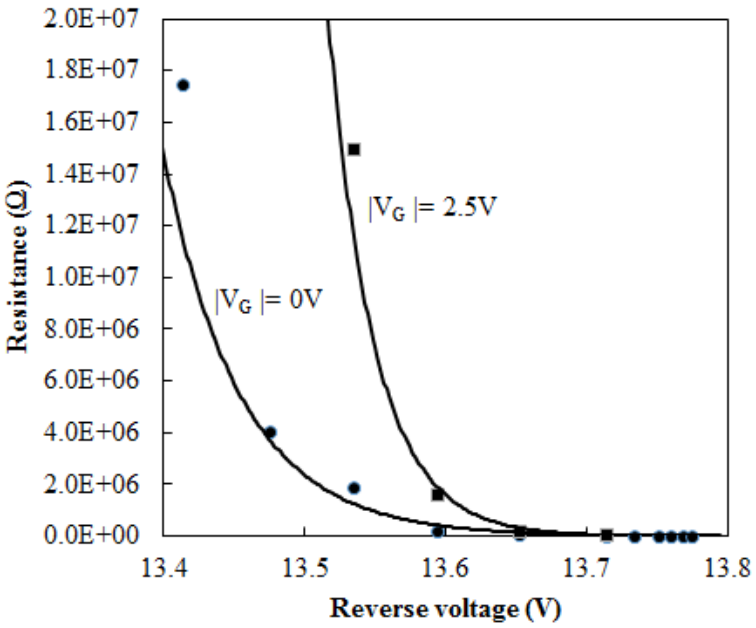



**Figure 4.2:** Exponential characteristics of PGSPAD. The solid lines are the fitting curves.

I-V curve. The secondary sweep yields the model of the voltage-controlled-voltage-source (VCVS) [70].

The dynamic properties of the device are used to extract the values of the sensing resistor, voltage-controlled-switches, and capacitor. The value of the avalanche current at which the quenching starts is determined experimentally. The value of the sensing resistance and the threshold voltage of the voltage-controlled-switch are calculated from that current value. This equivalent capacitance results from a parallel combination of the junction capacitance and the stray capacitance. The stray capacitance is the series combination of capacitances between cathode-substrate and anode-substrate [70, 73]. Zappa et al. showed that the junction capacitance has a dependency on the applied reverse bias voltage [70, 73]. But, in the range of interest for applied reverse bias voltage, the dependency of capacitance values on applied reverse bias voltage is negligible, thus a constant equivalent capacitance value ($C_{eq}$) is used in this model.

Equations 4.1 and 4.2 model the resistances. Where, A, B, C, D, Q, and R experimentally extracted constants, and $V_{CA}$ is the voltage between cathode and anode terminals (reverse voltage) of the device.

$$RSPAD_{REV} = Ae^{-B(V_{CA}+QV_G^2+RV_G)} \tag{4.1}$$

$$RSPAD_{FOR} = Ce^{-DV_{CA}} \tag{4.2}$$

### 4.2.2 Operating Principle of PGSPAD Model

For simulation, the model block is biased above the breakdown voltage. The switch $S_{TRIG}$ closes for a brief moment to simulate a photon incident and creates a path for current. So, current starts flowing through $R_{SENSE}$ develops a voltage across it to turn ON $S_{SELF}$ switch, and sustains the current even after $S_{TRIG}$ is open. For I-V simulation with the model two voltage sources are used. One for applying voltage between the anode and the cathode. The second voltage source is used to apply the gate voltage.

For dynamic simulation to look and avalanche, quench and reset as discussed in Chapter 2, a quenching technique is needed. For simplicity, passive quenching technique with a 100kΩ quenching resistor is adopted to validate the simulation and experimental measurements.

The voltage build-up across the quenching resistance due to the avalanche current reduces the voltage between the anode and the cathode of the PGSPAD. The Resistance $RSPAD_{REV}$ increases exponentially when the $V_{CA}$ starts going below breakdown resulting in an exponential reduction in current through $R_{SENSE}$. This reduction pulls the input voltage of the switch $S_{SELF}$ below the threshold and $S_{SELF}$ becomes open. PGSPAD returns to its normal state after the discharging of the parasitic capacitors.

## 4.3 Stochastic Model for PGSPAD

This model simulates not only the noise behavior, but also the spectral response of the device. The noise modeling and the spectral response modeling are discussed separately in following subsections.

### 4.3.1 DCR Modeling

PGSPAD noise or the dark count rate is due to avalanches occurring in the absence of light. If the device is biased above the breakdown voltage ($V_R > V_{Br}$), free carriers in the depletion region initiate impact ionization resulting in unwanted avalanches. Free carriers are generated as a function of temperature and this is knows as thermal carrier generation. In this phenomenon, the vibration of the atoms in the crystal lattice due to heat energy breaks the covalent bond and creates free carriers. The higher the temperature, the more free charge carriers are available for conduction. Band-to-band tunneling is another phenomenon by which free charge carriers can be generated. In band-to-band tunneling, electrons in the valence band tunnel across the potential barrier to reach the conduction band and generating free carriers. Minority carrier diffusion from the neutral region is another process of generating free carriers. Each generated carrier through any of the aforementioned processes has a finite, non-zero probability of initiating an avalanche. The carrier generation rate (CGR) for these processes are summed to derive the total carrier generation rate. However, the

diffusion current density due to excess minority carrier is typically 2 to 3 orders of magnitude smaller than the other processes and is ignored for this model [28, 71].

The DCR caused by thermally generated carriers can be calculated using the Shockley-Read-Hall equation [62, 77] and the net generation rate of thermally generated carriers is:

$$G = \frac{n_i^2 - pn}{\tau_e\left(p + n_i e^{\frac{-(E_t - E_i)}{kt}}\right) + \tau_h\left(n + n_i e^{\frac{(E_t - E_i)}{kt}}\right)} \tag{4.3}$$

where $\tau_e$ and $\tau_p$ are given by $\tau_i = \frac{1}{v_{th}\sigma_i N_t}$ $(i = e, h)$ where $\sigma_i$ is the capture cross section for the carriers and $N_t$ is the density of generation/recombination centers, $v_{th}$ is the thermal velocity. In the space charge region, the values of $n$ and $p$ are much lower than the intrinsic electron concentration $(n_i)$. So, if $n_i >> n$ and $n_i >> p$ and $\tau_i = \tau_e = \tau_h$, equation 4.3 becomes:

$$G \approx \frac{n_i v_{th} \sigma_i N_t}{2} \tag{4.4}$$

where $v_{th}$ is given by

$$v_{th} = \sqrt{\frac{3kT}{m^*}} \tag{4.5}$$

where $k$ is Boltzmann's constant, $T$ is the temperature, and $m^*$ is the carrier effective mass. For a device with active area $A_{Active}$ and effective thickness of the depletion

layer $W_D$ the the thermal carrier generation rate is

$$CGR_{Thermal} = G \times A_{Active} \times W_D \tag{4.6}$$

The carrier generation rate due to band-to-band tunneling can be calculated using the tunneling current equation [78–80]:

$$J = cqFV_R \exp\left(-\frac{F_0}{F}\right) \tag{4.7}$$

The values of $c$ and $F_0$ have been modeled differently in different study. R. B. Fair et al. [80] and G. Karve et al. [81] reported the following equation:

$$CGR_{BTBT} = \frac{\sqrt{2m^*}q^2FV_R}{4\pi^3h^2\sqrt{E_g}} \exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3qFh}\right)A_{Active} \tag{4.8}$$

Recently, in a SPAD model, the carrier generation rate due to band-to-band tunneling is calculated using the following equation [82],

$$CGR_{BTBT} = \frac{\sqrt{2m^*}q^2FV_R}{h^2\sqrt{E_g}} \exp\left(-\frac{8\pi\sqrt{2m^*}E_g^{3/2}}{3qFh}\right)A_{Active} \tag{4.9}$$

where $h$ is Plank's constant, $E_g$ is the silicon bandgap energy, $V_R$ is the reverse bias voltage, and $F$ is the average electric field in the depletion region. The average electric field, $F$, of a PGSPAD is modulated by the applied bias at the gate of the device.

Moreover, the breakdown voltage, $V_{Br}$, increases with the increased $V_G$. For a fixed excess bias, $V_R$ changes by the same amount as $V_R = V_A = V_{Br} + V_{Exc}$.

The relationship between $V_{Br}$ and $V_G$ has been experimentally verified using PGSPADs designed and fabricated in a standard CMOS process. Figure 4.3 shows relationship between $V_{Br}$ and $V_G$ used in this model. The effect of surface fields on the breakdown voltage of planer Silicon p-n junctions was described in [16] which established a linear relation between the breakdown voltage and the gate voltage. Based on this, a linear fitting of the experimental data has been adopted and incorporated into this model. Simulation using Sentauras shows that the average electric field decreases with increasing gate bias (4.4), but increases with the excess bias (Figure 4.5) (for a constant applied voltage).

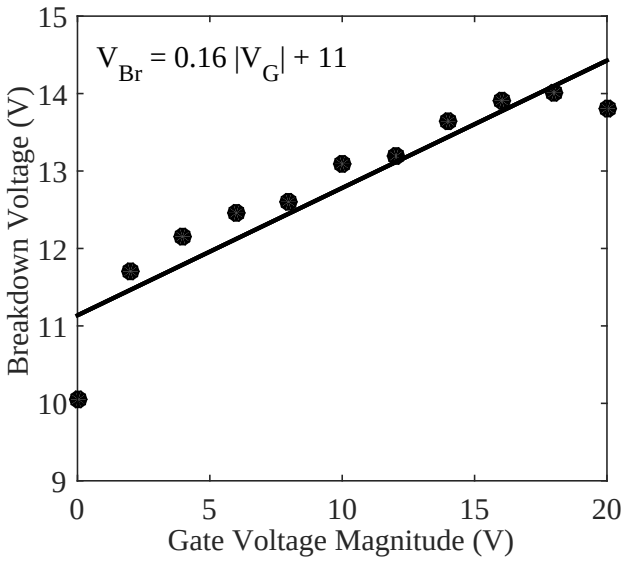



**Figure 4.3:** Breakdown voltage, $V_{Br}$, increases with increasing gate voltage $|V_G|$ for the PGSPAD.

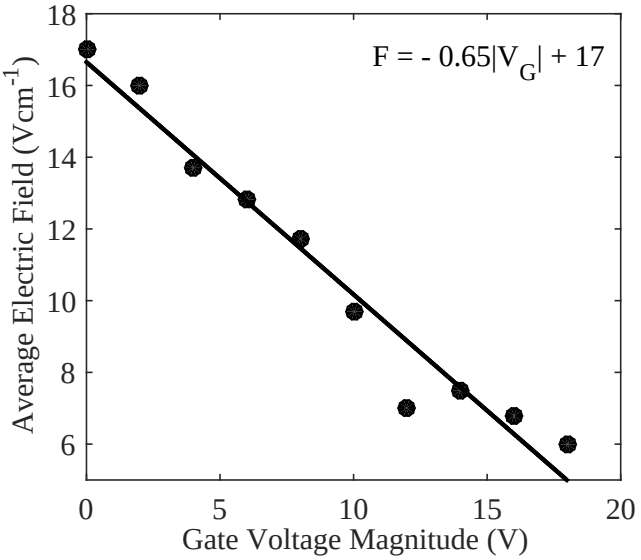



**Figure 4.4:** Average electric field, $F$, decreases with gate voltage, $|V_G|$.

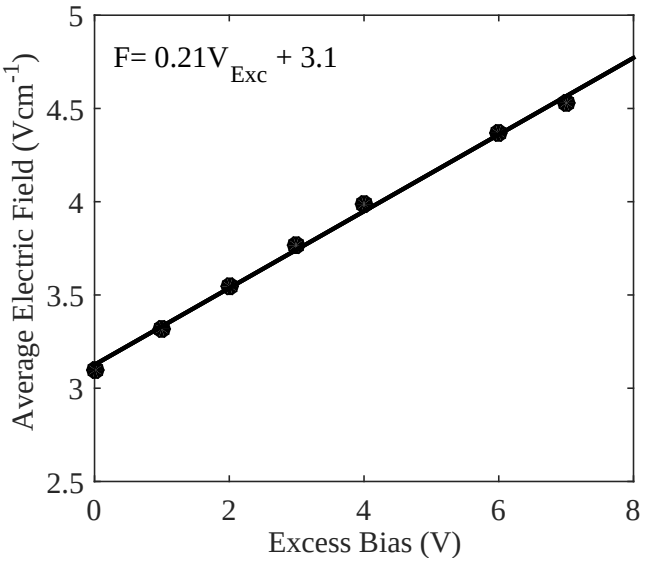



**Figure 4.5:** Average electric field, $F$ increases with $V_{Exc}$.

The probability that a generated carrier start an avalanche, ($P_{Av}$), is [71],

$$P_{Av} = \begin{cases} 0 & \text{for } V_{Exc} < 0 \\ 1 - e^{-\frac{V_{Exc}}{\eta_T V_{Br}}} & \text{for } V_{Exc} \geq 0 \end{cases} \tag{4.10}$$

where $\eta_T$ is an experimentally derived parameter. Since, the breakdown voltage is a function of the gate voltage, $P_{Av}$ is also a function of the gate voltage. The dark count rate is,

$$DCR = P_{Av} \times CGR \tag{4.11}$$

Thus, the gate bias affects the dark count rate through both the generation rate due to band-to-band tunneling and the probability of starting an avalanche. The parameters $n_i$, $E_g$ and $V_{Br}$ are the temperature dependent parameters. The temperature dependency is incorporated into the model using established theories [62, 83].

### 4.3.2 Spectral Response Modeling

The spectral response in the wavelength range 400nm-800nm is included in the model. The photon detection probability, PDP, the probability of detecting a single photon if it is incident on the active area is [84],

$$PDP(\lambda, \beta, P) = T_s(\lambda, \beta, P) \times QE(\lambda) \times PA \tag{4.12}$$

where $\lambda$ is the wavelength, $\beta$ is the angle of incidence at the sensor surface, $P$ is the polarization of the incident light, $T_s$ is the optical transmittance through the sensor's silicon surface, $QE$ is the quantum efficiency of the PGSPAD's depletion layer, and $PA$ is the probability of a photo-generated carrier initiating an avalanche.

$\beta$ and $P$ have been kept constant while collecting the experimental data. Moreover, considering that the probability of any generated carrier initiating an avalanche is the same, equation 4.12 can be simplified to,

$$PDP(\lambda) = QE^*(\lambda) \times P_{Av} \tag{4.13}$$

where $QE^*(\lambda) = T_s(\lambda) \times QE(\lambda)$. $QE^*$ values have been estimated from experimental measurement. Figure 4.6 shows the $QE^*$ profile of collected data for a wavelength range of 400nm-800nm.

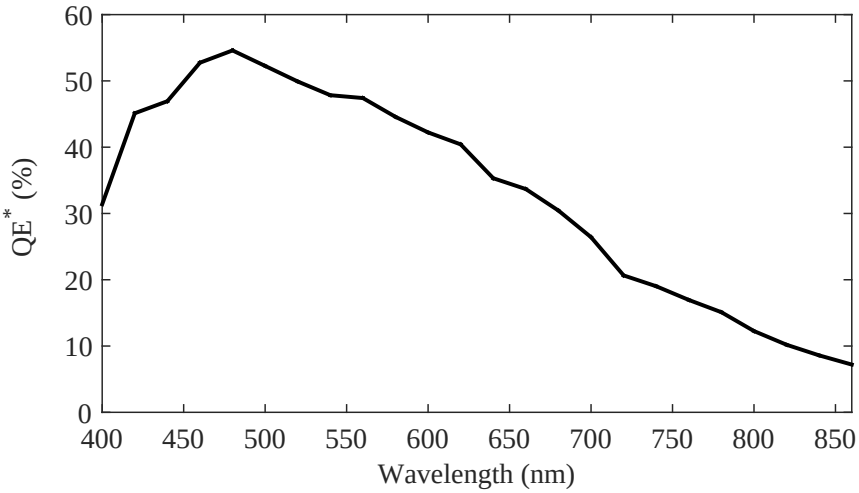



**Figure 4.6:** Effective quantum efficiency ($QE^*$) of the PGSPAD.

Afterpulsing is another probabilistic behavior inherent to SPADs. The phenomenon creates false counts by releasing carriers trapped in deep levels when $V_R > V_{Br}$ is within the dead time window. In [82], this phenomenon is modeled using a time depended probabilistic equation and then fitting the parameter values from experimental data. However, no afterpulsing was detected while testing the dynamic characteristics of our device. Therefore, afterpulsing modeling has been excluded from the scope of this model.

## 4.4 Results

The I-V characteristics, from the model simulation and experiment, are shown in Figures 4.7 and 4.8. The breakdown voltage and forward and reverse properties of the device extracted from the model simulation are in good agreement with the measured values. So, the breakdown voltages corresponding to different gate voltage values can be predicted using this model through simulation.

The effect of gate voltage in simulation is in good agreement with the experimental values. A voltage pulse of 1V with a width of 0.1ns is used to simulate the incident photon. Figure 4.9 and 4.10 present the accuracy of the dynamic behavior simulation. Using this model, the dead time of the device can be simulated before fabrication.

The simulation of the model has been performed in Cadence. The model is written in Verilog-A and a symbol created with required inputs (Anode, Cathode, Gate) and outputs ($DCR$, $DCR_{Thermal}$, $DCR_{BTTB}$, $P_{Av}$, $PDP$). This symbol has been used in

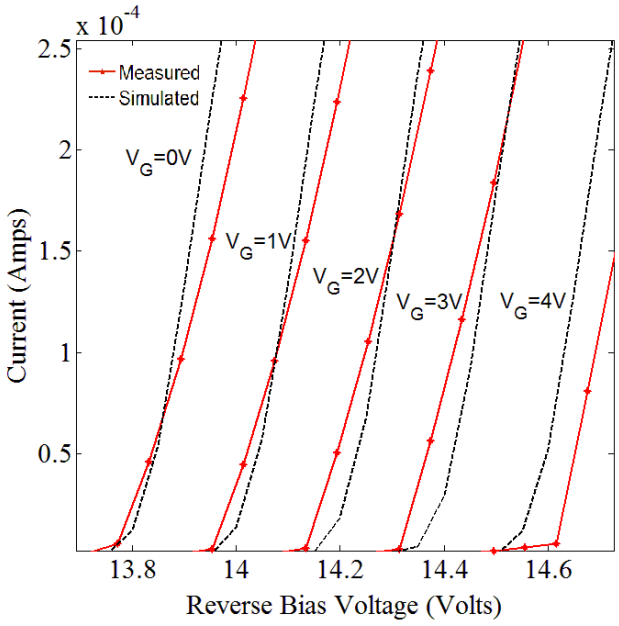



**Figure 4.7:** Simulated and measured reverse I-V characteristic for device1 [71].

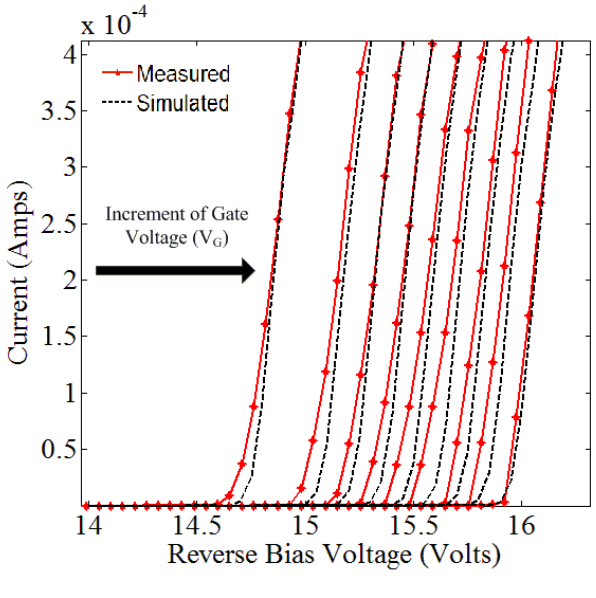



**Figure 4.8:** Simulated and measured reverse I-V characteristic for device2. VG increased from 0V to 8V [71].

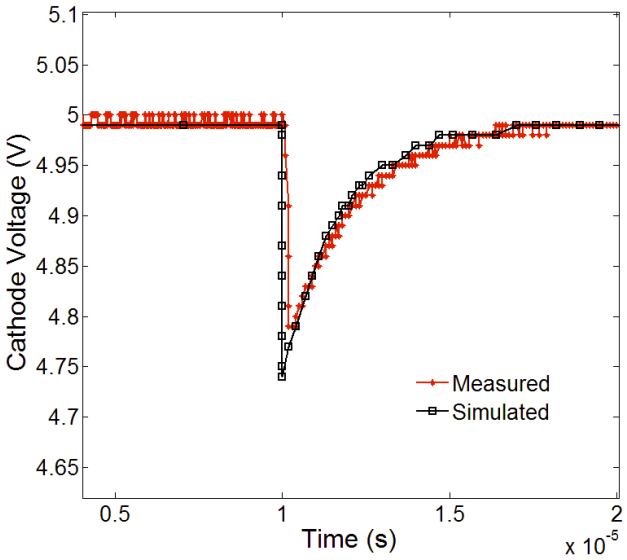



**Figure 4.9:** Simulated and measured cathode voltage at photon event and quenching behavior for device1 [71].

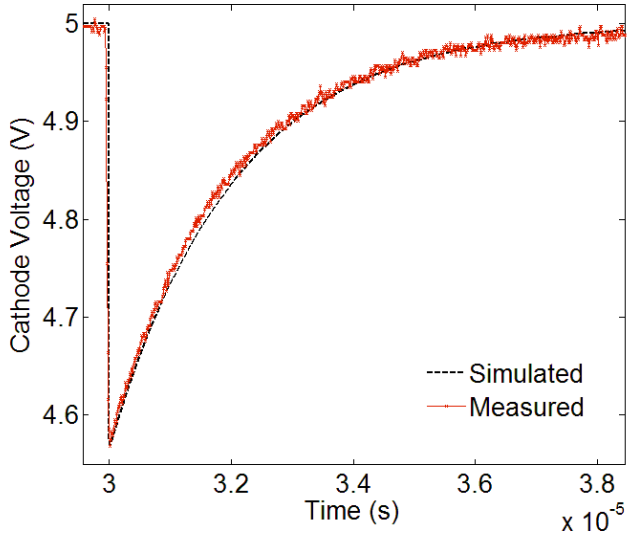



**Figure 4.10:** Simulated and measured cathode voltage at photon event and quenching behavior for device2 [71].

a circuit test bench as any other circuit simulation in Cadence. Figure 4.11 shows the temperature dependence of the dark count rate due to thermally generated carriers ($DCR_{Thermal}$) and carriers generated due to band-to-band tunneling ($DCR_{BTBT}$). At relatively lower temperatures the band-to-band tunneling dominates. At higher temperatures the thermal carrier generation is dominant.

From equations 4.6 and 4.9, the thermal generation rate is unaffected by the gate bias. However the generation rate due to band-to-band tunneling is a function of the gate voltage. Figure 4.12 shows that the gate voltage decreases the avalanche probability by a small amount. Thus, the voltage applied at the gate of the PGSPAD reduces the noise (DCR) by primarily reducing the generation rate due to band-to-band tunneling. Figure 4.13 shows the significant impact of $V_{Exc}$ on $P_{Av}$, and this result is in agreement with prior measurements.

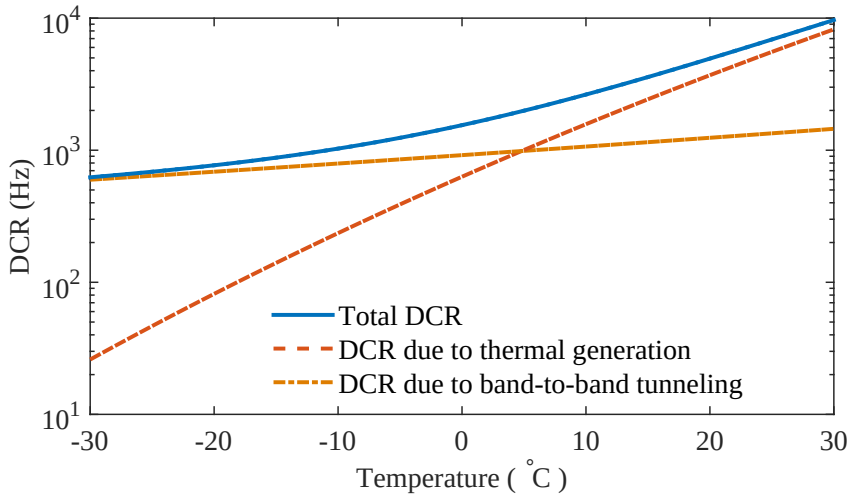



**Figure 4.11:** Simulation results showing temperature dependence of the dark count rate, DCR, due to thermal generation and band-to-band tunneling ($|V_G|$=5V & $V_{Exc}$=0.5V).

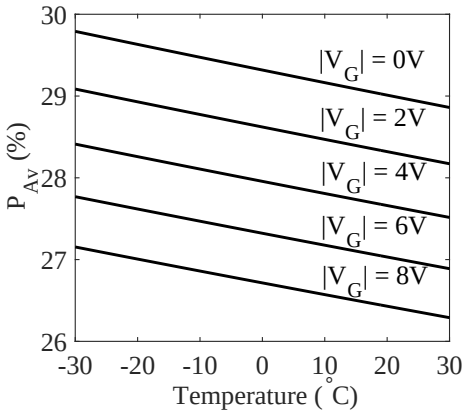



**Figure 4.12:** Simulation results showing the effect of gate voltage, $V_G$, on the avalanche triggering probability,$P_{Av}$, for $V_{Exc}$=0.5V.

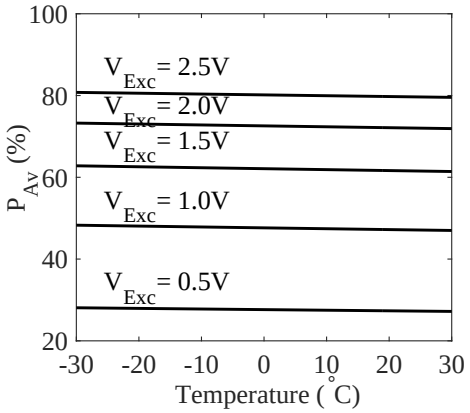



**Figure 4.13:** Simulation results showing the effect of excess bias, $V_{Exc}$, on avalanche triggering probability, $P_{Av}$, for $|V_G|$=5V.

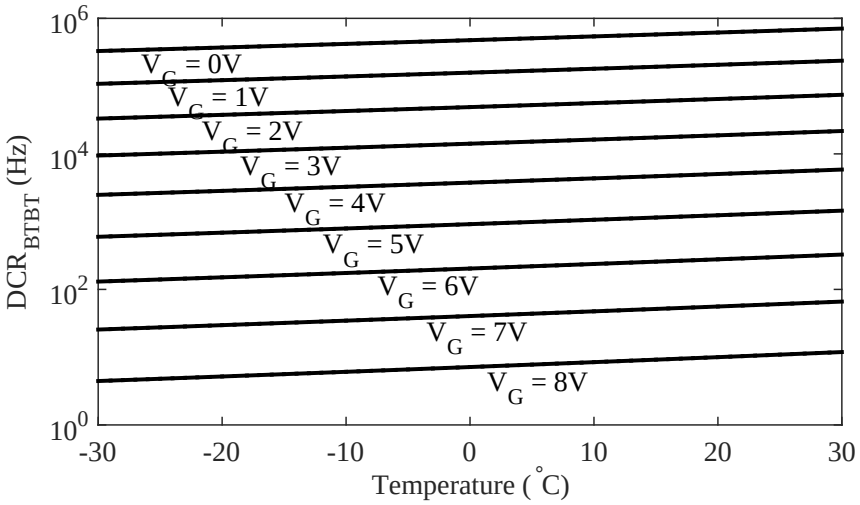



**Figure 4.14:** Simulation results showing the effect of the gate voltage, $V_G$, on the dark count rate, DCR, due to band-to-band tunneling ($V_{Exc}$=0.5V).

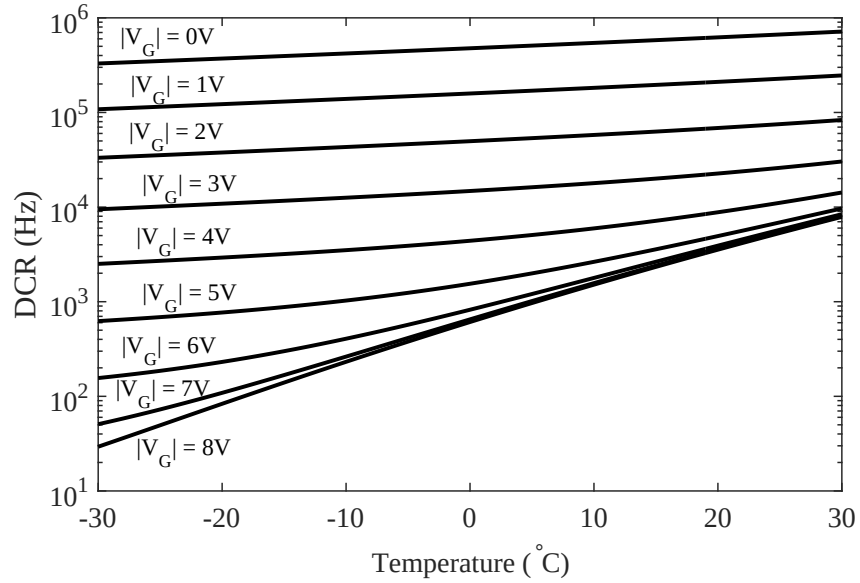



**Figure 4.15:** Simulation results showing the effect of the gate voltage, $V_G$, on the total dark count rate, DCR, for $V_{Exc}$=0.5V.

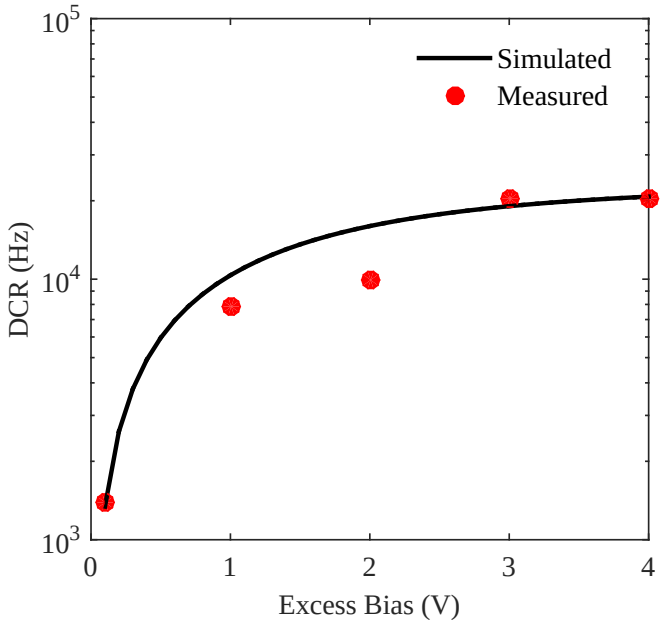



**Figure 4.16:** Dark count rate, $DCR$, as a function of excess bias, $V_{Exc}$.

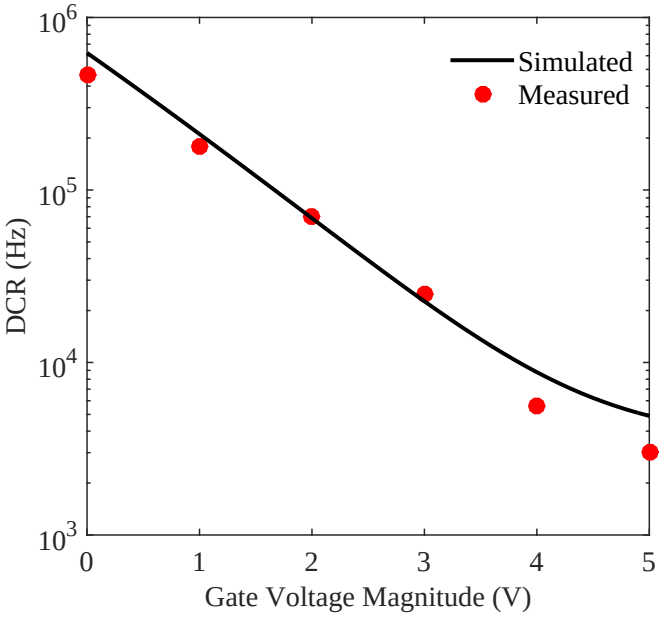



**Figure 4.17:** Dark count rate, $DCR$, as a function of gate voltage, $V_G$.

Figure 4.14 shows the significant reduction in band-to-band tunneling as a result of increasing $|V_G|$. Figure 4.15 presents the total dark count rate of the PGSPAD. At relatively lower temperature, the DCR can be minimized to few Hz for PGSPAD. But, as the temperature increases the rate of thermal generation increases. Around room temperature, the effect of $V_G$ in minimizing the noise is relatively lower.

The simulation results have been validated with experimental measurements. Figure 4.16 and Figure 4.17 compare the simulation with the experimental data showing the effect of $V_{Exc}$ and $V_G$ on the noise of the PGSPAD. The spectral profile simulation is compared in Figure 4.18. The simulations show good agreement with the measured experimental data.

The SPICE model reported in [70] simulates the static and dynamic behavior characteristics of a PGSPAD when a hardware description language (HDL) based

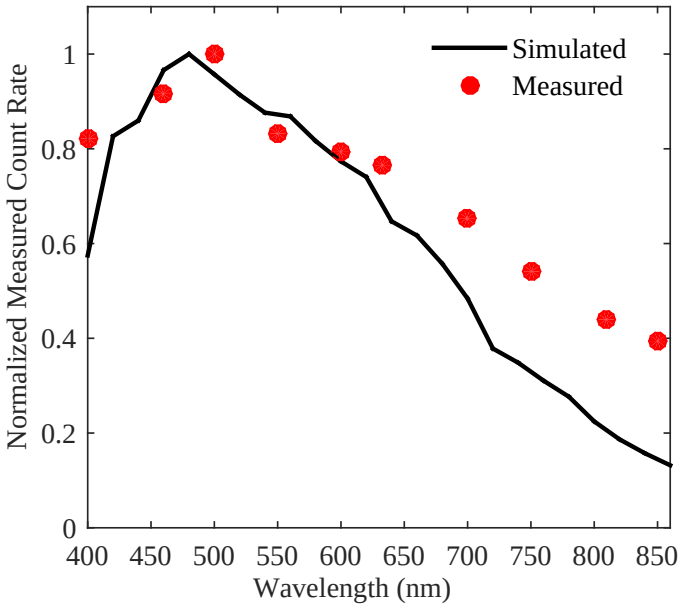



**Figure 4.18:** Spectral profile showing the normalized count rate as a function of the wavelength.

Verilog-A model, simulates the noise and optical behavior. Cadence has the capability of co-simulating Verilog-A and SPICE level circuits in the same test bench allowing for a comprehensive simulation of a PGSPAD.

## 4.5 Conclusion

This PGSPAD model, the first ever described, simulates static, dynamic, noise, and spectral behavior of the device, and shows good agreement with experimental data. This is the first model simulating the effect of gate voltage on the dark count rate (DCR) and spectral profile for a PGSPAD. This model will aid in designing and optimizing CMOS PGSPAD based circuits by providing estimated results before fabrication. Additionally, this model showcases the specific improvement in the noise floor of PGSPADs. The model still has room for improvement by including the effect of secondary breakdown, and improved parameter extraction.

# Chapter 5

# Improved Signal to Noise Ratio Across the Spectral Range for CMOS Silicon Photomultipliers

** **Portions of this chapter were published in:**

1. M. H. U. Habib, N. McFarlane, *"Improved Signal to Noise Ratio Across the Spectral Range for CMOS Silicon Photomultipliers,"* IEEE Sensors Conference, Nov. 2016.

2. M. H. U. Habib, N. McFarlane, *"A Perimeter Gated Single Photon Avalanche Diode Based Silicon Photomultiplier as Optical Detector,"* IEEE International Midwest Symposium on Circuits and Systems, Aug. 2015.

## 5.1 Introduction

Silicon photomultipliers (SiPM) are an alternative to photomultiplier tube (PMT) for overcoming PMT's shortcoming of being bulky, expensive, high voltage operated, and magneto sensitive. The application area of SiPMs covers, but is not limited to ,biophotonics, radiation detection, medical imaging, and light detection and ranging (LiDAR) [85, 86]. An SiPM is an array of single photon avalanche diodes (SPAD) connected in parallel, where the total current is proportional to the number of SPADs

triggered (Figure 5.1) [55,87,88]. This chapter describes the segments of this research presented in [55,88]. SiPMs require readout electronics whose architecture depends on the application. CMOS technology reduces the overall cost and enables the monolithic integration of the photosensor and the required readout electronics on the same chip.

In an ideal case, an SiPM should show a null output (no current) when the number of photons hitting the active area of the photosensor is zero. But, CMOS SiPM microcells (SPADs) suffers from unwanted events such as thermal carrier generation, trap assisted tunneling, and band to band tunneling as described in previous chapters. This leads to a current in complete darkness without the help of any photon. This unwanted current is the noise of the SiPM, and this noise affects the performance of the detector as any other detectors. This noise is termed as dark current of the SiPM. This chapter reports how the perimeter gated technique described earlier affects the dark current of the photodetector and improves the signal to noise (SNR) ratio of a CMOS SiPM over a spectral range of 350nm-800nm wavelength. As mentioned in in [55,88], this is the first reported perimeter gated SiPM with dark current reduction thus SNR improvement feature.

## 5.2 SiPM Architecture and Operation

The designed SiPM is an array of 9 $\times$ 18 microcells (Figure 5.1). Each microcell in the SiPM has a perimeter gated SPAD (PGSPAD) and a PMOS for quenching. The implemented perimeter gated SPAD is a square nwell-$p^+$ device with a polysilicon

strip of 3.3$\mu$m overlaying the junction. The SiPM is fabricated in 0.5$\mu$m standard CMOS process. Previous chapters described how the applied voltage on the polysilicon gate reduces the noise by modulating the electric field from non-uniformity to uniformity around the junction and mitigates premature breakdown [4, 55, 69, 89].

In this SiPM, all polysilicon gates of the PGSPADs are connected at a common node. Using a PMOS for quenching affords two advantages (1) fill-factor improvement and (2) quenching resistance variability. Fill-factor is the ratio of active area and total area of the device [55]. The active area is defined by the area sensitive to photons. Higher fill-factor is better because it reduces the dead-space or optically inactive spaces, in the array. Laying out a resistor in standard CMOS requires significant real estate. Thus, using a PMOS increases the fill-factor by reducing the dead-space.

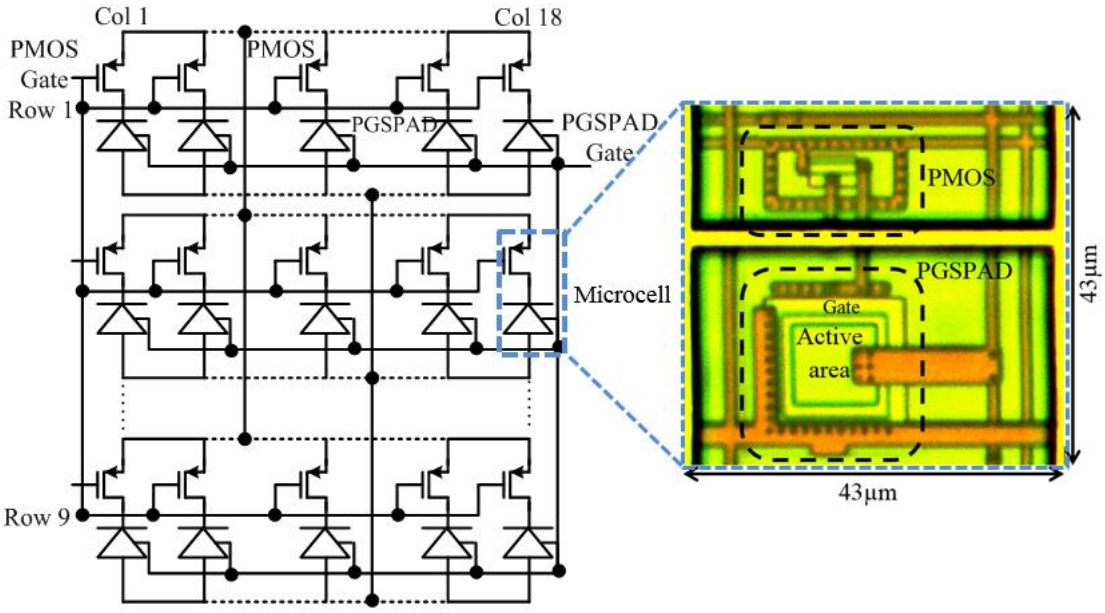



**Figure 5.1:** SiPM array (9 × 18 microcells) circuit diagram with photomicrograph of the microcell [89].

Each microcell has a total area of 43$\mu$m $\times$ 43$\mu$m, including an active area of 11$\mu$m $\times$ 11$\mu$m (Figure 5.1) yielding a fill-factor of 6.5%.

The voltage at the quenching PMOS gate is varied to set the quenching resistance size. The value of the quenching resistance ranges from 70k$\Omega$ to higher values by adjusting the gate voltage of the PMOS. For characterization described in Chapter 3, a discrete quenching resistance of 100k$\Omega$ was used [89] the PGSPADs. The sizing of the PMOS transistor helps in obtaining a resistance of around the 100k$\Omega$.

## 5.3 Experimental Results and Discussion

The experimental setup and the effect of gate voltage and excess bias voltage on the dark current and spectral response are discussed in this section. The SiPM was biased with two source-measure-units (SMUs). One SMU supplied the voltage between the source of the PMOS and the common anodes of all the PGSPADs. Other SMU was used to apply a voltage at the gates (node 'PGSAPD Gate' in Figure 5.1). The current limiting mechanism of the SMU protects the gates of the PGSPADs. The dark currents at different biasing conditions were measured by sweeping the voltage.

For spectral profiling, an optical testbench was developed. A monochromator with tunable light source (TLS-300X) provides lights of different wavelength with different optical power. A integrating sphere (819D-SL-3.3) helps with the evenly distribution of the light. An optical power meter (1936-R) is couple with the integrating sphere

for measuring the optical power coming on to the SiPM. The SiPM is couples with another port of the integrating sphere. Figure 5.2 gives a general idea of the optical testbench. The integrating sphere was connected to the TLS-300X using an optical coupler through which the light enters the sphere.

For studying repeatability, three chips were tested for each dataset and average values are reported in this study. The maximum deviation from the average value is 8% for any recorded value. The dark current is reduced with the increase in voltage magnitude at the gate of the PGSPADs (Figure 5.3) as discussed in Section 5.2. The dark current starts decreasing as the electric field around the junction becomes more uniform and the device moves closer to full volumetric breakdown.

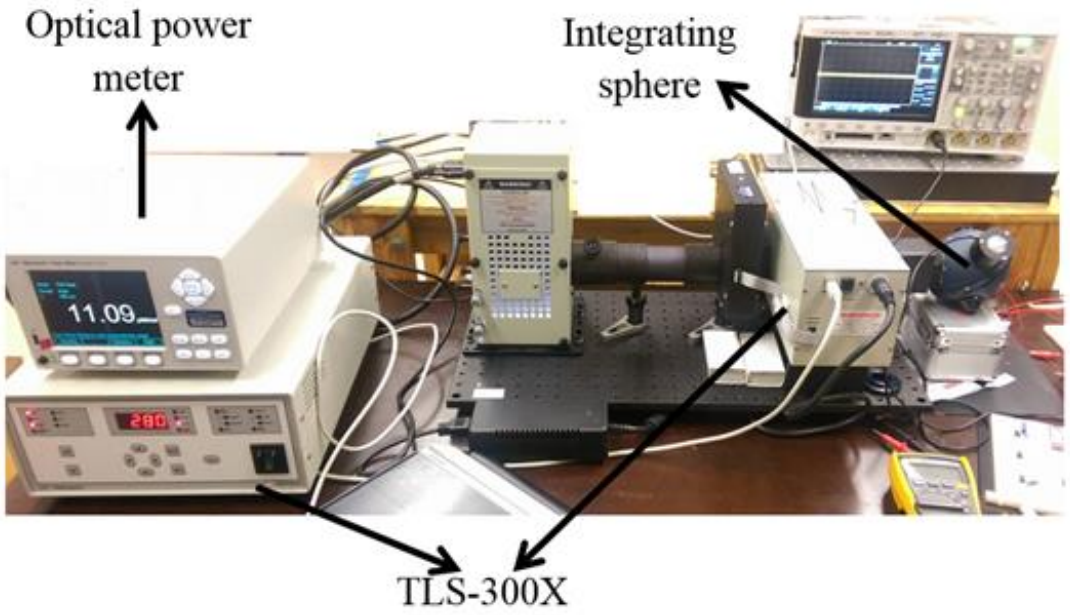



**Figure 5.2:** Optical testbench used to measure the current response at different wavelength [89].

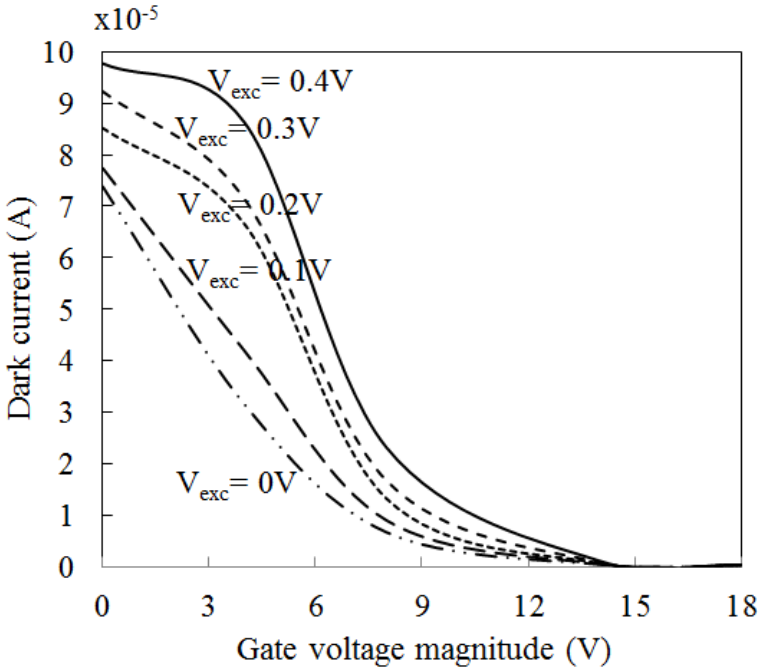



**Figure 5.3:** Dark current vs gate voltage for different excess bias voltages [89].

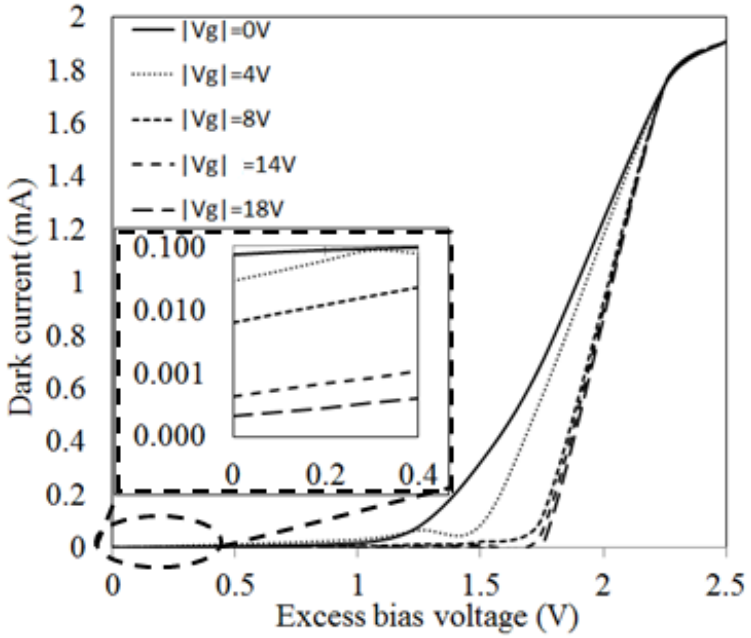



**Figure 5.4:** Dark current vs excess bias voltage for different gate voltages (inset shows zoomed in values up to 0.4V excess bias voltage [89].

The amount of applied voltage beyond the breakdown voltage is termed as the excess bias voltage ($V_{Exc}$). $V_{Exc}$ was swept from 0V to 2.5V. For a fixed gate voltage the dark current increases as the excess bias voltage is increased. The effect of $V_{Exc}$ on dark current for different fixed gate voltages is presented in Figure 5.4. Increasing excess bias increases the applied electric field resulting in increased drift velocity. The probability that generated carrier start an avalanche increases with excess bias. As a result of this dark current increases.

The spectral response is reported in terms of the signal to noise ratio (SNR). Dark current does not depend on wavelength. The current through the SiPM was measured for different electrical biasing conditions and different wavelengths while optical power was kept fixed at $20\mu W cm^{-2}$ ($8.14 \times 10^9$ photons/sec) [55]. This number is chosen as commercial SiPM manufacturers, such as Hamamatsu, characterized their optical detectors with a range of $10^8$-$10^{11}$ photons/sec for a wavelength of 500nm [90].

The spectral response of the SNR has a similar trend as photon detection efficiency (PDE). This is due to the fact that SNR and PDE are both proportional to the measured photocurrent. PDE is a probability that a SPAD produces an output signal in response to an incident photon and is proportional to the quantum efficiency of the material. For SiPMs, PDE and SNR are defined as [90, 91]:

$$PDE = \frac{I_m hc}{P_{op} G \lambda e} \tag{5.1}$$

$$SNR = \frac{I_m - I_d}{I_d} \tag{5.2}$$

where $I_m$= measured photocurrent, $I_d$ = dark current, $P_{op}$ = incident optical power at a particular wavelength ($\lambda$) over the active area, $G$=gain of the SiPM microcells, $h$=Planck's constant, $c$ = speed of light, and $e$ = electron charge. The gain ($G$) of the microcell is defined as:

$$G = \frac{CV_{Exc}}{e} \tag{5.3}$$

where $C$ = capacitance of the microcell and $V_{Exc}$= excess bias voltage.

The spectral profile for different excess bias with a gate voltage at a magnitude of 18V is shown in Figure 5.5. In the spectral range the signal to noise ratio has a peak at 500nm. Since dark current or noise increases with the excess bias, increasing the excess bias reduces the SNR of the device. The gain is proportional to the excess bias

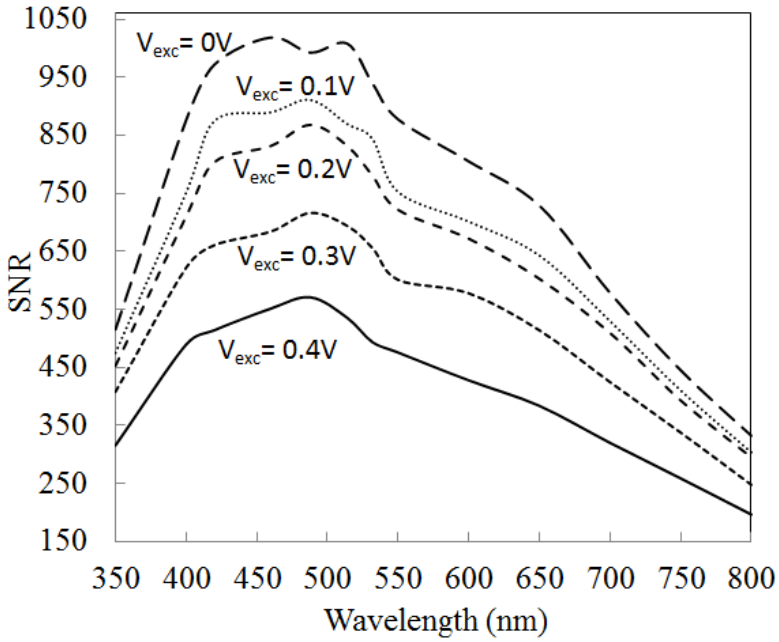



**Figure 5.5:** SNR is decreasing with the increase in excess bias voltage ($|V_G|$=18V) [89].

voltage (Equation 5.3). As discussed in Chapter 4, increasing excess bias increases the noise thus both PDE and SNR get reduced.

Device sensitivity is the rate of change in output current with optical power. Sensitivity increases with excess bias voltage, but at the same time the noise floor also increases. Biasing the SiPM with relatively higher excess bias will help in detecting very weak optical signals, such as in biophotonic applications, by achieving higher sensitivity. However, higher noise (lowered SNR) could make detection impossible. This is supported by the data presented in Figure 5.5 showing the SNR spectral profile for different excess biases and gate voltages [55]. The SNR is less than 1 when the gate voltage magnitude of 0V and 4V and the optical power is $20\mu W cm^{-2}$. This makes it very hard to detect a $20\mu W cm^{-2}$ optical signal when the excess bias voltage

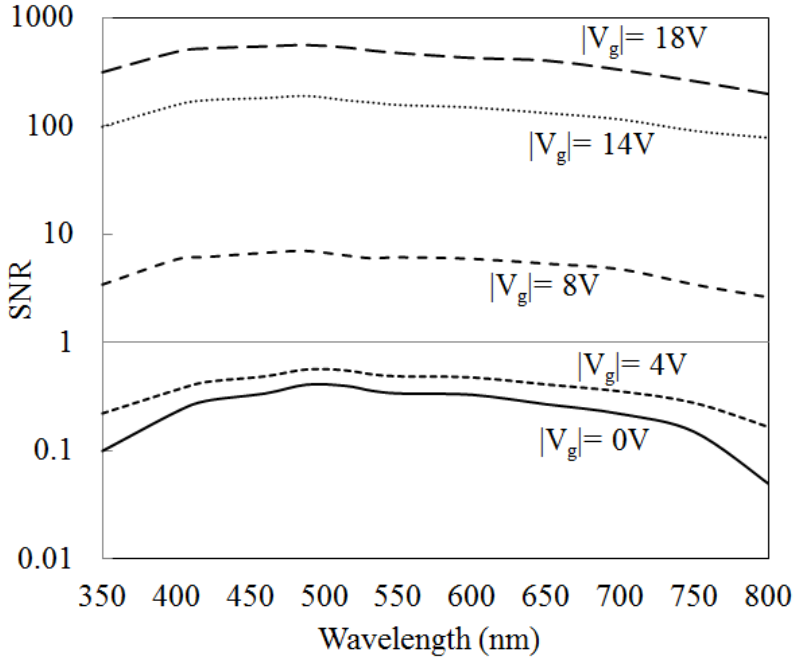



**Figure 5.6:** SNR is increasing with the increase in gate voltage magnitude ($V_{Exc}$=0.4V) [89].

is higher than 0.4V. Due to this, 0.4V was chosen as the highest limit for excess bias voltage while taking the measurements with a light of $20\mu W cm^{-2}$ optical power. But, the SNR can be increased by increasing the gate voltage magnitude. Higher SNR, at the same excess bias voltage, can be achieved by raising the gate voltage magnitude, and an SNR higher than 500 can be achieved when the gate voltage magnitude is 18V (Figure 5.6) [55]. For low sensitivity applications, an SNR of 1000 can be achieved by biasing the device relatively close to the breakdown voltage as shown in Figure 5.5 [55].

## 5.4 Conclusion

A CMOS SiPM with 162 microcells in a 0.5$\mu$m 2-poly 3-metal standard CMOS process was designed, fabricated, and experimentally characterized. In this chapter, the spectral response of PGSPAD based SiPM is reported for the first time. The SiPM shows the unique feature of tunability by using an additional applied gate voltage. The experimental results indicate promise as a method of normalizing the SNR response over multiple SiPM devices.

# Chapter 6

# A Tunable Dynamic Range Digital Single Photon Avalanche Diode

** **Portions of this chapter were published in:**

M. H. U. Habib, N. McFarlane, *"A Tunable Dynamic Range Digital Single Photon Avalanche Diode,"* IEEE Electron Device Letters, vol. 38, no. 1, pp. 60-63, Jan. 2017.

## 6.1 Introduction

In this chapter the performance of a digital SPAD pixel is quantified where the signal to noise ratio and dynamic range were improved using the perimeter gated technique. The perimeter gated technique to prevent premature breakdown added a tunability to the pixel that can broaden the application of the detector. This device was reported in [92] as first PGSPAD pixel with tunability.

## 6.2 Device Description

Previously, it has been verified that the breakdown voltage of a SPAD can be increased using the gate voltage creating the device known as the PGSPAD or perimeter gated single photon avalanche diode. This corresponded to a decrease in the dark count rate

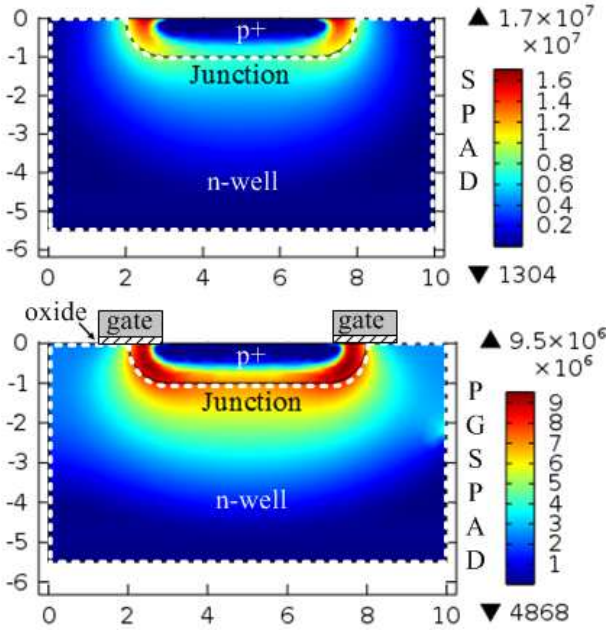



**Figure 6.1:** Electric field distribution of regular SPAD (top) and perimeter gated SPAD (bottom) with voltage applied at the gate. x-axis and Y-axis are in $\mu$m and colormaps are in $\mathrm{Vm}^{-1}$ [93].

(DCR) [4,5,16,55,70]. This is verified using Sentaurus device simulator (Figure 6.1). Two identical SPADs, one with a perimeter gate and one without, were modeled and simulated. The doping profile model (doping concentration, doping gradient, depth) of reference [4] was adopted and repeated here. The peak concentration in the $p^+$ region was $1\times10^{20}\mathrm{cm}^{-3}$. This concentration decreases with $\sigma = 50$nm in depth and $\sigma = 120$nm in the lateral direction. A shifted Gaussian profile with a mean of $0.1\mu$m away from the surface was used. For the n-well, the empirically obtained maximum doping from [4] was $1.22\times10^{17}\mathrm{cm}^{-3}$ with a shifted Gaussian profile. The p-substrate had a doping of $1\times10^{15}\mathrm{cm}^{-3}$. The simulation results of Figure 6.1 show that the electric field around the junction becomes more uniform which allows for full volumetric breakdown. Figure 6.2 shows the photomicrograph of the designed pixel.

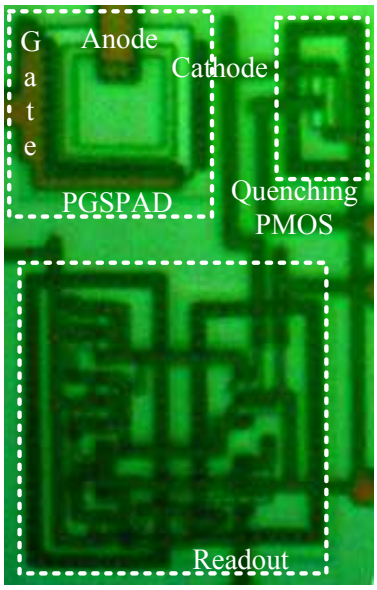



**Figure 6.2:** Photomicrograph of the perimeter gated SPAD pixel [93].

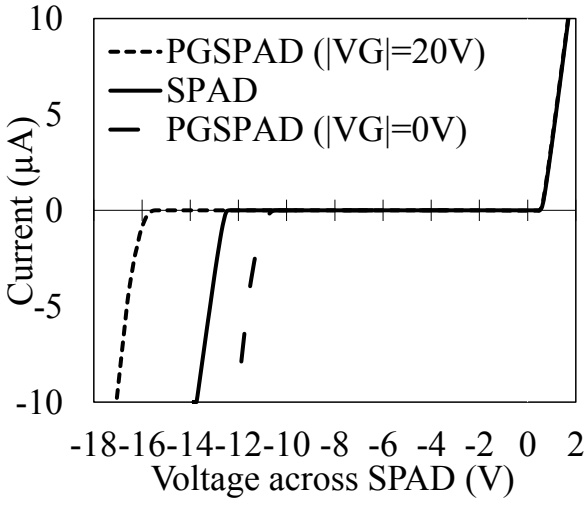



**Figure 6.3:** Breakdown voltage comparison for regular SPAD and perimeter gated SPAD with 0V and 20V applied at the gate [93].

Two identical SPADs with nwell-$p^+$ junction, one with a perimeter gate and one without a gate (regular SPAD), were fabricated. Experimental measurements of the IV characteristic are shown in Figure 6.3. The breakdown voltage for the regular SPAD is 12.5V. However, the breakdown voltage for perimeter gated SPAD can be varied withing a range of 11V to 15.8V by applying a voltage at the gate of the device. The perimeter gated device has a breakdown voltage less than a regular SPAD when the SPAD's gate voltage is 0V. However, it can be increased beyond the regular SPAD's breakdown voltage by increasing the magnitude of the gate voltage. This phenomenon was also reported in [16]. The experimental variation in the breakdown voltages show that the perimeter gated technique increased the breakdown voltage by almost 3.5V (Figure 6.3) relative to the regular SPAD. Since the noise floor (DCR) is reduced by increasing the breakdown voltage of the device with the prevention

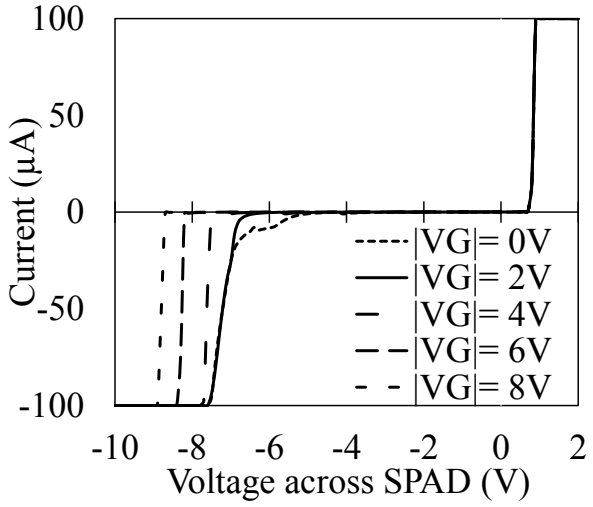



**Figure 6.4:** Breakdown voltage shifting for perimeter gated SPAD fabricated in 180nm standard CMOS process [93].

of premature breakdown [4, 5, 55, 89], noise minimization through this technique can improve the optical input dynamic range and output dynamic range of the device.

The process used previously have all been in non-STI (shallow trench isolation) processes. However, the technique has been verified in a submicron STI process (Figure 6.4). Shallow trench isolation (STI), in a submicron processes, results in poor performing SPADs. Techniques have been reported to mitigate its effects in commercial processes [24, 68]. A perimeter gated SPAD was designed and fabricated in a 180nm standard CMOS process and tested. The experimental results show the breakdown voltage changes with the same trend as the larger processes. The avalanche mechanism is inherently a probabilistic process with the breakdown voltage ($V_{Br}$) explicitly affecting the probability of initiating an avalanche as mentioned in Chapter 4. For a fixed excess bias voltage the probability of initiating an avalanche decreases with the increasing breakdown voltage. Thus, the change in breakdown voltage in the STI sub-micron process will have similar improvements as the larger CMOS processes.

## 6.3 Pixel Architecture

The pixel was designed and fabricated in a standard 0.5$\mu$m, 2-poly, 3-metal CMOS process. The total area of the pixel (Figure 6.2) is 2640$\mu m^2$, and the size of the optically sensitive active area was 100$\mu m^2$. The fill-factor of the pixel was 3.8%. A PMOS (Figure 6.2) operating in the ohmic region, with 1.5V bias applied at

MOSRes_Bias (labeled in Figure 6.5), was used for quenching. Using the PMOS in triode/ohmic region reduces the chip real estate area, and improves the fill-factor. The resistance of this PMOS can be varied from 70kΩ up to GΩ range. While characterizing a stand alone device [89], a discrete quenching resistance of 100KΩ was used. Thus, the size of the PMOS transistor (W=1.5$\mu$m, L=6$\mu$m) was selected to obtain a resistance of approximately 100kΩ.

The operation of a SPAD can be divided into three states, (1) build-up, (2) quench, and (3) recharge. The timing of these states depends on the value of the quenching resistor and the parasitics of the device [70]. The internal resistance and capacitance are beyond designer's control, and can only be optimized through sizing and layout techniques. However, the value of the quenching resistor can be selected. The quenching resistance cannot be too small, otherwise it may not be able to quench

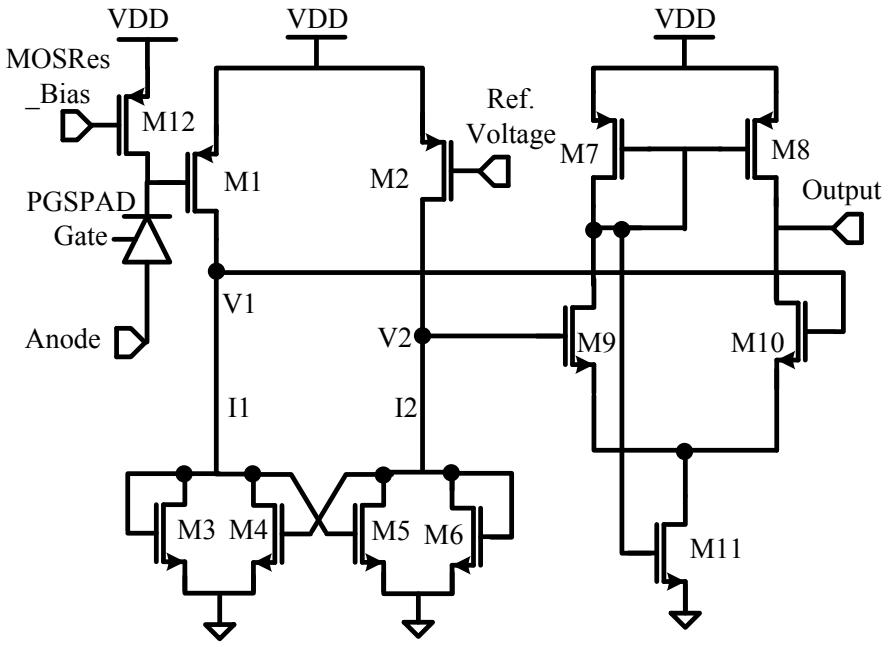



**Figure 6.5:** Circuit schematic of the pixel with experimental output pulses [93].

the avalanche. If the resistance is too large, the device takes longer to recharge, resulting in slower speeds. In this design, the dead time of the pixel (proportional to the value of this PMOS resistance) can be set between 5$\mu$s to 10ms by setting the voltage at MOSRes_Bias.

A comparator, consisting of a 6 transistor decision circuit and a 5 transistor differential amplifier, was used to generate the digital output of the PGSPAD. The transistors have a width of 2$\mu$m and length of 1$\mu$m. 2.5V was used for biasing. The cross coupled transistors M3-M6 allows the 5 transistor OTA to swing to one of the rails (high or low) depending on whether the input at the gate of M1 is greater than or less than the reference voltage. The reference voltage is set experimentally and an inverter is used to restore the output to digital logic levels.

## 6.4 Simulation and Experimental Results

Figure 6.6 shows the simulation results for the pixel. The PGSPAD model developed in [70] was used in the test bench. Each photon event generates a voltage spike ('Input' in Figure 6.6) at the gate of M1. The voltage at nodes V1 and V2 are also displayed in Figure 6.6. The output voltage goes to 0V with each photon event. Each time the SPAD triggers, a down going pulse is generated as shown in Figure 6.6.

For spectral profiling, an optical test bench consisting of a tunable light source system (TLS-300X), an integrating sphere (819D-SL-3.3), an optical power meter (1936-R), and two source-measure-units (SMUs) were setup. The TLS-300X is able to

vary the optical power and the wavelength of the light. An optical coupler coupled the integrating sphere to the tunable light source system. The pixel chip and the detector of the optical power meter were optically coupled to the ports of the integrating sphere.

Figure 6.7 shows the spectral profile of the pixel for different voltage magnitudes applied at the gate of the device. The maximum measured count rate, $\text{MCR}_{max}$, is limited by the dead time of the device. The digital pulse width is proportional to the dead time, and the $\text{MCR}_{max}$ is the reciprocal of the pulse width. Figure 6.7 shows that when the SPAD's gate voltage magnitude is 8V, the MCR reaches its maximum and the MCR does not vary with the wavelength. For lower gate voltages, the DCR is large and converges to the maximum count rate of the device. Therefore, the variation

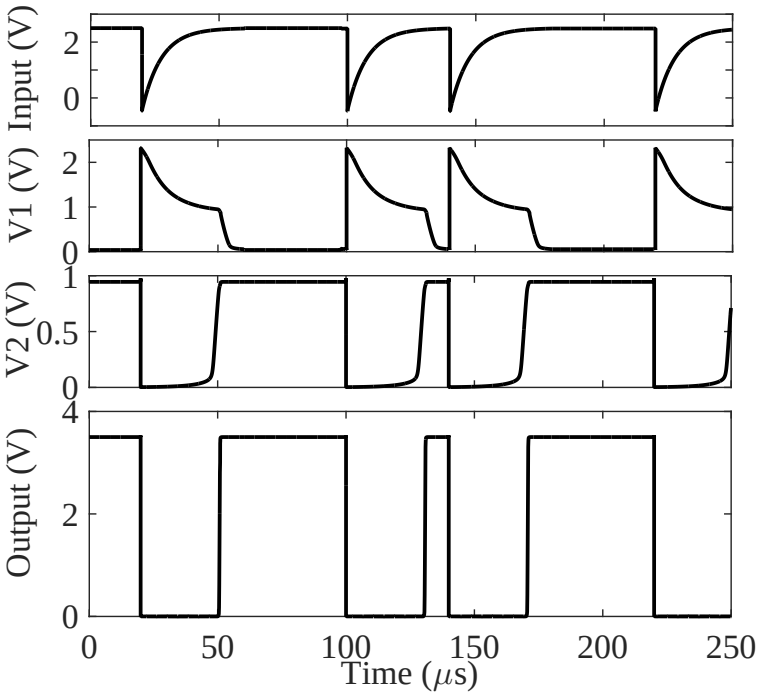



**Figure 6.6:** Simulation results showing the digital output for simulated photon events [93].

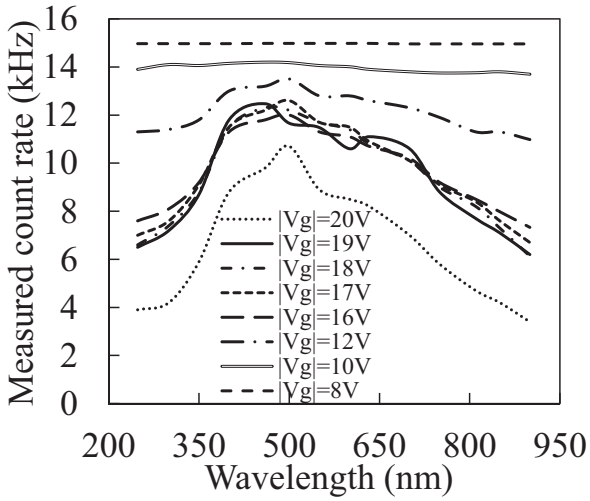



**Figure 6.7:** Measured count rate over the spectral range for different gate voltage [93].

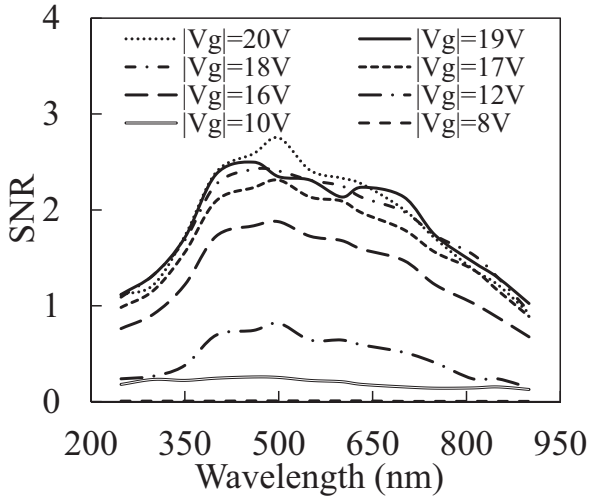



**Figure 6.8:** SNR throughout the spectrum for different gate voltage showing the improvement of SNR [93].

in measured count rate for a fixed gate voltage (lower in value) is less. As the gate voltage increases, the DCR decreases. As a result of this, at a gate voltage magnitude of 20V, the highest separation between the peak value and the noise floor is observed. Figure 6.8, illustrates the improvement in signal to noise (SNR) with applied gate voltage.

Figure 6.9 shows that the input optical dynamic range is improved for the designed pixel. When the PGSPAD's gate voltage magnitude ($|V_G|$) is 10V, the pixel can be used to detect light with optical power in the range of 10nWcm$^{-2}$ to 30nWcm$^{-2}$. The maximum detectable signal can be increased to 130nWcm$^{-2}$ by increasing the $|V_G|$ to 20V.

Table. 6.1 illustrates the effect of $|V_G|$ on the breakdown voltage, sensitivity, dynamic range, and SNR of the pixel. For a regular SPAD with no perimeter gate, the breakdown voltage is lower, and Equation 5.1 predicts an increase in the probability of an avalanche with the reduced breakdown voltages. The dark count rate is a function

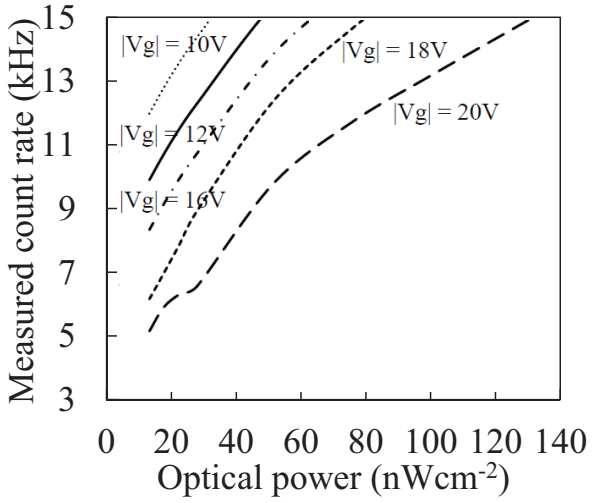



**Figure 6.9:** Output-input profile at different gate voltages [93].

**Table 6.1:** Gate voltage affecting breakdown voltage, sensitivity, dynamic range, SNR [93].

| Gate Voltage Magnitude ($V$) | Break-down Voltage ($V$) | Average Sensitivity ($Hz/nWcm^{-2}$) | Input Dynamic Range ($nWcm^{-2}$) | Output Dynamic Range ($dB$) | Peak SNR @ $30nWcm^{-2}$ |
|---|---|---|---|---|---|
| 10 | -15.12 | 147 | 20 | 1.1 | 0.26 |
| 12 | -15.32 | 137 | 36 | 3.1 | 0.82 |
| 16 | -15.52 | 125 | 51 | 8.7 | 1.87 |
| 18 | -15.66 | 123 | 69 | 12.4 | 2.42 |
| 20 | -15.83 | 77 | 122 | 18.9 | 2.75 |
| No Gate | -12.83 | – | – | – | – |

of the carrier generation rate and the probability that an avalanche is initiated. The generation rate is due to band-to-band tunneling, diffusion of carriers in the neutral regions, and thermal generation of carriers in the depletion region. This leads to an increased DCR of the regular SPAD device. The regular SPAD with the same dimensions and readout circuit as the PGSPAD described, did not exhibit avalanche breakdown.

As shown in Figure 6.10, increasing $|V_G|$ increases the input dynamic range of the pixel. This means the device saturates at relatively brighter light (higher photon flux) when the gate voltage of the perimeter gated SPAD is increased. However, this increased dynamic range is at a moderate cost of the sensitivity (Figure 6.10). Increasing $|V_G|$ for the perimeter gated SPAD also increases the output dynamic range of the pixel (Figure 6.11). There is a clear trade-off between the input dynamic range and the sensitivity while biasing the pixel for any particular application. Figure 6.12 shows the inverse relationship between the input dynamic range and the sensitivity.

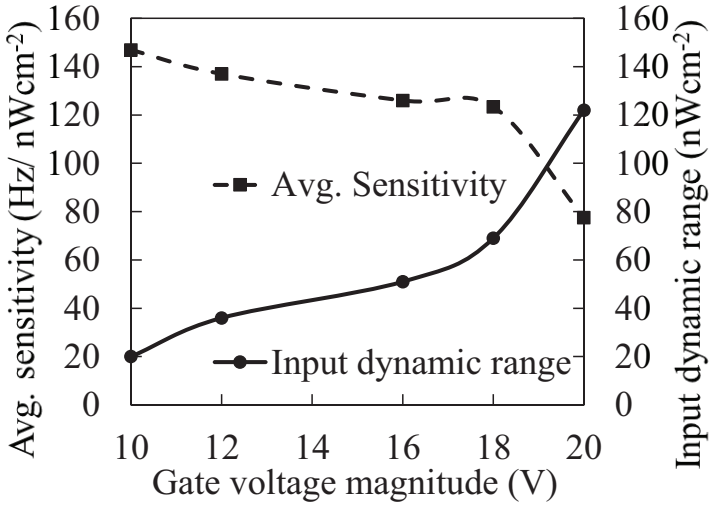



**Figure 6.10:** Average sensitivity and input dynamic range tuned by the gate voltage [93].

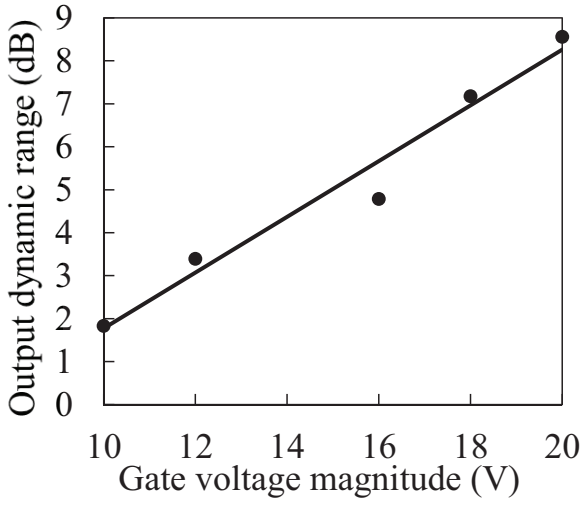



**Figure 6.11:** Gate voltage magnitude improving the output dynamic range [93].

Table 6.2 presents the performance comparison of this pixel with prior reported works. A study of SPAD's figures of merit (FoM) was reported in [54]. In this chapter SPADs fabricated in different technology nodes for different application were compared. The figure of merit for counting based detectors is defined by the following equation:

$$FoM = PDE \times \frac{\sqrt{A_{Active}}}{\sqrt{DCR}} \times \frac{1 - P_{AP}}{T_{Dead}} \tag{6.1}$$

where $PDE$ is photon detection efficiency, $P_{AP}$ is afterpulsing probability and $T_{Dead}$ is the dead time of the device. The higher the $FoM$ the better the performance of the device. In Equation 6.1, $FoM$ is directly proportional to $\sqrt{A_{Active}}$. But, increasing the size of the device will not yield a better performance because it will also increase the noise (DCR) as described in Chapter 4. As reported in Table 6.2, the performance of the designed pixel, without gate correction, is worse than other reported SPADs [33, 37, 40, 49]. However, increasing the gate voltage makes the performance better

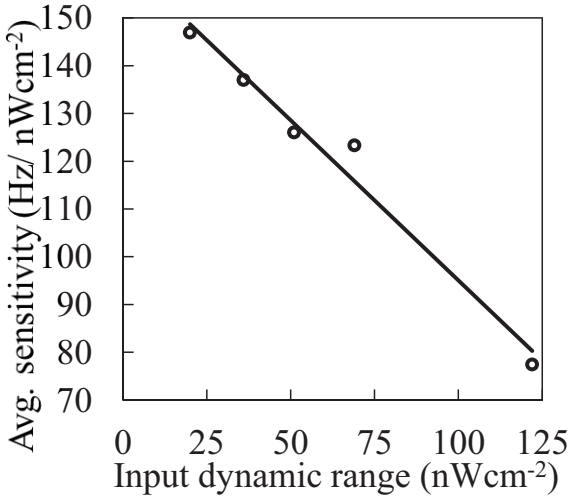



**Figure 6.12:** Average sensitivity vs. input dynamic range for sensitivity and dynamic range trade-off [93].

**Table 6.2:** Comparison with prior art.

| | [33] | [37] | [40] | [49] | This Pixel | | |
|---|---|---|---|---|---|---|---|
| | | | | | $\|V_G\|$=8V | $\|V_G\|$=16V | $\|V_G\|$=20V |
| $PDE_{PEAK}$ | 35 | 2.5 | 36 | 38 | 2.1 | 14 | 20 |
| CMOS Node (nm) | 350 | 180 | 180 | 90 | 500 | 500 | 500 |
| Area ($\mu m^2$) | 38.5 | 78.5 | 78.5 | 50.3 | 100 | 100 | 100 |
| DCR (kHz) | 0.65 | 60 | 5 | 16 | 14.9 | 5.5 | 1.7 |
| FoM | 0.2 | 0.03 | 0.03 | 0.01 | 0.003 | 0.04 | **0.1** |

than SPADs reported in [37, 40, 49] and close to the device in [33] by reducing the noise. Thus, without any special layout techniques or circuits, a perimeter gated SPAD can significantly improve the efficiency of the SPAD device.

## 6.5 Conclusion

A tunable dynamic range CMOS digital SPAD pixel was designed, simulated, fabricated, and experimentally characterized for dynamic range, sensitivity, and SNR. The improvement in dynamic range that using perimeter gating affords is reported for the first time. The effect was characterized in a non-optimized 0.5$\mu$m process design, but the tuning effect on the breakdown voltage has been experimentally verified in a submicron STI process. Moreover, as mentioned in Chapter 4, the avalanche probability ($P_{Av}$) increases with the lowering of temperature. As a results of which better sensitivity can achieved at lower temperature. Since, the noise (DCR) will be reduced at lower temperature, the input optical dynamic range will be higher as well. The exact choice of the PGSPAD's gate voltage will be application dependent.

This study shows not only a technique for improvement, but also offers qualitative guidelines for operating conditions for a given application.

# Chapter 7

# A 3 × 3 Digital Silicon Photomultipier with Noise Variation Compensation

## 7.1 Introduction

Implementation of high-performance SPAD devices comparable to PMT performance, high photon detection efficiency and high timing resolutions have been reported in [34, 93]. However, the main drawbacks of such systems are raised cost, reduced levels of miniaturization, and higher parasitics restricting the performance. In this chapter, the design the results of a PGSPAD pixel array is described. A technique for dead time minimization is used for the pixel. Moreover, how the noise variation in pixels of the the array can be reduced is explained in this chapter.

## 7.2 Design of the Pixel

This technique does not reduce the dead time of the device itself. It instead uses four identical PGSPADs in a single pixel. If one of these four enters the dead time zone the other three PGSPADs are still active for absorbing the photon energy and initiating an avalanche. Each PGSPAD has a PMOS connected to its cathode. This PMOS, operating in the triode/ohmic region is the variable quenching resistance.

The spike generated at the cathode of the PGSPAD produces a digital pulse at the output of the Schmitt trigger. The period of this pulse is small relative to the dead time of the PGSPAD. The avalanche produces a positive edge at the Schmitt trigger output. The output can come back to the initial value, depending on the threshold, long before the PGSPAD is reset back to the idle condition. The output of the OR gate sums all the pulses from the four PGSPADs if the pixel.

Figure 7.1 shows the architecture of the pixel. All the anodes of the PGSPADs are shorted. Each Schmitt trigger block has six transistors and all the Schmitt trigger blocks are biased identically. A basic eight transistor OR gate is used in the design.

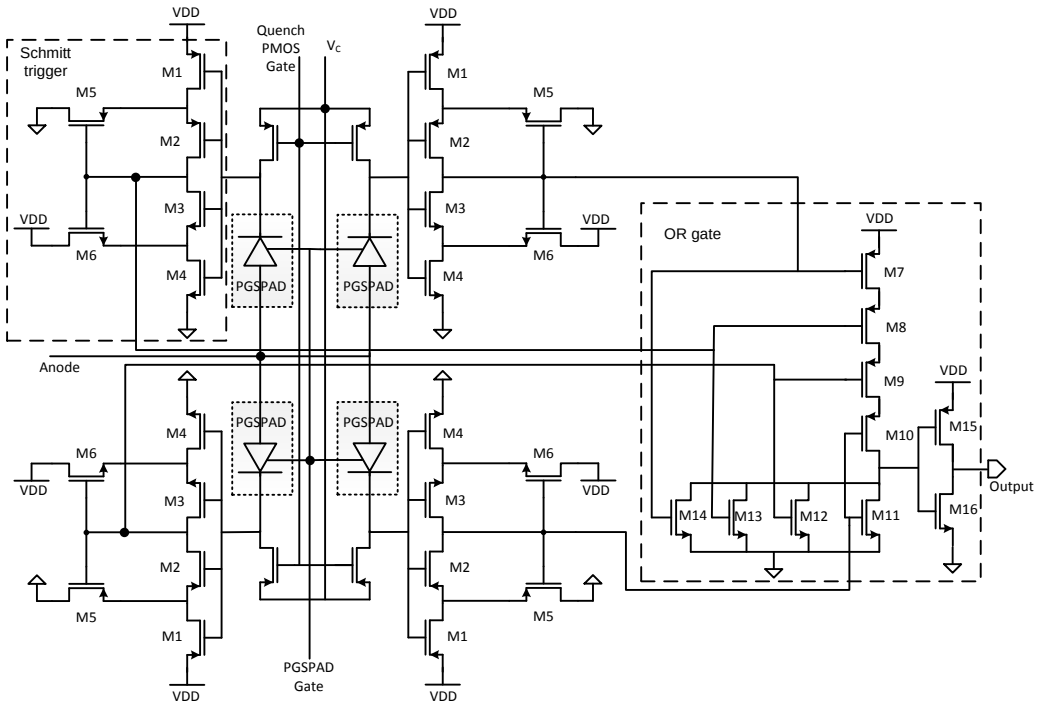



**Figure 7.1:** Schematic of the designed pixel. Each PGSPAD has a PMOS for quenching and a Schmitt trigger block for processing. The OR gate is combining the all the processed outputs from four PGSPADs.

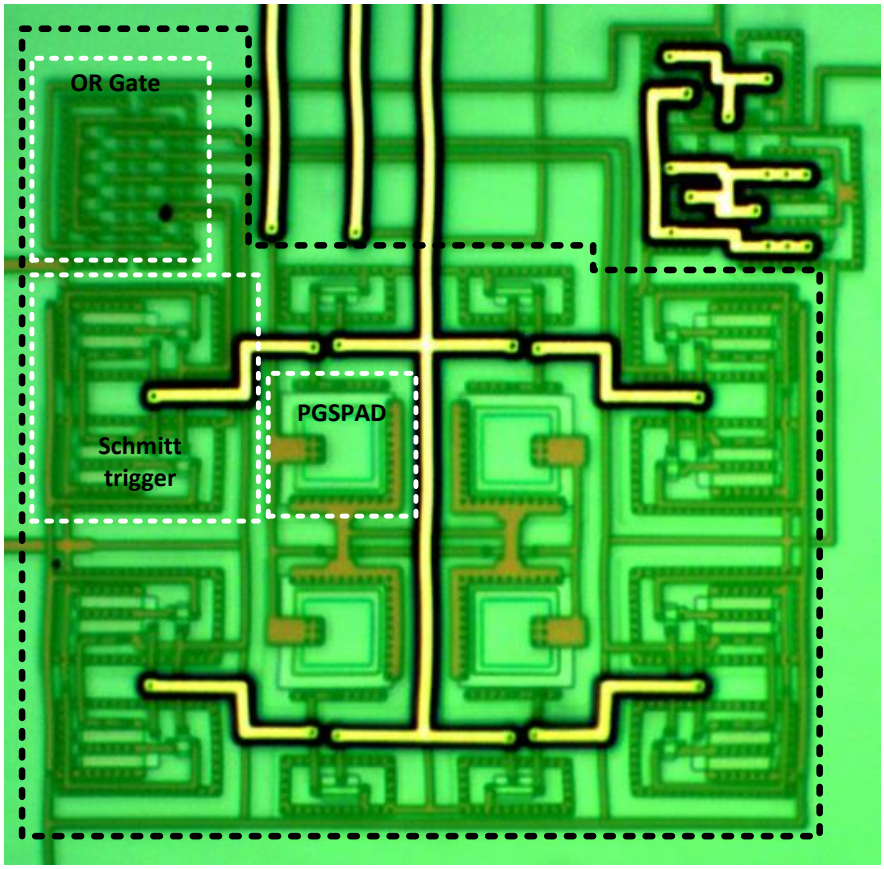



**Figure 7.2:** Photomicrograph of the pixel showing PGSPAD, Schmitt trigger block and the OR gate.

The photomicrograph of the pixel is shown in Figure 7.2. This pixel is fabricated in standard 0.5$\mu$m, 2-poly, 3-metal CMOS process. The active area of each PGSPAD is 10$\mu$m $\times$ 10$\mu$m. The The diode is layed out using the n-well and p diffusion layers. $\left(\frac{W}{L}\right)_{M_{1-4}} = \frac{10}{2}$, $\left(\frac{W}{L}\right)_{M_{5-14}} = \frac{2}{2}$ are the sizes of transistor used in the design (Figure 7.1). The quenching PMOS size is $\frac{W}{L} = \frac{1.5}{6}$. The total area of the pixel is 8150$\mu$m$^2$ with a total active area of 400$\mu$m$^2$.

## 7.3 Test Setup

The testbench showed in Figure 7.3 was developed for optical testing. Two Keithley 2400 source-measure-units (SMUs) were used: one for applying voltage at the common

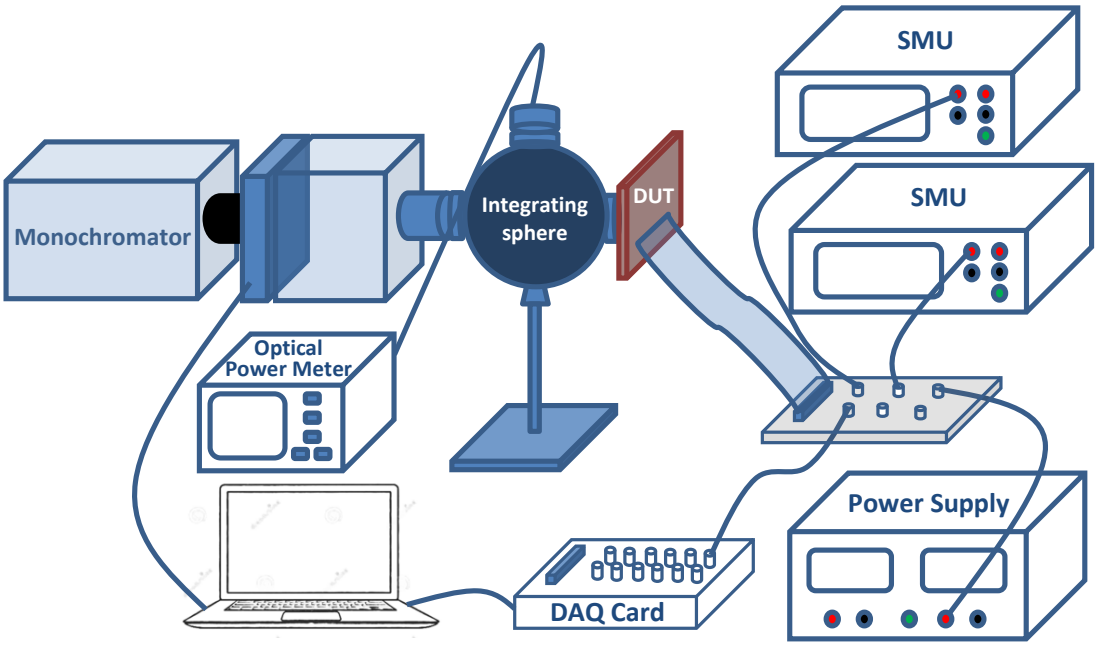



**Figure 7.3:** Test setup developed for optical testing. The same setup was used for I-V characterization without using the optical equipment.

anode terminal of the pixel and the other supplied the gate voltage. Using compliance of the SMUs, current values were limited to prevent damaging the device. The power supply was used to supply bias voltage to the Schmitt trigger blocks and the OR gate. For the I-V characterization, the bias voltage was swept during the testing. The gate voltage does not have any effect on the forward bias. In the reverse mode, the magnitude of the gate voltage shifts the breakdown voltage.The voltage on the gate was swept using another SMU. Figure 7.6 shows the I-V characteristics of the detector.

To test the optical functionality, the optical profiling of the pixel is needed. A tunable light source system (TLS-300X) with the functions of changing the wavelength and optical power was used. An optical coupler coupled the integrating sphere (819D-SL-3.3) to the tunable light source system. An optical power meter (1936-R) was used to measure the power of the light coming to the pixel. Two SMUs and a power supply were used for biasing. The output is counted with a Data acquisition (DAQ) card. A MATLAB code controls the DAQ card, saves data on the computer. It also counts the pulses and calculate the measured count rate and plot the output.

## 7.4 Simulation and Experimental Results

Figure 7.4 shows the simulation results of the design. The pixel was simulated in Cadence using the PGSPAD model reported in [69, 70] and described in earlier chapters. This timing diagram shows the voltages at the cathode terminals of the

PGSPADs numbered 1 to 4. Here PGSPAD3 goes into avalanche before the others. A digital pulse is recorded at the output for that. PGSPAD3 starts reseting, and PGSPAD1 goes to avalanche. Another digital pulse is recorded for PGSPAD1 while PGSPAD3 is still recovering. Here a total four photon events are detected, including the detection by PGSPAD3, while PGSPAD3 is still reseting to the initial state. From simulation, the time resolution of this pixel is better than the time resolution of the PGSPADs used in the pixel. In simulation the output pulse width is less than 100ns but the dead time and number of PGSPADs used in the pixel determine the degree of improvement. Since, four PGSPADs are used in this pixel, the dead time can reduced to 25% of dead time of the PGSPAD with same active area at best.

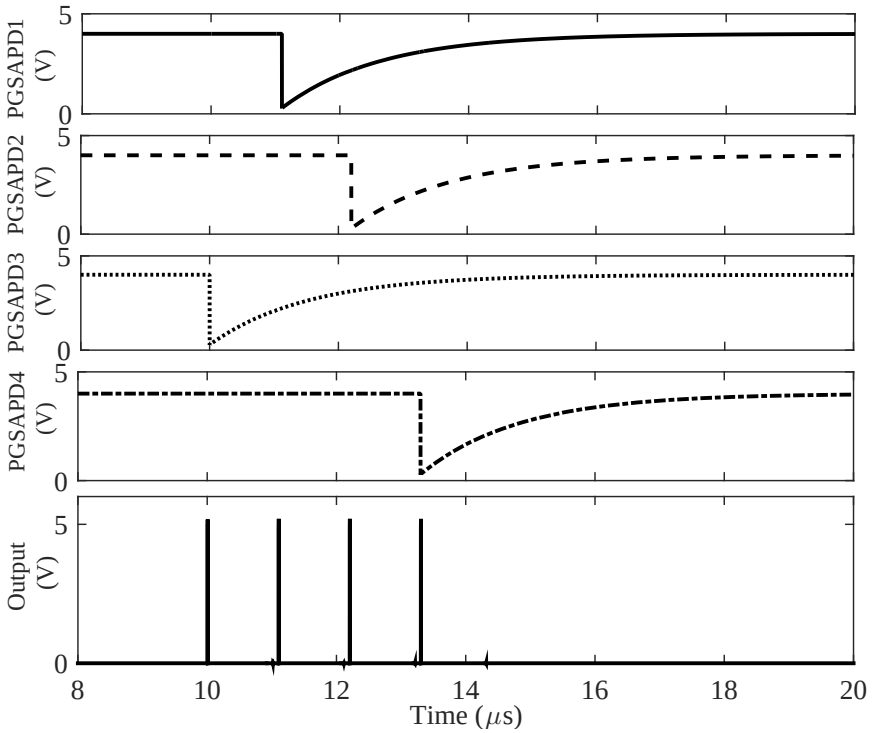



**Figure 7.4:** Simulation result showing how one PGSPAD of the pixel can generate a response when the other are non responsive from previous detection and thus reducing the dead time.

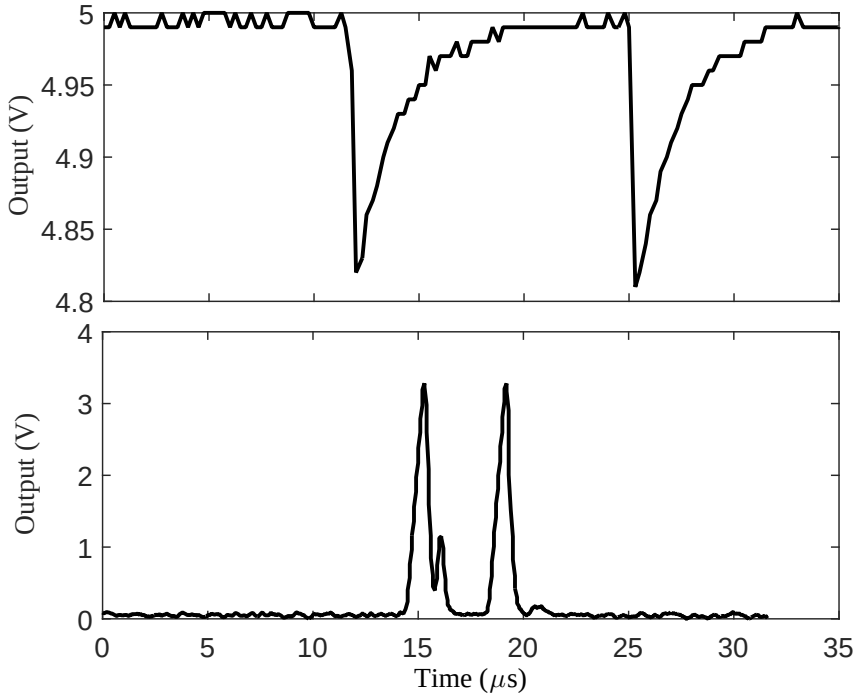



**Figure 7.5:** Experimental results showing the dead time minimization. The dynamic response shown in the top figure is from a PGSPAD with area of 12,000$\mu$m$^2$. The bottom shows around 75% reduction in dead time for the designed pixel having an area of 8,150$\mu$m$^2$.

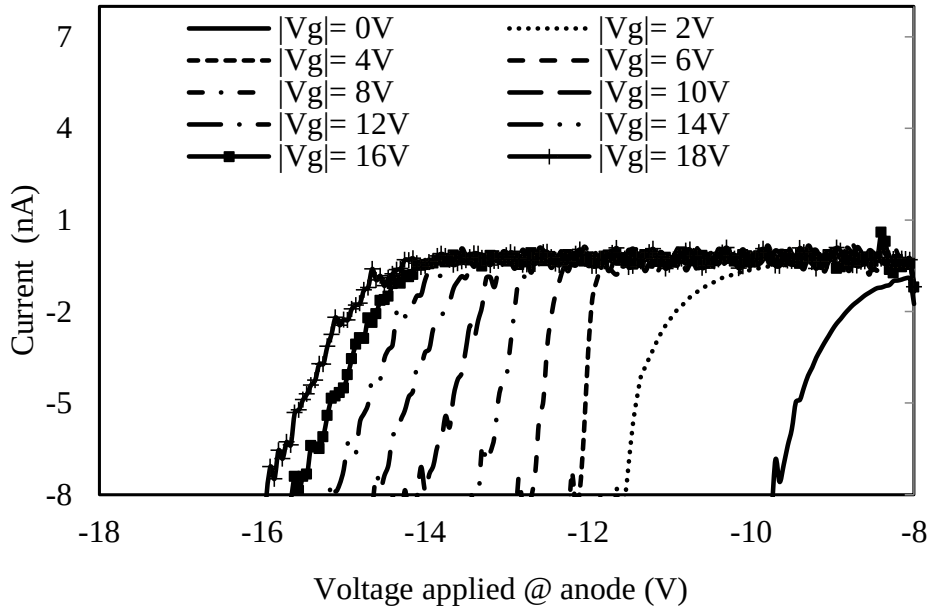



**Figure 7.6:** IV characteristics showing the gate voltage improving the breakdown voltage by reducing the non-uniformity in electric field distribution.

Earlier research shows that the dead time of a SPAD increases with the size of the device. So, a PGSPAD of the same size as the pixel should have higher dead time. So, using the same chip real estate higher time resolution can be achieved using this technique.

Figure 7.5 shows the experimental results for this pixel and a perimeter gated SPAD with the same chip space as the pixel. Under same condition, the dead time of the for the PGSPAD is around 10$\mu$s where the for the pixel a 2.5$\mu$s. Here the dynamic property is compared using same time scale. The pixel can detect the next event while the standalone PGSPAD is still recovering.

The effect of the gate is verified and optically characterizes the pixel. The change in breakdown (Figure 7.6) voltage verifies that the PEB prevention technique works for this pixel.

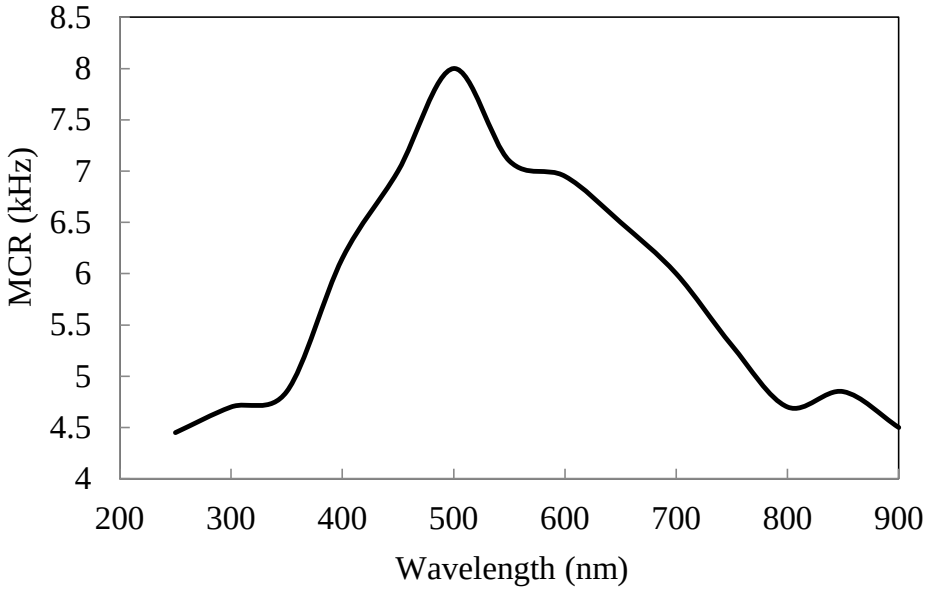



**Figure 7.7:** Optical response of the pixel over the spectral range.

Figure 7.7 shows the spectral response of the pixel. The spectral profile is similar to profiles reported earlier [30]. It has a peak around 500nm as expected. The spectral response is for an optical power of 100nWcm$^{-2}$.

The limits of the dead time minimization depends on the dead time of the actual PGSPAD device used in the pixel and the pulse width of the OR gate output. The dead time of the PGSPAD is a function of the RC time constant of the device and associated quenching circuit. The pulse width of the output at the OR gate depends on the pulse width of the Schmitt trigger circuit. The pulse width of the Schmitt trigger is determined by the high and low switching voltages and the dynamic characteristics of the PGSPAD. The switching voltages of the Schmitt trigger depends on the transistor sizing. The maximum number of PGSPADs in the pixel is the ratio of the dead time of the PGSPAD and the pulse width. Exceeding this maximum will not result in any further minimization of the overall pixel dead time.

The 3 $\times$ 3 digital SiPM is designed using the pixel shown in Figures 7.1 and 7.2. The gate voltages of the pixels can be controlled individually for noise (DCR) variation compensation. A data acquisition (DAQ) and MATLAB code as shown in Figure 7.3 is used to test this optical detector. Figure 7.8 shows how the noise is reduced with increasing the gate voltage. The variation in noise while the sharing the same biasing can be corrected by individually controlling the gate voltage for each pixel (Figure 7.9).

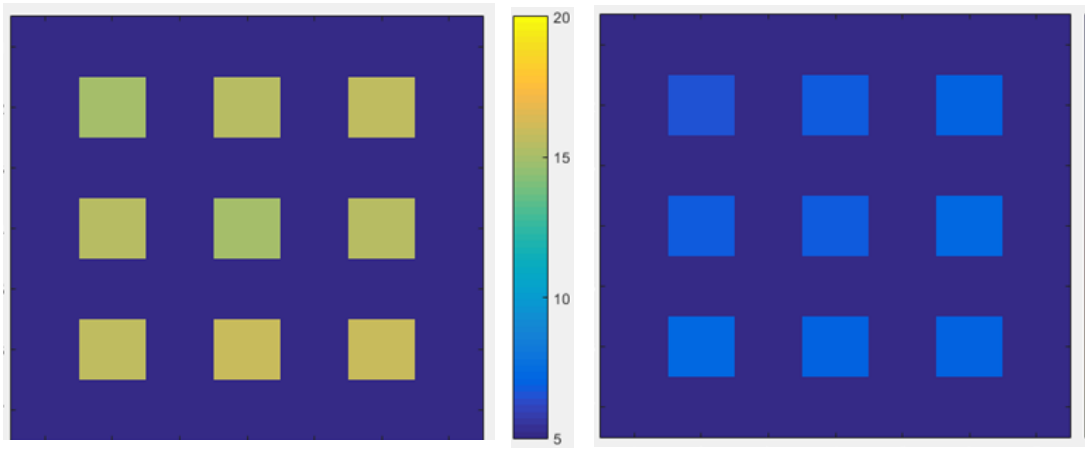



**Figure 7.8:** Noise of 3 × 3 array of pixel designed as optical detector. The noise response shown in the left block is when gate voltage the relatively low (10V). Increasing the gate voltage (15V) reduces the noise as shown in the right block. The noise (dark count rate) value in the colormap is in kHz.

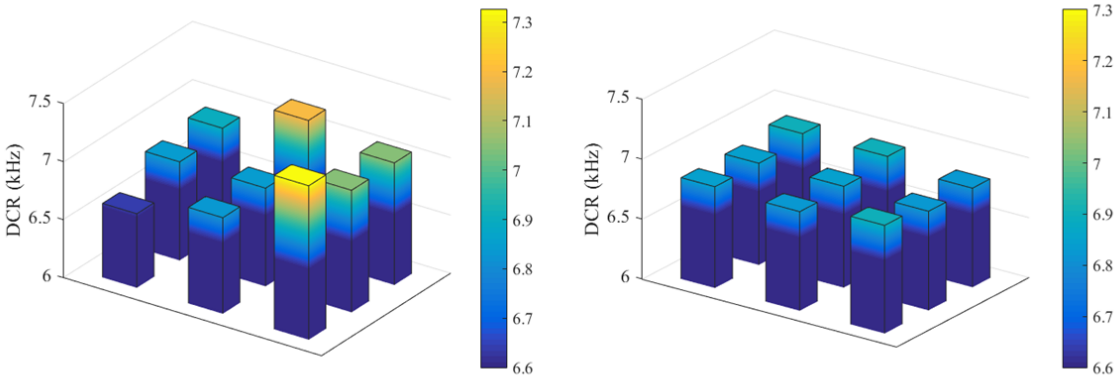



**Figure 7.9:** Noise variation compensation by controlling individual gate voltages: (left) before compensation, (right) after compensation.

## 7.5 Conclusion

A 3 × 3 digital SiPM using pixel with reduced dead time is reported in this chapter where the dead time is reduced to 25%. This is the first ever reported digital SiPM in which the noise variation between pixels is compensated using the perimeter gated technique. This technique also improves the detection efficiency of this digital SiPM. Thus, for applications where fixed pattern noise variation pixel to pixel is a limiting factor on detection, this technique provides significant improvements.

# Chapter 8
# Conclusion and Future Work

## 8.1 Original Contribution

Monolithic perimeter gated single photon avalanche based optical detectors are presented in this dissertation. The perimeter gated technique prevented the premature breakdown of the device and reduced the noise. This gate also enabled the option for noise variation minimization between pixels in an array.

The original contributions of this work are:

- Characterization of perimeter gated SPAD to observe the effect of placing the poly-gate and applying voltage to it. Devices were designed, fabricated, and tested for characterization as a function of shape, size, and junction type.

- Development of a novel comprehensive model for simulating the perimeter gated SPAD. This is the first reported model for this device. This model has the capability of simulating the static, dynamic, noise, and optical behavior of the device. The model was validated with experimental data and showed excellent agreement.

- Demonstration of a perimeter gated SPAD based silicon photomultiplier (SiPM) with improved noise performance for the first time. The dark current of the SiPM is reduced by applying the perimeter gated technique.

- Demonstration of the first ever digital perimeter gated SPAD with tunable dynamic range. The input dynamic range can be increased by reducing the dark count rate of the pixel but this also deceases the sensitivity of the pixel. Therefore, a trade-off between the dynamic range and sensitivity has to be made based on the application. The use of the tunable PGSPAD improves the figure of merit by 3 orders of magnitude.

- Demonstration of a 3 $\times$ 3 digital SiPM where the pixels use a dead time minimization technique consisting of multiple devices and simple electronics. The noise variation occurs for the breakdown voltage variation between the pixels. The noise variation between the pixels of the array can be minimized by controlling the pixel's gate voltage individually.

The core contribution of this dissertation is to reduce the noise (dark count rate) of SPADs fabricated in standard CMOS processes and develop detectors with improved system performance. The reported technique successfully validates the core of this research. This is very important for developing cheap, compact CMOS single photon detector with comparable performance.

## 8.2 Future Work

The following can be considered as future works for moving this research forward:

- The increment in breakdown voltage by applying the perimeter gated technique in PGSPADs fabricated in 0.5$\mu$m and 0.18$\mu$m process is reported in this dissertation. In the future, it can be applied to smaller processes to observe the effects of quantum mechanical related phenomena on the use of the gate.

- The effect of temperature on this device can be investigated to observe how the perimeter gated technique affects the noise in lower temperature.

- A row-column arrangement such as memory access technique can be developed for the array to make it more scalable.

- Power consumption was not within the scope of this dissertation. For many biological applications, this is an important consideration. In future work, an exploration of power consumption can help in increasing the device portability.

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# Vita

Md. Habib Ullah Habib received his B.Sc. degree in electrical and electronic engineering from Bangladesh University of Engineering and Technology in 2008. He worked as a telecommunication engineer in Bangladesh from 2008 to 2011. He received his M.S. degree in electrical engineering from University of South Alabama in 2013. He is currently working toward the Ph.D. degree at the University of Tennessee, Knoxville under the supervision of Dr. Nicole McFarlane. His research interests lie in mixed-signal circuit design, photodetector modeling, design, and testing, biomedical sensors, image processing, and pattern recognition.