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Design, Control and Protection of Modular Multilevel Converter (MMC)-Based Multi-Terminal HVDC System

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I am submitting herewith a dissertation written by Yalong Li entitled "Design, Control and Protection of Modular Multilevel Converter (MMC)-Based Multi-Terminal HVDC System." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

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Abstract

Even though today's transmission grids are predominantly based on the high voltage alternating current (HVAC) scheme, interests on high voltage direct current (HVDC) are growing rapidly during the past decade, due to the increased penetration of remote renewable energy. Voltage source converter (VSC) type is preferred over the traditional line-commutated converter (LCC) for this application, due to the advantages like smaller station footprint and no need for strong interfacing ac grid. As the state-of-the-art VSC topology, modular multilevel converter (MMC) is mostly considered. Most renewable energy sources, such as wind and solar, is usually sparsely located. Multi-terminal HVDC (MTDC) provides better use of transmission infrastructure, higher transmission flexibility and reliability, than building multiple point-to-point HVDCs. This dissertation studies the MMC-based MTDC system, including design, control and protection.

Passive components design methodology in MMC is developed, with practical consideration. The developed arm inductance selection criterion considers the implementation of circulating current suppression control. And the unbalanced voltage among submodule capacitor is taken into account for submodule capacitance design.

Circulating current suppression control is found to impact the MMC operating range. The maximum modulation index reduction is calculated utilizing a decoupled MMC model.

A four-terminal HVDC testbed is developed, with similar control and communication architectures of the practical projects implemented. Several most typical operation scenarios and controls are demonstrated or proposed.

In order to allow HVDC disconnects to online trip a line, dc line current control is proposed

through station control. Utilizing the dc line current control, an automatic dc line current limiting control is proposed. Both controls have been verified in the developed testbed.

A systematic dc fault protection strategy of MTDC utilizing hybrid dc circuit breaker is developed, including a new fast and selective fault detection method taking advantage of the hybrid dc circuit breaker special operation mechanism. Detailed criteria and control methods to assist system recovery are presented.

A novel fault tolerant MMC topology is proposed with a hybrid submodule by adding an ultra-fast mechanical switch. The converter power loss can be almost the same as the half-bridge MMC, and 1/3 reduction compared to the similar clamp-double topology.

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1 Introduction

1.1 Background and Motivation

Modern transmission grids are predominantly based on high voltage alternating current (HVAC) scheme due to the superior performance and low cost of ac generators and transformers. However, high voltage direct current (HVDC) transmission scheme also has some distinct advantages [1], including:

- Lower cost for long distance bulk power transmission;
- Lower cost for cable transmission (subsea, offshore);
- Capability to exchange power between two asynchronous power systems, even two systems with different frequencies;
- AC system support capabilities, including power flow control, frequency and voltage support, oscillation damping, and fault current limiting;
- Better use of right-of-way;
- Environmental benefits, such as less corona and audible noise, etc.

On the other hand, HVDC lines are embedded in HVAC grids and require power electronics converters and other associated station equipment, including filters, communications and special transformers. The high cost of converter stations makes the HVDC a niche, albeit important technology in today's transmission grid. But recently driven by the increased penetration of remote renewable energy, such as offshore wind and solar in the deserts, interests on HVDC are growing rapidly during the past decade [2].

Power electronic converter is the key component of HVDC. There are mainly two types of HVDC converters, the traditional thyristor-based line-commutated converter (LCC) and more recent IGBT-based voltage source converter (VSC). The LCC is a relatively mature technology, and majority of the existing HVDC projects use this converter type. The advantages of LCC are high efficiency, high power handling capability, simple and low-cost. On the other hand, it needs a large station footprint due to the large filter need and requires a strong interfacing ac grid to avoid commutation failure. What's more, the dc voltage polarity has to be changed in order to reverse the power flow direction. VSC HVDC was developed when high voltage and high current IGBT and IGCT became commercially available in 1990s. IGBT and IGCT are full switching devices which can be both turned on and turned off by gate control signals. It has the advantages of smaller station footprint, easy and fast active power reversal, inherent dynamic reactive power support, and since there is no need to reverse the dc voltage polarity, low-cost cross-linked polyethylene (XLPE) cable system can be used instead of the mass impregnated (MI) cable [3]-[5]. Considering the remote renewable integration usually has one or more of the following features: 1) long transmission length, 2) weak or even no interfacing ac grid, and 3) high cost on the station footprint, VSC HVDC is a more suitable transmission system in this application. Despite the limited power handling capability compared to LCC HVDC, the maximum dc voltage and power rating of VSC HVDC system have reached ±320 kV and 1000 MW, and are still increasing.

The use of VSC for HVDC was first pioneered over 15 years ago. Traditional two-level converter and three-level neutral-point diode-clamped converter topologies were used originally. Recently, the modular multilevel converter (MMC) is proposed, as shown in Figure 1-1, and emerges as a better candidate due to the following advantages [6]-[8]:

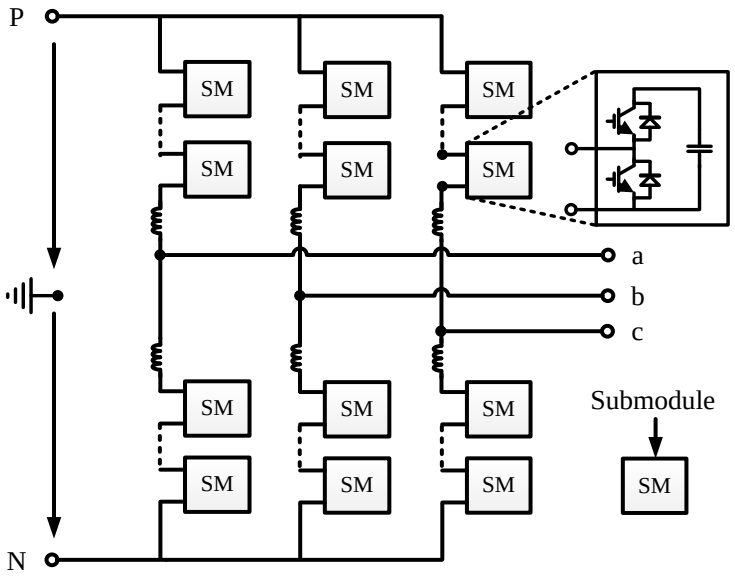


Figure 1-1. Basic structure of MMC with half-bridge submodule.

1) No direct series of power switches;

2) Much reduced slope (di/dt) of the arm currents and thus reduced high frequency noise;

3) Lower switching frequency and as a result of lower power loss;

4) Less requirement on ac filters;

5) Distributed locations of capacitive energy storages;

6) Inherent redundancy for sub-module failure management.

Many of the benefits are brought up because of the multilevel structure. And the modular structure feature distinguishes MMC from other traditional multilevel converter, such as diode-clamped multilevel converter and flying capacitor multilevel converter, with the advantages of easy assembly and flexibility in converter design. Therefore, MMC has become the state-of-the-

art topology for HVDC, and is adopted for commercial products like Siemens “HVDC plus” and ABB “HVDC light”.

Most existing HVDC are point-to-point and only limited multi-terminal HVDC (MTDC) projects were installed. But interests on MTDC system are growing, and even more complicated dc grids are proposed, such as the European supergrid [9] and pan Asia-Pacific supergrid [10]. The benefits of MTDC include better use of transmission infrastructure, higher transmission flexibility and reliability. An economic assessment between the point-to-point HVDC and VSC MTDC was conducted in [11]. It was concluded that there is no clear preference between these two options before 2020, due to the need of expensive dc circuit breaker for the multi-terminal system. However, the dc circuit breaker cost is expected to decrease in the future, as many manufacturers are involved in developing the new hybrid dc circuit breaker, like ABB and Alstom [12]-[13], which brings more opportunities for VSC MTDC.

MMC-based MTDC system is a promising solution for remote renewable integration. However, there are still some challenging hurdles for the development of MMC-based MTDC.

1) MMC has bulky passive components – arm inductor and submodule capacitor. The capacitor need is even 10 times larger than the 2-level converter. In order to minimize the converter size, it is critical to understand how to design these passive components.

2) Due to the complexity, most of the MTDC related research relies on simulation and only very limited testbeds and project installations exist. Many of the necessary operation and controls have not yet been demonstrated in experiments.

3) DC fault protection remains an open question in MTDC, due to the extreme demands on the protecting device, detection method and system recovery strategy.

The objectives of this research are to investigate the design methodology of the main passives in MMC, develop a MTDC testbed with the capability to demonstrate various operation and controls, and develop better control and protection methods of the MMC-MTDC system.

1.2 Dissertation Organization

The chapters of this dissertation are organized as follows.

Chapter 2 reviews the research activities in the design methodology of arm inductance and submodule capacitance of MMC, existing MTDC testbed and the development status of dc fault protection strategy as well as the fault tolerant converter topology. Based on the review, the research challenges in these areas and the objectives of this dissertation are pointed out.

Chapter 3 develops the arm inductance selection criterion with the consideration of circulating current suppression control, by deriving the analytical relationship between arm inductance and switching frequency circulating current.

Chapter 4 investigates the relationship between submodule capacitance and capacitor unbalanced voltage. The derived relationship is important for the submodule capacitance selection.

Chapter 5 studies the impact of circulating current suppression control on maximum modulation index of MMC.

Chapter 6 presents the design and development of a four-terminal HVDC testbed. The test results of different operation scenarios are also presented.

Chapter 7 proposes a dc line current control in MTDC for partial power flow control. A dc line current limiting control is also proposed based on the dc line current control.

Chapter 8 develops a systematic dc fault protection strategy of MTDC utilizing hybrid dc circuit breaker. A new fast and selective fault detection method is proposed and detailed criteria and methods for system recovery are presented.

Chapter 9 proposes a novel fault tolerant MMC topology. The proposed topology uses a hybrid submodule including an ultra-fast mechanical switch. The operation principle, benefits and cost are evaluated.

Chapter 10 summarizes the work has been done so far and plans the work which will be done next.

2 Literature Review and Challenges

This chapter reviews the research activities in the corresponding areas of modular multilevel converter (MMC) and MMC based multi-terminal HVDC (MTDC) system. The research challenges and objectives are explained to identify the originality of the work.

2.1 MMC Passives Design

2.1.1 Arm Inductor

As shown in Figure 1-1, each submodule of MMC has a dc capacitor. The dc capacitor is expected to perform as a constant dc voltage source for normal operation, but low-frequency ripple exists due to ac current flowing through the capacitor. For modulation methods which assume a constant dc capacitor voltage, like the direct modulation in [1], the generated total submodule voltages in different phase-legs could be different, causing circulating current among the three phases.

Circulating current increases converter power loss and thus should be limited. Rohner *et al.* [15] showed that the dominant component of the circulating current is second-order harmonic. A relatively large arm inductor is required to suppress this low-frequency circulating current. In addition to circulating current suppression, the other main function of the arm inductor is to limit the fault current during a dc side short circuit fault. Therefore, the arm inductance selection principle is mainly determined by the requirement on circulating current suppression and dc short circuit fault current limitation. Tu *et al.* [16] developed the analytical relationship between the arm inductance and second-order circulating current with certain approximations. Ilves *et al.* [17] further improved the accuracy of the relationship with fewer approximations. Also much

effort has been made to understand the impact of the arm inductor on dc short circuit fault current through fault analysis in literature [18]-[19]. The fault current calculation is complex due to the diode rectification stage after detecting the fault and turning off the IGBTs. Zhang *et al.* [18] considered all the possible fault current paths and developed an engineering method to calculate the fault current for each path. Gao *et al.* [19] even observed that among all the possible fault current paths there is one occurs most of the time. So the arm inductance requirement for limiting fault current can be provided by the engineering method in [18], only considering the most potential fault current path. Typically, the arm inductances required by the two criteria are close. Practically, the arm inductance can be selected based on the circulating current suppression requirement, and if it is not enough to limit the fault current, ac side inductance can be increased to meet the requirement.

Several active methods (circulating current suppressing control) have been proposed to suppress the circulating current in MMC [20]-[22]. By implementing the control, the second-order circulating current is largely reduced. The arm inductance requirement based on circulating current suppression is reduced as well, and the design criterion in [16]-[17] is no longer valid. Therefore, the arm inductance should instead be selected based on the fault current requirement. However, the arm inductor is not the only inductor that can limit the dc fault current. The dc and ac side inductors can play the same role. Zhang *et al.* [18] pointed out that minimum fault current does not happen when there is only an arm inductor or ac inductor. Therefore, the arrangement of dc inductor, arm inductor and ac inductor should be reconsidered for a minimized cost target. Furthermore, if fault tolerant submodule like full-bridge is used, much smaller arm inductance is needed to limit the fault current. So it is worthwhile to understand the arm inductance requirement on circulating current suppression considering the active control methods, even

though it is much reduced.

2.1.2 Submodule Capacitor

Submodule capacitor is a key component in MMC, and a driving factor on the converter size, weight and cost. The capacitor need of MMC is much higher than that of the 2-level converter, could be even 10 times higher. So it is important to select the minimized capacitor while satisfying all the criteria. Maximum voltage, voltage ripple and current ripple are three main design criteria for submodule capacitor in MMC [25]. Typically, the maximum voltage and voltage ripple are linked together, as the maximum voltage is the normal capacitor voltage plus voltage ripple. Tang *et al.* [25] demonstrated that the capacitance need by voltage ripple is usually larger than that by ripple current, which makes the voltage ripple the main design criteria for submodule capacitor.

Submodule capacitor voltage ripple is constituted by average ripple and local ripple. The average capacitor voltage ripple is caused by the flowing of arm current. It mainly includes the fundamental frequency component and second-order harmonic. The local ripple is the voltage difference among submodules in each arm. In this thesis, it is also named as "unbalanced voltage", which is defined as twice the maximum difference between a submodule capacitor voltage and the average capacitor voltage. Many references [26]-[29] have established the relationship between submodule capacitance and average capacitor voltage ripple, neglecting the unbalanced voltage. However, the unbalanced voltage is usually not small enough to be neglected [30].

The unbalanced voltage of MMC depends on the voltage-balancing control, which essentially manipulates the currents flowing into the different submodule capacitors to achieve

balanced voltages, by adjusting the inserting instant and duration for each submodule. An effective voltage-balancing control can result in a small unbalanced voltage, but at a cost of higher switching frequency, which directly influences the converter efficiency. So the design of submodule capacitance and converter switching frequency is interconnected. Hassanpoor *et al.* [31] developed the relationship between switching frequency and maximum unbalanced voltage through simulation. However, the simulation based relationship is only valid for one operating condition, and numerous simulations are needed to consider different operating conditions. Also, it lacks a theoretical insight on how these two impact each other.

2.2 MTDC Projects and Testbeds

Even though VSC MTDC system has been proposed and researched for a long while, there are only limited commercial projects. Table 1 lists all the commercial MTDC projects including LCC based until early 2016. Only two more recent projects, Nan'ao and Zhoushan, are VSC based using the MMC topology. Little operation experience has been published, and many practical system control and protection issues still remain. Therefore, a number of scaled VSC MTDC testbeds were developed and reported in [40]-[43], with 4 or 5 terminals. Egea-Alvarez *et al.* [40] developed a 4-terminal testbed with radial connection. The TWENTIES project [41] built a 5-terminal mock-up with a ring connection among 3 terminals. Stoylen *et al.* from Norwegian University of Science and Technology [42] and Wang *et al.* from Cardiff University in UK [43] both built a 4-terminal testbed with star connection. The testbed is a valuable platform for control and protection development, and usually the technology pioneer for developing commercial projects.

Among the commercial projects and all the developed testbeds, the 5-terminal mock-up in

Table 1. MTDC projects list

Project	Commissioning year	Location	Terminal No.	Topology
Italy–Corsica–Sardinia (SACOI) [36]	Phase I:1967 Phase II: 1988	Italy	3	LCC
Hydro-Quebec-New England [37]	Phase I:1986 Phase II: 1992	Canada, USA	5	LCC
Nan'ao [38]	2013	China	3	MMC
Zhoushan [39]	2014	China	5	MMC

[41] is the only one with dc ring topology. All others are either with the simplest radial or star topology. However, ring topology could be most common for the future meshed dc grid. It is important to understand how the MTDC system with ring topology works.

2.3 MTDC DC Fault Protection

DC fault protection is a main challenge for MTDC system. The state-of-the-art method is relying on ac side circuit breaker [44]-[45]. After detecting the fault, ac circuit breakers at all terminals are opened to cut off the fault current from interconnecting ac system, and then fast dc disconnects on the faulted line are used to isolate the fault. The shortcomings with this method are 1) large current stress on diodes because of the long ac circuit breaker opening time, and 2) long system recovery time due to the need to shut down and de-energize the whole dc system. The dc circuit breakers are considered in [46]-[48]. The dc mechanical circuit breaker is similar to the ac counterpart, but needs an extra resonant circuit branch to create current zero crossing.

The opening time is usually around 15~30 ms, which is a little bit faster than the ac circuit breaker. But the fault interruption current capability is limited, and maximum ratings have been realized are 250 kV, 8 kA or 500 kV, 4 kA [46]. Considering the fast rising rate of VSC HVDC system (e.g. 3.5 kA/ms in [12]) and still long opening time, the dc mechanical circuit breaker may not be suitable. Solid state dc circuit breaker has much better performance, which can be opened in μs, and capable to take large fault current [47]. But the drawbacks are large conduction loss and high cost. ABB proposed the hybrid dc circuit breaker, which normally conducts the current through a mechanical switch and is capable to quickly commutate the current to a solid state circuit breaker branch during a fault [12]. It barely has any operation loss like the mechanical switch, and still maintains a fast opening time (~2 ms) by utilizing ultra-fast mechanical switch. However, similar to a pure solid state breaker, the drawback is the high cost. Other alternative methods include using fault tolerant converters which will be discussed in subsection 2.4, and fast dc disconnects. The overall protection strategy is similar to that of utilizing ac circuit breaker. The difference is that fault tolerant converter can cut off the fault current injection from ac system much faster, which can reduce the system recovery time. However, the dc system still needs to be shut down and de-energized, and the cost is higher than ac circuit breaker. Table 2 summarizes the performance of these protection methods, as well as the availability of the protection devices.

The fault protection process has two stages: fault clearance and system recovery. The fault clearance period starts from the time a fault occurs to when the faulted line is cleared, including fault detection and protection device actuation. System recovery period is the rest time until the system is fully recovered. As shown in Table 2, the methods using ac circuit breaker and fault tolerant converter take longer time to clear the fault, due to the need to shut down and deenergize

Table 2. DC fault protection methods comparison

Protection Method	Fault Clear Time	Recovery Time	DC System Shutdown	Availability
Mechanical DC Circuit Breaker (P-RCB)	~ 28 ms [47]	— *	Yes	Yes (Limited current)
Mechanical DC Circuit Breaker (A-RCB)	~ 14 ms [47]	— *	Yes	No
Hybrid DC Circuit Breaker	~ 9 ms [47]	~ 150 ms [48]	Not sure	Near Future
Solid State DC Circuit Breaker	~ 4 ms [47]	— *	Not sure	No **
AC Circuit Breaker + High-Speed DC Mechanical Switch	~ 200 ms [44]	~ 150 ms [44]	Yes	Yes
Fault Tolerant Converter + High-Speed DC Mechanical Switch	~ 150 ms [49]	~ 100 ms [49]	Yes	Near Future

* No literature has provided the recovery time for this protection method

** Solid state dc circuit breaker is usually not preferred due to the high operation loss

the dc system. The recovery process of these two methods is more like a full system restart. With hybrid dc circuit breaker, the system may not need to shut down since the fast fault clearance. The recovery process could also be different as the dc voltage will not drop to zero. These three options are the most practical methods nowadays. Other methods listed in Table 1 are less promising either because of protection devices commercial unavailability in near future or high cost.

Among the three viable protection methods, the one using hybrid dc circuit breaker is the fastest, which is investigated in this thesis. As shown in Table 2, the system recovery process takes most of the time. However, most related research work in literature focuses on fault clearance, and few of them study the system recovery. Chang *et al.* [48] observed the dc system overvoltage issue during the recovery process, and proposed a bump-less control to reduce the overvoltage. But no detailed criteria for converter restart are provided, and they do not address the converter restart sequence issue either.

2.4 Fault Tolerant Converter Topology

As mentioned in subsection 2.3, fault tolerant converter is an alternative option for MTDC dc fault protection. The traditional MMC with half bridge submodule does not have any intrinsic fault current limiting or blocking capability. In case of a dc short circuit fault, the fault current can still flow from the ac side to the faulted dc side through the anti-paralleled diodes of the controllable power switches, even these switches are turned off.

Several converter topologies or solutions have been proposed to provide fault current blocking capability. They are mainly divided into two categories: MMC with different sub-module topologies and hybrid converters. Full-bridge submodule is well known and can be used

to block the fault current [66]. The drawback is double the number of semiconductor devices and increased conduction loss. Marquart [66] further proposed a "clamp-double" submodule which uses less semiconductor devices and has less loss compared to the full-bridge submodule. The shortcoming is the provided reverse voltage is half of that by the full-bridge submodule. Some other proposed topologies include cross-connected submodule in [67], unipolar-voltage full-bridge submodule and three-level cross-connected submodule in [68], and two new topologies in [69]. Qin *et al.* [68] compared most of the possible topologies, in which the "clamp-double" submodule has the lowest loss and minimum semiconductor devices. Full-bridge submodule on the other hand may cost most, but it has the best performance as shown in [70].

Alstom proposed a hybrid multilevel converter called alternate-arm multilevel converter [71]. It uses the full-bridge submodule as the basic cell to construct the multilevel voltages, but also adopts the two-level converter concept with a director switch made of series power switches for each arm. The efficiency of the proposed topology could be close to that of the traditional MMC based on half-bridge submodule. But a major challenge is to balance the submodule capacitor voltages, which may limit the converter operating range. Also it requires the direct series of semiconductor devices.

Adam *et al.* [72] proposed a hybrid cascaded MMC topology, which basically is a two-level converter with an active filter, constructed by a series of full-bridge submodules. The use of full-bridge submodule enables the fault current blocking capability. In addition, due to the implementation of an active filter, the main two-level converter can operate at a low switching frequency, reducing the power loss as a result. However, the two-level converter still under high voltage pressure, which requires the series of semiconductor devices. Furthermore, the capacitor need is also larger than the traditional MMC.

2.5 Research Objectives

According to the survey above, there are many unsolved issues on the development of MMC-based MTDC system. The main challenges include:

(1) Arm inductance design considering circulating current suppression control.

(2) Submodule capacitance design considering the unbalanced voltage.

(3) Limited MTDC testbed and limited demonstrated control and operation scenarios.

(4) DC fault protection strategy with detailed criteria and considering the recovery process.

(5) Fault tolerant converter with comparable efficiency to the half-bridge MMC.

Corresponding to the challenges listed above, the main tasks of this dissertation are:

(1) Reveal the limiting factor of arm inductance selection after implementing the circulating current suppression control, and develop the theoretical arm inductance selection criterion.

(2) Develop the analytical relationship between submodule capacitance and capacitor unbalanced voltage.

(3) Build a four-terminal HVDC testbed with a dc ring topology, and demonstrate the most typical operation scenarios.

(4) Propose a systematic dc fault protection strategy of MTDC utilizing hybrid dc circuit breaker, including detailed criteria and methods for system recovery process.

(5) Propose a new topology with dc fault blocking capability, together with the same high efficiency as half-bridge MMC.

3 MMC Arm Inductance Design

In this chapter, the arm inductance requirement for circulating current suppression in MMC is investigated after implementing the active circulating current suppression control. With circulating current suppressing control, the dominant second-order circulating current in MMC can be effectively decreased, and the arm inductance requirement based on the circulating current is thus reduced. The circulating current at switching frequency is found to be the new limitation for arm inductance design. The theoretical relationship between switching frequency circulating current and arm inductance is further developed. Finally, the theoretical analysis and calculation are verified by the experiment.

3.1 MMC Operating Principle

Figure 3-1 shows a single-phase equivalent circuit of the MMC. The series connection of submodules in each arm is represented by a controllable voltage source (v_{up} and v_{low} for upper and lower arms, respectively). The relationships between ac and dc terminal voltages (v_g and v_{dc}) are expressed as

$$v_g = \frac{v_{low} - v_{up}}{2} - \frac{L_{arm}}{2}\frac{di_{ac}}{dt} \tag{3-1}$$

$$v_{dc} = v_{up} + v_{low} + 2L_{arm}\frac{di_{cm}}{dt} \tag{3-2}$$

where i_{cm} is the common mode component of the upper and lower arm currents, which is

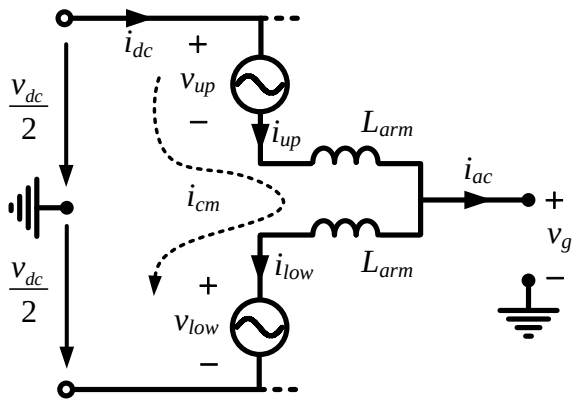


Figure 3-1. Single-phase equivalent circuit of the MMC.

$$i_{cm} = \frac{i_{up} + i_{low}}{2}. \tag{3-3}$$

The ac voltage v_{ac} and current i_{ac} are defined as

$$v_{ac} = \frac{v_{low} - v_{up}}{2} = V_{ac}\, cos(\omega t) \tag{3-4}$$

$$i_{ac} = i_{up} - i_{low} = I_{ac}\, cos(\omega t + \phi) \tag{3-5}$$

where ϕ represents the phase difference between v_{ac} and i_{ac}.

Based on (3-2) and (3-4), the upper and lower arm voltages are similarly given as

$$v_{up} = \frac{V_{dc}}{2} - V_{ac}\, cos(\omega t) \tag{3-6}$$

$$v_{low} = \frac{V_{dc}}{2} + V_{ac}\, cos(\omega t) \tag{3-7}$$

The key of MMC operation is to generate the desired arm voltages by inserting or bypassing

submodules. The number of submodules to be inserted is determined by modulation, and different modulation schemes have been proposed in the literature [23]. The direct modulation is a most popular scheme and considered here. The insertion indices, which is the ratio of the inserted submodule number to total submodule number in each arm, can be obtained as

$$n_{up} = \frac{V_{dc}}{2NV_c}(1 - M\,cos(\omega t)) = \frac{1}{2}(1 - M\,cos(\omega t)) \tag{3-8}$$

$$n_{low} = \frac{V_{dc}}{2NV_c}(1 + M\,cos(\omega t)) = \frac{1}{2}(1 + M\,cos(\omega t)) \tag{3-9}$$

where N is the total number of submodules per arm, M is the modulation index defined as $2V_{ac}/V_{dc}$ and V_c is the average submodule capacitor voltage, which usually is

$$V_c = \frac{V_{dc}}{N} \tag{3-10}$$

Eqs. (3-8), (3-9) and (3-10) give the number of how many submodules to be inserted, but do not tell which specific submodules should be inserted. Different arrangements of inserted submodules have little impact on the overall arm voltages, but could cause capacitor voltage unbalance issue among submodules. Therefore, the submodule selection algorithm is usually included in the voltage balancing control in MMC. In this chapter, the submodule capacitor voltages are assumed ideally balanced.

3.2 Circulating Current Suppression Control

The direct modulation obtains insertion indices by assuming a constant submodule capacitor voltage, however, the actual capacitor voltage varies due to the current flow. So by using the insertion indices in (3-8) and (3-9), the generated arm voltages can be expressed as

$$v_{up\_real} = N\left(\frac{1}{2} - \frac{M}{2}cos(\omega t)\right) \cdot v_{up\_c\_real} \tag{3-11}$$

$$v_{low\_real} = N\left(\frac{1}{2} + \frac{M}{2}cos(\omega t)\right) \cdot v_{low\_c\_real} \tag{3-12}$$

where $v_{up\_c\_real}$, $v_{low\_c\_real}$ are the actual submodule capacitor voltages. Ilves *et al.* [17] analyzed the harmonic components of the capacitor voltage, and gave the expression of arm voltages as

$$v_{up\_real} = \frac{v_{dc}}{2}(1 - M\,cos(\omega t)) + v_{cir} \tag{3-13}$$

$$v_{low\_real} = \frac{v_{dc}}{2}(1 + M\,cos(\omega t)) + v_{cir}. \tag{3-14}$$

where v_{cir} is the voltage difference compared to the desired arm voltage. The phase-leg voltage is given as

$$v_{ph\_real} = v_{dc} + 2v_{cir}. \tag{3-15}$$

The phase-leg voltage is not equal to the dc side voltage, and the voltage difference ($2v_{cir}$) is applied on the two arm inductors, causing the circulating current. The harmonics of the circulating current have been analyzed in [17], showing that the second-order harmonic is the dominant component.

Different circulating current suppression control methods have been proposed, but the essential principles are generally the same, and the method introduced by Tu *et al.* [21] is considered in this dissertation. A common mode component (v_{cm}) is added to the arm voltage reference in (3-8) and (3-9) in order to compensate for the submodule capacitor voltage variation.

The insertion indices are thus changed to

$$n_{up\_real} = \frac{1}{2} - \frac{M}{2} cos(\omega t) - n_{cm} \tag{3-16}$$

$$n_{low\_real} = \frac{1}{2} + \frac{M}{2} cos(\omega t) - n_{cm} \tag{3-17}$$

where n_{cm} is the common mode component added to the insertion indices, and defined as $2v_{cm}/V_{dc}$. Using these insertion indices, the generated arm voltages are

$$v_{up\_real} = N\left(\frac{1}{2} - \frac{M}{2} cos(\omega t) - n_{cm}\right) \cdot v_{up\_c\_real} \tag{3-18}$$

$$v_{low\_real} = N\left(\frac{1}{2} + \frac{M}{2} cos(\omega t) - n_{cm}\right) \cdot v_{low\_c\_real}. \tag{3-19}$$

Compared to (3-13) and (3-14), the arm voltages can be rewritten as

$$v_{up\_real} = \frac{v_{dc}}{2}(1 - M\, cos(\omega t)) + v_{cir} - n_{cm} \cdot v_{up\_c\_real} \tag{3-20}$$

$$v_{low\_real} = \frac{v_{dc}}{2}(1 + M\, cos(\omega t)) + v_{cir} - n_{cm} \cdot v_{low\_c\_real}. \tag{3-21}$$

The phase-leg voltage is thus derived as

$$v_{ph\_real} = v_{dc} + 2v_{cir} - n_{cm} \cdot \left(v_{c\_up} + v_{c\_low}\right). \tag{3-22}$$

According to (3-22), the phase-leg voltage may equal to the dc voltage by controlling n_{cm}. Theoretically, the circulating current harmonics lower than the bandwidth of the MMC inner controller can be eliminated. As stated previously, second-order harmonic component dominates the circulating current, whose frequency is much lower than the controller bandwidth.

3.3 Switching Frequency Circulating Current

The circulating current suppressing controller can effectively eliminate the second-order harmonic, however not the higher frequency harmonic like the switching frequency, which is out of the bandwidth of the controller. The switching frequency circulating current can only be limited by the arm inductors. This section will explain the mechanism of the switching frequency circulating current, and provides the selection criterion for arm inductance.

The modulation scheme analyzed in this section has a PWM submodule. Figure 3-2 shows the pulse-width voltages generated for the PWM submodules. The reference voltages are compared with the triangular carriers to decide whether the submodules should be inserted or bypassed. The triangular carriers for the upper and lower arms are complementary. The reference voltages are actually the representation of the insertion indices. When circulating current suppressing control is not implemented, the sum of insertion indices for the upper and lower equals to 1 based on (3-8) and (3-9), which means there are N submodules always inserted in a phase-leg. Thus the voltages of PWM sub-modules in the upper and lower arms are complementary. Based on (3-13) and (3-14), the resulting phase-leg voltage is not equal to the dc voltage and the voltage difference is $2v_{cir}$. The difference between the phase-leg voltages of stages I, III and stage II is because of the submodule capacitor voltage difference in the upper and lower arms.

Because the circulating current suppressing controller introduces a common mode component into the insertion indices, the voltages of PWM submodules in the upper and lower arms are no longer complementary, but have an overlap as shown in Figure 3-2. Additional submodules would be inserted or bypassed in the circuit based on the sign of n_{cir} during the overlap period, which means it is not always N submodules inserted in a phase-leg. The phase-

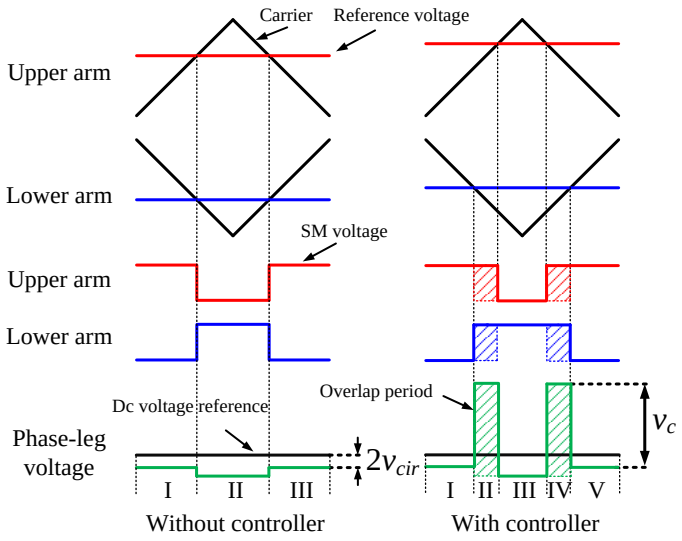


Figure 3-2. Voltage generation of PWM sub-modules

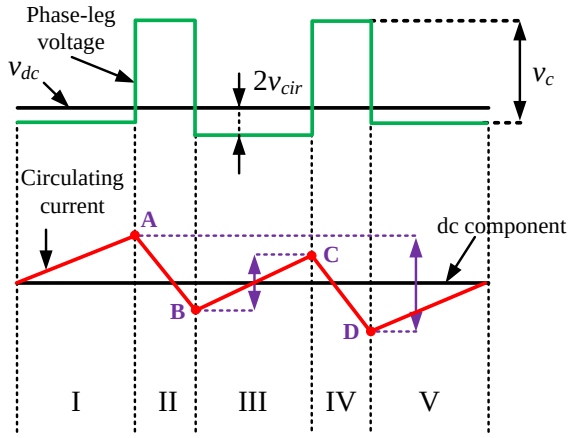


Figure 3-3. Phase-leg voltage and circulating current in a switching period

leg voltage could have two pulses with magnitude of v_c in each switching period due to the circulating current suppressing control. Figure 3-3 shows the resulting phase-leg voltage with the circulating current suppressing controller and the corresponding circulating current in one switching period. In Figure 3-3, a switching cycle is divided into 5 stages. Stages II and IV represent the overlap periods, and the phase-leg voltages in these two periods are v_c higher than the voltages in the other periods. The phase-leg voltages in stages I, III and V are nearly the same. The voltage difference between them to the dc voltage is $2v_{cir}$, as shown in (3-15). If without the circulating current suppressing controller, the phase-leg voltages in stages II and IV should be similar to other periods, and the circulating current either keeps increasing or decreasing in the whole switching cycle, causing the second-order line frequency circulating current.

But with the circulating current suppressing controller, the voltages in stages II and IV can compensate for the voltage differences in the other three periods and make the average value of the phase-leg voltage in each switching cycle equal to the dc voltage. The second-order circulating current is thus eliminated, but the switching frequency circulating current appears as a side effect. As shown in Figure 3-3, in order to calculate the switching frequency circulating current, the voltage difference between the phase-leg voltage and dc voltage should be obtained. Based on [17], v_{cir} can be derived as

$$v_{cir} = \frac{N}{8C_{sub}}\left\{-\frac{3}{4\omega}M \cdot I_{ac} \cdot \sin(2\omega t - \theta) + \frac{1}{3\omega}M^2 I_{dc} \cdot \sin(2\omega t)\right\} \qquad (3\text{-}23)$$

As shown in Figure 3-3, the peak current would occur either at points A and D, or at B and C, determined by the length of periods I, V, and III. Considering the overlap periods are relatively small, and the longest time period among I, V, and III can thus be derived as

$$\Delta T = max(\, D_{ap\_real}\,,\quad D_{an\_real}) \cdot T_s \tag{3-24}$$

where T_s is the switching period. Thus the peak to peak value of the switching frequency circulating current can be derived as

$$I_{pp} = \frac{v_{cir}}{L_{arm}} \cdot \Delta T. \tag{3-25}$$

In order to design the arm inductance, the worst case with maximum switching frequency circulating current should be identified. Assuming the maximum modulation index is 1, the maximum v_{cir} can be derived as

$$v_{cir\_max} = \frac{N}{8\omega C_{sub}} \sqrt{\frac{9}{16} I_{ac}^2 + \frac{1}{9} I_{dc}^2 - \frac{1}{2} I_{ac} I_{dc}}. \tag{3-26}$$

As shown in Figure 3-3, the largest ΔT would be T_s. Thus the maximum switching frequency circulating current is obtained as

$$I_{pp\_max} = \frac{N \cdot T_s}{8\omega L_{arm} C_{sub}} \sqrt{\frac{9}{16} I_{ac}^2 + \frac{1}{9} I_{dc}^2 - \frac{1}{2} I_{ac} I_{dc}}. \tag{3-27}$$

It shows that the switching frequency circulating current is related to both the arm inductance and submodule capacitance. The sub-module capacitance is mainly designed by its voltage ripple requirement, which will be presented in next chapter. Then, the arm inductance requirement based on the switching frequency circulating current can be derived.

3.4 Experimental Verification

A three-phase MMC with 2 submodules per arm is developed to verify the analysis on the switching frequency circulating current. As shown in Figure 3-4, it is connected to a constant dc voltage source, and operates in inverter mode. The ac side is connected to a passive load bank that consists of resistors and inductors. The detailed hardware parameters are listed in Table 3.

The prototype has two control units, including a TI TMS320F28335 DSP and an Altera Cyclone III FPGA. The DSP is the main controller, responsible for ac current/voltage control and circulating current control. The arm voltage reference is generated in the DSP, and then sent to FPGA. Used as an auxiliary controller, the FPGA executes the voltage-balancing control and generates PWM signals.

Figure 3-5 shows the experimental results when arm inductance is 1 mH at rated conditions. The circulating current suppression control is disabled, and the result shows a large second-order circulating current. Figure 3-6 shows the test result with enabled circulating current suppression controller. It can be seen clearly that the second-order circulating current is almost eliminated. Figure 3-5 and Figure 3-6 also show the two capacitor voltages in one arm. They are nearly the same, which validates the effectiveness of the voltage-balancing control.

Table 3. Experimental parameters of the MMC prototype

Rated power	1 kW	Rated ac frequency	60 Hz
Rated dc voltage	100 V	submodule capacitor voltage	50 V
Rated ac current	10 A	Submodule capacitance	2.7 mF

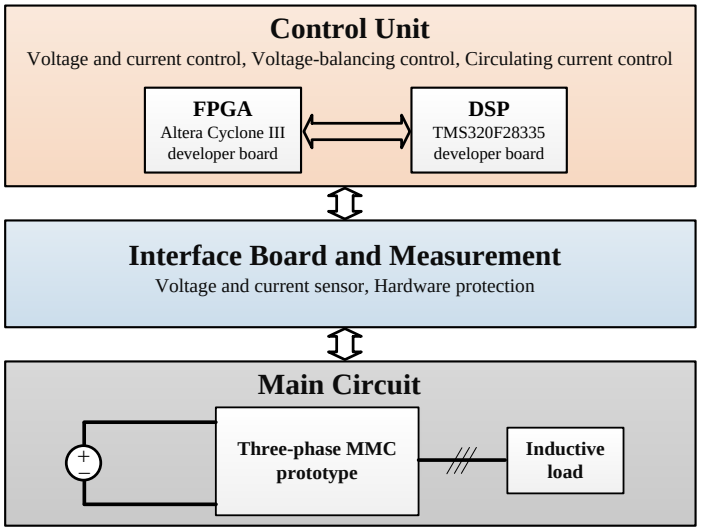


Figure 3-4. System configuration of the experimental setup of the MMC prototype

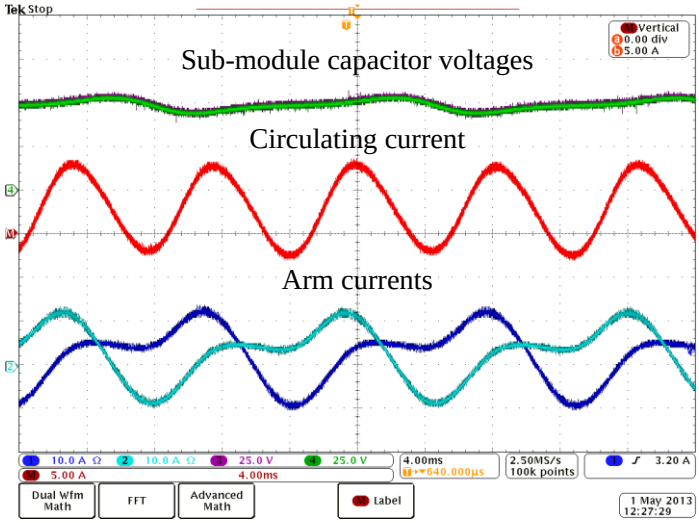


Figure 3-5. Experimental results at $L_{arm} = 1$ mH with circulating current suppressing control disabled

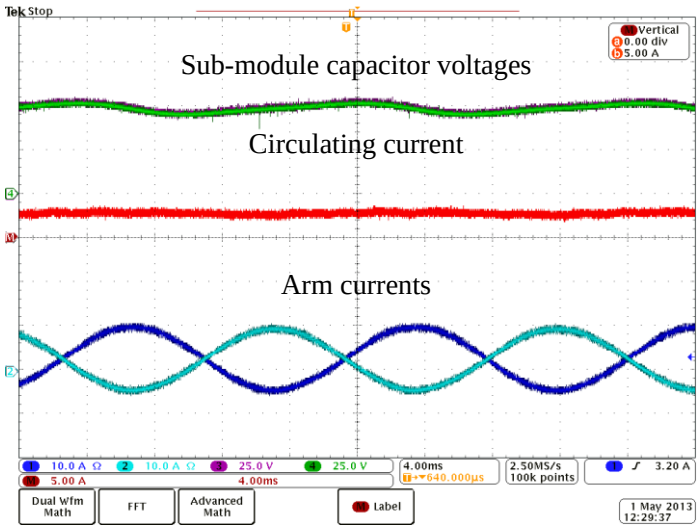


Figure 3-6. Experimental results at $L_{arm} = 1$ mH with circulating current suppressing control enabled

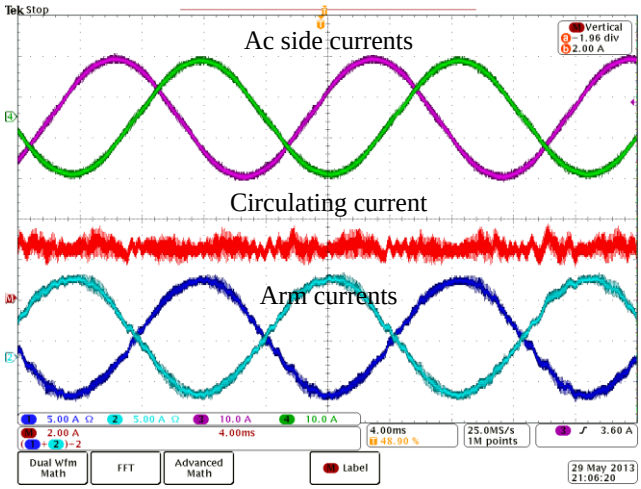


Figure 3-7. Experimental results at $L_{arm} = 0.1$ mH with circulating current suppressing control enabled

Figure 3-7 shows the experimental result with 0.1 mH arm inductor, which is 1/10 of that in Figure 3-6. The circulating current contains high frequency harmonics. Figure 3-8 shows the waveform with a small time scale of circulating current and the corresponding phase-leg voltage. The waveform matches the theoretical analysis in Figure 3-3, validating the existence of the switching frequency circulating current.

Tests have been conducted for different arm inductors. Figure 3-9 shows a comparison of the theoretical and experimental values of the maximum peak to peak switching frequency circulating currents with different arm inductors. The experimental results have a close agreement with the calculation.

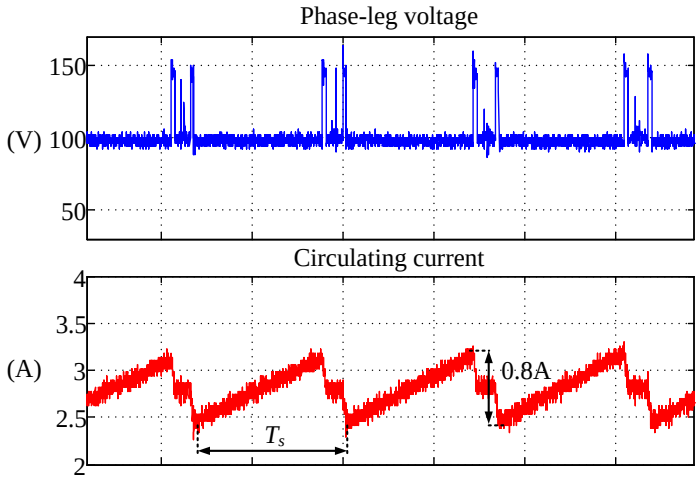


Figure 3-8. Experimental results at $L_{arm} = 0.1$ mH with circulating current suppressing control enabled

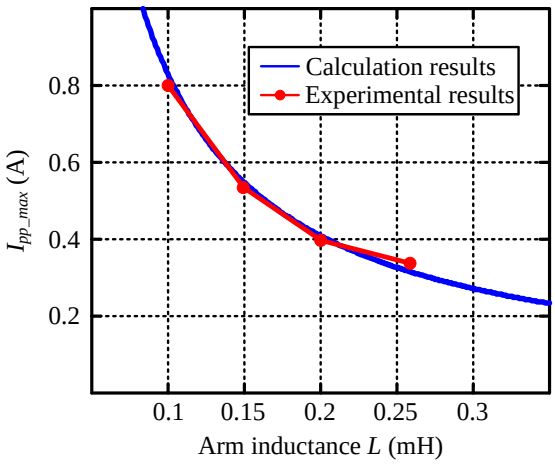


Figure 3-9. Maximum switching frequency circulating current versus arm inductance

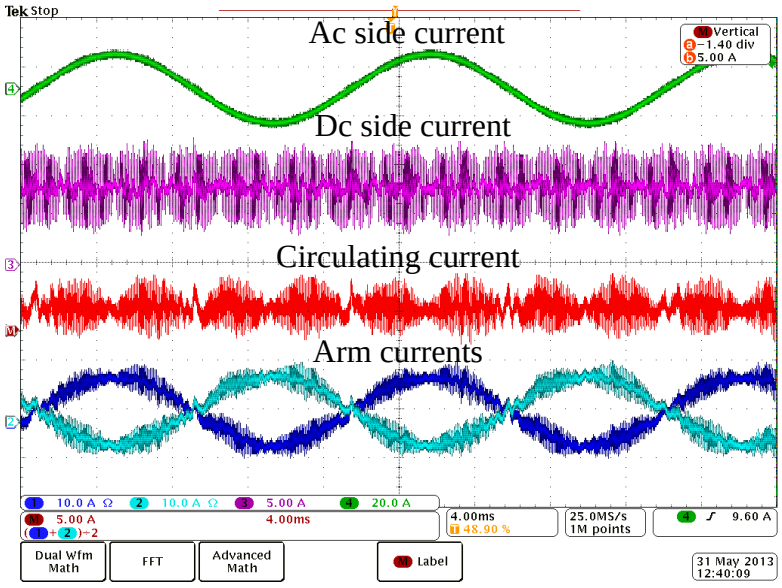


Figure 3-10. Experimental results at $L_{arm} = 0.015$ mH with circulating current suppressing control enabled

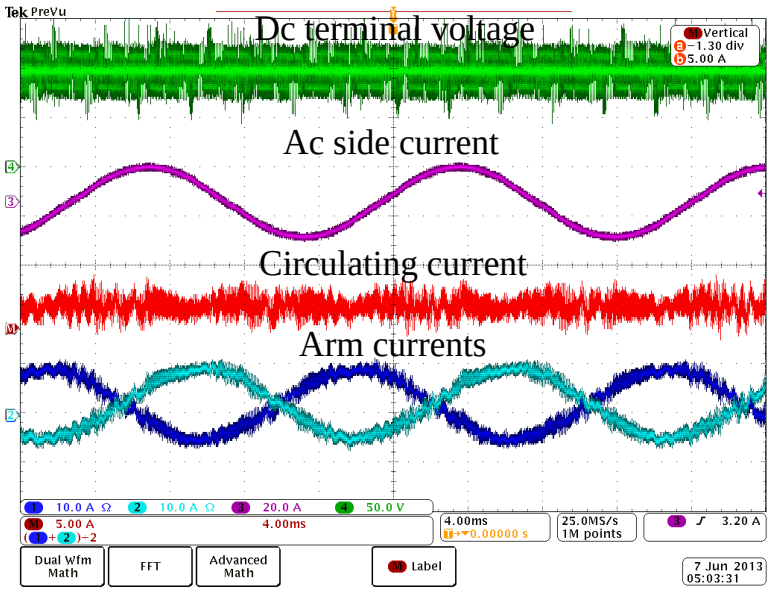


Figure 3-11. Experimental results at $L_{arm} = 0.015$ mH with circulating current suppressing control enabled and a 1 mH dc inductor

Figure 3-10 shows the experimental result with an extremely small arm inductance of 15 uH. The switching frequency circulating current is further increased, and more importantly the circulating current may not just flow among three phases, it also goes to the dc side as shown in the waveform. And if the dc side has inductors, the MMC dc terminal voltage will also have the switching frequency harmonics, as shown in Figure 3-11 with a 1 mH dc inductor. The ripple voltage could be as high as 2/3 of the submodule capacitor voltage [24]. Therefore additional dc filter may be required, if extra small arm inductor is used.

3.5 Conclusion

The dominant second-order circulating current in MMC can be theoretically eliminated after the implementation of the circulating current suppressing control, but a switching frequency

circulating current is produced in turn. The theoretical analysis presented in this chapter shows that the switching frequency circulating current has a dependence on the arm inductance and the submodule capacitance, and the arm inductance requirement based on the switching frequency circulating current limit can thus be derived. Finally, the experimental results of a down-scaled prototype verify both the existence of the switching frequency circulating current and its relationship with the arm inductance.

4 MMC Submodule Capacitance Design

As has been discussed in subsection 2.1.2, the unbalanced voltage should be considered for MMC submodule capacitance design. It is related to the voltage-balancing control, or fundamentally depends on the converter switching frequency. This chapter develops the analytical relationship between the unbalanced voltage and submodule capacitance, considering the voltage-balancing control impact. Two boundary criteria for submodule capacitance design are derived.

4.1 Voltage-Balancing Control

According to the operating principle description in subsection 3.1, the total number of submodules to be inserted in each arm is given by the insertion index multiplied by the submodule number in each arm. If the number is not an integer, the closest integer is used based on the nearest-level modulation as considered in this paper, which is a commonly adopted method in MMC [1]. The insertion index does not indicate which individual submodule should be inserted. The phase-shifted method may be used to predefine a sequence for submodule selection as in [32]-[33], or else an active selection method is required to dynamically assign submodule switching states. The active selection method is usually integrated in voltage-balancing control. In this dissertation, the modified sorting method in [34] is considered. The algorithm is shown in the flowchart in Figure 4-1. Similar to the traditional sorting method in [1], this method has improved to avoid unnecessary switching actions. The submodule switching states only vary under the following two cases:

Case 1): The unbalanced voltage is larger than the predefined threshold value (V_{th});

Case 2): The number of submodules to be inserted has changed.

The submodules selected to change switching states for case 1 depend on the arm current direction. If the current charges the capacitors in that arm, the submodule with the highest capacitor voltage is bypassed and the submodule with the lowest capacitor voltage is inserted. If the current discharges the capacitors in that arm, the submodule with the lowest capacitor voltage is bypassed and the submodule with the highest capacitor voltage is inserted. This is the same as in the traditional sorting algorithm. For case 2, an additional submodule will be inserted or bypassed. The selection of this submodule is similar to case 1. This modified sorting method with an unbalanced capacitor voltage threshold is commonly used in MMC, due to its easy implementation and reduced switching loss.

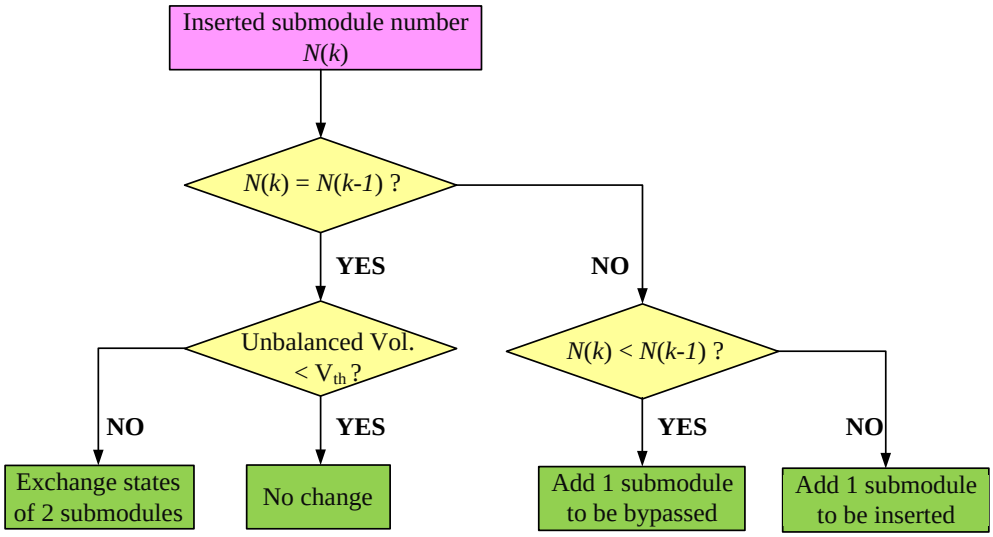


Figure 4-1. Modified sorting algorithm [34]

4.2 Unbalanced Voltage Derivation

The MMC operation relies on generating desired arm voltages. As described in subsection 3.1, the insertion indices are obtained based on the assumption that all submodule capacitor voltages are equal. Otherwise, the resulting arm voltages using these insertion indices will not equal to the reference value. Voltage-balancing control is used to balance the capacitor voltages, but in most cases it cannot achieve instantaneous balance. It is expected that there will be an instantaneous arm voltage error, but voltage-balancing control should keep this error close to zero. In other words, voltage-balancing control can compensate for the arm voltage error and achieve an approximately zero accumulated arm voltage error for a longer time period (i.e. one fundamental cycle).

The arm voltage reference in the following section is approximated by the arm voltage value with the assumption that MMC operates with instantaneously balanced submodule capacitor voltages. And since the effect of circulating current control on insertion indices is relatively small, Equations (3-8) and (3-9) are used in this section. Only the upper arm is considered due to the symmetry between the upper and lower arms.

4.2.1 Arm Voltage Error

The actual arm voltage v_{up_act} is the sum of capacitor voltages for all inserted submodules, that is

$$v_{up\_act} = Nn_{up}\bar{v}_{sub\_act} \tag{4-1}$$

where $\bar{v}_{sub\_act}$ denotes the average capacitor voltage of the inserted submodules. For the instantaneously balanced case, all capacitor voltages are the same. The arm voltage reference

v_{up_ref} can be rewritten as

$$v_{up\_ref} = Nn_{up}v_{sub\_ref} \tag{4-2}$$

where v_{sub_ref} represents the submodule capacitor voltage reference. The instantaneous error between the arm voltage reference and the actual voltage is obtained as

$$v_{up\_err} = Nn_{up}\left(\bar{v}_{sub\_act} - v_{sub\_ref}\right). \tag{4-3}$$

With nearest-level modulation, the whole fundamental cycle is divided into many small time intervals, in which the inserted submodule number remains constant. The increment of arm voltage error for each time interval is derived as

$$dv_{up\_err}(t) = Nn_{up}\left(d\bar{v}_{sub\_act}(t) - dv_{sub\_ref}(t)\right). \tag{4-4}$$

Practically, only the capacitor voltages of those inserted submodules will change and the bypassed submodules' capacitor voltages remain the same. For the instantaneously balanced case, all the submodule capacitors in the arm experience the same voltage change. As the total capacitor charge variation is the same for both cases, that is

$$Nn_{up}(t)d\bar{v}_{sub\_act}(t) = Ndv_{sub\_ref}(t). \tag{4-5}$$

The capacitor voltage reference is obtained based on the average model in [17], and its increment for a small time interval is given as

$$dv_{sub\_ref}(t) = \frac{1}{C_{sub}}n_{up}(t)i_{up}(t)dt. \tag{4-6}$$

Inserting (4-5) and (4-6) into (4-3) gives the expression of the arm voltage error

$$dv_{up\_err}(t) = \frac{N}{C_{sub}} n_{up}(t)\left[1 - n_{up}(t)\right] i_{up}(t) dt. \tag{4-7}$$

Integrating (4-7) over a fundamental cycle T yields

$$\int_0^T dv_{up\_err}(t) = \frac{N}{C_{sub}} \frac{I_{dc}}{12} \left(1 - \frac{M^2}{2}\right) T \tag{4-8}$$

which indicates that there will be a constant arm voltage error during each fundamental cycle. Therefore, voltage-balancing control should be employed to compensate this error.

4.2.2 Effect of Voltage-Balancing Control on Arm Voltage Error Compensation

Based on the voltage-balancing control algorithm described above, the submodule switching states will change under the two cases as described in subsection 4.1.

Case 1, when the unbalanced voltage is larger than the threshold value, leads to an exchange of switching states between the two submodules with highest and lowest capacitor voltages. The voltage difference between these two submodules is added to the arm voltage. Due to the voltage-balancing control, the maximum voltage difference among capacitors should be around V_{th} and the arm voltage variation caused by an exchange of switching states is V_{th}. The arm voltage error shown in (4-7) has the same polarity as the arm current; but the arm voltage variation introduced for this case has the opposite polarity, which is given as

$$\Delta v_{com1} = -V_{th}. \tag{4-9}$$

Therefore, this switching event actually compensates for the arm voltage error.

When an additional submodule is inserted or bypassed in case 2, the arm voltage is either

increased or decreased by the selected submodule's capacitor voltage. For the instantaneously balanced case, the arm voltage variation is the average capacitor voltage. It is clear that this switching event also compensates for the arm voltage error, and the compensated voltage is half of the unbalanced voltage of the selected submodule. For example, if arm current is charging the capacitor and an additional submodule is required to be inserted. The voltage-balancing control algorithm selects the submodule in "bypassed" mode with the lowest capacitor voltage. If there are many submodules in "bypassed" mode, the compensated arm voltage should be around half of V_{th}, that is

$$\Delta v_{com2} = -\frac{V_{th}}{2}. \tag{4-10}$$

However, if only a few submodules are in "bypassed" mode, the compensated arm voltage is smaller than that. During a fundamental cycle, both scenarios will occur, and the average compensated arm voltage should have the boundaries

$$0 < \left|\Delta v_{com2\_avg}\right| < \frac{V_{th}}{2}. \tag{4-11}$$

The compensated arm voltage during a fundamental cycle is obtained as

$$v_{com\_T} = \Delta v_{com1} N_{sw1} + \Delta v_{com2\_avg} N_{sw2} \tag{4-12}$$

where N_{sw1} and N_{sw2} represent the total switching transitions in a fundamental cycle for cases 1 and 2, respectively. The average switching frequency can then be expressed as

$$f_{sw} = \frac{(N_{sw1} + N_{sw2})}{2N}\frac{1}{T}. \tag{4-13}$$

As explained above, the compensated arm voltage should approximately equal to the arm

voltage error over a fundamental cycle, that is

$$v_{com\_T} + \int_0^T \left| dv_{up\_err}(t) \right| = 0. \tag{4-14}$$

Due to the defined polarity of the compensated arm voltage, the absolute value of the arm voltage error in (4-7) is used. Substituting (4-9)-(4-13) into (4-14) yields two boundary equations

$$f_{sw} V_{th} > \frac{1}{T} \int_0^T \left| \frac{1}{C_{sub}} n_{up} (1 - n_{up}) i_{up} \right| dt \tag{4-15}$$

$$f_{sw} V_{th} < f_m V_{th} + \frac{1}{T} \int_0^T \left| \frac{1}{C_{sub}} n_{up} (1 - n_{up}) i_{up} \right| dt \tag{4-16}$$

which describe the relationship between the average switching frequency and unbalanced capacitor voltage threshold. The difference between the upper and lower boundaries is $f_m V_{th}$, where f_m is the switching frequency required by modulation. It can be calculated as

$$f_m = M f_0. \tag{4-17}$$

where f_0 is the fundamental line frequency.

4.3 Submodule Capacitance Design Consideration

4.3.1 Boundary Criteria

As mentioned previously, it includes the average ripple and unbalanced voltage. The relationship between the average ripple and submodule capacitance was derived in [27], that is

$$V_{ripple\_avg} = \frac{1}{C_{sub}} \frac{1}{4\omega} I_{ac} \left(1 - \left(\frac{M}{2}\cos\phi\right)^2\right)^{\frac{3}{2}}. \tag{4-18}$$

Some references determine the submodule capacitance requirement by ignoring the unbalanced voltage, which is valid if the unbalanced voltage is much smaller than the average ripple. However, this may not be the practical case. The derived relationships in (4-15) and (4-16) show that the unbalanced voltage increases when the switching frequency is low. Jacobson *et al.* [35] suggests that the practical switching frequency for MMC in a HVDC application is around 150 Hz. Figure 4-2 shows the waveforms of the submodule capacitor voltages when the switching frequencies are 100 Hz, 200 Hz and 3.3 kHz, respectively. For the well balanced case at 3.3 kHz switching frequency, all the capacitor voltages have approximately the same voltage variation ΔV_1, which equals to the average ripple $V_{\text{ripple\_avg}}$. For the poorly-balanced case like at 100 Hz switching frequency, the capacitor voltage variation is increased to ΔV_1+ΔV_2, where ΔV_2 is the unbalanced voltage and should be equal to V_{th}. As shown in Fig. 9, ΔV_2 is around 30% of ΔV_1 when the switching frequency is 200 Hz and increased to 60% when the switching frequency decreases to 100 Hz. This indicates that the unbalanced voltage should not be ignored in the low switching frequency case. Combining (4-15), (4-16) and (4-18) gives two boundary equations for the total submodule capacitor voltage ripple, which are

$$V_{ripple\_total} > \frac{1}{C_{sub}} \left\{ \frac{1}{f_{sw}} \frac{1}{T} \int_0^T \left| n_{up}(1 - n_{up}) i_{up} \right| dt + \frac{1}{4\omega} I_{ac} \left(1 - \left(\frac{M}{2}\cos\phi\right)^2\right)^{\frac{3}{2}} \right\} \tag{4-19}$$

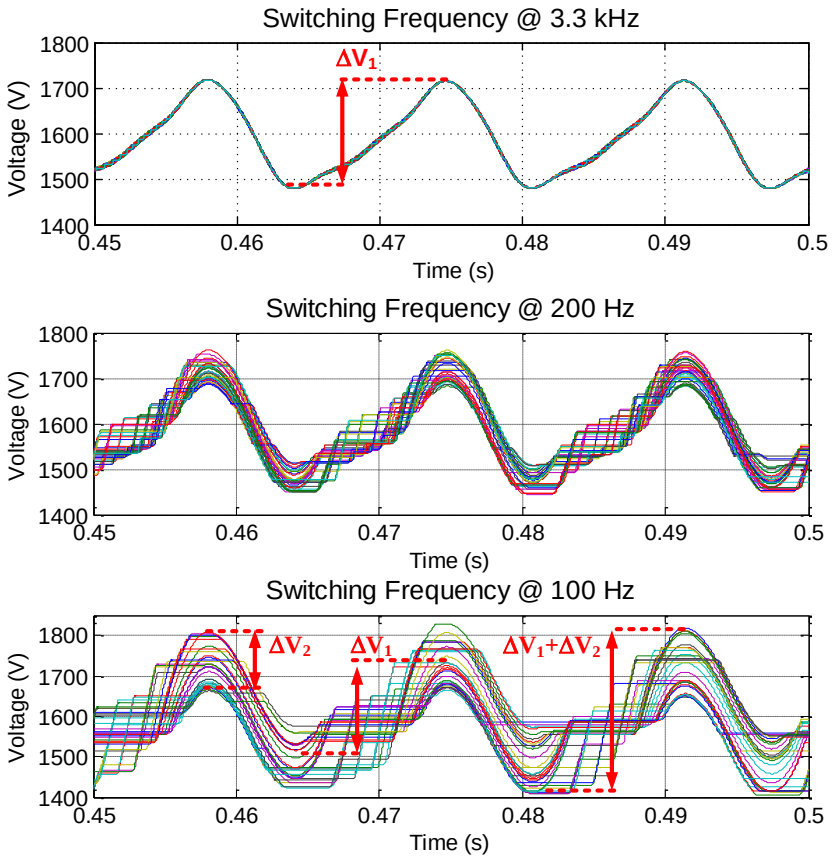


Figure 4-2. Simulation waveforms of submodule capacitor voltages at different switching frequency.

$$V_{ripple\_total} < \frac{1}{C_{sub}}\left\{\frac{1}{f_{sw}-f_m}\frac{1}{T}\int_0^T \left|n_{up}\left(1-n_{up}\right)i_{up}\right|dt + \frac{1}{4\omega}I_{ac}\left(1-\left(\frac{M}{2}\cos\phi\right)^2\right)^{\frac{3}{2}}\right\}. \quad (4\text{-}20)$$

These two boundary equations can be used for submodule capacitance design.

4.3.2 Unbalanced Voltage Selection

In order to choose a reasonable unbalanced voltage, its impact on converter design and operation needs to be understood. It has been shown that the unbalanced voltage impacts 1) converter switching frequency, and 2) submodule capacitor voltage ripple. The converter switching frequency will impact the power loss, while the capacitor voltage ripple is related to the submodule voltage rating. Both of them are important design specifications. However, there are several other important aspects, which have not been considered, including 3) voltage and current harmonics, and 4) converter normal operation.

- Impact on voltage and current harmonics

Higher unbalanced voltage means larger deviation of submodule capacitor voltage. It will cause higher distortion of the arm voltage, which is the sum of the capacitor voltages of inserted submodules. The distorted arm voltage, on the other hand, impacts the alternating voltage and current. Figure 4-3 shows the total harmonic distortion (THD) comparison of the ac voltage/current, as well as the arm voltage/current, with different threshold voltages in simulation. The results show that, in general, higher threshold voltage leads to slightly higher distortions for both alternating voltage/current and arm voltage/current.

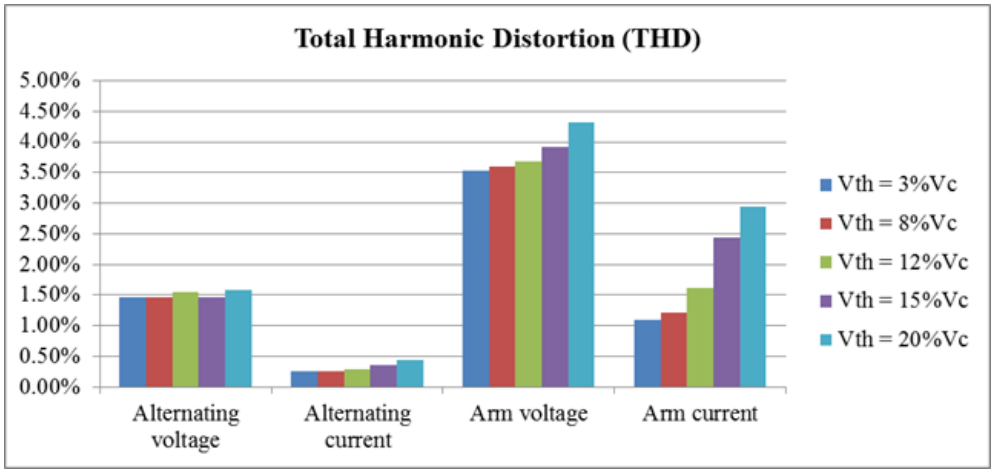


Figure 4-3. Harmonic comparison in simulation with 32 submodules per arm.

IEEE standard 519 defines several harmonic requirements for alternating voltage and current. The THD limits of a > 161 kV system are defined as 1.5% and 1% for the voltage and current, respectively. Based on the results in Figure 4-3, the THD of ac voltage is close to or even above the limit while the current stays within the predefined limits. So the slight difference on ac voltage distortion, caused by the unbalanced voltage, is important. However, the harmonics are also related to the submodule number. Figure 4-4 shows the same THD comparison, but for a scaled system with double submodule number (64 submodules per arm) in simulation. It also shows that higher unbalanced voltage leads to higher distortion. Compared to Figure 4-3, the overall THDs are much smaller due to the larger submodule number, and both the ac voltage and current harmonics are well below the limits. So the impact of unbalanced voltage on harmonics is not that important for larger submodule number cases.

In HVDC applications, different manufacturers may adopt different submodule numbers for their products. For example, Siemens HVDC plus has 200 submodules per arm for a ±160 kV

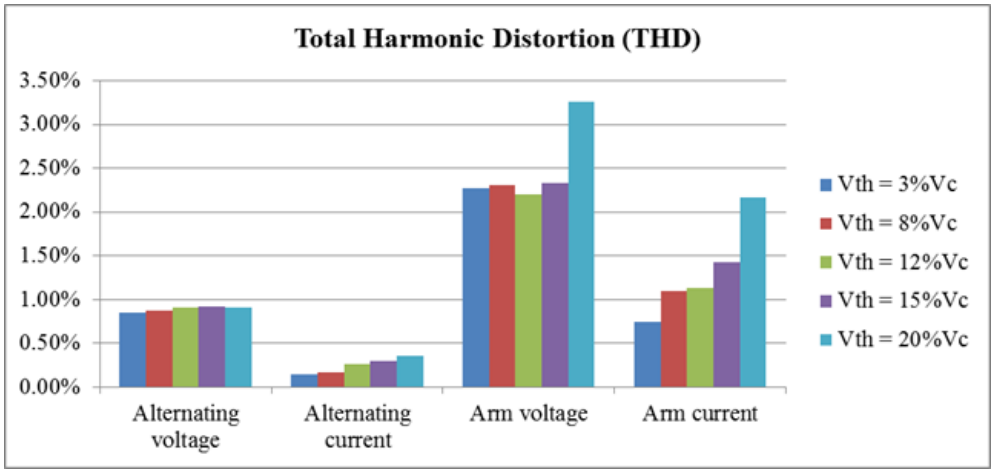


Figure 4-4. Harmonic comparison in simulation with 64 submodules per arm.

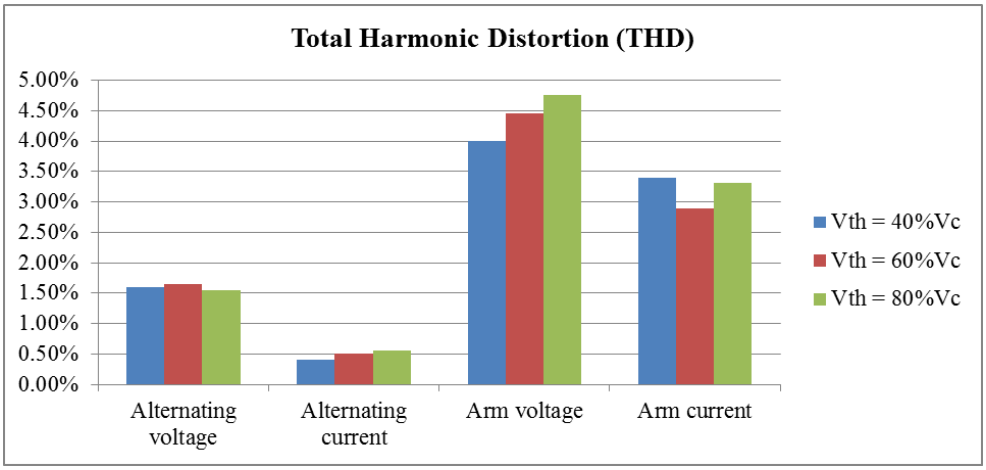


Figure 4-5. Harmonic comparison in simulation with 32 submodules per arm for higher Vth.

system while ABB HVDC light uses 38 submodules. The ac voltage and current harmonics should be well below the limit for Siemens HVDC plus; on the contrary, the harmonics may be designed to be just lower than the limit for ABB HVDC light, in which case the impact of unbalanced voltage cannot be neglected. Therefore, the importance of the threshold voltage's impact on ac voltage and current harmonics highly depends on the submodule number.

In terms of arm voltage and current, no harmonic requirements exist as they are considered as internal variables. However, it should be noticed that arm current harmonic will impact the converter power loss. Higher unbalanced voltage, as a result, may cause slight increase of the converter power loss. Similarly, the importance of this impact is related to the submodule number.

- Impact on converter operation

For threshold voltage selection, it is important to understand that whether it will impact the converter normal operation, especially when the threshold voltage is relatively high. Three different cases are simulated in the scaled system with 32 submodules per arm, in which the threshold voltage is 40%, 60% and 80% of the nominal submodule capacitor voltage, respectively. Figure 4-5 shows the THDs of the alternating voltage/current and arm voltage/current for all three different cases. Compared to the results in Figure 4-3, in which the same simulation system is utilized but with much smaller threshold voltage, the THDs are only slightly higher, and no abnormal phenomenon is observed. So the threshold voltage does not impact the converter normal operation much.

Realizing that the threshold voltage only slightly impacts the voltage and current harmonics, and only matters when the submodule number is small, its selection is mainly a design tradeoff

between the converter switching frequency (or power loss) and submodule capacitor voltage ripple (or submodule voltage rating). Therefore, the derived relationship between the threshold voltage and converter switching frequency is a necessary tool for the threshold voltage selection. With (4-15)-(4-18), the ratio between the threshold voltage and average ripple V_{th}/V_{ripple_avg} is obtained as a function of the converter switching frequency and other operating condition parameters, that is

$$V_{th}/V_{ripple\_avg} = \mathrm{F}(f_{sw}). \tag{4-21}$$

As the total submodule capacitor voltage ripple is the sum of threshold voltage and average ripple, (4-21) can be rewritten as

$$V_{th} = \frac{\mathrm{F}(f_{sw})}{1 + \mathrm{F}(f_{sw})} V_{ripple\_total}. \tag{4-22}$$

Normally the converter switching frequency and submodule capacitor voltage ripple requirements are generated from the overall system design. Provided these design results, the threshold voltage can then be easily selected using (4-22).

4.4 Simulation Verification

Simulation results are presented in this subsection to verify the above analysis. The parameters of the simulated system are listed in Table 4. The full system parameters are based on the INEFLE project [20]. The submodule capacitance is designed for 12.5 % average ripple (half peak-to-peak value) and the arm inductance is selected as 0.15 p.u. considering fault current limiting. For simulation, a downscaled platform with 32 submodules per arm is used.

Table 4. System parameters

Description	Full System	Downscaled System	Downscaled Hardware
Direct voltage	640 kV	51.2 kV	300 V
Rated power	1000 MVA	80 MVA	1 kVA
Alternating voltage	333 kV	26.64 kV	_____
Submodule number per arm	400	32	6
Rated submodule voltage	1.6 kV	1.6 kV	50 V
Submodule capacitance	10 mF	10 mF	2.7 mF
Arm inductance	50 mH	4 mH	0.26 mH

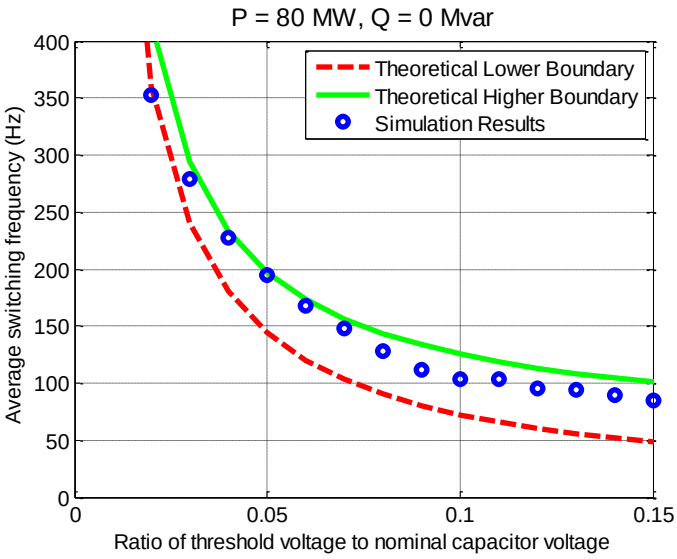


Figure 4-6. Simulated relationship between the switching frequency and unbalanced capacitor voltage.

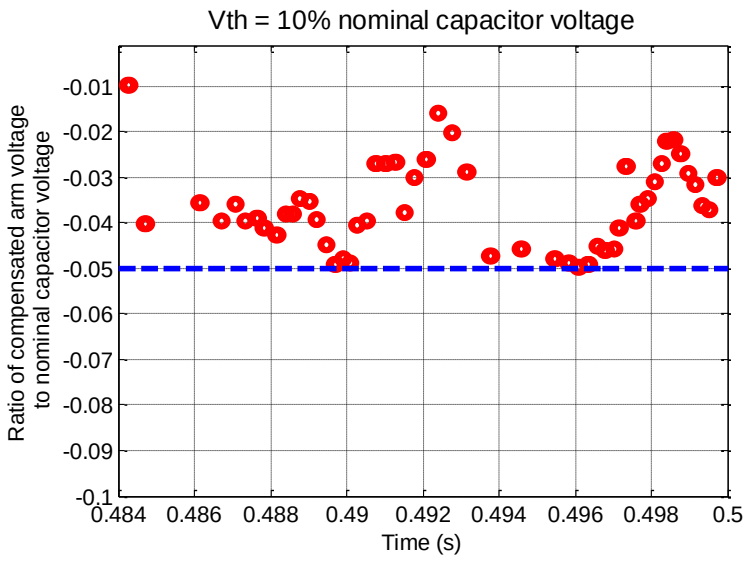


Figure 4-7. Waveform of compensated arm voltage.

Figure 4-6 compares the simulation and calculation results for the relationship between the switching frequency and the unbalanced capacitor voltage threshold at rated power. The simulation results fall within the boundaries given in (4-15) and (4-16). Figure 4-7 shows the compensated arm voltages for case 2 as described previously. V_{th} is set to 10% of the nominal capacitor voltage.

According to the previous analysis, the maximum compensated arm voltage should be $V_{th}/2$, shown in Figure 4-7 as a blue dashed line. It can be seen that the compensated arm voltages are smaller in magnitude than the theoretical maximum value, which matches the analysis. Figure 4-8 shows the comparison under different operating conditions. The simulation results still mostly fall within the boundaries, except for when threshold voltage is small. When the threshold voltage is small, the switching frequency in the simulation is lower than expected. This is because the unbalanced voltage cannot be well maintained within the threshold value.

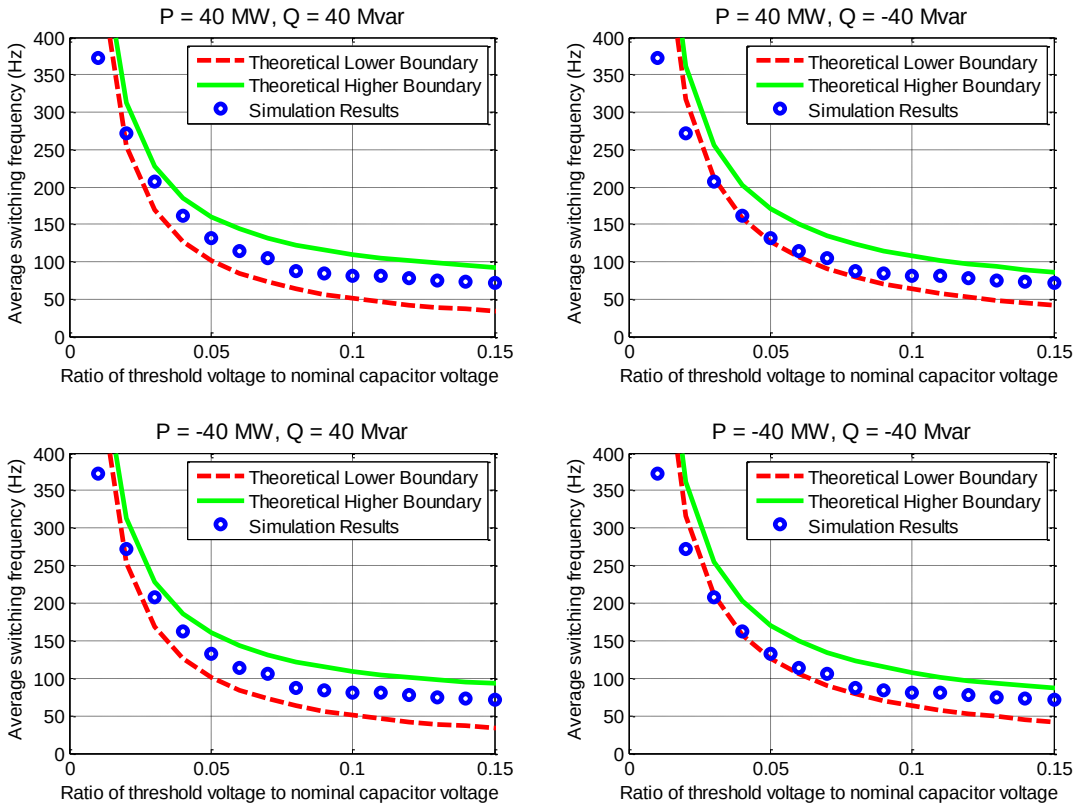


Figure 4-8. Simulated relationship between the threshold voltage and switching frequency at different operating conditions: (a) P = 40 MW, Q = 40 Mvar; (b) P = 40 MW, Q = -40 Mvar; (c) P = -40 MW, Q = 40 Mvar; (d) P = -40 MW, Q = -40 Mvar.

4.5 Experimental Verification

The three-phase, 2 submodules per arm MMC prototype introduced in subsection 3.4 is reconfigured as a single-phase MMC with 6 submodules per arm. The detailed parameters are listed in Table 4.

Figure 4-9 and Figure 4-10 show the experimental results when threshold voltages are 1 V and 9 V (2% and 18% of the nominal capacitor voltage), respectively. According to the analysis, a higher threshold voltage should cause higher voltage and current distortion. This is verified by the arm current waveforms. It is shown that arm currents are more distorted for the case with a 9 V threshold, because the circulating current control is not well executed due to the large arm voltage error.

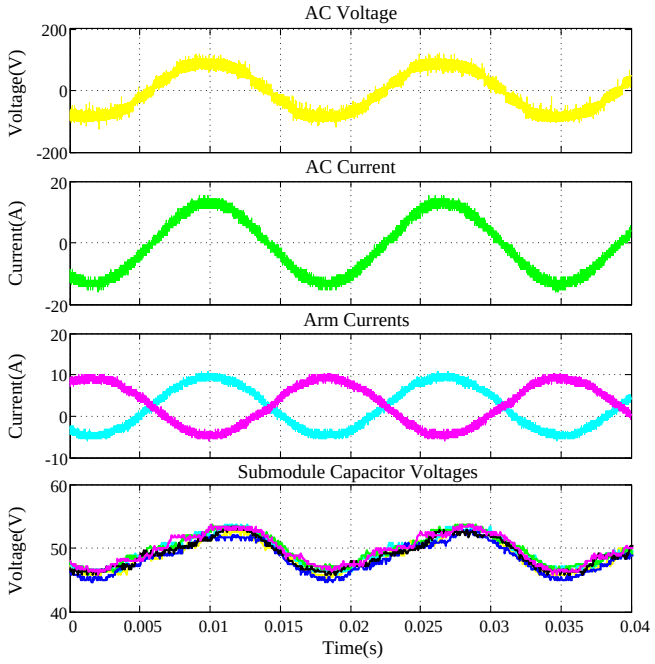


Figure 4-9. Experimental waveforms with threshold voltage of 1 V.

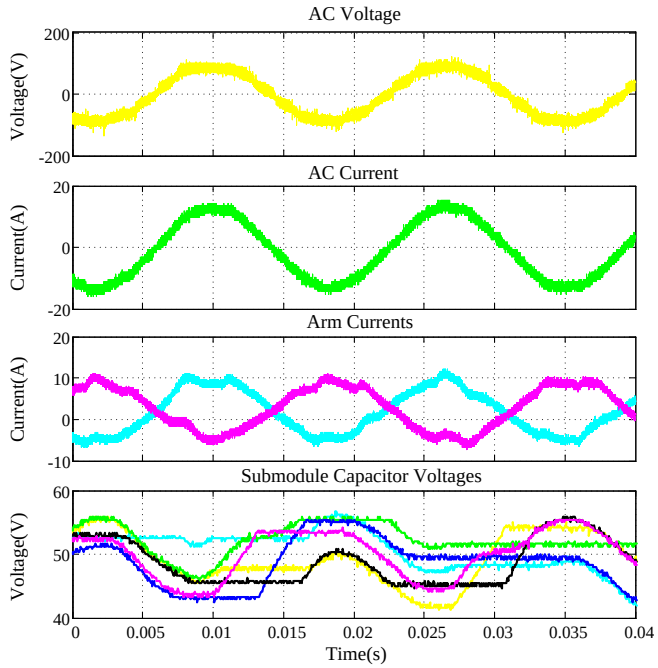


Figure 4-10. Experimental waveforms with threshold voltage of 9 V.

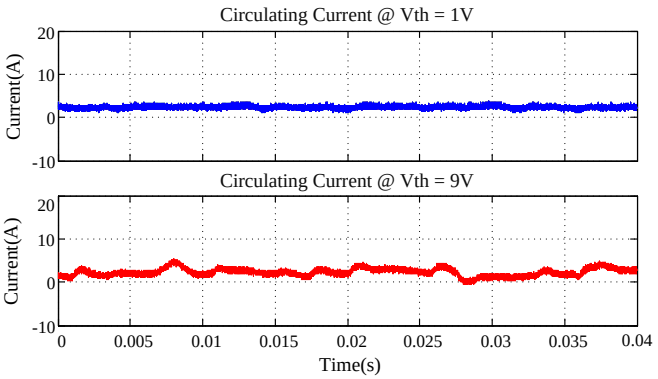


Figure 4-11. Circulating current waveform comparison.

Figure 4-11 shows the circulating current waveforms for both cases. The circulating current for the 9 V threshold case is not well controlled compared to the 1 V threshold case. However, the impact on the alternating current is not obvious in the waveforms. This is mainly because of the relatively large ac inductance, much larger than the arm inductance in this hardware setup.

Figure 4-12 and Figure 4-13 illustrate the proper implementation of the modified sorting method with an unbalanced voltage threshold. Figure 4-12 shows the maximum capacitor voltage difference for two cycles when the threshold voltage is 4 V. Its maximum value, i.e. the maximum unbalanced capacitor voltage, is around 4.5 V. So the maximum unbalanced capacitor voltage is not strictly equal to the threshold voltage. This is also true for cases with different threshold voltages. Figure 4-13 shows the relationship between the threshold voltage and maximum unbalanced capacitor voltage.

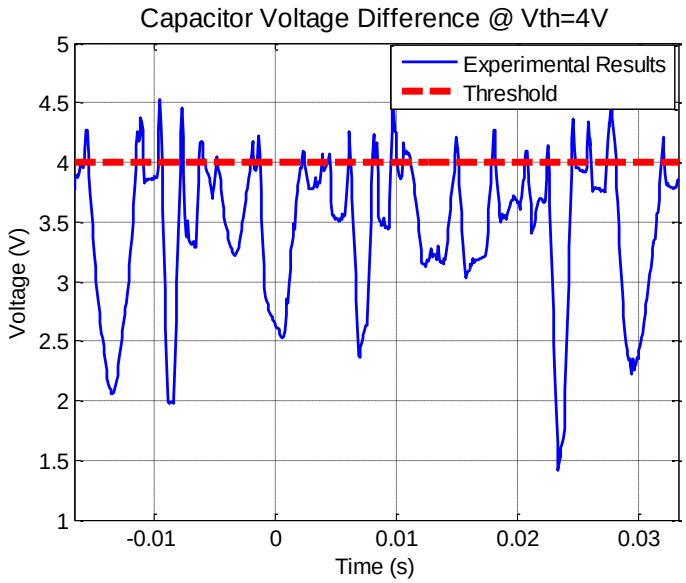


Figure 4-12. Experimental waveforms with threshold voltage of 9 V.

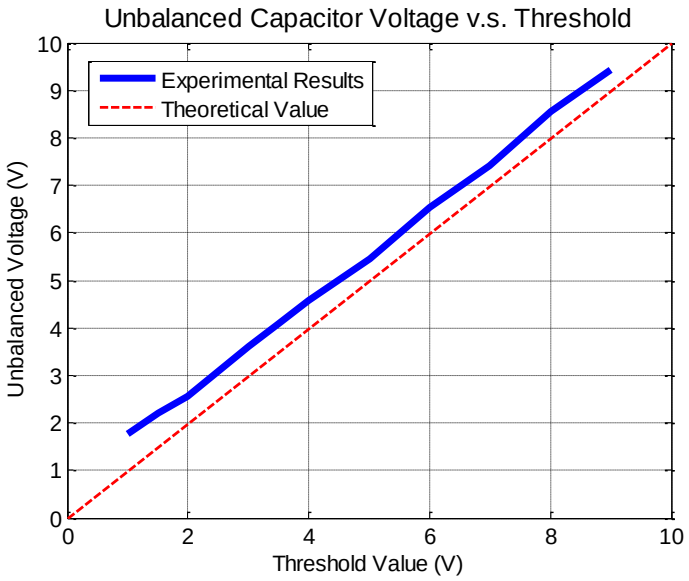


Figure 4-13. Experimental waveforms with threshold voltage of 9 V.

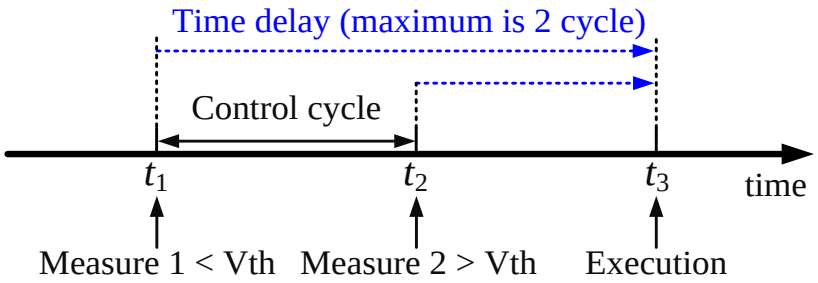


Figure 4-14. Time delay explanation.

The unbalanced capacitor voltage in these results is always larger than the threshold value by a nearly constant value ($\approx 0.5\,\mathrm{V}$). This is mainly because of the time delay, which is explained in Figure 4-14. At time t_1, the unbalanced voltage is approaching but still smaller than the threshold voltage. After a control cycle at time t_2, the unbalanced voltage becomes larger than the threshold voltage. This will trigger the voltage-balancing control to send out the command to exchange the switching states of submodules. Considering the one cycle delay of the digital control, the maximum time delay for executing the voltage-balancing control can be two control cycles. During this delay time, the unbalanced voltage will keep increasing and grow larger than the threshold voltage. The worst case may occur when the arm current is at its maximum value, and the difference between the maximum unbalanced capacitor voltage and threshold voltage can be obtained as

$$\Delta V_{max} = \frac{1}{C_{sub}} i_{arm\_max} T_{delay\_max} = 0.56\,\mathrm{V}. \tag{31}$$

For other cases, the difference should be smaller than this maximum value.

Figure 4-15 shows the experimental results of the relationship between switching frequency and threshold voltage under two different load conditions: 1) R = 7 Ω, L = 0.5 mH; and 2) R = 10 Ω, L = 0.5 mH. For both cases, the rated alternating current is 10 A. It should be noted that because of the small submodule number, PWM is used and its frequency is 12 kHz, much higher than the expected switching frequency. So the PWM is implemented in a way that does not participate in the voltage-balancing control. The theoretical curves are obtained using (4-16), and only the switching actions caused by the voltage-balancing control are considered in these results for switching frequency. The experimental results match the theoretical calculation well.

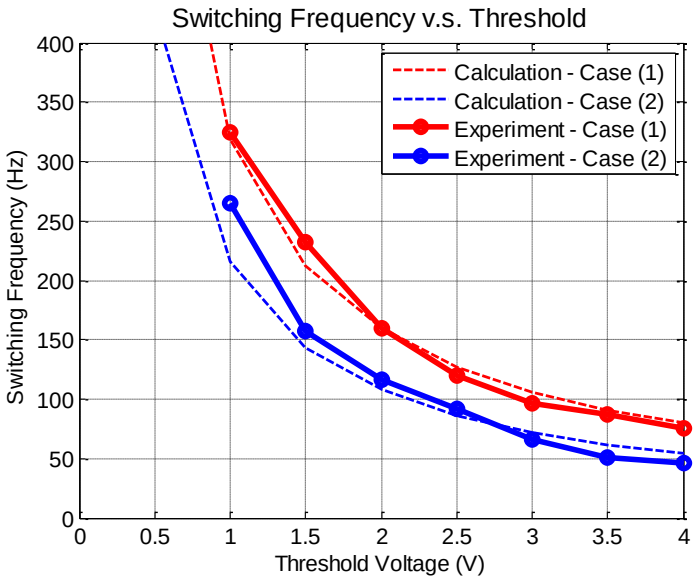


Figure 4-15. Experimental result of the relationship between the switching frequency and unbalanced capacitor voltage.

4.6 Design Tradeoff Between Submodule Capacitance and Switching Frequency

The relationship among the submodule capacitance, switching frequency and capacitor voltage ripple has been derived. If the switching frequency is defined and with the capacitor voltage ripple requirement, the submodule capacitance can be selected. We can notice that the submodule capacitance need is negative correlation with the switching frequency, and switching frequency is directly related to the converter loss. For today's HVDC application, the switching frequency is usually selected at 100 – 150 Hz and the switching loss is smaller than the conduction loss, around 1/3 of the conduction loss based on our simulation. In the literature, there are some works to further push the switching frequency lower. But the derived relationship tells us that lower switching frequency can definitely reduce the loss, but since the switching loss is already a small portion of the total converter loss, which may only gain a little bit benefit. But

lower switching frequency, on the other hand, will require larger submodule capacitance. Since submodule capacitor is also a main contribution to the overall cost, we need to have a tradeoff between the switching frequency and submodule capacitance.

4.7 Conclusion

This chapter evaluates the impact of voltage-balancing control on the submodule capacitance design of MMC. It found that the switching frequency, which determines the effectiveness of the voltage-balancing control, is related to the submodule capacitor unbalanced voltage, and their relationship is derived for the modified sorting method. A key of the derivation is considering voltage-balancing control as a compensation for the arm voltage error. The derived analytical relationship gives the expression of submodule capacitor voltage ripple, as a function of submodule capacitance and switching frequency. So the submodule capacitance can be selected, if providing the voltage ripple and switching frequency requirements. The relationship can also be used for unbalanced capacitor voltage threshold selection, given the design specifications of the switching frequency and submodule voltage rating.

5 MMC Maximum Modulation Index Reduction Due to Circulating Current Suppression Control

As mentioned in subsection 2.1.1, circulating current suppression control can help to reduce the converter power loss. Harnefors *et al.* [50] suggested it can also improve the converter control stability, which made the circulating current suppression control favored for use. The mechanisms of circulating current and corresponding suppression control have been explained in subsection 3.2. The cause of circulating current is arm voltage cannot achieve the desired value due to the submodule capacitor voltage variation. And the circulating current suppression control introduces a common mode component to the arm voltage reference, to compensate the submodule capacitor voltage variation.

The arm voltage references are given in (3-6) and (3-7). It consists of dc voltage bias and fundamental frequency ac voltage. The reference voltage should not go beyond the submodules can supply, i.e. the insertion indices in (3-8) and (3-9) should be limited within [0, 1]. Therefore, the maximum modulation index, if 3rd harmonic injection is not considered, is unity which is the same as typical 2-level VSC. Circulating current suppression control adds additional common mode component into the arm voltage reference, which will decrease the maximum modulation index of MMC. This may lead to the reduction of dc voltage utilization, as well as the converter operating range. This chapter is to determine the maximum modulation index of MMC considering the circulating current control. A MMC model with fundamental frequency component and 2nd order harmonic decoupled is first presented using the concept from [50]-[51]. The common mode component introduced by the circulating current suppression control is then theoretically derived based on the maximum obtainable modulation index that is provided. Since

third harmonic injection is usually adopted for three phase converters, the maximum modulation index for this case is also investigated. Finally, the simulation and experimental results are provided.

5.1 MMC Model

In this chapter, the submodule capacitor voltages are assumed ideally balanced. The arm voltages given in (3-11) and (3-12) can be rewritten as

$$v_{up} = N \cdot n_{up} \cdot v_{up\_c} \tag{5-1}$$

$$v_{low} = N \cdot n_{low} \cdot v_{low\_c} \tag{5-2}$$

where v_{up} and v_{low} are arm voltages, n_{up} and n_{low} are insertion indices, and v_{up_c} and v_{low_c} are submodule capacitor voltages, with subscript "*up*" means upper arm quantities and "*low*" means lower arm quantities. The derivatives of the submodule capacitor voltages can be given as

$$\frac{dv_{up\_c}}{dt} = \frac{1}{C_{sub}} \cdot n_{up} \cdot i_{up} \tag{5-3}$$

$$\frac{dv_{low\_c}}{dt} = \frac{1}{C_{sub}} \cdot n_{low} \cdot i_{low} \tag{5-4}$$

where i_{up} and i_{low} are arm voltages, and C_{sub} is the submodule capacitance.

For the purpose of better explanation, (3-1) and (3-2) are rewritten as

$$v_g = \frac{v_{low} - v_{up}}{2} - \frac{L_{arm}}{2}\frac{di_{ac}}{dt} \tag{5-5}$$

$$v_{dc} = v_{up} + v_{low} + 2L_{arm}\frac{di_{cm}}{dt}. \tag{5-6}$$

The common mode and differential mode submodule capacitor voltages can be defined as

$$v_{cm\_c} = \frac{v_{low\_c} + v_{up\_c}}{2} \tag{5-7}$$

$$v_{dm\_c} = \frac{v_{low\_c} - v_{up\_c}}{2}. \tag{5-8}$$

Similarly, the common mode and differential mode insertion indices are defined as

$$n_{cm} = \frac{n_{low} + n_{up}}{2} \tag{5-9}$$

$$n_{dm} = \frac{n_{low} - n_{up}}{2}. \tag{5-10}$$

Combining (5-7)-(5-10) into (5-1) and (5-2) gives

$$v_{low} + v_{up} = 2N \cdot \left(n_{cm} \cdot v_{cm\_c} + n_{dm} \cdot v_{dm\_c}\right) \tag{5-11}$$

$$v_{low} - v_{up} = 2N \cdot \left(n_{dm} \cdot v_{cm\_c} + n_{cm} \cdot v_{dm\_c}\right). \tag{5-12}$$

Inserting (5-11) and (5-12) into (5-5) and (5-6) gives

$$\frac{L_{arm}}{2}\frac{di_{ac}}{dt} = -v_g + N \cdot n_{dm} \cdot v_{cm\_c} + N \cdot n_{cm} \cdot v_{dm\_c} \tag{5-13}$$

$$L_{arm}\frac{di_{cm}}{dt} = \frac{v_{dc}}{2} - N \cdot n_{cm} \cdot v_{cm\_c} - N \cdot n_{dm} \cdot v_{dm\_c}. \tag{5-14}$$

Adding (5-4) to (5-3) and subtracting (5-4) to (5-3) give

$$C_{sub}\frac{d\left(v_{low\_c}+v_{up\_c}\right)}{dt}=n_{low}i_{low}+n_{up}i_{up} \tag{5-15}$$

$$C_{sub}\frac{d\left(v_{low\_c}-v_{up\_c}\right)}{dt}=n_{low}i_{low}-n_{up}i_{up}. \tag{5-16}$$

Similarly, with the substitutions in (5-9) and (5-10), (5-15) and (5-16) can be rewritten as

$$C_{sub}\frac{dv_{cm\_c}}{dt}=n_{cm}i_{cm}-n_{dm}\frac{i_{ac}}{2} \tag{5-17}$$

$$C_{sub}\frac{dv_{dm\_c}}{dt}=n_{dm}i_{cm}-n_{cm}\frac{i_{ac}}{2}. \tag{5-18}$$

Equations (5-13)-(5-14) and (5-17)-(5-18) give the model of MMC with state variables of i_{ac}, i_{cm}, v_{cm_c} and v_{dm_c}. The good thing with this model is that all the four state variables are usually with single frequency, unlike the arm voltage and submodule capacitor voltage.

5.2 Steady State Calculation

The above derived model shows that there are two controllable variables, which are usually used to control the ac current and circulating current. Assuming i_{cm} only includes dc component and the i_{ac} is defined as

$$i_{ac}=I_{ac}\cos(\omega t-\varphi) \tag{5-19}$$

where φ represents the power angle between ac phase current and phase voltage, which is defined as

$$v_{ac}=v_g+\frac{L_{arm}}{2}\frac{di_{ac}}{dt}=V_{ac}\cos(\omega t) \tag{5-20}$$

If the converter loss is neglected, i_{cm} can be expressed as

$$i_{cm} = \frac{M}{4} I_{ac} \cos(\varphi) \tag{5-21}$$

At first, the submodule capacitor voltage ripple is neglected. So v_{cm_c} and v_{dm_c} can be approximated by

$$v_{cm\_c} \approx \frac{v_{dc}}{N} \tag{5-22}$$

$$v_{dm\_c} \approx 0. \tag{5-23}$$

Inserting (5-19)-(5-23) to (5-13) and (5-14) gives

$$V_{ac}\, cos(\omega t) = v_{dc} \cdot n_{dm} \tag{5-24}$$

$$\frac{v_{dc}}{2} = v_{dc} \cdot n_{cm}. \tag{5-25}$$

n_{cm} and n_{dm} can be solved as

$$n_{cm} = \frac{1}{2} \tag{5-26}$$

$$n_{dm} = \frac{M}{2} cos(\omega t). \tag{5-27}$$

where M is the modulation index, defined as $2\, V_{ac}/v_{dc}$.

Inserting (5-19), (5-21), (5-26) and (5-27) into (5-17) and (5-18), and then integrating it gives

$$v_{cm\_c} = \frac{v_{dc}}{N} - \frac{1}{C_{sub}} \frac{M}{16\omega} I_{ac} \sin(2\omega t - \varphi) \tag{5-28}$$

$$v_{dm\_c} = -\frac{1}{C_{sub}} \frac{1}{4\omega} I_{ac} \left[-\sin(\varphi)\cos(\omega t) + \left(1 - \frac{M^2}{2}\right)\cos(\varphi)\sin(\omega t) \right]. \tag{5-29}$$

Compared with the approximations in (5-22) and (5-23), the initial approximations are only valid when the submodule capacitor is large enough. As discussed in Chapter 4, the capacitance is preferred to be small for reduced converter cost. A reasonable design example would be to limit the average capacitor ripple (half peak to peak value) within 10%.

To facilitate the following derivation, the variation of v_{cm_c} is defined as

$$\Delta v_{cm\_c} = -\frac{1}{C_{sub}} \frac{M}{16\omega} I_{ac} \sin(2\omega t - \varphi). \tag{5-30}$$

Since the approximations in (5-22) and (5-23) are not valid, the insertion indices obtained in (5-26) and (5-27) are not accurate. Inserting (5-20) and (5-21) into (5-13) and (5-14), the n_{cm} and n_{dm} can be solved as

$$n_{cm} = \frac{1}{N} \frac{1}{v_{cm\_c}^2 - v_{dm\_c}^2} \left(\frac{v_{dc}}{2} v_{cm\_c} - v_{ac} v_{dm\_c} \right) \tag{5-31}$$

$$n_{dm} = \frac{1}{N} \frac{1}{v_{cm\_c}^2 - v_{dm\_c}^2} \left(v_{ac} v_{cm\_c} - \frac{v_{dc}}{2} v_{dm\_c} \right). \tag{5-32}$$

Neglecting the second-order derivative, the following equations are derived as

$$n_{cm} = \frac{1}{2} + \frac{v_{ac}}{v_{dc}} \frac{N v_{dm\_c}}{v_{dc}} + \frac{N \Delta v_{cm\_c}}{2 v_{dc}} \tag{5-33}$$

The variation on n_{dm} is not considered as the circulating current only adds a common mode component. Inserting (5-28) and (5-29) to (5-33) gives

$$n_{cm} = \frac{1}{2} + \frac{1}{2v_{dc}} \frac{N}{C_{sub}} \frac{M}{8\omega} I_{ac} \left\{ -\frac{3}{2} \sin(\varphi) \cos(2\omega t) + \left(\frac{3}{2} - \frac{M^2}{2} \right) \cos(\varphi) \sin(2\omega t) \right\}. \tag{5-34}$$

5.3 Maximum Modulation Index Derivation

Equations (5-34) shows that the needed common mode compensating component is a second-order harmonic, and is related to the system parameters (C_{sub} and N) and operating conditions (M, I_{ac} and φ). It is not convenient to evaluate its impact on the modulation signal.

The capacitor voltage ripple can be derived by inserting (5-28) and (5-29) into (5-7) or (5-8) [27], that is

$$V_{Ripple} = \frac{1}{C_{sub}} \frac{1}{4\omega} I_{ac} \left(1 - \left(\frac{M}{2} \cos(\varphi) \right)^2 \right)^{\frac{3}{2}}. \tag{5-35}$$

The maximum capacitor voltage ripple depends on the converter operating range. According to [14], the maximum reactive power is usually defined as half of the maximum active power, which means the minimum power factor for MMC operating at full apparent power is $\sqrt{3}/2$. Therefore, the maximum capacitor voltage ripple is obtained as

$$V_{Ripple} = 0.73 \frac{1}{C_{sub}} \frac{1}{4\omega} I_{ac} \tag{5-36}$$

where maximum *M*=1 is considered. The coefficient 0.73 is related to the maximum reactive

power limitation. The ratio of the ripple voltage to the average capacitor voltage is given as

$$\varepsilon = 0.73 \cdot \frac{N}{v_{dc}} \frac{1}{C_{sub}} \frac{1}{4\omega} I_{ac}. \tag{5-37}$$

ε usually can be considered as a constant value from design point of view. Equations (5-34) can then be simplified as

$$n_{cm} = \frac{1}{2} + \varepsilon \frac{M}{2.92} \left\{ -\frac{3}{2} \sin(\varphi) \cos(2\omega t) + \left(\frac{3}{2} - \frac{M^2}{2} \right) \cos(\varphi) \sin(2\omega t) \right\}. \tag{5-38}$$

5.3.1 Without 3rd Harmonic Injection

The insertion index for the lower arm (upper arm is similar) can be obtained as

$$\begin{aligned} n_{low} = \frac{1}{2} + \frac{M}{2} \cos(\omega t) \\ + \varepsilon \frac{M}{2.92} \left\{ -\frac{3}{2} \sin(\varphi) \cos(2\omega t) \right. \\ \left. + \left(\frac{3}{2} - \frac{M^2}{2} \right) \cos(\varphi) \sin(2\omega t) \right\} \end{aligned} \tag{5-39}$$

which should satisfy

$$0 \le n_{low} \le 1. \tag{5-40}$$

Based on (5-39), the maximum and minimum of the lower arm insertion index are obtained when $\cos(\varphi)$ equals to its minimum value, that is

$$n_{low}(max) = 0.5 + (0.5 + 0.26\varepsilon)M \tag{5-41}$$

$$n_{low}(max) = 0.5 - (0.5 + 0.26\varepsilon)M \tag{5-42}$$

The limitation on the modulation index can be obtained as

$$M \leq \frac{1}{1 + 0.52\varepsilon}. \tag{5-43}$$

It shows that the maximum modulation index is smaller than 1, and larger capacitor voltage ripple leads to more reduction.

5.3.2 With 3rd Harmonic Injection

A third-order harmonic is usually added to the modulation signal to increase the dc voltage utilization. In the two-level converter case, the maximum modulation index can be increased from 1 to 1.155. But the implementation of circulating current control in MMC would also impact the maximum modulation index. With the third-order harmonic injection, the differential mode component of the insertion indices is changed to

$$n_{dm} = \frac{M}{2}\left[\cos(\omega t) - \frac{1}{6}\cos(3\omega t)\right]. \tag{5-44}$$

Similarly, (5-37) should be updated to

$$\varepsilon = 0.68 \cdot \frac{N}{v_{dc}} \frac{1}{C_{sub}} \frac{1}{4\omega} I_{ac}. \tag{5-45}$$

The common mode compensating component can then be calculated as

$$\Delta n_{cm} = \varepsilon \frac{M}{2.72}\left\{\left(\frac{19}{12} - \frac{7M^2}{12}\right)\cos(\varphi)\sin(2\omega t) - \frac{17}{12}\sin(\varphi)\cos(2\omega t)\right\}. \tag{5-46}$$

By calculating the maximum and minimum values of n_{low}, the limitation on the modulation index is obtained as

$$M \leq \frac{1}{0.87 + 0.70\varepsilon}. \tag{5-47}$$

The limitations on modulation indices for the cases without and with third harmonic component injection are given in (5-43) and (5-47). Considering a practical capacitor voltage ripple requirement of 10%, the maximum modulation indices for both cases are

$$M(max) = 0.95 \tag{5-48}$$

$$M(max)_{3rd} = 1.06. \tag{5-49}$$

Therefore, if the submodule capacitance is designed for 10% voltage ripple, the maximum modulation index is reduced by 5% (from 1 to 0.95) by implementing the circulating current control. And if considering the third harmonic component injection, the reduced percentage is even around 8% (from 1.155 to 1.06). These decreases are not negligible, and should be considered for the nominal modulation index selection for MMC at the design stage.

5.4 Simulation Verification

A MMC simulation model is built in MATLAB to verify the above theoretical calculations and analysis. It operates at inverter mode, with the rated power at 250 MVA, rated dc and ac voltages at 300 kV and 161 kV, respectively. The submodule capacitance is designed to allow a maximum of 10% average voltage ripple. The submodule number is selected as 4 to reduce the simulation time, while this should not affect the validity of the verification.

The validity of the MMC model derived in (5-13)-(5-14) and (5-17)-(5-18) is first verified.

Figure 5-1 shows the steady state values for i_{ac}, i_{cm}, v_{cm_c} and v_{dm_c} at full load with power factor of $\sqrt{3}/2$. The simulation results match the calculation very well. Other operating conditions are also simulated, and all show a good match between the simulation and calculation. Figure 5-2 and Figure 5-3 show the comparison of $n_{dm}, \Delta n_{cm}$ and n_{low} for the cases without and with third harmonic injection. The accuracy of the derived expression of Δn_{cm} is verified. It also shows that the shape of n_{low} is slightly changed because of the compensating component.

To verify the maximum modulation index calculation, MMC operates at the worst case with $\sqrt{3}/2$ power factor. Figure 5-4 and Figure 5-5 show the lower arm insertion index under different modulation indices. Without third harmonic injection, the modulation signal starts to hit the limit when $M = 0.95$; with third harmonic component injection, the maximum modulation index is 1.05. The results match the calculations in (5-48) and (5-49).

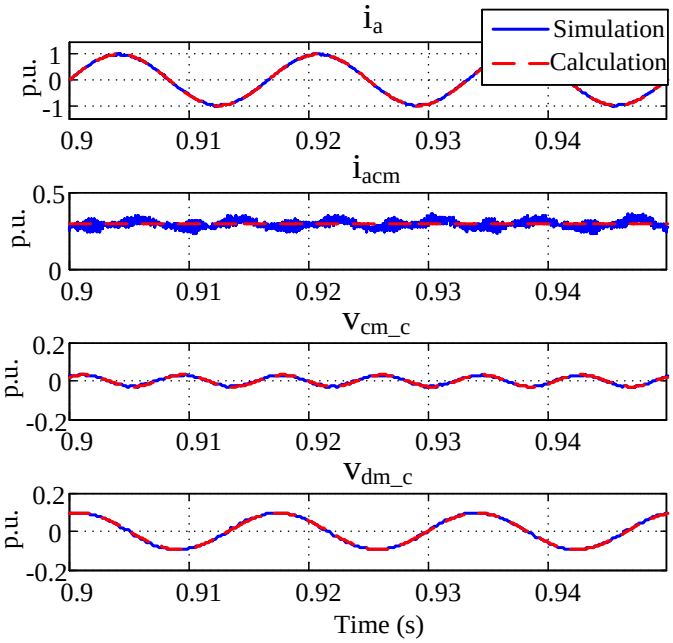


Figure 5-1. Steady state simulation results of the defined MMC system.

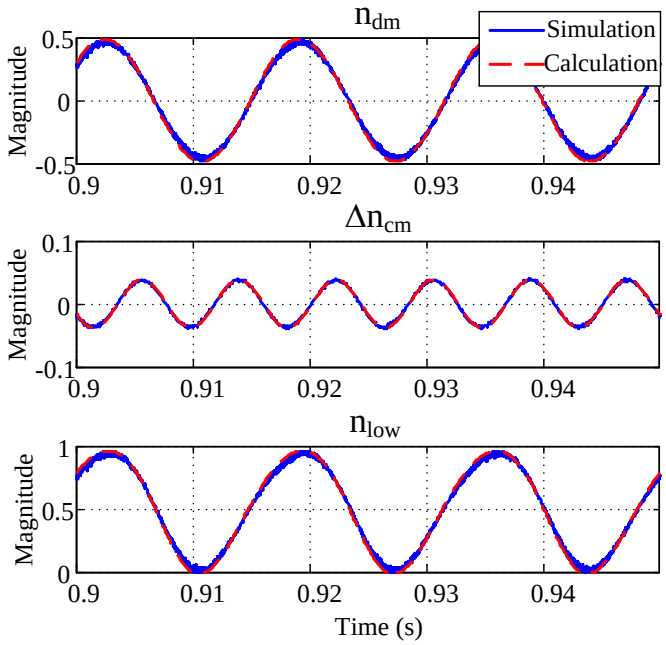


Figure 5-2. Lower arm modulation signal components.

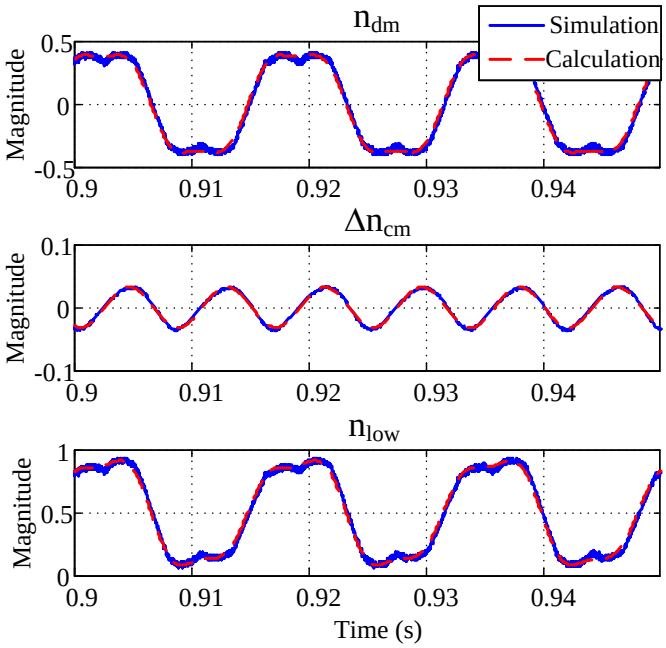


Figure 5-3. Lower arm modulation signal components with 3rd harmonic injection.

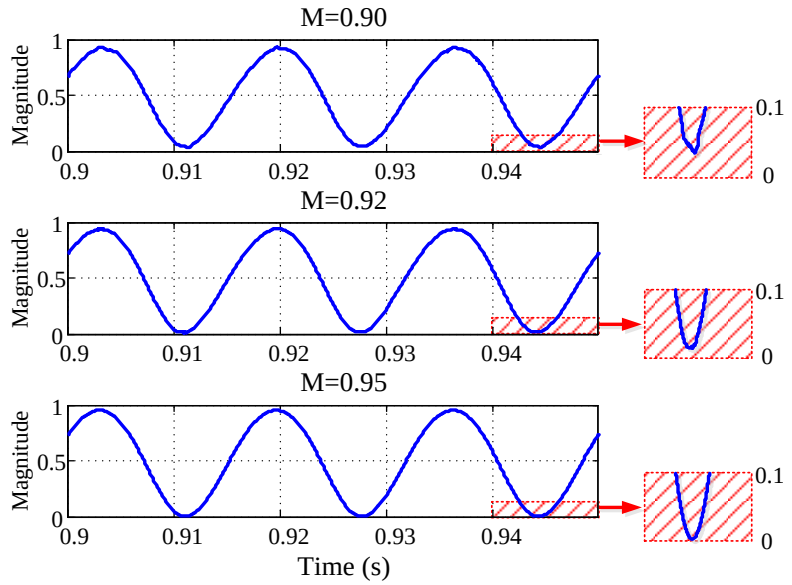


Figure 5-4. Lower arm modulation signal under different modulation indices.

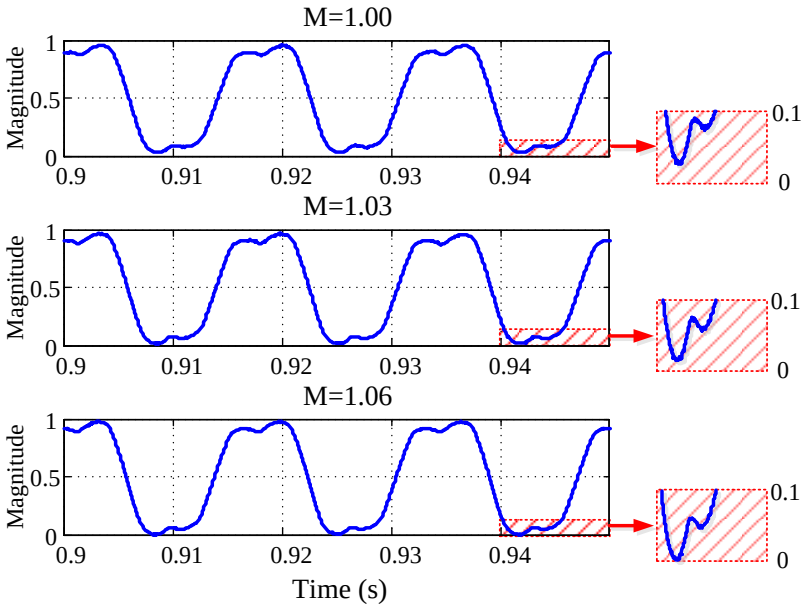


Figure 5-5. Lower arm modulation signal under different modulation indices with 3rd harmonic injection.

5.5 Experimental Verification

The three-phase MMC prototype with 2 submodules per arm introduced in subsection 3.4 is used. The arm inductance is chosen as 0.26 mH. The prototype is connected to a constant dc voltage source operating at inverter mode and with three-phase balanced passive load of inductors and resistors. The resistance of each phase is 3.6 Ω and the inductance is 5.5 mH, as to emulate the worst case at power factor of $\sqrt{3}/2$. The load impedance of each phase is 4.16 Ω.

5.5.1 Without 3rd Harmonic Injection

In the test, the maximum insertion index for each arm is limited to 0.98 due to the dead time implementation. The ratio of capacitor voltage ripple to average capacitor voltage is 5% with selected system parameters. The maximum modulation index in (5-48) can be recalculated as

$$M(max) = \frac{0.96}{1 + 0.52 \times 5\%} = 0.936. \tag{5-50}$$

The maximum ac current not causing overmodulation is obtained as

$$I_{ac\_max} = \frac{50 \cdot M(max)}{\sqrt{2} \cdot Z_{load}} = 7.95\ A. \tag{5-51}$$

Fig. 7(a) and Fig. 7(b) show the experimental results at $I_{ac} = 7.8$ A and $I_{ac} = 8$ A respectively. The circulating current as well as the arm currents has some notches in the case when $I_{ac} = 8$ A. This is the sign of overmodulation. It can be seen more clearly from Fig. 8, which shows the modulation signal components. For the case with $I_{ac} = 8$ A, n_{low} becomes flat at its peak value and Δn_{cm} is distorted, which means the converter is overmodulated. Thus the experimental result matches theoretical analysis very well.

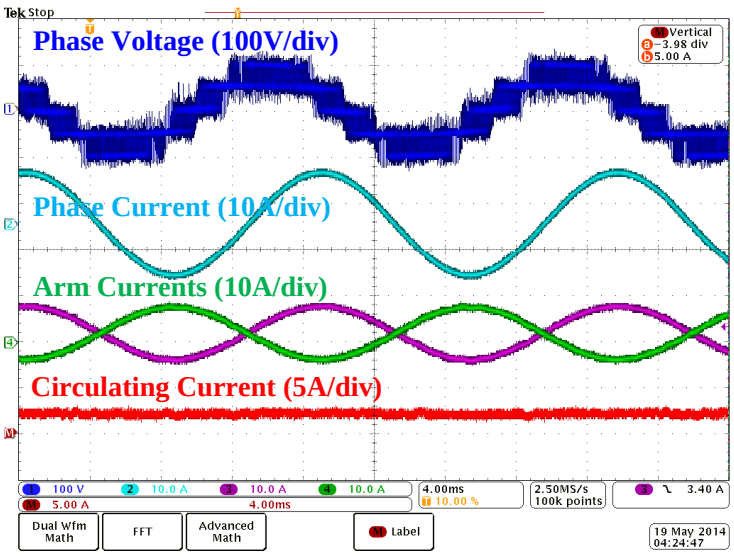


Figure 5-6. Experimental results without 3rd harmonic component injection when $I_{ac} = 7.8$ A

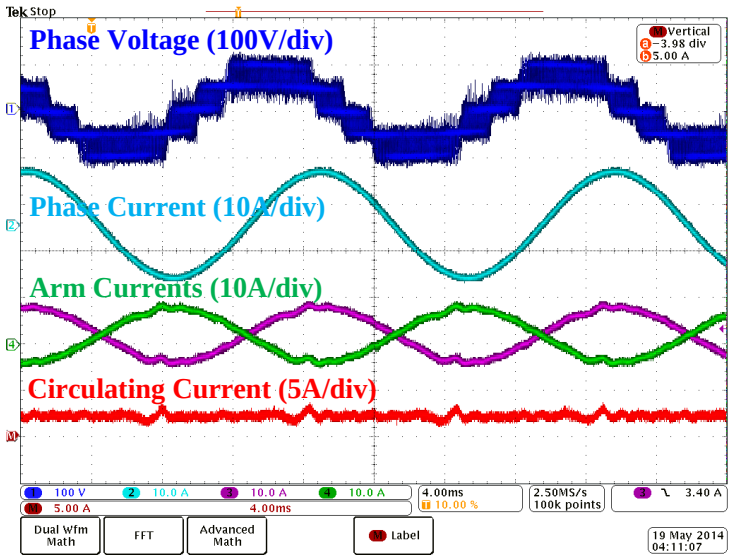


Figure 5-7. Experimental results without 3rd harmonic component injection when $I_{ac} = 8$ A.

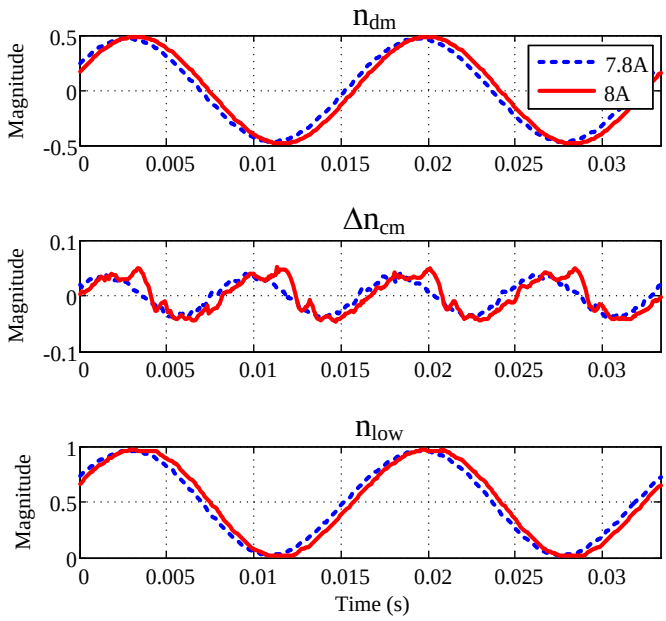


Figure 5-8. Lower arm modulation signal component comparison for cases when $I_{ac} = 7.8$ A and $I_{ac} = 8$ A.

5.5.2 With 3rd Harmonic Injection

Similarly, the maximum modulation index and maximum ac current not causing overmodulation for the case with 3rd harmonic injection can be recalculated, that is

$$M(max) = \frac{0.96}{0.87 + 0.70 \times 5\%} = 1.06. \tag{5-52}$$

$$I_{ac\_max} = \frac{50 \cdot M(max)}{\sqrt{2} \cdot Z_{load}} = 9\ A. \tag{5-53}$$

Fig. 9(a) and Fig. 9(b) show the experimental results for cases $I_{ac} = 7.8$ A and $I_{ac} = 8$ A, respectively. Fig. 10 shows the modulation signal comparison for the two cases. The modulation signal hits the limit for the case with $I_{ac} = 9$, which matches the theoretical calculation.

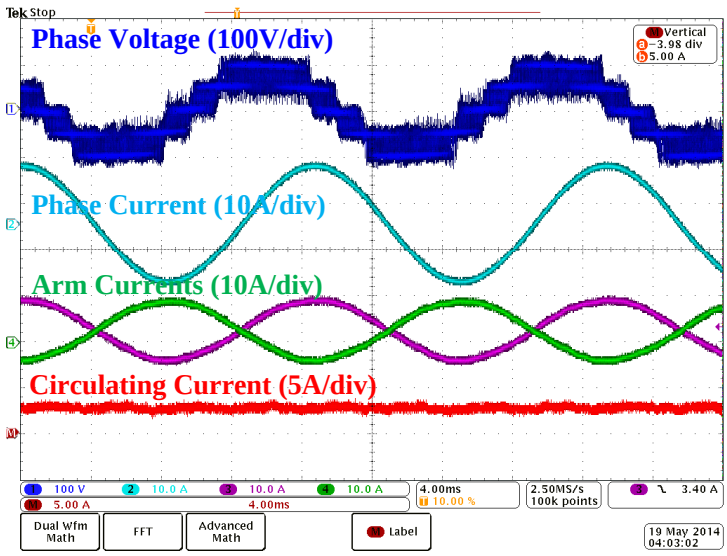


Figure 5-9. Experimental results with 3rd harmonic component injection when $I_{ac} = 8.8$ A

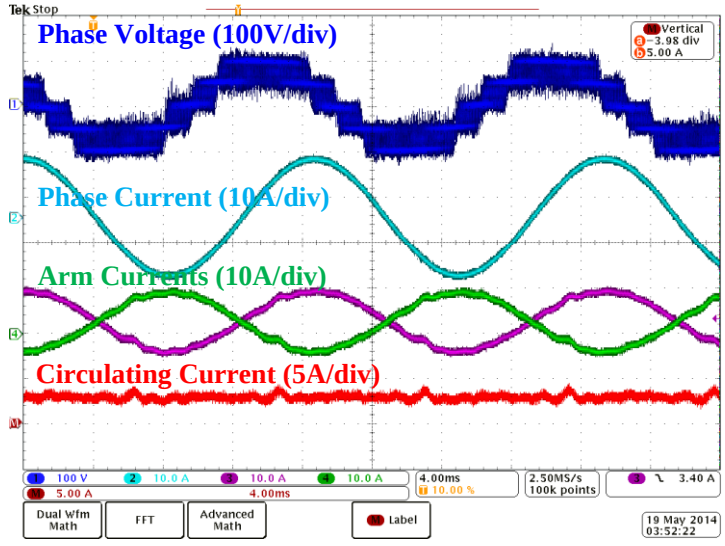


Figure 5-10. Experimental results with 3rd harmonic component injection when $I_{ac} = 9$ A.

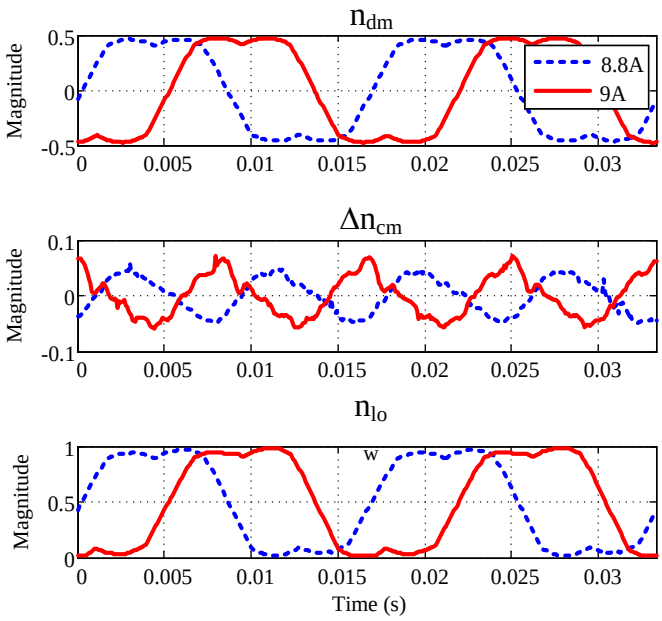


Figure 5-11. Lower arm modulation signal component comparison for cases when $I_{ac} = 8.8$ A and $I_{ac} = 9$ A.

5.6 Conclusion

The circulating current control in MMC adds an extra double fundamental frequency component into the modulation signal. This additional component as a result decreases the converter maximum modulation index which affects the dc voltage utilization. The reduction of the maximum modulation index is related to the submodule capacitance; smaller capacitance leads to larger reduction. If the capacitance is designed based on a 10% voltage ripple requirement, the maximum modulation index could be reduced by 5%, or 8% for the case with third harmonic component injection. This reduction is not negligible and should be considered for the nominal modulation index selection in the converter design. The maximum modulation index reduction phenomenon has been seen in both the simulation and experiment results, and the theoretical analysis is verified.

6 Four-Terminal HVDC Testbed

This chapter presents the development of a scaled four-terminal HVDC testbed, including hardware structure, communication architecture and different control schemes. The developed testbed is capable of emulating some typical operation scenarios including system start-up, power variation, line contingency, and converter station failure. Some unique scenarios are also developed and demonstrated, such as online control mode transition and station re-commission. The testbed will serve for the control and protection development in the next few chapters.

6.1 System Structure and Testbed Parameters

Figure 6-1 shows the circuit diagram of the proposed 4-terminal HVDC system with a dc ring topology. This system structure can be used for big city dc infeed with one large station receiving the power from three different power generations. Another potential application would be integrating two offshore wind farms to two onshore ac grids, which is considered in this thesis. In order to develop the testbed, a hypothetic MTDC system is first proposed, for transferring

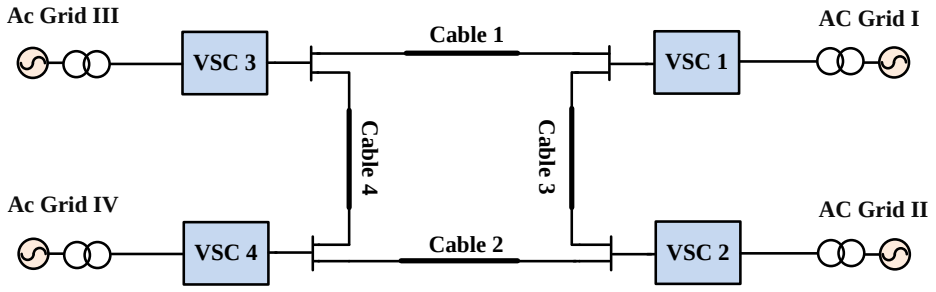


Figure 6-1. Circuit diagram of the proposed 4-terminal HVDC system.

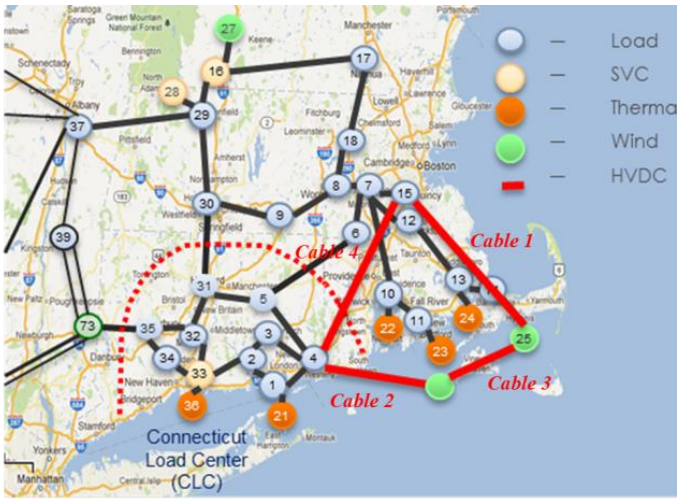


Figure 6-2. Proposed hypothetic system corresponding to Cape Wind Project in NPCC system.

Table 5. Parameters of the hypothetical system

Description	**AC Grid I (Wind Farm I)**	**AC Grid II (Wind Farm II)**	**AC Grid III**	**AC Grid IV**
DC voltage	±150 kV	±150 kV	±150 kV	±150 kV
AC voltage	33 kV	33 kV	345 kV	115 kV
Active power	250 MW	200 MW	250 MW	200 MW
Reactive power	—	—	150 Mvar	100 Mvar
Transformer ratio	33 kV/161 kV	33 kV/161 kV	345 kV/161 kV	115 kV/161 kV
	Cable 1	**Cable 2**	**Cable 3**	**Cable 4**
Type, Length	Land 100 km	Submarine 70 km	Submarine 60 km	Land 100 km

power from two wind farms in Cape Cod Bay area to two onshore load centers in Massachusetts (U.S.) and Connecticut (U.S.), as shown in Figure 6-2. The system contains 4 power converter stations and 4 transmission cables. The detailed parameters of the proposed system are shown in Table 5. The wind farm power ratings are roughly corresponding to the Cape Wind project [52]. From the geographical point of view, cables 1-3 cross both the land and sea. But for simplicity, cable 1 and cable 4 are assumed as land cables only and cable 2 and cable 3 are submarine cables.

The testbed is developed based on the proposed system with a power scaling factor of 1/50000, as shown in Figure 6-3. The scaling principle is by maintaining the per-unit values of all electrical parameters. Table 6 lists the main parameters of the testbed. 2-level VSC is used, and the detailed circuit diagram in each downscaled power station is shown in Figure 6-4. The converter ac terminal is connected to the grid through interfacing reactors, a pre-charge circuit and an Yn/Δ line-frequency transformer.

Figure 6-3. Photograph of the testbed.

Table 6. Parameters of the MTDC testbed

DC voltage	400 V	**Power rating of VSC 1,3**	5 kW
AC voltage (rms)	208 V	**Power rating of VSC 2,4**	4 kW
Transformer	208 Yn/208 Δ	**AC reactor of VSC 1,3**	3.2 mH
DC-link capacitance	1.35 mF	**AC reactor of VSC 2,4**	4 mH
Cable 1 resistance, inductance	0.2 Ω, 2.5 mH	**Cable 2 resistance, inductance**	0.15 Ω, 2.5 mH
Cable 3 resistance, inductance	0.5 Ω, 2.5 mH	**Cable 4 resistance, inductance**	1 Ω, 3.5 mH

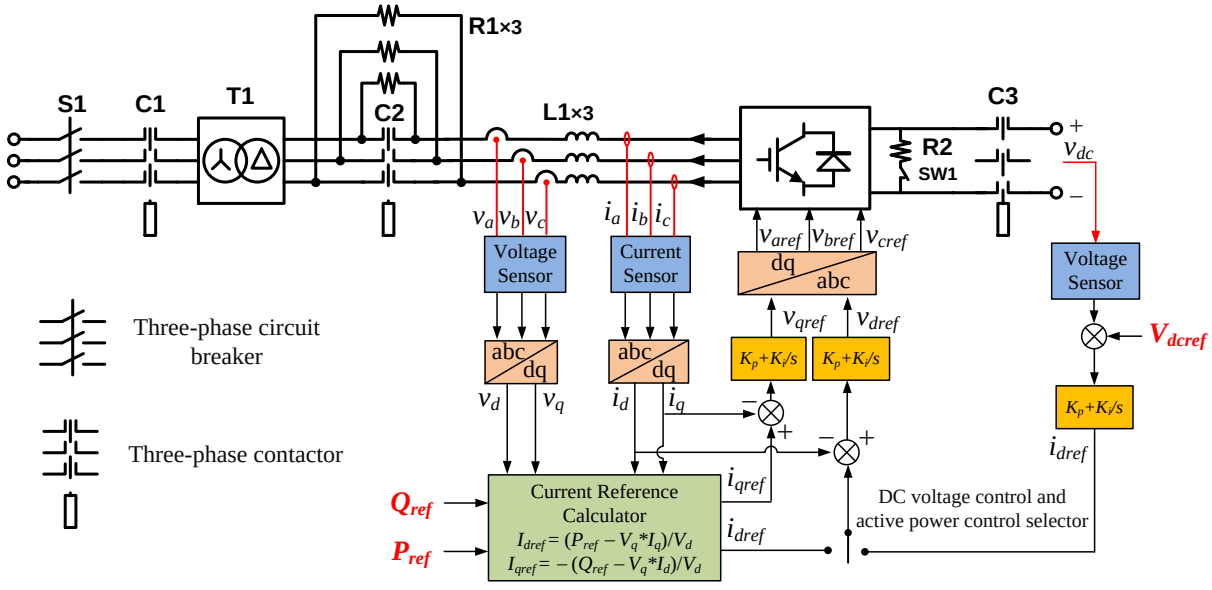


Figure 6-4. Circuit diagram and control schemes of the downscaled power station.

On the dc side, the converter connects to the joint of two cables and a discharge resistor is paralleled for dc capacitor energy dissipation after station shut down. The dc cable is emulated by discrete passive elements, according to the lumped π model [53]. The equivalent inductance, capacitance and resistance of each cable in the hypothetical system are obtained from the ABB land and submarine cable data [2], and then scaled for the testbed system. Only equivalent resistors and inductors are installed in the testbed, as the capacitors can be considered as combined into the dc link capacitor of each station.

6.2 Control and Communication

- *Converter control*

The converter is digitally controlled, using the Texas Instrument DSP TMS320F28335 as the controller. The converter control schemes are shown in Figure 6-4 as well, with inner current loop and outer dc voltage/active power and reactive power control loops. AC voltage and frequency control are not implemented as the converter is connected to a stiff ac grid. So each converter can either operate at dc voltage and reactive power control mode (Vdc/Q), or active power and reactive power control mode (P/Q).

- *Coordinated dc voltage control*

DC voltage control is a main objective and challenge in dc system, similar to controlling the frequency in ac system. An essential requirement is that at any time including during a contingency event, the system should have at least one station participating on the dc voltage control. For instance, if a station responsible for dc voltage control fails, another station in the system has to take over the dc voltage control responsibility automatically, without the communication need. Many coordinated dc voltage control schemes have been introduced in

literature. Voltage margin [54] and voltage droop [55] are two most popular ones and many other schemes are also based on them. These two methods are both implemented in the testbed. Figure 6-5 shows the Vdc-P characteristic curves of the two onshore converters (VSC 3 and 4) for voltage margin control. According to the curves, VSC 3 normally controls dc voltage and VSC 4 operates at P control mode. If for some reason such as a fault, VSC 3 loses the dc voltage control capability, the dc voltage will either increase or decrease until it reaches the voltage margin of VSC 4. After that, VSC 4 changes to dc voltage regulating mode. Therefore, the voltage margin control increases the system robustness in dealing with station outage.

Figure 6-6 shows the Vdc-P characteristic curves for voltage droop control. There is no longer a constant dc voltage or active power reference. Instead, the dc voltage reference is online calculated by a function of the real-time active power, which is the Vdc-P droop control; or otherwise the active power reference is calculated based on dc voltage, that is P-Vdc droop control. With the droop control, both VSC 3 and 4 are participating on the dc voltage control, and if one station fails, the other station can still maintain the dc voltage control.

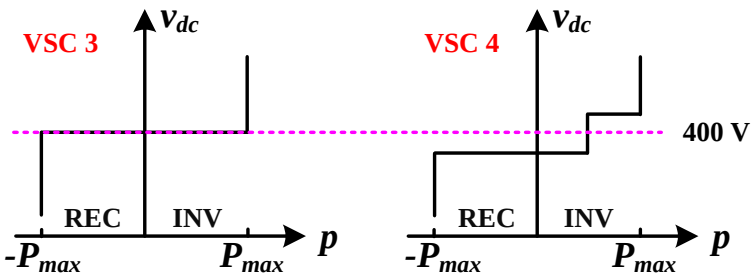


Figure 6-5. V_{dc}-P characteristic curve for voltage margin control.

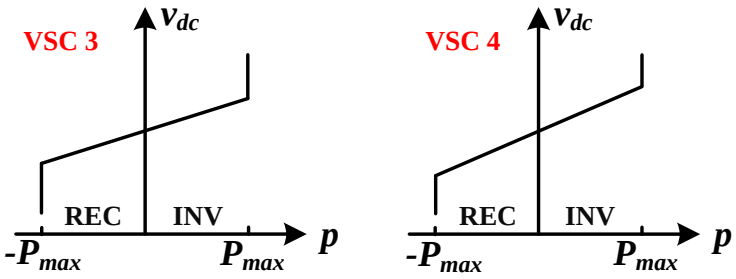


Figure 6-6. V_{dc}-P characteristic curve for voltage droop control.

Even though only two terminals are shown here as an example, both the voltage margin and droop control can be used for more than two terminals.

- *Communication*

In a real system, a system-level controller is usually needed beyond the station-level controller, responsible for command assignment (e.g. station start, stop, reset commands) and sending control references to each station (e.g. dc voltage, active power, reactive power reference). In the testbed, the system-level controller is fulfilled by another DSP and a human interface communicating to the system-level controller is built using NI LabVIEW.

Figure 6-7 shows the communication architecture in the testbed. The communication between computer (LabVIEW interface) and system-level controller is realized through RS232, and the system-level controller communicates with station-level controllers through CAN bus in DSP. The LabVIEW interface sends the commands and control references to system controller, and then the system controller dispatches the data to each station. At the same time, each station gathers the data like station status and some important measurements, and sends them to system controller. The system controller packages data and sends to Labview for real-time monitoring.

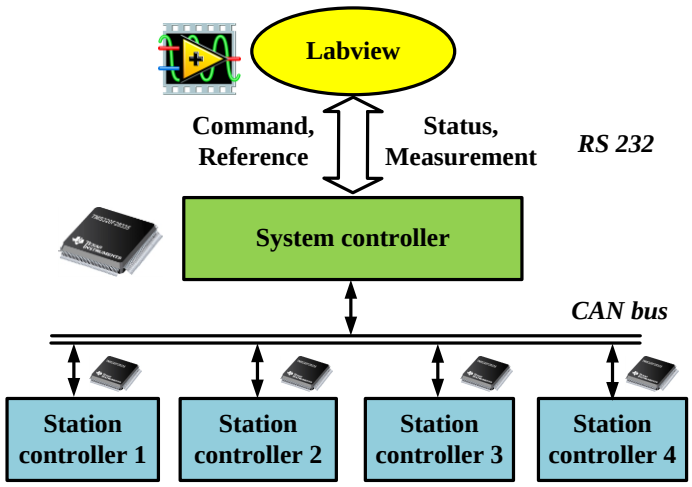


Figure 6-7. Communication architecture of the MTDC testbed.

6.3 Operation Scenario Emulation

A main purpose of developing the testbed is to understand the operation and control of the MTDC system. Therefore, the developed testbed should be capable to emulate the typical MTDC operation scenarios and demonstrate the basic control schemes. Corresponding test results will be presented in this section. In addition, several unique operation scenarios are also emulated, which have not been presented in any other testbeds but could be necessary in the real system. The emulated scenarios include:

a) system start-up

b) station online re-commission

c) station power variation

d) station online mode transition

e) station outage

The labeling of traces in the waveforms is declared here: V_{dc}, I_{dc}, I_{ac} represent the dc voltage, dc current and ac current, all at the converter terminals. The number in the subscript indicates which converter it belongs to, e.g. V_{dc1} represents the dc voltage of VSC 1. Also it should be noted that the positive active power is defined as power injecting from dc to ac.

A. System Start-up

The whole system may be shut down due to some severe faults. After the fault is cleared, MTDC system needs to restart quickly and safely. To emulate this scenario, the start-up procedure in the testbed is as follows: 1) Make sure all four cables are connected and close the dc side contactors C3 (in Figure 6-4) of all four stations. 2) Close the ac side contactor C1 of VSC 3, and the dc voltage is built up by diode rectifier through pre-charge resistor. 3) Bypass the pre-charge resistor by closing C2 and enable the dc voltage control of VSC 3. The dc voltage is then ramped to the rated value. 4) Close C2 and C3 in other stations and start the converters as P/Q mode.

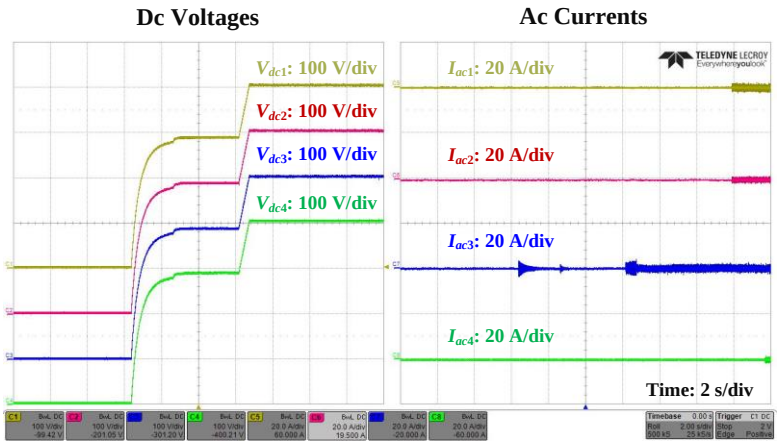


Figure 6-8. Waveform of system start-up.

This start-up procedure charges the dc-link capacitors of all four stations and dc cables at the same time. It avoids the high inrush current for energizing dc cable separately. The waveform during start-up is shown in Figure 6-8.

B. System Online Re-commission

If a station is shut down due to fault or maintenance purpose, the remaining system should operate continuously. After repair or maintenance, the station should re-commission online and not require the shutdown of the whole system. In [56], the re-commission method (**method I**) is to first build up the station dc voltage, and then close the dc switch while blocking the converter. The difficulty of this method is that the high voltage dc switch usually takes a long time to close (~ 10 seconds), which may cause a certain dc voltage decrease due to the dc link capacitor discharge. Therefore, there is voltage difference between the two sides of the dc switch when it is actually closed, generating a surge current. In [56], the voltage decay during the switch actuation delay time is estimated and the station dc voltage is charged to the grid side dc voltage plus voltage decay.

However, it is not easy to estimate the voltage decay, as the delay time is not always the same and more importantly the dc voltage discharge rate is difficult to calculate. An alternative re-commission method (**method II**) is not to block the converter, and maintain dc voltage regulating while closing the dc switch. It avoids the need to estimate the voltage decay, but the converter devices become vulnerable during the re-commission. Even though the station dc voltage is controlled equal to the grid side dc voltage, surge current may still occur and flows through the converter devices due to possible measurement or control error.

Both methods have been tested, and the test results are shown in Figure 6-9 and Figure 6-10. As the installed low voltage dc contactor closes much faster than the high voltage counterpart, the voltage decay is thus small. To emulate the inaccuracy of the voltage decay estimation for method I, the station dc voltage is charged to 2% higher than the grid side dc voltage. As for comparison, this 2% error is also applied for method II to account for the measurement and control error. As shown in the figures, the grid side dc voltage has a voltage spike when the switch is closed for both methods. This is mainly caused by the mechanical switch contact bounce, which however should not occur in the high voltage situation due to the arcing.

As shown in Figure 6-9, there is no ac current during the re-commission process as the converter is blocked. But dc current has a spike, small here but can become larger depending on the voltage difference between the two sides of dc contactor. In Figure 6-10, both ac and dc currents have a nearly step change. This is because the system power flow is changed after station re-commission. The after re-commission ac and dc currents also depend on the voltage

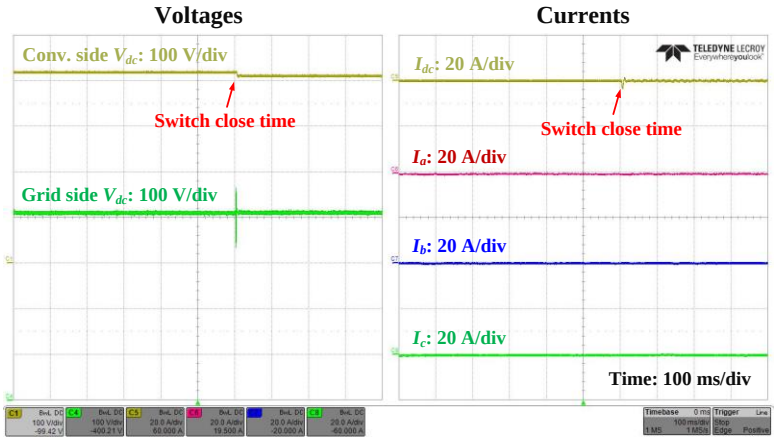


Figure 6-9. Waveform of station re-commission with method I.

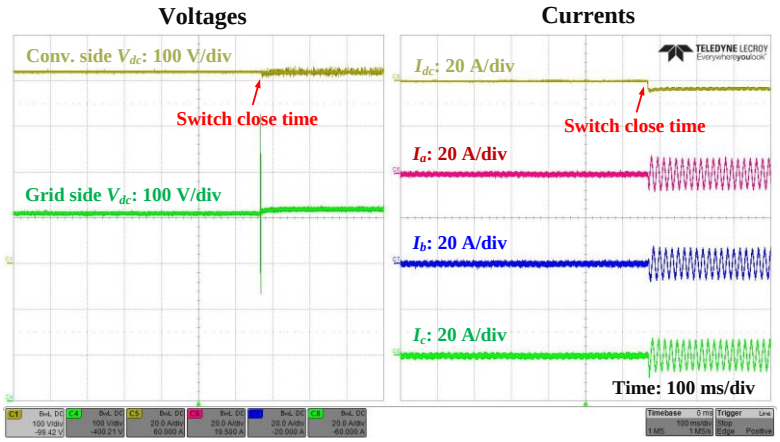


Figure 6-10. Waveform of station re-commission with method II.

difference between two sides of the dc switch, and larger voltage difference leads to higher current. But fortunately, the measurement and control error will not be that large (2% assumption is already very large), so method II should work well too.

The test results show that method I is a safer option, but more complicated. Method II on the contrary is simpler, and while the risk to converter power devices exists, it is relatively low.

C. Station Power Variation

Station power variation is one of the most typical scenarios of MTDC operation, especially for connecting offshore wind farm, where the generated power varies all the time. Both dc voltage margin and droop control are tested for this scenario. The waveforms are shown in Figure 6-11 and Figure 6-12, respectively.

1) Voltage margin control: the tested transients include: (I) VSC 1 active power ramps to -0.8 p.u.; (II) VSC 1 active power ramps from -0.8 p.u. to 0.8 p.u.; (III) VSC 2 reactive power ramps to 0.4 p.u.; (IV) VSC 4 active power ramps to -0.8 p.u.. As shown in Figure 6-11, VSC 3

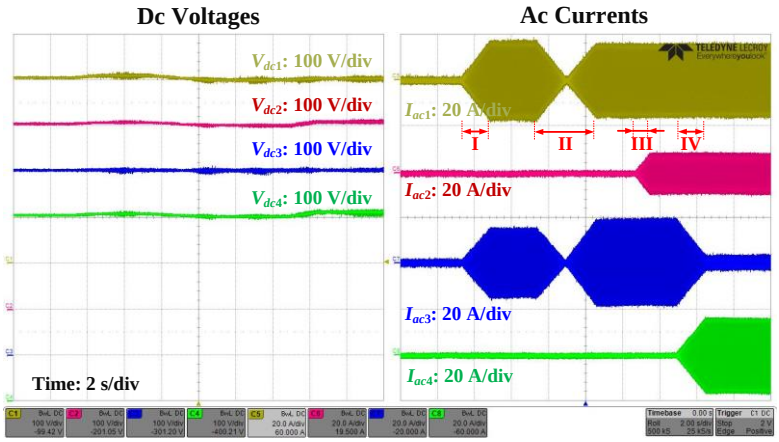


Figure 6-11. Waveform of station power variation with margin control.

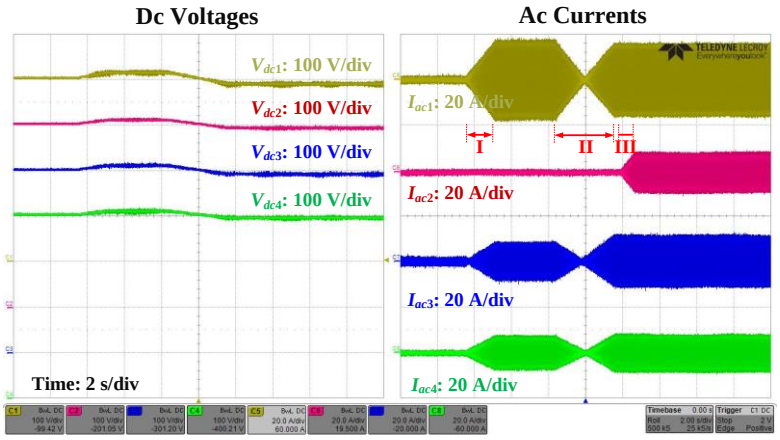


Figure 6-12. Waveform of station power variation with droop control.

adjusts its active power to achieve the power balance in dc grid, and the dc voltages are maintained well during all transients.

2) Voltage droop control: VSC 1 and 2 operate at P/Q mode, and VSC 3 and 4 operate at V_{dc}-P droop mode. The tested transients are almost the same as above except for step IV. With droop control, VSC 4 is not able to change the active power generation directly. Compared to the above case with voltage margin control, VSC 3 and 4 both adjust their active power to balance the system as shown in Figure 6-12. The droop control lets the two converters share the responsibility for power balance.

The dc voltages are maintained well for both methods. Therefore, the preference of voltage margin or droop control mainly depends on the system power dispatch requirement.

D. System Online Mode Transition

More than one control mode is usually deployed in each station. In the testbed, four control modes are implemented, which are V_{dc} control, P control, V_{dc}-P droop, and P-V_{dc} droop. There is the need, due to system requirements like power dispatch, to online change station control mode while not shutting them down. Therefore, converter online mode transition is required. Figure 6-13 shows the simplified block diagrams for V_{dc} and P control.

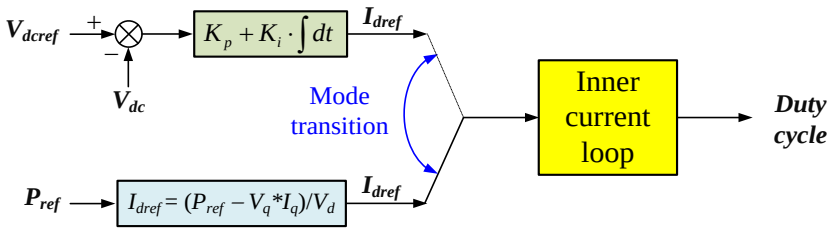


Figure 6-13. Control block diagrams of V_{dc}/Q and P/Q modes.

Transition from P control to V_{dc} control can be realized through the following steps: 1) overwrite the integrator in V_{dc} control by the current d-axis current reference (I_{dref}), and the dc voltage reference (V_{dcref}) uses the currently measured dc voltage as the initial value; 2) ramp the V_{dcref} to its target value. This ensures no abrupt I_{dref} transient during the mode transition. The transition from V_{dc} control to P control is similar, from V_{dc} control to P control is similar, and even simpler as P control is an open loop. It is fulfilled by overwriting the active power reference (P_{ref}) by the currently measured P, and then ramp P_{ref} to the target value.

Figure 6-14 shows the test result including different mode transitions. Originally, VSC 3 operates at V_{dc} control mode and the rest of the converters are at P control mode. VSC 4 and VSC 3 change to V_{dc}-P droop mode at t_1 and t_2, respectively. VSC 1 and VSC 2 then change to P-V_{dc} droop mode at t_3 and t_4, respectively. As shown in the waveform, the dc voltages are controlled well during all transitions, and dc currents change smoothly.

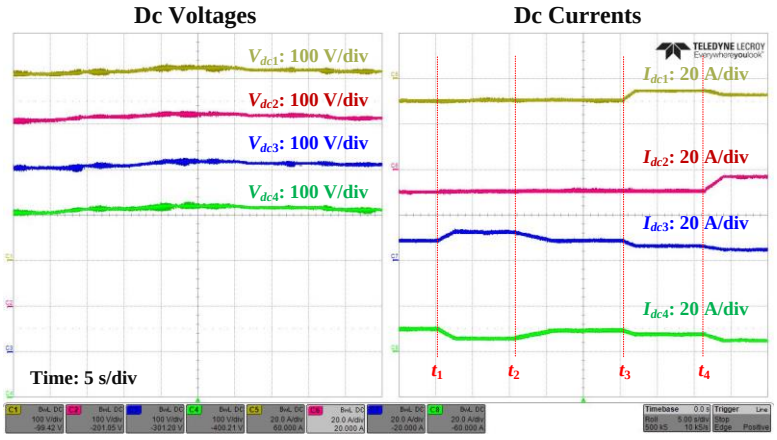


Figure 6-14. Waveform of station online mode transition.

E. Station Failure

Under some circumstances the station may lose its power transfer capability, like during ac side three-phase short circuit fault or some internal faults. The worst-case scenario is when this happens to a system voltage regulator. As mentioned in Section II, coordinated dc voltage control is needed to make sure at least one other station will automatically take over the voltage regulation responsibility, to avoid system collapse. This scenario has been tested for the MTDC system with voltage margin and droop control, respectively.

1) Voltage margin control: the test result is shown in Figure 6-15. The VSC 3, which is normally controlling the dc voltage, is blocked at t_1. The dc voltage increases quickly and reaches the voltage limit of VSC 1. Then VSC 1 changes to V_{dc} control mode and starts to regulate the dc voltage. The active power of VSC 1 is immediately reduced for power balance. As shown in the waveform, the dc voltage can be controlled well. At t_2, VSC 3 is re-commissioned. Similar to the mode transition, the initial dc voltage reference of VSC 3 is set equal to the measured dc voltage, and then slowly decreases to the target value. At t_3, VSC 1 goes back to P control mode and the dc voltage starts to decrease. Thus the station re-commission is very smooth with the voltage margin control.

2) Voltage droop control: to better demonstrate the effectiveness of droop control, the operating mode of each converter is set as follow: VSC 3 at V_{dc} control mode, VSC 4 at P control mode, and VSC 1 and 2 at P-V_{dc} mode. The test process is the same as that in the voltage margin case. As shown in Figure 6-16, when VSC 3 is blocked, VSC 1 and 2 together take over the voltage control responsibility and share the active power reduction. The system performs well for this scenario.

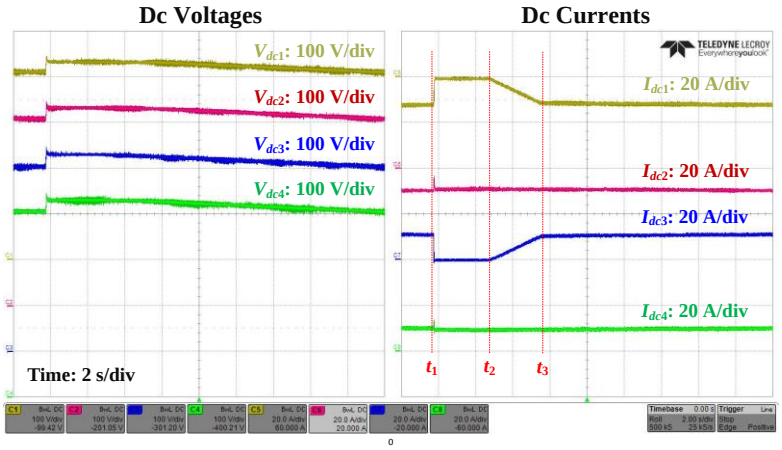


Figure 6-15. Waveform of VSC 3 failure with voltage margin control.

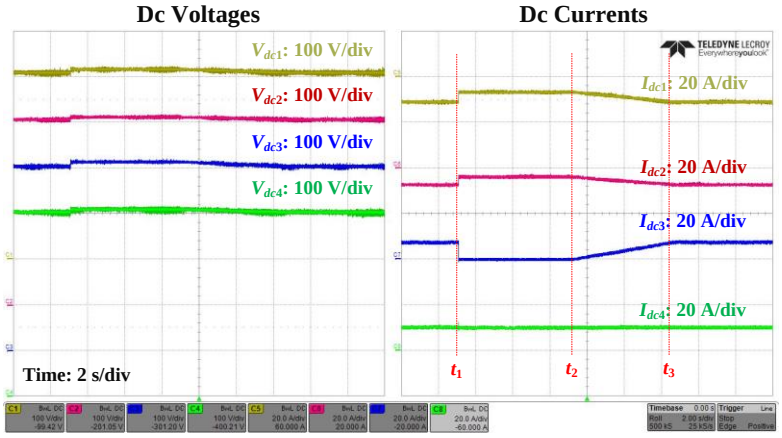


Figure 6-16. Waveform of VSC 3 failure with voltage droop control.

6.4 Conclusion

A 4-terminal down-scaled HVDC testbed is developed, based on a hypothetic system proposed for transferring power from two offshore wind farms to two onshore load centers. The developed testbed is capable to emulate several most typical operation scenarios, including system startup, power variation and station outage. Two most popular coordinated dc voltage controls – voltage margin and voltage droop, have been implemented and tested. The test results verify their capability to regulate dc voltage well in different conditions, and also reveal that their main difference is on the system power dispatch. Two unique scenarios, station online re-commission and mode transition, are also demonstrated. For station online re-commission, a new method is proposed and compared with an existing method. The proposed one has the benefit of easy implementation, but will cause inrush current which flows through the power devices in the converter. Fortunately, the inrush current is not large and should not damage the converter.

7 DC Line Current Control in MTDC

In this chapter, a dc line current control is proposed with the capability to regulate dc line current through station control. One benefit of this control is to allow the use of dc disconnects for online dc line trip. By controlling the line current to near zero, the dc disconnects with very low current breaking capability is able to trip a line without the need to de-energize the entire dc system, which is a much cheaper solution compared to utilizing a dc circuit breaker. Based on this control, a dc line current limiting function is further proposed. It helps to prevent dc line overloading, as the line current control will be automatically activated once the line is overloaded and regulate the current within the maximum allowable value. The validity of these two control schemes have been verified in the 4-terminal testbed in section 6.

7.1 DC Line Disconnection and Reconnection

If dc circuit breakers are installed in the MTDC system, dc lines can be online disconnected and reconnected for maintenance purpose or under situations like dc line short circuit fault. In the testbed, circuit breakers are installed at each terminal of the cable. Figure 7-1 shows the test results of disconnecting cable 2 at t_1 and reconnecting it at t_2. The terminal dc voltages (excluding VSC 3) vary a little after cable 2 is removed, due to the dc system power flow change. No obvious current overshoot is observed during the disconnection and reconnection processes. However, it could occur depending on the system parameters, as this transient is a step change between two different dc grid configurations. The overshoot current should not be a concern for the cable due to the short time duration, but its impact on current protection design should be considered in order to avoid false tripping.

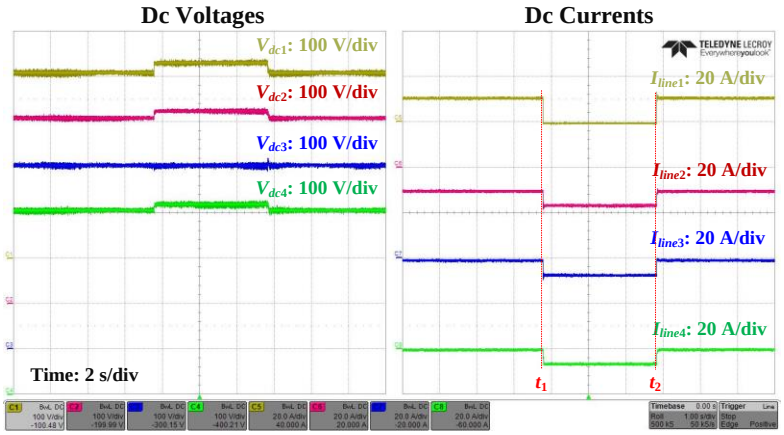


Figure 7-1. Waveform of dc line disconnection and reconnection.

7.2 Proposed DC Line Current Control

Since a cost-effective HVDC circuit breaker is still not available in the market, dc disconnects are more likely installed in the real system. Compared with the circuit breaker, HVDC disconnect has very limited current blocking capability, for example, 200 A for a commercial product in [57]. Even though the disconnect cannot replace the circuit breaker for interrupting large fault current, it is still desirable if the disconnect can be used to online disconnect the line for maintenance purpose, without de-energizing the entire system. Due to the small current blocking capability of the disconnect, only lines with very little current can be online disconnected. A dc line current control is therefore proposed. The line current will be first controlled to be small, and then get disconnected.

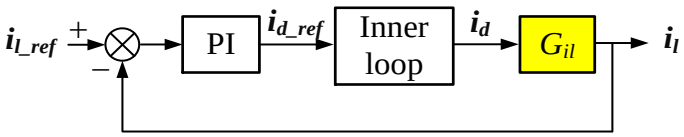
As line current depends on the line impedance and voltage difference between the two terminals, it can be controlled by terminal voltage of either connected station. Figure 7-2(a) shows a simplified block diagram of the proposed dc line current control in one station (i_l and i_{lref}

represent the line current and its reference value). It is similar to dc voltage regulator, except that the dc line current loop becomes the outer loop. The inner loop (i_d/i_{dref}) is the same, which is simplified as one block in the figure. For the controller design, the key is to find the transfer function (G_{il}) between i_l and i_d. Figure 7-2(b) gives the converter average model for two-terminal case by considering the other converter as an ideal voltage regulator. The transfer function G_{il} is derived as

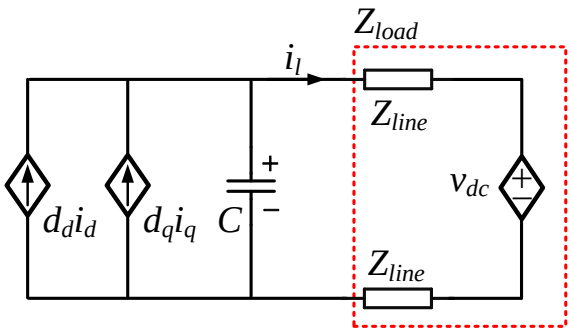
$$G_{il} = \frac{D_d}{Z_{load}/Z_c + 1}. \tag{7-1}$$

where Z_{load} is the equivalent load impedance including line impedance and voltage regulator impedance. D_d and Z_c are the d-axis duty cycle and dc-link capacitor impedance, respectively. With the transfer function, the dc line current controller can be designed. For the multi-terminal case, the only difference is the equivalent load impedance. However, the modeling of the multi-terminal system is complicated [58], and will not be covered in this dissertation.

Figure 7-3 shows the test result by implementing the line current control in line 1. At t_1, the line current control is enabled and the reference current is zero. The current of line 1 ramps to zero, while the currents of the rest lines remain almost the same. At t_2, the reference current is set to 5 A. The waveform shows the line current tracks the reference well. At t_3, the line current control is disabled and the line 1 current goes back to normal. As shown in Figure 7-3, the line 1 current is controlled well and has little impact on other lines. The dc voltage control will not be impacted either.



(a) Block diagram



(b) Average model of two-station setup

Figure 7-2. DC line current control principle.

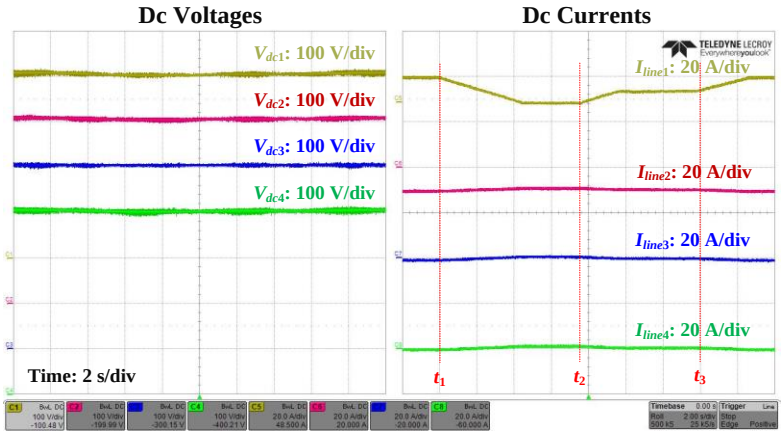


Figure 7-3. Waveform of dc line current control.

7.3 Proposed DC Line Current Limiting Function

Utilizing the proposed dc line current control, another idea is proposed for current limiting if the line is overloaded. The concept is as follows: when the line current becomes larger than the allowed maximum value, the line current control is "enabled" and regulates the current at the maximum value. If the line current goes back to the normal region, the line current control is automatically "disabled". The implementation of this line current limiting scheme is shown in Figure 7-4, which is similar to the voltage margin control. Two line current regulators are applied with the reference currents equal to the positive and negative maximum allowed line current, respectively. Normally, if the line current is within the maximum value, both line current regulators are saturated, and I_{dref} is generated by the active power regulator. But if the line is overloaded, one of the line current regulators will be desaturated and limit the current at either positive or negative maximum value.

Figure 7-5 shows a test result by implementing the line current limiting function. The left side waveform is with line current limiting function at a maximum current of 15 A, and the right side waveform is without line current limiting function. At t_1, the active power of VSC 1 is

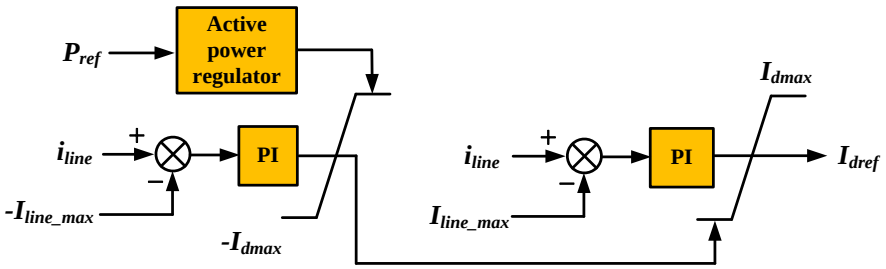


Figure 7-4. Implementation of dc line current limiting scheme.

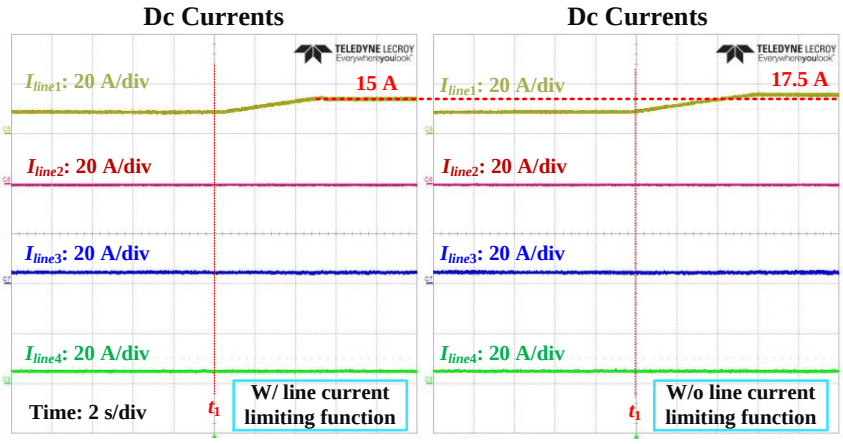


Figure 7-5. Waveform of dc line current limiting function test.

increased, and the line 1 current starts increasing. For the case without the limiting function, the line 1 current goes as high as 17.5 A, while with the limiting function, the current only reaches 15 A, which means the line current control becomes active.

7.4 Conclusion

A dc line current control is proposed and verified in the 4-terminal HVDC testbed. This control mainly has two key benefits. First, it facilitates the use of "low-cost" HVDC disconnect to online trip a dc transmission line, instead of the "high-cost" HVDC circuit breaker. Second, an automatic dc line current limiting function is further developed based on this control, which will automatically switch to current control once the transmission line is overloaded.

8 MTDC DC Fault Protection

This chapter develops a systematic dc fault protection strategy, utilizing hybrid dc circuit breakers. First, HVDC converters are temporarily blocked if dc voltage drops too much, to protect from overcurrent. Then, hybrid circuit breakers are tripped to cut off the fault current and isolate the faulted line. Finally, the HVDC converters are de-blocked and recovered to normal operating conditions, as soon as dc voltage backs to a safe range. A novel fast and selective two-step fault detection method is proposed by accommodating the special operation mechanism of the hybrid dc circuit breaker. Criteria for blocking HVDC converters and the restart are established. Voltage margin control is found to be helpful for fast system recovery. It simplifies the restart sequence for different converters and reduces the dc voltage variation during the recovery process. The overall protection strategy is demonstrated in a 4-terminal HVDC simulation platform.

8.1 Hybrid DC Circuit Breaker

Figure 8-1 shows the configuration of the hybrid dc circuit breaker proposed by ABB [12]. It contains a full solid state dc breaker branch with an additional bypass, formed by an auxiliary semiconductor based dc breaker in series with a fast mechanical disconnect. An inductor is usually in series with the hybrid breaker for current limiting purpose. During normal operation, nearly all the current flows through the bypass and the current in the main breaker is small, which lead to largely reduced losses compared to that of the pure solid state breaker. When a dc fault occurs, the auxiliary dc breaker immediately commutates the fault current to the main dc breaker, and the disconnect starts to open when the commutation is finished. The main dc

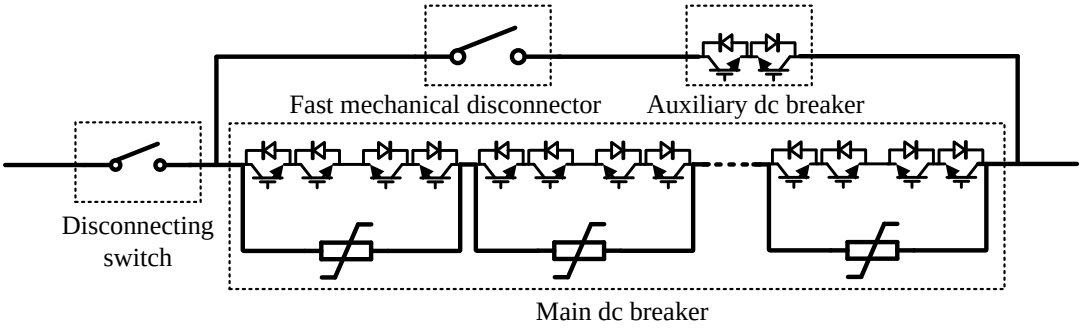


Figure 8-1. Configuration of the ABB hybrid dc circuit breaker.

breaker will be tripped once the disconnect reaches enough voltage insulation, and then the fault current flows through the arrester banks, which provide a reverse voltage to decrease the fault current. After the current reaches zero, the disconnecting switch is used to cut off the residual current of the arrestors.

The main dc breaker and auxiliary dc breaker are both semiconductor based, IGBT or IGCT may be used, which can be opened within several μs. The opening time of the hybrid dc circuit breaker is mainly determined by the fast mechanical disconnect. ABB uses Thomson drives, which has fast opening time and compact disconnect design using SF6 as insulating media, achieving an opening time less than 2 ms [59].

8.2 Fault Detection

In a dc system, the dc fault current rising rate is large, such as 3.5 kA/ms in [12]. In addition to shorten the dc circuit breaker opening time, fault detection time is also critical and should be as short as possible, to reduce the dc circuit breaker current rating. On the other hand, the detection method has to be reliable and selective, which means only the circuit breakers at each

end of the faulted line should be tripped. Buigues *et al.* [60] reviewed the detection methods proposed in the literature, and classifies them into two main categories: 1) travelling wave based method, and 2) current differential method. The basic theory of travelling wave method is that after a fault on the line, the wave of the fault will be travelling from the fault point to the system, along with subsequent reflections from the system to the fault points. The current derivative and voltage derivative are typically measured. Descloux *et al.* [61] uses the voltage of the limiting inductor for the hybrid breaker, which actually is measuring the fault current derivative. Sneath *et al.* [62] measures the derivative of the limiting inductor voltage. The advantage of travelling wave method is fast speed, but the drawback is hard to achieve full selectivity. The current differential method is also widely used in ac system protection. It has better selectivity, but needs longer detection time due to the communication between circuit breakers at both ends of the transmission line [63]. Optic fiber can be used, and the communication delay is around 1 ms for 200 km distance [65]. Since the HVDC transmission distance is usually several hundred kilometers, the communication delay could significantly impact the fault clearance time. In this thesis, a new detection method is proposed combining these two methods and achieves both fast speed and selectivity, by utilizing special operation mechanism of the hybrid dc circuit breaker.

As mentioned in subsection 8.1, the hybrid dc circuit breaker operates with two steps: first to open the bypass and then the main dc breaker. A two-step dc fault detection method is proposed to accommodate with the hybrid dc circuit breaker opening procedure. The proposed detection method includes two criteria. The first criterion is based on travelling wave method, and the bypass will open if this criterion is met. The second criterion is based on current differential method. The main dc breaker opens when the fast disconnect reaches enough voltage insulation as well as the fault is confirmed by the current differential criterion.

The proposed two-step detection method keeps the selectivity of the current differential method. If the current differential method detects the fault before the fast dc disconnect reaches enough voltage insulation, its longer detection time then does not matter and the detection time of the proposed method is only determined by the fast travelling wave method. Even if the current differential method takes longer time, the detection time of the proposed method is equivalently reduced by 2 ms. Therefore, this two-step detection method provides a frame, to combine a fast detection method and a selective one. Choosing the travelling wave method, but not the overcurrent detection used in [12], is because the travelling wave method still has certain selectivity to ensure the reliable operation if communication fails. In this dissertation, the method in [61] utilizing the voltage of limiting inductor in hybrid circuit breaker is used as the first criterion. And the second criterion uses the current differential method in [63]. The detailed criteria are shown as follows:

***Criterion* 1**: Limiting inductor voltage	***Criteria* 2**: Differential current
If $V_L > V_{th+}$; Trip	If $(I_{dc1} + I_{dc2}) > I_{th+}$; Trip
Else if $V_L < V_{th-}$; Block for 20 ms	Else if $(I_{dc1} + I_{dc2}) > I_{th-}$; Block for 20 ms
Else ; Stand By	Else ; Stand By

where V_L is the voltage of the circuit breaker limiting inductor, I_{dc1} and I_{dc2} are the line currents at the two ends as shown in Figure 8-2. V_{th+}, V_{th-}, I_{th+}, and I_{th-} are thresholds. The selection of these thresholds is explained in [61][63].

To verify the proposed fault detection method, a simulation platform is built in MATLAB based on the MTDC system in subsection 6.1. The hybrid dc circuit is added, with a 20 mH limiting inductor. The system structure is redrawn in Figure 8-3, with detailed system in Table 5.

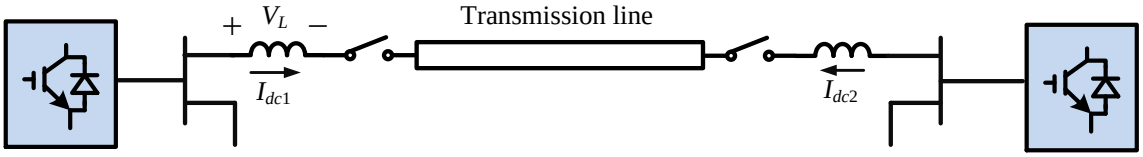


Figure 8-2. Required measurement for the proposed detection method.

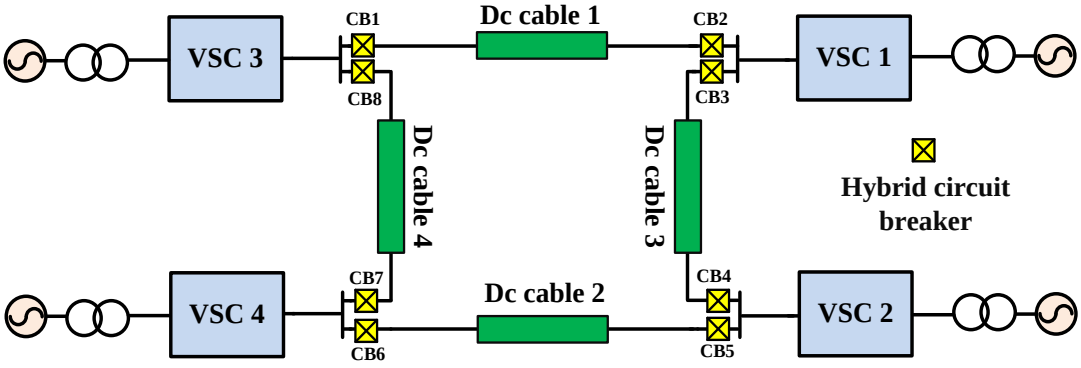


Figure 8-3. Structure of the 4-terminal HVDC system in simulation.

Table 7. DC cable parameters

Description	Cable 1	Cable 2	Cable 3	Cable 4
Capacitance	27 μF	14.7 μF	6.6 μF	14 μF
Inductance	32.4 mH	27.4 mH	28.5 mH	40.3 mH
Resistance	2.08 Ω	1.55 Ω	5.95 Ω	10 Ω

The dc cable is represented by a 2-section π model, as shown in Figure 8-4. The cable parameters are given in Table 7. In the simulation, both 2-level converter and MMC are tested. Due to the similarity, only the results with 2-level converter are presented.

Pole-to-pole short circuit fault at two different locations of cable 1 are tested, one at the middle point and the other at the cable end close to VSC 3. Figure 8-5 to Figure 8-8 show the measurements of the limiting inductor voltages and differential currents for these two scenarios.

As shown in the figures, both criteria are selective for these two particular scenarios. However, the threshold voltage for criteria 1 has to selected within a small region of [0.2, 0.3] p.u.. To provide full selectivity, the suitable region for the threshold voltage could be even smaller and may not exist considering different fault locations and short circuit impedances. On the contrary, the differential current criterion has much better selectivity. The inductor voltage threshold is selected as 0.3 p.u., and 5 p.u. for the differential current threshold in the simulation. The detection time is simulated for four different fault scenarios, including pole-to-pole fault and pole-to-ground fault at two different locations, middle point and cable 1 end close to VSC 3.

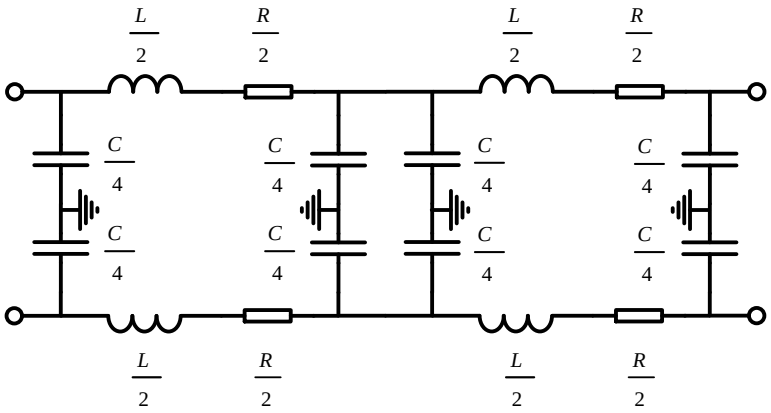


Figure 8-4. DC cable 2-section π model.

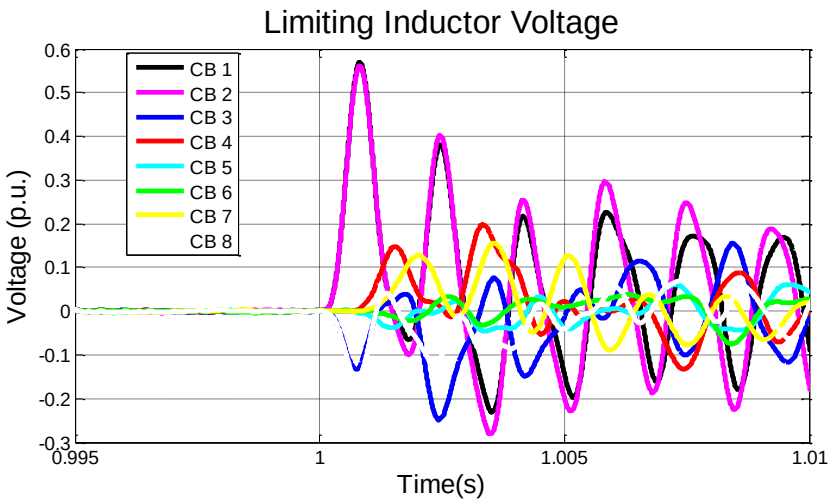


Figure 8-5. Limiting inductor voltage for pole-to-pole fault at the middle point of cable 1.

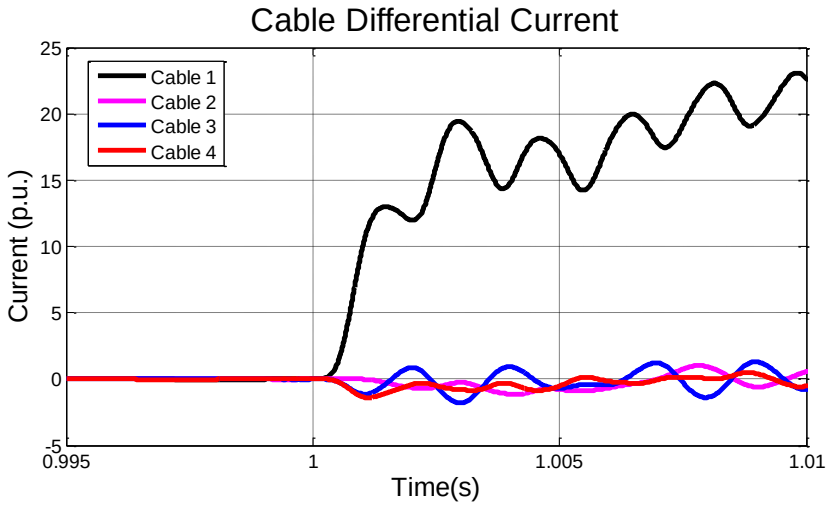


Figure 8-6. Differential current for pole-to-pole fault at the middle point of cable 1.

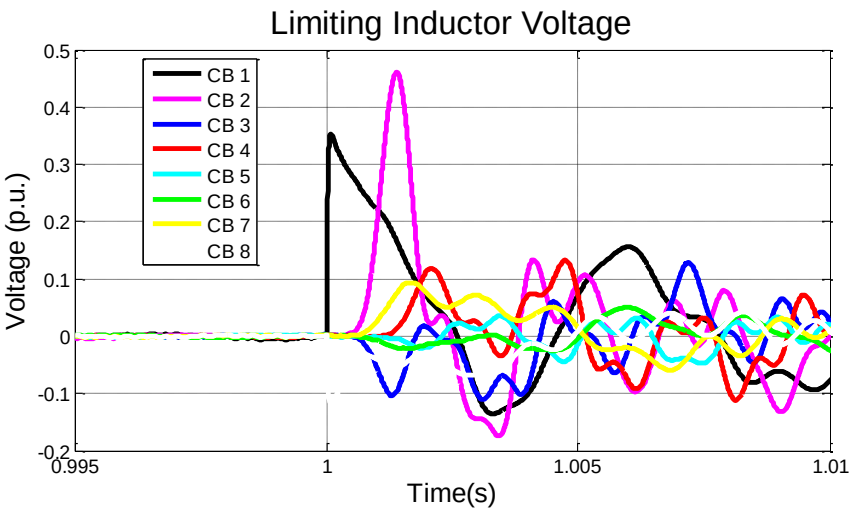


Figure 8-7. Limiting inductor voltage for pole-to-pole fault at cable 1 end close to VSC 3.

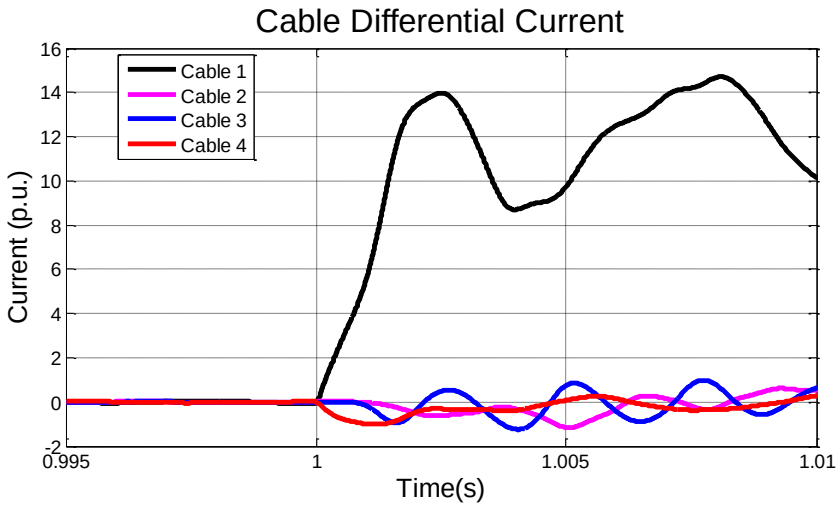


Figure 8-8. Differential current for pole-to-pole fault at cable 1 end close to VSC 3.

The resulting detection time is summarized in Table 8. For the current differential method, 0.5 ms communication delay is assumed for 100 km distance. The results show that the current differential method is slower, but the extra needed detection time is less than 2 ms. So the detection time of the proposed method is determined by the fast travelling wave method.

8.3 Recovery Strategy

8.3.1 Temporarily Blocking HVDC Converters

As mentioned in subsection 2.3, the protection methods utilizing ac circuit breaker or fault tolerant converter need to temporarily block the HVDC converters, in order to de-energize the dc system. For the system with hybrid dc circuit breaker, the need to block converters depends on many system conditions.

Table 8. Detection time of different dc fault scenarios on cable 1

Circuit Breaker Position	***Criterion 1*: Limiting inductor voltage**			
	Pole to Pole		Pole to Ground	
	Mid. point	Cable end	Mid. point	Cable end
near VSC 1	0.53 ms	1.06 ms	0.53 ms	1.07 ms
Near VSC 3	0.53 ms	0 ms	0.53 ms	0 ms
Circuit Breaker Position	***Criterion 2*: Differential current**			
	Pole to Pole		Pole to Ground	
	Mid. point	Cable end	Mid. point	Cable end
near VSC 1	1.22 ms	1.12 ms	1.22 ms	1.09 ms
Near VSC 3	1.22 ms	1.12 ms	1.22 ms	1.09 ms

Figure 8-9 shows the dc voltages for a pole-to-pole fault at the middle point of cable 1. The fault occurs at 1 s and the proposed detection method in the circuit breaker is implemented. There is a large dc voltage drop, which causes 2.6 p.u. ac overcurrent as shown in Figure 8-10. The converters thus need to be blocked for safety. The dc voltage drop varies under different conditions, such as converter is located far away from the fault location, high fault impedance, or larger dc-link capacitors. Figure 8-11 shows the results for a system with 5 times larger dc-link capacitor and a relatively large fault impedance of 10 Ω [64]. The dc voltage drop is small, and there is no ac overcurrent. For the pole-to-ground fault at the middle point of cable 1, both the ac overcurrent and dc voltage drop are much reduced compared to the previous pole-to-pole fault. The ac overcurrent is usually less than 2 p.u. which means no converter needs to shut down.

With hybrid circuit breaker, the HVDC converters may still need to be temporarily blocked under certain conditions for pole-to-pole fault. The ac overcurrent protection in each converter can be used as the converter blocking criterion. The dc fault detection in stations is also needed, to distinguish from other faults. The detection method in point-to-point HVDC system can be used [65], with the detailed criteria as:

1. Pole-to-pole fault detection criterion: $V_{dc} < 0.8$ p.u. & $I_{dc} > 1.5$ p.u.
2. Pole-to-ground fault detection criterion: $(V_p + V_n) > 0.1$ p.u.

where V_{dc} and I_{dc} are the converter terminal dc voltage and current; V_p and V_n are the converter terminal positive pole and negative pole to ground voltage.

Figure 8-13 shows the dc voltages with the detection method in stations during the pole-to-pole fault. All four stations are blocked with the detection criteria. The maximum ac current in VSC 1 is still above 2 p.u.; however, it flows through the anti-parallel diode not the IGBT.

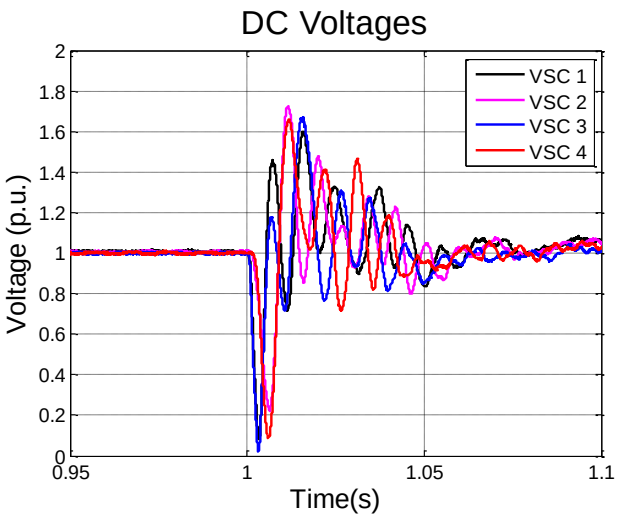


Figure 8-9. DC voltages of pole-to-pole fault at the middle point of cable 1.

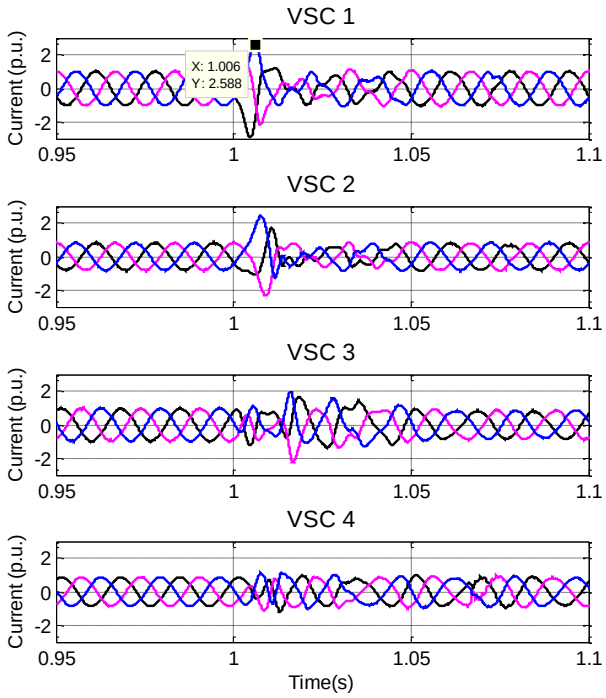


Figure 8-10. AC currents of pole-to-pole fault at the middle point of cable 1.

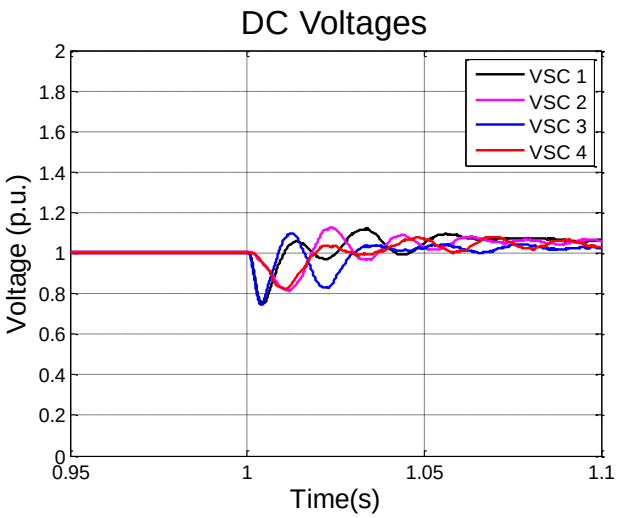


Figure 8-11. DC voltages during fault for system with larger dc-link capacitor.

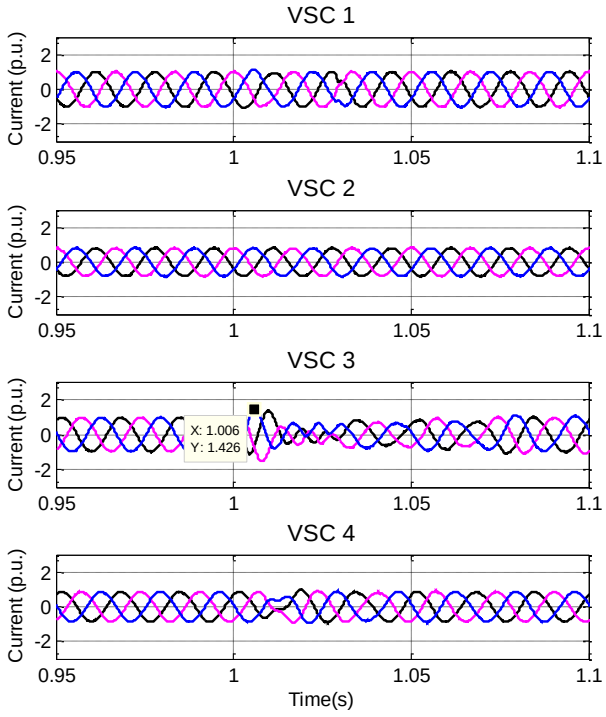


Figure 8-12. AC currents during fault for system with larger dc-link capacitor.

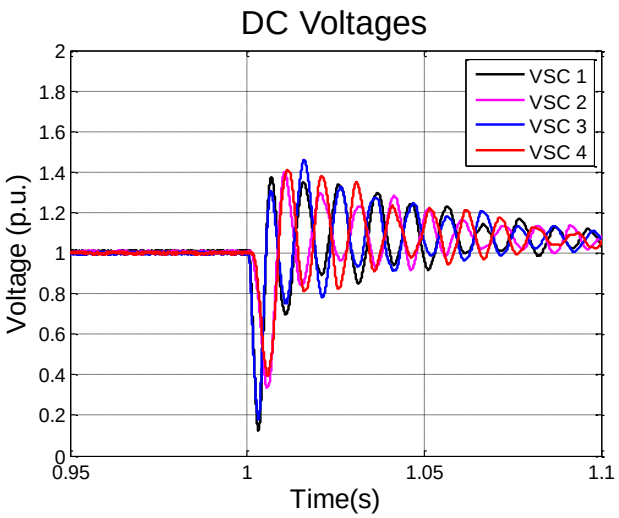


Figure 8-13. DC voltages during fault if the converters are blocked.

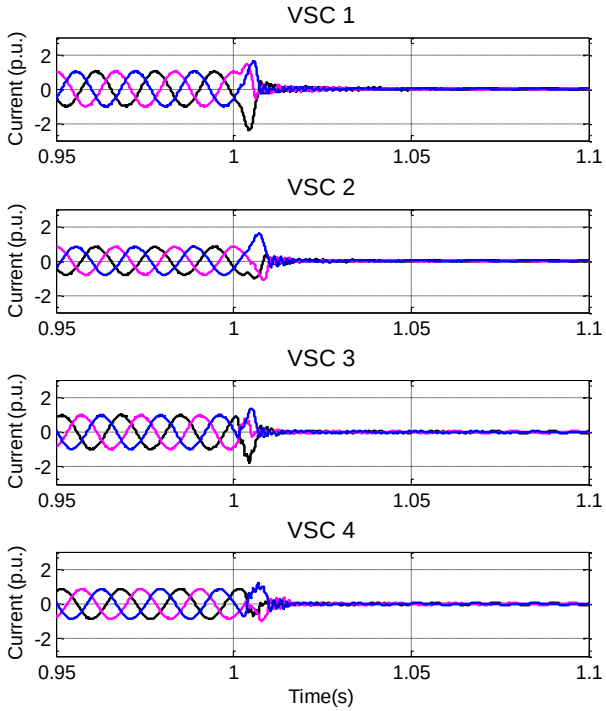


Figure 8-14. AC currents during fault if the converters are blocked.

8.3.2 Restart HVDC Converters

If HVDC converters are temporarily blocked, they should restart as quickly as possible. As shown in Figure 8-13, the dc voltage drops first and quickly comes back due to the diode rectification. The dc voltage will then have a resonance. To ensure safe operation, the converter should restart only when the dc voltage resonance dies down. So the criterion for converter to restart is developed as:

- The dc voltage is within a predefined safe range longer than certain time (10 ms is considered in this thesis).

The sequence to restart different converters is important. The dc voltage regulating converter should restart first to re-establish the dc voltage, which can be realized by using a larger voltage range for the restart criterion. The active power regulating converters use smaller voltage ranges, and should restart later. However, there are still multiple active power regulating converters, and the restart sequence also matters. The converters with the same power flow direction should not restart at the same time or too close, otherwise the voltage regulating converter will hit its maximum power limit and cause large dc voltage variation. Relying on the communication is viable, but will slow down the recovery process and is inconvenient. Even if the restart sequence does not have problem, the dc voltage regulation is hard due to the step power change on those active power regulating converters. Figure 8-15 and Figure 8-16 show the dc voltages and ac currents with the developed restart criterion for a pole-to-pole fault on the middle point of cable 1. It can be seen there is an overshoot as high as 1.25 p.u. on the dc voltages during the restart process. Some other fault locations may have even larger dc voltage variation. Ramping the active power reference during restart may help to reduce the dc voltage overshoot; however, the total recovery time can be longer and it is hard to choose a reasonable ramping rate.

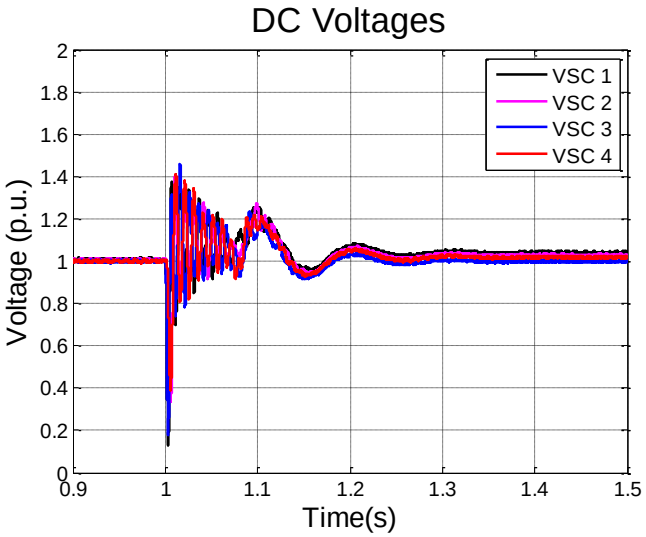


Figure 8-15. DC voltages during the restart process.

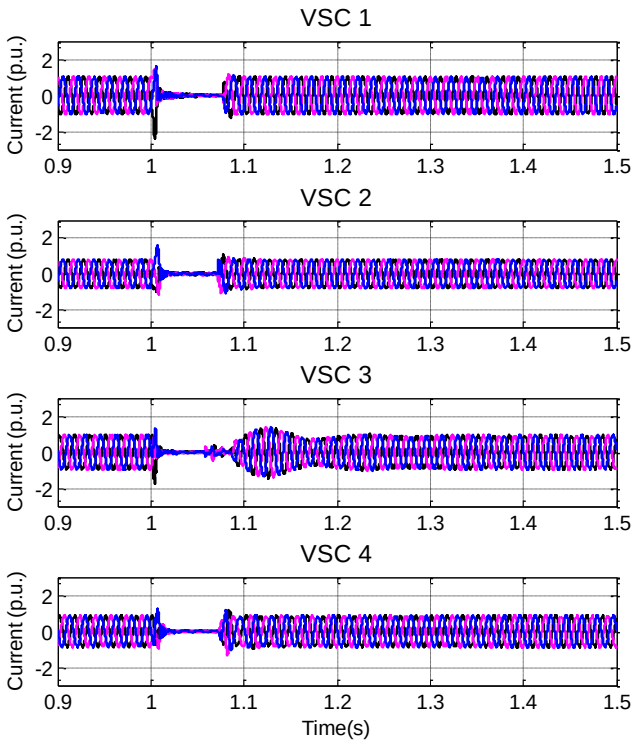


Figure 8-16. AC currents during the restart process.

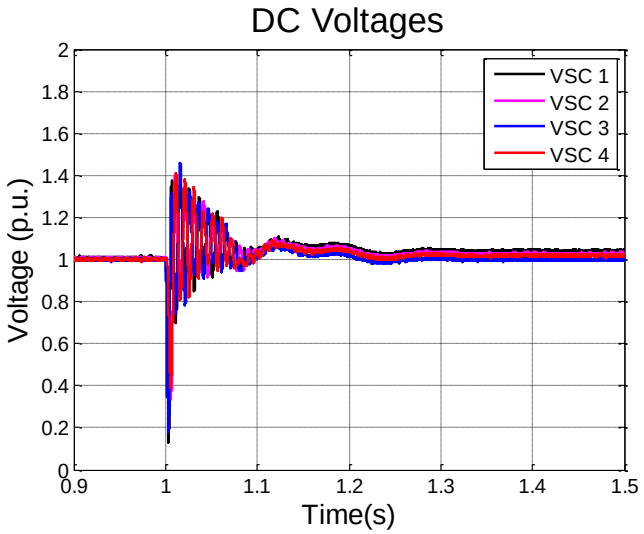


Figure 8-17. DC voltages during the restart process with voltage margin control.

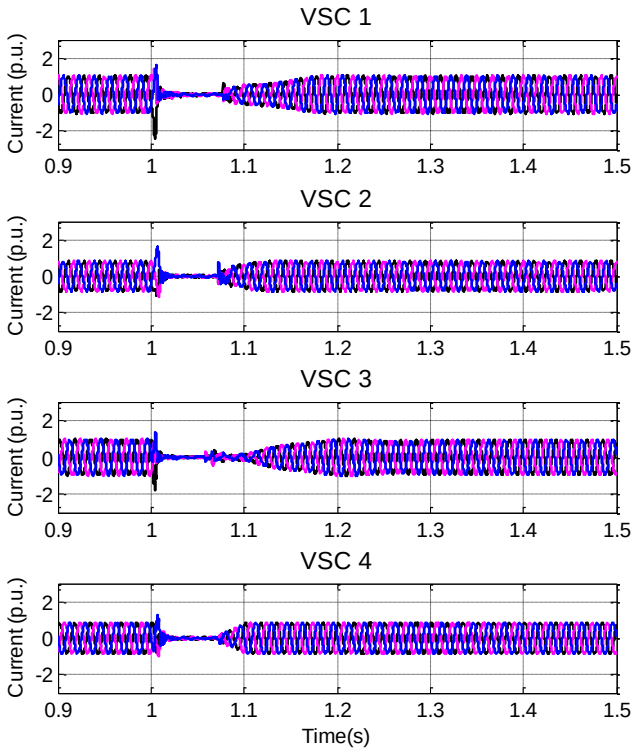


Figure 8-18. AC currents during the restart process with voltage margin control.

Therefore, a strategy without the need to emphasize the station restart sequence and with less stress on the dc voltage regulating converter is preferred. The voltage margin control is found to be helpful. The voltage margin control is a most common coordinated dc voltage control in MTDC system [54]. It provides an automatic shift between dc voltage control and active power control when the voltage or active power hits the predefined boundaries. For restarting the active power converters, voltage margin control will change the converter to regulating the dc voltage if needed, and slowly increase the active power instead of a step change. This is sort of automatically providing a most reasonable ramp rate for each station. Figure 8-17 and Figure 8-18 show the dc voltage and ac current with the assistance of voltage margin control. The dc voltages are maintained better compared to the case without voltage margin control as shown in Figure 8-15. It can also be seen that the active power regulating converters restart with an active power ramp, even though a step reference is given due to the voltage margin control.

8.4 Experimental Verification

To further verify the proposed dc fault protection strategy, experimental tests are conducted in the developed MTDC testbed. In order to test the dc fault, two dc circuit breakers are developed and installed. Also to better characterize the dc fault, parasitic capacitors are added into the dc cable in the MTDC testbed.

8.4.1 Solid State Circuit Breaker Development

Even though hybrid dc circuit breaker is considered in this Chapter, solid state circuit breaker is developed and used for the experimental verification. This is because the ultra-fast mechanical switch in the hybrid dc circuit breaker is more expensive than the solid state switch at low voltage. To emulate the opening time of the ultra-fast mechanical switch, a time delay is

programmed after the fault detection in the solid state circuit breaker. So the solid state circuit breaker can be functionally like the hybrid dc circuit breaker, and it provides the flexibility to represent different ultra-fast mechanical switch opening time.

Figure 8-19 shows the circuit diagram of the developed solid state circuit breaker. In each pole, two MOSFETs are series connected but in reverse direction, and MOV is paralleled for energy absorbing. The contactor is used to isolate the fault after the current decreases to zero, whose function is similar to the disconnecting switch in hybrid dc circuit breaker. The fuse is for protection in case of breaker failure.

Two 200 V/100 A solid state circuit breakers have been developed and the main parameters are shown in Table 9. It should be mentioned that in this Chapter, the dc voltage of the MTDC testbed is reduced to 200 V. The voltage rating of the MOV is selected to generate an approximate 1.5 times of the rated dc voltage during the maximum fault current. For the selected

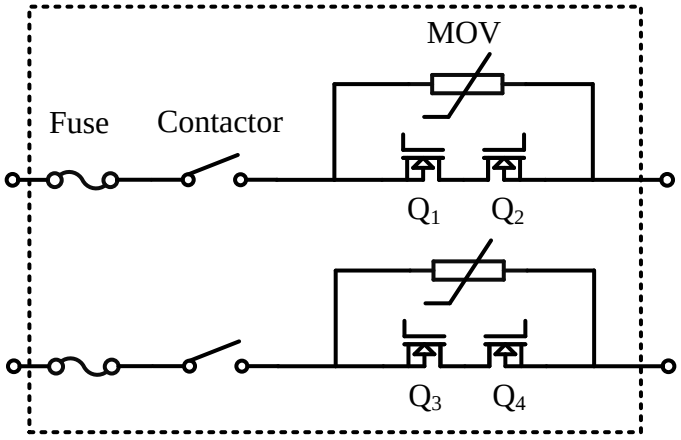


Figure 8-19. Circuit diagram of the solid state circuit breaker.

Table 9. Components of the solid state circuit breaker

Description	Parameter	Function	Manufacture #
MOSFET Q1-Q4	V_{ds}=500V, I_d=110A@25°	Cut off fault current, Overcurrent protection	STY105NM50N
MOV	$V_{m(dc)}$=65V, V_c=135V@20A, Need 2 parallel	Energy absorb circuit	Littelfuse V20E40P
Contactor	Opening time: 20~40 ms	Cut off the residual current	SIE 3RT1036-1AP60
Fuse	500 Vdc, 30A	Backup protection	Mcmaster 5054T19

MOV as shown in Table 9, the continuous allowed dc voltage is 65 V. During a dc short circuit fault, each MOV may still hold up as high as half of the dc voltage (100 V) after the MOSFETs are turned off, which is higher than the continuous allowed dc voltage of the MOV. To prevent the MOVs absorbing too much energy to blow up, the contactor has to be opened after the fault current is reduced to almost zero. If the MOV is selected with a continuous dc voltage rating higher than 100 V, its voltage at maximum fault current is increased, as well as the maximum voltage applied on the MOSFETs. In the high voltage application, power device's voltage rating increase usually cost more than adding a disconnector.

Figure 8-20 shows the photo of the developed solid state circuit breaker. A TI TMS320F28335 DSP developer board is used as the digital controller. Figure 8-21 shows the experimental setup for the circuit breaker test. The dc fault detection criterion 1 in Section 0 of utilizing the limiting inductor voltage is used.

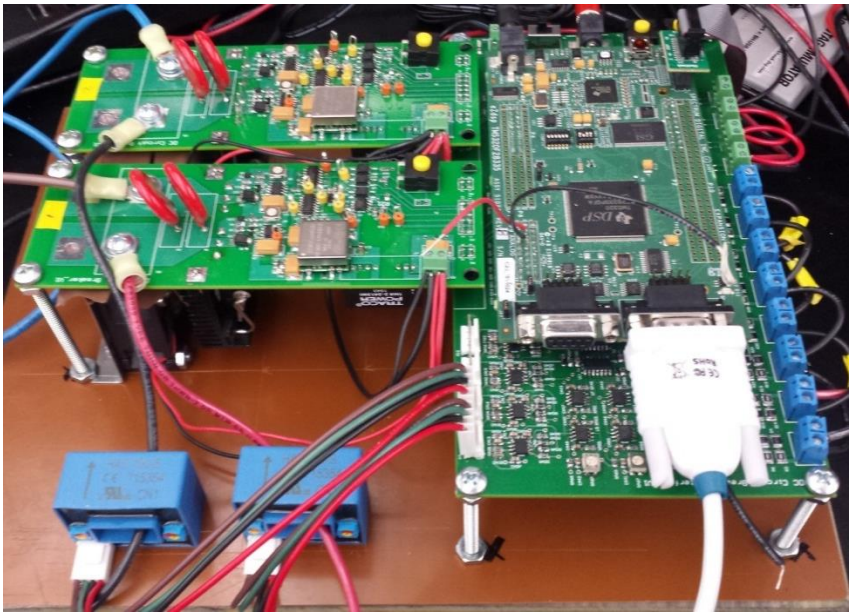


Figure 8-20. Photo of the developed solid state circuit breaker.

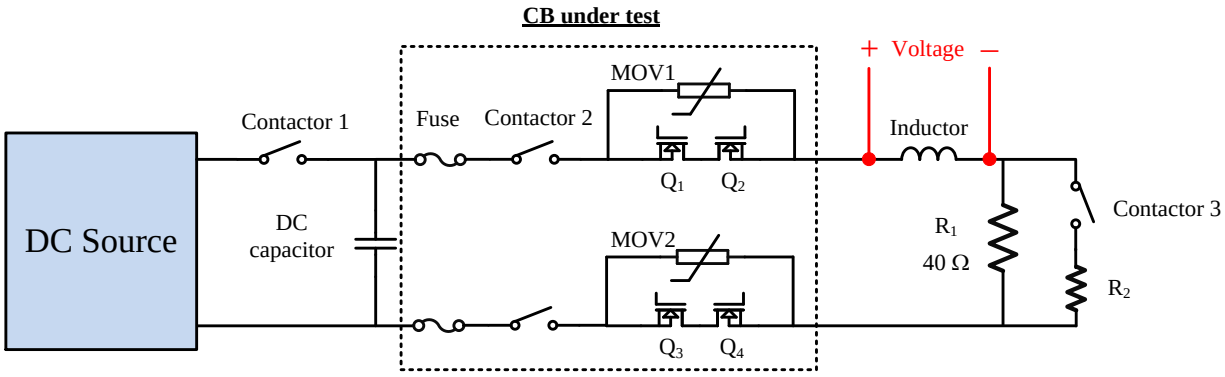


Figure 8-21. Experimental setup for solid state circuit breaker test.

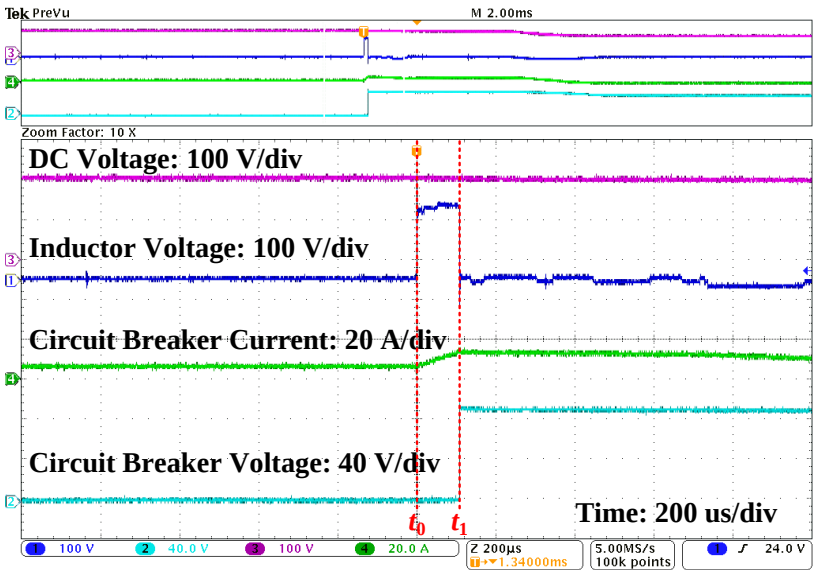


Figure 8-22. Test result with zero time delay of mechanical switch emulation.

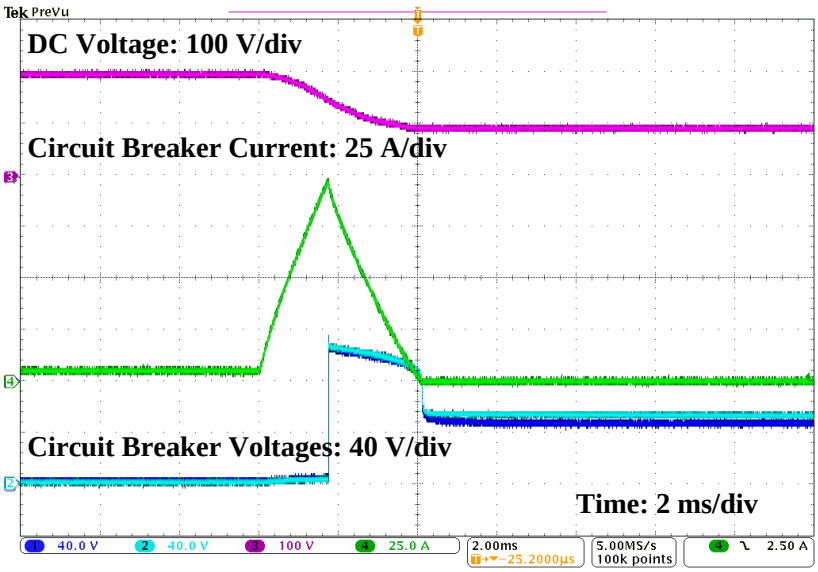


Figure 8-23. 100 A current breaking capability test.

The test procedure is as follows:

1) Close contactor 1, turn on the solid state circuit breaker (both MOSFETs and contactor 2) and open the contactor 3; 200 V dc voltage is applied, and the continuous current flowing through the circuit breaker is low due to the large resistance of R_1.

2) Close contactor 3 and open contactor 1 at the same time; R_2 is chosen with small resistance to emulate the dc fault.

Figure 8-22 shows the test result with zero time delay of the mechanical switch emulation. At t_0, the fault is created and the circuit breaker current increases. There is a step change on the inductor voltage, which makes it suitable for fast fault detection. At t_1, the solid state circuit breaker is tripped. The circuit breaker immediately takes over the voltage drop on the inductor, and the current starts to decrease. Since there is no programmable time delay in this test, the time difference between t_0 and t_1 (~ 100 us) is the required detection time of this method. It is around 2 sampling period in DSP, which includes 1 sampling period for the DSP execution. And the other sampling period required is because the filter of the voltage measurement reduces the sharpness of the sampled inductor voltage in DSP.

Figure 8-23 shows the test result under the rated current. The time delay after fault detection is tuned to achieve the maximum fault current at 100 A. It shows that the circuit breaker works fine at this condition and the voltages applied on the positive and negative branches are almost the same.

8.4.2 DC Circuit Modification in MTDC Testbed for DC Fault Test

The two developed solid state circuit breakers are installed in the two ends of the cable 1 in the MTDC testbed as shown in Figure 8-24 for the dc fault test. Originally, the dc cable in the

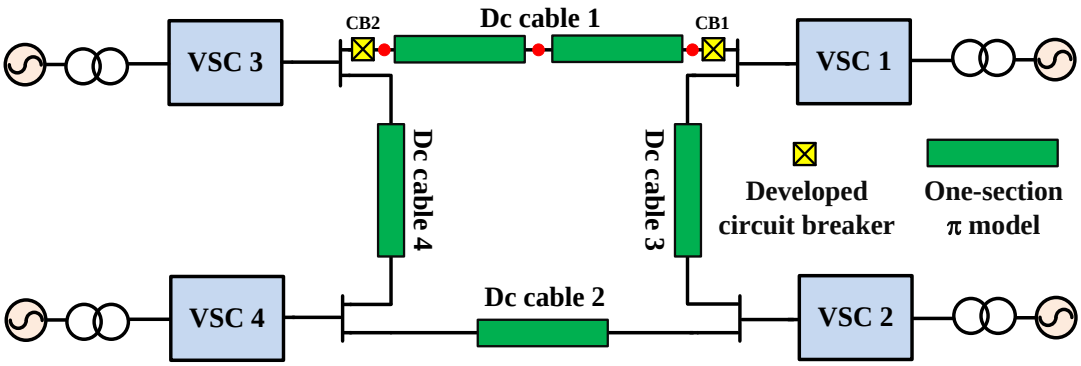


Figure 8-24. System structure with circuit breakers installed.

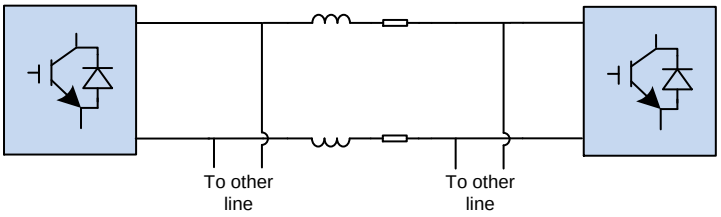


Figure 8-25. DC circuit in the original testbed.

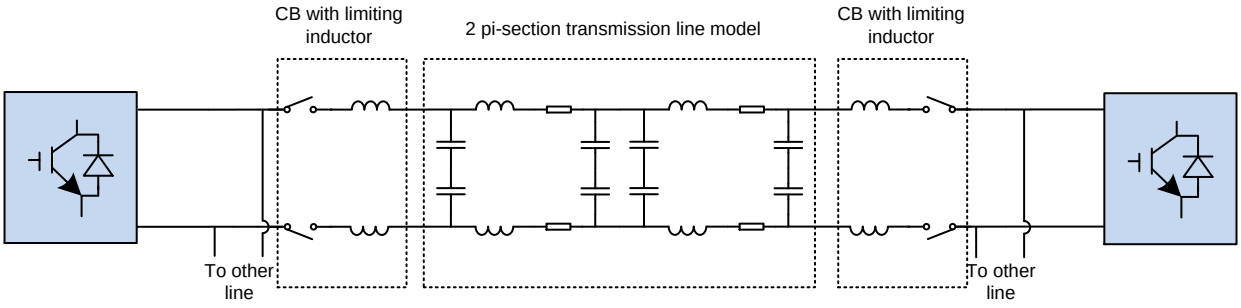


Figure 8-26. Required dc circuit for dc fault test in the testbed.

Table 10. DC fault test capability of the updated MTDC testbed

Fault type	Fault location	Fault resistance	Delay time
Pole-to-pole	Middle point of cable 1	1 Ω, 3 Ω, 6 Ω	0 ~ 5 ms
Pole-to-pole	The two ports of cable 1	1 Ω, 3 Ω, 6 Ω	0 ~ 5 ms
Pole-to-ground	Middle point of cable 1	0.5 Ω, 1.5 Ω, 3 Ω	0 ~ 5 ms
Pole-to-ground	The two ports of cable 1	0.5 Ω, 1.5 Ω, 3 Ω	0 ~ 5 ms

MTDC testbed is represented by a lumped circuit only including an inductor and resistor. But since the parasitic capacitor is important for the dc fault test, they will be added into the testbed.

Figure 8-25 shows the original dc circuit in the MTDC testbed, and Figure 8-26 shows the updated dc circuit with dc circuit breakers. Current limiting inductors are needed for the dc circuit breaker. Through the simulation with different sections of π-model for the cable, it is found that there is little difference when there are two or more sections. If only one section is used, the dc grid resonance may be different as well as the fault current. However, since the experimental test in this testbed is mainly to verify the viability of the proposed strategy, these differences are not that important. One-section π-model is used in cable without fault test. For the cable to be tested (cable 1), two-section model is used to allow fault in the middle point.

Figure 8-24 shows the updated system structure for the dc fault test. The dc fault can be created in three different locations including middle point of cable 1, the port of cable 1 close to VSC 1, and the port of cable 1 close to VSC 3. The short circuit fault is created by a contactor in series with resistors with small resistance. This test setup is also capable to do the pole-to-ground fault. The middle points of dc capacitors in converters and parasitic capacitors in dc cables are then required to connect to the ground. Table 10 lists the different fault conditions that can be

tested in the updated MTDC testbed. And the three sets of fault resistances are corresponding to the typical high, normal and small fault impedances according to [64].

8.4.3 Fault Detection Test

Figure 8-27 shows the waveforms of a pole-to-ground fault at the middle point of cable 1 with 3 Ω fault resistance. In order to get the pure fault detection time, no time delay is programmed for the circuit breaker. The detection method measuring the dc limiting inductor voltage is used, and the threshold for circuit breaker trip is set as 40 V (0.2 p.u.). Since the fault occurs at the middle point, both the limiting inductor voltages and circuit breaker currents are similar in the two circuit breakers. The limiting inductor voltage does not have a step change as in Figure 8-22, because the capacitors in dc cables, which represents the traveling waves in the real system.

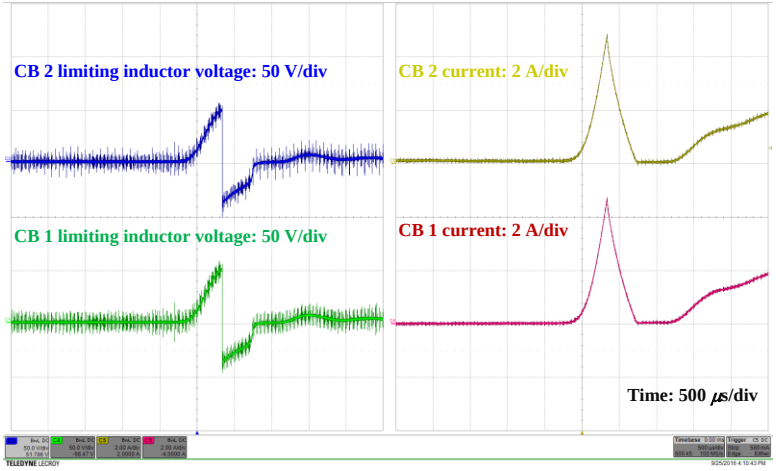


Figure 8-27. Pole-to-ground fault test at cable 1 middle point with 3 Ω fault resistance.

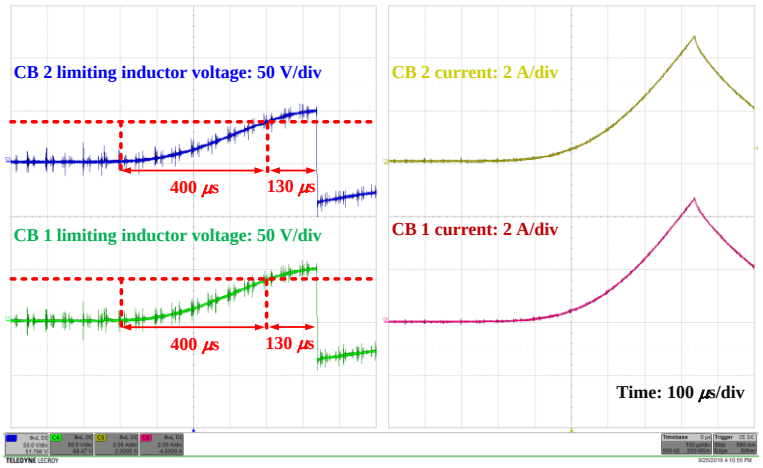


Figure 8-28. Zoomed-in waveform of Figure 8-27.

Figure 8-28 shows the zoomed-in waveforms of Figure 8-27. The limiting inductor voltage takes around 400 μs to reach the protection threshold, which is less than the 530 μs in the simulation as shown in Table 8. However, considering the threshold voltage in the simulation (0.3 p.u.) is higher than the experiment and cable parameters are not exactly the same as the scaled values from the simulation, these results are reasonable. The circuit breaker trips around 130 μs after the limiting inductor voltage reaches the threshold voltage, which is also close to the standalone test result in Figure 8-22.

Figure 8-29 shows the waveforms for a pole-to-ground fault test at cable 1 port near VSC 3. Due to the distance differences of two circuit breakers, the detection times are also different, which is consistent with the analysis and simulation results.

Figure 8-30 and Figure 8-31 shows the test results with larger fault resistance. The fault can also be detected with this method.

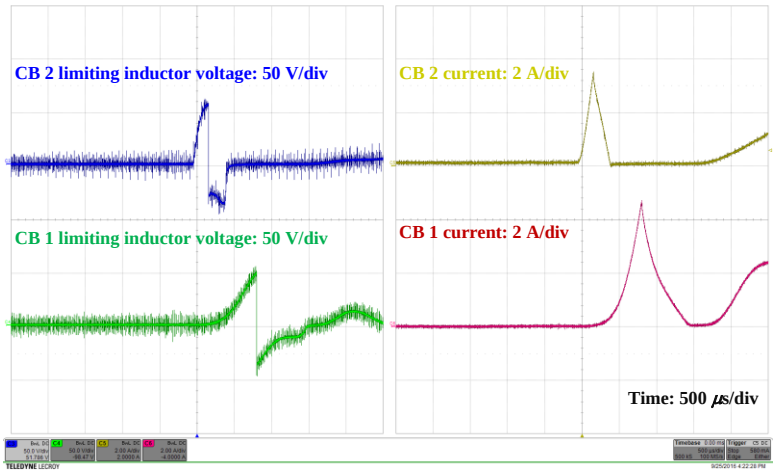


Figure 8-29. Pole-to-ground fault test at cable 1 port near VSC 3 with 3 Ω fault resistance.

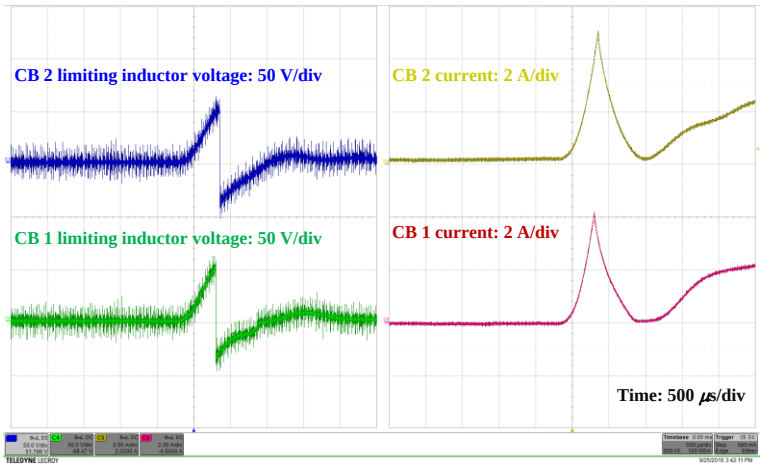


Figure 8-30. Pole-to-ground fault test at cable 1 middle point with 6 Ω fault resistance.

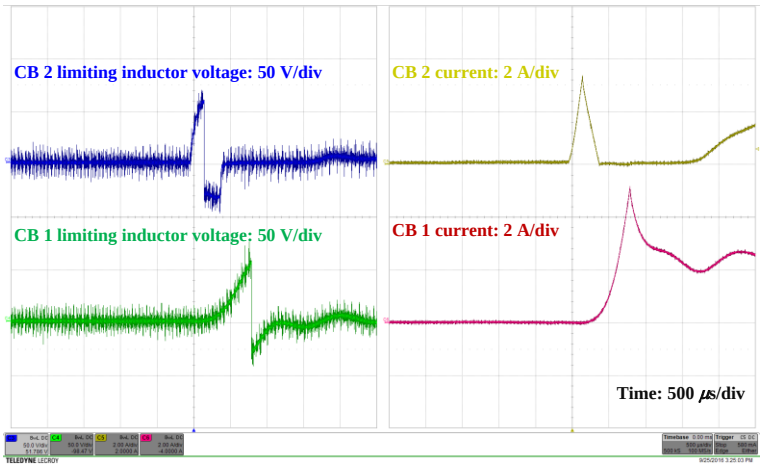


Figure 8-31. Pole-to-ground fault test at cable 1 port near VSC 3 with 6 Ω fault resistance.

8.4.4 Fault Test without Blocking HVDC Converters

This section shows the test results with the fault detections in HVDC converters disabled on purpose, to better show the system performance after a fault and evaluate the impact of control and circuit breaker delay time.

Figure 8-32 shows the test results of a pole-to-pole fault at cable 1 port near VSC 3. The test conditions are: 1 Ω fault resistance, 4 ms circuit breaker delay time and zero converter normal current. At t_0, the fault occurs and the dc fault currents flowing through the circuit breakers increase immediately. As shown in the waveforms, the converter dc voltages drop immediately and the ac currents increase. At t_1, the circuit breakers at both ports of cable 1 trip, as can be seen from the circuit breaker voltage waveforms. The circuit breaker voltages step to around 100 V, which is related to the MOV curves and current flowing through the circuit breaker. At the same time, the dc voltages start to recover and the circuit breaker currents are decreasing. Since the converters are not shut down, the dc system voltage is still applied on the circuit breakers. So

there is current still flowing through circuit breakers even though they are tripped, as well as the ac current of VSC 3 which regulates the dc voltage. After the circuit breaker current is less than a threshold for around 40 ms, the contactor is opened at t_2 to fully isolate the fault.

As shown in Figure 8-32, the maximum fault current flowing through the circuit breaker reaches around 60 A, which is below the circuit breaker current rating. The maximum ac current is 25 A, which is around 1.3 p.u. (base current is 19.6 A). The dc voltage of VSC 3 drops as low as half of the rated value. Figure 8-33 shows the test results with a smaller circuit breaker delay time (0.5 ms). The maximum circuit breaker fault current is much reduced, as well as the dc voltage drop. The maximum ac current, on the contrary, is only slightly reduced from 25 A to 20 A. The test results show that the shorter circuit breaker delay time, i.e. shorter opening time of

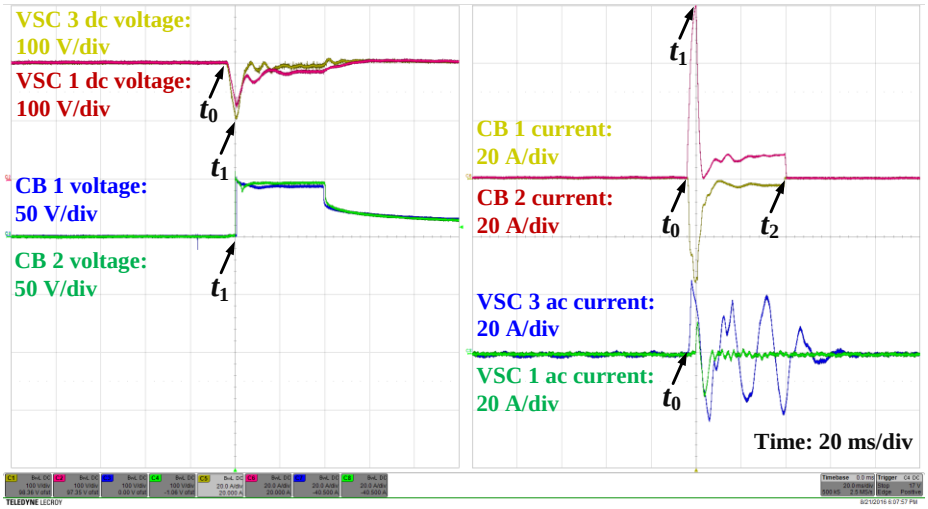


Figure 8-32. Pole-to-pole fault at cable 1 port near VSC 3 (1 Ω fault resistance, 4 ms circuit breaker delay time, zero converter normal current).

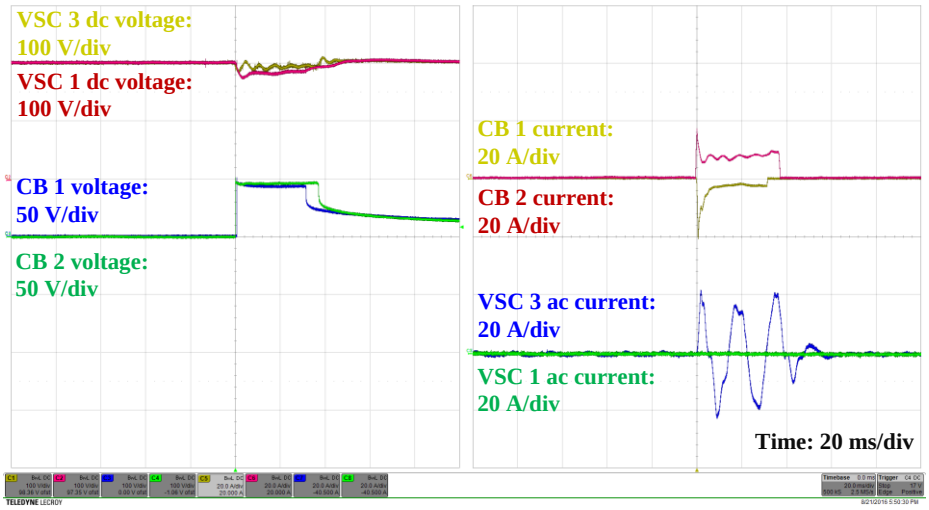


Figure 8-33. Pole-to-pole fault at cable 1 port near VSC 3 (1 Ω fault resistance, 0.5 ms delay time, zero converter normal current).

the ultra-fast mechanical switch in hybrid circuit breaker, leads to much reduced fault currents in the circuit breakers. This means that shorter circuit breaker delay time can reduce the current rating of the circuit breaker. Also with faster dc circuit breaker opening time, the disturbance caused by the dc fault can be reduced. Both the dc voltage drop and the ac fault current are smaller, and the system may be able to continuously operate without blocking the converters.

Figure 8-34 and Figure 8-35 show the test results of pole-to-ground fault under similar conditions. For fair comparison, the fault resistance is selected as half (0.5 Ω) of that in the pole-to-pole fault tests. For the fault test with 4 ms circuit breaker delay time, the dc voltage drops are smaller than that in pole-to-pole fault, as well as the ac current. The circuit breaker fault current is also smaller than the pole-to-pole fault, which is because the pole-to-ground voltage at the converter terminal drops faster than the pole-to-pole voltage.

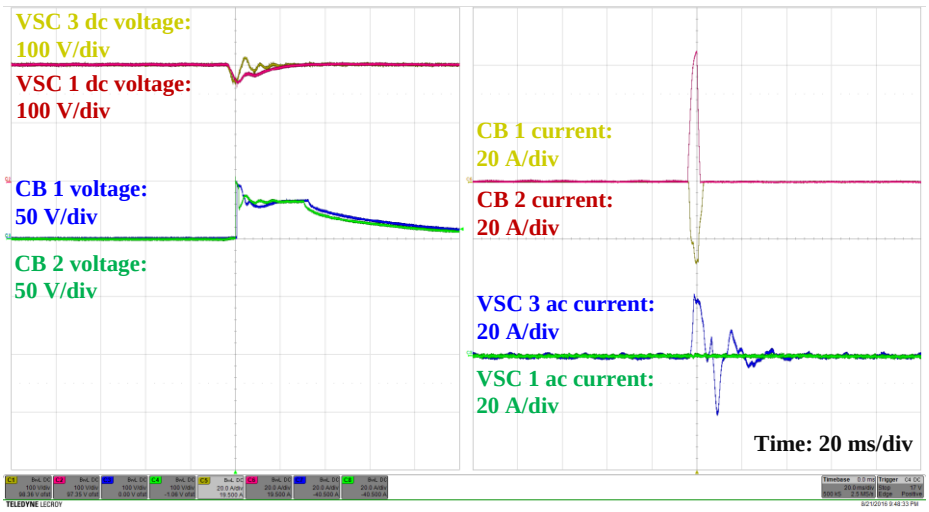


Figure 8-34. Pole-to-ground fault at cable 1 port near VSC 3 (0.5 Ω fault resistance, 4 ms delay time, zero converter normal current).

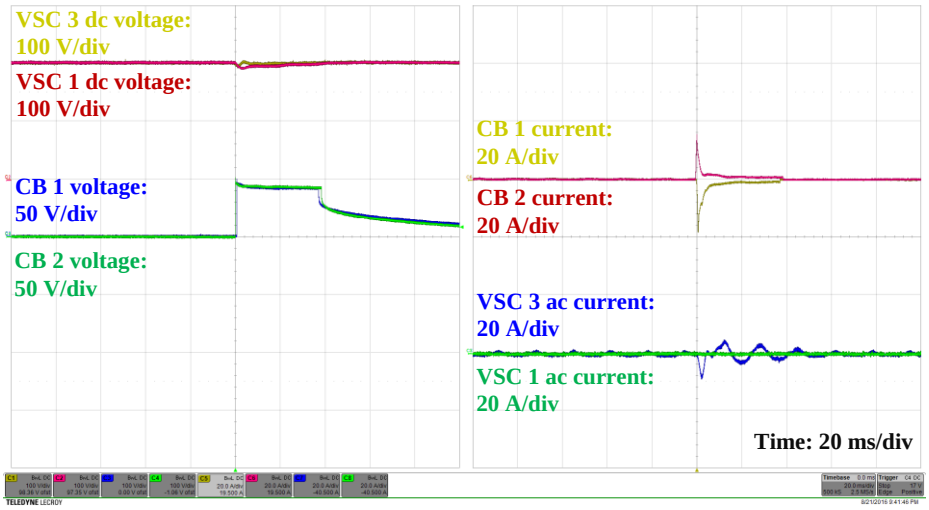


Figure 8-35. Pole-to-ground fault at cable 1 port near VSC 3 (0.5 Ω fault resistance, 0.5 ms delay time, zero converter normal current).

Faster circuit breaker opening time, similarly, leads to much reduced circuit breaker fault current and dc system voltage drop for pole-to-ground fault as shown in Figure 8-35. These test results verify that the pole-to-ground fault is less severe than the pole-to-pole fault, and the circuit breaker delay time makes a big difference on the system performance during fault.

Figure 8-36 to Figure 8-39 summarize the test results for different circuit breaker delay times under different test conditions. Some preliminary conclusions from these results are: 1) dc voltage drop becomes larger with longer circuit breaker delay time for pole-to-pole fault; for pole-to-ground fault, the dc voltage is almost constant when the delay time is large; 2) dc fault current in the circuit breaker increases with the circuit breaker delay time for both pole-to-pole and pole-to-ground faults; because the fault impedance is not zero, the fault currents are almost close to the theoretical maximum fault current which is related to the tested fault resistance, when the delay time is large; 3) the maximum ac currents are almost the same under different circuit breaker delay times for both pole-to-pole and pole to ground faults, and the values are pretty similar for these two fault types.

The maximum ac current during the dc fault is related to the ac current limitation in the control and the dc voltage drop. For the MTDC testbed, the converter is in overmodulation when the dc voltage drops to less than 0.75 p.u. And if considering the ac side inductor, the dc voltage can be even lower. In the testbed, the dc capacitor is around 2 times larger than the simulation in section 8.3, so the dc voltage drop is smaller. For the pole-to-ground fault, as shown in Figure 8-38 and Figure 8-39, the dc voltages are still higher than 0.75 p.u. So the maximum ac fault current is limited at around 1 p.u. (19.6 A). For the pole-to-pole fault, the dc voltage may drop to lower than 0.75 p.u. when the circuit breaker delay time is long, but since this time duration is short, the ac fault current may still be limited at 1 p.u. or just a little bit higher.

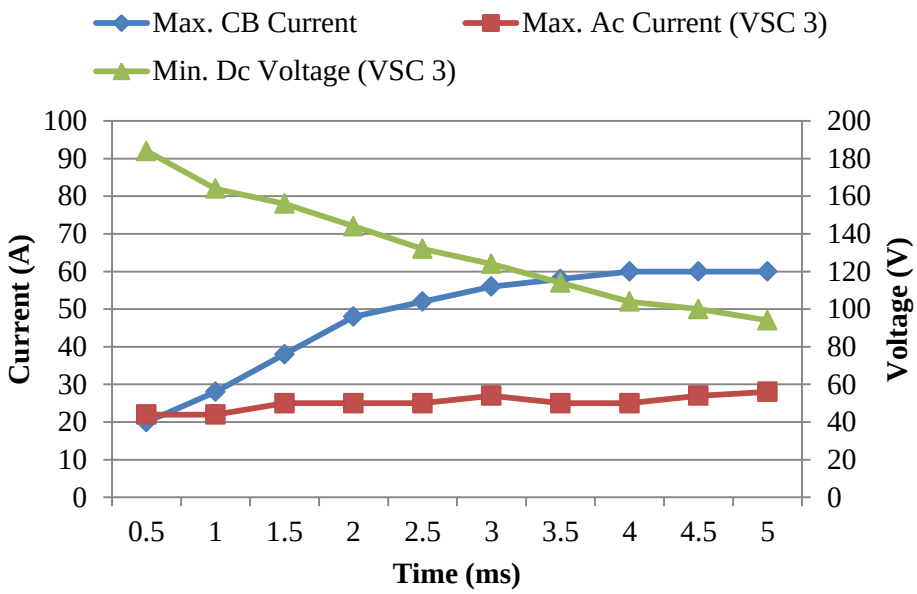


Figure 8-36. Test Results of different delay times for pole-to-pole fault at cable 1 port near VSC 3 (1 Ω fault resistance, zero converter normal current).

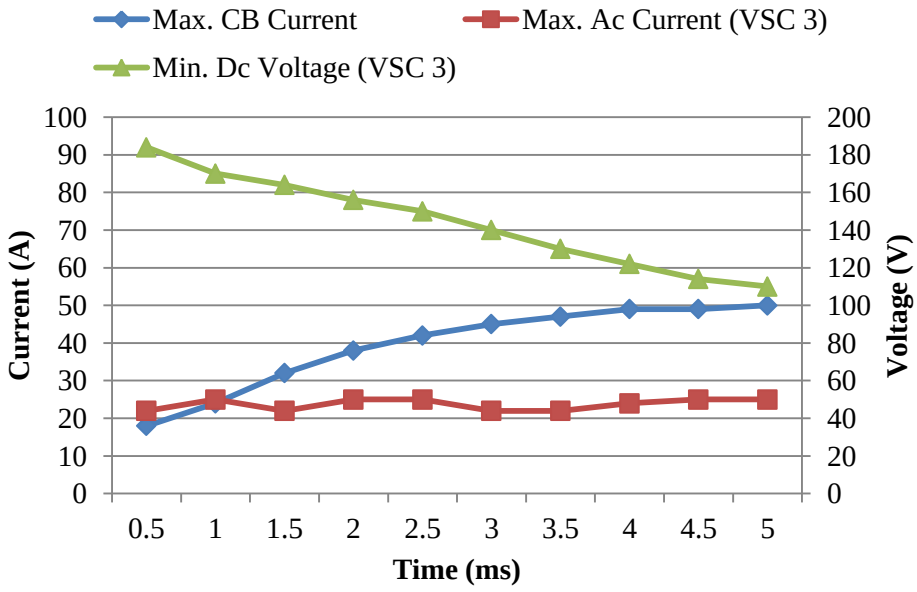


Figure 8-37. Test Results of different delay times for pole-to-pole fault at cable 1 middle point (1 Ω fault resistance, zero converter normal current).

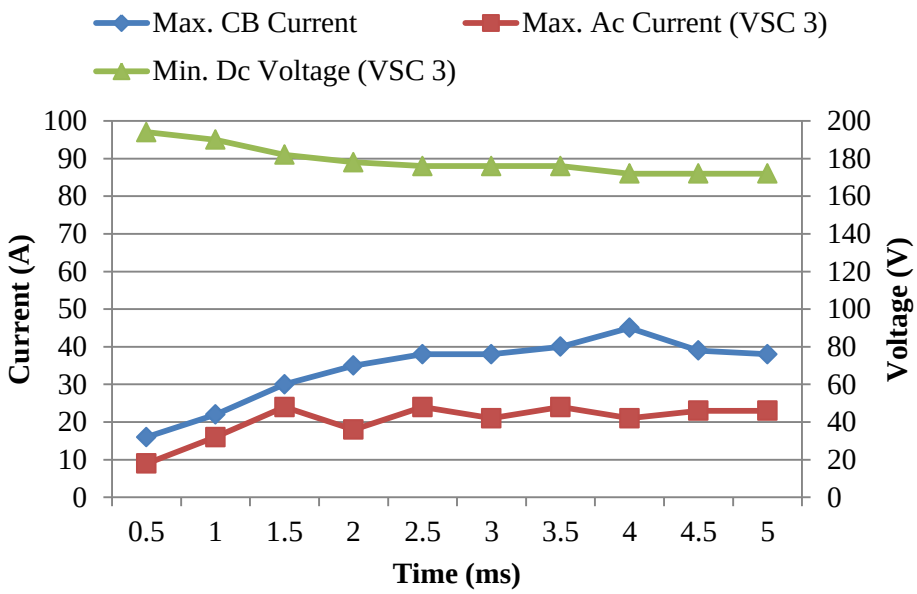


Figure 8-38. Test Results of different delay times for pole-to-ground fault at cable 1 port near VSC 3 (0.5 Ω fault resistance, zero converter normal current).

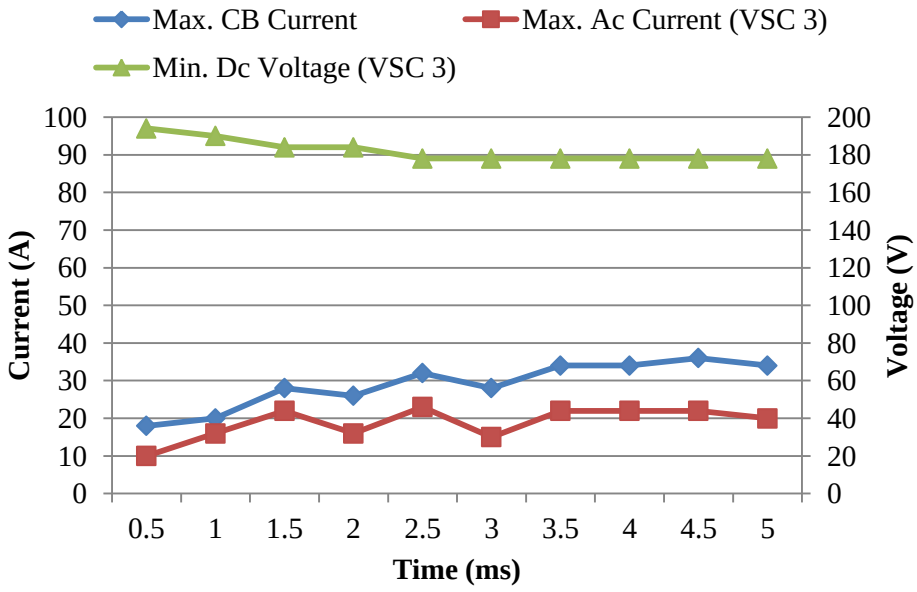


Figure 8-39. Test Results of different delay times for pole-to-ground fault at cable 1 middle point (0.5 Ω fault resistance, zero converter normal current).

A simulation platform with the same system parameters as in experiment has been developed in Matlab/Simulink. Figure 8-40 shows the simulation results (ac current waveforms) of a pole-to-pole fault at cable 1 port near VSC 3 under the same condition of Figure 8-32. The ac fault current is much larger than the experimental result. By simulating different operating conditions and trying to match the maximum fault current in circuit breaker, maximum ac current and minimum dc voltage, it is found that 0.6 Ω ac resistance is needed to match the simulation and experimental results. Figure 8-41 shows the summarized results of different circuit breaker delay times for pole-to-pole fault at cable 1 port near VSC 3. They have a good match with the experimental results in Figure 8-36.

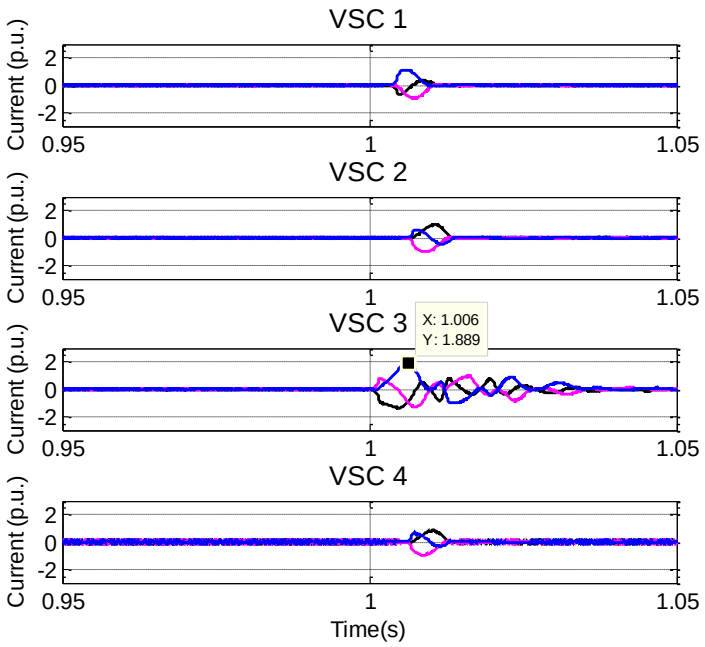


Figure 8-40. Simulation results of pole-to-pole fault at cable 1 port near VSC 3 (1 Ω fault resistance, 4 ms circuit breaker delay time, zero converter normal current).

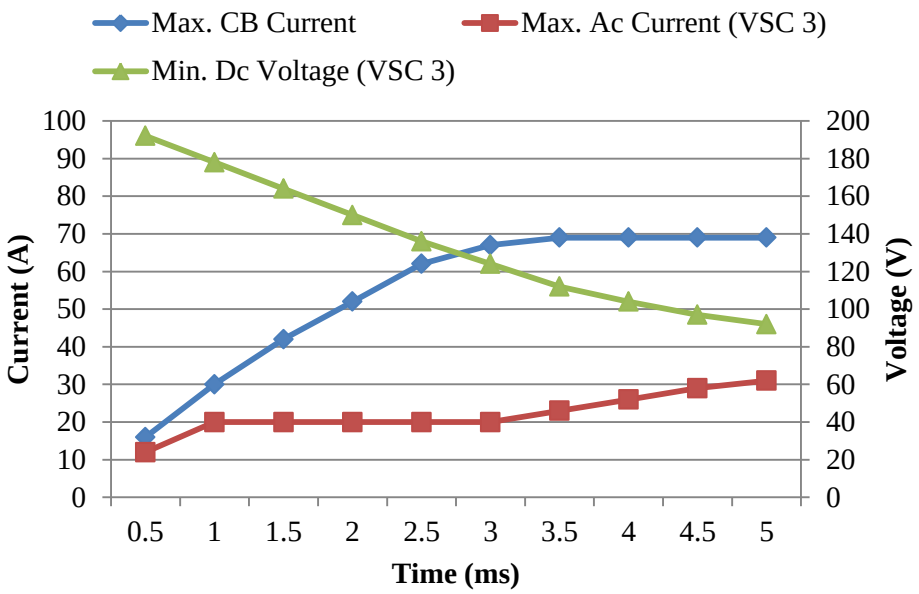


Figure 8-41. Simulation results of different delay times for pole-to-pole fault at cable 1 port near VSC 3 (1 Ω fault resistance, zero converter normal current).

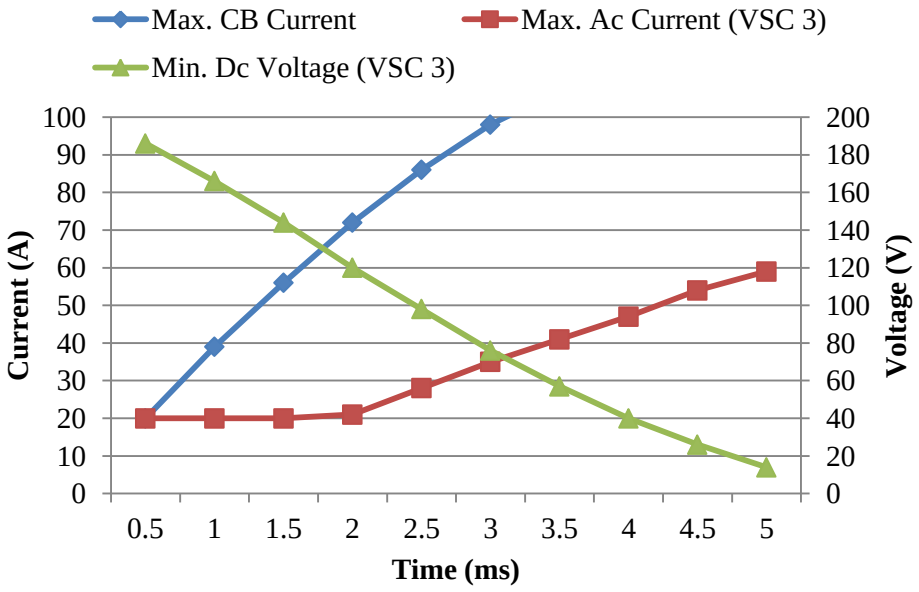


Figure 8-42. Simulation results of different delay times for pole-to-pole fault at cable 1 port near VSC 3 (0 Ω fault resistance, zero converter normal current).

Utilizing the hardware and simulation platforms, we have conducted the dc fault at different conditions to evaluate the impact of different system parameters, including the dc fault impedance and dc-link capacitance.

1) DC fault impedance impact

In the hardware tests, three sets of dc fault resistance are tested corresponding to the high, normal and small fault impedances. In the simulation, the worst case with zero fault impedance is tested, and the test results are summarized in Figure 8-42. Compared to the results in Figure 8-41, the dc voltage drop is much larger, as well as the dc fault current in circuit breaker and ac fault current. The maximum ac fault current is larger than 2 p.u. when the dc circuit breaker opening time is longer than than 3.5 ms, which means the converters need to be shut down.

2) DC capacitance impact

In the MTDC testbed, the dc capacitance is designed to store 10 ms energy of rated power, which is 2 times of the typical design. Since it is not convenient to change the dc capacitor in the hardware, the impact of dc capacitance on dc fault is evaluated in simulation. Figure 8-43 summarized the simulation results with dc capacitance designed to store 5 ms energy of rated power, i.e. half of the capacitance as in Figure 8-42. Compared to the results in Figure 8-42, the dc voltage drop becomes larger due to the small dc capacitance. It brings the benefit of reduced fault current in circuit breaker, but it slightly increases the ac fault current (when the circuit breaker opening time is less than 3.5 ms). So with small dc capacitance, the dc circuit breaker needs to be faster to prevent converter shut down, but the current breaking capability can be reduced.

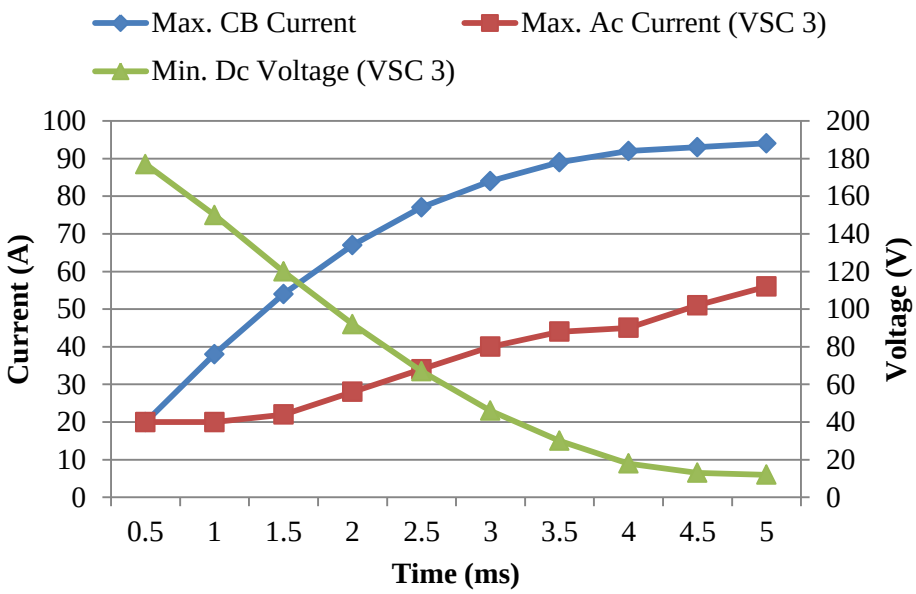


Figure 8-43. Simulation results of different delay times for pole-to-pole fault at cable 1 port near VSC 3 (0 Ω fault resistance, zero converter normal current, half the dc capacitance).

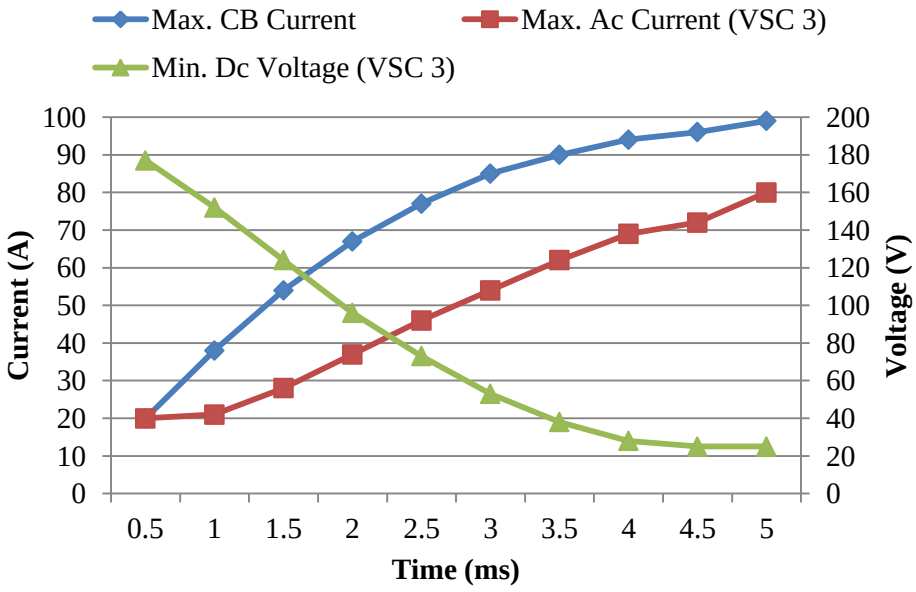


Figure 8-44. Simulation results of different delay times for pole-to-pole fault at cable 1 port near VSC 3 (0 Ω fault resistance, zero converter normal current, 0 Ω ac resistance).

3) AC resistance impact

To match the simulation and experimental results, additional ac resistance is added in the simulation. However, in the real high voltage applications, the ac resistance has to be very small. Therefore, the case with zero ac resistance is simulated and the results are summarized in Figure 8-44. Compared to the results in Figure 8-43, the dc voltage drop and dc fault current in circuit breaker do not change much, but the maximum ac fault current is much larger. Based on the results, the circuit breaker opening time has to be less than 2 ms in order to limit the maximum fault current within 2 p.u..

4) Current limitation impact

From the above experimental and simulation results, we notice that the maximum ac fault current is limited a certain value if the dc voltage is not dropped too low. This is related the ac current limitation in the control, and its impact is evaluated through experiments. Figure 8-45 to Figure 8-47 show the test results with different ac current limitations. With larger ac current limitation, the maximum ac current becomes larger, while the dc voltage drop and dc fault current flowing through circuit breaker are almost the same.

5) Power flow impact

The above tests are all conducted with zero converter normal current to better show the ac fault currents. Similar tests with converter current are conducted. VSC 3 typically has the largest ac fault current as it regulates the dc voltage, especially when the fault occurs at the cable 1 port near VSC 3.

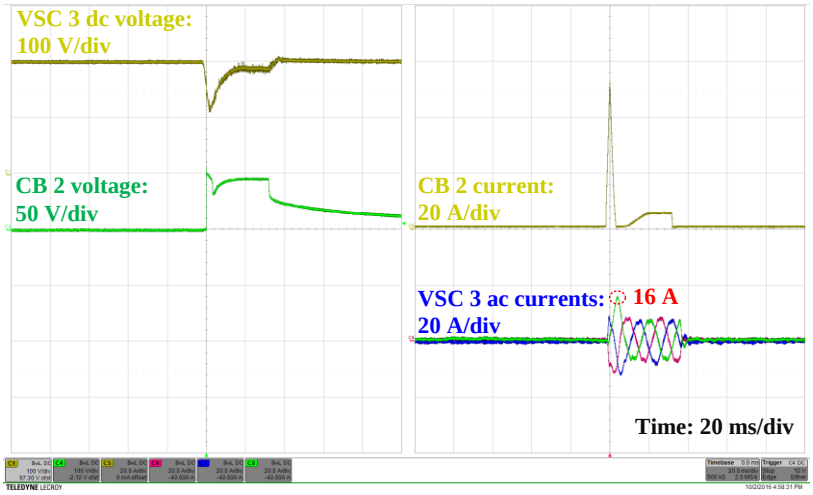


Figure 8-45. Pole-to-pole fault at cable 1 port near VSC 3 with 0.4 p.u. current limitation (1 Ω fault resistance, 2 ms delay time, zero converter normal current).

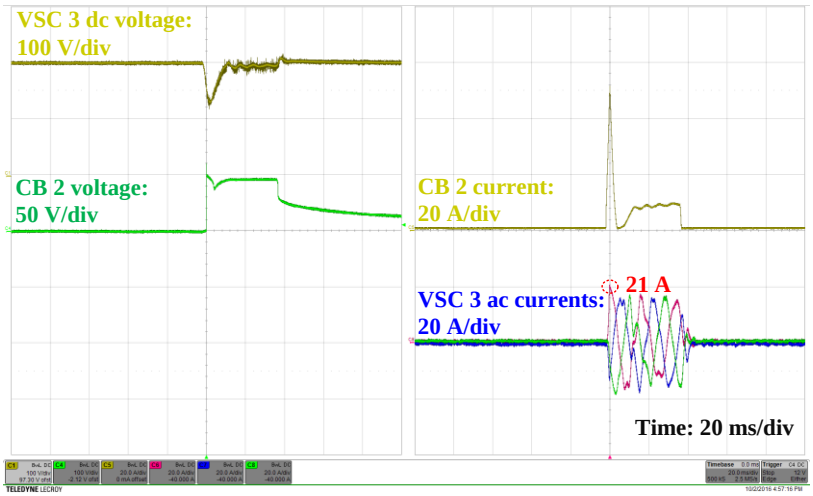


Figure 8-46. Pole-to-pole fault at cable 1 port near VSC 3 with 0.8 p.u. current limitation (1 Ω fault resistance, 2 ms delay time, zero converter normal current).

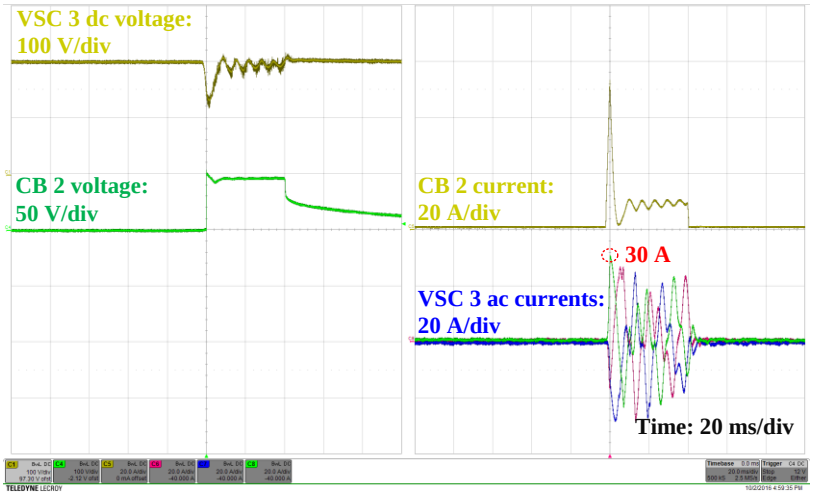


Figure 8-47. Pole-to-pole fault at cable 1 port near VSC 3 with 1.2 p.u. current limitation (1 Ω fault resistance, 2 ms delay time, zero converter normal current).

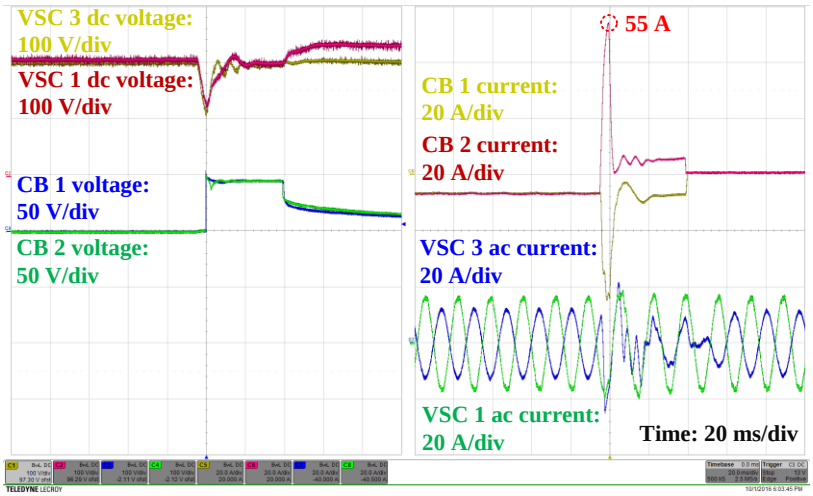


Figure 8-48. Pole-to-pole fault at cable 1 port near VSC 3 (1 Ω fault resistance, 4.5 ms delay time, VSC 3 power flow from dc to ac).

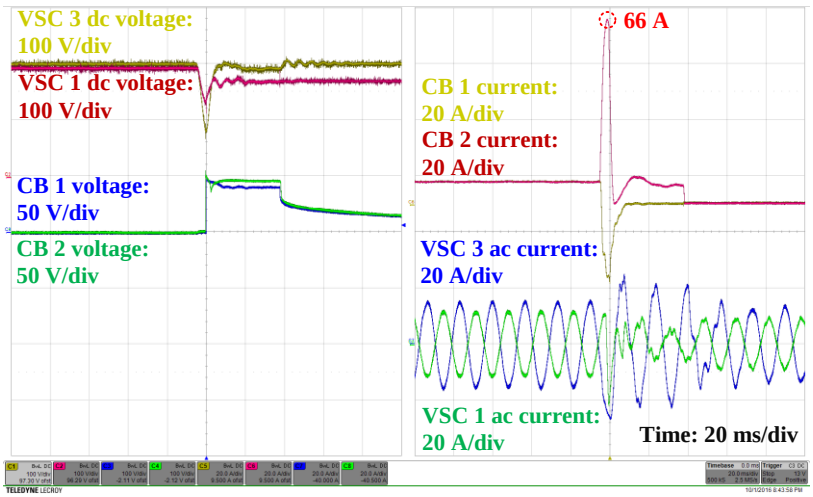


Figure 8-49. Pole-to-pole fault at cable 1 port near VSC 3 (1 Ω fault resistance, 4.5 ms delay time, VSC 3 power flow from ac to dc).

Two cases are tested: 1) VSC 3 has a power flow from dc to ac, and 2) VSC 3 has a power flow from ac to dc. The test results are shown in Figure 8-48 and Figure 8-49. The maximum ac currents are similar, which verify that they are mainly determined by the ac current limitation. If VSC 3 has the power flow from ac to dc, the dc fault current is larger and the dc voltage drop is larger. Therefore, for the dc fault current or the circuit breaker current rating, the worst case is when the VSC 3 has the largest power from ac to dc.

8.4.5 Recovery Strategy Test

According to the test results in Figure 8-36 to Figure 8-39, the maximum ac fault currents are all limited within 2 p.u. if the dc circuit breaker opening time is less than 5 ms. In other words, for our MTDC testbed, it can maintain continuous operation even during dc short circuit fault, if hybrid dc circuit breakers with less than 5 ms opening time are implemented. Figure 8-50 and Figure 8-51 show the waveforms of all four converters dc voltages and ac currents for pole-

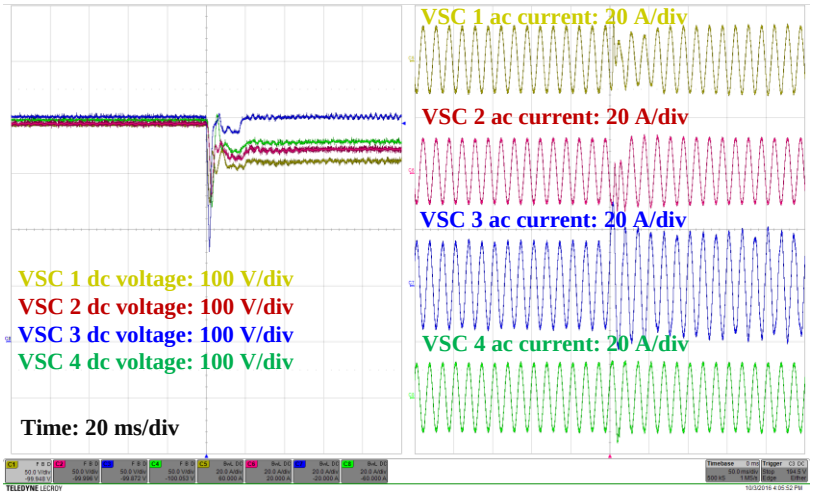


Figure 8-50. Pole-to-pole fault at cable 1 port near VSC 3 (1 Ω fault resistance, 4.5 ms delay time, VSC 3 power flow from ac to dc).

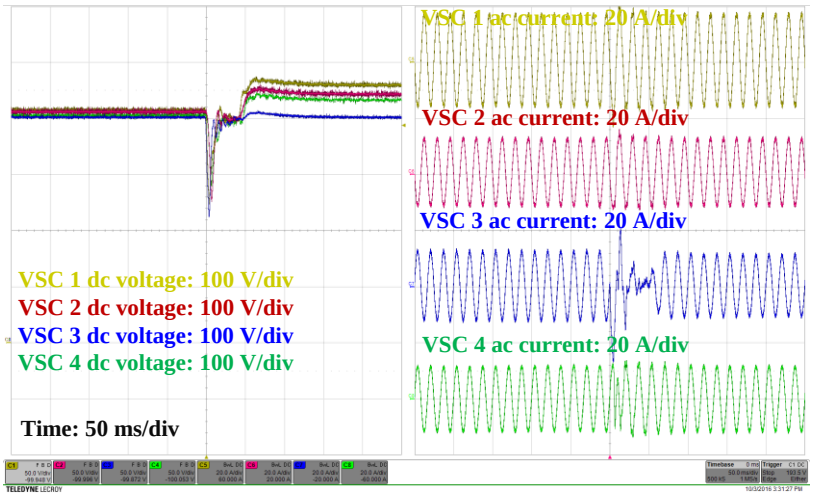


Figure 8-51. Pole-to-pole fault at cable 1 middle point (1 Ω fault resistance, 4.5 ms delay time, VSC 3 power flow from dc to ac).

to-pole fault at cable 1 port near VSC 3 with different power flow directions of VSC 3. For both conditions, the dc short circuit fault does not cause the dc system shutdown but more likely introduces a large disturbance to the system. And the system can quickly recover by isolating the faulted line.

As explained in Section 8.4.4, the dc fault performance is highly related to the dc fault impedance assumed in the tests and the ac resistance of the hardware setup. If considering the worst case using simulation, converters may need to shut down if the dc circuit breaker is not that fast (e.g. 2 ms in the evaluated system). Definitely, the requirement on circuit breaker opening speed to prevent converters shut down is also related to some other system parameters, such as dc capacitance, system power flow, ac current limitation and dc circuit breaker current limiting inductor.

In order to test the system recovery strategy proposed in Section 8.3.2, fast dc fault detection method is used, instead of the ac overcurrent protection. With more stricter detection criterion, some converters may need to shut down even though the ac current has not reached 2 p.u.. The detection criterion implemented is: V_{dc} < 0.8 p.u. and I_{dc} > 1.5 p.u., and the criterion to restart the converter is : V_{dc} is within [0.8 p.u., 1.2 p.u.] for more than 50 ms.

Figure 8-52 to Figure 8-54 show the test results with the above mentioned converter detection and recovery criteria, with different circuit breaker delay times. Figure 8-52 shows the case with 1 ms circuit breaker delay time, no converter is shut down. Figure 8-53 shows the case with 1.5 ms circuit breaker delay time, the VSC 3 is shut down due to the dc voltage drop. After VSC 3 is temporary blocked, there will be another converter regulating the dc voltage because of the voltage margin control. Therefore, the VSC 3 voltage comes back to the safe range and after

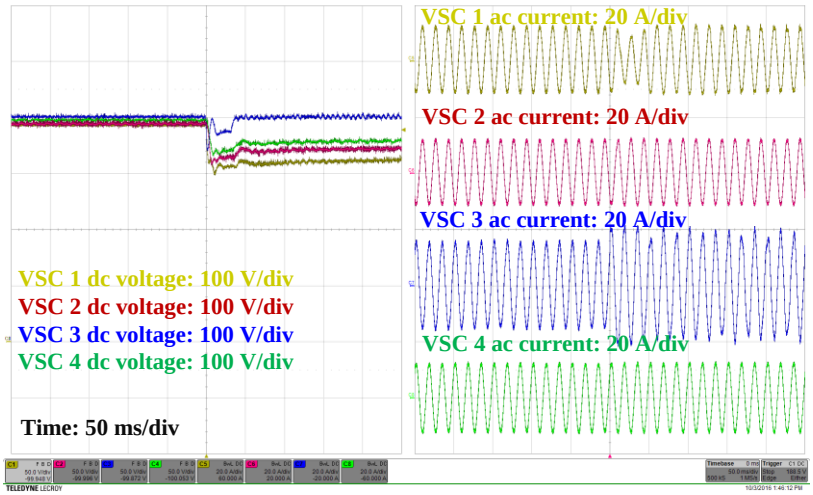


Figure 8-52. Pole-to-pole fault at cable 1 middle point (1 Ω fault resistance, 1 ms delay time, VSC 3 power flow from ac to dc).

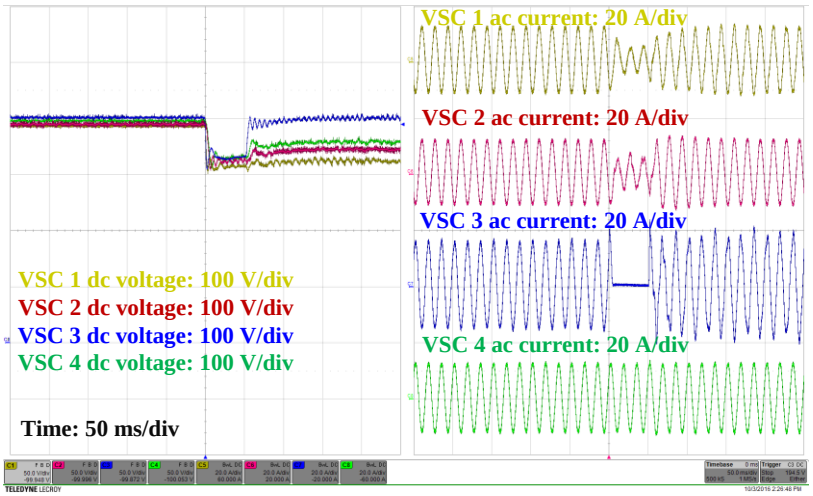


Figure 8-53. Pole-to-pole fault at cable 1 middle point (1 Ω fault resistance, 1.5 ms delay time, VSC 3 power flow from ac to dc).

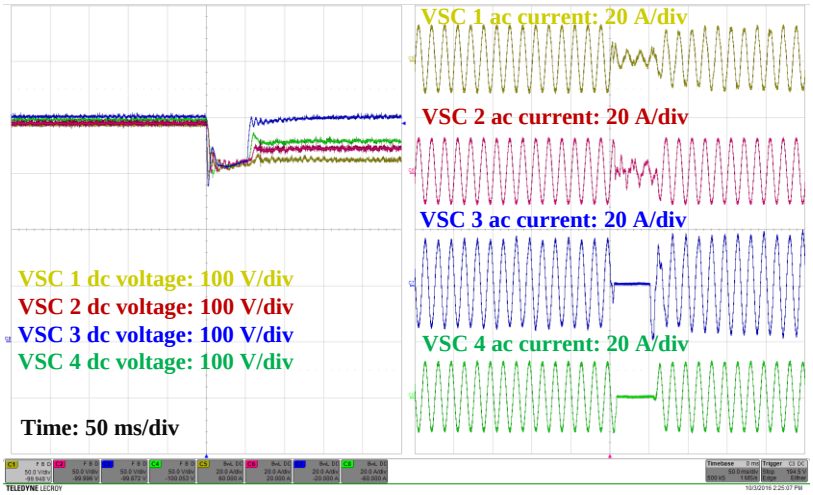


Figure 8-54. Pole-to-pole fault at cable 1 middle point (1 Ω fault resistance, 2 ms delay time, VSC 3 power flow from ac to dc).

another 50 ms delay time, VSC 3 can restart. Again, because of the large dc capacitors and fast dc voltage control, there is no large dc voltage overshoot and a very large ramping rate can be used for fast restart. Figure 8-54 shows the case with 2 ms circuit breaker delay time. VSC 3 and 4 are temporarily blocked, and similarly they can be restarted quickly without large dc overvoltage.

8.5 Conclusions

A dc fault protection strategy for MTDC system with hybrid dc circuit breaker is developed. Compared to the methods using ac circuit breaker or fault tolerant converter, the proposed method with hybrid dc circuit breaker does not need to de-energize the whole dc system, which can be faster. The proposed two-step dc fault detection method provides a framework to combine any fast detection method and selective method, while keeping the advantages of both methods. The HVDC converters may still need to be temporarily blocked, even with the hybrid circuit

breaker and fast detection method. For the fast system recovery after clearing the fault, voltage margin control can be used to simplify the converter restart sequence.

Solid state circuit breakers are developed with the capability to emulate the hybrid dc circuit breaker using a programmable time delay after fault detection, and installed into the MTDC testbed for dc short circuit fault test. The fast detection method using limiting inductor voltage has been verified and the test results shows that it is possible that the dc system maintains operation with a relative fast dc circuit breaker (< 5 ms opening time) for both pole-to-pole and pole-to-ground faults. Even if the converter requires to shut down in some conditions, the system can be recovered quickly.

9 A New DC Fault Tolerant MMC Topology

This chapter proposes a new and potentially lower-cost VSC topology for HVDC transmission with fault current blocking capability. The proposed topology uses a hybrid interrupting circuit with parallel solid-state and mechanical switches in each submodule to allow fast interruption of DC fault current without causing additional conduction losses during normal operation. The operating principle, design methodology and potential benefits and issues of such a converter will be presented.

9.1 Proposed Topology

Inspired by ABB's hybrid dc circuit breaker, a new MMC topology is proposed using a hybrid submodule which adds an ultra-fast mechanical switch on the basis of the clamp-double submodule in [66], as shown in Figure 9-1. The ultra-fast mechanical switch is paralleled with the middle connecting solid-state switch. During normal operation, both the mechanical switch and the paralleled solid-state switch are turned on, but nearly all the current flows through the mechanical switch because of its much lower on-state resistance. Therefore, power loss of the proposed converter is much reduced compared to the MMC based on clamp-double submodule. The power loss should be even comparable to the MMC based on half-bridge submodule, but with fault current blocking capability. When a dc short-circuit fault occurs, the mechanical switch will first commutate the current to the paralleled solid-state switch. With the mechanical switch in open position, the power switch turns off to break the fault current. The opening time of the mechanical switch is critical. A demonstration ultra-fast mechanical switch under a 4 kA/1.5 kV operating condition takes 300 μs to commutate the current to a paralleled solid-state

device [73]. By consulting some industry companies, 2 ms might be a reasonable assumption for mechanical switch opening time, which is still fast enough to deal with a dc short circuit fault.

The proposed converter topology has several benefits compared to the above mentioned converter topologies with fault current blocking capability in subsection 2.4. The extra power loss of the proposed converter over the basic MMC is small (~1%), which is largely reduced compared with that of MMC based on clamp-double submodule and definitely other alternative submodule topologies. The proposed converter also has the advantage of no need for series connection of semiconductor devices compared with the hybrid converters, as well as a reduced power loss. Compared with the method of using a hybrid dc circuit breaker and the traditional MMC in section 8, the proposed converter does not need the bypass thyristors in submodules, and it takes advantage of the large submodule capacitors in MMC, avoiding the arrester banks and additional efforts on voltage sharing issue.

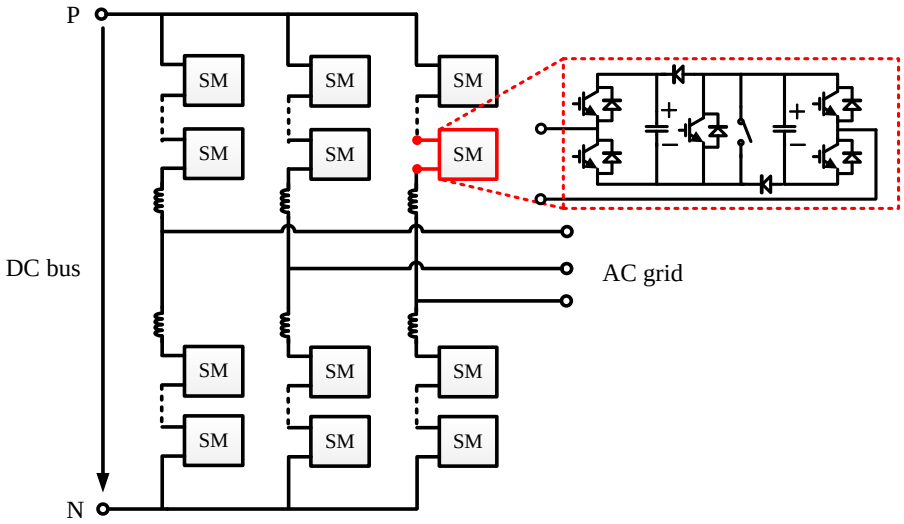


Figure 9-1. Proposed converter topology of MMC with hybrid submodule.

9.2 Ultra-Fast Mechanical Switch

For the proposed topology, the mechanical switch in the submodule must be able to commutate the current very quickly to the paralleled interrupting IGBT to limit the maximum fault current. A survey was conducted of available mechanical switch designs, and the Thomson-drive (TD) actuated switch was chosen because of its ultra-fast switching capability. ABB demonstrated in a prototype hybrid breaker that this technology could commutate 4 kA to a parallel IGCT circuit in 300 μs, with a voltage rating of 1.5 kV.

Meyer *et al.* [73] described the fault current commutation and interruption in four stages. The approximate durations of these stages are described in Table 11. Figure 9-2 shows the theoretical current characteristic during fault current commutation and interruption, and Figure 9-3 shows experimental results for IGCT current (i_{T1}, i_{T2}) and TD switch voltage (u_d) in [73]. The switch voltage includes a two-step arc voltage, first arcing at 12 V then stepping to 24 V. The two sides of the switch contact disconnect independently, due to the orthogonal orientation of the actuator relative to the current direction, and each disconnection results in a momentary 12 V arc. The time between the first and second arc was approximately 10 μs for [73]'s experiment.

Table 11. Stages of fault current interruption for TD switch circuit

Description	Description	Duration
Reaction (T_m)	Mechanical time delay in switch	180 μs
Commutation (T_{com})	Arc and current commutation to IGBT	60 μs
IGBT Conduction (T_{cond})	Build up blocking potential in mechanical switch	70 μs
Falling current (T_f)	Turn off IGBT and interrupt fault current	2 μs

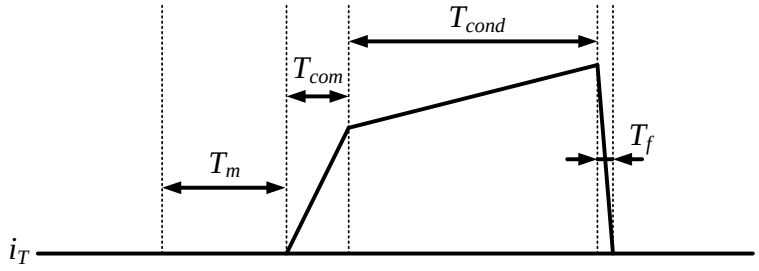


Figure 9-2. Theoretical switching behavior of TD current commutation.

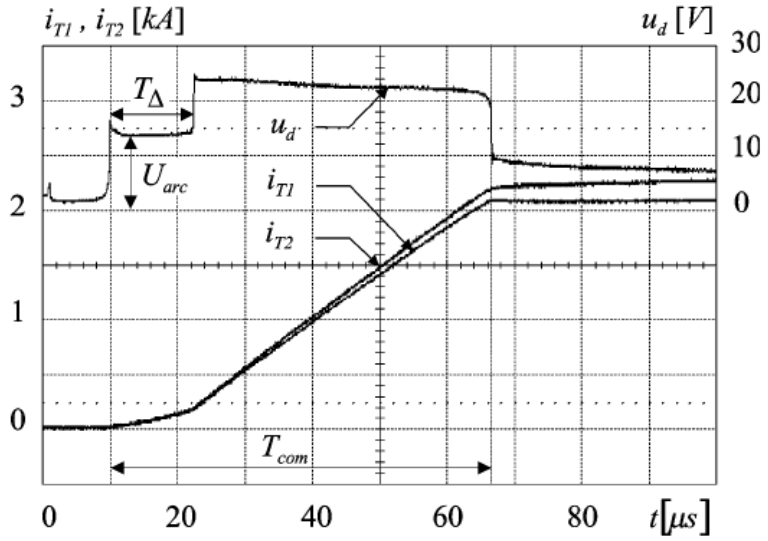


Figure 9-3. Experimental results showing arc voltage and current during TD switch fault current commutation [6].

The most significant factor in the total switching time of the TD switch is the reaction time, which is a physical limitation independent of voltage and current rating. However, the commutation time is a product of the commutation loop inductance and the maximum fault current. In this case, the fault current is lower than the 4 kA rating used by [73], and the commutation loop inductance is primarily composed of the connection inductances between components in the IGBT loop. Polman *et al.* [74] proposed some innovative methods to reduce connection inductances between semiconductor switches, which could allow for further reduction of the total switching time.

The timing and experimental results above were used to develop a Simulink model for the TD mechanical switch, as shown in Figure 9-4. The switch is normally on with series inductance and resistance representing the conducting impedance, until a fault is detected and a signal to open is received. After a mechanical delay of 180 μs, the two-step arc voltage is added in series with the switch impedance. Finally, after the mechanical switch has built up enough insulation potential, the mechanical switch model behaves as an open circuit. The simulation results using an initial commutation loop inductance of 800 nH are shown in Figure 9-5 and Figure 9-6. The results match the experimental results demonstrated in Figure 9-3.

The mechanical switch delay time is a main contribution to the overall opening time, and it is critical for the proposed converter. Even though it has been demonstrated in the prototype in [73], based on the feedback from ABB, 180 μs would be too fast for a reasonable assumption of the state-of-the-art ultra-fast mechanical switch; and it is suggested that 2 ms might be a reasonable assumption for a minimum mechanical switch delay time. Considering other time periods in Table 11 is much smaller, the mechanical switch opening time is assumed to be 2 ms.

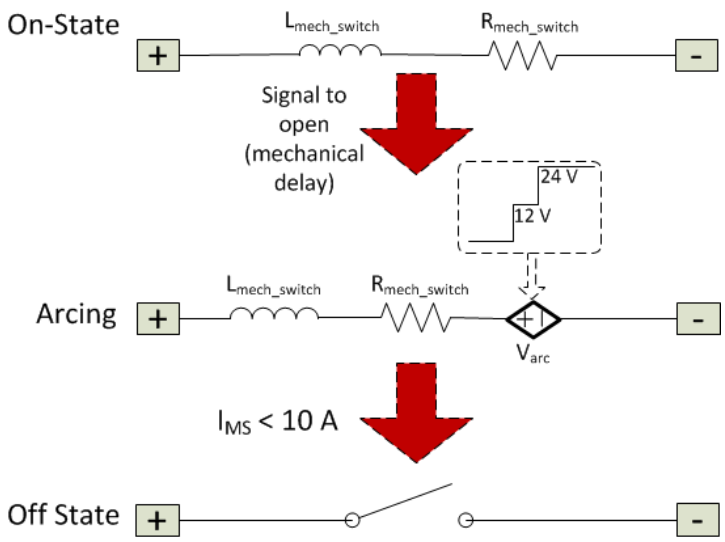


Figure 9-4. Simulink model developed for TD mechanical switch.

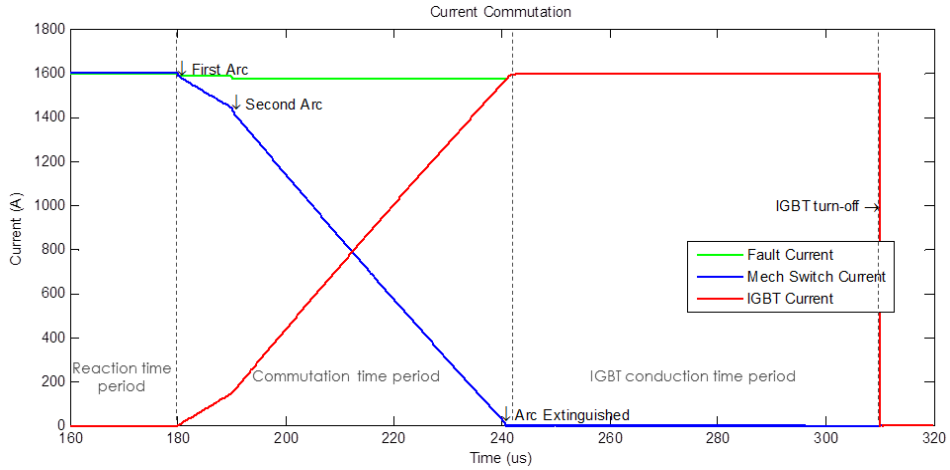


Figure 9-5. TD switch Simulink model current simulation results.

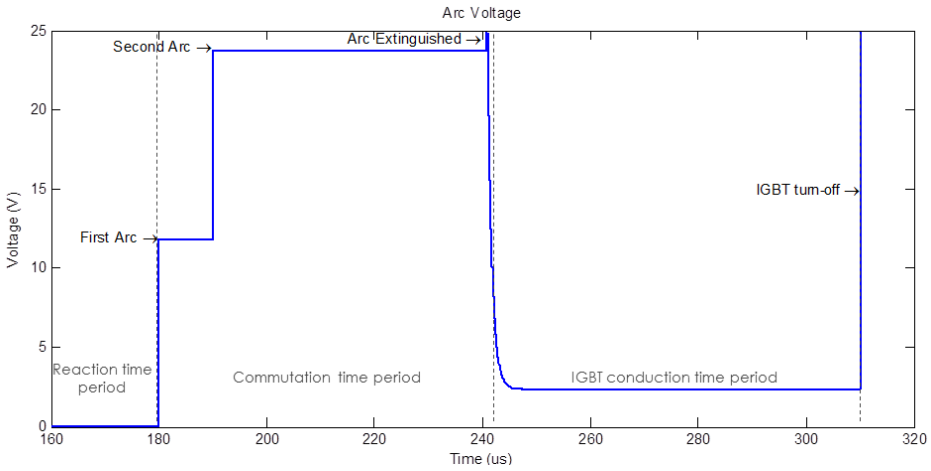


Figure 9-6. TD switch Simulink model voltage simulation results.

9.3 Interrupting Circuit Operation

Figure 9-7 shows the proposed hybrid submodule. Under normal condition, the mechanical switch is always "ON" or closed. The hybrid submodule thus operates the same as two series half-bridge submodule as shown in Figure 9-8.

Under fault conditions, the submodule capacitor voltages are inserted in the current path to limit the fault current by turning off all the IGBTs and the mechanical switch. Figure 9-9 (a) and (b) show the current path for two different cases, depending on current direction through the submodule. For case 1, one submodule capacitor voltage is inserted; for case 2, two submodule capacitor voltages are inserted. It can be seen clearly that the voltage stress of mechanical switch and interrupting IGBT is clamped to the capacitor voltage or diode on-state voltage, ensuring minimized overvoltage for them.

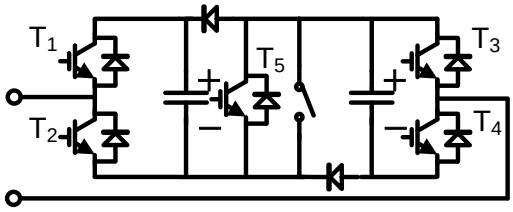


Figure 9-7. Proposed submodule circuit.

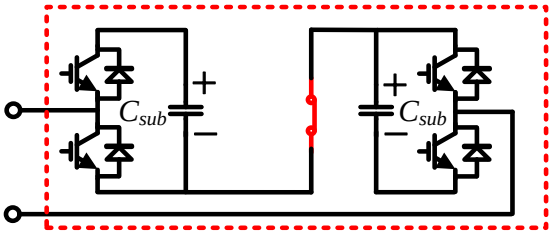
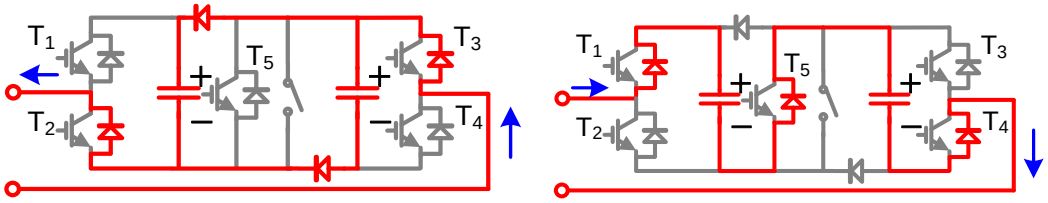


Figure 9-8. Proposed submodule during normal operation.



(a) (b)

Figure 9-9. Proposed submodule current path during fault: (a) Case 1, (b) Case 2.

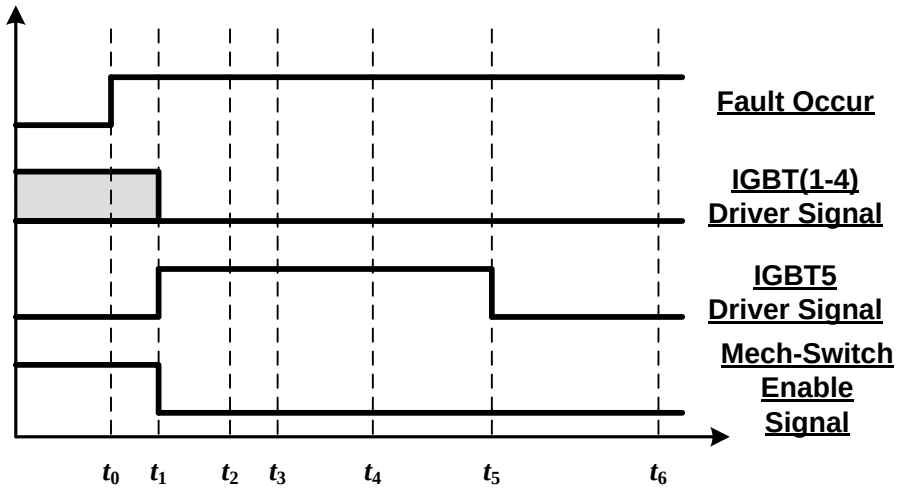


Figure 9-10. Proposed submodule during normal operation.

Figure 9-10 shows the protection sequence after the fault occurs at t_0. Once the fault is detected at t_1, a "turn off" signal will be sent to the mechanical switch and a "turn on" signal for the interrupting IGBT. After a mechanical switch delay, the mechanical switch starts to separate its contacts and the current flowing through the mechanical switch start to commutate to the interrupting IGBT at t_2. At t_4, the current commutation is completed, where t_3 represents the two-step arcing of the mechanical switch. After the current commutation, the mechanical switch continues to separate its contacts in order to gain enough insulation strength. At t_5, the insulation strength of the mechanical switch is achieved and the interrupting IGBT is turned off. The current then commutate to the submodule capacitor branch, and the fault current starts to decrease. At t_6, the fault current is decreased to zero.

9.4 Worst-Case Fault Current

For the design of the proposed converter, the current stresses on the interrupting IGBT and mechanical switch are required. In order to determine the current stresses, the worst case causing maximum fault current should first be identified. There are mainly two types of dc short circuit faults: pole-to-pole fault and pole-to-ground fault. Since the pole-to-pole fault is more severe than the pole-to-ground fault, only the dc pole-to-pole fault is investigated.

Fault analysis is conducted to identify the worst case condition when the maximum fault arm current occurs. Rectifier operation is considered as the fault current should be larger than that of inverter operation. The initial direction of the arm currents also influences the fault analysis. Normally, higher initial current would lead to higher fault current eventually; the maximum arm current (e.g. upper arm current) occurs when the lower arm current has an opposite direction. Thus only the case with arm currents for the upper and lower arms having opposite directions is considered. Figure 9-11 shows the equivalent circuits for each stage after the fault occurs and the converter is divided into dc and ac circuits. Figure 9-12 shows the theoretical fault current waveforms.

Stage 1: (t_0, t_1)

This stage starts at the time t_0 when the fault occurs and ends at the time t_1 when the bridge IGBTs are turned off. The duration of this stage is mainly determined by the fault detection time, pulse delay time and IGBT turn off time, usually in the range of several tens of microseconds.

The arm voltages can be assumed unchanged for such a short time. Thus, the phase-leg voltage ($\approx v_{dc}$) all applies on the arm inductors, and the circulating current i_{cir} including the dc component increases rapidly. The ac terminal voltages can be obtained as

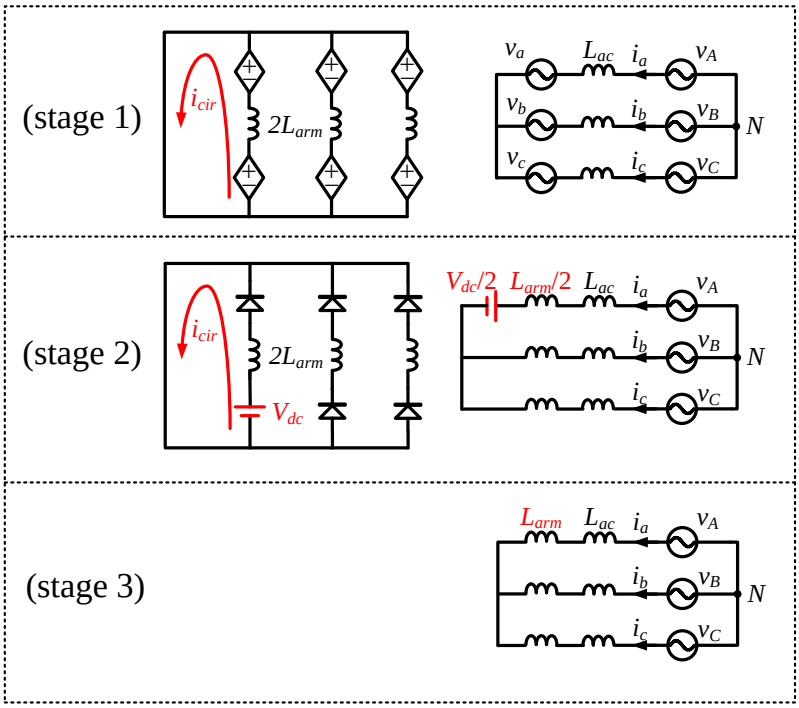


Figure 9-11. Equivalent circuit after fault occurs.

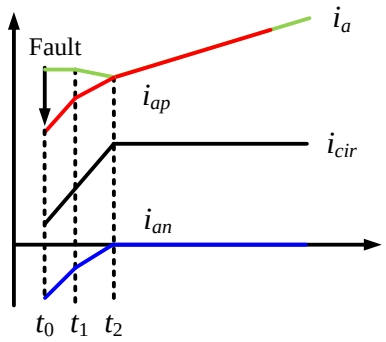


Figure 9-12. Theoretical fault current waveforms.

$$v_{ac} = \frac{v_{dc}}{2} - v_{up} = -\frac{v_{dc}}{2} + v_{low}. \tag{9-1}$$

Since the time duration is short, compared to the fundamental period, the ac terminal voltages and ac currents can be regarded as constant during this stage. The arm currents can thus be approximated as

$$i_{up}(t) = i_{up}(t_0) + \frac{v_{dc}}{2L_{arm}}(t - t_0) \tag{9-2}$$

$$i_{low}(t) = i_{low}(t_0) + \frac{v_{dc}}{2L_{arm}}(t - t_0). \tag{9-3}$$

During this stage, the arm current rise is because the discharge of inserted submodule capacitors.

Stage 2: (t_1, t_2)

At t_1, IGBTs are blocked and fault currents flow through diodes. If both arm currents are positive, this phase is equivalently shorted and the circulating current is freewheeling. If one arm current is negative, the capacitor voltages are inserted in the circuit which decreases the current to zero, and the total capacitor voltages approximately equal to v_{dc}. i_{cir} keeps increasing until the arm current decreases to zero. Also, there is an equivalent voltage inserted into the ac circuit as shown in Figure 9-11.

As rectifier operation, it can be assumed that only one arm current is negative (lower arm of *a* phase is considered). For this arm, the capacitor voltages are inserted in the circuit which decreases the current to zero, and the total capacitor voltages approximately equal to v_{dc}.

Both the dc and ac currents change in this stage. For dc side, the current rising rate is the same as that in stage 1. For ac side, the current cannot be considered unchanged. It should be

noted that only one phase is considered to have the additional inserted voltage, which because usually there is only one phase has negative arm current as rectifier operation. The ac side current rising rate of this phase should be much smaller compared to the dc side current rising rate. So the arm currents can still be approximated by (9-2) and (9-3). The minor difference between the current rising rates for stages 1 and 2 in Figure 9-12 is to reflect the difference between these two stages.

During stage 2, the lower arm current is decreasing and the upper arm current is increasing. At t_2 the lower arm current is decreased to zero. So the arm currents at t_2 can be expressed as

$$i_{up}(t_2) = i_{up}(t_0) - i_{low}(t_0) = i_{ac}(t_0) \tag{9-4}$$

$$i_{low}(t_2) = 0. \tag{9-5}$$

Stage 3: (t_2,–)

At t_2, the lower arm current decreases to zero. Since then, only diodes in the upper arm are conducting. Its current should be equal to the ac side current. The fault current in this stage is limited by both the ac inductors and arm inductors. The fault current will keep increasing until the interrupting circuit acts and the submodule capacitors voltages are effectively inserted in the circuit. Thus the maximum fault current is directly related to the fault interrupting time. The upper arm current during this stage can be derived as:

$$i_{up}(t) = i_{ac}(t_0) + \frac{v_{ac}}{L_{arm} + L_{ac}}(t - t_2) \tag{9-6}$$

where v_{ac} represents the ac voltage (one of v_A, v_B and v_C). For a short time, it can be considered as a constant value. Supposing that the interrupting circuit acts at t_3, the maximum fault current is

$$i_{fault\_max} = i_{ac}(t_0) + \frac{\bar{v}_{ac}}{L_{arm} + L_{ac}}(T_{inte} - \Delta T_2). \quad (9\text{-}7)$$

where T_{inte} is the total converter interrupting time, defined as $t_3 - t_0$, ΔT_2 is the total time of stage 1 and 2, defined as $t_2 - t_0$ and $\bar{v}_{ac}$ is the average ac voltage during stage 3. T_{inte} is determined by the mechanical switch, which should be considered fixed, while ΔT_2 is determined by the initial arm current, which can be expressed as

$$\Delta T_2 = -i_{low}(t_0)\frac{2L_{arm}}{v_{dc}}. \quad (9\text{-}8)$$

Inserting (9-8) into (9-7) gives

$$i_{fault\_max} = i_{up}(t_0) - \left(1 - \frac{L_{arm}}{L_{arm} + L_{ac}}\frac{2\bar{v}_{ac}}{v_{dc}}\right) i_{low}(t_0) + \frac{\bar{v}_{ac}}{L_{arm} + L_{ac}} T_{inte}. \quad (9\text{-}9)$$

Usually, the modulation index is less than 1, which leads to

$$1 - \frac{L_{arm}}{L_{arm} + L_{ac}}\frac{2\bar{v}_{ac}}{v_{dc}} > 0. \quad (9\text{-}10)$$

Equation (9-9) shows that the maximum fault current is related to the initial arm currents and the ac voltage charging. The worst case occurs at 1) the peak ac current, i.e. largest $i_{up}(t_0)$ and smallest $i_{low}(t_0)$; and 2) the maximum ac voltage, i.e. largest $\bar{v}_{ac}$. Since $\bar{v}_{ac}$ is the average voltage, the maximum $\bar{v}_{ac}$ is related to the time period of stage 3 (t_2, t_3). This time period is mainly determined by the mechanical switch delay time. For a short delay time case, the maximum $\bar{v}_{ac}$ simple occurs at the peak of AC side voltage; for a longer delay time (several milliseconds) case, the maximum $\bar{v}_{ac}$ occurs when the peak of ac voltage is at the middle of this period.

Table 12. System parameters of the simulation platform and INELFE project

Description	INELFE Project	Simulation Platform
Transmission Power (MW)	1000	10
DC Voltage (kV)	640	6.4
AC Voltage (kV)	333	3.33
Submodule Number per Arm	400	4
Submodule Capacitance (mF)	10	10
Arm Inductance (mH)	50	0.5
Equivalent Grid Transformer Inductance (mH)	60	0.6

9.5 Simulation Verification

A simulation platform is built in MATLAB to verify the above analysis. It is a reduced system of Siemens INELFE project [75], with the scaling factor of 1/100. Table 12 shows the system parameters of the simulation platform and INELFE project. The impedances of the arm inductor and transformer leakage inductor are kept the same in per unit.

Figure 9-13 shows the current waveforms of the proposed converter during a dc pole-to-pole fault for a short mechanical switch delay time (180 μs). The t_0-t_6 are corresponding to the time instants in Figure 9-10. It shows that the proposed converter has the capability to block fault current. Zoomed in waveforms of mechanical switch current and IGBT current are shown in Figure 9-14. It matches the description in subsection 9.3. Figure 9-15 shows the simulation result for a longer mechanical switch delay time (5 ms). Apparently, the fault current is larger than the case with shorter delay time.

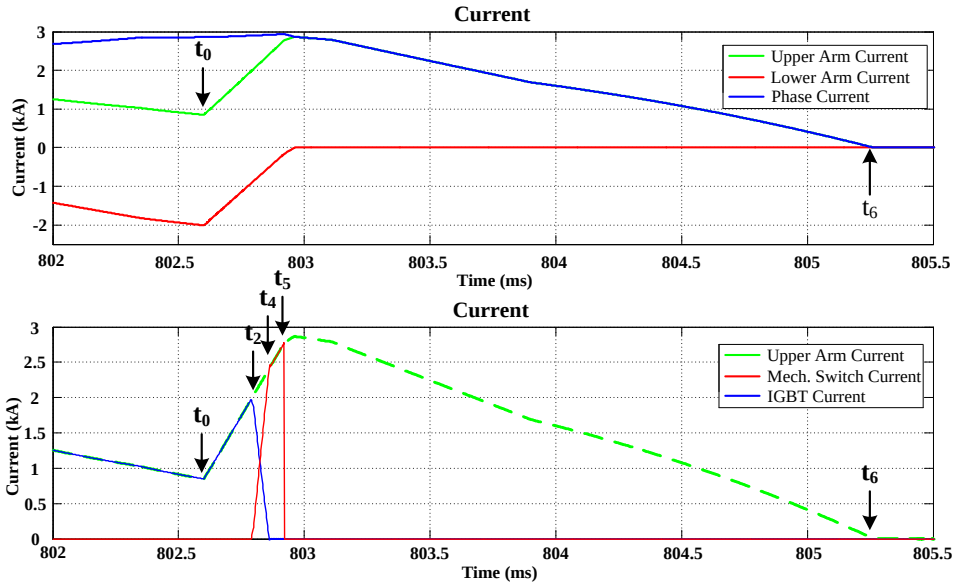


Figure 9-13. Current waveforms of the proposed converter during a dc pole-to-pole fault.

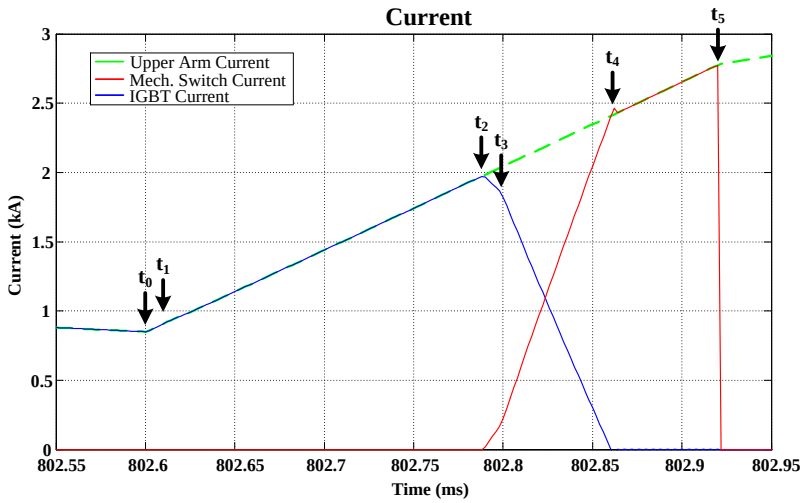


Figure 9-14. Zoomed in Current waveforms of Figure 9-13.

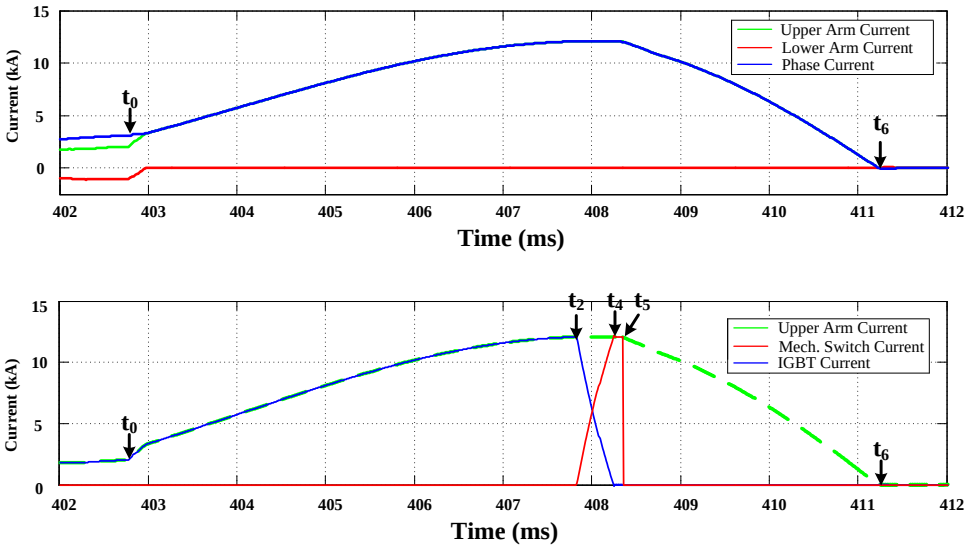


Figure 9-15. Current waveforms of the proposed converter during a dc pole-to-pole fault for a longer mechanical switch delay time.

9.6 Topology Comparison with Clamp-Double Submodule

As it is mentioned previously, the proposed hybrid submodule is based on the clamp-double submodule. Figure 9-16 shows the circuit diagram of the clamp-double submodule. The difference between the clamp-double submodule and the proposed hybrid submodule is the mechanical switch. The MMC with clamp-double submodule also enables the fault current blocking capability, and even with a potential shorter fault current interrupting time. On the other hand, the proposed hybrid submodule has the advantage of lower conduction loss because of the mechanical switch. Thus it is meaningful to compare these two submodule topologies.

9.6.1 Fault Clearance Performance Comparison

For clamp-double submodule, the fault interrupting time is shorter than the proposed converter as it does not have the mechanical switch. Figure 9-17 shows the simulation results of a dc pole-to-pole fault for MMC with clamp-double submodule. It is shown that the ac current decreases immediately after the interrupting IGBT is turned off. Figure 9-18 shows the ac current waveforms for both topologies.

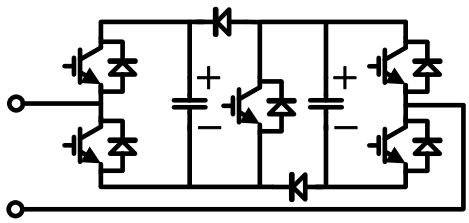


Figure 9-16. Circuit diagram of the clamp-double submodule.

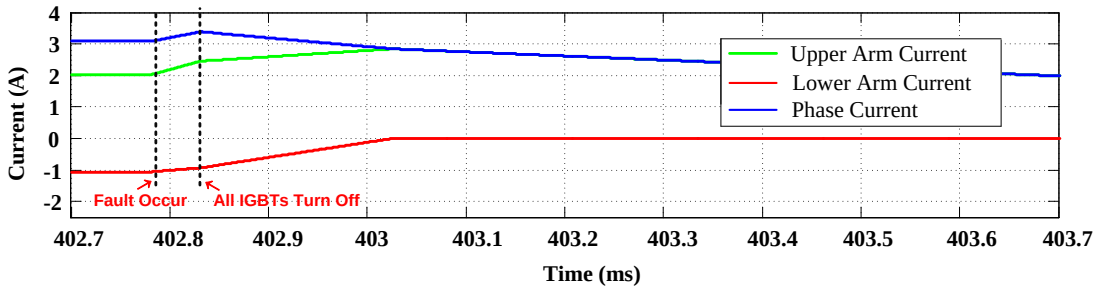


Figure 9-17. Fault interruption waveform for MMC with clamp-double submodule.

Since the clamp-double topology can interrupt the fault faster than the proposed converter, the maximum fault current should also be smaller than the proposed converter. As shown in Figure 9-19, the maximum fault current for clamp-double submodule topology is 2.3 kA; it is much lower compared to the 5.8 kA in the proposed converter. However, this does not necessarily indicate that the proposed converter requires much larger interrupting IGBT. As the interrupting IGBT in the proposed converter is designed based on the saturation current limit, a 1.5 kA IGBT module can be used in the proposed converter. For the clamp-double topology, the arm current continuously flows through the interrupting IGBT. So the interrupting IGBT is designed based on the SOA.

9.6.2 Loss Comparison

The converter loss mainly includes power semiconductor loss, inductor loss and mechanical switch loss. The mechanical switch loss is relatively small, which is neglected in this analysis. The half-bridge IGBT module should be first selected based on the normal operating condition. For the proposed converter, according to the simulation result, the RMS value of the arm current is 1 kA. The Infineon FZ1500R33HL3 IGBT module is selected considering a 50% current

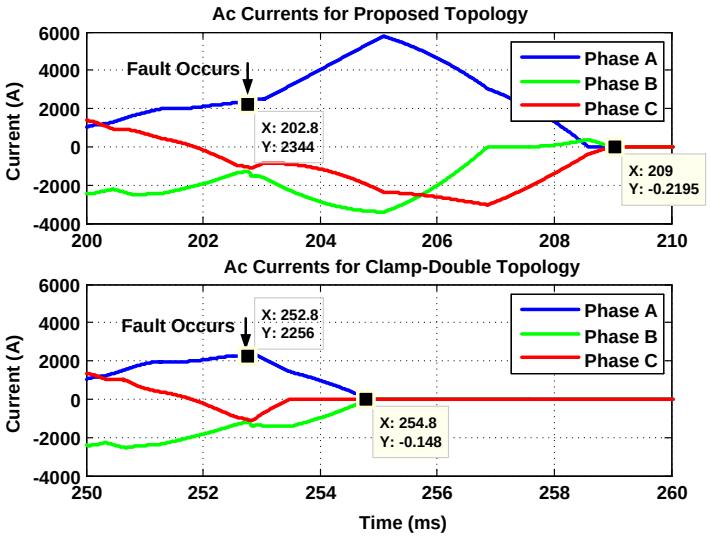


Figure 9-18. AC current waveforms comparison during pole-to-pole fault.

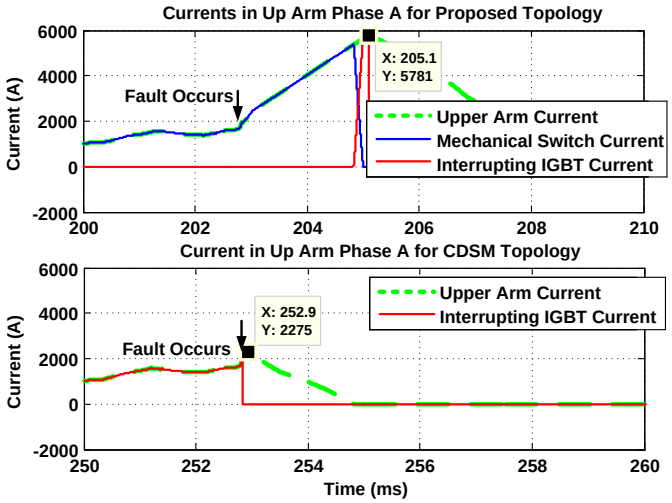


Figure 9-19. Interrupting IGBT current waveforms comparison during pole-to-pole fault.

margin. The interrupting IGBT is also chosen as the Infineon FZ1500R33HL3 IGBT module. The maximum fault current capability of this IGBT is 5.8 kA. It should be noted that the fault current capability for the interrupting IGBT is limited by the device saturation current rather than the safe operation area (SOA) as is typical in voltage source converter applications [12]. The arm inductor is then designed to limit the fault current within 5.8 kA. Figure 9-19 is the waveform of the worst case. The maximum fault current is 5.78 kA, which is in the safe range. The clamp-double topology is similar to the proposed converter under normal operating condition. So the half-bridge IGBT module, interrupting IGBT and arm inductor are chosen the same.

The power loss is first calculated in the reduced system, and then scaled to the high voltage system. Table 13 and Figure 9-20 show the comparison of the overall power loss of the proposed converter and clamp-double topology. The proposed converter has an efficiency of 99.4% compared to the 99.18% for the clamp-double topology. It should be noted that the transformer loss is not considered. It can be found that the clamp-double topology has a 37% higher power loss due to the interrupting IGBT compared to the proposed converter. Other operating conditions are also evaluated, and similar results are obtained.

Table 13. Converter Loss Comparison

Switch Frequency = 150 Hz	**Conduction Loss (kW)**	**Switching Loss (kW)**	**Inductors Loss (kW)**	**Total Loss (kW)**	**Efficiency**
Proposed Converter	4184.6	1615.0	263.8	6063.4	99.40%
Clamp-Double Topology	6632.8	1438.0	228.6	8299.4	99.18%

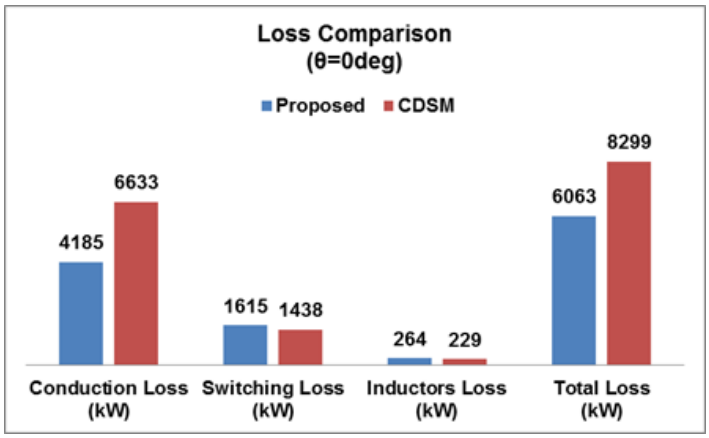


Figure 9-20. Power Loss Comparison.

9.6.3 Cost Comparison

A cost comparison of the converter main components is conducted and the results are listed in Table 14. Compared to the clamp-double topology, the proposed converter has the same power semiconductors and arm inductor. The submodule capacitor voltage ratings are a little different, while if considering some margin in the design the submodule capacitor could also be the same for these two converters.

The benefit of the proposed converter is the reduced power loss and as a result the reduced requirement on cooling system. The additional costs of the proposed converter include the dc inductor and mechanical switch. A detailed cost comparison is difficult without specific cost for all components, which is usually confidential from the manufacture. However, we can conclude that if the mechanical switching cost in the proposed converter plus the extra inductor cost, is lower than the cost saving from the reduced loss and cooling, the proposed converter will have a lower cost compared to the clamp-double topology. Otherwise, the proposed converter will have a higher cost.

Table 14. Converter Main Component Comparison

Component	Proposed Topology	Clamp-Double	Component	Proposed Topology	Clamp-Double
Bridge IGBT	3300V,1500A	3300V,1500A	**Arm Inductor**	0.15 p.u.	0.15 p.u.
Clamp Diode	Same	Same	**DC Inductor**	0.24 p.u.	No
Interrupting IGBT	3300V,1500A	3300V,1500A	**Submodule Capacitor**	10mF, 2100V	10mF, 1800V
Mech-switch	One per SM	No	**Cooling System**	1 p.u.	1.37 p.u.

9.7 Conclusions

The dc fault current blocking capability of the proposed converter with hybrid submodule was verified through theoretical analysis and simulation. The mechanical switch delay time was found to be critical for the fault clearance performance and converter current and voltage stresses. In order to find the maximum fault current, detailed fault analysis was conducted to determine the worst case fault condition. It was found the maximum fault current occurs at the time of peak ac voltage and highest arm current. Loss calculation verified that the proposed converter can reduce the power loss by 1/3 compared to the similar clamp-double topology. Further cost comparison with the clamp-double topology shows that the cost saving from higher efficiency should account for the mechanical switch and extra inductor cost in order to make the proposed converter lower cost than the clamp-double topology.

10 Conclusion and Future Work

This chapter summarizes the work has been done and proposes the work which will be done to complete the dissertation.

10.1 Conclusion

The MMC based MTDC system has been evaluated in this thesis. Some key issues involving MMC design, MTDC control and protection have been explored. The conclusions can be drawn as follows.

- Switching frequency circulating current is the limit for arm inductance design of MMC, when the circulating current suppression control is implemented. The analytical relationship between the switching frequency circulating current and arm inductance is derived. The experimental results of a down-scaled prototype verify both the existence of the switching frequency circulating current and the analytical relationship.
- The unbalanced capacitor voltage, which is related to the voltage-balancing control or switching frequency, contributes a large portion to the total submodule capacitor voltage ripple in MMC. The relationship between the unbalanced capacitor voltage and converter switching frequency, for a selected voltage-balancing control method – modified sorting method, is established. This derived analytical expression can assist for the submodule capacitance design.
- Circulating current suppression control in MMC reduces the converter maximum modulation index. The reduction of the maximum modulation index is related to the submodule capacitance. If the capacitance is designed based on a 10% voltage ripple

requirement, the maximum modulation index could be reduced by 5%, or 8% for the case with third harmonic component injection. This reduction is not negligible and should be considered for the nominal modulation index selection in the converter design.

- A 4-terminal down-scaled HVDC testbed is developed, and is capable to emulate several most typical operation scenarios, including system startup, power variation and station outage. Two unique scenarios, station online re-commission and mode transition, are also demonstrated, with proposed methods.
- A dc line current control is proposed and verified in the 4-terminal HVDC testbed. This control mainly has two key benefits. First, it facilitates the use of a "low-cost" HVDC disconnect to online trip a dc transmission line, instead of the "high-cost" HVDC circuit breaker. Second, an automatic dc line current limiting function is further developed based on this control, which will automatically switch to current control once the transmission line is overloaded.
- A dc fault protection strategy for MTDC system with hybrid dc circuit breaker is developed. A two-step dc fault detection method is proposed, which provides a framework to combine any fast detection method and selective method, while keeping the advantages of both methods. The HVDC converters may still need to be temporarily blocked, even with the hybrid circuit breaker and fast detection method. For the fast system recovery after clearing the fault, voltage margin control is proposed to simplify the converter restart sequence.
- A novel MMC topology with dc fault current blocking capability is proposed. The proposed hybrid submodule parallels a mechanical switch to the interrupting IGBT in the clamp-double topology. By using the mechanical switch, the power loss of the

proposed converter can be close to the half-bridge MMC. A cost comparison with the clamp-double topology shows that the mechanical switch needs to account for less than 14.9% of the total converter (half-bridge MMC) cost in order to make the proposed converter lower cost than the clamp-double topology.

10.2 Recommended Future Work

To further extend the work in this dissertation, the following future works are recommends:

(1) Submodule capacitance reduction method

Even though in this dissertation, the submodule capacitance design method considering the unbalanced voltage is proposed, which helps to optimize the capacitance selection with minimum overdesign margin. However, the submodule capacitor is still a large contribution to the overall MMC cost and size. It is also the main obstacle for MMC to be used in some medium voltage applications. Therefore, if the submodule capacitance requirement can be reduced, the MMC will become much more promising not limited to HVDC but also some medium voltage applications.

To reduce the submodule capacitance requirement, there could be two methods – reshape the current through the capacitor or change the submodule topology. Some methods by injecting circulating current has been discussed, but the capacitance reduction is limited and it causes higher power loss. For the new submodule topology, there can be many possibilities.

(2) MMC loss optimization and thermal design

This dissertation covers the design of the main passive components; however, thermal management is also a key issue in MMC. A known issue associated with the half-bridge MMC is the power loss imbalance between the two power devices in one

module. For industry application, the half-bridge power module is typically used which causes one device to always operate at a lower temperature than the other one. This means the heatsinks for the power devices are actually overdesigned. Furthermore, for the full-bridge MMC, the higher power loss is one of the main disadvantages.

To alleviate the power loss imbalance of the two power devices in the half-bridge submodule, a potential solution is to inject certain circulating current to reshape the current distribution on the two devices. This method may slightly increase the converter total power loss, but it has the possibility to balance the power loss on devices and reduce the heatsink. For the full-bridge MMC, it is possible to utilize the additional switching states of full-bridge submodule to better balance the power losses.

(3) DC power flow controller

Through the process of developing the MTDC testbed, it is found that a lack of the existing control system is the power flow control. Even though the proposed line current control in this dissertation can conditionally solve this problem, but dc power flow controller is still needed to fully control the power flow in different lines. Especially when the more complicated dc grid is developed or combining several point-to-point HVDC systems or small dc grids to form to large dc grid, the power flow controller will become important.

(4) DC fault protection with full-bridge MMC

For the dc fault protection, the hybrid dc circuit breaker solution is considered in this dissertation. But fault tolerant converter, especially full-bridge MMC is another promising solution and is seriously considered in industry. But it still lacks a detailed study on the overall protection strategy, including the detection, and system recovery. It

also may be interest to evaluate the system with both full-bridge MMC and hybrid dc circuit breaker.

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