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Development and Analysis of Non-Delay-Line Constant-Fraction Discriminator Timing Circuits, Including a Fully-Monolithic CMOS Implementation

David Martin Binkley
University of Tennessee, Knoxville

To the Graduate Council:

I am submitting herewith a dissertation written by David Martin Binkley entitled "Development and Analysis of Non-Delay-Line Constant-Fraction Discriminator Timing Circuits, Including a Fully-Monolithic CMOS Implementation." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

James M. Rochelle, Major Professor

We have read this dissertation and recommend its acceptance:

William Bugg, Paul Crilly, Vaugh Blalock, Donald Bouldin

Accepted for the Council:

Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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DEVELOPMENT AND ANALYSIS OF NON-DELAY-LINE CONSTANT-FRACTION DISCRIMINATOR TIMING CIRCUITS, INCLUDING A FULLY-MONOLITHIC CMOS IMPLEMENTATION

A Dissertation
Presented for the
Doctor of Philosophy
Degree
The University of Tennessee, Knoxville

David Martin Binkley
December 1992

DEDICATION

This dissertation is dedicated to the memory of my mother, Carol Louise Dexter Binkley, who passed away in March 1991 during the early part of this research. Mother's enthusiasm, love of life, and courage set an example for all of us to follow. Her death at only fifty-six years of age is the greatest loss experienced by me, my father, Jerry W. Binkley, my sisters, Janet, Elaine, and Linda Binkley, mother's parents, William M. and Lucille W. Dexter, mother's brother and sisters, and many other relatives and friends. I hope this research will further encourage biochemical medical imaging with Positron Emission Tomography (PET) and contribute to better cancer detection, treatment, and the development of cures.

ACKNOWLEDGMENTS

This research was only possible with the encouragement and support of many people, for whom I am very grateful. I start by thanking my wife, Jacqueline, for all her support during a time when our time together was limited greatly. Her support during this research once again reminded me that the best decision I have made in life was to request our marriage. Additionally, I thank my father, Jerry White Binkley, sisters, Janet, Elaine, and Linda Binkley, grandparents, William M. and Lucille W. Dexter, and Robert T. Binkley, and other members of the Binkley and Dexter families for their support during this research. I am especially grateful for my father's total commitment to mother during her lengthy illness.

It is a great opportunity to be employed at CTI PET Systems, Inc., which has the mission of making PET a widely-available, clinical, medical-imaging modality. The potential of improving the quality of human life and, indeed, saving human life through medical research and clinical practice is enormous using PET biochemical imaging. The research reported here, in fact, was funded in part by a grant (grant number 2 R44 CA49405-02A1) from the National Cancer Institute.

Many individuals at CTI PET Systems, Inc. were supportive of this research. While few senior managers would have permitted a small company (less than 250 employees) to venture into the development of sophisticated, custom, high-speed, analog CMOS integrated circuits, Ron Nutt permitted us to launch into such a development. Ron's entrepreneurial spirit and vision has permitted him to lead the research and development activities of an organization which leads the world in PET development. Mike Casey served as a primary sounding board for this research, and his extensive knowledge and feel for radiation-detection statistics was invaluable. Additionally, Clif Moyers and Wilfried Loeffler offered continuing support for this research. Mike Paulus assisted with integrated-circuit layout and was very helpful in areas of CMOS processing. Brian Swann and Steve Hudson assisted with integrated-circuit layout, developed computer programs that interchanged data between commercial SPICE programs and circuit-optimization programs which I wrote, and prepared many figures. Brian Williams also helped with integrated-circuit layout and made many difficult laboratory measurements of the prototype monolithic CMOS constant-fraction discriminator circuit developed in this work. Mark Long built a number of complex test circuits, and as typical of Mark's work, these test circuits were always fully operational at the start of prototype testing. Finally, Larry Byars provided C programming

advice, and Jonathan Frey provided technical-writing advice through proof reading of this dissertation.

A dissertation committee of world-class researchers helped to guide and review this research. Jim Rochelle served as the committee head, and I enjoyed frequent discussions with him on analog CMOS design topics. Jim is an enormously knowledgeable, creative, and thorough researcher and I consider it rare opportunity to study under such an individual. Don Bouldin, active in VLSI design research, Vaugh Blalock, active in nuclear instrumentation and low-noise electronics research, William Bugg, active in high-energy physics experimentation research, and Paul Crilly, active in signal reconstruction research, complimented Jim in their guidance and review of this research.

Figure 5-2 (page 227) is reprinted from: Binkley, D. M., M. L. Simpson, and J. M. Rochelle, "A Monolithic, 2 μm CMOS Constant-Fraction Discriminator for Moderate Time Resolution Systems," *IEEE Transactions on Nuclear Science*, vol. 38, no. 6, December 1991, p. 1757, with permission of the Institute of Electrical and Electronic Engineers.

ABSTRACT

A constant-fraction discriminator (CFD) is a time pick-off circuit providing time derivation that is insensitive to input-signal amplitude and, in some cases, input-signal rise time. CFD time pick-off circuits are useful in Positron Emission Tomography (PET) systems where Bismuth Germanate (BGO)/photomultiplier scintillation detectors detect coincident, 511-keV annihilation gamma rays.

Time walk and noise-induced timing jitter in time pick-off circuits are discussed along with optimal and sub-optimal timing filters designed to minimize timing jitter. Additionally, the effects of scintillation-detector statistics on timing performance are discussed, and Monte Carlo analysis is developed to provide estimated timing and energy spectra for selected detector and time pick-off circuit configurations. The traditional delay-line CFD is then described with a discussion of deterministic (non statistical) performance and statistical Monte Carlo timing performance. A new class of non-delay-line CFD circuits utilizing lowpass- and/or allpass-filter delay-line approximations is then presented. The timing performance of these non-delay-line CFD circuits is shown to be comparable to traditional delay-line CFD circuits.

Following the development and analysis of non-delay-line CFD circuits, a fully-monolithic, non-delay-line CFD circuit is presented which was fabricated in a standard digital, 2-μ, double-metal, double-poly, n-well CMOS process. The CMOS circuits developed include a low time walk comparator having a time walk of approximately 175 ps for input signals with amplitudes between 10-mV to 2000-mV and a rise time (10 - 90%) of 10 ns. Additionally, a fifth-order, continuous-time filter having a bandwidth of over 100 MHz was developed to provide CFD signal shaping without a delay line. The measured timing resolution (3.26 ns FWHM, 6.50 ns FWTM) of the fully-monolithic, CMOS CFD is comparable to measured resolution (3.30 ns FWHM, 6.40 ns FWTM) of a commercial, discrete, bipolar CFD containing an external delay line. Each CFD was tested with a PET BGO/photomultiplier scintillation detector and a preamplifier having a 10-ns (10 - 90%) rise-time. The development of a fully-monolithic, CMOS CFD circuit, believed to be the first such reported development, is significant for PET and other systems that employ many front-end CFD time pick-off circuits.

PREFACE

The enormous complexity of PET-tomograph front-end electronics prompted the research and development staff of CTI PET Systems, Inc. to find a way to integrate this electronics into semicustom or custom integrated circuits. Such integration was vital to significantly reduce the cost, size, power consumption, and complexity of the front-end electronics, which is one of the requirements for making PET a widely-available, clinical, medical-imaging modality.

The idea to integrate PET front-end electronics into CMOS circuits originated while I was attending a course in analog CMOS design taught by Jim Rochelle at the University of Tennessee in Knoxville. We had been investigating the use of bipolar integration at CTI PET Systems, Inc., but the cost and power required using this technology would not permit us to reach the aforementioned objectives of significantly reducing the cost, size, power consumption, and complexity of PET front-end electronics.

As a result of the analog CMOS course, we began researching the feasibility at CTI PET Systems, Inc. of fabricating monolithic, high-speed (50 - 200 MHz bandwidth), analog CMOS circuits. Such circuits had previously seemed unfeasible given the low-speed (1 MHz bandwidth) of commercial CMOS analog integrated-circuit and standard-cell offerings. Following this feasibility research, CTI PET Systems, Inc., initiated the research and development of custom, high-speed, analog and digital CMOS circuits to replace the existing PET front-end circuitry consisting of high-speed bipolar operational amplifiers, CMOS digital-to-analog converters, and other circuits. A $500,000 Small Business Innovative Research grant (grant number 2 R44 CA49405-02A1) was then successfully obtained from the National Cancer Institute to help fund the research and development. The fully-monolithic, CMOS constant-fraction discriminator described in this work is one part of the CMOS, integrated-circuit, front-end electronic development project.

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LIST OF ABBREVIATIONS

ADC	analog-to-digital converter
ARC	amplitude rise-time compensated
BaF_2	Barium Fluoride
CAT	computerized axial tomography
CFD	constant-fraction discriminator
CMOS	complementary metal-oxide semiconductor
CMR	common-mode rejection
DAC	digital-to-analog converter
ECL	emitter-coupled logic
FWHM	full width half maximum
FWTM	full width tenth maximum
GaAs	Gallium Arsenide
MCA	multichannel analyzer
MOSFET	metal-oxide semiconductor field-effect transistor
MRI	magnetic resonance imaging
NIM	nuclear instrumentation module
OP AMP	operational amplifier
OTA	operational transconductance amplifier
PET	positron emission tomography
PMT	photomultiplier tube
PPM	parts per million
PSR	power-supply rejection
SRT	slow rise-time reject
TAC	time-to-amplitude converter
TDC	time-to-digital converter
TOF	time of flight

1. INTRODUCTION

Time-Measurement Systems

Operation

The measurement of time between physical events is of great importance in many experimental and applied systems. Such time measurements can be obtained using a time-spectroscopy system where the time differences between pairs of events are histogrammed. A block diagram of a time-of-flight time-spectroscopy system is shown in Figure 1-1[1]. The time-spectroscopy system shown consists of two detectors, each detecting a physical occurrence (light, nuclear radiation, etc.) from an event located somewhere between the detectors. Each detector is connected to a time pick-off device that provides a timing signal related in time to a detected event. Finally, a time-interval measuring system provides the measurement of time differences between the detector timing signals, one detector timing signal being designated as a *start* signal and the other timing signal designated as a *stop* signal. Typical time-interval measuring systems include time-to-amplitude converters (TACs) and time-to-digital converters (TDCs). Time-interval measurements from a time-spectroscopy system can be histogrammed using a multi-channel analyzer (MCA) or other histogramming device to provide a timing-coincidence spectrum like the one shown in Figure 1-2.

In an ideal time-of-flight time-spectroscopy system, all time-interval measurements are the same for physical events having a fixed location between the two detectors. Such a time-spectroscopy system precisely locates the events spatially using the difference in propagation time between detected events at the two detectors. In actual time-spectroscopy systems, time-measurement uncertainty results from detector statistical and electronic noise, time pick-off circuit errors and noise, and time-interval measurement system errors and noise. Actual time-spectroscopy system timing resolution (in seconds) is specified using the quality factors full-width-half-maximum (FWHM) and full-width-tenth-maximum (FWTM) as shown in the timing-coincidence spectrum of Figure 1-2.

The Constant-Fraction Discriminator As a Time Pick-Off Circuit

The ideal time pick-off circuit develops a timing signal having a fixed time delay from the detector signal. Such a circuit introduces only a fixed timing error and does not degrade

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[1]Due to the large number of figures in this work, figures are placed in an appendix at the end of each numbered section to avoid interruption of text.

system timing resolution. Actual time pick-off circuits exhibit time walk (varying time delay) caused by variations in detector output amplitude and rise-time. This time walk degrades system timing resolution. Detector output amplitude variations are caused by varying event energy and detector energy absorption. Detector output rise-time variations are caused, particularly in semiconductor detectors, by energy absorption at varying locations in the detector.

The time walk of a simple level discriminator (also known as a leading-edge discriminator) for varying amplitude and rise-time input signals is shown in Figure 1-3. As shown in the figure, the simple level discriminator develops a timing signal whenever the input signal crosses the fixed threshold V_T and can exhibit time walk equal to a significant portion of the input signal rise-time. The walk performance of the simple level discriminator is acceptable for time-measurement system applications only if input signal rise-times are considerably shorter than the desired timing resolution, or if input signal amplitude and rise-time variations are small.

The constant-fraction discriminator (CFD) is a time pick-off circuit that develops a timing signal that is largely insensitive to input-signal amplitude and rise-time. This circuit was first reported by Gedcke and McDonald [1, 2] in 1967 and 1968, and is in wide use today. As seen in the CFD block diagram of Figure 1-4, attenuated and delayed versions of the input signal are compared using a comparator to develop a timing signal when these two signals are equal. This timing signal, assuming there are no comparator time-walk errors, is insensitive to input signal amplitude and rise-time for linear-edge input signals as shown in Figure 1-5. The CFD can also be considered a shaping circuit where the attenuated version of the input signal is subtracted from the time-delayed version to produce a bipolar signal with a zero-crossing time that is insensitive to input amplitude and rise-time. This is also shown in Figure 1-5.

As shown in Figure 1-5, the CFD may be operated in two modes: the true constant-fraction mode and the amplitude-rise-time compensated (ARC) mode [3]. In the true constant-fraction mode, the timing point occurs *after* the input signal reaches its peak value (flat-top pulses are assumed) when the delayed signal is equal to a fixed (constant) fraction of the input signal peak value. In the true constant-fraction mode, CFD timing is insensitive to input amplitude, but is not insensitive to input rise-time. In the amplitude-rise-time compensated mode, the timing point occurs *before* the minimum rise-time input signal reaches its peak value. In this mode, CFD timing is insensitive to both input

amplitude and rise-time provided input rise-time is greater than the minimum rise-time selected for operation.

The selection of true-constant fraction operation or amplitude-rise-time compensated operation is determined from the minimum input signal rise-time ($t_{r\,(min)}$), the signal delay (t_d) chosen, and the signal fraction (f) chosen as described in the equations in Figure 1-5. Typically, a fraction close to 20% is used with the delay chosen to select either true constant-fraction or amplitude-rise-time compensated operation. As seen for signals *1* and *2* in Figure 1-5, signal slope through the timing point is higher for the true constant-fraction mode compared to the amplitude-rise-time compensated mode. As a result, there is a noise advantage (less timing jitter) in using the true constant-fraction mode. However, as mentioned, the true constant-fraction mode does not provide rise-time insensitive timing.

The arming comparator shown in the CFD block diagram of Figure 1-4 is used to inhibit the CFD timing output unless the input signal is above a preset threshold level. This is required as the CFD will normally trigger continuously on input noise when no input signal is present.

Applications of Time-Measurement Systems

Experimental Physics and Industrial Applications

Time-measurement systems are widely used in nuclear structure and particle physics experiments. Applications include measuring the lifetimes of excited nuclear states, time measurements for particle identification, and time-of-flight measurements for heavy-ion mass spectrometry [4]. Additional applications include locating x-ray scattering and diffraction using position-sensitive detectors in conjunction with time-spectroscopy measurements [5].

Time-measurement applications are not limited to the measurement of nuclear or x-ray radiation as there are many applications in radio and laser ranging. In a ranging application, the time intervals between transmitted and reflected radio or light pulses are measured to determine physical distance. Industrial laser ranging applications include the measurement of levels in silos, automatic control of robots and manipulators, and dimension measurement in mechanical and construction industries [6].

Laser ranging measurements are used to measure the difference in earth movement on both sides of the San Andreas fault in California for possible earthquake prediction [7, 8]. In a ground-based system, laser ranging is done using reflections from the Laser Geodetic Satellite [7]. In this system, a time digitizer with 9.76-ps channels is used for time

measurements. CFDs are used to provide accurate time pick-off signals from the laser light-detector signals which vary greatly in intensity due to atmospheric conditions. Another similar system, planned for space-borne operation in the Space Shuttle, will operate by reflected laser light from small reflective cubes located on both sides of the San Andreas fault [8]. The measurement accuracy of this space-borne system is expected to be ±2 cm.

Positron Emission Tomography Applications

The CFD development described in this work is for use in commercial positron emission tomography (PET) medical imaging systems. These systems are designed and manufactured (under the name Siemens) by CTI PET Systems, Inc. in Knoxville, Tennessee. In these systems, time measurement is required to detect the time coincidence of twin, 511-keV, 180°-opposing gamma rays that result from the annihilation of a positron with a neighboring electron.

In a PET system, many gamma-ray detectors are arranged adjacent to each other in a ring that encircles the patient. Additionally, other parallel rings of detectors are used to provide for axial coverage of the patient. Through the use of time-coincidence circuitry, the time-coincident, opposing gamma rays from a positron annihilation are detected and histogrammed for all possible opposing detector pairs, the lines through these detector pairs being known as lines of response. The histogrammed array of coincident events for all lines of response is known as a sinogram and is converted to an image following certain correction and filtering operations. A block diagram of a commercial PET system is shown in Figure 1-6.

In the conventional PET system just described, time-coincidence measurements are used to locate positron annihilations on various lines of responses without regard for where on the lines the annihilations occurred. In time-of-flight (TOF) PET systems, additional time resolution is used to locate a positron annihilation along a line of response through the difference in gamma-ray arrival time at the detectors. TOF PET systems are not in wide use today because commercially available fast scintillation detectors have poor energy and poor spatial resolution compared to the Bismuth Germanate (BGO) scintillators used in conventional PET systems. There is, however, great interest in the PET community in the development of a scintillator with sufficient time resolution for time-of-flight operation while maintaining the energy and spatial resolution of BGO scintillators. Time-of-flight information offers improvements in PET imaging by reducing the image noise caused by random coincidences (coincidences from separate positron annihilations) and by improving spatial information. One recently developed research TOF PET system with Barium

Fluoride (BaF_2) scintillation detectors has time-measurement channels of 62.5 ps and a timing resolution (dominated by the detectors) of slightly over 600-ps FWHM [9].

Medical images are obtained in PET systems by labeling biochemical compounds with positron-emitting isotopes so that the resulting biochemical tracers may be imaged in the human body. These biochemical tracers allow the imaging of metabolism, blood-flow, oxygen, cancer, brain function, and other biological functions. The imaging of biochemical function through these tracers significantly differentiates PET imaging from other medical imaging systems, such as Computerized-Axial Tomography (CAT) and Magnetic-Resonance Imaging (MRI), which image tissue structure and have limited biochemical function imaging capability.

PET metabolic imaging permits the diagnosis and location of severe brain epilepsy for surgical removal where the affected area of the brain cannot be seen using structural imaging or even using surgical examination. Similarly, PET metabolic and blood-flow imaging permits study of the heart muscle to determine if tissue is viable (alive) or necrotic (dead). If an affected area of the heart muscle is necrotic, heart bypass surgery to resupply blood to this area would not benefit the patient, whereas the patient would likely benefit from bypass surgery if the affected area is still viable. In addition to the clinical PET applications described, there are other clinical applications and many research applications in use worldwide. Brain research applications include study of mental illness, dementia, and pharmacological drug effects. Other research applications include the diagnosis and treatment evaluation of cancer tumors. Although much of the PET medical application literature is targeted for physicians and medical researchers, the overview paper by Wagner is recommended for the nonmedical reader desiring further PET application information [10]. Additionally, the paper by Phelps et al. [11] on PET brain imaging and the paper by Chollar et al. [12] on PET heart imaging are recommended for PET application information.

Presently, there are over 122 PET systems installed or under construction worldwide [13]. This number is projected to exceed 650 by the year 1995, illustrating the rapid growth of PET medical imaging [13].

Significance of Integrating a CFD into CMOS Technology for PET Systems

PET System Detector and Front-End Electronics Requirements

The commercial Siemens ECAT EXACT-HR PET system, manufactured by CTI PET Systems, Inc., consists of 784 BGO detector crystal elements in a single ring with a diameter of 82.3 cm [14]. Twenty-four of these rings are used to provide 15 cm of axial patient

coverage giving a total of 18,816 individual BGO detector crystal elements. These detector crystal elements are arranged in three rings consisting of 112 *block detectors* each. Each *block detector* consists of a 7 x 8 array (7 elements in the transaxial direction, 8 elements in the axial direction) of crystal elements attached to four photomultiplier tubes (PMTs) providing scintillation light detection. Each block detector is then connected to a front-end analog signal-processing circuit that amplifies the PMT output signals, decodes the PMT output signals into transaxial and axial position information, sums the PMT output signals for energy information, and develops a constant-fraction timing signal from the summed PMT output signals. The front-end analog signal processing circuit also contains flash analog-to-digital converters (ADCs) giving transaxial position, axial position, and energy information. The digital data from these flash ADCs is passed to a front-end digital-signal processing circuit that assigns each detected gamma ray to a specific crystal element and determines if the event energy is within an acceptable energy window. The front-end digital-signal processing circuit also provides time-to-digital conversion using the constant-fraction developed timing signal as a *start* signal and a system clock as the *stop* signal. A block diagram of a single block-detector channel complete with the front-end analog and digital circuitry is shown in Figure 1-7.

Since 336 front-end analog and digital circuits are required to process signals from the 336 block detectors in the Siemens ECAT EXACT-HR PET imaging system, the large quantity of repeated circuits justified a development program to develop both analog and digital custom CMOS integrated circuits for these circuits. The development of these custom CMOS circuits includes the development of a CFD as a part of the analog circuit development.

Advantages of Integrating PET Front-End Circuits into Custom CMOS Circuits

Listed below are the actual numbers of discrete components (includes commercial integrated circuits) and solder connections present in the 336 front-end analog circuits of the commercial Siemens ECAT EXACT-HR PET system [14].

Front-End Analog Component and Solder Connection Count for the Siemens ECAT EXACT-HR PET System

- 84,000 discrete components (250 x 336)
- 301,728 solder connections (898 x 336)

The compelling reasons for developing PET front-end analog circuits into custom CMOS integrated circuits include lower manufacturing costs, improved system reliability, smaller

physical space requirements, lower power supply requirements, lower risks of component availability problems, and the potential of later mixed analog and digital circuit integration.

In order for PET imaging systems to be available outside large research hospitals, it is necessary for system costs to be nearly halved from the present cost of over two-million-dollars per system. Lower manufacturing costs in PET electronics are required to meet overall cost objectives, and cost savings of at least a factor of four are projected using CMOS implementations. The factors affecting manufacturing cost reductions are listed below.

Factors Lowering Electronic Manufacturing Costs Using CMOS Integration (Expected Factor-of-Ten Component and Solder Count Reduction)

- Lower parts costs using custom integrated circuits compared to discrete components
- Fewer parts to order, inventory, and sort
- Fewer parts vendors to track for component availability
- Fewer parts to preform, insert, and solder
- Fewer parts to insert or solder incorrectly for later repair
- Smaller printed-circuit board size required
- Less circuit inspection for proper component and solder assembly required
- Less final circuit testing time and troubleshooting time required

In addition to significant reductions in PET system costs, improved reliability is required in PET systems for widespread clinical acceptance. Clinical users are less tolerant of PET system reliability problems compared to research users as the clinical users schedule larger number of patients for imaging and are usually less familiar with the technical operation of a PET system. Factors outlining the projected reliability improvements and significance of these improvements by using CMOS integration of PET front-end circuits are listed below.

Reliability Improvement and Resulting Significance Using CMOS Integration (Expected Factor-of-Ten Solder and Component Count Reduction)

- Discrete implementation of 300,000 solder connections with solder failure rate of 10 ppm (parts-per-million) per year would result in 3 average system failures per year
- CMOS implementation of 30,000 solder connections with solder failure rate of 10 ppm per year would result in one average system failure per 3.3 years
- Reliability is paramount as patients may be scheduled for surgery pending results of PET imaging

- Reliability is paramount as extensive patient rescheduling is required to compensate for system downtime
- Reliability is paramount as many hospitals are now requiring PET system suppliers to pay penalties for system downtime

In addition to the cost and reliability advantages described for integrating PET front-end functions into CMOS processes, the advantages listed below are also significant.

Other Advantages Using CMOS Integration

- Much smaller physical circuit space required (at least a factor-of-four)
- Lower power requirements and heat dissipation (at least a factor-of-four)
- Critical high-speed sole-source analog integrated circuits are eliminated with sole-source issues addressed by identifying alternate CMOS foundries for CMOS fabrication

It would be possible to integrate the PET front-end analog electronics into a high-speed bipolar process and this was investigated initially. It is, however, more advantageous to integrate the PET front-end electronics in a CMOS process versus a bipolar process for the reasons listed below.

Advantages of CMOS Integration Compared to Bipolar Integration

- Analog switches, digital-to-analog and analog-to-digital conversion, and most digital functions can be integrated more effectively in CMOS processes [15]
- Front-end analog CMOS circuits can be integrated on a large, predominantly digital CMOS VLSI circuit
- CMOS processes are much more widely used, permitting potential multiple sources
- CMOS production die costs are approximately a factor-of-two lower because of larger wafers, higher yields, and higher overall circuit volume
- CMOS mask charges are lower since typically 13 masks are required compared to typically 20 masks (for bipolar)
- CMOS prototyping charges are *significantly* lower through the use of the MOSIS prototype service where prototype CMOS integrated circuits are available for $510.00 [16]

Scope of Dissertation

The role of time measurement in PET systems and the significance of integrating PET timing systems using CMOS integrated-circuit technology has been established. The scope of this dissertation then, is the development of a fully-monolithic CMOS CFD as a part of a complete PET timing system. This timing system is itself part of a complete PET monolithic CMOS (gamma-ray) timing, energy, and position processing circuit.

In order to develop the fully-monolithic CMOS CFD, three separate objectives must be met. The first objective is the development of analysis which permits the prediction of CFD energy-discrimination and timing performance for a selected CFD circuit topology and scintillation-detector system. Such analysis is necessary to predict system performance prior to integrated-circuit fabrication. The second objective is the development of non-delay-line CFD timing-shaping networks having performance comparable to existing delay-line networks. Non-delay-line networks are required to permit a fully monolithic CFD implementation. The third and final objective is the development of high-speed CMOS circuits necessary for implementation of the fully-monolithic CMOS CFD circuit. These circuits include a wideband continuous-time filter to implement the non-delay-line timing-shaping network and a low time-walk comparator to derive the CFD timing signal.

Although the immediate application of the monolithic CMOS CFD presented here is for use with PET BGO/photomultiplier detectors with timing resolutions of approximately 3-ns FWHM, the CFD was designed to permit transition into time-of-flight PET applications with detector timing resolutions of approximately 400-ps FWHM. Subnanosecond timing-resolution performance is available for future applications because of the development of high-performance CMOS timing-shaping circuits and timing comparators. The fully-monolithic CMOS CFD presented here contains no external delay lines or other components, except for the components required to develop the arming-threshold voltage which will be integrated later using an on-chip digital-to-analog converter (DAC).

New Contributions Presented in Dissertation

Although a fully-monolithic bipolar integrated-circuit CFD was reported by Tanaka et al. [17] during the course of this work, no fully-monolithic CMOS integrated-circuit CFD is believed to have been reported. The feasibility of implementing CFD CMOS timing circuits has been reported by Binkley et al. for a monolithic CMOS CFD requiring an external delay line [18]. The fully-monolithic bipolar CFD reported by Tanaka et al. [17] uses the non-delay-line CFD circuits developed by Nowlin [19, 20] which are not used in the monolithic CMOS CFD presented here. Instead, considerably different CFD circuits were developed which have been designated as *Binkley CFD* circuits to differentiate them from the Nowlin and traditional delay-line CFD circuits. The Binkley CFD circuits offer performance and implementation advantages compared to the Nowlin circuit. The performance advantages include increased shaping-signal underdrive and zero-crossing slope, and reduced shaping-signal timing jitter through the use of second- or higher-order Binkley CFD circuits. Additionally, the Binkley CFD circuits do not require the floating capacitor required in the

Nowlin CFD circuits for circuit differentiation. As a result, the Binkley CFD circuits are more easily implemented in monolithic integrated circuits. A patent is currently pending for the Binkley CFD circuits [21].

In order to predict the energy-discrimination and timing performance of the monolithic CMOS CFD, Monte Carlo analysis was developed to generate a predicted CFD energy and timing spectrum resulting from scintillation-detector statistical noise. Although Monte Carlo analysis has been reported for determining the arrival times of scintillation-detector photoelectrons [22, 23, 24, 25], it is not believed that the energy-discrimination and timing performance of time pick-off circuits has been included in this analysis. Monte Carlo analysis is useful for selecting CFD circuit configurations that will give desired performance for a given scintillation detector. A paper describing Monte Carlo simulation of CFD performance has been presented at the 1992 IEEE Nuclear Science Symposium [26].

Two circuits included in the monolithic CMOS CFD are described in detail in this work, both of which are believed to be new contributions. The first circuit is a wideband (-3-dB bandwidth of over 100 MHz) 2-μ CMOS continuous-time filter for implementation of a Binkley CFD timing-shaping circuit. This current-mode fifth-order filter circuit, although fully differential, does not require common-mode feedback and requires only 60 MOSFET devices, 18 of which are only required for testing with voltage signals. The second circuit described is a low time walk CMOS voltage comparator having SPICE-simulated walk performance of 175 ps for input-signal amplitudes ranging from 10 - 2000 mV and input-signal rise-times of approximately 10 ns. A comparison, given in this work, of SPICE-simulated and measured comparator walk performance for a similar comparator design indicates that actual walk performance may be comparable or lower than SPICE-simulated walk. The walk performance for the CMOS CFD voltage comparator is comparable to that reported for high-speed ECL bipolar comparators [27, 28]. Comparisons of comparator topologies and device selections (MOSFET sizes) for a selected topology are given with regard to minimizing comparator walk performance. This is believed to be the first reported discussion of comparator design for low time walk.

Organization of Dissertation

In this work, the material in *Section 2* provides the analysis methods necessary for evaluating system timing errors due to walk and circuit noise-induced timing jitter in time pick-off circuits. The material in *Section 3* provides the analysis methods necessary for evaluating system timing errors due to scintillation-detector statistical noise. Together, the material in *Sections 2* and *3* provides the background necessary for evaluating the

performance of existing CFD circuits as well as the performance of the newly developed Binkley CFD circuits. The evaluation of existing CFD circuits, as well as the development and evaluation of the Binkley CFD circuits, is then covered in *Section 4.* Issues surrounding the practical implementation of CFD circuits are discussed in *Section 5*, including the development and evaluation of a fully-monolithic CMOS CFD. Finally, concluding remarks and suggestions for future research are contained in *Section 6.*

Each section begins with an overview discussion introducing the topics covered in the section and the relationship of these topics to the development and implementation of non-delay-line CFD circuits.

References for Section 1

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Appendix for Section 1 — Figures

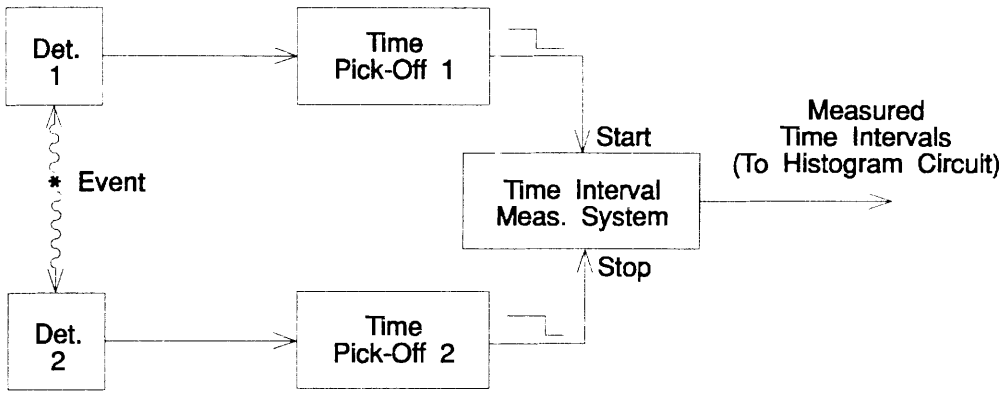

Figure 1-1. Block Diagram of a Time-of-Flight Time Spectroscopy System.

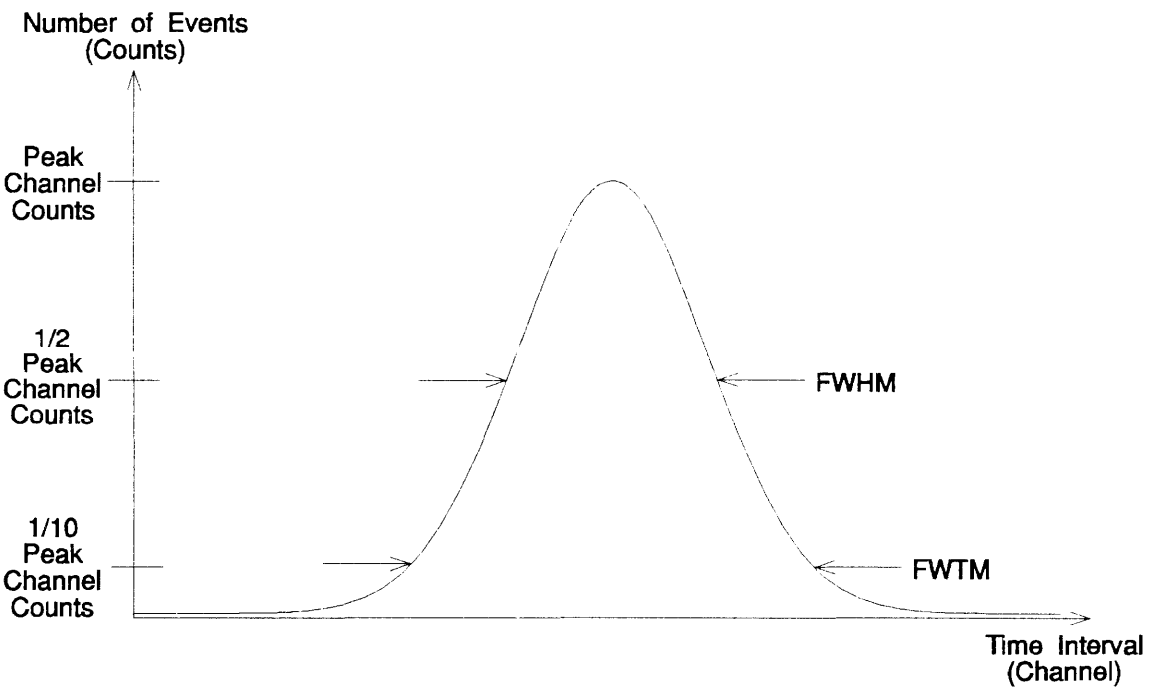

Figure 1-2. Timing Coincidence Spectrum.

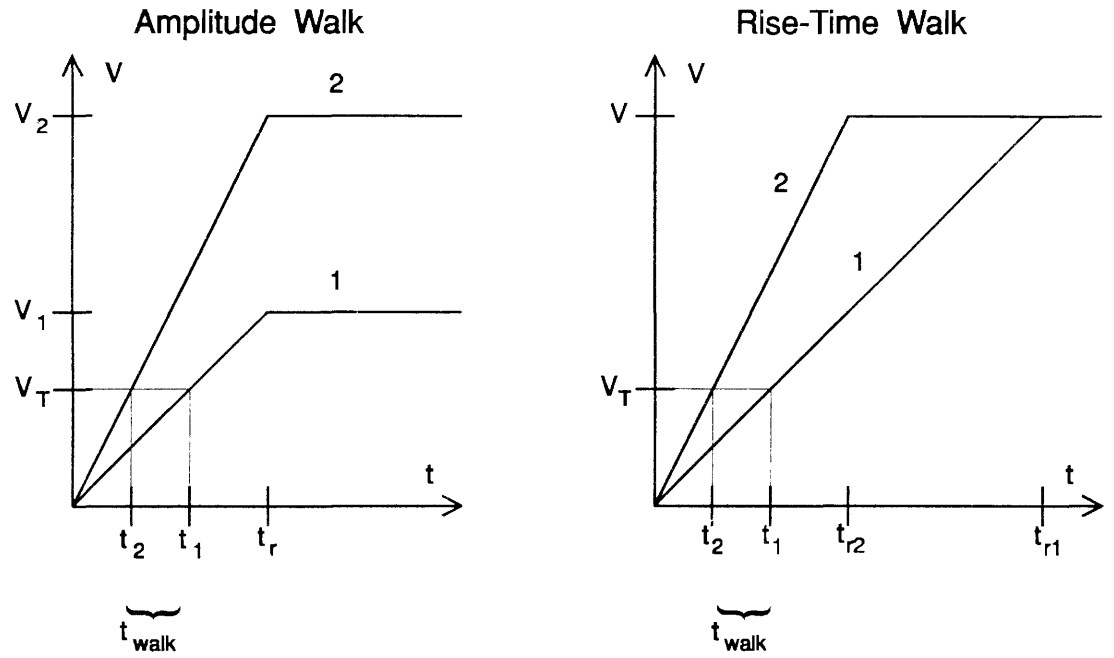

Figure 1-3. Illustration of Amplitude and Rise-Time Walk for a Leading-Edge Discriminator.

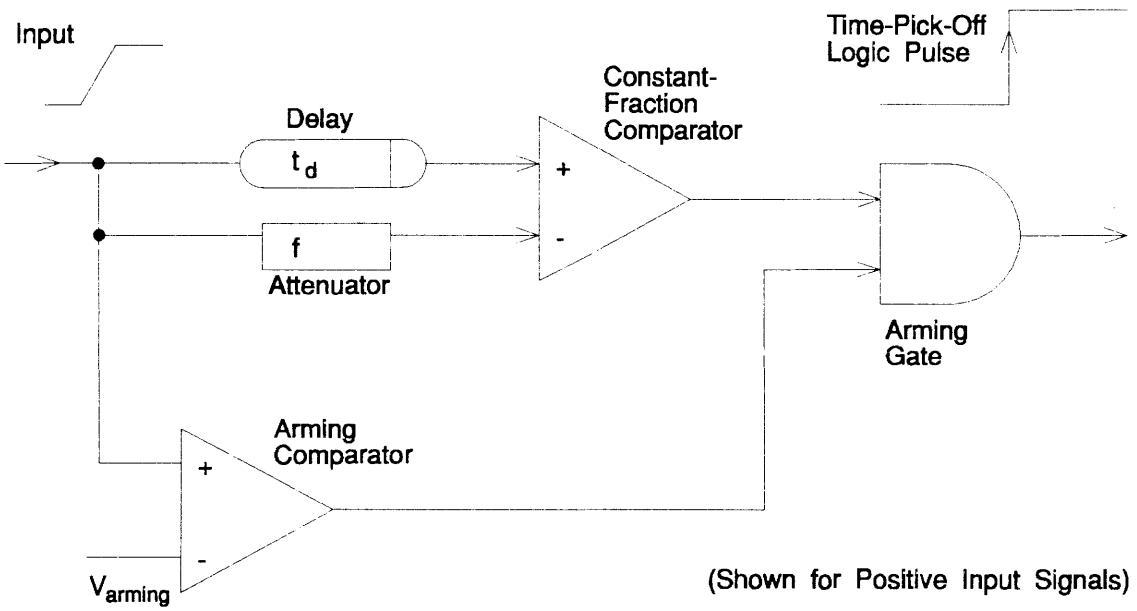

Figure 1-4. Block Diagram of a CFD.

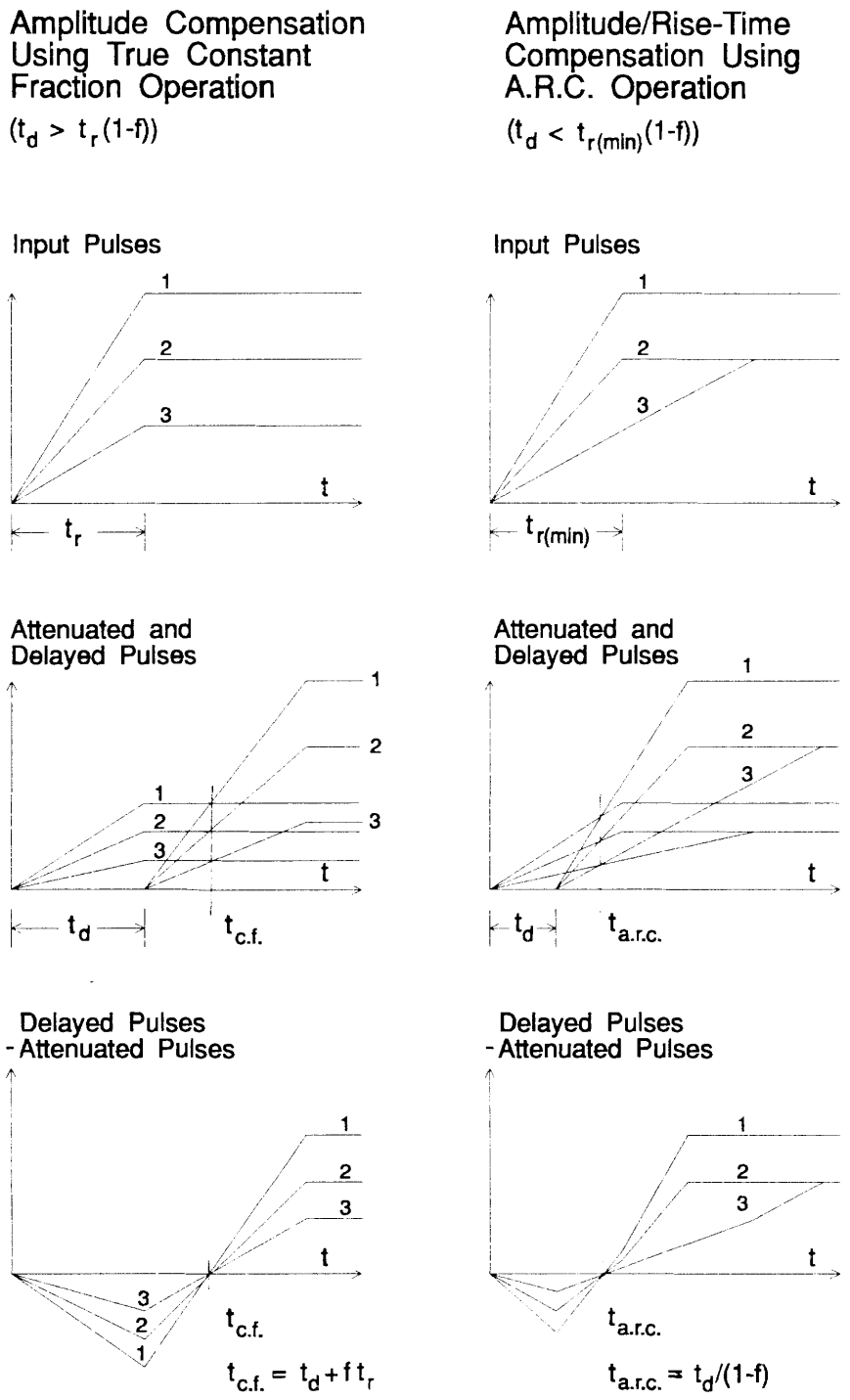

Figure 1-5. Illustration of CFD Operation for Linear-Edge, Flat-Top Pulses.

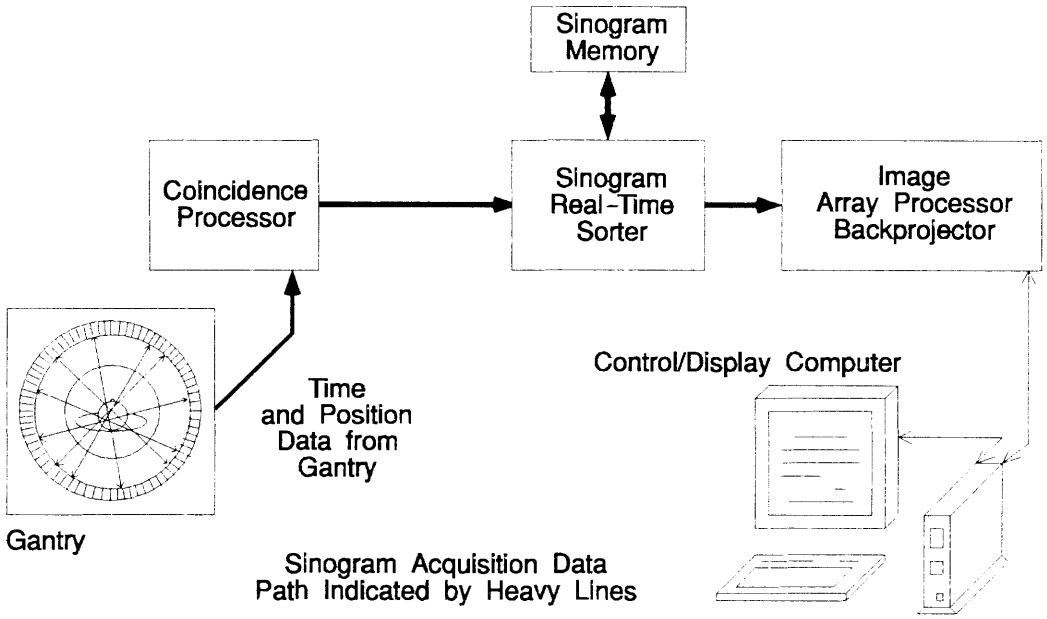

Figure 1-6. Block Diagram of a Commercial PET Imaging System.

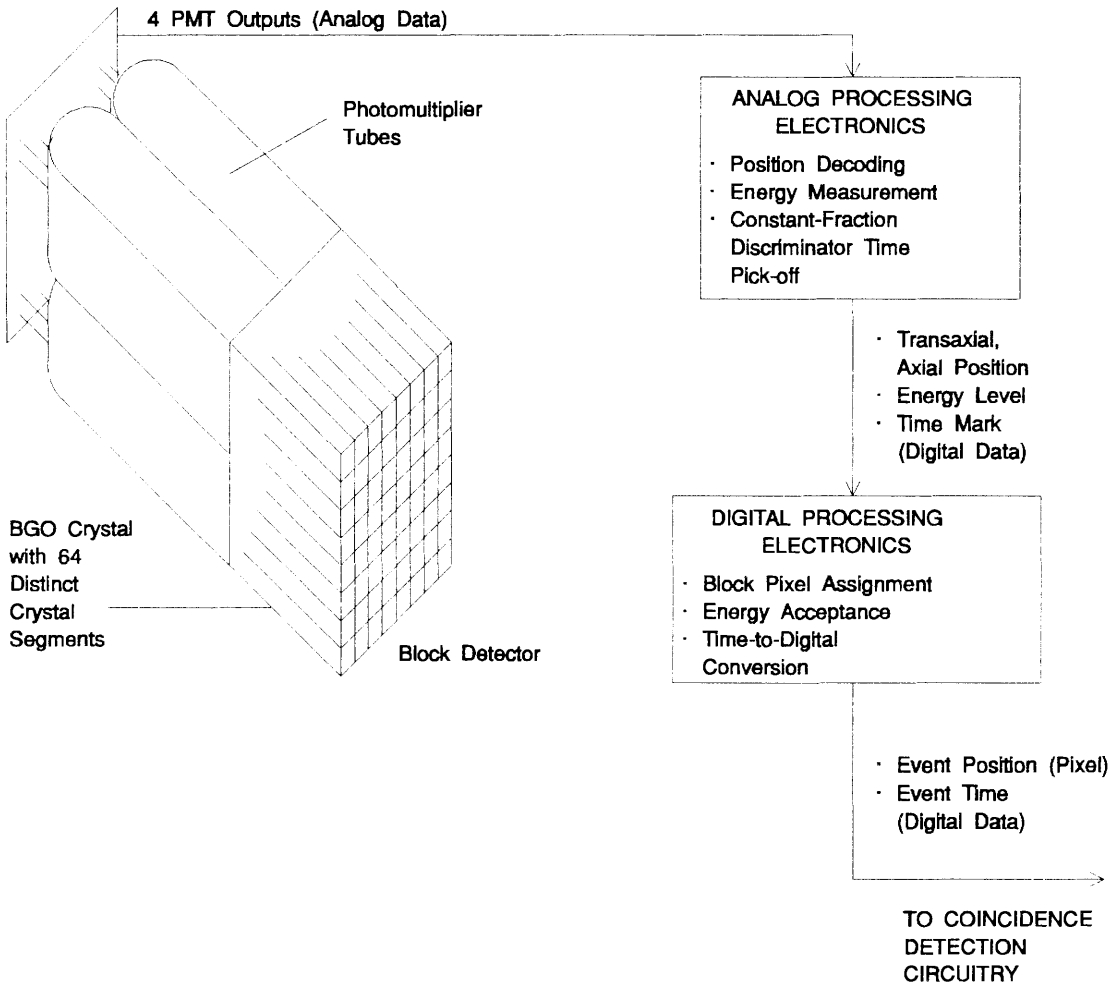

Figure 1-7. Block Diagram of a Block-Detector, Front-End Electronics Channel for a Commercial PET Imaging System.

2. TIMING PERFORMANCE OF TIME PICK-OFF CIRCUITS

Overview

In this section, the performance of time pick-off circuits is considered excluding the effects of detector statistical noise. Degradation of system timing resolution caused by time walk in time pick-off circuits is described and examples are given for the walk introduced by leading-edge and CFD time pick-off circuits. In addition, time walk introduced by practical comparators for input signals of varying slope and overdrive is described using the comparator charge-sensitivity model. Minimizing comparator time walk is a major design objective for the timing comparator in the monolithic CMOS CFD described later in *Section 5*.

Timing jitter in time pick-off circuits, caused by electronic noise, is also considered in this section. The concept of optimal or matched filters for minimum timing jitter is presented along with several examples of nonrealizable optimal timing filters. The optimal filter analysis is used to give insight into physically realizable, suboptimal timing filters. One example is given for scintillation-detector systems where both the input signal and white circuit noise are bandwidth limited by front-end amplification circuitry. For this case, it is shown that it is desirable to maximize signal bandwidth since signal slope increases directly with bandwidth while total noise increases as the square-root of bandwidth. In another example, an optimal timing filter is presented for a linear-edge input signal in the presence of white noise. The performance of this optimal filter is compared with the performance of a single-pole lowpass filter having various time constants. Here, the advantage of limiting system bandwidth, assuming white circuit noise, to that bandwidth just required to preserve the input signal slope is discussed as a way of minimizing timing jitter.

Circuit noise-induced timing jitter is not a significant contributor of system timing errors for the initial monolithic CMOS CFD application with PET BGO/photomultiplier scintillation detectors. However, circuit noise is the dominant contributor of timing errors for BGO/avalanche-photodiode scintillation detectors because of photodiode noise. The discussions of circuit-noise timing-jitter effects are included for completeness and to permit the design of timing systems where circuit noise-induced timing jitter is a significant contributor of timing error. This section concludes with a brief discussion of time-variant timing filters as well as a discussion of temperature- and time-related time drift in time pick-off circuits.

Time Walk

Leading-Edge Discriminator Time Walk

The leading-edge discriminator, described in *Section 1*, develops a timing signal whenever its input signal crosses a fixed threshold. As was shown in Figure 1-3 (page 15), time walk from a leading-edge discriminator can equal a significant portion of the input-signal rise-time. The propagation delay of an ideal leading-edge discriminator, one in which the comparator propagation delay is zero, can be determined graphically from Figure 1-3. The propagation delay is given by

$$t_{prop} = \frac{V_T\, t_r}{V_{inpk}} \quad , \tag{2-1}$$

where V_T is the threshold (referenced to the initial signal level), t_r is the input-signal (linear-edge) rise-time, and V_{inpk} is the input-signal amplitude. Equation 2-1 is valid only for input-signal amplitudes above the threshold ($V_{inpk} > V_T$), and the discriminator propagation delay is always less than the input-signal rise-time ($t_{prop} < t_r$). The leading-edge discriminator is not triggered, of course, for signals below the threshold.

In Figure 2-1, ideal leading-edge discriminator propagation delay (Equation 2-1) is plotted for a 0.5-V threshold for signals of varying amplitude with fixed 10-ns rise-times. The propagation delay is almost 10 ns for signals slightly over the 0.5-V threshold and is 2.5 ns for 2-V signals. The corresponding time walk is nearly -7.5 ns for a 0.5-V to 2-V input range with the propagation delay decreasing monotonically with increasing signal level (the propagation delay is inversely proportional to signal level).

The effect of leading-edge discriminator time walk on system timing performance is found by evaluating the leading-edge discriminator timing spectrum (the output timing probability density) for a given input-voltage spectrum. The input spectrum, representing varying input signal levels, is transformed to a timing spectrum representing varying propagation delays. This may be evaluated mathematically using a transformation of random variables where the input random variable corresponds to the input-voltage spectrum, the transformation function corresponds to the leading-edge discriminator propagation-delay function, and the output random variable corresponds to the resultant leading-edge discriminator timing spectrum.

The monotonic transformation of a random variable is described by

$$p_t(t) = \left|\frac{d}{dt} T^{-1}(t)\right| p_v\left[T^{-1}(t)\right] \quad , \tag{2-2}$$

where $p_t(t)$ is the probability density of the output random variable t, $p_v(v)$ is the probability density of the input random variable v, $t = T(v)$ is the transformation function mapping the input random variable v to the output random variable t, and $v = T^{-1}(t)$ is the inverse transformation function mapping the output random variable t to the corresponding input random variable v [1]. Equation 2-2 applies for both monotonically increasing or decreasing transformation functions.

The timing spectrum for the leading-edge discriminator described by Figure 2-1 will be evaluated using Equation 2-2 for a Gaussian input-voltage spectrum with the probability density function

$$p_v(v) = \frac{1}{\sqrt{2\pi\sigma_v^2}} e^{\frac{-(v-\mu_v)^2}{2\sigma_v^2}} \quad , \tag{2-3}$$

where μ_v is the mean input voltage and σ_v^2 is the input voltage variance. The random variable transformation function ($t = T(v)$) is the leading-edge discriminator propagation delay given in Equation 2-1 (shown in Figure 2-1) for fixed V_T and t_r with substitutions $t_{prop} = t$ and $V_{inpk} = v$, giving

$$t = T(v) = \frac{V_T t_r}{v} \quad . \tag{2-4}$$

The inverse transformation function ($v = T^{-1}(t)$) is available explicitly by solving Equation 2-4 for v in terms of t, giving

$$v = T^{-1}(t) = \frac{V_T t_r}{t} \quad . \tag{2-5}$$

Finally, the derivative of the inverse transformation function is determined by differentiating Equation 2-5 with respect to t, giving

$$\frac{d}{dt} T^{-1}(t) = \frac{-V_T t_r}{t^2} \quad . \tag{2-6}$$

Now that all terms of Equation 2-2 have been found, the timing spectrum for a leading-edge discriminator can be obtained for a given Gaussian input-voltage spectrum. The leading-edge discriminator considered has a threshold (V_T) of 0.5 V with input-signal rise-times (t_r) of 10 ns. The propagation delay, taken from Equation 2-1, is shown in Figure 2-1. A Gaussian input-voltage spectrum having a mean voltage of 1 V and a standard deviation (σ_v) of 0.213 V will be considered for the leading-edge discriminator. This input-voltage spectrum has a resolution of 0.5 V FWHM (FWHM = 2.35σ for a Gaussian density), or a resolution of 50% FWHM expressed as a percentage of the mean. This is comparable to the energy resolution of a BGO block detector used in commercial CTI/Siemens PET systems (the energy spectrum of a BGO block detector is wider than the energy spectrum of a single-crystal BGO detector because of variations in PMT light coupling between different block-detector crystal elements) [2]. The leading-edge discriminator input-voltage spectrum is shown in Figure 2-2, and the resultant leading-edge discriminator timing spectrum is shown in Figure 2-3 for the propagation delay shown in Figure 2-1.

The timing spectrum shown in Figure 2-3 is not Gaussian because of the nonlinear propagation delay of the leading-edge discriminator. The timing spectrum is wider for higher time values due to the larger increase in propagation delay for smaller input signals. If the propagation delay were linear with signal level, the output timing spectrum would be Gaussian for the Gaussian input voltage spectrum.

The timing resolution of 2.2 ns FWHM (Figure 2-3) for the ideal leading-edge discriminator considered here is significant compared to a typical timing resolution of 3 ns FWHM for commercial PET BGO/photomultiplier detector timing systems [2]. System FWHM timing resolution would be degraded to 3.72 ns from 3 ns if the leading-edge discriminator timing resolution of 2.2 ns was combined (assuming Gaussian timing spectra) in an uncorrelated way with a detector-statistical timing resolution of 3 ns. The evaluation of actual system timing performance, however, is considerably more complex because of correlation between the statistical threshold-crossing time and leading-edge discriminator walk (a higher detector photoelectron rate reduces the statistical threshold crossing time and reduces walk due to higher signal slope). Additionally, Gaussian timing spectra cannot be assumed. The timing performance of systems using leading-edge or CFD timing can be evaluated using the Monte Carlo techniques described in *Section 3*. Leading-edge discriminator timing performance can be improved by lowering the threshold voltage, by decreasing the input-signal rise-time, or by raising the input-signal level. Each of these actions will lower leading-edge discriminator time walk.

Comparator Time Walk

The CFD, as described in *Section 1*, is a pulse-shaping circuit that produces a bipolar output pulse having a zero-crossing point that is time invariant for linear-edge input signals of varying level. It will be discussed in *Section 4*, that this timing point is time invariant for inputs of varying level having arbitrary fixed shapes, including nonlinear leading edges. Actual CFDs do exhibit time walk with varying input signal levels due to comparator walk errors. These errors are due to varying comparator propagation delay as a function of signal slope, signal underdrive (initial signal level below the threshold), and signal overdrive (final signal level above the threshold).

Comparator walk can be described using a charge-sensitivity model where comparator triggering occurs after a fixed amount of charge has been exchanged at the comparator input after the input exceeds the threshold [3]. Comparator charge sensitivity is illustrated in Figure 2-4 for two cases: comparator triggering along the signal edge and comparator triggering after the signal edge. Linear-edge signals are considered for both cases in Figure 2-4.

For the case of comparator triggering along the signal edge (Figure 2-4), the voltage-time area (A) related to comparator charge sensitivity is a triangle with base equal to the propagation delay (t_{prop}) and height equal to the effective change in comparator threshold (ΔV_T). The charge related area for comparator triggering along the signal edge is given by

$$A = \frac{t_{prop}\,\Delta V_T}{2} \quad . \tag{2-7}$$

Equation 2-7 can be rewritten as

$$A = \frac{t_{prop}^2}{2}\frac{\Delta V_T}{t_{prop}} \quad , \text{or} \tag{2-8}$$

$$A = \frac{t_{prop}^2 K}{2} \quad , \tag{2-9}$$

where the signal slope, K, is equal to $\Delta V_T/t_{prop}$. Solving Equation 2-9 for the propagation delay gives

$$t_{prop\ (triggering\ on\ signal\ edge)} = \sqrt{\frac{2A}{K}} \quad . \tag{2-10}$$

Comparator propagation delay for triggering along the signal edge, as described in Equation 2-10, decreases monotonically with increasing signal slope and is proportional to the inverse square root of signal slope.

The second case considered in Figure 2-4 is the case of comparator triggering after the signal edge (on the final value of the signal). For this case, the voltage-time area (A) related to comparator charge sensitivity consists of two components: the triangular area along the signal edge and the rectangular area after the signal edge. The triangular area has a base equal to time t_1 and height equal to the input-signal overdrive ($V_{overdrive}$). The rectangular area has width of time t_2 and height also equal to the input-signal overdrive ($V_{overdrive}$). The total voltage-time area is given by

$$A = \frac{V_{overdrive}t_1}{2} + V_{overdrive}t_2 \quad . \tag{2-11}$$

From Figure 2-4, the time t_1 is given by

$$t_1 = \frac{V_{overdrive}}{K} \quad , \tag{2-12}$$

where K is the input-signal slope. Equation 2-11 can be solved for the comparator propagation delay ($t_{prop} = t_1 + t_2$) using Equation 2-12 giving

$$t_{prop\ (triggering\ after\ signal\ edge)} = \frac{A}{V_{overdrive}} + \frac{V_{overdrive}}{2K} \quad . \tag{2-13}$$

Comparator propagation delay in Equation 2-13 can be considered for the special case of step inputs where the signal slope (K) is infinite. For this case, t_{prop} (step input) is given by

$$t_{prop\ (step\ input)} = \frac{A}{V_{overdrive}} \quad , \tag{2-14}$$

where comparator propagation delay decreases monotonically with increasing signal overdrive and is proportional to the inverse of signal overdrive.

Note that comparator propagation delay, as predicted in the charge-sensitivity model, goes as the inverse square root of signal slope for comparator triggering along the signal edge and goes as the inverse of signal overdrive for step inputs. It will be shown that the comparator charge-sensitivity model, although widely referenced, is not accurate for the CMOS comparators considered in this section and in *Section 5* since comparator propagation delay can actually increase with increasing signal level for moderate to large signals.

Time Pick-Off Circuit Walk Due to Comparator Time Walk

Timing performance of time pick-off circuits is found by obtaining the propagation delay as a function of input signal level which must include the comparator contributions. For the leading-edge discriminator, the propagation delay function previously described must be modified to include the additional delay caused by the comparator. Once the propagation delay function has been determined for any time pick-off circuit, this can be used to transform the input-signal spectrum into a corresponding timing spectrum using a transformation of random variables as was described for the leading-edge discriminator.

As mentioned previously, the CFD has no theoretical walk for varying amplitude signals of fixed shape, the walk being due entirely to the constant-fraction comparator circuit. This comparator walk performance must be evaluated for the signals actually present in a given CFD application where comparator input-signal slope, underdrive, and overdrive depend on the constant-fraction input-signal level (this assumes that no walk offset adjust has been applied to the comparator as will be discussed in *Section 4*).

The CFD timing spectrum due to time walk can be easily determined from Equation 2-2 for a Gaussian input-signal spectrum if CFD propagation delay is assumed to be a linear function of input-signal level for the input-signal range of interest. This approach involves the use of small-signal linearization for the propagation delay (which is nonlinear based on the charge sensitivity model) for a given input-signal range. The resulting timing spectrum is Gaussian having a mean and variance that are functions of the slope and intercept of the (linear) propagation delay function and the mean and variance of the input-signal spectrum. The linear propagation-delay function assumed can be represented by

$$t_{prop} = aV_{inpk} + b \quad , \tag{2-15}$$

where V_{inpk} is the input-signal level, a is the propagation delay slope, and b is the propagation delay time-axis intercept. The propagation delay slope may be either positive or negative corresponding to monotonically increasing or decreasing propagation delay. The

mean and variance of the resulting timing spectrum for a Gaussian input-signal spectrum is given by

$$\mu_t = a\mu_v + b \quad , \text{ and} \tag{2-16}$$

$$\sigma_t^2 = a^2\sigma_v^2 \quad , \text{ where} \tag{2-17}$$

μ_v is the mean input-signal level and σ_v^2 is the input-signal variance [1]. Since timing resolution is determined by the timing standard deviation (σ_t) and is independent of the timing mean (μ_t), timing resolution can be expressed by

$$\sigma_t = |a|\sigma_v \quad , \text{ or} \tag{2-18}$$

$$t_{FWHM} = |a| v_{FWHM} \quad , \tag{2-19}$$

where timing resolution (expressed in either standard deviation or FWHM) is found by simply multiplying the input-signal resolution (also expressed in either standard deviation or FWHM) by the absolute value of the propagation delay slope.

For purposes of illustration, timing resolution will be evaluated for the CMOS CFD (containing an external delay line) described in [4]. This CFD has a measured propagation delay that is almost linear for an input range of 0.5 V to 1.5 V for input signals with 20-ns rise-times. The propagation-delay slope is approximately 1.4-ns/V over this 0.5-V to 1.5-V range, being somewhat less for signals greater than 1 V. The propagation-delay slope is positive, indicating increasing propagation delay for increasing signal level. As mentioned earlier, the propagation delay of some practical comparators *increases* with increasing signal level for moderate to large signals which is in conflict with the comparator charge-sensitivity model.

The CMOS CFD timing resolution will be evaluated for the Gaussian input-signal spectrum shown in Figure 2-2 having a mean of 1-V and a standard deviation of 0.213 V (50% FWHM). The resulting CMOS CFD timing resolution (σ_t), from Equation 2-18, is 0.298 ns (1.4-ns/V multiplied by 0.213 V) or 0.7-ns FWHM which is considerably less than the resolution of 2.2 ns given earlier for the ideal leading-edge discriminator. Although timing resolution (caused by walk) for the CMOS CFD considered is considerably higher than that of bipolar circuits, it would have little effect on commercial PET BGO/photomultiplier timing systems where timing resolution is approximately 3 ns FWHM

due to detector statistical noise [2]. The fully-monolithic CMOS CFD presented in *Section 5* has considerably improved walk performance over that of the CMOS CFD considered here.

Timing Jitter Due to Electronic Noise

Evaluation of Timing Jitter

Electronic noise degrades system timing resolution by creating timing jitter in the output of a comparator circuit whenever a signal, perturbed by electronic noise, crosses the comparator threshold. Timing jitter is present in time pick-off circuits, both leading-edge and constant-fraction, where noisy signals cross the comparator threshold to develop time mark signals. Similarly, timing jitter is present in timing logic circuits where noisy logic signals cross the thresholds of other logic devices. The creation of timing jitter is illustrated in Figure 2-5 where a signal having noise bands of $\pm\sigma_v$ is shown crossing a comparator threshold voltage V_T. Timing jitter, as shown in Figure 2-5, is given by

$$\sigma_t = \frac{\sigma_v}{|K|} \quad , \tag{2-20}$$

where σ_t is the standard deviation of the timing jitter, σ_v is the standard deviation of the noise, and K is the signal slope. Equation 2-20 can also be found from Equation 2-2 where an input-voltage random variable is monotonically transformed (using the reciprocal of input-voltage slope) to an output-time random variable. In Equation 2-20, signal slope is assumed constant over the range of noise about the timing threshold crossing. Additionally, the noise is assumed to be stationary (its statistical representation constant) over the range of times corresponding to the timing jitter distribution. Finally, the noise is assumed symmetrically distributed as a single standard-deviation value is used to describe the noise while another single standard-deviation value is used to describe the timing jitter distribution.

If the noise shown in Figure 2-5 is Gaussian, the timing jitter will also be Gaussian. If the noise is nonGaussian, statistical representations for the timing jitter are still available from the geometric conversion of noise to timing jitter as shown in Figure 2-5. It is interesting to note that signal perturbations above the threshold ($V_T + \sigma_v$) generate timing points that are below the timing mean ($\mu_t - \sigma_t$), and similarly, signal perturbations below the threshold generate timing points above the timing mean. This reverse relationship of noise to timing jitter is present for positive signal slope and has no effect on Gaussian noise because of the symmetry present.

The noise jitter for a typical PET BGO/photomultiplier detector timing system can be evaluated using Equation 2-20. Assuming a front-end voltage gain of 100 (after the photomultiplier tube), an equivalent input-noise voltage of 4 nV/$\sqrt{\text{Hz}}$ (typical for commercial high-speed bipolar integrated circuits), and a noise bandwidth of 50 MHz, the circuit noise (σ_v) is approximately 2800 μV rms (4 nV/$\sqrt{\text{Hz}}$ x 100 x $\sqrt{50\ \text{MHz}}$) [2]. Assuming a circuit rise-time (10 - 90%) of 10 ns, and a signal level of 1 V, the signal slope is approximately 1-V/10 ns [2]. The resulting timing jitter (σ_t) due to electronic noise is approximately 28 ps rms [2800 μV rms/(1-V/10 ns)]. PET-system timing resolution is not significantly degraded by this level of electronic-noise timing jitter as the timing resolution of commercial PET BGO/photomultiplier detector systems is much higher (approximately 3 ns FWHM) [2].

The Optimum Filter for Timing

Electronic noise-induced timing jitter is directly proportional to signal noise and is inversely proportional to signal slope at the timing (threshold) point as shown in Equation 2-20. It is necessary then to minimize signal noise while maximizing signal slope in order to minimize timing jitter. For a nonbandlimited input signal (e.g., a step input) in the presence of white noise, it is advantageous to maximize circuit bandwidth to the extent possible as signal slope increases directly with bandwidth while circuit noise voltage (or current) increases only as the square root of bandwidth. Timing jitter would then decrease as the inverse square root of increasing bandwidth. If, however, signal slope is detector limited, circuit bandwidth should not be maximized above the point necessary to preserve the detector-limited signal slope as this would bring in unnecessary noise and raise the timing jitter.

The effects of linear, time-invariant circuit filtering on timing jitter can be evaluated using Fourier transform representations of the signal and noise. In Figure 2-6, a filter with response $G(\omega)$ is shown having input signal $V_{in}(\omega)$, input noise-power spectral density $S_{in}(\omega)$, output signal $V_{out}(\omega)$, and output noise-power spectral density $S_{out}(\omega)$. Douglass derived the optimum filter $G_{opt}(\omega)$ for minimizing timing jitter as a function of the input signal $V_{in}(\omega)$, the input noise-power spectral density $S_{in}(\omega)$, and the measurement time, t_{meas} [5]. The key results of this derivation follow for the inputs, outputs, and filter response shown in Figure 2-6.

$V_{in}(\omega)$ is the Fourier transform of the input signal $v_{in}(t)$ and is given by

$$V_{in}(\omega) = \int_{-\infty}^{\infty} v_{in}(t) e^{-j\omega t}\, dt \quad . \tag{2-21}$$

$V_{out}(\omega)$ is the Fourier transform of the output signal $v_{out}(t)$ and is given by

$$V_{out}(\omega) = V_{in}(\omega) G(\omega) \quad , \tag{2-22}$$

where $G(\omega)$ is the filter response in Fourier notation. In order to find the timing jitter, the output-noise voltage must be found. $S_{out}(\omega)$ is the output noise-power spectral density and is given by

$$S_{out}(\omega) = S_{in}(\omega)\, |G(\omega)|^2 \quad , \tag{2-23}$$

where $S_{in}(\omega)$ is the input noise-power spectral density. The mean-square output noise voltage is given by

$$e_{out}^2 = \frac{1}{2\pi} \int_{-\infty}^{\infty} S_{out}(\omega) d\omega \quad , \text{ or from Equation 2-23,} \tag{2-24}$$

$$e_{out}^2 = \frac{1}{2\pi} \int_{-\infty}^{\infty} S_{in}(\omega)\, |G(\omega)|^2 d\omega \quad . \tag{2-25}$$

In addition to finding the output-noise voltage, it is necessary to find the output-signal slope. The Fourier transform of the output signal slope is given by

$$F\left\{\frac{d}{dt} v_{out}(t)\right\} = j\omega V_{out}(\omega) \quad , \text{ or from Equation 2-22,} \tag{2-26}$$

$$F\left\{\frac{d}{dt} v_{out}(t)\right\} = j\omega V_{in}(\omega) G(\omega) \quad . \tag{2-27}$$

The output-signal slope in the time domain is the inverse Fourier transform of Equation 2-27 and is given by

$$\frac{d}{dt}v_{out}(t) = \frac{1}{2\pi}\int_{-\infty}^{\infty} j\omega\, V_{in}(\omega)G(\omega)\; e^{j\omega t}\; d\omega \quad . \tag{2-28}$$

Finally, the mean-square timing jitter (from Equation 2-20 squared) is found from the mean-square output noise (Equation 2-25) divided by the square of the signal slope (Equation 2-28 squared) and is given by

$$\sigma_t^2(t_{meas}) = \frac{\frac{1}{2\pi}\int_{-\infty}^{\infty} S_{in}(\omega)\,|G(\omega)|^2 d\omega}{\left[\frac{1}{2\pi}\int_{-\infty}^{\infty} j\omega\, V_{in}(\omega)G(\omega)\; e^{j\omega t_{meas}}\; d\omega\right]^2} \quad , \tag{2-29}$$

where t_{meas} is the measurement time (the time of the output-signal threshold crossing). In Equation 2-29, output-signal slope is assumed constant (as discussed for Equation 2-20) over the range of output noise about the threshold crossing. Additionally, the input noise, and correspondingly the output noise, is assumed to be symmetrically distributed (the noise would normally be Gaussian). Finally, the input, and correspondingly the output signal noise, is assumed to be stationary.

Douglass showed, by using the Schwarz integral inequality, that the timing jitter due to noise (Equation 2-29) is minimized when

$$G(\omega) = G_{opt}(\omega) = \frac{V_{in}^*(\omega)}{S_{in}(\omega)}(-j\omega)e^{-j\omega t_{meas}} \quad , \tag{2-30}$$

where $V_{in}{}^*(\omega)$ is the complex conjugate of the Fourier transform of the input signal [5]. An arbitrary filter gain for $G_{opt}(\omega)$ is not included in Equation 2-30 as filter gain affects both noise and signal slope equally and has no effect on timing jitter. The filter with response $G_{opt}(\omega)$ is the optimum filter for minimizing timing jitter due to noise for a given measurement time t_{meas}. Radeka and Karlovac derived a similar expression for the optimum filter for energy measurements where the signal-to-noise ratio is maximized for a given measurement time [6].

Douglass also showed that the optimum (minimum) timing jitter obtained with the optimum filter for timing ($G_{opt}(\omega)$) is given by

$$\sigma^2_{t\,(opt)} = \left[\frac{1}{2\pi} \int_{-\infty}^{\infty} \frac{|V_{in}(\omega)|^2}{S_{in}(\omega)} \omega^2 d\omega \right]^{-1} \quad [5]. \tag{2-31}$$

Note that the optimum level of timing jitter (Equation 2-31) is independent of the measurement time (t_{meas}) while the optimum filter for timing (Equation 2-30), required to obtain the optimum level of timing jitter, is dependent on the measurement time.

The optimum filter for timing, $G_{opt}(\omega)$, can be synthesized in two parts: a whitening filter, $G_{white}(\omega)$, which converts the input noise-power spectral density to a constant (white) spectrum, and a filter, $G_{matched}(\omega)$, which is a matched filter for the signal slope at the output of the whitening filter [5]. This synthesis procedure is illustrated in Figure 2-7 and is analogous to the synthesis procedure used for standard matched filters. This synthesis procedure is convenient to use since the whitening filter is a function only of the input noise and the matched filter is a function only of the signal present at the output of the whitening filter. Arbitrary filter gains will not be considered since, as discussed earlier, filter gain affects both noise and signal slope equally and has no effect on timing jitter.

The whitening filter, $G_{white}(\omega)$, is a function only of the input noise-power spectral density, $S_{in}(\omega)$, and is described by

$$|G_{white}(\omega)| = \left(\frac{1}{S_{in}(\omega)} \right)^{1/2} . \tag{2-32}$$

The Fourier transform of the signal present at the output of the whitening filter is given by

$$V_{white}(\omega) = V_{in}(\omega) G_{white}(\omega) \ , \tag{2-33}$$

where $V_{in}(\omega)$ is the Fourier transform of the input signal. The Fourier transform of the matched filter is a function only of the signal at the output of whitening filter and is given by

$$G_{matched}(\omega) = V^*_{white}(\omega)(-j\omega)e^{-j\omega t_{meas}} \ , \tag{2-34}$$

where $V_{white}{}^*(\omega)$ is the complex conjugate of the Fourier transform for the signal at the output of the whitening filter and t_{meas} is the measurement time. Finally, the optimum filter for timing is the product of the whitening filter and the matched filter as given by

$$G_{opt}(\omega) = G_{white}(\omega) G_{matched}(\omega) \quad . \tag{2-35}$$

The matched filter ($G_{matched}(\omega)$), described by Equation 2-34, consists of a term which is the complex conjugate of the Fourier transform for the signal slope at the whitening filter output, and a delay term for a time delay of t_{meas}. The corresponding impulse response of the matched filter is then equal to the time-reversed, whitening-filter output slope with a time delay of t_{meas}. This understanding of the matched filter is useful for the synthesis of optimum filters for timing [5].

Optimum Timing Filter for a Semiconductor Detector with Charge-Sensitive Preamplifier

Although the fully-monolithic CMOS CFD being developed in this work is for PET scintillation-detector applications, the optimal timing filter for a semiconductor and charge-sensitive preamplifier will be considered first to demonstrate that the optimal timing filter is not physically realizable for this widely used system. Optimal timing-filter analysis, however, is useful as it permits a comparison of system timing performance using realizable suboptimal filters to the theoretically optimal performance.

The optimum timing filter for a semiconductor detector connected to a charge-sensitive preamplifier has been considered by Douglass [5]. The Fourier transform representation of the input to the timing filter is given by

$$V_{in}(\omega) = \frac{Q}{C_F}\left(\frac{1}{j\omega\,(1+j\omega t_{signal})\,(1+j\omega t_{amp})}\right) , \tag{2-36}$$

where Q is the total charge collected in the preamplifier, C_F is the preamplifier feedback capacitance, t_{signal} is the time constant associated with the exponential charge collection in the detector, and t_{amp} is the time constant associated with the preamplifier bandwidth. The timing-filter input noise-power spectral density is given by

$$S_{in}(\omega) = \frac{e_n^2}{2}\left(\frac{1}{1+(\omega t_{amp})^2}\right) , \tag{2-37}$$

where e_n^2 is the single-sided (positive frequency only) value of the preamplifier input noise-power spectral density. The whitening-filter transfer function, $G_{white}(\omega)$, must cancel the

preamplifier pole associated with t_{amp} in order to compensate for the noise roll-off in $S_{in}(\omega)$. The transfer function for the whitening filter is then given by

$$G_{white}(\omega) = 1 + j\omega t_{amp} \quad . \tag{2-38}$$

The Fourier transform of the signal at the output of the whitening filter is the product of $V_{in}(\omega)$ and $G_{white}(\omega)$ and is given by

$$V_{white}(\omega) = \frac{Q}{C_F}\left(\frac{1}{j\omega\,(1 + j\omega t_{signal})}\right) \quad . \tag{2-39}$$

The time-domain signal at the output of the whitening filter is the inverse Fourier transform of Equation 2-39 and is given by

$$v_{white}(t) = \frac{Q}{C_F}\left(1 - e^{-t/t_{signal}}\right)u(t) \quad . \tag{2-40}$$

It is necessary to find the slope of the whitening-filter output signal, $v_{white}(t)$, in order to find the matched filter, $G_{match}(\omega)$. The slope of $v_{white}(t)$ is given by

$$\frac{d}{dt}v_{white}(t) = \frac{Q}{t_{signal}C_F}e^{-t/t_{signal}}\,u(t) \quad . \tag{2-41}$$

The impulse response for the matched filter is the time-reversed, whitening-filter output slope with a time delay t_{meas}. This impulse response is noncausal as it has value before the application of an impulse, and the matched filter described by this impulse response is not physically realizable. The matched-filter impulse response and its graphical derivation are shown in Figure 2-8. In addition to the matched filter ($G_{match}(\omega)$), the whitening filter ($G_{white}(\omega)$) is also nonrealizable as the whitening filter consists of a single zero with no corresponding pole.

Although the optimum filter for timing is not realizable for the semiconductor detector, charge-sensitive preamplifier example just discussed, it does provide a comparison for the performance of realizable filters [5]. From Equation 2-31, the theoretical optimum value for timing jitter is given by

$$\sigma^2_{t\,(opt)} = \left[\frac{C_F}{Q}\right]^2 e_n^2\, t_{signal} \quad , \tag{2-42}$$

for the semiconductor, charge-sensitive preamplifier considered [5]. Using simple single-pole lowpass, single-pole highpass, and combined highpass-lowpass filters, Douglass reported theoretical and experimental values of timing jitter (σ_t) 30 - 40% higher than the theoretical minimum value [5].

Optimum Timing Filter for a Step Input in White Noise

In the previous optimum timing-filter example, the input signal was bandlimited (described with time constant t_{signal}) by semiconductor-detector charge collection. Consider now the optimum timing filter for a step input in the presence of white noise as an example of a signal that is not bandlimited. No whitening filter is required for this case as the input noise is already white noise, thus $G_{white}(\omega)$ is equal to a constant and the output of the whitening filter is a step signal, being equal to the input. The whitening-filter output slope is required to determine the impulse response of the matched filter, and this slope is a delta function having strength equal to the step signal transition. The impulse response of the matched filter ($G_{match}(\omega)$) is then the time-reversed, whitening-filter output-signal slope with a time delay of t_{meas}. Since a time-reversed delta function is also a delta function, the matched filter impulse response is a delta function of strength equal to the step signal transition with delay t_{meas} as shown in the graphical derivation of Figure 2-9. Thus the matched filter described by the derived impulse response has infinite bandwidth and a delay equal to t_{meas}. The total optimum filter ($G_{opt}(\omega)$) consists of the whitening filter and the matched filter, yielding a composite filter of infinite bandwidth with delay t_{meas}. The delay simply ensures that the filtered signal is delayed to the desired measurement time so that the time measurement occurs on the output-step transition edge.

Although both the whitening filter and the matched filter have causal impulse responses, each filter is of course nonrealizable because of its infinite bandwidth. The optimum timing filter derived implies that timing-filter bandwidth should be maximized to the extent possible for a step input in the presence of white noise. As mentioned earlier, bandwidth should be maximized for nonbandlimited inputs in white noise because signal slope increases directly with bandwidth while circuit noise voltage (or current) increases only as the square root of bandwidth. The resulting timing jitter decreases as the inverse square root of increasing bandwidth. In all cases, however, circuit bandwidth must be

limited so noise does not exceed the step signal level as this is required to permit comparator triggering on the step signal.

Optimum Timing Filter for a Bandlimited Input in Bandlimited Noise

Consider a step input and white noise that are both bandlimited by front-end amplification in a system. Such a system is typical of photomultiplier scintillation-detector systems where the step input represents photomultiplier photoelectron current resulting from instantaneous light output from the scintillator after a detected event, and bandwidth limiting models finite photomultiplier-tube and front-end-amplifier circuit bandwidth. White input noise is typical for such systems when voltage-sensitive amplifier circuits are used to amplify the voltage appearing across a termination resistor at the photomultiplier output. In such systems, the signal and noise reaching the timing filter are equally bandlimited by the front-end circuits. For the purposes of this discussion, single-pole lowpass filtering (with unity gain) of the step input and white noise will be assumed.

The Fourier transform of the input signal (at the timing filter) is given by

$$V_{in}(\omega) = V_{inpk}\left(\frac{1}{j\omega\,(1+j\omega t_{amp})}\right) , \tag{2-43}$$

where V_{inpk} is the final value of the step input, and t_{amp} is the time constant associated with the single-pole lowpass front-end circuitry. The input noise-power spectral density (at the timing filter) is given by

$$S_{in}(\omega) = \frac{e_n^2}{2}\left(\frac{1}{1+(\omega t_{amp})^2}\right) , \tag{2-44}$$

where e_n^2 is the single-sided (positive frequency only) noise-power spectral density at the input of the front-end circuitry.

The whitening filter must consist of a zero to cancel the front-end-circuitry pole in order to shape the noise into white noise. The whitening filter transfer function is given by

$$G_{white}(\omega) = 1 + j\omega t_{amp} \ . \tag{2-45}$$

The output signal from the whitening filter is then a step input as the single-pole bandwidth limit on the input signal has been canceled as described by the Fourier representation of the whitening filter output,

$$V_{white}(\omega) = V_{inpk}\left(\frac{1}{j\omega\,(1+j\omega t_{amp})}\right)(1+j\omega t_{amp}) \quad , \text{or} \tag{2-46}$$

$$V_{white}(\omega) = V_{inpk}\left(\frac{1}{j\omega}\right) \quad . \tag{2-47}$$

From the preceding optimum timing-filter example, it was shown that the matched filter for a step input is a circuit of infinite bandwidth having delay t_{meas}. The complete optimum timing filter is then the whitening filter and the matched filter yielding a composite filter consisting of a zero to cancel the input-signal noise pole and a delay of t_{meas}. Such a circuit is, again, nonrealizable as it contains no bandlimiting poles. Additionally, this filter contains a zero without an associated pole which is also nonrealizable. The graphical derivation of this optimum filter for timing is illustrated in Figure 2-10.

Suboptimal Timing Filter for a Bandlimited Input in Bandlimited Noise

Although the optimum timing filter just considered for the bandlimited step input in bandlimited noise is unrealizable, the analysis does give insight into a suboptimal, realizable timing emphasis filter. The timing emphasis filter considered contains a zero to cancel the pole associated with the front-end bandlimiting circuitry, but unlike the theoretical optimum-timing filter, contains a pole at a frequency location higher than the zero making it physically realizable. The timing emphasis filter considered here is a pole-zero compensation filter that effectively raises the bandwidth of front-end circuitry to a bandwidth determined by the pole location in the emphasis filter.

The Fourier transform of the emphasis filter output is the Fourier transform of the input signal multiplied by the emphasis filter response and is given by

$$V_{emphasis}(\omega) = V_{inpk}\left(\frac{1}{j\omega\,(1+j\omega t_{amp})}\right)G_{emphasis}(\omega) \quad , \tag{2-48}$$

where the emphasis filter response is given by

$$G_{emphasis}(\omega) = \left(\frac{1 + j\omega t_{amp}}{j\omega \, (1 + j\omega t_{emphasis})} \right) , \tag{2-49}$$

where $t_{emphasis}$ is the time constant associated with the emphasis-filter pole. The resultant output of the emphasis filter, in Fourier notation, is given by

$$V_{emphasis}(\omega) = V_{inpk} \left(\frac{1}{j\omega \, (1 + j\omega t_{emphasis})} \right) , \tag{2-50}$$

which corresponds in the time domain to an exponential rise to V_{inpk} with time constant $t_{emphasis}$. The output signal of the emphasis filter is identical to its input signal except the input time constant, t_{amp}, is replaced by the emphasis-filter time constant, $t_{emphasis}$.

The output noise-power spectral density for the emphasis filter is identical to the input noise-power spectral density with the input time constant, t_{amp}, again replaced by the emphasis-filter time constant, $t_{emphasis}$. The emphasis-filter-output noise-power spectral density is given by

$$S_{emphasis}(\omega) = \frac{e_n^2}{2} \left(\frac{1}{1 + (\omega t_{emphasis})^2} \right) . \tag{2-51}$$

An improvement in timing jitter is present using the emphasis filter because the filter output-signal slope increases directly with increased bandwidth while the noise increases as the square root of increasing bandwidth, so the total timing jitter (σ_t) decreases as the inverse square root of increasing bandwidth. This is illustrated by evaluating the timing jitter as a function of the circuit time constant.

As mentioned, the output signal from the emphasis filter is an exponential rise in the time domain with time constant $t_{emphasis}$. The output signal is given by

$$v_{emphasis}(t) = V_{inpk} \left(1 - e^{-t/t_{emphasis}} \right) u(t) , \tag{2-52}$$

where V_{inpk}, as mentioned earlier, is the final value of the step input before the bandlimiting filter and is also the final value of the emphasis-filter input signal (unity gain is assumed for the bandlimiting and emphasis filters as described earlier). The slope of the output signal from the emphasis filter is given by

$$\frac{d}{dt} v_{emphasis}(t) = \frac{V_{inpk}}{t_{emphasis}} \left(e^{-t/t_{emphasis}} \right) u(t) \quad , \tag{2-53}$$

which has maximum value at the beginning of the signal ($t = 0$) given by

$$K_{pk} = \frac{V_{inpk}}{t_{emphasis}} \quad . \tag{2-54}$$

The emphasis-filter mean-square output noise from Equation 2-25, using the output noise-power spectral density given by Equation 2-51, is given by

$$e_{out}^2 = \sigma_v^2 = \frac{1}{2\pi} \frac{e_n^2}{2} \int_{-\infty}^{\infty} \left(\frac{1}{1 + (\omega t_{emphasis})^2} \right) d\omega \quad , \tag{2-55}$$

which is equal to

$$e_{out}^2 = \sigma_v^2 = \frac{e_n^2}{4 t_{emphasis}} \quad , \tag{2-56}$$

where e_n^2 is the (single-sided) noise-power spectral density of the white noise present before the bandlimiting filter. Finally, the timing jitter at the output of the emphasis filter is given by

$$\sigma_t^2 (t = 0) = \frac{\sigma_v^2}{K_{pk}^2} \quad , \text{or} \tag{2-57}$$

$$\sigma_t^2 (t = 0) = \frac{\dfrac{e_n^2}{4 t_{emphasis}}}{\left[\dfrac{V_{inpk}}{t_{emphasis}} \right]^2} \quad . \tag{2-58}$$

Solving Equation 2-58 for σ_t gives

$$\sigma_t(t=0) = \frac{e_n\sqrt{t_{emphasis}}}{2V_{inpk}} \quad , \tag{2-59}$$

which is the timing jitter (rms) for a threshold crossing at the beginning of the output-signal transition (t = 0) where the signal slope is maximum.

Equation 2-59 illustrates that the timing jitter goes as the square root of the single-pole time constant or as the inverse square root of the single-pole bandwidth. If the pole-zero emphasis filter effectively increases the front-end bandwidth a factor-of-ten, then from Equation 2-59, the noise jitter will decrease by a factor of $\sqrt{10}$. Using an emphasis filter to increase the front-end bandwidth of a scintillation-detector signal may also permit triggering on the first photoelectron, as the increased bandwidth would better separate the individual photomultiplier-tube photoelectron impulses (first-photoelectron timing is discussed in *Section 3*). Practical issues, such as photomultiplier tube impulse-response ringing, will limit the degree of bandwidth emphasis that is possible in practical circuits. Emphasizing front-end bandwidth would have to be compared with lowering the timing threshold as a potential technique for first-photoelectron timing with scintillation detectors.

Optimum Timing Filter for a Linear-Edge Input in White Noise

The final timing filter considered is for linear-edge input signals in the presence of white noise. Although linear-edge input signals are not characteristic of scintillation-detector signals, linear-edge signals are present in coaxial semiconductor detectors for detector interactions occurring near the center of the depletion region [7, 8, 9]. It will be shown that, unlike the other filters presented, the optimum timing filter for linear-edge input signals in the presence of white noise is physically realizable. The performance of the optimum timing filter will then be compared to the performance of a simple single-pole lowpass timing filter.

The optimum timing filter is derived graphically as shown in Figure 2-11 for linear-edge input signals having rise-times of t_r. Since the input signal is in the presence of white noise, no noise shaping is required by the whitening filter. The slope for the linear-edge signal at the output of the whitening filter is a rectangular pulse signal having height equal to the linear-edge input-signal slope and width equal to the input-signal rise-time. Since the input-signal transition occurs before the reference time (t = 0), the time-reversed whitening-filter output-signal slope is causal as shown in Figure 2-11 for positive measurement times (t_{meas}). The time-reversed signal slope at the output of the whitening filter is, of course, the impulse response for the matched filter. This filter operates by taking the difference between the input signal and the input signal delayed by t_r. This difference is then fed into

an integrator as can be observed from the matched-filter impulse response. The complete optimum timing filter, consisting of the whitening filter (which has constant frequency response) and the matched filter, is described by Fourier notation as

$$G_{opt}(\omega) = \left(1 - e^{-j\omega t_r}\right)\left(\frac{1}{j\omega}\right) . \tag{2-60}$$

The response of the optimum timing filter for linear-edge input signals is shown graphically in Figure 2-12. Note that the peak value of output-signal slope occurs at the measurement time equal to zero, which corresponds to the end of the input-signal linear-edge transition (the measurement time (t_{meas}) as shown in Figures 2-11 and 2-12). The peak value of output-signal slope is equal to the input amplitude of the signal (V_{inpk}) and is independent of the input-signal rise-time. As the output-signal slope is known, it is now only necessary to find the noise at the output of the filter to evaluate the timing jitter performance.

The noise at the output of the timing filter is found from Equation 2-25 for a single-sided input-noise-power spectral density of e_n^2 and is given by

$$e_{out}^2 = \sigma_v^2 = \frac{1}{2\pi}\frac{e_n^2}{2}\int_{-\infty}^{\infty} G_{opt}(\omega)G_{opt}^*(\omega)d\omega \quad , \text{or} \tag{2-61}$$

$$e_{out}^2 = \sigma_v^2 = \frac{1}{2\pi}\frac{e_n^2}{2}\int_{-\infty}^{\infty} \frac{2(1-\cos\omega t_r)}{\omega^2} d\omega \quad , \text{or} \tag{2-62}$$

$$e_{out}^2 = \sigma_v^2 = \frac{e_n^2 t_r}{2} . \tag{2-63}$$

The output timing jitter σ_t is then given by the output noise divided by the signal slope at the measurement time. The output timing jitter is given by

$$\sigma_t(t = t_{end\ of\ input\ transition}) = \frac{\sqrt{\frac{e_n^2 t_r}{2}}}{V_{inpk}} \quad , \text{or} \tag{2-64}$$

$$\sigma_t(t = t_{end\ of\ input\ transition}) = \frac{e_n\sqrt{t_r}}{\sqrt{2}V_{inpk}} \quad , \tag{2-65}$$

where the timing crossing occurs at the peak value of the output-signal slope which corresponds to the end of the linear-edge input-signal transition. The timing jitter (Equation 2-65) for the optimal timing filter for linear-edge input signals in white noise is proportional to the square root of the input-signal rise-time

It is interesting to compare the timing jitter performance of the optimum timing filter for linear-edge input signals in white noise with the timing jitter performance of a simple suboptimal timing filter. The suboptimal timing filter that will be considered is a single-pole lowpass filter. It can be shown that the output-signal slope of this filter is maximum at time corresponding to the end of the input-signal linear-edge transition (measurement time (t_{meas}) equal to zero as shown in Figure 2-11) and that the peak output-signal slope is given by

$$\frac{d}{dt}v_{lowpass}(t = t_{end\ of\ input\ transition}) = \frac{V_{inpk}}{t_r}\left(1 - e^{-t_r/t_{lp}}\right) \quad , \tag{2-66}$$

where V_{inpk} is the input signal level, t_r is the linear-edge input rise-time, and t_{lp} is the lowpass-filter time constant. The peak output-signal slope approaches a maximum value, the input-signal slope, for a lowpass-filter time constant much less than the input signal rise-time.

The mean-square output noise of the single-pole lowpass filter for a white noise input can be taken from Equations 2-55 and 2-56 and is given by

$$e_{out}^2 = \sigma_v^2 = \frac{e_n^2}{4t_{lp}} \quad , \tag{2-67}$$

where $e_n{}^2$ is the single-sided input noise-power spectral density. The output timing jitter of the single-pole lowpass filter is then given by the output noise divided by the peak output-signal slope as described by

$$\sigma_t(t = t_{end\ of\ input\ transition}) = \frac{\frac{e_n}{2\sqrt{t_{lp}}}}{\frac{V_{inpk}}{t_r}\left(1 - e^{-t_r/t_{lp}}\right)} \quad , \text{or} \tag{2-68}$$

$$\sigma_t(t = t_{end\ of\ input\ transition}) = \frac{e_n t_r}{2V_{inpk}\sqrt{t_{lp}}\left(1 - e^{-t_r/t_{lp}}\right)} \quad . \tag{2-69}$$

The lowpass-filter timing jitter (σ_t) (Equation 2-69) is divided by the optimum-timing-filter timing jitter (Equation 2-65) and is plotted in Figure 2-13 as a function of the lowpass-filter time constant divided by the input-signal rise-time (t_{lp}/t_r). The minimum value of timing jitter for the lowpass filter occurs for $t_{lp} = 0.79t_r$ and is only 10.8% higher than the timing jitter for the optimum timing filter. The optimum value of lowpass-filter time constant relative to the input-signal rise-time represents a balance between a short time constant to preserve the input-signal slope and a long time constant to minimize output noise.

It is interesting to observe that the timing jitter of a single-pole lowpass filter with linear-edge input signals in white noise is only 10.8% higher than the theoretical minimum, whereas the timing jitter of a single-pole lowpass filter with exponential-rise input signals in bandlimited noise (the noise and signal time constants being different) is 30% higher than the theoretical minimum as described by Douglass [5]. Additionally, it is interesting to note that the optimum filter for timing is physically realizable for linear-edge input-signals in white noise but is not physically realizable for exponential-rise input-signals in bandlimited noise. Both linear-edge and exponential-rise signals are present in coaxial semiconductor detectors, the signal shapes depending on event interaction location and the resulting detector charge collection [7, 8, 9].

The optimum timing filter described for linear-edge input signals in the presence of white noise is physically realizable with some error because a perfect integrator is not realizable. This implementation error can be made quite small for signal rise-times much shorter than the single-pole time constant of a realizable lowpass filter acting as an integrator. However, there is a practical difficulty in using a nongated integrator circuit since the output can reach circuit saturation levels as no integrator reset is provided. Thus,

the optimum timing filter described would best be implemented as a gated integrator which is a time-variant filter.

The optimum timing-filter examples considered have been for the case of white or lowpass-filtered noise at the timing-filter input. These cases are representative of charge-sensitive preamplifiers where preamplifier output noise has lowpass characteristics and voltage-sensitive preamplifiers where preamplifier output noise has lowpass characteristics or white characteristics for the frequencies of interest. The case of current-sensitive (transimpedance) preamplifiers, however, was not considered. In this case, preamplifier output-noise density increases with frequency (ω^2 noise power) over a significant range of frequency. Recently, Binkley et al. reported a monolithic CMOS transimpedance preamplifier for PET BGO/avalanche-photodiode detector applications [10]. In these applications, unlike BGO/photomultiplier detector applications where detector statistical noise is dominant, timing jitter is the dominant source of system timing errors. The study of optimal timing filters for PET BGO/avalanche-photodiode detector applications should be considered for both transimpedance and charge-sensitive preamplifiers.

Time-Variant Filters for Timing

Time variant filters for timing are discussed by Douglass and can offer advantages over time-invariant filters [5]. Time variant filters often have a noise advantage as their output noise starts accumulating only after the filter is gated on. Thus, if the filter has been gated on for a short time, the output noise level may be considerably less than the steady-state output noise present for a time-invariant filter. This may permit the use of a lower timing threshold, the timing threshold being required to be above the noise [5]. A lower timing threshold lowers the walk effects in a leading-edge discriminator and also lowers CFD walk effects due to nonconstant signal shape. Additionally, a lower timing threshold may permit single-photon timing. Time-variant filters may also have considerably lower timing jitter compared to time-invariant filters for measurements times near the start of the input signal [5]. Again, this is particularly true if the time-variant filter has been gated on for a short period of time.

Time variant filters are widely used in nuclear instrumentation for energy measurements but are rarely used for timing measurements. This is because time-variant energy measurements are usually started (gated) from the output of a timing circuit. Time-variant timing systems, in contrast, must be started *before* the timing measurement is made which requires a high-sensitivity discriminator to gate the filters *before* the timing measurement is derived. Time variant filters, however, should be seriously considered for

systems where timing performance is limited by circuit noise. Time variant filters will not be discussed further in this work but further discussions are available in the literature [5, 11, 12, 13, 14].

Time Drifts Due to Temperature and Aging Effects

System timing drifts are caused by changing system time delay with temperature and aging. One component of system time delay is circuit propagation delay which is a function of signal amplitude, signal rise-time, discriminator threshold, and internal circuit delays. Another component is detector timing delay.

The input stage of most logic timing devices is effectively a leading-edge discriminator. Leading-edge timing drift can be found from the leading-edge discriminator propagation-delay function which is given by (as given in Equation 2-1)

$$t_{prop} = \frac{V_T t_r}{V_{inpk}} \quad , \tag{2-70}$$

where t_r is the linear-edge signal rise-time, V_{inpk} is the signal transition amplitude, and V_T is the discriminator threshold (referenced to the initial signal level). Equation 2-70 predicts a time drift of -5.18 ps/°C for an ECL (emitter-coupled logic) signal with a 2-ns rise-time, 0.85-V signal swing, and 0.425-V threshold (referenced to the initial signal level) which drifts -2.2 mV/°C. The threshold drift assumed in this example is the voltage drift associated with a silicon-diode junction. The same timing drift would occur if the initial signal level or baseline drifted +2.2 mV/°C with the threshold voltage held constant illustrating an effective change in threshold with signal baseline level.

In addition to leading-edge discriminator time drifts, time drifts are also caused by changes in internal circuit propagation delay. The specified propagation-delay temperature drift for the ECL 10K logic family is 2 ps/°C typical and 7 ps/°C maximum [15]. The specified propagation-delay temperature drift for the ECL 10KH logic family, with its improved rise-time and delay characteristics, is 0.5 ps/°C typical and 4 ps/°C maximum [15].

Reported circuit timing drift with temperature is typically in the low ps/°C range for modern, high-performance, bipolar timing discriminators, with a reported timing drift of only 0.3 ps/°C for one CFD design [7]. Such low levels of timing drift are not required for commercial PET BGO scintillation-detector timing systems as system timing resolution is approximately 3 ns FWHM [2].

Scintillation-detector timing drifts with temperature are caused by changes in scintillation light output and decay time constant. Additional temperature-induced timing drifts are caused by changes in photomultiplier cathode quantum efficiency, photomultiplier gain, and photomultiplier transit-time. The mechanisms of timing errors in scintillation detectors will be discussed in detail in *Section 3*.

Time drift due to circuit and detector aging effects is evaluated in the same manner as temperature-induced drifts. Signal amplitude, signal rise-time, discriminator threshold, and internal circuit delays can change with age. The gain of photomultiplier tubes used in scintillation detectors can change significantly with age, which necessitates the use of variable-gain front-end amplifiers in modern commercial PET systems.

References for Section 2

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Appendix for Section 2 — Figures

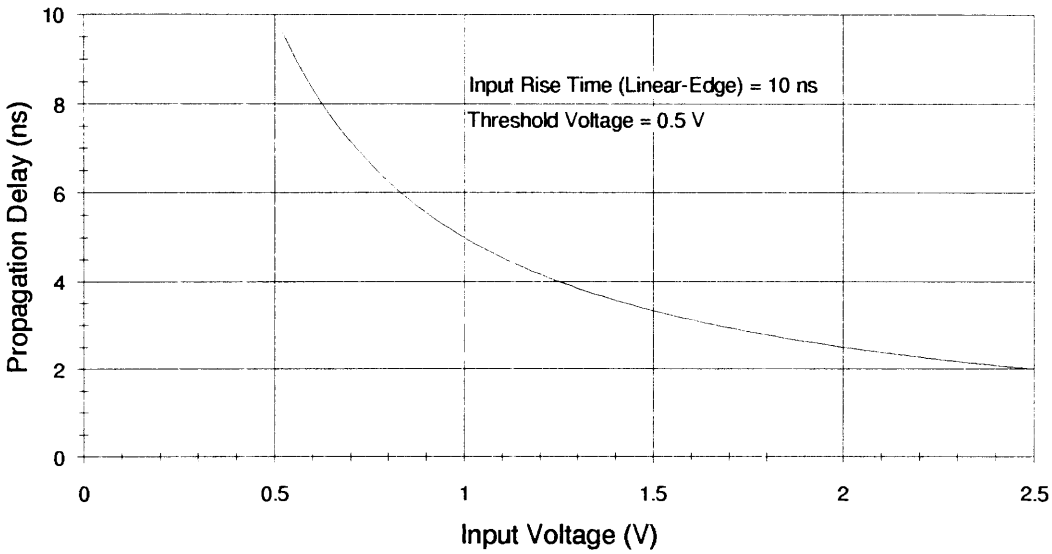


Figure 2-1. Propagation Delay of an Ideal Leading-Edge Discriminator.

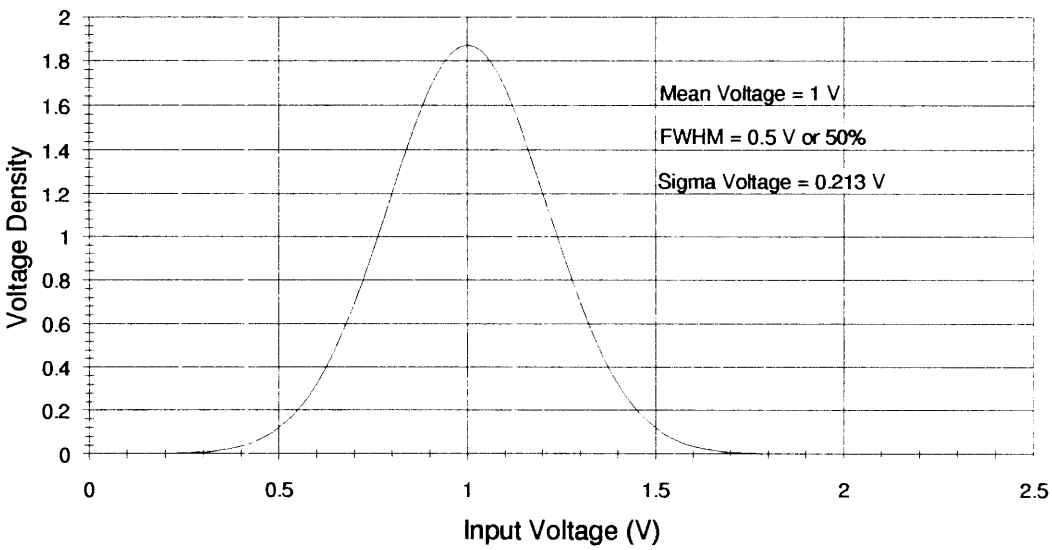


Figure 2-2. Input Voltage Spectrum Considered for an Ideal Leading-Edge Discriminator.

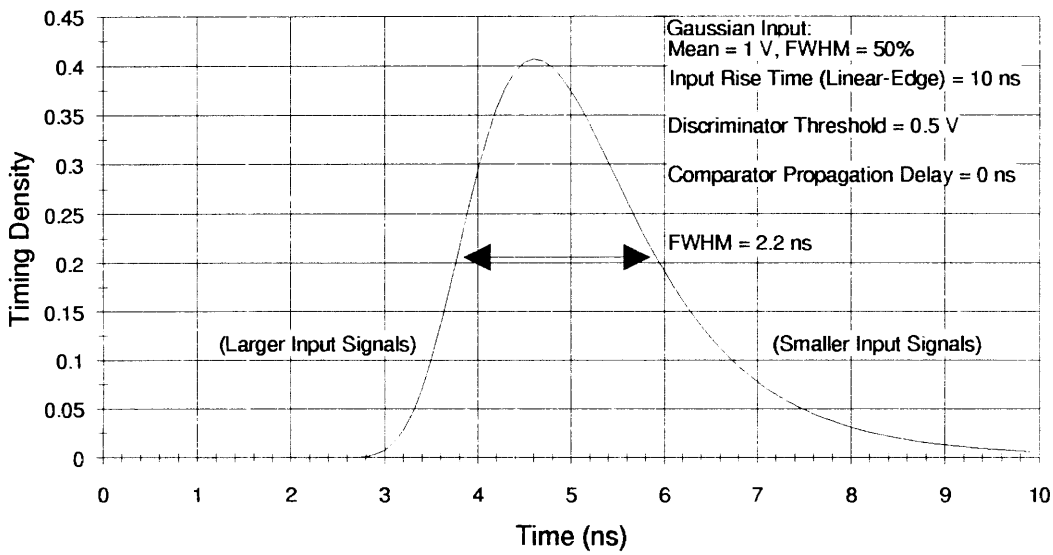


Figure 2-3. Timing Spectrum for an Ideal Leading-Edge Discriminator.

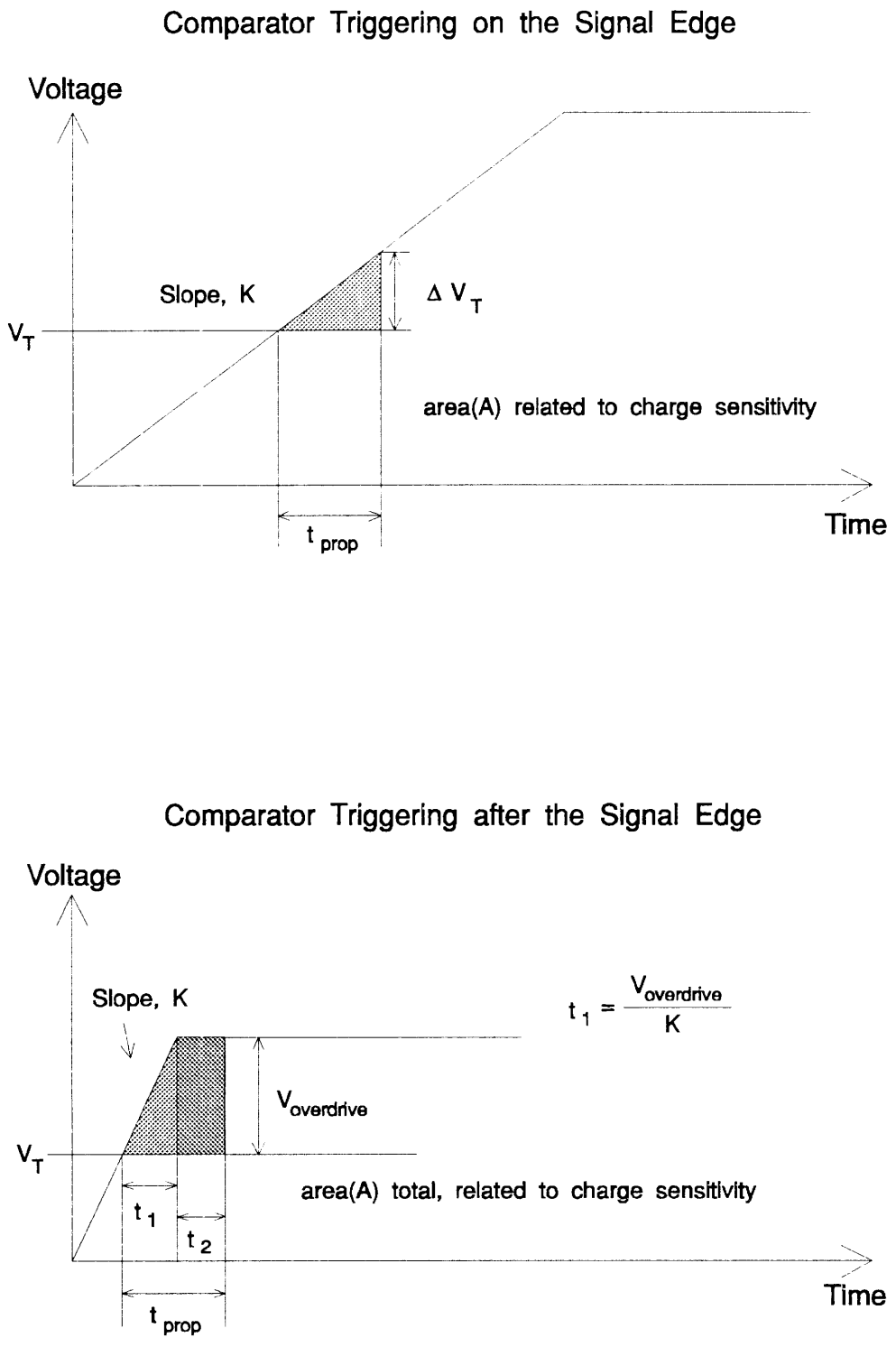


Figure 2-4. Illustration of Comparator Charge Sensitivity.

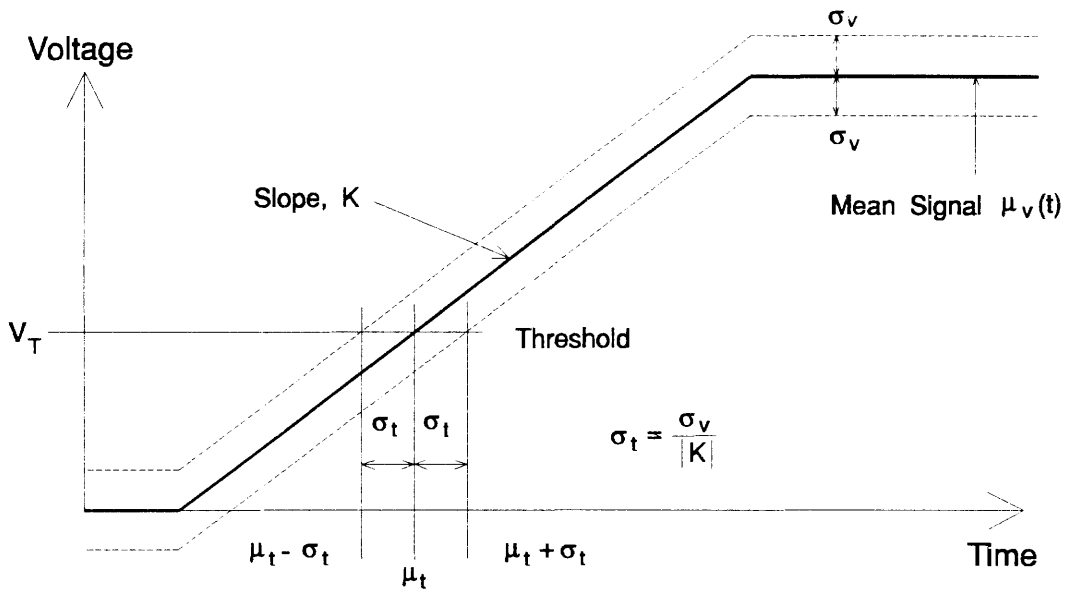


Figure 2-5. Illustration of Timing Jitter Due to Noise.

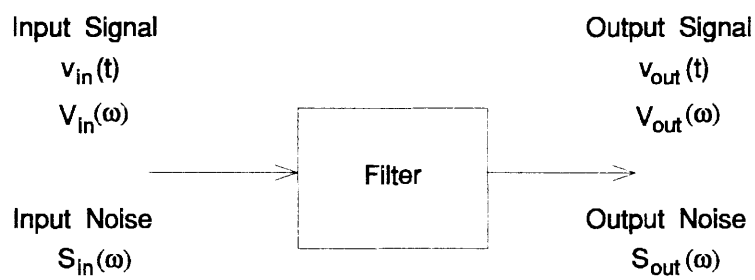
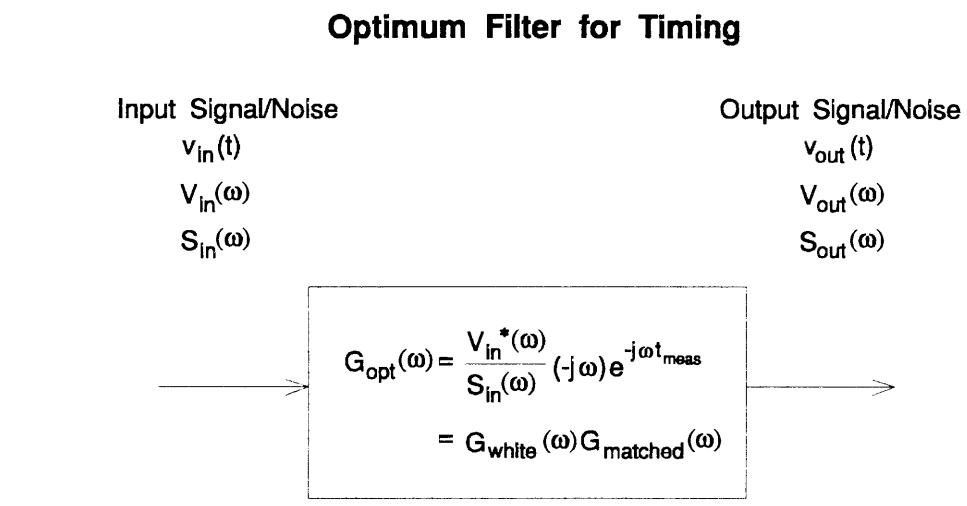


Figure 2-6. Illustration of Filter Used to Minimize Timing Jitter.



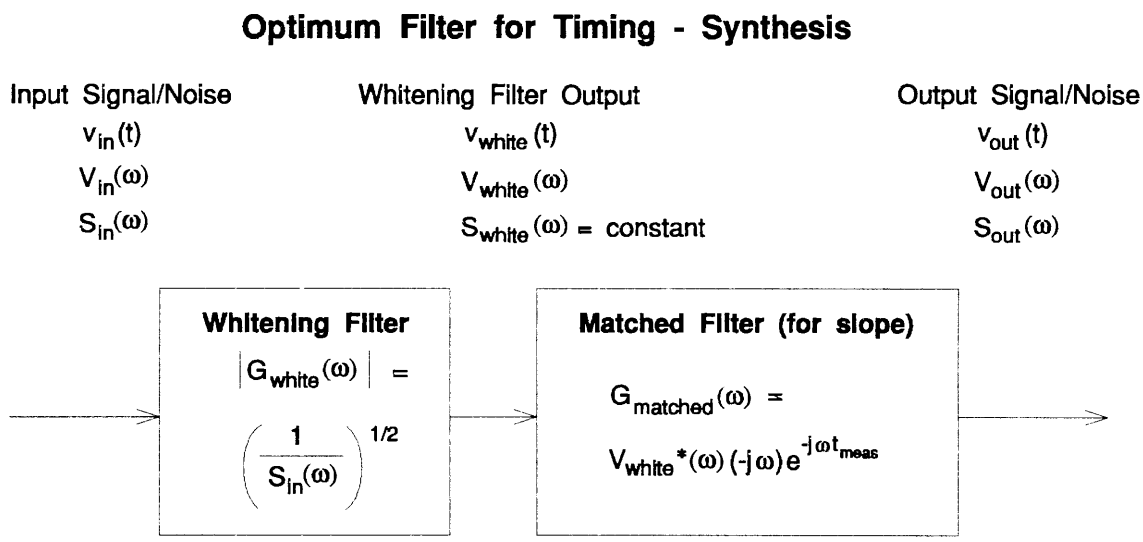


Figure 2-7. Synthesis of the Optimum Filter for Timing.

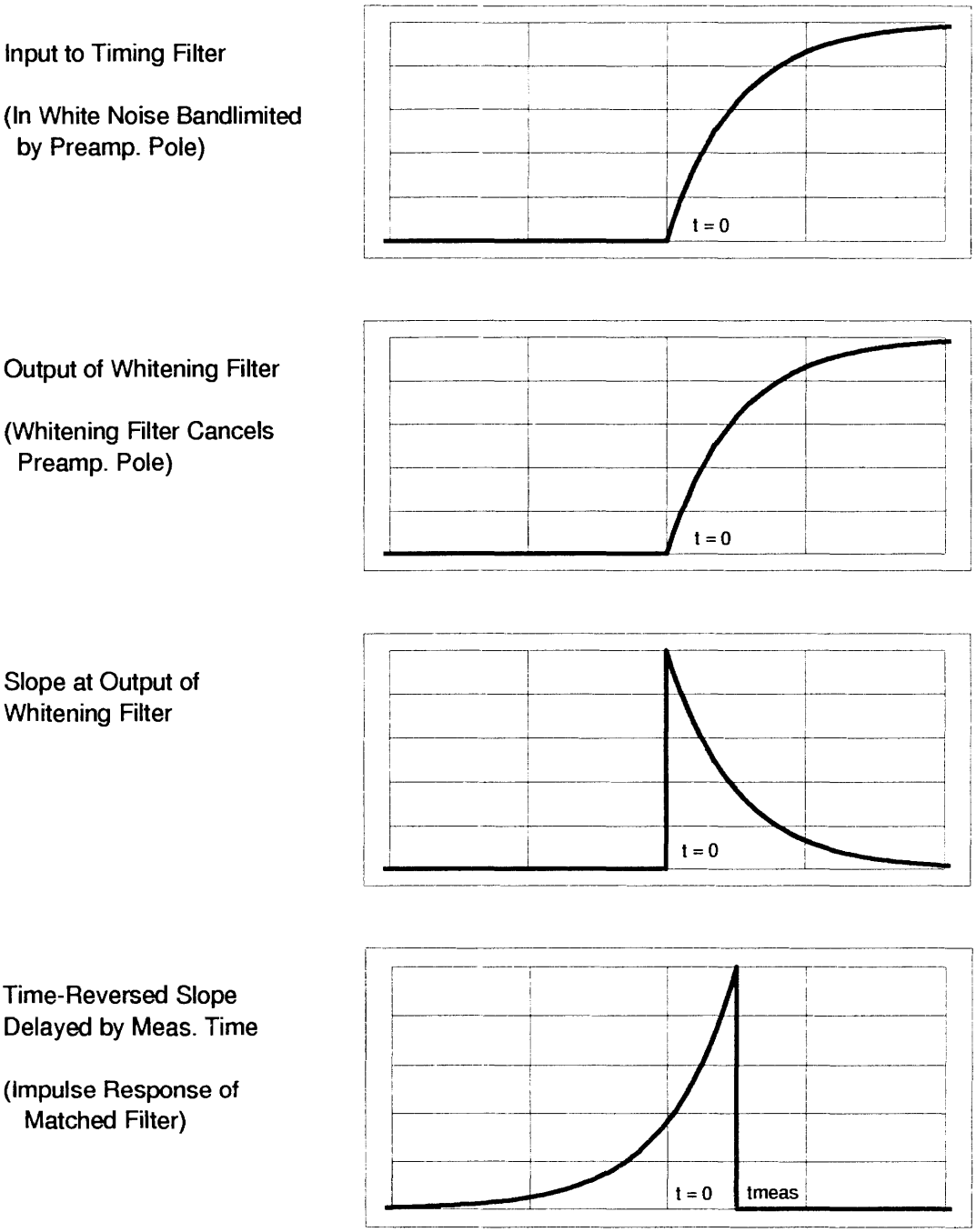


Figure 2-8. Illustration of the Optimum Timing Filter for a Semiconductor Detector and Charge-Sensitive Preamplifier.

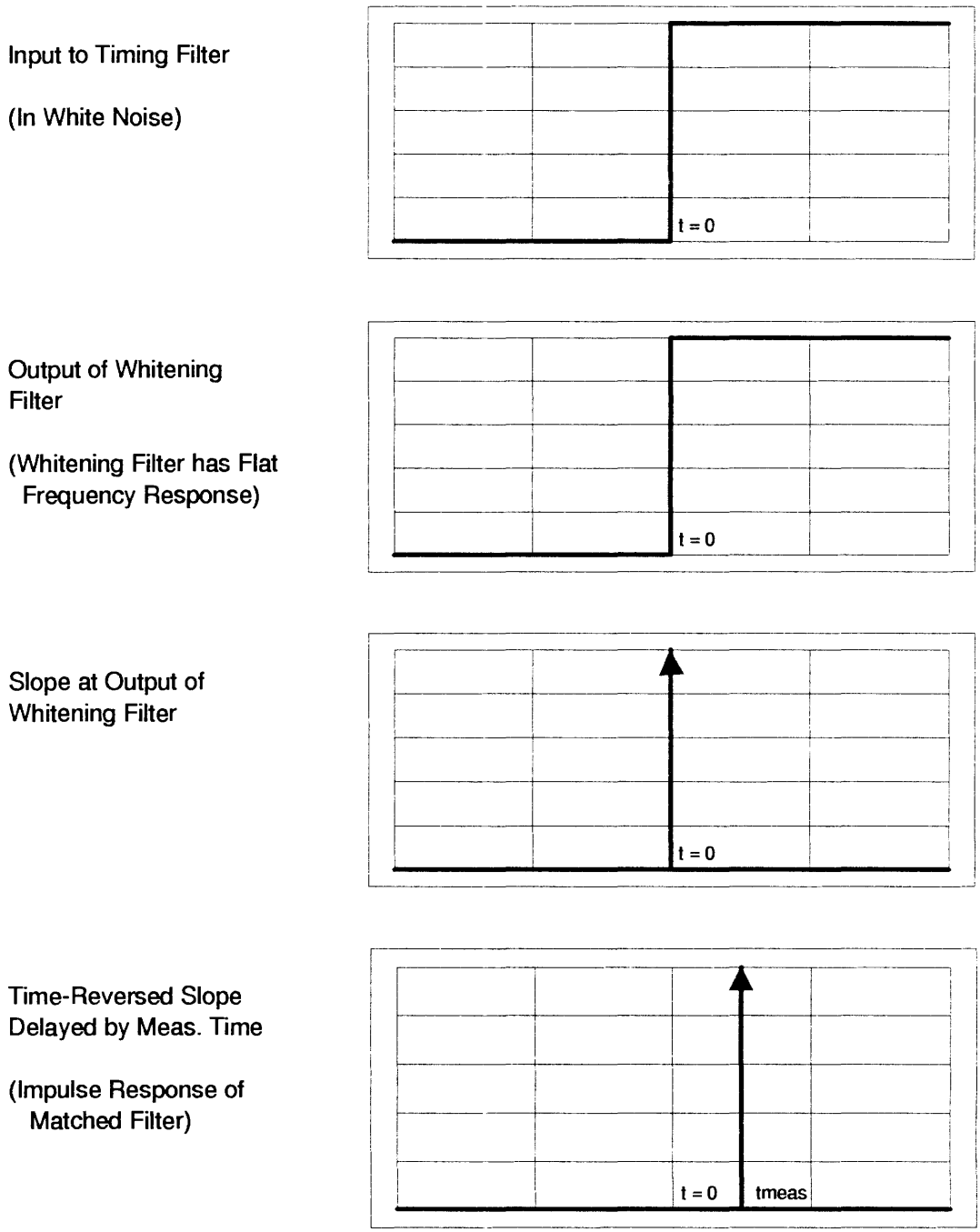
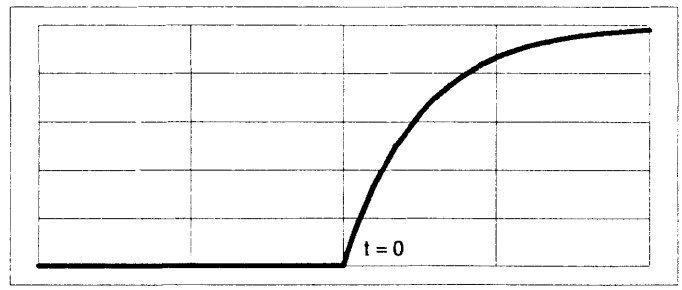


Figure 2-9. Illustration of the Optimum Timing Filter for a Step Input in White Noise.

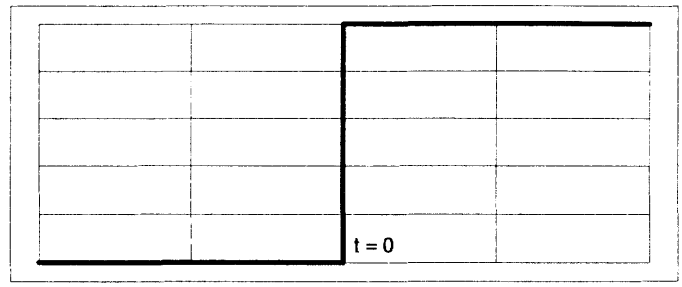
Input to Timing Filter

(Signal and Noise are Bandlimited)

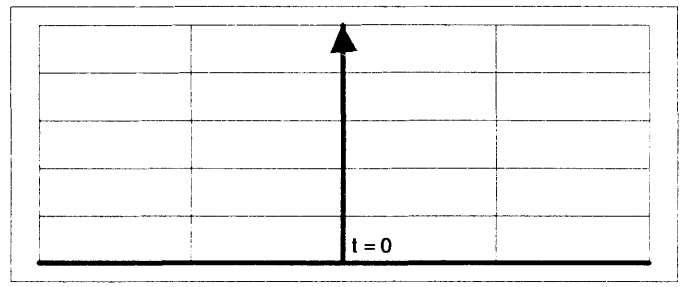


Output of Whitening Filter

(Whitening Filter Cancels the Bandlimiting Pole)

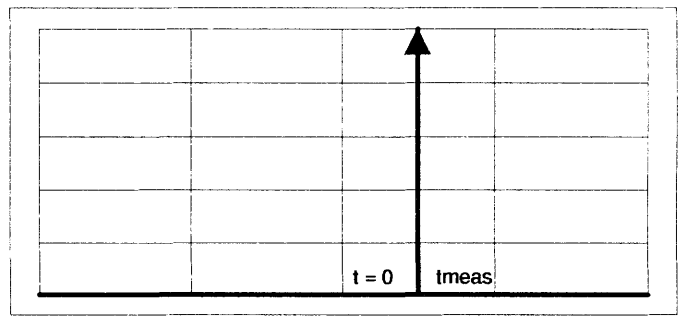


Slope at Output of Whitening Filter



Time-Reversed Slope Delayed by Meas. Time

(Impulse Response of Matched Filter)



Voltage Verses Time (Arbitrary Units)

Figure 2-10. Illustration of the Optimum Timing Filter for a Bandlimited Step Input in Bandlimited Noise.

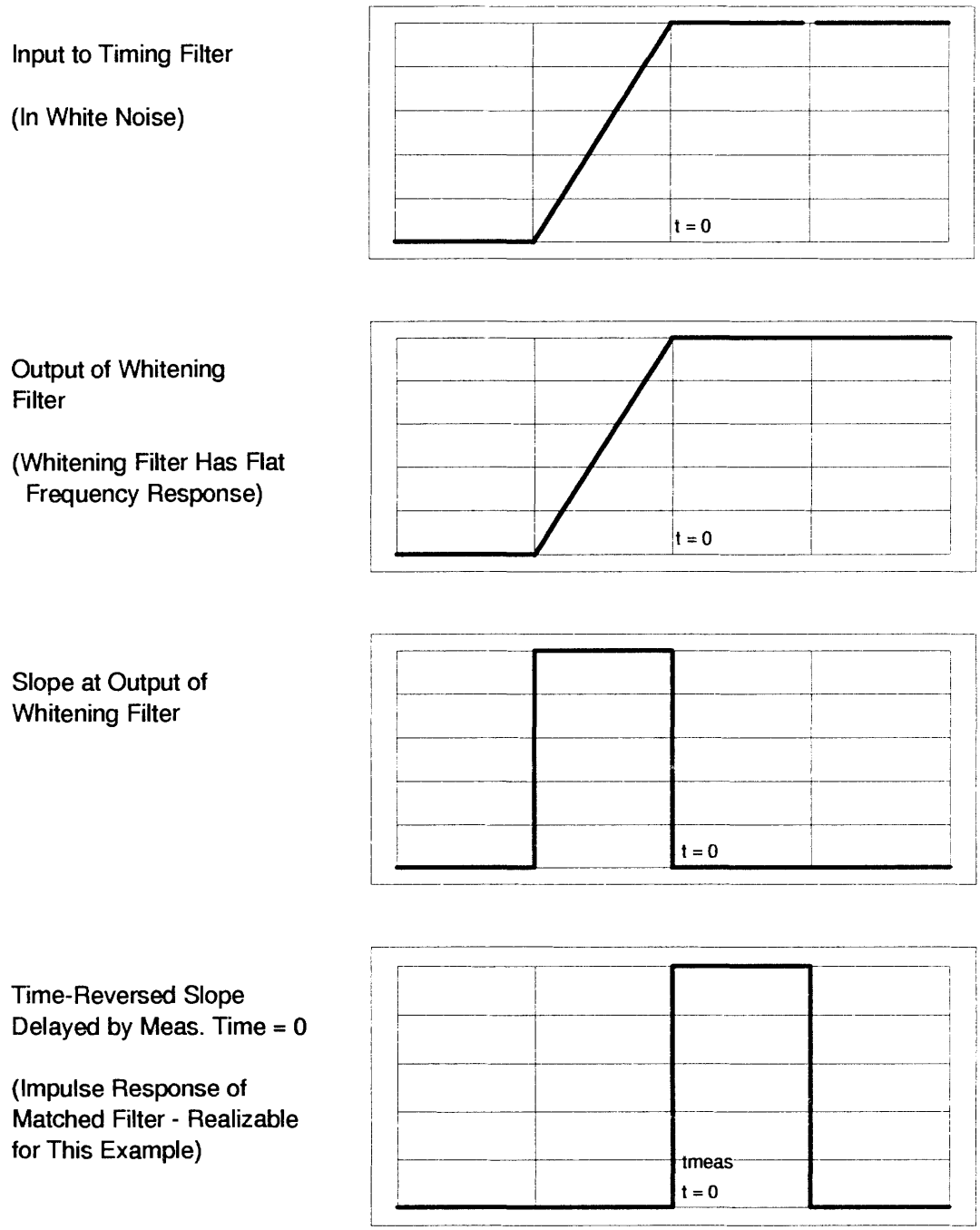


Figure 2-11. Illustration of the Optimum Timing Filter for a Linear-Edge Input in White Noise.

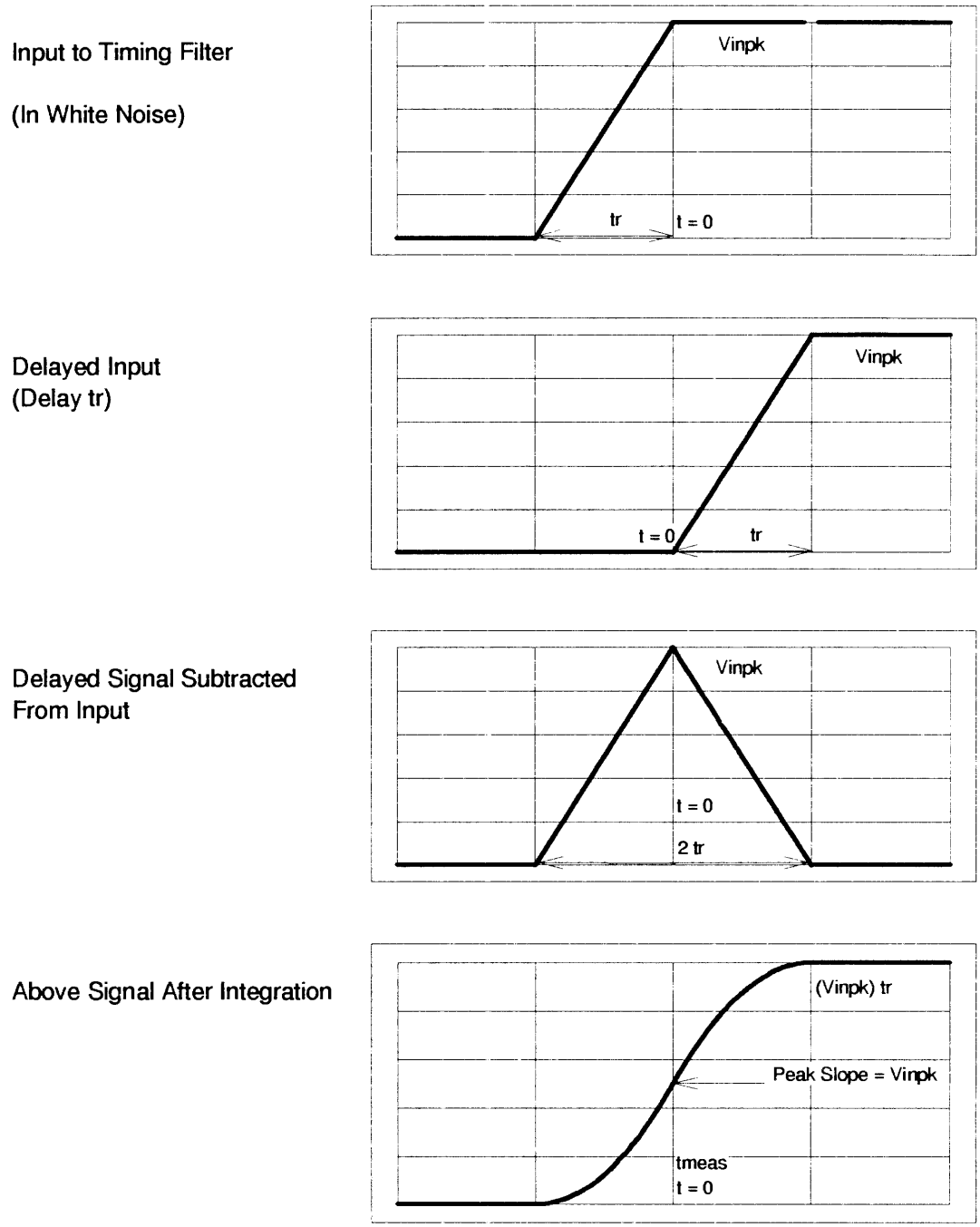


Figure 2-12. Illustration of Signals for the Optimum Timing Filter for a Linear-Edge Input in White Noise.

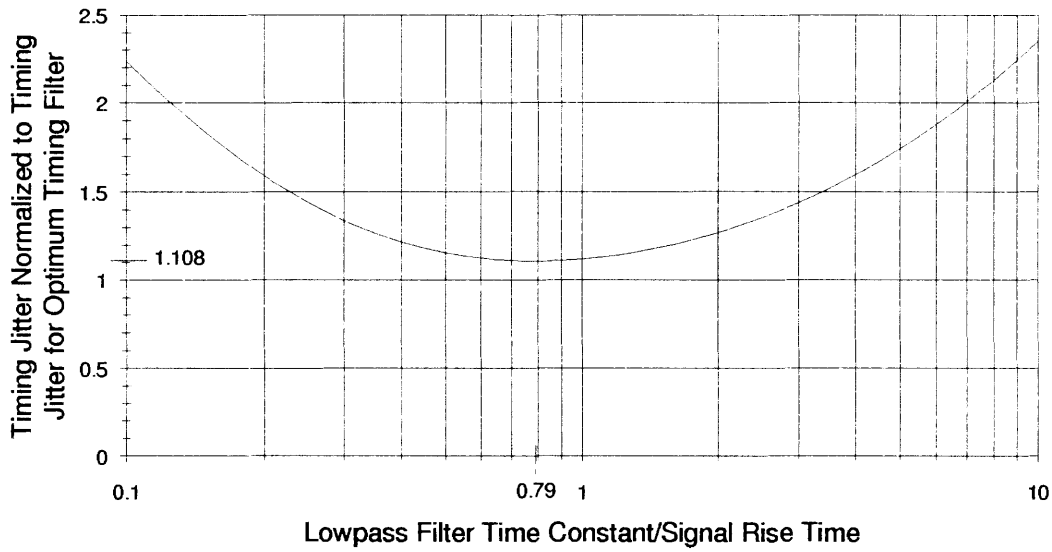


Figure 2-13. Output Timing Jitter for a Single-Pole Lowpass Filter with Linear-Edge Inputs in White Noise.

3. TIMING PERFORMANCE OF SCINTILLATION-DETECTOR SYSTEMS

Overview

In this section, the timing errors in scintillation-detector timing systems caused by detector statistical noise are considered. Detector statistical noise is the dominant source of timing errors for PET BGO/photomultiplier scintillation-detector systems.

The section begins with a description of scintillation-detector operation including the scintillation process and the conversion of scintillation photons (light) to detector photoelectrons. The random arrival times of detector photoelectrons following the detection of a gamma-ray event is then discussed as a major component of detector statistical noise. Detector photoelectron arrival times are modeled as a Poisson process and the theoretical timing spectra are presented for timing on the first through fifth detector photoelectrons.

Next, the operation of photomultiplier tubes is described, including sources of statistical noise. Photomultiplier single-electron impulse response, single-electron gain spread, and transit-time spread are discussed and illustrated for the photomultiplier tubes used in commercial PET BGO/photomultiplier detector systems. Additionally, the electronic noise of photomultiplier tubes is described. A brief comparison of PET BGO/photomultiplier and BGO/avalanche-diode detector timing performance is presented illustrating the significantly higher level of circuit noise present with the avalanche-diode detector.

The prediction of BGO/photomultiplier statistical noise is then discussed, first using Campbell's theorem which describes the statistical mean and variance for a linear system excited by Poisson-distributed impulses. As discussed, Campbell's theorem is not useful for quantitative prediction of statistical performance for the low number of detector photoelectron impulses present during timing discrimination. Instead, Monte Carlo analysis is developed where randomly occurring Poisson detector photoelectrons are simulated. This analysis is used to generate a timing spectrum resulting from the timing discrimination of simulated detector signals. Photomultiplier-tube statistical effects and the impulse response for the photomultiplier, front-end amplification circuit, and timing-shaping circuit are included in this analysis. Examples of Monte Carlo simulated timing spectra are given for low-threshold, first-photoelectron timing using both a mono- and tri-exponential BGO scintillation model that describes the rise-time and decay behavior of light scintillation following event interaction in the scintillator. The timing spectrum resulting from the tri-exponential BGO scintillation model represents the best timing performance available using the BGO/photomultiplier scintillation detector considered. Monte Carlo

analysis will be extended later in *Sections 4* and *5* to predict CFD timing and energy-discrimination performance.

Scintillation Detector Operation

A scintillation detector detects nuclear radiation by absorbing radiation, converting absorbed radiation into light (scintillation), and then converting this light into an electrical signal. In conventional (nontime-of-flight) PET systems, the scintillation detector consists of a BGO scintillator crystal coupled to a photomultiplier tube. The photomultiplier tube converts the BGO scintillation light to (photo) electrons at the photocathode, and these photoelectrons are then multiplied giving a typical electronic gain of one- to ten-million.

The BGO (chemical name $Bi_4Ge_3O_{12}$) scintillator is used in conventional PET systems because of its high density (specific gravity of 7.13) which is considerably higher than the density of sodium iodide, NaI(Tl) (specific gravity of 3.67) [1]. The NaI(Tl) scintillator is standardly used for scintillator comparisons, because of its high light output. The high density of BGO and high photoelectron cross-section for 511-keV annihilation gamma rays gives this scintillator excellent PET gamma-ray stopping power. Gamma-ray stopping power is an important consideration for PET applications because detection efficiency and spatial resolution are strongly dependent on gamma-ray stopping power. Unfortunately, the BGO scintillator is inefficient in its conversion of gamma rays to light, yielding only about 550 photoelectrons/MeV compared to about 9,000 photoelectrons/MeV for the NaI(Tl) scintillator [2]. The photoelectron yield includes the loss in photon-to-electron conversion at the photomultiplier cathode due to a quantum efficiency of approximately 20%.

Overview of Timing Errors in Scintillation Detectors

PET BGO/photomultiplier detector-system timing resolution is dominated by the statistical noise associated with limited detector photoelectron yield and nonzero scintillator decay time. As a result, a limited number of photoelectrons are randomly generated during a relatively long period of time after the initial gamma-ray excitation. This statistical process will be modeled in detail later as a nonstationary Poisson process.

Scintillation detector timing errors are also caused by variations in scintillation time with varying location of energy deposition and by variations in the scintillator light path length [3]. These errors may be significant for subnanosecond time-resolution scintillation detectors but are not dominant sources of timing error for PET BGO/photomultiplier scintillation detectors. The variation in scintillation time with interaction location is expected to be less than 100 ps FWHM for varying interaction locations of less than 30 mm

FWHM in the PET BGO block detector. The variation in light path-length time is expected to be in the order of 400 ps FWHM (for the PET BGO block detector) based on the difference in measured timing resolution for two BaF_2 scintillation detectors having different light path lengths [4]. The measured timing resolution for a uniform 10 mm x 10 mm x 30 mm BaF_2 scintillation detector is 214 ps FWHM degrading to 428 ps FWHM for a dodecahedron 10 mm x 18 mm x 45 mm crystal which necks down to a 10 mm x 10 mm area for photomultiplier coupling. Timing errors in the 100-ps to 400-ps range associated with variations in scintillation time and scintillator path-length time would combine in an uncorrelated sense with the detector statistical errors. Since PET BGO/photomultiplier detector timing resolution (for a single detector) is approximately 3 ns FWHM, the uncorrelated combination of 100 ps FWHM and 400 ps FWHM timing errors results in a total timing resolution of 3.03 ns FWHM. This indicates that these timing errors can be safely neglected as they would have to be much larger to be significant.

PET system timing performance is degraded somewhat by timing errors associated with the scintillation-detector photomultiplier tube. These photomultiplier timing errors include transit-time spread and single-electron gain spread which are functions of varying photoelectron paths in the photomultiplier tube [3]. These errors will be discussed later in this section.

Statistical Timing Performance of Scintillation Detectors

As mentioned, PET system timing performance is dominated by the statistical noise associated with the BGO/photomultiplier scintillation detectors. The measured photoelectron yield for a 511-keV annihilation gamma ray is approximately 300 for the BGO block detectors used in present CTI/Siemens PET systems [5]. This low number of photoelectrons and the relatively long (300 ns) decay time constant of BGO give rise to considerable statistical noise.

Scintillation-detector statistical timing performance is analyzed by considering the physical scintillation process. The description of this physical process will be simplified for brevity, and a more complete discussion is contained in *Radiation Detection and Measurement* by Knoll [1]. Absorbed radiation in the scintillator generates hole-electron pairs as some electrons in the scintillator lattice are knocked into excited states. The process of generating excited electron states is assumed to be nearly instantaneous with the absorption of radiation. The electrons in excited states then return to ground states giving off scintillation photons. The rate at which the excited electrons return to their ground

states (and the rate of the generation of scintillation photons) decays exponentially with time with a characteristic time constant for the scintillator.

Inorganic scintillators, such as BGO, typically have one dominant characteristic time constant [1], and a single time constant of 300 ns is often used to model BGO scintillation. These scintillators can be modeled with a mono-exponential scintillation model where scintillation light rises instantaneously (with zero rise-time) after event interaction, followed by a single-exponential decay. However, as will be illustrated by comparisons of Monte Carlo and measured timing performance in *Section 4*, a tri-exponential model must be used to accurately predict timing performance for BGO scintillation detectors. A tri-exponential characteristic has been reported for BGO having a 2.8-ns rise-time, a 300-ns decay time constant for 90% of the light, and a 60-ns decay time-constant for 10% of the light [2]. The finite rise-time of scintillation is due to a two-stage process where electrons are initially raised, essentially instantaneously, to excited states and then drop to intermediate states without giving off light [6]. Light emission (scintillation) then occurs when electrons return from intermediate states to ground states. A mono-exponential BGO scintillation model will be used for simplicity in Poisson statistical analysis of timing performance. Both the mono- and tri-exponential model will be used in Monte Carlo analysis of timing performance.

The statistical timing performance of scintillation detectors can be modeled as a non-stationary Poisson process where the average photoelectron rate is a function of time [7]. A Poisson process describes the arrival times of random events in time for some average rate. The probability density for the emission of N photoelectrons is given by

$$p_N(t) = \frac{[f(t)]^{N-1} e^{-f(t)} \frac{d}{dt} f(t)}{(N-1)!} , \tag{3-1}$$

where $f(t)$ is the average or expected number of photoelectrons emitted between the initial excitation ($t = 0$) and time t [7, 8].

The Poisson probability density given in Equation 3-1 can be evaluated for a constant average photoelectron emission rate, r_0, giving

$$p_N(t) = \frac{[r_0 t]^{N-1} e^{-r_0 t} r_0}{(N-1)!} , \text{ or} \tag{3-2}$$

$$p_N(t) = \frac{r_0^{\,N} t^{N-1} e^{-r_0 t}}{(N-1)!} \quad . \tag{3-3}$$

The photoelectron rate is assumed to step instantaneously, at the time of detector interaction (t = 0), from zero to a constant rate r_0. The constant photoelectron rate considered is given by

$$r_0 = N_0 / \tau \quad , \tag{3-4}$$

where N_0 is the total number of photoelectrons (the photoelectron yield) and τ is the scintillator decay time constant. A constant average photoelectron rate, r_0, can be assumed for a mono-exponential scintillation model for times much less than the decay time constant of the scintillator. For example, if BGO timing is derived in 5 ns, the average photoelectron rate at 5 ns is 98.3% ($e^{-5\ ns/300\ ns}$) of the initial rate and has thus decayed little from the initial rate.

It is interesting to note that the Poisson timing probability density for the arrival of N photoelectrons for a constant average photoelectron rate r_0 is identical to the impulse response of an N-th order, unity gain, Gaussian lowpass filter having a time constant of $1/r_0$. The timing probability density for the arrival of the first photoelectron (N = 1) has the form of a stepped, decaying exponential with initial value of r_0 and time constant $1/r_0$. The timing probability density has a semi-Gaussian shape for the arrival of the second photoelectron (N = 2) becoming increasingly Gaussian in shape for larger values of N. Plots of the timing probability density will be given later along with plots of the coincidence timing probability density for two BGO scintillation detectors.

The Poisson probability density given in Equation 3-1 can be evaluated for an average photoelectron rate that is a decaying exponential. This is useful for determining the arrival of events at times that are an appreciable fraction of the scintillator-decay time constant where the assumption of constant photoelectron rate is no longer valid. The average number of photoelectrons emitted between the initial excitation time (t = 0) and time t is then given by

$$f(t) = N_0\left[1 - e^{-t/\tau}\right] \quad , \tag{3-5}$$

where again N_0 is the total number of photoelectrons emitted and τ is the scintillator decay time constant. Substituting Equation 3-5 into Equation 3-1 gives the timing probability

density for the arrival of N photoelectrons at time t for an exponentially decaying average photoelectron rate. This timing probability density is given by

$$p_N(t) = \frac{N_0{}^N \left[1 - e^{-t/\tau}\right]^{N-1} e^{-N_0\left(1-e^{-t/\tau}\right)} e^{-t/\tau}}{\tau(N-1)!} \quad [8]. \tag{3-6}$$

Equation 3-6 simplifies to the constant photoelectron rate expression (Equation 3-3) for $t << \tau$ and $N_0 >> 1$.

The timing coincidence between pairs of BGO scintillation detectors is required in a PET system to determine if two 511-keV gamma rays are from the same positron annihilation. The coincidence-timing probability density for two detectors is the crosscorrelation of each detector timing probability density and is given by

$$p_{coin}(t) = \int_{-\infty}^{\infty} p_{start}(\tau) p_{stop}(\tau + t) d\tau \quad , \tag{3-7}$$

where $p_{start}(t)$ and $p_{stop}(t)$ are the timing probability densities for the start and stop detector respectively. Since the single-detector timing probability densities have values of zero for times less than zero, Equation 3-7 can be rewritten as

$$p_{coin}(-t) = \int_{t}^{\infty} p_{start}(\tau) p_{stop}(\tau - t) d\tau \quad , \text{and} \tag{3-8}$$

$$p_{coin}(t) = \int_{0}^{\infty} p_{start}(\tau) p_{stop}(\tau + t) d\tau \quad , \tag{3-9}$$

for $t \geq 0$ in each expression. Note that if both detectors have the same timing probability density, the coincidence-timing probability density is equal to the autocorrelation of the single-detector timing probability density. The coincidence-timing probability density is then symmetrical about time $t = 0$. For the PET coincidence-timing application considered, the start and stop detector timing probability densities will be assumed equal as the design of all detectors is the same.

The timing probability densities (Equation 3-3), or timing spectra, for a single BGO/photomultiplier scintillation detector are plotted in Figure 3-1 for the arrival of one to five photoelectrons (N = 1 - 5). A constant detector-photoelectron rate of 1.0/ns (511 keV) is assumed which corresponds to the initial rate for a mono-exponential BGO scintillation model having a photoelectron yield (N_0) of 300 and a 300-ns decaying-exponential time constant. Since the time values considered in Figure 3-1 range from 0 to 5 ns, the assumption of constant photoelectron rate is reasonable as the rate has decayed only 2% at 5 ns.

The single-detector timing spectra in Figure 3-1 are normalized to a maximum value of unity versus the standard normalization of unity area for probability densities to permit direct comparison of the FWHM timing resolutions. The timing spectrum for first photoelectron timing (N = 1), as discussed earlier, is a decaying exponential with time constant equal to the inverse of the photoelectron rate (r_0). The FWHM timing resolution for first photoelectron timing is given by

$$t_{FWHM}(N=1) = \ln(2)\frac{1}{r_0} , \tag{3-10}$$

which goes as the inverse of photoelectron rate. Similarly, the timing resolution for second (N = 2) and higher photoelectron timing also goes as the inverse of photoelectron rate. Timing resolution is then improved by raising the photoelectron rate by increasing the photoelectron yield, decreasing the photoelectron decay time constant, or a combination of both. There is considerable interest in obtaining a scintillator with the gamma-ray stopping power of BGO but with a higher initial photoelectron rate for improved timing resolution. Significantly improved timing resolution would permit the implementation of PET systems having lower random-coincidence noise than existing systems.

The timing probability densities, or timing spectra, for two BGO scintillation detectors in coincidence (Equations 3-8 and 3-9) are plotted in Figure 3-2 for the arrival of one to five photoelectrons (N = 1 - 5). The coincidence-timing spectra of Figure 3-2 were computed by numerical correlation of the single BGO scintillation-detector timing spectra shown in Figure 3-1. The coincidence-timing spectra in Figure 3-2 are normalized to unity to permit comparison of the FWHM timing resolutions.

Comparisons of single (Figure 3-1) and coincidence (Figure 3-2) BGO scintillation-detector timing spectra are shown in Table 3-1 for the arrival of one to five photoelectrons. Note that coincident timing resolution is a factor of 2.42 higher (a higher timing resolution

corresponds to a wider spectral line width, or poorer timing resolution) for second photoelectron timing compared to first photoelectron timing, indicating a clear resolution advantage in first photoelectron timing. Additionally, coincident timing resolution continues to increase, at a decreasing rate, for timing on an increasing number of photoelectrons. Finally, it is interesting to note that the coincident timing resolution for first photoelectron timing is *twice* that of the single-detector resolution, not the square-root-of-two increase as is often expected. This is because the single-detector first-photoelectron timing spectrum is a decaying exponential function instead of a Gaussian function. The coincident-timing resolution for second and higher photoelectron timing is, however, nearly the square-root-of-two larger than the single-detector timing resolution as these single-detector timing spectra are more nearly Gaussian in shape. The correlation of Gaussian functions gives a Gaussian function with a standard deviation that is the quadrature sum of the standard deviations for the functions correlated. Similarly, the quadrature combination applies to the convolution of Gaussian functions since convolution is a reverse-direction correlation operation and Gaussian functions are symmetrical.

Table 3-1. Detector Timing Resolution Versus Photoelectron Trigger Level for a Constant Photoelectron Rate of 1.0/ns.

Trigger	Single Detector Timing			Coincidence Timing			
N	50% Peak (ns)	50% Peak (ns)	FWHM (ns)	50% Peak (ns)	50% Peak (ns)	FWHM (ns)	Increase over Single
1	0.000	0.693	0.693	-0.693	-0.693	1.386	2.000
2	0.232	2.678	2.446	-1.678	1.678	3.357	1.372
3	0.761	4.156	3.395	-2.330	2.330	4.661	1.373
4	1.394	5.525	4.131	-2.850	2.850	5.699	1.380
5	2.083	6.838	4.755	-3.293	3.293	6.586	1.385

As mentioned earlier, single-detector timing resolution (for any selected photoelectron trigger level) is inversely proportional to the detector photoelectron emission rate. Similarly, coincident detector timing resolution is also inversely proportional to the photoelectron emission rate for the single detectors as the coincident (correlation) resolution scales with the resolution of the single detectors. Again, the significance of maximizing detector photoemission rate is clear. As an example, the GSO (Gadolinium Orthosilicate) scintillator material, under consideration for future PET systems, has a photoelectron yield 1.7 times greater than BGO and a decay time constant of 60 ns [9]. The GSO initial photoelectron emission rate (511 keV) is expected to be nearly 8.5/ns (300 x 1.7/60-ns) compared to the 1.0/ns rate for the photoelectron yield of 300 assumed for BGO. This would imply a greater-than factor-of-eight improvement (decrease) in detector timing resolution for PET systems using GSO verses BGO (neglecting photomultiplier-tube errors). Presently, cost considerations prohibit the large-scale use of GSO in PET systems.

Photomultiplier Tube Timing Performance

Overview of Photomultiplier Operation

The discussion of photomultiplier tube operation will be simplified for brevity, and a detailed discussion of photomultiplier tube operation is contained in the *Burle Photomultiplier Handbook*, formerly published by RCA [10]. The photomultiplier tube is used in PET BGO scintillation detectors to convert light (from the scintillator) into electrical current for subsequent electronic processing.

Incident light on the photomultiplier photocathode is converted to photoelectrons with a quantum efficiency that is a function of the photocathode material and the incident light wavelength. The 1-inch photomultiplier tubes used in CTI/Siemens PET systems use bialkali photocathode [11, 12] for good quantum efficiency at the BGO light wavelength of 480 nm [1], which is in the blue part of the visible spectrum. The quantum efficiency is, unfortunately, only about 20% resulting in an average release of photoelectrons at 20% of the incident photons [11, 12]. This greatly degrades the statistical timing performance of a BGO/photomultiplier scintillator detector by lowering the photomultiplier photoelectron rate from the much higher scintillator photon rate.

Photomultiplier electrical gain is accomplished by a series of dynodes which multiply the released photocathode photoelectrons through secondary emission. Secondary emission occurs when an electron with sufficient energy strikes a secondary-emitting surface resulting in the release of more than one electron. Photoelectrons released from the

photocathode are accelerated and focused by an electric field to strike the first dynode. The secondary electrons from this dynode are then accelerated by an electric field to strike the second dynode with the process continuing for additional dynodes until the multiplied electrons are intercepted at the photomultiplier tube anode. The photomultiplier tubes used in CTI/Siemens PET systems use 10 dynodes, each dynode having an approximate gain of four, resulting in an total photomultiplier gain of over 1,000,000 (4^{10}) [11, 12]. The dynode electric fields necessary for directing and accelerating electrons are provided by dynode voltages derived from a resistive voltage divider operating off a total voltage of 1500 Vdc [5].

Single-Electron Impulse Response

Timing on the lowest number of photoelectrons (preferably one) requires sufficient photomultiplier bandwidth to maximize the separation of individual photoelectrons. Photomultiplier bandwidth is typically characterized in the time domain using impulse response.

Photomultiplier time response is characterized by the output (anode) current response to an impulse or delta function of light at the photocathode [10]. This impulse response is the output response for a single photoelectron emitted from the photocathode and is characterized by output 10 - 90% rise-time, output 10 - 90% fall time, output FWHM pulse width, and output transit time (to the 50% point on the leading edge). The impulse response rise and fall times are due to the time dispersion of electrons during their travel in the photomultiplier tube. The transit time is the total time required for an electron to travel from the photocathode to the first dynode, the time of travel and multiplication in the dynode stages, and the time for multiplied electrons to be intercepted at the anode.

The impulse response for the one-inch, 10-stage photomultiplier tubes used in CTI/Siemens PET systems was experimentally measured [13, 14] for both the Burle C83062E [11] and the Hamamatsu R2497 [12] (either photomultiplier tube is used in a PET system). The impulse responses of both photomultiplier tubes were essentially identical, and the measured rise-times were within 20% of the specified 2.4-ns rise-times [11, 12]. From the measured impulse responses, the rise, fall, and width characteristics can be modeled by the impulse response of a three-pole Gaussian filter with a time constant (for each real pole) of 1.5 ns. This Gaussian model does not model the transit time (approximately 22 ns), but fixed transit time does not contribute to timing errors (transit-time spread is considered separately). The photomultiplier-tube impulse-response model is described for current entering the anode by

$$h_{PMT}(t) = \frac{Q}{\tau^3 2!} t^2 e^{-t/\tau} \quad (A) \quad , \tag{3-11}$$

where Q is the charge associated with a single electron multiplied by the photomultiplier gain of one-million and τ is the real-pole time constant of 1.5 ns.

The modeled photomultiplier single-electron impulse response is shown in Figure 3-3 for the photomultiplier gain of 1,000,000. The impulse-response rise-time (10 - 90%) shown in Figure 3-3 is 2.4 ns which agrees with the published 2.4-ns rise-times (10 - 90%) for the photomultiplier tubes used in CTI/Siemens PET systems [11, 12]. Note that the fall time is greater than the rise-time, which is typical of photomultiplier impulse responses [10, 15, 16, 17]. The longer fall time reduces the ability of a photomultiplier to separate individual photoelectrons. Additionally, the longer fall time increases photomultiplier step response as step response is found by integrating the impulse response.

Transit-Time Spread

Timing errors result from photomultiplier transit-time spread, which is caused by the varying path lengths of individual photoelectrons between the photocathode and first dynode and, to a lesser degree, by varying path lengths in the dynode multiplication and anode interception process [10]. The photoelectron path length from the photocathode to first dynode is a function of the location of photoelectron emission on the photocathode and photomultiplier tube electron-optic focusing. Additionally, transit-time spread is due to the statistically varying paths taken by photoelectrons and their corresponding multiplied electrons.

Photomultiplier transit-time spread is characterized by the width of the single-photoelectron transit-time spectrum resulting from uniform illumination of the photomultiplier tube cathode [10]. Transit-time spread can be modeled as a Gaussian density, based on reported experimental photomultiplier transit-time measurements [18, 19, 20, 21, 22, 23, 24, 25]. The specified transit-time spread for the Burle C83062E and Hamamatsu R2497 photomultipliers used in CTI/Siemens PET systems is 0.53 ns FWHM and 0.69 ns FWHM respectively [11, 12]. For subsequent timing analyses, a Gaussian transit-time spectrum having a value of 0.7 ns FWHM will be used to model transit-time spread.

Single-Electron Gain Response

The electron-multiplication gain of single photoelectrons emitted from a photomultiplier photocathode is described by the single-electron gain response [10]. The single-electron gain response is not constant for different photoelectrons because of electron multiplication statistics, the most dominant source of statistical variation being associated with a single photoelectron hitting the first dynode. Since the multiplication gain of this first dynode is on average about four, very poor statistics are associated with this multiplication process. Additionally, the remaining dynodes contribute to statistical variations in the single-electron gain response with decreasing effects for later dynodes since more electrons are available to strike the later dynodes. The total variation in photomultiplier single-electron gain response is described by the single-electron gain response spectrum.

The photomultiplier single-electron gain response spectrum is difficult to measure because of thermal (noise) emissions from the dynodes themselves that undergo partial multiplication. Electrons that undergo partial multiplication result in output pulses that are smaller than those associated with single photoelectrons released from the photocathode. It is necessary then to separate out the dynode noise from the single-electron gain spectrum associated with single photoelectrons. Additionally, it is necessary to excite the photomultiplier with low levels of light (this is a requirement for all single-photoelectron measurements) to ensure that only single photoelectrons are released.

The single-electron gain spectrum for the Burle C83062E photomultiplier tube was measured by Burle Industries, Inc. and is shown in Figure 3-4 [13]. In Figure 3-4, the single-electron gain spectrum is fitted to a Gaussian spectrum having a FWHM of 163%. This broad single-electron gain spectrum is not unusual for photomultiplier tubes, particularly those that are not specifically designed for single photoelectron timing [10]. Note that the Gaussian curve shown in Figure 3-4 fits the single-electron gain data very well except for low values of gain. The low-gain data that deviates from the Gaussian curve will not be considered as it is likely caused by dynode noise. For subsequent timing analyses, a Gaussian photomultiplier single-electron gain spectrum will be assumed having a FWHM of 163%. This is believed to also be a reliable indication of the Hamamatsu R2497 photomultiplier tube, also used in CTI/Siemens PET systems, because of its similarity to the Burle C83062E tube design [5].

Noise

Photomultiplier noise is caused by ohmic leakage of insulators, thermionic emission of electrons from the photocathode and dynodes, and internal regeneration effects [10]. At low

operating voltages where multiplication gain is low, noise is dominated by dark current associated with ohmic leakage of insulators. At typical operating voltages where multiplication gain is high, noise is dominated by dark current associated with thermionic emission. At very high operating voltages where multiplication gain is very high, noise is dominated by regenerative effects caused by dynode glowing under heavy electron bombardment and by glass scintillation from stray electrons attracted to the glass bulb near the photocathode and first dynodes (this effect is greatest if the glass bulb is surrounded by a shield connected to the anode voltage). For operation in PET systems under typical bias, photomultiplier tube noise is dominated by thermionic emission.

Single electrons emitted from the photomultiplier photocathode by thermionic emission result in anode current pulses with shape and average height equal to the single-electron impulse response (Figure 3-3). The statistical variation in pulse height is represented by the single-electron gain spectrum (Figure 3-4). The complete pulse-height spectrum for photomultiplier thermionic-emission noise pulses has an additional low pulse-height component due to thermionic emission from the dynodes. These electrons are only partially multiplied and result in lower amplitude output pulses.

The photomultiplier anode-current noise pulses associated with thermionic emission are much smaller and narrower than the 300-ns decaying-exponential anode-current pulses associated with BGO scintillation. As a result, the noise pulses can usually be rejected from the scintillation (signal) pulses. However, the rejection of these photomultiplier anode noise pulses becomes increasingly difficult for first-photoelectron timing systems where timing triggering occurs on individual photoelectron anode pulses (either signal or noise). It is necessary to properly qualify the timing output based on some measurement of signal energy. In constant-fraction discrimination timing systems, signal qualification is provided by the arming circuitry. Additionally, many systems (including PET systems) use a separate "slow" energy channel to further discriminate against low-energy signals and noise.

Photomultiplier anode noise pulses occur randomly in time with some average rate which is a Poisson process. These noise pulses give rise to shot noise, which is described by power spectral density in the frequency domain. This shot-noise power spectral density is constant for all frequencies if the photomultiplier anode noise pulses are impulses. However, actual anode noise pulses have finite width (described by the single-electron impulse response) causing shot-noise power spectral density to roll off at frequencies above

the frequency associated with this pulse width [10]. Photomultiplier anode-current noise-power spectral density is described by the shot noise equation,

$$i_n^2 = 2qI_{dark} \quad (A^2/Hz) \ , \tag{3-12}$$

where q is the unit of electronic charge and I_{dark} is the anode dark current.

The anode shot noise predicted by Equation 3-12 is 0.18 pA/Hz$^{1/2}$ for a maximum dark current of 100 nA for the photomultiplier tubes used in CTI/Siemens PET systems [11, 12]. This corresponds to a voltage noise density of only 9 pV/Hz$^{1/2}$ for a 50-Ω anode load, which is totally negligible compared to the typical 4 nV/Hz$^{1/2}$ input-amplifier voltage-noise density [5]. Photomultiplier anode shot noise increases when signal current is present, but this noise is negligible compared to the statistical noise associated with random photoelectron emissions resulting from BGO scintillation. Actual photomultiplier noise is approximately 15% higher than the value predicted by shot noise because of excess noise associated with the Poisson statistics of the multiplication process [10]. This 15% increase in photomultiplier anode noise due to excess noise is also negligible for PET applications.

Photomultiplier and Photodiode Comparisons for PET Applications

The previous noise calculations illustrate the excellent low electronic-noise performance of photomultiplier tubes, which together with their excellent gain-bandwidth performance (in excess of 50 MHz x 1,000,000) has not been challenged by semiconductor light detectors for PET applications. Silicon PIN photodiodes have the disadvantages, compared to photomultiplier tubes, of no gain, high device capacitance, and low-noise preamplification requirements [10]. Silicon avalanche photodiodes are more suitable than PIN diodes for PET applications because of internal gain (in the range of 100) but exhibit very high excess noise from the avalanche gain process [26].

The most significant limitation in using silicon photodiodes for PET applications is excessive timing jitter due to photodiode and preamplifier noise. Most reported timing performance is for a commercial gamma-ray detector module [27] consisting of a BGO crystal (3 x 5 x 20 mm) coupled to an avalanche photodiode (3 x 3 mm active area) [26, 28, 29, 30]. Timing performance of approximately 10 ns FWHM has been reported for this commercial detector using a nonintegrated charge-sensitive preamplifier [26, 28, 29]. Recently, timing performance of 9.2-ns FWHM has been reported for the commercial detector using a low-noise, integrated CMOS transimpedance preamplifier [30]. Since a separate avalanche photodiode would be required for each BGO-crystal element in a solid-

state PET detector to minimize photodiode size and noise, a monolithic CMOS preamplifier would be required to minimize system costs. Additionally, a monolithic CMOS CFD would be required for solid-state PET detectors as multiple BGO-crystal, avalanche-photodiode channels cannot be summed because of the high level of avalanche-photodiode noise present. The development of monolithic CMOS circuits is clearly even more significant for avalanche-photodiode, BGO-crystal PET detector systems compared to existing photomultiplier, BGO-block detectors because of the higher required front-end electronic-circuit density.

Avalanche-photodiode, BGO-crystal timing performance in the 10-ns FWHM range is considerably above the 3-ns FWHM value obtained with modern PET BGO/photomultiplier detector systems [5]. Further research is needed to improve the timing performance of avalanche photodiodes by reducing active area (reducing capacitance and diode noise) and by reducing noise due to edge effects. Such research is significant as a photodiode replacement of the photomultiplier tube could considerably reduce the size and cost of existing PET BGO/photomultiplier detectors.

Timing Performance of Scintillation Detector and Time Pick-Off Circuit

Overview

The timing performance of time pick-off circuits due to time walk and noise-induced timing jitter has been described in *Section 2*. Additionally, the statistical timing performance of scintillation detectors has been described in this section. It is necessary then to analyze system timing performance of the detector and time pick-off circuit combination. Such system analysis is necessarily complex because of the multiple effects considered: statistics of light generation and reflection within the scintillator (negligible for BGO/photomultiplier systems as described earlier), Poisson statistics associated with scintillation-detector photoelectrons, photomultiplier single-electron gain and transit-time statistics, and circuit response of the photomultiplier, front-end amplifier circuit, and timing-discriminator circuit. A closed-form analysis for the arrival times of photomultiplier anode photoelectron pulses for NaI(Tl)/photomultiplier systems was developed by Nutt using order statistics, although the effects of front-end amplification and time-discrimination circuits were not included [18]. A closed-form timing analysis including the performance of front-end amplification and time-discrimination circuits is not believed to exist.

In the following discussion, Campbell's theorem [31] will be described for modeling certain scintillation-detector statistical errors. Following this discussion, a Monte Carlo

technique for predicting timing performance will be developed, which includes Poisson photoelectron statistics, photomultiplier single-electron gain and transit-time statistics, and front-end amplification and timing-discrimination circuit response.

Campbell's Theorem Analysis

Campbell's theorem describes the statistical mean response and variance of a linear system excited by Poisson distributed impulses having some average rate. The generalized form of Campbell's theorem considers the nonstationary statistics associated with a time-varying average impulse rate and is given by

$$\mu(t) = \int_{-\infty}^{\infty} r(\tau)h(t-\tau)d\tau \quad \text{, and} \tag{3-13}$$

$$\sigma^2(t) = \int_{-\infty}^{\infty} r(\tau)h^2(t-\tau)d\tau \quad , \tag{3-14}$$

where $\mu(t)$ is the mean response, $\sigma^2(t)$ is the variance, $r(t)$ is the average impulse rate, and $h(t)$ is the linear-system impulse response [31]. Equations 3-13 and 3-14 can be evaluated for a system having causal impulse response with an average impulse rate that is a step function transitioning at time $t = 0$ (this is not stepped white noise, but rather randomly occurring impulses with an average rate that steps from zero to some stepped value). The mean response and variance (derived from graphical convolution) are then described by

$$\mu(t \geq 0) = r_0 \int_0^t h(\tau)d\tau \quad \text{, and} \tag{3-15}$$

$$\sigma^2(t \geq 0) = r_0 \int_0^t h^2(\tau)d\tau \quad , \tag{3-16}$$

where r_0 is the stepped value of the average impulse rate and $h(t)$ is the causal linear-system impulse response. As discussed earlier, scintillator photoelectron rate for a mono-exponential scintillation model is well approximated by a step function (transitioning at the time of detector event interaction) for timing derived at times much less than the

scintillation-detector decay time constant. The photoelectron rate is essentially constant for times much less than the scintillation-detector time constant.

Linear-system mean response and standard-deviation (square-root of variance) can be found using Campbell's theorem. This is shown in Figure 3-5 for the photomultiplier impulse response given in Figure 3-3 (Equation 3-11) for a step photoelectron rate (r_0) of 1.0/ns. Note that the detector-output standard-deviation increases rapidly for times greater than zero, reaching a final value for times greater than the width of the photomultiplier impulse response. The standard-deviation effectively describes the statistical fluctuations present at the signal output of the photomultiplier. The mean and standard-deviation shown in Figure 3-5 were found in closed form from Equations 3-15 and 3-16.

The BGO/photomultiplier detector-output mean and standard deviation given by Campbell's theorem in Figure 3-5 suggests that optimal timing occurs early on the output signal where the standard deviation is minimized. Quantitative timing performance, however, cannot be predicted for the case considered in Figure 3-5 because the mean and standard deviation described by Campbell's theorem do not represent a Gaussian density because of the low number of photoelectron emissions present (a mean value of five over the 5-ns time interval considered). An alternative analysis method is then required for the application considered where timing occurs on a low number of photoelectrons. Campbell's theorem analysis will be used later in *Section 4* to predict CFD energy-discrimination performance.

The timing performance illustrated qualitatively by Figure 3-5 indicates that optimum statistical timing performance occurs at the lowest possible timing threshold corresponding to timing on the earliest part of the detector output signal. Unfortunately, timing on the early part of the signal results in greater time-jitter and time-walk errors because of limited signal slope. Additionally, false triggering on noise is greater for the low threshold required for triggering on the early part of the signal.

As mentioned, no closed-form timing analysis is believed to exist that considers photoelectron Poisson statistics, photomultiplier single-electron gain and transit-time statistics, and time pick-off circuit response. With the lack of an analytical expression to predict system timing performance, timing performance must be evaluated by Monte Carlo simulation or by experimental evaluation.

Monte Carlo Simulation

Method

System timing performance of a scintillation detector and time pick-off circuit can be evaluated using Monte Carlo simulation where computer-generated random numbers are used to simulate statistical processes. In Monte Carlo simulation, the timing signal is simulated for a detected event, and the timing crossing of this signal is histogrammed into a timing spectrum. This process is repeated for many simulated detected events until enough timing values are found to build a statistically meaningful timing spectrum. Monte Carlo simulation of timing and energy-discrimination performance for CFD time pick-off circuits has been presented by the author at the 1992 IEEE Nuclear Science Symposium [32].

The Monte Carlo simulated timing signal is modeled as the output of a linear system randomly excited by Poisson-distributed impulses representing detector photoelectron emissions. This linear system is itself modeled by a causal impulse response, $h(t)$, which includes the photomultiplier single-electron response, front-end amplification and filtering response, and constant-fraction shaping-circuit response if constant-fraction shaping is used. Varying photomultiplier single-electron gain is considered by varying the strength of the simulated photoelectron impulses, and varying photomultiplier transit time is considered by varying the delay time of simulated photoelectron impulses. The modeling of scintillation-detector output signals by Monte Carlo simulation is illustrated in Figure 3-6.

The Monte Carlo simulated timing signal for each detected event is the sum of timing-system impulse responses resulting from photoelectron emissions. The timing signal is described mathematically as

$$Timing\ signal(t) = \sum_{K=1}^{K=M} G_{PMT}(K)\, h(t - t_{Poisson}(K) - t_{PMT}(K)) \quad \text{, where} \tag{3-17}$$

K is the index for each photoelectron emission (ranging from 1 to M) where M is the minimum number of photoelectrons required for timing crossing (normally much less than the total number of photoelectrons emitted (N_0));

$G_{PMT}(K)$ is the normalized photomultiplier single-electron gain from single-electron gain spectrum;

$h(t)$ is the impulse response of photomultiplier, front-end amplifier/filter, and timing shaping network (if present);

$t_{Poisson}(K)$ is the photoelectron emission time from Poisson distribution (function of detected energy); and

$t_{PMT}(K)$ is the photomultiplier single-electron transit time from transit-time spectrum.

Equation 3-17 is similar to other Monte Carlo timing-signal models reported in the literature; however, the reported models do not include front-end amplification and timing circuitry response [33, 34, 35].

The Poisson photoelectron emission times are given mathematically by

$$t_{Poisson}(K) = t_{Poisson}(K-1) + \left[\frac{1}{r(t_{Poisson}(K-1))}\right](-\ln(rand)) \quad , \tag{3-18}$$

where $t_{Poisson(K-1)}$ is the emission time for the previous photoelectron (taken as zero if no previous photoelectron has occurred), $r(t)$ is the average photoelectron rate, and *rand* denotes a uniformly-distributed random number between zero and one (with infinitesimal probability of equaling zero as $ln(0)$ is undefined). The photoelectron-emission times correspond to the emission times for single Poisson events where the probability density for waiting times between Poisson events is equal to the probability density for a single Poisson emission. The Poisson photoelectron emission times given in Equation 3-18 correspond to an average photoelectron emission rate that steps instantaneously from zero as representative of the mono-exponential BGO scintillation model. Equation 3-18 cannot be used, however, for the tri-exponential BGO scintillation model where the photoelectron emission rate has a finite rise-time.

The right-hand side of Equation 3-18 corresponds to the transformation function required to map a uniform (between zero and one) random variable to a random variable having the probability density associated with single Poisson-emission times. This transformation function is equal to the inverse probability-distribution function of the desired output Poisson random variable which can be shown by solving Equation 2-2 (page 21) for the transformation function required to map a uniform (between zero and one) input random variable to an output Poisson random variable. In Equation 3-18, the average emission rate $r(t)$ is assumed constant for the time interval between Poisson emissions, which is a good assumption since the rate changes very little for an average interval time of 1 ns corresponding to an initial BGO/photomultiplier detector photoelectron rate of 1.0/ns. The photoelectron rate given in Equation 3-18 is linearly proportional to detected event

energy having a mean value set by the photoelectron rate for a mean event energy of 511 keV. Fixed, exponentially-decaying, or arbitrary average emission rates may be used in Equation 3-18 subject to the assumption of constant rate between Poisson emissions.

In the Monte Carlo timing simulation, points are selected from the Gaussian event energy, Gaussian photomultiplier single-electron gain, and Gaussian photomultiplier transit-time spectra by a transformation of uniformly-distributed random numbers using the algorithm described in *Numerical Recipes in C* [36]. Photomultiplier single-electron gain and transit-time are assumed to be uncorrelated in the Monte Carlo analysis. The correlation present between the gain and transit time of single photoelectrons is not known, but the effects of transit-time spread (with a 0.7-ns FWHM resolution) are not significant for a system timing resolution of 3 ns FWHM. The good agreement between Monte Carlo simulated and measured timing spectra for both the delay line CFD (presented in *Section 4*) and the fully-monolithic CMOS CFD (presented in *Section 5*) indicates that the assumption of no correlation between photomultiplier single-electron gain and transit-time spread is reasonable, at least for timing resolutions near 3 ns FWHM. Correlation effects, if present, may need to be considered for timing resolutions approaching the photomultiplier transit-time resolution.

The computer program used for Monte Carlo simulation is included in *Appendix B*. This program is written in the C computer language and is documented for interpretation. The timing-signal impulse response, $h(t)$, is evaluated in a lookup table that is read in from a SPICE print listing. The lookup table permits the evaluation of complex impulse responses without mathematical derivation and greatly increases the execution speed of the Monte Carlo program by avoiding time-consuming exponential mathematical evaluations. The Monte Carlo program histograms all statistical quantities: the timing spectrum, the detected-energy spectrum, the photomultiplier single-electron gain spectrum, and the photomultiplier transit-time spectrum. Additionally, the coincidence timing spectrum for two identical timing systems is histogrammed by subtracting the timing difference between adjacent events. Digital filtering of the simulated spectra is provided, by convolving each spectrum with a selected Gaussian lowpass impulse response, to smooth out statistical noise. Finally, an analysis of each filtered spectrum is provided giving peak counts, FWHM, and FWTM information. The program writes the raw spectrum, filtered spectrum, and spectrum analysis data to an output text file for reading by commercial spreadsheet/plotting programs.

In addition to the Monte Carlo timing-simulation program, a Monte Carlo waveform-generation program was also written. The waveform-generation program uses the same Monte Carlo algorithms as the timing-analysis program but provides an output file consisting of multiple (one for each simulated event) signal waveform values.

Random Number Generation and Evaluation

As mentioned, uniformly-distributed random numbers are required for transformation into the Poisson and Gaussian points used in the Monte Carlo timing simulation. The generation of uniformly-distributed random numbers is often done using a linear congruential generator, where a random number is generated from a linear combination of the previous random number and numerical constants [36]. The linear congruential generator develops a pseudorandom number sequence that is uniformly distributed; however, excessive autocorrelation for nonzero delay values may be present in the random-number sequence. The generation of uniformly-distributed random numbers is complicated greatly by attempting to minimize the autocorrelation for nonzero delay values. Ideally, the random-number sequence autocorrelation would be zero for all nonzero delay values, which is analogous to the autocorrelation of white noise and indicates statistical independence of individual numbers in the random-number sequence.

The initial random-number algorithm considered consisted of a shuffled linear-congruential generator taken from *Numerical Recipes in C* [36]. The process of shuffling the generator (rearranging groups of bits in the output word) is intended to minimize the autocorrelation for nonzero delay values. It was found that this initial random-number generator produced excessive statistical noise in the Monte Carlo timing spectra, as will be illustrated in following timing spectra. The final algorithm used for random-number generation was also taken from *Numerical Recipes in C* but is based on the subtractive algorithm described by Knuth in *Seminumerical Methods - The Art of Computer Programming* [37].

The autocorrelation of a random-number sequence can be described mathematically as

$$\Phi_{xx}(k) = \frac{1}{N} \sum_{n=1}^{n=N} X(n)X(n+k) \quad , \tag{3-19}$$

where $X(n)$ denotes the n-th number in the random-number sequence, k denotes the delay considered between random-number samples, and N denotes the number of autocorrelation experiments evaluated. The autocorrelation coefficient is a useful measure of random-

number sequence autocorrelation as the effects of random-number sequence mean and variance have been subtracted and normalized out respectively. The autocorrelation coefficient is given by

$$\rho_{xx}(k) = \frac{\Phi_{xx}(k) - \mu_x^2}{\Phi_{xx}(0) - \mu_x^2} = \frac{\Phi_{xx}(k) - \mu_x^2}{\sigma_x^2} \quad , \tag{3-20}$$

where μ_x is the mean value, $\Phi_{xx}(0)$ is the mean-square value, and σ_x^2 is the variance value for the random-number sequence. The autocorrelation coefficient has values constrained between ±1 with a value of zero corresponding to statistical independence and values of ±1 corresponding to total statistical dependence. Equation 3-20, although different in notation, is equal to the serial-correlation coefficient described by Knuth [37] for testing random-number sequence autocorrelation. The random-number sequence mean required in Equation 3-20 is given by

$$\mu_x = \frac{1}{N} \sum_{n=1}^{n=N} X(n) \quad , \tag{3-21}$$

where N, again, is the number of autocorrelation experiments evaluated.

The random-number sequence autocorrelation coefficient (Equation 3-20) was computed for the subtractive random-number generator used in the Monte Carlo simulation program. The autocorrelation coefficient is shown in Figure 3-7 for a sequence length (N) of one-million and for sequence-delay values (k) ranging from one to one-hundred. The autocorrelation coefficient is below ±0.001 for most delay values and has an average absolute value of 0.000667 for all delay values considered. The level of autocorrelation shown in Figure 3-7 is within the level of autocorrelation expected by Knuth [37] for a "good" random-number generator. The autocorrelation coefficient expected for a "good" random-number generator is described by

$$(\mu_N - 2\sigma_N) < \rho_{xx}(k \neq 0) < (\mu_N + 2\sigma_N) \quad , \tag{3-22}$$

where the autocorrelation coefficient is expected to be within the limits described about 95% of the time [37]. The values of μ_N and σ_N are given by

$$\mu_N = \frac{-1}{N-1} \quad , \text{ and} \tag{3-23}$$

$$\sigma_N = \frac{1}{N-1}\sqrt{\frac{N(N-3)}{N+1}} \quad , \tag{3-24}$$

where N (the number of samples considered) is greater than two [37]. The autocorrelation-coefficient limits are ±0.002 from the preceding equations (one-million samples) and the autocorrelation coefficient given in Figure 3-7 is within these limits 98% of the time, exceeding the 95% requirement for a "good" random-number generator.

The testing of random-number generators is exceedingly complex, and the autocorrelation test described is only one of many available tests [37]. Press [36] suggests that Monte Carlo simulation results be compared using substantially different random-number generators in an attempt to validate results. As mentioned, both a re-seeded, linear congruential generator and a subtractive generator were evaluated. The subtractive generator ultimately selected had autocorrelation that was on average a factor-of-two less than the re-seeded, linear congruential generator. Additionally, as will be illustrated later, the statistical noise associated with the re-seeded, linear congruential generator was considerably higher than the subtractive generator. It is interesting, however, that the Monte Carlo simulation results compared well for both generators (as will be illustrated later) with the only exception of excess statistical noise for the re-seeded, linear congruential generator.

Simulation of First Photoelectron Timing without Photomultiplier Effects

In Figure 3-8, Poisson-distributed detector-photoelectron impulses are shown for a single 511-keV event detected by a BGO/photomultiplier scintillation detector. This train of impulses was generated by the Monte Carlo waveform-generation program assuming a total photoelectron yield of 300 (511 keV), a mono-exponential decay time constant of 300 ns, and a corresponding initial photoelectron rate of 1.0/ns (511 keV). The random time occurrence of these impulses is evident by random groupings and gaps in the photoelectron impulses. The exponentially-decaying average-photoelectron rate is not easily observed as only the first 50 ns of time following the detector event interaction is shown.

Monte Carlo timing simulation of first photoelectron timing was done without photomultiplier effects for the BGO/photomultiplier scintillation-detector photoelectron yield of 300 (511 keV), mono-exponential decay time constant of 300 ns, and corresponding initial photoelectron rate of 1.0/ns (511 keV) previously described. A monochromatic energy spectrum at 511 keV was considered for comparison with the timing spectrum predicted earlier in the monochromatic, 511-keV Poisson analysis. First photoelectron timing

simulation was done using a fast (duration of 10 ps) timing-signal impulse response so that timing crossings occurred immediately for the first simulated photoelectron emissions. Both raw and filtered timing spectra data were provided by the Monte Carlo timing-simulation program.

Monte Carlo timing simulation of first-photoelectron timing was made using the re-seeded, linear-congruential random number generator initially considered. Although the filtered Monte Carlo timing spectrum generated using this initial random number generator agrees well with the theoretical timing spectrum, the raw Monte Carlo timing spectrum contains excessive statistical noise as shown in Figure 3-9.

In Figure 3-10, the Monte Carlo timing spectrum for first photoelectron timing is shown for the final subtractive random-number generator used. Both raw and filtered timing spectra data are shown in Figure 3-10, and the computed timing resolution from the filtered data is 0.73 ns FWHM, which is in close agreement with the theoretical Poisson resolution of 0.693 ns FWHM from Figure 3-1 and Table 3-1. The Monte Carlo timing spectrum is compared in logarithmic form (Figure 3-11) with the theoretical first-photoelectron timing spectrum. The Monte Carlo timing spectrum and the theoretical Poisson, exponentially-decaying timing-spectrum agree very closely, both following a straight line indicative of a logarithmic presentation. The statistical noise present in the Monte Carlo spectrum of Figure 3-11 is appropriate for the number of channel counts present and appears exaggerated for low channel counts because of the logarithmic presentation.

Monte Carlo timing simulation of first photoelectron timing, again without photomultiplier effects, was repeated using the tri-exponential BGO scintillation model instead of the mono-exponential model previously considered. A scintillation rise-time time constant of 1.5 ns, primary decay time constant of 300 ns for 90% of the light, and secondary decay time constant of 60 ns for 10% for the light was assumed in the tri-exponential model. This is equivalent to the tri-exponential model reported by Moszynski [2], except that a time constant of 1.5 ns was used to model scintillation rise-time (the reported rise-time was 2.8 ns). The rise-time time constant of 1.5 ns was chosen based on comparisons described in *Section 4* between measured and Monte Carlo timing resolution for a commercial delay-line CFD. Monte Carlo simulations and measurements were compared for various CFD delays to ensure accurate modeling.

Monte Carlo first-photoelectron timing spectra are shown in Figure 3-12 for both the mono- and tri-exponential BGO scintillation models for a monochromatic energy spectrum at 511 keV and a photoelectron yield of 300 (511 keV). The timing spectrum associated with

the mono-exponential model (the model previously considered) is a decaying exponential, as predicted earlier by the Poisson statistics, having a resolution of 0.73 ns FWHM and 2.33 ns FWTM. The timing spectrum, however, associated with the tri-exponential model is semi-Gaussian in shape having a considerably higher resolution of 1.98 ns FWHM and 3.70 ns FWTM. The higher timing resolution present in the tri-exponential model is due to the finite scintillation rise-time. Comparisons between measured and Monte Carlo timing resolution given later in this section and in *Section 4* indicate that the tri-exponential BGO scintillation model is required for accurate modeling of timing resolution.

Monte Carlo simulations for an energy resolution of 14% FWHM indicate that first-photoelectron timing resolution is not a function of energy resolution for a (symmetrical) Gaussian energy spectrum. This is because energies below the mean result in higher timing resolution, whereas energies above the mean result in lower timing resolution. Thus, the timing spectrum for a Gaussian-energy spectrum is identical in shape to the timing spectrum for a monochromatic energy spectrum having energy equal to the mean Gaussian energy.

Simulation of First Photoelectron Timing with Photomultiplier Effects

In Figure 3-13, Monte Carlo simulated photomultiplier output signals are shown for several events detected by a BGO/photomultiplier scintillation detector, assuming again a photoelectron yield of 300 (511 keV) and a mono-exponential decay time constant of 300 ns which closely models a constant photoelectron rate of 1.0/ns (511 keV). The signals were simulated for a Gaussian energy spectrum having a mean energy of 511 keV and resolution of 14% FWHM, for the photomultiplier impulse response shown in Figure 3-3, for a photomultiplier single-electron gain of 1,000,000 (built into the impulse response) having ideal resolution (0% FWHM), and for a photomultiplier transit time of 5 ns having ideal resolution (0 ns FWHM). Actual photomultiplier transit time is approximately 22 ns, but a value of 5 ns is used for convenience as fixed delay has no effect on timing resolution. Simulations of output signals without photomultiplier single-electron gain or transit-time spread were done for comparison with output signals resulting from the photomultiplier when single-electron gain and transit-time spread are included.

The times associated with photomultiplier-output signals leaving the zero-current baseline (Figure 3-13) are equal to the single-photoelectron timing crossings as no photomultiplier resolution errors have been included other than finite photomultiplier bandwidth (the fixed, nonstatistical photomultiplier single-electron gain and transit time considered have no effect on timing resolution). The mean peak photomultiplier current

(511 keV) is approximately 160 μA, which is in agreement with the theoretical mean response illustrated in Figure 3-5. Additionally, it is clear from Figure 3-13 that timing resolution will degrade for increasing leading-edge discriminator threshold levels. If the timing point is delayed from the beginning of the detector signal, timing resolution will degrade for both leading-edge and constant-fraction timing.

In Figure 3-14, photomultiplier output signals are shown again for several detected events; however, this time full photomultiplier resolution errors have been included. These errors include a 163% FWHM single-electron gain resolution and a 0.7 ns FWHM transit-time resolution. A comparison of Figure 3-14 with Figure 3-13 illustrates that timing resolution degrades somewhat as a result of photomultiplier resolution errors. For first-photoelectron timing, the photomultiplier single-electron gain resolution does not influence timing; however, the photomultiplier transit-time resolution is significant. For timing at thresholds above the zero-signal baseline (timing on greater than the first photoelectron), both the single-electron gain and transit-time resolution have an effect on timing resolution.

In Figure 3-15, Monte Carlo simulated timing spectra are shown for timing directly on the photomultiplier output (Figure 3-14). A low-level timing threshold of 0.1 μA (the mean peak signal is approximately 160 μA for 511 keV) was used for the simulations to approach first-photoelectron timing, and a timing spectrum was simulated for both the mono- and tri-exponential BGO scintillation models. The simulated timing resolution for a Gaussian energy spectrum with mean of 511 keV and resolution of 14% FWHM is 1.37 ns FWHM and 3.35 ns FWTM for the mono-exponential model, and 2.06 ns FWHM and 4.01 ns FWTM for the tri-exponential model. The simulated timing resolution for the tri-exponential model is in close agreement with the measured resolution reported by Moszynski et al. [2] of 2.1 ns FWHM and 4.4 ns FWTM for first-photoelectron timing (using a BGO/photomultiplier scintillation detector). The close agreement between measured and simulated timing resolution using the tri-exponential model indicates that the tri-exponential model should be used in Monte Carlo timing simulations. Additionally, as mentioned earlier, comparisons of measured and simulated CFD timing resolution described in *Section 4* also indicate that the tri-exponential model should be used. The timing resolution available for low-threshold (first-photoelectron) timing at the photomultiplier output (Figure 3-15), using the tri-exponential BGO scintillation model, is believed to represent the best (lowest) timing resolution available for the BGO/photomultiplier detector considered.

Compton scatter is not included in the Gaussian energy spectrum used for the first-photoelectron timing spectra of Figure 3-15. Compton scatter will be discussed in *Section 4*

and included in Monte Carlo simulations contained in *Sections 4* and *5*. Monte Carlo simulations for the CMOS CFD described in *Section 5* indicate that timing resolution is degraded (increased) by approximately 5% for low-level Compton scatter (scatter associated with a point source and 1 x 1 x 1-inch BGO crystal) and by approximately 10% for high-level Compton scatter (scatter associated with a 20-cm diameter, water-filled source and 1 x 1 x 1-inch BGO crystal).

The Monte Carlo simulated timing spectra of Figure 3-15 are effectively the convolution of the ideal (exclusive of photomultiplier transit-time errors) first-photoelectron timing spectra shown in Figure 3-12 with the 0.7-ns FWHM Gaussian transit-time spectrum of the photomultiplier. This convolution operation significantly increases the near zero rise-time of the ideal first-photoelectron timing spectrum associated with the mono-exponential BGO scintillation model and also increases the fall time giving a resulting timing resolution equal to nearly twice the theoretical Poisson first-photoelectron resolution of 0.693 ns FWHM. The 0.7-ns FWHM Gaussian transit-time spectrum has little effect on the ideal first-photoelectron timing spectrum using the tri-exponential model since this (ideal) timing spectrum has a timing resolution of 1.98 ns FWHM which is considerably greater (for uncorrelated combination) than the transit-time spread of 0.7 ns FWHM.

The simulated energy spectrum for the Monte Carlo timing spectra of Figure 3-15 is shown in Figure 3-16. This energy spectrum is Gaussian in shape and the calculated resolution (from the Monte Carlo program) is 14.4% FWHM which compares well with the selected value of 14.1% FWHM. The simulated photomultiplier single-electron gain spectrum is shown in Figure 3-17 and is also Gaussian in shape. The calculated resolution is 167% FWHM which compares well with the selected value of 163% FWHM. Finally, the simulated photomultiplier transit-time spectrum is shown in Figure 3-18 which, again, is Gaussian in shape. The calculated resolution is 0.72 ns FWHM which agrees well with the selected value of 0.7 ns FWHM. As mentioned, a mean photomultiplier transit time of 5 ns has been assumed instead of the actual transit time of 22 ns, as fixed delay has no effect on timing resolution.

Although optimum timing for BGO/photomultiplier scintillation-detector systems is obtained using first-photoelectron timing, it is interesting to note that optimum timing for NaI(Tl)/photomultiplier systems is obtained for timing on more than the first photoelectron [18]. This is because the intrinsic Poisson first-photoelectron timing resolution of NaI(Tl)/photomultiplier detectors is considerably less than the photomultiplier-tube transit-time spread. The intrinsic Poisson first-photoelectron timing resolution of

NaI(Tl)/photomultiplier detectors is approximately 0.01925 ns FWHM (from Equation 3-10) for an initial photoelectron rate of 36.0/ns corresponding to a photoelectron yield of 9000 [1] and scintillator-decay time constant of 250 ns [18]. Optimal timing for NaI(Tl) systems has been reported for timing on 0.2 - 0.6% of the total number of photoelectrons (photoelectron yield) because of averaging of photomultiplier transit-time errors [18].

Simulation of General Scintillation-Detector Systems

General scintillation-detector system performance can be predicted using Monte Carlo simulation by using the appropriate photoelectron rate function, energy resolution parameters, system impulse response, and photomultiplier-tube resolution parameters. Additionally, time pick-off circuit walk performance can be included in Monte Carlo simulation by evaluating the timing-signal underdrive, overdrive, and slope at the threshold crossing. This can be done for each simulated event and the time walk can be included as an additional timing delay. This time walk can be modeled as a function of the variable timing-signal underdrive, overdrive, and slope at the threshold crossing. The walk function itself can be evaluated from the comparators used in the time pick-off circuit. Comparator walk performance will be discussed in detail in *Section 5*.

Time pick-off circuit electronic-noise timing jitter can also be added to Monte Carlo simulation by evaluating the timing-signal slope at the threshold crossing. The timing jitter is the ratio of noise-to-signal-slope and can be included for the variable timing-signal slope present for each simulated event.

Monte Carlo simulation will be used in *Section 4* for predicting CFD timing performance as a function of constant-fraction shaping-network design. Additionally, Monte Carlo simulation will be extended in *Section 4* to predict CFD energy-discrimination performance which is limited by the statistical noise in the BGO/photomultiplier scintillation-detector signal. Finally, Monte Carlo simulation will be used in *Section 5* to predict timing and energy spectra for the fully-monolithic CMOS CFD.

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Appendix for Section 3 — Figures

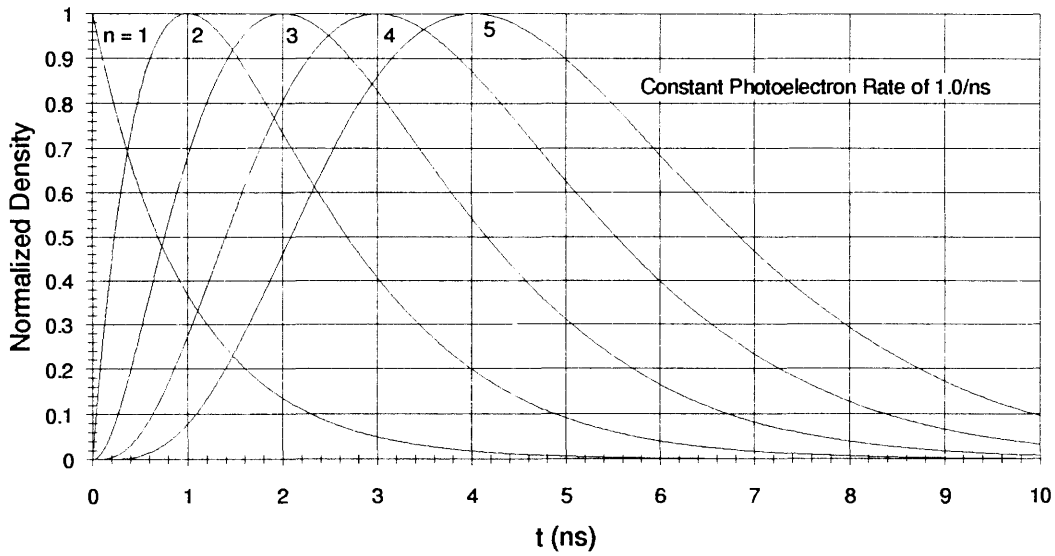

Figure 3-1. Theoretical Poisson Single-Detector Timing Spectrum Versus Photoelectron Trigger Level.

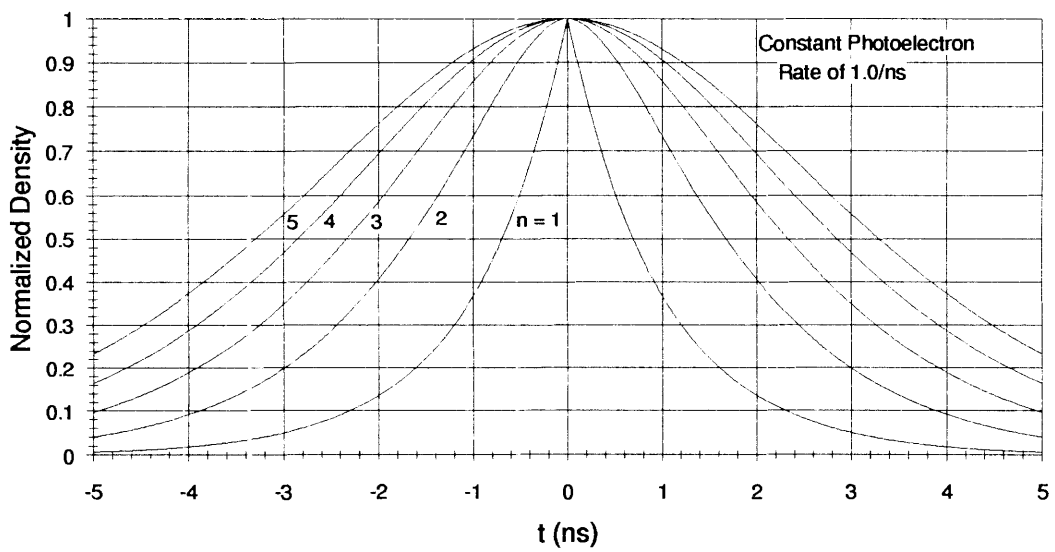

Figure 3-2. Theoretical Poisson Coincident-Detector Timing Spectrum Versus Photoelectron Trigger Level.

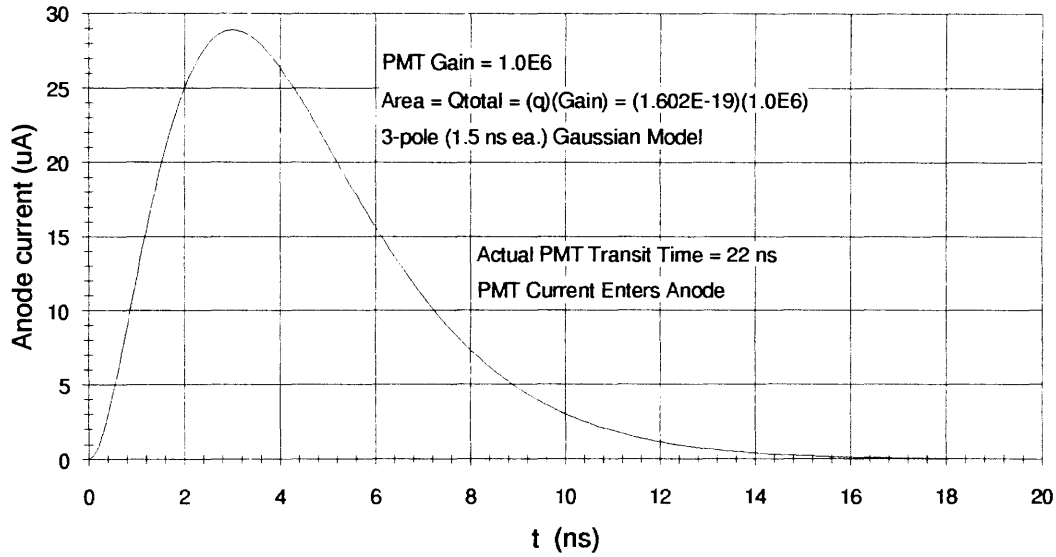

Figure 3-3. Single-Electron Impulse Response for Photomultiplier Tubes used in CTI/Siemens PET Systems.

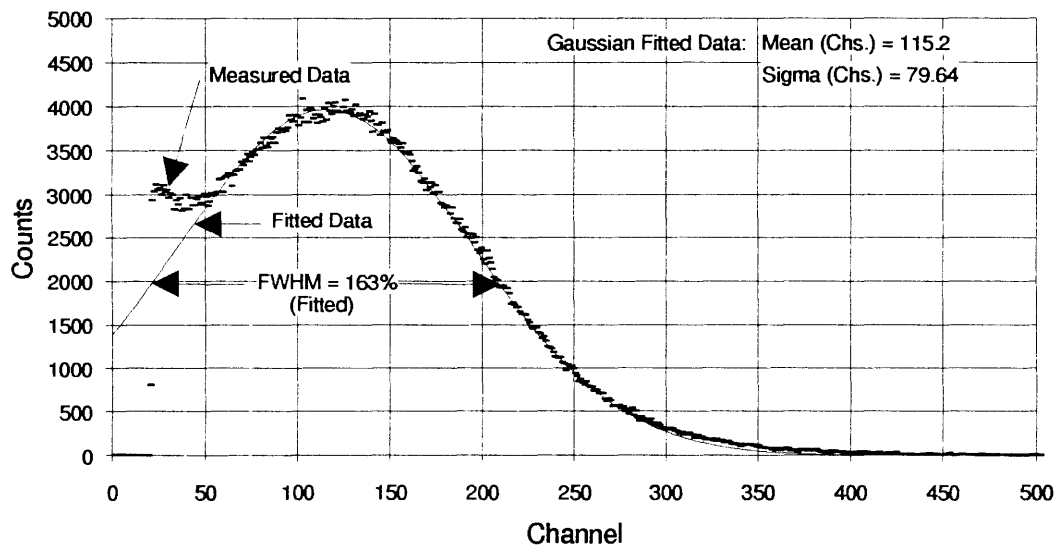

Figure 3-4. Single-Electron Gain Spectrum for the Photomultiplier Tubes Used in CTI/Siemens PET Systems.

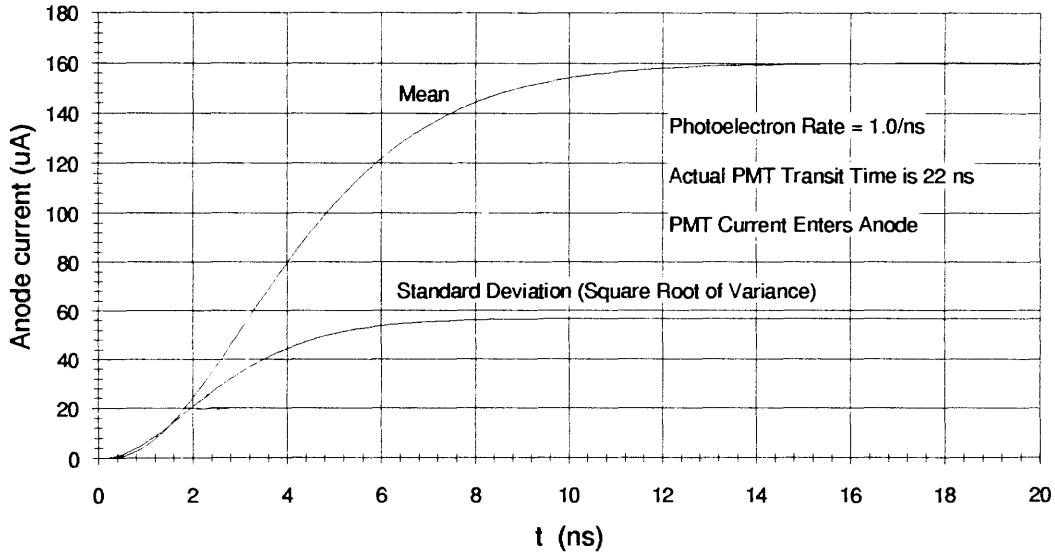

Figure 3-5. BGO/Photomultiplier Scintillation-Detector Mean Output and Standard-Deviation from Campbell's Theorem.

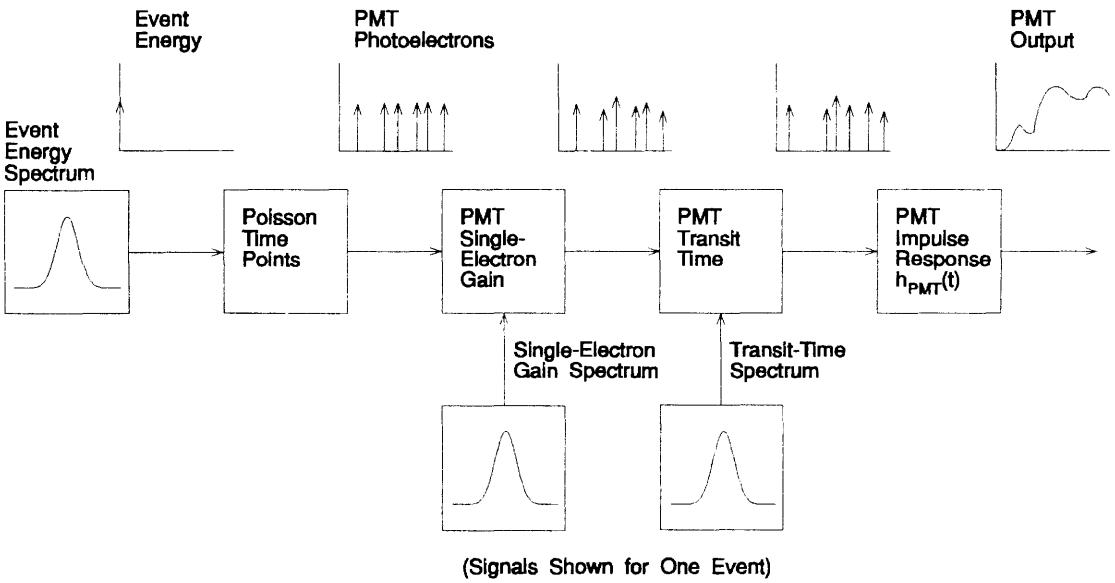

Figure 3-6. Modeling of Scintillation-Detector Output Signals for Monte Carlo Simulation.

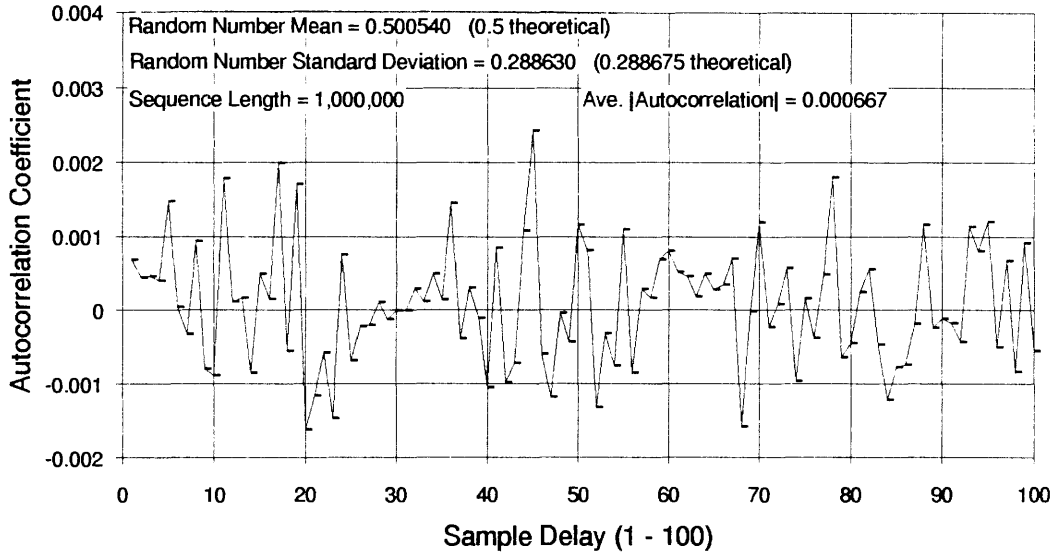

Figure 3-7. Autocorrelation of Random Number Sequence Used in Monte Carlo Simulation.

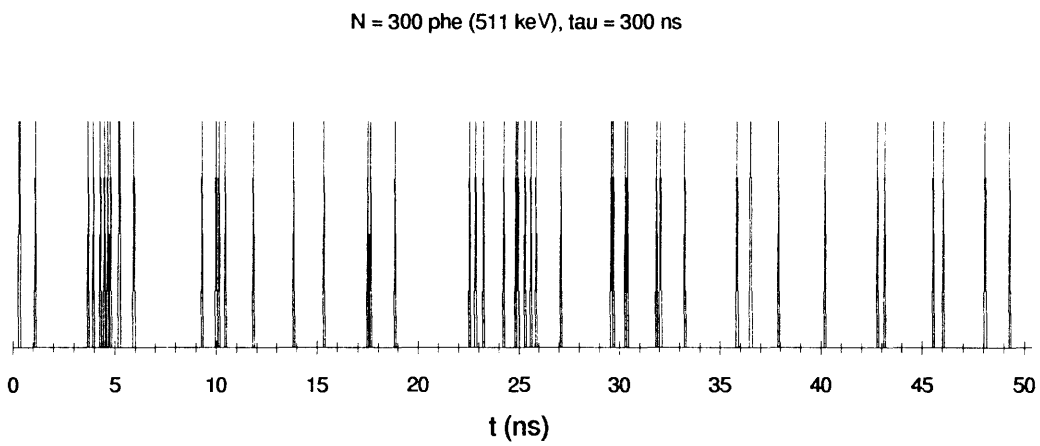

Figure 3-8. Monte Carlo Simulated Photoelectron Emissions for BGO/Photomultiplier Scintillation Detector.

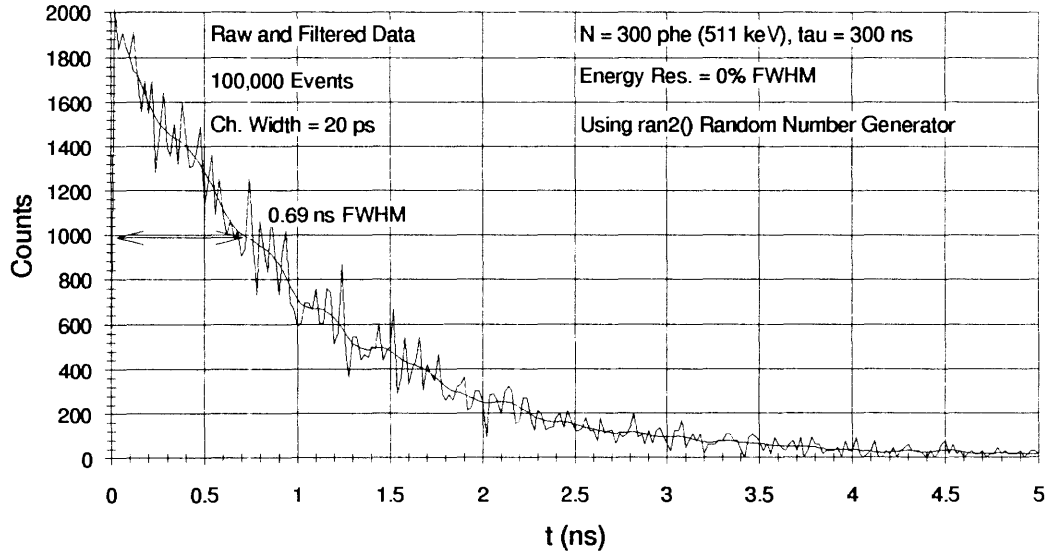

Figure 3-9. Monte Carlo Simulated First-Photoelectron Timing Spectrum (Using Initial Random Number Generator) for BGO/Photomultiplier Scintillation Detector without Photomultiplier Effects.

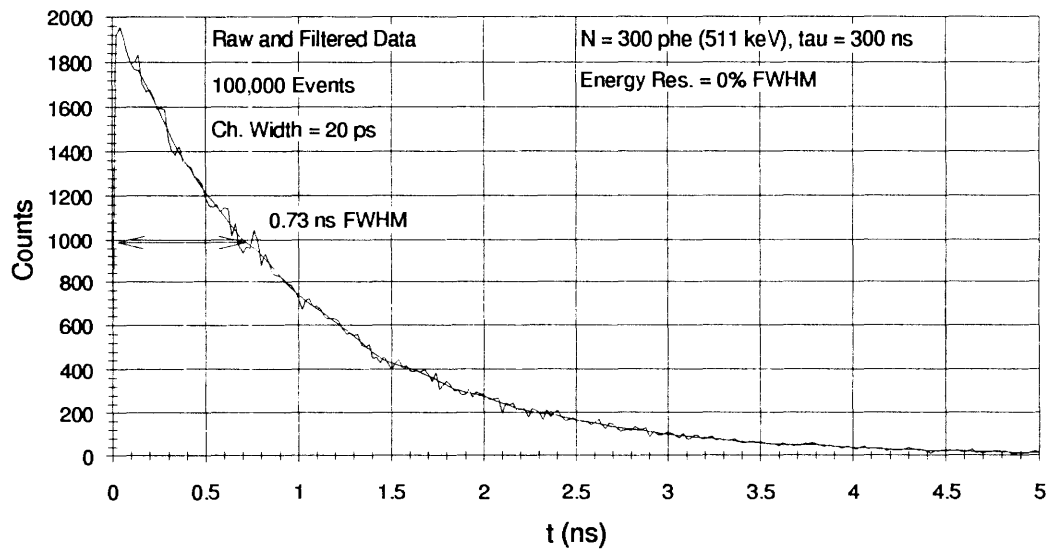

Figure 3-10. Monte Carlo Simulated First-Photoelectron Timing Spectrum for BGO/Photomultiplier Scintillation Detector without Photomultiplier Effects.

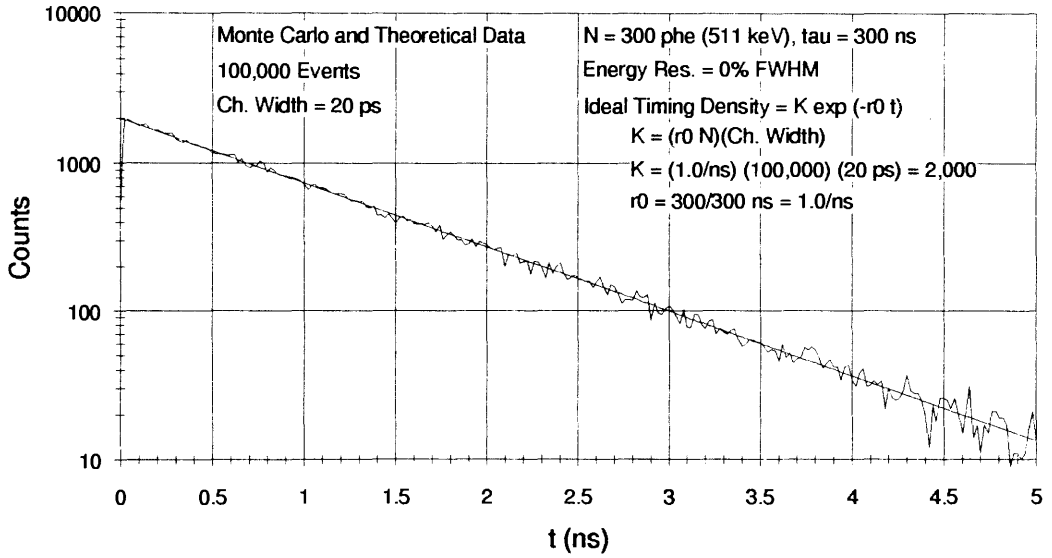

Figure 3-11. Comparison of Monte Carlo Simulated First-Photoelectron Timing Spectrum with Theoretical Poisson Timing Spectrum.

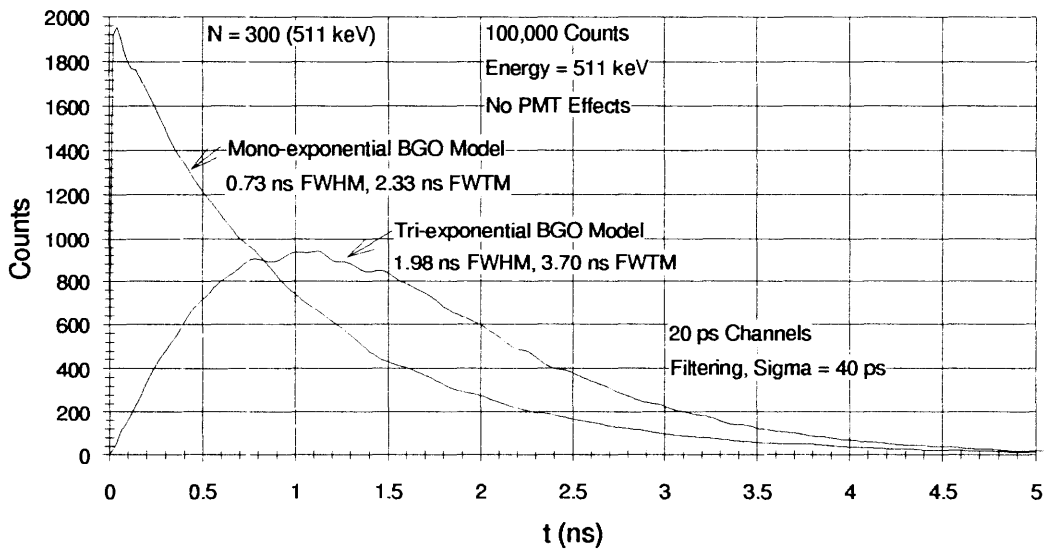

Figure 3-12. Monte Carlo Simulated First-Photoelectron Timing Spectra (Using Mono- and Tri-exponential Scintillation Models) for BGO/Photomultiplier Scintillation Detector without Photomultiplier Effects.

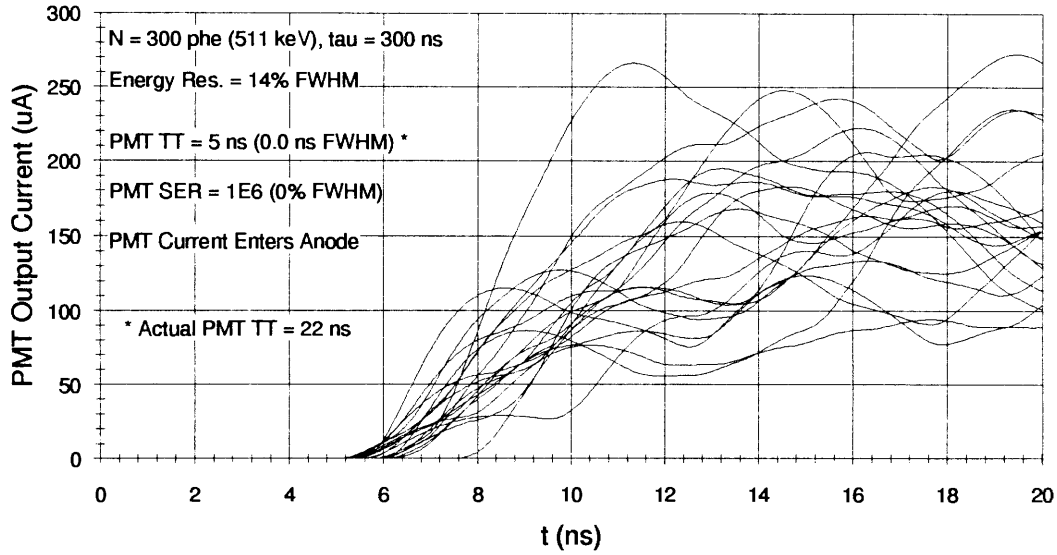

Figure 3-13. Monte Carlo Simulated Outputs for BGO/Photomultiplier Scintillation Detector without Photomultiplier Resolution Effects.

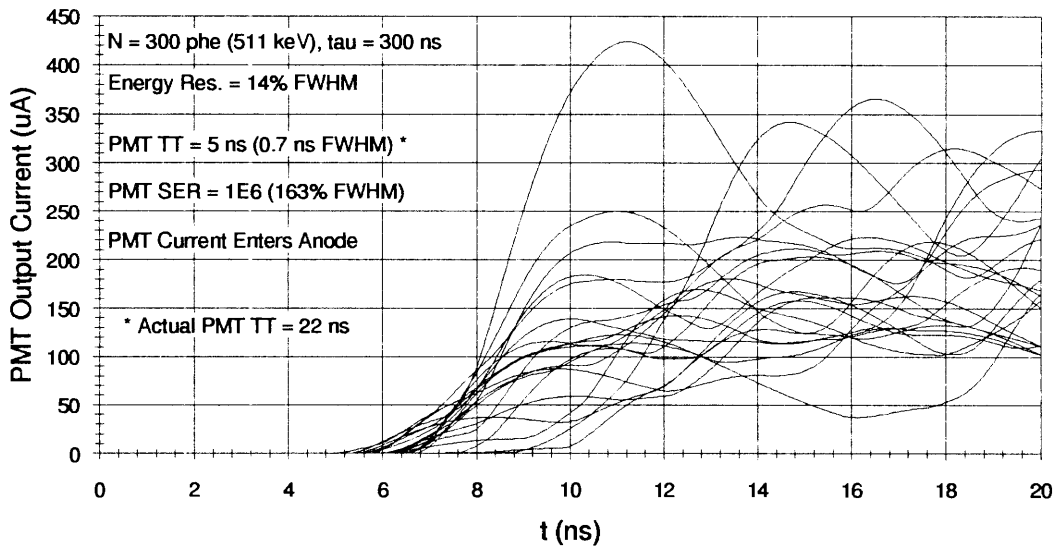

Figure 3-14. Monte Carlo Simulated Outputs for BGO/Photomultiplier Scintillation Detector with Photomultiplier Resolution Effects.

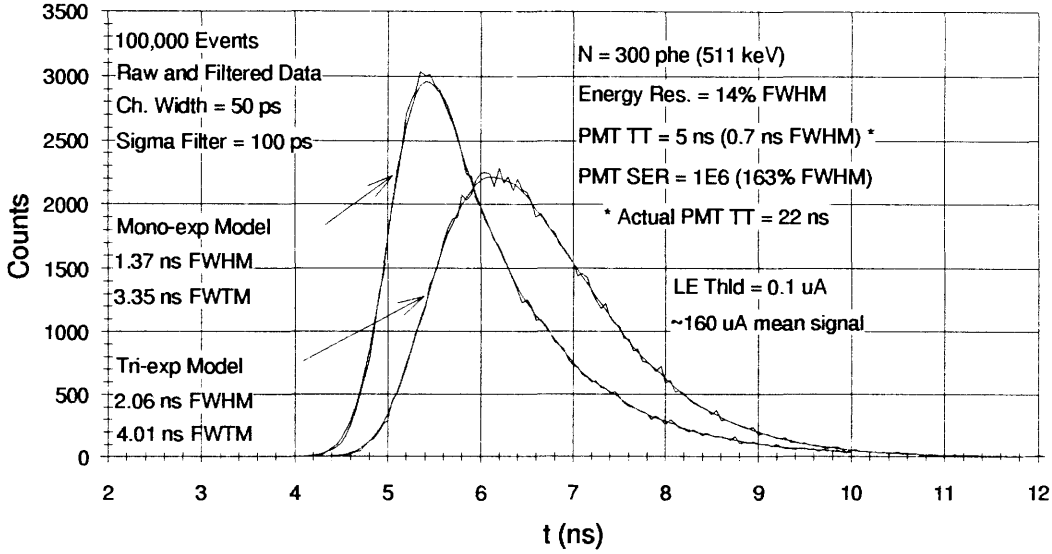

Figure 3-15. Monte Carlo Timing Spectrum (Using Mono- and Tri-exponential Scintillation Models) for First-Photoelectron Timing with BGO/Photomultiplier Scintillation Detector.

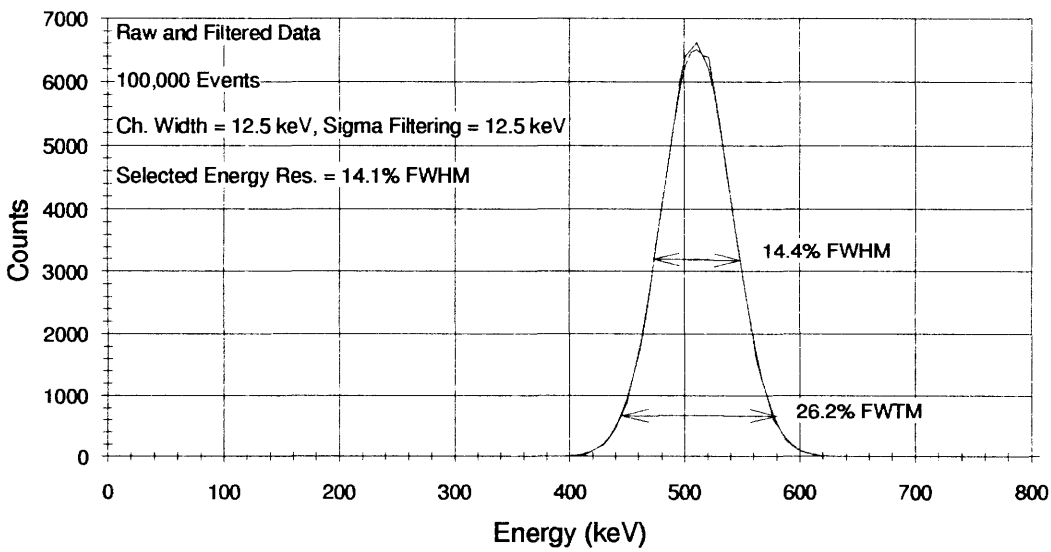

Figure 3-16. Energy Spectrum from Monte Carlo Simulation of First-Photoelectron Timing with BGO/Photomultiplier Scintillation Detector.

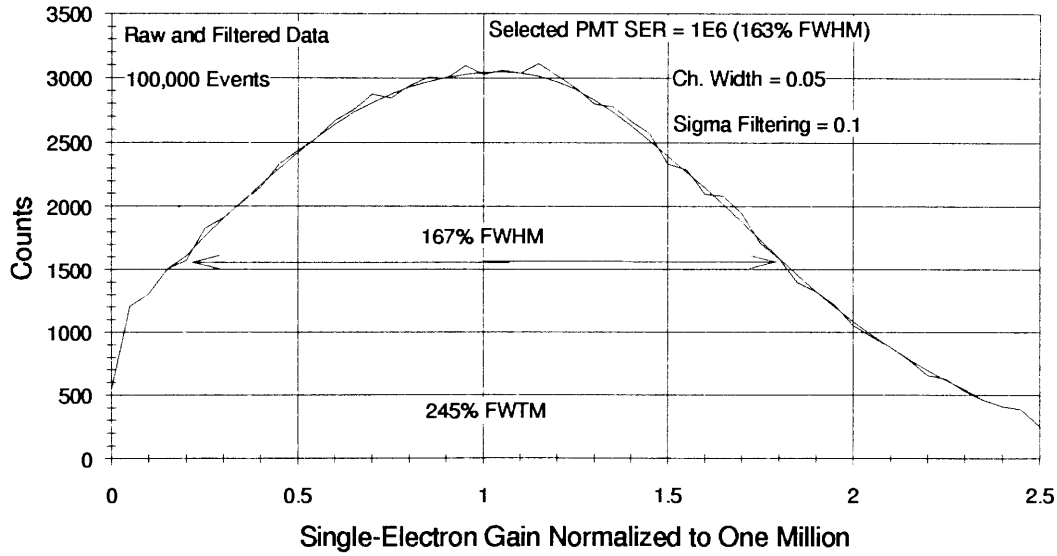

Figure 3-17. Photomultiplier Single-Electron Gain Spectrum from Monte Carlo Simulation of First-Photoelectron Timing with BGO/Photomultiplier Scintillation Detector.

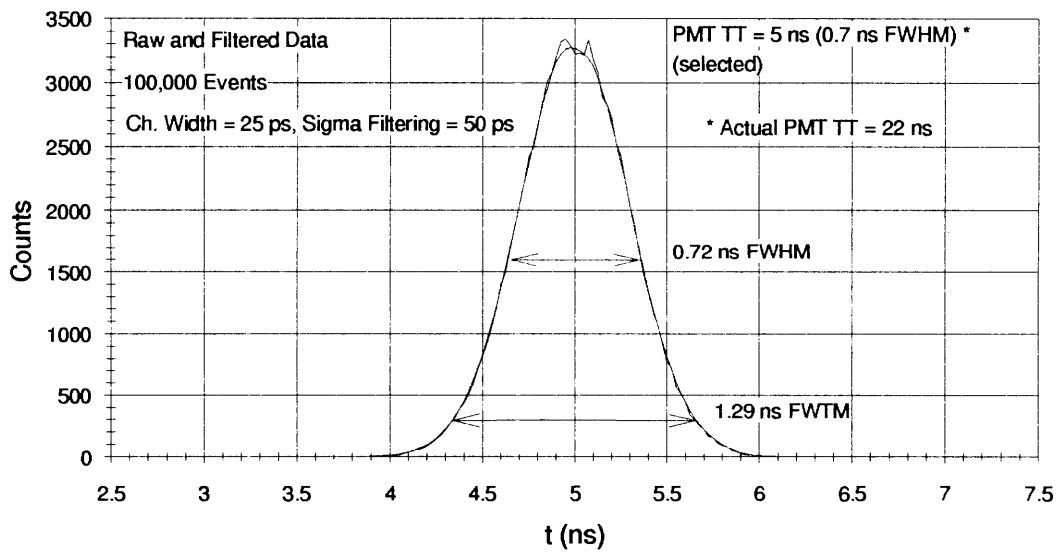

Figure 3-18. Photomultiplier Transit-Time Spectrum from Monte Carlo Simulation of First-Photoelectron Timing with BGO/Photomultiplier Scintillation Detector.

4. CFD Performance And Design

Overview

In this section, CFD performance is described for both delay-line and non-delay-line CFD circuits. CFD shaping-signal underdrive, overdrive, zero-crossing slope, zero-crossing time, and timing jitter performance are first described for the delay-line CFD with linear-edge input signals. Then, single- and two-pole step input signals are introduced which result from the lowpass filtering of a step input. Such signals are representative of scintillation-detector systems where the near step current from detector photoelectrons (following a gamma-ray interaction) is lowpass filtered through the detector and front-end amplification circuits. The performance of delay-line CFD circuits is then given for single- and two-pole step inputs. All CFD performance data is normalized to the input-signal rise-time and amplitude characteristics, and graphs of normalized CFD performance are included in *Appendix A*.

Following the discussion of delay-line CFD performance, non-delay-line CFD circuits are introduced. The Nowlin non-delay-line CFD, which uses highpass networks (approximate differentiators) in place of the delay-line in the delay-line CFD, is discussed first. Then, what is believed to be a new class of non-delay-line CFD circuits is discussed. These circuits use lowpass (approximate integrators) or allpass networks in place of the delay-line in the delay-line CFD and are designated as Binkley CFD circuits. The use of lowpass filters as delay-line approximation filters is discussed in detail, and synthesis of the Binkley non-delay-line CFD circuits is described using Gaussian lowpass delay-line approximation filters. CFD shaping-signal underdrive, overdrive, zero-crossing slope, zero-crossing time, and timing jitter are then given for the non-delay-line CFDs with normalized performance graphs included in *Appendix A*. Tabular comparisons of delay-line, and non-delay-line CFD circuit performance is also presented.

This section concludes with an analysis of delay-line and non-delay-line CFD energy-discrimination and timing performance for scintillation-detector applications. CFD energy-discrimination performance is discussed using Campbell's theorem, where the improvement in energy-discrimination performance present using a constant-fraction comparator circuit delay is discussed. This delay permits increased time for the accumulation of CFD arming statistics. Monte Carlo simulation of CFD timing performance is then given for both delay-line and non-delay-line CFD circuits, where comparable timing performance is shown. Finally, Monte Carlo and measured energy and timing spectra are given for a delay-line CFD. These spectra illustrate good agreement between Monte Carlo and measured results.

Conventional (Delay-Line) CFD

As discussed in *Section 1*, the conventional (delay-line) CFD is a time pick-off circuit which develops a timing signal that is largely insensitive to input-signal amplitude and, in certain cases, rise-time. A block diagram of the delay-line CFD is shown in Figure 1-4 (page 15). The CFD consists of a shaping circuit that subtracts an attenuated version of the input signal from a delayed version to develop a bipolar signal having a fixed zero-crossing time. The shaping signal is then coupled to a comparator for developing the timing signal. A second, arming comparator is used to inhibit CFD triggering on noise. Only those input signals that exceed a preset arming threshold result in a CFD timing output.

Performance with Linear-Edge Signals

Delay-line CFD operation is shown in Figure 1-5 (page 16) for linear-edge, flat-top signals. CFD timing performance can be analyzed by evaluating the signal and noise characteristics of the constant-fraction shaping signal for a given input signal and noise. A circuit model for delay-line CFD is shown in Figure 4-1.

In Figure 1-5 (page 16), two modes of CFD operation are shown: true-constant-fraction mode and amplitude-rise-time-compensated (ARC) mode. In the true-constant-fraction mode, the timing crossing occurs *after* the input signal reaches its final amplitude once the delayed signal reaches a fixed (constant) fraction of the input signal amplitude. Thus, the timing threshold tracks the input signal amplitude at a fixed fraction (f) of the amplitude, resulting in walk-free timing for signals of variable amplitude and fixed rise-time. In the amplitude-rise-time-compensated mode, the timing crossing occurs *before* the input signal reaches its final amplitude. As illustrated in Figure 1-5 (page 16), walk-free timing is provided in amplitude-rise-time-compensated operation for input signals having variable amplitudes and rise-times, provided the rise-times exceed the minimum rise-time selected for operation.

The CFD fraction value must be greater than zero and less than unity ($0 < f < 1$) to obtain proper operation. A fraction value of 20% is standardly used although experimentally-optimized adjustments deviating from this value are sometimes used. The CFD delay value must be greater than zero ($t_d > 0$) to again obtain proper operation. A delay value near the input-signal rise-time is typically used.

Zero-Crossing Time

The shaping-signal zero-crossing time for true constant-fraction operation, from Figure 1-5 (page 16), is given by

$$t_{cf} = t_d + f\,t_r \quad , \tag{4-1}$$

where t_d is the delay associated with the CFD delay line, f is the fraction (gain) associated with the attenuation network, and t_r is the (linear-edge) input-signal rise-time. True-constant-fraction operation is established for a given input-signal rise-time by the selection of circuit delay and fraction in accordance with the inequality:

$$t_{d\ (true\text{-}constant\text{-}fraction)} > t_r\,(1-f) \quad . \tag{4-2}$$

For true-constant-fraction operation at a typical fraction value of 20%, the constant-fraction delay must exceed 80% of the input-signal rise-time.

The timing crossing for amplitude-rise-time-compensated (ARC) operation, from Figure 1-5 (page 16), is given by

$$t_{arc} = \frac{t_d}{1-f} \quad . \tag{4-3}$$

Amplitude-rise-time-compensated operation is established for a given minimum input-signal rise-time by the selection of circuit delay and fraction in accordance with the inequality:

$$t_{d\ (amplitude\text{-}rise\text{-}time\text{-}compensated)} < t_{r\ (min)}\,(1-f) \quad . \tag{4-4}$$

For amplitude-rise-time-compensated operation at a typical fraction value of 20%, the constant-fraction delay must be less than 80% of the minimum input-signal rise-time.

It is advantageous to minimize the CFD time crossing or delay to the extent consistent with good timing jitter, good constant-fraction comparator signal level, and good statistical timing performance. A larger constant-fraction timing delay will result in a correspondingly larger temperature-induced timing drift due to delay-time drift in the CFD delay line. Additionally, excessive CFD delay can cause reduced gating time for systems employing gated energy measurements under control of the CFD output signal.

Shaping-Signal Amplitude and Slope

CFD shaping-signal amplitude and zero-crossing slope affect constant-fraction comparator time-walk performance and, subsequently, CFD output time-walk performance. For practical comparator circuits, it is desirable to maintain signal underdrive, overdrive, and slope at levels that minimize comparator time walk. Comparator time-walk performance as a function of signal underdrive, overdrive, and slope will be discussed in

Section 5. In addition to minimizing constant-fraction comparator time-walk, it is also desirable to minimize CFD timing jitter. Timing jitter is minimized by maximizing the shaping-signal zero-crossing slope to shaping-signal noise ratio.

Shaping-signal underdrive (the peak value the signal goes below zero) for both true-constant-fraction and amplitude-rise-time-compensated operation can be determined from Figure 1-5 (page 16) and is given by

$$V_{cf\,(underdrive)}(t_d < t_r) = -V_{inpk}\, f\,(t_d / t_r) \quad \text{and} \tag{4-5}$$

$$V_{cf\,(underdrive)}(t_d \geq t_r) = -V_{inpk}\, f \quad . \tag{4-6}$$

Shaping-signal overdrive (the peak value the signal goes above zero) for both true-constant-fraction and amplitude-rise-time-compensated operation can also be determined from Figure 1-5 (page 16) and is given by

$$V_{cf\,(overdrive)} = V_{inpk}\,(1 - f) \quad . \tag{4-7}$$

For true-constant-fraction operation with a typical fraction (f) of 20%, shaping-signal underdrive is 20% of the input-signal amplitude compared to 80% for the overdrive. Since comparator response-time is usually more dependent on signal overdrive than signal underdrive (discussed in *Section 5*), a larger comparator input overdrive is desirable.

Shaping-signal zero-crossing slope can be determined from Figure 1-5 (page 16) and is given by

$$K_{cf\,(true\text{-}constant\text{-}fraction)} = V_{inpk} / t_r \quad \text{and} \tag{4-8}$$

$$K_{cf\,(amplitude\text{-}rise\text{-}time\text{-}compensated)} = V_{inpk}(1 - f) / t_r \quad . \tag{4-9}$$

Shaping-signal zero-crossing slope is equal to input-signal slope for true-constant-fraction operation and is 80% of the input-signal slope for amplitude-rise-time-compensated operation assuming a typical fraction of 20%. The preservation of input-signal slope at the shaping signal is an advantage of the delay-line CFD compared to the non-delay-line CFD circuits that will be discussed later. Signal slope is preserved because an ideal delay line provides time delay without limiting signal bandwidth.

Timing-Jitter Performance

The timing-jitter performance of the CFD is found from the ratio of shaping-signal noise to shaping-signal slope at the timing crossing. The mean-square shaping-signal noise (from Figure 4-1) is given by

$$\sigma_{vcf}^2 = \sigma_{vin}^2\left(1^2 + f^2 - 2f\,\Phi_{in}(t_d)/\sigma_{vin}^2\right) , \tag{4-10}$$

where σ_{vin}^2 is the mean-square input noise (zero-mean Gaussian noise is assumed), $\Phi_{in}(t_d)$ is the input-noise autocorrelation evaluated for a delay time equal to the constant-fraction delay t_d, and f is the fraction value [1]. The term $\Phi_{in}(t_d)/\sigma_{vin}^2$ is the input-noise autocorrelation coefficient which has values between ±1 with a value of zero indicating no noise autocorrelation. CFD rms timing jitter is given by

$$\sigma_{t\ (true\text{-}constant\text{-}fraction)} = \frac{\sigma_{vin}\sqrt{1^2 + f^2 - 2f\,\Phi_{in}(t_d)/\sigma_{vin}^2}}{V_{inpk}/t_r} \quad \text{and} \tag{4-11}$$

$$\sigma_{t\ (amplitude\text{-}rise\text{-}time\text{-}compensated)} = \frac{\sigma_{vin}\sqrt{1^2 + f^2 - 2f\,\Phi_{in}(t_d)/\sigma_{vin}^2}}{V_{inpk}(1-f)/t_r} , \tag{4-12}$$

where the denominator expressions are equal to the zero-crossing shaping-signal slope given in Equations 4-8 and 4-9, and V_{inpk} is the input signal amplitude. It is interesting to note that CFD timing jitter is greater than leading-edge-discriminator timing jitter for white input noise ($\Phi_{in}(t_d)/\sigma_{vin}^2$ is equal to zero for white input noise) because of additional noise introduced by the combination of the delayed and attenuated signals. Additionally, CFD timing jitter is greater for amplitude-rise-time-compensated operation compared to true-constant-fraction operation because of the lower shaping-signal slope at the timing crossing. For white input noise and true-constant-fraction operation at a fraction value of 20%, CFD (rms) timing jitter is only 2% higher than leading-edge-discriminator timing jitter.

DC Baseline Effects on Timing Performance

The CFD analysis previously considered assumes that signals start from a zero-level baseline. Actual circuits may have nonzero DC baseline levels due to AC coupling of high count-rate pulses or electronic-circuit offsets in cases where DC coupling or baseline restorer circuits are used. A DC baseline level causes the CFD timing crossing to shift from the theoretical value and contributes to time walk which is not theoretically present for zero-

baseline levels. The shift in timing crossing due to DC baseline level can be determined from Figure 1-5 (page 16) by observing the DC shift in the shaping signal.

The CFD timing crossing for linear-edge input signals having a DC baseline is given by

$$t_{cf\,(true\text{-}constant\text{-}fraction)} = t_d + f t_r \quad -(V_{baseline} / V_{inpk}) t_r (1 - f) \quad \text{and} \tag{4-13}$$

$$t_{arc\,(amplitude\text{-}rise\text{-}time\text{-}compensated)} = t_d / (1 - f) \quad -(V_{baseline} / V_{inpk}) t_r \quad , \tag{4-14}$$

where $V_{baseline}$ is the DC baseline level. The last term in each equation gives the shift in the timing crossing due to the DC baseline level. This timing shift varies with input-signal amplitude resulting in time walk for both true-constant-fraction and amplitude-rise-time-compensated operation where amplitude insensitivity would normally be present. Additionally, this timing shift varies with input-signal rise-time resulting in time walk for amplitude-rise-time-compensated operation where rise-time insensitivity would normally be present.

Table 4-1 illustrates CFD timing error for varying-amplitude input pulses having a DC baseline. A signal rise-time (linear edge) of 10 ns, DC baseline level of 10 mV, constant-fraction delay of 10 ns, and fraction of 20% is used for the data in Table 4-1. This selection of delay and fraction value gives true-constant-fraction timing. The CFD timing error ranges from -0.8 ns to -0.08 ns for input levels of 100 mV to 1000 mV resulting in a time

Table 4-1. Delay-Line CFD Timing Errors Caused by DC Baseline Error.

V_{inpk}	Timing Error (from 12 ns)
100 mV	-0.8 ns
200 mV	-0.4 ns
500 mV	-0.16 ns
1000 mV	-0.08 ns
Walk (100 mV-1000 mV):	+0.72 ns
Baseline = +10 mV, Signal Rise-Time (linear edge) = 10 ns Constant-Fraction: Delay = 10 ns, Fraction = 20%	

walk of +0.72 ns over the input-signal range. This time walk is 7.2% of the input-signal rise-time and illustrates that significant CFD timing degradation can occur for DC baseline levels considerably below the input-signal levels.

Performance with Lowpass-Filtered Step Signals

Description of Lowpass-Filtered Step Signals

In the preceding discussion, CFD performance has been evaluated for linear-edge input signals. Although linear-edge signals are characteristic of coaxial semiconductor-detector signals for event interactions near the center of the depletion region [2, 3, 4], linear-edge signals are not characteristic of scintillation detector signals.

As discussed in *Section 3*, scintillation detector signals consist of a nearly instantaneous rise followed by an exponential decay which is characteristic of the scintillator. Since timing is usually derived on the leading-edge of the detector signal, the detector signal can be approximated as a step input filtered by a lowpass filter representing the response of the light detector (photomultiplier tube or photodiode detector) and subsequent amplification circuits. Both single- and two-pole lowpass-filtered step inputs will be considered for CFD performance. It will be assumed that both a step input and white-noise source are lowpass filtered to produce an input signal with noise that is characteristic of the signal bandwidth.

Delay-line CFD performance is catalogued in *Appendix A - Catalog of Normalized CFD Performance for Lowpass-Filtered Step Inputs* for single- and two-pole lowpass-filtered step inputs. A discussion of the characteristics of single- and two-pole lowpass-filtered step inputs follows.

The lowpass-filtered step-input signals are described in Laplace notation by

$$V_{in\ (single\text{-}pole\ input)}(s) = V_{inpk}\left[\frac{1}{s(1+st_{in})}\right] \text{ and} \tag{4-15}$$

$$V_{in\ (two\text{-}pole\ input)}(s) = V_{inpk}\left[\frac{1}{s(1+st_{in}/\sqrt{2})^2}\right], \tag{4-16}$$

where t_{in} is the time-constant associated with input bandwidth limiting, and V_{inpk} is the peak input-signal amplitude. The time-constant associated with each pole for the two-pole input is reduced by the square-root-of-two from the composite input-signal rise-time (t_{in}) to maintain a nearly equal signal rise-time (10 - 90%) for both the single- and two-pole inputs.

The time-domain input signals are found from the inverse Laplace transforms of Equations 4-15 and 4-16 and are given by

$$v_{in\ (single\text{-}pole\ input)}(t) = V_{inpk}\left(1 - e^{-t/t_{in}}\right)u(t) \quad \text{and} \tag{4-17}$$

$$v_{in\ (two\text{-}pole\ input)}(t) = V_{inpk}\left(1 - e^{-\sqrt{2}t/t_{in}}\,(1 + \sqrt{2}\,t / t_{in})\right)u(t) \quad . \tag{4-18}$$

Peak input-signal slope is found from the maximum value of the input-signal time derivative and is given by

$$K_{inpk\ (single\text{-}pole\ input)}(t = 0) = V_{inpk} / t_{in} \quad \text{and} \tag{4-19}$$

$$K_{inpk\ (two\text{-}pole\ input)}(t = t_{in} / \sqrt{2}) = \sqrt{2}\,e^{-1}\,V_{inpk} / t_{in} \quad . \tag{4-20}$$

The peak input-signal slope for the single-pole input occurs at 0% of the amplitude (at the beginning); the peak input-signal slope for the two-pole input occurs at 26.4% of the amplitude. The peak input-signal slope for the two-pole input is equal to 52% of that for the single-pole input, each input signal having the same composite time-constant, t_{in}.

The noise present with the lowpass-filtered step input is described by noise-power spectral density as

$$S_{in\ (single\text{-}pole\ input)}(\omega) = \frac{e_n^2}{2}\left[\frac{1}{1 + (\omega t_{in})^2}\right] \quad \text{and} \tag{4-21}$$

$$S_{in\ (two\text{-}pole\ input)}(\omega) = \frac{e_n^2}{2}\left[\frac{1}{\left(1 + (\omega t_{in} / \sqrt{2})^2\right)^2}\right] \quad , \tag{4-22}$$

where e_n is the single-sided input-noise density for the lowpass-filtered white-noise source. The total mean-square noise present with the lowpass-filtered step input is given by

$$\sigma_{vin}^2 = \frac{1}{2\pi}\int_{-\infty}^{\infty} S_{in}(\omega)\,d\omega \quad , \text{or} \tag{4-23}$$

$$\sigma^2_{vin\ (single\text{-}pole\ input)} = \frac{e_n^2}{4t_{in}} \quad , \text{and} \tag{4-24}$$

$$\sigma^2_{vin\ (two\text{-}pole\ input)} = \frac{e_n^2}{8t_{in}\ /\ \sqrt{2}} \quad . \tag{4-25}$$

The total rms input-signal noise for the two-pole input is 84.1% of that for the single-pole input, each input-signal having the same composite time-constant, t_{in}.

The minimum timing jitter associated with the single- and two-pole step inputs is equal to the total rms input noise divided by the peak input-signal slope. The minimum timing jitter is given by

$$\sigma_{tin\ (min,\ single\text{-}pole\ input)}(t=0) = \frac{\sqrt{\dfrac{e_n^2}{4t_{in}}}}{\dfrac{V_{inpk}}{t_{in}}} \quad , \text{or} \tag{4-26}$$

$$\sigma_{tin\ (min,\ single\text{-}pole\ input)}(t=0) = \frac{e_n\sqrt{t_{in}}}{2V_{inpk}} \quad , \text{and} \tag{4-27}$$

$$\sigma_{tin\ (min,\ two\text{-}pole\ input)}(t=t_{in}\ /\ \sqrt{2}) = \frac{\sqrt{\dfrac{e_n^2}{8t_{in}\ /\ \sqrt{2}}}}{\dfrac{\sqrt{2}\,e^{-1}\,V_{inpk}}{t_{in}}} \quad , \text{or} \tag{4-28}$$

$$\sigma_{tin\ (min,\ two\text{-}pole\ input)}(t=t_{in}\ /\ \sqrt{2}) = \frac{e_n\sqrt{t_{in}\ /\ \sqrt{2}}}{2\sqrt{2}\,e^{-1}\,V_{inpk}} \quad . \tag{4-29}$$

The minimum rms timing jitter for the two-pole input signal is 161.7% of that for the single-pole input signal, each input signal having the same composite time-constant, t_{in}. The increase in timing jitter is due to the lower peak slope for the two-pole input signal.

Derivation of Shaping Signal

The CFD circuit model in Figure 4-1 will be used to find the shaping signal for single- and two-pole step-input signals. The shaping signal can be found from the CFD input signal and transfer function $H_{cf}(s)$ as shown in Figure 4-1. The transfer function for the delay-line CFD is given by

$$H_{cf}(s) = \left(e^{-st_d} - f\right) \ , \tag{4-30}$$

where t_d is the constant-fraction delay and f is the fraction. The shaping signal for the single-pole step input (Equations 4-15 and 4-17) and the transfer function (Equation 4-30) is given by

$$V_{cf}(t) = V_{inpk}\left[\left(1 - e^{-(t-t_d)/t_{in}}\right)u(t-t_d) \ - f\left(1 - e^{-t/t_{in}}\right)u(t)\right] \ . \tag{4-31}$$

Equation 4-31 can be rewritten for time before and after the constant-fraction delay giving

$$v_{cf} \ (0 \le t \le t_d) \ = \ - V_{inpk} f \left(1 - e^{-t/t_{in}}\right) \text{ and} \tag{4-32}$$

$$v_{cf} \ (t > t_d) \ = \ V_{inpk}\left((1-f) - e^{-t/t_{in}}\left(e^{t_d/t_{in}} - f\right)\right) \ . \tag{4-33}$$

The shaping signal for the delay-line CFD along with full circuit-performance data is given in *Appendix A - Catalog of Normalized CFD Performance for Lowpass-Filtered Step Inputs*. Additionally, *Appendix A* contains full circuit-performance data for non-delay-line CFDs that will be introduced later. The delay-line CFD data of *Appendix A* will be referred to in the following discussion. Later in this section, after introduction of the non-delay-line CFDs, a comparison of delay-line and non-delay-line CFD performance will be given.

Both a single-pole step input and the corresponding CFD shaping signal is shown in Figure A-1 (page 262) as a function of time (t/t_{in}) normalized to the input signal time-constant. A constant-fraction delay was chosen to give a zero-crossing time equal to twice the input-signal time-constant ($t_{cf} = 2t_{in}$) for a fraction value of 20%. In Figure A-7 (page

266), a two-pole step input and the corresponding CFD shaping signal is shown. Again, a constant-fraction delay was chosen to give a zero-crossing time equal to twice the input-signal time-constant ($t_{cf} = 2t_{in}$) for a fraction value of 20%. The signals shown in Figures A-1 and A-7 illustrate CFD shaping of unipolar input pulses into bipolar timing pulses with clearly defined zero-crossing times.

Zero-Crossing Time

Equation 4-33 is used for finding delay-line CFD zero-crossing time for single-pole step inputs. The zero-crossing time is greater than the constant-fraction delay (t_d) since the shaping signal is negative for times less than the constant-fraction delay. The zero-crossing time can be solved in closed form for the single-pole step input because only one simple exponential term is present. The zero-crossing time is given by

$$t_{cf} = t_{in} \ln\left(\frac{e^{t_d/t_{in}} - f}{1 - f}\right) . \qquad (4\text{-}34)$$

The CFD timing crossing given in Equation 4-34 for a single-pole step input is independent of the input-signal amplitude but is not independent of the input-signal time-constant (t_{in}) or the input-signal 10 - 90% rise-time (~$2.2t_{in}$). It will be shown later that there is no constant-fraction delay ($t_d > 0$) or fraction ($0 < f < 1$) that will give rise-time independent timing as was available for linear-edge input signals (using the amplitude-rise-time-compensated mode).

The CFD timing crossing for single-pole step inputs (Equation 4-34) is shown in Figure A-2 (page 262) as a function of the constant-fraction delay (t_d) and fraction (f). Both the CFD timing crossing (t_{cf}/t_{in}) and the constant-fraction delay (t_d/t_{in}) are normalized to the input-signal time-constant (t_{in}). Since CFD shaping-network design is a filter design problem, normalization typical of filter design is advantageous to permit rapid scaling of circuit performance for any input-signal time-constant.

In addition to the CFD timing crossing for single-pole step inputs (Figure A-2, page 262), the timing crossing for two-pole step inputs is shown in Figure A-8 (page 266). The timing crossing for both the single-pole and two-pole step inputs was found numerically by specially-developed computer programs that initiated SPICE runs to generate CFD shaping signals. The programs then performed analysis to find the zero-crossing time, signal underdrive, zero-crossing slope, output noise, and timing jitter. Although closed-form

analysis is available for the zero-crossing time for single-pole step inputs, no closed-form analysis is available for two-pole step inputs which mandates the use of numerical analysis.

The CFD timing crossing for single-pole step inputs (Figure A-2, page 262) and two-pole step inputs (Figure A-8, page 266) increases monotonically with constant-fraction delay time (t_d) because the shaping signal cannot zero cross until after the delayed signal is present. The timing crossing increases monotonically with fraction value (f) because a higher fraction value corresponds to triggering on a higher fraction of the delayed signal.

The variation in CFD timing crossing with varying input-signal time-constant or 10 - 90% rise-time (~$2.2t_{in}$) can be determined in closed form for the single-pole step input. This is done by differentiating Equation 4-34 with respect to the input-signal time-constant giving

$$\frac{\delta}{\delta t_{in}} t_{cf} = \ln\left(\frac{e^{t_d/t_{in}} - f}{1-f}\right) - \frac{t_d / t_{in}}{1 - fe^{-t_d/t_{in}}} \quad . \tag{4-35}$$

Although not obvious, the timing sensitivity to input-signal time-constant given by Equation 4-35 has a value of zero for normalized constant-fraction delay (t_d/t_{in}) equal to zero and increases monotonically for increasing values of normalized constant-fraction delay for all allowable fraction values ($0 < f < 1$). This indicates that no CFD delay or fraction value is available for rise-time insensitive timing operation.

A plot of timing sensitivity to input-signal time-constant (Equation 4-35) is shown in Figure 4-2 as a function of normalized constant-fraction delay for a fraction (f) of 20%. The timing sensitivity to varying input-signal time-constants is minimum for minimum normalized CFD delay which is consistent with the shorter delay required for (amplitude-)rise-time-compensated timing with linear-edge input signals compared to nonrise-time-compensated timing (true-constant-fraction timing). It will be shown later that optimum statistical timing performance for scintillation detectors also occurs at minimum constant-fraction delay. Both input-signal time-constant sensitivity and detector statistical errors are minimized for "short" constant-fraction delays because timing occurs early on the signal. Unfortunately, as will be illustrated later, CFD shaping-signal level, shaping-signal slope, and timing jitter are not optimum for arbitrarily short constant-fraction delays.

The timing sensitivity to input-signal time-constant (Figure 4-2) for a single-pole step input is 12.5% for a fraction value of 20% and a constant-fraction delay ($t_d = 1.805t_{in}$) that

gives a zero-crossing time ($t_{cf} = 2t_{in}$) of twice the input-signal time-constant. This indicates a timing error of approximately +56.8 ps (0.454 ns x 0.125) for an input-signal rise-time (10 - 90%) increase of 1 ns corresponding to an input-signal time-constant increase of 0.454 ns (1 ns/2.2). In order to estimate timing sensitivity to input-signal time-constant, it is necessary to ensure that the change in input-signal time-constant is sufficiently small to maintain operation over a linear portion of the CFD timing crossing given in Equation 4-34.

Shaping-Signal Amplitude and Slope

CFD shaping-signal underdrive (the peak value the signal goes negative) for single-pole step inputs occurs at time equal to the constant-fraction delay ($t = t_d$) and is given from Equation 4-32 or 4-33 as

$$V_{cf\,(underdrive)} = -V_{inpk}\, f\left(1 - e^{-t_d/t_{in}}\right) . \qquad (4\text{-}36)$$

CFD shaping-signal underdrive is shown in Figure A-3 (page 263) for single-pole step-input signals and in Figure A-9 (page 267) for two-pole step-input signals. Shaping-signal underdrive is shown for different fraction values (f) as a function of constant-fraction delay (t_d/t_{in}) normalized to input-signal time-constant. Shaping-signal underdrive ($V_{cf\,(underdrive)}/V_{inpk}$) is normalized to the input-signal amplitude to illustrate the relative amount of underdrive present.

CFD shaping-signal underdrive (Figures A-3, page 263 and A-9, page 267) increases monotonically (negatively) with increasing constant-fraction delay and fraction for both single-pole and two-pole step inputs. Additionally, the normalized shaping-signal underdrive for both single-pole and two-pole step inputs approaches a maximum value of $-f$ for constant-fraction delays greater than $5t_{in}$. Although the shaping-signal underdrive is similar for both single-pole and two-pole step inputs, the underdrive is lower at low values of constant-fraction delay ($t_d/t_{in} < 2$) for two-pole step inputs because of the signal delay present in two-pole step-input signals (this can been seen in a comparison of Figures A-1, page 262, and A-7, page 266). Shaping-signal underdrive is (-)16.7% and (-)12.6% of the input-signal amplitude respectively for single- and two-pole step-input signals for a fraction value of 20% and a constant-fraction delay that gives a zero-crossing time of twice the input-signal time-constant ($t_{cf} = 2t_{in}$).

CFD shaping-signal overdrive occurs for time approaching infinity and is given from Equation 4-33 as

$$V_{cf\,(overdrive)} = V_{inpk}(1 - f) \quad . \tag{4-37}$$

Shaping-signal overdrive is equal to the CFD DC gain multiplied by the input-signal amplitude. Shaping-signal overdrive normalized to input-signal amplitude is simply equal to the CFD DC gain $(1 - f)$ and is not plotted in the data contained in *Appendix A*.

The CFD shaping-signal zero-crossing slope is found from the time-derivative of the shaping signal (Equation 4-33) and is given for single-pole step inputs by

$$\frac{d}{dt} v_{cf}(t \geq t_d) = \frac{V_{inpk}}{t_{in}} \left((e^{t_d/t_{in}} - f) e^{-t/t_{in}} \right) \quad . \tag{4-38}$$

Only times greater than the constant-fraction delay time $(t > t_d)$ are considered since the zero-crossing occurs after the delayed signal appears at the output of the delay line. The shaping-signal zero-crossing slope, found by evaluating Equation 4-38 for the zero-crossing time given in Equation 4-34, is given by

$$K_{cf} = V_{inpk}(1 - f) / t_{in} \quad . \tag{4-39}$$

The zero-crossing slope is independent of the constant-fraction delay and is equal to the input-signal slope at the fraction (f) of the input-signal amplitude. As illustrated for the case of linear-edge inputs, the delay-line CFD essentially preserves input-signal slope for the typical fraction of 20%.

CFD shaping-signal zero-crossing slope is shown in Figure A-4 (page 263) for single-pole step-input signals and in Figure A-10 (page 267) for two-pole step-input signals. Zero-crossing slope is shown for different fraction values (f) as a function of constant-fraction delay normalized to input-signal time-constant (t_d/t_{in}). Additionally, zero-crossing slope (K_{cf}/K_{inpk}) is normalized to the peak input-signal slope to illustrate the degradation of input-signal slope present.

Shaping-signal zero-crossing slope for single-pole step inputs (Figure A-4, page 263) is, as mentioned, independent of the constant-fraction delay. The zero-crossing slope (Equation 4-39), when normalized to the peak input-signal slope, is simply equal to $(1 - f)$ since the peak input-signal slope is V_{inpk}/t_{in} (Equation 4-19). Shaping-signal zero-crossing slope for two-pole step inputs (Figure A-10, page 267) increases monotonically with increasing constant-fraction delay and generally peaks for fraction values between 20 - 40% which is in

the vicinity of input-signal amplitude (26.4%) where signal slope is maximum. The zero-crossing slope is equal to 80% and 85.2% of the peak input-signal slope respectively for single- and two-pole step-input signals for a fraction value of 20% and a constant-fraction delay that gives a zero-crossing time of twice the input-signal time-constant ($t_{cf} = 2t_{in}$).

Timing-Jitter Performance

The mean-square shaping-signal noise (Equation 4-10) is given by

$$\sigma_{vcf}^2 = \sigma_{vin}^2 \left(1^2 + f^2 - 2f\,\Phi_{in}(t_d)/\sigma_{vin}^2\right) \quad , \tag{4-40}$$

where σ_{vin}^2 is the mean-square input noise (zero-mean Gaussian noise is assumed), $\Phi_{in}(t_d)$ is the input-noise autocorrelation evaluated for a delay time equal to the constant-fraction delay t_d, and f is the constant-fraction fraction [1]. The term $\Phi_{in}(t_d)/\sigma_{vin}^2$ is the input-noise autocorrelation coefficient which, for the single-pole input noise-power spectral density given in Equation 4-21, is given by

$$\Phi_{in}(t_d)/\sigma_{vin}^2 = \frac{\sigma_{vin}^2\, e^{-|t_d|/t_{in}}}{\sigma_{vin}^2} \quad \text{or} \tag{4-41}$$

$$\Phi_{in}(t_d)/\sigma_{vin}^2 = e^{-|t_d|/t_{in}} \quad . \tag{4-42}$$

The absolute-value operation in the preceding equations is included for mathematical completeness even though the constant-fraction delay is physically positive. Substituting Equation 4-42 into Equation 4-40 gives the shaping-signal mean-square noise which is expressed as

$$\sigma_{vcf}^2 = \sigma_{vin}^2 \left(1^2 + f^2 - 2f\, e^{-|t_d|/t_{in}}\right) \quad . \tag{4-43}$$

The shaping-signal rms noise can be normalized to the input-signal rms noise to illustrate the relative increase or decrease in rms noise caused by the CFD shaping network. The normalized shaping-signal rms noise for a single-pole step input is given by

$$\frac{\sigma_{vcf}}{\sigma_{vin}} = \sqrt{1^2 + f^2 - 2f\, e^{-|t_d|/t_{in}}} \quad . \tag{4-44}$$

Normalized CFD shaping-signal rms noise is shown in Figure A-5 (page 264) for single-pole input noise and in Figure A-11 (page 268) for two-pole input noise. The normalized noise is shown for different fraction values (f) as a function of normalized constant-fraction delay (t_d/t_{in}). Shaping-signal noise increases with increasing constant-fraction delay because of reduced correlated-noise cancellation in the attenuated-signal and delayed-signal path. Shaping-signal noise increases most dramatically with increasing constant-fraction delay for large fraction values because of significant correlated-noise cancellation at short delay values changing to significant uncorrelated-noise addition at long delay values. The normalized output rms noise is 98.7% and 94.4% respectively for a single- and two-pole input noise source for a fraction value of 20% and a constant-fraction delay that gives a zero-crossing time of twice the input-signal time-constant ($t_{cf} = 2t_{in}$).

Timing jitter for the single-pole step input is found from the shaping-signal noise (Equation 4-44) divided by the shaping-signal zero-crossing slope (Equation 4-39) and is given by

$$\sigma_{tcf} = \frac{\sigma_{vin}\sqrt{1^2 + f^2 - 2f\,e^{-|t_d|/t_{in}}}}{V_{inpk}(1-f)/t_{in}} \quad . \tag{4-45}$$

In Equation 4-45, shaping-signal slope is assumed to be constant over the range of noise about the timing crossing.

It is convenient to normalize the timing jitter to the minimum input-signal jitter which is equal to the rms input noise (σ_{vin}) divided by the peak input-signal slope. The minimum input-signal jitter for the single-pole step input is given by

$$\sigma_{tin\,(min)} = \frac{\sigma_{vin}}{V_{inpk}/t_{in}} \quad , \tag{4-46}$$

where the denominator expression is equal to the peak input-signal slope (Equation 4-19) which occurs at time equal to zero for the single-pole exponential-rise input signal. The normalized CFD timing jitter is then given by Equation 4-45 divided by Equation 4-46 and is expressed as

$$\frac{\sigma_{tcf}}{\sigma_{tin\,(min)}} = \frac{\sqrt{1^2 + f^2 - 2f\,e^{-|t_d|/t_{in}}}}{1-f} \quad . \tag{4-47}$$

Normalized CFD timing jitter is shown in Figure A-6 (page 264) for the single-pole step input and in Figure A-12 (page 268) for the two-pole step input. The normalized jitter is shown for different fraction values (f) as a function of normalized constant-fraction delay (t_d/t_{in}). Normalized timing jitter for the single-pole step-input signal is equal to unity for zero delay and fraction and increases monotonically with increasing delay and fraction. Operation at zero delay and fraction corresponds to timing on the beginning of the input signal where the slope is maximum. In contrast to the single-pole step input, normalized timing jitter for the two-pole step input reaches a minimum for non-zero delay and fraction. The delay and fraction associated with this minimum ensures timing operation near the maximum input-signal slope which occurs at 26.4% of the input-signal amplitude. The normalized timing jitter is 123.4% and 110.9% respectively for the single-pole and two-pole step inputs for a fraction value of 20% and a constant-fraction delay that gives a zero-crossing time of twice the input-signal time-constant ($t_{cf} = 2t_{in}$). The advantages of timing with no amplitude sensitivity and with reduced rise-time sensitivity come at the expense of an increase in timing jitter over the minimum input-signal timing jitter.

DC Baseline Effects on Timing Performance

As discussed earlier, CFD zero-crossing time shifts from the theoretical time if a nonzero input-signal DC-baseline level is present. The shift in zero-crossing time can be expressed for the delay-line CFD by

$$\Delta t_{cf\,(due\ to\ input\ DC\ baseline)} = \frac{-V_{baseline}\,(1-f)}{K_{cf}} \quad , \tag{4-48}$$

where $(1 - f)$ is the DC gain from the input-signal to the shaping-signal and K_{cf} is the shaping-signal zero-crossing slope for the input-signal under evaluation. In Equation 4-48, the shaping-signal zero-crossing slope is assumed to be constant between the theoretical zero-crossing point and the baseline-shifted zero-crossing point.

The shift in CFD zero-crossing time is -0.455 ns and -0.821 ns respectively for a 100-mV single- and two-pole input signal having a +10 mV DC baseline level. This example assumes a CFD fraction value of 20%, a constant-fraction delay that gives a zero-crossing time of twice the input-signal time-constant ($t_{cf} = 2t_{in}$), and an input-signal time-constant of 4.545 ns (10 - 90% rise-time of 10 ns). The increased zero-crossing time shift is present for the two-pole input signal because of the lower shaping-signal slope at the zero-crossing timing point.

Nowlin (Non-Delay-Line) CFD

Nowlin discovered a class of non-delay-line shaping circuits which produce output signals with zero-crossing times that are independent of input-signal amplitude and rise-time for linear-edge input signals [5, 6]. These circuits operate by differencing an attenuated version of the input signal with a differentiated version. The resultant shaping signal has zero-crossing time which is insensitive to input-signal amplitude and rise-time, provided the zero-crossing time occurs on the leading edge of the linear-edge input signal. The requirement of timing along the leading edge of a linear-edge input signal is also necessary for amplitude-rise-time-compensated timing using the delay-line CFD.

In addition to zero-crossing time that is independent of input-signal amplitude and rise-time for linear-edge signals, the (Nowlin) shaping-signal zero-crossing time is insensitive to input-signal amplitude for nonlinear-edge input signals of fixed, arbitrary shape. Shaping-signal zero-crossing time is independent of input-signal amplitude for all linear bipolar shaping circuits having input signals of fixed, arbitrary shape.

The simplest implementation of the Nowlin CFD consists of a single-pole highpass filter (acting as an approximate differentiation network) combined with an attenuation and differencing circuit. A circuit model of this implementation is shown in Figure 4-3.

Since the timing zero crossing occurs on the leading-edge of the input signal, it is necessary to consider only the leading-edge of the input signal for analysis of the Nowlin CFD. The leading edge of the input signal is described in the time and Laplace domains as

$$v_{in}(0 \le t \le t_r) = \frac{V_{inpk}}{t_r} t \quad \text{and} \tag{4-49}$$

$$V_{in}(s) = \frac{V_{inpk}}{t_r} \frac{1}{s^2} , \tag{4-50}$$

where V_{inpk} is the peak input-signal amplitude (occurring at $t = t_r$) and t_r is the input-signal linear-edge rise-time.

The transfer function for the Nowlin CFD is found from Figure 4-3 and is given by

$$H_{cf}(s) = f\left(\frac{1 - st_d\left(\frac{1-f}{f}\right)}{1 + st_d}\right) , \tag{4-51}$$

where f is the attenuation gain and t_d is the time-constant associated with the single-pole highpass network. This transfer function has a right-half-plane real zero and a left-half-plane real pole. Nowlin reported that only a single right-half-plane real zero is required in the shaping-network transfer function to give output signals with zero-crossing times that are insensitive to input rise-time (and, of course, amplitude) for linear-edge input signals [5, 6].

The shaping signal for the Nowlin CFD with linear-edge input signals is represented in Laplace notation as the product of the input-signal (Equation 4-50) and the shaping-network (Equation 4-51) Laplace expressions. The time-domain shaping signal is found from the inverse Laplace transform of this product and is given by

$$v_{cf}(0 \le t \le t_r) = \frac{V_{inpk}}{t_r}\left(ft - t_d(1 - e^{-t/t_d})\right) . \tag{4-52}$$

The shaping signal given by Equation 4-52 starts from a value of zero (at $t = 0$) and must go negative before making a positive-going zero crossing. An initial negative signal swing (underdrive) requires that the fraction (f) be less than unity, and a positive-going zero crossing requires that the fraction be greater than zero. In addition, the positive-going zero crossing must occur during the input-signal rise-time placing a further restriction on the fraction value. The range of acceptable values for the fraction are described by

$$0 < f < 1 \quad \text{and} \tag{4-53}$$

$$f \le \frac{t_d}{t_r}\left(1 - e^{-t_r/t_d}\right) , \tag{4-54}$$

where the fraction and single-pole highpass-filter time-constant must be selected based on the smallest expected input-signal rise-time. Under the constraints given, the zero-crossing time occurs for time greater than zero and time less-than-or-equal-to the input-signal rise-time. The zero-crossing time occurs when Equation 4-52 is equal to zero and is found by solving for the time when the right-hand bracketed expression is equal to zero. Clearly, the zero-crossing time is not a function of either the input-signal amplitude (V_{inpk}) or the rise-time (t_r), illustrating that the zero-crossing time is insensitive to input-signal amplitude and rise-time for linear-edge input signals. As can be seen from Equation 4-52, the zero-crossing time can not be solved in closed form; the zero-crossing time must be solved numerically.

It will be shown later that the Nowlin shaping-circuit transfer function is equal in form to the transfer function of one circuit in a class of Binkley timing-shaping circuits, even though the Binkley circuits do not utilize differentiator or approximate differentiator elements. The performance of the Nowlin shaping circuit for lowpass-filtered step inputs can be determined from the performance data given later for the analogous Binkley shaping circuit. Additionally, an illustration of rise-time insensitive timing will be given later for the analogous Binkley shaping circuit.

As mentioned in *Section 1*, Tanaka recently reported what is believed to be the first fully-monolithic CFD [7]. This circuit, fabricated in bipolar transistor technology, operates by differencing an attenuated version of the input signal and a single-pole highpass-filtered version. This circuit topology is the topology reported by Nowlin. The monolithic CMOS CFD reported later in this work uses the Binkley timing-shaping circuit topology that is believed to be previously unreported. Additionally, this circuit is believed to be the first reported, fully monolithic CMOS CFD.

Binkley (Non-Delay-Line) CFD

Description

A class of non-delay-line timing-shaping circuits, believed to be previously unreported, was developed independently and prior to knowledge of the Nowlin timing-shaping circuits. This class of circuits (described as Binkley CFD circuits) operates by subtracting an attenuated version of the input signal from a *lowpass-filtered (integrated)* or *allpass-filtered* version. The resultant bipolar shaping signal has zero-crossing time that is independent of input-signal amplitude for arbitrary, fixed-shape input signals. Additionally, for some shaping-circuit configurations, the zero-crossing time is independent of input-signal amplitude and rise-time for linear-edge input signals.

The Binkley CFD circuit (Figure 4-4) is architecturally opposite of the Nowlin circuit (Figure 4-3) since the Binkley circuit utilizes lowpass (integrator) or allpass elements instead of the highpass (differentiator) elements utilized in the Nowlin circuit. Additionally, the attenuated signal is subtracted from the filtered signal in the Binkley circuit compared to the subtraction of the filtered signal from the attenuated signal in the Nowlin circuit.

The Binkley CFD was initially developed to provide timing that is insensitive to input-signal amplitude for input signals of fixed shape. As mentioned earlier, shaping-signal zero-crossing time is independent of input-signal amplitude for all linear bipolar shaping circuits having input signals of fixed, arbitrary shape. Fixed rise-time input signals were initially considered because scintillation-detector output signals have fixed rise-time, excluding the effects of detector statistical fluctuations. It was later discovered, that the zero-crossing time for the Binkley CFD is, in fact, insensitive to input-signal rise-time for linear-edge input signals provided that the timing point occurs somewhere along the linear-edge of the input signal. The rise-time insensitivity is a direct result of a single right-half-plane real zero which, like the Nowlin CFD, is present in the shaping-circuit transfer function.

Development of Delay-Line Approximation Filters

The Binkley CFD was developed by replacing the delay line in the delay-line CFD with a delay-line approximation filter. An ideal delay-line is a linear-phase, allpass filter having constant amplitude response but linearly increasing phase shift with frequency. The group delay (the derivative of the phase response with frequency) of an ideal delay line is equal to the delay of the delay line and is constant for all frequencies, indicating that all input-frequency components are delayed equally in time. Additionally, the characteristic of linear phase or constant group delay results in overshoot-free transient response for the ideal delay line. This can be illustrated for a square-wave input since the square-wave frequency components (fundamental and odd harmonics) are delayed equally in time and sum to produce an output signal having no overshoot.

Delay-line approximation filters are designed for linear-phase response and constant-amplitude response over some limited frequency range [8, 9]. Above this frequency range, the phase shift deviates from a linear-phase response and the amplitude response deviates from a constant response.

The major specification for delay-line approximation-filter performance is the delay-time, bandwidth product [8, 9]. A high (much greater than unity) delay-time, bandwidth product corresponds to a filter having delay that greatly exceeds the filter rise-time. Fortunately, the delay time required for the delay-line CFD circuit is in the order of the

input-signal rise-time. As a result, the delay-time, bandwidth product required for a delay-line approximation filter is relatively low (in the range of 1 - 5). Delay-line approximation filters with delay-time, bandwidth products in this range can be designed using relatively low-order (fourth-order or less) allpass networks in contrast to the high-order networks typically used for commercial delay-line approximation filters.

In addition to allpass filters, delay-line approximation filters can be composed of linear-phase lowpass filters. The major disadvantage of lowpass filters for delay-line approximation filters is the low delay-time, bandwidth product compared to allpass filters. The improved delay-time, bandwidth product of allpass filters is due to the presence of right-half-plane zeros which are mirror images of the left-half-plane poles present. As a result of the mirror-image right-half-plane zeros, the allpass filter provides constant magnitude response while providing increasing phase shift with frequency. Although the magnitude response of allpass filters is constant, signal distortion (undershoot, overshoot) will occur for input-signal frequency components that are above the linear-phase frequency limit. This distortion can be minimized by limiting the input-signal bandwidth for the allpass filter.

The first-order or single-pole lowpass filter response is given in Laplace notation as

$$H(s) = \frac{\omega_n}{s + \omega_n} \quad , \tag{4-55}$$

where ω_n is the critical frequency associated with the pole (also the -3 dB frequency). The first-order allpass filter is synthesized by the addition of a mirror-image right-half-plane zero. The first-order allpass filter response is then given by

$$H(s) = -\left(\frac{s - \omega_n}{s + \omega_n} \right) \quad , \tag{4-56}$$

where negation is present in the expression to permit positive DC gain. As illustrated in Equation 4-56, the magnitude response for the first-order allpass filter is constant with frequency while the phase shift increases with frequency. Additionally, the phase shift (for any frequency) present in the first-order allpass filter is twice that of the first-order lowpass filter. The first-order allpass filter response can be obtained by subtracting the input signal from a first-order lowpass-filtered version of the input signal where the lowpass filter gain is equal to two.

The second-order or two-pole lowpass filter response (all-pole lowpass filters are assumed) is given in Laplace notation as

$$H(s) = \frac{\omega_n^2}{s^2 + (\omega_n / Q)s + \omega_n^2} \quad , \tag{4-57}$$

where ω_n is the natural frequency and Q $(1/(2\zeta))$ is the quality factor associated with the pair of poles. The second-order allpass filter is synthesized by the addition of mirror-image right-half-plane zeros. The second-order allpass filter response is then given by

$$H(s) = \frac{s^2 - (\omega_n / Q)s + \omega_n^2}{s^2 + (\omega_n / Q)s + \omega_n^2} \quad . \tag{4-58}$$

Like the first-order allpass filter, the magnitude response for the second-order allpass filter is constant with frequency while the phase shift increases with frequency. Additionally, the phase shift (for any frequency) present in the second-order allpass filter is twice that of the second-order lowpass filter. The second-order allpass filter response can be obtained by subtracting a second-order bandpass-filtered version of the input signal from the input signal where the bandpass filter gain is equal to two.

Second- and higher-order filters can be designed for Gaussian, Bessel, Butterworth, Chebyshev, etc., responses by the selection of pole locations (and mirror-image right-half-plane zeros for the case of allpass filters). In practice, the desired second-order filter response is obtained by the selection of second-order natural frequency (ω_n) and quality factor (Q). Third- and higher-order filters are obtained by cascaded second-order sections, with a single first-order section required if the composite filter order is numerically odd. Tables giving the natural frequency and quality factors for cascaded filter sections are given in the classic filter book by Zverev [8] and the more recent book by Williams [9]. Filter synthesis details are also available in many other filter books and electrical-engineering reference books.

Delay-line approximation filters, for the CFD application considered, will be evaluated for a two-pole lowpass-filtered step-input signal. As discussed earlier, the linear-edge signal is not representative of scintillation-detector signals. Similarly, the high initial slope of the single-pole lowpass-filtered step-input signal is not representative of PET scintillation-detector timing signals because of the presence of more than one significant bandwidth-limiting pole in the system response. The input signal considered is the same normalized

two-pole lowpass-filtered step-input signal considered earlier for delay-line CFD analysis. The composite time-constant for the input signal considered is one-second (t_{in} = 1 s) and the rise-time (10 - 90%) is approximately 2.2 seconds ($2.2t_{in}$).

The delay-line approximation filters considered are designed to give delays (at the 50% output point) of one second for the normalized two-pole lowpass-filtered step-input signal. This delay is equal to approximately one-half the input-signal rise-time which is relatively "short" for constant-fraction operation and corresponds to amplitude-rise-time-compensated operation for the delay-line CFD having the typical fraction of 20%. It will be shown later that "short" CFD operation, where timing is developed during the input-signal rise-time, is desirable for good scintillation-detector statistical timing performance.

Both lowpass and allpass delay-line approximation filters are considered of first-order, second-order, and fourth-order design. Additionally, Gaussian, Bessel, and Butterworth responses are considered for the second- and fourth-order designs. Synthesis details for the delay-line approximation filters are given in Table 4-2.

The two-pole lowpass-filtered step input and resulting output signals are shown in Figure 4-5 for the first-order lowpass and allpass delay-line approximation filters. Each filter provides a one-second signal delay but the allpass-filter output-signal slope is close to that of the input signal while the lowpass-filter output-signal slope is considerably lower. The higher allpass-filter output-signal slope is a result of allpass filter gain that does not roll off with frequency. Higher output-signal slope, assuming equivalent circuit noise levels, is advantageous for minimizing timing jitter. Additionally, higher output-signal slope is advantageous for minimizing comparator walk errors. The output-signal slope for the first-, second-, and fourth-order lowpass and allpass delay-line approximation filters considered will be compared later.

The first-order allpass filter output has considerable negative undershoot (Figure 4-5) since input-signal components are present at frequencies above the linear-phase frequency limit and these input-signal components are not lowpass filtered. Although this negative undershoot is undesirable for a delay-line approximation filter, the allpass-filter output signal is precisely what is desired for a CFD timing-shaping signal: a bipolar signal that initially goes negative followed by a zero-crossing with signal slope comparable to the input-signal slope. It will be shown later that there are special configurations of the Nowlin and Binkley CFD shaping circuits that exhibit a first-order allpass filter response.

The group delay for the first-order lowpass and allpass delay-line approximation filters is shown in Figure 4-6. The group delay at DC for both filters is approximately one second

Table 4-2. Synthesis Details for Delay-Line Approximation Filters.

Filter Type	Synthesis Details
1st-order Lowpass	ω_n = 0.95 rad/s
1st-order Allpass	ω_n = 1.9 rad/s
2nd-order Lowpass, Gaussian	ω_n = 1.45 rad/s ($\sqrt{2}$(1.45) rad/s ea. pole)
2nd-order Lowpass, Bessel	ω_n = 1.45 rad/s, Q = 0.578
2nd-order Lowpass, Butterworth	ω_n = 1.6 rad/s, Q = 0.707
2nd-order Allpass, Bessel	ω_n = 3.48 rad/s, Q = 0.578
4th-order Lowpass, Gaussian	ω_n = 2.07 rad/s ($\sqrt{4}$ (2.07) rad/s ea. pole)
4th-order Lowpass, Bessel	ω_n = 2.22 rad/s, 1st section: ω_n = (2.22)(1.419) rad/s, Q = 0.522 2nd section: ω_n = (2.22)(1.591) rad/s, Q = 0.806
4th-order Lowpass, Butterworth	ω_n = 2.76 rad/s, 1st section: ω_n = (2.76)(1.0) rad/s, Q = 0.541 2nd section: ω_n = (2.76)(1.0) rad/s, Q = 1.307
4th-order Allpass-Lowpass Combination, Bessel	Allpass section: ω_n = 4.85 rad/s, Q = 0.578 Lowpass section: ω_n = 4.85 rad/s, Q = 0.578
Filter delay (to 50% output point) is 1 s. Filter input is two-pole lowpass-filtered step input with composite time-constant of 1 s (0.707 s ea. pole).	

with the allpass filter having a bandwidth of constant group delay (linear phase) that is approximately twice that of the lowpass filter. The gain response for both the lowpass and allpass filters is shown in Figure 4-7. The gain of the both filters is unity at DC but the gain for the lowpass filter rolls off at frequencies above the cutoff frequency. The gain of the allpass filter is constant with frequency, the filter providing only phase shift.

The two-pole lowpass-filtered step input and resulting output signals are shown in Figure 4-8 for the second-order lowpass and allpass delay-line approximation filters. Each filter provides a one-second signal delay, but as was the case with the first-order filters, the

allpass-filter output-signal slope is close to that of the input signal while the output-signal slope of the lowpass filters is somewhat lower. Unfortunately, the allpass-filter output signal goes positive initially, which is not desirable for either the application of delay-line replacement in a CFD circuit or the application as a complete timing-shaping circuit. In both cases, the initial positive-going signal can cause a shallow zero-crossing prior to the main zero-crossing.

The second-order lowpass-filter output signals (Figure 4-8) are nearly equal for the Gaussian, Bessel, and Butterworth cases, with the output-signal slopes also being nearly equal. The output-signal slope for the Gaussian filter is the lowest, the output-signal slope for the Butterworth filter is the highest, and the output-signal slope for the Bessel filter is between that of the Gaussian and Butterworth filters.

The group delay for the second-order lowpass and allpass delay-line approximation filters is shown in Figure 4-9. The group delay at DC for all filters is approximately one second, with the allpass filter having a bandwidth of constant group delay (linear phase) that is considerably higher than that of the lowpass filters. Both the Bessel lowpass filter and the allpass filter (also of Bessel design) have maximally flat group delay characteristics without group-delay peaking. In contrast, the Gaussian lowpass filter has group delay that begins rolling off earlier in frequency, and the Butterworth lowpass filter has considerable group-delay peaking. Output-signal overshoot for the Butterworth filter, normally present for step inputs, is not observed (for the times shown in Figure 4-8) because of limited bandwidth of the two-pole lowpass-filtered step-input signal.

The gain response for the second-order lowpass and allpass filters is shown in Figure 4-10. The gain of all filters is unity at DC but the gain for the lowpass filters rolls off at frequencies above the cutoff frequency. The Butterworth lowpass filter has maximally flat gain response, whereas the Bessel and Gaussian lowpass filters have gain that rolls off earlier in frequency. Again, like the first-order allpass filter, the gain of the second-order allpass filter is constant with frequency, the filter providing only phase shift.

The two-pole lowpass-filtered step input and resulting output signals are shown in Figure 4-11 for the fourth-order lowpass and allpass-lowpass delay-line approximation filters. The allpass-lowpass filter consists of a second-order allpass filter combined with a second-order lowpass filter as illustrated in Table 4-2. The second-order lowpass filter is designed to minimize the initial positive-going signal distortion that is present at the output of the second-order allpass filter.

Each fourth-order filter response shown in Figure 4-11 provides a one-second signal delay, but as was true for the lower-order filters, the allpass-(lowpass)-filter output-signal slope is close to that of the input signal while the output-signal slope of the lowpass filters is somewhat lower. As will be shown later in a comparison of output-signal slope for the delay-line approximation filters considered, the output-signal slope for the fourth-order lowpass filters is more nearly equal to the input-signal slope than is the output-signal slope of the second-order filters.

The fourth-order lowpass-filter output signals (Figure 4-11) are similar for the Gaussian, Bessel, and Butterworth cases but there is greater difference in the output signals compared to the second-order lowpass filters previously considered. The differences between Gaussian, Bessel, Butterworth, Chebyshev, etc., filter responses become increasingly pronounced with higher filter order. As was true for the second-order lowpass filters, the output-signal slope for the fourth-order Gaussian filter is the lowest, the output-signal slope for the Butterworth filter is the highest, and the output-signal slope for the Bessel filter is between that of the Gaussian and Butterworth filters.

The group delay for the fourth-order lowpass and allpass-lowpass delay-line approximation filters is shown in Figure 4-12. The group delay at DC for all filters is approximately one second with the allpass-lowpass filter having a bandwidth of constant group delay (linear phase) that is higher than that of the lowpass filters. Again, as was true of the second-order lowpass filters, the Bessel lowpass filter and the allpass-lowpass filter (also of Bessel design) have maximally flat group delay characteristics without group-delay peaking. In contrast, the Gaussian lowpass filter has group delay that begins rolling off earlier in frequency (more pronounced for the fourth-order filter compared to the second-order filter), and the Butterworth lowpass filter has considerable group-delay peaking (again more pronounced for the fourth-order filter compared to the second-order filter). Also as was true for the second-order lowpass filters, output-signal overshoot for the fourth-order Butterworth filter is not observed (for the times shown in Figure 4-11) because of limited bandwidth of the two-pole lowpass-filtered step-input signal.

The gain response for the fourth-order lowpass and allpass-lowpass filters is shown in Figure 4-13. As was true of the second-order filters, the gain of all fourth-order filters is unity at DC but the gain for all filters rolls off at frequencies above the cutoff frequency. Gain roll-off occurs for the allpass-lowpass filter combination because of gain roll-off in the lowpass filter. As was true of the second-order filters, the Butterworth lowpass filter has maximally flat gain response, whereas the Gaussian and Bessel lowpass filters have gain

that rolls off earlier in frequency. The difference in the Gaussian and Bessel filter response is more pronounced for the fourth-order filters compared to the second-order filters.

The output-signal slope at various locations on the output signal is tabulated in Table 4-3 for the first-, second-, and fourth-order lowpass and allpass delay-line approximation filters. The input signal for all filters is the two-pole lowpass-filtered step-input signal having a composite time-constant of 1 s.

Table 4-3. Output-Signal Slope for First-, Second-, and Fourth-Order Lowpass and Allpass Delay-Line Approximation Filters.

Signal	Slope Normalized to Peak Input Slope at Various Percentages of Signal Level			
	10%	20%	33%	50%
Input Signal to Filters	85%	98%	99%	85%
Output, 1st-order Lowpass	48%	60%	63%	57%
Output, 2nd-order Lowpass, Gaussian	50%	65%	72%	67%
Output, 2nd-order Lowpass, Bessel	50%	66%	74%	71%
Output, 2nd-order Lowpass, Butterworth	50%	68%	77%	76%
Output, 4th-order Lowpass, Gaussian	55%	73%	80%	75%
Output, 4th-order Lowpass, Bessel	57%	77%	86%	81%
Output, 4th-order Lowpass, Butterworth	57%	81%	95%	93%
Output, 1st-order Allpass	81%	88%	87%	77%
Output, 2nd-order Allpass, Bessel	79%	92%	95%	84%
Output, 2nd-order Allpass + 2nd-order Lowpass, both Bessel	75%	91%	95%	84%

Peak input-signal slope = $(V_{inpk}/t_{in})e^{-1} = 0.5203$ V/s.
Filter input is two-pole lowpass-filtered step input with composite time-constant (t_{in})of 1 s (0.707 s ea. pole).
All filters provide 1 s delay at 50% output point; Filter synthesis details given in Table 4-2.

As seen in Table 4-3, lowpass-filter output-signal slope increases with filter order, the fourth-order lowpass filters having the highest level of output-signal slope. Additionally, for a given lowpass-filter order, the output-signal slope is maximum for the least damped filters, the Butterworth filters, and is minimum for the most damped filters, the Gaussian filters. Output-signal slope for the first- and second-order allpass filters is considerably higher than the lowpass filters of the same order, especially at output-signal points considerably below the peak output signal. As described earlier, the second-order allpass filter cannot be used for delay-line replacement or as a complete shaping circuit because of the presence of an initial positive-going lobe in its output signal. The fourth-order allpass-lowpass filter combination, a second-order allpass filter followed by a second-order lowpass filter to minimize the initial positive-going allpass-filter output lobe, has signal slope nearly equal to that of the second-order allpass filter.

The first-order allpass filter has higher output-signal slope at points at or below 20% of the peak output signal compared to the first-, second-, and fourth-order lowpass filters. The fourth-order Butterworth lowpass filter, however, has equal or higher output-signal slope at points at or above 33% of the peak output signal compared to the first-order allpass, second-order allpass, second-order allpass with second-order lowpass filter combination, and the other first-, second-, and fourth-order lowpass filters.

Gaussian lowpass filters are of special interest as delay-line approximation filters because of their simplicity. These filters have real poles with equal critical frequencies and do not require the state-variable or biquad second-order filter sections typically required for Bessel, Butterworth, Chebyshev, and other filters.

The group delay of an n-th order Gaussian lowpass filter is approximated by

$$t_d \cong n t_p \quad , \tag{4-59}$$

where n is the filter order (the number of poles) and t_p is the time-constant associated with each pole. The effective time-constant of the filter (representative of filter bandwidth and rise-time) is approximated by

$$t_{BW} \cong \sqrt{n}\, t_p \quad . \tag{4-60}$$

The delay-bandwidth product of the filter is then approximated by

$$t_d\,\omega_{-3\,dB} \cong \frac{t_d}{t_{BW}} \cong \frac{n t_p}{\sqrt{n}\,t_p} \cong \sqrt{n} \quad . \tag{4-61}$$

It is more useful to consider the filter delay-time to rise-time ratio for time-domain work. This ratio is closely related to the delay-bandwidth product and is approximated by

$$\frac{t_d}{t_{r\,(10\,-\,90\%)}} \cong \frac{t_d}{2.2 t_{BW}} \cong \frac{\sqrt{n}}{2.2} \quad . \tag{4-62}$$

Both the delay-bandwidth product and the delay-time to rise-time ratio increase as the square-root of the number of poles in a Gaussian lowpass filter. The increase over a single-pole filter is approximately a factor of 1.4 for a two-pole filter, 2.0 for a four-pole filter, and 3.2 for a ten-pole filter. The improvement increases at a diminishing rate as the number of filter poles continues to increase.

Synthesis of Binkley CFD Circuits Using Gaussian Lowpass Filters

The synthesis of Binkley CFD shaping circuits (circuit model shown in Figure 4-4) will be considered for Gaussian lowpass filters used as delay-line approximation filters. As mentioned, the simplicity of Gaussian lowpass filters makes these filters advantageous for circuit implementation. The Gaussian lowpass filters used for delay-line approximation have Laplace transfer functions given by

$$D(s) = \frac{\left[\sqrt{n}\omega_d\right]^n}{\left[s+\sqrt{n}\omega_d\right]^n} \quad , \tag{4-63}$$

where ω_d is a filter cutoff frequency that is inversely proportional to the desired filter time delay, and n is the filter order. The critical frequency associated with each real pole is increased above the filter cutoff frequency (ω_d) by the $\sqrt{n}$ factor shown to maintain nearly constant filter rise-time independent of filter order for a given cutoff frequency.

The transfer function for the Binkley CFD with Gaussian lowpass delay-line approximation filters is given from Figure 4-4 by

$$H_{cf}(s) = D(s) \cdot f \quad , \text{or} \tag{4-64}$$

$$H_{cf}(s) = \frac{\left[\sqrt{n}\omega_d\right]^n}{\left[s+\sqrt{n}\omega_d\right]^n} \cdot f \quad , \tag{4-65}$$

where f is the fraction value. The fraction value will be constrained, as in the case of the delay-line CFD, for values between zero and unity. Equation 4-65 can be rewritten as

$$H_{cf}(s) = \frac{\left[\sqrt{n}\omega_d\right]^n - f\left[s+\sqrt{n}\omega_d\right]^n}{\left[s+\sqrt{n}\omega_d\right]^n} \quad , \tag{4-66}$$

to permit study of the pole and zero locations. The transfer function contains the same real poles present in the Gaussian lowpass filter (the number of poles equal to the lowpass-filter order), but unlike the lowpass filter, the transfer function contains zeros (the number of zeros again equal to the lowpass-filter order). It will be shown later that one of these zeros is a right-half-plane real zero. The DC gain of the transfer function is given by

$$H_{cf}(dc) = 1 - f \quad , \tag{4-67}$$

which is valid for all lowpass and allpass delay-line approximation filters (of arbitrary type and order) having unity DC gain.

The transfer function of the Binkley CFD containing a first-order (Gaussian) lowpass filter can be evaluated from Equation 4-66 for n equal to one. The resulting transfer function is given by

$$H_{cf\,(n=1)}(s) = -f\left(\frac{s - \omega_d\left(\frac{1-f}{f}\right)}{s+\omega_d}\right) \quad . \tag{4-68}$$

Equation 4-68 contains one pole (having the same critical frequency as the lowpass-filter pole) and one right-half-plane real zero. The critical frequency for the right-half-plane zero can be adjusted to any real value by selection of the fraction value ($0 < f < 1$) and lowpass-filter cutoff frequency (ω_n). It is interesting to note that replacing the first-order lowpass filter with a first-order allpass filter still results in a CFD transfer function containing one

left-half-plane pole and one right-half-plane real zero. This configuration is not as useful, however, because the critical frequency associated with the right-half-plane real zero cannot be adjusted above the filter cutoff frequency (ω_n).

If a fraction value (f) of one-half is selected, the transfer function (Equation 4-68) of the Binkley CFD containing a single-pole lowpass filter has the form of a first-order allpass filter with gain of one-half. As mentioned earlier, the first-order allpass response is desirable for a CFD. It will be shown later, however, that even better response is available for the Binkley CFD using lowpass filters of higher order (order greater than one).

One configuration of the Binkley CFD gives a transfer function equivalent to the Nowlin CFD containing a single-pole highpass filter. The transfer function for the Nowlin CFD (Equation 4-51, page 116) can be rewritten in terms of the highpass-filter critical frequency ω_d instead of the highpass-filter time-constant t_d by using the substitution of $\omega_d = 1/t_d$. The transfer function is then given by

$$H_{cf\,(Nowlin)}(s) = -(1-f)\left(\frac{s-\omega_d\left(\frac{f}{1-f}\right)}{s+\omega_d}\right), \tag{4-69}$$

where it can be observed that the Nowlin CFD (using a single-pole highpass filter) is equivalent in form to the Binkley CFD (Equation 4-68) using a single-pole lowpass filter. The Binkley CFD is identical to the Nowlin circuit if the fraction value for the Binkley circuit is selected as described by

$$f_{(Binkley\ circuit\ with\ 1st\text{-}order\ lowpass)} = 1 - f_{(Nowlin\ circuit\ with\ 1st\text{-}order\ highpass)} \ . \tag{4-70}$$

It is interesting that the first-order Binkley and Nowlin CFDs are equivalent, with an appropriate interchange of fraction values, even though the Binkley circuit uses a lowpass filter and the Nowlin circuit uses a highpass filter. This circuit equivalence resulted even though the Nowlin circuit was developed without delay-line approximation filters [6] and the Binkley circuit was developed with delay-line approximation filters.

The Binkley CFD transfer function (Equation 4-66) is given in factored form as:

$$H_{cf(n=1)}(s) = -f\left(\frac{s-\omega_d\left(\frac{1-f}{f}\right)}{s+\omega_d}\right), \tag{4-71}$$

$$H_{cf(n=2)}(s) = -f\left(\frac{s-\sqrt{2}\omega_d\left(\frac{1-\sqrt{f}}{\sqrt{f}}\right)}{s+\sqrt{2}\omega_d}\right)\left(\frac{s+\sqrt{2}\omega_d\left(\frac{1+\sqrt{f}}{\sqrt{f}}\right)}{s+\sqrt{2}\omega_d}\right), \tag{4-72}$$

$$H_{cf(n=3)}(s) = -f\left(\frac{s-\sqrt{3}\omega_d\left(\frac{1-\sqrt[3]{f}}{\sqrt[3]{f}}\right)}{s+\sqrt{3}\omega_d}\right)\left(\frac{s+\sqrt{3}\omega_d\left(\frac{\sqrt[3]{f}+1/2\pm j\sqrt{3}/2}{\sqrt[3]{f}}\right)}{s+\sqrt{3}\omega_d}\right), \text{ and} \tag{4-73}$$

$$H_{cf(n=4)}(s) = -f\left(\frac{s-\sqrt{4}\omega_d\left(\frac{1-\sqrt[4]{f}}{\sqrt[4]{f}}\right)}{s+\sqrt{4}\omega_d}\right)\left(\frac{s+\sqrt{4}\omega_d\left(\frac{1+\sqrt[4]{f}}{\sqrt[4]{f}}\right)}{s+\sqrt{4}\omega_d}\right)\left(\frac{s+\sqrt{4}\omega_d\left(\frac{\sqrt[4]{f}\pm j}{\sqrt[4]{f}}\right)}{s+\sqrt{4}\omega_d}\right), \tag{4-74}$$

where n denotes the order of the Gaussian-lowpass delay-line approximation filter and ω_d is the delay-line-filter cutoff frequency which is equal to the inverse of the delay time constant ($t_d = 1/\omega_d$).

The Binkley Gaussian CFD transfer functions were factored (using a commercial symbolic mathematical analysis program) to identify the pole and zero locations. The pole-zero locations are given in Figure 4-14 for a delay-line-filter cutoff frequency of 1 rad/sec (a

delay time constant, $t_d = 1/\omega_d$, of 1 s) and fraction values of 0.3, 0.5, and 0.7. All transfer functions have one right-half-plane real zero which, as mentioned earlier, provides rise-time invariant timing for linear-edge input signals. Additionally, the second- and fourth-order circuits contain a left-half-plane real zero, and the third- and fourth-order circuits contain a pair of complex-conjugate left-half-plane zeros. As mentioned earlier, all circuits contain the same real (left-half-plane) poles that are present in the Gaussian lowpass filters.

It is interesting to note that the zeros in the Binkley Gaussian CFD transfer function (Figure 4-14) are located on a circle centered at the pole locations. One of these zeros is always located on the real axis of the right-half plane. The other zeros (for second and higher-order filters) are located at even spacing along the circle.

Performance with Lowpass-Filtered Step Signals

Derivation of Shaping Signal

The shaping signal for the Binkley Gaussian CFD can be found from the circuit model shown in Figure 4-4 (page 155) using Laplace expressions for the input signal ($V_{in}(s)$) and the transfer function ($H_{cf}(s)$). The lowpass-filtered step-input signal has a Laplace transform that was given in Equation 4-15 (page 104) for a single-pole input and in Equation 4-16 (page 104) for a two-pole input. Additionally, the transfer function was given in Equations 4-71, 4-72, 4-73, and 4-74 for the single-, two-, three-, and four-pole Binkley Gaussian CFD circuit.

The shaping signal for the Binkley Gaussian CFD, along with full circuit-performance data, is given in *Appendix A - Catalog of Normalized CFD Performance for Lowpass-Filtered Step Inputs*. This data will be referred to in the following discussion. Additionally, a comparison of delay-line and Binkley Gaussian CFD performance will be discussed later in this section.

The shaping signal for a single-pole step input is shown in Figure A-13 (page 270), A-25 (page 278), and A-37 (page 286) for the Binkley single-, two-, and four-pole Gaussian CFD. The normalized delay time-constants (t_d/t_{in}) for the CFDs were selected for a zero-crossing time equal to twice the input-signal time-constant ($t_{cf} = 2t_{in}$) and a fraction of 50% was selected. It will be shown later that a fraction of 50% generally results in minimum timing jitter for the Binkley Gaussian CFD. As seen in the figures, both the shaping-signal underdrive ($V_{cf\,(underdrive)}$) and zero-crossing slope (K_{cf}) increase with increasing CFD order because Gaussian lowpass-filter rise-time is degraded less for filters of higher order for a

given filter delay. The shaping-signal overdrive ($V_{cf\,(overdrive)}$) is independent of circuit order as the overdrive is set by the DC gain (1 - f).

The shaping signal for a two-pole step input is shown in Figure A-19 (page 274), A-31 (page 282), and A-43 (page 290) for the single-, two-, and four-pole Binkley Gaussian CFD. Again, the delay time-constants (t_d/t_{in}) for the CFDs were selected for a zero-crossing time equal to twice the input-signal time-constant ($t_{cf} = 2t_{in}$) and a fraction of 50% was selected. As seen in the figures, both the shaping-signal underdrive and zero-crossing slope increase with increasing CFD order for the reasons described for single-pole step inputs. Additionally, the shaping-signal overdrive is again independent of circuit order as the overdrive is set by the DC gain (1 - f). The shaping-signal underdrive is less for the two-pole step input compared to the single-pole step input (for CFD circuits of equal order) because of the initial signal delay present in the two-pole step input.

Zero-Crossing Time

Although the Binkley Gaussian CFD shaping signal can be expressed in closed form for lowpass-filtered step-input signals, no closed-form solution is available for the zero-crossing time. This is due to the presence of exponentials with differing time-constants and/or the presence of exponentials multiplied by expressions containing the independent time variable. The same numerical computer analysis used for delay-line CFD analysis was used to obtain the zero-crossing time and other circuit characteristics of the Binkley Gaussian CFD. The results of this numerical analysis are given in *Appendix A* and are discussed here.

The shaping-signal zero-crossing time for a single-pole step input is shown in Figure A-14 (page 270), A-26 (page 278), and A-38 (page 286) for the Binkley single-, two-, and four-pole Gaussian CFD. Additionally, the shaping-signal zero-crossing time for a two-pole step input is shown in Figure A-20 (page 274), A-32 (page 282), and A-44 (page 290) for the single-, two-, and four-pole circuits. For both the single- and two-pole step input, normalized zero-crossing time (t_{cf}/t_{in}) is given as a function of normalized delay time-constant (t_d/t_{in}) for various fraction (f) values. As was true of the delay-line CFD, shaping-signal zero-crossing time increases monotonically with delay time-constant (because of increased circuit delay) and increases monotonically with fraction (because of circuit triggering at a higher fraction of the input-signal).

Shaping-Signal Amplitude and Slope

Shaping-signal underdrive for a single-pole step input is shown in Figure A-15 (page 271), A-27 (page 279), and A-39 (page 287) for the Binkley single-, two-, and four-pole

Gaussian CFD. Additionally, shaping-signal underdrive for a two-pole step input is shown in Figure A-21 (page 275), A-33 (page 283), and A-45 (page 291) for the single-, two-, and four-pole circuits. Shaping-signal underdrive is shown for different constant-fraction fraction values (f) as a function of constant-fraction delay time-constant (t_d/t_{in}) normalized to the input-signal time-constant. Shaping-signal underdrive ($V_{cf\,(underdrive)}/V_{inpk}$) is normalized to the input-signal amplitude to illustrate the relative amount of underdrive present.

As was true of the delay-line CFD, shaping-signal underdrive increases monotonically (negatively) with delay time-constant and fraction, reaching a maximum value of $-f$ for constant-fraction delays much greater than $5t_{in}$. Shaping-signal underdrive is lower at low constant-fraction-delay time-constants ($t_d/t_{in} < 1$) for two-pole step inputs compared to single-pole step inputs because of the initial signal delay present in the two-pole step input. As mentioned earlier, shaping-signal underdrive increases with the order of the Binkley Gaussian CFD.

Shaping-signal overdrive, as was true for the delay-line CFD, is simply equal to the CFD DC gain multiplied by the input-signal amplitude. Shaping-signal overdrive normalized to input-signal amplitude is equal to the DC gain ($1 - f$) and is not plotted in the data of *Appendix A*.

Shaping-signal zero-crossing slope for a single-pole step input is shown in Figure A-16 (page 271), A-28 (page 279), and A-40 (page 287) for the Binkley single-, two-, and four-pole Gaussian CFD. Additionally, shaping-signal zero-crossing slope for a two-pole step input is shown in Figure A-22 (page 275), A-34 (page 283), and A-46 (page 291) for the single-, two-, and four-pole circuits. Shaping-signal zero-crossing slope is shown for different constant-fraction fraction values (f) as a function of constant-fraction-delay time-constant (t_d/t_{in}) normalized to the input-signal time-constant. Shaping-signal zero-crossing slope (K_{cf}/K_{inpk}) is normalized to the peak input-signal slope to illustrate the amount of input-signal slope loss.

For a single-pole step input, shaping-signal zero-crossing slope for the Binkley Gaussian CFD is maximized at minimum constant-fraction-delay time-constants at a fraction value of approximately 50%. In contrast, shaping-signal zero-crossing slope for the delay-line CFD is independent of constant-fraction delay and is maximized at minimum fraction values. For a two-pole step input, shaping-signal zero-crossing slope for the Binkley Gaussian CFD has a distinct maximum with constant-fraction-delay time-constant and is maximized at a fraction value of approximately 50%. In contrast, shaping-signal zero-crossing slope for the delay-

line CFD increases with constant-fraction delay and is maximized at fraction values of 20 - 30%. The distinct zero-crossing-slope maximum is present because the two-pole step-input signal has maximum slope at 26.4% of the amplitude compared to a maximum slope at 0% of the amplitude for the single-pole step-input signal.

Zero-crossing slope is maximized at higher fraction values for the Binkley Gaussian CFD compared to the delay-line CFD. This is because maximum signal slope at the output of the Gaussian-lowpass delay-line approximation filter occurs at a higher percentage of the signal amplitude compared to the signal present at the output of a delay line.

Timing-Jitter Performance

The mean-square shaping-signal noise for the Binkley Gaussian CFD can be found from steady-state noise analysis and is given by

$$\sigma_{vcf}^2 = \frac{1}{2\pi}\int_{-\infty}^{\infty} S_{in}(\omega)H_{cf}(\omega)H_{cf}^*(\omega)d\omega \quad , \tag{4-75}$$

where $S_{in}(\omega)$ is the input noise-power spectral density and $H_{cf}(s)$ is the CFD transfer function. The input noise-power spectral density was given in Equation 4-21 (page 105) for the single-pole input and Equation 4-22 (page 105) for the two-pole input. The transfer function was given in Equations 4-71, 4-72, 4-73, and 4-74 for the Binkley single-, two-, three-, and four-pole Gaussian CFD circuit.

Shaping-signal rms noise for a single-pole step input is shown in Figure A-17 (page 272), A-29 (page 280), and A-41 (page 288) for the Binkley single-, two-, and four-pole Gaussian CFD. Additionally, shaping-signal rms noise for a two-pole step input is shown in Figure A-23 (page 276), A-35 (page 284), and A-47 (page 292) for the single-, two-, and four-pole circuits. Shaping-signal rms noise is shown for different constant-fraction fraction values (f) as a function of constant-fraction-delay time-constant (t_d/t_{in}) normalized to the input-signal time-constant. Shaping-signal rms noise ($\sigma_{vcf}/\sigma_{vin}$) is normalized to input-signal rms noise to illustrate the relative change in noise through the CFD.

Shaping-signal noise generally decreases with increasing constant-fraction-delay time-constant for low fraction values because the noise bandwidth in the lowpass-filtered-signal path decreases with increasing time-constant. Conversely, shaping-signal noise generally increases with increasing constant-fraction-delay time-constant for high fraction values because of reduced correlated-noise cancellation in the attenuated-signal and lowpass-filtered-signal path. It is interesting to note that the shaping-signal noise shown in the

figures is always less than the input noise for the Binkley Gaussian CFDs. Additionally, for constant-fraction-delay time-constants near the input-signal time-constant, the shaping-signal noise is generally lower than that of the delay-line CFD. This is most significant and, as discussed later, permits the Binkley Gaussian CFD to have comparable timing-jitter performance to the delay-line CFD, even though the shaping-signal slope is lower for the Binkley Gaussian CFD.

Shaping-signal timing jitter is evaluated by finding the ratio of shaping-signal noise (σ_{vcf}) to the shaping-signal zero-crossing slope (K_{cf}). Timing jitter for a single-pole step input is shown in Figure A-18 (page 272), A-30 (page 280), and A-42 (page 288) for the single-, two-, and four-pole Binkley Gaussian CFD. Additionally, timing jitter for a two-pole step input is shown in Figure A-24 (page 276), A-36 (page 284), and A-48 (page 292) for the single-, two-, and four-pole circuits. Timing jitter is shown for different constant-fraction fraction values (f) as a function of constant-fraction-delay time-constant (t_d/t_{in}) normalized to the input-signal time-constant. Timing jitter ($\sigma_{tcf}/\sigma_{tin}$) is normalized to the minimum input-signal jitter to illustrate the relative amount of timing-jitter degradation present using the CFD compared to leading-edge timing on the input-signal at the maximum-slope point.

For a single-pole step input, shaping-signal timing jitter is minimized for the Binkley Gaussian CFD at minimum constant-fraction-delay time-constants and at large fraction values. For constant-fraction-delay time-constants near the input-signal time-constant, timing jitter is minimized at fraction values near 50%. In contrast, timing jitter is minimized for the delay-line CFD at minimum constant-fraction delay and minimum fraction values.

For a two-pole step input, timing jitter for the Binkley Gaussian CFD has a distinct minimum with constant-fraction-delay time-constant and is minimized at fraction values near 50%. Timing jitter for the delay-line CFD has a distinct minimum with constant-fraction delay but is minimized at fraction values of 20 - 30%. The distinct minimum for timing jitter is due largely to the distinct zero-crossing-slope maximum that occurs for two-pole step inputs.

As mentioned earlier, shaping-signal zero-crossing slope increases with the order of the Binkley Gaussian CFD for both single-pole and two-pole step inputs. As a result, timing jitter is minimized for Binkley Gaussian CFDs of higher order.

DC Baseline Effects on Timing Performance

As was true for the delay-line CFD, shaping-signal zero-crossing time shifts from the theoretical zero-crossing time if a nonzero input-signal DC-baseline level is present. The shift in zero-crossing time can be described by the same expression given for the delay-line CFD (Equation 4-48, page 114) and is given by

$$\Delta t_{cf\,(due\ to\ input\ DC\ baseline)} = \frac{-V_{baseline}\,(1-f)}{K_{cf}} \quad , \tag{4-76}$$

where $(1 - f)$ is the DC gain from the input signal to the shaping signal and K_{cf} is the shaping-signal zero-crossing slope for the input signal under evaluation. In Equation 4-76, the shaping-signal zero-crossing slope is assumed to be constant between the theoretical zero-crossing point and the baseline-shifted zero-crossing point.

The zero-crossing time shift with input-signal DC baseline is comparable for both the Binkley Gaussian and delay-line CFDs. This is because the lower zero-crossing slope of the Binkley Gaussian CFD is somewhat compensated for by the lower DC gain present due to the use of fractions near 50%.

Rise-Time Insensitivity of Binkley Gaussian CFDs with Linear-Edge Signals

The transfer function for the Binkley Gaussian CFD of any order contains one right-half-plane real zero in addition to left-half-plane poles and zeros. As mentioned earlier, Nowlin reported that only a single right-half-plane real zero is required in the shaping-network transfer function to give zero-crossing times that are insensitive to input rise-time for linear-edge input signals [5, 6]. Rise-time invariant operation is available only for input signals with rise-times greater than the zero-crossing time. This rise-time restriction also applies to amplitude-rise-time-compensated operation for the delay-line CFD.

Input-signal rise-time insensitivity was illustrated mathematically for the Nowlin CFD containing a single-pole high-pass filter. The transfer function of this Nowlin CFD circuit was later shown to be identical to the transfer function of the Binkley single-pole Gaussian CFD with an appropriate interchange of fraction values (the fraction value for the Binkley Gaussian circuit is one minus the fraction for the Nowlin circuit).

Figures 4-15 and 4-16 illustrate input-signal rise-time insensitivity for the single-pole and two-pole Binkley Gaussian CFDs. Linear-edge input signals with unity amplitude and rise-times of 2 s, 3 s, 5 s, and 10 s are shown in the figures along with the resulting shaping

signals. The CFDs are configured as indicated in the figures for zero-crossing times of 2 s at a fraction of 50%.

As observed in Figures 4-15 and 4-16, the shaping-signal slope transitions rapidly at the zero-crossing point for the signals with 2-s rise-time as this is at the threshold of rise-time invariant operation. Additionally, as observed in the figures, the two-pole constant-fraction circuit provides higher shaping-signal underdrive and zero-crossing slope compared to the single-pole circuit. Shaping-signal underdrive and zero-crossing slope is higher for higher-order Binkley Gaussian CFDs for both linear-edge input signals and lowpass-filtered step-input signals. Finally, as observed in the figures, underdrive decreases as input-signal rise-time increases placing practical limits on the maximum input-signal rise-time.

Comparison of Delay-Line and Non-Delay-Line CFD Performance for Lowpass-Filtered Step Signals

Comparison for Single-Pole Step Signals

It is useful to compare the performance of delay-line and Binkley Gaussian CFDs for single-pole step-input signals. In the first comparison, a zero-crossing time of twice the input-signal time-constant ($t_{cf} = 2t_{in}$) is considered which corresponds to triggering at 86% of the peak input-signal amplitude. The shaping signals for the delay-line CFD and Binkley single-, two-, three-, and four-pole Gaussian CFDs are shown in Figure 4-17. Delay values have been chosen to obtain the desired zero-crossing time of twice the input-signal time-constant. The standard fraction of 20% has been chosen for the delay-line CFD, and fractions of 50% have been chosen for the Binkley Gaussian CFDs because timing jitter is generally minimized for this value as discussed earlier. In Table 4-4, CFD shaping-signal underdrive, overdrive, zero-crossing slope, noise, and timing jitter are compared for the signals shown in Figure 4-17.

The Binkley Gaussian CFDs provide a bipolar timing signal similar in shape to the one provided by the delay-line CFD. The underdrive of the Binkley Gaussian circuits is comparable to that of the delay-line circuit except that underdrive in the Binkley Gaussian circuits is significantly greater during the initial part of the signal. This higher initial underdrive is advantageous for driving the constant-fraction comparator more rapidly out of baseline noise. Higher initial underdrive occurs because of the high fraction used in the Binkley Gaussian circuits. The overdrive, however, is somewhat less for the Binkley Gaussian circuits because of the higher fraction used. More importantly, however, the zero-crossing slope is considerably less for the Binkley Gaussian circuits because of bandwidth

Table 4-4. Comparison of Delay-Line and Non-Delay-Line CFD Performance for Single-Pole Step Inputs (Zero-Crossing Time at $2t_{in}$).

Circuit Configuration			Normalized Circuit Performance				
Topology	**Delay**	**Fraction**	**Underdrive**	**Overdrive**	**Zero-Cross Slope**	**Output Noise**	**Timing Jitter**
	$\frac{t_d}{t_{in}}$	(f)	$\frac{V_{und}}{V_{inpk}}$	$\frac{V_{ovr}}{V_{inpk}}$	$\frac{K_{zero}}{K_{inpk}}$	$\frac{\sigma_{vcf}}{\sigma_{vin}}$	$\frac{\sigma_{tcf}}{\sigma_{tin\,(min)}}$
Delay Line	1.805	0.2	-0.167	0.8	0.8	0.987	1.234
Binkley Gaussian, 1-pole	1.770	0.5	-0.157	0.5	0.176	0.500	2.861
Binkley Gaussian, 2-pole	1.059	0.5	-0.201	0.5	0.245	0.611	2.492
Binkley Gaussian, 3-pole	0.826	0.5	-0.225	0.5	0.287	0.666	2.316
Binkley Gaussian, 4-pole	0.702	0.5	-0.242	0.5	0.318	0.701	2.204

Input signal is 1-pole lowpass-filtered step input with time-constant t_{in}.
Normalization details given in Table A-1 for input signal.
Zero-crossing time (t_{cf}) is at $2t_{in}$.

limiting in the Gaussian lowpass filter used for delay-line approximation. The reduced zero-crossing slope results in increased timing jitter for the Binkley Gaussian circuits even though the shaping-signal output noise is lower. The timing jitter for the four-pole Binkley Gaussian CFD is 220% of the minimum input-signal timing jitter compared to 123% for the delay-line circuit.

In the second comparison, a zero-crossing time equal to the input-signal time-constant ($t_{cf} = 1t_{in}$) is considered which corresponds to triggering at 63% of the peak input-signal amplitude. Triggering earlier on the input signal (compared to the previous example) will result in less rise-time sensitivity, and as shown later, will result in better statistical performance with scintillation detectors. The shaping signals for the delay-line CFD and Binkley single-, two-, three-, and four-pole Gaussian CFDs are shown in Figure 4-18. Again, delay values have been chosen to obtain the desired zero-crossing time, the standard fraction of 20% has been chosen for the delay-line CFD, and fractions of 50% have been

chosen for the Binkley Gaussian CFDs. In Table 4-5, CFD shaping-signal underdrive, overdrive, zero-crossing slope, noise, and timing jitter are compared for the signals shown in Figure 4-18.

The underdrive of the Binkley Gaussian circuits is again comparable to that of the delay-line circuit and is significantly greater during the initial part of the signal. The overdrive is, again, somewhat less for the Binkley Gaussian circuits because of the higher fraction used. However, the zero-crossing slope is not as reduced for the Binkley Gaussian circuits set at the shorter zero-crossing time compared to the previous circuits set at higher zero-crossing time. This is because of the shorter delay and corresponding wider bandwidth of the Gaussian lowpass filter used for delay-line approximation in the circuits configured for shorter zero-crossing times. The improved zero-crossing slope at shorter zero-crossing time results in reduced timing jitter. The timing jitter for the four-pole Binkley Gaussian CFD is 167% of the minimum input-signal timing jitter compared to 117% for the delay-line circuit.

Table 4-5. Comparison of Delay-Line and Non-Delay-Line CFD Performance for Single-Pole Step Inputs (Zero-Crossing Time at $1t_{in}$).

Circuit Configuration			Normalized Circuit Performance				
Topology	**Delay**	**Fraction**	**Underdrive**	**Overdrive**	**Zero-Cross Slope**	**Output Noise**	**Timing Jitter**
	$\frac{t_d}{t_{in}}$	(f)	$\frac{V_{und}}{V_{inpk}}$	$\frac{V_{ovr}}{V_{inpk}}$	$\frac{K_{zero}}{K_{inpk}}$	$\frac{\sigma_{vcf}}{\sigma_{vin}}$	$\frac{\sigma_{tcf}}{\sigma_{tin\,(min)}}$
Delay Line	0.861	0.2	-0.115	0.8	0.8	0.933	1.167
Binkley Gaussian, 1-pole	0.758	0.5	-0.087	0.5	0.231	0.500	2.165
Binkley Gaussian, 2-pole	0.457	0.5	-0.114	0.5	0.312	0.586	1.873
Binkley Gaussian, 3-pole	0.368	0.5	-0.129	0.5	0.359	0.626	1.745
Binkley Gaussian, 4-pole	0.305	0.5	-0.140	0.5	0.390	0.651	1.672

Input signal is 1-pole lowpass-filtered step input with time-constant t_{in}.
Normalization details given in Table A-1 for input signal.
Zero-crossing time (t_{cf}) is at $1t_{in}$.

The choice of circuit order for the Binkley Gaussian CFD is dependent upon the desired underdrive, zero-crossing slope, and timing-jitter performance. The performance is better (more underdrive, more zero-crossing slope, and lower timing jitter) for the higher-order circuits. The two-pole circuit has considerably better performance over the single-pole circuit, but performance improvements diminish as circuit order continues to increase. Although circuit gain can be used to compensate for the lower overdrive and zero-crossing slope present in the Binkley Gaussian CFD, the timing jitter fundamentally limits the performance.

Binkley Gaussian CFD performance is inferior to that of the delay-line CFD for single-pole step-input signals because it is not possible (at reasonable circuit order) to sufficiently maintain the high initial slope of the single-pole step-input signal. However, the Binkley Gaussian CFD is useful for single-pole step inputs where system timing is not limiting by electronic-noise-induced timing jitter. Such applications include BGO/photomultiplier scintillation detector systems. As mentioned earlier, the single-pole Binkley Gaussian CFD is equivalent to the Nowlin CFD containing a single-pole highpass filter if the fraction value for the Binkley Gaussian circuit is adjusted to one minus the fraction value of the Nowlin circuit.

Comparison for Two-Pole Step Signals

In addition to comparing the performance of delay-line and Binkley Gaussian CFDs for single-pole step-input signals, it is useful to compare the performance for two-pole step-input signals. The two-pole step-input signal is more representative of higher-order lowpass-filtered step-input signals because of its low initial slope and constant slope over an appreciable portion of the signal. In the first comparison, a zero-crossing time of again twice the input-signal time-constant ($t_{cf} = 2t_{in}$) is considered which corresponds to triggering at 77% of the peak input-signal amplitude. The shaping signals for the delay-line CFD and Binkley single-, two-, three-, and four-pole Gaussian CFDs are shown in Figure 4-19. Again, delay values have been chosen to obtain the desired zero-crossing time, the standard fraction of 20% has been chosen for the delay-line CFD, and fractions of 50% have been chosen for the Binkley Gaussian CFDs. In Table 4-6, CFD shaping-signal underdrive, overdrive, zero-crossing slope, noise, and timing jitter are compared for the signals shown in Figure 4-19.

Table 4-6. Comparison of Delay-Line and Non-Delay-Line CFD Performance for Two-Pole Step Inputs (Zero-Crossing Time at $2t_{in}$).

Circuit Configuration			Normalized Circuit Performance				
Topology	**Delay**	**Fraction**	**Underdrive**	**Overdrive**	**Zero-Cross Slope**	**Output Noise**	**Timing Jitter**
	$\frac{t_d}{t_{in}}$	(f)	$\frac{V_{und}}{V_{inpk}}$	$\frac{V_{ovr}}{V_{inpk}}$	$\frac{K_{zero}}{K_{inpk}}$	$\frac{\sigma_{vcf}}{\sigma_{vin}}$	$\frac{\sigma_{tcf}}{\sigma_{tin\,(min)}}$
Delay Line	1.503	0.2	-0.126	0.8	0.852	0.994	1.109
Binkley Gaussian, 1-pole	1.325	0.5	-0.101	0.5	0.332	0.500	1.506
Binkley Gaussian, 2-pole	0.796	0.5	-0.131	0.5	0.446	0.600	1.344
Binkley Gaussian, 3-pole	0.623	0.5	-0.148	0.5	0.510	0.648	1.271
Binkley Gaussian, 4-pole	0.530	0.5	-0.159	0.5	0.551	0.677	1.228

Input signal is 2-pole lowpass-filtered step input with time-constant t_{in} ($t_{in}/\sqrt{2}$ each pole).
Normalization details given in Table A-2 for input signal.
Zero-crossing time (t_{cf}) is at $2t_{in}$.

Again, the Binkley Gaussian CFDs provide a bipolar timing signal similar in shape to the one provided by the delay-line CFD. The underdrive of the Binkley Gaussian circuits is again comparable to that of the delay-line circuit, and the underdrive in the Binkley Gaussian circuits is significantly greater during the initial part of the signal. Note that the underdrive for all circuits is considerably less for the two-pole step-input compared to the single-pole step input described previously. This is because of the initial signal delay present for the two-pole step input. The overdrive is, again, somewhat less for the Binkley Gaussian circuits because of the higher fraction used. Also, the zero-crossing slope is again lower for the Binkley Gaussian circuits, but this reduction in slope is considerably lower for the two-pole step input compared to the single-pole step input described previously. The lower degradation of zero-crossing slope results in significantly improved timing jitter for the two-pole step input. The timing jitter for the four-pole Binkley Gaussian CFD is 123% of the minimum input-signal timing jitter compared to 111% for the delay-line circuit.

In the second comparison, a zero-crossing time equal to the input-signal time-constant ($t_{cf} = 1t_{in}$) is considered which corresponds to triggering at 41% of the peak input-signal

amplitude. As in the single-pole step-input case, triggering earlier on the input signal will result in less rise-time sensitivity and better statistical performance with scintillation detectors. The shaping signals for the delay-line CFD and Binkley single-, two-, three-, and four-pole Gaussian CFDs are shown in Figure 4-20. Again, delay values have been chosen to obtain the desired zero-crossing time, the standard fraction of 20% has been chosen for the delay-line CFD, and fractions of 50% have been chosen for the Binkley Gaussian CFDs. In Table 4-7, CFD shaping-signal underdrive, overdrive, zero-crossing slope, noise, and timing jitter are compared for the signals shown in Figure 4-20.

The underdrive of the Binkley Gaussian circuits is again comparable to that of the delay-line circuit and is significantly greater during the initial part of the signal. The overdrive is, again, somewhat less for the Binkley Gaussian circuits because of the higher fraction used. Also, the zero-crossing slope is not as reduced for the Binkley Gaussian circuits set at the shorter zero-crossing time because of the shorter delay and corresponding wider bandwidth of the Gaussian lowpass filter used for delay-line approximation. The improved zero-crossing slope at shorter zero-crossing time results again in reduced timing

Table 4-7. Comparison of Delay-Line and Non-Delay-Line CFD Performance for Two-Pole Step Inputs (Zero-Crossing Time at $1t_{in}$).

Circuit Configuration			Normalized Circuit Performance				
Topology	**Delay**	**Fraction**	**Underdrive**	**Overdrive**	**Zero-Cross Slope**	**Output Noise**	**Timing Jitter**
	$\frac{t_d}{t_{in}}$	(f)	$\frac{V_{und}}{V_{inpk}}$	$\frac{V_{ovr}}{V_{inpk}}$	$\frac{K_{zero}}{K_{inpk}}$	$\frac{\sigma_{vcf}}{\sigma_{vin}}$	$\frac{\sigma_{tcf}}{\sigma_{tin\,(min)}}$
Delay Line	0.661	0.2	-0.051	0.8	0.614	0.858	1.399
Binkley Gaussian, 1-pole	0.516	0.5	-0.035	0.5	0.296	0.500	1.691
Binkley Gaussian, 2-pole	0.311	0.5	-0.045	0.5	0.382	0.542	1.419
Binkley Gaussian, 3-pole	0.244	0.5	-0.051	0.5	0.423	0.557	1.319
Binkley Gaussian, 4-pole	0.207	0.5	-0.055	0.5	0.446	0.566	1.269

Input signal is 2-pole lowpass-filtered step input with time-constant t_{in} ($t_{in}/\sqrt{2}$ each pole).
Normalization details given in Table A-2 for input signal.
Zero-crossing time (t_{cf}) is at $1t_{in}$.

jitter. The timing jitter for the four-pole Binkley Gaussian CFD is 127% of the minimum input-signal timing jitter compared to 140% for the delay-line circuit. Thus the four-pole Binkley Gaussian CFD exhibits comparable or superior timing-jitter performance to the delay-line CFD for this application.

As in the case of single-pole step inputs, the choice of circuit order for the Binkley Gaussian CFD is dependent upon the desired underdrive, zero-crossing slope, and timing-jitter performance. The performance, again, is better (more underdrive, more zero-crossing slope, and lower timing jitter) for the higher-order circuits. The two-pole Binkley Gaussian CFD circuit again has considerably better performance over the single-pole circuit, but performance improvements diminish as circuit order continues to increase. Again, circuit gain can be used to compensate for the lower overdrive and zero-crossing slope present in the Binkley Gaussian CFD, but the timing jitter fundamentally limits the performance.

Binkley Gaussian CFD performance is comparable to that of the delay-line CFD for two-pole step-input signals because it is possible (at reasonable circuit order) to sufficiently maintain the slope of the two-pole step-input signal. The reduction in zero-crossing slope present is, interestingly, nearly compensated for by the reduction in shaping-signal noise. The comparable timing-jitter performance of the Binkley Gaussian CFDs is quite significant for applications where electronic-induced timing jitter is a dominant component of system timing resolution. Such applications include BGO/avalanche-diode scintillation-detector systems. Independent of performance issues, the Binkley Gaussian CFDs have the advantage of requiring no delay line and may be implemented totally in monolithic integrated circuits.

CFD Performance with Scintillation Detectors

The performance of delay-line and non-delay-line CFDs has been given for deterministic (nonstatistical) signals with additive electronic noise. Knowledge of deterministic performance (shaping-signal underdrive, overdrive, zero-crossing time, and zero-crossing slope) is necessary for selecting constant-fraction comparators with adequate time-walk performance. Additionally, knowledge of circuit noise-induced timing jitter (using shaping-signal zero-crossing slope and noise) is necessary to evaluate this contribution of system timing resolution. Finally, knowledge of statistical performance with scintillation detectors is necessary to evaluate this often dominant contribution of system timing resolution.

Timing-Discrimination Performance

Monte Carlo Simulation of Timing Resolution

In *Section 3*, Monte Carlo simulation was described for predicting the timing resolution of scintillation detectors coupled to time pick-off systems. Monte Carlo simulation will be used here to predict CFD timing performance using the BGO-scintillator, photomultiplier, front-end amplifier, and CFD model shown in Figure 4-21. The BGO-scintillator and photomultiplier characteristics were described in *Section 3*. The front-end amplifier has a two-pole lowpass characteristic (time-constant of 4.545 ns/$\sqrt{2}$ for each pole) with a 10 - 90% rise-time of 10 ns. This front-end lowpass characteristic is representative of the front-end amplifiers used in Siemens/CTI PET systems [10]. Front-end amplifier noise is included for evaluation of timing jitter due to electronic-circuit noise. An input-noise voltage density of 4 nV/$\sqrt{\text{Hz}}$ is used which is representative for the noise of commercially-available high-speed bipolar current-feedback operational amplifiers.

In Figure 4-22, Monte Carlo simulated CFD signals are shown for twenty events for a delay-line CFD having a delay of 8 ns and fraction of 20%. A Gaussian energy spectrum with a mean of 511-keV and resolution of 14% FWHM, a mono-exponential BGO scintillation model with a yield of 300 (511 keV) and decay time constant of 300 ns, and the photomultiplier and front-end amplifier characteristics described in Figure 4-21 were used to generate the signals shown. The spread of CFD output zero crossings clearly illustrates the timing performance available for the PET BGO/photomultiplier detector and CFD timing system considered.

In Monte Carlo analysis of CFD timing resolution, Compton scatter (which is normally present at energies below the Gaussian energy spectrum) will be considered in the detector energy spectrum. Compton scatter is added to the Gaussian energy spectrum in the Monte Carlo simulation program (this program described in *Appendix B*) by a special algorithm [11]. This algorithm operates by transforming uniformly-distributed (0 - 1) random numbers into a uniform distribution (0 - 1) having an added impulse distribution at one. The resultant random numbers are then provided to the existing Gaussian transformation algorithm to provide a distribution representative of Compton scatter with a Gaussian detector photopeak. The energy spectrum used for CFD timing-resolution analysis is shown in Figure 4-23 and consists of a Gaussian photopeak with a mean of 511 keV and resolution of 14% added to low-energy Compton scatter. Only events above 200 keV are shown in the energy spectrum to model CFD energy discrimination. The energy resolution and Compton-scatter level in Figure 4-23 closely models experimentally measured energy spectra for a

BGO/photomultiplier scintillation detector with a 1 x 1 x 1-inch BGO crystal excited by coincident 511-keV gamma rays from a ^{22}Na point source.

CFD energy discrimination is considered by accepting only events above 200 keV as shown in Figure 4-23. This is equivalent to a CFD energy threshold of 200 keV and infinitely sharp energy resolution. Actual CFD energy resolution is not infinitely sharp because of limited photoelectron statistics, but accurate timing resolution can be obtained (as will be shown in comparisons with measured data) using the energy spectrum of Figure 4-23 since events rejected above 200 keV in practical CFDs are largely compensated for by events accepted below 200 keV. The arming circuitry shown in Figure 4-21 is not used in the Monte Carlo timing analysis as all detector events are collected from the spectrum shown in Figure 4-23. Actual CFD energy-discrimination performance will be modeled mathematically and by Monte Carlo methods later in this section.

Comparison of Monte Carlo Delay-Line and Non-Delay-Line CFD Timing Resolution

Monte Carlo simulated FWHM timing resolution (as a function of delay time) is shown in Figure 4-24 for the delay-line CFD (fraction of 20%) and the Binkley single-, two-, three-, and four-pole Gaussian CFD (fraction of 50%). Additionally, Monte Carlo simulated FWTM timing resolution is shown in Figure 4-25. In order to obtain the numerous Monte Carlo simulations required, a program was developed that called SPICE simulations for calculating CFD impulse response. This program then called the Monte Carlo simulation program and later reported the results to a file. Statistical noise is present in the Monte Carlo timing-resolution data of Figures 4-24 and 4-25 even though 100,000 events were used for each Monte Carlo simulation. Simulations for all five CFD circuits required an execution time of over 300 hours on a SUN Sparcstation 2 computer.

Monte Carlo FWHM (Figure 4-24) and FWTM (Figure 4-25) timing resolution was evaluated for the delay-line CFD using both the mono-exponential and tri-exponential BGO scintillation models. As described in *Section 3*, the mono-exponential model represents scintillation having an instantaneous rise time followed by a single-exponential decay with time constant of 300 ns. The tri-exponential model represents scintillation having a finite rise-time (rise-time time constant of 1.5 ns) followed by exponential decay with time constant of 300 ns for 90% of the light and exponential decay with time constant of 60 ns for 10% of the light.

Monte Carlo and measured FWHM (Figure 4-24) and FWTM (Figure 4-25) timing resolution is in very good agreement for the tri-exponential BGO scintillation model for the

delay-line CFD considered with delays between 4 and 12 ns. Monte Carlo timing resolution using the mono-exponential model, however, significantly underestimates (making it appear lower or better) timing resolution for constant-fraction delays below 6 ns. The comparison of Monte Carlo and measured timing resolution for the delay-line CFD considered has been previously reported by the author [12].

As discussed in *Section 3*, the tri-exponential BGO scintillation model closely matches the model reported by Moszynski et al. [13]. All future Monte Carlo simulations of CFD timing- and energy-discrimination performance will be performed using the tri-exponential BGO scintillation model because of the very good agreement between Monte Carlo and measured delay-line CFD resolution (Figures 4-24 and 4-25).

Experimental measurements of delay-line CFD timing resolution were made with the photomultiplier and front-end characteristics described in Figure 4-21 using a 1 x 1 x 1-inch BGO crystal excited by coincident 511-keV gamma rays from a ^{22}Na point source. An energy threshold of 200 keV (as used in Monte Carlo simulations) was used for all experimental CFD measurements, which were made with a commercial Tennelec 455 [14] NIM (Nuclear Instrumentation Module) delay-line CFD. All CFD measurements were made as described in the EG&G application note, AN-42 [1]

The timing resolution data of Figures 4-24 and 4-25 indicates that equivalent timing resolution is available for both the delay-line and Binkley Gaussian CFDs. Timing resolution decreases (improves) as constant-fraction delay decreases and theoretically approaches the timing resolution available for first photoelectron timing. First-photoelectron timing resolution is approximately 2.06 ns FWHM (Figure 3-15, page 96) for the detector under consideration due mostly to the Poisson statistical noise of 1.98 ns FWHM (Figure 3-12, page 94).

Although timing resolution decreases with decreasing constant-fraction delay, shaping-signal underdrive and zero-crossing slope also decrease placing practical restrictions on the choice of constant-fraction delay. Mean shaping-signal zero-crossing time, underdrive, zero-crossing slope, and timing jitter are shown in Figures 4-26, 4-27, 4-28, and 4-29. The mean shaping-signal performance was found by applying a step input at the photomultiplier lowpass-filter model (Figure 4-21) assuming a constant photoelectron rate of 1.0/ns (300 photoelectrons/300 ns using the mono-exponential scintillation model) at 511 keV. Monte Carlo simulated shaping-signal underdrive and zero-crossing slope were also found, but these are near the mean shaping-signal values for timing resolutions of 3 ns FWHM or greater and are not reported. At timing resolutions significantly below 3 ns FWHM,

shaping-signal underdrive and zero-crossing slope are reduced from the mean value, ultimately approaching levels given by the shaping-signal impulse response. Mean shaping signal overdrive is not given, but is equal to $(1 - f)\ V_{inpk}$ where V_{inpk} is the CFD mean input-signal amplitude (0.801 V for a photoelectron rate of 1.0/ns for the circuit model of Figure 4-21).

It is useful to compare shaping-signal underdrive, zero-crossing slope, zero-crossing time, and timing jitter for the delay-line and Binkley Gaussian CFDs when these circuits are configured for equal timing resolution. This comparison is shown in Table 4-8 for a timing resolution of approximately 3.275 ns FWHM.

As shown in Table 4-8, shaping-signal underdrive, zero-crossing slope, and overdrive are less for the Binkley Gaussian circuits compared to the delay-line circuit when both circuits are configured for equal timing resolution. Additionally, the timing jitter for the Binkley Gaussian circuits is higher compared to the delay-line circuit because of lower zero-crossing slope. Interestingly, the zero-crossing time for the Binkley Gaussian circuits is less than that of the delay-line circuit. This was first discovered after finding that the timing resolution of the Binkley Gaussian circuits is worse than that of the delay-line circuit when

Table 4-8. Comparison of Delay-Line and Non-Delay-Line CFD Performance for Equal Timing Resolution.

Circuit Configuration		Circuit Performance					
Topology	**Delay**	**Zero-Cross Time**	**Under-drive**	**Over-drive**	**Zero-Cross Slope**	**Timing Jitter**	**FWHM Timing Res.**
	(ns)	(ns)	(V)	(V)	(V/ns)	(ns rms)	(ns rms)
Delay Line	8.0	13.881	-0.080	0.641	0.049	0.049	3.288
Binkley, 1-pole Gaussian	3.5	9.553	-0.026	0.401	0.019	0.067	3.261
Binkley, 2-pole Gaussian	2.1	9.545	-0.033	0.401	0.024	0.060	3.283
Binkley, 3-pole Gaussian	1.6	9.411	-0.035	0.401	0.026	0.058	3.286
Binkley, 4-pole Gaussian	1.3	9.171	-0.035	0.401	0.026	0.058	3.263
Fraction for delay-line circuit is 20%. Fraction for Binkley Gaussian circuits is 50%. Detector and circuit details given in Monte Carlo circuit model.							

both circuits are configured for the same zero-crossing time. In order to obtain equal timing resolution, it is necessary to configure the Binkley Gaussian circuits for shorter zero-crossing time.

As was the case for single- and two-pole step inputs, shaping-signal underdrive and zero-crossing slope improve for higher order Binkley Gaussian circuits, approaching the performance of the delay-line circuit. Additionally, timing jitter improves (decreases) for higher-order Binkley Gaussian circuits. The timing jitter for the four-pole Binkley Gaussian circuit is near that of the delay-line circuit, having a value of 58 ps rms compared to 49 ps rms for the delay-line circuit. Timing jitter fundamentally limits circuit performance whereas lower shaping-signal underdrive and zero-crossing slope can be compensated for by additional circuit gain. Shaping-signal underdrive, overdrive, and zero-crossing slope for the four-pole Binkley Gaussian circuit are comparable to that of the delay-line circuit if a gain of two is included in the Binkley Gaussian circuit. This extra gain is included in the monolithic CMOS CFD described in *Section 5*.

Energy-Discrimination Performance

Statistical Analysis of Energy Discrimination

In scintillation-detector applications, Compton scatter is present at energies below the detector photopeak. In BGO PET applications, a low level of Compton scattering occurs within the scintillation detector itself and a considerably higher level occurs within the patient being imaged. It is important to assess the ability of a CFD to discriminate against unwanted Compton scattered events since triggering on these events increases system processing deadtime and counting losses. Additionally, it is important to assess photopeak losses due to limited CFD energy resolution. Loss of detector photopeak events results in reduced efficiency in a PET tomograph.

A CFD provides detector energy discrimination through the operation of its arming circuitry. Ideally, a CFD would accept all events having energy above the selected arming threshold while rejecting all events having energy below this threshold. In scintillation detector systems, however, the sharpness of energy discrimination is degraded significantly due to limited accumulation of photoelectron statistics in the short time interval available for circuit arming. This effect is particularly severe for low photoelectron-yield scintillators such as BGO.

The ratio of arming-signal standard deviation (square-root of variance) to arming-signal mean provides an indication of CFD energy-discrimination resolution. It is desirable to

minimize this resolution ratio by minimizing the arming-signal standard deviation and maximizing the arming-signal mean. The mean and variance can be found from Campbell's theorem since the arming signal results from a linear system excited by Poisson-distributed impulses [15]. From the Campbell's theorem discussion in *Section 3*, the statistical mean (Equation 3-15, page 73) was given by

$$\mu(t \geq 0) = r_0 \int_0^t h(\tau) d\tau \quad , \tag{4-77}$$

and the statistical variance (Equation 3-16, page 73) was given by

$$\sigma^2(t \geq 0) = r_0 \int_0^t h^2(\tau) d\tau \quad . \tag{4-78}$$

In Equations 4-77 and 4-78, the photoelectron-emission rate is assumed to be a step function having a value of zero for times before detector event interaction ($t < 0$) and a value of r_0 for times after detector event interaction ($t > 0$). Additionally, the linear-system impulse response ($h(t)$) is assumed to be causal. The mean and variance described by Campbell's theorem do not describe a Gaussian process unless the number of collected photoelectrons is sufficiently large (a number greater than ten will yield a process that is nearly Gaussian).

The resolution ratio of arming-signal standard deviation (square-root of variance) to arming-signal mean is plotted in Figure 4-30 as a function of arming-decision time for the CFD model of Figure 4-21. A single-pole lowpass arming filter (described by $H_{arm}(s)$ in Figure 4-21) is considered with a time-constant of 0 ns (arming directly on the input signal), 4 ns, and 9 ns. The single-pole lowpass-filter responses used are taken from the selectable-bandwidth arming filter used in the CMOS CFD (described in *Section 5*). The impulse response ($h(t)$) used for the data of Figure 4-30 includes the photomultiplier, the front-end amplifier, and arming filter as shown in the CFD model of Figure 4-21. In addition to the resolution ratios of CFD arming-signal standard deviation to arming-signal mean shown, the theoretical limit or lowest possible arming-signal resolution ratio is also shown in Figure 4-30. This theoretical limit occurs if all detector photoelectrons are collected, which would occur if the photomultiplier, front-end amplifier, and arming-filter impulse response was that of a pure integrator (impulse response equal to a step function).

In Figure 4-30, two arming-decision times are shown. The 12.3-ns decision time is equal to the CMOS CFD zero-crossing time (14.3 ns) less the required setup time (2 ns) of a D flip-flop used for arming qualification. The 22.3-ns decision time includes an additional 10-ns delay from an optional delay circuit at the output of the constant-fraction comparator. The use of this optional delay allows more time for the accumulation of arming statistics.

At the 12.3-ns arming-decision time (Figure 4-30), the resolution ratio of arming-signal standard deviation to arming-signal mean is equal to 33%, 38%, and 42% for an arming time-constant of 0 ns, 4 ns, and 9 ns, compared to a theoretical limit (minimum) of 28%. At the 22.3-ns decision time, the resolution ratio is significantly lower at approximately 26% for all three arming time-constants, compared to a theoretical limit of 21%. For early decision times, the resolution ratio is lower at minimum arming time-constants because more photoelectron statistics are available due to less delay in the arming impulse response. In contrast, for later decision times, the resolution ratio is lower at higher arming time-constants because less photoelectron statistics are lost (forgotten) due to longer decay time in the arming impulse response. The optimum arming-filter time-constant results in a resolution ratio that just reaches its minimum value at the decision time of interest. The resolution ratio reaches a constant minimum at an equilibrium point where incoming photoelectron statistics just equals the statistics lost due to impulse response decay.

It is interesting to note that the arming filter for optimal (minimal) arming-signal resolution is not a pure integrator (approximated by a large arming single-pole time-constant) for the 12.3-ns and 22.3-ns decision times. This is counter-intuitive since an integrator by itself optimally collects photoelectron statistics. The arming impulse response, however, consists of the convolution of photomultiplier, front-end amplifier, and arming-filter impulse responses so the use of an integrator as the arming filter does not yield a total impulse response equivalent to that of an integrator.

In *Section 5*, Monte Carlo and measured spectra (energy and timing) will be presented for the CMOS CFD. The CMOS CFD will be configured with and without an optional 10-ns delay at the output of the constant-fraction comparator. This will illustrate the improvement in energy-discriminator performance resulting from delaying the arming-decision time.

Monte Carlo Simulation of Energy-Discrimination Performance

In the previous Monte Carlo CFD timing simulations, a fixed Gaussian energy spectrum was used with added low-energy Compton scatter (Figure 4-23) to represent the energy spectrum from a BGO/photomultiplier detector excited by coincident 511-keV gamma rays from a ^{22}Na point source. The effects of CFD energy discrimination on timing performance

were considered by using only event energies above 200 keV to represent ideal CFD energy discrimination with an energy threshold of 200 keV.

In addition to the generation of a timing spectrum for a given input energy spectrum, it is possible to generate the accepted and rejected energy spectra associated with CFD energy discrimination using Monte Carlo techniques. The degree of Compton scatter rejection, along with the degree of photopeak acceptance, can then be used as an indication of CFD energy-discrimination performance.

CFD energy discrimination is simulated in a second Monte Carlo program (the previous Monte Carlo program was described in *Section 3* and *Appendix B*) by the addition of a statistically generated arming signal. This signal is generated identically to the constant-fraction signal except that the arming-system impulse response is used. An event is accepted if the arming signal exceeds a selectable arming threshold prior to the arming decision time. The arming decision time is equal to the zero-crossing time of the constant-fraction signal (generated in the Monte Carlo program) plus a selectable constant-fraction comparator delay less a selectable arming D flip-flop set-up time. A selectable delay at the output of the constant-fraction comparator is included in the Monte Carlo program to evaluate the improvement in CFD energy-discrimination available by delaying the arming decision time. The energy spectra associated with all detector events, events accepted by the CFD, and events rejected by the CFD are histogrammed by the Monte Carlo program along with the timing spectra associated with accepted events. As in previous Monte Carlo CFD timing simulations, Monte Carlo simulation of energy and timing performance is done using the circuit model shown in Figure 4-21.

Comparison of Monte Carlo and Measured Energy-Discrimination and Timing Performance for a Commercial Delay-Line CFD

Monte Carlo energy-discrimination and timing performance was simulated for a commercial Tennelec 455 [14] NIM (Nuclear Instrumentation Module) delay-line CFD using the circuit model shown in Figure 4-21. A detector energy spectrum (consisting of a Gaussian photopeak with a mean of 511 keV and resolution of 14% added to low-energy Compton scatter) was used to model the BGO/photomultiplier detector (with a 1 x 1 x 1 inch BGO crystal) excited by coincident 511-keV gamma rays from a ^{22}Na point source. The constant-fraction signal impulse response and the arming-signal impulse response were taken from SPICE simulations of a delay-line CFD having a delay time of 8 ns and a fraction of 20%. No arming filter was used as the arming comparator is connected directly to the input signal in the commercial CFD. Additionally, no optional constant-fraction delay

(included to delay the arming-decision time and improve energy-discrimination performance) was used as this is not provided in the commercial CFD. Finally, an arming D flip-flop set-up time of 2 ns was used to represent the set-up time of the ECL D flip-flop circuit contained in the commercial NIM CFD module.

Monte Carlo total-event, accepted-event, and rejected-event energy spectra are shown in Figure 4-31 for the commercial delay-line CFD. The arming threshold was set for a 200-keV energy threshold which is determined by the intersection of the accepted-event and rejected-event spectra. The Monte Carlo timing spectrum associated with the accepted-event energy spectra of Figure 4-31 is shown in Figure 4-32.

Measured total-event, accept-event, and rejected-event energy spectra are shown in Figure 4-33 for the commercial delay-line CFD. Again, the arming threshold was set for a 200-keV energy threshold. The measured timing spectrum associated with the accepted-event energy spectra of Figure 4-33 is shown in Figure 4-34. All measurements were made as described in the EG&G application note, AN-42 [1].

The Monte Carlo (Figure 4-31) and measured (Figure 4-33) CFD energy spectra are in good agreement, the primary difference being the presence of a backscatter peak at approximately 175 keV in the measured spectra. This backscatter peak is not modeled in Monte Carlo simulation since a uniform distribution of Compton scatter is assumed. The CFD 511-keV photopeak loss is 2.2% for Monte Carlo simulation which is in good agreement with the measured loss of 2.5%. CFD photopeak loss is due to poor energy-discrimination performance caused by limited accumulation of arming statistics. Minimizing CFD photopeak loss is significant in PET systems since the loss of valid photopeak events results in decreased detection efficiency. Limited CFD energy-discrimination performance can be observed in the Monte Carlo and measured energy spectra from the shallow edges of the rejected and accepted spectra.

The Monte Carlo (Figure 4-32) and measured (Figure 4-34) CFD timing spectra are in good agreement, with a Monte Carlo timing resolution of 3.22 ns FWHM compared to a measured timing resolution of 3.30 ns FWHM. Additionally, the shape of the Monte Carlo and measured timing spectra are in good agreement, with a Monte Carlo FWTM timing resolution of 6.41 ns compared to a measured FWTM timing resolution of 6.4 ns. Comparisons of both Monte Carlo and measured timing and energy spectra for the BGO/photomultiplier detector and CFD timing system considered have been previously reported by the author [12].

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Appendix for Section 4 — Figures

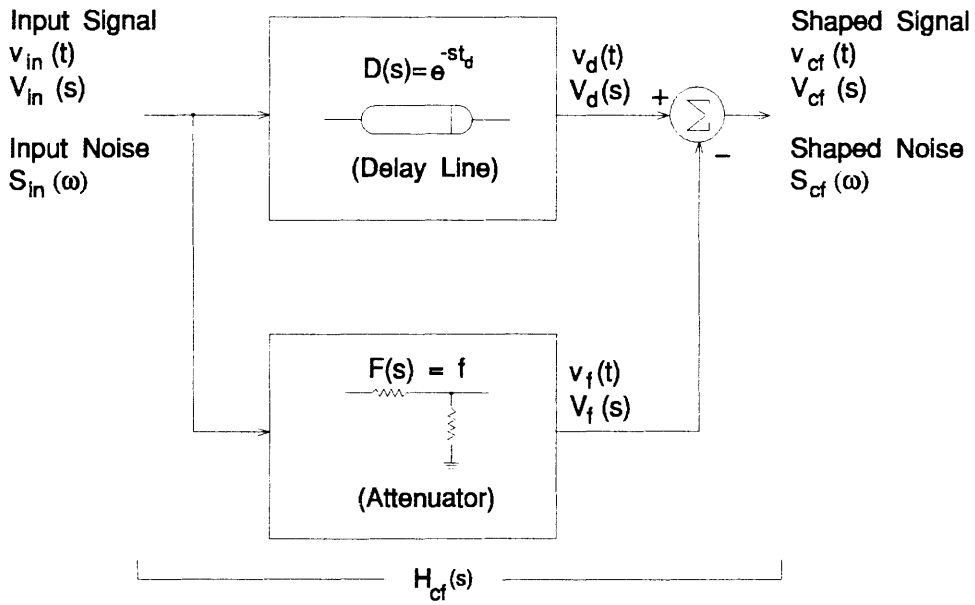


Figure 4-1. Delay-Line CFD Circuit Model.

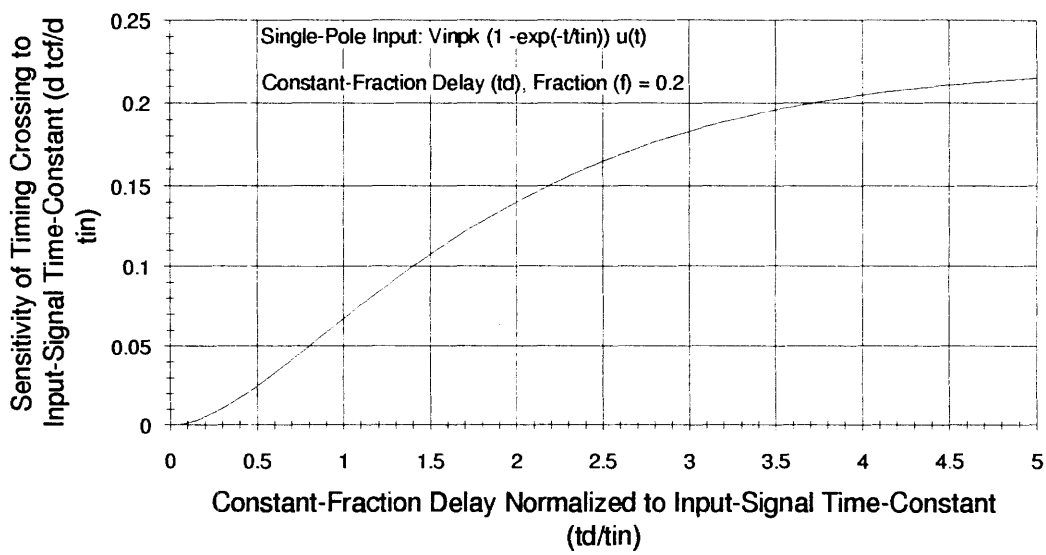


Figure 4-2. Delay-Line CFD Timing Sensitivity to Input-Signal Time-Constant for Single-Pole Step Input.

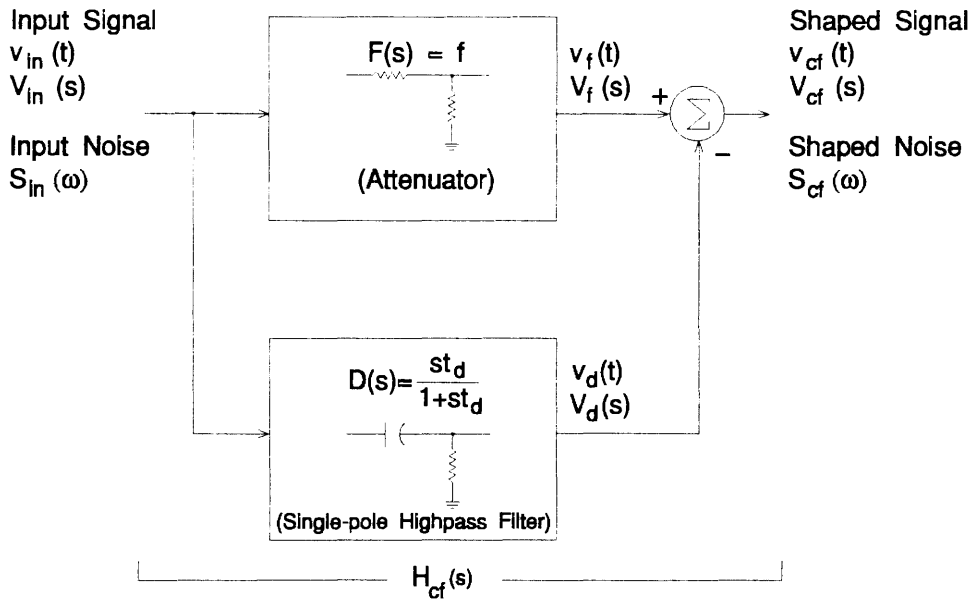


Figure 4-3. Nowlin CFD Circuit Model.

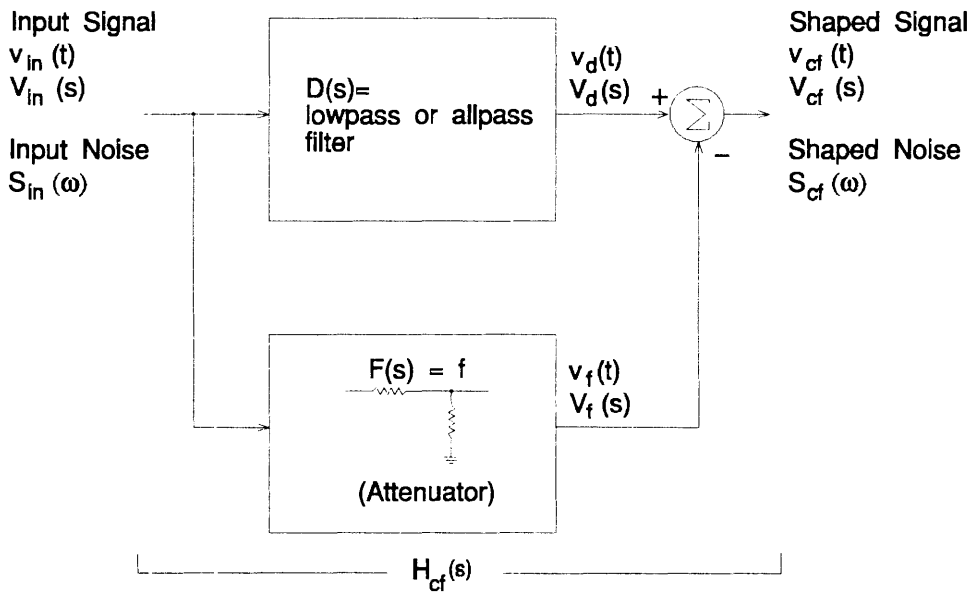


Figure 4-4. Binkley CFD Circuit Model.

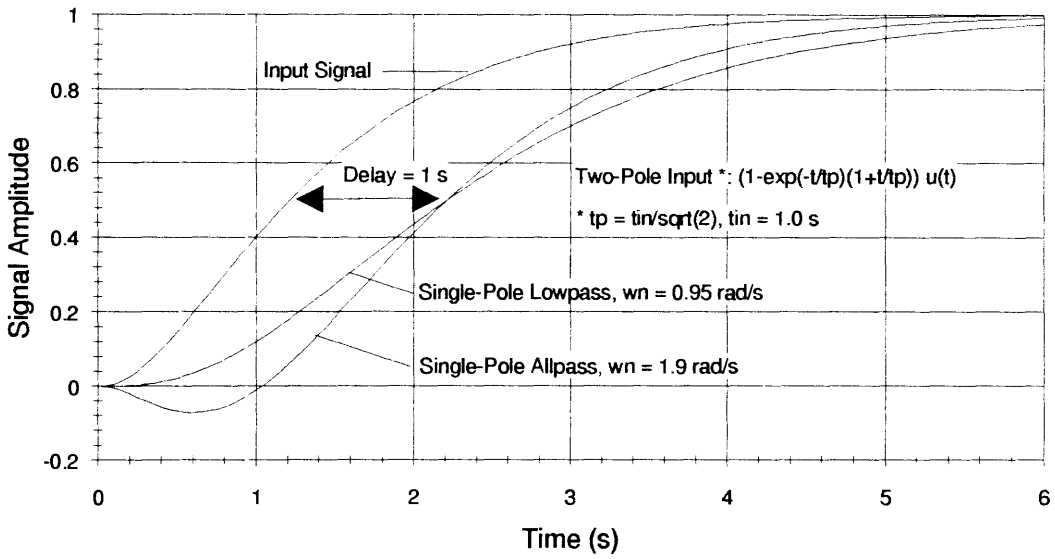


Figure 4-5. Output Signals of First-Order Lowpass, Allpass Delay-Line Approximation Filters.

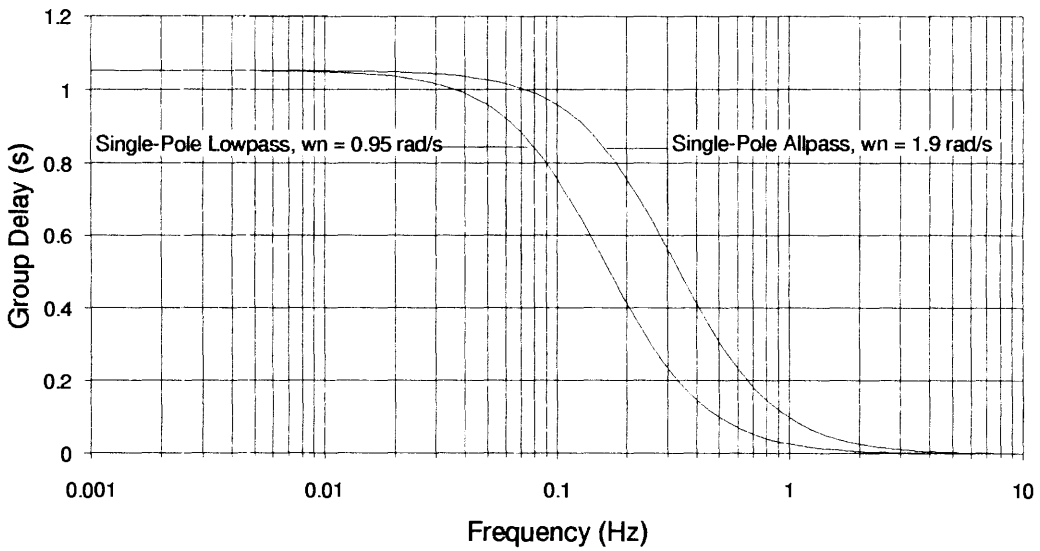


Figure 4-6. Group Delay of First-Order Lowpass, Allpass Delay-Line Approximation Filters.

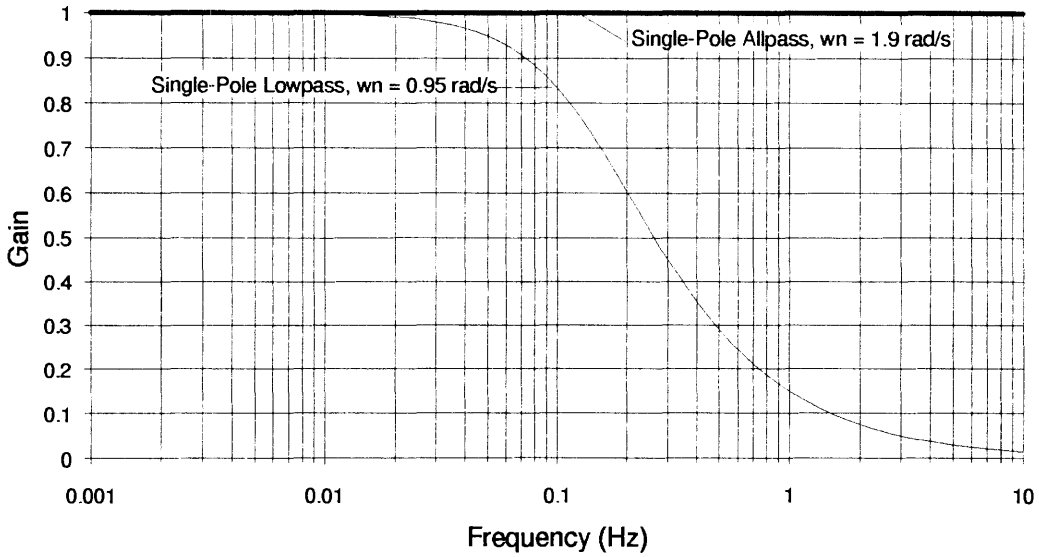


Figure 4-7. Frequency Response of First-Order Lowpass, Allpass Delay-Line Approximation Filters.

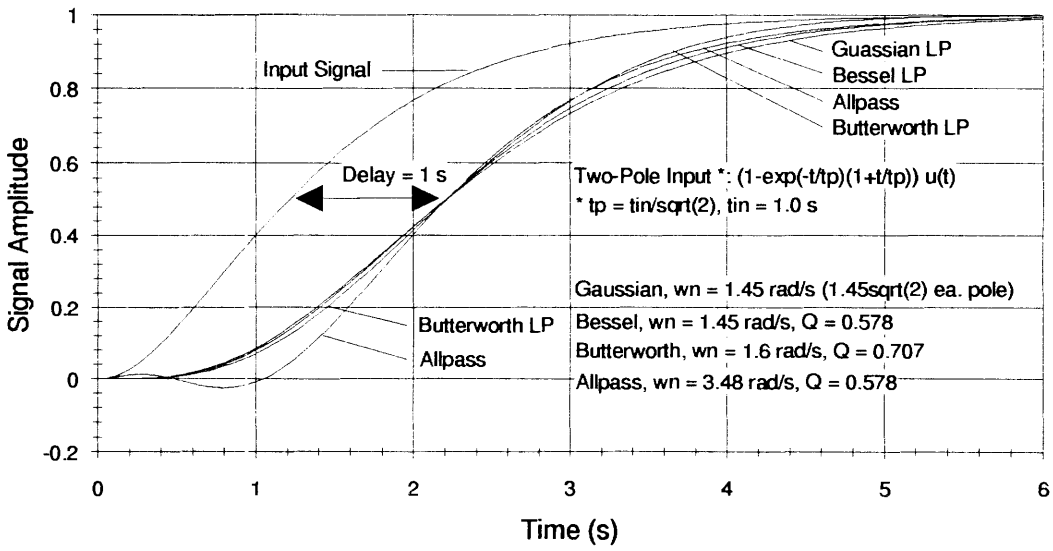


Figure 4-8. Output Signals of Second-Order Lowpass, Allpass Delay-Line Approximation Filters.

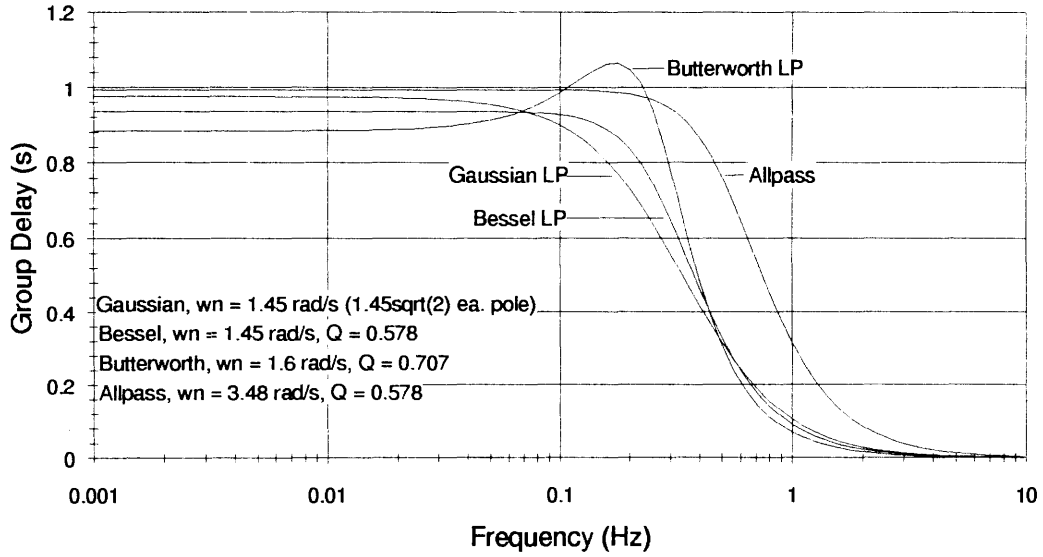


Figure 4-9. Group Delay of Second-Order Lowpass, Allpass Delay-Line Approximation Filters.

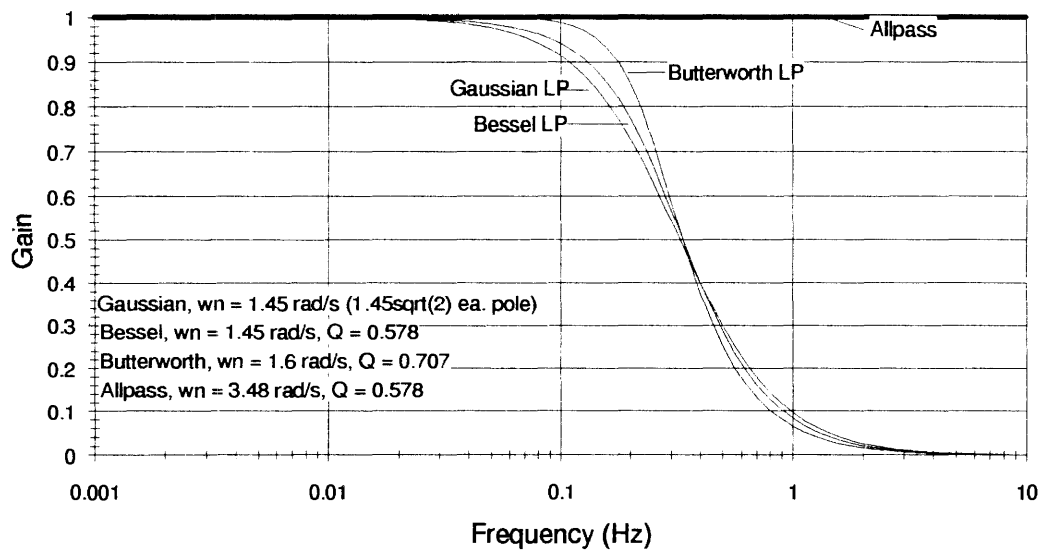


Figure 4-10. Frequency Response of Second-Order Lowpass, Allpass Delay-Line Approximation Filters.

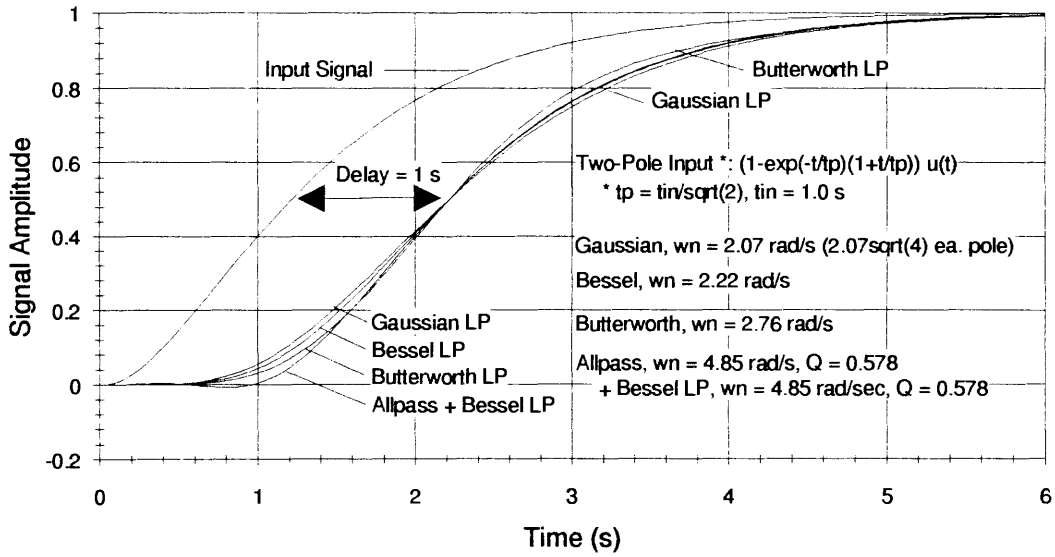


Figure 4-11. Output Signals of Fourth-Order Lowpass, Allpass Delay-Line Approximation Filters.

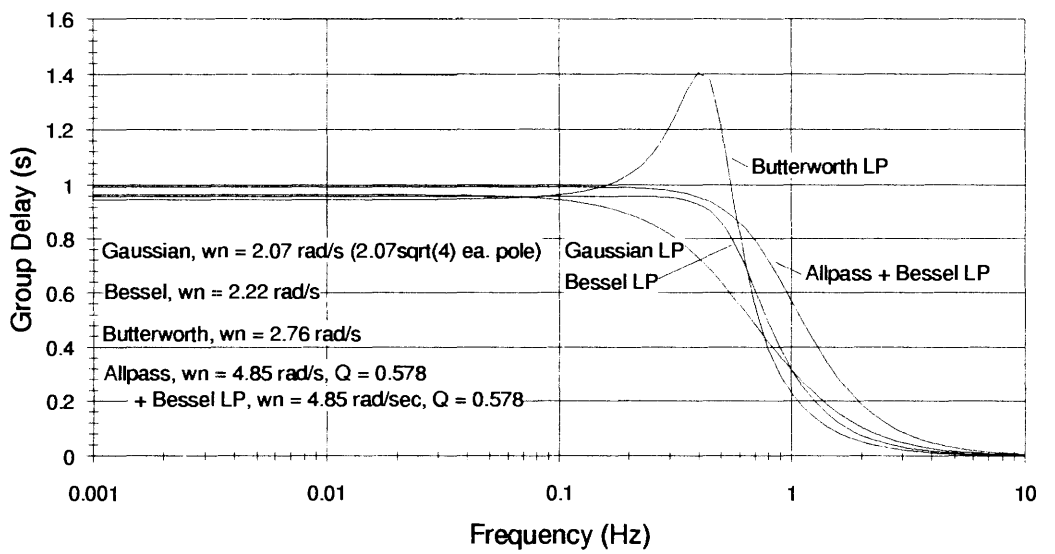


Figure 4-12. Group Delay of Fourth-Order Lowpass, Allpass Delay-Line Approximation Filters.

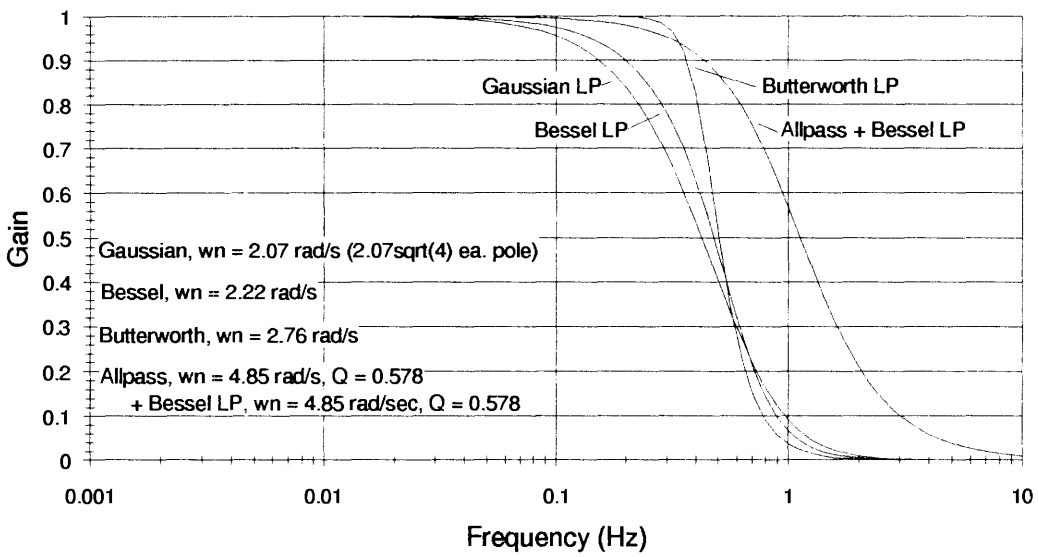


Figure 4-13. Frequency Response of Fourth-Order Lowpass, Allpass Delay-Line Approximation Filters.

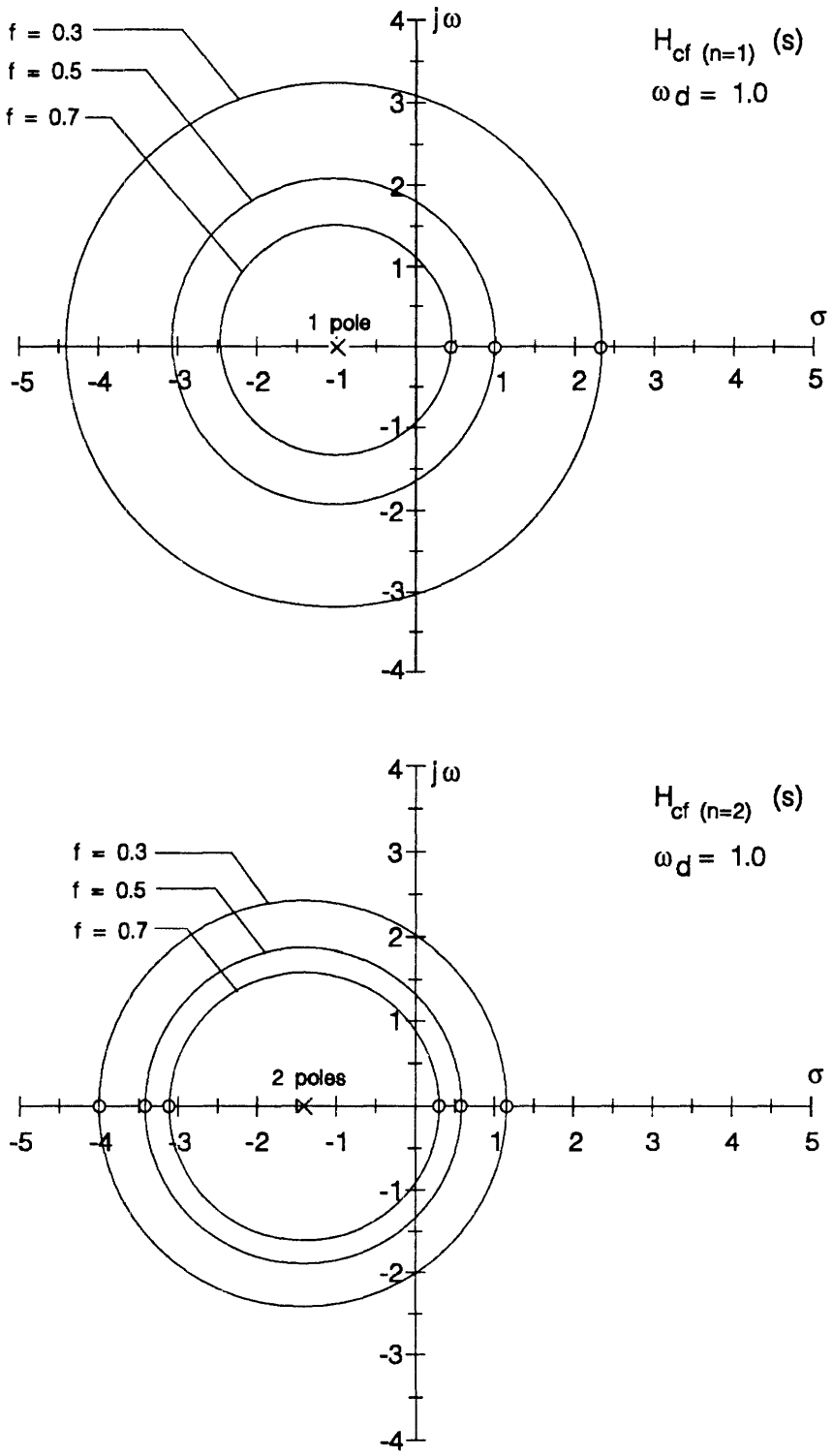


Figure 4-14. Pole-Zero Locations for Binkley Single-, Two-, Three-, and Four-Pole Gaussian CFDs.

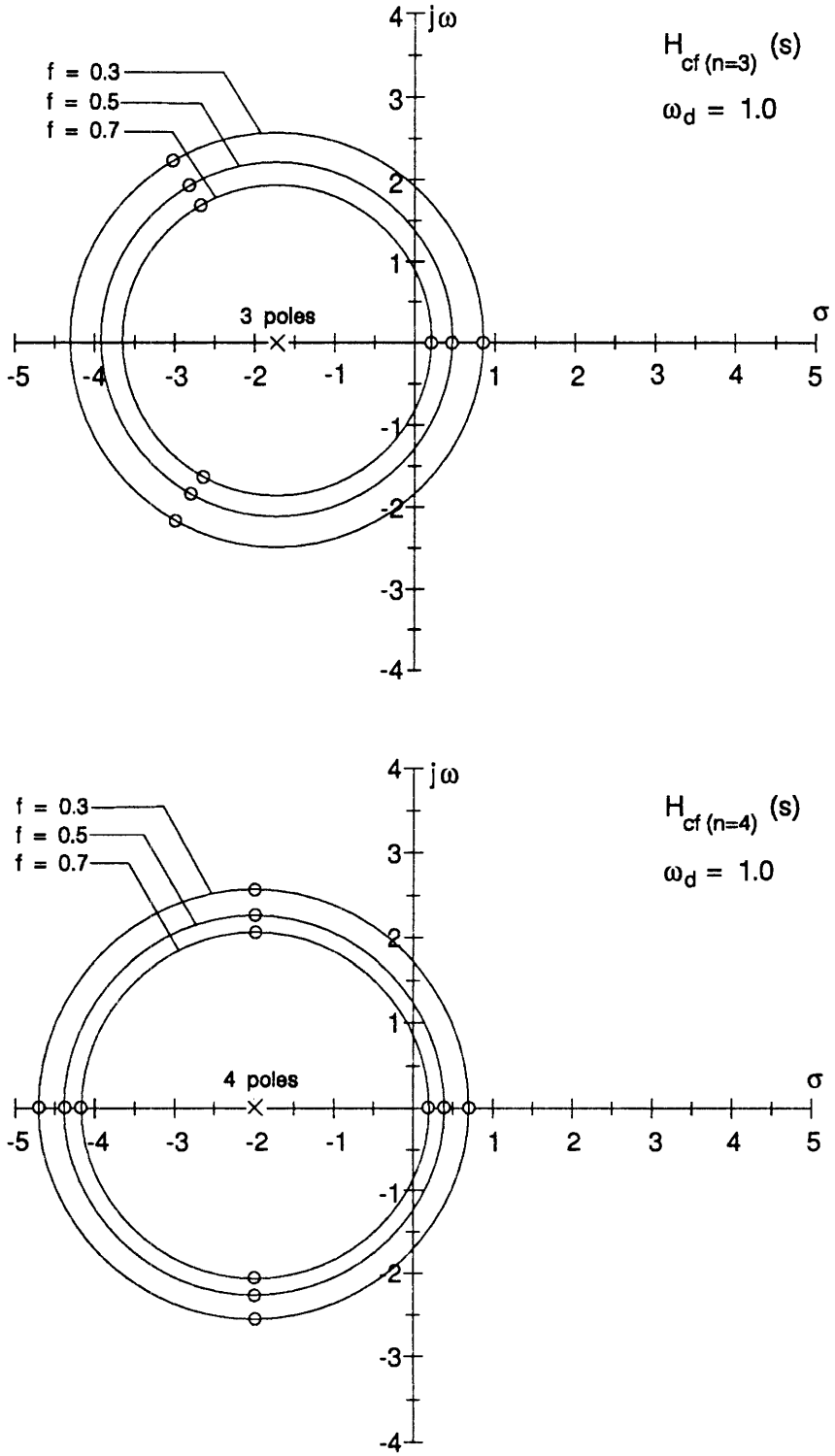


Figure 4-14. Continued.

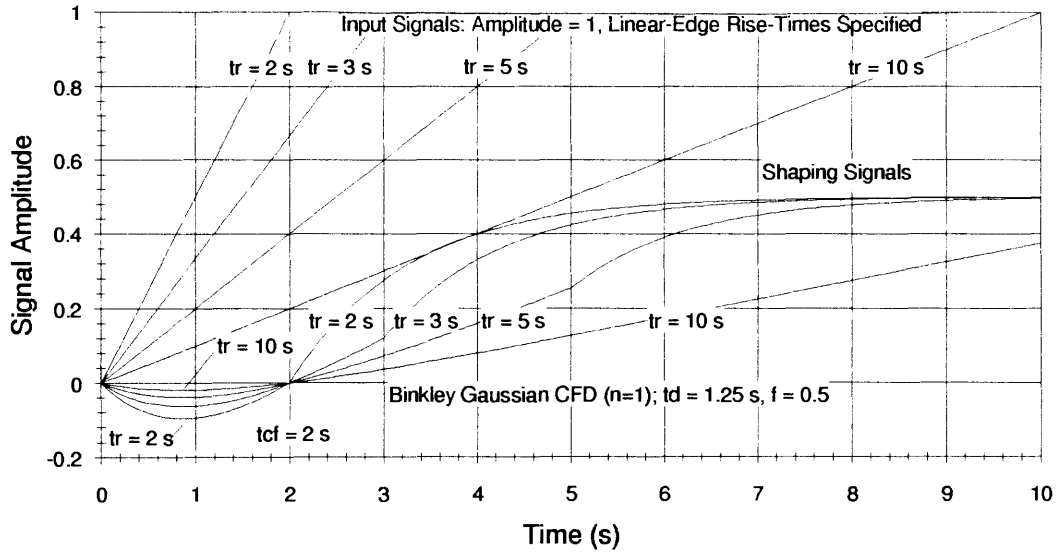


Figure 4-15. Illustration of Rise-Time Insensitivity for Binkley Single-Pole Gaussian CFD with Linear-Edge Signals.

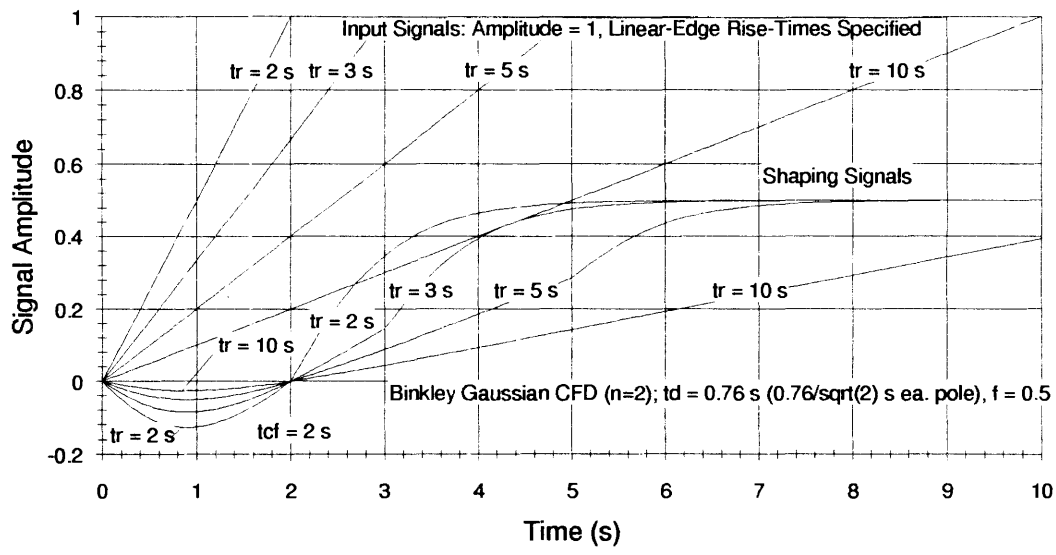


Figure 4-16. Illustration of Rise-Time Insensitivity for Binkley Two-Pole Gaussian CFD with Linear-Edge Signals.

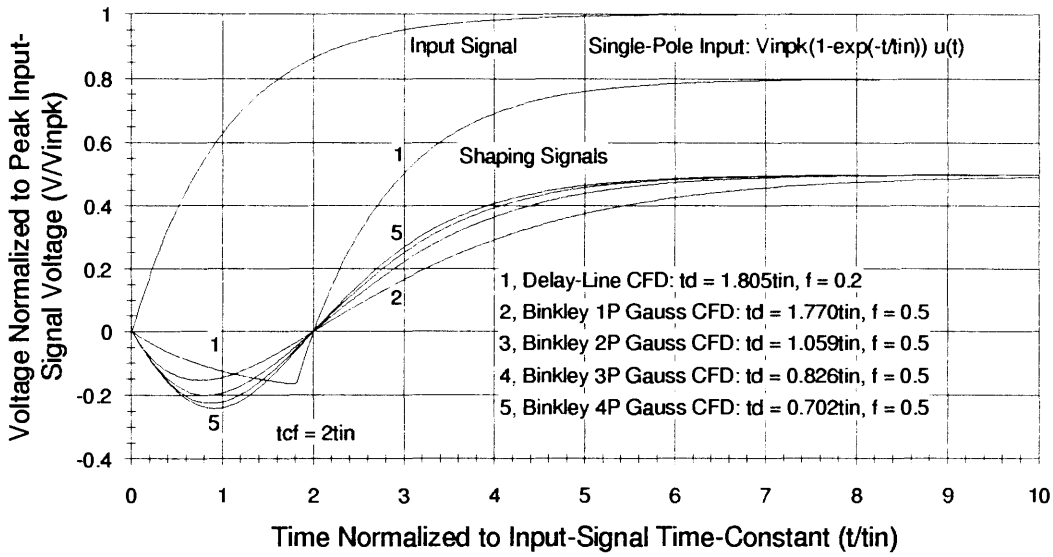


Figure 4-17. Shaping Signals for Delay-Line and Non-Delay-Line CFDs with Single-Pole Step Inputs (Zero-Crossing Time of $2t_{in}$).

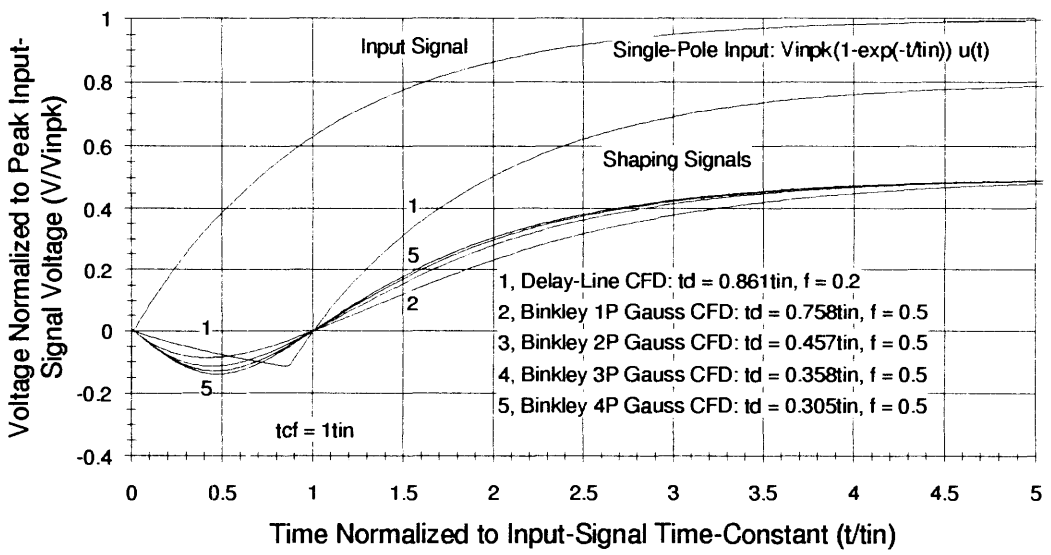


Figure 4-18. Shaping Signals for Delay-Line and Non-Delay-Line CFDs with Single-Pole Step Inputs (Zero-Crossing Time of $1t_{in}$).

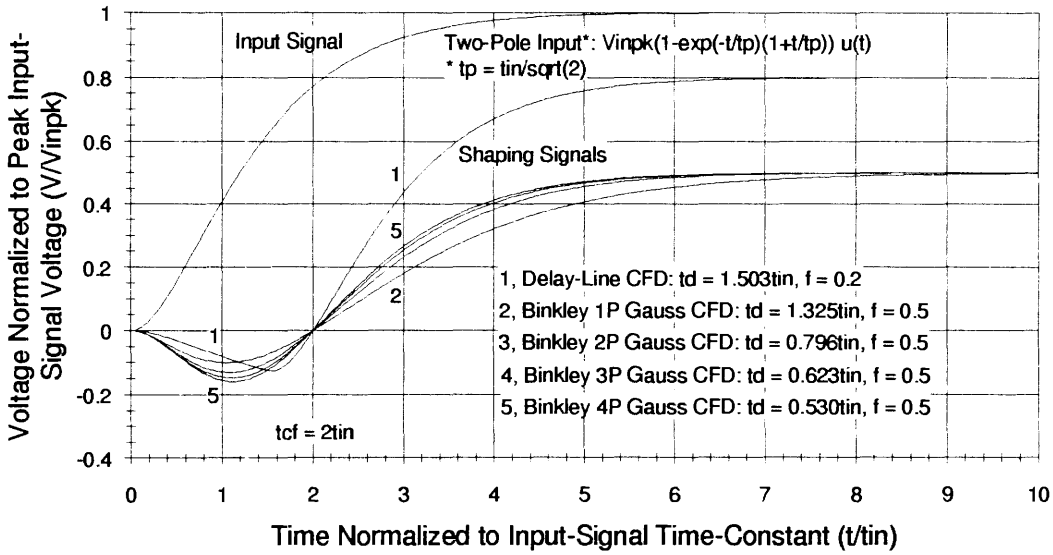


Figure 4-19. Shaping Signals for Delay-Line and Non-Delay-Line CFDs with Two-Pole Step Inputs (Zero-Crossing Time of $2t_{in}$).

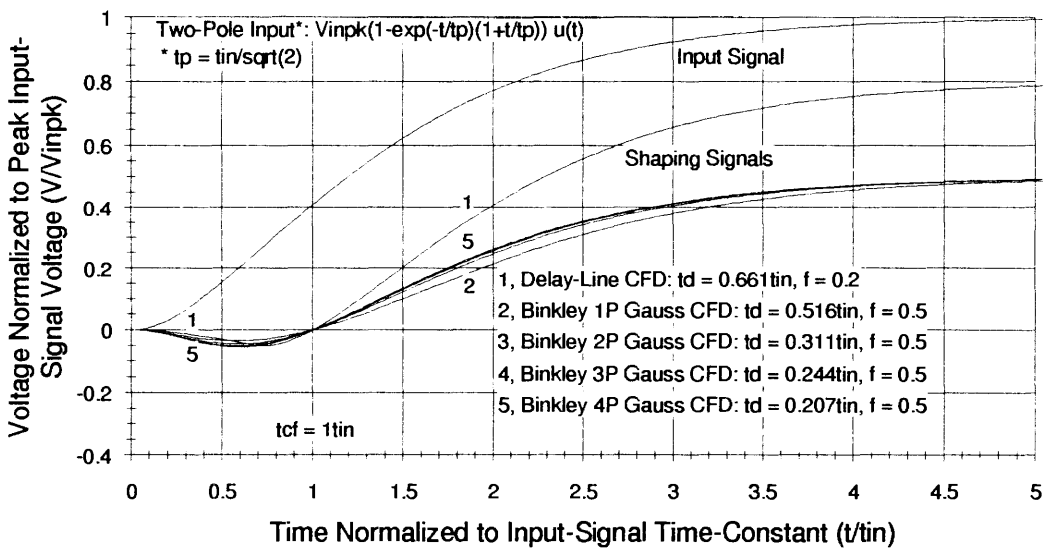
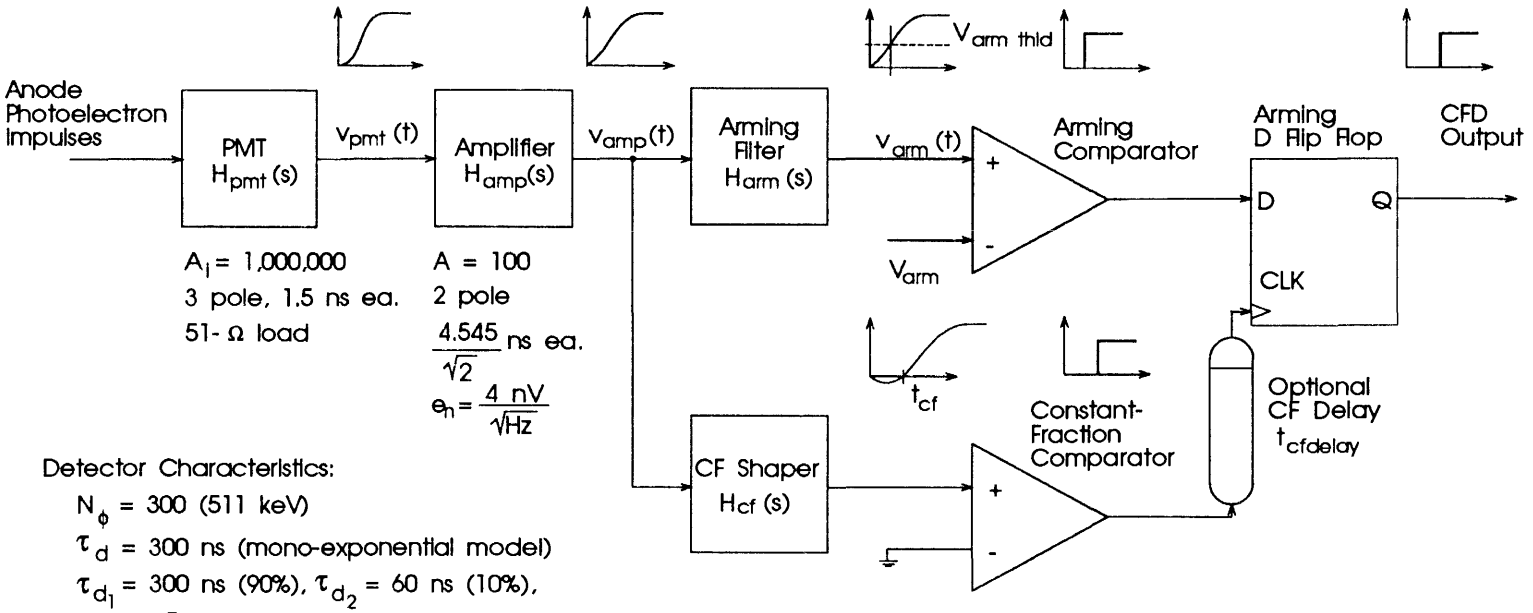


Figure 4-20. Shaping Signals for Delay-Line and Non-Delay-Line CFDs with Two-Pole Step Inputs (Zero-Crossing Time of $1t_{in}$).



Detector Characteristics:

N_ϕ = 300 (511 keV)

τ_d = 300 ns (mono-exponential model)

τ_{d_1} = 300 ns (90%), τ_{d_2} = 60 ns (10%),

τ_r = 1.5 ns (tri-exponential model)

Energy Resolution = 14% FWHM

Photomultiplier Characteristics:

Single-Electron Gain = 1,000,000

SER = 163% FWHM

Transit Time = 5 ns (actually 22 ns)

Transit Time Spread = 0.7 ns FWHM

Compton Scatter Characteristics:

Scatter Fraction = 0.0 (point source); 0.32 (20-cm diameter water-filled cylinder)

Scatter Knee = 450 keV

Photo Fraction = 0.54

Figure 4-21. Circuit Model for CFD Monte Carlo Analysis.

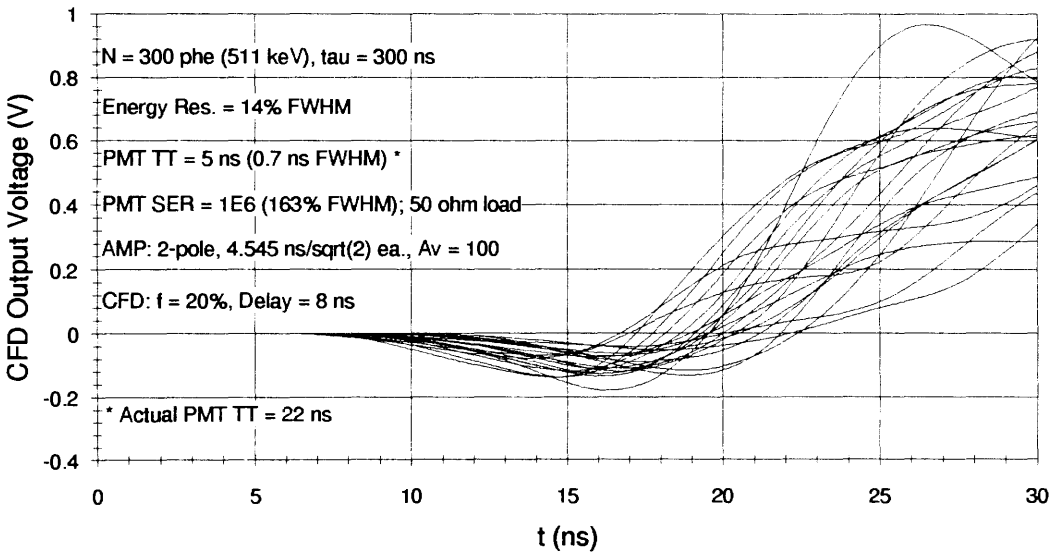


Figure 4-22. Monte Carlo Simulated CFD Output Signals for BGO/Photomultiplier Scintillation Detector and CFD Timing System.

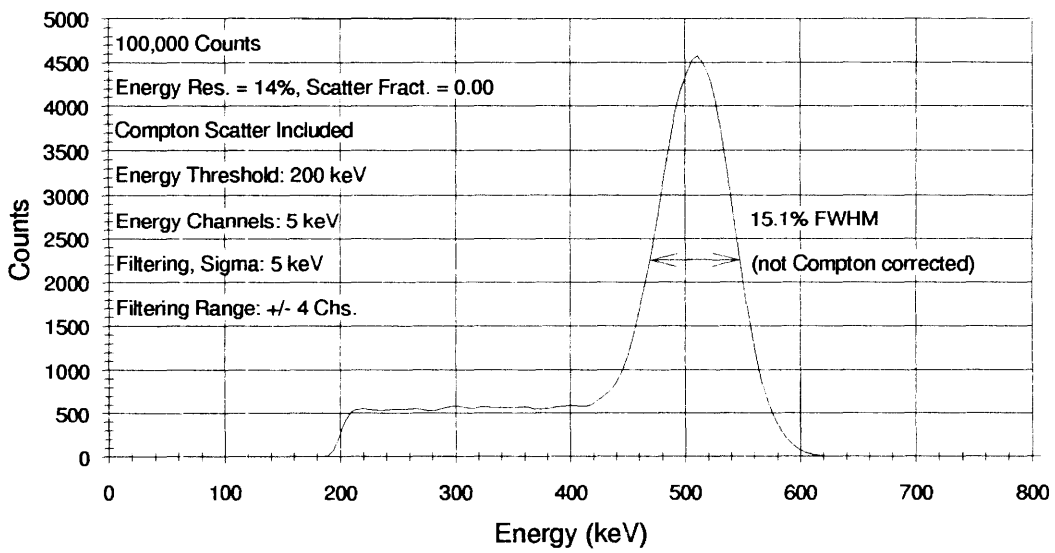


Figure 4-23. Energy Spectrum Used for Monte Carlo Simulation of CFD Timing Resolution.

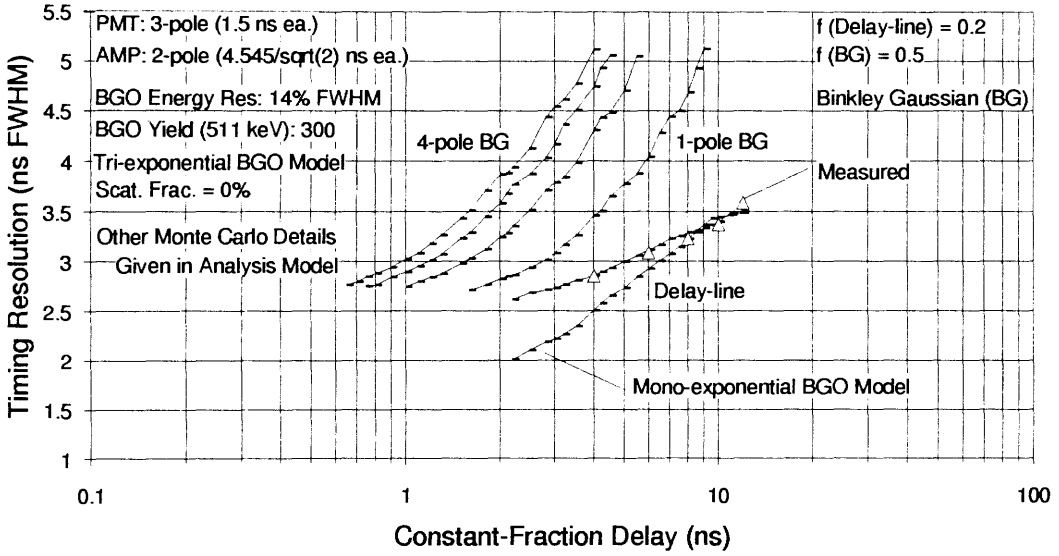


Figure 4-24. Monte Carlo Timing Resolution (FWHM) for Delay-Line and Non-Delay-Line CFDs with Measured Resolution for Delay-Line CFD.

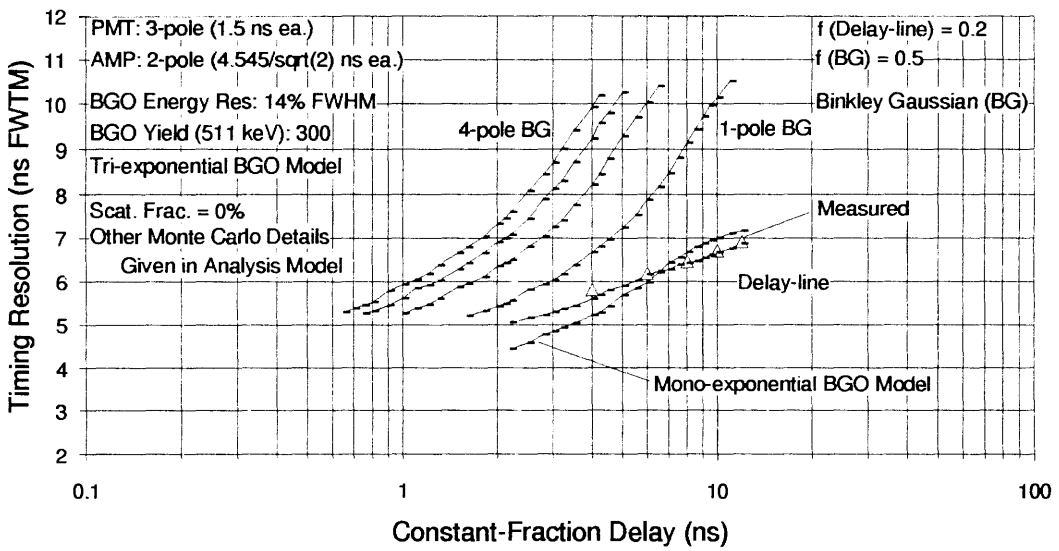


Figure 4-25. Monte Carlo Timing Resolution (FWTM) for Delay-Line and Non-Delay-Line CFDs with Measured Resolution for Delay-Line CFD.

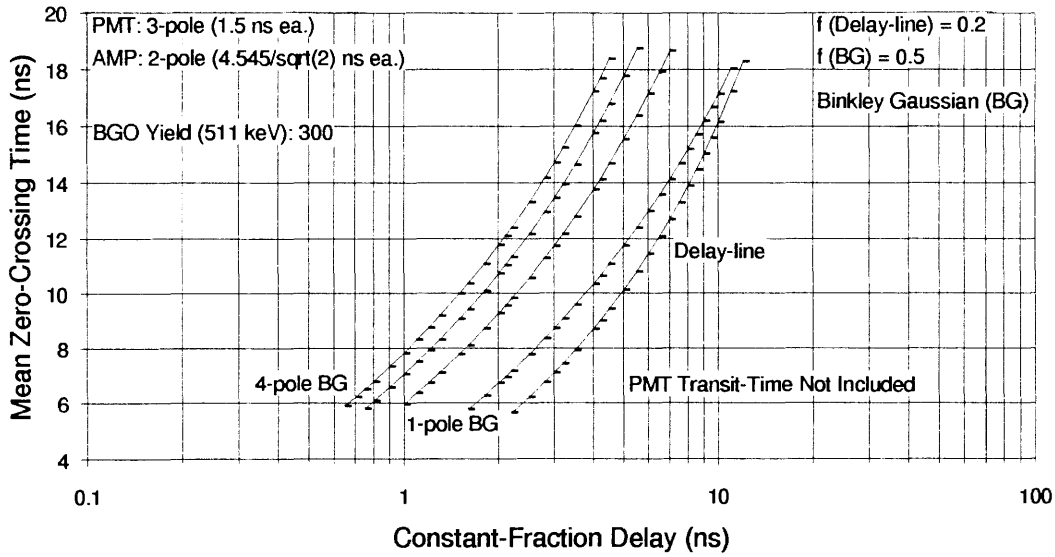


Figure 4-26. Mean Zero-Crossing Time for Delay-Line and Non-Delay-Line CFDs.

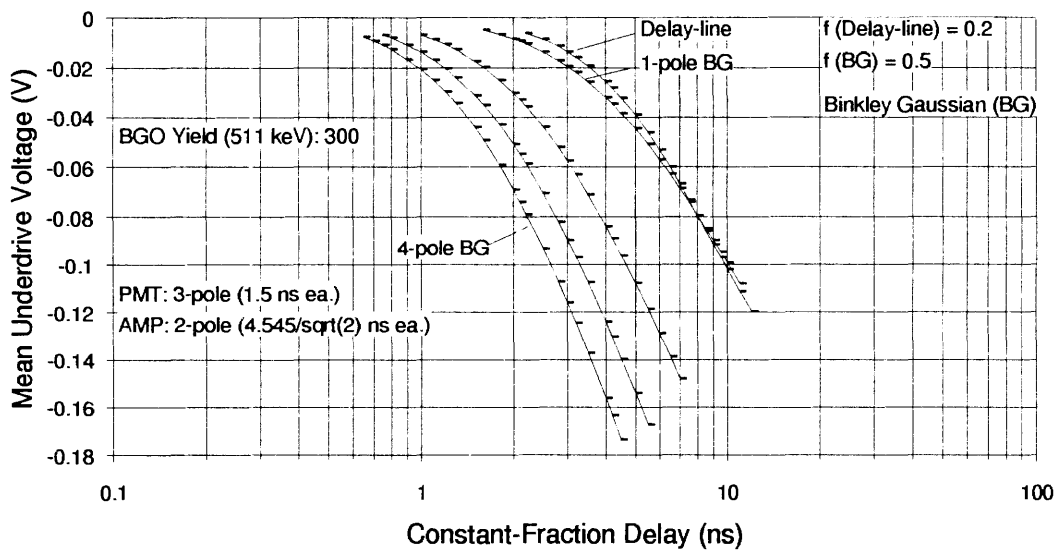


Figure 4-27. Mean Underdrive Voltage for Delay-Line and Non-Delay-Line CFDs.

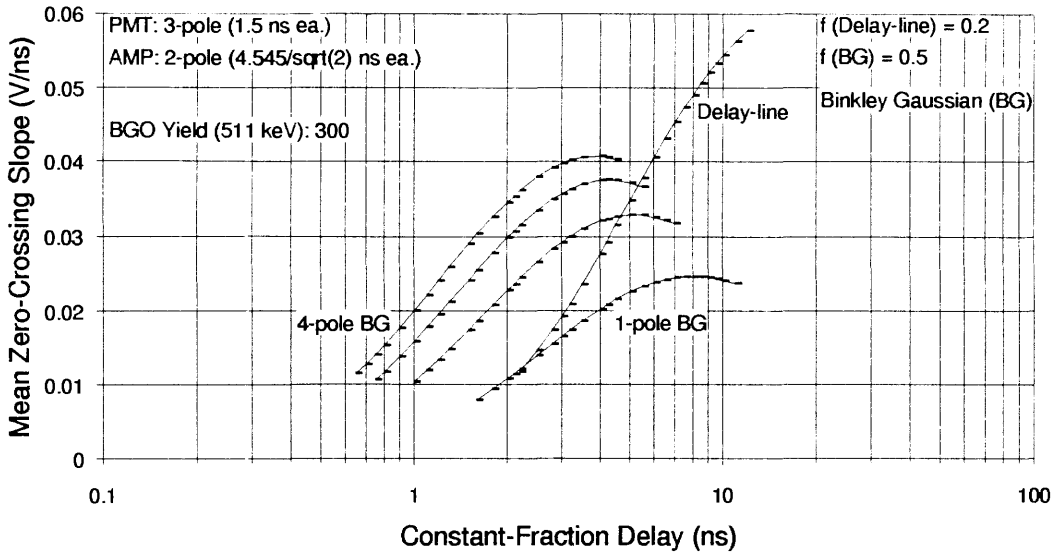


Figure 4-28. Mean Zero-Crossing Slope for Delay-Line and Non-Delay-Line CFDs.

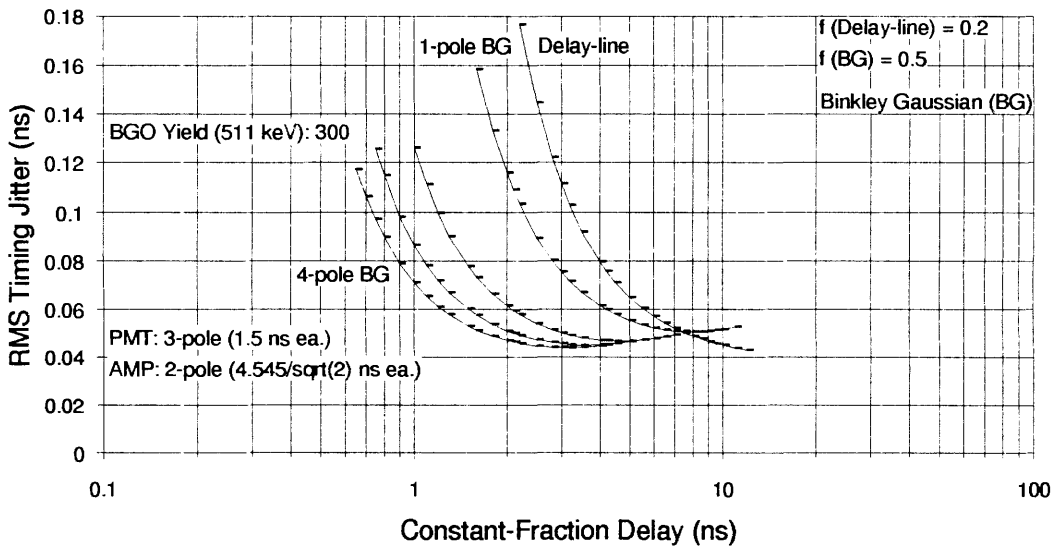


Figure 4-29. Timing Jitter for Delay-Line and Non-Delay-Line CFDs.

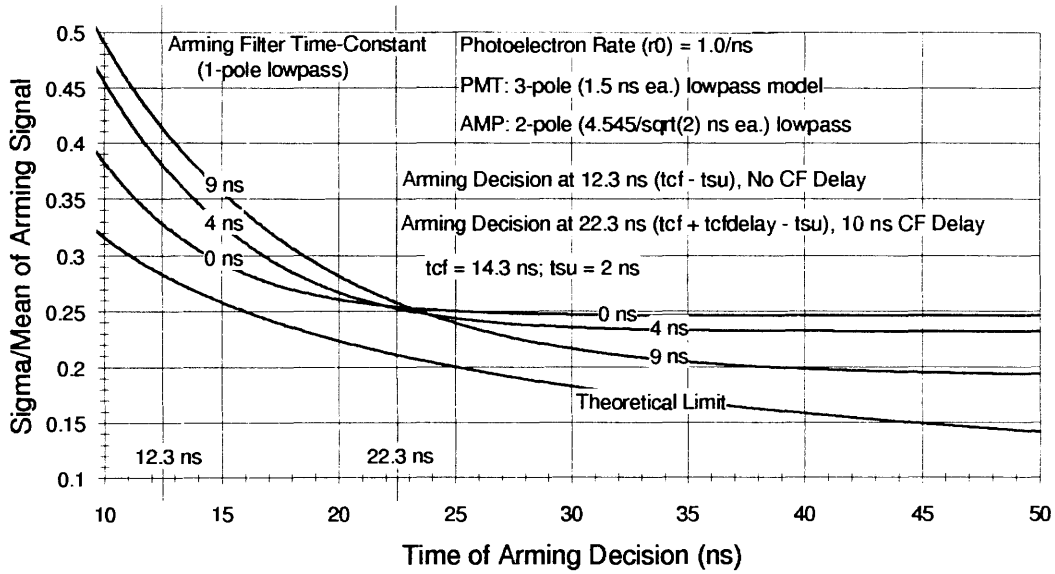


Figure 4-30. Ratio of Arming-Signal Standard Deviation to Arming-Signal Mean (CFD Energy Resolution).

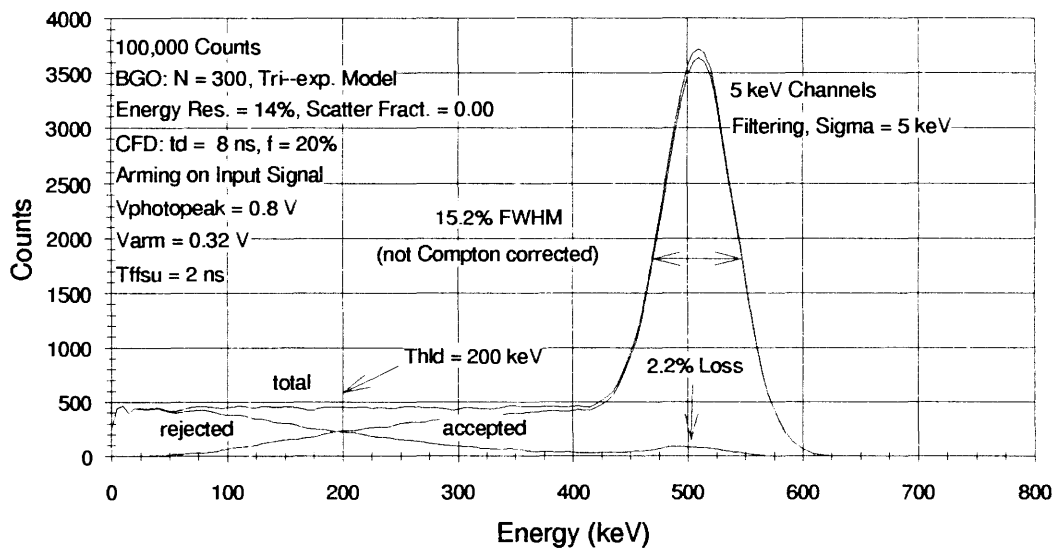


Figure 4-31. Monte Carlo Energy Spectrum for Commercial Delay-Line CFD.

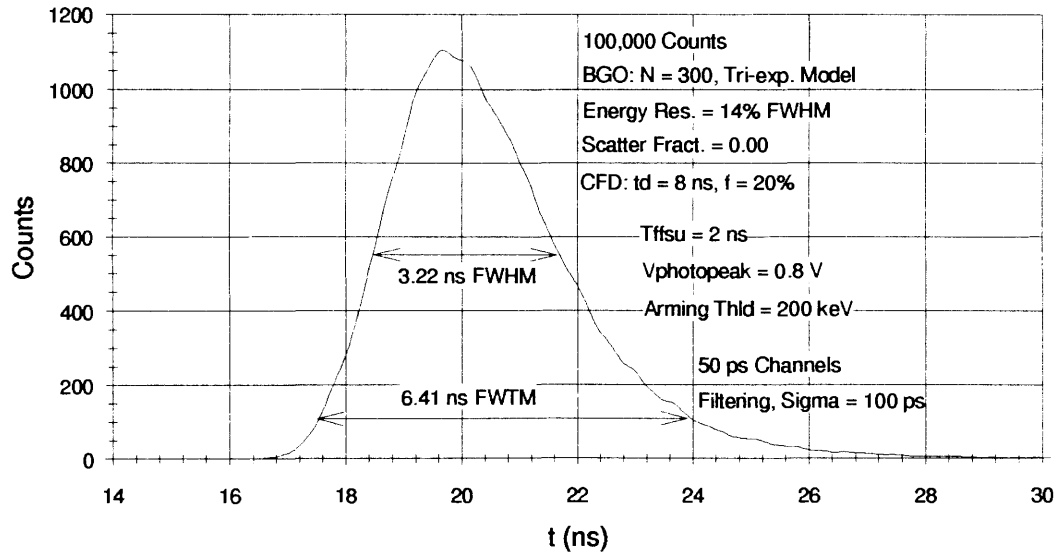


Figure 4-32. Monte Carlo Timing Spectrum for Commercial Delay-Line CFD.

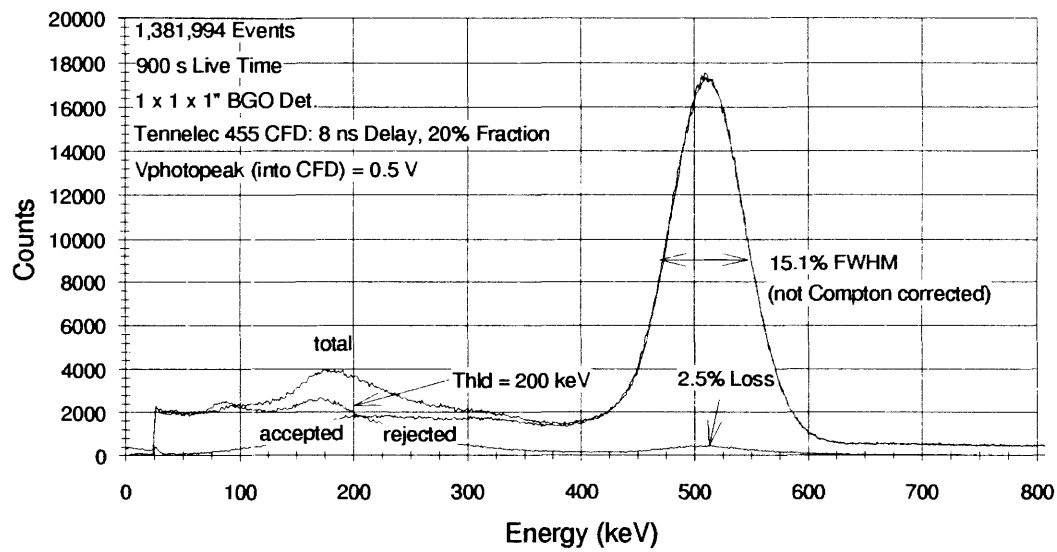


Figure 4-33. Measured Energy Spectrum for Commercial Delay-Line CFD.

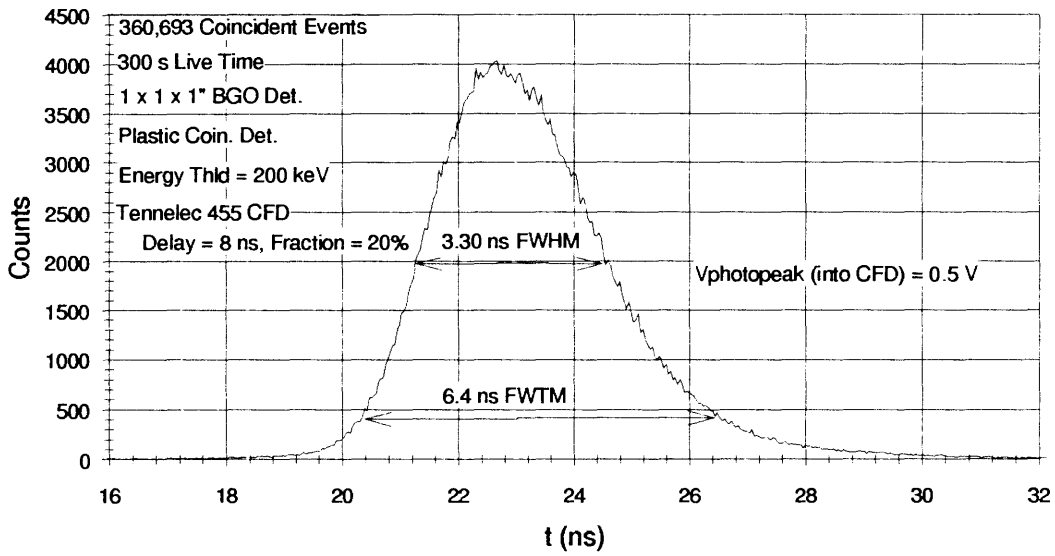


Figure 4-34. Measured Timing Spectrum for Commercial Delay-Line CFD.

5. CFD CIRCUITS, INCLUDING A FULLY-MONOLITHIC CMOS IMPLEMENTATION

Overview

In this section, previously reported CFD circuits are presented along with circuits developed for a fully-monolithic CMOS CFD. A historical review of major CFD circuit developments is presented including discussions of active and passive constant-fraction shaping circuits, constant-fraction comparator circuits, and arming circuits. In addition to CFD time pick-off circuits, other time pick-off circuits are reviewed. These circuits include leading-edge, conventional-crossover, trailing-edge, and differentiator-type discriminators.

Time-walk performance of comparator circuits is reviewed for high-speed, bipolar ECL comparators commonly used in CFD circuits and for recent high-speed bipolar, GaAs, and CMOS comparators. In addition, the performance of slow-rise-time reject (SRT) and traditional arming circuits is described, including a discussion of CFD timing errors resulting from these circuits. Finally, walk-adjustment circuits are described where constant-fraction comparator input offset is controlled to minimize CFD walk.

Design details are presented for a fully-monolithic CMOS CFD, believed to be the first reported monolithic CMOS CFD implementation. This circuit uses the Binkley non-delay-line CFD circuits described in *Section 4* to replace the delay-line typically used in CFD circuits. Process characteristics for the standard 2-μ, double-metal, double-poly, n-well, digital CMOS process used for the CMOS CFD are given along with an overview of each major circuit.

A wideband (bandwidth greater than 100 MHz), five-pole, five-zero, CMOS continuous-time filter is described which implements a Binkley, five-pole Gaussian, non-delay-line CFD shaping circuit. This fully differential circuit requires no common-mode feedback to set common-mode bias levels. SPICE simulations of pulse performance, dc linearity, ac response, noise, and time-walk distortion are presented.

Design optimization for low time-walk comparators, believed to be the first such reported analysis, is developed to permit selection of circuit topology and device sizes for the constant-fraction comparator used in the CMOS CFD. Performance tradeoffs associated with time walk due to limited small-signal gain-bandwidth and time walk due to large-signal circuit limiting are illustrated for a multistage, CMOS comparator design that is used as a basis for the constant-fraction comparator in the CMOS CFD. SPICE simulations of comparator response time, time-walk, ac response, and noise are presented for the constant-fraction comparator used in the CMOS CFD.

Monte Carlo simulations of energy and timing spectra are presented for the CMOS CFD. These simulations are especially useful since experimental verification of CFD performance is not possible prior to integrated-circuit fabrication. Additionally, an evaluation of CMOS CFD time walk and time jitter is presented, and these errors are shown to be negligible for the BGO/photomultiplier application considered. Finally, measured energy and timing spectra are presented for the fabricated CMOS CFD. The measured CMOS CFD timing resolution (3.25 ns FWHM, 6.50 ns FWTM) is comparable to simulated CMOS CFD timing resolution (3.45 ns FWHM, 6.71 ns FWTM) and measured timing resolution (3.30 ns FWHM, 6.40 ns FWTM, given in *Section 4*) for a commercial, delay-line CFD.

Review of CFD Circuits

A CFD circuit (Figure 1-4, page 15) contains shaping circuitry for creating bipolar timing pulses, a constant-fraction comparator to sense the zero-crossing of these bipolar timing pulses, an arming comparator to detect signals above a preset threshold, and arming logic to qualify the CFD timing output for those input signals above the threshold.

There are three CFD arming circuits in wide use and these are shown in Figure 5-1 [1, 2]. The traditional arming circuit in Figure 5-1 consists of a simple AND gate which provides an output if both the arming and constant-fraction signals are present. The AND gate is followed by a one-shot circuit which holds the output active for a duration of time equal to the blocking time. This prevents retriggering of the circuit on photoelectron emissions from the detected event.

In addition to the traditional arming circuit in Figure 5-1, two slow-rise-time (SRT) reject arming circuits are shown. Both of these circuits use a D flip flop to provide a timing output (which is related in time to the constant-fraction signal) only if the arming signal *precedes* the constant-fraction signal. These circuits are designed to prevent false (leading-edge) triggering that occurs in the traditional arming circuit when the constant-fraction signal precedes the arming signal. This condition occurs if the input-signal rise-time is not sufficiently fast or if the input-signal does not sufficiently cross the arming threshold. One slow-rise-time reject circuit shown in Figure 5-1 uses traditional arming with an AND gate to qualify the clock input of the D flip flop. The other slow-rise-time reject circuit shown does not utilize this gate.

Reported CFD Circuits

The first CFD circuits were reported by Gedcke and Mc Donald in 1967 and 1968 [3, 4]. These circuits, used for scintillation-detector timing, relied on passive signal summing to

produce a single-ended bipolar timing signal that was routed to a tunnel-diode detector for zero-crossing discrimination. The shaping circuit consisted of a delay line and wideband transformer for delaying and inverting the input signal and a resistor summing network to combine the delayed and attenuated input signal. The arming circuit used was effectively the traditional arming circuit, although no AND gate was used. Instead, the constant-fraction (zero-crossing) tunnel diode discrimination circuit was *primed* by a second arming tunnel-diode discrimination circuit. Although these were the first CFD circuits reported, the walk of the Gedcke and Mc Donald circuits was reported at ±120 ps for a 100:1 input-signal range of 1.2 mA to 120 mA [3, 4]. The input signal was provided directly from an RCA (now Burle) 8575 photomultiplier tube with a rise-time in the 2 - 4 ns range [5]. These early circuits had good timing performance because of the high-performance tunnel-diode discriminators (comparators).

Another CFD circuit utilizing tunnel diodes was reported in 1968 by Chase [6]. In this circuit, designed for timing with Ge(Li) detectors, amplitude-rise-time-compensated (ARC) timing was used where CFD constant-fraction delay is made short relative to the input-signal rise-time. As discussed earlier, ARC CFD operation minimizes time walk due to varying input-signal rise-time from semiconductor detectors. In 1972, another tunnel-diode CFD was reported by Cho and Chase for timing with Ge(Li) detectors [7]. This circuit used a "dual priming" technique where one ARC-configured CFD (containing a regular arming comparator) was used to arm a second ARC-configured CFD for the timing output. This circuit extended the low-energy range of Ge(Li)-detector timing operation from the previous limit of 200 keV to approximately 20 keV.

The first CFD circuit using integrated circuits was reported by Maier and Sperr in 1970 [8]. In this circuit, used for scintillation-detector timing, ECL logic circuits were used from the Motorola MECL II family [9]. Active summing, now widely used, was utilized in the circuit where the delayed and attenuated signal are actively summed (actually subtracted) at the differential input of the constant-fraction comparator. Both the constant-fraction comparator and arming comparator were constructed from three cascaded ECL line receivers. The arming circuit used was the traditional arming circuit which was implemented with an ECL AND gate. The walk performance of the Maier and Sperr circuit was reported at less than 250 ps for an input-amplitude range of 50:1 (-50 mV to -500 mV) with an input rise-time of 2 ns [8, 10]. A circuit similar to the Maier and Sperr circuit, also used for scintillation-detector timing, was reported in 1974 by Hall [11]. In this circuit, timing performance was improved through the use of iterative adjustment schemes

involving the trimming of DC comparator offsets and the trimming of the constant-fraction delay.

In 1974, Maier and Landis [10] reported a second version of the Maier and Sperr [8] CFD circuit. In this circuit, the AMD 685 ECL comparator was used [12] and ECL logic circuits were used from the Motorola MECL 10 K logic family [9]. The arming circuit used in the second version circuit consisted of either the traditional AND-gate logic or a specially-designed slow-rise-time reject circuit useful for Ge(Li) timing. The slow-rise-time reject circuitry contained a set-reset flip-flop circuit to ensure that arming only occurred if the arming signal preceded the constant-fraction signal. This slow-rise-time reject circuitry was first reported by Gabriel et al. in 1972 [13]. The walk performance of the Maier and Landis circuit was reported to be superior to the earlier Maier and Sperr circuit for signals lower in amplitude than -100 mV. The reported walk for the Maier and Landis circuit was 1 ns for an input-amplitude range of 1000:1 (-5 mV to -5 V) with an input rise-time of 2 ns.

In 1981, Wozniak et al. [14] reported on a modification to the Maier and Landis [10] CFD circuit. In the modified circuit, the AMD AM685 ECL constant-fraction and arming comparators were replaced with the Plessey SP9685 [15] high-speed ECL comparators. The reported walk for the modified circuit was 30 ps compared to 500 ps for the unmodified circuit for an amplitude range of 25:1 (0.1 V to 2.5 V) with an input rise-time of 1 ns. Additionally, the walk for the modified circuit was reported at 100 ps for an amplitude range of 50:1 (50 mV - 2.5 V) with the same input rise-time of 1 ns.

In 1983, Maier reported a CFD constructed with only two integrated circuits [16]. One of these circuits was the Plessey SP9687 dual version of the SP9685 high-speed ECL comparator [15], and the second was a Motorola MECL 10K [9] ECL flip-flop configured as a one shot. Traditional arming was used; however, no AND gate was directly used. Instead, the inverting outputs of the high-speed ECL arming and constant-fraction comparators were connected together creating negative wired-OR logic that implemented the required AND function. The reported walk performance of this circuit, used for scintillation-detector timing, was comparable to that of the earlier Wozniak circuit.

Widely used, modern, commercial CFDs, including the Tennelec 455 [17] and the ORTEC 583 [18] NIM-module CFDs, utilize the Plessey SP9685 family of high-speed ECL comparators (or alternate sources) for constant-fraction and arming comparators. Additionally, ECL logic from the Motorola MECL 10K, 10KH, or MECLIII families [9] is used for arming logic in these circuits. Most of the commercial circuits, including those previously mentioned, have arming circuits that can be configured for either traditional

arming or slow-rise-time reject arming. The slow-rise-time reject logic consists of a D flip-flop with AND logic preceding its clock input (Figure 5-1) and is especially useful for semiconductor-detector timing applications where the input rise-time varies widely. Additionally, the commercial circuits can be configured for amplitude-rise-time-compensated (ARC) operation (through the choice of external constant-fraction delay) for use with semiconductor detectors. The commercial CFD circuits have walk performance in the ±30 ps (60 ps) to ±120 ps (240 ps) range for an input-amplitude range of 100:1 (25 mV to 2.5 V) with an input-signal rise-time of 1 ns.

The CFDs used in Siemens/CTI 931, 951, ECAT EXACT (921), and ECAT EXACT HR (961) series of commercial PET tomographs [19] utilize a dual high-speed ECL comparator from the Plessey 9685 [15] family and MECL 10KH ECL [9] arming logic. The arming circuits are configured as slow-rise-time reject circuits using a D flip-flop with logic similar to AND logic preceding the clock input (Figure 5-1). The CFDs used in the Siemens/CTI 711 time-of-flight PET tomograph use the same comparator circuits but use a slow-rise-time (SRT) reject arming circuit consisting of a D flip-flop without logic preceding the clock input (Figure 5-1) [19]. Although the slow-rise-time reject arming configurations (Figure 5-1) are intended mainly for semiconductor-detector (e.g., Ge(Li)-detector) applications where slow-rise-time inputs can occur, slow-rise-time reject arming has been found experimentally to give better operation over traditional arming for PET BGO/photomultiplier scintillation-detector systems [20].

CFD circuits using comparators faster than the Plessey 9685 family of high-speed ECL comparators have been reported. Circuits using the VTC VC7695 high-speed ECL comparator [21] have been reported by Binkley and Casey [22] and by Turko [23]. The measured walk for the CFD (using the VC7695 comparator) reported by Binkley and Casey is 40 ps for an input dynamic range of 100:1 (25 mV - 2.5 V) with an input rise-time of 1.3 ns. The measured walk for the circuit reported by Turko (using the VC7695 comparator) is 100 ps for an input dynamic range of 100:1 (25 mV - 2.5 V) for narrow pulses having a pulse width of 1.5 - 15 ns FWHM. The measured walk for this circuit was also reported by Turko for the Honeywell HCMP96850 [24] and Analog Devices AD96687 [25] high-speed ECL comparators, with a reported value of approximately 200 ps. The circuit reported by Turko is not a delay-line CFD; instead, it is a differentiation circuit formed by differencing a single-pole-lowpassed version of the input signal from the input signal. This circuit will be described later. Finally, circuits using GaAs comparators have been reported by Bialkowski

et al. [2]. The reported walk for this circuit is 40 ps for an input dynamic range of 100:1 (20 mV - 2 V) with an input rise-time of 1 ns.

Although most commercial CFDs use one of the arming circuits shown in Figure 5-1, more elaborate arming circuits have been reported. These circuits are designed to permit more reliable arming for signals with widely varying rise-times from Ge(Li) detectors. These circuits attempt to minimize leading-edge timing errors caused by improper CFD arming while minimizing the rejection of good events. One such circuit, reported by White and Mc Donald [26, 27], and Robertson [28], consists of three paralleled CFDs operating at fractions of 10%, 30%, and 50%. The timing marks from each of these circuits are compared in time to determine if the input-signal rise-time is within acceptable limits. Another arming circuit reported by Bedwell and Paulus uses two arming comparators with initial arming derived from an arming comparator having a threshold of one-half that of a final arming comparator [29, 30, 31]. Since the final arming comparator ultimately qualifies events, signals from accepted events are guaranteed to exceed the initial arming threshold by a factor of at least two. This eliminates the leading-edge timing errors associated with signals that barely cross the arming threshold.

All of the CFD circuits described so far have been fabricated from discrete electronic devices or integrated circuits combined with discrete devices. A hybrid CFD (requiring an external delay line) was reported by Bedwell and Paulus in 1978 [32] and this circuit was used in the CTI/Siemens 911 series of PET tomographs [19]. Passive summing was used in this hybrid circuit, consisting of a wideband transformer for signal inversion of the delayed signal and a passive summing network for the attenuated signal. Although circuit details were not described for this hybrid circuit [32], high-speed ECL voltage comparators and ECL logic circuits were probably used.

Binkley et al. reported a monolithic CMOS CFD requiring an external delay-line and attenuation network in 1991 (actually first reported at the 1989 IEEE Nuclear Science Symposium held in January of 1990) [33]. This circuit, fabricated in a standard 2-μ CMOS process, has measured walk of 1.4 ns for a 10:1 input-amplitude range (-200 mV to -2000 mV input voltage) with an input-signal rise-time of 20 ns. The walk performance, which was shown to be adequate for PET BGO timing, is dominated by the walk associated with the single-stage CMOS comparator. The walk performance of the monolithic CMOS CFD reported later in this section is considerably improved from the first CMOS circuit. Most recently, Tanaka et al. reported a monolithic bipolar CFD which does not require an external delay line (first reported at the IEEE Nuclear Science Symposium in November of

1991) [34]. In this circuit, the Nowlin CFD circuit consisting of a single-pole highpass filter is used. The reported measured walk for this circuit is 1 ns for a 31.6:1 input-amplitude range (10 - 316 mV input voltage) and an input-signal rise-time of 10 ns which is considerably above the reported SPICE-simulated value of 100 ps. The power consumption of this circuit is 190 mW (the power dissipation was given in the submitted paper summary only). The monolithic CMOS CFD reported later in this section uses the Binkley CFD circuit and is believed to be the first fully-integrated CMOS monolithic (no external delay line or attenuation network) CFD. The power dissipation of the CMOS CFD circuit, expected to be approximately 70 mW in the final design, is considerably below the approximate 190-mW power dissipation of the Tanaka CFD circuit.

Other Reported Time Pick-Off Circuits

Delay-line CFDs contain both a delayed and attenuated signal path. In the non-delay-line CFD circuits previously described, the delayed path of the delay-line CFD is replaced with highpass networks (Nowlin CFD) or allpass/lowpass networks (Binkley CFD). In addition to the delay-line and non-delay-line CFDs discussed, other timing circuits have been reported.

The simplest time pick-off circuit is the leading-edge discriminator discussed earlier in *Section 2*. This circuit produces amplitude and rise-time walk for any nonzero threshold voltage, but can offer adequate timing performance for input-signals having a narrow amplitude range or having sufficiently fast rise-times (much less than the desired timing resolution).

Fast-crossover timing provides amplitude-insensitive timing for scintillation-photomultiplier detectors [35]. In this time pick-off circuit, the anode of the photomultiplier tube is connected to a zero-crossing discriminator and to a shorted stub of transmission line. A bipolar shaping signal results at the photomultiplier output due to the presence of the shorted transmission line. The zero-crossing time of this bipolar signal is independent of signal amplitude as is true for bipolar signals from all linear shaping circuits.

Fast-crossover timing has the advantage of circuit simplicity compared to the delay-line CFD as it requires a single transmission line or delay line and no attenuation network [35]. Additionally, circuit arming is simplified because the zero-crossing time occurs after the rise-time of the input signal. However, fast-crossover timing has the disadvantage of higher timing jitter compared to the delay-line CFD because of increased shaping-signal noise and decreased shaping-signal slope. Additionally, fast-crossover timing is sensitive to input-

signal rise-time and shape. Fast-crossover timing retains the complexity associated with a delay line, making a complete monolithic implementation impractical.

In 1969, Kinbara and Kumahara reported a timing shaping circuit where a differentiated version of the input signal is compared with a delayed version [36]. Later, Hartmann and Klein made a theoretical analysis of the Kinbara and Kumahara circuit and concluded that better performance is available by comparing a delayed, differentiated version of the input signal with the input signal [37]. Both timing shaping circuits retain the complexity of a delay line and are not in general use.

Conventional-crossover timing provides amplitude-insensitive timing from the bipolar shaping signals available at the output of bipolar shaping amplifiers [35]. Either double-delay-line or CR-RC-shaping circuits can be used for the shaping. Since most shaping amplifiers are optimized for energy performance and significant integration or lowpass filtering is usually present, the shaping-signal rise-time is significantly reduced resulting in significantly increased timing jitter compared to the delay-line CFD. Conventional-crossover timing, however, is useful for timing where optimum timing resolution is not required.

Timing can also be derived from the output of energy shaping amplifiers through the use of a trailing-edge CFD [35]. In this circuit, the unipolar or bipolar output from a shaping amplifier is passed directly into one side of a timing comparator while a pulse-stretched and attenuated version is passed into the other side. The timing point is derived on the *falling* edge of the input signal (the signal from the shaping amplifier) when the input is equal to a selected fraction of the peak input signal. The pulse stretcher is used to obtain the peak input signal, and the attenuation network is used to select the fraction. Like conventional-crossover timing, the trailing-edge CFD is useful for timing off pulses shaped for energy measurements. However, like conventional crossover timing, time derivation is dependent upon the input-signal rise-time and shape, and timing jitter performance is not optimized because of operation with low-bandwidth pulses optimized for energy measurements. Although conventional-crossover and trailing-edge-CFD circuits do not require a delay-line (if CR-RC-shaping circuits are used in the preceding energy-shaping amplifier circuits), these circuits are not optimized for minimum timing jitter compared to the wider bandwidth Nowlin and Binkley non-delay-line CFD circuits.

Recently, Turko reported a non-delay-line timing circuit for use with pulses having narrow pulse widths [23]. In this circuit, the input is connected directly to one timing-comparator input and a single-pole-lowpassed version of the input is connected to the other

timing-comparator input. The resulting circuit response is that of a single-pole highpass filter which acts as an approximate differentiator. The zero crossing of the output signal from this approximate differentiator occurs near the peak of the input signal where the signal slope is zero. Reported walk performance for this circuit (using the VTC VC7695 high-speed ECL voltage comparator [21]) is 100 ps for pulses with a pulse width of 1.5 - 15 ns FWHM having an 100:1 input-amplitude range (25 mV - 2.5 V). Although the circuit is actually equivalent to the Binkley single-pole Gaussian CFD with a fraction of 100% (a disallowed fraction value for the Binkley Gaussian circuit), its principle of operation is considerably different. The Turko circuit is a differentiation circuit sensing the peak of a narrow input pulse whereas the Binkley Gaussian CFD is sensing the leading-edge of the input signal independent of the pulse width.

Operation of CFD Circuits

Operation of CFD Arming and Constant-Fraction Comparators

As described by Binkley and Casey [22], a CFD provides walk-free timing (excluding any walk errors in the arming-logic circuitry) for a linear shaping network and an ideal, walk-free constant-fraction comparator. Walk errors for practical CFD circuits, however, are usually dominated by walk in the constant-fraction comparator.

Comparator walk performance in CFD applications can be inferred from the reported walk performance of CFD circuits previously discussed [2, 3, 4, 8, 10, 14, 16, 17, 18, 23, 33]. Measured walk performance for comparators not configured in CFD applications has recently been reported by Turko [38] following the paper by Binkley and Casey [22] in which detailed SPICE-simulated comparator walk data was reported. Turko measured comparator walk using a variable threshold voltage to provide triggering with different levels of input overdrive [38]. The resulting comparator input-signal underdrive changed with overdrive, decreasing as overdrive increased. The measured walk for high-speed bipolar ECL voltage comparators was approximately 210 ps (AD9685 [39]), 250 ps (VC 7695 [21]), 880 ps (HCMP 96870 [24]), and 1030 ps (AM685 [12]). The measured walk for high-speed GaAs ECL voltage comparators was approximately 220 ps (10G012B [40]), and 805 ps (TQ6330 [41]). These walk measurements are for overdrives between 10 mV and 1 V (100:1 dynamic range) for a 1-V input signal having a rise-time of 140 ps. The SPICE-simulated comparator-walk data reported by Binkley and Casey [22] was 185 ps for the VC7695 high-speed ECL voltage comparator with step inputs having symmetrical overdrive and underdrive between 10 mV and 1 V (100:1 dynamic range). Although the input-signal underdrive and rise-time

conditions are somewhat different, the simulated walk (185 ps) is near the walk (250 ps) measured by Turko.

Recently, several new high-speed, ECL voltage comparators have been introduced which should be considered for high-performance discrete timing circuits. The MAX9685 (MAX9687 is the dual version) [42] is an improved version of the widely-used AD9685 [39], SP9685 [15], and AM6685 [43] family of high-speed, ECL voltage comparators. The propagation delay for the improved comparator is nearly a factor of two faster at 1.3 ns typical, 1.8 ns maximum for a 100-mV step input having a 10-mV overdrive. The AD96685 (AD96687 is the dual version) [25] high-speed, ECL voltage comparator is another improved version of the widely-used AD9685, SP9685, and AM6685 family of comparators. The propagation delay for this improved comparator is essentially the same at 2.5 ns typical, 3.5 ns maximum for the same 100-mV step input having a 10-mV overdrive. However, the walk for the improved comparator is specified at 50 ps typical for a step input with input overdrives ranging from 100 mV to 1 V.

The fastest, high-speed, ECL voltage comparator recently introduced is the SPT9689A [24], which is a dual comparator. The specified propagation delay is 650 ps typical, 850 ps maximum for a step input having an overdrive of 20 mV, and the specified walk is typically less than 100 ps for overdrives between 5 mV and 50 mV. Although this bipolar circuit (all of the high-speed, ECL comparators mentioned are bipolar) has considerably improved propagation delay over other high-speed, ECL comparators, it still has a comparable DC gain of approximately 2,000.

Binkley et al. reported the walk performance of a single-stage CMOS voltage comparator used in a monolithic CMOS CFD that utilized an external delay line [33]. The measured walk for this comparator was 2 ns for a 20-ns rise-time input signal having symmetrical overdrive and underdrive between 100 mV and 2 V (20:1 dynamic range). Although this walk performance is considerably poorer than the walk performance of the multistage Bipolar and GaAs voltage comparators previously described, the resulting CFD timing performance was adequate with careful walk adjustment for BGO/photomultiplier scintillation-detector PET applications. As mentioned earlier, the CMOS comparator included in the fully-monolithic CMOS CFD (described later in this section) has considerably improved walk performance over the previously-reported single-stage design. The performance improvements are the result of a multi-stage design having considerably improved gain-bandwidth product. Design approaches for minimizing comparator walk will

be discussed later in the discussion of the CMOS comparator used in the fully-monolithic CMOS CFD.

Recently, a family of high-speed, 0.7-μ CMOS analog cells has been introduced by NCR [44]. One of these cells is a voltage comparator (CP1101), which has a typical propagation delay of 21 ns for an input overdrive of 10 mV and load capacitance below 1 pF, a typical input-offset voltage of 5 mV, and a typical power consumption of 2.11 mW (+5 V at 422 μA). As is typical for most commercial comparators, no walk specification is given for this circuit.

Operation of CFD Walk-Adjustment Circuits

In practical CFD circuits, time-walk adjustment is required to obtain optimum timing performance. Time-walk may be adjusted by applying input signals of varying amplitude and monitoring the CFD bipolar shaping signal. A DC offset voltage is then applied to the shaping signal until the zero crossings of the shaping signal occur at nearly the same point. This DC offset voltage corrects for DC offset errors in the circuitry.

In addition to monitoring the CFD bipolar shaping signal, it is also possible to monitor the constant-fraction comparator output during time-walk adjustment. Adjusting this output for equal timing edges will compensate for DC offset errors and, to some degree, comparator walk errors. Some compensation of comparator time walk is possible by effectively boosting the level of small shaping signals with an additive DC offset.

In Siemens/CTI PET tomographs, CFD time walk is adjusted by observing the output of the constant-fraction comparator with no input signal present [19]. This output consists of amplitude-limited noise because of the high constant-fraction comparator gain. The shaping-signal DC offset (the time-walk adjustment) is then adjusted to obtain symmetrical constant-fraction comparator output noise indicating that circuitry is biased in the center of its linear region. Such a time-walk adjustment does not compensate for comparator time-walk errors but is adequate for BGO timing with high-performance constant-fraction comparators (e.g., high-gain, high-speed ECL comparators like those in the Plessey SP9685 [15] family).

Automatic walk adjustment for CFDs has been reported in the literature [2, 16]. These circuits sense the DC-offset error in the shaping signal and, through feedback, correct for this error. A gated-baseline restorer circuit can be used where the correction circuitry is disabled during the presence of a signal [16], or continuous baseline-restoration can be used [2]. Gated-baseline restoration minimizes baseline error at high count rates since false correction during the presence of a signal is disabled. A gated, autozero time-walk circuit will be outlined in *Section 6* for possible future enhancement of the monolithic CMOS CFD described later in this section.

Optimum time-walk adjustment is available by experimentally adjusting CFD time walk to obtain minimum walk for input signals having a given amplitude dynamic range. This can be done using a fixed test-input pulse source with an attenuation network to provide input signals having various amplitude levels. The attenuation network must introduce negligible time walk (for different settings of signal attenuation) for this technique to be useful. Time-walk was adjusted in this manner for the CMOS CFD (using an external delay line) described by Binkley et al. [33]. The time walk for this circuit is shown in Figure 5-2 for input signals having a 20-dB and 30-dB amplitude dynamic range. The time walk initially decreases as the input-signal amplitude increases reaching a minimum before beginning to increase. The time walk then increases for large input-signal amplitudes. As mentioned earlier in *Section 2*, increasing comparator propagation delay with increasing signal level is sometimes observed for large input-signal amplitudes, even though this propagation-delay behavior is in conflict with the comparator charge-sensitivity model. Critical time-walk adjustments were required for the CMOS CFD reported because of the relatively poor (compared to the high-gain, high-speed ECL comparators previously mentioned) constant-fraction comparator walk performance. The walk performance of the constant-fraction comparator contained in the monolithic CMOS CFD described later in this section is considerably improved over the previous Binkley et al. CMOS CFD circuit, eliminating the need for experimental time-walk adjustments.

Operation of CFD Arming Circuits

CFD arming circuits are required to prevent triggering on baseline noise. This noise includes both electronic noise and photoelectron-emission noise pulses that occur after the initial timing discrimination. Photoemission noise is particularly severe for low photoelectron-yield detectors, as illustrated in Figure 5-3 for a typical 511-keV event detected by a BGO/photomultiplier scintillation detector. The detector-output waveform shown was developed using Monte Carlo simulation (described in *Section 3*) using the detector characteristics described in Figure 5-3. The waveform includes the effects of a two-pole front-end amplifier having a composite time-constant of 4.55 ns (4.55 ns/$\sqrt{2}$ each pole) with a 10 - 90% rise-time of 10 ns. As seen in the waveform, it is necessary to *block* or inhibit CFD operation for at least 550 ns (nearly two 300-ns decay time constants) following timing discrimination to prevent CFD retriggering on photoelectron-emission pulses. This blocking time is required for a CFD arming threshold of 40 μA (25% of the 511-keV signal level).

CFD arming operation is illustrated in Figure 5-4 for the standard arming circuits shown in Figure 5-1. As shown in Figure 5-4, there are three possible CFD arming situations: *normal*, *leading-edge*, and *random*. The particular arming situation depends on the time relationship between the CFD arming comparator signal (denoted by *Arm 1*, *Arm 2*, and *Arm 3* for each arming situation in Figure 5-4) and the CFD constant-fraction comparator signal (denoted by *CF* in Figure 5-4). The *normal* arming situation results in no timing errors, the *leading-edge* situation results in no timing errors for slow-rise-time (SRT) reject arming circuits only, and the *random* situation always results in timing errors. Each of these arming situations is described below.

In the *normal* arming situation (for arming signal *Arm 2* in Figure 5-4), the constant-fraction signal is quieted or driven to the inactive state (caused by the negative-going shaping signal at the constant-fraction comparator input) *prior* to the presence of the arming signal. *Afterwards*, the arming signal becomes active *followed* by the transition of the constant-fraction signal to the active state. In this situation, both the ANDing of the arming and constant-fraction signals or the D-flip-flop qualification of the constant-fraction signal (Figure 5-1) results in a timing output that is related in time to the constant-fraction signal. The *normal* arming situation occurs if the CFD input moderately exceeds the arming threshold.

In the *leading-edge* arming situation (for arming signal *Arm 3* in Figure 5-4), the operation is identical to the *normal* situation except that the constant-fraction signal transitions to the active state *before* the arming signal becomes active. In this situation, ANDing of the arming and constant-fraction signals results in a timing signal that is related in time to the arming signal, resulting in leading-edge timing instead of the desired constant-fraction timing. Leading-edge timing is prevented for this situation by the use of slow-rise-time (SRT) reject arming circuits, such as D-flip-flop qualification of the constant-fraction signal (Figure 5-1). The D flip-flop prevents leading-edge timing because it will not produce a timing output if the constant-fraction signal precedes the arming signal. The *leading-edge* arming situation occurs when the CFD input signal only slightly exceeds the arming threshold or when the input-signal rise time is long compared to the CFD discrimination time.

In the *random* arming situation (for arming signal *Arm 1* in Figure 5-4), the constant-fraction signal is quieted *after* the arming signal becomes active. In this situation, either the ANDing of the arming and constant-fraction signals or the D-flip-flop qualification of the constant-fraction signal (Figure 5-1) results in a timing output that is derived from the noise

triggerings of the constant-fraction comparator. Such timing is random and early compared to the actual timing point. The *random* arming situation occurs when the input signal greatly exceeds the arming threshold. The *random* arming situation can also occur if a delay is introduced in the constant-fraction signal to permit more time (and accumulation of better statistics) for the CFD arming decision. Such a delay will be shown to improve CFD energy-discrimination performance with low photoelectron-yield detectors.

The choice of arming circuits is strongly dependent upon the application and no attempt will be made to select the optimum configuration for applications outside of BGO/photomultiplier scintillation-detector timing. As mentioned earlier, slow-rise-time (SRT) reject circuits are often used for Ge(Li)-detector timing because of the presence of some signals with slow rise-times that will cross the arming threshold *after* the constant-fraction timing signal is generated. Experimental measurements made at CTI PET Systems, Inc. with BGO/photomultiplier scintillation detectors have shown that better timing performance is available using a slow-rise-time reject D-flip-flop arming circuit (Figure 5-1) [20]. Additionally, Bialkowski has reported that less CFD retriggering occurs for BaF_2 scintillation detectors if a slow-rise-time reject D-flip-flop arming circuit is used [1]. The slow-rise-time reject D-flip-flop arming circuit will, however, introduce some timing error. These errors are due to the fact that the setup and hold times for the D-flip-flop will be violated for some percentage of events because of the random time relationships between the arming and constant-fraction signals. The propagation delay of ECL D flip-flops varies in the 100 - 200 ps range for signals violating the setup or hold times [2, 20].

There is not believed to be any substantive data to indicate which of the slow-rise-time D-flip-flop arming circuits shown in Figure 5-1 offers the best performance. In the monolithic CMOS CFD described later, the clock input to the arming D flip-flop can be selected from either an ANDing of the arming and constant-fraction signals or a direct connection of the constant-fraction signal. Additionally, the traditional arming circuit can be selected by setting the D input of the D flip-flop active and ANDing the arming and constant-fraction signals at the clock input. All reported measurements of CMOS CFD performance are for a slow-rise-time D-flip-flop arming circuit with ANDing of the arming and constant-fraction signals at the clock input. The other arming configurations were evaluated, but little difference in CMOS CFD performance was observed.

CFD arming design is complex for the case of Ge(Li)-detector signals because of widely-varying rise-time and shape. Arming design is also complex for the case of low-photoelectron-yield scintillation detectors such as BGO/photomultiplier detectors because of

the very limited statistics available for making an arming decision. Arming-circuit design involves a compromise between minimizing the rejection of valid events (those with acceptable energy) and minimizing timing errors.

Design of a Fully-Monolithic CMOS CFD

Circuit Overview

A fully-monolithic CMOS CFD was designed and fabricated using a standard 2-μ, double-poly, double-metal, n-well, digital CMOS process. This circuit will be included in a larger monolithic CMOS circuit under development for front-end signal processing in CTI/Siemens commercial PET systems.

A top-level circuit diagram, illustrating subcircuits and interconnections, is shown in Figure 5-5 for the CMOS CFD. Each subcircuit will be described briefly and detailed descriptions will follow for selected subcircuits. Full circuit descriptions and schematics are not given for competitive protection of CTI PET Systems, Inc.

Subcircuit *X1* is an arming filter, threshold circuit which provides lowpass filtering (single-pole time constant of 4 ns) and threshold offset for the arming signal. This subcircuit is followed by an arming comparator (subcircuit *X2*) which derives the arming logic signal. Hysteresis is included in the arming comparator to minimize noise triggering. Subcircuit *X3* is the CFD shaping circuit which is a Binkley five-pole Gaussian CFD circuit. The CFD shaping circuit is followed by the constant-fraction comparator (subcircuit *X4*). The constant-fraction comparator derives the constant-fraction timing logic signal. Subcircuit *X5* is an arming delay generator which provides a nominal 10-ns delay at the constant-fraction-comparator output. As discussed earlier in *Section 4*, the use of this delay significantly improves CFD energy-discrimination performance by permitting additional time for the accumulation of arming statistics.

Two independent sets of arming-logic circuits are included in the CMOS CFD (Figure 5-5): traditional saturating CMOS-logic circuits (subcircuits *X9* - *X11*) and specially-designed linear CMOS-logic circuits (subcircuits *X6* - *X8*). The specially-designed linear CMOS-logic circuits consists of source-coupled logic circuitry having topology similar to bipolar ECL logic circuitry. These circuits are designed to introduce much lower power-supply switching noise compared to traditional CMOS saturating logic. Both the saturating and source-coupled arming logic circuits are configurable (through the assignment of three mode input pins) for the traditional arming or slow-rise-time reject arming configurations shown in Figure 5-1 (page 226).

Subcircuit *X12* (Figure 5-5) is a process-tuning circuit designed to regulate the resistance associated with 4 μ/4 μ (drawn-channel width/drawn-channel length) P-channel MOSFETs operated in the ohmic region. This circuit regulates the resistance of these ohmic devices at 15-kΩ by sensing a voltage drop of 1.5 V for an applied current of 100 μA. The 15-kΩ ohmic devices are used as resistors having low parasitic capacitance since only diffusion and poly-silicon resistors are available in the CMOS process used.

Subcircuit *X13* develops reference voltages for cascode current sources and cascode current sinks which are used to develop bias currents in the CMOS CFD. A reference current of 100 μA is externally provided for subcircuit *X13*. The remaining subcircuit, *X14*, is used for miscellaneous logic functions. These functions include logic inversion and combinational gating for arming-logic mode and reset control. The arming logic remains latched following a CFD output until an external reset signal is provided.

A layout plot of the CMOS CFD is shown in Figure 5-6. The circuit was laid out using the MAGIC geometrical layout editor (a public domain program) [45] onto an Orbit Semiconductor [46] tiny-chip die frame having dimensions of 2.4 mm x 2.4 mm. The CMOS CFD contains 640 CMOS transistors and consumes 135 mW for supply voltages of +5 V and -5.2 V. A differential output driver in the CMOS CFD (subcircuit X8 in Figure 5-5) consumes 50 mW of the total 135 mW power consumption. The transistor count and power consumption of the final circuit will be approximately one-half that of the prototype circuit because of the elimination of multiple logic sections and other extra circuits included for testing various constant-fraction arming configurations.

CMOS Process Characteristics

Nominal process characteristics for the 2-μ, double-poly, double-metal, n-well CMOS process used are given in Table 5-1 [46]. Prototyping services are currently available for this process through the Orbit Foresight service (run closings every week) [46] and through the MOSIS service (run closings every other month) [47]. Current prototype prices are $1500.00 for 12 tiny chips (2.4 mm x 2.4 mm die size) with a turn-around time of approximately 6 weeks (Orbit Foresight service) and $510.00 for 4 tiny chips with a turn-around time of approximately 10 weeks (MOSIS service). The development of the high-speed CMOS analog circuits is greatly facilitated by the availability of low-cost, fast turn-around prototype services.

Table 5-1. Nominal Process Characteristics for the 2-μ, Double-Poly, Double-Metal, N-Well CMOS Process Used.

Parameter	N-Ch	P-Ch
Threshold Voltage, V_T (V)	0.75	-0.75
Body Effect Parameter, γ ($\sqrt{V}$)	0.25	0.55
Transconductance Parameter, $K = \mu_0 C_{OX}$ ($V^2/\mu A$)	46	15
Subthreshold Slope (V^{-3}/decade)	100	100
Channel Length Lateral Diffusion, L_D (μ)	0.3	0.4
Channel Width Lateral Diffusion, W_D (μ)	not specified	not specified
Gate Oxide Thickness, T_{OX} (Å)	400	400
Nominal parameters given for Orbit Semiconductor 2-μ, 2-metal, 2-poly, n-well process.		

SPICE simulations for the CMOS CFD were performed using BSIM (level 4) MOSFET models which model circuit-parameter sensitivities to channel length and channel width [48]. Extracted BSIM parameters from MOSIS run *n09e* (extracted in early 1990) were used for simulations. These parameters are believed to be representative for an average process run based on comparisons of approximately ten process-parameter sets. Extracted BSIM parameters were not available for the Orbit Foresight prototype run used for fabrication of the CMOS CFD.

Binkley Five-Pole Gaussian CFD Shaping Circuit

A Binkley five-pole Gaussian CFD shaping circuit was implemented in the CMOS CFD. The use of this shaping circuit eliminated the external delay line required for the delay-line CFD and permitted a fully-monolithic implementation of the CMOS CFD. A nominal time constant of 0.75 ns was selected for each of the real poles used in the Binkley five-pole Gaussian CFD shaping circuit giving a delay time constant of 1.677 ns ($\sqrt{5}$ x 0.75 ns). This time constant was selected using Monte Carlo simulations to obtain a timing resolution of approximately 3 ns FWHM with the BGO/photomultiplier scintillation detector. A fraction of 50% was used for the Binkley Gaussian CFD shaping circuit because, as described in *Section 4*, zero-crossing slope is maximized and timing jitter is minimized for this fraction

value. The DC gain (and ratio of output overdrive to input-signal amplitude) of the Binkley Gaussian CFD is equal to one minus the fraction (1 - *f*). This gain is equal to one-half for the fraction of 50%, so an additional gain of two was added to give a nominal DC gain of one. As discussed in *Section 4*, gain can be applied to the Binkley Gaussian CFD circuit to make the shaping-signal underdrive, overdrive, and zero-crossing slope comparable to that of the delay-line CFD.

A CMOS continuous-time (non-switched) filter was used to implement the Binkley five-pole Gaussian CFD shaping circuit. There are two primary CMOS continuos-time filters in use: MOSFET-C and g_m-C filters. Both MOSFET-C and g_m-C filters are voltage-mode filters with input-voltage and output-voltage signals. In MOSFET-C filters, voltage integrators are constructed from operational amplifiers using capacitive feedback and MOSFET resistors (MOSFETs operating in the ohmic region) connected between the input signal and the integrator virtual ground [49, 50, 51, 52, 53]. In g_m-C filters, a transconductor or operational transconductance amplifier (OTA) is used to convert input voltage to current, and this current flows into a capacitive load creating an integrator [49, 54, 55, 56]. The integrators created by both MOSFET-C and g_m-C filters can be combined to create active biquad or state-variable filters.

In MOSFET-C and g_m-C filters, differential signal operation is generally used. Differential-signal operation results in even-order circuit-distortion cancellation (resulting in lower distortion and nonlinearity), zero systematic differential-signal offsets, and enhanced power-supply rejection compared to single-ended operation. Differential continuous-time filter circuits, however, usually require common-mode feedback circuits to establish common-mode signal levels. These circuits increase circuit complexity and may deteriorate large-signal transient response.

A special fully-differential, current-mode CMOS continuous-time filter was developed for the Binkley five-pole Gaussian CFD shaping circuit. This circuit has the advantages of circuit simplicity, the requirement of no common-mode feedback, and very wideband performance (> 100 MHz for the 2-μ CMOS process) compared to traditional MOSFET-C and g_m-C filters. A schematic diagram of the continuous-time filter is shown in Figure 5-7.

In the continuous-time filter shown in Figure 5-7, a linearized transconductor consisting of a cross-coupled differential pair (MOSFETs M1, M2, M3, and M4) is used to convert input-signal voltage to signal current. This transconductor is required for the CMOS CFD prototype because voltage signals are used for testing. In the final CMOS CFD, the input

transconductor will be removed as the continuous-time filter will be driven directly from an internally-generated current signal.

Linearized transconductors are an important component in MOSFET g_m-C continuous-time filters as they are dominant contributors of circuit distortion and noise. Linearized transconductors consist of cross-coupled differential pairs, differential pairs with resistive degeneration, and other circuit topologies designed to significantly reduce the large-signal distortion of a simple differential pair [56, 57, 58, 59]. In the cross-coupled differential pair of Figure 5-7, the feedback pair (MOSFETs M3 and M4) is used to cancel the third-order distortion of the primary pair (MOSFETs M1 and M2). Even-order distortion (excluding the effects of device mismatches) is canceled through differential operation.

In the linearized transconductor, the primary pair (MOSFETs M1 and M2) devices are nearly replicated from those used in the feedback pair (MOSFETs M3 and M4). The primary pair devices consist of a 3 μ/5 μ device in parallel with a 4 μ/5 μ device. The feedback pair devices consist of single 3 μ/5 μ devices. Device replication is used to minimize ratio mismatches between the primary and feedback pairs as a result of lateral (width) diffusion variations in the process. The device geometry ratios between the primary and feedback pair control the third-order distortion cancellation.

In the continuous-time filter (Figure 5-7), the input transconductor differential-output current is mirrored with cascode current mirrors into two paths: a (Binkley CFD) fraction path with output at the drains of MOSFETs M18 and M24, and a (Binkley CFD) lowpass-filtered path with output at the drains of M16 and M22. Signal current in the lowpass-filtered path is then directed through two cascaded grounded-gate stages: M25 and M26 which constitute the first stage, followed by M27 and M28 which constitute the second stage. The (input) sources of these grounded-gate devices are loaded with capacitance to create single-pole lowpass filters having a time constant of nearly 0.75 ns. The output of the second cascaded grounded-gate stage, the drains of M27 and M28, is then connected to a cascode current mirror with inputs at the drains of M32 and M34. The input of this current mirror is capacitively loaded to create another single-pole lowpass filter with a time constant of nearly 0.75 ns. The output of this current mirror, the drains of M36 and M38, is then connected to two final cascaded grounded-gate stages: M40 and M41 constituting one stage, and M42 and M43 constituting the second stage. The (input) sources of these grounded-gate devices are capacitively loaded to create single-pole lowpass filters with time constants of nearly 0.75 ns, resulting in a total of five single-pole lowpass stages for the (Binkley CFD) lowpass-filtered path in the continuous-time filter. Five single-pole lowpass stages are

provided by four grounded-gate stages and one current-mirror stage, each of which is capacitively loaded to set the real-pole time constant.

The five-pole lowpass-output current at the drains of MOSFETs M42 and M43 is combined with the fraction output current at the drains of M18 and M24 in the continuous-time filter (Figure 5-7). These currents are summed at the inputs (sources) of the grounded-gate stage consisting of M44 and M45. The summed currents then flow into ohmic-load devices, consisting of M46 and M47, where a differential voltage is developed. This differential-output voltage is buffered with a source-follower stage consisting of M51 and M52 to permit the driving of capacitive loads associated with the input capacitance of the following stage (the constant-fraction comparator) and interconnection trace capacitance. MOSFET transmission gates, M59 and M60, are included to permit DC monitoring of the continuous-time filter output voltage prior to output buffering. Such monitoring capabilities are useful for monitoring intermediate-stage outputs in a complex analog integrated circuit.

The DC current gain from the input current (drains of M14 and M20) of the continuous-time filter (Figure 5-7) to the output of the fraction path (drains of M18 and M24) is unity. However, the DC current gain from the input to the output of the lowpass-filtered path (drains of M42 and M43) is two. As a result, the DC current gain is one and the fraction is effectively 50% for the Binkley five-pole Gaussian CFD shaping circuit. As discussed earlier, gain was included to maximize shaping signal overdrive, underdrive, and zero-crossing slope (the DC gain is normally one-half for the Binkley CFD shaping circuit with a fraction of 50%). The continuous-time input transconductor transconductance is slightly under 100 μS, and the resistance associated with the ohmic loads (M46 and M47) is approximately 10 kΩ. The resulting DC voltage gain for the continuous-time filter is then slightly under one, being equal to the product of input transconductance, current gain, and load resistance. The subtraction of the fraction path from the lowpass-filtered path in the continuous-time filter is provided by circuit inversion in the fraction path.

The continuous-time filter of Figure 5-7 is considerably simpler than a corresponding MOSFET-C or g_m-C filter implementation. These implementations would require five integrator sections (one for each lowpass-filter pole), summing circuitry to set the Q and gain of two second-order sections and the gain of one first-order section, and circuitry for subtracting the fraction path from the filtered path. In addition, common-mode feedback circuitry would probably be required to establish common-mode signal levels. Also, it would be difficult, if even possible, to generate real poles with time constants of 0.75 ns (the

corresponding -3-dB frequency is 212 MHz) in a 2-μ CMOS process using integrator sections configured in biquad or state-variable active filters.

The continuous-time filter presented here (Figure 5-7) introduces only real poles in the lowpass-filtered path whereas complex-poles for Butterworth, Bessel, Chebyshev, etc., filters can be introduced by MOSFET-C and g_m-C filters. Interestingly, as discussed in *Section 4*, the subtraction of a fraction path from a Gaussian lowpass-filtered path results in a network response having real poles and a combination of real and complex zeros (assuming more than a second-order Gaussian filter is used). It is possible that complex poles could be introduced in the continuous-time filter presented here with the use of added feedback circuitry.

The variation in filter pole and zero locations with integrated-circuit process variations must be evaluated in continuous-filter design in order to determine what filter tuning, if any, is required. In the Binkley five-pole Gaussian CFD continuous-time filter (Figure 5-7), the time constants associated with real poles introduced by the Gaussian lowpass circuitry are set by the parallel combination of circuit capacitance and MOSFET transconductance. The time constant associated with the input node (source) of each grounded-gate stages is approximated by

$$\tau_{grounded-gate\,stage} = \frac{C_S}{g_m} = \frac{C_S}{\sqrt{2I_{bias}K'W/L}} \quad , \tag{5-1}$$

where g_m, K', W, L, and I_{bias} is the transconductance, transconductance factor for saturation operation in strong inversion, effective channel width, effective channel length, and bias current for the grounded-gate MOSFET device. C_S is the total capacitance connected to the grounded-gate MOSFET source terminal which includes the MOSFET gate-source capacitance, the MOSFET source diffusion capacitance, and externally connected capacitance.

From Equation 5-1, the time constant associated with each grounded-gate stage varies as the inverse square root of the transconductance-factor (K') and shape-factor (W/L) product (I_{bias} is held constant). This product is expected to vary by ±20% over the CMOS process resulting in a time-constant variation of ±10%. The time constant associated with each grounded-gate stage varies directly with total source capacitance (C_S) which is expected to vary below ±15% over the CMOS process, due to ±15% variations in poly-poly capacitors and lower variations in MOSFET gate-source capacitance. The total time-

constant variation is then expected to be below ±25% over the CMOS process, ±10% due to MOSFET transconductance variations and less than ±15% due total source capacitance variations. The same time-constant variation is expected for the single pole introduced by the current mirror in the lowpass filter path (input at MOSFETs M32 and M34) because this time constant is controlled by MOSFET transconductance and shunt capacitance as well.

In the continuous-time filter (Figure 5-7), tuning is not used to correct for filter time-constant variations caused by CMOS process variations. The change in timing resolution resulting from the expected ±25% variation in delay time constant for the continuous-time filter (Binkley five-pole Gaussian CFD shaping circuit) can be estimated by considering the change in Monte Carlo timing resolution for a Binkley four-pole Gaussian CFD shaping circuit. From the Monte Carlo timing resolution shown in Figure 4-24 (page 168) for the Binkley four-pole Gaussian CFD shaping circuit, timing resolution is 3.5 ns FWHM for a delay time constant of 1.5 ns ($\sqrt{4}$ x 0.75 ns; 0.75 ns time constant for each individual real pole in the continuous-time filter) varying by less than ±9% for ±25% variations in delay time constant. Variations in CMOS CFD timing resolution of ±9% resulting from CMOS process variations are acceptable. Variations in the CFD continuous-time filter zero-crossing time will, however, be corrected for by an adjustable delay generator in the final PET front-end monolithic CMOS circuit. These zero-crossing variations are expected to be ±2.5 ns over the CMOS process and will add to propagation-delay variations (±2 ns) expected for the CMOS CFD constant-fraction comparator and arming logic circuitry.

In Figure 5-8, SPICE-simulated signals are shown for the Binkley Gaussian CFD continuous-time filter (Figure 5-7). SPICE simulation was performed using BSIM model parameters and full layout parasitic capacitances. In Figure 5-8, the continuous-time filter input voltage, transconductor output current, fraction output current, Gaussian-lowpass stage output currents, CFD output current, and CFD output voltage are shown. The input signal has amplitude of 1 V and rise-time of 10 ns (10 - 90%) which models the photomultiplier-tube and two-pole-lowpass amplifier described in Figure 4-21 (page 166). All signals shown for the continuous-time filter in Figure 5-8 are differential voltage or current signals.

In Figure 5-8, the signal delay introduced by the Gaussian lowpass-filter stages is shown for the Binkley Gaussian CFD continuous-time filter. The delay for each of the five single-pole lowpass stages is nominally 0.75 ns (equal to the time constant associated with that stage). It was necessary, however, to shorten the delay of the final two stages to compensate

for excessive delay in the third stage, which is a cascode current mirror stage. The single-pole lowpass stages were retuned to compensate for layout parasitics by adjusting the value of the associated poly-poly capacitors.

The output voltage signal (Figure 5-8) for the Binkley five-pole Gaussian CFD continuous-time filter has an underdrive of -81 mV, an overdrive of +770 mV, and a zero-crossing slope of 46 mV/ns for the input voltage of 1 V. If the filter voltage gain were unity (it is actually 0.77), the zero-crossing slope would be 60 mV/ns or 68% of the peak input-voltage slope of 88 mV/ns (occurring at 36.4% of the peak input voltage). The filter, when set for unity DC gain, nearly preserves the input-signal slope.

The filter voltage gain of 0.77 is approximately equal to the transconductance of the input transconductor multiplied by the value of load resistance used to develop the output voltage signal. Additionally, there is a slight loss in gain caused by the output source-follower buffers due to MOSFET body effect. As mentioned earlier, the DC current gain from the input transconductor output to the output load resistance is unity.

SPICE-simulated DC linearity of the CFD continuous-time filter is shown in Figure 5-9 for both current and voltage output signals for DC input voltages up to 2 V. The circuit transconductance (output current divided by input voltage) is 0.88 μS, and the circuit voltage gain (output voltage divided by input voltage) is 0.77. The SPICE-simulated small-signal voltage gain (also shown in Figure 5-9) is equal to 0.772, 0.769, 0.771, and 0.780 for input levels of 0 V, 1 V, 1.5 V, and 1.8 V. This corresponds to a differential nonlinearity of less than ±0.002% for input signals between 0 and 1.5 V.

Low circuit distortion is needed to minimize large-signal time walk introduced by circuit distortion. Actual circuit distortion will be higher than that shown in Figure 5-9 because of MOSFET mismatches. Device mismatches result in incomplete cancellation of second-order distortion provided through differential operation. Additionally, mismatches result in incomplete cancellation of third-order distortion cancellation provided in the linearized input transconductor (MOSFETs M1, M2, M3, and M4). Measured DC output voltage is shown in Figure 5-9 illustrating that DC nonlinearity is not visually discernible in the figure. As only limited measurements were taken, no analysis of measured DC linearity was done. The measured DC gain is 0.746, approximately 3% below the SPICE-simulated gain of 0.77 (BSIM SPICE parameters used are from a nominal run as parameters were not available for the actual fabrication run).

SPICE-simulated walk performance for the CFD continuous-time filter is shown in Figure 5-10 for the input signal (representative of the BGO/photomultiplier output) used in

Figure 5-8. The simulated walk (Figure 5-10) is equal to 15 ps for input-signal overdrives ranging from 0.1 - 1 V, increasing to 50 ps and 80 ps respectively when input-signal overdrive is extended to 1.5 V and 2.0 V. Actual walk will be higher due to device mismatches causing increased circuit distortion, but time walk is expected to be negligible for BGO/photomultiplier detector applications. The effect of continuous-time filter walk on CMOS CFD timing performance will be evaluated later.

SPICE-simulated frequency response and group delay for the CFD continuous-time filter is shown in Figure 5-11 and Figure 5-12. The -3-dB frequency is approximately 75 MHz for the fraction current, 50 MHz for the five-pole lowpass current, 140 MHz for the CFD output current, and 120 MHz for the CFD output voltage. The group delay drops by only 10% at 30 MHz for the fraction and lowpass currents, indicating nearly constant signal delay. However, group delay drops rapidly above 5 MHz for the CFD output current and voltage. The nearly flat frequency response for the CFD output combined with the highly nonlinear phase response (nonconstant group delay) results in severe distortion for transient inputs. This transient distortion is, in this case, responsible for the desired CFD output characteristic: a bipolar pulse with good underdrive and zero-crossing slope levels.

Total SPICE-simulated output noise for the continuous-time filter is 1,600 μV rms. The commercial version of SPICE used does not properly model the noise of ohmic-region MOSFETs, as it bases the noise on the operating transconductance and not on the drain-source ohmic resistance [60]. The noise contribution of the ohmic-load MOSFETs is expected to be negligible compared to the input noise of the input transconductance stage. However, the actual continuous-time filter output noise is expected to be 1.5-2 times higher than the value predicted by SPICE due to increased MOSFET noise (for saturation operation) over the simple transconductance noise model which predicts an effective device noise resistance of $0.67/g_m$. Additionally, there will be some increase in noise due to 1/f noise in the small N-channel MOSFET input-transconductor devices (M1 - M4), but this is not expected to be significant for a CFD noise bandwidth of over 100 MHz (Figure 5-11). A wideband, continuous-time filter output noise of 3,200 μV rms (two times the SPICE-simulated value) will be assumed for later CFD timing jitter estimation.

Constant-Fraction Comparator Circuit

Comparator Propagation-Delay Modeling

As discussed in the charge-sensitivity model of *Section 2*, comparator propagation delay is dependent on input-signal slope and overdrive giving rise to time walk. The modeling of

comparator propagation delay, however, is considerably more complex than that predicted by the charge-sensitivity model. Actual comparator propagation delay consists of a fixed delay component, a component that is dependent upon input-signal slope and overdrive, and a component that is dependent to a lesser degree on input-signal underdrive [38]. Additionally, the monotonically-decreasing propagation delay with increasing input-signal overdrive predicted by the charge-sensitivity model is not always valid as propagation delay can actually begin to increase for large levels of overdrive. This has been observed for some CMOS comparators designed and evaluated at CTI PET Systems, Inc. [20], including the constant-fraction comparator developed for the CMOS CFD.

Comparator propagation-delay models will not be developed in this work except for one model which gives good accuracy compared to SPICE simulations. The comparator modeled is the VTC VC7695 [21] high-speed, ECL voltage comparator with SPICE-simulated propagation delay reported by Binkley and Casey [22] and measured propagation delay reported by Turko [23, 38].

The comparator propagation-delay model is considered for triggering along the edge of an input signal having constant slope. From the charge-sensitivity model, comparator propagation delay is given (Equation 2-10, page 24) by

$$t_{prop(\,triggering\ on\ signal\ edge)} = \sqrt{\frac{2A}{K}} \quad , \tag{5-2}$$

where K is the input-signal slope and A is a constant denoting comparator charge sensitivity. The charge-sensitivity model is modified to consider comparator slew-rate limitations and the presence of a fixed (latent) propagation delay. The modified propagation-delay model is given by

$$t_{prop(\,triggering\ on\ signal\ edge)} = \sqrt{\frac{2A}{K_{eff}}} + t_{latency} \quad , \text{ where} \tag{5-3}$$

$$K_{eff} = \frac{1}{\sqrt{(1/K)^2 + (1/K_{lim})^2}} \quad , \tag{5-4}$$

and K_{lim} is the limiting input-signal slope (or slew rate) due to slew-rate limitations within the comparator, and $t_{latency}$ is the fixed comparator propagation delay.

A comparison of modeled and SPICE-simulated delay is given in Table 5-2 for the VC7695 comparator. Values for the charge-sensitivity area (A), fixed delay ($t_{latency}$), and limiting input-signal slope (K_{lim}) are given in the table along with the calculated effective input slope (K_{eff}), calculated (modeled) delay, SPICE-simulated delay, and error between the calculated and SPICE-simulated delay. As shown in the figure, the modeling error (relative to SPICE simulations) is surprisingly good, within ±0.25% for input-signal slopes ranging from 5 - 1,000,000 V/μs. Although measurements of comparator propagation delay are not presented in the table, SPICE-simulated walk is believed to be reasonably accurate since Turko [38] reported measured walk of 250 ps which compares favorably with the SPICE-simulated walk of 185 ps reported by Binkley and Casey [22]. These walk measurements and simulations were for step inputs having input-signal overdrive between 10 mV and 1 V (100:1 dynamic range).

The comparator propagation-delay model just described is offered as a starting point for propagation-delay modeling beyond the simple charge-sensitivity model. Additional model development should include the case of comparator triggering after the signal edge as well as the case considered for comparator triggering along the signal edge. Additionally, nonlinear effects, such as possible propagation-delay increases with large input-signal overdrive, should be considered in future modeling.

Table 5-2. Comparison of Modeled and SPICE-Simulated Propagation Delay for the VC7695 High-Speed, ECL Voltage Comparator.

Input-Signal Slope (V/μs)	Effective Slope (V/μs)	Modeled t_{prop} (ns)	SPICE t_{prop} (ns)	Error (Modeled vs. SPICE)
5	4.925	2.686	2.680	+0.235%
10	9.440	2.398	2.403	-0.220%
20	16.390	2.217	2.220	-0.147%
50	24.826	2.110	2.105	+0.234%
100	27.498	2.087	2.090	-0.150%
1,000,000	28.600	2.078	2.083	-0.226%
Model Parameters: K_{lim} = 28.6 V/μs, A = 2.66E-6 (V μs), $t_{latency}$ = 1.647 ns				

Comparator Design Fundamentals

The comparators considered here are continuous-time comparators where regeneration is not used. A continuous-time comparator is required if the comparator decision time is arbitrary, which is the case for CFD applications. Clocked comparators employing regeneration are used to sample an input at a given point in time. Wu and Wooley [61] reported that the amplification required in a comparator is best achieved by regeneration from positive feedback. It is possible, however, to use limited positive feedback and raise comparator gain without regeneration for continuous-time comparator applications. This has been reported by Allstot [62].

Comparator design methods for minimizing propagation delay have been reported in the literature by Doernberg, Gray, and Hodges [63], by Wu and Wooley [61], and by others. Design methods for minimizing comparator walk, however, are not believed to have been reported.

Doernberg, Gray, and Hodges [63] give a method for determining the number of stages and the gain of each stage for achieving minimum comparator propagation delay for a selected total gain. In this method, identical cascaded single-pole-lowpass amplifier stages are considered. The gain-bandwidth of each stage is given by

$$GBW = A\omega_p = \frac{A}{\tau} = \frac{G^{1/n}}{\tau} , \tag{5-5}$$

where A, ω_p, and τ are the gain, 3-dB frequency, and time-constant associated with a single stage, and G is the total comparator gain. The total comparator delay is then given by

$$t_{prop} = n\tau = \frac{nG^{1/n}}{GBW} , \tag{5-6}$$

which is minimized (by solving for n when the derivative of Equation 5-6 with respect to n is equal to zero) for the number of stages and gain of each stage given by

$$n = \ln(G), \text{ and} \tag{5-7}$$

$$A = e . \tag{5-8}$$

From this analysis, total comparator delay is minimized using a stage gain of e (2.718) with the number of stages set by the total comparator gain. The result of this analysis has been

used to size cascaded digital CMOS inverters for driving an external load where the width-to-length ratio of successive inverters increases by nearly e [64]. The result of another comparator-propagation-delay analysis, reported by Wu and Wooley [61], is nearly identical to the analysis just described.

Comparator walk performance is dependent upon total comparator gain-bandwidth product, assuming linear circuit operation. Comparator walk is minimized for maximum values of total gain-bandwidth product. A high DC gain ensures full output-signal transitions for different input-signal levels, and a high bandwidth ensures quick output-signal transitions with small changes in propagation delay (walk) for different input-signal levels.

The conditions for minimizing comparator propagation delay are different from those for minimizing comparator time walk. Propagation delay is minimized using as many cascaded stages with gains of e as required to obtain the desired gain. Time walk is minimized (assuming linear circuits) using an infinite number of stages to maximize total gain-bandwidth product. In practice, there is a tradeoff between comparator delay, time walk, and the number of cascaded stages feasible.

Linear-circuit operation, or small-signal operation closely approximating linear operation, is assumed in the propagation-delay and time-walk analysis previously described. In practical comparator circuits, circuit nonlinearity contributes to time walk. Walk is introduced by varying comparator recovery time (from saturated output levels) with input-signal underdrive and overdrive.

Comparator Walk Comparisons for CMOS Integrator and Single-Pole-Lowpass Stages

Comparator output zero-crossing time (propagation delay) and time walk will be considered for a CMOS integrator and single-pole-lowpass amplifier stage. Zero-crossing propagation delay and time walk are largely independent of circuit gain because infinitesimal gain is required to obtain an output zero crossing (following an input zero crossing). Zero-crossing propagation delay, however, is a useful measure of inherent circuit response time. Additionally, zero-crossing time walk is a useful measure of walk caused by circuit nonlinearities. It will be shown that output zero-crossing time walk is much worse for the CMOS integrator compared to the single-pole-lowpass amplifier.

In the CMOS integrator stage of Figure 5-13, MOSFETS M1 and M2 form a differential pair which is biased at constant current. MOSFETS M3 and M4 are current sources which are regulated to set the integrator output common-mode voltage at 3 V. Integrator stages

have the disadvantage of requiring common-mode feedback circuits to set the common-mode output level. Integrator output-voltage limiting is provided by diodes on the differential-integrator outputs to model circuit limiting. Output limiting is inherently present for integrator stages, limiting occurring through MOSFETs which enter the ohmic region or through a circuit limiter such as diode-connected MOSFETs. In the single-pole-lowpass stage of Figure 5-13, the integrator current sources M3 and M4 are replaced with resistive loads and the limiting diodes are removed. The single-pole-amplifier stage with resistive loads has the advantage of well-defined internal limiting since the voltage across the load resistance is equal to zero when load current is switched off and is equal to the limiting voltage (the product of current and load resistance) when load current is switched on. Additionally, the single-pole-amplifier has the advantage of requiring no common-mode feedback to stabilize the common-mode output voltage.

SPICE-simulated (level 2) time-walk performance of the differential CMOS integrator comparator stage (Figure 5-13) is illustrated in Figure 5-14 for linear-edge, differential signals having rise times of 10 ns. The integrator output zero-crossing propagation delay is measured from the zero crossing of the input signal (at 5 ns) to the zero crossing of the differential output signal. Integrator output zero-crossing propagation delay is 4.5 ns, 3.4 ns, and 1.4 ns for input levels of -10 mV to 10 mV, -100 mV to 100 mV, and -1000 mV to 1000 mV. The time walk for this 100:1 input-signal dynamic range is 3.1 ns which is quite large relative to the input-signal rise-time and integrator propagation delay. Time walk is large once the integrator outputs are limited because the time required for the output to return of zero is dependent on output slew rate, which is itself dependent on the input-signal level.

SPICE-simulated (level-2) time-walk performance of the differential CMOS single-pole-amplifier comparator stage (Figure 5-13) is illustrated in Figure 5-15 for the same linear-edge input signals considered for the integrator stage. The single-pole-amplifier output zero-crossing propagation delay is approximately 0.60 ns, 0.60 ns, and 0.57 ns for the input levels of -10 mV to 10 mV, -100 mV to 100 mV, and -1000 mV to 1000 mV. The time walk for this 100:1 input-signal dynamic range is 30 ps which is quite low relative to the input-signal rise-time and single-pole-lowpass amplifier propagation delay. Unlike the integrator stage considered, time walk for the single-pole-lowpass amplifier with resistive loads remains low once the outputs are limited. It is interesting to note that differential amplifiers with resistive loads provide excellent, low phase-noise limiters for phase-lock-loop frequency

synthesizers [65]. The low phase noise of differential limiters indicates that timing jitter is very low for these circuits, even in the presence of hard limiting.

The small-signal gain-bandwidth product of the integrator stage is 1.7 GHz for a small-signal gain of 48 and delay (equal to single-pole time constant) of 4.5 ns. The small-signal gain-bandwidth product of the single-pole-lowpass amplifier is comparable at 1.9 GHz for a small-signal gain of 7.3 and delay of 0.6 ns. Even though the gain-bandwidth products are comparable, the single-pole-amplifier stage considered has only 30 ps of output zero-crossing walk compared to 3.1 ns (a factor of one-hundred higher) for the integrator stage. The only advantage of the integrator is higher gain in a single stage. Equivalent gain (53.3 = 7.3 x 2), however, is available with much less propagation delay (1.2 ns = 0.6 ns x 2) and walk (in the neighborhood of 30 ps) by cascading two single-pole-lowpass amplifier stages. The improved walk performance of the two cascaded single-pole-lowpass stages is due to the much lower walk present in each stage because of limiting providing by resistive loads.

Differential input signals (with common-mode voltages of zero) were used for the integrator and single-pole-lowpass amplifier stages considered. SPICE simulations indicate that time walk is much worse (approximately a factor of four worse for step inputs) for single-ended input signals compared to differential input signals [20]. Differential signals are used throughout the CMOS CFD to minimize even-order distortion and maximize power-supply rejection. Improved comparator walk performance is another advantage in using differential signals.

In addition to the integrator (high impedance) and resistive loads considered, MOSFET diode-connected loads can be used in a comparator. A 1.6-μ CMOS three-stage comparator using MOSFET diode-connected loads has been reported [63]. Like resistive loads, MOSFET diode-connected loads have the advantage of requiring no common-mode feedback. MOSFET diode-connected loads were considered initially for low-walk comparator design, but SPICE simulations indicated inferior walk performance (over a factor of two worse) compared to the performance available using resistive loads. Inferior walk performance is due in part to the slow subthreshold MOSFET pull up of load voltage when current into the load is switched off. In contrast, aggressive pull up of load voltage is available when current into a resistive load is switched off.

A 4-μ CMOS three-stage comparator has been reported using MOSFET diode-connected limiters to provide limiting for MOSFET active loads [66]. Common-mode feedback was not required for these load networks. Walk performance was not considered for these load

networks, although it was previously shown that walk performance is poor for circuits having high-impedance (integrator) loads and diode limiters (Figure 5-14).

Comparator Walk Performance of Multiple CMOS Stages Having Ohmic-MOSFET Loads

In Figure 5-16, a CMOS comparator stage containing MOSFET resistive loads is shown. This stage approximates a single-pole-lowpass amplifier and, like the previously presented integrator and single-pole-pole lowpass amplifier stages, is fully differential. The input differential pair (MOSFETs M1 and M2) is cascoded with MOSFETs M3 and M4 to minimize input capacitance due to Miller effect. Resistive loads are provided by MOSFETs M5 and M6, which are operated in the deep ohmic region. The parasitic capacitance of these small MOSFET loads is lower than diffused resistors or polysilicon resistors. Output source followers (MOSFETs M7 and M8) provide output level shifting and buffering to permit driving cascaded stages. The remaining MOSFETs provide bias currents for the input differential pair and source followers.

The small-signal gain of the CMOS comparator stage (Figure 5-16) is approximated by

$$A = R_L g_m = \frac{V_{lim}}{I_{bias}} \sqrt{2(I_{bias}/2)K'W/L} = \frac{V_{lim}}{\sqrt{I_{bias}}} \sqrt{K'W/L} \ , \tag{5-9}$$

where g_m, K', W, and L is the transconductance, transconductance factor for saturation operation in strong inversion, effective channel width, and effective channel length for differential-pair MOSFET devices (MOSFETs M1 and M2). Additionally, R_L is the load resistance, V_{lim} is the limiting voltage, and I_{bias} is the differential input-pair bias current. In Equation 5-9, MOSFET source follower gain is assumed to be unity which assumes negligible source-follower body effect (this is a reasonable assumption since the nominal body-effect parameter is 0.25 for the process considered) and negligible source-follower loading by the bias current sources (also a reasonable assumption since the current sources are cascoded).

The small-signal gain of a multistage comparator using the CMOS comparator stage of Figure 5-16 is dependent on the input differential-pair transconductance, load resistance, and the number of cascaded stages. Multistage comparator small-signal gain is given from Equation 5-9 by

$$G = \left[\frac{V_{lim}}{\sqrt{I_{bias}}} \sqrt{K'W/L} \right]^n \quad . \tag{5-10}$$

The small-signal delay of the CMOS comparator stage (Figure 5-16) can be approximated assuming a single-pole response. The pole associated with the load resistance and shunt capacitance is considered whereas the parasitic poles associated with the cascode and source-follower devices are neglected. The effects of these parasitic poles will be considered later using SPICE simulation. The approximate small-signal delay of the CMOS comparator stage is given by

$$\tau = R_L C_L = \frac{V_{lim}}{I_{bias}} C_L \quad , \tag{5-11}$$

where C_L is the total capacitance appearing across the load resistance.

The approximate small-signal delay of a multistage comparator using the CMOS comparator stage of Figure 5-16 is dependent on the load resistance, load capacitance, and the number of cascaded stages. Multistage comparator small-signal delay is approximated from Equation 5-11 by

$$t_{prop} = n\tau = n \frac{V_{lim}}{I_{bias}} C_L \quad . \tag{5-12}$$

The multistage small-signal gain-bandwidth product, defined as the gain divided by the effective time constant for bandwidth, is approximated from Equations 5-10 and 5-11 as

$$GBW = \frac{G}{\tau_{BW}} = \frac{\left[\frac{V_{lim}}{\sqrt{I_{bias}}} \sqrt{K'W/L} \right]^n}{\sqrt{n} \frac{V_{lim}}{I_{bias}} C_L} = \left[\frac{(V_{lim})^{n-1}}{\left(\sqrt{I_{bias}}\right)^{n-2}} \right] \left[\frac{\left(\sqrt{K'W/L}\right)^n}{\sqrt{n} C_L} \right] \quad . \tag{5-13}$$

The gain-bandwidth product is generally maximized for increasing n, V_{lim}, K', and W/L and for decreasing C_L. As mentioned earlier, time walk is minimized for increasing gain-bandwidth product assuming linear circuit operation. The load capacitance C_L is somewhat dependent on the differential-pair MOSFET capacitance (which is related to the product of

MOSFET W and L) because the source-follower devices do not provide full isolation from the input capacitance of successive stages. Additionally, the critical frequencies of parasitic poles associated with the cascode and source-follower devices are strongly dependent on differential-pair MOSFET geometry making these poles, in general, nonnegligible. SPICE analysis is required to consider the effects of parasitic poles and to consider nonlinear circuit operation for large signals.

Walk performance for a comparator constructed of four cascaded single-pole-lowpass amplifier stages (Figure 5-16) will be evaluated for different limiting voltages (V_{lim}) and differential-pair MOSFET geometry. The output of the fourth stage is loaded into the input of another identical stage to consider circuit loading. The input signals considered for the comparator model the photomultiplier-tube and two-pole-lowpass amplifier described in Figure 4-21 (page 166), and a Binkley two-pole Gaussian CFD with a delay time constant of 3 ns and a fraction of 50%. The input signals considered are representative of the CFD signals present in the CMOS CFD. These input signals are shown later in Figure 5-21 (page 244).

Comparator propagation delay will be measured from the zero crossing of the input signal (at 11.728 ns) for CFD signals having amplitudes (final values) ranging from 10 mV to 1 V (100:1 dynamic range). A series of computer programs was developed to modify differential-pair MOSFET width, compute SPICE geometry parameters (drain and source area, perimeter, and numbers of squares) for the differential-pair MOSFETs, submit the circuit file to SPICE, and analyze the SPICE waveforms to determine propagation delay. Level-2 SPICE analysis was used because of convergence difficulties with level-4 (BSIM) runs. These convergence problems were later solved with a newer version of a commercial SPICE program. BSIM SPICE simulations are used later for characterization of the constant-fraction comparator used in the CMOS CFD.

The differential-output zero-crossing time (propagation delay) for the first comparator stage is shown in Figure 5-17 as a function of input signal level. Three different limiting voltages (V_{lim}) are considered: 1.1 V, 1.5 V, and 2.2 V, and three different (drawn) differential-pair MOSFET widths (W) are considered: 24 μ, 50 μ, 100 μ. All MOSFET (drawn) lengths (L) are 2 μ and the (drawn) widths of the remaining MOSFETS are given in the figure along with the bias currents.

As shown in Figure 5-17, comparator output zero-crossing propagation delay is minimized for minimum limiting voltage which corresponds to minimum load resistance since load resistance is equal to the limiting voltage divided by the differential-pair bias

current. Additionally, propagation delay is minimized for minimum input differential-pair MOSFET width since output loading from the input capacitance of the succeeding stage is dependent on this width. Propagation delay is also minimized for minimum input differential-pair MOSFET width since the output capacitance of the input-pair MOSFETS is dependent on this width. This output capacitance parasitically loads the input of the cascode devices.

Zero-crossing time walk at the comparator first-stage output (Figure 5-17) is minimized for the same conditions that minimize propagation delay: minimum limiting voltage and minimum input differential-pair MOSFET width. Time walk is minimized because a smaller differential input voltage and smaller input differential-pair width result in less switching of differential-pair currents. This results in more linear circuit operation over a larger range of input signal voltages. Zero-crossing time walk (for 10-mV to 1-V input signals) is 278 ps, 37 ps, and 2 ps for a limiting voltage of 2.2 V, 1.5 V, and 1.1 V and input differential-pair width of 100 μ, 50 μ, and 24 μ.

Differential-output zero-crossing time (propagation delay) at the fourth comparator stage output is shown in Figure 5-18 as a function of input signal level (the input signal is applied to the first stage input). As was true for the first stage output, zero-crossing time walk is minimized for minimum limiting voltage and minimum input differential-pair MOSFET width. Zero-crossing time walk (for 10-mV to 1-V input signals) at the fourth stage output is 703 ps, 231 ps, and 19 ps for a limiting voltage of 2.2 V, 1.5 V, and 1.1 V and input differential-pair width of 100 μ, 50 μ, and 24 μ. The zero-crossing time walk present at the fourth stage output is considerably higher than the zero-crossing time walk present at the first stage output. This is because the zero-crossing time walk is dependent on circuit nonlinearity which increases with the number of stages.

Zero-crossing propagation delay and time walk has been considered for the first and fourth stage outputs of the multistage CMOS comparator. As mentioned earlier, zero-crossing propagation delay and time walk are largely independent of circuit gain because infinitesimal gain is required to obtain an output zero crossing (following an input zero crossing). Zero-crossing propagation delay and time walk are a useful measure, however, of circuit response time and linearity respectively.

In actual comparator applications, the output signal would be required to reach some nonzero level to trigger successive circuitry. The comparator propagation delay for the differential-output signal to reach +0.5 V is shown for the fourth-stage output in Figure 5-19. The walk (for 10-mV to 1-V input signals) for a limiting voltage of 2.2 V and differential-

pair width of 100 μ is 750 ps, which is nearly the same as the zero-crossing walk of 703 ps shown in Figure 5-18. For this case, walk is dominated by circuit nonlinearity and not by limited gain or gain-bandwidth product. The single-stage gain and gain at the fourth-stage output (from Equation 5-10) is approximately 8.94 and 6,390, respectively. It is interesting to note that the fourth-stage propagation delay monotonically *increases* with input signal level for the case considered, in direct conflict with the comparator charge sensitivity model which predicts monotonically decreasing propagation delay with increasing input signal level.

In contrast with the 2.2-V limiting voltage and 100-μ input differential-width case just considered, time walk for a fourth-stage 0.5-V output crossing is dominated by the effects of limited comparator gain for a 1.1-V limiting voltage and 24-μ differential-pair width. The single-stage gain and gain at the fourth-stage output (from Equation 5-10) is approximately 2.19 and 23, respectively. The gain is much lower for this case because of the low load resistance associated with the 1.1-V limiting voltage and the low input differential-pair transconductance associated with 24-μ input-pair widths. The total four-stage comparator gain (given in Equation 5-10) is a strong function of these parameters since the total gain is equal to the gain of a single stage raised to the fourth power. The propagation delay for a fourth-stage 0.5-V output crossing decreases strongly with increasing input signal level resulting in an extremely high walk (for 10-mV to 1-V input signals) of 8,485 ps.

A 1.5-V limiting voltage and 50-μ differential-pair width results in a good compromise between minimum propagation delay and minimum walk for a fourth-stage 0.5-V output crossing (Figure 5-19). The single-stage gain and gain at the fourth-stage output (from Equation 5-10) is approximately 4.31 and 345 respectively. The walk (for 10-mV to 1-V input signals) for a 0.5-V output crossing is 611 ps which is somewhat above the zero-crossing walk (Figure 5-18) of 231 ps due to limited comparator gain. In the arming and constant-fraction comparators used in the CMOS CFD, the 1.5-V limiting voltage and 50-μ differential-pair width will be used with an additional (fifth) comparator stage added to increase the comparator gain-bandwidth and further reduce 0.5-V output-crossing walk.

Comparator walk is controlled primarily by circuit nonlinearities (as observed by zero-crossing walk) and by circuit gain and gain-bandwidth product (as observed by the additional propagation delay required for the comparator output to reach a nonzero output threshold voltage). As previously illustrated, these two components of walk performance can be in conflict with each other. For example, a small limiting voltage and small MOSFET differential input-pair width gives low walk due to circuit nonlinearity but high

walk due to limited circuit gain and gain-bandwidth. Comparator design for minimizing walk is further complicated by the fact the comparator propagation delay and walk are each optimized differently. Comparator design involves complex compromises between walk performance, propagation delay, and circuit size and power dissipation. Such design is best optimized (especially considering circuit nonlinearities) using circuit iterations with the most accurate SPICE simulation available.

Measured and Simulated Performance of a Three-Stage CMOS Comparator

A three-stage comparator was fabricated in a standard 2-μ, double-metal, double-poly, p-well CMOS process using the MOSIS [47] prototyping service. The measured and SPICE-simulated propagation-delay and walk performance for this comparator is given here to validate SPICE comparator simulations. Validation of SPICE simulation is necessary since it was not possible to measure comparator performance in the CMOS CFD, as test comparators could not be included in the prototype circuit.

The three-stage comparator fabricated consists of the stages shown in Figure 5-16, except that single-transistor current sources are used. The MOSFET input-pair devices (M1 and M2) are 100 μ/2 μ devices and the ohmic-load devices (M5 and M6) are 3 μ/2 μ devices giving a limiting voltage of 1.1 V for the bias current of 100 μA. A saturating-logic output stage is included consisting of a differential-to-single-ended conversion stage and four tapered logic inverters (MOSFET widths increasing in successive stages) for driving an output pin. The additional gain provided by the output circuitry lowers the comparator walk compared to the walk present for the three-stage comparator alone.

The measured and SPICE-simulated propagation-delay and walk for the three-stage comparator are given in Table 5-3 for single-ended input pulses of equal underdrive and overdrive having a rise-time of 1 ns. BSIM (level-4) MOSFET SPICE modeling was used with extracted parameters from the comparator fabrication run.

Measured and SPICE-simulated values of comparator propagation delay (Table 5-3) are within 10% of each other indicating good SPICE-simulation accuracy. Both the measured propagation delay and walk are higher than simulated values. The measured comparator walk is 540 ps compared to simulated walk of 330 ps for input-signal amplitudes of 10 - 1000 mV. Most of the increase in measured walk compared to simulated walk is due to a 140-ps and 260-ps decrease in measured propagation delay for input signals between 20 - 50 mV and 500 - 1000 mV, respectively. As mentioned earlier, comparator time walk is reduced for differential input signals compared to single-ended input signals which were

Table 5-3. Measured and SPICE-Simulated Propagation Delay and Walk for a Three-Stage CMOS Comparator.

Input-Signal Level (mV)	SPICE t_{prop} (ns)	Measured t_{prop} (ns)
10	11.00	11.73
20	10.78	11.61
50	10.71	11.47
100	10.77	11.53
200	10.80	11.61
500	10.83	11.45
1000	10.67	11.19
Walk: 10 - 1000 mV	0.33	0.54
Walk: 20 - 1000 mV	0.16	0.42
Walk: 50 - 500 mV	0.12	0.16
Input signal: -V to +V with 1-ns rise time. t_{prop} measured when output reaches 2 V. Output load capacitance is 10 pF.		

considered here. Differential input signals will be used to evaluate the constant-fraction comparator used in the CMOS CFD.

Design of the Constant-Fraction Comparator

A five-stage comparator circuit based on the MOSFET ohmic-load stage of Figure 5-16 was used for the CMOS CFD constant-fraction comparator. A limiting voltage of 1.5 V and a differential-pair MOSFET channel width of 50 μ (the channel length is 2 μ) was selected based on the walk performance described earlier for the four-stage comparator. A fifth stage was added to the constant-fraction comparator to reduce walk due to gain and gain-bandwidth limitations. A schematic diagram of the constant-fraction comparator is shown in Figure 5-20.

In the constant-fraction comparator (Figure 5-20), triple cascode current sources are used instead of double cascode current sources used in the MOSFET ohmic-load stage of Figure 5-16. All current sources used in the constant-fraction comparator are connected to V_{ss} (-5.2 V) to avoid the extra biasing circuitry required if the source-follower current sources were connected to ground. This increases total power consumption to 13.8 mW (1.35 mA at +5 V and -5.2 V) from a level of 9.64 mW that would be required if the source-follower current sources were connected to ground. Since the current sources are connected to V_{ss}, triple cascode sources are required to limit the drain-source voltage (V_{DS}) of current-source MOSFETs. The use of voltages above 5 V (for NMOS devices with drawn gate lengths of 2 μ) could result in long-term hot-electron degradation and possible "snap-back" parasitic breakdown.

The ohmic MOSFET loads in the constant-fraction comparator (Figure 5-20) are tuned to values of 15 kΩ using the CMOS CFD process tuning circuit previously described (subcircuit *X12* in Figure 5-5). The load resistance of 15 kΩ gives the 1.5-V limiting voltage for the differential-pair current of 100 μA. The interstage source followers in the CFD operate at currents of 50 μA whereas the output source followers operate at currents of 200 μA. Higher bias currents are required in the output source followers to permit driving the 200-FF load capacitance present due to long (2000 μ x 4 μ) integrated-circuit metal traces. Long traces are required to connect the comparator output to both source-coupled logic and saturating-logic arming circuits. The output source followers contain both a direct output and a level-shifted output, the direct output connecting to source-coupled logic circuitry and the level-shifted output connecting to saturating-logic circuitry. A differential pair (consisting of MOSFETs M88 and M89) is included to provide a monitoring output for the constant-fraction comparator. This output permits external observation of CFD walk adjustment.

In Figure 5-21, SPICE-simulated interstage and output signals are shown for the constant-fraction comparator. Additionally, the input signal is shown which models the photomultiplier, front-end amplifier, and CFD shaping circuit as described in the preceding multistage comparator analysis. The input signal is applied differentially with a common-mode voltage of +2.5 V to represent the signal coming from the CFD continuous-time filter. SPICE simulation was done using BSIM (level 4) modeling with full post-layout interconnection capacitances. Additionally, a load capacitance of 200 FF was connected to each output to model the previously mentioned interconnection capacitance associated with

long output traces connecting to the source-coupled logic and saturating logic arming circuits.

The SPICE-simulated output zero-crossing propagation delay for each constant-fraction-comparator stage (Figure 5-21) is approximately 1.5 ns. The total output zero-crossing propagation delay is approximately 8.1 ns for the direct output (V_{out1}) and 8.7 ns for the level-shifted output (V_{out2}). This propagation delay is comparable to the "less than 10 ns" delay reported for a 1.6-μ CMOS ac-coupled three-stage comparator using MOSFET diode-connected loads [63]. Additionally, the CFD propagation delay is nearly half that of the typical delay (16.9 ns) specified for a commercial 2-μ CMOS high-speed comparator cell [44].

SPICE-simulated walk performance is shown in Figure 5-22 for the constant-fraction comparator. The representative CFD signal used for comparator simulations of Figure 5-21 was used for walk simulations. The simulated walk performance is 175 ps over the full 10 - 2000 mV input range, 158 ps over an input range of 10 - 1000 mV, and 76 ps over an input range of 100 - 1000 mV. The simulated walk of 158 ps for input-signal amplitudes of 10 - 1000 mV is somewhat lower than the measured walk of 210 ps (AD9685 [39]) and 250 ps (VC 7695 [21]) for high-speed bipolar ECL comparators [38]. The effects of constant-fraction comparator walk on CMOS CFD timing performance will be considered later.

It is interesting to note that the constant-fraction-comparator propagation delay *increases* (Figure 5-22) with increasing signal level. As mentioned earlier, increasing propagation delay with increasing signal level is in conflict with the comparator charge-sensitivity model. Walk performance for the constant-fraction comparator is dominated by circuit limiting (nonlinearity) effects since a linear comparator model would predict decreasing propagation delay with increasing signal level.

SPICE-simulated small-signal frequency response is shown in Figure 5-23 for each constant-fraction comparator stage. The single-stage gain is approximately four and the total comparator gain is approximately 1,024 which agrees well with calculated values of 4.308 and 1,485 using Equation 5-10. The total gain-bandwidth product, defined as the gain multiplied by the -3-dB bandwidth, is equal to 680 MHz (4 x 170 MHz) for a single stage and 61.4 GHz (1,024 x 60 MHz) for the total comparator. The single-stage gain-bandwidth product of 680 MHz is comparable to the value of 500 MHz reported for a three-stage 1.6-μ CMOS ac-coupled comparator with diode-connected MOSFET loads [63].

SPICE-simulated wideband input noise for the constant-fraction comparator is 70 μV rms. As described for the continuous-time filter, the commercial SPICE program used does not consider the noise associated with ohmic-region MOSFETs, but this noise component is

expected to be negligible compared to input noise of differential-pair MOSFETs. Also, as described for the continuous-time filter, a noise level of two times the SPICE-simulated value will be used to model MOSFET noise in excess of the simple transconductance noise model. The estimated comparator input noise is then 140 μV rms, which is negligible when compared (in an uncorrelated sense) with the estimated 3200 μV rms output noise of the continuous-time filter. As a result, the comparator input noise does not affect timing jitter for the CMOS CFD.

CFD Arming Logic Circuits

Two independent sets of arming-logic circuits are included in the CMOS CFD (Figure 5-5): traditional saturating CMOS-logic circuits (subcircuits *X9* - *X11*) and specially-designed linear CMOS-logic circuits (subcircuits *X6* - *X8*). As mentioned, the specially-designed linear CMOS-logic circuits consists of source-coupled logic circuitry having topology similar to bipolar ECL logic circuitry. Like ECL circuits, these circuits operate by switching constant currents into resistive or MOSFET diode-connected loads and use source-follower devices as output devices. Although considerably more complex than traditional saturating CMOS-logic circuits, the source-coupled CMOS logic circuits introduce much less power-supply noise (approximately two-orders of magnitude less [67]) and are more easily interfaced to linear circuits because of the use of small logic swings (e.g., 1.5-V is used in the CMOS CFD). Source-coupled CMOS logic circuits have been evaluated by Maskai, Kiaei, and Allstot [67] and Binkley [68].

Both the saturating and source-coupled arming-logic circuits include combinational logic, high-performance D flip-flops, and output-pin drivers. The arming logic circuits are configurable (through the assignment of three mode input pins) for the traditional arming or slow-rise-time reject arming configurations shown in Figure 5-1 (page 226).

The high-performance D flip-flops (both the saturating logic and source-coupled logic circuit) have been designed for minimum change in propagation delay or walk as a function of changing flip-flop setup time. This is analogous to design for minimum flip-flop metastability where the window of setup times resulting in increased flip-flop propagation delay is minimized. In CFD arming applications, operating flip-flop setup time changes with event energy, the setup time being minimum for those events with signal levels slightly above the arming threshold.

The saturating-logic D flip-flop is based on a previously reported master/slave cascode design optimized for minimum metastability [69]. The source-coupled D flip-flop is based on a master/slave design having similar topology to ECL D flip-flops [68]. MOSFET device

sizes were chosen for each flip-flop design through the use of a computer program that evaluated propagation delay walk as a function of setup time for various device sizes.

SPICE-simulated propagation delay walk for the saturating D flip-flop is approximately +500 ps for setup times ranging from 2.2 - 1.7 ns and is nearly zero for setup times greater than 2.2 ns. SPICE-simulated propagation delay walk for the source-coupled D flip-flop is approximately +600 ps for setup times ranging from 0.8 - 0.3 ns and is nearly zero for setup times greater than 0.8 ns. Setup times for both flip-flops were varied up from 100 ps above the setup-time threshold (the threshold of flip-flop operation). As true for all CMOS CFD SPICE simulations, post-layout parasitic capacitances were included in the simulations, and simulations were run using a set of extracted BSIM parameters that are believed to be nominal for the process (extracted BSIM parameters were not available for the CMOS CFD fabrication run). The effect of arming flip-flop propagation-delay walk on CMOS CFD timing performance will be considered later.

Estimation of CMOS CFD Walk

CMOS CFD time walk is controlled by walk contributions from the continuous-time filter (CFD shaping circuit), constant-fraction comparator, and arming flip-flop. The SPICE-simulated continuous-time filter walk (previously given) is +15 ps, +15 ps, and +80 ps for CFD input signals ranging from 100 - 1000 mV, 10 - 1000 mV, and 10 - 2000 mV with rise-times (10 - 90%) of 10 ns. The SPICE-simulated constant-fraction comparator walk (previously given) is +76 ps, +158 ps, and +175 ps for the same CFD input-signal ranges. The walk contributions of the continuous-time filter and the constant-fraction comparator add, giving a composite walk of +91 ps, +173 ps, and +255 ps for the CFD input-signal ranges considered.

As described earlier, propagation-delay walk of D flip-flops used in CFD arming circuits contributes to CFD walk. It is necessary, however, to ascertain the flip-flop setup times resulting from given CFD input-signal levels in order to evaluate flip-flop walk. The SPICE-simulated propagation-delay walk (previously given) is +500 ps for setup times ranging from 2.2 - 1.7 ns for the CMOS CFD saturating-logic flip-flop and +600 ps for setup times ranging from 0.8 - 0.3 ns for the CMOS CFD source-coupled logic flip-flop. The flip-flop propagation-delay walk is essentially zero for CFD input signals sufficiently above the arming threshold since flip-flop setup times would be greater than the setup times specified that result in propagation-delay walk. It is interesting to note that CMOS CFD flip-flop propagation-delay walk actually *decreases* with increasing CFD input signal level because the resulting flip-flop setup time increases. The flip-flop propagation-delay walk could then be expected

to partially cancel the increasing propagation delay associated with the continuous-time filter and constant-fraction comparator. For evaluation of the CMOS CFD, it will be assumed that CFD input signals sufficiently exceed the arming threshold, resulting in no walk cancellation from the arming flip-flop.

The estimated CMOS CFD walk (from the continuous-time filter and constant-fraction comparator) is +91 ps for 100 - 1000 mV input signals with rise-times (10 - 90%) of 10 ns. The corresponding propagation-delay slope is +101 ps/V, which can be multiplied by the input-voltage resolution of the CMOS CFD to estimate the timing resolution resulting from walk errors (Equation 2-19, page 26). Assuming a CFD input photopeak voltage of 0.8 V with a Gaussian resolution of 14% FWHM, the resulting timing resolution due to walk errors is 11.3 ps FWHM. This level of timing error is, of course, totally negligible compared to the BGO/photomultiplier detector statistical resolution of approximately 3 ns FWHM.

Although walk errors for the CMOS CFD are negligible for the BGO/photomultiplier detector application considered, walk errors may be significant for subnanosecond timing resolution systems. The effects of CFD walk errors can be considered for such systems by including walk effects in Monte Carlo simulations of timing resolution. In particular, the setup time of a D flip-flop used for CFD arming can be evaluated for each simulated event and mapped to a corresponding flip-flop propagation delay. Similarly, constant-fraction comparator underdrive, zero-crossing slope, and overdrive can be evaluated for each simulated event and mapped to a corresponding propagation delay. The inclusion of CFD walk errors in Monte Carlo timing simulations would address effects that are difficult to evaluate analytically, such as correlation effects between event energy and CFD walk.

Estimation of CMOS CFD Timing Jitter

The output noise of the CMOS CFD continuous-time filter combines with the input noise of the constant-fraction comparator giving rise to timing jitter when the constant-fraction comparator senses the zero crossing of the CFD shaping signal. The total shaping-signal noise is 3,203 μV rms which is the uncorrelated combination of the continuous-time filter output noise (previously given as 3,200 μV rms) and the constant-fraction comparator input noise (previously given as 140 μV rms).

CMOS CFD timing jitter is found by dividing the CFD shaping-signal noise by the shaping-signal zero-crossing slope (Equation 2-20, page 27). The resulting timing jitter is 70 ps rms or 164 ps FWHM for a shaping-signal noise of 3,200 μV and a shaping-signal zero-crossing slope of 46 mV/ns (Figure 5-8) resulting from a 1-V CMOS CFD input with a 10-ns rise-time. The CMOS CFD timing jitter of 164 ps FWHM is negligible when combined in an

uncorrelated sense with the BGO/photomultiplier statistical timing resolution of approximately 3 ns FWHM.

Monte Carlo Simulations of CMOS CFD Energy-Discrimination and Timing Performance

Monte Carlo simulation of CFD energy-discrimination and timing performance was illustrated in *Section 4,* and an example was given for a delay-line CFD. Monte Carlo simulations will be performed for the CMOS CFD using the same BGO-scintillator, photomultiplier, and front-end amplifier characteristics previously used (Figure 4-21, page 166). The CFD shaping-signal and arming-signal impulse responses used in the Monte Carlo simulation were found from post-layout SPICE simulations. As mentioned earlier, a nominal set of BSIM MOSFET parameters was used for all CMOS CFD simulations.

Performance without Compton Scatter

Compton scatter was not considered in the first Monte Carlo simulation in order to evaluate the slight degradation in timing resolution caused by Compton scatter. A Gaussian energy spectrum with photopeak energy of 511 keV and resolution of 14% FWHM, representative of the energy resolution for BGO block detectors used in CTI/Siemens commercial PET systems [19], was used in the simulation. All detector events were collected in the Monte Carlo simulation as energy discrimination was not used since Compton scatter was not present.

The Monte Carlo simulated timing spectrum is shown in Figure 5-24. The timing resolution is 3.28 ns FWHM and 6.63 ns FWTM which is comparable to the measured resolution of 3.30 ns FWHM and 6.40 ns FWTM for the commercial delay-line CFD given in Figure 4-32 (page 173). The commercial delay-line CFD measurements were made with the low level of Compton scatter present from a 1 x 1 x 1 inch BGO crystal excited by 511-keV gamma rays from a ^{22}Na point source.

Performance with Low-Level Compton Scatter

The next Monte Carlo simulations were performed for the low level of Compton scatter present for a 1 x 1 x 1 inch BGO crystal excited by 511-keV gamma rays from a ^{22}Na point source. This BGO crystal and source were used for experimental measurements for both the delay-line CFD and the CMOS CFD. A detector energy resolution of 14% and a scatter fraction of 0% were used in the simulations, which closely model the energy resolution and Compton scatter for the BGO crystal and source. CFD energy-discrimination performance was considered, and an energy threshold of 200 keV (as observed by the intersection of the accepted and rejected energy spectra) was used for all simulations. Simulations were

performed with and without the optional 10 ns constant-fraction comparator delay discussed in *Section 4*. This optional delay improves the statistical arming performance of the CFD, resulting in less rejection of valid photopeak events and better rejection of low-energy Compton scatter.

The total-, accepted-, and rejected-event energy spectra are shown in Figure 5-25 for the CMOS CFD with no optional constant-fraction comparator delay. The 511-keV photopeak loss in the accepted spectrum is 2.5%, which would correspond to a coincidence loss of nearly twice this (5%) in a PET application. The timing spectrum corresponding to accepted CFD events is shown in Figure 5-26. The Monte Carlo timing resolution of 3.43 ns FWHM and 6.69 ns FWTM is comparable to the measured resolution of 3.30 ns FWHM and 6.40 ns FWTM for the commercial delay-line CFD given in Figure 4-34 (page 173). As mentioned, the commercial CFD measurements were made using the low scatter and approximate 14% energy resolution of the 1 x 1 x 1 inch BGO crystal excited by 511-keV gamma rays from a ^{22}Na point source. The measured total-event energy spectrum for the commercial CFD (Figure 4-33, page 172) has comparable Compton scatter (neglecting the backscatter peak) and energy resolution as the simulated total energy spectrum shown in Figure 5-25.

The total-, accepted-, and rejected-event energy spectra are shown in Figure 5-27 for the CMOS CFD with the optional 10-ns constant-fraction comparator delay. The 511-keV photopeak loss in the accepted spectrum is only 0.5%, which is considerably lower than the loss of 2.5% simulated without the optional delay. In PET applications, the coincidence loss would be nearly 1% and 5% respectively with and without the optional delay, indicating an advantage for the better CFD arming performance available with the optional delay. The timing spectrum corresponding to accepted CFD events (using the optional delay) is shown in Figure 5-28. The Monte Carlo timing resolution is 3.45 ns FWHM and 6.71 ns FWTM, which is unchanged within statistical-simulation errors from timing resolution of 3.43 ns FWHM and 6.69 ns FWTM (Figure 5-26) for the case without the optional delay.

Performance with High-Level Compton Scatter

The final Monte Carlo simulations were performed for the high level of Compton scatter present from a 20-cm diameter, cylindrical, uniform radiation phantom filled with water. The scatter from this phantom approximates scatter from a patient being imaged in PET. A detector energy resolution of 14% and a scatter fraction of 32% was used in the simulations to model the energy resolution and Compton scatter observed in commercial CTI/Siemens PET BGO block detectors [19]. As chosen for the low-level Compton scatter simulations, a CFD energy threshold of 200 keV was used. Although experimental measurements were

not made for the case of high-level Compton scatter, Monte Carlo simulations give an indication of the degradation in timing resolution present for a high-level of scatter compared to a low-level of scatter (where experimental measurements were made).

The total-, accepted-, and rejected-event energy spectra are shown in Figure 5-29 for the CMOS CFD with the optional 10-ns constant-fraction comparator delay. The 511-keV photopeak loss in the accepted spectrum is only 0.4%, which is comparable to the loss seen for the low-scatter case (Figure 5-27). The timing spectrum corresponding to accepted CFD events (corresponding to Figure 5-29) is shown in Figure 5-30. The Monte Carlo timing resolution is 3.64 ns FWHM and 7.12 ns FWTM, which is approximately 5.5% above the low-scatter timing resolution of 3.45 ns FWHM and 6.71 ns FWTM (Figure 5-28) and 11% above the no-scatter timing resolution of 3.28 ns FWHM and 6.63 ns FWTM (Figure 5-24).

Compton scatter increases the timing resolution by lowering the mean detected-event energy. As discussed in *Section 3*, Poisson timing resolution goes inversely with photoelectron rate, which directly tracks energy deposition in the scintillation detector.

Measured Performance of the Fully-Monolithic CMOS CFD

Measured Timing Walk and Jitter

Time walk for the CMOS CFD was measured using input pulses having a 10-ns rise-time (10 - 90%). The measured walk was -255 ps for input signals ranging from 100 - 1000 mV compared to a SPICE-simulated walk of +91 ps given earlier. The measured propagation delay decreased with increasing signal level (negative walk) whereas the SPICE-simulated propagation delay increased with increasing signal level (positive walk). Measured CMOS CFD walk for input signals ranging from 1000 - 2000 mV was positive, however, indicating that propagation delay increased with signal level for large input signals (as predicted by SPICE simulations).

Several sources of measurement and SPICE-simulation errors may explain the differences observed between measured and SPICE-simulated walk for the CMOS CFD. Measurement errors can result from a bipolar test circuit used to convert single-ended signals into differential signals to drive the CMOS CFD. Although this test circuit was designed with significant amounts of degeneration to minimize distortion, distortion and time walk was not evaluated for the test circuit. SPICE simulation errors could result from the fact that device mismatches were not considered in the CMOS CFD walk simulations. As mentioned earlier, device mismatches can significantly increase circuit distortion because of incomplete second-order distortion cancellation and incomplete third-order

distortion cancellation for the linearized transconductor used in the CMOS CFD continuous-time filter. Increased circuit distortion (nonlinearity) can result in increased time walk.

Although measured CMOS CFD time walk was approximately a factor of three higher than SPICE-simulated walk, the SPICE-simulated walk of +91 ps (for an input-signal range of 100 - 1000 mV) was found earlier to contribute only 11.3 ps FWHM of timing resolution error. Such walk errors would have to be significantly higher before affecting timing resolution for the BGO/photomultiplier detector application considered where detector statistical timing resolution is approximately 3 ns FWHM.

CMOS CFD timing jitter was measured for 1-V input pulses having a rise-time (10 - 90%) of 10 ns. The measured timing jitter is shown in Figure 5-31 and is 140 ps FWHM which is in good agreement with the previously given SPICE-simulated jitter of 164 ps FWHM. As mentioned earlier, timing jitter at this level is negligible for the BGO/photomultiplier detector application considered where detector statistical timing resolution is approximately 3 ns FWHM.

Measured Timing and Energy Performance for Low-Level Compton Scatter

Measured energy and timing spectra were taken using the prototype CMOS CFD. The measurements were made using a 1 x 1 x 1 inch BGO crystal coupled to a 1-inch photomultiplier, which was connected to a front-end amplifier. A ^{22}Na point source was used to provide 511-keV gamma rays. The BGO crystal, photomultiplier tube, and front-end amplifier have characteristics used in the Monte Carlo simulations, which are given in Figure 4-21 (page 166). The detector energy resolution and Compton scatter is near the 14% FWHM resolution and scatter fraction of 0% used in the low-scatter Monte Carlo simulations. A comparison of the total-event energy spectra will be given for both Monte Carlo simulations and experimental measurements. All measured CMOS CFD energy and timing spectra were made as described in the EG&G ORTEC application note, AN-42 [35], using a CFD energy threshold of 200 keV (also used for Monte Carlo simulations).

The measured total-, accepted-, and rejected-event energy spectra are shown in Figure 5-32 for the CMOS CFD configured without the optional constant-fraction comparator delay. The measured 511-keV photopeak loss is 3.6%, which is slightly above the 2.5% Monte Carlo simulated loss (Figure 5-25). The measured CFD timing spectrum, corresponding to the accepted-event energy spectrum, is shown in Figure 5-33. The measured timing resolution is 3.26 ns FWHM and 6.50 ns FWTM, which is comparable to the Monte Carlo timing resolution of 3.43 ns FWHM and 6.69 ns FWTM (Figure 5-26).

The measured total-, accepted-, and rejected-event energy spectra are shown in Figure 5-34 for the CMOS CFD configured with the optional 10-ns constant-fraction comparator delay. The measured 511-keV photopeak loss is 1.8%, which is one-half the measured photopeak loss of 3.6% (Figure 5-32) present without the optional constant-fraction comparator delay configured. The measured photopeak loss of 1.8% present with the optional constant-fraction comparator delay configured is somewhat above the 0.5% Monte Carlo simulated loss (Figure 5-27) for the same configuration. The measured photopeak loss, using the alternate source-coupled arming logic circuitry included in the CMOS CFD (the saturating-logic arming circuits were used for all measurements presented), was 0.44% which is in good agreement with the Monte Carlo simulated loss. It is possible that the saturating-logic circuits did not provide a full 10 ns of constant-fraction comparator delay compared to the source-coupled logic circuits, and this will be investigated before completion of the final PET front-end CMOS integrated circuit. The measured 1.8% photopeak loss, using the saturating-logic arming circuitry with the constant-fraction comparator delay included, is acceptable for the PET application considered.

The measured CFD timing spectrum for the optional constant-fraction delay configured, corresponding to the accepted-event energy spectrum shown in Figure 5-34, is shown in Figure 5-35. The measured timing resolution is 3.25 ns FWHM and 6.50 ns FWTM, which is essentially unchanged from the timing resolution of 3.26 ns FWHM and 6.50 ns FWTM (Figure 5-33) obtained without the optional delay configured. The Monte Carlo timing resolution was also essentially unchanged for the CMOS CFD configured with and without the optional delay configured (Figures 5-26 and 5-28).

The measured timing resolution for the CMOS CFD (Figures 5-33 and 5-35) is comparable to the measured timing resolution for the commercial delay-line CFD (Figure 4-34, page 173). The measured CMOS CFD timing resolution was 3.26 ns FWHM and 6.50 ns FWTM compared to the measured resolution for the delay-line CFD of 3.30 ns FWHM and 6.40 ns FWTM. A fully-monolithic CMOS CFD was successfully implemented having timing resolution comparable to existing, delay-line CFD circuits for the BGO/photomultiplier detector application considered.

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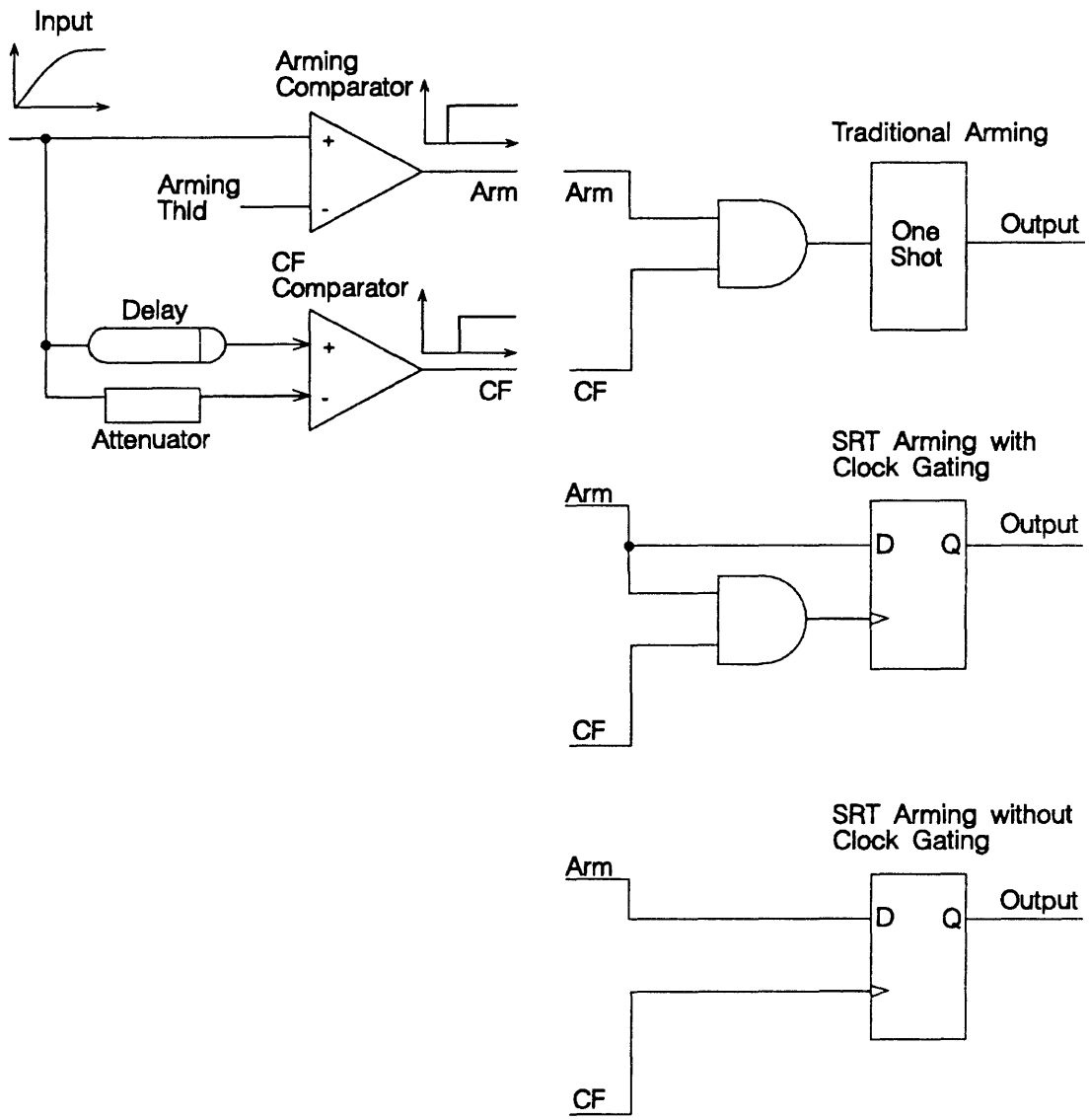


Figure 5-1. Block Diagram of Standard CFD Arming Circuits.

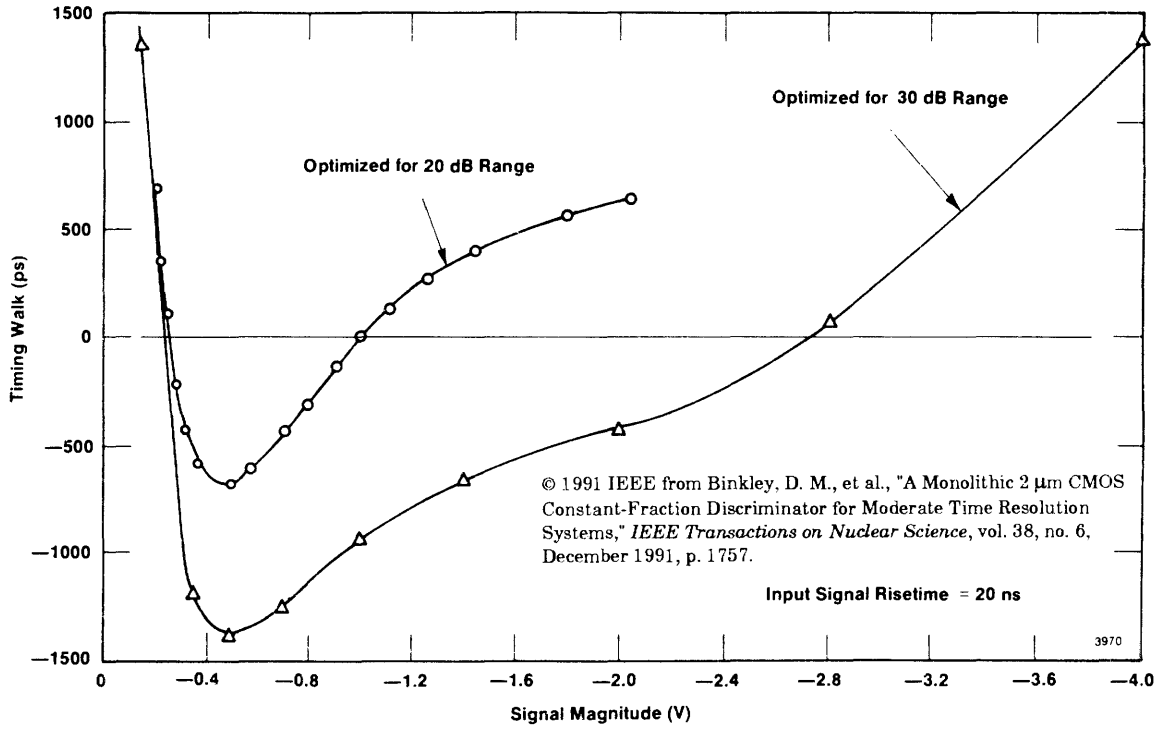


Figure 5-2. Measured Time Walk for the CMOS CFD Reported by Binkley et al.

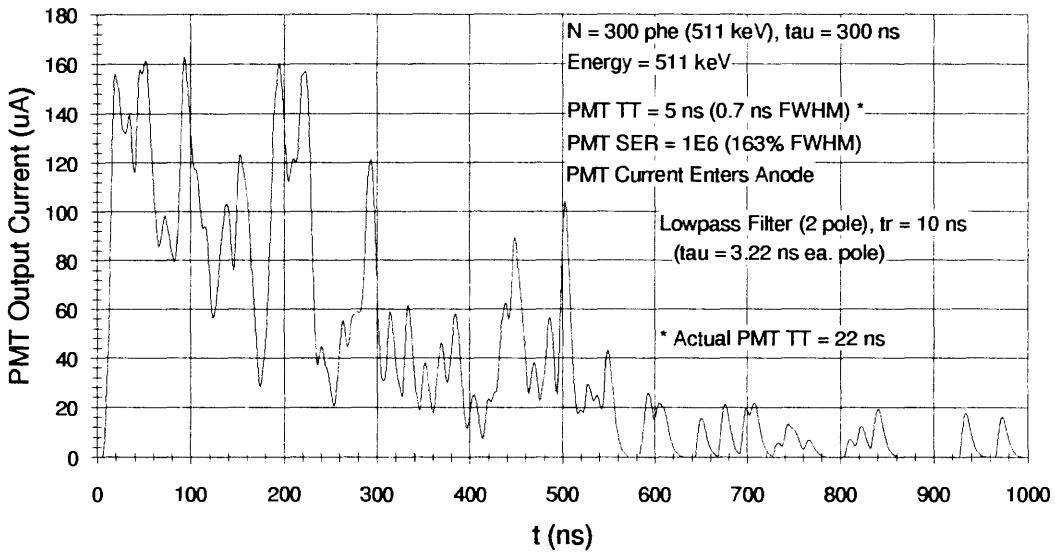


Figure 5-3. Illustration of Statistical Noise for BGO/Photomultiplier Scintillation Detector.

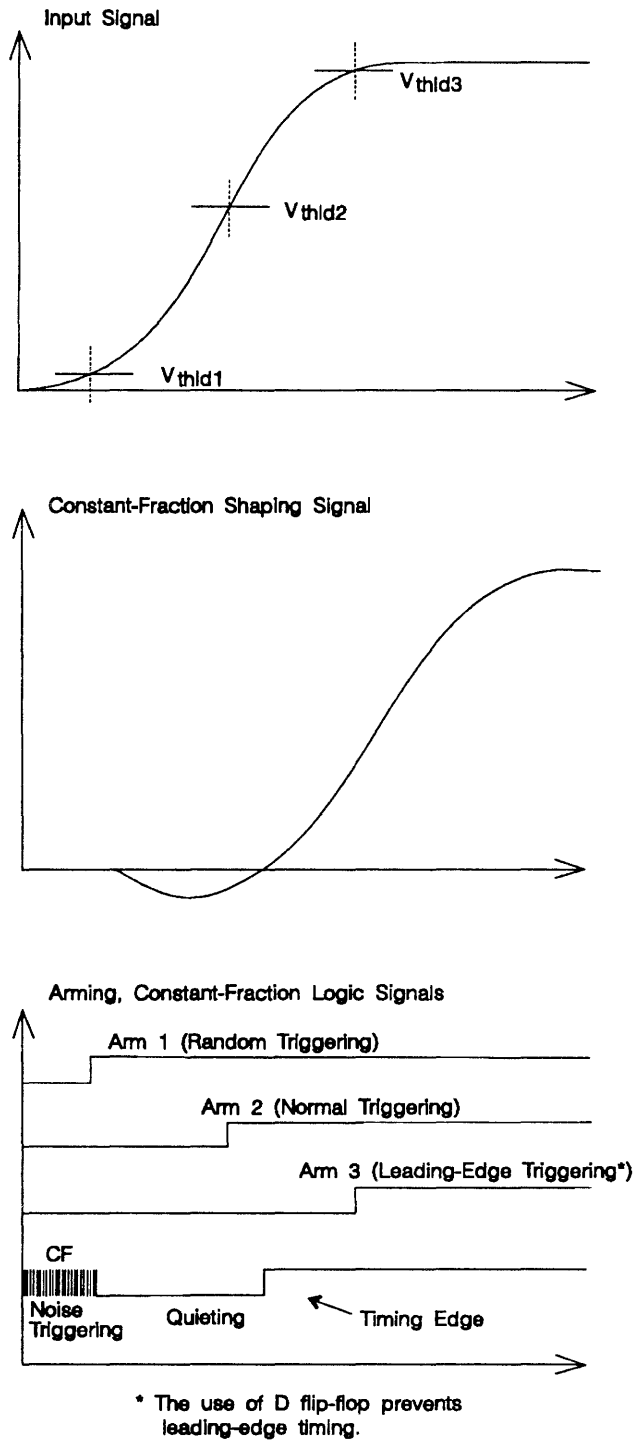


Figure 5-4. Illustration of CFD Arming Operation.

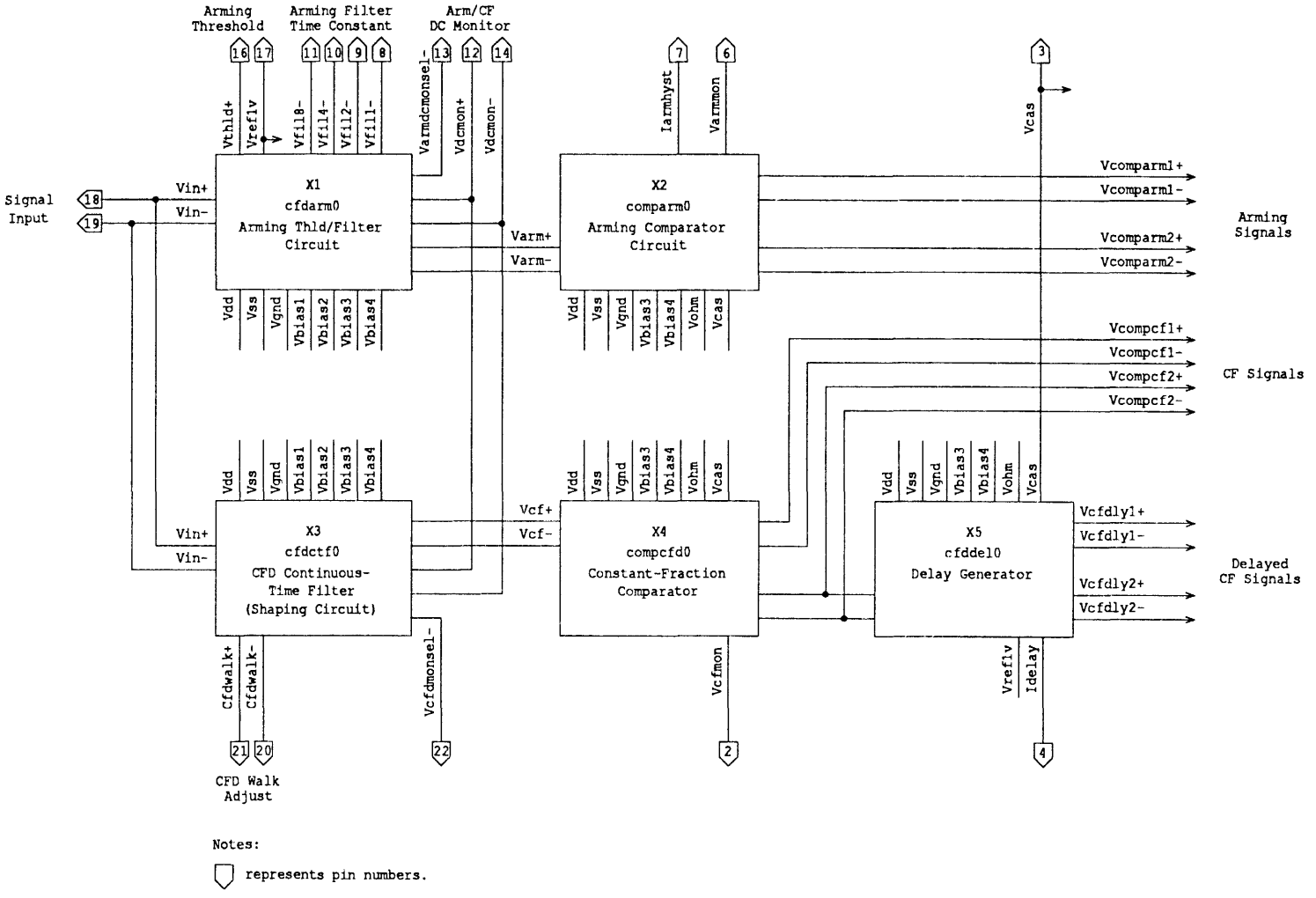
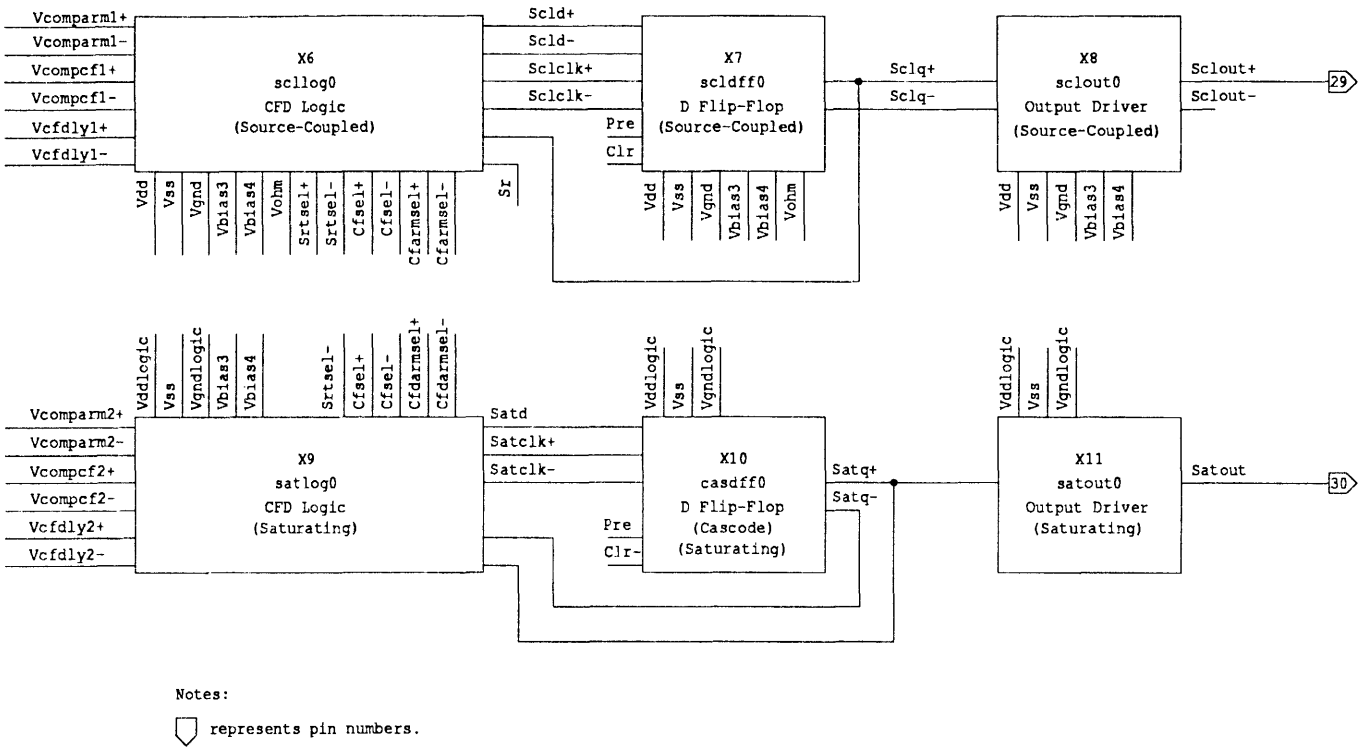


Figure 5-5. Top-Level Circuit Diagram for the CMOS CFD.



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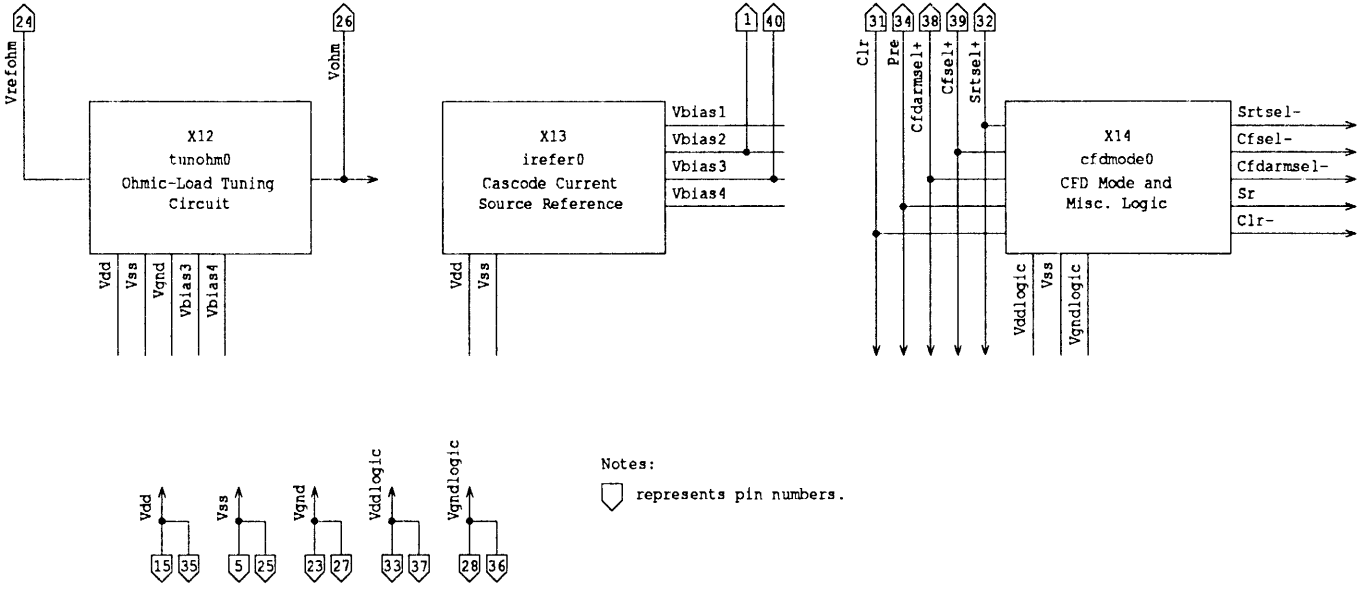

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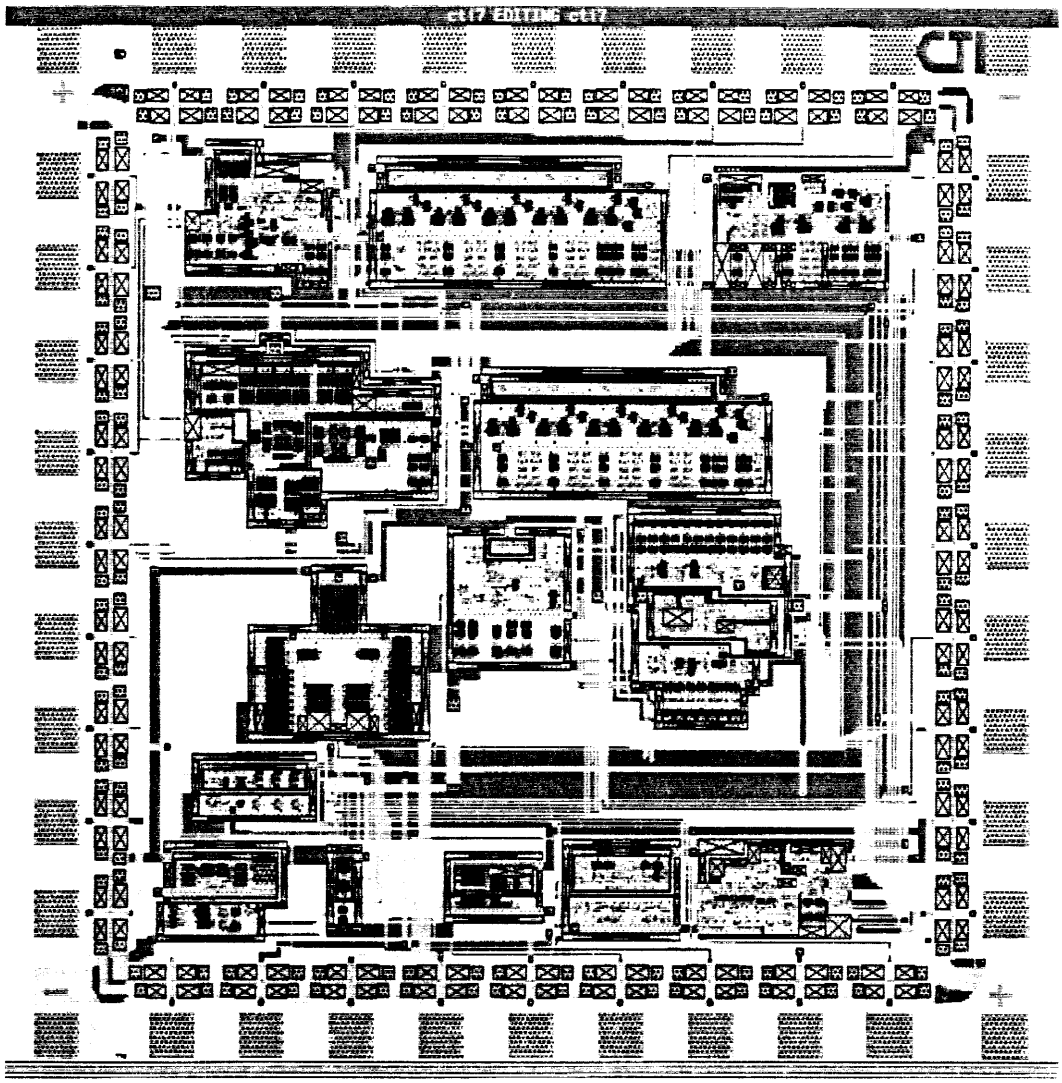


Figure 5-6. Integrated-Circuit Layout for the CMOS CFD.

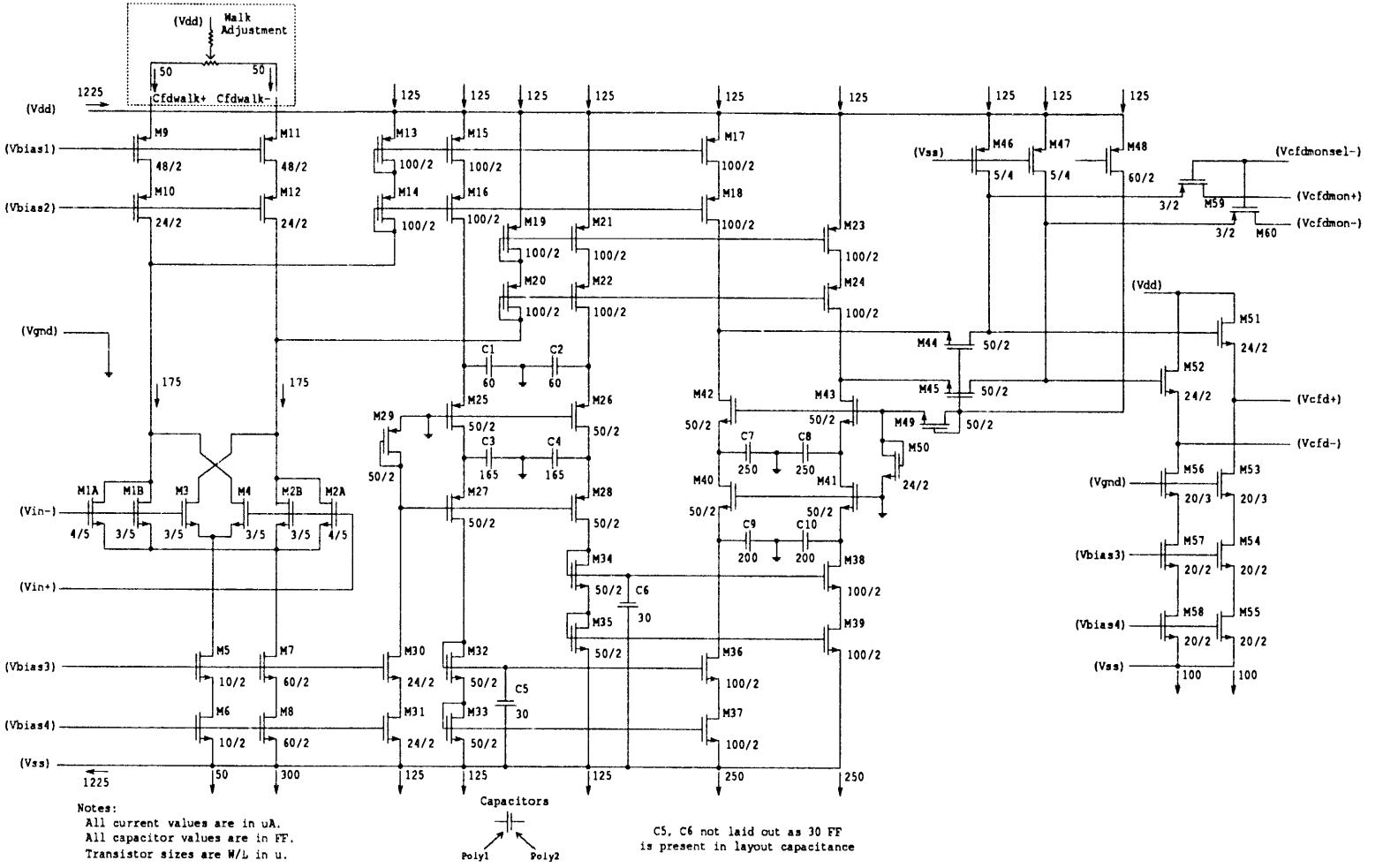


Figure 5-7. Schematic Diagram of the Binkley Gaussian CFD Continuous-Time Filter Used in the CMOS CFD.

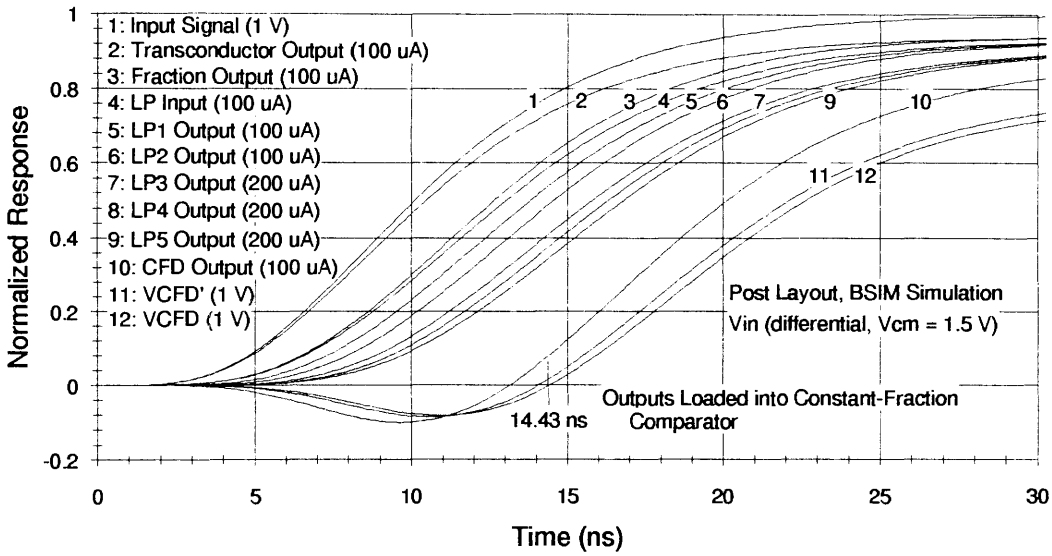


Figure 5-8. SPICE-Simulated Signals for the Binkley Gaussian CFD Continuous-Time Filter Used in the CMOS CFD.

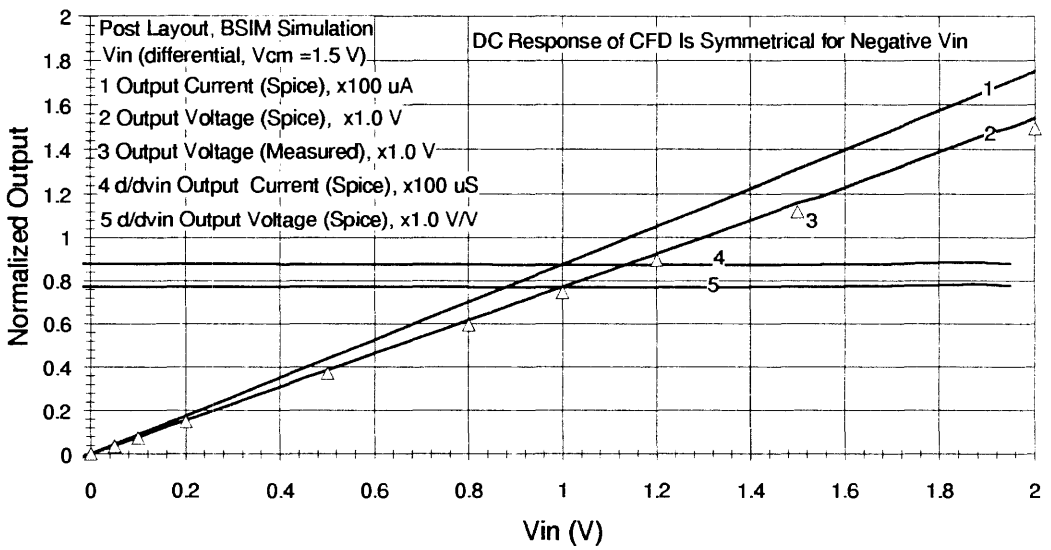


Figure 5-9. SPICE-Simulated DC Linearity for the Binkley Gaussian CFD Continuous-Time Filter Used in the CMOS CFD.

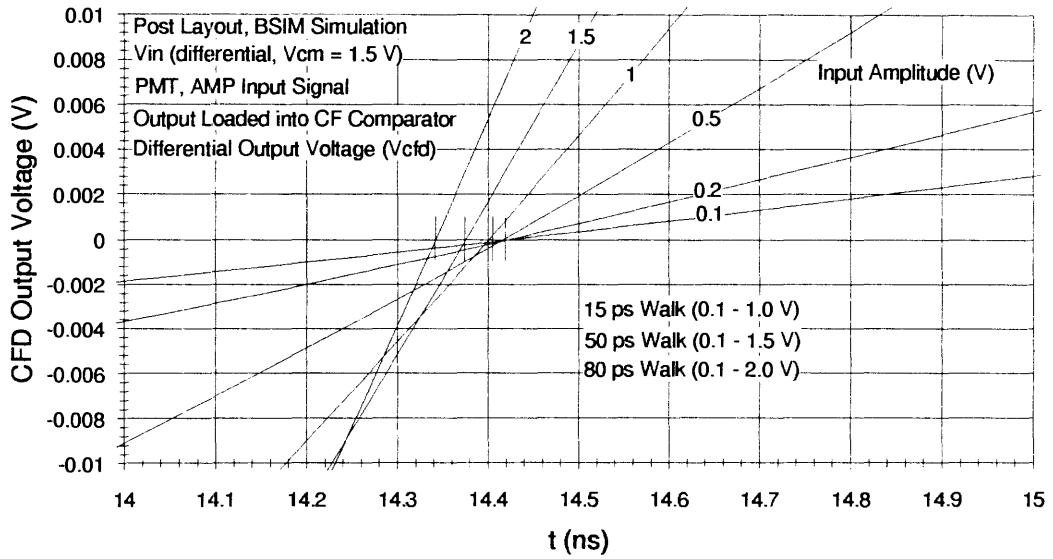


Figure 5-10. SPICE-Simulated Walk for the Binkley Gaussian CFD Continuous-Time Filter Used in the CMOS CFD.

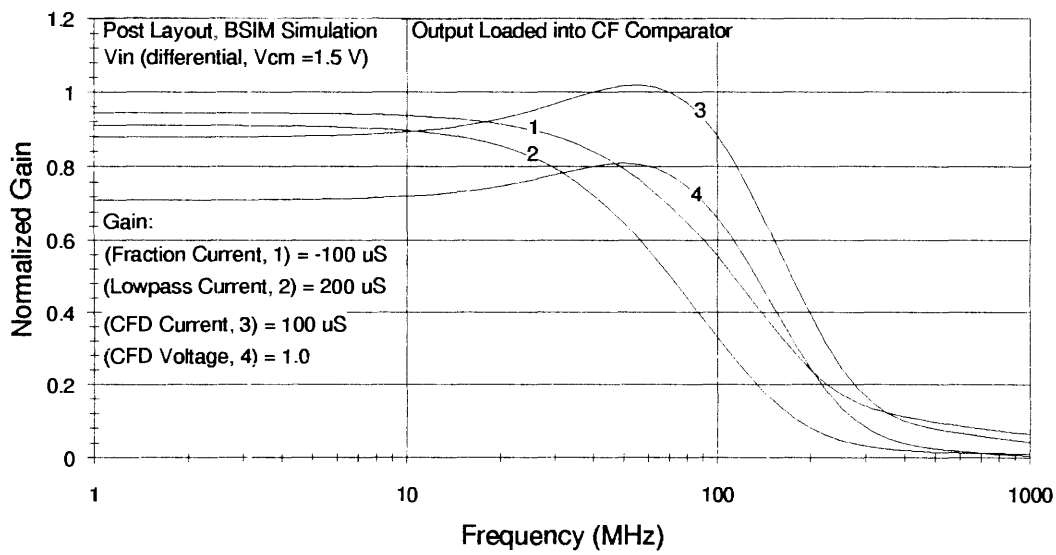


Figure 5-11. SPICE-Simulated Frequency Response for the Binkley Gaussian CFD Continuous-Time Filter Used in the CMOS CFD.

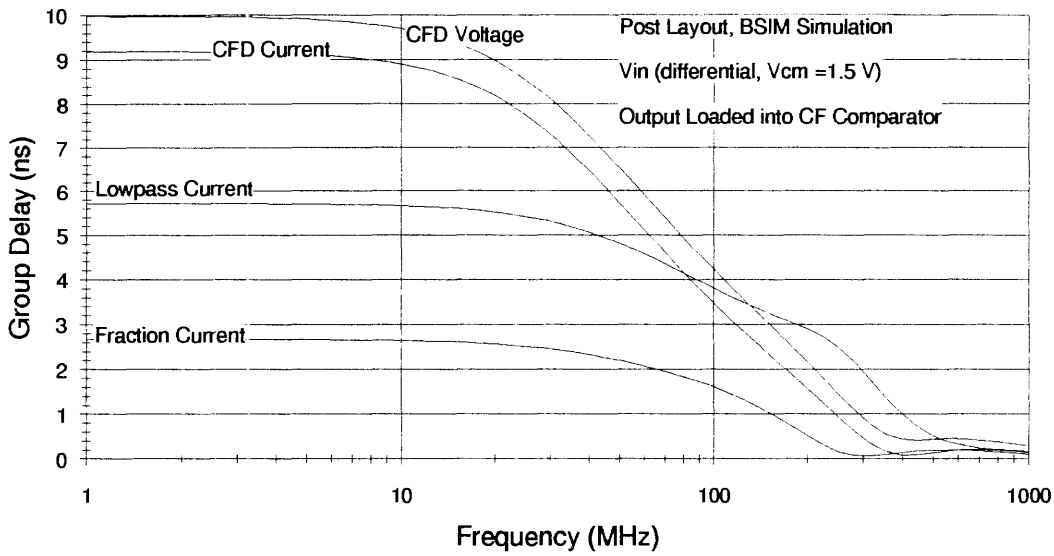
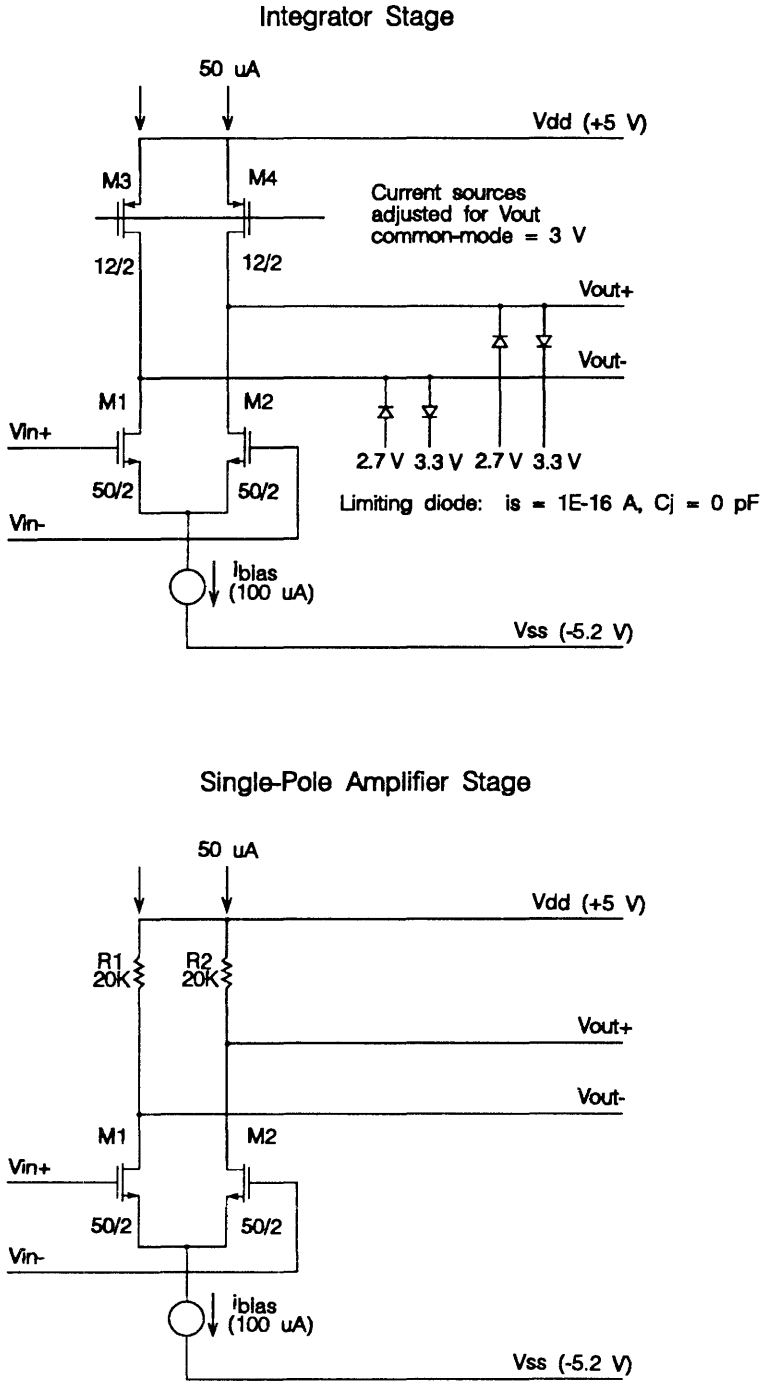


Figure 5-12. SPICE-Simulated Group Delay for the Binkley Gaussian CFD Continuous-Time Filter Used in the CMOS CFD.



Note: Transistor sizes are W/L in u.

Figure 5-13. Schematic Diagram of CMOS Integrator and Single-Pole-Amplifier Comparator Stages.

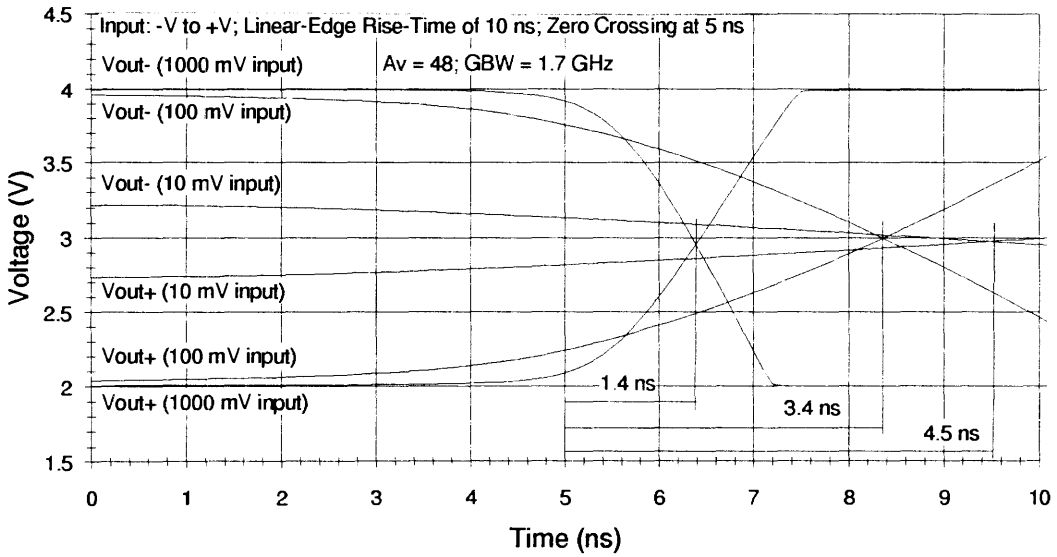


Figure 5-14. SPICE-Simulated Zero-Crossing Time of CMOS Integrator Comparator Stage.

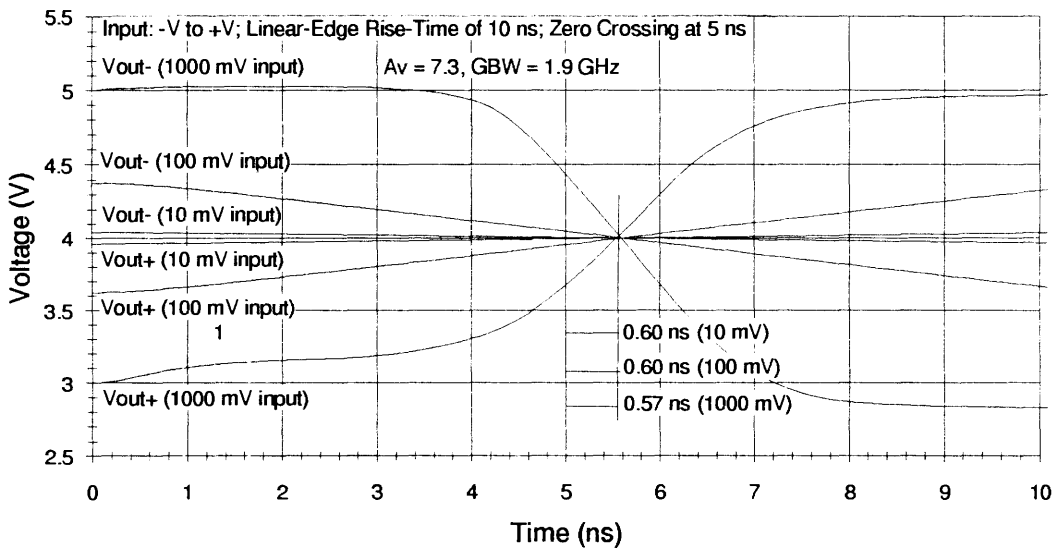
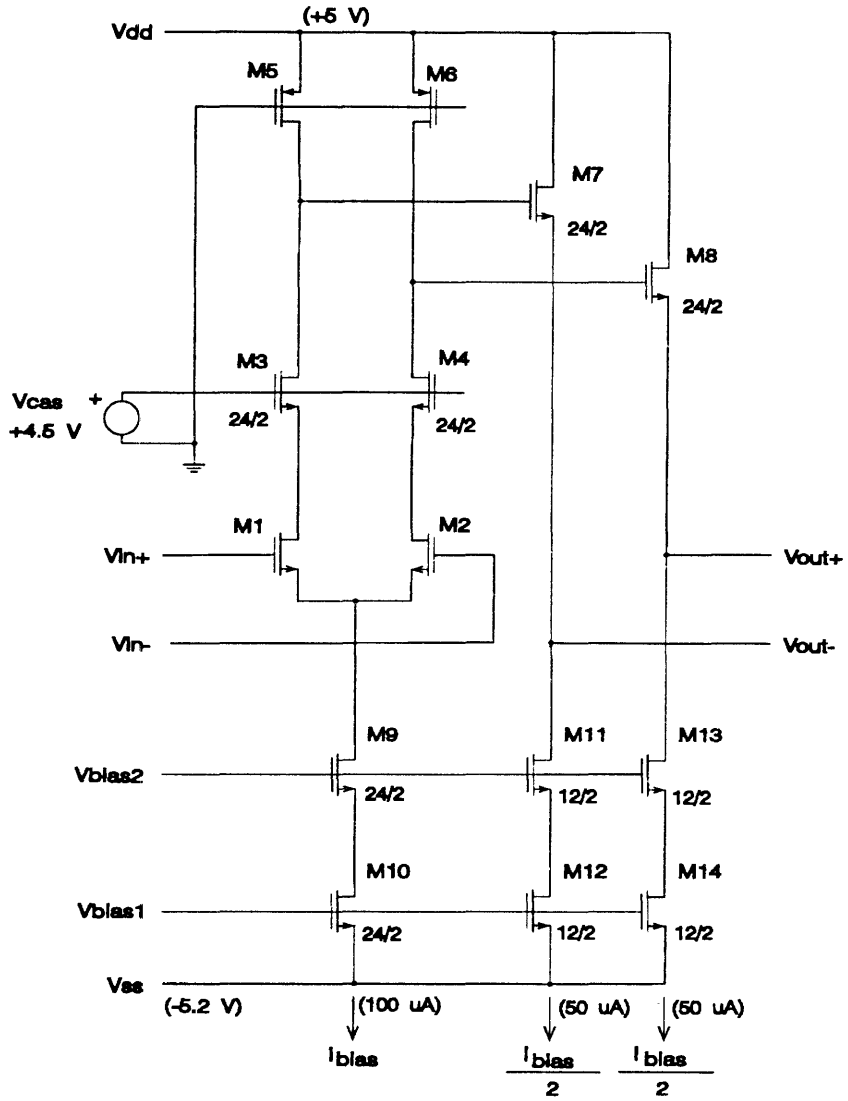


Figure 5-15. SPICE-Simulated Zero-Crossing Time of CMOS Single-Pole-Lowpass Comparator Stage.



M1, M2	24/2, 50/2, or 100/2
M5, M6	3/2 for Vlim = 1.1 V 4/3 for Vlim = 1.5 V, or 3/3 for Vlim = 2.2 V

Note: Transistor sizes are W/L in u.

Figure 5-16. Schematic Diagram of CMOS Comparator Stage with Ohmic-MOSFET Loads.

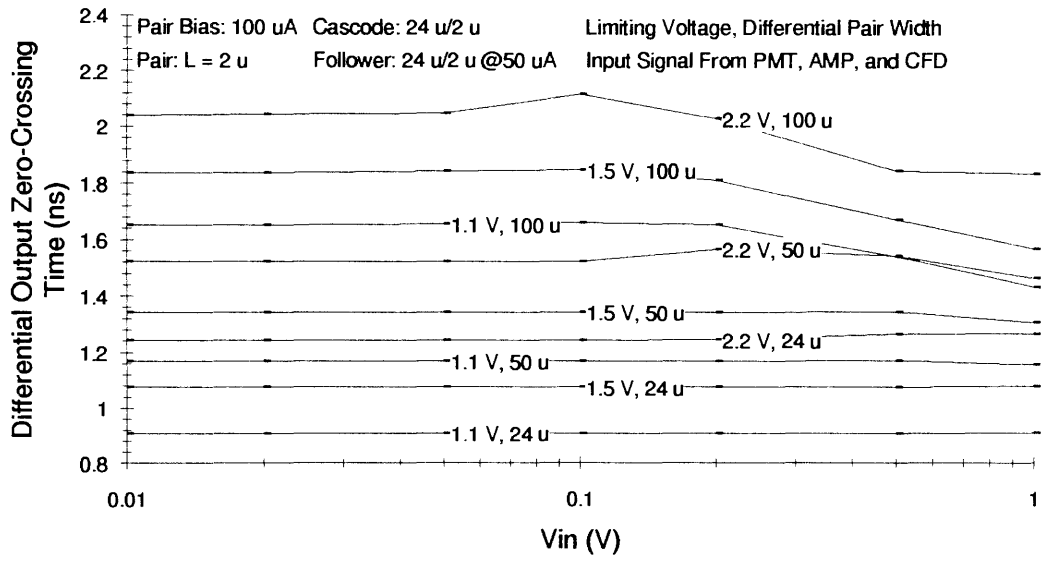


Figure 5-17. SPICE-Simulated Zero-Crossing Time at First-Stage Output for Multistage CMOS Comparator with Ohmic-MOSFET Loads.

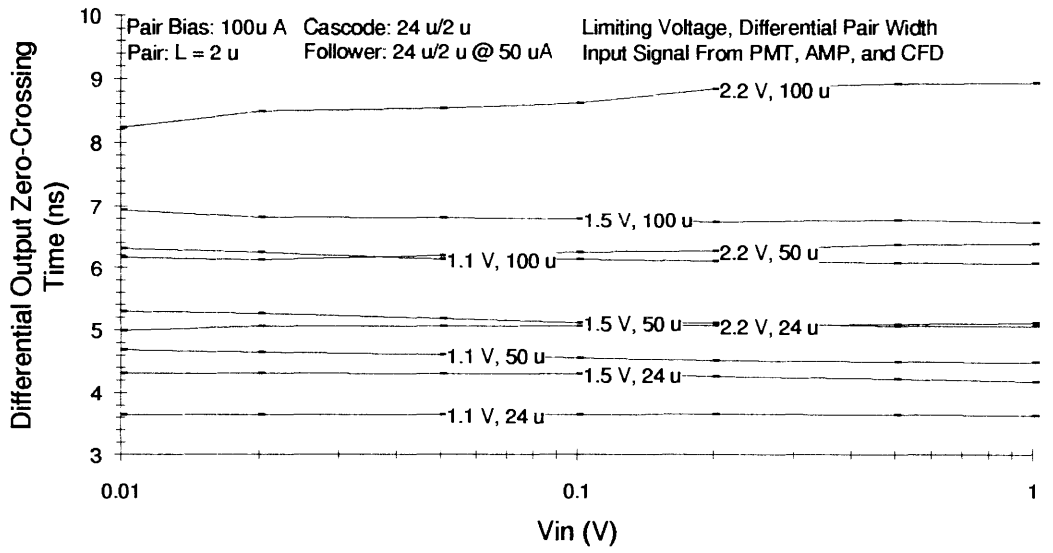


Figure 5-18. SPICE-Simulated Zero-Crossing Time at Fourth-Stage Output for Multistage CMOS Comparator with Ohmic-MOSFET Loads.

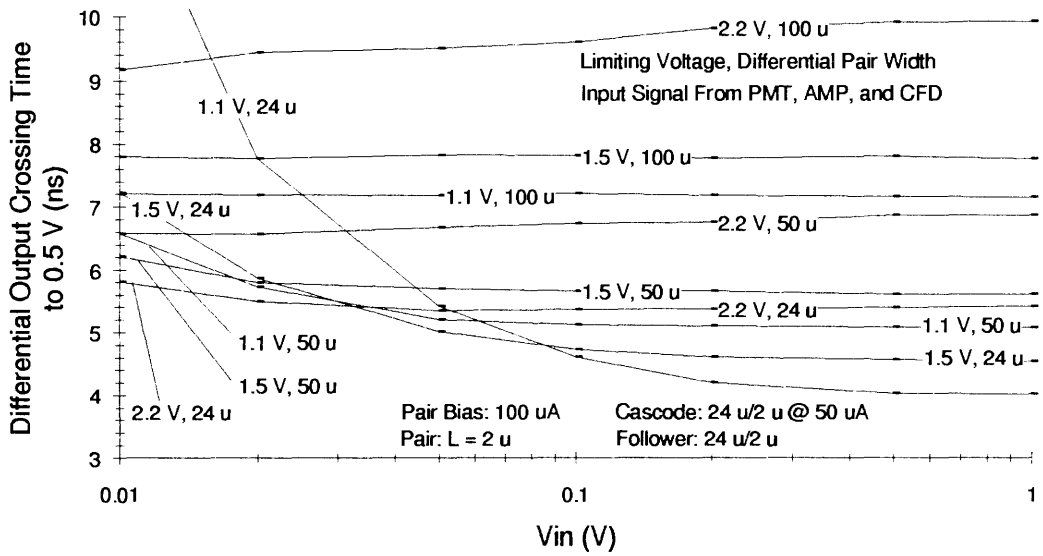
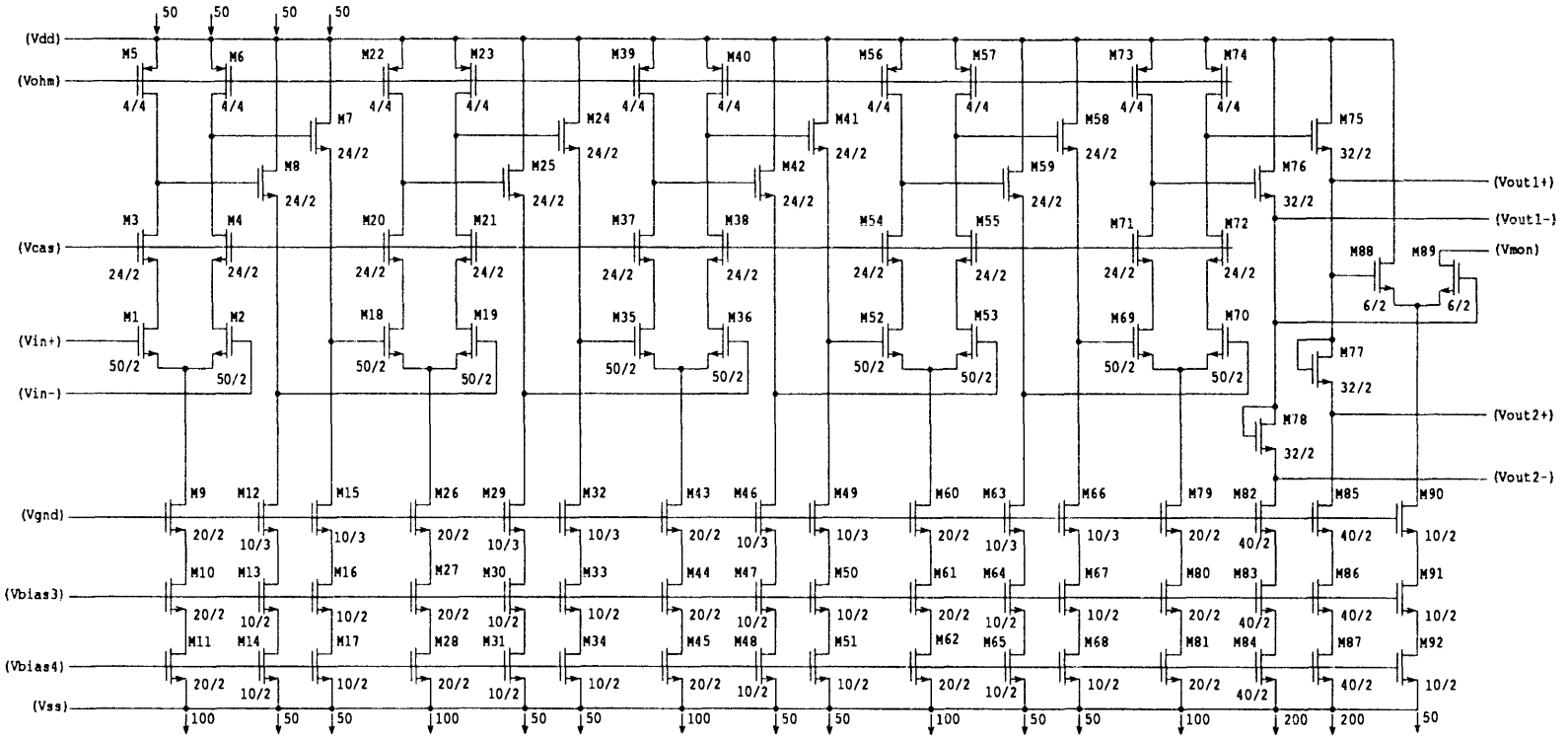


Figure 5-19. SPICE-Simulated 0.5-V Crossing Time at Fourth-Stage Output for Multistage CMOS Comparator with Ohmic-MOSFET Loads.



Notes:
All current values are in uA.
Transistor sizes are W/L in u.

Figure 5-20. Schematic Diagram for the Constant-Fraction Comparator Used in the CMOS CFD.

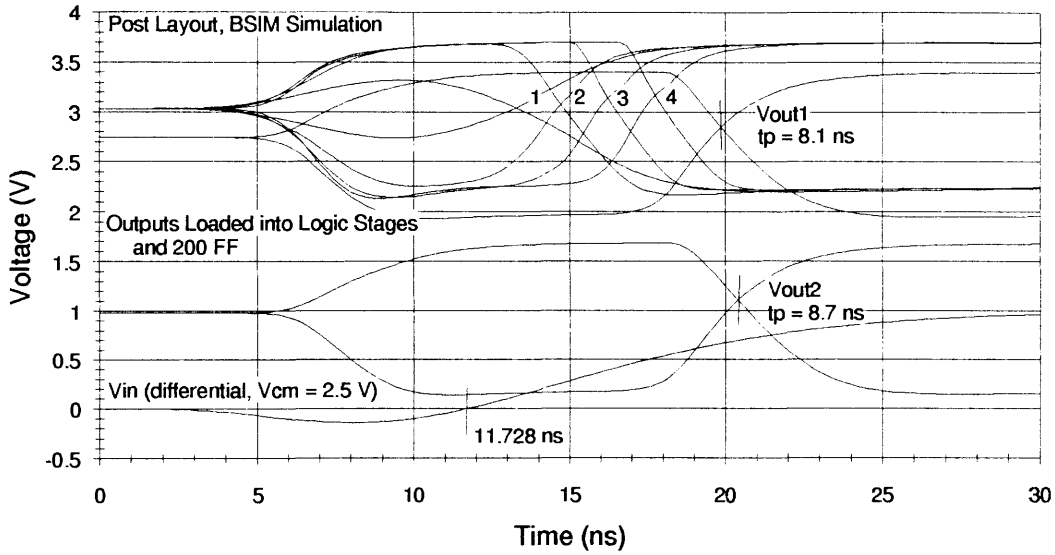


Figure 5-21. SPICE-Simulated Signals for the Constant-Fraction Comparator Used in the CMOS CFD.

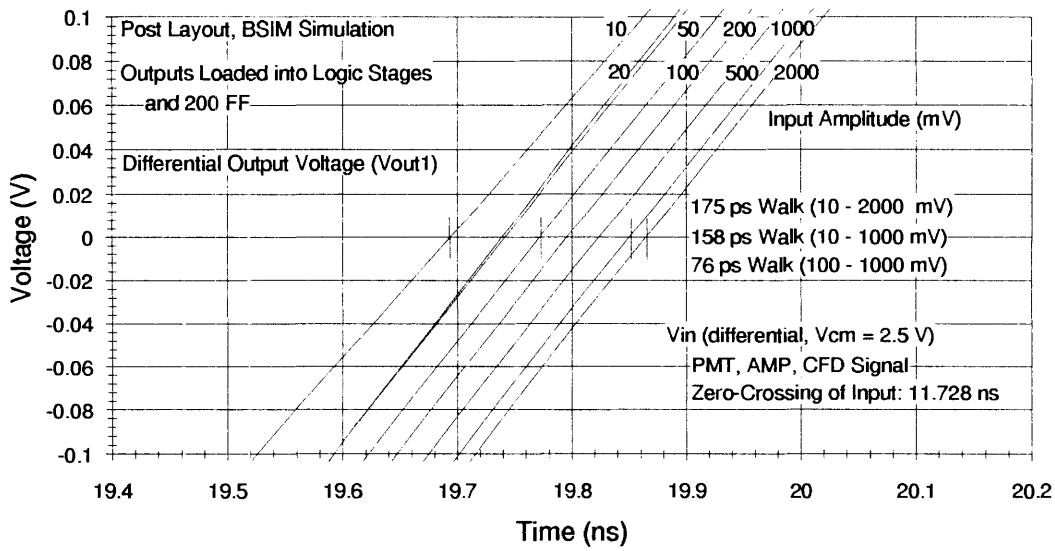


Figure 5-22. SPICE-Simulated Walk for the Constant-Fraction Comparator Used in the CMOS CFD.

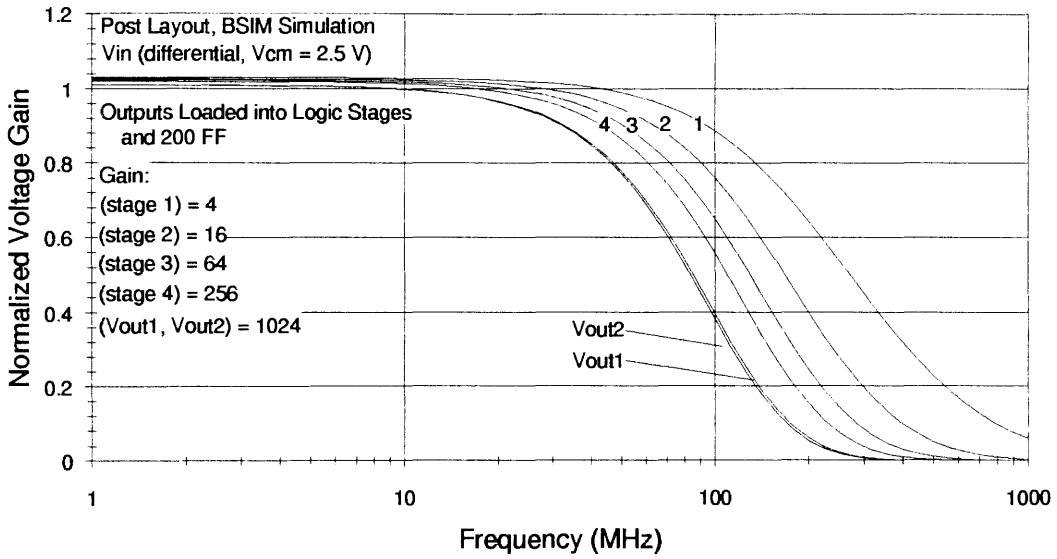


Figure 5-23. SPICE-Simulated Frequency Response for the Constant-Fraction Comparator Used in the CMOS CFD.

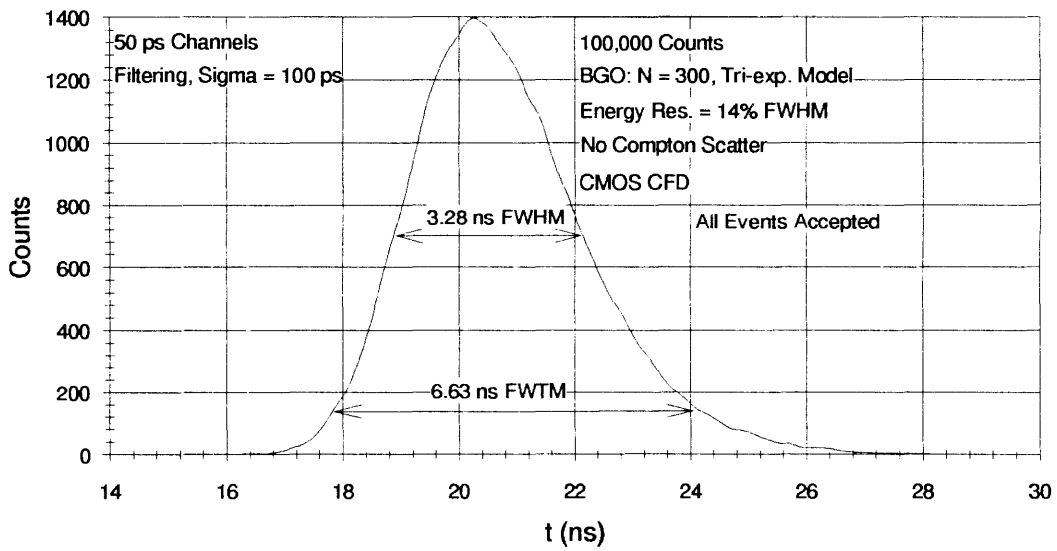


Figure 5-24. Monte Carlo Timing Spectrum without Compton Scatter for the CMOS CFD.

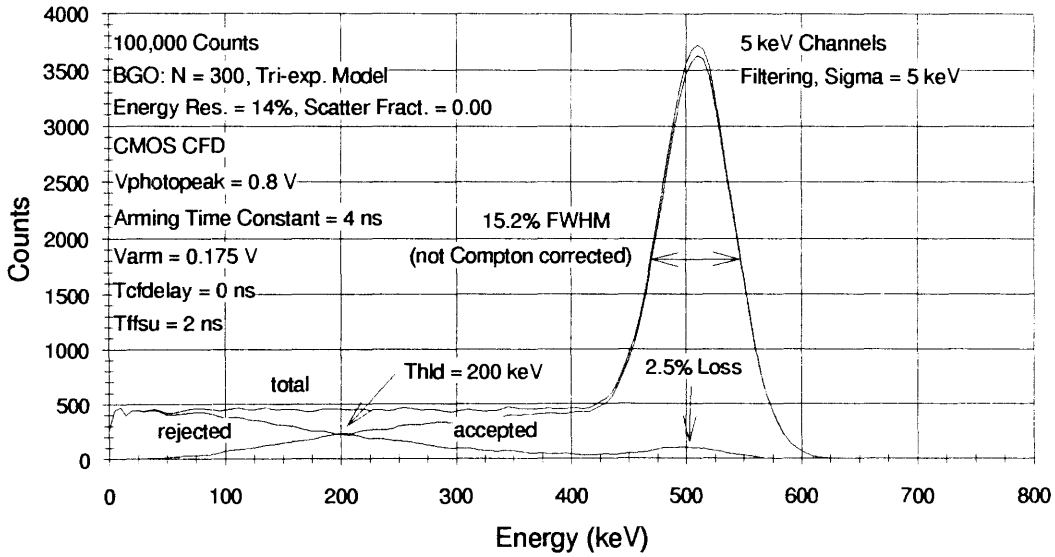


Figure 5-25. Monte Carlo Energy Spectrum with Low Compton Scatter for the CMOS CFD without Optional Arming Delay.

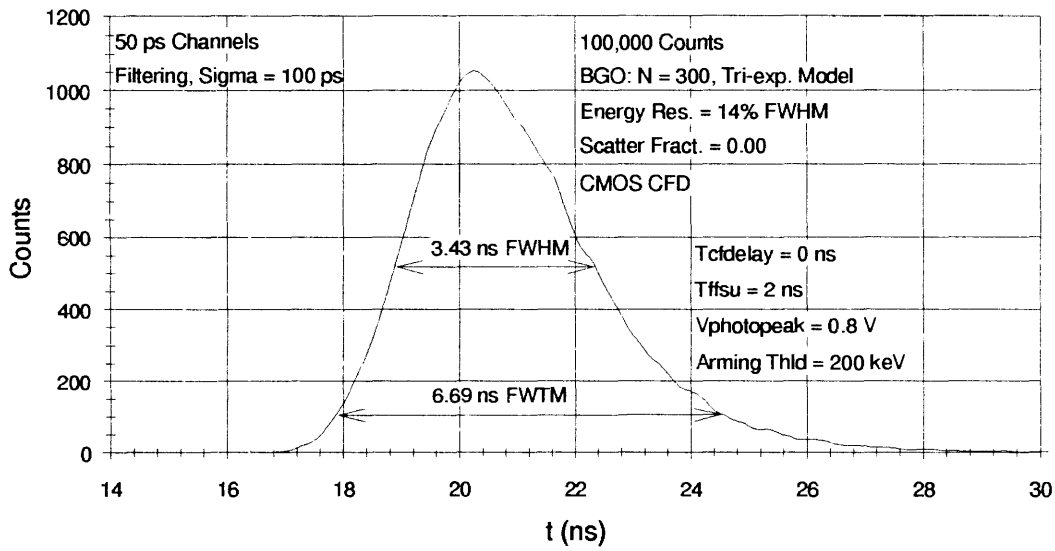


Figure 5-26. Monte Carlo Timing Spectrum with Low Compton Scatter for the CMOS CFD without Optional Arming Delay.

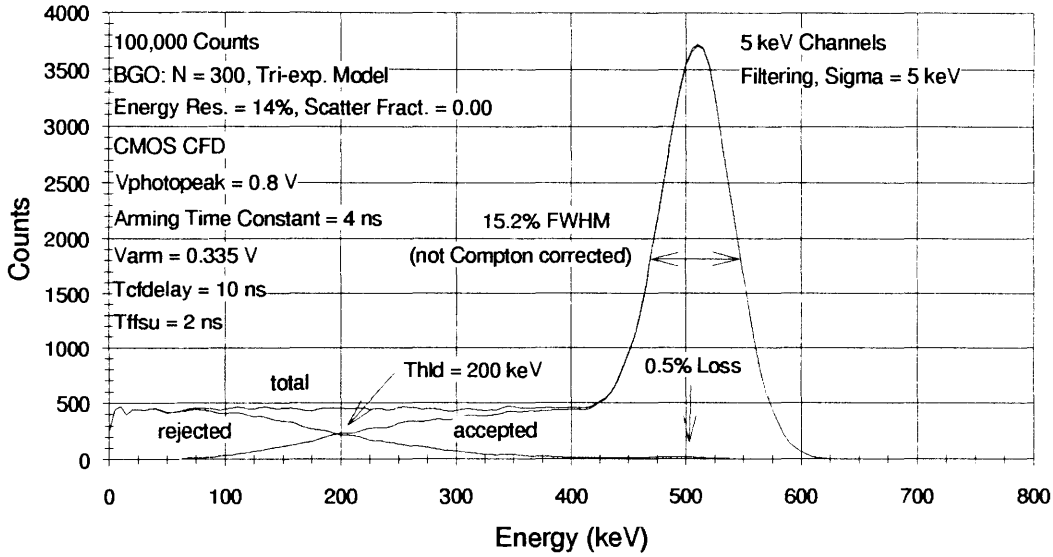


Figure 5-27. Monte Carlo Energy Spectrum with Low Compton Scatter for the CMOS CFD with Optional Arming Delay.

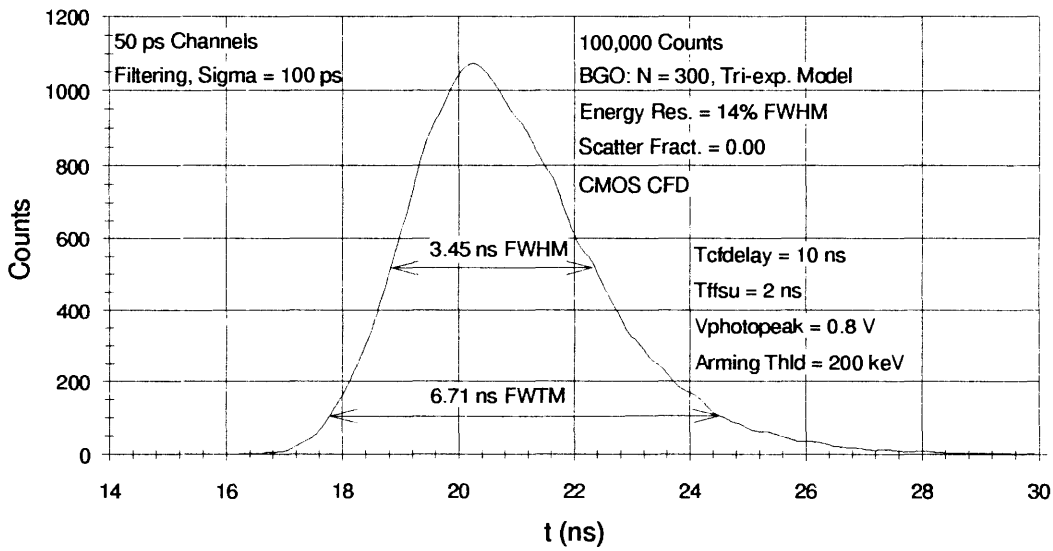


Figure 5-28. Monte Carlo Timing Spectrum with Low Compton Scatter for the CMOS CFD with Optional Arming Delay.

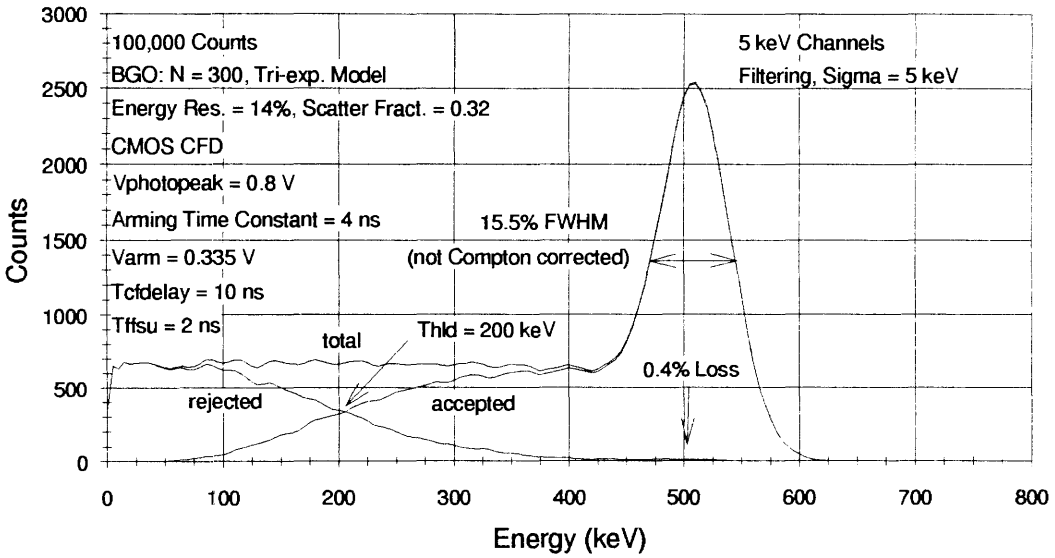


Figure 5-29. Monte Carlo Energy Spectrum with High Compton Scatter for the CMOS CFD with Optional Arming Delay.

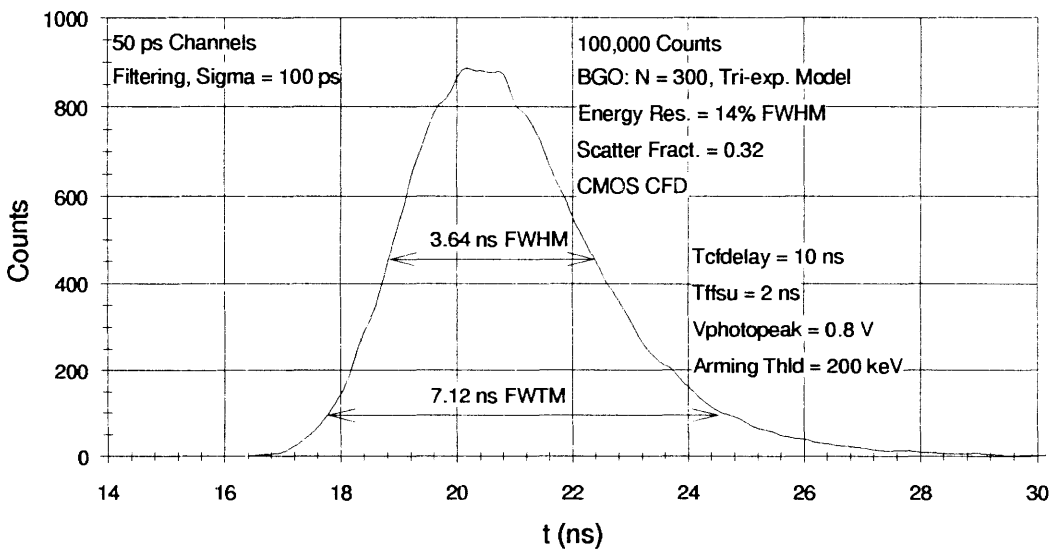


Figure 5-30. Monte Carlo Timing Spectrum with High Compton Scatter for the CMOS CFD with Optional Arming Delay.

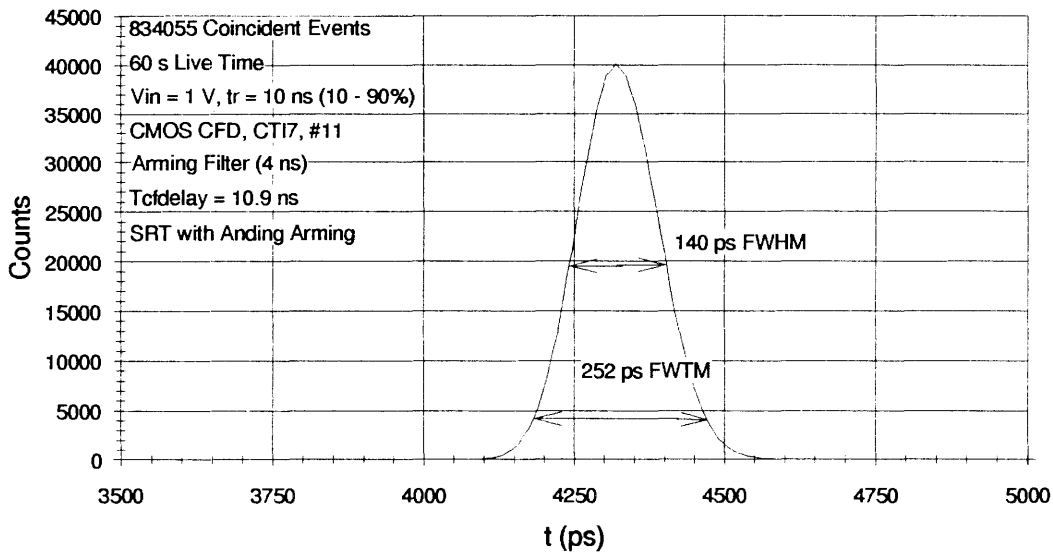


Figure 5-31. Measured Timing Jitter for the CMOS CFD.

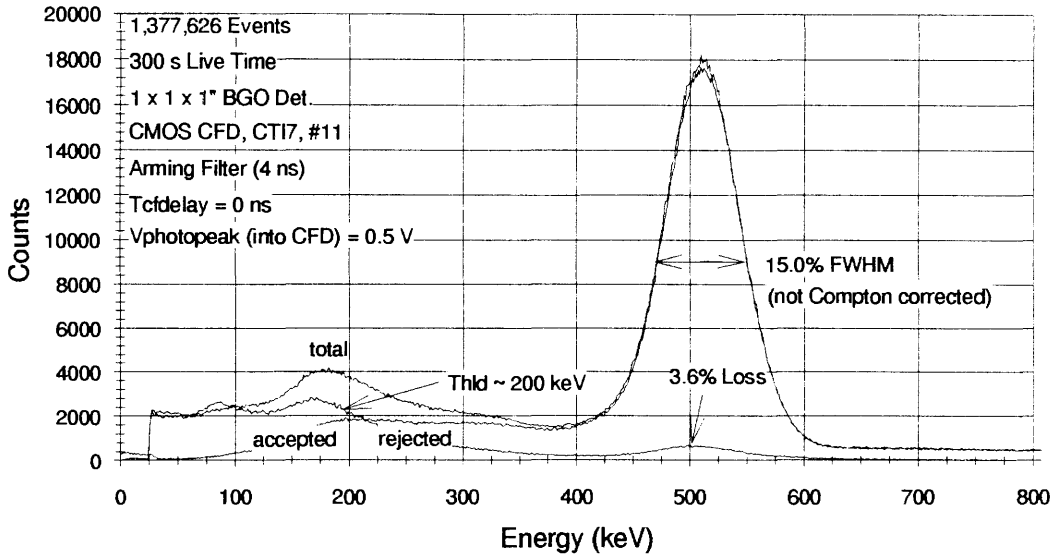


Figure 5-32. Measured Energy Spectrum with Low Compton Scatter for the CMOS CFD without Optional Arming Delay.

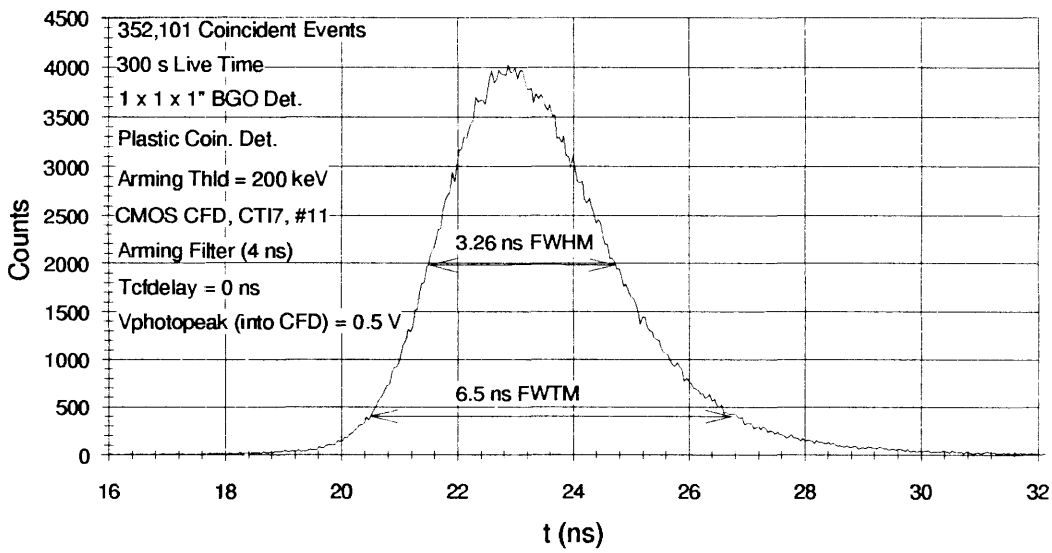


Figure 5-33. Measured Timing Spectrum with Low Compton Scatter for the CMOS CFD without Optional Arming Delay.

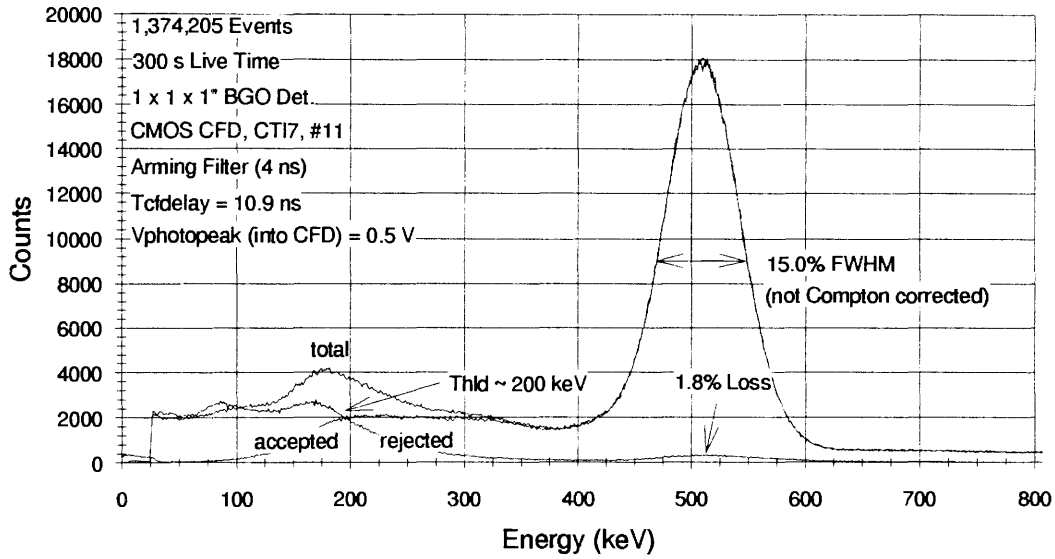


Figure 5-34. Measured Energy Spectrum with Low Compton Scatter for the CMOS CFD with Optional Arming Delay.

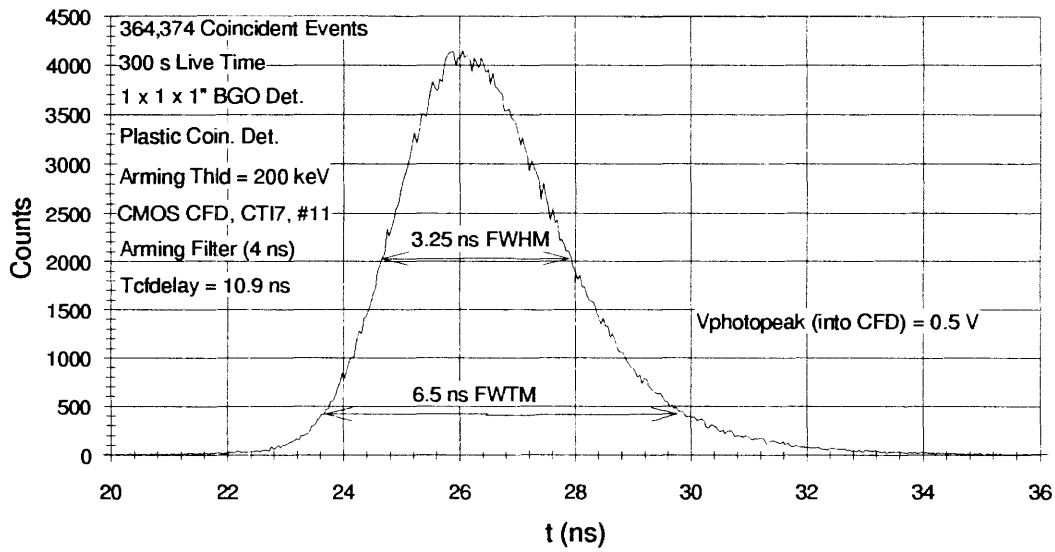


Figure 5-35. Measured Timing Spectrum with Low Compton Scatter for the CMOS CFD with Optional Arming Delay.

6. CONCLUSION

Summarizing Discussion

A fully-monolithic CMOS CFD, believed to be the first such reported circuit, was developed and experimentally evaluated. The measured timing resolution of 3.26 ns FWHM, 6.50 ns FWTM (Figure 5-33, page 250) for this circuit is comparable to the measured timing resolution of 3.30 ns FWHM, 6.40 ns FWTM (Figure 4-34, page 173) for a commercial bipolar CFD utilizing an external delay line. Both CFD circuits were evaluated with a BGO/photomultiplier scintillation detector excited by 511-keV coincident gamma rays from a ^{22}Na point source. The scintillation detector considered has energy resolution (approximately 14% FWHM) and timing resolution (approximately 3 ns FWHM using standard delay-line CFD circuits) for 511-keV gamma rays that is comparable to detectors used in commercial PET medical tomographs. The development of a fully-monolithic CMOS CFD is significant for PET and other systems where many channels of time pick-off circuits are required. The use of monolithic CMOS technology permits integration of the CFD with high-density, mixed analog and digital circuits.

Key to the development of the fully-monolithic CMOS CFD was the development and analysis of non-delay-line CFD timing circuits (described in *Section 4*) since it is not feasible to integrate delay lines into monolithic circuitry. The non-delay-line CFD circuit reported by Nowlin [1, 2], utilizing approximate differentiator networks in place of the delay line used in the standard CFD, was evaluated. Additionally, what is believed to be a new class of non-delay-line CFD circuits was presented. These circuits, designated as Binkley CFD circuits [3], utilize lowpass or allpass networks in place of the delay line used in the standard CFD.

It was shown that the Binkley CFD, utilizing a single-pole lowpass filter, has identical performance as the Nowlin CFD, utilizing a single-pole highpass filter, with an appropriate interchange of fraction values for the CFD circuits. Additionally, it was shown that CFD shaping-signal underdrive, zero-crossing slope, and timing-jitter performance is improved in the Binkley CFD with increasing circuit order for lowpass, delay-line approximation filters. Performance of the delay-line CFD and the Binkley non-delay-line CFD (utilizing 1 - 4-pole Gaussian lowpass delay-line approximation filters) is compared in Tables 4-4, 4-5, 4-6, and 4-7 (pages 138, 139, 141, and 142) for lowpass-filtered step inputs with bandlimited noise. Both single- and two-pole step inputs, resulting from lowpass filtering of a step input in the presence of white noise, are considered. The performance of the Binkley CFD, utilizing a four-pole Gaussian lowpass delay-line approximation filter, is shown to be comparable to the

performance of the delay-line CFD for two-pole step inputs. A two-pole step input models the signal present from the BGO/photomultiplier scintillation detector considered with subsequent front-end preamplification. The Binkley non-delay-line CFD circuits are advantageous for monolithic integration because high-order (four pole or more) lowpass delay-line approximation filters can be readily implemented.

In order to develop the fully-monolithic CMOS CFD, it was necessary to predict the CFD timing performance for the BGO/photomultiplier scintillation detector application considered. This is necessary because experimental adjustment of circuit parameters is not feasible following integrated-circuit fabrication. Monte Carlo analysis was developed (presented in *Section 3*) which modeled detector photoemission statistical noise, photomultiplier single-electron gain and transit-time statistics, and the impulse response of the photomultiplier tube, front-end preamplifier, and CFD (or other) time pick-off circuit [4]. This is believed to be the first such reported analysis that considers the characteristics of front-end preamplification and time pick-off circuitry.

Monte Carlo timing resolution, for the BGO/photomultiplier scintillation detector considered, was presented (Figures 4-24 and 4-25, page 168) for the delay-line CFD and non-delay-line Binkley CFD (utilizing 1 - 4-pole Gaussian lowpass delay-line approximation filters) as a function of constant-fraction delay. Monte Carlo timing resolution was experimentally verified for various constant-fraction delays for the delay-line CFD as illustrated in the figures. Comparable Monte Carlo timing performance was shown (Table 4-8, page 147) for the delay-line CFD and the Binkley non-delay-line CFD (utilizing 1 - 4-pole Gaussian lowpass delay-line approximation filters). This established the feasibility of using the Binkley CFD timing circuits in the fully-monolithic CMOS CFD to obtain timing performance comparable to existing delay-line CFD circuits.

In addition to timing-resolution prediction, Monte Carlo analysis was extended (*Section 4*) to predict time pick-off circuit energy discrimination. Monte Carlo timing and energy spectra (Figures 4-31 and 4-32, pages 171 and 172) are shown to be in good agreement with measured timing and energy spectra (Figures 4-33 and 4-34, pages 172 and 173) for a commercial delay-line CFD connected to the BGO/photomultiplier scintillation detector considered. Monte Carlo timing resolution of 3.22 ns FWHM, 6.41 ns FWTM is comparable to the measured resolution of 3.30 ns FWHM, 6.40 ns FWTM. The Monte Carlo predicted 511-keV photopeak loss is 2.2% comparable to the measured loss of 2.5%. The photopeak loss is due to limited energy-discrimination resolution in the CFD.

The addition of a time delay (10 ns for the BGO/photomultiplier scintillation detector considered) at the output of the CFD constant-fraction comparator was described (*Section 4*) as a way of reducing CFD photopeak loss by improving energy-discrimination performance. CFD energy-discrimination performance is improved because the arming decision time is delayed permitting better accumulation of arming-discrimination statistics. Monte Carlo simulations predicted the 511-keV photopeak loss for the CMOS CFD at 2.5% (Figure 5-25, page 246) without the constant-fraction comparator delay and 0.5% (Figure 5-27, page 247) with the delay. The measured CMOS CFD photopeak loss was 3.6% (Figure 5-32, page 250) without the delay and 1.8% (Figure 5-34, page 251) with the delay. Measured photopeak loss with the delay, using alternate source-coupled arming logic circuitry included in the CMOS CFD, was 0.44% which is in close agreement with the Monte Carlo prediction of 0.5%. This indicates that the saturating-logic arming logic circuitry used for most of the reported CMOS CFD measurements may not have provided the full 10 ns of constant-fraction comparator delay, and this will be investigated before completion of an entire PET front-end CMOS integrated circuit. The measured 1.8% photopeak loss, using the saturating-logic arming circuitry with the constant-fraction comparator delay included, is acceptable for the PET application considered. Minimizing CFD photopeak loss improves the detection efficiency of PET tomography systems resulting in better image statistics.

Monte Carlo predicted timing resolution for the CMOS CFD was in good agreement with measured data. The Monte Carlo timing resolution, without inclusion of the constant-fraction comparator delay, was 3.43 ns FWHM, 6.69 ns FWTM (Figure 5-26, page 246) compared to measured resolution of 3.26 ns FWHM, 6.50 ns FWTM (Figure 5-33, page 250). The Monte Carlo timing resolution, with inclusion of the constant-fraction comparator delay, was 3.45 ns FWHM, 6.71 ns FWTM (Figure 5-28, page 247) compared to measured resolution of 3.25 ns FWHM, 6.50 ns FWTM (Figure 5-35, page 251). Both the Monte Carlo and measured timing resolution were essentially unaffected when constant-fraction comparator delay was included to improve energy-discrimination performance.

In addition to Monte Carlo analysis of timing and energy-discrimination performance, analysis of timing walk and jitter was presented (*Section 2*) for time pick-off circuits. Comparator walk was discussed using the charge-sensitivity model to describe changing comparator propagation delay with input-signal overdrive and slope. Additionally, optimal (matched) filters for minimizing timing jitter are presented along with suboptimal filters. An optimal filter was developed (Figures 2-11 and 2-12, pages 55 and 56) for minimizing timing jitter associated with a linear-edge signal in the presence of white noise. Timing

jitter performance is compared (Figure 2-13, page 57) for the optimal filter developed and a single-pole lowpass filter where it is shown that timing jitter is at least 10.8% higher using the single-pole lowpass filter. Although timing walk and jitter are not dominant sources of error for the fully-monolithic CMOS CFD, analysis of these errors is included for completeness and to permit development of other timing systems, including BGO/avalanche-photodiode timing systems where timing jitter is significant.

Following the presentation of timing walk, jitter, and detector-statistical analysis (Monte Carlo analysis), and the presentation of delay-line and non-delay-line CFD timing circuits, previously reported practical CFD circuits were reviewed (*Section 5*). Following this, circuits developed for the fully-monolithic CMOS CFD were presented. These circuits were developed using a standard, digital, 2-μ, double-metal, double-poly, n-well CMOS process. The CMOS circuits developed include a wideband (>100 MHz bandwidth, Figure 5-11, page 236) continuous-time filter configured as a Binkley CFD circuit having a five-pole Gaussian lowpass delay-line approximation filter. This fully differential circuit (Figure 5-7, page 234) did not require common-mode feedback as is typically required in differential CMOS continuous-time filter circuits.

As a part of the constant-fraction comparator design for the CMOS CFD, design analysis was presented for minimizing comparator time walk. This analysis, believed to be the first such reported analysis, considers the tradeoffs between small-signal gain-bandwidth and circuit nonlinearities on walk performance. It was shown that walk is much less for differential CMOS stages with ohmic (resistive) loads compared to walk when current-source loads are used (Figures 5-14 and 5-15, page 239). The improvement in walk performance is due to well-controlled circuit limiting, where limiting voltage is equal to the voltage drop across an ohmic load when full differential-pair bias current is switched to the load). Graphs (Figures 5-17, 5-18, and 5-19, pages 241 and 242) of comparator propagation delay and walk, generated from multiple SPICE simulations, are shown for cascaded, differential CMOS stages with ohmic loads. These graphs permit selection of differential-pair MOSFET transistor size and circuit limiting voltage for a required comparator propagation delay and walk specification.

The constant-fraction comparator (Figure 5-20, page 243) for the CMOS CFD consists of five differential comparator stages with ohmic loads and was designed using the comparator walk-optimization analysis previously described. The SPICE simulated walk performance is 158 ps (Figure 5-22, page 244) for 10 - 1000 mV input signals having rise-times (10 - 90%) of approximately 10 ns, which is comparable to the measured walk of 210 ps (AD9685 [5]) and

250 ps (VC7695 [6]) for high-speed bipolar ECL comparators [7]. The propagation delay of the CMOS constant-fraction comparator, however, is higher at 8 ns compared to 2.5 ns for the ECL comparators.

Following presentation of the CMOS CFD circuit design and analysis, performance was experimentally verified using the BGO/photomultiplier scintillation detector considered. As mentioned, the measured timing resolution of 3.26 ns FWHM, 6.50 ns FWTM (Figure 5-33, page 250) is in good agreement with the Monte Carlo timing resolution of 3.43 ns FWHM, 6.69 ns FWTM (Figure 5-26, page 246). Additionally, the measured CMOS CFD timing resolution is comparable to the measured timing resolution of 3.30 ns FWHM, 6.40 ns FWTM (Figure 4-23, page 173) for a commercial delay-line CFD. Comparable timing performance between the fully-monolithic CMOS CFD and existing delay-line CFD circuits indicates that the CMOS CFD was successfully developed.

Suggestions for Future Work

The development of the fully-monolithic CMOS CFD presented here was for PET BGO/photomultiplier scintillation detector applications. All of the timing walk, jitter, and Monte Carlo statistical analysis presented can be extended to other applications, including BGO/avalanche-photodiode detector applications. Additionally, the non-delay-line CFD circuits presented can be optimized for other detector applications. Finally, the 2-μ CMOS circuits presented can be developed in faster processes if wider-band non-delay-line CFD circuits or faster constant-fraction comparator circuits are needed for other detector applications.

In the CMOS CFD presented here, arming threshold and CFD walk adjustments were provided externally. Arming threshold and walk adjustments can be provided on the monolithic circuit, and this is planned for a complete PET front-end, CMOS integrated circuit under development at CTI PET Systems, Inc. CFD arming threshold, under digital control, can be provided by a CMOS D/A converter circuit. CFD walk adjustment can be provided using a gated baseline restorer circuit (as described in *Section 5*). Such a circuit could sample the constant-fraction comparator differential output (at the final output or an intermediate stage) and, through negative feedback, inject a circuit offset to maintain a differential output voltage of zero when no input pulse is present. This will correct for CFD shaping-signal offset voltage and constant-fraction comparator offset voltage. The use of a gated baseline restorer circuit inhibits offset correction during the presence of a signal pulse. This improves offset correction and minimizes offset shifts with pulse count rate.

Monte Carlo predictions of CFD energy and timing spectra presented here did not include constant-fraction comparator and arming flip-flop walk errors as these errors were negligible for the application considered. These walk errors could be included in Monte Carlo analysis to predict energy and timing spectra for general timing systems.

No analytical expression for predicting CFD energy and timing spectra is believed to exist that fully considers detector photoemission statistics, photomultiplier single-electron gain and transit-time statistics, and impulse response of the photomultiplier, front-end preamplifier, and CFD circuit. The development of such an analytic expression, if possible, would be useful if it could be evaluated faster than Monte Carlo analysis or provide insight not available with Monte Carlo analysis.

Additionally, analytical expressions or modeling (most likely Monte Carlo) that simultaneously considers noise-induced timing jitter and detector statistical noise would be useful for applications, such as BGO/avalanche-photodiode applications, where timing performance is controlled by both circuit-noise induced timing jitter and detector statistical noise. Such analysis could permit the development of optimal filtering and timing shaping circuits for minimum timing resolution where tradeoffs between circuit-noise and detector statistical noise are considered.

References for Section 6

[1] Nowlin, C. H., "Amplitude- and Rise-Time-Compensated Filters," United States Patent 4,443,768, April 17, 1984.

[2] Nowlin, C. H., "Low-Noise Lumped-Element Timing Filters with Rise-Time Invariant Crossover Times," *Review of Scientific Instruments*, vol. 63, no. 4, April 1992, pp. 2322-2326.

[3] Binkley, D. M., "Amplitude- and Rise-Time-Insensitive Timing-Shaping Filters," United States Patent Pending, filed August 13, 1992.

[4] Binkley, D. M., "Optimization of Scintillation-Detector Timing Systems Using Monte Carlo Analysis," *Conference Record of the 1992 IEEE Nuclear Science Symposium and Medical Imaging Conference* (in publication).

[5] *1988 Linear Products Databook*, Analog Devices, Norwood, Massachusetts, 1988.

[6] *Linear Signal Processing (LSP) Data Book*, VTC Incorporated, Bloomington, Minnesota, 1978.

[7] Turko, B. T., W. F. Kolbe, and R. C. Smith, "Ultra-Fast Voltage Comparators for Transient Waveform Analysis," *IEEE Transactions on Nuclear Science*, vol. 37, no. 2, April 1990, pp. 424-429.

APPENDICES

APPENDIX A. CATALOG OF NORMALIZED CFD PERFORMANCE FOR LOWPASS-FILTERED STEP INPUTS

Characteristics of Single-Pole Step Inputs

A single-pole step-input signal consists of a step input and white noise source that are both lowpass filtered by a single-pole lowpass filter having a time-constant of t_{in}. The signal and noise characteristics of the single-pole step signal are summarized in Table A-1. These signal and noise characteristics are needed for interpretation of normalized CFD performance for single-pole step inputs.

Table A-1. Characteristics of Single-Pole Step Input.

Parameter	**Equation**	**(Eq.)**
Waveform	$v_{in}(t \geq 0) = V_{inpk}\left(1 - e^{-t/t_{in}}\right)$	4-17
Peak Slope	$K_{inpk}(t = 0) = V_{inpk} / t_{in}$	4-19
Noise Power-Spectral Density	$S_{in}(\omega) = \frac{e_n^2}{2}\left[\frac{1}{1+(\omega t_{in})^2}\right]$	4-21
Total Noise (rms)	$\sigma_{vin} = \frac{e_n}{2\sqrt{t_{in}}}$	4-24
Minimum Timing Jitter (rms)	$\sigma_{tin\ (min)}(t = 0) = \frac{\sigma_{vin}}{K_{inpk}} = \frac{e_n\sqrt{t_{in}}}{2V_{inpk}}$	4-27

Characteristics of Two-Pole Step Inputs

A two-pole step-input signal results from a step input and white noise source that are both lowpass filtered by a two-pole lowpass filter having real poles with time-constants of $t_{in}/\sqrt{2}$. The 10 - 90% rise-time for the two-pole step-input is approximately equal to that of the single-pole step-input having a (single) time-constant of t_{in}. The signal and noise characteristics of the two-pole step signal are summarized in Table A-2. These signal and noise characteristics are needed for interpretation of normalized CFD performance for two-pole step inputs.

Table A-2. Characteristics of Two-Pole Step Input.

Parameter	**Equation**	**(Eq.)**
Waveform	$v_{in}(t \geq 0) = V_{inpk}\left(1 - e^{-\sqrt{2}t/t_{in}}(1 + \sqrt{2}\,t/t_{in})\right)$	4-18
Peak Slope	$K_{inpk}(t = t_{in}/\sqrt{2}) = \sqrt{2}\,e^{-1}\,V_{inpk}/t_{in}$	4-20
Noise Power-Spectral Density	$S_{in}(\omega) = \frac{e_n^2}{2}\left[\frac{1}{\left(1 + (\omega t_{in}/\sqrt{2})^2\right)^2}\right]$	4-22
Total Noise (rms)	$\sigma_{vin} = \frac{e_n}{2\sqrt{2t_{in}/\sqrt{2}}}$	4-25
Minimum Timing Jitter (rms)	$\sigma_{tin\ (min)}(t = t_{in}/\sqrt{2}) = \frac{\sigma_{vin}}{K_{inpk}} = \frac{e_n\sqrt{t_{in}/\sqrt{2}}}{2\sqrt{2}\,e^{-1}\,V_{inpk}}$	4-29

Delay-Line CFD with Single-Pole Step Inputs

Table A-3 contains a directory of figures (data plots) and equations giving delay-line CFD performance for single-pole step-input signals. CFD performance is normalized to the input-signal characteristics which are given in Table A-1. The single-pole step-input signal and resulting constant-fraction-discriminator shaping signal are shown in Figure A-1.

Table A-3. Delay-Line CFD Performance for Single-Pole Step Inputs.

Parameter	Equation	(Eq.)	(Fig.)
Waveform	$v_{cf}\ (t \geq t_d) = V_{inpk}\left((1-f) - e^{-t/t_{in}}\left(e^{t_d/t_{in}} - f\right)\right)$	4-33	A-1
Zero-Crossing Time	$t_{cf}(t \geq t_d) = t_{in} \ln\left(\frac{e^{t_d/t_{in}} - f}{1-f}\right)$	4-34	A-2
Underdrive	$V_{cf\ (underdrive)} = \ -V_{inpk} f\left(1 - e^{-t_d/t_{in}}\right)$	4-36	A-3
Overdrive	$V_{cf\ (overdrive)} = V_{inpk}(1 \ - f)$	4-37	
Zero-Crossing Slope	$K_{cf} = V_{inpk}(1-f)/t_{in}$	4-39	A-4
Total Noise (rms)	$\sigma_{vcf} = \sigma_{vin}\sqrt{1^2 + f^2 - 2f\,e^{-\lvert t_d \rvert / t_{in}}}$	4-44	A-5
Timing Jitter (rms)	$\sigma_{tcf} = \frac{\sigma_{vcf}}{K_{cf}} = \frac{\sigma_{vin}\sqrt{1^2 + f^2 - 2f\,e^{-\lvert t_d \rvert / t_{in}}}}{V_{inpk}(1-f)/t_{in}}$	4-45	A-6

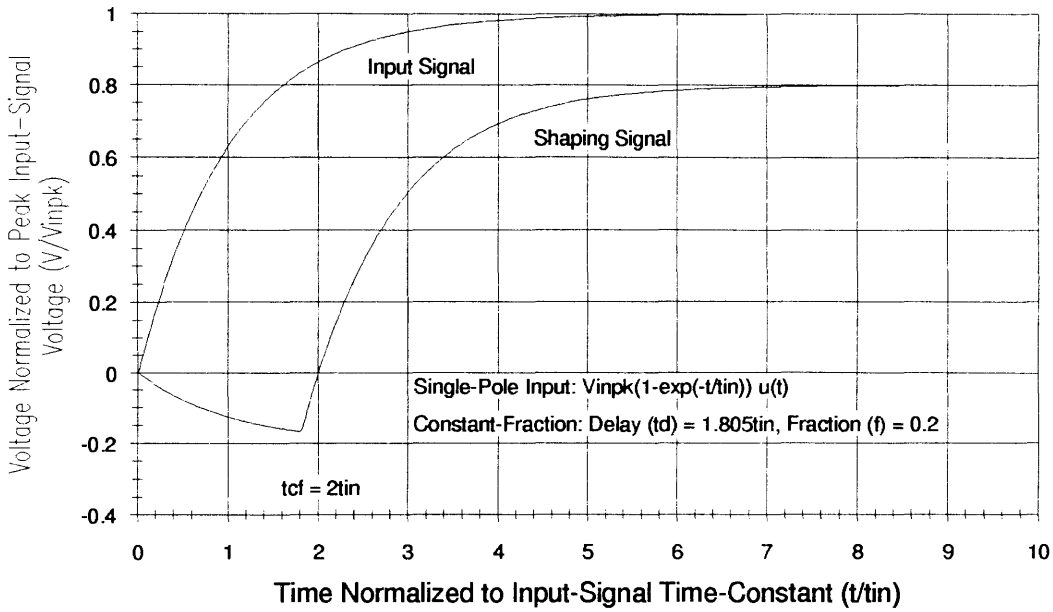


Figure A-1. Delay-Line CFD Shaping Signal for Single-Pole Step Input.

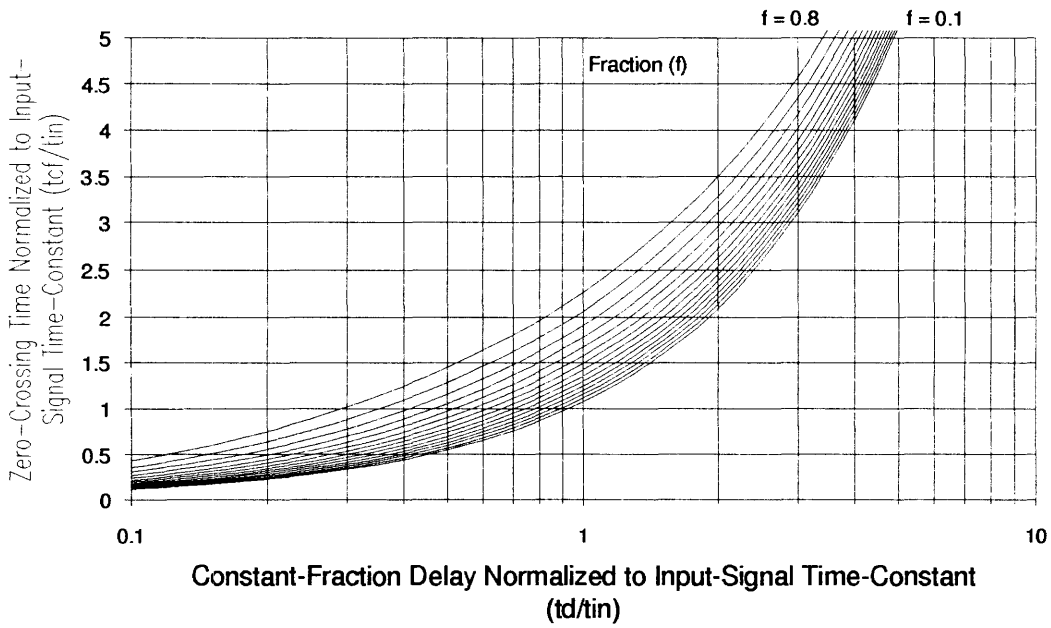


Figure A-2. Delay-Line CFD Zero-Crossing Time for Single-Pole Step Input.

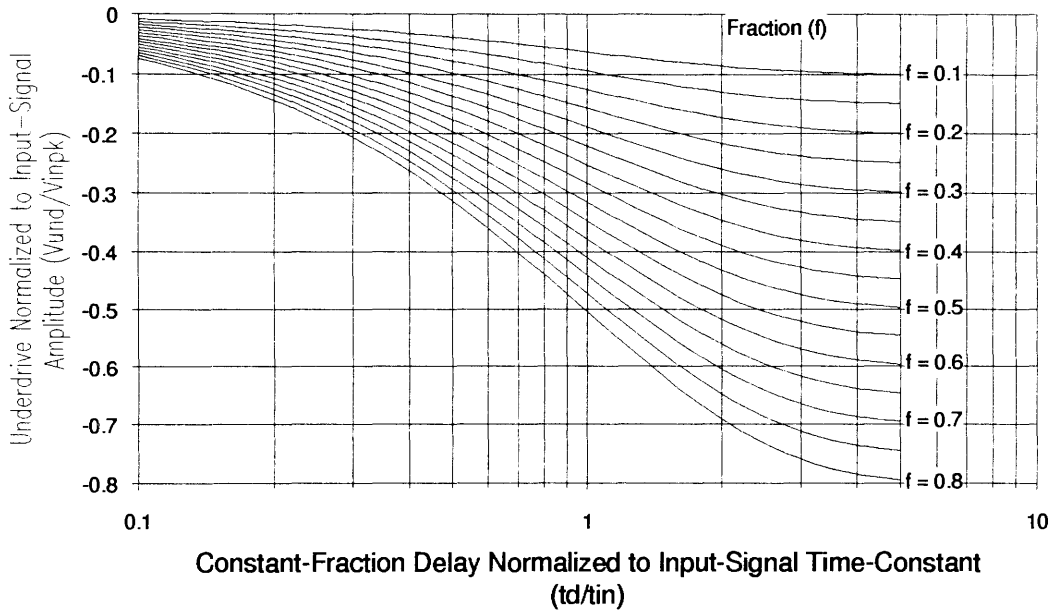


Figure A-3. Delay-Line CFD Underdrive for Single-Pole Step Input.

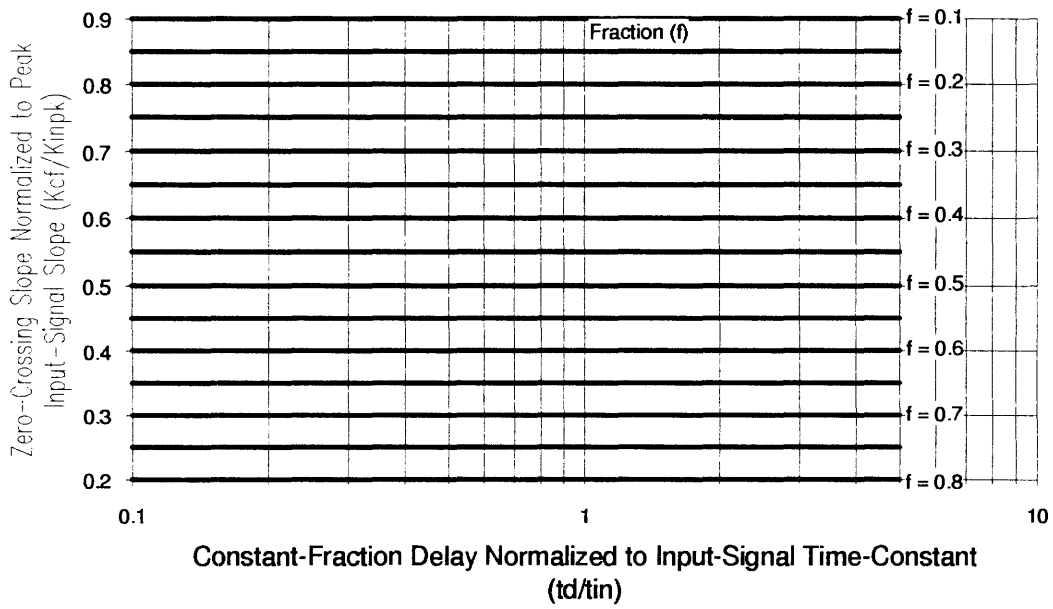


Figure A-4. Delay-Line CFD Zero-Crossing Slope for Single-Pole Step Input.

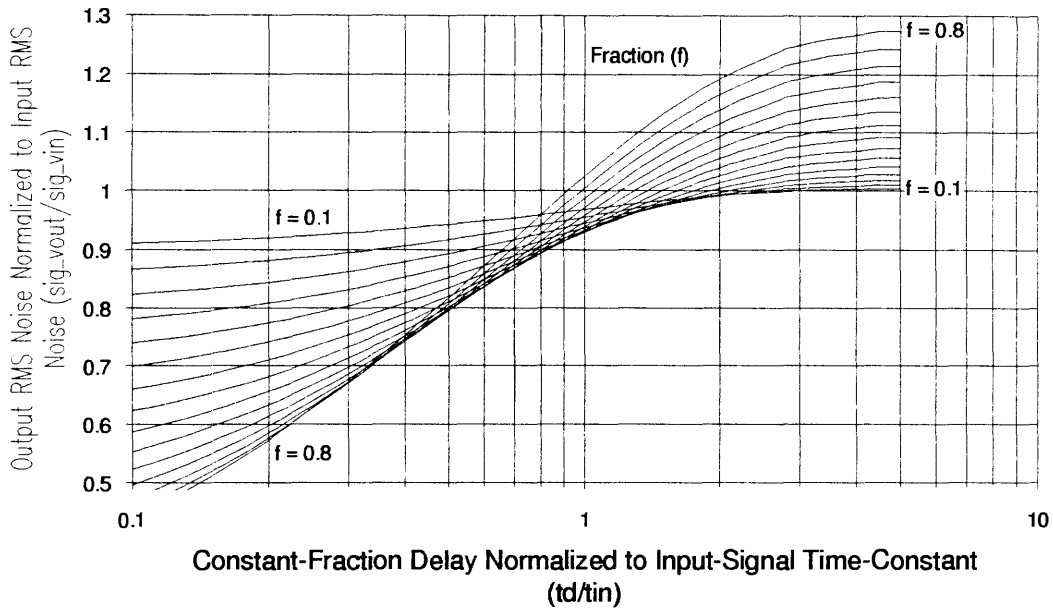


Figure A-5. Delay-Line CFD Noise for Single-Pole Step Input.

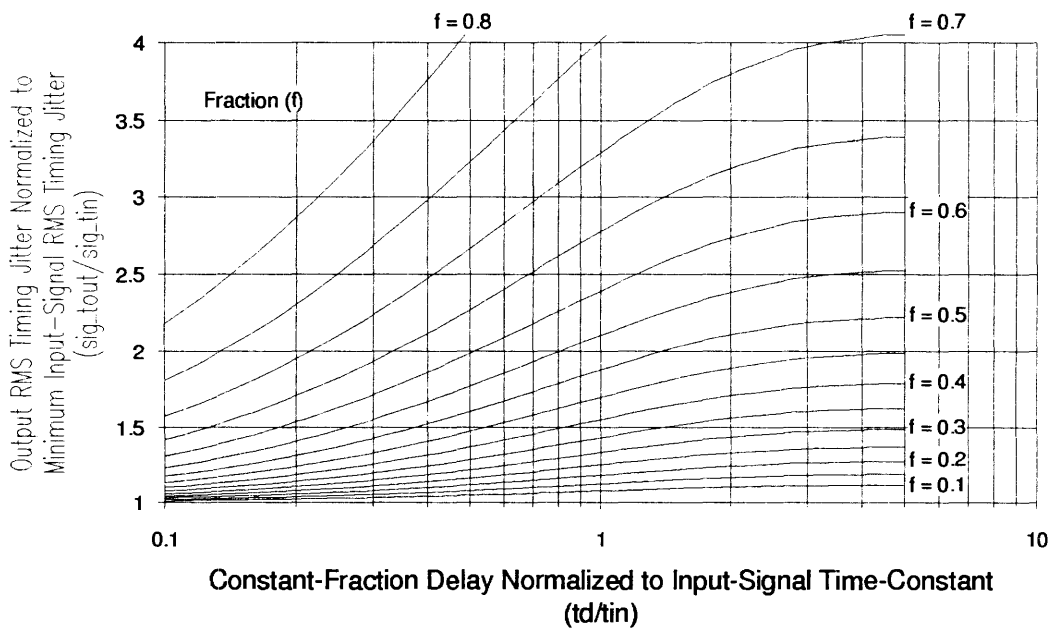


Figure A-6. Delay-Line CFD Timing Jitter for Single-Pole Step Input.

Delay-Line CFD with Two-Pole Step Inputs

Table A-4 contains a directory of figures (data plots) and equations giving delay-line CFD performance for two-pole step-input signals. CFD performance is normalized to the input-signal characteristics which are given in Table A-2. The two-pole step-input signal and resulting CFD shaping signal are shown in Figure A-7.

Table A-4. Delay-Line CFD Performance for Two-Pole Step Inputs.

Parameter	**Equation**	**(Eq.)**	**(Fig.)**
Waveform	$v_{cf}(t)$		A-7
Zero-Crossing Time	t_{cf}		A-8
Underdrive	$V_{cf\,(underdrive)}$		A-9
Overdrive	$V_{cf\,(overdrive)} = V_{inpk}(1 - f)$	4-37	
Zero-Crossing Slope	K_{cf}		A-10
Total Noise (rms)	σ_{vcf}		A-11
Timing Jitter (rms)	$\sigma_{tcf} = \frac{\sigma_{vcf}}{K_{cf}}$		A-12

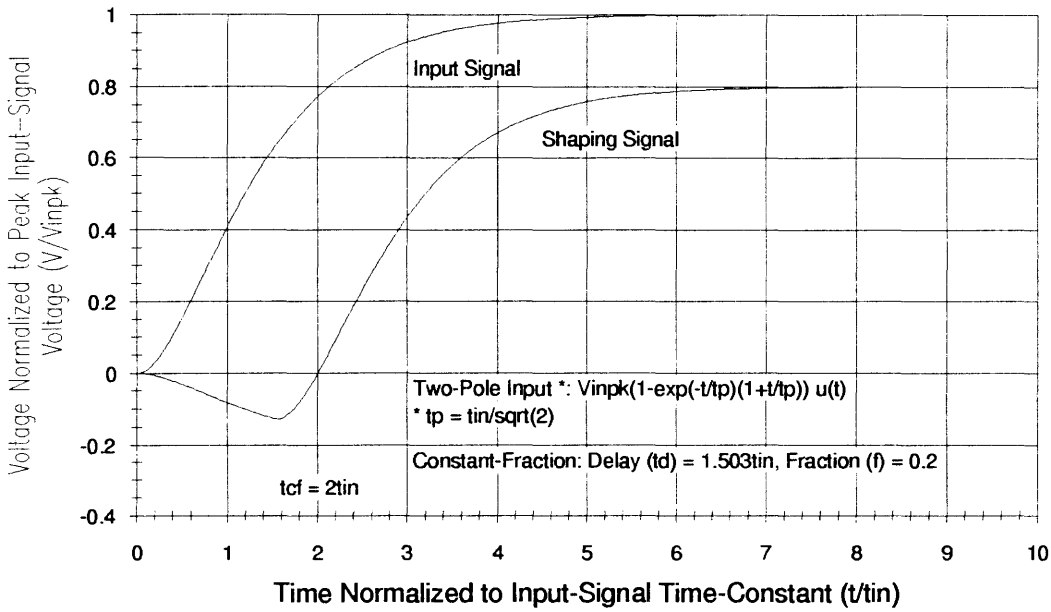


Figure A-7. Delay-Line CFD Shaping Signal for Two-Pole Step Input.

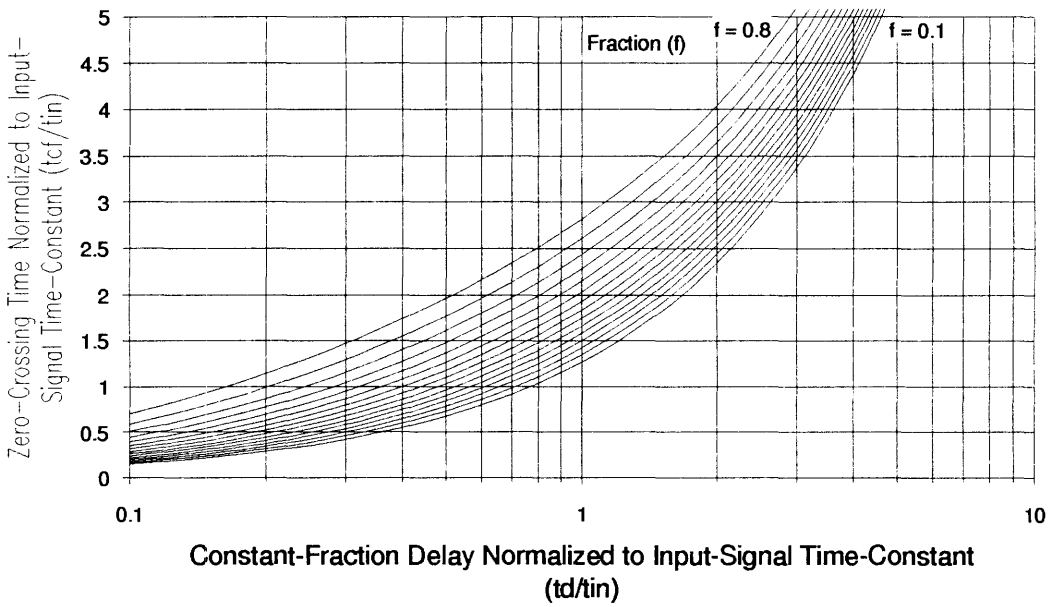


Figure A-8. Delay-Line CFD Zero-Crossing Time for Two-Pole Step Input.

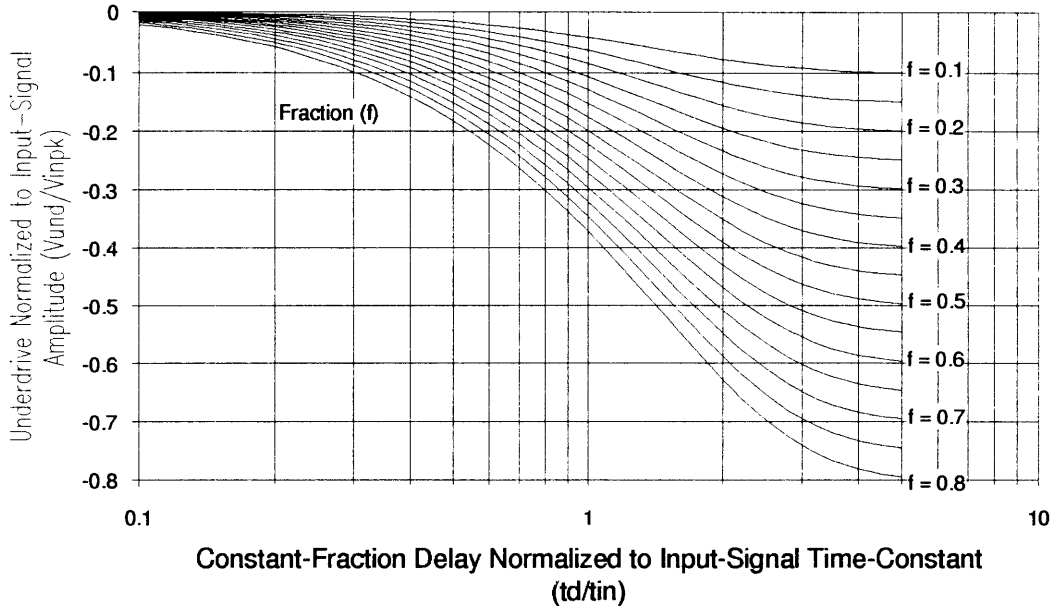


Figure A-9. Delay-Line CFD Underdrive for Two-Pole Step Input.

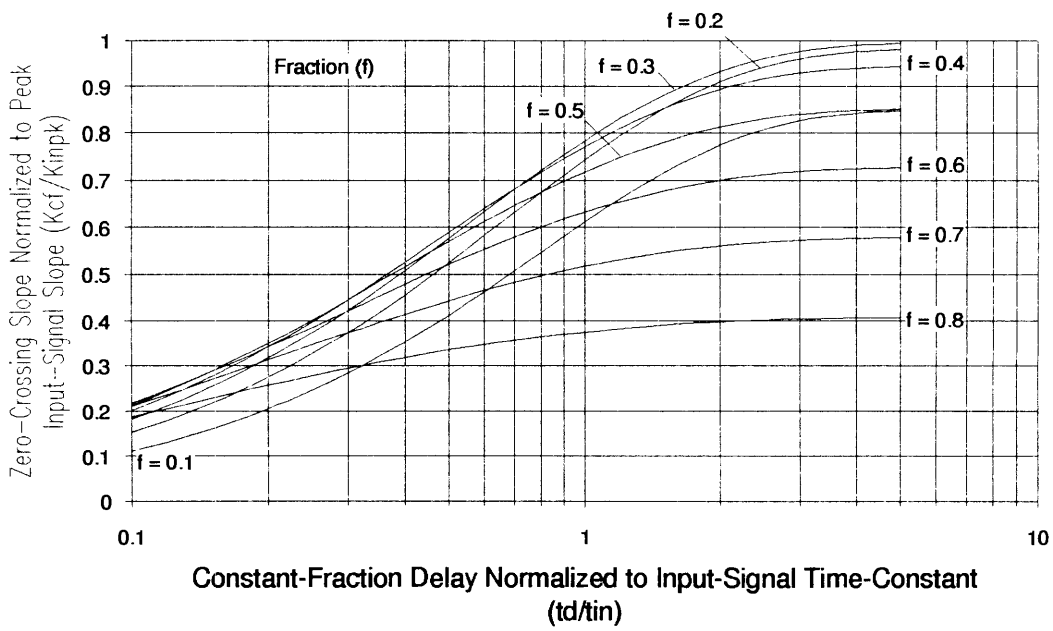


Figure A-10. Delay-Line CFD Zero-Crossing Slope for Two-Pole Step Input.

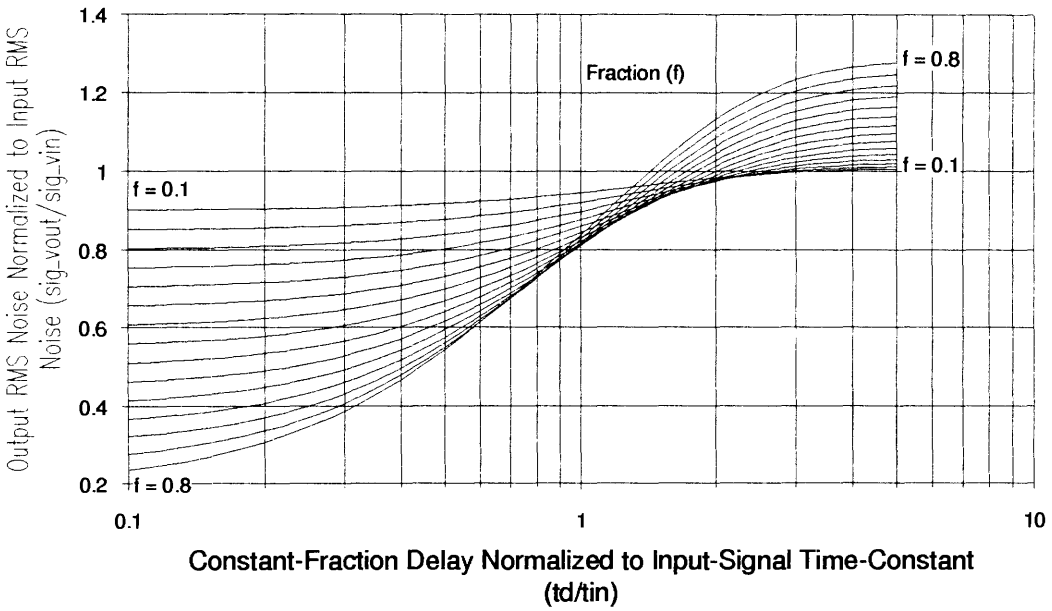


Figure A-11. Delay-Line CFD Noise for Two-Pole Step Input.

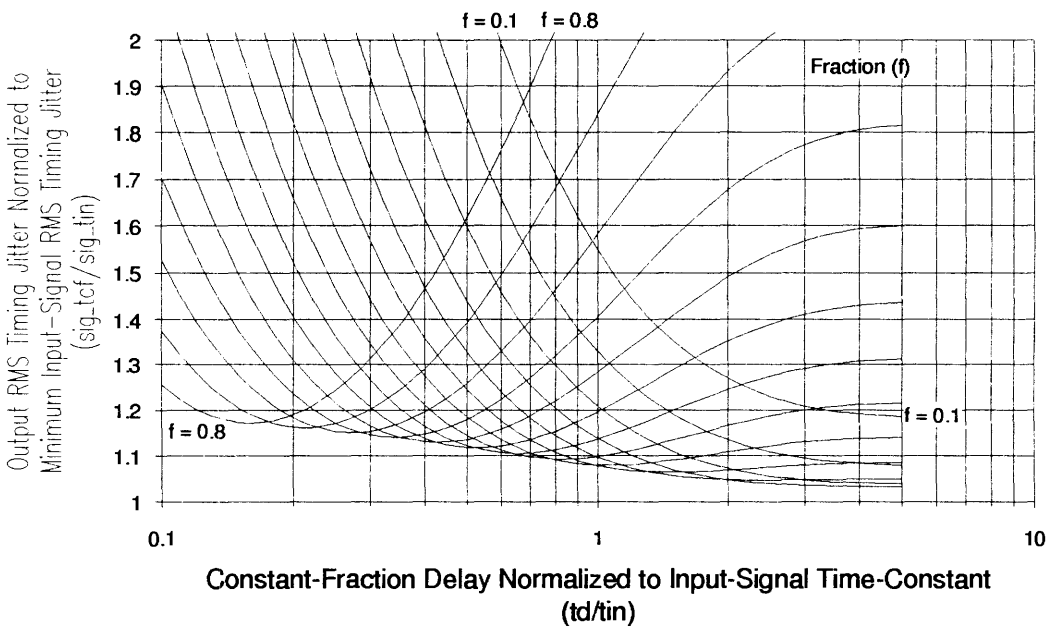


Figure A-12. Delay-Line CFD Timing Jitter for Two-Pole Step Input.

Binkley Single-Pole Gaussian CFD with Single-Pole Step Inputs

Table A-5 contains a directory of figures (data plots) and equations giving performance for the Binkley single-pole Gaussian CFD with single-pole step-input signals. CFD performance is normalized to the input-signal characteristics which are given in Table A-1. The single-pole step-input signal and resulting CFD shaping signal are shown in Figure A-13.

Table A-5. Binkley Single-Pole Gaussian CFD Performance for Single-Pole Step Inputs.

Parameter	Equation	(Eq.)	(Fig.)
Waveform	$v_{cf}(t)$		A-13
Zero-Crossing Time	t_{cf}		A-14
Underdrive	$V_{cf\,(underdrive)}$		A-15
Overdrive	$V_{cf\,(overdrive)} = V_{inpk}(1 - f)$	4-37	
Zero-Crossing Slope	K_{cf}		A-16
Total Noise (rms)	σ_{vcf}		A-17
Timing Jitter (rms)	$\sigma_{tcf} = \frac{\sigma_{vcf}}{K_{cf}}$		A-18

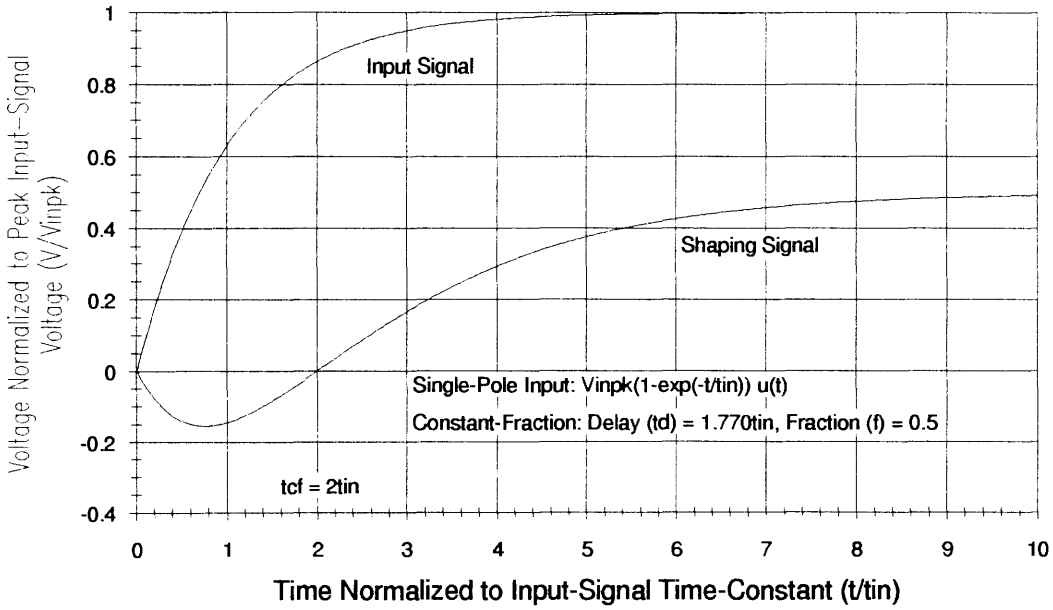


Figure A-13. Binkley Single-Pole Gaussian CFD Shaping Signal for Single-Pole Step Input.

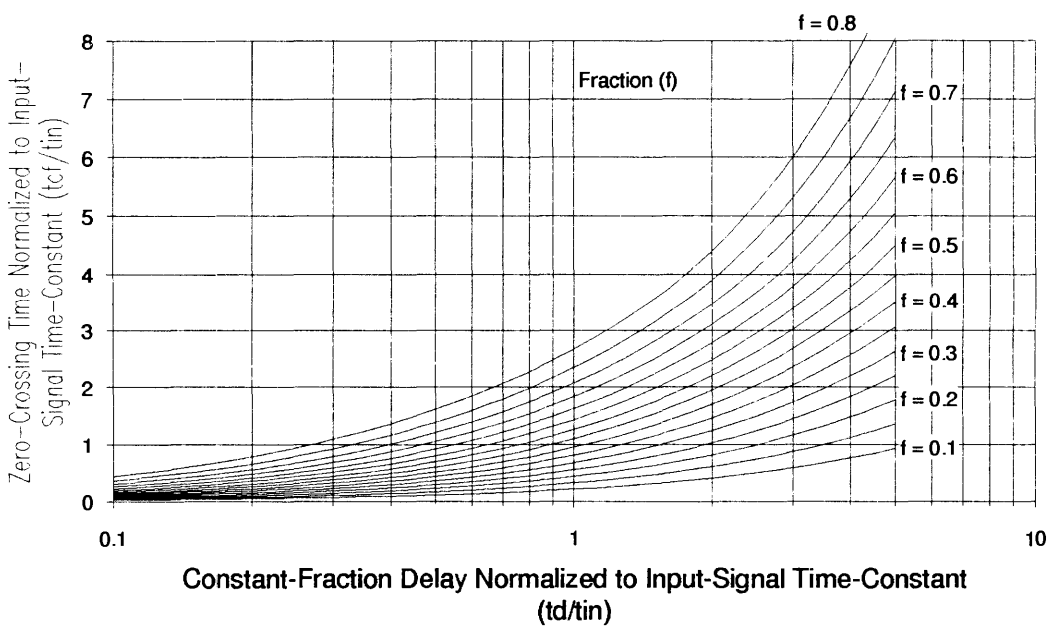


Figure A-14. Binkley Single-Pole Gaussian CFD Zero-Crossing Time for Single-Pole Step Input.

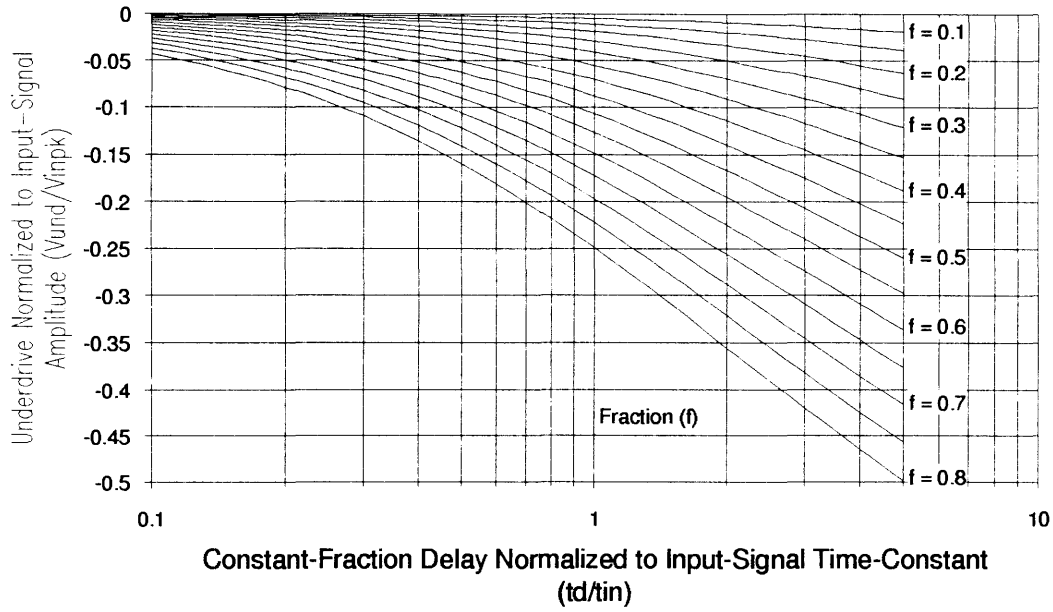


Figure A-15. Binkley Single-Pole Gaussian CFD Underdrive for Single-Pole Step Input.

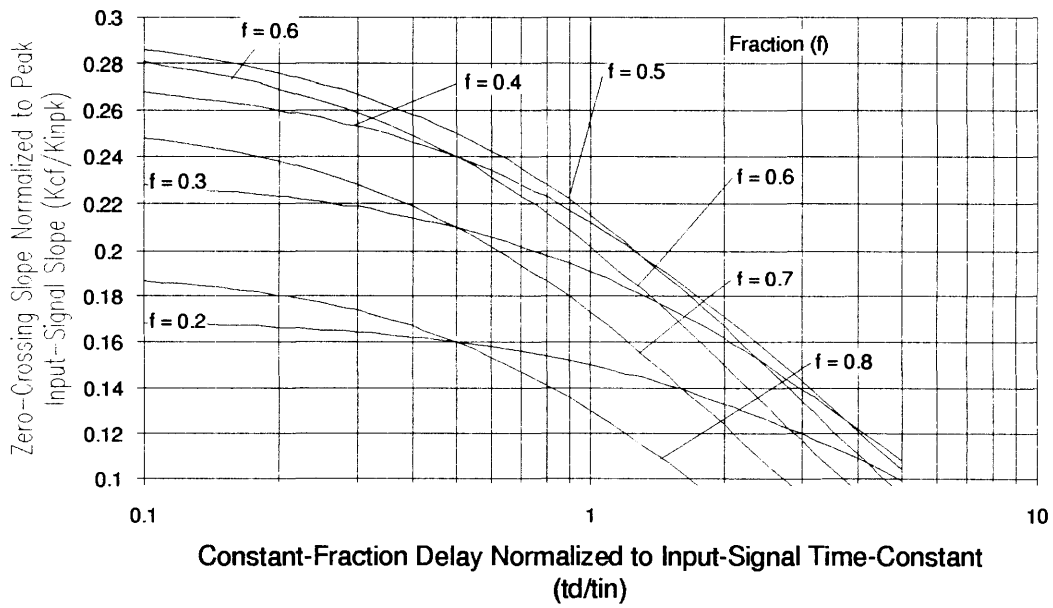


Figure A-16. Binkley Single-Pole Gaussian CFD Zero-Crossing Slope for Single-Pole Step Input.

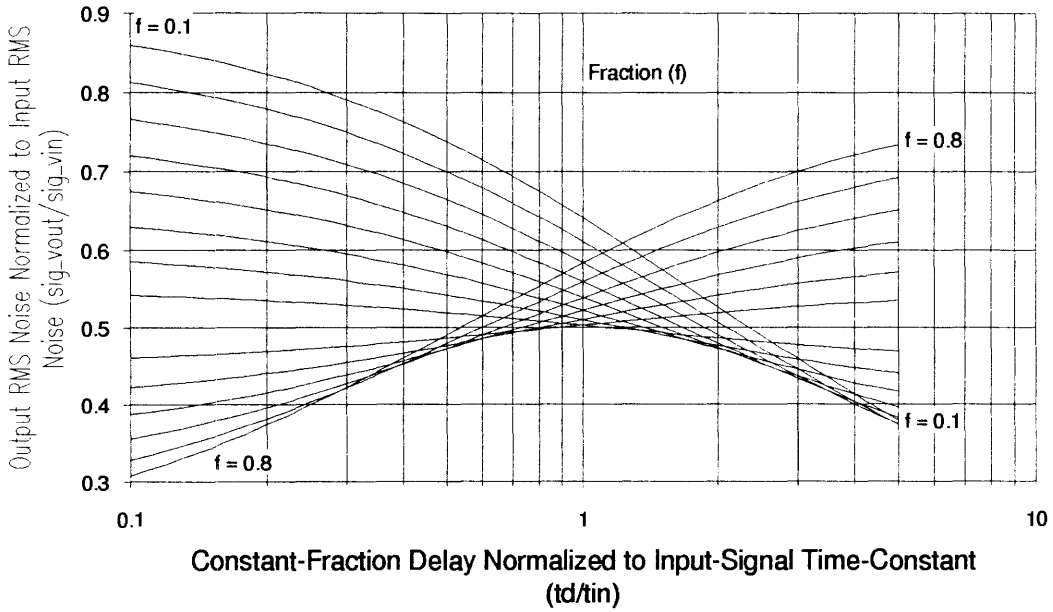


Figure A-17. Binkley Single-Pole Gaussian CFD Noise for Single-Pole Step Input.

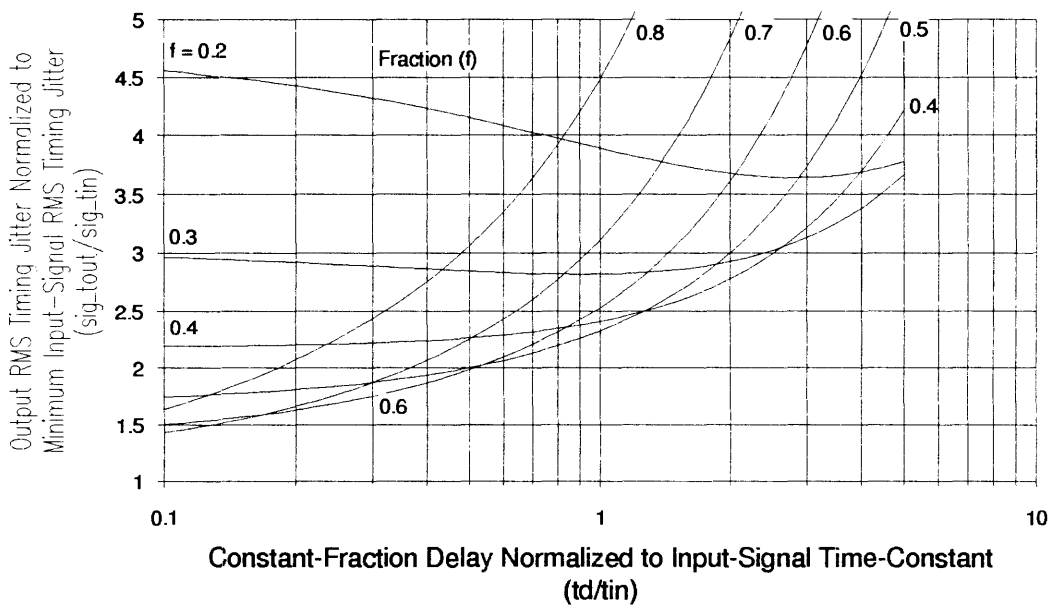


Figure A-18. Binkley Single-Pole Gaussian CFD Timing Jitter for Single-Pole Step Input.

Binkley Single-Pole Gaussian CFD with Two-Pole Step Inputs

Table A-6 contains a directory of figures (data plots) and equations giving performance for the Binkley single-pole Gaussian CFD with two-pole step-input signals. CFD performance is normalized to the input-signal characteristics which are given in Table A-2. The two-pole step-input signal and resulting CFD shaping signal are shown in Figure A-19.

Table A-6. Binkley Single-Pole Gaussian CFD Performance for Two-Pole Step Inputs.

Parameter	**Equation**	**(Eq.)**	**(Fig.)**
Waveform	$v_{cf}(t)$		A-19
Zero-Crossing Time	t_{cf}		A-20
Underdrive	$V_{cf\,(underdrive)}$		A-21
Overdrive	$V_{cf\,(overdrive)} = V_{inpk}(1 - f)$	4-37	
Zero-Crossing Slope	K_{cf}		A-22
Total Noise (rms)	σ_{vcf}		A-23
Timing Jitter (rms)	$\sigma_{tcf} = \frac{\sigma_{vcf}}{K_{cf}}$		A-24

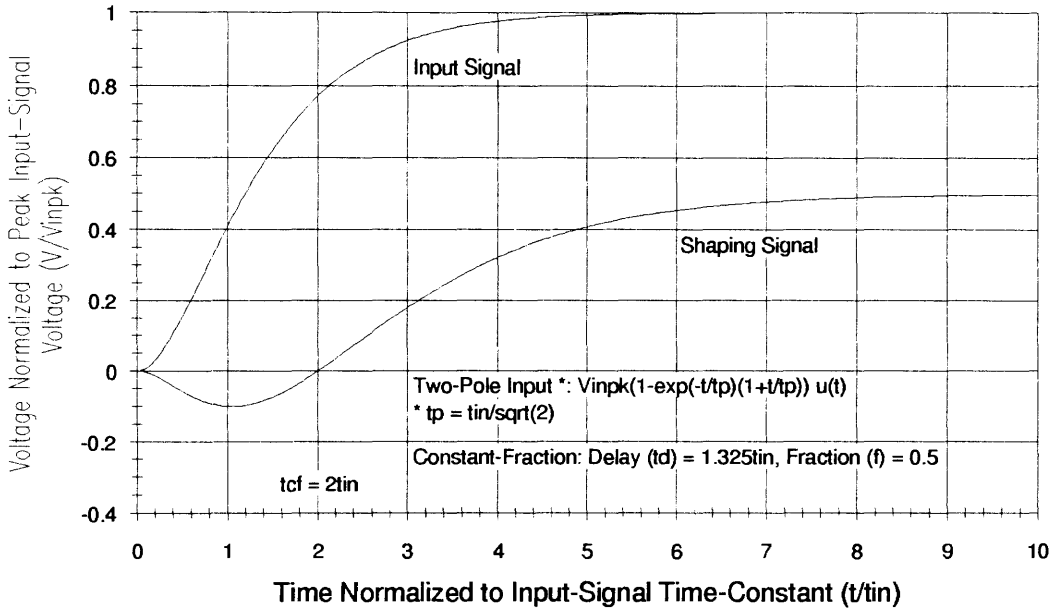


Figure A-19. Binkley Single-Pole Gaussian CFD Shaping Signal for Two-Pole Step Input.

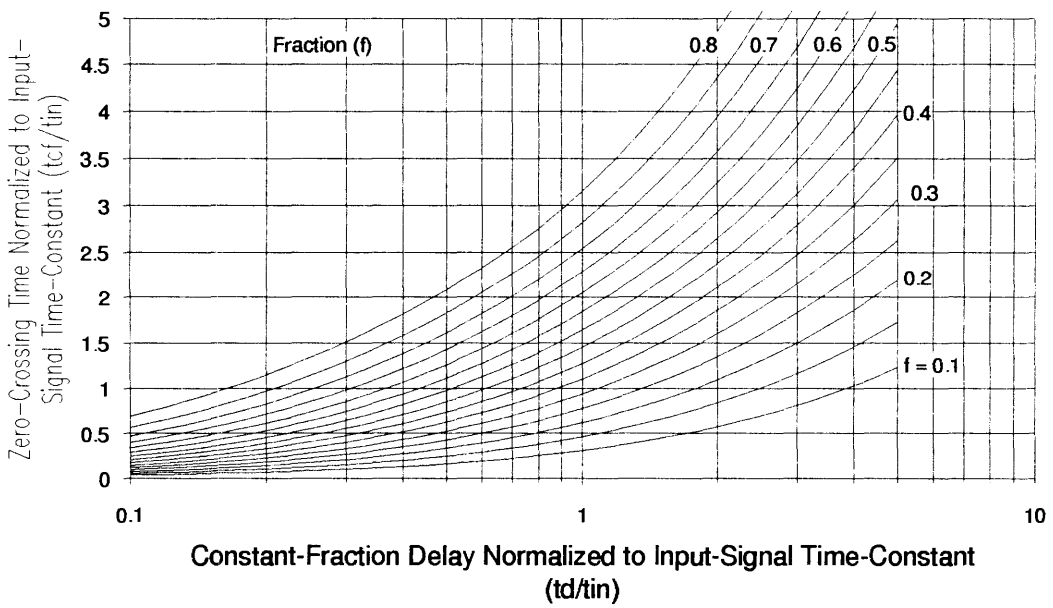


Figure A-20. Binkley Single-Pole Gaussian CFD Zero-Crossing Time for Two-Pole Step Input.

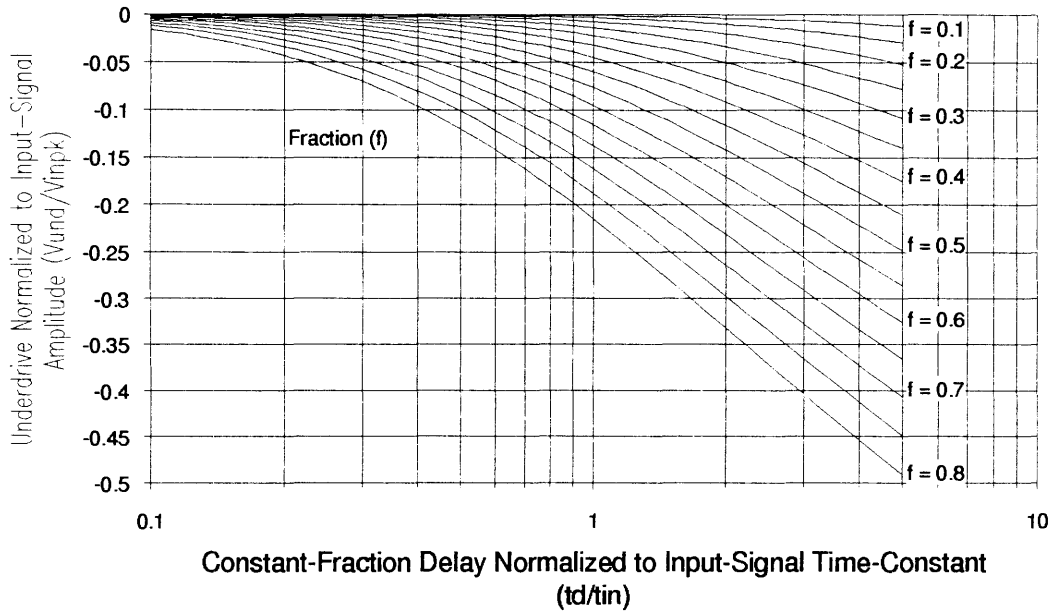


Figure A-21. Binkley Single-Pole Gaussian CFD Underdrive for Two-Pole Step Input.

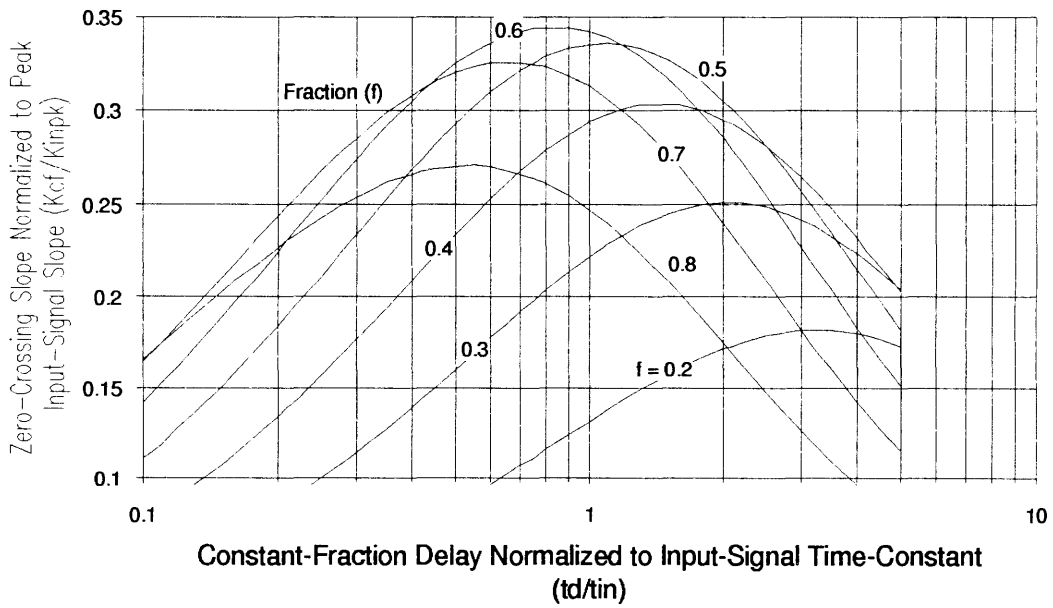


Figure A-22. Binkley Single-Pole Gaussian CFD Zero-Crossing Slope for Two-Pole Step Input.

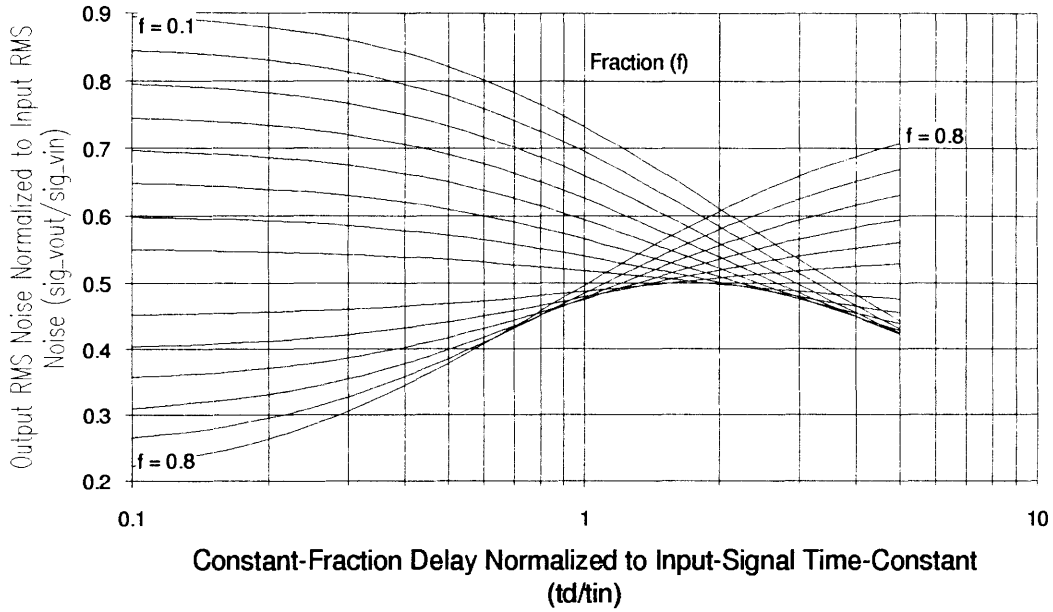


Figure A-23. Binkley Single-Pole Gaussian CFD Noise for Two-Pole Step Input.

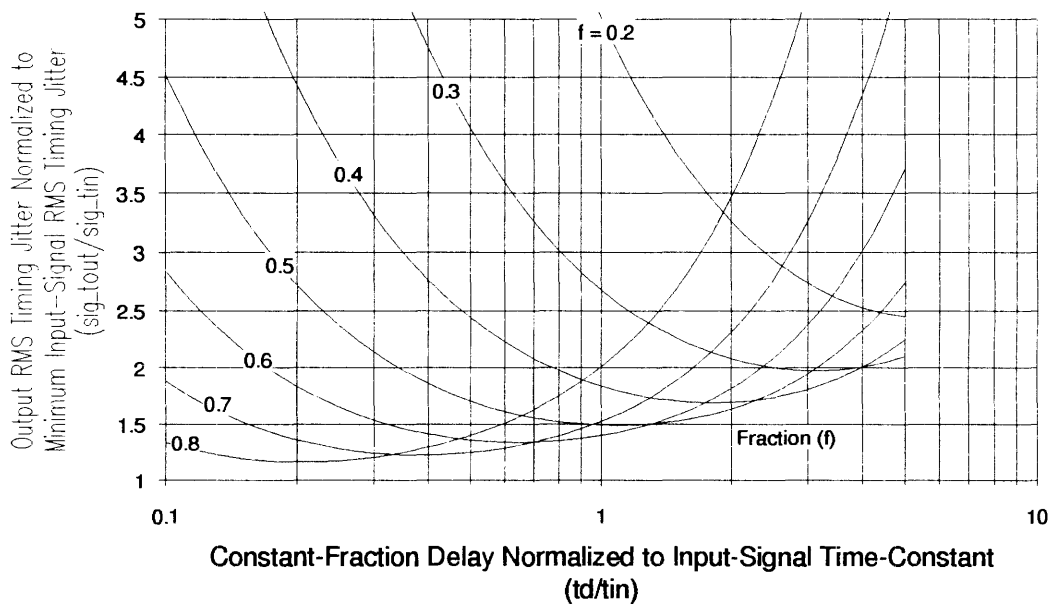


Figure A-24. Binkley Single-Pole Gaussian CFD Timing Jitter for Two-Pole Step Input.

Binkley Two-Pole Gaussian CFD with Single-Pole Step Inputs

Table A-7 contains a directory of figures (data plots) and equations giving performance for the Binkley two-pole Gaussian CFD with single-pole step-input signals. CFD performance is normalized to the input-signal characteristics which are given in Table A-1. The single-pole step-input signal and resulting CFD shaping signal are shown in Figure A-25.

Table A-7. Binkley Two-Pole Gaussian CFD Performance for Single-Pole Step Inputs.

Parameter	**Equation**	**(Eq.)**	**(Fig.)**
Waveform	$v_{cf}(t)$		A-25
Zero-Crossing Time	t_{cf}		A-26
Underdrive	$V_{cf\,(underdrive)}$		A-27
Overdrive	$V_{cf\,(overdrive)} = V_{inpk}(1 - f)$	4-37	
Zero-Crossing Slope	K_{cf}		A-28
Total Noise (rms)	σ_{vcf}		A-29
Timing Jitter (rms)	$\sigma_{tcf} = \frac{\sigma_{vcf}}{K_{cf}}$		A-30

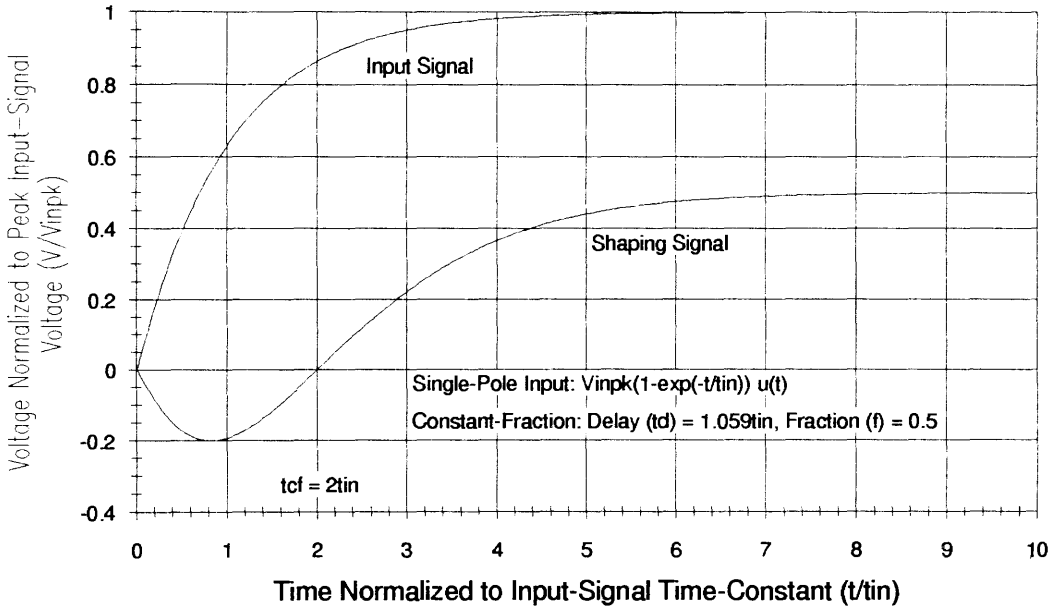


Figure A-25. Binkley Two-Pole Gaussian CFD Shaping Signal for Single-Pole Step Input.

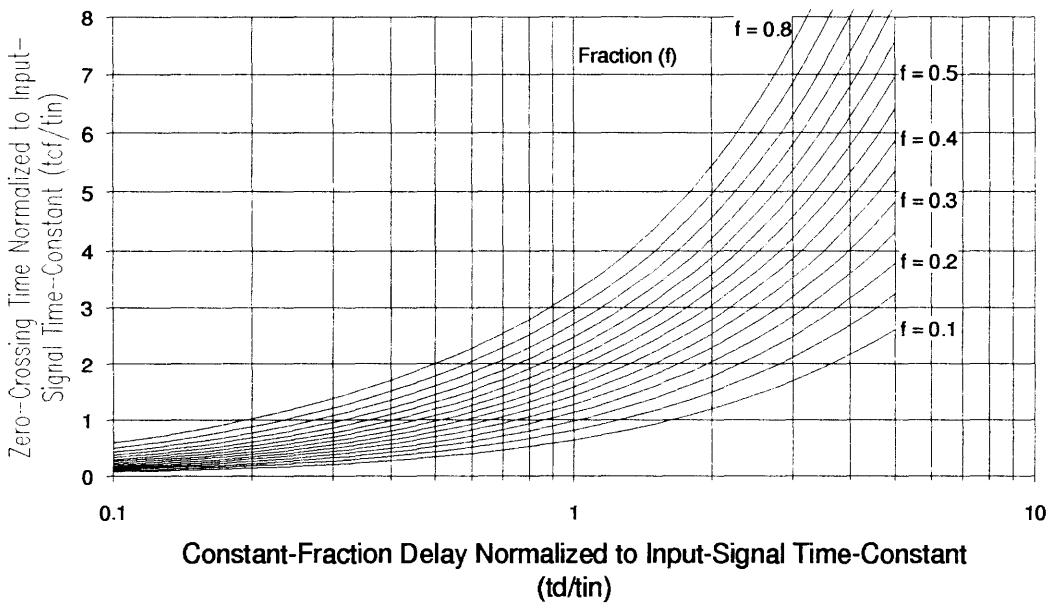


Figure A-26. Binkley Two-Pole Gaussian CFD Zero-Crossing Time for Single-Pole Step Input.

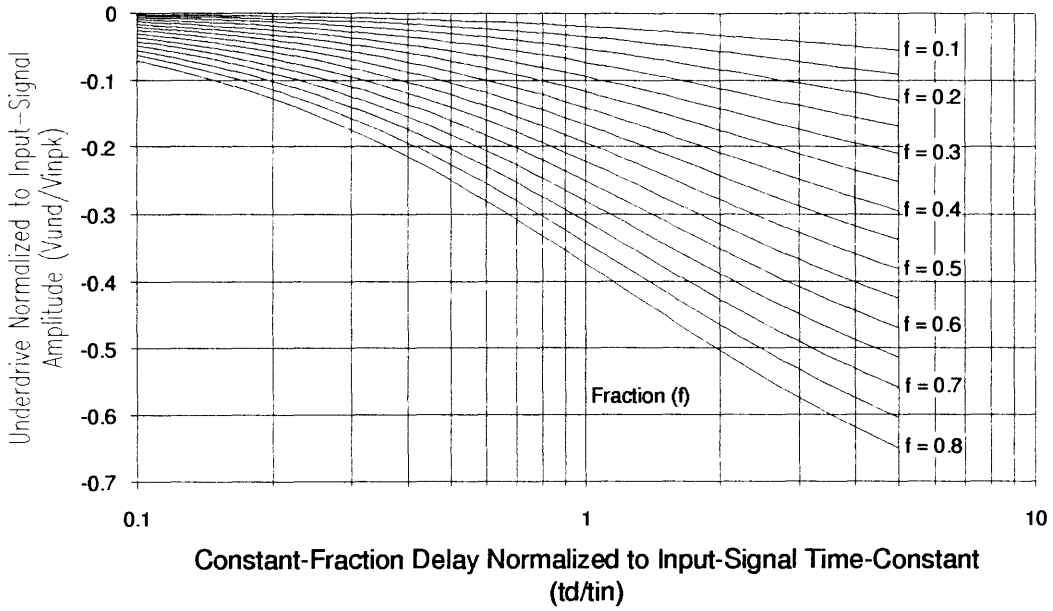


Figure A-27. Binkley Two-Pole Gaussian CFD Underdrive for Single-Pole Step Input.

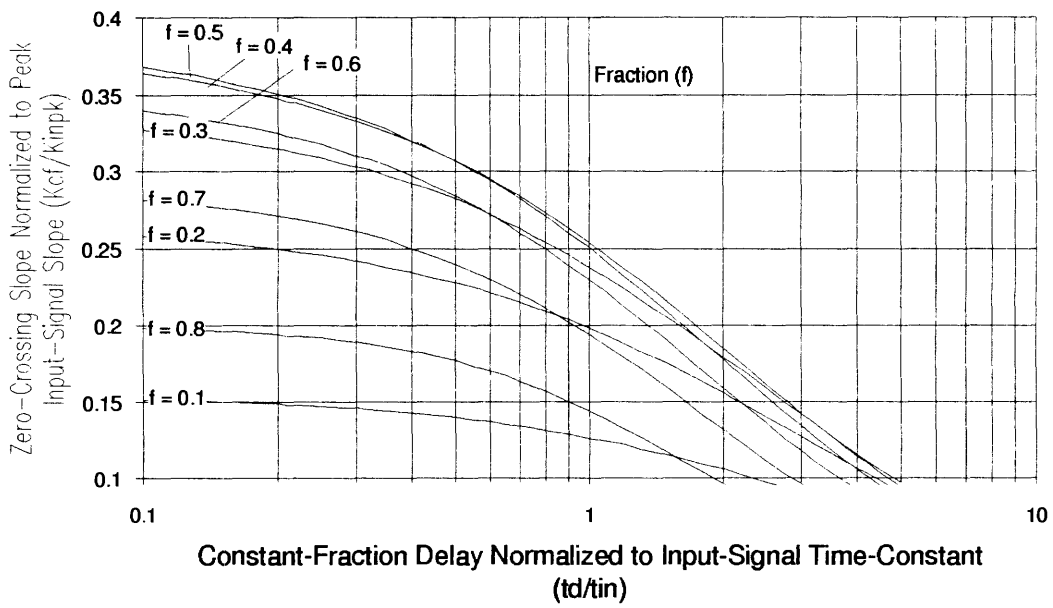


Figure A-28. Binkley Two-Pole Gaussian CFD Zero-Crossing Slope for Single-Pole Step Input.

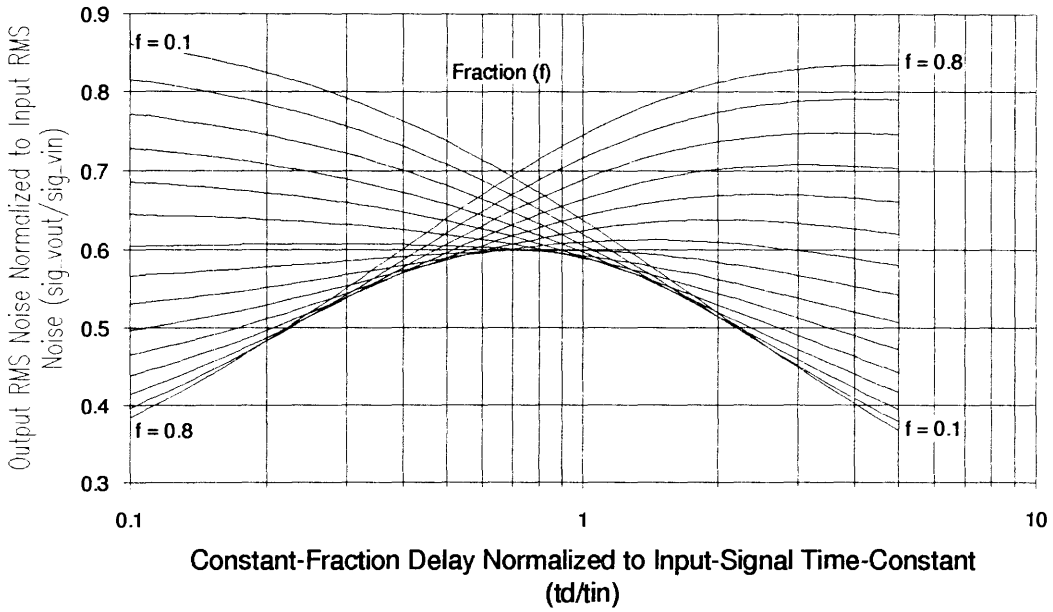


Figure A-29. Binkley Two-Pole Gaussian CFD Noise for Single-Pole Step Input.

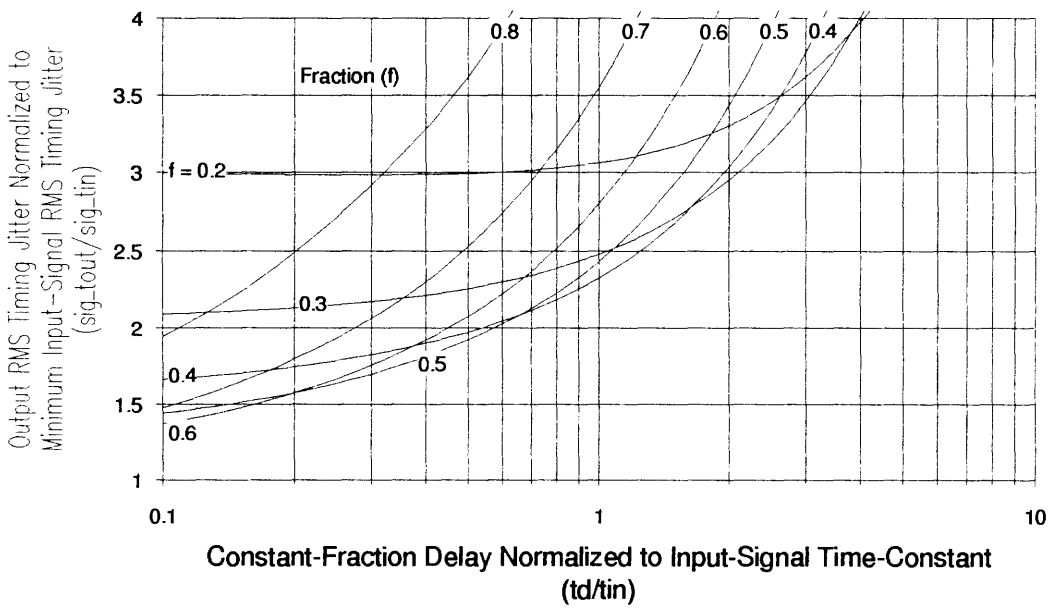


Figure A-30. Binkley Two-Pole Gaussian CFD Timing Jitter for Single-Pole Step Input.

Binkley Two-Pole Gaussian CFD with Two-Pole Step Inputs

Table A-8 contains a directory of figures (data plots) and equations giving performance for the Binkley two-pole Gaussian CFD with two-pole step-input signals. CFD performance is normalized to the input-signal characteristics which are given in Table A-2. The two-pole step-input signal and resulting CFD shaping signal are shown in Figure A-31.

Table A-8. Binkley Two-Pole Gaussian CFD Performance for Two-Pole Step Inputs.

Parameter	Equation	(Eq.)	(Fig.)
Waveform	$v_{cf}(t)$		A-31
Zero-Crossing Time	t_{cf}		A-32
Underdrive	$V_{cf\,(underdrive)}$		A-33
Overdrive	$V_{cf\,(overdrive)} = V_{inpk}(1 - f)$	4-37	
Zero-Crossing Slope	K_{cf}		A-34
Total Noise (rms)	σ_{vcf}		A-35
Timing Jitter (rms)	$\sigma_{tcf} = \frac{\sigma_{vcf}}{K_{cf}}$		A-36

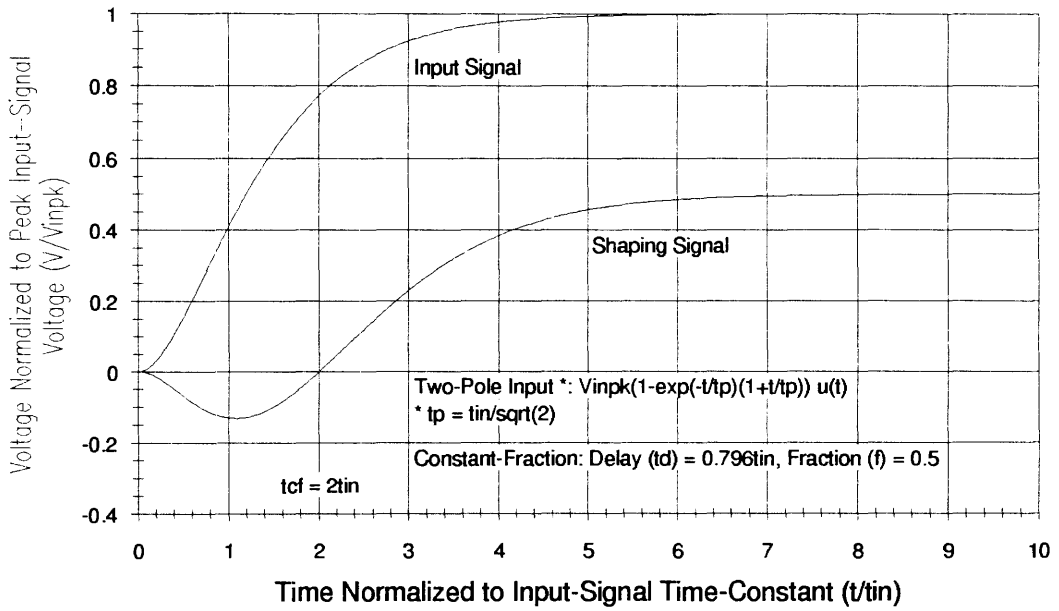


Figure A-31. Binkley Two-Pole Gaussian CFD Shaping Signal for Two-Pole Step Input.

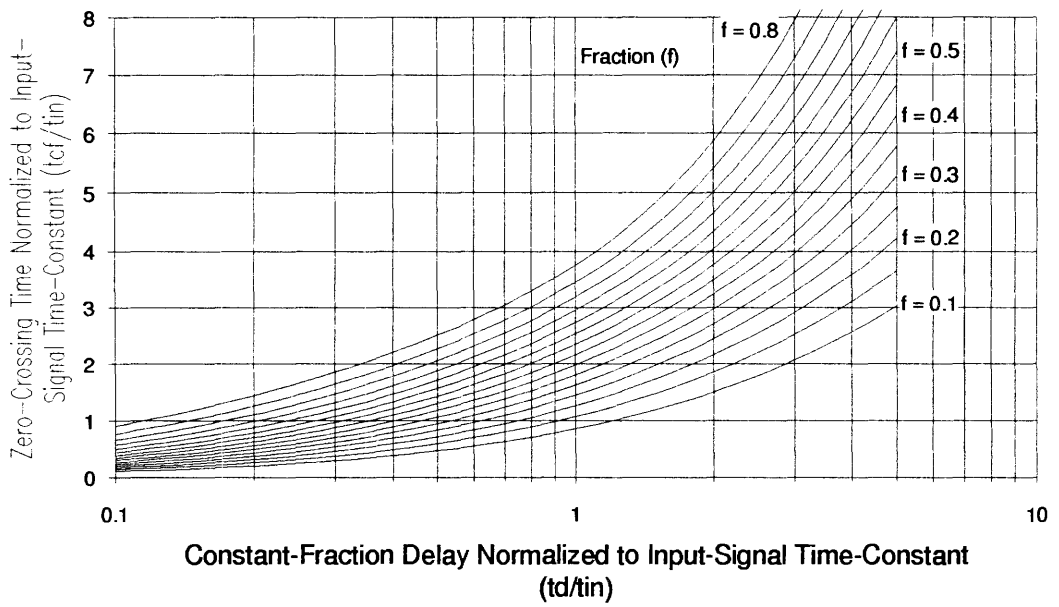


Figure A-32. Binkley Two-Pole Gaussian CFD Zero-Crossing Time for Two-Pole Step Input.

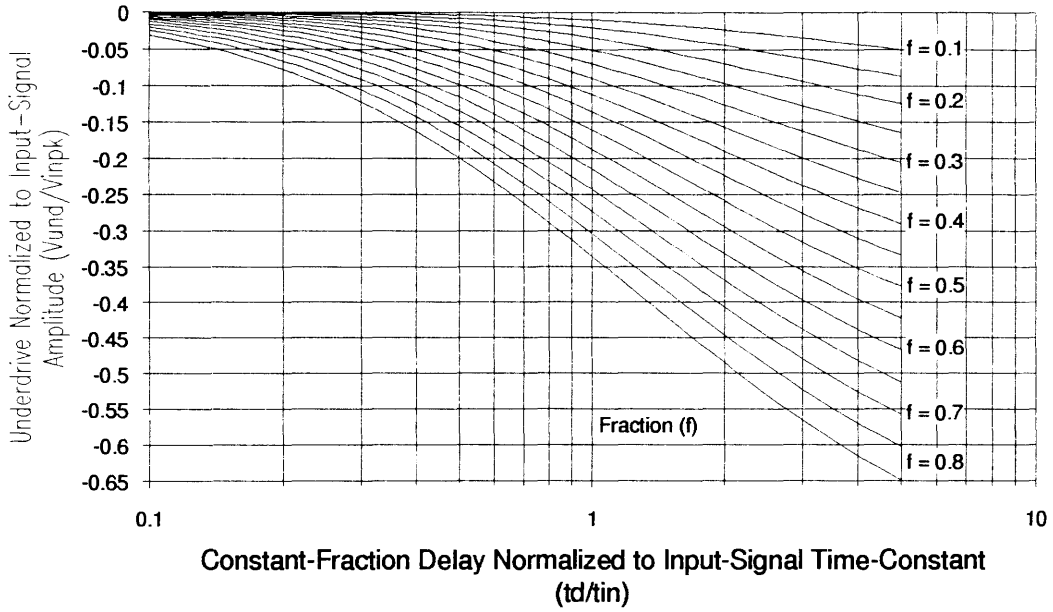


Figure A-33. Binkley Two-Pole Gaussian CFD Underdrive for Two-Pole Step Input.

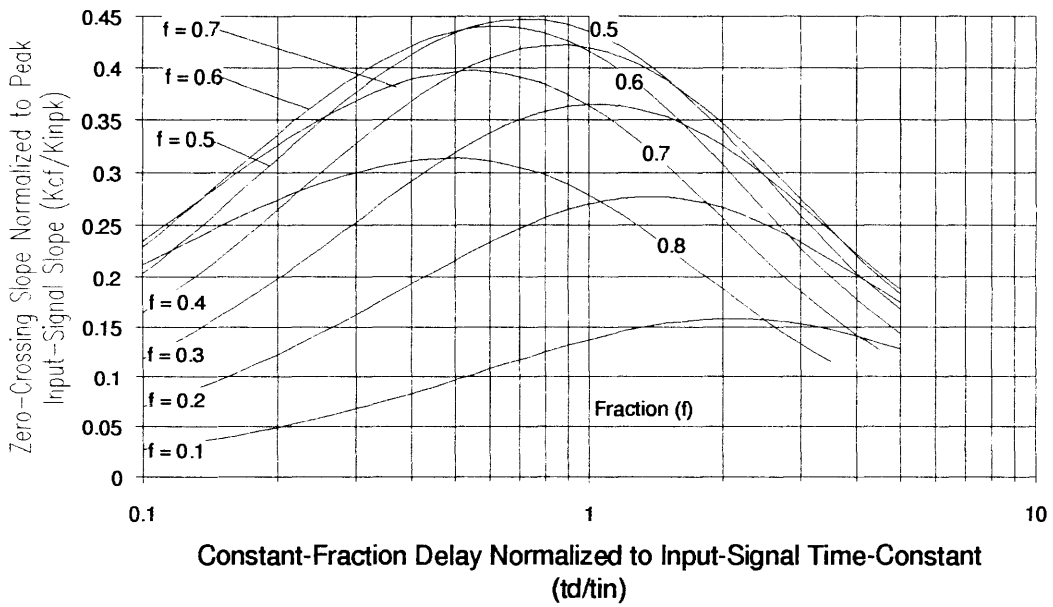


Figure A-34. Binkley Two-Pole Gaussian CFD Zero-Crossing Slope for Two-Pole Step Input.

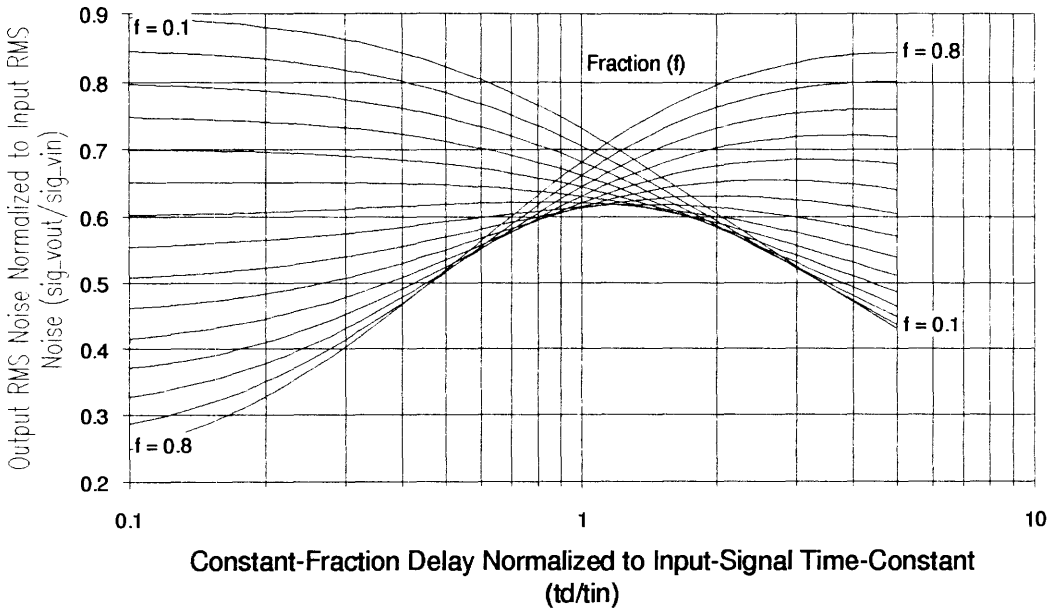


Figure A-35. Binkley Two-Pole Gaussian CFD Noise for Two-Pole Step Input.

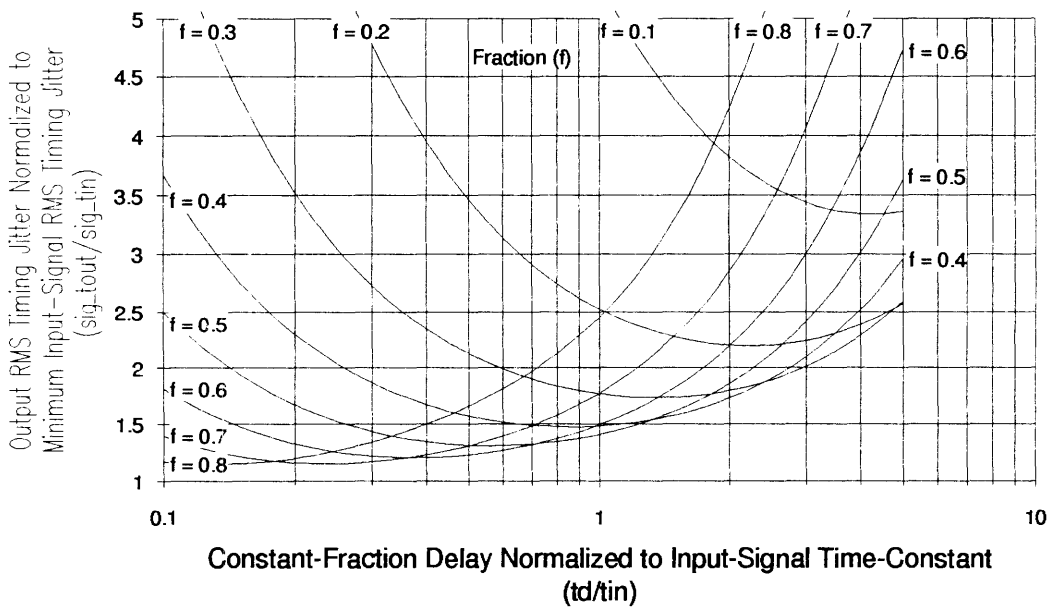


Figure A-36. Binkley Two-Pole Gaussian CFD Timing Jitter for Two-Pole Step Input.

Binkley Four-Pole Gaussian CFD with Single-Pole Step Inputs

Table A-9 contains a directory of figures (data plots) and equations giving performance for the Binkley four-pole Gaussian CFD with single-pole step-input signals. CFD performance is normalized to the input-signal characteristics which are given in Table A-1. The single-pole step-input signal and resulting CFD shaping signal are shown in Figure A-37.

Table A-9. Binkley Four-Pole Gaussian CFD Performance for Single-Pole Step Inputs.

Parameter	Equation	(Eq.)	(Fig.)
Waveform	$v_{cf}(t)$		A-37
Zero-Crossing Time	t_{cf}		A-38
Underdrive	$V_{cf\,(underdrive)}$		A-39
Overdrive	$V_{cf\,(overdrive)} = V_{inpk}(1 - f)$	4-37	
Zero-Crossing Slope	K_{cf}		A-40
Total Noise (rms)	σ_{vcf}		A-41
Timing Jitter (rms)	$\sigma_{tcf} = \frac{\sigma_{vcf}}{K_{cf}}$		A-42

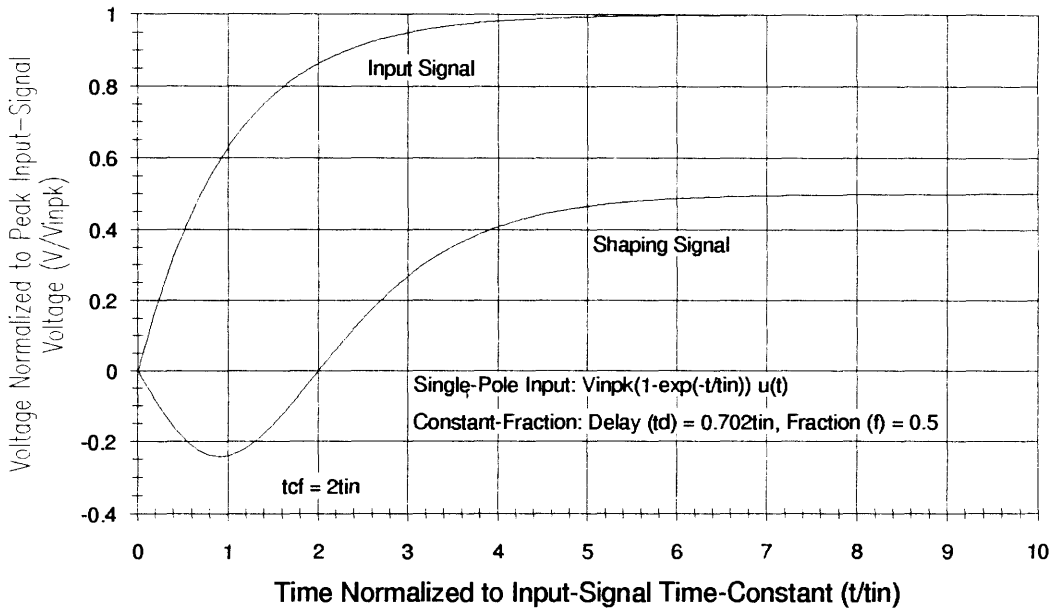


Figure A-37. Binkley Four-Pole Gaussian CFD Shaping Signal for Single-Pole Step Input.

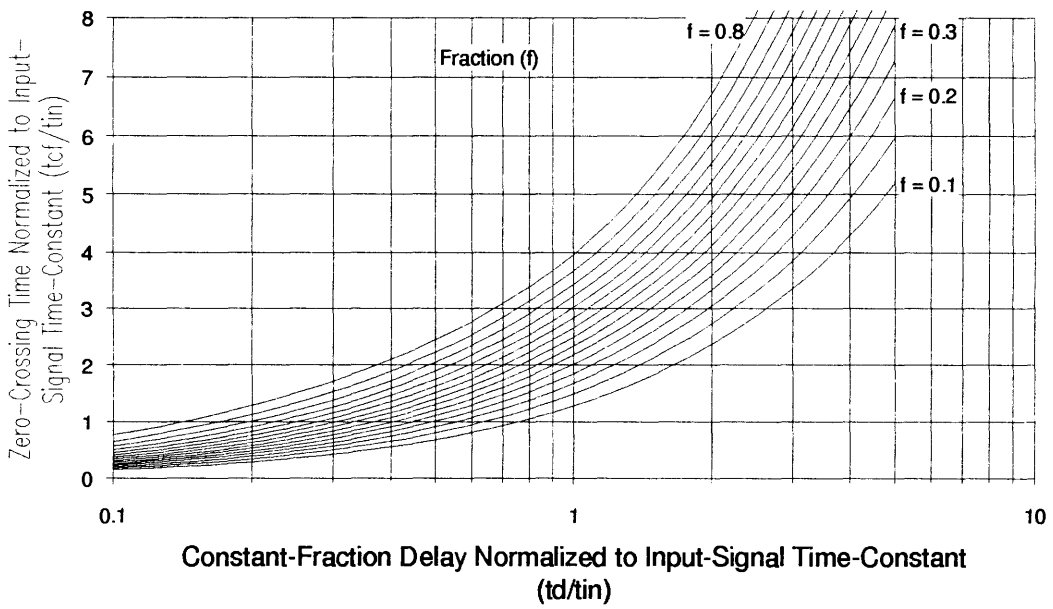


Figure A-38. Binkley Four-Pole Gaussian CFD Zero-Crossing Time for Single-Pole Step Input.

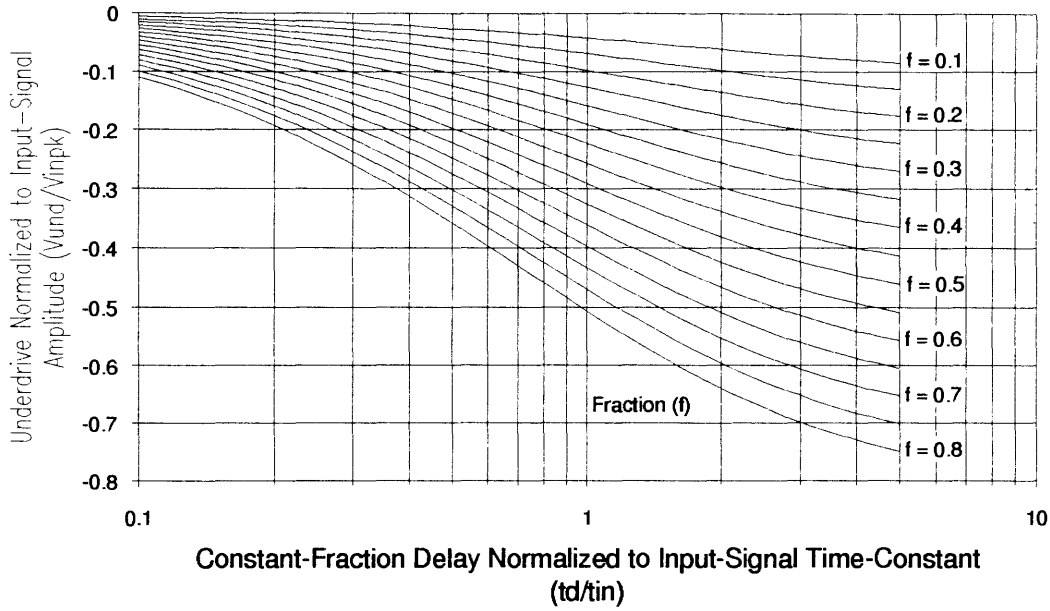


Figure A-39. Binkley Four-Pole Gaussian CFD Underdrive for Single-Pole Step Input.

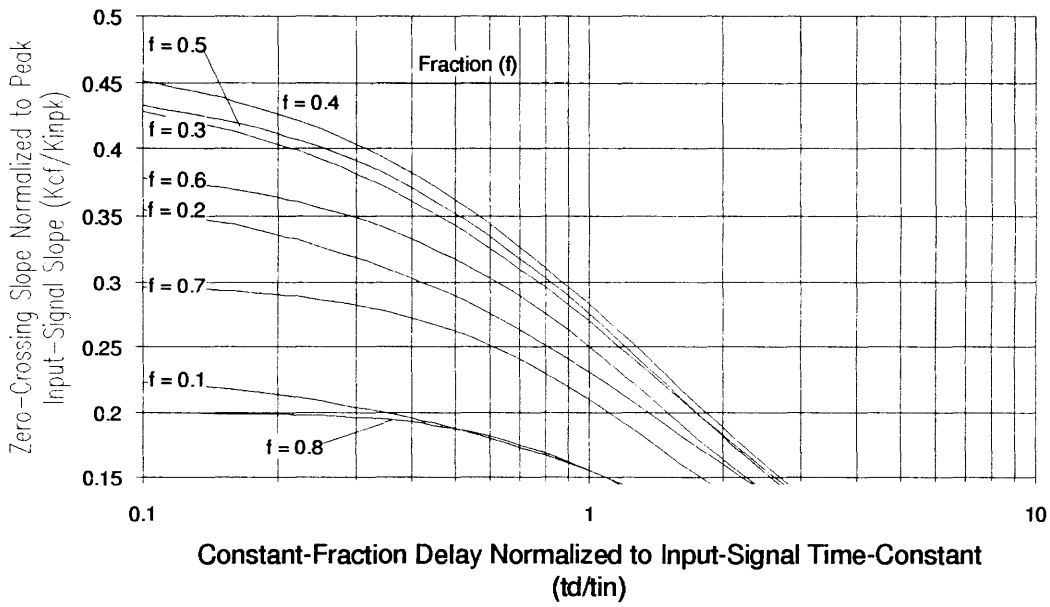


Figure A-40. Binkley Four-Pole Gaussian CFD Zero-Crossing Slope for Single-Pole Step Input.

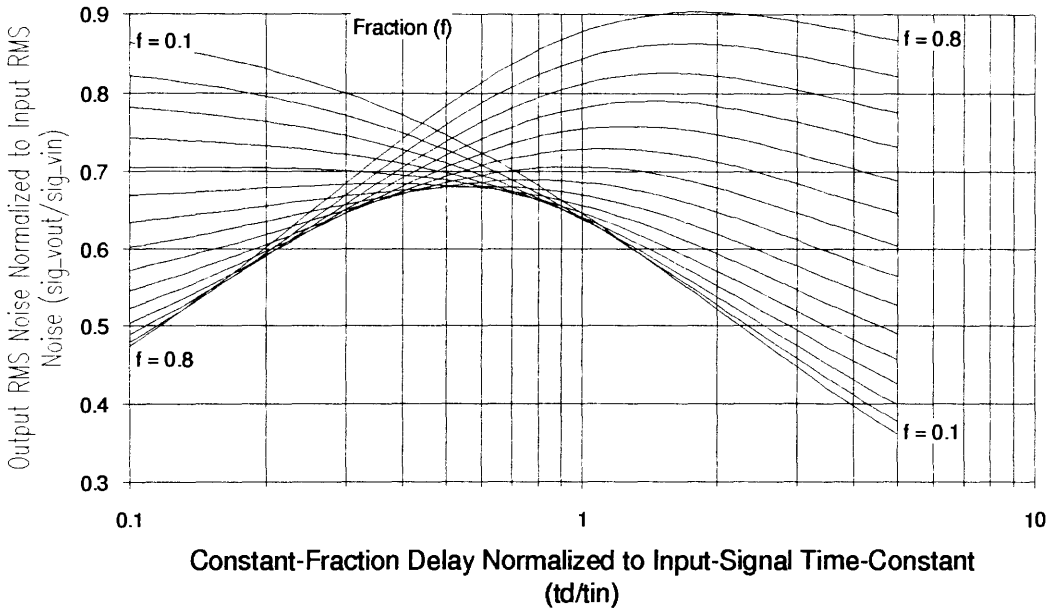


Figure A-41. Binkley Four-Pole Gaussian CFD Noise for Single-Pole Step Input.

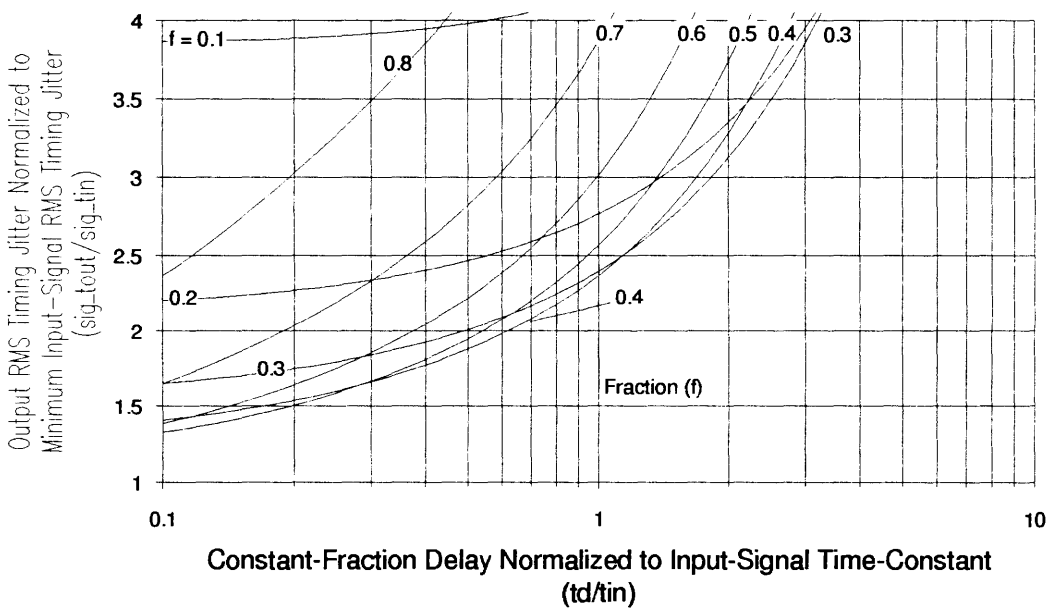


Figure A-42. Binkley Four-Pole Gaussian CFD Timing Jitter for Single-Pole Step Input.

Binkley Four-Pole Gaussian CFD with Two-Pole Step Inputs

Table A-10 contains a directory of figures (data plots) and equations giving performance for the Binkley four-pole Gaussian CFD with two-pole step-input signals. CFD performance is normalized to the input-signal characteristics which are given in Table A-2. The two-pole step-input signal and resulting CFD shaping signal are shown in Figure A-43.

Table A-10. Binkley Four-Pole Gaussian CFD Performance for Two-Pole Step Inputs.

Parameter	Equation	(Eq.)	(Fig.)
Waveform	$v_{cf}(t)$		A-43
Zero-Crossing Time	t_{cf}		A-44
Underdrive	$V_{cf\,(underdrive)}$		A-45
Overdrive	$V_{cf\,(overdrive)} = V_{inpk}(1 - f)$	4-37	
Zero-Crossing Slope	K_{cf}		A-46
Total Noise (rms)	σ_{vcf}		A-47
Timing Jitter (rms)	$\sigma_{tcf} = \frac{\sigma_{vcf}}{K_{cf}}$		A-48

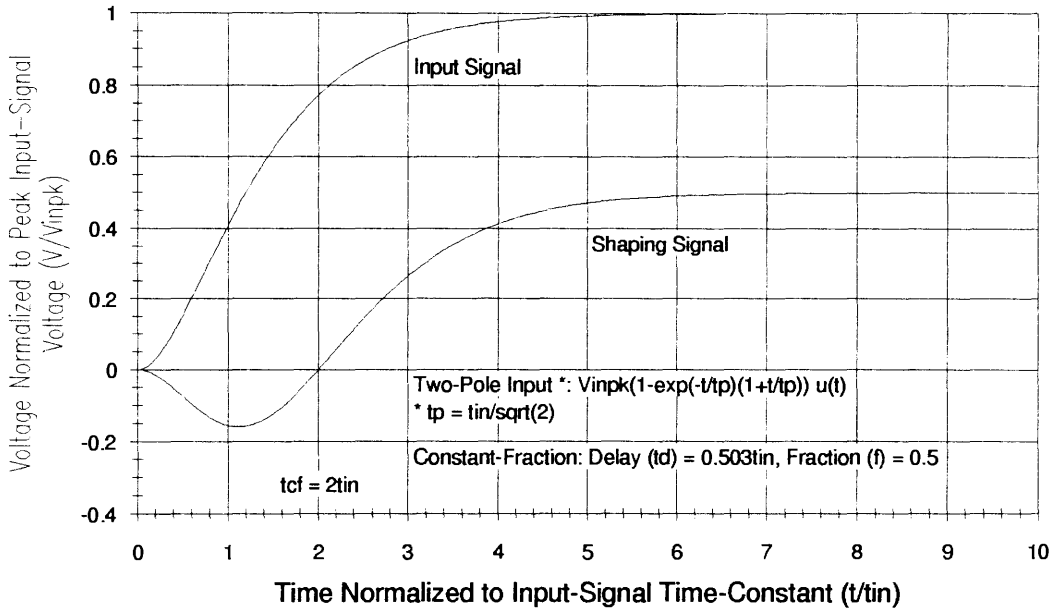


Figure A-43. Binkley Four-Pole Gaussian CFD Shaping Signal for Two-Pole Step Input.

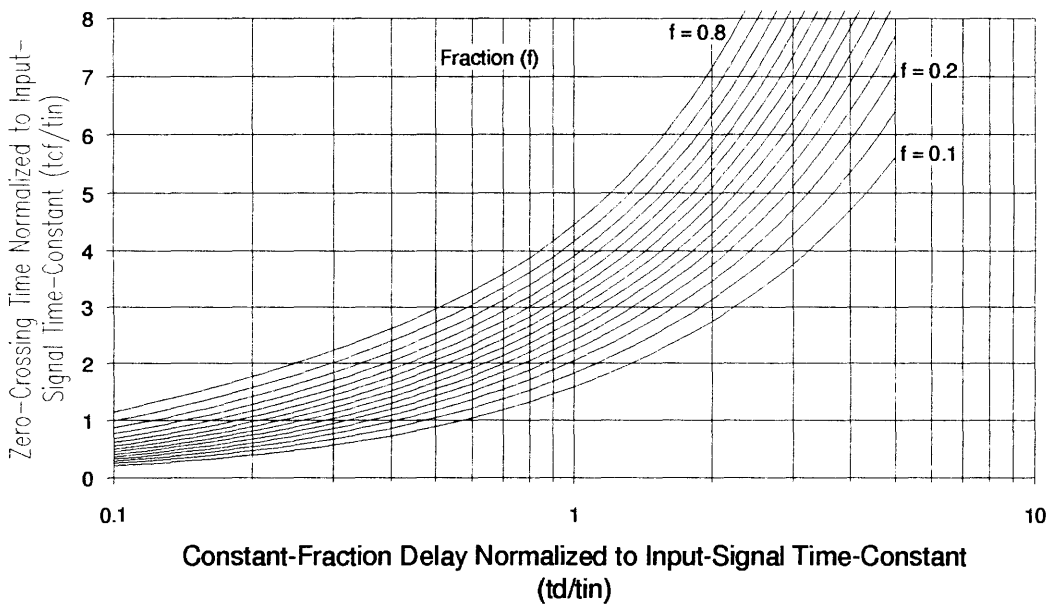


Figure A-44. Binkley Four-Pole Gaussian CFD Zero-Crossing Time for Two-Pole Step Input.

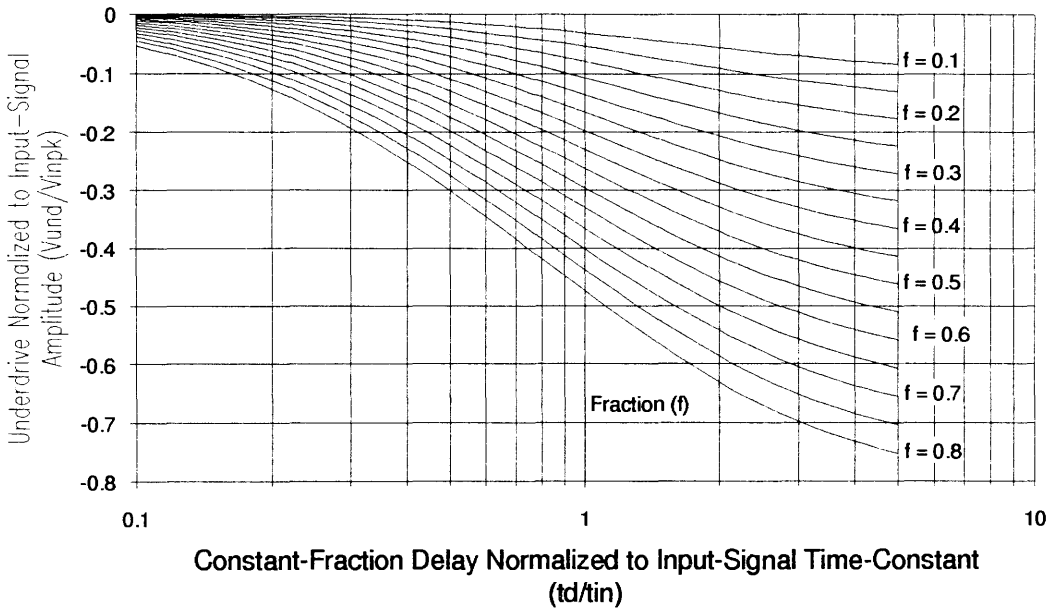


Figure A-45. Binkley Four-Pole Gaussian CFD Underdrive for Two-Pole Step Input.

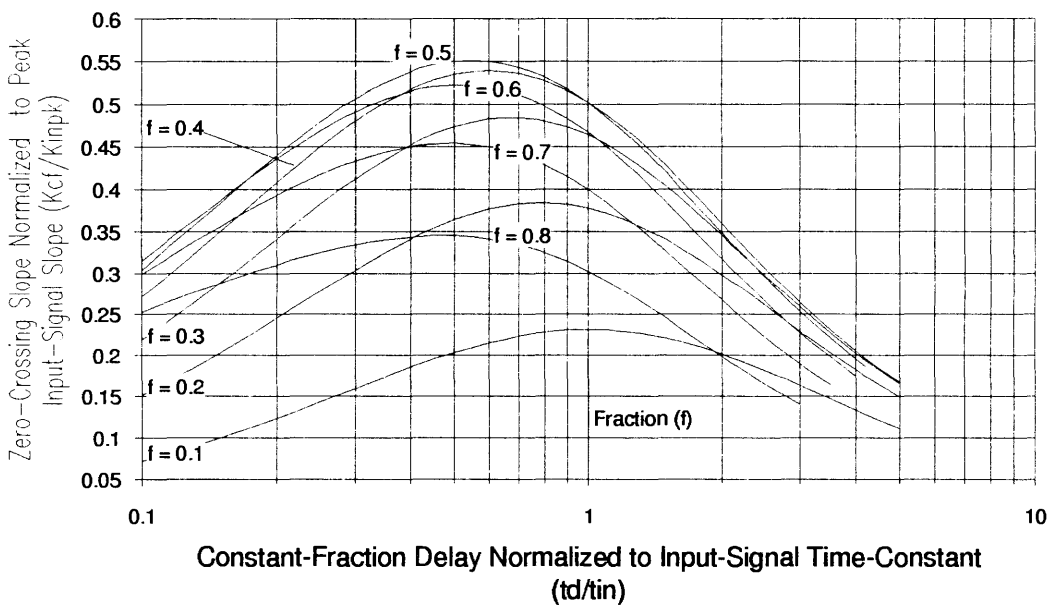


Figure A-46. Binkley Four-Pole Gaussian CFD Zero-Crossing Slope for Two-Pole Step Input.

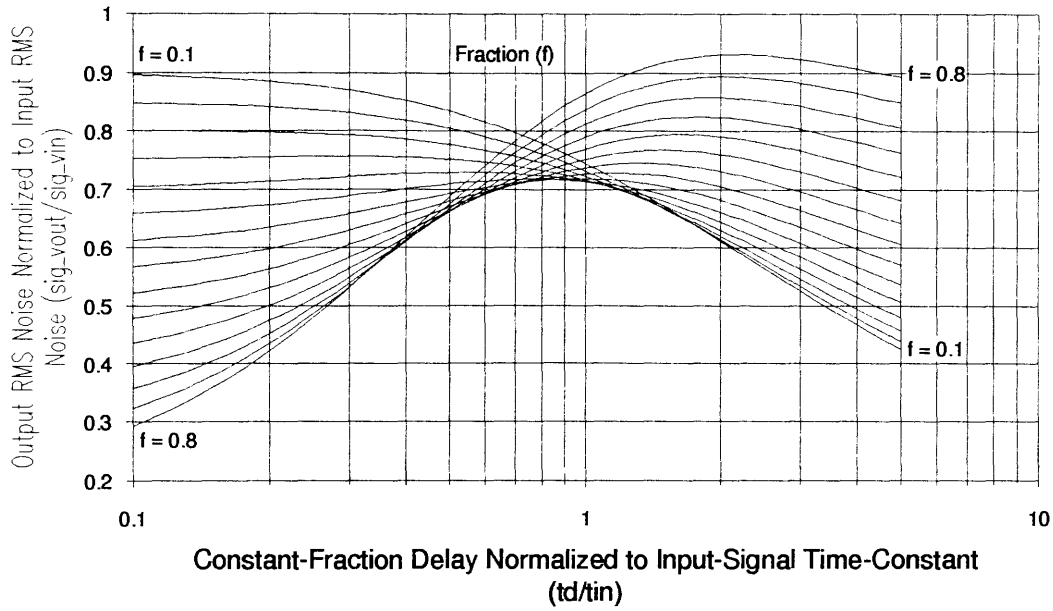


Figure A-47. Binkley Four-Pole Gaussian CFD Noise for Two-Pole Step Input.

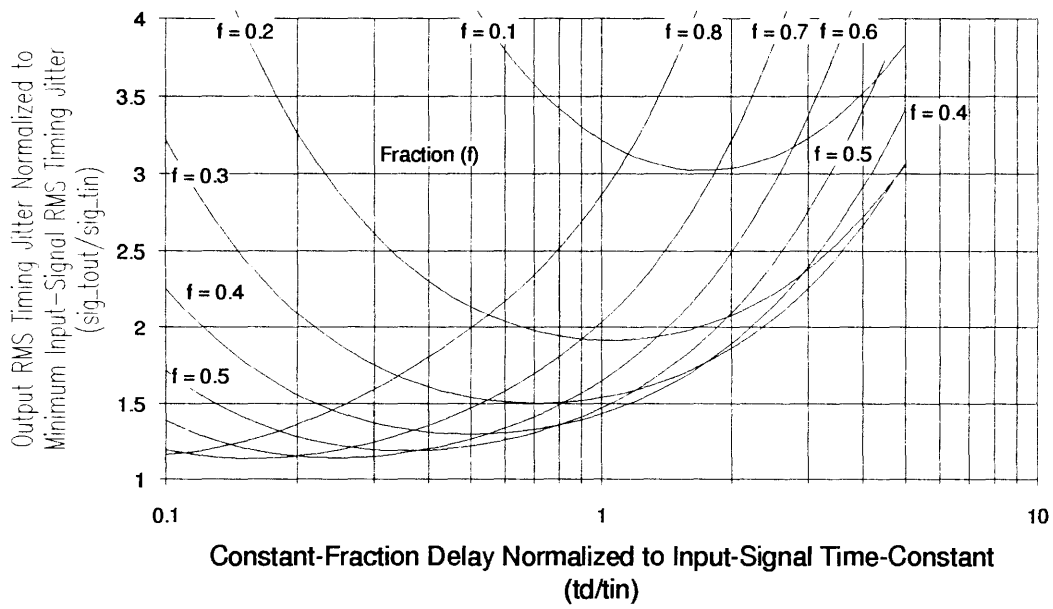


Figure A-48. Binkley Four-Pole Gaussian CFD Timing Jitter for Two-Pole Step Input.

APPENDIX B. MONTE CARLO TIMING ANALYSIS PROGRAM

```
/* cfdmont.c

   This program generates a CFD (or leading-edge) timing spectrum using
   Monte Carlo analysis.  The program assumes a Poisson detector impulse
   distribution in time, a Gaussian detector energy spectrum, a
   Gaussian PMT transit time spectrum, a Gaussian PMT single-electron
   gain spectrum, and a PMT/electronics impulse response that is in the
   form of a lookup table.  The program finds the threshold crossing times
   of the CFD (or leading-edge) signal from the PMT/electronics system to
   evaluate the timing spectrum.  Multiple spectra are provided by the
   program:  the detector energy spectrum, the detector timing spectrum,
   the PMT transit time spectrum, the PMT single-electron gain spectrum,
   the coincidence spectrum for two detectors, and the coincidence
   spectrum for the detector against a plastic detector.  Additionally,
   the voltage-underdrive spectrum is found along with the zero-crossing-
   slope spectrum.  Both raw spectra (identical to MCA spectra) and filtered
   spectra are outputted to a file for reading by the MicroSoft Excel
   spreadsheet program.  Finally, the filtered spectra are analyzed and their
   centroid, half channels, and tenth channels reported in the report file.

   The detector energy spectrum can include Compton scatter by the selection
   of a flag.  All energies above a selected energy threshold will be used
   for Monte Carlo timing analysis to simulate CFD (or leading-edge) energy
   qualification (see cfdmont1.c for full CFD energy qualification analysis).


   Dave Binkley, 11-05-92 Revision; Added triexponential BGO scintillation
                                    model.

   Dave Binkley, 10-19-92 Revision; Added Compton scatter and energy thld.

   Dave Binkley, 6-18-92 Revision; Added voltage-underdrive spectrum and
                                   zero-crossing-slope spectrum.
   Dave Binkley, 8-26-91

*/

#include <stdio.h>
#include <ctype.h>
#include <math.h>
#include <string.h>

/* ********** Program Parameters ************************************ */

#define SPICE_IMPULSE_RESPONSE_PRINT_FILE    "cfdnetm.tmp"
#define REPORT_FILE_FOR_SPECTRA              "cfdmont.xls"

#define KLIMIT 1000     /* Maximum number of Poisson points permitted */
#define ILIMIT 3001     /* maximum number of time data points per event */
#define TSTEP 10e-12    /* time step size used - MUST MATCH STEP SIZE USED
                             IN IMPULSE RESPONSE LOOKUP TABLE */
#define TEND 30e-9      /* ending time for producing poisson time points */

#define VTHRESHOLD 0.0     /* threshold voltage for timing crossing */
#define EPSILON    100e-6  /* amount signal must go below (negative) from
                              threshold prior to a threshold crossing */
```

```
#define PHE_YIELD_511KEV 300.0     /* number of photoelectrons per
                                        511 keV event (floating point) */
#define TAU1             300e-9    /* primary scint. decay time constant */
#define TAU1_YIELD       0.9       /* yield (0.0 - 1.0) of primary decay */
#define TAU2             60e-9     /* secondary scint. decay time constant */
#define TAU2_YIELD       0.1       /* yield (0.0 - 1.0) of secondary decay */
#define TAURISE          1.5e-9    /* scint. rise time time constant */

#define SIGMA_ENERGY     0.06      /* FWHM = 2.35*sigma */
#define MEAN_ENERGY      1.0       /* mean energy is 1.0 (for 511 keV) */

#define SIGMA_PMTDELAY   0.298e-9  /* FWHM = 2.35*sigma */
#define MEAN_PMTDELAY    5e-9      /* mean pmt delay */

#define SIGMA_PMTSER     0.694     /* FWHM = 2.35*sigma */
#define MEAN_PMTSER      1.0       /* mean pmt SER */

#define SIGMA_PLAST      63.8e-12  /* FWHM = 2.35*sigma */
#define MEAN_PLAST       0.0       /* mean plastic detector delay */

#define FLAG_COMPTON_SCATTER 1     /* 1 for Compton scatter, 0 otherwise */
#define PHOTOFRACTION    0.54      /* Photofraction for BGO scintillator */
#define SCATTERFRACTION  0.00      /* 0.00 for needle source, 0.32 for 20cm
                                        water-filled phantom */
#define SCATTERKNEE      0.88      /* knee of scatter relative to mean energy
                                        of 1.0 */

#define PHOTOPEAK_KEV    511.0     /* photopeak energy in keV (norm. 1.0) */
#define ENERGY_THLD_KEV  200.0     /* energy threshold in keV */

#define NEVENTS          100000    /* number of events to be histogrammed */


/* SEE INITIALIZATION OF MCA STRUCTURES FOR MCA SETUP VALUES */

#define MCA_CHANNELS_MAX 10000     /* maximum number of MCA channels */
#define MCA_TITLE_MAX    100       /* maximum character length of MCA title */
#define MCA_LABEL_MAX    100       /* maximum character length of MCA label */


/* Flag Assignments */

#define TRUE 1              /* assignments for flags */
#define FALSE 0             /* assignments for flags */


/* ************* Data Structure for MCAs ********************************** */

struct mca
  {
    int raw[MCA_CHANNELS_MAX];   /* mca array (raw data), indexed 0,1,2 */
    float fil[MCA_CHANNELS_MAX]; /* mca array (filtered data), floating pt
                                    used for filtered result */

    /* The following values must be inputted */

    float begin;                        /* beginning value of mca */
    float end;                          /* ending value of mca */
    float ch_wid;                       /* channel width */
```

```
    float ch_units;                     /* output listing channel units */
    int fil_nos;                        /* number of points used on each
                                           side of point for filtering */
    float fil_sig;                      /* value of sigma (chs) for Gaussian
                                           filtering */
    char title[MCA_TITLE_MAX];          /* title for mca */
    char label[MCA_LABEL_MAX];          /* label for mca channel, counts */

    /* The following values are computed */

    int ch_nos;                         /* number of mca channels */
    int nos_in;                         /* counts in mca */
    int nos_out;                        /* counts outside of mca */

    /* The following computed values describe the characteristics of the
         filtered spectrum; locations are in units defined by ch_units */

    float cent;                         /* location of centroid (peak) ch */
    float cent_cnts;                    /* centroid ch counts */
    float halfl;                        /* location of low 1/2 ch */
    float halfh;                        /* location of high 1/2 ch */
    float fwhm;                         /* FWHM of spectrum */
    float tenthl;                       /* location of low 1/10 ch */
    float tenthh;                       /* location of high 1/10 ch */
    float fwtm;                         /* FWTM of spectrum */
  }


/* ************************************************************************ */
/* ************* Beginning of Main() ************************************** */
/* ************************************************************************ */

main ()

{
   /* MCA structures for timing, energy, and single-electron gain spectra */

   struct mca mca_tdet;       /* Detector (single) timing spectrum */
   struct mca mca_tplas;      /* Plastic detector (single) timing spectrum */
   struct mca mca_tplasdet;   /* Detector against plastic timing spectrum */
   struct mca mca_tdetdet;    /* Detector against detector timing spectrum */
   struct mca mca_pmttran;    /* PMT transit time spectrum */
   struct mca mca_pmtser;     /* PMT single-electron gain spectrum */
   struct mca mca_edet;       /* Detector energy spectrum */
   struct mca mca_vnegpk;     /* Underdrive-voltage spectrum */
   struct mca mca_kzero;      /* Zero-crossing-slope spectrum */


   /* ******** Function declarations ********************************** */

   double gauss();            /* function to return element from
                                 gaussian dist. */
   int gpritr();              /* function to load impulse response array from
                                 SPICE .PRINT listing of impulse response */
   int gpoisson_times();      /* function to get poisson time points */
   double baseEnergy();       /* function to return scatter and photofraction
                                 between 0.0 and 1.0 with photopeak at 1.0 */

   /* void clear_mca();          function to clear mca */
   /* void load_mca();           function to load mca */
```

```
/* void filter_mca();         function to filter mca and analyze FWHM etc.*/
/* void print_spectrum();     function to print spectrum to report file */


/* ************* program variables ********************************** */

int n;                      /* index for events - starts at 1 */
int i;                      /* index for time step for each event -
                               starts at 0 */
int k;                      /* index for Poisson points for each event -
                               starts at 0 */
int k_total;                /* total number of Poisson points used */
int k_thld;                 /* total number of Poisson points up to
                               threshold crossing */

float tpoisson[KLIMIT];     /* array of Poisson time points */
float tpmtdelay[KLIMIT];    /* array of PMT Transit-time points */
float tpmt[KLIMIT];         /* array of PMT impulse-time points */
int   tpmt_i[KLIMIT];       /* array of PMT impulse-time points in TSTEP */
float gpmt[KLIMIT];         /* array of PMT SER gain points */
float event_energy;         /* event energy normalized to 1.0 (511 keV) */
int t_i;                    /* time value used (in TSTEP units) to find
                               timing waveform */
float v, vprev;             /* present and prev. voltage value in waveform */
float vnegpk;               /* peak negative (underdrive) voltage in wform */
float kzero;                /* zero-crossing slope (V/ns) in waveform */

float t_thld_crossing;      /* time of threshold crossing for event */
float t_thld_crossing_prev; /* time of threshold crossing for previous
                               event */
float t_plastic;            /* time of plastic detector for event */

int flag_eps_crossed;       /* flag to mark crossing of epsilon for event */
int flag_thld_crossed;      /* flag to mark crossing of threshold for event*/

float h[ILIMIT];            /* impulse response lookup table */
int i_total;                /* total numer of points read from SPICE impulse
                               response lookup table */

float base_energy;          /* normalized scatter, photopeak energy before
                               Gaussian blurring */

FILE *fptr;                 /* file pointer for MCA output file */


/* ******** Initialization of MCA Structures ************************** */

     /* Detector (single) timing spectrum */

mca_tdet.begin       = 5e-9;       /* beginning mca channel (sec) */
mca_tdet.end         = 30e-9;      /* ending mca channel (sec) */
mca_tdet.ch_wid      = 50e-12;     /* channel width (sec) */
mca_tdet.ch_units    = 1e-9;       /* channel units (sec) */
mca_tdet.fil_nos     = 4;          /* number of sym. filter channels */
mca_tdet.fil_sig     = 2.0;        /* sigma (channels) for filtering */
strcpy (mca_tdet.title,"Detector (Single) Timing Spectrum");
strcpy (mca_tdet.label,"ns\tcounts\tfcounts");
```

```
     /* Plastic detector against detector timing spectrum */

mca_tplasdet.begin   = 5e-9;       /* beginning mca channel (sec) */
mca_tplasdet.end     = 30e-9;      /* ending mca channel (sec) */
mca_tplasdet.ch_wid  = 50e-12;     /* channel width (sec) */
mca_tplasdet.ch_units= 1e-9;       /* channel units (sec) */
mca_tplasdet.fil_nos = 4;          /* number of sym. filter channels */
mca_tplasdet.fil_sig = 2.0;        /* sigma (channels) for filtering */
strcpy (mca_tplasdet.title,
         "Plastic Detector Against Detector Timing Spectrum");
strcpy (mca_tplasdet.label,"ns\tcounts\tfcounts");

     /* Detector against detector timing spectrum */

mca_tdetdet.begin    = -15e-9;     /* beginning mca channel (sec) */
mca_tdetdet.end      = 15e-9;      /* ending mca channel (sec) */
mca_tdetdet.ch_wid   = 100e-12;    /* channel width (sec) */
mca_tdetdet.ch_units = 1e-9;       /* channel units (sec) */
mca_tdetdet.fil_nos  = 4;          /* number of sym. filter channels */
mca_tdetdet.fil_sig  = 2.0;        /* sigma (channels) for filtering */
strcpy (mca_tdetdet.title,"Detector Against Detector Timing Spectrum");
strcpy (mca_tdetdet.label,"ns\tcounts\tfcounts");

     /* Plastic detector (single) timing spectrum */

mca_tplas.begin      = -0.5e-9;    /* beginning mca channel (sec) */
mca_tplas.end        = 0.5e-9;     /* ending mca channel (sec) */
mca_tplas.ch_wid     = 5e-12;      /* channel width (sec) */
mca_tplas.ch_units   = 1e-9;       /* channel units (sec) */
mca_tplas.fil_nos    = 6;          /* number of sym. filter channels */
mca_tplas.fil_sig    = 3.0;        /* sigma (channels) filtering */
strcpy (mca_tplas.title,"Plastic Detector (Single) Timing Spectrum");
strcpy (mca_tplas.label,"ns\tcounts\tfcounts");

     /* Detector energy spectrum */

mca_edet.begin       = 0.0;        /* beginning mca channel(norm. energy)*/
mca_edet.end         = 2.5;        /* ending mca channel (norm. energy) */
mca_edet.ch_wid      = 10e-3;      /* channel width (norm. energy) */
mca_edet.ch_units    = 1.0;        /* channel units (norm. energy) */
mca_edet.fil_nos     = 4;          /* number of sym. filter channels */
mca_edet.fil_sig     = 1.0;        /* sigma (channels) for filtering */
strcpy (mca_edet.title,"Detector Energy Spectrum");
strcpy (mca_edet.label,"enorm\tcounts\tfcounts");

     /* PMT single-electron spectrum */

mca_pmtser.begin     = 0.0;        /* beginning mca channel (norm. gain) */
mca_pmtser.end       = 2.5;        /* ending mca channel (norm. gain) */
mca_pmtser.ch_wid    = 50e-3;      /* channel width (norm. gain) */
mca_pmtser.ch_units  = 1.0;        /* channel units (norm. gain) */
mca_pmtser.fil_nos   = 4;          /* number of sym. filter channels */
mca_pmtser.fil_sig   = 2.0;        /* sigma (channels) for filtering */
strcpy (mca_pmtser.title,"PMT Single-Electron Gain Spectrum");
strcpy (mca_pmtser.label,"gnorm\tcounts\tfcounts");
```

```
      /* PMT transit-time spectrum */

   mca_pmttran.begin    = 2.5e-9;      /* beginning mca channel (sec) */
   mca_pmttran.end      = 7.5e-9;      /* ending mca channel (sec) */
   mca_pmttran.ch_wid   = 25e-12;      /* channel width (sec) */
   mca_pmttran.ch_units = 1e-9;        /* channel units (sec) */
   mca_pmttran.fil_nos  = 4;           /* number of sym. filter channels */
   mca_pmttran.fil_sig  = 2.0;         /* sigma (channels) for filtering */
   strcpy (mca_pmttran.title,"PMT Transit-Time Spectrum");
   strcpy (mca_pmttran.label,"ns\tcounts\tfcounts");

      /* Underdrive voltage spectrum (voltage treated positively) */

   mca_vnegpk.begin     = 0.0;         /* beginning mca channel (V) */
   mca_vnegpk.end       = 0.2;         /* ending mca channel (V) */
   mca_vnegpk.ch_wid    = 1.0e-3;      /* channel width (V) */
   mca_vnegpk.ch_units  = 1.0;         /* channel units (V) */
   mca_vnegpk.fil_nos   = 4;           /* number of sym. filter channels */
   mca_vnegpk.fil_sig   = 2.0;         /* sigma (channels) for filtering */
   strcpy (mca_vnegpk.title,"Underdrive-voltage Spectrum");
   strcpy (mca_vnegpk.label,"V\tcounts\tfcounts");

      /* Zero-crossing slope spectrum (slope units V/ns) */

   mca_kzero.begin      = 0.0;         /* beginning mca channel (V/ns) */
   mca_kzero.end        = 0.1;         /* ending mca channel (V/ns) */
   mca_kzero.ch_wid     = 1.0e-3;      /* channel width (V/ns) */
   mca_kzero.ch_units   = 1.0;         /* channel units (V/ns) */
   mca_kzero.fil_nos    = 4;           /* number of sym. filter channels */
   mca_kzero.fil_sig    = 2.0;         /* sigma (channels) for filtering */
   strcpy (mca_kzero.title,"Zero-crossing Slope Spectrum");
   strcpy (mca_kzero.label,"V/ns\tcounts\tfcounts");




   /* *********** clear the MCAs ************************************** */

   clear_mca (&mca_tdet);
   clear_mca (&mca_tplas);
   clear_mca (&mca_tplasdet);
   clear_mca (&mca_tdetdet);
   clear_mca (&mca_edet);
   clear_mca (&mca_pmttran);
   clear_mca (&mca_pmtser);
   clear_mca (&mca_vnegpk);
   clear_mca (&mca_kzero);


   /* *** read the impulse response lookup table from SPICE output file * */

   if (gpritr (SPICE_IMPULSE_RESPONSE_PRINT_FILE,h,&i_total))
     {
       printf ("Error Reading SPICE lookup table.  Program terminated.\n");
       exit (1);
     }
   if (i_total != ILIMIT)
     printf (
"WARNING - Impulse response lookup table length not equal to ILIMIT.\n");
```

```
   printf ("Impulse Response Lookup Table Read from SPICE .out File.\n");
   printf ("Starting Event Generation and Histogramming.\n\n");



   /* Special Impulse Response Lookup Table for 1st Photoelectron timing */
   /*   *** Comment Out for regular timing analysis ****                 */

/*
   h[0] = 0.0;
   h[1] = 1.0;
   h[2] = 0.0;
   h[3] = 0.0;
   h[4] = 0.0;
   h[5] = 0.0;

   for (i=6; i<ILIMIT; ++i)
     h[i] = 0.0;
*/

   /*  **** End of Special Impulse Response ****                          */



   /* ********** Main Loop for Events ********************************** */

   for (n=1; n<=NEVENTS; ++n)
     {

       /* get event energy (mean is 1.0 (511 keV));
            continue getting if energy is below selected threshold */


       if (!FLAG_COMPTON_SCATTER) /* Compton scatter not selected */
        {
          do
           {
             event_energy = SIGMA_ENERGY*gauss() + MEAN_ENERGY;
           }
          while (event_energy < (ENERGY_THLD_KEV/PHOTOPEAK_KEV) );
        }

       else                        /* Compton scatter selected */
        {
          do
           {
             base_energy = baseEnergy(); /* base_energy ranges from 0.0 to
                                            1.0 with scatter below 1.0 and
                                            photopeak at 1.0 */
             event_energy = base_energy
                          +SIGMA_ENERGY*sqrt(base_energy)*gauss();
           }
          while (event_energy < (ENERGY_THLD_KEV/PHOTOPEAK_KEV) );
        }
```

```
/* get poisson time points */

k_total = gpoisson_times (tpoisson,event_energy*PHE_YIELD_511KEV,
            TAU1,TAU1_YIELD,TAU2,TAU2_YIELD,TAURISE,TEND);


/* get pmt single-electron delays, pmt impulse times,
     and pmt single-electron gains */

for (k=0; k<k_total; ++k)
  {
    tpmtdelay[k] = SIGMA_PMTDELAY*gauss() + MEAN_PMTDELAY;
    tpmt[k] = tpoisson[k] + tpmtdelay[k];
    tpmt_i[k] = (int)(tpmt[k]/TSTEP +0.5);
    while ( (gpmt[k] = SIGMA_PMTSER*gauss() + MEAN_PMTSER) < 0.0 )
      ;                  /* get another point if point negative */
  }


/* **** find voltage waveform and threshold crossing for event ** */

flag_eps_crossed = FALSE;
flag_thld_crossed = FALSE;

vnegpk = 0.0;
kzero = 0.0;

for (i=0; i<ILIMIT; ++i)  /* loop for each time point in waveform */
  {
    v = 0.0;

    for (k=0; k<k_total; ++k)     /* loop for poisson points */
      {
        t_i = i - tpmt_i[k];      /* t_i is in units of TSTEP */
        if (t_i < 0)
          ;
        else
          v = v +gpmt[k]*h[t_i];
      }

    if (flag_eps_crossed)         /* can occur on 2nd or higher pass */
      {
        if (v>VTHRESHOLD)
          {
            flag_thld_crossed = TRUE;
            t_thld_crossing = (float)i*TSTEP
                              -TSTEP*(v-VTHRESHOLD)/(v-vprev);
            kzero = ((v -vprev)/TSTEP)*1e-9; /* V/ns units */
            break;
          }
      }

    else
      {
        if ((VTHRESHOLD -v) > EPSILON)
          flag_eps_crossed = TRUE;
      }

    if (v < vnegpk) /* find vnegpk */
      vnegpk = v;
```

```
            vprev = v;

          } /* Continue looking for threshold crossing */


        /* *** Threshold Crossing Determined for Event ***************** */

        /* Threshold Crossing Did NOT Occur - Do NOT Load MCAs */


        if (!flag_thld_crossed) /* MCA will reject event */
          {
            printf ("Threshold Crossing Not Found for Event %d of %d.\n",
                        n,NEVENTS);
          }


        /* *** Threshold Crossing Did Occur - Load MCAs *************** */

        else
          {

        /* Find k_thld (number of Poisson points up to threshold crossing) */

#if 0  /* Not used at first Poisson point loaded in PMT spectra */

           for (k=0; k<k_total; ++k)
              {
                if (tpmt[k] > t_thld_crossing)
                  break;
              }
            k_thld = k;
#endif


        /* Load Detector Energy Spectrum MCA */

        load_mca (&mca_edet,event_energy);


        /* Load Detector Timing Spectrum MCA */

        load_mca (&mca_tdet,t_thld_crossing);


        /* Load Plastic Detector Timing Spectrum MCA */

        t_plastic = SIGMA_PLAST*gauss() +MEAN_PLAST;
        load_mca (&mca_tplas,t_plastic);


        /* Load Detector Against Plastic Timing Spectrum MCA */

        load_mca (&mca_tplasdet,t_thld_crossing -t_plastic);


        /* Load Detector Against Detector Timing Spectrum MCA */
```

```
      if (n > 1) /* Do not load MCA on first event as previous one reqd. */
        load_mca (&mca_tdetdet,t_thld_crossing -t_thld_crossing_prev);


      /* Load PMT single-electron gain and transit-time spectra MCA */

      k_thld = 1;     /* only the first detector impulse is loaded */
      for (k=0; k<k_thld; ++k)
        {
          load_mca (&mca_pmttran,tpmtdelay[k]);
          load_mca (&mca_pmtser,gpmt[k]);
        }


      /* Load Underdrive-Voltage Spectrum MCA (make underdrive positive) */

      load_mca (&mca_vnegpk,-vnegpk);


      /* Load Zero-Crossing-Slope Spectrum MCA (units V/ns) */

      load_mca (&mca_kzero,kzero);


    }

      /* Print status of Event Histograms for Each 1000 events */

      if ( (n % 1000) == 0 )
        {
        printf ("Event %d of %d has been histogrammed.\n",n,NEVENTS);
        printf
("Energy: %d (in) %d (out)   Time (det-det): %d (in) %d (out)\n\n",
          mca_edet.nos_in,mca_edet.nos_out,
          mca_tdetdet.nos_in,mca_tdetdet.nos_out);
        }


      t_thld_crossing_prev = t_thld_crossing;  /* store value for previous
                                                  crossing */

    } /* ***************** Go get next event ************************** */




  /* ************** Load File with MCA Spectra Data ****************** */

  /* Compute all filtered MCA values and analyze each spectrum */

  filter_mca (&mca_tdet);
  filter_mca (&mca_tplas);
  filter_mca (&mca_tplasdet);
  filter_mca (&mca_tdetdet);
  filter_mca (&mca_edet);
  filter_mca (&mca_pmttran);
  filter_mca (&mca_pmtser);
  filter_mca (&mca_vnegpk);
  filter_mca (&mca_kzero);
```

```
   /* Open Report File */

   if ( (fptr = fopen (REPORT_FILE_FOR_SPECTRA, "w")) == NULL )
     {
       printf ("Report File Cannot Be Opened.  Program Terminated.\n");
       exit (1);
     }
   printf ("Report File Opened.\n");

   /* Label General Information on Report File */

   fprintf(fptr,"Monte Carlo Spectra Results from cfdmont.c\r\n\r\n");

   fprintf(fptr,
"N0 (511keV) = %f;tau1 (ns) = %f @%f;tau2 (ns) = %f @%f;taurise (ns) =
%f\r\n",
     PHE_YIELD_511KEV,TAU1*1e9,TAU1_YIELD,TAU2*1e9,TAU2_YIELD,
     TAURISE*1e9);

   fprintf(fptr,"Detector Energy (norm. to 511keV):Mean = %f;FWHM =%f;\r\n",
     MEAN_ENERGY,2.35*SIGMA_ENERGY);
   if (!FLAG_COMPTON_SCATTER)
     fprintf(fptr,"Compton Scatter Not Selected.\r\n");
   else
     fprintf(fptr,"Compton Scatter Selected.\r\n");
   fprintf(fptr,"Energy Threshold = %f (keV);\r\n", ENERGY_THLD_KEV);
   fprintf(fptr,"Scat. Fract. = %f; Scat. Knee = %f; Photofract. = %f;\r\n",
     SCATTERFRACTION, SCATTERKNEE, PHOTOFRACTION);
   fprintf(fptr,"PMT Transit Time: Mean = %f (ns); FWHM = %f (ns);\r\n",
     MEAN_PMTDELAY*1e9,2.35*SIGMA_PMTDELAY*1e9);
   fprintf(fptr,"PMT SER Gain (Norm): Mean = %f; FWHM = %f;\r\n",
     MEAN_PMTSER,2.35*SIGMA_PMTSER);
   fprintf(fptr,"Plastic Detector Timing:Mean = %f (ns);FWHM = %f (ns);\r\n",
     MEAN_PLAST*1e9,2.35*SIGMA_PLAST*1e9);
   fprintf(fptr,"TSTEP = %f (ns); TEND = %f (ns);\r\n",1e9*TSTEP,1e9*TEND);


   printf ("General Information in Report File Labelled.\n");


   print_spectrum (fptr,&mca_tdet);       /* Print detector timing spectrum */
   print_spectrum (fptr,&mca_tdetdet);    /* Print det-det timing spectrum */
   print_spectrum (fptr,&mca_tplasdet);   /* Print plastic-det timing spect */
   print_spectrum (fptr,&mca_tplas);      /* Print plastic timing spectrum */
   print_spectrum (fptr,&mca_edet);       /* Print detector energy spectrum */
   print_spectrum (fptr,&mca_pmttran);    /* Print PMT transit-time spect */
   print_spectrum (fptr,&mca_pmtser);     /* Print PMT SER spectrum */
   print_spectrum (fptr,&mca_vnegpk);     /* Print Underdrive spectrum */
   print_spectrum (fptr,&mca_kzero);      /* Print Zero-crossing slope spect.
*/

   printf ("Report File Spectra Data Completed.\n");
```

```
    if ( fclose (fptr) != NULL )
      {
        printf ("Report File Cannot Be Closed.  Program Terminated.\n");
        exit (1);
      }
    printf ("Report File Closed.\n");


    /* List Summary for Single-Detector Timing Spectrum */

    printf ("\n");
    printf ("Summary of Single-Detector Timing Spectrum (units = %e).\n",
      mca_tdet.ch_units);
    printf ("Centroid = %f, filtered centroid counts = %f.\n",
      mca_tdet.cent/mca_tdet.ch_units, mca_tdet.cent_cnts);
    printf ("1/2 chs: low = %f, high = %f, FWHM = %f.\n",
      mca_tdet.halfl/mca_tdet.ch_units,
      mca_tdet.halfh/mca_tdet.ch_units,
      mca_tdet.fwhm/mca_tdet.ch_units);
    printf ("1/10 chs: low = %f, high = %f, FWTM = %f.\n",
      mca_tdet.tenthl/mca_tdet.ch_units,
      mca_tdet.tenthh/mca_tdet.ch_units,
      mca_tdet.fwtm/mca_tdet.ch_units);
    printf ("\n");

    printf ("Monte Carlo Analysis Program Completed.\n");
    printf ("\n");
}



    /* Function to clear raw MCA data */

    clear_mca (m)

      struct mca *m;

        {
          int n;
          m->ch_nos = (int)((m->end -m->begin)/m->ch_wid +0.5) +1;
          for (n=0; n<m->ch_nos; ++n)
            m->raw[n] = 0;
          m->nos_in = 0;
          m->nos_out = 0;
        }



       /* Function to load raw MCA data */

    load_mca (m, value)

      struct mca *m;
      float value;

        {
          int mca_ch;
          mca_ch = (int)( (value -m->begin)/m->ch_wid +0.5 );
```

```
        if ( (mca_ch < 0)||(mca_ch > (m->ch_nos -1)) )
          {
            ++(m->nos_out);
          }
        else
          {
            ++(m->nos_in);
            ++(m->raw[mca_ch]);
          }
      }



   /* Function to compute filtered MCA and analyze spectrum */
   /* Function is called AFTER raw MCA has been fully loaded */

#define MAX_NOS_COEF   100    /* maximum number of total filter coeficients */

   filter_mca (m)

    struct mca *m;       /* m is mca structure */

       {
         int n;            /* variable for indexing mca values */
         int n_cent;       /* mca index for centroid channel */
         int ktotal;       /* total number of filter points */
         int k;            /* variable for indexing filter points */
         int flag_halfl;   /* flag for lower half channel found */
         int flag_halfh;   /* flag for higher half channel found */
         int flag_tenthl; /* flag for lower tenth channel found */
         int flag_tenthh; /* flag for higher tenth channel found */
         float coef[MAX_NOS_COEF];
                           /* the filter coefs are symmetrical and sum to 1.0*/
         float sum;        /* sum of filter coefs; used for normalization */
         float half_cent_cnts;    /* one-half of centroid counts */
         float tenth_cent_cnts;   /* one-tenth of centroid counts */

   /* Build filter coeficient array */

         ktotal = (m->fil_nos)*2 +1;
         sum = 0.0;
         for (k=0; k<ktotal; ++k)
           {
             coef[k] = exp( -(float)(k -(m->fil_nos))*(float)(k -(m-fil_nos))/
                         (2.0*(m->fil_sig)*(m->fil_sig))  );
             sum = coef[k] + sum;
           }
         for (k=0; k<ktotal; ++k)
           coef[k] = coef[k]/sum;

   /* Compute filtered mca array */

         for (n=0; n<m->ch_nos; ++n)  /* loop through all MCA channels */
           {
             /* bottom and top fil_nos channels are not filtered */
```

```
        if ( (n < m->fil_nos)||(n > (m->ch_nos -m->fil_nos -1)) )
          {
            m->fil[n] =(float)(m->raw[n]);
          }

        else      /* all other channels are filtered */
          {
            m->fil[n] = 0.0;
            for (k=0; k<ktotal; ++k)  /* loop for all filter points */
               m->fil[n] = m->fil[n]
                           +coef[k]*(float)(m->raw[n +k -m->fil_nos]);
          }
      }


/* Analyze filtered mca spectrum */

    /* set half/tenth points and fwhm/fwtm to -ch_wid as an error
         condition if half and tenth points are not found */

        m->halfl  = -m->ch_wid;
        m->halfh  = -m->ch_wid;
        m->tenthl = -m->ch_wid;
        m->tenthh = -m->ch_wid;
        m->fwhm   = -m->ch_wid;
        m->fwtm   = -m->ch_wid;

    /* find centroid (peak) value */

    n_cent = 0;
    m->cent_cnts = 0.0;
    for (n=0; n<m->ch_nos; ++n)
      {
        if (m->fil[n] > m->cent_cnts)
          {
            m->cent_cnts = m->fil[n];
            n_cent = n;
          }
      }
    m->cent = (float)n_cent*m->ch_wid +m->begin;


    /* find channel 1/2, 1/10 counts */

    half_cent_cnts  = 0.5*m->cent_cnts;
    tenth_cent_cnts = 0.1*m->cent_cnts;

    /* find lower 1/2, 1/10 point channels */

    flag_halfl = FALSE;
    flag_tenthl = FALSE;

    for (n=n_cent -1; n>= 0; --n)  /* start at one point down from
                                        centroid and go down */
      {
        if ( !flag_halfl && (m->fil[n] < half_cent_cnts) )
          {
            flag_halfl = TRUE;
```

```
            m->halfl = (float)n*m->ch_wid +m->begin
                       + m->ch_wid*(half_cent_cnts - m->fil[n])/
                         (m->fil[n+1] -m->fil[n]);
          }

        if ( !flag_tenthl && (m->fil[n] < tenth_cent_cnts) )
          {
            flag_tenthl = TRUE;
            m->tenthl = (float)n*m->ch_wid +m->begin
                       + m->ch_wid*(tenth_cent_cnts - m->fil[n])/
                         (m->fil[n+1] -m->fil[n]);
          }
      }
        /* lower 1/2, 1/10 ch not found if centroid at bottom ch */


    /* find upper 1/2, 1/10 point channels */

    flag_halfh = FALSE;
    flag_tenthh = FALSE;

    for (n=n_cent +1; n<m->ch_nos; ++n)  /* start at one ch up from
                                            centroid and go up */
      {
        if ( !flag_halfh && (m->fil[n] < half_cent_cnts) )
          {
            flag_halfh = TRUE;
            m->halfh = (float)n*m->ch_wid +m->begin
                       - m->ch_wid*(half_cent_cnts - m->fil[n])/
                         (m->fil[n-1] -m->fil[n]);
          }

        if ( !flag_tenthh && (m->fil[n] < tenth_cent_cnts) )
          {
            flag_tenthh = TRUE;
            m->tenthh = (float)n*m->ch_wid +m->begin
                       - m->ch_wid*(tenth_cent_cnts - m->fil[n])/
                         (m->fil[n-1] -m->fil[n]);
          }
      }
         /* upper half, tenth points not found if centroid last ch */


    /* compute fwhm, fwtm if both high and low points found */

    if (flag_halfl && flag_halfh)
      m->fwhm = m->halfh -m->halfl;

    if (flag_tenthl && flag_tenthh)
      m->fwtm = m->tenthh -m->tenthl;

}
```

```
  /* Function to Print Each Spectrum in Report File */

  print_spectrum (fptr,m)
    FILE *fptr;
    struct mca *m;

  {
    int n; /* index for printing out spectrum values */

    /* Print title, number of events, and data label */

    fprintf (fptr,"\r\n\r\n\r\n\r\n\r\n"); /* put in blank lines to separate */
    fprintf (fptr,m->title); fprintf (fptr,"\r\n");
    fprintf (fptr,"Total Events = %d:  %d (in)  %d (out)\r\n",
      NEVENTS,m->nos_in,m->nos_out);
    fprintf (fptr,"Channel: nos = %d, width = %e\r\n",
      m->ch_nos,m->ch_wid);

    fprintf (fptr,"Nos of sym filter chs = %d,Filter sigma (chs) = %f\r\n",
      m->fil_nos,m->fil_sig);
    fprintf (fptr,"\r\n");

    fprintf (fptr,"Spectrum Analysis(units same as spectrum listing)\r\n");
    fprintf (fptr,"Centroid = %f, filtered centroid counts = %f\r\n",
      m->cent/m->ch_units, m->cent_cnts);
    fprintf (fptr,"1/2 chs: low = %f, high = %f, FWHM = %f\r\n",
      m->halfl/m->ch_units, m->halfh/m->ch_units, m->fwhm/m->ch_units);
    fprintf (fptr,"1/10 chs: low = %f, high = %f, FWTM = %f\r\n",
      m->tenthl/m->ch_units, m->tenthh/m->ch_units, m->fwtm/m->ch_units);
    fprintf (fptr,"\r\n");

    fprintf (fptr,m->label); fprintf (fptr,"\r\n");


          /* Print channel values, raw counts, filtered counts */

    for (n=0; n<m->ch_nos; ++n)
      fprintf(fptr,"%6.3f\t%6d\t%8.1f\r\n",
        ((float)(n)*(m->ch_wid) + m->begin)/(m->ch_units),
        m->raw[n],
        m->fil[n]);

  }



/* Function to get Poisson time points */

int gpoisson_times (tpoisson,n0,tau1,yield1,tau2,yield2,taurise,tend)

  float tpoisson[],       /* array of poisson time points (returned) */
        n0,               /* photoelectron yield */
        tau1,             /* primary scint. decay time constant */
        yield1,           /* yield (0.0 - 1.0) of primary decay */
        tau2,             /* secondary scint. decay time constant */
        yield2,           /* yield (0.0 - 1.0) of secondary decay */
        taurise,          /* scint. rise time time constant */
        tend;             /* ending time for finding points */
```

```
{
  double ran3();       /* function for returning random number */
  int k;               /* index for poisson time points */
  float t,             /* time of present poisson point */
        rate,          /* present rate of photoelectrons */
        x;             /* random number between 0.0 and 1.0 */

  k = 0;
  t = 0.0;



    /* rate is photoelectrons/sec; rate is increased slightly
         to consider loss during rise time */

    /* Poisson point rejected if ran3() > (1.0 -exp(-t/taurise)) to
         accomplish unbiased, random rejection of photoelectrons
         during rise time and generate rise time in Poisson
         spectrum */


  while ( (t<tend)&&(k<KLIMIT-1) ) /* max value of k is KLIMIT-1 */
    {

      do
        {
          while ( (x=ran3())<=0.0 ) /* do not accept value <= 0.0 */
            ;
          rate = (n0*tau1/(tau1-taurise))* (
                    (yield1/tau1)*exp(-t/tau1)
                   +(yield2/tau2)*exp(-t/tau2) ) ;

          t = t -(1.0/rate)*log(x); /* compute Poisson times */
        }
      while ( ran3() > (1.0-exp(-t/taurise)) ) ;

      tpoisson[k] = t;
      ++k;
    }

  return (k);        /* function returns number of poisson points */

}



/*   Function to return a value between 0.0 and 1.0 corresponding to scatter
       with an impulse photopeak at 1.0;  Original function written by
       Mike Casey, CTI PET Systems */

   double baseEnergy()
     {
       double x,a,b,c;
       double ran3();
       a = SCATTERFRACTION +SCATTERKNEE*(1.0-SCATTERFRACTION)*
             (1.0-PHOTOFRACTION);
       b = 1.0 -(1.0 -SCATTERFRACTION)*PHOTOFRACTION;
       x = ran3();
```

```
      if (x < a)
        x = x*SCATTERKNEE/a;
      else if (x < b)
        x = (x-a)*(1.0-SCATTERKNEE)/(b-a) +SCATTERKNEE;
      else
        x = 1.0;
      return (x);
    }



/* Function to return a zero mean, unity variance Gaussian Distribution.
     From Numerical Recipes in C. */

   double gauss()
   {
        static int i =0;
   static double v1,v2,r,fac,g1,g2;
        double ran3();
   if (i == 0)
                {
                r=1.0;
                while (r >= 1.0)
                        {
                        v1=2.0*ran3()-1.0;
                        v2=2.0*ran3()-1.0;
                        r=v1*v1+v2*v2;
                        }
                fac = sqrt( -2.0 * log (r)/r);
                g1 = v1*fac;
                g2 = v2*fac;
                i = 1;
                return(g1);
                }
        else
                {
                i = 0;
                return(g2);
                }
   }


#if 0   /* Original Random Number Generator Tried; Not Used Ultimately*/

/* Function to return a uniformly distributed random number between 0 and 1.
     Portable routine using one shuffled linear congruential generator
     modified from ran2() in Numerical Recipes in C.

*/

#define M 714025
#define IA 1366
#define IC 150889

double ran2()
   {
        static long seed = -12567;
        static long random_list[97],hold_it;
        static int initial_flag=0;
```

```
        int j;
    if( seed < 0 || initial_flag == 0) /* runs for first call only */
        {
        initial_flag=1;
        if(( seed = (IC-(seed)) % M) < 0)
            seed = -(seed);
        for (j=0; j < 97; j++)
            {
            seed = (IA*(seed)+IC) % M;
            random_list[j]=seed;
            }
        seed = (IA*(seed)+IC) % M;
        }
    j = (97 * (seed))/M;
    /* 0 <= j < 96 */
    hold_it = random_list[j];
    seed = (IA*(seed)+IC) % M;
    random_list[j]=(seed);
    return ((double) hold_it/M);
    }

#endif



/* Function to return a uniformly distributed random number between 0 and 1.
     Portable routine using subtractive technique modified from ran3() in
     Numerical Recipes in C.
*/


#define MBIG 1000000000
#define MSEED 161803398
#define MZ 0
#define FAC (1.0/MBIG)

float ran3()

{
    static int idum = -12567;    /* if negative, reseed */
    static int inext,inextp;
    static long ma[56];
    static int iff=0;
    long mj,mk;
    int i,ii,k;

    if (idum < 0 || iff == 0) {
        iff=1;
        mj=MSEED-(idum < 0 ? -idum : idum);
        mj %= MBIG;
        ma[55]=mj;
        mk=1;
```

```
        for (i=1;i<=54;i++) {
            ii=(21*i) % 55;
            ma[ii]=mk;
            mk=mj-mk;
            if (mk < MZ) mk += MBIG;
            mj=ma[ii];
        }
        for (k=1;k<=4;k++)
            for (i=1;i<=55;i++) {
                ma[i] -= ma[1+(i+30) % 55];
                if (ma[i] < MZ) ma[i] += MBIG;
            }
        inext=0;
        inextp=31;
        idum=1;
    }
    if (++inext == 56) inext=1;
    if (++inextp == 56) inextp=1;
    mj=ma[inext]-ma[inextp];
    if (mj < MZ) mj += MBIG;
    ma[inext]=mj;
    return mj*FAC;
}

#undef MBIG
#undef MSEED
#undef MZ
#undef FAC



/*
GET PRINT TRANSIENT FILE FUNCTION
by Dave Binkley and Steve Hudson
CTI PET Systems, Inc.
8-23-91

   This function will scan a PSpice PRINT transient file and extract a list of
voltages found within. This listing is stored in a floating-point array
called gpritr_array.


EXAMPLE: In the data file shown below, the column marked V(3) would be scanned
     and would produce the output shown.

INPUT FILE:
```

```
*** 08/22/91 11:32:00 ******** PSpice 4.05 (Jan 1991) ******** ID# 62683 ****

 CFD COMPARISON OF SHAPED WAVEFORMS, CFDCOMP.CIR


 ****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C


*******************************************************************************
```

```
  TIME            V(3)

   0.0000000E+00   0.0000000E+00
   1.0000000E-02  -6.6360076E-06
   2.0000000E-02  -4.6051674E-05
   3.0000000E-02  -1.2385810E-04
   4.0000000E-02  -2.3905132E-04
   5.0000000E-02  -3.9046015E-04
```

```
OUTPUT FILE:
```

```
   0.0000000E+00   0.0000000E+00
   1.0000000E-02  -6.6360076E-06
   2.0000000E-02  -4.6051674E-05
   3.0000000E-02  -1.2385810E-04
   4.0000000E-02  -2.3905132E-04
   5.0000000E-02  -3.9046015E-04
```

```
*/


int gpritr(filein,gpritr_array,numdata)

#define MAXNAME 16       /* maximum filename length */
#define MAXDATA 1500     /* maximum number of data elements */

char filein[MAXNAME];          /* input filename */
float gpritr_array[MAXDATA];   /* data array */
int *numdata;                  /* number of elements in array */

{
#define MAXBUFFER 150       /* maximum character length for buffer */

FILE *fpin;                 /* pointer for input file */
char *compare;              /* comparison string to indicate data header */
char buffer[MAXBUFFER];     /* string buffer */
char *result;               /* result of comparison; dummy character */
double num,dumnum;          /* data number; dummy number */
int x,y;                    /* counters */

   if ( (fpin = fopen(filein,"r")) == NULL)   /* open input file */
     {
       printf ("SPICE Impulse Res. File Cannot Be Opened.  Prog. Term.\n");
       return (1);          /* return 1 as file not found */
     }
   compare = "TRANSIENT ANALYSIS";      /* set comparison string */
   fgets(buffer, MAXBUFFER, fpin);
   result = NULL;

   /* loop to search for header string */
   while ((result  = strstr(buffer,compare)) == NULL)
   {
      if (fgets(buffer, MAXBUFFER, fpin) == NULL)  /* check for EOF */
      {
                printf("******* ERROR - data not found *******\n");
```

```
                fclose (fpin);  /* close input file */
                return (2);     /* return 2 as data not found */
        }
    }

    x = 0;
    y = 0;

    /* loop to read data elements */
    while (fgets(buffer, MAXBUFFER, fpin) != NULL)
    {
        x = (sscanf(buffer,"%lg%lg",&dumnum,&num));
        if (x == 2)
            gpritr_array[y++] = num;
    }

    fclose(fpin);       /* close input file */
    *numdata = y;       /* set number of elements in array */
         return (0);        /* return with no errors */
}
```

VITA

David Martin Binkley was born in Knoxville, Tennessee on July 19, 1955. He graduated from Bearden High School and then attended the University of Tennessee in Knoxville, receiving the Bachelor of Science Degree in Electrical Engineering in 1978. In 1988, Mr. Binkley was married to the former Jacqueline Lee Wimsatt of Brandon Florida.

After graduating with the Bachelor of Science degree, Mr. Binkley was employed at Technology for Energy Corporation in Knoxville where he designed electronic instrumentation for nuclear power plants, including radiation-hardened preamplifiers. In 1984, while employed at Technology for Energy Corporation, Mr. Binkley received a Master of Science Degree in Electrical Engineering from the University of Tennessee. His master's thesis is entitled "A Low-Noise 45-75 MHz Phase-Locked Loop Frequency Synthesizer for a High-Performance Communications Receiver."

In 1985, Mr. Binkley joined the research and development staff of Computer Technology and Imaging (now CTI PET Systems, Inc.) where he is presently a senior scientist. At CTI PET Systems, Inc., he has designed front-end electronic circuitry for commercial positron emission tomograph (PET) medical imaging scanners, including subnanosecond time-to-digital converters. Mr. Binkley has also designed digital and microprocessor circuits, developed microprocessor firmware, and developed computer software for circuit optimization of monolithic CMOS circuits. Presently, he leads a small group developing custom, high-speed, analog, CMOS integrated circuits for PET front-end applications. While employed at CTI PET Systems, Inc., Mr. Binkley has been a candidate for the Ph.D. degree in electrical engineering from the University of Tennessee.

Mr. Binkley is the principal investigator for over one-half million dollars of Small Business Innovative Research grants. He has published papers in areas of radiation-hardened circuit design, nuclear timing circuitry, time-of-flight PET, and analog CMOS integrated-circuit design. Mr. Binkley presently has a patent pending for the non-delay-line constant-fraction discriminator circuits reported in this work.

Mr. Binkley is a member of the IEEE, Research!America (a national organization promoting medical research), Community Forum (a local organization of neighborhood groups), the Knoxville Musicians' Association, and is president of the West Forest Neighborhood Association. Mr. Binkley is a professional jazz pianist who performs regularly in the Knoxville area. His hobbies include jazz composition and arranging, amateur radio (call sign WB4TQM), photography, running, and participation in neighborhood organizations.