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Fault Diagnostic System for Cascaded H-bridge Multilevel Inverter Drives Based on Artificial Intelligent Approaches Incorporating a Reconfiguration Technique

Surin Khomfoi

To the Graduate Council:

I am submitting herewith a dissertation written by Surin Khomfoi entitled "Fault Diagnostic System for Cascaded H-bridge Multilevel Inverter Drives Based on Artificial Intelligent Approaches Incorporating a Reconfiguration Technique." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

Leon M. Tolbert, Major Professor

We have read this dissertation and recommend its acceptance:

Jack S. Lawler, J. Wesley Hines, Fangxing Li

Accepted for the Council:
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Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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FAULT DIAGNOSTIC SYSTEM FOR CASCADED H-BRIDGE MULTILEVEL INVERTER DRIVES BASED ON ARTIFICIAL INTELLIGENT APPROACHES INCORPORATING A RECONFIGURATION TECHNIQUE

A Dissertation
Presented for the
Doctor of Philosophy Degree
The University of Tennessee, Knoxville

Surin Khomfoi
May 2007

DEDICATION

This dissertation is dedicated to my parents

Mr. Somnuk Khomfoi

and

Mrs. Somran Khomfoi

Dad, I sense that you did not initially encourage me for doing this, but at the end of the day I recognize that you always cheer me up as you were in the side of a soccer field when I played for the team. Thanks for teaching me the values of faith and perseverance.

Mom, I wish you could see me receiving all of my degree (from B.Eng to Ph.D.). You are the one and only person I most want to take a photo with. Although you are not being here with me, I can feel your presence support to overcome any obstacles I have challenged. Deepest thank for encouraging me to be **Mr. Surin Khomfoi** on my way.

"Connecting the dots to the touchdown"

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ABSTRACT

A fault diagnostic and reconfiguration system in a multilevel inverter drive (MLID) using artificial intelligent based techniques is developed in this dissertation. Output phase voltages of a MLID can be used as valuable information to diagnose faults and their locations. It is difficult to diagnose a MLID system using a mathematical model because MLID systems consist of many switching devices and their system complexity has a nonlinear factor. Therefore, a neural network (NN) classification is applied to the fault diagnosis of a MLID system. Multilayer perceptron (MLP) networks are used to identify the type and location of occurring faults. The principal component analysis (PCA) is utilized in the feature extraction process to reduce the NN input size. A lower dimensional input space will also usually reduce the time necessary to train a NN, and the reduced noise may improve the mapping performance. The genetic algorithm is also applied to select the valuable principal components. The comparison among MLP neural network (NN), principal component neural network (PC-NN), and genetic algorithm based selective principal component neural network (PC-GA-NN) are performed.

Proposed neural networks are evaluated with simulation test set and experimental test set. The PC-NN has improved overall classification performance from NN by about 5% points, whereas PC-GA-NN has better overall classification performance from NN by about 7.5% points. Therefore, the application of a genetic algorithm

improves the classification from PC-NN by about 2.5% point. The overall classification performance of the proposed networks is more than 90%.

A reconfiguration technique is also developed. The effects of using the developed reconfiguration technique at high modulation index are addressed. The developed fault diagnostic system is validated with experimental results. The developed fault diagnostic system requires about 6 cycles at 60 Hz to clear an open circuit and about 9 cycles at 60 Hz to clear a short circuit fault. The experimental results show that the developed system performs satisfactorily to detect the fault type, fault location, and reconfiguration.

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1. INTRODUCTION

1.1 Background

In recent years, industry has begun to demand higher power ratings. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. An inverter drive in megawatt level is normally interfaced with a medium voltage network. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations, and also multilevel inverter drive (MLID) systems have become a solution for high power drive applications. Two topologies of multilevel inverters for electric drive application have been discussed in [1]. A cascade MLID is a general fit for large automotive all-electric drives because of the high VA rating possible and because it uses several dc voltage sources which would be available from batteries or fuel cells [1]. A multilevel inverter not only achieves high power ratings, but also enables the use of renewable energy sources such as photovoltaic, wind, and fuel cells that can be easily interfaced to a multilevel converter system for a high power application [1, 2].

The concept of multilevel converters has been introduced since 1975 [3]. Despite that plentiful multilevel converter topologies have been developed during the last two decades, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected.

The main disadvantage of multilevel inverters is that they use a high number of power semiconductors; for this reason, multilevel inverters may be considered less reliable. Also, multilevel inverter systems are utilized in high power applications; thereupon, the reliability of the power electronics equipment is very important. For example, industrial applications such as industrial manufacturing are dependent upon induction motors and their inverter systems for process control. Generally, the conventional protection systems are passive devices such as fuses, overload relays, and circuit breakers to protect the inverter systems and the induction motors. The protection devices will disconnect the power sources from the multilevel inverter system whenever a fault occurs, stopping the operated process. Downtime of manufacturing equipment can add up to be thousands or hundreds of thousands of dollars per hour; therefore, fault detection and diagnosis is vital to a company's bottom line.

Multilevel inverters provide more possibilities in the power circuit to operate under faulty conditions; however, faults should be detected as soon as possible after they occur, because if a motor drive runs continuously under abnormal conditions, the drive or motor may quickly fail. Thus, knowledge of fault behaviors, fault prediction, and fault diagnosis are necessary.

1.2 Multilevel inverter drives (MLIDs)

Power electronics technologies have provided an important improvement of electric vehicles; also, hybrid-electric vehicles that use large electric drives will require high power inverters (>50 kW). Therefore, multilevel inverters are suitable for this application because a multilevel inverter can possibly provide the high voltampere ratings. For a traction drive application, a cascaded H-bridge multilevel inverter can be applied to drive the traction motor from a group of batteries or fuel cells. In another way, if a generated ac voltage source is available such as from an alternator or generator, a back-to- back diode-clamped converter can convert this source to variable-frequency ac voltage source to drive the traction motor [1].

Most inverter drives employ conventional inverter drives (CID) consisting of six power switches with two-level sinusoidal pulse width modulation (SPWM). The disadvantage of conventional converters has degraded voltage and current waveform qualities. To improve the waveform quality, the switching frequency needs to be high; this causes higher switching losses. Moreover, harmonic voltages could cause additional loss in a

traction motor. The additional core losses in an induction motor due to harmonic voltage have been studied in [4-5]. Additionally, the dc utilization of a conventional inverter is quite low even with the advent of PWM techniques such as third harmonic injection and space vector PWM; the maximum of dc utilization is about 86%. The dc utilization is particularly important factor for traction drive application in order to achieve wide speed range operation.

Significantly, the use of CIDs might cause motor damage and failure because some CIDs have high-voltage change rates (*dv/dt*), which generate a common mode voltage across the motor windings. High-frequency switching can aggravate this problem because of the frequent times this common mode voltage is impressed upon the motor each interval. The major problems reported have been *motor bearing failure* and *motor insulation breakdown* because of dielectric stresses, circulating currents, voltage surge, and corona discharge [1, 6]. Moreover, CIDs with fast switching (1 μs) at high voltage level (600 V) of power semiconductors can produce broadband electromagnetic interference (EMI).

A multilevel inverter has several advantages over a conventional two-level inverter that uses high switching frequency pulse width modulation (PWM). The attractive features of a multilevel inverter can be briefly summarized as follows:

- *Staircase waveform quality*: Multilevel inverters not only can generate the output voltages with very low distortion, but also can reduce the *dv*/*dt* stresses; therefore electromagnetic compatibility (EMC) problems can be reduced;

- *Common-mode (CM) voltage*: Multilevel inverters produce smaller CM voltage; therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. Furthermore, CM voltage can be eliminated by using advanced modulation strategies such as that proposed in [7];
- *Input current*: Multilevel inverters can draw input current with low distortion;
- *Switching frequency*: Multilevel inverters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency.

Unfortunately, multilevel inverters do have some disadvantages. One particular disadvantage is the greater number of power semiconductor switches needed. Although lower voltage rated switches can be utilized in a multilevel inverter, each switch requires a related gate drive circuit. This may cause the overall system to be more expensive and complex.

Three different major multilevel converter structures have been reported in the literature: cascaded H-bridges converter with separate dc sources (SDCS), diode clamped (neutral-clamped), and flying capacitors (capacitor clamped). Two topologies of multilevel inverters for electric drive application have been discussed in [1]. First, the cascade MLID is a general fit for large automotive all-electric drives because of the high VA rating possible and because it uses several level dc voltage sources which would be available from batteries or fuel cells. Second, the back-to-back diode-clamped converter

is ideal where a source of ac voltage is available, such as in a hybrid electric vehicle. *The cascaded MLID is the focus of this dissertation*.

1.2.1 Cascaded H- bridge multilevel inverter drives

A single-phase structure of an *m*-level cascaded inverter is illustrated in Figure 1.1. Each separate dc source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, *0*, and $-V_{dc}$ by connecting the dc source to the ac output by different combinations of the four switches, S_1, S_2, S_3, and S_4. To obtain $+V_{dc}$, switches S_1 and S_4 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S_2 and S_3. By turning on S_1 and S_2 or S_3 and S_4, the output voltage is *0*. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels *m* in a cascade inverter is defined by $m = 2s+1$, where *s* is the number of separate dc sources.

Cascaded inverters have also been proposed for use as the main traction drive in electric vehicles, where several batteries or ultracapacitors are well suited to serve as SDCSs [1]. The cascaded inverter could also serve as a rectifier/charger for the batteries of an electric vehicle while the vehicle was connected to an ac supply as shown in Figure 1.2. Additionally, the cascade inverter can act as a rectifier in a vehicle that uses regenerative braking.

The main advantages and disadvantages of multilevel cascaded H-bridge converters are as follows [1].

Advantages:

- The number of possible output voltage levels is more than twice the number of dc sources ($m = 2s + 1$);
- The series of H-bridges makes for modularized layout and packaging. This will enable the manufacturing process to be done more quickly and cheaply.

Disadvantages:

- Separate dc sources are required for each of the H-bridges. This will limit its application to products that already have SDCSs readily available.

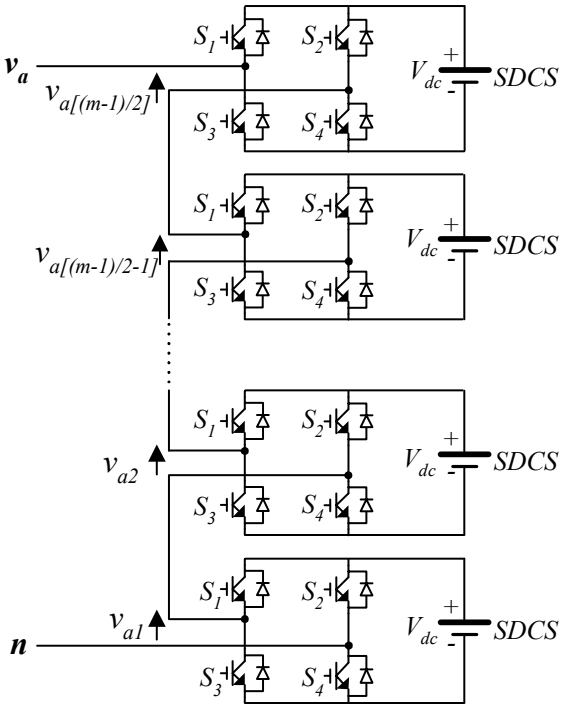


Figure 1.1. Single-phase structure of a multilevel cascaded H-bridges inverter.

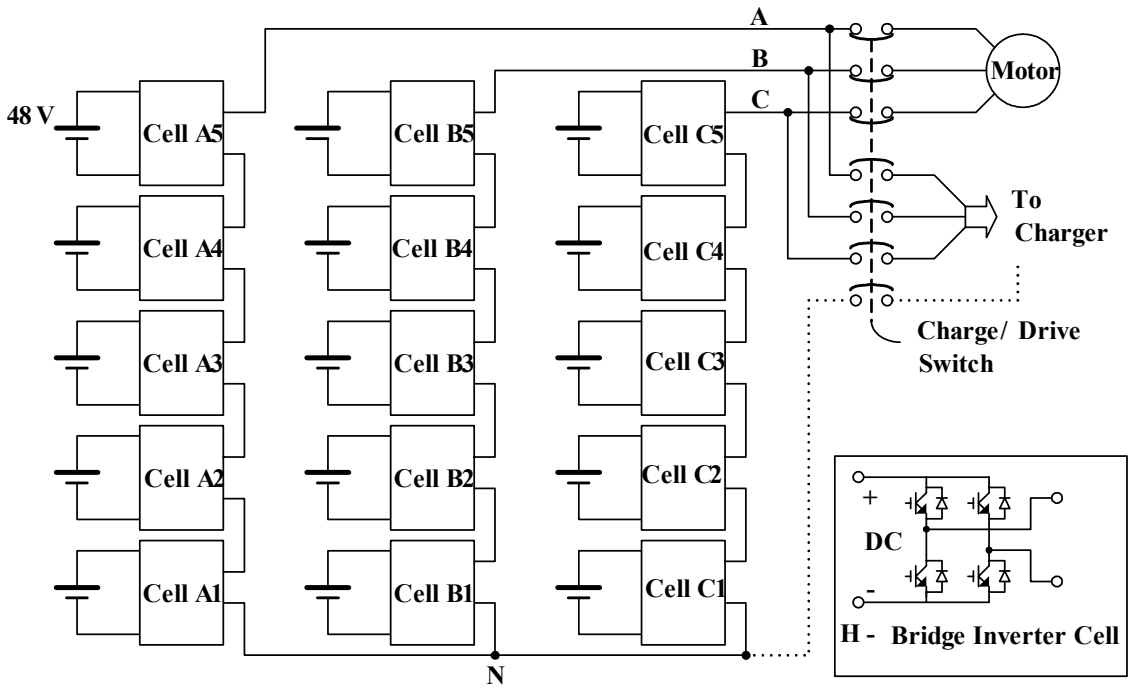


Figure 1.2. Three-phase wye-connection structure for electric vehicle motor drive and battery charging.

1.3 Faults and their consequences

Before continuing discussion in this research, it should be noted that the word *fault* is used to refer to a semiconductor power switch used in the MLID that fails to operate when provided gate drive signals and includes faults such as *short circuit or open circuit.* One particular effect on a faulty switch is unbalance output voltage of a MLID. In a balanced MLID system, the three line to neutral output voltages are equal in magnitude and are phase displaced from each other by 120 degree as illustrated in Figure 1.3[8-9].

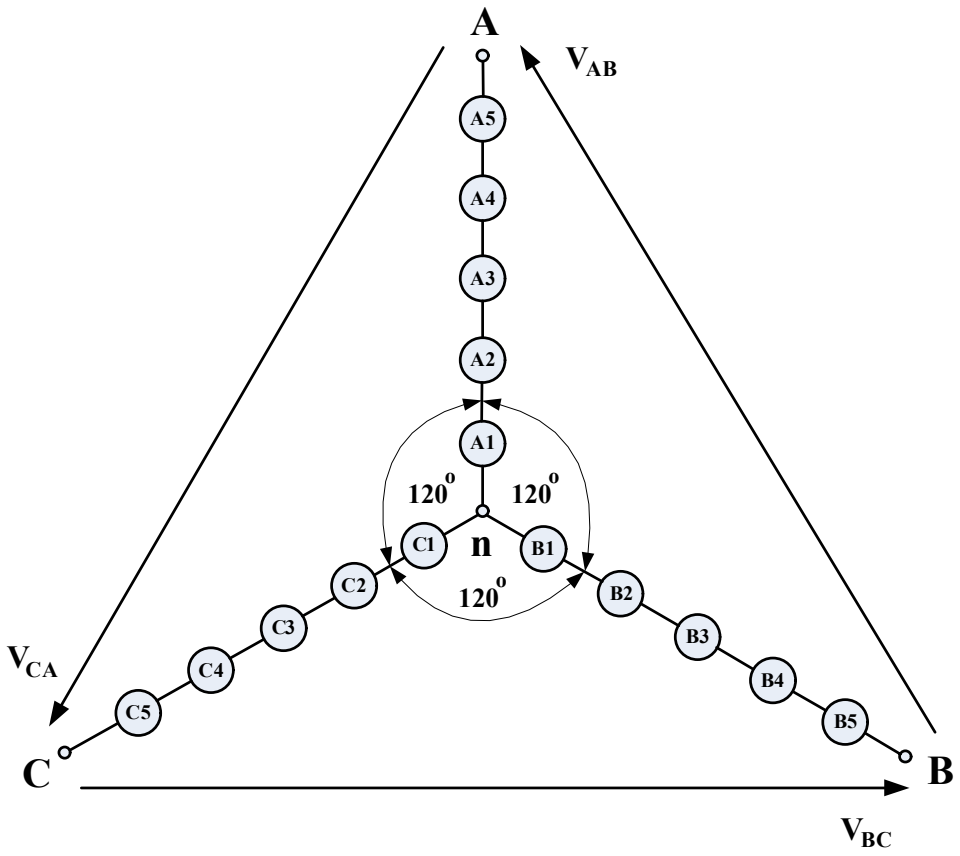


Figure 1.3. Balanced output voltage available for 5 cells per phase.

On the other hand, if a fault occurs at a semiconductor power switch in a cell, it will cause an unbalanced output voltage; for instance, the MLID system as shown in Figure 1.2 has fault (open or short circuit) on cell 5 at phase B, then the magnitude of line to neutral output voltages of phase B (V_{BN}) are not equal with other phases. This causes the line to line output voltages to also be unbalanced as shown in Figure 1.4 [9].

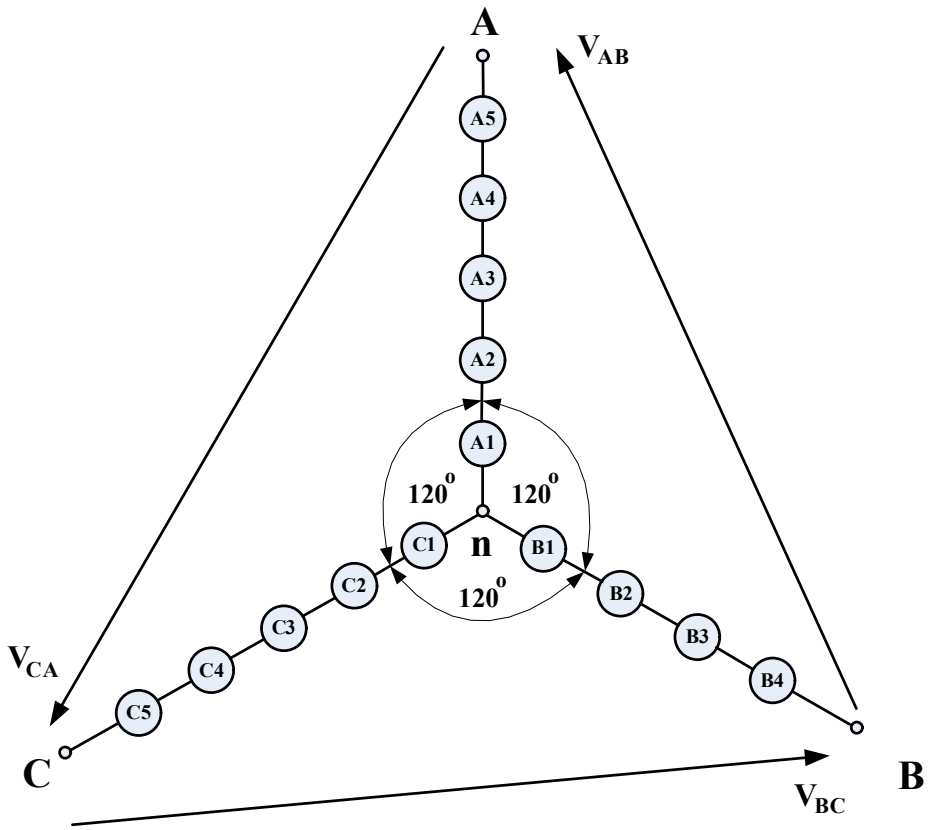


Figure 1.4. Unbalanced output voltage on VBC when a faulty cell occurs on phase B.

Voltage unbalance also has an impact on a conventional inverter drive system where the front end consists of three-phase rectifier systems. The triplen harmonic line currents which are uncharacteristic to these rectifier systems can exist in these situations leading to unexpected harmonic problems [8].

An excessive level of unbalanced output voltage can have serious impacts on mains connected to an induction motor. The level of an unbalanced current may have several

times the level of an unbalanced voltage. The unbalanced current in a line current can lead to disproportionate losses in the rotor and stator of the induction motor. Some induction motors are designed to tolerate a small level of unbalanced voltages and currents; however, they have to be derated if the unbalance is excessive. An induction motor that operates at its nameplate rated capacity without derating even though required load is not at rated capacity because of the unbalance voltages from a MLID will result in the useful lifetime of such an induction motor to be quite short. If the induction motor operates at full load all the time, the stator windings and the rotor may carry more current than that is permitted: this situation can lead to a reduction in induction motor efficiency and can reduce the insulation life caused by overheating. The average expected life of insulation halves for every 10^{o} C of temperature increase as reported in [8]. Moreover, an induction motor operating under unbalanced voltage condition will be noisy in its operation caused by torque and speed pulsation. Obviously, in such situations the effective torque and speed will be less then normal.

1.4 Reliability considerations of MLIDs

Since multilevel inverters contain several semiconductors connected in series to achieve medium voltage and high power demand, one might consider that multilevel inverters are less reliable. In contrast, multilevel cascaded H- bridge inverters using modular series-cells with separated dc sources as depicted in Figure 1.2 could improve reliability if the MLID has the ability to detect and bypass the faulty cell. If one of the power cells fails, it can be bypassed and operation can continue at reduced voltage capacity. The amount of

reduction in capacity that can be tolerated depends upon the application; however, in most cases a reduction in capacity is more preferable than a complete shutdown.

The reliability of a multilevel inverter having the bypass function in each cell has been described in [9]. The article explains how the bypass function improves the drive reliability. The major idea to improve reliability is to bypass the damaged cells by using a magnetic contactor. The proposed solution in [9, 11] protects the failure of all components in the faulty cells, rather than the damage to some power switches. The definition of reliability given by [10] is "*the probability of a device performing its purpose adequately for the period of time intended under the operating condition encountered"*. The word *adequately* permits some application at reduced capacity to be included in the probability calculations [9].

The engineering reliability analysis in a system is usually concerned with the reliability *R* and/or the probability of failure *P*. As a system is considered reliable unless it fails, the reliability and probability of failure sum to unity as explained in equation (1.1) [10].

$$\begin{aligned} R(t) + P(t) &= 1, \\ R(t) &= 1 - P(t), \\ P(t) &= 1 - R(t), \end{aligned} \tag{1.1}$$

where *P(t)* is probability of a system will fail by time *t* ,

R(t) is probability of a system will still be operational by time *t*. Therefore, (1.1) can be applied in MLID system reliability analysis. Suppose that the cascaded H-bridge MLID system as shown in Figure 1.2 contains *N* cells and can not tolerate any failures;

then, if the probability of a single cell will function properly during a time interval is *R*, so that the probability all *N* cells will function properly during the same time interval is R^N because the MLID system is considered as series system in this case. *P(t)* and *R(t)* can be defined as the point density functions; then, $P=\frac{d\,P(t)}{d(t)}$ and $R=\frac{d\,R(t)}{d(t)}$. Next, if the MLID has a cell which can tolerate failures, the MLID reliability will become $R^N + [N \times R^{(N-1)} \times (1- R)]$ instead of R^N. It is obvious that the MLID with a tolerated failure cell has a higher reliability than the one without tolerance for failures. A numerical reliability example of a MLID can be illustrated in Table 1.1. Assume that the MLID in Table 1.1 has a cell reliability *R* of 99% and it contains totally 15 cells. As can be seen, with one extra cell in each phase, the reliability of the MLID can increase from 86% to 99.0%; therefore, a fault diagnostic and fault reconfiguration (bypass) system can improve the reliability of the MLID system. In addition, for the case of *m* tolerated cells, the reliability function can be written as

$$R_m=\sum_{i=0}^{m}\left(\frac{N!}{(N-i)!\times i!}\times R^{(N-i)}\times(1-R)^i\right), \tag{1.2}$$

where m is number of tolerated cells,

N is number of cells in MLIDs,

R_m is total reliability of the system.

Table 1.1. Numerical example of 15 cells MLID with 99% reliability (R) in each power cell.

Number of tolerated cell faults	Reliability Function	Reliability (Percentage)
0	$R_0 = R^N$	86.006%
1	$R_1 = R_0 + [N \times R^{(N-1)} \times (1- R)]$	99.037%
2	$R_2 = R_1 + [(N \times (N-1) \times (R^{(N-2)}) \times (0.5 \times (1-R)^2)]$	99.958%
3	$R_3 = R_2 + [(N \times (N-1) \times (N-2) \times (R^{(N-3)}) \times (0.1667 \times (1-R)^3)]$	99.999%

1.5 AI applications in condition monitoring and diagnosis

The application of artificial intelligent (AI) in inverter drives is mostly based on speed or position controller applications. Fuzzy-logic (FL) and neuron network (NN) are mostly applied to such applications. Genetic algorithm is also applied on PI controller tuning and parameter estimation problems. The AI-based controllers could lead to improved performance, enhanced tuning and adaptive capabilities; however, there are additional possibilities in other aspects of AI-based applications in inverter drives or other power electronic areas.

It is possible that AI-based technique can be applied in condition monitoring and diagnosis. By using condition monitoring, vast savings may be made through improved maintenance procedures and policies. AI-based condition monitoring and diagnosis have several advantages; for instance, AI-based techniques do not require any mathematical models, therefore the engineering time and development time could be significantly reduced. AI-based techniques utilize the data sets of the system or expert knowledge. Moreover, the reliability of the system can also improve by using diagnosis; for example, in MLID applications, several types of signals such as voltage, current, noise, vibration, temperature, and flux signals which can convey valuable information for diagnosis on the electrical and mechanical state of a MLID system including motor, multilevel inverter and controller. The voltage and/or current signals could be used to diagnose a drift of power semiconductor switches in the multilevel inverter which contains numerous semiconductor switches.

AI-based fault diagnostic areas should include two different types of main tasks as follows:

- *Fault classification (detection)*: The purpose of this task is to detect any selected signals (electrical or mechanical) in the system. This could permit the system to be scheduled maintenance and might also prevent incipient system fault and would allow improving safety and reliability of the system;
- *Fault localization*: The purpose of this task is to identify the location of occurring faults. This specifies the cause of the detected abnormal behaviors.

AI-based techniques can be applied to both diagnostic tasks. Fault classification is a part of a protection paradigm and can also be considered as pattern recognition problems or non-linear problems [12]. Therefore, artificial neuron network (ANN) can be used to perform the fault classification. ANN techniques permit input/output mapping with a nonlinear relationship between nodes; also, ANN techniques provide the ability to recognize anomalous situations because of their intrinsic capacity to classify and generalize. Especially, the sensitivity and response time of the original procedure presented for the on-line analysis of fault set repetition enable on-line fault location techniques to be developed [13]. The normal and abnormal data or signals can be used to train the ANN, so that the ANN can have ability to classify the difference between normal and abnormal condition of the system.

1.6 Main contribution of the dissertation

The main contribution of this dissertation proposal is *to propose the fault diagnostic, fault detection, and fault reconfiguration paradigm for the cascaded H-Bridge multilevel inverter drive by applying artificial intelligent based techniques. In this dissertation, an attempt to diagnose the fault locations in a MLID from its output voltage waveforms is considered. MLID open circuit and short circuit faults at each switch are considered.* An example of a MLID open circuit fault at switch S_{A+} is represented in Figure 1.5. S_{A+} fault will cause unbalanced voltage and current output, while the induction motor is operating.

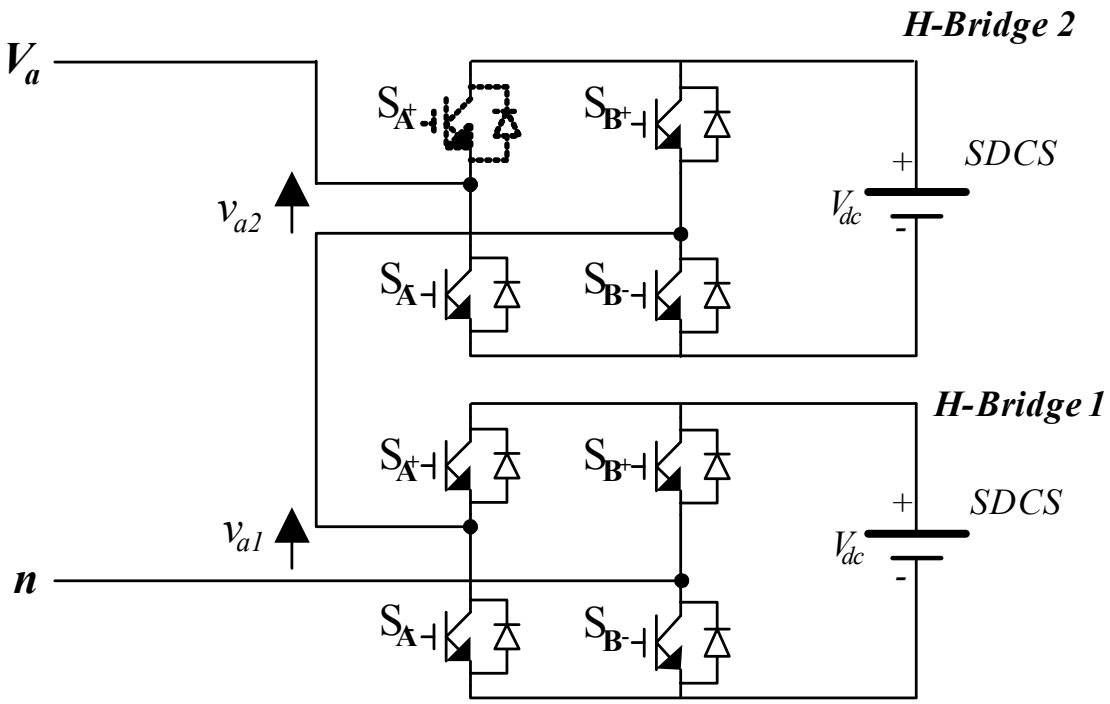


Figure 1.5. H-Bridge 2 Switch SA+ open circuit fault at second level of single-phase multilevel-inverter.

This unbalanced voltage and current may result in vital damage to the induction motor if the induction motor is run like this for a long time. The unbalanced condition from fault S_{A+} can be solved if the fault location is correctly identified. Switching patterns and the modulation index of other active switches in the MLID can be adjusted to maintain output voltage and current in a balanced condition. Therefore, the MLID can operate in a balanced condition at reduced power while the fault occurs until the operator knows and repairs the inactive switch.

All occurring fault features can be classified based on their effects of the output voltages; for that reason, one can use the output voltage signals as learning/training data to a neural network. A neural network has the ability to recognize anomalous situations because of their intrinsic capacity to classify and generalize. Genetic algorithm and principal component analysis can also be applied in feature extraction process in order to rate signals as an important feature. Thus, by applying the proposed AI-based techniques in a fault diagnostic system, a better understanding on fault behaviors, detections, and reconfigurations of a multilevel inverter drive system can be accomplished.

1.7 Organization of the dissertation

Chapter 2 provides a survey of previous works. Several approaches from previous research related in fault diagnosis, detection, and reconfiguration methods are investigated in this chapter. The proposed fault diagnostic and detection techniques for a multilevel inverter by using a neural network are described in chapter 3. Chapter 3 also provides the procedure of how to apply the AI techniques to fault diagnosis and detection. Reconfiguration techniques are introduced and examined in chapter 4. Chapter 5 illustrates the software and hardware implementation of an experiment test rig to validate the proposed fault diagnosis system. Finally, conclusions and recommendations for future work are discussed in chapter 6.

2. SURVEY OF PREVIOUS WORKS

2.1 Introduction

This chapter is intended as an overview of previous research in fault diagnosis, detection, and reconfiguration. The review particularly focuses on power electronic applications and drives. The organization of this chapter begins with a diagnostic system on conventional inverter drives (CID) because the knowledge of fault diagnosis in CIDs can be used to apply in other inverter drive topologies; therefore, several techniques of fault diagnosis and reconfiguration in CIDs are addressed. Subsequently, fault diagnostic and reconfiguration techniques for multilevel inverter drives are surveyed. Finally, promising technologies which are available in industry are also assessed.

2.2 A general protection used in a CID system

A conventional (voltage-fed) inverter drive has become one of the major applications in industry. Since a CID is used in various industrial applications, the reliability of the power electronic system of a CID is of paramount importance.

An example of an open loop volts/Hz speed control of a CID is shown in Figure 2.1; as can be seen, a CID usually consists of six diodes on the input side, dc link voltage, and six semiconductor power switches on the output side. Figure 2.1 shows that faults can occur in the motor, the rectifier, or the inverter. The conventional protection system used in a CID is mostly passive devices such as fuses, circuit breakers (CBs), and overload relays as illustrated in Figure 2.2. This protection system can protect against ground faults, dc link overvoltage and undervoltage, and inverter overcurrent. For instance, the input circuit breaker will trip for steady overcurrent to the inverter, and the input fuses will blow for short circuit fault of a diode in rectifier or a dc link capacitor. The inverter input fuse at dc link will protect the rectifier and filter capacitor from a shoot-through fault in the inverter. The metal oxide varistors at the input side will protect against overvoltage. The overtemperature of a motor will be protected by circuit breaker activated by thermal relay.

The protection system in Figure 2.2 is normally designed to shut down the inverter drive to protect the power circuit, overlooking the consequence of such accidental shut down. For instance, in the case of an inverter fault such as open or short circuit in a power switch, the fuse in dc link will blow when the current reaches to the safety limit, disconnecting the dc voltage supply. This may cause vitally consequent damages in the motor if the motor is running at base speed with rated load. Therefore, the passive protection system may not be adequate if the application of a CID needs a continuous operation or the motor is connected with a large load such as conveyer or hybrid/electric

vehicle. It would be better if one can isolate the fault and continue to operate the motor with a single phase mode with degraded motor performance.

The new generation of power semiconductor switches for a CID is mostly designed as modular package known as intelligent power module (IPM). An IPM usually combines a single phase or three phase rectifier and three phase inverter, gate drive circuit and protection circuit as one package as depicted in Figure 2.3. Generally, the protection system in Figure 2.2 is included in an IPM except an overload relay at the output side. An IPM provides a smaller size of a CID and more convenient interface with the control unit. However, the protection system of CID will normally turn off all gate drive signals as soon as a fault is detected; as a result, the inverter drive will stop operation.

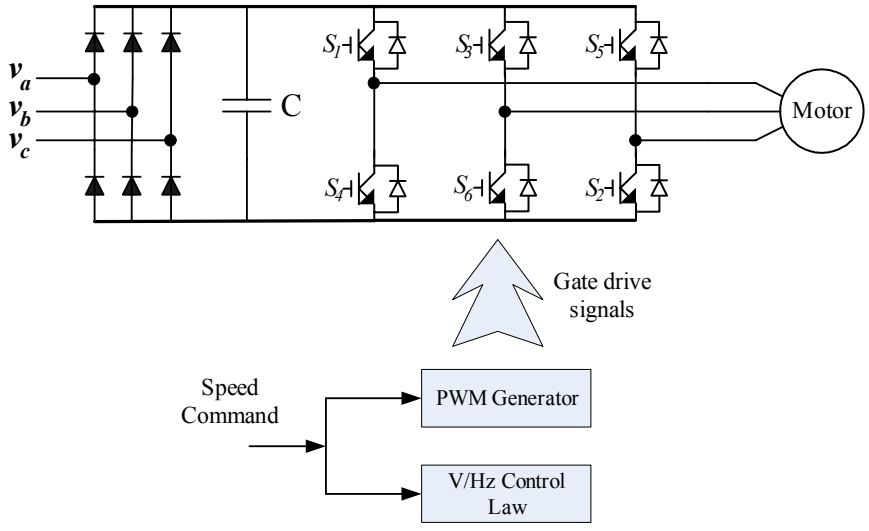


Figure 2.1. Conventional voltage-fed PWM inverter drives.

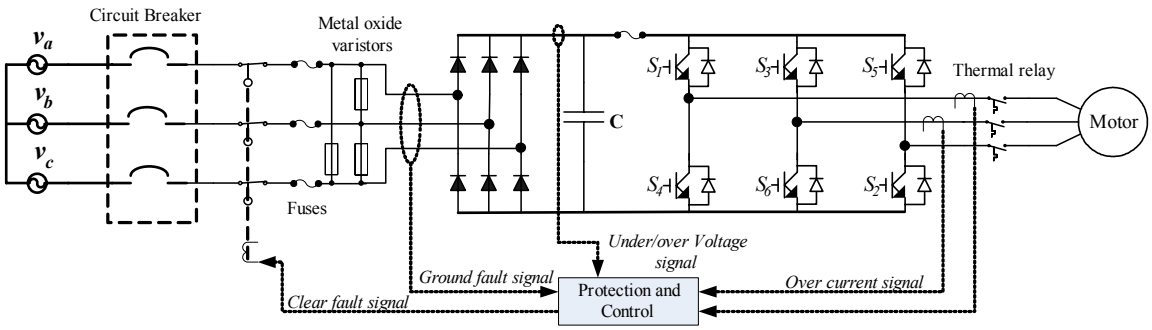


Figure 2.2. A typical protection of a conventional voltage-fed inverter drive.

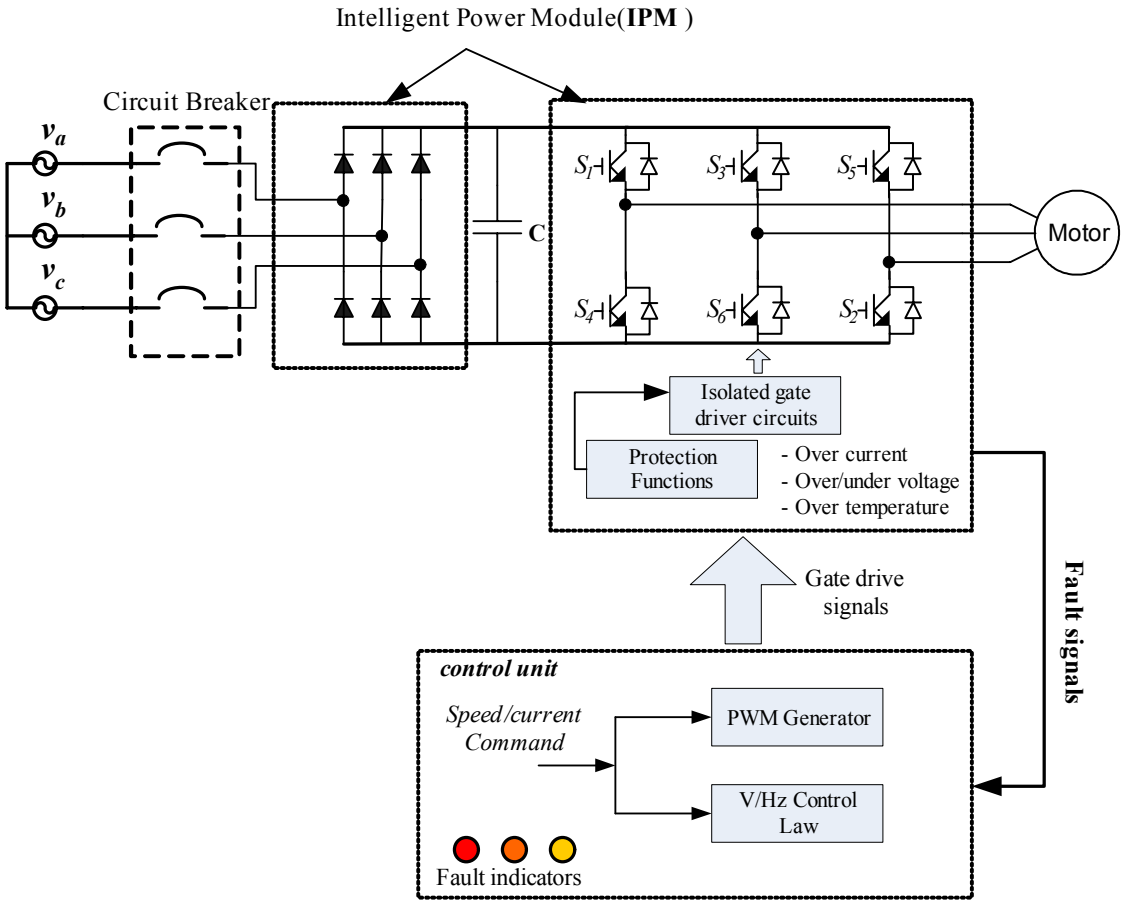


Figure 2.3. A typical protection system of a conventional voltage-fed inverter drive using IPM.

Several research papers on fault detection and reconfiguration for a CID have been elucidated in the last decade of the twentieth century. To begin with, Kastha and Bose [14] have investigated the possible fault modes of a voltage-fed inverter for induction motor drive. The method is based on mathematical model of possible faults and their consequences. The major fault modes based on mathematical models has been analyzed; specifically, input supply single line to ground faults, rectifier diode short circuit, inverter transistor base drive open circuit and inverter switch short circuit conditions. Although the research did not contribute a fault detection method, it provided an extensive study to design the zone of operation safely in a degraded mode of CID, which is important in high reliability applications. In addition, the research conveyed the available signals which can be used to detect particular faults as follows:

- input rectifier current for detecting input supply single line to ground faults;
- dc-link current and voltage for monitoring rectifier diode short circuit fault and over/under voltage;
- input motor current for sensing inverter transistor base drive open circuit and inverter switch short circuit fault.

Kastha [15, 16] also provided a single phase operation technique for a CID when a fault occurs in a leg of a CID; particularly, base drive open circuit and device short circuit. Assuming that the fault could correctly be detected and isolated, a CID could operate with a single-phase mode. The technique is based on torque compensation at an induction motor by injecting odd harmonic voltages at appropriate phase angles. In the next section, fault detection in an inverter of a CID system is described.

2.3 Fault diagnosis in an inverter of a CID system

A CID system usually consists of three cascaded subsystems: a rectifier, an inverter, and a motor. A review of fault detection techniques in an inverter is focused in this section. As previously mentioned, input motor supply current signals could be used to detect switch base drive open circuit and inverter switch short circuit fault. Two techniques are primarily applied in fault detection and diagnosis: model based technique and model-less based technique.

A model-based technique principally depends upon a mathematical model; for instance, analytical redundancy method and parameter estimation method. A model based technique is valuable if an accurate model of faults can be obtained. However, in the case of a CID, an accurate model representing all of the possible fault cases is difficult to obtain. A model based technique has some disadvantages as follows:

- expensive in engineering time to develop model;
- model may not be robust to nonlinear problems;
- model may not be robust to seasonal changes or plant degradation.

A model-less based technique is based upon expert-knowledge or artificial intelligent system; namely, a fuzzy logic, a neural network, and a statistical technique. An implementation of a model-less technique may be more expensive than a model based technique; however, the technology promise of very large scale integration (VLSI)

technology would reduce the implemented cost. Some advantages of a model-less based technique are as follows:

- model-less techniques are mostly non-linear;
- model-less techniques have input-output mapping and adaptivity: the model can be trained to perform a desired mapping;
- model-less techniques have fault tolerance capability: the failure of single neuron will only partially degrade performance;
- model-less techniques can be implemented as VLSI and parallel configuration.

2.3.1 Park's vector approach

A well-known Park's transform or Park's vector approach can be used to perform fault detection in a CID. The interaction between the rotor currents and the flux wave relating with stator currents can be written in primarily mathematical transformation called Clark-transform and Park-transform. A Clark-transform is a signal transformation method to transform the original three-phase signals (for example current signals: i_a, i_b, i_c) into two-phase signals in a new space (i_α, i_β) with an orthogonal basis (i_α is perpendicular with i_β). The i_α and i_β in the stationary frame can be transformed to the current components in the reference or *d-q* frame (i_{sd}, i_{sq}) with Park transform. The i_{sd}, i_{sq} together with instantaneous flux angle (φ), calculated by the motor flux model can be used to estimate the electric torque of an induction motor. The transformation using Clark transform to modify a three-phase system to a two-phase orthogonal alpha (α) and beta (β) system is shown in (2.1):

$$
\begin{aligned}
i_\alpha &= \frac{2}{3} i_a - \frac{1}{3}(i_b + i_c), \\
i_\beta &= \frac{1}{\sqrt{3}}(i_b - i_c), \\
i_0 &= \frac{1}{3}(i_a + i_b + i_c),
\end{aligned}
\tag{2.1}
$$

where i_α and i_β are components in an orthogonal space,

i_o is a homopolar component of the system,

i_a,i_b,and i_c are components in original space.

Assuming that the CID has a balanced load: $i_a+i_b+i_c = 0$, i_α and i_β can be rewritten as:

$$
\begin{aligned}
i_\alpha &= i_a, \\
i_\beta &= \frac{1}{\sqrt{3}} i_a + \frac{2}{\sqrt{3}} i_b, \\
i_a + i_b + i_c &= 0.
\end{aligned}
\tag{2.2}
$$

The transformation from a two-phase orthogonal α, β space to a three-phase stationary component is performed by

$$
\begin{aligned}
i_a &= i_\alpha, \\
i_b &= -\frac{1}{2} i_\alpha + \frac{\sqrt{3}}{2} i_\beta, \\
i_c &= -\frac{1}{2} i_\alpha - \frac{\sqrt{3}}{2} i_\beta.
\end{aligned}
\tag{2.3}
$$

The components of two-phase orthogonal α, β space can be fed to a vector rotation block where it rotates over an angle (θ) to follow the frame d, q attached to the rotor flux by using Park transform:

$$
\begin{aligned}
i_{sd} &= i_\alpha \cos(\theta) + i_\beta \sin(\theta), \\
i_{sq} &= -i_\alpha \sin(\theta) + i_\beta \cos(\theta).
\end{aligned}
\tag{2.4}
$$

The vector in the *d-q* frame can also be transformed to *α- β* frame by

$$\begin{aligned} i_\alpha &= i_{sd}\cos(\theta) - i_{sq}\sin(\theta), \\ i_\beta &= i_{sd}\sin(\theta) + i_{sq}\cos(\theta). \end{aligned} \tag{2.5}$$

A graphical relationship of current vector among original stator components (i_a,i_b,i_c), two-phase components in stationary space (i_α, i_β), and two-phase components in reference space (i_{sd}, i_{sq}) is depicted in Figure 2.4.

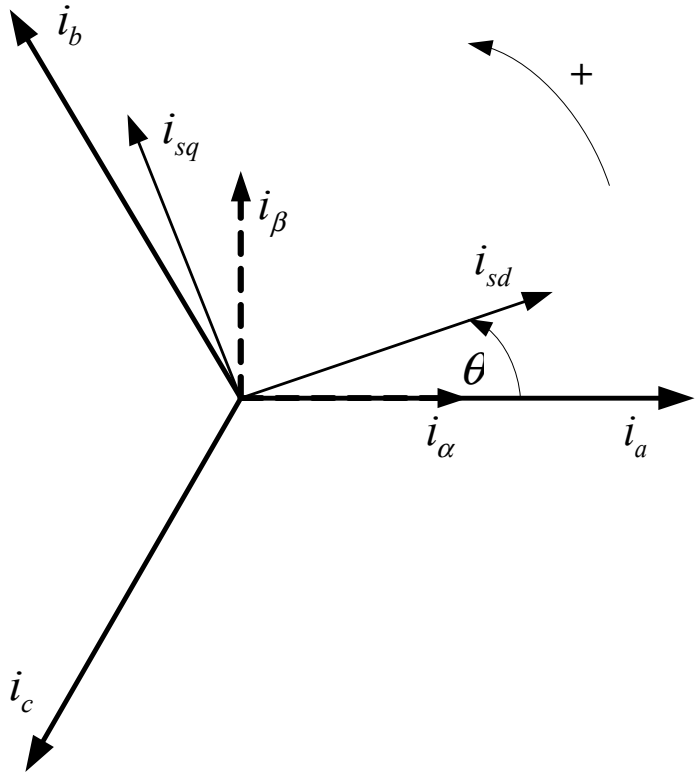


Figure 2.4. Current vector relationship among *a-b-c*, *α- β*, and *d-q* space.

Mendes introduced a monitoring technique for fault diagnosis in a CID based on Park' vector approach [17, 18], namely average Park's vector. Peuget also proposed a fault detection and isolation on a CID [19], called current-vector trajectory. Basically, Mendes and Peuget used input motor currents as diagnostic signals and modified the original Clark and Park transform method as fault feature extraction to rate input motor current signals as an important characteristic in order to classify a fault location in an inverter. The difference between Mendes's work and Peuget's work is the diagnostic paradigm to indicate fault locations (power switch of an inverter).

First, Mendes used average current Park's vector ($I_{a,av}$, $I_{b,av}$, and $I_{c,av}$) to detect a fault. The corresponding Park's vector can be expressed as follows:

$$\begin{aligned} &\left|\bar{I}_{d,av}\right|\angle\theta_{av} = I_{d,av} + j\, I_q\,, \\ &I_{d,av} = \frac{\sqrt{2}}{\sqrt{3}} I_{a,av} - \frac{1}{\sqrt{6}} I_{b,av} - \frac{1}{\sqrt{6}} I_{c,av}, \\ &I_{q,av} = \frac{1}{\sqrt{2}} I_{a,av} - \frac{1}{\sqrt{2}} I_{c,av}\,. \end{aligned} \tag{2.6}$$

The input motor currents are average value over one period. The magnitude and phase angle of the average vector ($I_{d,av}$, $I_{q,av}$) can be calculated in the complex coordinate. Obviously, the average current vector in orthogonal space runs in a circuit will be zero for a normal condition of a CID. In contrast, the magnitude of the vector will not be zero if a fault occurs; normally, the magnitude will exceed some threshold value. The average phase angle can be used to identify a fault location. Trajectories of Park's vector corresponding with the inverter switch locations (Figure 2.3) are illustrated in Figure 2.5.

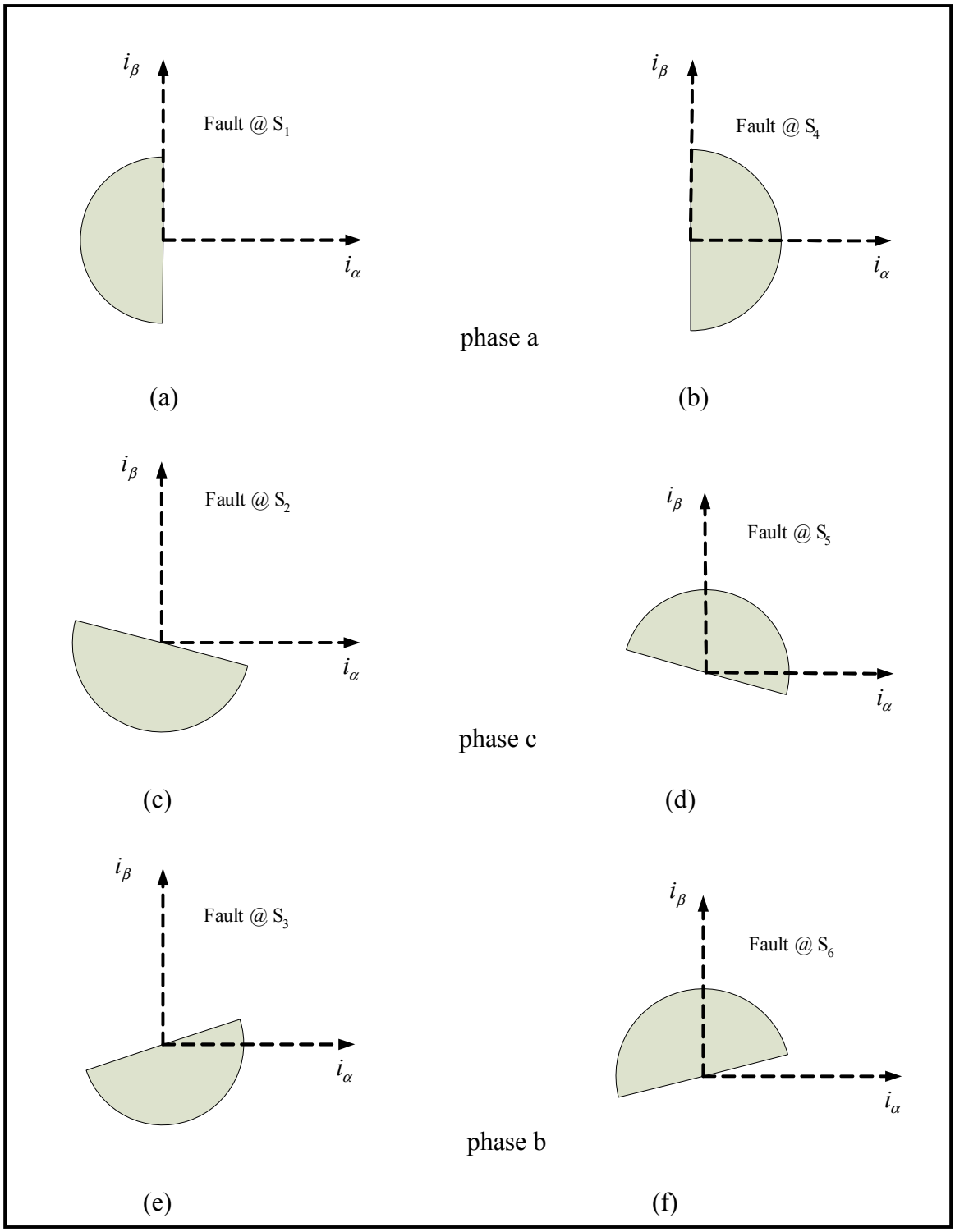


Figure 2.5. Current-vector trajectories in open circuit fault mode: (a) S_1, (b) S_4, (c) S_2, (d) S_5, (e) S_3, and (f) S_6 [19].

The magnitude can be used to determine the fault types (open or short circuit) by setting the threshold value: threshold values are usually based on experiment or simulation. The average angle can be used to identify a fault location as shown in Table 2.1.

Second, Peuget used the slope of trajectory in the orthogonal space to identify fault locations. The trajectory of input motor current is transformed by modifying (2.2) and (2.3). It should be noted that (2.3) assumes a balanced load. Equations (2.2) and (2.3) can be rewritten in terms of line currents as:

$$\begin{aligned} i_\alpha &= i_a, \\ i_\beta &= \frac{1}{\sqrt{3}}(i_b - i_c). \end{aligned} \tag{2.7}$$

Table 2.1. Interval of θ_{av} to identify fault locations

Switch locations	*Open circuit fault*	*Short circuit fault*
S_1	$150^o < \theta_{av} < 210^o$	$330^o < \theta_{av} < 30^o$
S_2	$210^o < \theta_{av} < 270^o$	$30^o < \theta_{av} < 90^o$
S_3	$270^o < \theta_{av} < 330^o$	$90^o < \theta_{av} < 150^o$
S_4	$330^o < \theta_{av} < 30^o$	$150^o < \theta_{av} < 210^o$
S_5	$30^o < \theta_{av} < 90^o$	$210^o < \theta_{av} < 270^o$
S_6	$90^o < \theta_{av} < 150^o$	$270^o < \theta_{av} < 330^o$

As can be seen in Figure 2.5, the trajectories consist of a non-linear part (semicircle) and a linear part (line). The slope (m) of the linear part can be found by:

$$m = \frac{\Delta i_\beta}{\Delta i_\alpha}. \tag{2.8}$$

One can see in Figure 2.5 that the slope is related with an inverter phase leg; for example, if a switch in phase b has an open circuit fault, the current i_b is zero, then the slope of this trajectory is $\frac{1}{\sqrt{3}}$. The same topology can be applied to other phases of a CID as follows:

- fault at phase a, i_a is zero: then, the slope of the trajectory (m) is infinite (∞);
- fault at phase b, i_b is zero: then, the slope of the trajectory (m) is $\frac{1}{\sqrt{3}}$;
- fault at phase c, i_c is zero: then, the slope the trajectory (m) is $-\frac{1}{\sqrt{3}}$.

The currents in the faulty phase can be used to determine the faulty switch in the faulty phase leg. If the current has negative direction, the switch connected with the positive dc link has a fault. Conversely, if the current has positive direction, the switch connected with negative dc link has a fault. A Schmitt-trigger circuit can be used to monitor the direction of currents: a hysteresis loop of a Schmitt-trigger can be set to observe current polarity for the slope method.

The Park's transform approaches are simulated by using PSIM from Powersim and MATLAB from Mathworks. PSIM is used to simulate the power circuit of a CID consisting of a rectifier, an inverter and a motor; then, the current signals are sent to perform Park's vector in MATLAB as illustrated in Figure 2.6. To create an open gate

drive fault, the drive signal for a particular switch is bypassed to ground (0); for instance, if switch S_1 has open gate drive fault, the gate drive signal of the switch S_1 is controlled to zero. Current signals after simulation are sent to Matlab and transformed to orthogonal space. The results of current trajectories in orthogonal space are shown in Figure 2.7.

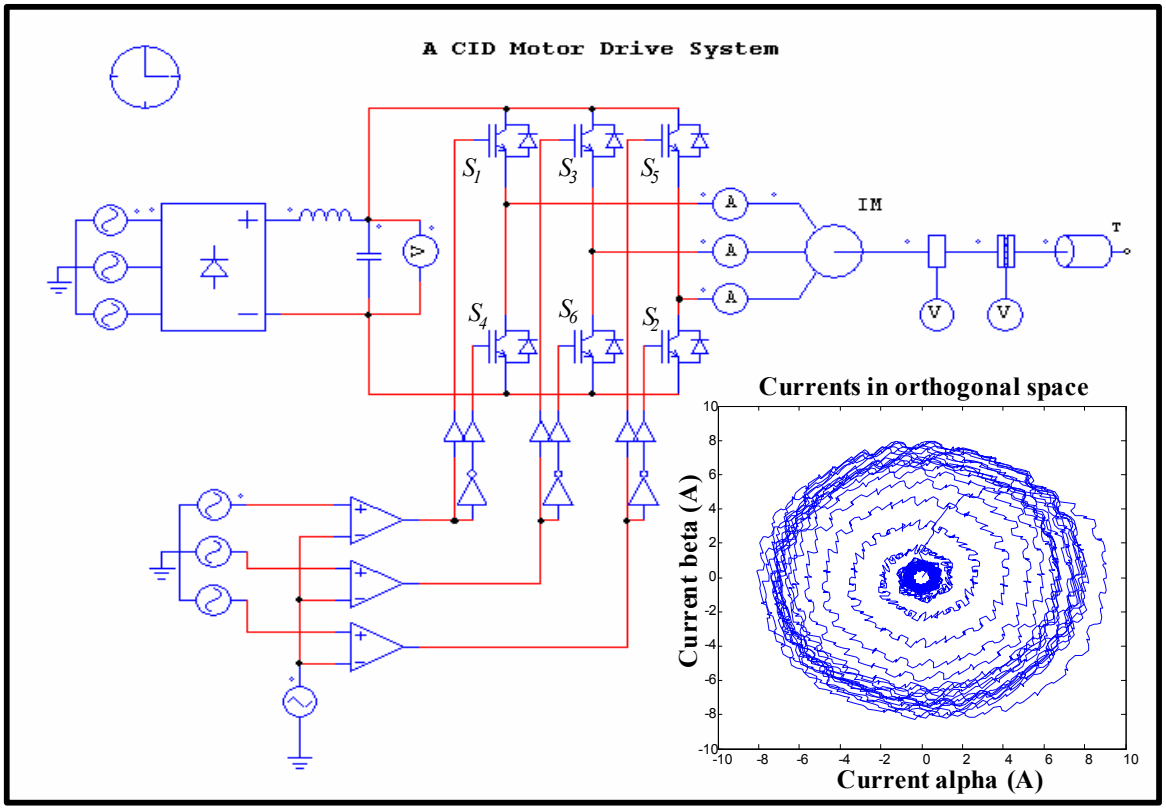


Figure 2.6. Power circuit of a CID simulated by PSIM with current trajectory at normal condition.

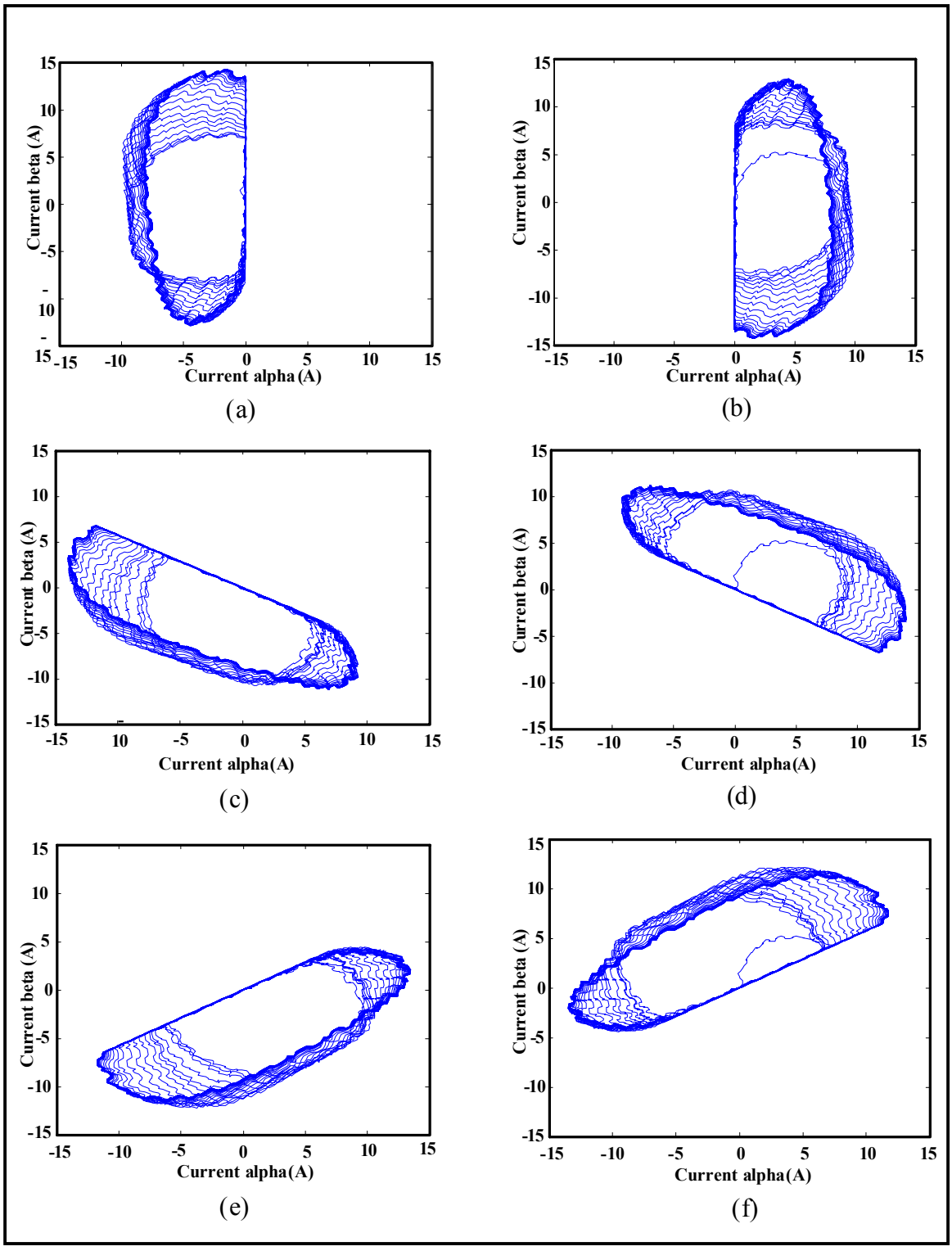


Figure 2.7. Simulation results of current trajectories on open circuit faults: (a) S_1, (b) S_4, (c) S_2, (d) S_5, (e) S_3, and (f) S_6.

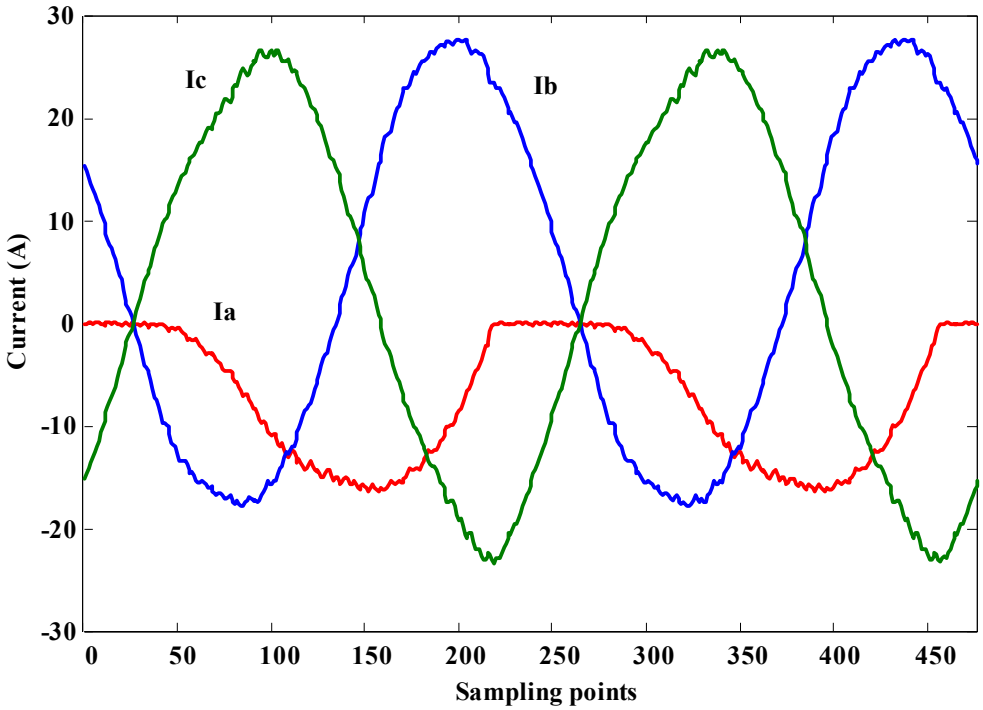


Figure 2.8. Line currents during open circuit faults at S_1.

Figure 2.8 shows the plot of line currents during open circuit at switch S_1. Obviously, the currents in orthogonal space are related with the switch locations as shown in Figure 2.7. The several locus curves at the same plot of each current trajectory are the current cycles of the motor. Obviously, slope detection and Park's average vector method may have a problem to detect the faults when the CID is running at light load or at low modulation index. As represented in Figure 2.7, the vector angle in orthogonal space is dependent with the load currents; for instance, if the fault occurs at S_6 during light load operation, the vector angle of S_3 and S_6 is located at the same interval as depicted in Figure 2.7 (d) and (f). Also, the switch S_3 and S_6 are placed in different inverter legs so that the detection system using slope detection and Park's average vector method would be incorrectly detected.

2.3.2 Control signal observer approach

Kral [20] introduced a monitoring method in a feedback CID by using the deviation between the reference current signal and the actual current signal as a diagnostic signal. The actual motor line currents can not track the reference current of the control unit when the faults occur. The detection technique is based on the observation of amplitude and phase of the deviation current. The DFT (discrete Fourier transform) is utilized for feature extraction; subsequently, the ratio of a fundamental component and a dc component is the fault indicator (f_{ind}) to determine faults. Also, the angle of the fault indicator ($\theta_{f_{ind}}$) can be used to identify fault locations as shown in Table 2.2. The threshold value of fault indicator is 0.5: this value is derived from several simulation results [20]. If the fault indicator is more than 0.5, the CID has an open circuit fault. The mathematical expression of this approach is explained as:

$$\begin{aligned}
\Delta i_s &= i_{s,ref} - i_{s,act} = \sqrt{\left(I_{d,ref}^2 - I_{d,act}^2\right)^2 + \left(I_{q,ref}^2 - I_{q,act}^2\right)^2}, \\
C^m &= \frac{1}{N}\sum_{k=0}^{N-1} \left|\Delta i_{s,k}\right| e^{\frac{j2\pi mk}{N}}, \\
f_{ind} &= \frac{C^1}{C^0} \begin{cases} if\ |f_{ind}| > 0.5, then\ fault \\ if\ |f_{ind}| < 0.5, then\ no\ fault \end{cases}, \\
\theta_{f_{ind}} &= \arctan\left[\frac{\mathrm{Re}\{f_{ind}\}}{\mathrm{Im}\{f_{ind}\}}\right],
\end{aligned} \tag{2.8}$$

where N is the total number of points per period,

k is *0,1,2…N-1*.

Table 2.2. Location of the faulty switch

Switch locations	*Fault indicator*	*Condition*
S_1	> 0.5	$\lvert \theta_{f_{ind}} \rvert < 30^o$
S_2		$30^o < \theta_{f_{ind}} < 90^o$
S_3		$-150^o < \theta_{f_{ind}} < -90^o$
S_4		$\lvert \theta_{f_{ind}} \rvert > 150^o$
S_5		$90^o < \theta_{f_{ind}} < 150^o$
S_6		$-90^o < \theta_{f_{ind}} < -30^o$

The advantage of this approach is that fault detection algorithm can be integrated in the control unit with a single digital signal processor (DSP), and also the extra measurements are not required. However, the subroutine software of the DSP must be modified, and this might degrade the execution speed of the main software in the DSP.

2.3.3 Normalized dc current approach

Abramik [21] proposed a diagnostic method for a CID, namely the normalized dc current method. The concept of the method is to use normalized dc current instead of the currents transformed to orthogonal space. The normalized dc current is the ratio between the dc component and the fundamental component. The fault observer is based upon the relationship of normalized dc current in each phase. To illustrate this, for instance, the current spectrums (i_a and i_b) of the open circuit fault at switch S_1 are shown in Figure 2.9.

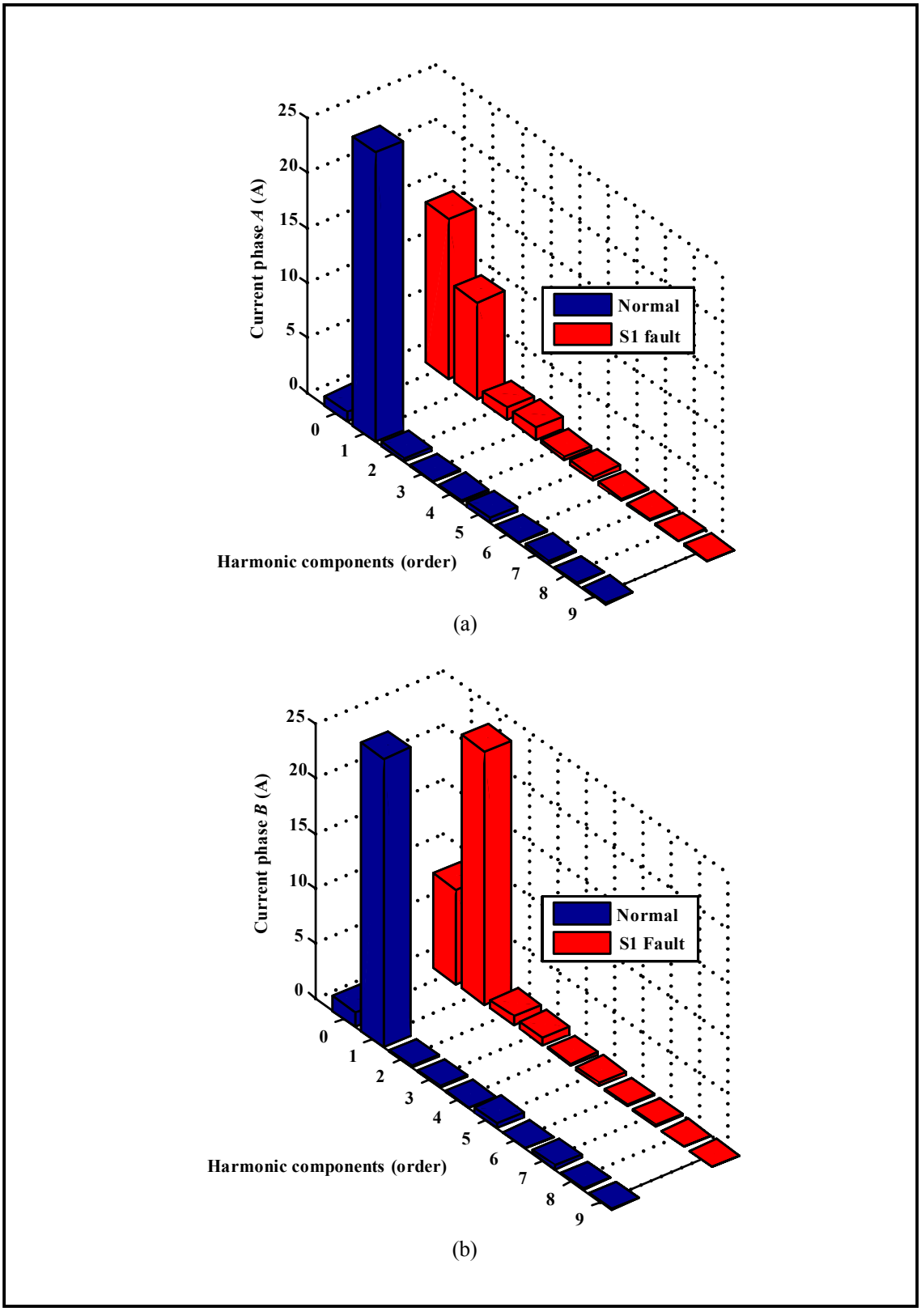


Figure 2.9. Current spectrum of i_a and i_b during normal and open circuit fault at S_1: (a) line current at phase A (i_a), and (b) line current at phase B (i_b).

Obviously, the dc component of the currents in both phases is not zero during faults as shown in Figure 2.9, and the fundamental component of a faulty phase (phase A) is smaller then a fundamental component of related phase (phase B); hence, the properties of current spectrums can be applied to detect the faults and localize the faulty switch of a CID. To achieve this, the recursive DFT algorithm is applied to calculate fundamental component and dc components of three-phase line currents. The threshold value of 0.45 is used as fault indicator; this threshold is derived from experience [21]. A fault is detected when the threshold is exceeded (> 0.45) in one phase, whereas the other phases are below the threshold value (< 0.45) and have the reverse polarities with respect to the faulty phase. The decision making rules using binary codes to detect and localize the faults are illustrated in Table 2.3.

Table 2.3. Diagnostic rules for open circuit faults.

Switch locations	*Binary codes for fault diagnosis*					
	$\frac{I_{av,A}}{I_{1,A}}$		$\frac{I_{av,B}}{I_{1,B}}$		$\frac{I_{av,C}}{I_{1,C}}$	
S_1	1	0	0	1	0	1
S_2	0	0	0	0	1	1
S_3	0	1	1	0	0	1
S_4	1	1	0	0	0	0
S_5	0	1	0	1	1	0
S_6	0	0	1	1	0	0

As can be seen, two binary bits are used in each phase; the left hand side bit and the right hand side bit. First, the left hand side bit is used to indicate when a normalized dc current exceeded the threshold or not; "0" is the normalized dc current lower than the threshold, whereas "1" is the normalized dc current more than the threshold. Second, the right hand side bit is used to determine the polarity of currents; "0" is negative current, while "1" is positive current. The mathematical expression of recursive DFT is represented as follows:

$$
\begin{aligned}
i_1(k\tau) &= a_1 \cos\left(\frac{2\pi}{T} \times k\tau\right) + b_1 \sin\left(\frac{2\pi}{T} \times k\tau\right), \\
a_1 &= \frac{2}{N} \sum_{k=1}^{N} i(k\tau) \cos\left(\frac{2\pi k}{T}\right), \\
b_1 &= \frac{2}{N} \sum_{k=1}^{N} i(k\tau) \cos\left(\frac{2\pi k}{T}\right), \\
i_{av}(k\tau) &= \frac{1}{N} \sum_{k=1}^{N} i(k\tau),
\end{aligned}
\tag{2.9}
$$

where N is a total number of points per period,

k is *0,1,2…N-1*,

τ is a sampling period ($\frac{T}{N}$).

The advantage of the normalized dc current method is that the diagnostic variables (normalized dc currents) are independent with motor load; whereas, average Park's vector approach is dependent with motor load. The current components in an orthogonal space will be small when the motor is running at light load; this might cause an incorrect identification of the fault location.

Rothenhagen also proposed the diagnostic method, namely modified normalized dc current [22]. This method basically uses the same algorithm as the normalized dc current; however, a less restrictive way to locate a faulty switch is conducted. The performance of previously discussed diagnosis for open circuit faults in voltage source inverter has been investigated by Rothenhagen in [22] for active rectifier application and [23] for drive application. The report of Rothenhagen's works can be summarized in Table 2.4. "Y" means the fault is detected, "N" means the fault can not be detected, and "(Y)" means the fault detection is ambiguous (sometime the fault can be detected and sometime the fault can not be detected).

Table 2.4. Performance of diagnostic methods reported by Rothenhagen.

Diagnostic method	*Active rectifier*				*Conventional Inverter drive*			
	Frequency (Hz)	*Current (A)*			*Frequency (Hz)*	*Current (A)*		
		30	*6*	*1.2*		*6.8*	*3.4*	*0.7*
Park's vector	50	Y	Y	(Y)	50 25 10	Y Y Y	Y Y Y	Y N N
Slope detection		Y	Y	N	50 25 10	Y Y Y	N (Y) Y	N N N
Control signal observer		Y	Y	(Y)	50 25 10	No Report		
Normalized dc current		Y	Y	N	50 25 10	Y Y N	Y Y Y	N N N
Modified normalized dc current		Y	Y	Y	50 25 10	Y Y Y	Y Y Y	Y Y N

As illustrated in Table 2.4, most diagnostic methods have problems to detect the faulty switches at low current in both applications; more specifically, at low speed for drive application, most methods have poor performance. This result suggests that normalized dc current using recursive DFT algorithm as feature extraction would be a more reliable approach for fault diagnosis in a CID system.

Rothenhagen also reported a consumed detection time of the diagnostic methods as summarized in Table 2.5. The fastest method is normalized dc current method for active rectifier application, whereas the slowest method is control signal observer. For drive application, one can see that the diagnostic system consumes more detection time at low speed operation than high speed operation. A study shows that the detection time may be different at different operating points.

Table 2.5. Consumed detection time of diagnostic methods reported by Rothenhagen.

Diagnostic method	*Active rectifier*		*Conventional Inverter drive*			
	Operating point	*Detection time (ms)*	*Operating point*	*Detection time (ms)*		
				Average	*Min*	*Max*
Park's vector	6 A, 50 Hz	5	No Report			
Slope detection		10				
Control signal observer		20				
Normalized dc current		3				
Modified normalized dc current		5	7 A, 50 Hz 7 A, 25 Hz 7 A, 10 Hz	15.90 25.85 61.56	6.6 9 17	25 42 111

2.3.4 Artificial Intelligent based approach

Thus far, one can observe that a diagnostic procedure can be divided into three major steps: feature extraction, fault identification, and corrective action taken. Feature extraction is a process performing the diagnostic signal transformation, with rated signal values as important features; for instance, Park's vector and normalized dc. Input motor current signals are mostly utilized in a CID system. Then, fault identification process performs the rule or decision making to identify fault types and their location; for example, slope detection, angle of current components in orthogonal space, and knowledge-based (threshold set-up) with observation of the current direction. The principal of a corrective action taken process is to clear the fault (bypass a faulty inverter leg) and derating operation (two-phase operation). A comparison of features, cost, and limitations of corrective action topologies in a CID system is investigated in [24]. The input motor current signals in time-domain are mostly used to detect faults from previous research; this is because the magnetizing and torque-producing components are related with the stator currents; therefore, the currents in time domain could identify intermittent faults faster. Smith [25] suggested that fault detection methods based on frequency domain signals are not suitable for condition monitoring with the system required fast response.

Since the recent development of computer program simulations such as Pspice, Matlab, and Psim, the fault behaviors can conveniently be simulated instead of complicated mathematic equations. Moreover, the simulation results can be analyzed to find an appropriate diagnostic signal and can be used as information for knowledge–based

system or training a neural network. Therefore, it is possible that artificial intelligence (AI)-based techniques can be applied in a diagnostic system; especially, in a fault identification process. AI-based techniques would give more degrees of freedom to classify the faults than the rules-based (IF, THEN or *hard limit*) technique. There are several types of AI-techniques: neural network, fuzzy logic and other statistical techniques such as polynomial and regression. Fuzzy logic might be considered a knowledge-based technique. The essence of a knowledge-based technique is the ability to use experience or knowledge to make the rules representing the physical system as a model; whereas, the neural network and other statistical methods are naturally nonlinear function approximation by using a nonlinear relationship between inputs and outputs (supervised learning) or relationship only inputs (unsupervised learning).

Fillippetti [26] presented a general review of recent developments in the field of AI-based diagnostic systems in machine drives. The application of AI-based techniques for monitoring and diagnosis is mostly in a motor. A review of machine signature analysis for fault diagnosis and condition monitoring has been reported in [27, 28]. Basically, electrical, mechanical, and chemical signals can be applied to indicate machine faults such as broken rotor bar, shorted rotor field winding, bearing fault, and stator winding faults; to name a few. Various types of faults and their detection techniques have been proposed from numerous researchers [29]; however, only limited research on fault diagnosis in an inverter drive based on AI- techniques have been published. It is possible that the machine diagnostic system can be combined with the fault possibilities of the converter if the machine is supplied by a CID. Input inverter current, a dc link current or

voltage, and input motor currents would be used as diagnostic signals to detect and identify the faults.

Curea [29-31] anticipated a diagnostic system based on AI-technique: polynomial and neural network approach. Curea reported that output voltages and currents of a converter can be used as diagnostic signals. Also, phasor diagram, Fourier transform, and complex power can be used as a signature extraction. The results of Curea's works show that a neural network provides a better characterization of the involved complex and nonlinear behavior than a polynomial method; however, the polynomial method uses a short computation time and requires less memory and CPU speed.

Diallo [32] proposed a fault diagnostic system for an induction machine drive with a pattern recognition approach. Diallo's method also uses input motor currents signal in orthogonal frame to diagnose the faults and their localization for open circuit faults; however, a probabilistic approach is also applied in the feature extraction process. This increases the robustness of the method against the uncertainties due to measurements of PWM signals. The radial basis function (RBF) neural network architecture is used to classify a normal and abnormal condition by building the healthy boundary of operation area; then a probability of each sector in orthogonal space is calculated by step of 60^{o} so that the sector having highest probability identifies the fault locations. Diallo also reported that the average Park's current vector reveals lack of reliability under faulty condition during light load operation.

Murphy [33] presented a fault diagnostic system in electric drives using machine learning for detecting and locating multiple classes of faults. The open circuit fault is focused in this work because the authors assume that a short circuit fault will eventually burn out and become permanently open circuit. The main point of this research is to propose the machine learning algorithm in training paradigm to find more representative data. A neural network based diagnostic system trained on more representative data is more likely to perform a better diagnosis.

Machine learning can be regarded as a subset of AI-based techniques concerned with the development of algorithms and techniques permitting a computer to learn. The proposed machine learning algorithm can automatically select a set of representative operating points of electric drive system to generate signals for training a neural network. Two voltage and current output inverter signals are used as diagnostic signals; then the diagnostic signals are divided into segments. Descriptive statistics of the diagnostic signals in each segment are calculated; descriptive statistics include maximum and minimum magnitude of signals, median and mean values of signals, standard deviation of signals, and dc component of power spectrum. The descriptive statistics of the diagnostic signals in each segment are utilized as a feature extraction. The advantage of using the proposed machine learning algorithm is the diagnostic system can automatically select the control parameters related with the faults to generate signals to train the network with *only simulation signals by using Matlab-Simulink*. Murphy also reported that the proposed diagnostic system effectively detected multiple classes of faults. The prediction accuracy is close to 98% in detecting different classes of faults [33].

2.4 Fault diagnosis in an inverter of a MLID system

As previously mentioned, three different major multilevel converter structures have been reported in the literature: cascaded H-bridges converter with separate dc sources (SDCS), diode clamped (neutral-clamped), and flying capacitors (capacitor clamped). The diagnostic methods applied in a CID can also be used in MLID; however, different multilevel converter structures may need different fault diagnostic and reconfiguration methods. A fundamental concept of multilevel inverter operation will not be provided here; however, a distinguished introduction and application of multilevel inverter has been provided by [34].

2.4.1 Diode clamped MLID

Diode clamped MLID is also known as neutral-point clamped (NPC) MLID. Park [35] proposed the control method of NPC inverter for continuous operation under one phase faults. The possible schematic of three-phase NPC inverter is shown in Figure 2.10. Three triacs are placed between the diode-clamped center tap and the phase output terminal; these triacs allow the current to flow from neutral point to the load during the faults. Thus, with bypassing the faulty leg, NPC can continuously operate under fault conditions. Park also provided the neutral point voltage control method based on space vector pulse width modulation to control the balance voltage at neutral point. The fault detection based on Park's vector approach for NPC-MLID has been proposed in [36]. The simulation of open circuit faults is represented in Figure 2.11. As can be seen, the method may incorrectly detect a fault at light load operation due to current dependence.

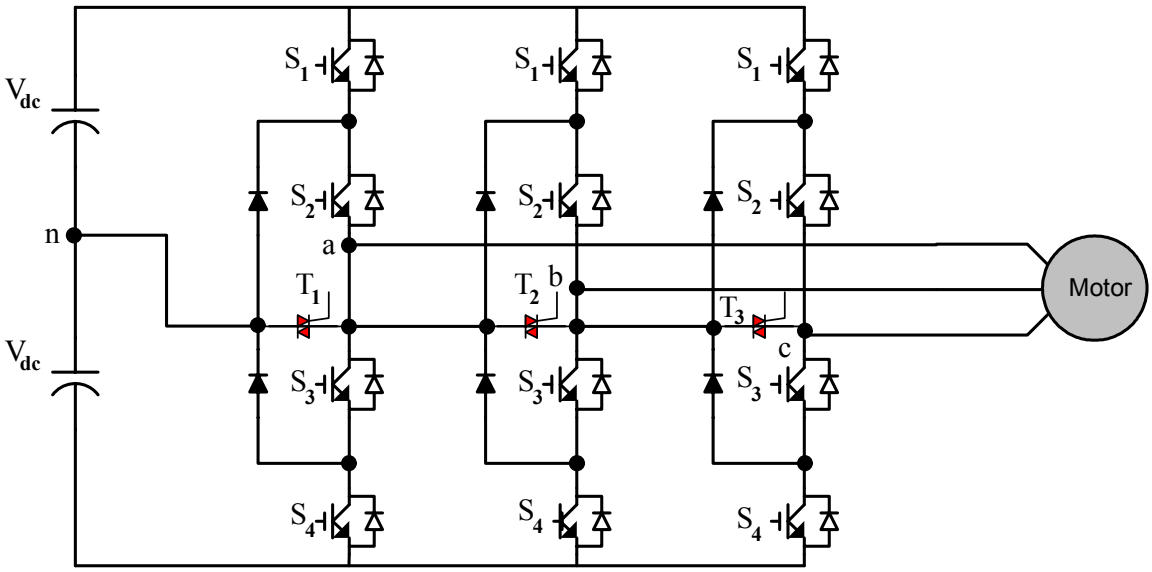


Figure 2.10. Schematic of three-phase diode clamped MLID with fault tolerance.

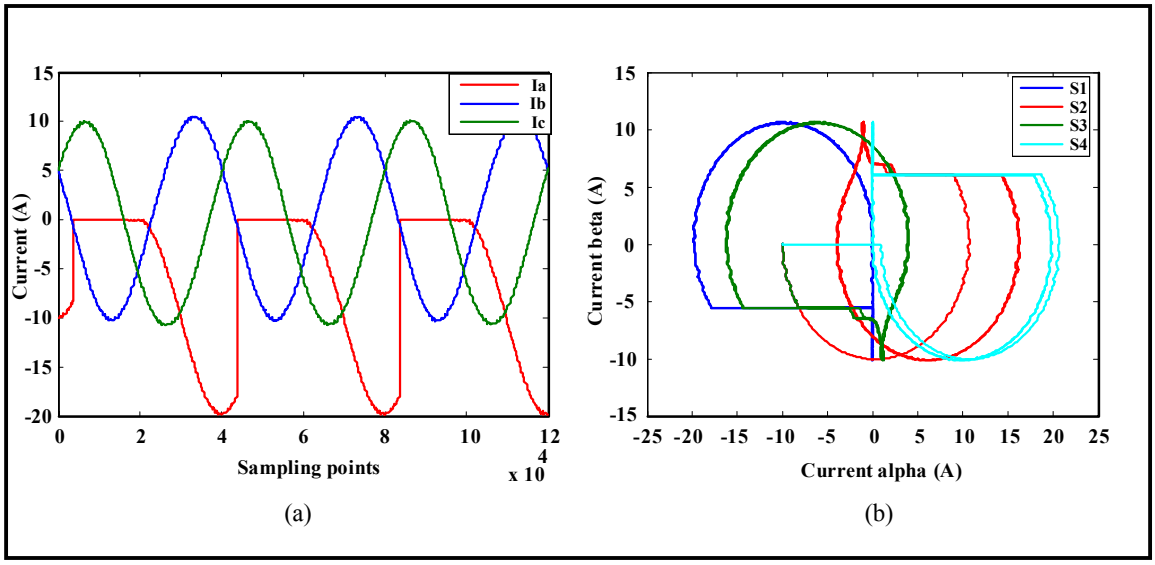


Figure 2.11. Input motor currents during open circuit faults:
(a) Currents of open circuit fault at S_2 of phase A, (b) Currents in orthogonal space for each switch.

2.4.2 Flying capacitor MLID

Kou and Corzine [37] presented a unique fault tolerant design for flying capacitor multilevel inverter. The proposed schematic of flying capacitor with fault tolerance is illustrated in Figure 2.12. Additional SCRs in parallel to power switches can bypass the faulty devices, when faults occur whether open or short circuit faults. Also, two more switches are added to the dc branch in each phase in order to disconnect the related dc branch during a fault. For example, if S_1 has an open circuit fault, S_1 will be bypassed as soon as the fault is detected, then S_6 is forced to be turned on and T_1 is needed to be turned off. The advantage of this scheme is that it can provide the same number of converting voltage levels if a single switch is failed per phase. Thus far, fault diagnosis and fault detection of flying capacitor MLID have not been reported in literatures.

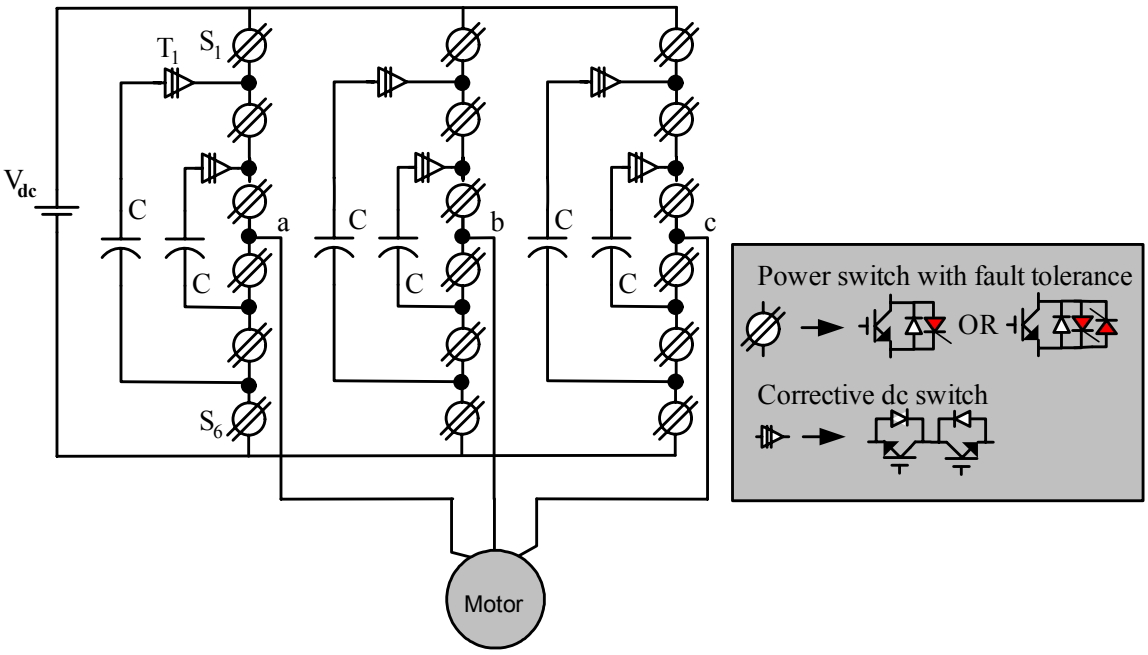


Figure 2.12. Three-phase four level flying capacitor MLID with fault tolerance.

2.4.3 Cascaded H-bridges MLID

Fault diagnostic method for cascaded H-bridges MLIDs to detect switch fault and location have not been reported in literature so far; however, the fault detection for a faulty power cell using fiber optic has been reported in [9]. The cascaded H-bridge MILD has been installed for fluidized-bed catalytic cracking unit (FCCU), which use 5,000 hp motor. This MLID has a bypass-contractor in each power cell to bypass during cell failure as depicted in Figure 2.13. Figure 2.13 shows that if faulty power cells are correctly detected, the bypass-contractor will turn on to bypass the power cell. As previously mentioned, a failure in a power cell causes unbalanced voltages. To solve unbalanced voltages, one possible method is to bypass an equal power cell in all three phases although power cells of other phases may not have malfunction. This method could solve unbalanced problems, but the method sacrifices possible voltage capability.

Hammond [38] proposed a corrective action taken to balancing output voltages for MLID called neutral shift (NS). The NS permits the extra power cell in one phase to partially compensate for a failure from other phases. The essence of NS is the adjustment angle of neutral point of three phase wye-connection system as shown in Figure 2.14. Obviously, the phase-voltages (V_{AN},V_{BN},V_{CN}) are not out of phase with each other by 120^{o} as usual; however, the line-voltages (V_{AB},V_{BC},V_{CA}) are balanced even though two power cells on phase *C* and one power cell on phase *A* are malfunctioning. The neutral shift provides more voltage available after faulty cells than an equal bypass method. The calculation of the reference signal to adjust neutral point angle is provided in [11], and the comparison of control schemes for cascaded MLID with faulty cell has been investigated in [39].

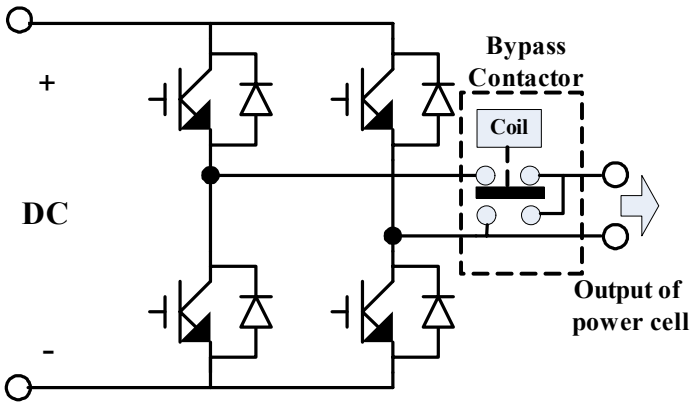


Figure 2.13. A typical power cell with bypassed ability.

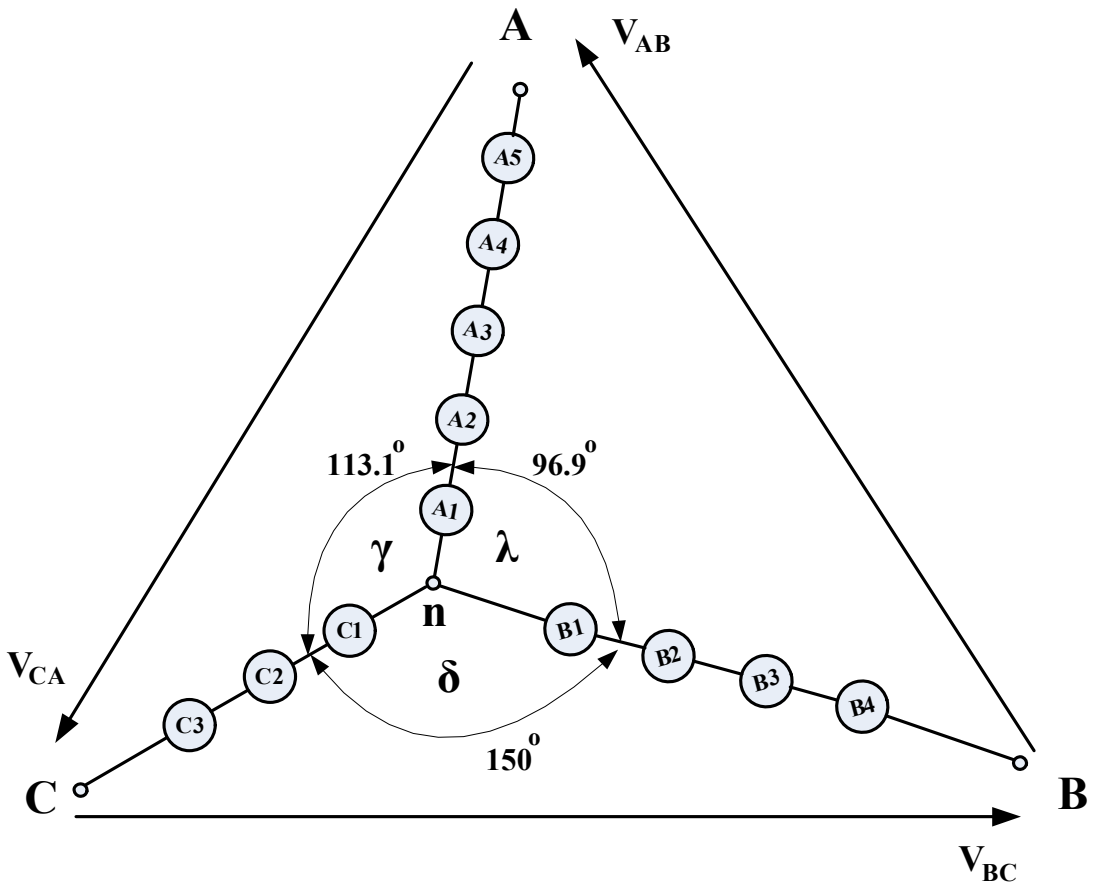


Figure 2.14. Rebalanced output voltage by adjusting phase angle of neutral point.

2.5 A promising support for AI-based fault protection in MLID

Since the objectives of this dissertation is for a diagnostic system for a MLID based-on AI-based technique, the survey of available manufacturing supports to implement the proposed method should be scrutinized. Two promising technologies are focused in the section: power switch devices and AI-based implementation.

2.5.1 Modular power switch for a MLID

The new generation of power semiconductor switches for a CID is mostly designed as modular package known as intelligent power module (IPM). Besides, the promising power switch used for a MLID should also be modular package. CT-concept technology Ltd provides a unique power switch module for diode-clamped MLID as shown in Figure 2.15. Figure 2.15(a) is the intelligent gate drive of the 1SD210F2 SCALE series (6.5 kV, 600 A) including a mounting protection and gate drive circuits. The external mounting board consists of the gate drive and protection circuit; the gate drive signals transmit via fiber optic interface and a V_{CE} voltage monitoring is depicted in Figure 2.15 (b). This power module is a "plug and play" solution meaning the users can select how many levels to use for the MLID application by selecting a jumper on the mounting board. However, the protection method of this power module is based on turning off gate drive signals, so the MLID must be stopped as soon as the fault is detected even though one switch is failed; hence, it would be better if the power module would have a function to reconfigure the MLID after the faults and their locations are detected.

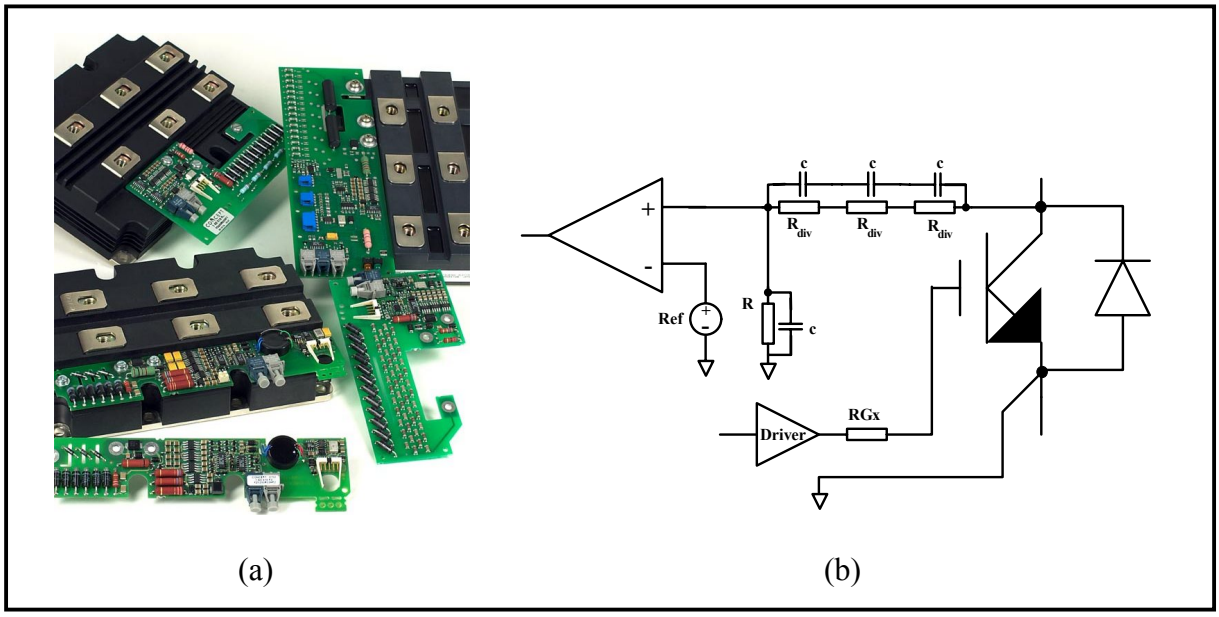


Figure 2.15. Modular power switch for a MLID 600 A/6500 V of CT-concept technology Ltd: (a) Product photo [40], (b) Voltage V_{CE} monitoring circuit.

It is possible that the function of fault detection, diagnosis, and reconfiguration can be integrated with the intelligent power module as a mounting board in Figure 2.15(a). Although the illustrated power module is used for diode clamped MLID, one would expect that the cascaded H-bridge module should be the same direction. The H-bridge power module may consist of four switches as a cell; as a result, the replacement of a failed power cell is convenient, and the bypass ability of a failed power cell is available.

The output phase-voltage signals can be detected by using a simple voltage divider technique as shown in Figure 2.15 (b); however, the percent error of resistors should be extremely small (0.1 %) with high frequency response since the output voltages are PWM

waveforms. It is evident that the use of voltage divider method can provide a small size of the mounting board as shown in Figure 2.15 (b); also, the signals from V_{CE} monitoring circuit mounting with power module can be used to calculate the output phase-voltage signals. In addition, International Rectifier also provides an integrated circuit (IC) for voltage sensor and short circuit protection for a CID [41]. Thus far, the promising power module and a voltage sensor are commercially available; therefore, it is optimistic that a fault diagnostic technique can use the output voltages of MLID to be diagnostic signals.

2.5.2 Hardware Implementation of AI-based diagnosis

One controversy of using neural networks or other AI-based diagnostic techniques is how to do a hardware implementation with a complicated activation function used in a neuron (sigmoid). As known, the neural network can be coded to training the network via software, such as Matlab, C language, Basic language, and Excel. After one finishes the training process, the final weight and bias matrices are parameterized to perform an input/output mapping; therefore, these weight and bias matrices would need to be implemented in the hardware. It is optimistic that the weight and bias matrices can be implemented in hardware for any "analog or digital solutions".

Analog solutions are based on a saturated operational amplifier (OP-AMP) for linear activation function and push-pull OP-AMP for sigmoid activation function. Vas [12] provided an example of analog hardware implementation as illustrated in Figure 2.16.

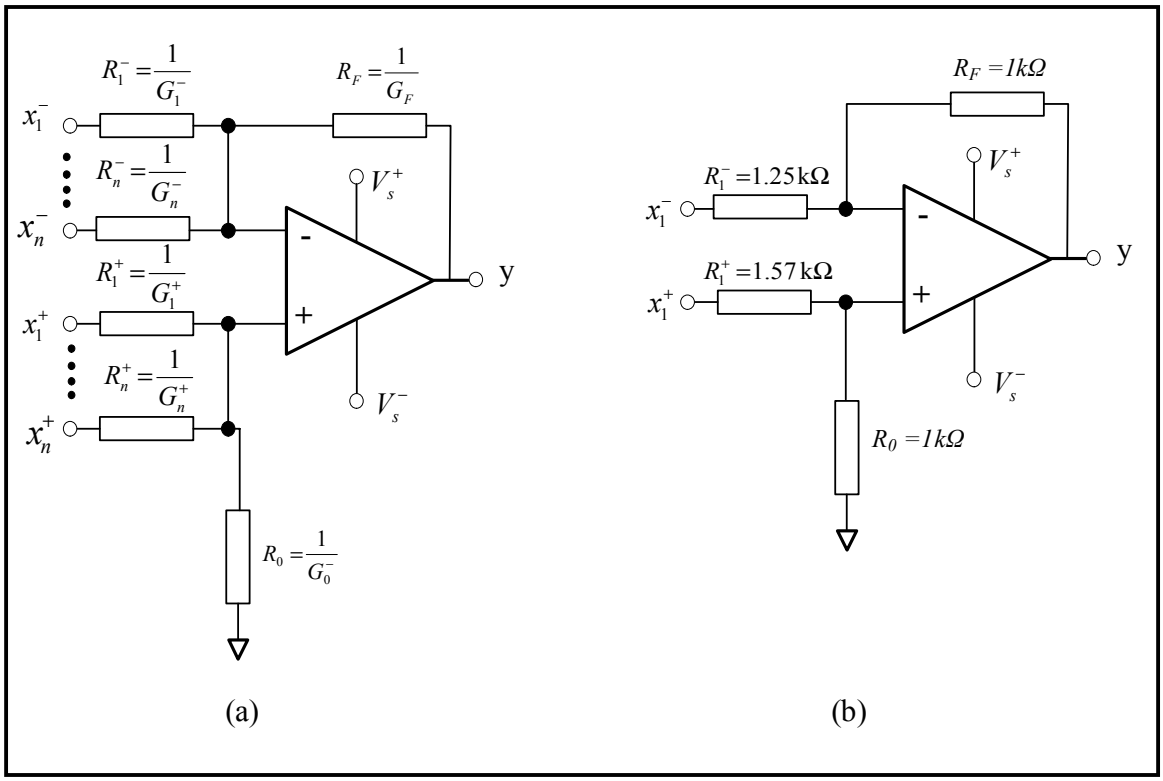


Figure 2.16. Neural network implementation using a saturated OP-AMP: (a) multiple input neurons, (b) an example of two input neurons *($[w_1,w_2]^T = [-0.8, 0.7]^T$)*.

As depicted in Figure 2.16 (a), the negative weights (w_i^-) is $(-R_F.G_i^-)=(-\frac{R_F}{R_i^-})$, where *i* is *1,2,3,...,n* , *G* is conductance, and *n* is the number of negative weights. The positive weights (w_k^+) is $\{1+R_F\sum_{j=1}^{n}G_j^-\}.\left\{\frac{\sum_{k=1}^{p}G_k^+}{\sum_{j=1}^{p}G_j^+}\right\}$, where *k* is *1,2,3,...,p, j* is *0,1,2,...,p*, and *p* is a number of positive weights. Since the activation function (***S**$_{act}$*) becomes $[w^-]^T.[x^-]+[w^+]^T.[x^+]$, the output (*y*) is a function of activation function (*f (**S**$_{act}$)*).

Figure 2.16 (b) shows an example of the weight matrix of two input neurons of $[w_1,w_2]^T = [-0.8, 0.7]^T$. By selecting R_F and R_0 =1 kΩ, the positive and negative resistors can be calculated as shown in Figure 2.16 (b). This example is evident that a neural network can be implemented in hardware based on simple analog circuits; however, the analog circuit will become more complicated in multiple input neurons and multiple neural network layers.

Recently, the development of a digital signal processing (DSP) and a field programmable gate array (FPGA) provides the possibility to implement the neural network in digital solution as a single chip. One can imagine that the several OP-AMPs from an analog circuit can be integrated into a single chip. Additionally, Matlab-Simulink also developed a toolbox based on graphic user interface (GUI) [42]. This toolbox conveys a convenient way to develop the neural network from training process to implementation process; the final weight and bias matrices can convert to be a C^{++} code, and then this C^{++} code can be directly download to the DSP by embedded development tool from DSP or FPGA companies such as Texas Instrument and Traquair. Also, much research has focused to develop the hardware of neural network in adaptive training function, meaning that the neural network card can perform training online by the card itself. Zhang and Li [43] proposed a feed-forward neural network based on FPGA applied for variable-speed wind turbine system. They suggest that FPGA are more suitable than DSP because a FPGA can parallelly execute commands, whereas DSP is naturally series execution.

Thus far, it is optimistic that the fault diagnostic system based on neural network or AI-based techniques can be conveniently implemented as a single chip. The training process could be both off-line and on-line training. In this dissertation, the Opal-RT system will be used to implement the proposed fault diagnostic system. The Opal-RT basically consists of several DSPs in the same board including analog/digital inputs and outputs. The neural network development process will be performed based on Matlab-Simulink until the final weight and bias matrices are achieved. More detail on hardware validation will be clarified in Chapter 5.

2.6 Summary

This chapter has provided the survey of previous research and promising technology of AI-based techniques. It is obvious that numerous fault diagnostic techniques are available for a conventional inverter drive (CID); however, only limited research on multilevel inverter drives (MLID) has been conducted. Most research in a CID used input motor current signals as diagnostic signals. The major difficulty of using current signals is load dependent so that the diagnostic system may have a problem with light load operation because the decision making rules are usually designed at the rated load. It would be better to use a signal which is independent from the load. A fault diagnostic system in cascaded MLIDs by using output voltage signals will be shown in the following chapters

The survey suggests that the design of fault diagnosis consists of three important steps: feature extraction, fault identification, and corrective action taken. The AI-based

technique methodology of fault diagnostic system for a cascaded MLID using output phase-voltage signals are presented in Chapter 3.

3. AI-BASED MLID FAULT DIAGNOSIS

3.1 Introduction

This chapter presents the methodology of the proposed AI-based fault diagnostic system in a cascaded multilevel inverter drive (MLID). Three important steps of the proposed design of fault diagnosis consist of: feature extraction, fault identification, and corrective action taken are clearly illustrated. To expediently understand, a two separated dc sources (SDCS) cascaded MLID (or five levels output phase-voltage MLID) is used as an example in a design process. Also, open circuit faults at each switch are considered, and for illustrative purposes, one level of a multilevel inverter is the focus of this chapter. Although the MLID system usually consists of three phases of H-bridge inverters and can also have short circuit faults, the fault diagnostic system will be the same topology as a single phase and open circuit case. In this research, the fault location in a MLID will be attempted to diagnose from its output voltage waveforms because the output voltages are normally independent from the load and correspond with fault types and locations.

3.2 Structure of fault diagnostic system

The structure for a fault diagnostic system is illustrated in Figure 3.1. The system is composed of three major states: feature extraction, fault identification (neural network classification and fault diagnosis), and corrective action taken (switching pattern calculation with gate signal output). The feature extraction, neural classification, and fault diagnosis are the focus of this chapter. The feature extraction performs the voltage input signal transformation, with rated signal values as important features, and the output of the transformed signal is transferred to the neural network classification. The networks are trained with both normal and abnormal data for the MLID; thus, the output of this network is nearly 0 and 1 as binary code. The binary code is sent to the fault diagnosis to decode the fault type and its location. Then, the switching pattern is calculated to reconfigure the MLID to bypass and compensate the failed cell.

3.3 Diagnostic signals

The multilevel carrier-based sinusoidal PWM is used for controlling gate drive signals for the cascaded MLID as shown in Figure 3.2. It should be noted that other modulation strategies can be used to control a cascaded MLID as well; one unique method to balance a switching loss of other levels, particularly at low modulation index, has been proposed by Tolbert [44]. Figure 3.2 shows that the output voltages can be controlled by controlling the modulation index.

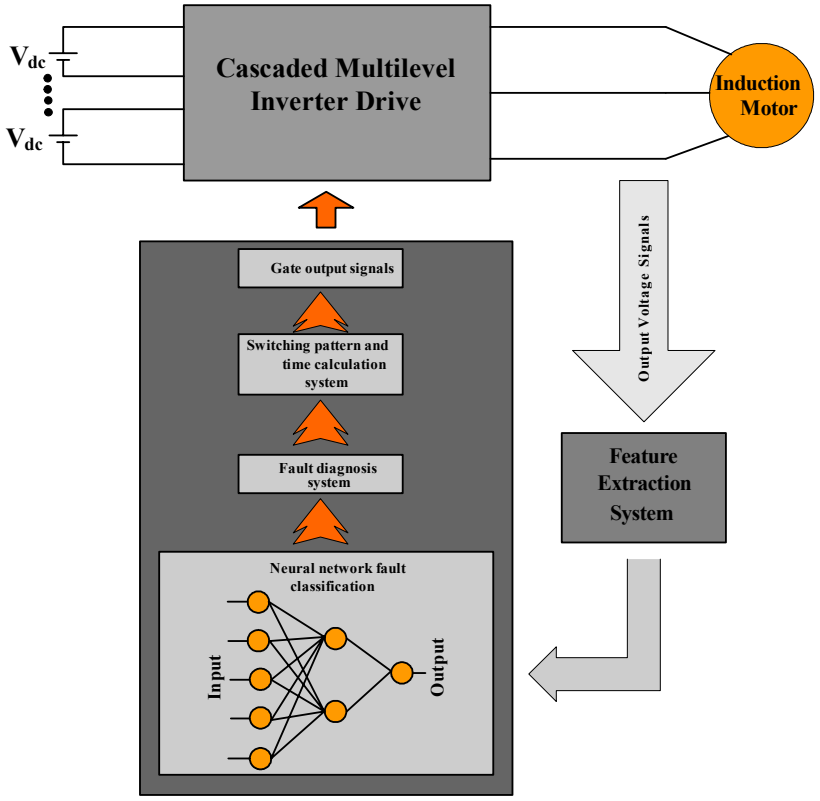


Figure 3.1. Structure of fault diagnosis system.

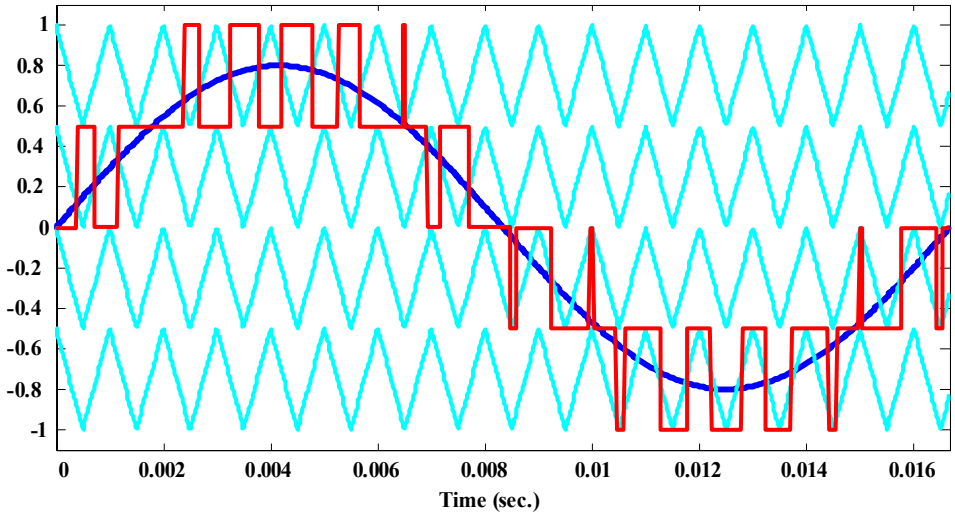


Figure 3.2. Multilevel carrier-based sinusoidal PWM showing carrier bands, modulation waveform, and inverter output waveform (m_a = 0.8/1.0).

The modulation index (m_a) is the ratio between an amplitude modulation waveform and an amplitude combination of carrier bands; for instance, the 0.8 out of 1.0 m_a is represented in Figure 3.2. The number of carrier bands depends upon the number of SDCS; the two SDCS cascaded MLID requires two carrier bands on positive side and two carrier bands on negative side and each band has equal amplitude.

The selection of diagnostic signals is very important because the neural network could learn from unrelated data to classify faults which would result in improper classification. Simulation results of input motor current waveforms during an open circuit fault at different locations of a MLID (shown in Figure 1.5) are illustrated in Figure 3.3 and Figure 3.4.

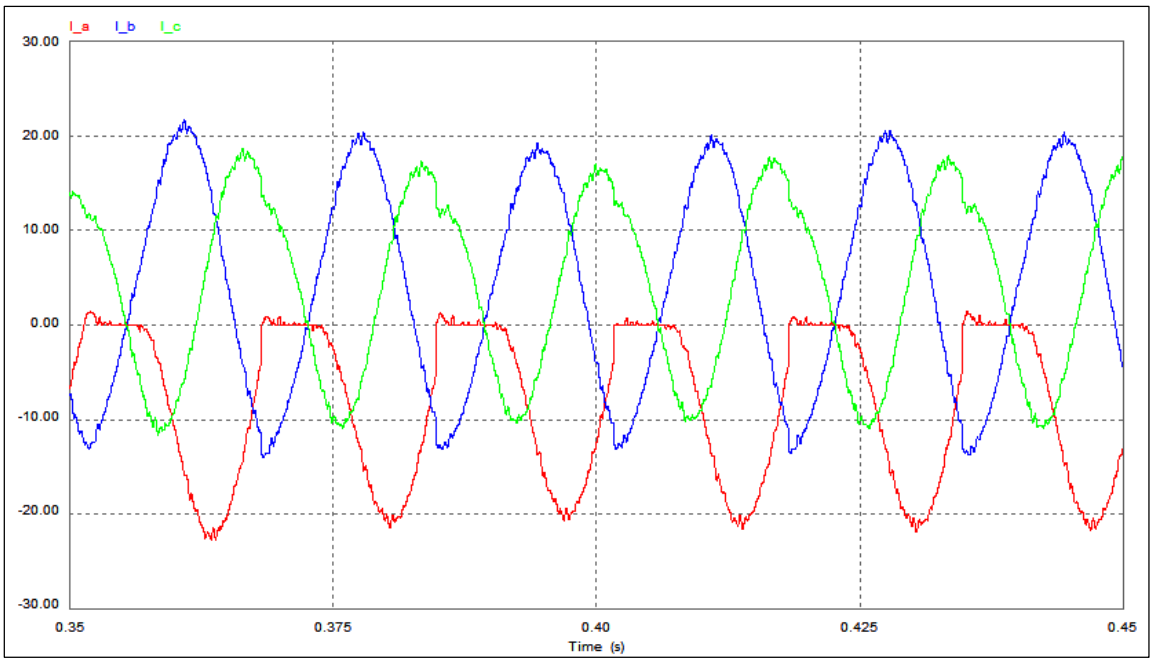


Figure 3.3. Input motor currents during open circuit fault at switch S_{A+} of H-bridge 2.

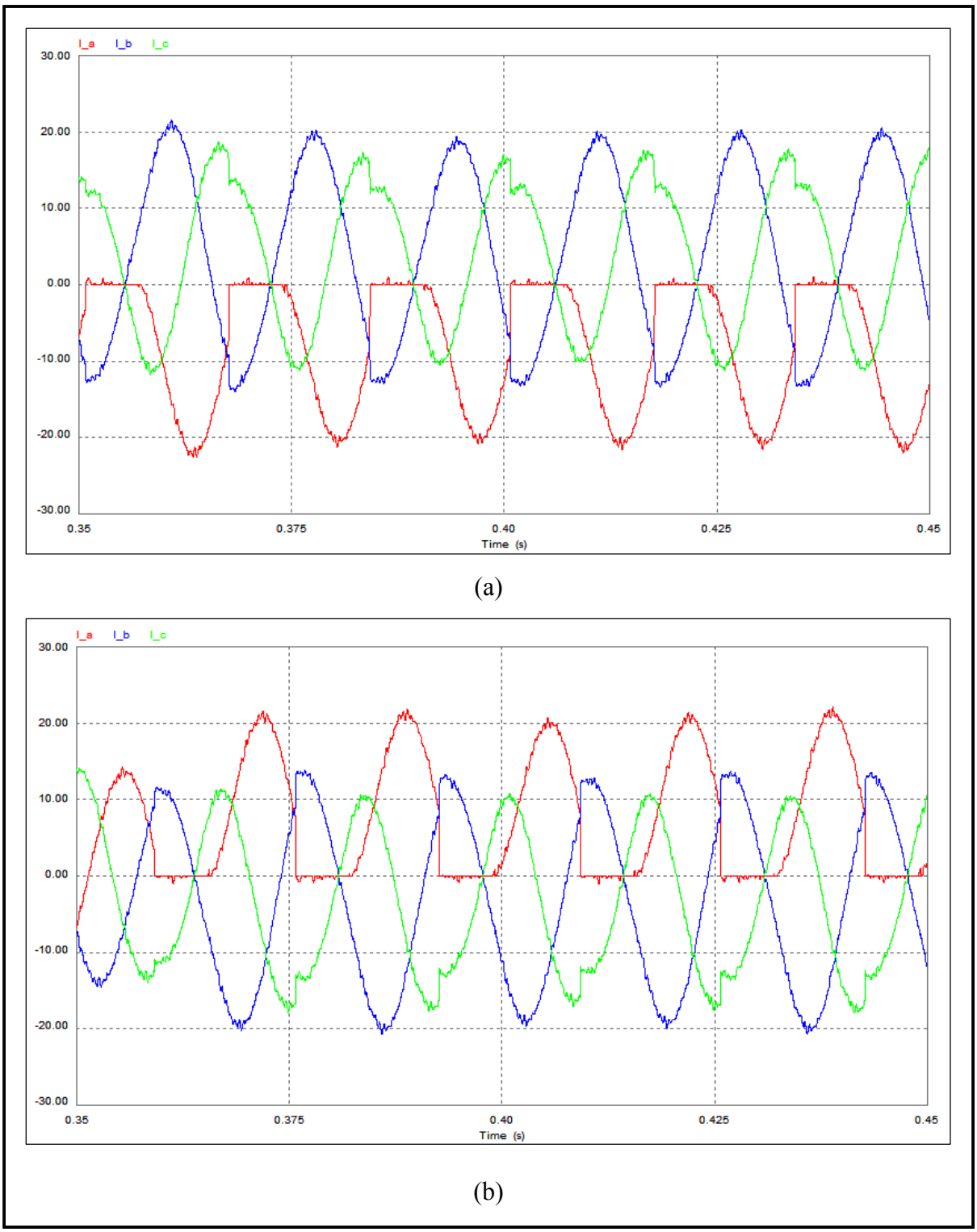


Figure 3.4. Input motor currents during open circuit fault at H-bridge 1: (a) switch S_{A+} , (b) switch S_{B+}.

The simulation model is illustrated in Figure 3.5; Power simulation (PSIM) from Powersim Inc is used as power circuit of a MLID and Matlab-Simulink from Matworks is used to generate gate drive signals. As can be seen in Figure 3.3 and 3.4, the input motor currents can classify open circuit faults at the same power cell by tracking current polarity (see Figure 3.4); however, it is difficult to classify the faults at different power cells; the current waveform for a fault of S_{A+} in H-bridge 2 (Figure 3.3) looks identical to that for a fault of S_{A+} in H-bridge 1 (Figure 3.4 (a)). As a result, the detection of fault locations could not be achieved with only using input motor current signals. Also, the current signal is load dependent; the load variation may lead to misclassification; for instance, light load operation as reported in a CID case in chapter 2. Auspiciously, Figure 3.2 indicates that an output phase PWM voltage is related to turn-on and turn-off time of associated switches; hence, a faulty switch can not generate a desired output voltage; The output voltage for a particular switch is zero if the switch has a short circuit fault, whereas the output voltage is about V_{dc} of SDCS if the switch has an open circuit fault. For this reason, the output phase voltage can convey valuable information to diagnose the faults and their locations.

The simulation results of output voltages are shown for an MLID with open circuit faults and short circuit faults in Figure 3.6. One can see that all fault features in both open circuit and short circuit cases could be visually distinguished. Also, experimental results of output voltage signals of open circuit faults in each location of two 12 V separate dc source (SDCS) MLID as shown in Figure 1.5 with multilevel carrier-based sinusoidal PWM gate drive signals are shown in Figure 3.7 and Figure 3.8.

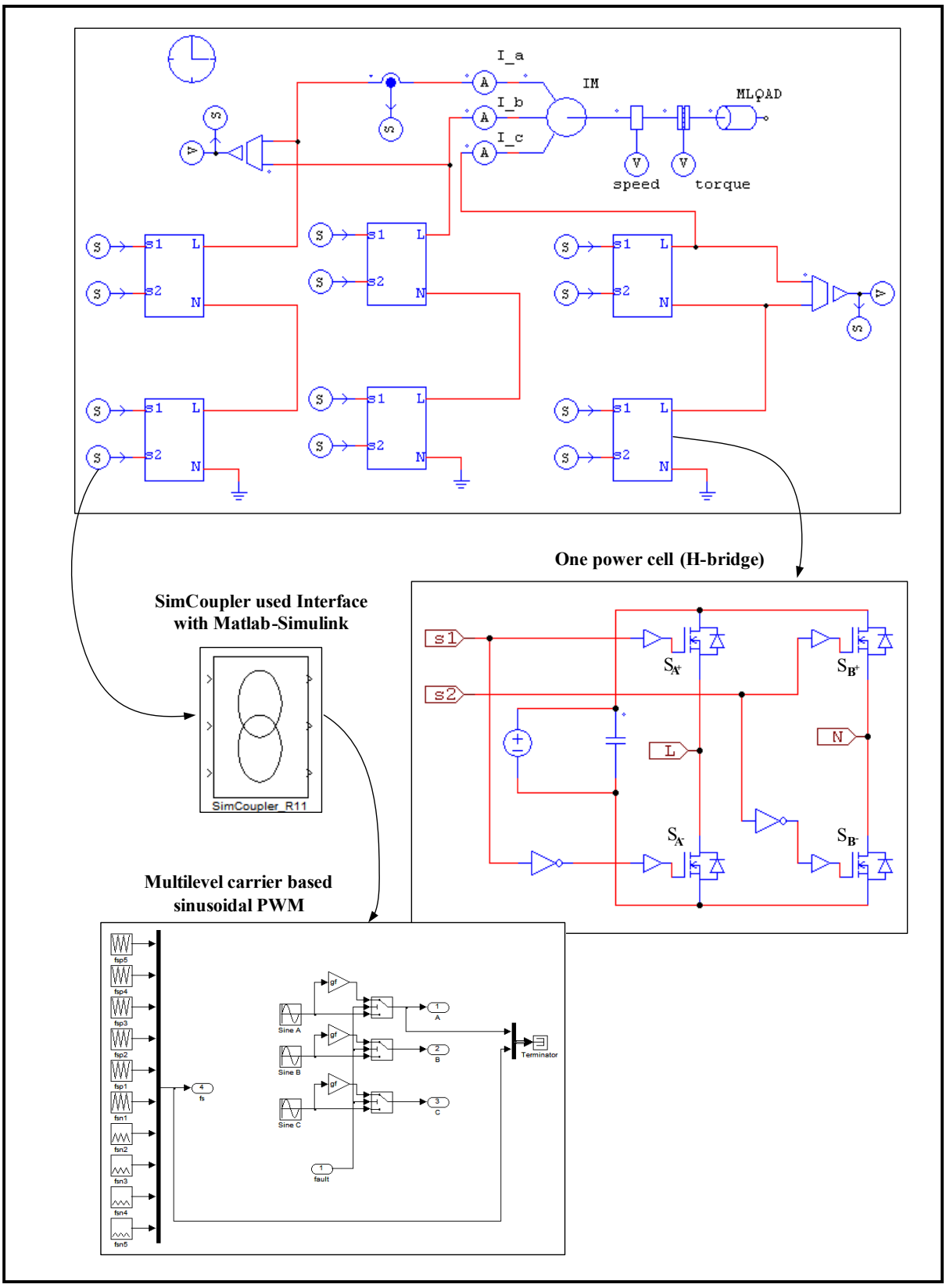


Figure 3.5. Simulation model using Psim and Matlab-Simulink.

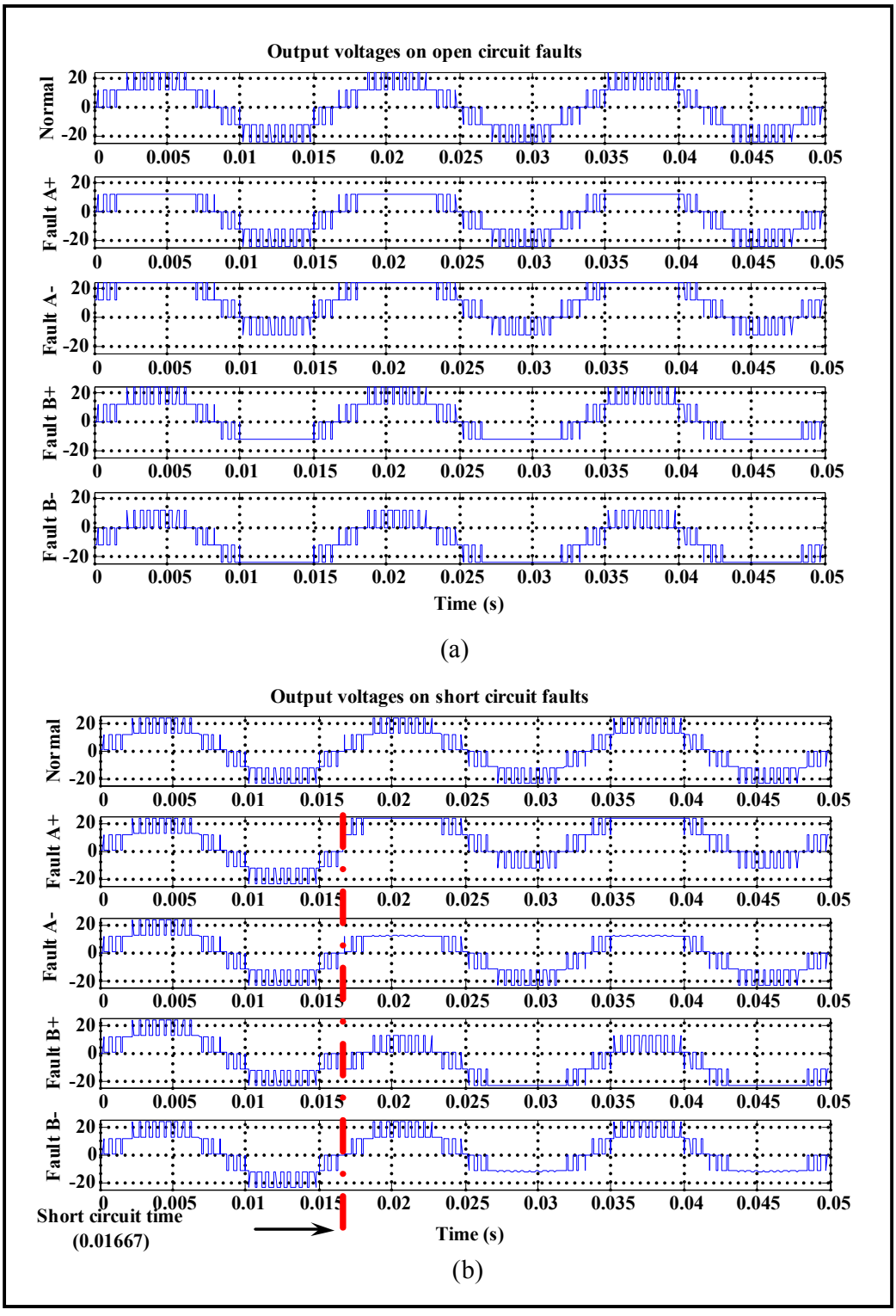


Figure 3.6. Simulation of output voltages signals showing fault features at S_{A+}, S_{A-}, S_{B+}, and S_{B-} of H-bridge 2 with modulation index = 0.8 out of 1.0.:
(a) open circuit faults, (b) short circuit faults.

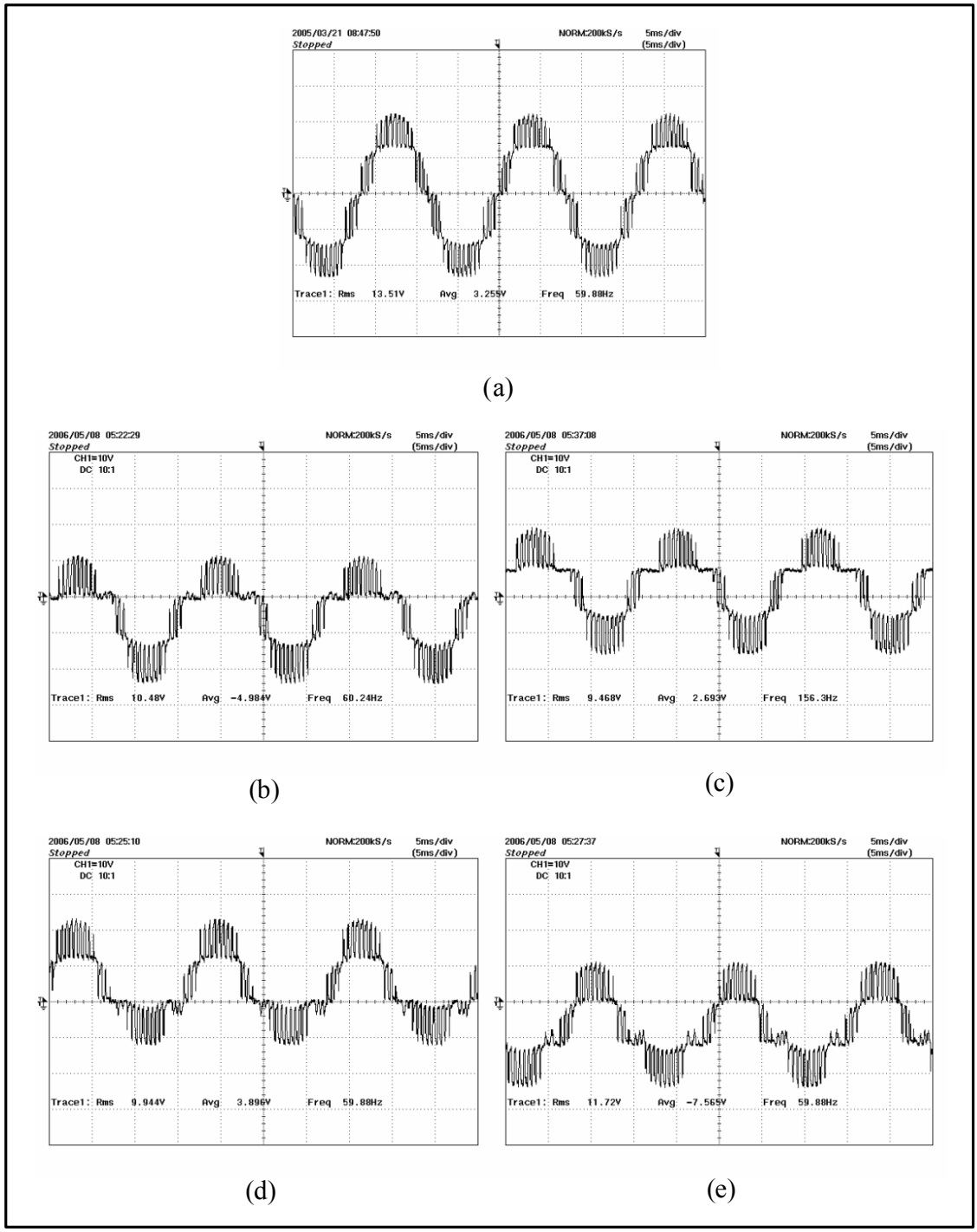


Figure 3.7. Experiment of open circuit fault of H-bridge 1 with modulation index = 0.8 out of 1.0: (a) normal, (b) S_{A+} fault, (c) S_{A-} fault, (d) S_{B+} fault, and (e) S_{B-} fault

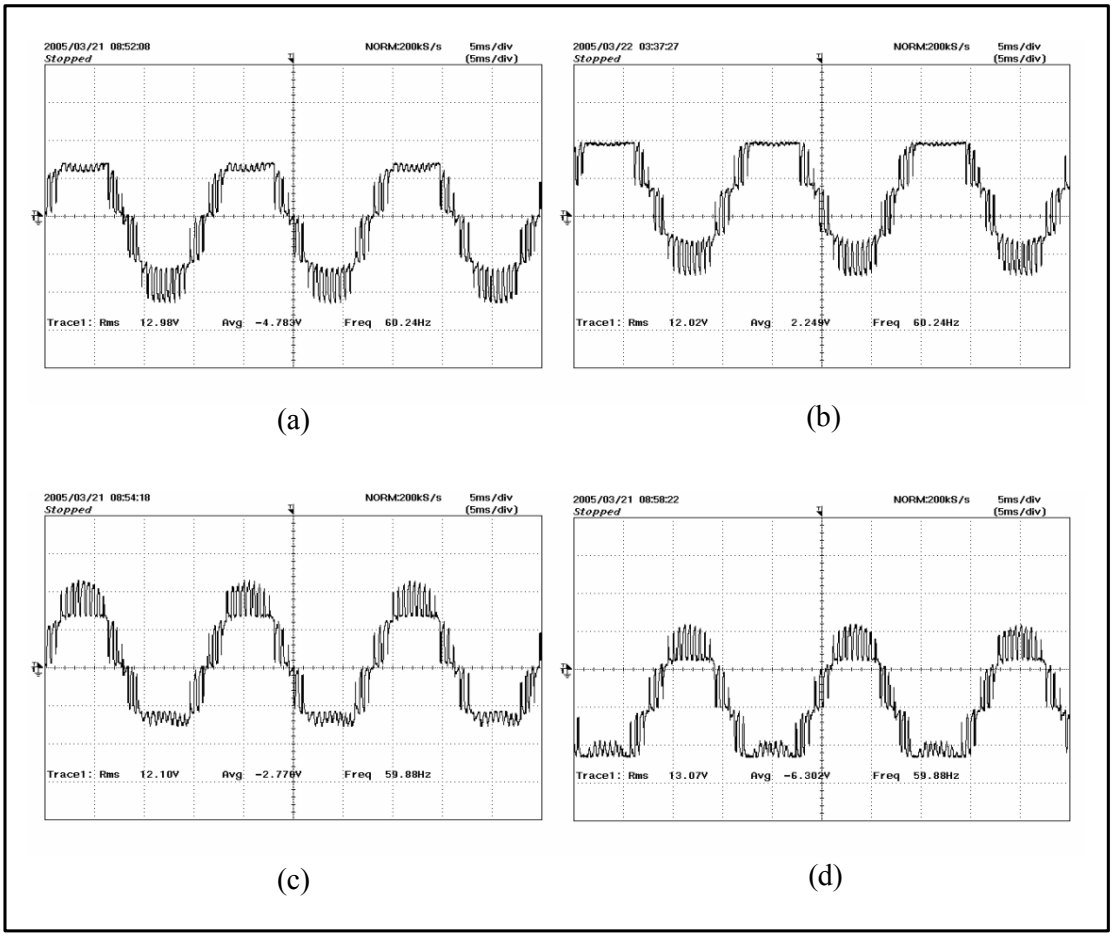


Figure 3.8. Experiment of open circuit fault of H-bridge 2 with modulation index = 0.8 out of 1.0: (a) S_{A+} fault, (b) S_{A-} fault, (c) S_{B+} fault, and (d) S_{B-} fault.

Obviously, the results show that the output phase voltage signals are related to the fault locations and fault types (open circuit and short circuit). One can see that all fault features can be visually distinguished in both fault types and fault locations via the output phase voltage signals; however, the computation unit cannot directly visualize as a human does.

A neural network is one suitable AI-based technique which can be applied to classify the fault features. Besides, a classification technique using a neural network offers an extra degree of freedom to solve a nonlinear problem; the failure of a single neuron will only partially degrade performance. If an input neuron fails, the network can still make a decision by using the remaining neurons.

In contrast, if only a single input, for instance the dc offset of signals, is used as the input data to classify the faults, the diagnosis system may not perform classification when the input data has drifted or the single sensor has failed. Furthermore, a neural network also permits parallel configuration and seasonal changes. Additional H-bridges and fault features (short circuit) can be conveniently extended into the system with more training data and parallel configuration. Therefore, the fault types and fault locations in a cascaded MLID will be attempted to diagnose from its output voltage waveform.

3.4 Feature extraction system

Simulated and experimental output voltages of a MLID are illustrated in Figures 3.6, 3.7, and 3.8. As can be seen, the signals are difficult to rate as an important characteristic for classifying a fault hypothesis, and they have high correlation with each other; hence, a signal transformation technique is required. An appropriate selection of the feature extractor is to provide the neural network with adequate yet significant details in the pattern set so that the highest degree of accuracy in the neural network performance can be obtained.

The comparison of signal transformation suitable to training a neural network for fault diagnosis tools is elucidated in [46], and one possible technique for hardware implementation with a digital signal processing microchip is fast Fourier transform (FFT).

An FFT is the development version of discrete Fourier transform (DFT). Beginning with the DFT in (3.1), and then the FFT using the decimation in time decomposition algorithm is illustrated in (3.2). Together, the computational savings of the FFT becomes N logarithmic time [O ($Nlog_2N$)] compared to quadratic time [O (N^2)] for the DFT. This means that if N is 16, the FFT will execute only 64 times, whereas the DFT will run 256 times. Therefore, the signal transformation using FFT is naturally faster than the DFT. Other popular signal transformation techniques such as Hartley and Wavelet are explained in [46].

$$F_k = \sum_{n=0}^{N-1} f_n W_N^{nk} \qquad for\ k = 0, \ldots, N-1 \ , \tag{3.1}$$

where $W_N = e^{-j\frac{2\pi}{N}}$,

N = the number of harmonic orders,

$$\begin{aligned} F_k &= G_k + W_N^k H_k \qquad for\ k = 0, \ldots, \frac{N}{2} - 1 \ , \\ F_{k+\frac{N}{2}} &= G_k - W_N^k H_k \qquad for\ k = 0, \ldots, \frac{N}{2} - 1 \ , \end{aligned} \tag{3.2}$$

G_k is for even-numbered elements of f_n, whereas H_k is for odd-numbered elements of f_n. G_k and H_k can be computed as shown in (3.3) and (3.4):

$$G_k = \sum_{n=0}^{\left(\frac{N}{2}\right)-1} f_{2n} W_{\frac{N}{2}}^{nk}, \tag{3.3}$$

$$H_k = \sum_{n=0}^{\left(\frac{N}{2}\right)-1} f_{2n+1} W_{\frac{N}{2}}^{nk} \ . \tag{3.4}$$

In this dissertation, the FFT is used to transform the output phase-voltage signals, and the transformed signals of both simulation and experiment are represented in Figure 3.9.

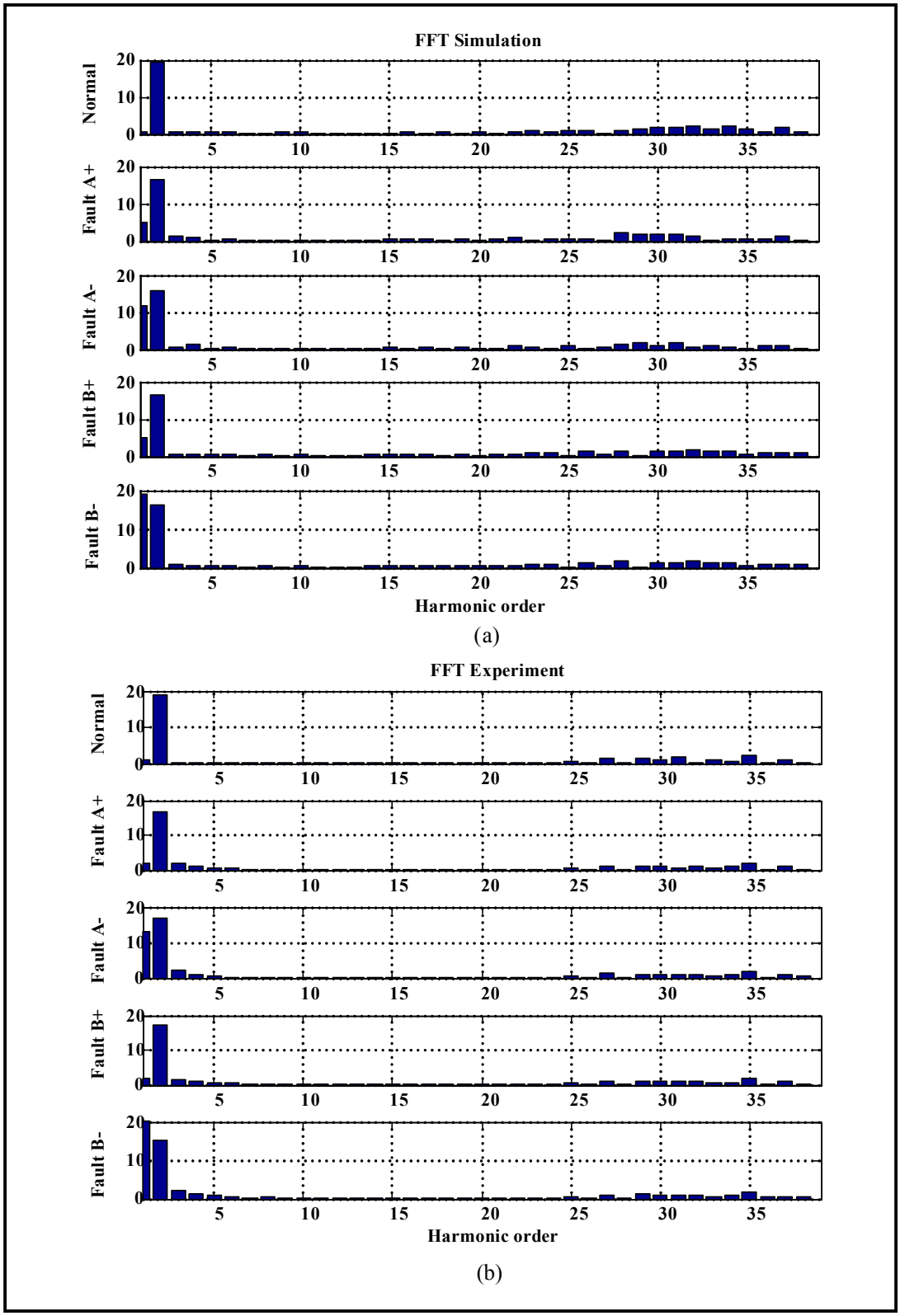


Figure 3.9.Signal transformation of output voltages on open circuit faults at H-bridge 2: (a) simulation (Figure 3.6 (a)) , (b) experiment (Figure 3.8) by using FFT with m_a = 0.8 out of 1.0.

Obviously, the results are nearly identical fault features. The FFT technique has a good identical feature to classify normal and abnormal features; as a result, FFT can be used to transform voltage output signals in order to rate signal value for important features so that the features for a fault hypothesis can be classified. It should be noted that PWM signals have relationship with carrier frequency (switching frequency) known as modulation frequency (m_f), so if one use harmonic order as variables to train the neural network, a range of harmonic order should cover from 0 to at least equal to the PWM switching frequency. In this case, the switching frequency is 2 kHz; accordingly, the harmonic order should be more than 34 orders. One can see that many neurons are required as inputs to train the neural network (i.e. one neuron for each harmonic order). Consequently, a huge input matrix will lead to a long time to train the neural network, and the high harmonic order may contain noise; this noise data can cause poor classification performance. Thus, one would prefer to reduce the dimension of the input matrix, but the question is which harmonic orders should be kept to train the network? One possible technique is a principal component analysis (PCA).

PCA is a method used to reduce the dimensionality of an input space without losing a significant amount of information (variability) [47]. The method also makes the transformed vectors orthogonal and uncorrelated. A lower dimensional input space will also usually reduce the time necessary to train a neural network, and the reduced noise (by keeping only valuable PCs) may improve the mapping performance. PCA is used to reduce the number of input neurons as illustrated in Figure 3.10.

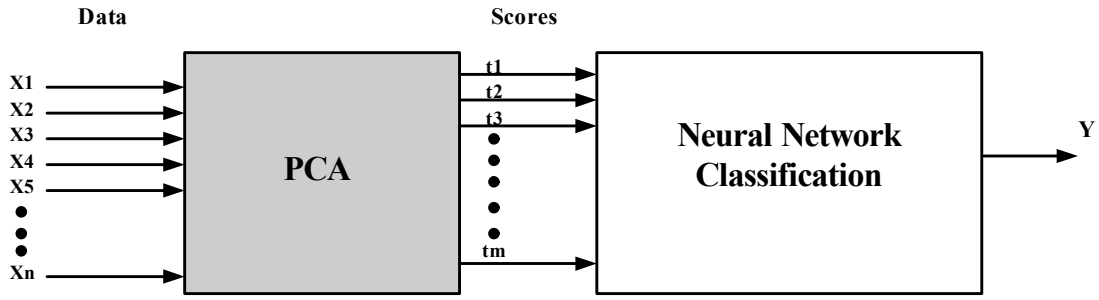


Figure 3.10. Principle Component Neural Network.

3.5 Principal component analysis

Basically, PCA is a statistical technique used to transform a set of correlated variables to a new lower dimensional set of variables which are uncorrelated or orthogonal with each other. A distinguished introduction and application of PCA has been provided by [48]. Also, PCA technique is possible to implement on floating point DSP for real-time applications as proposed in [49]. The discussion of PCA presented in this section will be brief, providing only indispensable equations to elucidate the fundamental PCA approach applied to a fault diagnosis system in MLID. The fundamental PCA used in a linear transformation is illustrated in (3.5). The original data matrix, $\boldsymbol{X}$ of n variables (harmonic orders) and m observations (different modulation indices of output voltage of MLID) is transformed to a new set of orthogonal principal components (PC), $\boldsymbol{T}$, of equivalent dimension ($m \times k$) as represented in (3.6). The transformation is performed such that the direction of first PC is identified to capture the maximum variation of the original data

set. The subsequent PCs are associated with the variance of original data set in order; for instance, second PC indicates the second highest variance of the original data set, and likewise.

$$T = X \bullet P, \tag{3.5}$$

where $\boldsymbol{T}$ is the $m \times k$ score matrix (transformed data): m = the number of observations, k = dimensionality of the PC space;

$\boldsymbol{X}$ is the $m \times n$ data matrix: m = the number of observations, n = dimensionality of original space;

$\boldsymbol{P}$ is the $n \times k$ loadings matrix (PC coordinates): n = dimensionality of original space, k = number of the PCs kept in the model.

$$\begin{bmatrix} t_{11} & t_{12} & \cdots & t_{1k} \\ t_{21} & t_{22} & \cdots & t_{2k} \\ \vdots & \vdots & \vdots & \vdots \\ t_{m1} & t_{m2} & \cdots & t_{mk} \end{bmatrix} = \begin{bmatrix} x_{11} & x_{12} & \cdots & x_{1n} \\ x_{21} & x_{22} & \cdots & x_{2n} \\ \vdots & \vdots & \vdots & \vdots \\ x_{m1} & x_{m2} & \cdots & x_{mn} \end{bmatrix} \bullet \begin{bmatrix} p_{11} & p_{12} & \cdots & p_{1k} \\ p_{21} & p_{22} & \cdots & p_{2k} \\ \vdots & \vdots & \vdots & \vdots \\ p_{n1} & p_{n2} & \cdots & p_{nk} \end{bmatrix} \tag{3.6}$$

$$(m \times k) \quad = \quad (m \times n) \quad \bullet \quad (n \times k)$$

$$\begin{bmatrix} t_1 & t_2 & \cdots & t_k \end{bmatrix} = \begin{bmatrix} x_1 & x_2 & \cdots & x_n \end{bmatrix} \bullet \begin{bmatrix} p_{11} & p_{12} & \cdots & p_{1k} \\ p_{21} & p_{22} & \cdots & p_{2k} \\ \vdots & \vdots & \vdots & \vdots \\ p_{n1} & p_{n2} & \cdots & p_{nk} \end{bmatrix} \tag{3.7}$$

$$(1 \times k) \quad = \quad (1 \times n) \quad \bullet \quad (n \times k)$$

Selecting a reduced subset (PCs kept in the model) of PC space results in a reduced dimension structure with respect to the important information available as shown in (3.7). The objective of PC selection is not only to reduce the dimension structure, but also to keep the valuable components. Normally, high variance components could contain related information, whereas small variance components that are not retained are expected to contain unrelated information; for instance, measurement noise. It should be noted that the high variance components may not contain the useful information for a classification problem.

3.5.1 Data analysis using PCA

The objective of this section is to illustrate how the input dimension matrix can be reduced; therefore, an example of data analysis using PCA is provided. The open circuit faults at H-bridge 2 at different switches are used. All possible open circuit faults at H-bridge 2 are simulated using a model as shown in Figure 3.5 at different operation points. The set of original input data at each MLID operation contains 5 classes: a normal data (normal condition) and four abnormal data (Fault A+, A-, B+, and B-). The MLID operation will be changed with desired load, so modulation index (m_a) must be changed. In this particular example, modulation indices are varied from 0.6 to 1 with 0.05 intervals. Thus, the original data contains 45 observers covering all possible operations.

The data from the FFT are transformed to principle component space by using MATLAB statistic toolbox function, *[PC, Latent, Explained]=PCACOV(XC)*; *PC* is the principal

component loading matrix, *Latent* is the eigenvalues of the covariance matrix of the original input data (*XC*), and *Explained* is the vector of variance in each PC. The relationship of principal components and their cumulative percentage variance explained are illustrated in Figure 3.11. As can be seen, the summation of the first 15 PCs contains about 90% of the data. However, the eigenvalues of the 14th, 15th and other PCs are less than 1; this means the PCs have less variance than the original data which might contain measurement noise or uncorrelated information. One can see from the plot in Figure 3.11 that the break is between 5 and 8 PCs; therefore, a study suggests that 5 or 8 PCs should be the optimum model.

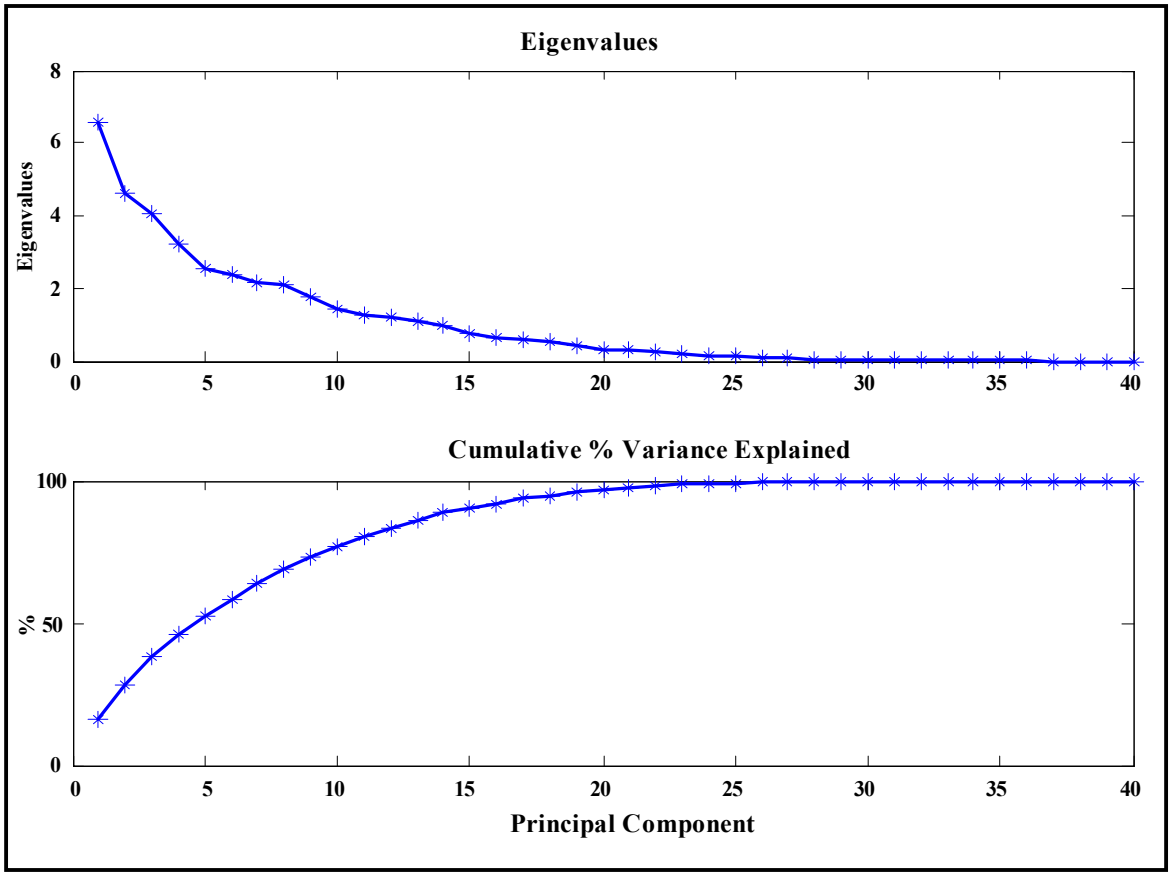


Figure 3.11. The plot of principal components versus eigenvalues.

The collected data from both simulation and experiment are analyzed to select valuable PCs for fault classification. The transformation matrix (Loading) for important PCs and the scores of samples of PCs are shown in Figure 3.12. The first 5 samples are normal condition, the next 5 samples are Fault A+, the next 5 samples are Fault A-, the next 5 samples are Fault B+, and the next 5 samples are Fault B-. The next 25 samples are unknown samples for testing the proposed neural networks. Clearly, the first PC can be used to distinguish between normal and fault conditions. One can see that the first 5 samples have positive scores, whereas the next 15 samples have mostly negative scores. As can also be seen, the first PCs are weighted negatively toward most of the samples. Also, the 4^{th} PC can be used to classify the different features between Fault A+ and A- and Fault B+ and B-. However, the 3^{rd} PC may not be useful because the 3^{rd} PC could not reveal any classification information as shown in Figure 3.12 (c), although it contains more information and variance (Eigenvalue) than the 4^{th}. Therefore, in this particular example, the combination of **1, 2, 4, 6** and **8** principal components are selected to perform the neural network classifications.

The 3-D plots of PC scores are shown in Figure 3.13. One can see that the classification between normal and faults could be a linear problem, whereas the classification among faults is a nonlinear problem. That is why the neural network is applied to solve this problem. By using PCA, the size of input neurons can be reduced from 40 nodes to 5 nodes (i.e. 5 harmonics instead of 40 harmonic components).

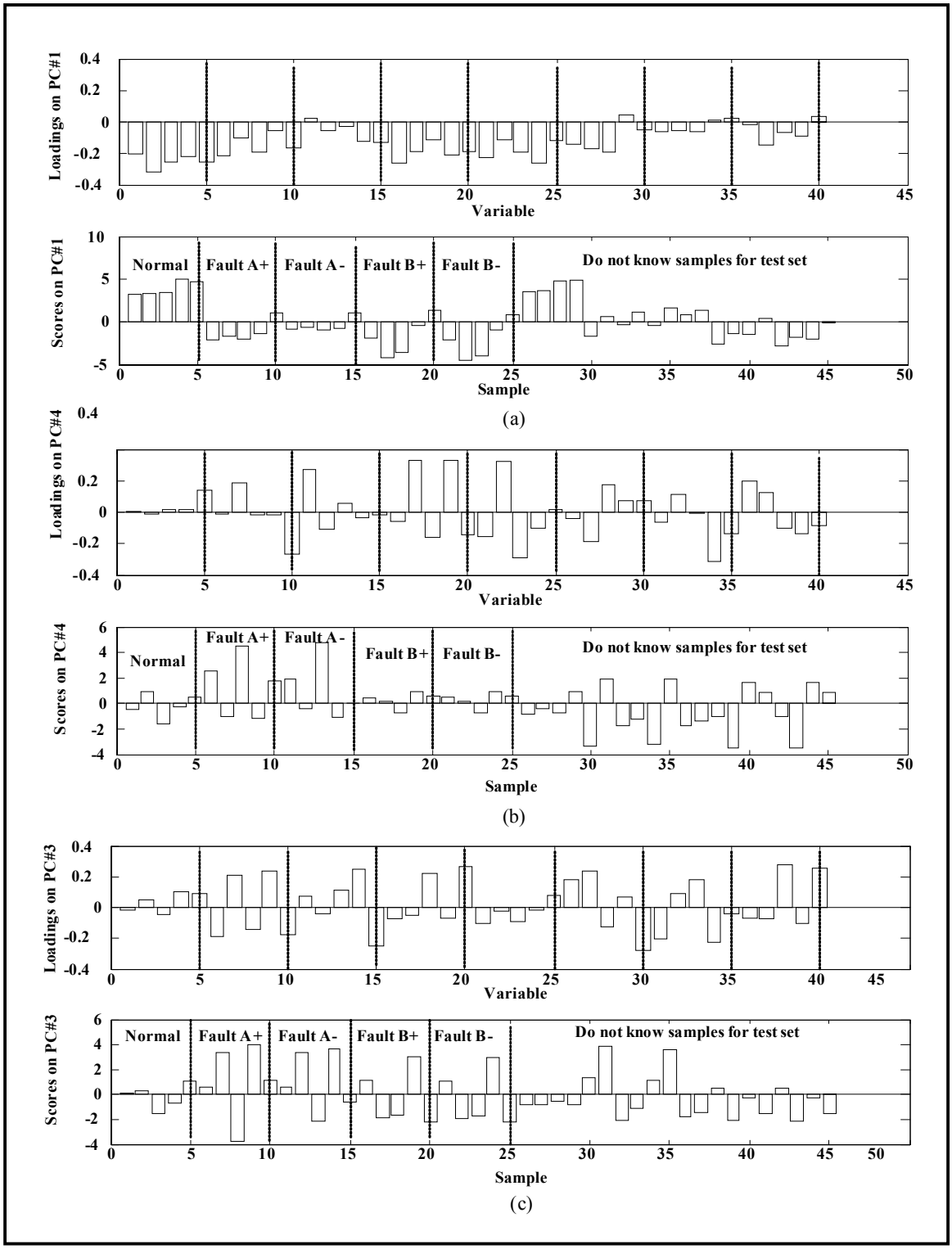


Figure 3.12. The selected plot of principal components score and loading: (a) first PC, (b) fourth PC, and (c) third PC.

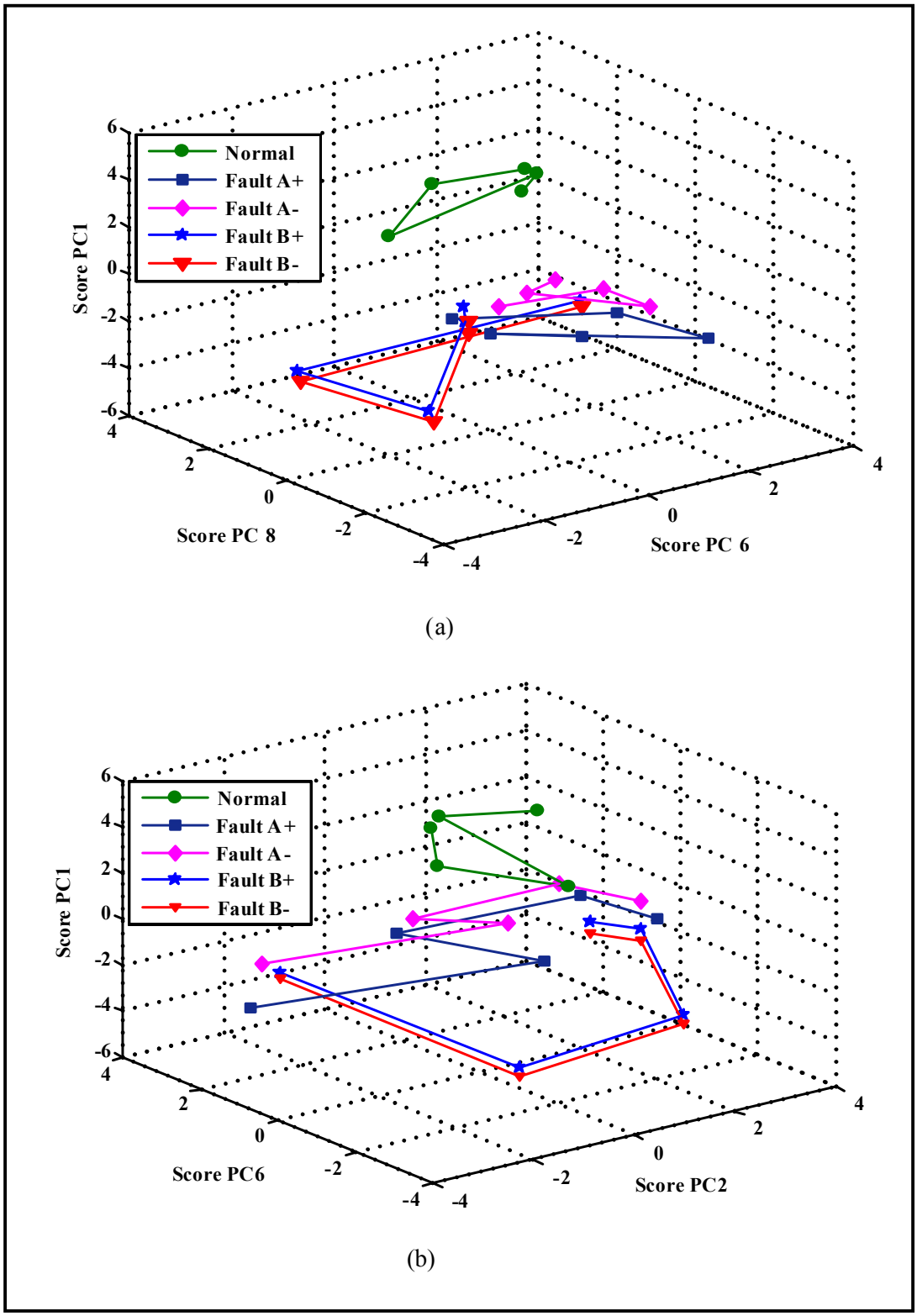


Figure 3.13. The 3-D plots of PC scores: (a) score on PC 6, 8, 1, (b) score on PC 2, 6, 1.

3.5.2 Principal component selection

The selection of principal component (PC) is very significant because input selected PCs can cause uncertainty results; additionally, unneeded input PCs to the neural network can increase the solution variance; also, absent necessary input PCs can increase bias. Usually, there are three methods to select a valuable PC: observed eigenvalue method, correlated method, and trial and error method. First, the observed eigenvalues method will choose PCs that contain most of the information (variability of original data set). This method is good for function approximation problems; however, it may not be useful for classification problems. Second, the correlated method will select PCs that are well correlated with the response variable. The correlated method is superior in both function approximation and classification problems; nevertheless, the method may not be an optimized solution and may consume a lot of time. Third, the trial and error method will pick the combination of PCs that provides minimum error; for instance, the misclassification error of the neural network. The trial and error method can offer a minimum error of the neural network, but the method requires a lot of time to search for the optimum combination of PCs for the model. One possible tool to search for the optimized combination of PCs is a genetic algorithm.

3.5.3 Genetic algorithm

Genetic algorithm (GA) is an optimization and search approach based on genetics and natural selection [50]. GA is not a function approximation technique; however, it has simple and powerful general purpose stochastic optimization methods [51]. GA permits a

population created from multiple individuals to evolve under specific fitness function which can be maximization or minimization problems. The advantage of using GA is that GA utilizes hypothetical operators instead of assigned rules to search for a solution. In addition, a GA contemplates multiple points in the search space at the same time, not a single point; therefore, it reduces an option to converge in local minima. Thus, with GA, the global minima of the problem statement could be found with high possibility. GA can possibly search multiple points in parallel because the evaluation of each point requires an independent computation. The data processed by the algorithm is a population (set) of chromosomes (bit strings), which represent multiple points in the search space. Because of GAs robustness, speed, efficiency and flexibility, GAs have been applied in various engineering and business problems [12]. Basically, GAs have three fundamental processes: selection, crossover and mutation. Selection process is a method to select the individuals called parents, which contribute to the population at the next generation. Crossover is a process which combines two parents to create children for the next generation. Mutation process is a method to apply random changes to individual parents to form children.

Recently, Matlab provides the genetic algorithm and direct search toolbox for Matlab users [52]. This toolbox offers a graphical user interface which enables to use a GA without working at the command line, called *gatool*. The use of *gatool* requires fitness function, number of variables, and GA options as clearly explained in [52]. One can see that GAs would become a popular optimization technique. In this research, *gatool* is utilized to perform GA processes which will be explained in the following section.

3.5.4 PC selection by genetic algorithm

From section 3.5.1, the 1,2,4,6 and 8 PCs are selected by correlated method (The PCs are correlated with respond variables). In this section, the GA is used to perform the PCs selection as illustrated in Figure 3.14. The result of PC selection by GA will be compared with the result from the correlated method. One can see from the flow chart in Figure 3.14 that the discrete GA (DGA) or binary GA can be applied to selecting PC. The idea is to randomly pass the PCs into the neural network and then a GA is utilized to search for the best combination of input PCs. The steps of GA process can be explained as follows:

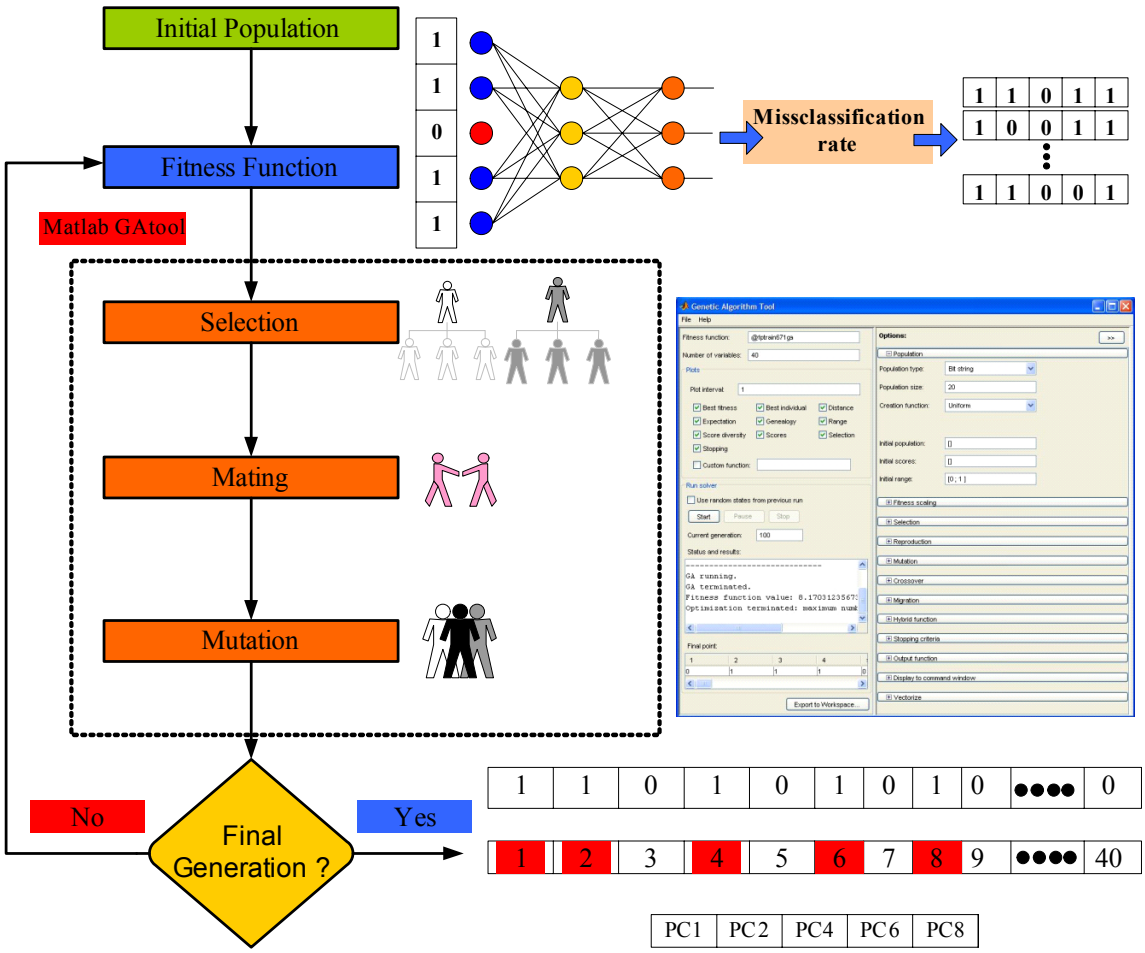


Figure 3.14. The flowchart of applied GA technique for PC selection.

- *Encoded input PCs:* the PCs to be optimized are represented by chromosomes in which each PC is encoded as a binary string known as a gene. Therefore, a chromosome consists of multiple genes as PCs to be selected. A population, consisting of a provided number of chromosomes is initially generated by haphazardly assigning "1" and "0" to all genes except for one chromosome which assigns to use all PCs. The binary string of the chromosomes has the same size as PCs to select from, whereby the presence of a PC is coded as "1", whereas the nonappearance of a PC is coded as "0". Accordingly, the binary string of a gene consists of only one single bit. The example of encoded input PCs is illustrated in Figure 3.14 on the right hand side. One can see that the bit "0" will be not used to train the network, whereas others will be used to train the network.

- *Fitness function*: The best chromosomes have the highest probability to survive as evaluated by the fitness function. An important point in applying GA is the design of the fitness function. A fitness function determines what a GA should optimize. In this research, the goal is to find the combination of selective PCs for fault classification which provides the minimum classification error. In this case, the classification is based on neural networks for modeling the relationship between input variables (PCs scores) and the responses (fault classes). Therefore, the evaluation of the fitness function begins with the encoding of the chromosomes into neural networks. Then, the networks are trained with a training set; and after that, the test set is examined. It should be noted that the test set in this research consists of simulation test set and experiment test set. Finally, the fitness function is evaluated by using (3.8) and (3.9). The fitness function is divided into two parts: sum of square error (SSE) of simulation set and

SSE of experiment test set. In this research, the experiment test set is weighted higher than the simulation test set as shown:

$$f = 0.2\,SSE_{Sim,set} + 0.8\,SSE_{Exp,set}\,, \tag{3.8}$$

$$SSE = \sum_{i=1}^{n} \left(y - \bar{y}_i\right)^2\,, \tag{3.9}$$

where y is the output target binary codes,

$\bar{y}_i$ is output of training data,

n is the number of training data.

- *GA parameter selection*: As previously mentioned, the *gatool* is used to set the GA options as shown in Figure 3.14 on the right hand side. The GA parameters can be conveniently selected by *gatool* [52]. It should be noted that different GA parameters could give the different results. For this particular example, the number of variables is 40, the population size is 20, and the fitness scaling is by rank.

After evolving the fitness function of the population as shown in Figure 3.14, the individuals are selected by using a roulette wheel; this can be directly set in *gatool* as "Roulette" in "selection" toolbar. Thereby, the chromosomes are allocated space on a roulette wheel proportional to their fitness value, and thus the more fit individuals are more likely selected. The next step is the mating process; a single point crossover technique is utilized. A crossover process will create offspring chromosomes which

randomly selects a crossover point within the chromosome. Then, two parent chromosomes are interchanged at this point to generate two new offspring. After that, the chromosomes are mutated with a probability of 0.05 (mutation rate) per gene by erratically changing genes from 0 to 1 and vice versa. The mutation prevents the GA from converging too quickly in a small area of search space [53]. Again, it should be noted that different GA parameters may give different results. Therefore, the GA parameter selection might need some experiences in a particular application.

- *Stopping Criteria***:** The evaluation and reproduction steps are repeated until a certain number of generations, a defined fitness or a convergence criterion of the population are reached. In this research, the maximum number of generations is 100. Ideally, all chromosomes of the last generation should have the same genes corresponding to the optimal solution.

3.5.5 Data analysis using GA and PCA

By using the same original data set represented in section 3.5.1, the best result from *gatool* after several attempts is shown in Table 3.1. The final point shows that the 8 PCs are selected by GA consisting of **1,2,3,5,7,8,13** and **14** with a minimum SSE 0.205. The PCs selected by correlated method (Section 3.5.1) are **1,2,4,6** and **8**. This GA result is interesting because one know that both 13 and 14 PCs contain small variance of the information as shown in Figure 3.11; however, one can see from the plot of the score on PC14 in Figure 3.15 that PC 14 can be used to categorize between Fault A+ and A-; also

PC 14 can be used to classify between Fault A+, Fault A- and Fault B+ and Fault B-. Meanwhile, the loading plot on PC 13 that the sampling from 16 to 20 has mostly positive eigenvalue, whereas the sampling from 21 to 25 has mostly negative eigenvalue. This shows that PC 13 can be utilized to classify between Fault B+ and Fault B-.

The 3-D plots of combination of PCs are illustrated in Figure 3.16. One can see that the combination of 5, 13, and 14 provides a bigger gap among faults A+, A-, B+, B- than the combination of 1, 2 and 6 PCs as represented in Figure 3.13(b). This result suggests that the neural network could perform a better classification performance with additional PC 13 and PC 14.

Table 3.1. The output final solution from GA using *gatool*.

Description	**Outputs from *gatool***
Final point	*1 2 3 4 5 6 7 8 9 10 11 12 13 14* **1 1 1 0 1 0 1 1 0 0 0 0 1 1** ***PC 15-40 are all 0*** **0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
Fval	**0.205**

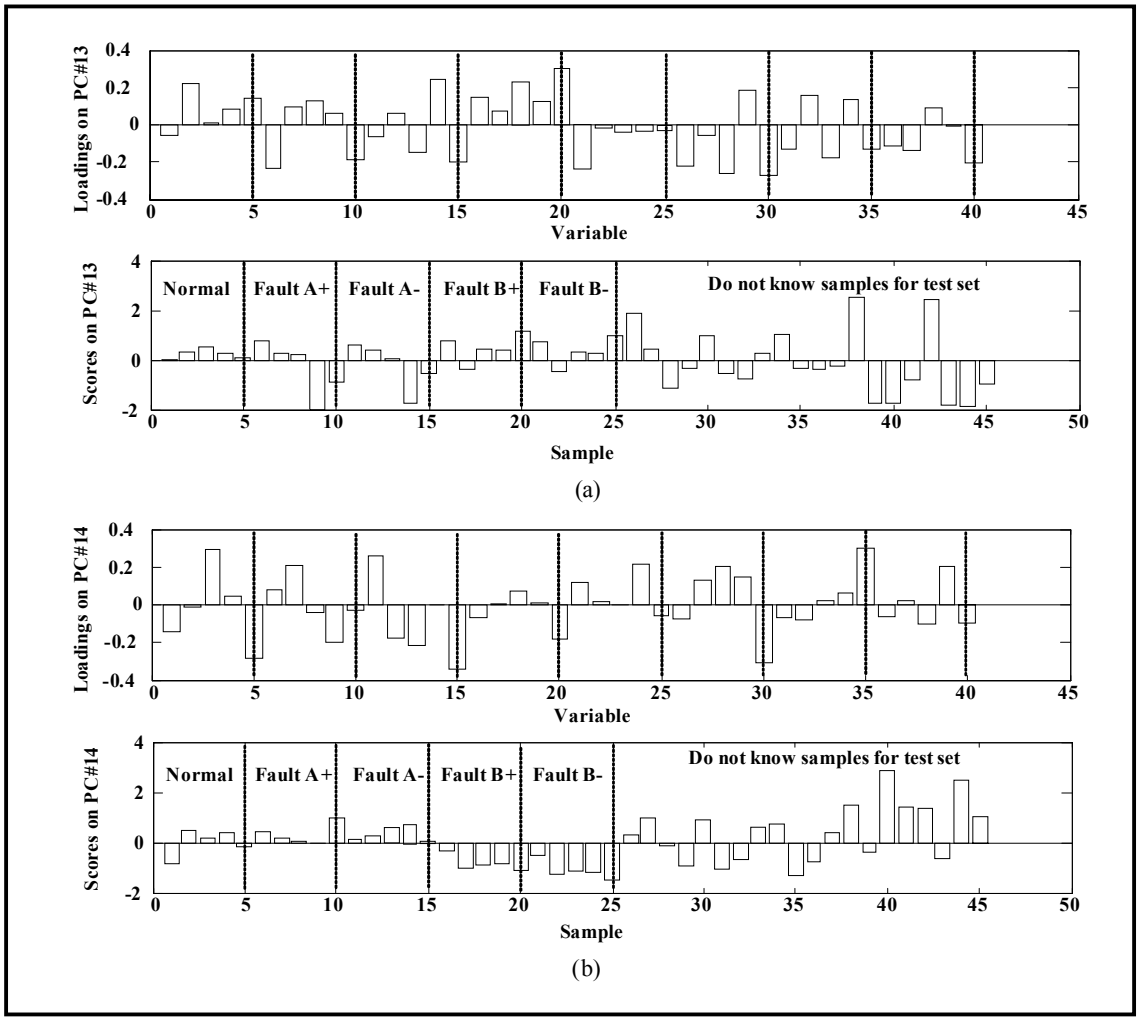


Figure 3.15. The plot of principal component loading and score of 13 and 14 PC.

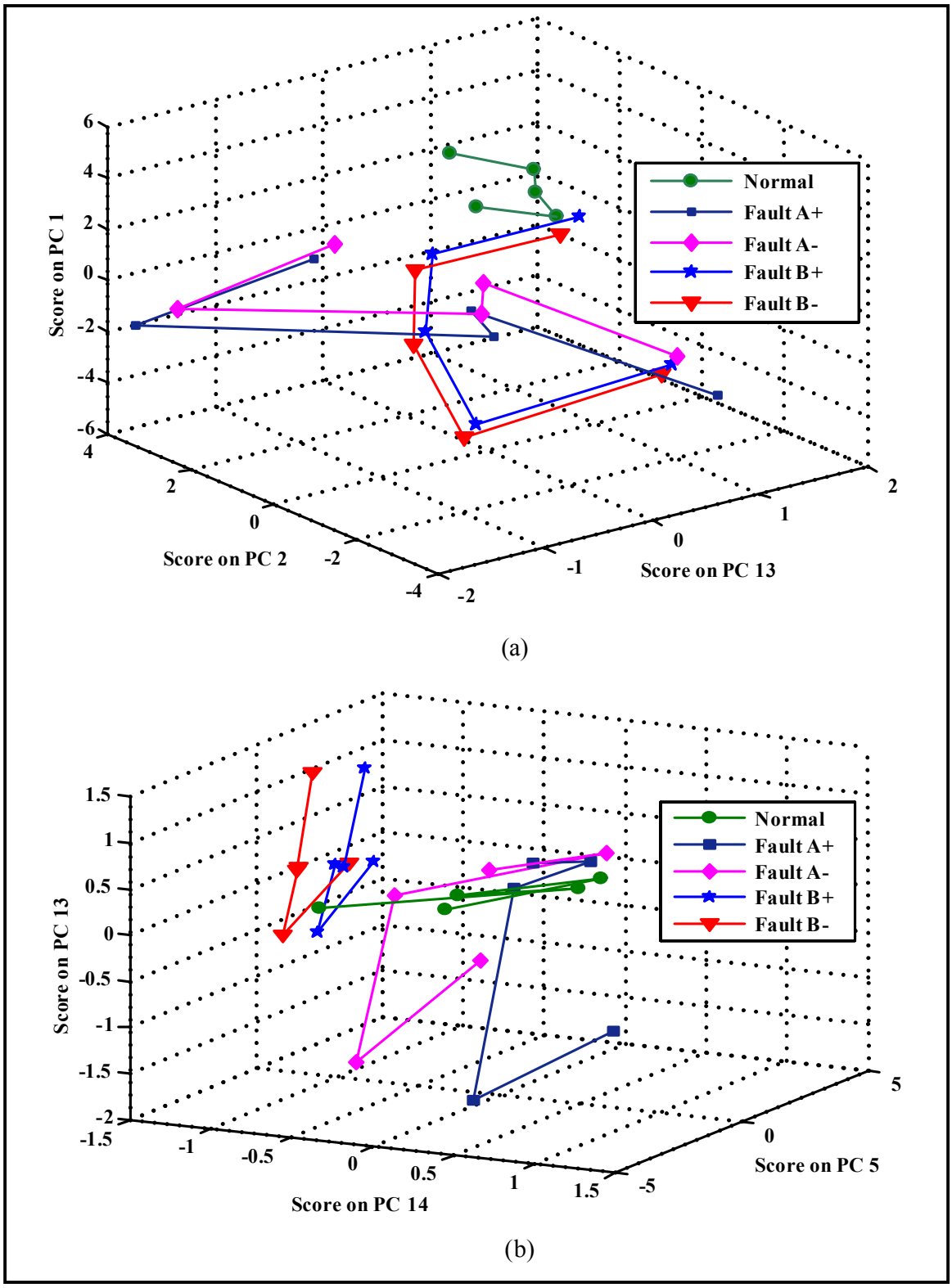


Figure 3.16. The 3-D plot of the combination PCs from GA results.

3.6 Neural network classification

All fault features, as previously discussed, can be classified based upon their effects upon the output phase-voltages. The transformation of output voltage signals is achieved by using FFT, PCA, and GA as illustrated in section 3.5.1 and 3.5.5. As mentioned before, the systematic mathematical technique may be complicated to implement in a practical real time control system; therefore, a feedforward neural network technique permitting input/output mapping with a nonlinear relationship between nodes will be utilized [54]. Neural networks provide the ability to recognize anomalous situations because of their intrinsic capacity to classify and generalize. Especially, the sensitivity and response time of the original procedure presented for the on-line analysis of fault set repetition enable on-line fault location techniques to be developed [55]. The stages of neural network fault classification are explained in the following sections.

3.6.1 Neural network architecture design

The fundamental architecture of the multilayer feedforward network or MLP is illustrated in Figure 3.17. The MLP is used in this research because the input data contain continuous features. The number of hidden layer and number of neurons depend upon the complexity of the problems; the more complicated problems may require more neurons or hidden layers. However, too many neurons could lead to overfitting problems (neural network learns noisy data). The proposed fault diagnostic neural network architecture utilizes one hidden layer network with multiple hidden neurons as shown in Figure 3.18.

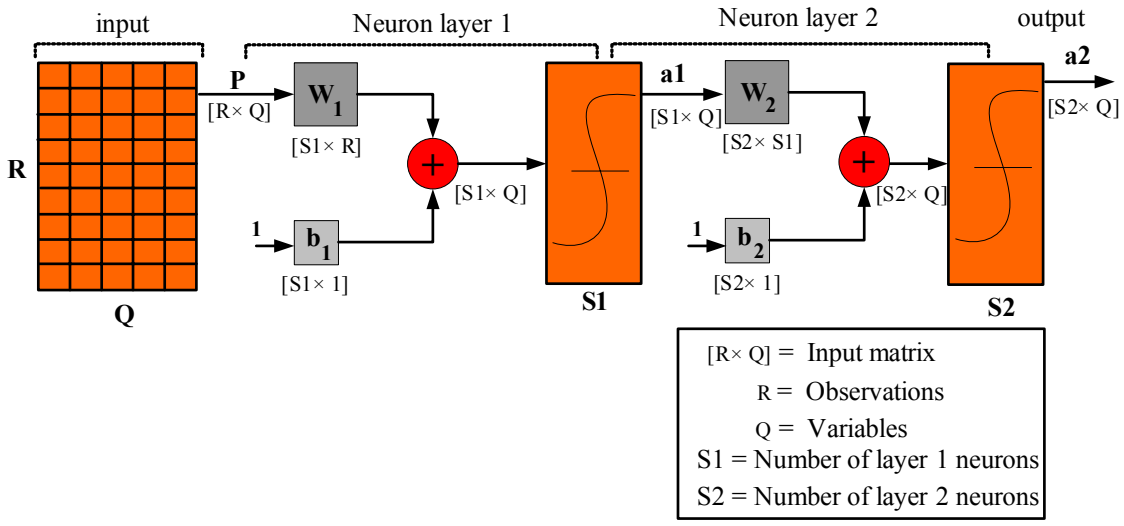
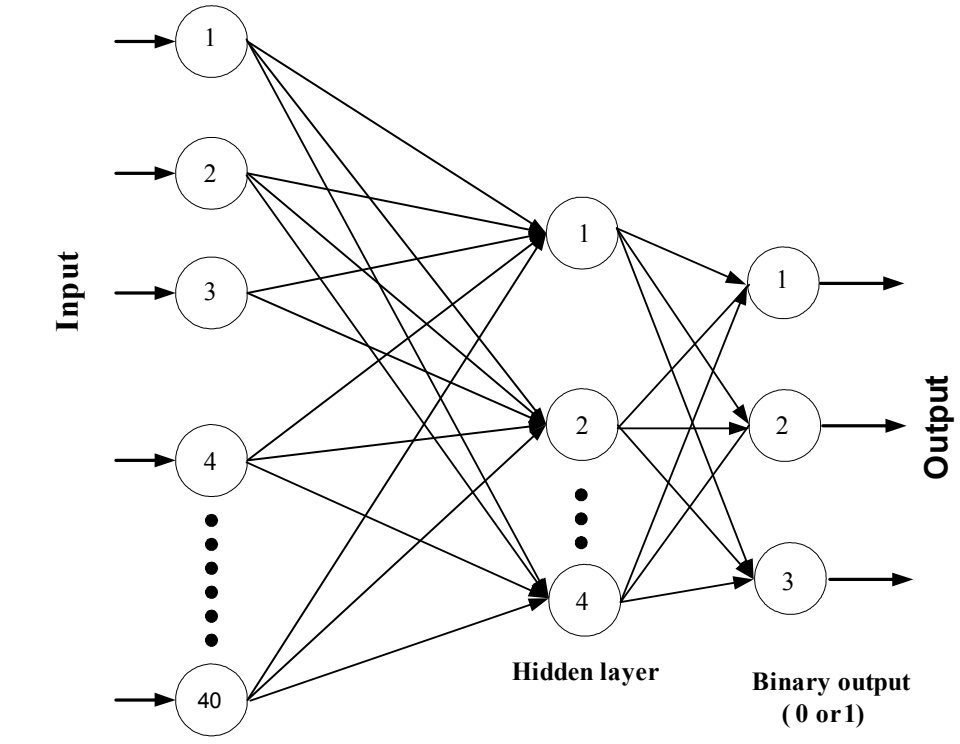


Figure 3.17. Multilayer feedforward network architecture.



Input variables are harmonic orders or selected PC
(one neuron is one harmonic order)

Figure 3.18. Proposed neural network architecture.

As a comparison among transformation methods, FFT, PCA and GA-PCA will be performed, and three different neural network (NN) architectures are used. The first NN architecture has one hidden layer with 40 input nodes, 4 hidden nodes, and 3 output nodes. The original data from the feature extraction system (FFT) is used in this network.

The second NN architecture has one hidden layer with 5 input nodes, 3 hidden nodes, and 3 output nodes. The PCA is applied in this network to reduce the number of input neurons as discussed in section 3.5.1. The combination of ***1, 2, 4, 6 and 8 principal components*** will be used to perform the neural network classifications.

The third NN architecture is based on GA selection as discussed in section 3.5.5 because the input neurons depend on how many PCs selected by GA. However, the one hidden layer with 3 hidden nodes and 3 output nodes are used since the comparison among proposed NN will be performed so that the NNs should have the same complexity and degree of freedom. The first network requires more neurons because the network has more input neurons.

The sigmoid activation function is used: *tansig* for hidden nodes and *logsig* for an output node. A *logsig* activation function is used for an output node because the target output is between 0 and 1. It should be noted that the number of nodes for the input and output layers depends on the specific application. The selection of number and dimension in the hidden layer is based on neural network accuracy in preliminary tests. Indeed,

optimization of the network architecture is a significant topic in a study of artificial intelligence aspects [54].

3.6.2 Input/output data

The set of original input data at each MLID operation contains 5 classes: a normal data (normal condition) and four abnormal data (Fault A+, A-, B+, and B-). The MLID operation will be changed with desired load, so modulation index must be changed. In this research, modulation indices are varied from 0.6 to 1 with 0.05 intervals. Therefore, the original data contains 45 observers covering all possible operations. The output target nodes are coded with a binary code as shown in the Table 3.2. The *round ( )* function is used to make the binary code outputs for the test sets.

3.6.3 Training paradigm

The Levenberg Marquardt training paradigm, *trainlm* [42] is utilized for all NNs in this research because *trainlm* not only performs very fast training time but also has inherent regularization properties [54]. Regularization is a technique which adds constraints so that the results are more consistent. The 1% misclassification and 1% input data error rate are chosen to calculate a sum of square error goal, SSE; therefore, a SSE < 0.025 goal is used to train the network by calculating from (3.9). The training process will be finished when the SSE goal is met. However, in the GA implementation case the training process will be finished either when SSE goal is met or when the maximum epoch is reached as shown in Figure 3.19. The maximum epoch for each iteration step of GA is 50.

Table 3.2. Target and classification data.

Classification	Target neurons [Y1 Y2 Y3]
Normal	[1 1 1]
Fault at S_{A+}	[0 0 1]
Fault at S_{A-}	[0 1 0]
Fault at S_{B+}	[1 0 1]
Fault at S_{B-}	[1 1 0]

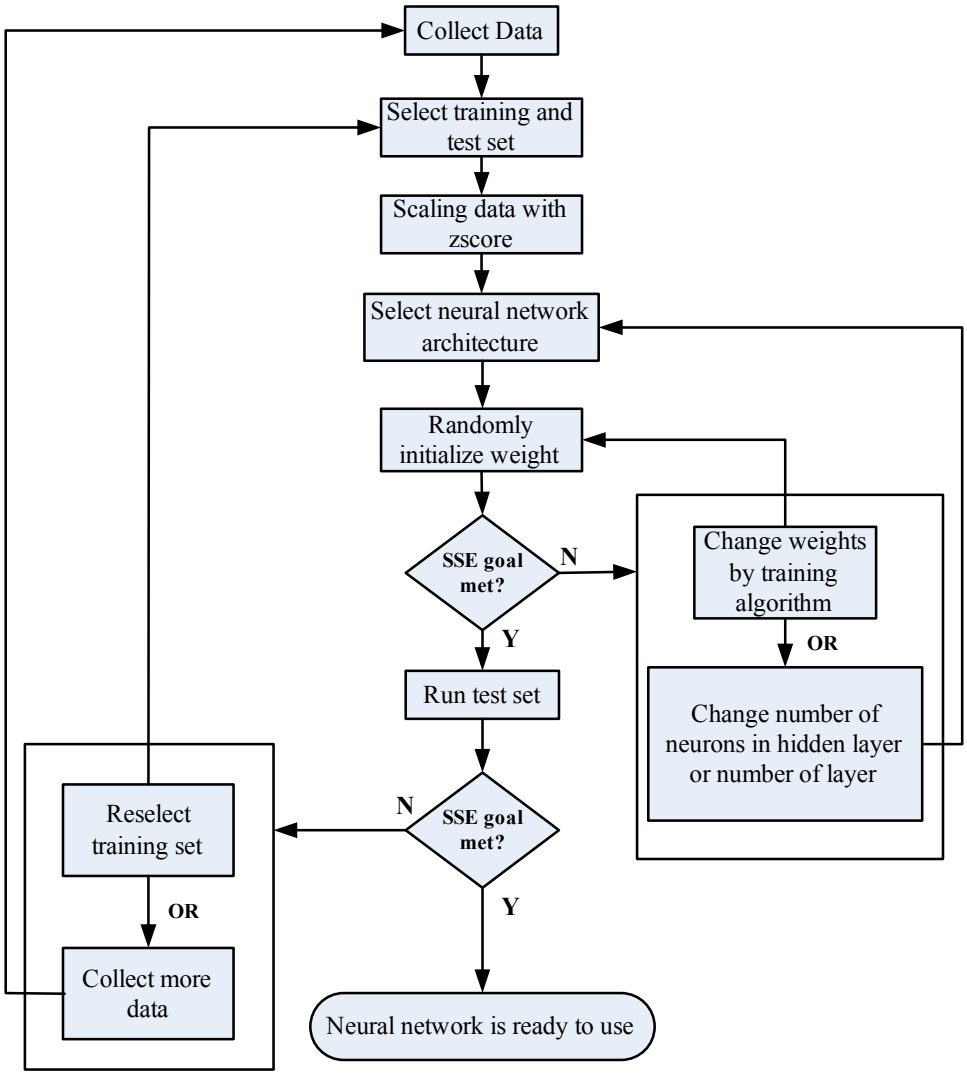


Figure 3. 19. A flowchart for multilayer feedforward training paradigm.

3.6.4 Training and testing data set selection

The training data set should also cover the operating region, thus the training set is generated from simulation with various operation points (different modulation indices such as 0.6, 0.7, 0.8, 0.9 and 1). The testing sets have two different sources; first, the test set is generated from simulation with modulation indices, 0.65, 0.75, 0.85, and 0.95. as shown in Figure 3.6 (a). Second, the test set is measured from experiment at different modulation indices of 0.7, 0.8, 0.9, and 1 as shown in Figure 3.8. Training and testing sets have 200 kHz sampling frequency. Both data sets are transformed by FFT from 0 to 39 harmonic orders as shown in Figure 3.9. Zero harmonic order means the dc component of the signals. Again, it should be noted that each modulation index has 5 classes: normal, Fault A+, A-, B+, and B-. The test sets are used to examine the neural network classification performance.

The input training data are scaled by using the mean center and unit variance method (Z-score scaling). The scaling data will avoid premature saturation of sigmoidal units and also allow the use of a specific output neuron [54]. The scaling parameters; the mean value (X_M) and the standard deviation value (X_S) are saved with the same data file as weights and biases. The testing data set will be scaled with the same scaling parameters as the training data set when the network is examined.

3.6.5 Neural network testing

The networks are examined with the test sets when the proposed networks are trained to meet the SSE goal. The Matlab function, *yp=simuff(xtest,W1,B1,'tansig',W2,B2,'logsig')*

[42], is used to simulate the target variables. Testing the network involves presenting the test set to the network and calculating the error. The target variable is compared with the actual variables (*yt*); then, the correct classification rate is calculated as a percentage based upon the number of correct classifications out of the total number of tests in each set.

3.7 Classification performance of proposed neural networks

In this section, the performance of proposed neural networks will be compared consisting of NN, PC-NN, and PC-GA-NN; the NN is the network that used original data from only FFT, the PC-NN is the network that used the PCA to reduce the original data dimension by the correlated method, and the PC-GA-NN is the network that used the PCA to reduce the original data dimension by trial and error (GA) method. The performances of the proposed networks are tested in two categories. First, the networks are tested with the simulation test sets as previously mentioned. Second, the networks are evaluated with the experimental test set. The tested results along with the testing data sets are illustrated in Table 3.3. Clearly, in the simulation test set, all proposed networks have a good classification performance (about 95%); therefore, the classification performance of the networks is quite satisfactory. The misclassification samples are the same operation point and class which are 0.65 modulation index and fault B-. This result suggests that both networks have confusion between Fault A- and Fault B- at low modulation index.

Table 3.3. Confusion table.

Testing set	Target	Actual Output			% Classification		
		NN	PC-NN	PC-GA-NN	NN	PC-NN	PC-GA-NN
Simulation test set	Normal [1 1 1]	1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1	100%	100%	100%
	Fault A+ [0 0 1]	0 0 1 0 0 1 0 0 1 0 0 1	0 0 1 0 0 1 0 0 1 0 0 1	0 0 1 0 0 1 0 0 1 0 0 1	100%	100%	100%
	Fault A- [0 1 0]	0 1 0 0 1 0 0 1 0 0 1 0	0 1 0 0 1 0 0 1 0 0 1 0	0 1 0 0 1 0 0 1 0 0 1 0	100%	100%	100%
	Fault B+ [1 0 1]	1 0 1 1 0 1 1 0 1 1 0 1	1 0 1 1 0 1 1 0 1 1 0 1	1 0 1 1 0 1 1 0 1 1 0 1	100%	100%	100%
	Fault B- [1 1 0]	1 1 0 1 1 0 1 1 0 0 1 0	1 1 0 1 1 0 1 1 0 0 1 0	1 1 0 1 1 0 1 1 0 0 1 0	75%	75%	75%
% Classification performance in simulation test set					***95%***	***95%***	***95%***
Experiment test set	Normal [1 1 1]	1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1	100%	100%	100%
	Fault A+ [0 0 1]	0 1 1 0 1 1 0 1 1 0 1 0	0 0 1 0 0 1 0 0 1 0 0 1	0 0 1 0 0 1 0 0 1 0 0 1	75%	100%	100%
	Fault A- [0 1 0]	0 1 0 0 1 0 0 1 0 0 0 1	0 1 0 0 1 0 0 1 0 0 1 0	0 1 0 0 1 0 0 1 0 0 1 0	75%	100%	100%
	Fault B+ [1 0 1]	1 0 1 1 0 1 1 0 1 1 0 1	1 0 1 1 0 1 1 0 1 1 0 1	1 0 1 1 0 1 1 0 1 1 0 1	100%	100%	100%
	Fault B- [1 1 0]	1 1 0 1 1 0 1 1 0 0 1 0	1 1 0 1 1 0 1 1 0 0 1 0	1 1 0 1 1 0 1 1 0 1 1 0	75%	75%	100%
%Classification performance in experimental test set					***85%***	***95%***	***100%***
Total %Classification performance					**90%**	**95%**	**97.5%**

The second category of testing results is also illustrated in Table 3.3. Obviously, the classification performance of PC-GA-NN is better than NN by 15% points and PC-NN by 5%. The NN has 85 % classification performance, and PC-NN has 95% classification, whereas PC-GA-NN has 100% classification performance. As expected, PCA conveys lower dimensional input space, reducing the time necessary to train a neural network. Also, the reduced noise could improve the mapping performance which leads to the improvement of total classification performance. GA offers the multivariable search of the minimum misclassification error providing the better neural network performance. Obviously, PC-GA-NN has a better overall classification performance of about 2.5% and 7.5 % points compared with PC-NN and NN, respectively. The results show that the application of GA and PCA can improve the classification performance of the neural networks. One know that the higher classification performance of the proposed neural networks could give higher reliability of fault diagnosis system in MLID.

3.8 Summary

The methodology of the proposed AI-based fault diagnostic system in a cascaded multilevel inverter drive (MLID) has been presented in this chapter. As can be seen, a genetic-algorithm-based selective principal component neural network method can be applied to a fault diagnostic system in a cascaded multilevel inverter. The GA-PC-NN performs very well with both simulation and experimental testing data set. The total classification performance is very good by about 97.5% points. Obviously, the results show that the PC-GA-NN has a better overall classification performance than PC-NN by

about 2.5% points. PCA conveys lower dimensional input space and reduces the time necessary to train a neural network. Also, the reduced noise may improve the mapping performance. In addition, GA offers multivariable optimized search so that the best combination of PCs or the minimum misclassification rating could be found, which leads to the improvement of total classification performance of the neural networks. Consequently, by utilizing PCA and GA, the reliability of fault diagnosis system in MILD can be improved. In the next chapter, the proposed reconfiguration technique will be presented.

4. RECONFIGURATION TECHNIQUE

4.1 Introduction

Fault diagnostic or monitoring system should consist of four major functions: fault detection, diagnostic fault effects, reconfiguration, and shutdown in emergency action. Fault detection and diagnosis are discussed in chapter 3. After the classification result provided by the output of the neural network is received, the corrective action taken is required to reconfigure the MLID from malfunction. Therefore, a reconfiguration technique for multilevel inverters incorporating a diagnostic system based on neural network is proposed in this chapter. The basic principal of the reconfiguration method is to bypass the faulty cell (H-bridge); then, other cells in the MLID are used to compensate for the faulty cell. The proposed reconfiguration technique is very simple to implement because the proposed technique is based on digital logic gate; a simple AND gate and OR gate can be implemented for this reconfiguration method. In addition, the effects of using the proposed reconfiguration technique at high modulation index are addressed.

4.2 Corrective action taken

The basic principal of the reconfiguration method is to bypass the faulty cell (H-bridge); then, other cells in the MLID are used to compensate for the faulty cell. For instance, if cell 2 of MLID in Figure 1.5 has an open circuit fault at S_{A+}; accordingly, S_{A-} and S_{B-} need to be turned on (1), whereas S_{B+} needs to be turned off (0) to bypass cell 2. The corrective actions taken for other fault locations are shown in Table 4.1. As can be seen, the corrective action would be the same for cases that have similar voltage waveforms during their faulted mode (for instance, see Figure 3.6 for a short circuit fault in S_{A+} and open circuit fault in S_{A-}). Therefore, even if the fault may be misclassified (an actual short circuit fault at S_{A+} is misclassified as an open circuit fault at S_{A-} or vice versa), the corrective action taken would still solve the problem.

Table 4.1. Gate drive signals of corrective action taken.

Fault types	***Locations***	***Signal S_{A+}***	***Signal S_{A-}***	***Signal S_{B+}***	***Signal S_{B-}***
Open circuit	S_{A+}	0	1	0	1
	S_{A-}	1	0	1	0
	S_{B+}	0	1	0	1
	S_{B-}	1	0	1	0
Short circuit	S_{A+}	1	0	1	0
	S_{A-}	0	1	0	1
	S_{B+}	1	0	1	0
	S_{B-}	0	1	0	1

4.3 Reconfiguration method

The reconfiguration diagram for an 11-level MLID with 5 SDCS is illustrated in Figure 4.1. It should be noted that multilevel carrier-based sinusoidal PWM is used as shown in Figure 4.2. The basic principle of the reconfiguration method is to use other cells (H-bridge) to compensate for the faulty cell. As known, the turn-on intervals of each cell are not equal with multilevel carrier-based sinusoidal PWM; cell 1 has the longest turn-on interval, then the turn-on interval decreases from cell 2 to cell 5 as staircase PWM waveform. The desired output voltage of a MLID can be achieved by controlling modulation index (m_a). For instance, suppose cell 2 has an open circuit fault at S_1 while the MLID operates at m_a = 0.8/1.0 (MLID is operated with four cells (cell 1-4)). One can see from Figure 4.1 (b) that S_3 and S_4 need to be turned on, then the gate signal of cell 2 will be shifted up to control cell 3, then the gate signal of cell 3 will shift to cell 4, and the gate signal of cell 4 will shift to cell 5 respectively. This reconfiguration also applies to other phases of MLID in order to maintain balanced output voltage. By using this method, the operation of MLID from 0.0 to 0.8 (out of 1) can be compensated such that the inverter will continue to function like normal operation; however, if MLID operates at $m_a > 0.8$ and has a fault, the lower order harmonics will occur in the output voltage since the MLID will operate at overmodulation region in order to try to continue to output the full requested voltage as illustrated in Figure. 4.3. To solve this problem, space vector, and third harmonic injection PWM schemes may be used. Also, a redundant cell can be added into the MLID, but the additional part count should be considered. Therefore, if the fault types and location can be detected, the continuous operation can be achieved.

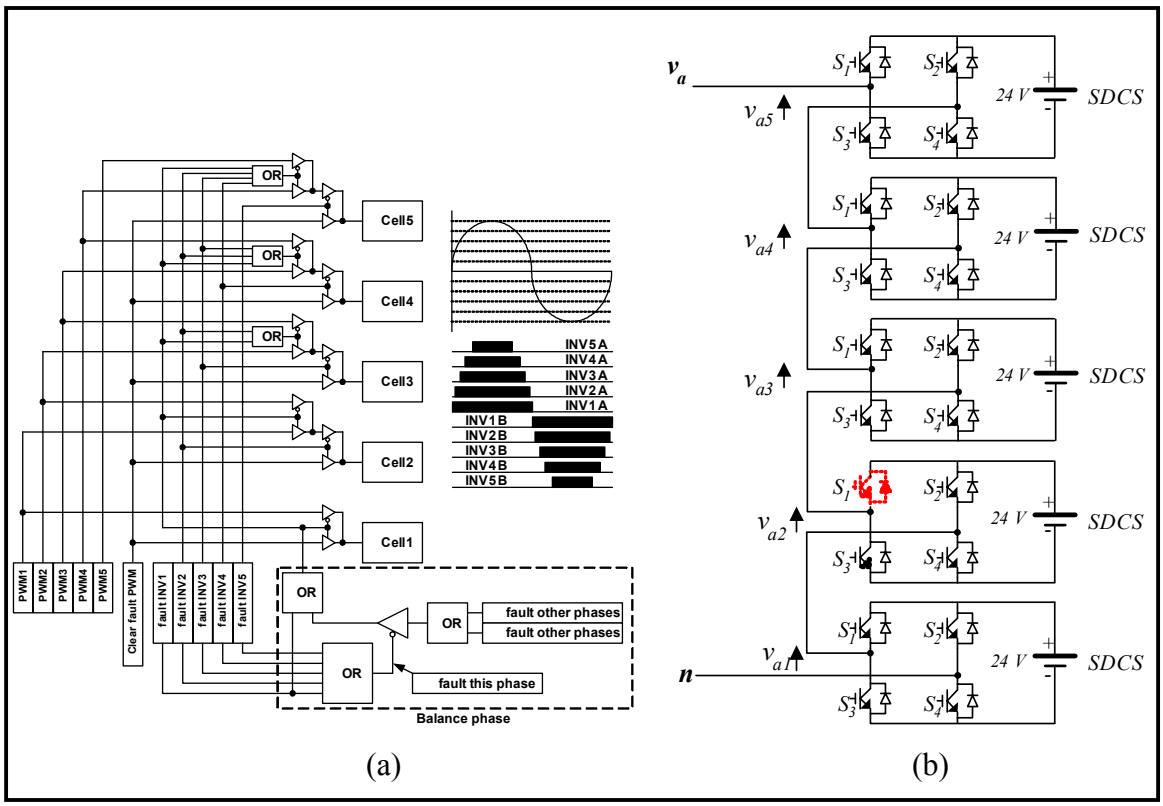


Figure 4.1. Reconfiguration diagram for MLID with five SDCS: (a) Reconfiguration diagram, (b) H-Bridge 2 Switch S_1 open circuit fault at second level of single-phase multilevel-inverter with 5 SDCS.

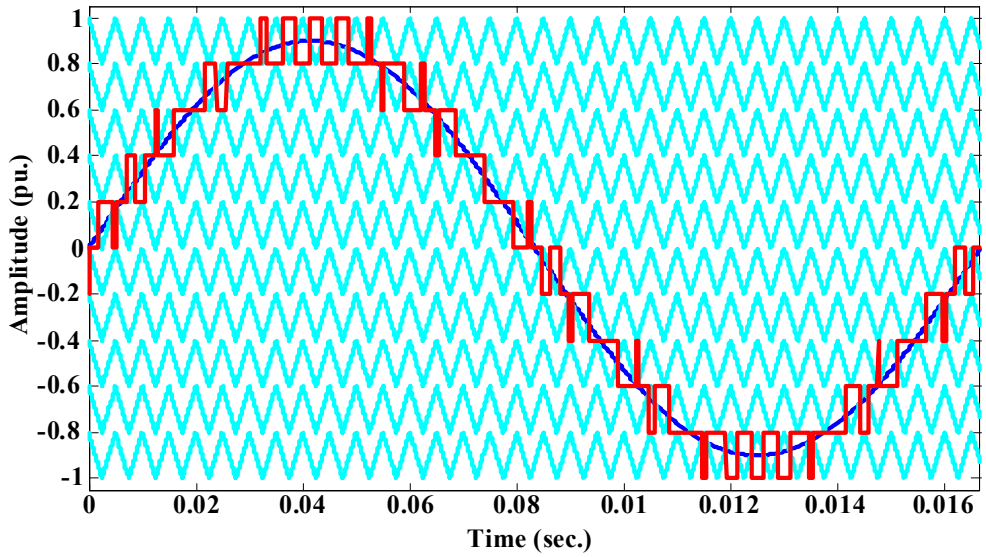


Figure 4.2. Multilevel carrier-based sinusoidal PWM with 2 kHz switching frequency for 5 SDCS MLID showing carrier bands, modulation waveform, and inverter output waveform (m_a = 0.9/1.0).

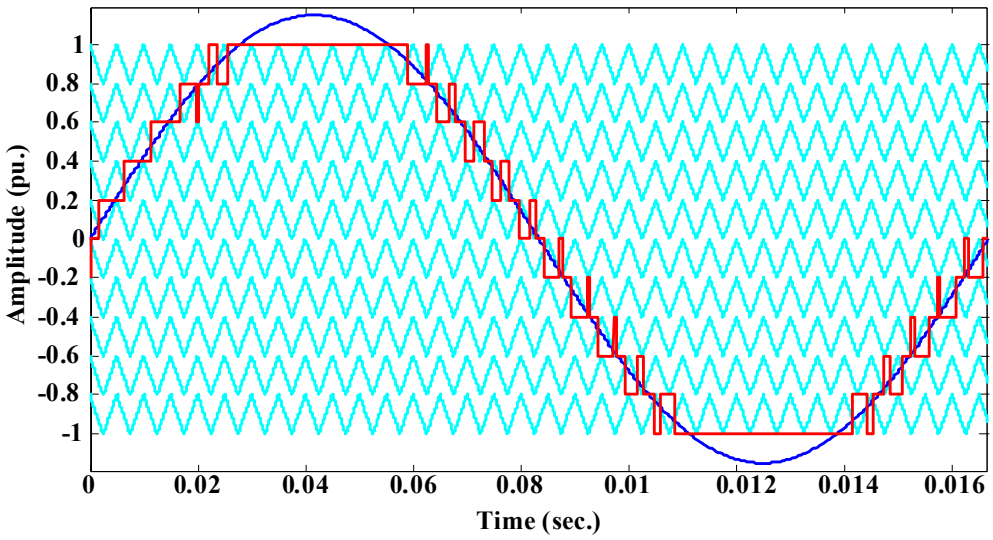


Figure 4.3. Multilevel carrier-based sinusoidal PWM with 2 kHz switching frequency for 5 SDCS MLID showing carrier bands, modulation waveform, and inverter output waveform (m_a = 1.2/1.0)

As previously mentioned, the operation under faulty condition requires the compensation gains during the MLID operating at $m_a > 0.8$ to keep the full requested output voltage. The compensated gain of the MLID operating at $m_a > 0.8$ is shown in Figure 4.4 This compensated gain can also be written as a function of m_a by using polynomial curve fitting. The fitting function can predict the compensated gain with a norm of residuals less than 0.09. One can see that the lower harmonic orders due to operating in overmodulation region will occur when the MLID operates at $m_a > 0.825$.

The compensated gain in the function of m_a can be conveniently implemented in the Simulink model. Figure 4.4 shows that the coefficient of polynomial curve fitting is high; this may lead to higher compensated errors due to noisy signal. However, in this particular case, the modulation signal is a constant value varying from 0.0 to 1.0.

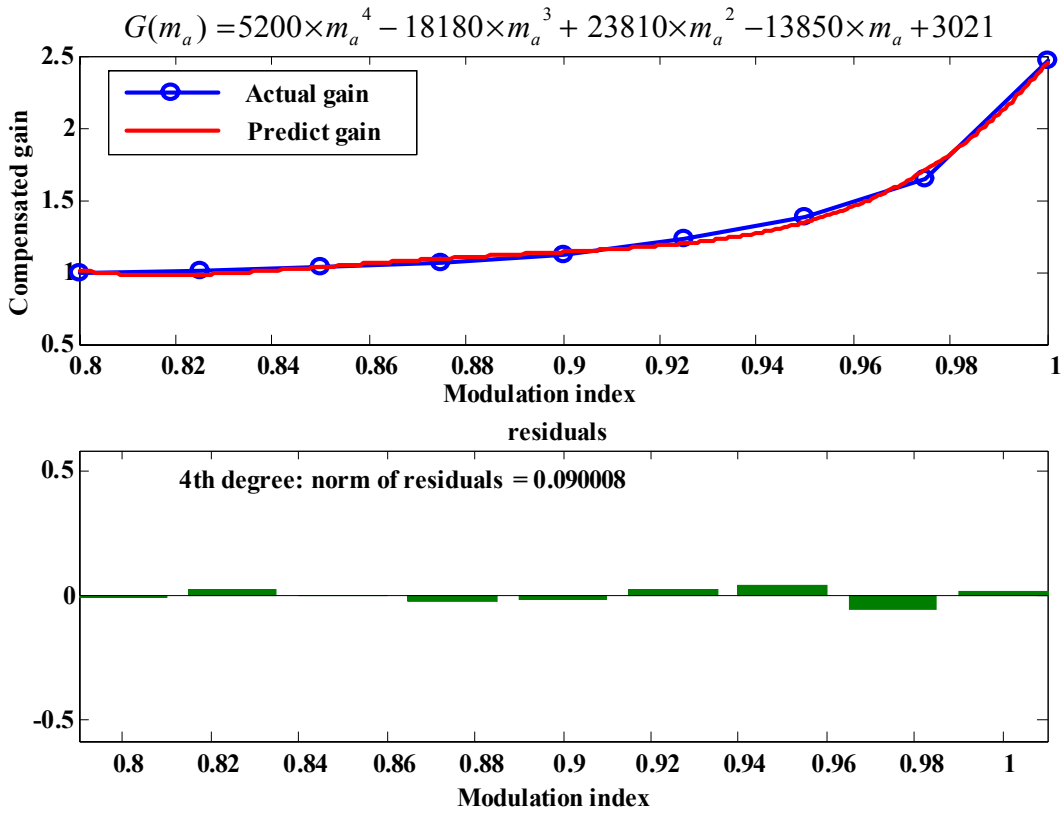


Figure 4.4. Compensated gain of the MLID operating at $m_a > 0.8$.

4.4 Reconfiguration effects and limitations

The proposed reconfiguration technique is simple to implement because the proposed technique is based on digital logic gate; a simple AND gate and OR gate can be implemented to this reconfiguration method. Unfortunately, the reconfiguration method has a limitation. Table 4.2 represents the maximum output phase voltage available of a MLID with 5 SDCS of 24 V/cell. As can be seen, the MLID can only operate at 50% of maximum m_a (1.0) if the MLID has two faulty cells. This means that MLID can drive the

traction motor only at half load condition, although the MLID operates in staircase mode. Nevertheless, the MLID can drive at full load condition in staircase mode if the MLID has only one faulty cell. The amount of reduction in capacity that can be tolerated depends upon the application; however, in most cases a reduction in capacity is more preferable than a complete shutdown.

As previously mentioned, if the MLID operates at $m_a > 0.9$, the output voltage harmonic distortion (THD_V) is higher because of additional lower harmonics when the converter is operated in overmodulation after reconfiguration. The MLID will operate at over modulation region or staircase mode because the compensated gain is needed to keep the full requested output voltage. Table 4.3 shows the comparison between normal and faulty operation of the MLID. One can see that the THD_V increases more than 4 times of normal operation at $m_a = 1.0$, whereas the THD_V slightly increases (about 1%) when MLID operates at $m_a = 0.9$.

The reconfiguration effects on THD_V are also shown in Figure 4.5. As can be seen, the lower order harmonics increase for both operating points, whereas the higher order harmonics, particularly at 34^{th}-38^{th} orders, decrease because of 2 kHz switching frequency.

Table 4.2. Maximum output phase voltage available of a MLID with 5 SDCS of 24V/cell.

Number of faulty cells	Maximum $\mathbf{m_a}$ can be compensated	*Fundamental component of output phase voltage available,* $V_{an,1}$ (rms)
1	1.0144	85.98 V
2	0.7624	64.42 V
3	0.5062	42.92 V
4	0.2525	21.40 V

Table 4.3. Comparison between normal and faulty operation of a MLID with 5 SDCS of 24 V/Cell.

Modulation index at an operating point	*Operating condition*	*Fundamental component of output phase voltage,* $V_{an,1}$ *(rms)*	*Compensated gain*	THD_V *(%)*
0.9/1.0	Normal	76.28 V	1	11.39%
	One faulty cell	76.28 V	1.12	12.43%
1.0/1.0	Normal	84.88 V	1	9.26%
	One faulty cell	84.88 V	2.47	31.97%

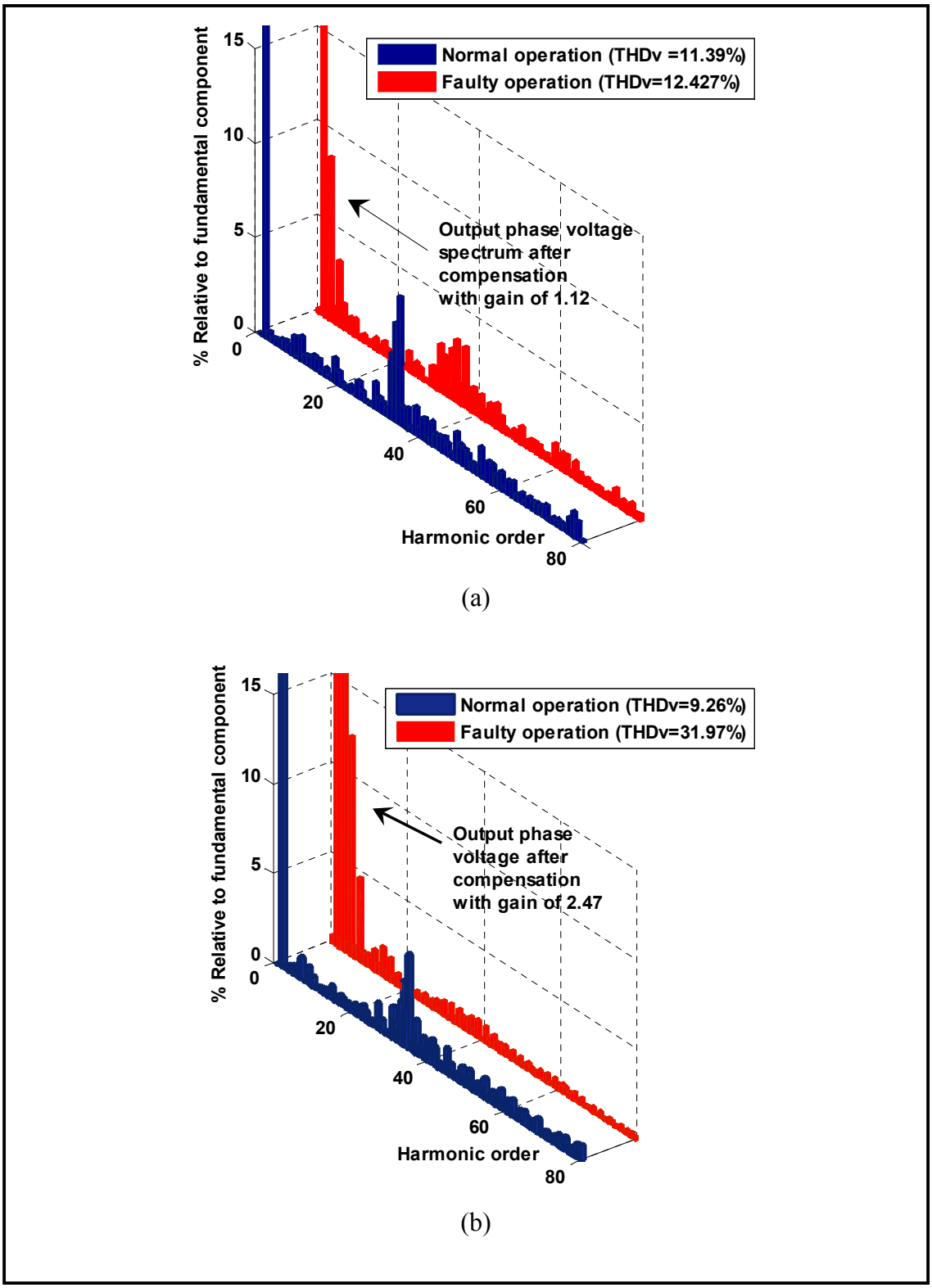


Figure 4.5. Reconfiguration effects at overmodulation index (a) normal operation m_a = 0.9/1.0, (b) normal operation m_a = 1.0/1.0.

The reconfiguration effect of increased THD_v under one faulty cell condition at $m_a > 0.8$ is shown in Figure 4.6. Again, the THD_v have more distortion if the MLID is operating at high modulation indices ($m_a > 0.925$). This harmonic voltage behavior is related to motor additional harmonic losses; the additional copper losses will increase, whereas the additional core losses will decrease as investigated in [5]. These additional losses can cause increased heating in the motor; also, increased harmonics can cause pulsating torque due to negative sequence currents. Also, an unbalanced output voltages effect of faulty MLID (See figure 1.2 with 24 V SDCS) is shown in Figure 4.7; the power cell 1 on phase B and power cell 1 and 2 on phase C are bypassed.

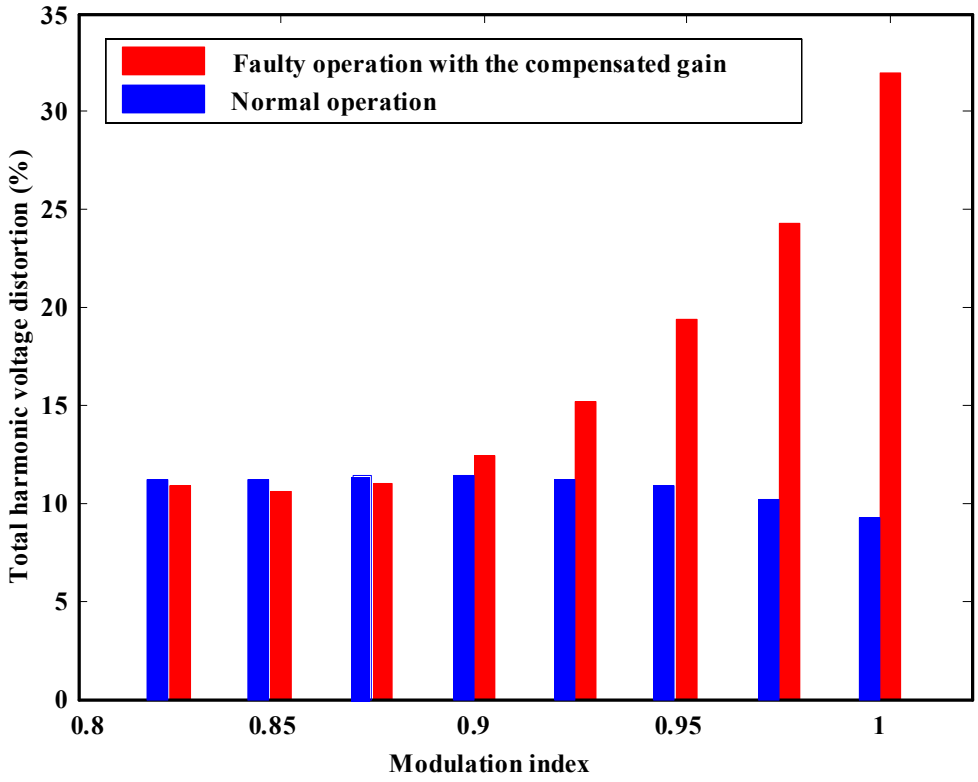


Figure 4.6. Total harmonic voltage distortion at different modulation indices under one faulty cell operation with their compensated gain.

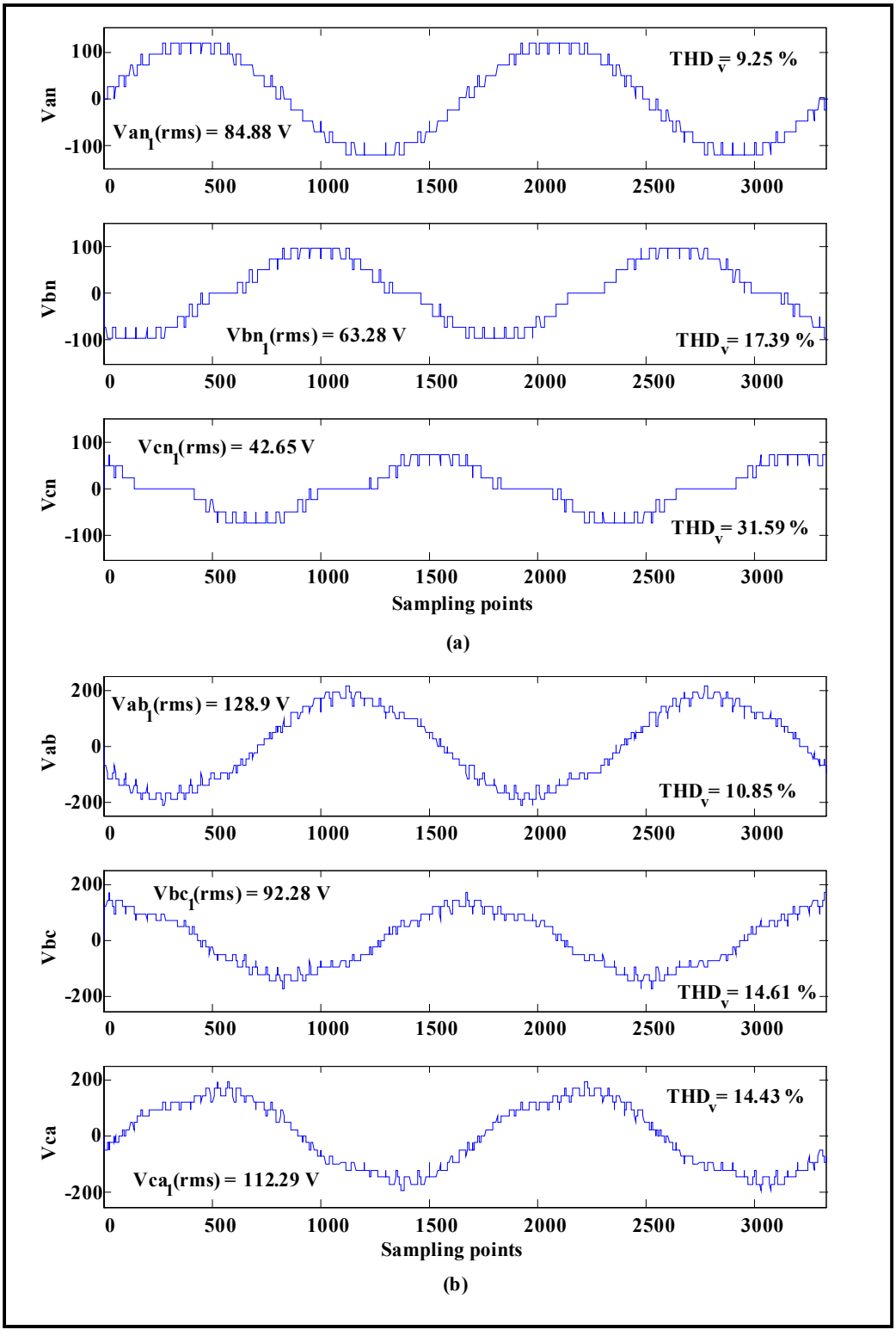


Figure 4.7. Output phase voltages (a) and line voltages (b) of malfunctioning MLID: bypassing cell 1 on phase B, cell 1 and 2 on phase C with 2 kHz switching frequency and 60 Hz fundamental frequency.

It is possible that the hybrid reconfiguration technique can be applied to reduce the harmonic effects and to avoid operation in the overmodulation region. If the malfunctioning MLID is running at m_a =1, the m_a should be maintained at unity after the MLID is reconfigured by the proposed method; then, the neutral shift technique proposed by [38] is performed. This hybrid reconfiguration method can provide a boost to the line voltage as shown in Table 4.4. One can see that the additional line voltages increase about 54 % with the hybrid reconfiguration when compared to the shifted gate signal if the MLID has three faulty cells; however, if MLID has only one faulty cell, the line voltage increase is about 6%. A study suggests that the hybrid reconfiguration technique can significantly improve available output voltages from the shifted gate signal technique when MLID has more than three faulty cells.

Table 4.4. Comparison line output voltages between a hybrid reconfiguration method and a shifted gate signal method.

Number of faulty cells can be compensated at **m_a =1**	Fundamental component of line-voltage available by **proposed hybrid method**		Fundamental component of phase-voltage available by **shifted gate signal method**	
	$V_{ab,1}$, $V_{bc,1}$ and $V_{ca,1}$ (rms)	$V_{an,1}$ (rms)	$V_{ab,1}$, $V_{bc,1}$ and $V_{ca,1}$ (rms)	$V_{an,1}$ (rms)
1	139.50	75.87	131.41	75.87
2	126.71	60.54	104.86	60.54
3	112.15	41.98	72.71	41.98
4	97.51	21.45	37.15	21.45

4.5 Summary

The reconfiguration technique for multilevel inverters incorporating a diagnostic system based on neural network has been proposed in this chapter. The basic principal of the reconfiguration method is to bypass the faulty cell (H-bridge); then, other cells in the MLID are used to compensate for the faulty cell. The proposed reconfiguration technique is simple to implement because the proposed technique is based on digital logic gate; a simple AND gate and OR gate can be implemented to this reconfiguration method. In addition, the effects of using the proposed reconfiguration technique at high modulation index have been discussed.

5. SIMULATION AND EXPERIMENT VALIDATION

5.1 Introduction

The simulation and experiment validation of the proposed fault diagnostic paradigm are presented in this chapter. In the simulation validation, two simulation programs are used. Matlab-Simulink is used to implement the neural network fault classification, and PSIM is used to implement the MLID power circuit. The reason of using PSIM is that the PSIM is a circuit-based simulation and conveniently interfaces with Matlab-Simulink via the toolbox called Simcouple. PSIM is also a simulation package especially designed for power electronics and motor controls; this would give us more options to perform the change of parameters and more realistic with practical circuits. After that, in the experimental validation, the Opal-RT-based platform is used to perform the Matlab-Simulink model; the same Simulink model used in the simulation will be converted into C code via Opal-RT software tool [56]. The Opal-RT will perform fault classification and generate gate drive signals; then, the gate drive signals interface with the hardware of five 24V-SDCS multilevel inverter. The results of simulation and experiment are also discussed.

5.2 Fault Diagnostic technique for 11-level MLID with 5 SDCS

Before continuing discussion, it should be mentioned that the methodology of fault diagnosis presented in Chapter 3 can be applied to any other cascaded H-bridges MLID. However, some minor processes are different such as neural network structure, input/output data set, and principal component (PC) selection. Since the simulation and experiment validation will be performed with 11-level MLID, the fault diagnostic processes for the 11-level MLID are explained as follows.

5.2.1 Neural network structure

The fault diagnostic diagram for an 11-level MLID with 5 SDCS is depicted in Figure 5.1. As can be seen, the neural network (NN) classification process consists of two networks: open circuit network and short circuit network. The training time and required memory for implementation are reduced with segregated NN as reported in [57-58]. Moreover, in this particular case, the short circuit data set includes the loss of separate dc source (SDCS) condition due to fuse protection because the fuse may blow before the fault is detected; therefore, the short circuit NN may contain more complexity than the open circuit neural network. Also, the NNs may be assigned to have the ability to provide "do not know" conditions. The multilayer feedforward networks (MLP) are used in both open circuit and short circuit NN. The NN architecture is based upon GA selection as discussed in section 3.5.4. The input neurons depend on how many PCs selected by GA; however, the hidden and output layer can be assigned. Therefore, the one hidden layer with 4 hidden nodes and 6 output nodes neural network architecture are used.

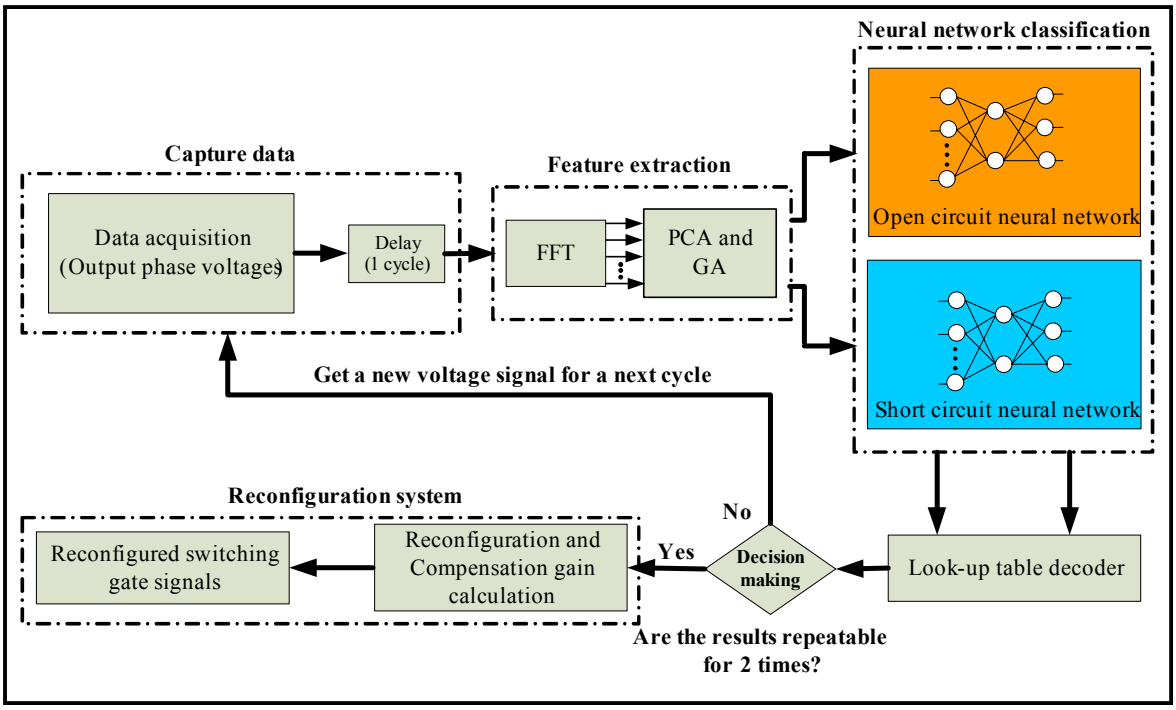


Figure 5.1. Fault diagnostic diagram for 11-level MLID with 5 SDCS.

5.2.2 Input/Output data

The input/output data set diagram for 11-level MLID is illustrated in Figure 5.2. One can see that the set of original input data set at each MLID operation point (modulation index) contains five fault classes: normal, Fault A+, A-, B+, and B-. Modulation indices (m_a) are observations changing with desired load. In this particular case, m_a is varied from 0.6 to 1.0 with 0.05 intervals. The original data are divided into two subsets: Open circuit and short circuit. Also, each subset is separated into one training set and two testing sets as shown in Figure 5.2. Both open circuit and short circuit neural networks are trained with both open and short circuit training set. However, the open circuit neural network

will be trained with short circuit training set and “do not know” target binary and vice versa with the short circuit neural network as depicted in Figure 5.2.

Target binary variables are also illustrated in Table 5.1. Six binary bits are used to code the input/output mapping. The first three bits (bit 5^{th}, 4^{th}, and 3^{rd}) are used to code the faulty cells, the 2^{nd} bit is used to code the fault types, and the next two bits (1^{st} and 0) are utilized to code the faulty switches. Also, the code [1 1 1 1 1 1] is used to represent the normal condition, whereas the code [0 0 0 0 0 0] is used to characterize the “do not know” condition. Therefore, the six output neurons are used for particular 11-level MLID. For instance, if the neural network provides [0 1 1 0 0 1] as the outputs, one can decode the fault type and location as cell 3 is faulty with open circuit fault at switch S_A-. This decoder paradigm can be implemented in a Simulink model by using 2-D dimension look-up table which is explained later in this chapter.

The output binaries provided by both neural networks are also required to give the same classification results for two times with the same input voltage signal. If the network provides different classification results, the reconfiguration process will not perform, and then a new cycle of the voltage signal is required for another classification process. The objective of this process is to provide more confidence in the classification result before taking action. Also, the detection process will allow the diagnostic system to acquire the output voltage signal only 2 times for short circuit cases and 3 times for open circuit cases. This means if the detection process can not give repeatable results, an operator will be notified, and then emergency action will be performed.

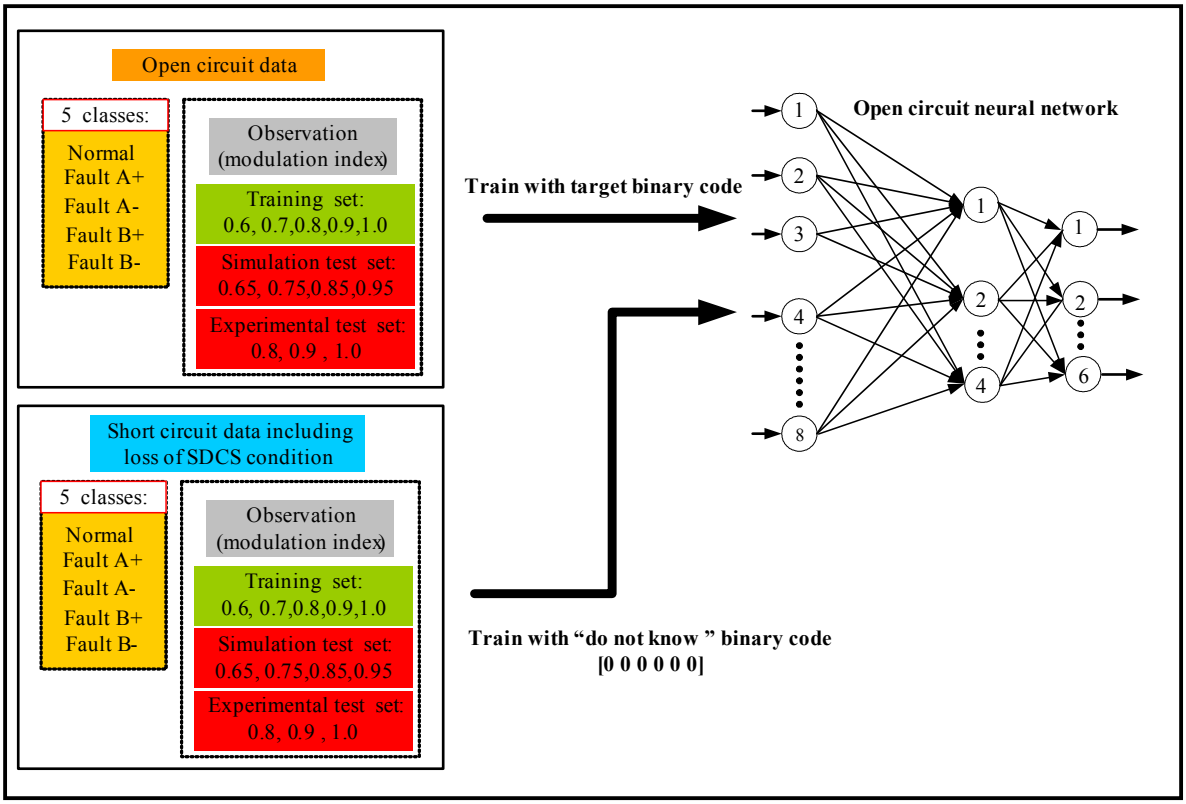


Figure 5.2. Training and testing data set diagram.

Table 5.1. Target binary codes for 11-level MLID.

Condition		Number of binary bits and their description					
		Faulty cell			*Fault type*	*Faulty switch*	
		5	4	3	2	1	0
Normal		1	1	1	1	1	1
Faulty cells	1	0	0	1	-	-	-
	2	0	1	0	-	-	-
	3	0	1	1	-	-	-
	4	1	0	0	-	-	-
	5	1	0	1	-	-	-
Fault types	open	-	-	-	0	-	-
	short	-	-	-	1	-	-
Faulty switches	Fault A+	-	-	-	-	0	0
	Fault A-	-	-	-	-	0	1
	Fault B+	-	-	-	-	1	0
	Fault B-	-	-	-	-	1	1
"Do not know"		0	0	0	0	0	0

5.2.3 Principal component selection

By using the methodology proposed in section 3.5.5, the principal components (PCs) selected by the genetic algorithm (GA) are represented in Table 5.2. As can be seen, 8 PCs are selected for open circuit neural network, whereas 11 PCs are chosen for the short circuit neural network. Also, the same PCs (*1, 2, 3, 5, 7, 8, 13, and 14*) as presented in section 3.5.5 are selected for open circuit fault neural network. Conversely, the GA chooses different PCs (*2, 3, 4, 5, 7, 8, 9, 11, 12, 13, and 14*) for the short circuit neural network. It should be noted that the training data for short circuit neural network also includes the short circuit fault for loss of SDCS conditions. Interestingly, as previously known in chapter 3, PC 1 corresponds with the dc component of MLID's output voltages and this dc component will naturally increase during faulty conditions as explained in section 3.3. However, the GA did not select PC 1 for shot circuit neural network. This result suggests that the PC 1 is not so important for short circuit neural network including training data of short circuit fault during loss of SDCS conditions. Therefore, the neural network architecture for open circuit neural network has 8 input neurons, 4 hidden neurons and 6 output neurons, whereas the short circuit neural network architecture has 11 input neurons, 4 hidden neurons and 6 output neurons.

Table 5.2. Principal component selected by GA for 11-level MLID.

Neural networks	Description	Outputs from *gatool*
Open circuit	*Final point*	*1 2 3 4 5 6 7 8 9 10 11 12 13 14* **1 1 1 0 1 0 1 1 0 0 0 0 1 1** ***PC 15-40 are all 0*** **0 0 0 0 0 0 0 0 0 0 0 0 0 0** **0 0 0 0 0 0 0 0 0 0 0 0**
	Fval	**0.205**
Short circuit with loss of SDCS conditions	*Final point*	*1 2 3 4 5 6 7 8 9 10 11 12 13 14* **0 1 1 1 1 0 1 1 1 0 1 1 1 1** ***PC 15-40 are all 0*** **0 0 0 0 0 0 0 0 0 0 0 0 0 0** **0 0 0 0 0 0 0 0 0 0 0 0**
	Fval	**0.773**

5.3 Simulation validation

Several Simulink subsystems are involved in the simulation tasks based on the Simulink model. The main Simulink model can be divided into three main subsystems: feature extraction, neural network classification, and reconfiguration.

5.3.1 Feature extraction subsystem

The feature extraction subsystem consists of two sub-functions: FFT and PCA. The signal processing toolbox [59] provided by Mathworks can be applied to perform FFT and PCA. The FFT subsystem interfaced with the Simulink model is illustrated in Figure 5.3. As can be seen, the output phase-voltage signals from the sensors are transferred to the FFT subsystem to perform signal transformation. At this state, it is necessary to point out that the one cycle delay of the phase-voltage signals is required before the FFT subsystem performs the signals' transformation. As previously mentioned in section 3.4, the default window of FFT requires one cycle to capture a signal; however, the FFT can be performed by a hardware card; one commercially available is FFT dual channel model 2080-2014 provided by DRS technology Inc [60]. It should be noted that a cycle delay is related with the fundamental frequency of output phase-voltage signals; for instance, a 60 Hz signal is 16.66 *ms* for a cycle. 1-39 order harmonics including a dc component are used in this particular simulation since a 2 kHz switching frequency is used. The FFT subsystem output size [1×40] matrix is passed to the PCA subsystem.

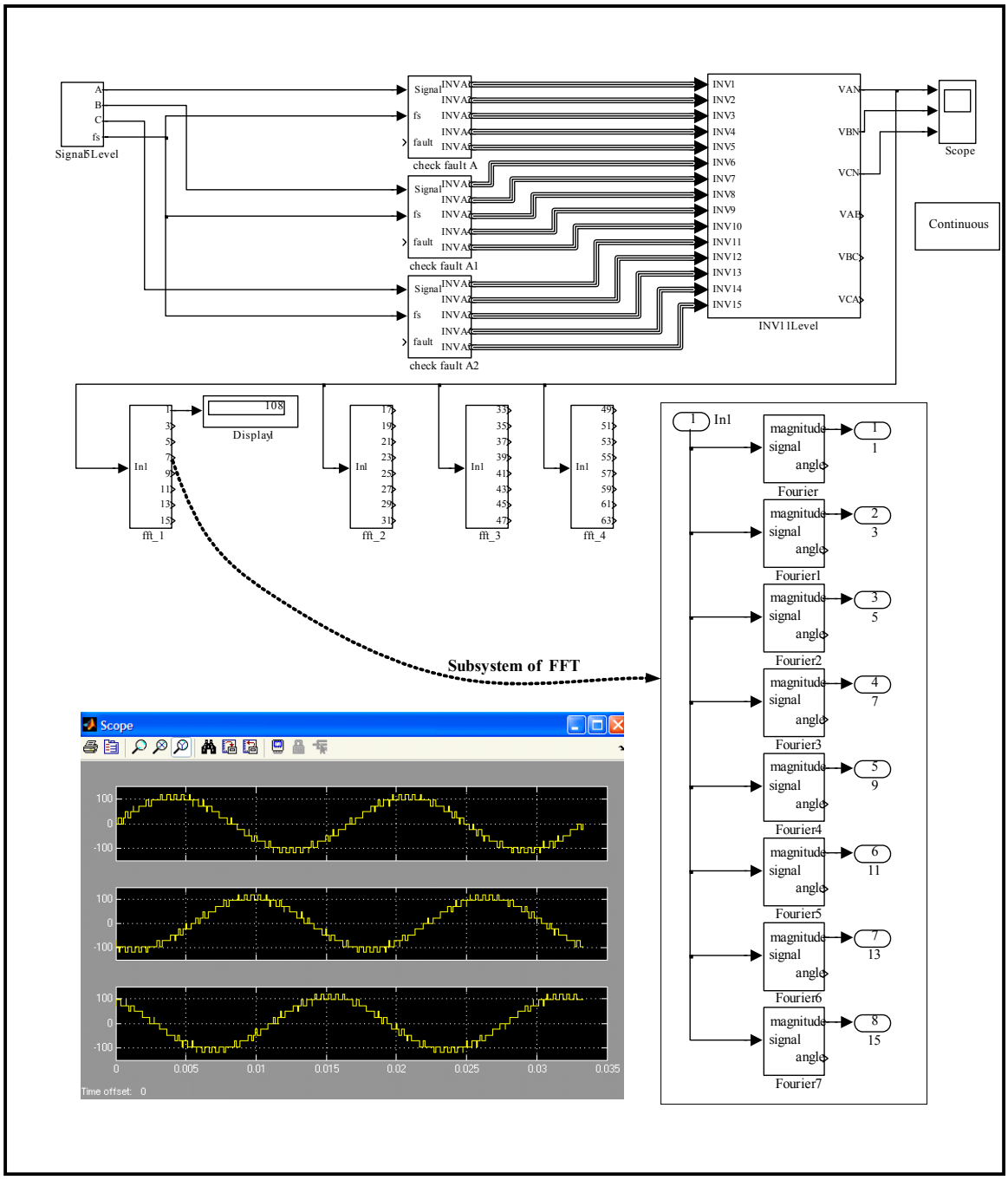


Figure 5.3. The FFT subsystem interfaced with a Simulink model.

The principal component analysis (PCA) is also performed by using the signal processing toolbox as illustrated in Figure 5.4. The transformed signals from the output of the FFT subsystem are sent to the PCA subsystem to transform the original data into PCA space. It should be noted that the valuable principal components (PC) selected by a genetic algorithm are performed "off line" meaning that wanted PCs are known a priori which PCs are required to keep in the model for the neural network classification as previously discussed in section 3.5. The outputs of the PCA subsystem are passed to the neural network classification subsystem.

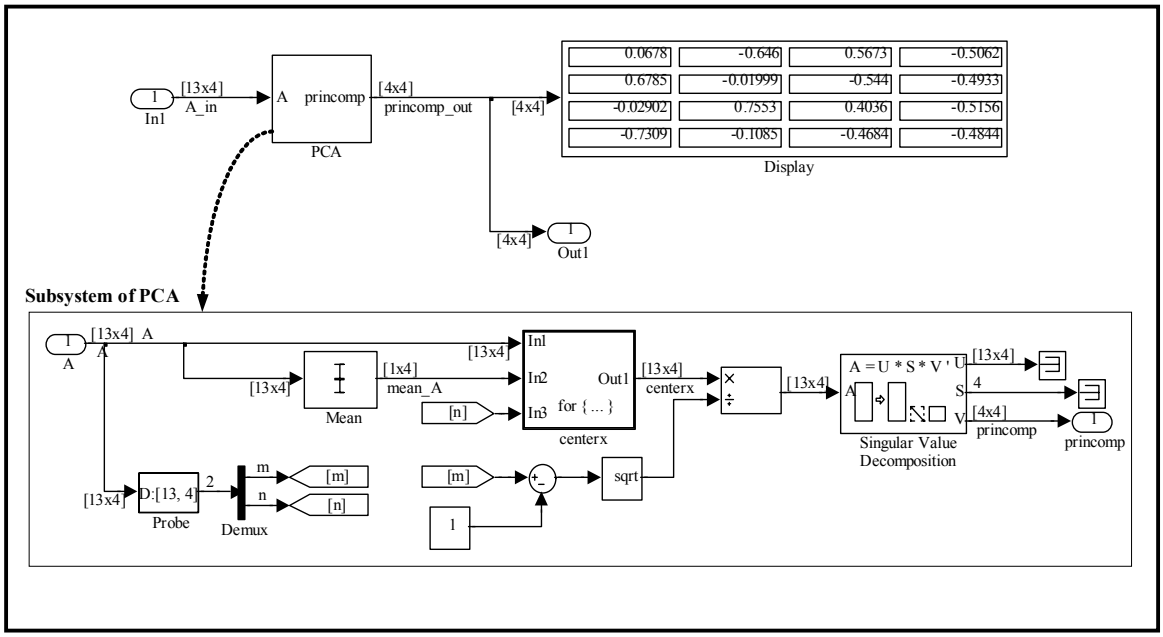


Figure 5.4. PCA subsystem performing data transformation into PCA space.

5.3.2 Neural network classification subsystem

The neural network classification subsystem can also be performed in the Simulink model using the neural network toolbox [42]. It should be noted that the creating and training process of the neural network are also performed off-line as previously demonstrated in section 3.6. Then, the neural network can be easily incorporated into a Simulink model by using the command, *gensim* [42]; a *gensim* command will automatically generate network simulation blocks for use with Simulink as shown in Figure 5.5; this feature also makes it possible to view the networks graphically. The outputs of the neural network classification subsystem are binary codes as shown in the scope in Figure 5.5. These outputs are transferred to the reconfiguration subsystem.

5.3.3 Reconfiguration subsystem

The reconfiguration subsystem consists of two functions: binary decoder and reconfiguration methods. It should be noted that the outputs from the neural network are not binary codes, so the *round* command is used to make the outputs to be binary codes. The output binary codes from the neural network are decoded into a fault hypothesis by using a 2-D look-up table as shown in Figure 5.6 (a). After the fault hypothesis is known, the reconfiguration method as discussed in section 4.3 is performed. Figure 5.6 represents the simple logic gate implemented in a Simulink-based model.

The interface between the fault diagnostic system in Simulink and PSIM is illustrated in Figure 5.5. The fault diagnostic model can be interfaced with PSIM via the Simcouple.

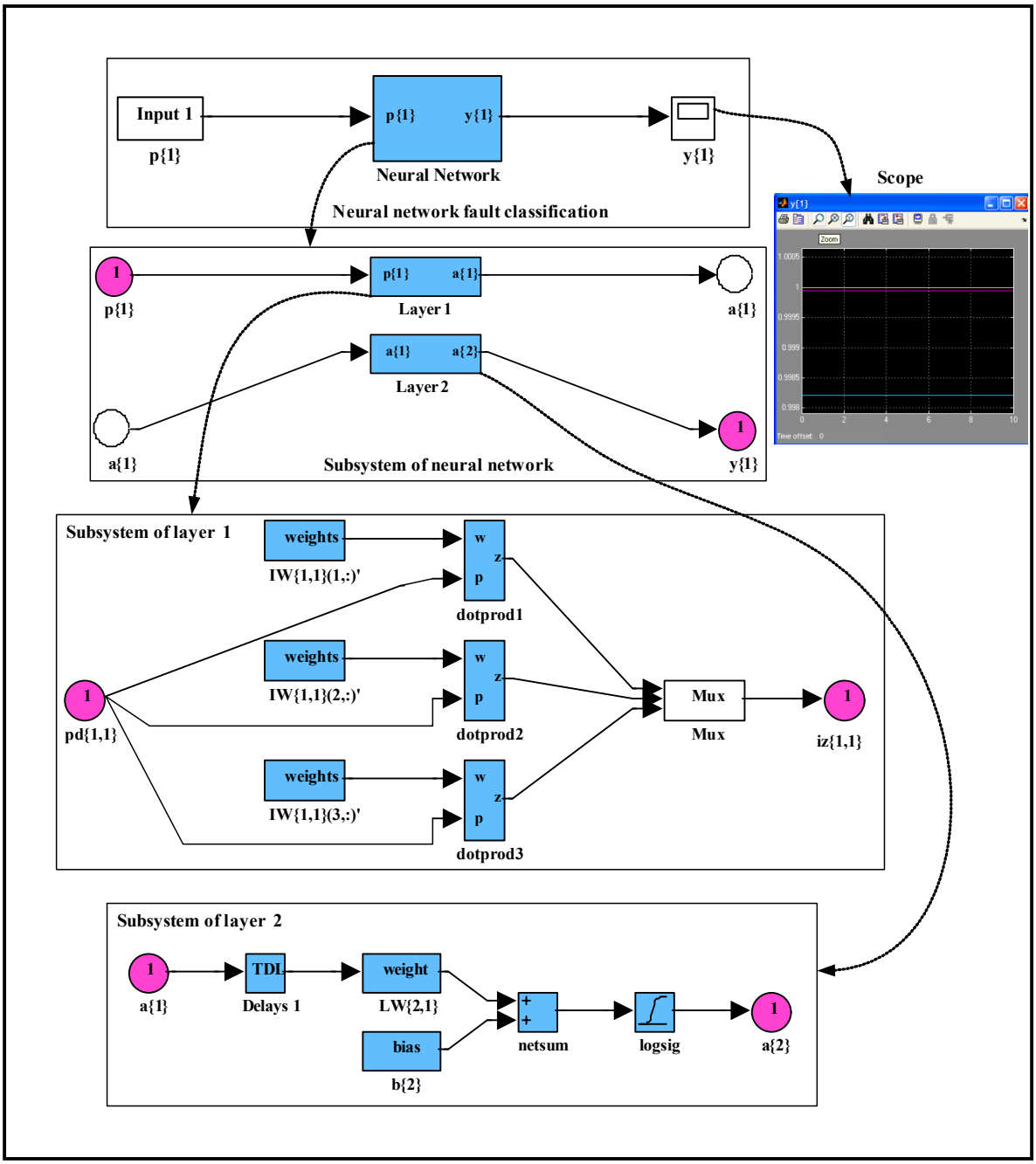


Figure 5.5. Subsystem of neural network classification.

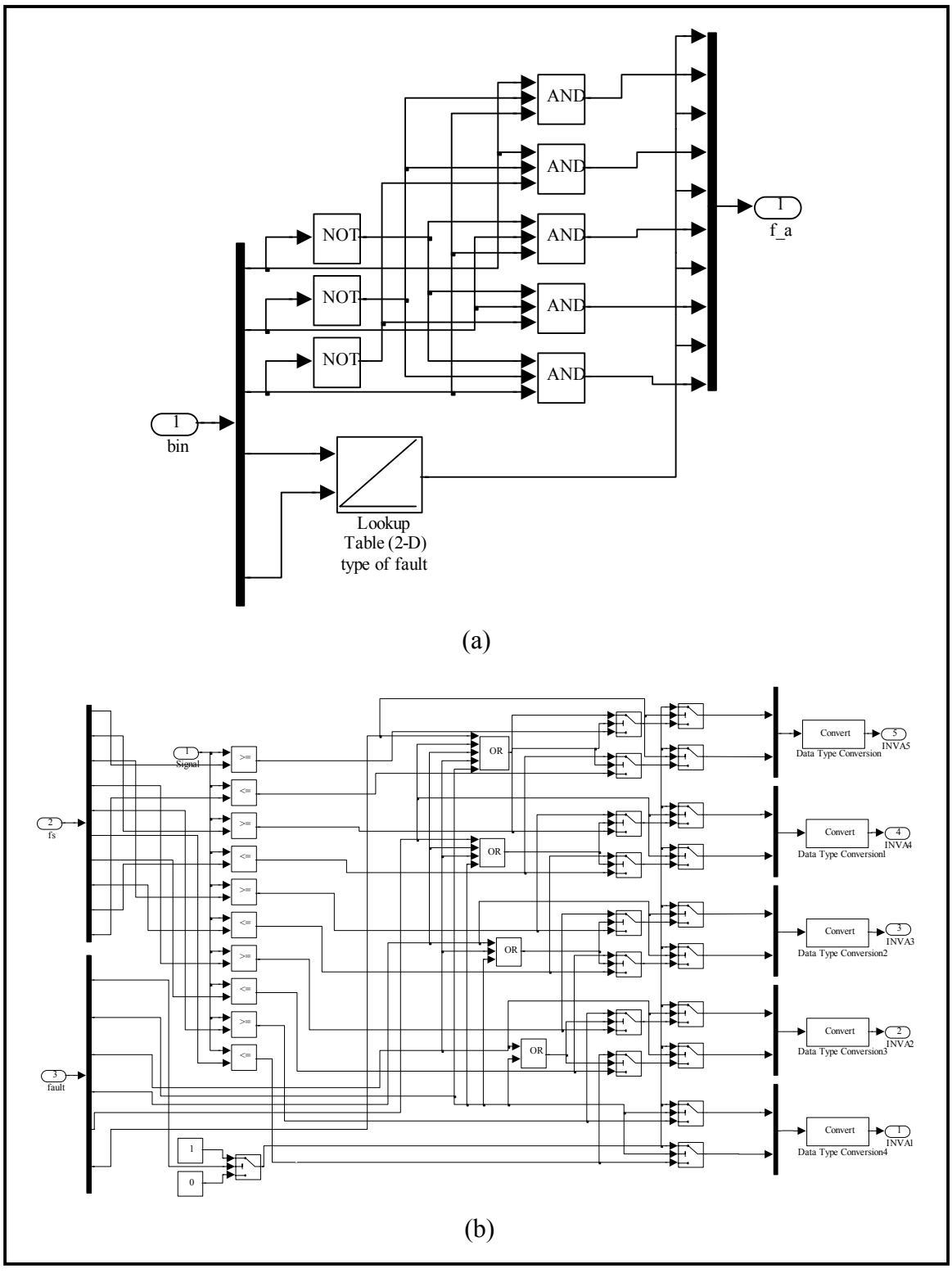


Figure 5.6. Subsystem of (a) binary decoder and (b) reconfiguration method.

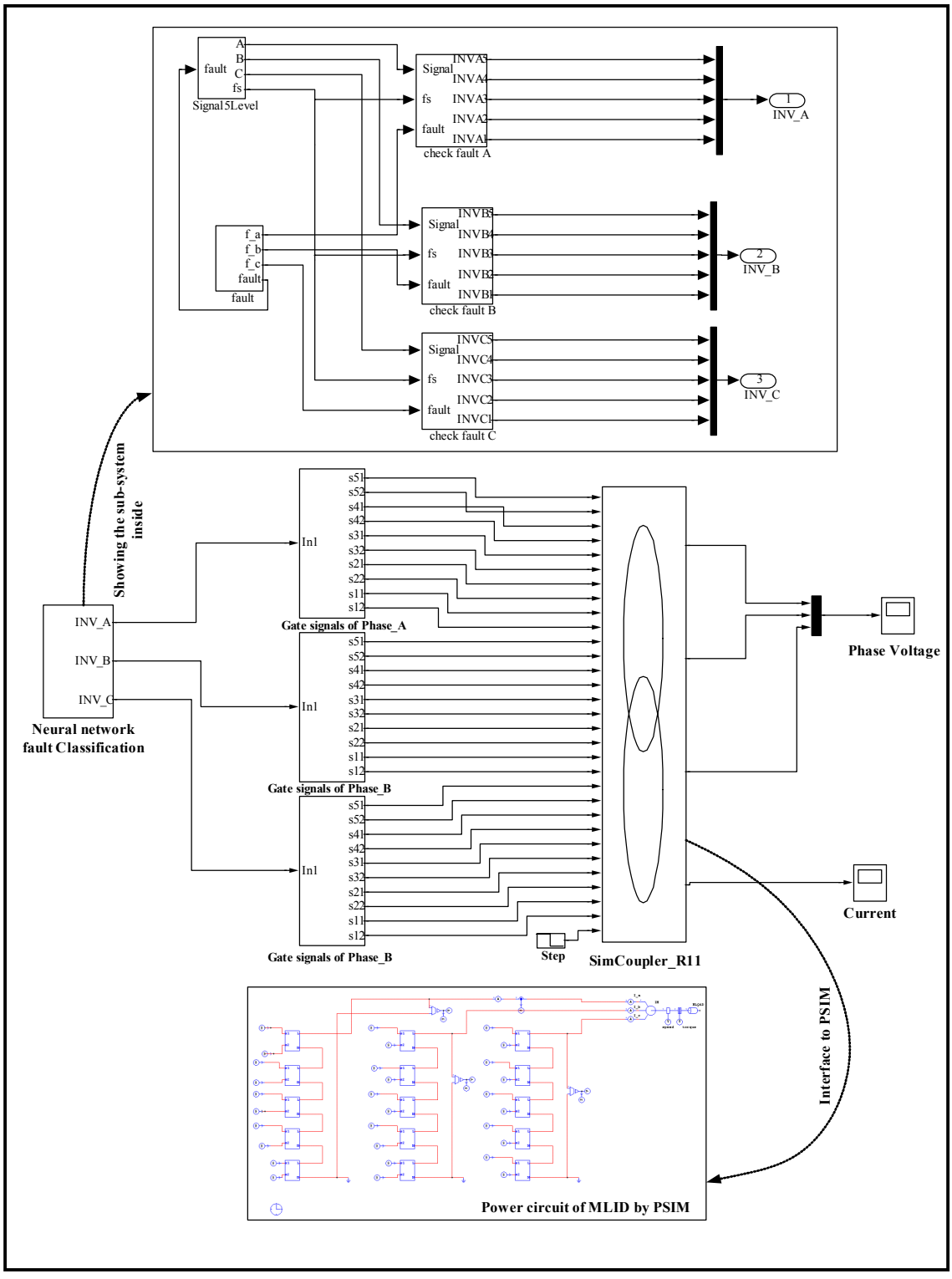


Figure 5.7. The fault diagnostic system interfaced with PSIM performing power circuit of a MLID.

5.4 Experiment validation

The experiment setup is represented in Figure 5.8. A three-phase wye-connected cascaded multilevel inverter using 100 V, 70 A MOSFETs as the switching devices is used to produce the output voltage signals. The MLID supplies an induction motor (1/3 hp) coupled with a dc generator (1/3 hp) as a load of the induction motor. The Opal RT-Lab system as shown in Figure 5.9 is utilized to generate gate drive signals and interfaces with the gate drive board. The switching angles are calculated by using Simulink based on multilevel carrier-based sinusoidal PWM. A separate individual 24-volt SDCS is supplied to each cell of the MLID, consisting of 5 cells per phase as shown in Figure 5.10. Open and short circuit fault occurrence are created by physically controlling the switches in the fault creating circuit. A Yokogawa DL 1540c is used to measure output voltage signals as ASCII files. The measured signals are set to N =10032; sampling frequency is 200 kHz. Voltage spectrum is calculated and transferred to the Opal-RT target machine.

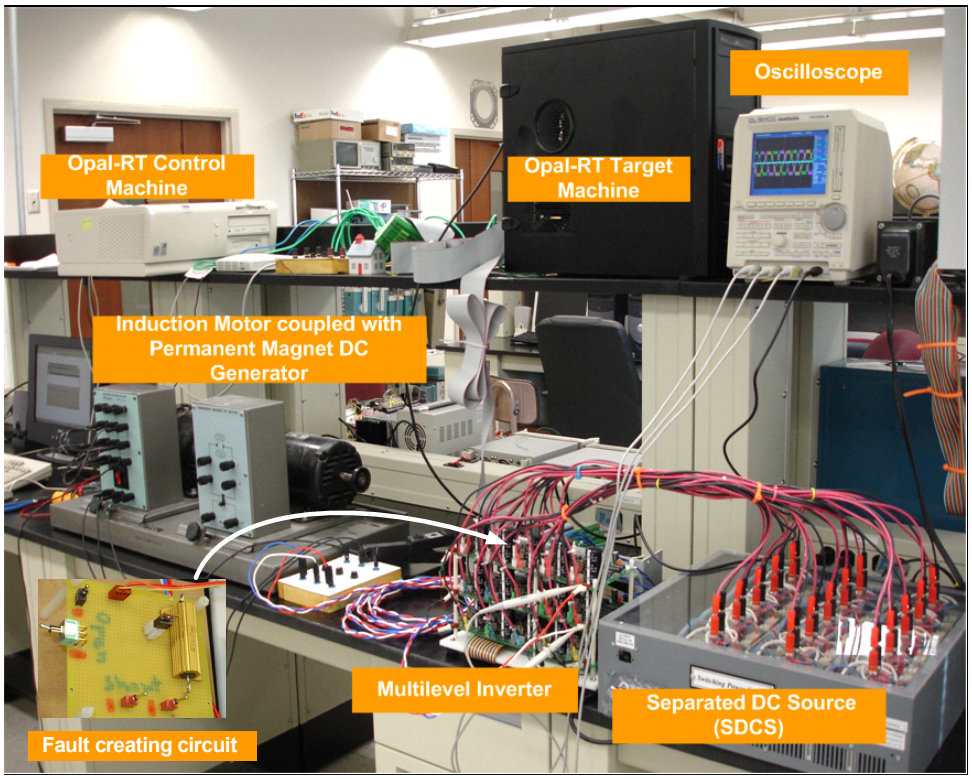


Figure 5.8. Experiment setup.

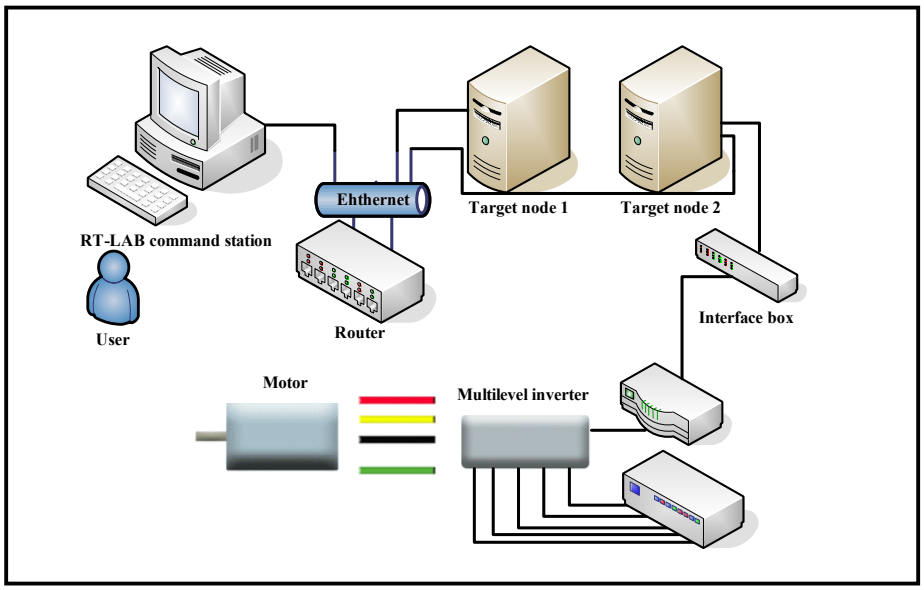


Figure 5.9. Hardware component for Opal RT-LAB configuration.

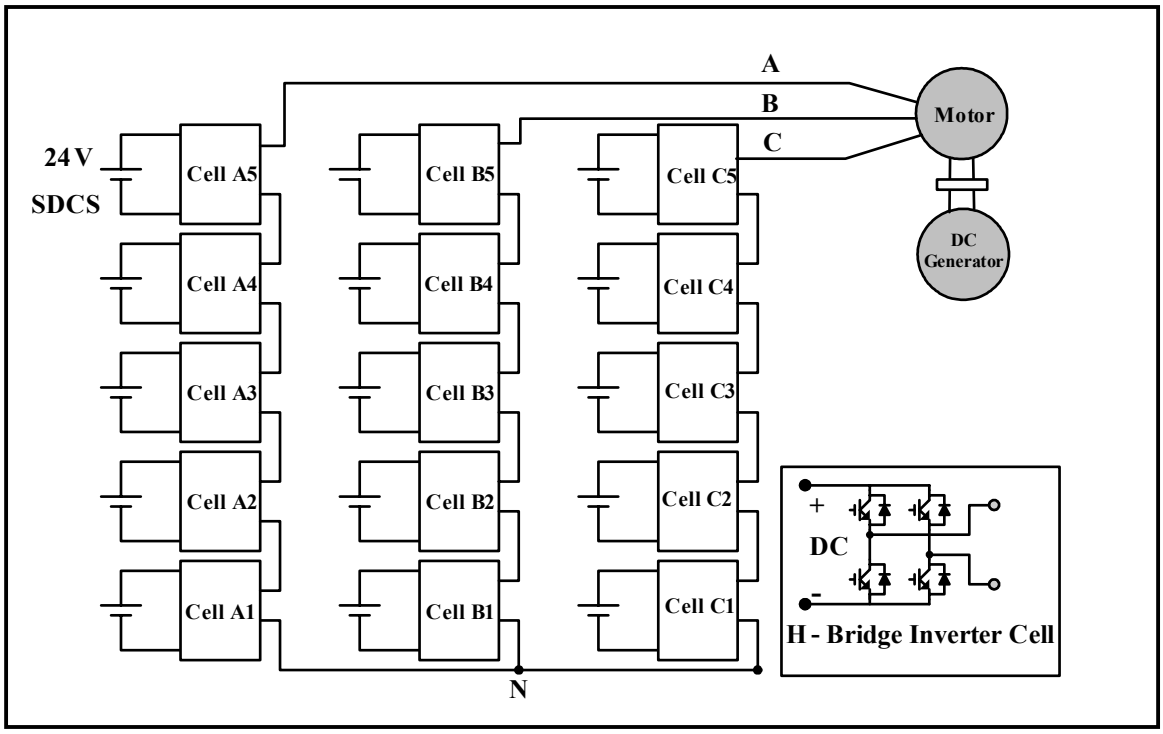


Figure 5.10. Three-phase wye-connection structure for electric vehicle motor drive.

5.5 Simulation and experiment results

An open circuit and short circuit fault in a power semiconductor switch are reported in this section. Before continuing discussion, the denotation of "open circuit fault" and "short circuit fault" used in this simulation and experiment validation should be clarified. The normal operation of an 11-level MLID at normal operation with 0.8/1.0 modulation index (m_a) is depicted in Figure 5.11. The open circuit fault, in this particular validation, consists of two cases: real open circuit case (both switch and its anti-parallel diode are disconnected) as shown in Figure 5.12 and loss of gate drive case as shown in

Figure 5.13. Obviously, the loss of gate drive case have different current waveforms compared to a real open circuit case during fault interval; also, output voltage signal of loss of gate drive case has lower spike than real open circuit fault when the fault occurs. This is because the anti-parallel diode at a faulty switch still connects in the cell in loss of gate drive case, so the line current can flow through the diode. The neural network may have difficulty to classify the faults because of spike of output voltage during the fault. However, the principal component analysis has inherited the ability to filter unwanted components (spike) for the neural network, and also both open circuit fault cases (loss of gate drive and switch failure) have the exact corrective action taken; therefore, the problems could be solved.

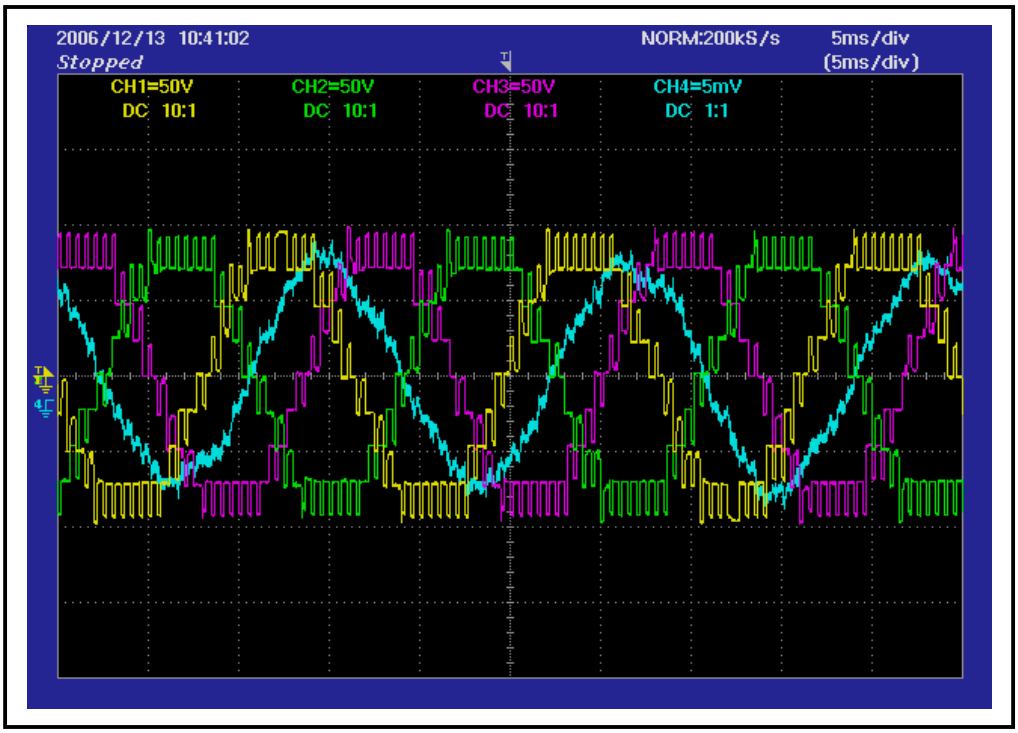


Figure 5.11. 11-level MLID operating at normal condition with 0.8/1.0 m_a.

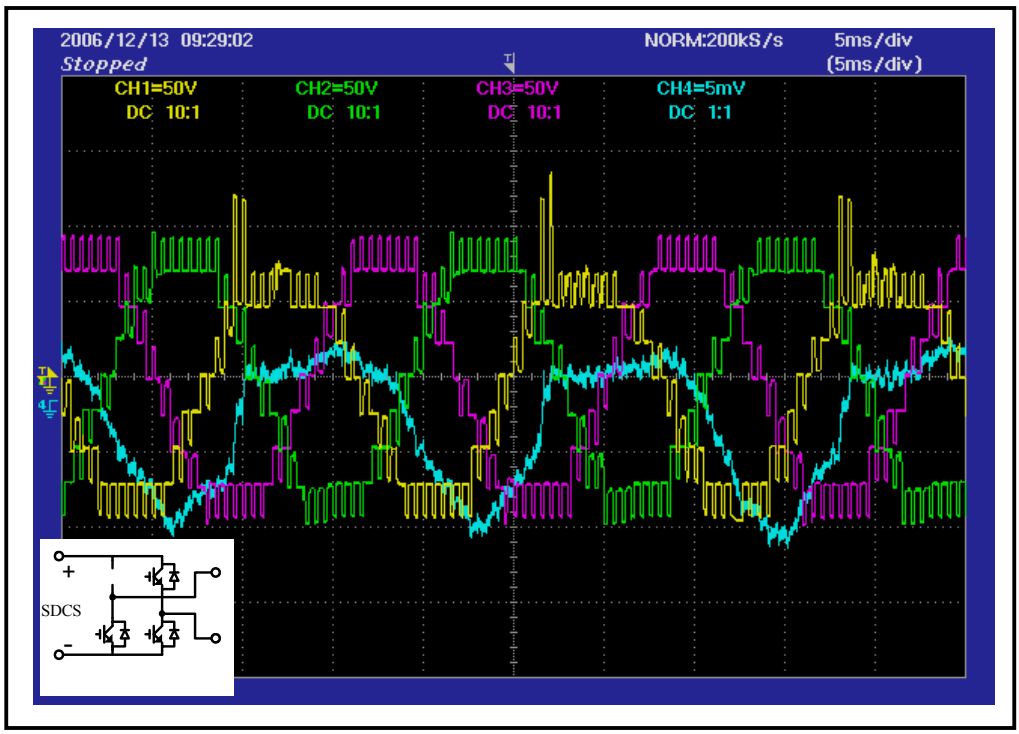


Figure 5.12. 11-level MLID operating at real open circuit fault at cell 3 switch S_{A+} with 0.8/1.0 m_a.

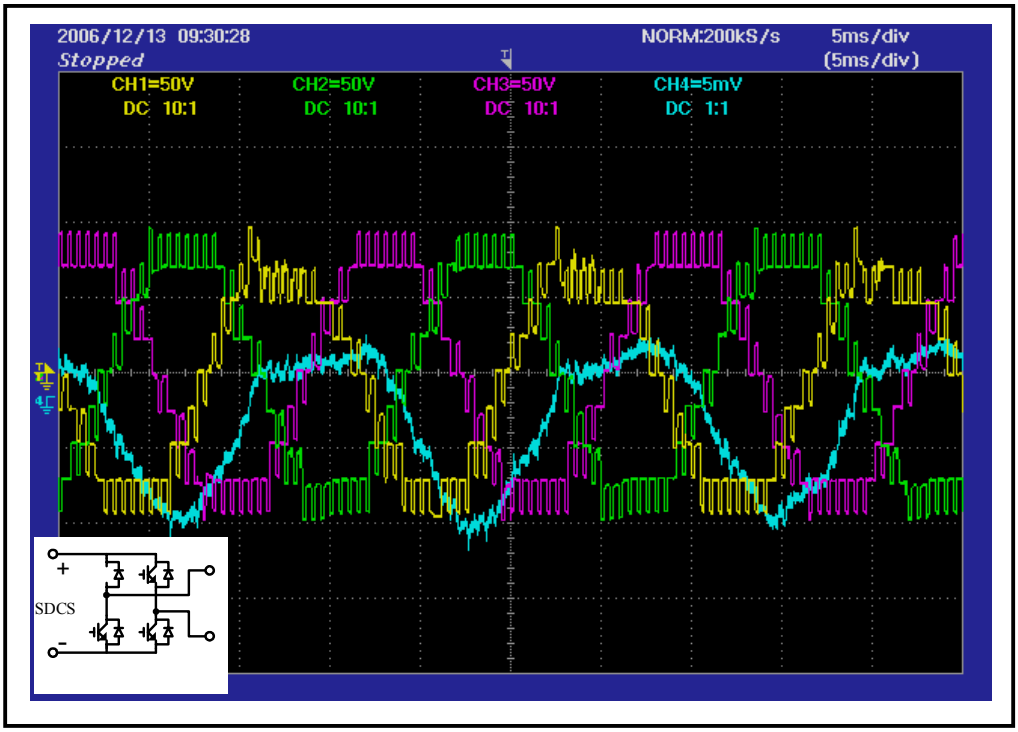


Figure 5.13. 11-level MLID operating at loss of gate drive fault at cell 3 switch S_{A+} with 0.8/1.0 m_a.

For the short circuit validation, the short circuit fault in loss of SDCS case due to fuse blown condition is also reported as shown in Figure 5.14. One can see that the fuse disconnects the faulty cell from separate dc source (SDCS). This could lead to the complexity to classify the faulty switches in the faulty cell.

The simulation is performed based on the model represented in Figure 5.7. The experiment is performed based on the diagram shown in Figure 5.8, 5.9, and 5.10. The multi-carrier based sinusoidal modulation as shown in Figure 4.2 is used.

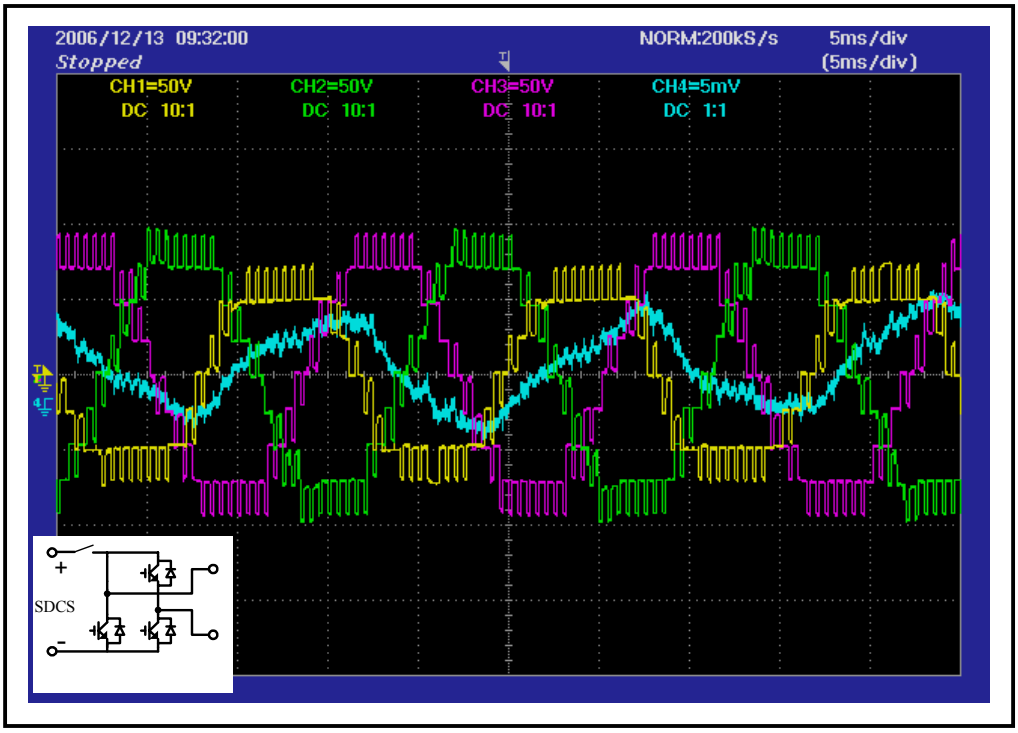


Figure 5.14. 11-level MLID operating at short circuit fault in loss of SDCS condition at cell 3 switch S_{A+} with 0.8/1.0 m_a.

5.5.1 Open circuit fault

The simulation of real open circuit fault occurrences is created by using a faulty power cell as shown in Figure 5.15. The auxiliary switches (F_1 and F_2) are normally closed type; then, the faulty cell will be simulated by disconnecting switch S_{A+} at time T commanded by a unit step from Simulink. This faulty power cell is placed at cell 2 on phase A (see Figure 5.10), and the multilevel inverter drive is operating at 0.8/1.0 modulation index before the fault occurs. In the experiment, an open circuit fault occurrence is created by physically controlling the switches in the fault creating circuit. The simulation and experiment results of an open circuit fault at cell 2 switch S_{A+} are represented in Figure 5.16 and Figure 5.17.

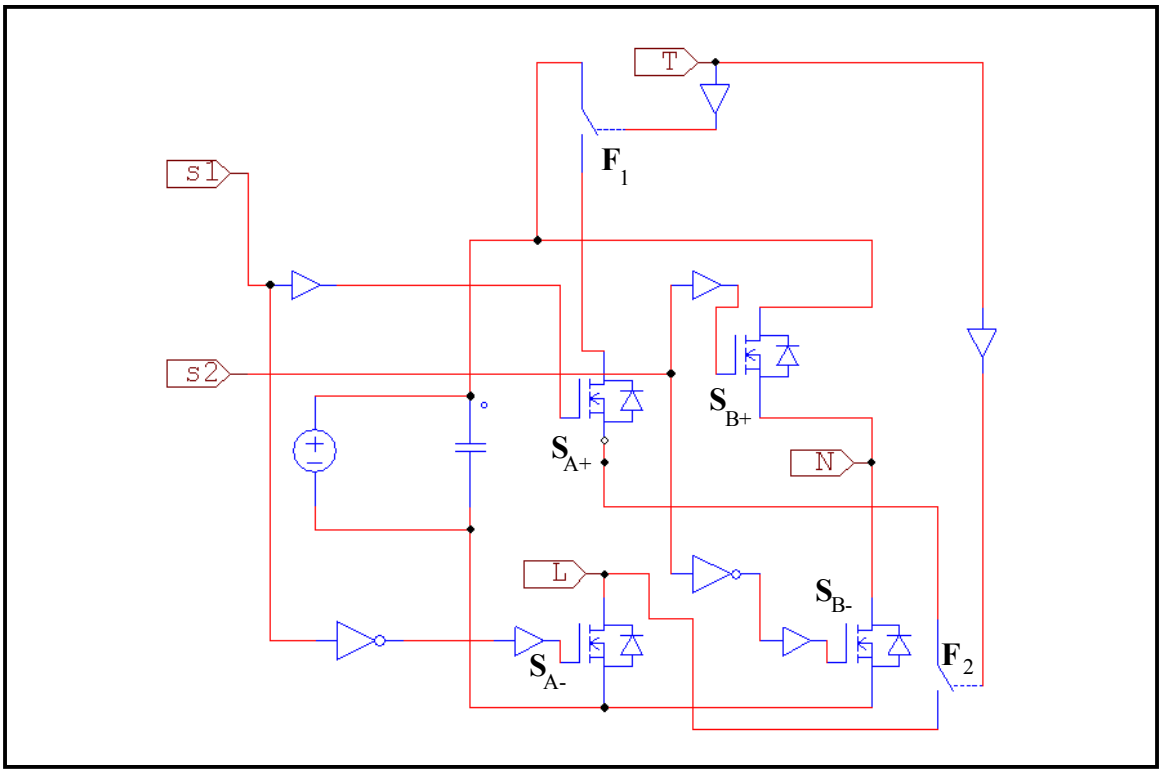


Figure 5.15. Open circuit faulty power cell at S_{A+}.

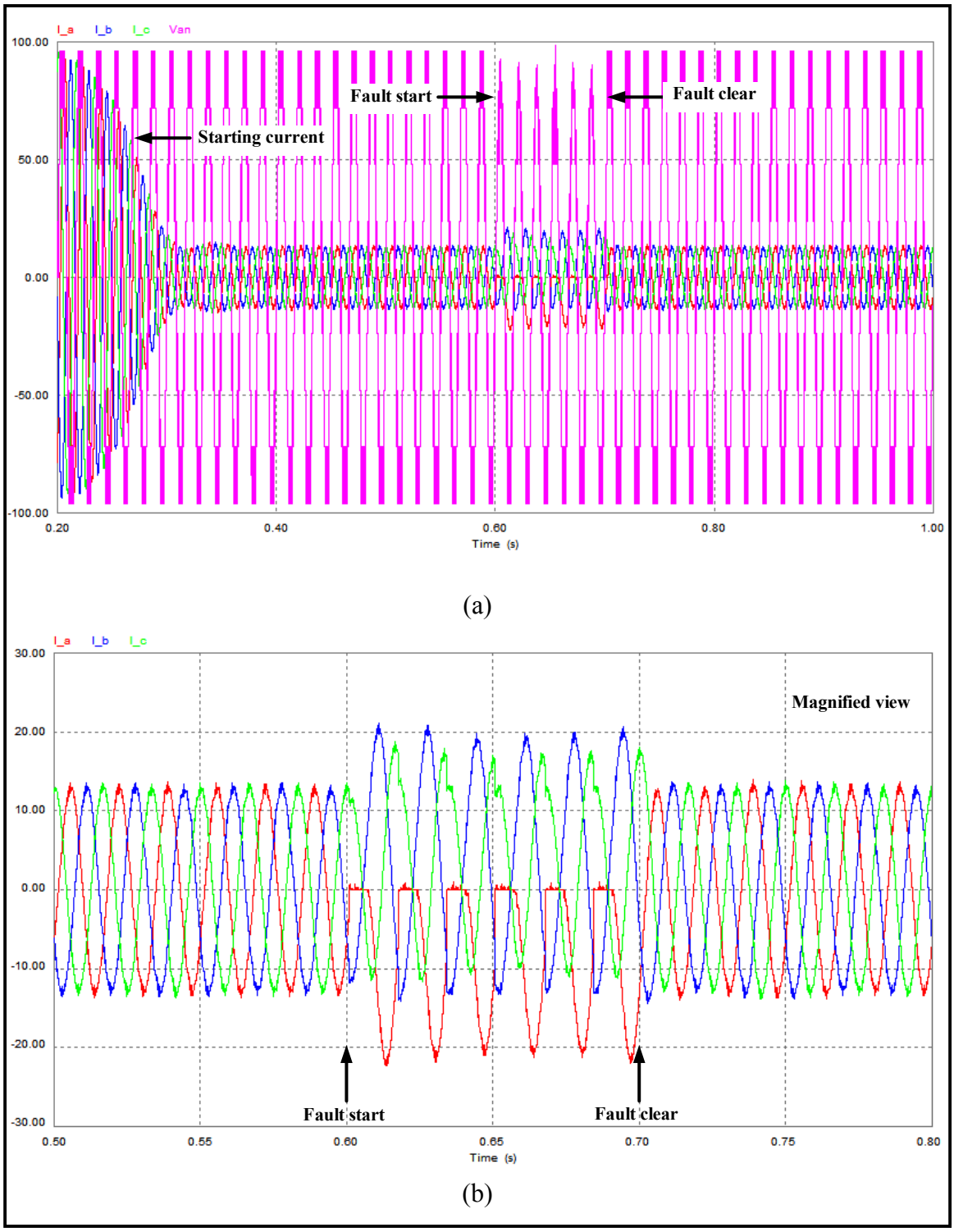


Figure 5.16. Simulation results of the open circuit fault at S_{A+}, cell 2 of the MLID during operated at m_a = 0.8/1.0 :(a) output voltage phase A, and (b) magnified view on current.

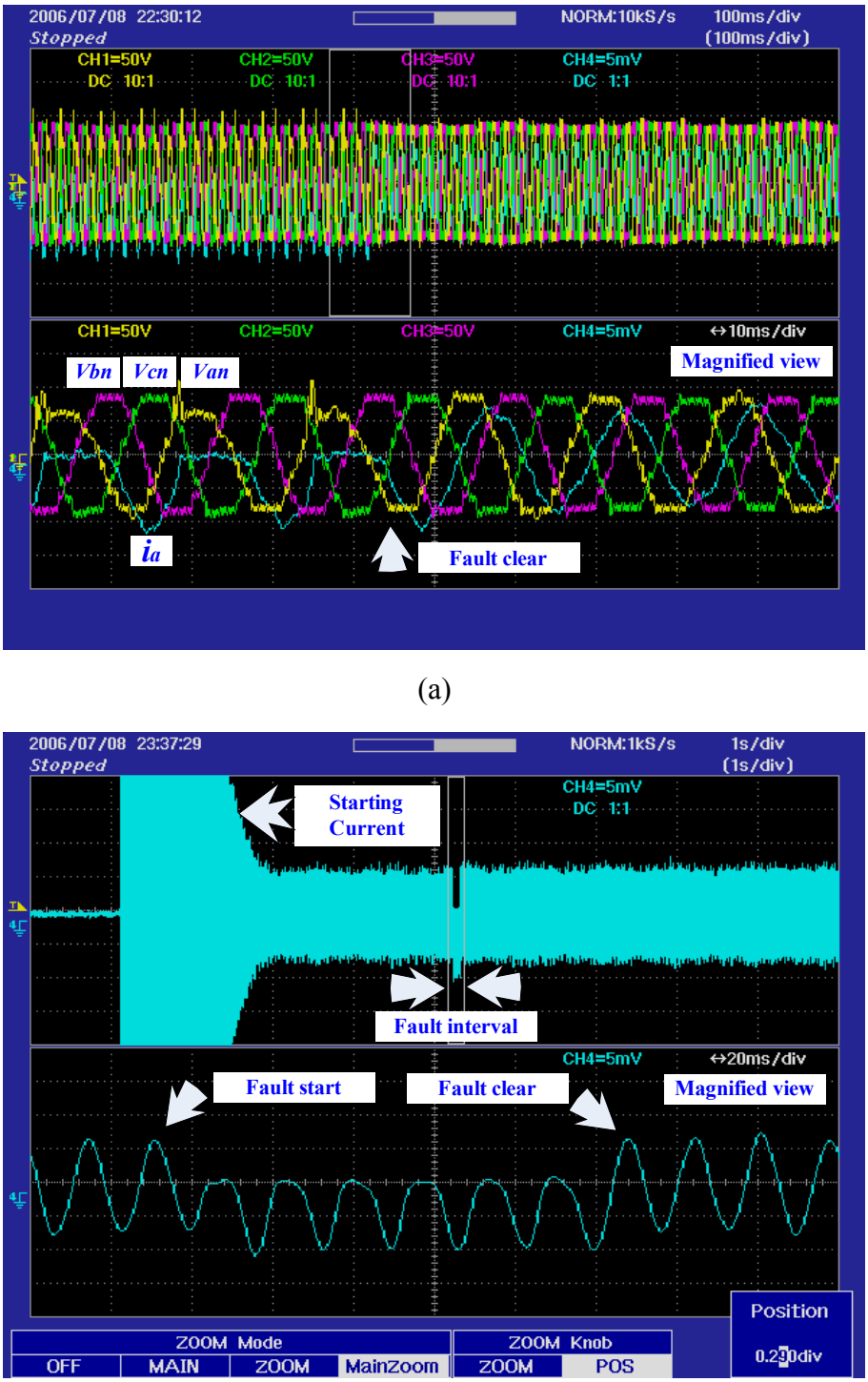


Figure 5.17. Experimental results of the open circuit fault at S_{A+}, cell 2 of the MLID at m_a = 0.8/1.0 (a) Output phase voltages and line current (i_a), (b) line current (i_a) showing starting current, fault interval, and fault clear.

As can be seen, the simulation and experiment results agree with each other. The fault diagnostic system requires about 6 cycles (~100 *ms* at 60 Hz) to clear the real open circuit fault as shown in Figure 5.16 (b) and Figure 5.17 (b). Obviously, the output voltage (V_{an}) of the MLID is unbalanced during the fault interval, and the average current on phase A (i_a) is negative polarity during the fault interval.

The open circuit fault in loss of gate drive case is also performed. Figure 5.18 shows the simulation and experiment results. Again, the simulation and experiment results also agree with each other. The proposed diagnostic and reconfiguration system also requires about 6 cycles to clear loss of gate drive faults. The results suggest that the output voltage signals of a MLID can be used as diagnostic signals to detect the open circuit faults with both real open circuit and loss of gate drive signal cases as shown in Figure 5.19.

The clearing time can be shorter than this if the proposed system is implemented as a single chip using an FPGA or DSP. The Opal-RT system needs a few cycles to load the output voltage signals from the target machine to the console PC machine via Ethernet. In addition, the window of FFT function requires at least a cycle to perform signal transformation. However, if the cascaded MLID can tolerate a few cycles of an open circuit fault, the proposed system can detect the fault and can correctly reconfigure the MLID; therefore, the results are satisfactory.

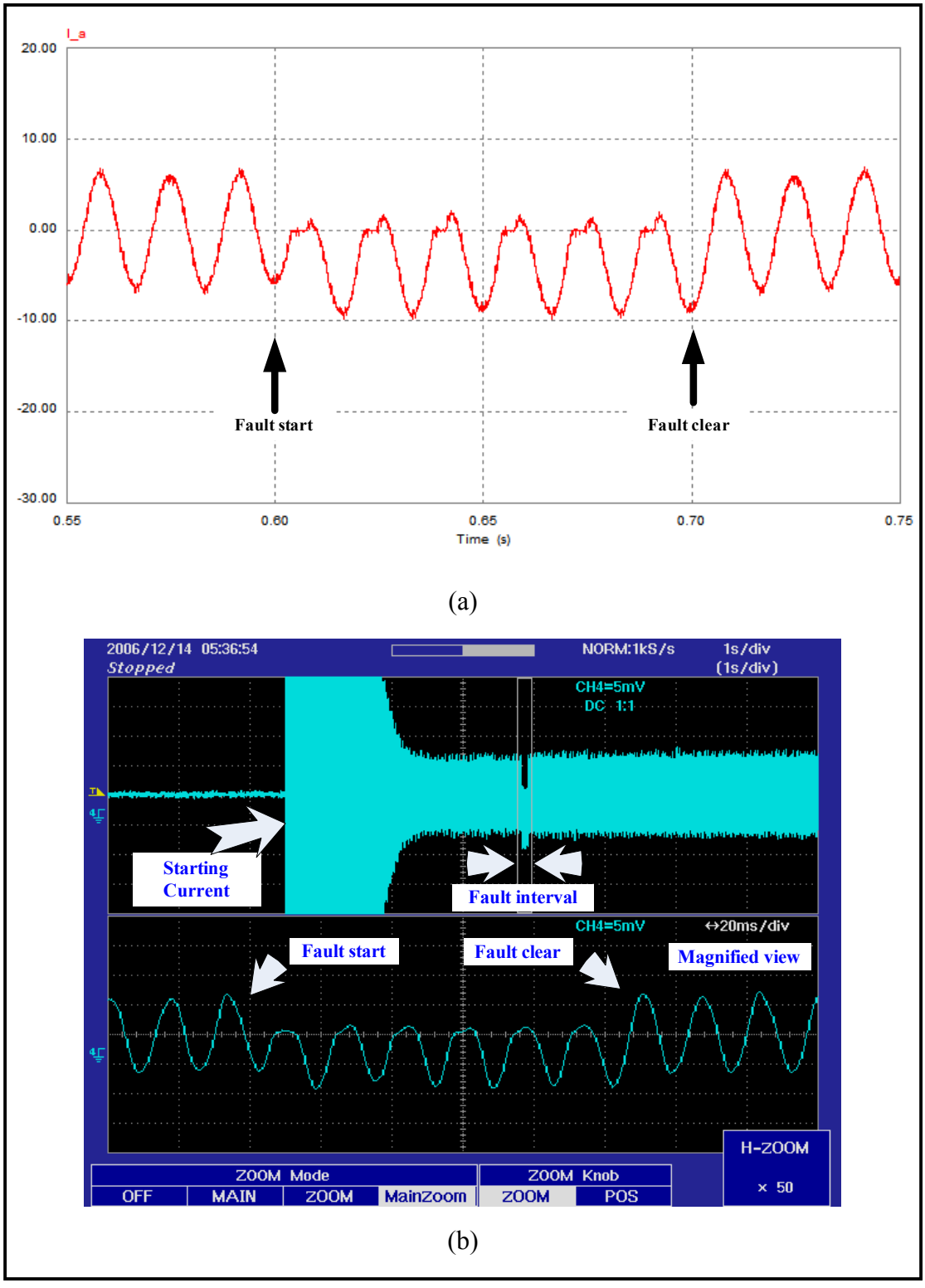


Figure 5.18. Experimental results of the loss of gate drive fault at S_{A+}, cell 2 of the MLID at m_a = 0.8/1.0 (a) Simulation result of line current (i_a), (b) Experiment result line current (i_a) showing starting current, fault interval, and fault clear.

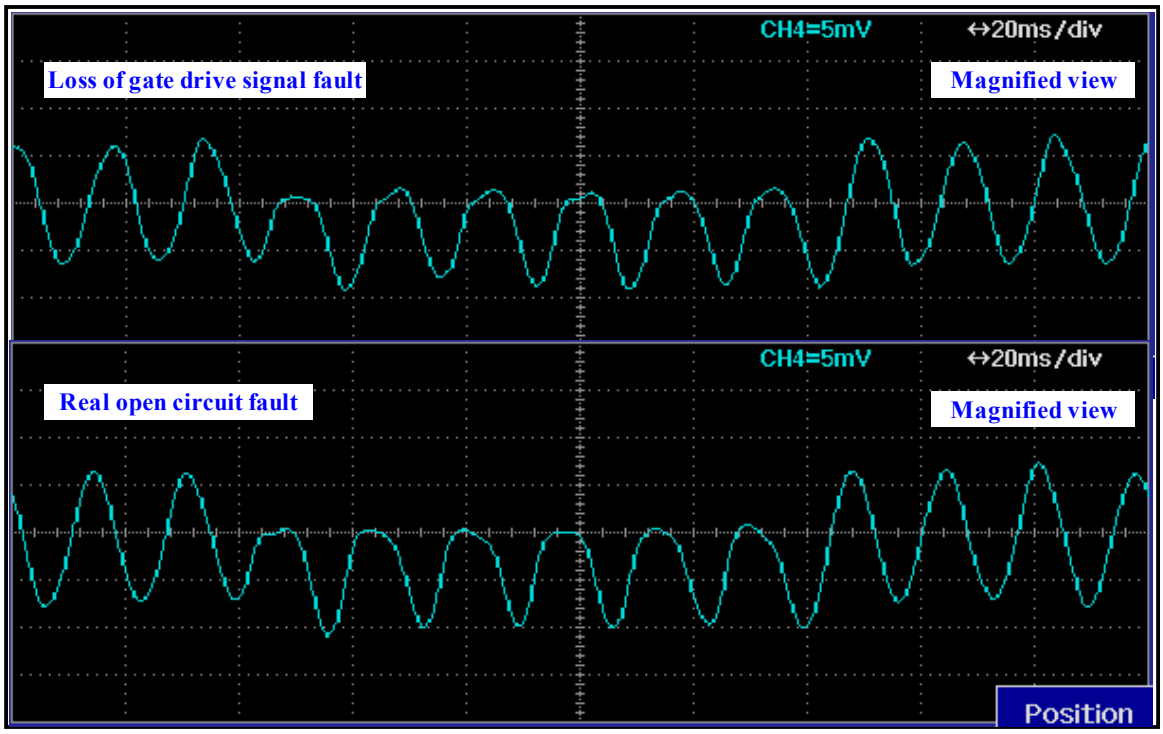


Figure 5.19. Experimental results of line current (i_a) on open circuit faults showing both loss of gate drive and real open circuit cases at S_{A+}, cell 2 of the MLID at m_a = 0.8/1.0.

5.5.2 Short circuit fault

The simulation of short circuit fault occurrences is created by using a faulty power cell as shown in Figure 5.20. The auxiliary switches are normally open type; then, the faulty cell will be simulated by closing switch F_1 at time T commanded by a unit step from Simulink. This faulty power cell is placed at power cell 3 on phase A (see Figure 5.10), and the multilevel inverter drive is operating at 0.8/1.0 modulation index before the fault occurs.

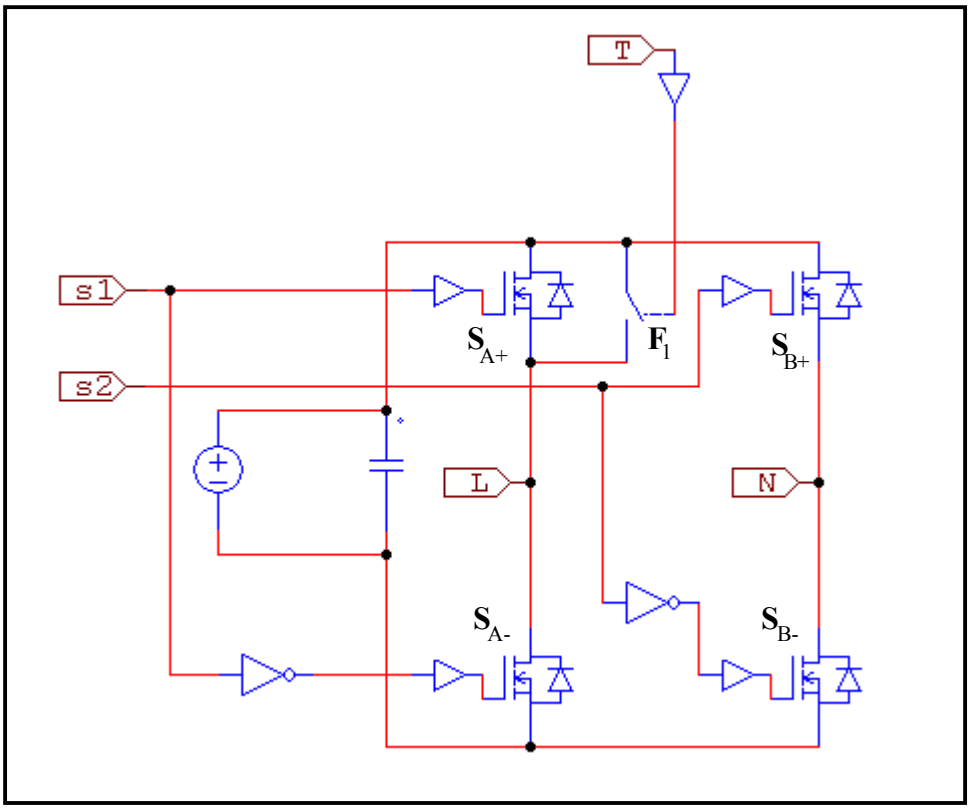


Figure 5.20. Short circuit faulty power cell at S_{A+}.

The simulation results of a short circuit fault at cell 3 switch S_{A+} are represented in Figure 5.21. The fault diagnostic system also requires about 6 cycles to clear the short circuit fault. Obviously, the output voltage (V_{an}) of the MLID is unbalanced during the fault interval (lost negative voltage at phase A), and the average current on phase A (I_a) is positive polarity during the fault interval. The peak of the fault current increases about 1.5 times compared with the normal operation. It should be noted that practically, the fuse protecting the SDCS may blow (disconnect the SDCS from a MLID) before the diagnostic system performs fault clearing so that the output phase-voltage will be zero. This behavior of output phase-voltage signals should be taken into account for training the neural network; that is why two different neural networks are used in training process.

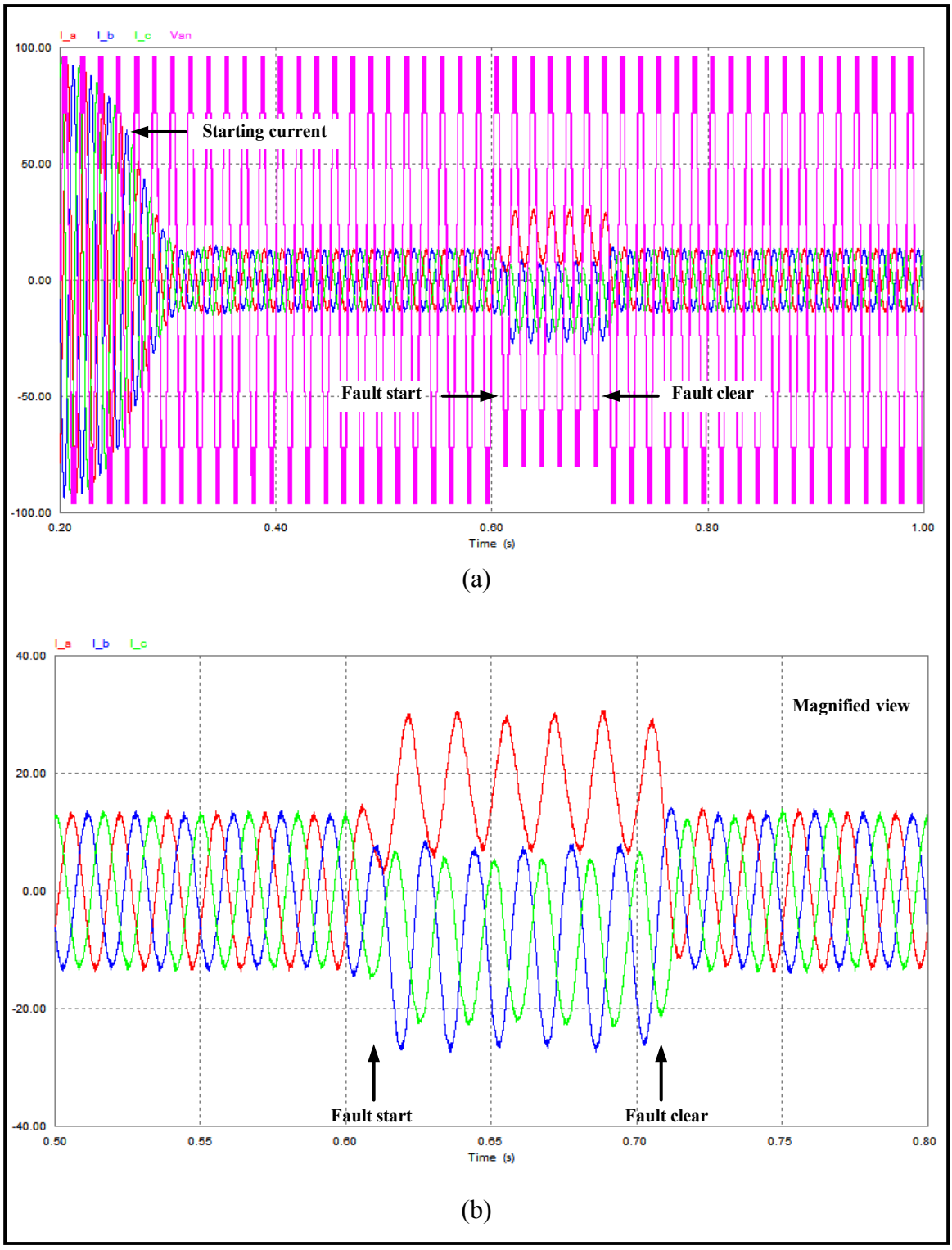


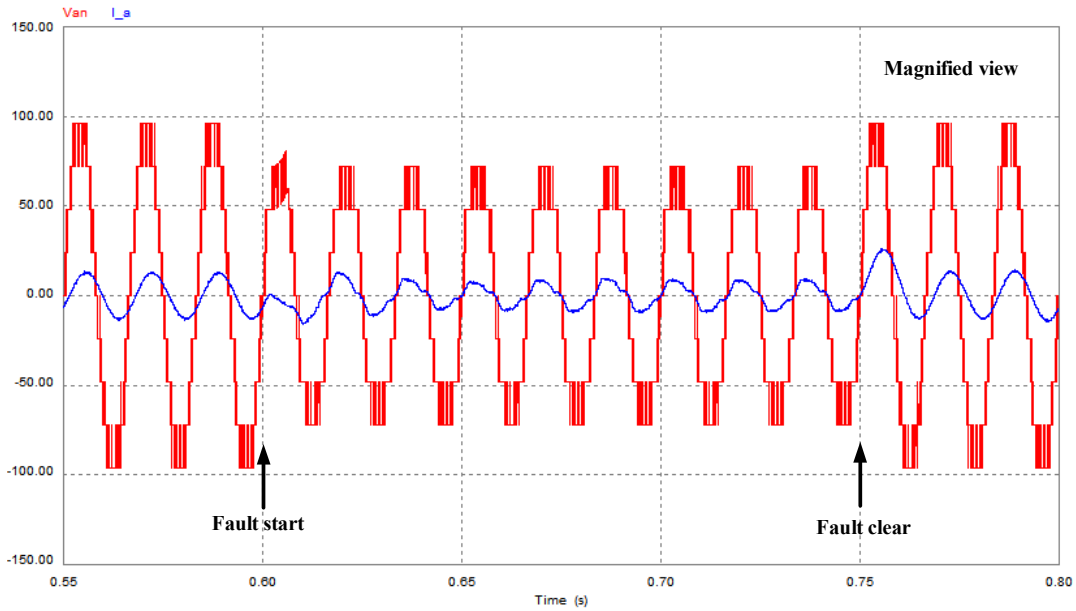
Figure 5.21. Simulation results of the short circuit fault at S_{A+}, cell 3 of the MLID operated at m_a = 0.8/1.0 :(a) output voltage phase A and (b) magnified view on current.

The proposed diagnostic system can also detect a short fault under loss of SDCS at the faulty cell condition as shown in Figure 5.22. The clearing time for this particular case is about 9 cycles. Also, the neural network can detect which cell has a fault and whether the switch was connected to the positive bus (S_{A+} and S_{B+}) or the negative bus (S_{A-} and S_{B-}). However, the neural network could not determine which specific switch (S_{A+} or S_{B+}) or (S_{A-} or S_{B-}) had failed. Nevertheless, the proposed corrective action taken would still solve this problem.

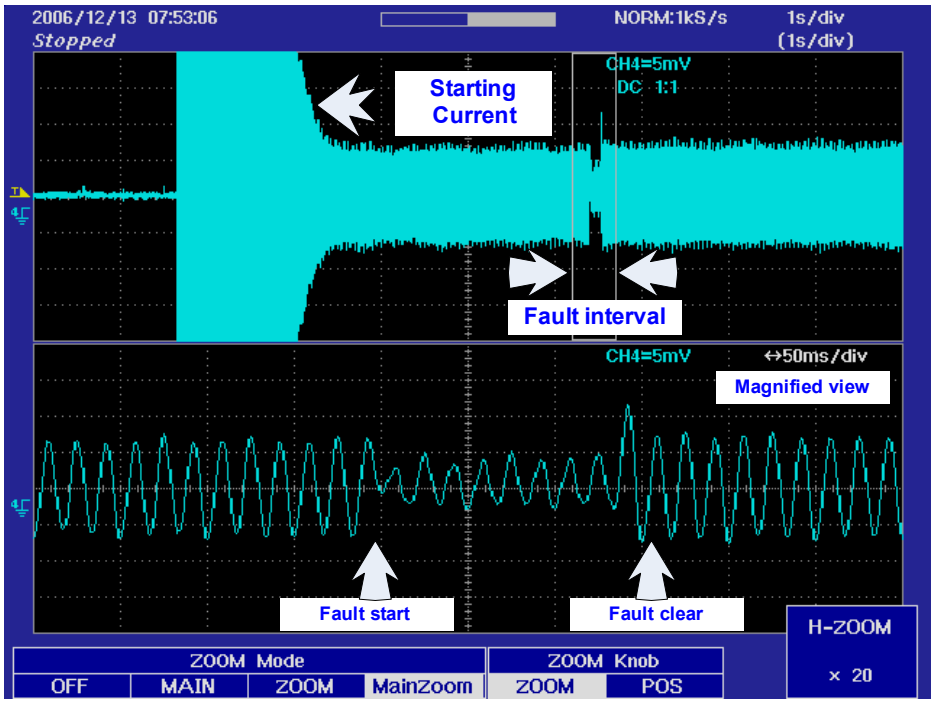
The clearing time of short circuit fault under loss of SDCS at faulty cell condition is longer than the open circuit and short circuit fault by about 3 cycles. This result suggests that using only output voltage signals in the loss of SDCS case may not adequately provide unique feature to detect the faults. Therefore, the current signals may be required to additionally train the neural network because Figure 3.4 shows that the current polarity of the faulty cell can be used to classify the faults at positive or negative dc bus.

5.6 Performance investigation

The performance investigation of the proposed diagnostic and reconfiguration system is evaluated in this section. The objective of this performance investigation is to evaluate the fault clearing times. The procedure used in particular investigation is that the MLID will operate at different load and fault conditions and each condition will be performed 5 times. Then, the average, maximum, and minimum clearing time consumed by the proposed system will be reported in tubular form.



(a)



(b)

Figure 5.22. Results of the short circuit fault at S_{A+}, cell 3 under loss of SDCS condition at the faulty cell of the MLID operated at m_a = 0.8/1.0 :(a) Simulation, (b) Experiment showing line current (i_a) at the faulty phase.

Yokogawa DL1540c digital oscilloscope is used to capture the faulty current signal by using zoom function. Resistor bank is used as a load of a dc permanent magnet generator coupled with an induction motor. The 150 MHz voltage probe of Yokogawa (Model 700998) is utilized as a voltage sensor.

Three fault types will be validated: open circuit fault at switch S_{B+} of cell 3, loss of gate drive fault at switch S_{A+} of cell 3, and short circuit at switch S_{A-} cell 2. It should be noted that a traction motor requires to keep a ratio of voltage and frequency constant (V/f) during changing fundamental frequency of voltage supply in order to maintain air gap flux of the motor constant for constant torque operation. Thereupon, four different modulation indices (m_a) and fundamental frequencies (f_1) will be investigated: 0.6/1.0 m_a at 15 Hz, 0.8/1.0 m_a at 30 Hz, 0.9/1.0 m_a at 60 Hz, and 1.0/1.0 m_a at 80 Hz. The performance validation results of the proposed diagnostic and reconfiguration system at different load conditions are illustrated in Table 5.3.

As can be seen, the proposed system can detect and reconfigure for different fault types and loads. The current waveforms of the MLID operating under several faulty conditions are illustrated in Figure 5.23 and 5.24. One can also see that the fault clearing time may not be equal in every attempt because, in some cases, the diagnostic system could not detect the fault at the first cycle required by the algorithm as explained in section 5.2. The consumed time of classification and reconfiguration algorithm can be estimated by subtracting the one cycle delay time required by FFT function. As shown in Table 5.3, the average consumed time of classification and reconfiguration is about 84 ms.

Table 5.3. Performance investigation of the proposed diagnostic and reconfiguration system.

Fault Types	*Multilevel inverter drive at different operating points*					
	Current (A)	*Modulation indices*	*Frequency*	*Fault clearing time (ms)*		
				Average of 5 attempts	*Min*	*Max*
Open circuit fault at Switch S_{B+} of Cell 3	1.56	1.0/1.0	80 Hz	95.8	87.5	112.5
	2.83	0.9/1.0	60 Hz	100	83.3	133.3
	2.26	0.8/1.0	30 Hz	117.2	100	166.6
	2.82	0.6/1.0	15 Hz	150	133.3	200
Loss of gate drive fault at Switch S_{A+} of Cell 3	1.56	1.0/1.0	80 Hz	96.25	87.5	112.5
	2.83	0.9/1.0	60 Hz	100	83.3	116.6
	2.26	0.8/1.0	30 Hz	126.7	100	166.6
	2.82	0.6/1.0	15 Hz	166.6	133.3	266.6
Short circuit at switch S_{A-} of Cell 2	1.56	1.0/1.0	80 Hz	145.8	137.5	162.5
	2.83	0.9/1.0	60 Hz	150	133.3	166.7
	2.26	0.8/1.0	30 Hz	166.7	133.3	200
	2.82	0.6/1.0	15 Hz	200	133.3	333.3

As previously mentioned in chapter 2, the voltage signal is naturally independent with load unlike using current signal; therefore, the proposed system did not have any detection problems at low frequency operation as reported in [22, 23]. Figure 5.25 shows that the current waveforms may not be useful information to detect the fault at low frequency operation. However, the current waveform could be useful in short circuit with loss of SDCS case for detecting the current polarity. The polarity of fault current can be used to determine the difference between fault S_{A+} and S_{B+} but the detection system may require more time to execute. As known, the cascaded MLID can tolerate a few cycles of faults; therefore, the detection and reconfiguration system may not need to have fast execution. It should be noted that this proposed system was implemented in Opal-RT.

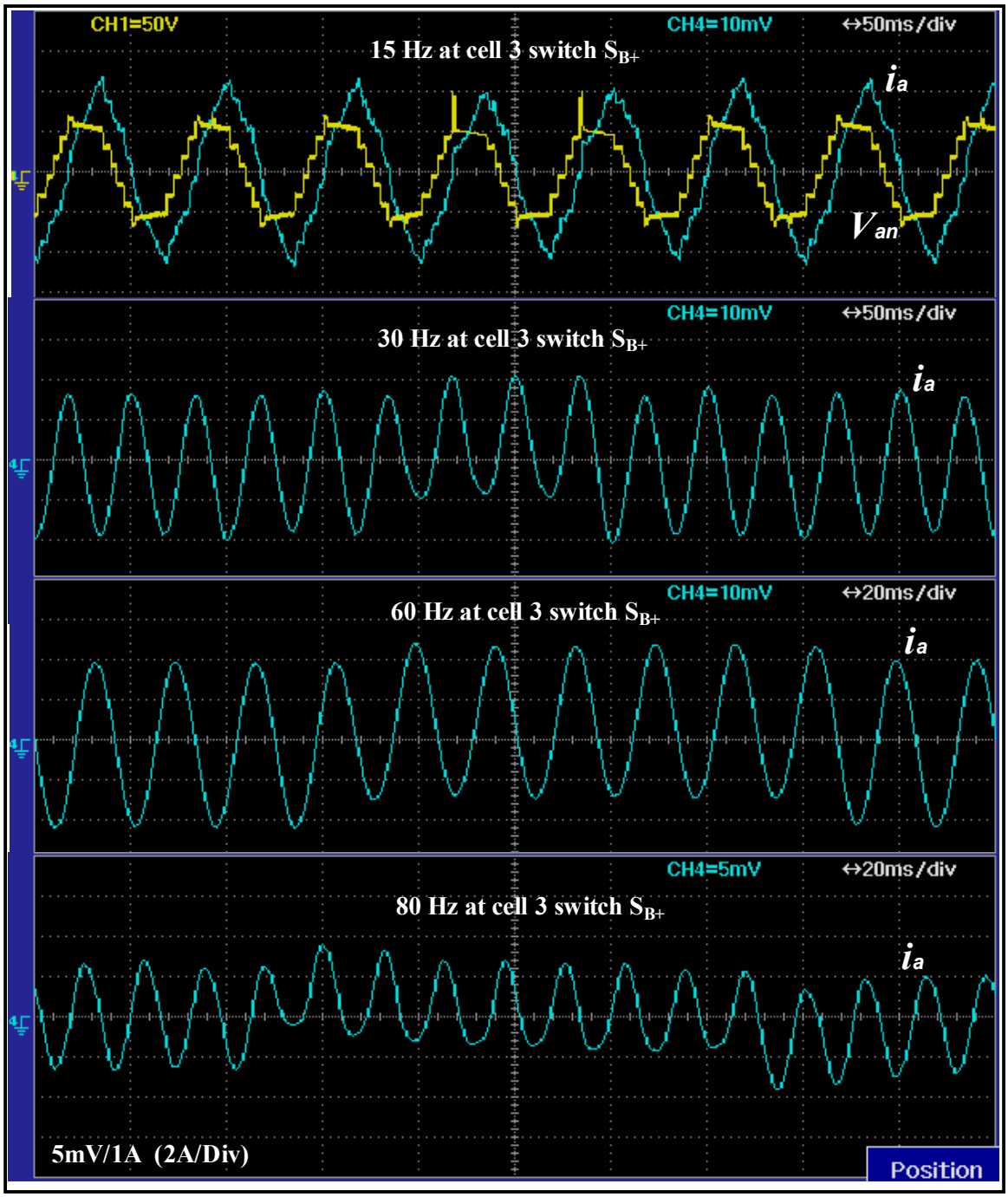


Figure 5.23. Experimental results of open circuit fault condition at different frequencies showing phase voltage (V_{an}) for 15 Hz and line current (i_a) for all frequencies.

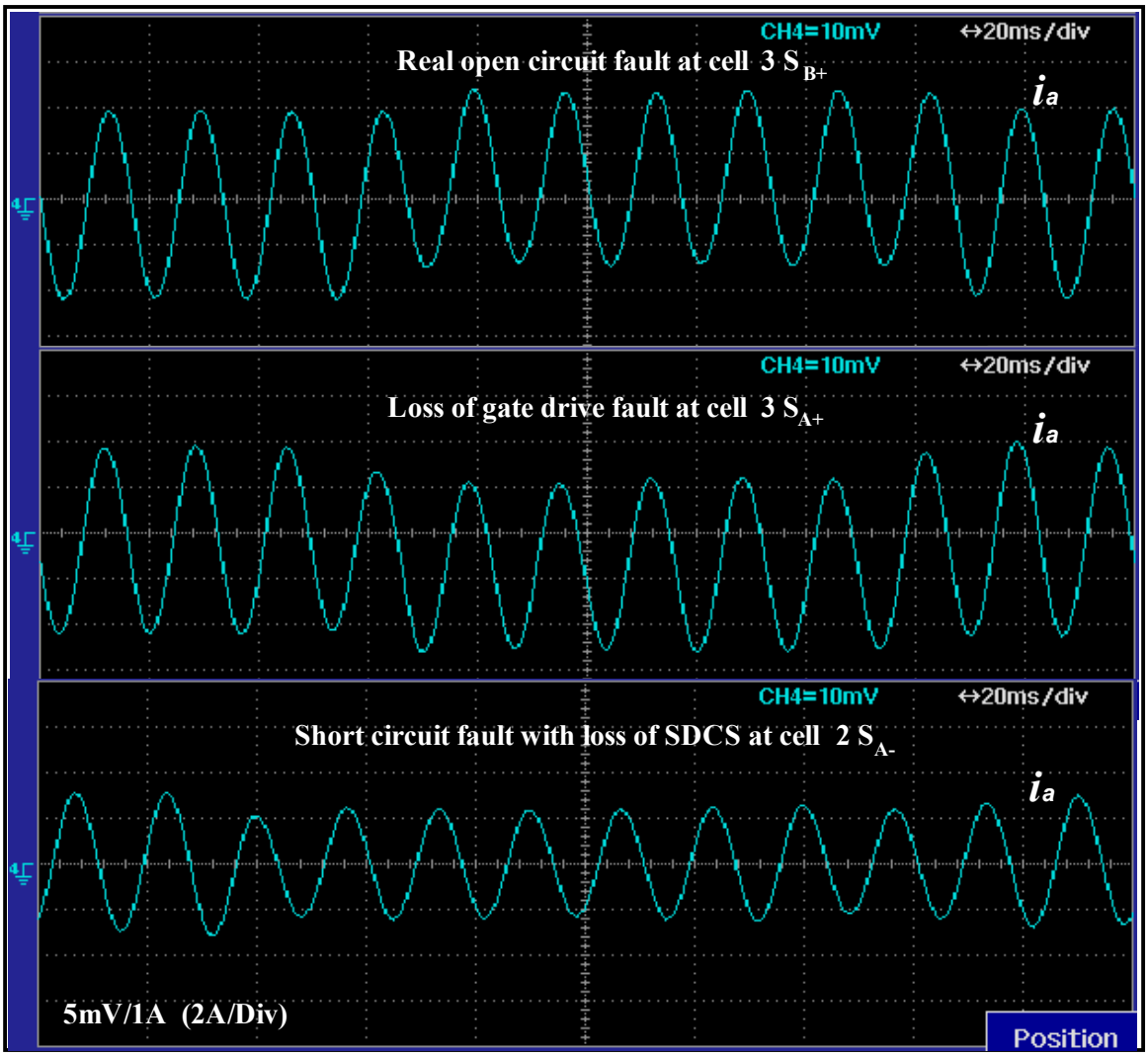


Figure 5.24. Experimental results of different fault types at 60 Hz showing line current (i_a).

(a)

(b)

Figure 5.25. Operation of the MLID at 0.6/1.0 m_a of 15 Hz: (a) normal condition and (b) open circuit fault at switch S_{A+} of cell 3.

The Opal-RT system needs a few cycles to load the output voltage signals from the target machine to the console PC machine via Ethernet. In addition, the window of FFT function requires at least a cycle to perform signal transformation. The clearing time can be shorter than this if the proposed system is implemented as a single chip using an FPGA or DSP. However, the proposed system can detect the fault and can correctly reconfigure the malfunction MLID; this shows that the proposed diagnostic and reconfiguration paradigm can be applied to MLID applications. Also, by using the proposed system, the reliability of the MLID system can be increased.

5.7 Summary

The proposed fault diagnostic paradigm has been validated in both simulation and experiment. The results show that the proposed fault diagnostic technique performs quite satisfactory. The fault diagnostic system requires about 6 cycles (~100 *ms* at 60 Hz) to clear the open circuit fault and about 9 cycles (~150 *ms* at 60 Hz) to clear short circuit fault with loss of SDCS. The experiment and simulation results in both open circuit fault and short circuit fault with loss of SDCS are in good agreement with each other.

In the short circuit fault case, the diagnostic system requires a longer time than the fuse protecting a short circuit fault at SDCS. Also, the neural network can detect which cell has a fault and whether the switch was connected to the positive bus (S_{A+} and S_{B+}) or the negative bus (S_{A-} and S_{B-}). However, the neural network could not determine which

specific switch (S_{A+} or S_{B+}) or (S_{A-} or S_{B-}) had failed. Nevertheless, the proposed corrective action taken would still solve this problem. The current signals can be used to classify the fault at S_{A+} and S_{B+} because Figure 3.4 shows that the current polarity of the faulty cell can be used to classify the faults at positive or negative dc bus

The performance validation is also performed, and the proposed system can also detect and reconfiguration with different load conditions. The average consumed time of classification and reconfiguration of algorithm is about 84 ms.

The overall clearing time can be shorter than this if the proposed system is implemented as a single chip using an FPGA or DSP. However, the proposed system can detect the fault and can correctly reconfigure the malfunction MLID; this shows that the proposed diagnostic and reconfiguration paradigm can be applied to MLID applications. Also, by using the proposed system, the reliability of the MLID system can be increased.

6. CONCLUSIONS AND RECOMMENDATIONS

6.1 Conclusions

The cascaded H-bridge multilevel inverter is one of optimistic solutions for high power drives or large traction drives. The series of H-bridges makes for modularized layout and packaging; as a result, this will enable the manufacturing process to be done more quickly and cheaply. Also, the reliability analysis reported in chapter 2 indicates that the fault-tolerance of cascaded H-bridge multilevel inverter (MLID) had the best life cycle cost and MLID using modular series-cells with separated dc sources could improve reliability if the MLID has the ability to detect and bypass the faulty cell. If one of the power cells fails, it can be bypassed and operation can continue at reduced voltage capacity. However, if a fault (open or short circuit) occurs at a semiconductor power switch in a cell, it will cause an unbalanced output voltage and current, while the traction motor is operating. The unbalanced voltage and current may result in vital damage to the traction motor if the traction motor is run in this state for a long time.

Although a cascaded MLID has the ability to tolerate a fault for some cycles, it would be better if one can detect the fault and its location; then, switching patterns and the

modulation index of other active cells of the MLID can be adjusted to maintain the operation under balanced load condition. Of course, the MLID can not be operated at full rated power. The amount of reduction of the rated power that can be tolerated depends upon the MLID application; nevertheless, in most cases a reduction of the rated power is more preferable than a complete shutdown.

It is possible that AI-based technique can be applied in condition monitoring and diagnosis. By using condition monitoring, vast savings may be made through improved maintenance procedures and policies. AI-based condition monitoring and diagnosis have several advantages; for instance, AI-based techniques do not require any mathematical models, therefore the engineering time and development time could be significantly reduced. Moreover, the reliability of the system can also improve by using diagnosis; for example, in MLID applications, several types of signals such as voltage, current, noise, vibration, temperature, and flux signals which can convey valuable information for diagnosis on the electrical and mechanical state of a MLID system including motor, multilevel inverter and controller. The voltage and/or current signals could be used to diagnose a drift of power semiconductor switches in the multilevel inverter which contains numerous semiconductor switches.

Therefore, the fault diagnostic system for cascaded H-bridge multilevel inverter based on artificial intelligent approaches incorporating a reconfiguration technique has been proposed in this dissertation. The fault diagnostic paradigm has been presented in chapter 3. The output phase voltage can be used as a diagnostic signal to detect the faults and

their locations. Also, a genetic algorithm (GA) based selective principal component (PC) neural network (NN) method can be applied to fault diagnostic system in a MLID. The GA-PC-NN performs very well with both simulation and experimental testing data set. The total classification performance is very good by about 97.5% points. Obviously, the results have shown that the PC-GA-NN has a better overall classification performance than PC-NN by about 2.5% points. Principal component analysis (PCA) conveys lower dimensional input space and reduces the time necessary to train a neural network. Also, the reduced noise may improve the mapping performance. In addition, GA offers multivariable optimized search so that the best combination of PCs or the minimum misclassification rating could be found, which leads to the improvement of total classification performance of the neural networks. Consequently, by utilizing PCA and GA, the reliability of fault diagnostic system in MILD can be improved.

The reconfiguration technique for multilevel inverters incorporating a diagnostic system based on neural network has been discussed in chapter 4. The basic principal of the reconfiguration method is to bypass the faulty cell (H-bridge); then, other available cells in the MLID are used to compensate for the faulty cell. The proposed reconfiguration technique is simple to implement because the proposed technique is based on digital logic gate; a simple AND gate and OR gate can be implemented to this reconfiguration method. In addition, the effects of using the proposed reconfiguration technique at high modulation index have been addressed.

The proposed fault diagnostic paradigm has been validated in both simulation and experiment in chapter 5. The results have shown that the proposed fault diagnostic technique performs quite satisfactory. The fault diagnostic system requires about 6 cycles (~100 *ms* at 60 Hz) to clear the open circuit fault and about 9 cycles (~150 *ms* at 60 Hz) to clear short circuit fault with loss of SDCS. The experiment and simulation results in both open circuit fault and short circuit fault with loss of SDCS are in good agreement with each other. Also, the performance validation was also performed and the proposed system can also detect and reconfigure with different load conditions. The average consumed time of classification and reconfiguration of algorithm is about 84 ms.

The overall clearing time can be shorter than this if the proposed system is implemented as a single chip using an FPGA or DSP. However, the proposed system can detect the fault and can correctly reconfigure the malfunctioning MLID; this shows that the proposed diagnostic and reconfiguration paradigm can be applied to MLID applications. Also, by using the proposed system, the reliability of the MLID system can be increased.

6.2 Contributions

This dissertation has contributed to the existing body of knowledge as follows:

- The fault diagnostic and reconfiguration system for cascaded H-bridge multilevel inverter drives based on artificial intelligent (AI) approaches by using output phase voltages ($V_{l\text{-}n}$) as diagnostic signals has been developed;
- The developed system can locate which of 60 switches in an 11-level 3-phases inverter has failed either open circuit fault or short circuit fault by using only three voltage sensors;
- The methodology of proposed diagnostic and reconfiguration system using AI-based techniques has been explained;
- The reconfiguration technique is also proposed. Also, the effects of using the proposed reconfiguration technique at high modulation index are addressed;
- Fault diagnostic processes for the 11-level MLID has been clearly explained;
- The proposed fault diagnostic and reconfiguration paradigm has been validated in both simulation and experiment and the results have illustrated that the simulation and experiment in both open circuit fault and short circuit fault with loss of SDCS are in good agreement with each other;
- The proposed diagnostic and reconfiguration paradigm can be applied to MLID applications. Also, the reliability of the MLID system can be increased by using this proposed system.

6.3 Recommendations for future work

This section contains recommendations for future investigations on fault diagnostic and reconfiguration techniques of cascaded H-bridge multilevel inverter drives.

The major disadvantage of this proposed algorithm is the fault clearing time. Therefore, research on decreasing fault clearing time would be attractive. There are two possible processes to reduce the fault clearing time: single chip implementation and feature extraction. As previously concluded, the overall clearing time can be shorter than this if the proposed system is implemented as a single chip using an FPGA or DSP. It should be noted that this proposed method was implemented in an Opal-RT system. The Opal-RT system needs a few cycles to load the output voltage signals from the target machine to the console PC machine. Also, the window of FFT function requires at least a cycle to perform signal transformation so that the proposed system requires longer clearing time at low frequency operation. Recursive DFT [21] and short FFT [46] or feature extraction in time domain [25] may be used; however, some fast transformation methods may be performed under hypotheses such as the MLID is running at balanced load condition and/or the signal is even/odd quarter waveforms. It should be mentioned that diagnostic signals of fault occurrences may not be possible under these hypotheses.

The results on short circuit fault case have shown that the current waveforms may be useful for additional diagnostic signals. The polarity of faulty current can be used to determine the difference between faulty switch in positive or negative bus. A possible

technique for tracking the current polarity is Schmitt-trigger as studied in [23]. The reason to use an external circuit is to reduce training time and complexity of the classification problem of a neural network. With an external circuit, the training time and complexity of the neural network would be decreased because the classification process requires detecting only a faulty power cell; then the positive and negative switch can be determined using the Schmitt-trigger circuit.

The proposed diagnostic and reconfiguration method can be extended to other multilevel inverter applications such as static synchronous compensator (STACOM). The proposed topology utilizes the output voltage signals to diagnose the faults; therefore, the proposed method is independent with loads. It should be noted that this method requires only three voltage sensors.

Other neural network architectures and training paradigms can also be applied in fault diagnostic applications. A radial basis function (RBF) neural network is also possible to use in the applications. An RBF network constructs a local approximation to non-linear input/output mapping, whereas a multilayer feedforward perceptron (MLP) neural network is a global approximation. This may result in fast learning and reduced sensitivity to the order of presentation of the input data.

It is also optimistic that the proposed method can be implemented in a power switch module with a single chip. Recently, International Rectifier (IR) introduces the integrated control circuit based on DSP and power module for embedded motion control

(IRMCT3UF1) [61]. This power module allows the users to interface with the DSP via RS232; therefore, the users can import/setup their own parameters and control techniques based on embedded Simulink toolbox. It is possible that the proposed fault diagnostic and reconfiguration algorithm can be implemented based on this power module technology; as a result, the reliability of multilevel inverter applications can be increased.

6.4 Publications

Parts of this dissertation have been published as follows:

- **S. Khomfoi**, L. M. Tolbert**,** "Fault Diagnostic System for a Multilevel Inverter Using a Neural Network," *IEEE Transactions on Power Electronics*, vol. 22, May, 2007 (accepted - in press);
- **S. Khomfoi**, L. M. Tolbert, "Multilevel Power Converters," *Power Electronics Handbook*, 2nd Edition, Elsevier, 2007, ISBN 978-0-12-088479-7, Chapter 17, pp. 451-482.
- **S. Khomfoi**, L. M. Tolbert, "Fault Diagnosis System for a Multilevel Inverter Using a Neural Network," *IEEE Industrial Electronics Conference,* November 6-10, 2005, pp. 1455-1460;
- **S. Khomfoi**, L. M. Tolbert, "Fault Diagnosis System for a Multilevel Inverters Using a Principal Component Neural Network," *37th IEEE Power Electronic Specialists Conference,* June 18-22, 2006, pp. 3121-3127;

- **S. Khomfoi**, L. M. Tolbert, "A Reconfiguration Technique for Multilevel Inverters Incorporating a Diagnostic System Based on Neural Network," *10th IEEE Workshop on Computers in Power Electronics,* July 16-19, 2006, pp. 317-323;
- **S. Khomfoi**, L. M. Tolbert, "A Diagnostic Technique for Multilevel Inverters Based on a Genetic-Algorithm to Select a Principal Component Neural Network," *IEEE Applied Power Electronics Conference,* February 25 - March 1, 2007, Anaheim, California, pp. 1497-1503;
- **S. Khomfoi**, L. M. Tolbert, B. Ozpineci, "Operation under Faulty Condition of Cascaded H-bridge Multilevel Inverter Drives Including AI-Based Fault Diagnosis and Reconfiguration," *IEEE International Electric Machines and Drives Conference*, May 3-5, 2007, Antalya, Turkey.

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