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System-on-Package Low-Power Telemetry and Signal Conditioning unit for Biomedical Applications

Mohammad Rafiqul Haider
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To the Graduate Council:

I am submitting herewith a dissertation written by Mohammad Rafiqul Haider entitled "System-on-Package Low-Power Telemetry and Signal Conditioning unit for Biomedical Applications." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

Syed K. Islam, Mohamed R. Mahfouz, Major Professor

We have read this dissertation and recommend its acceptance:

Benjamin J. Blalock, Ethan D. Farquhar

Accepted for the Council:
Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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A Dissertation
Presented for the
Doctor of Philosophy Degree

The University of Tennessee, Knoxville

Mohammad Rafiqul Haider
December 2008

Dedication

This dissertation is dedicated to my mother and to my wife.

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I am expressing my greatest thanks to my major advisor Dr. Syed K. Islam for all the support and encouragement he has given me throughout my Ph. D. program. I would also like to thank the co-chair of my committee Dr. Mohamed R. Mahfouz from Mechanical Aerospace and Biomedical Engineering (MABE) for supporting me throughout my graduate studies. Special thanks to Dr. Benjamin J. Blalock and Dr. Ethan D. Farquhar for serving on my committee and critically reviewing my work.

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Abstract

Recent advancements in healthcare monitoring equipments and wireless communication technologies have led to the integration of specialized medical technology with the pervasive wireless networks. Intensive research has been focused on the development of medical wireless networks (MWN) for telemedicine and smart home care services. Wireless technology also shows potential promises in surgical applications. Unlike conventional surgery, an expert surgeon can perform the surgery from a remote location using robot manipulators and monitor the status of the real surgery through wireless communication link. To provide this service each surgical tool must be facilitated with smart electronics to accrue data and transmit the data successfully to the monitoring unit through wireless network.

To avoid unwieldy wires between the smart surgical tool and monitoring units and to reap the benefit of excellent features of wireless technology, each smart surgical tool must incorporate a low-power wireless transmitter. Low-power transmitter with high efficiency is essential for short range wireless communication. Unlike conventional transmitters used for cellular communication, injection-locked transmitter shows greater promises in short range wireless communication. The core block of an injection-locked transmitter is an injection-locked oscillator. Therefore, this research work is directed towards the development of a low-voltage low-power injection-locked oscillator which will facilitate the development of a low-power injection-locked transmitter for MWN applications.

Structure of oscillator and types of injection are two crucial design criteria for low-power injection-locked oscillator design. Compared to other injection structures, body-level injection offers low-voltage and low-power operation. Again, conventional NMOS/PMOS-only cross-coupled LC oscillator can work with low supply voltage but the power consumption is relatively high. To overcome this problem, a self-cascode LC oscillator structure has been used which provides both low-voltage and low-power operation. Body terminal coupling is used with this structure to achieve injection-locking. Simulation results show that the self-cascode structure consumes much less power compared to that of the conventional structure for the same output swing while exhibiting better phase noise performance. Usage of PMOS devices and body bias control not only reduces the flicker noise and power consumption but also eliminates the requirements of expensive fabrication process for body terminal access.

Table of Contents

List of Tables

List of Figures

Chapter 1 Introduction

1.1 Introduction

Recent technological improvements of healthcare monitoring equipments, micro- and nano- fabrication processes and wireless communication technologies have led to the developments of miniature, light-weight, and energy-efficient circuit solutions for biomedical sensor applications. The silicon-based micro-fabrication and microelectromechanical (MEMS) techniques have been successfully applied for the fabrication of a large range of miniature biomedical sensors. Ubiquitous growth of wireless sensor networks has opened up a new and innovative application of wireless technology in medical as well as in healthcare field. This trend has just been started and it is expected that wireless networks are going to become an integral part of medical solutions due to their benefits in reducing healthcare costs and increasing accessibility for the patients as well as the healthcare professionals. This perspective has given birth to a new sensor network that is called Wireless Body Sensor Network (WBSN) or Wireless Body Area Network (WBAN). In near future, this WBAN will co-exist with the installed infrastructure, help augmenting data collection and provide real-time response among patients and healthcare providers. Examples of areas in which future medical systems can be benefited the most from wireless sensor networks are in-home assistance, smart homecare, and patient monitoring in emergency unit after physical rehabilitation.

Fig 1.1 shows a broad range of applications of wireless networks in medical field. Wireless technology provides an efficient tool for providing instant access to patient data, lab results, clinical histories, insurance information, etc. so that immediate healthcare is ensured in case of emergency eliminating the dependence on the sketchy clinical decision or wasteful medical duplications. Wireless technology can also improve the efficiency of the hospital staffs in different sectors ranging from patient database monitoring to hospital inventory management. A hospital staff can monitor the patient database in the hospital or mange the hospital inventory within a very short time by using radio frequency identification (RFID) network. RFID network can also help to identify the location of a physician or a patient within the hospital premises in case of special need or situation. A surgeon or a physician can inspect the status of a telesurgery or monitor the vital signs of patients using wireless personal area network (WPAN), respectively and can provide valuable feedback in case of emergency situation. A nurse in a hospital can take-care of a patient efficiently and in a real time manner by observing vital signs of the patients through WBAN and WPAN. Again, in case of any unknown abnormal symptoms patient data could be sent to a specialist for diagnosis and future medical treatments. This is not the end. Wireless technology helps extending the healthcare up to a patient home by using the concept of telemedicine or smart-home-care.

Telemedicine is a new concept where a patient staying in home can even be monitored by using smart medical devices and WBAN. In this case, various types of implantable or transdermal sensors are placed within the vicinity of human body. They continuously monitor various physiological parameters and send the signal to a near-by hub station

(see Fig 1.2). This hub could be either a cell phone or personal digital assistant (PDA). Then using the existing secure communication technologies, the sensor signals are transmitted to a doctor, nurse or healthcare provider. Based on the sensor signals coming from the patient, the physician or healthcare provider can initiate necessary action for instance, artificial dose control in emergency situation. This WBAN and telemedicine platform could also be configured for object location, medicine reminder or emergency alert in case of any sign of fatal disease.

Telesurgery is another promising concept of combining existing medical and communication technologies on the same platform. Here a patient stays far away from an expert surgeon and the surgeon's activities are impersonated by robot manipulators. The surgeon controls the robot manipulators from a remote location and the link between the surgeon and the robot manipulators is maintained by the existing matured communication technology. As reported in Nature Journal, the first telesurgery was performed on September 19, 2001 when the surgeons from New York, USA, accomplished a gallbladder surgery in Strasbourg, France, using a three-arm robot manipulator as shown in Fig 1.3. The trans-Atlantic fiber-optic link was used to maintain the reliable communication between New York, USA and Strasbourg, France. There was a time delay between the initiation of an action and the real operation but still the operation was successful.

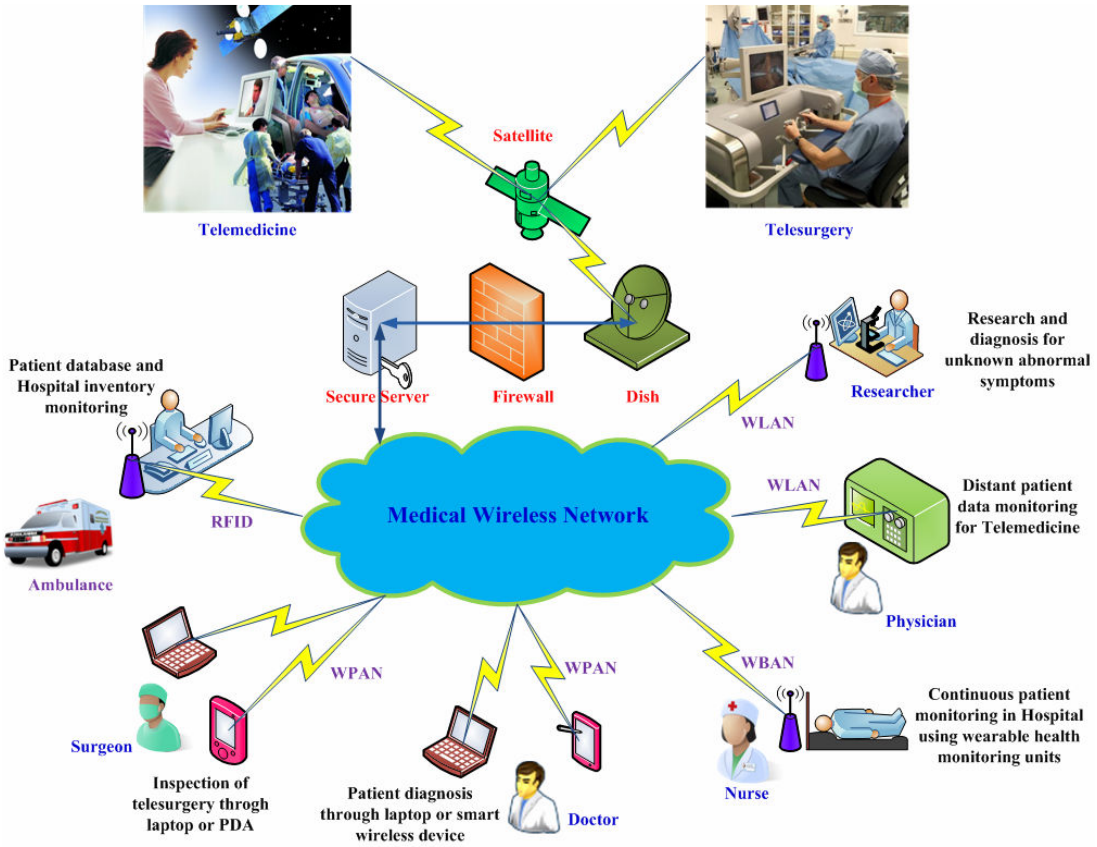


Fig 1.1: Applications of wireless networks in medical field

Fig 1.2: Conceptual WBAN and telemedicine (picture source: www.medapps.net)

Fig 1.3: First telesurgery using trans-Atlantic fiber-optic link

1.2 Sensor Networks for Medical Applications

Various types of wireless networks have been investigated in the past and in the recent years for health care applications. In this section a short description of different wireless networks used for medical applications will be discussed.

1.2.1 Wireless Body Area Network

Prolific growths of micro-sensors, integrated circuit technologies and wireless networks have introduced the necessity of low-power sensor platforms that can be integrated in wireless body area network (WBAN). The low power requirement of these networks has made them best suited for integration into wearable health monitoring units (WHMU) [1]. WHMU are usually incorporated with various types of implantable or transdermal sensors to measure various physiological parameters such as ECG, blood pressure, blood glucose level, motion/tilt, etc [2]. WBAN can be used inside a hospital to monitor patients in critical conditions. This can also be used in 'smart homecare' for data augmentation and transmission over the Internet to doctors, nurses or healthcare providers in real time.

1.2.2 Radio Frequency Identification

Radio frequency identification (RFID) technology has a wide variety of applications such as goods logistics, pet and human identification, healthcare and others. [3]. Hospital staffs can efficiently monitor the hospital inventory with the help of RFID tags. These tags can also be used to identify the location of a patient or a physician within the hospital premises and they can be recalled in emergency situation.

1.2.3 Wireless Personal Area Network

Wireless Personal Area Networks (WPAN) [4-6] using IEEE 802.15.4 or Bluetooth have potential uses in the medical fields. WPAN is used for short distance communication and hence these networks can be used to monitor patients in real time by a nurse without frequent visit to patient's room. This certainly helps to improve the monitoring performance and work efficiency of hospital staffs. WPAN can also be used for transferring data among multiple expensive and large devices within the hospital with minimum time overhead.

1.2.4 Sensor Networks

Unobtrusive access to health information is made possible by combining sensor network technologies such as Zigbee [4] with WBAN [7]. This combination forms smaller scale networks that can be easily placed on human clothing. A good example of an application

of sensor networks in the medical field is the CodeBlue project [1] being developed at Harvard University. Other experimental applications include forest fire detection and path tracking using ad hoc sensor networks [8]. Due to the low-cost and low-power consumption of the sensor network devices, they can be easily deployed ubiquitously. Some of the wireless sensor network devices use their own operating system called the TinyOS. Therefore they can be programmed over the air, making their management very easy.

1.2.5 GPRS/UMTS

GPRS and UMTS wireless technologies have also found their uses in the area of medical applications. An application called 'MobiHealth' has been designed by using WBAN with GPRS/UMTS for Internet connectivity.

1.2.6 Wireless LAN (IEEE 802.11)

Now-a-days wireless local area network (WLAN) access is present in most of the hospitals, universities and corporate offices. Some of the benefits of this technology is used for medical applications. In 'Telemedicine' WLAN in association with WBAN is used to monitor the vital signs of a remote patient. Patient's data transfer within the hospital or communication among different medical devices is also made possible using this wireless network.

1.3 Research Motivation

In telesurgery, a distant surgeon is entirely dependent upon the performance of advanced image vision, integrated electronics embedded in the surgical tools and the accuracy of robot manipulators. Surgical tools with embedded electronics play a vital role in the telesurgery to send valuable information on the status of the surgery. Surgical tools must provide vital information on the surgery such as the sensation of touch, the depth of a cut, the position of an organ, etc. Different surgical tools are used for different types of surgery, for example a spacer block is used for artificial knee joint implantation.

To be benefited with the concept of telesurgery, each surgical tool needs to be facilitated with smart electronics to accrue data and transmit the data successfully to the remote monitoring unit through wireless network. A research attempt has been undertaken by the Center for Musculoskeletal Research (CMR) group at the University of Tennessee to develop a system-on-package smart spacer block to help the surgeons during the artificial knee implant surgery. In the next section the system-on-package smart spacer block has been discussed which is going to incorporate sensors and embedded electronics for data acquisition and a low-power wireless transmitter for successful transmission of data to different monitoring units either directly or through a hub station such as cell phone or PDA.

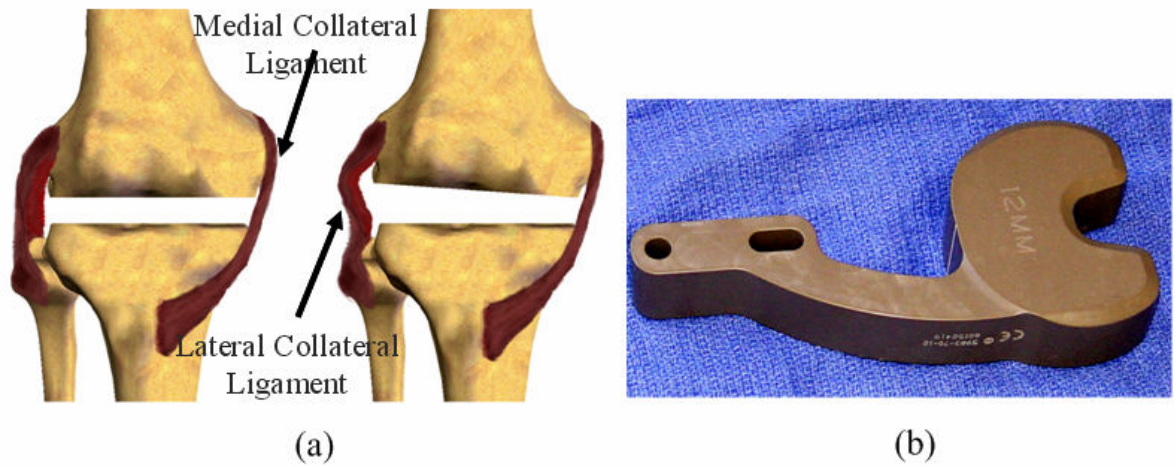


Fig 1.4: (a) Bone ligaments and alignment (b) Conventional spacer block

1.3.1 System-on-Package (SOP) Smart Spacer Block

In artificial knee joint implantation, surgeons perform the resection based on the information from certain surgical tools such as spacer block, tensioner and tram adapter.

In total knee arthoplasty (TKA), now-a-days surgeons use minimum invasive surgery (MIS) where only 3-4″ incision is made compared to 8-10″ incision in the conventional one. During the MIS, the conventional spacer block (Fig 1.4 (b)) provides a qualitative idea about the gap shape, tightness of the ligament, etc. (Fig 1.4 (a)). To quantify this information, a smart spacer block is needed where both the sensors and the embedded electronics reside in a single unit (see Fig 1.5). In the smart spacer block, various types of pressure sensors are mounted on the top layer whereas all the electronics for sensor signal processing is placed in the intermediate layers. The entire system needs to be a system-on-package (SOP) implementation that facilitates the surgeon with greater flexibility and better performance. Fig 1.6 shows the functional block diagram of the SOP smart spacer block.

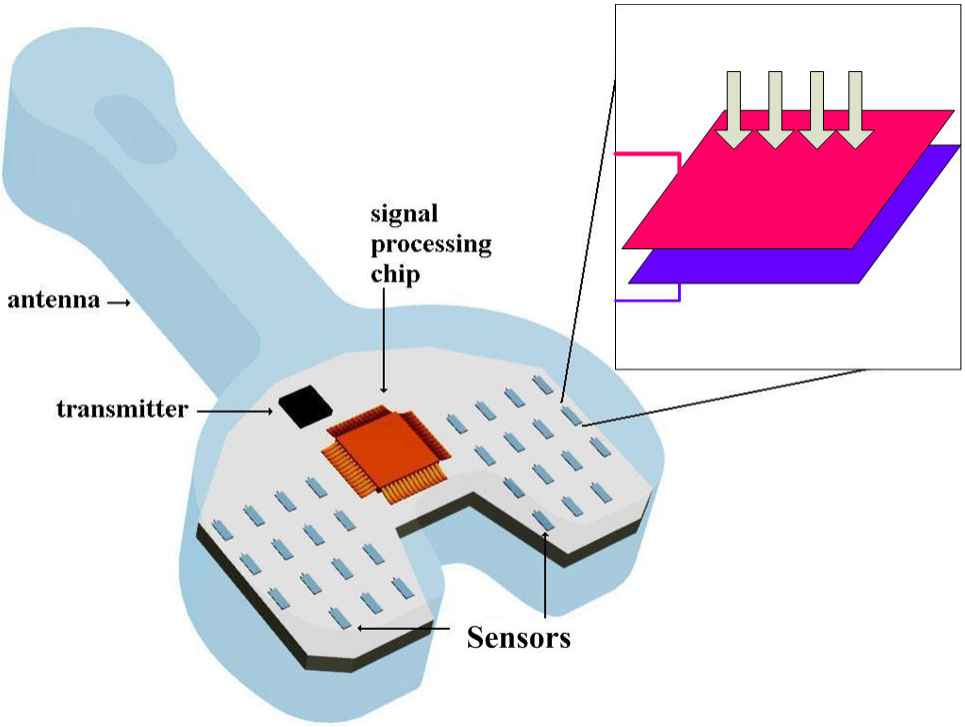


Fig 1.5: System-on-package (SOP) smart spacer block [9]

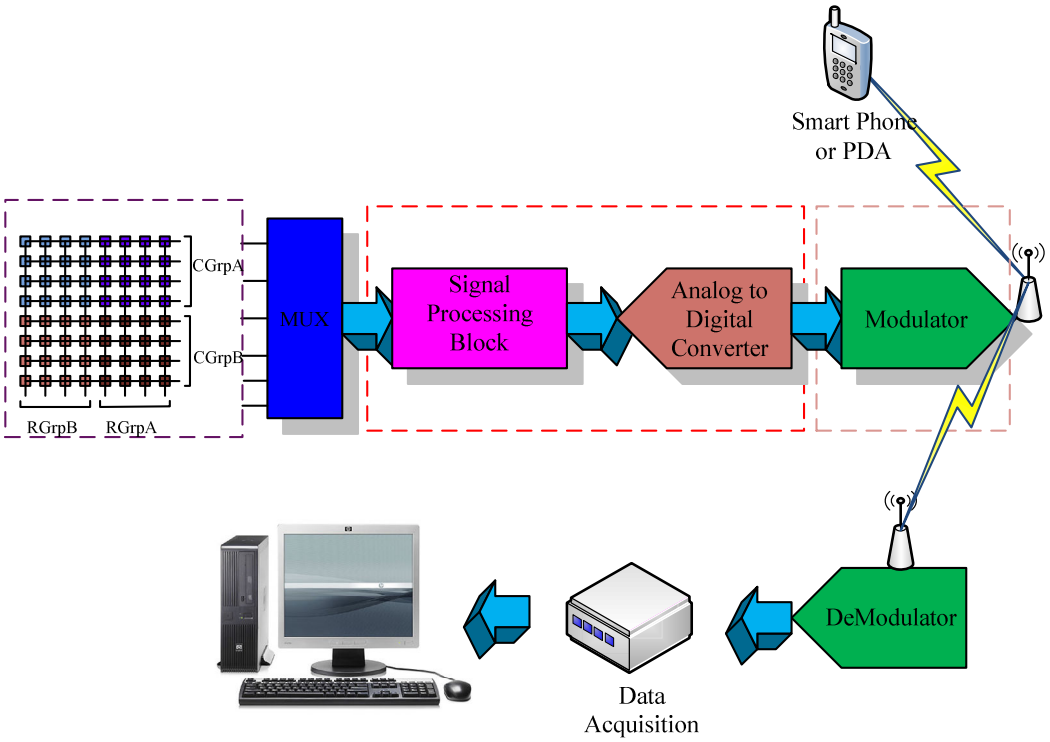


Fig 1.6: Functional block diagram of the SOP smart spacer block

The entire system manifests a sensor block, a multiplexer block, a sensor signal processing block, an analog-to-digital converter (ADC) block and finally a modulator block for wireless transmission of data. The sensor array mounted on the top surface of the smart spacer block measures the pressure profile exerted by the bones and the multiplexing unit addresses all of the sensors in a clever way so that there is a minimum time delay in between the successive scanning of each sensors. The signal processing block then amplifies the sensor signals and converts them to variable DC signals which are eventually converted to digital pulses/bits by the ADC block. These digital pulses convey valuable information about the pressure profile on the smart spacer block and ultimately quantify the tightness of ligaments or the alignment of bones over the implant. A brief description of the signal processing unit with an aim to final integration into the system-on-package smart spacer block has been depicted in the next section.

1.3.2 Signal Processing unit for Smart Spacer Block

One of the core system blocks of the smart spacer block is the signal processing unit. The signal processing unit comprises of a capacitance-to-voltage converter (C2V) chip and a successive approximation register (SAR) analog-to-digital converter (ADC) chip. A comprehensive functional description of the C2V and the SAR ADC chips has been given in the following paragraphs.

Fig 1.7 shows the functional block diagram of the C2V circuit which manifests current sense amplifiers, diode rectifiers and an instrumentation amplifier. Differential structure

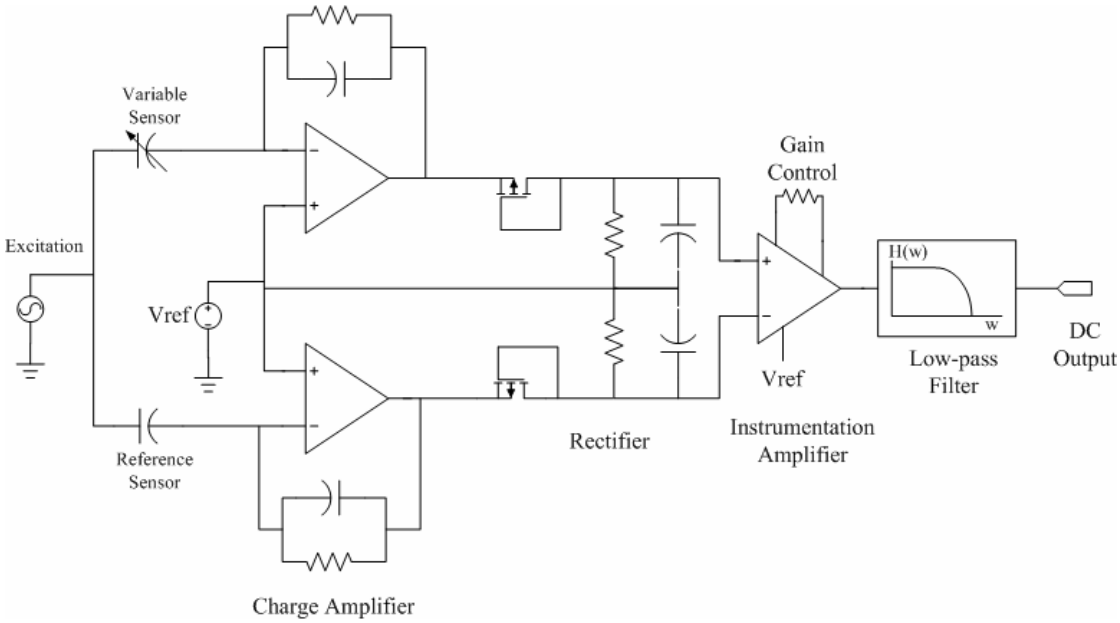


Fig 1.7: Functional block diagram of capacitance to voltage converter circuit

of the circuit eliminates even order harmonics and provides better noise performance. The sensors are arranged in differential structures and an excitation signal is used to excite the sensors. Based on the changes of the sensor signals, differential currents are produced which are then sent into the current sense amplifiers to amplify the signals and convert them to voltage signals. The converted voltage signals are then filtered and sent into an instrumentation amplifier to further amplify the differential signal and finally make a single-ended output DC signal. Therefore the variation of the output DC signal is a representation of sensor changes which eventually indicates the pressure exerted on the sensors.

The DC signal from the C2V circuit is then fed into a SAR ADC circuit. The functional block diagram of an 8-bit SAR ADC with serial output is shown in Fig 1.8. The entire

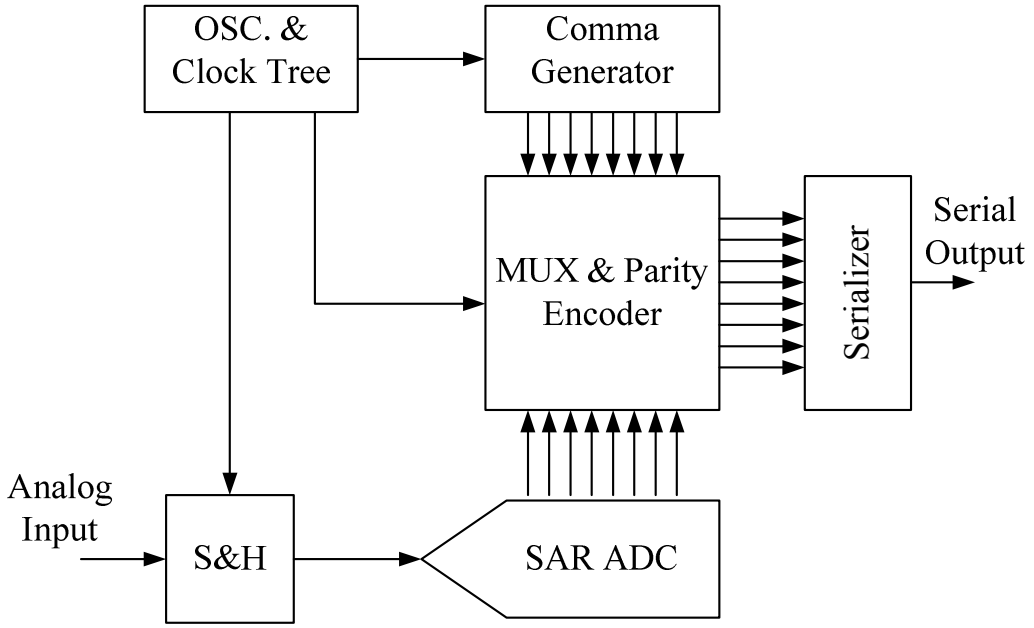


Fig 1.8: Functional block diagram of a custom SAR ADC with serial output

system consists of a SAR ADC, a serializer and a digital unit which includes an oscillator and clock tree (OSC. & Clock Tree) block, a comma generator block and a multiplexer (MUX) and parity encoder block. A sample and hold (S&H) unit is also used to sample the analog input signal and hold the signal level for conversion.

The ADC conversion time is 8 clock periods and an extra clock period is used for sampling. The parity check is designed to operate during the sampling and hence a parity check bit is added after the LSB of the previous conversion. Based on the analog input signal, an 8-bit digital parallel output is generated by the SAR ADC unit which is then serialized by a serializer. To indicate the start and end of an 8-bit data frame, a comma signal is inserted at the beginning and at the end of each 8-bit frame. The comma signal is 11001100 and 00110011 with odd parity check bit. The reason for the two byte comma

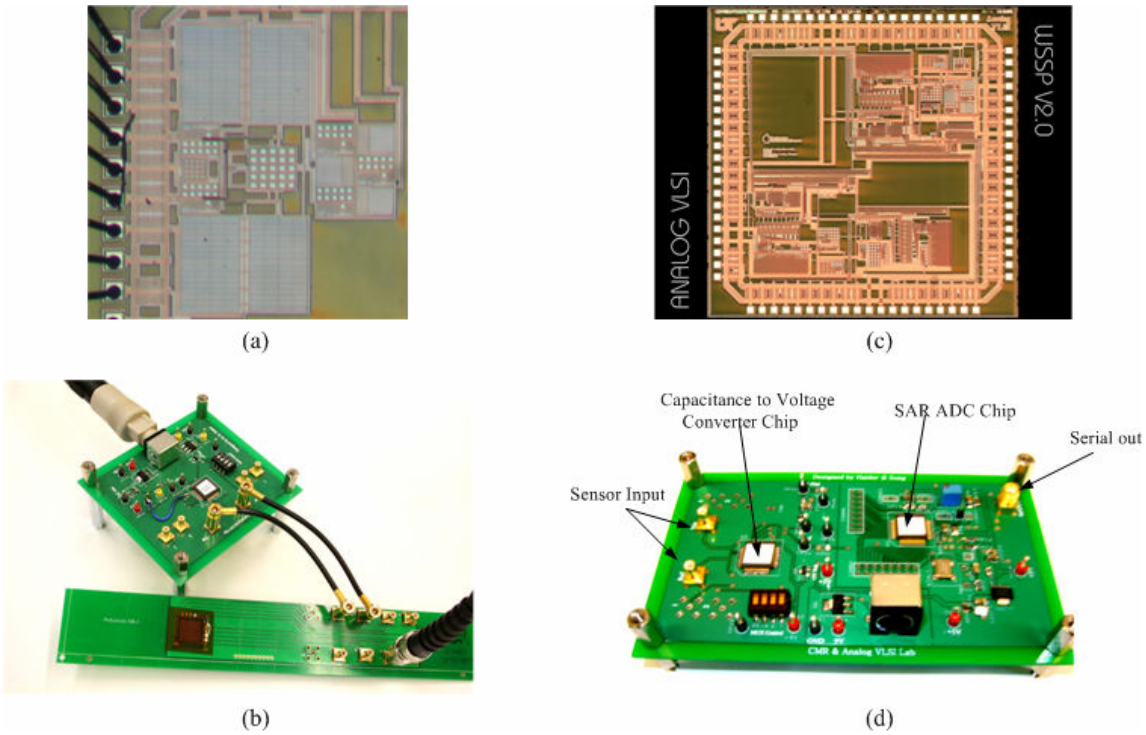


Fig 1.9: Microphotographs and Prototype Boards for Test Setup (a) microphotograph of C2V (b) test board of C2V with sensors (c) microphotograph of SAR ADC with serial output (d) test board of C2V and SAR ADC on a single board with on board connection in between the chips

signal is that the comma signal may appear in the random data pattern accidentally and may cause problem in the recovery of the data. The intentional setting of the odd parity bit and making the comma two bytes instead of one dramatically reduce the probability of a fake comma appearing in the data and also simplify the synchronous algorithm in the receiver.

Fig 1.9 shows the microphotographs and prototype boards for testing the C2V and SAR ADC chips. The C2V chip is used, as discussed earlier, to convert the sensor signal into a DC signal and the SAR ADC chip is used to convert that DC signal into an 8-bit serial data. This serial data then could be easily sent to a monitoring unit or to a transmitter for wireless transmission and monitoring from a remote location.

In the final integration of the system-on-package smart spacer block, both the C2V circuit and the SAR ADC circuit has been mapped to integrate on a single chip and a multiplexer has been placed in between the sensors and the C2V circuit for sensing signals from an array of sensors. For monitoring the data from the smart spacer block, a wire connection could be made between the smart spacer block and the monitoring unit. However, unwieldy wires limits the mobility of smart spacer block and hinders the potential screening activities by different expert persons to seek help in emergency situation. Therefore, the integration of the smart spacer block with a wireless transmitter compatible with medical wireless networks (MWN) is very critical. Since MWN works intimately with the existing matured cellular communication technology, integration of the wireless transmitter in the smart spacer block with the MWN not only helps to broadcast the data over the network in a secured fashion but also facilitates with a cost effective solution due to the usage of existing communication infrastructure.

1.4 Problem Overview

1.4.1 Powering the SOP Smart Spacer Block

Available power source is always a crucial factor for designing any portable electronic device. Different types of energy sources are investigated in the recent years such as battery, solar-power, vibration energy, etc. but until now no source is proven good enough to provide adequate power with minimum weight and almost zero maintenance. Miniature battery has been used in several implantable or biomedical devices. But the problem with the typical battery is low ampere-hour which results in shorter life. In

addition, the battery needs special biocompatible coating to prevent any kind of leakage when used with the implantable devices. It is expected that the smart spacer block will be energized with small coin size batteries. To reduce the number of coin size batteries and to realize small form factor of the smart spacer block, it is recommended that the entire electronics of the system-on-package smart spacer block should operate with low-voltage and low-power supply.

1.4.2 Low-power Wireless Transmitter

To avoid awkward wires between the smart spacer block and the monitoring unit, each smart spacer block must incorporate a low-power wireless transmitter. A conventional transmitter architecture manifests power-hungry frequency synthesizer, mixer, DAC, filters and power amplifiers. Thus the power consumption of the conventional transmitters is high and they consume a lot of expensive silicon area for monolithic integration. Therefore, the design challenges for low-power circuit involve optimization of power, silicon area and cost. Another design challenge of low-power wireless transmitter for biomedical applications is the selection of transmission frequency for reliable and safe communication between the patient and the monitoring unit.

1.4.3 Selection of Transmission Frequency

Maintaining a reliable contact between the patient and the monitoring unit is an urgent need for medical applications. Availability of clear spectrum is decreasing day by day due to the immense use of various types of wireless devices. Industrial scientific and

medical (ISM) band has been widely used for cellular communication. There are also potential chances of interference from competing uses such as television, microwave oven, private land mobile radio system (PLMRS), etc. Therefore, to overcome this problem FCC has approved wireless medical telemetry service (WMTS) band for hospital current and future use in 2000. There is no allocation of voice or video in this band. FCC has approved mainly three bands for WMTS. The first one is from 608 MHz to 614 MHz. This band is also used by radio astronomy observers. Therefore any hospital within 80 km of any radio astronomy observer needs to notify prior installation. The other two bands are 1.395 GHz to 1.4 GHz and 1.429 GHz to 1.432 GHz. Fig 1.10 shows the power transfer ratio in indoor environment of a copper wire loop antenna of radius 1 cm. The thickness of the copper wire is considered to be 0.25 mm. The power transfer ratio can be expressed as

$$\frac{P_{RX}}{P_{TX}} = \frac{\eta_{TX} \cdot D_{TX} \cdot \eta_{RX} \cdot D_{RX} \cdot p \cdot \lambda^2}{L_x \cdot (4 \cdot \pi \cdot d)^2} \qquad \textbf{(1.1)}$$

where $\eta_{TX} = \eta_{RX} = \eta$ is the efficiency of the transmitting or the receiving antennas, $D_{TX} = D_{RX} = D = \frac{3}{2}$ is the maximum directivity of the transmitting or the receiving antennas, p = 1 is the polarization vector, L = 1 is the path loss factor and d is the transmission distance (in meter) between the two antennas.

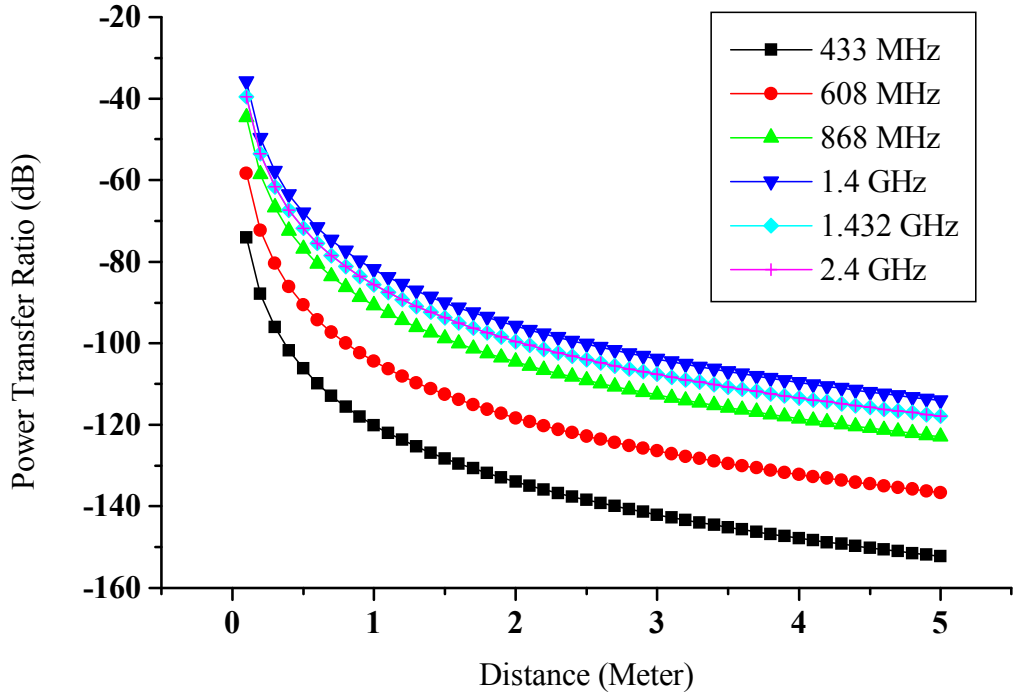


Fig 1.10: Power transfer ratio of a loop antenna in indoor environment for different frequency bands

The efficiency, radiation resistance and loss resistance of the antenna can be expressed by the following equations

$$\eta = \frac{R_{RAD}}{R_{RAD} + R_{LOSS}} \tag{1.2}$$

$$R_{RAD}(loop) = 320 \cdot \pi^4 \cdot \left(\frac{\pi \cdot r^2}{\lambda^2}\right)^2 \tag{1.3}$$

$$R_{LOSS}(loop) = \frac{\pi \cdot r}{r_o}\sqrt{\frac{f \cdot \mu}{\pi \cdot \sigma}} \tag{1.4}$$

where r = 1 cm represents the radius of loop antenna, r_o = 0.25 mm represents the thickness of copper wire used for the antenna, f for operating frequency, σ for

conductivity and μ for permeability of the copper wire. Based on this simple analysis, it is evident that in indoor environment a circular loop antenna of radius 1 cm exhibits highest power transfer ratio at 1.4 GHz frequency which also falls within WMTS band. Therefore, this research work is focused on the development of a low-power transmitter with 1.4 GHz operating frequency for biomedical applications.

1.4.4 Low-power Injection-locked Transmitter

Increasing the efficiency of a transmitter for short distance (~10m) communication is another design challenge. Usually for short range wireless communication, radiated power is low, typically in the range of 0 dBm (1mW) which is lower than the power consumption of power amplifier (PA) and pre-power amplifier (pre-PA) block of the transmitter. In addition, low-power power amplifier requires high drive requirements from the pre-power amplifier block which ultimately increases the power consumption of the later. Therefore, merely increasing the efficiency of the PA does not guarantee the overall transmitter efficiency. To resolve this problem, two lean transmitter architectures have been reported – direct modulation transmitter and injection-locked transmitter. Injection-locked transmitter provides better spectral purity of the output signal compared to the direct modulation transmitter. In addition, relatively simpler modulation schemes for instance, amplitude shift keying (ASK) or frequency shift keying (FSK) can be easily incorporated with the injection-locked transmitter by power cycling the oscillator or by varactor tuning, respectively. FSK scheme provides better noise immunity at the expense of power consumption whereas ASK scheme helps to save some power. Therefore, the

goal of the Ph. D. research is directed towards the development of a low-voltage low-power injection-locked transmitter with ASK modulation scheme for wireless sensor and body area networks.

Injection-locked transmitter consists of two oscillators – one is the reference-oscillator and the other one is the main oscillator or power-oscillator. Reference-oscillator generates a spectrally pure reference carrier frequency which is then injected to the main or power-oscillator to achieve injection-locking. Power-oscillator then feeds the signal to the antenna through the matching network or the antenna could be directly integrated with the oscillator to further reduce the loss in matching network. Injection-locked oscillator works as a first order phase locked loop (PLL) and therefore, tries to eliminate any frequency changes of the oscillator due to environmental variations. In injection-locked transmitter, the power-oscillator works as a substitute of the power amplifier and the drive requirement of the former one can be greatly reduced due to injection locking process. As a result, the power consumption of the pre-PA block can be reduced which facilitates with higher overall transmitter efficiency.

1.4.5 Low-power Injection-locked Oscillator

Structure of oscillator and types of injection are two crucial design criteria for low-power injection-locked oscillator design. Tail MOSFET injection structure requires additional voltage headroom while direct injection structure can potentially increase power consumption. Body-level injection has inherent property of low-voltage operation due to the elimination of tail MOSFET and low-power operation due to low transconductance of

the parasitic BJT in the MOSFET. In addition, conventional NMOS- only differential cross-coupled LC oscillator architectures can work with low power supply voltage but their current is relatively high due to relatively lower output resistance in each conducting path.

1.5 Research Objectives

Development of low-power transmitter is a key parameter for the future growth of wireless body area network. Existing transmitter architectures used for cellular network are not suitable for low-power short range communication because of their low efficiency. Various lean transmitter architectures have been investigated and they are proved to be potential candidates for the development of low-power transmitter. Among these, injection-locked transmitter architecture is getting interests among the researchers. However, existing injection-locked transmitter architectures either use low-voltage or low-power circuit topology and they are not suitable for both low-voltage and low-power operation. Within this era of deep sub-micron CMOS technology and batteryless operation (inductive powering) of implantable medical devices, both low-voltage and low-power circuit topology are needed for the development of low-power transmitter. Therefore, the objectives of this research project are:

(1) Development of a low-voltage low-power injection-locked oscillator structure that will facilitate the development of low-power transmitter.

(2) Derivation of the governing equations for the design of a self-cascode low-voltage low-power oscillator.

(3) Use of body-terminal coupling to increase voltage headroom and achieve low-power operation.

(4) Use of a frequency band dedicated for wireless medical telemetry.

(5) Incorporation of ASK scheme without degrading the voltage headroom.

1.6 Thesis Outlines

The outline of this dissertation is as follows.

A brief introduction of wireless telemetry and networks for medical applications has been presented in chapter 1. The motivation behind this research work and the research objectives have also been discussed in this chapter.

Conventional transmitter architectures are not suitable for low-power applications. Among the various types of low-power transmitter architectures, injection-locked transmitter shows greater promises due to its high efficiency and better phase noise performance. The building block of a low-power injection-locked transmitter is an injection-locked oscillator. Therefore a literature review has been performed on low-voltage low-power injection-locked oscillator in chapter 2.

The state of the art low-power wireless transmitter architectures and their suitability in wireless sensor network or wireless body area network have been discussed in chapter 3. This chapter has also presented some of the low-voltage circuit design topologies to overcome the problem of reduced supply voltage headroom.

Structure of injection is a crucial design factor for an injection-locked oscillator. Compared to other injection structures, body terminal coupling provides both low-voltage and low-power operation. Therefore mathematical analysis of a body coupled MOSFET has been presented in chapter 4. System dynamics of an injection-locked oscillator has also been discussed in this chapter for better understanding of the system.

To overcome the problem of reduced voltage headroom, self-cascode structure is a potential candidate for low-voltage low-power operation. Therefore the design and principles of a low-voltage low-power self-cascode body coupled oscillator has been discussed in chapter 5. Detailed mathematical analyses including the calculation of optimal MOSFET dimension, the equation for frequency of oscillation and the phase noise variation with capacitance ratio have been addressed in the chapter. Finally a comparison of the proposed design with the previously published works has been presented that confirms the effectiveness of the proposed design.

Measurement and test results of the fabricated self-cascode body coupled oscillator have been presented in chapter 6.

Finally a conclusion of this research work has been drawn and some of the future works in the related field have been mentioned in chapter 7.

Chapter 2 Literature Review

A wireless sensor or body area network consists of many distributed sensor nodes and the nodes are expected to operate for years with zero maintenance. Therefore each sensor node requires a highly integrated, low-cost transceiver with low-power consumption and high efficiency [10]. The major challenge of transceiver design in wireless sensor network (WSN) is low transmitter efficiency. In conventional high power transmitters, efficiency is largely dominated by that of the power amplifier (PA) itself. But in case of a low-power transmitter for short distance communication the driving power and the DC power consumption in the previous stage play the dominant role in the overall transmitter efficiency. Several research efforts have been reported [11, 12] to reduce power consumption in the previous stage by using a linear PA instead of a switch-mode PA. However, linear PA suffers from inherent low drain efficiency (DE) which significantly reduces the overall transmitter efficiency. Moreover, the pre-PA still incurs a significant amount of power consumption and eventually lowers the overall efficiency (i.e., power added efficiency (PAE)) by over 10% from DE of PA.

There already exist some efforts to overcome the challenges in designing low-cost, high-efficiency and small form factor transmitters for WSN applications. These transmitters either adapt existing transmitter architectures that work well for WLAN and cellular transceiver to WSN applications or utilize the inherent characteristics of WSN to reduce its complexity and power consumption. In the following section, the state-of-the-art WSN transmitters are reviewed.

2.1 Low-Power Transmitter

Direct conversion architecture is usually used for WLAN or Cellular communication. This scheme is versatile and it can support any kind of modulation schemes. Choi *et al*. have used the direct conversion transmitter architecture for WSN realized in a 0.18 μm CMOS process [13]. The direct conversion architecture uses two mixers to up-convert the baseband signal to the RF band (2.4 GHz) with the help of two quadrature local oscillator (LO) signals. Due tot the requirement of large number of circuit blocks (mixers, low pass filter, frequency synthesizer etc) the overhead power is high which ultimately reduces the transmitter efficiency. The reported transmitter consumes 30 mW of power while delivering 0 dBm power to the antenna. The overall transmitter efficiency is only 3.3%. The low efficiency is due to the low power amplifier efficiency and high power consumption by the stages prior to the power amplifier block.

Taking advantages of low data rate of WSN, simpler modulation schemes can be used such as on-off keying (OOK) and frequency-shift keying (FSK), at the expense of spectral efficiency. These simpler modulation schemes allow the use of the less complex direct modulation transmitter. In the WSN transceiver described in [14], the authors have employed a direct modulation transmitter architecture. The 900 MHz FSK transmitter consumes 1.3 mW while radiating 250 μW of power. In this transmitter, the output devices are stacked to provide for better antenna matching and to achieve a power amplifier efficiency of 40%. However, the high power consumption of the LO (accounts for 55% of the power budget) degrades the overall efficiency to only 19%. The

transmitter could deliver 0 dBm by operating the two stacked power amplifiers in parallel and combining their output powers, resulting in an overall transmitter efficiency of 13%. The transmitter supports a data rate of 100 kbps and requires one external inductor.

Since high efficiency PA requires high drive requirement, obtaining high DE and low pre-PA power at low radiated power level is particularly challenging. To relax the drive requirement injection-locking and RF MEMS have been proposed [15, 16] to achieve better compromise between pre-PA power and DE at low radiated power. Injection-locking allows the PA to be self-driven and minimizes the loading on its driver, while high-Q RF MEMS allows for ultra low-power RF carrier generation. In the injection-locked transmitter, the PA is replaced by an efficient power oscillator. To obtain an accurate carrier frequency, the power oscillator is locked to an ultra low-power high-Q film bulk acoustic resonator (FBAR). The power oscillator is then coupled to the antenna through a matching network. The transmitter has been realized in 0.13 μm standard CMOS process. In the reported injection-locked transmitter the pre-PA power has been reduced to 90 μW while the transmitter (operating at 1.9 GHz) achieves 32% efficiency at 0 dBm output power from a 280 mV supply. With 50% on-off keying, it consumes 1.6 mW and supports data rate up to 50 kbps.

2.2 Injection-locked Oscillator

Injection-locked oscillator is an essential part of the injection-locked transmitter. Low-voltage low-power operation of injection-locked power oscillator while delivering

sufficient amount of power to the antenna, is a breakthrough for the development of low-power injection-locked transmitter design. Structure of oscillator and types of injection are two crucial design criteria for the design of low-power injection-locked oscillator. Various types of injection-locked oscillator structures for different applications have been reported in the past few decades. A short literature review has been presented in the following paragraphs.

Stabilized oscillators, employed for frequency translations, are an important front-end part for any electronic systems. One method of oscillator stabilization, made popular in the 1950's and 1960's, is injection-locking [17, 18]. This technique involves injecting a stable reference signal into a free-running oscillator. Injection-locking methods are now becoming popular in a variety of applications [19-21].

Different methods of injection-locking are reported [17-18] [22-25]. Fundamental locking occurs when $f_{inj} = f_{lo}$ and a large associated locking range is obtained. However a stable source at a frequency close to the frequency of oscillation must be available. When $f_{inj} = f_{lo}/n$, an n^{th} subharmonic injection-locking takes place with a reduced locking range. Superharmonic injection-locking is observed when $f_{inj} = nf_{lo}$, and it is a well known choice now-a-days to implement a low-power frequency divider using superharmonic injection. Another type of less studied injection-locking process is parametric injection. This occurs when $mf_{inj1} + nf_{inj2} = p\, f_{lo}$. However, in parametric injection at least two injection sources are required.

Injection-locking becomes useful in a number of applications, including frequency division, quadrature generation [26, 27], and oscillators with finer phase separations [28]. Injection-locked oscillator structure has been widely used for low-power frequency divider applications. M. Tiebout [29] has reported an injection-locked oscillator based high frequency low-power frequency divider based on MOS switches directly coupled to the tank of well-known oscillators. The direct injection-locking scheme features wide locking ranges, a very low input capacitance, and highest frequency capability. The divider has been implemented using 0.13 μm CMOS process. The 40- and 50-GHz dividers consume 3 mW with 1.5 V supply for locking ranges of 80 MHz and 1.5 GHz, respectively. The 15-GHz divider consumes 23 mW and features a locking range of 2.8 GHz.

Y.-H. Chuang *et al*. [30] have reported a low-voltage and wide locking range injection-locked frequency divider using a standard 0.18 μm CMOS process. The wide locking range and the low-voltage operation are performed by adding an injection NMOS between the differential outputs of the divider that contains on-chip transformers which result in positive feedback loops to swing the output signals above the supply and below the ground potential. This dual-swing capability maximizes the carrier power and achieves low-voltage performance. The ILFD operates from 1.82 to 2.04 GHz at 0.75 V supply voltage and consumes 4.5 mW of power. The divider has more than 30% locking range. However, the divider requires two on-chip inductors.

A new current reused LC-tank injection-locked oscillator (ILO) based frequency divider realized in TSMC 0.18 μm CMOS process has been reported [31]. The ILO, used as a divide-by-two divider, consists of two switching transistors stacked in series. The injection locking is performed by adding an injection NMOS between the differential outputs of the divider. The divider can operate with a lower power due to the reuse of DC current. The measurement results show that at the supply voltage of 1.5 V, the divider free-running frequency is tunable from 2.11 to 2.42 GHz, and at the incident power of 0 dBm the locking range of the divider in the divide-by-2 mode is about 0.9 GHz (19.8%), from the incident frequency 4.1 to 5 GHz. The core power consumption is 0.97 mW.

Coupling transistors in ILO structure contributes a significant amount of power dissipation. As reported in [32-34], the coupling transistors dissipate 30 ~ 100% of the power dissipated in the core transistors, leading to a significant increase in overall power consumption. Compared to that by utilizing back-gate, the additional noise sources as well as power consumption can be avoided altogether. Although the transistor with back-gate coupling effectively works as two source-coupled transistors, the overall 1/*f* noise is expected to be the same as that of the conventional single transistor, since the 1/*f* noise of the transistor originates from the same location. Therefore, it can be considered that the body-coupled transistor is added free of 1/*f* noise. Considering these benefits a very low-power quadrature VCO (QVCO) with back-gate coupling has been presented by H. –R. Kim *et al*. [35]. The QVCO has been implemented using 0.18 μm CMOS process for 1 GHz band operation. Measurement results show the phase noise of -120 dBc/Hz at 1

MHz offset with output power of 2.5 dBm while dissipating 3 mA for the entire QVCO from 1.8 V supply.

2.3 Oscillator Structure

Structure of oscillator is another important design criterion for the development of low-power low-voltage CMOS oscillator design. There are four basic candidates for single differential topologies for low-voltage CMOS LC oscillator design [36], as follows:

1) NMOS differential topology with tail current source
2) NMOS differential topology with top current source
3) PMOS differential topology with tail current source
4) PMOS differential topology with top current source

For the tuning range capability topology (2) and (3) are preferable. This is because the anode varactor voltage remains fixed to highest potential and ground potential for case (1) and (4), respectively. In addition, PMOS devices provide lower phase noise due to inherently lower 1/f noise. Therefore, PMOS differential topology with tail current source facilitates low-phase noise with wide tuning range capability. However, tail current source requires additional voltage headroom and therefore, this tail current source can be eliminated for low-voltage operation at the expense of system linearity. Compared to NMOS or PMOS-only differential topology, CMOS differential topology provides higher transconductance and ensures low-power operation for a fixed output swing. But CMOS

structure requires almost twice the supply voltage as compared to NMOS or PMOS-only structure.

Low-power low-phase noise oscillator design has been a major focus among researchers for the last few decades. Many approaches have been developed to improve the performance of the integrated VCOs [37-40]. Cross-coupled oscillators have been preferred over other topologies due to their ease of implementation, relaxed start-up condition and differential operation. However, in cross-coupled oscillators, the noise is generated by the active devices when the oscillator is quite sensitive to perturbations [41], degrading the phase noise considerably. On the other hand, the Colpitts oscillator [42] has superior cyclo-stationary noise properties and can potentially achieve lower phase noise [43]. However, due to cascode structure of the Colpitts oscillator, this topology requires higher supply voltage.

2.4 Low-Power Low-Voltage Analog Block

In the recent years the need to develop battery operated efficient implantable medical devices has pushed the industry to design circuits with low voltage supply and low power consumption. In conventional 5 V analog circuits, the use of cascode structure yields high output impedance and therefore it is an attractive design choice. However, for less than 2 V supply, the cascode circuits are often not feasible due to the availability of reduced voltage headroom. This implies that stacking circuits vertically is not practical for low voltage design and the natural option is to grow horizontally. However, this horizontal

design style implies circuits in cascade require a sound design [44-46] to maintain stability and high performance. Because each stage contributes a pole and if more than two stages are used in closed loop, the system potentially might yield an unstable operation.

In this sub-micron CMOS era, supply voltage is reduced with each technological leap but the threshold voltage and drain-source saturation voltage do not scale at the same rate or do not scale at all. The threshold voltage does not scale down with the same rate mainly because of the sub-threshold current considerations for digital circuit in the mixed-signal environment [47]. Therefore, analog and RF designers have to face many difficulties and challenges with this limited supply voltage headroom. To overcome these problems mainly three techniques have been reported [48]. These are (a) Bulk Driven MOSFET (b) Floating Gate MOSFET, and (c) Self-Cascode Structure.

Using the property of bulk driven MOSFET, a low-voltage low-power LC VCO has been presented with a phase noise of -121dBc/Hz at 1 MHz offset [49]. The 1.14 GHz LC VCO operates with only 0.34 V supply and consumes only 103.7 μW. However, the inherent capacitor of the lateral BJT increases the capacitance of LC tank and decreases the oscillation frequency. In addition, the base-emitter junction can be forward-biased at higher voltage swing which limits the oscillation amplitude and degrades the quality factor of the LC tank VCO. This drawback can be minimized by operating the VCO at low supply voltage.

Self-cascode configuration [50] provides high output impedance with larger voltage headroom than the conventional cascode structures. Self-cascode structure has been mainly used for low-voltage low-power analog circuit design. In 2005, X. Li *et al*. have presented a self-cascode structure based differential Colpitts VCO for RF applications [51]. They have only presented phase noise simulation of the VCO.. However, the authors have not reported any fabrication of the circuit and hence any measurement results of the fabricated chip. They also have not mentioned the governing equations of oscillation frequency, required transconductance for start-up, optimal sizing of MOSFETs and trend of phase noise variations with capacitance ratios.

2.5 Summary

Low-power wireless transmitter is inevitable for easy deployment of wireless sensor nodes. Literature review reveals that conventional high power transmitters for cellular communication are not suitable for low-power and short distance wireless communication. Among the various types of low-power transmitters, injection-locked transmitter is more attractive due to its inherent features of high efficiency and better frequency stability. The core block of the injection-locked transmitter is an injection-locked oscillator. Conventional oscillator structures used for portable device applications work with either low-voltage or low-power operation. However, with the concept of scaling threshold voltage is not scaling at the same rate as that of the supply voltage. Therefore there is an urgent need to devise both low-voltage and low-power circuit to meet the future challenge. Based on literature review in this chapter self-cascode

structure and bulk-driven MOSFET can help to achieve both low-voltage and low-power operation. Self-cascode structure can be used to design a low-voltage low-power Colpitts oscillator while the body terminal coupling can used to achieve injection-locking. Mathematical analyses of such a circuit are also needed to predict the behavior of the circuit.

Chapter 3 Low-Power Transmitter for Sensor Network

3.1 Low-Power Transmitter

Power consumption of the communication system typically dominates the power consumption of the sensor nodes. Therefore to overcome this problem one has to reduce the power consumption of the transmitter. Fig 3.1 shows the block diagram of a typical wireless transmitter model.

The efficiency of this transmitter can be expressed as

$$\eta = \frac{P_{Radiated}}{P_{Radiated} + \underbrace{P_{LO} + P_{Mixers}}_{\Pr e-PA\ block} + P_{PA,loss} + P_{MN,loss} + P_{Ant,loss}} \quad \textbf{(3.1)}$$

where

$P_{Radiated}$ = Radiated power from the antenna

P_{LO} = Power loss due to local oscillator

P_{Mixer} = Power loss due to Mixer

$P_{PA,loss}$ = Power loss due to Power Amplifier

$P_{MN,loss}$ = Power loss due to matching network

$P_{Ant,loss}$ = Power loss occurred in the antenna

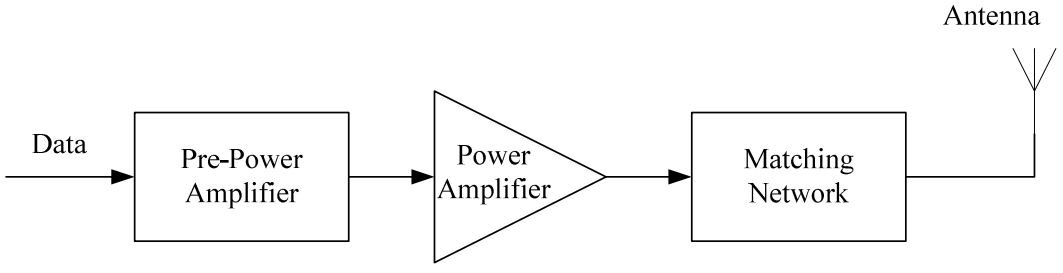


Fig 3.1: Wireless transmitter model

To minimize the transmitter total power consumption, the following steps need to be taken:

1. Minimize overhead power
2. Minimize losses in the power amplifier and pre-power amplifier
3. Radiate minimum power required for the transmission
4. Minimize duration to which PA is active

Although these requirements are quite universal, their relative importance in the case of sensor node transmitter is different compared to cellular/WLAN transmitters. In cellular/WLAN, the radiated power is much higher than the power consumption of the PA and pre-PA block. In other words, transmitter total power consumption is dominated by the power consumption of the power amplifier block. Therefore, the main focus goes to the improvement of efficiency and power consumption of the power amplifier only, which ultimately improves the performance of the entire transmitter.

In case of WBAN, the radiated power is much smaller than that of the PA and pre-PA due to the requirement of shorter communication distance, low data rate and low-power operation of the entire transmitter block. If radiated power is much higher than the pre-PA, transmitter efficiency mainly depends on the efficiency of PA. However, in WBAN radiated power is much smaller in the range of 0 dBm (1 mW) which becomes comparable or even less than the power consumption of the pre-PA block. Therefore,

simply reducing the radiated power or improving the efficiency of the PA only does not provide significant power savings.

If somehow the pre-PA power can be made lower than the radiated power then improving the efficiency of PA and decreasing the radiated power, the overall transmitter average power consumption can be reduced. However, highly efficient PA requires higher drive which ultimately increases the power consumption of the pre-PA block. As such, it requires design optimization of the PA and the pre-PA blocks altogether rather than the PA block alone.

In the following sections, conventional transmitter architecture will be discussed first and then some of the existing low-power transmitter architectures will be presented.

3.1.1 Conventional or Direct Conversion Transmitter

Fig 3.2 shows the block diagram of a conventional direct conversion transmitter. It

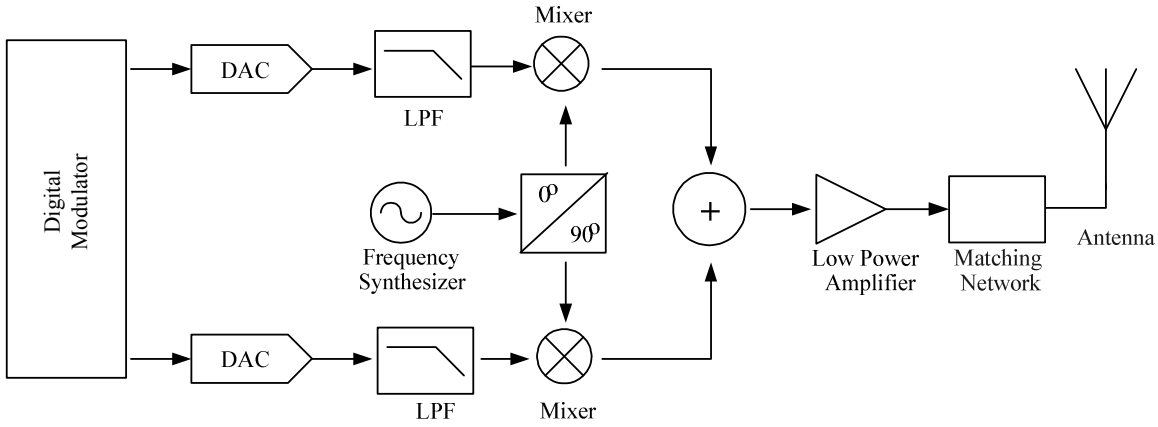


Fig 3.2: Direct conversion transmitter

consists of two up-conversion mixer to up convert the base band signal to the RF band, a frequency synthesizer with quadrature output options and a low-power amplifier. This architecture is very versatile and can support any modulation scheme with higher data rate. Due to the frequency synthesizer and mixers, the power consumption of this type of architecture is extremely high which ultimately results in poor transmitter efficiency for short range wireless communication. The reported transmitter efficiency of this architecture is in the range of 3.3%.

3.1.2 Direct Modulation Transmitter

Due to the low data rate operation in WBAN, relatively simpler modulation schemes such as on-off keying (OOK) and frequency-shift keying (FSK) can be employed. This leads to the development of less complex transmitter architecture namely direct modulation transmitter as shown in Fig 3.3. In direct modulation architecture, the baseband data

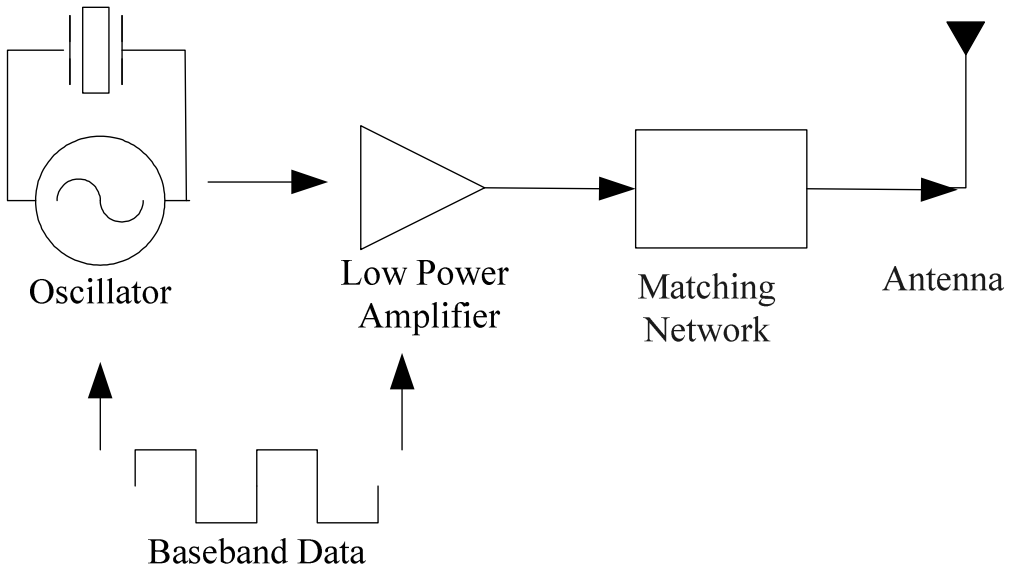


Fig 3.3: Direct modulation transmitter

directly modulates the local oscillator. Thus this architecture eliminates the requirements of power-hungry digital modulator, DACs, and I/Q mixers. OOK can be achieved by power cycling the transmitter while FSK can be achieved by varactor modulation of the local oscillator.

3.1.3 Injection-Locked Transmitter

High efficiency PA needs higher drive requirements and increases the power consumption of the pre-PA. To optimize the design requirements, injection-locked transmitter architecture can be used.

Injection-locked transmitter consists of two oscillators – one is the reference-oscillator and the other one is the main oscillator or power-oscillator (see Fig 3.4). Reference-oscillator generates a spectrally pure reference carrier frequency which is then injected to the main or power oscillator to achieve injection-locking. Power-oscillator then feeds the

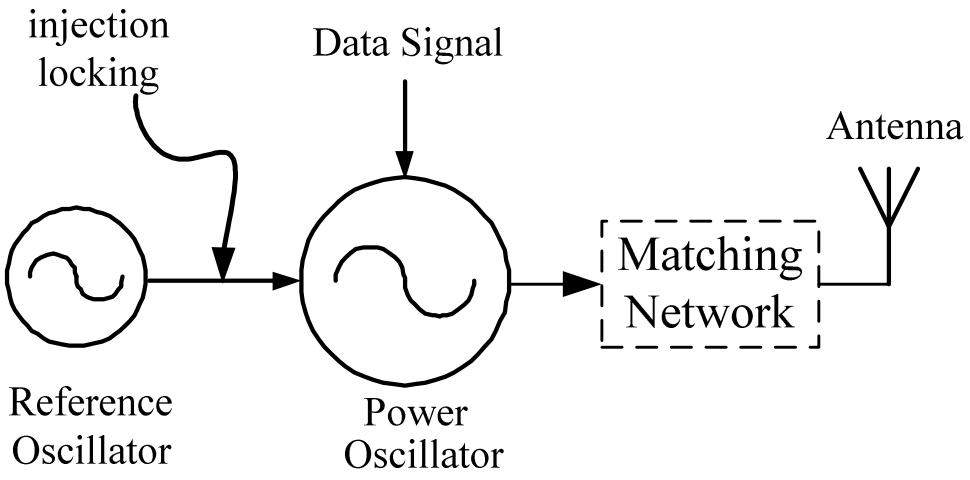


Fig 3.4: Injection-locked transmitter

signal to the antenna through the matching network or the antenna could be directly integrated with the oscillator to further reduce the loss in matching network. Injection-locked oscillator works as a first order PLL and therefore tries to eliminate any load changes of oscillator due to environmental variations. In injection-locked transmitter power-oscillator works as a substitute for the power amplifier and drive requirement of the power oscillator can be greatly reduced due to injection locking process. As a result, the power consumption of the pre-power amplifier block can be reduced which facilitates with higher overall transmitter efficiency.

3.1.4 Active Antenna Transmitter

Matching network in transmitter architecture incurs a reasonable amount of power loss and degrades the transmitter efficiency. The main purpose of matching network is to optimize the antenna impedance (~ 50 Ω) to achieve an optimal PA efficiency. In active antenna architecture as shown in Fig 3.5, the antenna provides the optimal impedance and the matching network can be eliminated. Thus no matching network loss is incurred and

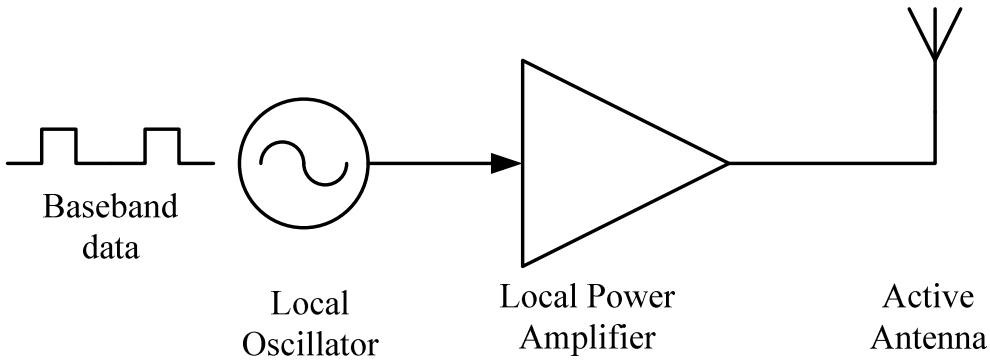


Fig 3.5: Active antenna transmitter

high PA efficiency can be achieved.

3.2 Low-Power Circuit Techniques

3.2.1 Subthreshold Operation

MOSFET operating in subthreshold region offers extremely low-power operation. In subthreshold region, MOSFET shows exponential behavior of drain current variation with gate bias voltage and offers higher transconductance efficiency (g_m/I_d). A higher g_m/I_d allows the circuit to achieve desired performance at low power. Typically when a MOSFET is operated in weak inversion or in subthreshold region its unity current gain cut-off frequency (f_T) deteriorates and thus making the device unsuitable for high frequency applications. However, with the blessing of technology scaling, today's submicron CMOS devices have achieved f_T values greater than 100 GHz and made them suitable for analog/RF circuit design even in subthreshold region.

3.2.2 Supply Voltage Reduction

Since power consumption in analog/RF circuit is proportional to the supply voltage, reducing the power supply can reduce the power consumption of the circuit. Lower supply voltage also reduces the electric field and improves the long term device reliability. However, lower supply voltage limits the dynamic range in analog circuit and offers reduced voltage headroom for cascode structures.

3.2.3 Bulk Driven MOSFET

The bulk-driven MOS transistor concept was introduced by A. Guzinski *et al*. in 1987 [52], where bulk terminals of the MOSFETs were used in the design of the differential input stage of an operational transconductance amplifier (OTA). It was later used in the design of a 1 V Op Amp utilizing the depletion characteristic of the bulk-driven MOS transistors. The reported Op Amp showed excellent rail-to-rail common-mode input range with a lower power supply voltage [53].

The original purpose of the bulk-driven differential amplifier was to yield a small g_m and to improve linearity. In conventional MOSFET configuration, gate-source voltage V_{GS} is used to control the drain current I_D through the channel whereas bulk and source terminals are shorted. Bulk-source voltage V_{BS} can also be used to modulate the drain current I_D, which is represented by g_{mb} in the MOSFET equivalent circuit. For a constant V_{GS}, bulk-driven MOSFET acts like a JFET where g_{mb} represents the effective transconductance of the signal.

Bulk-driven MOSFETs offer both advantages and disadvantages. Depletion characteristics of bulk-driven MOSFET help to avoid V_T requirement in the signal path and provide increased voltage swing for lower supply voltage. However, bulk-driven MOSFETs suffer from lower transconductance resulting in lower gain band-width (GBW) and poor frequency response. Due to lower transconductance, amplifier designed with bulk-driven MOSFETs has larger equivalent input referred noise compared to that of the gate-driven MOSFET.

3.2.4 Floating Gate MOSFET

Floating-gate technique is another low-voltage analog circuit design technique to reduce supply voltage requirement. This technique has been widely used in a number of low-power analog circuits development like CMOS analog trimming circuit [54], multipliers in neural network [55], digital-to-analog converters [56] and amplifiers [57–59].

Unlike conventional MOSFET, in floating gate MOSFET the floating gate voltage V_{FG} is controlled by the control gates through capacitive coupling. Fig 3.6 shows a simple layout and circuit symbol of a multi-input floating gate MOSFET. The floating-gate voltage can be expressed as

$$V_{FG} = \frac{\left(Q_{FG} + C_{FG,D}V_D + C_{FG,S}V_S + C_{FG,B}V_B + \sum_{i=1}^{n} C_{Gi}V_{Gi} \right)}{C_{\Sigma}} \tag{3.2}$$

where Q_{FG} is the static charge on the floating-gate, and

$$C_{\Sigma} = C_{FG,D} + C_{FG,S} + C_{FG,B} + \sum_{i=1}^{n} C_{Gi} \tag{3.3}$$

C_{Gi} is the total capacitance seen at the floating-gate.

One of the excellent properties of floating-gate MOSFET is that the electric charge in floating gate terminal can stay for several years with a variation of less than 2% at room temperature. As a result this type of device has been widely used for EPROM applications.

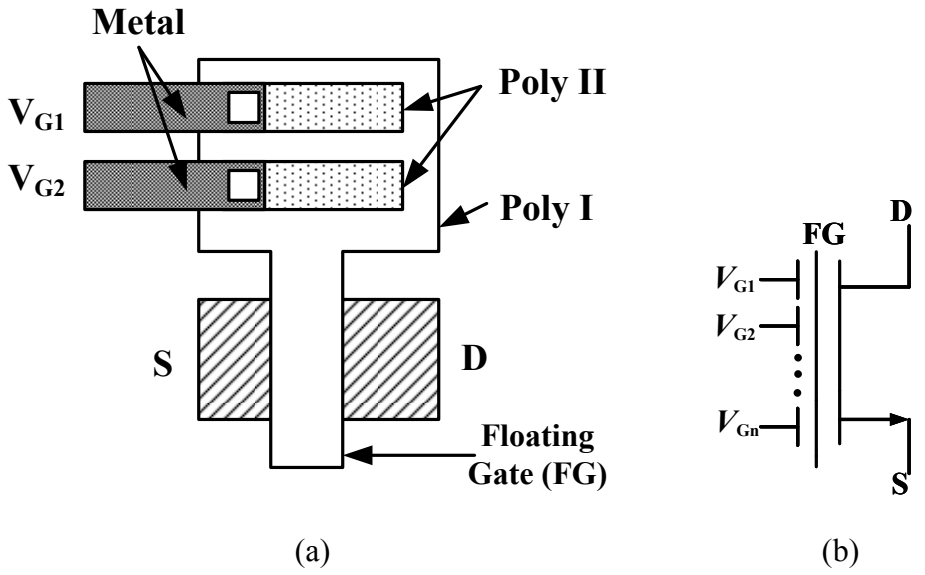


Fig 3.6: Multiple input Floating gate MOSFET (a) layout (b) schematic symbol

The static charge Q_{FG} in the floating gate terminal can be changed in three different ways:

1) Illumination under ultra-violet light,

2) Hot electron injection, and

3) Fowler-Nordheim (FN) tunneling.

3.2.5 Self-Cascode Structure

Self-cascode structure uses two MOSFETs connected in series and their gate terminals are shorted as shown in Fig 3.7. Self-cascode configuration [60] usually provides high output impedance with larger voltage headroom than the conventional cascode structures. The output resistance is approximately equal to $g_{m2}r_{o2}r_{o1}$ and $V_{DS(sat)}$ is equal to the gate over-drive voltage of a single MOSFET. For $(W/L)_2 >> (W/L)_1$, the circuit behaves like

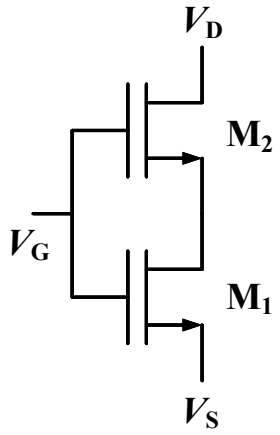


Fig 3.7: Self-cascode MOSFET

a single M1 operating in saturation region where the top (M2) MOSFET operates in the moderate inversion or weak inversion region. Although not necessary, multi-threshold voltages ($V_{T1} > V_{T2}$) help to improve the output impedance [61, 62].

3.3 Summary

A comprehensive understanding of low-power wireless transmitter including transmitter model, low-power transmitter requirements, and design challenges has been presented in this chapter. This chapter also gives short descriptions on different types of state-of-the-art low-power wireless transmitter architectures. Better frequency stability and high transmitter efficiency can be achieved from a low-power injection-locked transmitter. Active antenna transmitter can eliminate the matching network loss and can further increase the efficiency. To meet the design challenges of low-voltage and low-power operation, different low-power circuit design techniques have also been discussed at the end of this chapter.

Chapter 4 Low-Power Injection-Locked Oscillator

4.1 Introduction

Design of a low-power injection-locked oscillator is a vital task for the development of a low-power injection-locked transmitter. This chapter will focus on the large and small signal analyses of a self-cascode differential Colpitts oscillator and on the benefits of injection locking through the body terminal of the MOSFET. Different types of injection structures have been studied in the literature. Tail MOSFET injection structure (Fig 4.1) requires additional voltage headroom and direct injection structure (Fig 4.2) has a potential chance to increase power consumption. Body-level injection has inherent property of low-voltage operation due to

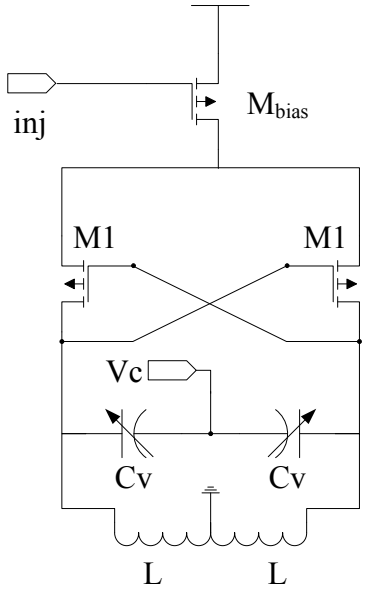


Fig 4.1: Tail-MOSFET injection-locked oscillator

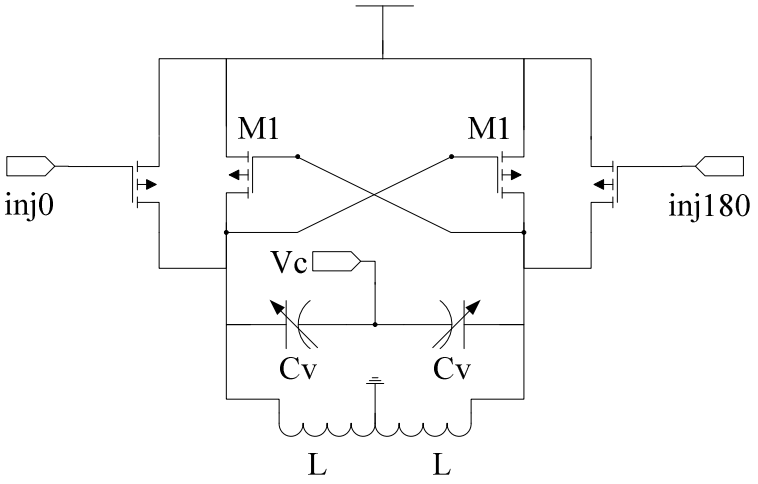


Fig 4.2: Direct injection-locked oscillator

the elimination of tail MOSFET and low-power operation due to low transconductance of the parasitic BJT in the MOSFET. As discussed earlier a conventional NMOS-only differential cross-coupled LC oscillator architecture can work with low power supply voltage but the current drawn is relatively high due to relatively lower output resistance in each conducting path. To overcome this problem, a self-cascode oscillator structure has been used which provides higher output resistance in each conducting path but is still capable of operating with lower power supply voltage. Simulation results show that the self-cascode structure consumes much less power compared to that of the conventional structure for the same output swing.

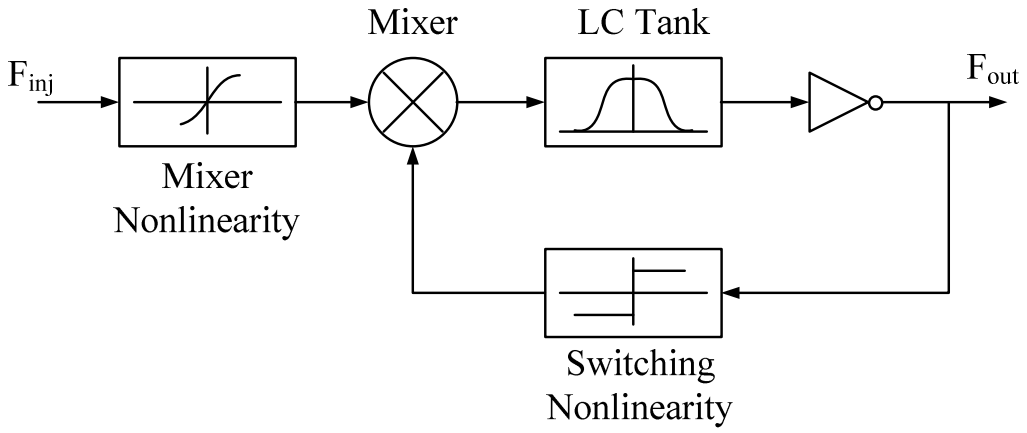


Fig 4.3: Behavioral block diagram of injection-locked oscillator

4.2 Injection-Locked Oscillator using Body Coupling (BCLO)

The behavioral block diagram of an injection-locked oscillator structure has been shown in Fig 4.3. The core functionality of an injection-locked oscillator lies in a mixer block. Inside the mixer the injection signal beats with the free running oscillator signal and the resultant harmonic signals are filtered out by the band pass filter of the LC tank. Only that harmonic signal falls within the bandwidth of the band pass filter comes out of the band pass filter and the oscillator continues to oscillate at that frequency.

The body terminal of a MOSFET (see Fig 4.4) can be used as an input of a mixer due to the mixer functionality of a body driven MOSFET [25].

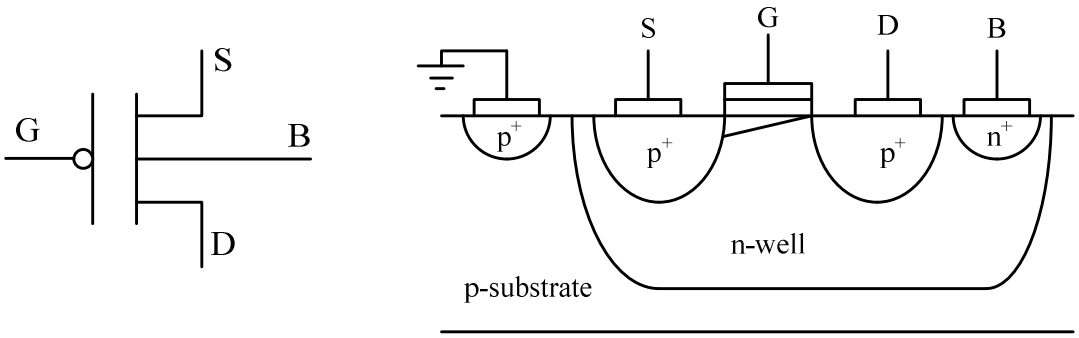


Fig 4.4: PMOS structure showing body terminal

The drain current of a body-driven MOSFET operating in saturation region can be expressed as

$$i_{DS} = \frac{\mu C_{ox}}{2} \cdot \left(\frac{W}{L}\right) \cdot \frac{\left(v_{GS} - v_T\right)^2}{1 + \theta \cdot \left(v_{GS} - v_T\right)} \cdot \left(1 + \lambda \cdot v_{DS}\right) \qquad \textbf{(4.1)}$$

If the signal at the gate terminal of the MOSFET contains both a DC component, V_{GS} and an AC component, v_{gs}, the gate terminal signal can be expressed as $v_{GS} = V_{GS} + v_{gs}$. Similarly considering body effect the threshold voltage of the MOSFET can be written as $v_T = V_T + \eta v_{sb}$, where v_{sb} is the AC component of the signal at the substrate or body terminal, η is the body factor and V_T is the threshold voltage at v_{sb}=0. Now inserting the values $v_{GS} = V_{GS} + v_{gs}$ and $v_T = V_T + \eta v_{sb}$ into equation (4.1), the drain current equation can be rewritten as

$$i_{DS} = \frac{\mu C_{ox}}{2} \cdot \left(\frac{W}{L}\right) \cdot \frac{\left\{\left(V_{GS} - V_T\right) + \left(v_{gs} - \eta v_{sb}\right)\right\}^2}{\left\{1 + \theta\left(V_{GS} - V_T\right)\right\}\left\{1 + \frac{\theta\left(v_{gs} - \eta v_{sb}\right)}{1 + \theta\left(V_{GS} - V_T\right)}\right\}} \cdot \left(1 + \lambda \cdot v_{DS}\right) \qquad \textbf{(4.2)}$$

Assuming $\theta\left(v_{gs} - \eta v_{sb}\right) < 1 + \theta\left(V_{GS} - V_T\right)$, the term $1 + \frac{\theta\left(v_{gs} - \eta v_{sb}\right)}{1 + \theta\left(V_{GS} - V_T\right)}$ can be expanded using Taylor's series expansion and considering only first three terms, the drain current equation of the MOSFET can be depicted as

$$i_{DS} = \frac{\mu C_{ox}}{2} \cdot \left(\frac{W}{L}\right) \cdot \frac{\left(V_{GS} - V_T\right)^2 + \left(v_{gs} - \eta v_{sb}\right)^2 + 2 \cdot \left(V_{GS} - V_T\right)\left(v_{gs} - \eta v_{sb}\right)}{1 + \theta\left(V_{GS} - V_T\right)} \times$$
$$\times \left\{1 - \frac{\theta\left(v_{gs} - \eta v_{sb}\right)}{1 + \theta\left(V_{GS} - V_T\right)} + \left\{\frac{\theta\left(v_{gs} - \eta v_{sb}\right)}{1 + \theta\left(V_{GS} - V_T\right)}\right\}^2 - \ldots\right\} \cdot \left(1 + \lambda \cdot v_{DS}\right) \qquad \textbf{(4.3)}$$

In equation (4.3) only $\left(v_{gs} - \eta v_{sb}\right)^2$ terms produce mixer output. Therefore taking the coefficients of $\left(v_{gs} - \eta v_{sb}\right)^2$ terms, the mixer functionality can be expressed as

$$Mixer\ Term = \frac{\mu C_{ox}}{2} \cdot \left(\frac{W}{L}\right) \cdot \frac{1 - \frac{2 \cdot \theta \cdot \left(V_{GS} - V_T\right)}{1 + \theta\left(V_{GS} - V_T\right)} + \frac{2 \cdot \theta^2 \cdot \left(V_{GS} - V_T\right)^2}{\left\{1 + \theta\left(V_{GS} - V_T\right)\right\}^2}}{1 + \theta\left(V_{GS} - V_T\right)} \times$$
$$\times \left(-2 \cdot \underbrace{v_{gs} \cdot \eta v_{sb}}_{Mixer\ Term}\right) \cdot \left(1 + \lambda \cdot v_{DS}\right) \qquad \textbf{(4.4)}$$

Fig 4.5 shows the I-V characteristics of the self-cascode structure with different body bias voltages using cadence Spectre™ simulator. For the simulation, it is assumed that the amplitude of the injection signal will not be larger than 300 mV i.e. body terminal of the

PMOS devices in the self-cascode structure will experience a body bias change of ±300 mV from the supply voltage.

For a nominal supply voltage of 1 V, the body bias of the MOSFETs in the self-cascode structure will vary from 700 mV to 1.3 V which is used in the simulation of I-V characteristics of self-cascode structure with different body bias voltages (Fig 4.5). If the body bias voltage varies with an amplitude more than 400 mV, there is a potential chance of forward biasing the source-body junction and the reverse bias condition of the body terminal of the MOSFET is violated. IBM7RF process does not provide model files for both BJT and MOS operation of the MOSFET devices. Therefore, for accurate simulation

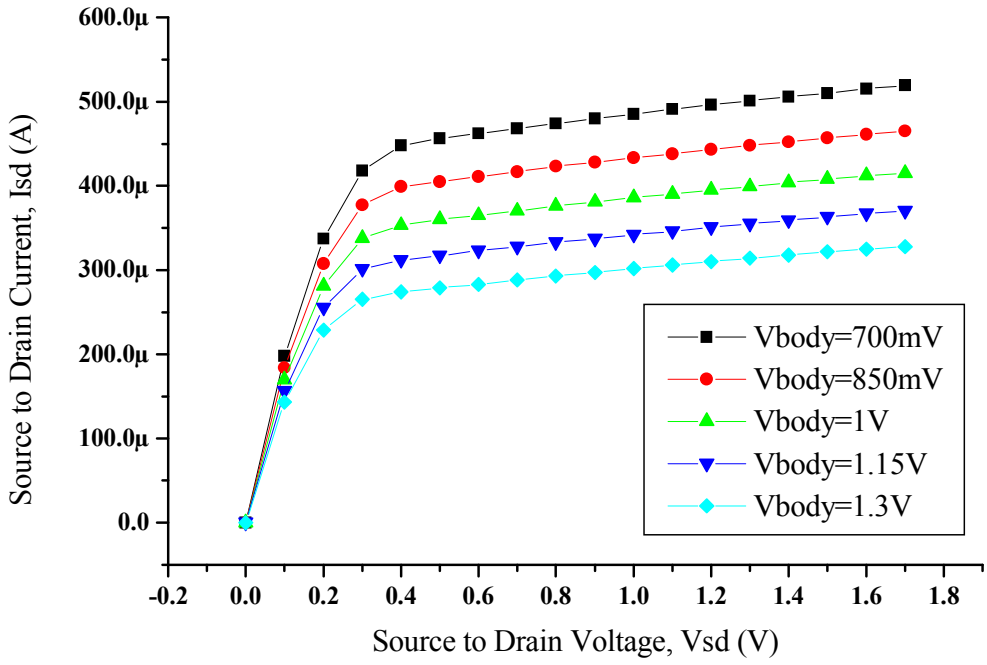


Fig 4.5: Simulated I-V characteristics of self-cascode structure with different body bias voltages

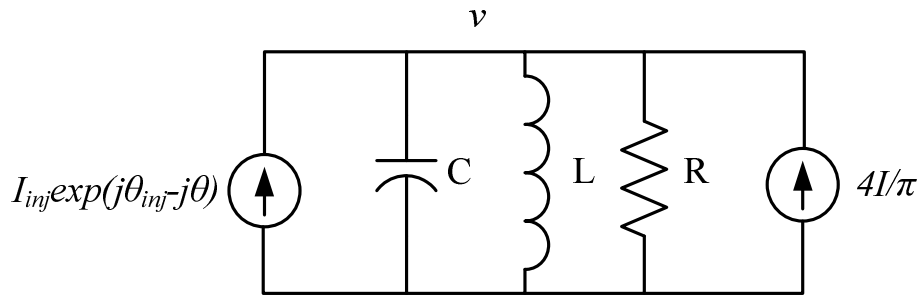


Fig 4.6: Equivalent circuit of injection-locked oscillator

and final circuit implementation, it is important to make sure that the body terminal of the MOSFET in the self-cascode structure remains in reverse bias condition.

4.3 Injection-locked LC oscillator

To study the dynamics of an injection-locked oscillator, the large signal equivalent circuit of an injection-locked LC oscillator as shown in Fig 4.6 is first considered. The single-ended half-circuit of a differential LC oscillator (Fig 4.6) consists of a lossy LC tank, the injection current $I_{\text{inj}}(t)\exp(j\theta_{\text{inj}}(t))$ and the cross-coupled transconductor that supplies negative resistance. The resonance frequency of the LC tank is $\omega_o=1/\sqrt{(LC)}$. In the absence of injected current, the circuit oscillates with free running frequency with an amplitude of $4RI/\pi$. Now if a current of magnitude I_{inj} is injected with a frequency ω_{inj} away from free running frequency ω_o, a time varying phase $\theta(t)$ and amplitude $A(t)$ will be generated in the oscillator circuit. Now applying KCL at the output node at the fundamental frequency of oscillation and using harmonic balance principle,

$$\frac{1}{R}A + C\frac{dA}{dt} + jCA\frac{d\theta}{dt} + \frac{1}{L}\exp(-j\theta)\int_0^t A\exp(j\theta)d\tau = \left(\frac{4I}{\pi}\right) + I_{inj}\exp\left(j\left(\theta_{inj}-\theta\right)\right) \qquad \textbf{(4.5)}$$

Say, $F = \exp(-j\theta)\int_0^t A\exp(j\theta)d\tau$, then

$$\frac{dF}{dt} = \exp(-j\theta)A\exp(j\theta) - j\exp(-j\theta)\frac{d\theta}{dt}\int_0^t A\exp(j\theta) \qquad \textbf{(4.6)}$$
$$\therefore \frac{dF}{dt} = A - j\frac{d\theta}{dt}F$$

Under injection-locking $\frac{d\theta}{dt} \approx \omega_0$ and envelop A(t) will be steady or it will beat at some frequency on the order of $\left|\omega_0 - \omega_{inj}\right|$. Therefore,

$$\begin{aligned} F \approx \frac{A}{j\frac{d\theta}{dt}} &= -j\frac{A}{\omega_0 + \left(\frac{d\theta}{dt} - \omega_0\right)} \\ &= -j\frac{A}{\omega_0\left(1 + \frac{\left(\frac{d\theta}{dt} - \omega_0\right)}{\omega_0}\right)} \\ &= -j\frac{A}{\omega_0}\left(1 + \frac{\frac{d\theta}{dt} - \omega_0}{\omega_0}\right)^{-1} \\ &= -j\frac{A}{\omega_0}\left(1 - \frac{\frac{d\theta}{dt} - \omega_0}{\omega_0} + ...\right) \\ &= -j\frac{A}{\omega_0^2}\left(\omega_0 - \frac{d\theta}{dt} + \omega_0\right) \\ &= -j\frac{A}{\omega_0^2}\left(2\omega_0 - \frac{d\theta}{dt}\right) \end{aligned} \qquad \textbf{(4.7)}$$

Now, using equations (4.5) and (4.7), the harmonic balance equation can be written as

$$\frac{1}{R}A + C\frac{dA}{dt} + jCA\frac{d\theta}{dt} - j\frac{A}{L}\frac{\left(2\omega_0 - \frac{d\theta}{dt}\right)}{\omega_0^2} = \left(\frac{4I}{\pi}\right) + I_{inj}\exp\left(j\left(\theta_{inj} - \theta\right)\right) \qquad \textbf{(4.8)}$$

Equating real and imaginary parts from the above equation

Real parts:

$$A + RC\frac{dA}{dt} = R\left(\frac{4I}{\pi} + I_{inj}\cos\left(\theta_{inj} - \theta\right)\right) \qquad \textbf{(4.9)}$$

Imaginary parts:

$$\begin{aligned}
&jCA\frac{d\theta}{dt} - j\frac{A}{L}\frac{\left(2\omega_0 - \frac{d\theta}{dt}\right)}{\omega_0^2} = jI_{inj}\sin\left(\theta_{inj} - \theta\right) \\
&\Rightarrow CA\frac{d\theta}{dt} - \frac{A}{L}\frac{\left(2\omega_0 - \frac{d\theta}{dt}\right)}{\omega_0^2} = I_{inj}\sin\left(\theta_{inj} - \theta\right) \\
&\Rightarrow \left(CA + \frac{A}{\omega_0^2 L}\right)\frac{d\theta}{dt} - \frac{2A}{\omega_0 L} = I_{inj}\sin\left(\theta_{inj} - \theta\right) \\
&\Rightarrow A\cdot 2\cdot\frac{d\theta}{dt} - 2\cdot\omega_0\cdot A = I_{inj}\sin\left(\theta_{inj} - \theta\right)\cdot\omega_0^2 L \qquad \textbf{(4.10)} \\
&\Rightarrow \frac{d\theta}{dt} - \omega_0 = \frac{\omega_0^2 L}{2A}I_{inj}\sin\left(\theta_{inj} - \theta\right) \\
&\Rightarrow \frac{d\theta}{dt} - \omega_0 = \frac{\omega_0}{2\cdot\frac{A}{R}\cdot\frac{R}{\omega_0 L}}I_{inj}\sin\left(\theta_{inj} - \theta\right)
\end{aligned}$$

$$\therefore \frac{d\theta}{dt} = \omega_0 + \frac{\omega_0}{2 \cdot Q} \cdot \frac{I_{inj} \sin(\theta_{inj} - \theta)}{\frac{4I}{\pi} + I_{inj} \cos(\theta_{inj} - \theta)} \tag{4.11}$$

This is the generalized Adler's Equation for injection-locking.

Under weak injection ($I_{inj} << I$), the equation (4.11) simplifies to Adler's original differential equation

$$\therefore \frac{d\theta}{dt} = \omega_0 + \frac{\omega_0}{2 \cdot Q} \cdot \frac{\pi}{4} \cdot \frac{I_{inj}}{I} \cdot \sin(\theta_{inj} - \theta) \tag{4.12}$$

Under lock condition, $\theta = \omega_{inj} t$ and $\theta_{inj} = \omega_{inj} t + \varphi$. From equation (4.11), the term φ must satisfy the following trigonometric function

$$\frac{\omega_o}{2Q} \frac{I_{inj}}{\omega_{inj} - \omega_o} \sin(\varphi) - I_{inj} \cos(\varphi) = \frac{4I}{\pi} \tag{4.13}$$

The equation (4.13) can be solved by replacing *sin(φ)* and *cos(φ)* to *2*tan(φ/2)/(1+tan²(φ/2))* and *(1+tan²(φ/2))/(1+tan²(φ/2))*, respectively. After simplification, the solution of equation (4.13) becomes

$$\tan\left(\frac{\varphi}{2}\right) = \frac{-a \pm \sqrt{a^2 + b^2 - c^2}}{2a} \tag{4.14}$$

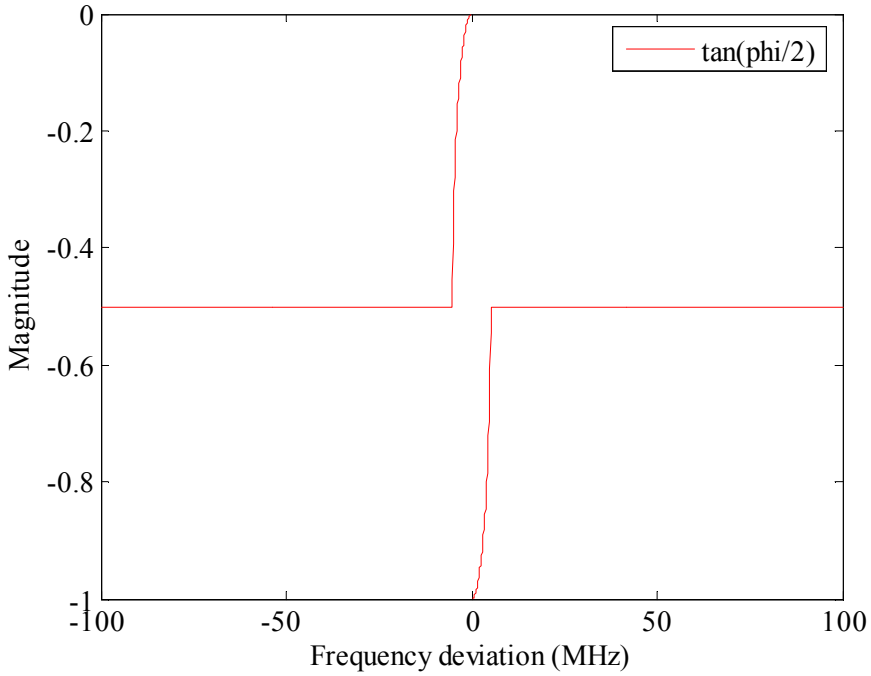


Fig 4.7: Graphical representation of equation 4.14

where $a = \frac{\omega_o}{2Q}\frac{I_{inj}}{\omega_{inj} - \omega_o}$, $b = I_{\text{inj}}$ and $c = 4I/\pi$ respectively. A graphical representation of equation (4.14) with frequency deviation with respect to free running frequency has been shown in Fig 4.7. From the figure, it is obvious that the magnitude of tan(φ/2) approaches close to zero as the injection signal becomes closer to the free running oscillating signal.

4.3.1 Quasi-Lock Condition

For an injection signal of frequency within the locking range, a perfect locking is achieved and oscillating signal follows the frequency of injection signal. However, if the frequency of the injection signal is at the edge or out of the locking range a quasi-lock condition is aroused and a 360^o phase slip occurs after a periodic interval.

The quasi-lock condition and the corresponding pulling behavior can be explained using the Adler's original equation of injection-locking which is expressed as [27]

$$\frac{d\theta}{dt} = \omega_0 - \omega_{inj} - \omega_L \cdot \sin\theta \qquad \textbf{(4.15)}$$

where ω_L represents the one-sided locking range of the oscillator.

Equation (4.15) can be rewritten as

$$\frac{d\theta}{\omega_0 - \omega_{inj} - \omega_L \cdot \sin\theta} = dt \qquad \textbf{(4.16)}$$

After carrying out simple mathematical manipulation, the solution of equation (4.16) becomes

$$\tan\frac{\theta}{2} = \frac{\omega_L}{\omega_0 - \omega_{inj}} + \frac{\omega_b}{\omega_0 - \omega_{inj}} \cdot \tan\frac{\omega_b t}{2} \qquad \textbf{(4.17)}$$

where $\omega_b = \sqrt{\left(\omega_0 - \omega_{inj}\right)^2 - \omega_L^2}$.

A graphical representation of equation (4.17) is shown in Fig 4.8. The important thing here is that if the injection signal is out of the locking range the injection signal (dashed line in Fig 4.8) maintains a constant 90^o phase shift with the oscillator signal as if the oscillator signal is locked with the injection signal. This is represented as 'Quasi-Lock' condition in Fig 4.8. However, at the end of each period and at the beginning of next

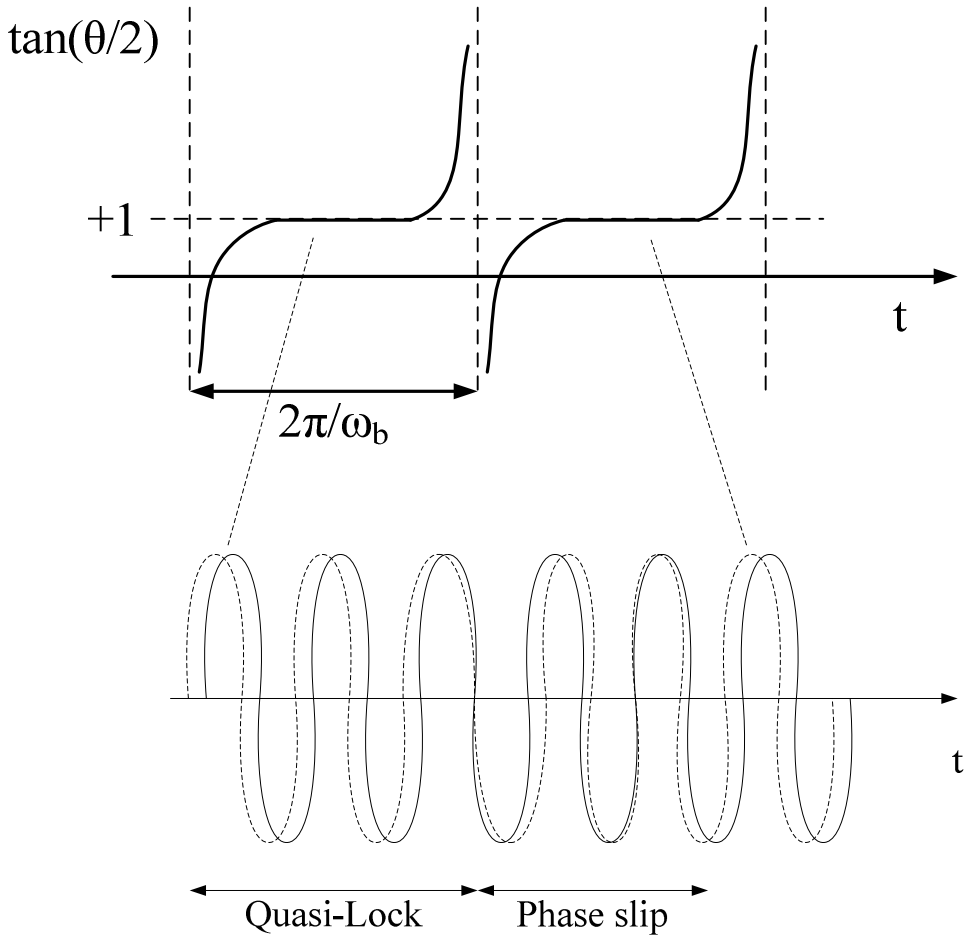
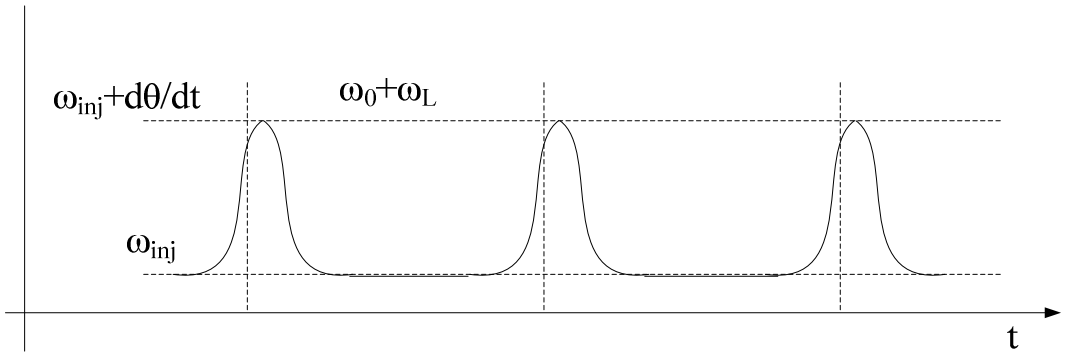


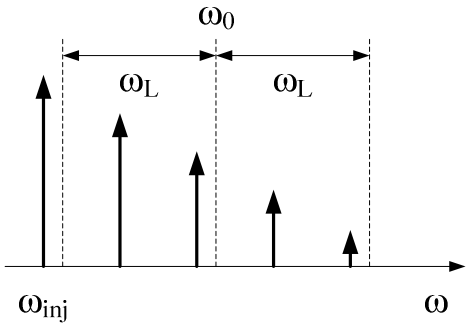
Fig 4.8: Phase variation of a quasi-lock oscillator

period the phase difference undergoes a rapid 360^0 change and returns to the quasi-lock condition.

The instantaneous frequency plot of a quasi-lock or injection pulled oscillator can be shown as in Fig 4.9(a). The important point here is that for injection frequency ω_{inj} less than the oscillator frequency, ω_0 by more than locking range ω_L i.e. $|(\omega_0 - \omega_{inj})| > \omega_L$, the oscillator frequency only goes above the injection frequency. This can be more clarified from equation (4.15) that can be rewritten as follows



(a)



(b)

Fig 4.9: (a) Instantaneous frequency and (b) power spectrum of a quasi-lock oscillator

$$\omega_0(t) = \omega_{inj} + \frac{d\theta}{dt} + \omega_L \cdot \sin\theta \qquad \textbf{(4.18)}$$

From equation (4.18) it is obvious that ω_0(t) can only vary above ω_{inj} and under quasi-lock condition i.e. ($\omega_0 \approx \omega_{inj} + \frac{d\theta}{dt}$), ω_0(t) can have a maximum value of $\omega_0+\omega_L$. The power spectrum of a quasi-lock oscillator is shown Fig 4.9(b) from where it can be seen that most of the energy is confined within the range [ω_{inj} $\omega_0+\omega_L$] and the magnitude of harmonic peaks diminishes almost linearly on a logarithmic scale.

4.4 Summary

The core block of a low-power injection-locked transmitter is an injection-locked oscillator. Structure of injection is a crucial factor to design a low-voltage low-power injection-locked oscillator. Compared to other injection mechanisms, body terminal coupling can provide both low-voltage and low-power operation. Therefore this chapter has presented mathematical formulation of a body coupled MOSFET. System dynamics and quasi-lock condition of an injection-locked oscillator has also been described in this chapter for better understanding of the system.

Chapter 5 Low-Power Low-Voltage Self-Cascode Oscillator

5.1 Introduction

Low-power LC oscillator design has been a long research in the past few decades. NMOS/PMOS-only cross-coupled oscillators have been preferred over other topologies due to their low-voltage operation, ease of implementation, relaxed start-up condition and differential operation. However, the cross-coupled oscillators are quite sensitive to active device noise which eventually degrades the oscillator phase noise. On the other hand, the Colpitts oscillator shows superior phase noise performance at the cost of higher supply voltage due to the cascode structure in the circuit. Therefore, a solution is needed to achieve better phase noise performance while maintaining a low-voltage low-power operation.

From the earlier discussion in chapter 3, section 3.2.5, a self-cascode structure can operate with a lower power supply voltage while facilitating all the excellent features of a regular cascode structure. However, the cascode MOSFET in the self-cascode structure needs to have large W/L ratio compared to the other one to achieve the required functionality of the structure. Therefore a mathematical formulation to calculate the optimal sizes of the MOSFETs in the self-cascode structure has been presented in this chapter. Other governing equations to design an LC oscillator such as frequency of oscillation, required transconductance to startup and phase noise variation have also been presented here. Finally a performance comparison of the proposed design with the existing LC oscillator structures confirms the effectiveness of the design.

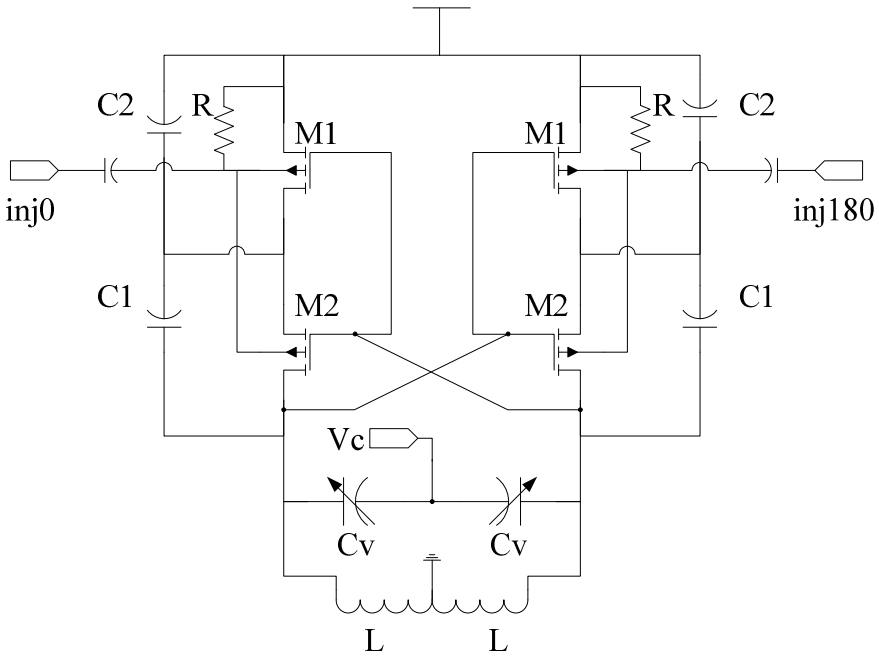


Fig 5.1: Circuit schematic of self-cascode body-coupled oscillator

5.2 Self-Cascode Body Coupled Oscillator

Fig 5.1 shows the circuit schematic of a self-cascode body-coupled differential oscillator. Assuming perfect symmetry, half of the circuit will resemble the other half. Considering the one half of the circuit, transistors M1 and M2 form the self-cascode structure where gates of two MOSFETs are shorted together. Body terminals of both the MOSFETs are tied together and connected to the supply voltage through a bias resistor R. External injection signal is applied to the body terminal using a coupling capacitor so that the source-substrate junctions of both the MOSFETs always remain in reverse bias condition and body coupling is ensured. Capacitor C1 and C2 are used to provide capacitive feedback and to boost the transcoductance (g_m) of the circuit. The total capacitance

including the varactor and the feedback capacitance resonates with the inductance L and sets the frequency of oscillation of the oscillator circuit.

Table 5.1: Comparison of power consumption of self-cascode and conventional LC oscillators

Oscillator Structure	Frequency (GHz)	Output Swing (V)	Supply Voltage (V)	DC Current (mA)	DC Power (mW)
PMOS Conventional	1.4474	1.073	0.750	3.784	2.8380
PMOS Self-Cascode	1.4482	1.07	1	1.62	1.62

Due to the self-cascode structure the oscillator is capable of operating with low supply voltage with low-power consumption. A comparative study of power consumption of a self-cascode LC oscillator and a conventional cross-coupled oscillator for a fixed frequency and fixed output swing has been presented in Table 5.1. It is evident from the table that the self-cascode LC oscillator can provide better performance while maintaining a low-voltage low-power operation. The capacitive feedback with self-cascode structure looks alike a Colpitts oscillator structure and hence provides better phase noise performance compared to a conventional tail-bias cross-coupled oscillator for the same output swing. Fig 5.2 shows the phase noise performance of the self-cascode oscillator and the tail-bias oscillator for the same output swing. The phase noise of the self-cascode oscillator at different process corners is shown in Fig 5.3. The lowest phase noise is found for the ‘ff’ process whereas the highest is found for the ‘ss’ process. Fig 5.4: depicts the simulated supply pushing of the self-cascode VCO. From the figure, it is obvious that with a supply voltage as low as 1 volt, the oscillator is capable of generating the desired output

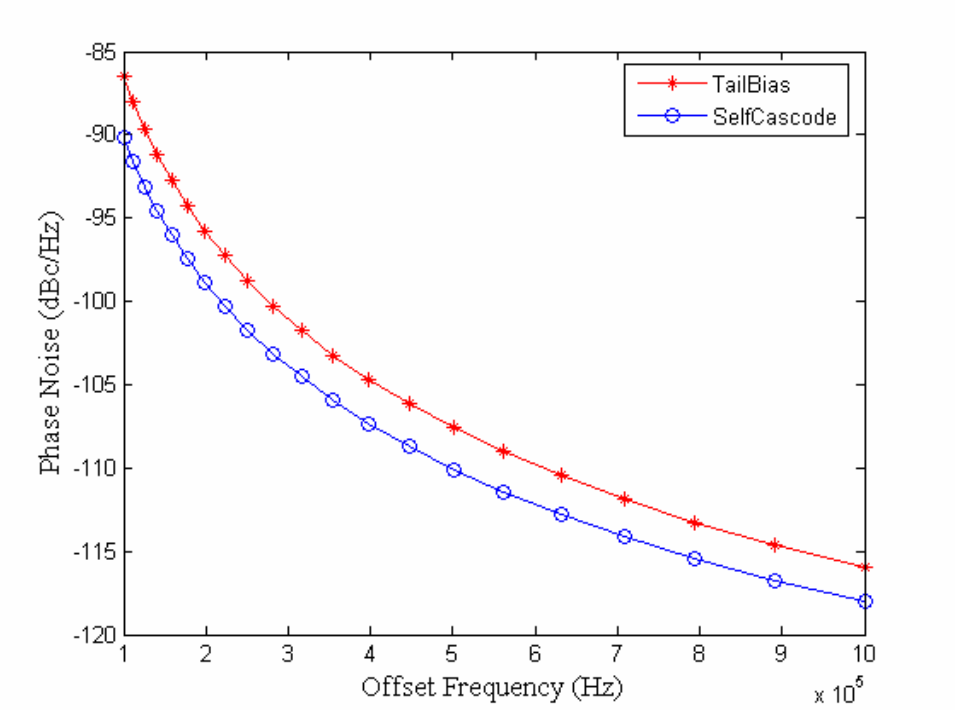


Fig 5.2: Phase noise comparison of conventional tail-biased VCO and self-cascode VCO

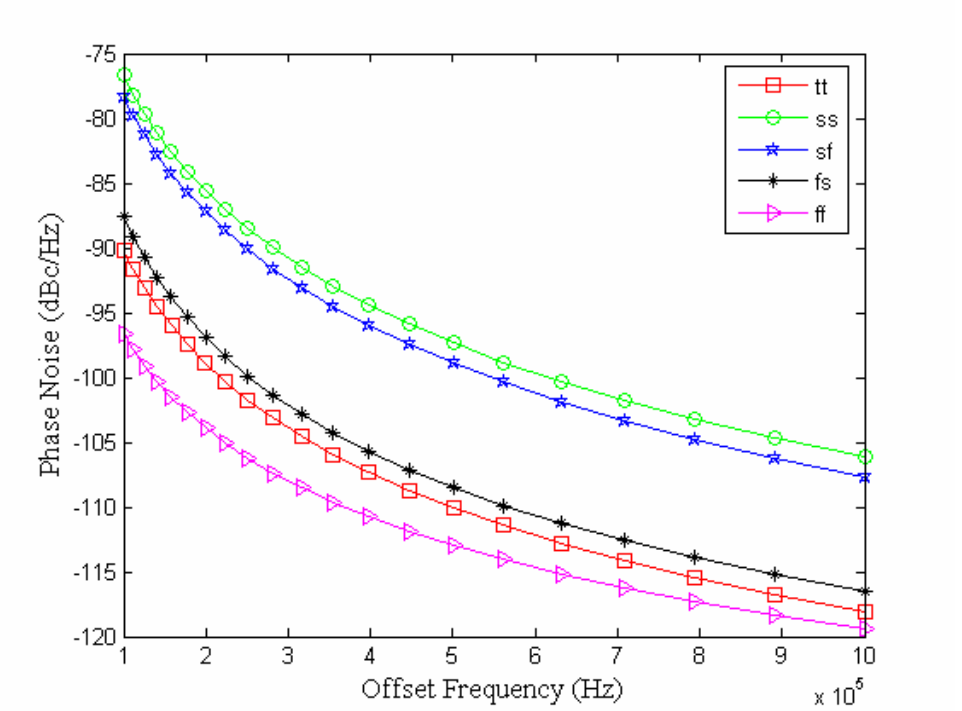


Fig 5.3: Phase noise of self-cascode VCO at different process corners

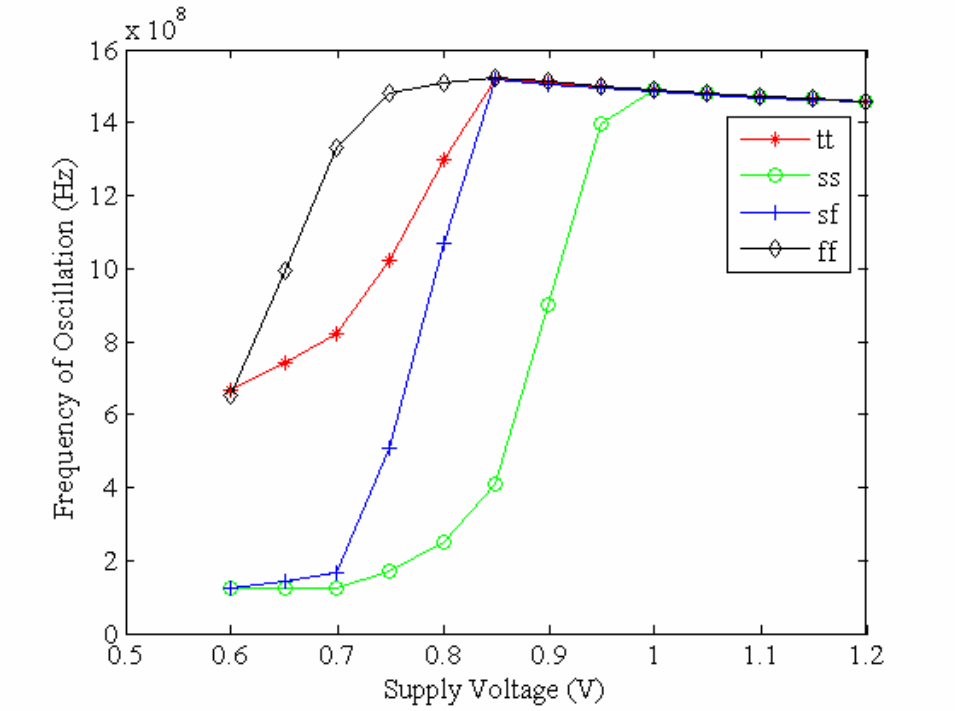


Fig 5.4: Supply pushing of self-cascode VCO

frequency. The large frequency deviation with process corners for less than 1 V supply is due to the voltage bias scheme used in this design.

5.3 Large Signal Analysis of Self-Cascode Structure

5.3.1 Transfer Function of Capacitive Impedance Transformer

Large signal equivalent circuit of a self-cascode LC oscillator with capacitive feedback structure is shown in Fig 5.5. Here R_p represents the equivalent parallel resistance of inductor and g_m represents the equivalent transconductance of the self-cascode structure, and C_1 and C_2 represent the two feedback capacitors.

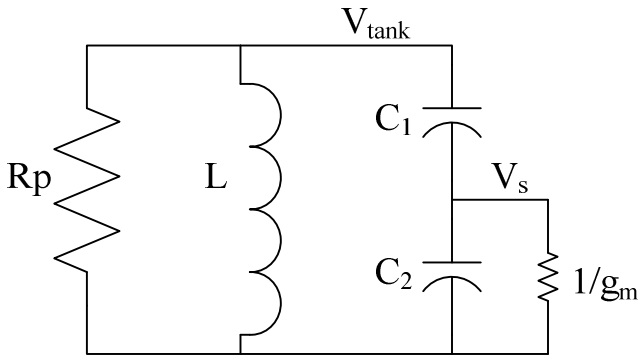


Fig 5.5: Large signal equivalent circuit of self-cascode LC oscillator with capacitive feedback structure

In Fig 5.5 V_{tank} represents the amplitude of the output voltage and V_s represents the voltage at the source terminal of the top MOSFET (M2 in Fig 5.1) in the self-cascode structure. Now using voltage divider rule the voltage V_s is given by

$$\frac{Z_1}{Z_1 + Z_2} V_{\tan k} = V_s \tag{5.1}$$

where $Z_1 = \frac{1}{j\omega C_1}$ and $Z_2 = \frac{\left(\frac{1}{g_m} \cdot \frac{1}{j\omega C_2}\right)}{\frac{1}{g_m} + \frac{1}{j\omega C_2}}$. Inserting the values of Z_1 and Z_2 in equation (5.1) and after simplification the resultant equation becomes

$$\frac{V_s}{V_{\tan k}} = \frac{j\omega C_1 \cdot \frac{1}{g_m}}{1 + j\omega \frac{1}{g_m}\left(C_1 + C_2\right)} \tag{5.2}$$

The equation (5.2) can be further simplified as

$$\therefore \frac{V_s}{V_{tank}} = \left(\frac{C_1}{C_1 + C_2} \right) \cdot \frac{j\frac{\omega}{\omega_c}}{1 + j\frac{\omega}{\omega_c}} \qquad \textbf{(5.3)}$$

where $\omega_c = \frac{g_m}{(C_1 + C_2)}$

Fig 5.6 depicts the transfer function of capacitive transformer for different capacitance ratios where the value of C_1 is 1 pF. From the figure, it is obvious that beyond the cut-off frequency of the capacitive transformer the gain of the transformer remains fixed for different frequencies but changes for different capacitance ratios. Therefore, one must use this type of capacitive transformer for impedance transformation where the frequency of operation is higher than the cut-off frequency of the transformer. Fig 5.7 shows the plot of cut-off frequency for different capacitance ratios. This plot helps to select the operating frequency of any circuit where this type of capacitive transformer will be used.

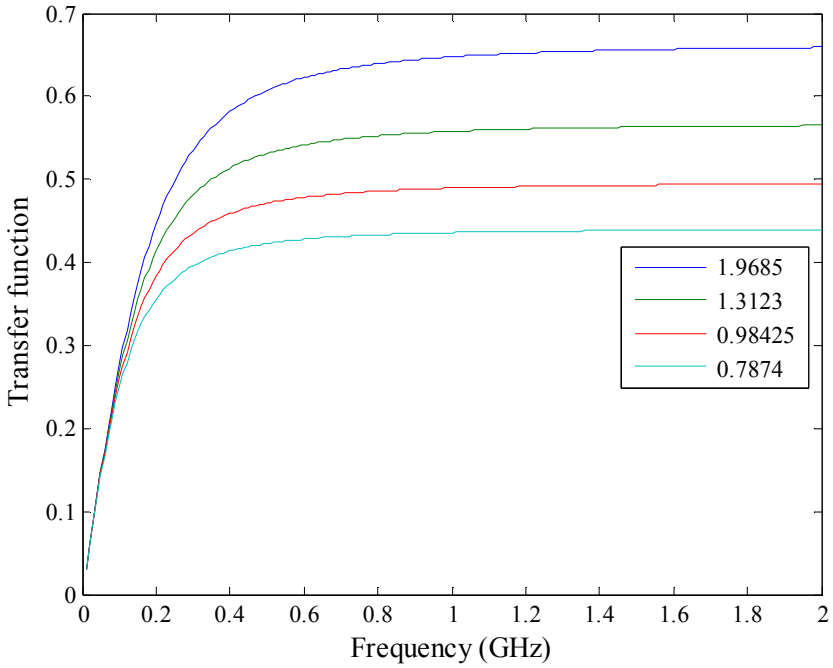


Fig 5.6: Transfer function of capacitive transformer for different capacitor ratios (C_1= 1pF)

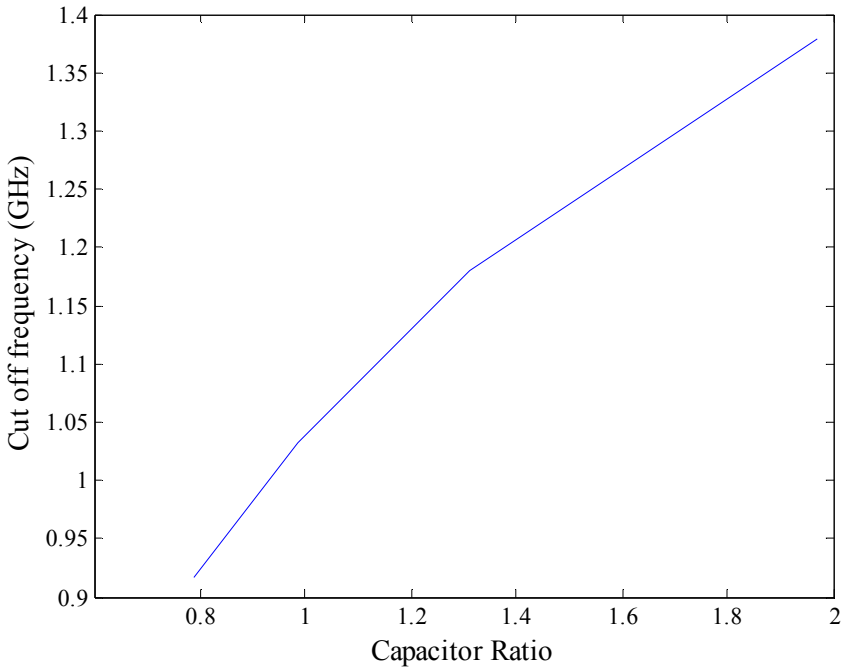


Fig 5.7: Cut off frequency variation with different capacitance ratios

5.4 Small Signal Analysis of Self-Cascode Structure

5.4.1 Calculation of Negative Resistance without Capacitive Feedback

Fig 5.8 shows the small signal equivalent circuit of the self-cascode structure without capacitive feedback. Here v_1 and v_2 represent two differential signals generated from the self-cascode differential oscillator. v_t is the test signal used to measure the negative resistance of the structure. The test current i_t flowing through the self-cascode structure can be expressed as

$$i_t = g_{m1} v_{2x} + \frac{(v_1 - v_x)}{r_{02}} \tag{5.4}$$

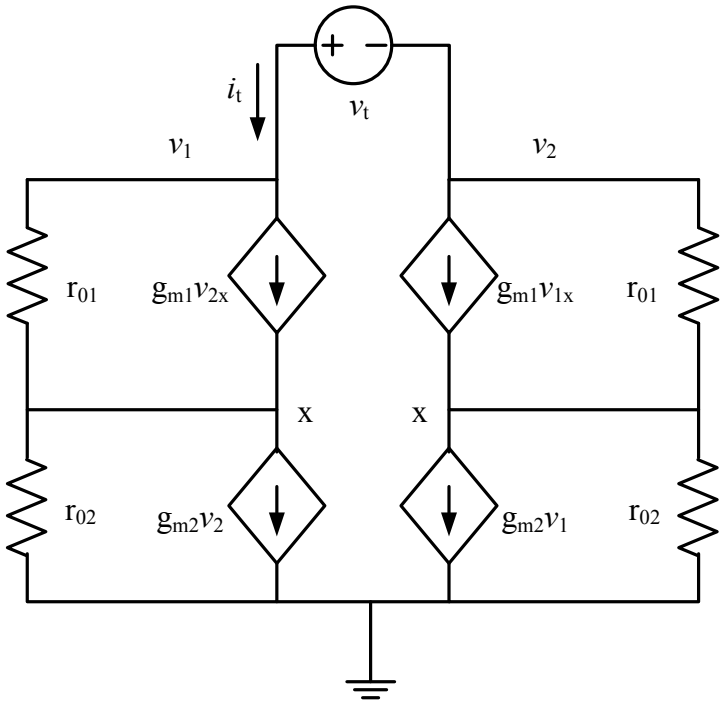


Fig 5.8: Small signal equivalent circuit of self-cascode structure

Now, using the conditions $v_t = v_1 - v_2$, $v_1 = -v_2$ and $v_x = (i_t - g_{m2}v_2)\cdot r_{02}$, the equation (5.4) can be rewritten as

$$i_t = g_{m1}\{v_2 - (i_t - g_{m2}v_2)\cdot r_{02}\} + \frac{\{v_1 - (i_t - g_{m2}v_2)\cdot r_{02}\}}{r_{01}} \qquad \textbf{(5.5)}$$

After simplification of equation (5.5), the negative resistance can be expressed as

$$\therefore R_{neg} = \frac{v_t}{i_t} = \frac{-2v_2}{i_t} = -2\cdot\frac{g_{m1}r_{01}r_{02} + (r_{01} + r_{02})}{(g_{m1}r_{01} + g_{m2}r_{02} - 1) + g_{m1}g_{m2}r_{01}r_{02}} \qquad \textbf{(5.6)}$$

For the special case,

if $g_{m1}r_{01}r_{02} >> (r_{01} + r_{02})$ and $g_{m1}r_{01} + g_{m2}r_{02} = 1$ then

$$R_{neg} = \frac{v_t}{i_t} = \frac{-2v_2}{i_t} \approx -2\cdot\frac{g_{m1}r_{01}r_{02}}{g_{m1}g_{m2}r_{01}r_{02}} \qquad \textbf{(5.7)}$$

$$R_{neg} \approx -\frac{2}{g_{m2}} \qquad \textbf{(5.8)}$$

This is similar to NMOS or PMOS-only differential topology. However, for self-cascode structure, the bottom MOSFETs have to have channel length modulation effect. Otherwise, the value of r_{02} will be infinity and the value of R_{neg} will be indeterminate.

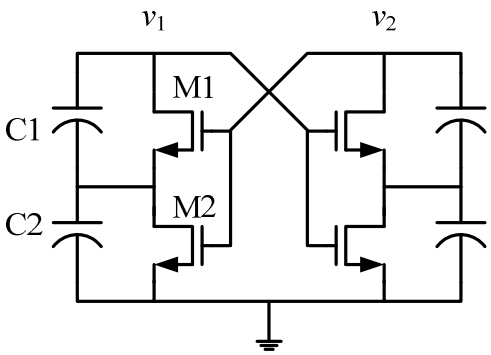


Fig 5.9: Differential self-cascode structure with capacitive feedback

5.4.2 Calculation of Negative Resistance with Capacitive Feedback

Fig 5.9 shows the self-cascode structure with capacitive feedback. Here again, v_1 and v_2 represent the differential output from the oscillator. The small signal analysis of this structure is depicted below.

Considering the bottom transistor as an ideal current source, the small signal equivalent circuit of the self-cascode structure with capacitive feedback is shown in Fig 5.10. With this structure the potential v_1 can be expressed as

$$v_1 = v_{C_1} + v_{C_2} \tag{5.9}$$

where $v_{C_2} = v_x = i_t \cdot \frac{1}{sC_2}$ and $v_{C_1} = \left\{ i_t - g_m \left(v_2 - i_t \cdot \frac{1}{sC_2} \right) \right\} \cdot \frac{1}{sC_1}$. Now using the values of v_{C1}, v_{C2} and using the condition $v_1 = -v_2$, the admittance of the self-cascode structure can be expressed as

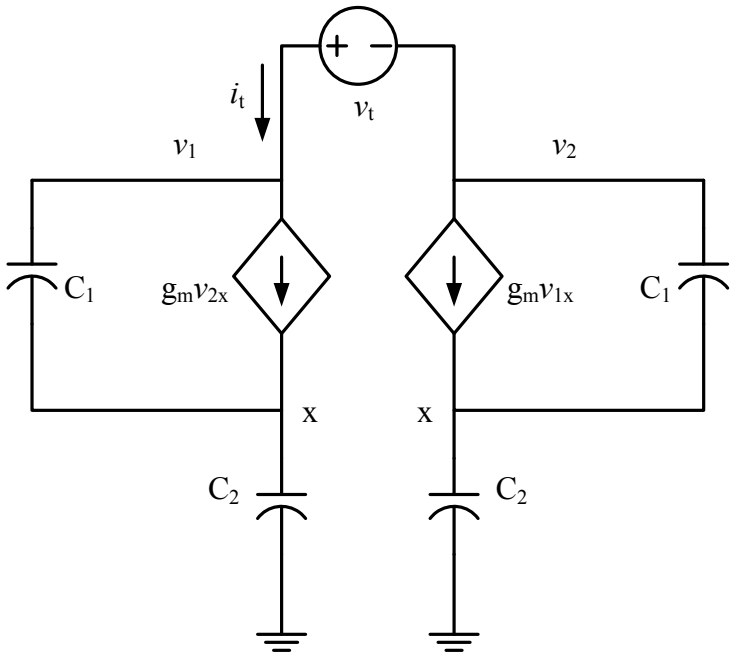


Fig 5.10: Small signal equivalent circuit of self-cascode structure with capacitive feedback (ideal current source approximation of bottom transistor)

$$Y_{in} = \frac{i_t}{v_1} = \frac{s^2 C_1 C_2 - g_m s C_2}{g_m + s(C_1 + C_2)} \tag{5.10}$$

Inserting s = jω, equation (5.10) can rewritten as

$$\begin{aligned} Y_{in} &= \frac{-\omega^2 C_1 C_2 - j\omega g_m C_2}{g_m + j\omega(C_1 + C_2)} \\ &= \frac{\left(-\omega^2 C_1 C_2 - j\omega g_m C_2\right) \cdot \{g_m - j\omega(C_1 + C_2)\}}{g_m + j\omega(C_1 + C_2)} \\ &= \frac{-\omega^2 g_m C_1 C_2 + j\omega^3 C_1 C_2 (C_1 + C_2) - j\omega g_m^2 C_2 - \omega^2 g_m C_2 (C_1 + C_2)}{g_m^2 + \omega^2 (C_1 + C_2)^2} \end{aligned} \tag{5.11}$$

Equating real and imaginary parts, one can get

$$\mathrm{Re}[Y_{in}] = \frac{-\omega^2 g_m C_1 C_2 - \omega^2 g_m C_2 (C_1 + C_2)}{g_m^2 + \omega^2 (C_1 + C_2)^2} = -\frac{\omega^2 g_m C_1 C_2 \left(2 + \frac{C_2}{C_1}\right)}{g_m^2 + \omega^2 (C_1 + C_2)^2} \tag{5.12}$$

$$\mathrm{Im}[Y_{in}] = \frac{\omega^3 C_1 C_2 (C_1 + C_2) - \omega g_m^2 C_2}{g_m^2 + \omega^2 (C_1 + C_2)^2} \tag{5.13}$$

From equation (5.12), it is obvious that total transconductance of the self-cascode structure is boosted up by the capacitance ratio.

Now considering the bottom MOSFET of Fig 5.9 as a regular transistor, the small signal equivalent circuit can be represented as shown in Fig 5.11. Again using the conditions $v_t = v_1 - v_2$, $v_1 = -v_2$ and $v_x = (i_t - g_{m2} v_2) \cdot \frac{1}{sC_2}$, the admittance equation becomes

$$Y_{in} = \frac{s^2 C_1 C_2 - s(g_{m1} C_2 + g_{m2} C_1) - g_{m1} g_{m2}}{g_{m1} + s(C_1 + C_2)} \tag{5.14}$$

Inserting s = jω in equation (5.14), one can get

$$Y_{in} = \frac{-\omega^2 g_{m1}C_1C_2 - j\omega g_{m1}\left(g_{m1}C_2 + g_{m2}C_1\right) - g_{m1}^2 g_{m2} + j\omega^3 C_1C_2\left(C_1 + C_2\right)}{g_{m1}^2 + \omega^2\left(C_1 + C_2\right)^2} + \frac{-\omega^2\left(g_{m1}C_2 + g_{m2}C_1\right)\left(C_1 + C_2\right) + j\omega g_{m1}g_{m2}\left(C_1 + C_2\right)}{g_{m1}^2 + \omega^2\left(C_1 + C_2\right)^2} \quad \textbf{(5.15)}$$

Equating real part of Y_{in},

$$\mathrm{Re}\left[Y_{in}\right] = -\frac{\omega^2 g_{m1}C_1C_2\left\{1 + \frac{g_{m1}C_2 + g_{m2}C_1}{g_{m1}} \cdot \left(\frac{C_1 + C_2}{C_1C_2}\right) + \frac{g_{m1}g_{m2}}{\omega^2 C_1C_2}\right\}}{g_{m1}^2 + \omega^2\left(C_1 + C_2\right)^2} \quad \textbf{(5.16)}$$

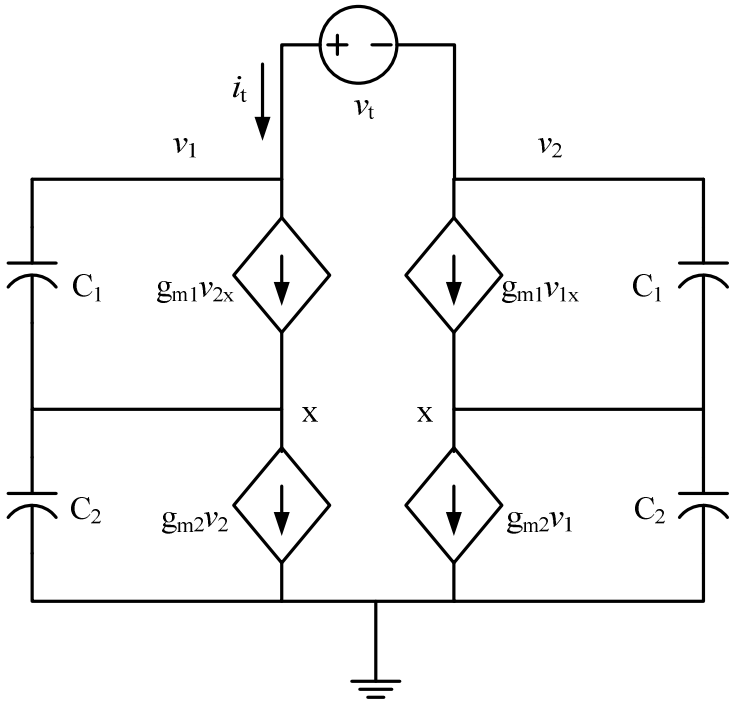


Fig 5.11: Small signal equivalent circuit of self-cascode structure with capacitive feedback

If $g_{m1} > g_{m2}$ and $C_2 > C_1$ then equation (5.16) can be simplified as

$$\mathrm{Re}\left[Y_{in}\right] = -\frac{\omega^2 g_{m1} C_1 C_2 \left\{1 + \frac{g_{m1} C_2}{g_{m1}} \cdot \left(\frac{C_1 + C_2}{C_1 C_2}\right) + \frac{g_{m1} g_{m2}}{\omega^2 C_1 C_2}\right\}}{g_{m1}^2 + \omega^2 \left(C_1 + C_2\right)^2} \qquad \textbf{(5.17)}$$

After simple mathematical manipulation, equation (5.17) can be rewritten as

$$\mathrm{Re}\left[Y_{in}\right] = -\frac{\omega^2 g_{m1} C_1 C_2 \left\{\left(2 + \frac{C_2}{C_1}\right) + \frac{g_{m1} g_{m2}}{\omega^2 C_1 C_2}\right\}}{g_{m1}^2 + \omega^2 \left(C_1 + C_2\right)^2} \qquad \textbf{(5.18)}$$

Equation (5.18) is similar to equation (5.12). The only difference is the additional term $\frac{g_{m1} g_{m2}}{\omega^2 C_1 C_2}$ that indicates the dependency of total transconductance not only on the capacitance ratio but also on the transconductances of the individual MOSFETs of the self-cascode structure.

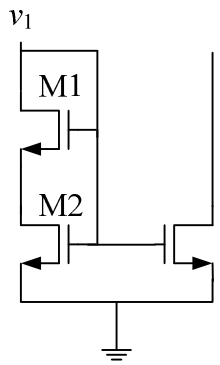


Fig 5.12: Self-cascode structure used in a current mirror

5.5 Calculation of MOSFET Dimensions in Self-Cascode Structure

Fig 5.12 shows the circuit diagram of a self-cascode structure used in a current mirror. To drive M_2 into saturation, one needs to satisfy

$$\begin{aligned} & v_{ds2} \geq v_{gs2} - v_t \\ & \Rightarrow v_{ds2} \geq \left(v_{gs1} - v_{ds2}\right) - v_t \\ & \therefore v_{gs1} \leq v_t \end{aligned} \tag{5.19}$$

That means M_1 transistor will operate in either moderate or weak inversion region. If L_1=$L_{\min}$ then L_2>$L_{\min}$ and W_1>W_2 are chosen to drive both M_1 and M_2 into saturation. This requires $v_{ds,sat} = \dfrac{v_{gs} - v_t}{n}$, where $n = 1 + \dfrac{\gamma}{2\sqrt{v_{sb} + 2\phi_F}}$ *where* γ *body factor*

Assume no body effect for M_1 and L_1=L_2, v_{t1}= v_{t2} = v_t

$$\frac{\beta_2}{2} \cdot \frac{\left(v_{gs2} - v_t\right)^2}{n} = \frac{\beta_1}{2} \cdot \frac{\left(v_{gs1} - v_t\right)^2}{n} \tag{5.20}$$

From the circuit diagram as shown in Fig 5.12,

$$v_{ds2} = v_{gs2} - v_{gs1} \tag{5.21}$$

For typical value of n =1.3 and for saturation condition (see Appendix A),

$$\boxed{\frac{\beta_1}{\beta_2} \geq 18.46 \quad \Rightarrow \frac{\beta_1}{\beta_2} \approx 20 \quad \therefore \beta_1 \approx 20\beta_2} \tag{5.22}$$

From equation (5.22) it is seen that the top MOSFET of the self-cascode structure has to be made 20 times larger than that of the bottom MOSFET.

Now, if body effect is considered then

$$V_{T1} > V_{T2} \ \ and \ \ n_1 < n_2$$

$$\frac{\beta_2}{2} \cdot \frac{(v_{GS2} - V_{T2})^2}{n_2} = \frac{\beta_1}{2} \cdot \frac{(v_{GS1} - V_{T1})^2}{n_1} \tag{5.23}$$

Here the condition for saturation can be defined as $v_{DS2} = v_{GS2} - v_{GS1} \geq \frac{v_{GS2} - v_{T2}}{n_2}$. Now, from Appendix B, the MOSFET dimension for self-cascode structure can be found as,

$$\boxed{\therefore \frac{\beta_1}{\beta_2} \geq \frac{n_1}{n_2} \cdot \left(\frac{n_2 - 1}{n_2} + \frac{V_{T2} - V_{T1}}{v_{GS2} - V_{T2}} \right)^{-2}} \tag{5.24}$$

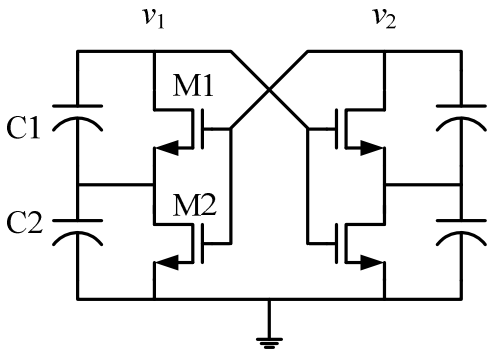


Fig 5.13: Differential self-cascode structure with capacitive feedback

From equation (5.24) it can be shown that both M_1 and M_2 can be driven into saturation for $\beta_1=5\beta_2$.

If capacitive feedback is used with self-cascode structure, it helps to boost the g_m of the structure and to provide better phase noise performance due to Colpitts oscillator structure. Fig 5.13 shows the differential self-cascode structure with capacitive feedback which will ultimately be used to develop an LC oscillator. Using Cadence Spectre™ simulation, it is shown that at the highest point of oscillation, both M_1 and M_2 transistors of the self-cascode structure operate in linear region. Based on this, a good approximation of the size of the MOSFETs can be determined using first order MOSFET drain current equation.

Let '*A*' be the highest oscillation amplitude, V_{t1} and V_{t2} are the threshold voltages of M_1 and M_2, and V_{DD} is the supply voltage. Since equal current flow through M_1 and M_2,

$$\beta_1\left\{\left(v_{GS1}-V_{T1}\right)v_{DS1}-\frac{1}{2}v_{DS1}^2\right\}=\beta_2\left\{\left(v_{GS2}-V_{T2}\right)v_{DS2}-\frac{1}{2}v_{DS2}^2\right\} \qquad \textbf{(5.25)}$$

Since $v_{DS}<<(v_{GS}-V_T)$ in the linear region, one can use approximation of the above equation as

$$\begin{aligned}
\frac{\beta_1}{\beta_2} &= \frac{(v_{GS2}-V_{T2})}{(v_{GS2}-V_{T2})}\cdot\frac{v_{DS2}}{v_{DS2}} \\
&= \frac{(V_{DD}+A-V_{T2})}{(V_{DD}+A+nA-V_{T1})}\cdot\frac{C_1}{C_2} \\
&= \frac{(V_{DD}+A-V_{T2})}{V_{DD}+A-V_{T2}+nA-(V_{T1}-V_{T2})}\cdot\frac{C_1}{C_2} \\
&= \frac{1}{1+\dfrac{nA-(V_{T1}-V_{T2})}{V_{DD}+A-V_{T2}}}\cdot\frac{C_1}{C_2} \\
\therefore \frac{\beta_1}{\beta_2} &= \left\{1-\frac{nA-(V_{T1}-V_{T2})}{V_{DD}+A-V_{T2}}\right\}\cdot\frac{C_1}{C_2}
\end{aligned} \tag{5.26}$$

where $n=\dfrac{C_1}{C_1+C_2}$. Now inserting the value of n, equation (5.26) can be rewritten as

$$\therefore \frac{\beta_1}{\beta_2} = \frac{C_1}{C_2}\left\{1-\frac{\dfrac{C_1}{C_2}}{1+\dfrac{C_1}{C_2}}\frac{A}{V_{DD}+A-V_{T2}}+\frac{(V_{T1}-V_{T2})}{V_{DD}+A-V_{T2}}\right\} \tag{5.27}$$

Again $g_{m1}=\sqrt{2\cdot\beta_1\cdot I}$ and $g_{m2}=\sqrt{2\cdot\beta_2\cdot I}$. Since equal current is flowing through the self-cascode structure

$$\therefore \frac{g_{m1}}{g_{m2}} = \sqrt{\frac{C_1}{C_2}\left\{1 - \frac{\frac{C_1}{C_2}}{1+\frac{C_1}{C_2}}\frac{A}{V_{DD}+A-V_{T2}} + \frac{(V_{T1}-V_{T2})}{V_{DD}+A-V_{T2}}\right\}} \quad \textbf{(5.28)}$$

$$\therefore g_{m1} = k \cdot g_{m2} \quad \textbf{(5.29)}$$

where $k = \sqrt{\frac{C_1}{C_2}\left\{1 - \frac{\frac{C_1}{C_2}}{1+\frac{C_1}{C_2}}\frac{A}{V_{DD}+A-V_{T2}} + \frac{(V_{T1}-V_{T2})}{V_{DD}+A-V_{T2}}\right\}}$

Since $\beta = \mu \cdot C_{ox} \cdot \frac{W}{L}$, one can easily get

$$\therefore \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2} = \frac{C_1}{C_2}\left\{1 - \frac{\frac{C_1}{C_2}}{1+\frac{C_1}{C_2}}\frac{A}{V_{DD}+A-V_{T2}} + \frac{(V_{T1}-V_{T2})}{V_{DD}+A-V_{T2}}\right\} \quad \textbf{(5.30)}$$

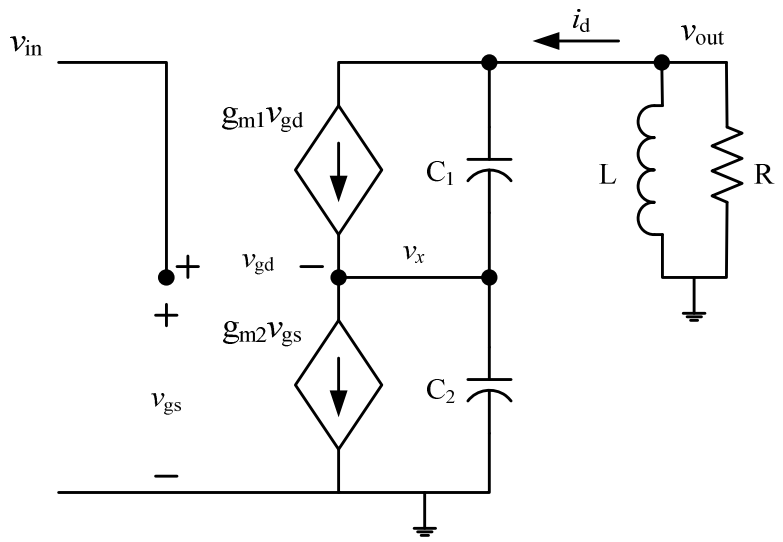


Fig 5.14: Small signal equivalent circuit of self-cascode oscillator

5.6 Calculation of the Oscillation frequency and the Required Transconductance

Fig 5.14 shows the small signal equivalent circuit of a self-cascode LC oscillator circuit. Here $v_{gs} = v_{in}$ and $v_{gd} = v_{in} - v_x$. Therefore the node voltage v_x can be given as

$$v_x = \left(i_d - g_{m2} v_{in}\right) \cdot \frac{1}{sC_2} \tag{5.31}$$

From Appendix C, the transfer function of the circuit can be expressed as

$$\frac{v_{out}}{v_{in}} = -\frac{\{sg_{m1}C_2 + g_{m2}(g_{m1} + sC_1)\}}{\left\{\left(\frac{R+sL}{sLR}\right)(g_{m1} + sC_1 + sC_2) + s^2C_1C_2\right\}} \quad \textbf{(5.32)}$$

For sustained oscillation, $\frac{v_{out}}{v_{in}} = -1$. Using this condition and equating real and imaginary parts of the transfer function, Appendix C gives,

$$\omega^2 = \frac{g_{m1}R}{L(C_1 + C_2) - LR(g_{m1}C_2 + g_{m2}C_1)} \quad \textbf{(5.33)}$$

and

$$\omega^2 = \frac{R(C_1 + C_2) + g_{m1}L - g_{m1}g_{m2}LR}{LRC_1C_2} \quad \textbf{(5.34)}$$

Assuming $g_{m2}R << 1$ and $R(C_1 + C_2) >> g_{m1}L$ the frequency of oscillation becomes

$$\omega^2 = \frac{R(C_1 + C_2)}{RLC_1C_2} = \frac{1}{L \cdot \frac{C_1C_2}{C_1 + C_2}} \quad \textbf{(5.35)}$$

If a varactor C_v is added to the drain terminals of top MOSFETs, then the equation becomes

$$\omega^2 = \frac{R(C_1 + C_2)}{RLC_1C_2} = \frac{1}{L \cdot \left(\frac{C_1C_2}{C_1 + C_2} + C_v \right)} \tag{5.36}$$

Inserting the value of ω^2 from equation (5.40) into equation (5.39), gives (Appendix C)

$$\frac{1}{L \cdot \frac{C_1C_2}{C_1 + C_2}} = \frac{g_{m1}R}{L(C_1 + C_2) - LR(g_{m1}C_2 + g_{m2}C_1)}$$

$$\therefore g_{m1}R = \frac{\left(1 + \frac{C_2}{C_1}\right)\left(1 + \frac{C_1}{C_2}\right)}{1 + \left(1 + \frac{C_2}{C_1}\right)\left(1 + \frac{1}{k}\frac{C_1}{C_2}\right)} \tag{5.37}$$

Table 5.2: Simulated transconductance variation with capacitance ratio

C_1/C_2	$(W/L)_1$	$(W/L)_2$	Required Transconductance (mS)
2	34	25	3.258
3	41	25	3.617
4	48	25	4.374
5	56	25	4.61

Table 5.2 depicts the transconductance variation of a self-cascode LC oscillator with different capacitance ratios for the same output swing. Higher the capacitance ratio (C_1/C_2) higher is the required transconductance to maintain equal output swing.

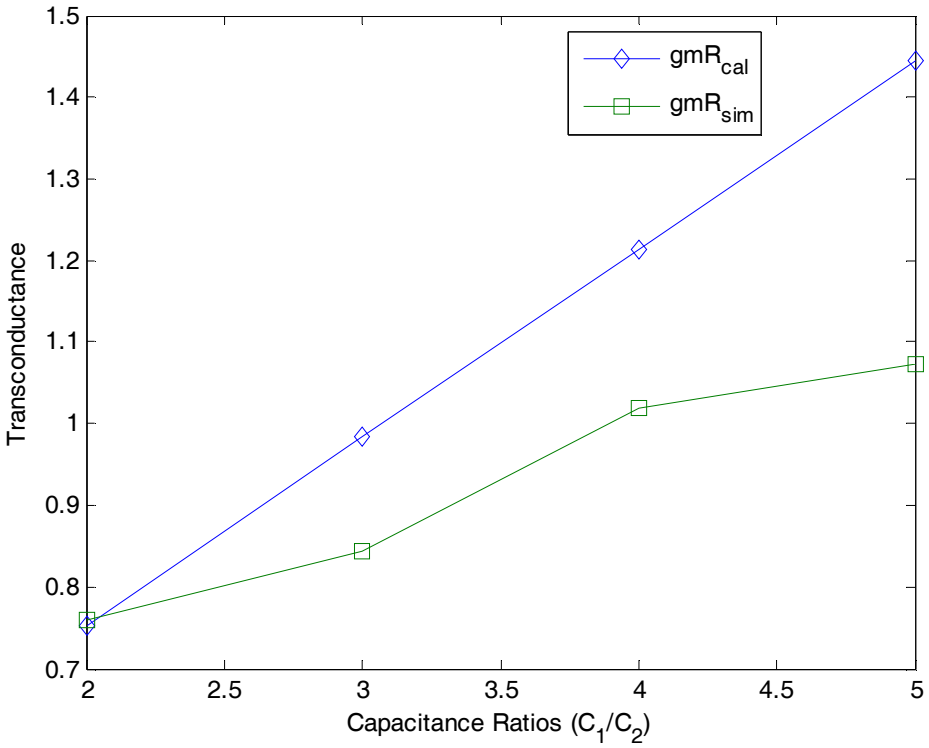


Fig 5.15: Simulated and calculated transconductance of the self-cascode structure`

A graphical plot of calculated (using.equation (5.37)) and simulated (using Cadence Spectre^{TM}) transconductance of the self-cascode oscillator is shown in Fig 5.15: It is obvious from the plots that the calculated values overestimate the simulated values. This is because of the simple MOS model used for the hand calculation.

5.7 Phase Noise Variation with Capacitance Ratio

Phase noise is an important design parameter for the design of any oscillator. As a simple mathematical model of phase noise in an LC oscillator, noise generated in the LC tank and inside the active devices are considered and compared with the signal power.

Frequency domain representation of this ratio represents the phase noise of the oscillator. Now the noise generated in the self-cascode LC oscillator can be represented as

$$N(\Delta\omega) = \left\{\frac{4kT}{R}(1+\gamma)\right\} \cdot \left(\frac{R}{2 \cdot Q \frac{\Delta\omega}{\omega}}\right)^2 \tag{5.38}$$

where R is the effective resitance of the tank, k is the Boltzman constant, T is the temperature in Kelvin, Q is the quality factor of the tank, ω is the angular frequency of oscillation, $\Delta\omega$ is the angular frequency offset from ω and γ is the drain noise current coefficient.

If the amplitude of the output signal is considered to be 'A', the signal power can be expressed as

$$P_{sig} = \frac{A^2}{2} \tag{5.39}$$

Using equations (5.38) and (5.39), the phase noise expression of the self-cascode LC oscillator can be depicted as

$$P(\Delta\omega) = 10\log_{10}\left[\left\{\frac{4kT}{R} \cdot (1+\gamma)\right\} \cdot \frac{2}{A^2} \cdot \left(\frac{R}{2 \cdot Q \cdot \frac{\Delta\omega}{\omega}}\right)^2\right] \tag{5.40}$$

In equation (5.40) the terms which vary with capacitance ratios are the output swing, A and the oscillation frequency, ω. The other parameters such as Q and R are assumed to be constant irrespective of the capacitance ratio. Based on this the next focus goes to the calculation of the output swing with capacitance ratio.

5.8 Amplitude Variation with Capacitance Ratio

The output amplitude of a self-cascode LC oscillator can be simply calculated by assuming perfect switching of the self-cascode structure. The output voltage swing of the VCO is derived from the time-domain waveform of the drain current $I_1(t)$, as shown in Fig 5.16.

For simplicity, the periodic drain current is modeled by a square wave with a period of $T_o=\omega/(2\pi)$ and an amplitude of I_o. I_o is approximated by the maximum drain current with

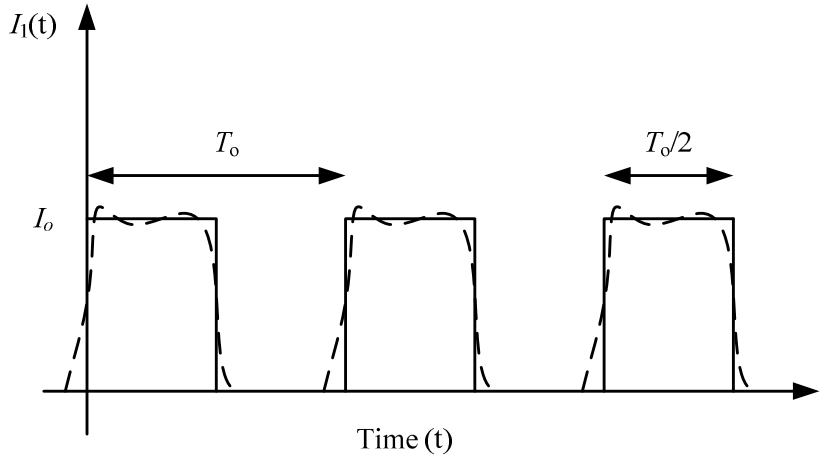


Fig 5.16: Actual and modeled drain current waveform (dashed for actual and solid for model)

the transistor operating in the linear region. It should be noted that, at the quiescent point, the transistors are biased at $V_{d1}=V_{d2}=V_{DD}$ (see Fig 5.16). The maximum drain current occurs when the gate voltage reaches its peak value. Assuming that the amplitude of output oscillating signal is A and the gate voltages V_{gs1} and V_{gs2} are $V_{DD}+A$ and $V_{DD}-A$, respectively.

From the Fourier series of $I_1(t)$, the fundamental current is given by

$$I_1(t)|_{fundamental} \approx \frac{2}{\pi} I_o \sin(\omega t) \tag{5.41}$$

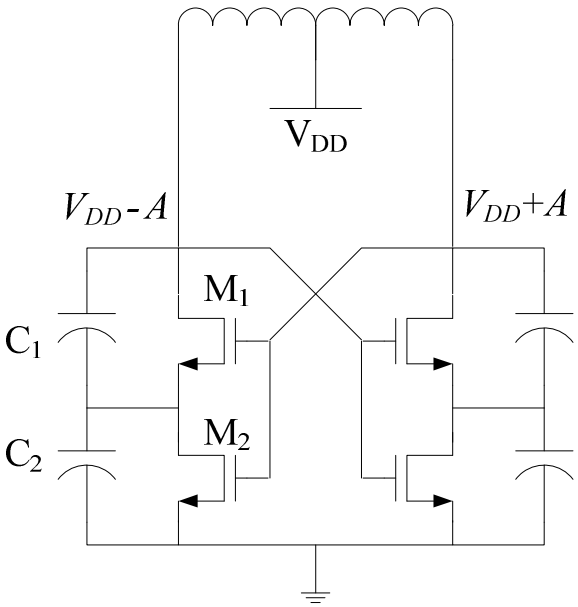


Fig 5.17: Self-cascode LC oscillator

And the fundamental voltage amplitude is

$$V_{DD} - A \approx \frac{2}{\pi} I_o R \tag{5.42}$$

Now,

$$\begin{aligned} & V_{DD} - A = \frac{2}{\pi} I_o R \\ & \Rightarrow V_{DD} - A = \frac{2}{\pi} R \cdot \mu_n C_{ox} \left(\frac{W}{L} \right)_2 \left\{ \left(v_{GS2} - V_{T2} \right) v_{DS2} - \frac{1}{2} v_{DS2}^2 \right\} \\ & \Rightarrow V_{DD} - A = \frac{2}{\pi} R \cdot \mu_n C_{ox} \left(\frac{W}{L} \right)_2 \left\{ \left(V_{DD} + A - V_{T2} \right) \left(-nA \right) - \frac{1}{2} \left(nA \right)^2 \right\} \end{aligned} \tag{5.43}$$

After simplification, the expression for output amplitude can be defined as

$$A = \frac{-M \pm \sqrt{M^2 - 4P \left(\frac{1}{2} \cdot \frac{1}{1 + \frac{C_2}{C_1}} + 1 \right) \cdot V_{DD}}}{2P \left(\frac{1}{2} \cdot \frac{1}{1 + \frac{C_2}{C_1}} + 1 \right)} \tag{5.44}$$

where $P = \frac{2n}{\pi} R \cdot \mu_n C_{ox} \left(\frac{W}{L} \right)_2$, $n = C_1/(C_1+C_2)$ and $M = P(V_{DD}-V_{t2})-1$ and V_{t2} is the threshold voltage of the transistor M_2.

Now inserting the values from equations (5.44) and (5.35) into equation (5.40) the phase noise variation with the capacitance ratio can be found. A graphical plot of phase noise variation with capacitance ratio using equation (5.40) is shown in Fig 5.18. Cadence Virtuoso-Spectre-RF is also used to perform the phase noise simulation of the self-cascode oscillator for different capacitance ratios. Fig 5.19 shows the simulated phase noise of the self-cascode oscillator with different capacitance ratios for different process corners. Fig 5.19 clearly indicates an upward trend with capacitance ratios i.e. phase noise increases with the capacitance ratios. For small values of the capacitance ratio and lower power supply voltage, the simulated (using Cadence Virtuoso-Spectre-RF) phase noise plot shows a minimum value and beyond that phase starts to increase with the capacitance ratios. This is also evident from the calculated phase noise plot as shown in Fig 5.18. Therefore, the calculated phase noise plot indicates a close match to the trends of phase noise variation with the capacitance ratios.

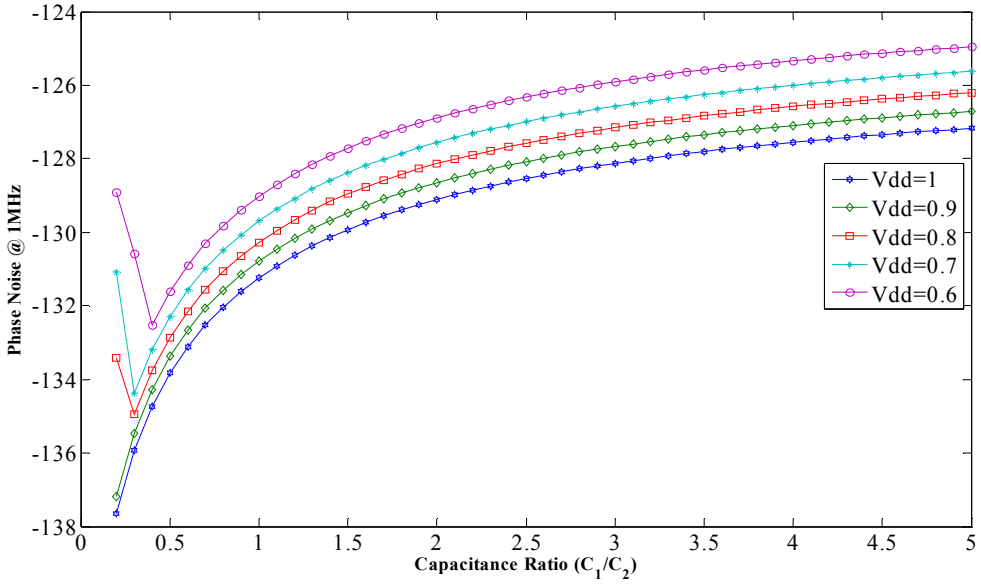


Fig 5.18: MATLAB simulation results of phase noise variation with capacitance ratios

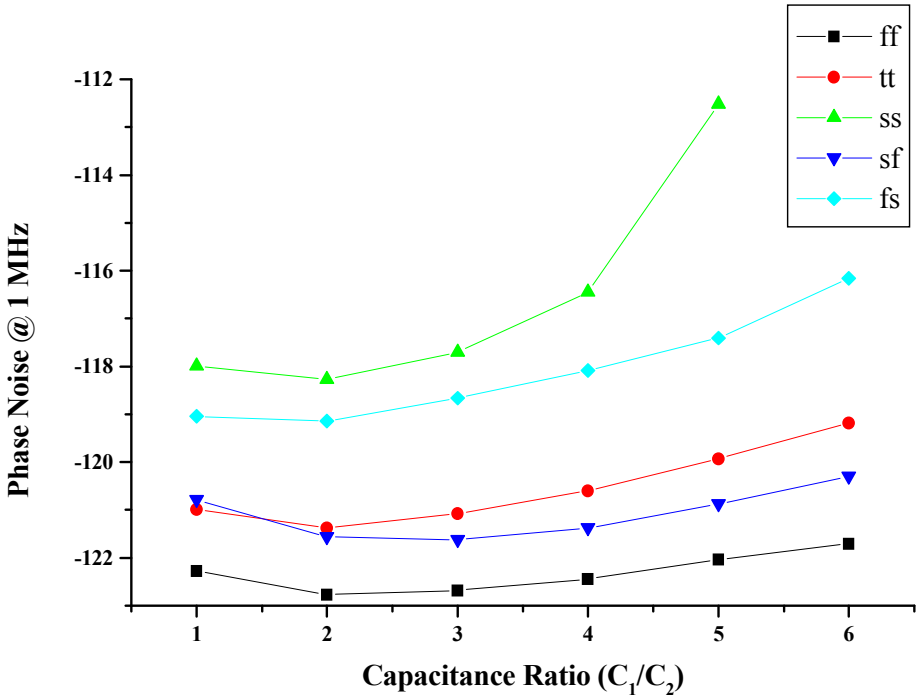


Fig 5.19: Cadence Virtuoso-Spectre-RF simulation results of phase noise variation with different capacitance ratios

5.9 Self-Cascode Oscillator and Performance Comparison

Based on the above analyses, a self-cascode LC oscillator with body-terminal coupling is designed using IBM7RF CMOS process. The minimum feature size of this process is 0.18-μm and it provides on-chip inductor option. Therefore, for inductor and varactor, the library standard inductor and varactor are used.

The complete schematic of the designed circuit is shown in Fig 5.20. Here PMOS devices (M1 and M2) have been used in the core oscillator block to achieve low flicker noise and easy access to the body terminals of the devices. Transistors M3 have been incorporated in the design to achieve ASK modulation of the data signal. The oscillator operates normally as long as the data signal is low. But whenever the data signal is high the outputs of the oscillator are shorted to ground through M3 transistors. Thus a ASK

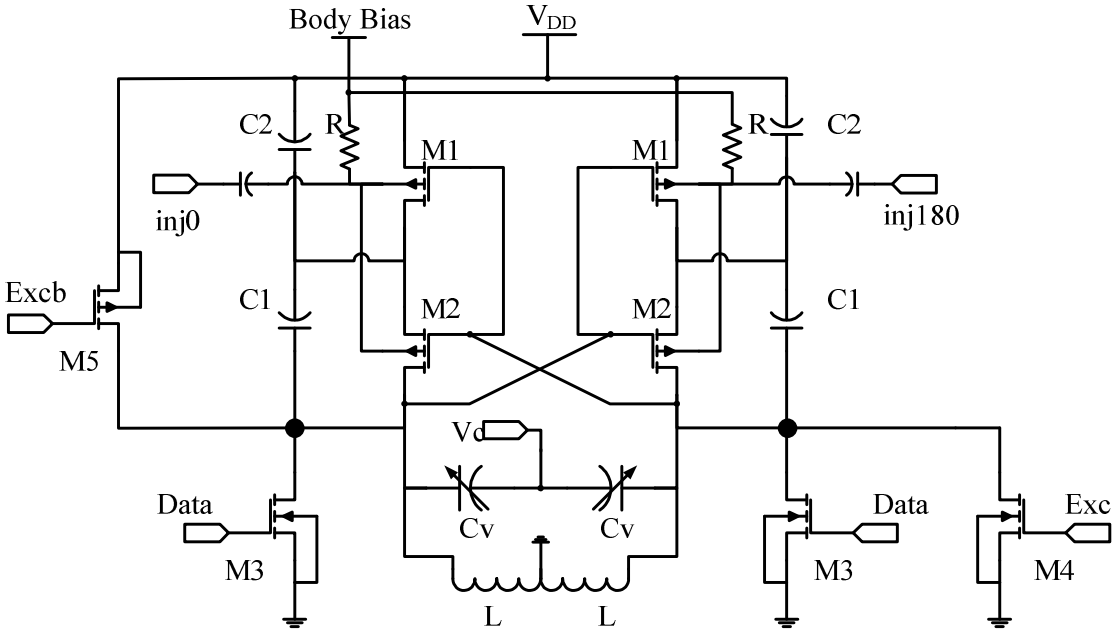


Fig 5.20: Schematic of the designed self-cascode body-coupled LC oscillator with data incorporation capability

scheme is achieved based on the data signal. Transistors M4 and M5 are used during startup to ensure reliable startup of oscillation. When the excitation signal is high both M4 and M5 are on and a current is injected to the LC tank which helps to start the oscillation reliably. To drive the package pads and the output matching network, a buffer is also incorporated with the main LC oscillator. Table 5.3 shows the device dimensions and capacitance values of the feedback network used in the designed circuit. Efforts have been made to optimize the device dimension and capacitance values through simulations to achieve low-voltage low-power operation while maintaining the desired output frequency and phase noise performance. A performance comparison of the designed self-cascode oscillator with other previously reported LC oscillator circuits is shown in Table 5.4.

Table 5.3: Device dimension and component values for self-cascode oscillator

M_1 (W/L)	24 μm/0.18 μm
M_2 (W/L)	48 μm/0.18 μm
C_1	201 fF
C_2	128 fF
M_3 (W/L)	6 μm/0.18 μm
M_4 (W/L)	1.2 μm/0.18 μm
M_5 (W/L)	3 μm/0.18 μm

Table 5.4: Comparison of self-cascode LC oscillator with existing LC Oscillators

Ref.	Process(µm)	Supply (V)	Power (mW)	Frequency (GHz)	Phase Noise (-dBc/Hz)	No of L	Current (mA)	CFOM[1]	MFOM[2]
[63]	0.18	1.6	0.688	0.99-1.21	79.7@50KHz	2	0.43	168.173	225.40
[64]	0.18	1.8	32	19.9	111@1MHz	4	17.77	181.926	199.78
[51]	0.18	2.0	7.2	1.59-1.98	128@1MHz	2	3.6	184.036	220.86
[65]	0.18	0.63	2.94	4.2	113@1MHz	2	4.6	180.78	225.39
[66]	0.18	1.8	4.5	4.024	108@1MHz	2	2.5	173.56	214.47
[67]	0.18	1.8	12.6	16.5	115@1MHz	4	7	188.35	214.29
[68]	0.18	0.6	3	5.6	118@1MHz	4	5	188.193	226.60
[69]	0.18	0.6	0.7	5.8	97@1MHz	2	1.16	173.82	230.89
[70]	0.18	1.5	3	4.8	120@1MHz	2	2	188.85	233.29
[71]	0.18	2.2	50	10.3	125.33@1MHz	2	22.72	188.60	208.59
[72]	0.18	0.85	6	8.7	100@600KHz	6	7.05	175.45	204.32
This Work	0.18	**0.8**	**0.714**	1.45	118.03@1MHz	**2**	**0.89**	**182.74**	**239.64**

Here,

$$^{1}CFOM = -PN + 20\log_{10}\left(\frac{f_o}{f_m}\right) - 10\log_{10}\left(\frac{P_{dc}}{1mW}\right)$$

$$^{2}MFOM = -PN + 20\log_{10}\left(\frac{f_o}{f_m}\right) - 10\log_{10}\left(\frac{P_{dc}}{1mW}\right) - 20\log_{10}\left(nL \times V_{\sup ply} \times I_{dc}\right)$$

To compare the performance of the proposed work, two figure-of-merit (FOM) formulations have been used. The well-known conventional figure-of-merit (CFOM) of oscillator is expressed as

$$CFOM = -PN + 20\log_{10}\left(\frac{f_o}{f_m}\right) - 10\log_{10}\left(\frac{P_{dc}}{1mW}\right) \quad \textbf{(5.45)}$$

In CFOM formulation only power consumption, frequency and phase noise are considered but there is no knowledge of supply voltage and current drawn of the circuit. In portable devices battery ampere-hour life is the defining parameter to determine the longevity of system performance. Therefore, both voltage and current requirements need to be incorporated in the CFOM formulation. In addition, the number of inductors is also important because they take the most of the valuable chip area. Hence, the modified FOM (MFOM) has been formulated which can be written as

$$MFOM = -PN + 20\log_{10}\left(\frac{f_o}{f_m}\right) - 10\log_{10}\left(\frac{P_{dc}}{1mW}\right) - 20\log_{10}\left(nL \times V_{\sup ply} \times I_{dc}\right) \quad \textbf{(5.46)}$$

where *nL* represents the number of inductors used in the circuit. Fig 5.21 shows the comparison of conventional figure-of-merit (CFOM) of previously published works with the proposed work. From Fig 5.21 it is seen that with CFOM five previously published works have better performance than that of the proposed work. Fig 5.22 depicts the modified figure of merit (MFOM) of previously published works with the proposed

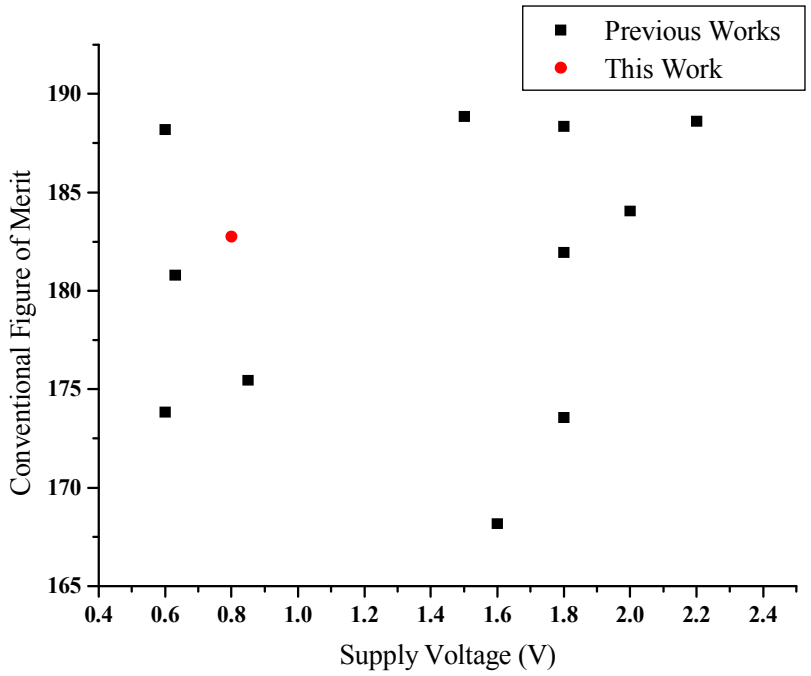


Fig 5.21: Conventional FOM of previously published works with respect to their operating voltages

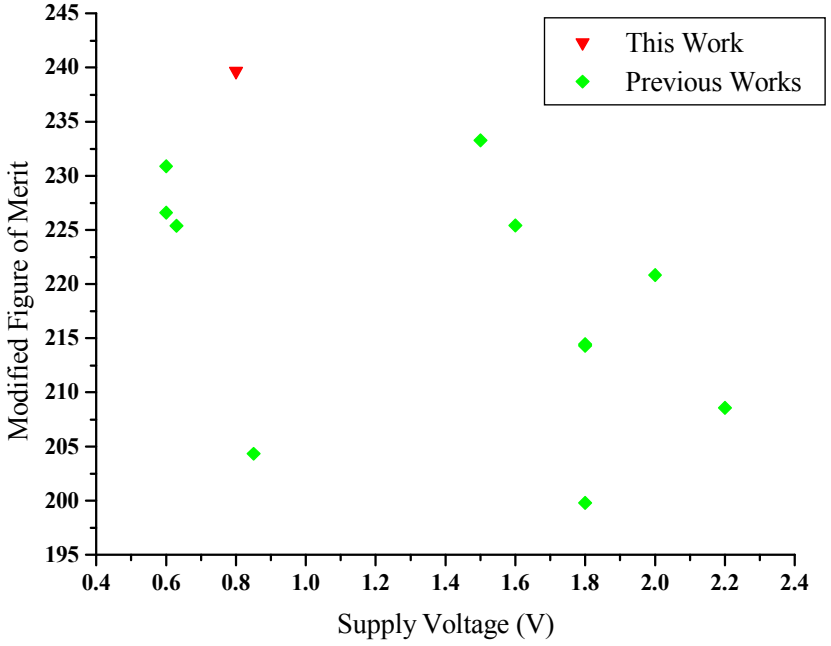


Fig 5.22: Modified FOM of previously published works with respect to their operating voltages

work. It is obvious from the MFOM plot that the proposed design outperforms all of the previously published works and demonstrates its effectiveness in low-voltage low-power portable device applications.

5.10 Summary

Low-voltage low-power oscillator design is a vital factor for the development of a low-power injection-locked transmitter. Conventional cross-coupled structures can exhibit either low-voltage or low-power operation. On the other hand, self-cascode structure facilitates with both low-voltage and low-power operation. Therefore this chapter has presented detailed mathematical analyses and computer simulation of a self-cascode structure based LC oscillator. The analyses include the calculation of optimal MOSFET dimension, the equation of frequency of oscillation, the required transconductance to startup and the phase noise variation with capacitance ratios. Finally to compare the performance of the designed circuit, a modified figure-of-merit expression has been formulated where supply voltage, current and number of inductors .have been taken into consideration. Based on this modified figure-of-merit formulation, it is seen that the designed oscillator circuit outperforms all of the previously published works of same type.

Chapter 6 Layout, Simulation and Measurement Results

6.1 Introduction

The self-cascode body-coupled oscillator can facilitate low-voltage low-power operation. The proposed LC oscillator circuit has been designed and fabricated using IBM7RF process. The minimum feature size of the process is 0.18 μm. The foundry provided inductors and varactors have been used to design and layout the circuit. The foundry provided PMOS devices with double gate connections have also been used to layout the self-cascode structure.

The quality factor of on-chip inductor is the dominant factor to achieve better phase noise performance and to reduce oscillator power consumption. To achieve better quality factor of the inductor, all the analog blocks are kept at least 80 μm away from the inductor layout. The grounded guard ring of the inductor is also used to eliminate any disturbance from the switching blocks. IBM7RF process uses special insulating layer beneath the inductor layout to reduce the capacitive coupling to the substrate and to eliminate the image current on the lossy substrate and essentially further improves the quality of the inductor. The foundry provided PMOS accumulation mode varactor is used with the inductor to form the LC tank and at the same time to tune the oscillation frequency. Special foundry provided 'tiedown' plugs are used to reduce antenna effects and other foundry requirements.

To bias the body terminal of the PMOS devices in the self-cascode structure, foundry provided precision polysilicon resistors are used. High dielectric constant metal-insulator-metal (MIM) capacitors are used to form the capacitive feed-back network in the self-cascode structure. MIM capacitors are also used with the body-bias resistors to facilitate with body terminal coupling. To achieve better matching of the PMOS devices in the self-cascode differential structure common centroid layout technique is utilized.

The output impedance of any LC oscillator is usually kept high to achieve better quality factor of the LC tank. Therefore, to drive any standard 50 Ω load an output buffer is needed. Fig 6.1 shows the circuit schematic of the output driver used with the self-cascode differential oscillator. The cascode structure of the output driver eliminates miller effects and provides better isolation of the LC oscillator from the output load. An LC tank was used as a load of the output driver where it resonates at the oscillation frequency of the self-cascode differential oscillator. To achieve better quality factor of the LC tank of the output driver, off-chip inductors and capacitors have been used. Fig 6.2 shows the microphotograph of the fabricated chip. It manifests self-cascode LC oscillator with body-coupling facility and the output driver. The core area consumption of the chip is 0.132 mm^2.

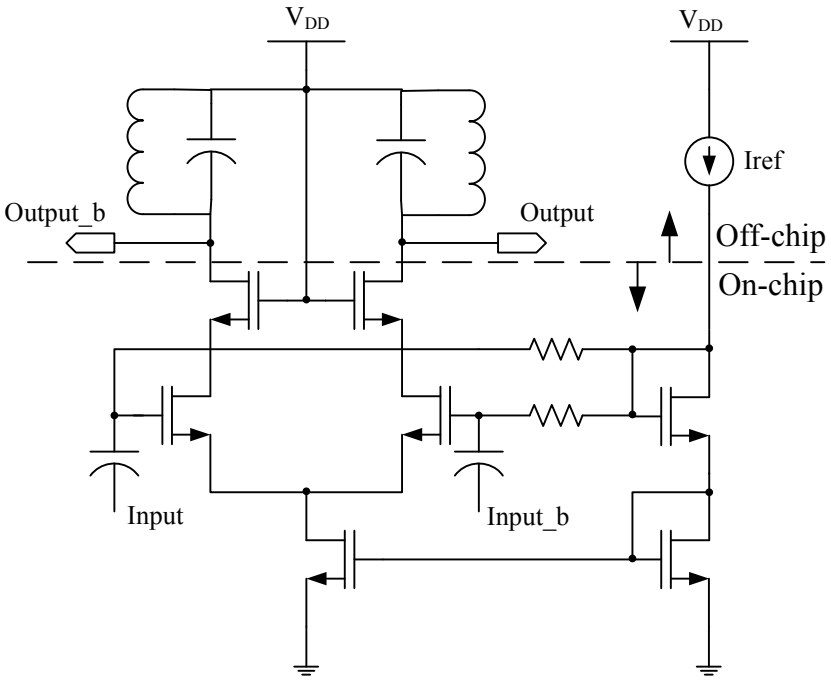


Fig 6.1: Schematic of output driver

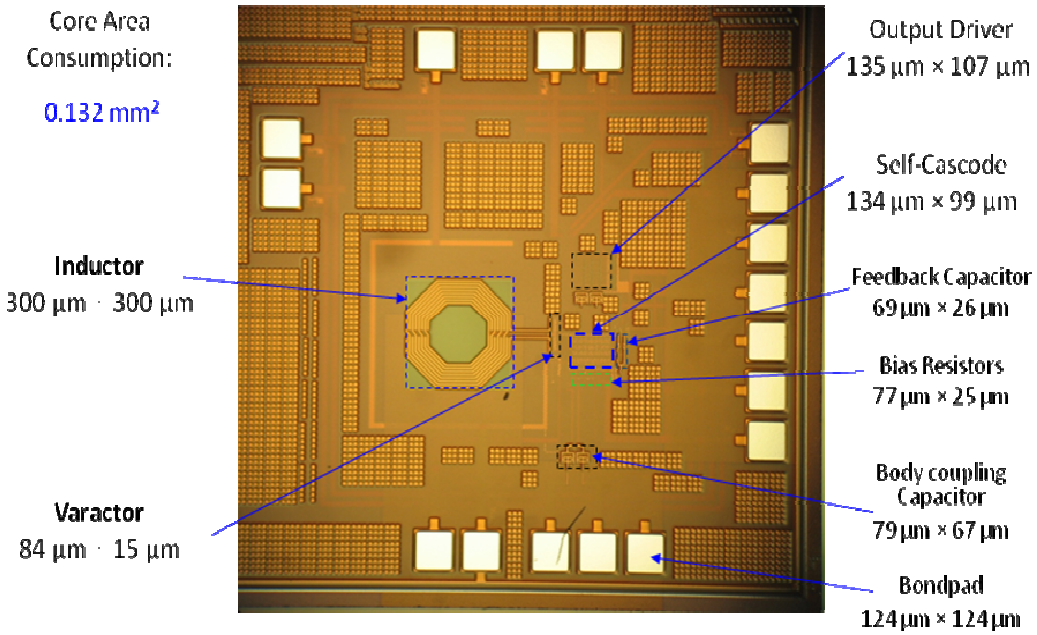


Fig 6.2: Microphotograph of the self-cascode LC oscillator

6.2 Test Results of Self-Cascode LC Oscillator

The designed self-cascode LC oscillator with body terminal coupling has been tested using Agilent 4407B spectrum analyzer. Fig 6.3 shows the test setup of the fabricated chip. To bias the circuit bias-T network is used to filter out the supply frequency in the power supply or in the control voltage line. Keithley 2400 source meter is used to generate the reference current for the output driver. To optimize the output impedance of the output driver tap-capacitor matching network is used which is shown in Fig 6.4. Miniature surface mount components (capacitors and inductors) and microstrip lines are used for better impedance matching and optimum power transfer to the 50 Ω load.

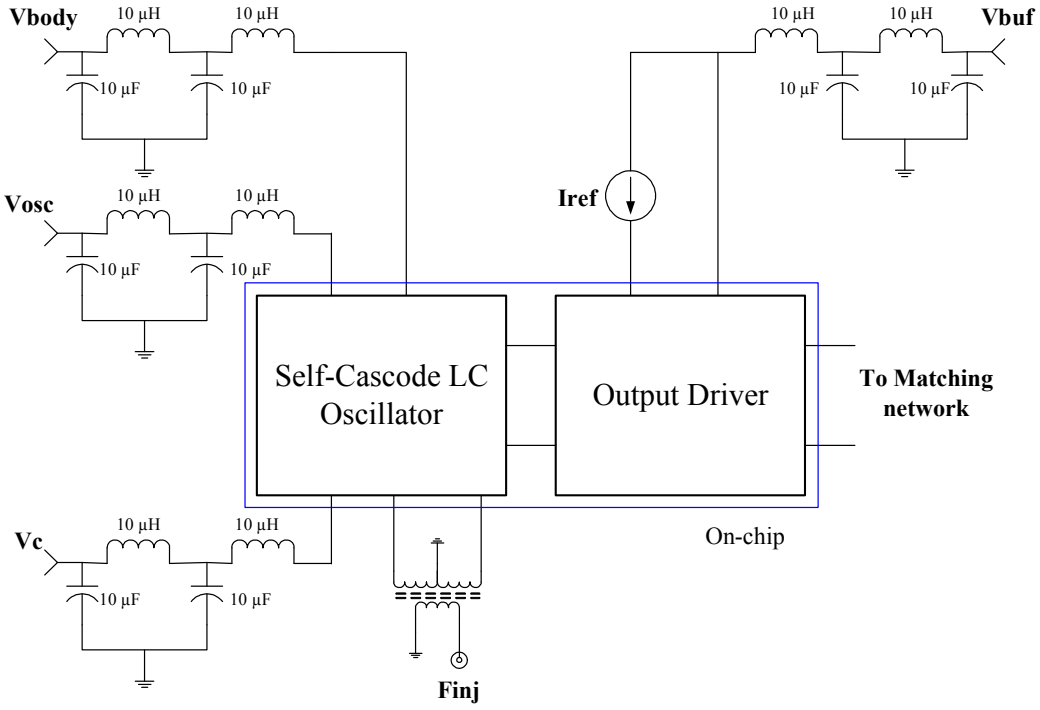


Fig 6.3: Test setup of self-cascode oscillator

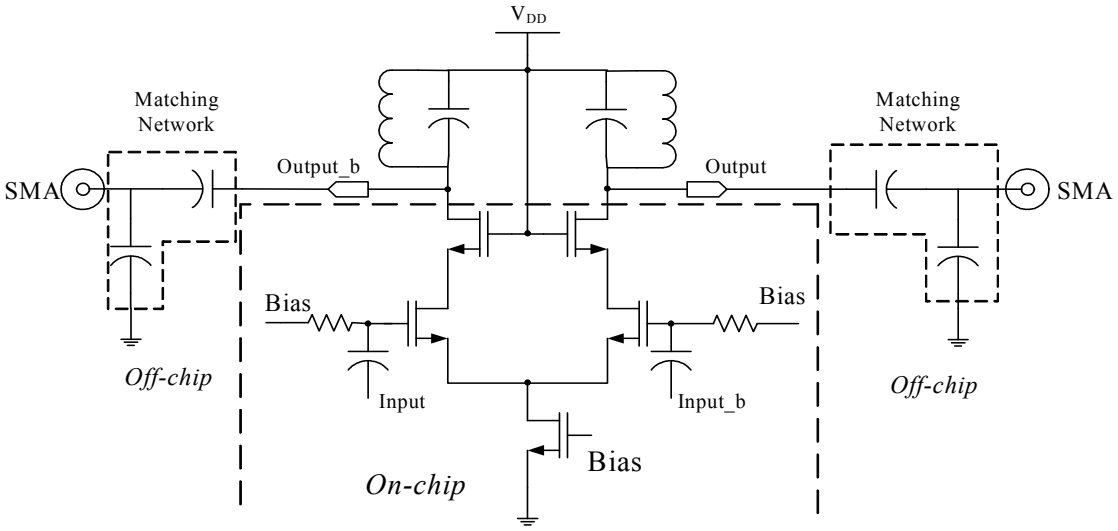


Fig 6.4: Schematic of output driver with matching network

Fig 6.5 shows the photograph of the test board for the self-cascode oscillator. The test board is fabricated using FR4 material with four layers. On the top and bottom layers several surface mount components as well as the fabricated chip are mounted. The second layer of the test board is a ground layer that makes sure perfect ground connections for both RF and DC bias signals. The total thickness of the board is 0.062 inch (62 mil) which corresponds to approximately 20 mil separation in between each layer. Based on this information and using 'TXLine' software the width of the microstrip line is calculated for the specified operating frequency (1.4 GHz) and 50 Ω output resistance.

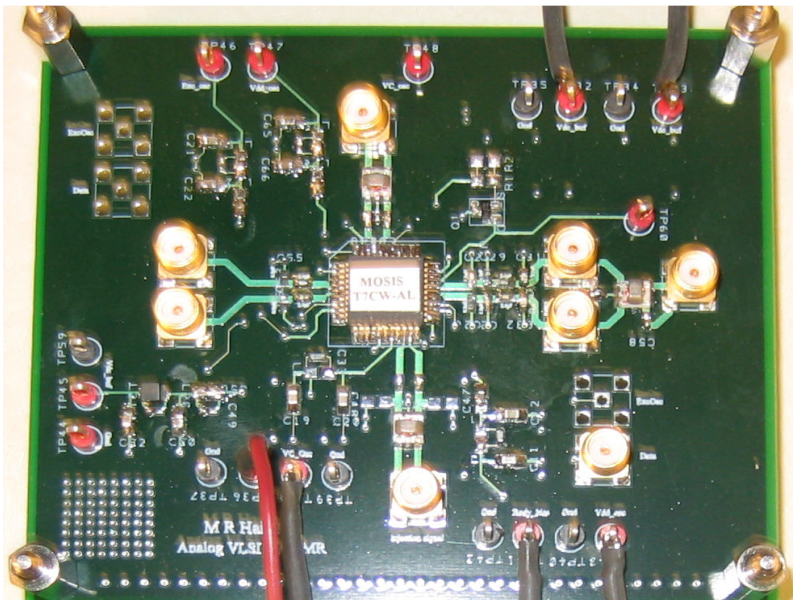
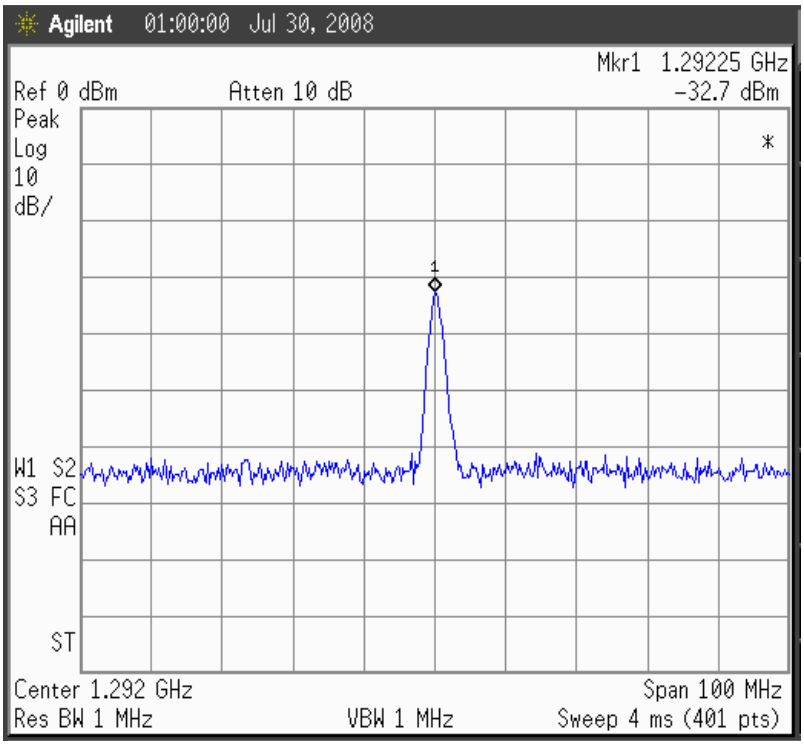
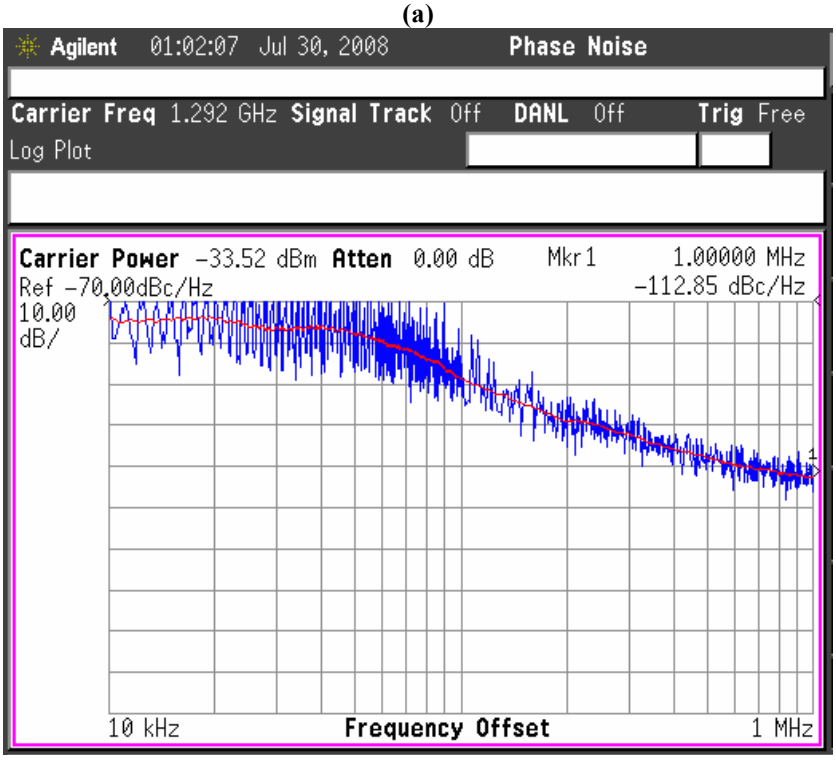


Fig 6.5: Test board of self-cascode oscillator

The fabricated self-cascode oscillator is tested using Agilent E4407B spectrum analyzer. Fig 6.6 and Fig 6.7 show the power spectrum and phase noise profile of the free running self-cascode oscillator for two different frequencies. The output power of the oscillating signal is –32.7 dBm (in Fig 6.6(a)) and –35.07 dBm (Fig 6.7(a)) with oscillating frequency of 1.292 GHz and 1.305 GHz, respectively. The phase noise plots of the free running oscillator demonstrate a phase noise of –112.85dBc@1MHz (in Fig 6.6(b)) and –110.102dBc@1MHz (in Fig 6.7(b)), respectively.

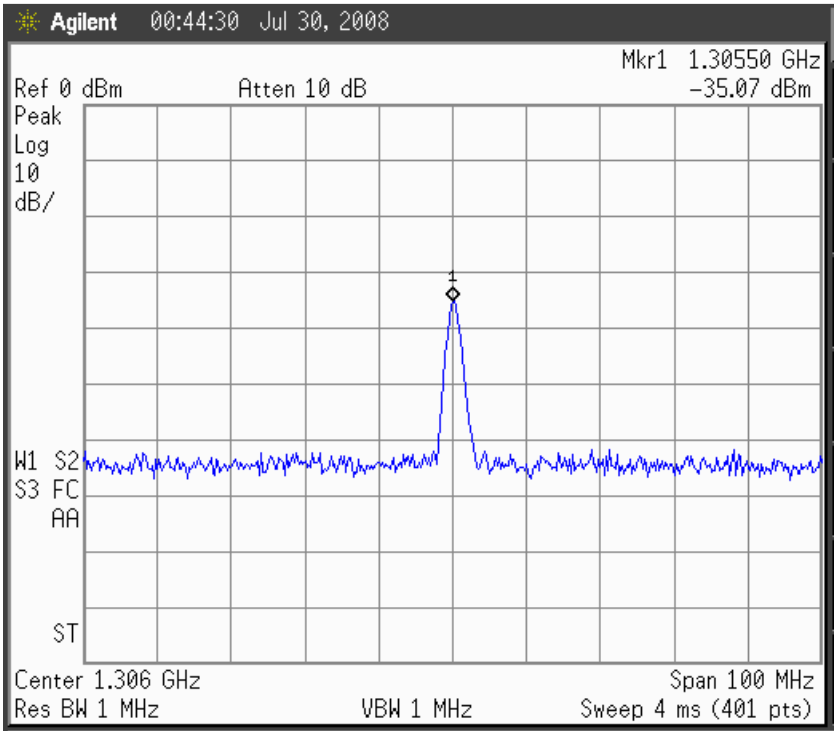


(a)

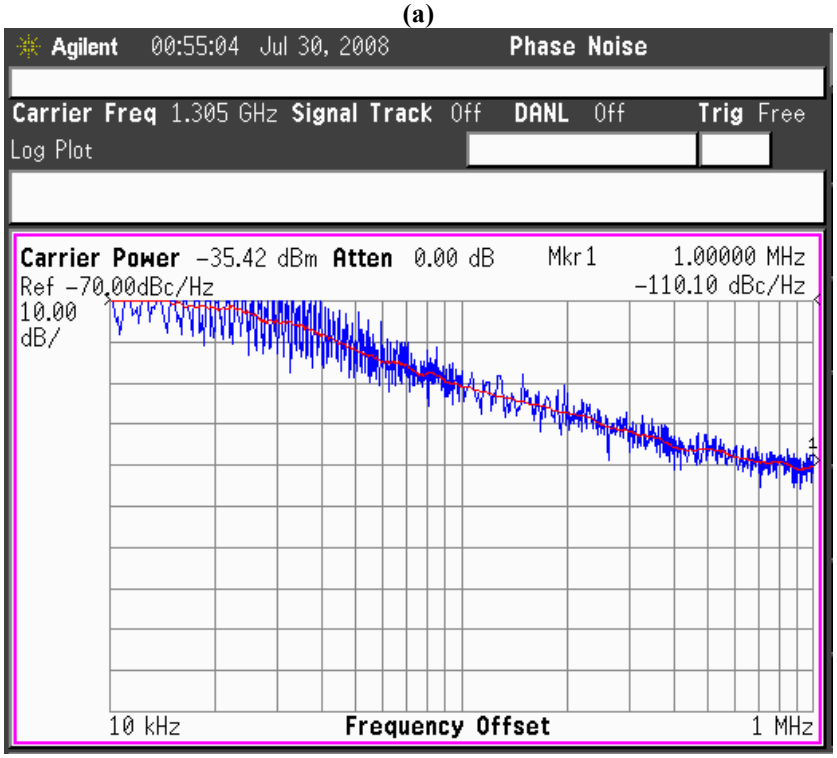


(b)

Fig 6.6: Free running self-cascode LC oscillator with frequency 1.292 GHz (a) power spectrum (b) phase noise profile



(a)



(b)

Fig 6.7: Free running self-cascode LC oscillator with frequency 1.305 GHz (a) power spectrum (b) phase noise profile

The output power of the oscillator depends upon the output driver and clever design of the matching network. The relatively low output power is due to the inefficient output driver and the absence of optimal matching of the matching network. The measured phase noise of the oscillator also shows little bit higher value than the simulated one (simulated –118 dBc@1MHz) which is also due to the relatively low output power obtained from the driver and matching network. The self-cascode oscillator has been designed for an output frequency of 1.4 GHz but from the measurement results the maximum frequency obtained is in the range of 1.33 GHz as shown in Fig 6.8. Fig 6.9 shows the variation of the output frequency with the change of control voltage. From the figure it is seen that for a control voltage in the range of 0.8 V to 1.8 V, the frequency of the oscillator varies almost linearly with the varactor tuning.

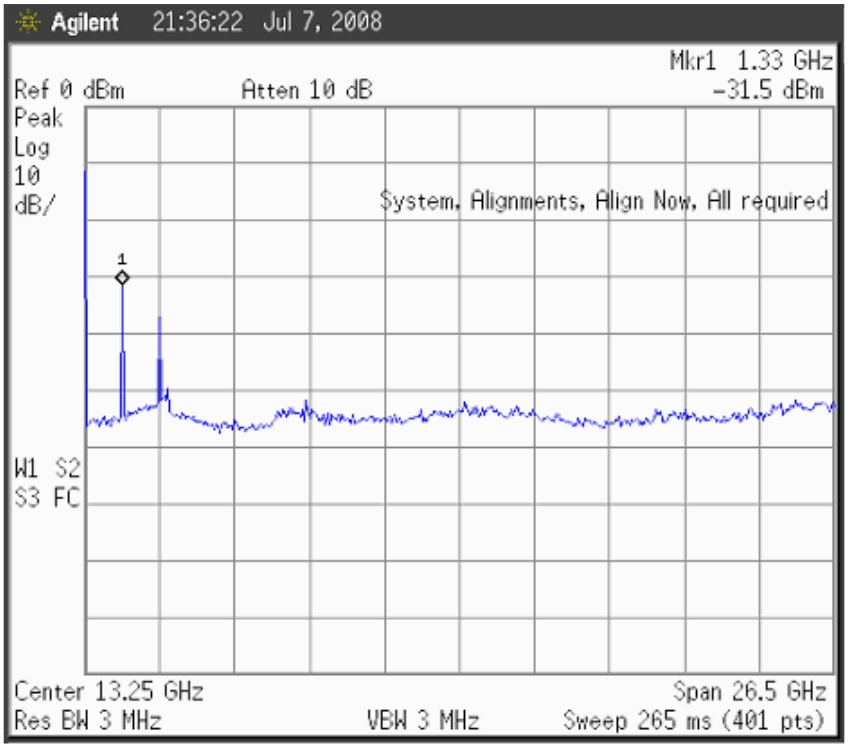


Fig 6.8: Full spectrum of the oscillator from the E4407B spectrum analyzer

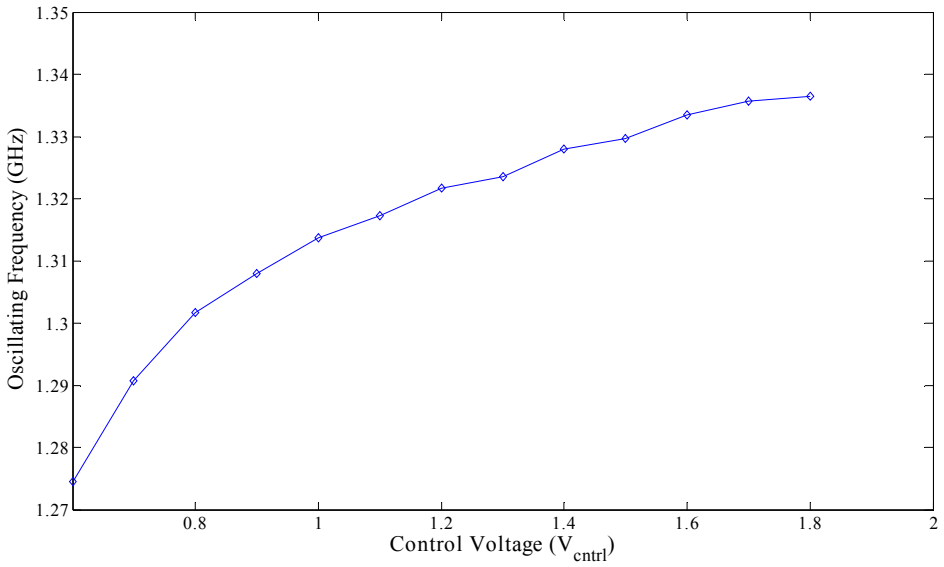


Fig 6.9: Measured tuning characteristics of the self-cascode oscillator

Table 6.1: Power consumption of the self-cascode oscillator with different body bias voltages

V_{body} (V)	I_{osc} (mA)			P_{DC} (mW)		
	V_{osc} = 1.05 V	V_{osc} = 1.2 V	V_{osc} = 0.9 V	V_{osc} = 1.05 V	V_{osc} = 1.2 V	V_{osc} = 0.9 V
0.8	2.25	_	_	2.3625	_	_
0.9	2.13	_	1.557	2.2365	_	1.4013
1	2.07	3.444	1.459	2.1735	4.1328	1.3131
1.1	1.92	3.307	1.339	2.0160	3.9684	1.2051
1.2	1.83	3.274	1.29	1.9215	3.9288	1.161
1.3	1.72	3.134	1.229	1.8060	3.7608	1.1061
1.4	1.63	2.970	1.154	1.7115	3.564	1.0386
1.5	1.54	2.927	1.074	1.6170	3.5124	0.9666
1.6	1.478	2.826	_	1.5519	3.3912	_
1.7	1.445	2.717	_	1.5173	3.2604	_
1.8	1.368	2.632	_	1.4364	3.1584	_

The body terminals of the PMOS devices in the self-cascode structure are connected to a separate supply voltage through a bias resistor. The variations of this supply voltage changes the body-bias of the devices in the self-cascode structure. Table 6.1 depicts the variation of the oscillator current and the corresponding power consumption for different body bias voltages. A graphical representation of Table 6.1 is also shown in Fig 6.10. From the Fig 6.10, it is obvious that by controlling the body terminal voltage the power consumption of the self-cascode oscillator can be further reduced.

The body terminals of the PMOS devices in the self-cascode oscillator are also used to inject an external signal to achieve injection locking. The injection signal is fed though a

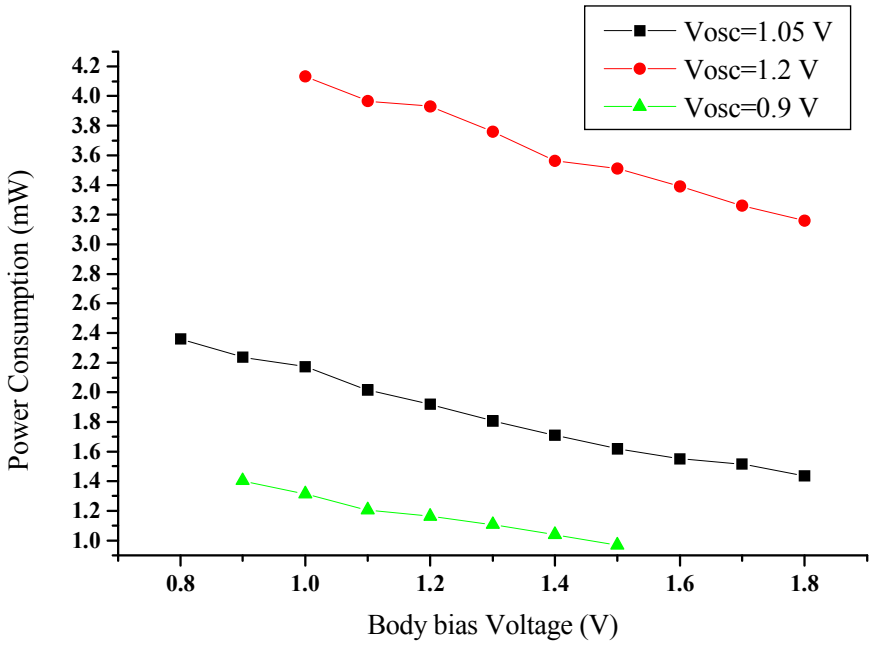
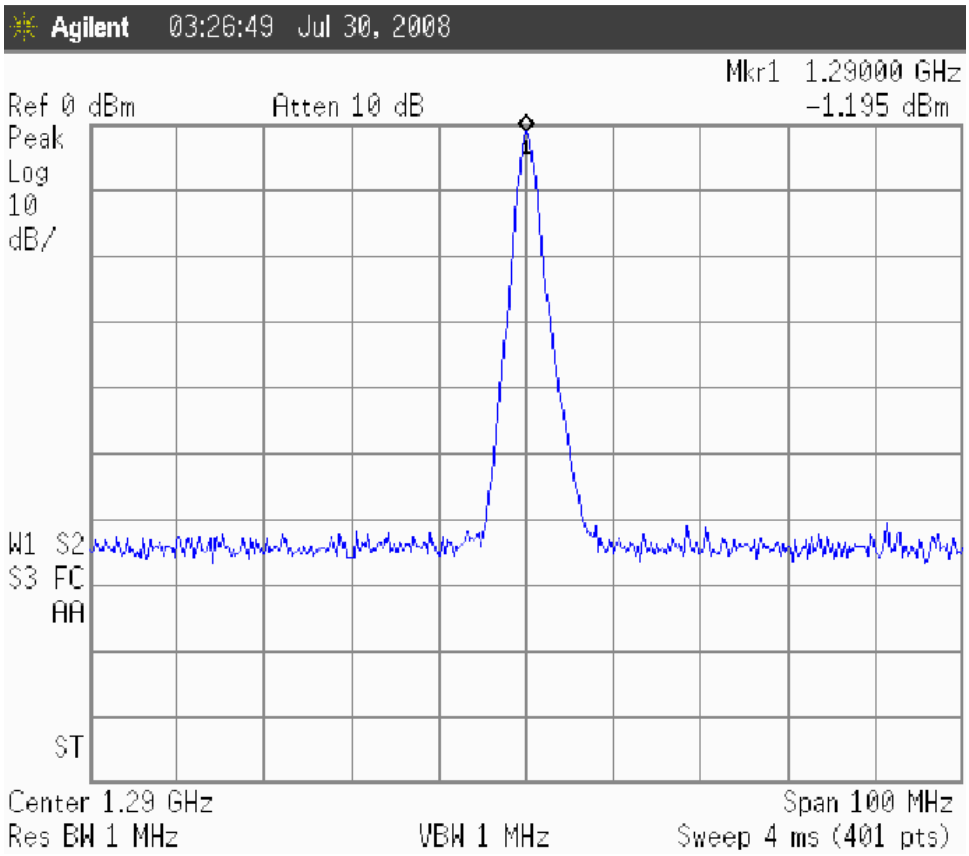


Fig 6.10: Power consumption with different body bias voltages

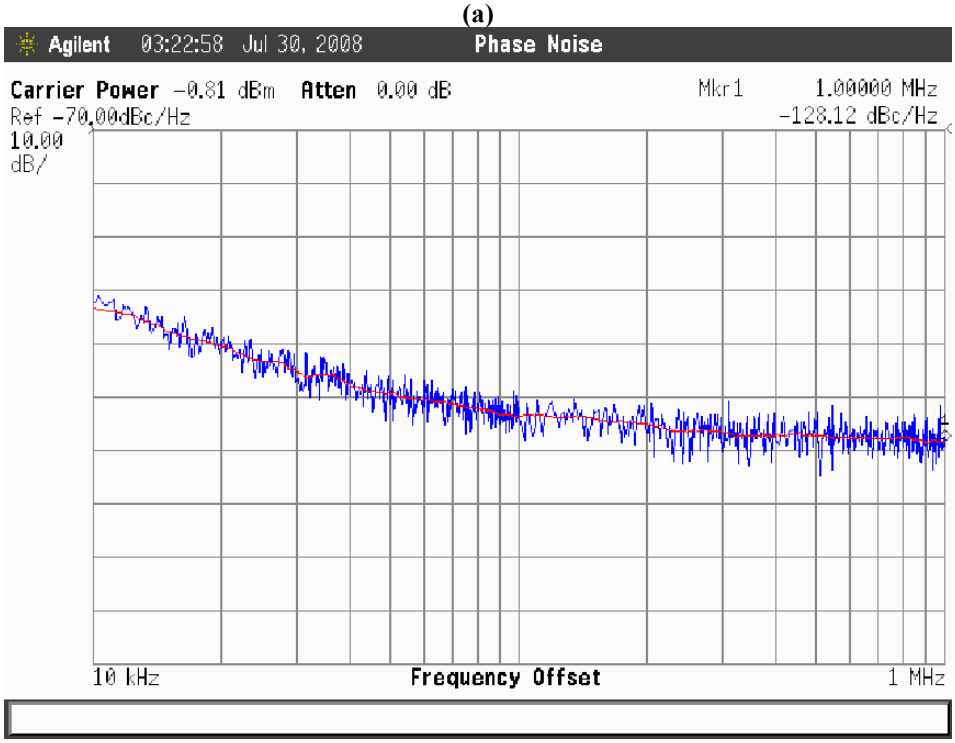
blocking capacitor so that the reverse bias condition of the body terminal of the MOSFET is not disturbed. In addition, the amplitude of the injection signal is restricted to the amount so that the body-source junction of the MOSFET always stays in reverse bias condition. The injection signal modulates the body bias of the MOSFET which ultimately modulates the drain current of the device.

Injection-locking in an oscillator provides frequency stability and improved phase noise performance. In an injection-locked oscillator the close-in phase noise follows the phase noise of the injection signal and the far-out phase noise follows that of the main oscillator. Different types of injection mechanisms have been reported in the literature but most of them incorporate either extra voltage head-room or increased power consumption. Body terminal coupling does not have any of these disadvantages; therefore this is a suitable option for the design of a low-voltage low-power circuit design.

To achieve body terminal coupling of the designed self-cascode oscillator, Agilent E8257D analog signal generator (250 KHz ~40 GHz) is used to generate the injection signal. Fig 6.11 shows the power spectrum and phase noise profile of the injection signal.



(a)



(b)

Fig 6.11: Injection signal from Agilent E8257D Analog Signal Generator (a) power spectrum (b) phase noise profile

From Fig 6.11 it is observed that, the injection signal has a power of -1.195 dBm with a frequency of 1.29 GHz (Fig 6.11(a)) and the phase noise profile indicates a phase noise of -128.12 dBc@1MHz offset (Fig 6.11(b)). This injection signal is fed to the self-cascode oscillator through the body terminals of the PMOS devices in the self-cascode structure to achieve injection locking. Fig 6.12 demonstrates the power spectrum of the injection-locked oscillator. From the figure, it is seen that the oscillator is perfectly locked to the injection signal i.e. the oscillator is oscillating with the frequency of the injection signal (1.29 GHz) instead of the free running frequency. While injection locked, the oscillator follows the phase noise (close-in) profile of the injection signal. Therefore, if the injection signal is a spectrally pure reference signal, the overall phase of the oscillator can be greatly improved.

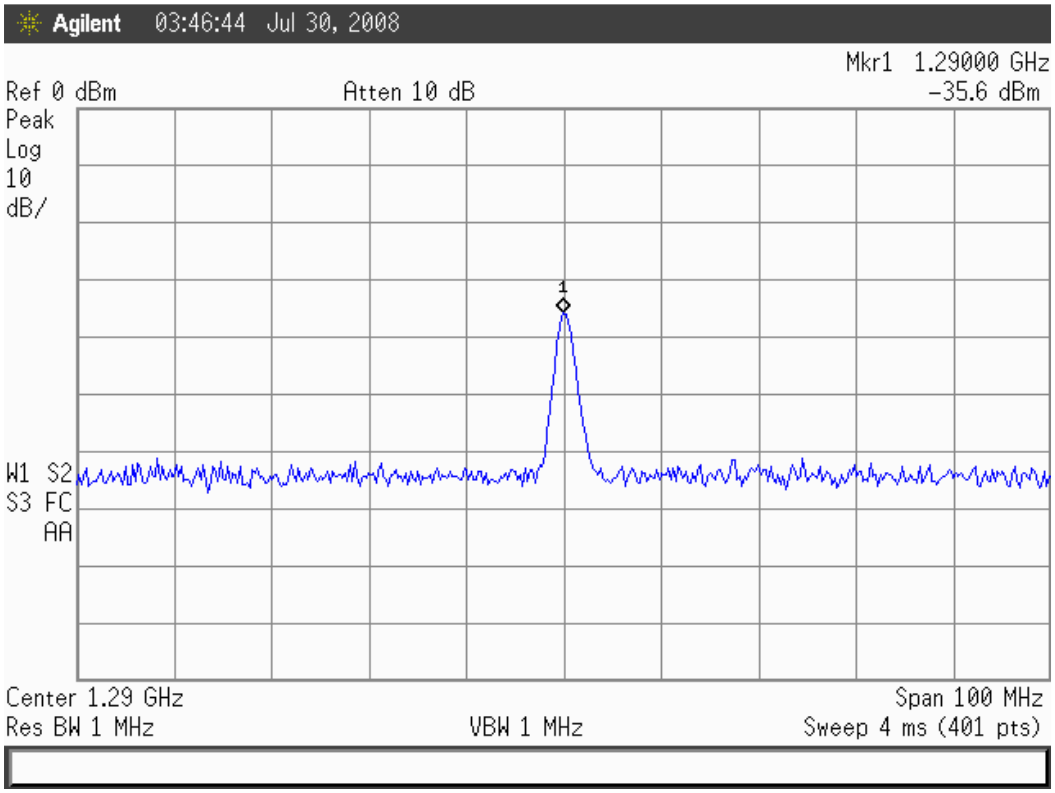
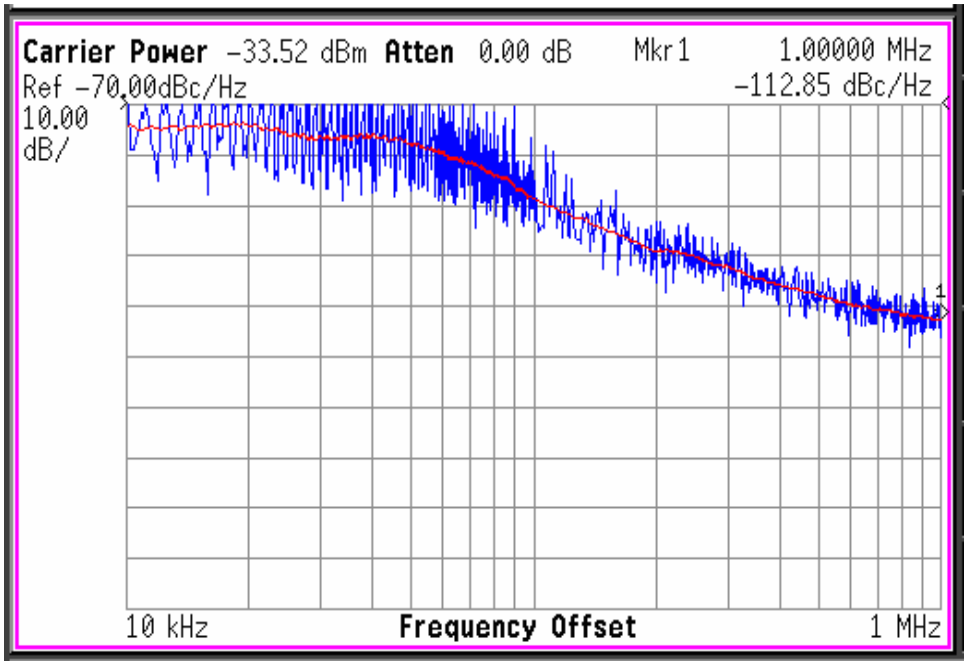


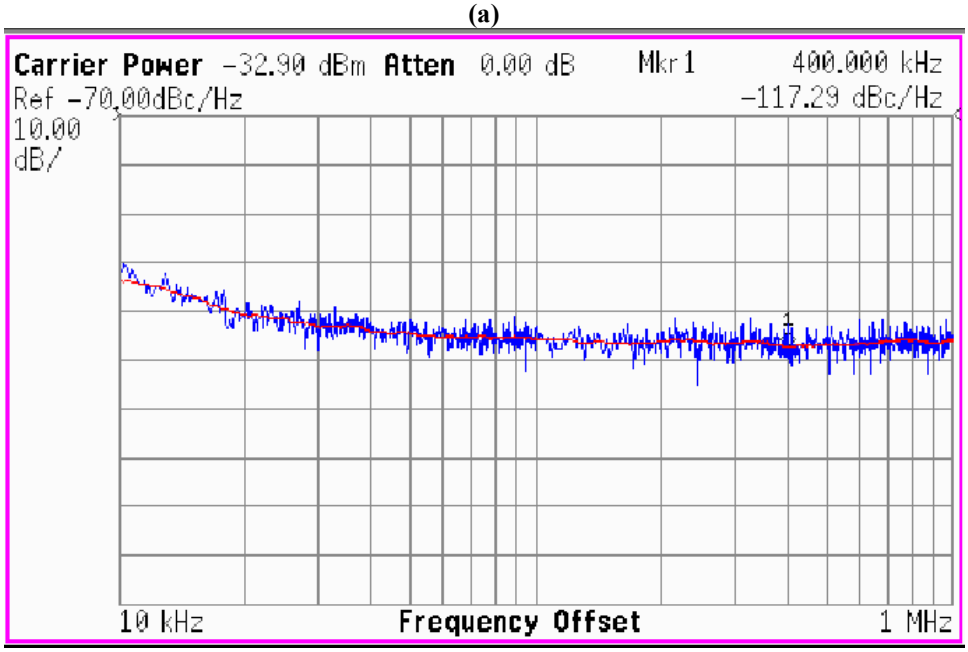
Fig 6.12: Power spectrum of the injection-locked self-cascode oscillator

Fig 6.13 depicts the phase noise profile of the self-cascode oscillator in free running (Fig 6.13 (a)) and injection locked condition (Fig 6.13(b)). From the figure, it can be easily seen that with injection locking the phase noise of the oscillator is substantially improved. In injection locked condition the phase noise is only -117.29 dBc@400 KHz offset whereas in free running condition the phase noise is -112.85 dBc@1 MHz offset.

In the injection locking process, if the frequency of the injection signal falls within the locking range the oscillator is perfectly locked and follows the frequency of the injection signal. However, if the frequency of the injection signal falls at the edge of the locking band, a quasi-locking occurs.



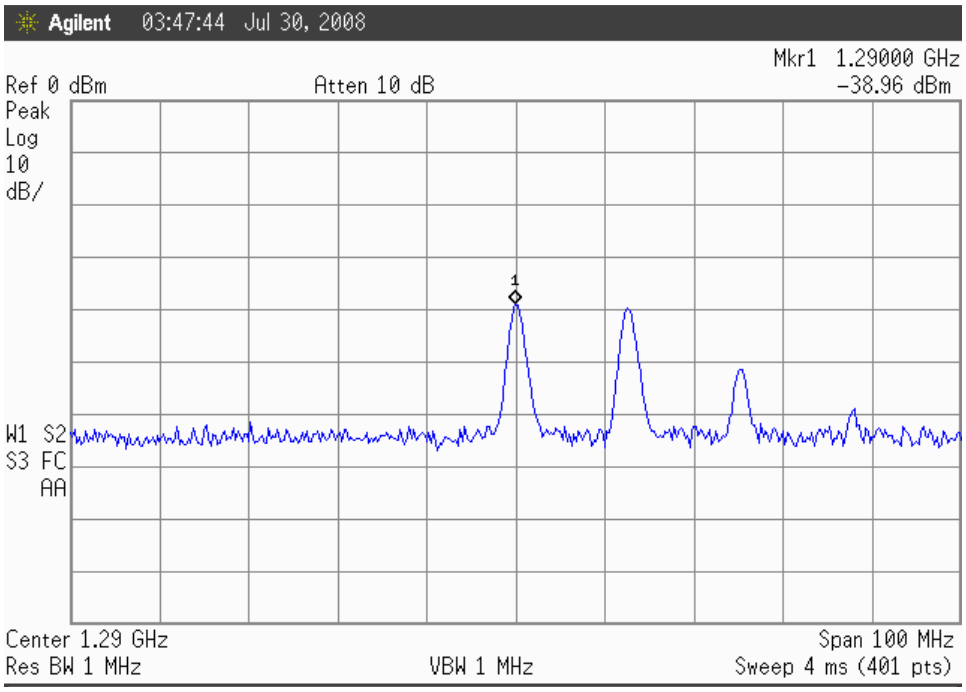
(a)



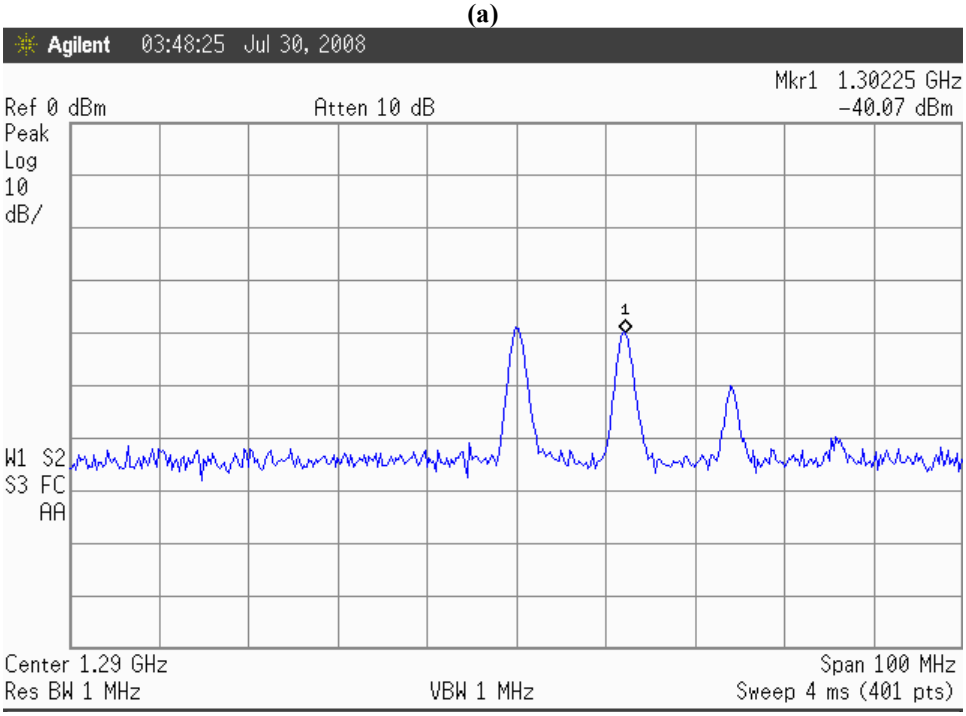
(b)

Fig 6.13: Phase noise profile of the body coupled self-cascode oscillator (a) free running condition (b) injection-locked condition

Fig 6.14 and Fig 6.15 demonstrate the quasi-locking condition for an injection signal of 1.29 GHz 0 dBm and 1.30 GHz -5 dBm, respectively. To achieve quasi-locking of the oscillator, the frequency of the injection signal is kept constant while the control voltage of the varactor is varied until the free running frequency moves to the edge of locking band. From the power spectrum of the quasi-lock condition the locking range of the oscillator can also be predicted. From Fig 6.14 and Fig 6.15 the frequency difference between the 1^{st} and 2^{nd} peaks is 12.25 MHz and 2.75 MHz, respectively. Since the harmonic signal peaks diminish within the locking range, the product of the number of equally spaced harmonic signal peaks and frequency separation between two signal peaks give a quantitative measure of the locking range. Therefore, from Fig 6.14 and Fig 6.15, it is obvious that the locking ranges of the oscillator for injection signal power of 0 dBm and -5 dBm are $12.25 \times 3 = 36.75$ MHz and $2.75 \times 5 = 13.75$ MHz, respectively. One important thing is that even in quasi-locking condition the phase noise of the oscillator is substantially improved as shown in Fig 6.16.

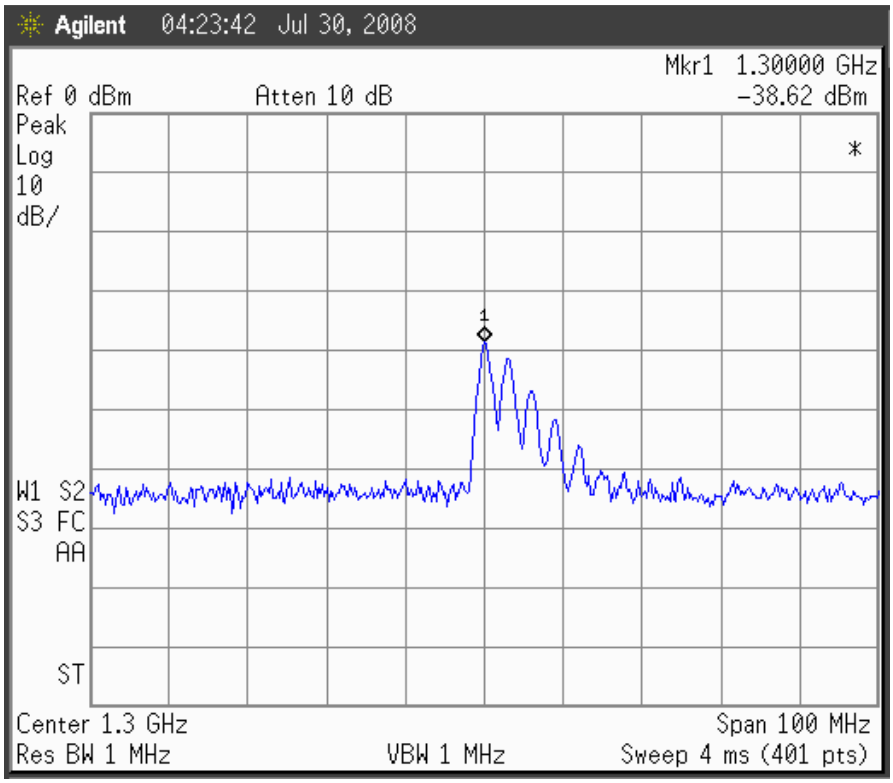


(a)

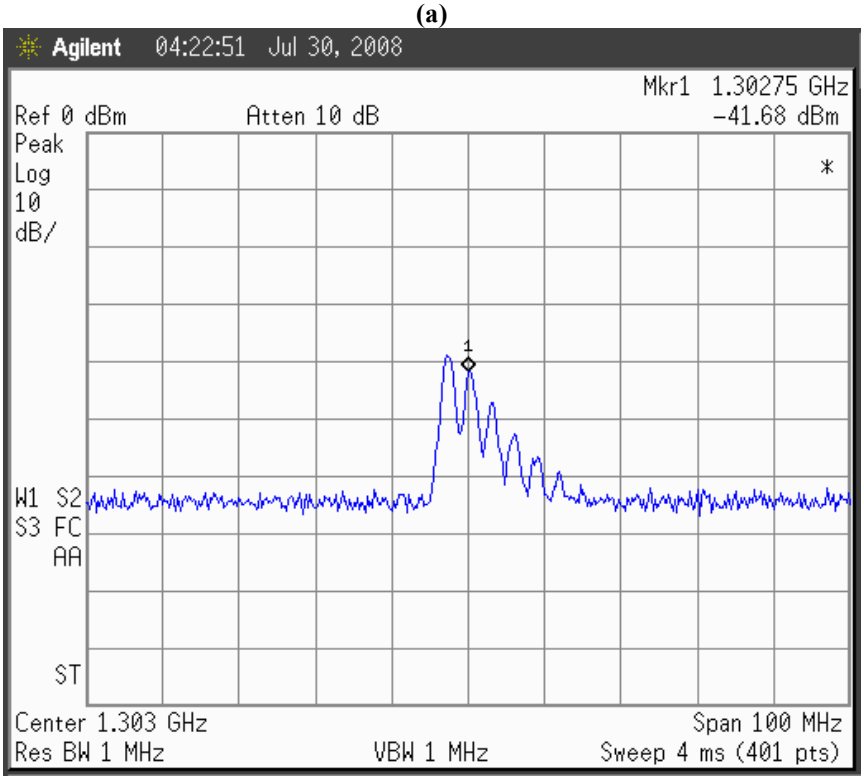


(b)

Fig 6.14: Power spectrum of quasi-locked self-cascode oscillator for a injection signal of 1.29 GHz and 0 dBm (a) 1st peak (b) 2nd peak



(a)



(b)

Fig 6.15: Power spectrum of quasi-locked self-cascode oscillator for a injection signal of 1.30 GHz and -5 dBm (a) 1st peak (b) 2nd peak

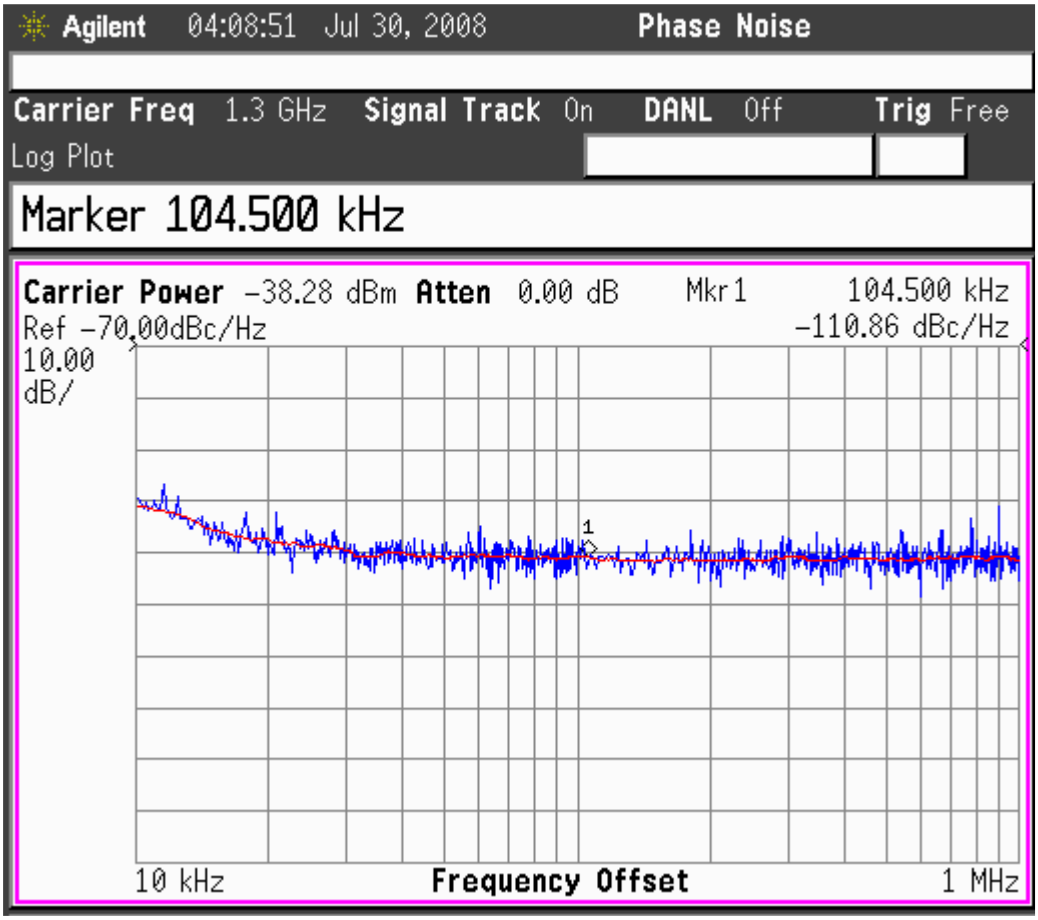


Fig 6.16: Phase noise of quasi-locked oscillator

Fig 6.17 shows the simulated locking range and the corresponding power consumption of the self-cascode oscillator with different injection signal power. It can be seen from the graph that higher the injection signal power higher is the power consumption of the core oscillator with higher locking range. The important thing is that power consumption of the core oscillator is increased approximately at a rate of (2.255-2.22)/3=11.6 μW for 1 dBm increase of the injection signal power. Finally Fig 6.18 shows the Amplitude Shift Keying (ASK) signal output from the self-cascode oscillator. The oscillating signal amplitude for high and low bit position is 182.7 mV and 12.34 mV, respectively.

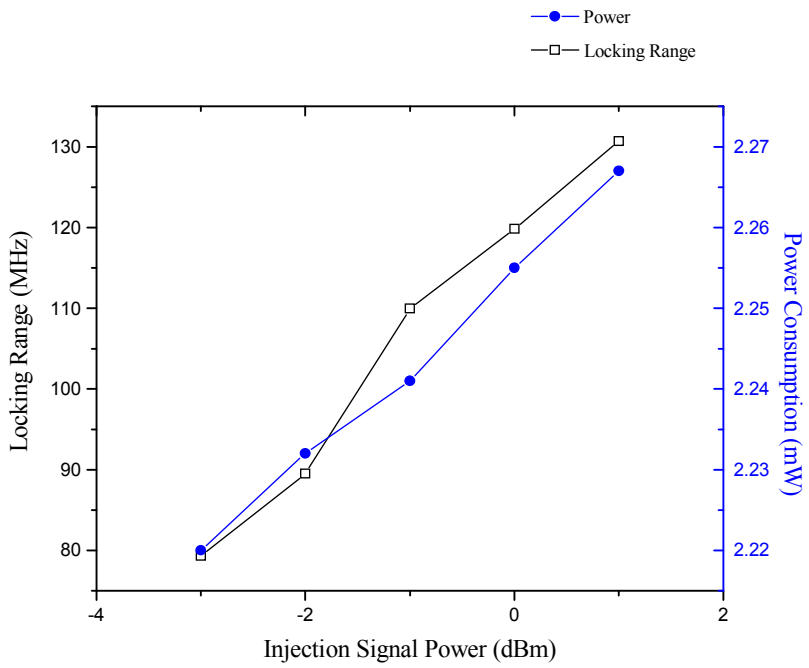


Fig 6.17: Simulated locking-range and power consumption with injection signal power

	High bit	Low bit
Frequency	1.399 GHz	1.4 GHz
Amplitude (p-p)	182.7 mV	12.34 mV

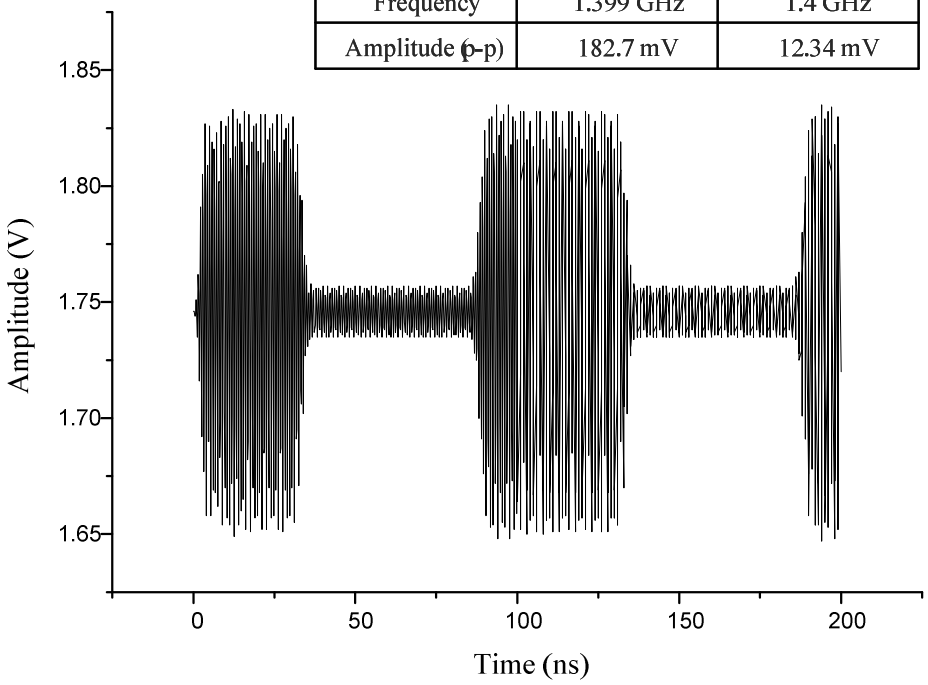


Fig 6.18: Simulated amplitude shift keying (ASK) signal output

It should be noted that the carrier frequency remains almost constant for high and low bit position. Therefore this ASK signal could be easily recovered using a simple envelope detector.

6.3 Summary

This chapter describes about different layout issues, the test setup and the measurement results of the fabricated chip. The self-cascode LC oscillator has been designed and fabricated using 0.18 μm standard CMOS process. In the fabricated chip, an output driver has been incorporated to drive the 50 Ω output load. The output power of the oscillator depends upon the output driver and the off-chip matching networks. Measurement results indicate that the actual output of the designed circuit is slightly different from the simulated one. The measured frequency of oscillation has been found to be1.33 GHz whereas the circuit was originally designed for 1.4 GHz output frequency. This frequency deviation is mainly for the approximate bond wire inductance and package model used in the simulation. The relatively low output power is due to the inefficient output driver and the absence of optimal matching networks. Measurement results also verify that the body terminal coupling helps to achieve injection-locking with better phase noise performance. The locking range of the fabricated oscillator has been measured using quasi-lock condition. The relatively small locking range is due to the low output power from the output driver. Finally a simulation result has been shown which indicates that simpler modulation scheme such as ASK can be easily performed with the designed circuit.

Chapter 7 Conclusion and Future Works

7.1 Conclusion

With the recent technological improvements portable medical devices either for health-care monitoring or for surgical applications are becoming popular day by day. Miniatured, light-weight and cost-effective devices are going to dominate the market in near future. Powering the circuit is always a crucial design factor for designing any circuit for portable devices. With the minimum number of batteries and the light-weight considerations of the portable device, the internal circuitry of the device must operate with low-voltage and low-power operation.

System-on-package (SOP) is an excellent consideration for making a smart potable medical device. The SOP unit for biomedical applications includes sensors to monitor any physiological parameters and the embedded electronics to process the signal and transmit the data to a monitoring unit for further diagnostics. The SOP unit works as a node in a sensor network and data aggregation and monitoring are performed throughout the network. For successful transmission of data each node accompanies a wireless transmitter block that dominates the power consumption of the node.

Development of low-power wireless transmitter for wireless sensor network such as WBAN is getting attention among the researchers. Conventional transmitter architectures are not suitable for short range communication in WBAN. Among the various types of investigated transmitter architectures injection-locked transmitter shows greater promises

due to frequency stability and lower power consumption. The core block of an injection-locked transmitter is an injection-locked oscillator. Therefore improving the performance of an injection-locked oscillator will benefit the improvement of the overall injection-locked transmitter.

Development of low-voltage low-power injection-locked oscillator is a crucial design goal. Conventional cross-coupled LC oscillator can work with low power supply voltage but the current consumption in each conducting branch is high leading to an overall increased power consumption. In this respect, self-cascode structure is an excellent choice to provide higher impedance in conducting branch leading to a lower current consumption and at the same time lower supply voltage operation of the structure. Among the various types of injection mechanisms, 'tail MOSFET injection' requires extra voltage headroom and superharmonic signal, and 'direct injection' incorporates extra power consumption in the injection MOSFET. Body terminal coupling can also perform injection of signal without degrading the voltage headroom and also offers less power consumption due to lower g_{mb}. Therefore, this work uses a self-cascode structure with body terminal coupling to achieve a low-voltage low-power injection-locked oscillator. Simulation and measurement results show the effectiveness of this design.

7.2 Original Contribution

Anticipated original contributions of this research work are summarized as follows.

1) Design of a low-voltage low-power self-cascode oscillator which will facilitate for the development of low-power transmitters.
2) Derivation of optimal MOSFET size of the self-cascode structure.
3) Derivation of oscillation frequency for the self-cascode oscillator.
4) Derivation of required transconductance for startup of the self-cascode oscillator.
5) Derivation of phase noise variation of the self-cascode oscillator with the capacitance ratio.
6) Incorporation of body terminal coupling with the self-cascode oscillator to achieve injection-locking without degrading voltage headroom and power consumption.
7) Incorporation of ASK scheme with the self-cascode body coupled oscillator without degrading voltage headroom.

7.3 Future Works

1) Incorporate current mode bias scheme (instead of voltage bias scheme) without degrading voltage headroom to reduce supply and process variation sensitivity.
2) Incorporate a spectrally pure reference oscillator on the chip to achieve injection locking.
3) Redesign the output driver to increase the output power.
4) Directly couple the oscillator with an antenna and measure the radiation power and overall efficiency of the body-coupled injection-locked transmitter.

5) Derive the governing equations of the self-cascode body-coupled oscillator using more accurate MOS model to improve the design. Use EKV model for Low-power and RF applications.

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Appendices

Appendix A Calculation of MOSFET Dimension – I

From the circuit diagram as shown in Fig 5.12,

$$v_{ds2} = v_{gs2} - v_{gs1} \tag{A.1}$$

Assume no body effect for M_1 and L_1=L_2, v_{t1}= v_{t2} = v_t

$$\frac{\beta_2}{2} \cdot \frac{\left(v_{gs2} - v_t\right)^2}{n} = \frac{\beta_1}{2} \cdot \frac{\left(v_{gs1} - v_t\right)^2}{n} \tag{A.2}$$

Using the condition for saturation for M_2 transistor, it is found that

$$\begin{aligned} & v_{ds2} \geq \frac{v_{gs2} - v_t}{n} \\ & \Rightarrow v_{gs2} - v_{gs1} \geq \frac{v_{gs2} - v_t}{n} \\ & \therefore n\left(v_{gs2} - v_{gs1}\right) \geq v_{gs2} - v_t \end{aligned} \tag{A.3}$$

Now inserting the value from equation (A.3), equation (A.2) can be simplified as follows

$$\frac{\beta_2}{2}\cdot\frac{n^2\left(v_{gs2}-v_{gs1}\right)^2}{n}\geq\frac{\beta_1}{2}\cdot\frac{\left(v_{gs1}-v_t\right)^2}{n}$$

$$\Rightarrow\frac{\beta_1}{\beta_2}\leq\frac{\left\{n\left(v_{gs2}-v_t\right)-n\left(v_{gs1}-v_t\right)\right\}^2}{\left(v_{gs1}-v_t\right)^2}=\frac{n^2\left(v_{gs1}-v_t\right)^2+n^2\left(v_{gs2}-v_t\right)^2-2n\left(v_{gs2}-v_t\right)\left(v_{gs1}-v_t\right)}{\left(v_{gs1}-v_t\right)^2}$$

$$=n^2\cdot\frac{\left(v_{gs2}-v_t\right)^2}{\left(v_{gs1}-v_t\right)^2}+n^2-2n^2\cdot\frac{\left(v_{gs2}-v_t\right)}{\left(v_{gs1}-v_t\right)}$$

$$=n^2\cdot\frac{\beta_1}{\beta_2}+n^2-2n^2\cdot\sqrt{\frac{\beta_1}{\beta_2}}$$

$$=n^2\cdot\left(\sqrt{\frac{\beta_1}{\beta_2}}-1\right)^2$$

$$\Rightarrow\sqrt{\frac{\beta_1}{\beta_2}}\leq n\cdot\left(\sqrt{\frac{\beta_1}{\beta_2}}-1\right)$$

$$\Rightarrow\sqrt{\frac{\beta_1}{\beta_2}}\left(n-1\right)-n\geq 0$$

$$\therefore\frac{\beta_1}{\beta_2}\geq\frac{n^2}{\left(n-1\right)^2}\qquad\textbf{(A.4)}$$

Appendix B Calculation of MOSFET Dimension – II

If body effect is considered then $V_{T1} > V_{T2}$ & $n_1 < n_2$

Since equal current is flowing through both M1 and M2 (in Fig 5.12), this can be written as

$$\frac{\beta_2}{2} \cdot \frac{(v_{GS2} - V_{T2})^2}{n_2} = \frac{\beta_1}{2} \cdot \frac{(v_{GS1} - V_{T1})^2}{n_1} \tag{B.1}$$

Using the condition $v_{DS2} = v_{GS2} - v_{GS1} \geq \frac{v_{GS2} - v_{T2}}{n_2}$ for saturation region operation of M2 transistor, equation (B.1) can be simplified as

$$\therefore \frac{n_2}{n_1} \cdot \frac{\beta_1}{\beta_2} = \frac{(v_{GS2} - v_{T2})^2}{(v_{GS1} - v_{T1})^2} \tag{B.2}$$

Now, using the condition of saturation of M2 transistor, one can write

$$(v_{GS2} - V_{T2}) \leq n_2 \cdot \{(v_{GS2} - V_{T2}) - (v_{GS1} - V_{T1}) + (V_{T2} - V_{T1})\}$$

$$\Rightarrow (v_{GS2} - V_{T2})^2 \leq n_2^2 \cdot \begin{Bmatrix} (v_{GS2} - V_{T2})^2 + (v_{GS1} - V_{T1})^2 + (V_{T2} - V_{T1})^2 - 2 \cdot (v_{GS2} - V_{T2}) \cdot (v_{GS1} - V_{T1}) \\ -2 \cdot (v_{GS1} - V_{T1}) \cdot (V_{T2} - V_{T1}) + 2 \cdot (v_{GS2} - V_{T2}) \cdot (V_{T2} - V_{T1}) \end{Bmatrix}$$

$$\Rightarrow \frac{(v_{GS2} - V_{T2})^2}{(v_{GS1} - V_{T1})^2} \leq n_2^2 \cdot \begin{Bmatrix} \frac{n_2}{n_1} \cdot \frac{\beta_1}{\beta_2} + 1 + \frac{(V_{T2} - V_{T1})^2}{(v_{GS1} - V_{T1})^2} - 2 \cdot \sqrt{\frac{n_2}{n_1}} \cdot \sqrt{\frac{\beta_1}{\beta_2}} - 2 \cdot \frac{(V_{T2} - V_{T1})}{(v_{GS1} - V_{T1})} \\ + 2 \cdot (V_{T2} - V_{T1}) \cdot \frac{(v_{GS2} - V_{T2})}{(v_{GS1} - V_{T1})^2} \end{Bmatrix}$$

$$\Rightarrow \frac{(v_{GS2}-V_{T2})^2}{(v_{GS1}-V_{T1})^2} \le n_2^2 \cdot \left\{ \begin{array}{l} \left(\sqrt{\frac{n_2}{n_1}\cdot\frac{\beta_1}{\beta_2}}\right)^2 - 2\cdot\sqrt{\frac{n_2}{n_1}}\cdot\sqrt{\frac{\beta_1}{\beta_2}} + 1 + \frac{(V_{T2}-V_{T1})^2}{(v_{GS1}-V_{T1})^2} - 2\cdot\frac{(V_{T2}-V_{T1})}{(v_{GS1}-V_{T1})} \\ + 2\cdot(V_{T2}-V_{T1})\cdot\frac{(v_{GS2}-V_{T2})}{(v_{GS1}-V_{T1})^2} \end{array} \right\}$$

$$\Rightarrow \frac{n_2}{n_1}\cdot\frac{\beta_1}{\beta_2} \le n_2^2 \cdot \left\{ \begin{array}{l} \left(\sqrt{\frac{n_2}{n_1}\cdot\frac{\beta_1}{\beta_2}} - 1\right)^2 + \frac{(V_{T2}-V_{T1})^2}{(v_{GS1}-V_{T1})^2} - 2\cdot\frac{(V_{T2}-V_{T1})}{(v_{GS1}-V_{T1})} \\ + 2\cdot(V_{T2}-V_{T1})\cdot\frac{(v_{GS2}-V_{T2})}{(v_{GS1}-V_{T1})^2} \end{array} \right\}$$

$$\Rightarrow \frac{n_2}{n_1}\cdot\frac{\beta_1}{\beta_2} \le n_2^2 \cdot \left\{ \left(\sqrt{\frac{n_2}{n_1}\cdot\frac{\beta_1}{\beta_2}} - 1\right)^2 + \frac{(V_{T2}-V_{T1})^2}{(v_{GS1}-V_{T1})^2} - 2\cdot\frac{(V_{T2}-V_{T1})}{(v_{GS1}-V_{T1})} + 2\cdot\frac{(V_{T2}-V_{T1})}{(v_{GS1}-V_{T1})}\cdot\frac{(v_{GS2}-V_{T2})}{(v_{GS1}-V_{T1})} \right\}$$

$$\Rightarrow \frac{n_2}{n_1}\cdot\frac{\beta_1}{\beta_2} \le n_2^2 \cdot \left\{ \left(\sqrt{\frac{n_2}{n_1}\cdot\frac{\beta_1}{\beta_2}} - 1\right)^2 + \frac{(V_{T2}-V_{T1})^2}{(v_{GS1}-V_{T1})^2} - 2\cdot\frac{(V_{T2}-V_{T1})}{(v_{GS1}-V_{T1})} + 2\cdot\frac{(V_{T2}-V_{T1})}{(v_{GS1}-V_{T1})}\cdot\sqrt{\frac{n_2}{n_1}}\cdot\sqrt{\frac{\beta_1}{\beta_2}} \right\}$$

$$\Rightarrow \frac{n_2}{n_1}\cdot\frac{\beta_1}{\beta_2} \le n_2^2 \cdot \left\{ \left(\sqrt{\frac{n_2}{n_1}\cdot\frac{\beta_1}{\beta_2}} - 1\right)^2 + \frac{(V_{T2}-V_{T1})^2}{(v_{GS1}-V_{T1})^2} + 2\cdot\frac{(V_{T2}-V_{T1})}{(v_{GS1}-V_{T1})}\cdot\left(\sqrt{\frac{n_2}{n_1}}\cdot\sqrt{\frac{\beta_1}{\beta_2}} - 1\right) \right\}$$

$$\Rightarrow \frac{n_2}{n_1}\cdot\frac{\beta_1}{\beta_2} \le n_2^2 \cdot \left(\sqrt{\frac{n_2}{n_1}\cdot\frac{\beta_1}{\beta_2}} - 1 + \frac{(V_{T2}-V_{T1})}{(v_{GS1}-V_{T1})}\right)^2$$

$$\Rightarrow \sqrt{\frac{n_2}{n_1}\cdot\frac{\beta_1}{\beta_2}} \le n_2 \cdot \left(\sqrt{\frac{n_2}{n_1}\cdot\frac{\beta_1}{\beta_2}} - 1 + \frac{(V_{T2}-V_{T1})}{(v_{GS1}-V_{T1})}\right) \qquad \textbf{(B.3)}$$

$$\Rightarrow \sqrt{\frac{\beta_1}{\beta_2}} \ge \sqrt{\frac{n_1}{n_2}}\cdot\frac{n_2}{n_2-1}\left(1 - \frac{(V_{T2}-V_{T1})}{(v_{GS1}-V_{T1})}\right)$$

$$\therefore \frac{\beta_1}{\beta_2} \ge \frac{n_1}{n_2}\cdot\frac{n_2^2}{(n_2-1)^2}\left(1 - \frac{(V_{T2}-V_{T1})}{(v_{GS1}-V_{T1})}\right)^2 \qquad \textbf{(B.4)}$$

Again, from equation (B.2)

$$\sqrt{\frac{n_2}{n_1}\cdot\frac{\beta_1}{\beta_2}}=\frac{(v_{GS2}-V_{T2})}{(v_{GS1}-V_{T1})}$$

$$\therefore (v_{GS1}-V_{T1})=\frac{(v_{GS2}-V_{T2})}{\sqrt{\frac{n_2}{n_1}\cdot\frac{\beta_1}{\beta_2}}} \qquad \textbf{(B.5)}$$

Now using the value from equation (B.5), equation (B.3) can be simplified as

$$\Rightarrow \sqrt{\frac{n_2}{n_1}\cdot\frac{\beta_1}{\beta_2}} \le n_2\cdot\left(\sqrt{\frac{n_2}{n_1}\cdot\frac{\beta_1}{\beta_2}}-1+\frac{(V_{T2}-V_{T1})}{(v_{GS2}-V_{T2})}\cdot\sqrt{\frac{n_2}{n_1}\cdot\frac{\beta_1}{\beta_2}}\right)$$

$$\Rightarrow \sqrt{\frac{n_2}{n_1}\cdot\frac{\beta_1}{\beta_2}} \le n_2\cdot\left\{\sqrt{\frac{n_2}{n_1}\cdot\frac{\beta_1}{\beta_2}}\cdot\left(1+\frac{V_{T2}-V_{T1}}{v_{GS2}-V_{T2}}\right)-1\right\}$$

$$\Rightarrow \sqrt{\frac{n_2}{n_1}\cdot\frac{\beta_1}{\beta_2}}\cdot\left\{n_2\cdot\left(1+\frac{V_{T2}-V_{T1}}{v_{GS2}-V_{T2}}\right)-1\right\}-n_2\ge 0$$

$$\Rightarrow \sqrt{\frac{\beta_1}{\beta_2}} \ge \sqrt{\frac{n_1}{n_2}}\cdot\frac{n_2}{(n_2-1)+n_2\cdot\frac{V_{T2}-V_{T1}}{v_{GS2}-V_{T2}}}$$

$$\Rightarrow \sqrt{\frac{\beta_1}{\beta_2}} \ge \sqrt{\frac{n_1}{n_2}}\cdot\frac{1}{\frac{(n_2-1)}{n_2}+\frac{V_{T2}-V_{T1}}{v_{GS2}-V_{T2}}}$$

$$\Rightarrow \frac{\beta_1}{\beta_2} \ge \frac{n_1}{n_2}\cdot\frac{1}{\left(\frac{(n_2-1)}{n_2}+\frac{V_{T2}-V_{T1}}{v_{GS2}-V_{T2}}\right)^2}$$

$$\therefore \frac{\beta_1}{\beta_2} \ge \frac{n_1}{n_2}\cdot\left(\frac{n_2-1}{n_2}+\frac{V_{T2}-V_{T1}}{v_{GS2}-V_{T2}}\right)^{-2} \qquad \textbf{(B.6)}$$

Appendix C Calculation of the Oscillation frequency and the Required Transconductance

Fig. 5.14 shows the small signal equivalent circuit of a self-cascode LC oscillator circuit. From the circuit,

$$v_{gs} = v_{in} \text{ and } v_{gd} = v_{in} - v_x$$

And

$$v_x = \left(i_d - g_{m2} v_{in}\right) \cdot \frac{1}{sC_2} \tag{C.1}$$

Therefore, the expression for drain current i_d in the equivalent circuit can be simplified as

$$\begin{aligned}
& i_d = g_{m1} v_{gd} + \left(v_{out} - v_x\right) \cdot sC_1 = g_{m1}\left(v_{in} - v_x\right) + \left(v_{out} - v_x\right) \cdot sC_1 \\
& \Rightarrow i_d = g_{m1} v_{in} - g_{m1} v_x + v_{out} \cdot sC_1 - v_x \cdot sC_1 \\
& \Rightarrow i_d = g_{m1} v_{in} + v_{out} \cdot sC_1 - \left(g_{m1} + sC_1\right) \cdot v_x \\
& \Rightarrow i_d = g_{m1} v_{in} + v_{out} \cdot sC_1 - \left(g_{m1} + sC_1\right) \cdot \left(i_d - g_{m2} v_{in}\right) \cdot \frac{1}{sC_2} \\
& \Rightarrow i_d \left\{1 + \left(g_{m1} + sC_1\right) \cdot \frac{1}{sC_2}\right\} = \left\{g_{m1} + g_{m2}\left(g_{m1} + sC_1\right) \cdot \frac{1}{sC_2}\right\} \cdot v_{in} + v_{out} \cdot sC_1
\end{aligned}$$

$$\Rightarrow -v_{out}\left(\frac{1}{sL} + \frac{1}{R}\right)\left\{1 + \left(g_{m1} + sC_1\right) \cdot \frac{1}{sC_2}\right\} = \left\{g_{m1} + g_{m2}\left(g_{m1} + sC_1\right) \cdot \frac{1}{sC_2}\right\} \cdot v_{in} + v_{out} \cdot sC_1$$

$$\Rightarrow -v_{out} \cdot \left\{\left(\frac{R + sL}{sLR}\right)\left(g_{m1} + sC_1 + sC_2\right) + s^2 C_1 C_2\right\} = \left\{sg_{m1} C_2 + g_{m2}\left(g_{m1} + sC_1\right)\right\} \cdot v_{in}$$

$$\therefore \frac{v_{out}}{v_{in}} = -\frac{\left\{sg_{m1} C_2 + g_{m2}\left(g_{m1} + sC_1\right)\right\}}{\left\{\left(\frac{R + sL}{sLR}\right)\left(g_{m1} + sC_1 + sC_2\right) + s^2 C_1 C_2\right\}} \tag{C.2}$$

For sustained oscillation $\frac{v_{out}}{v_{in}} = -1$

Therefore, equation (C.2) becomes

$$\left\{\left(\frac{R+sL}{sLR}\right)\left(g_{m1}+sC_1+sC_2\right)+s^2C_1C_2\right\}=\left\{sg_{m1}C_2+g_{m2}\left(g_{m1}+sC_1\right)\right\}$$

$$\Rightarrow \left(R+sL\right)\left(g_{m1}+sC_1+sC_2\right)+s^3LRC_1C_2=s^2g_{m1}LRC_2+sg_{m2}LR\left(g_{m1}+sC_1\right) \quad \textbf{(C.3)}$$

$$\Rightarrow g_{m1}R+sR\left(C_1+C_2\right)+sg_{m1}L+s^2L\left(C_1+C_2\right)+s^3LRC_1C_2=s^2g_{m1}LRC_2 + sg_{m2}LR\left(g_{m1}+sC_1\right)$$

Now inserting s=jω in the above equation, one can get

$$g_{m1}R+j\omega R\left(C_1+C_2\right)+j\omega g_{m1}L-\omega^2L\left(C_1+C_2\right)-j\omega^3LRC_1C_2=-\omega^2g_{m1}LRC_2 + j\omega g_{m2}g_{m1}LR-\omega^2g_{m2}C_1LR \quad \textbf{(C.4)}$$

Equating real parts

$$g_{m1}R-\omega^2L\left(C_1+C_2\right)=-\omega^2LR\left(g_{m1}C_2+g_{m2}C_1\right) \quad \textbf{(C.5)}$$

$$\therefore \omega^2=\frac{g_{m1}R}{L\left(C_1+C_2\right)-LR\left(g_{m1}C_2+g_{m2}C_1\right)} \quad \textbf{(C.6)}$$

Equating imaginary parts from equation (C.4),

$$\omega R\left(C_1+C_2\right)+\omega g_{m1}L-\omega^3LRC_1C_2=\omega g_{m1}g_{m2}LR$$
$$\Rightarrow R\left(C_1+C_2\right)+g_{m1}L-\omega^2LRC_1C_2=g_{m1}g_{m2}LR \quad \textbf{(C.7)}$$

$$\therefore \omega^2=\frac{R\left(C_1+C_2\right)+g_{m1}L-g_{m1}g_{m2}LR}{LRC_1C_2} \quad \textbf{(C.8)}$$

Now for the conditions $g_{m2}R<<1$ and $R\left(C_1+C_2\right)>>g_{m1}L$. The equation (C.8) can be further simplified as

$$\omega^2 = \frac{R(C_1 + C_2)}{RLC_1C_2} = \frac{1}{L \cdot \frac{C_1C_2}{C_1 + C_2}} \tag{C.9}$$

If a varactor C_v is added at the drain terminals of top MOSFETs, then the equation (C.9) becomes

$$\omega^2 = \frac{R(C_1 + C_2)}{RLC_1C_2} = \frac{1}{L \cdot \left(\frac{C_1C_2}{C_1 + C_2} + C_v \right)} \tag{C.10}$$

Now inserting the value of ω^2 from equation (C.9) into equation (C.6), one can easily get

$$\frac{1}{L \cdot \frac{C_1C_2}{C_1 + C_2}} = \frac{g_{m1}R}{L(C_1 + C_2) - LR(g_{m1}C_2 + g_{m2}C_1)}$$

$$\Rightarrow \left(1 + \frac{C_2}{C_1}\right) = \frac{g_{m1}R}{\left(\frac{C_1}{C_2} + 1\right) - R\left(g_{m1} + g_{m2}\frac{C_1}{C_2}\right)}$$

$$\Rightarrow \left(1 + \frac{C_2}{C_1}\right)\left(1 + \frac{C_1}{C_2}\right) - \left(1 + \frac{C_2}{C_1}\right)R\left(g_{m1} + g_{m2}\frac{C_1}{C_2}\right) = g_{m1}R$$

$$\Rightarrow g_{m1}R\left\{1 + \left(1 + \frac{C_2}{C_1}\right)\left(1 + \frac{g_{m2}}{g_{m1}}\frac{C_1}{C_2}\right)\right\} = \left(1 + \frac{C_2}{C_1}\right)\left(1 + \frac{C_1}{C_2}\right)$$

$$\therefore g_{m1}R = \frac{\left(1 + \frac{C_2}{C_1}\right)\left(1 + \frac{C_1}{C_2}\right)}{1 + \left(1 + \frac{C_2}{C_1}\right)\left(1 + \frac{1}{k}\frac{C_1}{C_2}\right)} \tag{C.11}$$

Vita

Mohammad Rafiqul Haider received his B. Sc. and M. Sc. from Bangladesh University of Engineering and Technology (BUET), Bangladesh, in 2002 and 2004, respectively. From 2002 to 2004, he worked as a Lecturer in the department of Electrical and Electronics Engineering (EEE) of BUET. From August 2005 he is pursuing his Ph. D. studies in the University of Tennessee, USA. His doctoral research is focused on the development of low-power telemetry for biomedical applications. He has several publications in different journals and conference proceedings. He has received best paper award from the journal committee of 'Sensors and Transducers' in 2007. His fields of interests are low-power analog and RF circuit design, low-power circuit design for sensor instrumentations, optical signal and image processing, etc.