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To the Graduate Council:

I am submitting herewith a dissertation written by Jihoon Kim entitled "A Study of Fabrication of Ultra-high Resolution Nano Devices through Electron Beam Lithography Process and Its Application to Electron – Optical Systems." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Materials Science and Engineering.

David C. Joy, Major Professor

We have read this dissertation and recommend its acceptance:

Philip D. Rack, Joseph E. Spruiell, Anthony J. Pedraza

Accepted for the Council:

Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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A dissertation presented for the

Doctor of Philosophy degree

The University of Tennessee, Knoxville

Jihoon Kim

August 2007

DEDICATION

To my parents In Tae Kim and Hee Ja Lee who have been devoted to, supported me all the way and prayed to God for me all the time since the beginning of my life and to my wife Chae Mi Lim who has supported, believed and loved me in spite of severe and difficult circumstances, and to my sister Ji-Young Kim, and my brother Won-Chul Kim. And also to my father and mother-in-law, Young Il Lim and Hye Sung Park who have supported and prayed all the time for us, me and my wife.

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ABSTRACT

Today's semiconductor industry has been significantly changing in its techniques and processes for the fabrication of devices and accordingly, there has been dramatic increase in performance and a reduction in cost. To obtain still higher device performances and still further cost reduction, the dimensions of patterns in integrated circuits should be as small as possible and the 3-dimensional accuracy of multidimensional semiconductor structures should be also achieved as well. The manufacturing of smaller feature dimensions and 3-dimensional devices has been enabled by developments in lithography – the technology which transfers designed patterns onto the silicon wafer. Especially, electron beam lithography is widely adapted in the nano fabrication technology due to its ability to achieve nanometer-scale resolution. The aim of this work is to fabricate test devices by the electron beam lithography possesses and apply them to the test of electron optical systems.

In this thesis, we first develop methods to fabricate a high resolution nano scale Fresnel zone plate and 3-dimenstional stair case structure by E-beam lithography. To optimize the fabrication we optimized the lithographic process and the subsequent process steps accounted for proximity effects via a correction program and controlled pattern transfer through reactive ion etching (RIE). The completed devices were tested in a Scanning Electron Microscopy (SEM) and the accuracy of feature parameters were examined by Fast Fourier Transformation methods (FFT). Finally, the application of these structures to the calibration and testing of e-beam systems was explored.

TABLE OF CONTENTS

CHAPTER 1 INTRODUCTION **1**

CHAPTER 2 LITERATURE REVIEW **5**

2.1 Lithography **5**
2.2 History of semiconductor **5**
2.3 Lithographic process **8**
2.4 Type of lithography **9**
2.4.1 Optical lithography **9**
2.4.1.1 Contact Printing 9
2.4.1.2 Proximity printing 10
2.4.1.3 Projection printing 11
2.4.2 X-ray lithography **12**
2.4.3 Ion-beam projection lithography **13**
2.5 Electron beam lithography **13**
2.5.1 Introduction and historical review **13**
2.5.2 Application area of Electron beam lithography system **15**
2.5.3 E-Beam Lithography Systems **15**
2.5.4 E-Beam Resists **16**
2.5.5 Commercially used e-beam resists **21**
2.5.5.1 The positive e-beam resists 21
2.5.5.2 The negative tone e-beam resists 21
2.6 Proximity effect **23**
2.6.1 Electron Solid interactions **23**
2.6.1.1 Forward scattering 24
2.6.1.2 Back scattered electron 26
2.6.1.3 Secondary electrons 26
2.6.2 Proximity effect correction **27**
2.6.2.1 Models of energy profile 27
2.6.2.2 Type of proximity correction 28
2.6.2.2.1 Dose correction methods 28
2.6.2.2.2 Shape modification methods 30

2.6.2.2.3 Background exposure correction 30
2.6.3 PYRAMID **30**
2.6.3.1 Digital signal processing (DSP) model 32
2.6.3.2 Global exposure 34
2.6.3.3 Local exposure 34
2.6.3.3.1 CDF method 34
2.7 Metrology **35**
2.7.1 Overlay metrology **35**
2.7.1.1 Error source 39
2.7.1.1.1 Low edge contrast 39
2.7.1.1.2 Accuracy 39
2.7.1.1.3 Precision of the tool 40
2.7.2 Critical Dimension (CD) metrology (linewidth metrology) **40**
2.7.2.1 Uncertainty in CD measurement 41
2.7.2.2 Linewidth metrology tools 44
2.7.2.2.1 Scanning Electron Microscopy (SEM) 44
2.7.2.2.2 Atomic Force Microscope 45
2.7.2.2.3 Scatterometry metrology 46

CHAPTER 3 FABRICATION OF FRESNEL ZONE PLATES **48**

3.1 Background **48**
3.1.1 What is Fresnel zone plate? **48**
3.1.2 Why a Fresnel zone plate? **53**
3.2 Electron beam lithography (JBX-6000FS/E) **54**
3.3 Experiment **58**
3.3.1 Design of Fresnel zone plate **58**
3.3.2 Proximity correction **58**
3.3.3 Exposure details **60**
3.3.4 Fabrication on Polymethylmethacrylate (PMMA) resist **63**
3.3.5 Fabrication on Hydrogen silsesquioxane (HSQ) resist **64**
3.4 Result and discussion **64**
3.4.1 Fabrication FZP on PMMA **64**
3.4.1.1 Field size effect on fabrication 64

3.4.1.2 Baking time and developing system 65
3.4.2 Fabrication of FZP on HSQ **75**
3.4.2.1 Resist behavior at two different baking and developing conditions as a function of base dose variation 79
3.4.2.2 Fabrication of FZP on HSQ 85

CHAPTER 4 CONTROLLING RESIST THICKNESS AND ETCH DEPTH FOR FABRICATION OF 3-D STRUCTURES **88**

4.1 Background **88**
4.2 Experiment **89**
4.2.1 Dose determination **89**
4.2.2 Fabrication of staircase structure **91**
4.2.3 Transfer of pattern using RIE (Reactive Ion etching) **92**
4.3 Result and discussion **93**
4.3.1 Fabrication of stair case structures **93**
4.3.2 Transfer of staircase structures in resist onto Si through RIE (reactive ion etching) **103**

CHAPTER 5 APPLICATION **122**

5.1 Introduction **122**
5.2 Basic technique **123**
5.3 Application of analysis program **125**
5.3.1 The application of Fresenel zone plates and analysis program for measuring of tool performance **125**
5.3.2 The application of staircase structres and analysis program for SEM DoF **133**
5.4 Summary **142**

CHAPTER 6 CONCLUSION **143**

REFERENCES **146**

VITA **154**

LIST OF TABLES

2.1 The characteristics of positive and negative resists. **20**

2.2 Comparison of commercially available electron beam resists. **22**

3.1 Field size, scanning step and beam diameter (minimum) according to operation modes and accelerating voltage. **56**

3.2 The measured value of fabricated and designed ring width of a zone plate. **78**

4.1 Dose factors and corresponding depth of stair case structures fabricated on ~100 *n*m PMMA with modified pattern layout **94**

4.2 Dose factors based on the relation ship curve between exposure and development depth and corresponding values of development depth. **98**

4.3 Dose factors based on the relation ship curve between exposure and development depth and corresponding values of development depth. **101**

4.4 Taguchi DOE for optimizing RIE process in CF_4-O_2 system. **104**

4.5 Taguchi DOE for optimizing RIE process in SF_6-O_2 system. **109**

LIST OF FIGURES

2.1	PMMA reaction mechanism.	18
2.2	The cross linking mechanism for COP.	19
2.3	a) Simulated trajectories of 100 electrons in PMMA film on Si and b) schematic electron scattering in electron resist exposure.	25
2.4	Schematic showing how the GHOST technique can be used to correct proximity effect.	31
2.5	Image processing model used to simulate the exposure of a circuit pattern.	33
2.6	Illustration of the CDF convolution methods: (a) the convolution value(Conv) of rectangle at the origin is calculated and (b) a graphical description to obtain Conv.	36
2.7	Centerline determination.	38
2.8	Definition of linewidth (Critical dimension).	41
2.9	Three dimensional representation of a line profile.	43
3.1	The schematic of Fresnel zone plate.	49
3.2	Fabrication of Fresnel zone plate on Si_3N_4 a) exposure and development, b) RIE(reactive ion etch) thin Ge mask, c) RIE AZ Photoresist, d) RIE thick Ge substrate.	51
3.3	Fabrication of Fresnel zone plate on Si_3N_4 with a trilayer resist and electroplating. a) exposure, development, and RIE (reactive ion etching) thin Ge mask, b) RIE AZ photoresist, c) RIE Ge, d) electroplate Nickel.	52
3.4	The schematic of Electron optics system of JBX-6000FS/E	55
3.5	The schematic for vector scanning and step and repeat method	57
3.6	The construction of a Fresnel zone plate.	59
3.7	A part of the outer-most ring (shaded) is shown, where the ring width is 20 *n*m and the pixel interval is 2.5nm. Those pixels in the shaded area, which are at the square grid points, are exposed.	61
3.8	The exposure distribution of a cross-section; deposited energy variation from the center of the Fresnel zones toward the outside.	62
3.9	The position of a zone plate in the subfields. a) Zone plate is centered at a subfield, and b) present at a junction among subfields.	66

3.10 The scanning trace of beam exposure according to the position of zone plate present in a) a subfield and b) at a junction of subfields. 67

3.11 Fresnel zone plate fabricated on PMMA; with a) base dose of 150μC/cm^2 and the pattern designed at a junction of subfields, b) base dose of 150μC/cm^2, and Fresnel zone plate fabricated on PMMA; with c) base dose of 160μC/cm^2 and the pattern designed at a junction of subfields, d) base dose of 160μ*u*C/cm^2 and the pattern designed within a subfield. 68

3.12 Fresnel zone plate fabricated on 50nm PMMA with baking time of 3 minutes at 180 ; a) 150μC/cm^2 b) 160μC/cm^2 c) 170μC/cm^2 d) 180μC/cm^2 e) 190μC/cm^2 71

3.13 Fresnel zone plate fabricated on PMMA a) with base dose of 160μC/cm^2, b) with base dose of 162μC/cm^2 and developing temperature of 20℃. 73

3.14 The schematic of beam exposure direction employed for PYRAMID program. Beam exposures are proceeding along the circle. 74

3.15 Fresnel zone plate fabricated on HSQ with base dose of 160μC/cm^2 and developing temperature of 20 a) at the magnification of 32kX and b) 95kX, and base dose of 154μC/cm^2 and developing temperature of 20.8 at the magnification of c) 32kX and d) 95kX. 77

3.16 The chemical structure of HSQ resist: a) ladder structure, b) cage structure, and c) network structure. 80

3.17 Presumable reaction mechanism of HSQ: a) SiH bonds, which are weaker than SiO bonds are broken by e-beam, b) Silanoles are formed by a reaction to moisture and c) Siloxne bonds are formed by cross linking. 81

3.18 Contrast curves obtained from the exposure on HSQ. a) Thickness remaining in relative unit as a function of base dose, and b) actual height change. 83

3.19 Fresnel zone plates fabricated on HSQ with the condition of baking at 100, 200 and 300 for 1minute respectively and developing at TMAH for 70 seconds, TMAH : D.I.W = 1: 9 for 10seconds and D.I.W for 10seconds with the base dose of a) 300 , b) 400 and C) 500μC/cm^2 . 86

3.20	Fresnel zone plates fabricated with the condition of baking at 120 and 200℃ for 2 minutes, respectively and developing at TMAH for 70 seconds, MF322 : D.I.W = 1:9 for 10seconds and D.I.W 10seconds with the base dose of a) 400 ,b) 500 and C) 580μC/cm^2 .	87
4.1	A staircase structure consisting of 6 steps: when it is transferred onto resist, the development depth refers to the initial thickness of resist minus the remaining thickness of resist.	90
4.2	The depth profile measured on AFM. Each picture shows the developed structure and is corresponding to the condition and numbering on table 3. Measuring of depth is performed on 3 different points of each stair and values are averaged.	95
4.3	Relationship between exposure and development depth for the staircase structure (step width of 1.0μm) transferred onto 100nm PMMA on Si with the beam energy of 50keV.	96
4.4	The remaining resist profiles, after development, of the staircase structures transferred onto PMMA on *Si* a) top view, b) cross-section: the left-most step is 2μm wide, and (c) 3-D image. The step height is about 20nm.	99
4.5	The remaining resist profiles, after development, of the staircase structures transferred onto PMMA on *Si* when the step width is 0.5 *u*m. a) top view and b) cross-section: the left-most step is 1.0μm wide. The step height is 20nm.	102
4.6	Effect of RF power, pressure, and gas composition on the etching rates of silicon and PMMA.	105
4.7	Potential distribution in a process chamber for an RIE system.	106
4.8	Effect of RF power, pressure, and gas composition on the a) etching rates of silicon and b) PMMA and c) the ratio of the silicon etching rate to the PMMA etching rate.	110
4.9	The etched pattern profiles of the staircase structures transferred into *Si* with condition of a) Power of 100*W*, SF_6 pressure of 50mtorr and Oxygen flow rate of 0*sccm*; b) Power of 100*W*, SF_6 pressure of 150mtorr and Oxygen flow rate of 10*sccm.* and c) Power of 150W, SF_6 pressure of 150mtorr and Oxygen flow rate of 0*sccm*.	112

4.10 The schematic expression for the variation of etchant concentration and a cross section of etched structure as etching is proceeding. 115

4.11 Representation of the PMMA cleavage scheme. PMMA decomposition is followed by the main chain cleavage or the ester carbonyl group cleavage mechanism. 117

4.12 The reaction scheme of PMMA with plasma induced radicals (**I•**). 118

4.13 The etched pattern profiles of the staircase structures transferred into *Si* when the step width is 1.oμm ((a) top view and (b) cross-section: the left-most step is 2μm wide) and 0.5μm ((c) top view and (d) cross-section: the left-most step is 1.0μm wide). 120

5.1 Fresnel zone plate fabricated on 50nm HSQ: a) the base dose of 480μC/cm^2 and developed in TMAH for 70seconds, TMAH: D.I.W = 1:9 for 10seconds and D.I.W for 10seconds and b) the base dose of 460μC/cm^2 and developed in 0.26N TMAH for 70seconds, TMAH: D.I.W = 1:10 for 60 seconds and D.I.W for 60seconds. SEM images are taken at 2keV on a LEO 1525 scanning electron microscope. 126

5.2 The intensity distribution normalized by the maximum value is plotted as a function of spatial frequency, *f*. 127

5.3 The diffractogram power spectrum of the central 512x512 pixel region of the image shown in figure 5.1. The power spectrum shown has been thresholded to display the boundary between signal and noise which defines the spatial resolution. 128

5.4 Manual mode analysis of the Power Spectrum derived from the image shown in figure 5.1. The superimposed rings are calibrated directly in units of nanometers. 130

5.5 Power spectrum obtained from superposition diffractogram mode. 132

5.6 The intensity distribution as a function of spatial frequencies. a) Normalized signal change as a function of spatial frequency, and b) signal change as a function of spatial frequency. The intensity distribution has been thresholded to display the boundary between signal and noise which defines the spatial resolution. 135

5.7 Diffractogram power spectrums obtained from automatic analysis mode; a) over focus, b) focus, and c) under focus. 137

5.8 Manual mode analysis of the Power Spectrum; a) under focus, b) focus, and c) under focus. The superimposed rings are calibrated directly in units of nanometers. 138

5.9 Power spectrum obtained from superposition diffractogram mode; a) under focus, b) focus, and c) over focus. 140

CHAPTER 1

INTRODUCTION

Today's semiconductor industry has been significantly changing in its techniques and processes for the fabrication of device since first monolithic integrated circuit was invented in 1960 [1] and accordingly there has been dramatic increase in performance and a reduction in cost. To obtain still higher device performances and still further cost reduction, the dimensions of patterns in integrated circuits should be as small as possible so as to make more devices integrated onto a single chip. The manufacturing of smaller feature dimensions has been enabled by developments in lithography – the technology which transfers designed patterns onto the silicon. [2]

Lithographic tools which make use of various beam sources have been developed and used in the industry and research. Currently, optical lithography which applies photons as the beam source is widely and dominantly used because of its high wafer throughput. However, this tool shows some limitation in manufacturing small feature size due to the wavelength of the illumination resulting in diffraction limited resolution. Therefore, other lithographic tools which use electron beams, x-ray beams or ion beams are being considered as possible tools for device manufacture. [3] Especially, electron beam lithography is widely adapted in the nano fabrication technology due to its ability to achieve nanometer-scale resolution.

Although e-beam lithography can create extremely fine patterns theoretically, it can not

do as much as might be expected. One of main factors causing problems is electron scattering through the inevitable electron beam-solid interactions that occur inside materials and give rise to pattern distortions that are called proximity effects. In addition, control of lithographic process such as the proper choice of resist and the deposition of the resist film, the beam exposure, the development, and the pattern transfer through the etching also affect the ability to fabricate small feature that accurately followed the desired design.

Another factor necessary to obtain higher device performance is controlling the 3-dimensional accuracy of devices. Many optoelectronic devices such as diffractive optical elements, blazed gratings, and photonic band gap crystals include multidimensional semiconductor structures and it is known that their performance is highly sensitive to dimensional accuracy of features in all three dimensions. Therefore, it is essential to achieve high dimensional fidelity in the fabrication process. One possible approach is to use the *binary* lithographic process multiple times. However, this approach has a few drawbacks, especially when the number of different depths is greater than two: a longer total process time, the alignment problem between processes, a higher probability for a lower yield due to the complicated process, and a higher cost. Also, a gradually varying 3-D surface cannot be handled by this approach. These drawbacks can be eliminated by one step of e-beam lithography.

Although 3-dimensional fabrication of devices is enabled by electron beam lithography, as the feature size decreases to the nanometer scale, proximity effects from electron scattering become more severe and can result in fabricated structures which are substantially different to the designed structures. Consequently, controlling proximity

effects and developments of optimum conditions for the lithographic process become crucial work for the more advanced technology. [4]

Another practical issue which arises as pattern dimension shrinks is how feature dimension can be precisely and accurately determined in the procedure called CD (Critical Dimension) metrology. The ability to measure the critical dimension (CDs) of structures on silicon wafers is very important because feature dimensions have a direct impact on the devices or chip performance. For example, gate length and width determine transistor performance and the dimensions of interconnect vias will affect resistance and hence signal speed. [5] [6]

Two or more decades ago, linewidths were big enough to be measured on optical microscopes, and thus could be easily determined and readily calibrated. However, current smaller feature sizes make it very difficult to measure dimensions exactly due to the limitation of measuring tools for small patterns, and also as the result of fluctuation between tools. Therefore, determination of constant and exact dimensions become key issues and the semiconductor industry demands not only high performance measuring tools, but also standardized tests and programs to ensure accurate calibration.

In current fabrication environments, line-width measurements in semiconductor industry are performed almost exclusively using scanning electron microscope (SEM) and this process is known as critical dimension SEM (CD-SEM) metrology. CD-SEMs are now required to achieve a spatial resolution below 1nm for current technology. In order to verify that the tool is reaching the required level of performance to subsequently monitor its performance during measuring CDs or to be able to compare the imaging parameters of one tool with those of others, it is necessary to quantify such parameters as resolution,

signal to noise ratio and drift under standard operating conditions. [7]

Another important parameter to be considered for CD-SEMs is the Depth of field (DoF). In general, pattern dimensions shrink, the pattern aspect ratio increases, and so the DoF becomes an important limit to performance. As mentioned above, many devices are very sensitive to size variations in all 3-dimensions. Therefore, exact measurements of feature size in 3- dimensional structures are very important.

For the above reasons, the industry demands not only high performance from its measuring tools but also standardized test procedures and programs for evaluation and ensuring tool performance.

In this thesis, we first develop methods to fabricate a high resolution nano scale Fresnel zone plate and 3-dimenstional stair case structure by E-beam lithography. To optimize the fabrication we optimized the lithographic process and the subsequent process steps accounted for proximity effects via a correction program and controlled pattern transfer through reactive ion etching (RIE). The completed devices were tested in a Scanning Electron Microscopy (SEM) and the accuracy of feature parameters were examined by Fast Fourier Transformation methods (FFT). Finally, the application of these structures to the calibration and testing of e-beam systems was explored.

CHAPTER 2

LITERATURE REVIEW

2.1 Lithography

Lithography is the composite word of "lithos" which is the ancient Greek word for stone and “-graphy”. This was invented by Alois Senefelder in Germany in 1798. Lithography was a method of printing an image by applying patterned color layers to paper with a series of etched metal or stone plates. In the early days of lithography, a smooth piece of limestone was used. [8]

Today lithography was developed for use in semiconductor industry manufacturing integrated circuit and in microelectronics industry (MEMS) and recently this technology has been used in nano biotechnology industry because it is one of the best methods currently in use for manufacturing devices on scales much smaller than a micrometer. Nowadays all the industry demand smaller and smaller size of devices because this can provide economical benefits and advancement of industrial technology. From this point of view, the advent of lithography technology is the kind of breakthrough in the industry.

2.2 History of semiconductor

The semiconductor industry started from the invention of the first semiconductor transistor by William Shockley, John Bardeen, and Walter Brattain at Bell Labs in 1947. [9] This was the first device designed to act as both a transmitter, converting sound waves

into electronic waves, and resistor, controlling electronic current, and composed of a small piece of germanium, some gold foil, a paper clip, and several pieces of plastic. This simple device is the parent of all the various semiconductor transistor devices produced over the years, including computer microprocessors, memory chips, and solid state power amplification circuits.

The key innovation in semiconductors was the invention of the first monolithic (formed from a single crystal) integrated circuit by Jack Kilby and Robert Noyce in 1960. In designing a complex electronic machine like a computer it was necessary to increase the number of components involved in order to make technical advances. The monolithic integrated circuit placed the previously separated transistors, capacitors and all the connecting wiring onto a single crystal which makes it possible to pack a large amount of function into areas much smaller than one discrete transistor. Kilby used germanium and Noyce used silicon for the semiconductor material. This invention started driving us to the information age. The typical minimum feature size in these early products was greater than 20μm. [9]

Significant progress has been made since 1960, when device features were approximately 20 μm wide. Today's leading edge semiconductor devices have critical dimensions as small as 70 nm. The dramatic increase in performance and cost reduction in the electronics industry are achieved by innovations in the integrated circuit and packaging fabrication process. It has been accordingly continued to shrink the dimensions of the patterns in semiconductor devices. Reductions in feature sizes enable more devices to be integrated onto a single chip and make products more functionally powerful. While the feature sizes have decreased and the number of ingredients in integrated devices has

increased, the overall cost of making a semiconductor device have remained constant due to the high wafer throughput of optical lithography. Consequently, cost per function has decreased dramatically. [10] [11]

Reductions in the feature sizes, especially in the size of transistor gate structure, have also led to dramatic increases in the speed of logic devices such as microprocessors.

The present trend of integrated circuit technology is toward large-scale integration. This requires making the components as small as possible and packing more circuits on a silicon chip. Smaller components give higher packing density, higher speed, and higher yield due to their small active area. [12] Manufacturing of these smaller features has been enabled by development in the lithography technology. Lithography was introduced at about the time of the invention of the integrated circuit (i.e., 1958) and this can print the feature of the planar transistors for the integrated circuit. [4] In the late 1960s, integrated circuits had line widths of 5μm, and in the 2005, it reached to the minimum feature sizes of 80nm with optical lithography. [11] [13] Currently, this size can be more minimized by using other high resolution lithography like electron beam lithography. [11] Historically, lithography technology has been advanced dramatically, innovatively and rapidly. As a result, IC technology has been greatly changed for the past two decades. Consequently, lithography is remarkably useful technology throughout the time of IC industry. [3]

Lithography replicates a pattern rapidly from chip to chip, wafer to wafer, or substrate to substrate for IC fabrication. Also, lithography is basic production method for nano-material, nano biosystem (nanobio industry), etc. A lithographic system includes exposure tool, mask, resist, and all of the processing steps to accomplish pattern transfer from a mask to a resist and then to devices. Above all, proper choice of the exposure tool

and resist are very important. [11] Lithography machine types are divided into 4 types according to the light or beam source. Currently, optical lithography is dominantly used due to its high wafer throughput. E-beam, Ion beam and X-ray lithography are also considered as good tools to manufacturing devices and alternatives to optical lithography due to its resolution limit. [3]

2.3 Lithographic process [14] [15] [16]

The manufacture of semiconductor products requires the ability to work selectively on small, well-defined areas of the semiconductor substrate. This is the lithographic process.

1) surface preparation

Cleaning and drying of wafer surface to elevate photo resist adhesion. (dehydration)

2) photo resist application.

Coating of a thin layer of photo resist to the wafer to give a uniform, adherent, defect-free polymeric film of desired thickness over entire wafer.

3) Soft baking.

Partial evaporation of photo resist solvent by hot plate baked at ~80℃ to promote adhesion of resist by relieving film stresses that arise from the shear forces resulting from the spinning process.

4) Exposure.

Exposure of some form of radiation in order to get pattern image projected onto wafer.

5) Development.

Removal of exposed or unexposed resist by developer.

6) Hard baking

Additional evaporation of solvents by baking at 150℃~200℃. This improves adhesion and increases the etch resistance. Sometimes this removes the incidence of pinhole or thin spots in the resist.

2.4 Type of lithography

2.4.1 Optical lithography

Optical lithography uses the UV (ultra violet) light as a light source, and there are 3 types of patterning methods.

2.4.1.1 Contact Printing

A photo resist-covered wafer was pressed against a photomask with pressure of about 0.05atm to 0.3atm, and the resist was then exposed with broadband-visible and near-UV light (300~450nm). [17] This contact printing achieves the most faithful image transfer and also the best resolution of less than 0.5µm line width of any optical lithographic exposure method. [18] The equation for the resolution is as follows.

$$2b_{\min} = 3\sqrt{\lambda(s + 1(1/2)z)} \qquad (2.1)$$

$2b$: grating period

s: gap width

λ: wavelength of the exposing radiation

z: photo resist thickness

However, due to the non-uniform contact between the mask and the substrate, a thin (0.2 μm) mask must be used. The debris due to repeated mask-to-wafer contacting steps generates the defect on the mask and wafer, which prevents the intimate contact between mask and wafers and degraded resolution. Also, this would print on the next wafer that was exposed through the mask and give rise to the need to replace the mask after a short period of time. [19] To minimize the problems, contact printing has replaced the emulsion mask with chromium mask, and chromium mask has become the work horse of the IC industry. Such chromium masks could be inspected and cleaned regularly, But eventually, the defects on the mask could not be removed by cleaning. Commercially, contact printing is never practiced due to these kinds of problems. [20]

2.4.1.2 Proximity printing

The first such non-contacting printing technology was proximity printing. In proximity printing, the mask is not in contact to the substrate but is placed with a separation of 20 to 50μm. As a result, this method avoids the mask damage that occurs in contact printing. The mask used in proximity printing has a larger life span due to the fact that there is no contact between it and the wafer. However, resolution is degraded and is not as good as compared to contact printing or projection printing due to the gap between the mask and the wafer. For example, at a gap of 10μm, for example, the maximum resolution with 400 nm exposing radiation is ~ 3μm. [21]

$$2b_{\min} \approx \sqrt{3s\lambda} \quad (2.2)$$

$2b$: grating period

s: gap width

λ: wavelength of the exposing radiation

Proximity printing requires a small, very constant spacing, which can be achieved only with extremely flat wafers and masks. Average flatness today of a mask or wafer is on the order of a few micrometers.

In spite of the limitation of contact and proximity printing, the relatively low cost and simplicity of operation of these techniques make them the methods of choice for fabrication devices with relatively large feature sizes. [19] [22]

2.4.1.3 Projection printing

The problems and limitations of contact and proximity printing give rise to the development of projection printing. In this method, the mask and wafer are separated by many centimeters and lens elements are used to focus the mask image onto the wafer surface. Since the mask is not in contact with the wafer, it has a much lower rate of wearing. This method saves the replacement cost, improves uniformity with the use of the mask and replaced the contact and proximity printing in the mid-1970s. The first projection printer was introduced in 1974 and it used all-reflective system. [19] This was 1X printer and could produce features down to about 1.5μm. To image even smaller

minimum feature sizes step-and-repeat projection printing (stepper) was introduced in 1978 and now this can produce feature size down to about 0.1μm sizes. [19] [21] [23] However, beyond that limit, non optical lithographic technique is necessary because of some limitation in its resolution according to impact of the depth of focus and optical resolution.

$$LW \cong 0.61\frac{\lambda}{NA} \quad \text{(Smaller is better)} \tag{2.3}$$

$$DOF = \pm\frac{\lambda}{2(NA)^2} \quad \text{(Larger is better)} \tag{2.4}$$

λ: exposure wavelength

NA : Numerical Aperture

From above equation, smaller LW and large DOF are desirable and thus optimum NA should be determined. [22] [24] [25]

2.4.2 X-ray lithography

The approach to reduce diffraction effect by shortening the wavelength by 2 to 3 orders of magnitude to the X-ray region was first suggested in 1972 by Spears and smith. Since then, X-ray lithography has been under intense investigation in many laboratories for the past 20 years as a possible alternative for photolithography. [26] [27] [28] This has the similar system to proximity printing of optical lithography and the process of imaging a

full-field onto a wafer. This provides high-structural resolution as wide as 0.1μm and a wide scope of advantages for the application in circuit production. [27] [29] The ultra short wavelength of 1nm x-rays eliminates the diffraction effects that limit the resolution of optical proximity systems. Although this system has its own advantages for manufacturing device, this system is not incorporated into IC- industry. The reason is that if the current lithography system in industry is switched this system, new exposure source, mask, resist, and alignment system should be introduced which might give rise to cost increase and significant risk. [26] [30]

2.4.3 Ion-beam projection lithography

Ion-beam lithography has been developing since the early 1980s. [31] This system uses the heavier charged particles such as protons (H^+) as a source. [32] Focused ion beam (FIB) lithography has several advantages over other high resolution techniques.

Compared to e-beam lithography, in which proximity compensation is required because of the feature broadening caused by electron scattering in the resist, no compensation is required for the FIB Heavy ion which has very little scattering, but continuous bombardment of the mask and substrate can result in fatal damage on it. [33]

2.5 Electron beam lithography

2.5.1 Introduction and historical review

Electron beam lithography (EBL) has played an important role in advancing the science and technology of very small semiconductor and metal device structures. [34] Electron

beam lithography(EBL) can create extremely fine patterns required by modern electronic industry for integrated circuits and submicron patterns less than 1µm from very small spot size of electron beam (sub micron patterns about 0.05µm). [28]

Main attributes of this system are capability of very high resolution [17] [35], flexible technique that can work with a variety of materials and an almost infinite number of patterns[36] slow speed of operation (one or more orders of magnitude slower than optical microscopy) [37] and expensive and complicated system(cost many millions of dollars and require frequent service to get properly maintained). [37]

Electron beam lithography was first used to fabricate photo-mask for conventional optical microscopy because it provided the required speed, automated pattern data processing, resolution and accuracy. [34] [38] Another field of e-beam lithography is to write directly on the wafer, eliminating the expensive, time consuming mask steps. The fundamental advantage of direct writing is the capability to use the writing e-beam probe to precisely measure and correctly position device patterns on wafer. [34] [36] [39] [40] However, throughput is slower than that of optical lithography.

The first electron beam lithography machines, based on the scanning electron microscopy, were developed in 1965. The first commercial system, EBES (electron beam exposure system), was built at Bell Laboratories in 1975. This system, based on scanning electron microscope technology, was called a Gaussian round beam system due to focusing of single round spot. [41] This system was improved as MEBES at ETEC Corporation which can satisfy the requirement for the 0.18µm generation technology. [42] The shaped beam e-beam lithography of high throughput, high resolution was

introduced in 1975 as EL-1 at IBM. [43] This system has developed to upgrade the speed of operation. [34] EL-4 and EL-4+, the latest in the series of e-beam exposure tools, was introduced in 1993, and received the reputation as the most advanced and capable mask-makers industry.

2.5.2 Application area of Electron beam lithography system

The most important use of EBL is to make photo mask. Masks are typically chrome on glass plate with e-beam sensitive resist layer and this is subsequently exposed and developed to generate the required pattern on the mask. This has been the method of choice because of the resolution and throughput as well as, its flexibility in providing rapid turn around for design changes. [34] [38] [44]

The second application is the direct write for advanced prototyping of integrated circuits and manufacture of small volume devices, such as gallium arsenide integrated circuits. This results from flexibility, the resolution of electron beam lithography and rapid turn around for new device designs. [34] [36] [39] [40]

Electron beam lithography is used for research into the scaling limits of integrated circuit and effect of downscaling existing production devices [17] [45] or for the study of quantum effects and other physics phenomena at very small dimensions. [17] [46]

2.5.3 E-Beam Lithography Systems [37] [47] [48] [49]

(1) Electron source (gun)

There are two types of electron guns used for making the electron beams.

a) Thermionic source

Beam is generated by heating materials to the temperature at which electrons are emitted. Examples of source are tungsten(W) and lanthanum hexa boride(LaB_6)

b) Field emission source

Electrons are emitted from the sharp tip of the material by applying high electric field and form a fine Gausian spot.

(2) Electron optical column

This consists of the electron source, focusing and magnifying lenses, a beam blanker, apertures and deflector.

(3) Mechanical system

This system is composed of wafer or mask stage and their loading system. Correct positioning (accuracy) and the speed of movement of the stage are very important.

(4) The computer

This is used to control the mechanical system and the electron optical column to transfer pattern information for generation of pattern data.

2.5.4 E-Beam Resists

The main purposes of resist are precise pattern formation and protection of the substrate during subsequent process like etching, ion implantation, coating, etc. Also, photoresist has an important role in determining the resolution of lithography system. Photoresist consists of polymer (changes structure when exposed to radiation), photoactive compound (controls chemical reactions) and solvent (allows spin application, controls

viscosity). [50]

The usual resists can be dissolved or less dissolved with the solvent after electron beam exposure. There are two types of e-beam resists: positive resist and negative resist.

Positive resists increase solubility by exposing of electron beam and exposed area disappears after developing. [51] When they get energy from electron beam, photo chemical transformation reaction happens and the functional groups are removed or replaced by others [52] [53] which changes the material properties and thus makes a material soluble in solvent. In figure 2.1, schematic PMMA reaction mechanism is shown. Negative resists [8] are insoluble after exposure to radiation, and thus the unexposed area can be removed by treatment with an appropriate solvent. [51] This resist generates three-dimensional molecular network (cross-linking) through the photochemical reaction by electron beam exposure. This cross-linking structure exhibits insolubility against the solvent. [53] In figure 2.2, schematic crosslinking mechanism of COP is shown.

Recently, positive resists have dominated the fabrication of leading edge devices primarily because of their higher resolution. [52] Negative resists has the inherent resolution limitations which makes this resist unavailable for patterns less than about 3.0μm size because they tend to have problems with scum (insoluble residue in exposed areas), swelling during developing, and distort the size. [50] [54] The characteristic features of positive and negative resists are shown in table 2.1. [50]

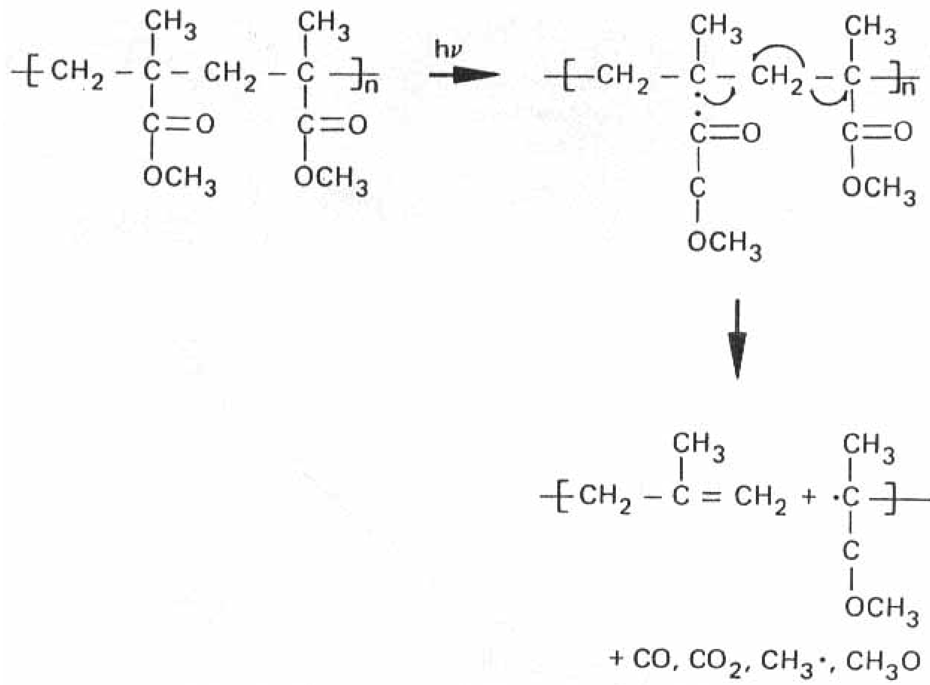


Figure. 2.1: PMMA reaction mechanism. [55]

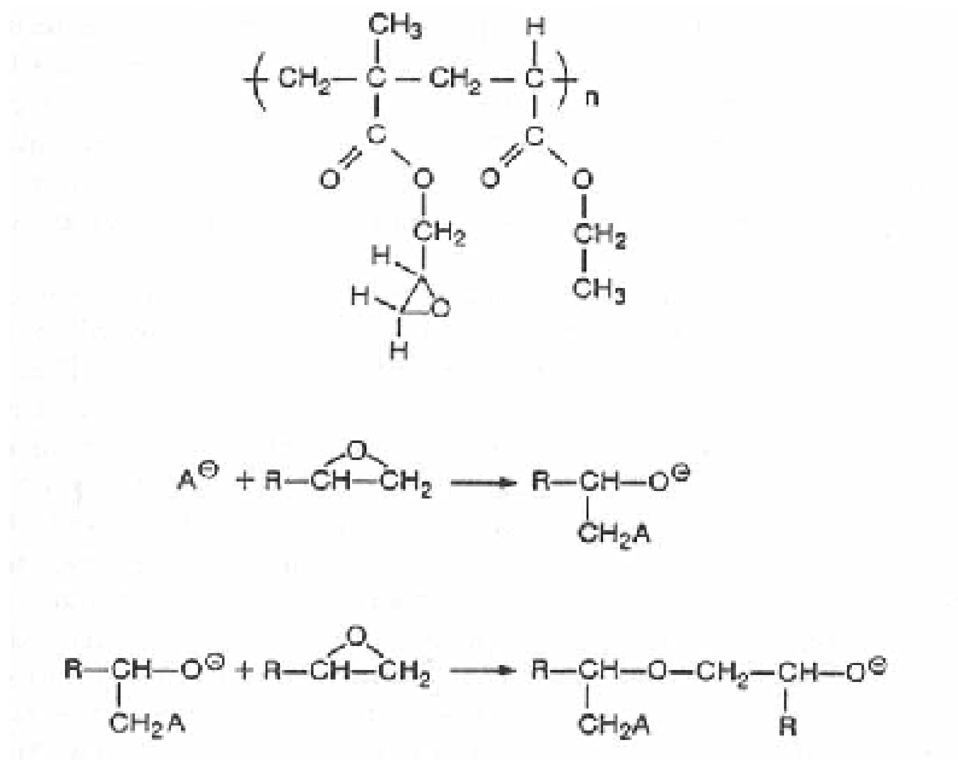


Figure. 2.2: The cross linking mechanism for COP. [56]

Table 2.1. The characteristics of positive and negative resists

Positive resists	***Negative resists***
High resolution	Better adhesion to some substrate surface
Aqueous based solvents	More sensitive
(some optical photoresist)	(higher exposure throughput)
Organic-based solvents	Relatively tolerant of developing conditions
(some electron photoresist)	
Low sensitivity	Better chemical resistance
	better mask material
	Less expensive
	Lower resolution
	Organic-based solvents

2.5.5 Commercially used e-beam resists

2.5.5.1 The positive e-beam resists [57]

Commercially available e-beam resists are illustrated in table 2.2

1) PMMA (Poly methylmethacrylate);

PMMA is one of the first materials developed for e-beam lithography. This is highest resolution resist available. [52] [58] [59]

2) EBR-9 (poly(2, 2, 2-trifluoroethyl-α-chloroacrylate) [60]

This resist is 10 times faster than PMMA, but its resolution is more than 10 times worse than that of PMMA.

3) PBS (Poly butene-1-sulphone) [60]

For high-volume mask, this is effective, but, for small to medium scale mask production, it is slow.

4) ZEP (a copolymer of chloromethacrylate and methylstyrene) [61]

ZEP is an order of magnitude faster than PMMA and resolution is almost same as that of PMMA. However, the price is high and it is difficult to inspect the pattern in the SEM due to its sensitivity to electrons.

2.5.5.2 The negative tone e-beam resists [57]

1) COP (an epoxy copolymer of glycidyl methacrylate and ethyl acrylate) [57] [62]

This is a very high speed resist, but relatively poor resolution (1um).

2) Shipley SAL (a base polymer, an acid generator, and a crosslinking agent).

This is one of the highest resolution commercially available negative resists and has a

Table 2.2. Comparison of commercially available electron beam resists [63]

	Tone	*Resolution nm*	*Sensitivity $\mu C/cm^2$*	*Developer*
PMMA	Positive	10	100.0	MIBK:IPA
EBR-9	Positive	200	10.0	MIBK:IPA
PBS 250	Positive	250	1.0	MIAK:2-Pentanone 3:1
ZEP 10	Positive	10	30.0	Xylene:p-dioxane
COP	Negative	1000	0.3	MEK:ethanol 7:3
SAL-606	Negative	100	8.4	MF 312:water

superior sensitivity. But, in the high voltage region this shows lower resolution. [64]

2.6 Proximity effect

Electron beam lithography is one of tools that can generate high resolution patterning. Normally the smallest beam size is about ~ 5nm (50keV) and thus it is possible to fabricate very fine size of patterns which are theoretically about 5nm if there is no other factors. However, actually there are a lot of factors affecting lithographic performance. Electron optic aberration and beam diffraction are two of those factors, but the strongest factor is electron scattering inside materials. As a result of scattering of electrons in the resist and the substrate, homogeneous incident electron exposure results in a non uniform exposure intensity distribution in the pattern area and then undesired influence on intended patterning. This effect is referred to as proximity effect. As the size of circuit pattern decreases and density increases, proximity effect is more and more severe because the neighboring features can be merged or feature shape can be transformed regardless of perfect electron beam condition.

This effect is characterized in two ways. One way is a variation between patterns and the other way is a variation inside a pattern. [65] [66] [67]

2.6.1 Electron Solid interactions

Electron beam in the e-beam lithography has complex interaction with the polymer film and substrate as the electrons are exposed on those materials. These interactions generate three types of electrons having different energy and spatial distribution determining beam

diameter. In Figure 2.3, simulated trajectories of electrons in PMMA film on Si and schematic electron scattering in electron resist exposure.

2.6.1.1 Forward scattering

As electrons penetrate the resist, they can collide with an electron of an atom belonging to resist or substrate. Some fraction of them will experience small angle diffraction, which can result in a significant broadening of primary beam profile at the bottom of the resist. When resist received the extra energy from electrons, molecule chain may break due to the excitation and ionization.

The increase of beam diameter due to forward scattering can be defined by following equation.

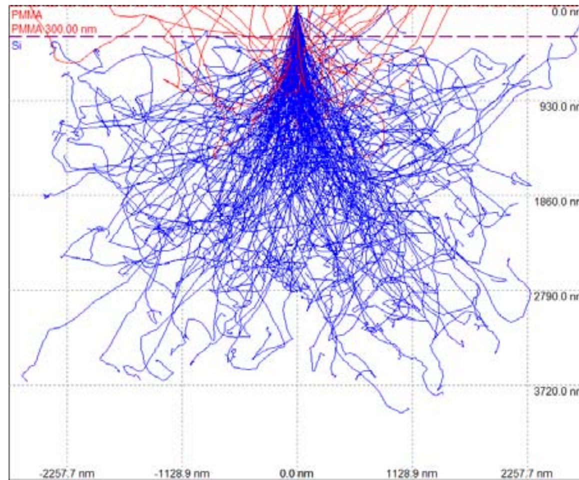
$$d_f = 0.9(R_f / V_b)^{1.5} \qquad (2.4)$$

d_f: beam diameter

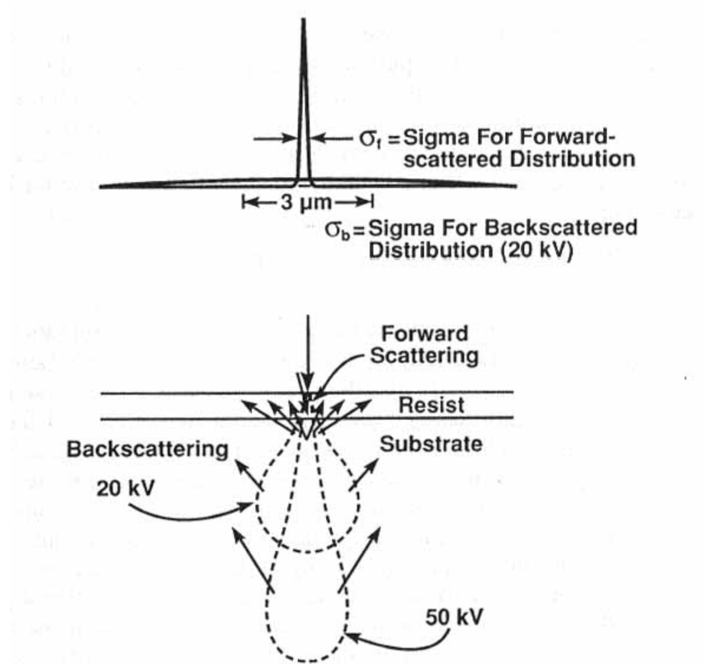
R_f: resist thickness

V_b: beam voltage in kV

Forward scattering can be minimized by applying the thinnest possible resist and the highest available accelerating voltage. [59] [63]



a)



b)

Figure 2.3: a) Simulated trajectories of electrons in PMMA film on Si and b) schematic electron scattering in electron resist exposure. [59]

2.6.1.2 Back scattered electron

As the electrons penetrate through the resist into the substrate, some of them experience large angle scattering events with some spatial distribution. [51] [65] [68] These electrons are turning back through the resist at some distance from the incident beam with its initial energy.

These electrons are called backscattered electrons and cause proximity effect. [69] The back scattered yield is roughly independent of beam energy. It is, however, strongly related to substrate materials. Substrate which is low atomic number gives less back scattered electrons than substrate with high atomic number. When it comes to relationship between back scattered yield and beam energy, the range electrons travel is related. As the beam energy high, range of proximity effect increases.

2.6.1.3 Secondary electrons

As the primary electron slow down, much of their energy is dissipated in the form of secondary electrons with energies from 2 to 50eV. They have only a few nanometer of spatial range in resist and thus contribute little to the proximity effect but this can cause effective widening of beam diameter together with forward scattering by roughly 10nm. [59] [70] [71]

2.6.2 Proximity effect correction

2.6.2.1 Models of energy profile

Proximity effect correction scheme requires electron energy density profile deposited at certain exposed point, which is called point spread function. The important properties of this profile are as follows. [72]

1) The shape is independent of dose

2) The shape does not change with position for homogeneous and planar substrates

3) The shape is a function of the system parameters

The profile due to a point exposure is normally expressed as double Gaussian function and given by equation (2.5) [67] [73]

$$f(r) = C_1 \exp(-(r/\beta_f)^2) + C_2 \exp(-(r/\beta_b)^2) \tag{2.5}$$

where the parameter β_f is defined by the forward scattering, β_b by the backscattered electrons, C_1 and C_2 are constants, and r is the distance from the point of electron incidence. More popular expression is given as following equation (2.6). [74]

$$f(r) = \frac{1}{1+\eta}\left(\frac{1}{\pi\alpha^2}\exp\left(-\frac{r^2}{\alpha^2}\right) + \frac{\eta}{\pi\beta^2}\exp\left(-\frac{r^2}{\beta^2}\right)\right) \tag{2.6}$$

where η is the ratio of backscattered energy to the forward-scattered energy, α is the forward scattering range parameter and β is the backscattering range parameter.

For some types of substrate, resist and very small feature size, PSF expressed by double Gaussian function is insufficient. Therefore, improved function such as triple and multi Gaussian function has been proposed. Very accurate results have been obtained by adding an extra exponential term as shown in equation (2.7). [74] [75]

$$f(r) = \frac{1}{\pi(1+\eta_1+\eta_2)}\left(\frac{1}{\alpha^2}\exp\left(-\frac{r^2}{\alpha^2}\right)+\frac{\eta_1}{\beta^2}\exp\left(-\frac{r^2}{\beta^2}\right)+\frac{\eta_2}{24\gamma^2}\exp\left(-\sqrt{\frac{r}{\gamma}}\right)\right) \quad (2.7)$$

The third term is introduced to explain any additional exposure which is not included in the first two terms and its width γ is a few hundreds of *n*m. η_2 represents the ratio of this additional exposure to the first term. [76] [77]

In general, the energy profile varies with depth and radius and two dimensional energy profiles also can be obtained by averaging the values according to depth and it result in greatly reduced computation time and correction.

2.6.2.2 Type of proximity correction

2.6.2.2.1 Dose correction methods

The most common technique of proximity correction is dose modulation which assign proper dose to the each individual shape in the pattern to make the feature print with its original shape. [78]

Several different algorithms have been used and developed. Most of them are using double Gaussian energy distribution profiles and convoluting them with the exposed area. Deposited energy on each pixel can be calculated and dose amount which will be exposed

on the each pixel can be controlled to adjust the energy density for desired developing threshold.

Earliest one applying above algorithm was self-consistent correction. Let Q_j be dose applied to pixel j and N the total amount of pixels. The total energy on pixel i will be [79]

$$E_i = \sum_{j=1}^{N} R_{ij} Q_j \tag{2.8}$$

$$R_{ij} = \frac{\overline{\Delta V_f}}{t}\left[\frac{1}{\pi\alpha^2}\exp\left(-\frac{r_{ij}^2}{\alpha^2}\right)+\frac{\eta}{\pi\beta^2}\exp\left(-\frac{r_{ij}^2}{\beta^2}\right)\right] \tag{2.9}$$

where ΔV_f (J) represents mean energy loss by electrons and r_{ij} is the distance between pixel centers of i and j.

Above equations can be expressed as matrix notation for all i and given by equation (2.10).

$$[E_i] = [R_{ij}][Qj] \tag{2.10}$$

However, above method does not correct proximity effects exactly because it is only consider exposed pixel, not unexposed pixels.

Variants and improvements of this algorithm were introduced and achieved superior proximity effect correction. However, there is still critical problem of computation time

as number of the shapes increase and the pattern sizes decrease.

2.6.2.2.2 Shape modification methods [78]

In this method, the shapes in pattern image are modified such that the extra doses from the nearby patterns are compensated by slightly reducing their size and developed image is almost close to the original image. To determine how much size will be modified, experimental data for the dose amount of the area is needed. This technique is very useful for the machines which are not capable of dose modulation and also relatively accurate result can be obtained. However, for the features whose dimension is close to the scale of pixel size of the electron beam system, it is inappropriate.

2.6.2.2.3 Background exposure correction [78] [80]

This method, often referred to as GHOST, perform the correction by writing the inversed tone of pattern using defocused spot and then make back ground dose roughly uniform as shown in figure 2.4. The advantages of this method are that it does not require any computation time. However, it has some disadvantages such as extra writing time, moderate loss of contrast. In addition, there is slight minimum resolution due to only correction of backscattered ground, not proper correction of forward scattering.

2.6.3 PYRAMID

PYRAMID is a hierarchical, rule-based proximity correction method. Main advantage of this method is correcting circuit patterns quickly and accurately. [72]

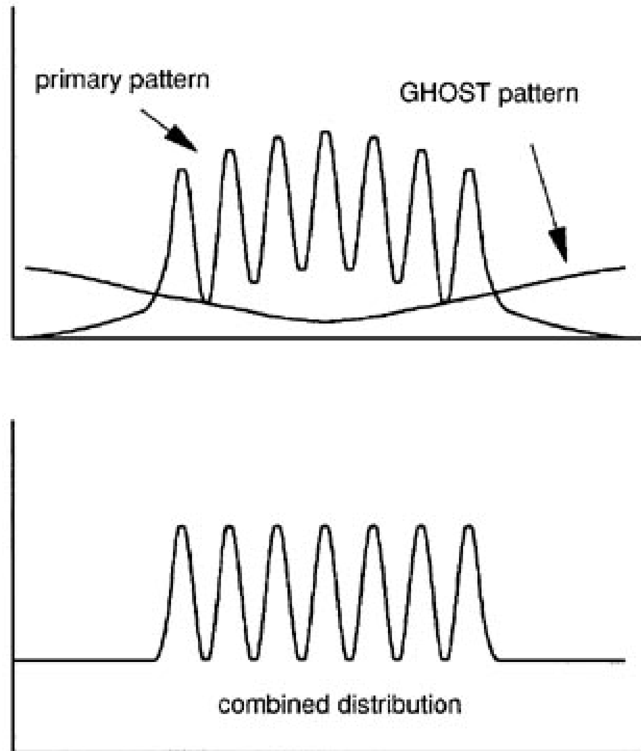


Figure 2.4: Schematic showing how the GHOST technique can be used to correct proximity effect. [80]

Throughout each correction, pre calculated rule tables are used and these rule tables depend on system parameter such as resist type, thickness, substrate type and particular circuit being corrected. Referring these computationally complex calculations can significantly cut the execution time.

The heart of hierarchical correction scheme is the digital image processing (DSP) model of electron beam lithography. This model calculates the energy received by any pixels in the patterns and determines how much correction should be made to a given pattern. Implementing this DSP model in a simple way is extremely computationally intensive and time consuming. PYRAMID introduces two-level hierarchical approach of exposure which can be decomposed into two components, local and global exposures to correct patterns quickly and accurately. [81] In the last stage of PYRAMID, hierarchical corrections consider each rectangle in the circuit and then take into account the interactions among neighboring circuit elements.

2.6.3.1 Digital signal processing (DSP) model [72] [4] [81]

The digital image processing model is illustrated in figure 2.5. The first step in this model is to produce 2-D digital image array $\left(f(i,j)\right)$ of patterns and each pixel in image represent the dose assigned to corresponding pixel in the resist. This image then is convolved with energy deposition profile $\left(h(i,j)\right)$ in which each pixel represented actual energy deposited on corresponding pixel and 2-D convolution array $\left(g(i,j)\right)$ is obtained.

$$g(i,j) = f(i,j) * h(i,j) \tag{2.11}$$

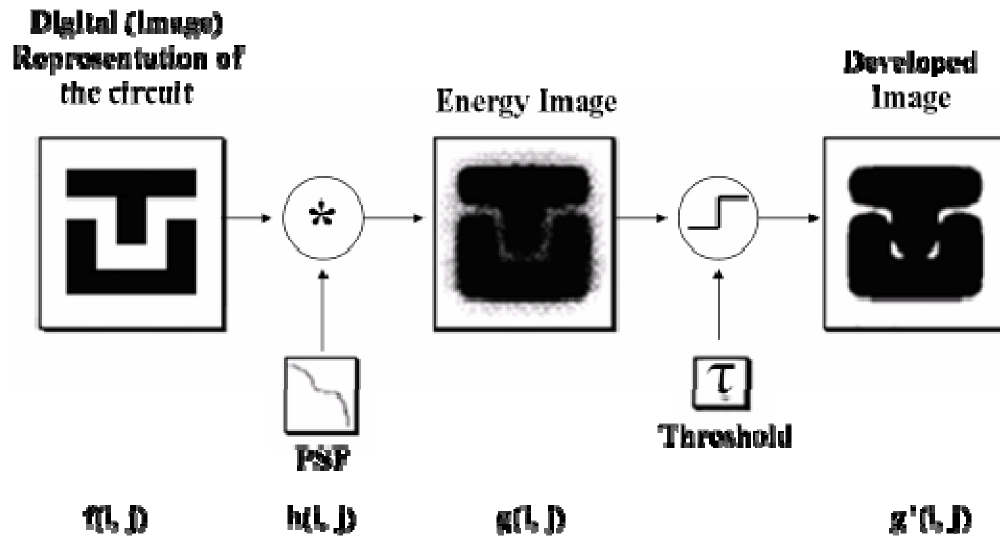


Figure 2.5: Image processing model used to simulate the exposure of a circuit pattern. [72]

Applying experimentally determined developing threshold results in a binary image representation of the developed pattern.

$$g(i,j)' = \begin{cases} 0 & if\ g(i.j) < \tau \\ 1 & if\ g(i,j) \geq \tau \end{cases} \qquad (2.12)$$

where τ is experimentally determined development threshold.

2.6.3.2 Global exposure [72] [4] [81]

Global exposure is an approximation of the exposure on circuit elements located far away from the critical point and is calculated through a coarse grain convolution because energy profile in this region smoothly change. 2-D point spread function (PSF) calculated from 1-D PSF is applied to calculate energy deposition

2.6.3.3 Local exposure [72] [4] [81]

Local exposure considers circuit area located close to the critical point and calculates the deposited energy exactly with pixel by pixel because energy profile around point of incident significantly changes. An efficient and exact scheme, referred to as cumulative distribution function (CDF) method, was developed and applied for rectangular features.

2.6.3.3.1 CDF method [81]

A look-up table or CDF table is precalculated, which contains exposure contribution to the origin from various sizes of rectangular features where one vertex of each rectangle is

at the origin. The exact calculation of exposure contribution from a rectangular feature then can be calculated with information of CDF table. The CDF convolution method is illustrated in figure 2.6.

2.7 Metrology

The photolithography process consists of aligning and optically transferring the pattern from a recticle onto the wafer which has photo resist coated on it. The resist is then developed and the resist image is transferred into the underlying material with the processes of dry, wet etch or implant, etc. This process may be repeated 15 to 25 times to generate a complex integrated circuit. In order to achieve proper device function, high product yield and reliability, it is necessary to ensure that levels are precisely aligned to one another among layers and to control critical dimensions within each patterned layer. [82] However, decreasing minimum feature size, increasing circuit density and great chip area make it difficult to control the effective alignment of layers and maintain the constant pattern dimension among lots and wafers. [83] Hence, the proper determination of image size and registration are very crucial and represent two of the primary goals of metrology as they are applied to the manufacture of integrated circuits.

2.7.1 Overlay metrology

Overlay is the process of aligning one layer to the subsequent layer in the photo lithographic process. There are two major roles of overlay metrology for microlithography. The first is termed lot dispositioning. If measured overlay exceeds

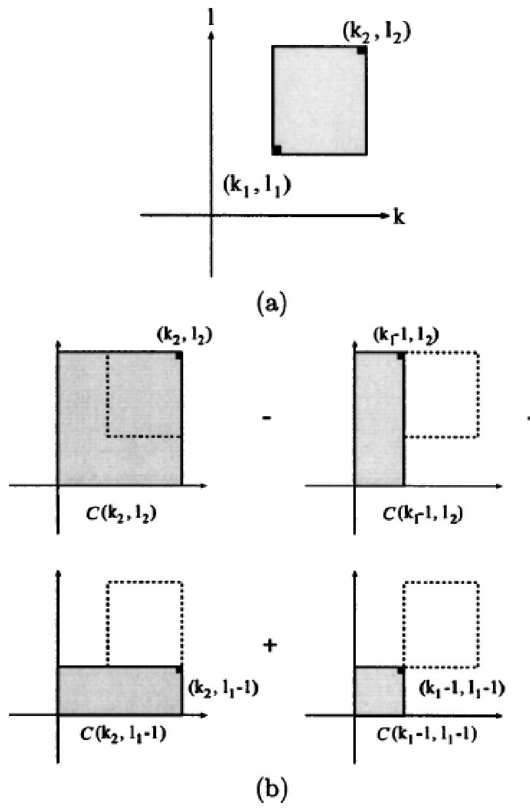
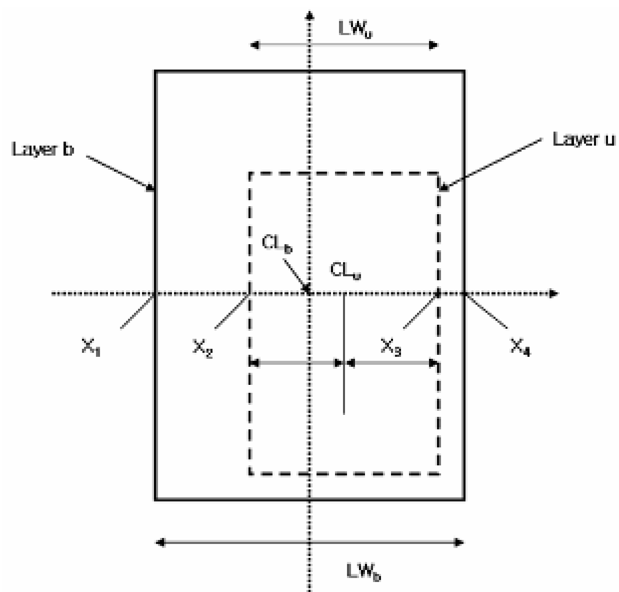


Figure 2.6: Illustration of the CDF convolution methods: (a) the convolution value(Conv) of rectangle at the origin is calculated and (b) a graphical description to obtain Conv.

some allowable threshold, the lot can not proceed to the next process step. This generally results in rework and the lot carried out should be returned to the previous lithography step after the resist is stripped. If the measurement is done after etch, lots outside of allowable threshold should be scrapped. [84]

The second use of overlay metrology is correction of exposure tool. Normally, the overlay is measured at four corners of the field and over several fields on the wafer, which provides the statistical sampling to obtain information to calculate stepper corrections model. This model includes intra- field and inter-field correctibles, such as offset, rotation and scale. Those correctibles enable the exposure tool to improve the performance on subsequent lots.

To measure overlay alignment, the first level on a wafer has a target which is represented by the large outer box, normally 20µm in size and the second level also has smaller inner box whose size is 10µm. Overlay error is defined as the planar distance from the center of the substrate (n level target) to the center of the next level (n +1 level) target. [85] The parameter defining this error is called overlay (O/L) or centerline overlay. Since microlithography involves patterning many features in each layer, a set of centerline coordinates, called registration [86], is of primary interest and centerline determination method is shown in figure 2.7. Registration, denoted R(X; Y), is a vector field made up of centerline vectors of all features in a layer. [87] The centers of symmetry of two boxes are designed to match each other. Overlay, however, appears as misregistration between the centers of symmetry of two layers due to many factors.



$$LW_b = |X_2 - X_3|$$

$$LW_u = |X_1 - X_4|$$

$$CL_b = \frac{X_4 + X_1}{2}$$

$$CL_u = \frac{X_3 + X_2}{2}$$

$$O/L = CL_u - CL_b$$

$$O/L(X;Y) = R_u(X;Y) - R_b(X;Y)$$

Figure 2.7: Centerline determination. [87]

2.7.1.1 Error source

Overlay measurement is also very sensitive to error sources resulting from measurement tools. Therefore, it is necessary that the effect of the measurement tool to the total error should be well controlled and minimized for all process levels.

2.7.1.1.1 Low edge contrast [88] [89]

As density of devices and number of interconnect levels increase, it is required to minimize the impact of the non planarity of successive layers on devices and process performance and chemical mechanical polishing (CMP) technique for planarization have become critical. Low-contrast edges result from the process of planarization of successive layers whose height difference is less than 100 Angstroms. This results in extremely low signal difference and potentially new forms of target asymmetry which causes low signal to noise ratio and makes it difficult to distinguish the target for the repeated measurement.

2.7.1.1.2 Accuracy

Optical aberration, illumination and alignment are unavoidable problems for the system optics. A simple and quantitative metric of the quality of the optical metrology toll is tool-induced shift (TIS) which is the tool error component of overlay measurement that is significantly related to the accuracy of device overlay measurement. [84] [90] [91] TIS can be quantified by overlay measurement of the same feature at 0 and 180° (wafer) rotations and given by equation(2.13)

$$TIS = (OVL(0^{0)} + OVL(180^{0}))/2 \qquad (2.13)$$

Nonzero TIS indicates that the metrology tool has performed with a systematic discrepancy in the overlay result due to the system imperfections mentioned. [84]

Another source of measurement inaccuracy is referred to as wafer-induced shift (WIS) which accounts for the errors due to asymmetry in the measurement structures. [90] [91] This error can be quantified by a symmetric tool on a symmetric target coated with asymmetric resist film which gives an asymmetric signal.

2.7.1.1.3 Precision of the tool [92]

The precision of overlay measurement tool should be significantly qualified. This component can be quantified by performing repeated measurements of a sample to obtain a statistically significant quantification of the measurement variation with carefully designed analysis.

2.7.2 Critical Dimension (CD) metrology (linewidth metrology)

Just as lithographic advancements have tightened layer-to-layer overlay tolerance, decreasing line width increasingly demands the tolerances on critical levels for linewidth measurement. [93]

In figure 2.8, the definition of linewidth is the quantity ($y_2 - y_1$) defined at the distance x_0 along the resist line and at height z_0 . [94] [95] [96] Linewidth measurement tool is expected to both quantify the magnitude of linewidth variations and verify their reduction

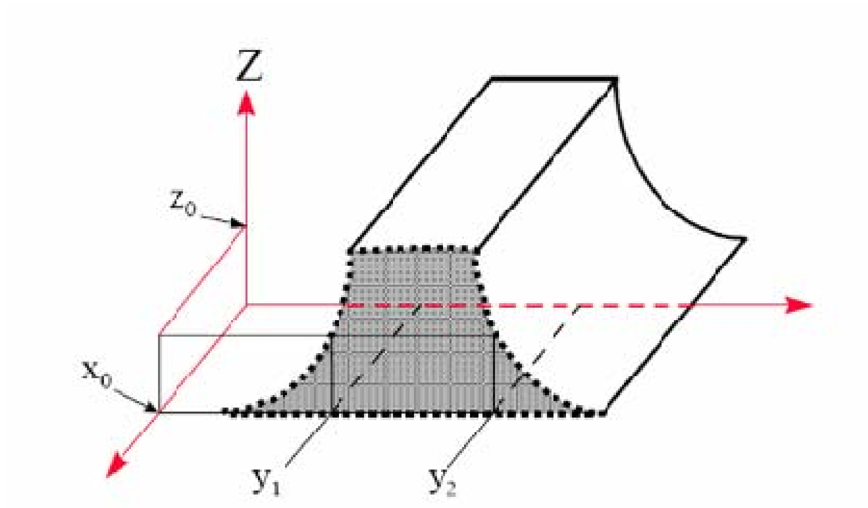


Figure 2.8: Definition of linewidth (Critical dimension). [95]

as the process improves. The measurement of minimum feature size, Critical Dimension (CD), was based on the optical microscopy which is technique over a hundred years old when critical feature size exceeded 1μm. [5] [95] As features shrink below the wavelength of light, it is turned out that the size and shape of a structure affected the precision and accuracy of the optical measurement tool. Therefore, industry has turned to and applied other tools like scanning electron microscopy (SEM) and scanning probe microscopy [97] which can measure smaller size features. Currently, advanced optical technology is taking growing interest because this can provide more complete information with imaging 3 - D shape, sidewall angle and the thickness of films. [98]

Although new technology such as optical techniques and scanning probe microscope is recognized as alternative tools, CD-SEM remains the best option for the most critical process, and other technologies are considered as complementary rather than competing.

2.7.2.1 Uncertainty in CD measurement

Actually the definition of linewidth is not clear for the structures typically encountered in IC technology. The line edges is normally ragged and side-walls are asymmetric as shown in figure 2.9. There are two factors mainly creates uncertainty in CD measurement.

The choice of height at which the measurement is performed is highly dependent on the fabrication process. For example, measuring the linewidth may be carried out at the bottom of resist structure generated from the highly selective etch process. The measuring point, however, must be different if resist is in the less selective etch process.

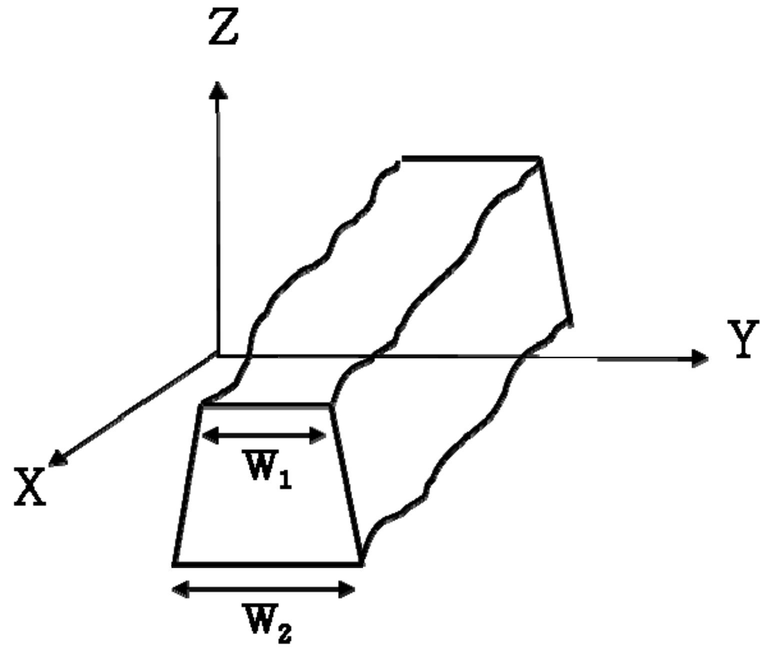


Figure 2.9: Three dimensional representation of a line profile. [97]

Another major factor which has effect on measuring linewidth is line edge roughness (LER). The difference of width measured at various cross section is depending on the degree of LER. [97] [99]

2.7.2.2 Linewidth metrology tools

2.7.2.2.1 Scanning Electron Microscopy (SEM)

Scanning electron microscopy (SEM) has been typically applied to measure CD since the semiconductor industry was undergoing a technological transition into the submicrometer range of device dimension. [5] [95]

SEM can provide high resolution and a large depth of focus which can measure outside the range of optical microscope and relatively rough surfaces even at high magnification. Even with these advantages, rapidly decreasing linewidth are not clearly detected and measured by this instrument. [6]

Thus, the tight CD control demands more improvement in SEM performance to reach best device performance through stabilization of manufacturing process.

Early scanning electron microscopy operated at relatively high (typically 20-30keV) accelerating voltages in order to obtain both the best signal to noise ratio and image resolution. [6] [100] On the other hand, early SEM at high voltage showed several problems.

In case of measuring non conduction material, it requires coating of some material to provide conduction to ground and to improve SE signal generation from the surface at this high voltage. Further, those instruments were designed to accommodate relatively small samples and thus large samples such as a large wafer should be broken prior to

inspection. The high energy electrons interacting with the sample can also damage sensitive devices.

As wafer size became larger, this process is undesirable and very costly. Hence, the improvement to overcome those problems is demanded and this requirement was driving the incorporation of field emission sources for improved low acceleration performance, large chamber capability, improved lens designs, clean pumping systems, and digital frame storage. [100]

On-line inspection in an SEM required that the sample should not be broken, viewed at a low accelerating voltage below the point where electron damage is not problem without coating.

2.7.2.2.2 Atomic Force Microscope

Atomic force microscopes have become valuable complementary instruments for scanning electron microscopy for inspection of surfaces on submicron scale. Standard AFM is equipped with a conical tip and measuring the depth of shallow and narrow features, which is strongly depending on tip dimension.[101] Another application of AFM is the measurement of sidewall angles and widths of structures such as via holes, line, and trenches. However, AFM of a conical tip shows highly inaccurate measurement results when the sidewalls are steep and angles are larger than 70°. Recent technical developments have introduced a new method for accurate measurement of line and trench width, using a flared tip and an improved scanning and it is referred to as Critical dimension AFMs (CD-AFMs). [102]

There are several advantages of CD-AFMs for metrology. This method does not require

the breaking of wafer to measure the side and tip is easily located thorough the center of a pattern. Another advantage is that it can collect cross-sectional data at several positions along a line or trench which enable averaging of surface roughness. [97] [101] In spite of its many advantages, low throughput is a critical factor to limiting AFM application for the CD metrology. [101]

2.7.2.2.3 Scatterometry metrology

Scatterometry is an optical metrology based on the analysis of light scattered from a periodic array of features such as line/space photoresist gratings or arrays of contact holes. This method has many attributes common to other optical metrologies. It is simple and inexpensive, and its measurement shows high precision repeatable and consistency with other methods, high accuracy. [103] [104]

The scattered or diffracted light pattern, referred to as a signature, can be used to characterize the details of grating shape. For a periodic device such as a series of lines and spaces in resist, the angles of scattered light are given by the grating equation. [98]

$$n\lambda = d(\sin\theta_i + \sin\theta_n) \qquad (2.14)$$

λ : Wavelength of the incident light

θ_i : The angle of incidence in air

θ_n : The angular location of the nth diffraction order

d : The spatial period

Diffraction signature is very sensitive to the shape and dimensional parameters and can be used to characterize its structure due to the complex interaction between incident light and sample. In addition, thickness of photoresist, the line width, and the thickness of underlying film layers can also be measured from analysis of scattered light pattern with using proper model. [103]

The advantages of scatterometry metrology other than described above is that it provides complex 2-D and 3-D information non-destructively.

CHAPER 3

FABRICATION OF FRESNEL ZONE PLATES

3.1 Background

3.1.1 What is Fresnel zone plate?

A Fresnel zone plate is a diffractive optic device and is the best tool for focusing and imaging with soft x-rays because it can generate the smallest focal spot of electromagnetic radiation at any wavelength. Zone plates perform constructive interference of light rays from adjacent zones to form a focus. In figure 3.1, the focal length f of a zone plate which is given by equation (3.1) is a function of its diameter *OD*, its outermost zone width ΔRn and the x-ray wavelength λ.

$$f = OD\Delta Rn / \lambda \tag{3.1}$$

The resolution of a zone plate is limited to 1.22 ΔRn which is Raleigh criterion and also, the positioning of all zones which should be positioned in the range of about a third of their width and the thickness of the zones which should be sufficient to adequately attenuate or phase-shift the transmitted x-ray front are important factors for the best performance of zone plate as well. When it comes to the resolution of zone plates, how outermost ring is fabricated in smaller scale is important issue. Normally Fresnel zone plate is fabricated on transparent thin membrane such as silicon nitride membrane (Si_3N_4) for optical purpose.

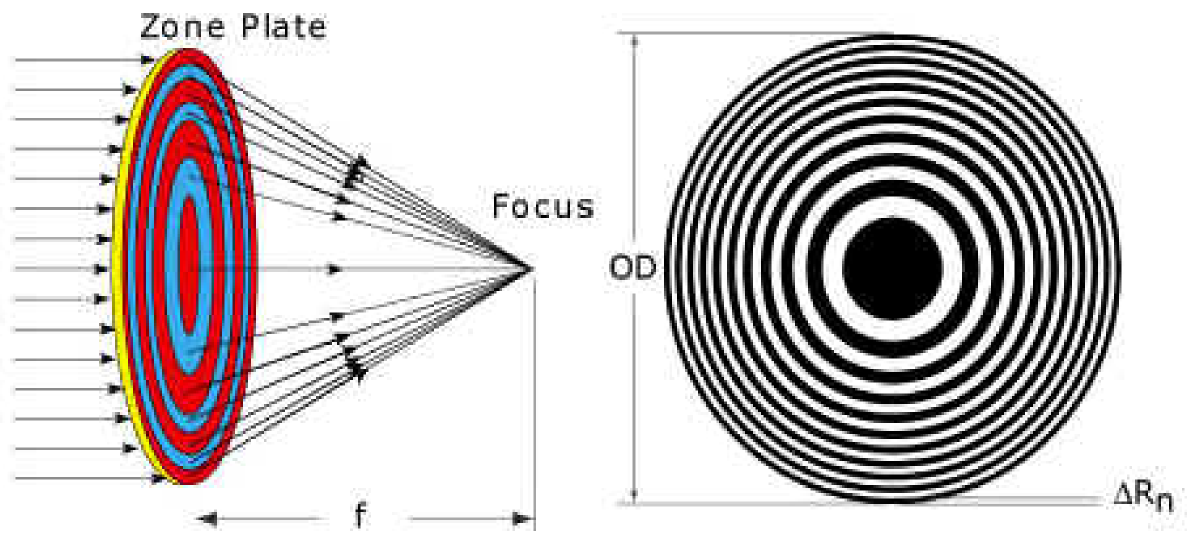


Figure 3.1: The schematic of a Fresnel zone plate.

Electron beam in electron lithography almost pass through the thin membrane and then there is a little less proximity effect which makes process easy. However, as outermost ring widths are smaller and smaller, there are proximity effect problems due to high pattern density although it still has much less proximity effect compared to metal substrate. This will be one of the limiting factors to fabricate better resolution of Fresnel zone plate.

The fabrication schemes of zone plates for the optical purpose suggested by D. Tennant et. *al* are illustrated in figure 3.2 and 3.3. [105] Pattern is first fabricated on resist and then transferred to below layers by post process such as RIE. Thicker resist have more proximity effect due to forward scattering and thus resist should be as thin as possible to reduce it, while it also should be thick enough to be a mask layer for mask etching at the same time. From the schemes, zone plate size fabricated on resist determines final dimension of zone plate although zone width can change with corresponding post processes. The method of fabrication of zone plates employed by A. Ozawa et. *Al* also shows similar schemes and indicates the importance of pattern sizes fabricated on resist, first layer.[106]

We fabricated zone plate on Silicon, not on membrane with several purposes. First purpose is to study proximity effect and control of it. Previously mentioned, Fresnel zone plate is highly dense structure and thus there are considerable proximity effects arising from zones during beam exposure. Therefore, zone plate is an optimum structure to study proximity effects and we controlled them during the fabrication of zone plates.

Secondly, current zone plate has an outermost ring width of larger than 30nm due to proximity effect even if it is fabricated on membrane. We can provide the optimum

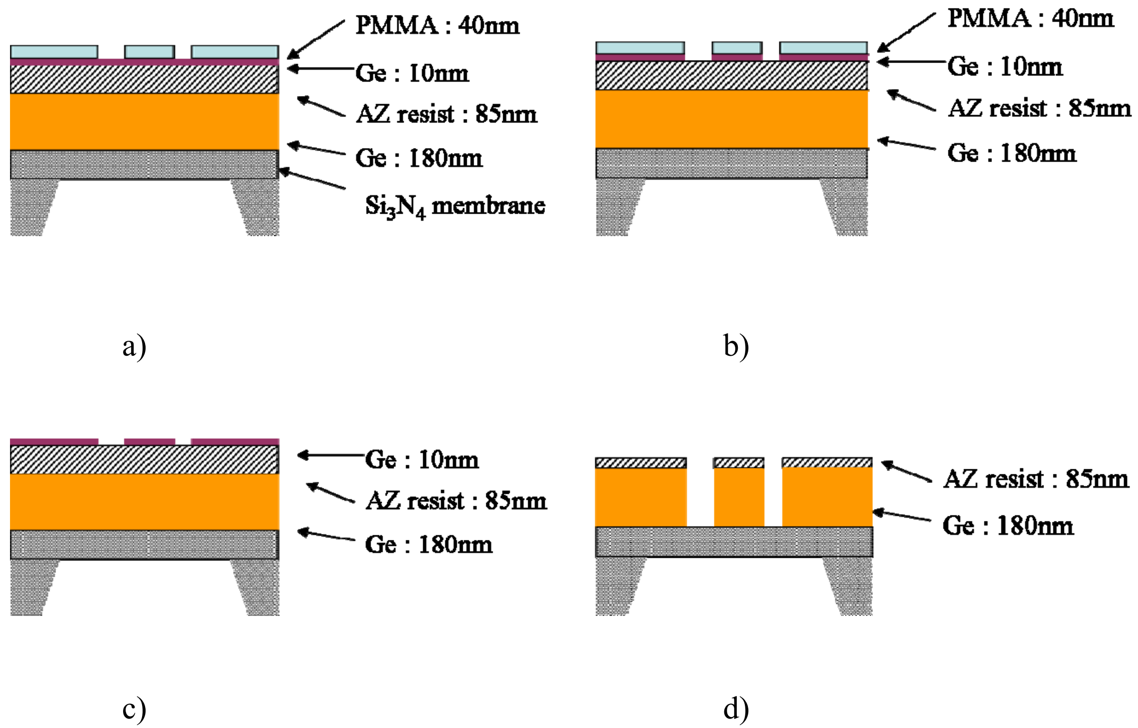


Figure 3.2: Fabrication of Fresnel zone plate on Si_3N_4 . a) exposure and development, b) RIE(reactive ion etch) thin Ge mask, c) RIE AZ Photoresist, d) RIE thick Ge substrate.

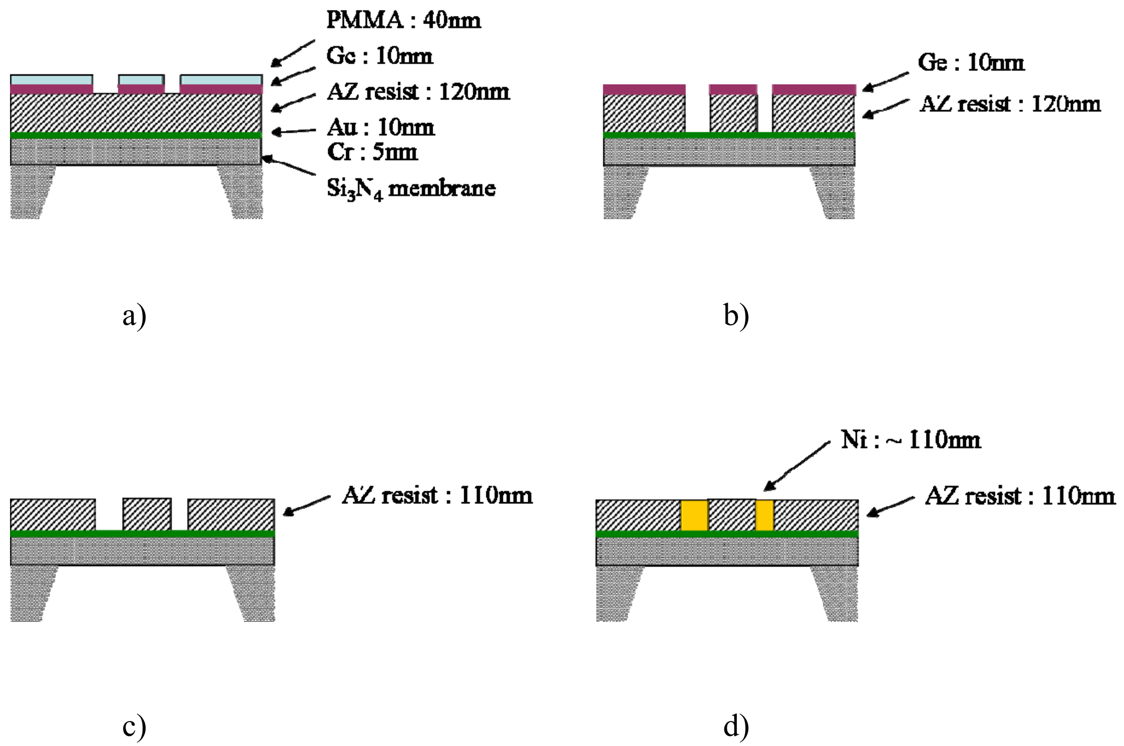


Figure 3.3: Fabrication of Fresnel zone plate on Si_3N_4 with a trilayer resist and electroplating. a) exposure, development, and RIE (reactive ion etching) thin Ge mask, b) RIE AZ photoresist, c) RIE Ge, d) electroplate Nickel.

methods such as lithography conditions and control of proximity effects to fabricate smaller dimension of zone plates on membrane with the successful fabrication of zone plates on metal substrates such as Silicon which has much more proximity effect.

Third purpose is that we use zone plates as test tools for electron optical systems. For this purpose, Zone plates should be fabricated on solid and steady substrate, not on fragile and weak membrane.

3.1.2 Why a Fresnel zone plate?

The factor which has most limited the application of Fourier and other standardized analytical techniques to test tool imaging performance has been the availability of suitable test targets. Common practice has been to use specimens such as gold or platinum particles dispersed on carbon for the determination of imaging resolution because they can be easily prepared and give high contrast and a useful amount of high spatial frequency information. However, these samples are random, each is unique, poorly controlled, and irreproducible. Such samples also typically contain materials which could introduce contamination if used inside *in-line* tools. Consequently, when using such samples, it is impossible to generate reliable results and either to properly verify a specification or to compare two tools in different locations. The ideal sample would be one that could be replicated at low cost with the same specification and which offered high contrast, isotropically dispersed detail with a spatial frequency content which extends beyond the resolution range of the imaging tool. With such a specimen the extension of the Fourier transform power spectrum would be limited only by the imaging performance of the tool rather than being constrained by the sample.

Fresnel Zone Plates have highly dense, small and symmetric structure, and have various zone widths which can provide information from high spatial frequency to low frequency through Fourier Transform. Therefore, this can provide much useful information such as optical resolution, beam drifting, beam instability by taking image of it on SEM and test performance of tools.[7]

3.2 Electron beam lithography (JBX-6000FS/E)

We used JBX-6000FS/E from JEOL to fabricate Fresnel zone plate and the other patterns which will be introduced later in this thesis. The schematic of Electron optics system of JBX-6000FS/E is illustrated in figure 3.4.

The emission source of the system is a high-brightness electron gun using a zirconium oxide coated tungsten thermal field emitter (ZrO/W TFE) and an in-lens deflector is employed. The operation modes are the 4th lens-mode and the 5th lens-mode. The 4th lens mode is used for writing of relatively large patterns with a diameter as small as tens of nanometers at large field. The 5th lens mode is for small patterns with a beam diameter of minimum 5nm at small field. In addition, two accelerating voltages can be applied and are manually convertible: 25 and 50KeV. The beam diameter and field size according to operation modes and accelerating voltage is shown in table 3.1. The vector scanning is used and step and repeat method for work piece stage movement is applied as shown in figure 3.5. Cassettes hold a wafer of up to 5-inch and a mask up to 7-inch for the mask fabrication. Continuous pattern writing can be accomplished on up to 12 consecutive cassettes from one time operation. The position of stage is detected by a laser interferometer whose resolution is $\lambda/1024$, about 0.62 *n*m. Four ion pumps are employed

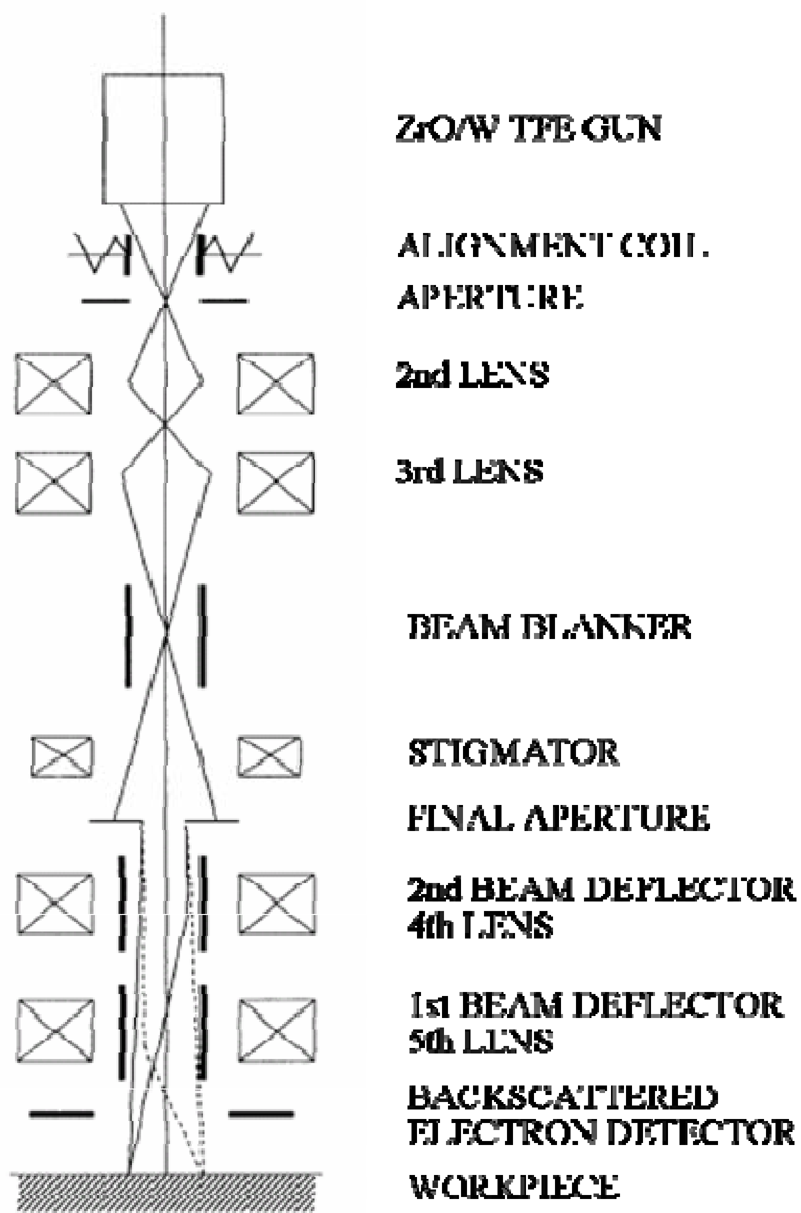


Figure 3.4: The schematic of Electron optics system of JBX-6000FS/E

Table 3.1. Field size, scanning step and beam diameter (minimum) according to operation modes and accelerating voltage

Mode No.	Accelerating voltage(keV)	Objective lens	Field size (μm)	Scanning step(nm)	Minimum beam diameter(nm)
1	25	4th	1600*1600	25	30
3	50	4th	800*800	12.5	20
5	25	5th	160*160	2.5	7
7	50	5th	80*80	1.25	5

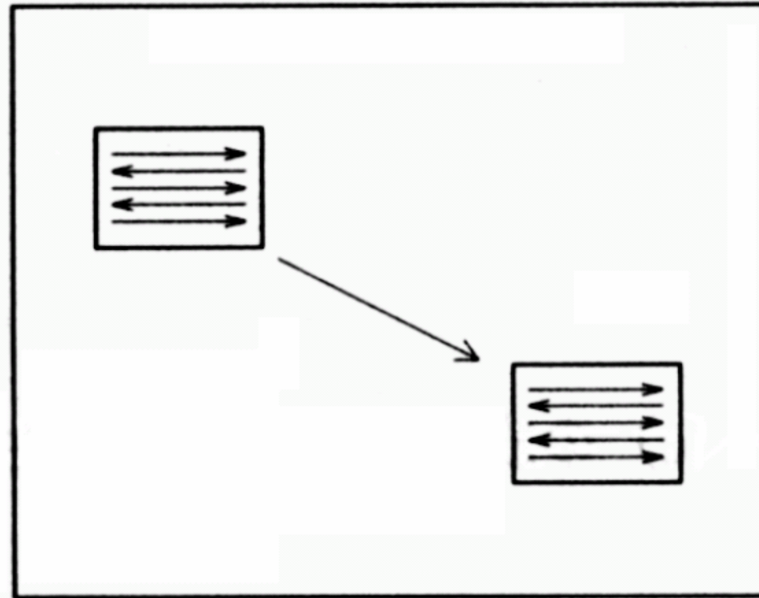


Figure 3.5: The schematic for vector scanning and step and repeat method

to evacuate the electron gun chamber and EOS column at pumping speed of 20L/sec to maintain high vacuum. For roughing, two oil rotary vacuum pumps (250L/sec and 610L/sec) and one turbo molecular pump (1,000L/sec) are used and one ion pump (400L/sec) is evacuating the workchamber (main chamber). Turbo pump is mainly used to evacuate the workpiece exchange chamber (autoloader).

3.3 Experiment

3.3.1 Design of Fresnel zone plate

Fresnel zone plate is constructed as illustrated in figure 3.6. Fresnel zone plate consists of a sequence of concentric rings in which the radius r_n of the *nth* ring (r_0 and n_0 are the center point of zone plate) is calculated by equation of $r_n = a_0\sqrt{n}$ and the area b_n and b_{n+1} is the same. Depending on the number of the rings, their width, and their diameter, such a structure provides a wide and flat Fourier spectrum.

3.3.2 Proximity correction

PYRAMID previously described in chapter 2 is used for proximity correction. Doses necessary to each ring in the zone plate are given with calculation of deposited energy on each pixel and CDF table considering global and local exposure. General patterns are divided into several rectangles whose dimension is exactly same as times of pixel size. On the other hand, ring or polygon can not be divided in the same way. The dimension along x and y axis is exactly same as the times of pixel size, but the other region is not. Therefore, there might be different amount of deposited energy along ring due to different

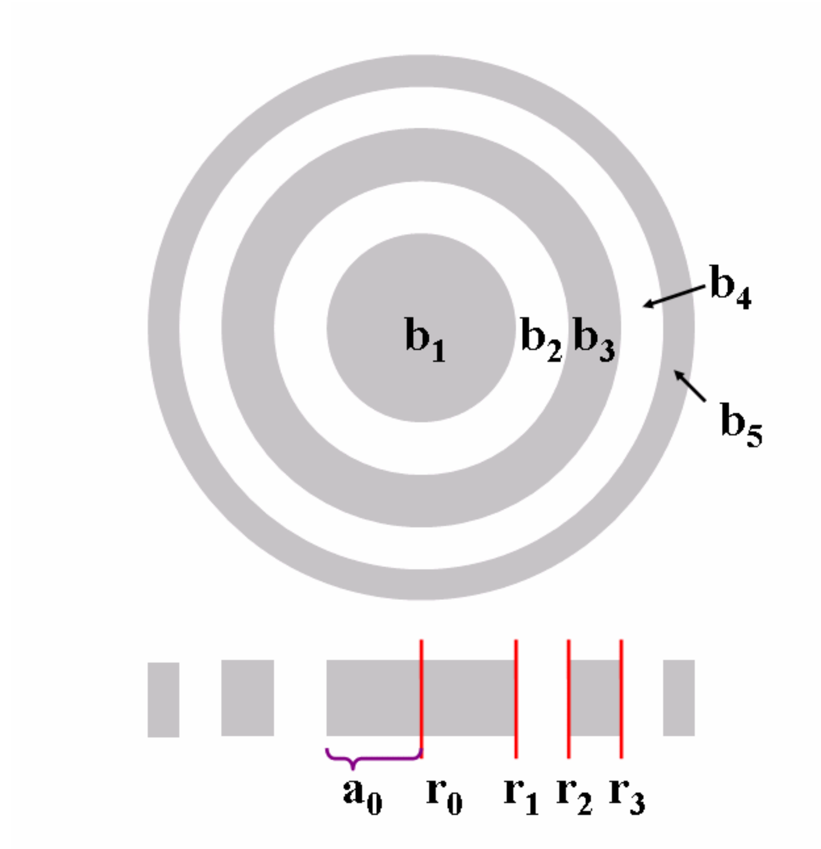


Figure 3.6: The construction of a Fresnel zone plate.

number of total pixels. The pixel points on the part of a zone are shown in figure 3.7. Deposited energy distribution for each ring is shown in figure 3.8. Exposure energy is dependent on base dose and exposure level changes as base dose changes while shape of energy distribution does not change. Dose factors computed by PYRAMID are applied to each ring to give same exposure level.

3.3.3 Exposure details

The machine JBX-6000FS has a minimum spot size of about 5nm with 100 *p*A at 50keV. All the works in this thesis were done at these beam conditions. To properly expose and fabricate small feature, beam size should be as small as it can. For the small feature lithographic biasing method is applied. Outer most ring width is set at smaller dimension compared to original pattern width. For example, pattern width is designed as 15nm to generate 20nm of zone width. Correspondingly, about 20nm width of zone will be formed from pattern broadening due to proximity effect after beam exposure. However, those methods need many trial and errors and also can not be applied on high proximity effect materials such as metals.

We do not change any dimension of zones because the dose factors calculated from the PYRAMID are assigned to each zone to minimize proximity effect. In the program, assigning dose amount to each zone is performed by MODULAT command. The Beam resident time on specific pixel called shot time and shot time during writing are described as following equations (3.2)(3.3).

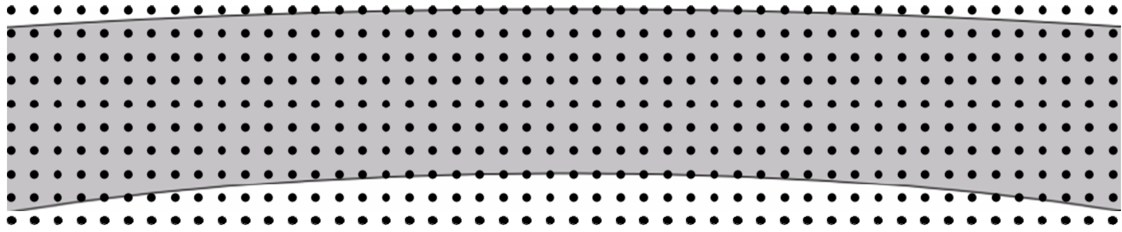


Figure 3.7: A part of the outer-most ring (shaded) is shown, where the ring width is 20nm and the pixel interval is 2.5nm. Those pixels in the shaded area, which are at the square grid points, are exposed.

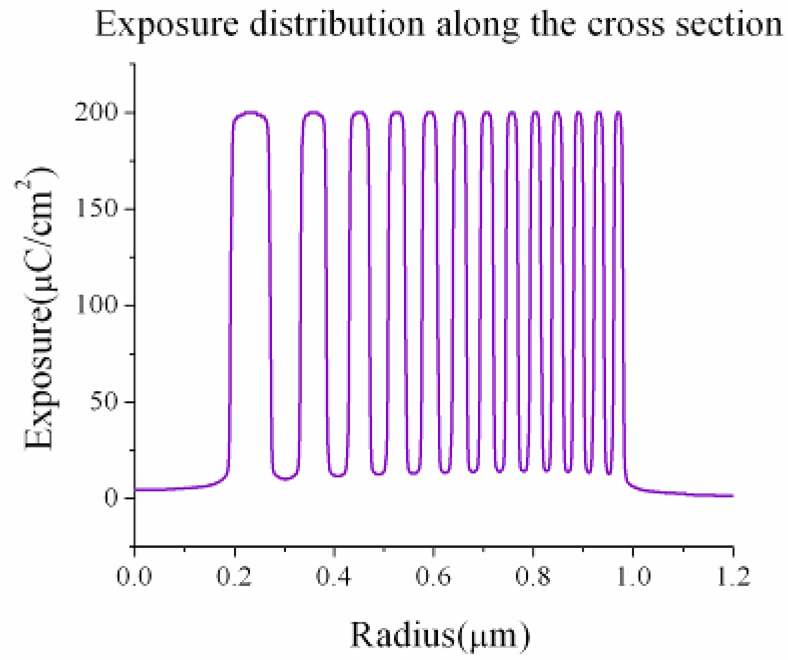


Figure 3.8: The exposure distribution of a cross-section; deposited energy variation from the center of the Fresnel zones toward the outside.

$$ShotTime(\mu \sec) = \frac{((Q(\mu C / cm^2) \times ScanStep(po\text{int})^2) \times Coefficient)}{BeamCurrent(pA)} \quad (3.2)$$

$$Shot\ time\ during\ writing = ShotTime \times \frac{(100 + V)}{(100)} \quad V : shot\ time\ modulation \quad (3.3)$$

In the program, shot modulation can be written as following

t : MODULAT: (r, V)   t: Name of the shot time modulation table

r: shot-rank number

V: shot time modulation

V values for each ring are given by PYRAMID and then the modulation of shot time calculated from above equations is applied to each pattern.

3.3.4 Fabrication on Polymethylmethacrylate (PMMA) resist

A Fresnel zone plate is fabricated on positive resist, PMMA resist. The layout of zone plate is designed in the same way of designing the grid pattern. It consists of 13 concentric rings, with an outer ring diameter of 2.0μm and a minimum line width of 20nm. The silicon wafers were spin coated with diluted PMMA solutions. Then, samples were baked at various temperatures for various times to see the effect of change of baking temperature and time on fabrication. The exposure was carried out with several base

doses on JBX-6000FS electron beam lithography.

Exposure is performed at 0.1nA and 50keV with the scan step of 2 which is 2.5nm (1 scan step is 1.25nm at mode 7).

After exposure the resist is then developed at various developing time and ratio of MIBK (methyl isobutyl keton): IPA (Isopropyl alcohol) and rinsed at IPA. After Au coating, patterns are inspected on SEM.

3.3.5 Fabrication on Hydrogen silsesquioxane (HSQ) resist

How to construct and design the layout of Fresnel zone plate are described in Sec. 3.4. Total number of rings in this experimental set is 15. Its outer ring diameter is 2.5 *u*m and outermost ring width is 18nm. HSQ is negative tone resist and beam exposure area is opposite to the case of PMMA. HSQ is diluted with MIBK and spun to get desirable thickness at various speed from 2000 to 5000*rpm* for 55seconds. HSQ has very low viscosity and film thickness is not affected that much by spinning rpm. Then, wafers are baked at several baking temperatures. Exposure procedure and conditions are same as PMMA. After exposure, the resist was then developed in the 0.26N tetramethyl ammonium hydroxide (TMAH) developer, TMAH and D.I.W mixed solution and D.I.W.

3.4. Result and discussion

3.4.1 Fabrication FZP on PMMA

3.4.1.1 Field size effect on fabrication

Mode 7 has field and subfield size of 80*80 and 5*5μm respectively. We change the

pattern position inside of a field and then investigate how it affects on fabrication as shown in figure 3.9. Beam is exposing on subfield in x direction and then y direction in the ring region. The beam and pixel size are 5nm and 2.5nm respectively in experimental condition. In figure 3.10, the beam trace is illustrated as electron beam is scanning horizontally. The beam is overlapping on the radius of 2.5nm and beam exposure starts again from the new subfield line when zone is present in cross point of subfield. In this case, there might be over exposure in two spots – new subfield line and end of a pattern. On the other hand, in case of zone plate being inside subfield, beam is overlapping at the end of pattern where there is over exposure. Therefore, first pattern design has more energy deposition in center area compared to second design due to the overlapping of beam exposure.

PMMA resist of 50nm is spun on Si and baked at 180℃ for 3minutes. After exposure, resist is developed at MIBK : IPA = 1:3 for 60seconds and IPA for 30seconds. Experimental results are shown in figure 3.11. The patterns which are positioned at a cross of 4 subfields are little bit more developed along the x and y axis as we expected. However, the difference of development corresponding to field position is not considerable.

3.4.1.2 Baking time and developing system

Soft baking has very important role on nano scale fabrication because it can vaporize left over solvent in the resist film after spinning and improves the adhesion of the resist by relieving film stresses that generated in spinning. [16] General baking temperature range

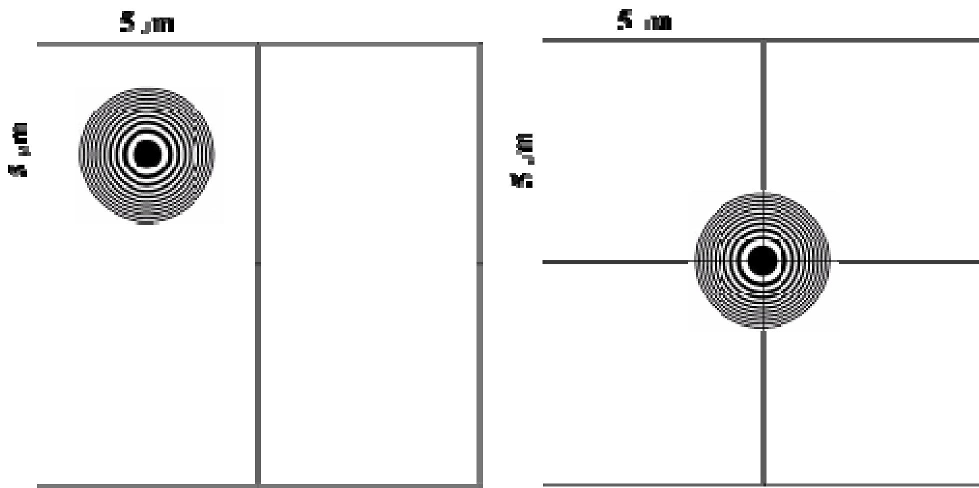
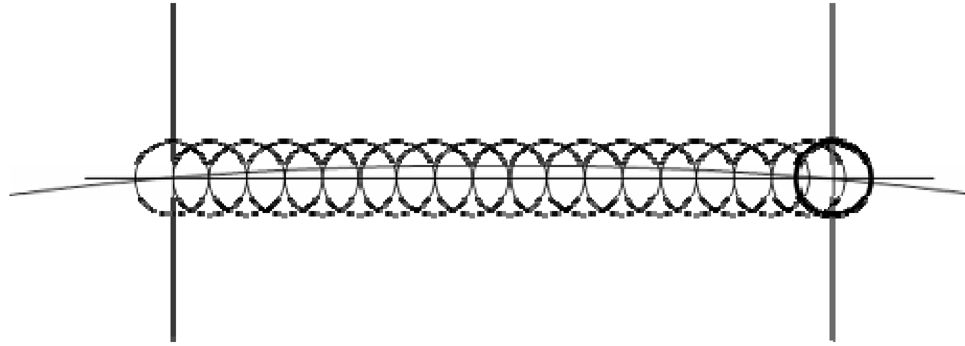
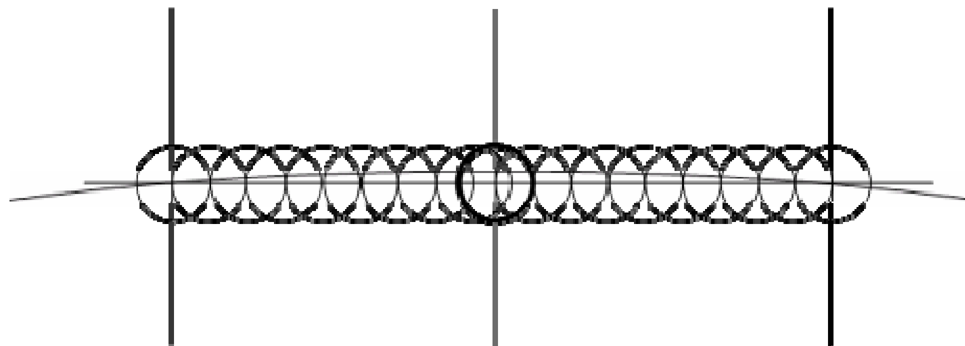


Figure 3.9: The position of a zone plate in the subfields. a) Zone plate is centered at a subfield, and b) present at a junction among subfields.

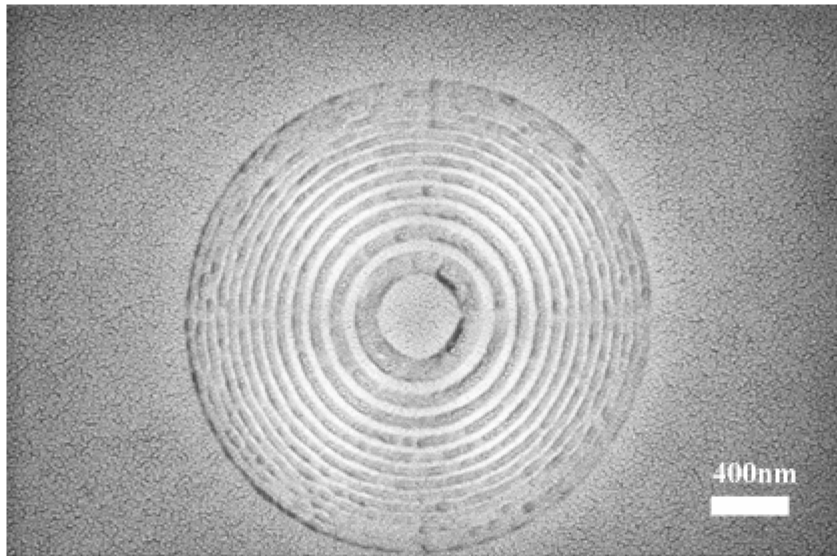


a)

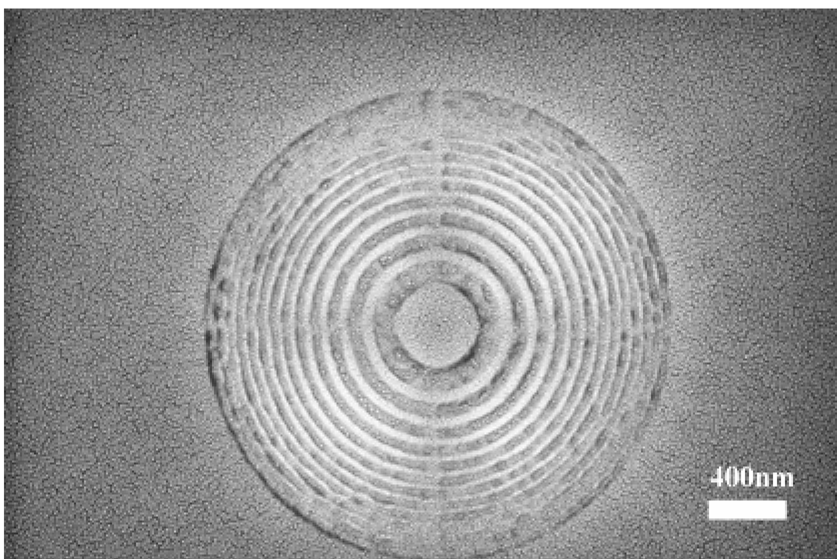


b)

Figure 3.10: The scanning trace of beam exposure according to the position of zone plate present in a) a subfield and b) at a junction of subfields.

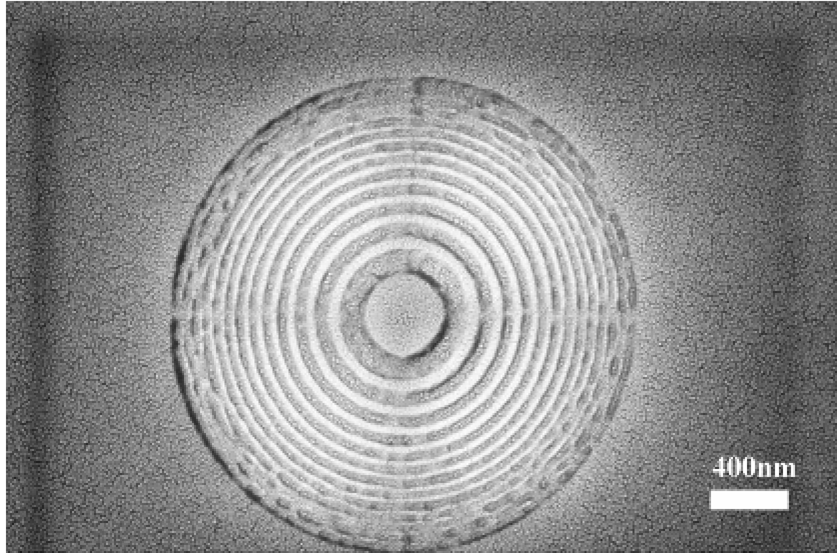


a)

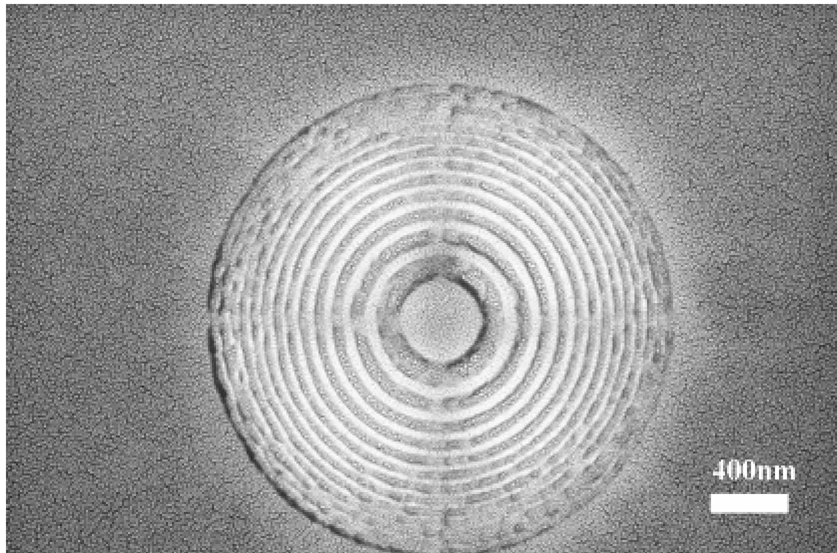


b)

Figure 3.11: Fresnel zone plate fabricated on PMMA; with a) base dose of 150μC/cm^2 and the pattern designed at a junction of subfields, b) base dose of 150μC/cm^2 and the pattern designed within a subfield.



c)



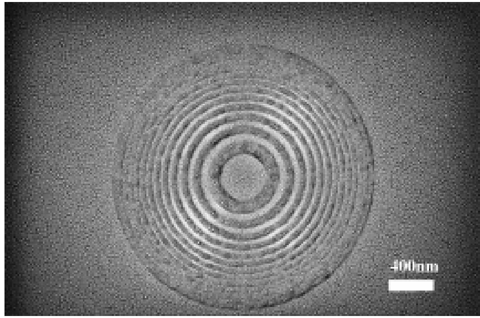
d)

Figure 3.11: Continued. and Fresnel zone plate fabricated on PMMA; with c) base dose of 160μC/cm^2 and the pattern designed at a junction of subfields, d) base dose of 160μC/cm^2 and the pattern designed within a subfield.

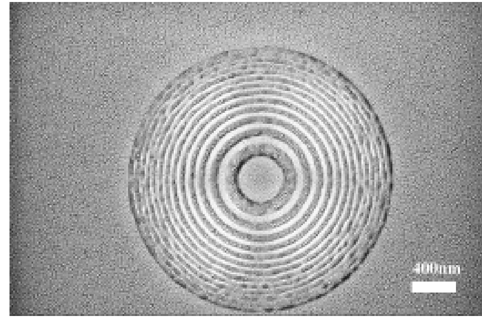
for PMMA is from 150 to 200℃ and baking at 180℃ is widely used. However, baking time is dependent on the concentration of original resist solution and spinning rpm. It is reported that solvent in PMMA/anisole is completely removed out of the resist film within 30 seconds during baking at over 140 ℃. [107] We tried two different baking time of 3min and 37min at 180℃ because the resist solvent was relatively thin (2.0 %*(v/v*)) and then developed at MIBK : IPA = 1:3 for 60seconds and IPA for 30seconds. As shown in figure 3.12, experimental results between two different baking times do not show any difference and as a result baking time of more than 3 minutes is acceptable for the soft baking.

With above results, experiments are performed with small base dose change of 2μC/cm^2. Fresnel zone plates are successfully fabricated and ring widths are almost same as designed as shown in figure 3.13, but it is seen that some of outer rings are not completely resolved which means there are developed and under developed regions along each ring. One of the reasons for this imperfect development of the outer rings is non-uniform deposited energy distribution along each ring.

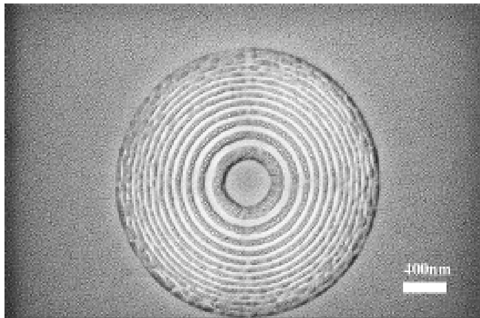
Proximity correction program (PYRAMID) assumed beam exposures are proceeding along the circle as shown in figure 3.14. However, the FPZ pattern was exposed in the Cartesian coordinate system, i.e., X-Y coordinate system (i.e., raster scan) as shown in figure 3.7. Therefore, the number of exposed pixels contributing energy deposition over the ring width varies along radial angle which leads to fluctuation of energy deposited along the ring. This deposited energy variation becomes relatively larger for a thinner ring.



a)



b)



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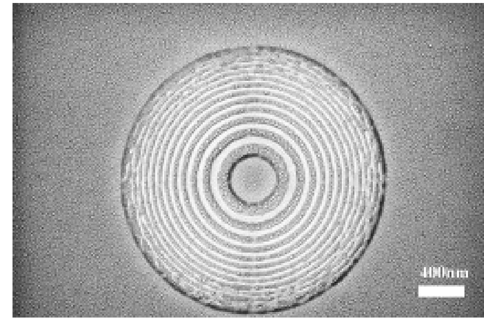

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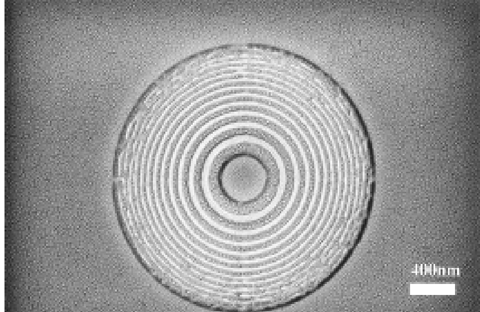
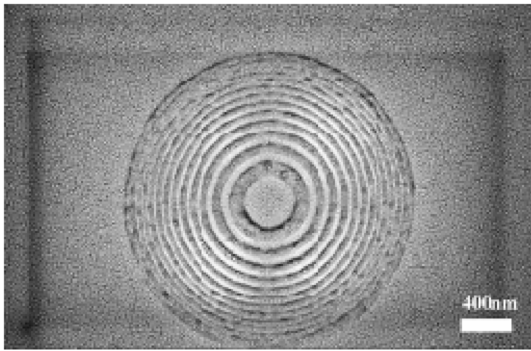
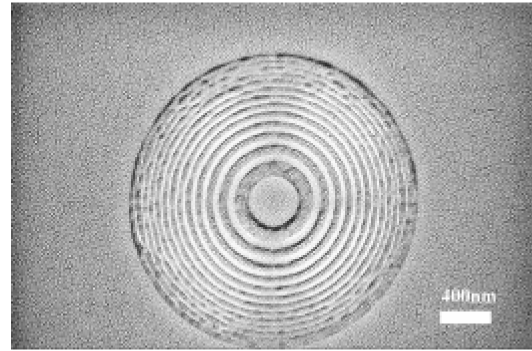


e)

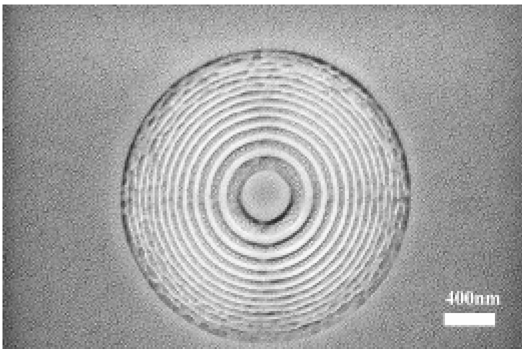
Figure 3.12: Fresnel zone plate fabricated on 50nm PMMA with baking time of 3 minutes at 180℃ ; a) 150μC/cm^2 b) 160μC/cm^2 c) 170μC/cm^2 d) 180μC/cm^2 e) 190μC/cm^2



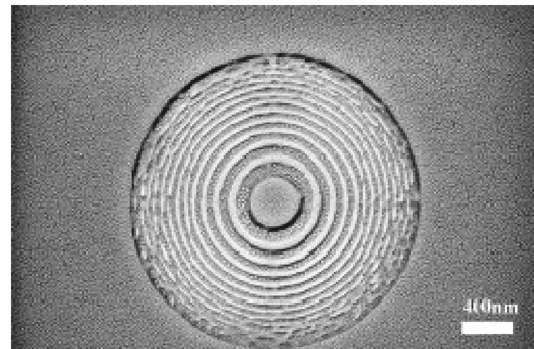
f)



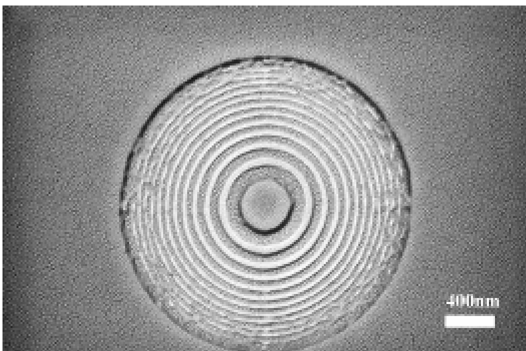
g)



h)

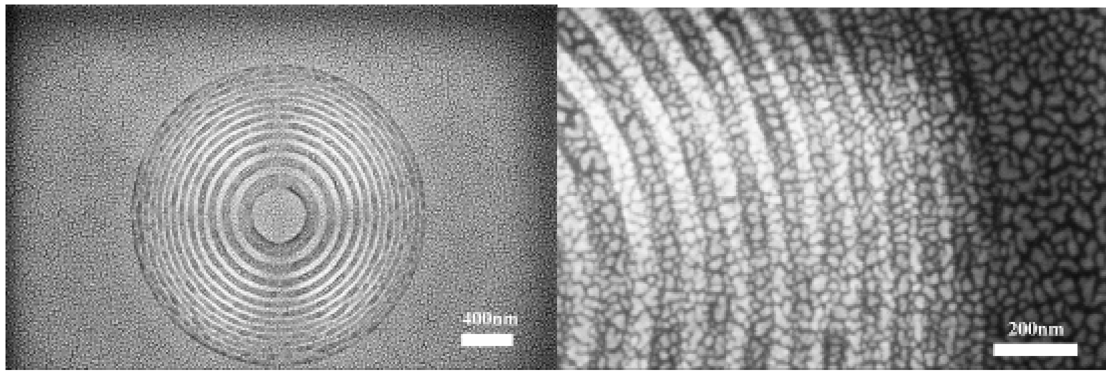


i)

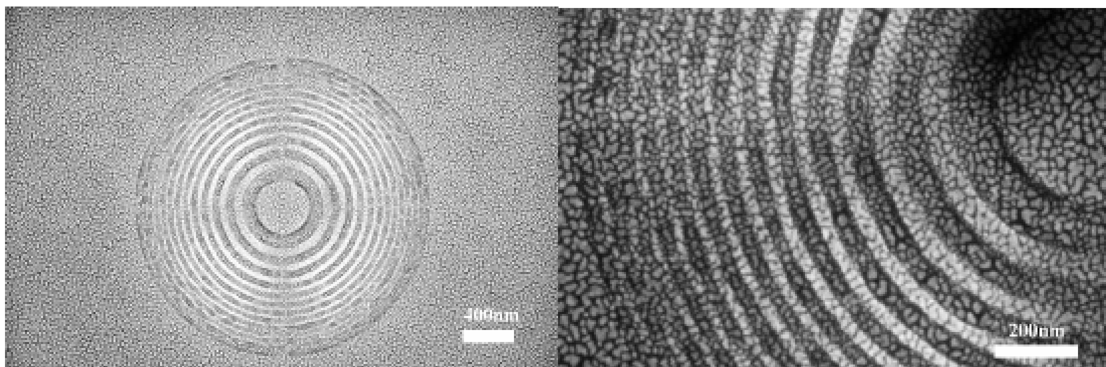


j)

Figure 3.12: Continued. and 37minutes at 180℃ ; f) 150μC/cm^2 g) 160μC/cm^2 h) 170μC/cm^2 i) 180μC/cm^2 j) 190μC/cm^2



a)



b)

Figure 3.13: Fresnel zone plate fabricated on PMMA a) with base dose of 160μC/cm^2, b) with base dose of 162μC/cm^2 and developing temperature of 20℃.

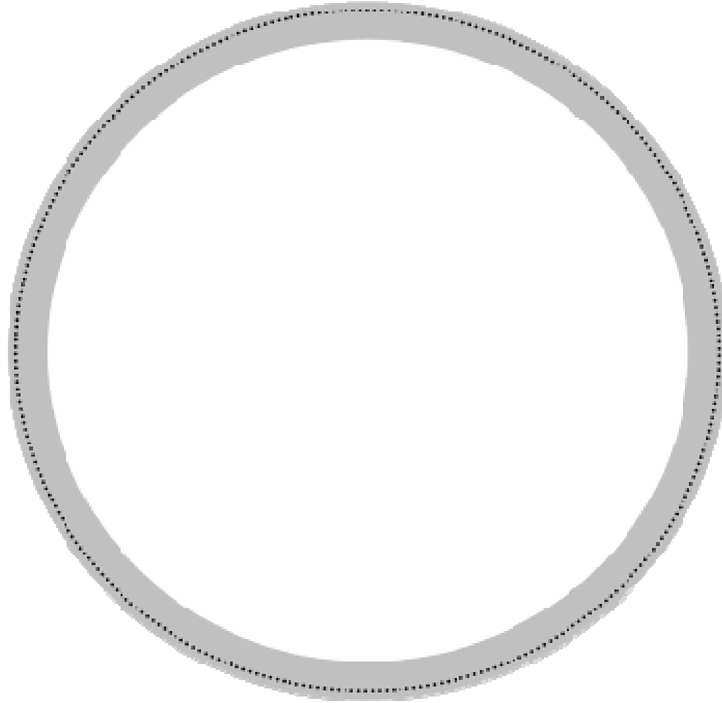


Figure 3.14: The schematic of beam exposure direction employed for PYRAMID program. Beam exposures are proceeding along the circle.

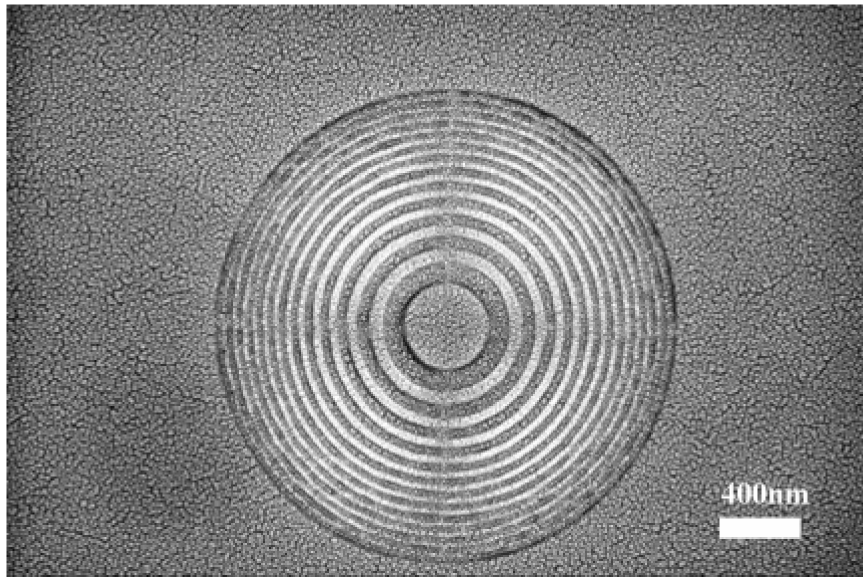
Another factor which can cause fluctuation of energy deposited is beam instability. Beam drifting or changing spot size during the e-beam exposure can result in dose variation contributing to deposited energy fluctuation. Also, in general, exposure contrast (deposited energy difference between the inside and outside a feature) tends to be lower for a smaller feature, which makes development more sensitive to the developing conditions (developing threshold).

It is reported that the resist contrast decreases as the strength of developer increases.[108] This indicates that a developer with higher concentration can lessen the effect of varying exposure along a ring on the developing process. As an effort to improve development of the outer rings, a higher-concentration developer (MIBK: IPA = 1:2) was employed in the subsequent experiments where base doses from 160 to 190 $\mu C/cm^2$ with the increase of $2\mu C/cm^2$, are exposed and then resist was developed at MIBK: IPA = 1:2 for 25 seconds and rinsed in Isopropyl alcohol for 45 seconds.

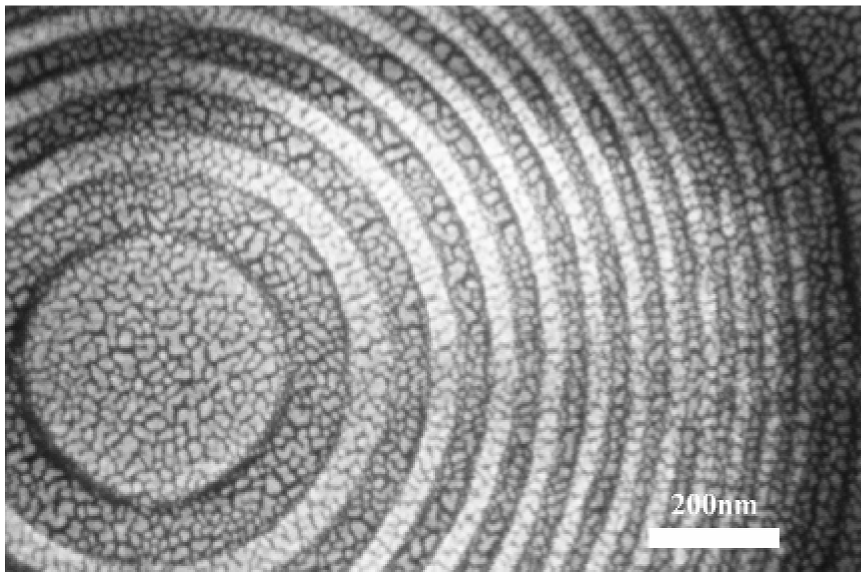
A Fresnel zone plate whose outermost ring size is 20nm was obtained with a base dose of $160 uC/cm^2$ and developed features are clearly resolved as shown in figure 3.15. The ring widths are briefly measured and it shows almost similar to designed values as illustrated in table 3.2.

3.4.2 Fabrication of FZP on HSQ

Hydro silsesquioxane (HSQ) resin is negative tone resist and several advantages such as high resolution with a moderate sensitivity, minimum line edge roughness, etch selectivity and stability of inspection under SEM have been reported.[109] Its chemical

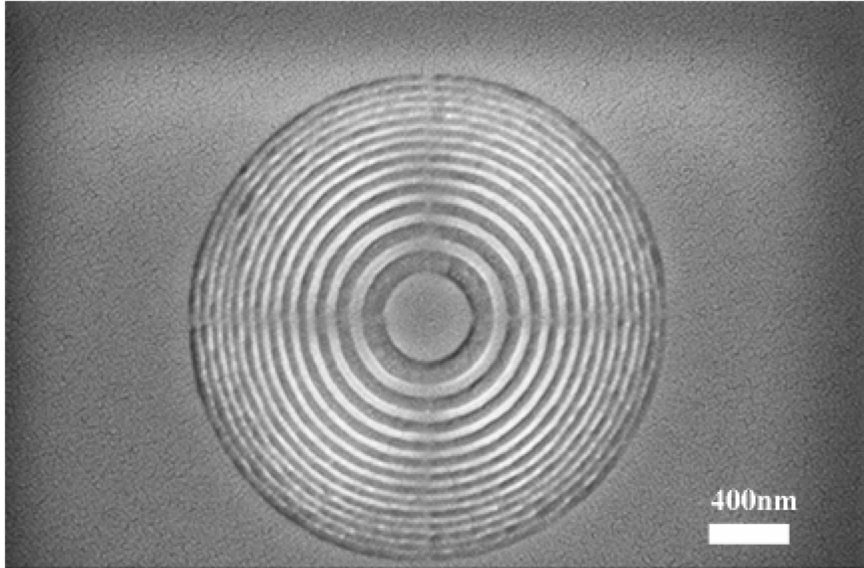


a)

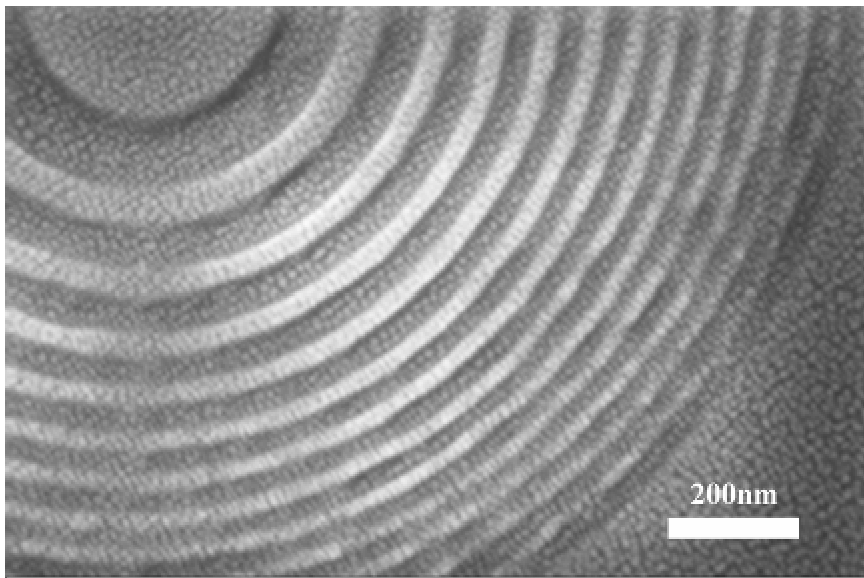


b)

Figure 3.15: Fresnel zone plate fabricated on HSQ with base dose of 160μC/cm^2 and developing temperature of 20℃ a) at the magnification of 32kX and b) 95kX,



c)



d)

Figure 3.15: Continued. and base dose of 154μC/cm^2 and developing temperature of 20.8℃ at the magnification of c) 32kX and d) 95kX.

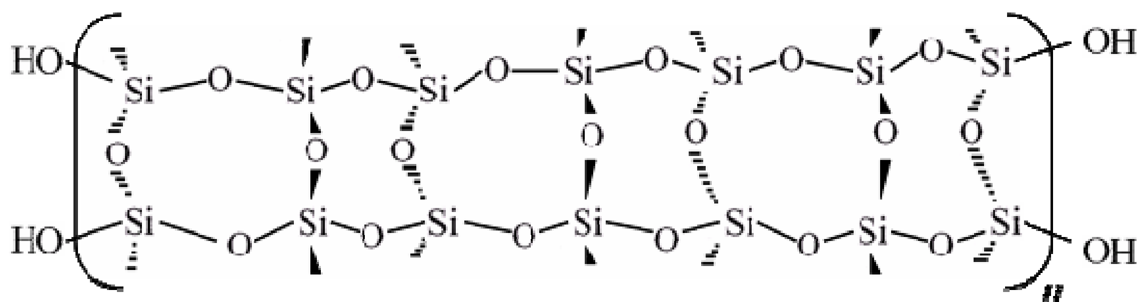
Table 3.2. The measured value of fabricated and designed ring widths of a zone plate

Ring number	Actual (nm)	Designed (nm)
1	400.0000	400.0000
2	80.4805	82.5000
3	60.0601	63.7500
4	52.8529	53.7500
5	44.4444	47.5000
6	40.8408	42.5000
7	37.2372	38.7500
8	33.6336	36.2500
9	33.6336	35.0000
10	30.0300	32.5000
11	30.0300	31.2500
12	27.6276	28.7500
13	26.4264	28.7500
14	25.2252	27.5000
15	25.2252	26.2500
16	25.2252	25.0000
17	22.8228	25.0000
18	22.8228	23.7500
19	22.8228	22.5000
20	22.8228	22.5000
21	21.6216	22.5000
22	21.6216	21.2500
23	21.6216	21.2500
24	21.6216	21.2500
25	20.4204	20.0000
26	20.4204	20.0000

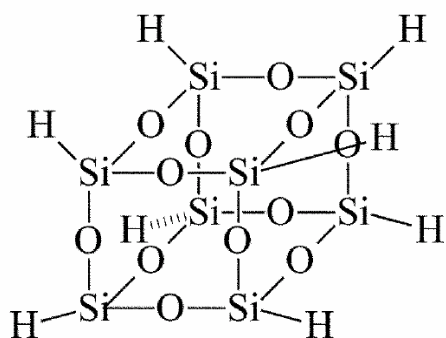
structures are assumed to consist of three types, ladder structure, cage structure and network structure as shown figure 3.16.[110] [111] During curing through baking, either a ladder structure or a cage structure transforms to a network structure. The transformation scheme for a ladder structure is assumed to be polymer crosslinking by condensation of Si-OH groups to Si-O-Si bonds. The other assumed scheme is that cage structures are opened and form network structure. As for thermal processing, electron beam exposure on HSQ also initiates a network formation. The presumable reaction mechanism is shown in figure 3.17. SiH bonds, which are weaker than SiO bonds, are broken by the e-beam. Siloxane bonds are formed from unstable Silanoles.[110]

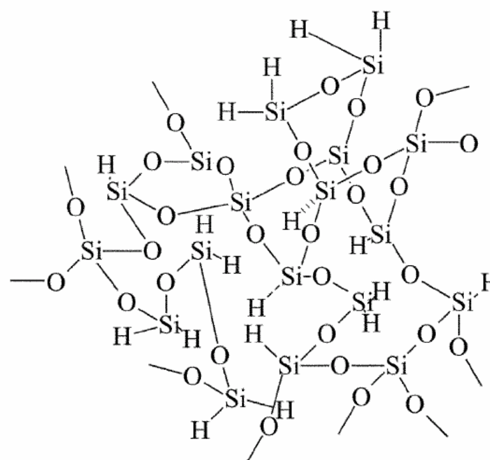
3.4.2.1 Resist behavior at two different baking and developing conditions as a function of base dose variation

We employed two generally used baking and developing systems for HSQ system. one is baking at 100, 200 and 300℃ for 1minute respectively and developing at 0.26N tetramethyl ammonium hydroxide(TMAH) for 70 seconds, TMAH : D.I.W = 1:10 for 60 seconds and D.I.W for 60 seconds. The other is baking at 120 and 200℃ for 2minutes, respectively and developing at TMAH for 70seconds, TMAH : D.I.W = 1:9 for 10seconds and D.I.W 10seconds. We changed base doses from 200 to 900$\mu C/cm^2$ applying dose factor of 1.24 to investigate how resist thickness varied as base dose changes. Rectangle whose size is 1*15µm is applied as a test pattern and HSQ of about 100nm is spinning on Si wafer. Baking and developing system above mentioned were



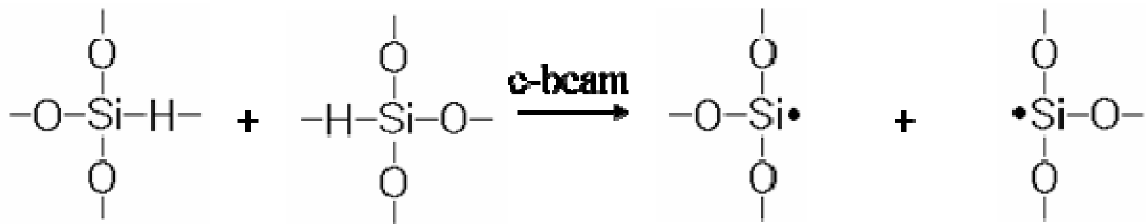
a)



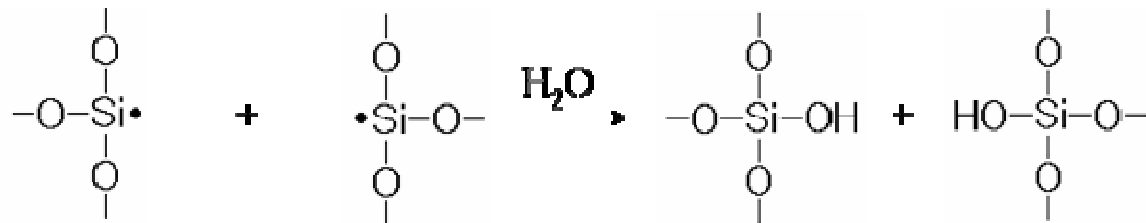


b) c)

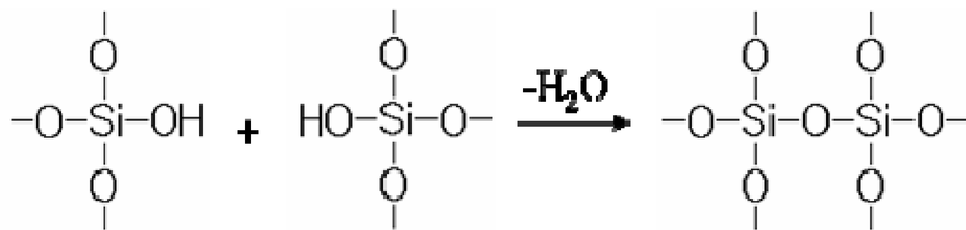
Figure 3.16: The chemical structure of HSQ resist: a) ladder structure, b) cage structure, and c) network structure.



a)



b)



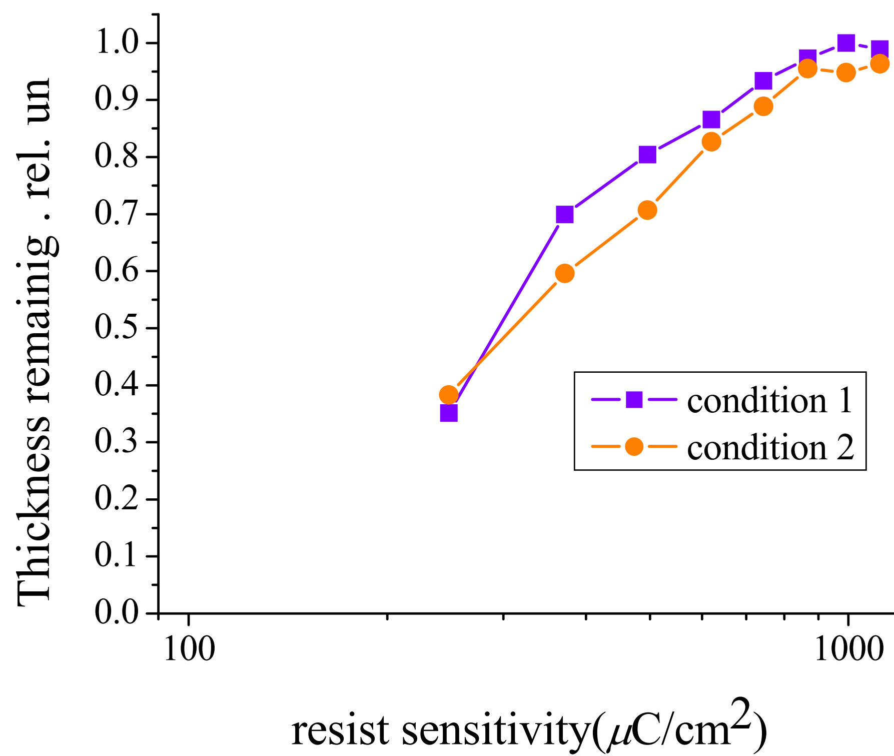
c)

Figure 3.17: Presumable reaction mechanism of HSQ: a) SiH bonds, which are weaker than SiO bonds are broken by e-beam, b) Silanoles are formed by a reaction to moisture and c) Siloxne bonds are formed by cross linking.

applied before and after exposure. Remaining resist thickness was measured by the Asylum MFP-3D AFM (Atomic Force Microscope).

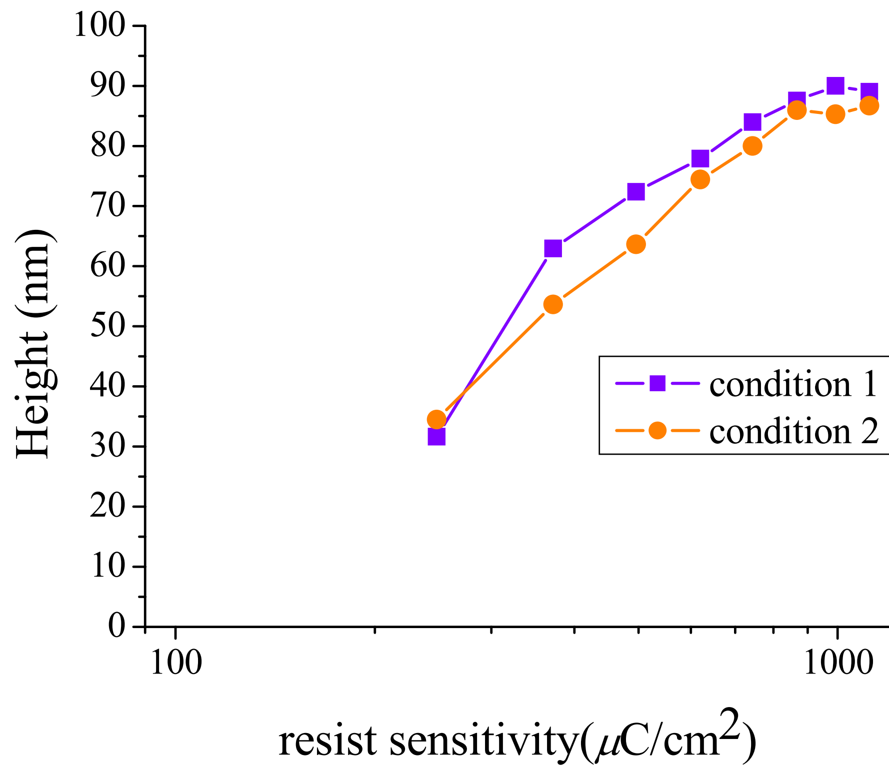
A contrast curves are obtained after development as shown in figure 3.18. The condition 1 is the baking at 100, 200 and 300℃ for 1minute respectively and developing at TMAH for 70seconds, TMAH : D.I.W = 1: 10 for 60seconds and D.I.W for 60seconds and condition 2 is the other one. The slight loss in resist thickness was observed at higher dose range and condition 1 whose baking temperature is higher needs lower base dose to achieve the same height as condition 2. Around base doses between 280 and 380μC/cm^2, condition 1 shows extremely higher sensitivity compared to condition 2 while two conditions have almost similar sensitivities at other base dose range.

When it comes to the contrast, we do not have onset doses for both conditions because it is impossible to find and measure the height of pattern less than 20nm on AFM, and thus contrast value can not be calculated. As already mentioned in section 3.3, during thermal processing a bond scission and recombination occur simultaneously reducing cage or ladder/network ratio due to the transition of a cage or ladder to a network structure and at the end of thermal treatment, a number of free Si bonds, dangling bonds, also exist due to incomplete recombination of broken Si-O and Si-H bonds which result in chemical instability of the film. During the electron beam exposure, similar processes also take place with higher energy deposition than thermal treatment and then the higher of bond scission and network formation. These stable three dimensional network structures have a low dissolution rate in developing solution. Therefore, we can conclude that thermal treatment is kind of pre-exposure of HSQ and resist at higher baking temperature need



a)

Figure 3.18: Contrast curves obtained from the exposure on HSQ. a) Thickness remaining in relative unit as a function of base dose,



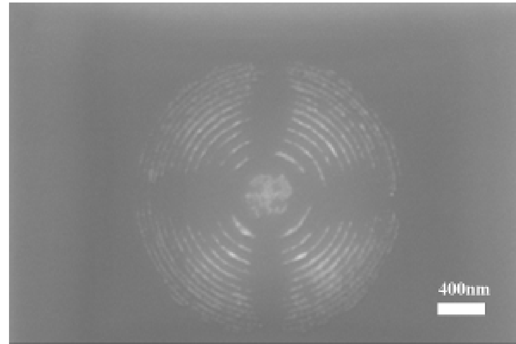
b)

Figure 3.18: Continued. and b) actual height change.

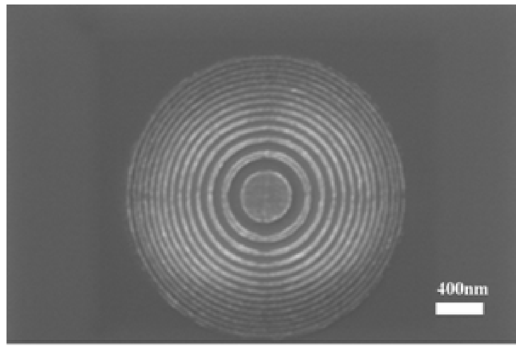
lower exposure dose to have same remaining resist thickness and short time to expose same pattern area while higher baking may cause problems to remove the unexposed area which result in poor development contrast due to readily transformation of the unexposed area to a network structure. From above experimental results, we can estimate optimum dose range for the fabrication of zone plates even if resist thickness and size of patterns are different.

3.4.2.2 Fabrication of FZP on HSQ

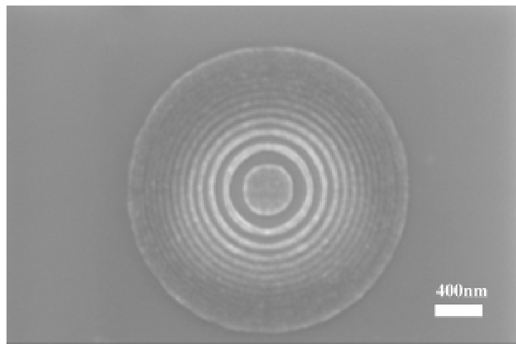
With the information obtained from previous section (section 3.4.2.1), the fabrication of zone plates on ~ 50nm of HSQ and silicon substrate were performed. Dose factors computed by PYRAMID were applied to each ring to remain after developing. Fabricated zone plates treated with developing system mentioned previously after exposure are shown in figure 3.19 and 3.20. As discussed earlier, zone plates with condition 1 is start being fabricated in lower base dose range than those from condition 2. Especially, two zone plates fabricated in relatively lower base dose range shows big difference of fabrication shapes and this results from extremely different sensitivities between two conditions in those base dose range. From the figure 3.19 and 3.20, it is seen that the fabricated Fresnel zone plates are not as perfect as those on PMMA. However, it should be noted that the exact diameter or perfect shape of rings are not important, unless the object is to be used as an optical lens, rather it is the symmetry and the harmonic relationship between the ring radii that provides the desirable spatial power spectrum for analysis. The resulting zone plate structure provides a useful level of imaging contrast when observed in secondary electron mode in a SEM as shown in figure 3.19 and 3.20 and the symmetrical structures makes it easy to focus and stigmate the microscope so as to achieve optimum imaging performance.



a)

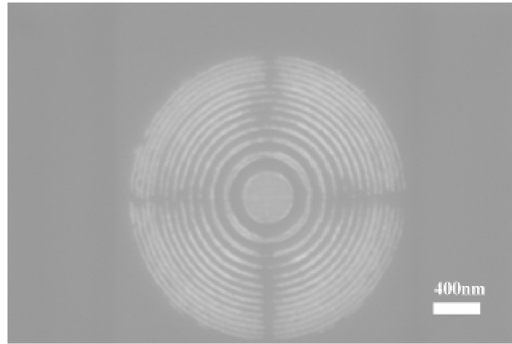


b)

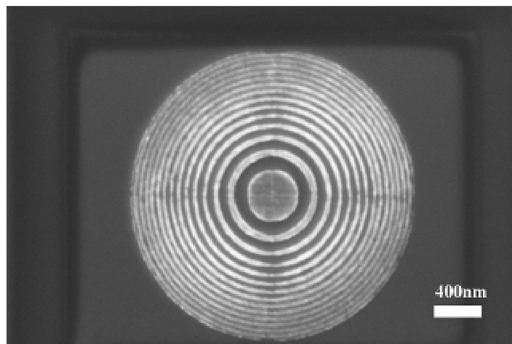


c)

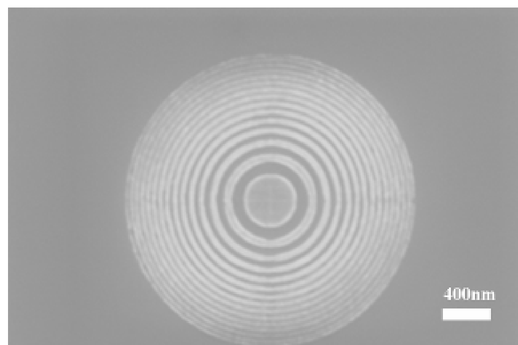
Figure 3.19: Fresnel zone plates fabricated on HSQ with the condition of baking at 100, 200 and 300℃ for 1minute respectively and developing at TMAH for 70seconds, TMAH : D.I.W = 1: 9 for 10seconds and D.I.W for 10seconds with the base dose of a) 300 , b) 400 and C) 500μC/cm^2 .



a)



b)



c)

Figure 3.20: Fresnel zone plates fabricated with the condition of baking at 120 and 200℃ for 2minutes, respectively and developing at TMAH for 70seconds, MF322 : D.I.W = 1:9 for 10seconds and D.I.W 10seconds with the base dose of a) 400 ,b) 500 and C) 580μC/cm^2 .

CHAPTER 4

CONTROLLING RESIST THICKNESS AND ETCH DEPTH FOR FABRICATION OF 3-D STRUCTURES

4.1 Background

There are many applications, including optical devices, where multi-level or 3-D structures are required. Performance characteristics of such devices are highly sensitive to dimensional accuracy of the structures.[4] Therefore, it is essential to achieve high dimensional fidelity in the fabrication process. A desired structure may be transferred onto the substrate by electron-beam (E-beam) lithographic and etching processes. One possible approach is to use the *binary* lithographic process multiple times, i.e., once for each depth. However, this approach has a few drawbacks, especially when the number of different depths is greater than two: a longer total process time, the alignment problem between processes, a higher probability for a lower yield due to the complicated process, and a higher cost. Also, a gradually varying 3-D surface cannot be handled by this approach. *Grayscale* lithography can eliminate these drawbacks since it requires only one step of E-beam lithographic process. A 3-D structure is first transferred onto the resist in one lithographic step such that the remaining resist profile resembles the structure. Then, the substrate is etched through the remaining resist to complete the pattern (structure) transfer.

The feature size was large, mostly $O(10) \sim O(100)$μm where $O(\,)$ denotes *in the order of.* Also, the depth resolution was $O(10)$μm.

The main focus of this study was on controlling thickness of the remaining resist after development in E-beam lithographic process and etch depth in the subsequent etching process for the feature size of $O(1)$μm or less and the depth resolution of $O(10)$nm.

In this thesis, the procedures to determine doses to be given to each feature and to achieve the desired etch depths of multiple features in a 3-D structure are described.

4.2 Experiment

4.2.1 Dose determination

A *mapping function* may be employed to model the fabrication process using grayscale E-beam lithography. Let f denotes the function. The function f relates exposure to resist development depth, i.e., $R = f(E)$ where E is the exposure and $R = T_0 - T$ where T_0 and T are the initial and remaining thicknesses of resist, respectively. Note that f is an increasing function which may be estimated through experiments and calibrations. In Figure 4.1, a 3-D structure of staircase which is employed to investigate feature depth.

In order to determine dose to be given to each feature or each step, the exposure level required for the feature is to be estimated first. The main focus of this study is on depth control, not critical dimension - CD (feature width and length) - control. Therefore, dose control within each feature by partitioning it into regions is not considered. Thickness control of the remaining resist is achieved by determining a proper level of energy deposited (*exposure*) for each feature (thickness). Given an exposure distribution to be achieved for a certain 3-D structure, the grayscale proximity effect correction scheme developed earlier [4] is employed to compute the energy to be given (*dose*) to each feature.

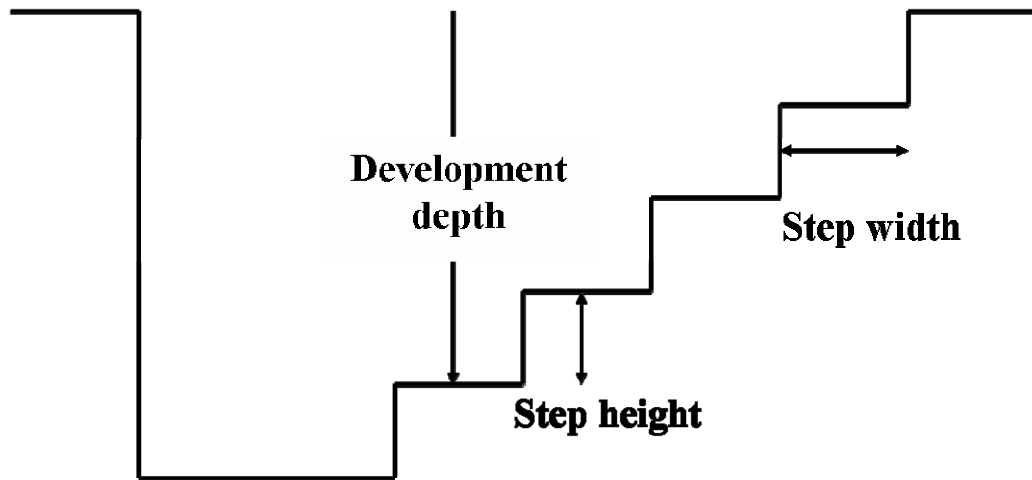


Figure 4.1: A staircase structure consisting of 6 steps: when it is transferred onto resist, the development depth refers to the initial thickness of resist minus the remaining thickness of resist.

A set of experiments is performed with the theoretically calculated dose factors by the grayscale proximity effect correction program PYRAMID [4] to get *f(E)* and then obtained results are used to derive the relationship between the development depth and exposure. After then, dose for each step in the staircase structure is computed again.

4.2.2 Fabrication of staircase structure

The staircase patterns which consist of 6 rectangles are first designed in the form of J01 and then converted to J51 by the previously described procedure. We tried to generate three different size of stair case structures whose dimensions set are 1*15μm, 0.5*15μm and 0.2* 15μm, respectively. The silicon wafers were spin-coated with the PMMA 495/11A diluted with anisole solution at various speed from 3000 to 4000*rpm* for 55seconds, to obtain the various resist thickness. Then, the samples were baked at 180°C for 3 minutes. The staircase patterns were exposed using a JEOL 6000 FS/E direct-write electron beam lithography tool, which is operated at 50keV and 0.1nA. Step number is set as 4 because PYRAMID program apply the pixel size of 5nm. The tool also requires a base dose of 300μC/ cm^2 which is applied to each rectangle with different dose factors calculated by PYRAMID. After exposure, the resist was developed in the MIBK (methylisobutyl ketone) : IPA (isopropyl alcohol) = 1:3 developing system for 60seconds and IPA for 30seconds. Developed patterns are measured by the Asylum MFP-3D AFM (Atomic Force Microscope).

4.2.3 Transfer of pattern using RIE (Reactive Ion etching)

Reactive Ion Etching (RIE) is an important process in the production of semiconductor devices and integrated circuits. This is due to the continuous need to process devices with extremely small line widths and feature geometries**.** The mechanisms involved in RIE are complex which employs the chemical and physical nature of plasma.[112] Plasma is created by applying electric field of certain magnitude between two electrodes to a gas. Any electrons from cathode are accelerated and collide inelastically with a neutral gas to transfer its energy to the gas. Gases received energy from the electrons are excited to higher energy level and then returned to ground state emitting photons or release secondary electrons which might react with another gas. As a result of electron-gas reaction, ions, electrons and free radicals are formed and play an important role in reactive ion etching.

Typical reactive ion etching process is mainly controlled by three process factors, i.e., RF power, gas pressure, and gas composition. Optimization of the three factors usually requires a large number of experiments and error analysis. In order to reduce the number of experiments, one may make use of the *Taguchi design of experiment* (DOE) to determine dependency of etching process on the three factors first and then guide subsequent experiments according to the dependency.[113]

The staircase structure was transferred onto the silicon substrate by etching, using Trion Technology Oracle RIE tool, through the remaining resist, of which profile resembles the structure. That is, the remaining resist was used as a grayscale etch mask which is also etched. The thickness of remaining resist of a feature (step) determines the time the silicon substrate area corresponding to the feature starts to be etched and the depth of the

etched feature depends on the ratio of resist and silicon etching rates.

Initial experiments were designed according to the DOE which consisted of three levels for the three process factors. We used two types of active gas systems which can generate fluorine atom and is normally used for silicon etching. First system is O_2 and SF_6 gases where the SF_6 flow rate was 45*sccm* with the O_2 flow rate varied. The other system is composed of various O_2 flow rate and fixed CF_4 flow rate of 40*sccm*.

Etched patterns are also measured by the Asylum MFP-3D AFM.

4.3 Result and discussion

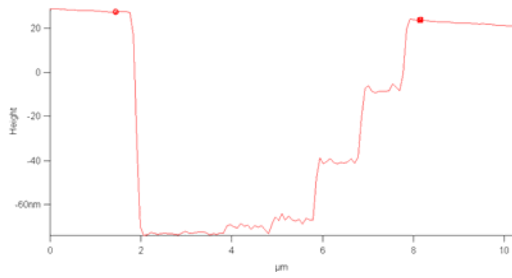
4.3.1 Fabrication of stair case structures

Pre experiments are performed to give initial relationship between generated step heights and dose factors theoretically calculated by PYRAMID. Dose factors and corresponding depth of patterns are shown in table 4.1. Experiments are set to make the height of each stair increase 20 nm from the two bottom layers in the 100±2nm of PMMA and carried out with 1μm width patterns. Developing temperature was 19℃. Experimental results profiled on AFM are shown in figure 4.2 and the curve for the relationship between the development depth and exposure was built up with obtained results is illustrated in figure 4.3. A curve may be fitted to these sample points in the graph such that a certain measure of error such as the mean square error is minimized and the exposure values in the graph means deposited energy, not provide of actual exposure. This curve is referred to when determining the exposure level for a given development depth.

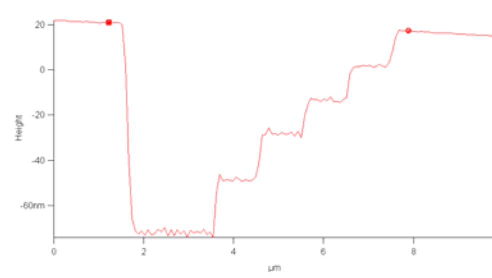
Table 4.1. Dose factors and corresponding depth of stair case structures fabricated on ~100nm PMMA with modified pattern layout.

a)		b)		c)	
Dose factors	Depth(nm)	Dose factors	Depth(nm)	Dose factors	Depth(nm)
1.350	100.34	1.220	93.82	1.250	99.80
1.340	99.87	1.220	93.35	1.250	98.40
1.120	96.94	0.990	69.08	1.060	91.10
1.020	92.04	0.890	50.57	0.930	59.50
0.900	64.62	0.780	35.14	0.810	37.90
0.710	33.29	0.620	19.08	0.650	20.63

d)	
Dose factors	Depth(nm)
1.250	99.63
1.250	99.15
1.030	78.36
0.930	54.66
0.830	38.79
0.650	19.35



a)



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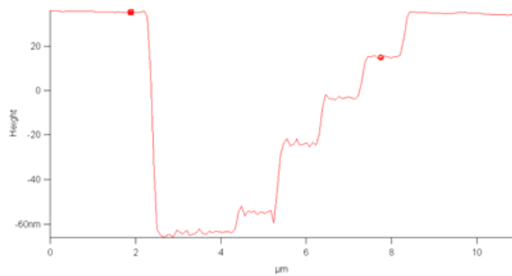

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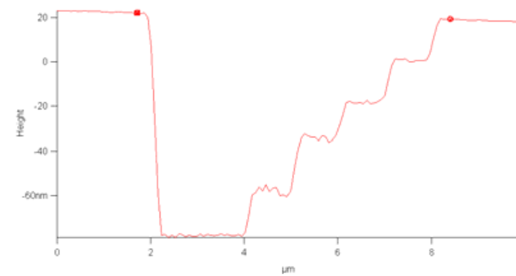


d)

Figure 4.2 The depth profile measured on AFM. Each picture shows the developed structure and is corresponding to the condition and numbering on table 3. Measuring of depth is performed on 3 different points of each stair and values are averaged.

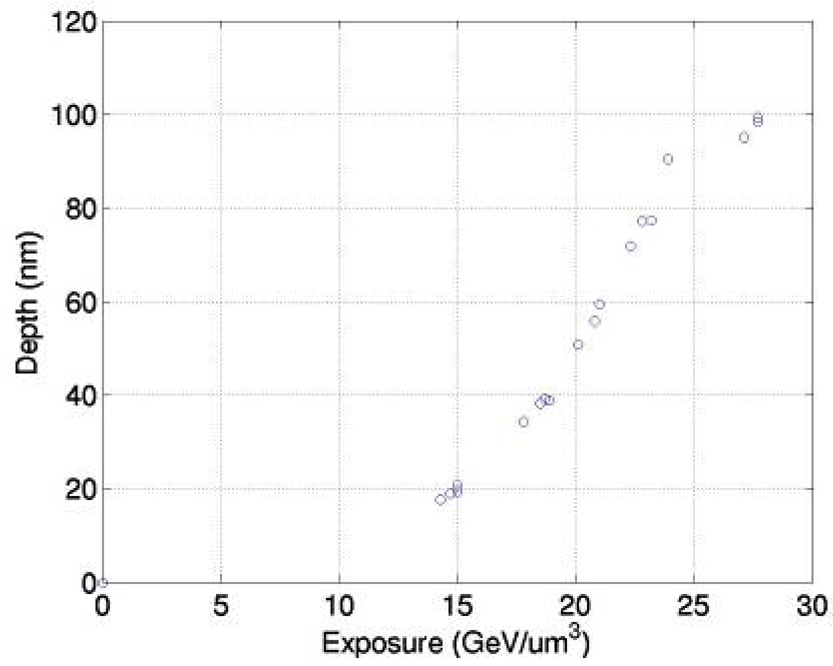


Figure 4.3: Relationship between exposure and development depth for the staircase structure (step width of 1.0μm) transferred onto 100nm PMMA on *Si* with the beam energy of 50keV.

Then, dose for each step in the staircase structure is computed by the grayscale proximity effect correction program PYRAMID. Dose factors based on the relationship curve was generated as illustrated in table 4.2 and applied to fabricate designed staircase structures on PMMA of 100 nm.

After exposure and development, designed stair case structure was successfully fabricated with dose factors computed by PYRAMID as shown in figure 4.4. It is seen that the five steps of the staircase structures are well separated in the resist profile and the step heights are uniform. Dose factors and development depth are shown in table 4.2 and the value of depth is an averaged measure since each step is not completely flat. The average percentage error (difference) between the ideal and actual depths of steps in the remaining resist profile is no greater than 2.5% in staircase structures.

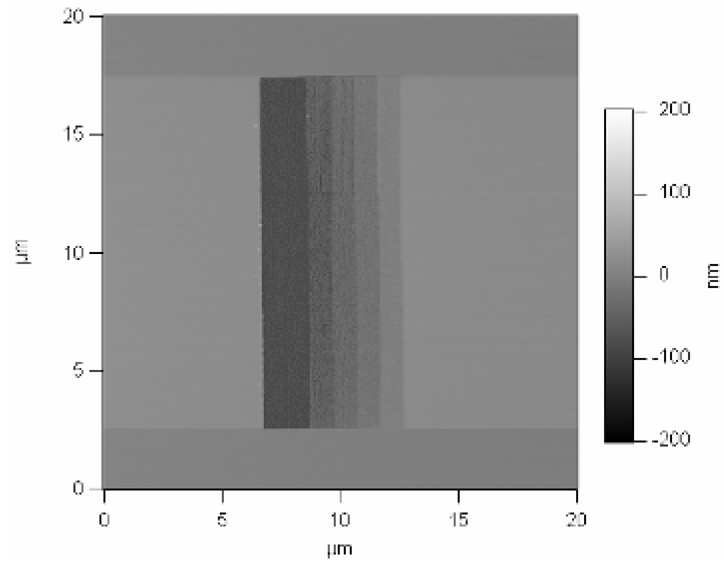
With successful transfer of designed stair case structure into 100nm PMMA, we tried to transfer smaller width of structures which is 0.5 and 0.2μm into same thickness of PMMA. After several pre experiments, we found that it is difficult to scan the staircase of 0.2μm step widths on AFM due to AFM tip size limitation and so we only performed the experiments for 0.5μm line width structures.

Ideally the relationship curve between exposure and development depth for 1.0μm and 0.5μm structure should be same because features are large enough so that the proximity effect on step edges is ignored. Therefore, we referred to relationship curve shown in figure 4.3.

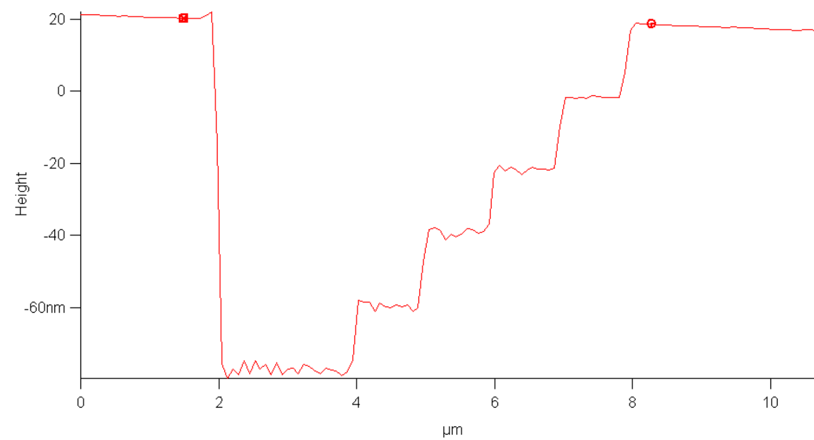
With the dose factors obtained from relationship curve shown in table 4.3, we succeeded to fabricate staircase structure whose step width is 0.5μm and height is ~20nm in figure 4.5. The average percentage error (difference) between the ideal and actual depths of steps in the profile is no greater than 2.5% in staircase structures.

Table 4.2. Dose factors based on the relation ship curve between exposure and development depth and corresponding values of development depth.

Dose factors	Depth(nm)
1.250	97.30
1.250	98.10
1.034	80.70
0.945	59.72
0.835	41.13
0.650	20.53

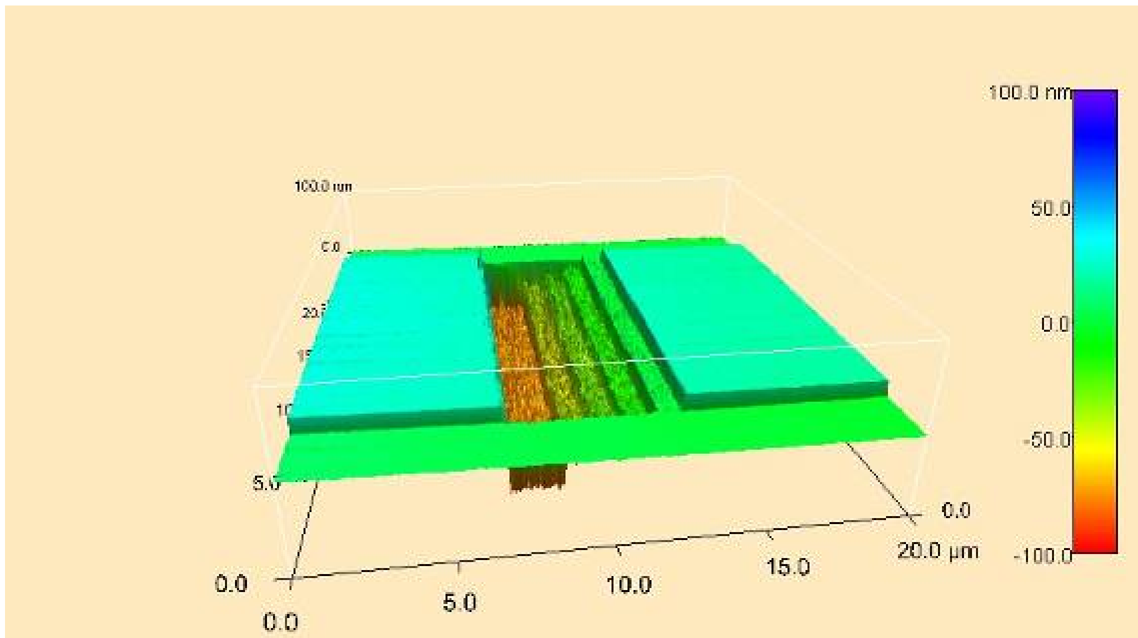


a)



b)

Figure 4.4: The remaining resist profiles, after development, of the staircase structures transferred onto PMMA on *Si* a) top view, b) cross-section: the left-most step is 2µm wide.

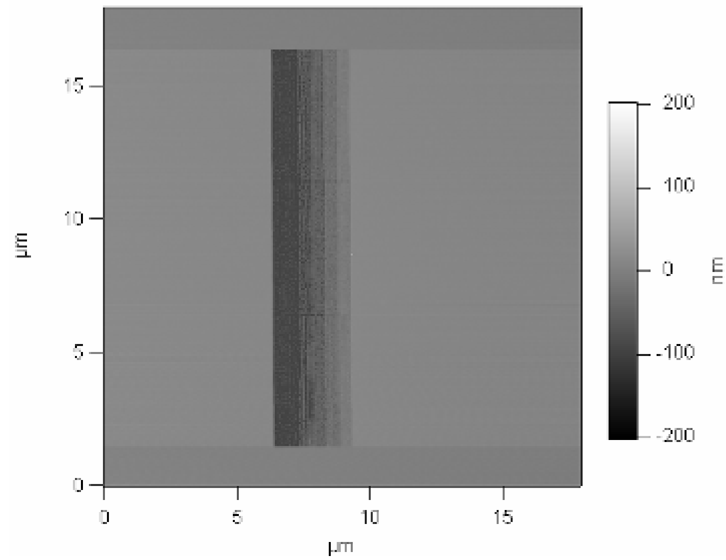


c)

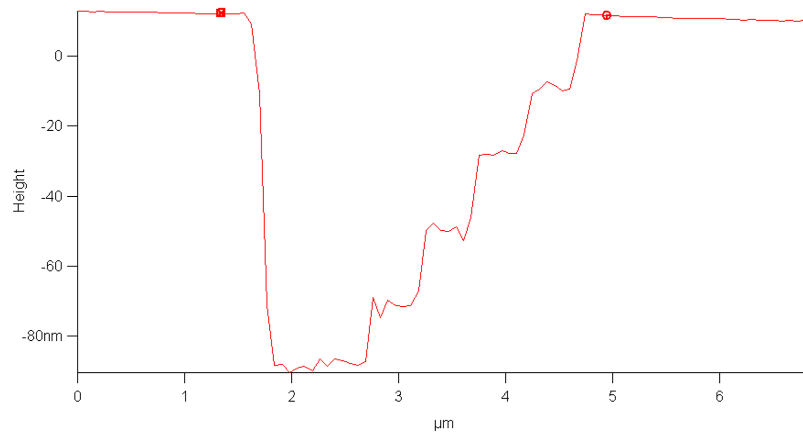
Figure 4.4: Continued. and (c) 3-D image. The step height is about 20nm.

Table 4.3. Dose factors based on the relation ship curve between exposure and development depth and corresponding values of development depth.

Dose factors	Depth(nm)
1.230	100.9
1.230	99.8
1.110	81.2
1.020	61.1
0.890	40.4
0.720	20.7



a)



b)

Figure 4.5: The remaining resist profiles, after development, of the staircase structures transferred onto PMMA on *Si* when the step width is 0.5µm. a) top view and b) cross-section: the left-most step is 1.0µm wide. The step height is 20nm.

4.3.2 Transfer of staircase structures in resist onto Si through RIE (reactive ion etching)

As mentioned previously, we applied Taguchi design of experiment (DOE) to minimize number of experiments and have information regarding to tendency of etching according to variation of three factors, i.e., RF power, gas pressure, and gas composition. First we introduced CF_4-O_2 gas system as etchant gases where the CF_4 flow rate was 50*sccm* with the O_2 flow rate varied. Effects of the three process factors on the etching rates of silicon and PMMA and their ratio are provided in Table 4.4. Tendency of responses for each factor is illustrated in figure 4.6. Both the PMMA and silicon etching rate show a strong dependency on RF power and oxygen flow rate.

As oxygen flow rate increases, PMMA etching rate increases and silicon etching rate has turning point on the graph due to oxidization of silicon surface. And also, PMMA and silicon etching rate increase as RF power increases. We can see silicon etching rate seems to saturate at high RF power.

In figure 4.7, potential distribution in a glow discharge process using RF power. Self biased voltage V_B in the established sheath voltage is given by following equation (4.1).

$$V_B = \frac{\left(A_P \sigma_e P_{RF}\right)^{1/2}}{A_S \omega \varepsilon_0 l_p^{1/2}} l_s \qquad (4.1)$$

where A_p and A_s are the cross-sectional areas for the plasma region and the sheath region, σ_e and R_{RF} are the conductivities of electrons and the applied RF power, ω and ε_0 are

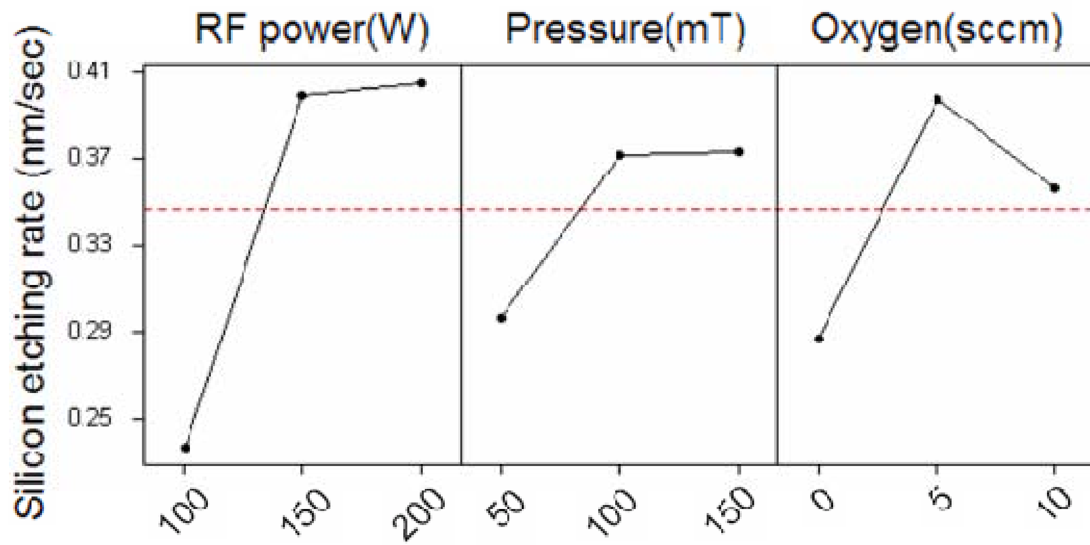
Table 4.4. Taguchi DOE for optimizing RIE process in CF_4-O_2 system.

No.	Factors			Responses		
	RF power, *W*	Pressure, *mtorr*	O_2, *sccm*	Si E/R [a], *nm/sec*	PR E/R [b], *nm/sec*	Rt Si/PR [c]
1	100	50	0	0.20	0.47	0.42
2	100	100	5	0.27	0.92	0.29
3	100	150	10	0.24	0.91	0.27
4	150	50	5	0.37	1.71	0.25
5	150	100	10	0.50	2.04	0.30
6	150	150	0	0.32	0.51	0.62
7	200	50	10	0.32	3.39	0.10
8	200	100	0	0.34	0.80	0.40
9	200	150	5	0.55	1.74	0.33

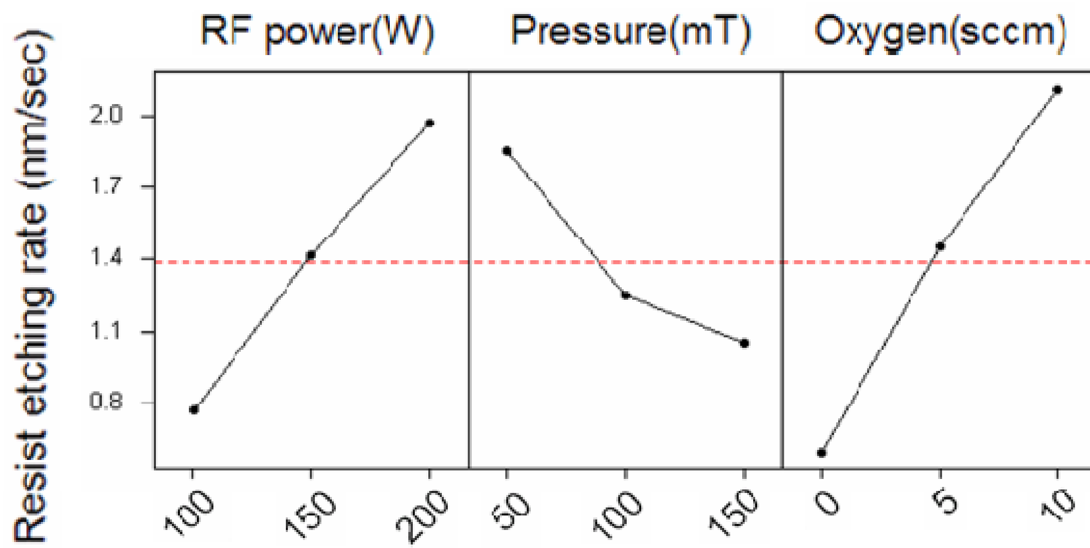
[a] Si E/R: silicon etching rate

[b] PR E/R: PMMA resist etching rate

[c] Rt Si/PR: the ratio of the silicon etching rate to the PMMA etching rate



a)



b)

Figure 4.6: Effect of RF power, pressure, and gas composition on the etching rates of silicon and PMMA.

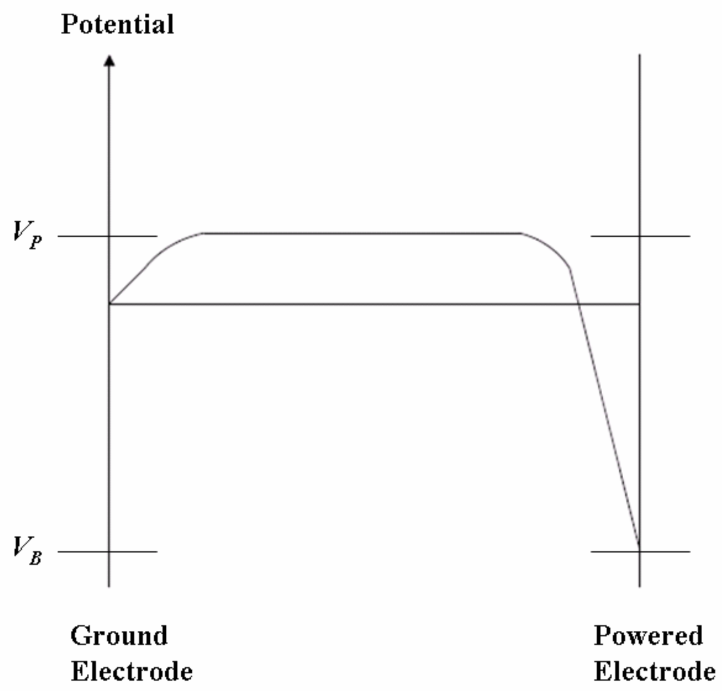


Figure 4.7: Potential distribution in a process chamber for an RIE system.

excitation angular frequency and the vacuum dielectric constant, and l_p and l_s are the length of plasma column and the sheath thickness. [114]

From the above equation, we can see the V_B is proportional to the applied RF power on the electrode and the sheath thickness. Furthermore, the measurement of sheath thickness as a function of the discharge pressure P, performed by Y. Catherine et al.[115] indicates that it is proportional to $P^{1/2}$.

Consequently, we conclude that V_B can be defined as following relation (4.2).[115]

$$V_B \propto \left(\frac{P_{RF}}{P}\right)^{1/2} \tag{4.2}$$

As the RF power increases, V_B will increase, which results in higher value of plasma sheath thickness, D_s, which is given by following equation (4.3) and (4.4).

$$D_s \approx \eta^{2/3} \times \lambda_D \tag{4.3}$$

$$\eta = \frac{e(V_P - V_B)}{kT_e} \tag{4.4}$$

Where λ_D is the Debye length, e is the electron charge, and T_e is the electron temperature. As D_S increases, the distance that the radicals travel onto the silicon surface increases and there is higher probability of collision among the radical and other ions or molecules in the sheath range. Consequently, this can affect the number of active etching species to

reach silicon surface and thus etching rate will saturate or drop in higher RF power range. When it comes to pattern transfer, too low silicon etching rate compared to PMMA does not show successful pattern transfer onto silicon. Therefore, we tried another etching gas system, SF_6-O_2 system, which is generating much larger concentration of fluorine radicals compared to CF_4-O_2 gas system. One of assumed reasons for higher fluorine radicals is that the dissociative electron attachment to SF_6 gas molecule has an extremely large cross section at low energies and is regarded as main decomposition process.[116] Furthermore, the bond strength of SF_5-F, about 85*k*cal/mol, is lower than bond strength of CF_3-F, 122*k*cal/mol. This bond strength difference might have different reactivity toward dissociation by electrons.

As for CF_4-O_2 gas system, initial experiments for SF_6-O_2 gas system were designed according to the DOE which consisted of three levels for the three process factors. The SF_6 flow rate was 45*sccm* with the O_2 flow rate varied.

Effects of the three process factors on the etching rates of silicon and PMMA and their ratio are provided in Table 4.5. Through statistical analysis of the data in Table 4.5, tendency of responses for each factor is estimated as shown in Figure 4.8 where it can be seen that both the individual etching rates and their ratio also show a strong dependency on RF power and oxygen flow rate. As the oxygen flow rate increases, the silicon etching rate also decreases since the silicon surface becomes oxidized.

As expected, the resist (PMMA) etching rate increases as the oxygen flow rate increases. In the low RF power region where the etching rate of silicon was considerably lower than that of the resist, the microloading effect was observed, i.e., the silicon etching rate was lowered as etching progressed as shown in figure 4.9. The term microloading effect is

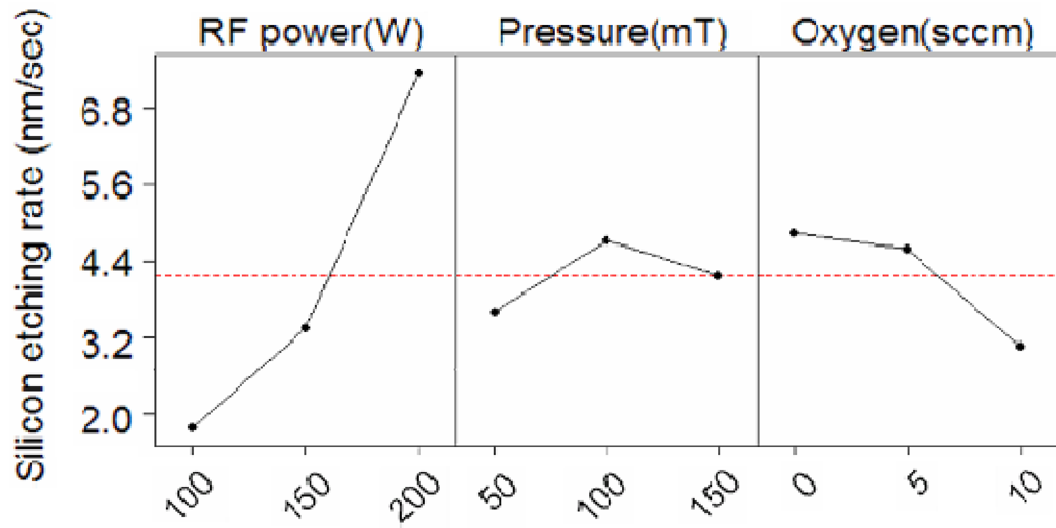
Table 4.5 Taguchi DOE for optimizing RIE process in SF_6-O_2 system.

No.	Factors			Responses		
	RF power, *W*	Pressure, *mtorr*	O_2, *sccm*	Si E/R [a], *nm/sec*	PR E/R [b], *nm/sec*	Rt Si/PR [c]
1	100	50	0	2.25	3.70	0.61
2	100	100	5	1.74	4.48	0.39
3	100	150	10	1.31	5.03	0.26
4	150	50	5	3.84	5.87	0.65
5	150	100	10	3.18	6.86	0.46
6	150	150	0	3.01	6.70	0.45
7	200	50	10	4.69	10.12	0.46
8	200	100	0	9.23	7.88	1.17
9	200	150	5	8.16	8.49	0.96

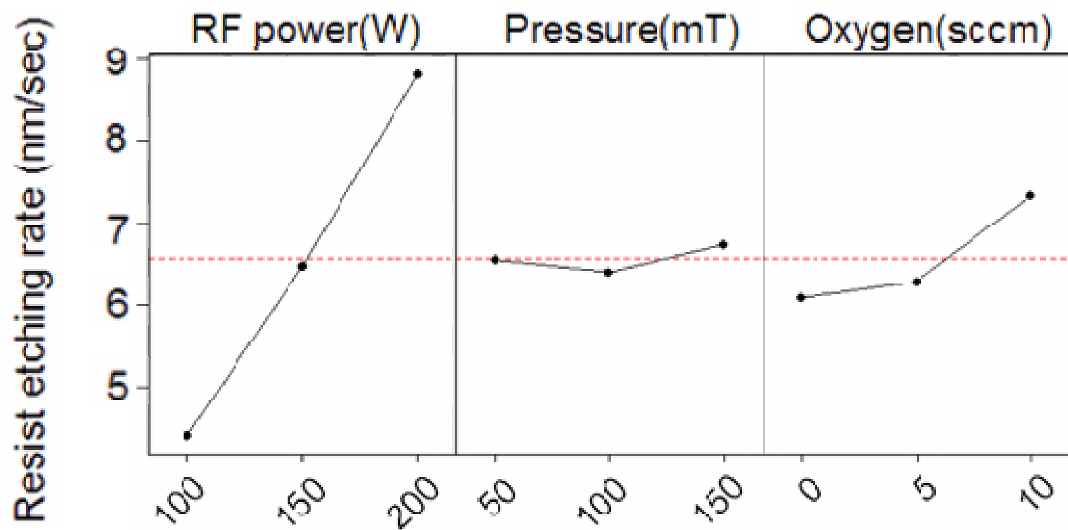
[a] Si E/R: silicon etching rate

[b] PR E/R: PMMA resist etching rate

[c] Rt Si/PR: the ratio of the silicon etching rate to the PMMA etching rate



a)



b)

Figure 4.8: Effect of RF power, pressure, and gas composition on the a) etching rates of silicon and b) PMMA.

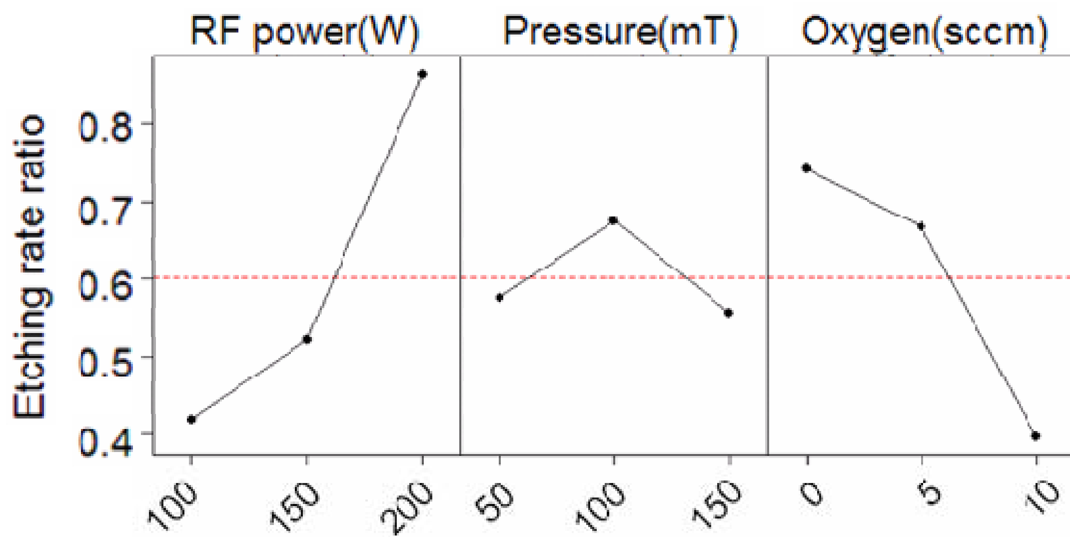
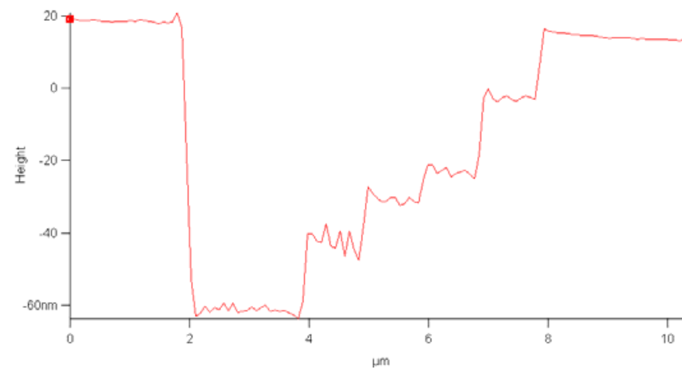
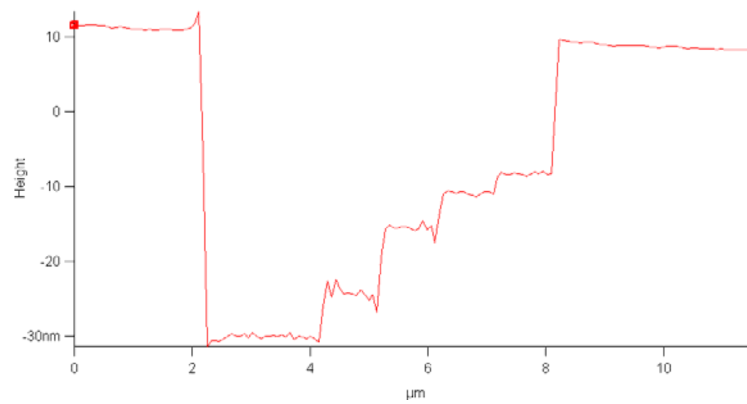


Figure 4.8: Continued. c) the ratio of the silicon etching rate to the PMMA etching rate.

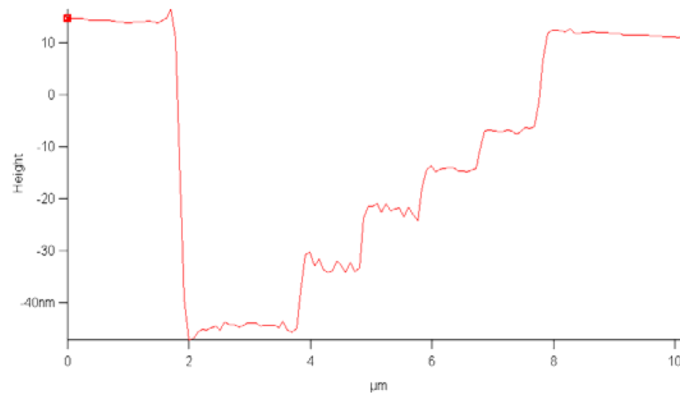


a)



b)

Figure 4.9: The etched pattern profiles of the staircase structures transferred into *Si* with condition of a) Power of 100*W*, SF_6 pressure of 50mtorr and Oxygen flow rate of 0*sccm*; b) Power of 100*W*, SF_6 pressure of 150mtorr and Oxygen flow rate of 10*sccm*.



c)

Figure 4.9: Continued. and c) Power of 150*W*, SF_6 pressure of 150mtorr and Oxygen flow rate of 0*sccm*. All those profiles show microloading effect.

often used when there is etch rate variation corresponding to local variation of pattern density and configuration. Micorloading effect means that pattern close together will etch at a lower rate than an isolated and identical feature in case that depletion of reactant species on surface is faster than transportation to the exposed area. [117]

For a relatively low RF power, the amount of active species is small and therefore the etching rate is limited by the transport rate of active species.[117] As the area of exposed silicon increases, the rate at which the active species are supplied to the silicon area doesn't scale up linearly, leading to a lower silicon etching rate as shown in figure 4.10. Decrease of silicon etching rate as the area increases normally means that the amount of active species being consumed in silicon area is higher than that in PMMA area but, higher etching rate of PMMA in the table 4.5 does not make sense to explain above assumption.

However, this may be explained, under the assumption of the same reactivity for both silicon and PMMA, by the fact that the volume per mole is smaller for silicon than for PMMA and silicon atom needs 4 F radicals to form volatile products. Silicon atom whose atomic weight is 28g/mole and density is 2.3g/cm^3 reacts with F radicals to form volatile SiF_4 or SF_2 and portion of SF_2 is only from 5 to 30%. [118] Thus, most of volatile gas is present as form of SiF_4. PMMA decomposition mechanism has not been clearly understood yet. However, postulated mechanism consists of three steps; Initiation, Propagation and Termination. In the initiation step, generated radicals, ions and atoms can react with PMMA to initiate PMMA decomposition which can be described as three competitive reactions. [119] First reaction is random chain scission which is normally induced by energy absorption such as electrons, photon and heat and lead cleavage the

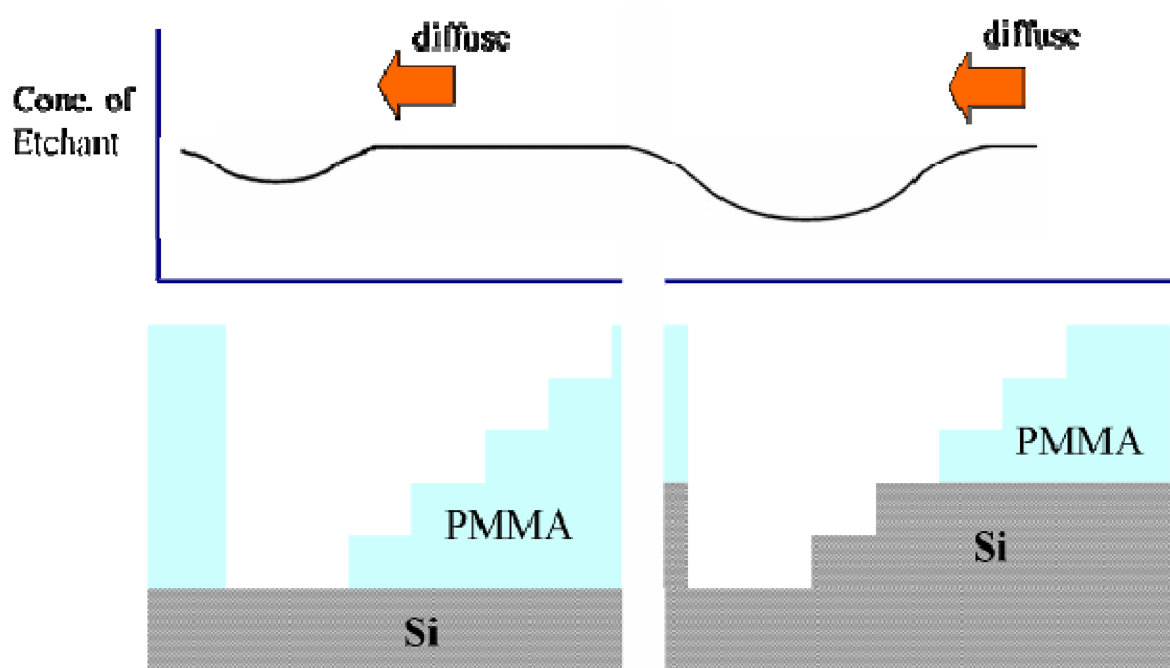


Figure 4.10: The schematic expression for the variation of etchant concentration and a cross section of etched structure as etching is proceeding. The concentration of etchant gas over silicone area is lower than over the PMMA area because silicon area is consuming more amounts of active etchant and is dropping down as exposed silicone area increased.

main chain bond or ester carbonyl group as shown in figure 4.11. For low RF power range, however, energy transfer by ion species bombardment is not effective because ions are not highly accelerated enough to get high acceleration energy. Next reaction type is reaction of polymer with plasma induced atomic oxygen. This type is not important in this experiment because we have microloading effect without oxygen. Third is reaction of polymer with plasma induced radicals. F radical abstracts hydrogen atom from the carbon chain and then polymer decomposition is initiated as shown in figure 4.12.

We can conclude, therefore, that in the low RF power range, consuming of active species, F radical, is directly related to the etching rate of PMMA.

The polymer unit involving initiation reaction with F radical is $C_5H_8O_2$ whose molecular weight is 100g/mole and density is 1.19g/cm^3. From the molecular weight and density, we obtained the volume per mole of silicon and PMMA polymer unit which are about 12.17cm^3/mole and 84.03cm^3/mole, respectively. Consequently, the etching rate of PMMA is much higher than that of Si, if PMMA polymer unit and silicon atom are assumed to react with an F radical with same reactivity. As shown in table 4.6, etching rate ratio between PMMA and silicon is about 3:1 which means consumption of active species in silicon area is still higher than in PMMA area in spite of higher etching rate of PMMA.

As the RF power is increased into the range shown in Figure 4.8, it appears that the microloading effect becomes insignificant and the 1:1 ratio of the silicon and resist etching rates is achievable. When the RF power is higher, more active species are generated and therefore, the silicon etching rate is limited not by the transport rate, but by reaction between silicon surface and active species. Hence, active species can be

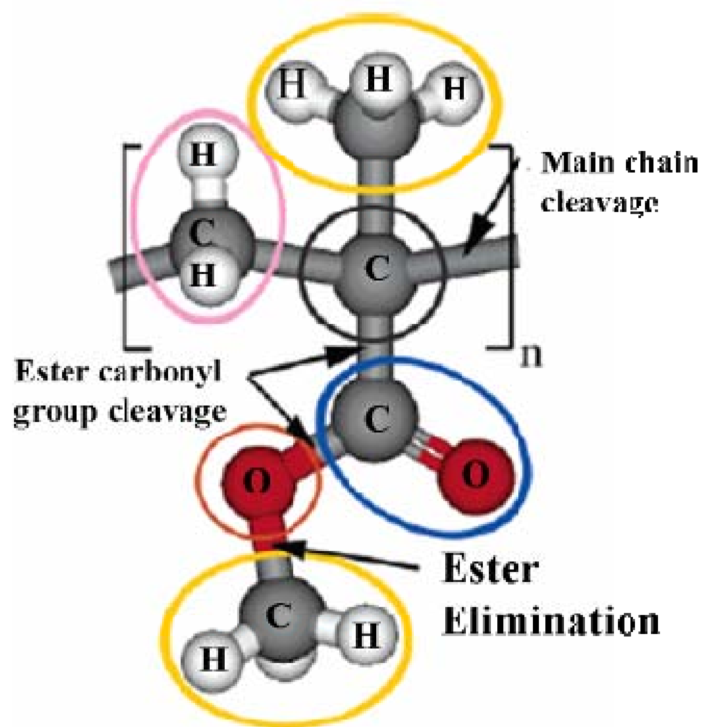


Figure 4.11: Representation of the PMMA cleavage scheme. PMMA decomposition is followed by the main chain cleavage or the ester carbonyl group cleavage mechanism.

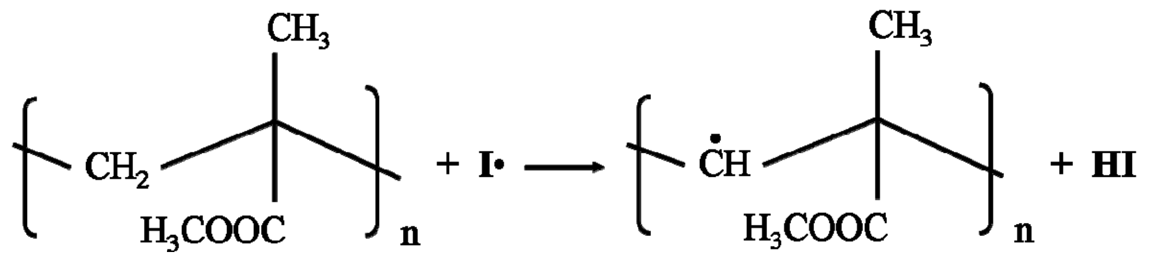


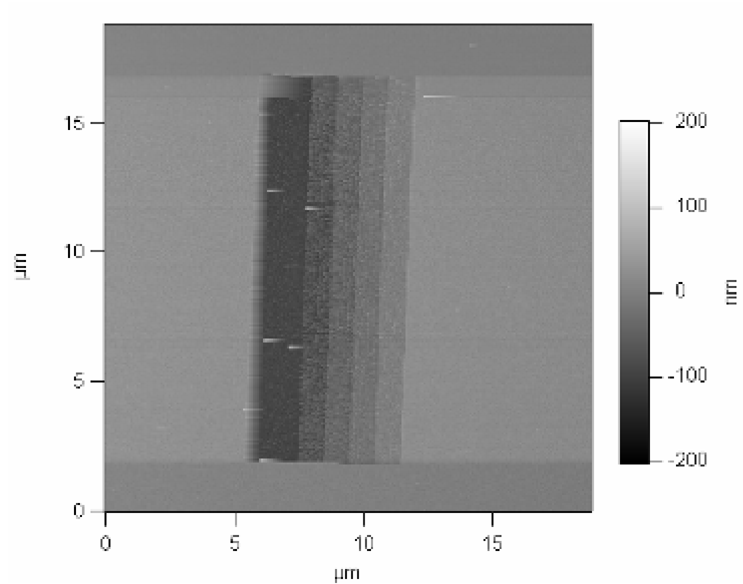
Figure 4.12: The reaction scheme of PMMA with plasma induced radicals (**I•**). The radicals are abstracting secondary hydrogen from the PMMA main chain, which gives the unsaturated polymer chain end and another polymer free radical.

provided in etching area with almost constant feeding rate and the microloading effect diminishes. Also, the energy associated with ion bombardment is higher for a higher RF power, increasing the silicon etching rate more than the PMMA etching rate thanks to the weaker Si-Si bonding energy (~ 2eV) of silicon than C-C (~ 3.5– 4.5eV) of PMMA[120], and in turn enabling the 1:1 ratio of the silicon and resist etching rates in the region of high RF power and low oxygen flow rate.

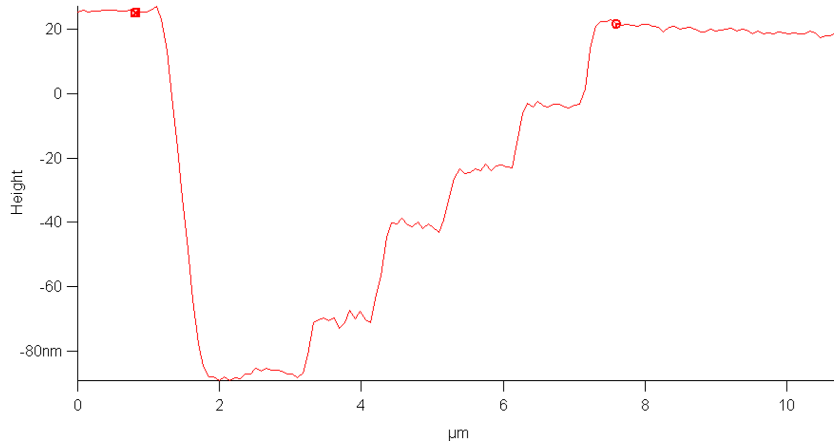
A few combinations of the three process factors, selected based on the tendencies in figure 4.10, were tried. The recipe RF power of 200 *W*, pressure of 100mtorr and oxygen flow rate of 2*sccm* resulted in an etching rate ratio very close to 1:1 and the best etched silicon profile. The etching rate of silicon was 9.48 and 8.97nm/sec for the staircase structures with the step width of 1.0µm and 0.5µm, respectively, and the PMMA etching rate for both structures was 8.72nm/sec.

The entire staircase structures are shifted down about 10nm and 5nm in the structures with step width of 1.0µm and 0.5µm, respectively. Ignoring this shift (which is most probably due to over-etching), the percentage step depth error is less than 2.1% for the two structures.

In Figures 4.13, etched silicon profiles obtained for the staircase structures are provided, which were measured by the Asylum MFP-3D AFM (atomic force microscope) and it can be observed that the remaining resist profiles of the staircase structures have been successfully transferred onto silicon. It is observed that the entire staircase structures are shifted down about 10nm and 5nm in the structures with step width of 1.0µm and 0.5µm, respectively and this is most probably due to over-etching. Ignoring this shift, the percentage step depth error is less than 2.1% for the two structures.

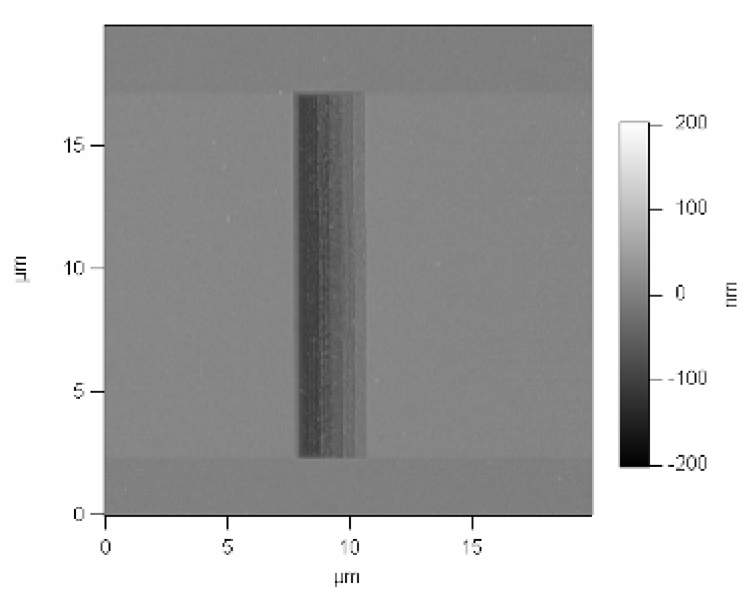


a)



b)

Figure 4.13: The etched pattern profiles of the staircase structures transferred into *Si* when the step width is 1.0µm ((a) top view and (b) cross-section: the left-most step is 2.0µm wide)



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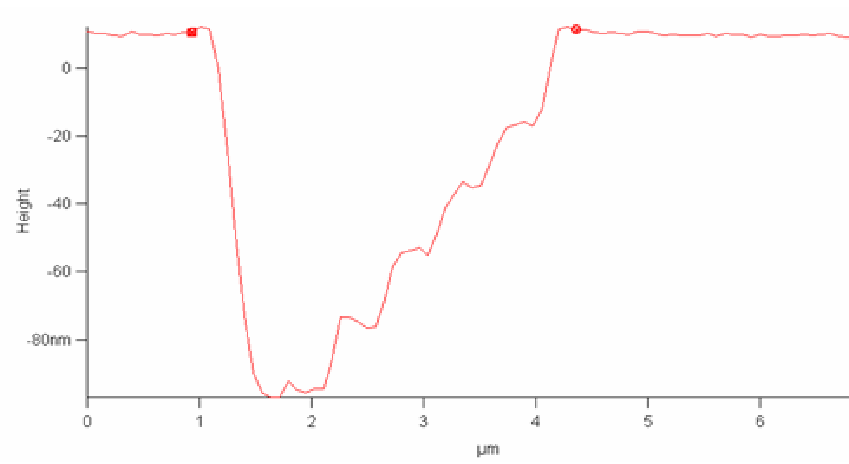


d)

Figure 4.13: Continued. and 0.5µm ((c) top view and (d) cross-section: the left-most step is 1.0µm wide).

CHAPTER 5

APPLICATION

5.1 Introduction

As semiconductor device dimensions continue to shrink, methods to determine precisely and correctly the size of a given structure become an important issue because the physical dimensions have a direct impact on chip performance. In the early days, linewidths were big enough to be imaged and measured on optical microscopes, but current device design rules result in structures which are so small as to challenge the performance of even the best scanning electron microscopes (SEM) by being required to routinely achieve a spatial resolution below 1nm.

In order to verify that the tool is reaching the required level of performance it is necessary to be able to continuously monitor and quantify its performance during use, and to be able to compare the imaging parameters of one tool with those of others, in such areas as resolution, signal to noise ratio, drift, and instability under standard operation conditions.

The Depth of Field (DoF) is also increasingly important in nano metrology because as feature sizes become smaller, there is a corresponding increase in aspect ratio and thus defocus effects on image profiles have become more significant. The DoF is the maximum vertical range over which the image resolution remains constant. If the convergence angle (numerical aperture NA) of the beam is α and the resolution is equated to the physical width of the beam, then the DoF is of the order of the resolution divided by α.

A recent improvement of CD-SEM resolution, which is usually accompanied by a larger α, has resulted in degradation of DoF especially in high magnification where the DoF depends on accelerating voltage and signal to noise ratio of image. Furthermore, as noted by Sato et al.[2] DoF is not well defined when the effect of lens aberrations which increase with an increasing beam convergence angle are included. It is, therefore, important to have a method to measure the DoF quantity directly and under realistic operating conditions.

5.2 Basic technique

The procedures employed here to determine the imaging resolution, and to extract additional information about the parameters which describe the imaging performance, are based on the use of two-dimensional power spectra (diffractograms) obtained from the Fourier analysis of recorded SEM images. These methods are commonly used for the analysis of optical tools and provide a consistent and thorough way of quantifying many aspects of the imaging behavior. The program now in use is the SMART routine described earlier [121] [122]], which is a macro routine in the public domain which is designed to work with the widely disseminated public domain image analysis programs NIH IMAGE[123], and SCION IMAGE[124]. When installed in IMAGE the SMART macro provides the automated routines which measure the spatial information transfer limit (i.e. resolution) and stigmation of a single image from the diffractogram, determine resolution and tool stability from a pair of sequentially recorded images (super-position diffractograms), and can determine the signal to noise ratio of digitally stored images (for such purposes as measuring the electron detector quantum efficiencies (DQE) [125]). In

this version the SMART package has been widely used and has proven to be a valuable diagnostic tool for the setting-up, and routine testing, of electron beam tools.

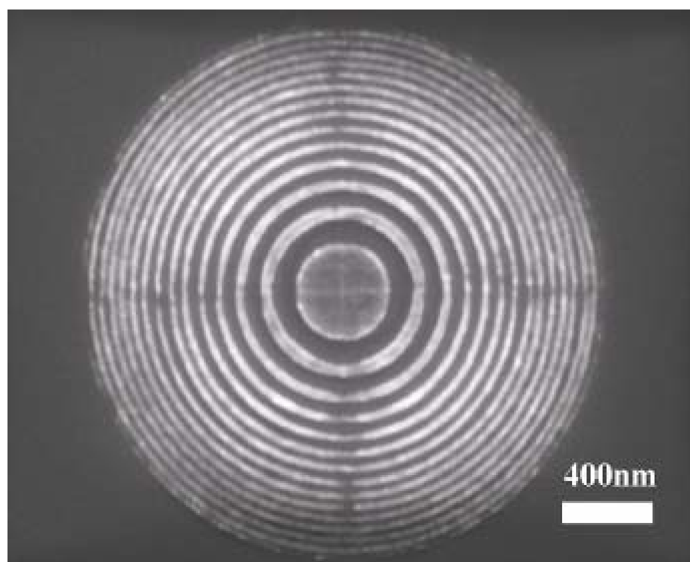
However, upgrades and enhancements for both the original Macintosh-based NIH IMAGE, and the later Windows-based SCION IMAGE programs have now ceased and both variants have been replaced by IMAGE JAVA [126] which replicates most of the facilities of the original programs but, recoded in Java, is now platform-independent and therefore more widely applicable. To accommodate this change the original SMART macro, which was written in a Pascal-like language, had to be replaced by a new SMART-J plug-in written in C++ which properly interfaces with the tools provided by IMAGE-J. The facilities provided by IMAGE-J, and as further extended by SMART-J, are similar to those of the original Mac or Windows versions although offering more facilities but a little less convenience because of some of the restrictions imposed by the use of JAVA. The full source code and documentation for the SMART-J plug-in, ready to be compiled and incorporated into IMAGE-J, are available from our website (http://pciserver.bio.utk.edu/metrology) or directly from the authors. Specifically, SMART-J can produce and analyze single image diffractograms to measure the spatial resolution and accuracy of stigmation correction; it can generate super-position diffractograms from a sequential pair of images to more precisely determine resolution and measure tool drift and instability; and it can measure the signal to noise ratio of stored digital images. Further enhancements provide the ability to obtain the optical transfer function (OTF) of the tool from an image[126], and generate data on quantities such as image entropy and normalized measures of performance[126] although these options are not covered in this paper.

5.3 Application of analysis program

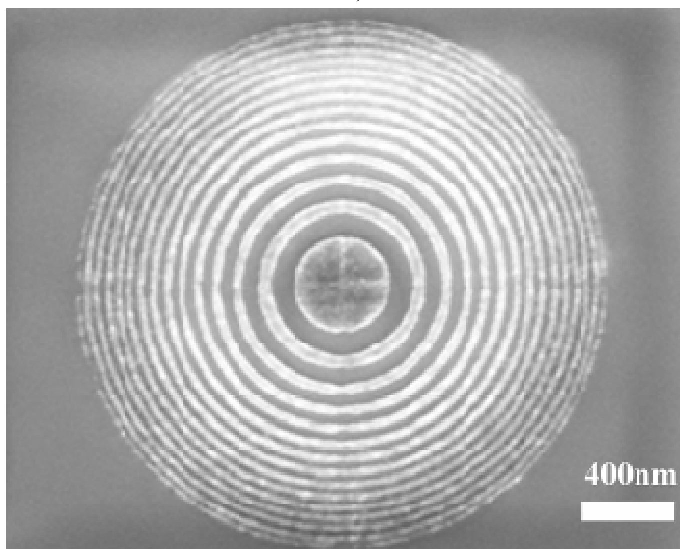
5.3.1 The application of Fresnel zone plates and analysis program for measuring of tool performance

A nano-fabricated HSQ Fresnel zone plate, and the SMART-J / IMAGE-J software, can be used to determine the imaging resolution of the tool under the chosen imaging conditions. The basis of the method is to obtain a diffractogram in the form of a power spectrum i.e. the two-dimensional Fourier transform, displayed as an intensity plot [127]. As a first step the FZP is imaged at the highest magnification which permits the complete zone plate structure to be captured as shown in figure 5.1. This guarantees the minimum possible pixel size. The IMAGE-J/SMART-J program combination displays the image contents by plotting the intensity distribution as a function of spatial frequency as shown in figure 5.2. The signal intensity decreases with increasing frequency (i.e. going away from the center of the diffractogram) and finally drops to the level of random background noise. The diffractogram power spectrum computed through the fast Fourier transform can be quantified in one of the two ways. The “automatic mode” fits an ellipse around the threshold region which represents the signal information as illustrated in figure 5.3. The major and minor axes of the ellipse (in units of inverse nanometers) are recorded to yield an overall resolution value in nanometers. The eccentricity E of the ellipse, i.e. the deviation from the ideally isotropic pattern is defined as the following equation (5.1);

$$E = \frac{(L_{maj} - L_{\min})}{L_{maj}} \qquad (5.1)$$



a)



b)

Figure 5.1: Fresnel zone plate fabricated on 50nm HSQ: a) the base dose of 480μC/cm^2 and developed in TMAH for 70seconds, TMAH: D.I.W = 1:9 for 10seconds and D.I.W for 10seconds and b) the base dose of 460μC/cm^2 and developed in 0.26N TMAH for 70seconds, TMAH: D.I.W = 1:10 for 60seconds and D.I.W for 60seconds. SEM images are taken at 2keV on a LEO 1525 scanning electron microscope.

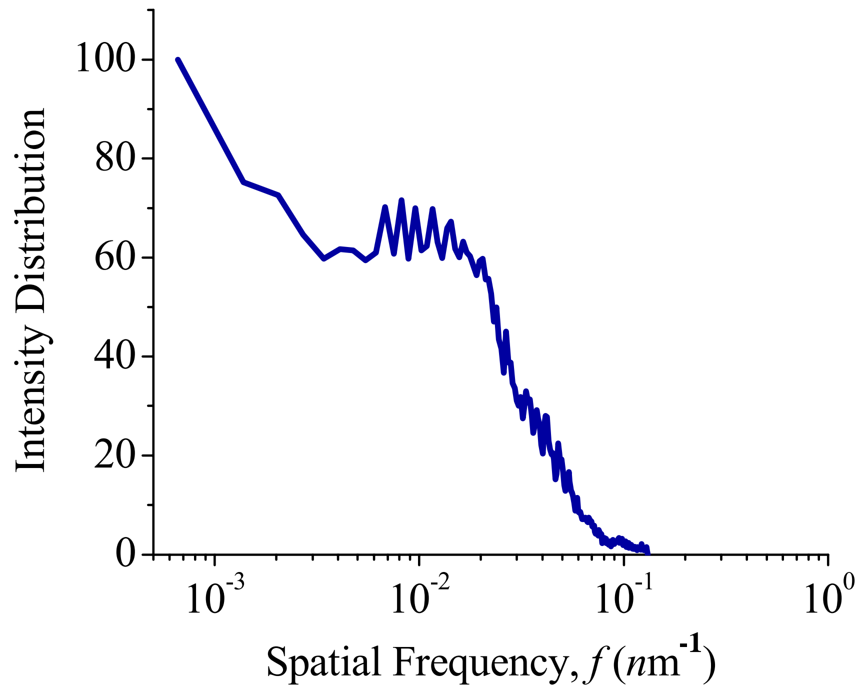


Figure 5.2: The intensity distribution normalized by the maximum value is plotted as a function of spatial frequency, *f*.

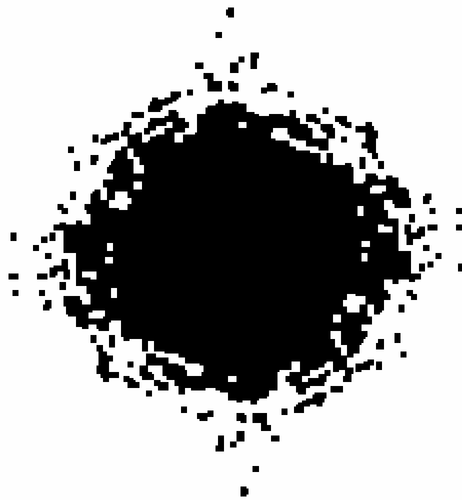


Figure 5.3: The diffractogram power spectrum of the central 512x512 pixel region of the image shown in figure 5.1. The power spectrum shown has been thresholded to display the boundary between signal and noise which defines the spatial resolution.

where L_{maj} and L_{min} are the lengths of major and minor axis, respectively. The eccentricity measures the stigmatic error which should be less than 0.1 and, ideally less than 0.05, in a well aligned and operated tool. The "manual mode" superimposes concentric circles, representing the spatial resolution in nanometers, over the power spectrum display which are directly calibrated as shown in figure 5.4. The concentric circle corresponding to the outer boundary of diffractogram represents the resolution of the image and the stigmatic correction is judged visually. In either mode, the highest spatial resolution obtained from the power spectrum is limited to the interval of two pixels, and thus images must be taken at a sufficiently high magnification to have the pixel size, at least a factor of three smaller than the anticipated resolution limit of the tool. We obtain the spatial resolution of about 13 to 15nm and eccentricity of 0.13 calculated and judged from obtained spectra.

Although the above approach can provide reliable data on resolution and the accuracy of stigmatic correction, it is subject to two significant deficits. Separating the signal from noise on the power spectrum is performed by manually setting the threshold, although the boundary between the signal and noise from a single image cannot be determined on a pixel by pixel basis. Therefore, there is a certain degree of uncertainty in defining the resolution properly even for a skilled the operator. The second limitation is that the resolution obtained from a single image only represents the tool performance over the relatively short period used for the image recording. Time-dependent parameters such as beam drifting, focus variation, and power supply instabilities can degrade the repeatability of parameters and precision of the tool and thus affect the overall performance of the tool.

Thus these limitations can be overcome by applying the "super-position diffractogram

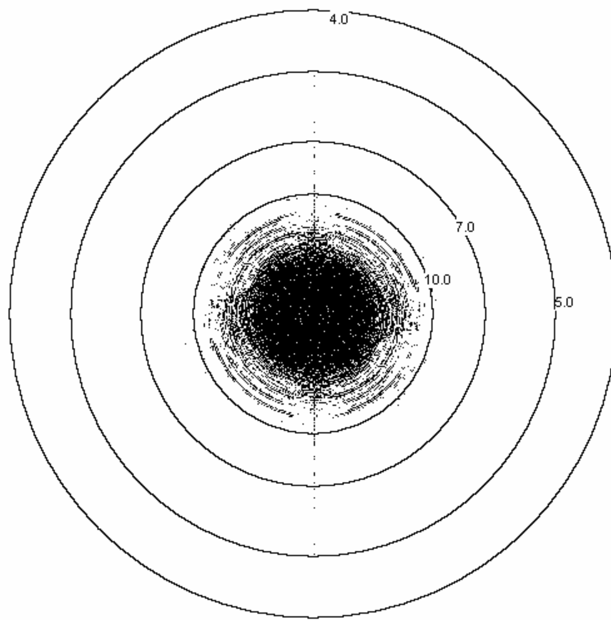


Figure 5.4: Manual mode analysis of the Power Spectrum derived from the image shown in figure 5.1. The superimposed rings are calibrated directly in units of nanometers.

mode" that is also offered by SMART-J. [128] In this mode, two sequential images taken a few minutes apart and under identical imaging conditions are digitally superimposed with a horizontal offset of typically 16 or 32 pixels to form a composite micrograph. The diffractogram of this composite looks like the power spectrum of either image but is crossed by a fringe pattern whose spacing is inversely proportional to the offset imposed. This method, first described by Frank et al. [128], has been widely used for measuring the performance of transmission electron microscopes (TEM) but is also applicable to the SEMs. [128] The fringes crossing the power spectrum represent interference ("Youngs Fringes") between details present in both versions of the images, and the power ratio of the coherent signal fringes to the incoherent noise is enhanced by a factor of four. The fringes vanish at the spatial frequency at which the signal vanishes into the noise. There is, thus, no uncertainty in identifying the maximum spatial frequency of information transfer in the images. Figure 5.5 shows a superposition diffractogram generated from the FZP. The two images analyzed were recorded at 2keV in a LEO FEGSEM at a magnification of 31kX and taken with a 40seconds time interval between exposures. The measured resolution is about 10 to 12nm which is a slightly more optimistic estimate when compared to the resolution of 13 to 15nm obtained from the single image procedures. This is because the high fringe modulation contrast (signal) is now easily distinguished from the weak, unmodulated, noise background. The information on the precision and stability of tool over the time interval required to record the two images is also obtained through the analysis of the super-position diffractogram. The fringes in the diffractogram are due to the lateral offset between the two images, and should therefore be completely vertical. Any deviation from the vertical indicates that there has been some

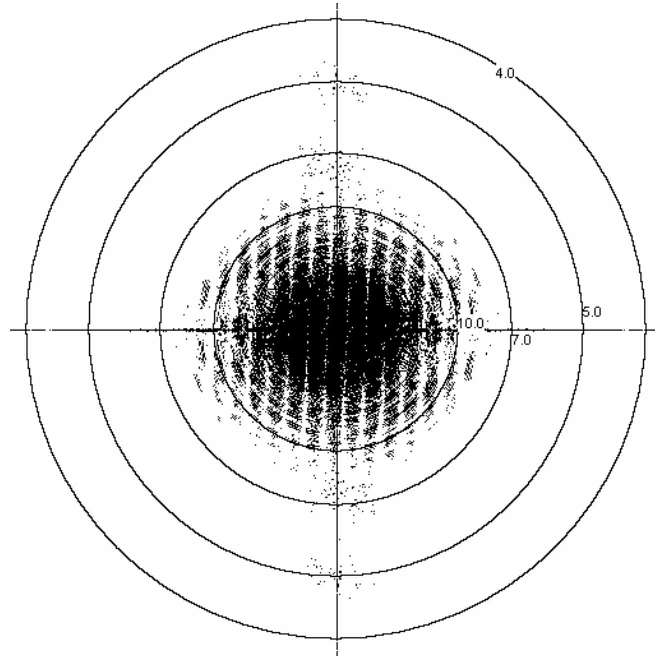


Figure 5.5: Power spectrum obtained from superposition diffractogram mode.

type of beam or stage drifting or instability. The magnitude of the drift over the elapsed time period, D, can be expressed by the following relationship.

$$D = 2*(\text{pixel offset} * \text{pixel size (nm)})*\sin(\theta/2)$$

where θ is the angle between the fringe pattern and the vertical. Here the pixel offset is 32 pixels with the pixel size of 3.8nm, and θ is 3.5degrees, so the drift D is 7.43nm over a period of 40seconds. Consequently, the drift rate less than 1nm per second is readily identified and measured by this method.

5.3.2 The application of staircase structres and analysis program for SEM DoF

The combination of a fabricated staircase structure and the SMART-J/IMAGE-J software is also applied to provide the information to determine the DoF of the tool under the chosen imaging conditions. Application is performed by following procedure. First the SEM is carefully focused on a the highest or lowest step in a staircase structure and images are then taken from each of the steps in turn without making further adjustments of focus. IMAGE-J/SMART-J program which uses Fourier methods is then applied to calibrate image and determine the spatial information limit defining the boundary between signal and noise in the obtained diffractogram. The image resolution as a function of the defocus quantifies the through-focus behavior and depth of field of the tool under the chosen imaging conditions, and provides the data necessary to derive a functional model of the DoF behavior. The optical Transfer Function (OTF) as a function

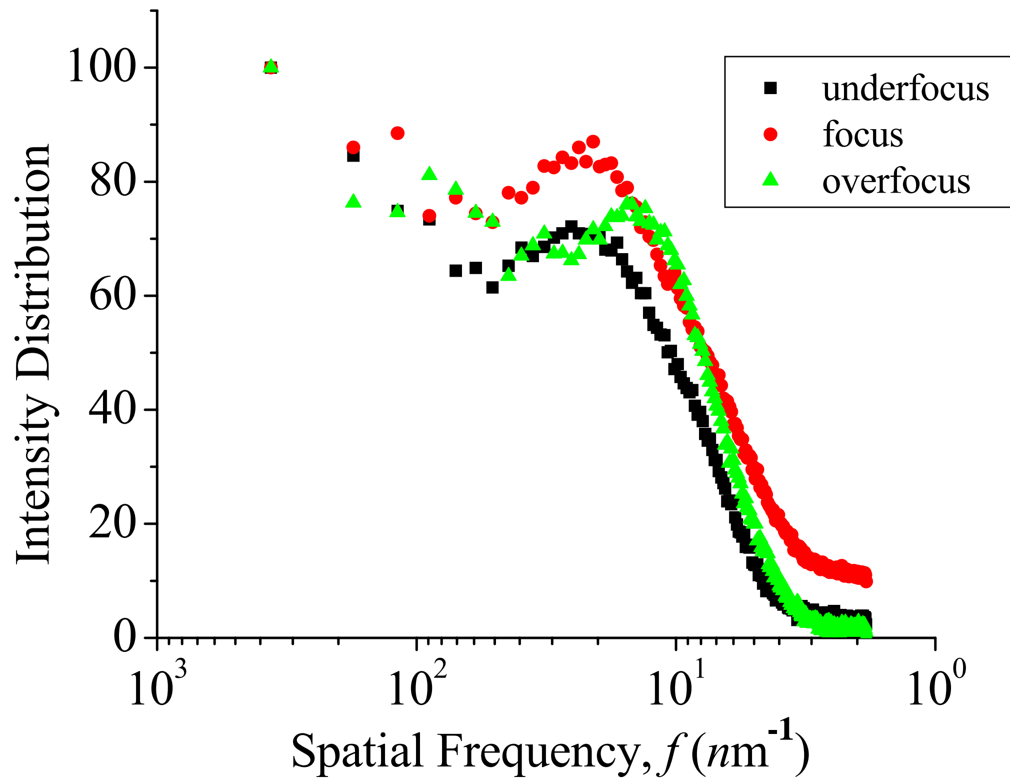
of spatial frequencies is for the focus and out of focus, i.e. over focus and under focus is obtained through the Fast Fourier Transform and displayed in figure 5.6.

The intensity of the signal for three types of focus decreases with increasing frequency and finally drops to the level of random noise background. Optical transfer function (OTF) shows response of SEM to the spatial frequency where defocus in the high and medium spatial frequencies shows lower signal intensity and is passed with reduced fidelity. From the diffractogram power spectrum, Fourier transform data can be quantified in one of two ways as explained previous section. The diffractogram power spectrums for three types of focus obtained by the automatic mode and manual mode are shown in figure 5.7 and figure 5.8. Power spectrum obtained through above methods shows the variation of image resolution which is degraded from about 3 to 4 nm when the image focus becomes defocused.

In spite of providing a good standard parameter such as image resolution, above approach is subject to two significant deficits also indicated in previous section. Therefore, we applied super-position diffractogram mode to get imaging parameters.

In figure 5.9, superposition diffractogram is generated from the analysis of two successive SEM images which were recorded at 12keV in a LEO FEGSEM at a magnification of 120kX and taken with 50seconds of time interval. Obtained resolution from the superposition diffractogram mode is almost same as previously obtained resolution values. The information about the precision and stability of tool over the time is also obtained through the analysis of diffractogram.

Drift D are for focus, over foucs and under focus autimatically calculated from equation



a)

Figure 5.6: The intensity distribution as a function of spatial frequencies. a) Normalized signal change as a function of spatial frequency.

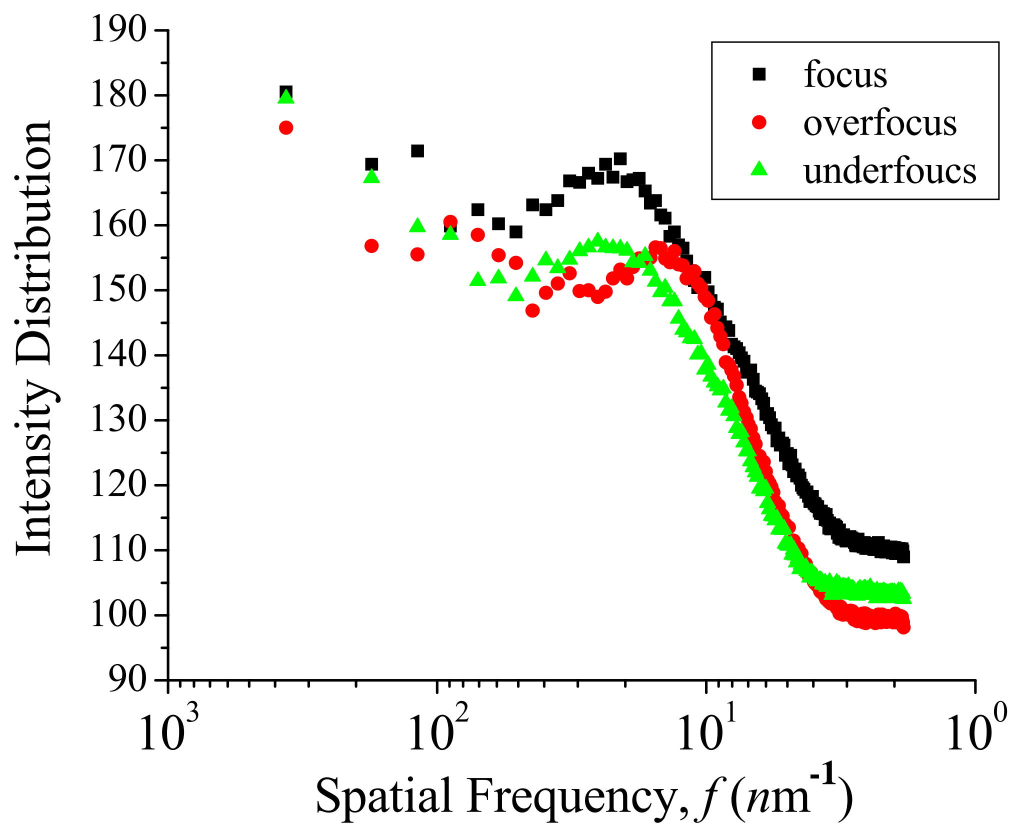
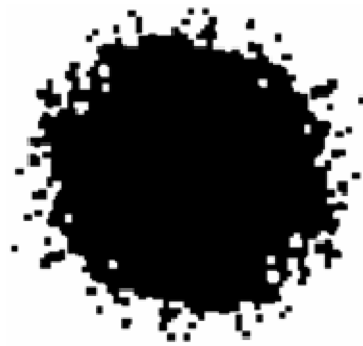


Figure 5.6: Continued. and b) signal change as a function of spatial frequency. The intensity distribution has been thresholded to display the boundary between signal and noise which defines the spatial resolution.

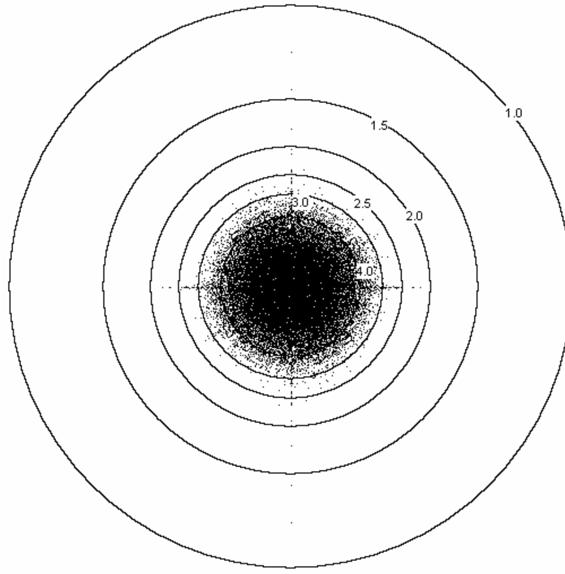
a)



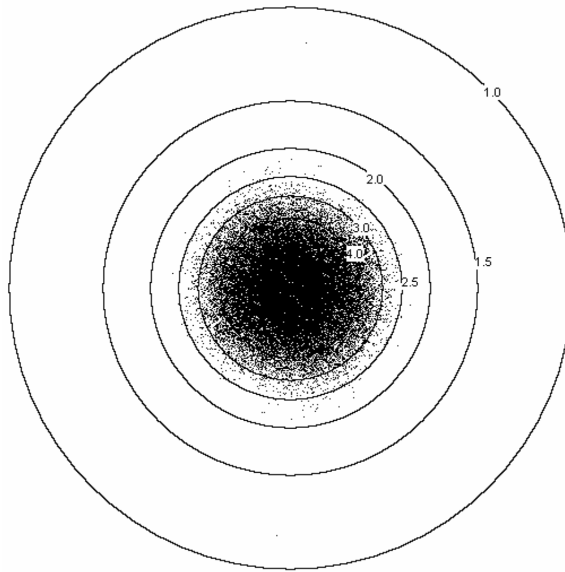
b)

c)

Figure 5.7: Diffractogram power spectrums obtained from automatic analysis mode; a) over focus, b) focus, and c) under focus.

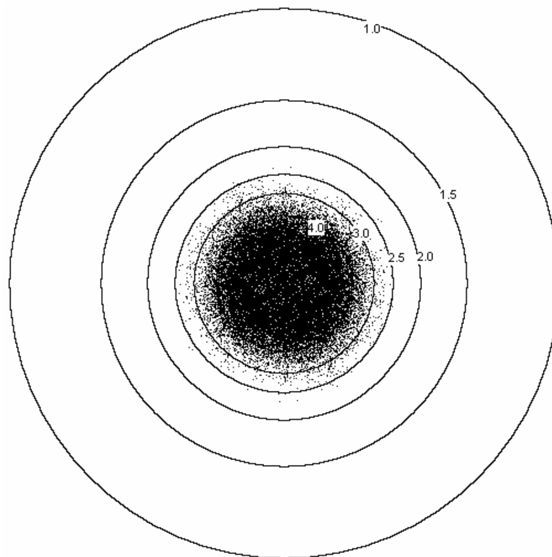


a)



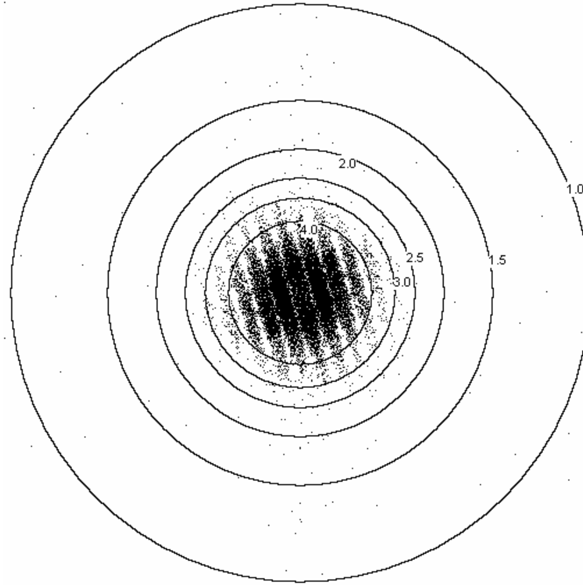
b)

Figure 5.8: Manual mode analysis of the Power Spectrum; a) under focus, b) focus.

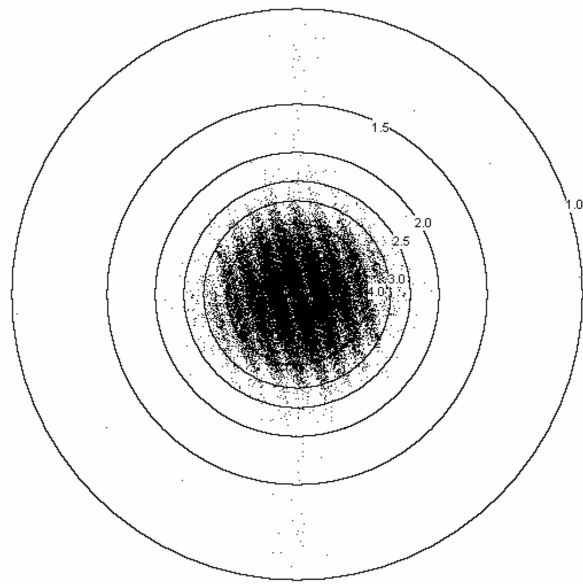


c)

Figure 5.8: Continued. and c) under focus. The superimposed rings are calibrated directly in units of nanometers.

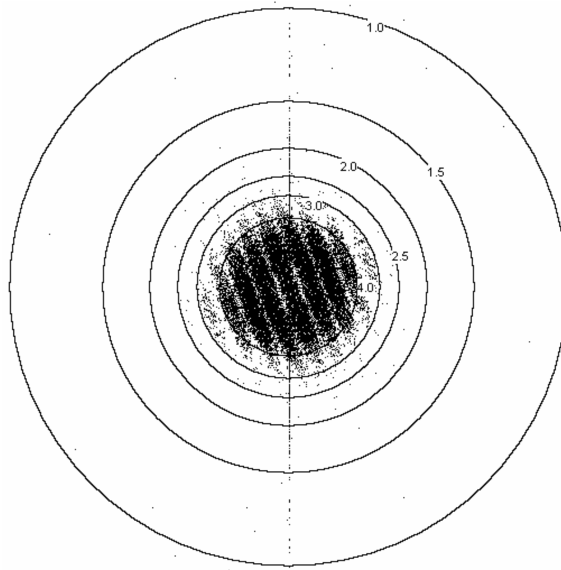


a)



b)

Figure 5.9: Power spectrum obtained from superposition diffractogram mode; a) under focus, b) focus.



c)

Figure 5.9: Continued. and c) over focus.

(5.2). Here the pixel offset is 32 pixels, the pixel size of 0.928nm/pixel, and. are 14, 14 and 15 degrees for focus, over focus and under focus, respectively, so the corresponding drift D are 7.23, 7.28, and 7.75nm over a period of 50seconds.

Consequetly, Drift rates as low as 1nm per second are readily identified and measured by this method.

5.4 Summary

Fresnel zone plate on PMMA and HSQ resist is successfully fabricated through electron beam lithography process and proximity correction program (PYRAMID) for the purpose of optimized imaging targets. Especially the zone plate structure fabricated on HSQ resist provide a useful level of imaging contrast and the symmetrical structure which makes it possible to achieve optimum imaging performance. The combination of the package of software designed to provide diffractogram through the Fast Fourier Transform and fabricated Fresnel zone plate provides the ability to quickly and accurately measure the imaging resolution for an SEM. In particular the super-position diffractogram method applying two sequential images which are taken with realistic time interval, is highly useful method for determining the resolution of a tool because of the enhanced true information through the correlation of each signal. The replication of same specification of measurement samples through lithographic process makes it enable to compare the performance of instruments in different locations and collect the performance data of given instrument over different time.

CHAPTER 6

CONCLUSION

The objective of my research was to fabricate the nano scale test structures by electron beam lithography processes studying control of pattern dimension (2 and 3-dimesionally) with proximity effect correction program and apply those fabricated structures to electron-optical systems for test of its performance. Electron Beam Lithography (JBX 6000 FS/E) was employed and parameters such as beam energy, beam current and aperture size were controlled and set to generate the best resolution. The fabrication of nano size structures can be accomplished by control of factors such as type of resists, base doses, baking system, pixel size, developing conditions which are developers and temperature, and proximity effect control.

Fabrication of Fresnel zone plates employs PMMA and HSQ as resist and proximity correction program (PYRMID) to give e-beam energy given on each ring. Control of factors such as baking system and developing conditions led successful fabrication of zone plates and study performed here indicates that understanding of deposited energy variation as pattern position and relationship between baking system or developing conditions and results, is very important to give ensured pattern dimension.

Especially the zone plate structure fabricated on HSQ resist provide a useful level of imaging contrast and the symmetrical structure which makes it possible to achieve optimum imaging performance.

Staircase structures are successfully fabricated on PMMA by grayscale lithography

process and transferred onto silicon substrate by RIE process. In this study, the issue of controlling feature depth in grayscale E-beam lithography and etching processes has been studied. For the E-beam lithographic process, dose to be given to each feature is derived from the exposure-depth mapping function by using the grayscale E-beam proximity effect correction scheme (PYRAMID). For the pattern transfer, Taguchi Design of experiment method is applied to plan the experiments and analyze obtained results statistically. The etching process is guided by controlling the etching rates of the resist (PMMA) and silicon substrate such that the desired structures are eventually transferred onto the substrates. Through experiments, it has been shown that depth control in the resolution of $O(10)$ nm is achievable. The percentage error of step depth in the two staircase structures considered is less than 2.5% in the E-beam lithography process and less than 2.1% in the final etched silicon profiles.

The application of fabricated structures to electron optical system is performed to obtain imaging parameters such as resolution, signal to noise ratio, drift, instability and Depth of Focus under standard operation conditions.

The combination of the package of software designed to provide diffractogram through the Fast Fourier Transform and fabricated Fresnel zone plates and staircase structures provides the ability to quickly and accurately measure the imaging resolution of zone plates for SEM and the imaging resolution according to focus and defocus which are corresponding to imaging depths for an SEM.

In particular the super-position diffractogram method applying two sequential images which are taken with realistic time interval is highly useful method for determining the resolution of a tool because of the enhanced true information through the correlation of

each signal. The replication of same specification of measurement samples through lithographic process makes it enable to compare the performance of instruments in different locations and collect the performance data of given instrument over different time.

The studies described in this thesis were focused on the basic fabrication techniques of test structures on silicon substrate and its application. For fabrication of smaller dimension and perfect shape of structures, further studies in such field as proximity effect correction for ring structures pattern where exposure directions are in x and y, and various developing system and baking system are needed.

Especially, for the application to various electron-optical systems such as TEM, fabrication of Fresnel zone plate will be studies on various substrate or membrane.

For staircase structures, more efforts will include consideration of smaller features (step width), optimization of the E-beam lithographic and etching processes which can control transferred pattern dimensions.

REFERENCES

1. Thomson, L.F., *Introduction to Microlithography.* American Chemical Society, 1994. **1**.
2. F. Hu, S.Y.L., J. Vac. Sci. Technol., 2003. **B 21**: p. 2672.
3. B. J. Lin, P.R.-C., *Handbook of Microlithography, Micromachining, and Microfabrication*, ed. P. Rai-Choudhury. Vol. 1. 1997: SPIE Optical Engineering Press. 3.
4. F. Hu, S.Y.L., *Dose control for fabrication of grayscale structure using a single step electron-beam lithographic process.* J. Vac. Sci. Technol., 2003. **B 21**: p. 2672.
5. M. L. Schattenburg, H.I.S., *The critical role of metrology in nanotechnology.* proc. SPIE 4608, 2001: p. 1.
6. M. T. Postek, J.S.V., A. E. Vladar, J. Vac. Sci. Technol., 2005. **B 23**: p. 3015.
7. J. Kim, K.J., S. Deo, S. Y. Lee, D Joy, *Tools to Measure CD-SEM Performance.* Proc. SPIE, 2006. **6152**: p. 279.
8. Beall, K.F., Art Journal, 1980. **39**(3): p. 195.
9. A. Goldstein, S.A., *The Solid-State Century*, in *Scientific America*. 1997. p. 80.
10. Thomson, L.F., *Introduction to Microlithography*, ed. C.G.W. L. F. Thomson, and M. J. Bowden. Vol. 1. 1994, Washington, DC: American Chemical Society. 1.
11. G. L. T. Chiu, J.M.S., IBM Journal of. Research and Development, 1997: p. 41.
12. S. Magdo, M.H., C. H. Ting, IBM Journal of. Research and Development, 1971: p. 446.
13. S. Wolf, R.N.T., *Silicon Processing for the VLSI era*. 2 ed. Vol. 1. 2000: Lattice Press. 546.
14. Washo, B.D., IBM Journal of. Research and Development, 1977. **21**(2): p. 190.
15. Jyh-Ping Hsu, S.-W.H., Shiojenn Tsengb, Journal of The Electrochemical Society, 2000. **147**(5): p. 1920.
16. S. Wolf, R.N.T., *Silicon Processing for the VLSI era*. 2 ed. Vol. 1. 2000: Lattice press. 510.
17. Hatzakis, M., IBM Journal of. Research and Development, 1988. **32**: p. 441.
18. S. Wolf, R.N.T., *Silicon Processing for the VLSI era*. 2 ed. Vol. 1. 2000: Lattice Press. 547.
19. Bruning, J.H., J. Vac. Sci. Technol., 1980. **B 17**: p. 1147.
20. Thomson, L.F., *Introduction to Microlithography*, ed. C.G.W. L. F. Thomson, and

M. J. Bowden. 1994, Washington, DC: American Chemical Society. 22.
21. S. Wolf, R.N.T., *Silicon Processing for the VLSI era*. 2 ed. Vol. 1. 2000: Lattice Press. 548.
22. L. F. Thomson, C.G.W., and M. J. Bowden, *Introduction to Microlithography*, ed. C.G.W. L. F. Thomson, and M. J. Bowden. 1994, Washington, DC: American Chemical Society. 24.
23. Fuller, G.E., *Handbook of Semiconductor Manufacturing Technology*, ed. R.D. Y. Nishi. 2000: Marcel Dekker, Inc. 461.
24. B. J. Lin, P.R.-C., *Handbook of Microlithography, Micromachining, and Microfabrication*, ed. P. Rai-Choudhury. Vol. 1. 1997, WA: SPIE Optical Engineering Press. 57.
25. Okazaki, S., J. Vac. Sci. Technol., 1991. **B 9**: p. 2829.
26. Bowden, M.J., *Introduction to Microlithography*, ed. C.G.W. L. F. Thomson, and M. J. Bowden. Vol. 1. 1994, Washington, DC: American Chemical Society. 120.
27. Cerrina, F., *Handbook of Microlithography, Micromachining, and Microfabrication*, ed. P. Rai-Choudhury. 1997, WA: SPIE Optical Engineering Press. 253.
28. Spiller, E., IBM Journal of. Research and Development, 1993. **37**: p. 291.
29. Heuberger, A., J. Vac. Sci. Technol., 1988. **B 6**(1): p. 107.
30. S. Wolf, R.N.T., *Silicon Processing for the VLSI era*. 2 ed. 2000: Lattice Press. 644.
31. G. Stengle, H.L., W. Maurer, P. Wolf, J. Vac. Sci. Technol., 1986. **B 4**(1): p. 194.
32. S. Wolf, R.N.T., *Silicon Processing for the VLSI era*. 2 ed. Vol. 1. 2000: Lattice Press. 650.
33. I. M. Templeton, M.F., L. E. Erickson, F. Chatenoud, E. S. Koteles, H. G. Champion, J. J. He, and R. Barber, J. Vac. Sci. Technol., 1995. **B 13**(6): p. 240.
34. H. C. Pfeiffer, T.R.G., T. H. Newman, IBM Journal of. Research and Development, 1988. **32**: p. 494.
35. Boers, A.N., IBM Journal of. Research and Development, 1988. **37**: p. 291.
36. F. J. Hohn, A.D.W., P. Coane, IBM Journal of. Research and Development, 1988. **32**: p. 514.
37. S. Wolf, R.N.T., *Silicon Processing for the VLSI era*. 2 ed. Vol. 1. 1988: Lattice Press. 638.
38. T. R. Groves, J.G.H., D. K. Bailey, H. C. Pfeiffer, D. Puisto, IBM Journal of.

Research and Development, 1993. **37**: p. 411.

39. L. K. Hanes, A.M., J. Vac. Sci. Technol., 1989. **B 7**(6): p. 1426.
40. M.G. Rosenfield, M.G.R.T., P. J. Coane, K. T. Kwietniak, J. Keller, K. P. Klaus, R. P. Volant, C. R. Blair. K. S. Tremaine, T. H. Newman, and F. J. Hohn, J. Vac. Sci. Technol., 1993. **B 11**(6): p. 2615.
41. D. S. Alles, F.R.A., A. M. Johnson, and R. L. Townsend, J. Vac. Sci. Technol., 1975. **B 12**: p. 1252.
42. Lieberman, B., J. Vac. Sci. Technol., 1978. **B 15**: p. 913.
43. Bowden, M.J., *Introduction to Microlithography*. 2 ed, ed. C.G.W. L. F. Thomson, and M. J. Bowden. 1994, Washington, DC: American Chemical Society. 117.
44. M. A. McCord, M.J.R., *Handbook of Microlithography, Micromachining, and Microfabrication*, ed. P. Rai-Choudhury. Vol. 1. 1997, WA: SPIE Optical Engineering Press. 143.
45. S. B. Rishton, H.S., D. P. kern, H. E. Luhn, T. H. P. Chang, G. A. Sai-Halasz, M. R. Wordeman, E. Ganin, and M. Polcari, J. Vac. Sci. Technol., 1988. **B 6**(1): p. 140.
46. B. J. Van Wees, H.V.H., C. W. J. Beenakker, J. G. Williamson, L. P. Kouwenhoven, D. van der Marel, C. T. Foxon, Phys. Rev. Lett., 1988. **60**: p. 848.
47. Saitou, N., *Handbook of Semiconductor Manufacturing Technology*, ed. R.D. Y. Nishi. 2000: Marcel Dekker, Inc. 571.
48. Bowden, M.J., *Introduction to Microlithography*, ed. C.G.W. L. F. Thomson, and M. J. Bowden. 1994, Washington, DC: American Chemical Society. 111.
49. M. A. McCord, M.J.R., *Handbook of Microlithography, Micromachining, and Microfabrication*, ed. P. Rai-Choudhury. Vol. 1. 1997, WA: SPIE Optical Engineering Press. 147.
50. S. Wolf, R.N.T., *Silicon Processing for the VLSI era*. 2 ed. Vol. 1. 2000: Lattice Press. 500.
51. D. F. Kyser, R.P., IBM Journal of. Research and Development, 1980. **24**: p. 426.
52. I. Haller, M.H., R. Srinivasan, IBM Journal of. Research and Development, 1968. **12**: p. 251.
53. T. M. Hall, A.W., L. F. Thompson, J. Vac. Sci. Technol., 1980. **B 16**(6): p. 1889.
54. L. F. Thomson, L.E.S., E. M. Doerries, J. Vac. Sci. Technol., 1978. **B 13**(3): p. 938.
55. Willson, C.G., *Introduction to Microlithography*, ed. C.G.W. L. F. Thomson, and

M. J. Bowden. 1994, Washington, DC: American Chemical Society. 200.

56. Willson, C.G., *Introduction to Microlithography*, ed. C.G.W. L. F. Thomson, and M. J. Bowden. 1994, Washington, DC: American Chemical Society. 205.
57. M. A. McCord, M.J.R., *Handbook of Microlithography, Micromachining, and Microfabrication*, ed. P. Rai-Choudhury. 1997, WA: SPIE Optical Engineering Press. 201.
58. H. W. Deckman, J.H.D., J. Vac. Sci. Technol., 1983. **B 1**(4): p. 1166.
59. Broers, A.N., IBM Journal of. Research and Development, 1988. **32**: p. 502.
60. Willson, C.G., *Introduction to Microlithography*. 2 ed, ed. C.G.W. L. F. Thomson, and M. J. Bowden. 1994, Washington, DC: American Chemical Society. 198.
61. M. A. McCord, M.J.R., *Handbook of Microlithography, Micromachining, and Microfabrication*, ed. P. Rai-Choudhury. Vol. 1. 1997, WA: SPIE Optical Engineering Press. 208.
62. L. F. Thomson, J.P.B., E. D. Feit, J. Vac. Sci. Technol., 1975. **B 12**(6): p. 1280.
63. M. A. McCord, M.J.R., *Handbook of Microlithography, Micromachining, and Microfabrication*, ed. P. Rai-Choudhury. 1997, WA: SPIE Optical Engineering Press. 213.
64. E. A. Dobisz, C.R.K.M., Appl. Phys. Lett., 1991. **58**(22): p. 3.
65. Chang, T.H.P., J. Vac. Sci. Technol., 1975. **B 12**: p. 1271.
66. Kratschmer, E., J. Vac. Sci. Technol., 1975. **B 12**: p. 1271.
67. Kratschmer, E., J. Vac. Sci. Technol., 1981. **B 19**: p. 1264.
68. Murata, K., J. Appl. Phys., 1974. **45**(9): p. 4110.
69. Thomson, M.G.R., J. Vac. Sci. Technol., 1993. **B 11**: p. 2768.
70. M. A. McCord, M.J.R., *Handbook of Microlithography, Micromachining, and Microfabrication*, ed. P. Rai-Choudhury. Vol. 1. 1997, WA: SPIE Optical Engineering Press. 159.
71. Seiler, H., J. Appl. Phys., 1983. **54**: p. R1.
72. S. Y. Lee, B.D.C., IEEE Trans. Semiconductor Manufacturing, 1998. **11**: p. 108.
73. E. Seo, B.K.C., O. Kim, Microelectron. Eng., 2000. **53**: p. 305.
74. M. Osawa, K.T., M. Sato, H. Arimoto, J. Vac. Sci. Technol., 2001. **B 19**: p. 2483.
75. S. Aya, K.K., H, Yabe, K. Marumoto, Jpn. J. Appl. Phys., 1996. **35**: p. 1929.
76. X. Huang, G.B., G. H. Bernstein, J. Vac. Sci. Technol., 1993. **B 11**: p. 2565.
77. S. J. Wind, M.G.R., G. Pepper, W. W. Molzen, P. D. Gerber, J. Vac. Sci. Technol., 1989. **B 7**: p. 1507.

78. M. A. McCord, M.J.R., *Handbook of Microlithography, Micromachining, and Microfabrication*, ed. P. Rai-Choudhury. Vol. 1. 1997, WA: SPIE Optical Engineering Press. 163.
79. Owen, G., J. Vac. Sci. Technol., 1990. **B 8**: p. 1889.
80. Owen, G., J. Appl. Phys., 1983. **54**: p. 3575.
81. S. Y. Lee, F.H., J. Ji, , J. Vac. Sci. Technol., 2004. **B 22**: p. 2929.
82. L. J. Lauchlan, D.N., N. Sullivan, *Handbook of Microlithography, Micromachining, and Microfabrication*, ed. P. Rai-Choudhury. Vol. 1. 1997: SPIE Optical Engineering Press. 477.
83. L. J. Lauchlan, D.N., N. Sullivan, *Handbook of Microlithography, Micromachining, and Microfabrication*, ed. P. Rai-Choudhury. Vol. 1. 1997: SPIE Optical Engineering Press. 496.
84. M. Adel, M.G., B. Golovanevsky, P. Izikson, E. Kassel, D. Yaffe, A. M. Bruckstein, R. Goldenberg, Y. Rubner, M. Rudzsky, IEEE Trans. Semiconductor Manufacturing, 2004. **17**: p. 166.
85. L. J. Lauchlan, D.N., N. Sullivan, *Handbook of Microlithography, Micromachining, and Microfabrication*, ed. P. Rai-Choudhury. Vol. 1. 1997: SPIE Optical Engineering Press. 498.
86. *Specification for Overlay Capabilities of Wafer Steppers*, SEMI. p. 18-92.
87. Starikov, A., *Handbook of Silicon Semiconductor Metrology*, ed. A.C. Diebold. 2001: Marcel Deckker, Inc. 414.
88. L. J. Lauchlan, D.N., N. Sullivan, *Handbook of Microlithography, Micromachining, and Microfabrication*, ed. P. Rai-Choudhury. Vol. 1. 1997: SPIE Optical Engineering Press. 525.
89. Starikov, A., *Handbook of Silicon Semiconductor Metrology*, ed. A.C. Diebold. 2001: Marcel Deckker, Inc. 461.
90. K. Hoshi, E.K., H. Morohoshi, H. Ina, T. Fujimura, H. Kurita , J. L. Seligson, *TIS-WIS Interaction Characterization on Overlay Measurement Tool.* proc, SPIE, 2002. **4689**: p. 715.
91. L. J. Lauchlan, D.N., N. Sullivan, *Handbook of Microlithography, Micromachining, and Microfabrication*, ed. B. P. Rai-Choudhury. Vol. 1. 1997: SPIE Optical Engineering Press. 500.
92. L. J. Lauchlan, D.N., N. Sullivan, *Handbook of Microlithography, Micromachining, and Microfabrication*, ed. P. Rai-Choudhury. Vol. 1. 1997: SPIE

Optical Engineering Press. 510.

93. S. S. H. Naqvi, R.H.K., J. R. McNeil, J. Opt. Soc. Am, 1994. **11**: p. 2485.

94. L. J. Lauchlan, D.N., N. Sullivan, *Handbook of Microlithography, Micromachining, and Microfabrication*, ed. P. Rai-Choudhury. Vol. 1. 1997: SPIE Optical Engineering Press. 528.

95. D. V Gorelikov, J.R., N. T. Sullivan, *CD-SEM-based Critical Shape Metrology of integrated circuits.* proc, SPIE, 2004. **5375**: p. 1.

96. *Specification for metrology pattern cells for integrated circuit manufacture*. 1996, SEMI. p. 19-92.

97. N. G. Orji, T.V.V., J. Fu, R. G. Dixon, C. V. Nguyen, J, Raja, Meas. Sci. Technol, 2005. **16**: p. 2147.

98. M. G. Moharam, T.K.G., G. T. Sincerbox, H. Whrlich, B. Yung, Appl. OPT, 1984. **23**: p. 3214.

99. H. M. Marchman, J.E.G., *Handbook of Silicon Semiconductor Metrology*, ed. A.C. Diebold. 2001: Marcel Deckker, Inc. 335.

100. M. T. Postek, A.E.V., *Handbook of Silicon Semiconductor Metrology*, ed. A.C. Diebold. 2001: Marcel Deckker, Inc. 303.

101. Y. Martin, H.K.W., J. Vac. Sci. Technol., 2005. **B 13**: p. 2335.

102. Y. Martin, H.K.W., Appl. Phys. Lett., 1994. **64**: p. 2498.

103. Raymond, D.J., *Handbook of Silicon Semiconductor Metrology*, ed. A.C. Diebold. 2001: Marcel Deckker, Inc. 478.

104. A. Hettwer, N.B., C Schneider, L Pfitzner, H. Ryssel, IEEE Trans. Semiconductor Manufacturing, 2002. **15**: p. 470.

105. Spector, S.J., in *Department of Physics*. 1997, State University of New York: stony brook.

106. A. Ozawa, T.T., T. Ishii, H. Yoshihara, and T. Kagoshima, Microelectronic Engineering, 1997. **35**: p. 525.

107. W. J. Lin, W.C.C., J. Electrochem. Soc., 2001. **148**(11): p. G620.

108. S. A. Bulgakova, A.Y.L., V. I. Luchin, L. M. Mazanova, S. A. Molodnjakove, N. N. Salashchenko, Nuclear Instruments and Methods in Physics Research, 2000. **A 448**(487).

109. H. Namatsu, M.N., T. Yamahuch, K. Yamazaki, K. Kurihara, J. Vac. Sci. Technol., 1998. **B 16**(6): p. 3315.

110. M. J. Loboda, C.M.G., and R. F. Schneider, J. Electrochem. Soc., 1998. **145**(8): p.

2861.

111. C. C. Yang, W.C.C., J. Mater. Chem., 2002. **12**: p. 1138.
112. A. A. Ehsan, S.S.a.B.Y.M., ICES2000 Proc., 2000: p. 228.
113. Ross, P.J., *Taguchi Techniques for Quality Enginnering*. 1996, New York: McGraw-Hill.
114. Zarowin, C.B., J. Vac. Sci. Technol., 1984. **A 2**(4): p. 1537.
115. Y. Catherine, a.P.C., Thin Solid Films, 1986. **144**: p. 265.
116. d'Agostino, R., J. Appl. Phys., 1981. **52**(1): p. 162.
117. Voshchenkov, A.M., J. Vac. Sci. Technol., 1993. **A 11**(4): p. 1211.
118. Flamm, D.L., Pure & Appl. Chem., 1990. **62**(9): p. 1709.
119. Harada, K., J. Appl. Polymer. Sci., 1981. **26**: p. 1961.
120. Y. G. Yingling, a.B.J.G., J. Phys. Chem, 2005. **109**: p. 16482.
121. D. C. Joy, J.J.H., Proc, SPIE, 2000. **3998**: p. 108.
122. Joy, D.C., J. Microscopy, 2002. **208**: p. 24.
123. *NIH IMAGE can be downloaded from http://rsb.info.nih/nih-image*.
124. *SCION IMAGE is an authorized port of NIH IMAGE for Windows and can be downloaded from http://www.scioncorp.com*.
125. D. C. Joy, C.S.J.a.R.D.B., scanning, 1996. **18**: p. 33.
126. *IMAGE JAVA can be downloaded from http://rsb.info.nih.gov/ij*.
127. S. J. Erasmus, D.M.H., K. C. A. Smith, Inst. Phys. Conf. Ser., 1980. **52**: p. 73.
128. J. Frank, P.B., R. Langer and W. Hoppe, Phys. Chem, 1970. **74**: p. 1105.

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