5-2007

Modular DC-DC Converters

Faisal Habib Khan
University of Tennessee - Knoxville

To the Graduate Council:

I am submitting herewith a dissertation written by Faisal Habib Khan entitled "Modular DC-DC Converters." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

Leon M. Tolbert, Major Professor

We have read this dissertation and recommend its acceptance:

Jack S. Lawler, Fangxing Li, Tsewei Wang

Accepted for the Council:
Dixie L. Thompson

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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MODULAR DC-DC CONVERTERS

A Dissertation
Presented for the
Doctor of Philosophy Degree
The University of Tennessee, Knoxville

Faisal Habib Khan
May 2007

DEDICATION

To my wife

Nadiah Khan

my mother

Ferdous Ara Khan

and my sister

Habiba Khan

ACKNOWLEDGMENTS

During the past four years I was in UT, I have come across many helpful faculties, friends, colleagues, and classmates. Down the road, they gave me motivations, offered inspirations, intellectual support and pleasant company in many events. I am especially grateful to my advisor Dr. Leon Tolbert to offer me a nice opportunity to do my research in the field I preferred most. I am very much influenced and benefited from his method of conducting research, teaching and mentoring style.

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ABSTRACT

DC-DC converter is one of the mostly used power electronic circuits, and it has applications in various areas ranging from portable devices to aircraft power system. Various topologies of dc-dc converters are suitable for different applications. In high power applications such as the bi-directional dc-dc converter for dual bus system in new generation automobiles, several topologies can be considered as a potential candidate. Regardless of the topology used for this application, the reliability of the converter can be greatly enhanced by introducing redundancy of some degree into the system. Using redundancy, uninterrupted operation of the circuit may be ensured when a fault has occurred.

The redundancy feature can be obtained by paralleling multiple converters or using a single modular circuit that can achieve this attribute. Thus, a modular dc-dc converter with redundancy is expected to increase the reliability and reduce the system cost. Recently, the advancement in power electronics research has extended its applications in hybrid electric automobiles. Several key requirements of this application are reliable, robust, and high efficiency operation at low cost. In general, the efficiency and reliability of a power electronic circuit greatly depend on the kind of circuit topology used in any application. This is one of the biggest motivations for the researchers to invent new power electronic circuit topologies that will have significant impact in future automobile industry.

This dissertation reviews existing modularity in power electronic circuits, and presents a new modular capacitor clamped dc-dc converter design that has many potential

uses in future automotive power system. This converter has multilevel operation, and it is capable of handling bi-directional power. Moreover, the modular nature of the converter can achieve redundancy in the system, and thereby, the reliability can be enhanced to a great extent. The circuit has a high operating efficiency (>95%), and it is possible to integrate multiple voltage sources and loads at the same time. Thus, the converter could be considered as a combination of a power electronic converter and a power management system.

In addition to the new dc-dc converter topology, a new pair of modular blocks defined as switching cells is presented in this dissertation. This pair of switching cells can be used to analyze many power electronic circuits, and some new designs can be formed using those switching cells in various combinations. Using these switching cells, many power electronic circuits can be made modular, and the modeling and analysis become easier.

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CHAPTER 1

INTRODUCTION

The modularity in power electronic circuits is becoming a very important issue in power electronics research. Unlike digital circuits, power electronic circuits are not usually modular, and this is why redundancy in power electronic circuits is not very common. Using modularity, it is possible to simplify the analysis of many power electronic circuits and additional improvements such as better efficiency or elevated performance can be obtained in an easier way. The purpose of this dissertation work is to introduce some modularity in power electronic dc-dc converters and some fundamental modular blocks that are the foundation of these modular topologies.

Some of the advantages of a modular circuit are reduced design cost, redundancy, and "hot swap" feature. The "hot swap" feature allows the user to remove any faulty module and replace it with a good one in a few easy steps. Moreover, there could be some intelligence in the control circuit, so that any module can be bypassed if it experiences any malfunction; and thus an uninterrupted operation can be confirmed. In addition, the modular nature of the some converters exhibits the advantage to stack multiple modules to increase the power rating of the converter. The modular nature of any converter also simplifies the behavioral analysis of the converter, and in some cases, new circuit topologies can be found by simply connecting multiple modules in various combinations.

The introduction of canonical switching cell in 1970's by Landsman [1] was the first modular structure in power electronic circuits. An inductor, a capacitor, and a single pole double throw switch forms a canonical switching cell. Later on, several modules have been presented, proposed, and successfully used in power electronic circuits. These modular blocks have significantly reduced the modeling and analysis complexity, and have allowed the designers to achieve additional functionalities such as reduced electromagnetic interference (EMI) and improved ripple performance in many converters. Although many modular blocks have been presented, the introduction of new modular units in power electronic circuits could simplify the analysis methods. This dissertation will introduce a family of modular units named as basic switching cells and their possible applications in power electronic circuits.

The recent development in hybrid automobile industry has created a massive requirement for many power electronic converters. The recent development in power electronics research has created a trend of using plenty of electronic appliances (essential and luxury components) in present and future automobiles [2][3]. In [2][3], it was shown that there will be a big demand of power for the dc appliances in future automobiles, and the standard 14 V bus will not be suitable to supply the power requirements for those dc loads. In this continuation, a 42V/14V bus system named as "42V PowerNet" was proposed [2] several years ago. In this system, there will be two voltage buses in the electrical system of a vehicle. Some electrical loads will be connected to the 42 V bus, and the existing electrical loads will remain connected to the 14 V bus. This system might have one or two sets of batteries; one for 14 V and one for 42 V bus. In both cases, there

will be a bi-directional converter that can manage power flow between the two voltage buses. In this way, loads connected at the 42 V bus can be powered from the battery connected on the same bus or from the 14 V bus. This is also true for the loads connected at the 14 V bus.

The development of a compact, high efficiency dc-dc converter can introduce several modifications to the overall automobile design. The overall performance of the bi-directional dc-dc converter will decide if the 42V/14V dual bus system will be a successful and cost effective solution for the future automobiles. Especially in automotive applications where high ambient temperature (~200°C) is present, conventional dc-dc converters with magnetic elements can be very inefficient, and dc-dc converters with bulky inductors can suffer from limited space issue. The other criterion that needs to be fulfilled from this bi-directional converter is high efficiency even in partial loads. It is a well known fact that classical dc-dc converters suffer from limited efficiency at partial loads, and the maximum efficiency is achieved at full load. Thereby, a new dc-dc converter having an operating principle other than the inductive energy transfer method could be advantageous. Several capacitor clamped converters can be considered as a solution to meet this criteria to achieve high efficiency operation and bi-directional power handling capability. The detail of this bi-directional power transfer feature will be discussed in the later sections.

Bi-directional power management is an important attribute of a dc-dc converter used in several applications. In a hybrid automobile, there are many electrical loads grouped into two main categories depending on the voltages they use. The main traction

motor is powered from the high voltage bus (around 500 V). There are also low voltage loads that need to be powered from a low voltage source in the range of 40-50 V. The low voltage source could be a battery or a stepped down voltage from the high voltage battery pack or any source. When the high voltage source is a fuel cell, the low voltage source must be a battery pack. During the start up time of the vehicle, the low voltage battery pack delivers power to the fuel cell system and to the main motor, and the low voltage loads in the vehicle [4]. This time, the dc-dc converter delivers power from the low voltage source to the high voltage bus and loads, and works in the up conversion mode. Once the fuel cell is ready, it starts providing power to the main motor, and low voltage loads. The low voltage battery is also charged from the fuel cell if required. During this time, the dc-dc converter works in the down conversion mode. Thus, a dc-dc converter used in the system must have the capability to deliver power in both directions depending on the state of the fuel cell or the low side battery voltage. A block diagram of this operation is shown in Figure 1-1.

There are many reported methods of constructing bi-directional dc-dc converters. The classical buck converter can be made as a bi-directional converter by replacing the free wheeling diode with an active switch, and a considerably higher efficiency can be achieved from the buck converter [5][6]. However, this classical circuit has several limitations that may prevent it from being used in automotive applications. For a buck converter with high conversion ratio, the main active switch can be a metal oxide semiconductor field effect transistor (MOSFET) or an insulated gate bi-polar transistor (IGBT), and the switch experiences a high voltage stress; which is as high as the highest

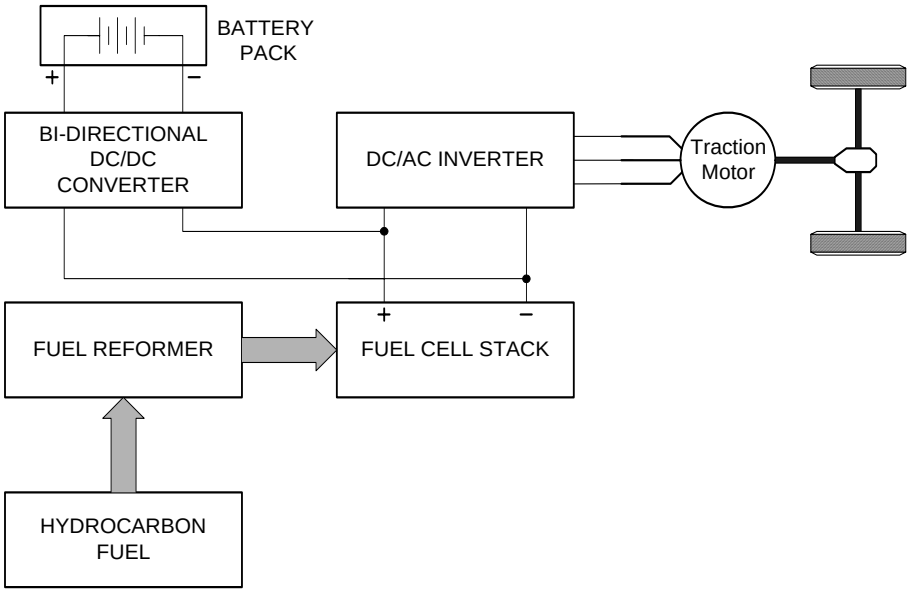


Figure 1-1. Typical topological arrangement of a hybrid fuel cell vehicle drive train [4].

voltage present in the circuit. Moreover, the entire power of the converter is controlled by this single device. When the power rating of the converter is high, it becomes difficult to find one suitable switch to handle the total power. The solution to this problem would be using paralleled switches to split the total current among the switches. In the same way, multiple transistors can be connected in series to reduce the voltage stress across one single transistor. However, the use of multiple transistors connected in either series or parallel introduces several additional costs including complicated gate drive circuits. This solution has some other limitations too.

When multiple transistors are connected in parallel, the choice of transistor becomes limited because of the inherent properties of a transistor. For dc-dc converters, the choice for a transistor would be either MOSFET or IGBT. MOSFETs can be easily connected in parallel to enhance current carrying capability, and MOSFETs connected in

parallel have natural current sharing characteristics. However, MOSFETs are usually available to work in moderate voltage range (~ 1 kV), and to increase the voltage rating, they need to be connected in series. At that point, the biggest issue is to confirm equal voltage stress across all the series connected MOSFETs, otherwise some MOSFETs in the series path will experience more voltage stress than others; and they may get into voltage breakdown.

IGBTs have an inherent property to withstand higher breakdown voltages (standard is 1200 V). So, for high voltage applications, series connection of IGBTs can be avoided up to an operating voltage of several kilovolts. However, the current sharing property of an IGBT is not as good as a MOSFET to connect them in parallel to increase the current handling capability, and a thermal runway may occur in IGBTs connected in parallel. Moreover, IGBTs are not designed to operate at very high frequency, and they operate at a frequency which is always less than the maximum operating frequency of a MOSFET having the same voltage and current ratings. To miniaturize the passive components in a dc-dc converter, the common trend is to make the operating frequency high, and thereby, it can achieve a smaller ripple voltage at the output. For this reason, the use of IGBTs is not the best choice in dc-dc converters with high operating frequency. For the same reason, a circuit using MOSFETs could be the optimum solution provided an individual MOSFET does not experience very high breakdown voltage, and the MOSFETs are not connected in series. In this way, the additional cost for the complicated gate drive circuit can be avoided, and an unequal voltage stress thereby the voltage breakdown can be bypassed.

It was already mentioned that classical dc-dc converters that are based on inductive energy transfer are not very efficient at higher temperatures, and transistors used in those circuits experience high voltage stresses. To find an alternative solution, dc-dc converters based on capacitive energy transfer were proposed to be an optimum solution for this application [7]. This circuit is known as the capacitor clamped converter, and the specialty of this circuit is the reduced voltage and current stress across individual transistors used in the circuit. The inherent nature of this topology employs multiple transistors to establish a capacitive energy transfer protocol, and the power rating of the converter is distributed among the transistors used in the circuit [7]. Another great feature of this converter topology is the inductor free operation, and this feature can be used to design a compact, high efficiency converter. Using high temperature capacitors, the circuit can be operated at relatively high ambient temperature.

There are some other dc-dc converters based on capacitive energy transfer. However, all of these converters fall into the group named as switched-capacitor circuit. The flying capacitor converter and series-parallel converter are the other examples of switched capacitor circuits. All the existing switched capacitor circuits suffer from one major limitation. They are not modular, and several features such as redundancy and fault bypass operation cannot be utilized from these topologies. In addition, most of the existing topologies of switched-capacitor circuits do not have a complete bi-directional power handling capability; although, some circuits such as the capacitor clamped circuit [7] exhibit a limited bi-directional power controlling feature. Thus, the dc-dc converter that will be used for the automotive application should have a new topology, and it

should have several advantageous features such as inductor free design, modular, bi-directional power handling and high efficiency operation. Unfortunately, all these criteria cannot be fulfilled using an existing topology, and this is the biggest motivation to develop a new circuit topology.

In this dissertation, a new capacitor clamped multilevel dc-dc converter is proposed, and its various features are demonstrated with experimental results. Previously discussed modularity feature will be used here to find the new modular topology. This added feature is expected to enhance the flexibility of changing the number of levels leading to changing conversion ratio, redundancy, and fault bypass capability. If there is any fault in the converter, it can be localized to a specific module, and later on, the module can be bypassed to ensure an uninterrupted operation. This modular feature may also facilitate the bi-directional power management capability of the converter. The proposed multilevel modular capacitor clamped dc-dc converter (MMCCC) [8] is enriched by many advantageous features such as complete modular structure, bi-directional power handling capability, module redundancy, fault bypassing capability, and multiple load-source integration capability. The modular construction of the MMCCC topology will have intermediate voltage nodes between two adjacent modules, and it allows a system to integrate multiple sources and loads simultaneously, and the converter can be considered as a dc transformer having multiple taps. Thus, a complete power management system can be established having various kinds of loads and sources.

In Chapter 2, the literature survey for existing modularity in power electronic circuits and circuit modules will be presented. The background search for multilevel dc-

dc converters, switched-capacitor or charge pump circuits will be presented in Chapter 3. The construction and attributes of the basic switching cells will be presented in Chapter 4, and the MMCCC circuit will be presented in Chapter 5, where the new topology will be compared with an existing topology with the help of several simulation and experimental results. Chapter 6 will present the analytical modeling of the MMCCC converter, and it will explain the startup and steady state operations with the help of voltage and current equations. As the final step of proof of concept, Chapter 7 will include the experimental results and several key features of the MMCCC converter. In continuation of this work, some future works will be referenced in Chapter 8.

CHAPTER 2

EXISTING MODULAR CONCEPTS

The introduction of modularity in power electronic circuits started with defining some cell structures. The use of those cell structures introduced some new circuit modeling techniques. With the use of these basic cells, it became possible to improvise existing circuit topologies. When any circuit is modeled with these cell structures, new insights of the topology can be revealed, and other new topologies can be found. Several dc-dc converter modeling and analysis procedures have been reported, and many of them include several cell structures as the basic unit of the converter circuit. The present discussion will arrange various cell structures that were reported in the past years in power electronic circuits. After this reviewing step, a new switching cell structure will be presented in chapter 3 along with its features and possible applications in power electronic circuits.

2.1 THE CANONICAL CELL

The canonical cell is the first fundamental switching cell to synthesize PWM dc-dc converters. It was first introduced in [1], and later on, it was used in many literatures [9] – [11], and considered as the fundamental block of dc-dc converters. A canonical switching cell is used to make a relationship among the three converters (up converter, down converter and up-down converter), and the derivation of the voltage control relationships were explained in many literatures. A canonical cell is a three

terminal device where an inductor, a capacitor, and a single-pole double throw switch form a basic canonical switching cell shown in Figure 2-1(a). The cell has three terminals A, B, and C, and each of them can be used as an input/output/common terminal. If terminal A is used as an input, B as an output and C is used as the common terminal, the canonical circuit forms one kind of dc-dc converter. Six different combinations can be formed by changing the function of the three terminals in various combinations [11]. Among these six combinations, only three distinct effective circuits are found, whereas the others are functionally the same. Thus, using these three combinations, the buck, boost, and buck-boost converter can be formed.

2.2 THE ADVANCED CANONICAL CELL

The traditional canonical cell can be modified by using two capacitors. The literature presented in [9] introduces the modified canonical cell shown in Figure 2-1(b),

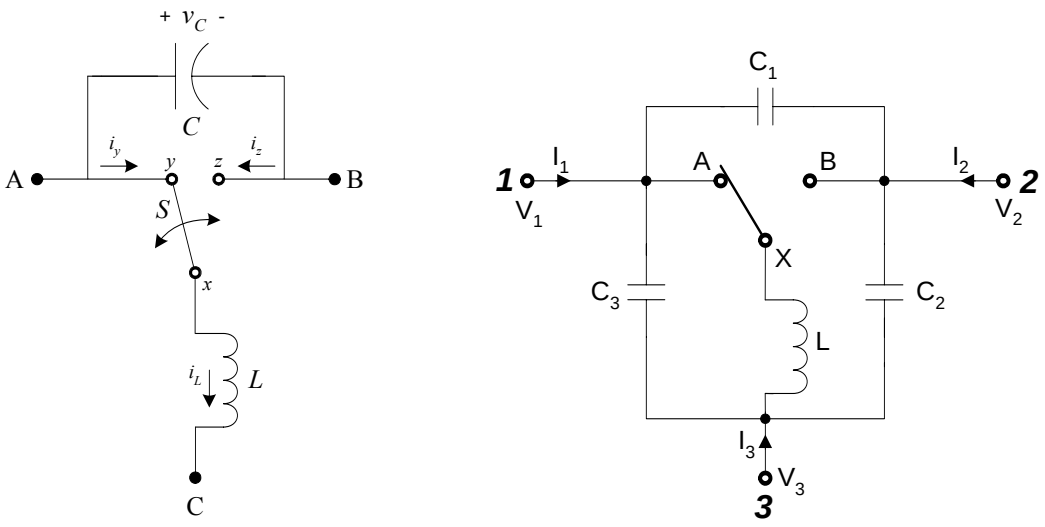


Figure 2-1. Schematic of the a) basic canonical cell, b) modified canonical cell.

and it discusses the effect of high frequency operation of the new converters built from this modified cell. When the switching frequency is high, [9] suggests that better performance can be obtained from the modified circuit. The three terminals in the circuit can be configured in many different ways. When terminal 1 or 2 is grounded and terminal 3 is configured as the output, there exists a direct path from the input to the output of the converter. This is defined as a direct converter. If terminal 3 is grounded, then there exists no direct path in between the input and output, and the converter is defined as an indirect converter. This step-down converter built from the canonical cell is a special form of the well-known chopper circuit where there is an additional low pass filter circuit at the output. The circuit can be operated in continuous or discontinuous conduction mode.

According to [1], it can be shown that the up converter and the down converter are special cases of the generalized bi-directional converter [10]. Even for the generalized topology, terminal 1 stays at higher potential than terminal 2. A transformation method was shown in [1] that leads a way to convert the isolated Ćuk converter into the buck-boost converter. The isolated version of the Ćuk converter with turn ratio 1:1 is shown in Figure 2-2. By reorganizing the isolation transformer, it can be made redundant, and the isolated version of the Ćuk converter can be converted into the classical buck-boost converter.

2.3 ANALYSIS USING h AND g PARAMETERS

The classical converters can be grouped into two major converter families - buck converter and boost converter [12]. The buck family converters' small signal models can

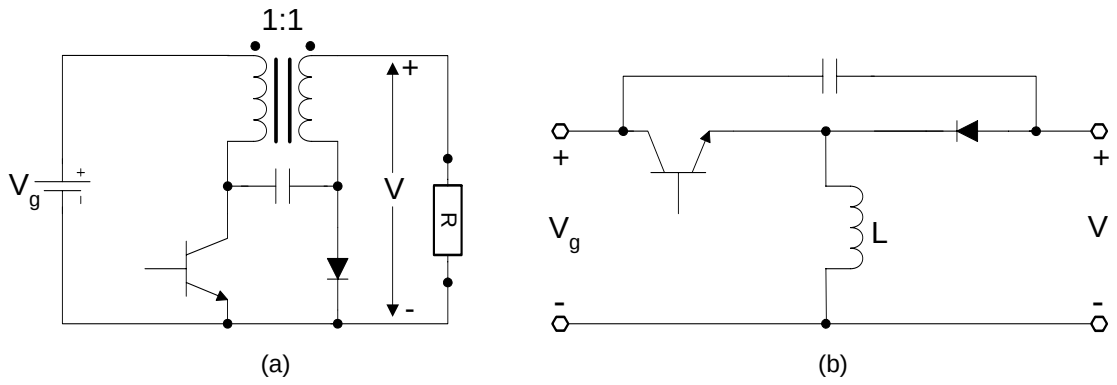


Figure 2-2. (a) The isolated Ćuk converter, (b) the conventional buck-boost converter.

be expressed in terms of h-parameters and those for the boost families are defined by g-parameters. When a unity feedback is applied in the buck converter, the buck-boost converter is formed, and this is shown in Figure 2-3. In addition to the feedback unit, when a filter block is added to the buck converter, the Zeta converter is formed. The Sepic and Ćuk converter can be synthesized from the boost converter [12]. Thus, a common platform based on buck converter could be found where the buck-boost or Zeta converter can be re-constructed by manipulating the circuit. In the same way, a common platform using boost converter can be obtained to derive the Ćuk or Sepic converter.

2.4 ANALYSIS USING GRAFT SCHEME

Using the technique presented in [13], the classical PWM converters can be represented by only the buck and boost converter connected in cascaded arrangement, and the two-port network theory is applied. This paper presents a unified and systematic method to synthesize and model transformer-less PWM dc-dc converters. To do that, 4 different basic unit cells were presented where the cells are made from two transistors.

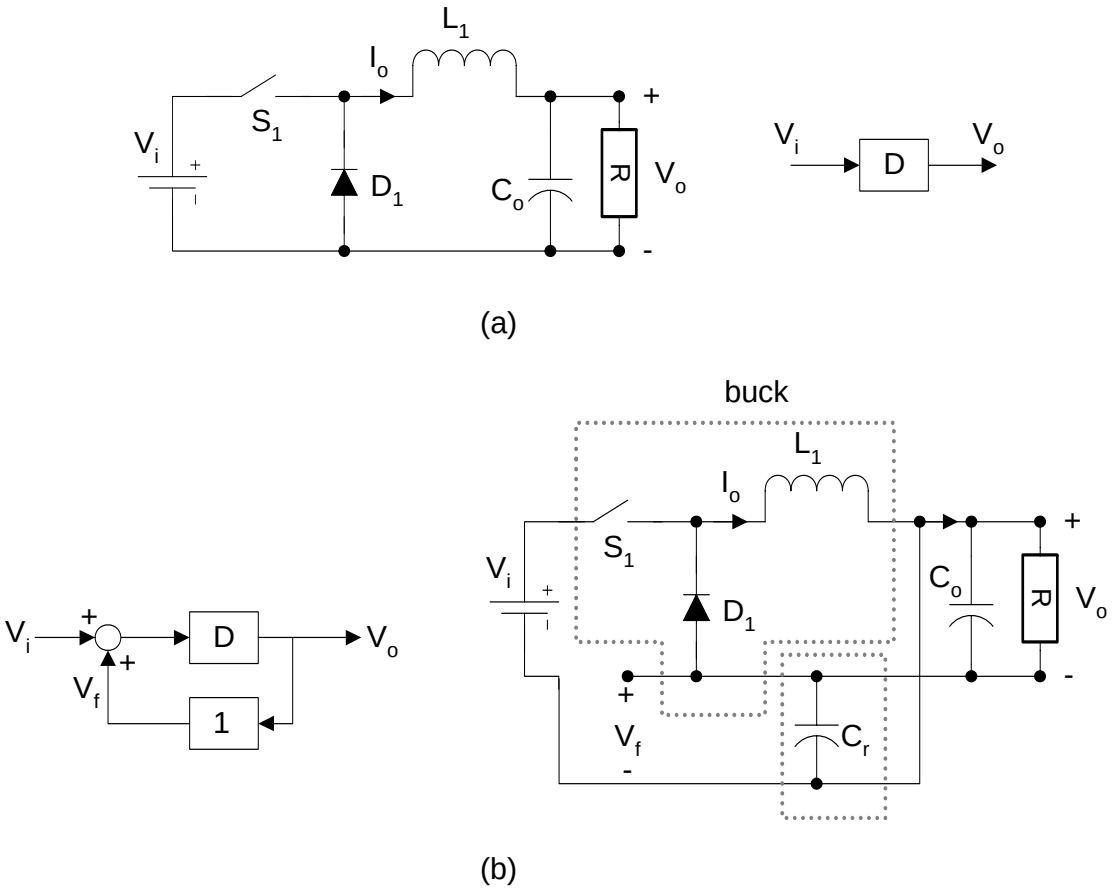


Figure 2- 3. Illustration of the buck-boost converter derived from buck converter. a) the buck converter and block diagram, b) the buck converter block diagram with feedback loop and the schematic of the block diagram; that is eventually a boost converter.

Then using the graft scheme, the diode-transistor realization of those 4 cells was derived.

Figure 2-4 shows the four cells and Figure 2-5 shows the grafted switching schemes. The basic purpose of this approach was to convert a two-stage converter into a single stage to simplify the model. To do that, a two-stage buck-boost circuit is formed, and a search is done for a pattern that matches with any of the four figures in Figure 2-4. Using the corresponding grafted switching scheme, the two-stage circuit is represented by grafted schemes only, and a simplification is made. In this way, the conventional single transistor buck-boost converter can be formed from two single stage circuits connected in cascaded fashion. The transformation process from a two-stage circuit to a one-stage circuit is shown in Figure 2-6. Using this method, it is also possible to deduce the small signal model of the converters.

2.5 THE UNIFYING APPROACH

The analysis presented in [14] and [15] summarize some other articles such as Landsman's [1], Erickson's [16], and Rao's [17] paper. The method presented in [14] and [15] creates a unifying connection among some converters which seem to be unrelated. It follows a similar approach like the Landsman's method to build some new dc-dc converters out of the canonical switching cell. In Rao's method [17], a four terminal switching cell was used where there was a transformer inside the cell. In contrast to Rao's work, Landsman's technique uses three terminal basic canonical switching cell as the building block.

The method synthesizes any converter into three major sections. The input source, converter cell, and the output sink circuit. A converter cell is a three terminal device that

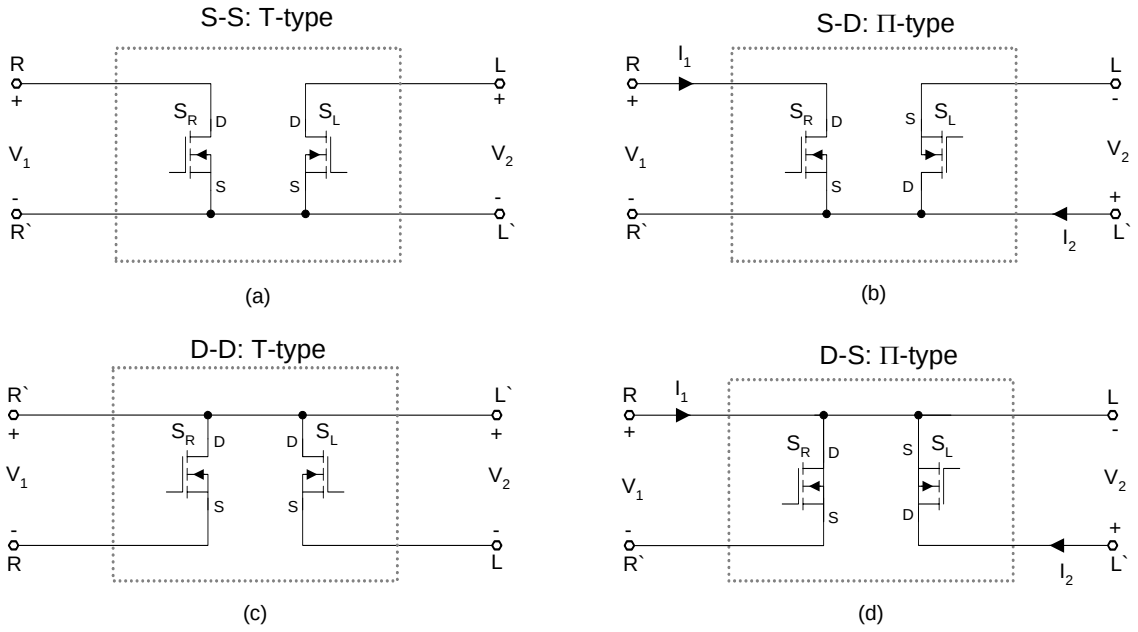


Figure 2-4. Illustration of the four possible common nodes and the orientation of the switches, a) S-S type, b) S-D type, c) D-D type, d) D-S type.

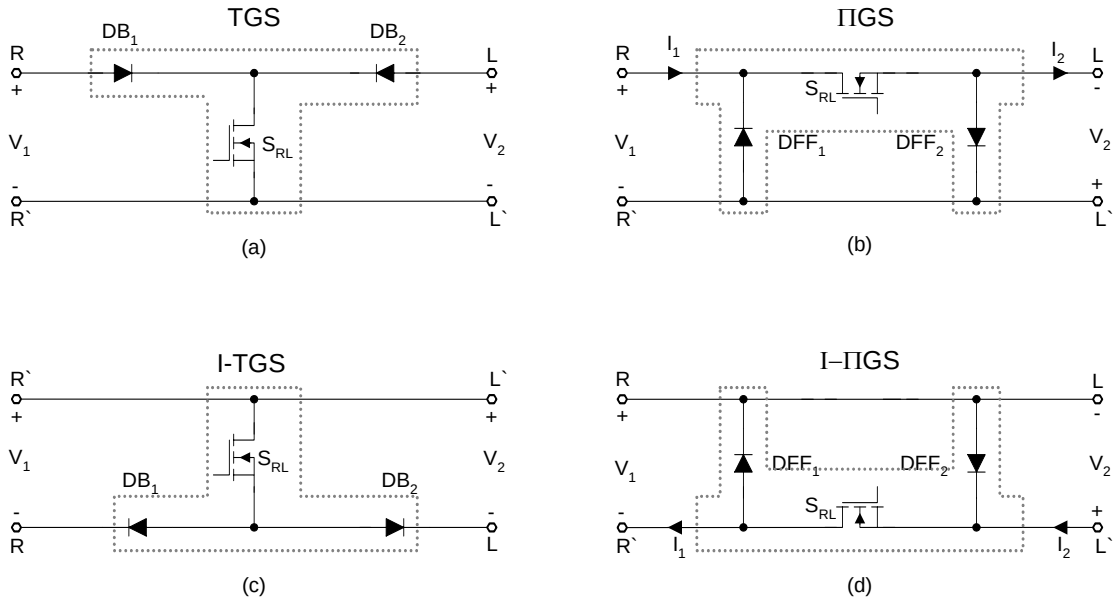


Figure 2-5. Grafted switching schemes, a) T-type grafted switch: TGS, b) Π-type grafted switch: ΠGS, c) inverted TGS: ITGS, d) inverted ΠGS: IΠGS.

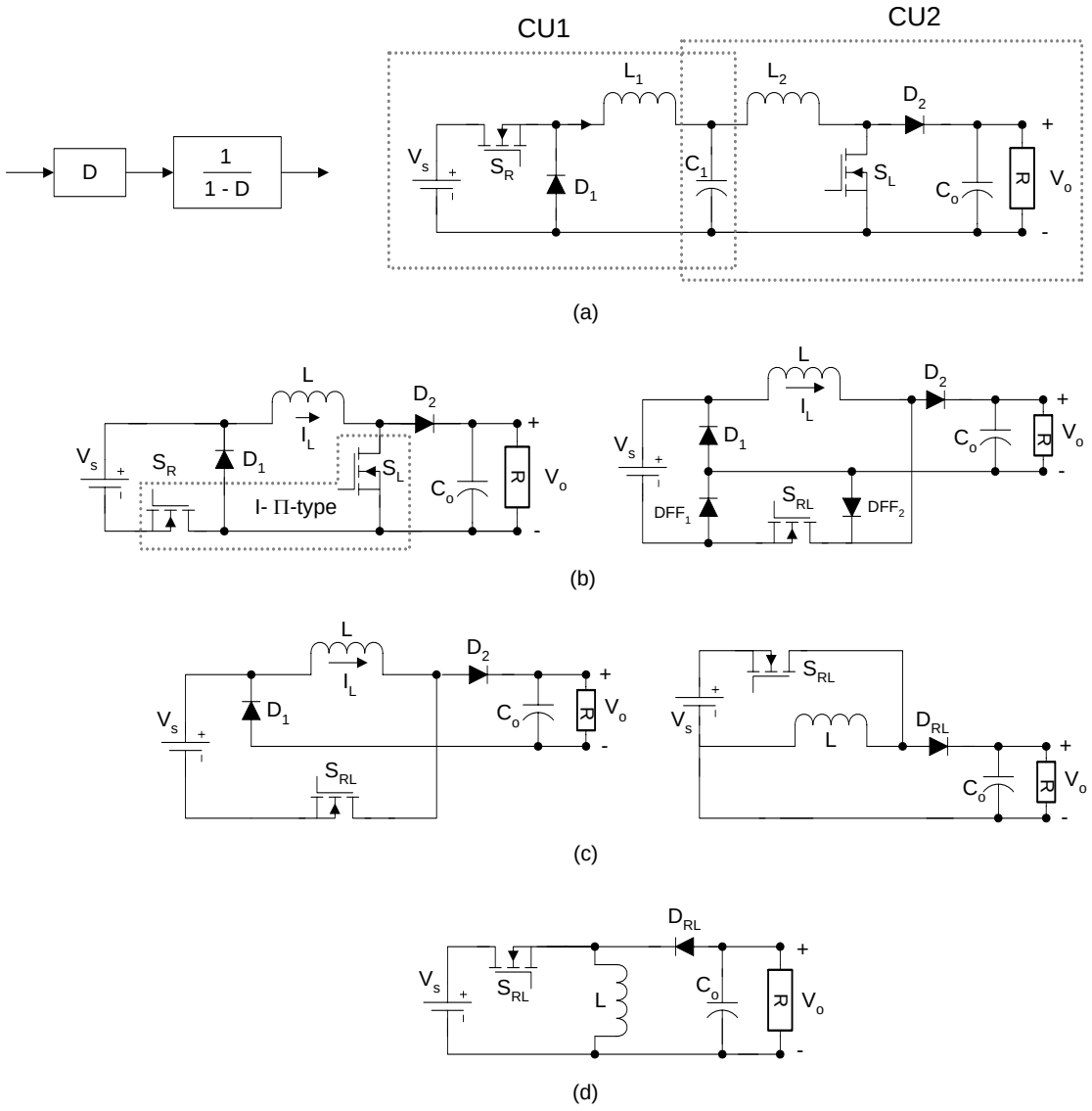


Figure 2-6. Illustration of the buck-boost single stage converter derived from two single stage buck and boost converters in cascade connection, a) buck (CU1) and boost converter (CU2) in cascade connection, b) finding the common nodes for 2-switch model and replacing them by graph switching cell, c) re-organizing and omitting the redundant diodes, d)the converter single-state buck-boost converter (conventional).

can be connected in six different ways. Due to the symmetry of the cell, only three configurations are possible. These configurations are shown in Figure 2-7. Of the two switches in a converter cell, the one which is controlled directly by the external control signal (gate drive) is considered as an active switch, and this is implemented by a three terminal device such as IGBT, MOSFET, or bi-polar junction transistor (BJT). The other switch in the circuit is not considered as an active switch, and it is controlled by the state of the active switch. This switch can be implemented by a diode.

It is possible to create many circuits out of this converter cell or from the combinational circuit of multiple cells. The conventional buck, boost, and buck-boost converters are considered to be in the same group, and this family is defined as first order 2-switch cell. However, the Ćuk converter does not fall into this group, rather it is considered to be one of the several third order two switch converter cells. Thus all the

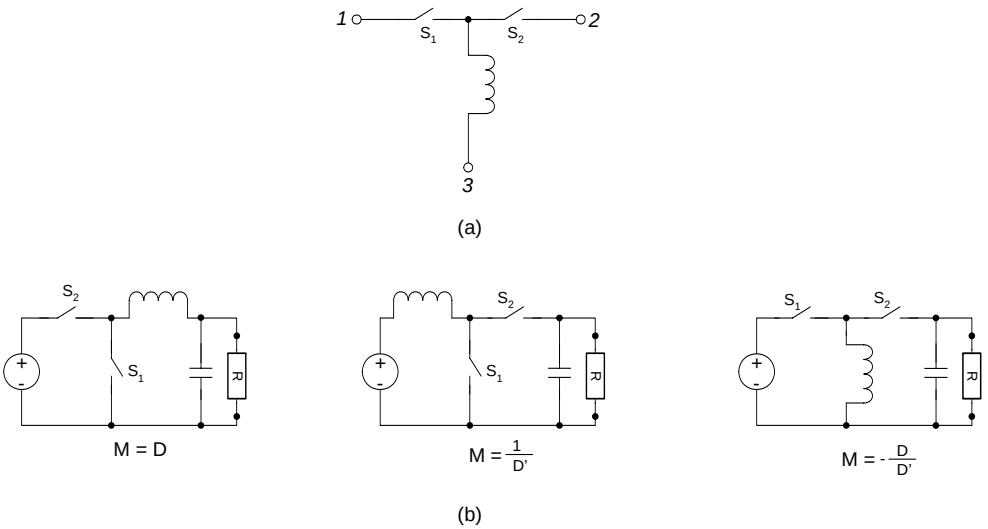


Figure 2-7. a) The switching cell, b) the 3 possible combinations of the ports of the switching cell.

different combinations can be grouped into 4 families such as, a) first order, 2 switch converter cell, b) first order, 4 switch converter cell, c) third order, 2 switch converter cell, d) third order, 4 switch converter cell.

The order of the cell depends upon the number of devices in the cell and their internal connection pattern. Thus when a capacitor is connected to a first order two switch cell, the order of the cell is raised to three. By virtue of the new converter circuits, it is possible to attain a very high down conversion ratio without a very small duty ratio. For some converters, a very large down conversion is possible by using a duty ratio close to 0.5.

There are several desired characteristics of any dc-dc converter such as two or four quadrant operation, ability to attain ripple free input/output current and so on. These requirements can lead to the invention of various dc-dc converters using basic building blocks. To obtain the desired characteristics, the cascade connection of two existing topologies could yield some promising results. The Ćuk converter was originally designed based on this method. New converters could be found even by a differential connection of two conventional converters.

According to the method presented in [16], the Sepic converter cannot be constructed from the conventional converters using the techniques stated in the previous section. However, this statement contradicts with the fact narrated in [12] where the author showed that introducing a feedback path in the conventional boost converter, one could obtain the Sepic converter. This paper introduces an analytical approach to derive every possible converter with desirable attributes. In this method, redundant cases will

occur when there are multiple ways to write the state equations for the same converter. Degenerate cases will occur when at least one capacitor voltage or inductor current is independent of the duty ratio of the converter. In the worst case, a degenerated case may appear in the circuit when the output voltage of the converter does not depend on the duty ratio. The elimination technique to reject the degenerated and redundant cases is also discussed in this paper.

The synthesis method proposed in [16] is based on writing state equations of the currents and voltages of any converter. However, all the transformations and operations cannot yield a complete set of basic converter topologies. In addition to it, for some specific combination of state equations, the method does not yield interesting topologies, and those were not discussed in this paper.

Both the buck and boost converters are simple in structure; however, they exhibit some undesirable attributes. The buck converter has discontinuous input current and the boost converter has discontinuous output current. This is even worse for buck-boost converter because none of the input/output currents are continuous for it. This is shown in Figure 2-8. Article [18] introduced a general unified approach to model switching-converter power stages. In addition to that, [19], [20] introduce a new topology to attain all the desirable properties of the conventional converters without obtaining the undesirable attributes of them. According to this paper, it can be shown that the buck-boost converter is a special form of the cascaded connection of a buck stage and a boost stage. Unfortunately it takes the undesirable attributes from both the converters. This is why, both the input and output current of a buck-boost converter is discontinuous.

The discontinuous input current causes the high electro magnetic interference (EMI) in the circuit, whereas the discontinuous (pulsed) output current is responsible for the higher output voltage ripple. According to this paper, all three basic converters can be constructed from the basic canonical cell. All of them can be generated by a cyclic rotation of the inductor/switch assembly. The same approach was presented in [14] and [16].

At first sight, the basic converters cannot be derived from each other, which contradicts to the other paper [12]. In this paper, a method was narrated to derive the buck-boost converter from the cascaded connection of the basic buck and boost converter which is shown in Figure 2-6. When a boost stage is connected after a buck stage in a cascaded fashion, a new converter is formed having two switches, two inductors and two capacitors. The effective load to the buck converter becomes $R_f = R/M^2$, where M is the dc gain of the boost stage, and R is the load resistance connected across the output of the boost stage.

Since the C_1 in Figure 2-6(a) does not alter the dc conditions, it can be omitted

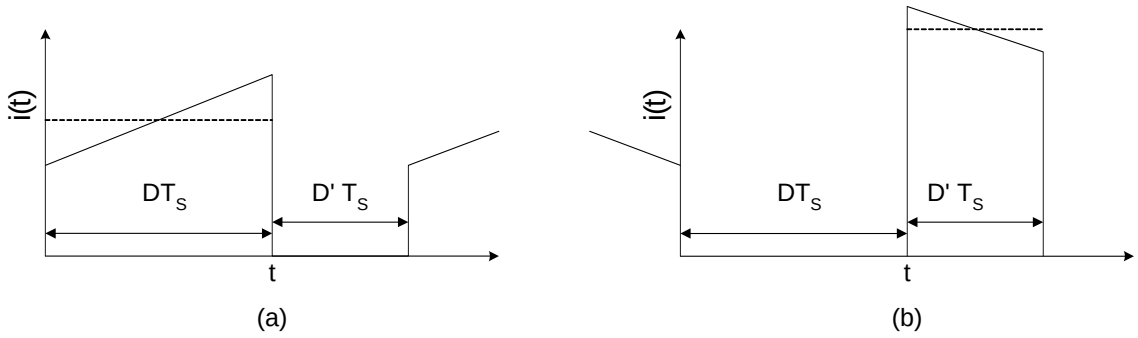


Figure 2-8. Current wave shapes of a buck-boost converter, a) input current, b) output current.

which results in the conventional circuit of the buck-boost converter. By eliminating C_1 and rearranging L_1 and L_2, the conventional buck-boost converter is formed. However, when this circuit is realized using one switch, the output gets inverted. Moreover, both the input and output current are discontinuous and a better converter is introduced in this paper, which will have continuous input and output current.

2.6 CONVERTERS WITH CAPACITIVE ENERGY STORAGE

Rather than a buck stage, when a boost stage is placed at the input, some dramatic changes take place in the circuit [19]. The circuit will have a continuous input current by virtue of the boost stage (a boost converter has continuous input current and discontinuous output current). The circuit will also achieve a continuous current at the output because of the buck stage (a buck converter has continuous output current and discontinuous input current). This new topology is shown in Figure 2-9. In conventional converters, the inductors work as the energy storage element. Now this circuit takes a shape where the capacitor C_1 is working as the energy-transferring element. When this capacitor is relocated and placed in a "floating" pattern, the circuit is simplified, and the circuit can be realized using only one active switch. The transformation procedure is shown in Figure 2-10, and the final circuit is shown in Figure 2-11.

Thus, a new converter is proposed by re-organizing the relative position of a Buck converter and a Boost converter inside a Buck-Boost converter. The new circuit will have all the desirable properties of Buck and Boost converters. Moreover, a capacitor is used as an energy transferring element rather than the inductors that is used in buck, boost or buck-boost converters.

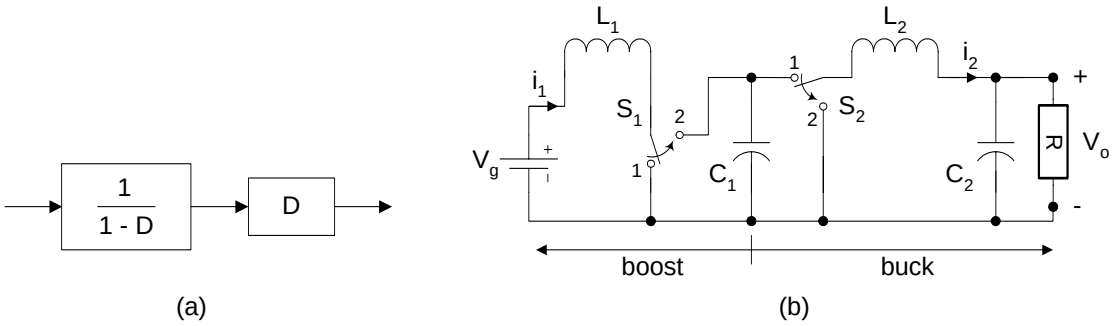


Figure 2-9. a) Block diagram of a boost power stage cascaded by a buck power stage, b) circuit realization of the block diagram.

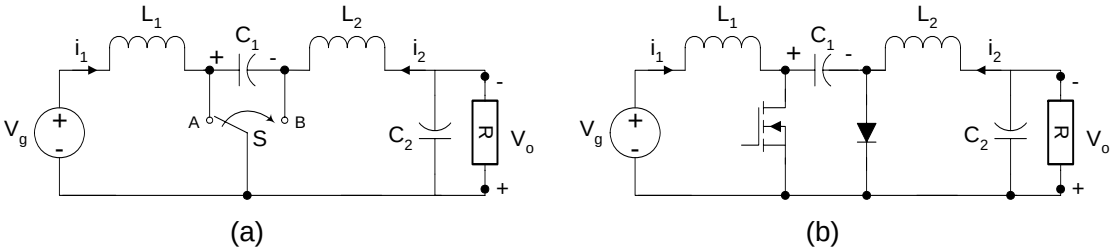


Figure 2-10. a) The new topology with capacitor energy transfer, b) the circuit realization with transistor and diode [06].

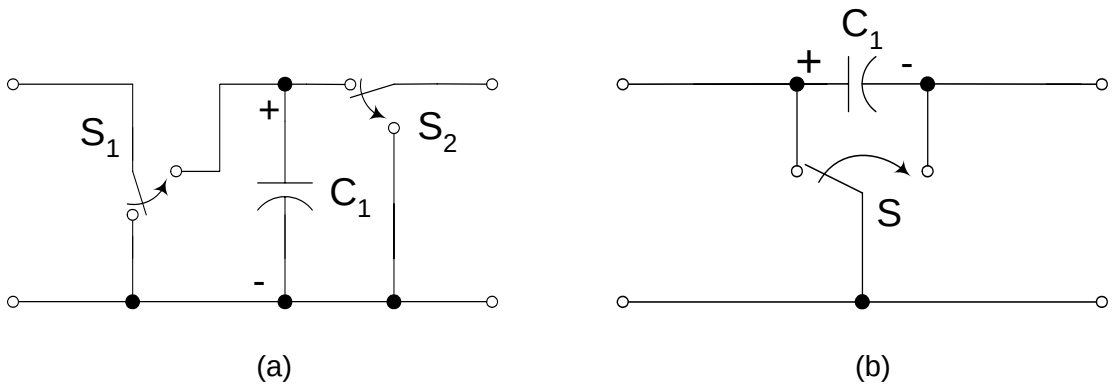


Figure 2-11. Topological reduction of the number of switches, a) two switches and non-inversion of capacitance voltage, b) single switch realization and inversion of capacitance voltage [6].

2.7 CHAPTER SUMMARY

Various circuit analysis and modeling methods have been summarized and some modular structures were presented in this section. Some methods use structured cells, and several of them use transformation techniques to deduce classical dc-dc converters from the buck and boost converter. Thus, it was felt that the commonly used dc-dc converters are related to each other and some unifying approach can establish this relationship. Moreover, the graft scheme or the canonical cell can be considered as the basic building block of a dc-dc converter circuit. In this continuation, chapter 4 will present a pair of basic switching cells each having only one transistor and one diode, and a method will be shown how classical converters can be made out of these basic switching cells. It will also explain how the classical converters are related to each other once they are expressed with the basic switching cells.

CHAPTER 3

EXISTING TOPOLOGIES OF MULTILEVEL AND SWITCHED-CAPACITOR DC-DC CONVERTERS

Multilevel dc-dc converter is becoming an indispensable element in some applications where high efficiency is a key factor. Along with the high efficiency, some converters can be made modular, and bi-directional power management can be established in the system. There are different topologies of multilevel dc-dc converters reported in the literature. Moreover, some switched-capacitor circuits with capacitive energy transfer topology can also claim to operate at very high efficiency. The present discussion will summarize several multilevel and switched-capacitor dc-dc converters that may have some similarities with the new converter presented in Chapter 5 of this thesis.

This chapter of the dissertation discusses the various features of the existing multilevel and switched-capacitor converters, their limitations, and the possible use of them in automotive applications with high power handling ability.

3.1 SERIES PARALLEL CONVERTER

The quest for a multilevel dc-dc converter was to achieve a circuit topology which can obtain high efficiency operation capability and magnetic element free (no inductor) design. The breakthrough was achieved by a series-parallel switched-capacitor converter that has only switching elements and capacitors [21] – [23]. Later on, these circuits were

presented in [24], [25] with some modified versions while comparing them with other topologies. Figure 3-1 shows a 3-level series parallel converter where V_{out} is 1/3 of V_{in}. To achieve this conversion ratio, three capacitors and a two-state switching scheme are used. During the first sub-interval, S_C, S_1 and S_2 are turned on, and all the capacitors are connected in series and get charged from V_{in}. During the other sub-interval, S_{1N}, S_{1P}, S_{2N}, and S_{2P} are turned on, and now all the capacitors are connected in parallel. During this sub-interval, all the capacitors are connected across the output load and get discharged to the output. The voltage conversion ratio is governed by the number of capacitors used in the circuit.

The operating principle of this topology is simple, and only two switching states are present in the entire operating cycle. The circuit may attain high efficiency, and >90%

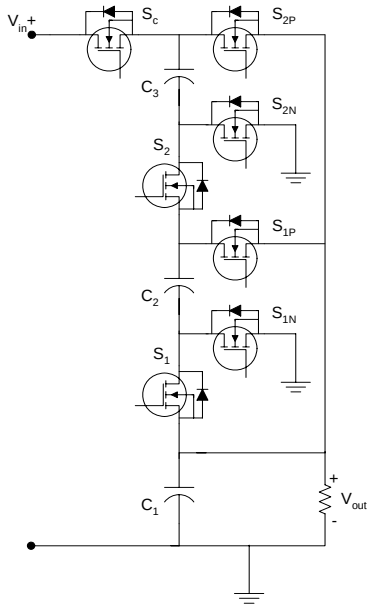


Figure 3-1. The schematic of a three level series-parallel switched capacitor dc-dc converter.

efficiency was reported from this circuit. However, the major disadvantage of this circuit is the difficulty to change the number of stages, and thereby the conversion ratio. In addition to that, the voltage stresses across the different switches are not equal. The top-level transistors S_C, S_{2P}, S_{2N} experience two times the voltage stress as the bottom level transistors.

The direction of power flow in the circuit depends on the voltages at the two ends. Thus, it is not possible to control power flow in between two voltage buses where the bus voltages may vary. In the charging state of the converter, all the capacitors are connected in series. It eventually may initiate a charge unbalance situation among the capacitors. The non-modularity of the circuit leads to a lack of any redundancy in the system to bypass any fault in the circuit. For this reason, it may not be a good candidate for a bi-directional power converter in automotive applications.

3.2 FLYING CAPACITOR MULTILEVEL DC-DC CONVERTER

The second multilevel converter considered in this literature is the circuit presented in [7], [25] - [27]. This converter is known as the flying capacitor multilevel dc-dc converter (FCMDC). The converter presented in [7] is shown in Figure 3-2. This 3-level design can control the power flow in between two voltage buses where the high voltage bus V_{42} is three times of the low voltage bus V_{14}. Though this circuit has a conversion ratio of three, it is defined as a 4-level converter in the literature [7], [25] - [27] considering the zero voltage as a level. In multilevel inverters, zero voltage is considered as an additional level because negative voltage levels are present in the circuit. However, in multilevel dc-dc converters, the zero voltage level

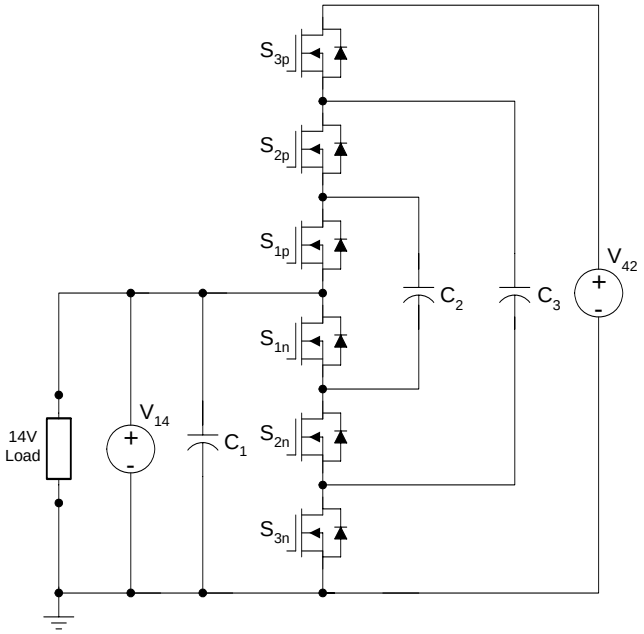


Figure 3-2. The schematic of a 3-level FCMDC circuit.

may be omitted, and in the foregoing discussion, zero voltage will not be considered as a level in the multilevel dc-dc circuits.

This circuit topology can achieve high average efficiency of more than 96%; the maximum efficiency could reach close to 98%. This is a magnetic-less design capable of bi-directional power flow, and the circuit could be designed with one power source or two. The circuit requires the minimum number of transistors for any conversion ratio. For an N-level design, it requires 2N transistors. Moreover, all the transistors used in the circuit experience equal voltage stress. However, this conventional circuit suffers from several limitations. First, the FCMDC circuit does not have a modular structure. For this reason, the circuit cannot be easily extended to increase/decrease the number of levels, hence changing the conversion ratio. The other major limitation is the complicated switching schemes for the different transistors shown in Figure 3-3. In

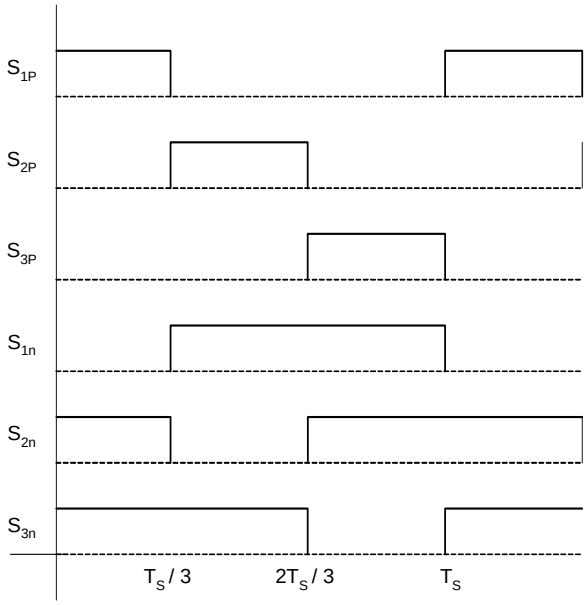


Figure 3-3. The switching scheme of a 3-level FCMDC circuit. There are three sub-intervals for three a level operation.

addition to that, during one operating cycle, only one sub-interval is associated with the energy extraction process from the high voltage side battery in this converter. During the other sub-intervals, energy stored in capacitor C_3 is transferred to the other capacitors through the output circuit. Thus, when the conventional converter is designed with a high conversion ratio such as 5 or more, one capacitor takes energy from the high voltage battery for a period of one-fifth of the switching cycle. This is not a serious issue when the conversion ratio is low. However, when the conversion ratio is high, only a small timeframe is allowed to transfer the energy from the voltage source to the capacitor, and from the capacitor to the next level capacitors as well. Sometimes it is desirable to operate the circuit at high frequency to reduce the capacitor sizes [7]. However, when the transition time (rise time and fall time) of a transistor is comparable to the ON time (t_{on}) of it, the circuit becomes inefficient. For an N-level converter, the ON time for any

transistor shrinks to $(1/N)^{th}$ of the total time period, and the effective switching frequency is N times of the original switching frequency. This increased effective switching will introduce high frequency noise at the output dc voltage. For these reasons this circuit cannot be operated at high frequency.

The higher voltage drop across the active switches or diodes during conduction is another limitation of the conventional FCMDC. This fact can be revealed from Figure 3-2. During any subinterval, 3 transistors/diodes are turned on and the input/output current flows through these 3 transistors/diodes. In fact, for an N-level converter, a total number of N transistors/diodes are intended to flow the current, which could add a severe voltage drop across them during high power applications. Since this operation takes place N times in a complete cycle, the dynamic loss is higher too. Thus, the remedy to this limitation would be to obtain a circuit such that the number of devices in a series path is significantly less. By obtaining a new circuit, the voltage regulation of the converter can be substantially enhanced and dynamic loss can be reduced.

In addition to the limitations mentioned above, the component utilization of this converter is limited compared to the new converter that will be proposed in Chapter 5. Because of the limited component utilization, the size of the capacitors and MOSFETs must be over designed in order to transfer a certain amount of power. The incapability to withstand any fault in the converter is another limitation. To form a 3-level converter, 6 transistors are required, and if any one of these transistors fails, it is not possible to continue the operation of the circuit. Hence, the circuit configuration is non-modular, so no redundancy can be incorporated in the circuit.

In the proposed application where the converter is responsible to transfer power from a high voltage battery to a low voltage battery or vice-versa, the direction of power flow depends on the voltages at the two ends. For a 3-level converter, if the voltage at the high voltage side battery is more than three times of the low voltage battery, then the power is transferred from high voltage side to the low voltage side. In the same token, if the high voltage side battery voltage is less than three times of the low voltage battery, then power is transferred from low to high voltage side battery. This property of power flow indicates the incapability of having a true bi-directional power flow where the direction will not depend on the battery voltages. Table 3-1 summarizes the possible cases where the converter fails to establish a bi-directional power management. In automotive applications, the battery voltage at two ends can vary within a wide range, though power transfer may be required in either direction irrespective of the two end battery voltages.

3.3 MAGNETIC-LESS MULTILEVEL DUAL VOLTAGE DC-DC CONVERTER

The next converter considered in this discussion is the one presented in [28], [29]. The circuit is shown in Figure 3-4. The heart of the circuit is the switching cell, which is

Table 3-1. Direction of power flow at different battery voltages.

Case	Ratio of battery voltages	Power flow direction	Power flow from high side to low side	Power flow from low side to high side
1	>3	High to Low	Possible	Not possible
2	<3	Low to High	Not possible	Possible

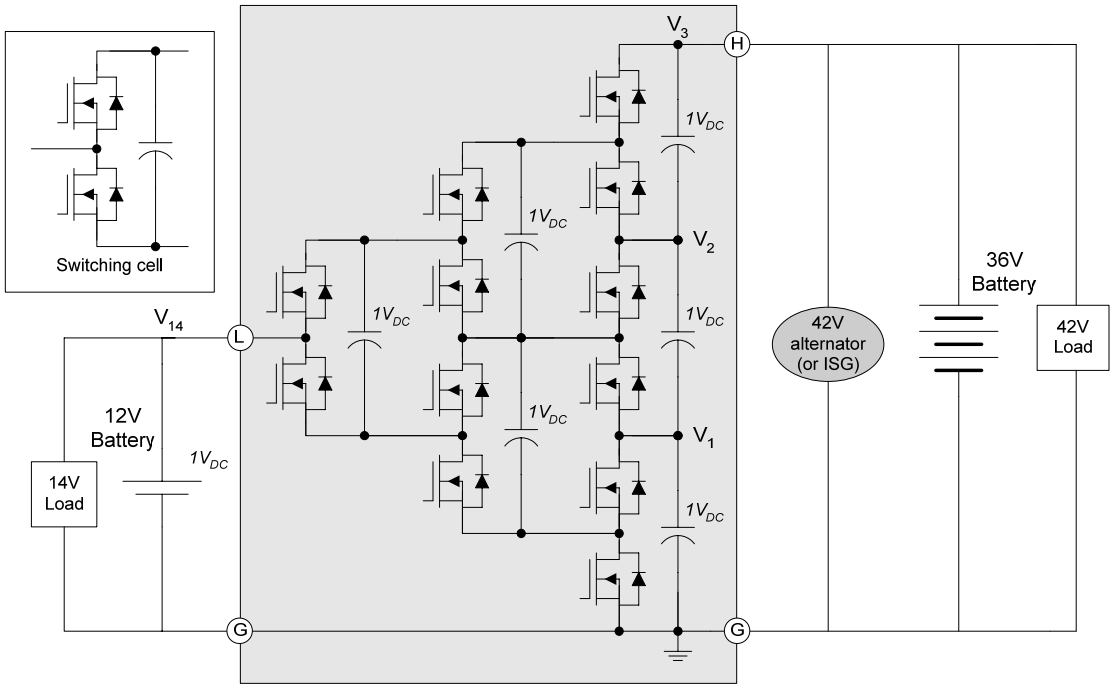


Figure 3-4. The design of a 3-level multilevel converter built from two transistor switching cell.

a modular block having two transistors and one capacitor, and the cell is shown in Figure 3-4 also. When multiple cells are connected in a mesh pattern, the whole converter is formed. The circuit shown in Figure 3-4 is a 3-level design (though it is defined as a 4-level circuit in the [28], [29] considering ground as an additional level) and it is capable of transferring power between V_{42} and V_{14} buses. In the down conversion mode, the circuit produces 14 V at the low voltage side when it is powered from a 42 V source. In the up conversion mode, it produces 42 V from a 14 V source.

This circuit has several advantages over the existing multilevel converter topologies. The circuit can be considered as a mesh circuit built from the switching cell. In each individual cell, the transistors experience 1 V_{DC} voltage stress, which is

independent of the conversion ratio. The circuit uses one bootstrap gate drive circuit driving two transistors (IR2011) in each switching cell. While powering up the circuit following some pre-defined steps, the circuit does not need individual power supplies for the bootstrap gate drive circuits. Thus, some part of the total cost can be saved.

However, there is a major drawback associated with the circuit, which prevents it to be an inexpensive and commercially viable choice. For an N-level converter, it needs [N(N+1)/2] switching cells meaning N(N+1) transistors and N(N+1)/2 capacitors. Thus for a 5-level converter (N = number of levels or the conversion ratio), it needs 30 transistors and 15 capacitors. Thus, the component count is much greater than the FCMDC converter presented in this literature (Figure 3-2). Moreover, when the number of levels is 4 or more, the increased cost for additional transistors cannot be compensated by the cost saving in the gate drive circuit.

The lack of a true bi-directional power management is another flaw of this design. For the same reason present in the FCMDC converter, this converter's power flow direction depends on the battery voltages at the two ends. This is why this is not a viable solution for some applications where the source voltages may vary.

3.4 SWITCHED-CAPACITOR BIDIRECTIONAL DC-DC CONVERTER

This section presents a switched-capacitor (SC) dc-dc converter with bi-directional power flow and some other attractive features presented in [30]. Figure 3-5 shows the schematic of the converter. The voltage conversion ratio of the circuit is governed by a control voltage. This control voltage controls the charging profile of the capacitor *C* in the circuit. To achieve a controlled charging profile, transistor *QS* is

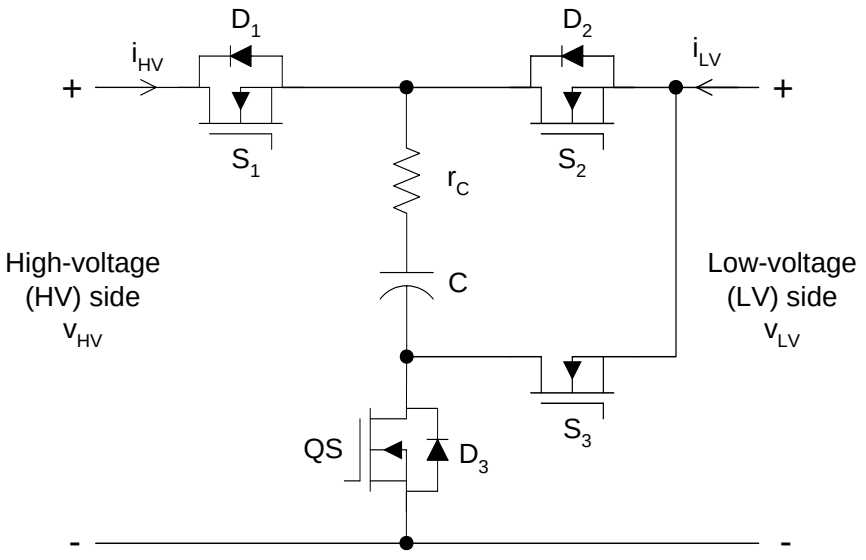


Figure 3-5. Basic SC-based bidirectional converter cell.

operated either in linear or saturated region and this indicates a conduction loss during the charging operation. The other transistors S_1, S_2, and S_3 are operated in either linear or cutoff region like any power electronic switch (considering the active switch a MOSFET).

The converter has two operating modes A and B, and in each mode, the converter works differently. In mode A, the converter works in down-conversion mode, and it works in up-conversion mode while it is in mode B. Each mode has a charging phase and discharging phase. In down conversion mode, these two states are AI and AII and in up-conversion mode, these states are BI and BII. Table 3-2 shows the operation of two converters connected in parallel operating in different modes and phases.

Some of the features of this circuit are as follows: The circuit has very simple structure, and it is an inductor-free design. The circuit can be operated at very high frequency (180 kHz). When connecting two circuits in parallel, the input and output

Table 3-2. Different operating modes of the switched-capacitor converter.

Mode	Time			
	0 to $T_s/2$		$T_s/2$ to T_s	
	Converter 1	Converter 2	Converter 1	Converter 2
Down-Conversion	AI	AII	AII	AI
Up-Conversion	BI	BII	BII	B1

current become continuous which is an advantageous feature of this circuit. However, there are some inherent limitations of this topology, and for these reasons, this converter cannot be successfully used in most power electronic applications. First, the transistor SC does not work as a power electronic switch, rather it operates in either saturation or linear state. For this reason a large conduction loss is associated with this transistor, and the maximum obtainable efficiency of this converter can reach only 85%. The other main reason is the low conversion ratio of the circuit. The present design has the conversion ratio of 2 only, and the paper does not provide any guidance for increasing the conversion ratio. Also, the paper does not have any indication of introducing modularity in the system to increase the conversion ratio.

3.5 FIBONACCI CONVERTER

The switching converter shown in this section is known as the Fibonacci converter presented in [31]. The reason for this naming is after the famous Fibonacci series as the converter works in the same fashion. Figure 3-6 shows the schematic of a Fibonacci converter. The detailed analytical expression of this converter is found in [31],

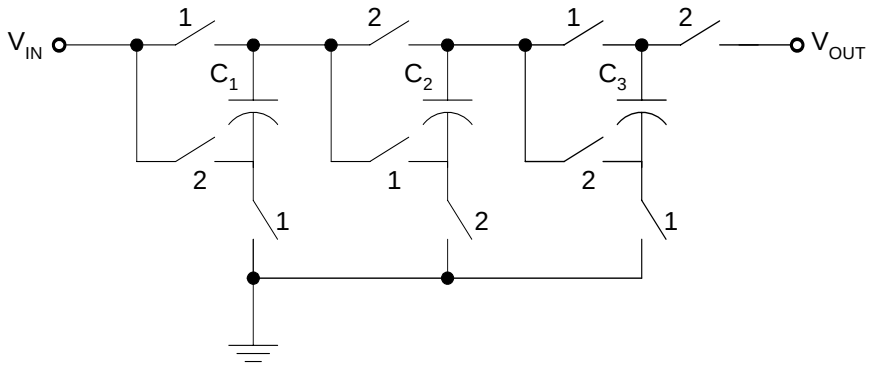


Figure 3-6. A Fibonacci converter with voltage amplification of 5.

[32], and it was analyzed with some other converters in [33]. Basically it was a voltage multiplier circuit and simple in design and operation. It can generate any output with a multiplication factor that follows the Fibonacci series. Thus, the output could be 3, 5, 8, 13, etc. times of the input voltage. Like this converter, many other similar voltage multiplier topologies are found in the literatures introduced in the 1970's [34], [35].

The major advantage of this topology is the high amplification factor from minimum number of components. The schematic shown in Figure 3-6 has only 3 capacitors and 10 transistors, and it can produce an output with a multiplication factor of 5. Using one more capacitor and three more transistors, the multiplication factor can be increased to 8. However, the main disadvantage of this topology is that the multiplication factor of this converter follows the Fibonacci series. So it is not possible to make the output voltage 2 or 4 times of the input voltage. The second limitation of this converter was the incapability of transferring power in both directions. Power can only be delivered from low voltage side to high voltage side.

3.6 "GEAR-BOX" CHARGE-PUMP CIRCUIT

Article [36] introduces a new topology of flying capacitor dc-dc converter for low conversion ratio. The conceptual circuit diagram of this topology is shown in Figure 3-7. This topology is a modified version of the conventional charge-pump circuit. The topology presented here is a cascaded combination of two single ended switched-capacitor circuits. The conversion ratio of the circuit has a range of 1/3 to 3, and this is shown in Table 3-3. By changing the internal connection of the capacitors, the conversion ratio can be changed among the 6 values mentioned in Table 3.3. However, it is possible to change the conversion ratio without this step manner. To implement this, the internal resistance of the conduction path of the transistors is changed. By changing the gate voltages, the $R_{DS(ON)}$ of the conducting transistors are controlled to attain any conversion ratio in the range of 0.333 to 3.

This new circuit has some better features compared to the other existing topologies. The circuit operation is simple. The fine change in the conversion ratio

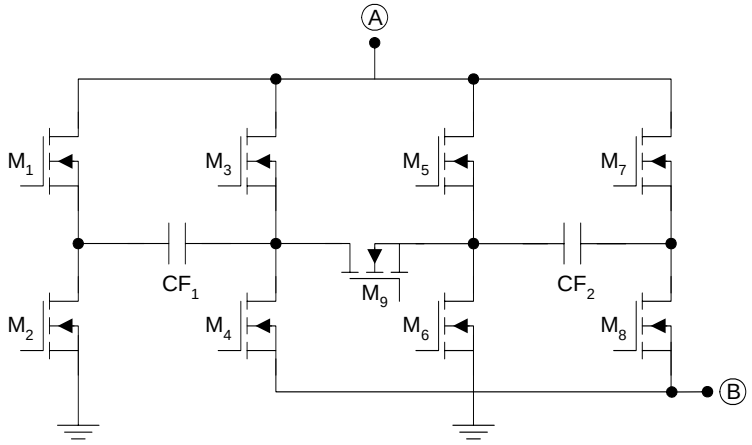
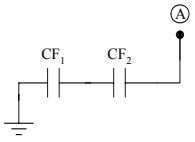
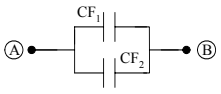
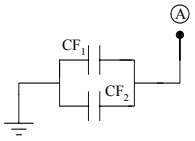
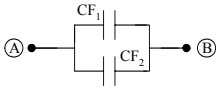
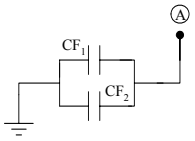
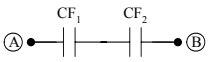


Figure 3-7. The "Gear-Box" Charge-Pump circuit.

Table 3-3. Conversion rates of the "Gear-Box" topology in different configurations.

Conv. Scheme	Charge Transfer in Phase A	Charge Transfer in Phase B	Node (A)	Node (B)	Conv. Ratio
I			Input	Output	3/2
			Output	Input	2/3
II			Input	Output	2
			Output	Input	1/2
III			Input	Output	3
			Output	Input	1/3

can be made by changing the gate signal of the transistors in the conduction path. Thus, it is possible to attain any conversion ration ranging from 0.33 to 3. However, these features come with some price. The circuit has greater number of transistors compared to the other topologies. For a maximum conversion ratio of 3, the circuit uses 9 transistors and two capacitors. A comparatively higher loss is associated with the circuit as the transistors (MOSFET) used in the circuit may work in saturation region ($V_{DS} > V_{GS}$) to control the conversion ratio. This increased conduction loss initiates a comparatively low efficiency (ranging from 65% to 90%) that can be achieved from the circuit.

In this literature, there was no clear indication of the operating frequency of the circuit. Thus, no definite guideline was found regarding the possible application of the circuit in high power electronics. The circuit may be suitably used in low power

applications, however, it may not be suitable for high power applications due to excessive loss caused by the transistors.

3.7 SWITCH-MODE STEP UP DC-DC CONVERTER

A similar approach to [21], [22] is presented in [37]. A modified step-up converter with continuous input current is presented with the addition of an extra phase. The schematic of the circuit is shown in Figure 3-8. The circuit works in a very simple way, and it has two parallel sections that work simultaneously. The entire operation of any section can be divided in four states. In state 1, the capacitors of section 1 are charged from V_1. At the same time, section 2 discharges the capacitor to the output. In state 2, only section 2 remains in action, and all the transistors in section 1 are turned off. In state 3, the charged capacitors in section 1 are employed to discharge energy to the output, and state 2 enters into the inactive state. In state 4, section 1 remains in the same state as state 3, and section 2 enters into the charging state. The time ratio of state 1

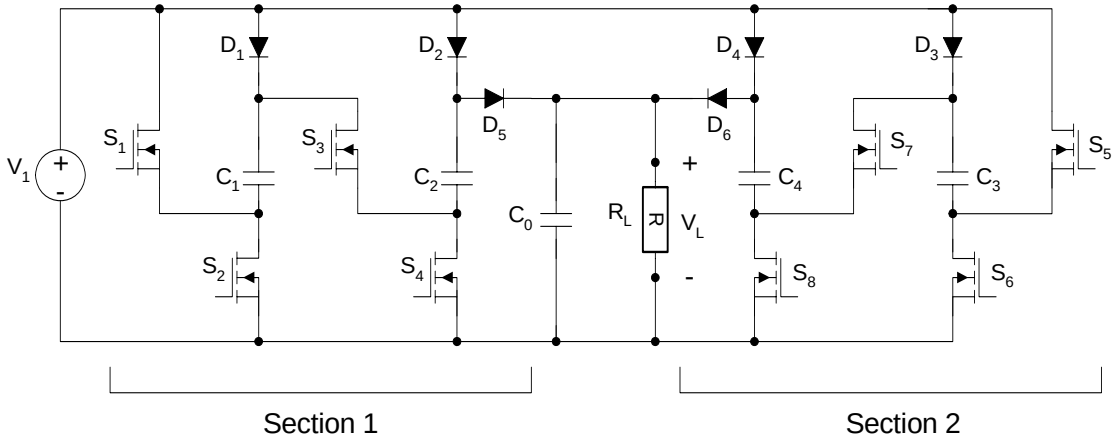


Figure 3-8. The schematic of the step-up dc-to-dc switch-mode converter [37].

to state 2 is termed as the duty ratio, and it is the same as the time ratio of state 3 and state 4. Figure 3-9 shows the timing diagram of the switches inside the converter.

The converter presented here has some good features. Its operation is simple, and output voltage can be controlled by adjusting the duty ratio. Moreover, using two sections, the input current taken from the low voltage source is continuous which eventually reduces the EMI generated in the circuit. However, the circuit suffers from several limitations that would hamper its use in high power electronic circuits. The circuit does not permit the bi-directional power transfer feature. It can deliver power only from low voltage side to the high voltage side. In addition to that, the circuit is suitable to operate at very high frequency (125 kHz), and this will introduce excessively high switching loss for high power applications.

For any power electronic circuit, the efficiency is a very important issue. The

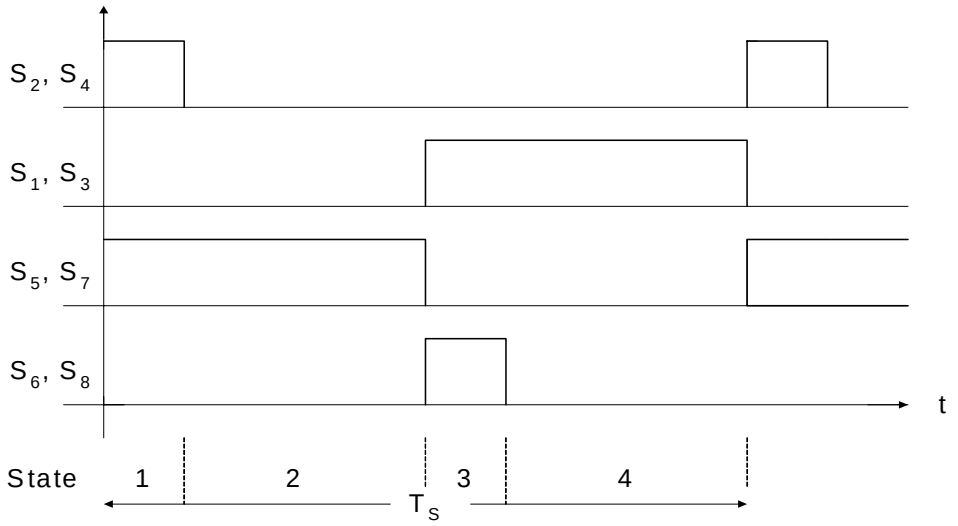


Figure 3-9. The timing diagram of the step-up dc-dc converter [37].

overall efficiency of the circuit is limited to 80% and some other converters can offer more than 90% efficiency for a similar kind of operation. Moreover, the literature does not provide any indication about extending the circuit to achieve a greater conversion ratio. The present design has a conversion ratio of 2.4. However, in high power applications, a converter with flexible conversion ratio would be more suitable.

The topology shown in [38] is almost the same topology as [37] except for the direction of power flow. The circuit presented in [38] is a down converter where the output voltage is half of the input voltage. Moreover, the circuit has two sections as [37] to get a continuous input current. However, all the flaws associated with the converter [37] are true for this converter too. For this reason, this converter cannot be considered as a good candidate for high power applications.

3.8 SWITCHED-CAPACITOR DC-DC CONVERTER WITH LOW INPUT CURRENT RIPPLE

The switched-capacitor converter presented in [39] is another example of capacitive energy transfer circuit. The schematic of the topology is shown in Figure 3-10(a). The topology presented in this literature is described as a step-down converter with a conversion ratio of 2. The main feature focused in this circuit is the continuous input current that helps to maintain a low EMI in the circuit.

The circuit has 4 switches, and they work in 2 phases. There is a delay time between two phases, which is shown in Figure 3-10(b). However, the converter does not seem to have any provision to increase the conversion ratio for various applications. With some modifications, the circuit could be used for bi-directional power management. However, this feature was not discussed in the literature. Although, the circuit has a

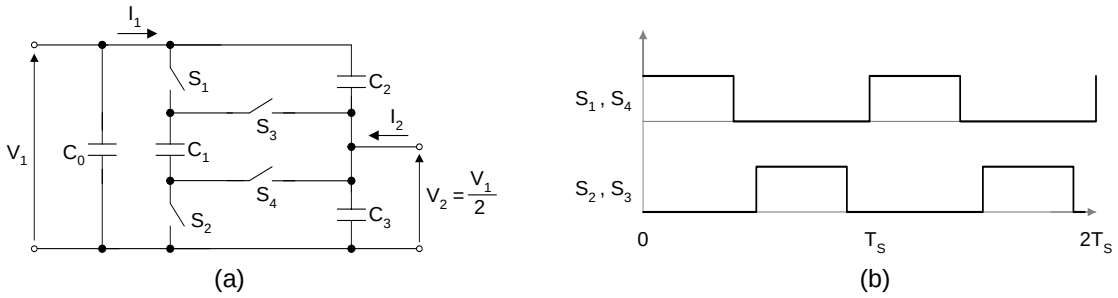


Figure 3-10. A switched-capacitor dc-dc converter with low input current ripple [39], a) the schematic, b) the timing diagram of the 4 switches used in the circuit.

maximum efficiency of 90%, it may not be very useful for high power applications requiring high conversion ratio.

3.9 OTHER CONVERTERS

There are many other different topologies that are not truly switched-capacitor circuits. One of those topologies is presented in [40] which is a special form of boost converter with high conversion ratio. This additional gain is achieved by virtue of a voltage multiplier circuit. The circuit is supposed to run with a higher efficiency compared to the "Flyback" converter. Moreover, more voltage gain can be achieved from a small circuit. Aside from the conventional boost converter, this circuit can achieve high voltage gain without making the duty ratio very high. However, this topology is not an inductor-free design, and the energy transfer is done with a coupled inductor and capacitors. So, at high power applications, the efficiency will not be as great as other switched-capacitor circuits.

The topology presented in [41] is a very good example of high power dc-dc converter running at high efficiency. The circuit has a conversion ratio of 10 and it steps

down 600V to 60V with a power rating of 1.5 kW. The maximum efficiency found from this converter is 92% and the operating frequency of the circuit is 50 kHz. The circuit employs a zero voltage switching (ZVS) technique to reduce loss and it also has a good voltage regulation. The key feature of the converter is the isolation between input and output and the reduced voltage stress across the transistors, which is 50% of the input voltage.

For several reasons, the converter may not be considered as a potential candidate for the requirement of this thesis proposal. The converter in [41] uses a high-frequency transformer and several inductors for ZVS operation. Although the topology is based on the "flying-capacitor" method, it is not a true switched-capacitor circuit; rather energy is transferred to the output through the transformer. The other limitation of the circuit is that it can only transfer power from the high voltage side to the low voltage side, and this is why this is simply a step down converter with a high conversion ratio.

The converter presented in [42] is a potential candidate for a bi-directional dc-dc converter specially designed for automotive applications. This converter can integrate three voltage buses with voltages of 14, 42 and high voltage (HV) bus. The working voltage of the HV bus could be in the range of 200-500 V. Using a high frequency transformer, a high conversion ratio can be achieved and power can be transferred from any one of those three buses to the remaining two buses. By virtue of the transformer, the circuit provides isolation between the high voltage and low voltage side.

The schematic presented in this literature [42] is very simple and uses minimum parts to build it. Moreover, a soft switching technique is employed to reduce losses.

However, the circuit suffers from two major limitations. The operating frequency of the converter is about 22 kHz, and for this high power rating (2 kW), this fairly higher switching frequency may incur high switching loss, and the overall efficiency may degrade (the overall efficiency of the converter is not mentioned in the article). In addition to the efficiency issue, the circuit uses one high frequency transformer and one inductor to incorporate three buses in the system. These inductive elements make the converter bulky and lossy. Moreover, from the experimental results, it was observed that, the voltage produced at the 14 V bus has amplitude of around 10 V when power is delivered from the 42 V bus. In addition, when the circuit works in down conversion mode and powered from the HV bus, the voltage generated at the 14 V bus is around 10 V too. This indicates that the circuit may suffer from voltage regulation at the 14 V bus in different operating conditions. Due to the use of inductive elements, it may not be the optimum choice to be used in automotive applications.

Another topology of isolated multiple source dc-dc converter family is shown in [43] and it presents a similar approach shown in [42]. Aside from [42], this converter uses three electrically isolated voltage sources using a three winding transformer. Thus, the V_{14} bus is isolated from the V_{42} bus. Like the method shown in [42], this topology also uses the zero voltage switching (ZVS) to reduce losses in the circuit. A detailed circuit model has been presented in the literature. However, this circuit also uses the high frequency inductors and transformers to get the isolation and high conversion ratio. Thereby, the overall efficiency of the circuit may not be as high as the efficiency of a switched-capacitor circuit.

The dc-dc converter presented in [44] was mainly developed for military applications, and this circuit could work as a bi-directional power converter to manage power flow between two buses. The circuit involves several magnetic elements and a high frequency step down transformer that provides the proper isolation between the buses. A special form of half bridge circuit at both ends of the transformer facilitates the bi-directional power management. This circuit has a great number of advantages to be used in rugged military applications. However, because of having magnetic elements, this circuit may not have high efficiency compared to its counterparts implemented by switched-capacitor circuits.

A combination of classical Ćuk converter and switched-capacitor voltage divider circuit is presented in [45]. The conventional Ćuk converter has some unique features over the other converter topologies including capacitive energy transfer and continuous input/output current. To achieve a high conversion ratio from a Ćuk converter, the duty cycle must be narrowed down to some extent, and in this situation, the converter may not work properly. Thereby, the method presented in [45] introduces switched-capacitor voltage divider unit so that large conversion ratio can be achieved without narrowing down the gate signal of the switch. To implement the new topology, a series of capacitors are charged to use as the energy transfer element in this converter, and in the discharge cycle, all the capacitors are connected in parallel. In this way, the output voltage can be reduced by some integral factors depending on the number of series capacitors used in the circuit.

The operation of the circuit is simple, and both the input and output currents are

continuous. All the transistors used in the circuit have a common ground and thereby, the gate drive circuit becomes very simple to drive all the transistors. However, the circuit was not designed for bi-directional power flow, and power can be transferred only from the high voltage side to the low voltage side. Moreover, the use of two inductors in the circuit prevents it to become a purely switched-capacitor circuit. The use of voltage blocking diodes is another reason for conduction power loss in the circuit. For these reasons, the maximum efficiency achieved from the circuit is only 75%.

3.10 CHAPTER SUMMARY

A detailed literature study of the existing multilevel and switched-capacitor topologies has been done, and their various features have been discussed. Based on this literature study, the need for a high efficiency, bi-directional, modular, capacitor-clamped dc-dc converter with high power handing capability was observed. The present converters have many good features, however, none of them posses all the desirable features at the same time. This was the main motivation to come up with a new design topology to use it in automotive applications where the converter is intended to establish a power management system having multiple voltage sources. Chapter 5 in this dissertation shows a new topology of multilevel modular capacitor-clamped dc-dc converter, and the modeling and control strategy of the converter are explained in Chapter 6 and 7, respectively.

CHAPTER 4

BASIC SWITCHING CELLS IN POWER ELECTRONIC CIRCUITS

Various forms of modularity in power electronic circuits have been discussed in Chapter 2. Several methods have been presented to construct basic power electronic circuits using small modular blocks consisting of very few elements. When a power electronic circuit is represented with some modular blocks, it becomes easier to analyze the circuit. Unlike digital circuits, most power electronic circuits do not have a uniform pattern so that they can be expressed using some modular blocks. However, the main intention of this literature will be to introduce some modular structures and show how existing power electronic circuits can be synthesized from these structures.

Power electronic converters use switching devices, diodes, inductors, and capacitors as the basic elements. Many circuits have been invented, proposed, and demonstrated to perform various power conversion uses. Classical dc-dc converters like buck, boost, buck-boost, and Ćuk converters are used in various applications, and the modeling of these various structures are important to design the control circuits for these converters. However, these circuits have rarely been examined and investigated in terms of their relationships, topological characteristics, or what are their basic building blocks [46].

The modularity in power electronic converters can be introduced by defining

some modular blocks in the circuit that can be used to construct many other power electronic circuits. These modular blocks can function as the foundation of any dc-dc converter or inverter, and they enhance the synthesizing procedure of the converter. This chapter will introduce two basic switching cells, P-cell and N-cell, along with the applications of them in various power electronic circuits. The basic cells presented here have one switching element and one diode. Existing well-known circuits can easily be represented using some modular blocks configured from these basic switching cells. Moreover, some new circuits will be addressed that are of great interest in understanding the basics of power electronic circuits and their control.

4.1 THE BASIC SWITCHING CELLS

Figure 4-1 shows the two basic switching cells defined in this literature. Each cell consists of one switching device and one diode connected to three terminals: (+), (-), and (→) /or (←). Each cell has a common terminal which is shown as (→) /or (←) on the schematic. For the P-cell, this common terminal is connected to the positive terminal of a current source or an inductor. For an N-cell, this common terminal is connected to the negative of a current-source or an inductor. The active switching device in a P-cell is connected between the (+), and common terminal, whereas in an N-cell, the switching device is connected between the (-) terminal and the common terminal. Thus, the P-cell is the mirror circuit of the N-cell and vice versa [47].

The basic switching cells proposed in this literature are the practical implementation of the canonical switching cell found in [1]. Although the switching cells presented in this literature have only two components, they can be connected in different

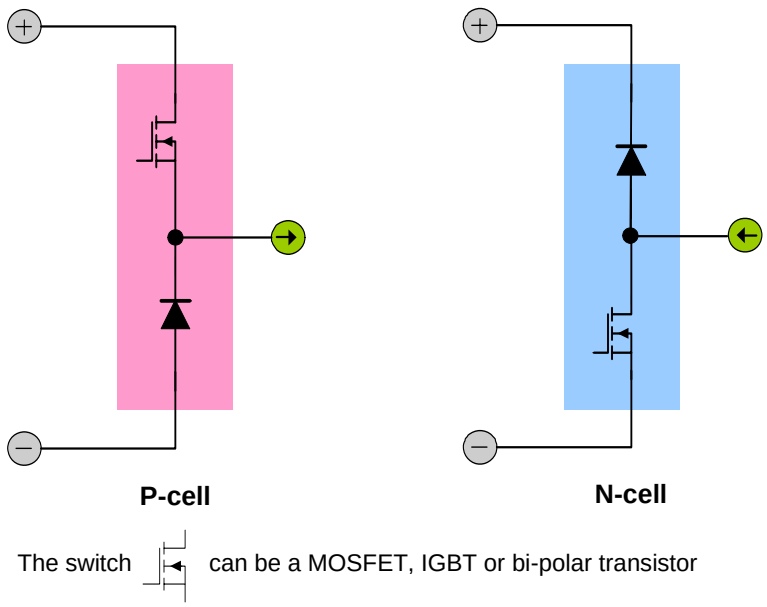


Figure 4-1. Two basic switching cells: P-cell and N-cell.

combinations to create various power electronic circuits. The P-cell is the mirror circuit of the N-cell and vice-versa, and most power electronic circuits can be analyzed and re-constructed using these basic switching cells. The present discussion will describe the construction and operation of these basic switching cells and will also show a sequential method to reconstruct several classical dc-dc converters and inverters. In addition, the use of basic switching cells introduces some new topologies of dc-dc converters that originate from the buck, boost, and Ćuk converter. This chapter will also illustrate the experimental results of the new and existing topologies constructed from basic switching cells.

4.2 DC-DC Converters Built from Basic Switching Cells

Figure 4-2 summarizes the four classical converters and their cell structures. In this figure, there are three columns and each column has 4 figures. The figures in the leftmost column show the four major classical converters. These converters are made

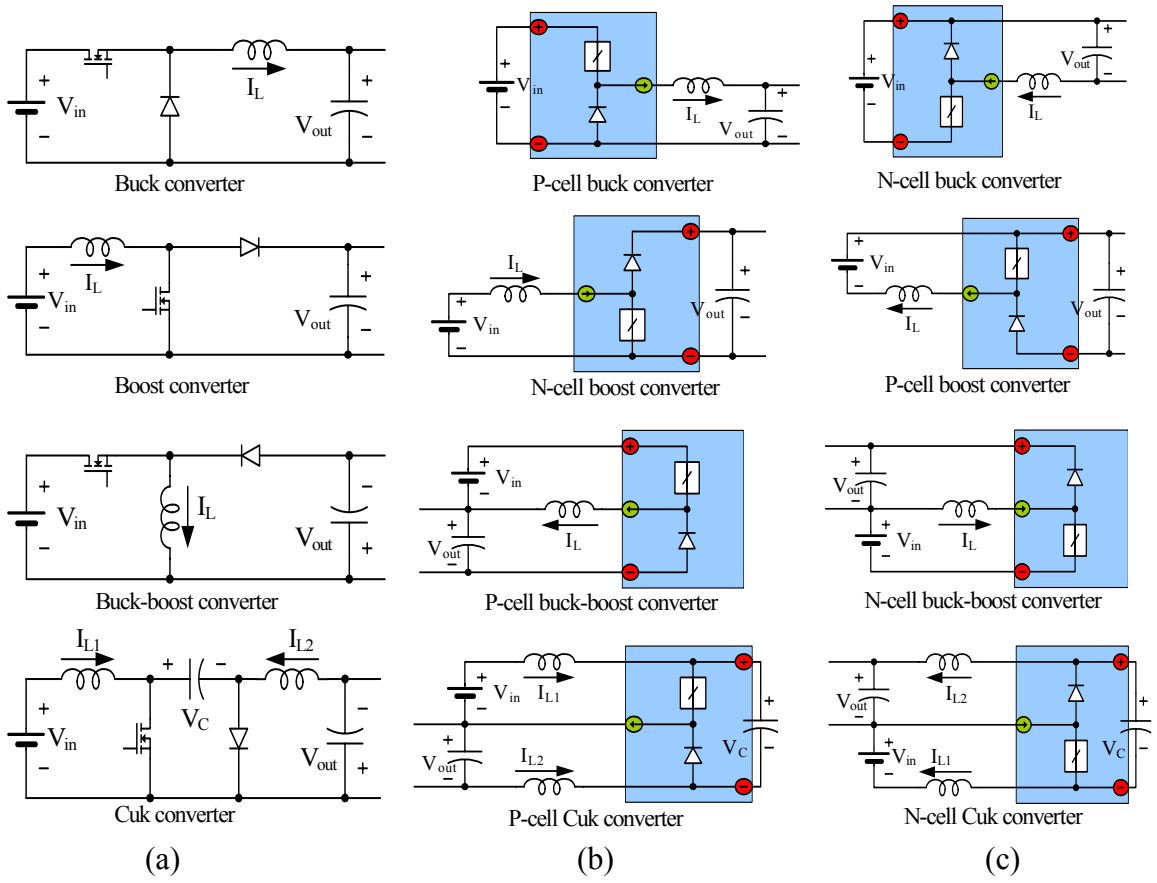


Figure 4-2. a) Classical dc-dc converters, b) formation by the basic cells, c) their mirror circuits.

from inductors, capacitors, diodes and controlled switches. As stated previously, each of these converters can be expressed using the basic switching cells, and their corresponding circuits are summarized in the middle column. The converters in this column are made from either N-cell or P-cell. Thus except for the boost converter, all of the conventional converters have an inherent P-cell structure where the active switching element is connected to the positive power supply terminal. The conventional boost converter is inherently an N-cell boost converter.

All of these classical converters also have a mirror circuit representation. When the P-cell in a buck converter is replaced with an N-cell, the circuit takes a different configuration. In this way, the classical boost converter can be re-constructed using a P-cell, rather than an N-cell. The buck and boost converters can be easily decomposed into a P-cell and N-cell based circuit respectively. However, this procedure is not so obvious for the buck-boost and Ćuk (boost-buck) converters; they inherently take the P-cell structure. The mirror circuit representation of each dc-dc converter is shown in the rightmost column of Figure 4-2. These circuits are new and will find some interesting applications.

The construction of a P-cell circuit differs from an N-cell circuit by the relative position of the active switch. The introduction of an N-cell module simplifies the gate drive circuit because of the ground referenced gate signal. When the gate drive circuit is ground referenced, the converter circuit is more immune to supply noise and gate drive noise. On the other hand, an N-cell circuit produces an output referenced to the (+) terminal of the input power supply. When it is not necessary to have the output side

referenced to input ground, an N-cell circuit should perform better than a P-cell structure because of the ground referenced gate drive signal. To compare the performance of the P-cell and N-cell structures, two different buck converters were simulated and tested experimentally, and the corresponding results are shown in section 4.4.

4.3 Insights of the Basic Cells and New DC-DC Converters

The conventional Ćuk converter has an especially unique structure [19]. A Ćuk converter has continuous input and output current, and the energy is transferred from the input to the output side by means of a capacitor. The classical Ćuk converter has an inherent P-cell structure, and using the technique presented in this chapter, an N-cell Ćuk converter can be achieved. A Ćuk converter is shown in Figure 4-3(a), and the switching cell realization is shown in Figure 4-3(b). The main limitation of the Ćuk converter is that it uses one additional inductor and capacitor. However, simplification can be done using

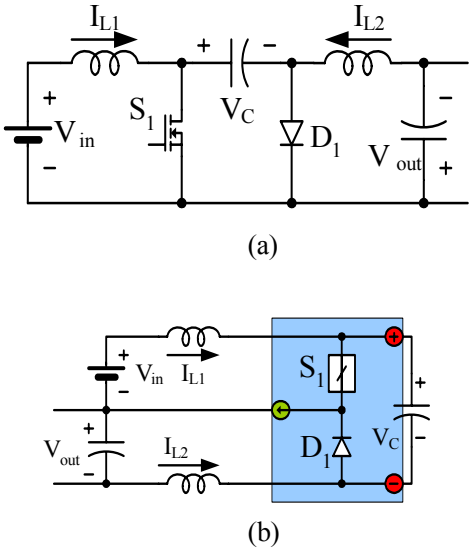


Figure 4-3. a) The Ćuk converter, b) P-cell Ćuk converter.

the basic switching cells and a new version of Ćuk converter can be obtained.

In Figure 4-3(a), during the time when S_1 is on, the rate of change of currents in L_1 and L_2 is the following [48]:

$$\frac{dI_{L1}}{dt} = \frac{V_{in}}{L_1} \tag{1}$$

$$\frac{dI_{L2}}{dt} = \frac{[-V_O - (V_C)]}{L_2} = \frac{V_C - V_O}{L_2} \tag{2}$$

where, $V_O = \frac{t_{on}}{t_{off}} \bullet V_{in}$ (3)

and, $V_C = \frac{T}{t_{off}} \bullet V_{in}$ (4)

Thus using (2) to (4), $\frac{dI_{L2}}{dt} = \frac{1}{L_2}\left[\frac{T \bullet V_{in} - t_{on} \bullet V_{in}}{t_{off}}\right] = \frac{1}{L_2}\left[\frac{t_{off} \bullet V_{in}}{t_{off}}\right] = \frac{V_{in}}{L_2}$ (5)

Using the same procedure, the rate of change of currents in L_1 and L_2 can be found while S_1 is off. During the time when S_1 is off,

$$\frac{dI_{L1}}{dt} = -\frac{1}{L_1} \bullet \frac{t_{on}}{t_{off}} \bullet V_{in} \tag{6}$$

$$\frac{dI_{L2}}{dt} = -\frac{1}{L_2} \bullet \frac{t_{on}}{t_{off}} \bullet V_{in} \tag{7}$$

Thus, using (1) and (5) to (7), a conclusion can be made that if $L_1 = L_2$, then the rate of change of currents in L_1 and L_2 are the same. Moreover,

$$\frac{I_{L1(avg)}}{I_{L2(avg)}} = \frac{I_{in}}{I_{out}} = \frac{D}{1-D} \tag{8}$$

From (8), it is found that, for a specific case when the duty ratio D is 0.5, both the inductors will have the same average value, and if $L_1 = L_2$, they will have the same

current slope. Using these facts, the two inductors can be equivalently moved to the center rail and consolidated into one inductor as shown in Figure 4-4. Because, the converter may not always work at duty ratio D = 0.5, there will be a current mismatch between L_1 and L_2 and the entire converter configuration will perform differently from the original Ćuk converter when D deviates from 0.5.

This new configuration of the Ćuk converter will be advantageous over the conventional Ćuk converter because of lesser part count. From Figure 4-4, it is obvious that the new Ćuk converter is very similar to the P-cell buck-boost converter, except for the capacitor across the positive and negative terminals of the P-cell. In practical use, it is necessary to place a decoupling capacitor in the buck-boost converter, which makes the buck-boost converter identical to the Ćuk converter. Thereby, introducing the P-cell and N-cell structures it is possible to create a link between these two converters. Moreover, new converter topologies can be developed using these basic switching cells. The new Ćuk converter presented in this chapter is an example of many potential findings.

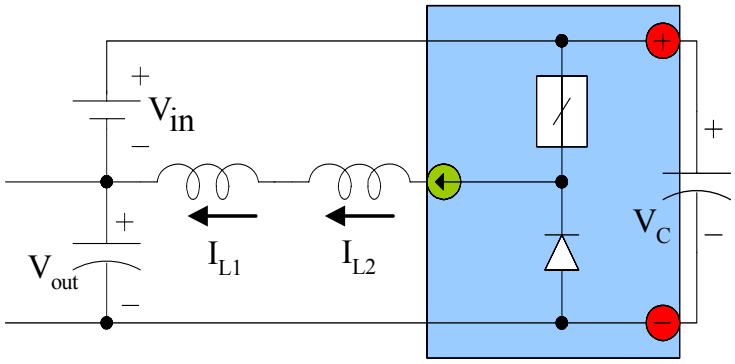


Figure 4-4. The schematic of the modified Ćuk converter. Moving the two inductors of the Ćuk converter to the center rail and combining them into one.

4.4 Simulation and Experimental Results

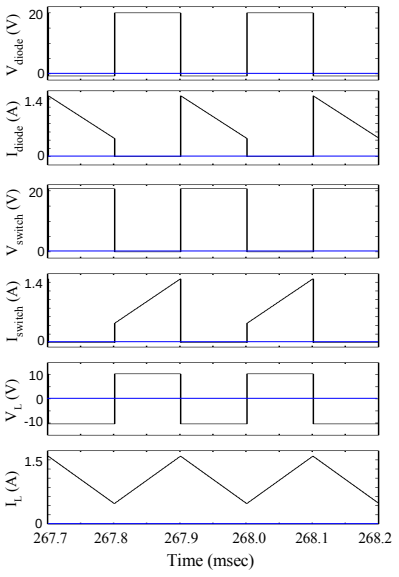
4.4.1 Buck Converter

To validate the concept of the P-cell and N-cell mirror relationship, a buck converter was simulated and tested under continuous and discontinuous conduction mode. The simulations were done in PSIM 6.0 (a power electronic circuit simulator) and the results are shown in Figure 4-5. However, there was no difference found in the simulation results, which leads to the conclusion that there is a mirror relationship between the N-cell and P-cell structures. Then for further verification, a pair of buck converters (one P-cell and one N-cell) were constructed from discrete components and tested in continuous conduction mode. The operating and loading conditions of the N-cell buck converter and the P-cell circuit were the same, but some slight differences were observed in their output voltage. The test results are shown in Figure 4-6.

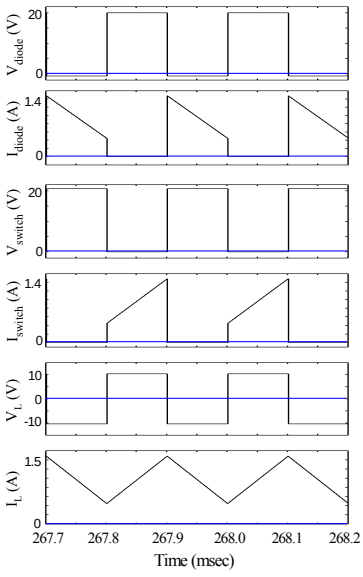
The test setup was as follows:

V_{in} = 20 V, D = 0.4, f_S = 10 kHz, C_1 = 100 μF, L_1 = 1 mH, D_1 = MURB1020CT-1, S_1 = IRG4BC30U, R_L = 20 Ω.

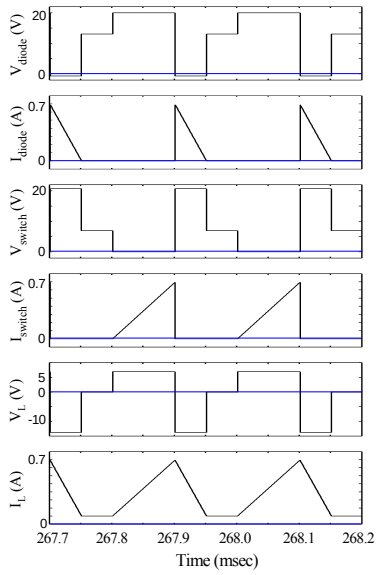
For an input voltage of 20 V and duty cycle 0.4, the dc output voltage for the N-cell structure was 6.82 V and for the P-cell buck converter, it was 7.07 V. Figure 4-6(a) and (b) show the output ripple components of the P-cell and N-cell structure respectively. The fundamental frequency component present in the ripple was the same for both topologies. However, the N-cell structure produces a cleaner output because of the



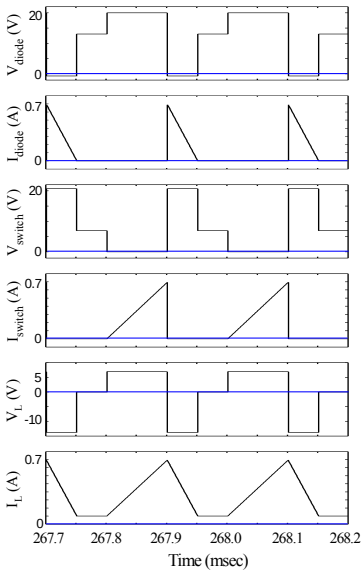
(a)



(b)

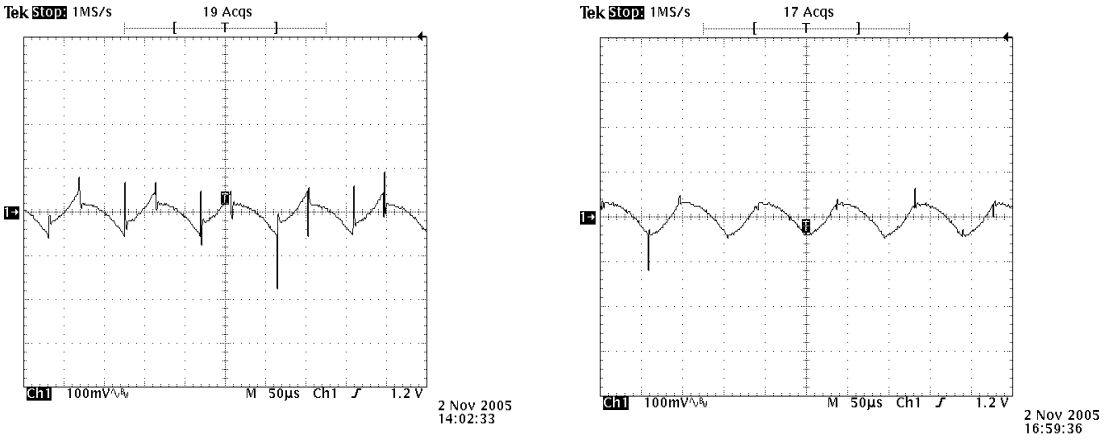


(c)



(d)

Figure 4-5. Simulation results of (a) N-cell buck converter with continuous conduction, (b) P-cell buck converter with continuous conduction, (c) N-cell buck converter with discontinuous conduction, (d) P-cell buck converter with discontinuous conduction.



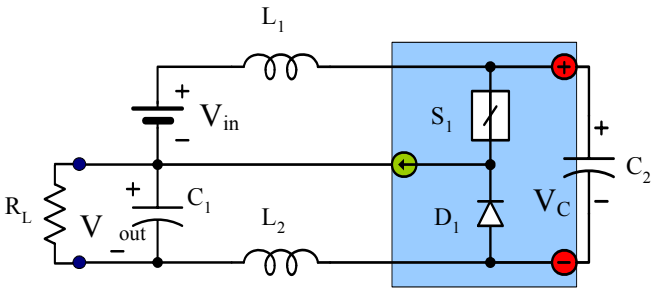
(a) (b)

Figure 4-6. Experimental output voltage ripple (100mV/div) of buck converter, a) P-cell, b) N-cell.

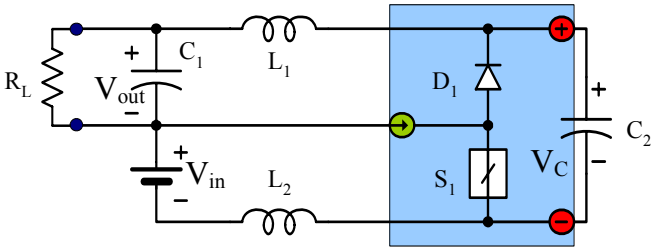
ground-referenced gate drive circuit. The ripple component of the P-cell structure has more harmonic components because its gate drive is referenced to the floating source of the active switch.

4.4.2 ĆUK CONVERTER

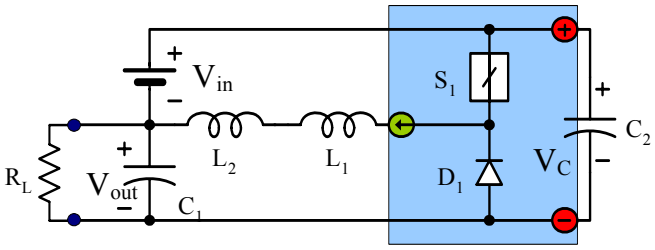
The previous section reveals the fact that the classical Ćuk converter is inherently a P-cell structure. Thereby, there exists a mirror circuit of it, which is the N-cell Ćuk converter. When the two inductors are transferred to one branch such that only one inductor is needed, one gets the third version of the Ćuk converter. To introduce the advantages of basic switching cells, three different kinds of Ćuk converters were constructed and tested. Figure 4-7 shows the schematic designs of the three topologies that were constructed and experimentally tested. Figure 4-8(a) shows the dc output voltages of these converters for a 20 Ω resistive load with a supply voltage of 20 V. The



P-cell Cuk converter



N-cell Cuk converter



New Cuk converter

$R_L = 20\ \Omega$, $C_1 = C_2 = 47\ \mu F$

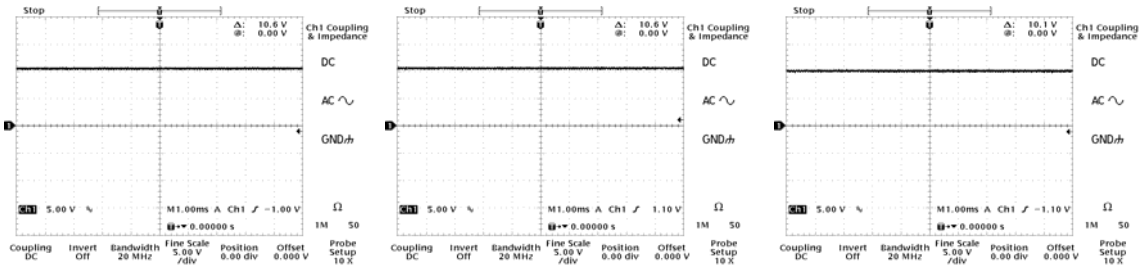
$L_1 = L_2 = 1$ mH

D_1 = MURB1020CT-1

S_1 = IRG4BC30U (Ultra fast IGBT without free wheeling diode)

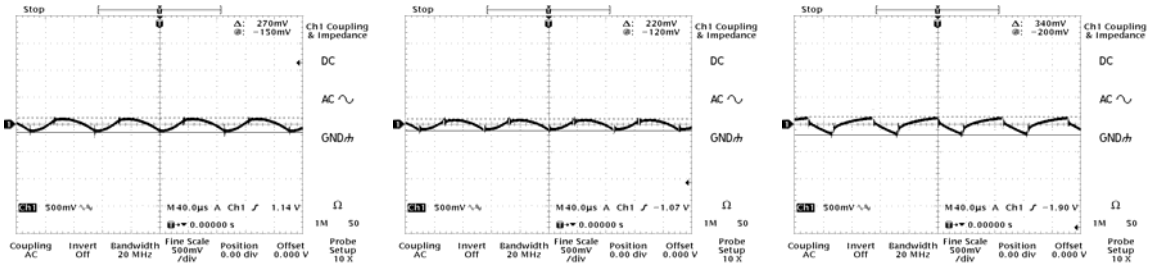
$V_{in} = 20$ V, $D = 0.333$, $f_S = 10$ kHz

Figure 4-7. Schematic of the experimental circuits for a Cuk converter.



P-cell Cuk Converter N-cell Cuk Converter New Cuk Converter

(a)



P-cell Cuk Converter N-cell Cuk Converter New Cuk Converter

(b)

Figure 4-8. a) Experimental output voltage of the converters (5V/div), b) output ripple for different configurations (500mV/div).

duty cycle of the gate drive was kept at approximately 0.33, and for this duty cycle, the output voltage of a Ćuk converter should be around 10 V. In Figure 4-8(b), the output ac ripple is shown by zooming the dc output voltage.

Figure 4-8 clearly shows the evidence that these three converters are fairly equivalent. For the same duty cycle, the P-cell and the N-cell structures produce a 10.6 V dc output, while the new combined inductor topology produces 10.1 V dc output. These are shown in Figure 4-8(a). The ripple component in the N-cell circuit has the lowest amplitude of 220 mVp-p compared to the P-cell structure producing 270 mVp-p. However, the new topology with the two combined inductors produces a ripple of 340 mVp-p, which is slightly higher than the other two topologies. Figure 4-8(b) shows the ripple components in the three configurations.

4.5 CONSTRUCTING VOLTAGE SOURCE INVERTERS FROM THE BASIC CELLS

Like the dc-dc converters, various inverters can be constructed by the use of basic cells in a similar way. Figure 4-9(a) shows that the parallel combination of the P- and N-cells creates a phase leg providing bi-directional current flow. Figure 4-9(b) shows the conventional anti-parallel diode/transistor configuration to create a bi-directional current flow. The parallel connection of a P-cell and an N-cell shown in Figure 4-9(a) has some distinct advantages over the conventional IGBT with an anti-parallel diode.

To create a bi-directional current port in a VSI, two transistors in a phase leg are switched periodically. However, there is a requirement of dead time between the switching periods of the two transistors that prevents a short circuit of the dc link. When an inductor is placed in the paralleled P-cell and N-cell configuration, it takes the shape

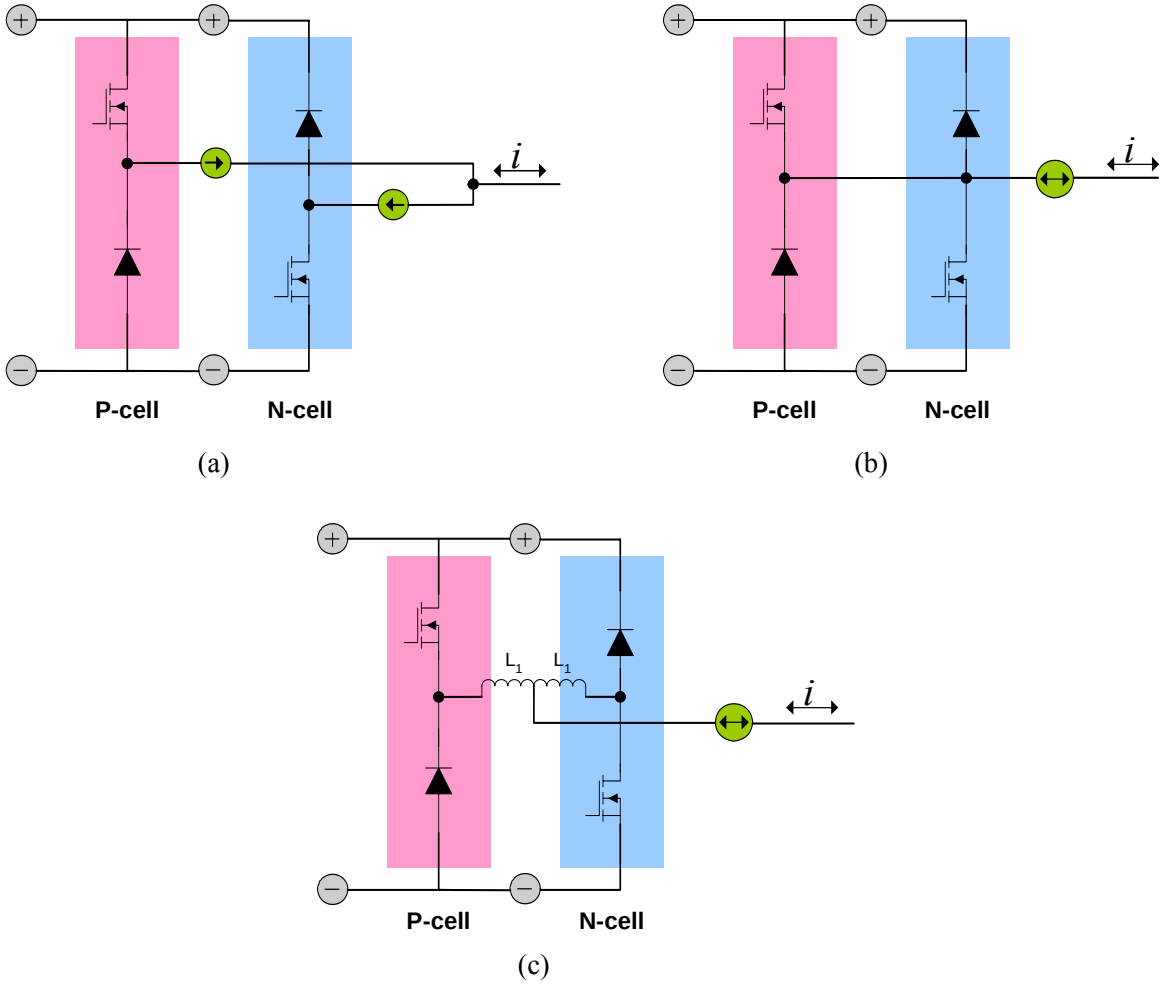


Figure 4-9. a) An inverter phase leg with bidirectional current flow by paralleling the P- and N-cells, b) conventional connection of anti-parallel diode, c) placing two inductors between P-cell and N-cell common terminals to control the current.

of Figure 4-9(c). In this case, a dead time is not required because the additional inductor and the stray inductance of the junction control the current incase if there is any overlap in the switching of the P-cell and N-cell devices. Therefore, IGBT-diode modules configured as the P- and N-cell are better suited for inverter operation, and at any instant of time, the load current only goes through the P-cell during the positive half cycle and through the N-cell during the negative half cycle of the current. Moreover, for a modulation scheme that can detect the direction of current to the load, and control them according to the direction of current, only the switch that can provide the current path need to be switched while the other can be kept off. In the VSI circuit shown in Figure 4-9(b), when the current is going to the load, the transistor in the P-cell is switched on and the transistor in the N-cell is kept off. In the same way, when the current is coming back from the load, it flows through the transistor in the N-cell, and the transistor in the P-cell is kept off.

Figure 4-10 and 4-11 show that the series connection of the P- and N- cells, which forms a three-level (flying capacitor) converter and inverter [49]. Similarly, the diode clamped multilevel inverter and the generalized multilevel inverter structure [50] can be constructed. In Figure 4-10, the series connection uses the same voltage polarity, thus adding voltage to a higher level. Again, it is obvious from these circuits that IGBT-diode modules should be assembled and built according to the P- and N-cell structures.

When two basic switching cells are connected in series to generate a flying capacitor voltage, a new kind of switching cell is obtained. In Figure 4-10(b), when two N-cells are connected in series, N-cell 2 becomes a new 4-terminal switching cell, which

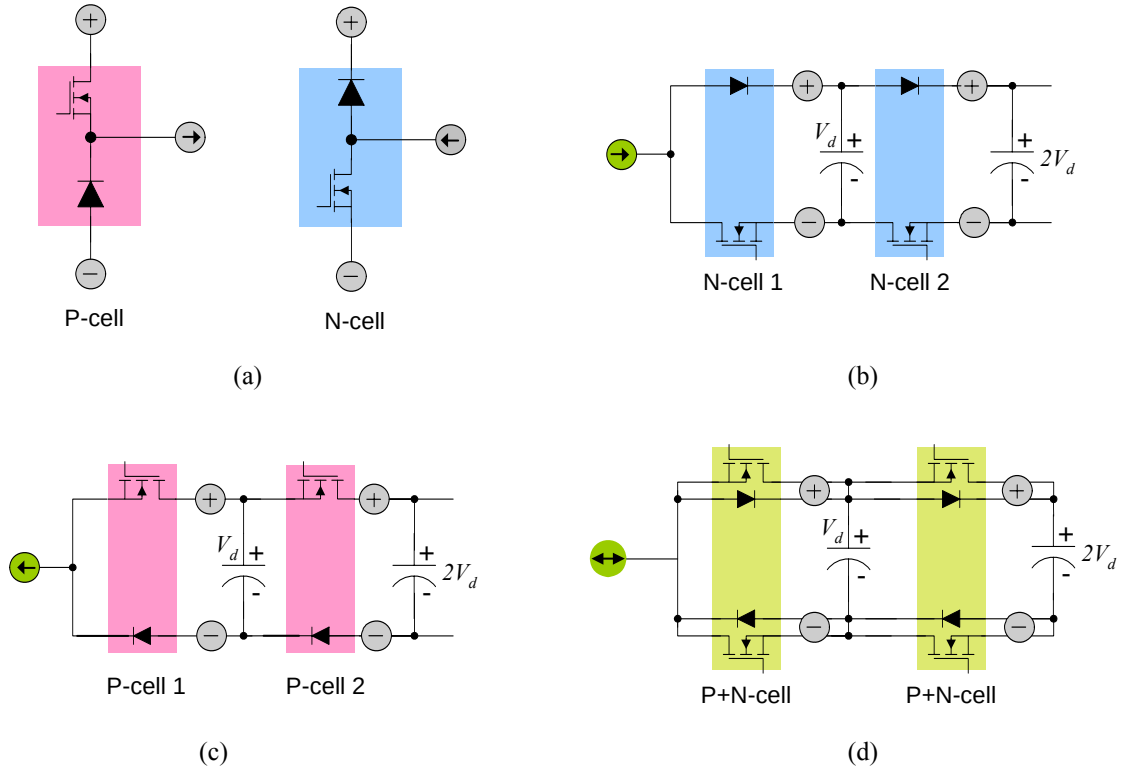


Figure 4-10. A three-level (flying capacitor) converter is formed by the series connection of the P- and N-cells, a) a P and N-cell, b) series connection of two N-cells, c) series connection of two P-cells, d) parallel connection of (b) and (c).

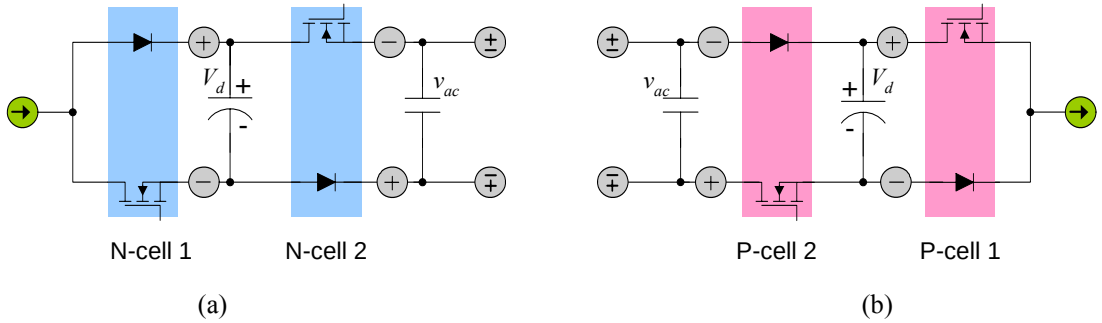


Figure 4-11. Series connection of the N-cells and P-cells to form an ac voltage port, a) an ac voltage port is created from a current source, b) a current source is created from an ac voltage port.

is different from N-cell 1. In the same way, P-cell 2 is different from P-cell 1. This phenomenon was also observed in Figure 4-11(a) and (b) while two switching cells were connected in series to generate an ac port. In addition to that, all the terminologies for P-cell and N-cell used in creating an ac port in Figure 4-11 were valid while v_{ac} was smaller than V_d.

4.6 CURRENT SOURCE INVERTER FROM BASIC SWITCHING CELLS

4.6.1 CONSTRUCTION

A current source inverter (CSI) has several key applications in industry. Figure 4- 12(b) shows a conventional CSI where the load is a series connection of a resistor and an inductor. Four switches S_1, S_2, S_3, and S_4 are operated in pairs so that an alternating current can flow through the load. To get the alternating current, S_1 and S_4 are operated during the positive half cycle of the current, whereas, S_2 and S_3 are switched on during the negative half cycle or vice-versa.

To form a VSI, a P-cell and an N-cell are connected in parallel to build a block, and two blocks in parallel form the entire VSI. However, the mirror structure of this VSI construction is followed to build the series combination of a P-cell and an N-cell, and thus a new type of CSI can be formed. This is shown in Figure 4-11(a), where two N-cells form an ac voltage port from a current source. Figure 4-11(b) shows the series combination of two P-cells to obtain a current source from an ac voltage input.

If the two blocks depicted in Figure 4-11 are connected together, a new single-phase current-source inverter can be constructed as shown in Figure 4-12(a). By eliminating the two middle capacitors (C_1 and C_2) in this inverter, the traditional current-

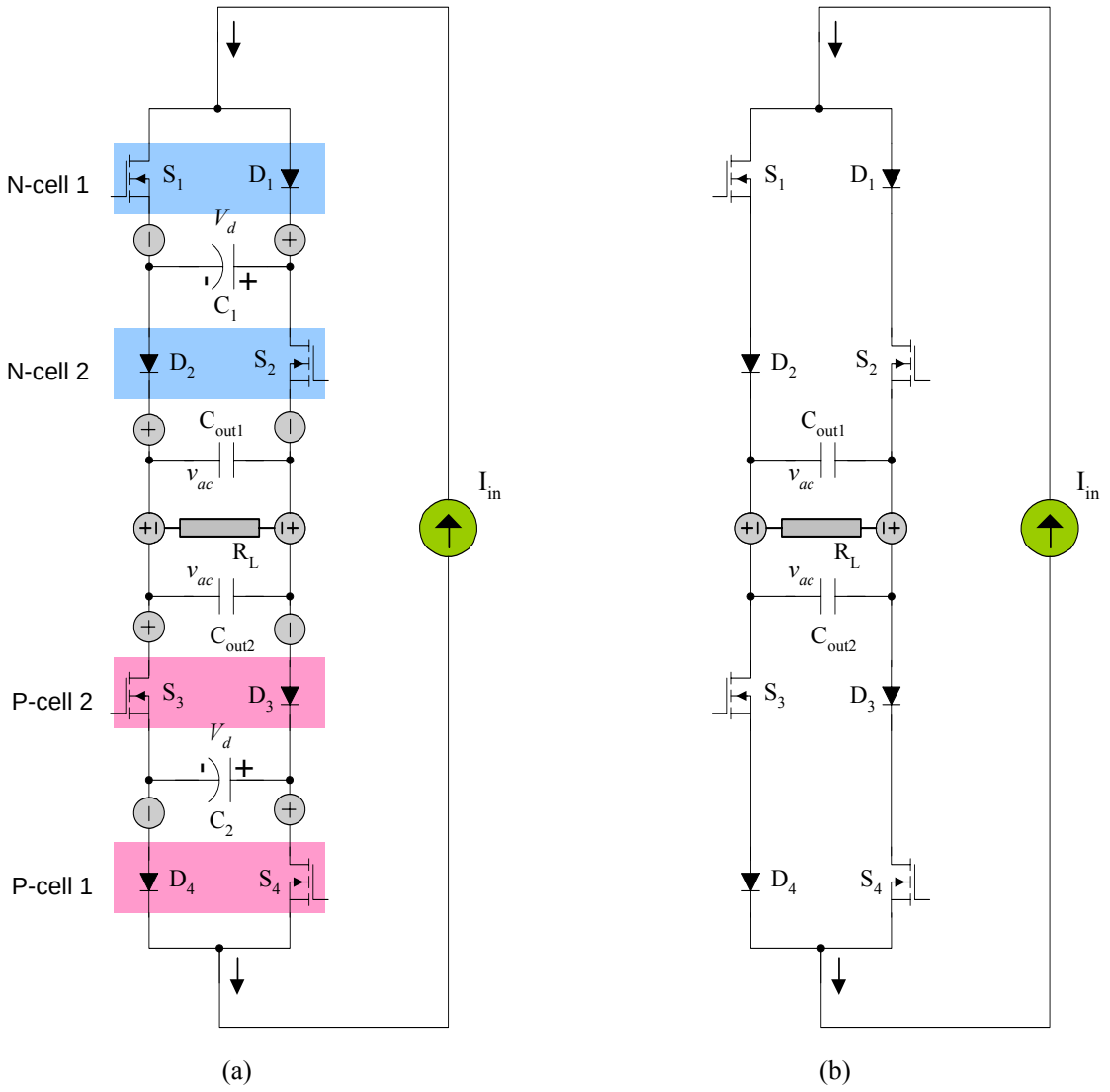
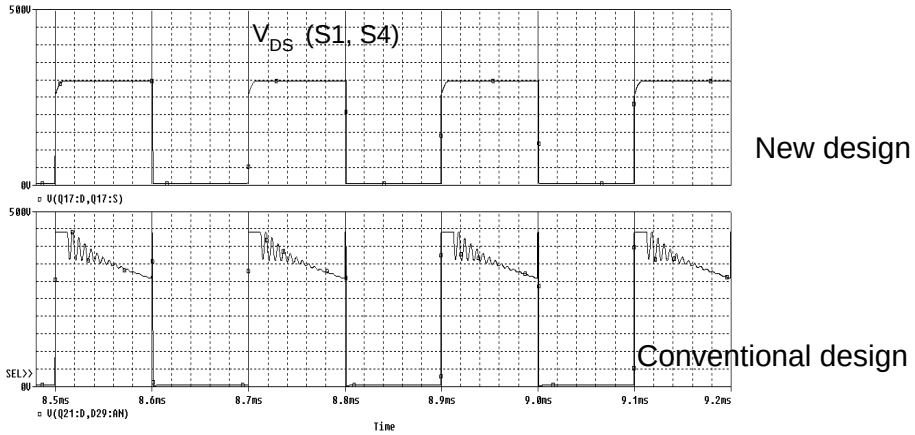


Figure 4-12. a) Current-source inverter with lossless snubber built from P-cell and N-cell, b) traditional current-source inverter.

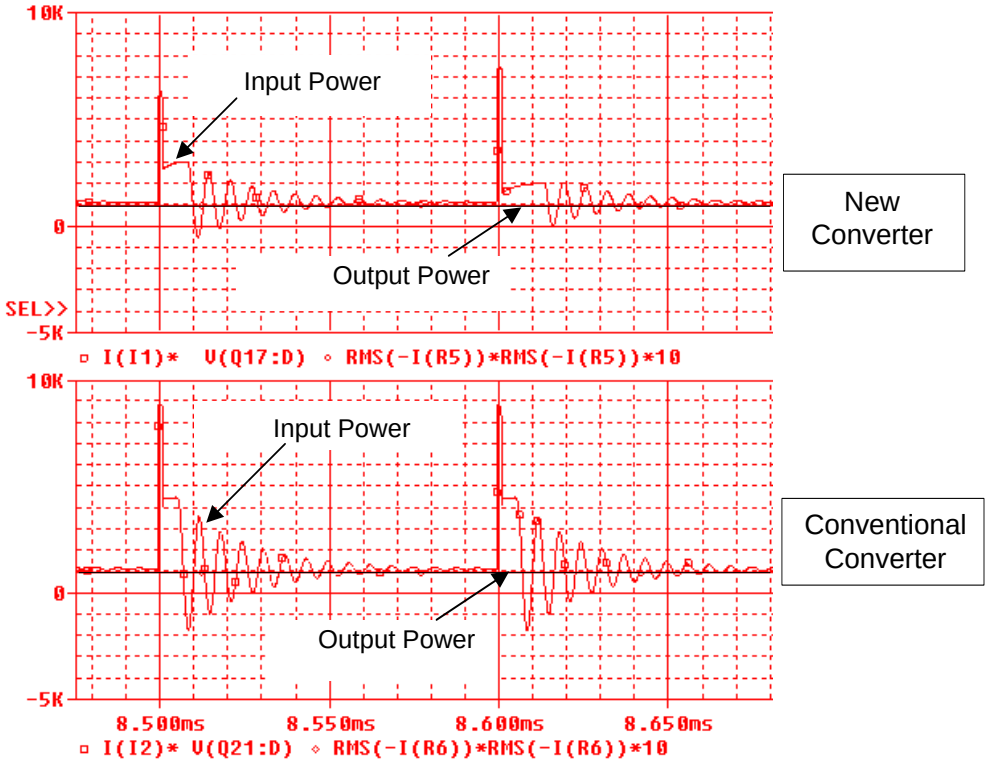
source inverter can be obtained as shown in Figure 4-12(b). As a well-known fact, the traditional current-source inverter experiences difficulties with voltage over-shoot at turn-off and a current commutation problem that requires over-lap time from one phase leg to another. However, the new current-source inverter in Figure 4-12(a) has no voltage overshoot and no current commutation problem. The capacitor C_1 (C_2) with the two diodes form a lossless snubber providing voltage clamping to the switching devices and a current path to the current source, thus improving reliability. The required capacitance should be very small for voltage clamping and current commutation. A justified choice for the value of C_1 (C_2) would be 0.01 μF for practical applications. The three-phase version of Figure 4-12(a) is obvious too.

4.6.2 CSI Simulation Results

To get a clear picture of the superiority of the new topology, a current source inverter was designed and simulated using the basic switching cells. The new circuit has no voltage overshoot as compared to the traditional CSI (illustrated in Figure 4-13(a)) and has less output power ripple (shown in Figure 4-13(b)). A constant load of 1 kW was used for the simulation of both converter types. The new topology can be implemented in several different inverter types. Multilevel inverters with voltage balancing features can be constructed using these basic switching cells, and thus it becomes easier to analyze the entire circuit. In Figure 4-13(a), the V_{DS} across S_1 and S_4 is shown and the new converter shows better performance than the conventional converter. In Figure 4-13(b), the input and output power of the two converters are compared. The input power of the conventional converter has more ripple than that of the new converter. Moreover, the



(a)



(b)

Figure 4-13. a) Comparison of drain to source voltage of the switches in the inverter. The top figure shows the V_{DS} for the new converter and the bottom figure shows the V_{DS} for the conventional converter, b) Input and output power wave shapes of the two converters, the output power is a constant line at a level of 1 kW.

switches in the new converter experience less voltage ripple compared to the voltage drop across the switches in a conventional converter. An R-L load (10 Ω + 100 μH) was used for the simulation. Two 1 μF electrolytic capacitors in parallel were used as the load capacitance (C_{out1} and C_{out2}). The experimental prototype for the P-cell and N-cell are shown in Figure 4-14.

4.6.3 CSI Experimental Results

To show how the new CSI converter constructed from basic switching cells has some superior characteristics compared to the conventional CSI circuit, a CSI circuit was built and tested using the schematics shown in Figure 4-12. Ultra fast IGBTs (IRG4BC30U) were used as the active switches in the circuit and MURB1020CT-1 diodes were used in each switching cell. A 20 V source and a series connected 1 mH inductor were used to get a constant current source. Two 0.01 μF polyester capacitors

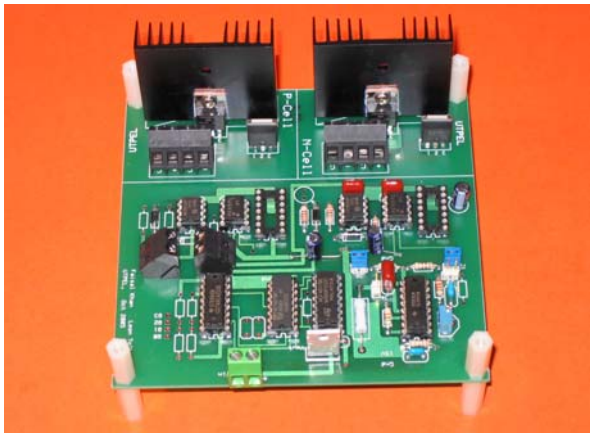


Figure 4-14. The experimental prototype of the P-cell and N-cell. The upper left section shows the P-cell, the upper right section shows an N-cell. The bottom part of the board shows the gate drive circuit.

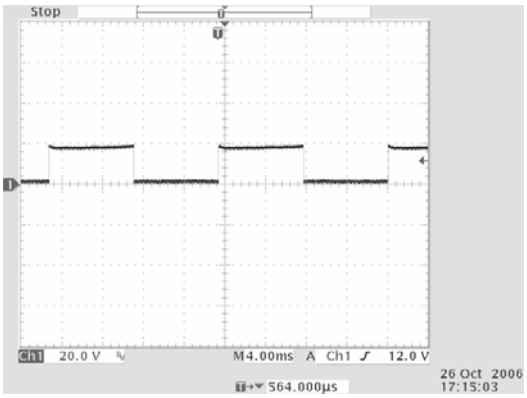
were used as C_1 and C_2 and a 0.1 μF polyester capacitor was used as the load capacitance. A resistor of 20 Ω was used as the output load, and the circuit was operated at 60 Hz.

Figure 4-15(a) shows the V_{DS} of S_1 of the new CSI and (b) shows the V_{DS} of S_1 in the conventional circuit. It is clear that C_1 performs the snubber operation so that the voltage across S_1 cannot increase beyond the supply voltage, and without C_1, the voltage stress across S_1 increases substantially in the conventional CSI. However, a small price has to be paid for this clamping feature. When C_1 is used to control the V_{DS} of S_1, the V_{DS} of S_2 increases slightly in the new CSI circuit. This effect of C_1 on S_2 is shown in Figure 4-15(c) and (d). In addition to the improvement in S_1, V_{DS} of S_3 is much smaller in the new CSI circuit as well. However, C_1 and C_2 do not have any significant impact on the V_{DS} of S_4. The effect of the snubber capacitor C_2 on S_3 and S_4 are shown in Figure 4-16. From these observations, it is prominent that the total improvement in the V_{DS} of S_1 and S_3 is much greater than the increased voltage stress across S_2.

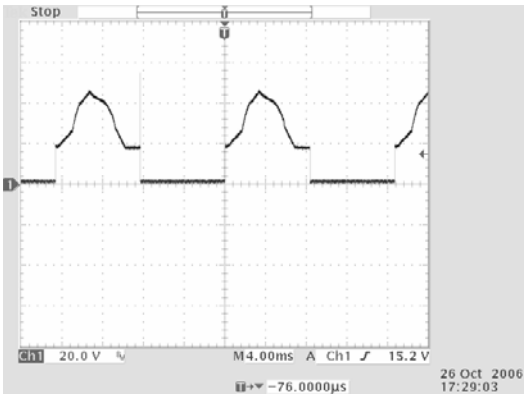
For the same operating condition, no significant difference was found between the output voltages for the new and conventional CSI circuit. It was true for the input current too. The experimental results of the input currents of the two configurations are shown in Figure 4-17. Moreover, the ripple present in the input current is slightly less in the new CSI circuit compared to the conventional CSI circuit as shown in Figure 4-17.

4.7. CHAPTER SUMMARY

The basic switching cells presented in this chapter are not limited to the applications described herein and the advantages of using P-cells and N-cells in dc-dc converters and current source inverters have been described with simulation and



(a)



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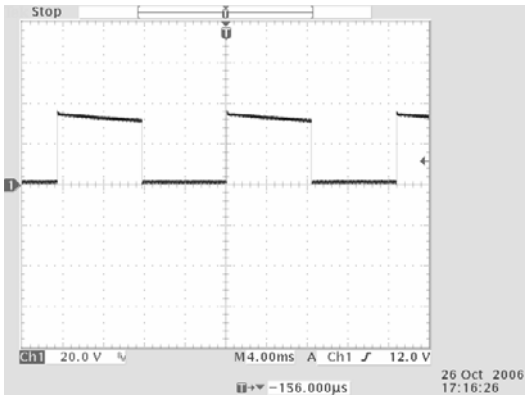
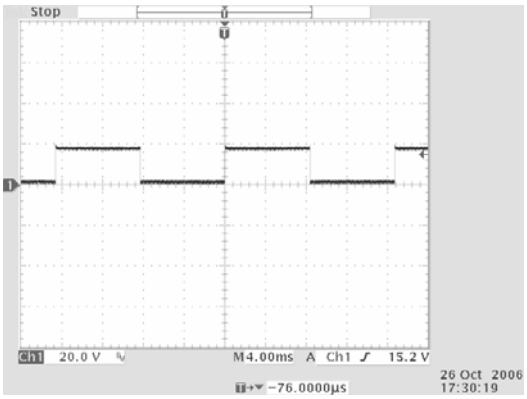
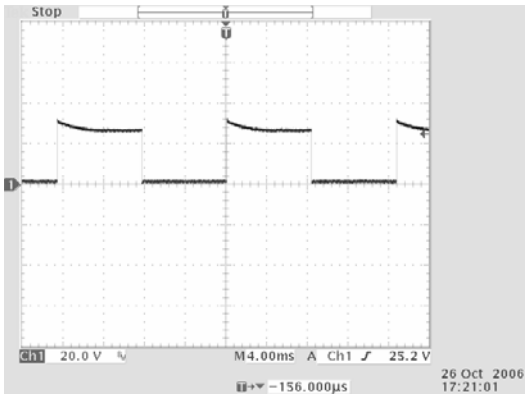


(c)

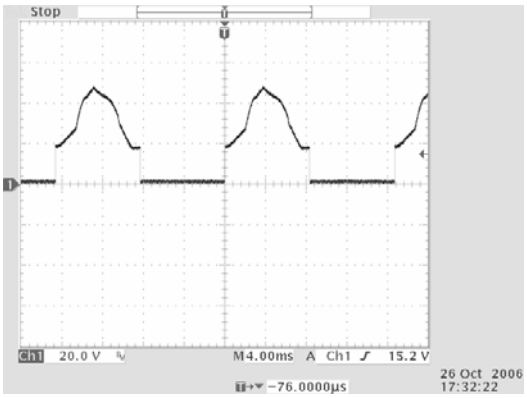


(d)

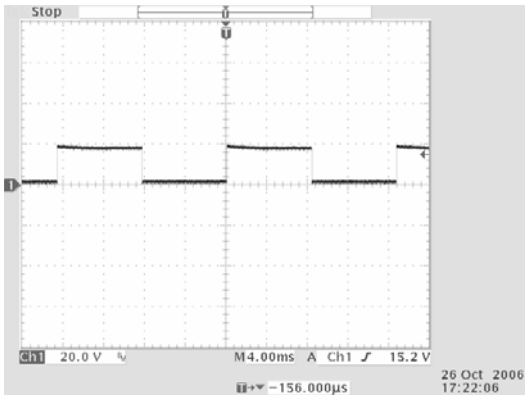
Figure 4-15. Experimental results of the conventional and new CSI circuit. (a) V_{DS} of S_1 in the new CSI circuit, (b) V_{DS} of S_1 in the conventional CSI circuit, (c) V_{DS} of S_2 in the new CSI circuit, (d) V_{DS} of S_2 in the conventional CSI circuit (all voltages are scaled at 20V/div).



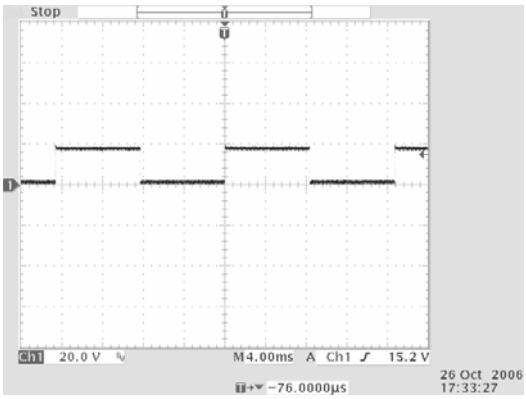
(a)



(b)

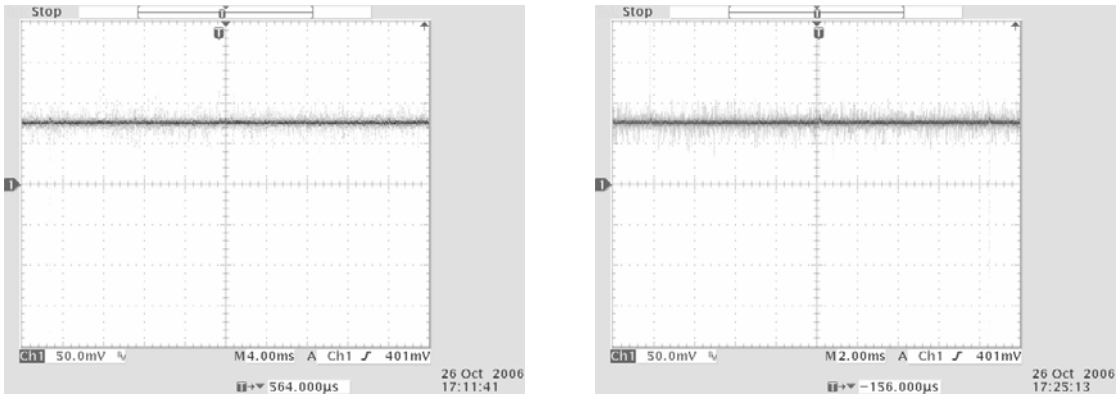


(c)



(d)

Figure 4-16. Experimental results of the conventional and new CSI circuit. (a) V_{DS} of S_3 in the new CSI circuit, (b) V_{DS} of S_3 in the conventional CSI circuit, (c) V_{DS} of S_4 in the new CSI circuit, (d) V_{DS} of S_4 in the conventional CSI circuit (all voltages are scaled at 20V/div).



(a) (b)

Figure 4-17. Experimental results of the conventional and new CSI circuit. (a) I_{in} of the new CSI circuit (500 mA/div), (b) I_{in} of the conventional CSI circuit (500 mA/div).

experimental results. From the experimental results, it was found that N-cell dc-dc converter circuits have smaller ripple at the output for the same operating condition. The new CSI circuit constructed from basic switching cells experiences much smaller voltage stress across the transistors and thereby, it increases the reliability of the circuit. However, the most advantageous part of the switching cell concept is that it creates a new vision to analyze the conventional power electronic converters by dividing them into smaller modular blocks. This modeling approach is not limited to the use of basic switching cells for analysis of existing power electronic circuits. Rather, it is a means to find different modular patterns in power electronic circuits, which can lead to several new circuit topologies.

CHAPTER 5

A NEW MULTILEVEL MODULAR CAPACITOR CLAMPED DC-DC CONVERTER

Several multilevel dc-dc converter technologies have been discussed in Chapter 3. These converters are based on flying capacitor technology, traditional switched-capacitor technique, charge pump circuit, or even voltage multiplier topology. Some of the topologies are practically suitable for low power applications only, and many of the topologies cannot provide bi-directional power transfer for high power automotive applications. As a result, no optimum topology was found that meets the criteria of performing in high power applications with very high efficiency. Thus, the major objective of this research was to derive a novel dc-dc converter topology that does not use any inductive elements in the circuit. The present discussion will introduce a new topology of multilevel dc-dc converter that will be shown to be an optimum solution for high power applications meeting many advantageous features.

There are many switched-capacitor dc-dc converters invented and proposed in the past. Most of the converters can be grouped into two main categories- series parallel converter and flying capacitor converter. The invention of the series parallel converter was a real breakthrough because of its several advantageous features. However, it was not free from its limitations. The flying capacitor dc-dc converter is comparatively a newer addition in switched-capacitor converter family. There are many other reported

topologies that are based on these two basic approaches.

In high power applications, the series parallel switched capacitor converter had many advantages such as inherent charge balancing feature of the capacitors, easier construction, and uniformity [21]. There are only two switching states present in the circuit which are independent of the conversion ratio (CR) of the converter. Moreover, the circuit can achieve high efficiency (>90%). However, there are some limitations of the converter that may prevent it from being used in high power applications. First, the circuit does not have a perfect modular construction, and the voltage stress across the transistors depends on at which level the transistors are located. Thus, it is not possible to get a common module that can be connected in cascade pattern to form the entire converter. The lack of bi-directional power flow is another key limitation that prevents the circuit to flow power from low voltage side to high voltage side. In addition, the lack of modularity is responsible not to get redundancy in the circuit, and the CR cannot be changed.

The second major category of the switched capacitor converter is the flying capacitor topology presented in [7], [25] – [27]. There is another modified version of it known as the magnetic-less multilevel dual voltage dc-dc converter presented in [28], [29]. The basic flying capacitor converter eliminates the voltage stress issue, and all the transistors in the circuit will experience the same voltage stress provided a startup procedure is applied in the converter operation. The major advantage of this topology is high operating efficiency, and efficiency more than 98% was reported in [7]. A second key advantage of the converter is the ability to flow power in both directions. Thus,

power can flow from the high voltage side to the low voltage side or vice-versa. However, the actual direction of power flow will depend on the two end voltages as the CR of the converter is fixed. This means that, if the high voltage side voltage is higher than the low voltage side voltage times the CR, power will flow from high side to low side, and power flow direction will be reversed if the high side is less than the product of CR and low side voltage.

The flying capacitor circuit also suffers from several limitations that create the driving force to develop a new topology. The flying capacitor circuit is not modular; the circuit cannot be easily extended to increase/decrease the number of levels, hence changing the CR. The other limitation of this converter is the excessive forward voltage drop across the transistors or diodes connected in series. From the schematic of a 4-level converter shown in [7], it is clear that the number of series connected devices (transistor/diode) is equal to the CR of the circuit. Thus, for a circuit with higher CR, the output voltage will suffer from a significant voltage regulation which is caused by the voltage drop across the transistors or diodes as the load current will flow through them. Moreover, the circuit has limited component utilization, and this issue will be discussed in Chapter 7.

The modified flying capacitor converter shown in [28] has a mesh pattern, and it is built from a unit module. However, for any CR, the circuit requires a large number of transistors compared to the series parallel or traditional flying capacitor converter. In the series parallel converter, the total number of transistors is (3N – 2), and this is 2N for the flying capacitor converter when N is the CR. However, for the modified flying capacitor

converter, this number is N(N+1). Moreover, similar to the flying capacitor converter, the circuit does not have a true bi-directional power management where the power flow should not depend on the high or low side voltages.

The converter proposed in [30] is known as the bi-directional switched capacitor converter. Structurally it can be viewed as a modified version of the series parallel converter; however, the operating principle is completely different. However, the circuit suffers from several limitations. One of the transistors in the circuit needs to operate in linear region for proper capacitor charging. For this reason, the overall efficiency of the circuit is limited to 85%. In addition, the literature does not mention any modified design guide to achieve CR more than 2. Thus, for high power application with high CR, the circuit does not seem to be suitable.

The operating principle of the Fibonacci converter presented in [33] is another example of a converter that has an operating principle similar to the flying capacitor topology. The main advantage of the converter is that it is possible to obtain a high CR from limited number of transistors or capacitors. However, the major limitation of Fibonacci converter is the incapability to obtain a CR beyond the values of the Fibonacci series. The other major disadvantage is that the circuit is capable of flowing power only from high voltage side to low voltage side.

The converter shown in [37] is known as the switch mode step up dc-dc converter. Basically it is based on a series parallel converter where power can only flow from low side to high side. Also, two of these circuits are connected in parallel and operated in two phases so that the output and input current become continuous. However,

the circuit is not modular, and it is not easy to change the CR. Moreover, the power flow direction is fixed, and the efficiency of the circuit was limited (80%).

From the various converters discussed above, a conclusion can be made that none of the converters has optimized characteristics such that it can be used in high power electronics with many desired features. After reviewing the various advantages and limitations of the converters, an enumeration of the features for the new converter can be made as follows.

1. The converter should be modular and can be extended to change the CR.

2. The voltage stress across the transistors should be evenly distributed so that a common module can be defined and the common module can be connected in cascade to form the entire converter.

3. The converter should have bi-directional power handling capability so that the power flow direction can be controlled irrespective of the high side or low side voltage.

4. The circuit should have very high operating efficiency, preferably more than 95%.

5. The circuit should have improved voltage regulation.

6. The control mechanism and operating principle of the converter should be simple and easily realizable.

This list of desired features cannot be met with any single converter, rather it may be possible to take the suitable features from individual converters and combine them in a single topology. In this continuation, the modularity feature can be adopted from the series-parallel converter although the series-parallel circuit does not have a complete

modular structure. Comparing it with the other contenders, it is the best option to find any modularity. From the series-parallel schematic in [21], a three transistor cell can be extracted that will have one capacitor in it. The cell will look like the unit cell shown in the fourth type of converters in the list under consideration [30]. However, the cell to cell connection and operating principle of the new topology will be completely different from the circuit shown in [21]. Thus, these three transistor cells can be considered as the foundation of the new topology.

To meet the second criteria, the circuit should have some mechanism to distribute the high voltage stress among all the transistors. To implement it, the various capacitors used in the circuit need to hold different voltages, and this attribute can be found in the flying capacitor converters. This feature of flying capacitor converter is different from the series-parallel converter because in series-parallel converter, the capacitors have equal voltages, and the transistors withstand unequal voltage stress. Following this fact, the unique module that was found in the previous step must be connected in such a way that in a series path, at most three capacitors are connected, and the number of series connected capacitors should be independent of the CR of the circuit. Thus, the interconnection of capacitors in flying capacitor converter is used in the new topology.

To meet the third criteria, the new circuit should have true bi-directional power handling ability, and the flying capacitor converter is the closest match to it. Although in a flying capacitor converter, the power flow direction depends on the end voltages, the new topology will take advantage of its extension feature, and by changing the number of active modules or levels, true bi-directional power management can be established. In

this way, the configuration of the flying capacitor converter is adopted here to implement the true bi-directional power management. While using the flying capacitor topology, the new topology can possibly achieve very high efficiency, and it fulfills the fourth criteria.

The fifth and sixth criteria actually go hand in hand. The flying capacitor converter has as many sub-intervals as the CR. On the other hand, the series-parallel converter has only two. Thus, the new topology will have some mechanism so that there are only two sub-intervals or two current paths, and each path will work in every other sub-interval. However, the operating principle of the flying capacitor converter is such that it involves one charging-discharging operation of a set of capacitors in each sub-interval. Thus, it may be possible to make several mutually exclusive charge-discharge operations simultaneously. This method can be easily observed in a 6-level flying capacitor that was not proposed in any publication. If the 4-level converter shown in [7] is extended to a 6-level converter for analysis purpose only, it can be seen that the group of operations that take place in sub-interval 1, 3, and 5 are independent of the group of operations that take place in sub-interval 2 and 4. Following this fact, the new topology of a 6-level converter can be proposed such that multiple charge-discharge operations will take place simultaneously, and all the charge-discharge operations can be completed in two sub-intervals. To implement this concept, several capacitors charging circuits are connected in parallel, and eventually it reduces the number of active transistors or diodes in a series path and a better regulation can be obtained from the new circuit. The detailed configuration of the new topology will be discussed in a later section.

Capacitor clamped topology in power electronic converters has many applications

for its high efficiency as the energy transfer is performed with capacitors only. For the same amount energy transfer, the loss associated with a non-ideal capacitor is significantly less than what is associated with a non-ideal inductor. For a long time, the capacitor clamped topology is used in multilevel inverters in many forms [7], [21]. However, there is always a capacitor charge balancing issue in capacitor clamped converters. The new topology presented here is designed to meet the requirements in multilevel dc-dc converters with bi-directional power handling capability, compact design, better component utilization, redundancy, and overall high efficiency operation.

5.1 THE NEW TOPOLOGY:

Figure 5-1 shows the schematic diagram of the proposed multilevel modular capacitor clamped dc-dc converter (MMCCC) having a CR (CR) of 5, which means the high side voltage V_{HV} is five times of the low side voltage V_{LV}. This design is based on the capacitor clamped topology although the operating principle is quite different. In this literature, this converter is defined as a 5-level design considering the presence of 5 voltage levels in the circuit. This way of defining number of levels excluding zero voltage as a level is different from other multilevel circuits. Usually multilevel converters were primarily applied in inverter circuits where zero voltage is considered as an individual level. Following this fact, multilevel dc-dc converters with CR of 3 are defined as 4-level converters [7], [25] - [29].

The 5-level circuit shown in Figure 5-1 has some unique features that make this converter advantageous compared to the converters discussed in Chapter 3. This circuit is modular, and the CR depends on the number of modules used in the circuit. The circuit

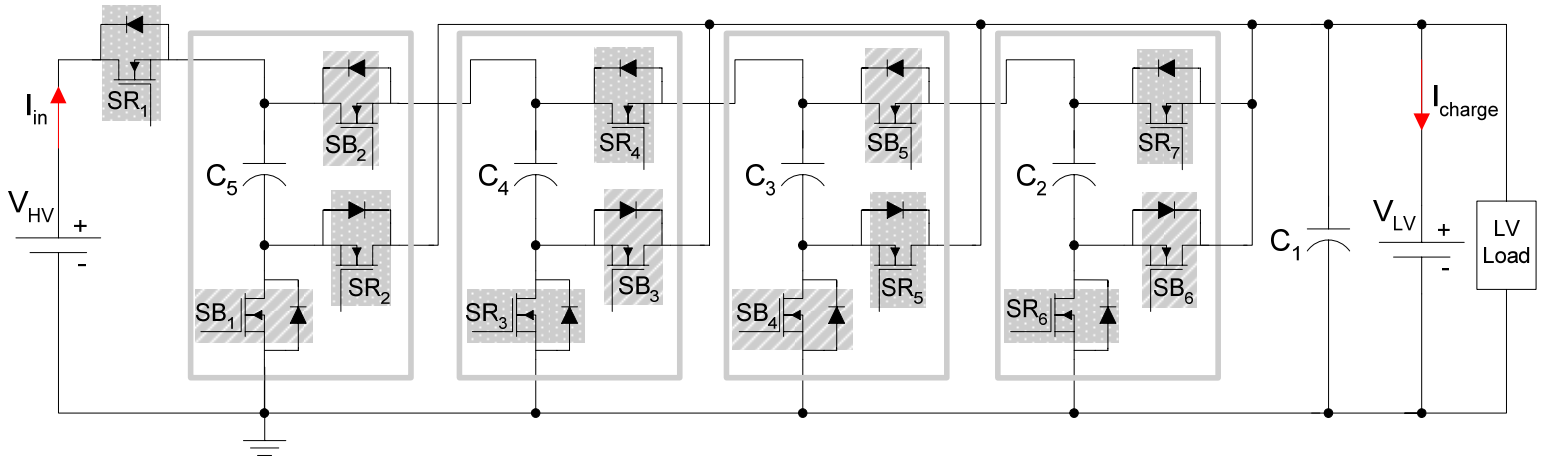


Figure 5- 1. The proposed 5-level MMCCC with four modular blocks.

shown in Figure 5-1 was designed primarily to manage power flow between two different dc bus voltages V_{HV} and V_{LV}. However, this converter would also work as a conventional dc-dc converter with one source connected at one end and a load at the other end. The present design has 4 modules that produce a CR of 5.

Thus for an N-level converter, N-1 modules are required in the circuit. Figure 5-2 shows one individual module used in the circuit. Each modular block has one capacitor and three transistors leading to three terminal points. The terminal V_{in} is connected to either the high voltage battery or to the output of the previous stage. One of the output terminals V_{next} is connected to the input of the next stage. The other output terminal V_{LV} is connected to the low voltage side + battery terminal. When a conventional flying capacitor multilevel dc-dc converter (FCMDC) comes with a CR of 5, the total operation takes 5 sub-intervals [17], which is shown in Figure 3-3 (this figure shows three sub-intervals for a three level converter) and Table 5-1. It is seen that only one charge-

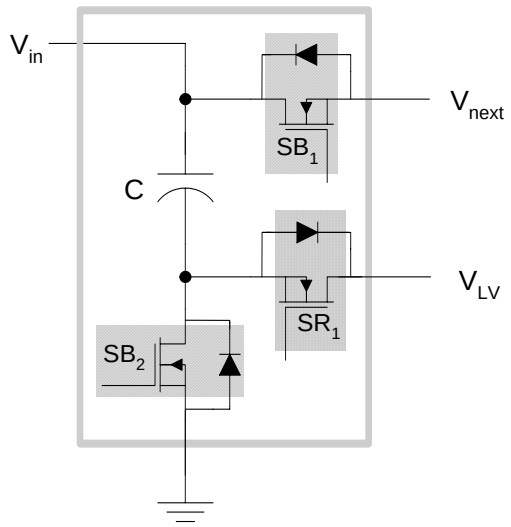


Figure 5-2. The unique modular block (the three transistor cell) of the MMCCC circuit.

Table 5-1. A comparison of the capacitor charge-discharge profile of the FCMDC and MMCCC. The operations that took place in 5 sub-intervals in an FCMDC are executed in only two sub-intervals in an MMCCC. ↑ = charging, ↓ = discharging.

FCMDC		MMCCC	
Sub interval No.	Operations	Sub interval No.	Operations
1	$V_{HV\rightarrow} C_5\uparrow + C_1\uparrow$	1	$V_{HV\rightarrow} C_5\uparrow + C_1\uparrow$ $C_4\downarrow \rightarrow C_3\uparrow + C_1\uparrow$ $C_2\downarrow \rightarrow C_1\uparrow$
2	$C_5\downarrow \rightarrow C_4\uparrow + C_1\uparrow$		
3	$C_4\downarrow \rightarrow C_3\uparrow + C_1\uparrow$		
4	$C_3\downarrow \rightarrow C_2\uparrow + C_1\uparrow$	2	$C_5\downarrow \rightarrow C_4\uparrow + C_1\uparrow$ $C_3\downarrow \rightarrow C_2\uparrow + C_1\uparrow$
5	$C_2\downarrow \rightarrow C_1\uparrow$		

discharge operation is performed in one sub interval. Thus, the component utilization is limited in this circuit. For an N-level converter, any capacitor except C_1 is utilized during only two sub-intervals for a complete cycle (one sub interval for charging, one for discharging) and for the remaining three sub-intervals in one period, the component is not used. Whereas the new converter introduced here increases the component utilization by performing multiple simultaneous operations shown in Table 5-1.

In Figure 5-3, the simplified operational circuit of the MMCCC is shown at different sub-intervals of operation. To achieve the new switching scheme, it is initially assumed that the new converter will perform the entire operation in 5 sub-intervals and later on it will be shown how these five operations can be done in only two sub-intervals.

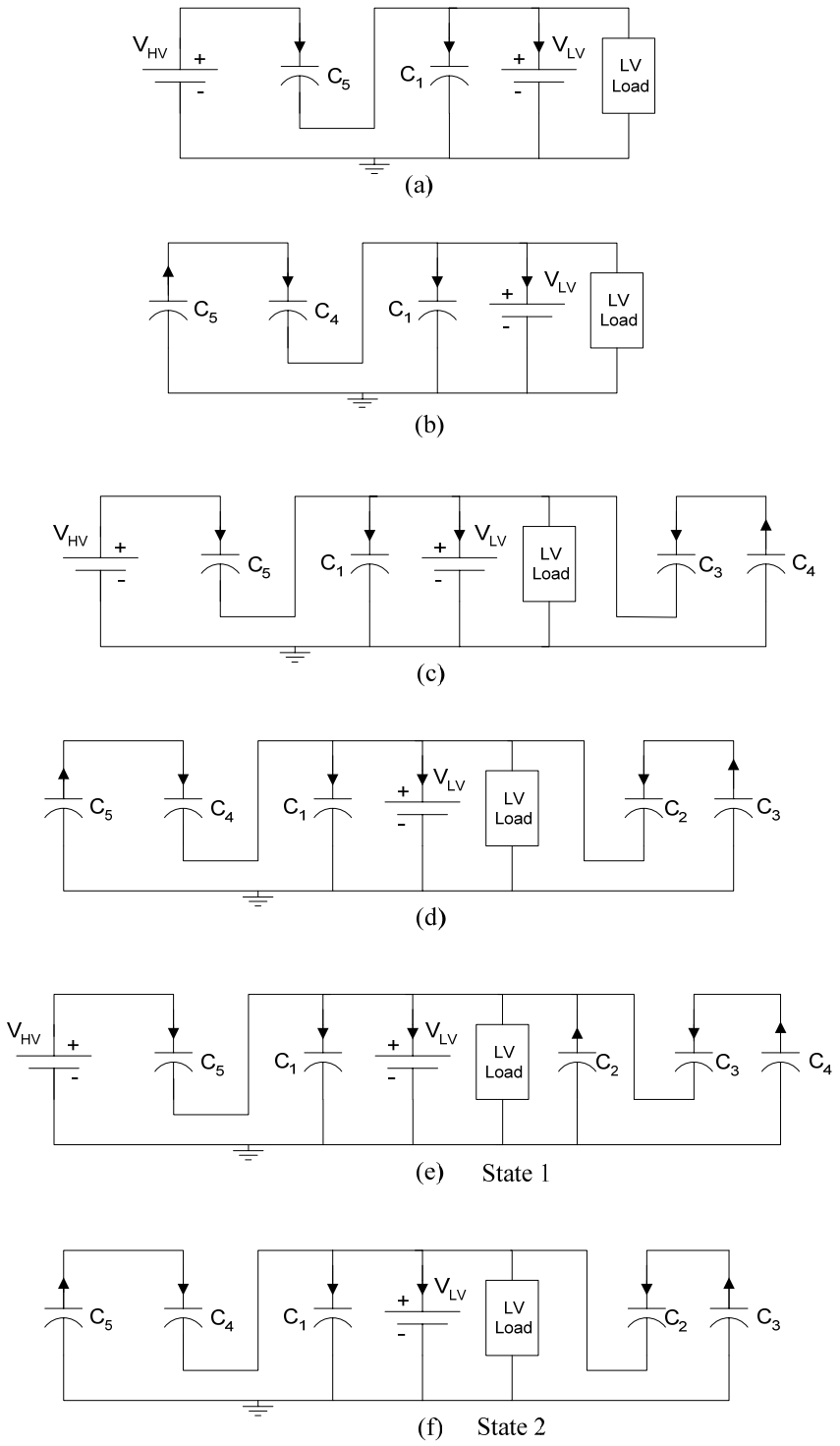


Figure 5-3. The simplified operational diagram of the MMCCC. Step 5 (shown in (e)) and step 6 (shown in (f)) become state 1 and state 2 in steady state operation of the MMCCC circuit.

Figure 5-3(a) shows the first sub-interval where C_5 is being charged from V_{HV} through the output circuit. In the second sub-interval, C_5 will transfer the charge to C_4 through the output circuit (in Figure 5-3(b)). During the third sub-interval, C_4 releases energy to C_3 through the output circuit (shown in Figure 5-3(c)). So far, these operations are the same as the conventional FCMDC. However, during this third sub-interval, the charging operation of the first sub interval (C_5 is charged from V_{HV} through the output circuit) can be performed without perturbing the operation of the entire circuit, which is shown in Figure 5-3(c) also. Thus in this stage, two operations are performed at the same time, and C_5 is charged for the second time through the output circuit.

During the 4th sub-interval, the same operation of Figure 5-3(b) can be performed. In addition, C_3 can transfer energy to C_2 through the output circuit without perturbing the entire operation. Thus, two operations can take place at the same time. These operations are shown in Figure 5-3(d). In this way, all the steps shown in Figure 5-3(a) to (d) are the initialization steps where all the capacitors are being charged and ready to transfer to the steady state operating conditions.

In the fifth stage shown in Figure 5-3(e), C_5 is again energized from V_{HV}, and C_4 transfers energy to C_3. C_2 was charged in the previous stage, and now it transfers the energy to the output circuit. Thus three independent operations take place at the same time. The operations shown in Figure 5-3(d) are repeated again in the sixth step, which is shown in Figure 5-3(f). Thus, these two steps shown in Figure 5(e) and (f) are the steady state operations of the converter where the 4th step and the 6th step are the same. The simplified diagram shown in Figure 5-3(e) is defined as state 1 during steady state, and

the diagram in Figure 5-3(f) shows state 2 of steady state operation. Once all the capacitors are charged after the initialization stage, the circuit enters into steady state and state 1 and state 2 will be repeated in every clock cycle.

The switching sequence in the new converter works in a simpler way than the conventional converter. As there are only two sub-intervals, two switching states are present in the circuit. Following this fact, switches SR_1 to SR_7 in Figure 5-1 are operated at the same time to achieve state 1; the equivalent circuit is shown in Figure 5-3(e). Similarly, switches SB_1 to SB_6 are operated simultaneously to achieve the steady state, whose equivalent circuit is shown in Figure 5-3(f). This new switching pattern is depicted in Figure 5-4.

5.2 SUMMARY FEATURES OF THE MMCCC TOPOLOGY

The MMCCC circuit has several key features that make it advantageous over the other capacitor clamped or switched-capacitor circuits. The MMCCC circuit has a modular structure, and it exhibits redundancy and fault bypass ability. Because the MMCCC topology is based on the capacitor clamped method, it results in low voltage stress across the transistors and the entire power handling capacity of the converter is uniformly distributed among the transistors allowing it to operate conveniently at high output power.

Another key feature of the MMCCC converter is the ability of accommodating connections of multiple sources and loads in the circuit. The modular nature of the circuit introduces several intermediate nodes in the circuit, and several voltage sources or loads can be connected to them, thus permitting its use in future fuel cell vehicles, and in

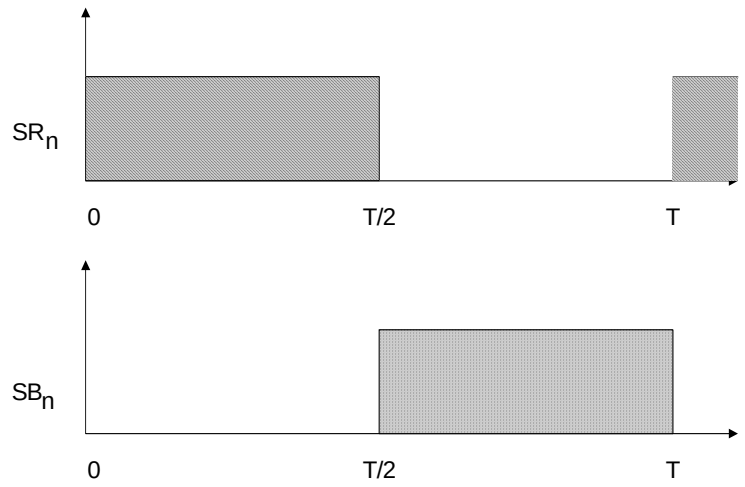


Figure 5-4. The gating signal of the switches in the new circuit, i.e. there are only two switching states present in the circuit.

integrating multiple sources, loads and establishing a complete power management system.

Another important feature of the MMCCC topology is the bi-directional power handling capability, a key requirement in future fuel cell automobiles. The requirement of bi-directional power management is described in Chapter 1, and the MMCCC topology may completely facilitate the application where bi-directional power management is required. Along with this feature, the MMCCC topology has a better component utilization compared to other capacitor clamped converters. In addition, the operating principle is simpler. However, the different key features of the MMCCC topology will be thoroughly discussed in Chapter 7 with supporting experimental results.

5.3 LIMITATIONS OF THE MMCCC TOPOLOGY

The MMCCC circuit has 2 detractions.

5.3.1 GREATER NUMBER OF TRANSISTORS

The MMCCC circuit uses more transistors than what is required for the conventional FCMDC with the same CR (except for CR = 2). For an N-level design, the conventional converter requires 2N transistors whereas the MMCCC circuit needs (3N-2) transistors. Thus for a five level design, the FCMDC circuit needs 10 transistors in contrast to 13 transistors needed for the MMCCC circuit. However, the need for more transistors is more than offset by many desirable features the new converter exhibits.

5.3.2 TRANSISTORS WITH HIGH BREAKDOWN VOLTAGE

In a conventional FCMDC circuit, the maximum voltage stress across any transistor is V_{LV} considering a startup circuit is used [32], [37]. In contrast, in the MMCCC circuit, (N-2) transistors have to withstand a voltage stress of 2 V_{LV} in an N-level design. Thus for a 5-level design, 3 transistors (SB_2, SR_4 and SB_5; one transistor in each of the three modules) are to be rated at 2 V_{LV}. The remaining 10 transistors are to be rated at V_{LV}. Although some transistors in the MMCCC circuit have higher voltage rating, the overall VA rating of the installed transistors is 36% less than what is required for a FCMDC circuit. The quantitative analysis of this feature will be presented in Chapter 7.

5.4 SIMULATION RESULTS

A 6-level converter was simulated in PSIM 6.0 to primarily validate the concept. For comparison, a 6-level FCMDC circuit was also simulated. Both were simulated in three modes as listed in Table 5-2. To compare the various attributes, both of the circuits

were simulated in down-conversion, up-conversion and battery charging mode. In down-conversion mode, a voltage source V_{HV} is connected at the high voltage side and a load is connected at the low voltage side. In up-conversion mode, a voltage source (12 V) is connected at the low voltage end and a load is connected at the high voltage end. In the battery- charging mode, the converter works in the down-conversion mode. A voltage source is connected at the high voltage side, and rather than a load, a 12 V battery is connected at the low voltage side.

There are some issues that were deliberately not considered while carrying out the simulations. In the battery charging mode, the low voltage side battery terminal voltage changes with time because the battery is taking charge. However, in the simulation, the battery voltage was considered constant. For this reason, a constant charging current was achieved in the simulation during the battery charging mode. However, in real situation,

Table 5-2. Simulation setup in different modes of operation

Mode	V_{in} (V)	Output load Impedance	Battery Voltage
Down-conversion ($V_{in} = V_{HV}$)	75	1 Ω	NA
Up Conversion ($V_{in} = V_{LV}$)	12	30 Ω	NA
Down-conversion with battery charging ($V_{in} = V_{HV}$) (V_{LV} = 12 V)	80	NA	12 V

this charging current gradually decreases as the battery voltage increases.

5.4.1 DOWN-CONVERSION MODE

The simulation results of the FCMDC and MMCCC in down-conversion mode are shown in Figure 5-5. With a 75 V input voltage and a CR of 6, the output voltage of both the converters should be 12 V. In Figure 5-5(a), the output voltage of an FCMDC is shown to be close to be only about 8.2 V. In contrast, the MMCCC circuit delivers an output voltage close to 12 V; near the theoretical level of output. Figure 5-5(c) and (d) compare the input current of the two designs. These simulation results clearly show that the peak current stress for the MMCCC circuit is only about 40% of that of the FCMDC circuit. This feature ensures higher reliability and the freedom of using smaller size

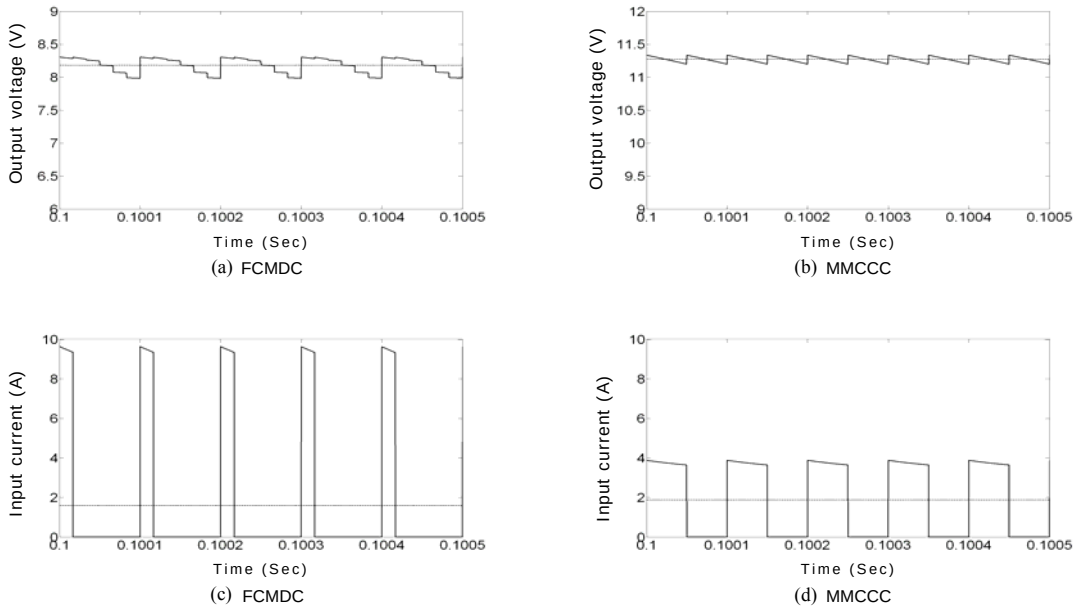


Figure 5-5. Comparison of simulation results in down-conversion mode. (a) the output voltage of the FCMDC, (b) the output voltage of the MMCCC, (c) the input current of the FCMDC, (d) the input current of the MMCCC. The higher output voltage and the lower peak current stress are achieved in the MMCCC circuit.

transistors.

5.4.2 UP-CONVERSION MODE

Figure 5-6 shows the simulation results in the up-conversion mode. When the low voltage side is energized by a 12 V source and the high voltage side is loaded by a 30 Ω load, the conventional converter produces an average output of only 37 V while the MMCCC circuit produces a voltage very close to 60 V. They are shown in Figure 5-6(a) and (b) respectively. Figure 5-6(c) and (d) compare the input currents taken from the 12 V source. It is also evident that the ripple present in the output of MMCCC is substantially less than the FCMDC converter. Moreover, more power from the 12 V

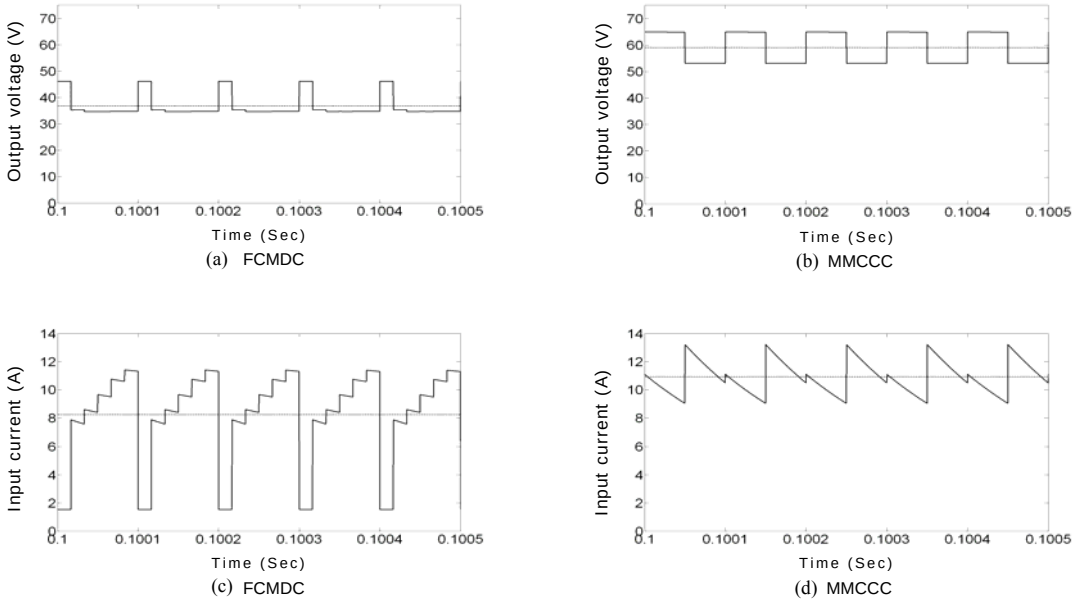


Figure 5-6. Comparison of simulation results in up-conversion mode. (a) the output voltage of the FCMDC, (b) the output voltage of the MMCCC, (c) the input current of the FCMDC, (d) the input current of the MMCCC. For the same input voltage, the MMCCC circuit produces about 50% more voltage, and exhibits reduced input current ripple.

source is transferred to the high voltage side by the MMCCC circuit. By virtue of the higher component utilization, the MMCCC delivers more power than the FCMDC using the same components.

5.4.3 BATTERY CHARGING MODE

Figure 5-7(a) to (d) compare the simulation results in the battery charging (down-conversion) mode. They clearly show that the average output charging current of the MMCCC is substantially higher than the conventional circuit although the input (high voltage side) peak current is comparable for both cases. The charging current of the MMCCC circuit is higher because the generated voltage at the low voltage side is

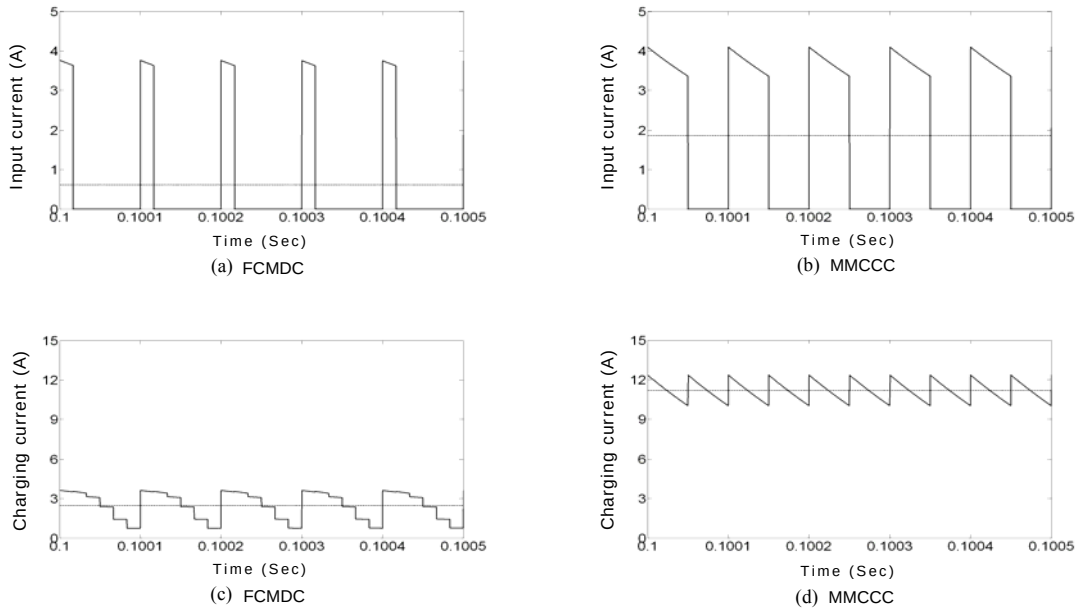


Figure 5-7. Simulation results in battery-charging mode. (a) the input current of the FCMDC, (b) the input current of the MMCCC, (c) the charging current of the FCMDC, (d) the charging current of the MMCCC. The MMCCC circuit provides higher charging current compared to the FCMDC circuit.

Higher than that of the FCMDC circuit for the same input voltage. Moreover, the ripple component present in the current for the MMCCC converter is significantly less than that of FCMDC circuit.

5.5 CHAPTER SUMMARY

A new topology of capacitor clamped dc-dc converter has been presented with simulation results. The basic operating principle of the converter has been explained and the key features have been briefly mentioned. It was shown how the MMCCC circuit can complete the charge-discharge operation of the capacitors in only two sub-intervals, and this number of sub-intervals is independent of the conversion ratio of the converter. In contrast to FCMDC circuit, this feature of the MMCCC topology can achieve simpler gate driver circuit and easier control mechanism. Through the simulation results, the concept of the MMCCC topology has been verified, and the performances of the MMCCC circuit were compared with the FCMDC topology. The simulation results support the claim that the MMCCC circuit produces higher voltage, and it can deliver more power than the FCMDC circuit while using components of equal ratings. Moreover, the MMCCC circuit exhibits some additional features that are not available from the FCMDC circuit.

In continuation of this discussion, Chapter 6 will show the analytical derivation of various capacitor voltages during start up and steady state operation. Eventually, these capacitor voltages will decide the voltages at the high and low voltage end of the converter. Once these capacitor voltages are calculated, the output voltages in up and down conversion mode can be calculated also. In addition, this analysis will explain how

the different nodes of the converter attain the normal operating voltages and it will also show the voltage variations at load during steady state. Finally, Chapter 7 will present a discussion of the key features of the MMCCC converter with experimental results.

CHAPTER 6

ANALYTICAL MODELING OF THE MMCCC

Chapter 5 has presented the MMCCC topology, and the concept has been supported by the simulation results. However, for a completeness of the proof of concept, an analytical derivation that comprises the voltage equations and charge transfer behavior of the capacitors is presented in this chapter. The first part of the analytical derivation, which is the startup analysis will show how the capacitors inside the converter attain the normal operating voltages beginning from zero voltage. Once the startup step is completed, the circuit operates in the steady state. The second part of the analytical derivation is the steady state analysis of a 5-level MMCCC that shows the voltage variations of the capacitors when a load is connected at the output. The third part consists of the steady state analysis of a 4-level MMCCC. Validating with experimental results would be the last step of the proof of concept analysis, and it will be presented in Chapter 7.

6.1 OUTLINE OF THE ANALYSIS

There are many reported methods of deriving the analytical model of a power electronic converter. The approach presented in [25] shows the capacitor loss modeling of the flying capacitor converter. In [26], the peak current stresses through the active devices were discussed. However, the analysis presented in [28] shows a sequential method to estimate the capacitor voltages for a flying capacitor converter, and a similar

analysis method will be used to derive a steady state model for the MMCCC converter.

To find an example of startup analysis, several publications [51] - [53] were reviewed. These papers present a dynamic analysis method for the multilevel "Imbricated Cell" or multicell inverters. Thus, these papers could not be considered as a suitable choice to proceed with the startup analysis for MMCCC. The method presented in [54] was a dynamic analysis of a switched-capacitor converter, and the paper also presents an analytical approach of the frequency response of the circuit. The dynamic analysis was formulated in a matrix form and it seemed to be very close to the computing method for the MMCCC circuit.

When the operating frequency of the converter becomes very high, the time constant τ of the capacitors used in the circuit becomes comparable to the time period of the converter. In this case, the state-space averaging technique presented in [55] may be suitable for the analysis. As the MMCCC converter is operated at a lower frequency and the τ of the capacitors is much smaller than the time period, the state-space averaging method can not be used and a simpler method will be adopted instead.

Considering all the methods discussed in this section, several assumptions were made prior to the actual derivation steps for a simple and complete expression. These assumptions were,

1. The on-state resistances of the switching MOSFETs are zero.

2. The equivalent series resistances (ESR) of the capacitors are zero.

3. The load is not connected at the output during the startup time.

The MMCCC topology is based on the capacitor-clamped converter circuit. Thus,

energy is transferred from high voltage side to low voltage side (or vice-versa) through capacitors only. For this reason the voltage stresses across the transistors will entirely depend on the various capacitor voltages in the circuit. From Figure 6-1, it can be seen that the low-voltage side voltage is actually the voltage across C_1. In the same way, the high-voltage side voltage (V_{HV}) is the total voltage of C_5 and C_1 connected in series [Figure 5-3(e)]. Thus, if an expression can be found for all the capacitor voltages, then all the working voltages such as V_{LV}, V_{HV}, and the voltage stresses across the transistors can be determined. In this way, the concept of the MMCCC topology can be verified through analytical derivations.

The startup analysis presented here has been made considering the MMCCC in a 5-level configuration. It will be explained later that when the conversion ratio is even, the time ratio of state 1 and state 2 is 1:1. However, for odd conversion ratio such as 5, this ratio is 3:2. These time factors decide the capacitor voltages during steady state because the load is connected during that time. On the other hand, during the startup process, these ratios do not have any impact. Following these facts, the startup analysis is applied

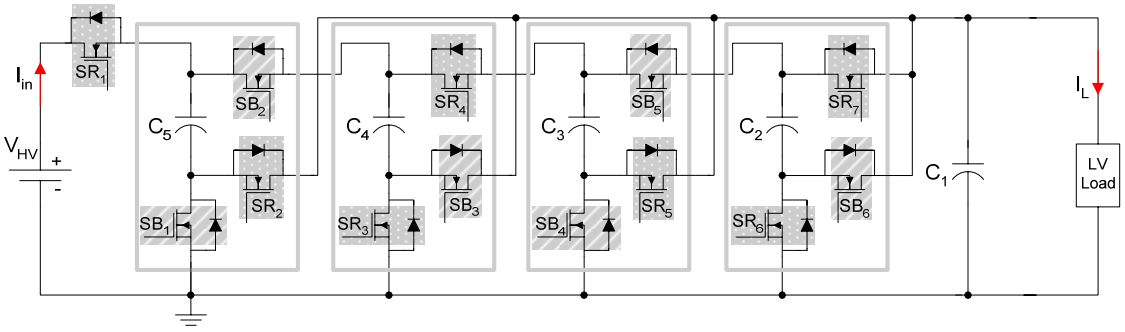


Figure 6-1. The schematic diagram of a 5-level MMCCC circuit.

to a 5-level converter. In addition, the steady state analysis is done for 5 and 4-level configurations covering the different time ratios of state 1 and state 2. If the circuit works for one odd and one even conversion ratio, a conclusion can be made that it will work for any conversion ratio.

There is one more important issue that needs to be stated before initiating the analytical derivation. The ESR of any capacitor used in the circuit is one of the components responsible for the time constant τ of the capacitor charging-discharging profile. For all the capacitors used in the circuit, τ was around 10e-6, and this value is much smaller than the time duration of state 1 or state 2. For this reason, the charging profile of the capacitors does not depend on the time duration of state 1 or state 2 in various conversion ratios. Using this advantage, the startup analysis estimates that at the end of a sub-interval (state 1 or 2), the capacitor charge-discharge operation is completed.

It was mentioned in Chapter 5 that the MMCCC topology is inherently modular. Thus all the capacitors used in the circuit have the same value to make all modules compatible and interchangeable. This can introduce a phenomenal simplicity in the analytical derivation of startup and steady state operation. Thus, for the startup and steady state analysis, $C_1 = C_2 = C_3 = C_4 = C_5 = C$.

6.2 STARTUP ANALYSIS OF A 5-LEVEL MMCCC

This analysis and step by step procedure will show how a 5-level MMCCC converter is started sequentially to avoid any potential damage to the transistors used in the circuit. The schematic diagram of a 5-level MMCCC is shown in Figure 6-1. In steady state, these 13 transistors are operated in two states- state 1 and state 2. The

operational diagrams of state 1 and state 2 are shown in Figure 6-2. Seven transistors are activated in state 1, and six transistors in state 2. In these steady states, the capacitors have nominal average dc values, and the voltage stresses across the transistors are either 1 V_{LV} or 2 V_{LV}. However, if the startup process is bypassed, the converter will try to build up the rated output voltage beginning from zero voltages across the capacitors. This will cause excessive voltage stress across the transistors when they are switched off. This is why a systematic startup process is needed, and done in such a way that all of the transistors experience the rated V_{DS} that they experience during normal operating conditions.

6.2.1 STEP 1 OF THE STARTUP PROCESS

The operation of this step is shown in Figure 6-3(a). In this step, capacitor C_1 and C_2 are connected to the V_{LV} source. From Figure 6-1, it is clear that C_1 is always connected to V_{LV}, and the other capacitors are interconnected among themselves depending on the state of operation. In step 1, no other capacitor is charged or discharged.

Thus the voltage equations of the capacitors would be,

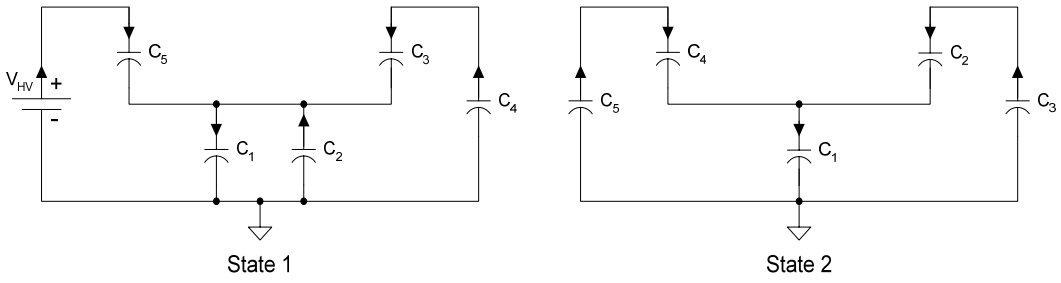


Figure 6-2. The steady state operational diagrams of a 5-level MMCCC.

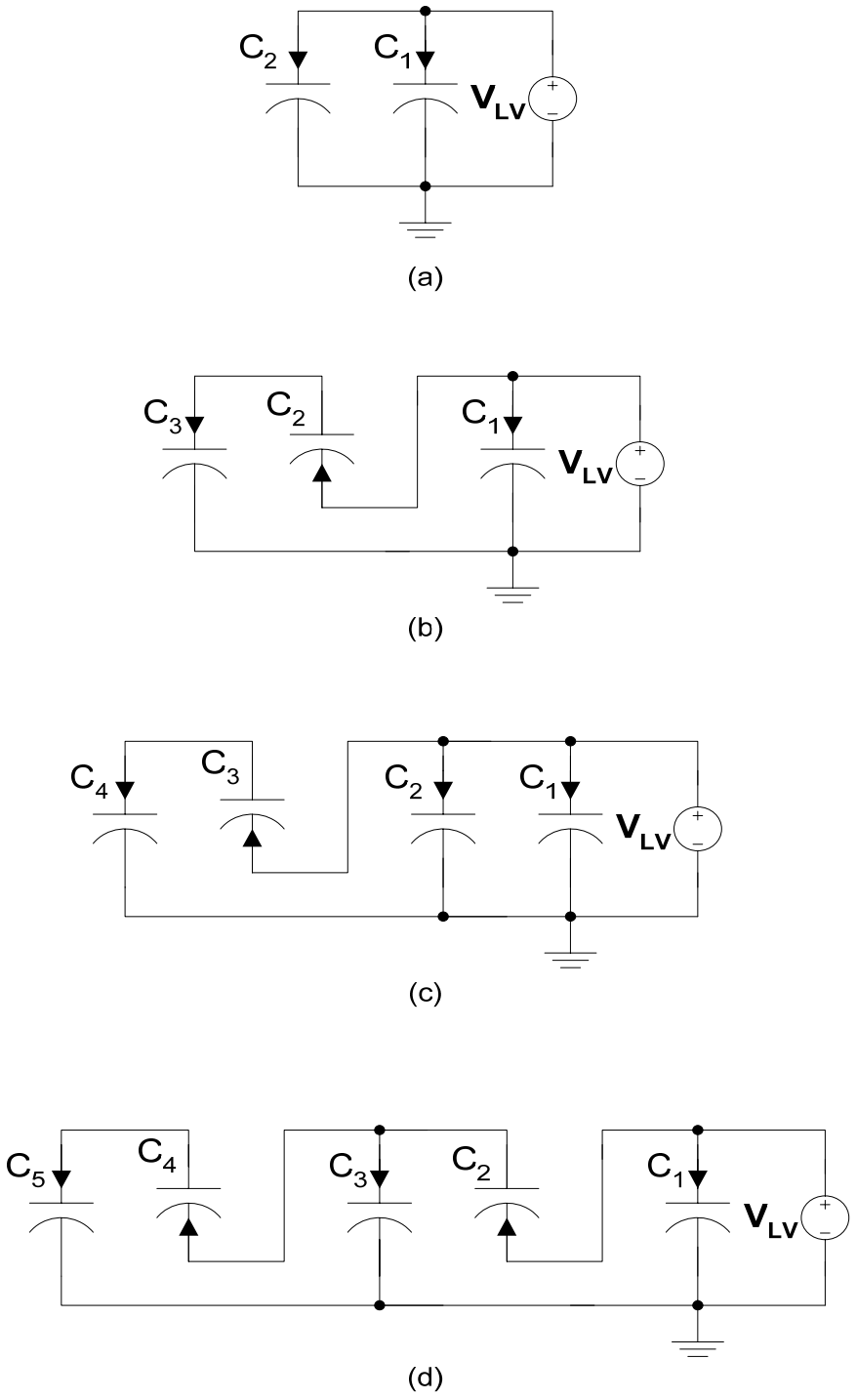


Figure 6-3. The operational diagrams of the startup process of MMCCC. a) step 1, b) step 2, c) step 3, and d) step 4.

$$V_{C1}(t_1) = V_{C2}(t_1) = V_{LV},$$
$$V_{C3}(t_1) = V_{C4}(t_1) = V_{C5}(t_1) = 0. \tag{6.1.1}$$

6.2.2 STEP 2 OF THE STARTUP PROCESS

This step involves the discharging operation of C_2 and the charging operation of C_3. The operation is shown in Figure 6-3(b). Thus, only C_1, C_2 and C_3 are involved in this step, and C_4 and C_5 are left unused. When there is a charge transfer from one capacitor to another, the amount of transferred charge (and thereby the voltage variation) depends on the capacitor voltages that were present before the transfer operation is established. Following this fact and using (6.1.1),

$$\begin{aligned}
&V_{C1} = V_{LV},\\
&V_{C2}(t_2) = V_{C2}(t_1) - [V_{LV} + V_{C2}(t_1) - V_{C3}(t_1)] \bullet \frac{C_3}{C_2 + C_3} = V_{C2}(t_1) - V_{LV} = 0,\\
&V_{C3}(t_2) = V_{C3}(t_1) + [V_{LV} + V_{C2}(t_1) - V_{C3}(t_1)] \bullet \frac{C_2}{C_2 + C_3} = V_{C3}(t_1) + V_{LV} = V_{LV},\\
&V_{C4} = V_{C5} = 0.
\end{aligned} \tag{6.1.2}$$

6.2.3 STEP 3 OF THE STARTUP PROCESS

This operational diagram of this step is shown in Figure 6-3(c). In this step, charge is transferred from C_3 to C_4. C_2 is again connected to V_{LV} as in step 1. Thus, the voltage equations are,

$$\begin{aligned}
&V_{C1}(t_3) = V_{C2}(t_3) = V_{LV},\\
&V_{C3}(t_3) = V_{C3}(t_2) - [V_{LV} + V_{C3}(t_2) - V_{C4}(t_2)] \bullet \frac{C_4}{C_3 + C_4} = V_{C3}(t_2) - V_{LV} = 0,\\
&V_{C4}(t_3) = V_{C4}(t_2) + [V_{LV} + V_{C3}(t_2) - V_{C4}(t_2)] \bullet \frac{C_3}{C_3 + C_4} = V_{C4}(t_2) + V_{LV} = V_{LV},\\
&V_{C5}(t_3) = 0.
\end{aligned} \tag{6.1.3}$$

6.2.4 STEP 4 OF THE STARTUP PROCESS

So far, the propagating charge has reached to C_4. Thus, this step involves the operations that took place in step 2 in addition to the charge transfer from C_4 to C_5. The operational diagram of step 4 is shown in Figure 6-3(d), and the voltage equations are,

$$
\begin{aligned}
&V_{C1} = V_{LV},\\
&V_{C2}(t_4) = V_{C2}(t_3) - [V_{LV} + V_{C2}(t_3) - V_{C3}(t_3)] \bullet \frac{C_3}{C_2 + C_3} = V_{C2}(t_3) - V_{LV} = 0,\\
&V_{C3}(t_4) = V_{C3}(t_3) + [V_{LV} + V_{C2}(t_3) - V_{C3}(t_3)] \bullet \frac{C_2}{C_2 + C_3} = V_{C3}(t_3) + V_{LV} = V_{LV},\\
&V_{C4}(t_4) = V_{C4}(t_3) - [V_{LV} + V_{C4}(t_3) - V_{C5}(t_3)] \bullet \frac{C_5}{C_4 + C_5} = V_{C4}(t_3) - V_{LV} = 0,\\
&V_{C5}(t_4) = V_{C5}(t_3) + [V_{LV} + V_{C4}(t_3) - V_{C5}(t_3)] \bullet \frac{C_4}{C_4 + C_5} = V_{C5}(t_3) + V_{LV} = V_{LV}.
\end{aligned}
\tag{6.1.4}
$$

After these 4 steps, a conclusion can be made that in every odd indexed step (such as step 1, 3, 5 etc.), some additional charge-discharge operations take place on top of some operations that took place in the previous odd indexed step. This is why step 3 has some new operations in addition to the operations that took place in step 1. This fact is also true for even indexed steps.

6.2.5 STEP 5 OF THE STARTUP PROCESS

After step 4, all the capacitors are charged at least once. C_5 has been charged from C_4. In step 5, C_5 will be unused, and a charge transfer will occur among C_3 and C_4 like step 3. The operations that will take place in step 5 are exactly the same that took place in step 3. However, the voltage equations will be different because of the modified capacitor voltages at the beginning of step 5 which is different from the voltages the capacitors had at the beginning of step 3. Thus, the voltage equations are,

$$
\begin{aligned}
&V_{C1}(t_5) = V_{C2}(t_5) = V_{LV},\\
&V_{C3}(t_5) = V_{C3}(t_2) - [V_{LV} + V_{C3}(t_4) - V_{C4}(t_4)] \bullet \frac{C_4}{C_3 + C_4} = V_{C3}(t_4) - V_{LV} = 0,\\
&V_{C4}(t_5) = V_{C4}(t_4) + [V_{LV} + V_{C3}(t_4) - V_{C4}(t_4)] \bullet \frac{C_3}{C_3 + C_4} = V_{C4}(t_4) + V_{LV} = V_{LV},\\
&V_{C5}(t_5) = V_{C5}(t_4) = V_{LV}.
\end{aligned}
\tag{6.1.5}
$$

The five startup steps discussed so far are the initialization steps of the MMCCC operation. As mentioned earlier, in a 5-level MMCCC, 13 transistors are used, and they are operated in two sub intervals or states. The operations that take place in those sub-intervals are similar to those that occur in the startup steps discussed in this chapter. Among the five startup steps, step 4 can be compared with the state 2 (sub-interval 2) of the MMCCC. Also, the operations that take place in step 5 are almost the same that take place in state 1 (sub-interval 1) except that S_{R1} was activated in state 1, and here it is not.

The purpose of the initialization steps is to develop proper voltages across all the capacitors so that when the circuit is connected to V_{HV} through S_{R1}, the transistors used in the circuit experience the normal voltage stresses that they should experience during normal operating conditions. In Figure 6-1, S_{R7} and S_{R6} are turned on to activate step 1, and this ensures C_1 and C_2 connected across V_{LV}. In step 2, S_{B6}, S_{B5}, and S_{B4} are activated to transfer the charge from C_2 to C_3. Thus Table 6-1 can be made that shows the list of transistors that are operated during the initialization or startup steps of the converter.

Table 6-1 shows an important fact that links the initialization steps with the steady state operation of the converter. As mentioned earlier, the steady state operation of the converter involves the operation of the two sub-intervals state 1 and state 2. During state 1, S_{R1}-S_{R7} are turned on and in state 2, S_{B1}-S_{B6} are activated. Thus initialization step 4 is

Table 6-1. The active transistors and capacitors in the startup steps.

Step	Active transistors	Active capacitors
1	S_{R7}, S_{R6}	C_1, C_2
2	S_{B6}, S_{B5}, S_{B4}	C_1, C_2, C_3
3	S_{R7}, S_{R6}, S_{R5}, S_{R4}, S_{R3}	C_1, C_2, C_3, C_4
4	S_{B6}, S_{B5}, S_{B4}, S_{B3}, S_{B2}, S_{B1}	C_1, C_2, C_3, C_4, C_5
5	S_{R7}, S_{R6}, S_{R5}, S_{R4}, S_{R3}	C_1, C_2, C_3, C_4

exactly the same as the state 2 operation. Whereas, state 1 is little different from step 3 or 5, because S_{R1} or S_{R2} is not activated to prevent high voltage stress. Thus, after repeating step 3 and step 4 several times, the capacitor voltages reach to the steady state values. Once the capacitors attain the normal operating voltages, S_{R1} and S_{R2} can be safely activated in the corresponding states. Then the converter will start working in the normal mode, and the load can be connected at the output.

To prove the concept of the MMCCC topology, the circuit needs to be modeled based on the capacitor voltage variation and switching schemes. If the circuit works without any loss or voltage drop across any active or passive device, a 5-level MMCCC will have a V_{HV}/V_{LV} ratio of 5. At steady state, the capacitors should have voltages like the following:

$V_{C1} = V_{LV}$, $V_{C2} = V_{LV}$, $V_{C3} = 2\ V_{LV}$, $V_{C4} = 3\ V_{LV}$, $V_{C5} = 4\ V_{LV}$; where $V_{HV} = 5\ V_{LV}$

To model the 5-level MMCCC circuit, a general expression of the charge transfer and voltage variation needs to be developed. As a first step, using (6.1.2), the voltage equations in step 2 can be re-arranged as,

$$
\begin{aligned}
&V_{C1} = V_{LV},\\
&V_{C2}(t_2) = V_{C2}(t_1) - [V_{LV} + V_{C2}(t_1) - V_{C3}(t_1)] \bullet 0.5 = 0.5 \bullet [V_{C2}(t_1) + V_{C3}(t_1)] - 0.5V_{LV},\\
&V_{C3}(t_2) = V_{C3}(t_1) + [V_{LV} + V_{C2}(t_1) - V_{C3}(t_1)] \bullet 0.5 = 0.5 \bullet [V_{C2}(t_1) + V_{C3}(t_1)] + 0.5V_{LV},\\
&V_{C4} = V_{C5} = 0.
\end{aligned}
\tag{6.1.6}
$$

In the same way, the voltage equations in step 3 can be re-arranged like the following,

$$
\begin{aligned}
&V_{C1}(t_3) = V_{C2}(t_3) = V_{LV},\\
&V_{C3}(t_3) = 0.5 \bullet [V_{C3}(t_2) + V_{C4}(t_2)] - 0.5V_{LV},\\
&V_{C4}(t_3) = 0.5 \bullet [V_{C3}(t_2) + V_{C4}(t_2)] + 0.5V_{LV},\\
&V_{C5}(t_3) = V_{C5}(t_2).
\end{aligned}
\tag{6.1.7}
$$

And, at step 4, the voltage equations will be,

$$
\begin{aligned}
&V_{C1}(t_4) = V_{LV},\\
&V_{C2}(t_4) = 0.5 \bullet [V_{C2}(t_3) + V_{C3}(t_3)] - 0.5V_{LV},\\
&V_{C3}(t_4) = 0.5 \bullet [V_{C2}(t_3) + V_{C3}(t_3)] + 0.5V_{LV},\\
&V_{C4}(t_4) = 0.5 \bullet [V_{C4}(t_3) + V_{C5}(t_3)] - 0.5V_{LV},\\
&V_{C5}(t_4) = 0.5 \bullet [V_{C4}(t_3) + V_{C5}(t_3)] + 0.5V_{LV}.
\end{aligned}
\tag{6.1.8}
$$

Using (6.1.6), the capacitor voltages at the end of step 2 are,

$$
X_0 = \begin{bmatrix} V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C4} \\ V_{C5} \end{bmatrix} = \begin{bmatrix} V_{LV} \\ 0 \\ V_{LV} \\ 0 \\ 0 \end{bmatrix}. \tag{6.1.9}
$$

The values found from (6.1.9) will be used as the initial conditions for step 3; the voltages at the end of step 3 will be used as the initial voltages for step 4. As mentioned earlier, step 5 is the repetition of step 3, the circuit can be modeled using two repetitive operations described in step 3 and 4. Thus the operation in step 3 can be generalized as an operation for any odd indexed step. In the same way, step 4 can be considered as a

general operation for any even indexed step. For convenience, step 3 is defined as general start up state 1 (GSS 1) and step 4 is defined as general start up state 2 (GSS 2).

The reason for generalizing the system from step 3 and not from step 1 is because of the capacitor voltages. The equations used to generalize the system will work once the capacitors have reached the voltages shown in (6.1.2). Thus GSS 1 can be expressed in the following matrix form,

$$\begin{bmatrix} V_{C1}(k+1) \\ V_{C2}(k+1) \\ V_{C3}(k+1) \\ V_{C4}(k+1) \\ V_{C5}(k+1) \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0.5 & 0.5 & 0 \\ 0 & 0 & 0.5 & 0.5 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{C1}(k) \\ V_{C2}(k) \\ V_{C3}(k) \\ V_{C4}(k) \\ V_{C5}(k) \end{bmatrix} + \begin{bmatrix} 1 \\ 1 \\ -0.5 \\ 0.5 \\ 0 \end{bmatrix} V_{LV} . \qquad (6.1.10)$$

where k is the index of the step. In the same way, the generalized equations of GSS 2 in matrix form can be derived from (6.1.8). The form is,

$$\begin{bmatrix} V_{C1}(k+2) \\ V_{C2}(k+2) \\ V_{C3}(k+2) \\ V_{C4}(k+2) \\ V_{C5}(k+2) \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0.5 & 0.5 & 0 & 0 \\ 0 & 0.5 & 0.5 & 0 & 0 \\ 0 & 0 & 0 & 0.5 & 0.5 \\ 0 & 0 & 0 & 0.5 & 0.5 \end{bmatrix} \begin{bmatrix} V_{C1}(k+1) \\ V_{C2}(k+1) \\ V_{C3}(k+1) \\ V_{C4}(k+1) \\ V_{C5}(k+1) \end{bmatrix} + \begin{bmatrix} 1 \\ -0.5 \\ 0.5 \\ -0.5 \\ 0.5 \end{bmatrix} V_{LV} . \qquad (6.1.11)$$

From (6.1.10) and (6.1.11), GSS 1 can be considered as a system $y = Ax + b$, and GSS 2 can be considered as $z = Cy + d$

where $A = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0.5 & 0.5 & 0 \\ 0 & 0 & 0.5 & 0.5 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}$ $b = \begin{bmatrix} 1 \\ 1 \\ -0.5 \\ 0.5 \\ 0 \end{bmatrix} V_{LV}$

$$C = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0.5 & 0.5 & 0 & 0 \\ 0 & 0.5 & 0.5 & 0 & 0 \\ 0 & 0 & 0 & 0.5 & 0.5 \\ 0 & 0 & 0 & 0.5 & 0.5 \end{bmatrix} \qquad d = \begin{bmatrix} 1 \\ -0.5 \\ 0.5 \\ -0.5 \\ 0.5 \end{bmatrix} V_{LV}$$

$X_0 = \begin{bmatrix} V_{C1}(k) \\ V_{C2}(k) \\ V_{C3}(k) \\ V_{C4}(k) \\ V_{C5}(k) \end{bmatrix}$, where X_0 is the voltage vector at the end of step 2.

To get the capacitor voltages after several operations, the two operations GSS 1 and GSS 2 must be applied repetitively on the initial value of the capacitor voltages found from (6.1.9). At the end of step 4, the capacitor voltages would be,

$$z = Cy + d = C(Ax + b) + d = CAx + Cb + d$$

In the same way, the voltages at the end of step 5,

$$p = Az + b = A(CAx + Cb + d) + b = ACAx + ACb + Ad + b$$

This method of computing capacitor voltages suffers from one limitation. With more iterations, the state variables for capacitor voltages (x, z, p etc.) are taking the shape of a polynomial, and for large number of iterations, it will be quite difficult to get a finite form of the state variable.

However, if the system would be in the form $y = Ax$ and $z = Cy$, then the steady state capacitor voltage vector f after n iterations would be in the form of,

$f \equiv CACACACACACA.....x = (CA)^n x$, where the GSS 1 step has occurred n times and GSS 2 has applied n times to the system. Also, the final value that $(CA)^n$ converges to

has to be finite such that a further operation of GSS 1 or GSS 2 will not affect the steady state value $(CA)^n x$. In other words, when n is a very large number,

$$A(CA)^n \approx CA(CA)^n \approx ACA(CA)^n ..... \approx (CA)^n$$

To obtain a compact form of the final value, the matrix form found in (6.1.10) and (6.1.11) needs to be re-configured. In (6.1.10) and (6.1.11), the constant terms are responsible to have the polynomial form at the value of final output. As V_{C1} is always a constant having a value of V_{LV}, the two constant vectors in (6.1.10) and (6.1.11) can be expressed in terms of V_{C1}. Then we will get two new matrices A and C, where they will have dimensions 5×5. After doing that, the operation in GSS 1 and GSS 2 will look like the following,

$$\begin{bmatrix} V_{C1}(k+1) \\ V_{C2}(k+1) \\ V_{C3}(k+1) \\ V_{C4}(k+1) \\ V_{C5}(k+1) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ -0.5 & 0 & 0.5 & 0.5 & 0 \\ 0.5 & 0 & 0.5 & 0.5 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{C1}(k) \\ V_{C2}(k) \\ V_{C3}(k) \\ V_{C4}(k) \\ V_{C5}(k) \end{bmatrix}. \tag{6.1.12}$$

and

$$\begin{bmatrix} V_{C1}(k+2) \\ V_{C2}(k+2) \\ V_{C3}(k+2) \\ V_{C4}(k+2) \\ V_{C5}(k+2) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ -0.5 & 0.5 & 0.5 & 0 & 0 \\ 0.5 & 0.5 & 0.5 & 0 & 0 \\ -0.5 & 0 & 0 & 0.5 & 0.5 \\ 0.5 & 0 & 0 & 0.5 & 0.5 \end{bmatrix} \begin{bmatrix} V_{C1}(k+1) \\ V_{C2}(k+1) \\ V_{C3}(k+1) \\ V_{C4}(k+1) \\ V_{C5}(k+1) \end{bmatrix}. \tag{6.1.13a}$$

where

$$V_{C1}(k) = V_{C1}(k+1) = V_{C1}(k+n) = V_{LV}$$

Thus, (6.1.12) would be the final voltage equation for GSS 1, and (6.1.13a) would

be the final form of GSS 2. Now the new system has the following matrices,

$$A=\begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ -0.5 & 0 & 0.5 & 0.5 & 0 \\ 0.5 & 0 & 0.5 & 0.5 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \text{ and } C=\begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ -0.5 & 0.5 & 0.5 & 0 & 0 \\ 0.5 & 0.5 & 0.5 & 0 & 0 \\ -0.5 & 0 & 0 & 0.5 & 0.5 \\ 0.5 & 0 & 0 & 0.5 & 0.5 \end{bmatrix}. \quad (6.1.13b)$$

After n iterations of GSS 1 and GSS 2 each, the output voltage vector f is given as the following,

$$f=(CA)^n \bullet X_0 . \quad (6.1.14)$$

where, X_0 is the capacitor voltage matrix at the end of step 2. According to (6.1.9),

$$X_0=\begin{bmatrix} V_{LV} \\ 0 \\ V_{LV} \\ 0 \\ 0 \end{bmatrix}. \quad (6.1.15)$$

To get a closed form of the final voltage vector f, we need to estimate the value of $(CA)^n$. To do that, the matrix CA is considered first. Using (6.1.13b),

$$CA=\begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ -0.25 & 0 & 0.25 & 0.25 & 0 \\ 0.75 & 0 & 0.25 & 0.25 & 0 \\ -0.25 & 0 & 0.25 & 0.25 & 0.5 \\ 0.75 & 0 & 0.25 & 0.25 & 0.5 \end{bmatrix}. \quad (6.1.16)$$

This CA matrix can be analyzed using the eigenvalue decomposition method, and CA has a full set of eigenvectors and the largest eigenvalue is equal to 1. This is a clear indication of having a finite value of $(CA)^n$. Using linear algebra,

$$(CA)^n = VD^nV^{-1} \tag{6.1.17}$$

Where, V is the eigenvector matrix, and D is the diagonal matrix having the eigenvalues in the diagonal positions. After computing,

$$V = \begin{bmatrix} 0.1796 & 0 & 0 & 0 & 0 \\ 0.1796 & 0.2706 & 0.6533 & 0.6274 & 1 \\ 0.3592 & 0.2706 & 0.6533 & 0.5506 & 0 \\ 0.5388 & 0.6533 & -0.2706 & -0.5506 & 0 \\ 0.7184 & 0.6533 & -0.2706 & 0 & 0 \end{bmatrix}. \tag{6.1.18}$$

Taking the inverse of V,

$$V^{-1} = \begin{bmatrix} 5.5678 & 0 & -0.0000 & 0.0000 & -0.0000 \\ -5.7674 & 0 & 0.5412 & 0.5412 & 0.7654 \\ 0.8582 & 0 & 1.3066 & 1.3066 & -1.8478 \\ -1.8161 & 0 & 0.0000 & -1.8161 & 1.816 \\ 1.1394 & 1.0000 & -1.0000 & 0.1394 & -0.1394 \end{bmatrix}. \tag{1.19}$$

and

$$D = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 0.8536 & 0 & 0 & 0 \\ 0 & 0 & 0.1464 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}. \tag{6.1.20}$$

It is clear from D that the largest eigenvalue is 1, and while computing D^n for n = 100, one approaches the steady state vector f. Now,

$$D^n|_{n=100} = \begin{bmatrix} (1)^n & 0 & 0 & 0 & 0 \\ 0 & (0.8536)^n & 0 & 0 & 0 \\ 0 & 0 & (0.1464)^n & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \approx \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}. \quad (6.1.21)$$

Once the values of V and D^n are obtained, the final capacitor voltage matrix f can be calculated using (6.1.14), (6.1.15), (6.1.17), (6.1.18), (6.1.19), and (6.1.21). Thus,

$$f(\text{final}) = \begin{bmatrix} 1 \\ 1 \\ 2 \\ 3 \\ 4 \end{bmatrix} \bullet V_{LV}$$

Figure 6-4 shows the elements of the vector f, and these values are eventually the deciding factors of the capacitor voltages after n iterations when n is sufficiently large. In

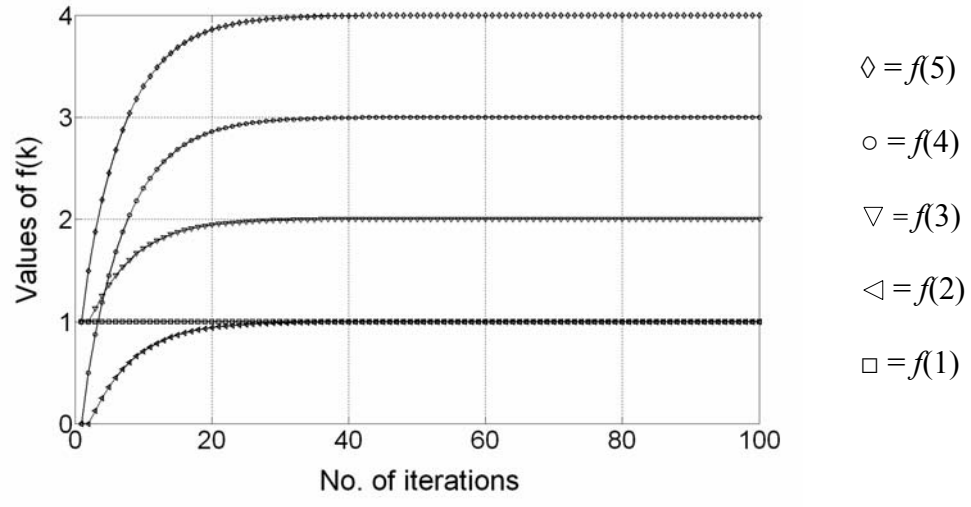


Figure 6-4. The capacitor voltage variations with iterations. At n=40, all voltages have reached steady state for all practical purposes.

Figure 6-4, the components of vector *f* are plotted against the number of iterations *n*, and it was found that after 40 iterations, voltages almost reach steady state. After 100 iterations, capacitor voltages are very close to the components of *f* and the errors become negligibly small ($<10^{-7}$).

A 5-level MMCCC has two sub intervals in steady state, and the operations GSS 1 and GSS 2 takes place in subsequent sub-intervals. Thus, *n* iterations of GSS 1 and GSS2 take *n* clock cycles for the converter. The MMCCC converter runs at 10 kHz clock, and one clock period is 100 μs. So even if the converter is allowed to have 100 clock periods to stay in the startup state, it will take 10 ms to complete the start up procedure. Thus, after 10 ms, the capacitor voltages are,

$$\begin{aligned} V_{C1} &= 1V_{LV}, \\ V_{C2} &= 1V_{LV}, \\ V_{C3} &= 2V_{LV}, \\ V_{C4} &= 3V_{LV}, \\ V_{C5} &= 4V_{LV}. \end{aligned} \tag{6.1.22}$$

The analytical derivation presented in this section explains the operation of a 5-level MMCCC circuit, and it can be cross-matched with the operation explained in Figure 6-2. In this figure, the two sub-intervals of the circuit are shown. In the first sub-interval, C_5 and C_1 are connected in series, and they are connected across V_{HV}. If there is no loss in the circuit or no load connected at the output, the total voltage across the series connected circuit of C_5 and C_1 is 5 V_{LV}, and this is found from (6.1.22). As the conversion ratio of the circuit is 5, $V_{HV} = 5\ V_{LV}$ and the circuit will not take any power from V_{HV}. In addition, there is another current path comprised of C_4, C_3, and C_1. In Figure 6-2, during state 1, C_4 is connected across the series combination of C_3 and C_1. Equation (6.1.22) shows that the

voltage across C_4 (3 V_{LV}) is equal to the summation of voltages across C_1 (1 V_{LV}) and C_3 (2 V_{LV}). Moreover, C_2 is connected across C_1, and their voltages are matched also. Thus, the voltages across the capacitors at state 1 are matched to each other.

In state 2, C_5 is connected across the series circuit of C_4 and C_1. These voltages are also matched and it can be seen in (6.1.22). In the same way, C_3 is connected across the series circuit of C_2 and C_1, and the voltage across C_3 (2 V_{LV}) is the same as the total voltage across C_1 and C_2 (V_{LV} + V_{LV} = 2 V_{LV}). Thus, the capacitor voltages during state 2 are also matched, and the load can be connected either at high voltage side or low voltage side. Once a load is connected at either side, the load current will discharge the capacitors, and charge transfer will take place either from a voltage source (V_{LV} or V_{HV}) to a capacitor or from one capacitor to another. In this case, the steady state capacitor voltages will be different from the values mentioned in (6.1.22), and the analysis is shown in section 6.3.

The eigenvalues found in D were such that except for the largest eigenvalue (1), all other values diminish in D^n with increasing n. However, it was observed that for n equal to 100, the diagonal values in the D^n matrix (except the first one) become smaller than 10^{-7}. For this reason, n was chosen to be 100 for the startup process.

6.3 STEADY STATE ANALYSIS:

Section 6.2 presented the step by step switching scheme that would ensure safe operating voltage of the transistors in the circuit. After 100 cycles, the capacitor voltages reach the values shown in (6.1.22). During that time, the load was not connected at the output, and the source V_{LV} was connected at the low voltage side to balance the capacitor

voltages. Thus, the values found from (6.1.22) will be used as the initial conditions of the steady state operation of the circuit. During the steady state operation, the MMCCC circuit operates in two states shown in Figure 6-2. Based on these operating states, the operation of the MMCCC circuit can be divided into four operating zones. They are,

1. State 1
2. Transition 1 (from state 1 to state 2)
3. State 2
4. Transition 2 (from state 2 to state 1)

These different time zones are shown in Figure 6-5. From t_1 to t_2, the circuit stays in state 1 or the first sub-interval in the steady state. From t_3 to t_4, the circuit operates in state 2 or the second sub-interval in the steady state. Time t_0 to t_1 is the transition time from state 2 to state 1. In the same way, t_2 to t_3 is the time required for the transition from state 1 to state 2. The transition times are negligibly small compared to the time required for state 1 and state 2. After one complete cycle, voltage and current equations at t_4 and t_5 would be the same as t_0 and t_1 respectively.

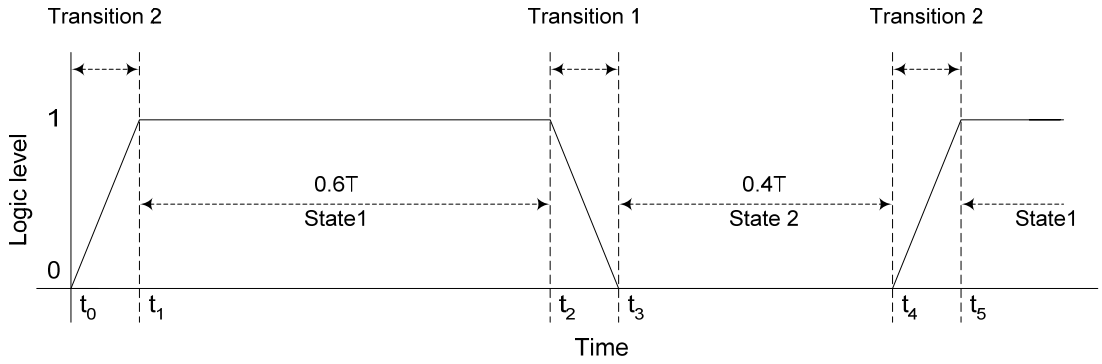
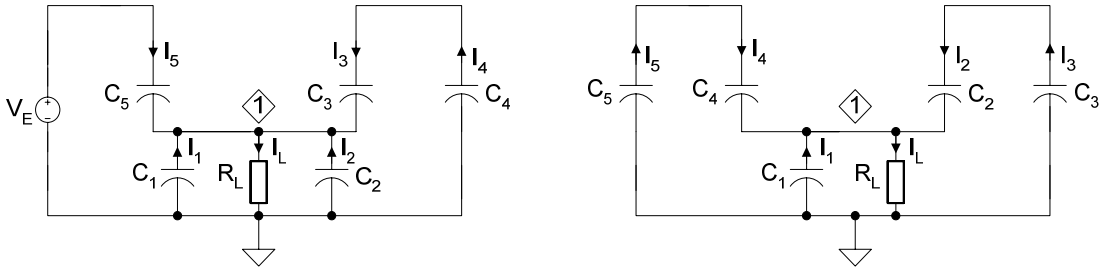


Figure 6-5. The steady state and transition state timing diagram of a 5-level MMCCC.

For a 5-level conversion, $(t_2 - t_1)$ is 1.5 times $(t_4 - t_3)$. Thus, $(t_2 - t_1) = 0.6T$ and $(t_4 - t_3) = 0.4T$, where T is the time period of one cycle. For the proposed design, T is 100 μS for an operating frequency of 10 kHz. The reason for unequal width of state 1 and state 2 will be explained later in this chapter.

As mentioned earlier, the final values of the capacitors found from the startup analysis will be used in the steady state analysis as a starting point. However, these values were found under the assumption that there was no loss involved in the circuit. As there was no load connected at the output, the capacitor values did not change with time. However, in the steady state, load current discharges the capacitors, and the capacitor voltages will vary in different operating zones. To include the effect of the load current, four constant error components δ_1, δ_3, δ_4, and δ_5 are added to the capacitor voltages at the beginning of state 1. Depending on the load current, the capacitor voltages will change, and if the computation is correct, after transition 2 the capacitor voltages will be the same as found at the beginning of state 1.

Figure 6-6 shows the steady state diagrams with load connected at the low voltage



(a) (b)

Figure 6-6. The re-defined steady state diagrams with load connected at the low voltage side, (a) state 1, (b) state 2.

side, and a voltage source V_E is connected at the high voltage side. For this analysis, the converter is considered to work in down conversion mode. Thus, Figure 6-6 is a modified version of the schematics shown in Figure 6-2. For easier understanding of the derivation, the voltage source V_{HV} has been renamed as V_E in Figure 6-6 to relate it with the capacitor voltages expressed in terms of the amplitude of V_E.

6.3.1 CURRENT AND VOLTAGE EQUATIONS IN STATE 1

At time $t = t_1$, the MMCCC circuit is on the verge of state 1, and it is shown in Figure 6-5. Using the voltages found from the startup analysis and considering some constant deviations,

$$V_{C5} = 0.8E + \delta_5 \tag{6.2.1}$$

$$V_{C4} = 0.6E + \delta_4 \tag{6.2.2}$$

$$V_{C3} = 0.4E + \delta_3 \tag{6.2.3}$$

$$V_{C2} = V_{C1} = 0.2E + \delta_1 \tag{6.2.4}$$

where E is the voltage amplitude of the source V_E shown in Figure 6-6, and the following equations can be used as boundary conditions derived from this figure. These boundary conditions are not global, and are valid during state 1 only. Thus,

$$E = V_{C5} + V_{C1} \tag{6.2.5}$$

$$V_{C4} = V_{C3} + V_{C2} \tag{6.2.6}$$

$$I_1 + I_2 + I_4 + I_5 = I_L \tag{6.2.7}$$

and $V_{C2} = V_{C1}$

Using (6.2.1), (6.2.4), and (6.2.5),

$$E = 0.8E + \delta_5 + 0.2E + \delta_1$$

$$\Rightarrow \delta_5 + \delta_1 = 0 \tag{6.2.8}$$

Using (6.2.2 -6.2.4) and (6.2.6)

$$0.6E + \delta_4 = 0.4E + \delta_3 + 0.2E + \delta_1$$

$$\Rightarrow \delta_4 = \delta_3 + \delta_1. \tag{6.2.9}$$

Figure 6-6 shows the direction of currents through the capacitors and the load. Depending on the direction of the current and the capacitor voltages, the following equations could be written at the end of state 1 (at $t = t_2$):

$$V_{C5} = 0.8E + \delta_5 + \frac{I_5 \cdot 0.6T}{C}. \tag{6.2.10}$$

$$V_{C4} = 0.6E + \delta_4 - \frac{I_4 \cdot 0.6T}{C}. \tag{6.2.11}$$

$$V_{C3} = 0.4E + \delta_3 + \frac{I_4 \cdot 0.6T}{C}. \tag{6.2.12}$$

$$V_{C1} = V_{C2} = 0.2E + \delta_1 - \frac{I_1 \cdot 0.6T}{C}. \tag{6.2.13}$$

where $C_1 = C_2 = C_3 = C_4 = C_5 = C$, and $I_3 = I_4$, $I_1 = I_2$.

To satisfy the boundary condition (6.2.5),

$$E = 0.8E + \delta_5 + \frac{I_5 \cdot 0.6T}{C} + 0.2E + \delta_1 - \frac{I_1 \cdot 0.6T}{C}$$

$$\Rightarrow I_5 = I_1 \ (\delta_5 + \delta_1 = 0). \tag{6.2.14}$$

Using (6.2.11-6.2.13) and constraint (6.2.6),

$$0.6E + \delta_4 - \frac{I_4 \cdot 0.6T}{C} = 0.4E + \delta_3 + \frac{I_4 \cdot 0.6T}{C} + 0.2E + \delta_1 - \frac{I_1 \cdot 0.6T}{C}$$

$$\Rightarrow I_1 = 2I_4 \ (\delta_4 = \delta_3 + \delta_1). \tag{6.2.15}$$

To satisfy the boundary condition stated in (6.2.7), the following equation can be derived

using (6.2.14) and (6.2.15),

$$I_1 = I_2 = I_5 = \frac{2I_L}{7}. \tag{6.2.16}$$

And,

$$I_4 = \frac{I_L}{7}. \tag{6.2.17}$$

Using (6.2.16), (6.2.17) in (6.2.10 - 6.2.13), the capacitor voltages at $t = t_2$ can be summarized as,

$$V_{C5}(t_2) = 0.8E + \delta_5 + \frac{6\Delta}{35}. \tag{6.2.18}$$

$$V_{C4}(t_2) = 0.6E + \delta_4 - \frac{3\Delta}{35}. \tag{6.2.19}$$

$$V_{C3}(t_2) = 0.4E + \delta_3 + \frac{3\Delta}{35}. \tag{6.2.20}$$

$$V_{C1}(t_2) = V_{C2} = 0.2E + \delta_1 - \frac{6\Delta}{35}. \tag{6.2.21}$$

where $\Delta = \frac{I_L \bullet T}{C}$

Now, there will be a transition from state 1 to state 2 at $t = t_2$, and it will continue until $t = t_3$. This transition is shown in Figure 6-5 in time axis. The capacitor voltages after the transition can be determined using a general quantitative method that will be presented in section 6.3.2. After this transition, the converter will be transformed from the circuit shown in Figure 6-6(a) to the circuit shown in Figure 6-6(b). Thus, the capacitor voltages found at the end of state 1 will be the inputs in transition 1, and the voltages found at the end of transition 1 will be used as the inputs in state 2. This

generalized analysis determines the capacitor voltages at the end of this transition state based on the voltages the capacitors had at the beginning of the state. The purpose of this generalized method is to find a set of simpler voltage and current equations during the transition state.

6.3.2 CURRENT AND VOLTAGE EQUATIONS IN TRANSITION 1

Once the converter completes state 1, capacitor voltages change from the original values at the beginning of state 1. During the transition, the circuit is converted from state 1 to state 2, and this is shown in Figure 6-6. During the transition process, all the five capacitors participate in the charge transfer process simultaneously. However, for the convenience of analysis, it is assumed that this operation takes place in sequential steps. These steps are such that a superposition can be applied to them, meaning the effect of interconnecting multiple capacitors simultaneously would be the same as connecting them sequentially.

Figure 6-7 explains the sequential capacitor switching in a transition state. This

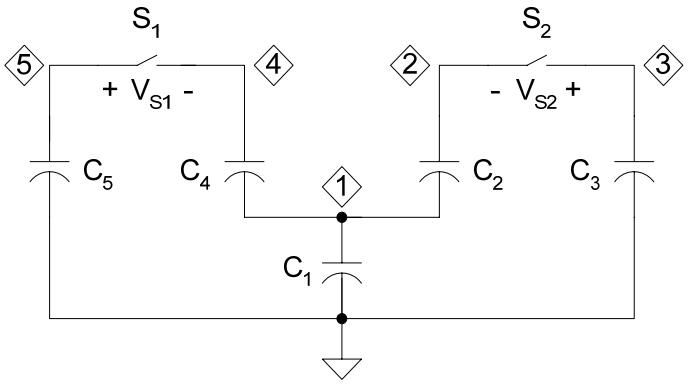


Figure 6-7. The sequential switching operation of capacitors in transition state 1.

transition is controlled by the operations of two switches S_1 and S_2, and a superposition can be applied to explain the consequence of the operation of these switches. It is assumed that S_1 is turned on first and then S_2. Thus, the effect of turning on both S_1 and S_2 would be the same as the combined effect of operating S_1 and S_2 separately. Based on this switching scheme, a generalized equation of the capacitor voltages will now be derived.

Figure 6-7 shows the transition operation between state 1 and state 2. By closing switches S_1 and S_2, the circuit is transformed to operate in state 2. For the convenience of the analysis, the capacitor voltages at the beginning of this transition state are defined as V_{C1}, V_{C2}, V_{C3}, V_{C4}, and V_{C5} rather than using the exact values found in (6.2.18) to (6.2.21). Two intermediate variables Δ_1 and Δ_2 are defined as follows,

$$\Delta_1 = V_{S1} = V_{C5} - (V_{C4} + V_{C1}). \tag{6.2.21b}$$

and

$$\Delta_2 = V_{S2} = V_{C3} - (V_{C2} + V_{C1}). \tag{6.2.21c}$$

In addition, the analysis will determine the capacitor voltages at the end of this transition state as a function of Δ_1 and Δ_2.

When S_1 is closed and S_2 is open, C_5 will be discharged and it will transfer some of its charge to C_4 and C_1. Thus, there will be a voltage drop across C_5, and the change in V_{C5} is, $\Delta V_{C5} = \Delta_1 \bullet \frac{C_{5eq}}{C_{5eq} + C}$, where C_{5eq} is the capacitance connected at terminal 5 of Figure 6-7 or the capacitance seen by C_5. As S_2 is open, the total capacitance at node 5 is the series capacitance of C_4 and C_1. Thus, $C_{5eq} = 0.5C$.

Thus, $\Delta V_{C5} = \Delta_1 \bullet \frac{0.5C}{0.5C + C} = \frac{\Delta_1}{3}$. (6.2.22)

The change in the voltage at node 4 is,

$$\Delta V_4 = \Delta_1 \bullet \frac{C}{C_{5eq} + C} = \frac{2\Delta_1}{3}. \tag{6.2.23}$$

The change in the voltage of C_4 is $\Delta Vc_4 = \Delta V_4 \bullet \frac{C_1}{C_1 + C_4} = \frac{\Delta_1}{3}$. (6.2.24)

In the same way, $\Delta Vc_1 = \frac{\Delta_1}{3}$. (6.2.25)

Thus, the new capacitor voltages are,

$$V'_{C5} = V_{C5} - \Delta V_{C5}$$

$$= V_{C5} - \frac{\Delta_1}{3}. \tag{6.2.26}$$

$$V'_{C4} = V_{C4} + \Delta V_{C5}$$

$$= V_{C4} + \frac{\Delta_1}{3}. \tag{6.2.27}$$

$$V'_{C1} = V_{C1} + \Delta V_{C5}$$

$$= V_{C1} + \frac{\Delta_1}{3}. \tag{6.2.28}$$

In the beginning, $\Delta_2 = V_{S2} = V_{C3} - (V_{C2} + V_{C1})$

Because V_{C1} has changed due to the closing operation of S_1, the new Δ_2 can be determined using (6.2.28). Thus,

$$\Delta'_2 = \Delta_2 - \frac{\Delta_1}{3}. \tag{6.2.30}$$

When S_2 is activated, there occurs some charge transfer among the capacitors and the voltages of the capacitors are re-configured as follows,

$$\Delta V_{C3} = \Delta'_2 \bullet \frac{C_{3eq}}{C_{3eq} + C}. \tag{6.2.31}$$

So, $V'_{C3} = V_{C3} - \Delta'_2 \bullet \frac{C_{3eq}}{C_{3eq} + C}$. (6.2.32)

And, the change at node 2 is,

$$\Delta V_2 = \Delta'_2 \bullet \frac{C}{C_{3eq} + C}. \tag{6.2.33}$$

Where, C_{3eq} is the capacitance seen by C_3. After looking at the circuit at node 2,

$$C_{3eq} = \frac{\left[\left(\frac{C_4 \bullet C_5}{C_4 + C_5}\right) + C_1\right]}{C2 + \left[\left(\frac{C_4 \bullet C_5}{C_4 + C_5}\right) + C_1\right]} \bullet C_2 = \frac{1+0.5}{1+0.5+1} \bullet C = 0.6C. \tag{6.2.34}$$

Using (6.2.34) and (6.2.31),

$$V'_{C3} = V_{C3} - \frac{3\Delta'_2}{8}$$

Using (6.2.30),

$$V'_{C3} = V_{C3} - \frac{3\Delta_2 - \Delta_1}{8}. \tag{6.2.35}$$

And,

$$\Delta V_2 = \frac{5\Delta'_2}{8}. \tag{6.2.36}$$

So, the change in the voltage in C_2 is,

$$\Delta Vc_2 = \Delta V_2 \bullet \frac{C_{1eq}}{C_{1eq} + C}. \tag{6.2.37}$$

where C_{1eq} is the capacitance at node 1.

$$C_{1eq} = C_1 + \frac{C_4 \bullet C_5}{C_4 + C_5} = 1.5C\,. \tag{6.2.38}$$

Thus, using (6.2.37) and (6.2.38),

$$\Delta Vc_2 = \frac{3\Delta V_2}{5} = \frac{3\Delta'_2}{8} = \frac{3\Delta_2 - \Delta_1}{8}. \tag{6.2.39}$$

$$V'_{C2} = V_{C2} + \Delta V_{C2}. \tag{6.2.39a}$$

And the change in voltage at node 1 is

$$\Delta V_1 = \Delta V_2 \bullet \frac{C}{C_{1eq} + C}\,. \tag{6.2.40}$$

Thus, using (6.2.36), (6.2.38), and (6.2.40),

$$\Delta V_1 = \frac{2\Delta V_2}{5} = \frac{\Delta'_2}{4}.$$

Using (6.2.30),

$$\Delta V_1 = \frac{3\Delta_2 - \Delta_1}{12}\,. \tag{6.2.41}$$

So, the re-configured voltage at node 1 is

$$V''_{C1} = V'_{C1} + \Delta V_1$$

$$= V_{C1} + \frac{\Delta_1}{3} + \frac{\Delta'_2}{4}\,. \tag{6.2.42}$$

Using (6.2.30) and (6.2.42),

$$V''_{C1} = V_{C1} + \frac{\Delta_1 + \Delta_2}{4} = V_{C1} + \Delta' V_{C1}, \tag{6.2.43}$$

where $\Delta' V_{C1} = \dfrac{\Delta_1 + \Delta_2}{4}$. (6.2.44)

The change in the voltage at node 1 will also have an impact on the voltages of C_4

and C_5. As C_4 and C_5 are connected in series and they have equal capacitance, the voltage variation in C_5 and C_4 would be the same. Thus, using (6.2.41),

$$\Delta' Vc_5 = \Delta' Vc_4 = \Delta V_1 \bullet \frac{C_4 (or\, C_5)}{C_4 + C_5} = \frac{3\Delta_2 - \Delta_1}{24}. \tag{6.2.45}$$

So $V''_{C5} = V'_{C5} + \Delta' V_{C5}$

Using (6.2.26) and (6.2.45),

$$V''_{C5} = V_{C5} - \frac{\Delta}{3} + \frac{3\Delta_2 - \Delta_1}{24} = V_{C5} - \frac{3\Delta_1 - \Delta_2}{8}. \tag{6.2.46}$$

In the same way,

$$V''_{C4} = V_{C4} + \frac{\Delta}{3} - \frac{3\Delta_2 - \Delta_1}{24} = V_{C4} + \frac{3\Delta_1 - \Delta_2}{8}. \tag{6.2.47}$$

At this point, all the capacitor voltages have been found in terms of their original values and two intermediate variables Δ_1, Δ_2.

Using (6.2.18) - (6.2.21), (6.2.21b) and (6.2.21c),

$$\Delta_1 = \frac{15\Delta}{35} + (\delta_5 - \delta_4 - \delta_1) \tag{6.2.48}$$

And,

$$\Delta_2 = \frac{15\Delta}{35} + (\delta_3 - 2\delta_1) \tag{6.2.49}$$

Using (6.2.21), (6.2.43), (6.2.48) and (6.2.49),

$$V_{C1}(t_3) = 0.2E + \frac{3\Delta}{70} + \frac{1}{4}\delta_5 \tag{6.2.50}$$

Using (6.2.21), (6.2.39), (6.2.39a), (6.2.48) and (6.2.49),

$$V_{C2}(t_3) = 0.2E - \frac{9\Delta}{140} - \frac{1}{8}\delta_5 + \frac{1}{2}\delta_4 \tag{6.2.51}$$

Using (1.20), (1.35), (1.48) and (1.49),

$$V_{C3}(t_3) = 0.4E - \frac{3\Delta}{140} + \frac{1}{8}\delta_5 + \frac{1}{2}\delta_4 . \tag{6.2.52}$$

Using (1.19), (1.47), (1.48) and (1.49),

$$V_{C4}(t_3) = 0.6E + \frac{3\Delta}{140} + \frac{3}{8}\delta_5 + \frac{1}{2}\delta_4 . \tag{6.2.53}$$

Using (1.18), (1.46), (1.48) and (1.49),

$$V_{C5}(t_3) = 0.8E + \frac{9\Delta}{140} + \frac{5}{8}\delta_5 + \frac{1}{2}\delta_4 . \tag{6.2.54}$$

6.3.3 Current and voltage equations in State 2

Once the circuit goes through the first transition state, it enters into state 2, and the equivalent circuit is shown in Figure 6-6(b). The length of this state is $0.4T$ for a 5-level MMCCC converter. The state starts at $t = t_3$, and ends at t_4. From Figure 6-6(b), the voltage and current constraints during this state are

$$I_L = I_5 + I_3 + I_1,$$

$$V_{C5} = V_{C4} + V_{C1},$$

$$V_{C3} = V_{C2} + V_{C1}.$$

Using the same method followed in state 1, the capacitor voltages at $t = t_4$ are,

$$V_{C5}(t_4) = V_{C5}(t_3) - \frac{I_5 \cdot 0.4T}{C} \tag{6.2.55}$$

$$V_{C4}(t_4) = V_{C4}(t_3) + \frac{I_5 \cdot 0.4T}{C} \tag{6.2.56}$$

$$V_{C3}(t_4) = V_{C3}(t_3) - \frac{I_3 \cdot 0.4T}{C} \tag{6.2.57}$$

$$V_{C2}(t_4) = V_{C2}(t_3) + \frac{I_3 \cdot 0.4T}{C} \tag{6.2.58}$$

$$V_{C1}(t_4) = V_{C1}(t_3) - \frac{I_1 \cdot 0.4T}{C}\,. \tag{6.2.59}$$

Using the second constraint for this state and equations (6.2.50), (6.2.53), (6.2.54), (6.2.55), (6.2.56) and (6.2.59),

$$0.8E + \frac{9\Delta}{140} + \frac{5}{8}\delta_5 + \frac{1}{2}\delta_4 - \frac{I_5 \cdot 0.4T}{C} = 0.6E + \frac{3\Delta}{140} + \frac{3}{8}\delta_5 + \frac{1}{2}\delta_4 + \frac{I_5 \cdot 0.4T}{C} + 0.2E + \frac{3\Delta}{70} + \frac{1}{4}\delta_5 - \frac{I_1 \cdot 0.4T}{C}$$

Thus,

$$I_1 = 2I_5\,. \tag{6.2.60}$$

Again, $V_{C3}(t_4) = V_{C2}(t_4) + V_{C1}(t_4)$

Thus, using the third constraint and equations (6.2.50), (6.2.51), (6.2.53), (6.2.57), (6.2.58) and (6.2.59),

$$I_1 = 2I_3\,. \tag{6.2.61}$$

Using the first constraint and equations (6.2.60) and (6.2.61),

$$I_1 = \frac{I_L}{2}\,. \tag{6.2.62}$$

$$I_3 = \frac{I_L}{4}\,. \tag{6.2.63}$$

$$I_5 = \frac{I_L}{4}\,. \tag{6.2.64}$$

Thus, using (6.2.51) – (6.2.59), (6.2.62) – (6.2.64),

$$V_{C5}(t_4) = 0.8E - \frac{\Delta}{28} + \frac{5}{8}\delta_5 + \frac{1}{2}\delta_4\,. \tag{6.2.65}$$

$$V_{C4}(t_4) = 0.6E + \frac{17\Delta}{140} + \frac{3}{8}\delta_5 + \frac{1}{2}\delta_4 . \quad (6.2.66)$$

$$V_{C3}(t_4) = 0.4E - \frac{11\Delta}{140} + \frac{1}{8}\delta_5 + \frac{1}{2}\delta_4 . \quad (6.2.67)$$

$$V_{C2}(t_4) = 0.2E + \frac{\Delta}{28} - \frac{1}{8}\delta_5 + \frac{1}{2}\delta_4 . \quad (6.2.68)$$

$$V_{C1}(t_4) = 0.2E - \frac{11\Delta}{70} + \frac{1}{4}\delta_5 . \quad (6.2.69)$$

where $\Delta = \frac{I_L \bullet T}{C}$

At the end of state 2, there will be a second transition that will take the circuit from state 2 to state 1 again. After transition 2, the capacitor voltages should be the same as they were at the beginning of state 1 provided the circuit is lossless and has stability. This second transition starts at t_4 and ends at t_5. Thus, at t_5, the circuit operating point is exactly the same as it was at t_1. The same generalized technique that was followed to determine voltages after transition 1 will be used in transition 2, where these voltages will depend on the capacitor voltages at $t = t_4$, and the two intermediate variables Δ_3 and Δ_4. Thus all the terminologies used in the derivation of transition 2 such as V_{C1}, V_{C2} etc. will be the voltages at t_4.

6.3.4 Current and Voltage Equations in Transition 2

This second transition operation is shown in Figure 6-8. The operation of this transition can be explained using the operations of three switches where a superposition theory can be applied. This means that, the effect of operating three switches simultaneously is the same as operating them sequentially. After closing these three

switches, the circuit will be transformed to operate in state 1 again.

Before operating any switches at $t = t_4$,

$$\Delta_3 = V_{S1} = E - V_{C5} - V_{C1}$$

Using (6.2.65) and (6.2.69),

$$\Delta_3 = \frac{27\Delta}{140} - \frac{7}{8}\delta_5 - \frac{1}{2}\delta_4 . \tag{6.2.70}$$

And,

$$\Delta_4 = V_{S2} = V_{C4} - V_{C3} - V_{C1}$$

Using (6.2.66), (6.2.67) and (6.2.69),

$$\Delta_4 = \frac{5}{14}\Delta . \tag{6.2.71}$$

It is assumed that S_0 is operated first. Before closing S_0,

$$V_{S0} = V_{C2} - V_{C1}$$

After closing S_0,

$$V'_{C1} = V'_{C2} = \frac{V_{C1} + V_{C2}}{2}$$

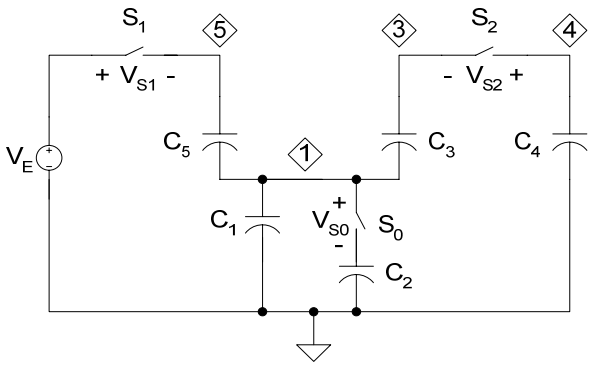


Figure 6-8. The sequential switching operation of the capacitors to obtain transition 2.

Using (6.2.68) and (6.2.69),

$$V'_{C1} = V'_{C2} = 0.2E - \frac{17\Delta}{280} + \frac{1}{16}\delta_5 + \frac{1}{4}\delta_4 . \tag{6.2.72}$$

and $\Delta V_{C1} = V'_{C1} - V_{C1}$

Thus, $\Delta V_{C1} = \frac{27\Delta}{280} - \frac{3}{16}\delta_5 + \frac{1}{4}\delta_4 .$ (6.2.73)

Due to a change in V_{C1}, Δ_3 will also change. Thus, the new Δ_3 will be

$$\Delta'_3 = \Delta_3 - \Delta V_{C1} . \tag{6.2.74}$$

Now, if S_1 is closed,

ΔV_{C5} = change in V_{C5}

$= \Delta'_3 \bullet \frac{C_{5eq}}{C_{5eq} + C}$, where C_{5eq} is the capacitance seen by C_5 at node 1 in Figure 6-7.

Here, $C_{5eq} = \frac{C_1 \bullet C_2}{C_1 + C_2} = 2C.$

Thus, $\Delta V_{C5} = \frac{2\Delta'_3}{3}.$ (6.2.75)

Due to a charge transfer between C_5 and C_{5eq}, voltage at node 1 in Figure 6-7 will increase.

So, $\Delta V'_{C1} = \Delta'_3 \bullet \frac{C_5}{C_5 + C_{5eq}} = \frac{\Delta'_3}{3} .$ (6.2.76)

Thus, $V''_{C1} = V'_{C1} + \Delta V'_{C1} = V'_{C1} + \frac{\Delta'_3}{3} .$ (6.2.77)

As, V_{C1} has changed twice, Δ_4 will also change from its original value.

$$\Delta'_4 = \Delta_4 - \Delta V_{C1} - \Delta V'_{C1}$$

Using (6.2.73) and (6.2.76),

$$\Delta'_4 = \frac{3\Delta_4 - \Delta_3 - 2\Delta V_{C1}}{3}. \tag{6.2.78}$$

Now, if S_2 is operated at this moment,

$\Delta V_{C4} = \Delta'_4 \bullet \frac{C_{4eq}}{C_{4eq} + C}$, where C_{4eq} is the capacitance at node 4 seen by C_4 in Figure 6-7.

Thus, $C_{4eq} = \frac{C_3 \bullet (C_1 + C_2 + C_5)}{C_3 + (C_1 + C_2 + C_5)}$

$$= \frac{3}{4}C.$$

$$\Delta V_{C4} = \frac{3/4}{1 + 3/4} \bullet \Delta'_4 = \frac{3\Delta'_4}{7}. \tag{6.2.80}$$

Voltage change at node 3 is

$$\Delta V_3 = \frac{C}{C + C_{4eq}} \bullet \Delta'_4 = \frac{4\Delta'_4}{7}. \tag{6.2.81}$$

So, $\Delta V_{C3} = \Delta V_3 \bullet \frac{C_{1eq}}{C_{1eq} + C} = \frac{3}{4} \bullet \frac{4}{7} \bullet \Delta'_4 = \frac{3\Delta'_4}{7}.$ (6.2.82)

where C_{1eq} is the capacitance at node 1 seen by C_3, and it is the parallel combination of C_1, C_2 and C_5.

Due to charge transfer between C_4 and the remaining circuit, V_{C3} has increased and V_{C1} will also increase.

So, $\Delta V''_{C1} = \Delta V_3 \bullet \frac{C_3}{C_3 + C_{1eq}} = \frac{\Delta'_4}{7}.$ (6.2.83)

Using (6.2.78) and (6.2.83),

$$\Delta V''_{C1} = \frac{3\Delta_4 - \Delta_3 - 2\Delta V_{C1}}{21}. \tag{6.2.84}$$

Thus, using (6.2.73), (6.2.76) and (6.2.85), the final voltage at node 1,

$$V'''_{C1} = V_{C1} + \Delta V_{C1} + \Delta V'_{C1} + \Delta V''_{C1} = V_{C1} + \frac{79\Delta}{490} - \frac{5}{14}\delta_5$$

$$V_{C1}(t_5) = V_{C2}(t_5) = V_{C1} + \frac{79\Delta}{490} - \frac{5}{14}\delta_5 . \tag{6.2.85}$$

Using (6.2.69),

$$V'''_{C1} = V_{C1}(t_5) = V_{C2}(t_5) = 0.2E + \frac{\Delta}{245} - \frac{3}{28}\delta_5 . \tag{6.2.86}$$

Final voltage at across C_5 is

$$V'_{C5} = V_{C5}(t_5) = E - V'''_{C1} = 0.8E - \frac{\Delta}{245} + \frac{3}{28}\delta_5 . \tag{6.2.87}$$

Using (6.2.78) and (6.2.82), the final voltage of C_3 is

$$V'_{C3} = V_{C3}(t_5) = V_{C3} + \Delta V_{C3} = 0.4E + \frac{19\Delta}{980} + \frac{17}{56}\delta_5 + \frac{1}{2}\delta_4 . \tag{6.2.88}$$

And, final voltage at C_4,

$$V'_{C4} = V_{C4} - \Delta V_{C4}$$

Using (6.2.78) and (6.2.80),

$$V'_{C4} = 0.6E + \frac{23\Delta}{980} + \frac{11}{56}\delta_5 + \frac{1}{2}\delta_4 . \tag{6.2.89}$$

Equations (6.2.86) to (6.2.89) show the 4 values of the five capacitor voltages at $t = t_5$. Starting at t_1, the converter completes a cycle at t_5, and thus, the capacitor voltages found at t_5 should be the same as they were at t_1.

So, comparing (6.2.1) and (6.2.87),

$$0.8E + \delta_5 = 0.8E - \frac{\Delta}{245} + \frac{3}{28}\delta_5$$

$$\therefore \delta_5 = -\frac{4\Delta}{875}. \tag{6.2.90}$$

Comparing (6.2.2) and (6.2.89),

$$0.6E + \delta_4 = 0.6E + \frac{23\Delta}{980} + \frac{11}{56}\delta_5 + \frac{1}{2}\delta_4$$

$$\therefore \delta_4 = \frac{79\Delta}{1750}. \tag{6.2.91}$$

Comparing (6.2.3) and (6.2.88),

$$0.4E + \delta_3 = 0.4E + \frac{19\Delta}{980} + \frac{17}{56}\delta_5 + \frac{1}{2}\delta_4$$

$$\therefore \delta_3 = \frac{71\Delta}{1750}. \tag{6.2.92}$$

Comparing (6.2.4) and (6.2.86),

$$0.2E + \delta_1 = 0.2E + \frac{\Delta}{245} - \frac{3}{28}\delta_5$$

$$\therefore \delta_1 = \frac{4\Delta}{875}. \tag{6.2.93}$$

Now the calculated values of δ_1, δ_3, δ_4, and δ_5 can be proven to be accurate if they satisfy the initial constraints that were made in state 1. To check that,

(6.2.90) + (6.2.93) $\therefore \delta_5 + \delta_1 = -\frac{4\Delta}{875} + \frac{4\Delta}{875} = 0$, and it satisfies (6.2.8).

So, the values of δ_5 and δ_1 are correct.

Again, (6.2.91) – (6.2.92) – (6.2.93) $\therefore \delta_4 - \delta_3 - \delta_1 = \frac{79\Delta}{1750} - \frac{71\Delta}{1750} - \frac{4\Delta}{875} = 0$, and it satisfies (6.2.9).

Thus, the calculated values of δ_4 and δ_3 are consistent. So, using the computed

values of δ_5, δ_4, δ_3, and δ_1, the capacitor voltages at the beginning of state 1 are,

$$V_{C5} = 0.8E - \frac{4\Delta}{875}. \tag{6.2.94}$$

$$V_{C4} = 0.6E + \frac{79\Delta}{1750}. \tag{6.2.95}$$

$$V_{C3} = 0.4E + \frac{71\Delta}{1750}. \tag{6.2.96}$$

$$V_{C1} = V_{C2} = 0.2E + \frac{4\Delta}{875}. \tag{6.2.97}$$

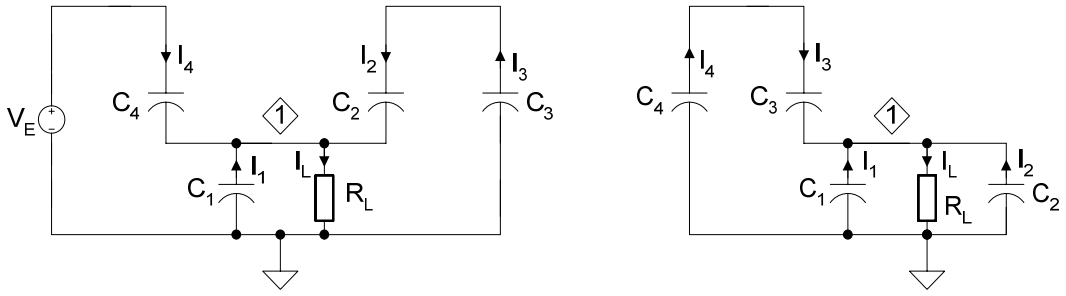
These computational steps prove that the MMCCC converter obtains a stable operation even when the load is connected to it. The capacitor voltages found from (6.2.94) – 6.2.97) are the steady state values for them. It means if the converter starts with these capacitor values at the beginning of state 1, after one complete cycle, the capacitors will have these same values. This steady state operating point will be shifted due to a change in load because the term Δ is a function of load current. However, for different loading conditions, the values of δ_1 to δ_5 will be different, and after one cycle, the converter will have the same capacitor voltages that it had at the beginning of state 1 during the new loading condition.

6.4 STEADY STATE ANALYSIS OF A 4-LEVEL CONVERTER

A detailed analytical derivation for the startup operation of a 5-level converter has been summarized in section 6.2. From this analytical part, the capacitor voltages at the end of initialization or startup phase for a 4-level converter can be determined using a 4×4 matrix, rather than the (5×5) matrix used for 5-level analysis. To do that, matrix *C*

and A are needed to be downsized by taking the first four rows and columns. In this way, the variable V_{C5} can be eliminated from the computation process and the capacitor voltages of a 4-level circuit can be calculated. The advantage of the startup analysis lies in the fact that the initialization operation of a MMCCC converter having any conversion ratio less than 5 can be determined by simply downsizing the matrix. In the same way, converters with higher conversion ratio can be modeled using different A and C matrices that can be derived from the original A and C matrices by adding new voltage equations for additional levels.

However, to get the steady state model for any conversion ratio, the task is not that easy and a generalized model could be difficult to find. The switching sequence in the 4-level operation will be different too. This can be explained comparing Figure 6-6 and Figure 6-9. Figure 6-9 shows the schematic diagrams of a 4-level MMCCC circuit in state 1 and state 2. The difference between a 5-level and a 4-level converter is the number of current paths active in any sub-interval. In a 5-level converter, there are 3 current paths



(a) (b)

Figure 6-9. The steady state operational diagrams of a 4-level MMCCC converter, (a) state 1, (b) state 2.

in state 1 (V_E - C_5 - C_1, C_4 - C_3 - C_1, C_2 - C_1), and 2 current paths in state 2 (C_5 - C_4 - C_1, C_3 - C_2 - C_1), as seen in Figure 6-6. The amount of ripple present at node 1 or at the output depends on how much the capacitors are discharged, and the discharging amount depends on how long the capacitors are connected to the load. Thus, to keep the ripple component equal in these two sub-intervals or states, the time duration of state 1 is 1.5 times the time duration of state 2 considering more current paths are present during state 1. If the time duration of state 1 and state 2 would be the same, three paths in state 1 would provide the same charge as the 2 paths in state 2 would provide. Thereby, the voltage ripple in state 2 would be higher than state 1 for equal time width of state 1 and 2.

When the conversion ratio is 4, there are 2 current paths in state 1 ($V_E - C_4$ - C_1, C_3 - C_2 - C_1) and two current paths in state 2 (C_4 - C_3 - C_1, C_2 - C_1), and it is shown in Figure 6-8. Thus, the time width of state 1 and state 2 must be the same to have equal output voltage ripple in both states. These two examples of equal and unequal time width of the states can be summarized as when the conversion ratio is odd, the time width ratio of state 1 and state 2 is the ratio of the number of active current paths in state 1 and state 2. For even conversion ratio, the time width ratio should be 1:1.

Using the capacitor voltages found from the start-up analysis presented in section 6.2, a steady state analysis for a 4-level converter can be accomplished following the technique presented in section 6.3. Like the 5-level circuit, the steady state analysis of a 4-level configuration is divided into 4 parts. They are,

1. State 1

2. Transition 1 (from state 1 to state 2)

3. State 2

4. Transition 2 (from state 2 to state 1)

Figure 6-10 shows the timing diagram of the 4 steps involved in the steady state analysis. The time duration of state 1 is (t_2-t_1) and that for state 2 is (t_4-t_3), and these two states have same time length. As before, the transitions times are considered negligibly small compared to state 1 and state 2. Using the startup analysis in section 6.2, the no-load no-loss capacitor voltage matrix for a 4-level converter is,

$$\begin{bmatrix} V_{C4} \\ V_{C3} \\ V_{C2} \\ V_{C1} \end{bmatrix} = \begin{bmatrix} 3 \\ 2 \\ 1 \\ 1 \end{bmatrix} \bullet V_{LV} \,. \tag{6.4.1}$$

where V_{LV} is the low voltage side voltage, and ideally, the factor V_{HV}/V_{LV} is equal to the number of levels active in the converter. However, during steady state, load is connected at the low voltage side, and capacitor voltages will not follow the values in (6.4.1) due to the load current. Thus, some constant offsets are added to these voltages in the beginning

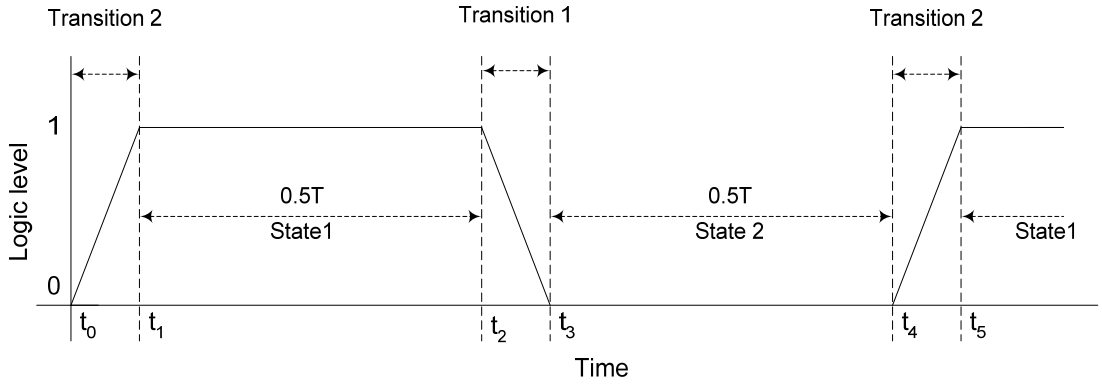


Figure 6-10. The steady state and transition state timing diagram of a 4-level MMCCC.

of state 1, and after one full cycle, the derived voltage equations are compared with the values assumed in the beginning of state 1. The detailed analytical computation is presented in the following sub-section.

6.4.1 CURRENT AND VOLTAGE EQUATIONS IN STATE 1

In the beginning of this state, it is assumed that capacitor voltages slightly deviate from the ideal values mentioned in (6.4.1). Thus, the capacitor voltages at the instance $t = t_1$ are,

$$\begin{aligned} V_{C4} &= 0.75E + \delta_4, \\ V_{C3} &= 0.5E + \delta_3, \\ V_{C2} &= 0.25E + \delta_2, \\ V_{C1} &= 0.25E + \delta_1. \end{aligned} \tag{6.4.2}$$

For convenience, the amplitude of V_{HV} has been used as E in (6.4.2), and for a 4-level converter, $E = 4\ V_{LV}$. The corresponding operational diagram for this state is shown in Figure 6-9(a). At the end of this state, the voltages across the capacitors will change, and the voltage variation will depend upon the load current. Like the steady state analysis of a 5-level conversion, the boundary conditions for a 4-level MMCCC throughout state 1 are,

$$\begin{aligned} E &= V_{C4} + V_{C1}, \\ V_{C3} &= V_{C2} + V_{C1}, \\ I_L &= I_4 + I_3 + I_1. \end{aligned} \tag{6.4.3}$$

Using (6.4.2) and (6.4.3),

$$\begin{aligned} \delta_4 + \delta_1 &= 0, \\ \delta_3 &= \delta_2 + \delta_1. \end{aligned} \tag{6.4.4}$$

The current directions through the capacitors are shown in Figure 6-9(a). From this figure, the capacitor voltages at the end of state 1 can be derived. Thus at $t = t_2$,

$$
\begin{aligned}
V_{C4}(t_2) &= 0.75E + \delta_4 + \frac{I_4 \bullet 0.5T}{C}, \\
V_{C3}(t_2) &= 0.5E + \delta_3 - \frac{I_3 \bullet 0.5T}{C}, \\
V_{C2}(t_2) &= 0.25E + \delta_2 + \frac{I_3 \bullet 0.5T}{C}, \\
V_{C1}(t_2) &= 0.25E + \delta_1 - \frac{I_1 \bullet 0.5T}{C}.
\end{aligned}
\tag{6.4.5}
$$

where $C_1 = C_2 = C_3 = C_4 = C$, and $I_2 = I_3$. Because the boundary conditions in (6.4.3) are valid all through state 1, the following equations at can be written using (6.4.5) and (6.4.3).

$$
\delta_4 + \delta_1 + \frac{I_4 \bullet 0.5T}{C} - \frac{I_1 \bullet 0.5T}{C} = 0
$$

Using (6.4.4),

$$
I_1 = I_4 \tag{6.4.6}
$$

In the same way, using (6.4.5), (6.4.3) and (6.4.4),

$$
I_1 = 2I_3 \tag{6.4.7}
$$

Using the current constraint in (6.4.3) the above two equations can be re-written as,

$$
\begin{aligned}
I_1 &= I_4 = 0.4I_L \\
I_2 &= I_3 = 0.2I_L
\end{aligned}
\tag{6.4.8}
$$

Thus, putting the current magnitudes found from (6.4.8) in (6.4.5), the capacitor voltages at t = t_2 can be obtained. Thus,

$$
\begin{aligned}
V_{C4}(t_2) &= 0.75E + \delta_4 + 0.2\Delta, \\
V_{C3}(t_2) &= 0.50E + \delta_3 - 0.1\Delta, \\
V_{C2}(t_2) &= 0.25E + \delta_2 + 0.1\Delta, \\
V_{C1}(t_2) &= 0.25E + \delta_1 - 0.2\Delta.
\end{aligned}
\tag{6.4.9}
$$

where $\Delta = \frac{I_L \bullet T}{C}$

Now there will be a transition that will convert the circuit from state 1 configuration to state 2 configuration. In Figure 6-10, transition 1 is shown that lasts for a brief period of time starting from t_2, and it ends at t_3. Thus, the capacitor voltages found at the end of state 1 will be the inputs in transition 1, and the voltages found at the end of transition 1 will be used as the inputs in state 2. The generalized derivation discussed in section 6.4.2 will determine the capacitor voltages at the end of this transitions state based on the capacitors, voltages at the beginning of the state.

6.4.2 CURRENT AND VOLTAGE EQUATIONS IN TRANSITION 1

To reduce computational complexity, the transition operation is considered as several sequential operations that obey superposition principal. It means that, doing all the operations simultaneously is equivalent to doing them sequentially. The transition 1 operation is shown in Figure 6-11. This transition is controlled by the operation of two switches S_1 and S_2. It is assumed that S_2 is turned on first followed by S_1, although

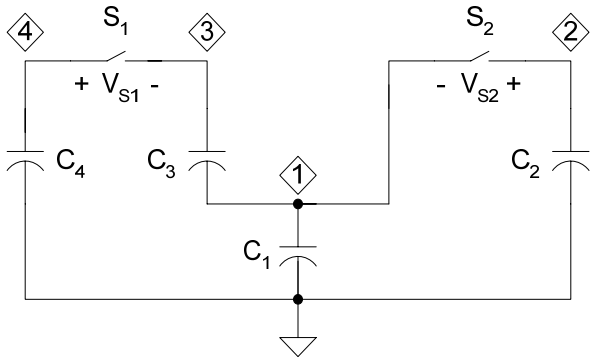


Figure 6-11. The sequential switching operation of capacitors in transition 1.

reversing the switching sequence gives the same charge transfer operation. The capacitor voltage conventions used in the analysis such as V_{C1}, V_{C2} etc. will be the voltages at the end of state 1 or at the beginning of transition 1.

When S_2 is closed, C_1 and C_2 are connected in parallel, and the new V_{C1} is,

$$V'_{C1} = V'_{C2} = \frac{V_{C1} + V_{C2}}{2} = 0.5V_{C1} + 0.5V_{C2}\,. \tag{6.4.10}$$

Using (6.4.9),

$$V'_{C1} = V'_{C2} = 0.25E + 0.5\delta_1 + 0.5\delta_2 - 0.05\Delta\,. \tag{6.4.11}$$

Once the switch S_1 is closed, a charge transfer among C_4, C_3, C_2 and C_1 will take place. The final capacitor voltages after this transition will depend upon V_{S1} and V_{C1}. Thus, $V_{S1} = (V_{C4} - V_{C3} - V'_{C1})$. Using (6.4.9) and (6.4.11),

$$V_{S1} = -2.5\delta_1 - 1.5\delta_2 + 0.35\Delta\,. \tag{6.4.12}$$

After closing S_1, V_{C4} will change as well as V_{C3}. Thus, the new V_{C4} is,

$$V'_{C4} = V_{C4} - V_{S1} \bullet \frac{C_{4eq}}{C_4 + C_{4eq}}\,. \tag{6.4.13}$$

where C_{4eq} is the capacitance seen by C_4 at node 4 or 3 (as S_1 is closed now). By looking at the circuit at node 4,

$$C_{4eq} = \frac{C_3 \bullet (C_1 + C_2)}{C_3 + C_1 + C_2} = \frac{2}{3}C$$

Using this value of C_{4eq} in (6.4.13) and using (6.4.9) and (6.4.12),

$$V'_{C4} = V_{C4}(t_3) = 0.75E + 0.6\delta_2 + 0.06\Delta\,. \tag{6.4.14}$$

The change in voltage at node 3 will be,

$$\Delta V_3 = V_{S1} \bullet \frac{C_4}{C_4 + C_{4eq}} = \frac{3}{5} \bullet V_{S1} = -1.5\delta_1 - 0.9\delta_2 + 0.21\Delta\,. \tag{6.4.15}$$

Thus, the change in voltage in V_{C3} will be,

$$\Delta V_{C3} = \Delta V_3 \bullet \frac{C_{1eq}}{C_{1eq} + C_3}. \tag{6.4.16}$$

where C_{1eq} is the capacitance at node 1 looking from left. In Figure 6-11, C_{1eq} is the parallel capacitance of C_1 and C_2. Thus $C_{1eq} = 2C$

Using this value in (6.4.16),

$$\Delta V_{C3} = -\delta_1 - 0.6\delta_2 + 0.14\Delta$$

Thus, $V_{C3}(t_3) = V_{C3} + \Delta V_{C3} = 0.5E + 0.4\delta_2 + 0.04\Delta$. (6.4.17)

Due to the charge transfer among C_4, C_3, C_1 and C_2, V_{C1} will change from the value that was initially found in (6.4.11). So,

$$V_{C1}(t_3) = V'_{C1} + \Delta V_{C1}, \tag{6.4.18}$$

where $\Delta V_{C1} = \Delta V_3 \bullet \frac{C_3}{C_{1eq} + C_3} = \frac{\Delta V_3}{3} = -0.5\delta_1 - 0.3\delta_2 + 0.07\Delta$. (6.4.19)

Using (6.4.11), (6.4.18) and (6.4.19),

$$V_{C1}(t_3) = V_{C2}(t_3) = 0.25E + 0.2\delta_2 + 0.02\Delta. \tag{6.4.20}$$

So far, we have found all the capacitor voltages at the end of transition 1. These voltages will be the initial capacitor voltages for state 2.

6.4.3 Current and voltage equations in State 2

Once the MMCCC circuit completes the first transition, it is transformed into the schematic shown in Figure 6-9(b) to operate in state 2. This state starts at $t = t_3$ and ends at $t = t_4$. The duration of this state is the same as state 1 and the reason for equal state 1 and state 2 has been explained in the previous section.

The method for how the currents and voltages of the capacitors are determined in this state are similar to the technique followed for state 1 analysis. However, the operational diagram of state 2 is different from state 1, thus the current and voltage equations will be different. Moreover, the initial capacitor voltages will be different also. In state 2, the initial value of the capacitor voltages would be the values found at the end of transition 1. Based on those values, the capacitor voltages at the end of state 2 are determined. Similar to the state 1 analysis, there are some boundary conditions for the capacitor voltages that are determined by the interconnections of the capacitor in the operational diagram of state 2. According to Figure 6-9(b),

$$\begin{aligned} V_{C4} &= V_{C3} + V_{C1}, \\ V_{C2} &= V_{C1}, \\ I_L &= I_1 + I_2 + I_4. \end{aligned} \tag{6.4.21}$$

This set of constraints is valid all through state 2 because the operational diagram does not change. Using the same method followed in state 1 analysis,

$$\begin{aligned} V_{C4}(t_4) &= V_{C4}(t_3) - I_4 \bullet \frac{0.5T}{C}, \\ V_{C3}(t_4) &= V_{C3}(t_3) + I_4 \bullet \frac{0.5T}{C}, \\ V_{C2}(t_4) &= V_{C2}(t_3) - I_2 \bullet \frac{0.5T}{C}, \\ V_{C1}(t_4) &= V_{C1}(t_3) - I_1 \bullet \frac{0.5T}{C}. \end{aligned} \tag{6.4.22}$$

Applying the boundary conditions shown in (6.4.21) and using (6.4.22),

$$V_{C4}(t_3) - I_4 \bullet \frac{T}{2C} = V_{C3}(t_3) - I_4 \bullet \frac{T}{2C} + V_{C1}(t_3) - I_1 \bullet \frac{T}{2C}$$

Thus, $I_1 = 2I_4$ (6.4.23)

In the same way, using the second constraint of (6.4.21),

$$I_1 = 2I_4 \tag{6.4.24}$$

Using (6.4.23), (6.4.24) and the third constraint of (6.4.21),

$$\begin{aligned} I_1 &= I_2 = 0.4I_L \\ I_4 &= 0.2I_L \end{aligned} \tag{6.4.25}$$

After putting the current magnitudes in (6.4.22), the following equations are found.

$$\begin{aligned} V_{C4}(t_4) &= V_{C4}(t_3) - 0.1\Delta, \\ V_{C3}(t_4) &= V_{C3}(t_3) + 0.1\Delta, \\ V_{C2}(t_4) &= V_{C2}(t_3) - 0.2\Delta, \\ V_{C1}(t_4) &= V_{C1}(t_3) - 0.2\Delta. \end{aligned} \tag{6.4.26}$$

where $\Delta = \dfrac{I_L \bullet T}{C}$

To get the exact values of the capacitor voltages at the end of state 2, the voltage equations at $t = t_3$ derived in transition 1 are used with (6.4.26). Thus, using (6.4.14), (6.4.17) and (6.4.20) and (6.4.26), the following equations are found.

$$\begin{aligned} V_{C4}(t_4) &= 0.75E + 0.6\delta_2 - 0.04\Delta, \\ V_{C3}(t_4) &= 0.5E + 0.4\delta_2 + 0.14\Delta, \\ V_{C2}(t_4) &= V_{C1}(t_4) = 0.25E + 0.2\delta_2 - 0.18\Delta. \end{aligned} \tag{6.4.27}$$

These are the final capacitor voltages at the end of state 2. Now there is one more transition to consider completing a full operating cycle. For transition 2, the voltages found in (6.4.27) will be used as the initial values, and depending on the interconnection of the capacitors, the appropriate voltages will be determined.

6.4.2 CURRENT AND VOLTAGE EQUATIONS IN TRANSITION 2

The operational diagram of the transition 2 is shown in Figure 6-12. Like the

method followed in transition 1 analysis, the analysis in transition 2 is considered as a sequential operation of two switches S_1 and S_2. Using the capacitor voltages found in state 2 analysis,

$$\begin{aligned} V_{S1} &= (E - V_{C4}(t_4) - V_{C1}(t_4)) \\ &= -0.8\delta_2 + 0.22\Delta. \end{aligned} \tag{6.4.28}$$

When S_1 is closed, the voltage source V_E is connected in series with C and C_1. Thus the voltages across them will increase once S_1 is closed. Thus, after closing S_1,

$\Delta V_{C4} = \text{change in } V_{C4}$

$= \dfrac{V_{S1}}{2}$, because C_1 and C_4 are connected in series and no other capacitors are connected to them.

Thus, $\Delta V_{C1} = \dfrac{V_{S1}}{2} = \Delta V_{C4}$. (6.4.29)

Using (6.4.26), (6.4.28) and (6.4.29),

$$V'_{C1} = V_{C1}(t_4) + \Delta V_{C1} = 0.25E - 0.2\delta_2 - 0.07\Delta. \tag{6.4.30}$$

Thus, $V_{S2} = (V_{C3}(t_4) - V_{C3}(t_4) - V'_{C1}) = 0.4\delta_2 + 0.39\Delta$. (6.4.31)

Now S_2 will be closed, and after that,

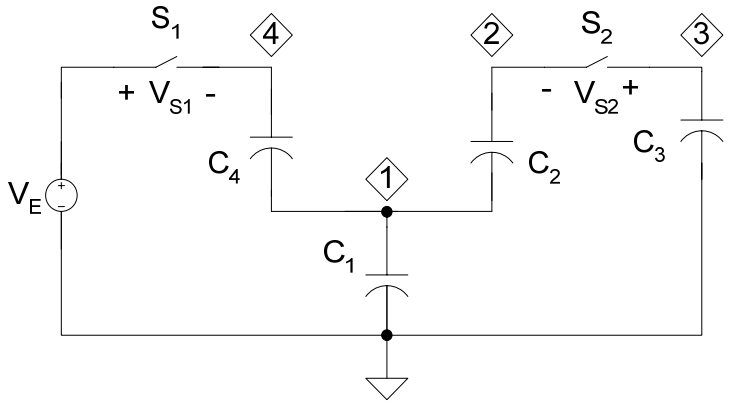


Figure 6-12. The sequential switching operation of capacitors in transition 2.

$$\Delta V_{C3} = V_{S2} \bullet \frac{C_{3eq}}{C_{3eq} + C_3} . \quad (6.4.32)$$

where C_{3eq} is the equivalent capacitance seen by C_3 at node 2 or 3.

Thus, $C_{3eq} = \frac{C_2 \bullet (C_1 + C_4)}{C_4 + C_1 + C_2} = \frac{2}{3} C$. (6.4.33)

Using (6.4.32) and (6.4.33),

$$\Delta V_{C3} = 0.4 V_{S2} = 0.16\delta_2 + 0.156\Delta . \quad (6.4.34)$$

So, $V_{C3}(t_5) = V_{C3}(t_4) - \Delta V_{C3} = 0.5E + 0.24\delta_2 - 0.016\Delta$. (6.4.35)

Due to the closing operation of S_2, voltage at node 2 will also change. Thus,

$$\Delta V_2 = V_{S2} \bullet \frac{C_3}{C_{3eq} + C_3} = 0.6 V_{S2}$$

$$= 0.24\delta_2 + 0.234\Delta.$$

(6.4.36)

As C_1 and C_2 are connected in series, a change in voltage at node 2 will change the voltage in V_{C2}, and at node 1 where C_1 and C_4 are connected in parallel. So,

$\Delta V_{C2} = \Delta V_2 \bullet \frac{C_{1eq}}{C_{1eq} + C_2}$, where C_{1eq} is the equivalent capacitance at node 1. Using (6.4.31) and (6.4.36),

$$\Delta V_{C2} = 0.6 \bullet V_{S2} \bullet \frac{2C}{2C + C} = 0.16\delta_2 + 0.156\Delta . \quad (6.4.37)$$

Now, $V_{C2}(t_5) = V_{C2}(t_4) + \Delta V_{C2}$,

Using (6.4.27) and (6.4.37),

$$V_{C2}(t_5) = 0.25E + 0.36\delta_2 - 0.024\Delta . \quad (6.4.38)$$

In the same way,

$$\Delta V_{C1} = \Delta V_2 \bullet \frac{C_2}{C_{1eq} + C_2} = 0.08\delta_2 + 0.078\Delta . \quad (6.4.39)$$

Therefore, $V_{C1}(t_5) = V'_{C1} + \Delta V_{C2}$

Using (6.4.30) and (6.4.39),

$$V_{C1}(t_5) = 0.25E - 0.12\delta_2 + 0.008\Delta . \quad (6.4.40)$$

From Figure 6-11,

$$V_{C4}(t_5) = E - V_{C1}(t_5)$$

Using (6.4.40),

$$V_{C4}(t_5) = 0.75E + 0.12\delta_2 - 0.008\Delta . \quad (6.4.41)$$

Now the converter has completed one full cycle. If the analysis is correct and the converter has a stable operation, the capacitor voltages found at the end of transition 2 ($t = t_5$) must be equal to the values assumed at the beginning of state 1 ($t = t_1$). Thus comparing (6.4.2) and (6.4.38),

$$\delta_2 = 0.36\delta_2 - 0.024\Delta$$

So, $\delta_2 = -\frac{3\Delta}{80}$. (6.4.42)

Comparing (6.4.2) and (6.4.40) and using (6.4.42),

$$\delta_1 = \frac{\Delta}{80} . \quad (6.4.43)$$

Comparing (6.4.2) and (6.4.41) and using (6.4.42),

$$\delta_4 = -\frac{\Delta}{80} . \quad (6.4.44)$$

In the same way, comparing (6.4.2) and (6.4.35) and using (6.4.42),

$$\delta_3 = -\frac{\Delta}{40}. \tag{6.4.45}$$

If these computations are correct, the values found from (6.4.42 – 6.4.45) must satisfy the boundary conditions stated in (6.4.4). From (6.4.43) and (6.4.44), it is clear that $\delta_4 = -\delta_1$. Using (6.4.42), (6.4.43) and (6.4.45),

$$\delta_2 + \delta_1 = -\frac{3\Delta}{80} + \frac{\Delta}{80} = -\frac{\Delta}{40} = \delta_3$$

Thus, the values of δ_1 to δ_4 are correct, and using these values in (6.4.2), the steady state capacitor voltages can be obtained as the following.

$$\begin{aligned} V_{C4}(t_1) &= 0.75E - \frac{\Delta}{80}, \\ V_{C3}(t_1) &= 0.5E - \frac{\Delta}{40}, \\ V_{C2}(t_1) &= 0.25E - \frac{3\Delta}{80}, \\ V_{C1}(t_1) &= 0.25E + \frac{\Delta}{80}. \end{aligned} \tag{6.4.46}$$

This is the final set of capacitor voltages in a 4-level MMCCC converter. When the converter is operated in down-conversion mode, the load voltage is the low side voltage, which is equal to V_{C1}. This analysis thus provides the load voltage during the different sub-intervals of the MMCCC operation. The analytical computation also shows that the circuit's operation is stable, and after completing a full cycle, the capacitor voltages get back to their initial values that they had at the beginning of the cycle. As a final work, the various capacitor voltages obtained for a 4 or 5-level circuit will be compared with the experimental results in Chapter 7.

CHAPTER 7

FEATURES OF THE MMCCC AND EXPERIMENTAL RESULTS

The concept and operation of the MMCCC topology has been explained in Chapter 5 with several simulation results. As a further work, Chapter 6 presents an analytical approach that verifies the startup and steady state operation of the circuit. Through those steps, the concept of the MMCCC topology has been verified and established. However, the MMCCC topology exhibits some interesting features, and these features may not be easily explained and verified through simulation and analytical approaches. In this chapter, several key features of the MMCCC topology will be explained along with necessary experimental results to get a complete proof of concept. Among the key features, the bi-directional power flow management, redundancy and faults bypass capability, and multiple load-source integration will be discussed in this chapter.

7.1 OVERVIEW OF THE MMCCC EXPERIMENTAL SETUP

A 6-level 500 W prototype of the proposed design has been constructed on the printed circuit board shown in Figure 7-1 for further verification of the new concept. For a 6-level design, 5 modules are used and each module will have its own gate drive circuit on board. Inside one module, two bootstrap gate drive circuits (IR2011) have been used to drive three IRFI540N MOSFETs. These MOSFETs have an on state resistance of 52

mΩ, and they are rated at 100 V, 20 A. An onboard dc-dc converter has been used to drive the top transistor in each module (Transistor S_{B1} in Figure 5-2). General-purpose 1000 μF 100 V electrolytic capacitors having 0.1 Ω ESR have been used in the circuit. The main board has been built in such a way that each module is connected to the main board through a 10-pin header. Thus, if there is any fault in any one of the modules, either it can be bypassed by the fault clearing circuit or it can be physically disconnected from the main board and can be replaced by another good module. This 500 W model was designed to operate up to 100V dc as V_{HV}. The schematic of the gate drive circuit is attached in the appendix.

7.2 INSTRUMENTS USED FOR THE EXPERIMENT

A Fluke 87 III multimeter has been used to measure all the voltages and currents, and a Tektronix TDS 3034B digital phosphor oscilloscope was used to record the voltage

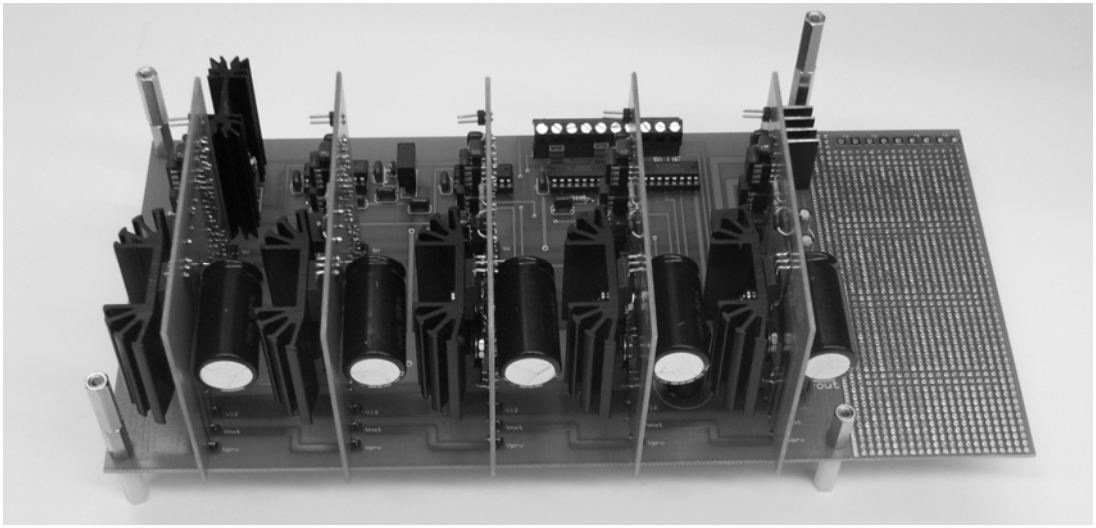


Figure 7-1. Proof of concept, the actual 500 W 6-level prototype.

and current wave shapes. A programmable load bank 3711A was used to connect resistive loads to the circuit.

7.3 Experimental Results of the MMCCC Operation

Similar to the simulation, this 6-level converter was tested in three steps to prove the concept of the MMCCC topology. Those three steps are, a) up-conversion mode, b) down conversion mode, c) battery charging mode. Each of these tests was performed multiple times to find any variation in the obtained results. For the same experiment, no significant variations among the test results were observed.

The selection of the operating frequency was also critical because of several reasons. If the circuit is operated at high frequency, it is possible to transfer the rated power using comparatively smaller capacitors. Thus, it is possible to reduce the size of the converter, and the cost will be reduced. However, there is a downside of the high frequency operation. Being a capacitor clamped topology, the circuit suffers from high switching loss at high frequency because of larger number of transistors. To reduce the switching loss, the frequency can be reduced; however, it will require larger capacitors to maintain the same power flow with the same ripple components at the output. For this reason, the switching frequency was chosen to be 10 kHz for optimum performance.

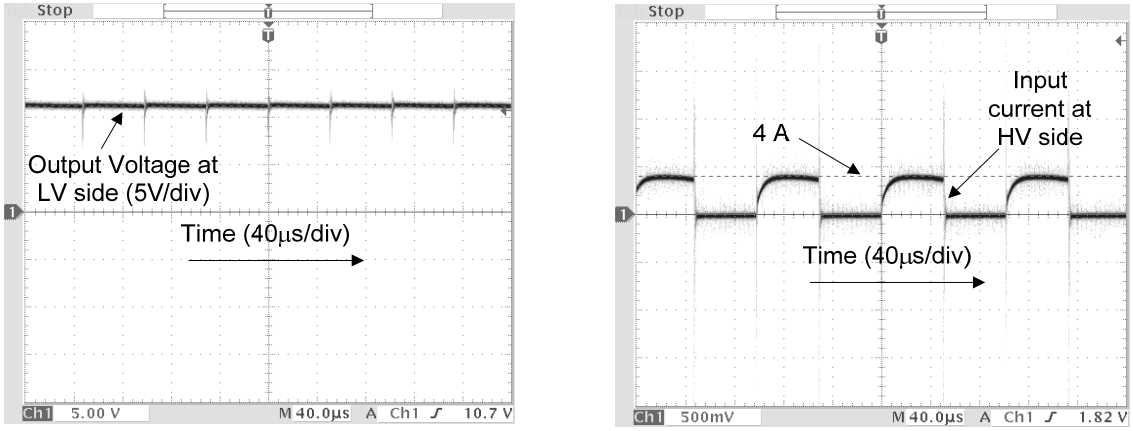
7.3.1 Down-conversion mode

In the first step, the down-conversion operation was tested by connecting a 75 V source to the high voltage side of the converter. A 1 Ω resistive load from a 3711A programmable load bank was connected across the low voltage side output, and the

voltage wave shape was recorded with the digital oscilloscope. Because the load was entirely resistive, the current will have the same wave shape like the voltage signal. Figure 7-2(a) shows the output voltage of the MMCCC, and Figure 7-2(b) shows the input current wave shape. Thus the peak input current was found to be 4 A (400 mV drop across a 0.1 Ω resistor), which is the same as found in the simulations (Figure 5-8(d)). During the testing, the conversion ratio was 6, and the average load voltage recorded was 11.92 V, which is very close to the no-load, no-loss output voltage of 12.5 V (75/6). The voltage regulation of the circuit is acceptable because the voltage drop of 0.58 V across the several series connected devices is very natural.

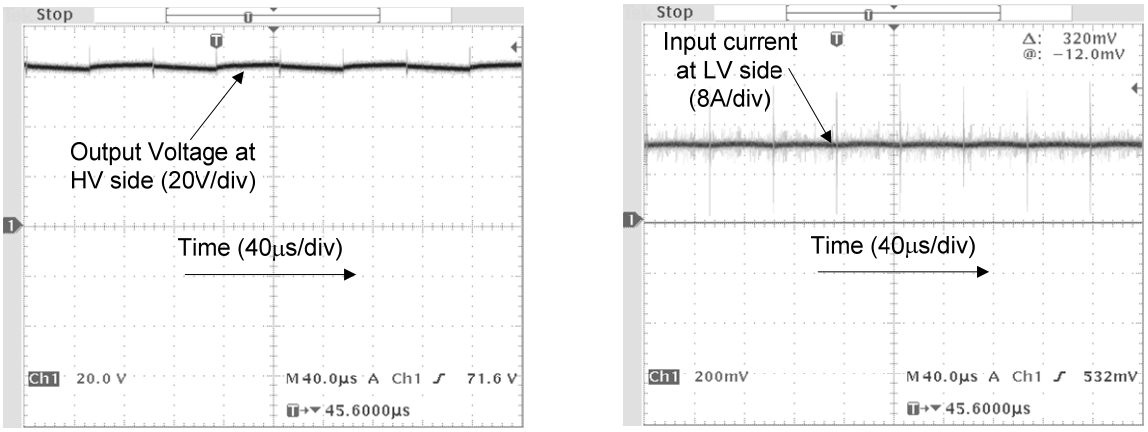
7.3.2 UP-CONVERSION MODE

Figure 7-3 summarizes the experimental results in the up conversion mode. In this up conversion mode, a 65.3 V output is produced from a 12 V input with 30 Ω loading at



(a) (b)

Figure 7-2. The experimental results for the down-conversion mode, a) output voltage, b) input current (1 V = 10 A).



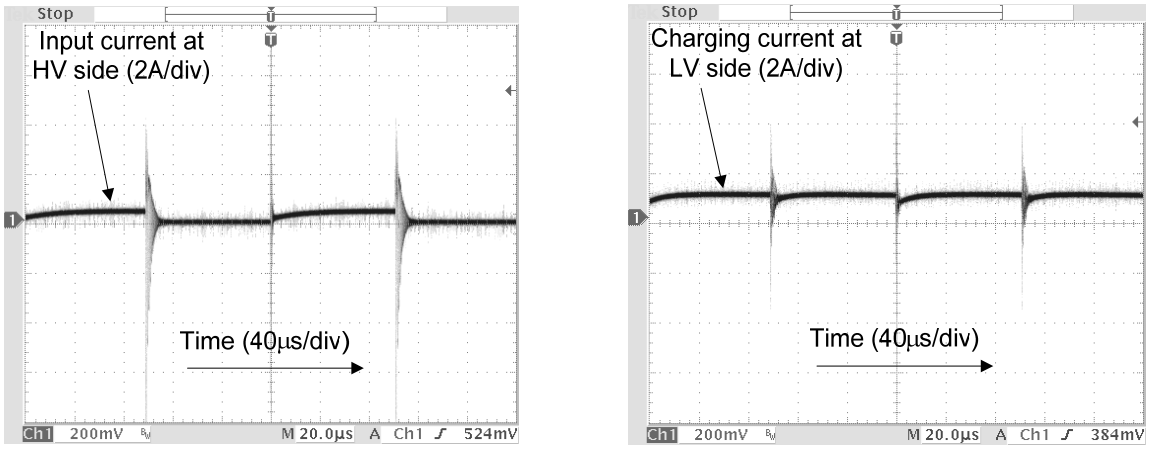
(a) (b)

Figure 7-3. The experimental results for the up-conversion mode, (a) output voltage, (b) input current (100 mV = 4 A).

the high voltage side. The output voltage is shown in Figure 7-3(a). The input current is shown in Figure 7-3(b). From the experimental result of this mode, it is clear that the converter has a continuous input current in the up-conversion mode. However, the output voltage in up-conversion mode has larger ripple because the converter transfers power to the high voltage side for 50% time of the total time period. A large capacitor of 1000 μF connected at the output maintains the continuous wave shape of the output voltage.

7.3.3 BATTERY CHARGING MODE

In the battery-charging mode, an 80 V source was connected at the high voltage side, and the low voltage side of the converter was connected to a 12 V lead-acid battery. Figure 7-4(a) shows the input current and (b) shows the output or charging current. For this setup, the maximum charging current to the battery was only 1.2 A which is much less than the simulation result. The reason for this low current was the increased battery



(a) (b)

Figure 7-4. The experimental results for the battery charging mode, a) input current (100 mV = 1 A), b) charging current (100 mV = 1 A).

voltage, which was eventually 13.2 V while taking the measurement. In the simulation, the battery voltage was considered constant at 12 V.

7.3.4 EFFICIENCY MEASUREMENTS

The converter was tested to measure the efficiency at different operating conditions. Figure 7-5 shows the efficiency of the converter at different loading conditions for both up and down conversion mode. In this figure, it is seen that a maximum efficiency of 99.1% was achieved at 20 W power output (in up-conversion mode). The relatively higher on-state resistance (52 mΩ) of the transistors causes the efficiency to drop at higher loading conditions. However, when the converter is designed for higher power rating, larger MOSFETs will ensure low on-state loss and better efficiency at higher output power. Although the high efficiency level of 99% is slightly on the optimistic side, an operating efficiency in the range of 94% - 97% is expected

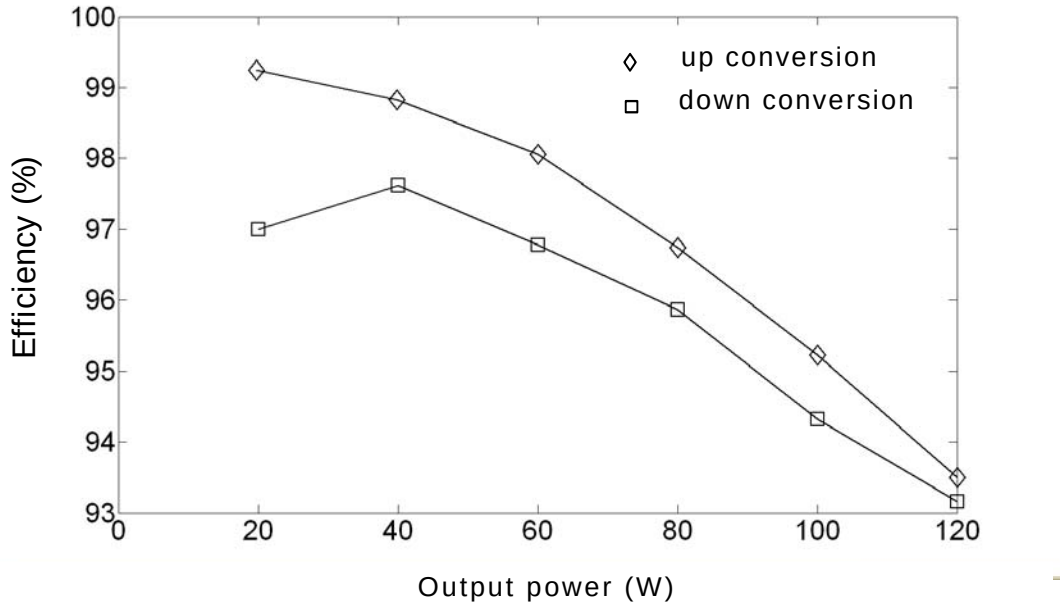


Figure 7-5. The efficiency of the MMCCC at different power output levels.

from the circuit with improved MOSFET and capacitor selection. This result is also consistent with the efficiency obtained from the FCMDC circuit (Fig. 13 in [27]).

7.2. MULTIPLE LOAD-SOURCE INTEGRATION

It was mentioned in Chapter 5 that the modular nature of the MMCCC topology allows the integration of multiple loads and sources at the same time. In this section, that concept will be discussed in more detail with several experimental results.

7.2.1. SOURCE INTEGRATION

The modular MMCCC topology can be used to integrate multiple voltage sources simultaneously to build a power management system among various voltage sources. The 6-level MMCCC circuit shown in Figure 7-6 has 5 modules, and every module's input

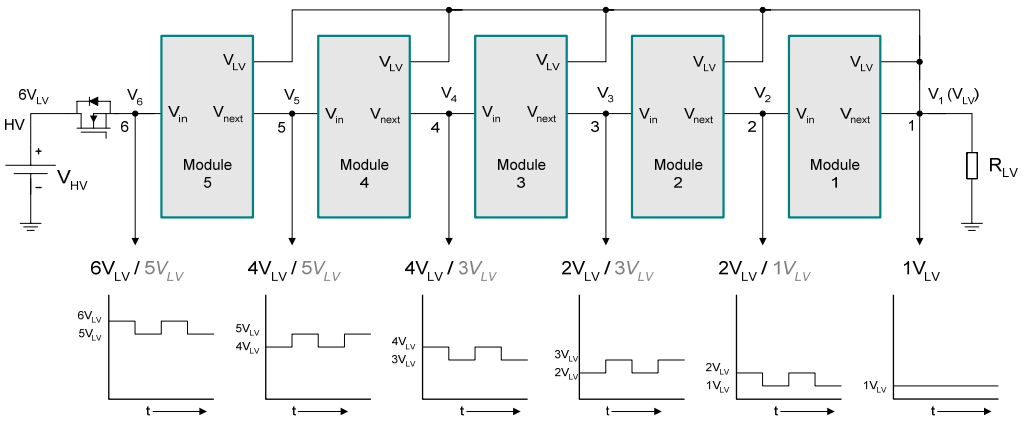


Figure 7-6. The simulation results of the intermediate node voltages in a 6-level MMCCC circuit. The voltage magnitude at any node printed in black is the value during state 1, the value printed in gray is the voltage magnitude during state 2.

port creates a voltage node in the circuit. Figure 7-6 also shows the analytically computed voltage levels generated at nodes 1 to 6. It is seen that each node produces a time varying dc voltage which is a combination of an ac voltage superimposed on a dc value. The amplitude of the ac voltage swing is equal to 1 V_{LV} or V_1. The voltages at different nodes are summarized in Table 7-1.

Using the time-varying nature of these node voltages, some additional voltage sources can be connected at these nodes. Inherently, the MMCCC circuit is a bi-directional converter and it can be used to manage the power flow between V_{HV} and V_{LV} (Figure 7-6) by controlling the conversion ratio (CR) of the circuit. Moreover, the number of active levels present in the circuit governs the CR. In this way, the added functionality of the multiple source integration can facilitate a system to integrate up to 7 voltage sources for a 6-level converter; which means 5 additional voltage sources at nodes 2 to 6 can be connected. This feature may be used to integrate various kinds of

Table 7-1. The time varying node voltages of a 6-level MMCCC circuit.

State	Active Switches	V_6	V_5	V_4	V_3	V_2
1	S_{R1}-S_{R7}	$6V_{LV}$	$4V_{LV}$	$4V_{LV}$	$2V_{LV}$	$2V_{LV}$
2	S_{B1}-S_{B6}	$5V_{LV}$	$5V_{LV}$	$3V_{LV}$	$3V_{LV}$	$1V_{LV}$

energy sources such as solar cell, fuel cell, battery etc. having different voltages in the same system.

Table 7-1 shows the simulated values of the time varying voltages at different nodes of the 6-level MMCCC circuit for the two states present in the circuit. At state 1, the voltage at node 5 is 4 V_{LV}, and during state 2, the voltage is 5 V_{LV}. Thus, if an external voltage source of amplitude 4 V_{LV} is connected to node 2, it will contribute power along with V_{HV} to the low voltage side of the converter during state 1. During state 2, the voltage at node 5 becomes 5 V_{LV}, which is higher than the external source voltage; thus the converter will not draw any power from the external source connected at this node. In the same way, other voltage sources can be connected at nodes 2, 3, 4, and 6.

While connecting multiple sources in the system, one issue needs to be considered to keep the output voltage ripple the same as in the case when only V_{HV} is connected to the system. To achieve this, the current shared by the external sources must be in phase with the current provided by V_{HV}. Table 5-1 shows that the converter takes power from V_{HV} during state 1 only. Thus, the additional voltage sources must be connected in the system in such a way that they provide power during state 1 only. As mentioned earlier,

the magnitude of an external voltage source needs to be close to the lower value among the two voltage levels present at any node, and this is required to bring a balance between the voltage at the node and the external source. Thus, if an external voltage source needs to be connected at node 6, its magnitude needs to be close to 5 V_{LV}. At node 6, the voltage varies between 6 V_{LV} and 5 V_{LV}, and during state 1, the voltage is 6 V_{LV}. Thus, it is not possible to connect a voltage source at node 6 while keeping the output voltage ripple unaffected. For the same reason, node 4 and node 2 will not be suitable for integrating a voltage source in this 6-level converter. Figure 7-7 shows the integration of two external sources connected at nodes 3 and 5, because they share the load current during state 1 only. However, it is always possible to connect voltage sources at any node, but a compromise must be made with the output voltage ripple.

7.2.2 Load Integration

Another advantage of this integration feature is the ability to connect multiple loads at the same time, and having the loads shared among the several voltage sources. Figure 7-6 shows the no-load voltages at different nodes of the MMCCC circuit. Nodes 2-6 generate time varying dc voltages; however, a dc load cannot be connected between any of these nodes and ground. From Figure 7-6, it can be observed that the time varying voltage at node 2, 4, and 6 have the same phase. This is true for node 3 and 5 also. Thus, it is possible to connect a load in various ways between these in-phase nodes. Figure 7-7 shows how loads can be connected between nodes (6, 4), (5, 3), and (4, 2) to obtain a constant dc voltage across the loads. The voltage difference between two adjacent in-phase nodes is 2 V_{LV}. In the same way, the voltage difference between node 6 and 2

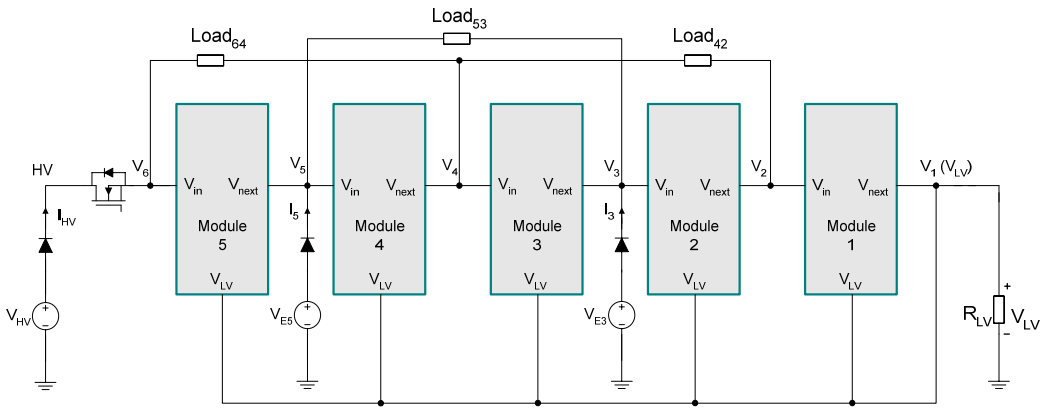


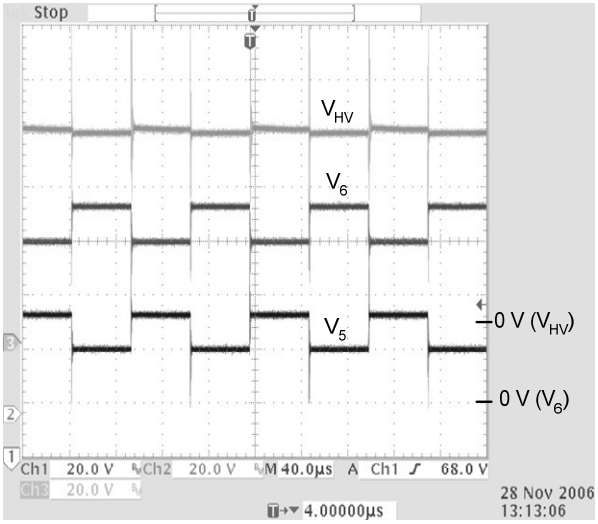
Figure 7-7. The schematic diagram of the integration of multiple sources and loads in a 6-level MMCCC circuit.

would be $4V_{LV}$. Thus, it is possible to connect multiple loads of 1 V_{LV}, 2 V_{LV}, and 4 V_{LV} simultaneously in a 6-level MMCCC circuit. In this way, the entire converter can be considered as a dc transformer with multiple taps.

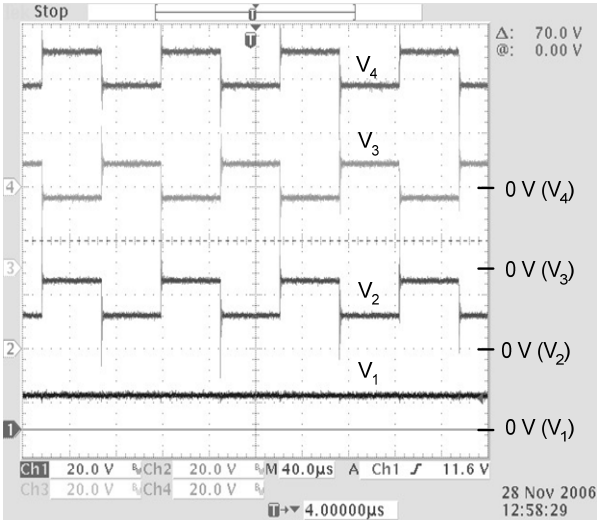
7.2.3 Experimental Results

To verify the concept of integrating multiple loads and sources in the circuit, an experimental setup was made, and the schematic in Figure 7-7 was followed. A 500 W 6-level MMCCC prototype shown in Figure 7-1 was used. Three bench top power supplies were used as V_{HV}, V_{E5}, and V_{E3}, and a diode was used in series with each voltage source to protect the power supplies from reverse power flow. A 3 Ω load was used as R_{LV}, and two 24 Ω loads were used as $Load_{42}$ and $Load_{53}$. In addition to them, one 48 Ω load was used as a load connected between node 6 and 2. The main input voltage V_{HV} was kept at 75 V. Figure 7-8(a) shows the no-load voltages at HV (the cathode terminal of the diode connected to V_{HV}), V_6 and V_5 nodes.

Fig. 7-8(b) shows the voltages recorded at V_4, V_3, V_2, and V_1 nodes. These



(a)

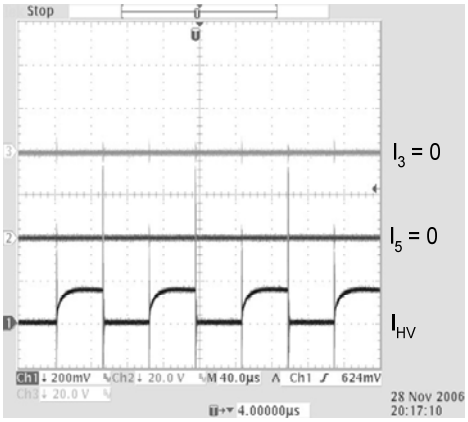


(b)

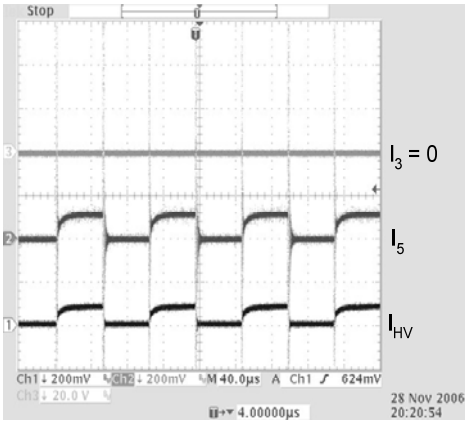
Figure 7-8. The experimental result of the node voltages in a 6-level MMCCC circuit at no-load condition; (a) voltages V_{HV}, V_6, and V_5 (b) voltages V_4, V_3, V_2, and V_1. The converter was operated in down-conversion mode.

voltages exhibit the same variations in phase and magnitude as that found in the simulation (shown in Figure 7-6) and by analytical computation. The voltages at nodes 2-6 have a voltage swing of 1 V_{LV}. Thus, the voltage at node 2 varies between 12.3 V and 25 V. In addition, the voltages at 2, 4 and 6 exhibit the same phase, and node 3 and 5 are in phase also. There was a small variation found at HV node, although it was supposed to be a constant value of 75 V obtained from V_{HV}. This voltage was measured at the converter board and not across the power supply terminals. Due to the voltage drop across the current sampling resistor and wire stray inductance, a small ripple was observed at this voltage input port of the converter.

Figures 7-9 and 7-10 show how three sources connected to the converter can share the total load current simultaneously. For this experiment, a 3 Ω resistive load was connected across the V_1 node and ground. This power sharing operation was tested in two steps. In the first case, V_{E5} was kept less than 48 V and V_{E3} was kept less than 24 V. During this time, there was no power flow from these two sources, and this is shown in Figure 7-9(a). In this step, V_{HV} was kept at 75.8 V. When V_{E5} is varied to go beyond 48 V level, it starts to share the power delivered to the output side, and this is shown in Figure 7-9(b). When V_{E5} reaches 52 V, it delivers the entire power to the load and no current is drawn from the V_{HV} source. This is shown in Figure 7-9(c). However, if V_{HV} is removed from the system, V_{E5} can provide the total power to the load with a voltage lower than 52 V. This time V_5 (before connecting V_{E5}) decreases due to the absence of any current injected by V_{HV}, and a lower V_{E5} is required to flow the same current to load as before when V_{HV} was present.



(a)



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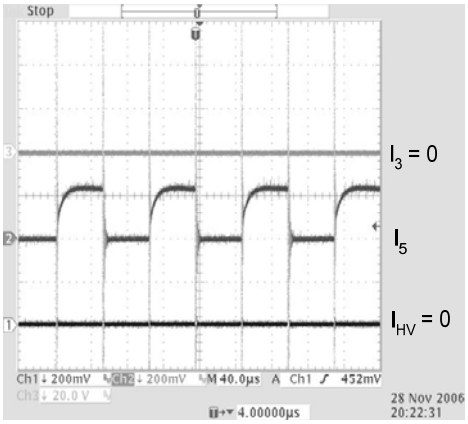
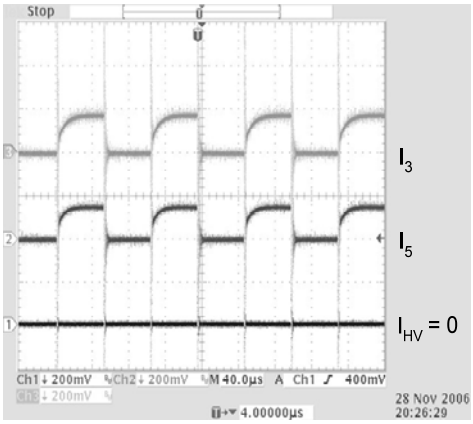
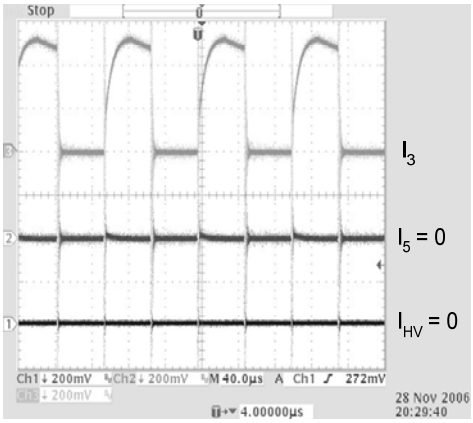


(c)

Figure 7-9. Experimental results of the input currents (2 A/div) shared by three sources (V_{HV}, V_{E5}, and V_{E3} in Figure 7-7). (a) total current is provided by V_{HV} (75.8 V), (b) current is shared by V_{HV} and V_{E5} (51.8 V), (c) total current is provided by V_{E5} (52 V) only.



(a)



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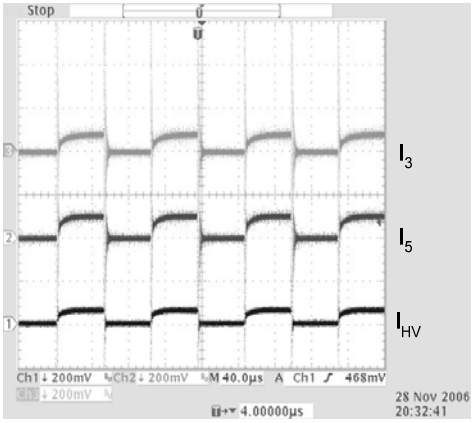


(c)

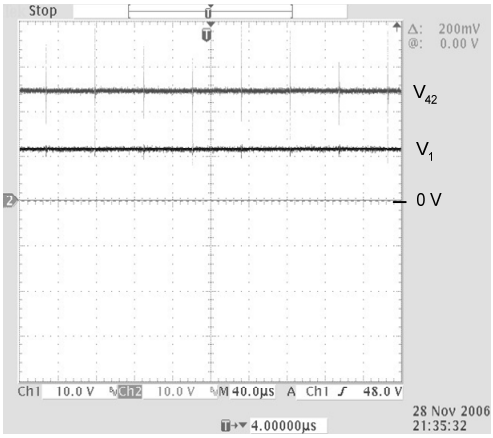
Figure 7-10. The experimental result of the input currents (2A/div) shared by three sources (V_{HV}, V_{E5}, and V_{E3} in Figure 7-7). (a) current is shared by V_{E5} (52 V) and V_{E3} (26.75 V), (b) total current is provided by V_{E3} (30.7 V) only, (c) total current is shared by V_{HV}, (75.9 V), V_{E5} (51.2 V), and V_{E3} (26.07 V).

In the second case, V_{E3} was used to share the load current. Figure 7-10(a) shows the result when the magnitude of V_{E3} was raised to 26.75 V so that it starts to share the load current with V_{E5}. This time, V_{HV} and V_{E5} were kept the same as they were in case 1. When V_{E3} was raised to 30.7 V, it provided the entire power to the load, and power delivered by V_{HV} and V_{E5} became zero. This is shown in Figure 7-10(b). This implies that, if V_{HV} and V_{E5} were removed from the system or become inactive due to a fault, V_{E3} can still deliver the desired total power with a voltage level of 30.7 V. Finally, when the magnitude of V_{E5} and V_{E3} were reduced, V_{HV} was back in operation, and all of these three dc sources become sharing the load current again. This is shown in Figure 7-10(c). The six experimental steps discussed using Figure 7-9 and Figure 7-10 are summarized in Table 7-2. In this table, the voltages at node 3, 5, and HV are enumerated for different current sharing modes.

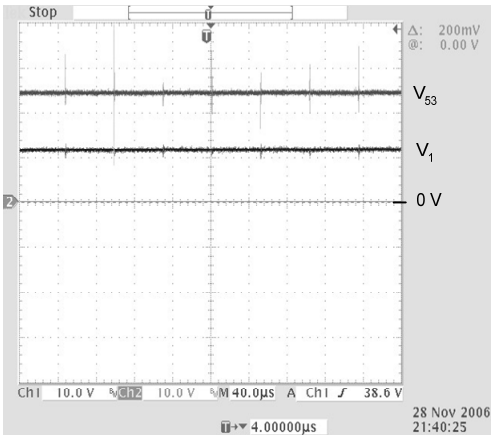
Figure 7-11 explains the multiple load integration method in the system. A 24 Ω load was connected between node 4 and 2 ($Load_{42}$), and a 3 Ω load (R_{LV}) was present at node V_1. The voltages across these loads are shown in Figure 7-11(a), and it can be seen that the voltage across $Load_{42}$ is almost 2 V_{LV} as expected. Figure 7-11(b) shows the load

Table 7- 2. Experimental setup of the node voltages for demonstrating power sharing.

Step	1	2	3	4	5	6
V_{HV}	75.8 V	75.8 V	75.8 V	75.8 V	75.8 V	75.9 V
V_5	51 V	51.8 V	52 V	52 V	52 V	51.2 V
V_3	26 V	26 V	26 V	26.8 V	30.7 V	26.1 V



(a)



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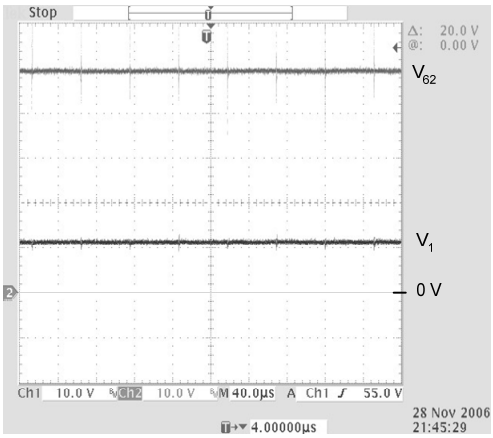


(c)

Figure 7-11. Experimental results of the load voltages connected between intermediate nodes. (a) V_1 and V_{42}; and V_{42} is two times V_1, (b) V_{53} and V_1, (c) V_{62} and V_1; and V_{62} is 4 times V_1.

voltages when R_{LV} and $Load_{53}$ (24 Ω) are present in the circuit. Similar to $Load_{42}$, $Load_{53}$ also experiences a voltage of approximately 2 V_{LV}. In Figure 7-11(c), the load voltage at V_1 node and voltage across $Load_{62}$ (48 Ω) are shown, and voltage across $Load_{62}$ was found to be almost 4 times V_{LV} or V_1. These experiments prove that 3 different kinds of loads having voltages 1 V_{LV}, 2 V_{LV}, and 4 V_{LV} can be connected simultaneously in the circuit.

7.3 Redundancy and Fault Bypass Capability

One of the unique features of this converter design different from many other converters is its modularity. Whenever there exists any modularity in dc-dc converters, it can be used to enhance the different characteristics of the converter such as voltage and current ratings, conversion ratio, and to provide redundancy. Redundancy is a highly desirable feature in high power electronic circuits, and it can ensure uninterrupted operation during faults. The redundancy feature can localize the fault in the associated module when it occurs, and using some control circuits, the faulty module can be removed and replaced with a good module. The next sections will discuss this feature in the MMCCC circuit.

The proposed MMCCC circuit is made from multiple modules, and the number of modules is governed by the conversion ratio. The present converter was designed for a conversion ratio of 5, and thus it has 4 modules. Adding or subtracting a level or module, the conversion ratio can be made 6 or 4. To implement redundancy and fault bypass features in the circuit, a control circuit is used on the main board where all the modules are connected to it through some headers. At the same time, an additional control and

fault detection circuit is installed inside every module.

To take the full advantage of the modular structure, it is necessary to introduce redundancy in the circuit. This unique feature of the MMCCC topology enables an uninterrupted operation when there is a fault in any of the modules. When transistor SB_1 in Figure 5-2 is permanently on and the other two transistors are permanently off, the module works as a bypass module. In this condition, the module does not participate in the operation of the converter and simply bypasses the current through itself. During normal operation that is defined as the active state, all three transistors in a module are controlled by the proper gate-driving signal. Thus, any module can be operated in either the active state or bypass state by activating the appropriate control signals in a module.

To achieve some level of redundancy in the system, some modules are operated in bypass state and the remaining modules operate in the active states. When a fault is detected inside any of the active modules, the main board control circuit detects the location of the fault and sends a signal to the faulty module and thereby bypasses the module. However, to keep the conversion ratio (CR) unchanged, the control circuit would then engage one of the redundant modules, which was in a bypass state. As a result, an uninterrupted operation can be ensured. The level of redundancy is application specific, and depending on the application of the converter, the number of redundant levels can be extended to any desired level.

Figure 7-12 demonstrates the redundancy and fault bypass operation, and shows how the converter can withstand a fault and still continue its normal operation. A 3-level converter with two redundant modules is shown in Figure 7-12. During normal

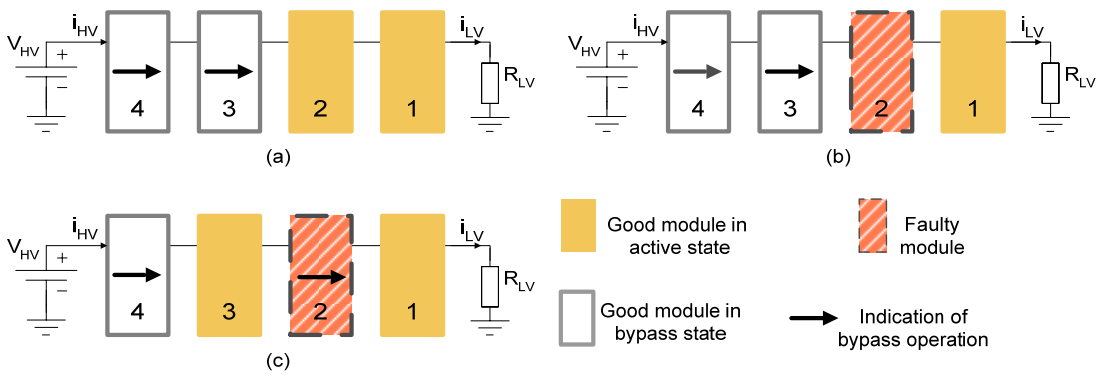


Figure 7-12. The redundancy and fault withstand capability of the converter, (a) a three level converter running at normal operating mode with two redundant modules (3 and 4), (b) a fault occurred in module 2, (c) module 2 went into bypass mode and replaced by module 3.

operation, module 1 and 2 work as active modules, and module 3 and 4 work as bypass module. This is shown in Figure 7-12(a). Figure 7-12(b) shows a situation where a fault has occurred in module 2. To keep the CR unchanged, the converter needs two active modules in the system. After the control circuit detects the location of the fault, it bypasses module 2 and engages module 3 into an active state, which was formerly in bypass state. This operation is shown in Figure 7-12(c). From this moment on, modules 1 and 3 operate as active modules, and modules 2 and 4 serve as bypass modules. At this point, the present state of the circuit is capable of handling one more fault which can be bypassed by activating module 4.

7.4. BI-DIRECTIONAL POWER MANAGEMENT

For a dual bus system, a bi-directional converter can transfer power from high voltage bus to a low voltage bus or vice-versa. The CR of the converter depends upon the number of active modules and the duty ratio of the gate driving signal. Two different gate

drive signals are fed to each of the modules in the MMCCC converter, and this pair of signals is common to all modules. When the number of active modules is even, these two signals have durations of 0.6T and 0.4T, where T is the time period of the gate driving signals. For an odd number of active modules, each of the signals has duration of 0.5T. Thus, when 4 modules are active, the CR is 5, and the CR is 6 for 5 active modules in the system.

Table 7-3 shows that for a 5-level converter having an RVS greater than 5, power can only flow from the high voltage side to the low voltage side. In this situation, CR must be greater than RVS to transfer power in the opposite direction (low to high). This requirement can be mitigated by adding one redundant level to the circuit and thereby the CR becomes 6. On the other hand, if RVS is less than 5, the default direction of power flow is from low voltage side to high voltage side. To transfer power to the opposite direction, CR must be reduced so that it is less than RVS. This can be done by subtracting one module from the system, and the CR will become 4.

Table 7- 3. Direction of power flow at different battery voltages.

Case	Ratio of battery voltages	Power flow direction	Power flow from high side to low side	Power flow from low side to high side
1	>5	High to Low	Possible	Not possible
2	<5	Low to High	Not possible	Possible

For any number of active modules, if the duty ratio of the two gate driving signals are reduced, the CR would increase from the previous value, and would no longer be an integer value. Thus, for 4 active modules (CR = 5), if the two signals are reduced from their original value of 0.6T and 0.4T, a non-integer CR of more than 5 is obtained. This phenomenon is used to control the power in any direction. To implement this variable duty ratio, a precision control circuit is used in open loop or closed loop configuration. In the closed loop operation, a voltage proportional to the output current is fed back to the control circuit, and the control circuit sends proper signal to the monostable circuit to control the output duty ratio. In this way, the CR value can be fractionally controlled in the range 4 to 5 and 5 to 6 for the number of active modules 3 and 4 respectively. The schematic of the variable duty ratio generator circuit is attached in the appendix. In the open loop configuration, the duty ratio thereby the output current is controlled manually.

When a multilevel converter is used to transfer power between two voltage sources, the direction of power flow is governed by the ratio of the two voltage sources (RVS) and the CR. Unlike the RVS, the CR is usually an integer value for capacitor clamped converters, and when the CR is greater than the RVS, the low voltage source transfers power to the high voltage (HV) side. On the other hand, a CR smaller than the RVS will force the converter to transfer power from the high voltage side to the low voltage (LV) side. However, depending on the source voltages, RVS may change; and for a fixed CR, the power flow may change its direction, even if it is not desired. In this situation, a variable CR could solve this problem, and in the MMCCC circuit, the CR value can be changed by adding or subtracting a level in the system. Thus, a 6-level

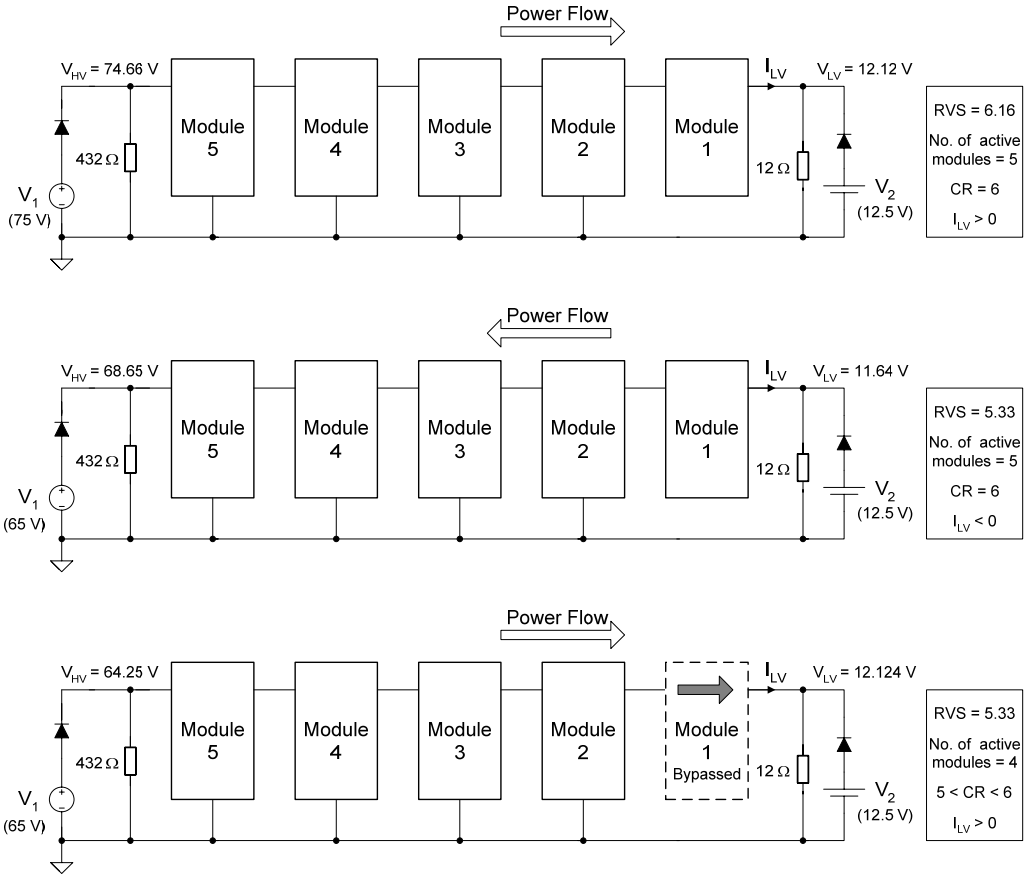
converter can be operated in either a 5 or 6 level configuration. The experimental results of this operation are shown in Figure 7-13.

Figure 7-13(a) shows the operation when the high voltage source is feeding power to the low voltage side. The CR was 6, and the RVS was 6.16. When V_1 is reduced to 65 V, RVS drops to 5.33, and the direction of power flow is reversed. This is shown in Figure 7-13(b). To maintain the same current to the low voltage side, the CR of the circuit needs to be less than 5.33, and this is done by bypassing a level, and changing the duty ratio of the gate drive signals. This operation is shown in Figure 7-13(c). If the gate drive signal is not controlled, 4 active modules will produce a CR of 5, and the LV side current will be very high. Thus, by reducing the duty ratio of the gate drive signals, a CR close to 5.33 is obtained, and the LV side current can be controlled. The new average I_{LV} was controlled at 1 A.

Figure 7-14 shows the experimental results of the bi-directional power management of a 6-level MMCCC converter. Figure 7-14(a) shows the case when V_1 is sending power to the LV side, and the average I_{LV} was around 1 A. When V_1 is 65 V, the I_{LV} becomes negative, and V_2 feeds power to the HV side as the power flow direction has changed. This is shown in Figure 7-14(b). To maintain the same current to the LV side, module 1 is bypassed, and the gate signal duty ratio is changed. Thus I_{LV} becomes positive again, and this is shown in Figure 7-14(c).

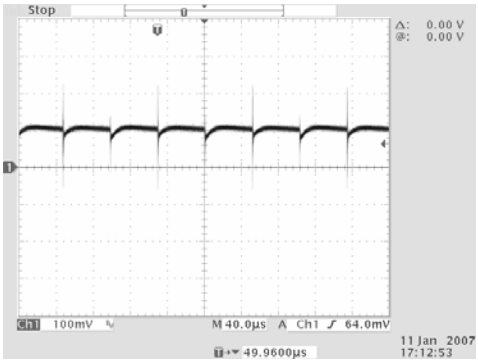
7.5 GENERATING AC OUTPUT FROM MMCCC

By virtue of the modular nature, the MMCCC circuit can produce multiple dc voltages at different intermediate nodes of the converter. In addition, it is possible



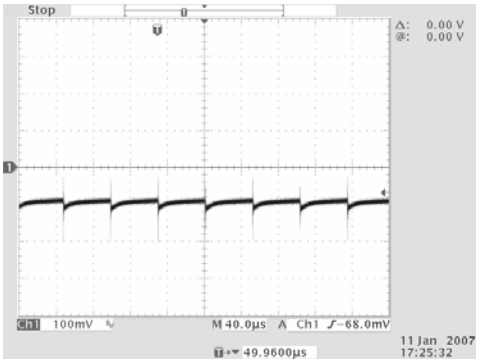
to

Figure 7-13. The bi-directional power management operation, (a) V_1 is feeding power to LV side using 5 active modules, (b) V_1 has decreased, power flow direction has been reversed, and I_{LV} has become negative; V_2 is feeding power to HV side, (c) module 1 has been bypassed and a conversion ratio less than 6 is achieved using 4 active modules.



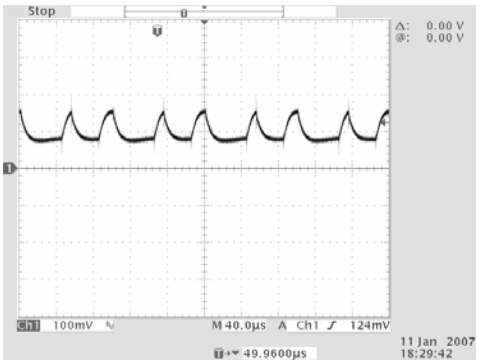
I_{LV} (avg.) ≈ 1 A

(a)



I_{LV} (avg.) ≈ –1 A

(b)



I_{LV} (avg.) ≈ 1 A

(c)

Figure 7-14. Experimental results of the bi-directional power management operation; (a) I_{LV} (10A/V) when V_1 is feeding power to the LV side, (b) I_{LV} (10A/V) when V_2 is feeding power to the HV side, (c) I_{LV} (10A/V) when module 1 is bypassed and the duty ratio of the gate driving signal is controlled to achieve 5<CR<6.

to generate multiple ac output voltages from the circuit. These ac outputs can be used to run ac loads, or transformers could be connected at these outputs to generate isolated ac or dc voltages (after rectification). In Figure 7-15, the negative terminal of the capacitor in each module produces a time varying voltage, and the MMCCC circuit shown in this figure has 5 of these nodes. The voltages at these nodes were investigated and some promising results were discovered. To validate the concept that the MMCCC circuit can produce ac outputs, several simulation and experiments were done, and the operational MMCCC circuit with ac outputs is shown in Figure 7-16.

The ac operation of the MMCCC circuit is mirror to the dc operation. When multiple dc loads are connected to the MMCCC converter, they are connected across alternate nodes (shown in Figure 7-7). However, an MMCCC produces ac outputs across two adjacent nodes of the five nodes shown in Figure 7-15 (V1a, V2a, V3a, V4a, and V5a). Thus, when a load is connected across V1a and V2a, it experiences an ac voltage with amplitude of 1 V_{LV}. However, zero voltage is found across two alternate nodes such as V1a and V3a. The simulation and experimental results of this operation is shown in the next section.

7.5.1. Simulation Results

A 6-level 5 kW MMCCC converter was simulated in PSIM to generate ac voltages across the loads connected to the converter. As a second phase of the prototype fabrication, a 5 kW MMCCC converter was also constructed and tested. The operational diagram shown in Figure 7-16 was followed to get the simulation and experimental results. Three 20 Ω resistors were used as R12, R23, and R14 and a 10 Ω resistor was

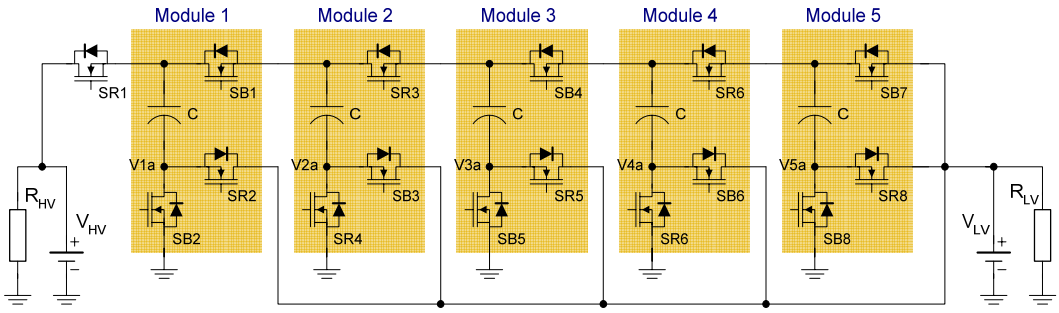


Figure 7-15. The 6-level MMCCC circuit shows intermediate nodes to produce ac voltage outputs.

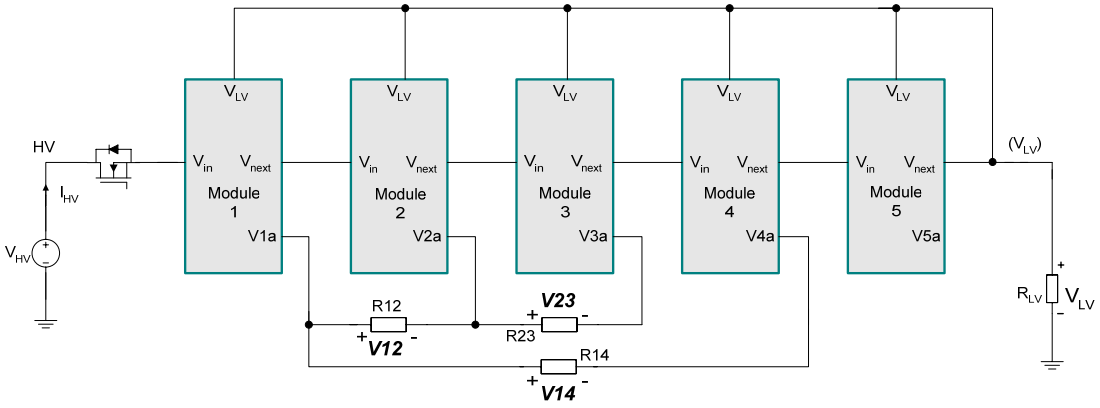


Figure 7-16. The operational diagram of a 6-level MMCCC to produce ac outputs in simulation and experiment.

used as R_{LV} in both simulation and experiment. This 5 kW converter was operated in down conversion mode at 10 kHz switching frequency, and the HV side was connected to a 240 V dc source. The simulation results are summarized in Figure 7-17.

Figure 7-17(a) shows the dc output at the loaded LV node, and it shows that the output dc voltage is around 40 V, which is close to the theoretical value (240V/6). The ac output across R12 is shown in Figure 7-17(b), and it shows that $V12$ is close to 40 V (1 V_{LV}) also. Figure 7-17(c) shows the simulated voltage across R23, and Figure 7-17(d) shows $V14$. It is found that $V12$ and $V23$ will have opposite phases; $V12$ and $V14$ are in phase.

7.5.2 Experimental Results

Figure 7-18 shows the experimental results of the of the ac outputs produced by a 6-level MMCCC circuit. For a 240 V dc input, the circuit should produce a 40 V dc output at the LV side, and a 40 V ac output across two adjacent nodes. Figure 7-18(a) shows the recorded voltages at LV node and across R12, and the ac output $V12$ has an amplitude close to 40 V. At the same time the dc output V_{LV} was close to the theoretical figure too (actual value recorded was 39.3 V). This step of the experiment proves that the circuit can simultaneously generate dc and ac outputs. Figure 7-18(b) compares the voltages $V12$ and $V23$ on the same window, and it shows that $V12$ is out of phase of $V23$. Figure 7-18(c) compares the voltages $V12$ and $V14$, and it is found that they are in phase. These experimental results match closely to the simulation results shown in Figure 7-17.

The ac output produced by the MMCCC circuit has a frequency of 10 kHz, which is equal to the switching frequency of the converter. These ac outputs can be directly

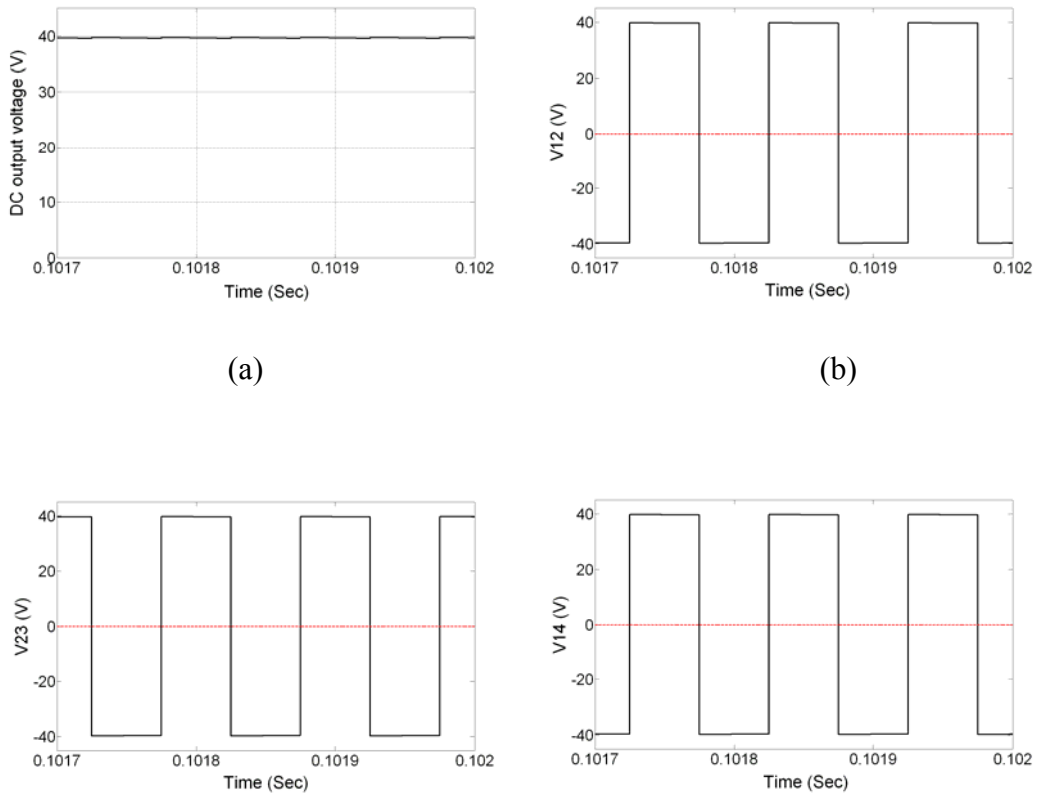
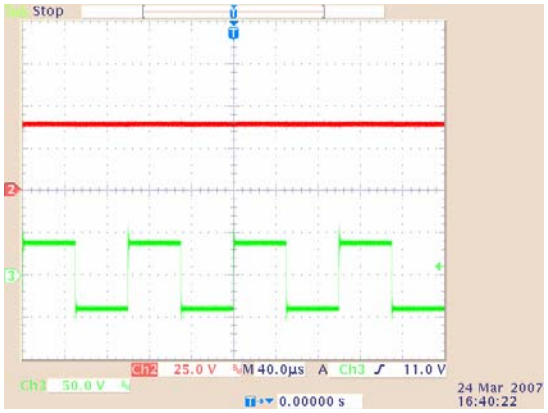
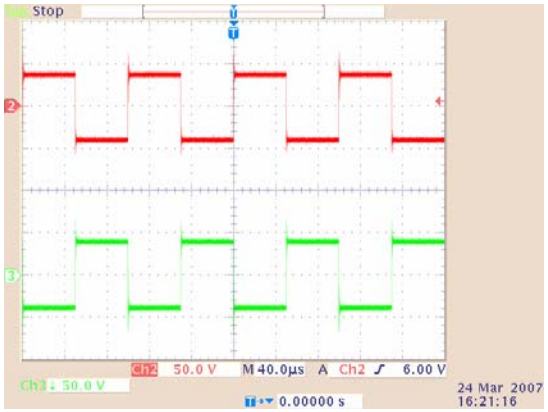


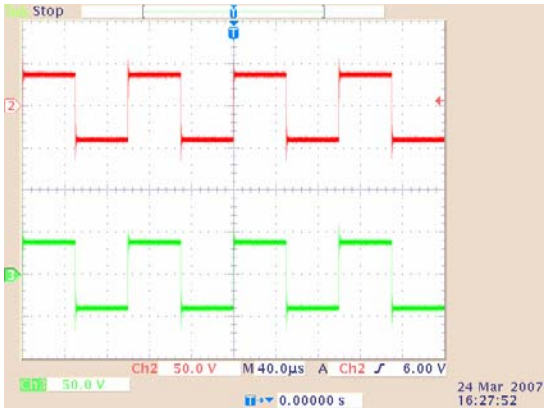
Figure 7-17. The simulation results of the 5 kW MMCCC to generate ac and dc outputs simultaneously. (a) dc output at LV node, (b) *V*12, (c) *V*23, (d) *V*14.



(a)



(b)



(c)

Figure 7-18. The experimental results of the 5 kW MMCCC circuit. (a) V_{LV} (25V/div) and $V12$ (50V/div), (b) $V12$ and $V23$ (50V/div), (c) $V12$ (50V/div) and $V14$ (50V/div).

connected to any high frequency ac load; or these outputs can be rectified, and dc outputs of magnitude 1 V_{LV} can be achieved. Thus, to produce ac or dc voltages having amplitudes different from 1 V_{LV}, transformers can be coupled to these outputs. Using transformers, it is possible to generate various ac voltages, and by connecting a rectifier circuit, it is possible to produce various dc outputs also. In this way, the conversion ratio of the converter can be varied in a wide range, and very low voltage dc loads can be connected to the system without needing any additional step-down converter circuit. The 5 kW prototype of the MMCCC circuit featuring this power management option is shown in Figure 7-19.

7.6 HIGH FREQUENCY OPERATION

The new converter has the flexibility to be operated at higher switching frequency compared to the FCMDC circuit while having the same components used in the circuit. In capacitor clamped circuits, it is always desirable to run the circuit at a higher frequency so that smaller capacitors can be used to accomplish the same amount of

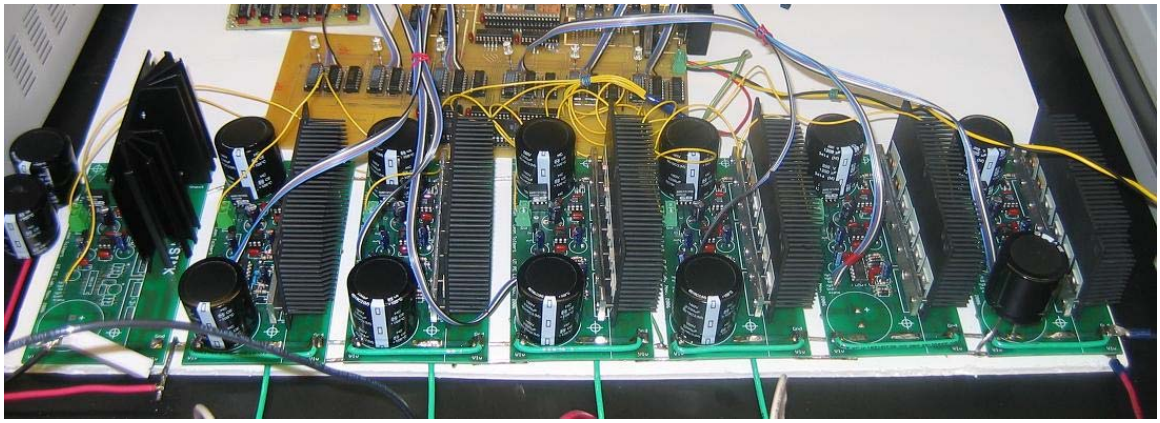


Figure 7-19. The proof of concept; the 6-level 5 kW MMCCC with 6 modules. The sixth module (first one from right) is bypassed for normal operation.

energy transfer at a faster rate. The use of smaller capacitors save space and cost and makes the converter more compact and cost effective.

The simpler switching scheme enables high-speed operation for the new MMCCC circuit. In a conventional FCMDC, the permitted time for charging/discharging of any capacitor depends on the conversion ratio. Thus for a 5-level converter running at frequency f_s, the allowable charging/discharging time is $T_s/5$ ($T_s = 1/f_s$). As the circuit is based on capacitive energy transfer, the allowable time to charge or discharge a capacitor is very crucial as the RC time constant of the capacitor dominates the charging/discharging profile. If this time is the minimum for a complete charging/discharging operation considering a specific amount of ripple at the output, the switching frequency of the circuit must be less than or equal to f_s. However, this problem is eliminated in the MMCCC circuit by virtue of the new switching scheme. As there are only two switching states, the minimum time period is $2 \cdot Ts/5$ considering the same charging/discharging period is required. In this case, the maximum switching frequency can be made to $1/(2 \cdot Ts/5)$ or $2.5f_s$. This advantageous feature has been illustrated in Figure 3-3 and Figure 5-4.

7.7 Improved Voltage Regulation and Higher Component Utilization

The closest match for the MMCCC's switching operation and capacitor charge balancing is the conventional FCMDC converter [7]. This is why the voltage regulation and on-state loss of the MOSFETs used in the MMCCC circuit are well suited to compare with the FCMDC circuit's behavior. The MMCCC offers a better voltage regulation compared to the conventional FCMDC converter. In up-conversion mode, the

FCMDC's input current flows though (N-1) series-connected transistors and one diode [7], where N is the conversion ratio. The situation becomes worse when the conventional converter attempts to deliver current from the high voltage side to the low voltage side. During this time, the current flows through (N-1) diodes and only one transistor. Usually the voltage drop across the diode is greater than the voltage drop across any transistor and thereby the regulation is limited when the conversion ratio is high. On the other hand, the current flows through at most 3 transistors or diodes in the new converter irrespective of the conversion ratio. The reduced number of series-connected devices in the new converter is responsible for less voltage drop and better voltage regulation. This feature is observed in Figure 5-1 and Figure 5-3. Moreover, the converter uses only two switching states, which simplifies the design of the gate drive circuit.

The MMCCC circuit also offers high component utilization compared to its close contender the FCMDC circuit. For a hypothetical 100 V/20 V and 1000 W design, all the transistors in an FCMDC circuit should be rated at 20 V and 50 A considering a startup circuit is used to initially charge all the capacitors so that the transistors experience minimum off-state voltage. This is a 5-level design and the number of transistors would be 10. Among these 10 transistors, 5 are on for 80% time of one cycle, and the remaining 5 are on during only 20% time of one full cycle. Thus, the total volt-ampere rating of the transistors is (10·20·50) = 10 kVA, and the average would be 5 kVA. On the other hand, for MMCCC circuit, the total current flows through 3 parallel paths during half of the time period and flows through 2 parallel paths during the other half period. Thus, the average number of paths is 2.5 and each path contributes 50/2.5 = 20A. For a 5-level

converter, an MMCCC circuit requires 13 transistors and among them, 3 will experience $2V_{LV}$ during off state (this is one of the limitations of the MMCCC circuit). Thus, the total VA rating of the transistors would be (10·20·20) + (3·20·40) = 6.4 kVA, and the average would be 3.2 kVA. This comparison clearly shows that there will be a saving of 36% in the component rating if MMCCC is used over the FCMDC circuit. Moreover, the average current through any transistors in MMCCC circuit would be only 10 A compared to a current of 40 A for 5 bottom transistors and 10 A for the top 5 transistors in FCMDC circuit (see Figure 3-2). Thus, smaller size transistors can be used throughout the MMCCC circuit, thus expected to save a great amount of manufacturing cost.

7.8 CHAPTER SUMMARY

Several key features of the MMCCC topology have been discussed in this chapter and they were validated using experimental results. In Chapter 1, the importance of designing a high efficiency dc-dc converter with bi-directional power management system was emphasized. In future hybrid or fuel cell automobiles, the efficiency and performance of the dc-dc converter will be an important factor to dictate the overall performance of the automobile. The MMCCC topology not only meets the present needs, but also acquires several novel features such as multiple load-source integration, and fault bypass capability, and these features are not available from any existing dc-dc converter circuits. Incorporating these features into the MMCCC topology, the entire converter can be considered as a dc transformer having multiple taps to integrate multiple sources and loads. Thus, this MMCCC topology can be considered as an advanced solution in future hybrid or fuel cell power train system exhibiting power management capability.

CHAPTER 8

CONCLUSIONS AND FUTURE WORK

8.1 CONCLUSIONS

The concept of modularity in power electronic circuits was the main focus in this dissertation. The dissertation has presented many forms of modular structure in the circuit designs of dc-dc converters and inverters. In Chapter 2, the existing modular structures in power electronic circuits were presented and a new methodology of analyzing dc-dc converters and inverters was introduced in Chapter 4. The concept of the basic switching cells using P-cell and N-cell explores a new modeling technique that can simplify the existing dc-dc converter circuits and can lead to find new circuit topologies. Chapter 3 concludes the design work by introducing the new Cuk converter and one current source inverter using these basic switching cells.

The circuit analyzing technique using modules was the major driving force to create a modular dc-dc converter that becomes the foundation of the drive train of the future fuel cell or hybrid electric vehicles. The necessity of a bi-directional dc-dc converter with very high efficiency was discussed in Chapter 1, and the quest for a suitable bi-directional dc-dc converter started at that point. In Chapter 3, several topologies of dc-dc converter was analyzed to find an optimum solution for the desired power train application; however, none of them was suitable to meet the future automotive needs. The search was limited to the capacitor clamped topologies because of

their inductor-free construction and high efficiency operation during partial loads.

From the various converters discussed in Chapter 3, a platform was created where it was attempted to obtain a combination of several converters. The common platform consists of series parallel converter, flying capacitor multilevel converter and other bi-directional dc-dc converters. The first part was simple, and it involved the step to find a unifying approach among the various topologies and to compare them. However, the second part was the actual challenge to extract the desirable topologies from individual converters. In this process, the simple two phase operation and three transistor cell structure were adopted from the series-parallel converter. In addition, to equalize the voltages across the switching devices, the interconnection technique of capacitors in the flying capacitor converter was used. After this integration step, a new topology of multilevel modular capacitor clamped topology was obtained which was named as MMCCC.

Chapter 5 was dedicated to the introduction of the MMCCC topology and the construction of the circuit. The concept of the MMCCC topology was verified though several simulations, and it was shown how the MMCCC topology could achieve improved performances over the flying capacitor converter (FCMDC). In those simulation results, the converter's up-conversion, down-conversion and battery charging operation were analyzed and compared with FCMDC topology. For a verification of the MMCCC concept, several analytical derivations were performed that modeled the startup (dynamic) and loading characteristics (steady state) of a MMCCC converter. In the startup analysis, it was shown how the MMCCC topology can generate the rated voltages

at the various nodes of the converter. However, these voltages were derived without considering any load connected to the converter, and it was verified how the converter would attain the desired conversion ratio.

The second part of the analytical derivation in Chapter 6 explained the steady state characteristics of the converter when a load is connected to the converter at the LV node. Because of the load current, the capacitor voltages will shift from the no-load values, and there will be voltage ripple at different nodes of the converter. In is obvious that the amount of ripple will depend on the load current, and the steady state analysis showed the steady state values at different nodes as a function of load current and capacitor values. The analysis also proved the stability of the operation of the MMCCC and explained how the converter had a steady average voltage over one period of cycle. The analytical expression was done for a 4 and 5-level configuration, and the method was eventually correct for any conversion ratio.

Once the MMCCC topology was verified through simulations and analytical computations, a 6-level prototype was constructed and tested. The experimental setup and the key features of the 6-level converter have been summarized in Chapter 7. The prototype was designed for a maximum 500 W power delivery, and several key attributes such as bi-directional power management, multiple load-source integration, and fault bypass capability were tested and the test results were summarized in Chapter 7 also. Thus, Chapter 7 was last part of the verification of the topology that was initiated in Chapter 5. Then to test the converter for higher power application, a 5-kW 5-level converter was built, and a microcontroller based circuit was used to generate appropriate

control signals for the converter. The 5-kW converter was tested for down-conversion mode, and the fault bypass mode was tested by creating some mimic faults inside the converter controller board. Thus, the all the attributes of the MMCCC topology were verified through experiments.

Two prototypes of the MMCCC circuit (500 W and 5 kW) were tested to implement various features of them. The bi-directional power management capability and the multiple load/source integration features were tested using the 500 W MMCCC circuit. Later on, the 5 kW prototype was built and tested to generate ac outputs along with regular dc outputs simultaneously. In this way, the inherent power management capability of the MMCCC involving various kinds of sources and loads war demonstrated and verified.

8.2 FUTURE WORKS

During the analytical derivation, several assumptions were made in order to obtain a simple closed form of the solution of the startup and steady state operation of the converter. Those assumptions were zero ESR of capacitors and zero $R_{DS(ON)}$ of MOSFETs. It was also assumed that during startup, the load was not connected to the converter. It would be more representative if the first two factors ($R_{DS(ON)}$ and ESR) can be included in the derivation, leading to a more accurate model. In addition, these assumptions will create some level of complexity in the analysis, and at this moment it is considered as a future work.

As stated in Chapter 5, the MMCCC topology has several features similar to the FCMDC converter. In the FCMDC topology, unequal values of capacitors were used to

ensure equal voltage stresses across the switching devices [27]. However, capacitors having the same capacitance were used in each module to make each module identical and compatible to each other. Although these two circuits use different orientations of capacitors, the capacitors experience similar voltage stresses across them. Moreover, several simulations of the MMCCC circuit were done using unequal values of capacitors following the FCMDC topology, and the circuit still functioned well. Those results were not included in this thesis because the final MMCCC converter was built using capacitors having the same capacitance in each module. Although those simulations are not considered as official, an important result was found that can lead to a future work in improving the MMCCC topology. It was found that the converter also works with capacitors having unequal capacitance, although the various node voltages were slightly different from the original MMCCC circuit's node voltages. As a result, an analysis can be made on the variation of node voltages as a function of capacitances of the various capacitors used in the circuit. This analysis will show how sensitive the conversion ratio is to the capacitor values.

While the MMCCC design exhibits redundancy and fault bypass ability of the circuit, the fault occurrences were assumed to be present in the circuit. It implies that the control circuit was not designed to detect any fault inside a module, rather it worked with some fault signal created by the user of the converter. It was assumed that when a fault occurs inside the circuit, a fault signal will be available corresponding to the location of the fault. Thus, a future work would be to provide the ability to detect the short circuit and open circuit faults inside any module, and a detection circuit needs to be designed.

Many algorithms are available to detect different kinds of faults in the system. However, a suitable and cost effective algorithm needs to be adopted to provide for the completeness of the fault bypass operation of the circuit.

An additional feature that could be added to the present design is to design an automated current control scheme for a wide range of conversion ratios. In the present design, the control circuit works in an open loop mode, and by changing the duty ratio of the two phase signal (Red and Blue), load current can be controlled. However, there is no current sensor installed in the circuit, and the circuit cannot make an automatic change in the duty ratio when a specific amount of current is required to flow in the circuit. The automated current control scheme would be useful during bi-directional power management. When the conversion ratio of the circuit is reduced by one, and if the circuit works in down conversion mode, the duty ratio of the Red/Blue signals must be reduced to control the current. Using a current sensor at the low voltage side, a low pass filter could generate a dc voltage which would be proportional to the current. Then using a voltage comparator, a current threshold can be fixed, and the microcontroller could generate variable duty ratio to control the current. All the enhancement features mentioned above would make the MMCCC design even more flexible in providing one-step design to meet the requirements in various applications.

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APPENDIX

APPENDIX A

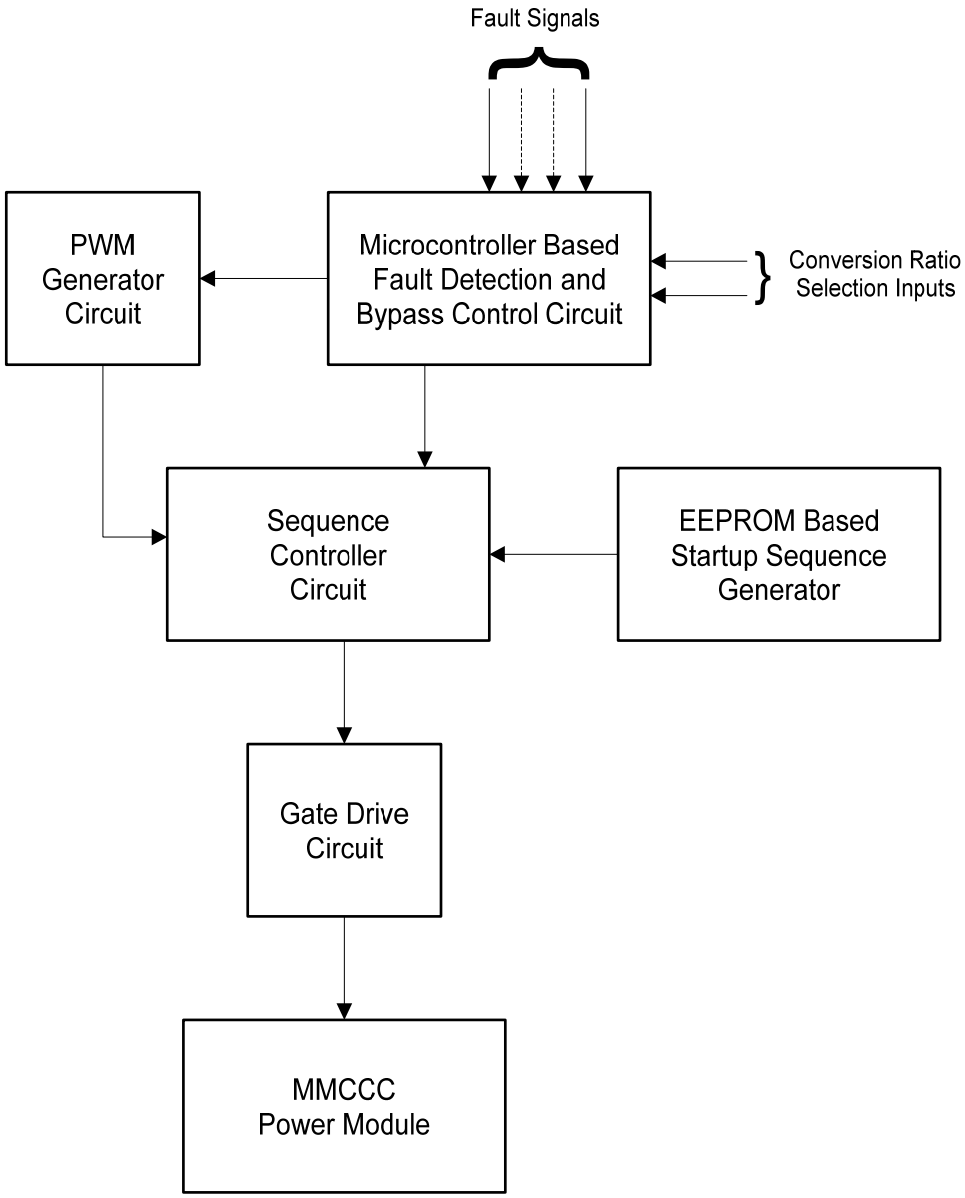

Figure A-1. The block diagram of the MMCCC control circuit.

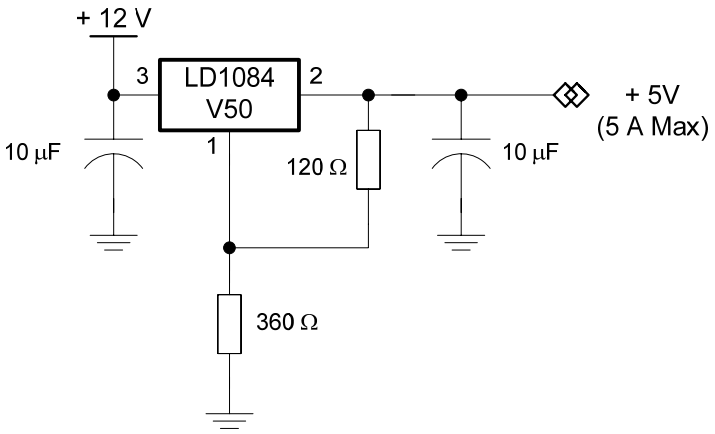

Figure A-2. The 5 V regulator circuit.

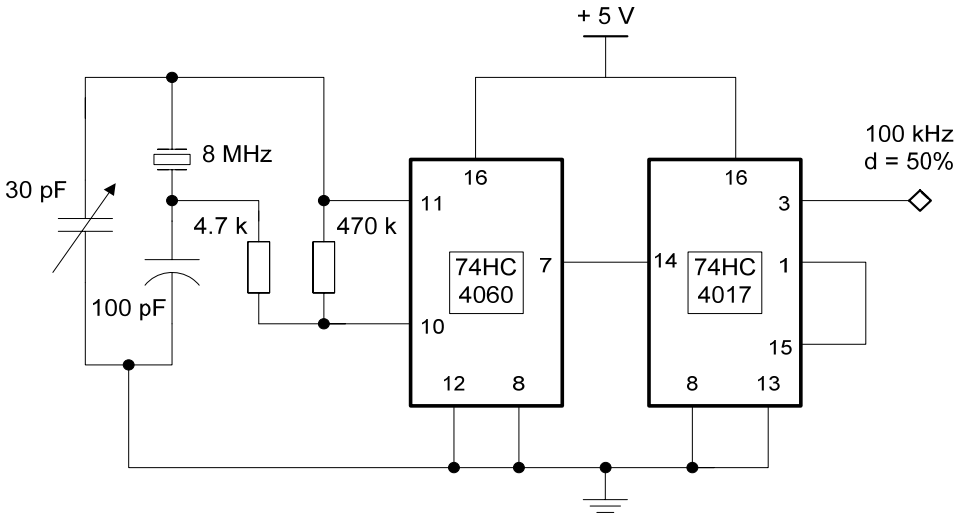

Figure A-3. 100 kHz clock generator circuit.

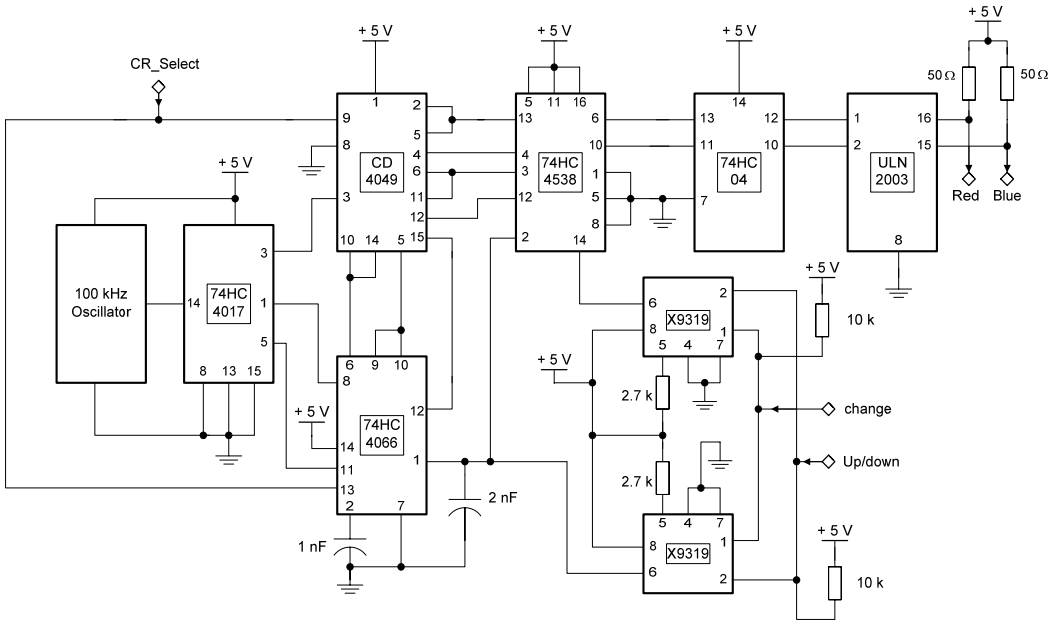

Figure A-4. PWM generator circuit for MMCCC power module. The circuit produces two phase outputs ‘Red’ and ‘Blue’ with variable duty ratio.

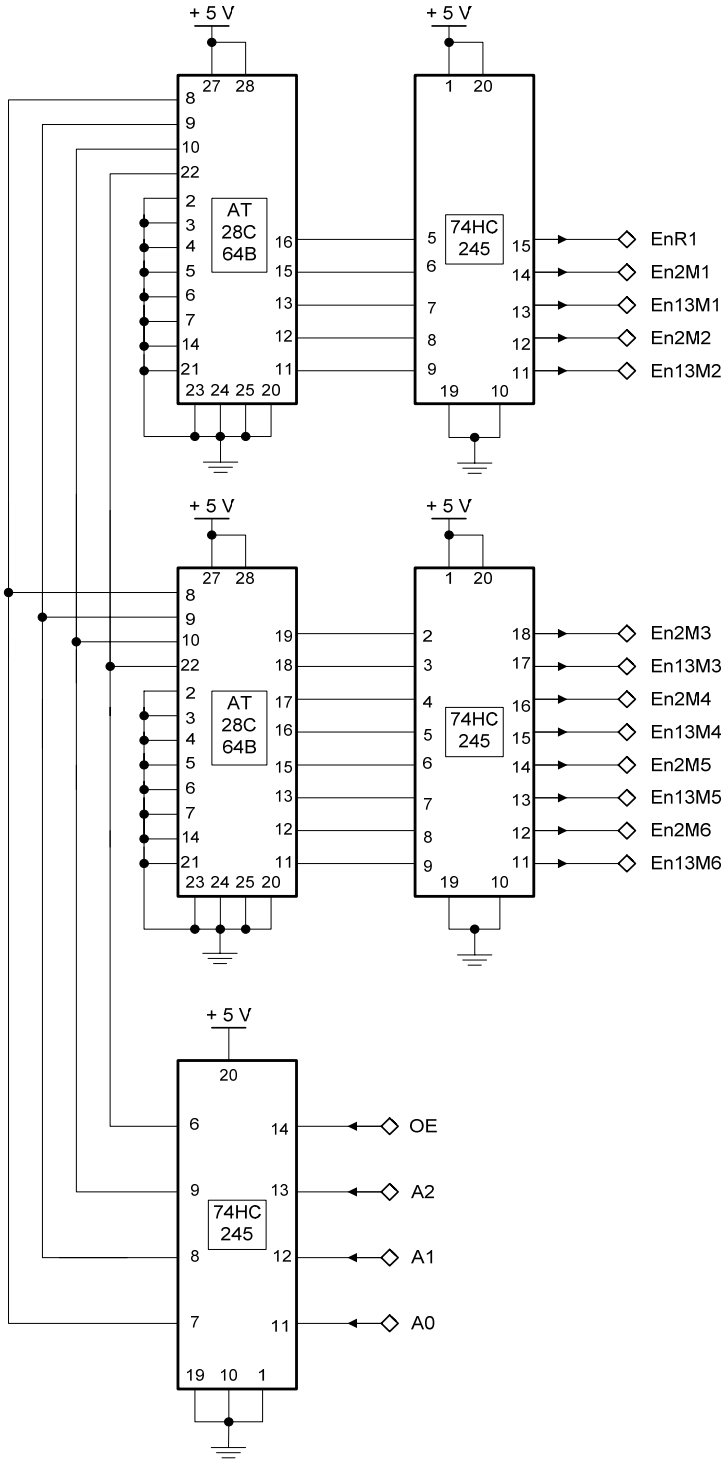

Figure A-5. The EEPROM based sequence generator circuit for the startup step.

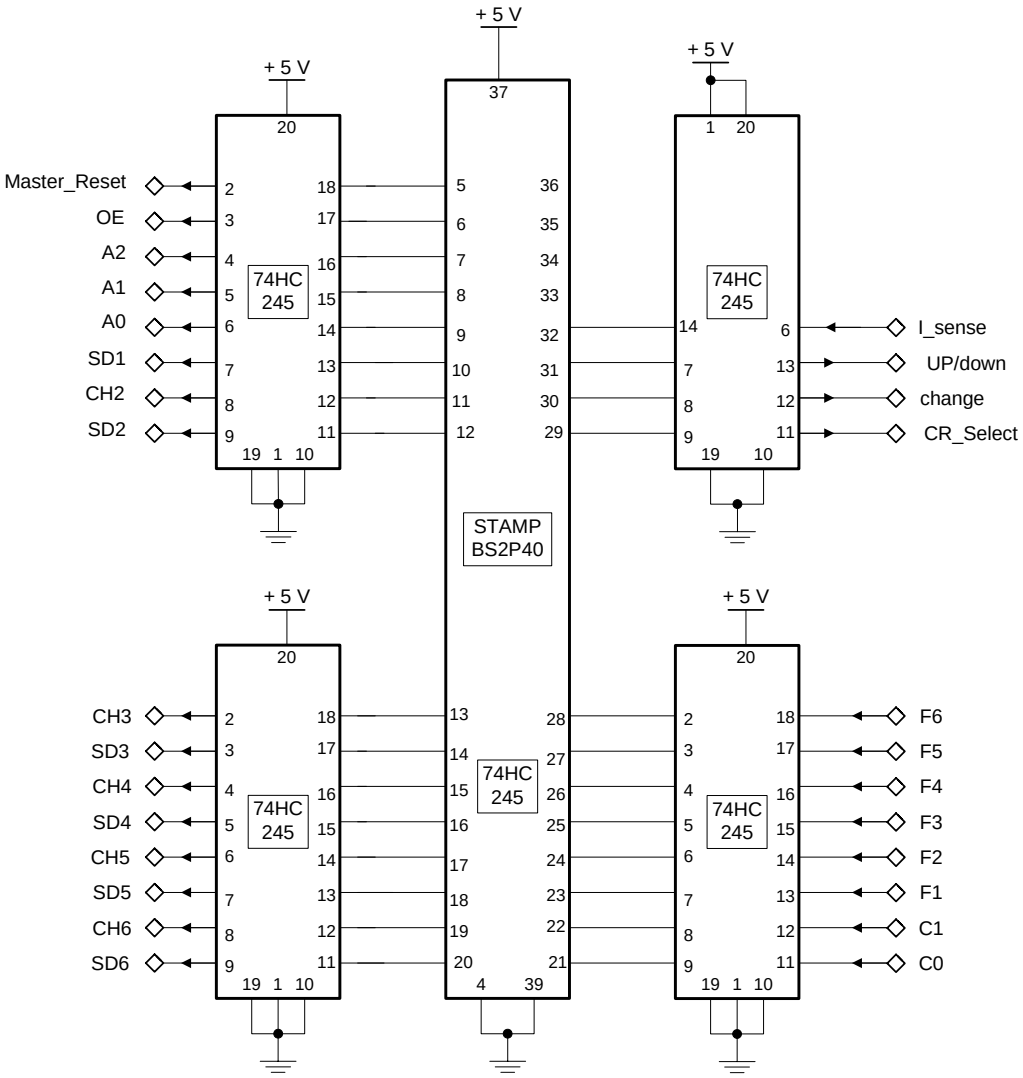

Figure A-6. Microcontroller interface circuit.

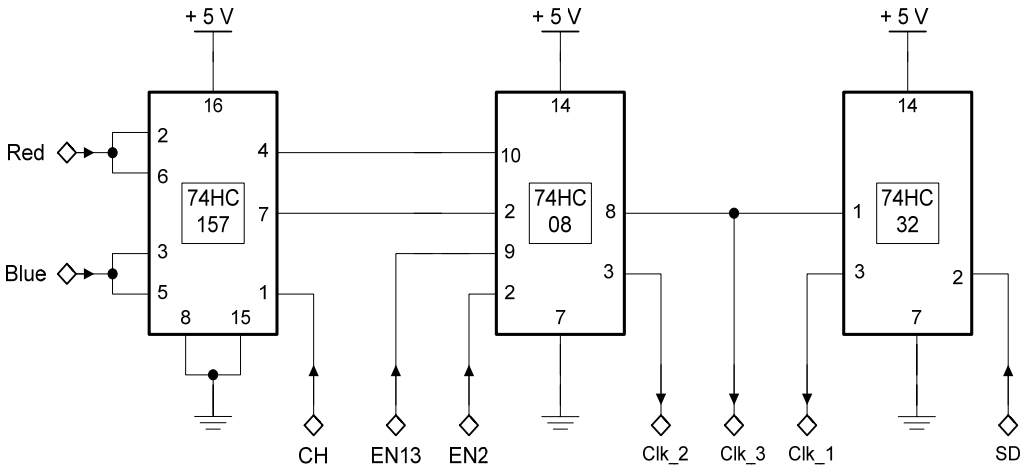

Figure A-7. The sequence controller circuit.

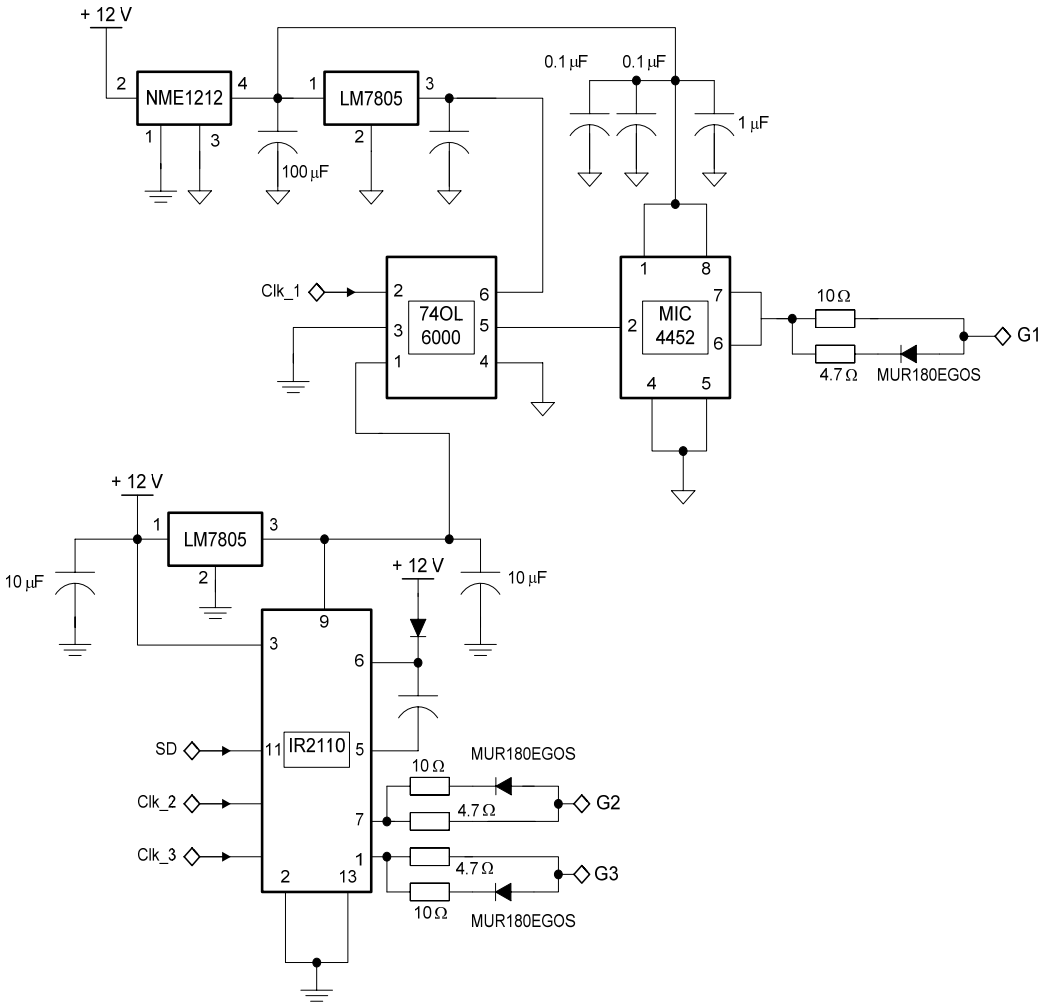

Figure A-8. The gate drive circuit for the MMCCC power module.

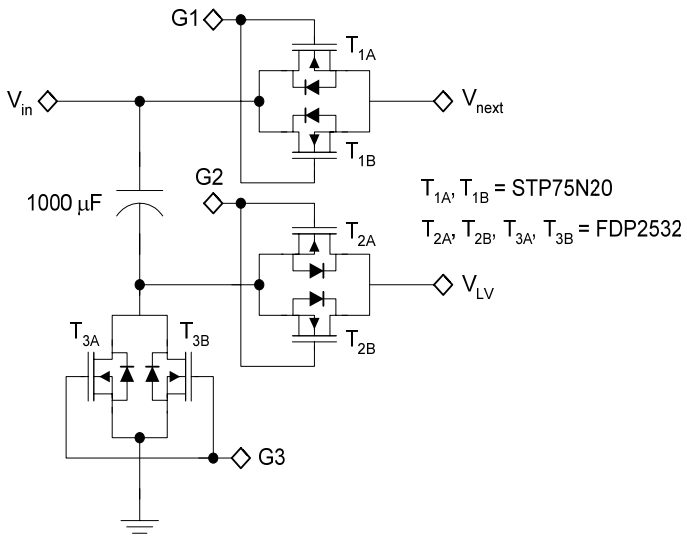

Figure A-9. The schematic of one of the power modules of the 5-kW MMCCC prototype.

APPENDIX B

THE PBASIC PROGRAM FOR THE PARALLAX STAMP BS2P40 MICROCONTROLLER

```
**************************************************************************

' {$STAMP BS2p}
' {$PBASIC 2.5}
MAINIO
'Activating the Master Reset
HIGH 0
PAUSE 1
LOW 0
'****************************************
'Generating Preliminary CH and SD signals
LOW 5 'SD1
LOW 6 'CH2
LOW 7 'SD2
HIGH 8 'CH3
LOW 9 'SD3
LOW 10 'CH4
LOW 11 'SD4
HIGH 12 'CH5
LOW 13 'SD5
LOW 14 'CH6
LOW 15 'SD6
'****************************************
'Defining output variables
OE_bar VAR Bit    'Main 1  out1
AD2 VAR Bit       'Main 2  out2
AD1 VAR Bit       'Main 3  out3
AD0 VAR Bit       'Main 4  out4
'****************************************
'Doing 100 iterations with the EEPROM
add_count VAR Nib
Iter_no VAR Word
FOR iter_no=1 TO 100
   FOR add_count=0 TO 3
     IF add_count = 0 THEN
        LOW 2
        LOW 3
        LOW 4
```

```
        HIGH  1
        PAUSE 1
        LOW 1
        PAUSE 1
      ENDIF
      IF add_count = 1 THEN
        LOW 2
        LOW 3
        HIGH 4
        HIGH  1
        PAUSE 1
        LOW 1
        PAUSE 1
      ENDIF
      IF add_count = 2 THEN
        LOW 2
        HIGH 3
        LOW 4
        HIGH  1
        PAUSE 1
        LOW 1
        PAUSE 1
      ENDIF
      IF add_count = 3 THEN
        LOW 2
        HIGH 3
        HIGH 4
        HIGH  1
        PAUSE 1
        LOW 1
        PAUSE 1

      ENDIF
    NEXT
NEXT
'*********************************************
'Starting the loop
Mainloop:
AUXIO
'Defining the variables
C0 VAR Bit     'Aux 0
C1 VAR Bit     'Aux 1
'CR is the conversion ratio variable
C_R VAR Nib         'Depends on C0 and C1
```

```
I_sense VAR Bit      'Aux 11
C_F_odd_even VAR Bit     ' if C_R is 4 or 6, then C_F_odd_even = 0, else 1      Aux 8
up_down VAR Bit          '1 is up, 0 is down  Aux 10
change_value VAR Bit ' Aux 9, change at 0
'Defining the fault input variables
F6 VAR Bit
F5 VAR Bit
F4 VAR Bit
F3 VAR Bit
F2 VAR Bit
F1 VAR Bit
No_of_F VAR Nib
'Reading the conversion ratio commands
INPUT 0
C0 =IN0
INPUT 1
C1=IN1
'**************************************
'Changing red/blue duty ratio
C_R = 4 + (C0 + (2*C1))
DEBUG ? C_R
IF C_R = 4 THEN
LOW 8
ENDIF
IF C_R =5 THEN
HIGH 8
ENDIF
IF C_R=6 THEN
LOW 8
ENDIF
'**************************************
'Reading the fault commands
INPUT 2
F1=IN2
INPUT 3
F2=IN3
INPUT 4
F3=IN4
INPUT 5
F4=IN5
INPUT 6
F5=IN6
INPUT 7
F6=IN7
```

```
'************************************
No_of_F = F1+F2+F3+F4+F5+F6
IF No_of_F>1 THEN
'STOP
GOTO Mainloop 'show some error signal, make the eeprom address 000.
ENDIF
'************************************
'Detecting current feedback
INPUT 11
I_sense=IN11
SD1 VAR Bit
Ch2 VAR Bit
SD2 VAR Bit
Ch3 VAR Bit
SD3 VAR Bit
Ch4 VAR Bit
SD4 VAR Bit
Ch5 VAR Bit
SD5 VAR Bit
Ch6 VAR Bit
SD6 VAR Bit
MAINIO
'Defining output variables
OUTPUT 0  'Master_reset
OUTPUT 1  'OE_bar
OUTPUT 2  'A2
OUTPUT 3  'A1
OUTPUT 4  'A0
OUTPUT 5  'SD1
OUTPUT 6  'Ch2
OUTPUT 7  'SD2
OUTPUT 8  'Ch3
OUTPUT 9  'SD3
OUTPUT 10 'Ch4
OUTPUT 11 'SD4
OUTPUT 12 'Ch5
OUTPUT 13 'SD5
OUTPUT 14 'Ch6
OUTPUT 15 'SD6
'Start Computation
'************************************************************
'Defining conditions for SD signals
IF F1=1 THEN
SD1 = 1
```

```
ELSE
SD1 = 0
ENDIF
IF F2=1 THEN
SD2 = 1
ELSE
SD2= 0
ENDIF
IF F3=1 THEN
SD3 = 1
ELSE
SD3 = 0
ENDIF
IF ((F4=1)OR ((C_R = 4) AND ((F1 OR F2 OR F3)=0))) THEN
SD4 = 1
ELSE
SD4 =0
ENDIF
IF ((F5=1) OR (C_R=4) OR ((C_R = 5) AND ((F1 OR F2 OR F3 OR F4)=0)))THEN
SD5 = 1
ELSE
SD5 =0
ENDIF
IF ((F6=1)OR (C_R=4) OR (C_R=5) OR ((C_R = 6) AND ((F1 OR F2 OR F3 OR F4
OR F5)=0)))THEN
SD6 = 1
ELSE
SD6 =0
ENDIF
'Defining conditions for CH signals
IF (SD1=1) THEN
CH2 =1  'default is zero
ELSE
CH2 =0
ENDIF
IF ((SD1 OR SD2)=1)  THEN
CH3 = 0   'default is one.
ELSE
CH3 = 1
ENDIF
IF ((SD1 OR SD2 OR SD3)=1)  THEN
CH4 = 1   'default is zero.
ELSE
CH4 = 0
```

```
ENDIF
IF (((C_R > 4)AND ((SD1 OR SD2 OR SD3 OR SD4)=1)) OR ((C_R = 4)AND ((SD1
OR SD2 OR SD3)=1))) THEN
CH5 = 0   'default is one.
ELSE
CH5 = 1
ENDIF
IF ((C_R = 4)AND ((SD1 OR SD2 OR SD3)=1)) THEN
CH6 = 1   'default is zero.
ELSE
CH6 = 0
ENDIF
IF ((C_R=5)AND ((SD1 OR SD2 OR SD3 OR SD4)=1)) THEN
CH6 = 1   'default is zero.
ELSE
CH6 = 0
ENDIF
IF ((C_R=6)AND ((SD1 OR SD2 OR SD3 OR SD4 OR SD5)=1)) THEN
CH6 = 1   'default is zero.
ELSE
CH6 = 0
ENDIF

'Generating output signals
'*********************************************************
OUT5 = SD1
OUT6 = CH2
OUT7 = SD2
OUT8 = CH3
OUT9 = SD3
OUT10 = CH4
OUT11 = SD4
OUT12 = CH5
OUT13 = SD5
OUT14 = CH6
OUT15 = SD6
'*********************************************************
'Enabling all modules
HIGH 2
LOW 3
LOW 4
HIGH 1
PAUSE 1
LOW 1
```

```
'*****************************************************
AUXIO
'Checking the current
IF I_sense = 0 THEN
   HIGH 10  'make the change to high
 ELSE
   LOW 10
ENDIF
 LOW 9     'make count change in digital potentiometer
 PAUSE 1
 HIGH 9
 DEBUG ? C0
 DEBUG ? C1
 DEBUG ? C0
 DEBUG ? C1
 DEBUG ? F1
 DEBUG ? F2
 DEBUG ? F3
 DEBUG ? F4
 DEBUG ? F5
 DEBUG ? F6
 DEBUG ? SD1
 DEBUG ? SD2
 DEBUG ? SD3
 DEBUG ? SD4
 DEBUG ? SD5
 DEBUG ? SD6
 DEBUG ? CH2
 DEBUG ? CH3
 DEBUG ? CH4
 DEBUG ? CH5
 DEBUG ? CH6
GOTO Mainloop

*****************************************************************
```

VITA

Faisal Khan was born in Dhaka, Bangladesh on November 28, 1974. He completed his B.S in Electrical Engineering from Bangladesh University of Engineering and Technology (BUET) in August 1999. In January 2001, Faisal enrolled in the M.S program in solid state electronics in Arizona State University. In August 2003, Faisal started the PhD program in The University of Tennessee majoring in power electronics.

Faisal's research interest includes dc-dc converters, multilevel inverters, power supply efficiency issues, and power management in hybrid electric automobile power system. He is presently pursing his doctorate in power electronics.