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A Digital-to-Analog Converter Architecture for Multi-Channel Applications

Mark D. Hale
University of Tennessee - Knoxville

To the Graduate Council:

I am submitting herewith a dissertation written by Mark D. Hale entitled "A Digital-to-Analog Converter Architecture for Multi-Channel Applications." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

Benjamin J. Blalock, Major Professor

We have read this dissertation and recommend its acceptance:

Charles L. Britton, M. Nance Ericson, Vasilios Alexiades, Ethan Farquhar, Syed K. Islam

Accepted for the Council:
Dixie L. Thompson

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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A Digital-to-Analog Converter Architecture for Multi-Channel Applications

A Dissertation

Presented for the

Doctor of Philosophy

Degree

The University of Tennessee, Knoxville

Mark David Hale
May 2008

Dedication

To my parents

Jerry Brady Hale and Nancy Walker Hale

Acknowledgments

First and foremost I would like to thank my advisor, Professor Benjamin Blalock, for supporting this research and for providing guidance. It has been a privilege to work in his laboratory. I have also enjoyed our numerous mountain biking rides together. I wish him success in converting many of his current and future students to becoming mountain bikers.

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I would also like to thank my family for their continuous support and encouragement.

Abstract

Systems-on-chip with the capability of driving multiple analog voltages are useful for a variety of applications, including multiple actuator control for robotics applications, automated test equipment systems, industrial automation, programmable logic controllers, and satellite flywheel motor control. Such applications require a DAC for each analog output. A multi-channel architecture that saves power and area by sharing hardware is needed.

This work introduces a new single-ramp multi-channel 12-bit DAC architecture. The architecture includes a low power Gray code counter, ramp generator, digital comparator, analog memory units, and control logic.

The new multi-channel DAC architecture allows hardware sharing between multiple channels, and enables Systems-on-Chip to have multiple analog outputs for stimulating transducers or motors. The DAC architecture is to be used in a variety of space and defense applications as part of the BAE Systems RAD6000 microcontroller project.

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Chapter 1

Introduction

1.1 Motivation

The topic of this dissertation is a multi-channel digital-to-analog converter (DAC) architecture. Part of the motivation for this work was to develop a DAC architecture for the BAE Systems RAD6000 microcontroller project. This microcontroller is intended for use in a wide variety of space and defense applications. One of the applications that the microcontroller is intended to be used for is satellite control. This application requires that the microcontroller interface with the satellite's flywheel motors to control the satellite's orientation. Three flywheels are needed to control the satellite orientation, so three DAC channels are needed to send analog control signals from the microcontroller. The DAC will be integrated on chip with the RAD6000 microcontroller for use in satellite control and other applications. The

architecture developed for the RAD6000 project, and presented in this dissertation, is a new single-ramp DAC architecture that is suitable for multi-channel applications.

Additional motivation for this work is to explore the design challenges and characteristics of this novel single-ramp DAC architecture. The usefulness of this architecture for multi-channel applications will be analyzed. Performance data on ramp-based DAC architectures is scarce in literature, and this work will present test results of such an architecture.

The basic single-ramp DAC architecture is useful for low power, low speed, and high linearity applications. The single-ramp DAC presented in this dissertation is a modified version of the basic single-ramp DAC architecture that allows the DAC to share hardware between multiple channels. This DAC architecture is analogous to the Wilkinson ADC architecture that has been discussed numerous times in literature. Both circuits use a digital counter and an analog ramp generator. In the single-ramp DAC architecture, the counter and ramp generator circuits have reversed roles from that in the ADC. In the Wilkinson ADC, the counter value is passed to the output when the analog ramp voltage equals the analog input. In the DAC, the analog ramp voltage is passed to the output when the digital counter value equals the digital input.

The DAC architecture developed in this work shares some attributes with the Wilkinson ADC. These attributes include low power and usefulness for multi-channel applications. The ramp generator in these converters often requires a large capacitor, and this circuit can take up a significant portion of the circuit's area. The Wilkinson ADC is useful for multi-channel applications because this architecture allows the ramp generator and counter to be shared between channels. Unfortunately, the basic

single-ramp DAC architecture does not allow the ramp generator to be shared between channels. The DAC architecture presented in this work uses an analog memory circuit that not only functions as a sample and hold, but also allows the ramp generator to be shared between channels.

1.2 Research Goals

The goals of this research are as follows:

- To investigate the strengths and weaknesses of the modified single-ramp DAC architecture
- To show the advantages of this architecture compared to other architectures for multiple channel applications
- To design, layout, and test a multiple channel DAC

To accomplish these goals, a multi-channel DAC has been designed in the AMI 0.5 μm process. This DAC architecture has been modified from the basic single-ramp DAC architecture to make the DAC suitable for multiple channel applications. The modifications allow the ramp generator circuit and other hardware to be shared between channels. This is a key contribution toward enabling low power multiple channel DACs. It includes a low power digital counter, a ramp generator with a high output impedance current source, a binary to Gray code converter, a digital comparator, and analog memory units with control signal logic. The DAC has 2 channels (for this demonstration), and fits in an area of approximately 1 mm^2.

1.3 Overview of the Dissertation

Chapter 2 will include a review of DAC architectures. There will be a discussion of several frequently used architectures along with a brief analysis of the advantages and disadvantages each architecture. The single-ramp DAC architecture, which is less frequently used, will also be discussed. Chapter 3 will discuss previously reported multi-channel DACs and the suitability of the single-ramp DAC architecture for multi-channel applications. Chapter 4 will discuss the novel multi-channel DAC architecture of this research. Design details and simulation results will be presented. A discussion of the major tools used in this research will also be presented in this chapter. Chapter 5 will include test results from the DAC and analysis. Chapter 6 will address the original contributions of this research and provide conclusions.

Chapter 2

Overview of DACs

2.1 Introduction

Digital-to-analog converters (DACs) are circuits that are used to convert a digital signal into an analog signal. The DACs discussed in this chapter convert binary digital signals into an analog voltage or current signal. This literature review will be limited to frequently used Nyquist-rate DAC architectures. Oversampling DACs, which sample data at frequencies much higher than the Nyquist frequency, will not be discussed. In addition to the more common DAC architectures, this chapter will discuss a less frequently used architecture that is relevant to this work.

2.2 Common DAC Architectures in Prior Art

The resistor string DAC consists of a resistive voltage divider between reference voltages [1–3]. The resistors in the voltage divider generate 2^N reference voltages for an N-bit DAC. These reference voltages are selected using switches controlled by the digital input to the DAC. The selected voltage is buffered so that the load that the DAC is driving does not affect the voltage division. This DAC is also known as the Kelvin divider. It was invented by Lord Kelvin in the 18th century [1]. A 3-bit resistor string DAC is shown below in Figure 2.1.

One advantage of this architecture is that it is inherently monotonic. The resistor string DAC is useful for high speed and lower resolution applications. Implementing a high resolution resistor string DAC can be very problematic due to the large number of resistors and switches required and the matching requirements of the resistors. For N-bit resolution, 2^N resistors are required [4]. To reduce the number of resistors and switches required, a segmented resistor-string DAC can be used [5, 6]. This architecture uses a resistor string DAC that is controlled by a number of MSB bits. The outputs of this MSB DAC are buffered and used as the references for a second LSB DAC. The buffers can introduce nonlinearity if they are not matched.

The R-2R ladder architecture consists of a resistor and switch network [7–9]. It is more useful than the resistor-string DAC for high linearity applications because the number of required resistors grows linearly with the number of bits (as opposed to exponentially for the resistor-string DAC architecture). This architecture is shown below in Figure 2.2. A MOSFET-only approach is described in [8]. This MOSFET-only approach can save area if large resistors are desired to reduce power consumption.

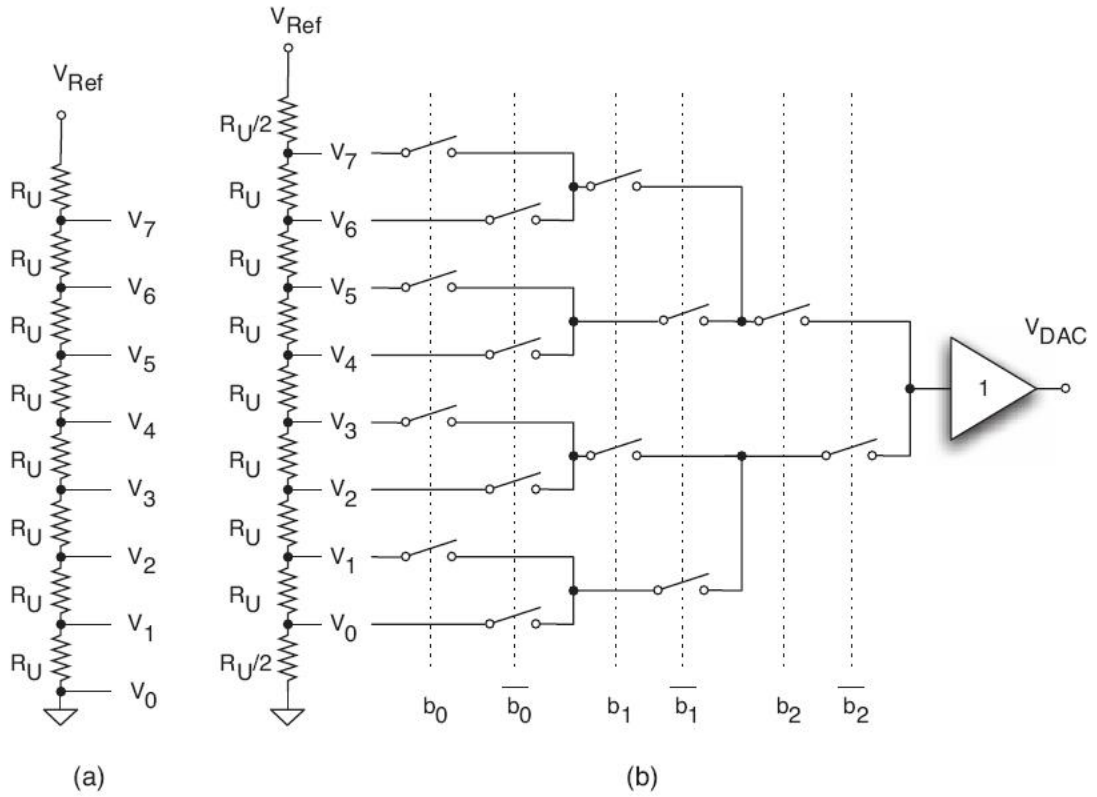

Figure 2.1: (a) A resistor string DAC (b) Resistor string DAC with 1/2 LSB offset [1]

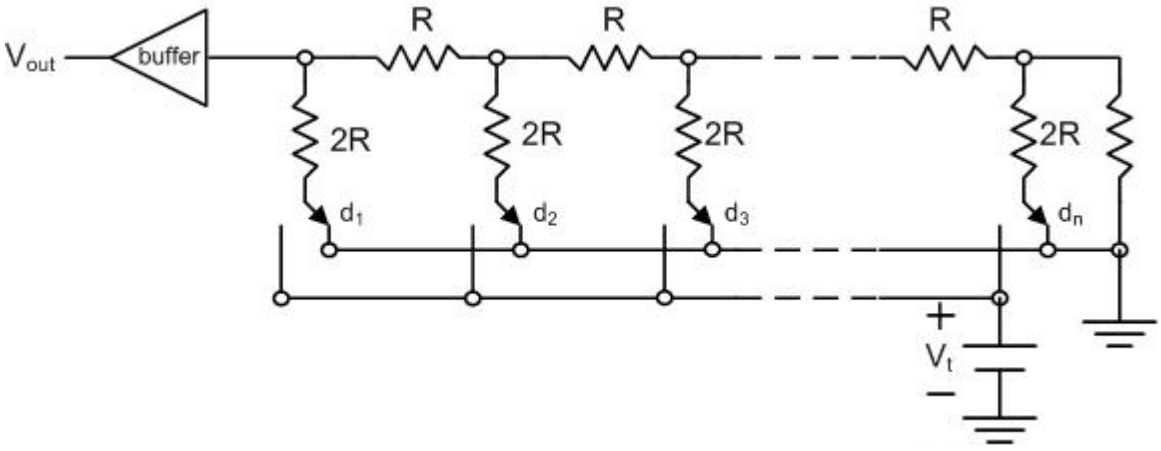

Figure 2.2: An n-bit R-2R DAC [8]

For both the resistor and MOSFET-only R-2R architecture, an output buffer is required to prevent the DAC's load from affecting the output voltage. One disadvantage of these architectures is that the resistive load of the reference voltage can vary. For example, if the MSB is high and all other bits are low for a 3-bit R-2R DAC, the resistance between the reference voltage and ground is 4R. The load of the reference voltage will change to about 3R if the LSB is high and the other bits low. For high resolution DACs, the reference circuit must be able to provide a very accurate reference while it's resistive load changes by more than 30 %.

The charge scaling flash DAC architecture performs a conversion by dividing the DAC's reference voltage using matched capacitors. This architecture can either use unary weighted capacitors or binary weighted capacitors. The unary architecture uses 2^N capacitors to implement an N-bit converter, but the binary weighted capacitor architecture can implement an N-bit converter using N capacitors [10]. The binary-weighted capacitor architecture can require large capacitors in high resolution DACs, because the capacitance spread increases exponentially with the number of bits. To reduce the capacitance spread in this architecture, an attenuator can be used [1]. The unary and binary weighted architectures are shown in Figure 2.3.

The charge scaling architecture can have nonlinearities introduced by capacitor mismatches [10–12]. These errors can be reduced by using common-centroid layout techniques. Voltage dependence of the capacitors and parasitic capacitance can also be a source of nonlinearity [10].

Another commonly used DAC architecture is the current steering DAC [1, 13, 14]. This architecture uses a set of current sources that can be unary or binary weighted.

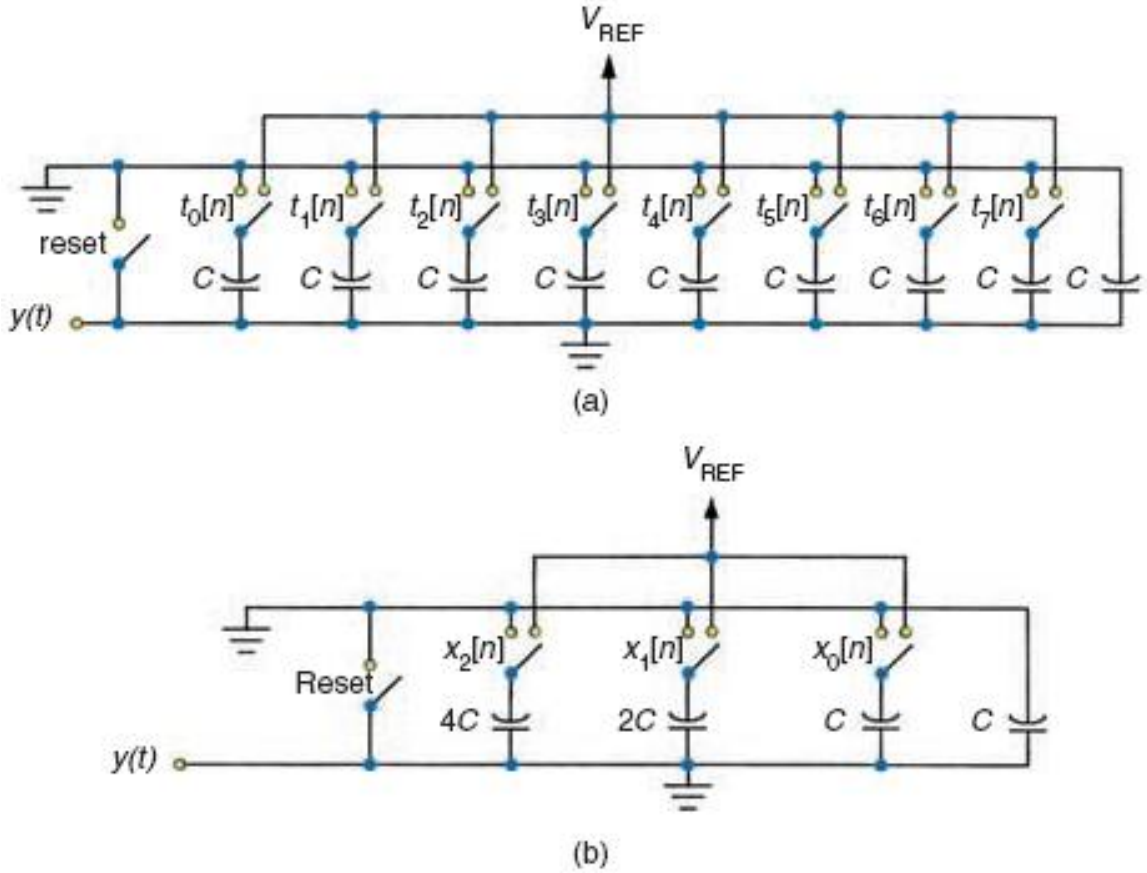

Figure 2.3: (a) Unary and (b) binary weighted 3-bit charge scaling flash DAC [10]

Switches are used to connect the currents and produce the DAC's output current. An N-bit DAC using unary weighted current sources requires 2^N current sources. An N-bit converter using binary weighted current sources requires only N current sources. The binary and unary weighted current steering DAC architectures are shown in Figure 2.4.

This architecture is useful for high speed applications. Unfortunately, the DAC's output can have glitches when the digital input changes. If the switches steering the current sources do not all change at the same time, a spike will occur at the DAC's output. Another disadvantage of this architecture is the stringent matching required of the current sources for high linearity DACs [13].

2.3 Ramp Based DACs

The single-ramp DAC architecture is much less frequently used than the architectures discussed above [1]. This architecture requires a counter, a digital comparator, a ramp generator, and a sample and hold amplifier. At the beginning of each conversion cycle, the ramp generator begins ramping synchronously with the start of the counter. The digital inputs should be latched and held constant until the conversion is complete. When the counter value reaches the digital input, the digital comparator stops the ramp generator and the ramp voltage is held constant. The sample and hold circuit refreshes the output with the ramp voltage at the end of each conversion cycle. The single-ramp architecture is shown in Figure 2.5.

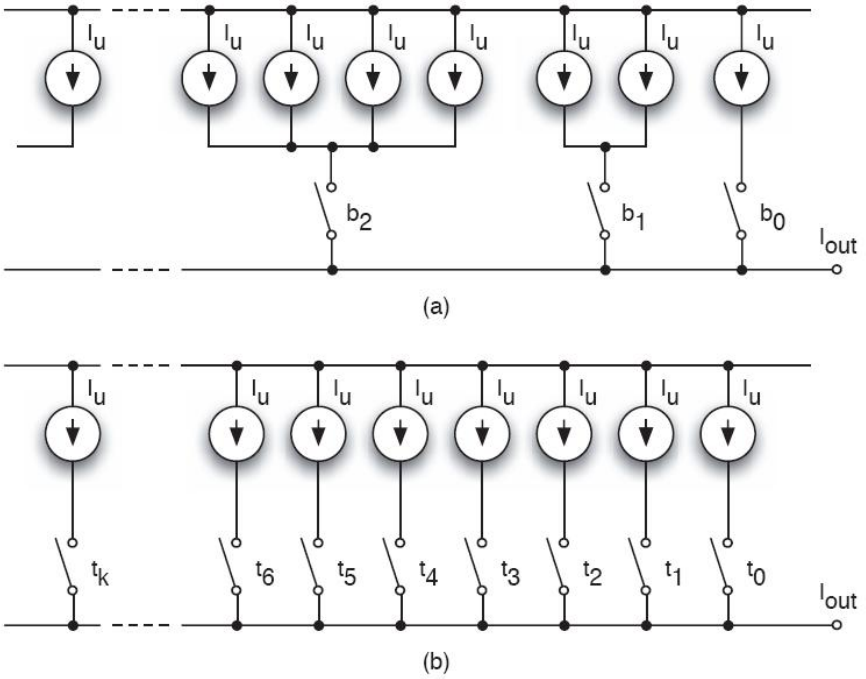

Figure 2.4: (a) Binary weighted and (b) unary weighted 3-bit current steering DAC [1]

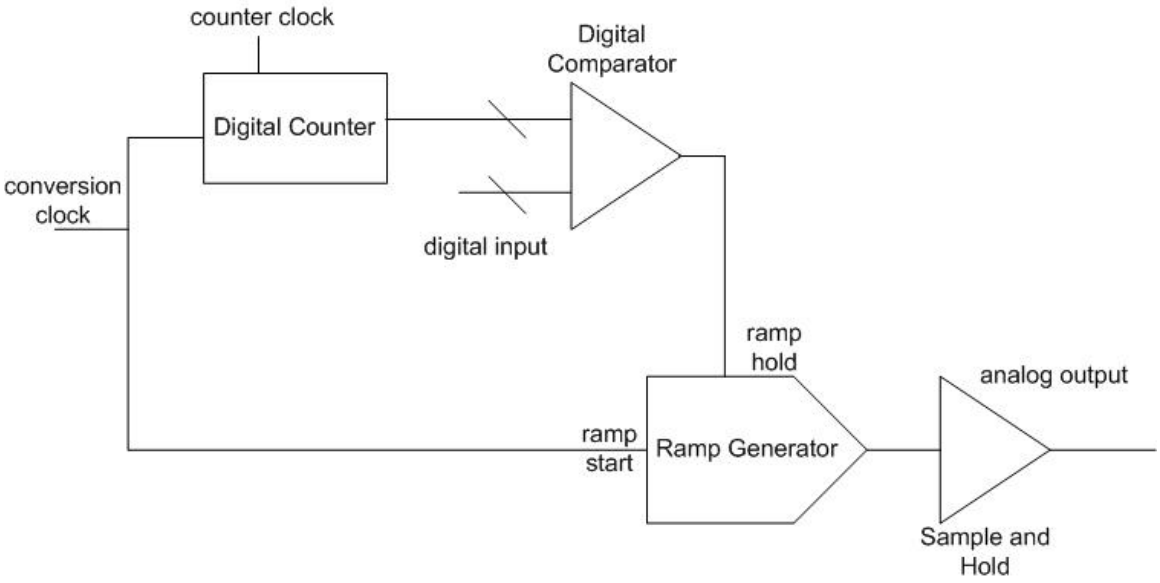

Figure 2.5: Single-ramp DAC architecture

This architecture is useful for low power, low speed, and high resolution applications. The ramp generator can be implemented with a current source and capacitor. The ramp can be highly linear if the current source has a high output impedance. For high resolution single-ramp DACs, a digital counter with a high number of bits is required. A disadvantage of this architecture is that the counter must operate at a frequency that is 2^N times higher than the conversion rate. Because of this, the counter is likely to limit the conversion rate of a high resolution single-ramp DAC.

The dual-ramp DAC is a ramp-based DAC architecture that can be used for DACs that need to operate at higher frequencies than the single-ramp DAC is capable of, such as 100 kSps for a DAC with 12 or more bits of resolution. A dual-ramp DAC was reported by W. Mack et al. [15]. This architecture consists of 2 single-ramp DACs running simultaneously. The digital inputs for one of the DACs are the MSB inputs to the overall DAC. The inputs for the 2nd DAC are the LSB inputs to the overall DAC. The architecture is shown below in Figure 2.6. During the reset phase before a conversion, all three switches (S1, S2, and S3) are closed. This sets the output voltage to VFS (full-scale voltage). At the beginning of a conversion, S2 opens. Switch S1 opens when the counter value equals the MSB inputs. Switch S2 opens when the counter value equals the LSB inputs. The currents I1 and I2 are scaled such that

$$I_2 = \frac{I_1}{2^{\frac{n}{2}}} \tag{2.1}$$

The resulting DAC output is the sum of the voltage produced by the integration of the coarse and fine DAC current sources. In order for this output voltage to be accurate, the architecture requires a precision current divider. For a 14-bit converter,

as shown in Figure 2.6, the scaling factor between the coarse and fine current sources is $2^{(14/2)}$, or 128. An error in the scaling factor between the currents will cause signal-dependent nonlinearity in the DAC. To achieve a precise current ratio for 14-bit linearity, the circuit requires trimming circuitry [15].

This architecture requires a lower clock frequency than a single-ramp DAC. The coarse and fine DACs need $2^{N/2}$ clock cycles per conversion for an N-bit dual-ramp DAC, but an N-bit single-ramp DAC requires 2^N. Because of the lower clock frequency needed, the dual-ramp architecture has a speed advantage over the single-ramp architecture. The suitability of this architecture for multi-channel applications will be discussed in chapter 3.

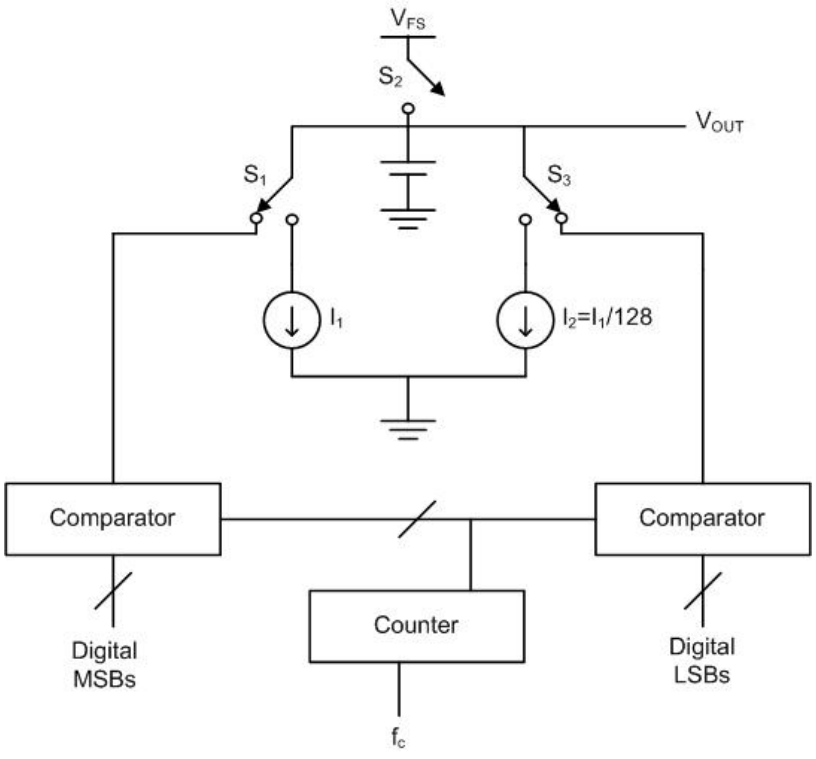

Figure 2.6: Dual-ramp DAC architecture [15]

Chapter 3

Multi-Channel DAC Applications and Prior Art

3.1 Applications for Multi-Channel DACs

Some applications require multiple digital signals to be converted to analog signals. Examples of these applications include:

- multiple actuator control for robotics applications [16]
- automated test equipment (ATE) systems
- industrial automation [17]
- programmable logic controllers
- satellite flywheel motor control

Meeting the parallel conversion requirement of these applications can be achieved using several DACs operating in parallel. A DAC architecture that shares hardware

between multiple channels is an alternative that can consume less area and power. Another alternative for these applications is to use a high speed DAC with a digital multiplexer on the input and an analog multiplexer on the output (with a sample and hold circuit on each channel). This option might be suitable for some applications, but the sampling rate of the DAC will need to increase linearly with the number of digital inputs. A multi-channel DAC does not require any increase in speed with the addition of extra channels. This chapter will discuss possible DAC architectures that may be suitable for use in a multi-channel application by sharing hardware between channels.

3.2 Previously Reported Multi-Channel DACs

There are very few multi-channel DACs reported in literature. Only three published multi-channel DAC architectures were found. This section discusses these three previously reported multi-channel DACs.

A 28-channel DAC for ATE systems was reported by Imamura and Kuwahara [18]. This DAC uses a 5.7-bit course and 3-bit fine resistor string DACs followed by a 4-bit binary weighted g_m output DAC. The authors refer to this architecture as a triple-rank DAC. The resistor string is shared between multiple channels. A diagram of the architecture is shown below in Figure 3.1. The 2^{nd} rank DAC shown in the figure is the binary weighted g_m output DAC. A schematic for this DAC is shown below in Figure 3.2.

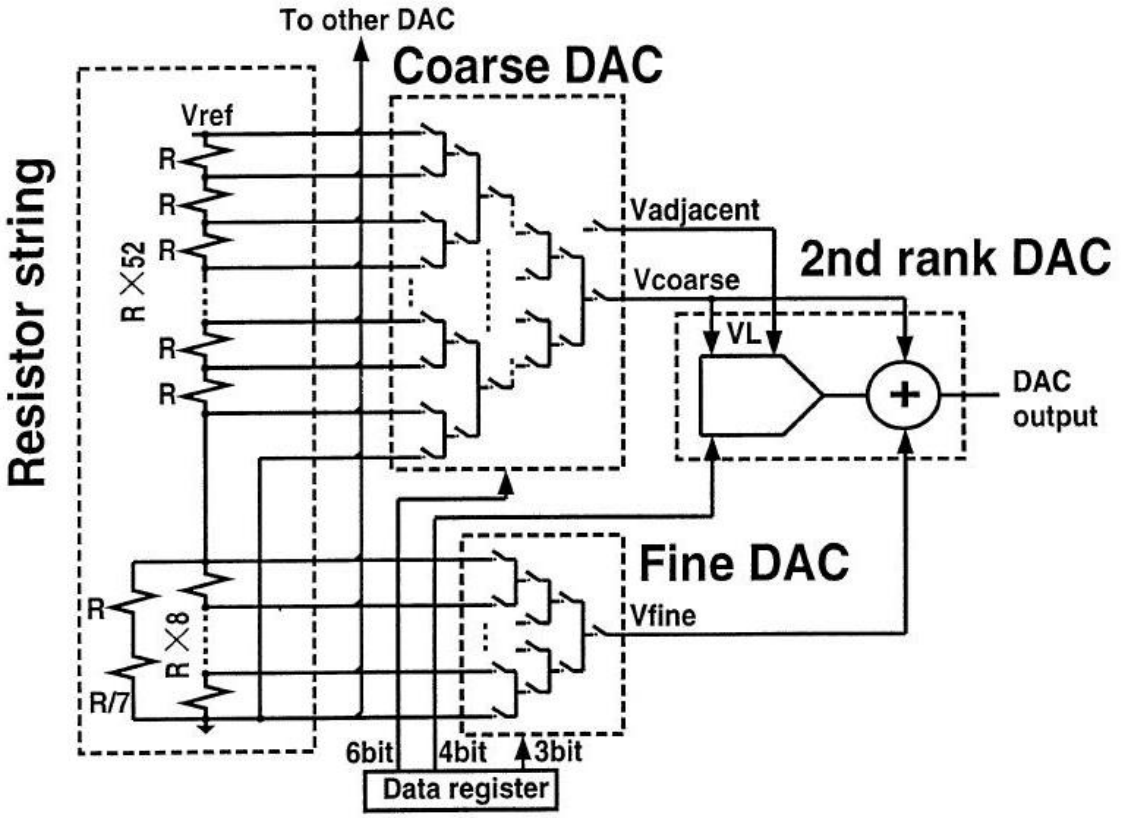

Figure 3.1: Triple-rank architecture for multi-channel DACs [18]

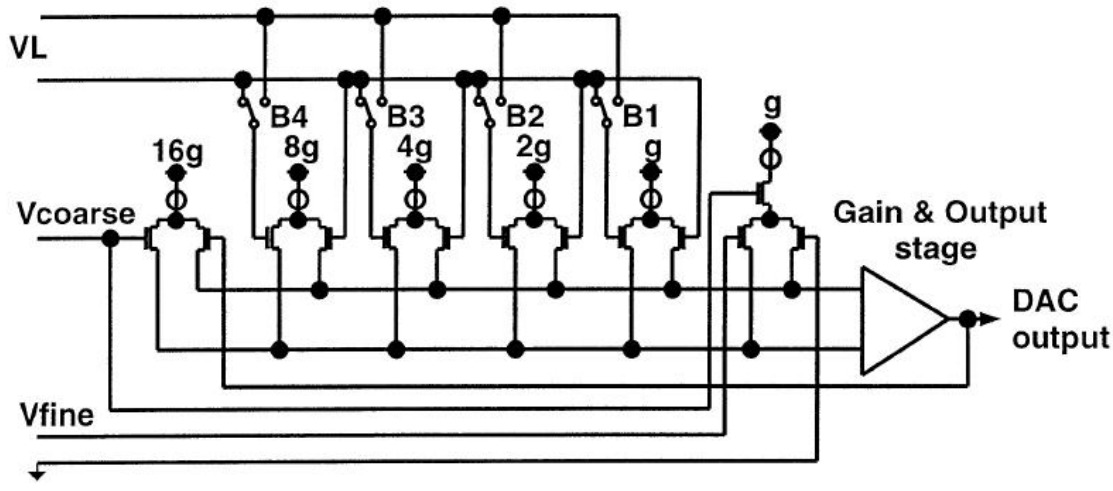

Figure 3.2: 2^{nd} rank binary weighted g_m output DAC [18]

The 2^{nd} rank DAC has six differential pairs with binary weighted g_m. The main differential pair acts as a voltage follower and buffers Vcoarse, which is the output of the course DAC. The other differential pairs add drain currents that are proportional to their input voltage and g_m. The differential input voltage to four of the smaller differential pairs is either VL or zero, depending on the 4-bit binary input to the 2^{nd} rank DAC. VL is one LSB voltage from the coarse DAC. The last differential pair (shown furthest to the right in Figure 3.2) adds a drain current proportional to Vfine, the output of the fine DAC. The analog output of the 2^{nd} rank DAC (and overall DAC) is given by the following equation [18]:

$$V_{out} = V_{coarse} + \frac{VL \times \sum_{1}^{4} B_n \times 2^{n-1}}{16} + \frac{V_{fine}}{16} \tag{3.1}$$

The output voltage range of the DAC is reported to be from the negative rail to 3.392 V. Twelve of the DAC channels were current output rather than voltage output. The output current for these DAC channels ranges from 0 to 384 μA.

The linearity of this triple-rank DAC is dependent upon resistor matching and g_m matching. The authors report a maximum DNL error of 0.82 LSBs. The maximum INL error is 3-LSBs at the lower end of the DAC's output range, but is constrained to less than .99 LSBs for most of the output range. The authors do not present any dynamic performance characteristics such as THD, SNR, SNDR, or ENOB. There are also no results showing matching between DAC channels. The resistor strings are shared between multiple channels, but the 2nd rank DAC is not. Because of this, separate channels could have different characteristics. There is also the likelihood

that a change of inputs to one channel causes a glitch on another channel. This can occur because the resistor string nodes are tapped out through switches to MOSFET gates within the 2nd rank DACs of separate DAC channels. As the digital input of one channel is changed, charge can be injected into the resistor string node, causing a glitch at the other resistor string nodes and at the output of the other DAC channels.

The power dissipation of this DAC was reported to be 110 mW, or an average of 3.9 mW per channel. Conditions for this power measurement were not given. The power consumption of the DAC will change as the digital input changes, especially in the current output channels.

A microphotograph of the resistor string and a single channel of the DAC is shown in Figure 3.3. The area of each DAC channel is 1.535×0.31 mm^2. The area of the resistor string is less than the area of the DAC channel. The area saved by sharing the resistor string between channels is probably close to a factor of 2.

Other multi-channel resistor string DAC architectures have been presented by Levinson *et al.* [20] and by Churchill *et al.* [21]. Both of these architectures incorporate a primary resistor string shared between channels and additional resistor strings in each channel for more resolution. Levinson *et al.* uses a voltage summing amplifier to sum the outputs of the MSB and LSB resistor string DACs. This approach is similar to that presented by Imamura. The architecture presented by Churchill *et al.* is a segmented resistor string architecture that requires buffers between the resistor strings. Simulation or measurement results for these two proposed DAC architectures were not presented.

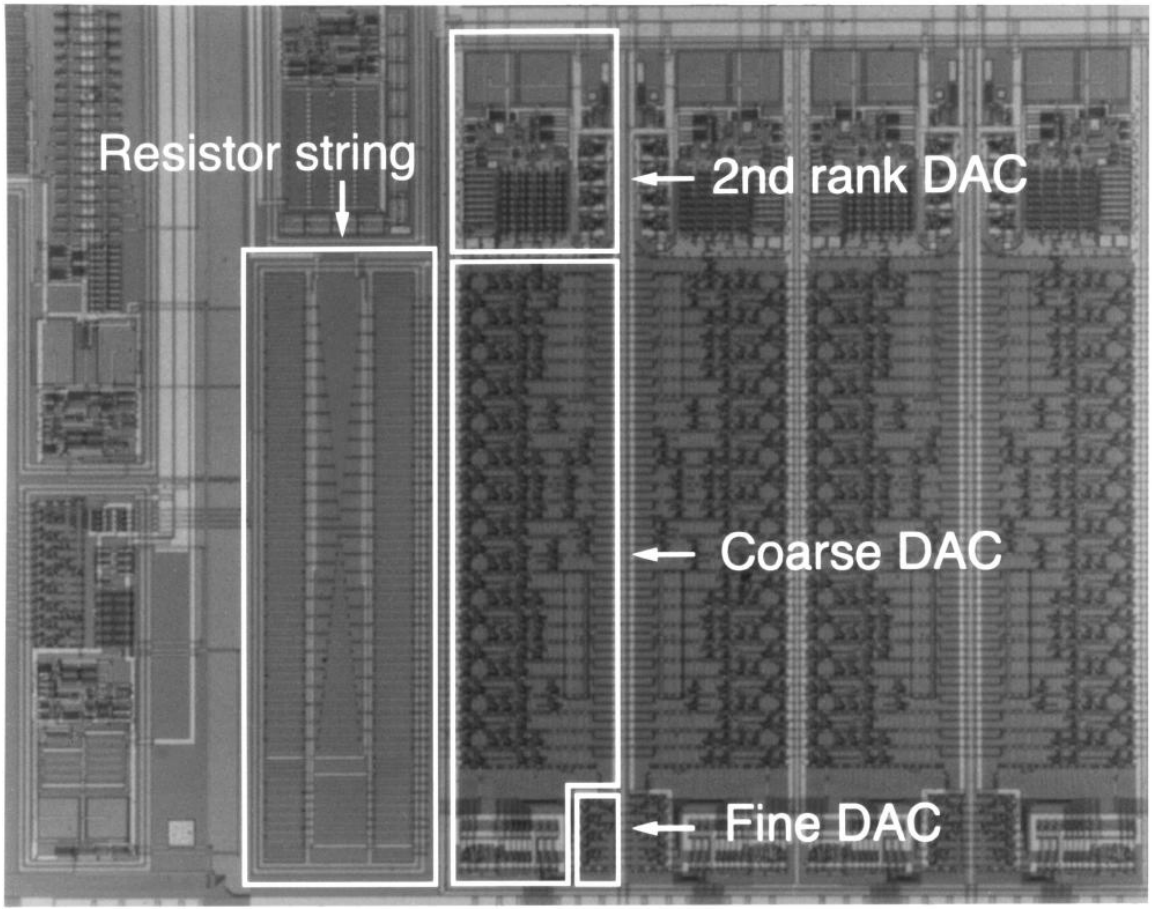

Figure 3.3: Resistor string and single channel of triple-rank DAC [19]

3.3 Suitability of Ramp Based DAC Architectures for Multi-Channel Applications

As discussed in the previous chapter, the dual-ramp DAC has a speed advantage over the single-ramp DAC architecture. Unfortunately, the dual-ramp architecture has a coarse and fine DAC that operate in parallel. The coarse and fine current sources are turned off by the MSB or LSB comparator. The current sources need to be turned off at different times for different channels in a multi-channel DAC, so there must be separate hardware for each of the channels.

The single-ramp architecture is not compatible for high speed applications, but it is area efficient, power efficient, and suitable for low to moderate speed use (less than 100 kHz for DACs as high as 1 kHz). It does not depend on resistor matching for linearity. Its accuracy depends largely on the accuracy of the ramp generator and sample and hold circuits. For multi-channel applications, the basic single-ramp architecture can share a digital counter among channels. A digital comparator would need to be provided for each channel. Because the ramp generator is stopped when the comparator of one channel trips, it can not be shared between channels. This is unfortunate, because the ramp generator can take up a significant amount of area. One possible solution is to use a sample and hold circuit in each channel to sample the ramp voltage when the comparator in that channel trips. This would cause the output of the DAC to be updated when the comparator trips, instead of being updated periodically at the end of each conversion. The response of the DAC to an input waveform would be distorted. Figure 3.4 shows a MATLAB simulation result of the sine wave response of an ideal 12-bit DAC compared to the single-ramp

DAC described above. The figure illustrates the signal-dependent waveform distortion caused by the basic single-ramp DAC architecture. The next chapter will present a novel DAC architecture that is able to share the ramp generator between multiple DAC channels without causing signal distortion.

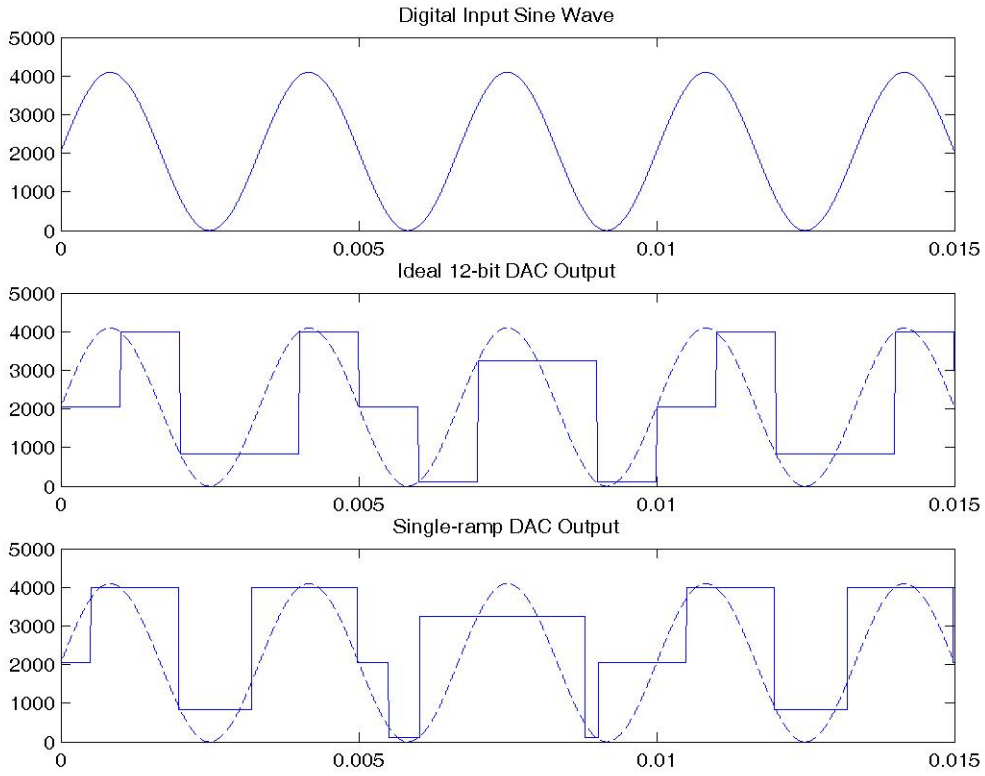

Figure 3.4: Sine wave response of an ideal 12-bit DAC and a basic single-ramp DAC with a shared ramp generator between channels

Chapter 4

Overview of Dissertation Research

4.1 Multi-channel DAC Architecture

This chapter discusses a new multi-channel DAC architecture that allows hardware to be shared between channels. As discussed in the previous chapter, a basic single-ramp DAC architecture is not able to share the ramp generator circuit between multiple channels. The architecture presented here is able to share this hardware without causing input-signal dependent distortion of the sampled digital waveform. To accomplish this, each channel in this architecture samples the ramp voltage when its comparator trips, but waits until the end of the conversion to pass this voltage to the channel's output. To achieve this operation, each channel includes a ramp-sampling analog memory unit (AMU) with control logic. The architecture of the DAC is shown below in Figure 4.1. Three channels are shown, but the number of channels can be expanded by adding additional comparators and AMU circuits.

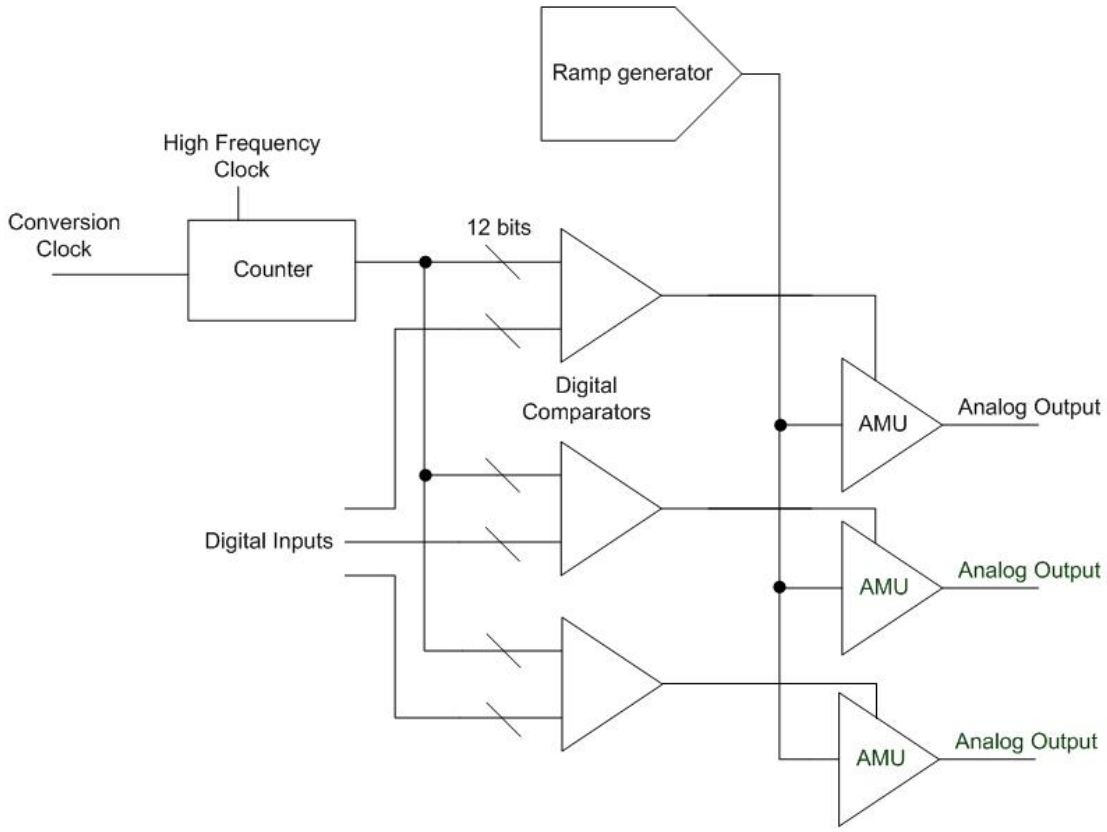

Figure 4.1: Architecture of a 3-channel single-ramp DAC

The counter and the ramp generator circuits start synchronously with a rising edge of the conversion clock. The digital comparator sends a signal to the control circuitry in the AMU when the counter value reaches the digital input. The AMU circuit samples the ramp voltage when this signal is received. The output of the AMU circuit is updated at the end of the conversion. The details of these circuits are discussed in the next section.

4.2 DAC Components and Design Issues

This DAC uses a Gray code counter architecture that was originally presented by Milgrome et al. [22]. This architecture is useful for low power and low speed applications. The counter is pipelined, and has one stage for each bit. The schematic for one stage of the counter is shown in Figure 4.2. The skew from the first stage to the last stage of the counter limits the maximum count rate. If the skew is a significant portion of the clock period, the counter will cause INL and DNL error in the DAC. Because the counter is double edge triggered, the counter clock frequency needs to be higher than 2.048 MHz for 1 kSps 12-bit DAC operation (there must be 4,096 counts per conversion).

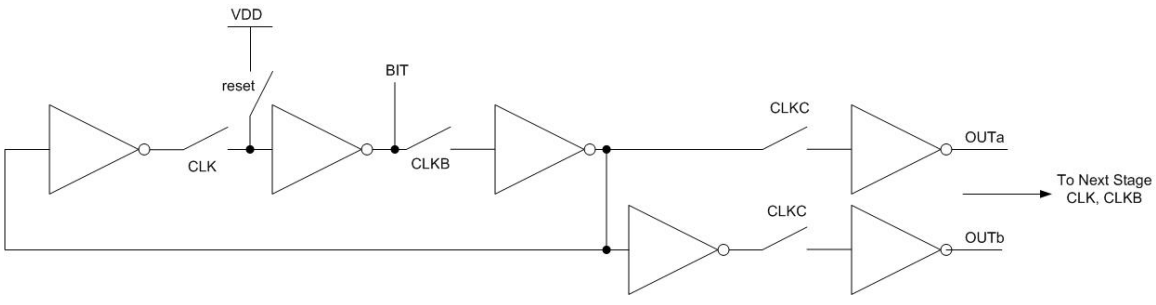

Figure 4.2: Single stage of a pipelined Gray code counter

The ramp generator consists of a high impedance current source driving a capacitor. The slope of the ramp is set by the capacitance value and the current ($dV_{ramp}/dt = I_{ramp}/C_{ramp}$). A schematic of a basic ramp generator is shown below in Figure 4.3. The ramp starts when the reset switch opens. A high output impedance is essential to the ramp generator's linearity because finite output impedance of the current mirror will cause the ramp current (and therefore ramp slope) to change as the ramp voltage changes. Such a change in ramp current would cause distortion in the ramp and non-linearity in the DAC. A ramp generator using a current source with an output impedance of 1 MΩ would result in the distorted ramp waveform shown in Figure 4.4. An output impedance of 10 MΩ will result in the waveform shown in Figure 4.5. This waveform is not visibly distorted, but it is only 6-bit linear. The ramp deviates from a best fit line by as much as 31 mV. In order for the ramp to be 12-bit linear, an output impedance of at least 1 GΩ is required.

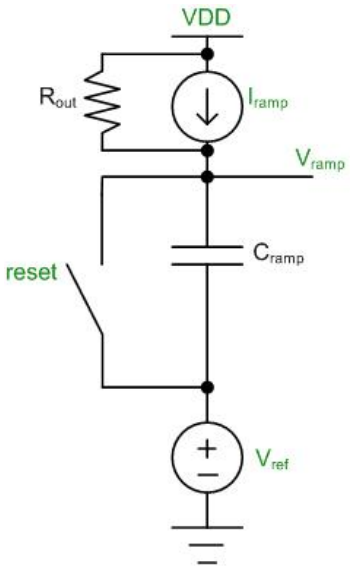

Figure 4.3: A basic ramp generator

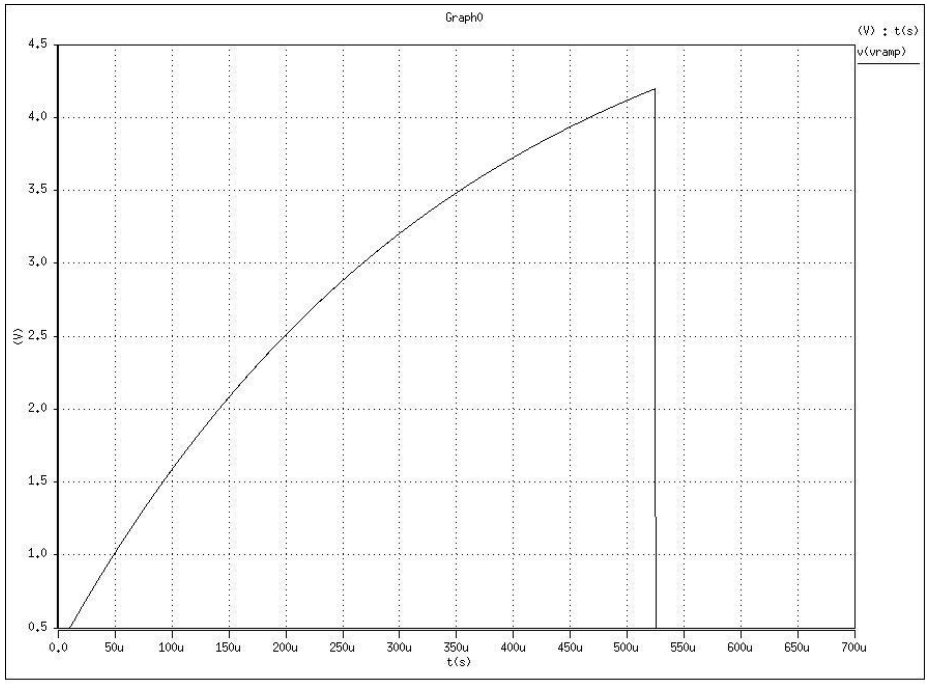

Figure 4.4: Ramp waveform generated using a 1 MΩ current source

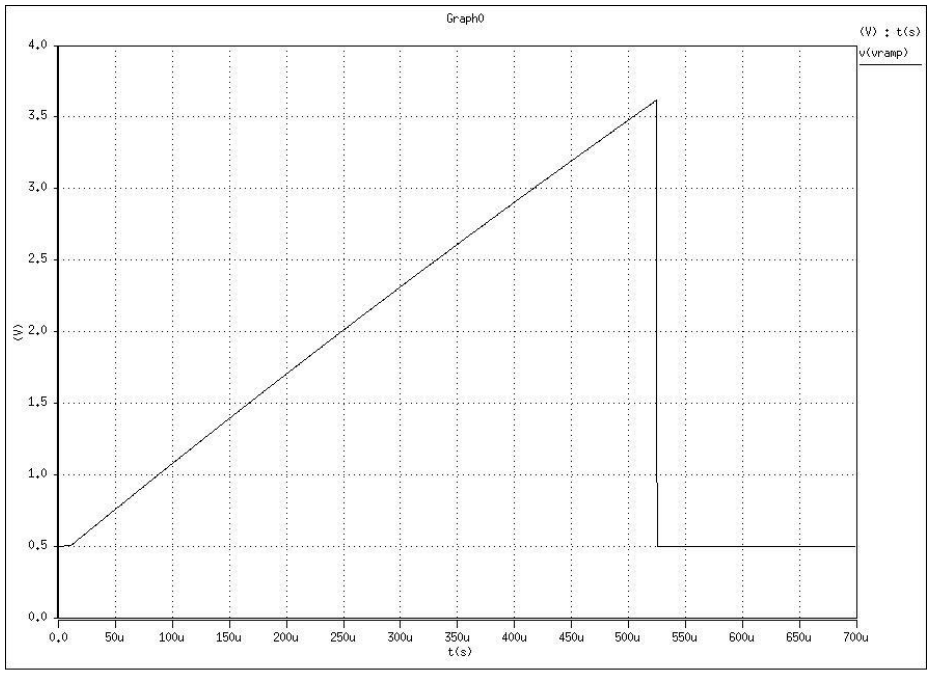

Figure 4.5: Ramp waveform generated using a 10 MΩ current source

The schematic of the ramp generator is shown in Figure 4.6. The negative feedback around the operational transconductance amplifier (OTA) is used to mirror the input bias current (IBIAS) to the ramp current (I_{ramp}). This regulated cascode current mirror configuration has a high output impedance. The output impedance of this regulated cascade configuration can be calculated using the small signal model of the PMOS output device, as shown in Figure 4.7. The output impedance of the ramp generator is derived below in equations 4.1-4.6, where R_{out} is the output impedance, A is the dc gain of the amplifier, g_m is the transconductance of the PMOS device, and r_o is the drain-source impedance of the PMOS device.

$$R_{out} = \frac{V_{test}}{I_{test}} \tag{4.1}$$

$$V_g = -AV_s \tag{4.2}$$

$$g_m V_{sg} = g_m(V_s + AV_s) = g_m V_s(1 + A) \tag{4.3}$$

$$I_{test} = \frac{V_{test} - I_{test}}{r_o} - g_m V_s(1 + A) \tag{4.4}$$

$$V_s = I_{test} 500k\Omega \tag{4.5}$$

$$R_{out} = r_o + 500k\Omega + g_m r_o(500k\Omega)(1 + A) \tag{4.6}$$

From simulation, A was found to be 158.5, g_m was found to be 32μS, and r_o was found to be 3.26 MΩ. Substituting these values into Equation 4.6 gives a value of 8.3 GΩ for R_{out}. This output impedance is more than sufficient for 12-bit linearity. Simulations of the ramp generator (loaded by an output pad with ESD protection) were run to get the output impedance of the ramp generator vs. frequency. These simulations were run with the DC value of the ramp voltage at both extremes of the

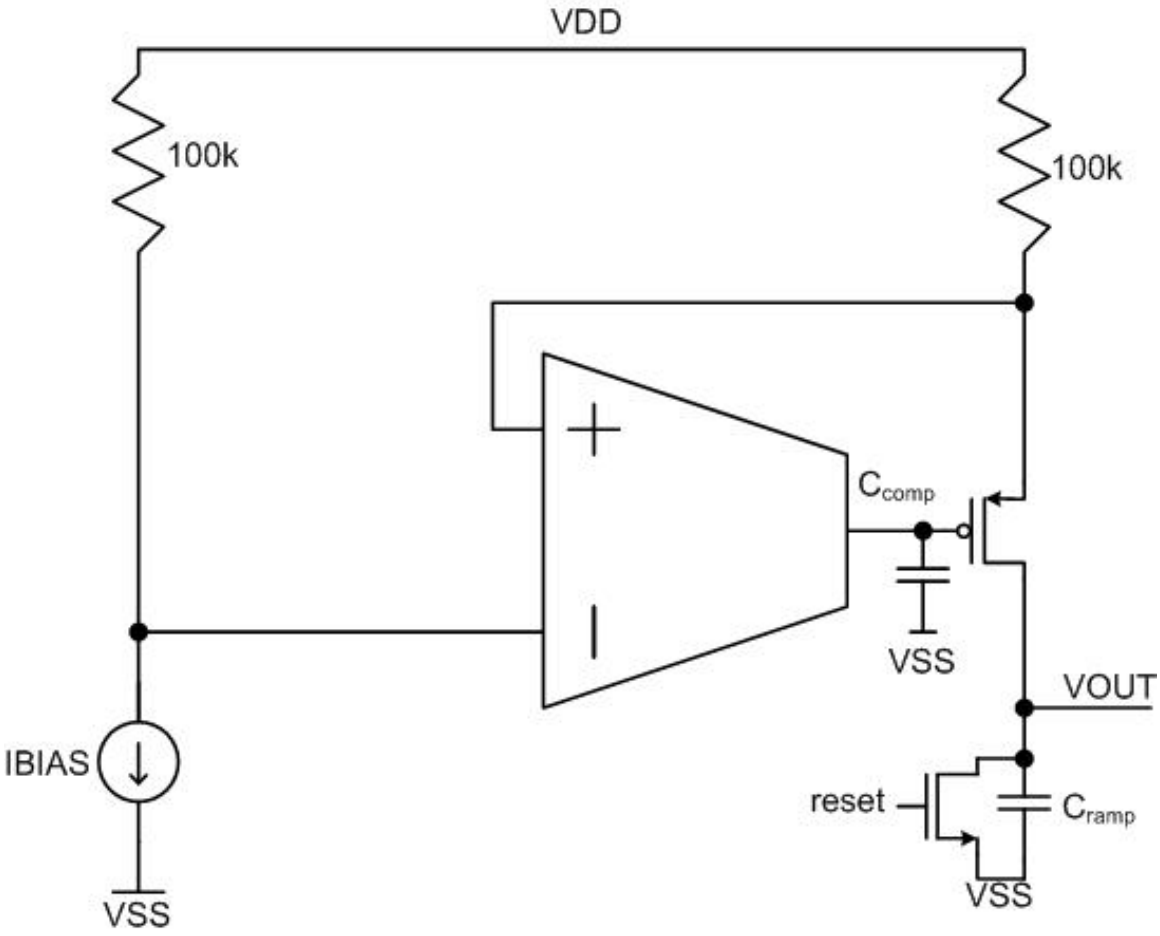

Figure 4.6: Ramp generator

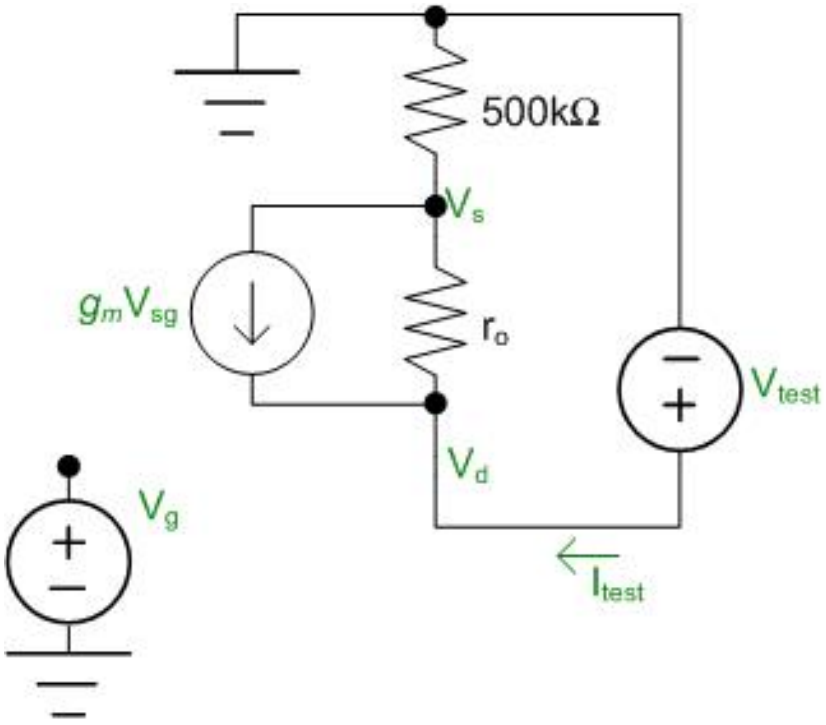

Figure 4.7: Small-signal model for calculating ramp generator output resistance

ramp generator's range. The output impedance of the ramp generator vs. frequency and over temperature is shown in Figure 4.8 and Figure 4.9. These simulation results show that the ramp generator's output impedance is reduced at higher temperatures. The impedance is still theoretically high enough for 12-bit linearity at high temperatures.

In order to save space and improve testability, the ramp capacitor can be external to the chip. An NMOS reset switch may be used to reset the ramp generator when the counter has reached a full scale count (4,096). For 1 kSps DAC operation, the counter will be operating at 4 MHz. At this frequency, a full scale count will occur in 512 μs, allowing 488 μs before the next conversion begins. The ramp generator will ramp from 0.5 V to 3.5 V in 512 μs. A ramp capacitance of 350 pF and a ramp current of 2 μA is used for this test chip. If both are supplied externally, the ramp slope can be tuned on the test board if necessary. The gate capacitance on the NMOS reset switch is approximately 9 fF. When the reset switch is turned off, the charge injection from the reset switch adds an offset of less than 0.2 LSBs. Because this is a constant offset it will not contribute to non-linearity error.

The logic circuit in Figure 4.10 is used to control the counter and ramp generator. The SOC (start of conversion) is the conversion clock. The EOC (end of conversion) signal comes from the last stage of the Gray code counter. A rising edge of this signal indicates that the counter has counted to a full scale count (4,095). The POR (power on reset) signal is tied to VDD on the test board through a jumper. The CLKin signal is the high frequency counter clock. The rampstart signal is connected to the reset switch in the ramp generator. The CLK and CLKB signals go to the Gray code counter. On a rising edge of the SOC signal, the START_in signal will go high. This

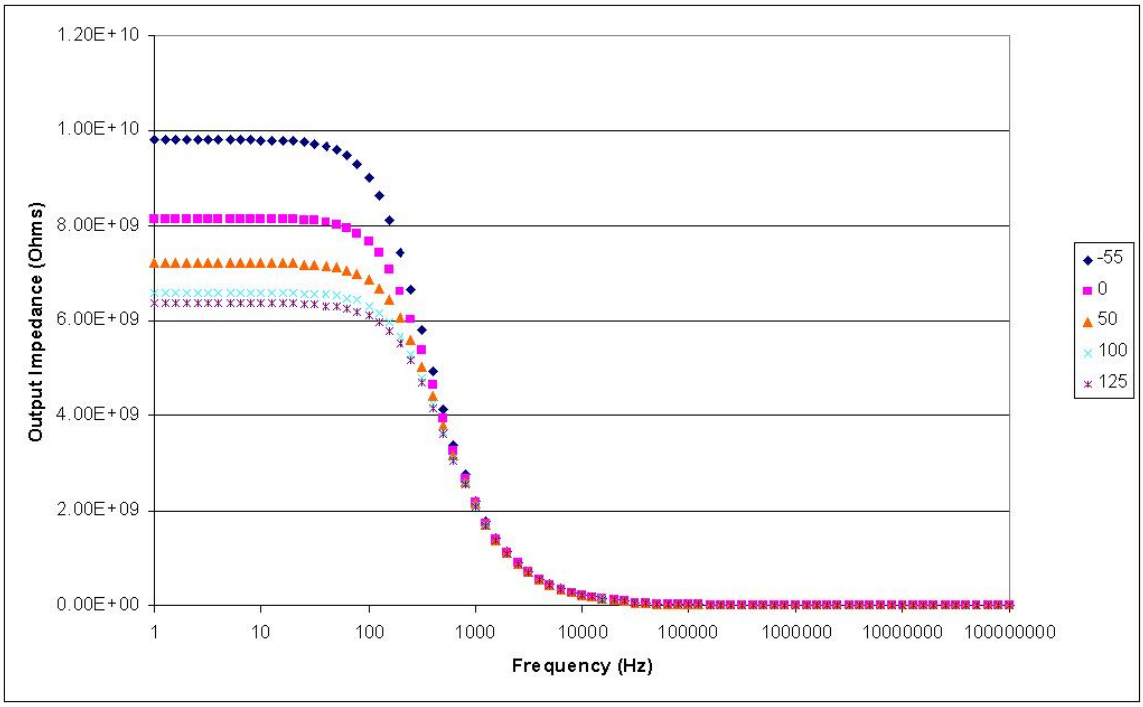

Figure 4.8: Ramp generator output impedance vs. frequency with Vramp at 0.5 V

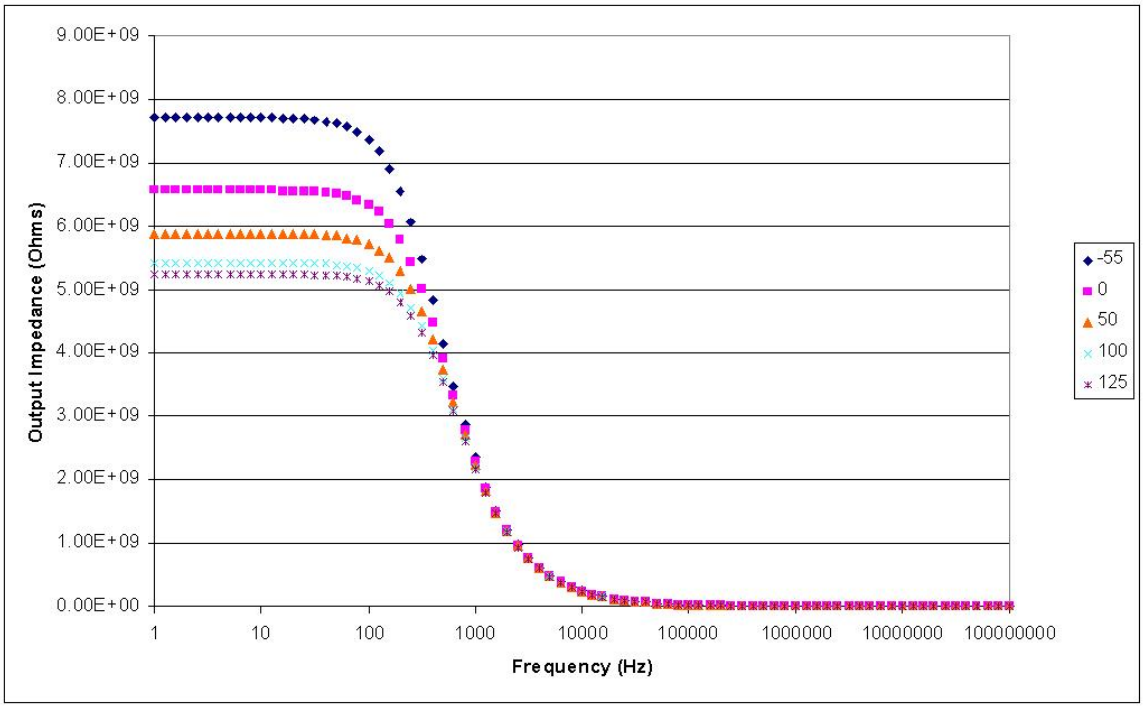

Figure 4.9: Ramp generator output impedance vs. frequency with Vramp at 3.5 V

starts the ramp generator and Gray code counter simultaneously. The START_in signal will stay high until the counter reaches a full scale count, and the EOC signal goes high. At this time, both the counter and ramp generator will shut off until the next rising edge of the SOC signal. The EOC , SOC, rampstart and ramp signals are shown over several conversions in Figure 4.11.

There is a binary to Gray code converter in front of the digital comparator that allows the binary input to be compared to the Gray code counter value. The digital comparator for each channel consists of a set of exclusive-OR and OR gates that generates a logic high at the output when the counter value equals the digital input value. This results in a pulse at the comparator output whose pulse width is half of a counter clock wide. This pulse signal is connected to the AMU control logic circuit of that channel. The control logic generates four signals that control the switches within the AMU circuit. The AMU circuit schematic is shown below in Figure 4.12. A unity-gain buffer is used to isolate the ramp generator from charge injection in the AMU. There are two capacitors in the circuit. These capacitors are used to store the sampled ramp voltage and pass it to the output. One capacitor samples and holds the ramp voltage while the second capacitor connects the ramp voltage sampled during the previous conversion to the output of the circuit. The capacitors alternate tasks between conversions. The control logic is shown in Figure 4.13. The logic circuit generates $\Phi 3$ and $\Phi 4$ using a non-overlapping clock generator. COUT is the comparator output pulse. This signal is used to create $\Phi 1$ and $\Phi 2$.

The timing of the control signals is shown in Figure 4.14. Phases $\Phi 3$ and $\Phi 4$ represent the sampling periods of the capacitors. The switches on these two phases connect the capacitors to the buffered ramp voltage. These switches open when the

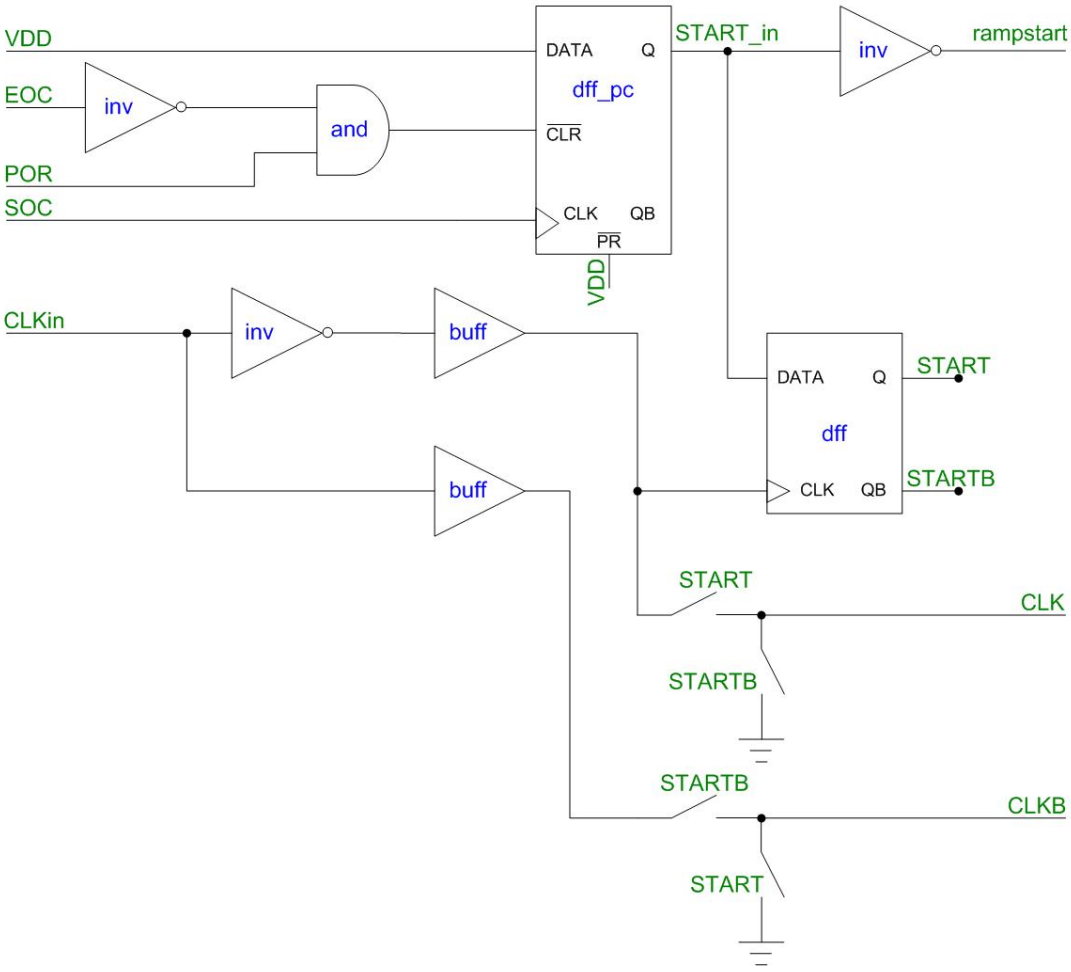

Figure 4.10: Counter and ramp generator control circuit

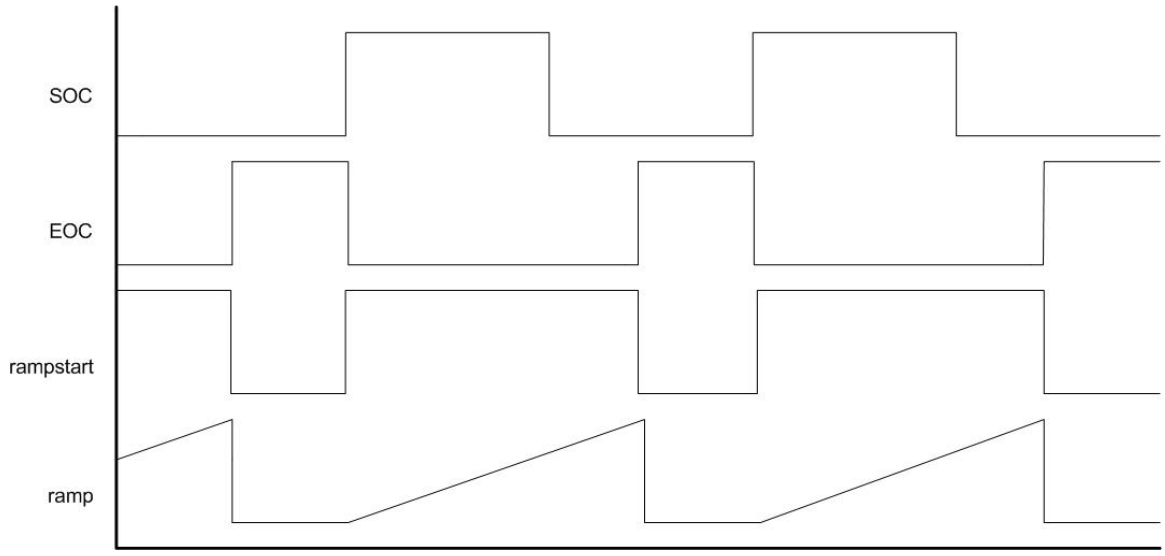

Figure 4.11: Control signals for counter and ramp generator control circuit

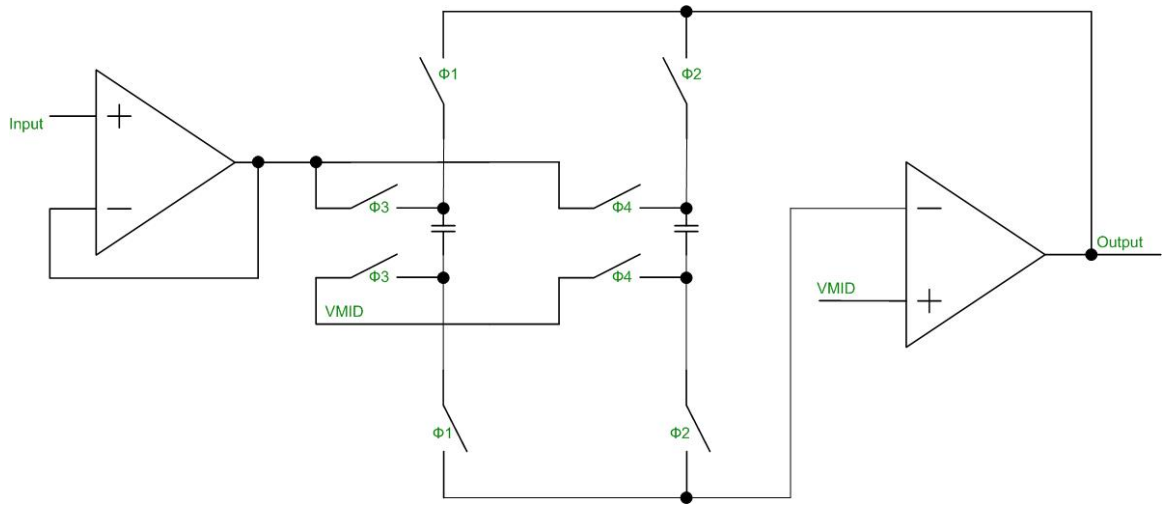

Figure 4.12: Analog memory unit (AMU)

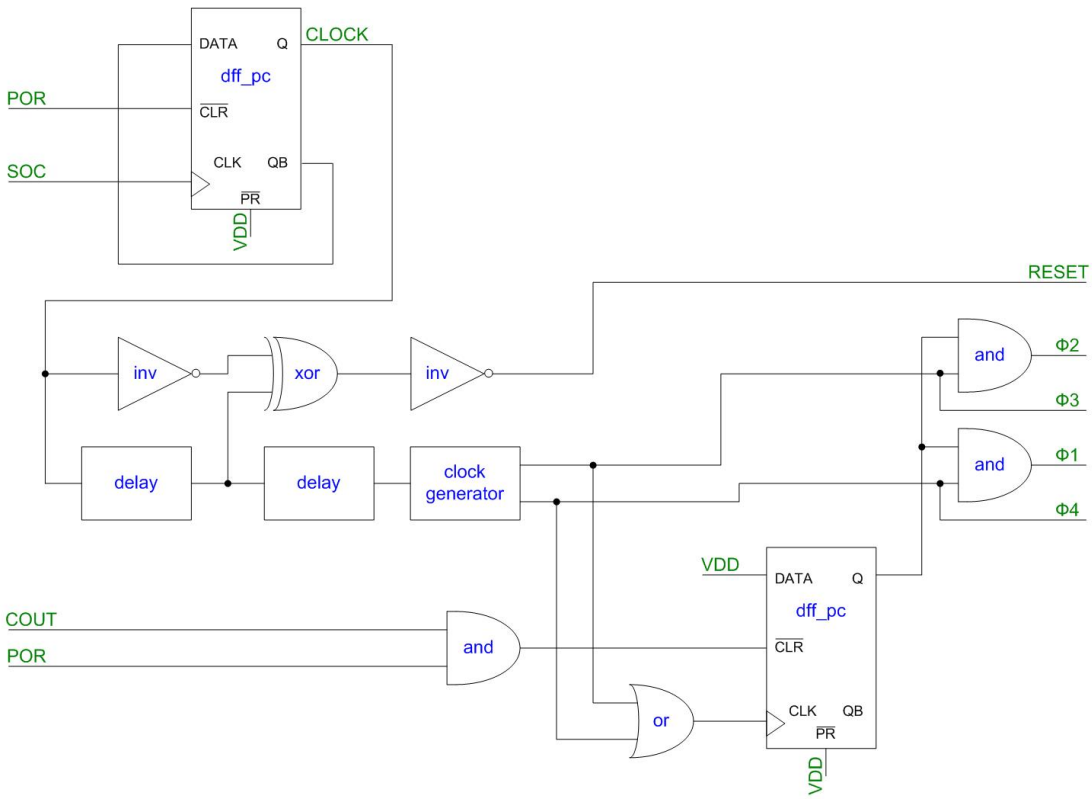

Figure 4.13: AMU control circuit

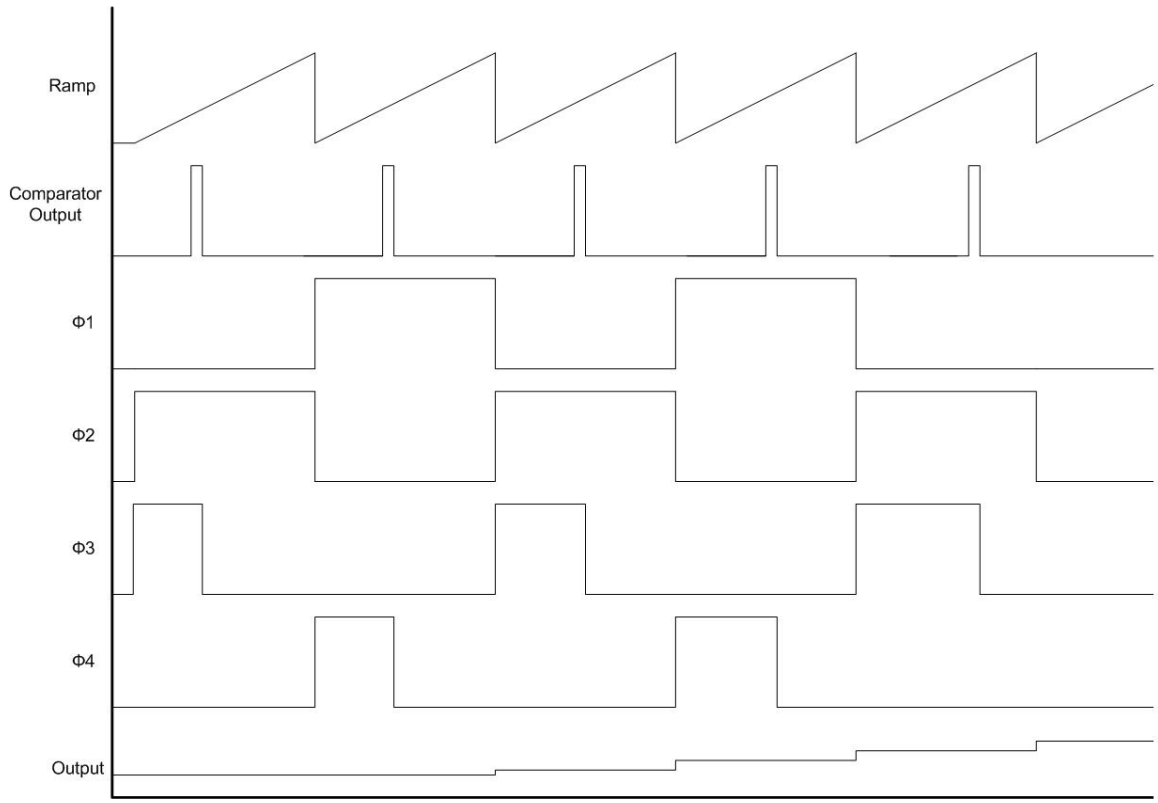

Figure 4.14: AMU control signals

comparator trips. In order to reduce voltage droop, both terminals of the capacitors are left floating for the remainder of the conversion (until Φ1 and Φ2 change). The capacitors hold the sampled ramp voltage at the output when phase Φ1 or Φ2 are high. A reset signal from the control logic drives a switch in the AMU (not shown) that removes the charge from the capacitor at the end of the conversion.

4.3 Prototype Chip Details

Due to chip area limitations, the DAC prototype chip was limited to 2 channels. The DAC is fabricated in the AMI C5N 0.5 μm process. It operates on a 5-V power supply. The analog output range is 3 V (0.5 V to 3.5 V). The LSB size (at 12-bit resolution) is 733 μV. The maximum conversion rate is 5-10 kSps, and is limited by the low power Gray code counter. A faster conversion rate can be achieved at the cost of more power, but the single-ramp architecture is not suitable for high speed applications. The worst case total power dissipation at 10 kSps is 3.96 mW.

4.4 Simulation Results

Spectre simulations of the Gray code counter show the skew between the first and last counter stages to be 8 ns at room temperature. The simulation results for the Gray code counter skew over temperature is shown in Figure 4.15. For 1 kSps DAC operation, the 8 ns of skew at room temp would cause a DNL error of less than 0.07 LSBs. This skew would cause a DNL error close to 0.5 LSBs for a 12-bit DAC

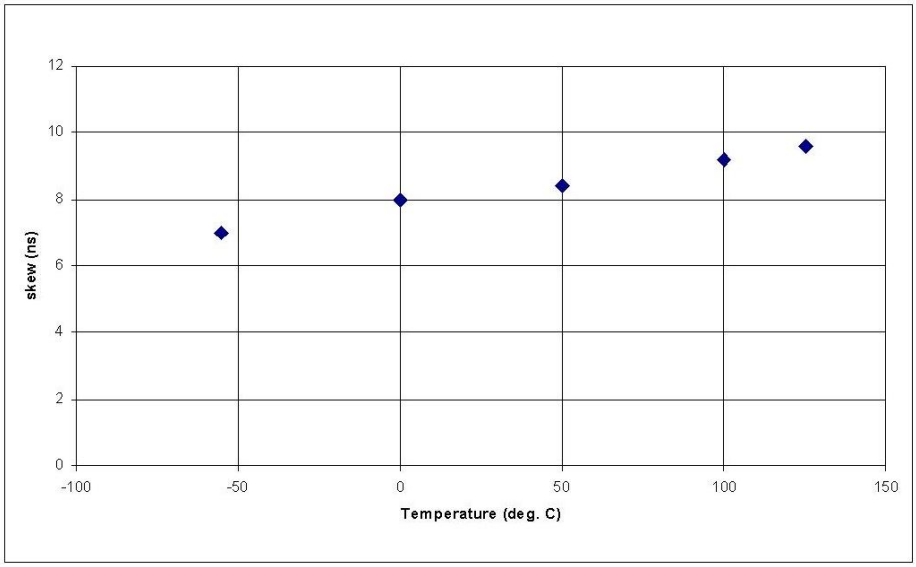

Figure 4.15: Gray code counter skew vs. temperature

operating at 15 kSps. The DAC is not expected to maintain 12-bit linearity at 15 kSps without a faster (and higher power) counter. The power dissipation of the counter was simulated to be 38 μW at 4 MHz and 54 μW at 40 MHz. Simulations of the ramp generator show the maximum deviation of the ramp from a best fit line to be 103 μV, or 0.14 LSBs. The simulated worst case power dissipation of the ramp generator is 790 μW.

It is time consuming to simulate this architecture, because a single conversion involves 4096 clock cycles. It is therefore not reasonable to simulate every input code to obtain a simulated INL and DNL for the DAC. Instead, simulations were run over the DAC's range to get an estimate of the linearity of the DAC. Figure 4.16 shows the simulation results.

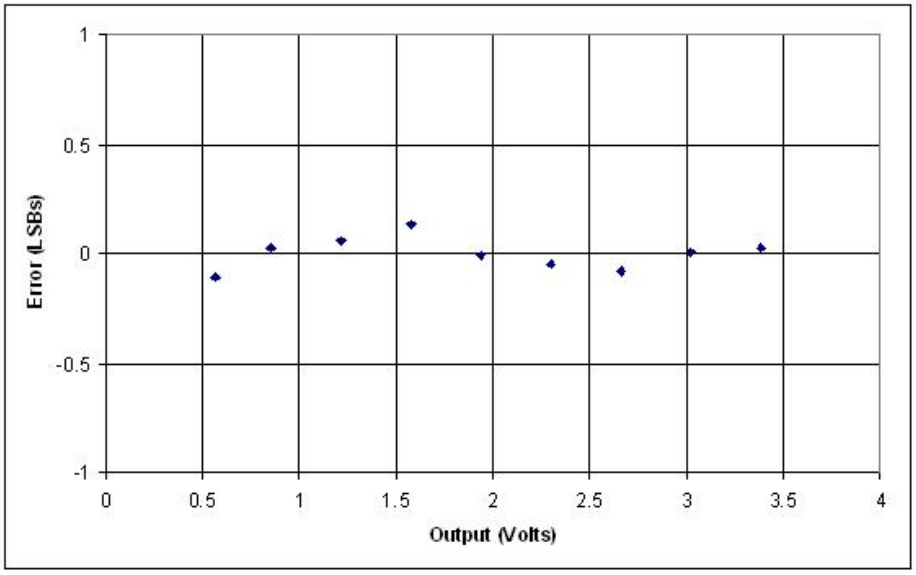

Figure 4.16: Simulated DAC Error vs. Output

4.5 Tools Used in the Research

For schematic entry, Cadence Composer was used. Cadence Virtuoso Analog Circuit Design Environment was used for netlist extraction, and Spectre was used for netlist simulation. The Cadence Virtuoso tool was used for layout. MATLAB and Microsoft Excel were used for data analysis. For testing preparation, Eagle Layout Editor was used for PCB layout. For data acquisition and analysis, a National Instruments USB-6259 DAQ card and Labview was used. The DAQ card was used for two purposes: to generate a 12-bit digital waveform to be used as the DAC input, and to collect the output of the DAC's channels using the analog input channels of the DAQ card. The 16-bit ADCs in the DAQ card are sufficient for measuring the DAC's linearity.

4.6 Layout

The layout of the DAC is shown in Figure 4.17. The 1-mm chip size limits the options for the layout geometry, but care was taken to use layout practices that optimize performance. The capacitors in the AMU circuit were implemented in a common-centroid array in the lower left of the chip layout. Each DAC channel alternates the use of two capacitors in the AMU circuit. These capacitors do not necessarily need to be accurately matched unless charge injection and droop are considered. If the capacitance values are not matched, the capacitors will still sample the voltage and store it. The charge injection and droop error will be consistent from one conversion to the next if the capacitors are matched (for a fixed digital input). The analog circuits are on the right side of the chip. They are separated from the digital circuits at the top left of the chip. The ramp generator is at the bottom right and the AMU circuits for each channel are at the middle and top of the right side. The use of guard rings in the analog section should help to isolate these circuits from the counter and digital control circuitry at the top left of the chip. Unfortunately, connections between the AMU capacitor array and the AMU circuits had to be routed close to the digital section of the chip, but care was taken to keep these traces as far from high frequency digital signals as possible. The analog and digital circuits are on separate supplies, which are tied together on the test board.

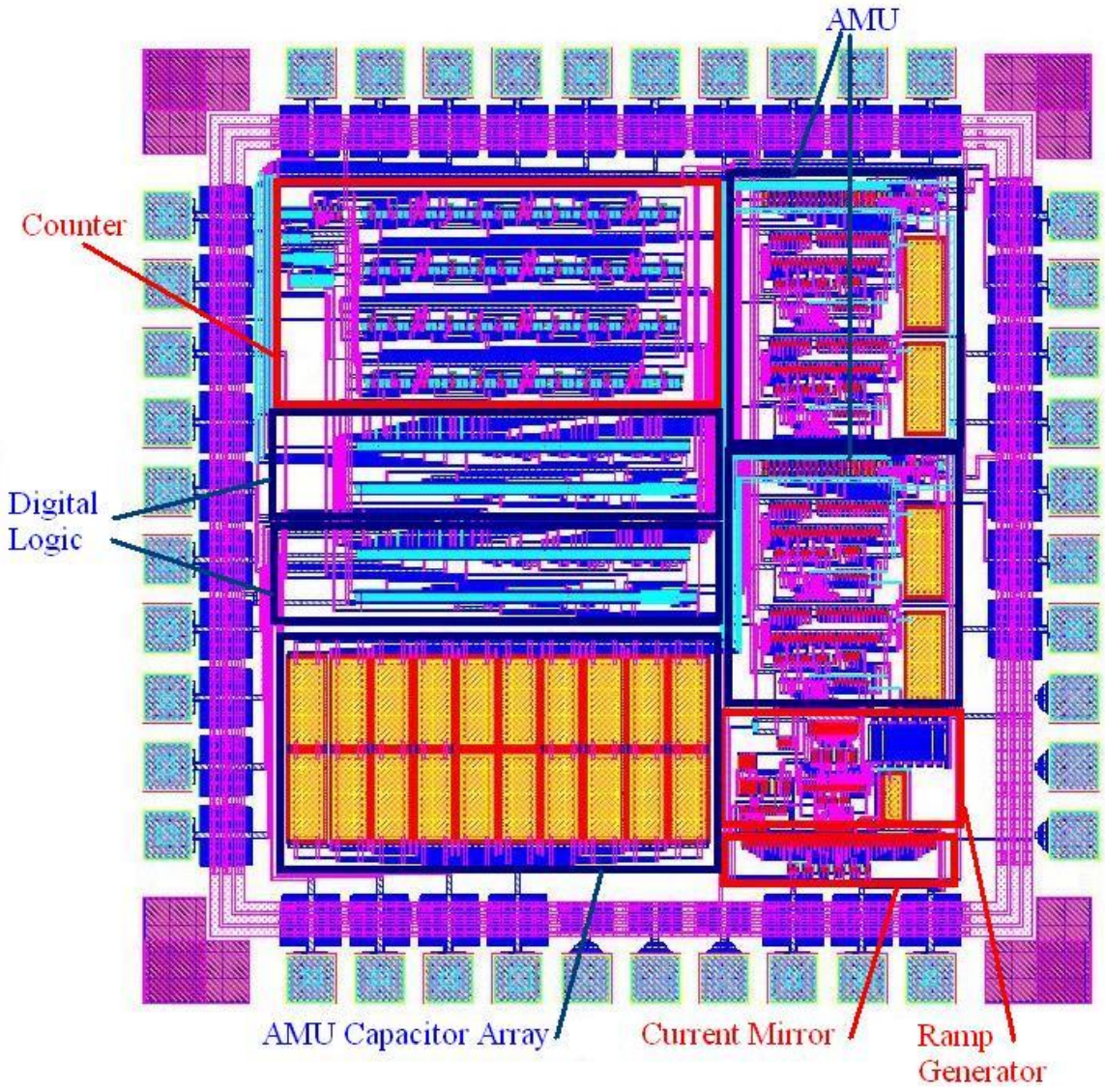

Figure 4.17: Multi-channel DAC layout

Chapter 5

Test Results and Analysis

5.1 Test Setup

The chip was fabricated in the AMI C5N process through MOSIS and packaged in a 40-pin DIP for testing. A microphotograph of the fabricated ASIC is shown in Figure 5.1. A four-layer PCB was designed for testing the DAC. The board is shown in Figure 5.2. Digital inputs to the DAC can be supplied on the board using dipswitch arrays or through a ribbon cable that connects to an NI DAQ card. Two 12-bit multiplexers are used to select between on board or external digital inputs. The digital input waveforms for the DAC were programmed using Labview. The Labview code programs the DAQ card to generate a digital waveform while simultaneously sampling analog inputs that are received from the DAC's output. A simplified schematic of the DAC's external connections on the test board and connections between the DAC and the NI DAQ card is shown in Figure 5.3.

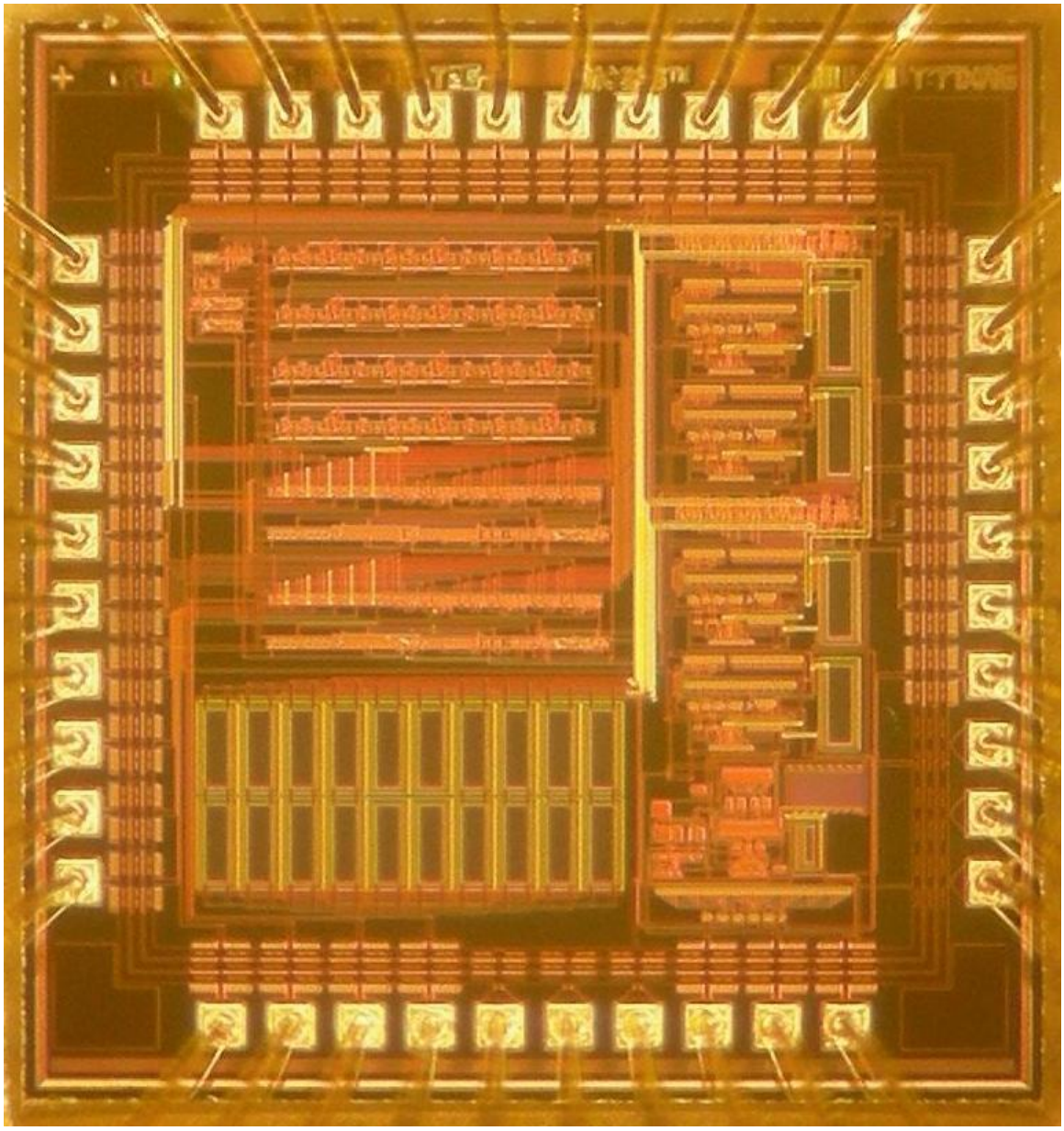

Figure 5.1: A microphotograph of the fabricated ASIC

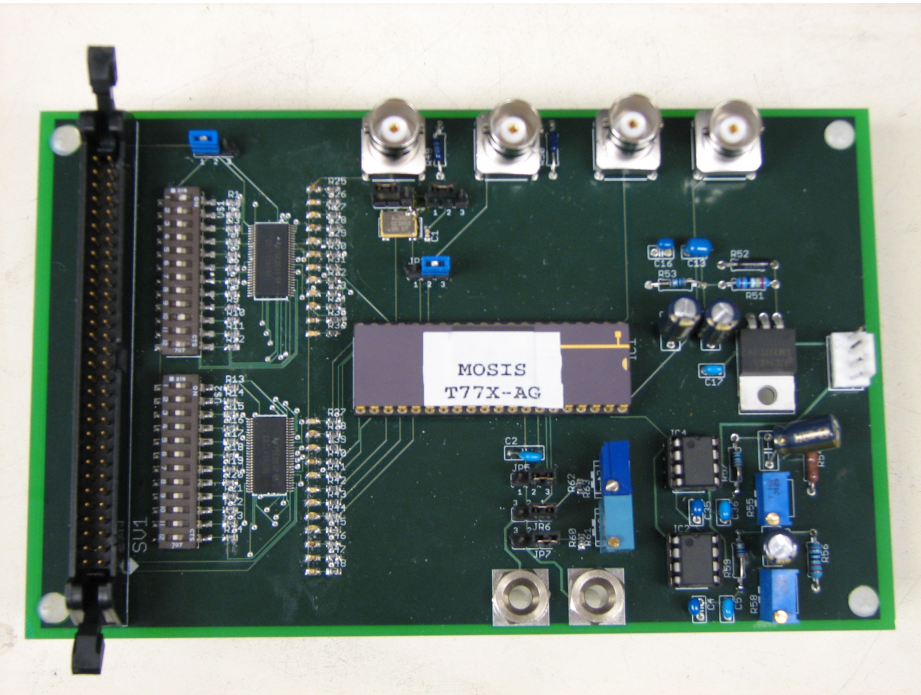

Figure 5.2: DAC test board

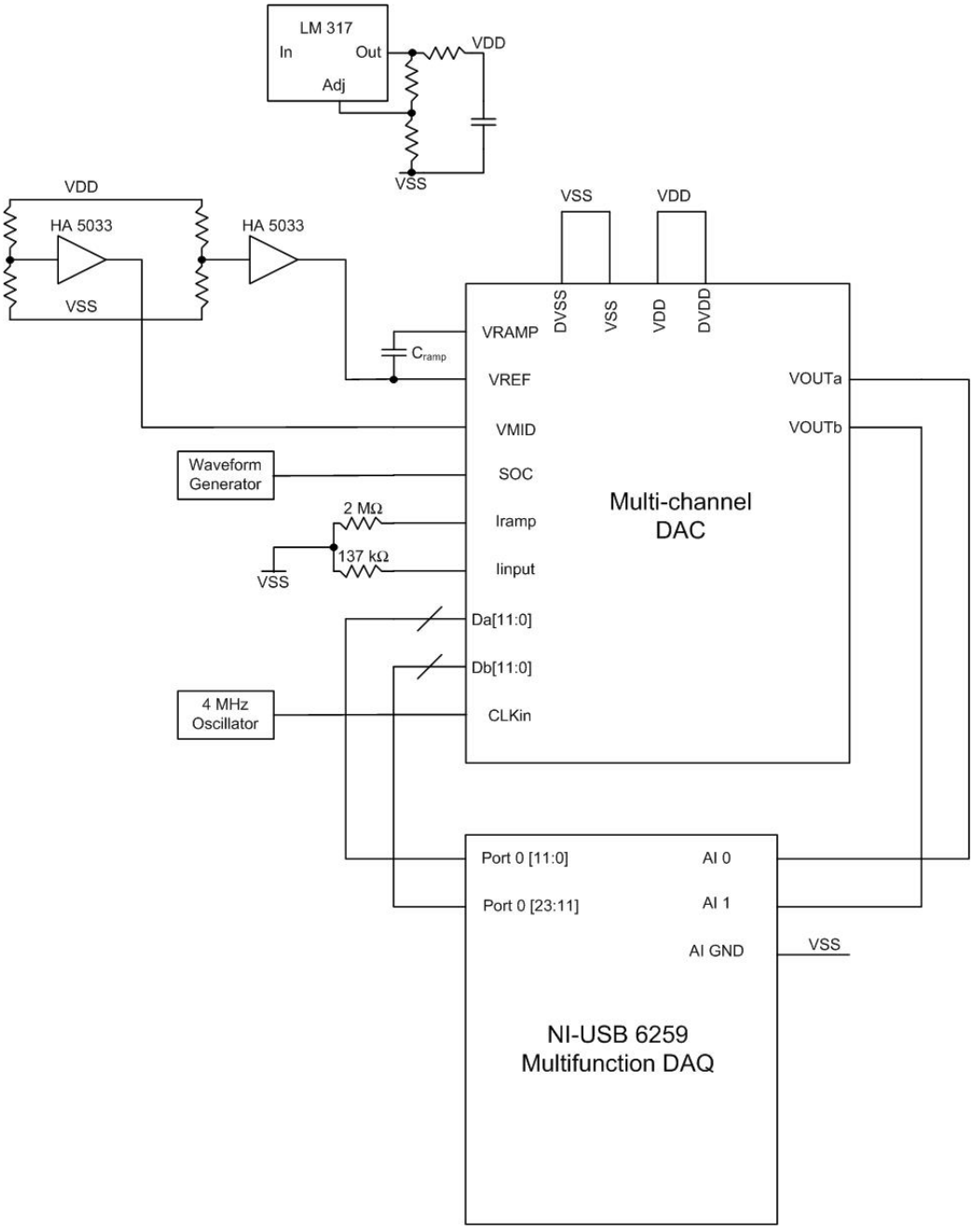

Figure 5.3: DAC external connections for testing

In order for the NI DAQ card to perform simultaneous digital waveform generation and analog sampling, a framed sequence structure needed to be used in Labview. The Labview code for producing a sine wave digital input to the DAC and simultaneously acquiring the corresponding analog samples from the DAC is shown below in Figure 5.4. The framed sequence structure in the center of the image ensures that the waveform generation and analog sampling are synchronized with an external clock. The external clock comes from a waveform generator, and is a phase-shifted version of the clock that goes to the SOC signal on the test board. This external clock edge occurs before the beginning of a conversion. This ensures that the digital inputs to the DAC are ready for the next conversion, and also that the analog output of the DAC is not sampled during the transition period between conversions.

The board has a 4 MHz oscillator to use as the counter clock. Jumpers are used to provide the option to shut down the on board oscillator and use an external clock instead. The ramp reference current and bias current can be adjusted using potentiometers on the board. The power supply voltage is regulated with an LM 317 voltage regulator. The supply voltage is filtered with an RC lowpass filter next to the regulator. Bypass capacitors are used at the regulator and next to the supply pins on the chip. The supply voltage is also used as a reference for resistive voltage dividers to generate the V_{REF} and V_{MID} reference voltages for the DAC. To prevent the DAC from affecting the output of the voltage dividers, these references are buffered using HA 5033 voltage follower video buffers.

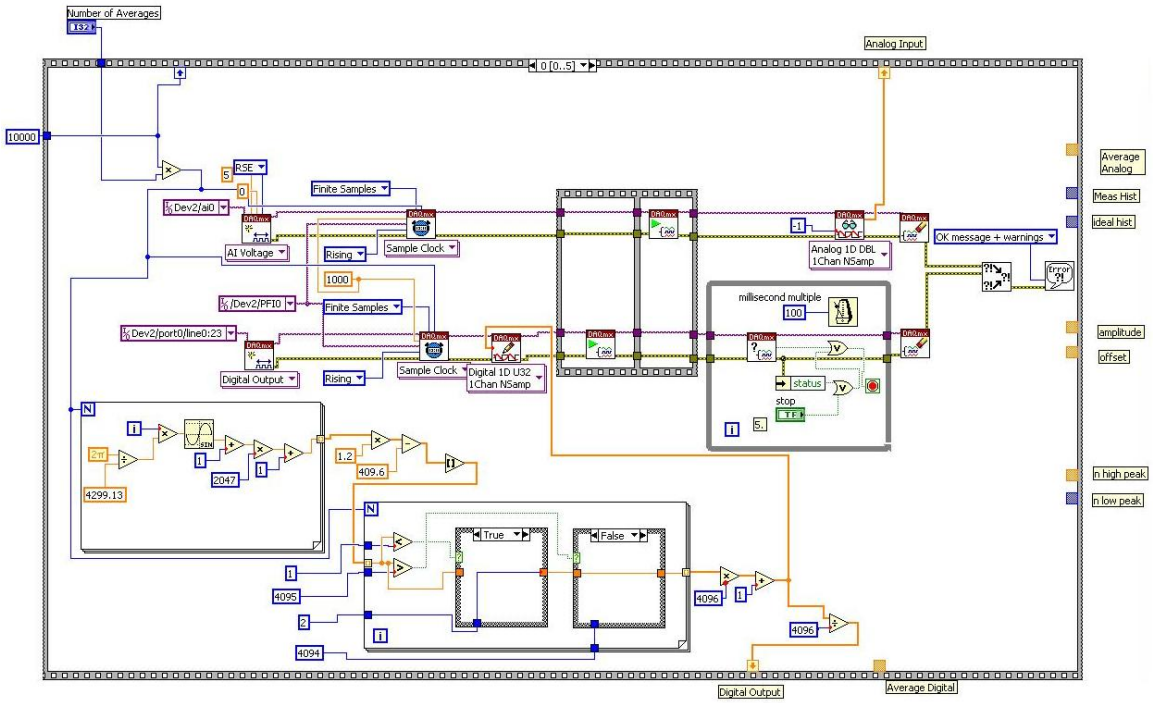

Figure 5.4: Labview code for synchronized digital waveform generation and analog sampling

5.2 Functional Test Results

The DAC was found to be functional by manually changing the inputs on the test-board using the dip switches while probing the analog output on an oscilloscope. During this testing, it was found that the DAC does not function correctly when given a zero code input. The analog output of the DAC should be approximately V_{REF} for a zero code input, but the output is close to the power rail. This problem is the result of a design flaw that was not noticed in simulations. The AMU control logic leaves the sampling capacitors floating when the input code is zero. Unfortunately, only a small number of input codes were tested due to the long simulation time required for a single conversion. After simulating the DAC with a zero input code, this problem was reproduced. A solution for this problem will be presented in the following chapter.

The DAC's response to a sine wave is shown below in Figure 5.5. The input sine wave ranges over the full scale of the DAC, excluding the zero code (1 - 4095). The DAC was operating at a sampling rate of 1 kSps.

It is obvious from this sine wave response that the DAC is functional and does not have any large blocks of missing codes. More extensive characterization of the DAC is discussed in the following sections.

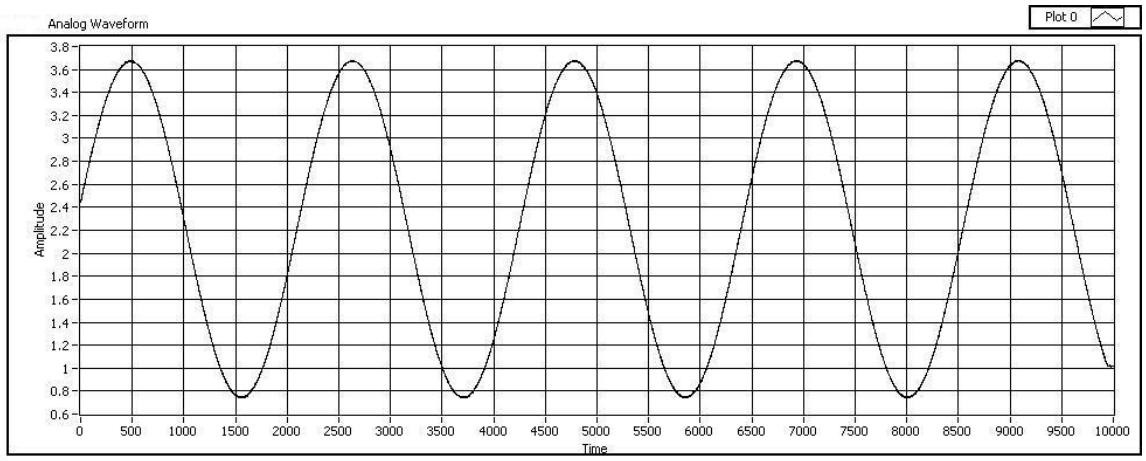

Figure 5.5: DAC sine wave response

5.3 Differential Nonlinearity and Integral Nonlinearity Test Results

A common method for measuring the differential nonlinearity (DNL) and integral nonlinearity (INL) is the histogram test [23]. This test uses a sine wave as the input to the DAC. The analog output of the DAC is histogrammed with bin widths of one least significant bit. The histogram is compared to the probability density function of an ideal sine wave to measure the linearity. If the input sine wave has amplitude A and frequency ω, then the probability of a sample being in a range between *V1* and *V2* is given by Equation 5.1 [24].

$$P(V1, V2) = \frac{1}{\pi}(arcsin\frac{V2}{A} - arcsin\frac{V1}{A}) \tag{5.1}$$

The difference between the measured and expected probability of the DAC output falling within an LSB range can be used to calculate the DNL error [24]. The equation

for the DNL error at a particular input is given by Equation 5.2. The INL error is measured by integrating the DNL error.

$$ERROR = \frac{Counts_{actual}}{Counts_{ideal}} - 1 \tag{5.2}$$

The length of data required for the histogram test is large for a high resolution converter. The number of samples M required for a high confidence measurement is given by Equation 5.3 [24]. The number of bits is represented by N. For a 99 % confidence level, $Z^2_{\alpha/2}$ is equal to 2.576. β is the accuracy in the measurement. To measure 12-bit DNL within accuracy of 0.2 LSBs at a 99 % confidence, 1.06 million samples are needed. Four million samples were taken for the linearity measurements shown in this chapter.

$$M = \frac{\pi 2^{N-1} Z^2_{\alpha/2}}{\beta^2} \tag{5.3}$$

In order to measure the INL accurately, the sine wave input to the DAC had an amplitude larger than the DAC input range and was clipped at the upper and lower range limits (4095 and 1). This was necessary because INL measurements are very sensitive to differences between the expected and actual sine wave amplitudes and offsets near the peaks of the sine wave. The exact amplitude of the best fit output sine wave can be estimated using a best sine wave approximation [1]. A simpler method is to estimate the best fit sine wave based on the two histogram maxima and overrange the input sine wave, thus reducing the INL measurement sensitivity to the amplitude and offset differences between the best fit and actual sine waves. However,

this method causes problems at the upper and lower end of the DAC range. The histogram test averages out noise for a sine wave input. Because the input sine wave is clipped, noise in the DAC will produce an incorrect number of counts in histogram bins that are close to the range limits since that noise will not be averaged out. Due to this problem, the INL and DNL close to the range limits were not tested.

The INL measurement is also sensitive to the impedance at the output of the ramp generator. The ramp capacitor is external to the chip, and leakage at this node on the test board will cause integral nonlinearity errors. After initial measurements showed significant INL error, the board was cleaned and baked to improve the impedance at the ramp generator output. After baking, a polystyrene moisture barrier (Qdope) was applied to protect the surface of the PCB so that a high impedance could be maintained over time.

The DNL results changed very little after the clean/bake, but INL results improved significantly. The DNL and INL test results before and after the clean, bake, and moisture barrier application are shown below in Figures 5.6 and 5.7, respectively. The test results show that the DNL error is contained to less than 0.4 LSBs. After cleaning and baking the board, the INL error is contained to +/- 2 LSBs. The improvement in INL after the clean and bake suggests that there was an impedance limitation at the ramp generator output node on the board. This could have been caused by moisture or other contaminants on the board. The impedance limitation would not affect the DNL measurement in a significant way, but would affect the INL.

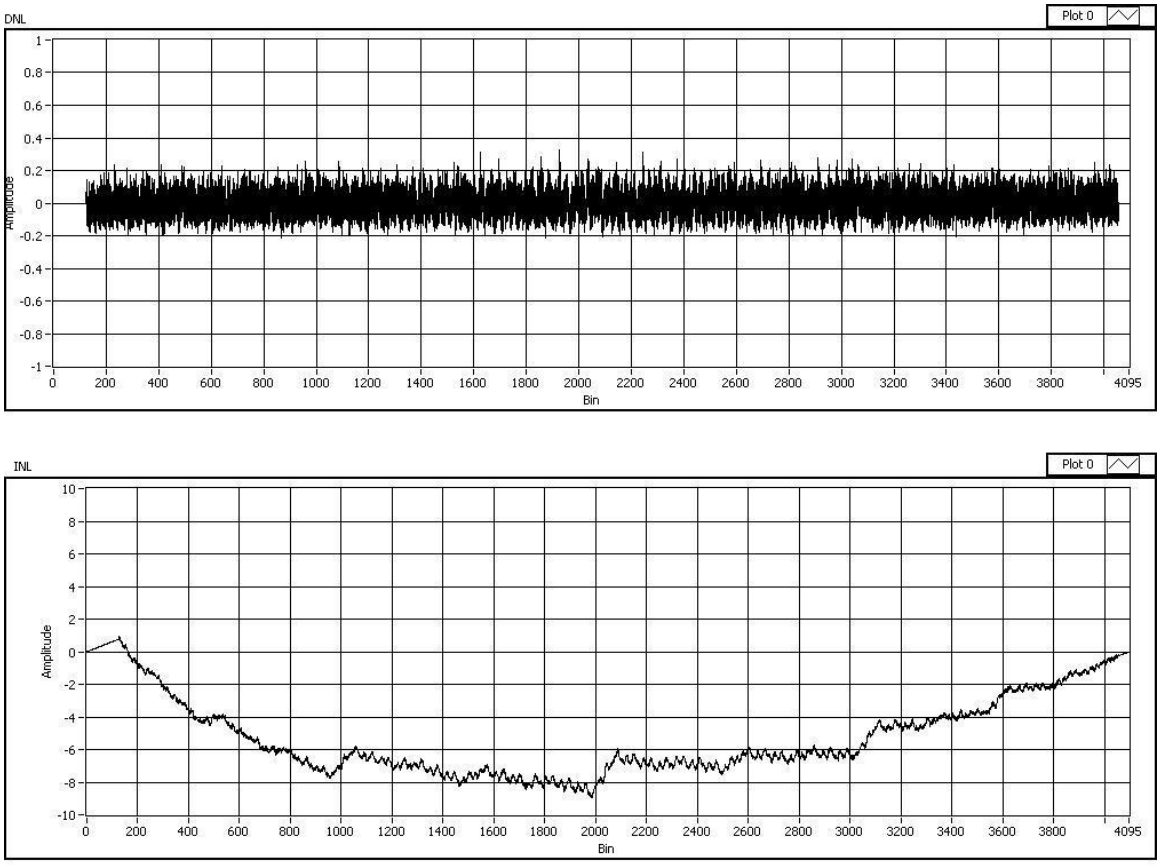

Figure 5.6: DNL and INL measurement results before board clean and bake

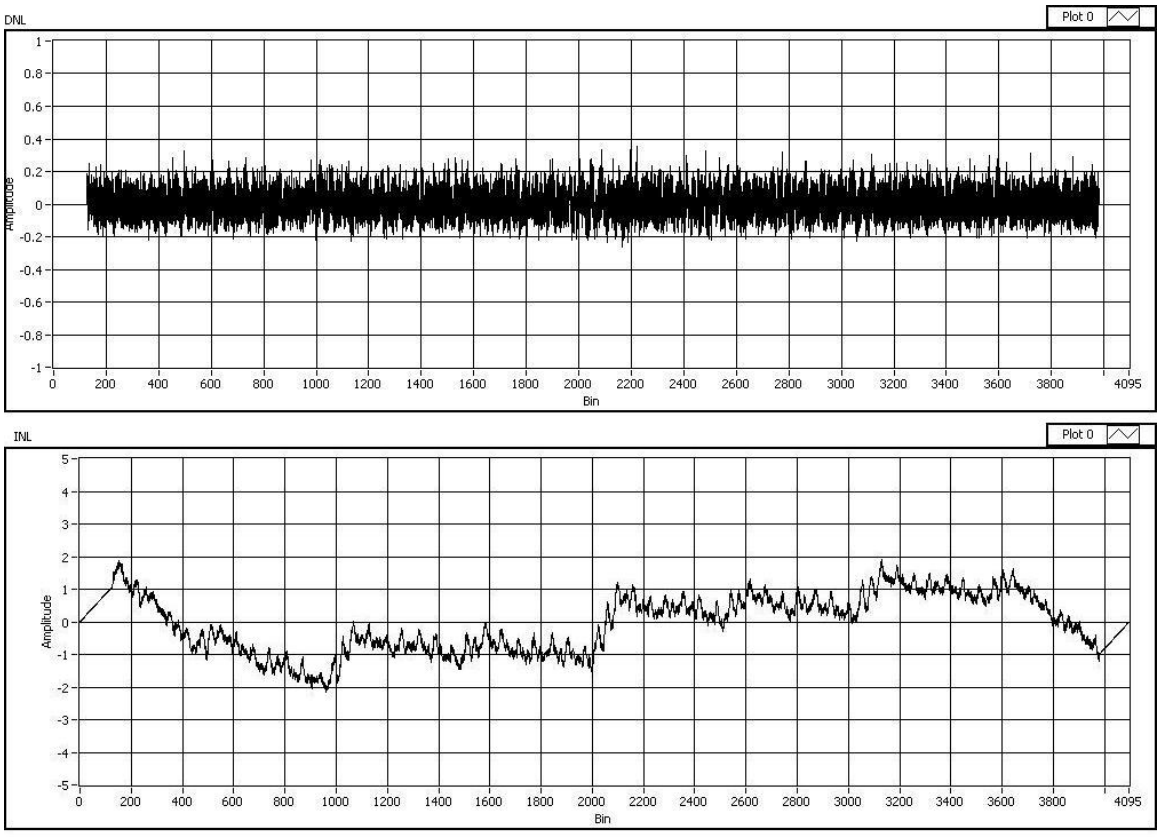

Figure 5.7: DNL and INL measurement results after board clean and bake

The data presented in Figures 5.6 and 5.7 are from one channel of a single chip. DNL and INL testing was performed on three separate chips, with similar results. The worst maximum DNL error from the 3 chips was found to be approximately 0.45 LSBs. The INL error for the worst chip was contained to +/- 3.5 LSBs. The results of these linearity tests are shown below in 5.8. Testing of the 2^{nd} channel shows similar DNL and INL results, although there is a constant offset between channels of the same chip that was measured to be 8 mV on the worst case chip. This offset is most likely introduced by the operational amplifiers in the analog memory unit. Because this offset is constant, it does not add any linearity error. For applications that require less offset between channels, a future revision of this architecture should address this issue. The offset could be reduced by using offset cancelation techniques in the op-amps within the analog memory unit. A ping-pong architecture could be used to achieve a low offset [25].

The INL error is worse than expected for 12-bit linearity. It is apparent in Figure 5.7 that the most significant shifts in the INL plot occur when the input code is close to powers of two. There is a jump in the INL error that occurs near input code 2048. Two other significant shifts in the INL plot are seen near codes 1024 and 3072. These results suggest that much of the INL error is due to the Gray code counter. It was not feasible to simulate the INL of the DAC due to time limitations, but the simulated skew of the Gray code counter was not enough to cause the observed integral nonlinearity. A worse than expected skew in the counter could cause this problem. Because the power consumption of the counter is a small proportion of the total power, a replacement of the low power counter with a faster but less power efficient counter should be considered in future revisions of this architecture to improve the DAC's performance.

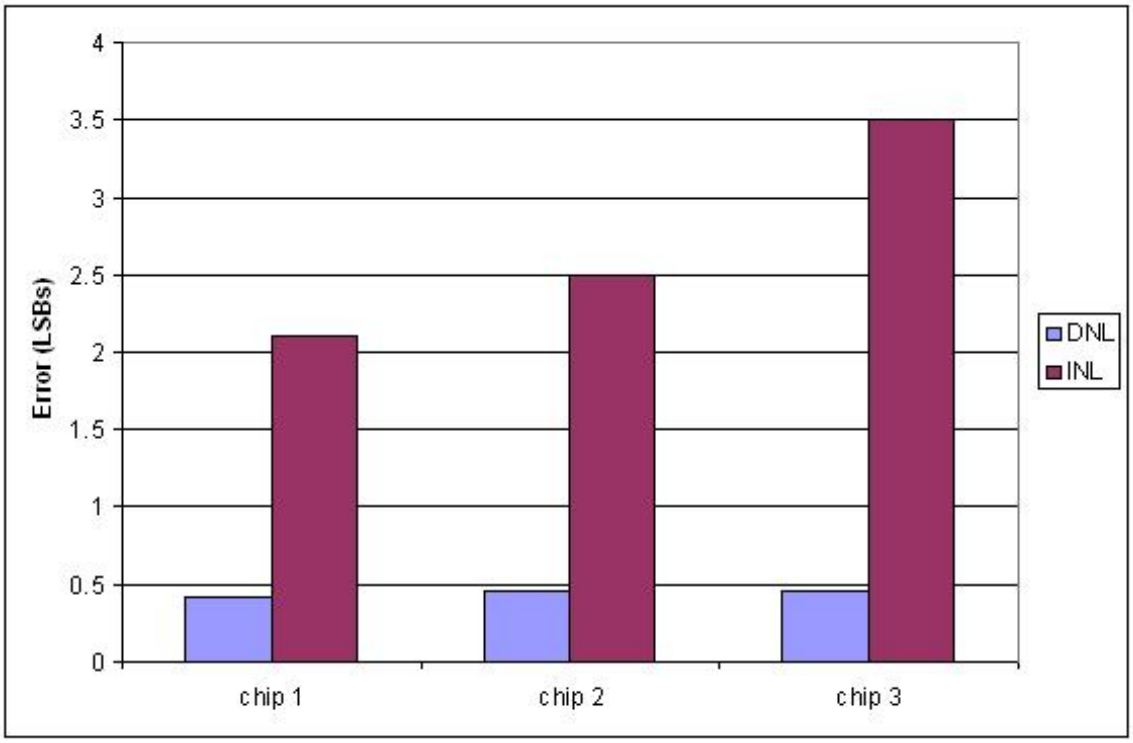

Figure 5.8: Chip-to-Chip Variation in Linearity Error

An alternative method for measuring the DNL and INL of the DAC is to step the DAC's input through each code and measure the analog output at each step. To reduce noise in the measurement, 1000 samples are taken at each input code and averaged. The INL error is found by calculating the difference (in LSBs) between each averaged data point and the best fit line through all of the data points. The DNL error is found by calculating the difference between adjacent data points (in LSBs). The DNL result is shown in Figure 5.9. The DNL error is contained to within +/- 0.8 LSBs. The INL error is shown in Figure 5.10. The INL error is also contained to within +/- 0.8 LSBs. The DNL results are worse than the results achieved using the sine wave histogram method. This alternative measurement is a more direct measurement of the DNL, so these results are probably more accurate than the sine wave method. The INL results are better than the sine wave histogram method. This step testing method is not sensitive to the ideal sine wave amplitude. For the sine wave histogram measurements, it appears that some of the INL error is due to sensitivity to the ideal sine wave amplitude used for calculating the error. The results in Figure 5.10 still show jumps in the INL error at the same locations that were seen in the sine wave measurements. These results that were acquired using the step method also suggest that improvements should be made to the Gray code counter.

In addition to the Gray code counter, there are other possible sources of error that could be reduced with layout techniques. Noise coupling from the digital section of the chip to the analog circuits could be introducing errors. Care was taken to separate the analog sections from the digital sections, but due to area constraints there are some analog signals that run close to the digital section of the chip. A few of the analog signals within the AMU circuit run close to the counter and control

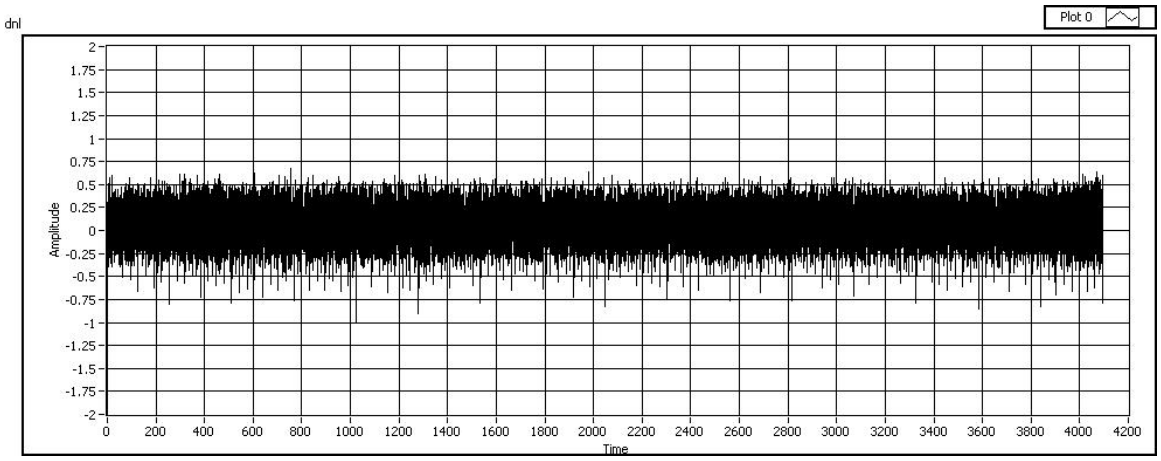

Figure 5.9: Differential Nonlinearity Error Measured with Step Test

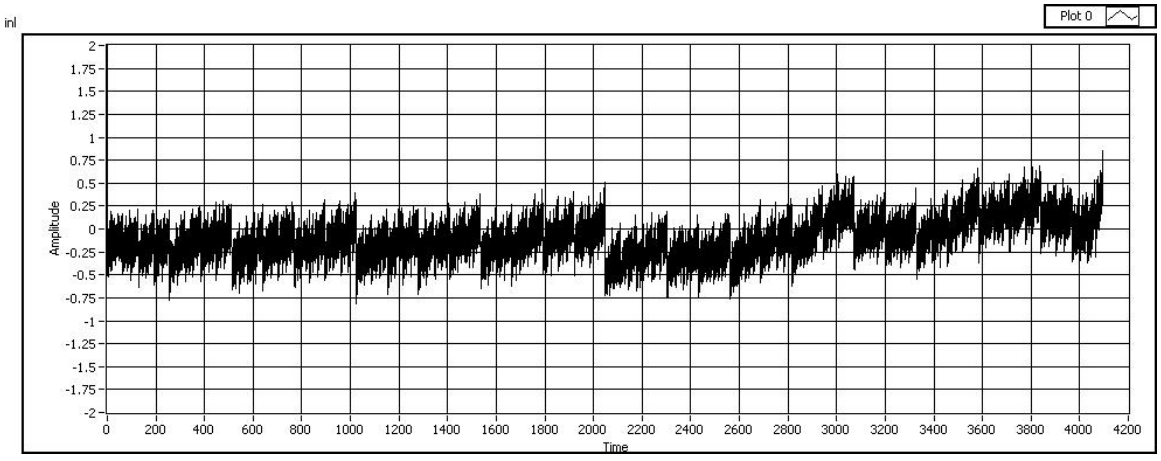

Figure 5.10: Integral Nonlinearity Error Measured with Step Test

logic. Better separation between the analog circuits and digital circuits might reduce any error that is caused by noise coupling.

5.4 Temperature Testing

The DNL and INL errors for the DAC were measured over temperature from -55 °C to 125 °C. The results of these tests are shown in Figures 5.11 - 5.15. These results show that there is a slight increase in DNL error at 75 °C and higher temperatures. At 125 °C, the maximum DNL error is slightly higher than 0.6 LSBs. The INL error is worst at -55 °C.

The temperature measurements were taken using the sine wave histogram method for measuring DNL and INL. As discussed in the previous section, INL measurements made using this method are sensitive to the ideal sine wave amplitude used to calculate the error. However, this sensitivity does not explain the patterns shown over temperature. It appears that the ramp generator is beginning to saturate near the higher end of the output range at low temperatures, but simulations of the ramp generator over temperature did not predict any significant degradation of the linearity at lower temperatures. Simulations of the ramp generator's output impedance over frequency were presented in chapter 4. The simulation results indicated that the ramp generator's output impedance is sufficient for 12-bit linearity over temperature. The measurement results at higher temperatures do not show the apparent saturation of the ramp generator near the higher end of the output range, but they do show integral nonlinearity error that is higher than expected from simulations. The simulations of the ramp generator do predict a lower output impedance at higher temperature. The

ramp generator's linearity is sensitive to changes in the ramp bias current, because the input bias current sets the common mode input at the positive terminal of the op-amp in the ramp generator. It is possible that this bias current is changing over temperature, because the ramp generator is biased using an external resistor on the board, and the temperature coefficient of this resistor may be different from that of the on chip resistors in the ramp generator. If a change in the ramp generator's bias current over temperature is occurring, it could explain the observed nonlinearity at lower and higher temperatures. An alternate ramp generator that is less sensitive to changes in bias current is discussed in the future work section of the next chapter.

The polystyrene moisture barrier crystallizes, cracks, and begins to flake off at high temperatures. Because of this, the moisture barrier was removed using a Methyl Ethyl Ketone solvent and a high impedance was achieved by disconnecting the ramp generator connection from the board. This was done by bending the pin up before placing the chip in the dip socket. The ramp capacitor was then soldered directly to the pin without any connection on the PCB. This prevented any impedance limitations on the surface of the PCB to cause leakage from that node. The temperature tests in this section were done after making this change to the board. DNL and INL results after this change were similar to the results achieved after the board clean and bake.

5.5 Dynamic Test Results

The output spectrum of the ADC was measured for a 100 Hz digital input sine wave sampled at 1 kHz. The spectrum is shown in Figure 5.16. The figure also shows

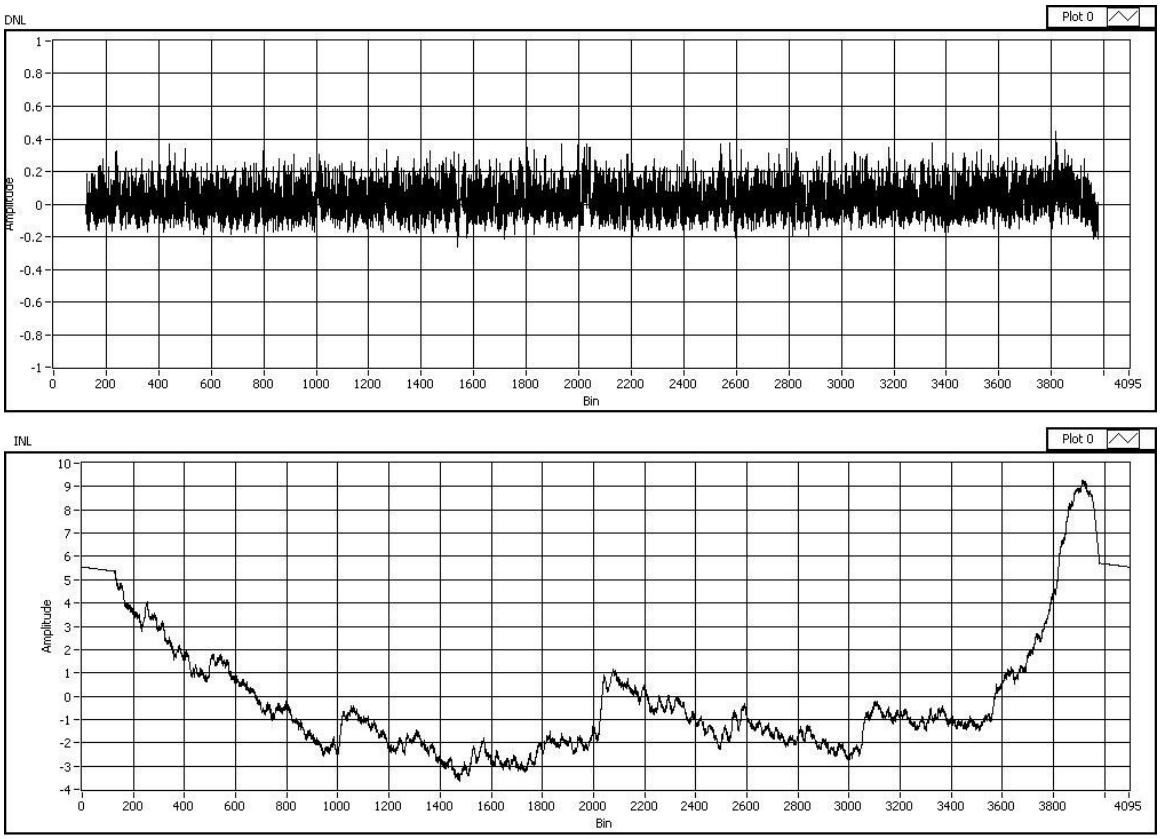

Figure 5.11: DNL and INL measurement results at -55 °C

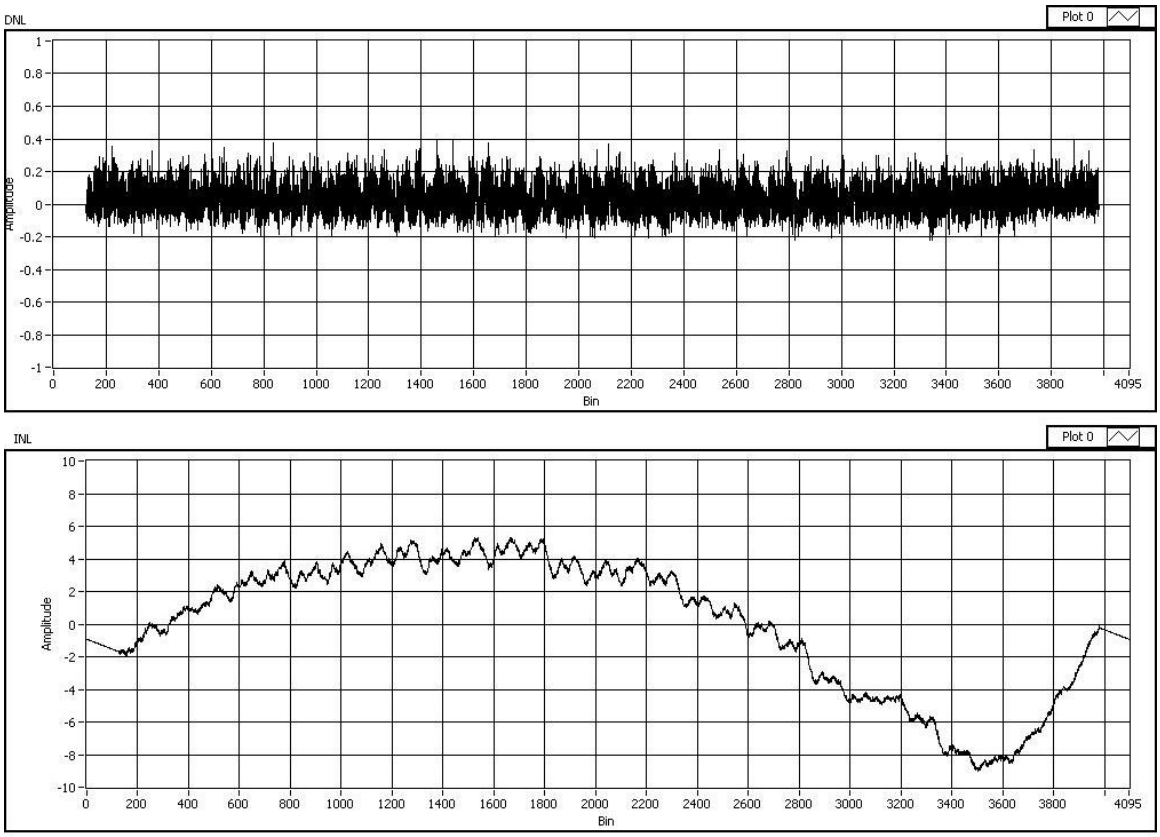

Figure 5.12: DNL and INL measurement results at 0 °C

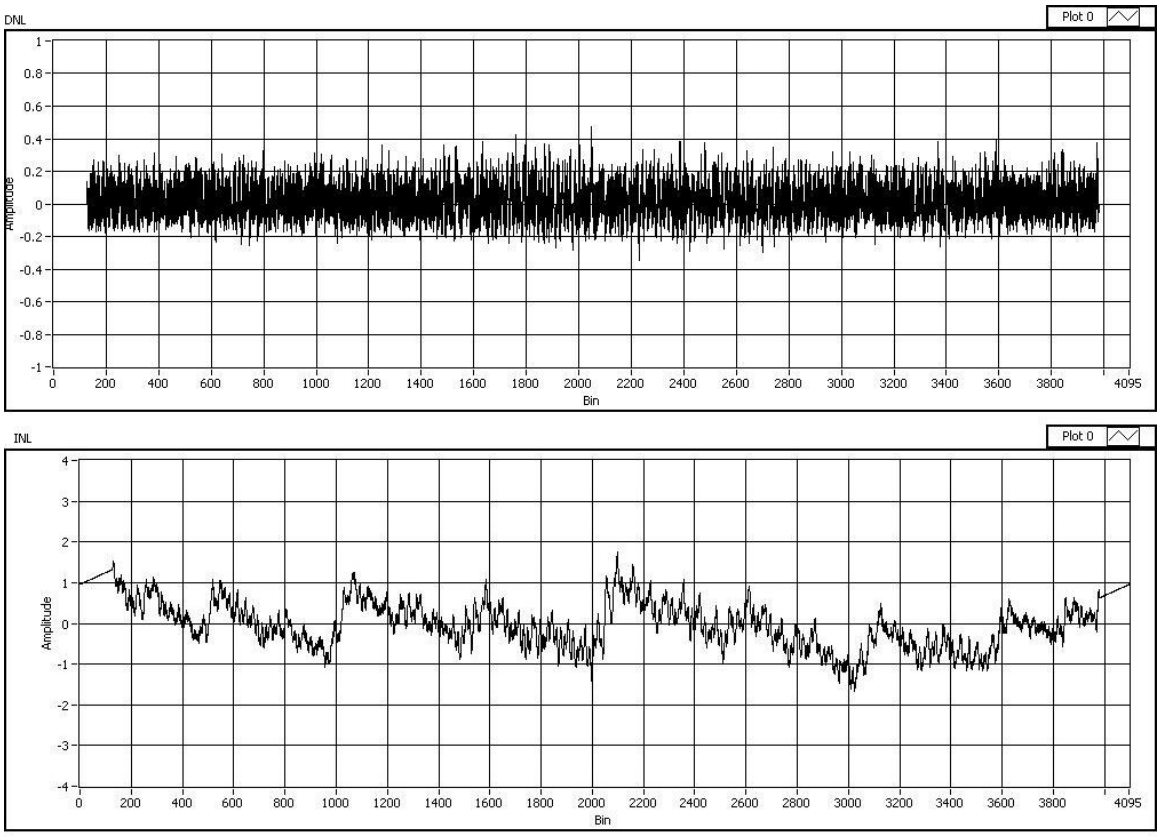

Figure 5.13: DNL and INL measurement results at room temperature (27 °C)

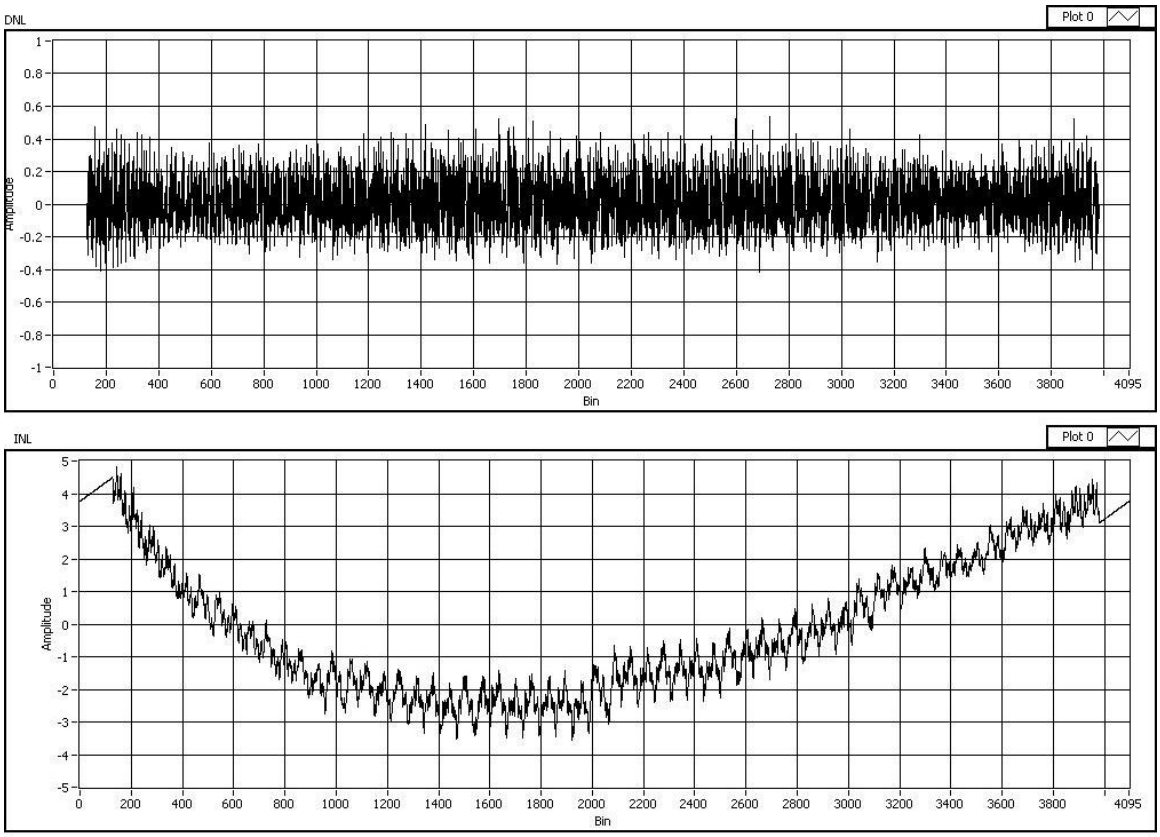

Figure 5.14: DNL and INL measurement results at 75 °C

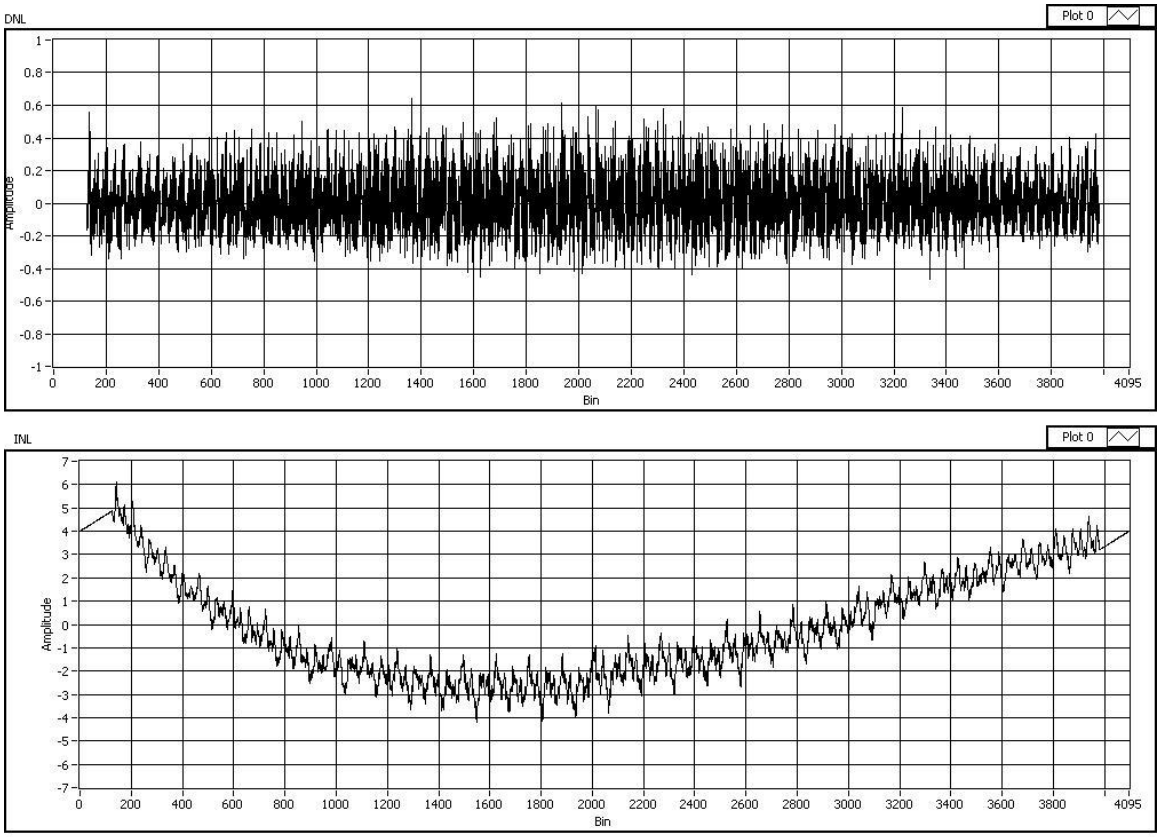

Figure 5.15: DNL and INL measurement results at 125 °C

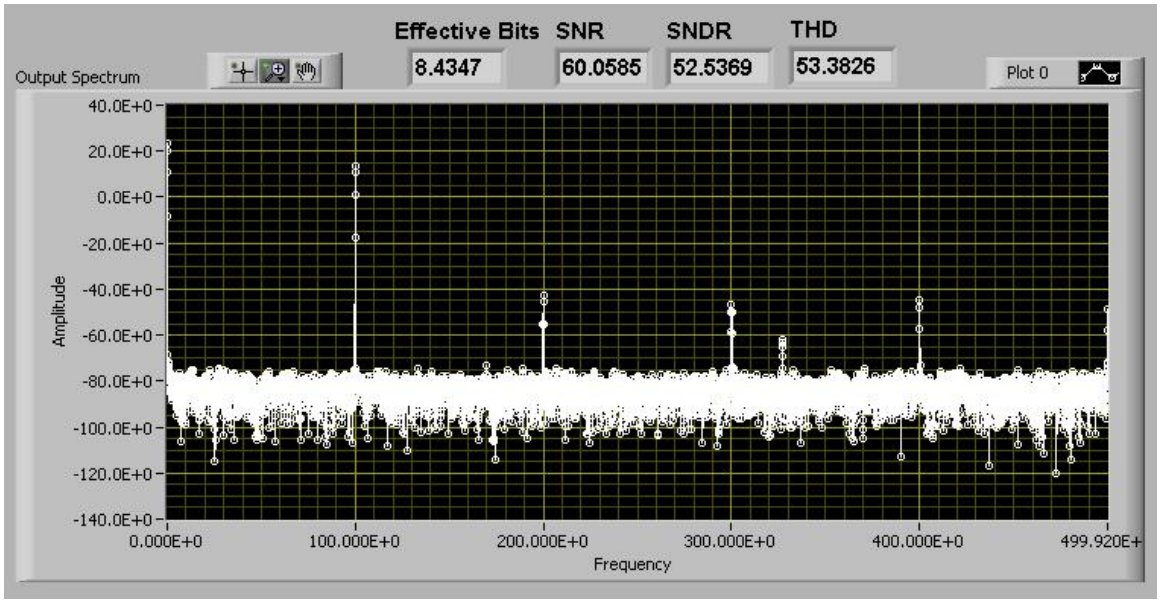

Figure 5.16: Dynamic Test Results (Measured)

the signal-to-noise ratio (SNR), the signal-to-noise-and-distortion ratio (SNDR), the total harmonic distortion (THD), and effective bits (ENOB). SNR represents the ratio of the signal power to noise power expressed in dB. THD represents the ratio of signal power to the power in the harmonics. SNDR represents the ratio of the signal power to the remaining power in the output spectrum (noise and distortion). These terms are calculated from the FFT results in LABVIEW using equations 5.4 - 5.7. S represents the signal power. D represents the distortion, or power in the harmonics. N represents the noise power.

$$SNR = \frac{S}{N} \tag{5.4}$$

$$THD = \frac{S}{D} \tag{5.5}$$

$$SNDR = \frac{S}{N + D} \tag{5.6}$$

$$ENOB = \frac{SNDR - 1.76}{6.02dB/bit} \tag{5.7}$$

The measured value of 60 dB for the SNR means that the noise taken in the measurement limits the linearity to 10 bits. This value could likely be increased with improvements in the test setup and chip layout. A six layer test board could provide more isolation between analog and digital signals by routing them on entirely separate

layers separated by power planes. Also, noise coupling from the digital circuits to the analog circuits could be reduced by more separation between the analog and digital circuits. The measured value for the THD was 53.38 dB. Given that the INL measurement showed linearity errors of 2 LSBs, it is expected that the THD would be less than 60 dB. If the theory that the low power Gray code counter is responsible for much of the INL error is correct, the THD should be improved by using a faster counter with less skew. With an improvement in the THD, the effective number of bits would be higher than the measured value of 8.43.

5.6 Step Response, Sampling Rate, and Power Supply Range Tests

Figure 5.17 shows the DAC's small signal step response. The large signal step response is shown below in Figure 5.18. These step response test results show that for a small or large change in the DAC's input code, the time required for the DAC to settle is much less than the conversion time. Simulation results also show that the DAC's output settles in much less than the conversion time both for small and large changes in the DAC's input code.

To test the DAC at different sampling rates, the slope of the ramp must be changed by either changing the ramp bias current or the ramp capacitor. Because the ramp generator was designed for a fixed bias current, it is not convenient to test the DAC at many different sampling rates. Tests at higher frequencies were performed by decreasing the external ramp capacitor to speed up the ramp rate, and by adjusting

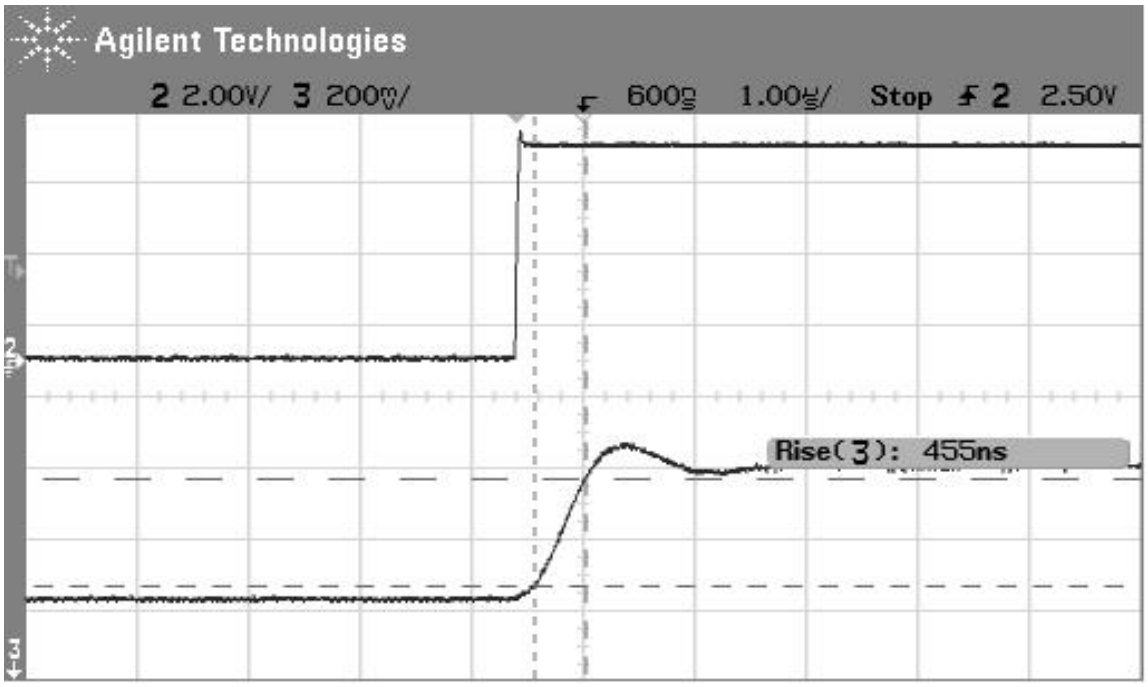

Figure 5.17: Small Signal Step Response (Measured)

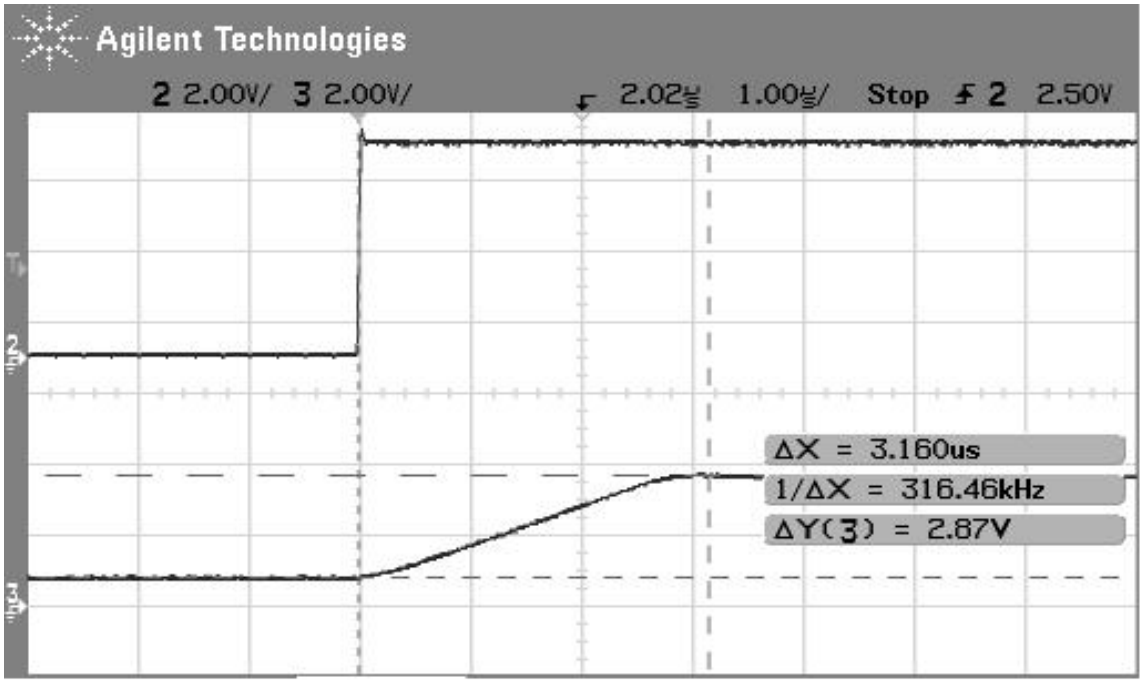

Figure 5.18: Large Signal Step Response (Measured)

the DAC clock. The measured DNL at a 4 kHz sampling rate was 0.5 LSBs, and the INL was 4 LSBs. At 5 kHz, the DNL was 0.95 LSBs and the INL was 6 LSBs. A faster Gray code counter should reduce the linearity error at higher frequencies.

Figure 5.19 below shows the linearity of the DAC vs. power supply voltage. The DAC operates with as much as a 6 % reduction in the power supply without a significant increase in non-linearity. This reduction in linearity with a 4.65 V power supply is due to output swing limitations of the op-amp in the ramp generator. There are two cascoded PMOS devices between the output and the power supply. The ramp voltage must swing from 0.5 V to 3.5 V. When the power supply is reduced, the two PMOS devices are pushed out of strong inversion saturation when the ramp voltage approaches 3.5 V. This reduces the gain of the op-amp and therefore introduces INL error. As discussed previously, the simulated linearity of the ramp generator does not account for the total INL error with a 5 V supply, but simulations do show reduced linearity of the ramp generator at reduced power supplies.

5.7 Comparison of Results with other DAC Architectures

To judge how well this DAC is suited for multi-channel applications compared to other DAC architectures, different figures of merit will be discussed here. A sample of DACs reported in literature were chosen for this comparison [8, 15, 18, 26–34]. To compare the area advantage of the DAC with other architectures, the number of input codes for each DAC (2^N) was divided by the reported area of the DAC scaled to a

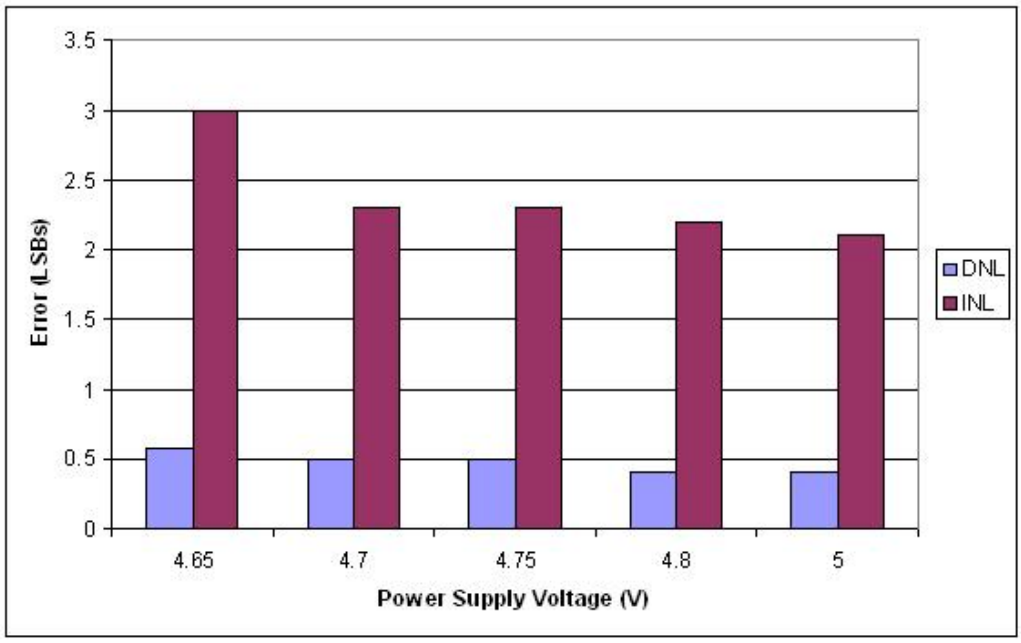

Figure 5.19: Linearity Error vs. Power Supply Voltage (Measured)

1 μm process. For the 28-channel DAC reported by Imamura and Kuwahara, the per-channel area is used. For fair comparison, the area used for the multi-channel DAC in this work is an estimate of the per-channel area required for a 28 channel version of the DAC architecture with the ramp generator on chip. This figure of merit is presented in Figure 5.20.

Figure 5.20 shows that the DAC architecture would be advantageous compared to other architectures for higher resolution multi-channel applications that benefit from low area. When power consumption and speed are included in the comparison, the DAC architecture is less competitive (see Figure 5.21). The energy per conversion of the multi-channel DAC prototype is not very competitive, but this could be improved by replacing the low power Gray code counter. The low power Gray code counter was used because it was sufficient for a 1 kSps application. If a faster counter is used,

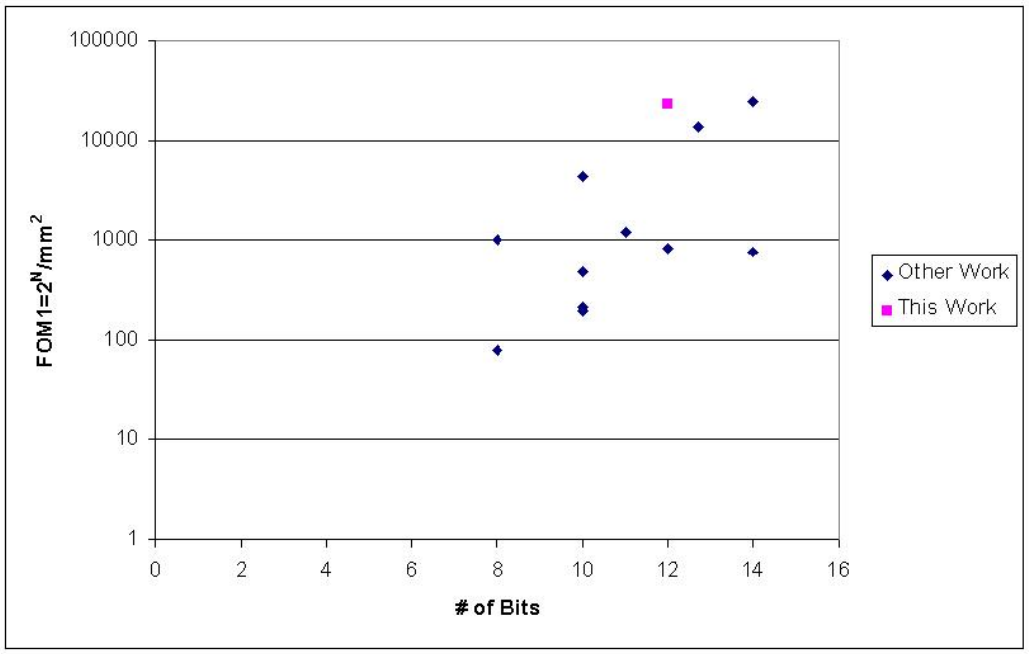

Figure 5.20: Figure of merit: Input codes per mm^2

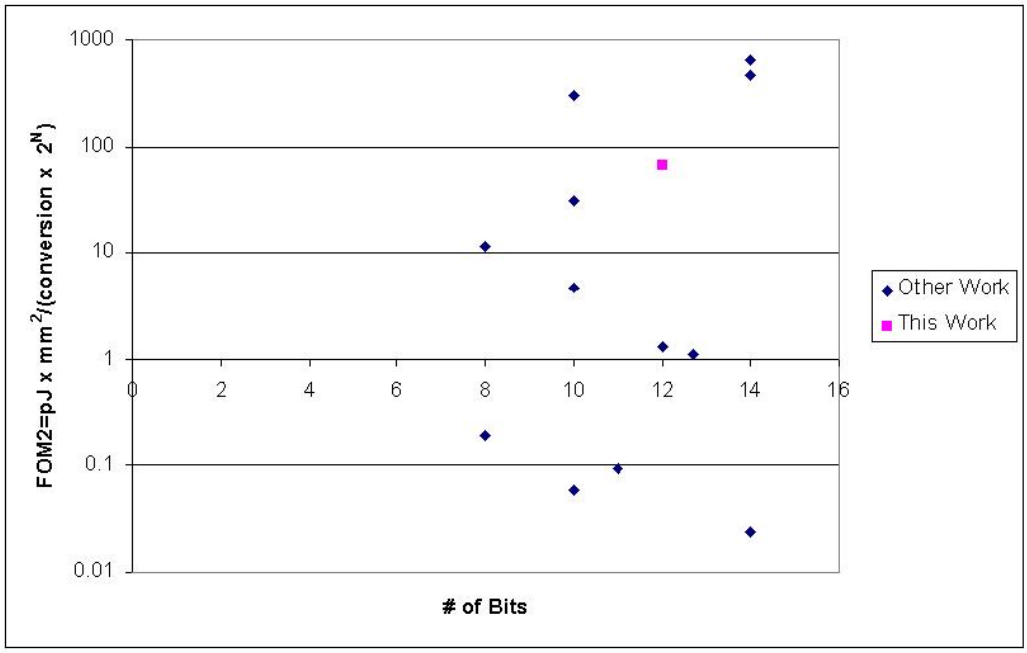

Figure 5.21: Figure of merit including power consumption and speed

the architecture is theoretically capable of much faster conversion rates than 1 kSps. This speed improvement would come at the cost of increased power dissipation from the counter. The ramp generator and AMU circuits are capable of operating at much higher frequencies without an increase in power consumption. Given that the ramp generator and AMU circuits dominate the power consumption, the increase in power by upgrading the Gray code counter would reduce the energy per conversion of the DAC significantly because the increase in power consumption would be much less than the increase in conversion rate.

A third figure of merit is shown in 5.22. This figure of merit compares the area and power consumption of the multi-channel DAC with the other DACs. This DAC was intended for low power and low speed applications. When speed is not taken into

consideration, this DAC clearly excels. Table 5.1 shows a brief summary of the DAC testing results.

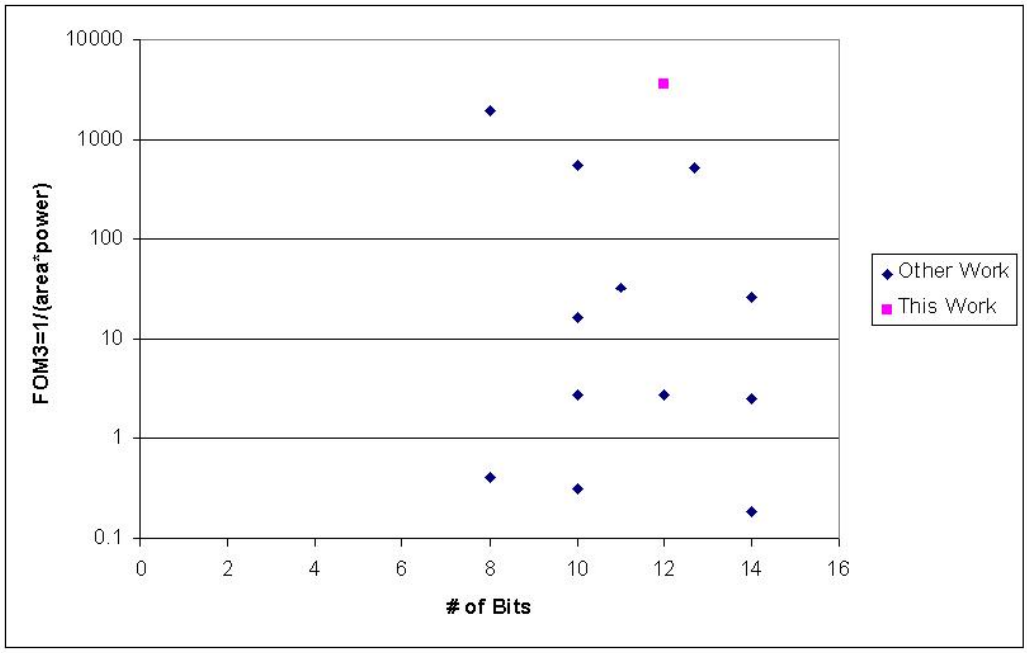

Figure 5.22: Figure of merit area and power consumption

Table 5.1: Summary of DAC results

process	0.5 μ
area	1140 μm by 1130 μm
power	1.98 mW
fs	1 kHz
max DNL error at room temp	+/- 0.4 LSBs
max INL error at room temp	+/- 2 LSBs
SNR	60 dB
THD	53.4 dB
SNDR	52.5 dB
ENOB	8.44

Chapter 6

Future Work and Conclusions

6.1 Recommendations for Improving Performance

As discussed in the previous chapter, an upgrade of the Gray code counter is recommended for reducing the DAC nonlinearity, distortion, and total energy per conversion. There is also room for improvement in the power efficiency of the ramp generator and AMU circuits.

Future revisions of this DAC architecture should consider alternate topologies for the ramp generator circuit. The ramp generator used in this work is sensitive to the impedance at the output of the ramp generator. Charge leakage from this node can cause nonlinearity error. An op-amp based integrator with capacitive feedback should be considered as an alternative (see Figure 6.1 below). The op-amp in this circuit would reduce the effect of loading on the ramp signal. Also, the voltage across the

current source would remain constant, thus eliminating the need for a high output impedance current source [35].

In the prototype DAC presented in this work, the DAC does not function correctly with a zero code input. This problem is caused by a timing error in the AMU control logic. When the input code to the DAC is zero, the COUT signal from the digital comparator arrives to the flip-flop before the clock signal that indicates a new conversion has started. Because of this timing error, the Φ3 and Φ4 control signals do not go high. This prevents the AMU capacitors from sampling the ramp voltage. A simple fix for this problem is shown below in Figure 6.2. Simulations have verified that the added delay cell (shown in red) fixes the timing error. An alternative fix would be to latch the COUT signal with a flip-flop clocked by the output of the clock generator circuit.

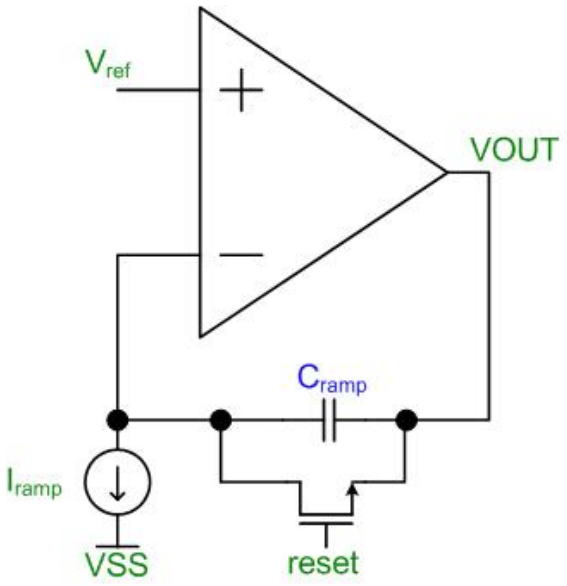

Figure 6.1: Alternate ramp generator possibility

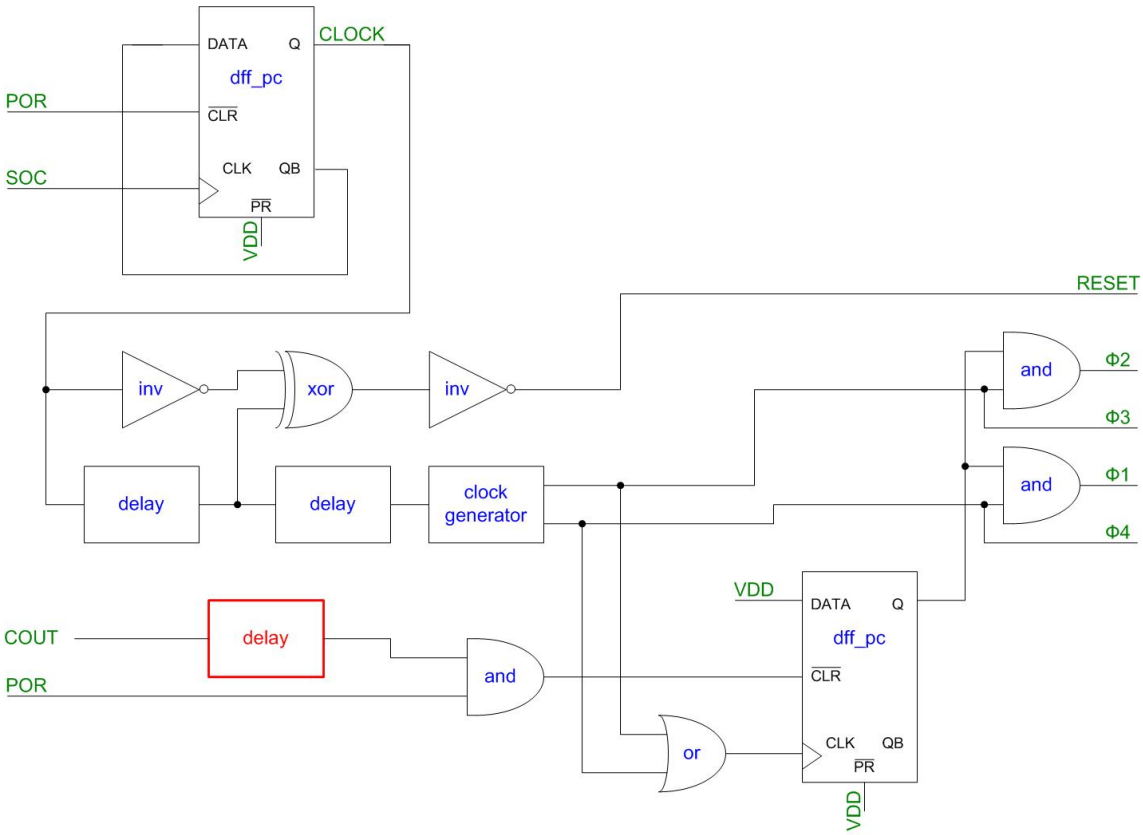

Figure 6.2: AMU control circuit fix for zero code input

6.2 Hardware Sharing with Wilkinson ADC

As mentioned in the introduction to this dissertation, the single-ramp DAC architecture shares some features with the Wilkinson ADC architecture. An interesting continuation of this work would be to share hardware between the DAC and a Wilkinson ADC. The ramp generator and counter can be shared between the ADC and DAC, as shown in Figure 6.3. The only additional hardware required for the DAC is the AMU circuit and a small amount of digital logic.

6.3 Improvement in chip layout and PCB design

Improvements in the layout and PCB design can possibly improve the DAC performance in future revisions. Layout area for the prototype DAC presented in this work was limited. The layout floorplan could be modified to increase isolation between analog and digital circuits if more flexibility were allowed in the aspect ratio of the layout. In the layout of the prototype DAC, some analog signals had to be routed close to digital circuits. Avoiding this in future revisions would reduce noise coupling from digital circuits to the analog circuits. More extensive use of guardrings can also help. A six layer PCB design would allow better isolation between the analog and digital signals.

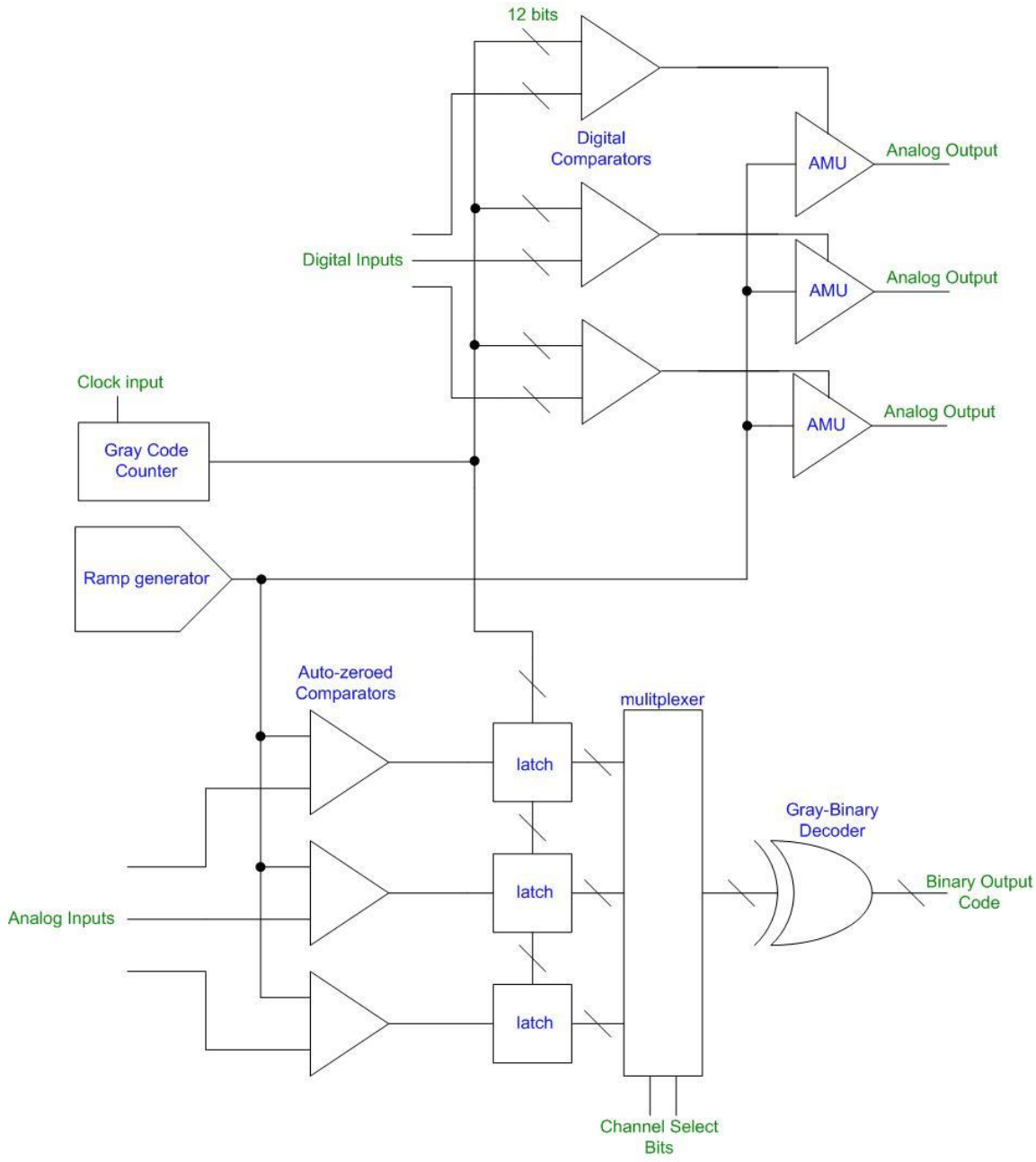

Figure 6.3: Hardware sharing between Wilkinson ADC and DAC

6.4 Conclusions

This research presents a new DAC architecture that allows hardware sharing between multiple channels. The DAC architecture allows Systems-on-Chip to have multiple analog outputs for stimulating transducers or motors. The architecture allows additional channels to be added with significantly less area and power penalties than a basic single-ramp architecture. This work also presents data from a single ramp DAC architecture, which is scarce in literature. From the measurement data taken in this work, it can be concluded that this architecture can be useful in lower speed multi-channel applications that require high linearity along with low area and power consumption.

Bibliography

Bibliography

[1] F. Maloberti, *Data Converters*. Springer, 2007.

[2] A. R. Hamade and E. Campbell *ISSCC Digital Tech. Papers*, pp. 154–155, 1976.

[3] A. R. Hamade and E. Campbell *IEEE Journal of Solid-State Circuits*, vol. 13, no. 6, pp. 785–791, 1978.

[4] P. Oborn and D. Comer *Proceedings of IEEE International ASIC Conference and Exhibit*, pp. 304–307, 1997.

[5] J. A. Schoeff *IEEE Journal of Solid-State Circuits*, vol. 14, no. 6, pp. 904–911, 1979.

[6] H. Post and K. Schoppe *IEEE Journal of Solid-State Circuits*, vol. 18, no. 6, pp. 297–301, 1983.

[7] D. Dooley *IEEE Journal of Solid-State Circuits*, vol. 8, no. 6, pp. 297–301, 1973.

[8] L. Wang, Y. Fukatsu, and K. Watanabe *IEEE Instrumentation and Measurement Technology Conference*, 2001.

[9] J. Cecil and W. Howard *International Solid States Circuits Conference*, pp. 52–53, 1971.

[10] J. W. Bruce, "Nyquist rate digital-to-analog converters," *IEEE Potentials*, pp. 24–28, August/September 2001.

[11] U. Moon, J. Silva, J. Steensgaard, and G. Temes *International Symposium on Circuits and Systems*, pp. 421–424, 2000.

[12] J. McCreary and P. Gray *International Solid States Circuits Conference*, pp. 38–40, 1975.

[13] M. Ericson, S. Frank, C. Britton, M. Emery, J. Sam, and A. Wintenberg *IEEE Nuclear Science Symposium*, pp. 671–674, 1997.

[14] J. Deveugele and M. Steyaert *IEEE Solid State Circuits Conference*, pp. 362–532, 2004.

[15] W. Mack, M. Horowitz, and R. Blauschild *IEEE Journal of Solid-State Circuits*, vol. 17, no. 6, 1982.

[16] E. Gat, R. Desai, R. Ivlev, J. Loch, and D. Miller *IEEE Transactions on Robotics and Automation*, vol. 10, no. 4, pp. 490–503, 1994.

[17] D. Pessen, *Industrial Automation: Circuit Design and Components*. Wiley-IEEE, 1989.

[18] M. Imamura and K. Kuwahara *International Solid States Circuits Conference*, pp. 384–385, 1997.

[19] M. Imamura and K. Kuwahara *International Solid States Circuits Conference*, 1997. slides.

[20] R. Levinson, J. Caruso, and A. Tasdighi. U. S. Patent No. 5,294,927.

[21] S. Churchill, G. Shah, D. Webb, and B. Mandyam. U. S. Patent No. 6,995,701.

[22] O. Milgrome, S. Kleinfelder, and M. Levi *IEEE Transactions on Nuclear Science*, vol. 39, no. 4, 1992.

[23] W. Kester *EDN*, pp. 103–112, 1984.

[24] K. Lundberg, "Adc testing," 2002.

[25] I. Opris and G. Kovacs *IEEE Journal of Solid-State Circuits*, vol. 9, no. 31, pp. 1320–1324, 1996.

[26] K. Maio, M. Hotta, N. Yokozawa, M. Nagata, K. Kaneko, and T. Iwasaki *IEEE Journal of Solid-State Circuits*, vol. 16, no. 6, 1981.

[27] M. Borremans, A. V. den Bosch, M. Steyaert, and W. Sansen *IEEE Custom Integrated Circuits Conference*, pp. 157–160, 2001.

[28] T. Wu, C. Jih, J. Chen, and C. Wu *IEEE Journal of Solid-State Circuits*, vol. 30, no. 1, 1995.

[29] K. Ryu, K. S. Yoon, and H. K. Min *Midwest Symposium on Circuits and Systems*, pp. 538–541, 1998.

[30] P. Eloranta *International Symposium on Circuits and Systems*, pp. 109–112, 2006.

[31] O. Matsumoto, H. Harada, Y. Morimoto, T. Kumamoto, T. Miki, and M. Hatta *Asia and South Pacific Design Automation Conference*, pp. 809–814, 2005.

[32] H. Wang, H. Kao, and T. Lee *Asia-Pacific Conference on Advanced System Integrated Circuits*, pp. 102–105, 2004.

[33] K. Nojima, M. Yano, and M. Kawata *International Solid States Circuits Conference*, pp. 198–199, 1990.

[34] I. H. H. Jorgensen and S. A. Tunheim *International Symposium on Circuits and Systems*, pp. 425–428, 1996.

[35] M. S. Emery, S. S. Frank, J. C. L. Britton, A. L. Wintenburg, M. L. Simpson, M. N. Ericson, and G. R. Young *IEEE Transactions on Nuclear Science*, pp. 374–378, 1997.

Vita

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