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Driving and Protection of High Density High Temperature Power Module for Electric Vehicle Application

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To the Graduate Council:

I am submitting herewith a dissertation written by Zhiqiang Wang entitled "Driving and Protection of High Density High Temperature Power Module for Electric Vehicle Application." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

Leon M. Tolbert, Major Professor

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Driving and Protection of High Density High Temperature Power Module for Electric Vehicle Application

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Abstract

There has been an increasing trend for the commercialization of electric vehicles (EVs) to reduce greenhouse gas emissions and dependence on petroleum. However, a key technical barrier to their wide application is the development of high power density electric drive systems due to limited space within EVs. High temperature environment inherent in EVs further introduces a new level of complexity. Under high power density and high temperature operation, system reliability and safety also become important.

This dissertation deals with the development of advanced driving and protection technologies for high temperature high density power module capable of operating under the harsh environment of electric vehicles, while ensuring system reliability and safety under short circuit conditions. Several related research topics will be discussed in this dissertation.

First, an active gate driver (AGD) for IGBT modules is proposed to improve their overall switching performance. The proposed one has the capability of reducing the switching loss, delay time, and Miller plateau duration during turn-on and turn-off transient without sacrificing current and voltage stress.

Second, a board-level integrated silicon carbide (SiC) MOSFET power module is developed for high temperature and high power density application. Specifically, a silicon-on-insulator (SOI) based gate driver board is designed and fabricated through chip-on-board (COB) technique. Also, a 1200 V / 100 A SiC MOSFET phase-leg power module is developed utilizing high temperature packaging technologies.

Third, a comprehensive short circuit ruggedness evaluation and numerical investigation of up-to-date commercial silicon carbide (SiC) MOSFETs is presented. The short circuit capability of three types of commercial 1200 V SiC MOSFETs is tested under various conditions. The experimental short circuit behaviors are compared and analyzed through numerical thermal dynamic simulation.

Finally, according to the short circuit ruggedness evaluation results, three short circuit protection methods are proposed to improve the reliability and overall cost of the SiC MOSFET based converter. A comparison is made in terms of fault response time, temperature dependent characteristics, and applications to help designers select a proper protection method.

Table of Contents

List of Tables

List of Figures

1 Introduction

This chapter starts with the introduction of the background of this research, driving and protection of high density high temperature power module for electric vehicle application. Then, the research objectives, approaches, and the organization of this dissertation are presented.

1.1 Background and Motivation

Petroleum is the largest energy source in the Unites States (U.S.), and it contributes to around 32.5% of total U.S. greenhouse gas emissions in 2010 [1]. In the consumption of petroleum, transportation accounts for 70% of U.S. petroleum consumption, with a dominant part in light vehicles, as shown in Figure 1-1 [2]. In order to reduce greenhouse gas emissions and dependence on petroleum, there has been an increasing trend for the commercialization of electric vehicles (EVs). According to the recent report from International Energy Agency (IEA), the global EVs sold more than doubled from 45,000 in 2011 to 113,000 in 2012 [3].

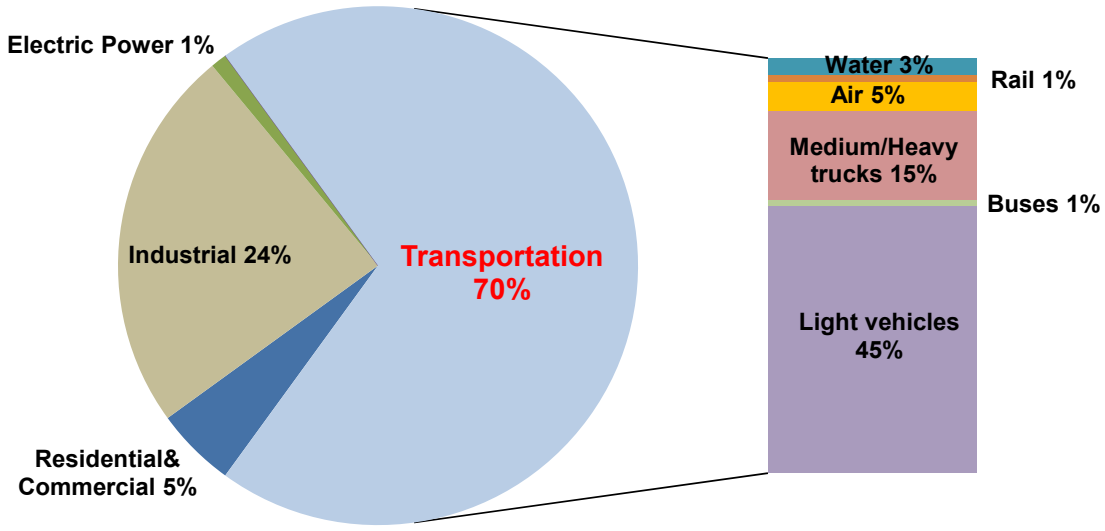


Figure 1-1. U.S. oil consumption in 2010.

Although EVs possess many advantages, a number of key issues in electric traction drive systems must be overcome, such as cost, volume and weight, efficiency, and reliability. The U.S. Department of Energy (DOE) technical targets for electric traction drive system are shown in Figure 1-2 [4], where the left table lists the targets at system level and the right part indicates an approximate distribution between electric motors and power electronics. The on-the-road technology status presented in [5] identifies the gaps between the current status and the targets. As reported, the key reason for the gaps is that the electric machine and drive electronics are packaged separately.

Electric Traction Drive Systems (ETDS)

Impact	Reduce Cost	Reduce Weight	Reduce Volume	Reduce Energy Storage Requirements
Year	Cost ($/kW)	Specific Power (kW/kg)	Power Density (kW/L)	Efficiency (%)
2015	12	1.2	3.5	>93
2020	8	1.4	4.0	>94

Power Electronics (PE)

($/kW)	(kW/kg)	(kW/L)
5	12	12
3.3	14.1	13.4

Electric Motors (EM)

($/kW)	(kW/kg)	(kW/L)
7	1.3	5
4.7	1.6	5.7

Figure 1-2. Technical targets for the electric traction drive systems [4].

The most common on-the-road technology is to integrate all the power electronic converters (including bi-directional DC/DC converter, three-phase inverter, on-board battery charger, etc.) in a central box. This kind of power architecture is simple, while the expensive and bulky housing is difficult to be integrated in the engine compartment of existing vehicles. Therefore, the power electronic converters are not able to share the 105 ˚C engine coolant, and usually a separate 65 ˚C liquid cooling system is required to remove the heat generated by the electric traction drive system. Another disadvantage is that a lot of "overhead" items (e.g., shielded high-voltage connectors and cables) are necessary to transfer the power from the central box to various loads (motor, battery, ancillary loads, etc.), which contributes heavily to the overall volume, weight and cost.

An alternative solution for the integration of electric traction drive systems is the so called "site-of-action integration" [6]. Each power electronic converter is locally attached to the specific load it operates, and thus the interconnection cables can be greatly reduced. However, significant challenges originating from both the limitations on available installation space and harsh operating environment should be addressed. Continued advancement in power electronic components and packaging technologies, including the development of high power density semiconductor modules, will help to meet these challenges [4]. The system-level benefits by developing high density and high temperature power module is shown in Figure 1-3.

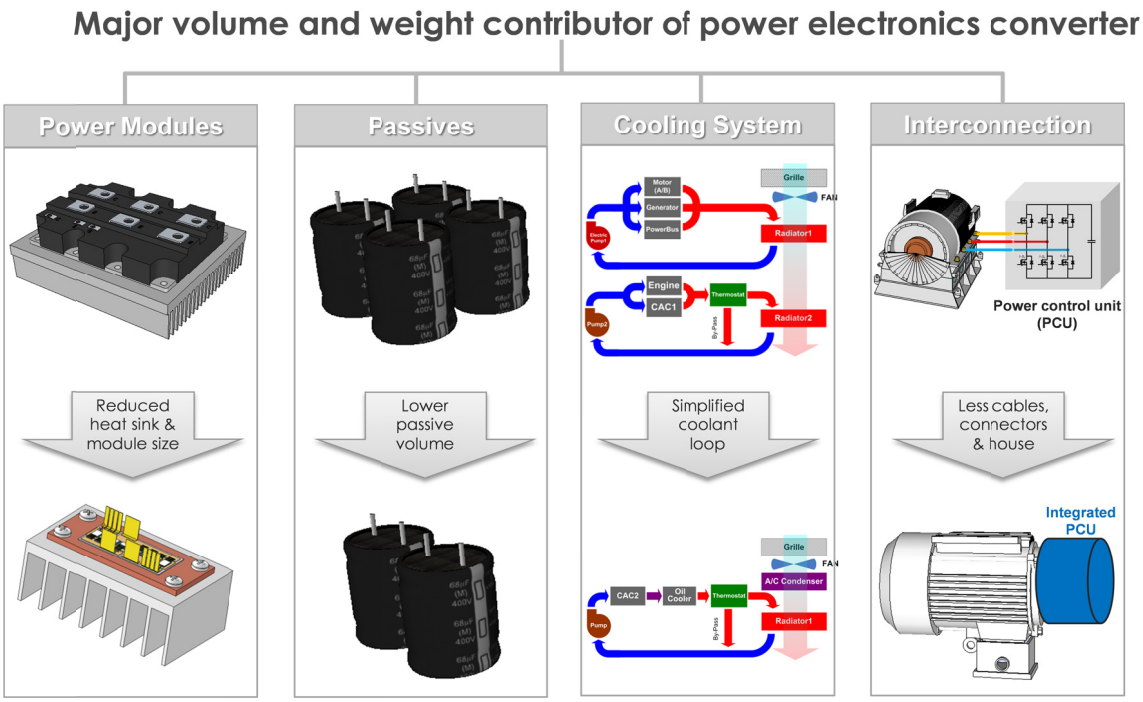


Figure 1-3. System-level benefits by developing high density and high temperature power module.

The high temperature environment inherent in electric vehicles introduce a new level of complexity in the design of the electric traction drive system. Reference [7] recently published a summary of automotive high temperature electronics requirements that is shown in Table 1-1. In addition, Figure 1-4 shows temperatures and related automotive electronic systems [8].

Table 1-1. Mechatronic maximum temperature ranges

On-Engine	150-200 °C
In-Transmission	150-200 °C
On Wheel-ABS sensors	150-250 °C
Cylinder pressure	200-300 °C
Exhaust sensing	Up to 850 °C, ambient 300 °C

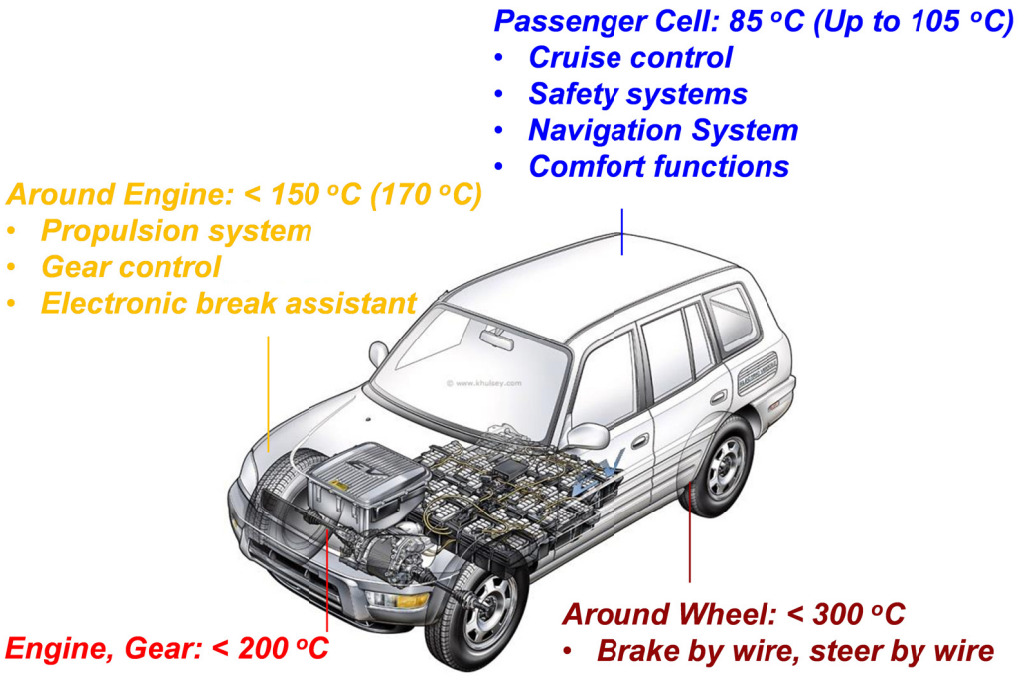


Figure 1-4. Ambient temperatures for automotive electronics applications.

In automotive electronics industry, electronics operating at 125 °C or above are considered as high temperature electronics. However, many of the automotive electronics components shown in Figure 1-4 have ambient temperature conditions above 150 °C. The development of high temperature capable power semiconductor modules and related control electronics will not only allow reliable operation under harsh environment, but also a significant increase in power density and reduced cooling.

On the other hand, while achieving higher power density (due to limited space and carrier capability) and high temperature electrical design (due to inherent harsh environment), the ability to guarantee the reliability and safety of power modules becomes critical [4]. One of the key reliability issues is the short circuit capability and protection of power semiconductor devices.

According to the classic transient thermal model, the short circuit capability of a power device can be expressed as a function of DC bus voltage (V_{dc}) and saturation current / power density (J_{sat}) [9], as shown in (1-1), where R_{th} and C_{th} are the thermal resistance and capacitance from junction to case, T_{jcrit} and T_c are the critical temperature and case temperature, and t_{sc} is the short circuit withstand time.

$$t_{sc} = \frac{R_{th}C_{th}}{ln\left(1 - \frac{1}{R_{th}} \cdot \frac{T_{jcrit} - T_c}{V_{dc} \cdot J_{sat}}\right)} \qquad (1-1)$$

This equation indicates that under a given DC bus voltage and critical temperature point the short circuit capability will be reduced if the saturation current density or operating temperature is increased. The tradeoff between the high power density high temperature and high reliability needs to be carefully considered for a power module. Moreover, a fast short circuit / overcurrent protection scheme needs to be equipped for a power module.

1.2 Research Objectives and Approaches

The objective of this research is to develop advanced driving and protection technologies for high temperature high density power module that is capable of operating under the harsh environment of electric vehicles, while ensuring system reliability and safety under short circuit conditions.

Corresponding to the challenges discussed in section 1.1, the research approaches are listed as follows.

(1) To adaptively reduce the switching energy loss of IGBT power modules, a novel *di/dt* feedback based active gate driver is proposed, which can reduce the turn-on and turn-off energy loss under different operating conditions. Moreover, it shares the same isolated power supply with the push-pull buffer, and high bandwidth detection and regulation circuits (e.g. current/voltage sensors, operational amplifier, etc.) are avoided, which is beneficial to the overall reliability and potential integration into a gate drive chip.

(2) To thoroughly exploit the benefits of SiC devices under high temperature environment, a SiC MOSFET and SOI gate drive based board-level integrated power module is built, with the goal of high temperature capability (up to 225 °C for power module, 200 °C for SOI gate driver), high frequency capability (up to 100 kHz), high sourcing and sinking current capability (up to 4 A for each gate driver channel), and low volume / size. In addition, a thermo-sensitive electrical parameter (TSEP) is proposed for the junction temperature measurement.

(3) To identify the key limiting factors, the short circuit capability of three types of commercial 1200 V SiC MOSFETs is evaluated under various case temperatures (from 25 °C to 200 °C), DC bus voltage levels (from 400 V to 750 V), and fault types (hard switching fault and fault under load). The associated failure mechanism has also been analyzed and compared through electro-thermal model and leakage current model.

(4) Based on the short circuit capability evaluation, the protection requirement is first proposed for SiC MOSFETs considering single-event, repetitive short circuit, and noise immunity. To help designers select a proper protection method for SiC power MOSFETs, two conventional candidates are implemented, i.e. solid-state circuit breaker (SSCB) and desaturation technique, and a novel protection scheme based on the fault current evaluation is also proposed, with special focus on the design optimization, potential issues of each method, and their performance comparison.

1.3 Dissertation Organization

This research report is organized as follows:

Chapter 2 gives a detailed literature review on the key enabling technologies to develop a high temperature and high density power module. Based on the literature review, the associated challenges in each focused area are pointed out and addressed.

Chapter 3 introduces an active gate driver (AGD) for IGBT modules to improve their switching performance under normal condition. The design consideration and circuit implementation of AGD are discussed. Experimental results are presented and compared with conventional gate driving strategy.

Chapter 4 presents the design, development, and testing of a high temperature silicon carbide MOSFET power module with an integrated silicon-on-insulator based gate drive. The junction temperature limitation of the developed power module is discussed as well.

Chapter 5 discusses the temperature dependent short circuit capability of three different types of commercial SiC MOSFETs. The short circuit behavior and associated failure mechanism are compared and analyzed through transient thermal simulation.

Chapter 6 evaluates the performance of three protection schemes under various conditions, considering variation of fault type, decoupling capacitance, protection circuit parameters, etc. A comparison is made to help designers select a proper protection method.

Chapter 7 summarizes the dissertation and its key contributions, and provides suggestions for additional research in the future.

2 Literature Review

The high density high temperature power module is a basic element for the development of high density electric drive system. As described in [10] and [11], the relationship of the key factors to achieve a high power density and high temperature power module is given in (2-1)

$$\frac{\$}{kW} \propto \frac{S_{die}}{P} = \frac{(1-\eta)}{T_j - T_a} \cdot R_{ja(sp)} \qquad (2-1)$$

where S_{die} is the power semiconductor device area; P is the total power handled by the corresponding power semiconductor devices; η is the efficiency; $R_{ja(sp)}$ is the specific thermal resistance; T_j and T_a represent the junction temperature and ambient temperature, respectively.

As indicated in (2-1), there are several ways to increase the power density of a power module. The first way is reducing the power loss or increasing the efficiency of a power module. The second way is increasing the operating junction temperature of power devices utilizing high temperature packaging technologies and control electronics. Another way is reducing the thermal resistance through advanced cooling and packaging design. This dissertation presents the application of the first two techniques for the development of high density power module: reducing the switching loss of IGBT power modules and developing a high temperature integrated SiC MOSFET power module.

On the other hand, the reliability of the power module is also critical. Usually, with the increase of current density/power density and operating temperature, the device life time will decrease. This dissertation will only focus on the short-term ruggedness, and the long-term reliability issues are out of the scope of this work. Since the voltage source converters are widely used in the EVs, the short circuit capability and protection of SiC MOSFETs are studied, aiming at improving the reliability and overall cost of the SiC MOSFET based converter in future electric vehicles.

This section will first review the state-of-the-art research activities in the above mentioned areas. The issues and unsolved problems of previous research efforts are examined, and then the challenges of this research are addressed.

2.1 IGBT Switching Loss Reduction under Hard Switching Condition

Electric vehicle applications have created new demands on IGBTs, e.g. higher current and voltage requirements, increased power density, faster switching speeds, higher efficiencies, reliable and fast protection [4]. Gate drivers serving as the interface between the IGBT power switches and the logic-level signals are expected to be optimized to meet these requirements. Conventional gate driver (CGD) circuits have employed fixed gate voltages and resistors, which are selected to minimize switching losses, suppress cross-talk and electromagnetic interference (EMI) noise, and also limit the switch stresses during switching transients and fault transients. However, these conflicting requirements, as shown in Figure 2-1, are difficult to be realized simultaneously in a CGD.

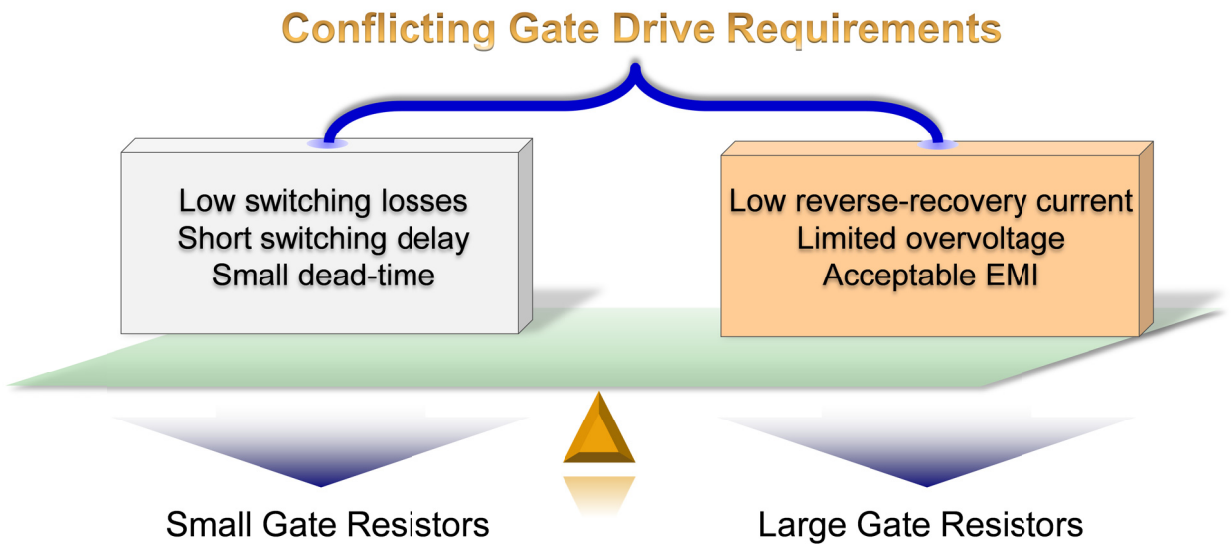


Figure 2-1. Conflicting requirements of conventional gate driver.

To deal with this issue, some research efforts have focused on reducing the switching losses by actively controlling gate drive signals. A gate drive circuit for IGBTs with a snubber circuit was proposed in [12]. This circuit utilizing the recycled energy from the snubber circuit to drive the IGBT cannot be directly applied to the hard-switched IGBTs. A multi-stage gate drive control concept has been proposed

in [13] and [14] to realize optimal turn-on and turn-off performance, as shown in Figure 2-2. The switching delay and switching losses are effectively reduced using large gate current, and the current rising/falling rate are limited using small gate current. The main issues of this method are control complexity for accurate detection of the instances for changes in driving modes, and poor adaptivity to various IGBTs with different thresholds, internal gate resistance and capacitance, etc., due to fixed control instants for certain switching stages.

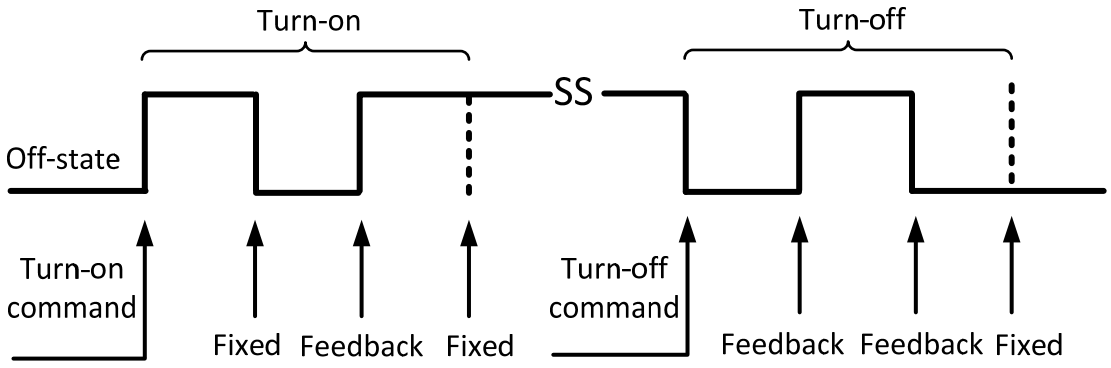
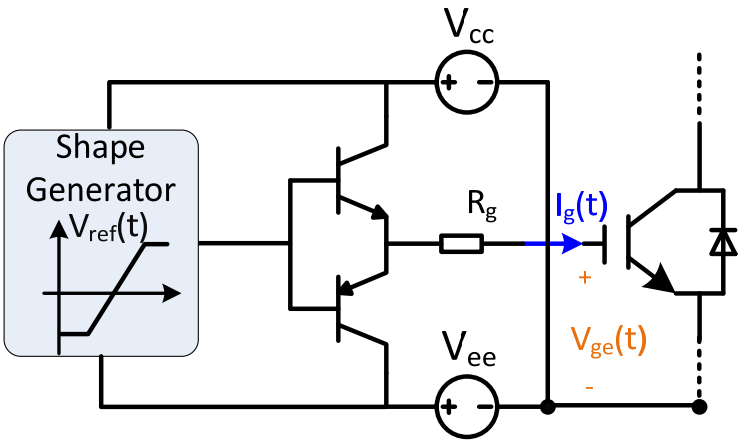
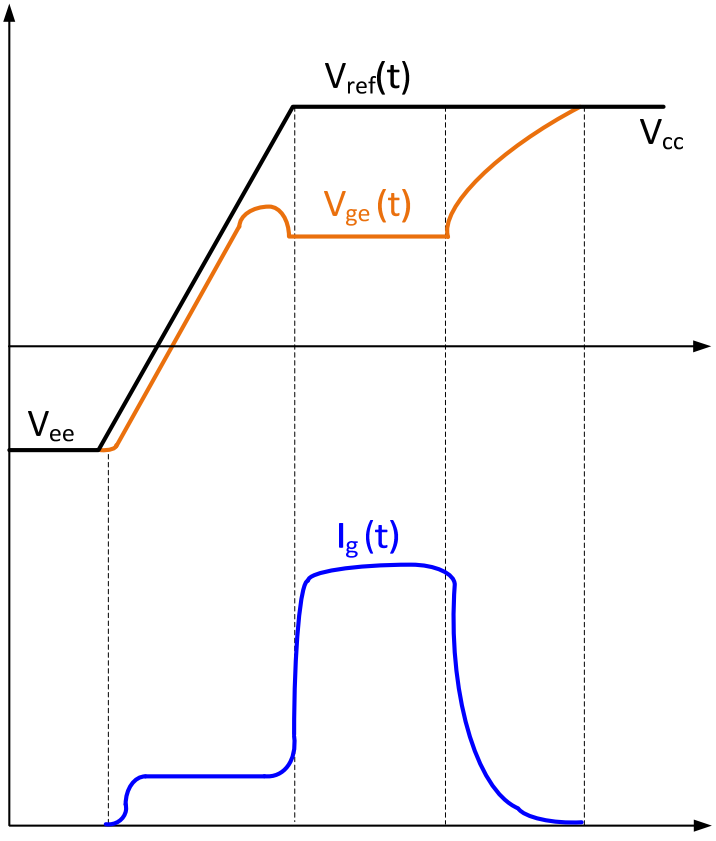


Figure 2-2. Multistage gate drive concept [13] [14].

In [15]–[17], a gate driver based on the Miller plateau detection by a phase-locked loop was analyzed and proposed. This technique is able to reduce switching loss by injecting an additional gate current, however, it can result in poor operation under transient load current conditions, and the inherent one switching period delay of the updated control instructions impairs the overall effectiveness. References [18], [19] have described a sensorless gate driver with feedforward control of the turn-on dynamics to reduce switching losses, as shown in Figure 2-3. Without direct feedback control, high bandwidth current/voltage sensing and high sensitivity to EMI noise can be avoided. The gate signal reference comes from a ramp shape generator whose rising slope is designed based on data sheet parameters. The turn-off performance keeps unchanged, and turn-on delay is still quite large due to the intentionally designed low slew rate of the gate references.



(a) Circuit diagram



(b) Operating principle

Figure 2-3. Feedforward active gate driver [18].

Recently, there have been several research efforts on improving the switching performances using digital approaches [20]–[22], as shown in Figure 2-4. These techniques could provide optimization among minimization of switching losses, reverse recovery current, and turn-off collector-emitter overvoltage by controlling the gate current in accordance with the desired switching operation. The main drawbacks associated with the digital method is large delay times of the D/A and A/D conversion in the signal paths, as well as considerable cost for high performance digital controllers.

Other references aiming at closed-loop/open-loop regulation of the collector current slope and collector-emitter voltage slope by means of either analog or digital approaches have been proposed and analyzed in [23]–[29]. Such techniques provide full *di/dt* or *dv/dt* control capability but sacrifice additional switching losses at switching transients.

Based on the literature survey, there is no active gate drive capable of adaptively reducing the switching energy loss of IGBTs by optimizing turn-on/off switching performance. Moreover, the existing switching energy loss reduction techniques are difficult to be integrated into a gate drive chip, which impedes the potential commercial application.

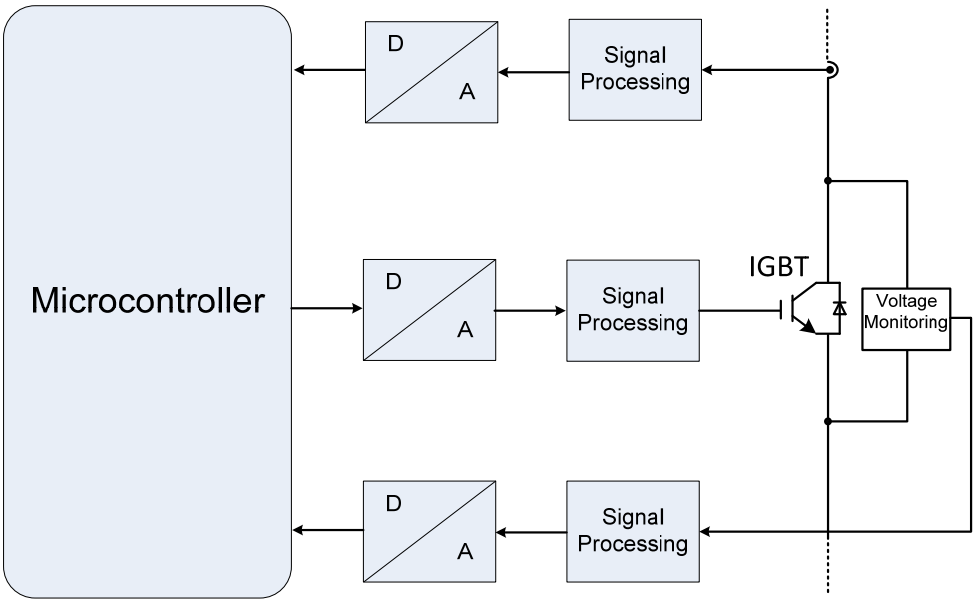


Figure 2-4. Digital control based active gate driver [20]-[22].

2.2 High Temperature Integrated Power Module

The trend of electrification in transportation applications, like electric vehicle, hybrid electric vehicle, and electric aircraft, brings severe challenges to future power electronic converters on both power devices and their gate drivers to operate in a high temperature environment with low weight and volume [30]–[33]. In terms of power devices, Si IGBTs are not suitable to be used in such conditions due to their limited junction temperature (<175 °C) and switching frequency (usually several tens of kilohertz). From the gate driver point of view, traditional silicon complementary metal oxide semiconductor (CMOS) based integrated circuit (IC) can only work reliably below 125 °C. The development of a high temperature integrated power module is quite challenging due to the lack of available materials and control electronics.

Featuring higher breakdown voltage, increased operating temperature, higher thermal conductivity, and lower switching and conduction loss, SiC devices are promising solutions to meet these challenges in transportation electrification [34]–[39]. Among the existing commercially available SiC devices, the SiC MOSFET is more preferable for widely used voltage-source converters because of its normally-off feature and compatible gate drive design with Si devices.

Low temperature SiC MOSFET power modules have recently become commercially available [40]–[42], as shown from Figure 2-5 to Figure 2-7. All of these modules are rated at 1200 V voltages and have a current rating of greater than 100 A. However, their junction temperatures, as indicated in the datasheets, are limited below 200 ^{o}C, due to the utilization of low temperature packaging materials.

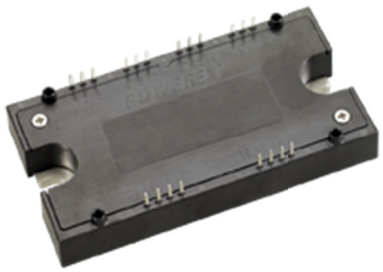


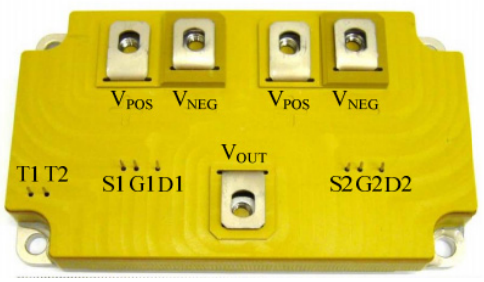
Figure 2-5. 1200 V / 100 A SiC MOSFET module [40].

Figure 2-6. 1200 V / 120 A SiC MOSFET module [41].

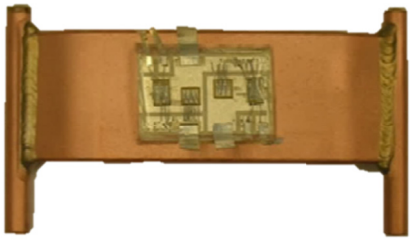
Figure 2-7. 1200 V / 120 A SiC MOSFET module [42].

High temperature SiC modules are still at the research stage, as reported in [43]–[50] (shown in Figure 2-8). In [43], a 1200 V, 60 A SiC MOSFET module with optimized internal layout for fast switching speed and low turn-off overvoltage is presented. The power module is successfully operated at 100 kHz, with a junction temperature of 200 °C. Two generations of SiC MOSFET-JBS diode based multi-chip power modules are reported in [44] and [45] for 200 °C and 20 kHz operations. Reference [46] presented a line of 250 °C half-/full-bridge SiC power modules, which can be configured as either a half or full bridge through external bussing, and constructed with SiC MOSFETs, JFETs, or BJTs. Moreover, there are also some research efforts on high temperature SiC JFET power modules based on different packaging techniques [47]–[50]. All of these power modules are able to operate at a high junction temperature above 200 °C employing high temperature packaging technologies. Their full potential,

however, cannot be achieved without the presence of a high temperature gate driver (placed as close to the power module as possible for reduced volume, parasitic effect, fast switching speed, etc.) to operate them in high temperature environments.

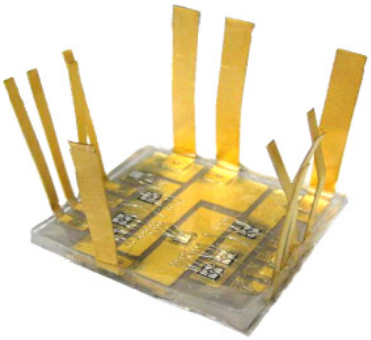


(a) SiC MOSFET module in [43]



(b) SiC MOSFET module in [89]

(c) SiC module in [46]



(d) SiC JFET module in [47]

Figure 2-8. High temperature SiC power modules.

In order to thoroughly exploit the high temperature capability of SiC power modules, researchers from Arkansas Power Electronics International Inc. (APEI) have focused on the integration of high temperature gate drive with a SiC power module. In [51], a high temperature gate driver, composed of high temperature passive components and discrete silicon-on-insulator (SOI) active devices, is integrated into the power package and is rated for an ambient temperature of 250 °C, as shown in Figure 2-9. A similar integration technique has been applied to the design and development of a 4 kW three phase high temperature SiC inverter [52]–[54], which demonstrates the feasibility of the concept. However, the major

limitation of this concept is that only the basic driving function, i.e. totem-pole output buffer, is implemented using discrete SOI active devices. Also, the overall size, volume, sourcing and sinking current capability (below 2 A), and switching frequency (targeted at 15 kHz) of the integrated power module are limited by the high temperature gate driver based on discrete passive and active devices.

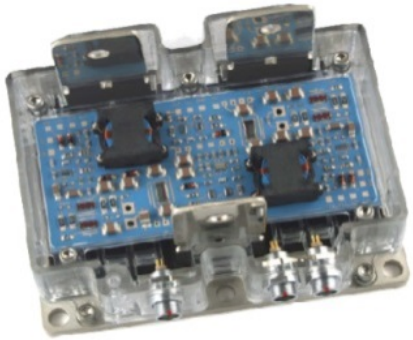


Figure 2-9. Integrated high temperature SiC MOSFET power module [51].

There are some commercial high temperature gate driver boards and one product from Cissoid is shown in Figure 2-10.

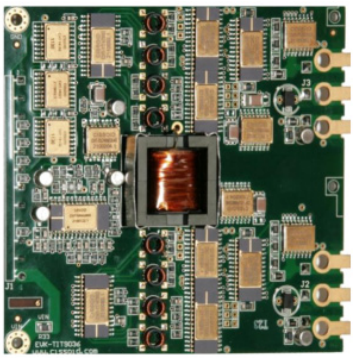


Figure 2-10. Commercial high temperature SOI gate driver [55].

A review of the state of the art of high temperature integrated gate drivers and the SOI gate driver used in this work (named as “Corinth”) are summarized in Table 2-1.

Table 2-1. Comparison of high temperature integrated gate drivers

	Temperature	Driving Capability	Frequency	Process Technology	Input Isolation
Valle-Mayorga [56]	Up to 225 °C	150 mA without external driver stages	200 kHz Not capable of DC operation	1 µm SOI CMOS	Transformer based, on-board
CISSOID Pallas	–55 °C to 225 °C junction	80 mA (low-side channel) 20 mA (high-side channel)	N/A	N/A	N/A
CISSOID Hyperion	–55 °C to 225 °C junction	1 A	3 nF at up to 500 kHz	N/A	N/A
CISSOID Themis and Atlas	–55 °C to 225 °C junction	2 A (two channels per chip in parallel can output 4 A)	N/A	N/A	Possible with additional chip CHT-RHEA
CISSOID Hades	175 °C	2 A (can be 4 A through parallel drivers)	150 kHz	Polyimide PCB	Transformer based, on-board
Corinth	−55 °C to > 200 °C	Sourcing: 5.5 A at −55 °C, 4.5 A at 200 °C Sinking: 6.0 A at −55 °C, 5.0A at 200 °C	Minimum: DC (100% high-side duty cycle) Maximum: > 200 kHz (> 550 kHz measured with adjusted charge pump input voltage)	BCD-on-SOI 0.8-micron, 2-poly, 3-metal process	N/A

CISSOID has commercialized several high-temperature integrated circuits developed on an SOI process, while the maximum on-chip source and sink current is around 2 A for each channel [55]. From the maximum current driving capability point of view, although the authors in [56] reported successful operation of a SOI gate drive chip at ambient temperatures greater than 200 °C, their on-chip output stage was limited to 150 mA. In order to increase the current capability of the SOI gate driver IC, an off-chip buffer stage based on discrete SiC JFETs are added to reach a driving capability of 5 A.

From the switching frequency point of view, all of these gate drivers are capable of high frequency operation (>150 kHz). However, there are currently no high-temperature integrated power modules based on either Cissoid's or Valle-Mayorga's solution. The only high-temperature integrated power module is reported by researchers from Arkansas Power Electronics International Inc. (APEI). Their gate driving solution is implemented using discrete SOI active devices and passive components, which limits the operating frequency and overall size/volume of the integrated power module.

In addition, during the testing of the aforementioned SiC power modules, the junction temperature measurement of the power module is either estimated through case temperature monitored by embedded thermocouples / thermistors close to the dies, or infrared radiation based measuring tool, e.g. thermal camera. All of these methods outlined necessitate visual or mechanical access to the die, which is not appropriate for an integrated power module. Is it possible to explore an online junction temperature monitoring technique for high temperature integrated power modules without any visual and mechanical access to the die?

2.3 Short Circuit Capability of SiC MOSFETs

The short circuit capability of Si IGBTs has been investigated in lots of previous literature. As reported in [57], IGBT short-circuit failure mechanism can be divided into four major modes, as shown in Figure 2-11.

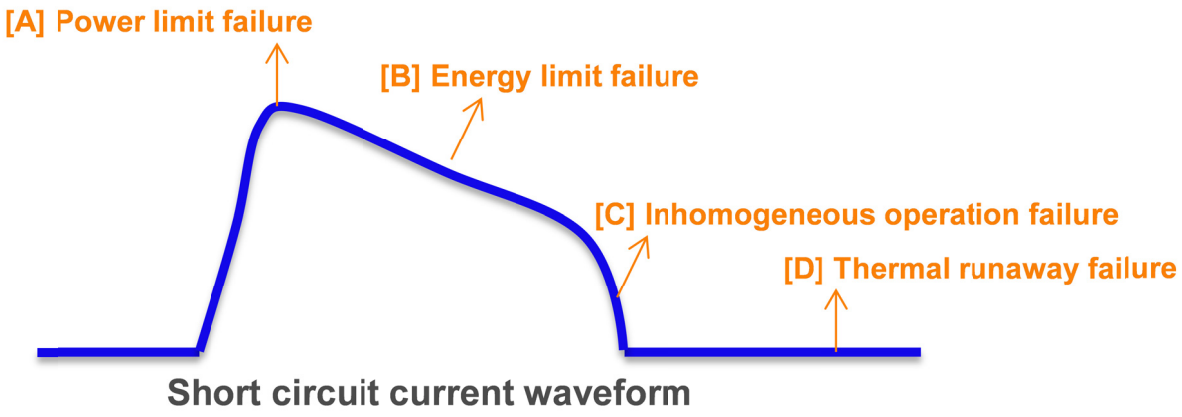


Figure 2-11. IGBT short-circuit failure modes described in previous literature

The four failure modes are described in detail as following:

[A]: The device failure occurs near the current peak due to I^2t limitation. This failure mode is an important issue for high voltage class IGBTs, i.e. over 4.5 kV.

[B]: The high-energy dissipation during the short circuit transient causes a high local temperature, which prevents IGBTs from sustaining the maximum allowable collector-emitter voltage. This is the most common failure mechanism for various kinds of IGBTs.

[C]: Inhomogeneous operation failure is generally caused by using parallel-connected IGBTs with different gate resistances.

[D]: This failure mode is associated with the large leakage current caused thermal runaway. It has been observed in the short circuit test of FS-IGBT structure. When the device is turned off from a short circuit event, the temperature within the device is still so high such that the high temperature generated leakage current is able to cause a thermal runaway issue.

Several recent research efforts have focused on the short circuit capability testing of 1200 V SiC power MOSFETs. In [58], the short circuit capability of 1200 V / 100 mΩ SiC MOSFETs with active areas of 3.5 mm × 3.5 mm are studied and analyzed at 400 V DC bus voltage, 10 V / 15 V positive gate bias, and 25 ^{o}C case temperature. It is shown that the short circuit withstand time (SCWT) is around 80 μs

at 10 V gate voltage and 50 μs at 15 V. Similar investigation of 1200 V commercially available devices is reported in [59], with a DC bus voltage of 400 V, gate voltage of +18 / 0 V, and case temperatures of 90 ^{o}C and 150 ^{o}C. A major concern of these testing results is that the short circuit test conditions may not represent the real application scenarios of 1200 V SiC MOSFETs that usually has a positive gate voltage as high as 20 V and DC bus voltage greater than 600 V. A more practical evaluation of short circuit capability can be found in [60] and [61] with 600 V DC bus voltage, 20 V / -5 V gate voltage, and 25 ^{o}C case temperature. However, the temperature dependent short circuit characteristics and associated failure mechanisms have not been investigated. In addition, it is still unclear what the key limiting factor (DC bus voltage level, temperature, fault type, device type, etc.) of short circuit capability is.

2.4 Short Circuit Protection of SiC MOSFETs

SiC MOSFETs are expected to be widely used in future converters. However, a key obstacle to its wide application is the lack of fast, reliable, low loss, and cost effective protection schemes for overcurrent/short-circuit faults. Like Si IGBTs that usually have at least 10 μs SCWT, SiC MOSFETs are also expected to have long enough SCWT for the protection circuit to detect and interrupt the fault.

Compared to overcurrent protection of Si devices and SiC JEFTs, overcurrent protection of SiC MOSFETs is more challenging in the following aspects.

From thermal point of view, SiC MOSFETs tend to have lower short circuit withstand capability compared to the Si IGBTs and MOSFETs due to smaller chip area and higher current density. According to [62], for 1200V/33A SiC MOSFETs experiencing a 600 V hard switching fault, the device failure occurs after approximately 13 μs. However, a significant leakage current is observed after 5 μs of the short-circuit condition, indicating degradation between gate and source electrodes during a short-circuit condition. As reported in [63], the short circuit withstand time of SiC MOSFETs in TO-247 package is around 8 to 10 μs under 700 V DC bus voltage and 18 V gate voltage. Recent investigation on SiC devices has shown that SiC MOSFETs present significantly lower ruggedness and robustness than SiC JFETs under short-circuit condition due to positive temperature coefficient of channel mobility up to 600

K [62]–[65]. The weaker short circuit withstand capability gives a higher pressure on the response time of the protection circuit to guarantee SiC MOSFETs operate within a safe operating area (SOA) margin.

Besides thermal breakdown, an overcurrent condition also has a negative impact on the long term stability of SiC MOSFETs, which have traditionally suffered gate oxide reliability issues induced by poor interface quality [66], [67]. Although it has been effectively mitigated by recent process improvements when operated below the maximum temperature specified by the manufacturer (125 °C), significant degradation resulting from Fowler–Nordheim tunneling current into the dielectric is evident if the temperature is raised above 125°C under overcurrent condition [68]–[70]. Low channel mobility of SiC MOSFETs requires higher positive gate bias (+20 V), i.e. higher gate electric field, and further worsens this problem [71]–[73]. In addition, as shown in [68]–[70], pulsed overcurrent operation at room temperature also results in degradation due to high junction temperature induced electron trapping, and the variation of threshold voltage increases with enhanced current levels, and increased frequencies.

Even when fast fault response time becomes the design focus of the protection scheme for SiC MOSFETs, the objective is quite challenging in a fast-switching environment. Since SiC MOSFET die has higher current density and smaller size than Si die, SiC MOSFETs tend to have lower junction capacitances and higher switching speed. Moreover, the switching speed presents different characteristics from other devices in that both the turn-on *di/dt* and *dv/dt* increases as junction temperature rises, due to the unique positive temperature coefficient of transconductance [72]. Under such high *di/dt* and *dv/dt* condition, fast response time and strong noise immunity of an overcurrent protection scheme would be a sharp contradiction. Unfortunately, currently no IEEE standard and published work exists on the allowable response time (which is a function of the amount of overcurrent, i.e. moderate overload, extensive overcurrent, and short-circuits), while a faster fault response time is always preferable to prevent it from damage and/or degradation as long as enough noise immunity can be guaranteed.

Various approaches have been proposed to protect IGBTs based on the measurement of the collector current, collector-emitter voltage, and gate voltage. The most reliable method is the direct current sensing concept, i.e. connecting a current sensor, e.g. current transformer, shunt resistor, in series with the power

devices [74], [75], as shown in Figure 2-12. The drawbacks of the current transformer are poor DC measurement, and also the need of a wide bandwidth magnetic core due to the rapid rising rate of the fault current. The drawbacks for a shunt resistor are the power consumption and also the potentially increased parasitic inductance of the power loop. In addition, costly additional sensors can make the main power circuit packaging more complicated, especially for a laminated planar busbar structure. Another similar protection scheme is based on a current mirror, realized by integrating a second sensing IGBT into the devices [76], [77]. The current mirror could indicate an overcurrent fault in that the current through the mirror is proportional to that of the main IGBT while this increases the manufacturing complexity, conduction losses, and overall cost of power modules.

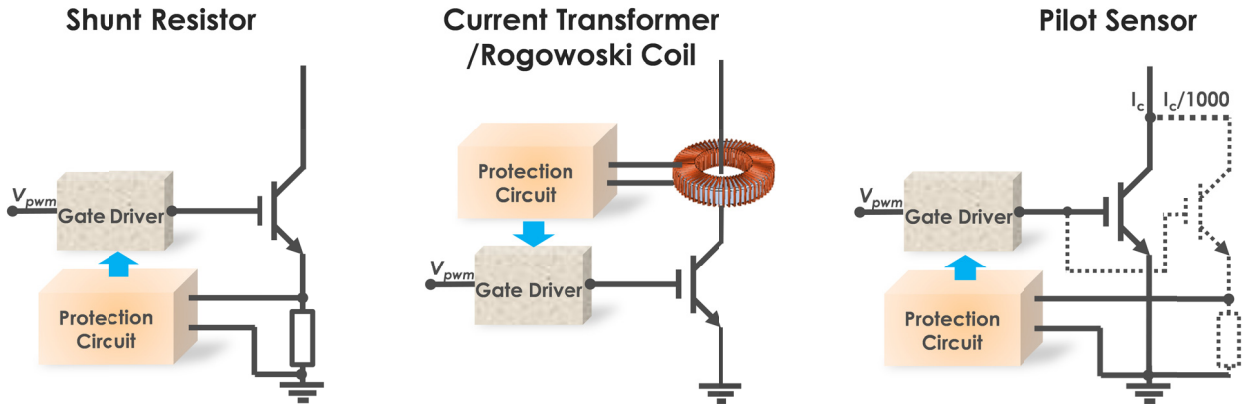


Figure 2-12. Direct current sensing based IGBT protection methods.

The other category of protection method is based on the indirect current sensing (Figure 2-13). The well-known desaturation technique uses a sensing diode to detect the collector-emitter voltage under overcurrent faults [78]–[80]. No dissipative current sensing element is required in the method. However, in order to avoid false triggering, it requires a programmed delay, so-called blanking time, of around 1 µs to 5 µs to allow collector-emitter voltage to drop below the predetermined threshold voltage (usually around 7 V) during turn-on switching transients. The fault current could surge to a very high value during the blanking time, resulting in degradation and damage of the device due to local heating.

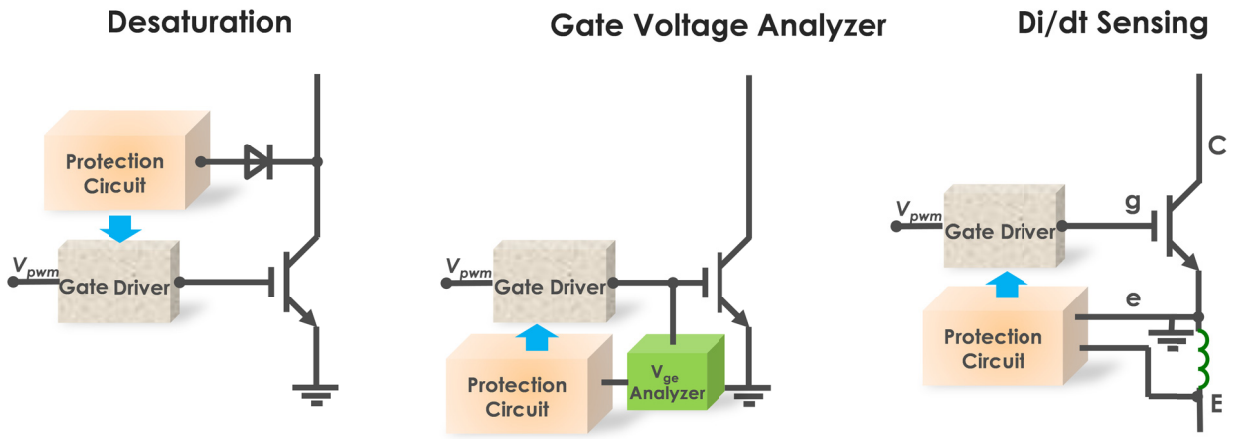


Figure 2-13. Indirect current sensing based IGBT protection methods.

Recently, changes in the gate voltage and *di/dt* have been analyzed to identify a fault condition [81]–[84] . These protection methods present a small fault detection time and are preferable to be integrated within a gate driver chip. Nevertheless, these methods require complicated detection circuitry and are sensitive to parasitic inductance caused gate loop noise and diode reverse recovery current, and thus may be challenging for practical applications.

Although various active approaches are proposed to protect IGBTs there are no known publications discussing the short circuit protection of SiC MOSFETs since they became commercially available.

2.5 Summary

In this chapter, the literature is reviewed for the four specific topics in this dissertation, i.e. the active gate drive techniques for IGBT switching loss reduction, high temperature SiC power modules, short circuit capabilities and failure mechanisms, and short circuit protection of SiC MOSFETs. The advantages and drawbacks of the state-of-art techniques are discussed, and the challenges of these topics are identified.

3 Active Gate Drive for IGBT Switching Loss Reduction

In this chapter, the switching characteristics of IGBTs using a conventional gate driver are briefly analyzed. Based on the analysis, an active gate driver (AGD) for IGBT modules is proposed to reduce the switching energy loss through switching performance improvement. A step-down converter is built as well to evaluate the performance of the proposed driving schemes under various conditions, considering variation of turn-on/off gate resistance and current levels. Experimental results and detailed analysis are presented to verify the feasibility of the proposed approach.

3.1 Analysis of IGBT Switching Characteristics

Figure 3-1 depicts the IGBT switching behavior during turn-on and turn-off transients. The turn-on transient can be divided into four stages. Stage I: The gate voltage v_{ge} rises from negative bias V_{ee} to its threshold V_{th}. Both the collector-emitter voltage v_{ce} and collector current i_c are unaffected during this stage. Stage II: v_{ge} continues increasing from V_{th} to the Miller plateau voltage V_{miller}, leading to the rapid increase of i_c. The high di/dt causes a current spike $\Delta I_{rr(peak)}$ across the device when i_c approaches its final value I_L. Stage III: v_{ce} begins to fall rapidly, while the IGBT is carrying current I_L. A voltage tail is presented at the end of this stage due to nonlinear Miller capacitance. Stage IV: v_{ge} continues to increase from V_{miller} to its final value V_{cc}. Meanwhile, the v_{ce} attains the on steady-state value $V_{ce(on)}$.

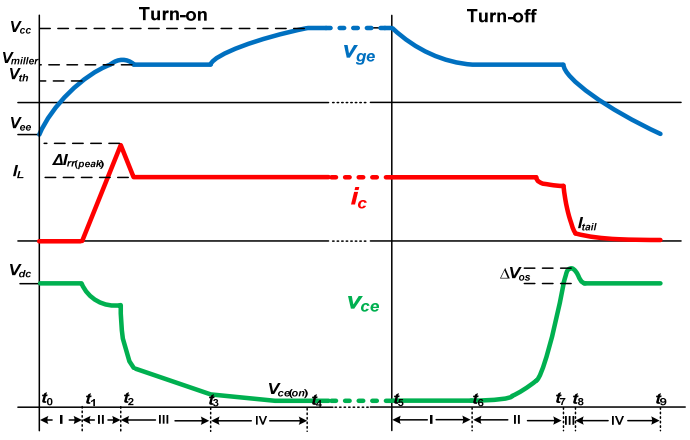


Figure 3-1. Switching waveforms of an IGBT under clamped inductive load.

The turn-off transient also includes four stages. Stage I: v_{ge} decreases from positive bias V_{cc} to V_{miller}, without changing the current and voltage across the IGBT. Stage II: The collector-emitter voltage v_{ce} begins to increase while i_c maintains at the on steady-state current I_L. v_{ce} rises slowly at the beginning due to large Miller capacitance, while it quickly increases to the DC bus voltage V_{dc} at the end. Stage III: v_{ge} falls to its threshold V_{th} and the current flowing through the IGBT deceases rapidly, inducing a voltage overshoot of ΔV_{os}. Stage IV: The current continues deceasing, with a current tail caused by the slow recombination of stored minority charge in the drift region.

3.2 Proposed Active Gate Drive

Under normal condition, the proposed AGD comprised of a turn-on and a turn-off control section, focuses on reducing the switching loss, delay time, and total switching time, while maintaining the switching stress and EMI noise level during both turn-on and turn-off transients.

3.2.1 Turn-on Control

The block diagram of the turn-on AGD is shown in Figure 3-2. In addition to a conventional push-pull buffer, the proposed turn-on control is mainly composed of five parts: *di/dt* sensing, logic circuit, level shifter, source follower, and gate charger. The functionality of each part is described as follows.

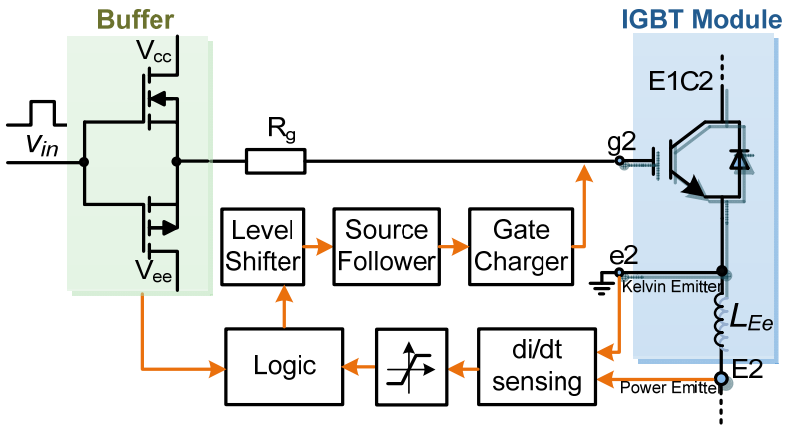


Figure 3-2. Turn-on control diagram.

The *di/dt* sensing network is used to detect the different turn-on stages based on the voltage across the parasitic inductance L_{Ee} between the Kelvin emitter and power emitter of an IGBT module. This is a pragmatic choice since using a current sensor would make the circuit more complicated and expensive. Another benefit is that the voltage is converted into logic control signals, independent of the specific inductance value of an IGBT module.

The logic circuit powered by the negative power supply V_{ee} receives both the feedback signal and the enabling signal so that the circuit works properly at different stages. The detailed circuit operation will be explained below. Considering that the feedback signal may exceed the normal input voltage range of the logic circuit at high *di/dt* and large parasitic inductance L_{Ee}, a clamping circuit is employed to protect it from failure.

An open drain level shifter serves as an interface between the logic and source follower. The level shifter serves two purposes in this implementation: 1) it inverts the logic output, and 2) it references the logic output signal to the positive rail V_{cc} of the buffer. During operation of the level shifter, a small DC current flows in the level shifter keeping the source follower and gate charger biased in correct states. Both the buffer and the turn-on auxiliary circuit power are provided by a dc-dc power supply chip.

The source follower receives the logic signal from the level shifter, and activates/deactivates the gate charger. Another key function is that it reduces power loss of the level shifter, as will be explained later.

The gate charger, a voltage controlled current source driven by the source follower, injects an additional current into the gate at certain stages to minimize the turn-on delay time and switching losses. It also decouples the turn-on control from other parts of the whole AGD.

Figure 3-3 illustrates the circuit implementation of the turn-on AGD, and its operating principle is described as follows. When the turn-on command V_{in} is applied at the turn-on delay stage, the voltage across parasitic inductance L_{Ee} is zero since no current is flowing through the IGBT module. The output of the AND logic gate becomes high, which activates the level shifter's small-signal MOSFET M_1, and subsequently the source follower MOSFET M_3 and gate charger MOSFET M_2 are turned on. Hence, the IGBT gate emitter capacitance C_{ge} is now charged by the conventional gate current i_{g1} together with the

current source i_{g2}. The delay time can be significantly reduced by adjusting the control gate resistor R_x. However, the resistance should not be too small to prevent potential gate loop oscillation. The resistance is selected for reasonable damping and low gate loop equivalent resistance, i.e.

$$2\xi\sqrt{\frac{L_G}{C_{ge}}} < R_x < R_g \qquad (3-1)$$

where, ξ is the damping factor (usually around 0.707).

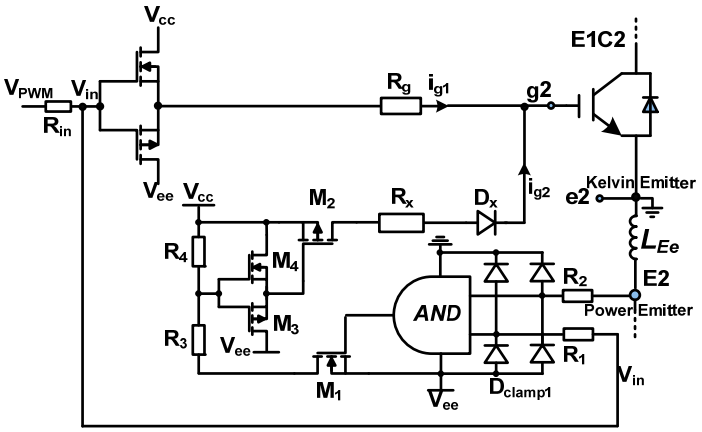


Figure 3-3. Circuit implementation of the turn-on control.

The additional gate current continuously charges the gate capacitance until the gate voltage hits the threshold V_{th} and the IGBT starts to conduct current. The collector current is increased with a rate of di/dt defined by (3-2)

$$\frac{di}{dt} = \frac{V_{cc} - v_{ge}}{L_{E1} + R_g C_{ies}/g_m} \qquad (3-2)$$

where g_m, C_{ies} (=C_{ge}+C_{gc}), and L_{E1} represent the transfer conductance, the input capacitance, and common emitter inductance of the IGBT, respectively. Accordingly, a negative voltage drop across parasitic inductance L_{Ee} is induced. When

$$-L_{Ee}\frac{di}{dt} = V_{ILmax} \qquad (3-3)$$

where $V_{IL\max}$ is the maximum allowable low-level input voltage of the AND logic circuit, the output of the AND logic circuit is flipped to low level close to V_{ee}. The low level output deactivates the M_1 of the level shifter, and consequently M_3 and M_2 are turned off, while M_4 is turned on. The IGBT input capacitance is only charged by the conventional gate current i_{g1}, which means the *di/dt*, peak reverse recovery current, and the corresponding EMI noise level stay the same as for the conventional gate drive circuit. The energy loss during the current rising stage is also not changed.

The turn-on and turn-off speed of M_2 depend on R_3 and R_4, respectively. To have fast switching speed of M_2, R_3 and R_4 should be small. However, the resistive loss of the level shifter is increased. Considering that the power dissipation of the small signal device (MOSFETs, diodes) and logic gates (AND) is very small (from several μW to several mW), the total loss of the auxiliary circuit P_s can be estimated by

$$P_s = Q_2 \cdot V_{cc} \cdot f_s + \frac{{V_{cc}}^2 \cdot D_{logic}}{R_3 + R_4} \tag{3-4}$$

where Q_2 is the gate charge of M_2, f_s is the switching frequency, and D_{logic} is the duty cycle of the logic circuit's output signal. The first term represents the driving loss of M_2, which is much smaller than the resistive loss (usually in hundreds of mW) in the second term. The source follower is an integral part in accelerating the switching speed of M_2 under the large resistance of R_3 and R_4. The source follower effectively decouples M_2's gate capacitance from the level shifter resistors. M_3 and M_4 are selected based on (3-5) to guarantee fast switching of M_2,

$$C_{iss3} \approx C_{iss4} = \left(\frac{1}{5} \sim \frac{1}{10}\right) \cdot C_{iss2} \tag{3-5}$$

where C_{iss2}, C_{iss3}, and C_{iss4} represent the input capacitance of M_2, M_3 and M_4, respectively.

At the end of the current rising stage, the reverse recovery current of the freewheeling diode (FWD) decays from its peak value back to zero. The FWD stops conducting and starts to block voltage. The device enters into the voltage falling stage. Since the current has reached its steady-state value, the output of the logic circuit is flipped back to a logic high level, and the gate charger is activated again. Higher

gate current charges the input capacitance more rapidly. As a result, the duration of the Miller plateau and the voltage tail are reduced. The turn-on energy loss due to the voltage tail is considerably reduced.

The gate charger stays in the active state until the turn-off command is received by the logic circuit. The large gate current speeds up the gate voltage rising to the steady-state value V_{cc}, and minimizes the third part of turn-on switching loss which is much smaller than the current rising and voltage falling induced switching loss. The IGBT will spend less time in the active region while transitioning to the ohmic region. Hence, the total turn-on switching time and loss are reduced.

3.2.2 Turn-off Control

The block diagram of the turn-off control is shown in Figure 3-4. It is mainly composed by four function blocks: *di/dt* sensing, logic circuit, voltage regulator, and gate discharger. Similar to the turn-on control, the *di/dt* sensing aims at detecting different turn-off stages, irrespective of the variation of stray inductance for different IGBT modules. A logic circuit activates/deactivates the gate discharger to remove current from the gate capacitance of the IGBT during part of the turn-off transient.

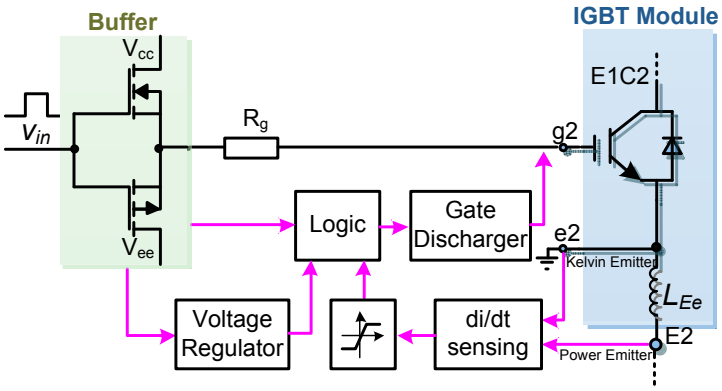


Figure 3-4. Turn-off control diagram.

Figure 3-5 illustrates the circuit implementation of the turn-off AGD. Like the logic circuit of the turn-on AGD, the turn-off logic circuit receives not only the switching command V_{in} but also the power supply from the buffer. The difference is that the turn-on logic circuit is powered by the negative power supply

V_{ee}, while the turn-on one is powered by a positive voltage regulator (R_z, C_z , S_z and D_z), due to the opposite polarity of *di/dt* induced voltage across L_{Ee} during the turn-on and turn-off transients.

The small-signal transistors (S_1 ~ S_3) are paralleled to enhance the sinking current capability of the gate discharger. The design principle of the turn-off control gate resistor R_y is the same as that of the turn-on. The diode D_y decouples the turn-off control from other parts of the whole AGD.

The operating principle of the turn-off AGD is described as follows. When the turn-off command V_{in} is applied to the AGD, the voltage across parasitic inductance L_{Ee} stays zero during both the turn-off delay stage and voltage rising stage since no current is flowing through the IGBT. The output of the NOR logic gate is high, which activates the paralleled small-signal MOSFETs of the gate discharger. The IGBT input capacitance is then discharged by the conventional gate current i_{g1} together with the current sink i_{g3}. The higher total gate current discharges the Miller capacitance more rapidly, contributing to a shorter voltage tail duration and lower turn-off switching loss.

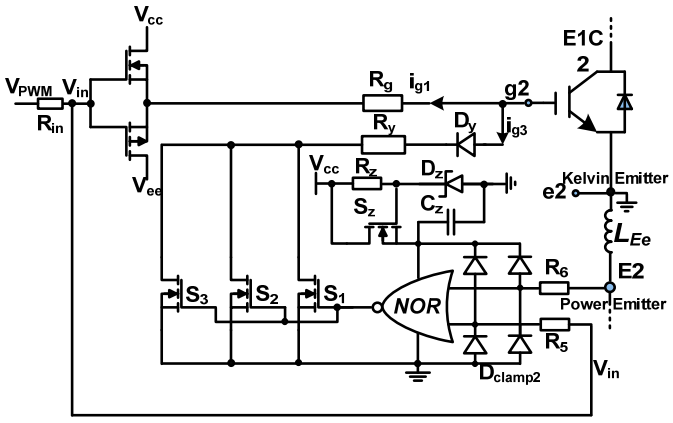


Figure 3-5. Circuit implementation of the turn-off control.

During the current falling stage, the collector current is decreased with a rate of *di*/*dt* defined by (3-6)

$$\frac{di}{dt} = \frac{V_{ee} - v_{ge}}{L_{E1} + R_g C_{ies}/g_m} \qquad (3-6)$$

A positive voltage drop across parasitic inductance L_{Ee} is induced accordingly. When there is

$$-L_{Ee}\frac{di}{dt} > V_{IHmin} \qquad (3-7)$$

where V_{IHmin} is the minimum allowable high-level input voltage of the NOR logic gate, the output of the gate is flipped to a logic low level. This low level output deactivates the gate discharger by turning $S_1 \sim S_3$ off. The gate is only discharged through the CGD. Therefore, the current falling induced switching loss and voltage spike through power loop parasitic inductance are the same as that of using a CGD.

As soon as the device enters into the current tail stage, the gate discharger is activated again to speed up the gate voltage to its final value, V_{ee}. The switching loss, however, caused by the tail current cannot be reduced with this gate driving strategy.

For the turn-off control auxiliary circuit, the power dissipation primarily comes from the small signal device (MOSFETs, diodes) and logic gates (NOR), which is even less than that of the turn-on auxiliary circuit due to the elimination of the level shifter with relatively large resistive loss.

According to the above analysis, the proposed active gate driver is actually an open-loop control system based on the event feedback of the switching transients, and therefore the circuit stability is not a key issue. However, all of the active devices and logic gates should have small switching and propagation delay times for a minimum control delay and high control accuracy. Moreover, in the design of the AGD, the dynamic and steady state behavior of the small signal transistors and the diodes should be taken into account. The on-state resistance of the gate charger/discharger transistor (M_2, $S_1 \sim S_3$) and the on-resistance of the decoupling diodes (D_x and D_y) should also be low for proper operation.

3.3 Experimental Verification

Experimental results are presented for an IGBT module using both the CGD and AGD. The test circuit is a step down converter shown in Figure 3-6, which represents one phase leg of a three phase inverter with a clamped inductive load. In addition, to verify the protection function of the AGD, the short circuit control switch, composed by two paralleled IGBT modules, is used to create a shoot-through fault.

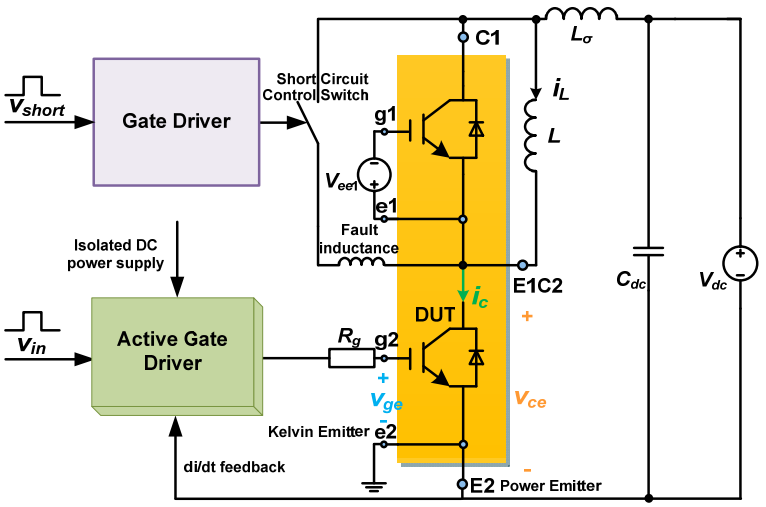


Figure 3-6. Experimental test circuit.

3.3.1 Test and Measurement Setup

The device used for the experimental test is a 600 V / 400 A IGBT module (CM400DY-12NF) from Powerex. The experimental waveforms are recorded by a Tektronix DPO5204 2 GHz 4 channel digital phosphor oscilloscope. The voltages are measured with calibrated active high voltage probe Tektronix P5205, with bandwidth of 100 MHz. The collector current is measured using a T&M Research SSDN-015 coaxial shunt with resistance of 0.015 Ω and bandwidth of 1.2 GHz. The switching energy loss is calculated by programming a math function of the oscilloscope. Moreover, the channel delays caused by different types of probes are compensated before testing.

The experimental test and measurement setup is shown in Figure 3-7. The low side IGBT serves as the device under test (DUT) in this work. The high side IGBT could also be adopted as the DUT as long as its stray inductance is identified. The operation principle of the AGD for low side and high side device is similar, regardless of the constantly changing emitter potential of high side IGBTs. The two channel synchronous waveform generator sends one signal (v_{in}) to the gate driver of the DUT, and the other one (v_{short}) to the gate driver of the short circuit control switch. All testing waveforms are extracted by MATLAB to compare switching performances and protection performances under different conditions.

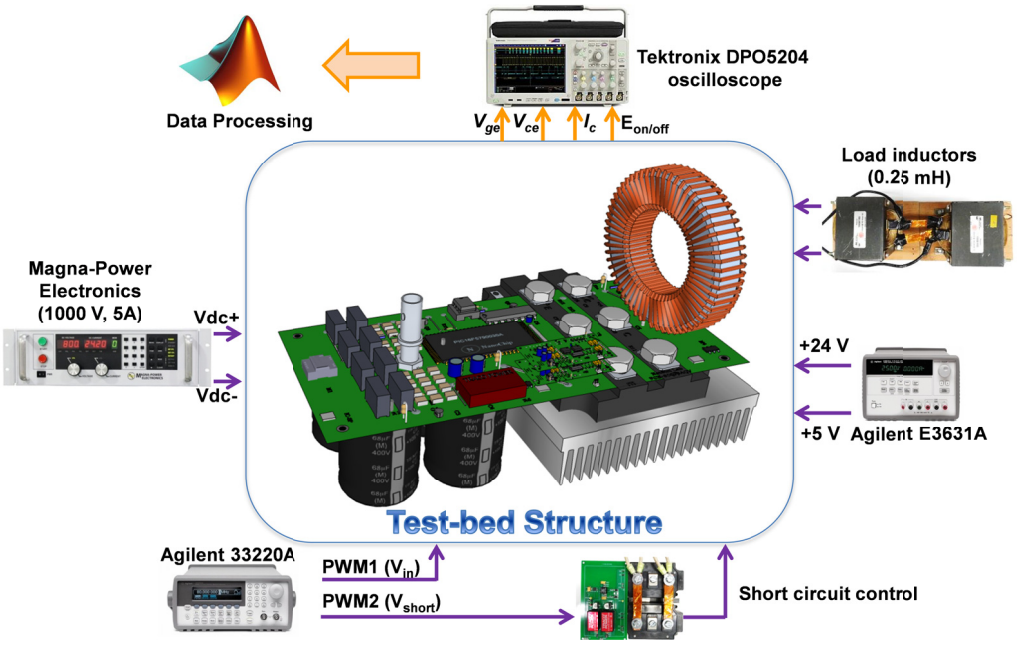


Figure 3-7. Experimental test and measurement setup.

The hardware testbed is shown in Figure 3-8. The IGBT module and DC capacitors are connected by a planar busbar structure within the PCB board. The turn-on control, turn-off control, and overcurrent protection (OC protection) are integrated together and physically closest to the device control pins.

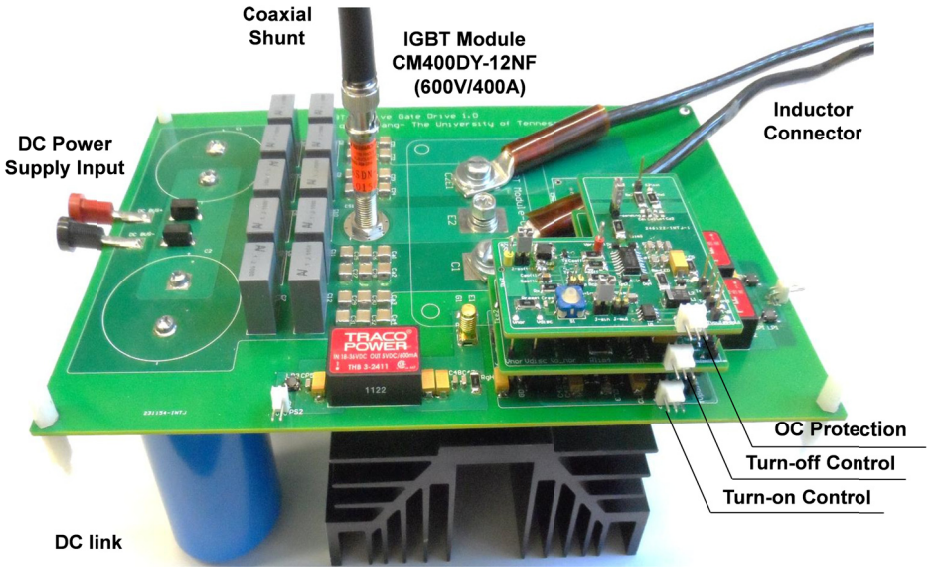
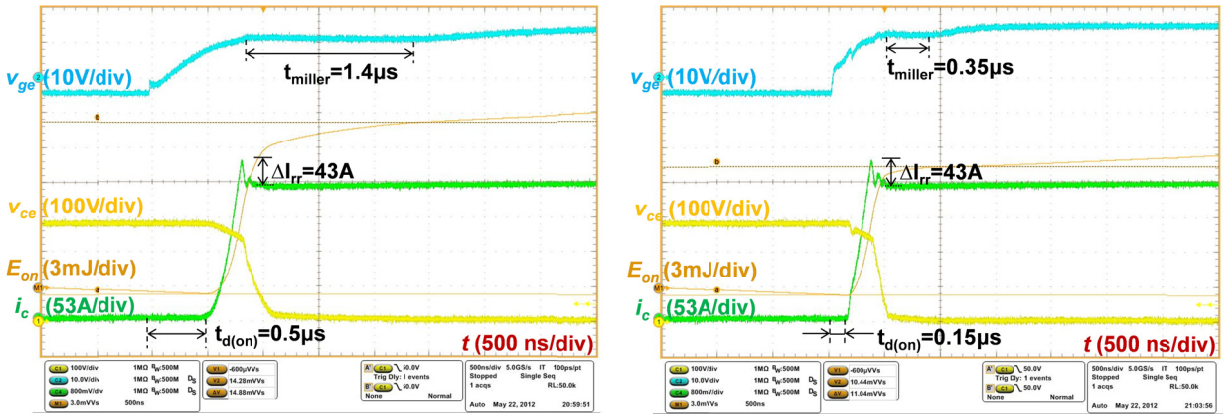


Figure 3-8. Hardware testbed for performance evaluation of the AGD.

3.3.2 Turn-on Performance Comparison

Comparative turn-on switching waveforms at 300 V DC bus voltage and 200 A load current with 10 Ω gate resistance is shown in Figure 3-9(a) and (b). In the figure, E_{on}, t_{miller}, $t_{d(on)}$, and ΔI_{rr} represent turn-on energy loss, Miller plateau duration, turn-on delay, and peak reverse recovery current, respectively.

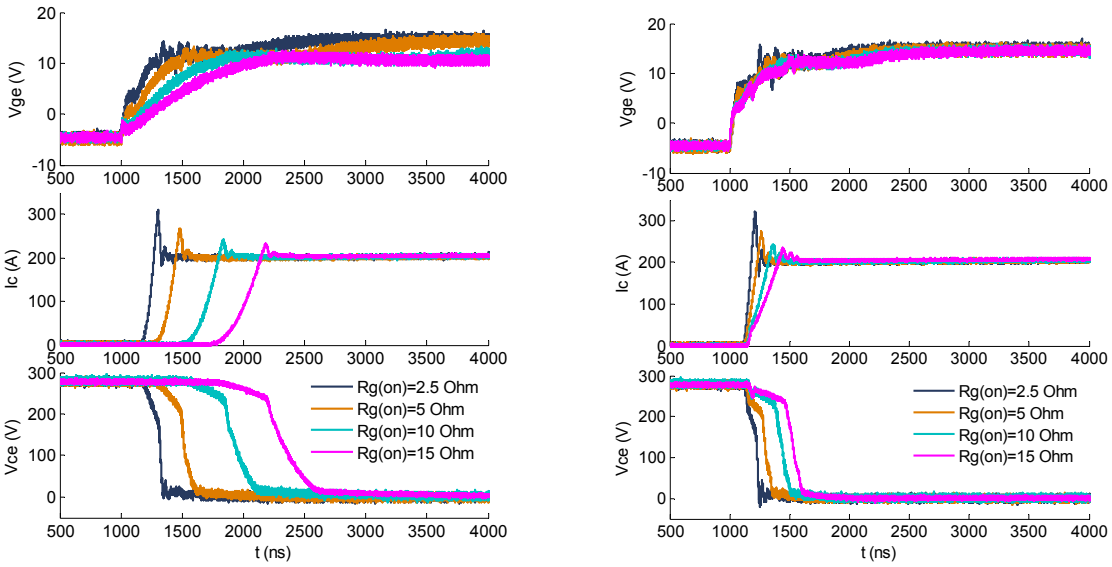


(a) Conventional gate driver (b) Active gate driver

Figure 3-9. Comparison of turn-on waveforms with different gate drivers.

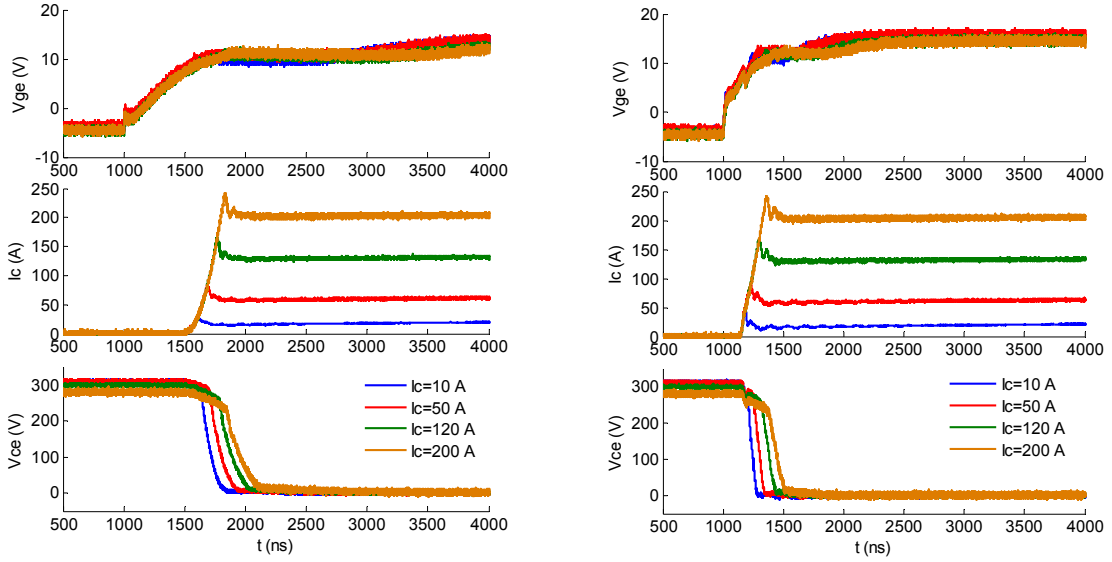
With the conventional gate drive, the turn-on delay is around 0.5 µs, while it is reduced to around 0.15 µs when the AGD is used. The peak reverse-recovery current for both cases is kept at the same value (43 A). The Miller plateau duration time is reduced from 1.4 µs with CGD to 0.35 µs with AGD, leading to a shorter voltage tail and turn-on energy loss reduction from 14.9 mJ to11.0 mJ.

Both gate drivers with different turn-on gate resistors (2.5 Ω, 5 Ω, 10 Ω, 15 Ω) under a constant load current of 200 A and DC bus voltage of 300 V are also tested. The results are imported into MATLAB and compared, as shown in Figure 3-10(a) and (b). It can be seen that there is a large variation of switching time with CGD, while the switching waveforms tend to merge together when AGD is adopted, indicating a reduction of total switching time as well as energy loss.



(a) Conventional gate driver (b) Active gate driver

Figure 3-10. Comparison of turn-on waveforms with different gate resistors using CGD and AGD.

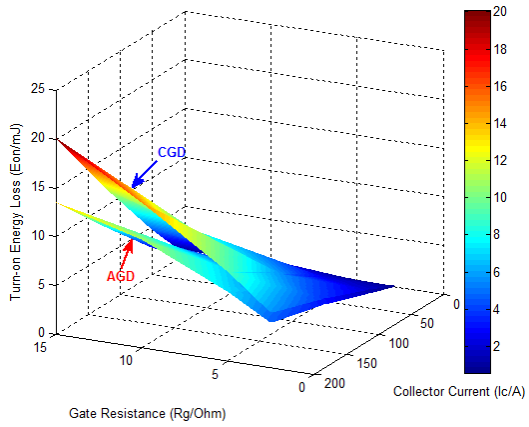


(a) Conventional gate driver (b) Active gate driver

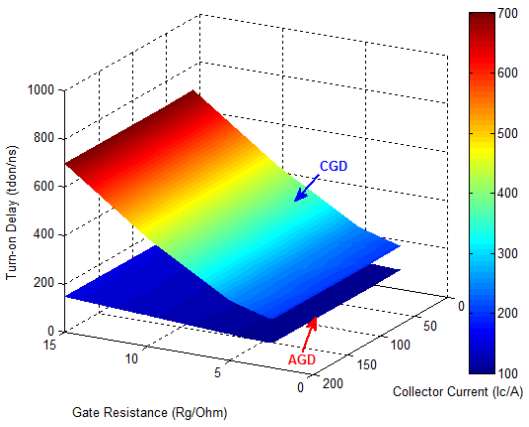
Figure 3-11. Comparison of turn-on waveforms with different current levels using CGD and AGD.

More testing waveforms are recorded under different current levels (10 A, 50 A, 120 A, 200 A), with a gate resistance of 10 Ω and DC bus voltage of 300 V, as shown in Figure 3-11(a) and (b). Similar to the trend in Figure 3-10, the turn-on switching time is reduced by the AGD under different current levels, while the *di/dt* and associated peak reverse recovery current keeps nearly unchanged in both cases.

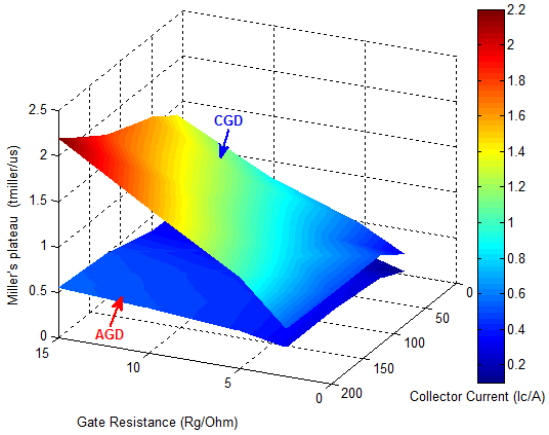
The turn-on AGD is also extensively evaluated with different combinations of gate resistance and current levels. The turn-on energy loss, delay time, Miller plateau duration, and peak reverse-recovery current as functions of the gate resistance R_g and current level I_c are plotted for both gate drive circuits under 300 V DC bus voltage, as shown in Figure 3-12(a) to (d), respectively.



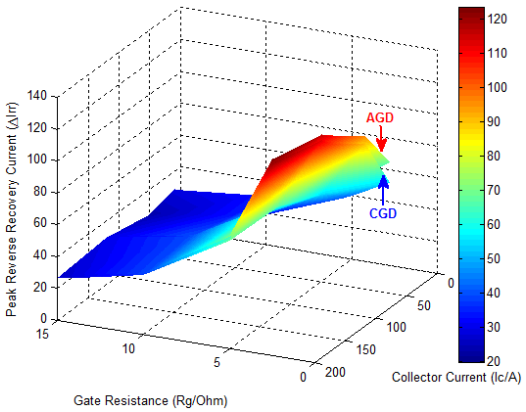
(a) Turn-on energy loss



(b) Turn-on delay



(c) Turn-on Miller plateau duration



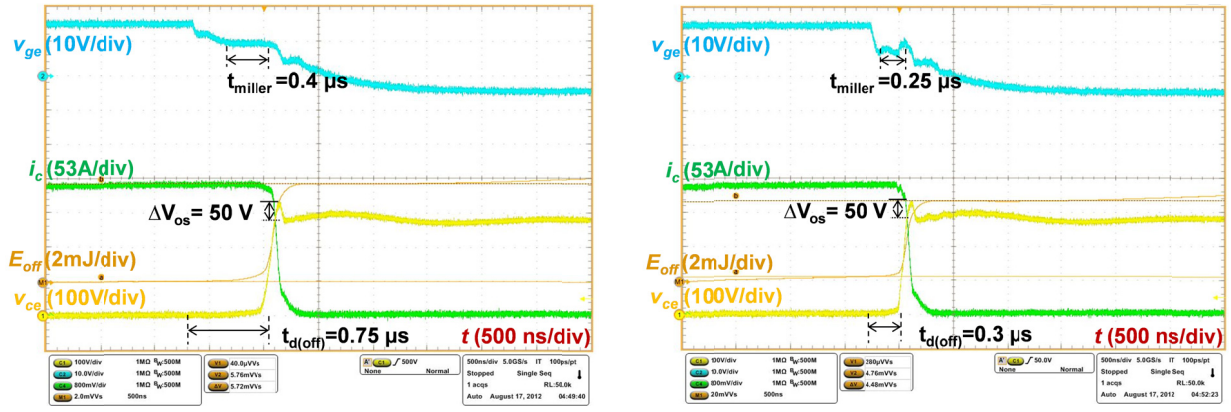
(d) Turn-on reverse recovery current peak

Figure 3-12. Comparison of the two gate drivers under different current levels and gate resistors.

As the turn-on gate resistance is increased, the delay time and the dissipated turn-on energy increase monotonically, while the peak reverse-recovery current decreases. The delay time of the proposed AGD circuit only changes from 100 ns to 150 ns, even shorter than that of a CGD with gate resistance of 2.5 Ω. The switching energy is reduced by 20% to 35% in the plotted gate resistor and current level range, and the turn-on delay is reduced by 50% to 80%. The Miller plateau duration, which represents a significant portion of total turn-on switching time, is reduced by 30% to 80% in the plotted range. Moreover, there is a trend that more switching time and energy loss are saved with larger gate resistance and higher current levels. The reverse recovery current peak values with both drivers are nearly the same at high gate resistance and high current level region. However, the reverse recovery current peak of AGD gradually exceeds that of CGD with a decrease in gate resistance and current level, due to turn-on *di/dt* feedback control delay.

3.3.3 Turn-off Performance Comparison

The turn-off experimental results using the power module under the same test conditions as turn-on are obtained. Comparison of the turn-off switching waveforms at 300 V DC bus voltage, and 200 A load current with 10 Ω gate resistance is shown in Figure 3-13(a) and (b). In the figure, E_{off}, $t_{d(off)}$, and ΔV_{os} represent turn-off energy loss, turn-off delay, and voltage overshoot, respectively.



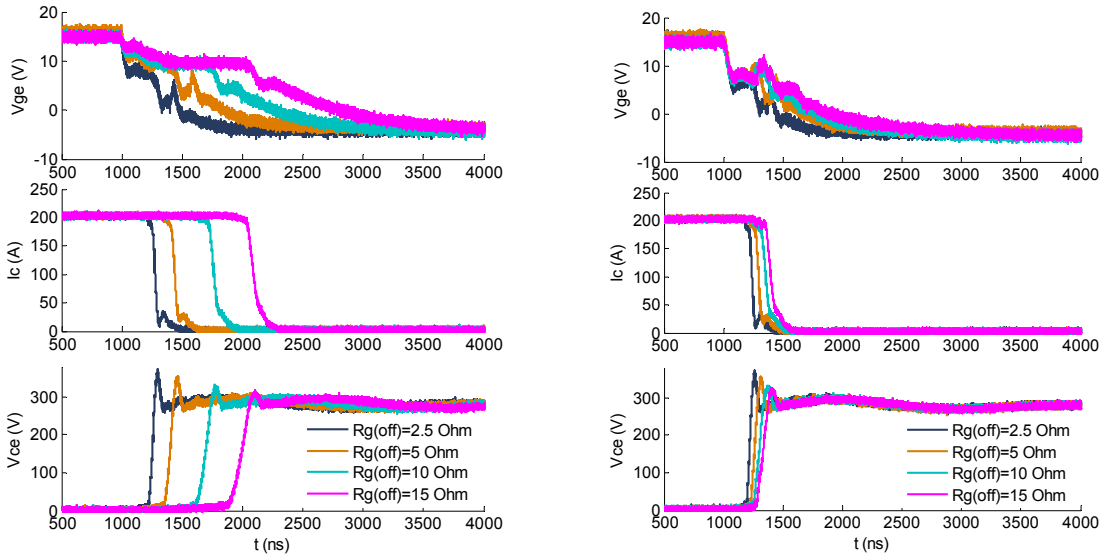
(a) Conventional gate driver (b) Active gate driver

Figure 3-13. Comparison of turn-off waveforms for the two methods.

The AGD reduces the turn-off delay time from 0.75 μs to 0.3 μs, and turn-off switching energy loss from 5.72 mJ to 4.48 mJ, while keeping the same turn-off overvoltage (50 V) as that of using the CGD. The Miller plateau time is reduced from 0.4 μs to 0.25 μs, which contributes to the contraction of voltage tail and turn-off energy loss.

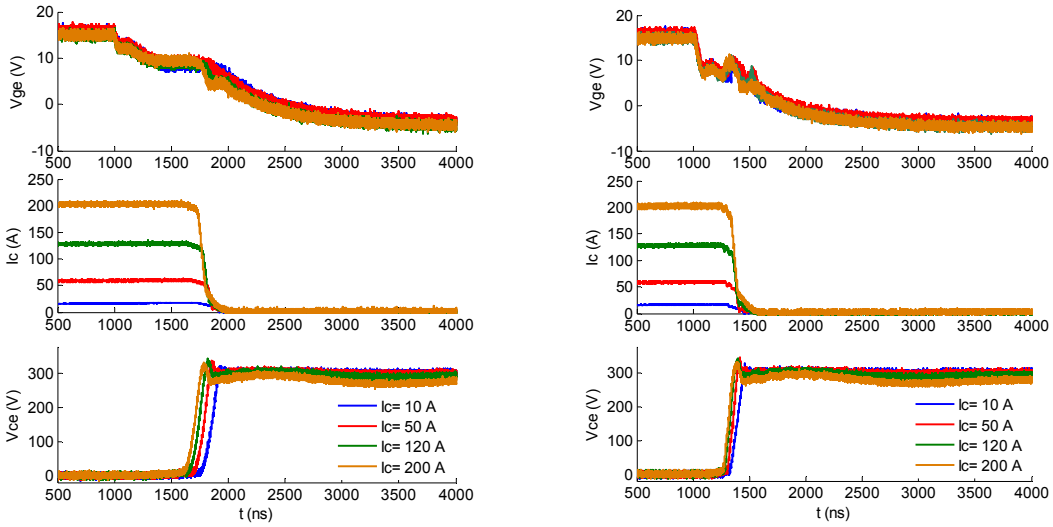
Different turn-off gate resistors are also used under a constant load current of 200 A and DC bus voltage of 300 V for both the CGD and AGD to compare their switching characteristics, as shown in Figure 3-14(a) and (b). With different turn-off gate resistors, a large variation of turn-off switching time is clearly observed when CGD is used, while the switching waveforms tend to merge with each other when AGD is adopted, indicating a reduction of total switching time as well as energy loss.

Turn-off experimental waveforms are also measured and compared under different current levels (10 A, 50 A, 120 A, 200 A), with a gate resistor of 10 Ω and DC bus voltage of 300 V for both gate drivers, as shown in Figure 3-15(a) and (b). The turn-off switching time is reduced by the AGD under different current levels, while the *di/dt* and associated voltage overshoot stays nearly unchanged for both.



(a) Conventional gate driver (b) Active gate driver

Figure 3-14. Comparison of turn-off waveforms with different gate resistors using CGD and AGD.



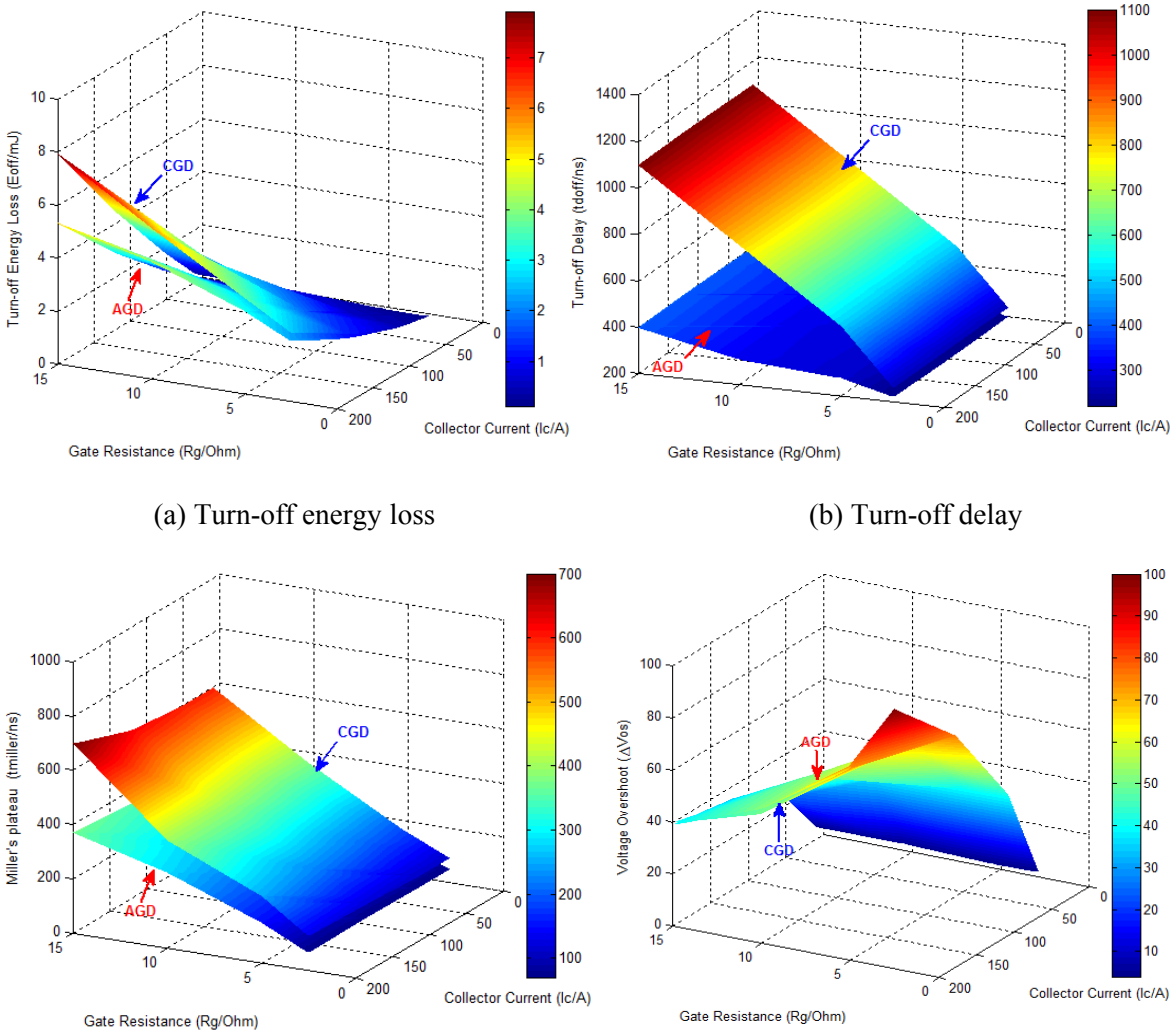
(a) Conventional gate driver (b) Active gate driver

Figure 3-15. Comparison of turn-off waveforms with different current levels using CGD and AGD.

The AGD is also extensively evaluated with different combinations of gate resistors and current levels. The turn-off energy loss, delay time, Miller plateau duration, and overshoot voltage as functions of the gate resistance R_g and current level I_c are plotted for both gate drive circuits under 300 V DC bus voltage, as shown in Figure 3-16(a) to (d), respectively.

The delay time and the dissipated turn-off energy are increased with the increase of gate resistance, while the voltage overshoot decreases. When the AGD is adopted, the delay time fluctuation is small (from 220 ns to 400 ns), compared with the delay time of 260 ns to 1100 ns with the CGD. The turn-off switching energy is reduced by 15% to 33% in the plotted gate resistance and current level range, and the turn-off delay is reduced by 15% to 64%. The Miller plateau duration is reduced by 36% to 47% in the plotted range. Like the turn-on test results, even more improvement can be shown in reduced switching time and turn-off energy loss for applications with larger gate resistance and higher current levels, which indicates that the proposed AGD is preferable for EMI sensitive applications that usually have larger gate resistance, and high power converters with high current levels.

The voltage overshoot with both drivers keeps nearly unchanged not only at high gate resistance and high current level region, but also low gate resistance and low current level region. This is because the turn-off *di/dt* feedback control delay is much smaller compared to the total current falling time.



(a) Turn-off energy loss

(b) Turn-off delay

(c) Turn-off Miller plateau duration

(d) Turn-off voltage overshoot

Figure 3-16. Comparison of the two gate drivers under different current levels and gate resistances.

3.4 Conclusion

In this chapter, a *di/dt* feedback based IGBT gate driver is proposed for switching performance improvement and short circuit protection. The design consideration and circuit implementation of the gate

driver are discussed. Experimental results are presented and compared with conventional gate driving strategy. The key features of the proposed gate driver could be summarized as follows:

1) The switching loss, delay time, and Miller plateau duration are reduced by means of auxiliary current source/sink, regardless of power level, gate resistance, as well as IGBT types with some variation of parasitic inductance L_{Ee}. Switching stresses are still controlled by conventional gate drivers.

2) The AGD could detect an overcurrent fault through evaluation of the current through IGBT modules without any blanking time. The built-in protection modes prevent the interruption of converter operation in the event of momentary short circuits.

3) The AGD shares the same isolated power supply with the push-pull buffer, and high bandwidth detection and regulation circuits (e.g. current/voltage sensors, operational amplifier, etc.) are avoided, which is beneficial to the overall reliability and potential integration into a gate drive chip.

One drawback of the AGD is the lack of online regulation of *di/dt* and *dv/dt*. Also, the fault response time of the AGD is subjected to considerable extension under faults with large short-circuit impedance, e.g. ground fault. Fortunately, this type of short circuit leading to a fault current with low *di/dt* generally can be detected by current sensors of converters.

4 High Temperature Integrated Power Module

This chapter presents a board-level integrated silicon carbide (SiC) MOSFET power module for high temperature and high power density application. Specifically, a silicon-on-insulator (SOI) based gate driver capable of operating at 200 °C ambient temperature is designed and fabricated. Also, a 1200 V / 100 A SiC MOSFET phase-leg power module is developed utilizing high temperature packaging technologies. The static characteristics, switching performance, and short-circuit behavior of the fabricated power module are evaluated at different temperatures. Moreover, a buck converter prototype composed of the SOI gate driver and SiC power module is built for high temperature continuous operation. The converter is operated at different switching frequencies up to 100 kHz, with its junction temperature monitored by a thermo-sensitive electrical parameter (TSEP) and compared with thermal simulation results. The experimental results from the continuous operation demonstrate the high temperature capability of the power module at a junction temperature greater than 225 °C.

4.1 Silicon-on-Insulator Gate Drive

Although SiC power devices are commercially available for high temperature application, SiC control electronics and integrated circuits are still in early stages of development [85]. For high temperature integrated circuits (up to approximately 300 °C), the most mature and commercially available alternative is SOI process technology [56], [86].

The high temperature SOI gate drive chip used in this work was fabricated on a Bipolar-CMOS-DMOS (BCD) on silicon-on-insulator (BCD-on-SOI) 0.8-micron, 2-poly, 3-metal process, which combines the advantages of high-voltage LDMOS devices with SOI technology. Instead of utilizing a die bonded to a package (e.g. dual in-line package or small-outline IC packages) and mating the package to a printed circuit board (PCB) through a socket, the chip-on-board (COB) approach is adopted, which directly bonds the die to a PCB. One advantage of this approach is that the overall size / volume and thus power density of the integrated power module can be enhanced. This implementation could also have a

large impact on gate-loop parasitics and switching loss reduction, due to much shorter wire bonds to the PCB and the elimination of bulky chip package and socket.

Figure 4-1 illustrates placement of the SOI die to a polyimide PCB with COB approach. The connection between the die and PCB can be observed under a microscope without glob top encapsulations. Before the COB process, the pads of the entire PCB are coated with soft bondable gold surface finish (electrolytic Ni / Au plating, thickness: 100-150 / 30-50 μin) to improve its overall bondability. The die is mounted to the board through conductive die attach adhesive (Ablebond 84-1), followed by a curing process that facilitates the final mechanical, thermal, and electrical properties. Then, 1 mil Au wirebonds are connected between the board and the die via thermocompression bonding process. Finally, the assembly is encapsulated by an epoxy-based material (Hysol EO1061) to protect the die and wirebonds from mechanical and chemical damage. Both the die attach and encapsulation materials are rated up to 250 ^{o}C.

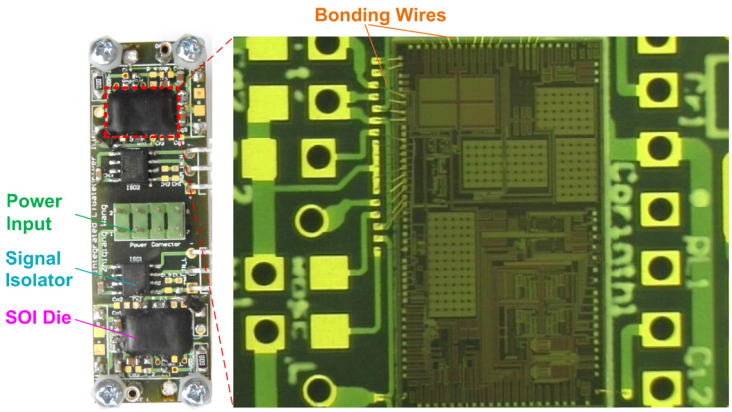


Figure 4-1. SOI die placement on PCB with COB approach.

The SOI die discussed here does not include a high temperature input isolation function, which means this SOI chip cannot be used to drive a phase-leg power module (in “totem pole” structure). In order to build a gate driver board for the developed SiC MOSFET phase-leg power module, a commercial input signal isolator is used, with a maximum operating temperature of 105 °C. Therefore, the whole gate driver

board is unable to be tested at a high temperature environment up to 200 °C, even though all other parts (SOI die, PCB substrate, passive components, etc.) are high temperature capable. For high temperature testing, another COB-based polyimide board using the same SOI die is built (without the signal isolator), and the testing results have been published in [87].

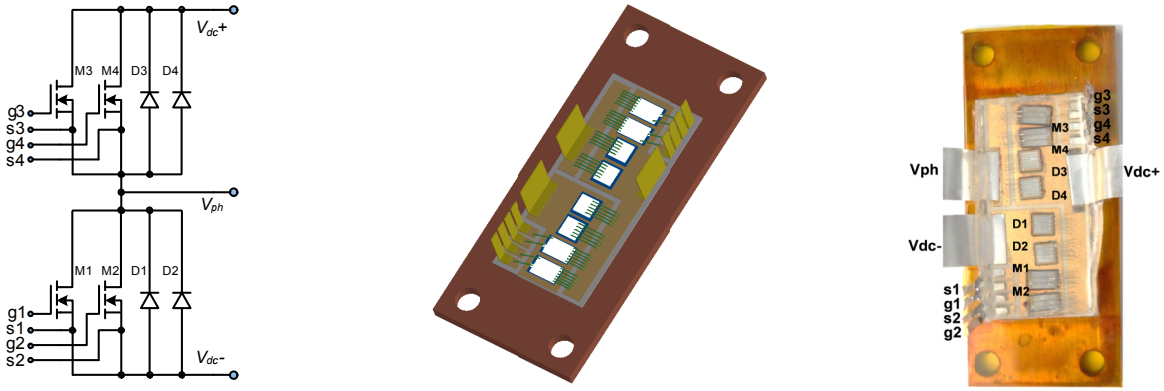
On the other hand, a SOI air core transformer-based isolator for the integrated power module is under development, aiming at reduced isolator volume for easy chip-level integration and elimination of high temperature aging effects of magnetic materials found in conventional transformer-based isolators.

4.2 High Temperature Power Module

The SiC power module needs to be carefully designed to operate at high junction temperature (>225°C). Also, the temperature dependent electrical performance of the power module needs to be evaluated before potential high temperature continuous operation.

4.2.1 Phase-Leg Power Module Design

The high temperature phase-leg power module utilizes Cree's second-generation 1200 V, 50 A SiC MOSFET (CPM2-1200-0025B) and 1200 V, 50 A SiC Schottky diode (CPW5-1200-Z050B). Two MOSFETs and two diodes are paralleled in each switch position to reach a rated current of 100 A. Figure 4-2(a) to (c) show the schematic, layout design, and the prototype of the power module, respectively.



(a) Schematic (b) Module layout (c) Fabricated power module

Figure 4-2. 1200 V / 100 A SiC MOSFET based high temperature phase-leg power module.

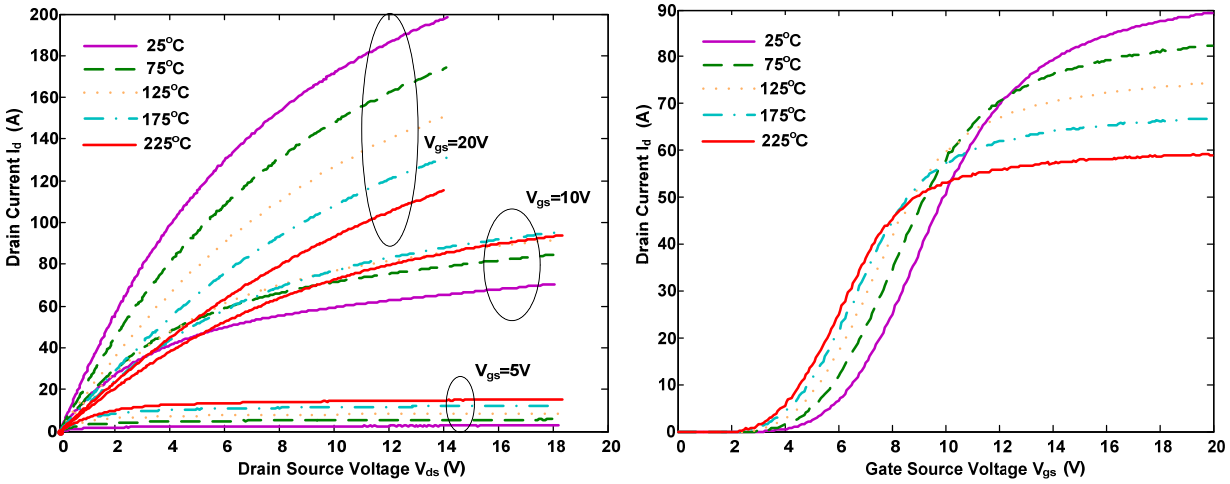
In order to operate at high junction temperature, packaging materials for each part of the power module are selected based on the literature study and past research experience at Oak Ridge National Laboratory [88]–[90].

4.2.2 Static Characterization

The static characteristics of the fabricated power module are measured using a Tektronix 371B curve tracer. The power module is heated by a controlled hotplate so that it can be characterized under various temperatures up to 225 °C. The case temperature, nearly identical to the junction temperature due to negligible self-heating under static characterization, is monitored by two K-type thermocouples. All testing results are extracted by MATLAB to clearly show the temperature dependent characteristics.

Figure 4-3(a) illustrates the temperature dependent output characteristics of the SiC MOSFET. At low gate voltage (5 V), the curve moves up with the increase of junction temperature, indicating a decrease in on-state resistance. However, it presents the opposite trend at high gate voltage (20 V). At medium voltage levels, e.g. 10 V, the curve first moves up and then moves down as temperature rises. Similar temperature dependent behavior can also be observed in the transfer characteristic, as shown in Figure 4-3(b). The slope, i.e. transconductance, increases at elevated temperatures with low gate voltages, decreases with high gate voltages, and first increases and then decreases at medium gate voltages.

These temperature behaviors, different from the Si MOSFET, can be explained by the competition between the channel resistance (negative temperature coefficient) and the drift region resistance (positive temperature coefficient) [43]. A more direct representation of this phenomenon is seen in Figure 4-4. A valley appears in the curve with the gate voltage v_{gs} = 15 V, whereas the on-state resistance $R_{ds(on)}$ monotonously increases in the case of v_{gs} = 20 V. The higher gate voltage level contributes to not only lower $R_{ds(on)}$, but also easier device paralleling or current sharing. In this work, +20 V is selected as the positive gate bias.



(a) Output characteristics (b) Transfer characteristics

Figure 4-3. Static characteristics of the SiC MOSFET (one die) at various temperatures.

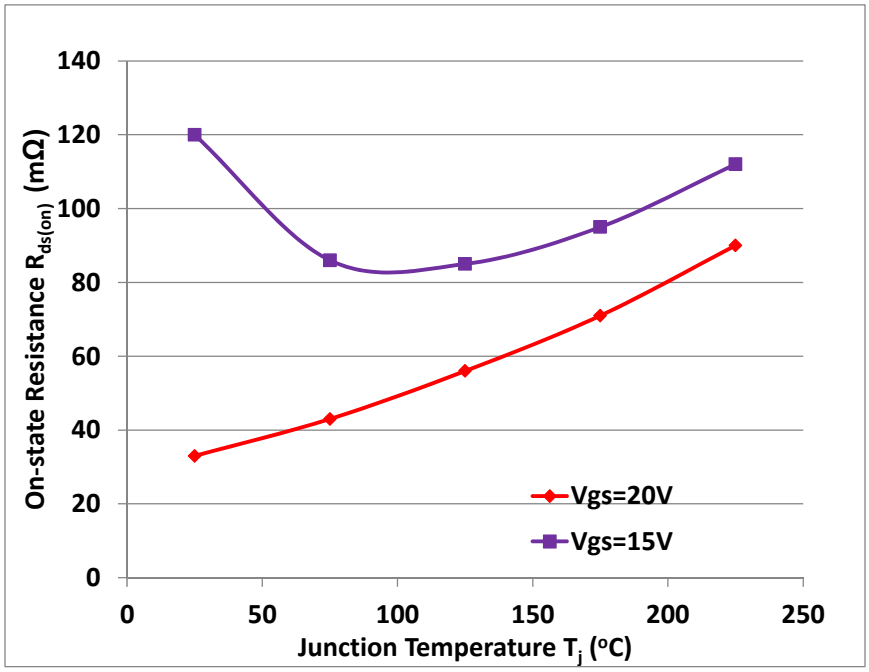


Figure 4-4. Temperature dependent on state resistance.

Another important characteristic is the leakage current of the power module at various temperatures. The total leakage current of each switch position (two SiC MOSFETs and two SiC Schottky diodes) are measured at 600 V as a function of the junction temperature, with gate-source terminals shorted. As

shown in Figure 4-5, the leakage current of the upper and lower switch position shows close trend, and is below 100 μA within the tested temperature range. This low leakage current and corresponding negligible power dissipation prevents the power module from potential thermal runaway issue at high temperature operation, a key issue for high temperature operation of Si devices.

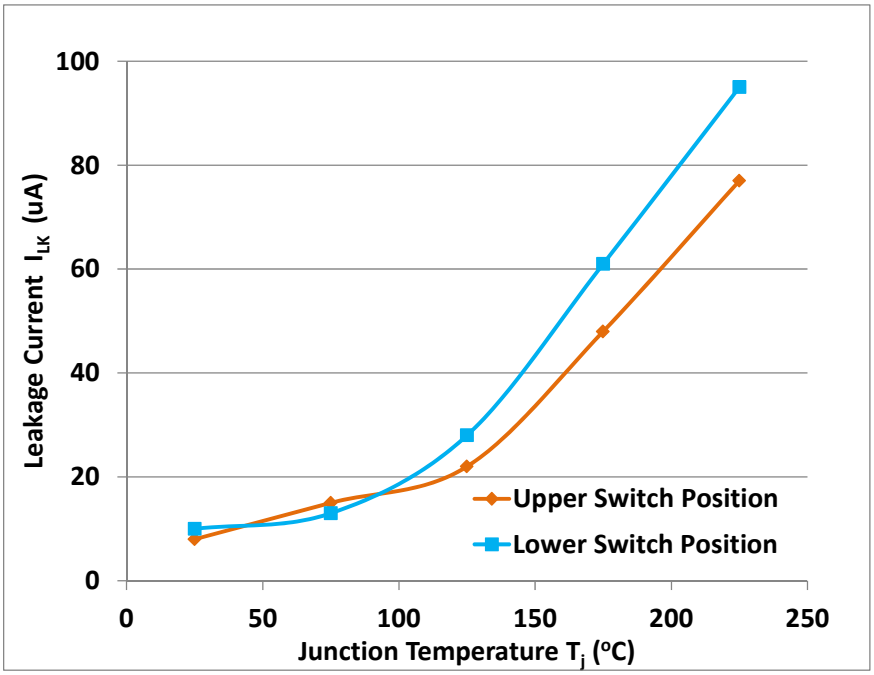


Figure 4-5. Temperature dependent leakage current.

4.2.3 Switching Characterization

The board-level integrated power module is shown in Figure 4-6, incorporating the fabricated SiC MOSFET phase-leg power module, the SOI gate driver board discussed above, and a gate driver power supply board with two-channel isolated output for a phase-leg configuration. The final volume of the integrated power module (without including the gate driver power supply, baseplate and heatsink) is 46.5 mm × 21 mm × 11 mm.

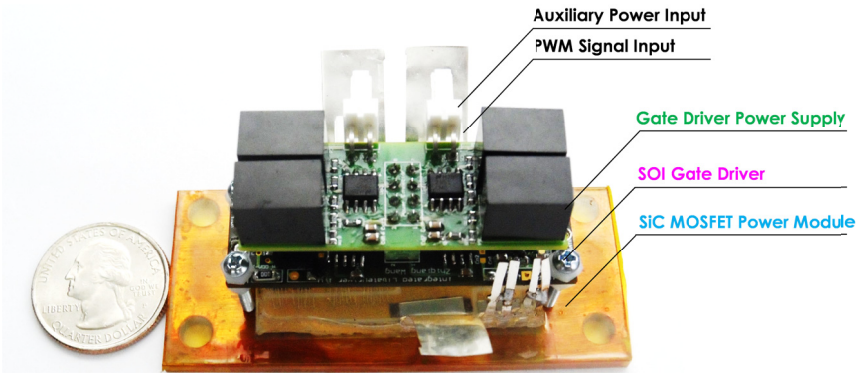


Figure 4-6. Board-level integrated power module.

The switching behavior of the integrated power module is characterized by a multifunction power stage. The circuit diagram and hardware of the power stage are shown in Figure 4-7 and Figure 4-8. The basic functions of the power stage include standard double pulse test, short-circuit and overcurrent protection test (with short-circuit control branch in parallel with upper device), and continuous buck operation (with LRC load instead of pure inductive load). The inductances L, L_σ, and L_{fa} stand for the load inductance, main-loop parasitic inductance, and short-circuit inductance. C_{dc} and C_s represent the DC bus energy storage capacitance and decoupling capacitance. A normally-on solid state circuit breaker taking advantage of the well-known desaturation protection schemes of IGBTs is connected in series with the DC bus to detect and clear overcurrent faults [91].

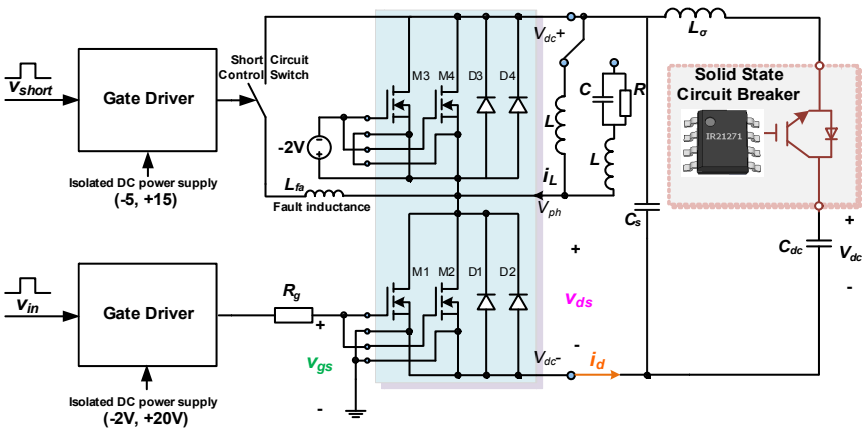


Figure 4-7. Circuit diagram of the multifunction power stage.

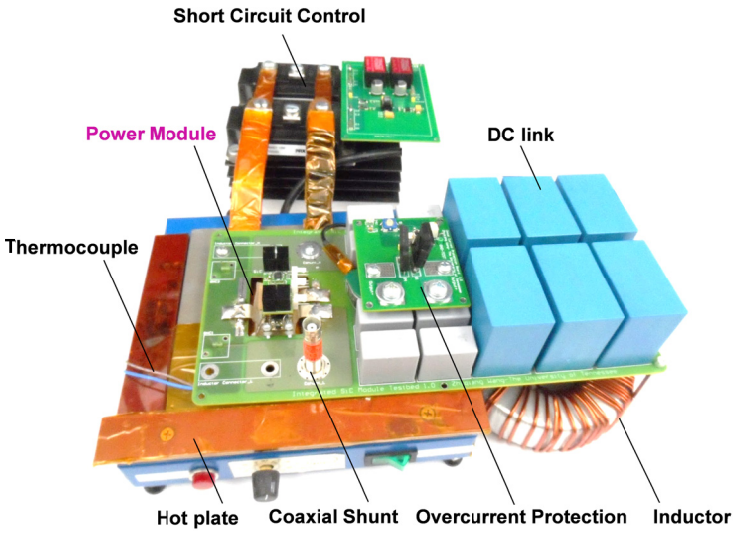


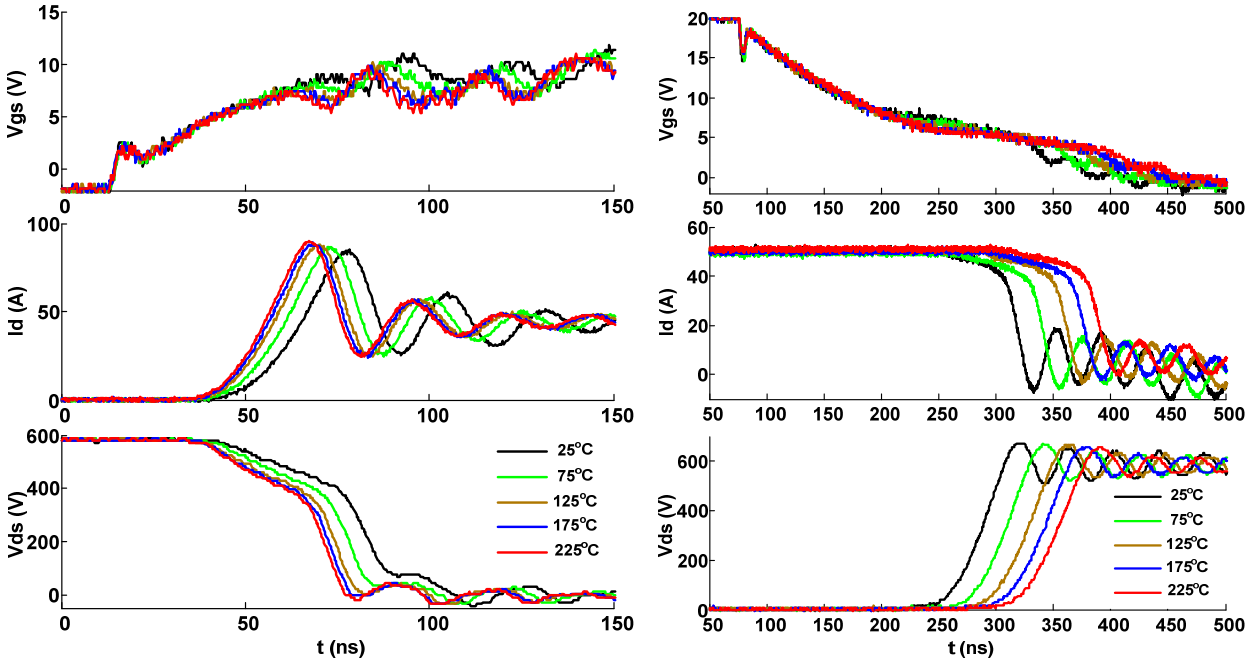
Figure 4-8. Hardware picture of the multifunction power stage.

The temperature dependent turn-on and turn-off transient waveforms of the integrated power module are shown in Figure 4-9(a) and (b) respectively, with a 600 V DC bus voltage, 50 A load current, and 10 Ω gate resistance. The v_{gs}, i_d, and v_{ds} in the figure represent the gate-source voltage, drain current, and drain-source voltage of the device under test. With the rise of temperature, the turn-on process becomes faster, i.e. lower turn-on delay, shorter current rising time and voltage falling time. In sharp contrast, the turn-off switching transient presents the opposite trend. Those behaviors are attributed to the negative temperature coefficient of threshold voltage and positive temperature coefficient of transconductance of SiC MOSFETs at low gate voltages, as indicated in the transfer characteristic.

When the double pulse test function is used, the short-circuit control branch is removed, and the upper SiC MOSFETs are reversed biased. The entire power stage is placed in room ambient environment (25 °C), while only the power module is heated by a hotplate to various temperatures up to 225 °C.

During turn-on switching transient, a huge current peak is presented due to the rising *dv/dt* induced displacement current and a small amount of diode reverse recovery current of the upper switch position. With a larger gate resistance, *di/dt*, *dv/dt*, current peak, and current/voltage ringing will be reduced, while the switching loss will increase. A proper gate resistance should be selected based on these tradeoffs.

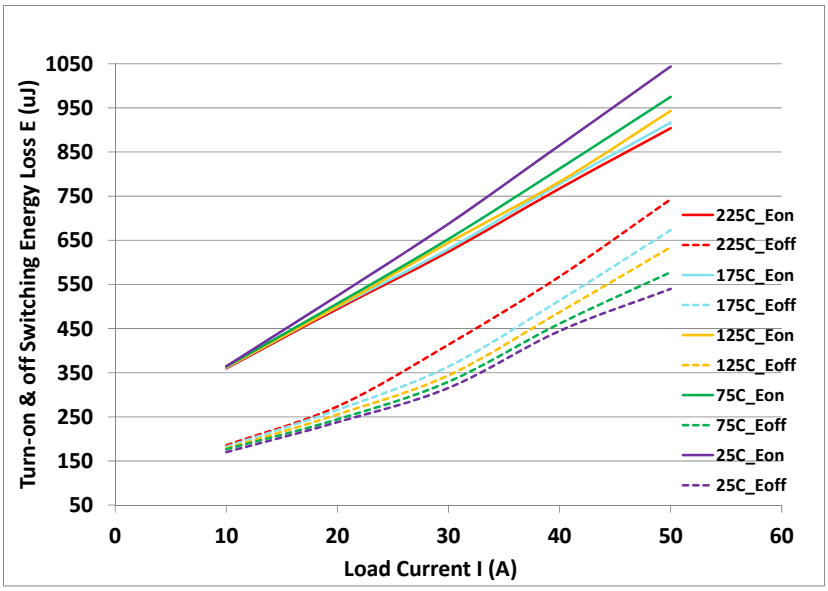
During turn-off transient, the power loop parasitic inductance resonates with the output capacitance of the low side switches, causing strong current and voltage ringing. For lower ringing, the parasitic parameters need to be reduced through circuit board layout optimization, power module packaging improvement, and better decoupling techniques.



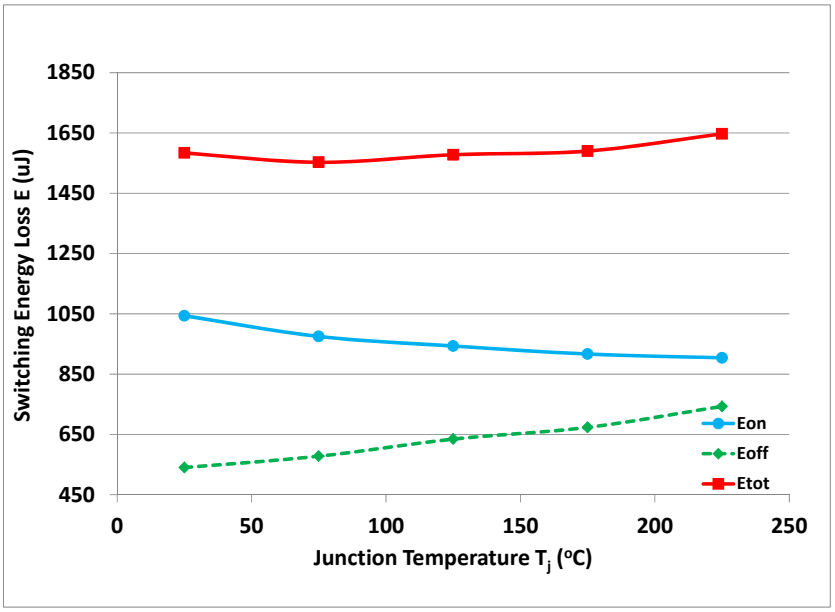
(a) Turn-on transient (b) Turn-off transient

Figure 4-9. Temperature dependent switching waveforms.

The turn-on switching energy loss E_{on} and turn-off switching energy loss E_{off} under different current and temperature levels are plotted in Figure 4-10(a). Both of them increases monotonously with current but show the opposite trend with temperature. A more clear representation is shown in Figure 4-10(b), with a current level of 50 A. E_{on} decreases with temperature and E_{off} increases with temperature, which together results in an almost constant total switching energy loss E_{tot} within the plotted temperature range. This temperature dependent feature would be beneficial for thermal stability under high temperature operation.



(a) Turn-on and off switching loss



(b) Total switching loss

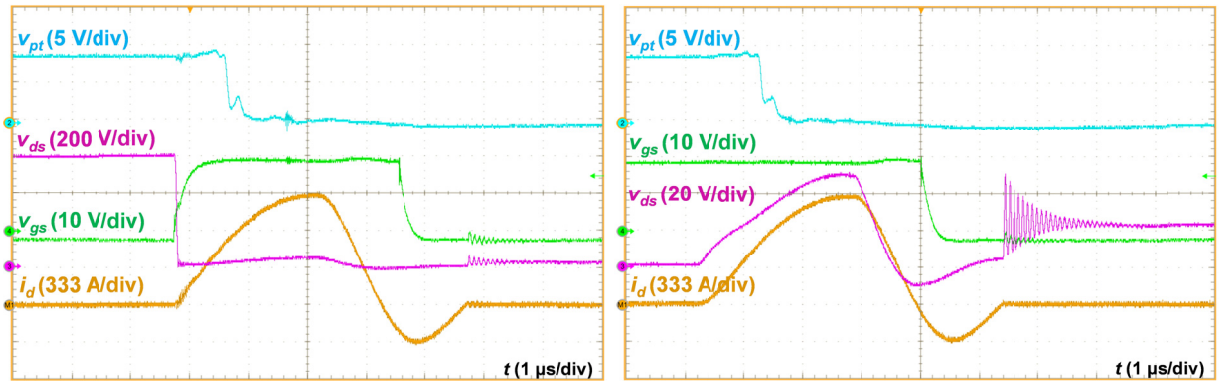
Figure 4-10. Temperature dependent switching energy loss.

4.2.4 Fault Characterization

The fault characterization is also carried out based on the multifunction power stage shown in Figure 4-7 and Figure 4-8. The short-circuit control switch, connected in parallel with the reverse-biased upper

SiC MOSFETs, is controlled to create a shoot-through fault when the lower device is on. Depending on the time sequence of the drive signals (v_{short} and v_{in} in Figure 4-7), the lower device could present overcurrent during the turn-on switching transient or during the on-state condition, resulting in hard switching fault (HSF) or fault under load (FUL) condition respectively. In this work, the integrated power module under both fault types will be evaluated, with the overcurrent protection of the solid state circuit breaker.

Figure 4-11(a) and (b) illustrate the testing results of the power module under HSF and FUL condition, with a 600 V DC bus voltage, 10 Ω gate resistance, 3.84 μF decoupling capacitance and 25 °C room temperature, where v_{pt} represents the protection signal of the solid state circuit breaker. On the occurrence of a short circuit fault, the drain current increases quickly. When the current flowing through the solid state circuit breaker reaches the predetermined protection threshold, it cuts off the energy storage capacitors C_{dc} after a short circuit of around 1 μs. However, the decoupling capacitance C_s continues discharging through the main power loop, resulting in a peak fault current as high as 1000 A. The fault current is gradually damped and cleared within 5 μs.

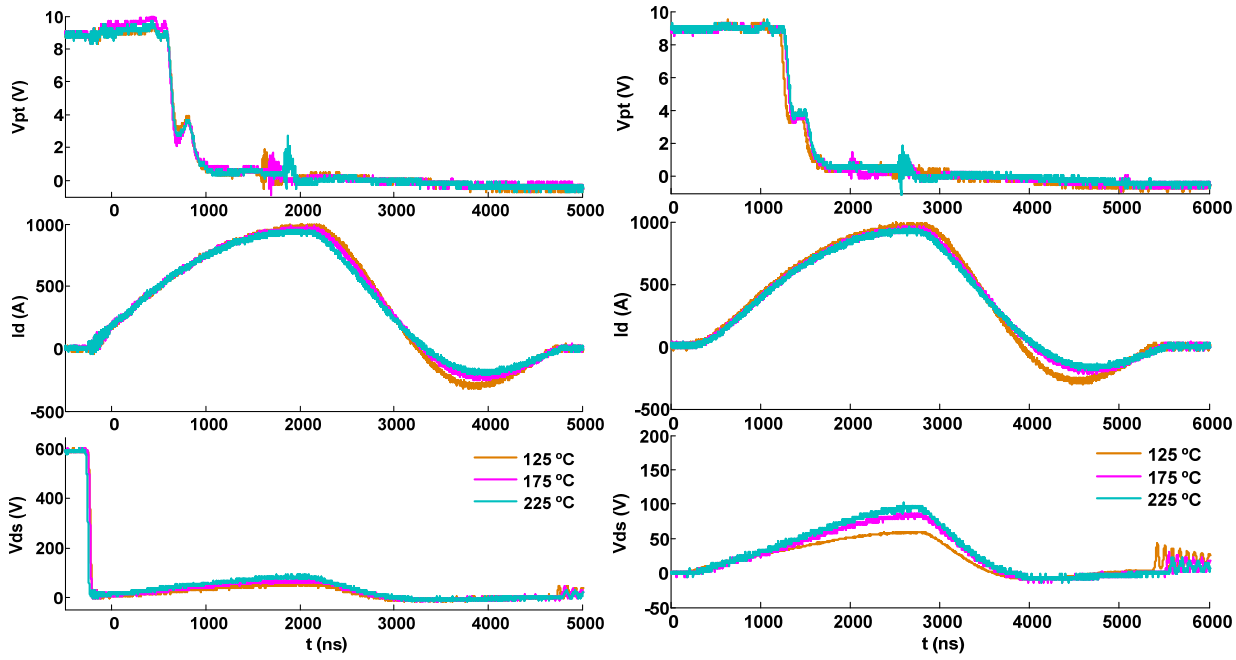


(a) HSF (b) FUL

Figure 4-11. Short circuit protection waveforms at room temperature (25 °C).

The fault characteristics at various temperatures up to 225 °C are also conducted, as shown in Figure 4-12. The temperature has nearly no influence on the overcurrent protection performance, except that the

short-circuit current peak decreases slightly due to the increase of $R_{ds(on)}$ at higher temperatures. Such a stable temperature behavior owes to the solid state circuit breaker that relies on its own power device instead of the SiC MOSFET power module subject to high temperature environment. The performance evaluation of the temperature dependent overcurrent protection guarantees the safe continuous operation of the integrated power module at elevated temperatures.



(a) HSF (b) FUL

Figure 4-12. Temperature dependent short circuit protection waveforms.

4.3 Power Density Limitation

According to the switching performance characterization in the previous section, it can be seen that both switching loss and conducting loss (or on-state resistance) are junction temperature dependent, which together cause a junction temperature rise. The power loss and junction temperature present a circular relationship, as shown in Figure 4-13.

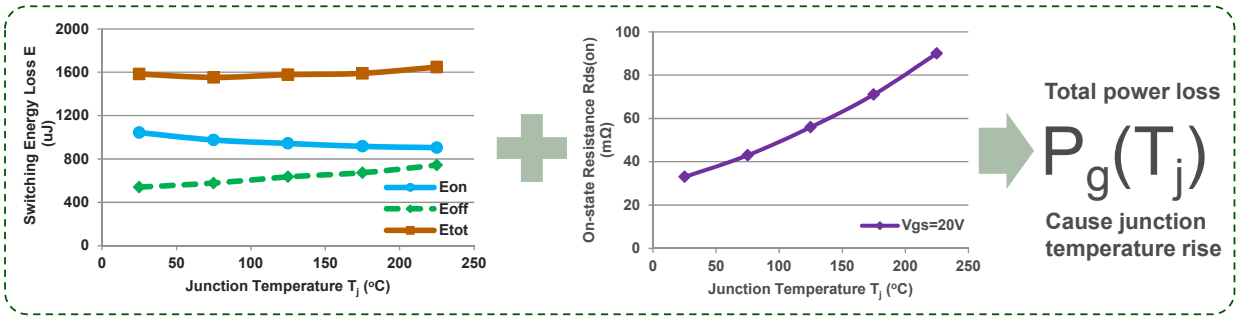


Figure 4-13. Temperature dependent power loss.

In order to increase the power density of a power module, one can either push more power into the power module while keeping the same heat sink size, or maintain the power while reducing the heat sink size. The subsequent questions are: (1) What is the maximum power that can be increased and largest heat sink volume that can be reduced? (2) What is the junction temperature limit?

Under thermal steady-state, the junction temperature is determined by the total power loss $P_{g1}(T_j)$ and the cooling system with a thermal resistance of R_{th1}, as shown in Figure 4-14. When the power loss is increased to $P_{g2}(T_j)$, or the thermal resistance is increased to R_{th2}, the steady-state junction temperature will increase correspondingly. However, under a certain condition, if the power loss is always higher than the power that can be dissipated by the cooling system, a thermal runaway issue occurs.

Under thermal steady-state, the following relationship can be obtained:

$$R_{on}(T_j) = \alpha_0 {T_j}^2 + \alpha_1 T_j + \alpha_2$$

$$E_{tot}(I) = \beta_0 I^2 + \beta_1 I + \beta_2$$

$$P_g(T_j, I) = I^2 \cdot R_{on}(T_j) \cdot D + E_{tot}(I) \cdot f_{sw}$$

$$P_s(T_j) = (T_j - T_a)/R_{th} \qquad (4-1)$$

$$P_g(T_j, I) = P_s(T_j)$$

$$\frac{\partial P_g(T_j, I)}{\partial T_j} \leq \frac{\partial P_s(T_j)}{\partial T_j}$$

Solution for the above equations yields:

$$T_a \le T_j \le \frac{\alpha_0(T_a + E_{tot}(I)f_{sw}R_{th}) + \sqrt{\alpha_0{}^2(T_a + E_{tot}(I)f_{sw}R_{th})^2 + \alpha_0\alpha_1(T_a + E_{tot}(I)f_{sw}R_{th}) + \alpha_0\alpha_2}}{\alpha_0}. \quad (4-2)$$

For a given ambient temperature T_a, the lowest thermal runaway temperature can be achieved under pure conduction state, i.e.

$$E_{tot}(I)f_{sw}R_{th} = 0\,. \quad (4-3)$$

Minimum thermal runaway temperature becomes

$$T_{j(runaway)\_min} = \frac{\alpha_0 T_a + \sqrt{\alpha_0{}^2 T_a{}^2 + \alpha_0\alpha_1 T_a + \alpha_0\alpha_2}}{\alpha_0}\,. \quad (4-4)$$

It can be seen that the minimum thermal runaway temperature is only related with device on-resistance characteristic and ambient temperature.

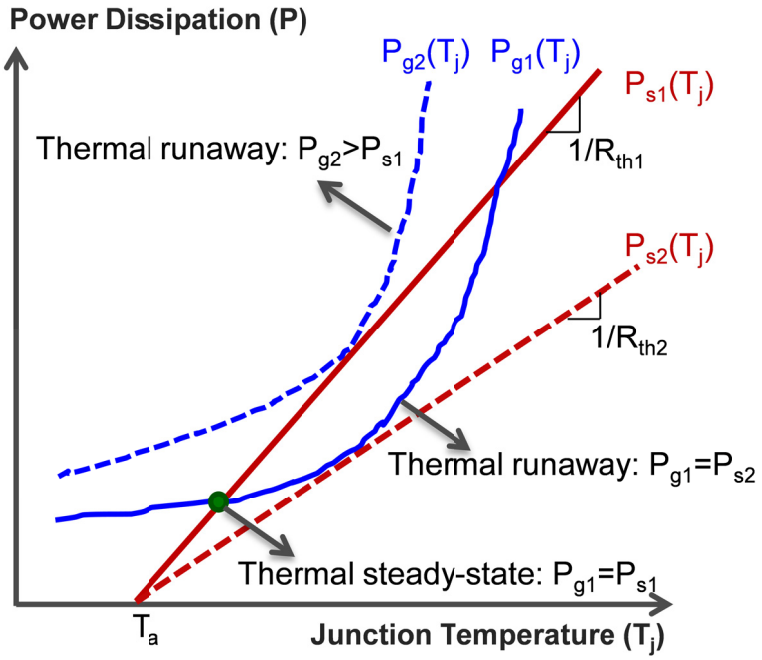


Figure 4-14. Thermal runaway issue caused by increased power and/or thermal resistance.

Based on the derived relationship, the thermal runaway temperatures under different operating conditions are plotted in Figure 4-15. As can be observed, the power density improvement becomes exponentially less at higher junction temperatures. The minimum thermal runaway temperature is achieved under pure conduction mode and is independent of cooling conditions. The low thermal resistance, i.e. better cooling conditions, is beneficial for higher power density but is not helpful to realize a higher thermal runaway temperature.

To verify the junction temperature limitation, thermal simulation has been conducted for the developed power module under different ambient and cooling conditions, as shown in Figure 4-16. The thermal performance of a commercial SiC JFET is also evaluated under pure conduction state. From the simulation comparison, the thermal runaway temperature increases with ambient temperature, but is independent of thermal resistance. The thermal runaway temperature is around 260 ^{o}C, which matches with the calculated value in Figure 4-15. In addition, SiC MOSFETs tend to present a higher thermal runaway temperature than SiC JFETs since their on-resistance is relatively less sensitive to the rise of junction temperature.

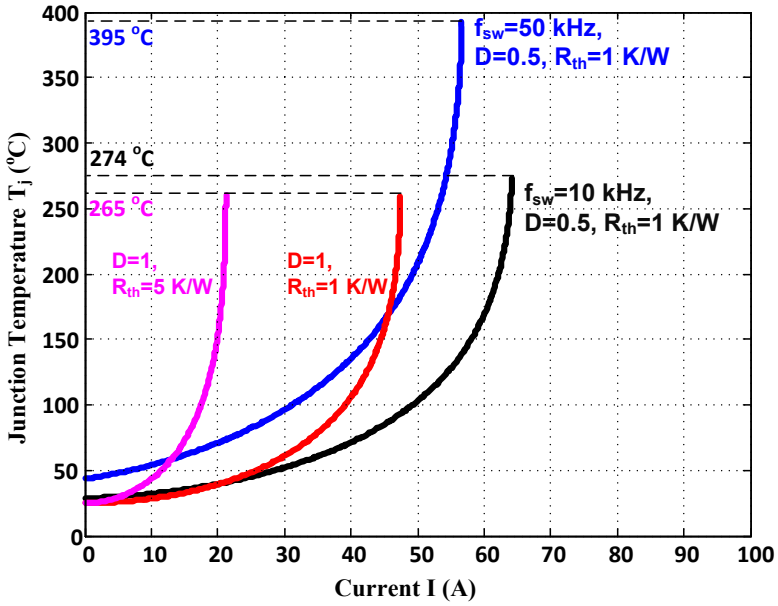


Figure 4-15. Thermal runaway temperature under different operating conditions.

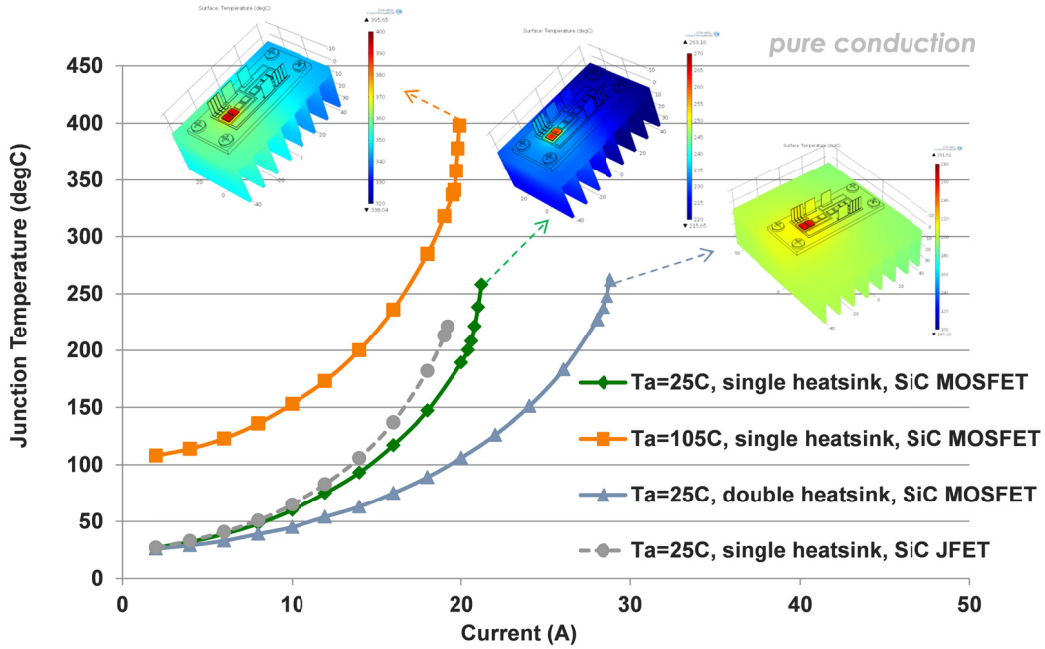


Figure 4-16. Thermal simulation verification of thermal runaway temperatures.

4.4 High Temperature Continuous Operation

A buck converter based on the multifunction power stage is used to demonstrate the high temperature capability of the power module. Low conduction loss (10 A) and high switching loss (100 kHz) strategy is adopted to prevent thermal runaway issue under high temperature operation.

Before hardware implementation and operation, the thermal performance of the power module is evaluated through thermal simulation. Also, a proper temperature measurement method is necessary for real-time junction temperature monitoring.

4.4.1 Thermal Simulation

The buck converter is assumed to operate at a 600 V input DC bus voltage, 10 A load current, 0.25 duty-cycle. The gate resistance is still 10 Ω so that the switching loss obtained from the above switching characterization can be directly used for power loss calculation. The power losses of each part within the power module are calculated under different switching frequencies. The switching loss of the low-side SiC MOSFETs, around 54 W at 100 kHz, dominates the total loss of the power module.

While the whole power module is heated to 225 °C for static and dynamic characterization, under continuous operation the junction temperatures of each die within the power module are different due to uneven power losses. As with [43], [47], [50], the junction temperature of the device under test, i.e., the low-side SiC MOSFET, is selected to verify the feasibility of the high temperature packaging technology.

The power loss will heat up the module and the steady-state junction temperature depends on the cooling system. Given that the objective of the continuous operation test is to verify the high temperature capability of the integrated power module, the cooling system is not specifically designed and optimized. In this work, an aluminum alloy heatsink with natural air convection is applied to the integrated power module, with an ambient temperature of 25 °C.

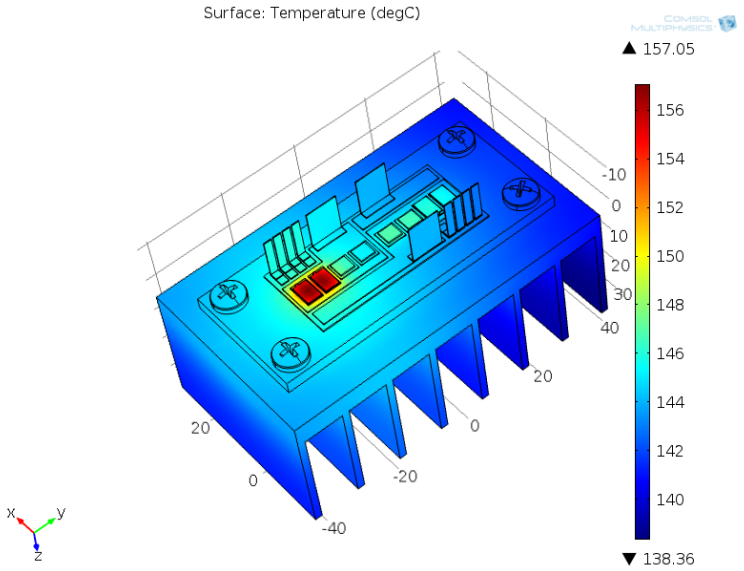
In order to determine a proper heatsink size and evaluate the temperature distribution of the power module, finite element simulation based on the multiphysics software COMSOL™ has been carried out. The 3D geometry model of the assembly is built in SolidWorks®, and then imported into COMSOL™ through the interface software – LiveLink™, enabling a real time interactive simulation environment. Materials of the 3D model are set according to the fabricated power module. The power losses of each part are applied to the corresponding dies as heat sources.

The thermal simulation results with switching frequencies of 50 kHz and 100 kHz are shown in Figure 4-17(a) and (b), respectively. The hottest point appears in the middle area of the low-side SiC MOSFETs due to high power loss and poor cooling conditions. The junction temperature of the low-side SiC MOSFET reaches 157 °C at 50 kHz, and 238 °C at 100 kHz under continuous operation.

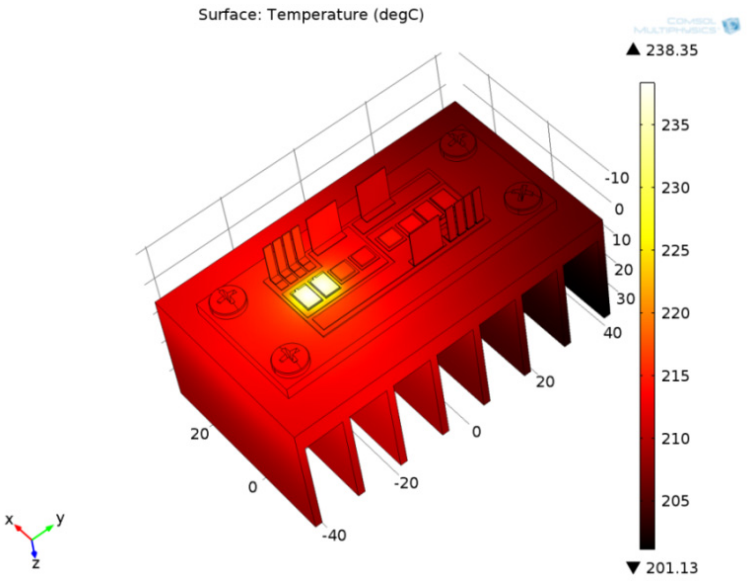
4.4.2 Junction Temperature Measurement

The junction temperature should be monitored during the converter operation. An infrared thermal camera is inappropriate considering that the power module is perpendicularly covered by its gate driver and the emissivity decreases with an increasing viewing angle. Moreover, uniform emissivity is difficult to be achieved due to the encapsulation material of the power module. The widely used thermocouple needs mechanical access to the die during module fabrication, and can be only embedded on the substrate.

The temperature difference from junction to the bottom pad of the die may induce fairly large measurement errors.



(a) 50 kHz buck operation



(b) 100 kHz buck operation

Figure 4-17. Temperature distribution by thermal simulation.

In this study, a thermo-sensitive electrical parameter (TSEP) is proposed for the junction temperature measurement. Based on the switching characterization shown in Figure 4-9, the turn-on / off delay, current rising / falling time, and voltage falling / rising time are all functions of temperature. Among those candidates, the turn-off delay time $t_{d(off)}$, defined as the time interval between the moment when the gate-source voltage falls to 90% of its initial value and the drain-source voltage rises to 10 % of the blocking voltage, is selected for the temperature measurement due to its high sensitivity and good linearity.

The relationship between the turn-off delay time $t_{d(off)}$ and the junction temperature T_j should be determined through calibration prior to real application. The calibration circuit and continuous operation circuit are kept the same (except for different loads and heating methods) to avoid any hardware induced calibration error. Furthermore, the current and voltage probes are also the same. The turn-off delay time can be estimated as

$$t_{d(off)} \approx R_g C_{iss} ln\left(\frac{V_{cc}-V_{ee}}{V_{th}+I_L/g_m-V_{ee}}\right) \quad (4-5)$$

where, R_g is the gate resistance; C_{iss}, V_{th} and g_m represent the input capacitance, threshold voltage and transcondutance of the SiC MOSFET, respectively; V_{cc} and V_{ee} are the positive and negative gate voltage level; I_L is the load current.

The gate resistance and gate voltage levels are constant values (R_g = 10 Ω, V_{cc} = 20 V and V_{ee} = -2 V), while the others are DC bus voltage, load current and/or junction temperature dependent variables. In order to simplify the calibration efforts, the DC bus voltage is set to 600 V for both the calibration circuit and the continuous operation circuit. The calibration process is carried out under different temperature points (25 °C, 75 °C, 125 °C, 175 °C, 225 °C) and current points (10 A, 20 A, 30 A, 40 A, 50 A), as shown in Figure 4-18. The turn-off delay time increases with temperature due to the reduced threshold voltage and increased transconductance, while it decreases with load current thanks to the increased miller plateau voltage.

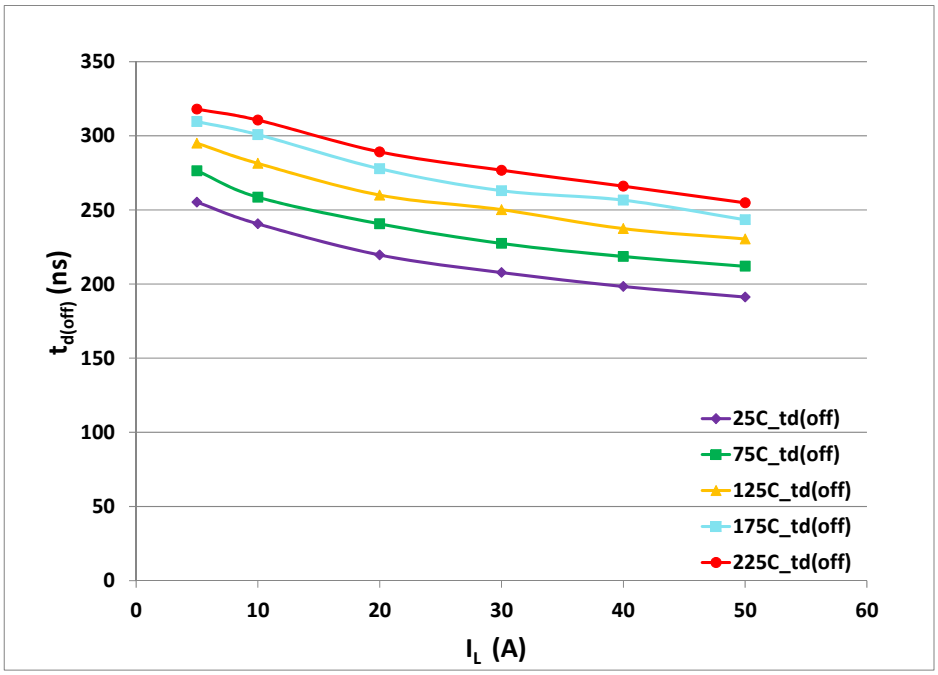


Figure 4-18. Calibration curves under different load current levels and junction temperatures.

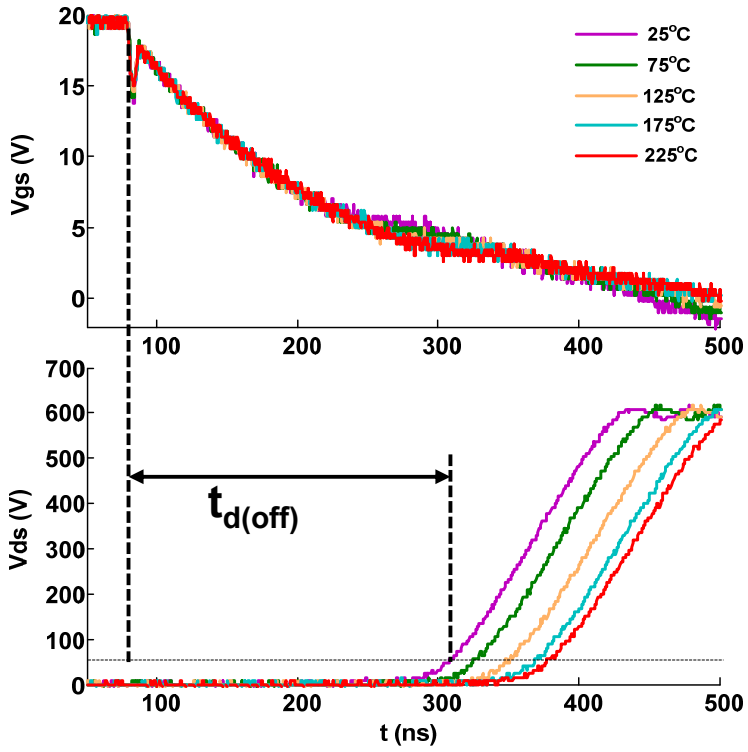


Figure 4-19. Turn-off waveforms under different junction temperatures.

Figure 4-19 illustrates the turn-off transients of the power module under various temperatures with 600 V DC bus voltage, 10 A load current, and 10 Ω gate resistance. The turn-off delay time is extracted and summarized in Figure 4-20. The data points are linearized by the curve-fitting toolbox in MATLAB.

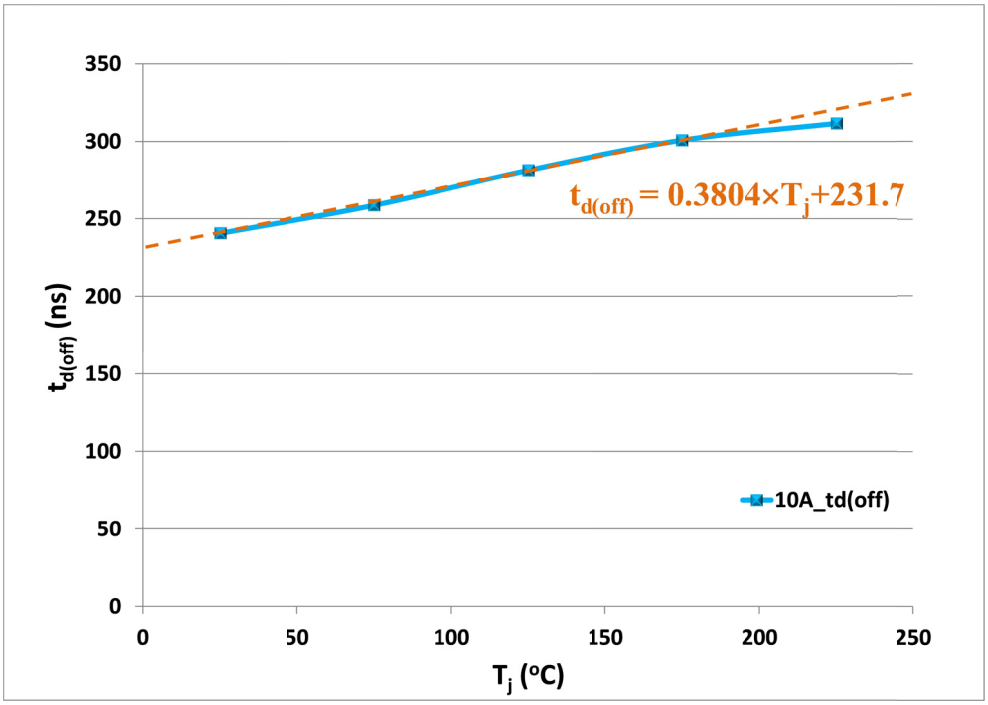


Figure 4-20. Calibration curve with 10 A load current.

4.4.3 Buck Converter Operation

The buck converter is built through the reconfiguration of the multifunction power stage. Specifically, the short-circuit control branch is removed, the upper SiC MOSFETs are reversed biased, and the pure inductive load is replaced by a LRC load. The LC filter is composed of an inductor of 0.75 mH and a capacitor of 20 μF. The equivalent resistive load is around 18 Ω. The buck converter is operated at 600 V input DC bus voltage, 0.25 duty-cycle, the same condition used for thermal simulation. The power level achieved by the buck converter (about 1.25 kW) is much lower than the rated power because the objective of this work is to verify the high temperature capability through power module selfheating. The hardware

test setup for buck continuous operation is shown in Figure 4-21, where the integrated power module is mounted on a heatsink with the dimensions obtained from thermal simulation.

The switching frequency is gradually pushed from 10 kHz to 100 kHz to heat the power module above 225 °C. The continuous power test at each switching frequency point lasts for 30 minutes to reach the steady state. The junction temperature at each step is compared with the corresponding thermal simulation results to ensure the safe operation of the test setup. Figure 4-22(a) and (b) illustrates the waveforms of buck operation at a switching frequency of 50 kHz and the zoomed-in turn-off transient. The measured turn-off delay time is 293 ns, which corresponds to a junction temperature of 161 °C according to the calibration curve shown above. Further increase in the switching frequency to 100 kHz results in a turn-off delay of 320 ns, i.e. a junction temperature of 232 °C, as shown in Figure 4-23.

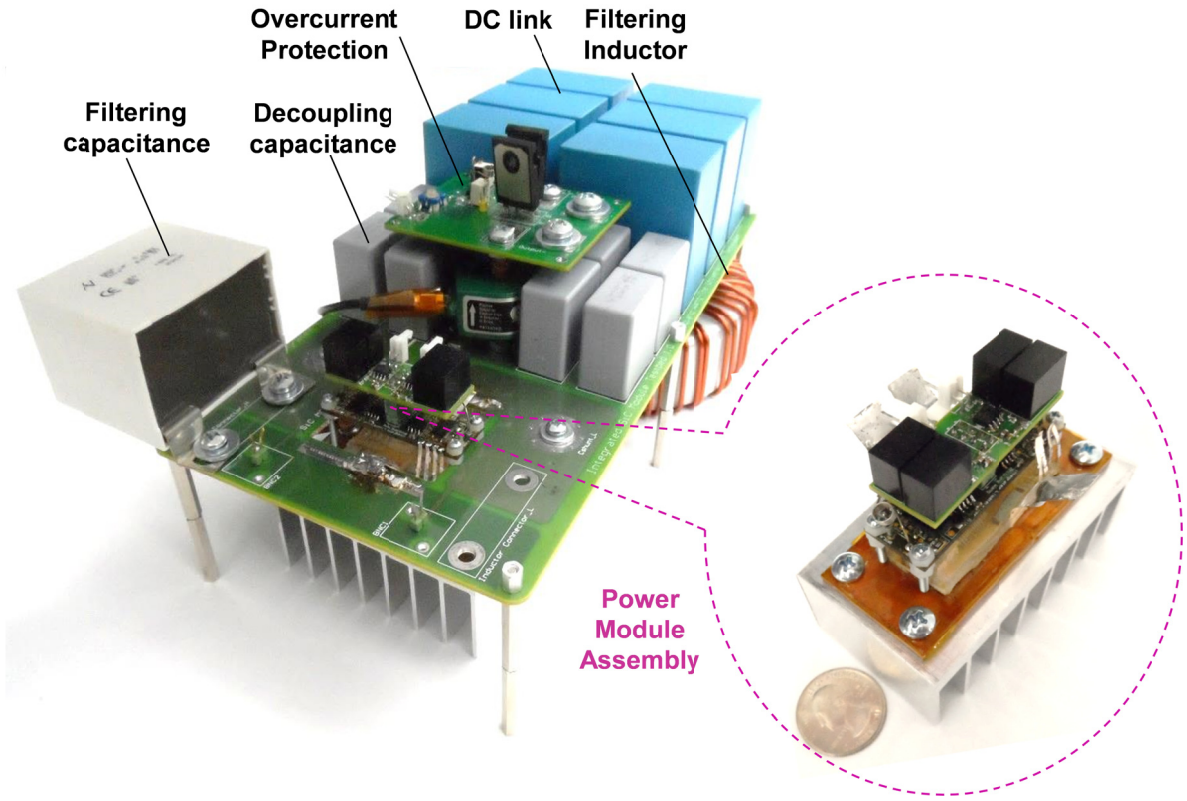
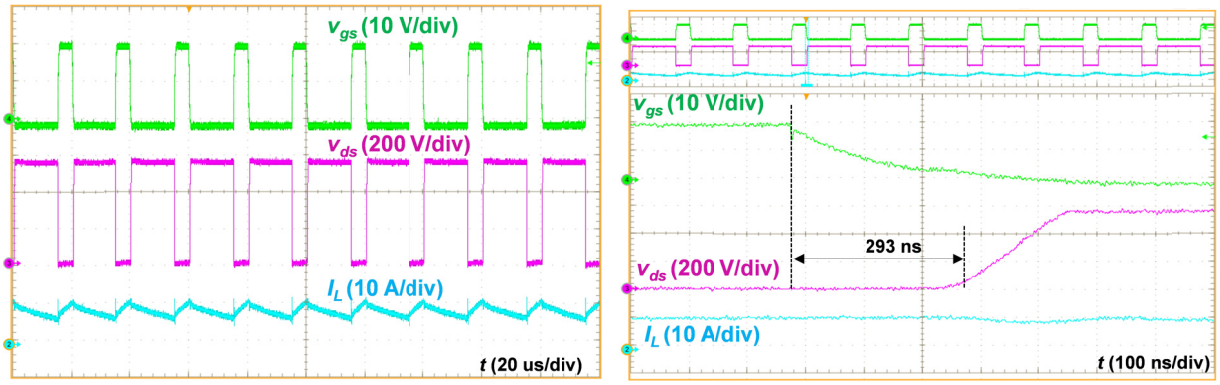
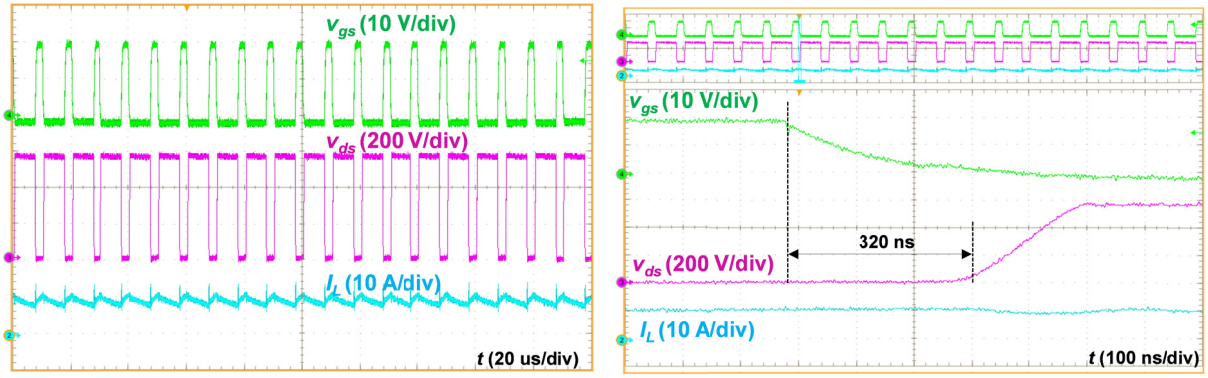


Figure 4-21. Hardware test setup for buck converter operation.



(a) Continuous waveform (b) Turn-off transient

Figure 4-22. Buck operation at a switching frequency of 50 kHz.



(a) Continuous waveform (b) Turn-off transient

Figure 4-23. Buck operation at a switching frequency of 100 kHz.

4.5 Conclusion

In this chapter, the design, development, and testing of a high temperature silicon carbide MOSFET power module with an integrated silicon-on-insulator based gate drive have been presented. A two-channel high temperature gate driver board is built based on the chip-on-board technique. In addition, a silicon carbide MOSFET phase-leg module is fabricated utilizing high temperature packaging technologies. The static characteristics, switching performance, and short-circuit behavior of the power module have been evaluated at different temperatures. The evaluation results show that the power module

is preferable for high temperature operation thanks to its low leakage current, small variation in total switching loss, positive temperature coefficient of on-state resistance, etc. A buck converter prototype incorporating the phage-leg power module and the silicon-on-insulator gate drive is operated successfully at a switching frequency of 100 kHz. The junction temperatures are 238 °C according to finite element thermal simulation and 232 °C based on the proposed thermo-sensitive electrical parameter measurement method, which together demonstrates the high temperature capability of the power module through continuous operation.

The junction temperature limitation of the fabricated power module related to thermal runaway phenomenon is investigated. Theoretical and thermal simulation results demonstrate that:

(1) The power density improvement becomes exponentially reduced by pushing junction temperatures.

(2) The minimum thermal runaway temperature is around 265 ^{o}C, which is lower than the solder melting point

(3) The lowest thermal runaway temperature is independent of device scaling and external cooling condition, while increases with ambient temperature

(4) SiC MOSFETs tend to present a higher thermal runaway temperature than SiC JFETs thanks to their negative temperature coefficient effect of MOS-channel resistance

(5) With the same total power loss, less conduction loss is beneficial to prevent the thermal runaway issue.

5 Short Circuit Capability Evaluation of SiC MOSFETs

This chapter presents a comprehensive short circuit ruggedness evaluation of up-to-date commercial SiC MOSFETs. The short circuit capability of three types of commercial 1200 V SiC MOSFETs is tested under various case temperatures from 25 °C to 200 °C. The short circuit behavior and associated failure mechanism are also compared and analyzed through transient thermal simulation.

5.1 Evaluation Methodology and Hardware Test Setup

Three commercially available discrete 1200 V SiC MOSFETs with TO-247 package are investigated in this work, as shown in Table 5-1. These devices have the same on-state resistance and comparable current rating, while their die sizes are different.

Table 5-1. SiC MOSFETs under test [93]-[96]

Device / Types / Parameters	CREE		ROHM SEMICONDUCTOR
	1st Generation (1G)	**2nd Generation (2G)**	
Rated Voltage / Current	1200 V / 24 A (100 °C)	1200 V / 20 A (100 °C)	1200 V / 28 A (100 °C)
On-Resistance	80 mΩ	80 mΩ	80 mΩ
Normalized Die Area	1.59	1.0	1.21

The test circuit configuration for short circuit capability and protection evaluation is shown in Figure 5-1, which represents one phase leg of a three phase voltage source converter with a clamped inductive load. The inductances L, L_{σ}, and L_{fa} are the load inductance, main-loop parasitic inductance, and short-circuit impedance, respectively. The lower side device serves as the device under test (DUT). The short-circuit control switch in Figure 5-1, connected in parallel with the upper SiC MOSFETs (always off for the inductor current free-wheeling through its body diode), is controlled to create a short circuit fault

when the lower device is on. In order to prevent the potential damage of the whole test setup when the DUT fails, a solid state circuit breaker with a proper short circuit protection threshold is employed, as discussed in detail later.

Depending on the time sequence of the drive signals (v_{short} and v_{in} in Figure 5-1), the DUT could present a short circuit during the turn-on switching transient or during the on-state condition, resulting in hard switching fault (HSF) or fault under load (FUL) respectively. The detailed analysis of the short circuit behavior of the two fault types is given in [92]. In this work, the short circuit capability under both fault types will be evaluated.

The experimental test setup is shown in Figure 5-2. A two channel synchronous waveform generator sends one signal (v_{in}) to the gate driver of the DUT, and the other one (v_{short}) to the gate driver of the short-circuit control switch. To test its temperature dependent characteristics, the DUT is heated by a controlled hot plate at the bottom side of the test board, and the case temperature is monitored by a thermocouple. A fan is used to cool the current sensor and gate driver loop to guarantee measurement accuracy. Testing waveforms can be extracted by MATLAB for performance comparison under different conditions and/or transient thermal analysis.

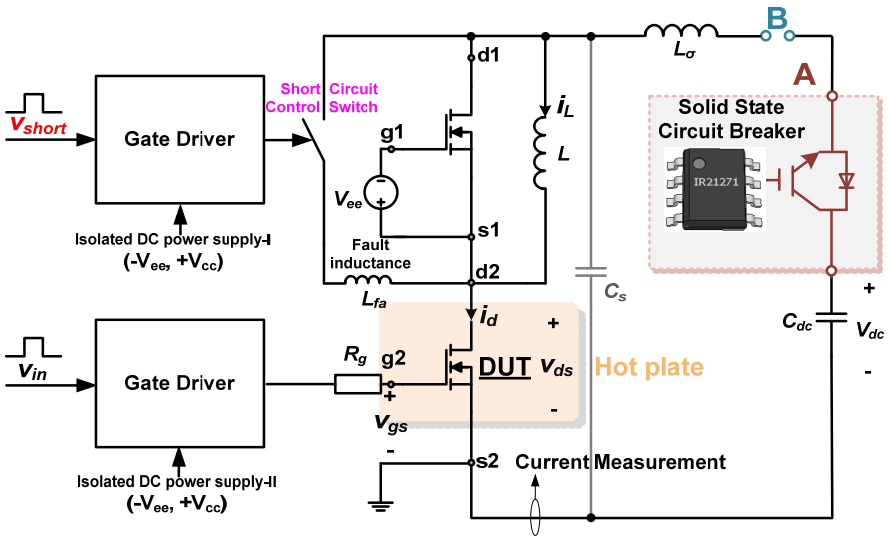


Figure 5-1. Test circuit configuration for short circuit capability and protection evaluation.

The hardware testbed is shown in Figure 5-3. The SiC MOSFET phase-leg configuration and DC capacitor bank are connected by an internal planar busbar structure within the test board. The SSCB, desaturation technique, and short-circuit control board are integrated together with the main power testing circuit. When one protection scheme is tested, the other is deactivated to eliminate their interaction.

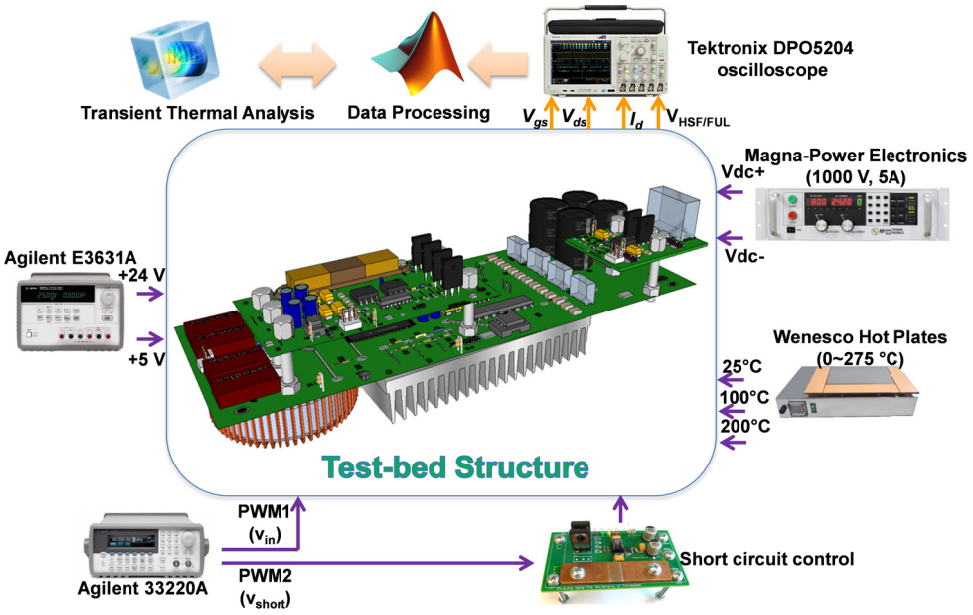


Figure 5-2. Experimental test and measurement setup.

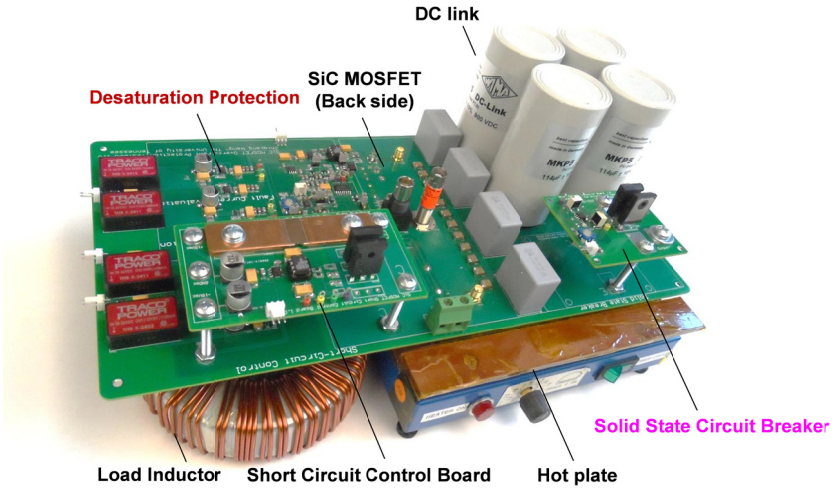


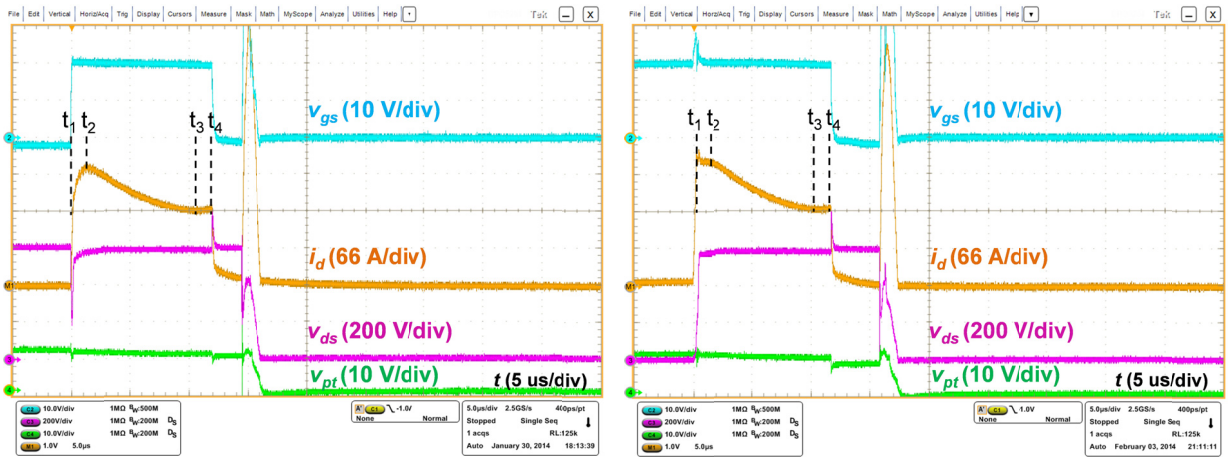
Figure 5-3. Hardware testbed for short circuit capability and protection evaluation.

5.2 Short Circuit Capability Evaluation

The short circuit capability testing results of the three SiC MOSFETs listed in Table 5-1 are presented as follows.

5.2.1 CREE 1G SiC MOSFETs

Figure 5-4(a) and (b) show the short circuit transient waveforms of the CREE 1G SiC MOSFETs under HSF and FUL condition, with DC bus voltage V_{dc} = 600 V, gate voltage v_{gs} = + 20 / - 2 V, and case temperature T_c = 25 ºC, where v_{ds}, i_d, and v_{pt} are the drain-source voltage, drain current of the DUT, and the protection signal from the SSCB, respectively. The overall short circuit behavior under both fault types is similar and can be divided into four stages.



(a) HSF (b) FUL

Figure 5-4. Short circuit capability of CREE 1G SiC MOSFET with V_{dc} = 600 V and T_c = 25 ºC.

Stage I [$t_1 \sim t_2$]: When a short circuit occurs at t_1, the drain current increases quickly due to small inductance in the main power loop. Meanwhile, the device enters from linear region to active region, with a saturated drain-source voltage close to the DC bus voltage. The current keeps increasing in this stage due to positive temperature coefficient of MOS channel mobility up to 600 K [97].

Stage II [$t_2 \sim t_3$]: The device conducts in saturation as the full DC bus voltage appears across it. This involves considerable power loss, and as a consequence the semiconductor junction temperature increases rapidly due to self-heating. The temperature rise leads to reduction in the MOS channel (and drift region) carrier mobility, and thus the short circuit current presents a negative slope. The device can be successfully turned off if the semiconductor temperature is within safe range.

Stage III [$t_3 \sim t_4$]: As junction temperature continues increasing, the *di/dt* of the short circuit current waveform changes to be positive. This is likely because the decreasing rate of MOS channel electron current is lower than the rising rate of leakage current induced by thermally assisted impact ionization.

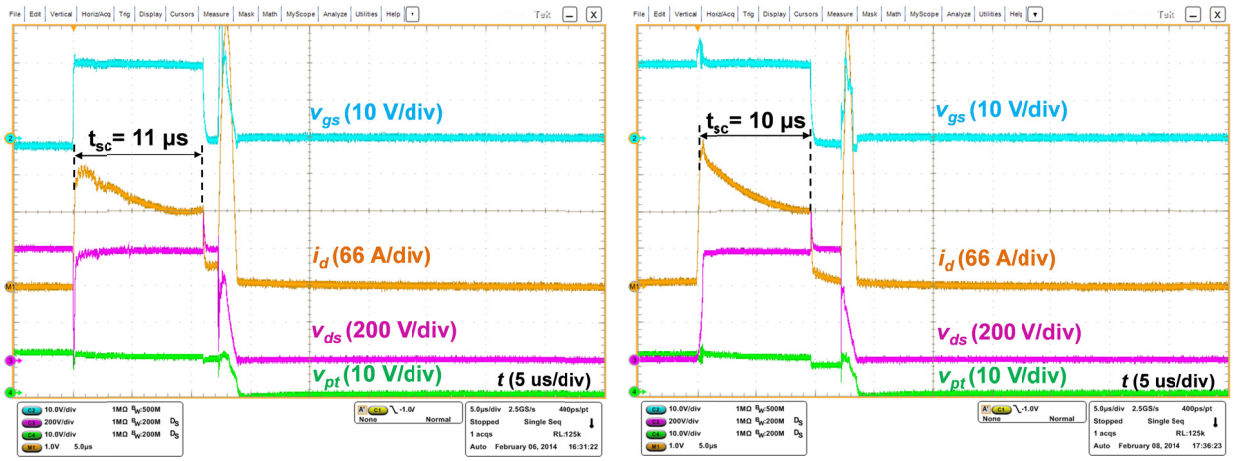
Stage IV [$t_4 \sim$]: When the device is switched off at t_4, a tail leakage current remains after the turn-off process and eventually leads to a thermal runaway phenomenon and device failure. This failure mode, occurring after a delay time from the device turn-off, has been reported by some authors in Si field-stop IGBTs [98].

The short circuit withstand time (from t_1 to t_4) is 12 μs under HSF, and 11.5 μs under FUL. The slightly lower SCWT for FUL is associated with the higher peak fault current caused by a gate voltage spike during the fault transient. The short circuit critical energy E_c, defined by (5-1), is around 1.18 J for both cases.

$$E_c = \int_{t_1}^{t_4} V_{ds} \cdot I_d \, dt. \qquad (5-1)$$

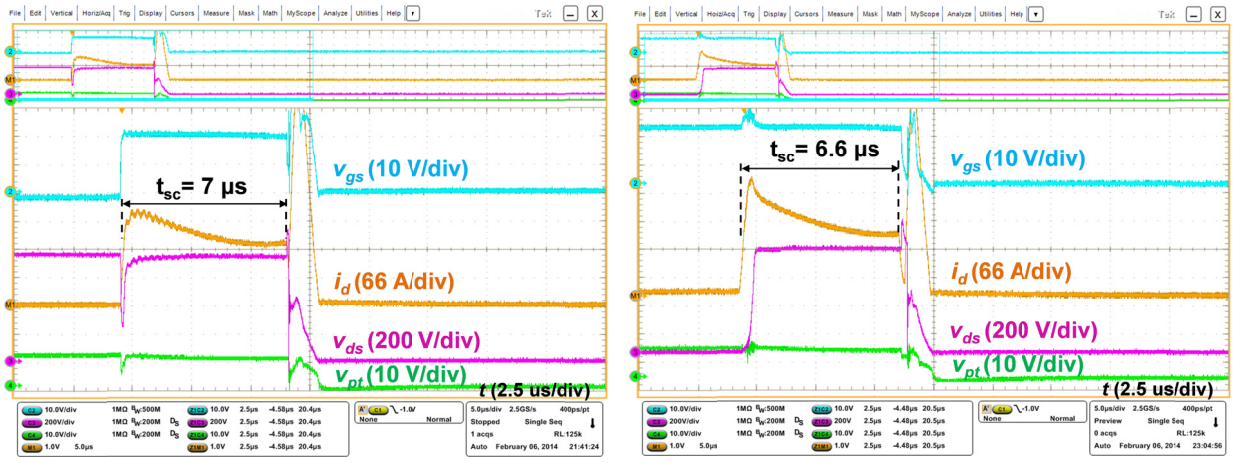
The high temperature short circuit capability of the CREE 1G SiC MOSFETs is also evaluated with DC bus voltage V_{dc} = 600 V, gate voltage v_{gs} = + 20 / - 2 V, and case temperature T_c = 200 ºC, as shown in Figure 5-5. Compared to Figure 5-4, several observations can be made regarding the current waveforms: 1) the SCWT decreases slightly from 12 μs (25 ºC) to 11 μs (200 ºC) under HSF, and 11.5 μs (25 ºC) to 10 μs (200 ºC) under FUL; 2) the peak fault current point (occurring at time t_2) moves towards fault starting moment (at t_1); 3) the delay time to failure becomes shorter.

The CREE 1G SiC MOSFETs are further tested at an elevated voltage level, V_{dc} = 750 V, while keeping other conditions the same as Figure 5-5. As shown in Figure 5-6, the SCWT is significantly reduced to 7 µs under HSF and 6.6 µs under FUL due to higher dissipated short circuit energy. Moreover, the device immediately fails after turn-off.



(a) HSF (b) FUL

Figure 5-5. Short circuit capability of CREE 1G SiC MOSFETs with V_{dc} = 600 V and T_c = 200 ºC.



(a) HSF (b) FUL

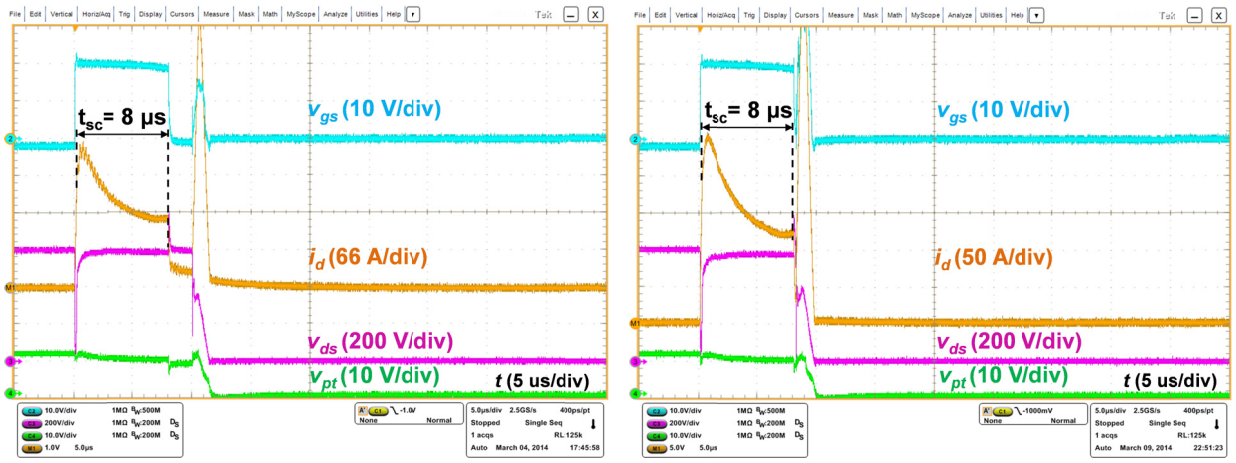
Figure 5-6. Short circuit capability of CREE 1G SiC MOSFETs with V_{dc} = 750 V and T_c = 200 ºC.

5.2.2 CREE 2G SiC MOSFETs

The short circuit capability of the second generation SiC MOSFETs from CREE has also been evaluated using the power stage in Figure 5-1. Given that HSF and FUL have nearly the same short circuit characteristics, only HSF testing results are presented hereafter.

Figure 5-7(a) and (b) show the HSF short circuit transient waveforms under case temperatures of 25 ºC and 200 ºC respectively, with DC bus voltage V_{dc} = 600 V and gate voltage v_{gs} = + 20 / - 2 V. The overall short circuit behavior is the same as 1G SiC MOSFETs, while the SCWT becomes much shorter. A scrutiny of the waveforms reveals that the SCWT is almost inversely proportional to the die size, i.e., 1G die size / 1G SCWT ≈ 2G die size / 2G SCWT. Moreover, the SCWT stays unchanged at different case temperatures, which is around 8 µs.

The CREE 2G SiC MOSFETs are further tested at a higher stress condition, with a DC bus voltage of 750 V and case temperature of 200 ºC. As can be observed in Figure 5-8, the SCWT is as low as 5 µs, which is quite challenging for the design of protection circuits.



(a) 25 ºC (b) 200 ºC

Figure 5-7. Short circuit capability of CREE 2G SiC MOSFETs under different case temperatures when V_{dc} = 600 V.

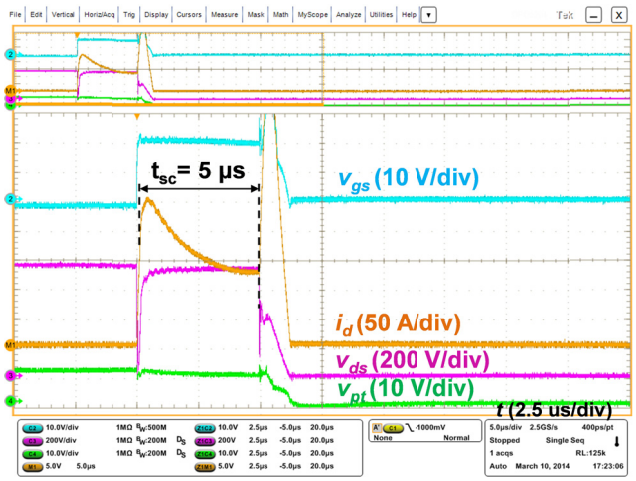
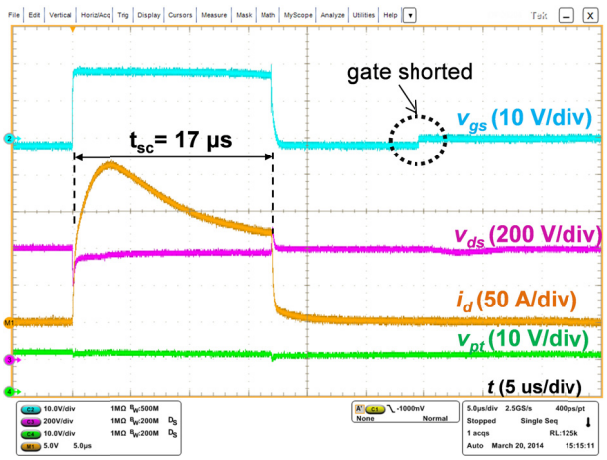


Figure 5-8. Short circuit capability of CREE 2G SiC MOSFET with V_{dc} = 750 V and T_c = 200 ºC.

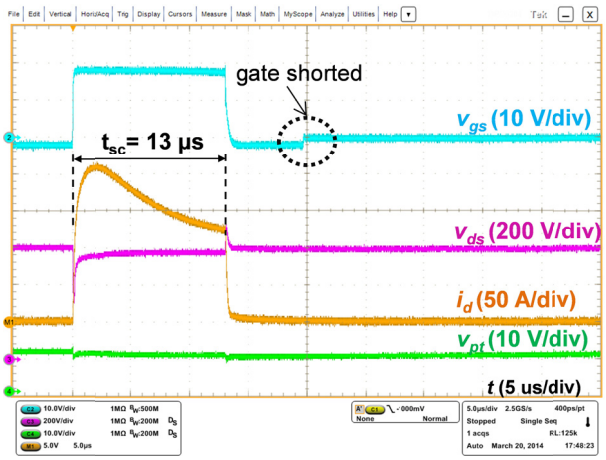
5.2.3 ROHM SiC MOSFETs

Short circuit tests have been conducted for the SiC MOSFETs from ROHM. The positive gate bias is set at 18 V, as recommended by the device manufacturer [99]. Figure 5-9(a) and (b) show the HSF short circuit transient waveforms under case temperatures of 25 ºC and 200 ºC respectively, with DC bus voltage V_{dc} = 600 V and gate voltage v_{gs} = + 18 / - 2 V. The short circuit behavior before device turn-off is similar to that of the CREE SiC MOSFETs; however, the SCWT is much longer. Different from the CREE devices, while the drain current can be successfully switched off, the gate and source terminals are shorted together after a delay following device turn-off.

In order to identify the key limiting factor, the ROHM SiC MOSFETs are further tested at a higher DC bus voltage (750 V) and positive gate bias (20 V), while keeping the case temperature constant at 200 ºC. As shown in Figure 5-10, the devices still present a delayed failure at the gate-source junction. The SCWT is around 10 µs at V_{dc} = 750, which is higher than the CREE 1G and 2G SiC MOSFETs. Nevertheless, the SCWT is close to that of the CREE 1G SiC MOSFETs when the positive gate bias is increased to 20 V.

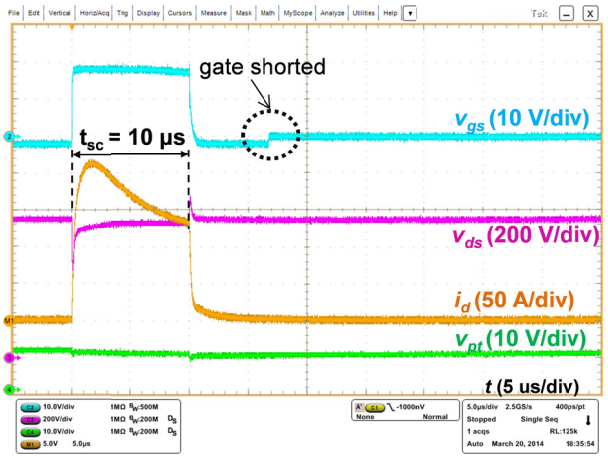


(a) 25 ºC

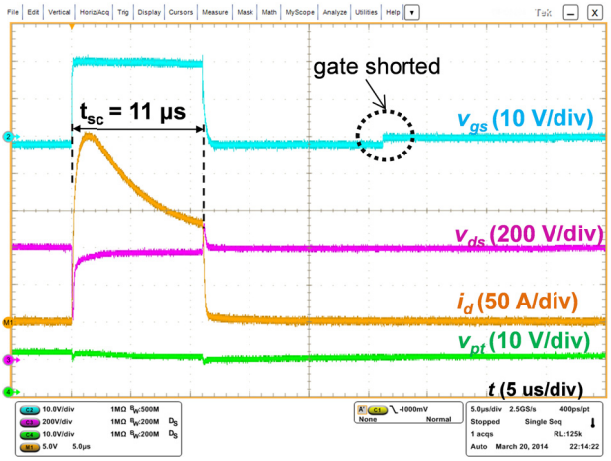


(b) 200 ºC

Figure 5-9. Short circuit capability of ROHM SiC MOSFETs under different case temperatures when V_{dc} = 600 V.



(a) V_{dc} = 750 V and v_{gs} = + 18 / - 2 V



(b) V_{dc} = 600 V and v_{gs} = + 20 / - 2 V

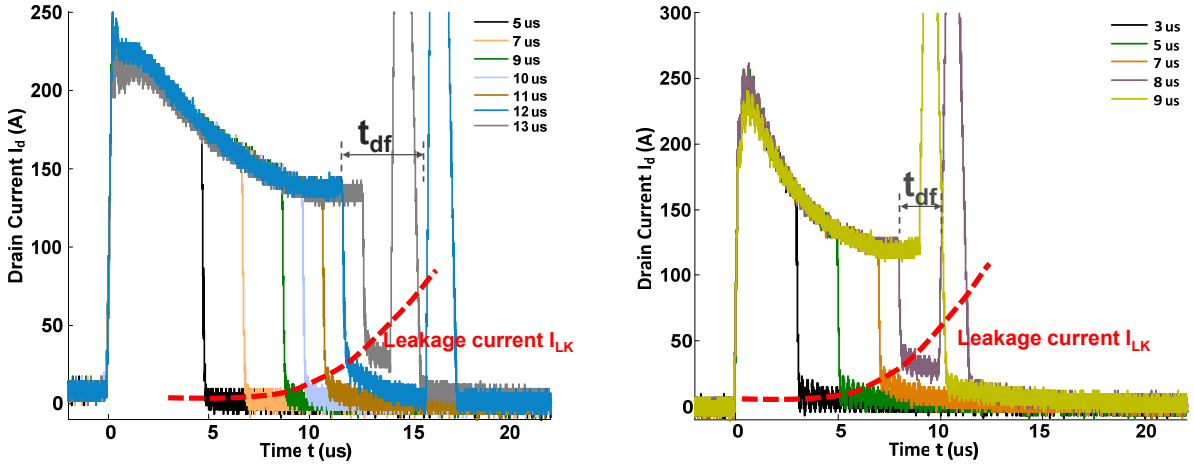
Figure 5-10. Short circuit capability of ROHM SiC MOSFETs with T_c = 200 ºC.

5.3 Comparison and Analysis

The short circuit capability testing results of the three SiC MOSFETs are compared in terms of their delayed failure mode, short circuit withstand time / energy, and transient thermal performance.

5.3.1 Delayed Failure Mode

According to the experimental results, both the CREE 1G and 2G devices present a delayed failure mode. In order to further investigate the evolution of the failure mode, the short circuit duration is gradually increased until the failure of the power device, as illustrated in Figure 5-11. When the device is turned off, the initial leakage current I_{LK} gradually increases with the extension of short circuit duration. Once the leakage current is large enough, the internal thermal instability after device turn-off occurs following a delay time (depending on heat diffusion), which eventually leads to a thermal runaway. Moreover, the delay time to failure t_{df} is short circuit duration or energy dependent. With the increase of short circuit duration (i.e. higher energy), the delay time to failure becomes shorter.



(a) CREE 1G SiC MOSFETs (b) CREE 2G SiC MOSFETs

Figure 5-11. Evolution of delayed failure mode with different short circuit durations.

After the destructive tests, the impedance between the three terminals of the DUT and the forward voltage of the body diode are measured using a digital multimeter. The typical measurement values are summarized in Table 5-2. As can be observed, all three terminals are nearly shorted together for the CREE 1G and 2G SiC MOSFETs. The ROHM SiC MOSFETs only show a short circuit in gate-source junction. The gate-drain, drain-source junction, and body diode still appear to be normal. However, a

detailed comparison with a new device reveals that the two junctions and the body diode are actually degraded. Both the impedance and forward voltage drop tend to decrease.

Table 5-2. Summary of typical data of failed devices

Device Types / Parameters	CREE		ROHM SEMICONDUCTOR
	1st Generation (1G)	2nd Generation (2G)	
R_{gs}/R_{sg} (Ω)	0.1 / 0.1	0.2 / 0.2	0.3 / 0.3
R_{gd}/R_{dg} (Ω)	10.4 / 10.4	17.2 / 17.2	800k / ∞
R_{ds}/R_{sd} (Ω)	10.5 / 10.5	17.4 / 17.4	∞ / 800k
V_F (V)	0.015	0.018	1.222

5.3.2 Short Circuit Withstand Time and Critical Energy

Based on the testing results under different case temperatures up to 200 °C, the temperature dependent short circuit withstand time and critical energy are summarized in Figure 5-12, where the DC bus voltage is 600 V and the gate voltages are + 20 / - 2 V for the CREE devices and + 18 / - 2 V for the ROHM devices.

Under low temperature levels, more dissipated energy is required for the devices to reach the critical failure temperature point and the corresponding SCWT is longer. The short circuit capability of the CREE 2G devices is nearly independent of temperature, and the short circuit critical energy and withstand time remain nearly constant. Similarly, the short circuit capability of the CREE 1G SiC MOSFETs show a slight dependence on temperature. In contrast to the CREE devices, both the short circuit critical energy and withstand time of the ROHM devices decrease linearly with the increase of case temperature.

The SCWT and critical energy under different DC bus voltage levels are also investigated, as shown in Figure 5-13. The case temperature is kept at 200 ºC by a hot plate. The short circuit capability of the three

SiC MOSFETs is strongly voltage dependent. With the increase of DC bus voltage, less dissipated energy is needed to cause a thermal destruction, and the device can survive for shorter time duration.

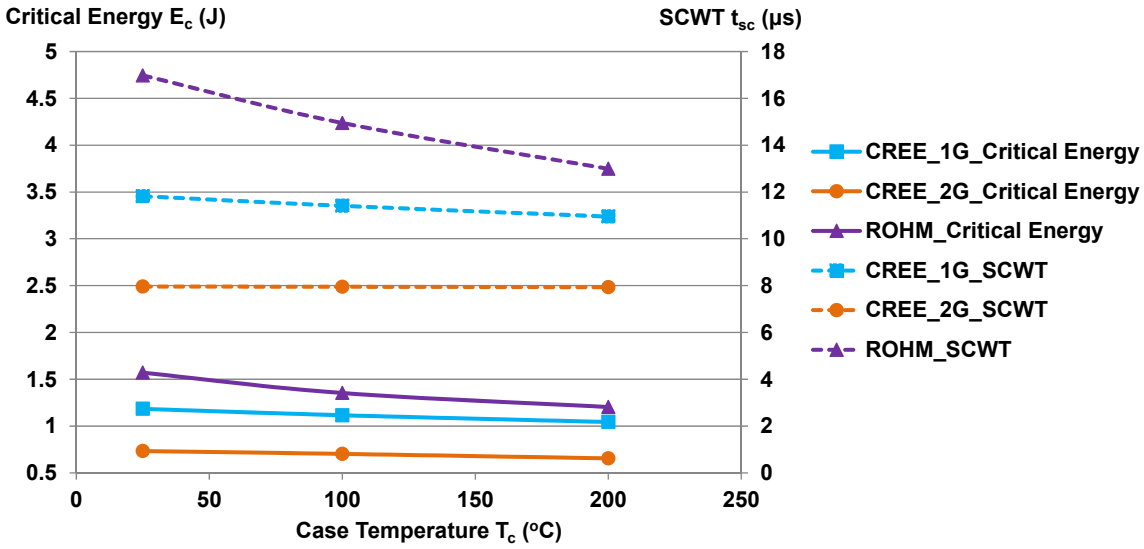


Figure 5-12. Comparison of temperature dependent short circuit capability.

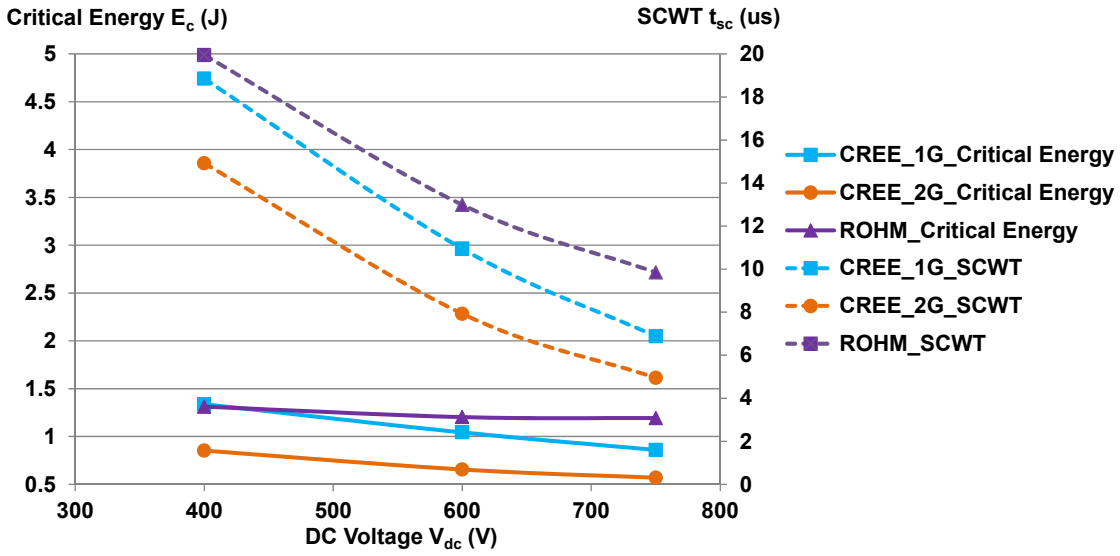


Figure 5-13. Comparison of DC bus voltage dependent short circuit capability.

5.3.3 Electro-Thermal Model

In order to evaluate the temperature distribution across the device assembly and thus further investigate the failure mechanism of the tested power devices as well as other SiC MOSFETs, an electro-thermal model (including the power semiconductor die, die-attach material, and case) is built, as shown in Figure 5-14.

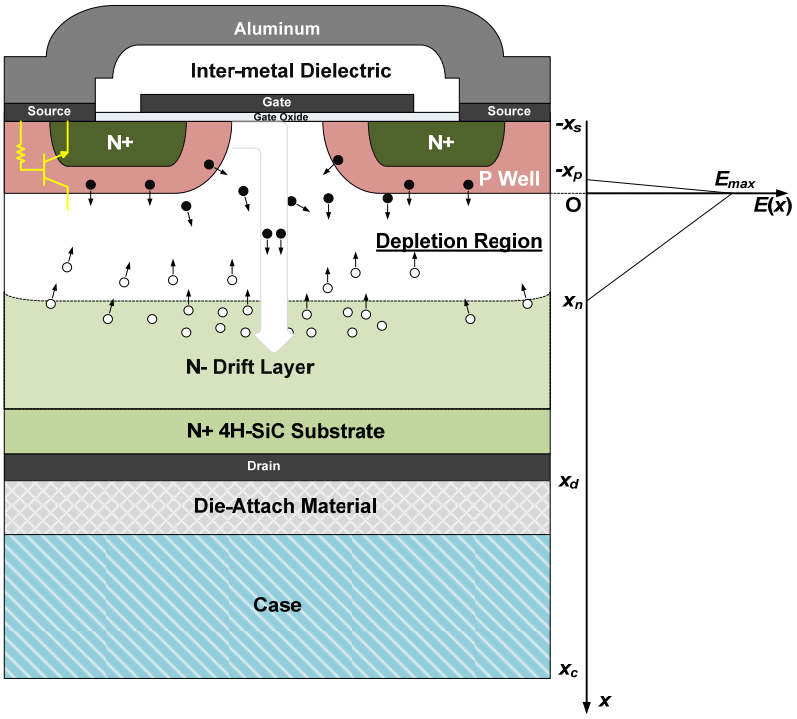


Figure 5-14. Electro-thermal model of SiC MOSFET with TO-247 package.

During short circuit transient, the full DC bus voltage V_{dc} applies to the power device, leading to a depletion layer width of x_p in the P-well and x_n in the N- drift region

$$x_p = \frac{N_d}{N_d + N_a}\sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_d + N_a}{N_d N_a}\right)V_{dc}} \qquad (5-2)$$

$$x_n = \frac{N_a}{N_d + N_a}\sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_d + N_a}{N_d N_a}\right)V_{dc}} \qquad (5-3)$$

where, ε_s is the dielectric constant for the 4H-SiC material; q is the electron charge; N_a and N_d represent the doping density of P well and N- drift region respectively. For the three types of SiC MOSFETs, the breakdown voltage provides an estimated N- drift region thickness of 20 μm and doping density of 2×10^{15} cm^{-3}.

The temperature distributions within the device T (x, y, z) under various short-circuit condition can be obtained by solving the heat diffusion equation in Cartesian coordinates

$$\frac{\partial}{\partial x}\left(k_p\frac{\partial T}{\partial x}\right)+\frac{\partial}{\partial y}\left(k_p\frac{\partial T}{\partial y}\right)+\frac{\partial}{\partial z}\left(k_p\frac{\partial T}{\partial z}\right)+Q=\rho c_p\frac{\partial T(x,y,z)}{\partial t} \quad (5-4)$$

where, k_p, ρ, and c_p are the thermal conductivity, material density, and specific thermal capacity; Q is the heat generation source due to the power dissipation during short circuit transient. Since the generated heat flux essentially flows in one dimension, from upper surface (i.e. source metallization layer) of the die to the case, (5-4) reduces to

$$\frac{\partial}{\partial x}\left(k_p\frac{\partial T}{\partial x}\right)+Q=\rho c_p\frac{\partial T(x)}{\partial t}. \quad (5-5)$$

The thermal properties of the die attach material and the case are assumed to be constant due to small temperature variation. However, the temperature dependence of thermal conductivity and specific heat of 4H-SiC material should be considered for SiC MOSFETs because of high internal temperature gradient [100]

$$k_p(T)=\frac{1}{-0.0003+1.05\times10^{-5}T} \quad (5-6)$$

$$c_p(T)=925.65+0.3772T-7.9259\times10^{-5}T^2-\frac{3.1946\times10^7}{T^2}. \quad (5-7)$$

The internal heat generation Q can be given as

$$Q=E(x)J(t)=\frac{E(x)I(t)}{S} \quad (5-8)$$

where J (t) is the short circuit current density; S is the power device active area; I (t) is the short circuit current in experiments; E (x) is the electric field distribution in the space charge region given by (5-9) and (5-10)

$$E(x) = -\frac{qN_d}{\varepsilon_s}(x - x_n) \qquad 0 \le x \le x_n \qquad (5-9)$$

$$E(x) = \frac{qN_a}{\varepsilon_s}(x + x_p) \qquad -x_p \le x \le 0. \qquad (5-10)$$

Substituting (5-8) – (5-10) and (5-2) – (5-3) into (5-5) yields

$$\frac{\partial}{\partial x}\left(k_p \frac{\partial T}{\partial x}\right) + \frac{qN_d}{\varepsilon_s}\left[\frac{N_a}{N_d + N_a}\sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_d + N_a}{N_d N_a}\right)V_{dc}} - x\right]\frac{I(t)}{S} = \rho c_p \frac{\partial T(x)}{\partial t} \qquad (5-11)$$

$$\frac{\partial}{\partial x}\left(k_p \frac{\partial T}{\partial x}\right) + \frac{qN_a}{\varepsilon_s}\left[\frac{N_d}{N_d + N_a}\sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_d + N_a}{N_d N_a}\right)V_{dc}} + x\right]\frac{I(t)}{S} = \rho c_p \frac{\partial T(x)}{\partial t}\,. \qquad (5-12)$$

The above equations can be applied to all SiC MOSFETs to obtain their temperature distribution. According to (5-11) and (5-12), several qualitative conclusions can be drawn as follows: (a) The increase of DC bus voltage V_{dc} (thus the increase of short circuit saturation current I (t)), causes a fast junction temperature rise ($\partial T/\partial t$). For a given failure temperature, the short circuit withstand time will be reduced. (b) The increase of current density, by larger channel width to length ratio (W/L) and/or higher gate voltage levels, will be at the cost of lower short circuit capability. Currently, the low channel mobility of SiC MOSFETs requires higher positive gate bias (+18 V~ +20 V) than Si devices (+15 V). Under the same DC bus voltage, the temperature rising rate is actually proportional to the current density. (c) The device scaling through die paralleling should not affect the failure temperature and short circuit withstand time.

The derived heat equations can be solved by finite-difference methods. Since (5-11) and (5-12) are second order in spatial coordinates and first order in time, two boundary conditions and one initial condition must be specified. In this work, the case temperature is fixed (from 25 ºC to 200 ºC) at the bottom surface of the case. The generated heat flux is assumed to be unidirectional, and the top surface of the die is considered to be adiabatic. In addition, the device junction temperature before short circuit test equals to the case temperature. These boundary conditions and initial conditions are summarized as

$$T(x = x_c, t) = T_c \qquad (5-13)$$

$$k_p \frac{\partial T}{\partial x}|_{x=-x_s} = 0 \quad (5-14)$$

$$T(x, t=0) = T_c. \quad (5-15)$$

5.3.4 Leakage Current Model

Since the leakage current seems to be responsible for device failure in experiments, the temperature dependence of leakage current is also evaluated using the derived electro-thermal model. In this work, three essential leakage current mechanisms are taken into account, namely the thermal generation current, diffusion current, and avalanche multiplication current.

(1) Thermal Generation Current

The thermally activated carrier generation is described by Shockley-Read-Hall (SRH) theory, and the corresponding leakage current is given by (5-16) [101]

$$I_{g\_th} = \frac{qSn_i}{\tau_g} \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_d + N_a}{N_d N_a}\right) V_{dc}} \quad (5-16)$$

where, n_i is intrinsic carrier concentration and τ_g is the SRH generation lifetime. As can be observed, the SRH generation current is actually both voltage and temperature dependent. With the increase of DC bus voltage (from 400 V to 750 V in this work), the thermal generation current will also increase. The temperature dependence of this leakage is mainly caused by the intrinsic charge carrier density of 4H-SiC material

$$n_i(T) = 1.7 \times 10^{16} \times T^{\frac{3}{2}} \times e^{-\frac{2.08\times10^4}{T}}. \quad (5-17)$$

Although the intrinsic carrier concentration for SiC is far smaller than for Si due to the large difference in band gap energy, its impact on the leakage current of SiC MOSFETs at high junction temperatures cannot be neglected. The generation lifetime depends on not only temperature but also other factors, such as the material dislocation density, surface effects, the capture cross sections, and the trap energy [101]. Based on the previous measurement results in [102]–[104], the carrier generation lifetime in 4H-SiC epilayers

ranges from less than 1 ns to approximately 1 μs. Due to its high uncertainty, several different lifetimes will be used in the later simulation to obtain a realistic value.

(2) Diffusion Current

As mentioned above, the intrinsic minority carriers in P well and N- drift layer will quickly increase due to the rise of junction temperature during short circuit transient. These minority carriers diffuse into the depletion region and drift across the PN- junction with the aid of electric field E (x), leading to a saturation current proportional to the doping concentration at the low doped side of the junction.

According to [105]–[109], the temperature dependence of the saturation current I_{g_diff} is given by the diffusion coefficient (D_p and D_n), minority diffusion length (L_p or L_n), and the intrinsic carrier concentration (n_i) as follows

$$I_{g\_diff} = qS\left(\frac{n_i^2 D_n}{L_n N_a} + \frac{n_i^2 D_p}{L_p N_d}\right) \tag{5-18}$$

$$L_p = \sqrt{D_p \tau_p} \qquad L_n = \sqrt{D_n \tau_n} \tag{5-19}$$

$$D_p = \frac{kT}{q}\mu_p \qquad D_n = \frac{kT}{q}\mu_n \tag{5-20}$$

$$\mu_p(T) = \mu_{p0}\left(\frac{T}{300}\right)^{-2.2} \qquad \mu_n(T) = \mu_{n0}\left(\frac{T}{300}\right)^{-2.6} \tag{5-21}$$

$$\tau_p(T) = \tau_{p0}\left(\frac{T}{300}\right)^{1.5} \qquad \tau_n(T) = \tau_{n0}\left(\frac{T}{300}\right)^{2.32} \tag{5-22}$$

where k is the Boltzmann constant; μ_p and μ_n are the temperature dependent hole and electron mobility of 4H-SiC epilayers; μ_{p0} and μ_{n0} are the hole and electron mobility at 300 K; τ_p and τ_n are the temperature dependent hole and electron lifetime in N- region and P well region respectively; τ_{p0} and τ_{n0} are the hole and electron lifetime at 300 K.

(3) Avalanche Generation Current

Under short circuit condition, both the majority electron charge and thermally induced minority charge carriers in the depletion region will be accelerated by the electric field E(x). Like the well-known avalanche breakdown mechanism, if the kinetic energy of the charge carriers is high enough to generate

new electron hole pairs, an additional leakage current gradually forms based on the avalanche multiplication.

For a given DC bus voltage V_{dc}, the avalanche current is given as

$$I_{g\_av} = S\sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_d + N_a}{N_d N_a}\right)V_{dc}}\left(\alpha_n|J_n| + \alpha_p|J_p|\right) \quad (5-23)$$

In (5-23), J_n and J_p are the electron and hole current density, respectively. Since most of the short circuit current within SiC MOSFETs are composed by electrons, hole current density is neglected (i.e. $J_n = J$) in the following analysis. α_n and α_p represent the impact ionization coefficient for electrons and holes, which depend not only on electric field but also temperature. As reported in [110] and [111], the impact ionization rate of SiC material is much larger for holes than for electrons, which can be curve-fitted with the empirical law of impact ionization coefficient proposed by Chynoweth:

$$\alpha_p(T) = (6.3 \times 10^6 - T \times 1.07 \times 10^4) \times exp\left[-\frac{1.75 \times 10^7}{E(x)}\right] \quad (5-24)$$

$$\alpha_n(T) = (1.6 \times 10^5 - T \times 2.67 \times 10^2) \times exp\left[-\frac{1.72 \times 10^7}{E(x)}\right]. \quad (5-25)$$

5.3.5 Simulation Results

Using the experimental short circuit waveforms and derived electro-thermal model, the temperature distribution within the SiC MOSFETs can be evaluated and the temperature dependent leakage current is calculated numerically.

Figure 5-15 shows the comparison of depletion region boundary (x = 0) temperature evolution for the three types of devices, under a DC bus voltage of 600 V and case temperature of 25 ºC. As can be seen, the failure temperatures of CREE SiC MOSFETs are close, while that of ROHM device is higher. Under the same short circuit condition, the device with higher current density presents faster temperature rising rate, as predicted by the electro-thermal model in (5-11) and (5-12). For example, the CREE 2G and ROHM SiC MOSFETs have the highest $\partial T/\partial t$ at the initial and end stage, respectively. For the CREE SiC MOSFETs, the higher current density or $\partial T/\partial t$ eventually leads to a lower SCWT. However, ROHM

device has higher saturation current density, but also longer SCWT. Their different failure mechanisms will be discussed in detail later.

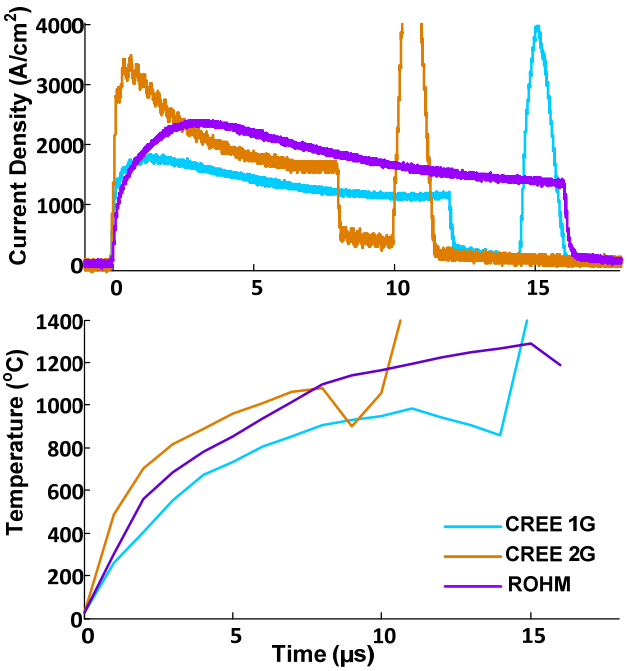


Figure 5-15. Comparison of saturation current density and junction temperature.

The x-axis temperature distribution of the three devices at turn-off moment is plotted in Figure 5-16. The maximum temperature is reached at the depletion region boundary ($x = 0$) due to the highest electric field. It is shown that the heat flux only diffuses less than 200 μm for the three types of devices. Compared with the other two devices, CREE 2G SiC MOSFETs tend to have a higher temperature gradient ($\partial T/\partial x$) and lower heat diffusion distance. This is probably because the current density of CREE 2G device is the highest at the turn-off moment. Such a low heat diffusion distance reveals that the short circuit capability of SiC MOSFETs can be independent of packaging technologies and external cooling conditions. Moreover, the concentrated heat generated within the depletion region could cause the degradation or even damage of the gate oxide and metallization layer [112].

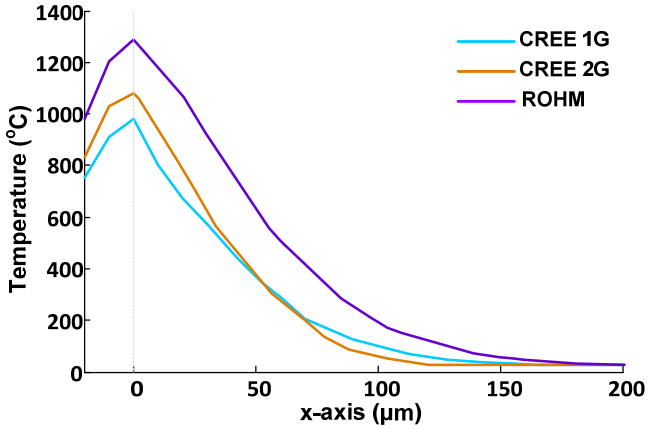
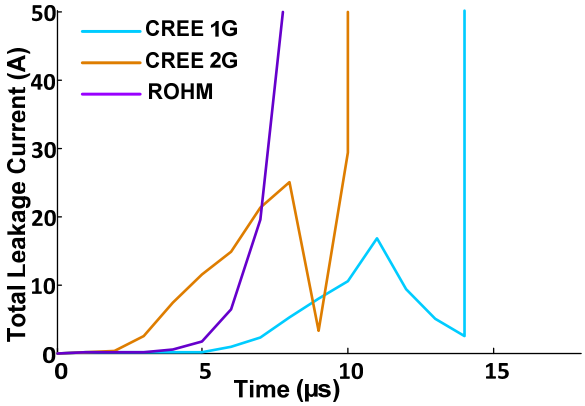


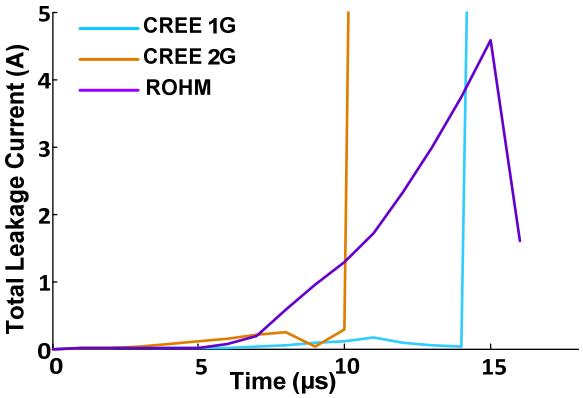
Figure 5-16. Comparison of temperature distribution along vertical path.

The leakage current of the three devices can be calculated from the junction temperature information. However, as discussed above, the thermal generation lifetime is not easy to be identified precisely for SiC MOSFETs from different device manufacturers. The simulation results will be tentatively obtained using different average generation lifetimes to match with experimental testing results. Based on the junction temperature and leakage current model, the total leakage current is shown in Figure 5-17(a) and Figure 5-17(b), with an average SRH generation lifetime of 1 ns and 100 ns, respectively. The simulated leakage currents decrease with the increase of generation lifetime. A comparison of the simulated leakage current with the previous experimental results reveals that CREE SiC MOSFETs tend to present a much lower thermal generation lifetime than ROHM SiC MOSFETs.

For CREE SiC MOSFETs, such a high additional bipolar leakage current flowing horizontally in the P well region may activate the parasitic BJT structure shown in Figure 5-14. Moreover, high junction temperature will further contribute to the activation of the parasitic BJT, since the built-in voltage of the PN junction decreases with temperature (-2.3 to -3.5 mV / K for 4H-SiC [113]). If the parasitic BJT is on, short circuit current will increase quickly and eventually leads to a device failure due to typical second breakdown and associated thermal runaway issues. On the other hand, the small leakage current of ROHM SiC MOSFETs is difficult to initiate a thermal runaway phenomenon. They are more likely to be damaged because of the high local temperature close to the gate oxide.



(a) 1 ns



(b) 100 ns

Figure 5-17. Comparison of total leakage current with different generation lifetimes.

Figure 5-18 gives the calculated components of the total leakage current for the three devices. As can be observed, the thermal generation current (I_{g_th}) is dominant during the whole short circuit transient. The reason is that the heat wave within the depletion region creates a positive feedback on the intrinsic carrier density when flowing towards the substrate of the power devices.

The thermal generation current, responsible for the thermal runaway issue, increases monotonously with temperature evolution and reaches around 20 A for CREE SiC MOSFETs before device turn-off. The avalanche generation current (I_{g_av}) is negligible, and decreases with temperature due to reduced impact ionization rate at higher temperatures. The diffusion generation current (I_{g_diff}) is also small before device turn-off, while it increases quickly at the end of the short circuit transient.

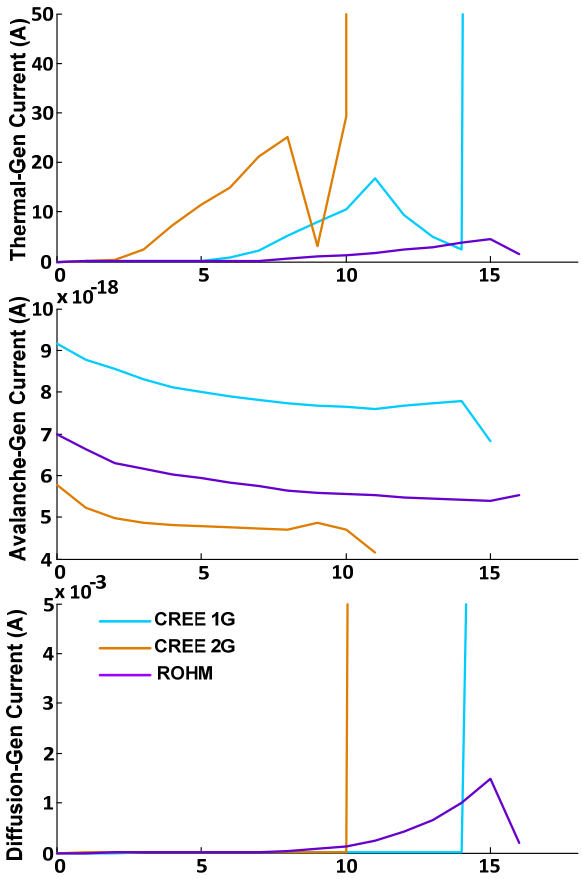


Figure 5-18. Calculated leakage current components of the three SiC MOSFETs.

More numerical simulation studies have also been conducted for the CREE 1G SiC MOSFETs based on the previous testing results. Figure 5-19 illustrates the comparison of depletion region boundary ($x = 0$) temperature evolution and total leakage current of the CREE 1G SiC MOSFETs with different combinations of DC bus voltage (600 V to 750 V) and case temperature (25 ºC to 200 ºC).

As can be observed, even though the short circuit critical energy and withstand time are different for the three cases, the leakage currents start to increase quickly when the temperature is higher than 700 ºC. The leakage currents continue increasing until the temperature reaches around 1000 ºC. With the assumption of the same device failure temperature, the short circuit withstand time can be predicted under given short circuit conditions. In addition, for the same die size (or current density), higher voltage stress (or electric field) results in a faster temperature rise, as revealed by the heat diffusion equation.

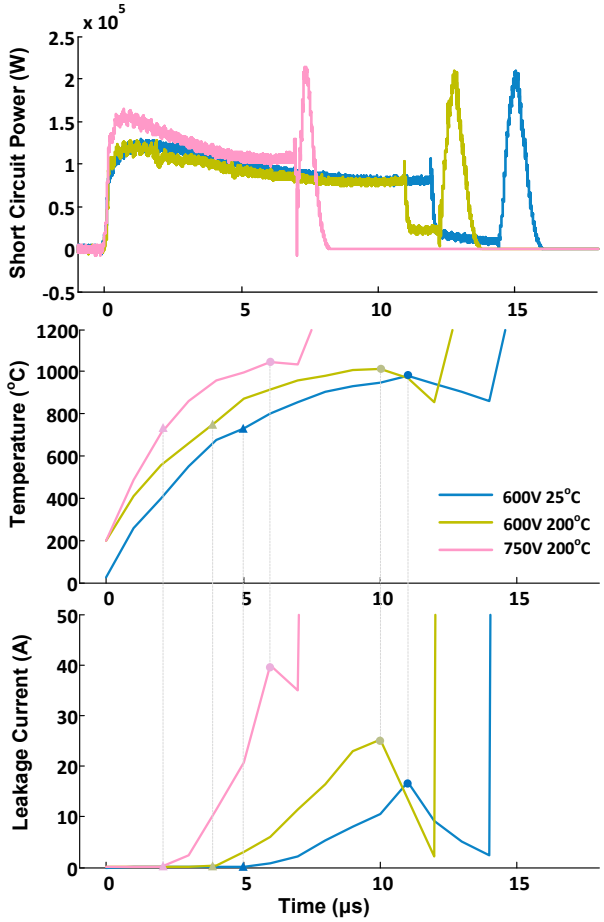


Figure 5-19. Numerical simulation results with different combinations of DC bus voltage and case temperature.

5.3.6 Repetitive Short Circuit Robustness

Up to this point, the ruggedness of SiC MOSFETs has been evaluated under single-event short circuit condition. The device under test fails immediately after a single-event short circuit. However, long term reliability of SiC MOSFETs under repetitive short circuit condition is still a concern.

The repetitive short circuit robustness of IGBT and MOSFETs has been reported in previous work [114]. It is shown that the relative value of short circuit energy versus critical energy plays an important role in different robustness, as illustrated in Figure 5-20. For short circuit energies above the critical value ($E > E_c$), the device cannot survive after a short circuit event. For short circuit energies below the critical

value ($E < E_c$), the device fails after a certain number of short circuits due to cumulative aging effects. More interestingly, when the short-circuit energy equals to the critical value ($E = E_c$), the number of short circuit events that the device can withstand is randomly distributed.

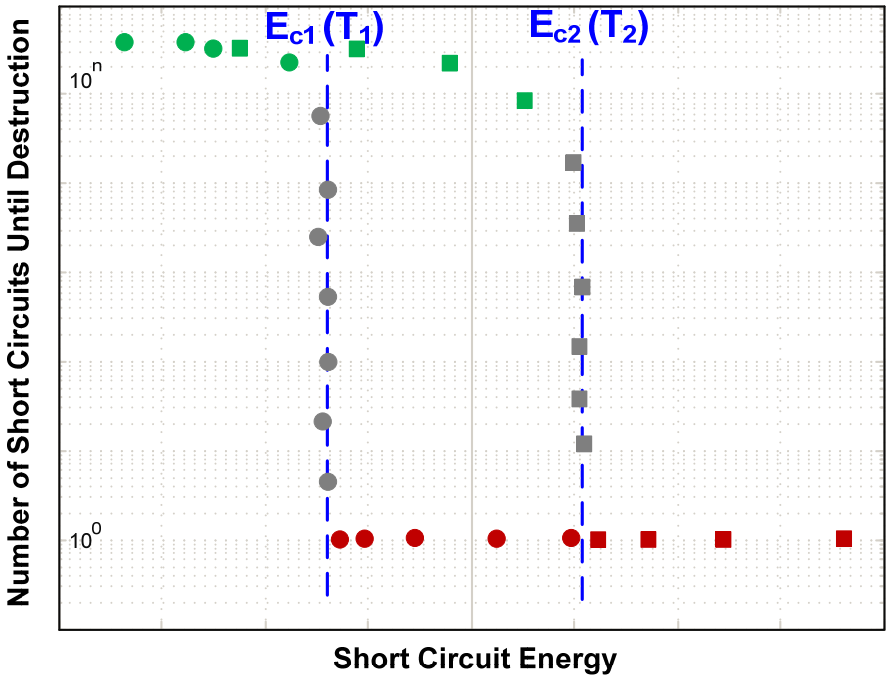


Figure 5-20. Repetitive robustness of IGBTs and MOSFETs.

The robustness of SiC MOSFETs under repetitive short circuit conditions is analyzed in this work based on the developed electro-thermal model and leakage current model. The numerical simulation results of CREE 1G SiC MOSFETs is redrawn in Figure 5-21.

According to the junction temperature and leakage current information, five-level repetitive short circuit robustness can be observed:

(i) Thermal runaway (around 1000 ^{o}C)

(ii) Leakage current surge (around 750 ^{o}C)

(iii) Metallization degradation (660 ^{o}C for aluminum melting points)

(iv) Ohmic contact and passivation (< 450 ^{o}C [115])

(v) Gate oxide degradation (135 ^{o}C for CREE 1G, 150 ^{o}C for CREE 2G [116])

These robustness levels actually determine the response time of a protection circuit, as discussed in detail in the next chapter.

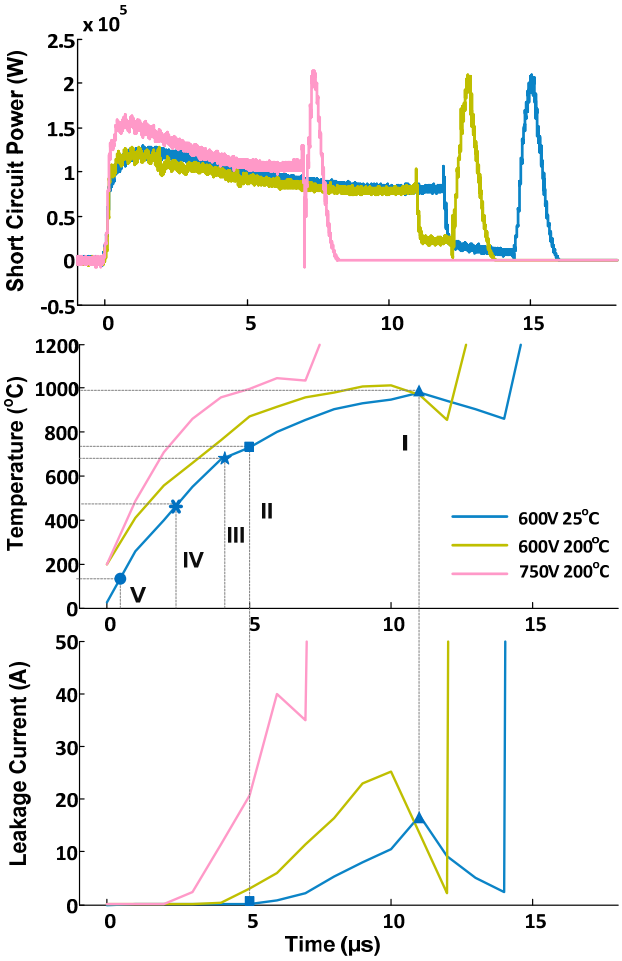


Figure 5-21. Numerical simulation results for repetitive short circuit analysis.

5.4 Conclusion

In this chapter, the temperature dependent short circuit capability of three different types of commercial SiC MOSFETs has been evaluated experimentally. An electro-thermal model and a leakage current model, taking temperature dependent thermal properties of SiC material into account, have also

been built to calculate the junction temperature distribution and leakage current components. The key points of this chapter can be summarized as follows:

1) The short circuit withstand time and critical energy of SiC MOSFETs will be reduced with the increase of current density, case temperature, and DC bus voltage. However, these are nearly independent of device scaling (i.e. die paralleling) and fault types (i.e. HSF and FUL).

2) The junction temperature will increase quickly during a short circuit transient, which reaches a maximum point at the boundary of depletion region. The higher current density results in a faster temperature rise and larger temperature gradient.

3) The high temperature heat wave within the depletion region creates a positive feedback on the intrinsic carrier density. The fast increase in intrinsic carrier density leads to a thermal generation current which dominates the total leakage current during the whole short circuit transient.

4) The short circuit failure mechanisms of SiC MOSFETs can be thermal generation current induced thermal runaway or high temperature related gate oxide damage.

5) The heat flux diffuses a limited distance toward the substrate before device failure, which indicates the short circuit capability of modern SiC MOSFETs can be independent of packaging materials and external cooling conditions.

The experimental results and numerical simulation results presented in this chapter aim at helping designers to evaluate actual safety margins for SiC MOSFET based converters. Additionally, it may provide device manufacturers with some useful feedback to improve their future device technologies.

6 Short Circuit Protection of SiC MOSFETs

Short circuit protection of silicon carbide (SiC) MOSFETs remains a challenge due to lack of practical knowledge. Based on the short circuit capability evaluation results in the previous chapter, the requirements for active protection schemes can be obtained, taking noise immunity into consideration, as shown in Figure 6-1.

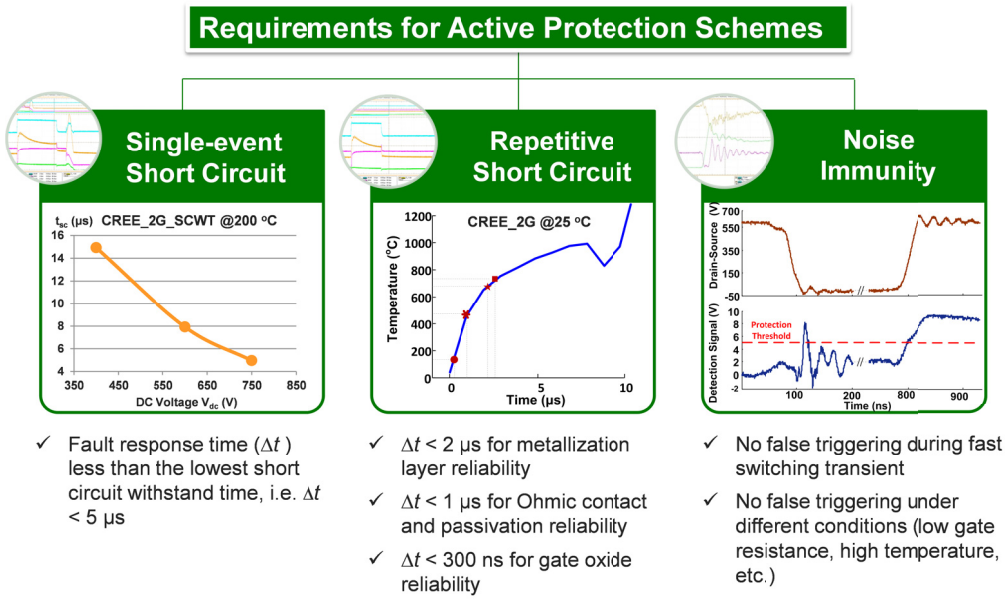


Figure 6-1. Requirements for active protection schemes.

Bearing in mind these requirements, this chapter presents three overcurrent protection methods to improve the reliability and overall cost of the SiC MOSFET based converter. First, a solid state circuit breaker (SSCB) composed primarily by a Si IGBT and a commercial gate driver IC is connected in series with the DC bus to detect and clear overcurrent faults. Second, the desaturation technique using a sensing diode to detect the drain-source voltage under overcurrent faults is implemented as well. Third, an active overcurrent protection scheme through dynamic evaluation of fault current level is proposed. The design considerations and potential issues of the protection methods are described and analyzed in detail. A phase-leg configuration based step-down converter is built to evaluate the performance of the proposed

protection schemes under various conditions, considering variation of fault type, decoupling capacitance, turn-on gate resistance, protection circuit parameters, etc. Finally, a comparison is made in terms of fault response time, temperature dependent characteristics, and applications to help designers select a proper protection method.

6.1 Methodology and Test Setup

An overcurrent condition can be caused by either a short-circuit or an overload fault, and the current level of both can be different depending on the impedance of the fault current path. Shoot-through fault, usually with very low short-circuit impedance, is considered as the most dangerous type, which is also the focus of this work.

The testing circuit is shown in Figure 6-2, which represents one phase leg of a three phase inverter with a clamped inductive load. The short-circuit control switch, composed of four paralleled SiC MOSFETs, is controlled to create a shoot-through fault.

The device under test (DUT) could present overcurrent during the turn-on switching transient or during the on-state condition, resulting in hard switching fault (HSF) or fault under load (FUL), respectively [92], and their corresponding drive signal and ideal short-circuit waveforms are shown in Figure 6-3. In this work, the performance of the three protection schemes under both fault types will be evaluated.

The device used for the experimental test is a 1200 V/42 A discrete SiC MOSFET (CMF20120D) from CREE. The experimental waveforms are recorded by a Tektronix DPO5204 2GHz 4 channel digital phosphor oscilloscope. The gate-source voltage and drain-source voltage are measured by passive probe Tektronix P6139A (500 MHz) and high voltage passive probe Tektronix P5100 (250 MHz), respectively. The drain current is measured by a T&M RESEARCH SSDN-10 coaxial shunt (0.1 Ω, 2000 MHz) in the SSCB, SSDN-015 coaxial shunt (0.015 Ω, 1200 MHz) in the desaturation technique, and Pearson current transformer 2877 (1V/A, 200 MHz) in the fault current evaluation method. Moreover, the channel delays caused by different types of probes are compensated before testing.

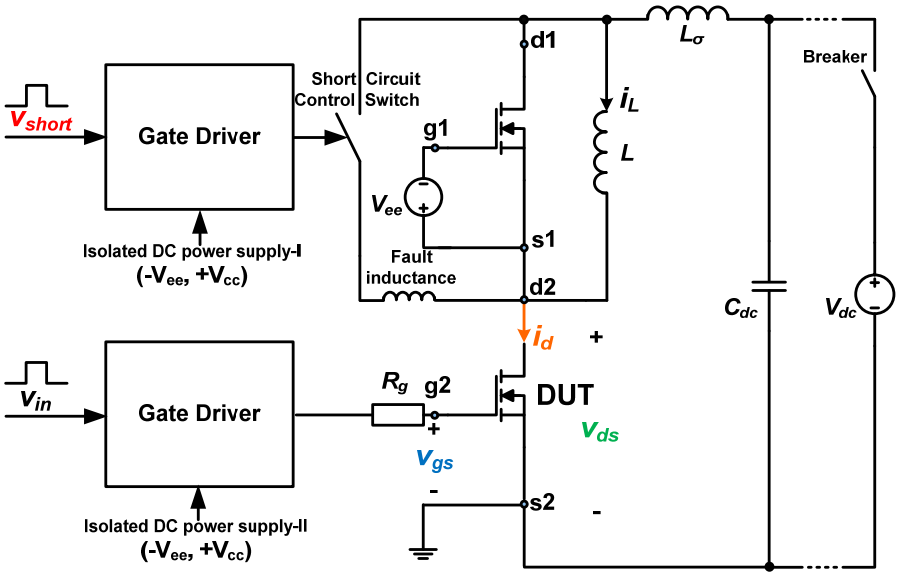
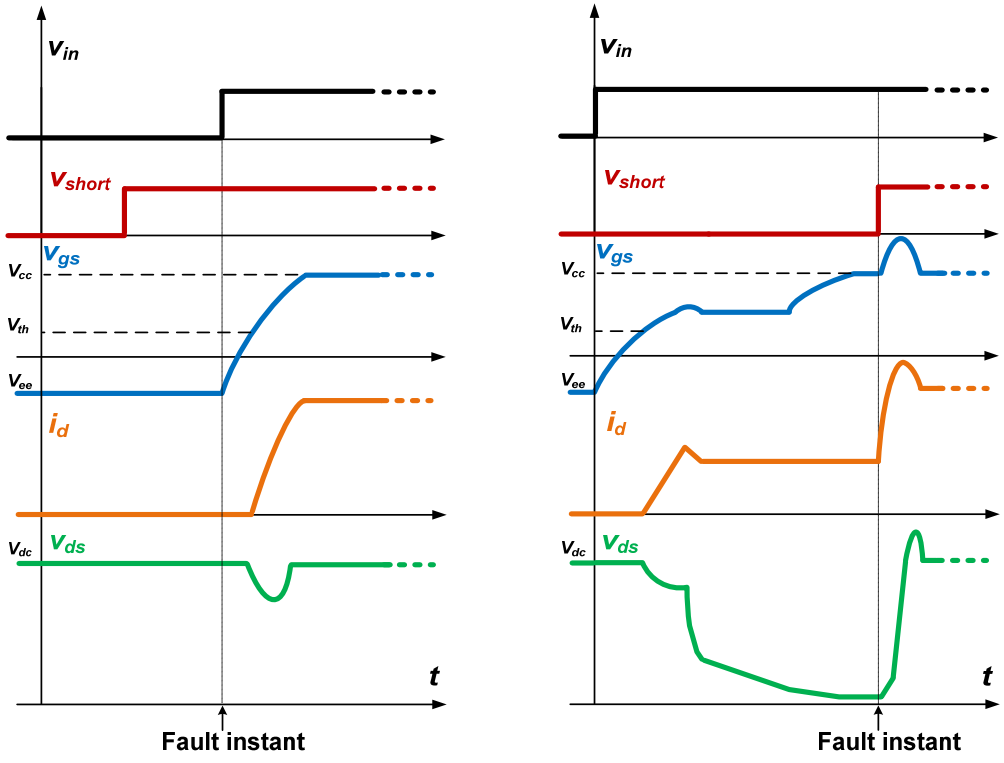


Figure 6-2. Overcurrent protection testing circuit.



(a) HSF (b) FUL

Figure 6-3. Drive signal and ideal short-circuit waveforms.

The experimental test setup is shown in Figure 6-4 and Figure 6-5. The two channel synchronous waveform generator sends one signal (v_{in}) to the gate driver of the DUT, and the other one (v_{short}) to the gate driver of the short-circuit control switch. To test the protection performance at different temperatures, the device is heated by a controlled hot plate at the bottom side of the test board, and the temperature is monitored by a thermocouple. A fan is used to cool the current sensor and gate driver loop to improve measurement accuracy. All testing waveforms are extracted by MATLAB to compare protection performance under different conditions.

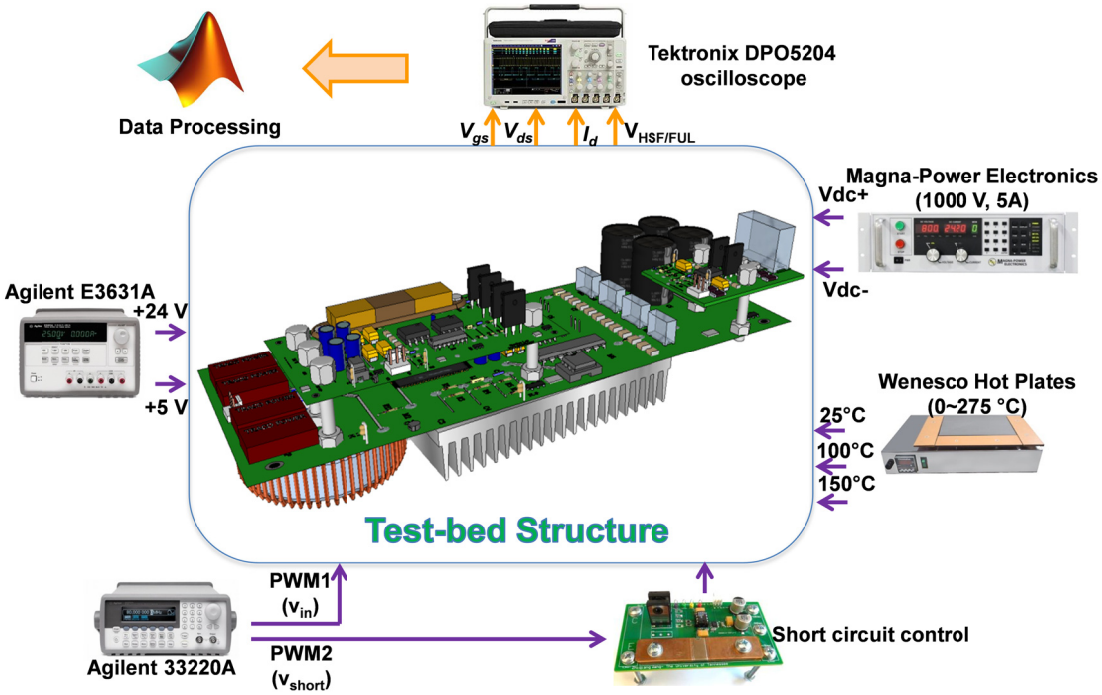


Figure 6-4. Experimental test and measurement setup.

The hardware test bed is shown in Figure 6-5. The SiC MOSFETs phase-leg configuration and DC capacitor bank are connected by an internal planar busbar structure within the test board. The SSCB, desaturation technique, fault current evaluation method, and short-circuit control board are integrated together with the main power testing circuit. When one protection scheme is tested, the other two are deactivated to eliminate their interaction.

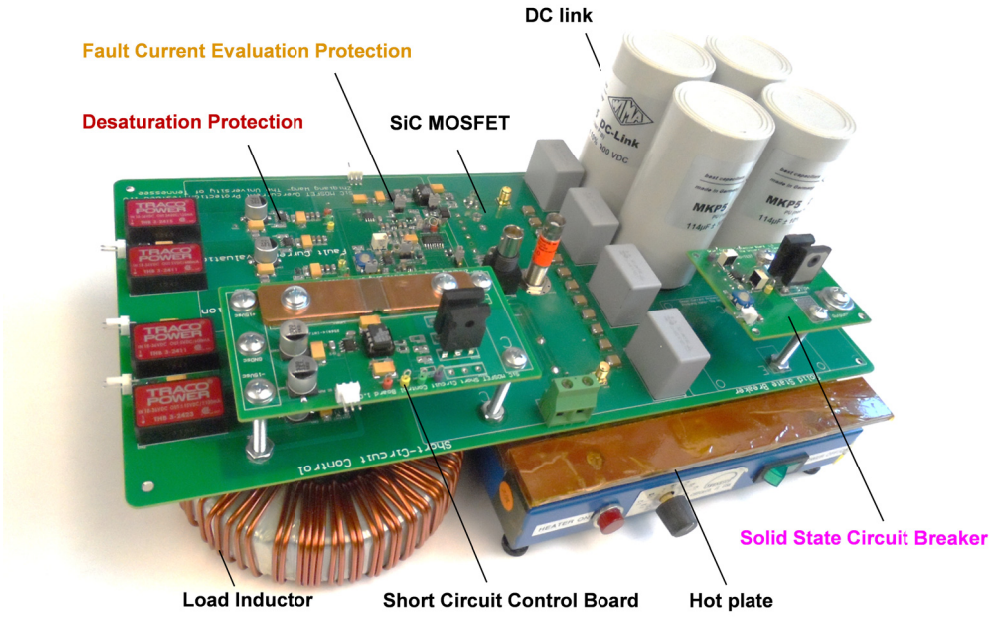


Figure 6-5. Hardware testbed for performance evaluation of the overcurrent protection schemes.

6.2 Solid State Circuit Breaker

Figure 6-6 describes a SiC MOSFET based step-down converter with a normally-on SSCB.

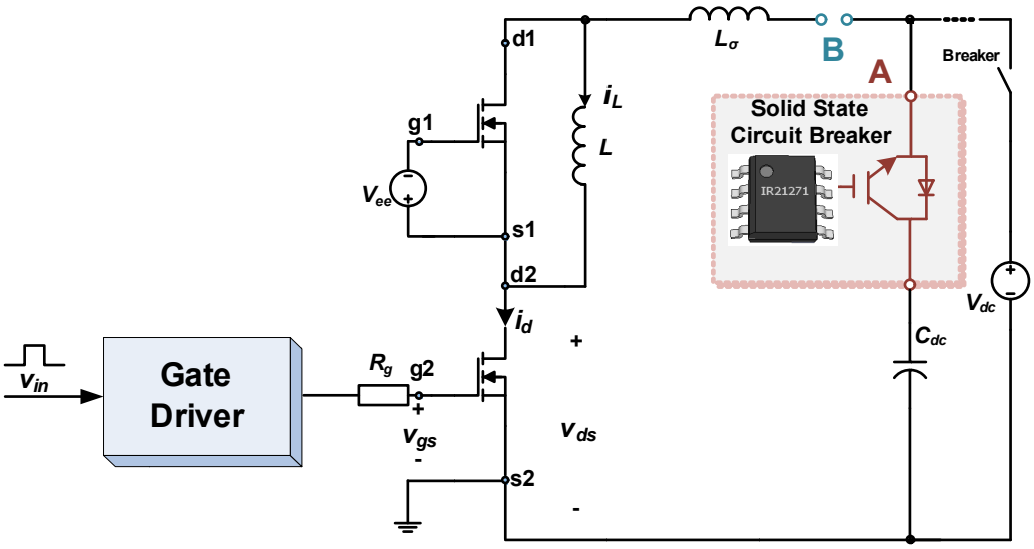


Figure 6-6. Step-down converter with a SSCB.

The SSCB could be inserted either in series with the energy storage capacitors (position A), or in series with the main power loop (position B). Inserting it into the main power loop can reliably detect and clear overcurrent faults, while minimizing power dissipation is also a priority. Alternatively, the loss associated with the SSCB is small since only ripple current goes through the SSCB in series with the DC link energy storage capacitors. However, SiC MOSFETs could still be destroyed by the short-circuit loop from the DC source V_{dc} or front-end rectifier to the device.

6.2.1 Design Guideline

The circuit implementation of an IGBT and a commercial gate driver IC IR2127 based SSCB is illustrated in Figure 6-7. The voltage divider, R_{d1} and R_{d2}, is used to adjust the gate voltage and saturation current level of the IGBT. The gate resistor R_g and gate diode D_g determine the turn-off speed and voltage spike under overcurrent condition. The R_{ho} is selected to minimize the increased miller capacitance effect from sensing diode D_{sat}, and makes sure there is no significant current being drawn from the HO output.

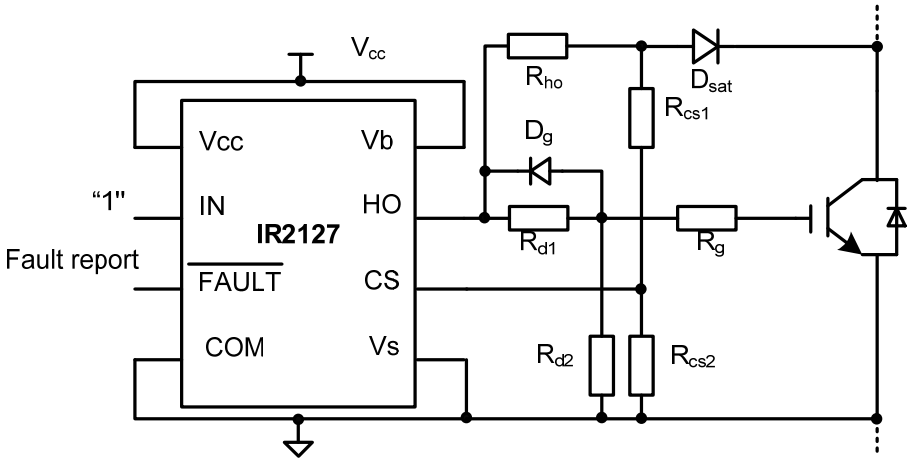


Figure 6-7. Circuit implementation of the SSCB.

The value of R_{cs1} and R_{cs2} should be carefully selected considering that a protection is triggered as long as the voltage on the CS-pin V_{cs} is greater than the threshold voltage V_{cs_th}. Under normal operation, the diode D_{sat} together with the on-state resistance $R_{ce(on)}$ is in parallel with R_{cs1} and R_{cs2}. Under fault

condition, the diode D_{sat} still conducts when the IGBT is slightly saturated, and then becomes reverse biased when the IGBT is highly saturated.

To make sure a fault can be detected when the IGBT is highly saturated,

$$V_{cs\_off} = \frac{V_{cc} \cdot R_{cs2}}{R_{ho} + R_{cs1} + R_{cs2}} > V_{cs\_th} \quad (6-1)$$

where, V_{cs_off} is the CS-pin voltage when the diode D_{sat} is off. For fast fault response, an overcurrent condition should be detected when the IGBT is slightly saturated (e.g. V_{ce} = 8 V),

$$V_{cs\_on} = \frac{(V_{ce} + V_{diode}) \cdot R_{cs2}}{R_{cs1} + R_{cs2}} = V_{cs\_th} \quad (6-2)$$

where, V_{diode} is the voltage across D_{sat}, and V_{cs_on} is the CS-pin voltage when the diode D_{sat} is on.

6.2.2 Impact of *dv/dt*

During both normal turn-on transient and short-circuit transient of the SiC MOSFET, the collector-emitter voltage of the IGBT increased dramatically due to current with high *di/dt* flowing through the IGBT of SSCB. The high dV_{ce}/dt causes three displacement currents through either the junction capacitance of diode D_{sat} or the miller capacitance of IGBT, as shown in Figure 6-8.

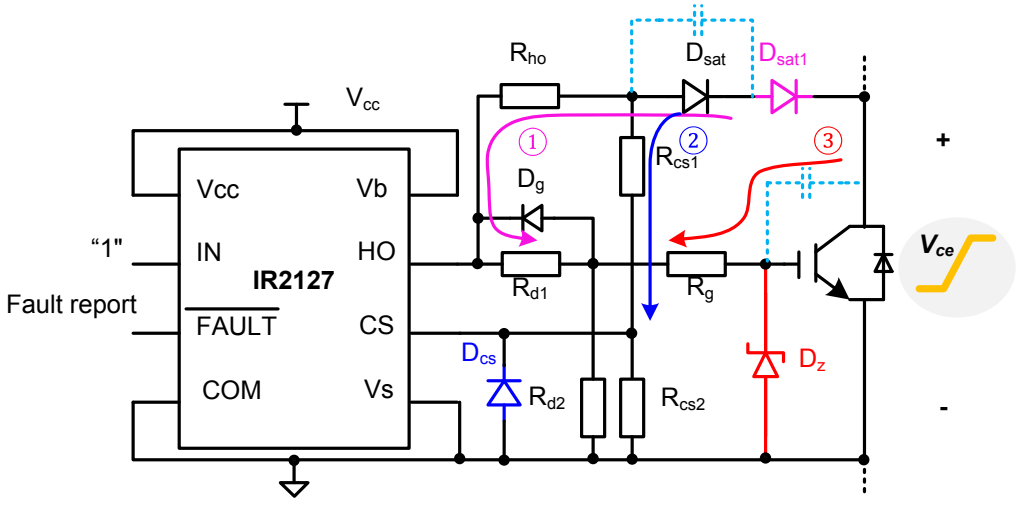


Figure 6-8. Impact of dV_{ce}/dt on the SSCB.

The first current increases the gate voltage by flowing through the resistance R_{ho}, R_{d1} and R_{d2}. The second current induces an additional voltage noise across CS-pin by flowing through the resistance R_{cs1} and R_{cs2}, which might falsely trigger an overcurrent protection during normal turn-on transient. In addition, high dV_{ce}/dt may push the CS-pin voltage to exceed its normal range. The third current flows through the gate loop, which increases the internal gate voltage of the IGBT V_{ge_in} according to (6-3)

$$V_{ge\_in} = V_{preset} + C_{gc}\frac{dV_{ce}}{dt}\cdot\left(R_g + R_{g\_in}\right) + L_g C_{gc}\frac{d^2V_{ce}}{dt^2} \qquad (6-3)$$

where, V_{preset}, C_{gc}, L_g, and R_{g_in} represent the preset gate voltage, miller capacitance, gate loop equivalent inductance, and IGBT internal gate resistance, respectively.

To avoid a false trigger and regulate the CS-pin voltage within normal range, several sensing diodes are connected in series to minimize the equivalent junction capacitance effect, as shown in Figure 6-8. Furthermore, a clamping diode D_{cs} is placed in parallel with R_{cs2} to absorb the noise caused by high dV_{ce}/dt. To suppress the increase of gate voltage, a zener diode is added in the gate to decouple the external gate resistance and gate-loop inductance. The zener diode must be located physically closest to the IGBT–an easily overlooked aspect, in order to minimize the internal gate loop inductance.

Besides a proper power rating, the IGBT should have low internal gate resistance and low miller capacitance to mitigate the dV_{ce}/dt effects, as shown in (6-3). Table 6-1 shows a comparison of several IGBT candidates. With nearly equal miller capacitance, APT35GP120BG with internal gate resistance as low as 0.6 Ω is selected in this work.

The output characteristic of the IGBT is measured by a Tektronix 371B curve tracer at room temperature, as shown in Figure 6-9. According to the measured output characteristic, the theoretical protection threshold is set to 35 A by tuning the preset gate voltage of the IGBT to be 7.5 V. However, the actual saturation current level is subject to change somewhat by increased junction temperature at protection transient.

Table 6-1. Comparison of IGBTs used for the SSCB

IGBT Type	Power Rating	Internal Gate Resistance R_{gi}	Miller Capacitance C_{res} (V_{ce} =0~10V)
APT25GT120BRG	1200V/54A (25°C)	4.3 Ω	2000pF~150 pF
IRG4PH50S	1200V/57A (25°C)	1.6 Ω	3000pF~600 pF
IXGH30N120B	1200V/60A (25°C)	4.8 Ω	2000pF~400 pF
APT35GP120BG	1200V/96A (25°C)	0.6 Ω	3000pF~200 pF
APT75GN120LG	1200V/200A (25°C)	10.5 Ω	2000pF~300 pF

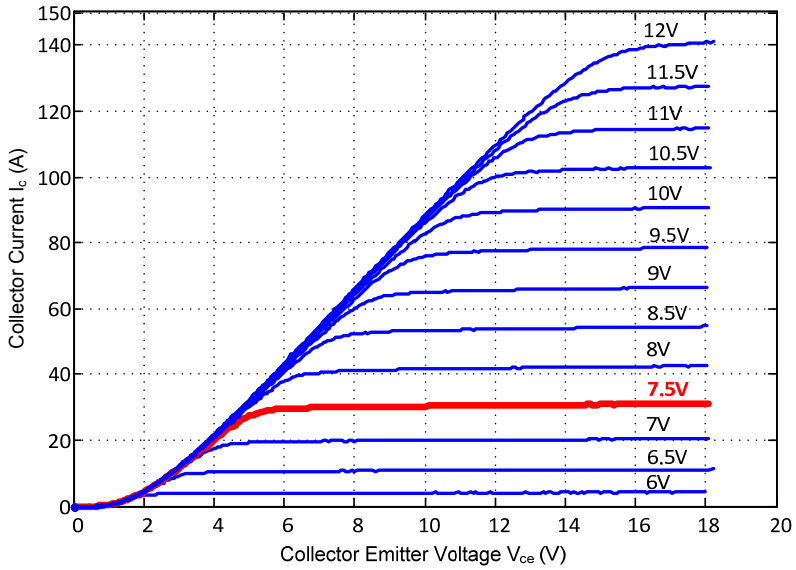
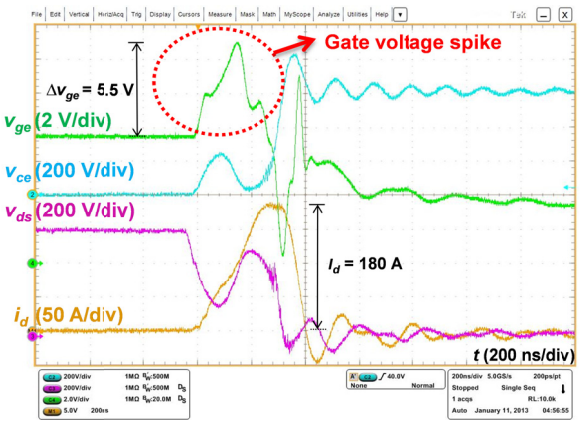
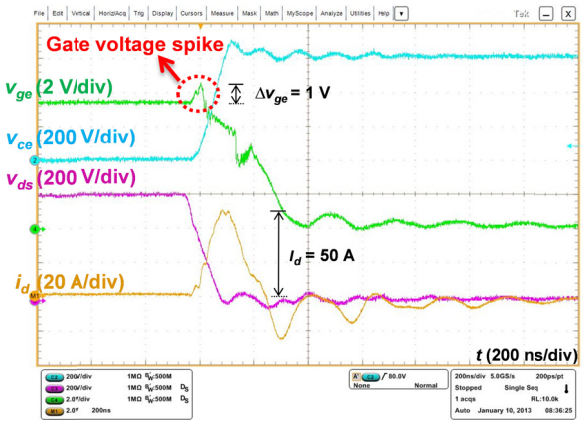


Figure 6-9. Output characteristic of the selected IGBT.

Comparative results using the proposed SSCB with/without gate zener diode to protect a HSF and FUL with a DC bus voltage of 600 V are shown in Figure 6-10 and Figure 6-11, where v_{ge}, v_{ce}, v_{ds}, and i_d represent the gate voltage, collector-emitter voltage of the IGBT, the drain-source voltage, and drain current of the SiC MOSFET, respectively.

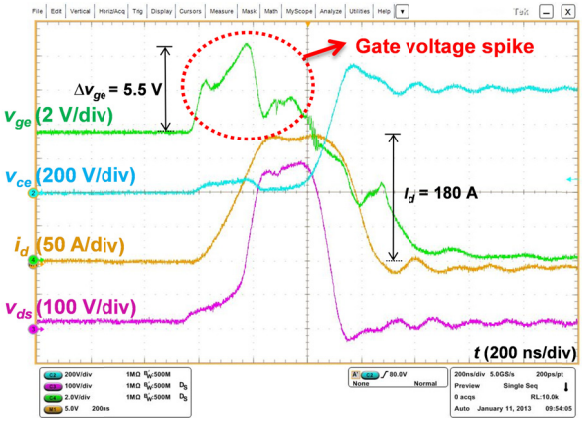


(a) Without gate zener diode

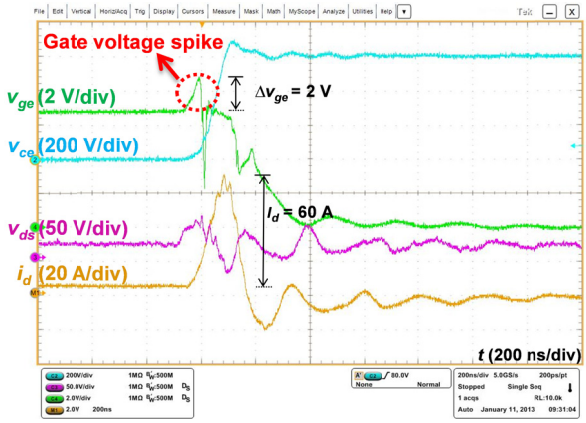


(b) With gate zener diode

Figure 6-10. Solid state circuit breaker with/without gate zener diode under HSF.



(a) Without gate zener diode



(b) With gate zener diode

Figure 6-11. Solid state circuit breaker with/without gate zener diode under FUL.

In both fault types, the gate voltage of the IGBT surges to 13 V without the gate clamping zener diode D_z, and the corresponding peak fault current is 180 A, which is about 5 times of the protection threshold. The gate voltage spike is suppressed to 8.5 V in HSF and 9.5 V in FUL by D_z. The reduced gate voltage spikes contribute to lower peak fault currents, i.e. 50 A in HSF, and 60 A in FUL. The suppressed fault current peaks are still greater than the protection threshold, mainly for two reasons. First, during short-circuit transient the internal gate voltage of the IGBT is actually a little higher than 7.5 V due to the

internal gate loop parasitic inductance and resistance. Second, the protection delay, mainly the chip internal logic delay, deteriorates the overall performance.

6.2.3 Impact of Decoupling Capacitors

In most practical applications, decoupling capacitors are required and placed close to the SiC MOSFETs to minimize the equivalent power loop parasitic inductance. During the on-state, the current of the device is mainly supplied by the energy storage capacitor C_{dc}. However, during a short-circuit, most of the fault current is supplied first by the decoupling capacitor C_s (current ①) due to relatively lower high frequency impedance, and then by the energy storage capacitor C_{dc} (current ②), as shown in Figure 6-12. This mechanism would definitely cause fault detection error and delayed fault response as the current through the SSCB is smaller than the actual fault current through the SiC MOSFETs. The detection error becomes larger with higher decoupling capacitance, and lower protection threshold.

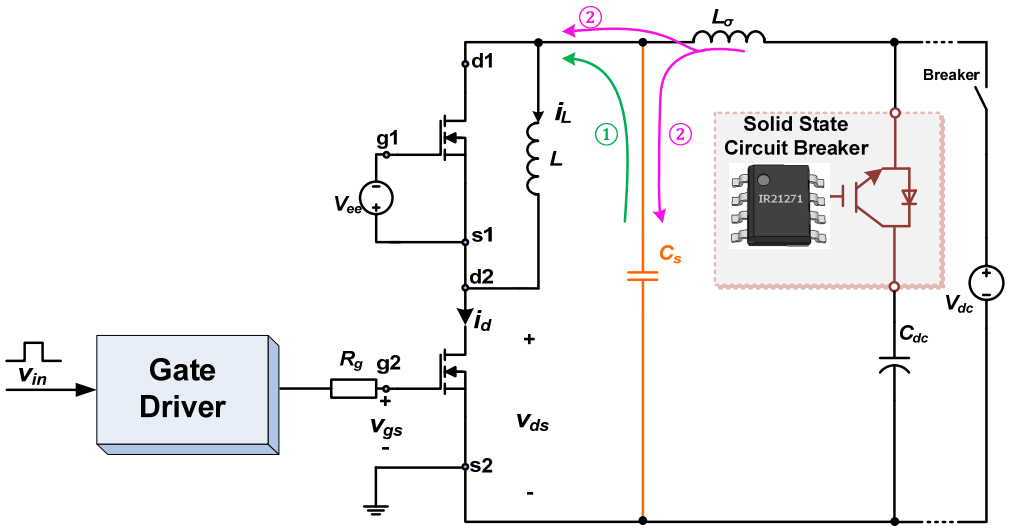
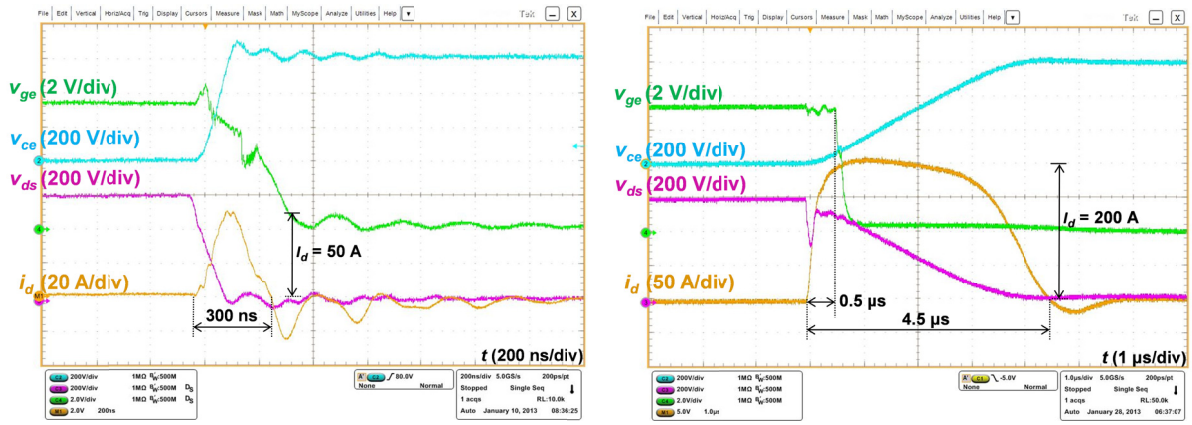


Figure 6-12. Impact of decoupling capacitance.

Figure 6-13 shows the testing results without and with 1.32 μF decoupling capacitance under HSF condition. Without decoupling capacitance, the SSCB quickly responds to the short circuit, and the fault current is cleared in 300 ns. With the decoupling capacitance, the SSCB presents delayed response. It cuts

off the energy storage capacitors after a short-circuit of 0.5 µs, while the decoupling capacitance continues discharging through the main power loop, resulting in a 4.5 µs, 200 A current pulse.



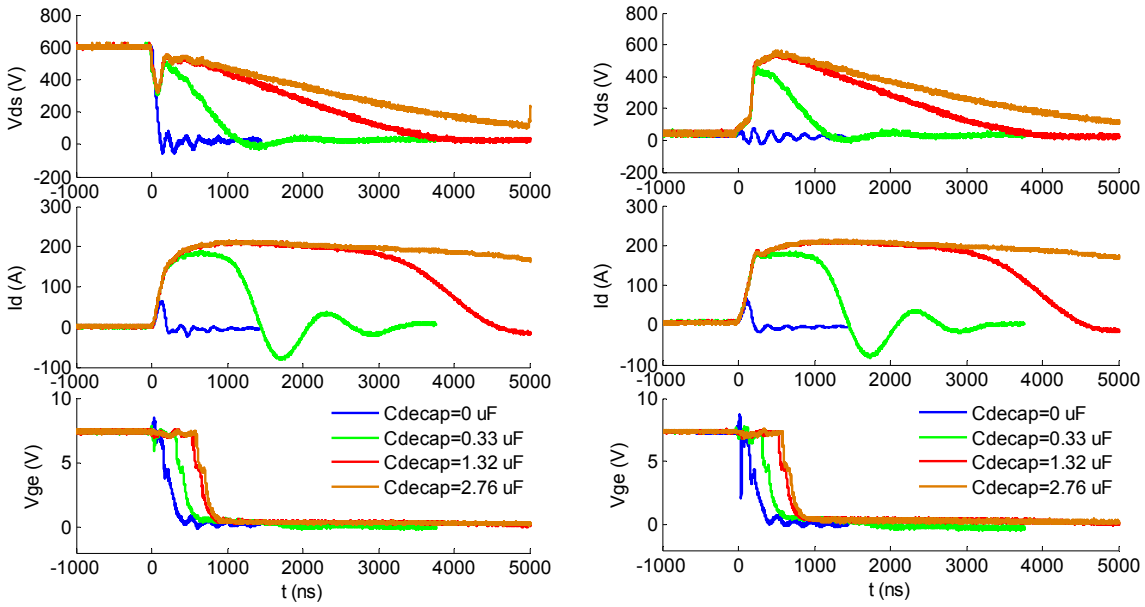
(a) Without decoupling capacitance (b) With 1.32 µF decoupling capacitance

Figure 6-13. SSCB protection with/without decoupling capacitance under HSF condition.

More testing results with different decoupling capacitances under both HSF and FUL condition are illustrated in Figure 6-14. The protection delay and fault clearing time become longer with the increase of decoupling capacitance, resulting in potential degradation and damage of the device due to local heating, as mentioned above. Hence, short-circuit performance should be taken into consideration in the design of the decoupling circuit, besides voltage spike mitigation during normal switching transitions. Although the decoupling capacitance improves the gate voltage spike of the SSCB through bypassing the high *di/dt* drain current, the delayed response impairs the overall performance of the protection scheme.

6.3 Desaturation Technique

Bipolar device (e.g. IGBTs) based power circuits have commonly used what is known as “desaturation detection” to prevent the devices from damage under overcurrent condition. When the collector current rises above the knee of their output characteristics, the device pulls out of saturation and the increased collector-emitter voltage can trigger a protection circuit.



(a) HSF (b) FUL

Figure 6-14. Impact of different decoupling capacitances under HSF and FUL condition.

For unipolar devices, e.g. MOSFETs, the desaturation protection would depend on individual types. Generally, it can be applied to high voltage MOSFETs given that their output characteristics are similar to IGBTs in the active region. However, some low voltage MOSFETs have very low drain-source voltage at rated maximum pulse current, and there is a large range of I_d that will cause device destruction before V_{ds} rises to the protection threshold. Since the protection region lies far beyond the rated maximum pulse current, they would be destroyed by overcurrent before a protection circuit ever triggers.

The subsequent question is that whether desaturation technique could be used for SiC MOSFETs. The output characteristic of the SiC MOSFET under test is shown in Figure 6-15. Unlike most Si devices which have a high impedance constant current active region (Figure 6-9), the transition from ohmic to active region for SiC MOSFETs is not clearly defined and spread over a wide range of drain current due to its short-channel effects [117]. According to Figure 6-15, the desaturation protection circuit could be triggered by the increased drain-source voltage V_{ds} of SiC MOSFETs under overcurrent condition. However, some unique features should be carefully considered in the design of desaturation detection

circuit. First, commercial IGBT/MOSFET gate drivers with desaturation detection usually have a minimum fault response time of around 3 μs. This level of response time is unsatisfactory for SiC MOSFETs taking the long-term reliability into account, and design optimization is required to achieve a sub-microsecond response time. Second, the voltage threshold is set at the knee point (around 7 V) for Si devices, while an appropriate threshold voltage for SiC MOSFETs is not straightforward due to unclearly defined active region. Third, under higher switching speed environment, the noise immunity of a desaturation detection circuit should be enhanced to avoid false triggering while maintaining a faster response time.

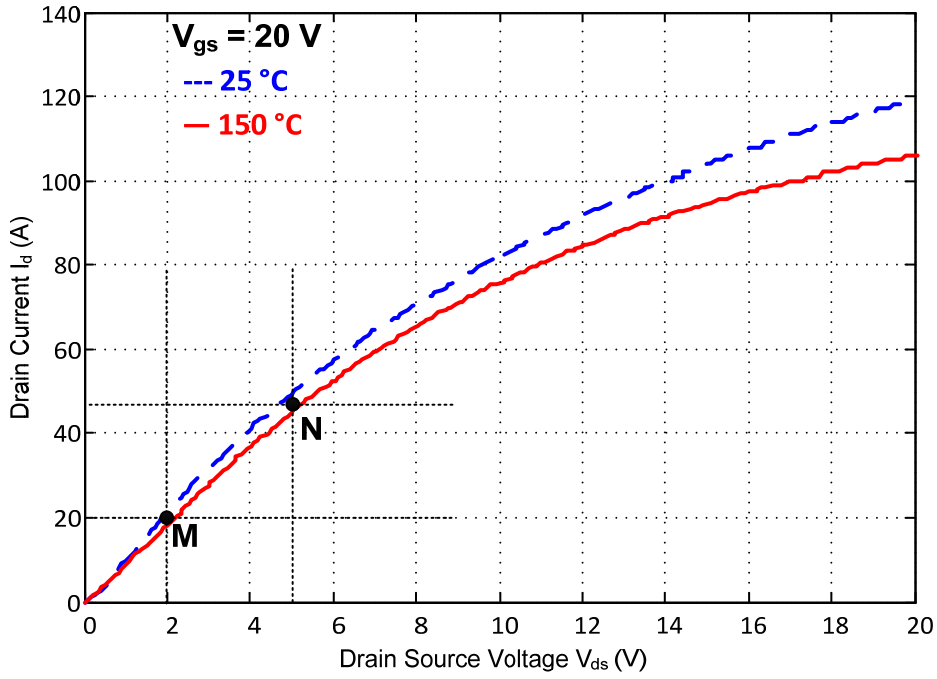


Figure 6-15. Output characteristic of the device under different temperatures.

The desaturation protection circuit implemented in this work is shown in Figure 6-16. The drain-source voltage of DUT is monitored by the sensing diode D_{ss}, and the R-C network (R_{sat1}, R_{sat2} and C_{blk}). When the DUT is "on" and saturated, D_{ss} will pull down the voltage across C_{blk}. When the DUT pulls out of saturation under overcurrent condition, the buffer output will charge C_{blk} up and trip the comparator.

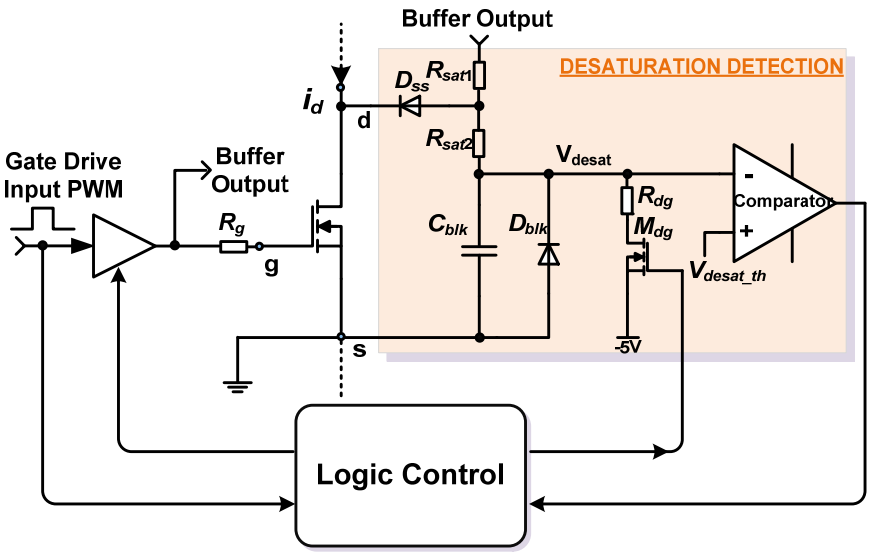


Figure 6-16. Implementation of desaturation technique.

6.3.1 Blanking Time Delay

To avoid false triggering during normal turn-on switching transients, blanking time is required to allow the drain-source voltage of the DUT to drop to its steady-state value. However, fault current could surge to a very high value during the blanking time, due to their rather large triode region.

A proper blanking time can be selected based on the turn-on switching characteristics of the power device. Since higher gate resistance and higher current level result in a longer switching transient, the turn-on switching time is compared under different voltage levels at room temperature, with an external gate resistance of 10 Ω and drain current of 20 A, as shown in Figure 6-17. In the figure, V_{buffer} is the gate drive output voltage which is synchronized with the desaturation protection circuit to charge C_{blk}.

As shown in the testing results, all of the turn-on switching transients are completed within 70 ns. With some margin, a 100~200 ns blanking time is preferable for the DUT.

The blanking time is determined by the threshold voltage V_{desat_th} and time constant of the R-C circuit τ,

$$t_{blk} = \tau \ln \frac{V_{cc}}{V_{cc} - V_{desat\_th}}, \qquad \tau = (R_{sat1} + R_{sat2}) \cdot C_{blk}. \tag{6-4}$$

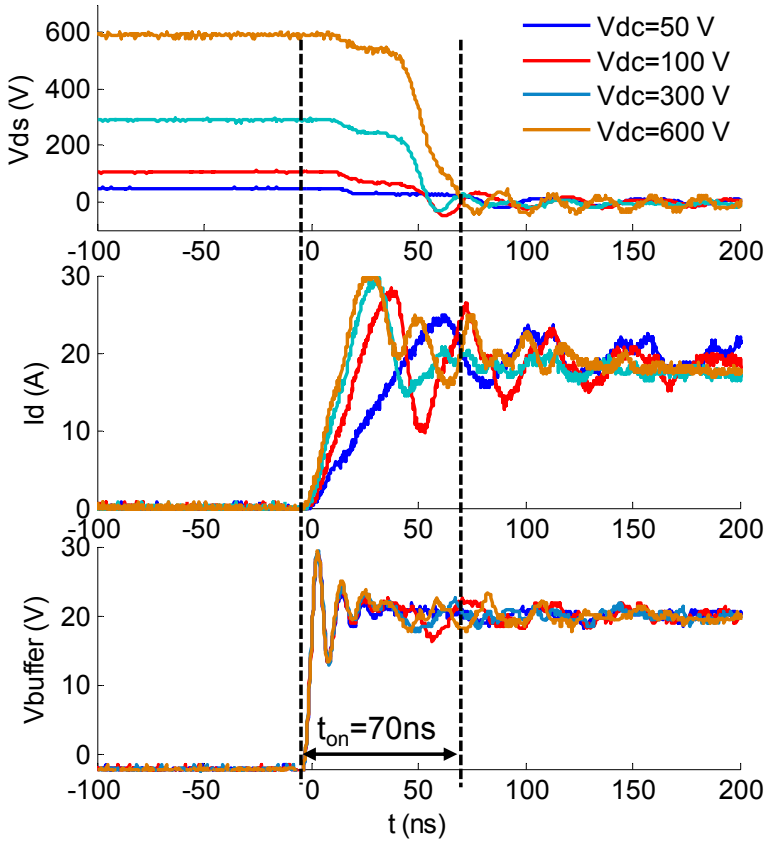


Figure 6-17. Comparison of turn-on switching waveforms under different voltage levels.

The selected V_{desat_th} in (6-4) should guarantee that the DUT operates within the SOA before the protection circuit is triggered. Based on the temperature dependent output characteristics shown in Figure 6-15, the instantaneous power dissipation of the DUT at point N $P_{d(N)}$ is close to the maximum allowable power dissipation $P_{d(max)}$ provided by the manufacturer in [118]

$$P_{d(N)} = I_{d(N)} \cdot V_{ds(N)} = 225\ (W)\ \approx P_{d(max)} = 215\ \ (W). \qquad (6-5)$$

From a normal operating point (e.g. point M) to the point N, the power dissipation is well below $P_{d(\max)}$ and the DUT always operates within the SOA before protection triggering. Actually, even though the power dissipation is fairly higher than $P_{d(\max)}$, it does not necessarily indicate that the DUT would have thermal breakdown if the pulse duration is not long enough. In this work, a somewhat conservative threshold voltage, i.e. 5 V, is selected due to limited knowledge of the device physic characteristics.

6.3.2 False Triggering Suppression

During normal switching transients, the dv_{ds}/dt of the tested 1200 V SiC MOSFET generally ranges from 20 V/ns to 40 V/ns, which is much higher than that of a 1200 V Si IGBT. This high dv_{ds}/dt can falsely trigger the desaturation protection circuit during both turn-on and turn-off switching transients.

The turn-on and turn-off dv_{ds}/dt induced displacement current together with the reverse recovery current of the sensing diode D_{ss} causes an oscillation among diode junction capacitance C_j, blanking capacitance C_{blk}, and loop parasitic inductances, as shown in Figure 6-18.

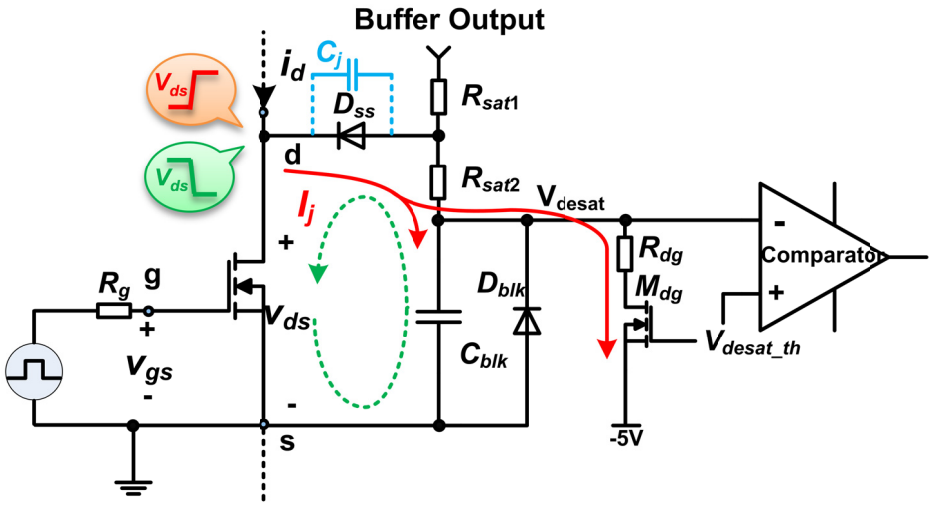


Figure 6-18. False trigger suppression at normal switching transients.

If the discharging branch (M_{dg} and R_{dg}) is deactivated and the reverse recovery current of D_{ss} is neglected, the impact of dv_{ds}/dt on the inverting input voltage of the comparator V_{desat} can be given as

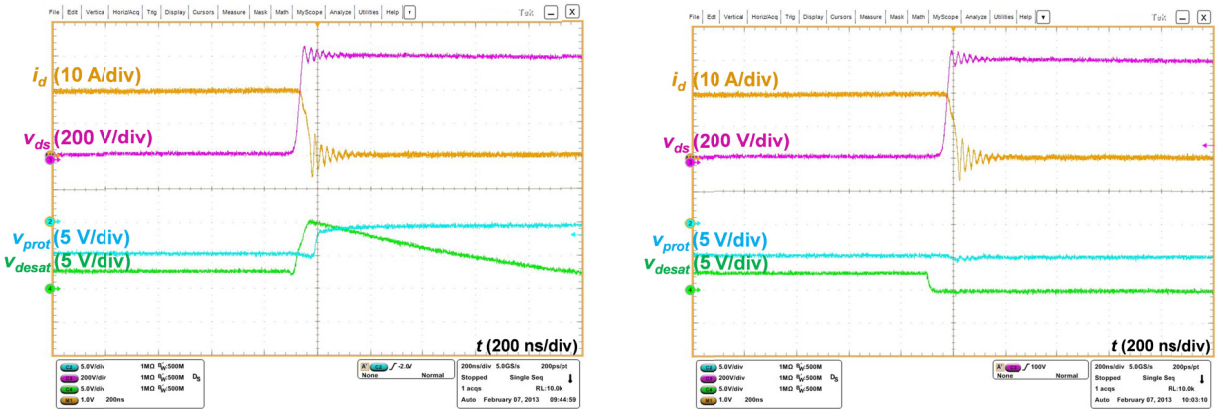
$$\frac{V_{desat}(s)}{V_{ds}(s)} = \frac{1}{1 + C_{blk}/C_j + sC_{blk}R_{sat2}}. \qquad (6-6)$$

Without R_{sat2}, V_{desat} depends on the ratio of C_{blk} and C_j. High C_{blk} can reduce the induced voltage, while it results in a significant increase of blanking time.

The contradictory effect is suppressed by the following means: (1) Connect two low current rating SiC diodes D_{ss} in series to minimize the displacement current as well as reverse recovery current; (2) Activate

the auxiliary discharging switch M_{dg} at turn-off transient to bypass the undesired current; (3) Increase the damping of the oscillation loop by a small R_{sat2} ($R_{sat2} << R_{sat1}$).

Figure 6-19 shows the turn-off transient waveforms without and with the auxiliary discharging switch, where v_{prot} represents output of the logic control. Without M_{dg}, a false protection signal is detected by the logic control circuit due to unexpected jump of V_{desat}. With M_{dg}, the blanking capacitance is fully discharged before turn-off transient, and thus a false trigger is avoided.



(a) Without auxiliary discharging switch M_{dg} (b) With auxiliary discharging switch M_{dg}

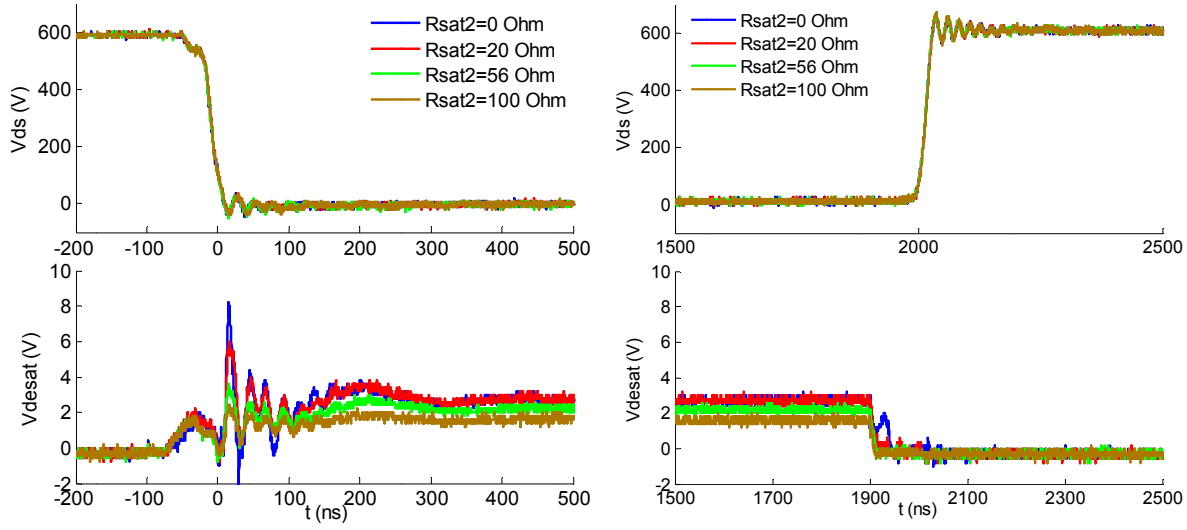
Figure 6-19. False trigger suppression at turn-off transient by auxiliary discharging switch.

Figure 6-20 shows the turn-on and turn-off transient waveforms with M_{dg} under different damping resistances for R_{sat2}. The oscillation and associated voltage noise on the blanking capacitor is gradually damped with the increase of damping resistance, at the cost of small increase in blanking time.

6.3.3 Performance Evaluation

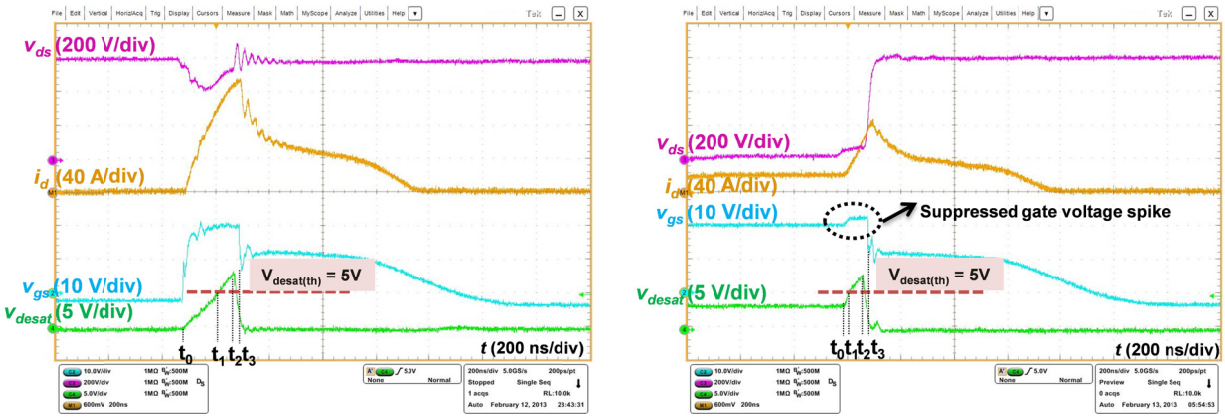
Figure 6-21 shows experimental waveforms with desaturation protection scheme under HSF and FUL condition. The blanking time is set to be 100 ns in both cases. The HSF fault current is limited to 130 A within 210 ns, and then it is clamped to around 50 A, with a corresponding clamped gate voltage of 12 V.

Following a delay of 400 ns, the device is softly turned off. However, for FUL the fault peak current is 80 A, and associated protection delay time is 110 ns.



(a) Turn-on (b) Turn-off

Figure 6-20. False trigger suppression by different damping resistances.



(a) HSF (b) FUL

Figure 6-21. Experimental waveforms with desaturation protection.

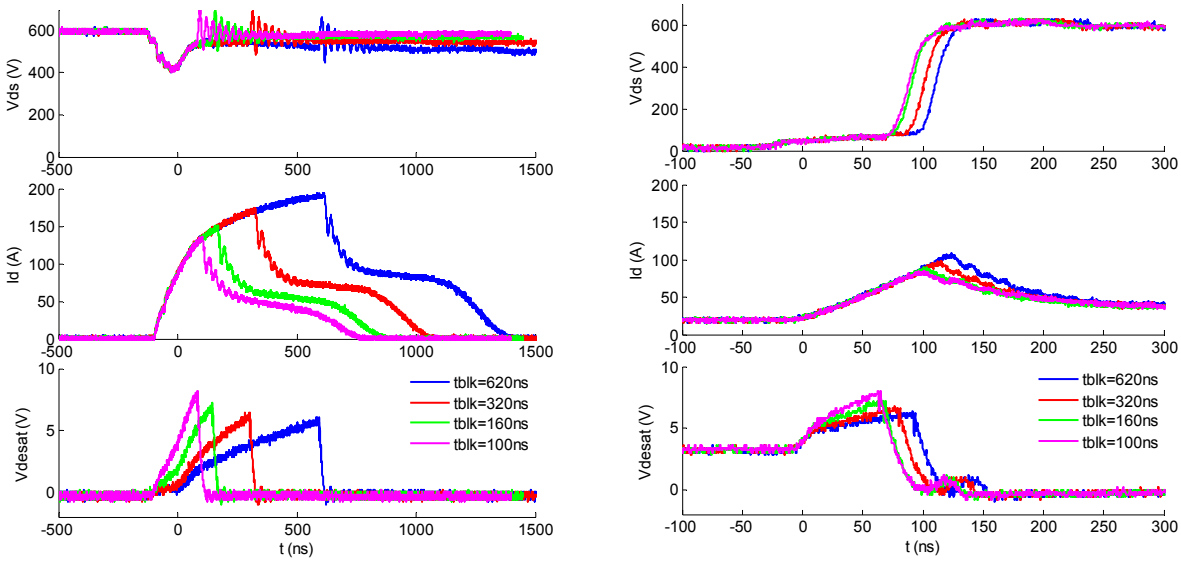
The different performance can be explained in terms of fault response, as shown in Table 6-2. Although the blanking time is the same, the induced detection delay presents a significant difference between HSF and FUL. It is a little higher than the preset value in HSF due to the parasitic capacitance of diode D_{blk}, and negative dv_{ds}/dt across the junction capacitance of the sensing diode D_{ss}. The detection delay of FUL fault is much lower than the preset value owing to initial voltage of blanking capacitance C_{blk} at fault instant, and positive dv_{ds}/dt across the junction capacitance of D_{ss}. Moreover, dv_{ds}/dt induced gate voltage spike in FUL is suppressed by the clamping diode D_z within its upper limit, and potential degradation can be mitigated.

Table 6-2. Comparison of fault response time for HSF and FUL using desaturation technique

Fault Type	Detection delay (t_0~t_1):	Comparator delay (t_1~t_2):	Logic control delay (t_2~t_3):	Total delay
HSF	120 ns	65 ns	25 ns	210 ns
FUL	20 ns	65 ns	25 ns	110 ns

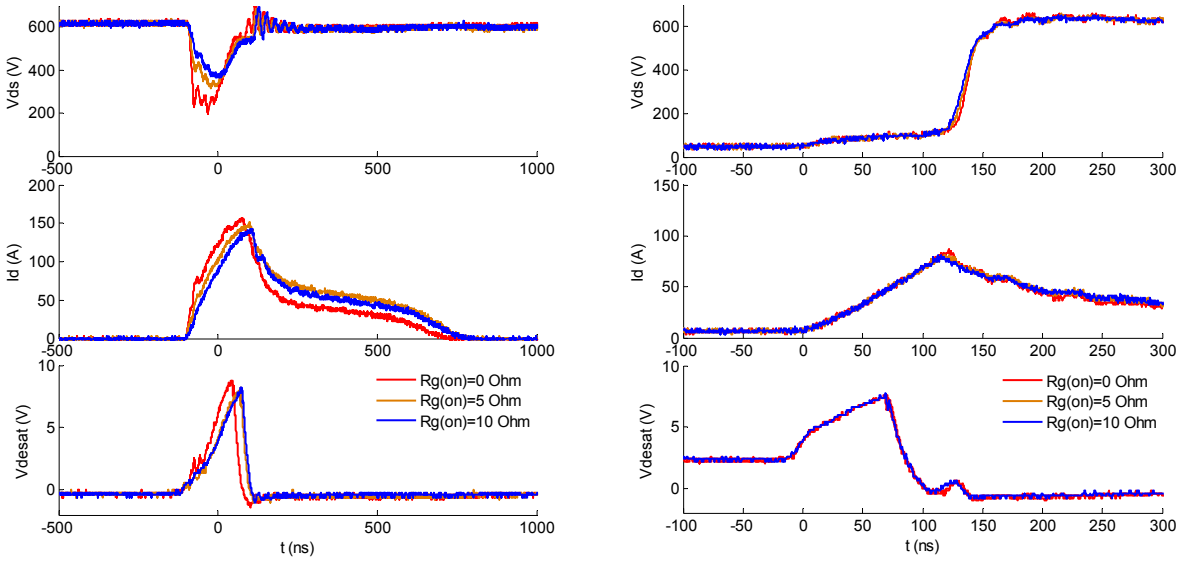
Figure 6-22 shows waveforms of desaturation protection scheme with different blanking time under HSF and FUL condition. As can be observed, longer blanking time results in higher fault current and longer protection delay.

Compared to HSF, FUL is less sensitive to the variation of blanking time since the dv_{ds}/dt effect contributes to the acceleration of fault response. More testing results with different turn-on gate resistance are shown in Figure 6-23. For HSF, lower gate resistance will increase the fault current due to higher di_{ds}/dt. However, the performance is nearly unchanged for FUL. This is because the DUT is already on before a FUL occurs, and the gate resistance has no impact on the di_{ds}/dt and fault current.



(a) HSF (b) FUL

Figure 6-22. Desaturation protection with different blanking time.



(a) HSF (b) FUL

Figure 6-23. Desaturation protection with different turn-on gate resistances.

6.4 Fault Current Evaluation Scheme

A new overcurrent protection scheme is also proposed to realize fast response time and strong noise immunity simultaneously. The block diagram of the proposed fault current evaluation scheme is shown in Figure 6-24. There are mainly four function blocks: fault current evaluation, logic control, gate voltage clamping, and soft turn-off, as discussed in detail later.

Compared to the *di/dt* monitoring based protection method [80], [84], the proposed one in this dissertation aims at estimating the peak fault current level through the passive integration of *di/dt* by a RC filter. The key advantage of the proposed method is that it could detect a short circuit without any programmed delay, despite strong ringing of drain current.

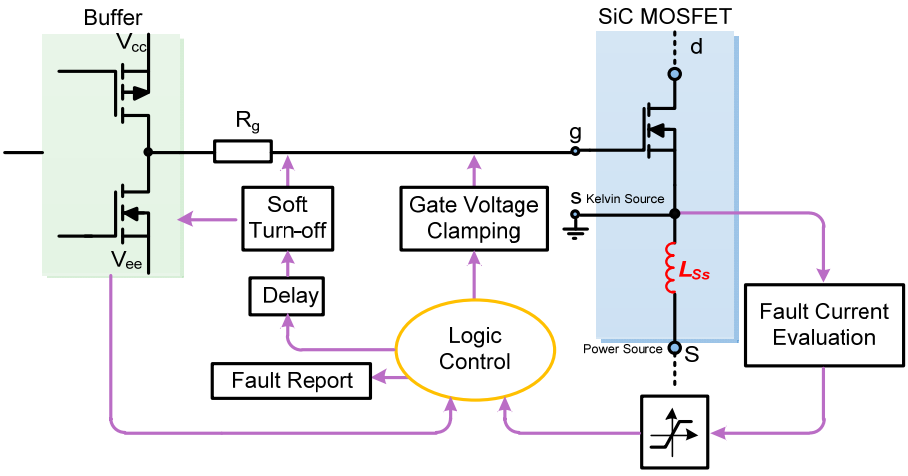


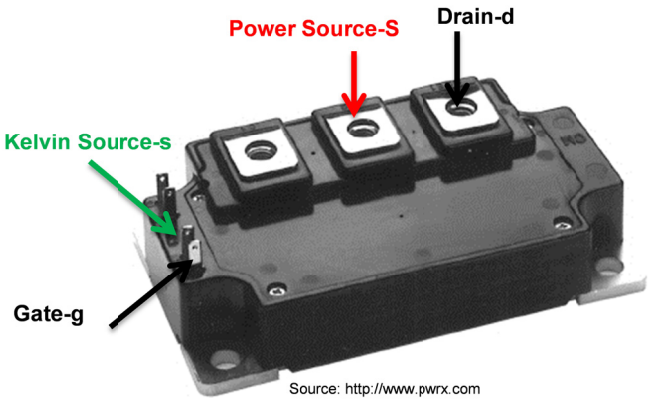
Figure 6-24. Proposed fault current evaluation protection scheme.

6.4.1 Kelvin Source Connection

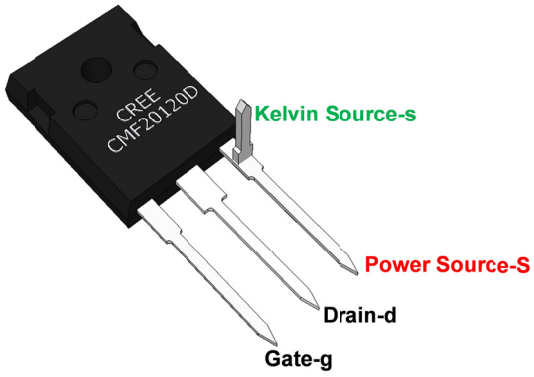
The common source inductance is the inductance that is shared by the main power loop and the gate loop. During turn-on and turn-off switching transients, this inductance establishes a negative feedback from the main power loop to the gate loop by counteracting part of the gate voltage. Consequently, SiC MOSFETs present lower switching speed, higher switching loss, and higher ringing. The impact of common source inductance has been extensively evaluated in [119]–[121].

To deal with the common source inductance effect, a Kelvin source (a separate wire to the source is provided for the source and gate return) for the gate drive is recommended by manufacturers [118], as shown in Figure 6-25. In doing so, this inductance is excluded from the gate drive loop, though it still functions as an equivalent power loop parasitic inductance.

The physical Kelvin connection of the commercial SiC MOSFET power module (Powerex QJD1210007) is shown in Figure 6-25(a), which is similar to most commercial IGBT modules. For the discrete SiC MOSFET with TO-247 package tested in this work, the Kelvin connection is realized by adding an auxiliary source pin at the root of packaging power source lead, as shown in Figure 6-25(b).



(a) Power module



(b) Discrete device

Figure 6-25. Physical Kelvin source connection of SiC MOSFETs.

6.4.2 Functionality Implementation

The circuit implementation of the proposed protection scheme is shown in Figure 6-26.

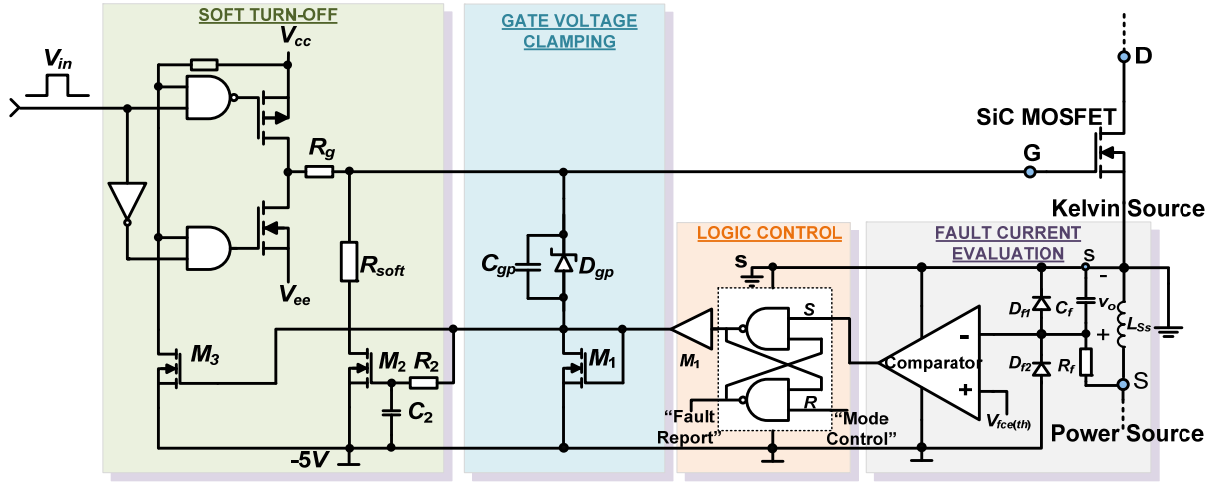


Figure 6-26. Proposed fault current evaluation protection scheme.

(1) Fault Current Evaluation

The circuit implementation of fault current evaluation functionality is shown in Figure 6-27. The current through the device during turn-on switching transient is dynamically evaluated by measuring the induced voltage across the stray inductance L_{Ss} between the Kelvin emitter and power emitter of the device.

At current rising stage of turn-on transients, the voltage drop V_{Ss} across stray inductance L_{Ss} is given as

$$V_{Ss}(s) = i_d(s) \cdot sL_{Ss}. \tag{6-7}$$

When a RC filter is applied in parallel with the stray inductance, the output voltage of the filter is

$$V_o(s) = \frac{V_{Ss}(s)}{R_f + \frac{1}{sC_f}} \cdot \frac{1}{sC_f} = \frac{V_{Ss}(s)}{sR_fC_f + 1} \tag{6-8}$$

where, R_f and C_f are the resistance and capacitance of the RC filter respectively. Substituting (6-7) into (6-8), the solution for the drain current i_d yields

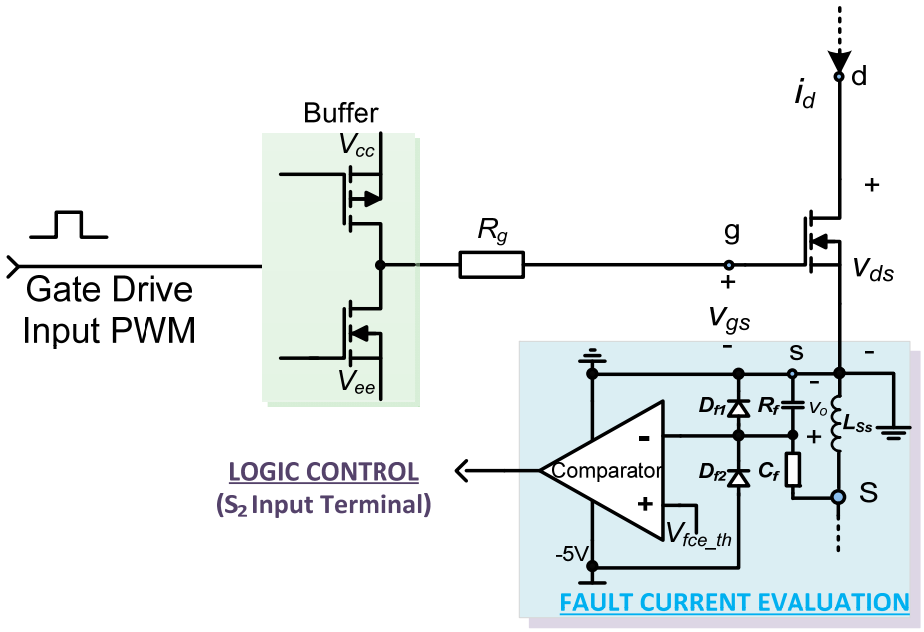


Figure 6-27. Circuit implementation of fault current evaluation functionality.

$$i_d(s) = V_o(s)\frac{sR_fC_f + 1}{sL_{Ss}}. \qquad (6-9)$$

During a short circuit transient, the steep fault current can be evaluated by

$$i_d(s) = V_o(s)\frac{R_fC_f + \frac{1}{s}}{L_{Ss}} \approx V_o(s)\frac{R_fC_f}{L_{Ss}}. \qquad (6-10)$$

Equation (6-10) indicates that the fault current is proportional to the output voltage of the filter. Under certain stray inductance L_{Ss} and fixed values of R_f and C_f, the current protection threshold could be adjusted by selecting different references for voltage $V_o(s)$.

The stray inductance L_{Ss} between the Kelvin source and power source can be identified through experimental measurement of V_{Ss} and i_d during turn-on transient, as shown in Figure 6-28, where $L_{d(int)}$, $L_{s(int)}$, and $L_{g(int)}$, represent the drain, source, and gate parasitic inductance within device package, respectively; R_g represents the internal gate resistance; L_{ks} is the parasitic inductance induced by Kelvin connection.

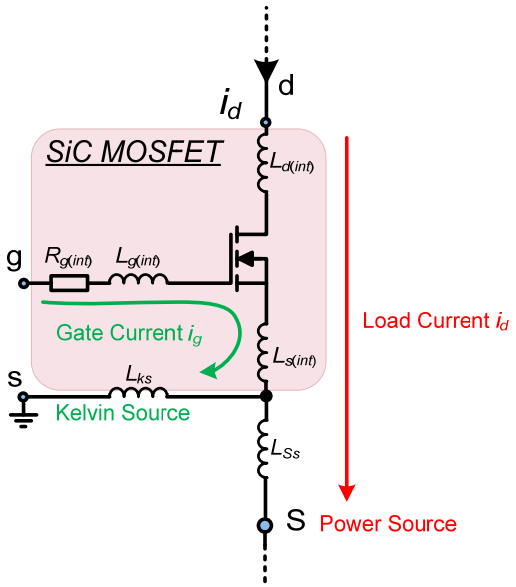


Figure 6-28. Identification of stray inductance L_{Ss} through experiment.

The resulting voltage V_{Ss} between the power and the Kelvin source terminals is given by the inductances L_{ks}, L_{Ss}, and the derivatives of the gate and drain currents:

$$V_{Ss}(s) = -L_{Ss}\frac{di_d}{dt} + L_{ks}\frac{di_g}{dt}. \qquad (6-11)$$

As the polarities of the two induced voltages in (6-11) are different and the gate has to be partially charged through gate resistance before the rising of drain current, the di_d/dt and di_g/dt induced voltage which appear at different stages can be easily identified, as shown in Figure 6-29. Moreover, since the di_g/dt is much lower than di_d/dt during drain current rising stage, L_{Ss} is simplified as

$$L_{Ss} \approx \frac{-V_{Ss}(s)}{\frac{di_d}{dt}} = \frac{-6.8\,V}{1.045\frac{A}{ns}} = 6.5\ (nH). \qquad (6-12)$$

In practical measurements, L_{Ss} values at different current/voltage levels and gate resistance, are evaluated and averaged for more accurate results. The inductance L_{Ss} is estimated to be 6.5 nH. The current evaluation waveform with R_f = 200 Ω, and C_f = 1 nF is shown in Figure 6-30. The experimental value (0.92 V) is a little lower than the theoretical evaluation given by (6-10), due to neglecting the term $1/s$,

$$V_o(s) = i_d(s) \cdot \frac{L_{Ss}}{R_f C_f} = 29A \cdot \frac{6.5nH}{200\Omega \times 1nF} = 0.95V. \qquad (6-13)$$

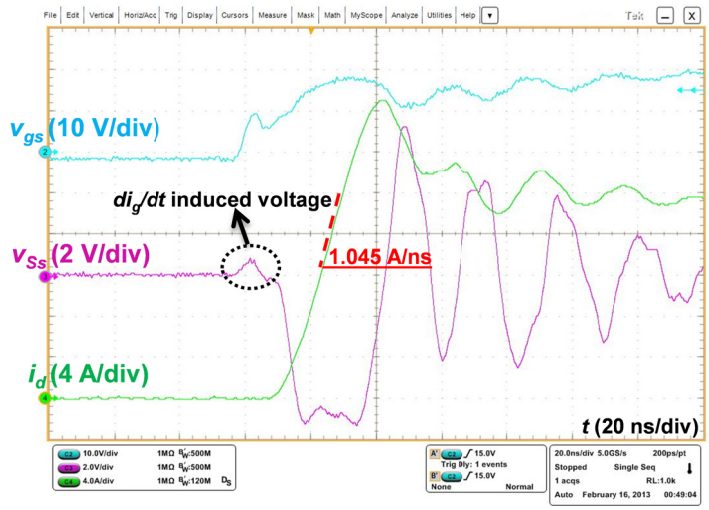


Figure 6-29. L_{Ss} measurement through V_{Ss} and di_d/dt in experiment.

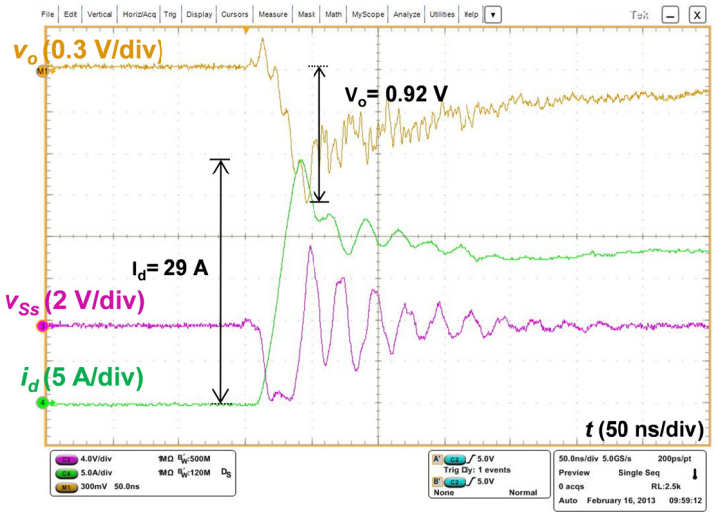


Figure 6-30. Current evaluation during turn-on transient.

Figure 6-31 illustrates the relationship between the filter peak output voltage V_o and peak drain current i_d, both in theoretical calculation and in experimental measurement with different combinations of filter parameters R_f and C_f. The measured result is close to the calculated one with R_f (200 Ω) and C_f (1 nF),

while it deviates from the calculation in the case of a higher R_f (2 kΩ) and lower C_f (0.1 nF). The reason is that the total parasitic capacitances (including the input capacitance of the comparator and junction capacitances of clamping diodes D_{f1} to D_{f2}) are comparable to C_f, and the increased equivalent capacitance would decrease the output voltage V_o. Generally, C_f should be higher than 1 nF to avoid the parasitic capacitance effects. On the other hand, the capacitance of C_f should be as low as possible to present high impedance together with R_f during switching transients, and thus the normal switching performance would not be affected.

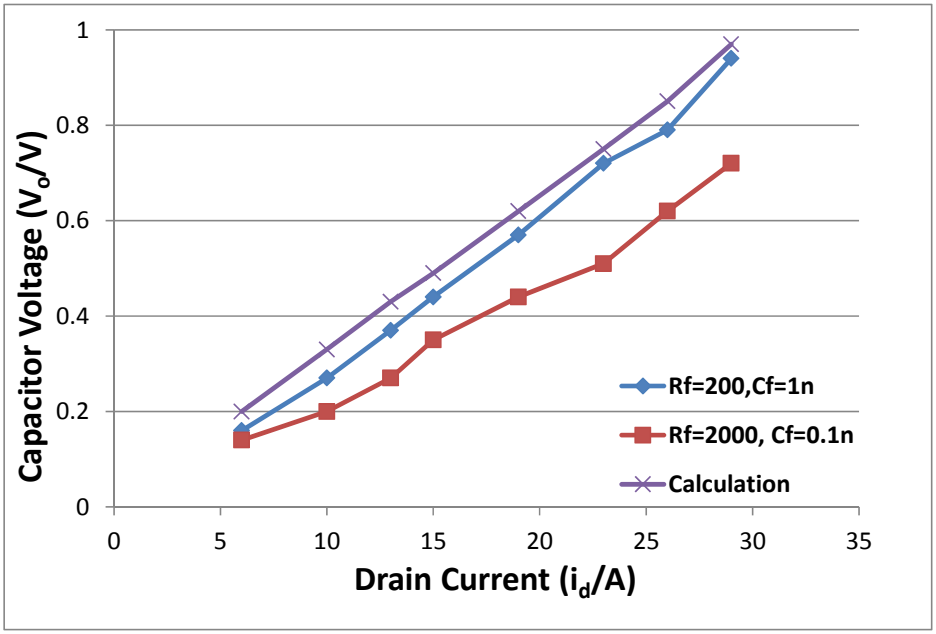


Figure 6-31. Measured filter output voltage V_o and peak drain current.

(2) Logic Control

The proposed overcurrent fault detector consists of a latch circuit and a clamping circuit regulating the feedback signal to normal ranges, as shown in Figure 6-26.

One input of the latch circuit (S terminal) is connected to the output of the RC filter. During normal operation, the S terminal is in high state, the detector output keeps unchanged. Under fault condition, when the S input reaches the maximum allowable low-level input voltage of R-S latch (around 0.8 V), a

fault is detected. In order to realize flexible protection thresholds, an additional voltage comparator can be inserted between the S terminal and RC filter in a practical implementation. With the default threshold of R-S latch, R_f = 200 Ω, and C_f = 1 nF, the protection threshold is set to 25 A according to Figure 6-31. Upon the change in detector state, the high level output will drive the following stages to respond to the fault. In addition, the detector is able to report a fault to the system microprocessor when a fault is detected.

The other input (R terminal) receives the protection mode information determined by users. Specifically, two optional protection modes are implemented: single-mode, with R terminal set to be high level, and multiple-mode, with R terminal synchronized to the input PWM signal of gate driver (v_{in}). For single-mode, the gate driver will be shut down once a fault is detected. However, for multiple-mode, the gate driver will only be blocked in the fault switching cycle. The gate driver continues to work until a shutdown signal is sent by a microprocessor counting the reported fault times. For example, the microprocessor may send a shutdown command to the gate driver when the cumulative number of faults is greater than three within a certain period of time.

(3) Gate Voltage Clamping

Under fault condition, especially FUL condition, the gate voltage of SiC MOSFET would be increased and eventually exceed its upper limit specified by the manufacturer (+25 V) [118], due to a large *dv/dt* across the miller capacitance and gate resistance. This increased gate bias, i.e. increased electric field in the gate oxide, causes a higher tunneling current into the dielectric, thus accelerating the degradation and destruction of SiC MOSFETs. On the other hand, the gate voltage spike would induce a larger fault current during short circuit transient, like the case in SSCB discussed above.

To deal with these issues, a discharging capacitor C_{gp} and zener diode D_{gp}, actively controlled by transistor M_1, are employed as shown in Figure 6-26. Once a fault is detected, M_1 is turned on, which causes C_{gp} to charge up to the voltage level of D_{gp}, thus effectively discharging the gate capacitance and suppressing gate voltage spikes. The final gate voltage and fault current level are clamped by D_{gp}.

The value of C_{gp} should be selected carefully in that a large C_{gp} value results in unexpected fast turn-off of IGBT modules and a slow ramp up to the clamp current level, while a small one results in a high peak fault current due to insufficient gate discharge. The value of the zener voltage is selected such that the fault current is clamped to a safe current level and the clamped gate voltage is above the threshold voltage to avoid fast turn-off, e.g. 10 V ~ 13 V, while an optimized one should still be determined through experimental test.

Compared to the active clamping with a single voltage level, zener clamping is more flexible since there is a wide range of zener diodes with different breakdown voltages. In addition, some variation of the gate clamping voltage due to the spread of the zener diode breakdown voltage and the slope in the output characteristics is allowed because the clamped safe current level does not need to be very accurate.

(4) Soft Turn-off

Although the negative voltage bias is able to accelerate the process of interrupting a short-circuit current, the SiC MOSFET has to be softly turned off to reduce voltage overshoot due to the effect of power-loop stray inductance and high *di/dt* under short-circuit condition. When the logic control output is activated, the buffer is disabled by turning on M_3, and a large gate resistor R_{soft} is inserted into the gate to turn off the device at a reduced rate of gate voltage change following a delay.

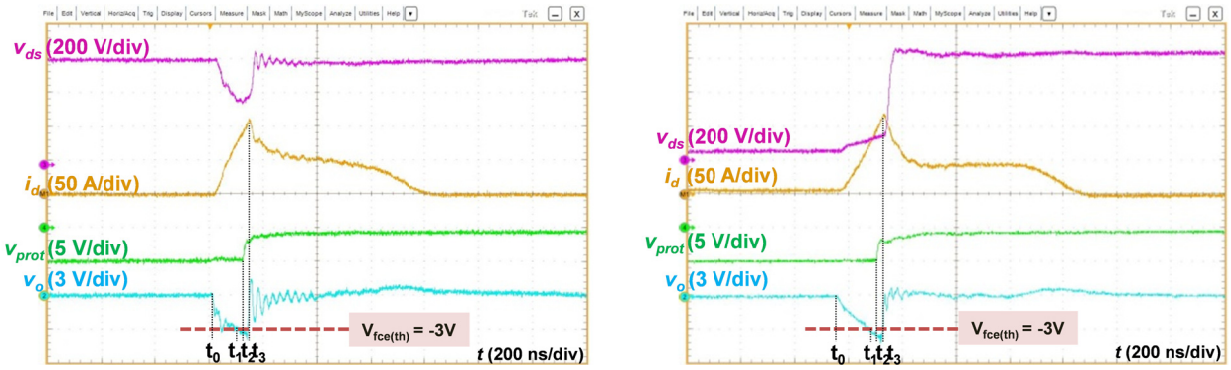
6.4.3 Performance Evaluation

Figure 6-32 shows experimental waveforms with the fault current evaluation protection scheme under HSF and FUL condition. With R_f = 200 Ω, C_f = 1 nF and $V_{fce(th)}$ = -3 V, the current protection threshold is around 100 A in both cases according to (6-10).

The HSF fault current is limited to 130 A within 140 ns, and then it is clamped to around 50 A, with a corresponding clamped gate voltage of 12 V. Following a delay of 400 ns, the device is softly turned off. Similar protection characteristics are also shown under FUL, while its fault peak current (120 A) is a little higher due to larger protection delay. The detailed fault response analysis is shown in Table 6-3.

Although the protection threshold is the same, the induced detection delay still presents some difference. The reason is that the *di/dt* of HSF and FUL depends respectively on the DUT and short-

circuit control transistor. In addition, it is worth mentioning that the comparator delay is much lower than the desaturation technique since a low-voltage (+5 V) high speed comparator is used in this case.



(a) HSF (b) FUL

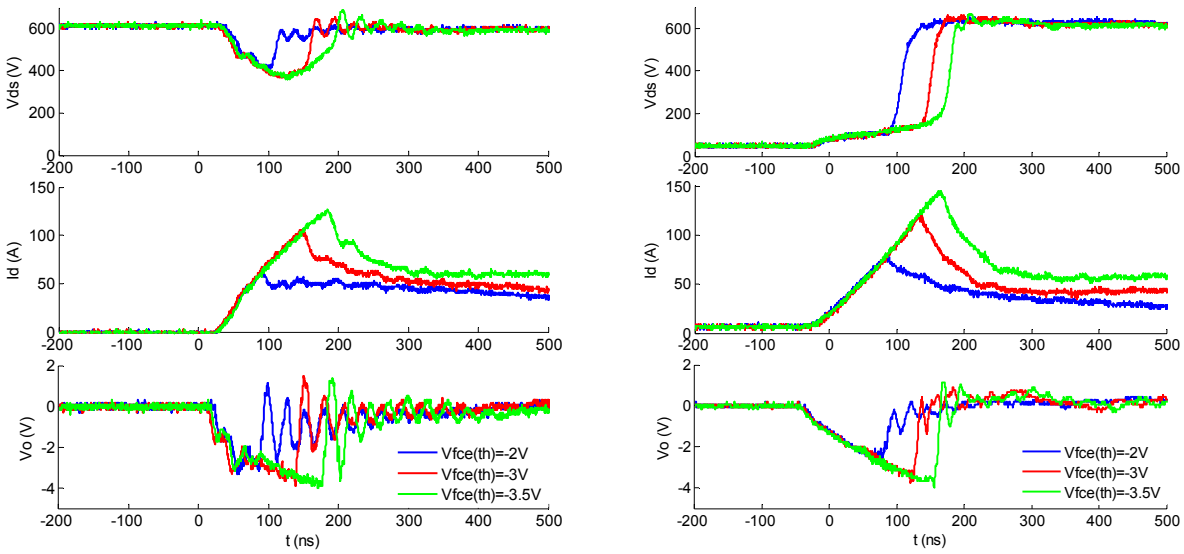
Figure 6-32. Experimental waveforms with fault current evaluation protection.

Table 6-3. Comparison of fault response time for HSF and FUL using proposed technique

Fault Type	Detection delay (t_0~t_1):	Comparator delay (t_1~t_2):	Logic control delay (t_2~t_3):	Total delay
HSF	100 ns	15 ns	25 ns	140 ns
FUL	130 ns	15 ns	25 ns	170 ns

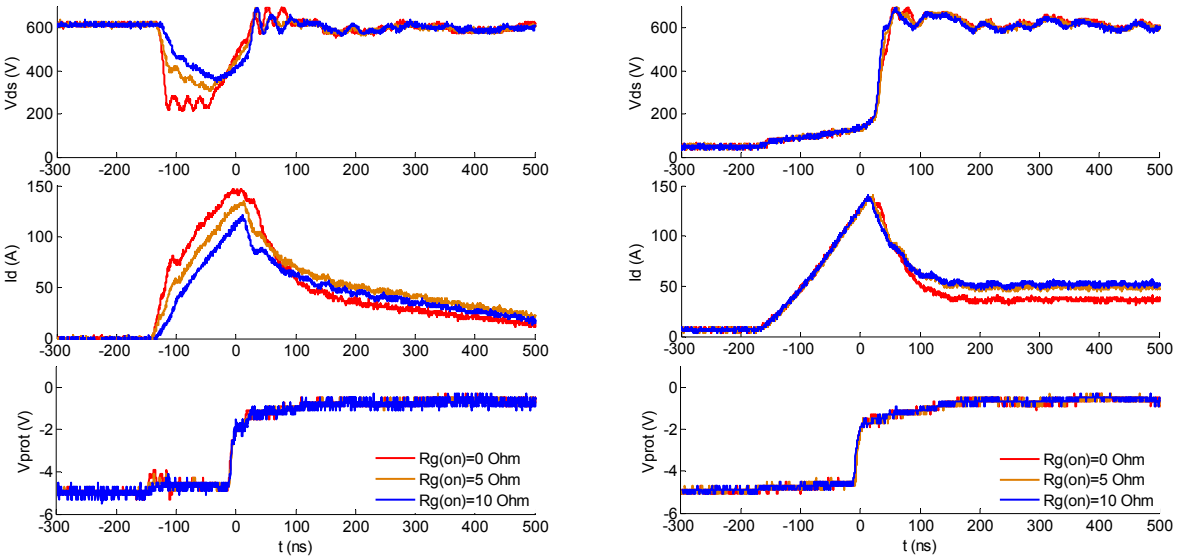
Figure 6-33 shows fault transient waveforms of the protection scheme with different threshold voltages under HSF and FUL condition. As can be seen, higher protection threshold results in higher peak fault current and longer protection delay.

The testing results with different turn-on gate resistances are shown in Figure 6-34. For HSF, lower gate resistance will increase the fault current due to higher di_{ds}/dt. However, the protection performance for FUL keeps nearly unchanged. The reason is that the DUT is already on before a FUL fault occurs, and thus the gate resistance has nearly no impact on the di_{ds}/dt and fault current. The protection circuit operating in different protection modes is the same as the desaturation protection, and is not repeated here.



(a) HSF (b) FUL

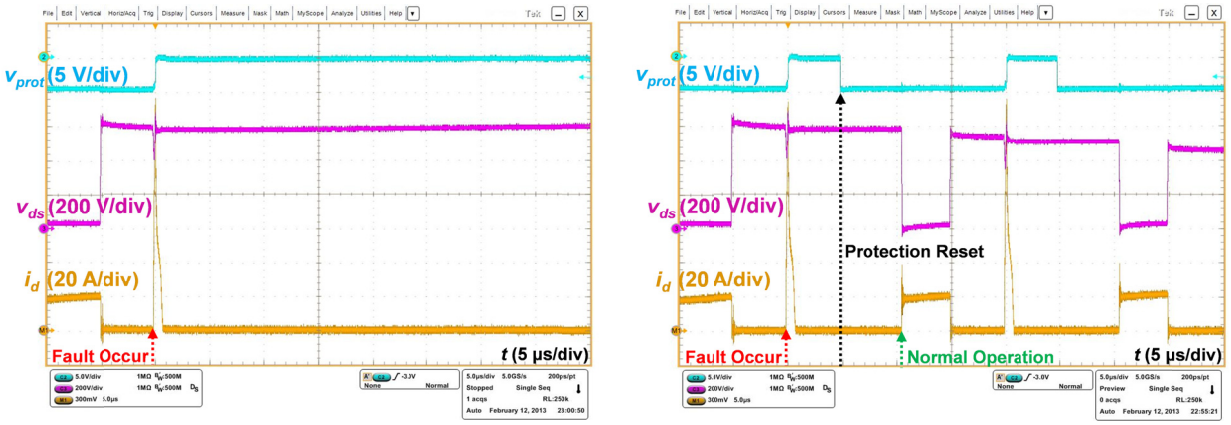
Figure 6-33. Fault current evaluation protection with different threshold voltages.



(a) HSF (b) FUL

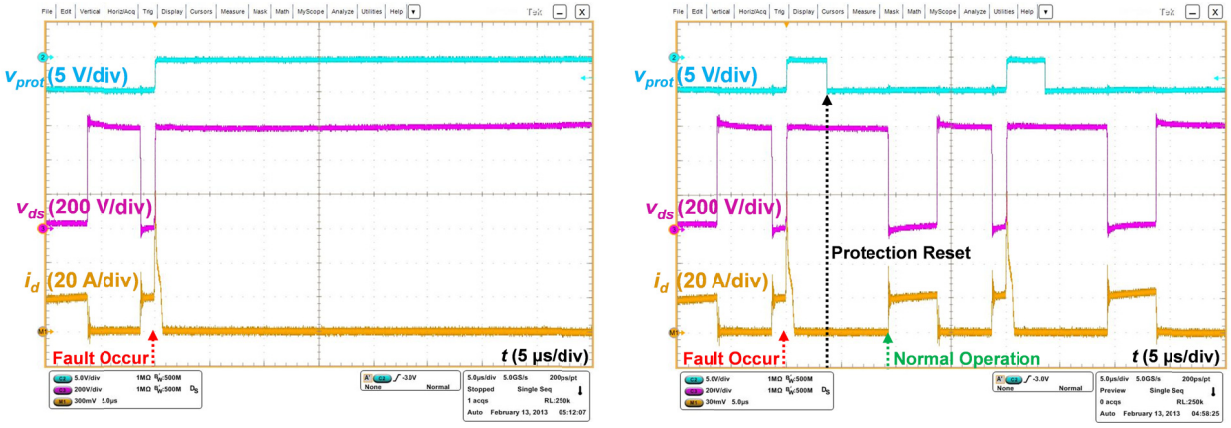
Figure 6-34. Fault current evaluation protection with different turn-on gate resistances.

Figure 6-35 and Figure 6-36 show the protection circuit operating in different protection modes under HSF and FUL, respectively. As can be observed, once a fault is detected, the gate driver is shut down in single-mode, despite the turn-on PWM signal after the fault instant. While in multiple-mode, the fault is protected cycle-by-cycle, and the protection circuit automatically resets before the next 'on' cycle, i.e. the gate driver is restarted and SiC MOSFET continues to work until a shutdown command is received.



(a) Single mode (b) Multiple mode

Figure 6-35. Protection of HSF with different protection modes.



(a) Single mode (b) Multiple mode

Figure 6-36. Protection of FUL with different protection modes.

6.5 Discussion

Up to this point, three different protection schemes that can be used for overcurrent protection of SiC MOSFETs have been discussed. The purpose of this section is not to determine the best one, but explore the benefits and drawbacks of each method, and its potential applications. A fair comparison among the three protection techniques is difficult, considering that application cases and design optimization targets vary from design to design. The focus of this discussion is a comparison of their fault response time, temperature dependent performance, and potential applications.

6.5.1 Fault Response Time

The fault response time is one of the most crucial factors in overcurrent protection, while it depends on different design cases. In this work, the fault response time is pushed closer to its lowest limit in order to avoid potential degradation of the SiC devices.

Based on the experimental results shown in the previous sections, the fault response time and corresponding fault peak current of the three methods under HSF and FUL are summarized in Figure 6-37.

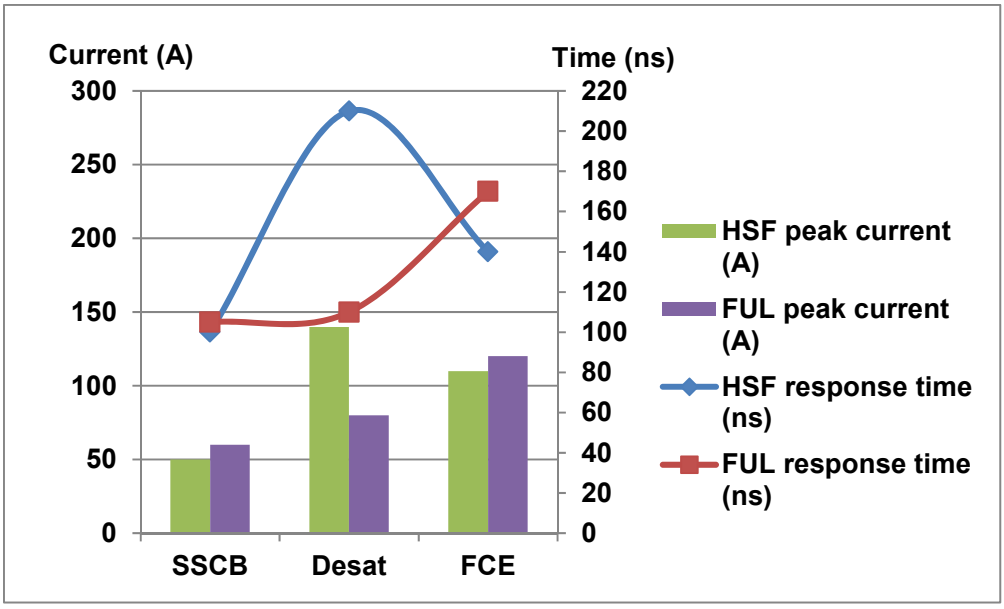


Figure 6-37. Comparison of fault response time and peak current.

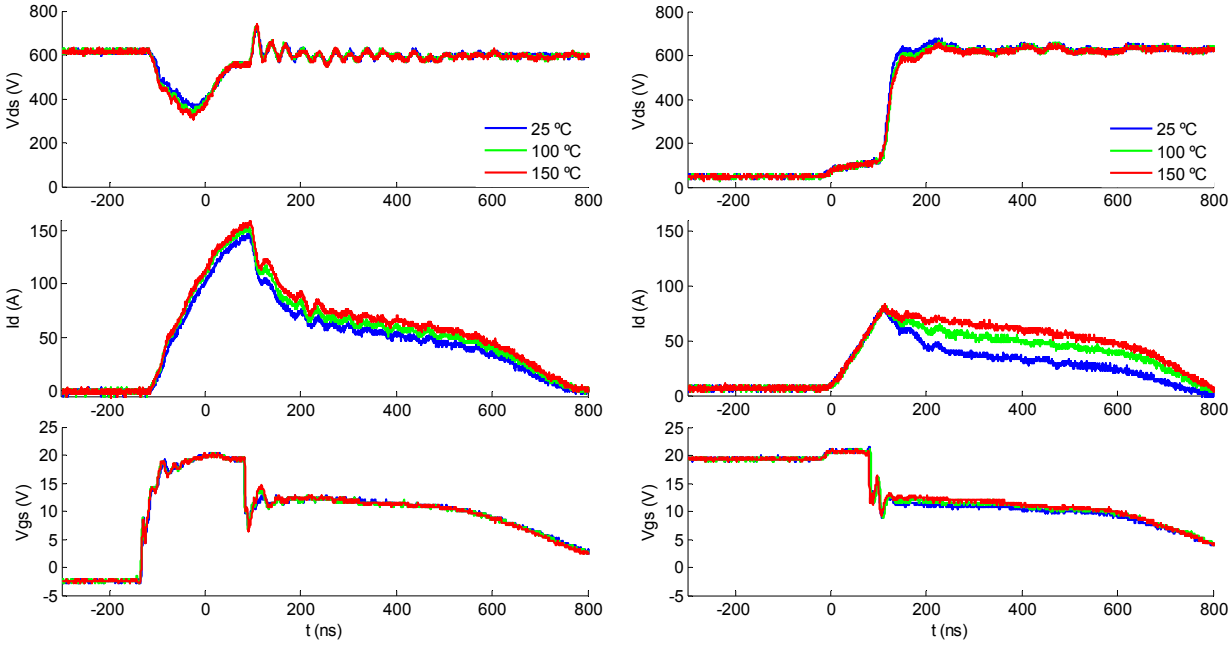
The SSCB has the quickest fault response time and nearly the same response time for both HSF and FUL. The desaturation (Desat) technique has the longest fault response time under HSF, but very short fault response time under FUL. This large difference results from the dv_{ds}/dt across the junction capacitance of the desaturation detection diode at fault transient. The fault current evaluation (FCE) method shows moderate performance under HSF, but the worst performance when protecting a FUL, the most serious threat to SiC MOSFETs.

The fault peak current has a similar trend as that of fault response time since the *di/dt* is identical under different cases. Without decoupling capacitance, the fault peak current can be controlled to a very low level by the SSCB. However, it will increase far beyond this level due to the discharge of decoupling capacitance. Unfortunately, many applications do have more or less decoupling capacitance, which limits its application to some extent. Regardless of decoupling capacitance values, both the desaturation technique and fault current evaluation have fast response against shoot-through faults where *di/dt* is extremely high, whereas this response time is subject to extension under faults with large short-circuit impedance, e.g. ground fault. The high impedance short-circuit caused low *di/dt* fault current generally can be detected by current sensors of converters. The impact of different short-circuit impedance is beyond the scope of this dissertation.

6.5.2 Temperature Dependent Performance

The variation of junction temperature will cause some changes on device characteristics/parameters. However, it has no impact on SSCB that relies on its own power device instead of the SiC MOSFET.

The influence of different temperature on desaturation protection is shown in Figure 6-38. Both the turn-on dv_{ds}/dt and di_d/dt become faster as the temperature rises, as explained in [72]. As seen, the fault response time keeps unchanged with the variation of temperature under both HSF and FUL. The clamped current levels in both fault types increase due to the increase of transconductance g_m as temperature rises.



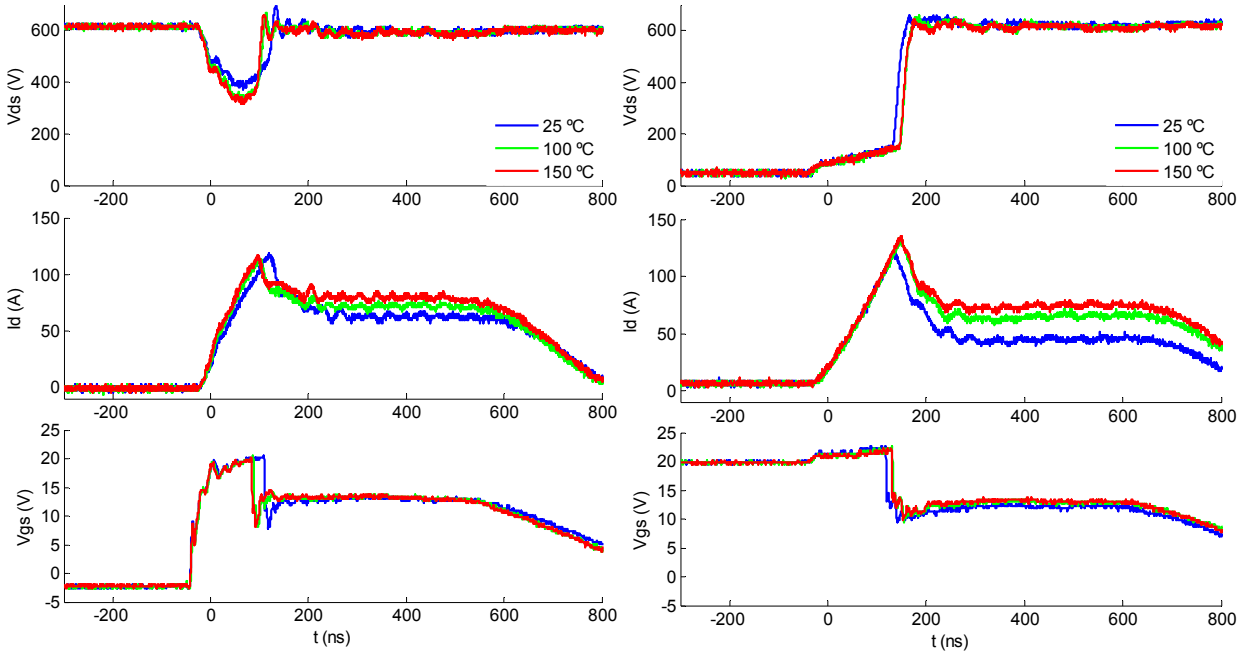
(a) HSF (b) FUL

Figure 6-38. Desaturation protection under different junction temperature.

The influence of different temperatures on fault current evaluation scheme is shown in Figure 6-39. The fault current evaluation method presents faster fault response time of HSF thanks to the increased di_{ds}/dt at high temperature. The clamped current levels also increase due to the increase of transconductance g_m as temperature rises.

The temperature dependent fault peak current of the three methods under HSF and FUL is illustrated in Figure 6-40. The SSCB shows the best temperature dependent performance since it is operated independent of junction temperature of the device under test. For the desaturation technique, the di_{ds}/dt of HSF increases with the rise of temperature, while the di_{ds}/dt of FUL controlled by short-circuit control switch does not change. Consequently, the fault peak current of HSF increases slightly at higher temperature, and remains the same in FUL. The fault current evaluation method presents opposite temperature dependent characteristics under HSF and FUL. The peak value of HSF decreases a little

thanks to the faster response time at higher temperatures, while the fault current peak value of FUL increases with temperature.



(a) HSF (b) FUL

Figure 6-39. Fault current evaluation under different junction temperature.

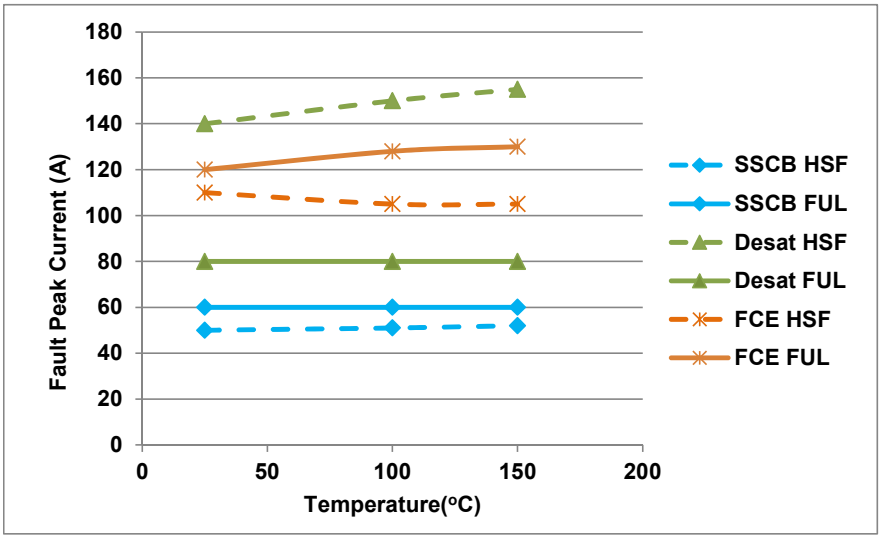


Figure 6-40. Comparison of temperature dependent fault peak current.

The possible reason is that the filter resistance R_f, which is physically close to the SiC MOSFET, is heated together with the power device. Hence, the protection threshold becomes higher due to the temperature effect, as shown in Figure 6-39(b). Moreover, the current sensor (Pearson 2877), which is not fully heat-shielded, may also have an impact on the current measurement at high temperatures, while the specific temperature characteristic is not clearly indicated by the manufacturer.

6.5.3 Applications

According to their operating principle, it can be observed that the SSCB does not rely on the specific device packages but it strongly depends on the system-level packages due to its relatively large volume. The desaturation technique is neither device package dependent nor system-level package dependent, and thus can be readily integrated into a gate drive circuit. However, the fault current evaluation method is inherently suitable for power modules with built-in parasitic inductance between Kelvin source and power source terminal. However, this parasitic inductance, depending on packaging techniques, varies from module to module, which impairs the generality of this method to some extent. Nonetheless, this inductance is not difficult to be identified and calibrated through experimental measurements. Moreover, for the whole converter using the same SiC MOSFET devices/power module, the calibration process needs to be done only once.

Because the protection performance of the SSCB is independent of specific devices, it is suitable to protect a converter including different types of SiC MOSFETs and even Si devices. Also, it can be used for any power/current level. They key issue is the considerable power loss under high power/current level applications such as the typical back-to-back converter in a renewable energy system. However, the power dissipation would still acceptable in the application with low active power flow in the DC link, e.g. active power filters (APF), static var generator (SVG), double pulse tester (DPT).

The desaturation technique can be applied to a wide range of power/current levels, while it may not work effectively at low voltage levels. As a result of easy integration and low power dissipation, it is preferable to be used in high temperature and high density application, like electric vehicle (EV) / hybrid electric vehicle (HEV) and aircraft.

The fault current evaluation method is targeted at power modules and high power/current levels. Similar to the desaturation technique, it may not work effectively at low voltage levels due to low *di/dt*. From the integration point of view, it has a large overlap with the desaturation technique, while the potential application in high temperature environment still needs further investigation.

The primary difference between the potential applications of desaturation and fault current evaluation method is summarized as follows:

1) As mentioned above, desaturation technique can be used for any device package and current level, while fault current evaluation method is generally applied to power modules.

2) Compared to the desaturation technique based on the temperature dependent nonlinear I-V characteristics, the fault current evaluation method has a temperature independent linear I-V relationship, which indicates that the latter one is much easier to set an accurate protection threshold to limit the fault current to an expected level.

3) In a converter built by different types of SiC MOSFETs, the fault current evaluation method needs more effort on calibration, while desaturation technique only needs to change the voltage protection threshold slightly according to their output characteristics.

6.5.4 Other Factors

Besides those aspects discussed above, other factors including overall cost, reliability, power dissipation, implementation and integration complexity should also be taken into consideration to select a proper overcurrent protection method for SiC MOSFET based converters.

For example, the SSCB has fairly good reliability and generality to protect different types of SiC MOSFETs. However, it creates high power dissipation, and is relatively expensive and bulky. In addition, it requires a separate isolated power supply and gate driver to operate. The reliability of the protection method in this work means that whether the protection technique can be triggered under any short-circuit condition. A broader definition of the reliability should be a comprehensive factor with many other aspects involved, power dissipation and related degradation issues, component number, component failure rate, etc.

In contrast, the desaturation detection circuit has very low power dissipation and low cost. This technique, however, is rather complex because it requires deliberate circuit design to achieve a fast fault response, accurate synchronization with the gate signal, as well as good reliability for different types of SiC MOSFETs.

The fault current evaluation scheme also has very low power dissipation and cost, while it may present relatively lower reliability to protect different types of SiC MOSFETs due to the variation of stray inductance. The comparison of the three overcurrent protection methods is summarized in Table 6-4.

Table 6-4. Comparison of the three protection methods.

Features	**SSCB**	**Desat**	**FCE**
Power Loss	High	Low	Very low
Generality	Very good	Good	Bad
Reliability	Very good	Good	Good
Implementation Complexity	Medium	High	High
Integration Complexity	High	Low	Medium
Cost	High	Low	Low

6.6 Conclusion

In this chapter, the requirements for short circuit protection of SiC MOSFETs are proposed considering single-event, repetitive fault conditions, and noise immunity. To meet these requirements, three overcurrent protection methods have been presented for SiC MOSFETs under both hard switching fault and fault under load condition. The design consideration and associated issues of these methods are analyzed and verified through experiments. A qualitative comparison of these techniques is made for fault response time, temperature dependent performance, and their potential applications to help the designer

select an appropriate protection scheme. The experimental results based on a step-down converter indicate that the proposed protection schemes have the capability of clearing a short-circuit fault within 200 ns, irrespective of junction temperature variation of SiC MOSFETs.

7 Conclusion and Future Work

This chapter summarizes this dissertation including its major contributions and provides suggestions for future research.

7.1 Conclusion

This dissertation investigates the development of a high power density integrated phase-leg power module capable of operating under the harsh environment of electric vehicles, while ensuring system reliability and safety under short circuit conditions. The key points of this dissertation are summarized as follows.

(1) A *di/dt* feedback based active gate driver is proposed for switching performance improvement of IGBT power modules. The switching loss, delay time, and Miller plateau duration are reduced by means of auxiliary current source/sink, regardless of power level, gate resistance, as well as IGBT types with some variation of parasitic inductance. Moreover, the proposed active gate drive is suitable to be integrated since no separate power supply, high bandwidth detection and regulation components (e.g. current/voltage sensors, operational amplifier, etc.) are needed.

(2) The design, development, and testing of a high temperature silicon carbide MOSFET power module with an integrated silicon-on-insulator based gate drive are presented. A two-channel high temperature gate driver board is built based on the chip-on-board technique, and experimental results demonstrate the high temperature driving capability of the gate driver up to 200 °C. In addition, a silicon carbide MOSFET phase-leg module is fabricated utilizing high temperature packaging technologies. The junction temperature limitation of the fabricated power module related to thermal runaway phenomenon is investigated. A buck converter prototype incorporating the phage-leg power module and the silicon-on-insulator gate drive is operated successfully at a switching frequency of 100 kHz, with a junction temperature of 232 °C.

(3) The temperature dependent short circuit capability of three different types of commercial SiC MOSFETs is evaluated. It is found that the short circuit withstand time and critical energy of SiC

MOSFETs will be reduced with the increase of current density, case temperature, and DC bus voltage. However, these are nearly independent of device scaling (i.e. die paralleling), fault types (i.e. HSF and FUL), packaging materials, and external cooling conditions. The associated failure mechanism is also analyzed and compared through the developed electro-thermal model and leakage current model. According to the models, the short circuit failure mechanisms of SiC MOSFETs can be thermal generation current induced thermal runaway or high temperature related gate oxide damage.

(4) Based on the short circuit capability evaluation results, the requirements for short circuit protection of SiC MOSFETs are first proposed, considering single-event, repetitive fault conditions, and noise immunity. Three overcurrent / short circuit protection methods are designed and implemented for SiC MOSFETs under both hard switching fault and fault under load condition. The design consideration and associated issues of these methods are analyzed and verified through experiments. A comparison of these techniques is made for fault response time, temperature dependent performance, and their potential applications to help the designer select an appropriate protection scheme.

7.2 Future Work

Some recommended future work is focused on the following aspects:

(1) Advanced IGBT Active Gate Driver

Although the proposed active gate driver is able to reduce the switching loss stage by stage for the selected IGBT, it may not be as effective as the testing results when applied to other IGBTs with much faster switching speed, due to the inherent propagation delay issues. Design optimization of the active gate driver circuits is necessary to achieve a fast response and thus more accurate control. The chip-level integration of these auxiliary circuits will also be helpful to improve their overall performance.

The proposed IGBT active gate driver in this dissertation focuses on the switching performance improvement, especially reduction of switching loss and switching time. During the current rising stage of turn-on and falling stage of turn-off transient, the *di/dt* of the IGBT is still controlled by a conventional gate resistance. The *dv/dt* is always higher than that of using a conventional gate driver. However, this

kind of control strategy may not fit some real application scenarios. For example, under certain operating conditions, electric vehicle drive system may require a controlled *di/dt* to guarantee the IGBTs to operate within their safe operating areas, and a lower *dv/dt* to meet with the vehicle EMI standards. Closed-loop *di/dt* and *dv/dt* control with device health information feedback is desired to be implemented, in addition to switching loss reduction.

(2) High Temperature Integrated Power Module

The high junction temperature operation of the integrated SiC MOSFET power module has been demonstrated, while it cannot be qualified as a full high temperature version without the integration of a high temperature signal isolation chip. A continuous operation of the full high temperature integrated power module needs to be demonstrated under a high ambient temperature environment, such as thermal chamber. In addition, advanced cooling techniques instead of natural air cooling should be used to support high power density and high temperature operation.

In this dissertation, a thermo-sensitive electrical parameter, i.e. turn-off delay time, is proposed for the junction temperature monitoring. This technique is effective and easy for lab demonstration. However, it cannot be used for the online junction temperature measurement. Dedicated detection and control circuits are required to be developed to obtain the junction temperature during high temperature continuous operation.

Another interesting research aspect is the experimental investigation of the thermal runaway issue. Specifically, the thermal runaway temperatures of the fabricated power module should be quantified under different operation conditions (cooling condition, switching frequency, duty cycle, etc.) and compared with other types of SiC MOSFETs and SiC JFETs.

(3) Short Circuit Capability of SiC MOSFETs

According to the electro-thermal model, the higher current density results in a faster temperature rise and larger temperature gradient. The tradeoff between current density and short circuit capability needs to be carefully considered in the device design, especially for the next generation trench gate SiC MOSFETs.

Recently, ROHM Semiconductor demonstrated its third generation SiC MOSFETs based on trench gate structure technology. On one hand, compared to the commercially available planar gate SiC MOSFETs, the trench gate device has even lower on-state resistance and higher current density due to the elimination of JFET region resistance. On the other hand, the device short circuit behavior can be optimized through more homogeneous electric field distribution and specific arrangement of cell size, width, and distance [122]. The short circuit capability of the new device needs to be investigated and compared to the previous devices.

The repetitive short circuit capability and its associated long-term reliability have been studied to some extent for Si devices and SiC JFETs, while there is still no report on the SiC MOSFETs. The temperature dependent repetitive short circuit capability is critical for the wide application of SiC MOSFETs, especially under high temperature environment. Another interesting research aspect is the impact of repetitive short circuit condition on the gate oxide reliability of the SiC MOSFETs.

(4) Short Circuit Protection of SiC MOSFETs

For a conventional solid state circuit breaker, Si IGBTs are widely used with regard to fast, high voltage, and high current switching devices. However, IGBT conduction losses become quite large at high currents and voltages, which is not acceptable in electric vehicle application. The development of SiC MOSFET and SiC JFET based solid state circuit breaker is attractive, allowing low loss, high temperature operation, and simplified cooling requirements. Specifically, normally-on SiC JFET is preferable since solid state circuit breaker basically operates in pure conduction mode. The multi-chip SiC power module with integrated cooling system and gate drive are the core technologies to achieve a high power density and high temperature solid state circuit breaker.

Compared to solid state circuit breaker, desaturation and fault current evaluation techniques are relatively easy to be chip-level integrated. The integration will likely supposed to further improve the fault response time by reducing circuit parastics. The high temperature version of these techniques needs to be developed as well for harsh environment application.

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