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A Low-Power BFSK/OOK Transmitter for Wireless Sensors

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A Low-Power BFSK/OOK Transmitter for Wireless Sensors

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Degree

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Mohammed Shahriar Jahan

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Dedication

This dissertation is dedicated to the free-thinkers and
the freedom-fighters of the world.

Acknowledgement

It has been a little more than five years since I started my studies in UT and there are so many people I should thank for helping me to get to where I am now. First of all, I would like to express my gratitude to my advisor, Dr. Jeremy Holleman, who offered me the opportunity to work with him and grow as a researcher in IC design. I thank him for all the guidance and encouragement throughout all these years of my Ph.D. program. I am also grateful to Dr. Syed Islam, Dr. Benjamin J. Blalock and Dr. Christopher Cherry for serving as my Ph.D. committee members. Their valuable suggestions helped me improve my work and dissertation.

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thank my elder brother, who is an engineer himself, for sparking my interest in math and science by showing me all those cool math tricks in my childhood.

Abstract

In recent years, significant improvements in semiconductor technology have allowed consistent development of wireless chipsets in terms of functionality and form factor. This has opened up a broad range of applications for implantable wireless sensors and telemetry devices in multiple categories, such as military, industrial, and medical uses. The nature of these applications often requires the wireless sensors to be low-weight and energy-efficient to achieve long battery life. Among the various functions of these sensors, the communication block, used to transmit the gathered data, is typically the most power-hungry block. In typical wireless sensor networks, transmission range is below 10 meters and required radiated power is below 1 milliwatt. In such cases, power consumption of the frequency-synthesis circuits prior to the power amplifier of the transmitter becomes significant. Reducing this power consumption is currently the focus of various research endeavors. A popular method of achieving this goal is using a direct-modulation transmitter where the generated carrier is directly modulated with baseband data using simple modulation schemes.

Among the different variations of direct-modulation transmitters, transmitters using unlocked digitally-controlled oscillators and transmitters with injection or resonator-locked oscillators are widely investigated because of their simple structure. These transmitters can achieve low-power and stable operation either with the help of recalibration or by sacrificing tuning capability. In contrast, phase-locked-loop-based (PLL) transmitters are less researched. The PLL uses a feedback loop to lock the carrier to a reference frequency with a programmable ratio and thus achieves good frequency stability and convenient tunability.

This work focuses on PLL-based transmitters. The initial goal of this work is to reduce the power consumption of the oscillator and frequency divider, the two most power-consuming blocks in a PLL. Novel topologies for these two blocks are proposed which achieve ultra-low-power operation. Along with measured performance, mathematical analysis to derive rule-of-thumb design approaches are presented. Finally, the full transmitter is implemented using these blocks in a 130 nanometer CMOS process and is successfully tested for low-power operation.

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Chapter 1 Introduction

1.1 Motivation

The semiconductor industry has progressed significantly in recent years and allowed consistent improvement of wireless chipsets in terms of functionality, cost, form factor and power consumption. This has enabled a broad range of new short-range, low-power applications, such as wireless sensors. Applications for these sensors include military use, such as target tracking, equipment monitoring in industrial sectors, and medical use, such as patient monitoring. These sensors are typically remotely deployed to gather data and relay them to the end-user or base station and rely on small batteries or harvested energy for power supply. Often because of their locations, battery replacement is not desirable or even feasible. Wireless devices are also used in animal tracking systems such as small bird flight recorders that require payloads less than one gram [1]. High power consumption in these devices is problematic because it will reduce battery life or increase system weight, which is dominated by battery weight. As such, energy efficiency is one of the most important factors in the design of these sensors so that sensor lifetimes in the order of months to years can be ensured without any maintenance.

Among all the functions of wireless sensors, communication usually requires most of the power and so, it is important to have an energy-efficient transmitter. In typical wireless sensor networks, transmission range is below 10 m and required radiated power is less than 1 mW [2]. For example, MICS (Medical Implant Communication Service, 402–405 MHz) band compatible devices must transmit no greater than 25 μW of power [3]. At such low radiated power, the power consumption of the transmitter is no longer dominated by the power amplifier. The power consumed by the circuits prior to the power amplifier (PA) becomes significant and degrades the

transmitter efficiency substantially. Transmitter efficiency is defined as the ratio of transmitted power to the power consumed by the transmitter. For example, in the MICS compatible transceiver reported in [4], a 400 µW direct-modulation FSK transmitter uses a digitally controlled LC oscillator as a pre-PA frequency synthesizer which consumes 210 µW power, resulting in an efficiency of only 6.25% at -16 dBm output power. Another 2.4 GHz CMOS transceiver reported in [5] uses a direct-conversion transmitter where a fractional-N phase-locked loop (PLL) consumes 9.72 mW out of the total 23.58 mW power consumption of the whole transmitter at 0 dBm transmitted power. This results in only 4.2% transmitter efficiency. Thus, at low transmitted power, a very low pre-PA power is essential as well as high PA efficiency for an efficient ultra-low-power transmitter.

The frequency synthesizer is one of the key pre-PA building blocks in any transmitter architecture. As this generates RF (radio frequency) carrier signals, this is usually one of the most power-hungry pre-PA blocks. For example, the phase-locked-loop-based frequency synthesizer used in the 2.4 GHz transmitter reported in [6] is the largest power consuming block in the system, as shown in Fig. 1.1.

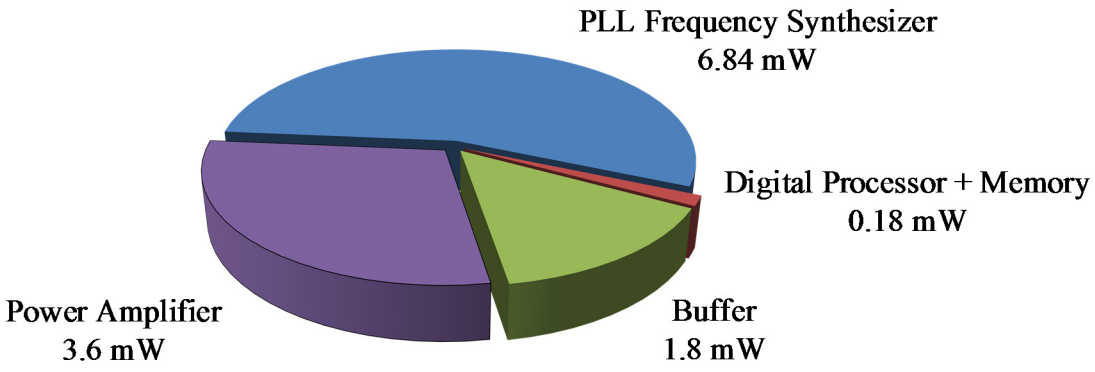


Fig. 1.1. Power distribution in the 2.4 GHz PLL-based transmitter reported in [6].

Both direct-modulation and direct-conversion type transmitters need a local frequency synthesizer. Fig. 1.2 shows the typical structures of direct-conversion and direct-modulation transmitters. A direct-conversion transmitter uses an up-conversion mixer circuit to generate a modulated carrier signal from the synthesizer and baseband data signal. While this architecture is well-suited for multi-standard operation and supports complex modulation schemes, they are usually not energy-efficient due to power-hungry mixer circuits [5] [7] [8]. Direct-modulation transmitter, on the other hand, is a more favored architecture for low-power transmitters because here baseband data directly modulates the carrier generated from the local frequency synthesizer. Thus, it eliminates the need for mixers and complex DAC circuits. As data-rate requirements of wireless sensor networks are usually low, spectral efficiency is traded off for power efficiency so that simple modulation schemes, such as on-off keying (OOK) or frequency-shift keying (FSK),

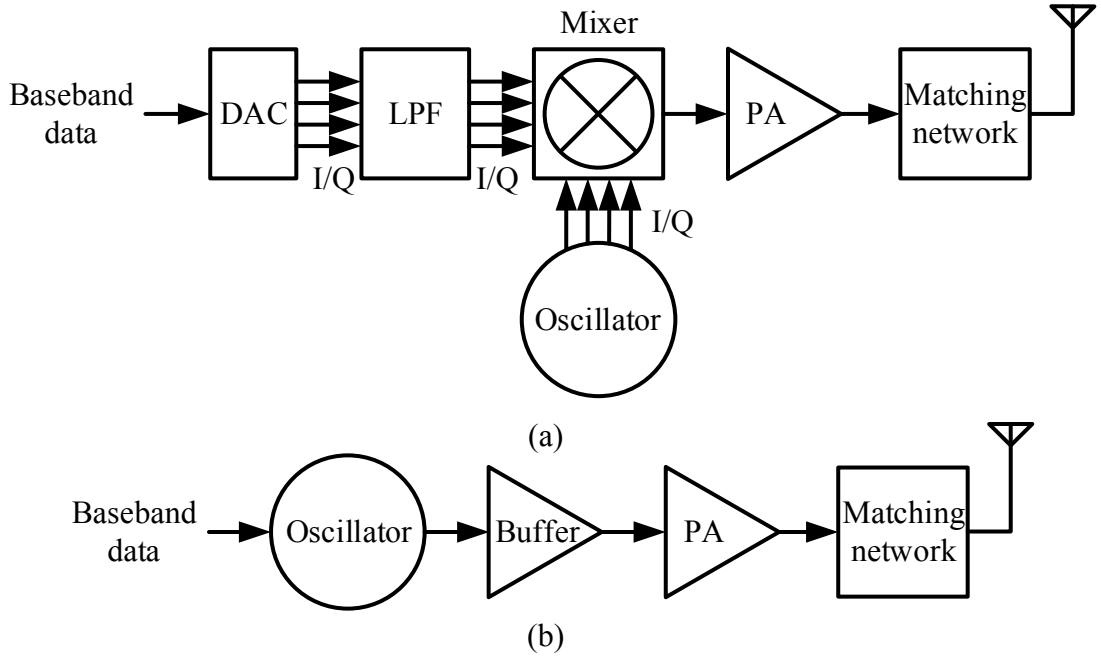


Fig. 1.2. Typical (a) direct-conversion and (b) direct-modulation transmitter structures.

can be used. Direct-modulation transmitters, such as [9] and [10], use unlocked oscillators, discarding any extra circuitry used to stabilize the frequency. This topology normally can achieve high data-rate and consumes relatively lower pre-PA power than other topologies. However, since there is no feedback loop for frequency stability, unlocked oscillators consume high amount of power to achieve improved close-in phase noise performance. In practice, this open-loop topology requires periodic relocking or calibration of the oscillator frequency to counter frequency drift due to voltage and temperature variations, thus making continuous operation difficult [6]. Recently, a new direct-modulation topology is reported in [11]. Here a low frequency local oscillator is used, injection-locked to a crystal oscillator of same frequency to improve signal quality and then a frequency-multiplying power amplifier is used to up-convert the frequency. The transmitter consumes only 90 μW power while operating at MICS band, which makes it very suitable for ultra-low-power wireless sensors, but the topology offers little or no on-chip frequency-tuning, thus no channel selection and its operation at MICS band or 433 MHz ISM (Industrial, Scientific and Medical) band is dependent on the external crystal used. Other direct-modulation transmitters based on injection-locked oscillators or MEMS resonators, such as [12], are also reported. Although these transmitters achieve good signal quality at considerably low power, they have the same problem of limited or no on-chip frequency selection as the frequency is directly locked to external reference frequency or determined by the external resonator.

PLLs are also widely used for radio frequency synthesis. PLL-based frequency synthesis usually offers improved communication quality by locking the VCO frequency to a clean reference frequency, derived from a low-frequency crystal oscillator. They also offer superior flexibility of frequency selection as they can be varied by programming the feedback loop. Of the many known PLL architectures [13] [14], the most widely used is the classical PLL architecture [6] [15] [16],

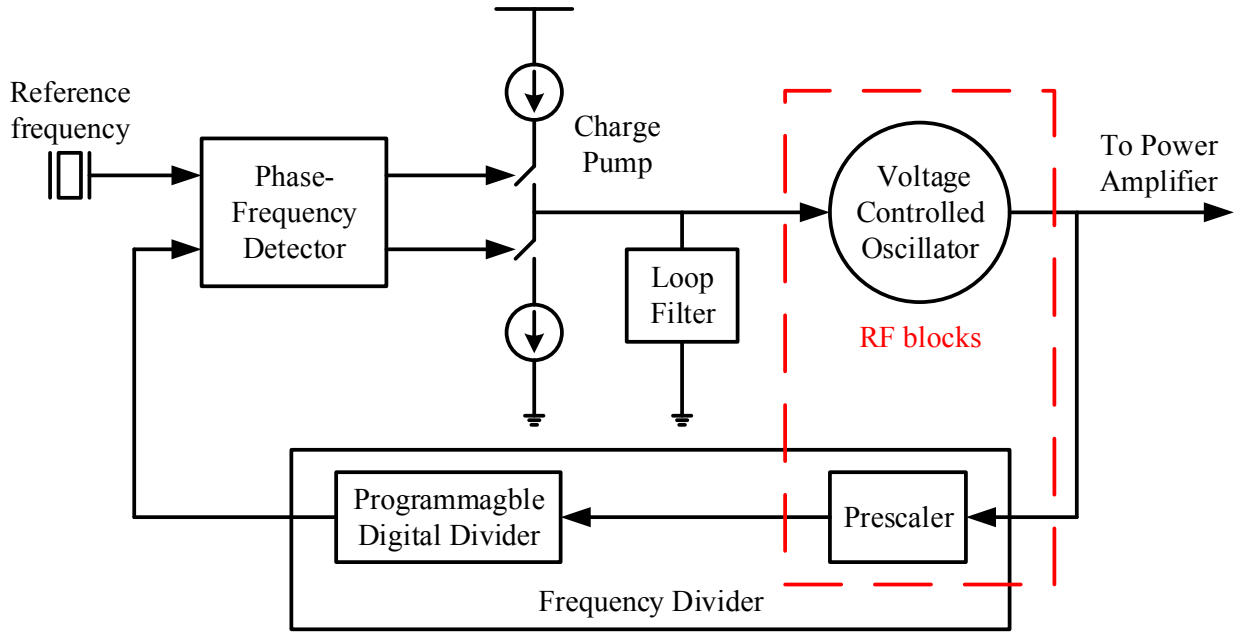


Fig. 1.3. The structure of a typical PLL.

which is simple in structure. Fig. 1.3 shows the structure of this type of PLL which consists of the following blocks: a phase-frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage-controlled oscillator (VCO) and a divide-by-N frequency divider (FD). The PFD block determines the phase error between the reference frequency and VCO frequency divided down by FD and CP-LF combination translates this error to an analog voltage signal to tune the VCO frequency so the phase error is removed. This feedback acts as high-pass filter for the VCO phase noise, suppressing close-in phase noise and thus improves VCO signal quality. The FD block has a low-power analog frequency divider or prescaler at the front-end, which is followed by a programmable digital divider. The division ratio of the FD can be programmed and thus the frequency synthesizer can be tuned to different channels. The tuning resolution depends on the reference frequency and prescaler ratio.

As the VCO and the prescaler blocks operate in full radio frequency in a PLL, these two are the most power-hungry blocks in any PLL [17] and together can consume about 80% of the total power in a PLL, as shown in Fig. 1.4. This is the disadvantage of a PLL-based transmitter compared to the other direct-modulation transmitters mentioned above, as they only use the oscillator and discard the rest of the PLL to reduce power consumption. As a result, much less investigation is done on PLL-based transmitters with μW-range power consumption. Instead, research in this area is recently more focused on unlocked or injection-locked direct-modulation transmitters, sacrificing either the tuning flexibility or the improved noise tolerance and frequency stability of PLL-based architecture. A brief overview of the state-of-the-art is shown in Table 1.1.

1.2 Research Goal

The goal of this research is to explore the prospect of PLL-based architecture for ultra-low-power transmitters, which can be used for implantable wireless sensors where power consumption is constrained in order to reduce maintenance and battery-bulk weight. High power efficiency can be achieved by minimizing the power consumption of the VCO and the prescaler blocks in a PLL.

In this work, an ultra-low-power PLL-based transmitter is proposed. The classical structure for a 3rd order PLL is used for simplicity. The PLL's power consumption is minimized by developing new topologies of the VCO and the prescaler, thus reducing the pre-PA power consumption of the transmitter. The transmitter operates in the 902 – 928 MHz (915 MHz) ISM band. Binary frequency-shift keying (BFSK) and on-off keying (OOK) modulation schemes are adopted where the baseband data directly modulates the carrier generated by the PLL.

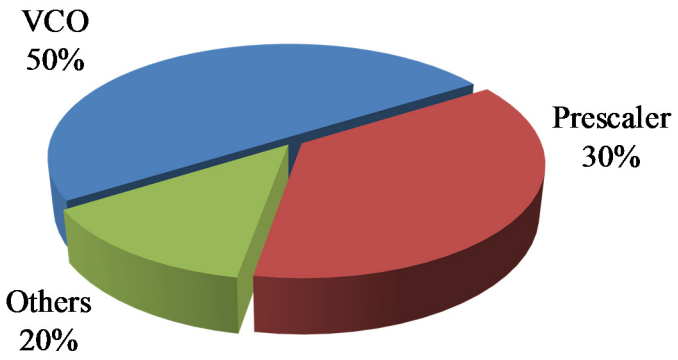


Fig. 1.4. Power budget of the blocks in a PLL [17].

Table 1.1. Brief overview of power consumption and efficiency of state-of-the-art transmitter architectures.

	Topology	CMOS Tech. (nm)	Freq.	Modulation, Data-rate	Pre-PA power	PA power	Output power (dBm)	Efficiency
[8]	Direct-conversion	180	2.4 GHz	IEEE 802.15.4	8.88 mW		-1.72	7.6%
[18]	Direct-modulation	90	915 MHz	2-tone BPSK	300 µW	2.35 mW	0	37.7%
[4]	Direct-modulation	180	400 MHz	BFSK, 250 kbps	210 µW	189 µW	-16	6.3%
[11]	Direct-modulation *	130	400 MHz	BFSK, 200 kbps	90 µW		-17	22.2%
[6]	PLL-based	180	2.4 GHz	BFSK, 200 kbps	8.82 mW	3.6 mW	0	8%

* Cascaded multi-phase injection-locking and frequency multiplication.

1.3 Dissertation Overview

The remaining chapters of this proposal will cover the different steps of design of the 3rd-order PLL-based FSK/OOK transmitter. Chapters 2 and 3 describe the design and analysis of the VCO and the prescaler topologies developed in the work, respectively. Chapter 4 introduces the proposed PLL using these two blocks along with necessary design considerations. In Chapter 5, a power amplifier suitable for this low-power transmitter is discussed. The full transmitter is fabricated and its measured performances are presented and compared to the state-of-the-art in Chapter 6. Chapter 7 concludes this dissertation and proposes potential future works.

Chapter 2 Low-Power Voltage-Controlled Oscillator

The VCO is one of the key components in a frequency synthesizer as it most critically determines the performance of the synthesizer. Recently, increasing demand for lower cost and higher integration has led to continuous study and research to enhance CMOS integrated VCO performance. As stated earlier, the VCO is the most power-hungry block in a PLL frequency synthesizer. As the demand for low-power operation increases, it poses an increasing challenge for the VCO's noise performance, particularly phase noise and supply noise tolerance. As the spectral purity of the synthesized signal heavily depends on the quality of the VCO signal, substantial research has been conducted on the two types of VCO topologies – LC resonance oscillator and Ring oscillator, to improve their noise performance.

2.1 LC Oscillator

Fig. 2.1 shows the typical structure of an LC oscillator. R_P is the equivalent parallel tank resistance, which includes the series resistance of L and C and represents the loss or finite quality factor, Q of the tank. Oscillation occurs when the positive feedback loops meets the Barkhausen criteria for oscillation (unity gain with an integer multiple of 360° phase shift around the loop) at the resonance frequency of the LC tank, $f_{osc} = \frac{1}{2\pi\sqrt{LC}}$.

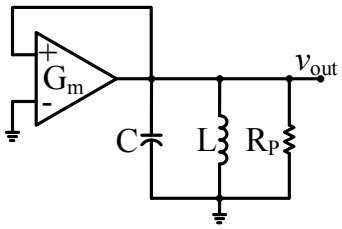


Fig. 2.1. Typical structure of an LC oscillator.

To meet the gain requirement, an active G_m-cell is used which injects charge that is dissipated by R_P in each cycle. The G_m-cell has the voltage-to-current gain, g_m, such that at equilibrium, $g_m R_P = 1$. For oscillation startup, g_m should be greater than $\frac{1}{R_P}$. This sets the lower limit of power consumption of the LC oscillator and is determined by R_P, and thus, tank Q.

Fig. 2.2 shows typical structures of the three conventional LC oscillators. The Colpitts oscillator uses common-gate topology because of 0° drain-to-source phase shift. Thus, it achieves 0° phase shift around the loop for oscillation at the resonance frequency, $f_{osc} = \frac{1}{2\pi}\sqrt{\frac{1}{L\left(\frac{C_1 C_2}{C_1+C_2}\right)}}$. For oscillation startup, the following requirement should be met.

$$g_{m1} R_P \geq \frac{C_1}{C_2} + \frac{C_2}{C_1} + 2 \tag{1}$$

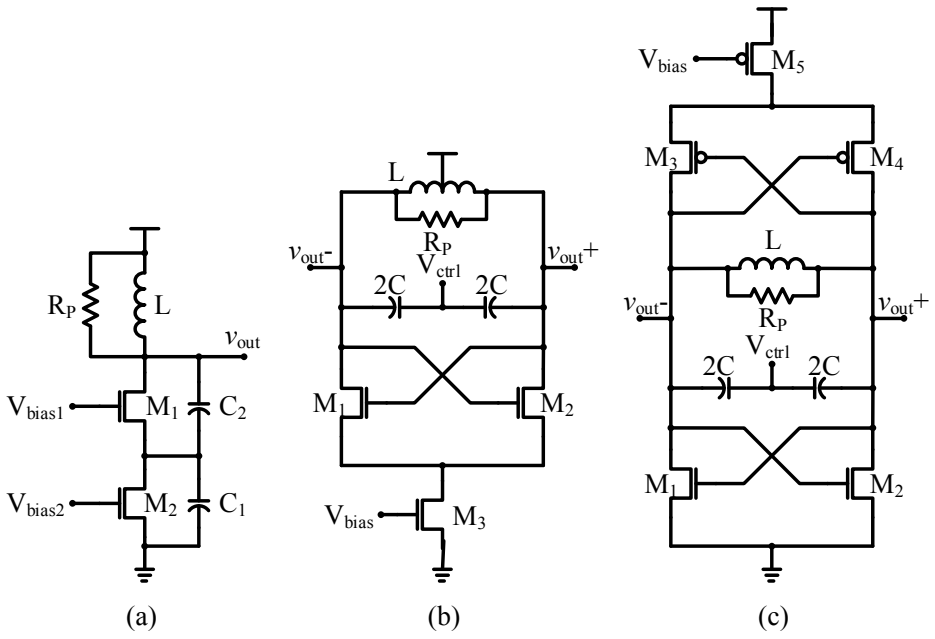


Fig. 2.2. Typical structures of (a) common-gate Colpitts oscillator, (b) cross-coupled oscillator and (c) complementary cross-coupled oscillator.

From (1), the minimum required value of g_m of M_1 will be when $C_1 = C_2$ and in this case $g_{m1} \geq 4/R_P$.

The cross-coupled has a pair of cross-coupled NMOSs and an LC tank to contain the latch-up (0° phase shift) only at the resonant frequency, $f_{osc} = \frac{1}{2\pi\sqrt{LC}}$. The startup condition of this oscillator is $g_m \geq 2/R_P$. By using varactors instead of the capacitors and varying V_{ctrl}, the oscillation frequency can be varied.

The complementary cross-coupled oscillator uses a pair of cross-coupled inverters instead of a cross-coupled NMOS pair to relax the startup requirement, such that $\left(g_{mn} + g_{mp}\right) \geq 2/R_P$.

2.2 Ring Oscillator

A ring oscillator consists of several active gain stages or delay cells in a loop. The structures of two basic ring oscillator topologies are shown in Fig. 2.3. Single-ended structures need an odd

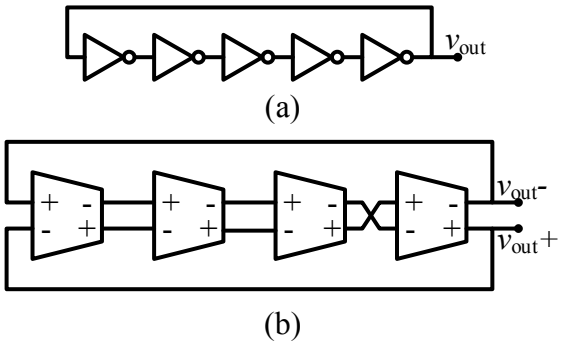


Fig. 2.3. Typical structures of (a) five-stage single-ended ring oscillator and (b) four-stage differential ring oscillator.

number of stages whereas differential ring oscillators can operate with both even and odd number of stages.

A single-ended oscillator can consist of an odd number of CMOS inverters. This results in a net 180° phase shift around the loop due to inversions which prevents the loop from a latch-up at DC. As Barkhausen criteria dictates, the output poles of the stages must provide another 180° phase shift for oscillation to occur. For example, in a 3-stage ring oscillator, each stage can be described as $-\frac{A}{1+\frac{s}{\omega_{3dB}}}$, where A is the low-frequency gain and $\omega_{3\text{dB}}$ is the 3dB bandwidth. Thus, the loop transfer function would be

$$H(s) = -\frac{A^3}{\left(1+ s/\omega_{3dB}\right)^3}. \tag{2}$$

The circuit will only oscillate at a frequency f_{osc} if each stage provides 60° frequency-dependent phase shift, totaling to 180°. Thus, $\tan^{-1}\left(\frac{\omega_{osc}}{\omega_{3dB}}\right) = 60°$. Hence,

$$\omega_{osc} = \sqrt{3}\omega_{3dB} \tag{3}$$

Barkhausen criteria dictates that the magnitude of the loop gain should be unity. Therefore, from (2) we get,

$$\frac{A^3}{\left(\sqrt{1+\left(\omega_{osc}/\omega_{3dB}\right)^2}\right)^3} = 1. \tag{4}$$

Combining (3) and (4), we get $A = 2$ which means a 3-stage ring oscillator would require a DC gain greater than 2 per stage for oscillation startup.

Another expression for a ring oscillator's oscillation frequency is $f_{osc} = 2Nt_d$, where N is the number of stages and t_d is the propagation delay of each stage.

2.3 LC Oscillator vs. Ring Oscillator

2.3.1 Frequency Stability

An ideal oscillator would have an output expressed as $A\cos(\omega_o t + \varphi)$ with fixed amplitude A, frequency ω_o and a fixed phased reference ϕ. However, due to various device noise sources in the circuit, the output would have amplitude and phase fluctuations and more generally expressed as $A(t).f\left[\omega_o t + \varphi(t)\right]$, where the amplitude and phase are now functions of time and f is a periodic function with period 2π. The spectrum of this signal has sidebands close to oscillation frequency ω_o instead of being just two impulses at $\pm \omega_o$.

These short-term instabilities of the signal are usually characterized in terms of the single-sideband noise spectral density [19]. The unit is decibels below the carrier per hertz (dBc/Hz) and is defined as

$$L_{total}\{\Delta\omega\} = 10\log\left[\frac{P_{sideband}(\omega_o + \Delta\omega, 1\,Hz)}{P_{carrier}}\right]$$

Here $P_{sideband}(\omega_o + \Delta\omega, 1\,Hz)$ represents the single sideband power at $\Delta\omega$ frequency offset from carrier frequency ω_o with 1 Hz measurement bandwidth. This includes both fluctuations, *A(t)* and $\phi(t)$. Usually, the amplitude fluctuation is reduced by some amplitude limiting mechanism in the oscillator circuit and $L_{total}\{\Delta\omega\}$ is dominated by its phase portion, which is known as phase noise, denoted by $L\{\Delta\omega\}$.

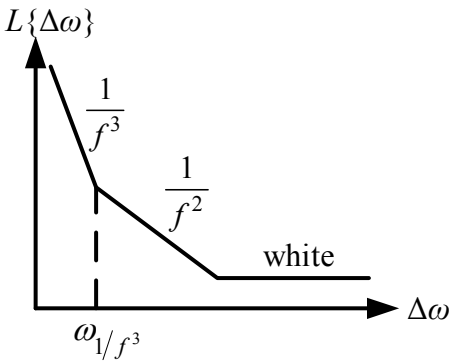


Fig. 2.4. Typical plot of the phase noise of an oscillator versus frequency offset from carrier.

Fig. 2.4 shows the typical phase noise plot of a free-running oscillator. The corner frequency, ω_{1/f^3}, between $1/f^3$ and $1/f^2$ regions of the plot is derived from device flicker noise corner. If the VCO is integrated into a PLL, the PLL will act as a high-pass filter for the VCO phase noise and suppress most of the close-in phase noise, given enough bandwidth. Beyond PLL's bandwidth, VCO's phase noise will not be suppressed and the VCO needs to be noise-immune and with low intrinsic noise to achieve good performance.

For an LC oscillator, phase noise in the $1/f^2$ region of the spectrum can be expressed as [19] [20], based on Leeson's equation,

$$L\{\Delta\omega\} = 10\log\left[\frac{FkT}{Q^2}\cdot\frac{R_P}{V_P^2}\cdot\left(\frac{f_o}{\Delta f}\right)^2\right]. \tag{5}$$

Here F is device excess noise number, an empirical parameter, k is Boltzmann's constant, T is the absolute temperature, V_P is the voltage swing and Q is the effective quality factor of the tank with all loads accounted for. From (5), it is seen that phase noise is dependent on the Q of the circuit and the voltage swing and improves if these two increases.

In an oscillator with large Q, the required instantaneous change in frequency to compensate any phase shift due to various noise sources is smaller. This results in better frequency stability. For a fully integrated LC VCO, the low-Q on-chip inductor often dominates the tank Q. LC VCOs using high-Q, off-chip inductors [18] [21] or bondwire inductors [22] are reported. In a ring oscillator, however, Q (defined as ratio of energy stored to energy dissipated in each cycle or 2π radian) is very low and thus, it is prone to higher phase noise.

Phase noise in the $1/f^2$ region [19] is also described by the following equation.

$$L\{\Delta\omega\} = 10\log\left[\frac{\Gamma_{rms}^2}{q_{\max}^2}\cdot\frac{\overline{i_n^2}/\Delta f}{4\cdot(\Delta\omega)^2}\right] \tag{6}$$

Here $q_{\max}$ is the maximum charge displacement across the capacitor on the node under consideration. $\Gamma(\omega t)$ is the known as the impulse sensitivity function (ISF), which is shown in Fig. 2.5 for generic structures of LC and ring oscillators. This is a dimensionless, frequency and

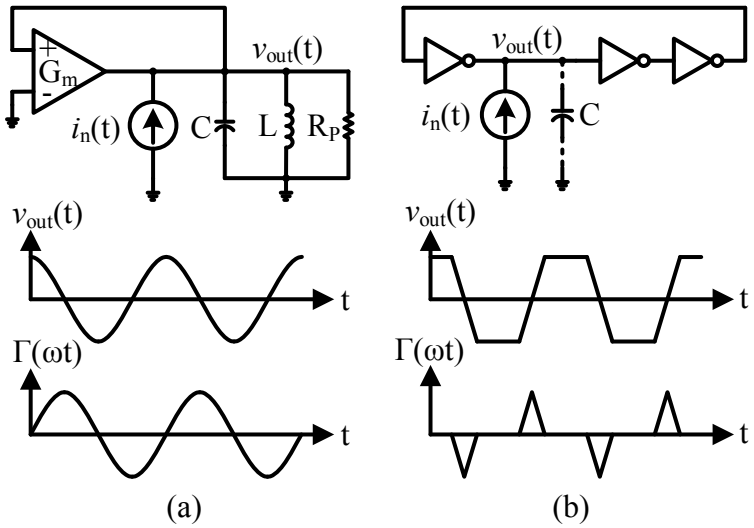


Fig. 2.5. Typical structures with noise-current injection source, $i_n(t)$, shown at a node, waveforms and impulse sensitivity functions of (a) an LC oscillator and (b) a ring oscillator [19].

amplitude-independent periodic function with period 2π which describes how much phase shift results from a unit current impulse at a given time t. $\overline{i_n^2}/\Delta f$ represents noise current power injected from various noise sources at the node under consideration. It can be understood from the ISF curves shown in Fig. 2.5 that an oscillator's phase is most sensitive to noise near the transition of its waveform and least at the peaks.

LC oscillators generally have better phase noise performance than ring oscillators at the same power consumptions [23]. From (6), this can be understood more clearly. In a ring oscillator, device noise current is maximum during the transition (both PMOS and NMOS being "on" in transition) where the sensitivity, and hence ISF, is also the largest [19]. Also, a ring oscillator stores a certain amount of energy in the load capacitors every cycle and dissipates all of it in the same cycle. On the other hand, an LC resonator dissipates only $2\pi/Q$ of the total energy in one cycle. Thus, for a given power consumption, q_{max} is much smaller for a ring oscillator than an LC oscillator. In other words, a ring oscillator would consume much larger power than an LC oscillator to achieve same phase noise performance. For example, the ring oscillator in [24], while operating at 685 MHz frequency, achieves -110.8 dBc/Hz phase noise at 1 MHz offset with 10 mW power consumption. On the opposite side, the LC oscillator in [25], while operating at 915 MHz frequency, shows -126 dBc/Hz phase noise at 1 MHz offset with 1.06 mW power consumption.

Power-supply noise is another large source of VCO noise. Because of higher Q, LC oscillators are usually much less sensitive than ring oscillators. LC oscillators are also more immune to CMOS PVT (process, voltage and temperature) variations than ring oscillators. The oscillation frequency of an LC oscillator is dominated by the LC tank resonance. On the other

hand, in the ring oscillator, as shown before, oscillation frequency is determined by individual delay-cell bandwidth which varies with PVT variations.

2.3.2 Power Consumption, Chip Area and Tuning Range

Despite superior frequency stability, LC oscillators have their own drawbacks. The on-chip inductors consume large area. Minimization of power consumption necessitates a large inductor, leading to large R_P ($\approx 2\pi f_{osc} LQ$). This is in conflict with large tuning range, as for a given frequency, a large inductor limits the size of the variable tank capacitance. Also, low-phase-noise design of LC oscillators has the following challenges [20]:

1) Switched capacitor arrays are widely used to achieve wide tuning range. Wide (low-resistance) MOS switches, needed for low phase noise, add parasitic capacitances in series with the switched capacitors, limiting the tuning range.
2) With CMOS scaling, supply voltage is also reduced, resulting in reduced maximum voltage swing across the LC tank. Usually, phase noise is improved by scaling down the inductor to reduce R_P. This also increases power consumption. Here, wide tuning range necessitates large capacitor arrays where interconnections introduce significant low-Q inductance, making it difficult to achieve low phase noise.
3) Minimization of power consumption necessitates a large inductor, leading to large R_P ($\approx 2\pi f_{osc} LQ$). This is in contrast with large tuning range performance, as for a given frequency, a large inductor limits the size of the variable tank capacitance [25]. Also, since R_P scales down with frequency, a wide-tuning-range oscillator must be provided enough start-up power at the low end of the tuning range and will exhibit a bias current excess as the frequency increases.

Ring oscillators, since they do not require any inductor, occupy very small die area and thus, are highly integrable. They also can achieve wide tuning range using simple mechanisms to tune delay-cell bandwidth. This is very useful to counter PVT variations. With several high-gain stages in the loop, ring oscillators easily meet the Barkhausen criteria at very low power consumption, whereas LC oscillators are hard-limited in lowering startup power. For example, the self-calibrated ring oscillator in [26] operates at 1.38 GHz frequency with only 46 μW power consumption.

2.4 Phase Noise – Power Tradeoff for Low-data-rate Communication Systems

As discussed in the previous section, ring oscillators require much less startup power than LC oscillators, but they have poorer phase noise performance and PVT-variation. Therefore, substantial research has been conducted on improving frequency stability of ring oscillators [26] [27] [28] [29] [30] at the cost of higher power consumption or added complex circuitry.

However, it can be shown that simple modulation systems require only modest frequency stability and low-data-rate digital modulation systems are able to tolerate higher phase noise than that in most of the recently published VCOs. Fig. 2.6 shows bit error rates (BER) for different oscillator phase noise levels and data-rates for a 2-FSK modulated system with 500 kHz frequency shift. This plot is obtained using the MATLAB communication toolbox. It shows that a 200 kbps 2-FSK system yields a BER of only 5.5 ppm with carrier phase noise as high as -80 dBc/Hz at 1 MHz offset. BER increases with data rate. This shows that for simple low-data-rate systems, phase noise of the VCO can be compromised as a trade-off for low power consumption.

Fig. 2.7 shows simulated phase noise at 1 MHz offset of 1 GHz signals generated by simplified structures of a single-ended Colpitts oscillator and a single-ended, 5-stage ring oscillator.

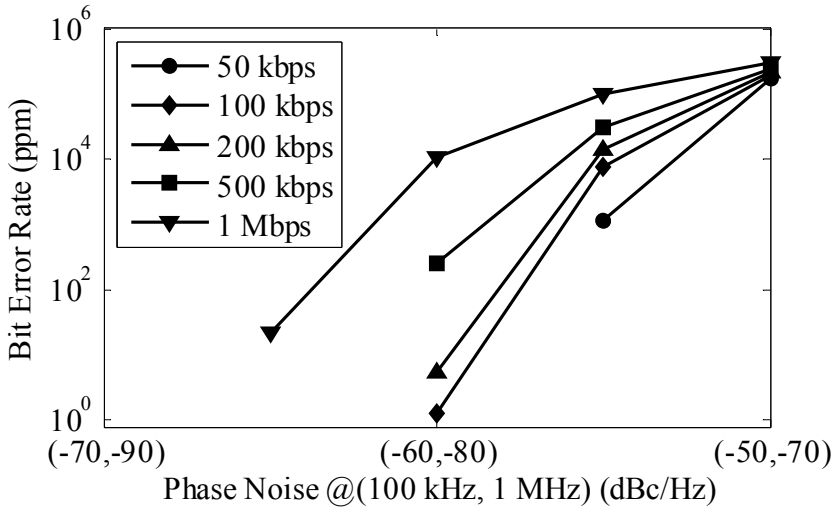


Fig. 2.6. Bit error rate (BER) of 2-FSK system with 500 kHz frequency shift for different data rates and carrier phase noise levels.

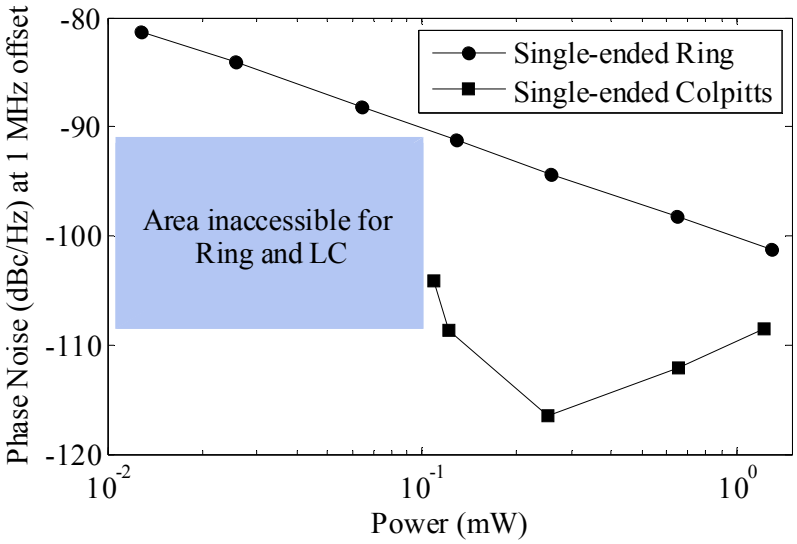


Fig. 2.7. Simulated phase noise of 1 GHz signals, at 1 MHz offset from generalized structures of a single-ended, 5-stage ring oscillator and a single-ended Colpitts oscillator for different core power consumptions from 1.2 V supply.

It is to be noted that the simulations are performed in pre-layout and therefore, the degradation of phase noise by parasitic elements is not accounted for. It is clear that there is an intermediate area between LC and ring oscillators where moderate phase noise can be considered as a tradeoff for low-power operation.

2.5 Gain-Boosted LC Oscillator

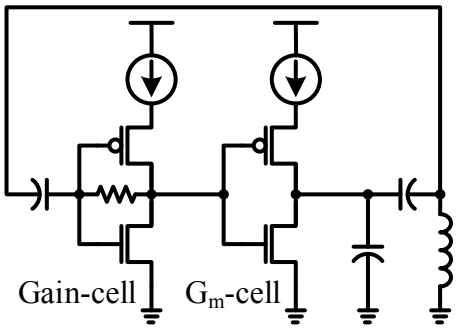


Fig. 2.8. Simplified structure of the developed GB-LC VCO topology.

A possible solution for designing low-power high-quality VCOs is to design an LC oscillator with boosted g_m so that reduced startup power can be achieved while still retaining LC's frequency stability to some extent. Efforts on such g_m-boosting have been reported in literature. For example in [31], a conventional Colpitts oscillator is converted into a differential structure and g_m is boosted by the passive gain from capacitive dividers in the tank. However, the boosting factor is limited by its dependence on the tank capacitor ratio which also affects the startup criteria in a Colpitts oscillator.

In this work, a novel single-ended LC VCO topology is developed that fills the previously mentioned gap between high-power LC oscillator and high-noise ring oscillator. Fig. 2.8 shows a

simplified structure of this gain-boosted LC (GB-LC) VCO. This VCO is a combination of a conventional common-source LC oscillator and an active gain cell from single-ended ring oscillators. This hybrid structure offers frequency stability superior to a ring oscillator, while the gain cell introduced provides high active gain to boost the g_m greatly. In this way, Barkhausen criteria can be met with much lower startup power, although this approach degrades noise performance to some extent, compared to conventional LC VCOs.

Fig. 2.9 shows a comparison between simulated phase noises of 1 GHz signals, at 1 MHz offset, generated by simplified structures of a single-ended Colpitts oscillator, a single-ended current-starved ring oscillator and the proposed GB-LC oscillator for different power consumptions from 1.2 V supply. The GB-LC oscillator, with its moderate phase noise and low startup criteria, sits between the high-noise, low-power ring oscillator and low-noise LC oscillator whose power consumption reduction is limited by startup criteria. Fig. 2.10 shows simulated supply sensitivity of a single-ended, 5-stage ring oscillator and a GB-LC oscillator of the same structure in Fig. 2.9. Again, the GB-LC structure shows much better supply sensitivity than ring oscillators. These simulations do not count the effect of parasitics, which the ring oscillator is much more sensitive to. On the other hand, the GB-LC oscillator has the inherent stability of the LC oscillators, but it is somewhat degraded due to the phase delay of the gain-cell. Moreover, if an SNR degradation of 10 dB in the transmission path is assumed, considering Fig. 2.6, a 50 μW GB-LC would still have BER below 1 ppm at 1 Mbps data-rate. In the same case, a 60 μW ring oscillator would yield a BER of 10000 ppm.

Detailed description, analysis and measured performances of the GB-LC developed in this work are discussed in the following sub-sections.

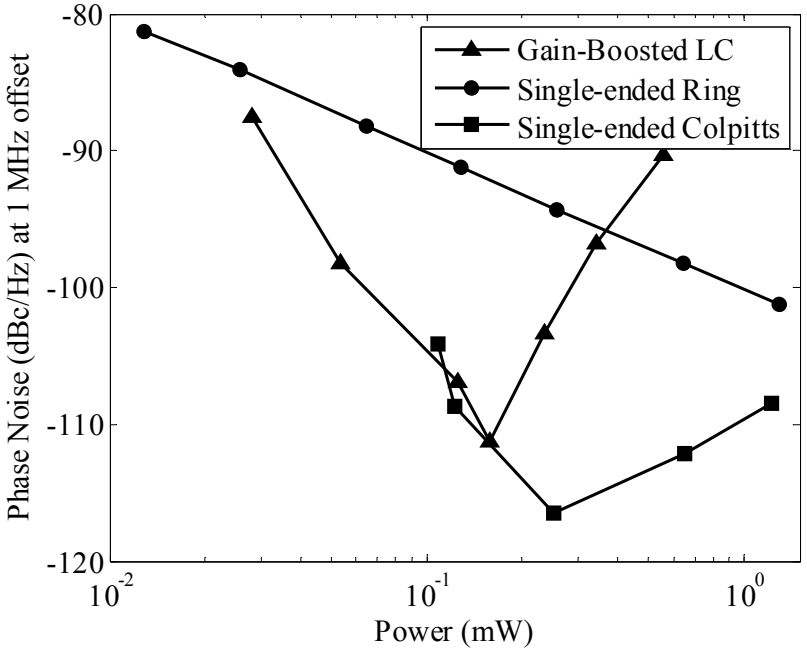


Fig. 2.9. Simulated phase noise of 1 GHz signals, at 1 MHz offset from generalized structures of a single-ended, 5-stage ring oscillator, a single-ended Colpitts oscillator and a GB-LC oscillator for different core power consumptions from 1.2 V supply.

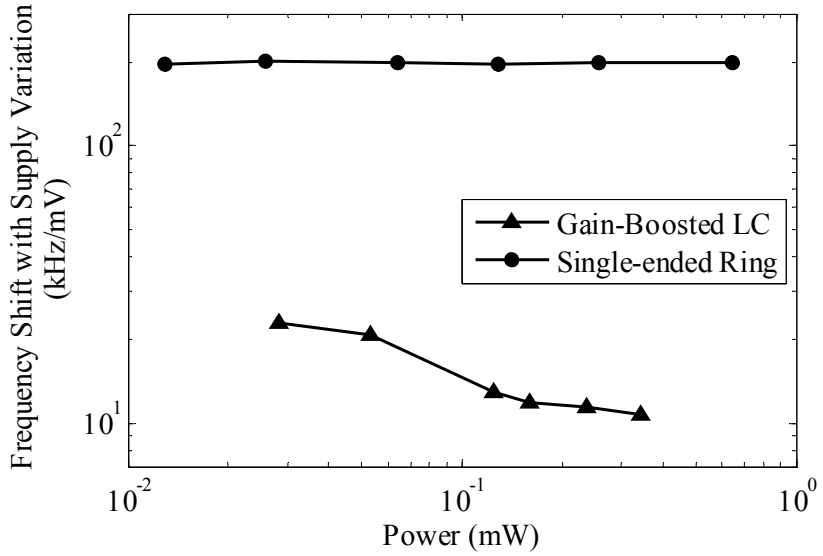


Fig. 2.10. Simulated supply sensitivity of generalized structures of a single-ended, 5-stage ring oscillator and a GB-LC oscillator, running at 1 GHz, using a 1.2 V supply.

2.5.1 Architecture and Operation

2.5.1.1 Core Structure

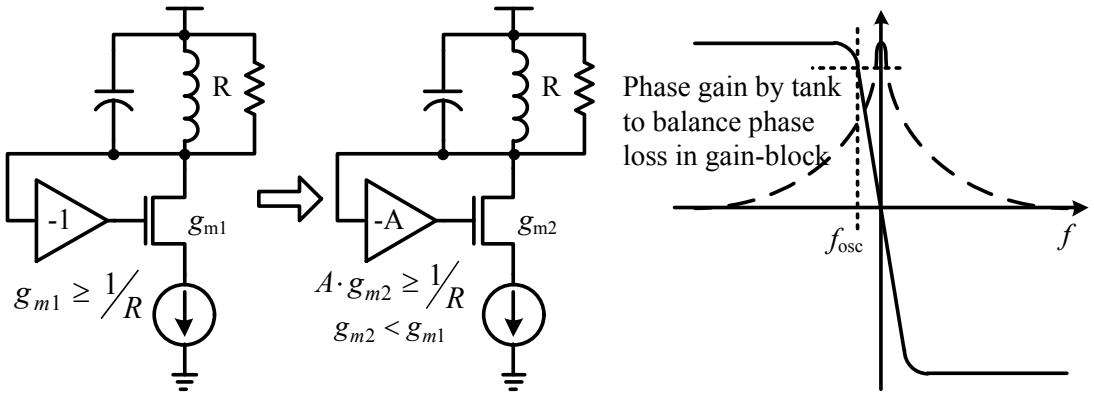


Fig. 2.11. (a) Derivation of core structure of the proposed VCO and (b) frequency of oscillation.

The derivation of the core structure of the proposed GB-LC VCO is shown in Fig. 2.11. The gain cell is introduced in the loop to boost a smaller g_m which can be achieved with lower startup power. Also, the gain cell, driving only the gate capacitance of the g_m device, can achieve the desired boosting gain with much lower power consumption. Thus reduction of total power consumption, compared to conventional LC oscillator, can be achieved. Large reduction of power consumption is possible by bringing the bandwidth of the gain-block close to the desired frequency of oscillation. However, the phase delay of the gain-block will cause oscillation to occur at a frequency offset from tank resonance where the tank will be slightly inductive and provide necessary phase lead to counter the delay. This offset will be determined by the tank's Q and the bandwidth of the gain-block. Optimum power reduction will be achieved when the oscillation frequency will settle in the steep portion of tank-phase curve where frequency sensitivity to noise is the least.

A detailed schematic of the proposed oscillator is provided in Fig. 2.12. The core structure consists of a "G_m-cell" and a gain block "A-cell". A-cell is self-biased with a large resistor RF at its threshold point where it provides maximum gain. The G_m-cell is DC-coupled with A-cell and they have the equal device-size and bias currents to have the same threshold point. The tail current sources have large capacitances at outputs to form low-pass filters for supply noise with very low corner frequency. C_c and C_2 decouples the two cells from inductor so it doesn't disrupt their bias conditions. The corner frequency from C_c and R_F should be much less than the oscillation frequency. A digital single-ended inverter chain operates as a buffer to convert the sinusoid voltage v_t to square waveform. The input capacitance of the buffer is small compared to tank capacitance and does not affect the core loop.

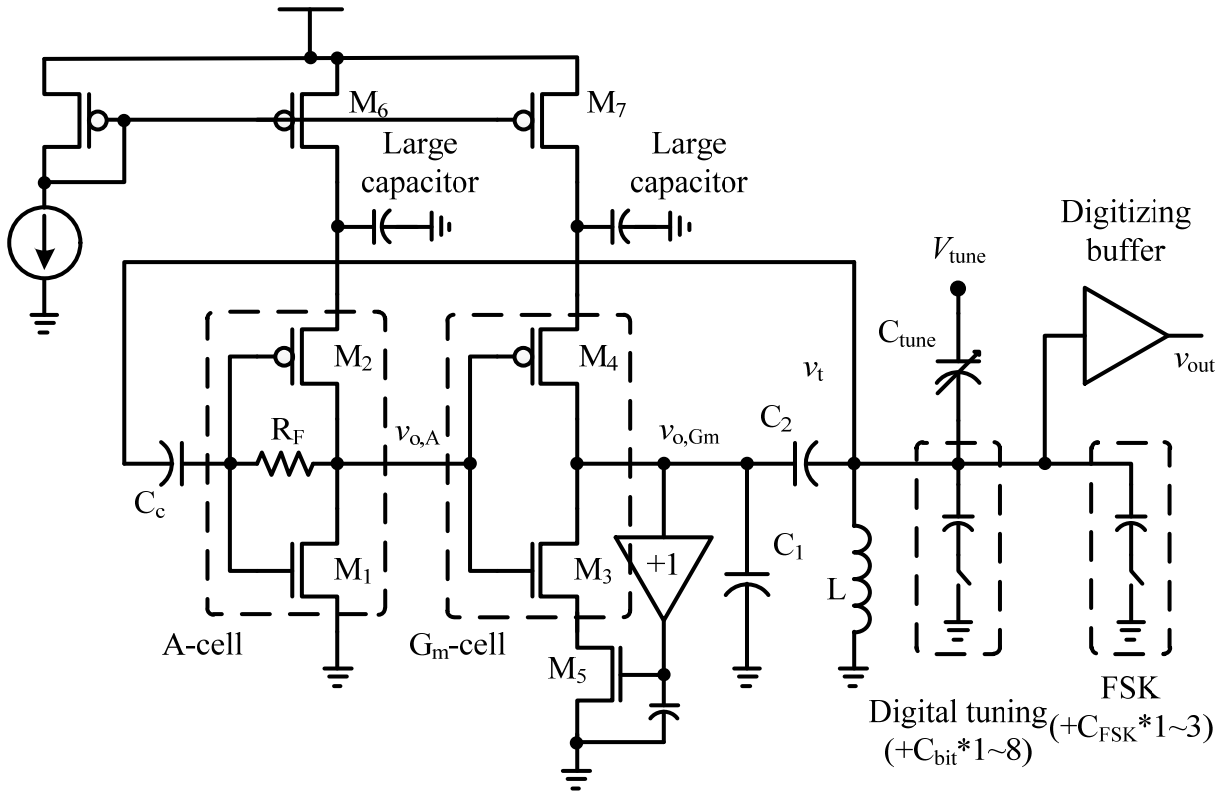


Fig. 2.12. Detailed schematic of the gain-boosted LC VCO.

2.5.1.2 G_m-cell Bias Stabilization

The PMOS side of the G_m-cell is starved and the discharge of this node through the un-starved NMOS side is stronger. This imbalance causes a non-linear *V-I* curve for the Gm-cell which causes increase in the DC tail current draw of this cell after oscillation starts. This increases the V_{DS} of M_7 and reduces DC average of $V_{o,Gm}$. This disrupts the bias condition of the G_m-cell, preventing sustained oscillation. To address this problem, M_5 is added, which is controlled by the DC average of $V_{o,Gm}$ and stabilizes $V_{o,Gm}$ by balancing the charging and discharging currents onto $V_{o,Gm}$. Thus the oscillation is sustained. The DC average is generated with a low-pass filter formed by a small capacitor and a single-stage differential amplifier, configured for unity-gain.

2.5.1.3 Tuning System

The GB-LC used in this work includes two tuning systems and a BFSK (Binary Frequency Shift Keying) modulation system. All three systems change the tank capacitance to change the tank resonance frequency and thus oscillation frequency is tuned.

The analog tuning system is a narrow-range one which is available for PLL to tune the GB-LC to correct phase error, relative to reference. The tuning gain, K_{VCO} (kHz/mV) is designed to be small to reduce the reference spurs, resulting from noise in reference frequency. It consists of a varactor (NMOS in N-well capacitor), C_{tune} connected to the tank. It is controlled by a rail-to-rail (0 – 1.2 V) input voltage, V_{tune}, with the highest frequency obtained when $V_{tune} = 0$ V. The frequency range of analog tuning, and hence sensitivity, is affected by the digital tuning configuration. C_{tune} is sized so the tuning range varies within 22.5 – 30.2 MHz, which almost covers the 915 MHz ISM band.

To counter process and supply variations, a wide-range digital tuning system is used along with the narrow-range analog tuning. It consists of 8 equal-sized capacitances controlled by a 4-bit word and provides a 9-step tuning. With tuning code '0', all the capacitors are switched off and oscillator frequency is highest. With codes '1' – '8', the corresponding number of capacitors is switched on and adds to the equivalent tank capacitance to lower oscillation frequency. This system provides a tuning range of about 80 MHz with the 902 – 928 MHz ISM band at center, which is sufficient to counter process variations.

The BFSK modulation system is similar to the digital tuning system. It consists of three small, equal, switched capacitors. These capacitors are switched, individually or in combination, with an FSK input. Each capacitor, when switched on, connects in parallel to the tank, reducing oscillation frequency by about 550 kHz. Combination of two or all three capacitors can be used to increase the shift to 1.2 MHz or 1.825 MHz, respectively.

2.5.2 Mathematical Analysis

2.5.2.1 Estimation of Oscillation Frequency

The GB-LC VCO would operate similar to a conventional negative-g_m oscillator at the LC tank resonance frequency provided that the A-cell has bandwidth much higher than the resonance frequency. In this case, the two cells will each provide 180º phase shift and total phase shift would be 360º around the loop. The gain cell's bias current can be varied to shift the tradeoff between power consumption and phase noise. To reduce the power consumption, the gain cell bandwidth is set close to the oscillation frequency. As a result, phase shift from the A-cell would be more than 180º and oscillation frequency will be slightly lower than resonance frequency where the tank will provide phase lead to cancel the extra phase delay. The frequency of oscillation can be thus

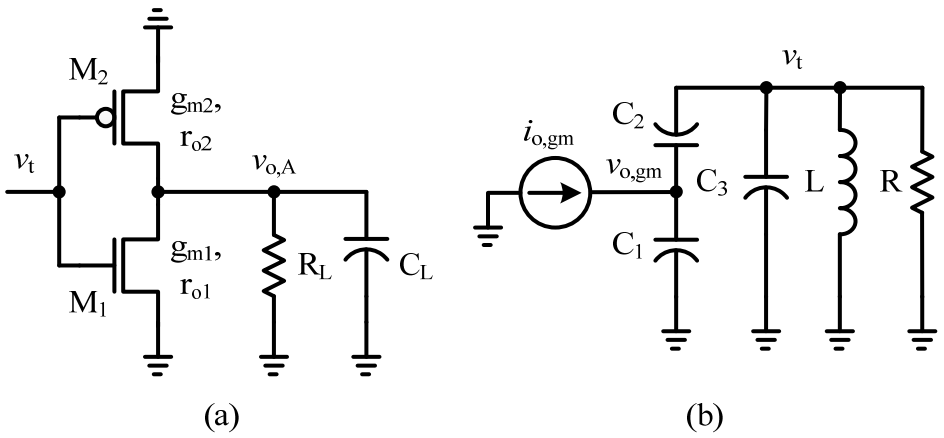


Fig. 2.13. AC equivalent circuits of the A-cell (a) and LC tank (b) for estimating oscillating frequency with phase-balance equation.

determined by estimating the phase lead and lag from the tank and A-cell respectively. AC equivalent circuits of these two parts are shown in Fig. 2.13. For simplicity, the 180º phase shifts of the two cells will be ignored as they cancel each other and only the excess phase will be calculated.

The phase delay of the A-cell can be determined from its transfer function, which is given by the following equations.

$$A = \frac{|A|}{1 + j\,\omega/\omega_c} = \frac{|A|}{1 + j\omega R_L C_L}$$

$$|A| = (g_{m1} + g_{m2})(r_{o1} \| r_{o2})$$

$$R_L = r_{o1} \| r_{o2} \| \left(\frac{R_F}{1 + 1/|A|} \right) \tag{7}$$

$$C_L = C_{i,Gm} + C_{RF}/2 + C_{dg,A}\left(1 + 1/|A|\right) \tag{8}$$

Here $C_{i,gm}$ is the input capacitance of G_m-cell, C_{RF} is parasitic capacitance of polysilicon resistor R_F and $C_{dg,A}$ is the drain-gate capacitance of the A-cell. R_F is large enough to provide only DC feedback for the A-cell and no significant ac negative feedback. With the values of design parameters of the proposed oscillator, $|A|$ and ω_c are calculated to 12.493 V/V and 7.5457 Grad/s. The phase delay of the A-cell is given by

$$\theta_A = \tan^{-1}\left(\omega / \omega_c\right). \tag{9}$$

The output current of the G_m-cell, $i_{o,Gm}$ is in phase with $v_{o,A}$, neglecting the 180º phase shift. The phase lead in v_t from $i_{o,gm}$ or $v_{o,A}$ would be the phase angle of the LC network, θ_t. In the LC network, C_1 and C_2 are metal-to-metal capacitors and C_3 and R is given by the following equations.

$$C_3 = C_{2,bot} + C_{c,bot} + C_P + C_{i,A} + C_{RF}/2$$

$$R = R_P \left\| \left(R_F / 1 + |A| \right) \right. \tag{10}$$

Here, $C_{2,bot}$ and $C_{c,bot}$ are bottom-plate capacitances off C_2 and C_c, C_P is the parasitic capacitance of inductor L, $C_{i,A}$ is the input capacitance of A-cell. R_P is the equivalent parallel tank resistance. Mid-band gain $|A|$ is used in (7), (8) and (10) to simplify the analysis. v_t is given by the following equation.

$$v_t = i_{o,Gm} \cdot \frac{R \left\| sL \right\| 1/sC_3}{1 + C_1/C_2 + sC_1\left(R \left\| sL \right\| 1/sC_3\right)} \tag{11}$$

θ_t can be determined from (11) as in the following expression.

$$\theta_t = \tan^{-1} \frac{R\left(1 - \omega^2 LC_{eff}\right)}{\omega L} \tag{12}$$

Here, $C_{eff} = C_3 + C_1C_2 / C_1 + C_2$. Oscillation will occur at a frequency where θ_t and θ_A balance each other so the total phase shift around the loop is zero.

$$\theta_t + \theta_A = 0 \tag{13}$$

Equation (13) may be referred to as the "Phase-balance equation". Using (9), (12) and (13), oscillation frequency, f_{osc} is given by

$$f_{osc} = \frac{1}{2\pi}\sqrt{\frac{\omega_c R}{L\left(1+\omega_c R C_{eff}\right)}}. \tag{14}$$

For this design, f_{osc} is calculated to be 1.154 GHz using (14), ignoring the added capacitors of the tuning systems. Simulation predicts oscillation at 1.126 GHz. The tuning capacitors with their parasitics will add to C_3 and with the tuning switched off, simulation predicts f_{osc} to be 948.5 GHz where θ_t is about 48º. The digital tuning system is then used to tune to the ISM band.

2.5.2.2 Criteria for Oscillation

A small-signal equivalent circuit of the oscillator core is shown in Fig. 2.14. The gain block represents the A-cell and the voltage-dependent current source represents the G_m-cell, where g_m is

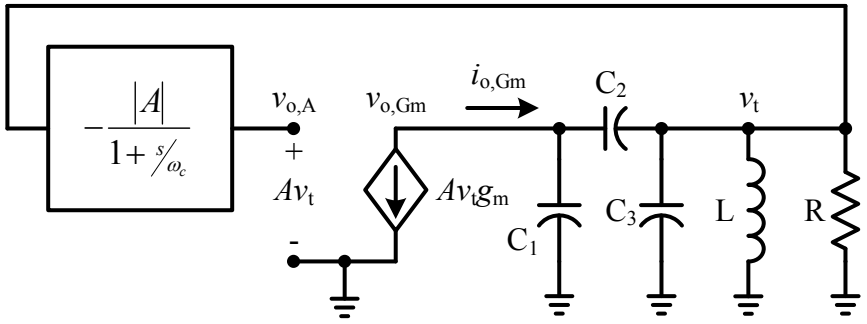


Fig. 2.14. Small-signal equivalent circuit of the GB-LC oscillator core.

the sum of the g_ms of M_3 and M_4. To simplify analysis, the small-signal output resistance, r_o, of M_3 and M_4 is ignored.

The relationship between $i_{o,Gm}$ and v_t is given by (11) and $i_{o,Gm}$ is given by the following equation.

$$i_{o,Gm} = -Av_t g_m = \frac{|A|}{1+sT_c} \cdot v_t g_m \tag{15}$$

Here $T_c = 1/\omega_c$. Combining (11) and (15), the following expression is obtained.

$$\frac{|A|}{1+sT_c} \cdot v_t g_m \cdot \frac{R \| sL \| 1/sC_3}{1 + C_1/C_2 + sC_1 \left(R \| sL \| 1/sC_3 \right)} = v_t \tag{16}$$

Assuming oscillation has begun, $v_t \neq 0$ and simplifying (16) leads to

$$\begin{aligned} s^3 T_c LRC_{eff} + s^2 L\left(T_c + RC_{eff}\right) + \\ s\left(L + RT_c - |A| g_m LR\tfrac{C_2}{C_1+C_2}\right) + R = 0. \end{aligned} \tag{17}$$

Equation (17) is the characteristic equation of the proposed GB-LC VCO. Using $s = j\omega$ then rearranging the real and imaginary terms of the equation leads to

$$\begin{aligned} R - \omega^2 L\left(T_c + RC_{eff}\right) + j[\omega(L + RT_c - \\ |A| g_m LR\tfrac{C_2}{C_1+C_2}) - \omega^3 T_c LRC_{eff}] = 0. \end{aligned} \tag{18}$$

Equating the real part of (18) to zero yields

$$\omega^2 = R/L\left(T_c + RC_{eff}\right). \tag{19}$$

Equation (19) gives the frequency of oscillation, which is same as (14).

Equating the imaginary part of (18) to zero and using (19), the condition for steady-state oscillation is derived.

$$g_m R = \left(1 + \left(f_{osc} / f_c\right)^2\right)\left(1 + C_1 / C_2\right) 1 / |A| \tag{20}$$

Initially, for oscillation to start and grow, $g_m R$ needs to be greater than the right-hand side of (20). The following observations about g_m requirement can be made from (20):

1) Required g_m increases with the ratio of C_1 and C_2. If C_2 is chosen much larger than C_1, as in this design, this leaves g_m unaffected.
2) g_m can be reduced in proportion with increase in $|A|$.
3) g_m is also influenced by the high corner frequency of the A-cell. The larger the bandwidth, f_c, is relative to oscillation frequency, the lower g_m is required.

The second and third observations show how power consumption is reduced in the proposed GB-LC VCO. For example, if A-cell is designed with a $|A| = 10$ and $f_c = f_{osc}$, required g_m is 5 times lower than what would be required without the A-cell, thus allowing a much lower startup power than conventional LC oscillators. However, the A-cell would also require significant power. This is where total power consumption of the VCO can be optimized. The A-cell has a much smaller load capacitance than the G_m-cell driving the LC-tank and its bandwidth and gain are determined by its bias current. Thus, a large f_c can be achieved for the A-cell. With high power, the A-cell may have an f_c much higher than f_{osc} and its phase delay, θ_A would be very small and thus f_{osc} would be very close to tank resonance where frequency sensitivity to the device and supply noises are minimized. In this case, the proposed oscillator would have same noise tolerance as a conventional LC oscillator. This is shown in shown in Fig. 2.9, where the GB-LC curve coincides with the Colpitts curve. Trading off noise performance for lower power consumption, f_c can be chosen close to desired f_{osc} while θ_A is small enough for f_{osc} to still remain in the steep portion of the tank-phase curve, achieving acceptable noise tolerance. Thus total power consumption can be

optimized to be much lower than conventional LC oscillators with sufficiently low phase noise and supply sensitivity.

2.5.2.3 Phase Noise

It is known that one of the reasons LC oscillators have generally better phase noise performance than ring oscillators is that in a ring oscillator, charge injections onto a node occur during transitions of the driving delay cell [23]. This is when device noise is at a maximum and also when the sensitivity is highest as shown by the ISF in Fig. 2.5. In LC oscillators, for example in Colpitts, charge injection to the tank occurs at or near the voltage peak where the ISF is the lowest. As a result, device noise has a much smaller effect than in ring oscillators.

The proposed GB-LC oscillator's normalized waveforms are shown in Fig. 2.15. The G_m-cell, driven by the almost square waveform output of A-cell, injects charge ($i_{o,Gm}$) into the LC tank and this injection is spread across a wide time-length around tank voltage (v_t) peak instead of in the form of a narrow pulse at the peak that is usual in LC oscillators. This means charge injection is occurring at times other than that which minimizes ISF. As a result, phase noise is degraded in this oscillator structure compared to LC oscillator. Compared to the ring oscillators (where the full 360° phase shift around the loop is contributed by noise-sensitive delay cells), in this hybrid oscillator, about 40-50° extra phase delay is provided by the single delay cell, which is corrected by the G_m-cell-tank combination to have a 0° or 360° around the loop. As a result, oscillation frequency is less sensitive to delay-cell noise in this hybrid structure.

Phase noise of this GB-LC VCO in the $1/f^2$ region can be predicted using the following form of widely used Leeson's equation [32] [19].

$$L\{\Delta\omega\} = 10\log\left[\frac{2FkT}{P_{sig}}\cdot\left(\frac{\omega_o}{2Q_{eff}\Delta\omega}\right)^2\right] \tag{21}$$

Here, k is Boltzmann's constant, T is absolute temperature, P_{sig} is the power of the output signal or signal at the tank node Q_{eff} is the effective quality factor of the LC tank, ω_o is the oscillation frequency, $\Delta\omega$ is offset frequency. F is known as the device excess noise number, which is an *a posteriori* fitting parameter on measured data. Since oscillation frequency is offset from the tank resonance frequency in this structure, Q_{eff} will be lower than the loaded Q of the LC tank. Q_{eff} can be determined by the following equation [33].

$$Q_{eff} = \frac{\omega_o}{2}\left|\frac{d\phi}{d\omega}\right|$$

Here $\frac{d\phi}{d\omega}$ is the slope of the phase transfer function of the LC tank at the oscillation frequency. The value of F is chosen to be 5 based on post-layout simulation result of the proposed VCO. Fig. 2.16 shows simulated phase noises at 1 MHz offset frequencies of the GB-LC structure at different power consumptions. The device sizes are scaled as the power consumption is increased by increasing bias current. Pre-layout simulations are performed on two different GB-LC structures to verify the estimations from (21). In one structure, the A-cell and the G_m-cell has equal device sizes and bias current. In the other one, the G_m-cell is reduced to half of the A-cell in device sizes and bias current. Estimations of phase noise using (18) show only 2-3 dB errors from the simulated values. For the proposed GB-LC, phase noise at 1 MHz offset frequency is found to be -99.3 dBc/Hz using (21).

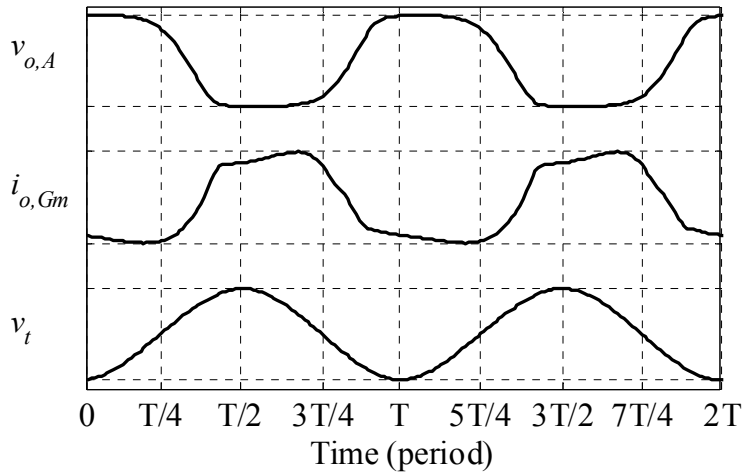


Fig. 2.15. Normalized waveforms of the GB-LC oscillator in post-layout simulation.

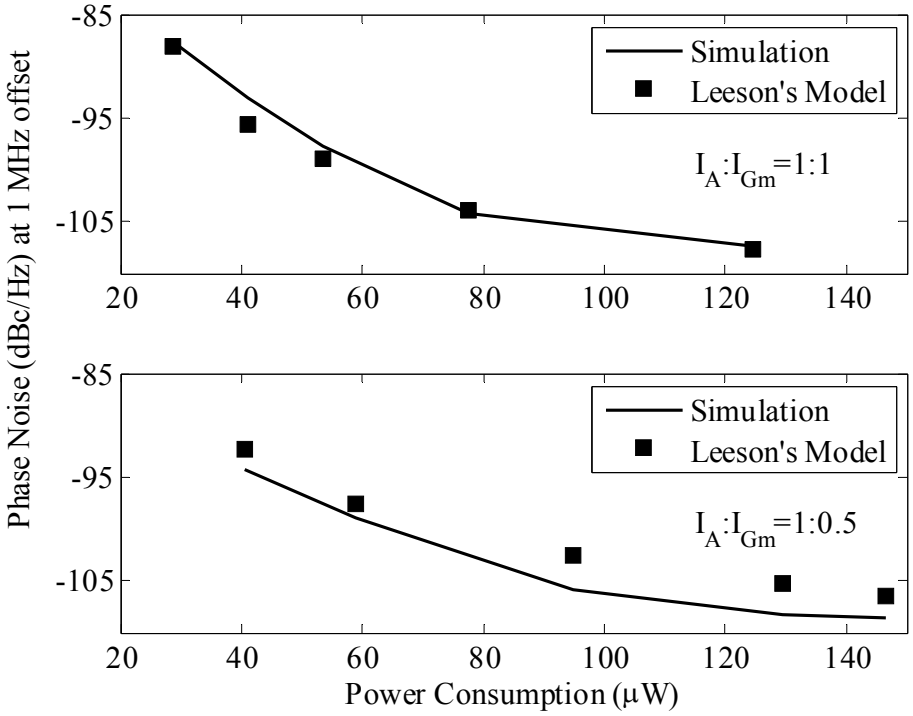


Fig. 2.16. Simulated (pre-layout) phase noise of the proposed GB-LC VCO at different power consumptions. Phase noise can be predicted using Leeson's model with $F = 5$. Two different structures of the VCO are simulated – one where the ratios of device sizes and bias currents between the A-cell and the Gm-cell are both 1:1 and another where the ratios are both 1:0.5.

2.5.3 Measured Performance

A GB-LC VCO has been implemented in a 0.13 µm 1P8M CMOS process for testing. Fig. 2.17 shows the microphotograph of the fabricated oscillator. The core and the bias circuit occupies 360×340 µm^2 and 245×345 µm^2 areas, respectively. The on-chip inductor is 36.87 nH with 220×220 µm^2 area with metal ground-shield.

To avoid the parasitic effects from packaging, chip-on-board bonding was used. The measurements were performed with Agilent N9010A EXA signal analyzer. The BFSK GB-LC's spectra are shown in Fig. 2.18, which shows 550 kHz frequency shift, operating at 914.5 MHz. With all three FSK inputs driven together, the measured shift increases to 1.825 MHz. The measured phase noise spectrum is provided in Fig. 2.19, showing -97.9 dBc/Hz at 1 MHz offset.

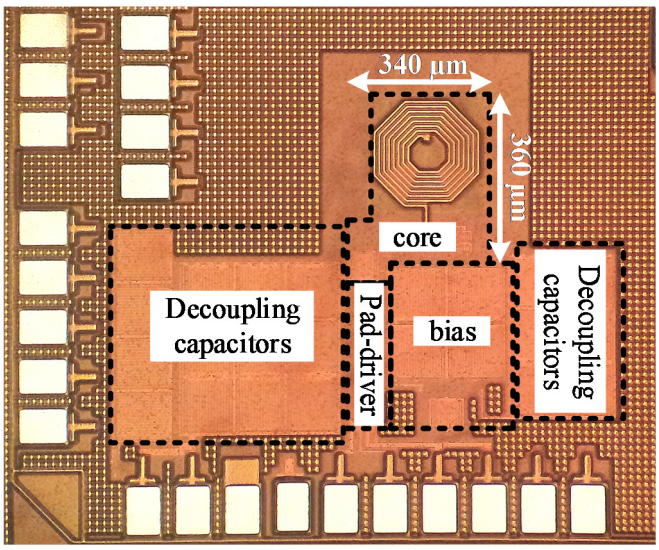


Fig. 2.17. Microphotograph of the fabricated GB-LC VCO in a bare die. The core occupies 360×340 µm^2 chip area. The bias circuit occupies 245×345 µm^2 chip area.

Fig. 2.20 shows the constellation diagram and error statistics of BFSK-modulated output of the GB-LC. The oscillator is modulated with a 100 kHz, 50% duty cycle square wave simulating a '01010101' bitstream at 200 kbps rate. The selected frequency shift is 550 kHz. The two clusters for two bits in the constellation diagram are well separated and rms FSK error is about 11.5% which is adequate for most low-cost wireless applications [7]. BER can be predicted from this data by calculating the probability of a random variable from a Gaussian distribution, with 0 mean and 11.5% standard deviation, to be greater than 0.5. Thus BER is calculated to be 6.87 ppm.

Fig. 2.21 shows the tuning range of the two tuning systems included in the fabricated GB-LC. The digital tuning range is measured to be 80 MHz, which is sufficient to allow for process variations. The analog tuning range varies from 22.5 to 30.2 MHz and with digital tuning code set to '3', covers the entire 902 – 928 MHz ISM band. With the help of digital tuning, any frequency in the ISM band can be reached by varying V_{tune} within the lower almost linear portion of the analog range.

The proposed GB-LC oscillator, along with its digitizing output buffer, consumes 166.8 μW from a 1.2 V power supply, when tuned to 914.5 MHz. This excludes power consumed by the additional pad-driver buffer which drives the external 50 Ω load. The digitizing output buffer consumes about 30% of the total 166.8 μW power, as predicted by post-layout simulation. Minimum startup current is measured to be 100 μA.

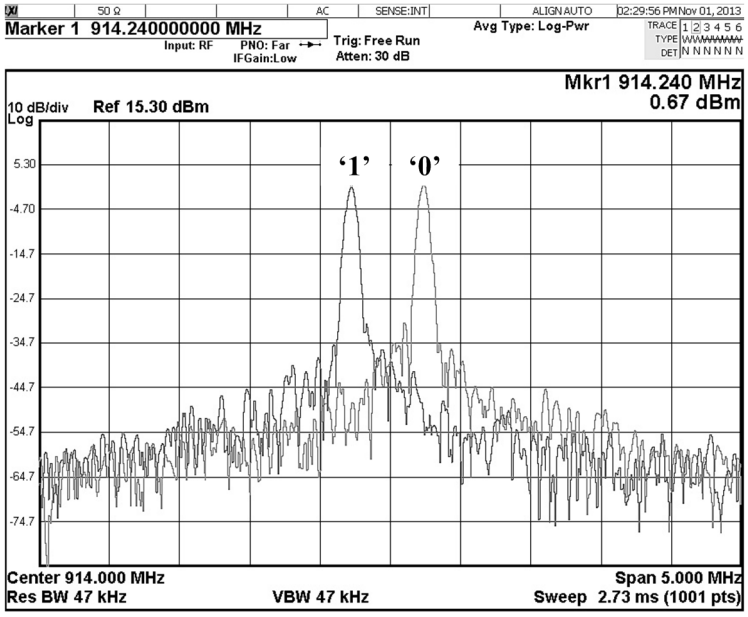


Fig. 2.18. Measured output spectra of the the BFSK GB-LC VCO showing about 550 kHz frequency shift around 914.5 MHz center frequency.

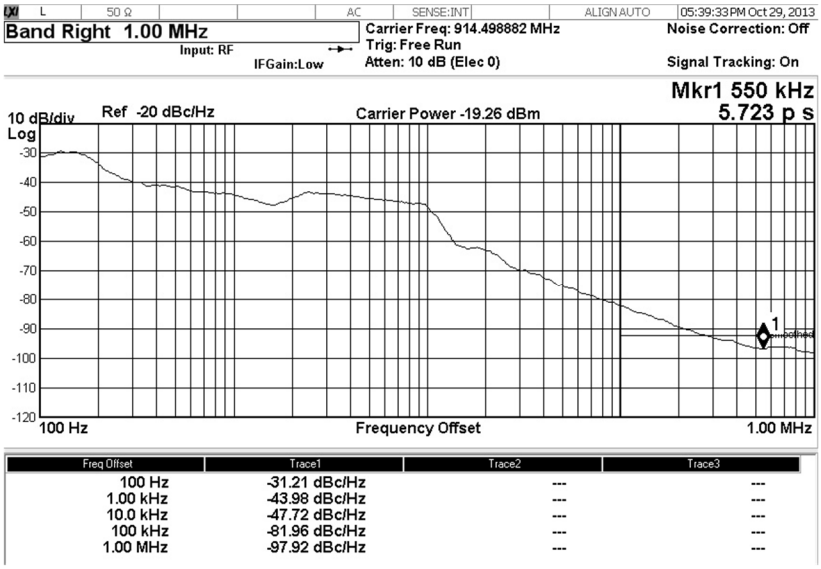


Fig. 2.19. Phase noise spectrum of the GB-LC VCO output at 914.5 MHz. Phase noise is -97.9 dBc/Hz at 1 MHz offset.

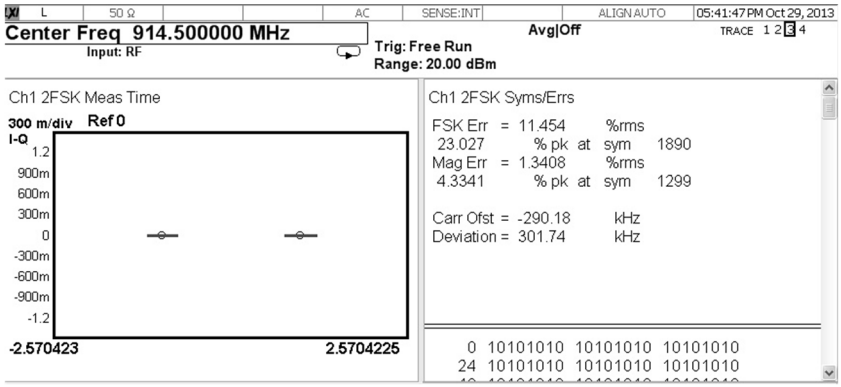


Fig. 2.20. Constellation diagram and FSK error results of the GB-LC VCO output. The oscillator is tuned to 914.5 MHz and is 2-FSK modulated with a 100 kHz, 50% square wave simulating '01010101' bitstream at 200 kbps rate. RMS FSK error is about 11.5%.

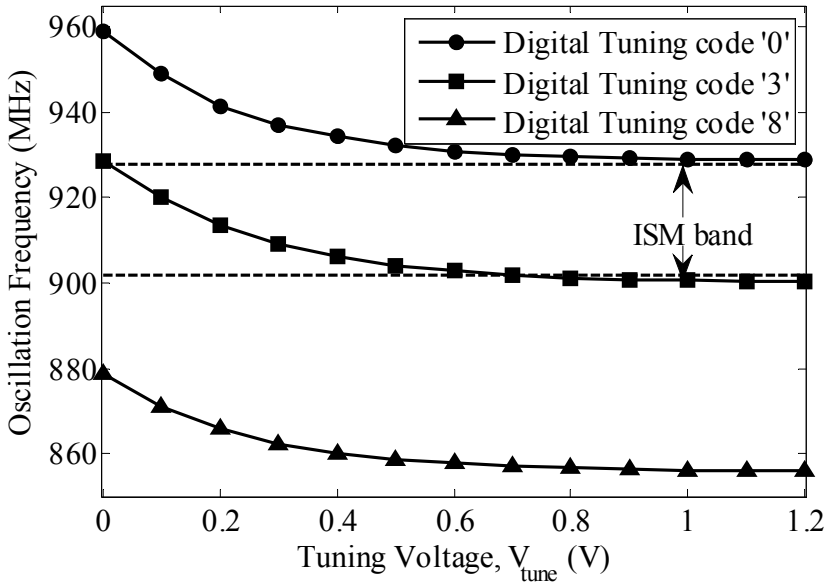


Fig. 2.21. Tuning range of the GB-LC VCO. The digital tuning system has a range of 80 MHz which is sufficient to cover for process variations and the analog tuning range varies from 22.5 MHz to 30.2 MHz, corresponding to digital tuning code '0' to code '8'.

Figure-of-Merit (FoM) of the GB-LC is calculated using the following equation [20].

$$FoM = 10\log_{10}\left[\frac{1}{P}\left(\frac{f_o}{\Delta f}\right)^2\right] - L(\Delta f)$$

Here $L(\Delta f)$ is phase noise in dBc/Hz at Δf offset from oscillation frequency f_o with power consumption of P mW. Thus FoM is calculated to be 164.9 dB. Table 2.1 shows comparison of this oscillator to some existing works. The FoM achieved by the GBLC is somewhat inferior to the LC oscillators, and superior to most of the ring oscillators in Table 2.1. This work has been reported in [34].

Table 2.1. Performance comparison of the fabricated GB-LC with state-of-the-art.

Works	Topology	Process (nm)	Frequency (GHz)	Power (mW)	Phase noise (dBc/Hz)	Supply sensitivity (ppm/mV)	FoM (dB)
[35]	Ring	130	7.64	60	-103.4 @ 1 MHz	-	163.2
[26]	Ring*	65	1.38	0.046	-98 @ 10 MHz	53.3	154.2
[28]	Ring**	130	4	42	-	37.5	-
[27]	Ring	180	2.5	10.1	-92.42 @ 1 MHz	9.6	150.3
[24]	Ring	65	0.685	10	-110.8 @ 1 MHz	-	157.0
[36]	LC	90	0.915	0.38	-117 @ 1 MHz	-	180.4
[37]	LC	90	5.63	14	-108.5 @ 1 MHz	-	172.0
[25]	LC	180	1.19	1.06	-126 @ 1 MHz	-	187.3
[20]	LC	65	5.52	9.8	-151.7 @ 20 MHz	-	190.6
[38]	LC	180	4.6	2.4	-139.5 @ 10 MHz	-	189.0
This work	GB-LC	130	0.9145	0.1668 (core) 0.1169	-97.9 @ 1 MHz	35.0	164.9

* Self-calibrated ring oscillator

** Ring oscillator is integrated into a PLL instead of free-running.

Chapter 3 Low-Power Prescaler

The prescaler is the first stage of the frequency dividing feedback path in a typical PLL. Fig. 3.1 shows the topology of the commonly used pulse-swallowing frequency divider with a dual-modulus prescaler with division ratios selectable between N and N+1 by "modulus control". Here "P" is set to be larger than "S" in the counters. The division ratio of the full divider is NP+S.

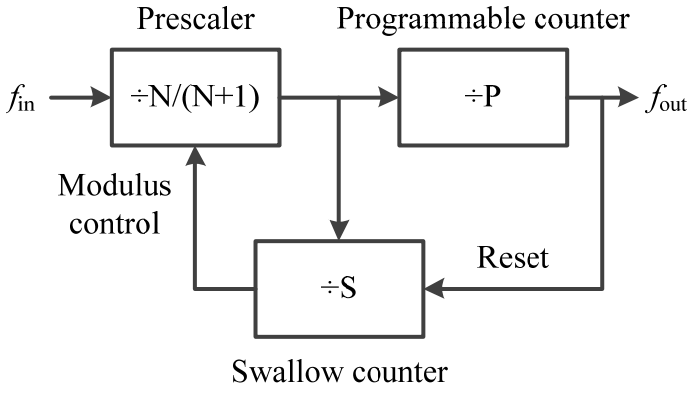


Fig. 3.1. Topology of the commonly used Pulse Swallow frequency divider [39].

The prescaler divides down the VCO frequency by a small ratio, so that the subsequent dividers (counters) can operate at low frequency with low power cost. Besides the VCO, the prescaler is the other block in a PLL running at full RF and thus, is another dominating block in a PLL power budget. Therefore, it is highly desirable to design an ultra-low-power prescaler to reduce PLL's power consumption.

Another important parameter of the prescaler is the locking range, which is the difference of minimum and maximum input frequency the prescaler can operate on. In a PLL, the full tuning range of a VCO should be well within the divider's locking range to avoid any VCO "runaway"

condition where at startup VCO oscillates at a frequency beyond the PLL locking range. Wide locking range is also very desirable to accommodate multi-band PLL operation. Moreover, a PLL design with good channel resolution benefits from multi-modulus dividers. Various structures for prescalers have been developed with a focus on maximizing the locking range and reducing power consumption. These structures can be divided into two broad categories – digital logic dividers and oscillator-based injection-locked dividers.

3.1 Digital Logic Frequency Divider

A digital prescaler is a synchronous circuit which is formed by D flip-flops. Additional logic gates are incorporated between the flip-flops to easily achieve multi-modulus operation, i.e. different division ratios. Due to these additional gates, the speed of the prescaler is affected and the switching power increases. To reduce number of devices, the additional gates are sometimes fused with flip-flops [39]. Various flip-flops have been proposed to improve the operating frequency, including current-mode logic (CML) [40], true single phase clocked logic (TSPC) [39] and extended-TSPC (E-TSPC) [41] logic flip-flops.

CML prescalers use logic cells that provide the highest speed among known topologies with the cost of high power consumption (up to tens of milliwatts). For this reason, they are used only at very high frequencies where other topologies cannot operate. TSPC prescalers are dynamic CMOS logic circuits that operate on only one clock signal to avoid problems associated with skew between complementary clock phases [39]. They have the lowest power consumption, typically on the order of several hundred microwatts [42], but they also offer operating speed lower than CML and are usually limited below 5 GHz [43]. E-TSPC prescalers are similar to TSPC circuits but use one less transistor in each branch, reducing total switching load. This increases the

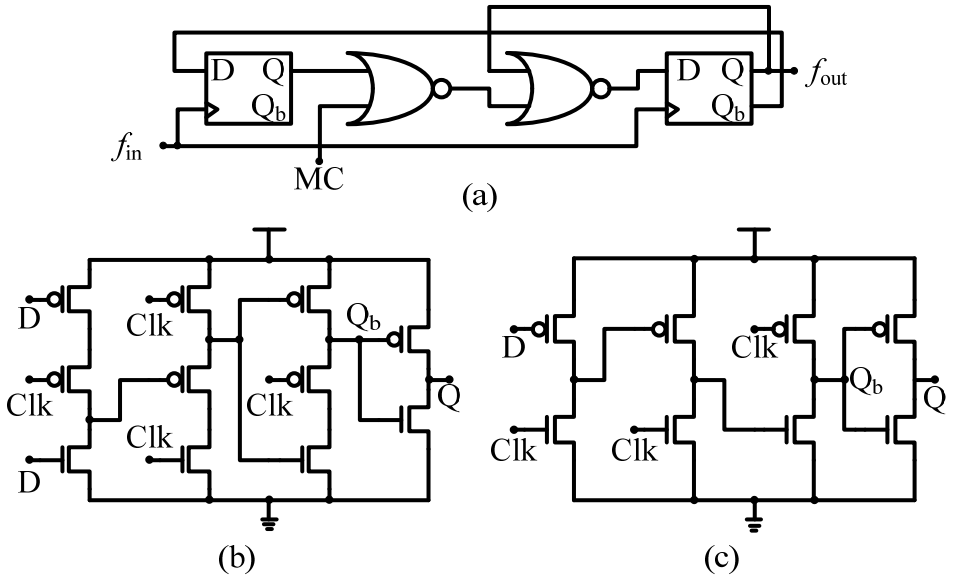


Fig. 3.2. (a) A TSPC-based divide-by-2/3 prescaler reported in [39] and (b) TSPC and (c) E-TSPC flip-flops.

maximum operating frequency, but also increases short-circuit power (power consumed in a period during which a direct path exists between supply and ground, causing short-circuit). It has been shown in [39] that due to this fact E-TSPC prescalers are more power-hungry than TSPC prescalers and this power is also affected by the input signal amplitude and DC level, unlike TSPC. For this reason, a TSPC prescaler is usually preferred among digital prescalers as long as it satisfies the speed requirement. Commonly used dual-modulus TSPC prescalers are divide-by-2/3 and divide-by-3/4 prescalers [42] that can be chained together to achieve arbitrary division ratios. Fig. 3.2 shows one such TSPC-based divide-by-2/3 prescaler reported in [39] along with TSPC and E-TSPC flip-flop topologies. One of the improved TSPC prescalers reported here achieves maximum locking frequency of 4.9 GHz and consumes 306 μW power when locked at 2 GHz input in divide-by-2 mode (16 GHz/mW).

3.2 Injection-Locked Frequency Divider

It has been shown that a free-running oscillation can be pulled or tuned to a different oscillation frequency when an external oscillatory force at a nearby frequency is injected into it [44] [45]. Injection-locked frequency dividers (ILFD) are based on this fact and use oscillators that run at a sub-harmonic frequency of an injected input signal. This effectively lowers the speed requirement for the process technology by N-fold, N being the division ratio. Thus, compared to their digital counterparts, analog dividers such as ILFDs can achieve much lower power operation. That is why ILFDs are usually preferred for ultra-low-power operations [46].

ILFDs can be either based on LC oscillators or ring oscillators. However, LC-based Is are useful only with high frequencies [47] [48]. Inductors occupy large areas in low-frequency operation and that makes this type of ILFD unsuitable for area-efficient implementations. The locking range achievable is also usually narrower than ring-based dividers because of its narrow-band nature. Ring-based ILFDs can be very area- and power-efficient in low-frequency operation. The low Q and hence, inherent broadband nature of CMOS ring oscillators helps achieve large locking range. Although the phase noise of traditional ring oscillators is high, the noise dramatically performance improves when locked to a clean reference [49].

Fig. 3.3 shows a simplified architecture, presented as the Miller-type model in [45], of ILFD. It includes memoryless non-linear functions *g* and *f* and a multiplier to represent the mixing

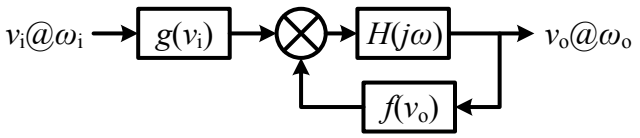


Fig. 3.3. Miller-type model for injection-locked frequency divider [45].

of an injected signal (ω_i) with ILFD output (ω_o), which generates multiple harmonic tones ($n\omega_i \pm m\omega_o$). The band-pass filter $H(j\omega)$ filters out all frequencies other than ω_o, which is a Nth sub-harmonic of the injected frequency (ω_i/N). To compensate for the phase-shift in the injector portion, the phase shift from $H(j\omega)$ changes so that the net phase around the loop remains integer multiples of 2π. The loop changes the oscillation frequency to accommodate this phase shift. Thus, ω_o is synchronized with sub-harmonics of the injection signal and tracks ω_i and divide-by-N operation is achieved.

In [49], a divide-by-5 ILFD based on a 5-stage, single-ended ring oscillator is reported that achieves ultra-low-power operation. The structure of the divider, along with the analytical model of one stage is shown in Fig. 3.4. The function block, $f(\ldots)$, represents non-linear transformation on the summation of two signals – input voltage at the gate and the corresponding injection input at S node. The linear block, $A(\omega)$, represents the transfer function of one stage, which is typically a first-order low-pass filter, that is $A(\omega) = A_o \Big/ 1 + j\frac{\omega}{\omega_p}$. Here A_o is the low-frequency gain and ω_p is the output pole of the stage.

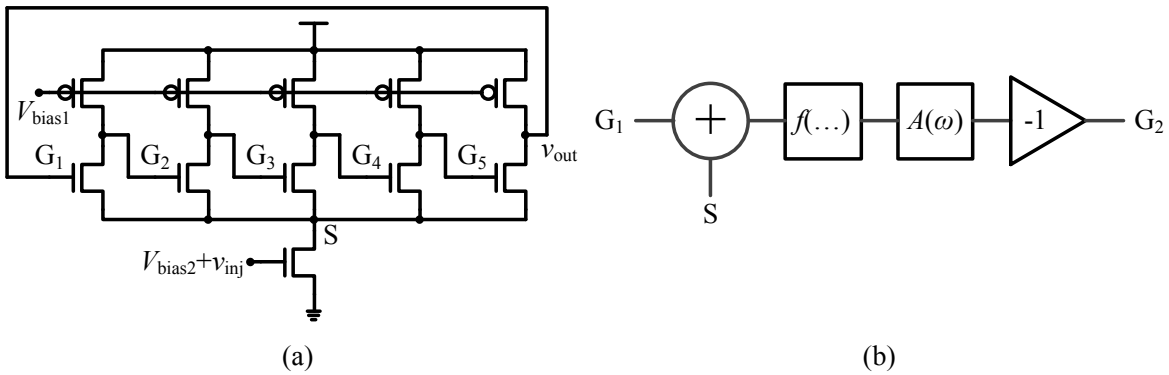


Fig. 3.4. (a) Ultra-low-power divide-by-5 ILFD reported in [49] and (b) analytical model for one stage of the ILFD.

The input signal is injected into the shared source-node, S, of the 5 stages. In free-running oscillation with frequency, the G nodes have large swings with $2\pi/5$ radian phase shift between adjacent G nodes. In this case, the S node experiences a large 5^{th} harmonic component. When the ILFD is locked to $5\omega_o$ frequency at v_{inj}, where ω_o is the output frequency, the actual strength of the injected current that reaches the individual stage has strong 1^{st} to 5^{th} harmonics of ω_o. The nonlinear block mixes with a strong tone of ω_o and its harmonics at G_1 and generates a strong component of ω_o. The higher frequency components are filtered out by $A(\omega)$ with ω_p close to ω_o. The DC and lower frequencies are blocked by the loop which has a negative gain at low frequencies.

The observations made in [49] on ring-based ILFD are as follows –

1) The locking range decreases for higher division ratios as increased number of stages results in sharper band-pass filtering.
2) As the lock frequency is moved away from free-running frequency, input signal strength needs to increase to provide additional gain to meet Barkhausen Criterion of loop gain.
3) If the DC bias current is increased, ω_p of the stages is increased. Thus with higher power consumption, free-running frequency as well as absolute locking range will increase, but relative or fractional locking range will remain same.

Various ultra-low-power ILFDs has been reported. For example, the divider in [49] consumes only 3 μW locked at 400 MHz input frequency. Another 43 μW ILFD is reported in [50] that operates at 6 GHz input frequency. On the other hand, ILFD's locking range is limited on both high and low ends, such as 56% in [49] or 80% in [50] unlike digital dividers that can

operate on incoming frequencies approaching DC. Compared to the digital dividers, ILFDs are also hard to design for multi-modulus operation and require complex circuitry, such as programmable delay chain [51], multi-phase injection inputs [52], complex design method [53] or multiple oscillator cores [54].

3.3 Hybrid Frequency Divider

From the previous sections it can be understood that a ring-oscillator-based ILFD or a TSPC-based digital prescaler would be the practical choice for a prescaler in a low-power sub-GHz PLL. It is also discussed that ILFDs come with narrower locking ranges than dynamic logic prescalers while consuming lower power than them. ILFDs are also difficult to design for multi-modulus operation.

For this work, a dual-modulus (4/5) hybrid frequency divider is designed and tested that combines features from dynamic logic dividers and injection-locked dividers to simultaneously achieve wide fractional locking range and ultra-low power consumption. The divider is designed in 90 nm CMOS process with detailed design considerations presented in [55] and mathematical analysis and measurement results reported in [56]. Fig. 3.5 shows the comparison between the hybrid divider and state-of-the-art, considering fractional locking range and figure-of-merit (FoM). Here FoM is defined in GHz/mW as the ratio of operating frequency to corresponding power consumption.

The topology of the divide-by-4/5 hybrid divider is shown in Fig. 3.6. Similar topologies are reported in [57] and [58]. However, the topology in [57] is an injection-locked divider with sinusoidal injection signal only varying the edge-times of the ring oscillator core and is not optimized for power consumption. The topology in [58] is also not exploited for maximizing

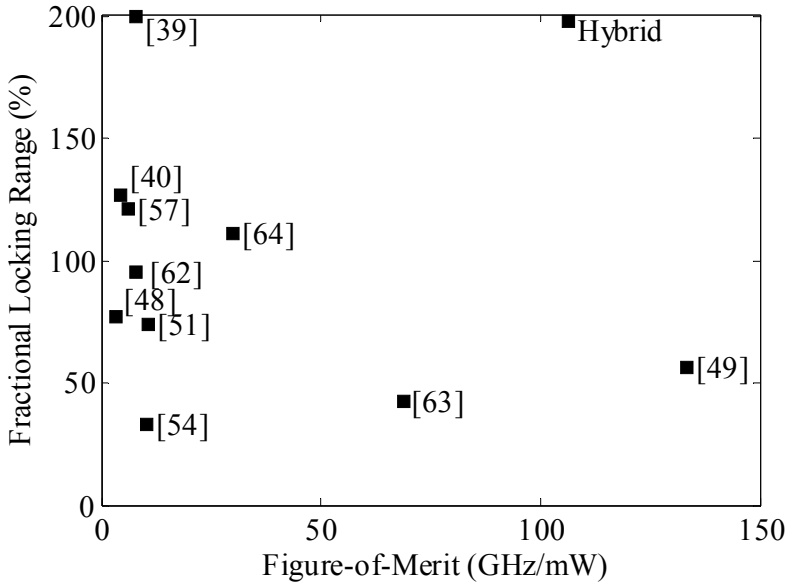


Fig. 3.5. Overview of state-of-the-art prescalers along with the hybrid frequency divider.

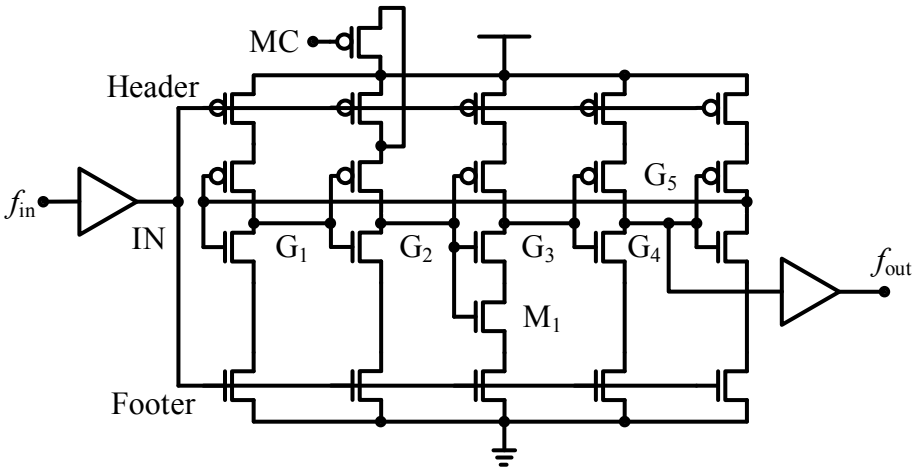


Fig. 3.6. Topology of the divide-by-4/5 hybrid frequency divider for this work.

locking range and minimizing power consumption. In this work, the divider topology is further exploited in this work in the sub-GHz region (MICS and ISM bands) and has been built to operate in a digital mode which maximizes the locking range. The digital operating principle also facilitates use of minimum size transistors of available technology for sub-GHz frequency, thus reducing power consumption and increasing FOM. Also, a simple and flexible multi-modulus feature can be introduced.

Detailed description of operation, analysis and measured performances of the hybrid dual-modulus divider developed in this work are discussed in the following sub-sections.

3.3.1 Architecture and Operation

The divider is based on a 5-stage single-ended ring oscillator. Each stage in the ring is a dynamic CMOS inverter with PMOS header and NMOS footer. The key factor in the operation of the developed divider is digitally controlled propagation of the oscillation signal through the stages of the oscillator. Thus, a single-ended ring oscillator with (2n+1) stages can be converted to a divide-by-(2n+1) divider.

The hybrid divider is designed for dual-modulus operation by introducing an extra parallel header switch in one stage as a modulus control (MC) switch. With logic “low” applied to the MC switch, the divider operates in divide-by-4 mode.

A two-stage input buffer converts the input RF signal into a digital input IN. Another two-stage output buffer ensures rail-to-rail output signal levels.

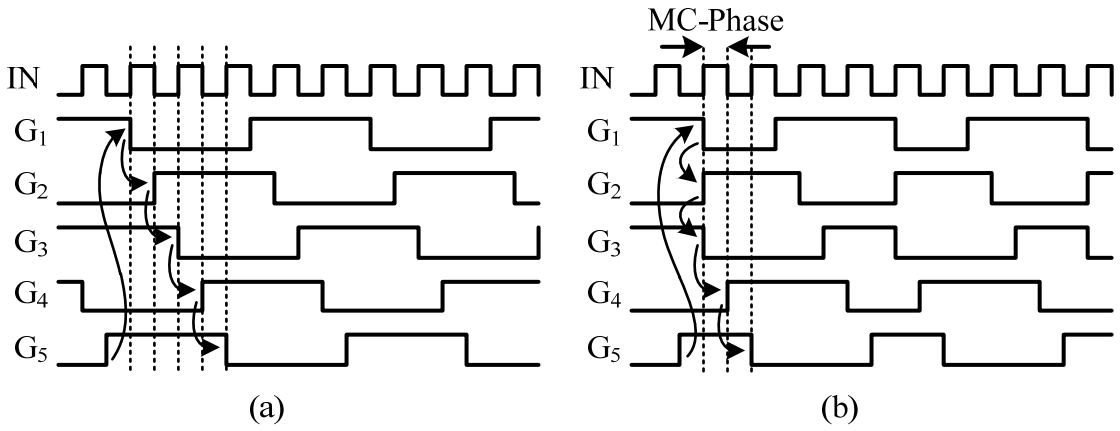


Fig. 3.7. (a) Divide-by-5 and (b) divide-by-4 operations of the designed divider. The arrows indicate propagated transitions controlled by input signal.

When the MC switch is off (MC = logic '1'), the divider operates in divide-by-5 (÷5) mode, illustrated in Fig. 3.7(a). During this mode, the transitions in the outputs of all inverter stages are controlled by IN, through corresponding headers and footers. For example, if G_1 becomes logic low, G_2 has to wait for the following "low" half-cycle of IN signal, so that the header of the second stage turns on, allowing G_2 to rise. In this way, five stages require five consecutive IN half-cycles for a transition in a G signal to propagate through the five stages. Therefore, a cycle in a G_n signal (n = 1~5) consists of five IN cycles and thus, divide-by-5 operation occurs.

The divide-by-4 (÷4) operation is illustrated in Fig. 3.7(b). The MC switch is turned on (MC = logic '0') for this mode and it shorts the header of the corresponding stage. As a result, as soon as G_1 becomes low in a "high" IN half-cycle, referred to as "Modulus-Control phase" or "MC-phase", G_2 becomes high, allowing G_3 to become low in the same IN half-cycle. In the process, an IN cycle is thus "swallowed" and a G_n cycle corresponds to four IN cycles. Thus, in

this case, the frequency divider performs a divide-by-4 operation. The divider can also be designed for lower division ratios by introducing additional MC switches to other stages.

The structure can also be designed to be multi-modulus by adding more MC switches across the header devices. Minimum size available in the target technology is chosen for PMOS and NMOS devices in the ring core and the header and footer switches to minimize power consumption for sub-GHz operation.

3.3.2 Mathematical Analysis for Design

For simplification of analysis, a divide-by-5 structure of the hybrid divider will be considered where the MC switch and NMOS M_1 (Fig. 3.6) are omitted.

3.3.2.1 Minimum Locking Frequency

The minimum locking frequency is limited by the sub-threshold leakage current in MOS devices. This limitation applies to all stages. Since NMOSs are stronger than equally-sized PMOSs, this problem is more significant when a G_n signal is high, as shown in Fig. 3.8.

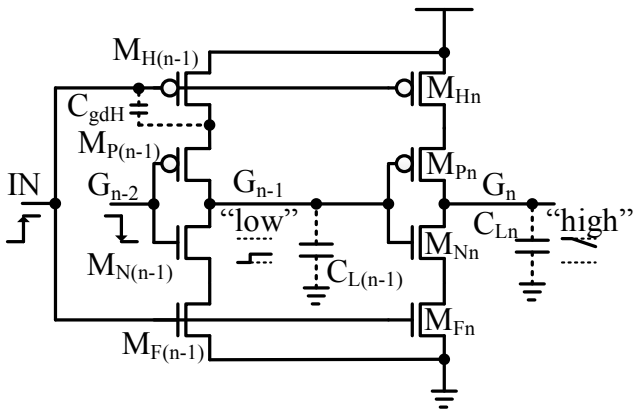


Fig. 3.8. Two stages of the ring structure of the proposed divider showing the situation where sub-threshold leakage limits the low frequency operation.

Here G_{n-1} and G_n are settled low and high respectively in previous IN half-cycles. At the positive edge of IN, the headers, M_H, turn off and the footers, M_F, turn on. $M_{P(n-1)}$ enters saturation mode due to G_{n-2} becoming "low". M_{Nn}, instead of staying completely off, enters weak inversion mode as the positive edge of IN couples to G_{n-1} through C_{gdH} and $M_{P(n-1)}$ and raises it to some extent. As a result, if the positive IN half-cycle is wide enough, charge stored in C_{Ln} leaks though the NMOSs and given enough time, logic "high" G_n ramps down below the threshold voltage of $M_{P(n+1)}$ causing an early trigger to the next ring-stage. Given all the devices have W width and L length, and the raise in G_{n-1} will be

$$\Delta V_{G(n-1)} = V_{DD}\left(\frac{C_{gdH}}{C_{gdH}+C_{L(n-1)}}\right). \tag{22}$$

If sub-threshold drain current of M_N for $V_{gsN} = \Delta V_{G(n-1)}$ is i_{leak}, and threshold voltage of M_P is V_{tp}, minimum locking frequency can be approximated as

$$f_{low} = \frac{i_{leak}}{2C_L\left(V_{DD}-\left|V_{tp}\right|\right)}. \tag{23}$$

It is assumed here that the G_{n-1} will retain the slightly higher than zero voltage for entire IN half-cycle, whereas in reality $V_{G(n-1)}$ ramps down as the coupled charge leaks through "off" $M_{N(n-1)}$ and "on" $M_{F(n-1)}$. As a result i_{leak} slowly reduces and thus lowers f_{low}.

For minimum-sized devices in 90 nm CMOS process with 2.8 nm oxide thickness, $\Delta V_{G(n-1)}$ is approximately 0.14 V using (22), for which i_{leak} is found to be about 5 nA through simulation. With $|V_{tp}|$ for minimum-sized PMOS as 0.46 V, f_{low} is approximated to be 15.43 MHz using (23). With minimum-sized devices, wiring capacitance becomes comparable to gate capacitance,

increasing C_L, reducing $\Delta V_{G(n-1)}$, and thus lowering f_{low}. Post-layout simulation at typical process corner and room temperature predicts f_{low} to be about 5 MHz.

Introducing the MC switch for divide-by-4 operation worsens this situation as the larger PMOS MC switch adds more diffusion capacitance to C_{gdH} in the 2nd stage. As a result, ΔV_{G2} is further increased, increasing i_{leak} in the 3rd stage and raising f_{low}. To prevent this, an extra minimum-sized NMOS is added in series with M_N in the 3rd stage (M_1 in Fig. 3.6). It is to be noted that adding the extra NMOS increases the edge times of this stage limiting high-frequency operation. Therefore, it can be omitted if low frequency or high temperature operation is not a priority.

3.3.2.2 Maximum Locking Frequency

The limiting factor in high-frequency operation is that each half-cycle of IN must have enough room to accommodate the rising or falling edge of corresponding G_n signal, along with its own edge-time. In the hybrid divider, the rising edges of the ring stages will be slower than falling edges because the PMOSs have the same minimum size as the NMOSs. Also, the stage driving the output buffers, G_4, will be the slowest because of additional capacitive load from the output buffer. Hence, the rising edge of G_4, t_{rise}, and falling edge of IN, t_{fall}, to enable it will determine the maximum input frequency, f_{high}, which in divide-by-5 mode is given as

$$f_{high} = \frac{1}{2\left(t_{fall} + t_{rise}\right)}. \tag{24}$$

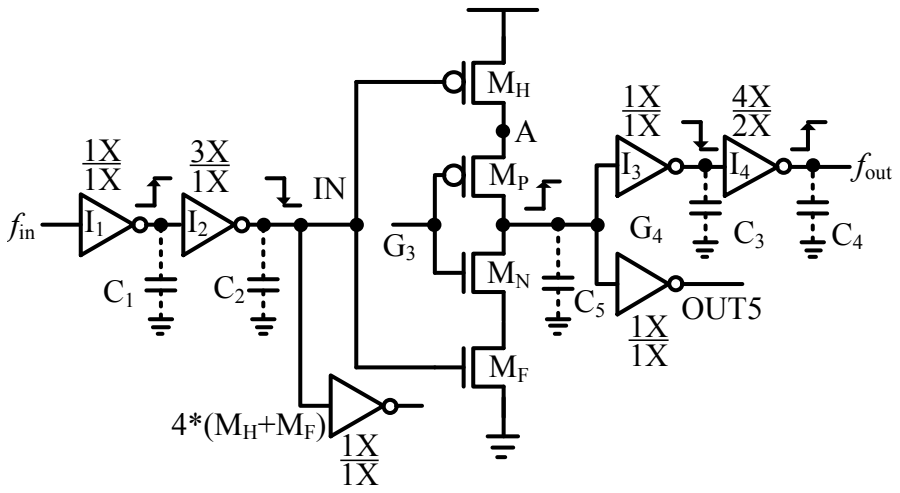


Fig. 3.9. Critical portion of divider for maximum locking frequency and phase noise estimation.

The edge-times, t_{rise} and t_{fall}, can be approximated using path effort. Fig. 3.9 shows a simplified diagram of the input signal path for maximum locking frequency estimation. Minimum-sized devices are represented as "1X". Defining the 0-70% edge-time of a unit-sized inverter (both PMOS and NMOS as "1X") driving an identical inverter as τ, the edge-time, t, of a gate can be described as [59]

$$t = (gh + p)\tau. \tag{25}$$

Here logical effort, g, is the ratio of input capacitance of the gate to input capacitance of an inverter with equal current-drive. Electrical effort, h, is the ratio of load capacitance and input capacitance. Parasitic delay, p, is the delay of the gate driving no load, caused by drain capacitances at output. τ can be found through simulation.

Using (25), the falling edge-time of IN, t_{fall}, is estimated from the effort of the second stage of input buffer to be 60 ps. Since the rising-edge of G_4 is triggered by IN, t_{rise} can be estimated by considering the PMOS side of this ring-stage as a 2-input NOR gate and calculating its effort being

driven by IN. Thus, t_{rise} is calculated to be 121ps. Using these values of t_{rise} and t_{fall} in (24), f_{high} is calculated to be approximately 2.8 GHz. By neglecting overlap in the edges of adjacent stages, (24) yields a conservative estimate of the maximum locking frequency. Also with minimum-sized devices, parasitic capacitors become comparable to gate capacitance, increasing edge-times and reducing f_{high} to an estimated 1.5 GHz based on post-layout simulations at typical process corner and room temperature.

For divide-by-4 mode, a PMOS is used as the MC switch so that the MC phase consists of two falling edges and one rising edge of the G_n signals, since falling edges are faster. This PMOS is chosen to be 300 nm wide to provide a sharper rising edge in MC phase. Also, the input buffer is skewed so that IN has more than 50% duty cycle to easily accommodate the three transitions. Maximum locking frequency in this mode will be lower than that of divide-by-5 mode, because minimum IN half-cycle width is limited to accommodate these three G_n transitions instead of just one.

3.3.2.3 Phase Noise

The base phase noise of the divider can be conveniently derived by calculating the jitter or time variations in threshold-crossings of the divider signals and then relating it to the spectrum. For time jitter due to thermal noise $\sigma_{t,W}^2$, phase noise at output frequency f_{out}, can be described as [60]

$$L_W = 4\pi^2 f_{out} \sigma_{t,W}^2 .$$

As G_4 drives the output buffers, only jitter from this stage, along with the input and output buffers, needs to be calculated to estimate the phase noise of the divider. Jitter in the other G_n signals can be disregarded as they are already settled when G_4 transitions.

Fig. 3.9 shows the portion of the divide-by-5 structure of the proposed divider that contributes jitter to the divider output. As the thermal noises in these stages are independent, jitter contributions from them can be separately calculated and summed together. Time jitter from inverters I_1 through I_4 is described as [61]

$$\sigma_t^2 = \left(\frac{1}{I_D^2}\right)\cdot\left(\frac{\overline{i_n^2}}{\Delta f}\right)\cdot\left(\frac{T_d}{2}\right). \tag{26}$$

Here, T_d is the propagation delay, I_D the drain current and $\overline{i_n^2}/\Delta f$ the thermal drain current noise of the conducting MOS. For short-channel devices, these are given by the following equations, where symbols convey their conventional meanings.

$$I_D = WC_{ox}v_{sat}(V_{GS} - V_t) \tag{27}$$

$$\frac{\overline{i_n^2}}{\Delta f} = 4kT\gamma\mu C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_t) \tag{28}$$

$$T_d = \frac{0.52C_L V_{DD}}{I_D} \tag{29}$$

Calculation of jitter from the ring-stage requires understanding of the triggering mechanism of this stage. For example, in case of rising edge in G_4, G_3 is already settled as "low" in previous half-cycle of IN, and M_P is ready to turn on. As soon as the falling edge of IN appears, M_H turns on and M_P enters saturation mode, pushing node A to ($|V_{tp}|+|V_{ov}|$) where gate overdrive, $|V_{ov}|$, is about 250 mV. This pushes M_H into linear region. It can be assumed that M_P stays in the saturation mode for the duration of propagation delay. In this case, jitter contribution of this ring stage will be the summation of jitter from two independent noise sources, thermal drain current noise of M_P and thermal voltage noise of the equivalent resistance of M_H, band-limited by the pole at the stage

output. Jitter from the first component is computed using (26) through (29) and jitter from the second component is expressed as

$$\sigma_t^2 = \frac{kTC_5\gamma}{I_D^2}. \tag{30}$$

It can be seen from (26) that jitter contribution of any stage increases with its edge time and decreases with drain current. Therefore, the ring-stage in Fig. 3.9 is the major contributor in output jitter due to its lower drain current compared to the buffers, and the resulting larger edge-time. The thermal noise from the header and footer also adds to this contribution.

For the proposed divider, phase noise in the white-noise region is calculated to be -152.3 dBc/Hz, using the above equations. Pre-layout simulation predicts this to be -150 dBc/Hz. A γ of 2.5 [23] is used in these equations. The process parameters are taken from the foundry-provided models. Wiring capacitances, which will be significant compared to minimum-size devices, will add to C_L and C_5 in (29) and (30) to increase jitter. It is assumed in (27) that the corresponding devices are saturated along the full transition times. Crowbar currents and currents required by diffusion capacitance of corresponding driver stage are also not considered in this calculation. These assumptions will result in optimistic results in (29) and (30). Post-layout simulation in typical process corner shows -145 dBc/Hz phase noise at the white-noise region, after a corner at around 1 MHz.

3.3.2.4 Power Consumption

Power consumption of the proposed divider can be estimated as $P = fC_L V_{DD}^2$, where C_L represents the total gate capacitance in the circuit. For the divide-by-5 structure, power consumption is to be estimated for the input buffer driving the headers and footers at the input

frequency and the core ring oscillator and the output buffer running at output frequency. Thus, power consumption for the divide-by-5 structure can be approximated to be 1.27 μW, which corresponds well with pre-layout simulation of the dual-modulus structure (1.63 μW). Additional power will be consumed due to diffusion and wiring capacitances and crowbar currents. Post-layout simulations indicate power consumption at 400 MHz of 3.16 μW and 3.39 μW in divide-by-5 and divide-by-4 modes, respectively.

It is to be noted that about 67-70% of this power is consumed by the 2-stage input buffer driving the header and footer devices at full input frequency, as predicted by simulation. The total number of these devices is 10 in a ÷5 structure of this topology. This will reduce to 6 minimum-sized devices in a sub-GHz ÷3 structure, which represents less capacitive load for RF compared to a ÷3 TSPC divider (8 devices). This results in lower power consumption in the hybrid structure.

3.3.3 Measured Performance

The divide-by-4/5 hybrid divider was implemented in a 90 nm CMOS process for testing. Fig. 3.10 shows the microphotograph of the fabricated divider which occupies only 4.5×10 μm^2 area. A 16×90 μm^2 area buffer is used to drive external 50 Ω load. To avoid the parasitic effects from packaging, chip-on-board bonding was used. The input test signal is generated with Anritsu MG3693C signal generator and output is measured with Agilent N9010A EXA signal analyzer. Fig. 3.11 shows the output spectrum centered at 80 MHz when the divider is locked to 400 MHz input frequency at ÷5 operation. The locking range is measured as 6 MHz-1.5 GHz and 4 MHz-1.3 GHz in ÷5 and ÷4 modes, respectively. Thus, a 198% dual-modulus locking range is achieved covering MICS band and 433 and 915 MHz ISM bands.

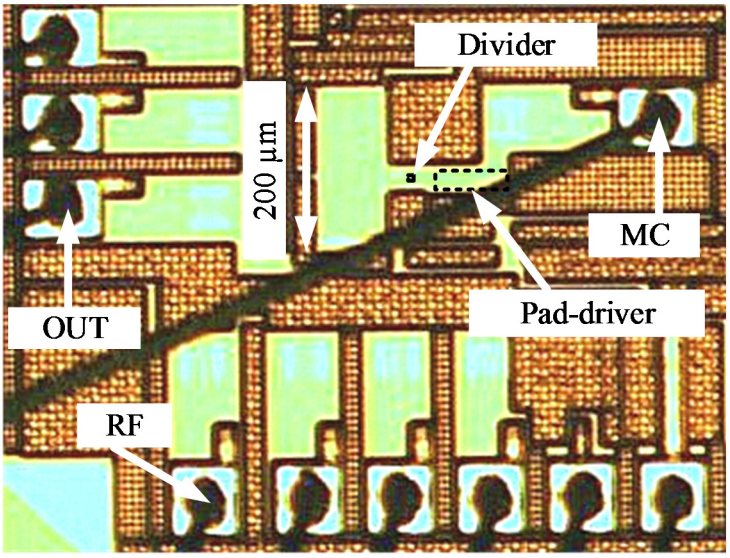


Fig. 3.10. Microphotograph of the fabricated dual-modulus divider.

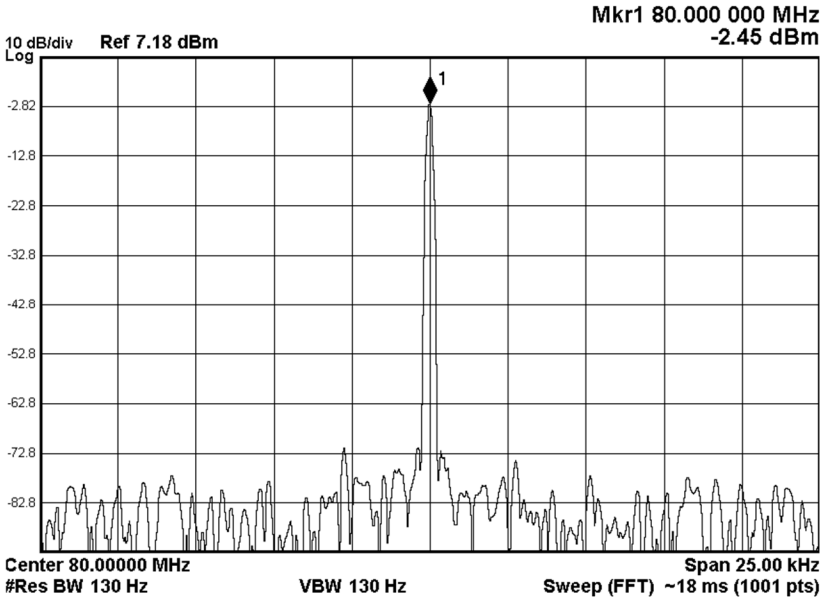


Fig. 3.11. Output spectrum of the divider at ÷5 mode locked by 400 MHz input frequency.

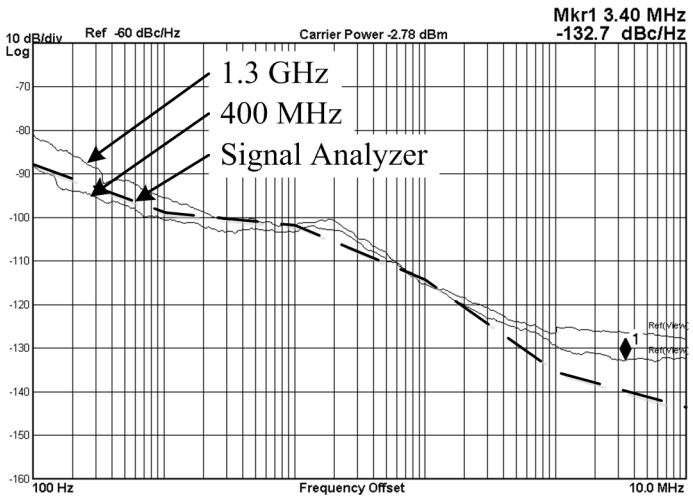


Fig. 3.12. Phase noise spectra of divider output in ÷4 mode, locked by 1.3 GHz and 400 MHz input frequencies. The dashed curve shows the base phase noise of the signal analyzer.

Fig. 3.12 shows the phase noise plots of the divider in ÷4 mode, locked at 400 MHz and 1.3 GHz input frequencies. The phase noise corner is at 1 MHz. Phase noise in flicker-noise region is dominated by the signal analyzer, as indicated by the dashed line. However, phase noise from the divider can be measured in the white-noise region to be -133.3 dBc/Hz for 400 MHz input frequency. Phase noise increases as the input frequency approaches the maximum locking range because the time for ring-stage G_4 to settle reduces and the other stages also start to contribute their own jitter to the output.

Phase noise spectrum near the minimum locking frequency coincides with that of 400 MHz. Stepping out of the locking range, the ring-stages starts to miss-trigger and phase noise dramatically increases. The minimum and maximum locking frequencies were determined by finding the extreme frequencies at which no significant carrier-frequency deviation (>1 Hz) or phase noise aberrations were observed over a span of 10 minutes.

With 400 MHz input frequency, the divider, along with the two-stage buffers consumes only 3.76 μW and 4.07 μW power at divide-by-5 and divide-by-4 modes respectively from a 1 V supply. Thus, this work achieves a high figure-of-merit of 98.2 GHz/mW in divide-by-4 mode.

Because of the digital mode of the divider's operation, the two-stage digital input buffer is needed to convert the input RF signal to a rail-to-rail square wave. Thus, it is more important to observe the amplitude than power of the input RF signal driving the gate capacitance of the first-stage inverter. At 400 MHz, divide-by-4 mode, a sinusoidal wave with minimum 178 mVpp amplitude is required so the buffer can convert it to a digital signal with fast enough edges for the headers and footers. As input frequency increases, required minimum amplitude increases to ensure fast edges to be accommodated in input half-cycles. At 1 GHz, a sinusoid with at least 796 mVpp is required for locking.

Fig. 3.13 shows the power consumption of the proposed divider across its locking range and provides comparison with existing works in this regard. A more detailed comparison is also provided in Table 3.1. The proposed divider, due to its ILFD-like structure, consumes much less power than most existing dividers. While growing interest in wireless medical applications has spurred recent works in low-power sub-GHz dividers [49] [64], the majority of published dividers have focused on higher input frequencies, with larger transistors and correspondingly lower FOM. Among the sub-GHz frequency dividers, [49] achieves a better FOM than this work, but with less fractional locking range. This work achieves a much larger fractional locking range by taking advantage of its digital control. Unlike most previous low-power dividers, this work also features dual-modulus operation.

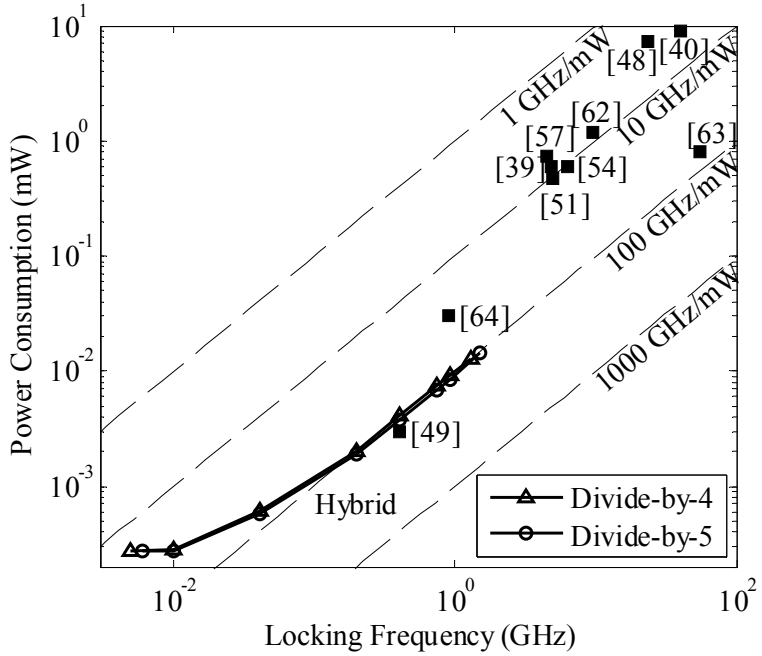


Fig. 3.13. Power consumption of the dual-modulus hybrid divider across locking range and a comparative overview with the state-of-the-art.

Table 3.1 Performance comparison with the state-of-the-art.

Works	Topology	Process (nm)	Division Ratio	Power (mW)	Locking Range		FoM (GHz/mW)
					GHz	%	
[40]	CML	(SiGe) 180	2	9	10 - 45	127.3	4.4
[39]	TSPC	180	2/3	(/2) 0.6	Max. 4.9*	200.0	8.0
[62]	TSPC	130	2/3	(/2) 1.2	(/2) 5 - 14.1	95.3	7.9
[63]	LC-ILFD	90	2	0.8	35.7 - 54.9	42.4	68.8
[49]	Ring-ILFD	90	5	0.003	0.37 - 0.66	56.3	133.3
[57]	Ring-ILFD	180	3	0.74	1.2 - 4.9	121.3	6.8
[48]	CML+LC-ILFD	130	4	7.3	13.5 - 30.5	77.3	3.2
[51]	Ring-ILFD	130	2/3/4/5/6	0.47	(/2) 2.56 - 5.56	73.9	10.6
[54]	Ring-ILFD	40	2&3	0.6	4.5 - 6.3	33.3	10.5
[64]	Relax.-ILFD	90	3	0.03	0.4 - 1.4	111.1	30
This work	Hybrid	90	4	0.00407	0.004 - 1.3	198.8	98.3
			5	0.00376	0.006 - 1.5	198.4	106.4

* Minimum locking frequency not mentioned; fractional locking range is assumed to be 200%.

Chapter 4 Power Amplifier

The power amplifier (PA) is another major power-consuming block in a transmitter. Fig. 4.1 shows the general power amplifier model [65]. The global efficiency of a high-output-power transmitter, which is defined as the ratio of transmitted power to total transmitter power consumption, is often dominated by the drain efficiency of the PA. Drain efficiency of a PA is defined as the ratio of output power to the DC power consumption of the PA. For example, in [18], a 2.35 mW PA with 0 dBm output shows 42.5% drain efficiency and after adding the 300 μW pre-PA power to it, the global efficiency is 37.7%. For applications where output power is very low, PA power is still one of the major components of total power consumption. The 189 μW PA in the 400 μW MICS band transmitter in [4] is an example where the PA here is only 13% efficient. Substantial research has been conducted on improving the efficiency of RF power amplifiers.

4.1 Classes of Power Amplifiers

There are many different classes of power amplifiers that have been developed in order to improve their efficiency. These classes can be developed in two main categories – linear power amplifiers and switching power amplifiers.

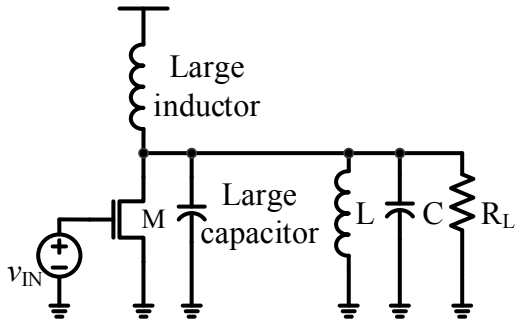


Fig. 4.1. General power amplifier model.

4.1.1 Linear Power Amplifiers

Linear classes of power amplifiers are classes A, AB, B and C, depending on how the transistor M in Fig. 4.1 is biased. Fig. 4.2 shows different biasing conditions of these classes.

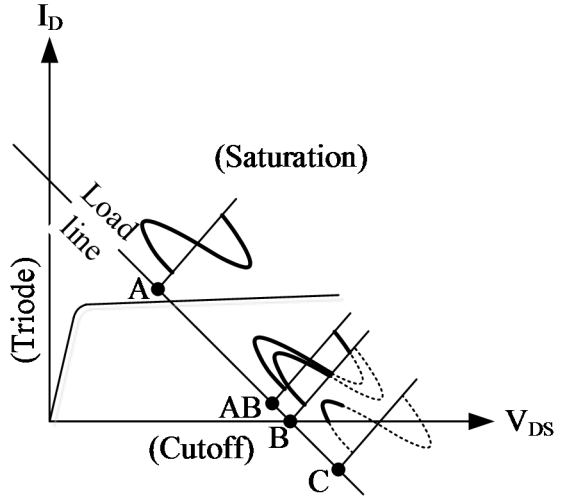


Fig. 4.2. Bias points of Class A, AB, B and C power amplifiers.

The Class A PA is basically a standard small-signal amplifier configured as power amplifier. In this case the MOS transistor is biased so that it operates linearly. This condition is satisfied by avoiding cutoff and triode modes and the quiescent point is settled in the middle of I_D-V_{DS} load line. This class of PA is the most linear. On the other hand, since the transistor is conducting quiescent current through the full RF cycle, efficiency is very low. Theoretically, Class A PAs can reach highest 50% efficiency [65].

Classes AB, B and C PAs are variations where the biasing condition is such that the transistor conducts the quiescent current during a portion of the RF cycle. In Class B PA, the transistor is turned on for one RF halfcycle. As a result, less DC power is dissipated, increasing

the efficiency. Theoretically a Class B PA's efficiency can be maximum 78.5%. On the other hand, because of reduced conduction time, the amplifier is not linear anymore. The gain is also reduced. Class AB is a compromise of linearity and efficiency between Classes A and B, where conduction cycle is more than half a cycle. A commonly used configuration of Class B PA is the push-pull configuration where, a PMOS and a NMOS are turned on alternatively through halfcycles.

In Class C, the PA transistor conducts quiescent current for less than half RF cycle. As a result, Class C PAs can theoretically reach efficiency over 90%. The disadvantage of Class C PA is much reduced linearity and gain.

Because of their high efficiency, Classes B and C are very popular for low-power transmitter design. Also, it is possible to achieve small circuit area with these classes employing simple impedance matching networks which allows easy integration. However, for very low-power outputs, quiescent power and power consumed by the driver stages becomes significant and reduce the efficiency. For example, in [66], a 868/915 MHz transceiver is reported with a Class AB amplifier which delivers maximum -4 dBm output power with 47.6% efficiency. This efficiency is reduced to 32.4% when the power consumed by the driving inverter stages are included. Another Class B PA, used in a 2.4 GHz transmitter in [67], achieves only about 11% efficiency at -11 dBm output power. Both these PAs use on-chip matching networks. The Class C PA in the aforementioned MICS transceiver in [4] uses simple off-chip matching network and achieves 13% efficiency.

4.1.2 Switching Power Amplifiers

In switching power amplifiers, the transistors are used more as switches than active current control devices. An ideal switch either has zero voltage across (on) or zero current through (off) itself. As a result, an ideal switch always has zero V-I product or dissipates zero power. This concept in used in switching PAs. Most known classes in this category are classes D, E and F. Fig. 4.3 shows the schematic of a voltage-mode Class D (VMCD) PA used in a 915 MHz transmitter reported in [68].

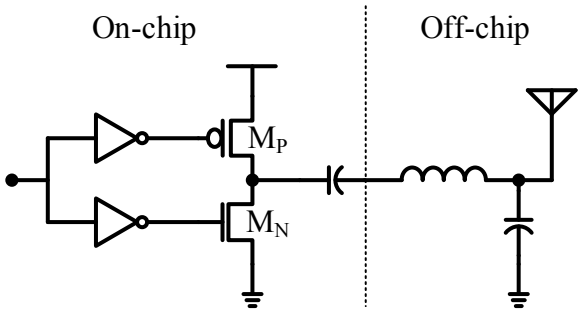


Fig. 4.3. A voltage-mode Class D power amplifier [68].

Class D amplifier structure is similar to the push-pull Class B PA. But in this case the CMOS devices are driven hard enough to make them act like switches with fast-edge signals, thus reducing DC power consumption. This results in very high drain efficiency. However, Class D PAs suffer from losses due to the non-ideal switching behavior of MOS devices. The VMCD PA in [68] shows near 60% efficiency at 6 dBm output power.

Classes E and F amplifiers are more efficient PAs than Class D. Here a complex, high order reactive network is used to shape the voltage waveform in order to have zero value and zero slope at switch turn on, thus reducing switch losses [65].

However, these switching PAs require full scale rail-to-rail operation for maximum power efficiency and thus require drive-stages that usually consume significant power. As a result, although these PAs are popular for applications with high output power, they become impractical for medical applications and other low-power wireless sensors. An added disadvantage of Classes E and beyond is their need for complex matching circuits with extra inductors which makes integration difficult.

4.2 Low-Power Power Amplifier

As discussed in the previous section, at low output power levels, typical of short-haul wireless sensors, simple PA design and operation is desirable to reduce power consumption of driver circuits and use small matching networks. Therefore, Classes B and C are promising in this area as evidenced by their popularity in recent transmitter works [66] [67] [4] [11] [69]. Since these amplifiers need sinusoidal input, they can be directly connected with the VCO, eliminating the necessity of power consuming driver circuits. This acts as a great advantage for transmitters using unlocked DCO or injection-locked or resonator-based VCOs. A form of Class D amplifier is also reported in a low-output-power transceiver in [70]. This PA is basically an output buffer consisting of four cascaded tapered inverter stages. The stages are enabled and disabled to transmit "on-off keying" (OOK) modulated carrier.

In this work, a similar approach is taken for a simple Class D low-power PA. The generated carrier in this work is already digitized at the output of the GB-LC VCO in order to be compatible with the rail-to-rail operation of the hybrid prescaler. This eliminates the need of drive-stages typical to Class D PAs in this work. The proposed PA starts with a small two-stage input buffer after which the digitized carrier signal drives four identical inverter stages in parallel. The PA

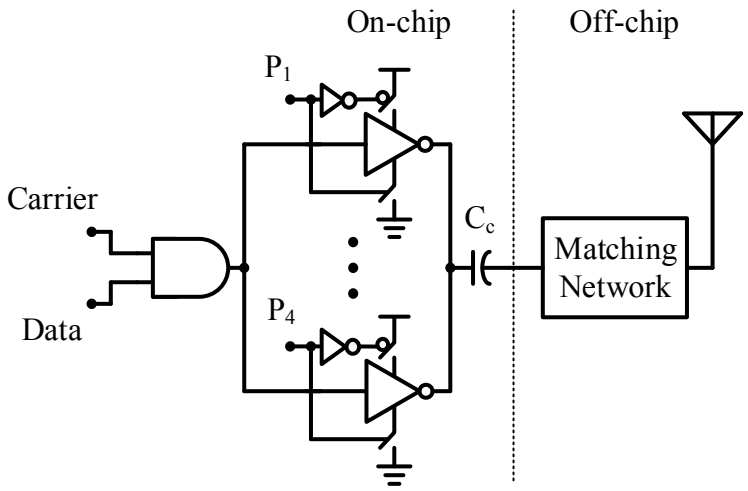


Fig. 4.4. Schematic of low-power power amplifier with OOK modulation, used in this work.

stages are designed with small devices to reduce the load capacitance for the input buffer. As a result, each PA stage has a large output resistance, in the range of 4 kΩ. A matching network transforms the 50 Ω load from an antenna to high impedance load, in the range of 2~3 kΩ, to be driven by the PA at low power. A coupling capacitor, Cc, prevents the network from disrupting the DC bias of the inverter. Output power can be varied by turning the stages on or off individually or together. The schematic of this inverter-based PA is shown in Fig. 4.4.

The digital structure of the PA also allows easy integration of an additional on-off keying (OOK) modulation system. To enable OOK modulation, the carrier is ANDed to the baseband data in the input buffer.

4.2.1 Matching Network Calculation

The matching network in this PA design is implemented off-chip using high-Q components. Using the design guidelines in [65], a tapped-capacitor or Pi network can be designed to transform a load R_L to a real high impedance R_{in}.

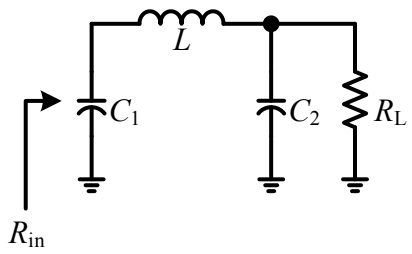


Fig. 4.5. Pi network for impedance transformation.

Fig. 4.5 shows an impedance transforming network in Pi configuration. The following equations are used to derive the L, C_1 and C_2 parameters for specific values of R_L, R_{in} at certain center frequency f_0 and desired bandwidth Δf or network quality factor Q.

$$Q_{\text{initial}} = \frac{f_0}{\Delta f} \tag{31}$$

$$R_I = \frac{\left(\sqrt{R_{in}} + \sqrt{R_L}\right)^2}{Q_{initial}} \tag{32}$$

$$Q_{new} = \sqrt{\frac{R_{in}}{R_I} - 1} + \sqrt{\frac{R_L}{R_I} - 1} \tag{33}$$

$$L = \frac{Q_{new} R_I}{2\pi f_0} \tag{34}$$

$$C_1 = \frac{1}{2\pi f_0 R_{in}} \cdot \sqrt{\frac{R_{in}}{R_I} - 1} \tag{35}$$

$$C_1 = \frac{1}{2\pi f_0 R_L} \cdot \sqrt{\frac{R_L}{R_I} - 1} \tag{36}$$

Using these equations, it can be calculated that a $R_L = 50\ \Omega$ can be transformed to $R_{in} = 2.45\ \text{k}\Omega$ at $f_0 = 915$ MHz with 45 MHz network bandwidth using a Pi network with

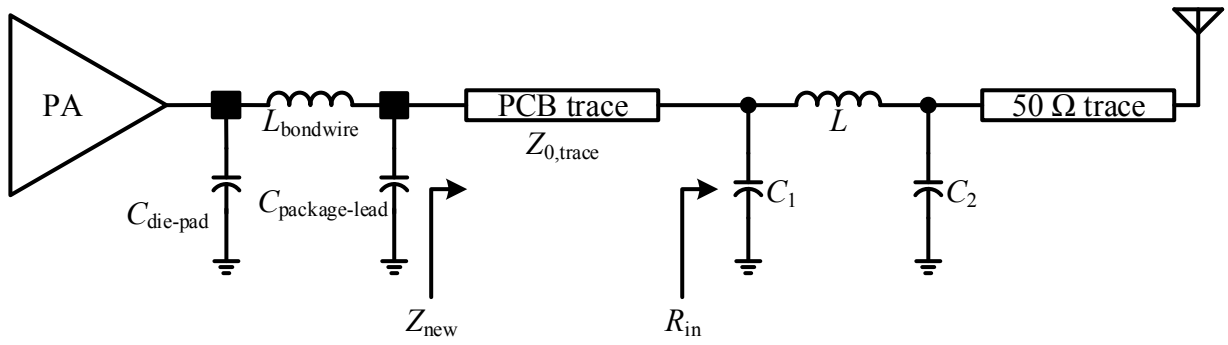


Fig. 4.6. PA output matching network with non-idealities.

L = 27 nH, C_1 = 1.26 pF and C_2 = 8.13 pF. Post-layout simulation of the PA with this network (Q_L assumed to be 50) shows maximum output power of -15.79 dBm with 23.6% efficiency. Output power can be reduced by 4 levels with minimum at -25.49 dBm with 6.2% efficiency. The two-stage buffer at the PA input consumes about 16 μW power.

These calculations assume the matching network to be lossless. Furthermore, the parasitic elements like the bondwire, the printed-circuit-board (PCB) traces also need to be considered. Including these non-idealities, the entire network can be approximated to a circuit as shown in Fig. 4.6. The parasitic components such as bondwire inductance (1 nH for 1 mm bondwire) or capacitances from package lead or die pad (~100 fF) have little effect in sub-GHz frequencies, as in this work. Therefore, they can be ignored. However, for an off-chip matching network with very high transformation ratio as described above, the PCB trace between the PA and Pi network can create significant problems. It can be shown using any easily available microwave impedance calculator tool that it is impossible to achieve a trace characteristic impedance in the order of kΩ at 915 MHz. For example, for a 62 mil thick FR4 PCB, a trace with only 5 mils width and 1.4 mil thickness will have characteristic impedance, $Z_{0,trace}$, of only about 150 Ω. As a result, this trace

transforms the aforementioned R_{in} to a low complex impedance. The new transformed impedance is expressed by [71]

$$Z_{new} = Z_{0,trace} \cdot \frac{R_{in} + jZ_{0,trace} \tan \beta l}{Z_{0,trace} + jR_{in} \tan \beta l}. \tag{37}$$

Here l is the trace length and $\beta = \frac{2\pi}{\lambda}$ with λ as the wavelength of signal. As l approaches zero, Z_{new} approaches R_{in}. Therefore, for the matching network to be effective, it is of crucial importance that this trace is very short and very narrow. With simulations using ADS software and its Optimization tool, it can be shown that the previously discussed transformation from 50 Ω to 2.5 kΩ at PA output can still be achieved with L = 27 nH, C_1 = 1.2 pF and C_2 = 7.8 pF if the PCB trace is only 5 mils wide and 40 mils long (0.005λ at 915 MHz) in a 62 mil thick FR4 board. This is shown in Fig. 4.7 with the help of scattering parameters.

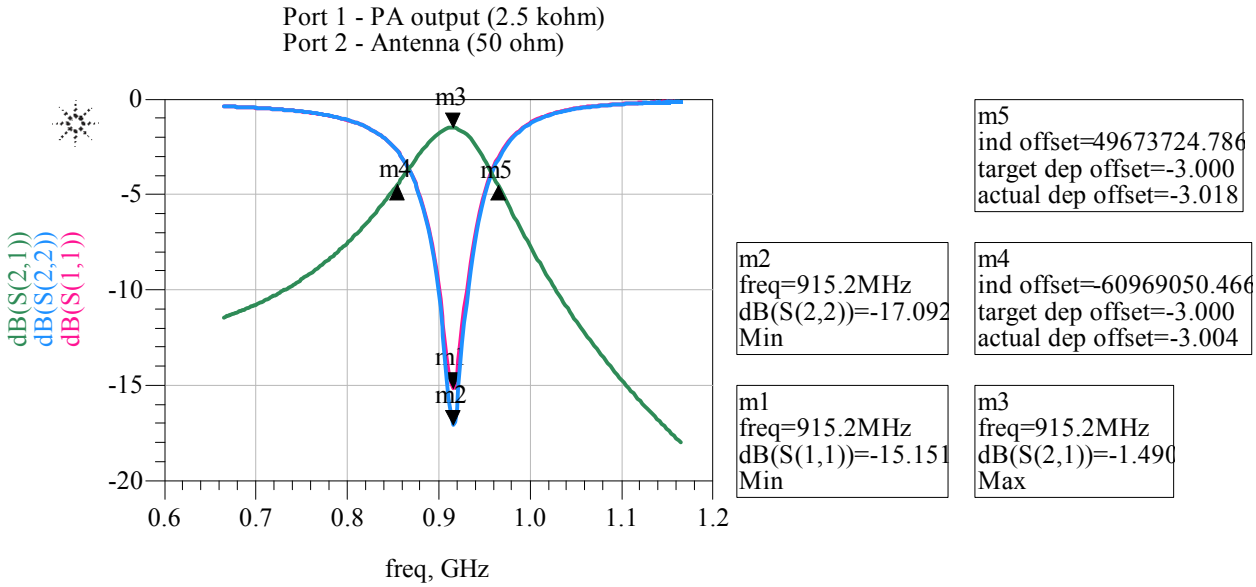


Fig. 4.7. Impedance transformation simulation with non-idealities, including short PCB trace between PA output and off-chip matching network using ADS.

The low values of s_{11} and s_{22} at center frequency in Fig. 4.7 indicate that the desired impedance transformation is achieved, including the effect of the low-impedance, very short PCB trace. With the resulting 2.5 kΩ real impedance at the PA output, the efficiency is simulated to remain same as before, around 23%.

Chapter 5 Low-Power 915 MHz Transmitter

For this work, a low-power transmitter is designed where a low-complexity 3rd order PLL with the aforementioned GB-LC VCO and hybrid prescaler is used to reduce pre-PA power consumption. Fig. 5.1 shows the structure of the transmitter.

The frequencies commonly used for wireless sensors and medical telemetry devices are –

1) MICS band (402 – 405 MHz)
2) 433 MHz ISM band (433.05 – 434.79 MHz)
3) 915 MHz ISM band (902 – 928 MHz)
4) 2.4 GHz ISM band (2.4 – 2.5 GHz)

For this work, the 915 MHz ISM band is chosen and thus, the GB-LC VCO is designed which leads to an inductor with reasonable area and sufficiently low power consumption.

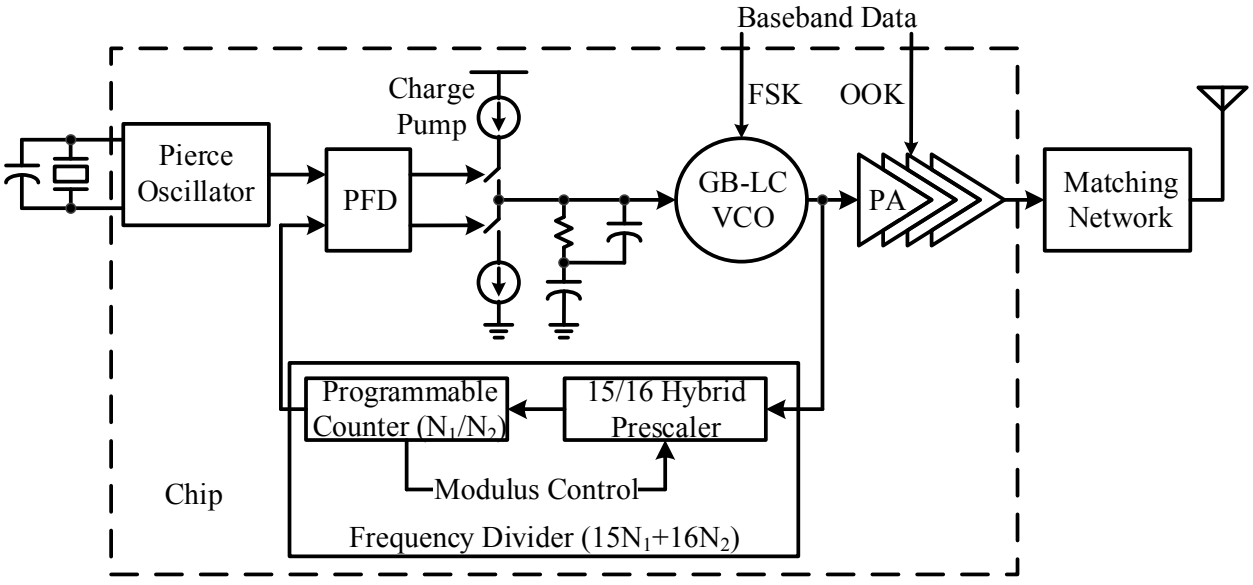


Fig. 5.1. Topology of the proposed low-power 915 MHz transmitter.

The hybrid prescaler is ported to the currently available 130 nm CMOS process, same process as for the GB-LC VCO. Post-layout simulation at the "slow-slow" process corner (worst case) on the divide-by-4/5 prescaler is used to confirm operation at 1 GHz locking frequency, well above the ISM band. A 3/4-prescaler is also cascaded to achieve divide-by-15/16 operation. At typical process corner, the 15/16-prescaler consumes 17.7 μW power, locked at 915 MHz.

Over the course of the design various improvements and modifications are performed on the 915 MHz PLL. Several blocks, such as a power amplifier, a reference frequency generator, a tunable bias circuit etc. are designed and integrated into the design. This chapter discusses the various steps taken towards realization of a fully integrated low-power ISM-band transmitter.

5.1 Preliminary 3rd-Order PLL Design

5.1.1 Loop Filter (LF) Design

It can be seen from Fig. 2.21 that the tuning curve of the VCO is very non-linear. As it is shown in Fig. 5.2, VCO tuning gain, $|K_{VCO}|$, varies by a large amount – from below 1 MHz/V to

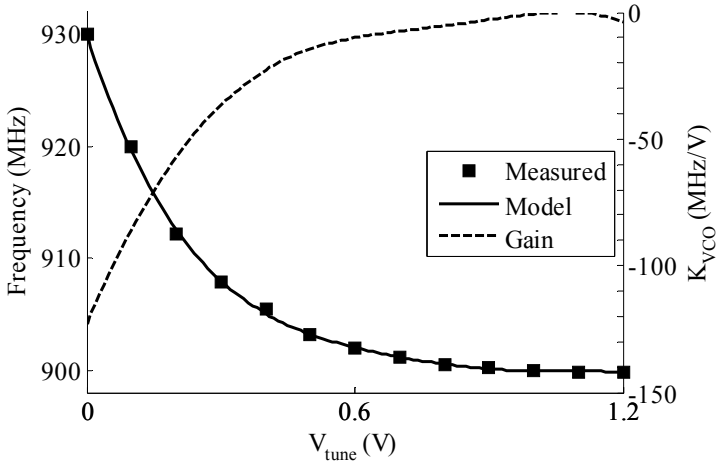


Fig. 5.2. Variation of tuning gain of the fabricated GB-LC described in Section 2.5.3.

over 100 MHz/V. The tuning curve becomes almost flat as V_{tune} reaches the supply voltage, which limits the usable tuning voltage range. The major challenge that arises from this nonlinearity is to maintain PLL stability over the range of K_{VCO} variation. That is why careful loop filter design is required.

The design guidelines in [72] are followed for this PLL. Bode plot is a simple way to analyze the stability of the PLL. The open loop transfer function of the 3rd order PLL, shown in Fig. 5.2, is given by

$$G(s) = \frac{K_P K_{VCO}}{s^2 C_1 N} \cdot \frac{1 + sT_2}{1 + sT_3}.$$

Here, K_P is the gain from PFD-CP blocks and is expressed as $K_P = I_{CP}/2\pi$, I_{CP} being the charge-pump current. The zero and the pole from ω_2 and ω_3 are given by $\omega_2 = 1/T_2 = 1/R_2(C_1 + C_3)$ and $\omega_2 = 1/T_3 = 1/R_2 C_3$, respectively. If ω_2 is chosen to coincide with the transition frequency, ω_T, the Bode plot should be as shown in Fig. 5.3, with the phase margin (PM) determined at ω_2.

Keeping in mind the wide range of K_{VCO} variation, values of R_2, C_1 and C_3 is chosen such that –

- $\omega_3 = 10\omega_2$
- $\omega_2 = \omega_T$, for minimum value of K_{VCO} under consideration) and
- reasonable phase margin for stability, for example 40º, is achieved.

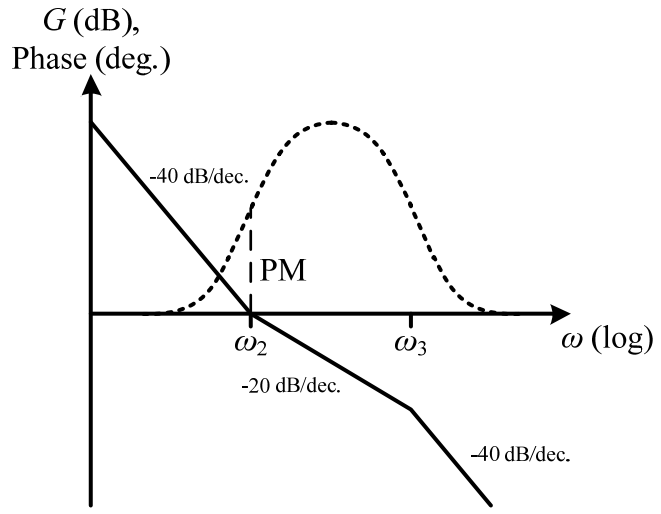


Fig. 5.3. Bode plot of open-loop gain of the 3rd order PLL in Fig. 5.1.

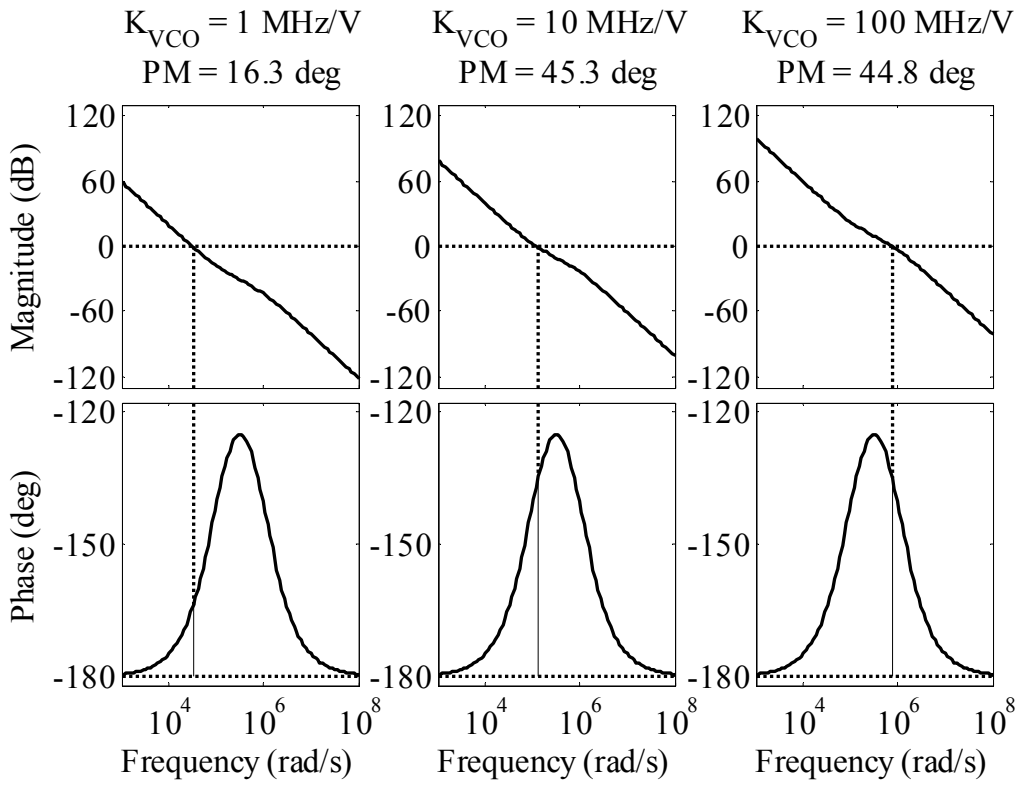


Fig. 5.4. Variation in phase margin of PLL due to variation of VCO gain.

Now, if $|K_{VCO}|$ varies by one order of magnitude, for example 10 MHz/V to 100 MHz/V, G(dB) curve in Fig. 5.3 will move up by 20 dB and ω_T will shift to ω_3, with higher than 40º phase margin achieved over the range of K_{VCO} variation (Fig. 5.4). Thus, loop stability for an order of magnitude variation of K_{VCO} can be achieved. Care is taken in the loop filter design such that some positive phase margin remains as K_{VCO} decreases below 10 MHz/V. It is to be noted that the loop bandwidth also decreases with K_{VCO} and less close-in phase noise from VCO will be suppressed.

5.1.2 Tuning Limiter

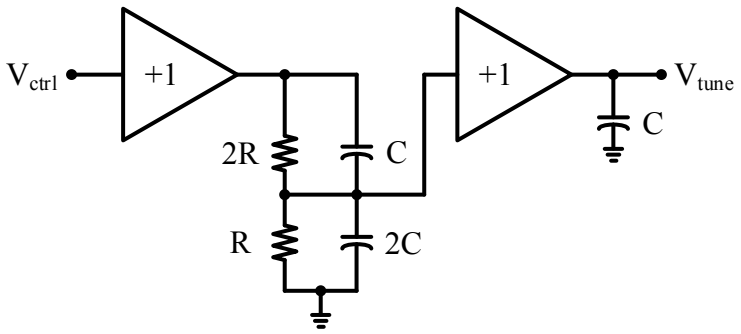


Fig. 5.5. The structure of the tuning limiter block introduced between the LF and the VCO in the PLL.

It is clear from Fig. 5.2 and Fig. 5.4, when V_{tune} nears the supply voltage, K_{VCO} is much reduced (below 1 MHz/V) which lowers the phase margin to almost zero, risking oscillation. To avoid this, it is desired to limit V_{tune} below 0.4 V where K_{VCO} varies by less than one order of magnitude. To perform this, the PLL architecture is modified with a limiter block introduced between the LF and the VCO. The structure of this block is shown in Fig. 5.5. The first stage is a high-input-impedance, low-input-capacitance unity gain buffer that supports rail-to-rail input and consists of two operational transconductance amplifiers (OTA) with NMOS and PMOS input pairs.

The resistive divider scales down V_{ctrl} from LF to V_{tune} for VCO by 1/3, i.e. 0~0.4 V. Also because of the scaling down, K_{VCO} variation, as seen by the PLL, is further reduced and tuning becomes more linear. The limiter block is designed to consume only 10 μA from 1.2 V supply. The output poles from the two stages are designed to be at least 5 times higher than pole ω_3 from the LF. Also, the resistor value R should be chosen large enough to not load the first stage.

5.1.3 PLL Power Breakdown

Based on these design considerations, a PLL is designed in a 130 nm 1P8M CMOS process. To avoid large simulation time, the PLL was simulated with behavioral-level blocks before fabrication. Table 5.1 shows the power consumption breakdown of this PLL as expected from simulation and previous measurement results.

Table 5.1. Expected power consumption breakdown of the 3rd order PLL with 1 MHz frequency resolution.

Block	Status	Power consumption
GB-LC VCO	Measured	166.8 μW
Divide-by-15/16 Prescaler	Simulated	17.7 μW
PFD + Charge Pump + Programmable Counter	Simulated	17.5 μW
Tuning Limiter	Simulated	12 μW
Total pre-PA power		214 μW

5.2 Modifications and Improvements over Preliminary PLL Design

5.2.1 Modification of GB-LC Analog Tuning

As discussed in the previous section, the severe nonlinearity of the tuning range affects the PLL dynamics and a tuning limiter is required to mitigate this effect. However, this solution has some drawbacks. The V_{ctrl} is a critical node in the PLL as it directly modulates the VCO frequency. Introducing the limiter block adds thermal noise from the large resistors and device noises to this node and will result in spurs at the VCO output and therefore, needs to be optimized for noise contribution. The large resistors also consume extra die area. The OTAs used in the limiter also must be designed to have good supply-noise rejection.

To understand the reason of this nonlinearity in tuning, the C-V characteristic curve of the tuning capacitor, shown in Fig. 5.6(a), should be examined. The tuning capacitor is an NMOS (with drain-source shorted) in N-well and its capacitance reaches its maximum as the V_{GS} reaches mid-rail. In the GB-LC described in Chapter 2 , C_{tune} is connected to the tank node, v_t. In this case,

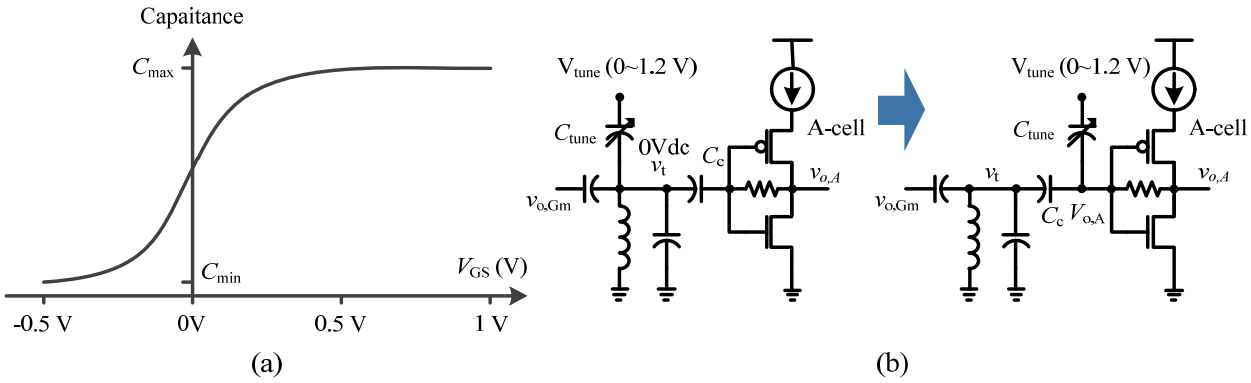


Fig. 5.6. (a) The tuning varactor, C_{tune}, is moved from the tank node to the A-cell input to reduce variation of K_{VCO}. (b) C-V characteristic curve of the varactor (NMOS in N-well).

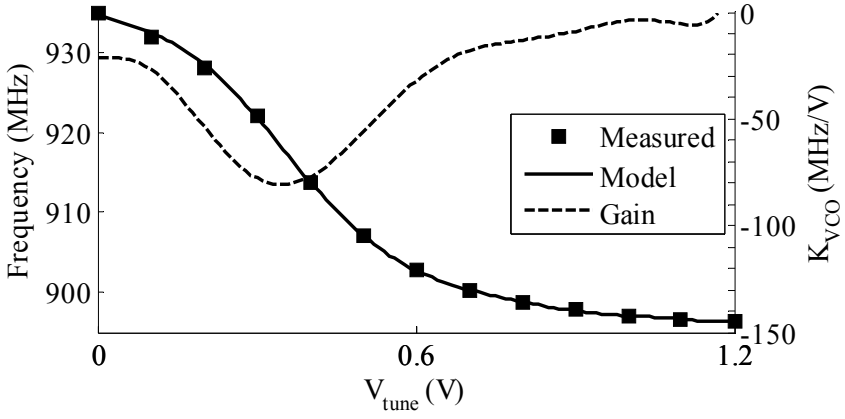


Fig. 5.7. Reduced K_{VCO} variation due to new placement of the tuning capacitor.

$V_{GS}=V_{tune}=0\sim1.2V$. As a result, as V_{tune} is increased, the tuning curve becomes almost flat beyond $V_{tune}\approx0.7V$.

The C-V plot is more linear if V_{tune} is varied in the -0.5~0.5 V range. Therefore, C_{tune} is moved to the input of the A-cell (Fig. 5.6(b)), which is biased at its threshold voltage, $V_{o,A}$. In this case, $V_{GS}=V_{tune}-V_{o,A}$. Simulation predicts that $V_{o,A}$ stays within 0.35~0.5 V across process corners for the already designed A-cell and allows good linearity in C_{tune}, and thus reduces K_{VCO} variation within an order of magnitude. This eliminates the need of the tuning limiter.

The analog tuning range of the GB-LC in this case is also doubled. The varactor is reduced in size to decrease maximum K_{VCO} in order to reduce reference spurs at the VCO output. The changed tuning curve is shown in Fig. 5.7. The gain curve is obtained through MATLAB. The variations in the gain curve near $V_{tune}=1.2V$ are due to the inaccuracy of the polynomial curve-fitting in MATLAB.

5.2.2 Optimization of GB-LC Power Consumption

It is shown in Table 5.1 that the VCO still consumes over 75% power of the total power consumption in the proposed PLL. The observations made in Chapter 2 can be further exploited to reduce this power consumption.

According to the startup criterion, (20), g_m of the G_m-cell can be further decreased by increasing the gain of A-cell. Thus, power consumption of G_m-cell can be further reduced. However, this will have the following effects –

- Lower G_m-cell current in reduced voltage swing at the tank, v_t and Leeson's equation, if applied to the GB-LC, dictates an increase in phase noise as a result.
- Reduced swing in v_t allows the A-cell to drive the G_m-cell with a more sinusoidal waveform. This will cause the charge injected to the tank by the G_m-cell ($i_{o,Gm}$) to spread across a narrower time-length. This is should be improving phase noise or at least mitigating its degradation due to reduced v_t swing to some extent.
- The tank node, v_t is also input to the digitizing buffer, which consists of CMOS inverters. Reduced v_t swing will cause more static current consumption in the first stage of this buffer.

The fabricated GB-LC, with -97.9 dBc/Hz phase noise at 1 MHz offset yields 11.5% FSK rms error that results in a BER of only 6.87 ppm ($< 10^{-3}$ ppm). This means that there is more room for tradeoff between power and phase noise. In the fabricated version of GB-LC described in Chapter 2 , both the A-cell and G_m-cell consist of equally-sized devices and are biased with equal currents to allow DC-coupling between them. As a result, the G_m-cell exhibits excess g_m, meaning extra power consumption. This is improved by decreasing the bias current of the G_m-cell,

compared to that of the A-cell. The device sizes are decreased in the same ratio to maintain equal current density and V_{GS} for DC coupling. However, this reduction is limited due to the effects mentioned above. As a result, the bias current and device sizes of the G_m-cell can be reduced to be half of those of the A-cell. The first inverter of the digitizing buffer should also be starved to limit the resultant increased static power consumption. Post-layout simulation at typical corner indicates that the VCO current consumption is reduced to 111 µA with phase noise raised to about -89 dBc/Hz at 1 MHz offset. Phase noise can still be lowered by increasing bias current.

5.3 On-chip Integration of PLL Peripherals

The proposed PLL is designed to achieve 1 MHz channel resolution. For this, a Pierce oscillator is implemented on-chip [73]. The oscillator needs only an off-chip, 2.5 mm × 2 mm, 16 MHz crystal and its 8pF load capacitor. The 16 MHz signal generated by the oscillator is then divided down to 1 MHz for PLL's reference using D Flip Flop-based asynchronous counter. The schematic of the oscillator is shown Fig. 5.8.

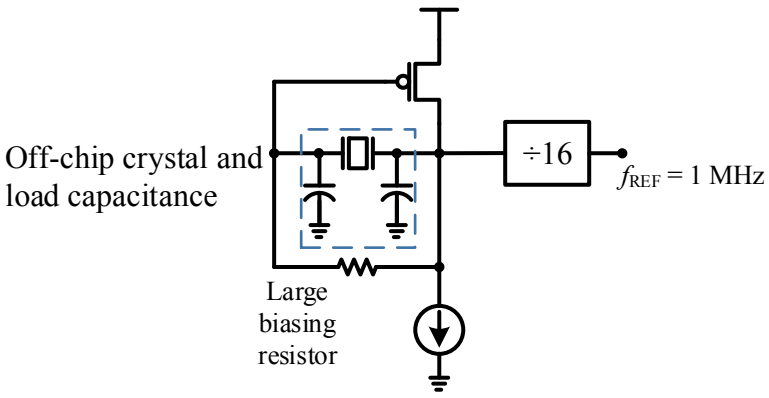


Fig. 5.8. Schematic of Pierce crystal oscillator for generating reference frequency for PLL.

A tunable bias circuit with cascade current mirrors is also implemented on-chip which provides biasing to the GB-LC VCO, the crystal oscillator and the charge-pump. The bias circuit is digitally tunable over a good range to counter process and voltage variations.

As mentioned before, a BFSK modulation system is built into the GB-LC VCO and the PA block has a built-in OOK modulation system. A logic circuit is integrated in the transmitter to provide selectivity between these two systems.

The transmitter is programmed with a 35-bit shift register. The bits distribution of this register is shown in Table 5.2. Desired transmitter settings can be written into the register using an off-chip microcontroller at the beginning of transmitter operation and the register draws negligible current during any transmitter operation.

Table 5.2. Memory distribution of the transmitter-programming register.

Block	Register bits
VCO coarse frequency control	4-bit
VCO FSK shift control	3-bit
PA output level control	2-bit
Bias tuning	14-bit
Programmable counter in divider	12-bit

Chapter 6 Measured Performance of Low-Power Transmitter

The proposed low-power transmitter has been developed in two phases. The measured performance of the transmitter in these phases are discussed in the next sections.

6.1 Low-Power 3rd Order PLL

In the first phase, the 3rd order PLL was taped out and measured in a 130 nm 1P8M CMOS process. The PLL in this phase was designed with the hybrid prescaler and the GB-LC VCO with the modified analog tuning and optimized power consumption, as described in sections 5.2.1 and 5.2.2. The layout and die microphotograph of this PLL is shown in Fig. 6.1. The die was assembled in a 7 mm × 7 mm QFN package which was then placed in an RF test socket and the PLL was

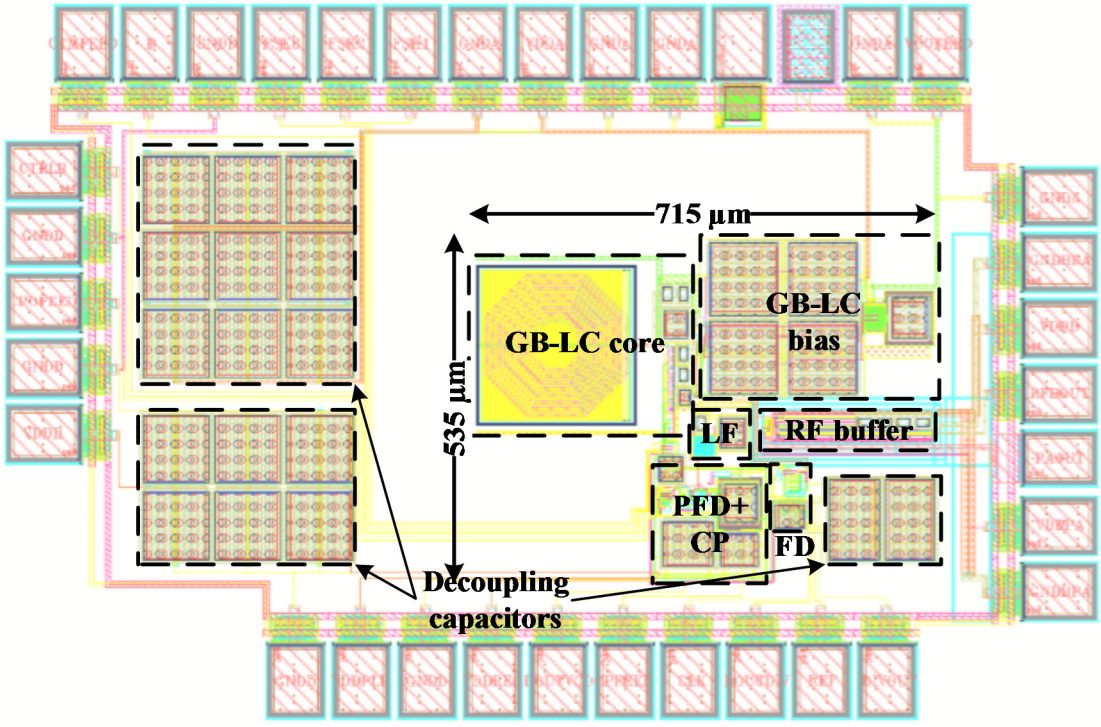


Fig. 6.1. Layout of the 3rd order PLL in the first phase of proposed transmitter implementation.

tested with the setup showed in Fig. 6.2. An off-chip 1 MHz crystal oscillator is used to generate reference for the PLL. A digital, high-frequency, pad-driving buffer provides the RF output. Buffers are also added to monitor the frequency divider output and the PLL control voltage, v_{ctrl}, generated by the Charge Pump (CP) and Loop Filter (LF). Individual bias currents are provided for the VCO, CP and buffers by off-chip transconductor circuits.

Fig. 6.3 shows the output spectrum of the unmodulated 915 MHz carrier generated by the PLL, obtained using spectrum analyzer. It is to be noted that the reference spurs at 1 MHz offset shows up with higher strength (-31 dBm offset from carrier) only if the buffer for v_{ctrl} is turned on. The frequency divider output and the settled v_{ctrl}, observed in oscilloscope, are shown in Fig. 6.4.

The phase noise spectra of the free-running GB-LC VCO and the PLL is shown overlaid in Fig. 6.5. The v_{ctrl} buffer is turned off during this. The PLL suppresses close-in phase noise in about 10 kHz closed-loop bandwidth. Phase noise is -87.93 dBc/Hz at 1 MHz offset. The GB-LC VCO draws 111.8 μA current. This agrees very well with the results from post-layout simulation.

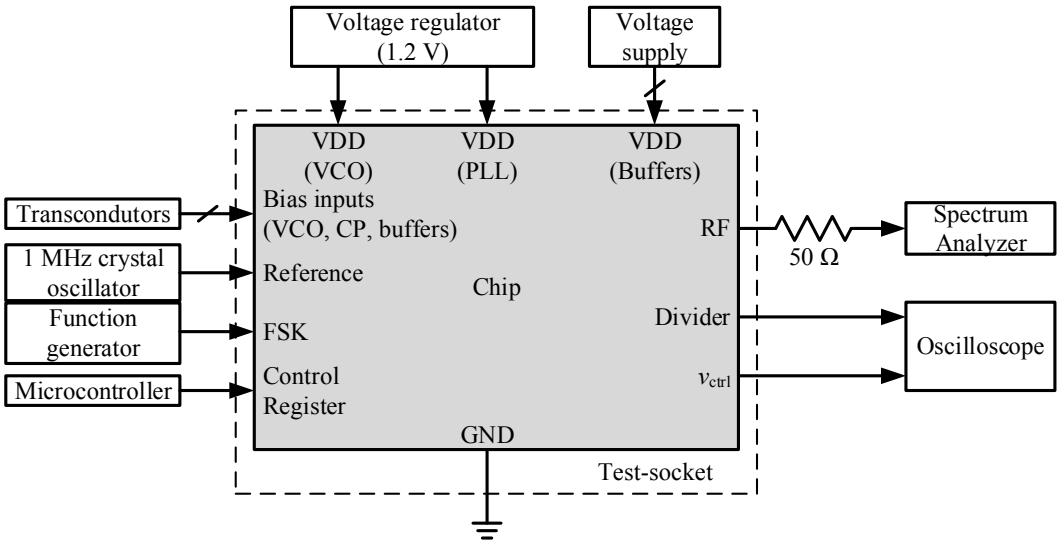


Fig. 6.2. Test setup for the 3rd order PLL in the first phase.

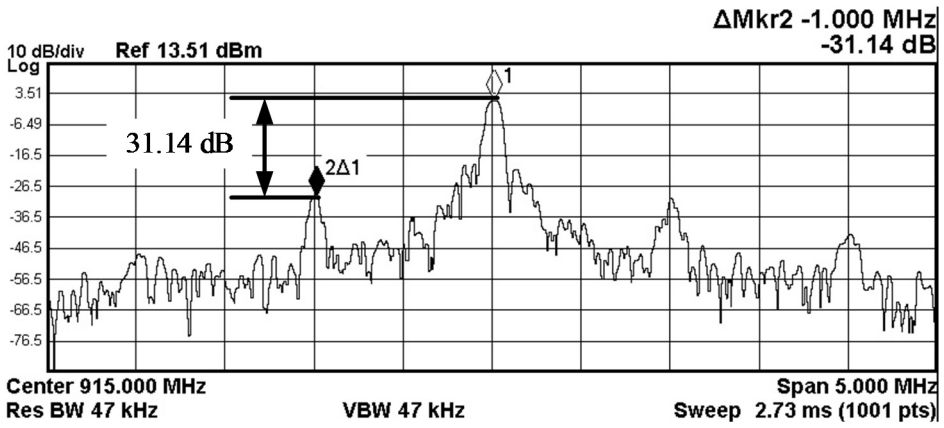


Fig. 6.3. Spectrum of unmodulated 915 MHz carrier generated by the PLL.

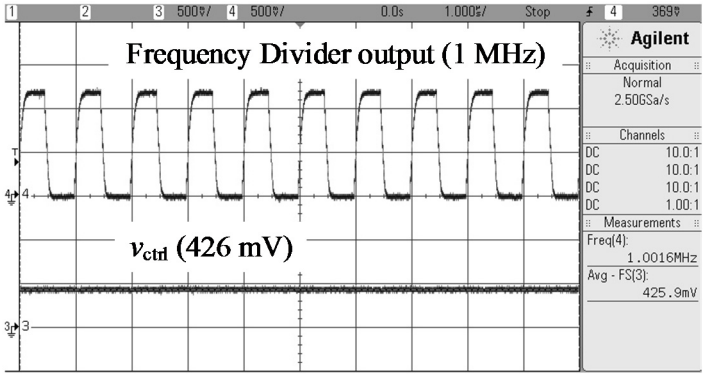


Fig. 6.4. VCO signal divided down to 1 MHz and CP-LF generated control voltage.

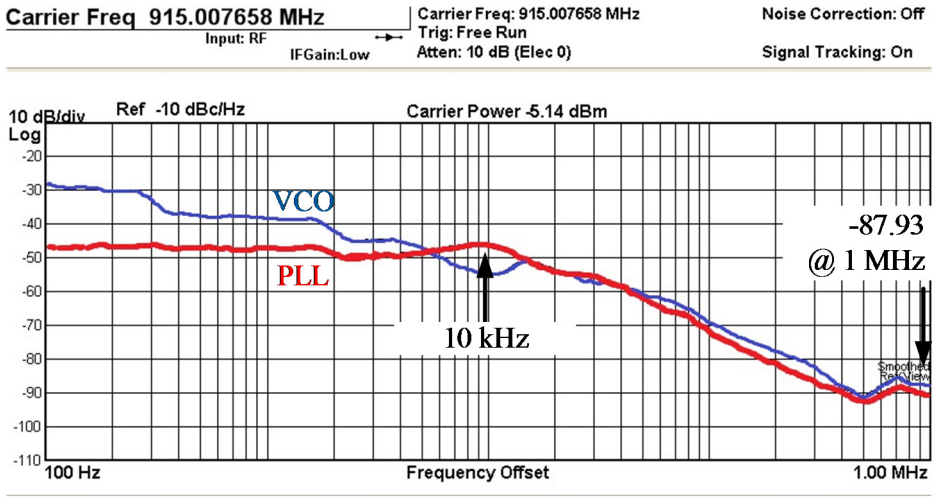
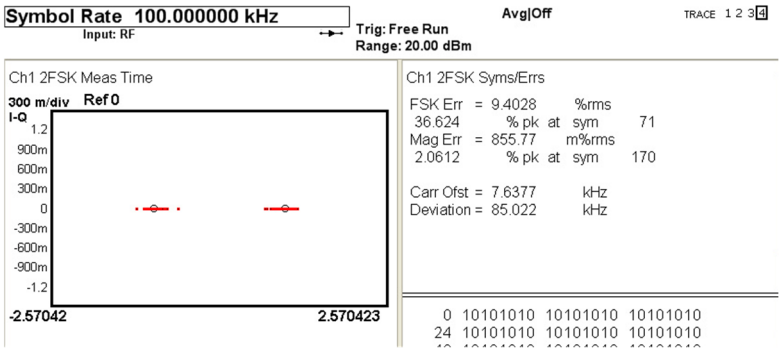
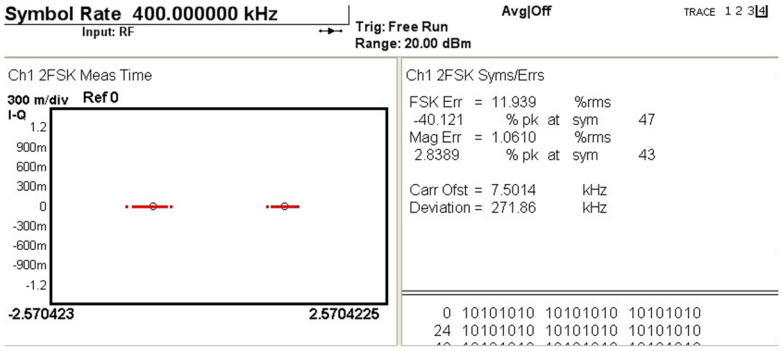


Fig. 6.5. Overlaid phase noise spectra of the VCO and PLL. This shows 10 kHz PLL bandwidth and unsuppressed phase noise of -87.93 dBc/Hz at 1 MHz offset.



(a)



(b)

Fig. 6.6. Constellation and statistical error results of FSK modulated carrier at (a) 100 kbps and (b) 400 kbps data rate. The data is simulated by a square wave a from function generator.

Fig. 6.6 shows the performance of the BFSK modulation system of the PLL with the power-reduced VCO. The BFSK modulation with 250 kHz deviation shows only 12% rms error at 400 kbps data rate, which corresponds to 15.45 ppm BER using the method described in Chapter 2 . It is to be noted that as this BER is more than that found from the GB-LC in Chapter 2 . This is the result of sacrificing phase noise performance for lower power consumption.

The PLL consumes total 175.3 µW power from a 1.2 V supply. This power is distributed among the VCO and the rest of the PLL (including the hybrid prescaler) as 134.2 µW and 41.1 µW.

6.2 Low-Power Transmitter

In the second phase, the crystal oscillator and the power amplifier was integrated with the PLL to implement the low-power transmitter in the same 130 nm CMOS process. A tunable bias circuit is also implemented on-chip, such that all the blocks in the transmitter can be biased using only one off-chip resistor. The die was assembled in a 12 mm × 12 mm QFN package and then placed in an RF test socket for testing. The transmitter occupies 0.29 mm^2 silicon area. The die microphotograph and a schematic of the test setup are shown in Fig. 6.7 and Fig. 6.8.

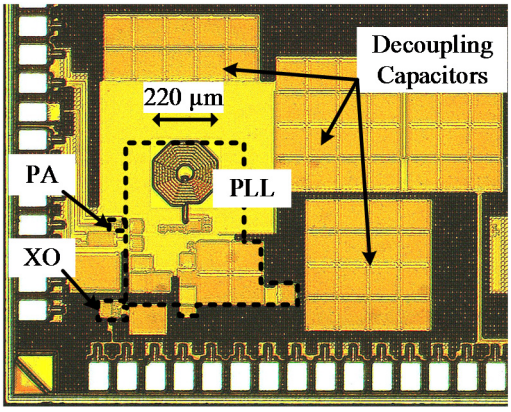


Fig. 6.7. Microphotograph of the transmitter die.

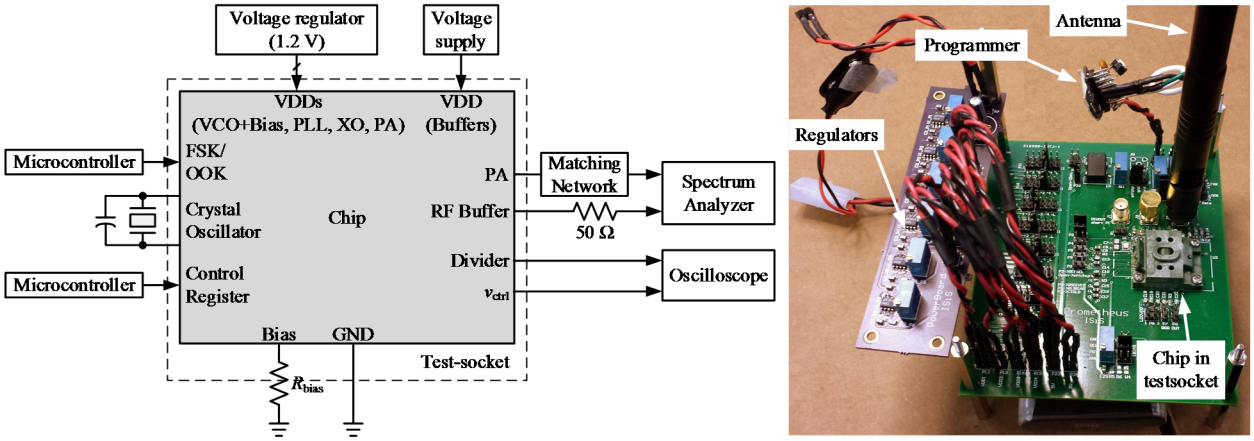
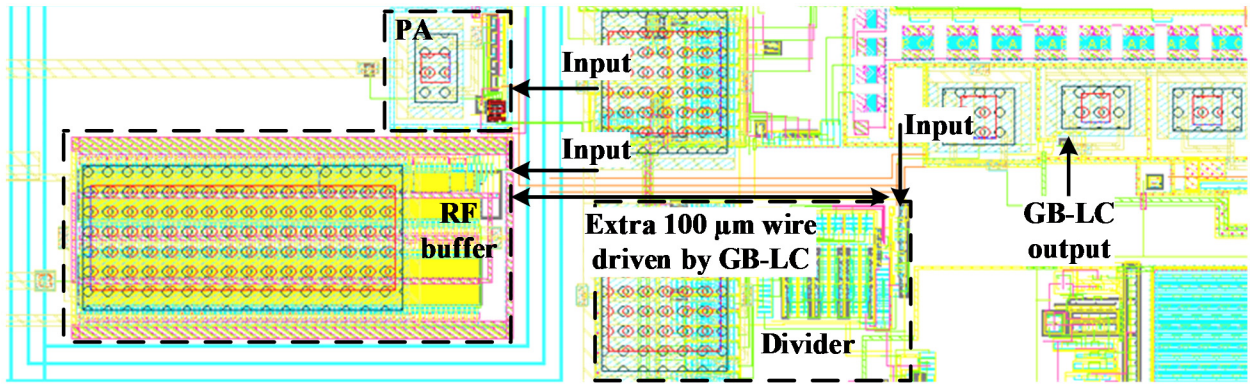
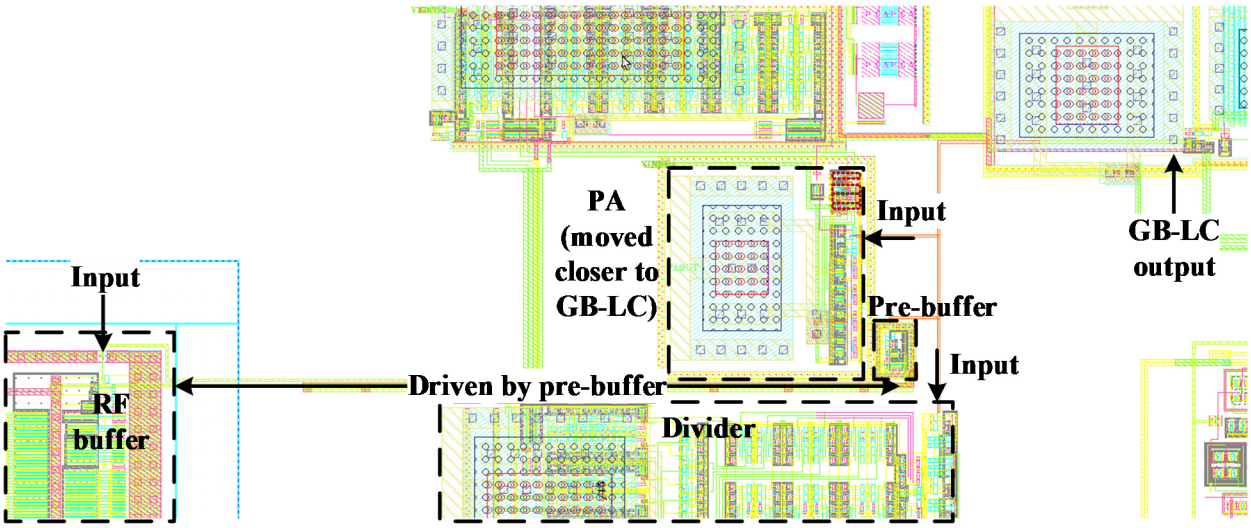


Fig. 6.8. Test setup for the transmitter.

During the measurements of the preliminary transmitter, some modifications were found necessary with the digitizing buffer of the GB-LC VCO. This buffer provides the output of the GB-LC to the rest of the circuit. The number and strength of the inverter stages needed to be increased to ensure sufficient digitization. In the transmitter circuit, the digitizing buffer provides the signal to three blocks – the frequency divider, the power amplifier and a pad-driving RF test buffer. The RF buffer is designed to drive an off-chip load capacitance of 30pF from measurement instruments. As a result, the RF buffer consumes very large amount of current (about 30 mA) and the multiple large inverter stages generates enough noise to disrupt in the substrate the operation of sensitive low-frequency blocks of the PLL. With this insight, the RF buffer is placed in an isolated substrate using low-doped, highly resistive substrate region. This also results in long metal wiring between the RF buffer and the digitizing buffer and thus, large parasitic capacitance to be driven by the digitizing buffer. This increases its power consumption, as observed to be about 48 μW in the GB-LC described in Chapter 2 . To remedy this problem, a small pre-buffer can be placed close to the digitizing buffer, before the RF buffer. This pre-buffer would share the same power supply with the RF buffer which would be separate from the transmitter's supply, and therefore its power consumption would not be counted for total power consumption. Careful placement of the divider and PA blocks are also necessary to reduce the wiring capacitance at the digitizing buffer's output. These adjustments are shown in Fig. 6.9. For this transmitter-under-test, however, the bias current input is increased to raise the oscillation amplitude. As the bias input is also common to the charge pump and the crystal oscillator, their power consumption is also increased. As a result, power consumption of the PLL in this phase is higher than that in the first phase.



(a)



(b)

Fig. 6.9. (a) Previous layout of the output wiring of GB-LC's digitizing output buffer. (b) New layout showing the adjustments done to reduce the extra power consumption for driving the RF test buffer.

Also because of using larger test socket, the PCB trace between the PA output and the matching network is long enough to deteriorate the impedance transformation by the matching network. As a result, the PA efficiency is reduced from estimation through simulations. The matching network was adjusted using ADS software with microstrip model for the trace to provide maximum possible power output and efficiency.

Fig. 6.10 shows the output spectrum of the unmodulated 925 MHz carrier generated by the proposed transmitter. The maximum output power is -18.6 dBm with 12.5% drain efficiency, achieved by turning on all four PA stages. The different output power levels and corresponding efficiencies of the PA at different settings are listed in Table 6.1. The phase noise spectra of the free-running GB-LC VCO and the PLL is shown in Fig. 6.11. The PLL suppresses close-in phase noise in about 10 kHz closed-loop bandwidth. Phase noise is -100.2 dBc/Hz at 1 MHz offset.

Fig. 6.12 and Fig. 6.13 show the performance of the BFSK modulation system. The BFSK modulation with 250 kHz deviation achieves maximum 3 Mbps speed with 11% rms error, corresponding to 2.74 ppm BER. At 200 kbps speed, the error reduces to 4.4%. A pseudo-random data set of about 2.6 million bits is also transmitted at a receiver-limited rate of 400 kbps and received at 1 m distance with 0 bit errors. Manchester encoding is used to prevent symbol degradation due to the PLL's frequency correction response by removing any DC state in data. This also aids in clock and data recovery. This is to be noted that Manchester encoding doubles the number of bits or the bit rate for a certain data rate. As a result, Manchester-encoded data at 400 kbps is equivalent to 800 kbps not-encoded data. At 800 kbps speed, the transmitter yields 7.68% rms FSK error with '01010101' bitstream, corresponding to 3.7×10^{-5} ppm BER.

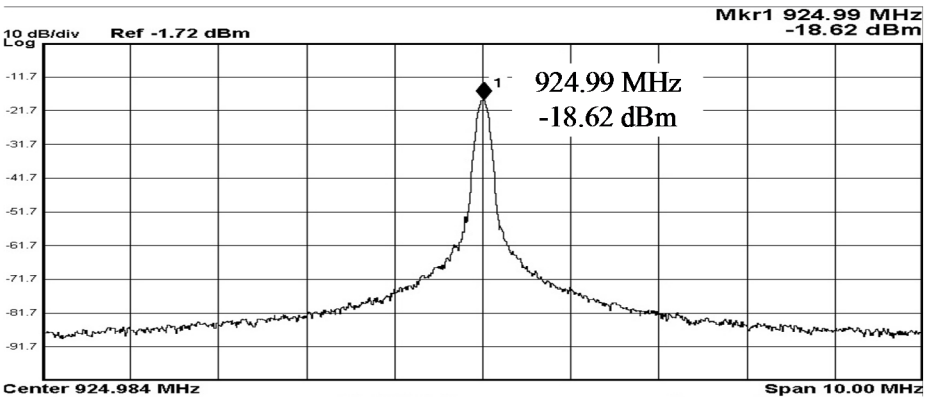


Fig. 6.10. Spectrum of unmodulated 925 MHz carrier signal, with PA at maximum output power, -18.6 dBm.

Table 6.1. Power Amplifier output power levels, power consumption and efficiencies.

No. of active stages	Output power (dBm)	Power consumption (μW)	Efficiency (%)
1	-29.67	43.2	2.5
2	-24.1	69.12	5.6
3	-21.12	92.4	8.4
4	-18.62	110.4	12.5

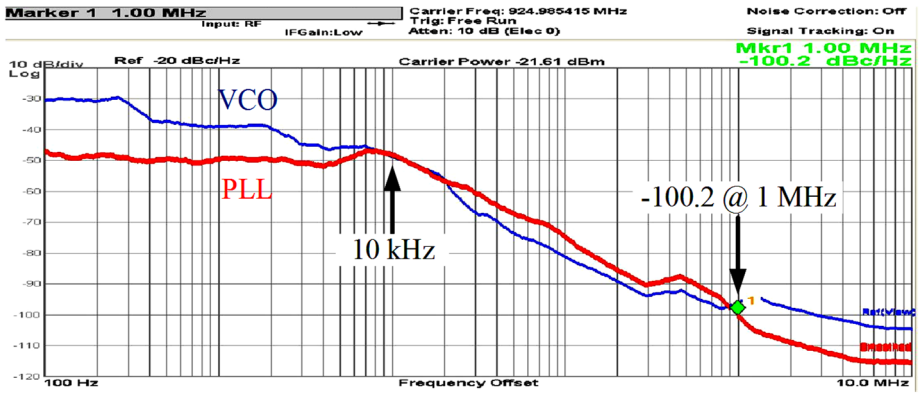


Fig. 6.11. Overlaid phase noise spectra of the PLL and the free-running VCO. Phase noise of PLL is -100.2 dBc/Hz at 1 MHz offset.

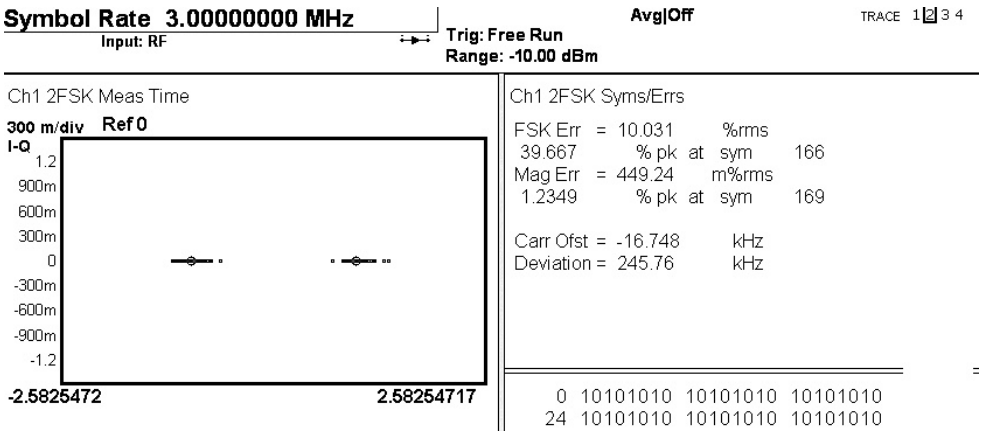


Fig. 6.12. Constellation diagram and BFSK error results of the transmitter with continuous '01010101' bitstream at 3 Mbps speed with 250 kHz deviation. RMS FSK error is about 11%.

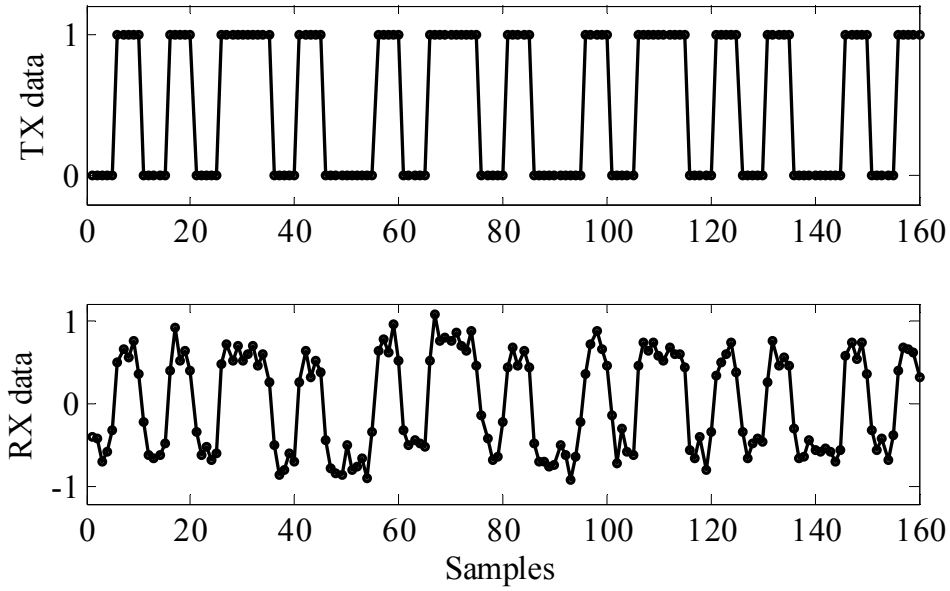


Fig. 6.13. Two bytes from a pseudo-random data (Manchester encoded) set transmitted and received at 400 kbps speed through FSK modulation system. Data is sampled at 4 MHz by the receiver.

Fig. 6.14 and Fig. 6.15 show the performance of the OOK modulation system. The OOK output is observed in oscilloscope first with continuous '01010101' bitstream as baseband data at maximum 20 Mbps speed. The pseudo-random data set mentioned previously is again transmitted through OOK at 400 kbps and received at 1 m distance with 0 bit errors. Manchester encoding is used for clock and data recovery.

For -18.6 dBm radiated power, the transmitter consumes 367.1 μW power from 1.2 V supply in FSK mode and 314.3 μW in OOK mode. The power breakdown of the different blocks is listed in Table 6.2. The transmitter shows energy efficiency of 122.3 pJ/bit during 3 Mbps FSK transmission and only 15.7 pJ/bit during 20 Mbps OOK transmission. This efficiency is superior to recent low-power transmitter works. The performance summary of the transmitter, with comparison with the state-of-the-art is shown in Table 6.3. This work has been reported in [74].

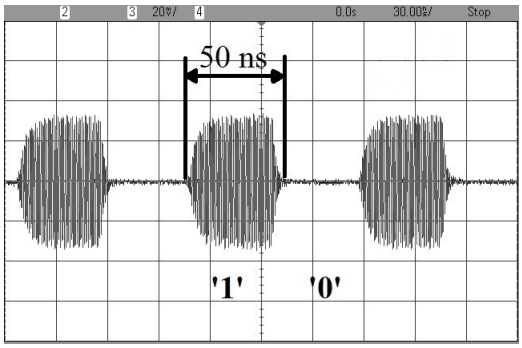


Fig. 6.14. 925 MHz carrier OOK-modulated by continuous '01010101' bitstream at 20 Mbps speed.

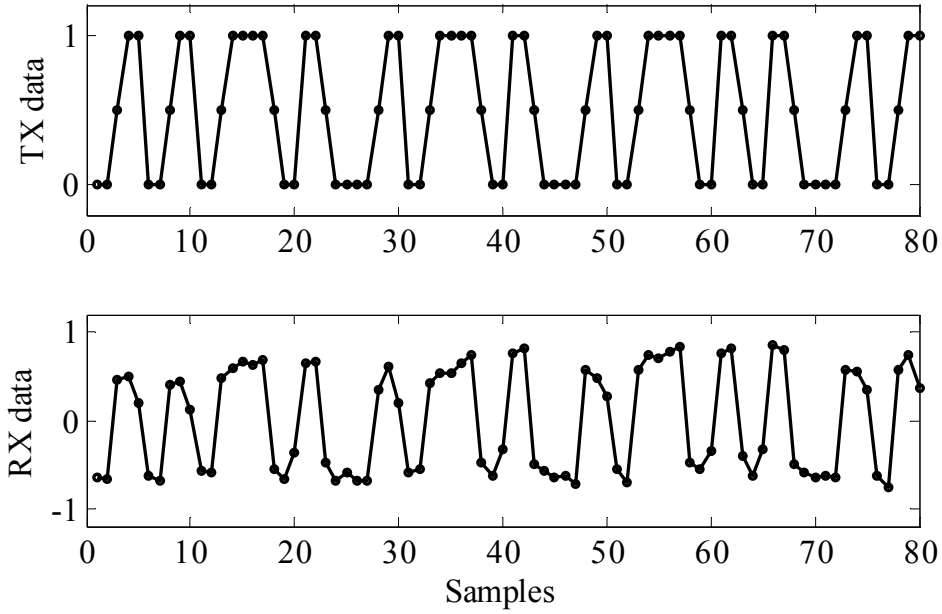


Fig. 6.15. Two bytes from a pseudo-random data (Manchester encoded) set transmitted and received at 400 kbps speed through FSK modulation system. Data is sampled at 2 MHz by the receiver.

Table 6.2. Power breakdown of the proposed transmitter in the second phase.

Block	Power consumption (μW)	
Crystal oscillator		32.6
PLL (= PFD + Charge pump + Frequency divider)		50.1
GB-LC VCO + Bias network		174
Power amplifier (-18.6 dBm output)	FSK	110.4
	OOK	57.6
Total	FSK	367.1
	OOK	314.3

Table 6.3. Performance summary of the proposed BFSK/OOK transmitter and comparison to state-of-the-art.

	This work		[75]	[11]	[69]	[76]	[77]
Publication	RFIC,'15		JSSC,'11	JSSC,'11	RFIC,'13	TBioCAS,'11	TBioCAS,'13
Frequency (MHz)	925		920	400	400/433	2400	400
CMOS (nm)	130		180	130	130	90	90
Die area (mm^2)	0.29		-	0.04	0.41	0.882	0.06
Architecture	PLL + PA		Unlocked DCO + PA	ILVCO + Edge-combining PA	PLL + PA	PLL+PA	ILVCO + Edge combiner + PA
On-chip channel selection	Yes		Yes	No	Yes	Yes	No
Output power (dBm)	-18.6		-10	-16	-16	0	-17
Modulation	FSK	OOK	FSK	FSK	FSK	OOK	OOK
Data rate (Mbps)	3*	20	5	0.2	0.08	10	1
Power consumption (μW)	367	314	700	90	150	2530	160
Energy efficiency (pJ/bit)	122.3	15.7	140	450	1875	253	160
Supply voltage (V)	1.2		0.7	1.2	0.7-1.2	1	0.6

* 11% rms FSK error, reduces to 4.4% at 200 kbps data rate.

Chapter 7 Conclusion and Future Works

7.1 Original Contributions

A low-power, low-complexity PLL-based transmitter for wireless sensors is presented in this dissertation. Pre-power-amplifier power consumption has been identified as the key challenge for this work. New circuit topologies for the two most power-hungry blocks, oscillator and prescaler, have been developed and analyzed as solutions to this problem.

The original contributions of this work are listed below –

- Designed and tested an ultra-low-power, wide-locking-range, dual-modulus frequency divider as the prescaler in a PLL. The wide locking range enables it to be integrated into PLLs aimed at MICS band, 433 and 915 MHz ISM bands. The dual-modulus feature is very desirable for a programmable frequency divider.
- Developed critical design considerations and mathematical analysis enabling easy estimation of the divider's power consumption, locking range and white-region phase noise.
- Designed and tested a novel low-power gain-boosted LC (GB-LC) oscillator as the VCO in a PLL. The gain-boosting topology enables much reduced startup power in a simple single-ended structure, while retaining reasonable noise performance for wireless sensor applications with simple, low-data-rate modulation schemes.
- Developed mathematical analysis for predicting the GB-LC oscillator's frequency of oscillation, startup criteria and phase noise.

- Designed and implemented a low-power PLL-based transmitter on-chip, integrating the new VCO and prescaler topologies and successfully tested for short-range transmissions using both FSK and OOK modulation schemes. The transmitter shows very high energy efficiency, suitable for low-power wireless sensors.

The proposed transmitter successfully proves the core concept of this work which is that carrier phase noise tolerance can be loosened while maintaining acceptable transmission quality for applications with low-data-rate simple modulation schemes, such as low-power wireless sensors. This is a very important consideration when reduction for power spent for carrier generation is desired.

7.2 Future Work

Some improvements to the proposed transmitter remain yet for future work. They are summarized below –

- The GB-LC VCO still consumes more than 50% of the total power of the transmitter. It has been shown in [78] that current-reuse technique can greatly reduce power consumption of an LC VCO. Techniques such as this can be investigated also on the proposed GB-LC VCO to further reduce its power consumption while maintaining current phase noise performance. High-Q bondwire inductances can be also investigated for the VCO tank to improve the power and noise performance.
- The power amplifier is the second most power-hungry block in this transmitter and it needs a more efficient design. The Class D amplifier used here takes the digitized carrier as the input and needs a small driver, which consumes power. Driverless PA

classes like B and C can be investigated to use the sinusoidal carrier in the VCO tank directly, which can provide better efficiency.

- The off-chip matching network used by the PA can be integrated on-chip with bondwire or on-chip inductors. This will eliminate the degradation of transformation ratio by non-idealities such as circuit-board traces. This will also reduce the circuit-board size.
- A process- and supply-insensitive beta-multiplier reference block can be integrated on-chip to generate current reference for the tunable bias circuit.
- The GB-LC VCO can be investigated for unlocked DCO-based transmitters with calibration, which can prove to be lower-power transmitter than a PLL-based one.
- The proposed transmitter should be integrated in a wireless sensor system-on-chip and field-tested for performance.

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