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A Low-Power, Reconfigurable, Pipelined ADC with Automatic Adaptation for Implantable Bioimpedance Applications

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To the Graduate Council:

I am submitting herewith a dissertation written by Terence Cordell Randall entitled "A Low-Power, Reconfigurable, Pipelined ADC with Automatic Adaptation for Implantable Bioimpedance Applications." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

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Abstract

Biomedical monitoring systems that observe various physiological parameters or electrochemical reactions typically cannot expect signals with fixed amplitude or frequency as signal properties can vary greatly even among similar biosignals. Furthermore, advancements in biomedical research have resulted in more elaborate biosignal monitoring schemes which allow the continuous acquisition of important patient information. Conventional ADCs with a fixed resolution and sampling rate are not able to adapt to signals with a wide range of variation. As a result, reconfigurable analog-to-digital converters (ADC) have become increasingly more attractive for implantable biosensor systems. These converters are able to change their operable resolution, sampling rate, or both in order convert changing signals with increased power efficiency.

Traditionally, biomedical sensing applications were limited to low frequencies. Therefore, much of the research on ADCs for biomedical applications focused on minimizing power consumption with smaller bias currents resulting in low sampling rates. However, recently bioimpedance monitoring has become more popular because of its healthcare possibilities. Bioimpedance monitoring involves injecting an AC current into a biosample and measuring the corresponding voltage drop. The frequency of the injected current greatly affects the amplitude and phase of the voltage drop as biological tissue is comprised of resistive and capacitive elements. For this reason, a full spectrum of measurements from 100 Hz to 10-100 MHz is required to gain a full understanding of the impedance. For this type of implantable biomedical

application, the typical low power, low sampling rate analog-to-digital converter is insufficient. A different optimization of power and performance must be achieved.

Since SAR ADC power consumption scales heavily with sampling rate, the converters that sample fast enough to be attractive for bioimpedance monitoring do not have a figure-of-merit that is comparable to the slower converters. Therefore, an auto-adapting, reconfigurable pipelined analog-to-digital converter is proposed. The converter can operate with either 8 or 10 bits of resolution and with a sampling rate of 0.1 or 20 MS/s. Additionally, the resolution and sampling rate are automatically determined by the converter itself based on the input signal. This way, power efficiency is increased for input signals of varying frequency and amplitude.

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Chapter 1 – Introduction

1.1 Motivation

In 1880, the use of bioelectrical impedance as a safe, convenient, and accurate method to measure the conductivity of the body was first documented. In the mid 1900s, bioimpedance studies focused on correlations between bioimpedance measurements and total body water (TBW) as well as other physiological parameters such as blood flow, basal metabolism, and thyroid function. It was found that the bioelectric impedances of certain tissues, organs, and cells were correlated to a number of biological phenomena. This led to the development of some of today's applications for bioelectric impedance such as electrical impedance tomography (EIT), which is a medical imaging procedure that uses surface electrical measurements to infer an image of the conductivity of parts of the body, and electrical impedance spectroscopy (EIS) which is a multi-frequency measurement of bioimpedance that has been proven to be effective at detecting some afflictions such as acute ischemia [1].

In the late 1900s, the use of single-frequency and multi-frequency impedance measurements to estimate body composition was heavily explored. The development of commercial, relatively inexpensive bioimpedance analyzers helped scientists recognize the value of bioimpedance research. However, uncertainty in exactly how to interpret bioimpedance data led to the National Institute of Health (NIH) holding a technology assessment conference in December 1994. The conference aimed to answer the following 5 questions:

(i) What does bioelectrical impedance measure in terms of electrical and biological parameters, and how safe is it?

(ii) How bioelectrical impedance should be performed, and how can BIA measurements be standardized?

(iii) How valid is the bioelectrical impedance technology in the estimation of TBW, fat-free mass, and adiposity?

(iv) What are the appropriate clinical uses of bioelectrical impedance technology, and what are the limitations?

(v) What are the future directions for basic science, and epidemiological evaluation of body composition measurements?

The full application of bioelectrical impedance is still unknown, but the NIH conference indicated some of the directions the research should take. Now researchers are exploring many different applications such as glucose monitoring, foot sole blood perfusion, breast cancer monitoring, and instantaneous arterial blood pressure to name a few [2] – [5].

Researchers have begun to explore implantable bioimpedance analyzers that would enable around-the-clock monitoring of data in a minimally invasive way. Correlations between bioimpedance and various biological phenomena would then be able to be more closely monitored. One group that works with regenerative tissue is trying to regenerate an old infarction scar using myocardial cell precursors derived from stem cells [6]. After a patient has a myocardial infarction (heart attack), heart muscle cells in the left ventricle are starved of oxygen and eventually die. This results in the thinning of the left ventricle as is illustrated in Figure 1.1. Side effects of this include blood pressure overload, heart failure, and eventually death [7]. One

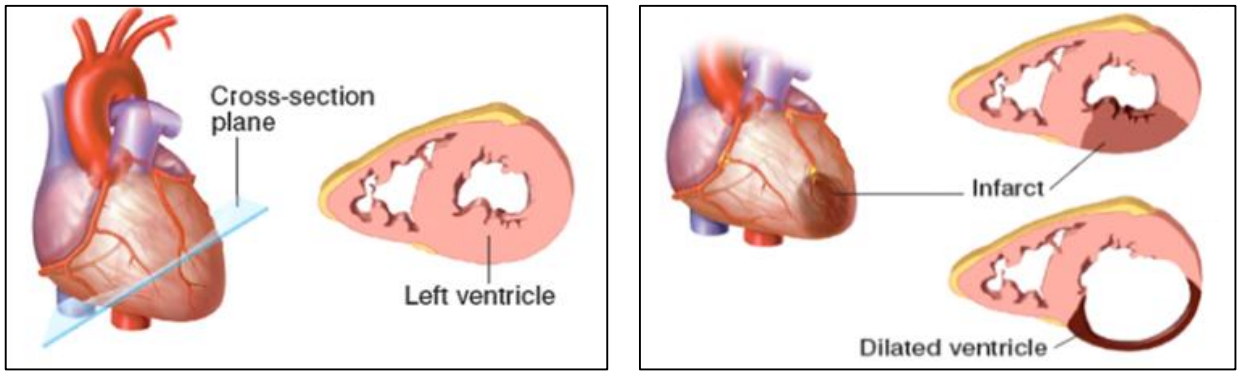


Figure 1.1 Normal heart (left) and a heart after a heart attack (right) [7].

mechanism for heart repair to prevent this from happening is strengthening the post-infarction scar with the use of stem cells.

Stem cells can repopulate scar tissues making them more muscle-like and improve left ventricular function. In order to monitor how well the engineered tissue was being accepted, an implantable bioimpedance monitoring system was developed for an animal model heart. A block diagram of the system is shown in Figure 1.2. The system measures impedance at fourteen discrete frequencies—100 Hz, 200 Hz, 500 Hz, 700 Hz, 1 kHz, 2 kHz, 5 kHz, 7 kHz, 10 kHz, 20 kHz, 50 kHz, 70 kHz, 100 kHz, and 200 kHz. The current source injects an AC current into the biosample at one of the above mentioned frequencies and the corresponding voltage drop is amplified and then analyzed. The measurements are stored in 16-Mbit memory and are transmitted to an external PC at any time using ZigBee protocol. The impedance measurement and digitization is handled by the AD5933, an impedance converter and network analyzer from Analog Devices. The chip is equipped with a 12-bit, 1 MS/S analog-to-digital converter of undisclosed topology. The AD5933 requires a power supply of 2.7 to 5.5 V and consumes a nominal current of 10 mA [8]. The implantable system is wrapped with cellophane film (3M)

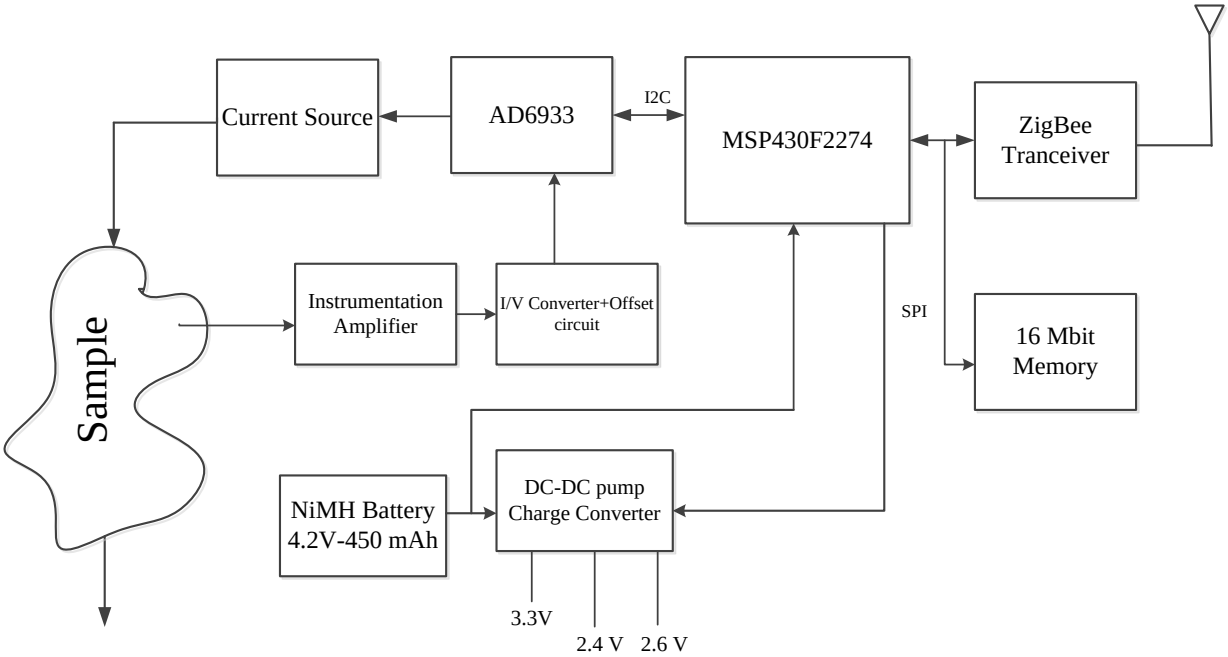


Figure 1.2 Block diagram of implantable bioimpedance monitoring system.

and sealed with medical-grade silicone, and the electrode cables are covered with a silicone tube and cured with epoxy [6].

Preliminary results of the system validate the possibility of an implantable bioimpedance monitor; however, there are many flaws with the system with one of them being the use of the AD5933. First, the power supply requirement of the AD5933 is too high to be attractive for modern implantable medical systems [9], [10]. As CMOS technology is scaled down, so are supply voltages. A system that operates between 1 – 2 V is ideal for implantable systems to help extend battery life or relax the requirements of wireless powering schemes such as inductive link or optical power. A reconfigurable converter would offer a number of improvements over the converter included in the AD5933. For example, the AD5933 samples at 1 megasample per second (MS/S) regardless of the input signal. This is overkill for a slow input signal such as 100 Hz, and power efficiency is decreased as a result. On the other hand, the maximum 1 MS/S

sampling rate is also a drawback because it is too slow. As can be seen in the Appendix, valuable bioimpedance data can be obtained from high frequency measurements in the tens of megahertz range. By limiting the input data frequency to 500 kHz, valuable information could be lost. A reconfigurable ADC with the ability to sample at high frequencies, and also be able to scale down the bias currents for lower frequency measurements would be extremely attractive for a bioimpedance monitoring system. In this way, the full spectrum of useful bioimpedance data can be monitored with increased power efficiency.

1.2 Research Goal

The goal of this research is to design an auto-adapting reconfigurable pipelined analog-to-digital converter in terms of resolution and sampling rate. The converter will be integrated into the back-end signal processing of an implantable bioimpedance monitoring system. The ADC should consume a minimal amount of power and occupy as small an area as possible while maintaining proper, accurate functionality throughout the entire range of operation. A conversion will take place with one of two sampling rates and resolutions. This enables four regions of operation:

a) Low Resolution – Low Sampling Rate mode
    - The ADC operates at 100 kS/s and 8-bit resolution
b) High Resolution – Low Sampling Rate mode
    - The ADC operates at 100 kS/s and 10-bit resolution
c) Low Resolution – High Sampling Rate mode
    - The ADC operates at 20 MS/s and 8-bit resolution
d) High Resolution – High Sampling Rate mode
    - The ADC operates at 20 MS/s and 10-bit resolution

1.3 Dissertation Overview

The remainder of the dissertation is organized as follows: A survey of the popular analog-to-digital converter architectures will be conducted in Chapter 2. A review of reconfigurable data converters and low power data converters and their various implementations and concerns are given in Chapter 3. In Chapter 4, the conventional pipelined converter architecture is presented along with fundamental ADC basics. Chapter 5 discusses the principles of reconfiguration and automatic adaption. Non-idealities of the pipelined converter are analyzed in Chapter 6. Key blocks in the design of the system along with the chip layout are described in Chapter 7. In Chapter 8, the static and dynamic performances of the system are presented, the converter figure-of-merit is analyzed, and a comparison to existing reconfigurable pipelined ADCs is made. The dissertation is concluded in Chapter 9 where the original contributions of this work are reported along with future work. In addition, an Appendix on bioimpedance is included at the very end.

Chapter 2 – ADC Survey

Over the years, several ADC architectures have been developed to meet the needs of a wide range of applications. Among them all, four architectures, namely *successive approximation register* (SAR), *delta-sigma* (ΔΣ), *pipelined*, and *flash*, have stood out as the dominant architectures in industry and research [11]. Each of these converters offers their own advantages while suffering from unique drawbacks. As electronics become more integrated into society day by day, and as the limits of electronics get pushed further and further, the need for high performance, low-power analog-to-digital converters increases more and more. Thus, research is actively being conducted on the aforementioned ADC architectures to eliminate their respective drawbacks and/or improve their performance in terms of dynamic range, linearity, bandwidth, etc. In this chapter, a survey of the four main analog-to-digital converter architectures will be conducted. An overview of each type of converter is presented in the following section. The key concepts surrounding each converter are discussed, and the state-of-the-art trends in research on them are presented.

2.1 SAR ADC

Successive-approximation-register (SAR) analog-to-digital converters (ADCs) are frequently the architecture of choice for medium-to-high-resolution applications with slow-to-medium sample rates. Classically, SAR sampling rates did not exceed roughly 5 megasamples per second (MS/S); however, with device scaling and newfound techniques, this is no longer the case as will be discussed later. Resolutions for SAR ADCs typically range from 8 to 16 bits, and

the ADCs provide low power consumption along with small die area. This combination of features makes these converters ideal for a wide variety of applications, such as portable instruments, industrial controls, and data/signal acquisition [12].

As the name implies, the SAR converter employs a binary search algorithm. Therefore, the internal circuitry is required to operate much faster than the overall ADC sampling rate. Generally, the internal circuitry will run *at least* as fast as the ADC sampling rate times the resolution. Therefore a 10-bit, 1 MS/S SAR ADC will internally run no slower than 10 MHz so that all 10 bits can be resolved within a single sampling period. The basic architecture for an SAR ADC is quite simple and can be seen in Figure 2.1, although the architecture has evolved over the years as more variations and improvements were developed. The analog input voltage (V_{IN}) is held on a sample-and-hold (or track-and-hold). Then a binary search algorithm is used to digitize the analog voltage with the following basic flow: the N-bit register is first set to midscale (only the MSB is set to 1 and all other bits are set to 0), forcing the digital-to-analog converter (DAC) output (V_{DAC}) to be equal to $V_{REF}/2$, where V_{REF} is the reference voltage provided to the ADC. A comparator then determines if V_{IN} is less than, or greater than, V_{DAC}. If V_{IN} is greater than V_{DAC}, the comparator output is logic 'high', and the MSB of the N-bit register remains at 1. Conversely, if V_{IN} is less than V_{DAC}, the comparator output is logic 'low', and the MSB of the register is switched to 0. The SAR control logic then moves to the next bit down, and the sequence repeats until all bits have been determined. Once completed, the N-bit digital word is available in the register, and the next sampled analog voltage is ready to be converted.

Notice that four comparison periods are required for a 4-bit ADC. In general, an N-bit SAR ADC will require N comparison periods and will not be ready for the next conversion until the current one is complete. This explains why these ADCs are power-and-space efficient. On

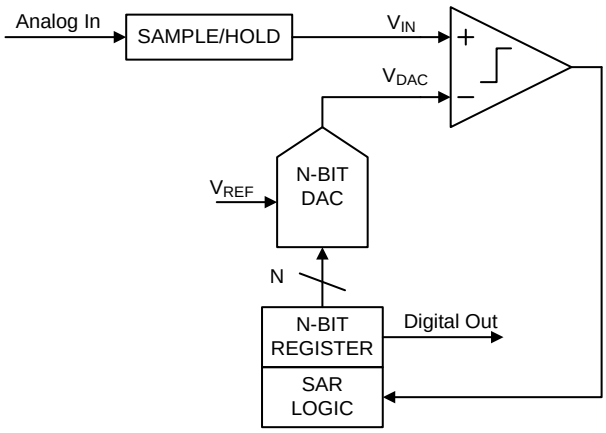


Figure 2.1 Basic block diagram of a Successive Approximation Register analog-to-digital converter.

the other hand, it also accounts, in part, for their limited speed. As a whole, the speed of an SAR ADC is limited by the setting time of the DAC, which must be as accurate as the total converter, the comparator, which must be fast and have minimal settling time, and the logic overhead.

The two most critical components in an SAR converter are the DAC and the comparator because they dictate most of the performance parameters as they are directly responsible for the conversion of the analog sample to a digital code.

2.1.1 The Digital-to-Analog Converter

Most SAR converters use a capacitive DAC which provides a built-in track-and-hold function and consist of an array of N capacitors with binary weighted values plus one "dummy LSB" capacitor. Figure 2.2 shows an example of a 16-bit capacitive DAC connected to a comparator. During the acquisition phase, the common terminal (the terminal at which all the capacitors share a connection) of the array is connected to ground and all free terminals are connected to the input signal, V_{IN}. The common terminal is then disconnected from ground, and the free terminals are disconnected from V_{IN}, thus a charge proportional to the input voltage is

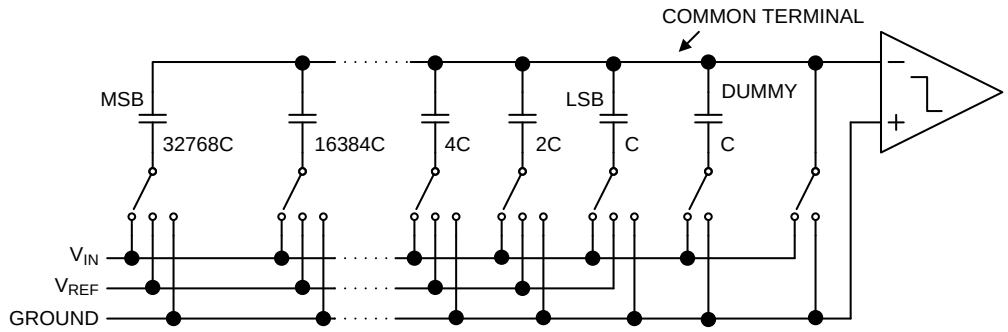


Figure 2.2 A 16-bit capacitive DAC.

trapped on the capacitor array. The free terminals of all the capacitors are then connected to ground, driving the common terminal of the capacitor array to a negative voltage equal to $-V_{IN}$.

At the beginning of the binary search algorithm, the bottom plate of the MSB capacitor is disconnected from ground and connected to V_{REF}. This drives the common terminal in the positive direction by an amount equal to $\frac{1}{2}V_{REF}$. Therefore, $V_{COMMON} = -V_{IN} + (\frac{1}{2} \times V_{REF})$. The comparator output yields a logic 1 if $V_{COMMON} < 0$ (i.e., $V_{IN} > \frac{1}{2} \times V_{REF}$). The comparator output yields logic 0 if $V_{IN} < \frac{1}{2} \times V_{REF}$. If the comparator output is logic 1, then the bottom plate of the MSB capacitor stays connected to V_{REF}. Otherwise, the bottom plate of the MSB capacitor is connected back to ground. The bottom plate of the next smaller capacitor is then connected to V_{REF} and the new V_{COMMON} voltage is compared with ground. This continues until all the bits have been determined. In general,

$$V_{COMMON} = [-V_{IN} + (B_{N-1} \times V_{REF}/2) + (B_{N-2} \times V_{REF}/4) + (B_{N-3} \times V_{REF}/8) + \ldots + B_0 \times V_{REF}/2^{N-1}] \quad (2.1)$$

where $B_{\#}$ is the comparator output or ADC output bits.

Beyond 10 or 12 bits, a calibration scheme is needed to compensate for errors in the DAC capacitors. In one popular scheme, there is a calibration DAC for each capacitor in the MSB array. These DACs are capacitively coupled to the main DAC output and offset the output of the

main DAC according to the value on their digital inputs. The stored code is provided to the appropriate calibration DAC whenever the corresponding bit in the main DAC is 'high'. Calibration is usually initiated by the user or done automatically when the circuit is powered up. To reduce the effects of noise, each calibration experiment is performed many times, and the results are averaged.

2.1.2 The Comparator

Because the internal circuitry must run at roughly N times the converter sampling rate and because a single comparator is responsible for all the of analog-to-digital conversions, the comparator in an SAR ADC is required to be very fast and very accurate. Although comparator offset does not affect the overall converter linearity since it appears as an offset in the transfer characteristic, offset-cancellation techniques are usually applied to reduce it. Also, the comparator is usually designed to have input-referred noise less than 1 LSB. Additionally, the comparator needs to resolve voltages within the accuracy of the overall system.

2.1.3 State-of-the-Art in SAR ADCs

From the previous discussion, it is apparent that the SAR architecture has many advantages such as low complexity, low power consumption, small form factor, with medium-to-high resolution. The biggest drawback of these converters is the limited speed. A decade ago, SAR sampling rates did not exceed 5 MS/S, but with the advancement of CMOS technology and the development of a few architectural variations, designers have been able to extend the sampling rate of SAR ADCs as high as the gigahertz (GHz) range while still taking advantage of some of the benefits of the SAR architecture [13]-[15]. A key feature of SAR ADCs is that they greatly benefit from CMOS technology improvements because most of the design is digital and there is no linear amplification (such as an opamp) required. Therefore, similar to digital circuits,

speeds of SAR converter have increased substantially (up to tens of MHz) simply because of semiconductor technology improvements. In the following sub-sections, a few of the most popular state-of-the-art variations to the SAR architecture will be discussed.

Time-Interleaving

Time-interleaving is a technique that is not unique to SAR converters, but as its main function is to increase the sampling rate, it has found profound use in SAR implementations [11]. Time-interleaving involves having two or more ADCs that operate on different, but defined clock phases. This way, each adjacent conversion is handled by a different ADC, effectively increasing the sampling rate by a factor equal to the number of interleaved converters. The multiple converters work together to simultaneously sample an input signal and produce a combined output signal that results in a sampling rate at some multiple of the individual ADCs. For example, if two converters with a sampling rate of f_S are interleaved, the overall resultant sampling rate is simply $2f_S$. For the interleaving to work properly, the two ADCs must have a clock-phase relationship, which is dictated by Equation 2.2, where 'a' is the specific ADC and 'b' is the total number of ADCs.

$$\Phi_a = 2\pi\left(\frac{a-1}{b}\right) \tag{2.2}$$

Continuing with the two-ADC example, assume two SAR ADCs with a 10 MS/S sampling rate are interleaved to achieve a total sampling rate of 20 MS/S. This means that the clock phase relationship will be $\Phi_1 = 0°$ and $\Phi_2 = \pi = 180°$. A block diagram of a sample interleaved system is shown in Figure 2.3.

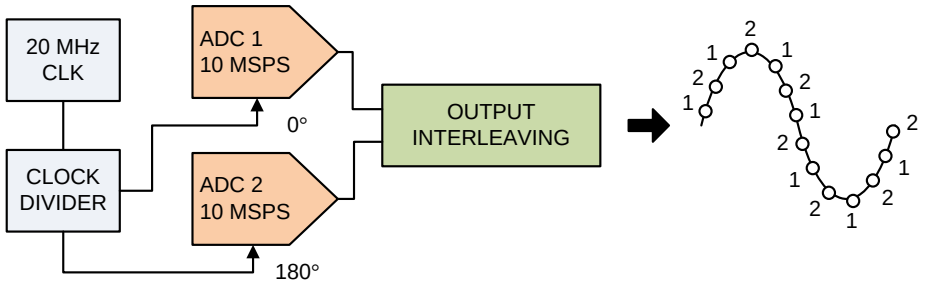


Figure 2.3 Block diagram example of time-interleaved ADC.

There are a number of imperfections associated with interleaving. Most are the result of one or more of 4 different mismatches: offset mismatch, gain mismatch, timing mismatch, and bandwidth mismatch. To understand offset mismatch, consider that each ADC will have an associated DC offset value. As the samples are acquired alternatively between each ADC, the DC offset of each successive sample changes. The output switches between these offset values at a rate of $f_S/2$ which will result in a spur in the output spectrum located at $f_S/2$. In the case of gain mismatch, a spur will occur in the output spectrum that is related to the input frequency as well as the sampling rate at $f_s/2 \pm f_{IN}$. In order to minimize the spur caused by the gain mismatch, the gain of one of the ADCs is chosen as the reference and the gain of the other ADC is set to match that gain value as closely as possible. Timing mismatch has two components, group delay in the analog circuitry and clock skew. The timing mismatch also causes a spur in the output spectrum $f_S/2 \pm f_{IN}$. Finally, bandwidth mismatch has a gain and frequency component, as well as a timing component which causes signals at different frequencies to have different delays through each converter. Bandwidth mismatch between ADCs is minimized through good circuit design and layout technique [16].

Asynchronous Timing

Another technique that is not exclusive to the SAR architecture but has been largely exploited in their designs is asynchronous timing. Usually, there is a global clock that distinguishes the analog input signal acquisition phase and the conversion phase as well as a clock for the internal circuitry. Each bit of the final output code is resolved based on the timing of the internal circuitry clock, as in Figure 2.4. For a high speed design, this could lead to a very power hungry clock generator as well as difficulty in realizing a comparator with adequate performance.

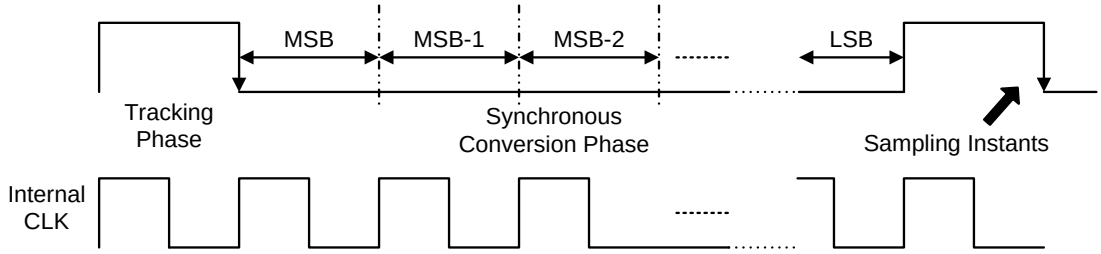


Figure 2.4 Typical timing diagram of an SAR ADC with synchronous timing.

In an asynchronous implementation, however, the internal circuitry operates without a clock and only the global clock is required. Instead of resolving the output bits on internal clock edges, each bit takes only as much time as needed to resolve the logic level and then the next comparison is immediately started. This is depicted in Figure 2.5. The graph on the bottom indicates how it takes variable time to determine each bit of the digital output code. Overall converter sampling rate is increased using asynchronous timing due to the digitized analog sample being available sooner because each comparison is made as soon as the one before it is complete. Additionally, this eliminates the need for a high-speed clock generator which can be too power hungry to be desirable in most applications.

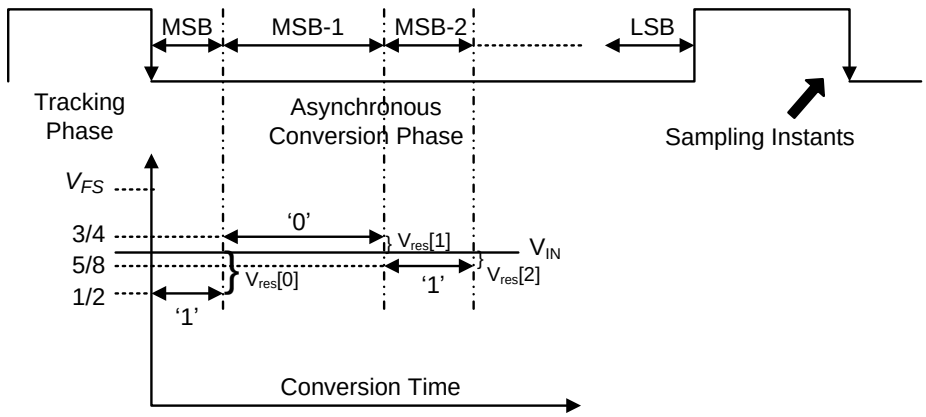


Figure 2.5 Typical timing diagram of an SAR ADC with asynchronous timing.

Multi-Bit Per Cycle

Conventional SAR algorithms utilize one comparison per cycle and thus require at least N (usually N+1) comparison cycles for N-bit resolution. If more comparisons can be accomplished within one comparison cycle, the conversion time will be reduced proportionally. Another way of thinking about it is that the sampling rate of the overall converter can be increased proportionally for a given internal clocking speed. For example, a 10-bit converter with an internal clock running at 500 MHz will have an overall sampling rate of 50 MHz when resolving 1 bit/cycle. But when resolving 2 bits/cycle, the overall sampling rate will be 100 MHz. In recent years, multiple capacitive DACs have been utilized to perform 2 bits/cycle SAR algorithm by generating various reference levels as shown in Figure 2.6 [17]. The comparator offset of a conventional 1 bit/cycle SAR only leads to the global offset without distortion. However, a consequence of adopting a multi-bit per cycle architecture is the vulnerability to the comparator offset, which leads to ADC nonlinearity. Therefore, the multi-bit per cycle SAR architecture is not as power efficient and most likely requires offset cancellation techniques. In

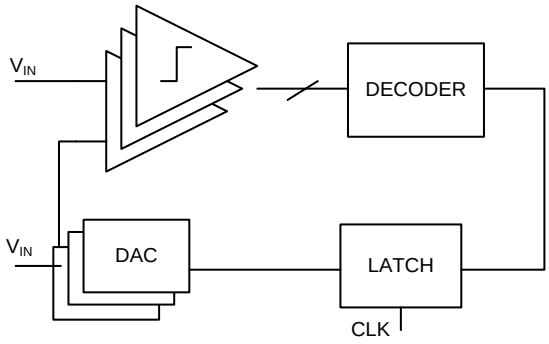


Figure 2.6 Block diagram depiction of a multi-bit per cycle SAR ADC.

addition, to mitigate the drawback of additional capacitive loading, interpolation technique can be adopted with the mixture of resistive and capacitive DACs [18], [19].

2.1.4 Summary

As CMOS technology evolves, the SAR architecture benefits of low power consumption and small area improve with it. Although through device scaling and advanced techniques, SAR sampling rates have increased substantially in the recent past, some of the other benefits have suffered. The power consumption of the SAR converter heavily scales with the sampling rate (Figure 2.7), so as researchers develop ways to increase the sampling rates, the power consumption is quickly reaching levels that are on par or greater than other topologies. SAR ADCs with the best figure-of-merit (FOM) still sample at speeds less than 10 MS/s. Therefore, at this time, SAR converters are still **best** suited for low-to-medium speed applications. As time-interleaving and other sampling rate increasing techniques improve, the SAR architecture will become even more attractive for high-speed applications as well.

2.2 Delta-Sigma ADC

The key feature of Delta-Sigma (ΔΣ) analog-to-digital converters is their ability to produce very high-resolution digital outputs with relatively low power consumption, low cost,

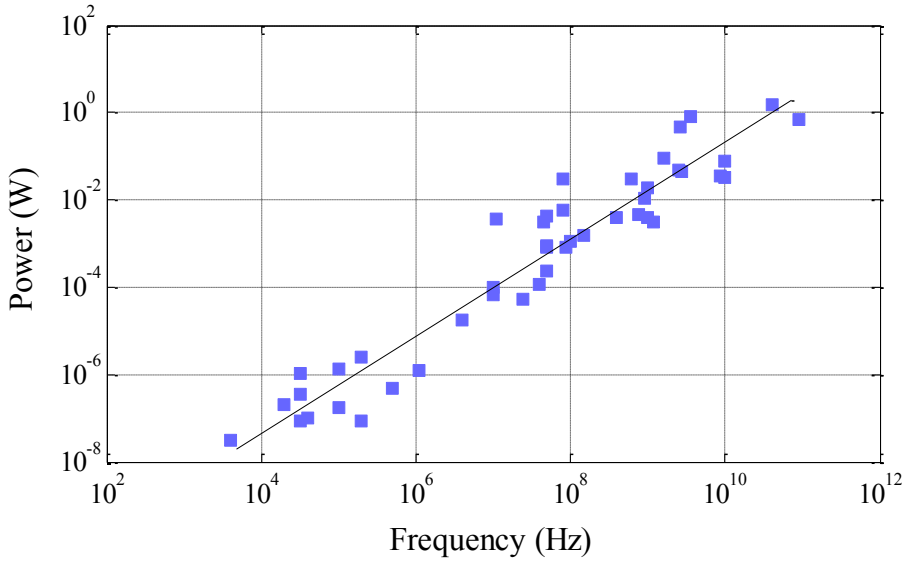


Figure 2.7 SAR ADC power consumption versus sampling rate. The data points were taken from all SAR ADCs published in ISSCC and VLSI journals from 2009 to 2014.

and high integration. Because of the oversampling required to achieve such high signal-to-noise ratio, these converters are usually limited to low-to-medium speed applications. However, similar to the SAR architecture, improvements and changes to the architecture over the years have broken this boundary. ΔΣ ADCs are ideal for applications such as precision temperature measurements, audio applications, and some biomedical sensing applications [20].

The design of a ΔΣ ADC is roughly one-quarter analog and three-quarters digital which makes it inexpensive to produce. The analog portion of the design is generally considered the simplest part and consists of a difference amplifier, an integrator, a comparator, and a 1-bit DAC as shown in Figure 2.8. The 1-bit DAC simply connects one of the two reference voltages to the inverting terminal of the difference amplifier. These components form what is known as a *delta-sigma modulator*. The digital portion of the design includes a digital/decimation filter. This filter is responsible for the large signal-to-noise ratios which is characteristic most ΔΣ ADCs.

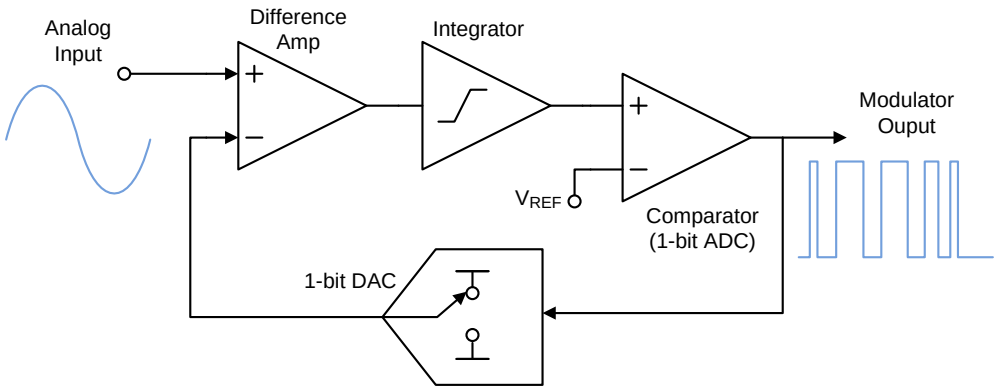


Figure 2.8 Block diagram of delta-sigma modulator.

The block diagram of a ΔΣ ADC is shown in Figure 2.9. The ΔΣ modulator produces a high-speed, 1-bit stream of '1's and '0's. Because of the integrator, the modulator also pushes low frequency noise outside of the bandwidth of interest into a higher band. This is called noise shaping and will be discussed more in detail later. The digital filter function then produces a high-resolution, digital representation of the input signal, and finally, the decimation filter function discards some of the samples to reduce the data rate to a more manageable speed, resulting in the final digital output code. Similar to the SAR architecture, power consumption of ΔΣ ADCs scales with sampling rate as most of the circuitry is digital. In the following

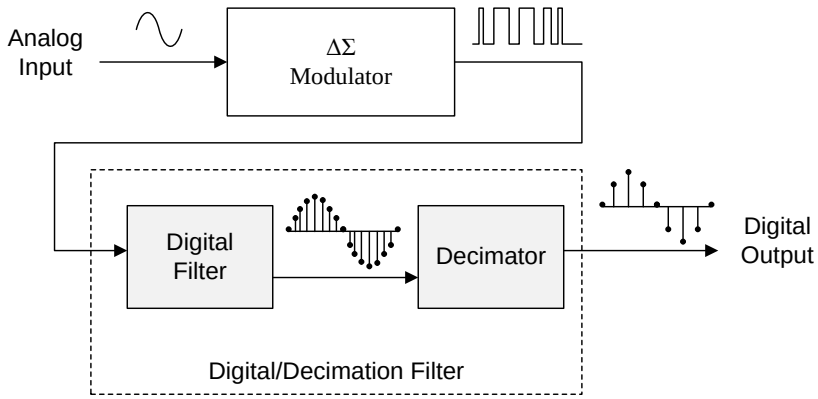


Figure 2.9 Block diagram of delta-sigma ADC.

subsections, critical ΔΣ converter concepts, namely oversampling, noise shaping, digital filtering, and decimation will be discussed.

2.2.1 Oversampling

Oversampling is a technique in which the input signal is sampled much faster than the Nyquist rate, f_S. Doing so spreads the noise energy over a larger spectrum, effectively increasing the resolution of the sampled data. Consider the frequency-domain transfer function of an ADC with a sine-wave input signal. A typical FFT analysis on the digital output will depict a single large tone with lots of random (quantization) noise surrounding it up to $f_S/2$ as shown in Figure 2.10. Because of this quantization noise, the conversion from analog-to-digital loses some information and introduces some error. The magnitude of this error is random, with values up to ±LSB. Ideally, for an N-bit ADC, SNR = 6.02N + 1.76dB. This implies that in order to improve SNR (and consequently the accuracy of signal reproduction) the number of bits must be increased Consider again the above example, but with a sampling frequency increased by the oversampling ratio *k*, to kf_S (Figure 2.10b). An FFT analysis shows that the noise floor has dropped. SNR is the same as before, but the noise energy has been spread over a wider frequency range. ΔΣ ADCs make use of this effect by following the modulator with a digital filter, which

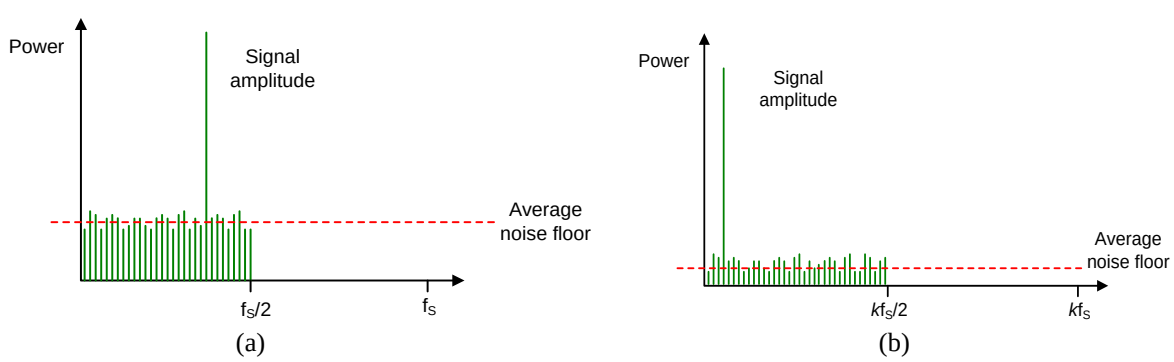


Figure 2.10 Typical output spectrum of ADC with quantization noise from DC to half of the sampling frequency. Noise floor is lowered due to spreading it across a wider spectrum.

removes noise outside of the band of interest, decreasing the RMS noise. This action enables ΔΣ converters to achieve wide dynamic range from a 1-bit ADC. Note that each factor-of-4 oversampling increases the SNR by 6dB, and each 6dB increase is equivalent to gaining one bit of resolution. A 1-bit ADC with k = 12 achieves a resolution of three bits, and to achieve 16-bit resolution, an oversampling factor of 415 must be used, which is not realizable. However, ΔΣ converters overcome this limitation with noise shaping, which enables a gain of more than 6dB for each factor of 4x oversampling.

2.2.2 Noise Shaping

Recall that one of the blocks in the delta-sigma modulator is the integrator which is responsible for noise shaping. Consider, again, the block diagram of a delta-sigma modulator (Figure 2.9). The purpose of the feedback DAC is to keep the average of the output of the integrator close to the comparator reference voltage. At the time that the output of the comparator switches from 'high' to 'low' or vice versa, the 1-bit DAC responds by changing the input reference voltage into the difference amplifier. This creates a different output voltage from the amplifier, causing the integrator to progress in the opposite direction. This time-domain output signal is a pulse-wave representation of the input signal at the sampling rate (kf_S). For an

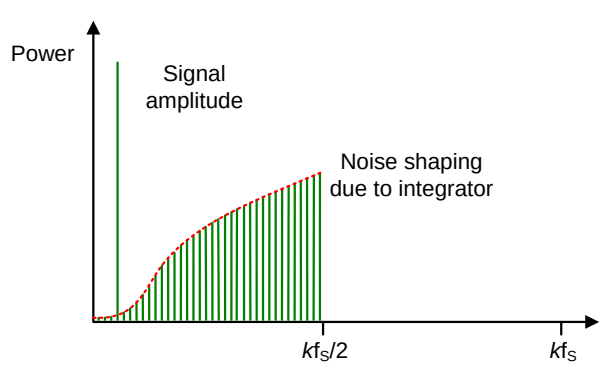


Figure 2.11 Typical output spectrum with noise shaping due to integrator.

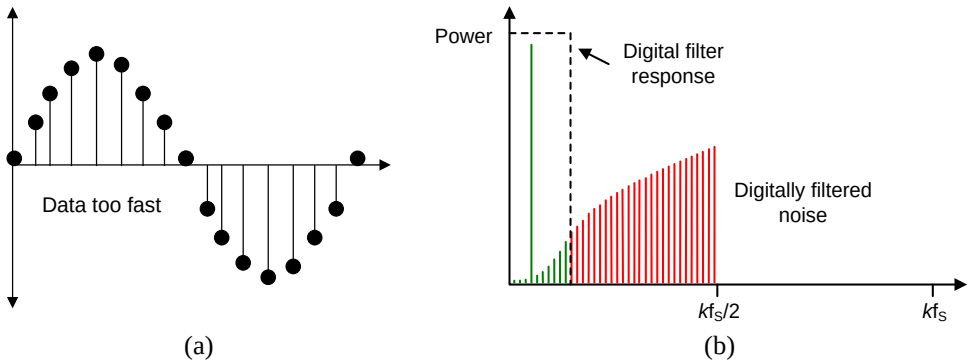


Figure 2.12 Output of the digital filter in the time domain (a) and frequency domain (b).

increasing input signal, the comparator generates a greater number of '1's, and for a decreasing signal, it generates less '1's. By summing the error voltage, the integrator acts as a low-pass filter to the input signal and a high-pass filter to the quantization noise. Thus, most of the quantization noise is pushed into higher frequencies as shown in Figure 2.11. To shape the noise even more, i.e. "push" more noise out of the band of interest into high frequencies, multi-order modulators can be used by including more integration and summing stages [21], [22]. For example, a 3rd order modulator will have three integration stages.

2.2.3 Digital/Decimation Filter

The digital-filter function implements a low-pass filter by first sampling the modulator stream of the 1-bit code. An averaging filter is the most common filter technique used in ΔΣ converters, and in most cases sinc filters are used. A sinc filter ideally removes all frequency components above a designated cutoff frequency, without affecting lower frequencies. In the time domain, the filter's impulse response resembles the sinc trigonometric function, and its frequency response is a rectangular function. Their notch response in the frequency domain is what these particular filters are so widely used. The output rate of a digital filter is the same as the sampling rate. Figure 2.12 shows the effect of the digital filter. In the time domain (Figure

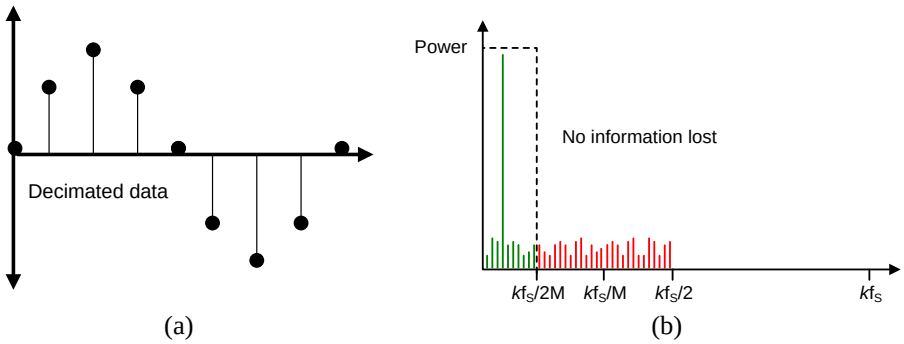


Figure 2.13 Digital output after decimation (a) in the time domain (b) and frequency domain.

2.12a), the digital filter is responsible for the high resolution of the ΔΣ converter. In the frequency domain (Figure 2.12b), the digital filter applies only a low-pass filter to the signal. In so doing, it not only attenuates the quantization noise of the modulator but also reduces the output bandwidth. With the quantization noise reduced, a high-resolution, digital signal re-emerges in the time domain, but it is still too fast to be useful.

The second function of the digital/decimation filter is to "decimate" portions of the output data by discarding some of the samples as illustrated in Figure 2.13. According to Nyquist theorem, the signal after discarding some of the samples does not lose any information from the signal before decimation. The decimation ratio, M, can have any integer value, provided that the output data rate is more than twice the signal bandwidth. If the input has been sampled at f_S, the filtered output data rate can therefore be reduced to f_S/M without any loss of information.

2.2.3 State-of-the-Art in Delta-Sigma ADCs

Previously, ΔΣ converters were designed for low-frequency, high-resolution applications in which case they clearly outperform the other topologies. Recently, these converters are finding application in medium-to-high speed applications that require less resolution. That being said, the strength of ΔΣ ADCs will always be their large dynamic range. Much of the research in ΔΣ

converters focuses on ways to increase dynamic range, bandwidth, or both. In the following sub-sections, some of the more relevant work in these areas will be discussed.

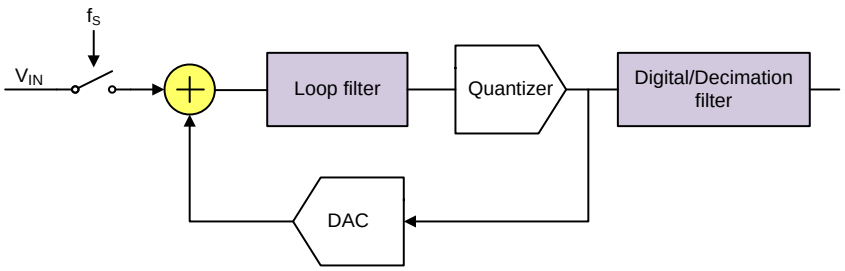
Continuous-Time Delta-Sigma Modulator

The earliest ΔΣ ADC introduced in 1962 was actually a continuous-time (CT) ΔΣ converter [23]. However, once the discrete-time (DT), switched-capacitor ΔΣ converter was developed, it became the dominant topology. Recently, continuous-time converters have gained more attention because of the inherent benefits associated with them and their usefulness in communications applications. These benefits include:

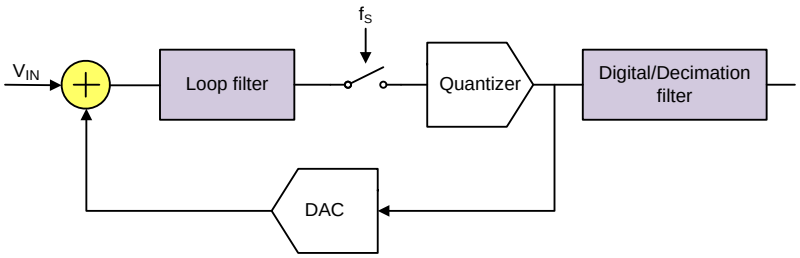
- Increased power efficiency and lower power consumption for a given noise performance
- An alias-free Nyquist band
- A non-switching input which is easier to drive and couples less noise into the system
- Easier migration to future CMOS processes

Continuous-time converters differ from their discrete counterparts in two main ways. First, CT modulators use continuous-time integrators rather than discrete-time circuits. Instead of the switched-capacitor loop filter, the CT ΔΣ modulator often uses RC or g_m/C integrators. Secondly, in a CT modulator, sampling takes place just before the quantizer, after the loop filter whereas in the discrete version, sampling occurs before the loop filter. This is illustrated in the block diagrams in Figure 2.14.

The benefits of a continuous-time system do not come for free. The CT architecture can only be used with a fixed clock frequency because the pole locations of the integrators do not scale with frequency. The signal transfer function for a CT ΔΣ ADC is not flat as is the case with discrete converters. This limits the functional input signal range of the converter. Continuous-time converters also have limited common mode input range because of the limited common



(a) Discrete-time



(b) Continuous-time

Figure 2.14 Block diagrams illustrating the difference between discrete-time and continuous-time delta-sigma converter. In discrete (top), Sampling takes place before filtering, and in continuous (bottom), sampling takes place after loop filter.

mode rejection ratio caused by mismatch in the input transconductance. Lastly, since most CT converters use a continuous-time feedback DAC, they are more susceptible to clock jitter than discrete-time converters.

Multi-Bit Quantizers

As previously stated, the key feature of ΔΣ ADCs is their high dynamic range. For decades, designs have increased dynamic range by increasing the modulator order; however, at some point the improvements can be outweighed by instabilities. Recently, an alternative method for further increasing the modulator dynamic range has gained more attention in research. It consists of using embedded quantizers with larger resolution. Classically, the ΔΣ modulator would output a 1-bit data stream that was then averaged by the digital filter. With a multi-bit quantizer, the modulator will output a multi-bit data stream instead. The main advantages of a

multi-bit quantizer are that the internal nonlinearities are less evident, the quantization noise power for the band of interest is approximately 6 dB lower per additional bit in the embedded quantizer, and the stability properties are better for a given order loop filter.

The benefits previously listed suggest that, for a target modulator performance, multi-bit quantization can be traded for oversampling and noise shaping. In fact, multi-bit ΔΣ modulators are often utilized in wideband applications, since the oversampling ratio can be lower than in the 1-bit versions. As a result, the operation frequency, and therefore, power consumption are reduced for the entire ΔΣ converter. Apart from the added circuit complexity when moving to a multi-bit quantizer, another major drawback is a decrease in linearity. 1-bit quantizers are intrinsically linear because the quantization process uses only two levels. However, multi-bit quantizers present some nonlinearity in their transfer characteristic mostly due to mismatch [24].

VCO-Based Delta-Sigma ADC

Because ΔΣ ADCs are mostly digital, researchers have looked for ways to exploit the continuous scaling of CMOS technology in their design. Recently, voltage-controlled oscillator (VCO)-based ΔΣ ADCs have emerged as an attractive solution due to the highly digital intensive circuit architecture, inherent noise shaping characteristic, and anti-aliasing property [25]. VCO-based ΔΣ ADCs utilize a VCO as a multi-bit quantizer as shown in Figure 2.15. Many of the nonlinearities associated with the VCO voltage-to-frequency tuning curve are dampened by placing the VCO within an analog feedback path. The inherent noise-shaping property of the VCO quantizer also adds an additional order of noise shaping to the modulator output [26]. Additionally, no analog comparator is required because of the VCO quantizer. However, the VCO nonlinearities, although suppressed by the analog feedback path, still limit the performance of these converters. At present, the VCO is forced to be used on the back end, at the last stage of

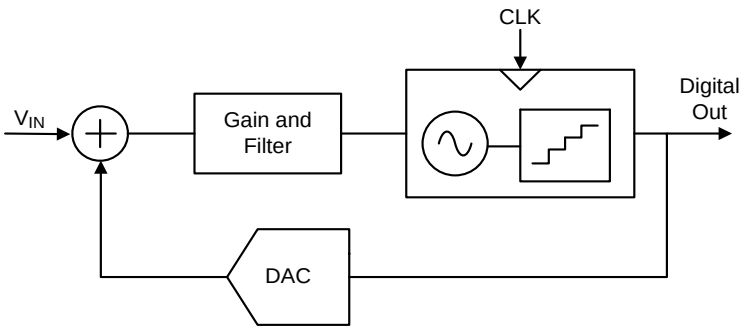


Figure 2.15 Block diagram of VCO-based delta-sigma converter.

the ΔΣ modulator, while high-performance gain and filtering block such as RC integrators are still required at the front end. A highly linear feedback DAC is also required.

2.2.4 Summary

Delta-Sigma ADCs were the saving grace for systems that required high precision. Now, researchers are focused on extending the application of these converters. Extending the operation speed of ΔΣ ADCs usually comes at the cost of resolution as the bandwidth of many of the recent works on these converters are in the range 10-100 MHz with effective resolutions of about 10-12

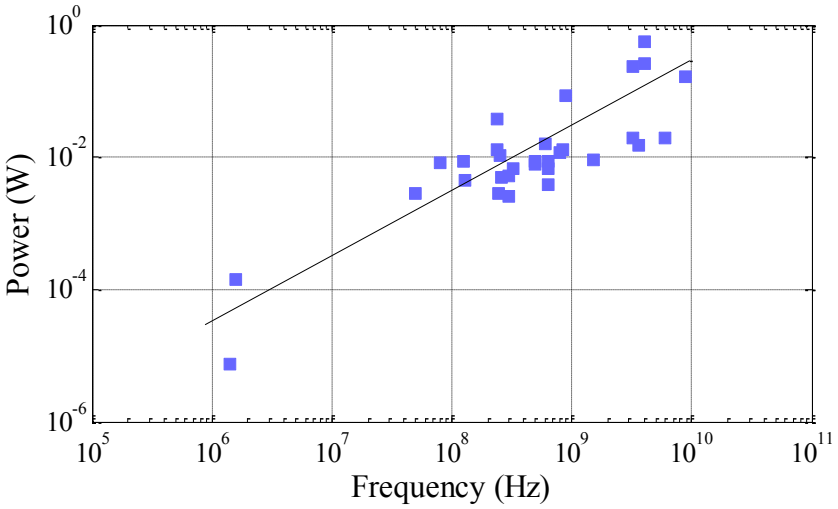


Figure 2.16 Delta-Sigma ADC power consumption vs. sampling rate. The data points were taken from all ΔΣ ADCs published in ISSCC and VLSI journals from 2009 to 2014.

bits [11]. Similar, to the SAR architecture, ΔΣ power consumption scales with operation speed (Figure 2.16), so as faster converters are developed, although FOMs are not necessarily getting better.

2.3 Pipelined ADC

Pipelined analog-to-digital converters have become the most popular ADC topology for medium-to-high speed applications with resolutions from about 8 bits to 14 bits. Pipelined converters are usually used when sampling speeds are too fast for the SAR architecture and not fast enough to warrant a flash architecture, or conventionally, sampling rates ranging from a few MS/s to roughly 100 MS/s. When these converters are designed well, they can exhibit good time-domain performance such as bandwidth, setting time, and noise as well as good frequency-domain performance such as THD and SFDR. Because of these characteristics pipelined converters have found use is a wide spectrum of applications including communications, data acquisition, and CCD imaging [27].

A block diagram of a typical pipelined ADC is shown in Figure 2.17. It consists of a line of virtually identical stages connected in series and an alignment block to combine the final

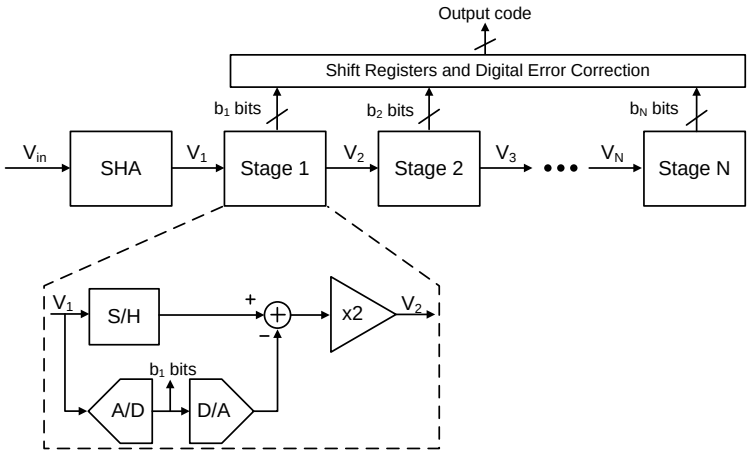


Figure 2.17 Pipelined ADC architecture.

digital output code. The analog input signal is sampled and held while a coarse A/D conversion by a (flash) sub-ADC is carried out. The resolution of the coarse analog-to-digital converter is a design decision based mostly on application although most converters employ a 1.5 bit architecture which will be discussed more in detail later. The digital bits of the sub-ADC are fed to a DAC whose output is subtracted from the sampled analog signal. This creates a "residue" voltage that is then multiplied by an integer factor and fed to the next stage which does the exact same operation as the stage before, but on the residue voltage. The residue voltage propagates through all of the stages, resolving the least significant bits of the output code further along the pipeline until it reaches the final stage. Shift registers align all of the bits of the digital output since they were determined at different points in time after which a digital error correction circuit removes any redundancy that was built into the code. It should be pointed out that, the name "pipeline" comes from the fact that once a stage has performed its operation on a sample and passed the residue on to the next stage, it can work on the next sample to be processed. This is responsible for the high throughput associated with pipelined converters. Conversely, since an analog sample must propagate through each stage before the bits can be combined there is some latency between the sampled input and the corresponding digital output code. The latency is dependent on the number of stages used in the pipeline and is not a major issue in most applications [28].

2.3.1 Component Accuracy

As it turns out that for an N-bit pipelined ADC, only the first stage needs N-bit accuracy. Subsequent stages can get by with less accuracy (depending on how many bits per stage are resolved) because each stages error is divided by the gain of its preceding stage. For example, the first stage of a 12-bit pipelined converter that resolves 2 bits per stage will need 12-bit accuracy.

Stage 2 needs 10-bit accuracy, 8-bit for stage 3, 6-bit for stage 4, and so on. Designers usually take advantage of this by gradually decreasing the power of each stage. The sample-and-hold circuit, DAC, subtractor, and gain amplifier form what is known as a multiplying DAC (MDAC). The main limitation to high resolution accuracy within an MDAC is capacitor mismatch. This is why pipelined converters with resolutions above 10 bits typically require some form of calibration or trimming [29], [30]. However, today many pipelined architectures with medium resolutions (10 bits or lower) include calibration anyway to improve performance as will be seen later. The sub-ADC (and the comparators used to construct them) in each pipeline stage does not require the same accuracy as the stage they are associated with. Instead, the digital error correction logic reduces the accuracy needed from these blocks.

2.3.2 Digital Error Correction

Most, if not all, modern pipelined ADCs make use of digital error correction to reduce the accuracy requirement of the flash ADCs in each pipeline stage. Therefore, designers can focus on minimizing power for a desired speed. If a comparator in the sub-ADC in one of the early stages of the pipeline has substantial offset, a digital code that does not accurately represent the analog input signal could be produced, and thus an incorrect DAC output would result, producing an error in the residue voltage. It has been proven that as long as the gained-up residue for a single stage does not exceed the range of the subsequent sub-ADC, the LSB code generated by the remaining stages will still give the correct overall output code. This implies that that none of the sub-ADCs have to be as accurate as the entire ADC. Consequently, digital error correction does not affect the last stage in the pipeline, but in this case, the error is divided by the gains of all stages before it, inherently reducing the accuracy requirement of the last stage sub-ADC. Another factor that helps reduce the accuracy requirement of each sub-ADC is redundancy. For

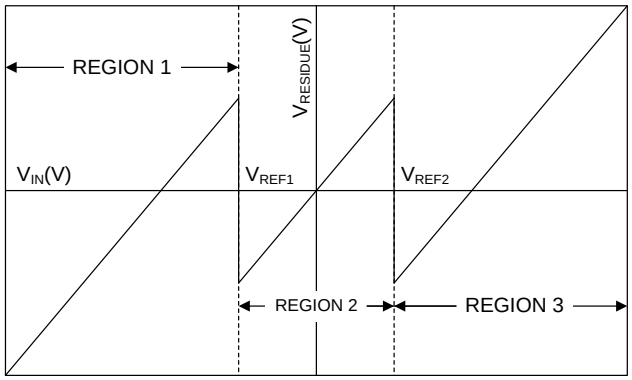


Figure 2.18 Transfer function of 1.5 bit per stage architecture. $V_{IN}(V)$ is the differential analog input voltage. $V_{RESIDUE}$ is the differential analog output of stage n (and input to stage n+1).

example, a 3-bits/stage architecture will actually resolve 2-bits of the final output code per stage with 1 bit of redundancy. The extra bit reduces the size of the residue by one half, allowing extra range in the next sub-ADC for digital error correction.

2.3.3 1.5 bits per Stage

The 1.5-bits-per-stage architecture has emerged as one of the most popular implementations of a pipelined converter. It offers increased accuracy because of the half bit of redundancy while consuming less power than higher bits-per-stage implementations. In this scheme, a 1.5 bit flash ADC compares the analog input to two different comparator thresholds, V_{REF1} and V_{REF2}. The ADC then gives a digital output corresponding to the region in which the analog input falls. The 1.5-bit indicates that there are three regions on the $V_{RESIDUE}$ vs. V_{IN} transfer characteristics as indicated in Figure 2.18. For comparison, a 1-bit ADC would have one comparator and two regions (1 or 0), and a 2-bit ADC would have 3 comparators and four regions (00, 01, 10, and 11) on the transfer characteristics. Depending on the region in which the input to the sub-ADC falls, the residue voltage is calculated as follows and is fed to the next stage as the input voltage:

- $V_{RESIDUE} = 2V_{IN} - V_{REF}$, for $V_{IN} > V_{REF2}$
- $V_{RESIDUE} = 2V_{IN}$, for $V_{REF1} < V_{IN} < V_{REF2}$
- $V_{RESIDUE} = 2V_{IN} + V_{REF}$, for $V_{IN} < V_{REF1}$

Although 1.5 bits per stage is one of the most popular implementations for pipelined converters, it is not the only one. For some designs, the number of bits per stage is determined by the sampling rate and resolution. In general, higher speed pipelined ADCs tend to favor a lower number of bits per stage, because it is difficult to realize wideband amplifiers with high gain. Conversely, lower sampling rate pipelined ADCs tend to favor more bits per stage. This results in less data latency.

2.3.4 State-of-the-Art in Pipelined ADCs

Time-Interleaving

Time-interleaving has already been discussed earlier in the SAR ADC section, and all of the same concepts apply. Time-interleaved pipelined converters have the same goal of achieving faster sampling rates by interleaving multiple, slower converters. Particularly with the pipelined architecture, time-interleaving can lead to power savings because of all of the circuitry that can be shared, similar to the opamp sharing technique.

(Background) Calibration

Traditionally, calibration was only used in high resolution converters to achieve decent linearity. As CMOS technology is scaled down, lower power digital circuit designs can be realized allowing researchers to develop low-power digital calibration techniques to help improve linearity for medium-resolution pipelined ADCs. There are two schemes for adaptively

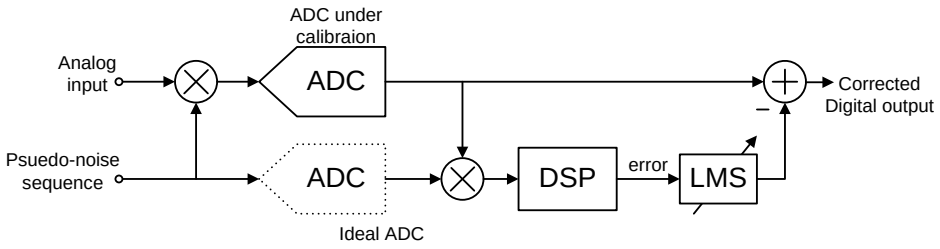


Figure 2.19 Example of a background calibration scheme.

measuring and dealing with an unknown error—foreground calibration and background calibration.

Foreground calibration estimates the unknown errors sources by interrupting normal ADC operation and applying a known input sequence to the ADC. A comparison is made between the expected output and the actual output and the error can be quantified and corrected. The advantage of a foreground scheme is that calibration can be achieved within a small number of clock cycles. The disadvantage of foreground calibration is that the ADC is required to be taken offline every time calibration is performed, which in some applications may not be possible.

Background calibration continuously measures unknown errors within a pipeline stage and corrects their effects. The vast majority of new publications based on calibration focus on background techniques because of the significant advantage over foreground calibration that the ADC is not required to be taken offline. There are many implementations of background calibration in the literature, though at the core of a majority of them, a statistical-based approach is employed [29], [30]. In a statistical scheme, the input of the pipeline stage under calibration is combined with a controlled pseudo-random noise source. Then by correlating the digital output of the ADC with the known pseudo-random noise, the impact of the error can be determined.

Figure 2.19 shows the basic principle of background calibration. The drawback to background calibration schemes is since the digital output of the ADC is highly correlated with the analog input and weakly correlated with the pseudo random sequence, a large number of clock cycles are required to extract the random sequence from the output of the ADC. In fact, in [31] it was shown through empirical data that statistical techniques required on the order of 2^{2N} clock cycles to calibrate gain errors only. For 10-bit linearity approximately one million clock cycles are required to only correct gain errors using statistics based background calibration. Thus while background schemes are popular as they enable continuous operation, the calibration time of background approaches is rather lengthy.

Non-Opamp Based Pipeline Stages

While the opamp is a key component in a pipeline stage, it is generally the most power hungry and it scales poorly with CMOS technology. A lot of current research in pipelined ADCs involves designing stages without the use of opamps, and instead using a circuit that is less power hungry and scales better. One of the more popular non-opamp based implementations uses comparator-based switched-capacitor circuits (CBSC). In conventional switched-capacitor circuits, the opamp is mainly responsible for providing a virtual ground to ensure accurate charge transfer from sampling to feedback capacitors [32]. Instead of using an opamp to generate a virtual ground, CBSC circuits use a comparator in a feedback loop to effectively emulate the functionality of an opamp with a large DC gain. Figure 2.20 depicts a CBSC circuit which provides a gain of two.

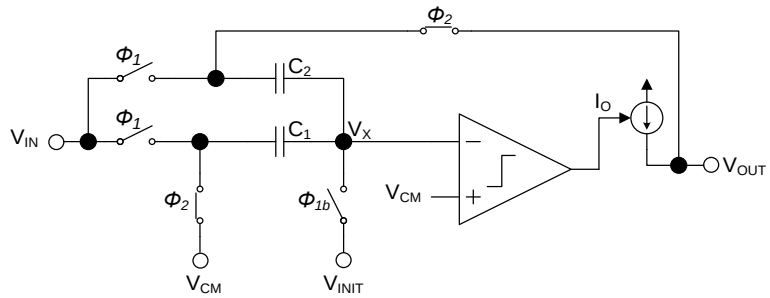


Figure 2.20 Comparator-based switched capacitor circuit implementing a 2x circuit.

During Φ_1, the input is sampled on capacitors C_1 and C_2, and the node V_X is initialized to be below V_{CM}. This is different than the case when an opamp is used in which case V_X would be initialized to V_{CM}. During Φ_2, the current source at the output, I_O, is turned on and V_{OUT} and V_X subsequently increase. When V_X equals V_{CM}, the comparator toggles and turns off the current source I_O, and the node voltages at V_X and V_{OUT} appear the same as if an opamp were used to create a virtual ground at V_X. Thus the CBSC arrangement implements the same functionality as an opamp based arrangement (i.e. gain of 2x).

The significant advantage of CBSC is that the topology does not depend on an opamp which would otherwise require a large DC gain and/or large supply voltage to implement the same functionality in a switched-capacitor circuit. As comparators can be easily designed even

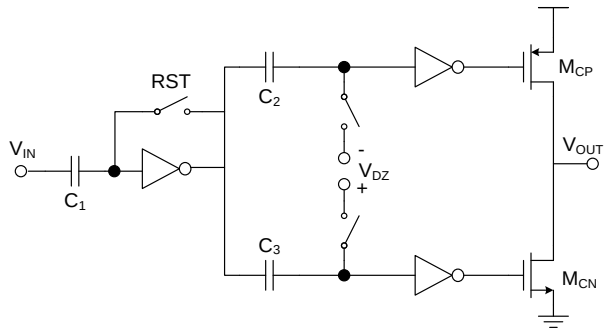


Figure 2.21 Schematic of a ring amplifier.

with low supply voltages and with transistors that have low intrinsic gain, CBSC is well suited for implementation in deep submicron technologies. Furthermore in [33] it is shown that the CBSC approach has less inherent thermal noise than an opamp based approach and thus is able to use smaller sampling capacitors, hence have lower power consumption. One of the drawbacks of CBSC is thus far the technique has only been shown in single-ended form and not the more desirable differential form. As such, it is susceptible to common mode noise.

Another implementation of a non-opamp based pipeline stage is the ring amplifier switched-capacitor circuit. The schematic of a ring amplifier is shown in Figure 2.21. A ring amplifier is created by splitting a ring oscillator into two signal paths and embedding a different offset in each path. When placed in switched-capacitor feedback, a set of internal mechanisms generate stability and allow the oscillator to be used as an amplifier. Ring amplifiers enable efficient amplification in scaled environments and possess the benefits of efficient slew-based charging, rapid stabilization, inherent rail-to-rail output swing, and performance that scale with process technology. There have only been a few reports of ring amplifier based converters to date [34], [35], but it is a promising solution.

2.3.5 Summary

Pipelined ADCs have improved to the point of being able to handle many of the applications that flash converters were previously used for. Since the power consumption of a pipelined converter does not scale closely with sampling rate, the speed improvements do not harm FOM very much. Instead, the power consumption of a pipelined converter mostly scales with resolution, specifically 2^N, and loosely scales with sampling rate. This is illustrated in Figure 2.22. This fact is what allows pipelined converters to have similar resolutions as SAR ADCs but sample much faster and still have a good FOM. Once non-opamp based topologies

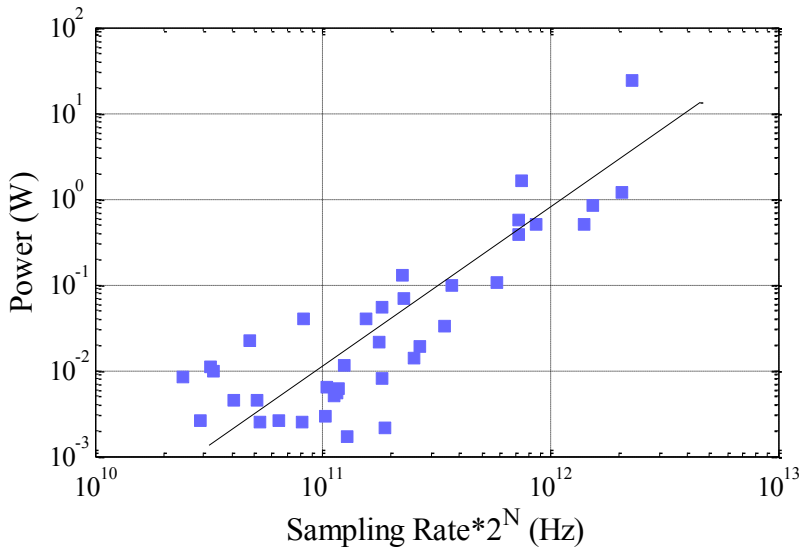


Figure 2.22 Pipelined ADC power consumption versus. sampling rate·2^N. The data points were taken from all pipelined ADCs published in ISSCC and VLSI journals from 2009 to 2014.

develop further and as a result, static power consumption is significantly reduced, pipelined ADCs will exhibit even better performance.

2.4 Flash ADC

Flash analog-to-digital converters, also called parallel ADCs, are perhaps the most straight forward, brute force method of data conversion. Because all of the digital bits are decided at the same time, they are, by far, the fastest way to converter an analog signal to the digital domain. This comes at the cost of power, resolution, and cost. That is to say, flash converters generally are the most power hungry, have the lowest resolution, and occupy the most chip area. These characteristics limit flash ADCs to the highest of frequency applications that cannot be addressed by any other means such as satellite communication, sampling oscilloscopes, and high-density disk drives.

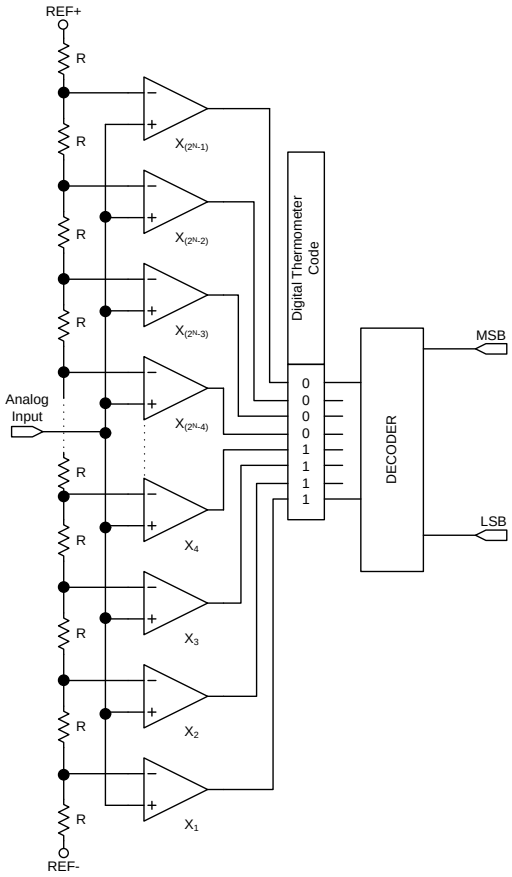


Figure 2.23 Flash ADC architecture.

As Figure 2.23 shows, flash ADCs are constructed by cascading many high-speed comparators along with a large chain of resistive dividers. For a converter with a resolution of N bits, 2^N-1 comparators are required, and a resistive divider consisting of 2^N resistors generates the reference voltages. The resistors are sized so that the reference voltage for each comparator is exactly 1 least significant bit (LSB) higher than the comparator directly below it. When the analog input signal is higher than the reference voltage of a comparator, the comparator outputs a ‘1’, otherwise it outputs ‘0’. The output from the cascade of comparators is called thermometer code. This is because, similar to mercury in a thermometer, the ‘1’s in the output rise until a comparator has a reference voltage that is higher than the input signal, at which point there are

only ‘0’s in the output code. A 2^N-1 to N decoder is then used to transform the thermometer code into the appropriate digital output code.

The comparators in a flash ADC are designed to have low-gain and high-speed because of the difficulty in realizing analog circuitry with both high gain and speed. Special attention is given to minimizing the input voltage offset to be at least smaller than a LSB of the converter. If this was not the case, a comparator could falsely output ‘high’ when it should be ‘low’ resulting in errors in the thermometer code as well as the final output code. An error that is unique to flash converters, namely sparkle codes, is when an out-of-sequence ‘0’ is present in the thermometer code. For example, a typical thermometer code might look like “0001111.” A sparkle code will look like “00010111.” This could be caused by bad input settling or timing mismatch between the cascaded comparators.

Since flash converters are so comparator dependent, they have added vulnerability to metastability. Metastability results in when a digital output is neither ‘high’ nor ‘low’. It is easy to comprehend how this could be a problem. The two common ways to counter metastability in a flash converter is to allow more time for comparator output to settle or to use Gray-code encoding. Also, since these converters handle such high frequencies, it is essential to provide the ADC with a low-jitter clock [36].

For flash converters, the size and power double with each additional bit of resolution. Therefore, power scales with resolution which is in contrast to SAR and delta-sigma converters that scale with sampling rate. The doubling in size with resolution is also in contrast to SAR, pipeline, and delta-sigma converters which increase linearly with resolution. However, conversion time is not affected by resolution for flash converters, whereas conversion time increases linearly with resolution for SAR and pipelined converters.

2.4.1 State-of-the-Art in Flash ADCs

Because the role of the flash converters in data conversion is well defined, not much work has been done on them in research compared to the other analog-to-digital converters. They have been the least published ADC architecture in ISSCC and VLSI journals dating back to 2009 [11]. Most of the state-of-the-art work in flash converters is on reducing power consumption. A smaller amount of research focuses on achieving higher speeds for specific applications. Apart from taking advantage of the inherent speed increase from continuous scaling of CMOS technology, some researchers use time-interleaving to increase the operation speed of the flash converters. Usually coupled with a calibration technique, time-interleaved converters can consume less power than non-time-interleaved converters.

An architectural improvement that has been recently developed is the reduction of the number of comparators. As mentioned previously, for an N-bit flash ADC, usually 2^N-1 comparators are required. But if the number of comparators can be reduced, a significant saving of chip area and power can be achieved. In [37], half of the comparators are replaced with SR latches. The SR latches act as an offset averaging circuit to quantize the input signal. As Figure 2.24 illustrates, each offset averaging latch (OAL) is connected to the outputs of two adjacent comparators and functions as a comparator with built-in, known offset equivalent to the average offset of the two comparators.

Another technique used to reduce power consumption is comparator redundancy. A tradeoff between power, speed, and accuracy usually has to be balanced for flash converter comparators. However, by adding redundancy to the comparators, designers can focus on minimizing power consumption for a target speed, while accepting whatever offset results from

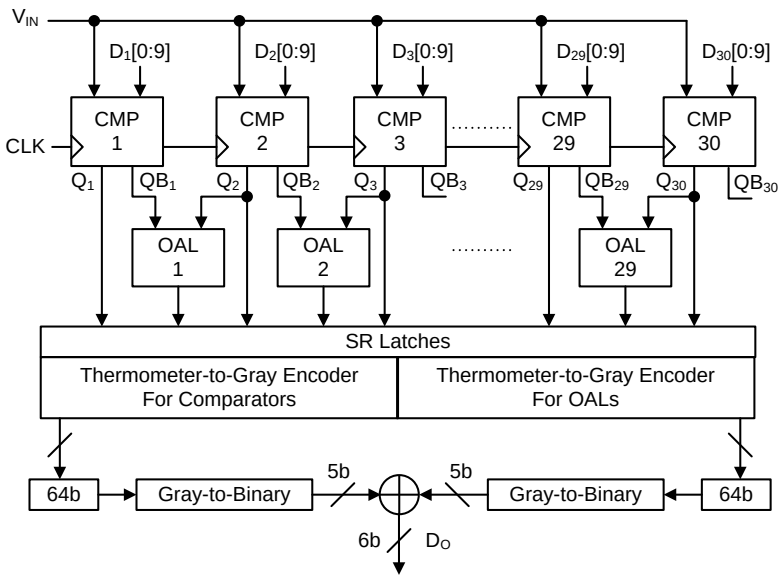


Figure 2.24 Example of a flash ADC that replaces comparators with SR latches (OALs).

it. A calibration technique is needed since the offset can be on the order of several LSBs, but it allows the use of minimum sized devices which saves chip area.

2.4.2 Summary

The role of flash converters has not really changed over the years; they are reserved for the extremely high frequency applications that cannot be handled by any other topology. That being said, the lower limit on when a flash ADC is required is being raised as other topologies are finding ways to sample in the GHz range. Flash ADC power consumption scales mostly with 2^N; basically, for each additional bit of resolution, the power consumption doubles. However, with such high sampling rates, the dynamic power consumption begins to become a factor, so increasing resolution and sampling rate could negatively affect the FOM of the flash converter if not properly designed (Figure 2.25). A few researchers have attempted to reduce the power consumption of the flash converter, but they will more than always only be applicable for the fastest applications.

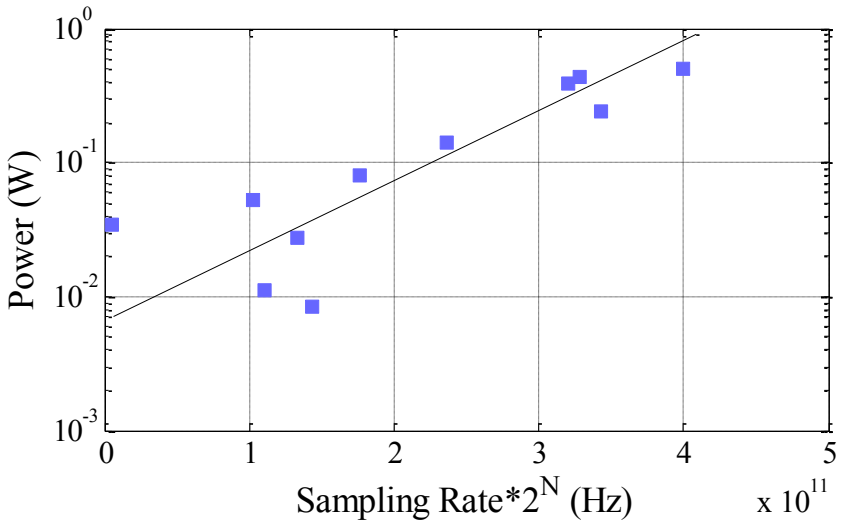


Figure 2.25 Flash ADC power consumption vs. sampling rate·2^N. The data points were taken from all flash ADCs published in ISSCC and VLSI journals from 2009 to 2014.

Chapter 3 – Low-Power and Reconfigurable Data Converters

Analog-to-digital converters are integral components in systems, such as sensor networks, that deal with real world analog signals. Eventually, these signals need to be digitized in order to make sense of the data and more easily interface with electronics. As a result, ADCs have found use in a large variety of applications leading to different optimizations across those applications. A data converter for broadband communications is optimized for high speed operation [38]-[40], while a converter designed for harsh environments, such as jet engine exhaust monitoring or space flights, focuses on a design with extended temperature operation [41], [42]. An ADC designed for implantable electronics is optimized for low power consumption and small form factor [43]-[45]. The converter described in this work can be classified into two categories—reconfigurable data converter and low-power data converter. In the following sections, these two categories will be discussed in terms of implementation, and common concerns with these types of ADCs will be mentioned.

3.1 Reconfigurable Data Converter

Reconfigurable data converters have become more popular in research recently because of their ability to increase power efficiency for systems with variable speed and resolution requirements. The reconfigurable tag refers to the fact that the ADC is able to change its operable sampling rate, resolution, or both after fabrication. The resolution or sampling rate configuration range depends on the requirements of the system for which the converter is being

designed for. Some popular implementations for reconfiguration will be described in the following subsections.

3.1.1 Sampling Rate

The sampling rate of an analog-to-digital converter refers to the rate at which a single analog sample is converted to a digital output. Data converters are typically mixed-signal circuits (they consist of analog and digital circuitry). Since digital circuits can easily operate much faster than analog circuits, the limiting factor in ADC operation speed is generally the analog circuitry, or specifically, the amplifiers and comparators.

Bias Current Scaling

The bandwidth of an amplifier is proportional to the bias current as can be seen from Equations 3.1 and 3.2, assuming square-law saturation operation [71]. Thus, a common method of configuring the sampling rate of a data converter is through adaptive biasing [46]-[48].

$$GBW = \frac{g_m}{2\pi C_c} \tag{3.1}$$

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \tag{3.2}$$

Adaptive biasing, as the name implies, results when the bias currents of the analog blocks are adjusted so that they achieve the desired bandwidth for a conversion. By increasing and decreasing the bias currents, the ADC can more efficiently operate with a higher or lower sampling rate, respectively. One way this is achieved is through digital calibration. In [48], a 4-

bit counter is used to control the bias current of a ramp generator in a comparator-based pipelined architecture. The ramp generator regulates the overshoot voltage of the output of the comparator, so the output settles to its final value in a certain time frame. At lower frequencies, that time frame is greatly extended and so the current of the digitally-controlled ramp generatoris reduced for power efficiency as well as increased linearity because of reduced overshoot. There are many other examples in which the bias currents of amplifiers in conventional architectures are scaled with the help of resistors and switches [49], [50].

Current-Modulated Power Scaling

Another form of sampling rate reconfiguration that does not revolve around excessively scaling bias currents was introduced by Ahmed et al. The technique, known as current modulated power scaling (CMPS), operates under the principle that the outputs are digital although an ADC is a mixed signal system. The analog portion of the circuit only needs to be on long enough to set the digital outputs to the correct logic level. In the mean time, these circuits can be turned off

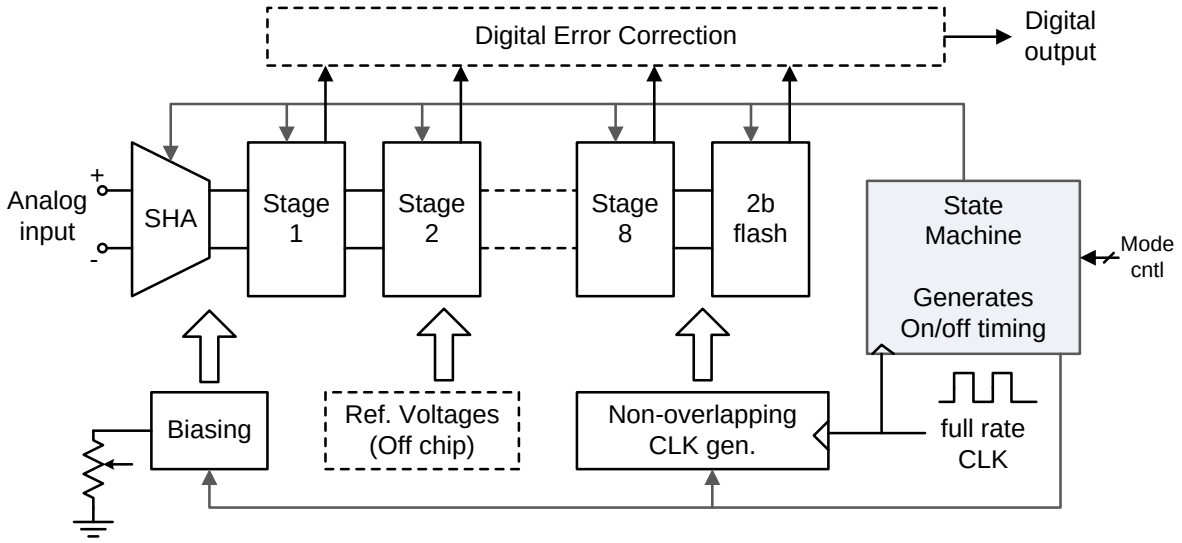


Figure 3.1 Block diagram of Ahmed's reconfigurable pipelined ADC with current modulated power scaling.

until the next input sample is ready for conversion. In this way, at lower sampling rates, the analog portion can maintain the same current, resolve the correct digital output levels, and then shut off for the remainder of the sampling period [51]. A block diagram of the system is shown in Figure 3.1. Using this technique, along with adaptive biasing can result in significant power savings. However, the potential drawbacks of this approach are the precise timing associated with the rapid turning on and off of the amplifiers and also increased system complexity and size.

Interstage Configuration

Another method for controlling sampling rate is by manipulating connections between stages. For example in a time-interleaved architecture, the sampling rate can be configured by altering the number of parallel channels [52] or by using re-sampling. For instance, even stages of a pipelined ADC can be re-sampled by their preceding stages. By re-sampling one time, the sampling rate is reduced to half the clock frequency while by re-sampling twice, the sampling rate will be one third of the clock frequency, and so on [53].

3.1.2 Resolution

Resolution reconfiguration capabilities are generally decided by the ADC architecture. For example, pipelined converter resolution is generally configured by turning on and off either the beginning or ending pipeline stages. This will be discussed in detail later.

SAR converters typically reconfigure their resolution through one of two methods. The first is bit cycling which is when digital control is used to decide the number of clock periods used in a conversion cycle to give the desired resolution [54], [55]. In one form of bit cycling, the most significant bit is resolved and then the remaining bits are resolved until the desired resolution is achieved. This approach is avoided by some because cycling the large MSB

capacitors consumes most of the sub-DAC power so that only linear power savings is achieved [55]. Another way bit cycle is executed is to start in the middle of the array and always cycle to the least significant bit. In this case, switches can be placed at the top plate of the MSB capacitors to decouple them from the sub-DAC resulting in more power savings [55].

The second popular method for configuring SAR resolution is using a variable capacitor array. In this implementation, the large capacitors used to resolve the most significant bits of a digital output code are switched in and out of the charge distribution DAC. Depending on the desired resolution, switches on the top and the bottom of the configuring capacitors will connect or disconnect them from the rest of the array. This inherently involves bit cycling because as the number of capacitors in the array changes, the number of clock cycles used in the conversion will have to change with it.

The resolution of a sigma-delta converter is generally configured using sigma-delta modulation. Decimation filtering and different decimation filters can be selected to configure the resolution. However, this approach is generally reserved for low signal bandwidths because implementing the decimation filters is challenging because of the high oversampling ratio [56], [57].

Systems that include both reconfigurable sampling rates and resolution generally consist of a combination of the aforementioned methods. A least attractive way to accomplish this is to combine two types of ADC architectures into one system. Examples of this are the pipelined/cyclic ADC [46] or the pipelined/sigma-delta ADC [53]. Because many components such as amplifiers, capacitors, and comparators are shared, the area penalty is not too significant. However, circuit complexity is greatly increased, and the system suffers from increased distortion, noise, and lower power efficiency.

3.1.3 Common Concerns of Reconfigurable ADCs

All analog-to-digital converters are susceptible to noise and interference. These sources can greatly affect the linearity and dynamic performance of an ADC. Reconfigurable converters are even more susceptible to noise and interference because of the added wiring, switches, and circuitry required in implementing the different settings. To minimize these possibilities, it is a better practice to minimize the added complexity of the analog portions of the system, and instead, exploit the robustness of digital circuitry [58]. Additionally, reconfigurable data converters must make sure to take advantage of the power-versus-performance tradeoff. There should be a clear advantage to reconfiguring the sampling rate and/or resolution in terms of power efficiency without a significant degradation in performance.

3.2 Low Power ADC

Reduced power consumption has become a necessity for circuit designers across all applications. In particular, bioelectronic circuits aim to utilize a minimal amount of power for reasons such as safety, elongated lifetime, and simplifying power supply schemes. As a result, a number of low power strategies have been applied to the design of analog-to-digital converters in an attempt to achieve a more attractive figure of merit. A few popular, low-power strategies that have been applied to ADC designs will be outlined in the following sections.

3.2.1 Bulk-Driven Technique

The bulk (or body)-driven technique is a technique that allows designers to realize ultra low voltage (and therefore low power) designs. In typical CMOS circuits, the body terminal of the NMOS devices is tied to ground and the PMOS devices to the source or the supply rail. Bulk-driven circuits make use of the bulk terminal of a MOSFET as an AC input. By keeping the gate of the device at a potential which keeps the transistor on at all times, the threshold voltage

limitation is eliminated. This enables ultra low supply voltage designs to be realized. Researchers have used this technique to design low voltage, low power analog-to-digital converters with supply voltages as low as 160 mV [59]. A drawback of this approach is the signal to be digitized must be extremely small in amplitude to be within the dynamic range of the converter. Therefore, this technique can really only be applied to a limited number of applications [60].

3.2.2 Switched-Opamp Technique

Another technique that allows for very low voltage, and consequently low power, designs is the switched-opamp technique. Switched-opamp circuits are a style of switched-capacitor

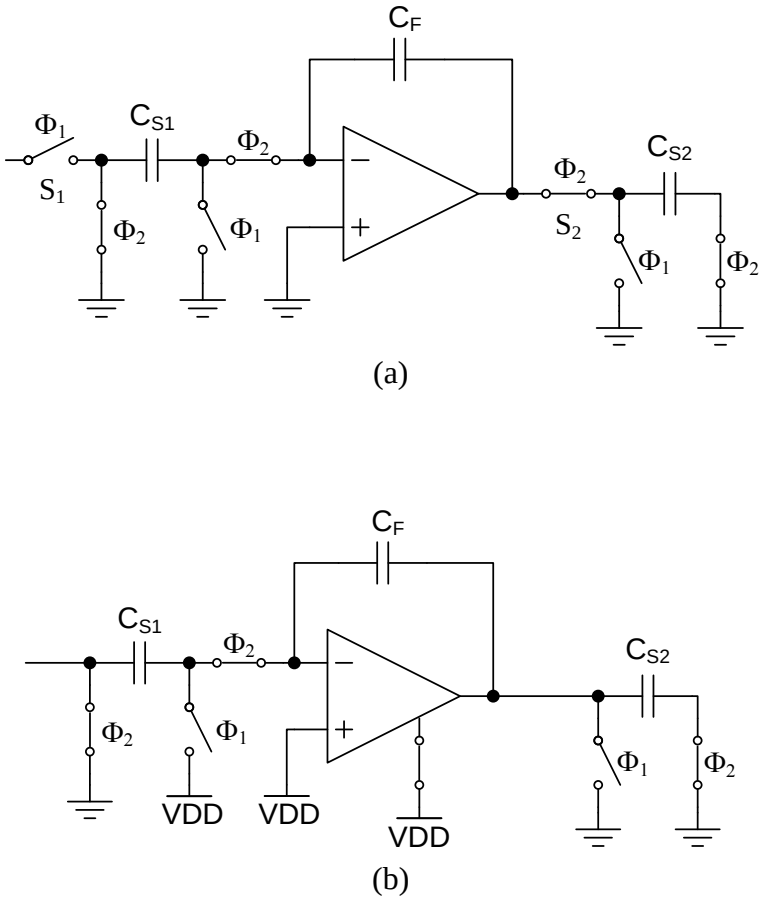


Figure 3.2 Conventional switched-capacitor integrator (a), and a switched-opamp integrator (b). Series input and output switches have been eliminated and output of opamp is made a high impedance node.

circuit that eliminates the problem of insufficient switch transistor overdrive voltage that plagues low supply voltage designs. A typical switched-capacitor circuit is shown in Figure 3.2a. The series switches, S_1 and S_2, are connected to the output of the amplifier which is normally set at $V_{DD}/2$ for maximum output swing. This means that in the worst case, the switch only has an overdrive voltage of $V_{DD}/2 - V_t$. In the switched opamp implementation shown in Figure 3.2b, the series switches are removed, and the output of the opamp is turned into a high impedance node so that it does not resist the pulling of its output to ground. This technique has been implemented in ADCs, particularly the pipelined topology, to realize low-voltage, low-power analog-to-digital conversion [60], [61]. The switched-opamp technique suffers from two main drawbacks. First, in deep sub-micron CMOS process, the threshold voltages do not scale with the supply voltages, so it is difficult to design an input switch over a large dynamic range. Second, the sampling rate of an ADC using this technique is limited by slow transients caused by the turning on and off of the amplifiers. However, the latter problem is less of an issue for most biomedical applications.

3.2.3 Opamp Sharing

Opamp sharing is another technique employed in analog-to-digital converters to reduce power consumption [62]-[64]. Opamp sharing is based on the fact that for a given conversion period with two phases, ϕ and $\bar{\phi}$, the amplifier is only needed for one of those phases for a single stage. Therefore, adjacent stages in a pipelined architecture can share amplifiers so that stage N uses the amplifier during phase ϕ, and stage N+1 uses the amplifier during phase $\bar{\phi}$. This way, the number of amplifiers required for a converter is cut in half resulting in power savings. An example of an opamp-sharing scheme is shown in Figure 3.3. This also suffers from two main drawbacks. First, the additional switches are required to implement this technique adds series

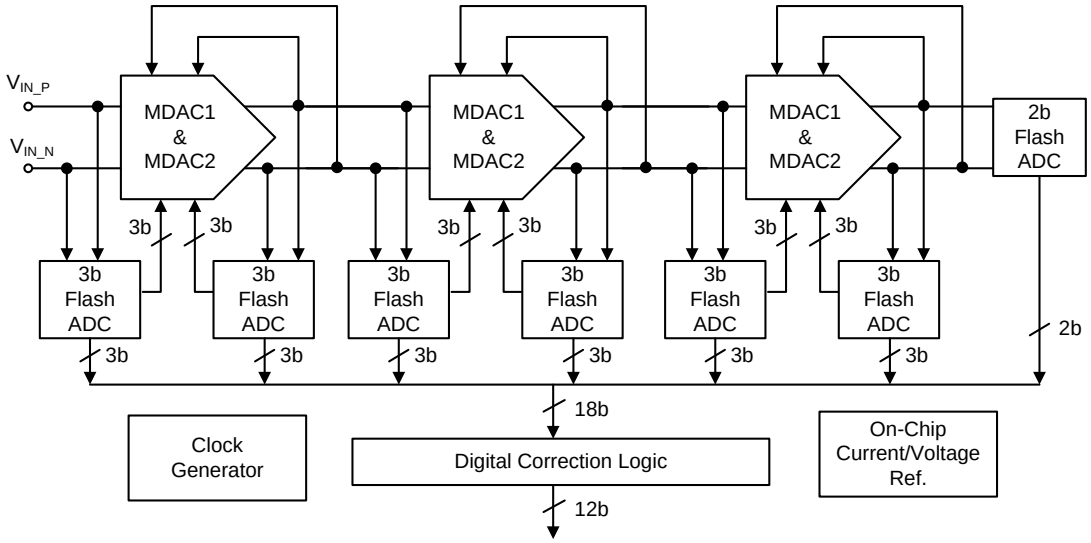


Figure 3.3 Block diagram of pipelined ADC with opamp sharing.

resistance which when coupled with the input capacitance slows the settling behavior of each stage. Second, if the opamp is not allowed enough time to reset before switching between stage N and stage N+1, a previously sampled signal could interfere with the current sample [61].

3.2.4 Subthreshold Design

The final method that will be discussed that has been used to realize low power analog-to-digital converters is subthreshold design. In subthreshold region, or weak inversion, design, the gate-to-source potentials of the MOSFETs are biased below the threshold voltage ($V_{GS} \leq V_{TH}$) of the transistor. Previously it used to be assumed that no current flows through the MOSFET in the cutoff region. Now, it has been proven that there is current flow mostly due to the diffusion (instead of diffraction) of electrons from the drain to the source. A common expression for the subthreshold current of a MOSFET operating in saturation is given in Equation 3.3 [71].

$$I_D = I_{D0} \frac{W}{L} e^{\left(\frac{V_{GS}-V_{TH}}{nU_T}\right)} \tag{3.3}$$

where I_{D0} is the current that flows when $V_{GS} = V_{TH}$, n is a technology specific slope parameter, and U_T is thermal voltage ($kT/q \approx 26$ mV at room temperature). Notice the exponential relationship between the drain current and the gate-to-source voltage. This causes subthreshold region designed circuits to be extremely sensitive to noise and matching. There have been few reports of analog-to-digital converters designed using weak inversion biased transistors [65]. With judicious circuit design and layout, this can be a useful method for realizing low power analog-to-digital converters.

3.2.5 Common Concerns for Low-Power ADCs

The major problems concerned with each technique for realizing low-power analog-to-digital converters were mentioned in each sub section above. In general, for low voltage designs, the dynamic range of the converter becomes a concern, and it limits the applications the converter can be used in. For low current designs, the possibility of noise and PVT (process, voltage, temperature) variations interfering with signals or limiting linearity or dynamic performance of the ADC becomes a concern.

Chapter 4 – Pipelined ADC Architecture

Now that the analog-to-digital converter topologies have been reviewed and the implementations for reconfigurability and low power designs have been discussed, the selection of the pipelined architecture can be justified. Because this particular application is neither an ultra high-speed one nor one that requires very high precision, the flash and the delta-sigma converters were not chosen. The choice is between the SAR and the pipelined. ADCs

On the surface, the SAR architecture is a very attractive option. Generally, it requires the smallest area and consumes the least amount of power. Also, the advancements in CMOS technology have enabled the SAR converters to operate in the tens of megasamples per second range fairly easily. The pipelined architecture usually requires more area and power than the SAR, but has an advantage at higher sampling rates. Figure 4.1 displays a chart comparing figure of merit (FOM) versus effective number of bits (ENOB) for the four major data converter architectures where FOM is defined as,

$$\mathrm{FOM} = \frac{P}{2^{\mathrm{ENOB}} \cdot f_S} \tag{4.1}$$

where P is the power consumption and f_S is the sampling rate. It is quickly obvious that the SAR architecture has the lowest seven FOM values with an ENOB greater than or equal to 8 bits (low FOM is good). SAR converters also achieve the most number of FOM values lower than 100 fJ/conv. Now, let us take a look at Figure 4.2. It is similar to Figure 4.1 except it only includes converters with a sampling rate of 20 MS/s (the target high-speed sampling rate of the proposed converter) or higher. Notice that the pipelined architecture now has the lowest FOM as well as

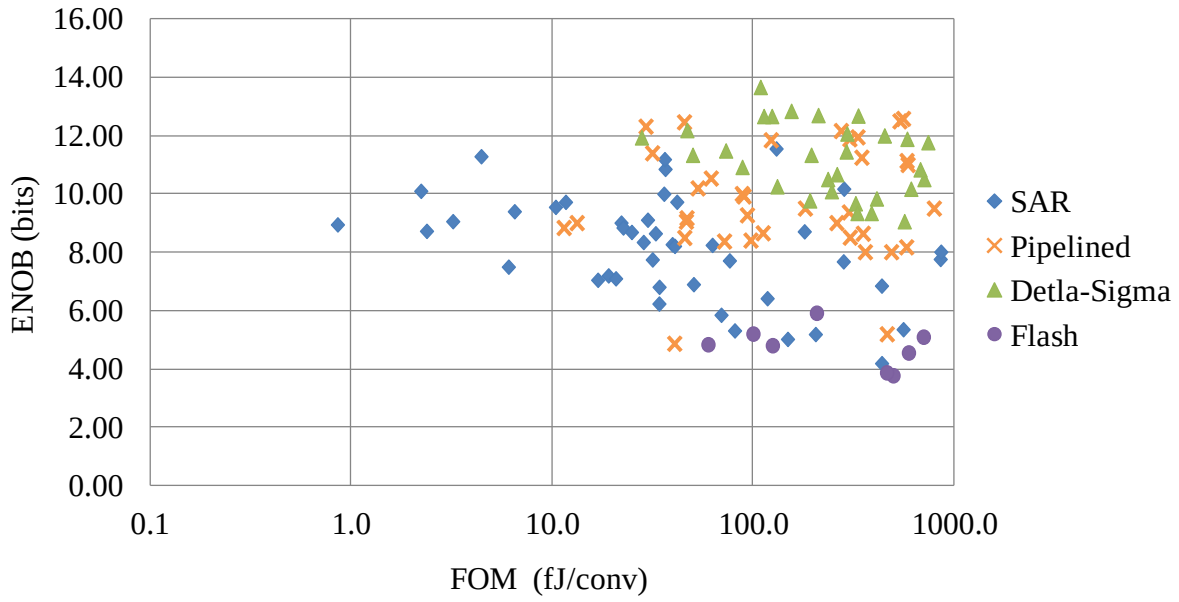


Figure 4.1 FOM versus ENOB for all ADCs published in ISSCC and VLSI from 2009 to 2014.

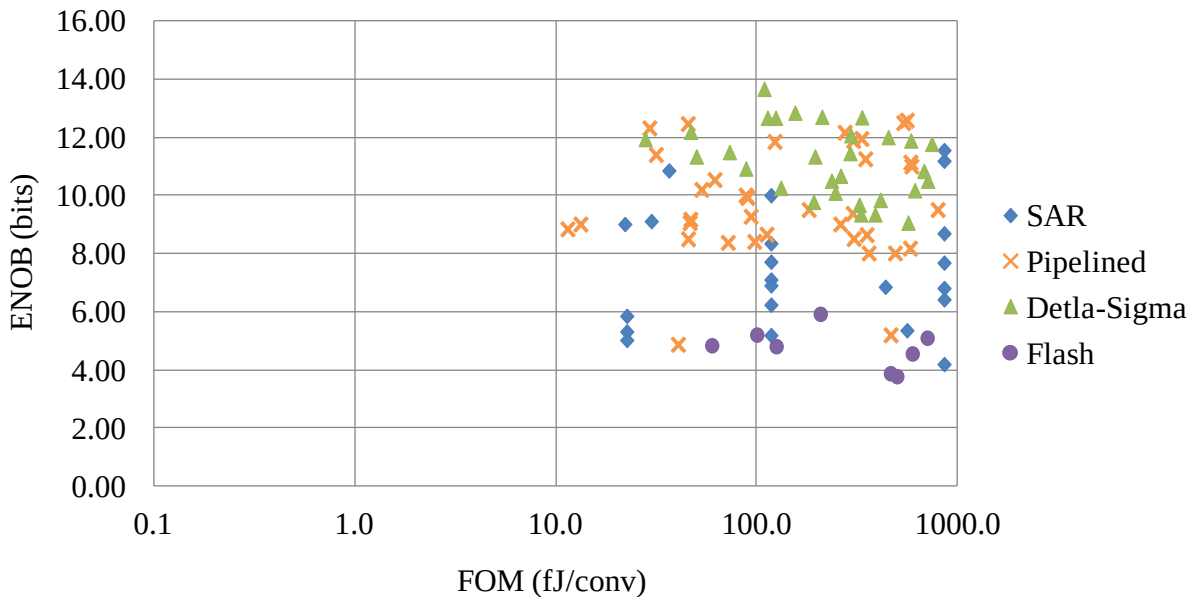


Figure 4.2 FOM versus ENOB for all ADCs with a sampling rate of 20 MS/s or higher published in ISSCC and VLSI from 2009 to 2014.

the most number of FOM values under 100 fJ/conv. Because of this and the ability of the pipelined architecture to be reconfigured more easily than the SAR architecture [66]-[68], the pipelined architecture was selected for this work.

In the remainder of this chapter, performance metrics used to evaluate data converters are described, the conventional pipelined architecture is reviewed, and some of the key sub-circuits of the pipelined converter are discussed.

4.1 ADC Basics

In this section, some of the common terminology, including the static and the dynamic performance metrics, associated with analog-to-digital converters will be described.

Least Significant Bit

In general, the least significant bit (LSB) is the lowest bit in a binary sequence and it is often the right-most bit. In data conversion, a voltage, V_{LSB}, is defined as the voltage change when one LSB changes, or,

$$V_{LSB}=\frac{V_{FS}}{2^N} \tag{4.2}$$

where V_{FS} is the full-scale voltage. With that in mind, an LSB "unit" can be defined as,

$$1\ \text{LSB}=\frac{1}{2^N} \tag{4.3}$$

where N is the resolution of the converter.

4.1.1 Static Error

Static errors are the errors that would affect ADC accuracy if a DC signal were applied to it. It can be summarized by four terms, offset error, gain error, integral nonlinearity, and differential nonlinearity.

Offset and Gain Error

In an analog-to-digital converter, offset error is defined as the difference between the ideal and the actual offset points. The offset point is the mid-step value when the digital output is zero. This error affects all codes by the same amount and can usually be compensated for through calibration or software. It is mathematically defined as [102],

$$E_{off}=\frac{V_{0\ldots01}}{V_{LSB}}-\frac{1}{2}LSB \tag{4.4}$$

Gain error is defined as the difference at the full-scale value between the ideal and actual transfer functions when the offset error has been removed. It is mathematically defined as [102],

$$E_{gain}=\left(\frac{V_{1\ldots1}}{V_{LSB}}-\frac{V_{0\ldots01}}{V_{LSB}}\right)-\left(2^{N}-2\right) \tag{4.5}$$

Gain and offset errors are illustrated in Figure 4.3.

Integral Nonlinearity and Differential Nonlinearity

The integral nonlinearity (INL) is defined to be the deviation from the straight line ideal ADC transfer function after offset and gain errors have been removed.

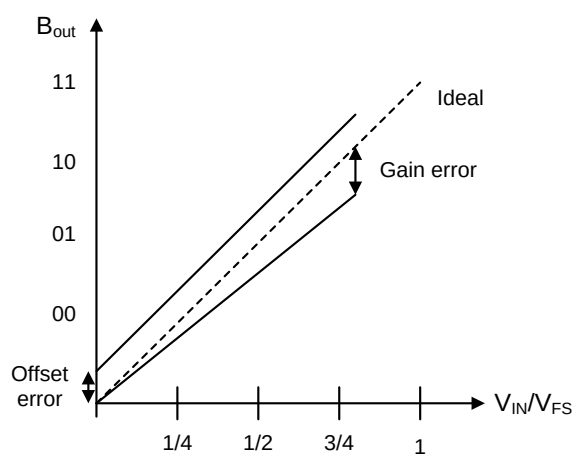
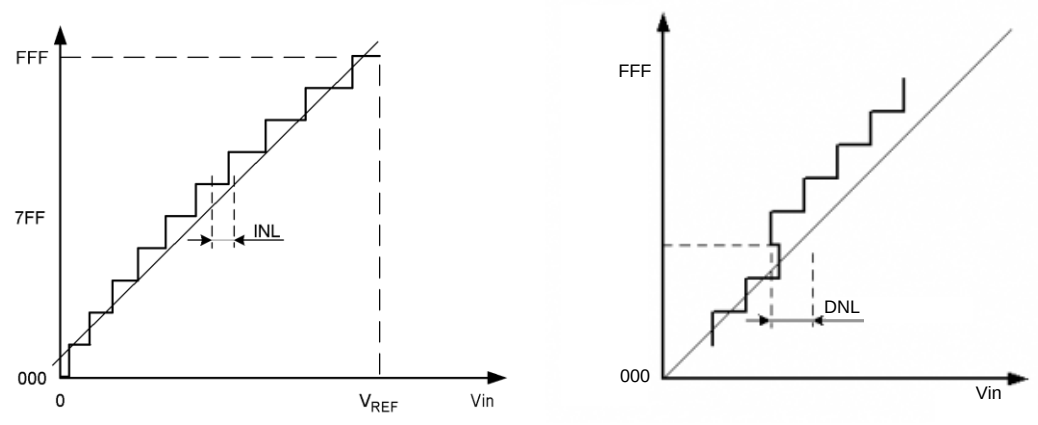


Figure 4.3 Illustrating offset and gain errors for a 2-bit ADC.



(a) (b)

Figure 4.4 Analog-to-digital converter transfer function illustrating integral nonlinearity (a) and differential nonlinearity (b)

To explain differential nonlinearity, consider that in an ideal converter, each analog step size is equal to 1 LSB. Differential nonlinearity (DNL) is the variation in analog step sizes away from 1 LSB typically after offset and gain errors have been removed. Mathematically, DNL and INL can be expressed as [102],

$$DNL(i)=\frac{V_{in}(D_i)-V_{in}(D_{i-1})-\Delta}{\Delta} \tag{4.6}$$

$$INL(i)=\sum_{k=1}^{i} DNL(k) \tag{4.7}$$

Figure 4.4 illustrates INL and DNL for a 12-bit analog-to-digital converter. These errors include noise, mismatch, distortion, and PVT variations. A *missing code* is when a digital output code does not show up in the transfer characteristic during a full scale voltage sweep. An ADC is guaranteed not to have missing codes if the maximum DNL error is less than 1 LSB or if the maximum INL error is less than 0.5 LSB.

4.1.2 Dynamic Performance

Signal-to-Noise Ratio

The signal-to-noise ratio (SNR) is a comparison of the root-mean-square (RMS) input signal power to the RMS noise power. It indicates how weak of a signal can be converted. Assume that V_{IN} is a sinusoidal signal between 0 and V_{ref}. Therefore, the AC power of the sinusoidal wave is $V_{ref}/(2\sqrt{2})$, which results in [102],

$$\mathrm{SNR} = 20\log\left(\frac{V_{in(RMS)}}{V_{Q(RMS)}}\right)$$

$$= 20\log\left(\frac{V_{ref}/\left(2\sqrt{2}\right)}{V_{LSB}/\left(\sqrt{12}\right)}\right)$$

$$= 20\log\left(\sqrt{\frac{3}{2}}2^{N}\right)$$

$$\mathrm{SNR} = 6.02N+1.76\ \mathrm{dB} \tag{4.5}$$

For example, a 12-bit converter has a best possible SNR of about 74 dB. However, note that Equation 4.5 gives the best possible SNR for an N-bit ADC. In practice, this number is impossible to achieve due to errors such as noise and mismatch.

Signal-to-Noise-and-Distortion Ratio

Signal-to-noise-and-distortion ratio (SNDR) is very similar to SNR except it includes harmonics. Therefore, SNDR is a ratio of the RMS input signal power to the RMS noise plus distortion power. It can be expressed as,

$$\mathrm{SNDR} = 10\log\frac{\text{Signal Power}}{\text{Noise and Distortion Power}} \tag{4.6}$$

SNDR is a good indication of the overall dynamic performance of an analog-to-digital converter because it includes all of the components that make up noise and distortion.

Effective Number of Bits

SNDR is often converted to effective number of bits (ENOB) because it is a more physical representation of the performance of a converter. Ideally, an analog-to-digital converter will have 2^N signal levels for an N-bit converter. ENOB specifies the resolution of an ideal converter that would have the same resolution as the actual converter with all of its noise and distortion. ENOB can be found using Equation 4.7 [102].

$$\text{ENOB} = \frac{\text{SNDR-1.76}}{6.02} \tag{4.7}$$

Spurious-Free Dynamic Range

The spurious free dynamic range is the ratio of RMS fundamental signal power to the power of the strongest spurious frequency at the output. A spur is a harmonic distortion component. SFDR is important because it represents the smallest signal that can be distinguished from a large interfering signal. SFDR can be expressed as,

$$\text{SFDR}=10 \log\left(\frac{\text{Fundamental amplitude (RMS)}}{\text{Largest spur amplitude (RMS)}}\right) \tag{4.8}$$

Total Harmonic Distortion

Total harmonic distortion is the ratio of the total power of the second and all higher harmonic components to the power of the fundamental frequency, or mathematically,

$$\begin{aligned}\text{THD} &= 10 \log\left(\frac{\text{Harmonic power}}{\text{Fundamental power}}\right)\\ &= 10 \log\left(\frac{V_{h2}^2+V_{h3}^2+V_{h4}^2+\cdots}{V_f^2}\right)\end{aligned} \tag{4.9}$$

Dynamic Range

The dynamic range of a converter is defined as the ratio of the RMS value of the maximum amplitude input sinusoidal signal to the RMS output noise plus distortion measured when the same sinusoid is present at the output. In other words, it is the range between the noise floor and the maximum output level. For example, an ADC with a dynamic range of 60 dB can resolves signal amplitudes from x to 1000x.

4.2 Pipelined Architecture

The overall pipelined architecture has already been described in Chapter 2. This section gives a mathematical analysis of the pipelined converter and discusses a few of the key sub-circuits in detail. A block diagram of a pipelined converter is illustrated in Figure 4.5. Each stage consists of a sample-and-hold circuit, sub-ADC, DAC, subtractor, and gain amplifier. The input to each stage is held while it goes through a coarse A/D conversion. The result of the coarse conversion is sent to shift registers to align the output code before it is digitally corrected to remove some errors. At the same time, the coarse A/D conversion is converted back to the analog domain by the DAC and subtracted from the original input signal. This *residue* is then

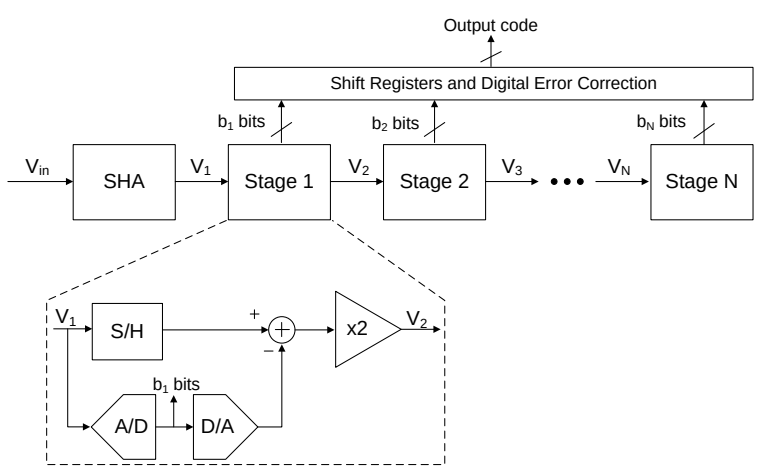


Figure 4.5 Pipelined ADC architecture.

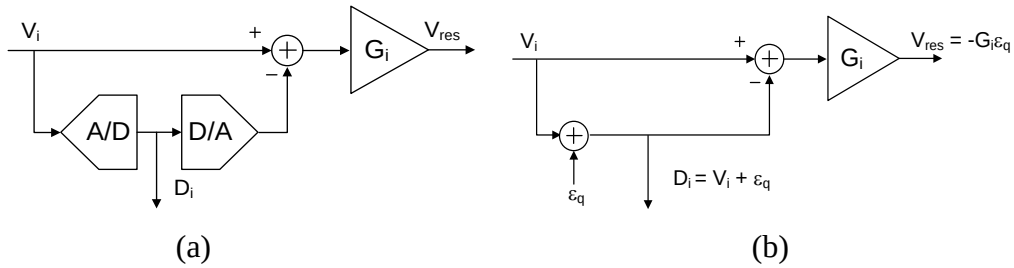


Figure 4.6 Block diagram of a single pipeline stage (a) and its equivalent model (b).

multiplied and sent to the next stage. This repeats until the end of the pipeline is reached.

There is no concrete rule for the resolution of the sub-ADC in each stage. However, it is a decision that impacts power, speed, and accuracy constraints for each stage [69]. The rule of thumb, however, is that high-speed converters favor a low-resolution sub-ADC and high-resolution converters favor a high-resolution sub-ADC. For lower bits per stage schemes, the comparators and the gain amplifier requirements are relaxed, and for larger bits per stage schemes, matching requirements for the front-end circuitry in the converter can be relaxed. Perhaps the most common selection is a 1.5 bits per stage architecture. The reader is directed to Chapter 2 for a discussion on this scheme. A more detailed analysis on pipeline stage resolution can be found in [69].

4.2.1 Pipelined Converter Analysis

Each pipeline stage has two tasks – coarse quantization and residue generation. The gain amplifier, the subtractor, and the DAC form what is more commonly known as an MDAC The sub-ADC performs the coarse quantization, and the MDAC converts the bits back into an analog form and generates the residue. The simplified model of a single pipeline stage (Figure 4.6a) can be modeled as in Figure 4.6b. The residual analog output of each individual stage can be expressed as,

$$V_{res} = -G\varepsilon_q = -G(V_{in} - V_{DAC}) = -G\varepsilon_q \tag{4.10}$$

$$D = V_{in} + \varepsilon_q \tag{4.11}$$

where ε_q is the quantization noise of the stage. Using Figure 4.6b, the overall pipelined ADC model based on stage analysis can be drawn as in Figure 4.7.

The locally computed and amplified residue propagates through subsequent stages, uncovering further less significant digital information. After the signal has passed through all stages, the sub-quantization results are combined to yield the final digital output word. This is represented by the expression

$$D_{out} = V_{in,ADC} + \varepsilon_{q1}\left(1 - \frac{G_1}{G_{d1}}\right) + \frac{\varepsilon_{q2}}{G_{d1}}\left(1 - \frac{G_2}{G_{d2}}\right) + \cdots + \frac{\varepsilon_{q(n-1)}}{\prod_{i=1}^{n-2} G_{di}}\left(1 - \frac{G_{n-1}}{G_{d(n-1)}}\right) + \frac{\varepsilon_{qn}}{\prod_{i=1}^{n-1} G_{di}} \tag{4.12}$$

where ε_i (I = 1~n) represents the quantization noise added by stage *i*. If the digital gain (G_{di}) is equal to the analog gain (G_i), all of the quantization noise we be canceled out with the last stage being an exception. Therefore, the digital output can be expressed as

$$D_{out} = V_{in,ADC} + \frac{\varepsilon_{qn}}{\prod_{i=1}^{n-1} G_i} \tag{4.13}$$

$$B_{ADC} = B_n + \sum_{i=1}^{n-1} \log_2 G_i \tag{4.14}$$

where B_n is the number of bits of the last stage. The above analysis reveals a few things. The only difference between the analog input and the digital output is the quantization noise from the last stage. The quantization noise is what ultimately limits the resolution of a converter. In practice, pipeline stages can be cascaded to increase resolution up to about 10 bits without the need for calibration or trimming. In addition, the aggregate resolution is mostly determined by the interstage gains. The resolution from adding each stages coarse A/D conversion is usually

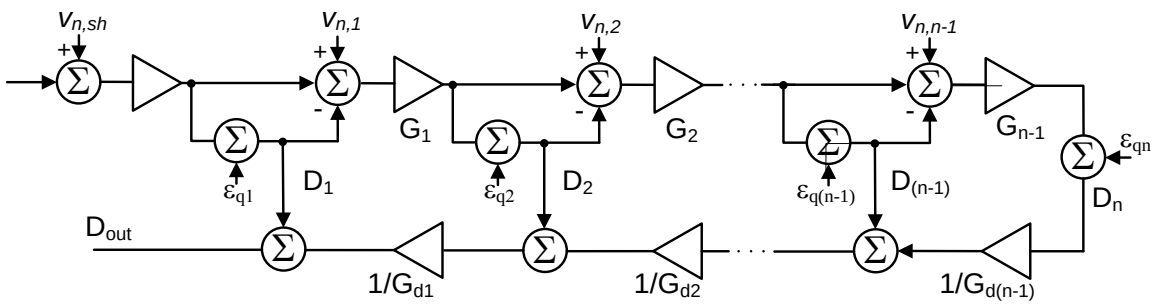


Figure 4.7 Pipeline ADC model

larger than the aggregate resolution due to redundancy which can be removed by digital correction which will be addressed in Chapter 7.

4.3 Pipelined Sub-Circuits

4.3.1 Front-End Sample-and-Hold Amplifier

A front-end sample-and-hold amplifier (SHA) can be used to ensure that the first stage sub-ADC and MDAC see the same voltage. At high frequencies, the comparators in the first stage MDAC must distinguish between small voltages in a short amount of time. Furthermore, the on resistance of the sampling switches must be small enough to minimize the voltage drop on the switch in order to decrease the signal-dependent charge injection. This would lead to a more stringent comparator design, or introduce more error in the final output code. Instead, a front-end SHA can provide the first stage with a stable, static voltage reducing the requirements for the following stages. More recently, designers are omitting the SHA because it introduces significant power, noise, and area penalties.

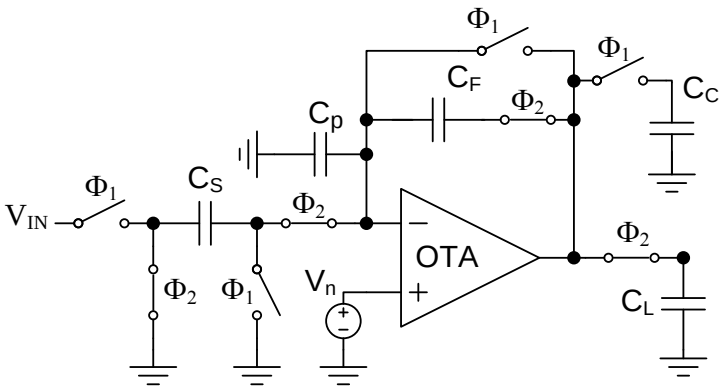


Figure 4.8 Charge redistribution sample-and-hold amplifier.

Charge Redistribution SHA

A charge redistribution SHA is shown in Figure 4.8. In an actual converter, it would be implemented in fully differential mode. However, for simplicity, it is shown in single-ended mode. Its operation can be broken into two phases, sampling phase and hold phase. During the sampling phase, Φ_1 is closed, Φ_2 is open, and the input signal is sampled on the capacitor C_S. As the OTA is not connected to the input, it is allowed to set the common mode voltage during this cycle. At the end of this cycle, the charge stored on the sampling capacitor is equal to $V_{IN} \cdot C_S$. During Φ_2, the summing node voltage is forced to be V_n due to the virtual short, the charge

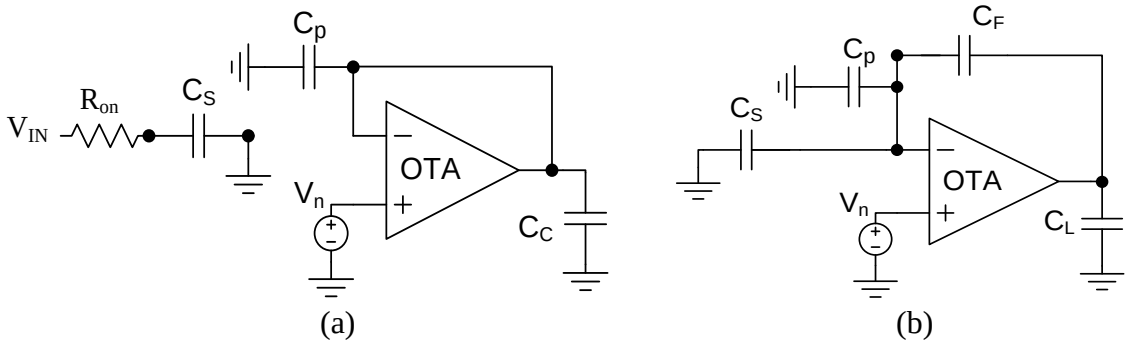


Figure 4.9 Charge redistribution SHA equivalent circuit during sampling phase (a) and hold phase (b).

stored on C_S is transferred to C_f. Equivalent circuits for sampling and hold phase are illustrated in Figure 4.9. Based on the law of charge conservation, the output voltage of the OTA can be expressed as,

$$V_o = V_{IN} \frac{C_S}{C_f} \tag{4.15}$$

The input common-mode voltage will not change from the sampling phase to the hold phase, but the charge redistribution SHA suffers from two main drawbacks, matching and settling time [70]. From Equation 4.15, it is quickly noticeable that the gain of the SHA depends on the matching of C_S and C_f. In terms of settling, the feedback factor during hold phase (Φ_2 closed) can be calculated to be

$$F = \frac{C_S}{C_S + C_f + C_p} \tag{4.16}$$

The -3 dB bandwidth of the circuit in Figure 4.9(b) is

$$\omega_{-3dB} = \omega_u \cdot F = \frac{g_m}{C_{Leff}} F \tag{4.17}$$

where $C_{Leff} = C_L + (1-F)C_f$. From the above equations, it can be seen that the small feedback factor leads to a small -3 dB bandwidth, resulting in slow settling.

Flip-Around SHA

In a flip-around SHA, the same capacitor is used for both sampling and holding. Similar to the charge-redistribution SHA, the input signal is sampled on the sampling capacitor, C_S, during Φ_1. However, during Φ_2, the sampling capacitor is disconnected from the input and connected to the output. The schematic of a flip-around SHA is shown in Figure 4.10 and the equivalent circuits for each phase are depicted in Figure 4.11. With the elimination of C_f, the feedback factor becomes

$$F=\frac{C_S}{C_S+C_p} \tag{4.18}$$

Assuming $C_S = C_f$, the feedback factor of the flip-around SHA is nearly double that of the charge-redistribution SHA. Recalling the expression for the -3 dB bandwidth in Equation 4.17, it can be concluded that the flip-around SHA has much better settling performance. Also, since a single capacitor handles sampling and holding, there is no matching problem. The drawback is that the input common mode voltage for the OTA will change between phases due to the polarity of the capacitor charge changing.

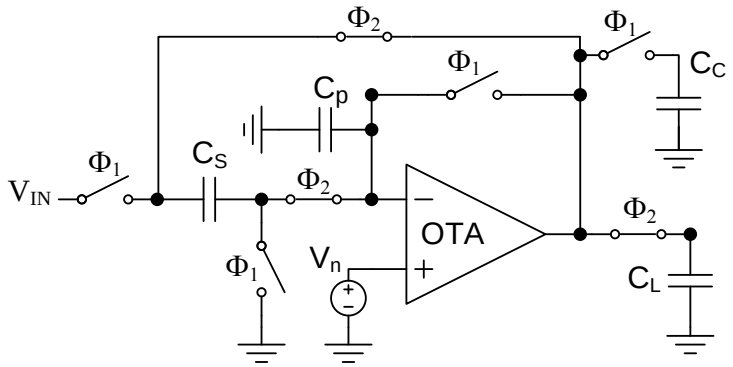
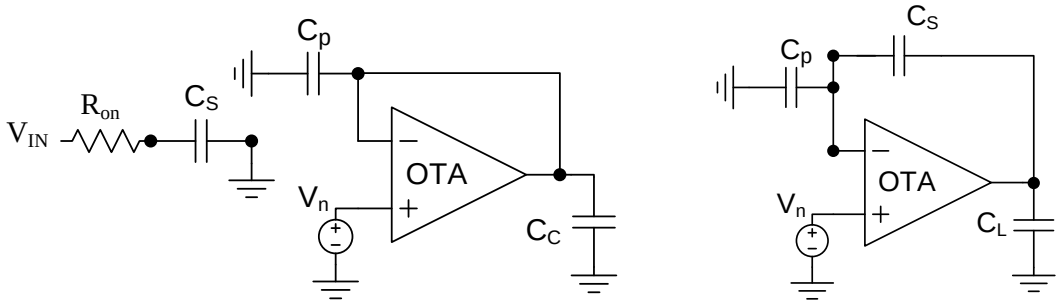


Figure 4.10 Flip-around sample-and-hold amplifier.



(a) (b)

Figure 4.11 Flip-around SHA equivalent circuits during sample phase (a) and hold phase (b)

4.3.2 Sub-ADC

Each stage of a pipelined converter contains a sub-ADC which is typically a low resolution flash ADC. The converter in this work utilizes a 1.5 bit per stage architecture. In this case, there will be two comparators ($2^{1.5} - 1 = 1.83$) and three decision regions (Figure 2.18). When the input signal into any particular pipeline stage is larger than $V_{ref}/2$, the output code is '11.' When the input is larger than $-V_{ref}/2$ but smaller than $V_{ref}/2$, the output code is '01.' When the input signal is smaller than $-V_{ref}/2$, the output code is '00'. The sub-(flash) converter is depicted in Figure 4.12. In order for the timing to work correctly, the coarse A/D and D/A conversions of each stage must finish in half of the sampling phase clock cycle. The use of digital error correction and redundancy reduces the accuracy requirement of every sub-ADC in the design to 3 bits even though the overall pipeline stages have to be much more accurate.

4.3.3 Multiplying Digital-to-Analog Converter

The circuit responsible for converting the coarse A/D conversion bits back to the analog domain, subtracting that voltage from the original input signal, and multiplying it by 2x is called the MDAC. It is a switched-capacitor style circuit and is illustrated in Figure 4.13. During the phase when Φ_1 is closed, the input signal is sampled onto capacitors C_S and C_f as the low-

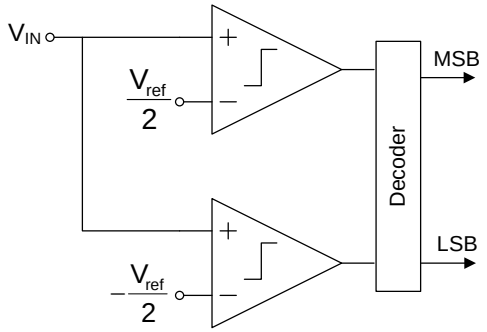


Figure 4.12 Block diagram of sub-ADC.

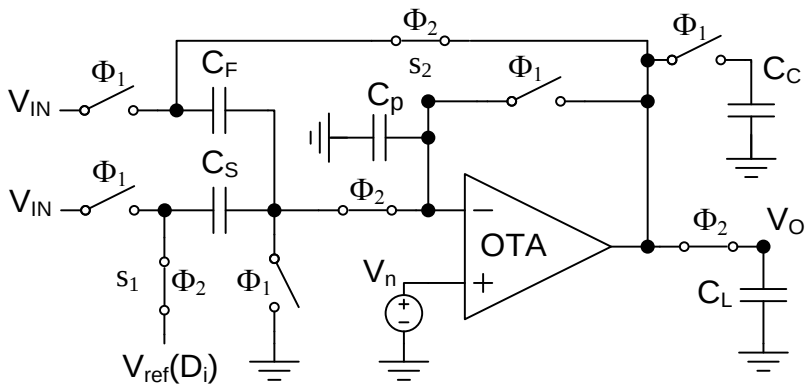


Figure 4.13 Schematic of switched-capacitor MDAC. The implemented version is fully differentially, but it is shown single-ended here for simplicity.

resolution sub-ADC quantizes the input signal. When Φ_2 closes and Φ_1 opens, depending on the output of the sub-flash converter, S_1 will connect to $-V_{ref}$, V_{ref}, or ground. Also, the charge on C_S will transfer to C_f. Since the charge is conserved during these two phases, the expression for the output voltage can be expressed as,

$$V_O = \left(1+\frac{C_S}{C_f}\right)\left(V_{IN} - D_i \cdot \frac{V_{ref}}{2}\right) \tag{4.19}$$

where D_i is based on the flash converter results. If $C_S = C_f$, then the interstage gain is equal to 2. From Equation 4.19, it becomes apparent how this single circuit performs D/A conversion, subtraction, and amplification to produce the residue voltage, V_O. Equation 4.19 also gives some insight as to why calibration or trimming is needed to obtain resolutions above 10 bits. If C_S and C_f are not precisely matched, high accuracy will be impossible to achieve.

4.4 Summary

While the successive approximation register analog-to-digital converter is an attractive choice for most implantable biomedical applications, the pipelined architecture was selected for two main reasons. First, bioimpedance monitoring requires the use of high frequency signals into

the tens of mega-Hertz range. It was shown that at 20 MS/s and higher, pipelined converters achieve a lower figure of merit than SAR converters. This is due to the fact that SAR power consumption scales heavily with sampling rate. Also, special techniques, such as time-interleaving, are generally required to reach high-speed operation in SAR converters, whereas the basic pipelined architecture can easily operate at these speeds. The second reason the pipelined converter was selected is because of its ease in reconfigurability. The resolution and sampling rate of a pipelined converter are independent of each other which make them easy to control separately. In the SAR architecture, the resolution and master clock are intertwined. If the resolution changes, the master clock has to adjust to maintain proper functionality. Similarly, if the master clock sampling rate is reconfigured, the SAR logic used to determine the number of bits must also change.

The pipelined architecture has been analyzed mathematically to relate the analog input to the digital output code. Also, key sub-circuits including the sample-and-hold amplifier, sub-ADC, and MDAC have been discussed. The flip-around SHA was chosen over the charge redistribution topology for its superior setting performance and independence on matching in the feedback capacitors.

Chapter 5 – Operation Principles of Auto-Adapting Pipelined ADC

In this chapter, the reconfigurable sampling rate and resolution schemes is described. The potential drawback of the resolution reconfiguration scheme is analyzed, and a solution to the potential problem is presented. Also, the automatic adaptation scheme of the pipelined converter is introduced.

5.1 Sampling Rate Configuration

In Chapter 3, three methods for configuring sampling rate were mentioned: adaptive biasing, current modulated power scaling (CMPS), and interstage manipulation. The ADC in this work utilizes adaptive biasing. Although CMPS proved to be a useful method for increasing power efficiency, it adds a significant amount of complexity and area penalty to the system. As one of the focuses of this work is to minimize area in addition to power consumption, CMPS was not used. Smaller area means lower cost which makes for a more attractive solution.

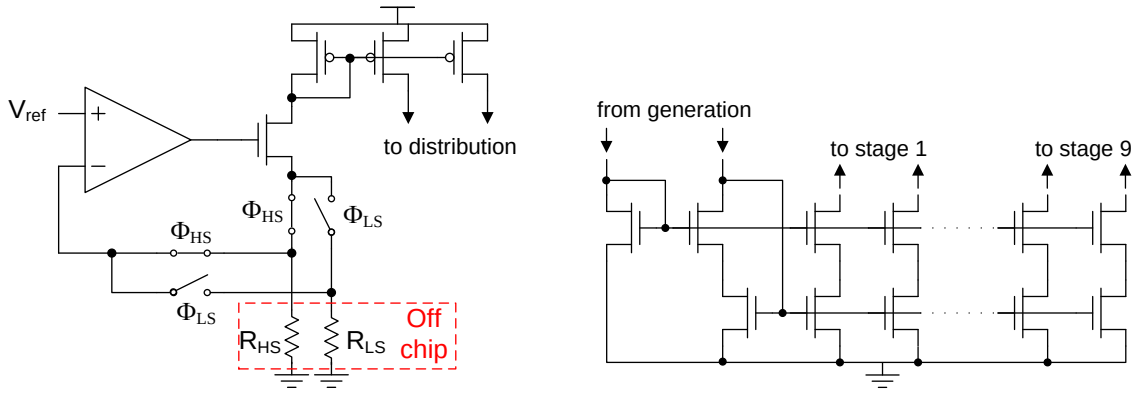


Figure 5.1 Adaptive current bias generation circuit. R_{HS} and R_{LS} are implemented off chip for easier debugging.

To get a thorough estimation of the impedance of a target tissue, cell, or organ, a wide spectrum, ranging from a few Hz to tens or hundreds of MHz, should be measured (Appendix). Consequently, the sampling rate of the proposed ADC changes with respect to the input signal frequency, so that slower inputs are sampled at a lower rate, but high frequency inputs are still able to be accurately converted. To take advantage of this, the bias currents for the amplifiers in each pipeline stage are scaled accordingly so that they achieve a bandwidth that is adequate for the desired sampling rate. The circuit responsible for generating the adaptive bias currents is shown in Figure 5.1. This circuit generates all of the bias currents for all of the pipeline stages in the converter. Delivering current signals makes for a more robust design than using voltage biasing since voltage signals are more susceptible to interference and fluctuations [71]. When the sampling rate configuring signal selects high-speed mode, Φ_{HS} is closed and Φ_{LS} is open, connecting the top terminal of resistor, R_{HS}, to V_{ref}. In low-speed mode, Φ_{HS} is open and Φ_{LS} is closed, so V_{ref} is connected to the top terminal of R_{LS}. R_{LS} is chosen to be very large in order to generate a small current while R_{HS} is a small resistance (in comparison) to generate a larger current. For the prototype design, the biasing resistors are implemented off-chip for easier debugging. However, these resistors could be implemented on-chip for a finalized ASIC.

In similar cases where bias currents are scaled down to a level that could push the transistors into weak inversion, special measures are taken to prevent it from happening. In this design, however, weak inversion-biased transistors are taken advantage of. When the ADC operates in high sampling rate mode, the transistors operate in strong inversion is as the case with many analog circuits. On the other hand, when the bias currents are scaled for low sampling rate mode, some of the transistors operate in subthreshold.

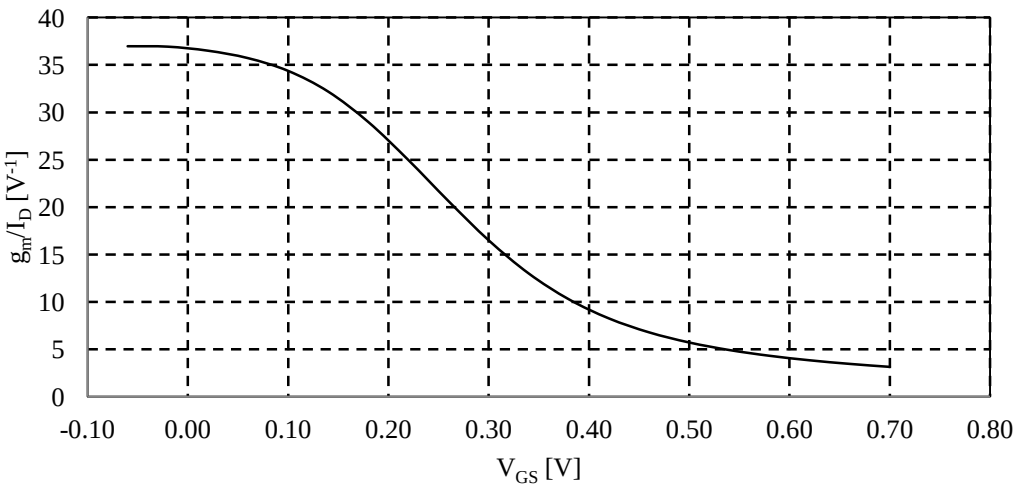


Figure 5.2 Transconductance efficiency (g_m/I_D) versus gate-source voltage curve in 130 nm process illustrating maximum transconductance efficiency in subthreshold region.

One of the biggest drawbacks of a transistor operating in weak inversion is the low transition frequency (f_t) which is the frequency at which a transistor becomes virtually useless because of degradation in transconductance. This is not a problem for the proposed system though since subthreshold region is only used for low sampling rate mode when the amplifier only needs a small bandwidth. Apart from low-current (and thus lower power) operation, another benefit of subthreshold design is that a MOSFET's transconductance efficiency (g_m/I_D) is highest when operating in weak inversion as shown in Figure 5.2.

5.1.1 Reconfigurable Amplifiers

Since the bias currents change, the amplifiers also must change to maintain proper functionality. However, since weak inversion is not being avoided, the task of designing a reconfigurable amplifier becomes simpler and less risky. If subthreshold region was being avoided, the aspect ratios of the transistors within the core of the transistor would have to adapt to keep the transistor in the desired operation region. But since this is not the case, the biasing circuitry can be adapted instead to generate the appropriate voltages to allow the transistors to

work in subthreshold region. This is beneficial because having to alter the core amplifier transistors could introduce noise and interference into the signal path. Additionally, extra switches could lead to undesirable voltage drops, and to avoid that, the switches would have to be made larger, making the parasitic gate capacitance large. These large parasitic capacitors could limit the already slow speed of the weak-inversion transistors even more. This is why the chosen method is a lot safer and simpler. The reconfigurable amplifier biasing circuitry is shown in Figure 5.3. The circuit receives the bias currents from the bias distribution circuit from Figure 5.1. Depending on the setting from the auto-adaptation unit, the sampling rate control (SRC) signal will be 'high' or 'low', connecting the respective setting's transistors to the rest of the circuit. Voltages *vnb, vnc, vpb, vpc, vncc, vc,* and *vct* are used by the core amplifier and their values will change depending on the setting of SRC. The resolution control switch at the top of the schematic is used to turn on/off the amplifier in the SHA and the first two pipeline stages. When the resolution control signal closes the switch, the bias current flows from VDD to GND. No current flows through the bias circuit, so the amplifier consumes no power. When the switch is open, the circuit operates as normal.

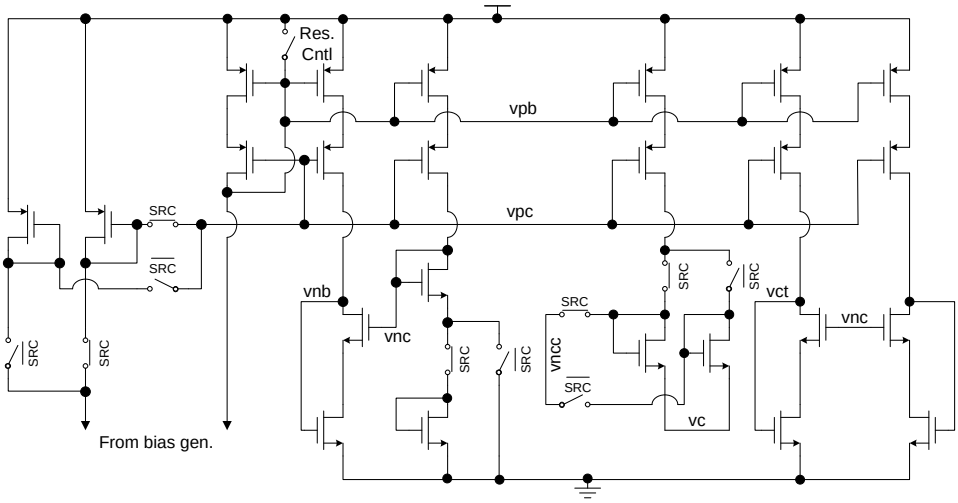


Figure 5.3 Bias scheme for reconfigurable operational transconductance amplifier.

5.2 Resolution Configuration

As mentioned previously, the converter in this system can be configured for 8-bit mode or 10-bit mode depending on the amplitude of the input signal. Smaller amplitude signals need greater precision to be distinguished, so 10-bit mode is selected for input amplitudes 250mV or less. On the other hand, larger amplitude signals are more easily distinguished, so 8-bit mode is selected for amplitudes greater than 250 mV [71]. For a pipelined ADC, there are two ways to configure the resolution, turning off the beginning stages or the ending stages as illustrated in Figure 5.4. The second method is generally easier than the first as it does not disrupt the pipeline. The first method disrupts the pipeline and requires re-routing of original signal from the main sample-and-hold amplifier to stage 3. Although, using the beginning stages adds slightly more complexity, the added power efficiency outweighs this drawback. An analysis of the resolution configuration scheme, a potential drawback, and a solution to that drawback is carried out here.

5.2.1 Power in Pipeline Stages

The later stages of a pipelined ADC generally consume far less power than the earlier stages because the earlier stages require more accuracy. For instance, the SHA of a 10-bit pipelined ADC requires 10-bit accuracy. Another way of saying this is the SHA is allowed 1 part in 2^{10}, or 0.1%, error. The next stage needs 9-bit accuracy, or 0.2% error is allowed, and so on. This error includes all non-idealities such as finite gain, dynamic settling error, slewing, charge injection, noise, interference, etc. In order to achieve high accuracy in the earlier stages, more current is used to increase the bandwidth and the slew rate, and lessen the effects of noise. Current is then slightly relaxed in the later stages to save power as accuracy requirements are diminished. As a result, using the beginning stages for resolution configuration achieves more power efficiency. A graph of the normalized power consumption of each pipeline stage is shown

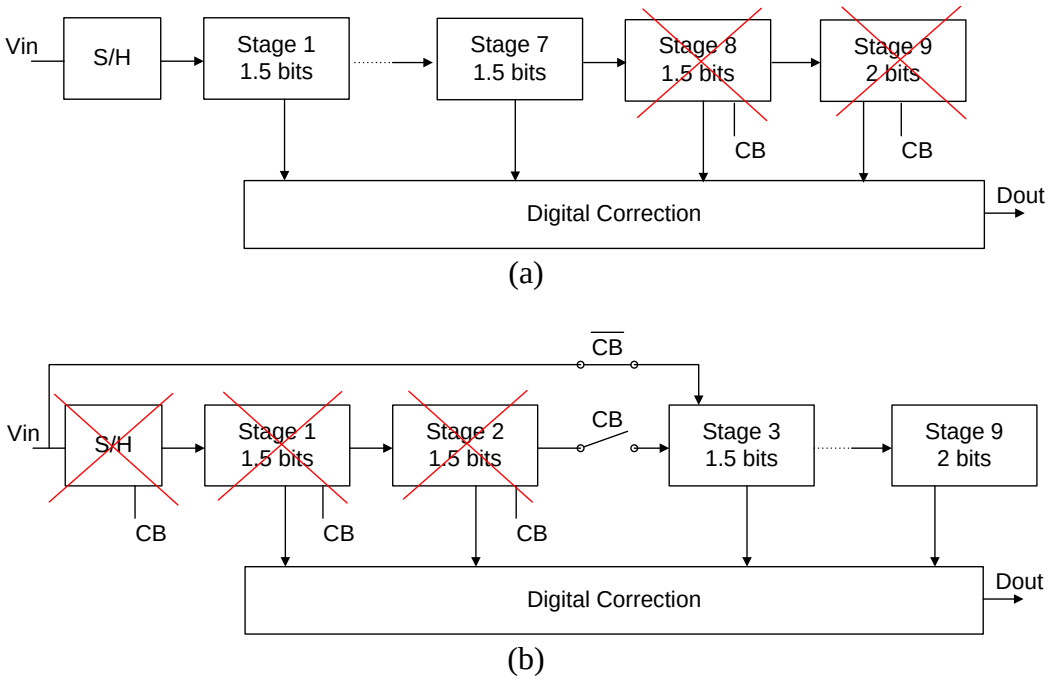


Figure 5.4 Two possible reconfigurable resolution schemes for pipelined ADC.

in Figure 5.5. It is clear that the earlier stages use significantly more power than the later stages for the reasons expressed above. Using the beginning stages for reconfiguration also eliminates an extra stage, the front end sample-and-hold amplifier, which further improves power efficiency.

5.2.1 Interference Elimination

Since the first three stages (including S/H) will be turned off during 8-bit mode, the original input signal must be re-routed to stage 3. However, stage 3 usually receives only the residual signal from stage 2, but the extra wiring and switches used to re-route the original input signal could introduce interference. In 10-bit mode, the original input signal could interfere with the residue from stage 2 via leakage through the off-state switch, and vise versa in 8-bit mode. An off-state analog switch along with its equivalent circuit to analyze its off isolation is shown in

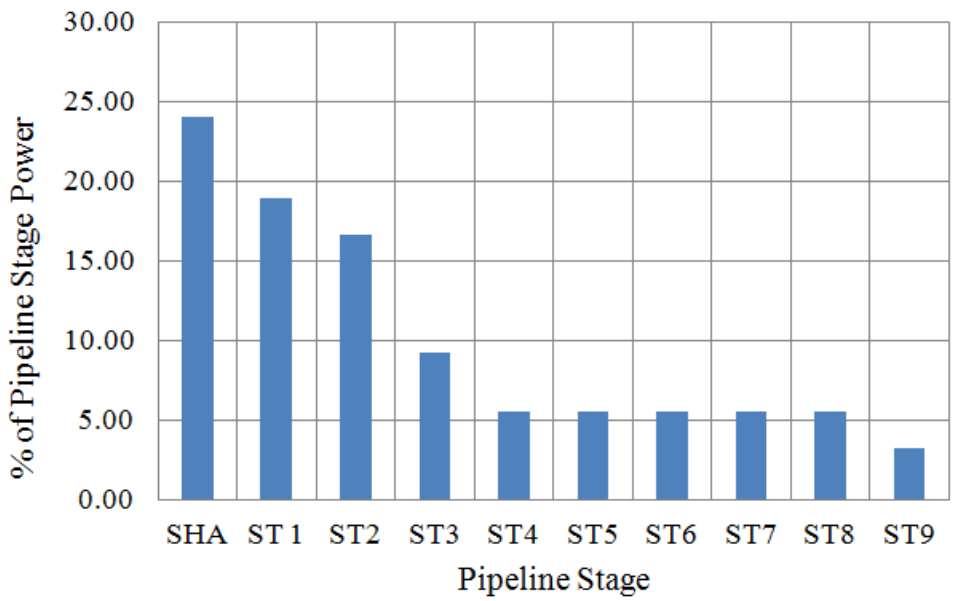


Figure 5.5 Normalized power consumption for pipelined converter stages.

Figure 5.6. Since both the gate and the body are connected to the ground, C_{gd} and C_{bd} are in parallel and form C_d. Similarly, C_{gs} and C_{bs} make up C_s. C_{ds} couples the input signal to the output load degrading the off-isolation performance of the switch. The transfer function of the off isolation is expressed in Equation 5.3. Depicted in Figure 5.7, a plot of the transfer function indicates that at higher frequencies and smaller channel lengths, signal leakage can become a factor.

$$\frac{V_{out}}{V_{in}} = \frac{Z_D}{Z_D + {}^{1}/_{sC_{DS}}} \tag{5.1}$$

$$Z_D = \frac{R_L(1+sR_sC_S)}{(1+sR_LC_S+sR_SC_S)+[sR_LC_D(1+sR_SC_S)]} \tag{5.2}$$

$$A(s) = \frac{V_{out}}{V_{in}} = \frac{s^2(R_LR_SC_{DS}C_S)+s(R_LC_{DS})}{s^2(R_LR_SC_DC_S+R_LR_SC_{DS}C_S)+s(R_LC_S+R_SC_S+R_LC_D+R_LC_{DS})+1} \tag{5.3}$$

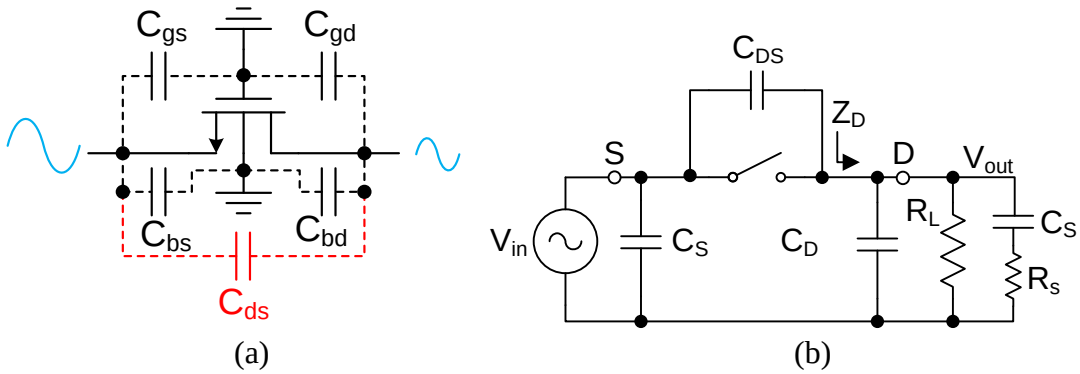


Figure 5.6 Off-state switch model (a) and its equivalent circuit (b).

To put these simulation results into perspective, assume that stage 3 requires 8-bit accuracy. Therefore 0.4% error is allowed for the entire stage. If a -65 dB signal is introduced as interference, then that already accounts for about 14.4% of the allowed error in the stage. To alleviate the signal leakage possibility, stage 3 is implemented as shown in Figure 5.8. This implementation takes advantage of the high common mode rejection ratio (CMRR) of operational transconductance amplifiers (OTA) by turning any possible interfering leakage signal into a common mode signal. This signal is then rejected by the amplifier and can be ignored.

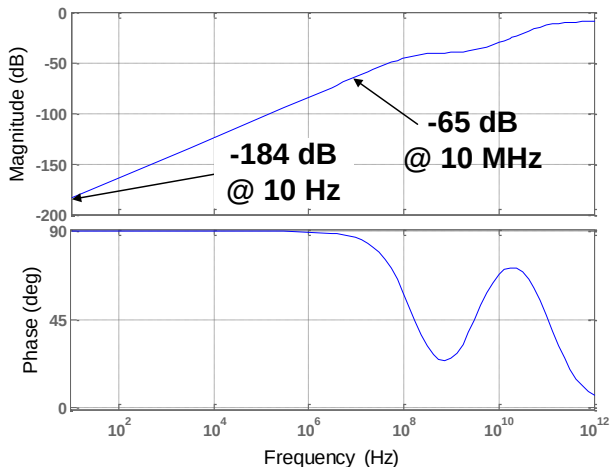


Figure 5.7 Calculated off-state switch isolation versus frequency plotted in MATLAB.

For example, if a 0 dBm signal is present at the source of an off switch that has −40 dB of isolation, and the amplifier has a CMRR of 70 dB, a −110 dBm interference signal will be present at the drain terminal. In 10-bit mode, Φ8b will be low turning off the main switch. Part of the signal 'V_{IN_P}' will pass through the off switch through C_{ds}, but because of how stage 3 is implemented, that leakage will appear on the non-inverting terminal of the amplifier and the inverting terminal through an always-off dummy switch. As a result, the common signal is

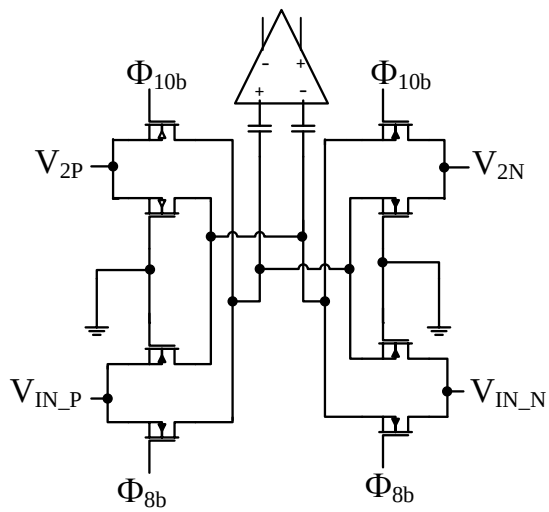


Figure 5.8 Stage 3 implementation to eliminate possibilities of off-switch leakage signal interference.

rejected by the amplifier. The same attenuation mechanism also happens for signal 'V_{IN_N}' as well as 'V_{2P}' and 'V_{2N}' under 8-bit operation.

The new transfer function of an off-switch isolation including the CMRR of the OTA can be expressed as,

$$A_{iso}(s)=A_{sw}(s)\cdot A_{CMRR}(s)=A_{sw}(s)\cdot\frac{1+2g_{m,in}(R_{out}+\frac{1}{sC_p})}{\frac{\Delta g_m}{g_m}+\frac{\Delta R_{out}}{R_{out}}} \tag{5.4}$$

It can be seen in Figure 5.9 that the implemented interference elimination technique greatly attenuates any possible interference that arises due to the use of the resolution configuration scheme.

5.3 Automatic Adaptation

Bioimpedance readings should be taken over a large spectrum to obtain all useful information about a target sample. Therefore, a wide frequency range of currents should be used to excite the target biosample, and depending on the value of the current and the impedance of the target sample, the voltage drop can greatly vary across the spectrum. For a power-efficient analog-to-digital converter to be designed for this type of system, it has to not only be able to adapt its sampling speed and resolution, but it has to be able to quickly and constantly decide which configuration to operate in to accommodate the analog input signal. For this purpose, a low-power, low-complexity automatic adaptation unit was developed.

Many reconfigurable ADC architectures in the literature mention that the configuration of the resolution, the sampling rate, or both can be controlled digitally. However, most of these

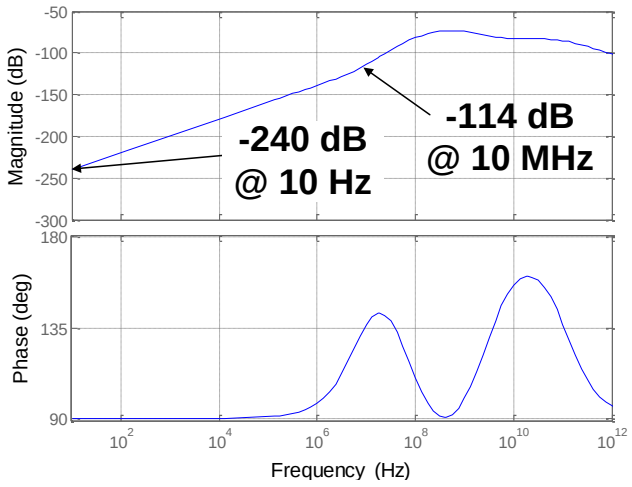


Figure 5.9 Calculated off-state switch isolation using elimination interference technique versus frequency plotted in MATLAB.

designs depend on manual signals from a user or a separate programmable controller to make these reconfigurations happen [53], [54], [72]-[74]. In an implantable system, this would involve extra telemetry circuitry for receiving the configuration signal in addition to the transmitter circuitry already required to transmit the data to a PC or smart phone. Obviously, this would lead to a larger, more power hungry system. If instead, the configuration of the ADC can be decided automatically without the need for a third party source, the system will consume less power, be less complex, and occupy a smaller area.

The block diagram of the auto-adaptation unit is shown in Figure 5.10. It is a simple circuit suitable for biomedical applications because it requires little power and area penalty. It uses the input signal frequency and amplitude to decide what mode the converter should operate in. An input signal faster than 50 kHz will configure the ADC in fast mode; otherwise, it operates in slow mode. Input signals smaller than 50 mV will configure the converter in 10-bit mode; otherwise, it converts with 8 bits of resolution.

5.3.1 Sampling Rate Control Signal

To configure the sampling rate, the input signal is amplified and transformed into a square wave via Schmitt trigger. A frequency-to-voltage converter (FVC) is then used to output a DC voltage that is inversely proportional to the input signal frequency. Finally, the DC voltage

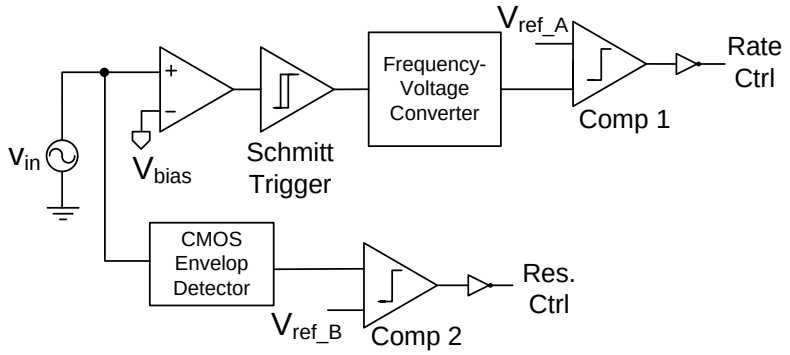


Figure 5.10 Block diagram of automatic adaptation unit used to configure the pipelined ADC.

produced by the FVC is compared to a reference voltage that corresponds to 50 kHz. The output of the comparator is buffered and then serves as the control bit for the entire converter to control the sampling rate.

Frequency-to-Voltage Converter

The principal block of the adaptation unit is the frequency-to-voltage converter. As the name implies, it translates the input signal frequency into a DC voltage so that it can be compared to a reference voltage to generate the sampling rate control bit. The schematic is depicted in Figure 5.11. The operation of the circuit can be broken into three states. In the first state, M2, M3, and M4 are off while P1 is on, so that the bias current I_B charges C1. The charge that is accumulated is proportional to half the period of the input wave. In the next state, P1, and M2 are off while M3 and M4 are switched on, so the charge stored on C1 transfers to C2. In the last state, P1, M3, and M4 are switched off, and M2 is switched on, so C1 is discharged to ground and C2 maintains its charge as it is isolated. To make the circuit suitable for biomedical applications, the aspect ratio of transistor M2 is made small so C1 does not discharge too quickly at low frequencies.

If the input signal frequency is constant, the above steps will be repeated periodically, and after a few periods, the charge stored on C2 will reach a steady state. This charge is directly related to the charge acquired on C1 during the time when P1 is on, so the voltage at the output can be expressed as [75],

$$V_{out} = \frac{I_B}{C1} T \tag{5.5}$$

If the input signal is a symmetrical wave with 50% duty cycle, Equation 5.5 can be expressed in terms of the frequency, f_{in}, directly as,

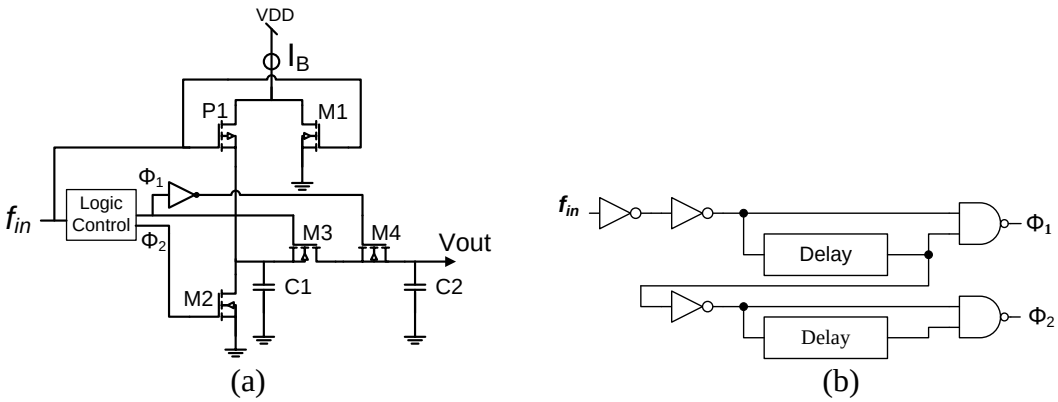


Figure 5.11 Frequency to voltage converter used in the self adaptation unit (a) and its logic control block (b).

$$V_{out}=\frac{I_B}{2f_{in}C_1} \tag{5.6}$$

where I_B is the bias current, f_{in} is the input signal frequency and C1 is the storage capacitance. From Equation 5.6, it is evident that the converter is limited with respect to how wide a frequency range can be distinguished. For example, with a supply voltage of 2 V, and a converter designed to give a 1 V DC output at 100 kHz, 50 kHz will theoretically produce the maximum output voltage. An input frequency of 200 kHz will produce a 500 mV output, 400 kHz a 250 mV output, and so on. In practice, the maximum output voltage would be reached before 50 kHz because of the on resistances of transistors P1, and M3. This is acceptable for this application because the only distinction required is between low frequency and high frequency.

5.3.2 Resolution Control Signal

For resolution configuration, a novel CMOS envelope detector is used to determine the amplitude of the input signal. A schematic of the envelope detector is shown in Figure 5.12. The CMOS full-wave rectifier works on a wide spectrum of input signals due to the use of pseudo-resistors. Complimentary input signals enter the capacitors to block their DC levels. The PMOS

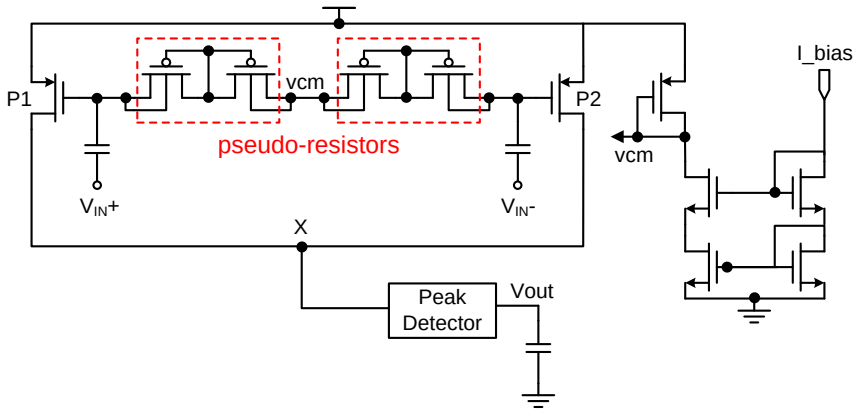


Figure 5.12 Low power, wide dynamic range CMOS envelope detector used for resolution. control.

pseudo-resistors create a large time constant with the capacitors so that low frequency signals can still be rectified. The bias voltage, *vcm*, set right at the threshold of transistors P1 and P2 so that only the positive cycle will cause current flow. Since complimentary input signals are used, full-wave rectification is achieved. The two half-wave rectified currents are summed at node X before going to the peak detector.

The full-wave rectified current, I_{rec}, flows into the peak detector, which consists of a source follower M1 and M2, a storage capacitor C, and a feedback path M3 and M4. Since the charging current of the capacitor is larger than the discharging current through M2, the output voltage, V_{out}, will track the peak value of input signal [76]. The DC voltage generated by the envelope detector is then compared to a reference voltage that corresponds to 50 mV input amplitude.

Comparator

Unlike the comparator used in the subADC of each pipeline stage, the comparators used in the self adaptation unit needs to be static because they are always checking if the FVC-generated voltage and the envelope detector voltage are above their respective reference voltages

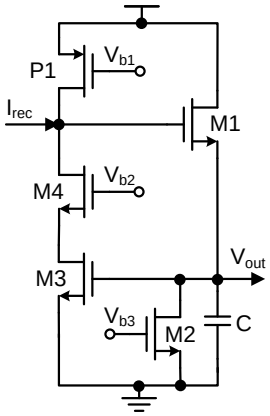


Figure 5.13 Peak detector used in low-power envelope detector.

to determine how the ADC should be configured. A schematic of the comparator is shown in Figure 5.14. Speed is not an issue because all of the input voltages are static signals. Instead, metastability is the major concern. If the DC voltage generated by the FVC is close to the reference voltage, noise or other interference could make the output of the comparator rapidly and incorrectly switch states or potentially put the comparator output at a voltage that is neither a logic ‘0’ nor ‘1’. To counteract this, hysteresis is designed into the comparator so that the compared voltage must be higher or lower than the reference voltage by a certain amount for the output to change. A drawback of this is that the transition from one operation mode to the next will happen at different frequencies for an increasing and decreasing frequency signal.

5.4 Summary

The sampling rate and resolution reconfiguration schemes have been presented. An adaptive biasing scheme was adopted to control the bias currents for a changing sampling rate, and the beginning pipeline stages are used for resolution configuration. It was shown that using the beginning stages saves considerably more power and greatly increases power efficiency over using the end stages. An interference elimination technique that takes advantage of the common

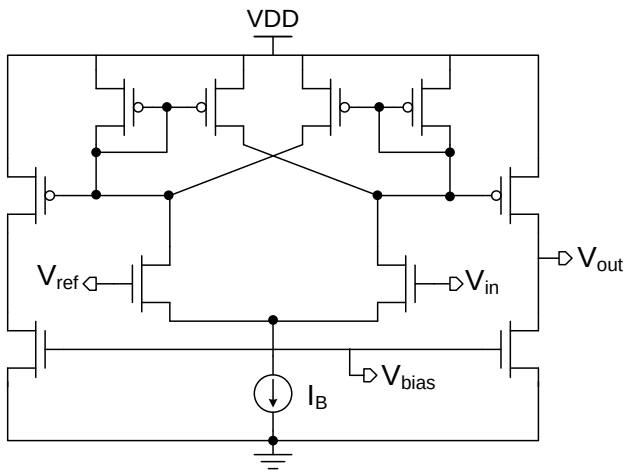


Figure 5.14 Static comparator used in the self adaptation unit.

mode rejection ration of operation transconductance amplifiers was employed to decrease the possibility of crosstalk between the original input signal and residue from stage 2 in stage 3.

The circuit responsible for automatically adapting the converter was introduced. The circuit is a key addition to the system because it allows a full spectrum of bioimpedance measurements to be taken with increased power efficiency without the need for user control. As the frequency is increased or decreased, the automatic adaptation unit will control what bias currents get sent to the analog circuits throughout the design. This is done with the help of a frequency-to-voltage converter. Similarly, as the voltage drop across the biosample changes in amplitude, the automatic adaptation unit decides what resolution is suitable for the conversion.

Chapter 6 – Nonidealities in Pipelined ADC

In this chapter, nonidealities such as mismatch and noise will be analyzed for a pipelined analog-to-digital converter. The topics discussed here are fundamental limitations to ADC performance and designers should be aware of them and how to minimize their effects when designing a data converter.

6.1 Mismatch

It is best to analyze mismatch using statistical analysis in which all of the possible causes of mismatch are treated as random variables that are unrelated and normally distributed. Systematic mismatch is assumed to be eliminated through proper design techniques and will not be discussed here. To begin, consider the mismatch model of a transistor. A top view of a typical CMOS MOSFET looks like a rectangle as illustrated in Figure 6.1. Based on Fourier analysis, the variance of some parameter P between two identical rectangular objects is expressed as [77], [78]

$$\sigma^2(\Delta P)=\frac{A_P^2}{WL}+S_P^2\cdot D_X^2 \tag{6.1}$$

where A_p is a technology dependent area proportionality constant, S_p is a spacing constant, and D_x is the spacing between the two objects. Extensive research in this area has revealed that the second term can be neglected, and so it becomes apparent that the mismatch of some parameter P between two devices is largely a function of gate width and length.

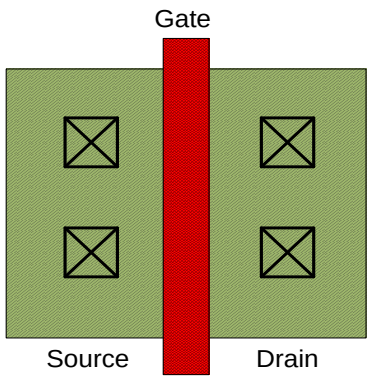


Figure 6.1 Top view of CMOS transistor to analyze mismatch.

6.1.1 Current Mirror Mismatch

Experimental data has shown that the two primary sources of drain current (or gate-source voltage) mismatch between transistors are threshold voltage and current factor variance [78]. Threshold voltage (V_T) mismatch happens because of substrate doping, oxide thickness, and short channel effects. Current factor is defined as $\Delta\beta/\beta$, where $\beta = \mu_n C_{OX} W/L$. Current factor mismatch happens mainly because of mobility difference as well as other physical effects such as photomask offsets [79]. Thinking of both of these sources as a different parameter for mismatch and using Equation 6.1, their variances can be written as,

$$\sigma^2(\Delta V_T) = \frac{A_{VT}^2}{WL} \tag{6.2}$$

$$\left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 = \frac{A_\beta^2}{WL} \tag{6.3}$$

where again, A_{VT} and A_β are technology dependent. From the above equations, it can be seen that to decrease the threshold voltage and the current factor variations and therefore decrease errors caused by mismatch, larger area transistors should be used. To see how these parameters

effect circuit performance, the variance for the drain current and the gate-source voltage can be written in terms of threshold voltage and current factor mismatch.

$$\left(\frac{\sigma(\Delta I_{DS})}{I_{DS}}\right)^2 = \left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 + \left(g_m/I\right)^2\sigma^2(\Delta V_T) \tag{6.4}$$

$$\sigma^2(V_{GS})=\sigma^2(V_T) + \frac{1}{\left(g_m/I_{DS}\right)^2}\left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 \tag{6.5}$$

Equations 6.4 and 6.5 are valid from weak inversion to strong inversion which is important because some of the transistors in the amplifiers used in this design operate in both depending on the mode of operation. Equation 6.4 can be rewritten to give a more insightful expression for the drain current mismatch.

$$\sigma^2(\Delta I_{DS})=I_{DS}\left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 + g_m\sigma^2(\Delta V_T) \tag{6.6}$$

The transconductance for a MOSFET operating in weak inversion and strong inversion can be expressed as,

$$g_m=\frac{\kappa I_{DS}}{U_T} \tag{6.7}$$

and

$$g_m=\frac{2I_{DS}}{V_{OV}} \tag{6.8}$$

respectively; where κ is the subthreshold gate coupling coefficient, U_T is thermal voltage, and V_{OV} is the overdrive voltage ($V_{GS} - V_T$). By subbing either Equation 6.7 or 6.8 for g_m in Equations 6.6, it can be determined that in strong inversion, current mismatch can be mitigated to

some extent with a larger overdrive voltage. However, mismatch in subthreshold transistors is harder to manipulate. Notice from Equations 6.4 and 6.5 that the heightened transconductance efficiency of transistors operating in weak inversion hurts current mismatch but helps voltage mismatch.

6.1.2 Offset Voltage due to Mismatch

The offset voltage of a fully differential OTA is caused by a couple of factors. The first is the threshold voltage and the current factor mismatch in the input pair. The second is the mismatch induced by the current mirror load. From Equation 6.5, the offset voltage generated by the input pair can be expressed as,

$$V_{os,in}=\Delta V_{T,in}+\frac{I_{DS}}{g_{m,in}}\frac{\Delta\beta_{in}}{\beta_{in}} \tag{6.8}$$

Unlike current mismatch, a higher V_{OV} harms offset voltage mismatch in strong inversion. The current mismatch from the current mirror load will also contribute to the offset voltage mismatch. By referring the current mirror load mismatch to the input through the input pair transconductance, this offset can be expressed as,

$$V_{os,cm}=\frac{g_{m,cm}}{g_{m,in}}\Delta V_{T,cm}+\frac{I_{DS}}{g_{m,in}}\frac{\Delta\beta_{cm}}{\beta_{cm}} \tag{6.9}$$

The overall offset is the combination of Equations 6.8 and 6.9, and so it becomes

$$V_{os}=\Delta V_{T,in}+\frac{g_{m,cm}}{g_{m,in}}\Delta V_{T,cm}+\frac{I_{DS}}{g_{m,in}}\left(\frac{\Delta\beta_{in}}{\beta_{in}}+\frac{\Delta\beta_{cm}}{\beta_{cm}}\right) \tag{6.10}$$

If ΔV_T and $\Delta\beta/\beta$ are substituted for the expressions found in Equations 6.2 and 6.3, respectively, then the offset voltage can be rewritten,

$$\sigma^2(V_{os}) = \frac{A_{VT,in}^2}{W_{in}L_{in}} + \left(\frac{g_{m,cm}}{g_{m,in}}\right)^2 \cdot \frac{A_{VT,cm}^2}{W_{cm}L_{cm}} +$$

$$\left(\frac{I_{DS}}{g_{m,in}}\right)^2 \cdot \left[\frac{A_{\beta,in}^2}{W_{in}L_{in}} + A_{\beta,in}^2\left(\frac{1}{W_{in}^2} + \frac{1}{L_{in}^2}\right) + \frac{A_{\beta,cm}^2}{W_{cm}L_{cm}} + A_{\beta,cm}^2\left(\frac{1}{W_{cm}^2} + \frac{1}{L_{cm}^2}\right)\right] \quad (6.11)$$

For a given process, A_β and A_{VT} are fixed. Therefore, to improve matching, the only thing that can be done is to increase device sizes or decrease the ratio of the current mirror transconductance to the input pair transconductance. Fortunately, these are all things that lend themselves to subthreshold design and improving noise performance.

6.1.3 Capacitor Mismatch

For identical capacitors, similar expressions can be obtained that lead to larger components resulting in better matching. As mentioned earlier, capacitor mismatch is a major limiting factor for MDAC accuracy. Most modern processes are able to achieve 10-bit accuracy in terms of capacitor variance. However, for higher resolutions, precision trimming can be used to identically match capacitors. Also mentioned before, digital calibration can be used to remove the effects of capacitor mismatch as well as other causes of error.

6.2 Noise

6.2.1 Thermal Noise

Thermal noise, or Nyquist noise, is noise generated by electrons (or charge carriers) due to thermal agitation. Thermal noise is present in all electronic components and it usually uniformly distributed across the entire frequency spectrum up to about 1000 GHz [80]. For a pipelined converter, the input-referred thermal noise can be found for each stage and then the overall thermal noise for entire converter can be determined. As discussed earlier, the MDAC in each pipeline stage is a switched-capacitor style circuit that includes a gain amplifier. The two

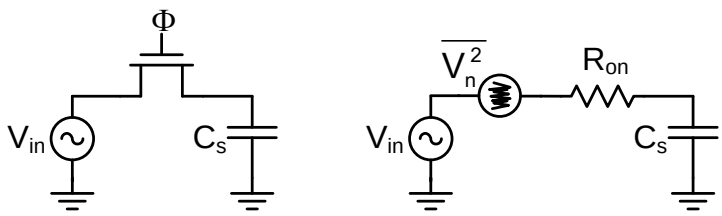


Figure 6.2 Sample and hold circuit (a) and its equivalent circuit model during sample period (b)

main sources of thermal noise present in this configuration are the noise generated by the sampling switches and the gain amplifier.

Thermal Noise in Sampling Circuit

A sample-and-hold circuit and its equivalent circuit during sample mode are shown in Figure 6.2. The circuit has no noise immunity because it is incapable of distinguishing the signal from noise, so when it samples the data it also samples the noise on the sampling capacitor. The root-mean-square (RMS) thermal noise voltage can be expressed as [81]

$$\sqrt{v_n^2}=\sqrt{\int_0^{\infty}\frac{4kTR_{on}}{1+(2\pi f\cdot R_{on}C)^2}df}=\sqrt{\frac{kT}{C}} \tag{6.12}$$

where k is Boltzmann's constant and T is temperature in Kelvin. The noise spectral density is just the square of Equation 6.12, so it becomes

$$S(f)=\frac{kT}{C_S} \tag{6.13}$$

hence why this noise is often referred to as "kT/C" noise. Note that it is independent of the noise source, R_{on}. The above expression implies that in order to decrease noise, a larger sampling capacitor should be used.

Thermal Noise in Gain Amplifier

The input-referred noise power spectral density of the gain amplifier can be expressed as [82],

$$S(f)=2\cdot\frac{8}{3}\frac{kT}{g_m} \tag{6.14}$$

where g_m is the transconductance of the input transistor. The factor of 2 is because of the fully-differential implementation. In order to reduce the thermal noise of the gain amplifier, larger g_m values for the input pair are preferred.

Thermal Noise in MDAC

The two thermal noise contributors in the MDAC have been analyzed separately, and the noise of the MDAC as a whole involves these two expressions. However, the noise voltage during sampling will be different (and uncorrelated) with the noise voltage during holding. Since they are uncorrelated, their noise powers can be calculated separately and then added together. The equivalent circuits for the different phases of the MDAC are shown in Figure 6.3. During sampling, the OTA is connected with unity gain and so the feedback factor, $F_{\beta 1}$, is equal to 1. The equivalent load capacitance is $C_{L,1} = C_C + C_p$. The unity gain bandwidth for a single-pole OTA is $\omega_u = g_m/C_{L,1}$. The −3 dB bandwidth is $\omega_{-3dB} = \omega_u \cdot F_{\beta 1}$ and the noise bandwidth is

$$BW_{n,1}=\frac{\omega_{-3dB}}{4}=\frac{g_m}{4(C_p+C_c)} \tag{6.15}$$

The total noise power during sampling can then be expressed as

$$v_{n,1}^2=S(f)\cdot BW_{n,1}=\frac{8}{3}\frac{kT}{g_m}\cdot\frac{g_m}{4(C_p+C_c)}=\frac{2}{3}\cdot\frac{kT}{C_p+C_c} \tag{6.16}$$

During the hold phase, the feedback factor of the OTA is $F_{\beta 2} = \frac{C_F}{C_F+C_S+C_{amp}}$. The equivalent load capacitance in this case is $C_{L,2} = C_L + (1- F_{\beta 2})C_f$, so the noise bandwidth becomes,

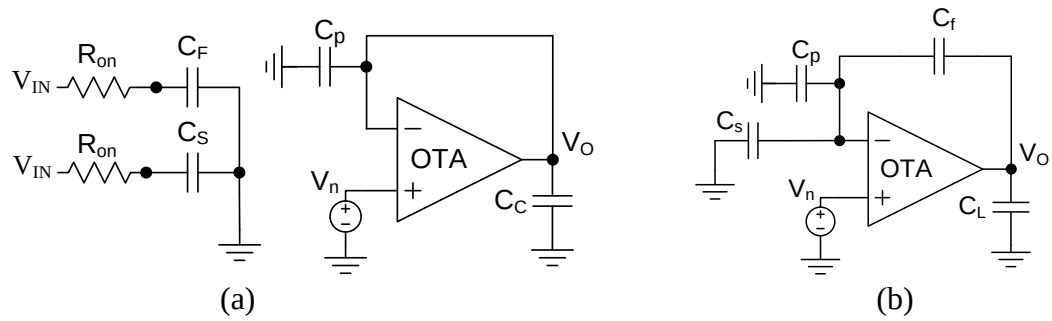


Figure 6.3 Switched-capacitor MDAC equivalent circuit during sample phase (a) and hold phase.

$$BW_{n,2}=\frac{\omega_{-3dB}}{4}=\frac{g_m}{4\left[\left(1-F_{\beta 2}\right)C_f+C_L\right]}\cdot F_{\beta 2} \tag{6.17}$$

and the total noise power during the hold phase can be calculated as,

$$v_{n,2}^2=\frac{8}{3}\frac{kT}{g_m}\cdot\frac{g_m}{4\left[\left(1-F_{\beta 2}\right)C_f+C_L\right]}\cdot F_{\beta 2}=\frac{2}{3}\cdot\frac{kT}{C_L+F_2\cdot C_p}\cdot F_{\beta 2} \tag{6.18}$$

Based on the charge conservation law, the total noise voltage appearing on the output at the end of hold phase is

$$v_{n,o}=\frac{1}{F_{\beta 2}}\cdot v_{n,2}-\frac{C_p}{C_f}v_{n,1} \tag{6.19}$$

The total MDAC noise can be determined by dividing Equation 6.19 by the closed-loop voltage gain ($1 + C_s/C_f$) and adding the kT/C noise from the sampling switching. Therefore, the total input-referred thermal noise for the MDAC can be expressed as,

$$v_n^2=\frac{2}{3}\left(\frac{C_s+C_f}{C_f}\right)\left[\left(\frac{kT}{C_L+F_2\cdot C_p}\cdot F_{\beta 2}\right)+\left(\frac{kT}{C_p+C_c}\right)\right]+\frac{kT}{C_s+C_f} \tag{6.20}$$

where the first term is the noise contribution from the gain amplifier and the second term is from the sampling circuit. The above expression reveals that the sampling and feedback capacitors as well as the amplifier parasitic capacitance play a significant role is the noise performance of each pipeline stage. It can also be seen that most of the noise contribution is from the sampling circuit,

followed by the gain amplifier during the hold phase, and lastly the gain amplifier during the sampling phase. Sufficiently sized capacitors are critical for achieving the accuracy required in the beginning stages of the pipelined ADC.

Thermal Noise in Pipelined ADC

Now that an expression for the thermal noise of each individual stage has been obtained, the total input referred noise for the pipelined ADC can be modeled as in Figure 6.4. There is a gain of 2x between each stage, so the input-referred noise of stage *N* will be attenuated by $\frac{1}{2^{N-1}}$. Notice that each stage is attenuated by $\frac{1}{2^{N-1}}$ and not $\frac{1}{2^{N}}$. This is because there is no attenuation between the front-end sample-and-hold amplifier and the stage 1. Therefore stage 2's noise is divided by 2, stage 3 by 4, stage 4 by 8, and so on. The total input-referred noise for the pipelined ADC can be generalized as

$$\overline{V}^2_{in,TOT}=\overline{V}^2_{in,SH}+\overline{V}^2_{in,1}+\frac{\overline{V}^2_{in,2}}{G_1}+\cdots+\frac{\overline{V}^2_{in,N}}{G_{N-1}} \tag{6.21}$$

6.2.2 Flicker Noise

Flicker noise is the dominant noise contributor for CMOS devices at low frequencies [80], [83]. This low frequency noise is primarily caused by fluctuation of the number of inversion layer carriers as they are trapped and untrapped to and from oxide traps. These fluctuations can also cause fluctuations in the channel mobility of the remaining carriers in the channel since traps act as Coulombic scattering sites when they capture a carrier. This explains why PMOS devices exhibit less flicker noise than NMOS devices; the PMOS channel is buried underneath the surface [83]. Typically, flicker noise is ignored in pipelined ADC analysis because it is assumed that the sampling rate and the input signal will be at a high enough

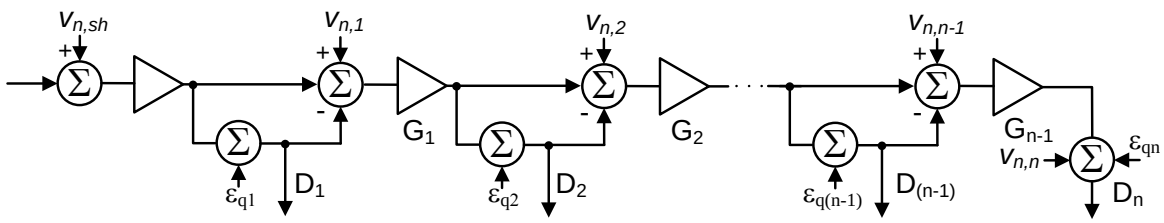


Figure 6.4 Pipelined ADC model for noise analysis

frequency that the effects of flicker noise can be neglected. However, since the system is designed for a biomedical application, the input signals could be quite slow, so flicker noise should be discussed.

The input referred flicker noise power spectral density (PSD) of a MOSFET, based on empirical data, can be written as

$$S(f)=\frac{K_F}{C_{OX}^2 WL}\frac{1}{f} \tag{6.22}$$

where K_F is a technology dependent parameter and C_{OX} is the oxide capacitance. The expression in Equation 6.22 indicates why flicker noise is often referred to as "1/f" noise. It is apparent that as frequency decreases, the flicker noise contribution increases. As the frequency increases, flicker noise and thermal noise will become equal at some point. Above that frequency, thermal noise dominates. This *corner frequency* can be found by setting the noise power spectral density for each noise type equal to one another. The corner frequency can be calculated as,

$$f_c=\frac{3I_D K_F}{8\pi kTC_{OX}^2 WLV_{OV}} \tag{6.23}$$

Bioimpedance measurements in the alpha dispersion spectrum (Appendix) can be as low as 100 Hz, so flicker noise must be accounted for.

Flicker Noise in Pipeline Stage

Unlike thermal noise, the analog switches used in the switched-capacitor implementation of the SHA and MDAC do not contribute significant flicker noise to the system. This is because they do not have a DC current flowing through them and are switched as a speed that is higher than the corner frequency. Therefore, the flicker noise contribution of these devices can be neglected.

The main source of flicker noise within each pipeline stage is the gain amplifier. The flicker noise PSD for a single MOSFET can be expressed as in Equation 6.22. As stated before, parameter K_F is a technology dependent parameter, but it also depends on the operation region of the transistor. In saturation region, it can be calculated as,

$$K_{Fsat}=\frac{q^2kTN_t(E)}{\gamma} \tag{6.24}$$

where

q	charge of an electron [1.602 x 10^{-19} Coulombs]
k	Boltzmann's constant [1.381 x 10^{-23} $m^2 \cdot kg \cdot s^{-2} \cdot K^{-1}$]
T	absolute temperature [K]
$N_t(E)$	the density of oxide traps per unit volume and unit energy [$cm^{-3} \cdot eV^{-1}$]
γ	the McWhorter tunneling parameter

In subthreshold, the inversion and the depletion capacitances become a factor and the equation for K_F becomes,

$$K_{Fsub}=\frac{q^2kTN_t(E)}{\gamma}\frac{1}{n^2}\left(\frac{C_{inv}}{C_{ox}}\right)^2 \tag{6.25}$$

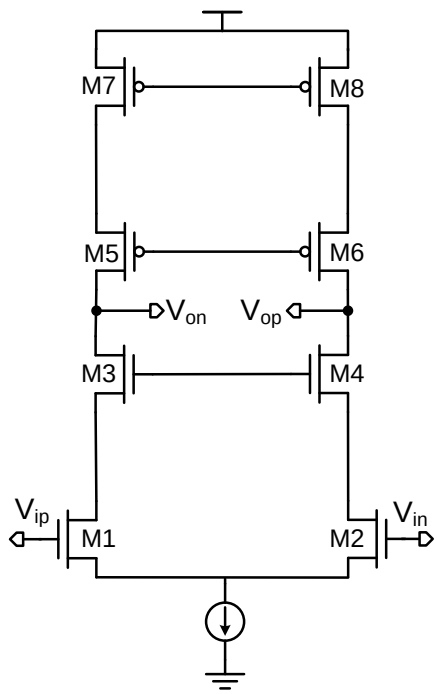


Figure 6.5 Telescopic amplifier used for gain stage noise analysis.

where $n = (C_{OX} + C_d)/C_{OX}$ and C_{inv} and C_d are the inversion layer and the depletion layer capacitances, respectively.

The telescopic amplifier shown in Figure 6.5 is used as the gain amplifier in this design. The input-referred noise power spectral density of the amplifier can be expressed as,

$$S(f)=2\left[\overline{v_{n1}^2}+\overline{v_{n8}^2}\left(\frac{g_{m8}}{g_{m1}}\right)^2\right] \tag{6.26}$$

Subbing in Equation 6.22 into Equation 6.26, the flicker noise PSD becomes,

$$S(f)=\frac{2K_{F1}}{C_{OX}^2W_1}\frac{1}{f}\left[\frac{1}{L_1}+\left(\frac{K_{F8}}{K_{F1}}\right)\left(\frac{I_{D8}}{I_{D1}}\right)\frac{L_1}{L_8^2}\right] \tag{6.27}$$

Typically, $I_{D1} = I_{D8}$ so the above equation can be simplified to,

$$S(f)=\frac{2K_{F1}}{C_{OX}^2W_1}\frac{1}{f}\left[\frac{1}{L_1}+\left(\frac{K_{F8}}{K_{F1}}\right)\frac{L_1}{L_8^2}\right] \tag{6.28}$$

where K_{F1} is the technology dependent parameter for the input devices and K_{F8} is the technology dependent parameter for the PMOS load devices. Equation 6.28 holds true from subthreshold to saturation. The K_F value will change depending on the operation region of the MOSFET devices; if they are in saturation or subthreshold, Equation 6.24 or 6.25 will be used, respectively. The (K_{F8}/K_{F1}) term is normally less than 0.5 [84], so it becomes evident that the first term is much greater than the second term, indicating that the biggest contributor to flicker noise is the input pair which is expected. To refer the noise to the input of the overall pipeline stage, the expression in (6.28) can be divided by the gain, and thus the input referred noise power spectral density for a single pipeline stage can be expressed as,

$$S(f)=\frac{2K_{F1}}{C_{OX}^2 W_1}\frac{1}{f}\left[\frac{1}{L_1}+\left(\frac{K_{F8}}{K_{F1}}\right)\frac{L_1}{L_8^2}\right]\cdot\left(\frac{C_f}{C_s+C_f}\right)^2 \tag{6.29}$$

In general, to reduce flicker noise, larger devices should be used. Similar to thermal noise, once the flicker noise for each stage is found, the total flicker noise can be referred to the input by summing all of the noise contributions from each individual stage, making sure to divide the noise contribution of stage N by the cumulative gains of all stages before it.

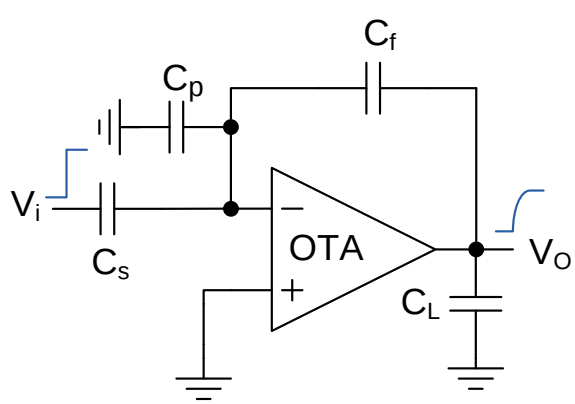


Figure 6.6 Sample-and-hold amplifier in MDAC.

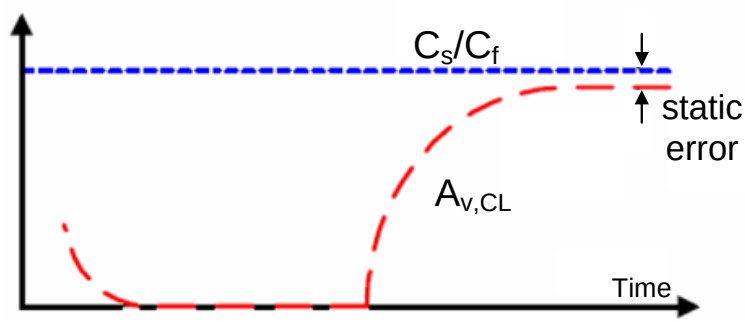


Figure 6.7 Illustration of static error caused by gain error.

6.3 Other Nonidealities in Pipelined ADCs

6.3.1 Finite Open Loop Gain

Ideally, the closed loop gain of an opamp is set precisely by the passive components in the feedback network. However, if the amplifier open loop gain is finite, the closed loop gain will be slightly different than the calculated value set by the passives. The gain will instead be a function of the passive elements along with the loop gain, but the expression can be simplified to be a function of the open loop. The gain of the MDAC in the hold mode depicted in Figure 6.6 can be expressed as,

$$A_{v,CL}=\frac{V_o}{V_i}\cong-\frac{C_s}{C_f}\frac{1}{1+\frac{1}{A}\left(1+\frac{C_s}{C_f}\right)} \tag{6.30}$$

where A is the OTA open loop gain.

Notice that if A is infinite, the gain expression is simply $A_{V,CL} = -C_s/C_f$. The smaller A is, the more the gain will deviate from the ideal expression. Recall the equation for D_{out} in Equation 4.12 in Chapter 4. If the digital gain and the analog gain are equal, the quantization noise will be canceled. Since the open loop gain of the amplifier is finite, the two gains will not be equal and more distortion will be passed in the residue. An illustration of static error caused by finite gain

is shown in Figure 6.7. The open loop gain required for the finite gain error to contribute less than ¼ LSB for a given stage can be found using [85],

$$\frac{1}{4\cdot LSB}=\frac{1}{4\cdot 2^{10}}=\frac{1}{4096} \tag{6.31}$$

Including a pessimistic feedback factor of 1/3, an open loop gain of 12288, or 81.8 dB, is required for 10-bit accuracy. Gain boosting or other gain enhancing techniques are often used in the beginning stages of a pipelined ADC to reduce finite gain error.

6.3.2 Finite Amplifier Bandwidth

The finite bandwidth of a non-ideal amplifier could prevent the residue voltage from being completely settled at the end of the sampling period. However, a large bandwidth requires high power consumption for analog designs, so to minimize power consumption, the bandwidth should be optimized. Equation 6.32 can be used to determine the unity gain bandwidth of the amplifiers used in each pipeline stage.

$$f_u=\frac{(N-n)\ln(2)}{\beta\pi}f_s \tag{6.32}$$

where N is the resolution of the overall converter, n is the per-stage resolution, β is the feedback factor, and f_s is the desired sampling rate.

6.3.3 Error Caused by Charge Injection

MOSFET switches have a large amount of mobile charge stored in its channel due to the gate capacitance. This charge is distributed between the source and the drain terminals based on the impedance seen by it during turn off [86]-[88]. Furthermore, the injected charge is also signal dependent and bottom plate sampling is used to alleviate this problem. The model for bottom plate sampling is shown in Figure 6.8. First, the switch, S_{1e}, is turned off. The charge stored in the channel will inject into the sampling capacitor, C_s, but since the switch is grounded, the

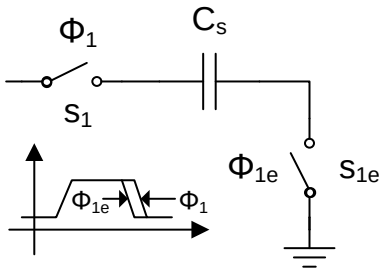


Figure 6.8 Bottom plate sampling model and its timing diagram.

amount of charge injected is fixed. Then when S_1 is turned off, no charge will inject into C_s, because the bottom plate of the capacitor is floating.

6.4 Summary

Matching is a fundamental limit in all analog circuits but in data converter design, it deserves special attention. Since high levels of accuracy are needed, unmatched components can lead to significant static errors. In a pipelined converter, the most critical matching components are the sampling and feedback capacitors in the MDAC structure. These capacitors set the residue gain factor, so small errors in the resultant residue voltage can lead to incorrect digital output codes. The analysis showed that the best way to improve matching is to use large components.

The biggest contribution to noise comes from the beginning pipeline stages since the later stage noise contributions are divided by the cumulative gains of all stages before it. Since each stage is implemented with a sample-and-hold configuration, most of the noise is in the form of kT/C noise from the sampling circuit. Flicker noise is also analyzed since the target application deals with low frequencies. The trend for improving noise performance is the same as improving matching which is to use larger capacitors.

Chapter 7 – Sub-Circuit Implementation

For switched-capacitor pipelined analog-to-digital converters, the gain amplifier used in the MDAC and the subADC comparators are fundamental blocks. They will be described in detail in this chapter. Other important blocks such as digital correction and clock generation will be described along with the layout of the final chip design.

7.1 Amplifier Design

From the discussions in the previous chapters, it is apparent that the gain amplifier within each pipeline stage has a significant effect on the overall performance of the converter. The open loop gain must be large enough to avoid introducing significant error in the closed loop gain. Sufficient bandwidth and slew rate are required to not introduce settling time errors. Sufficient output signal swing is needed to pass on the residue signal to a subsequent stage. Large common mode rejection ratio (CMRR) is desired to increase accuracy as well. All of these parameters must be optimized while being restricted by power consumption, chip area, and noise performance. In this work, three different amplifiers are needed to fulfill the needs of the system, and they will be described in the following sub-sections.

7.1.1 Gain Boosted Folded Cascode Amplifier in SHA

Recall that in the front-end SHA, a flip around sample-and-hold topology was chosen because of its superior settling performance and matching over the charge redistribution topology. The downside to using the flip around topology is that because the charge across the sampling capacitor will change directions between the sampling period and the hold period, the

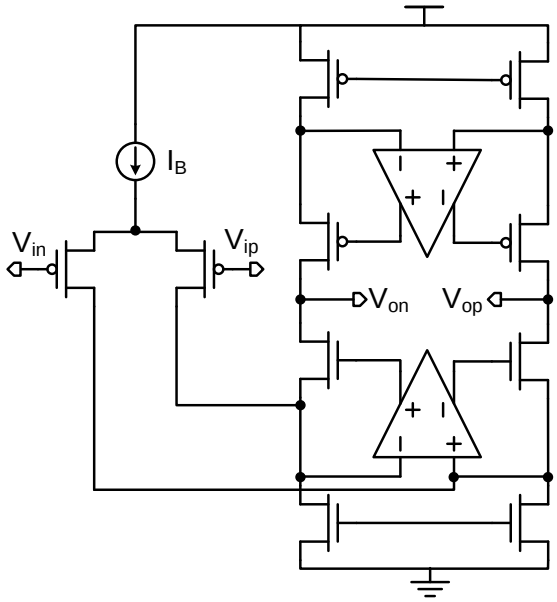


Figure 7.1 Folded cascode amplifier used in front-end SHA of pipelined ADC

input common mode range will vary. To combat this effect, a fully differential folded cascode amplifier was used. A schematic of the amplifier is depicted in Figure 7.1.

The folded cascode topology has two main disadvantages when compared to its telescopic counterpart. First, for a given slew rate, the folded cascode amplifier requires twice as much power than a telescopic amplifier due to the extra leg used to bias the input transistors. Another drawback is a larger excess noise factor because of the noise contributions from both PMOS and NMOS current mirror loads. The main advantages of this topology are increased input common mode range and CMRR. Since the input common mode voltage into the amplifier will fluctuate, the extra power spent implementing the SHA with a folded cascode amplifier is worth it to ensure proper operation.

The gain for this amplifier without gain boosting is roughly $(g_m r_o)^2$. Using typical values for the 130 nm process used in this work, a gain of approximately 50 dB can be expected. In section 6.3.1, it was determined that for 10-bit accuracy, a gain of roughly 82 dB is required.

Therefore, something must be done to boost the gain of the amplifier so that the stage does not contribute significant gain error. As shown in Figure 7.1, the gain boosting amplifiers are used to increase the gain to roughly $(g_m r_o)^4$. The gain boosting amplifier is also a folded cascode amplifier but biased with a fraction of the current. A potential drawback of the gain boosting technique is slow settling time due to a pole-zero doublet. However, this can be eliminated by moving the doublet to a frequency that is larger than the -3 dB bandwidth and smaller than the open loop non-dominant pole [89].

The input common mode range is roughly from ground to $V_{DD} - V_{THp} - 3V_{OVp}$, and the output common mode range is from $2V_{OVn}$ – to $V_{DD} - 2V_{OVp}$ where V_{THp} is the PMOS threshold voltage, V_{OVp} is the PMOS overdrive voltage, and V_{OVn} is the NMOS overdrive voltage. The unity gain bandwidth can be calculated as,

$$\omega_u = \frac{g_m}{C_L} \tag{7.1}$$

where C_L is the load capacitance which is not shown in Figure 7.1. The slew rate is determined by,

$$SR = \frac{I_B}{C_L} \tag{7.2}$$

For linear one pole settling, to avoid slewing, the slew rate must be larger than the maximum slope at the output, or

$$SR \geq \frac{d}{dt} V_o(t) = V_{step} \cdot \beta \cdot \omega_u \tag{7.3}$$

This is a difficult constraint to be satisfied so a small amount of slewing is unavoidable.

The input and the load transistors are sized so that they can operate in weak inversion during low speed mode in order to take advantage of the high transconductance efficiency while the bias transistors are kept in strong inversion to improve current mismatch and ensure reliable

operation at low currents across PVT variations. This results in some odd but acceptable aspect ratios for the bias transistors.

Common Mode Feedback (CMFB)

When using fully differential amplifiers, a common mode feedback (CMFB) circuit is required to regulate the output common mode voltage. Because the amplifier is being used in a switched-capacitor circuit, the switched-mode CMFB circuit shown in Figure 7.2 is used. Capacitors labeled C_2 generate the average of the output voltages, which is used to generate control voltages for the opamp current sources. The DC voltage across C_2 is determined by C_1, which is switched between bias voltages and is in parallel with C_2. C_1 may be ten to four times smaller than C_2, but they are both chosen in such a way that they will not significantly load the amplifier and maintain a large loop gain for the common mode feedback path. In applications where the amplifier is being used to realize a switched-capacitor circuit, such as this one, the switched-capacitor CMFB circuit is preferred because of the larger output swing capability over their continuous-time counterpart. A continuous-time CMFB circuit is implemented in the gain-boosting amplifier since large output range is not necessary. The bias circuitry for the folded cascode OTA is a slightly condensed version of the bias circuit shown in Figure 7.5. A simulated Bode plot of the amplifier is depicted in Figure 7.3.

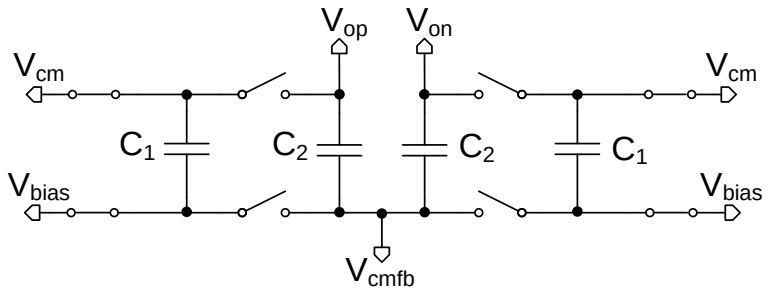


Figure 7.2 Switched capacitor common mode feedback circuit.

7.1.2 Gain Boosted Telescopic Amplifier

The fully differential, gain-boosted telescopic amplifier shown in Figure 7.4 is used in pipeline stages 1 and 2. The additional transistor in the path from VDD to GND makes its output range slightly smaller than the folded cascode amplifier, but the excess noise factor is smaller than that of a folded cascode amplifier. As a result, the overall dynamic range of the telescopic

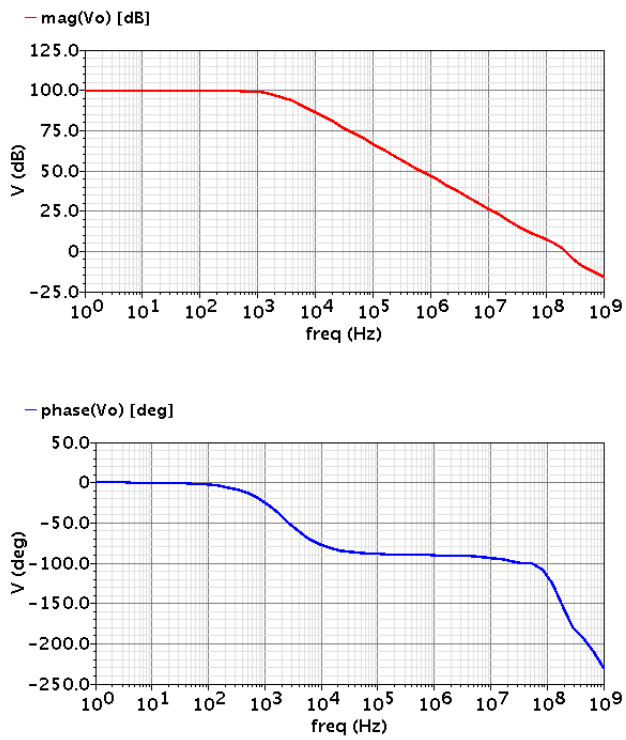


Figure 7.3 Simulated bode plot of folded cascode OTA used in SHA

amplifier is larger than the folded cascode. The input common mode range is roughly $2V_{OVn}+V_{THn}$ to $V_{OP(n)}+V_{THn}-V_{OV,}$ which could be quite small when the output swing is large. The output common mode range is from $3V_{OVn}$ to V_{DD}-$2V_{OVp}$. The unity gain bandwidth is still expressed as,

$$\omega_u=\frac{g_m}{C_L} \tag{7.4}$$

where C_L is the output capacitance, which is not shown in Figure 7.4. The slew rate is given by

$$SR=\frac{I_B}{C_L} \tag{7.5}$$

where I_B is the bias current for the differential pair.

The reconfigurable bias circuit for the telescopic OTA is shown in Figure 7.5. *Vpb* is the bias voltage for the PMOS current mirror load for the core amplifier and gain booster, *vpc* is the common mode voltage for the PMOS gain booster. *Vnb* is the bias voltage for the NMOS current mirror load for the core amplifier and gain booster. *Vncc* is the common mode voltage for the NMOS gain booster. *Vct* is the reference voltage for the switched-mode common mode feedback circuit, and *vx* is the common source node of the input differential pair which can track the input common mode voltage. The same switched-mode CMFB circuit depicted in Figure 7.2 was also used in this amplifier. A simulated Bode diagram of the gain boosted telescopic amplifier is depicted in Figure 7.5.

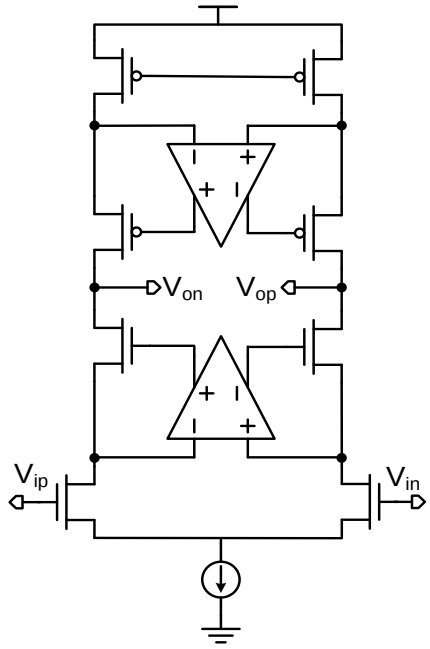


Figure 7.4 Gain boosted telescopic amplifier used in stages 1 and 2 of the prototype ADC.

7.1.3 Telescopic Cascode OTA

Stages 3 through 8 do not require the same high gain that the front-end SHA and two pipeline stage require. Therefore, a telescopic operational transconductance amplifier without gain boosting is used in these stages. Also the bias currents for these stages are reduced since the accuracy requirements are greatly reduced from the front-end stages. This way a significant saving is power is achieved. The design of the amplifier is the same as the one depicted in Figure 7.4 without the gain boosting amplifiers. The bias circuitry is also a less complex version of the scheme in Figure 5.3. The simulated bode plot of the telescopic cascode OTA is shown in Figure 7.6.

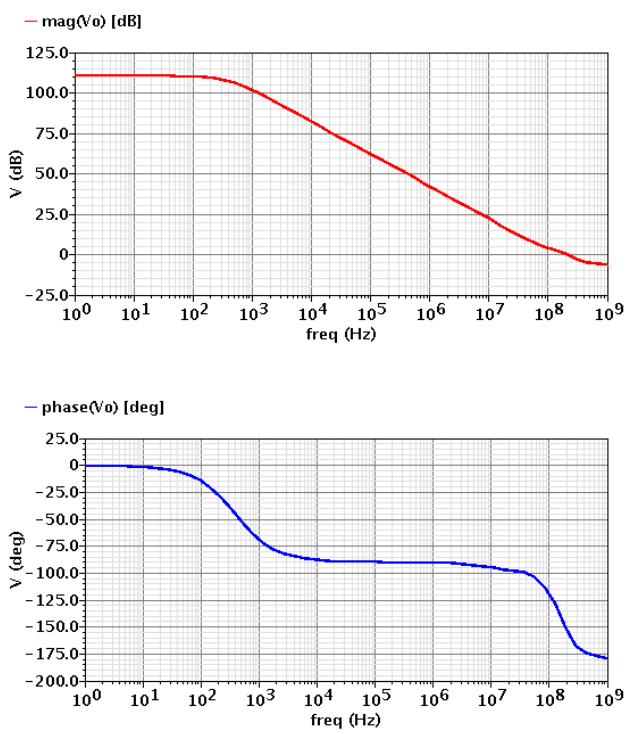


Figure 7.5 Simulated bode plot of gain boosted telescopic OTA used in pipeline stages 1 and 2.

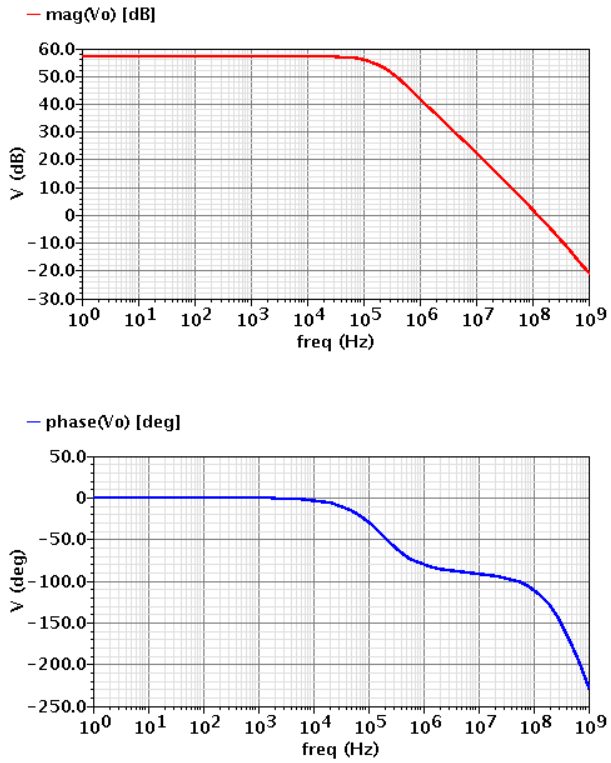


Figure 7.6 Simulated bode plot of telescopic OTA used in pipeline stages 3 through 8.

7.2 Sub-ADC Comparator Design

Analog-to-digital converter designs require high-speed, low offset comparators to distinguish between small voltage differences in a short amount of time. Additionally, low power operation is desired especially for implantable applications. Relatively high gain is needed to boost potentially small voltage differences to a level that can be sensed by the digital output. Typically, a high speed voltage comparator design will follow the block diagram shown in Figure 7.7. A pre-amplifier is used to amplify the difference between the two input signals and a positive feedback latch further increases the gain and the speed since stability is not an issue. Since high gain and high speed are contradictory, usually a number of low-gain, high-speed pre-amplifier stages are cascaded to achieve sufficient gain. The problem with these comparators are the pre-amplifiers contribute significant static power consumption for a large bandwidth and as

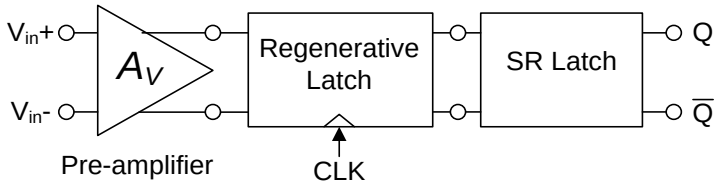


Figure 7.7 Block diagram of a typical high-speed voltage comparator.

CMOS technology scales, the intrinsic gains of the pre-amplifiers are reduced due to lower r_{ds} values. Consequently, a high-speed, low-power, fully-dynamic comparator without pre-amplification is used in this work. The comparator features low offset voltage and higher drive strength then conventional high speed comparators while only consuming dynamic power [90]. A schematic of the comparator is shown in Figure 7.8.

During the pre-charge phase (CLK = 0 V), the PMOS transistors P1 and P2 turn on and the capacitance at both *Di* nodes is charged to V_{DD}, which, as a result, turn the NMOS transistors N8 and N9 of the inverter pair on and discharge both *Di'* nodes to ground. Sequentially, PMOS transistors P4, P5, P8, and P9 turn on and the *Out* nodes and *Sw* nodes are charged up to V_{DD} while both NMOS transistors N4 and N5 are off.

During evaluation phase (CLK = V_{DD}), each *Di* node capacitance is discharged from V_{DD} to ground in a different rate proportional to the magnitude of each input voltage. As a result, an input dependent differential voltage is formed between *Di*+ and *Di*− nodes. Once either *Di*+ or *Di*− drops below $V_{DD} - |V_{THp}|$, the inverter pairs (P3/N8 and P10/N9) invert each *Di* node signal into the regenerated (amplified) *Di'* node. Then the regenerated *Di'* nodes which are 180° out of phase with the *Di* nodes, are relayed to the output-latch stage by P5, P8, N4, and N5. As the *Di'* voltage rises from 0 to V_{DD}, N4 and N5 turn on in succession and the output latch starts amplifying the small voltage difference transmitted from the *Di'* nodes into a full-scale digital

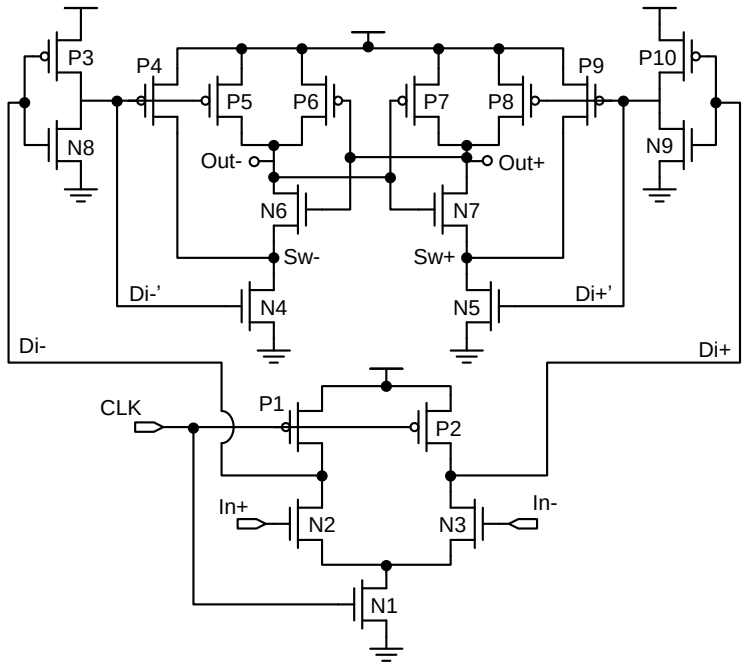


Figure 7.8 Fully Dynamic comparator used in subADC of each pipeline stage [90].

level: *Out*+ node outputs logic high if *Di*+*'* rises faster than *Di*− *'* node and *Out*+ outputs logic low otherwise. Once either *Out* node drops below $V_{DD} - |VT_{Hp}|$, this positive feedback becomes stronger because either P6 or P7 will turn on. The two inverters inserted between the *Di* and *Di'* nodes enable the comparator to have less input referred offset voltage in the output latch by regenerating the weak *Di* signal into the *Di'* signals [90].

7.3 Digital Correction

For a 1.5 bit per stage pipeline architecture, the sub-ADC compares the residual voltage output from each stage to two references voltage. Therefore, two bits, each with a half bit of redundancy, are resolved per stage. This redundancy must be eliminated for the final output code. A digital error correction circuit like the one depicted in Figure 7.9, can be used to take out the redundancy, but first, delay must be added to the digital outputs of earlier stages to remove timing skew. Stages 1 and 2 output codes require five clock cycles of delay, stages 3 and 4

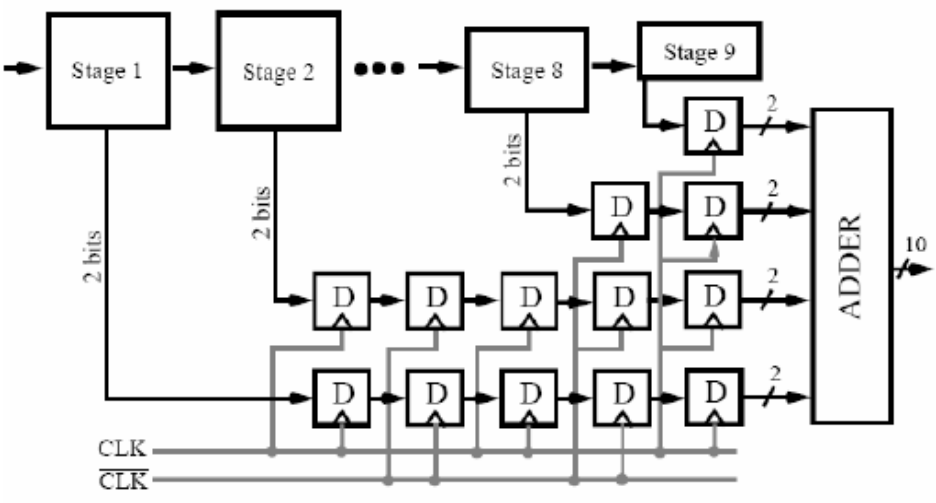


Figure 7.10 Digital correction and alignment circuit used to output final digital code.

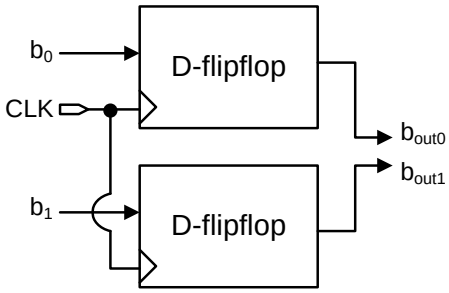


Figure 7.11 Delay block used in digital error correction logic.

output codes need a delay of four clock cycles, stages 5 and 6 output codes require a delay of 3 clock cycles, stages 7 and 8 output codes need a delay of 2 clock cycles, and the final stage only needs 1 clock cycle of delay. The delay block is displayed in Figure 7.10. Finally, a full adder is used to remove the redundancy [91]. The 1.5 bit per stage architecture along with the digital correction circuit reduce the accuracy requirements of the components in each pipeline stage and remove errors from the final output code.

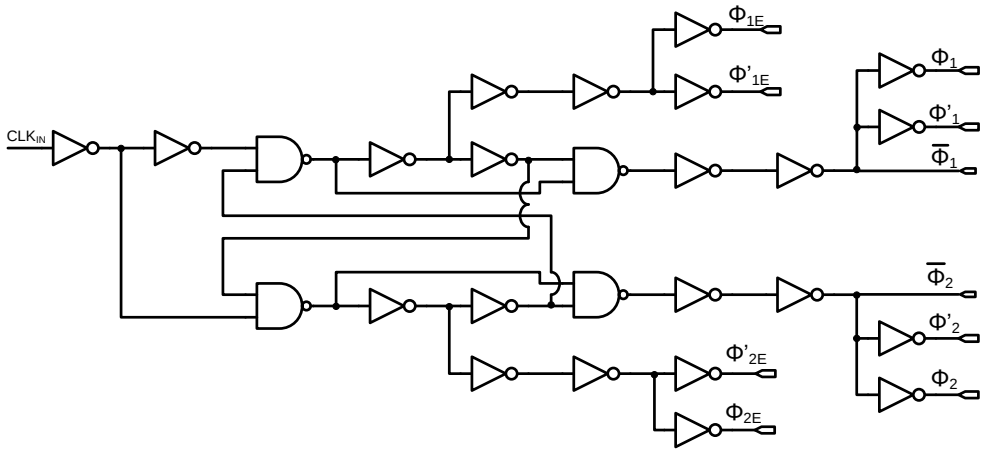


Figure 7.11 Circuit to generate all of the clock phases for the pipeline stages.

7.4 Clock Generation

The system in this work utilizes a buffered off-chip crystal oscillator for a global clock; however there are many different phases of that clock signal needed between the pipeline stages for the internal circuitry. The circuit responsible for generating all of these different clock signals is shown in Figure 7.11. The Φ_1 and Φ_2 set of clock signals serves as the clocks for adjacent pipeline stages. For example, stage 1 will operate on Φ_1, and stage 2 will operation on Φ_2. Each signal generated in the above circuit is split so that each stage gets its own set of clock signals. This way, if there is an issue with the clock of one stage clock, the remaining stages are unaffected.

7.5 Layout

Layout is a critical step in data converter design. Proper placement of system blocks and routing of important signals is of utmost importance while keeping in mind that a small, concise design is a major design constraint. Generally, the analog and digital parts are separated as much as possible. For example, the sub-ADC is placed on one side of the sampling and feedback capacitors while the residue gain amplifier is placed on the other side. The clock and the bias

generation circuits are placed in the middle of the system for easy distribution to the rest of the system, but the clock signals are not routed close to the reference voltage wires. The global reference signals are made wide since they carry a lot of current during settling, and they are routed around all of the pipeline stages. All good practice layout techniques such as common centroid layout, guard rings, and dummy transistors are used extensively throughout the system. More information on analog layout can be found in [92]. The final layout and micrograph of the design are shown in Figures 7.12 and 7.13, respectively.

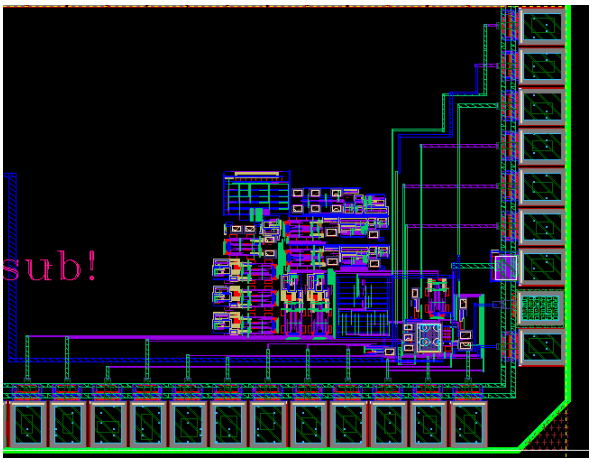


Figure 7.12 Final layout of the prototype reconfigurable pipelined ADC.

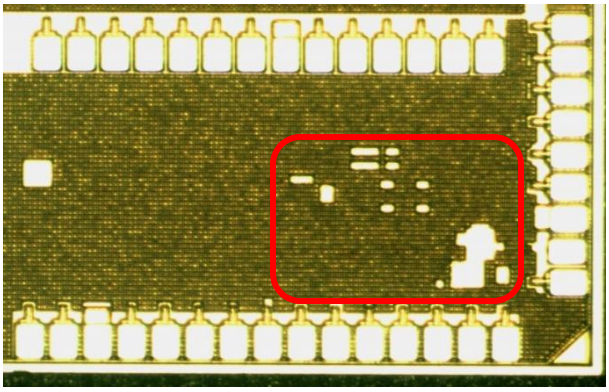


Figure 7.13 Micrograph of the reconfigurable pipelined ADC.

Chapter 8 – Measured Results

The proposed system has been designed and fabricated in a standard 130 nm bulk CMOS process with a 1.5 V power supply. A printed circuit board (PCB) test board was constructed to test the static and dynamic performance of the analog-to-digital converter as well as monitor key signals in the automatic-adaptation unit. In section 8.1, the performance metrics of the ADC are presented, and the performance is summarized and analyzed in section 8.2. In section 8.3, a comparison of this work to other analog-to-digital converters and specifically, reconfigurable, pipelined converters is carried out.

8.1 Test Results

The performance metrics for an analog-to-digital converter were described in Chapter 4. Linearity, or static, performance basically measures the accuracy of the ADC and is generally measured in terms of integral nonlinearity (INL) and differential nonlinearity (DNL) which were described in section 4.1.1. Ideally, to measure INL and DNL a linear ramp would be applied to so that each digital output code could be observed. However, this is impractical for the testing of high resolution data converters because of the inability to realize a highly linear, high-resolution ramp generator. Therefore, to measure the INL and DNL of the converter in this work, the histogram testing method from Maxim Integrated tutorial 2085 was used [93]. This method involves taking a high volume of data points and using a statistical approach to determine the linearity of an analog-to-digital converter. A slightly larger than full-scale amplitude is required

for this test which makes the results somewhat amplitude dependent, but the effects are insignificant.

The dynamic performance parameters include SNR, SNDR, SFDR, THD, and ENOB; all of which were defined in section 4.1.2. Similarly, MATLAB code based off Maxim tutorial 729 [94] was used to find the dynamic performance parameters of the proposed ADC. The basis of the measurement presented by the code is Fast Fourier Transform (FFT) analysis. Since the number of cycles used in acquiring the data is not an integer, the test data is said to be obtained through non-coherent sampling. Therefore, a window function is first employed to decrease spectrum leakage. There are three frequently used window functions including Hanning, Hamming, and flat top. Hanning was chosen for its good frequency resolution and reduced spectral leakage [94]. By summing all of the FFT bins (f_{SAMPLE}/N), the harmonics, and the noise, separately, all of the dynamic performance parameters can be determined.

8.1.1 High-Resolution (10-bit) Mode

Static Results

Figures 8.1 and 8.2 depict the INL and DNL of the converter when applying a 183 kHz sinusoidal wave, respectively. The INL and DNL values mainly reflect the matching in the sampling capacitors and gain error caused by finite open loop gain. The low INL and DNL values indicate good matching and linearity, and the absence of an INL error greater than 0.5 and a DNL error greater than 1.0 indicate that there are no missing codes. Table 8.1 compares the static performance of the converter to the applied signal amplitude. It can be seen that the linearity does not significantly vary with a change in the amplitude. There also does not seem to be a positive or negative correlation between an increase or decrease in the amplitude and a change in the linearity performance. To see how the input signal frequency affected the linearity

performance, measurements were taken with a varying input signal frequency. Input signals below 50 kHz were sampled at 100 kS/s while signals above 50 kHz were sampled at 20 MS/S. The results are shown in Table 8.2. The INL and DNL get worse with an increase in frequency due to increased errors caused by settling and finite bandwidth as well as increased charge injection effects.

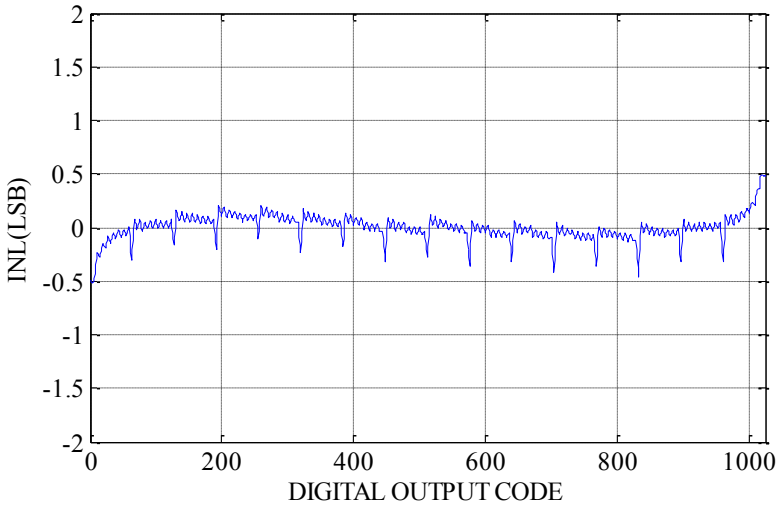


Figure 8.1 Integral nonlinearity of proposed ADC in 10-bit mode.

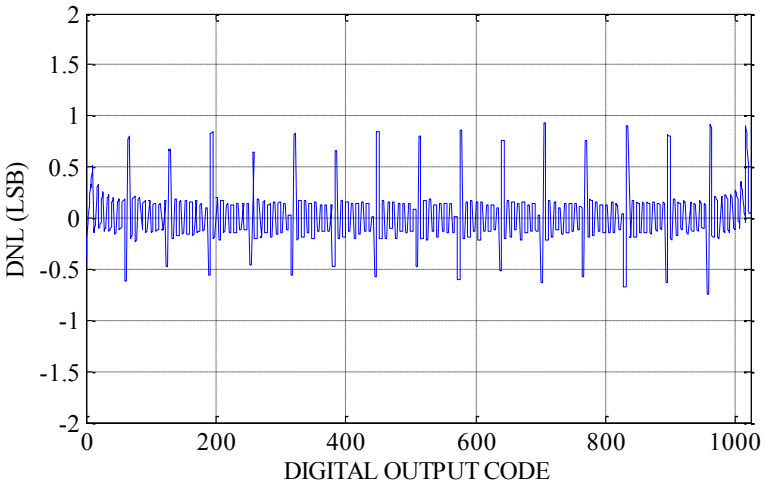


Figure 8.2 Differential nonlinearity of proposed ADC in 10-bit mode

Table 8.1 Comparison of Full-scale Amplitude and Linearity (10-bits)

Input Amplitude (FS)	INL	DNL
1.004	+0.48/-0.52	+0.93/-0.75
1.019	+0.48/-0.50	+0.98/-0.75
1.040	+0.46/-0.51	+0.95/-0.80
1.060	+0.47/-0.50	+0.96/-0.74
1.081	+0.47/-0.53	+0.92/-0.83

Table 8.2 Comparison of Input Frequency and Linearity (10-bits)

Input Frequency	INL	DNL
1.267 kHz	+0.48/-0.50	+0.95/-0.76
5.487 kHz	+0.46/-0.51	+0.99/-0.59
12.913 kHz	+0.51/-0.49	+1.08/-0.45
29.014 kHz	+0.55/-0.53	+1.51/-0.68
75.593 kHz	+0.48/-0.47	+0.89/-0.76
239.153 kHz	+0.48/-0.50	+0.95/-0.72
567.109 kHz	+0.58/-0.54	+0.91/-0.63
1.967 MHz	+0.60/-0.75	+1.24/-0.63
4.329 MHz	+0.89/-1.01	+1.51/-0.68

Dynamic Results

To obtain dynamic parameters for the converter, a 16,384 point FFT analysis was conducted Figure 8.3 illustrates the results. The different symbols of varying colors denote the 2nd through 9th order harmonic tones. Figure 8.4 shows how SNR and SNDR are affected by a change in the input signal frequency. The decrease in SNDR is due mainly to increased distortion as the input frequency is increased. As expected, the total harmonic power is increased as the applied signal frequency increases as is depicted in Figure 8.5. The ENOB as a function of frequency is shown in Figure 8.6. Since ENOB is closely related to SNDR (Equation 4.7), it makes since that ENOB decreases gradually with frequency.

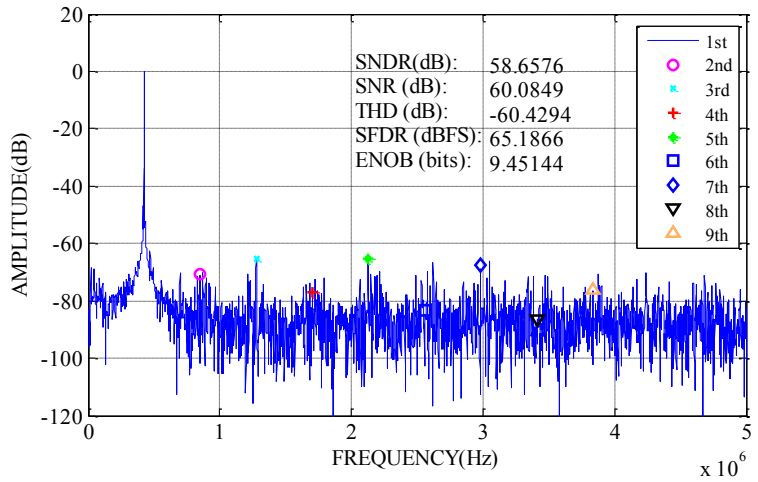


Figure 8.3 16,384 point FFT analysis of ADC to determine dynamic performance in 10-bit mode.

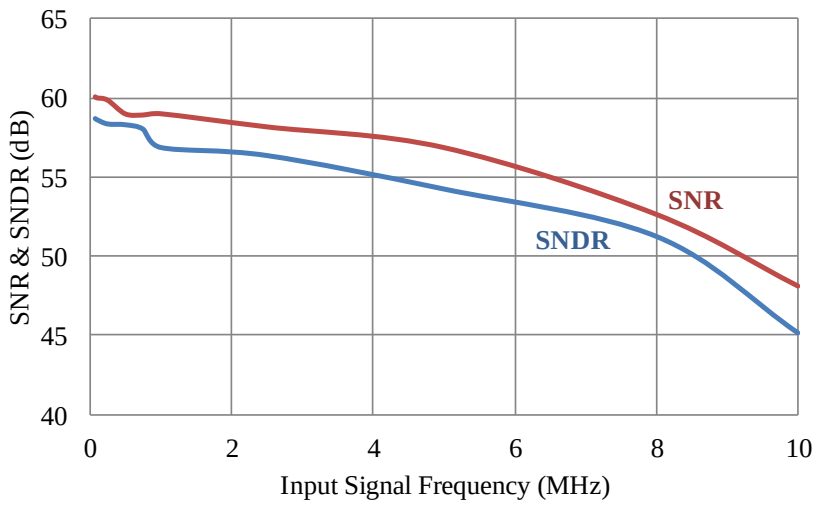


Figure 8.4 SNR and SNDR versus input signal frequency for the ADC in 10-bit mode.

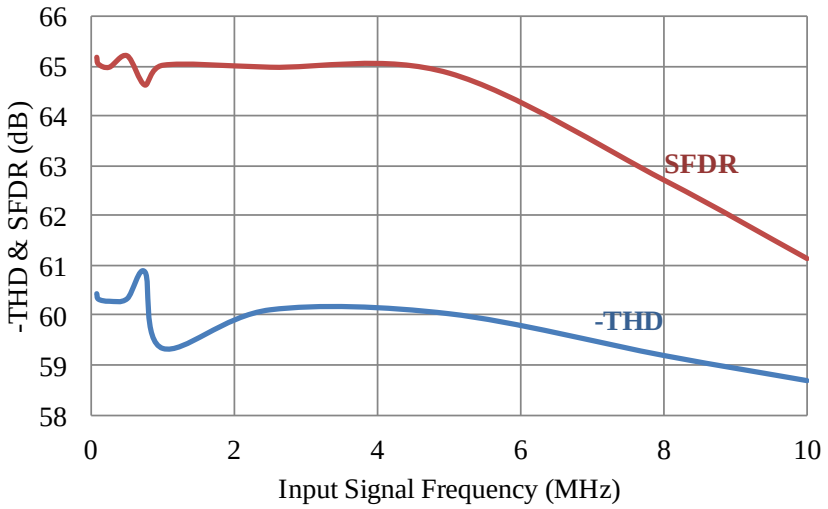


Figure 8.5 SFDR and THD versus input signal frequency for the ADC in 10-bit mode.

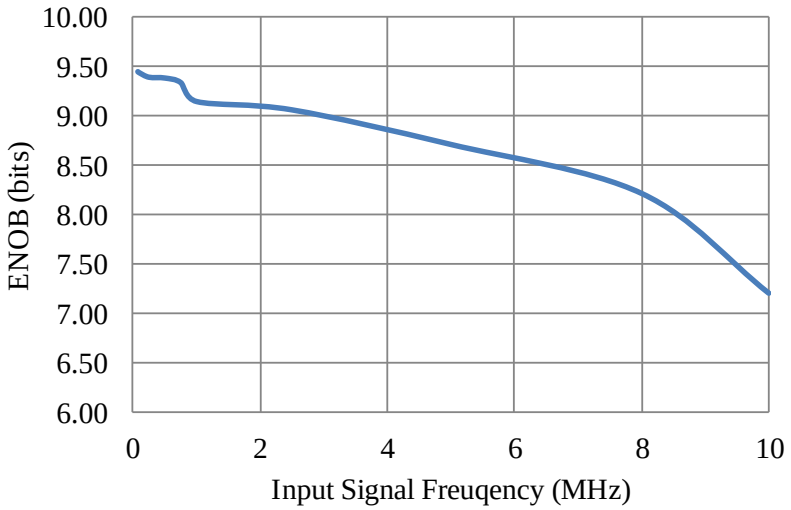


Figure 8.6 ENOB versus input signal frequency for the ADC in 10-bit mode.

8.1.2 Low-Resolution (8-bit) Mode

Static Results

Figures 8.7 and 8.8 depict the INL and DNL of the converter when applying a 183 kHz sinusoidal wave to the converter in 8-bit mode, respectively. The INL and DNL values remain

low, indicating good matching and linearity. However, the absence of the front-end sample-and-hold amplifier degraded the INL slightly resulting in a maximum INL error greater than 0.5. Therefore, there could be missing codes in the ADC transfer function in 8-bit mode. The maximum DNL error remains below 1.0. Table 8.3 compares the static performance of the ADC in 8-bit mode to the input amplitude. As in the high-resolution case, there does not seem to be a positive or negative correlation between an increase or decrease in the amplitude and a change in static performance. Table 8.4 shows how the input signal frequency affected the linearity performance. Once again, the degradation in INL and DNL as the input frequency is increased is mainly due to increased errors caused by settling and finite bandwidth as well as increased charge injection effects.

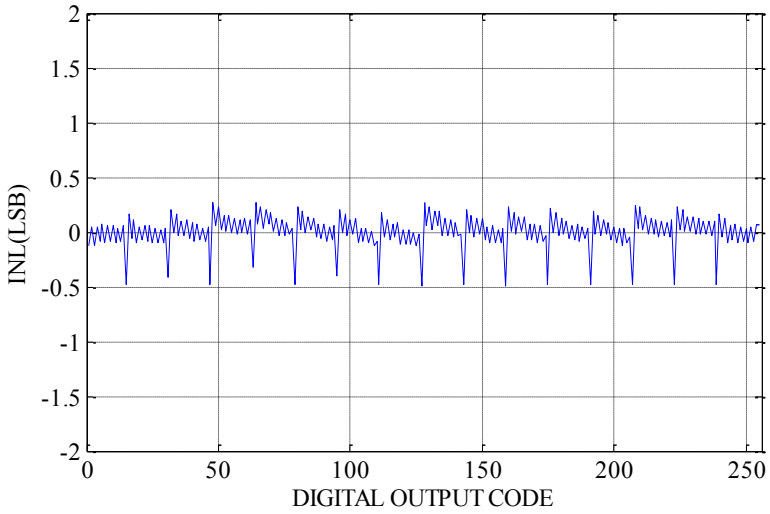


Figure 8.7 Integral nonlinearity of proposed ADC in 8-bit mode

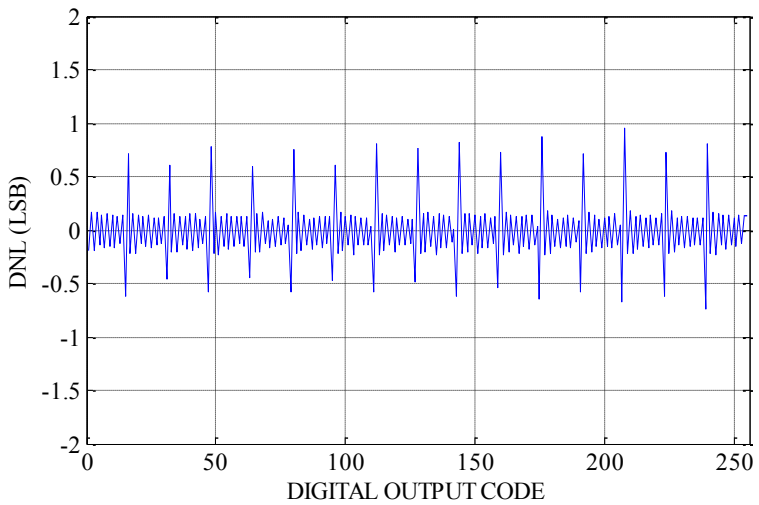


Figure 8.8 Differential nonlinearity of proposed ADC in 8-bit mode

Table 8.3 Comparison of Full-scale Amplitude and Linearity (8-bit)

Input Amplitude (FS)	INL	DNL
1.004	+0.37/-0.79	+0.95/-0.74
1.019	+0.38/-0.81	+0.98/-0.75
1.040	+0.39/-0.82	+0.95/-0.74
1.060	+0.37/-0.82	+0.96/-0.74
1.081	+0.38/-0.81	+0.95/-0.74

Table 8.4 Comparison of Input Frequency and Linearity (8-bit)

Input Frequency	INL	DNL
1.267 kHz	+0.37/-0.79	+0.95/-0.76
5.487 kHz	+0.60/-0.80	+0.99/-0.59
12.913 kHz	+0.51/-0.84	+1.08/-0.45
29.014 kHz	+0.91/-1.07	+1.51/-0.68
75.593 kHz	+0.34/-0.71	+0.89/-0.76
239.153 kHz	+0.38/-0.69	+0.95/-0.72
567.109 kHz	+0.48/-0.85	+0.91/-0.63
1.967 MHz	+0.69/-.92	+1.24/-0.63
4.329 MHz	+1.02/-1.13	+1.51/-0.68

Dynamic Results

The 8,192 point FFT analysis used to test the dynamic performance of the converter in 8-bit mode is shown in Figure 8.9. The different symbols of varying colors denote the 2nd through 9th order harmonic tones. A graph that plots SNR and SNDR versus the input signal frequency is shown in Figure 8.10.

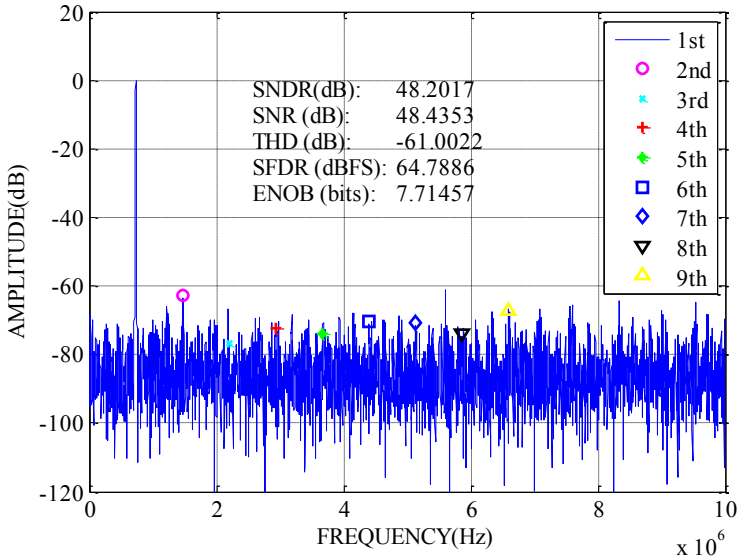


Figure 8.9 8,192 point FFT analysis of ADC to determine dynamic performance in 8-bit mode.

The decrease in SNDR is due mainly to increased distortion as the input frequency is increased. Since the ADC is implemented with a fully differential topology, the 2nd order harmonics should be canceled out leaving the 3rd harmonic as the main spurious tone. However, due to mismatch and other distortions, the 2nd order harmonic still contributes significant power to the output spectrum. In Figure 8.11, THD is plotted as a function of input signal frequency, and similar to the high-resolution configuration, the total harmonic power increases with frequency. The ENOB as a function of frequency is shown in Figure 8.12. Since ENOB is

closely related to SNDR (Equation 4.7), it makes since that ENOB decreases gradually with frequency.

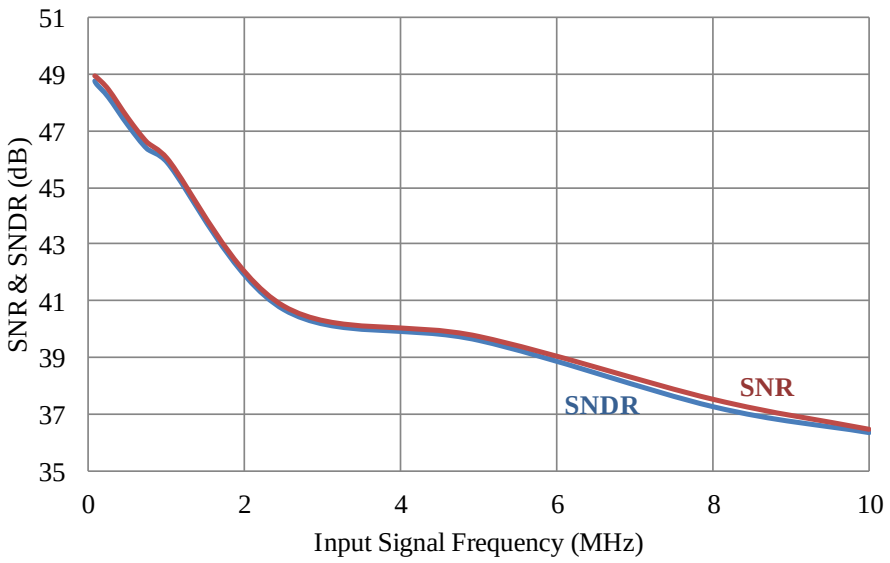


Figure 8.10 SNR and SNDR versus input signal frequency for the ADC in 8-bit mode.

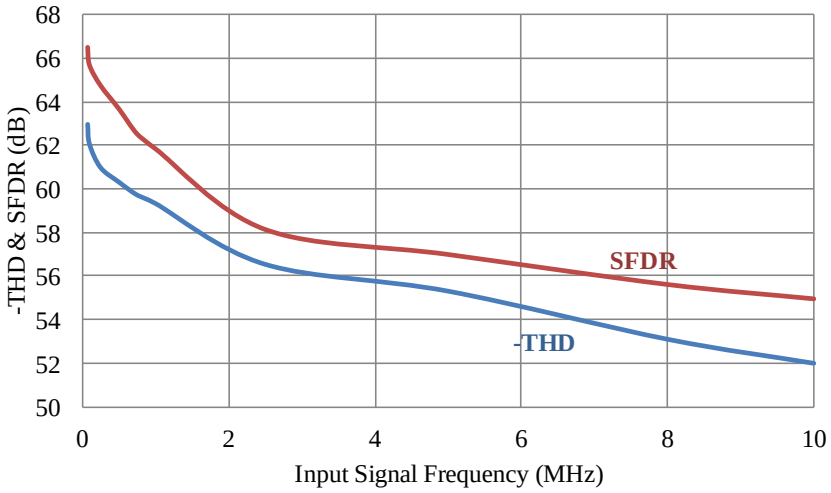


Figure 8.11 SFDR and THD versus input signal frequency for the ADC in 8-bit mode.

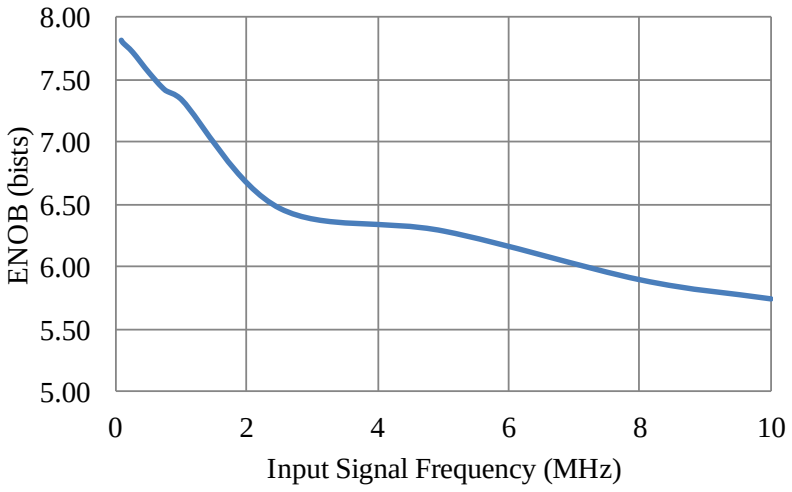


Figure 8.12 ENOB versus input signal frequency for the ADC in 8-bit mode.

8.1.3 Automatic Adaptation

Two graphs illustrating the functionality of the automatic adaptation unit are shown in Figures 8.13, 8.14, and 8.15. Figure 8.13 illustrates how the automatic adaptation unit responds to a changing input signal frequency. Ideally, when the input signal frequency is less than 50 kHz, the sampling rate control bit is logic 1. As the frequency increases, the voltage generated by the frequency-to-voltage converter decreases until it is beneath the reference voltage. Once the input signal frequency is greater than 50 kHz, the control bit switches to logic 0. Actually, the transition frequency is around 37 kHz, but this is due to bad matching in the on-chip resistors used to set the reference voltage for the comparator. Notice there is roughly a 20 μsec delay between when the frequency changes and the control bit switches. This is because it takes time for the FVC voltage to change since large capacitors were used at the output.

In Figure 8.14, the input signal is originally below 250 mVpp, so the resolution control bit is logic 1. Once the input amplitude is increased past 250 mVpp, the control bit changes to logic 0. The final control bit is an inverted version of the output of the comparator for the

configuration to work out. Figure 8.15 just illustrates the auto adaptation unit's ability to respond to a signal that changes frequency and amplitude simultaneously.

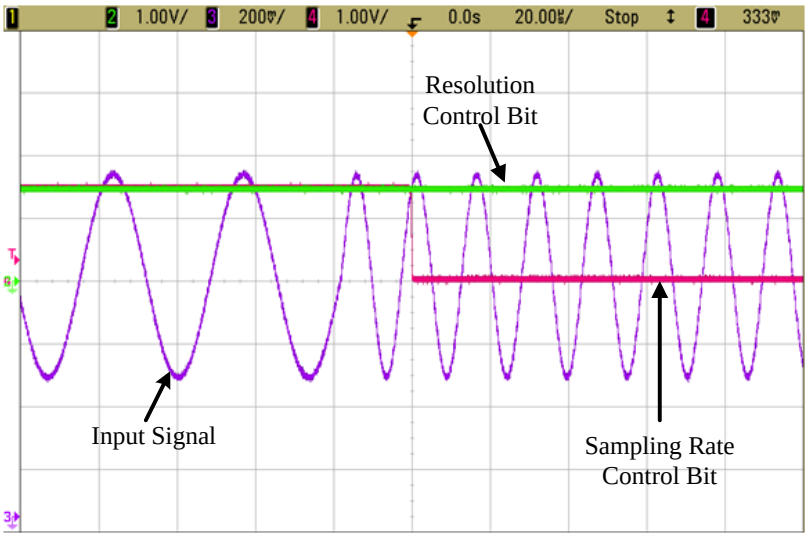


Figure 8.13 Oscilloscope graph illustrating automatic adaptation unit's ability to respond to a changing frequency.

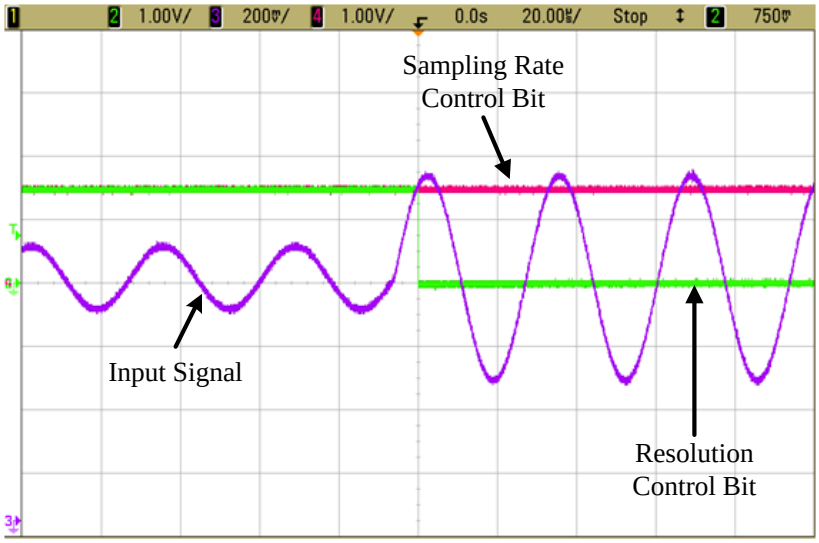


Figure 8.14 Oscilloscope graph illustrating automatic adaptation unit's ability to respond to a changing amplitude.

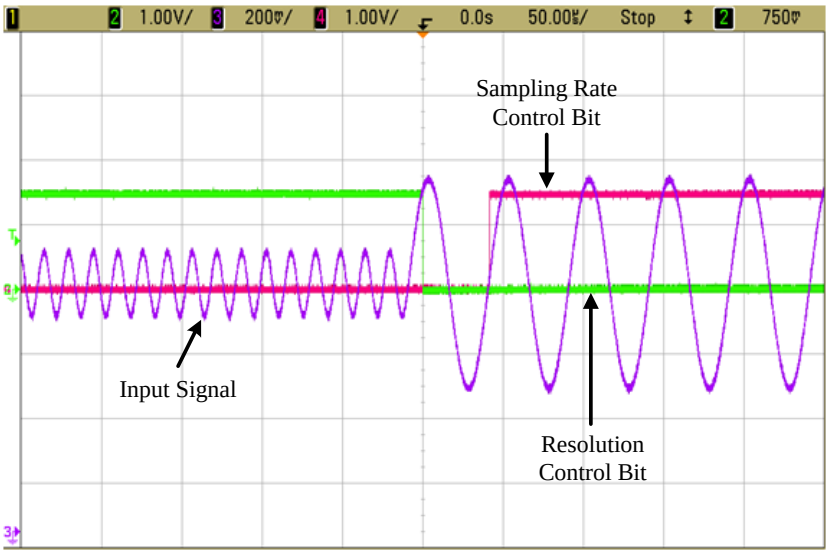


Figure 8.15 Oscilloscope graph illustrating automatic adaptation unit's ability to respond to both a changing frequency and amplitude simultaneously.

The automatic adaptation unit consumes 32 μW and occupies 0.014 mm^2 of chip area, and since each block is current biased, it exhibits consistent, reliable functionality. The frequency-to-voltage converter output voltage as a function of the input signal frequency is plotted in Figure 8.16. The linear range of the converter is quite narrow spanning from about 10 kHz to 40 kHz. This is mainly due to the circuit itself. Recall the expression for the FVC output voltage in Equation 5.6 [$V_{out}=\frac{I_B}{(2\cdot f\cdot C)}$]. With a supply voltage of 1.5 V, if the circuit is designed such that 50 kHz produces the mid voltage of 750 mV, the maximum voltage would theoretically be produced at 25 kHz. In practice, the maximum voltage is achieved sooner than that because of the on resistance of the bias transistor. A 375 mV output would be produced from a 100 kHz input, and so on. In Figure 8.15, the frequency range from 100 Hz to 20 kHz all produces the maximum achievable voltage because of the V_{ds} of the biasing transistor. At frequencies above 100 kHz, the change in voltage is not as significant as the voltage changes in the frequency

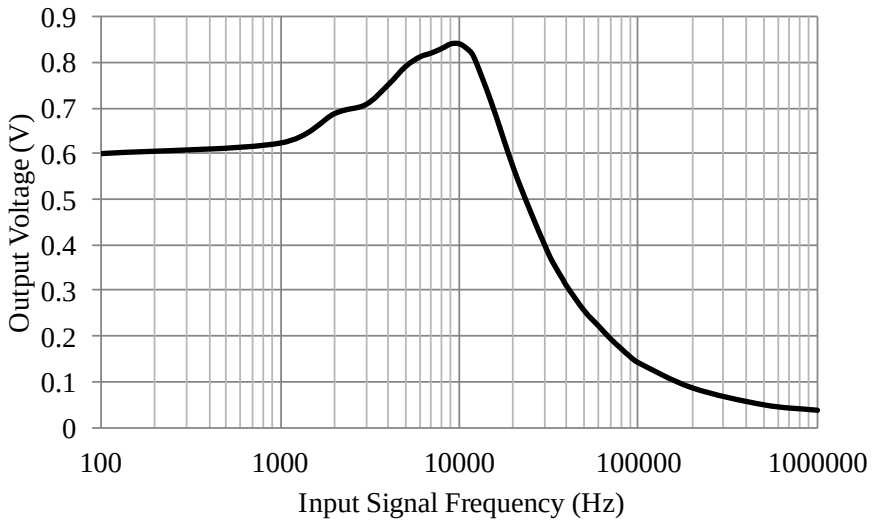


Figure 8.16 FVC generated voltage versus input signal frequency.

spectrum centered around the mid voltage. This is acceptable for bioimpedance monitoring, however, since the only distinction required is frequencies higher or lower than 50 kHz.

The envelope detector output versus input signal amplitude is shown in Figure 8.17. Similar to the FVC, the linearity of the transfer characteristic for the envelope detector is not very high. This is because the peak detector is biased with subthreshold transistors to minimize

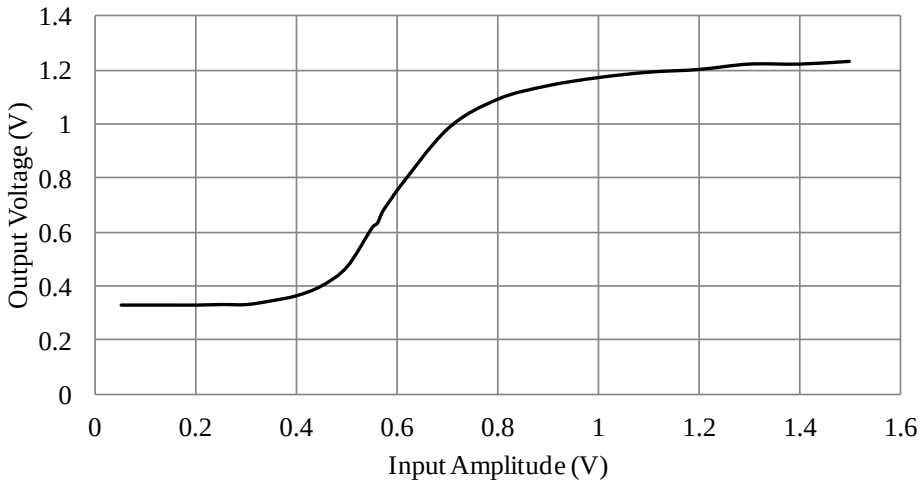


Figure 8.17 Envelope detector output voltage versus input signal amplitude.

power consumption. As a result, there is an exponential relationship between the input amplitude and output voltage. Again, this is acceptable since the only distinction is between amplitudes above and below 250 mV.

8.2 Performance Summary

The performance of the reconfigurable analog-to-digital converter is summarized in Table 8.5. The static parameters were determined with an input signal frequency of 183 kHz. The dynamic parameters were obtained from a 16,293 point FFT analysis with a 427 kHz input signal in high-resolution mode and a 8,192 point FFT analysis with a 427 kHz input signal in low-resolution mode.

Table 8.5 Performance Summary of ADC

	High-Res	Low-Res
Sampling Rate (MHz)	0.1 / 20	0.1 / 20
Resolution (bits)	10	8
SNR (dB)	60.08	46.36
SNDR (dB)	58.66	46.56
ENOB (dB)	9.45	7.41
THD (dB)	-60.43	-59.73
SFDR (dB)	65.15	62.56
INL	+0.48/-0.50	+0.37/-0.79
DNL	+0.93/-0.75	+0.95/-0.74
Power (mW)	0.016 / 1.061	0.009 / 0.440
FOM* (fJ/conv)	157 / 51	540 / 130

***FOM = $P/(2^{ENOB} \cdot f_{SAMPLING})$**

The presence of an INL value greater than 0.5 indicates that there could be missing codes in the ADC transfer curve, although, further inspection of the INL plots show that these maximum values are the result of large periodic spikes. These spikes are caused by access interference in the fourth least significant bit of the digital output code. Using the definition for signal-to-noise

ratio, SNR = 6.02N + 1.76, where N is the resolution of the converter, it can be observed that the dynamic performance is also satisfactory. These results verify that an auto-adapting reconfigurable analog-to-digital converter with reasonable performance can be realized.

Bioimpedance Example

The proposed ADC system was used in a bulvine aortic smooth muscle cell bioimpedance measurement test setup and the results are shown in Figure 8.18. The excitation signal and corresponding voltage drop that was reconstructed from the ADC output codes are presented on the same graph to observe the phase shift due to the membrane capacitance.

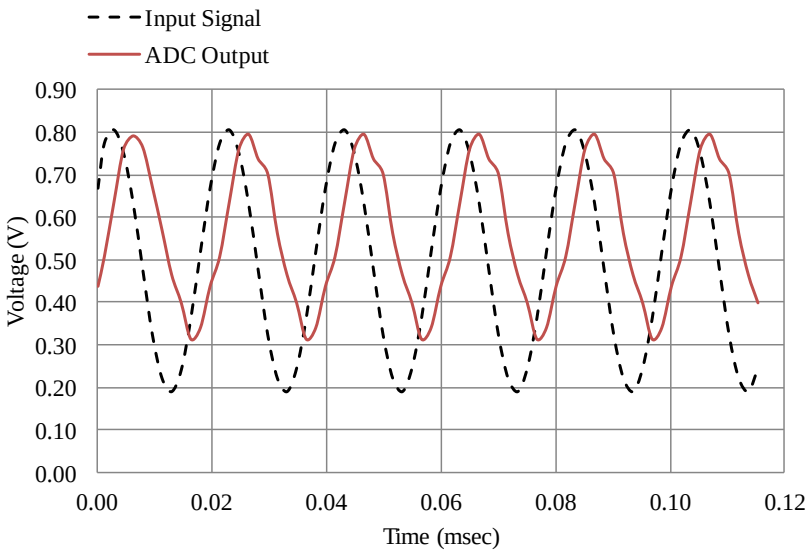


Figure 8.18 Sample bioimpedance measurement data using the proposed pipelined ADC.

8.3 Previous Work Comparison

It is difficult to directly compare different ADC designs across a wide range of sampling rates and resolutions. To attempt to do so, researchers generally report a figure-of-merit (FOM).

Table 8.6 Reconfigurable Pipelined ADC Comparison

	This Work	[53]	[48]	[95]
Technology	130 nm	180 nm	180 nm	90 nm
Supply Voltage	1.5 V	1.8 V	1.8 V	1.2 V
Sampling Rate (MS/s)	0.1 / 20	10 - 80	0.1 - 10	0.4 - 44
Resolution	8 / 10	10	10	10 - 12
Power (mW)	0.0016 / 1.06	81 - 94	0.158 - 1.95	0.184 - 22.87
SNDR (dB)	48.2 / 58.7	58.8 - 56.5	56.4 - 53.5	59.1 - 66.6
FOM (pJ/conv)	0.157 / 0.051	11.4 - 2.15	3.37 - 0.50	0.50 - 0.35
Core Area (mm^2)	0.426	1.9	0.6	1.0

There have been different definitions of FOM, but the mostly widely used definition and the one used in this work is expressed as,

$$\mathrm{FOM} = \frac{P}{2^{\mathrm{ENOB}} f_{\mathrm{SAMPLING}}} \tag{8.1}$$

where P is the average power consumption. The unit for FOM is energy per conversion, so it is a measure of how efficiently an ADC can convert a single analog value into a digital code. Table 8.6 compares the ADC in this work to a few previously reported reconfigurable pipelined converters. The ADC in this work exhibits comparably low power consumption and area. It also achieves competitive FOM at 51.7 fJ/conv. The main source of power saving in low speed mode is the use of subthreshold region along with smaller currents. In high speed mode, significant power is saved by the use of a fully dynamic, high-speed comparator.

In Figure 8.19, the proposed converter is compared to all pipelined analog-to-digital converters published in ISSCC and VLSI journals from 2004 to 2014. The converter in this work is consistent with the trend of achieving an ENOB between 8 and 12 bits while achieving a very

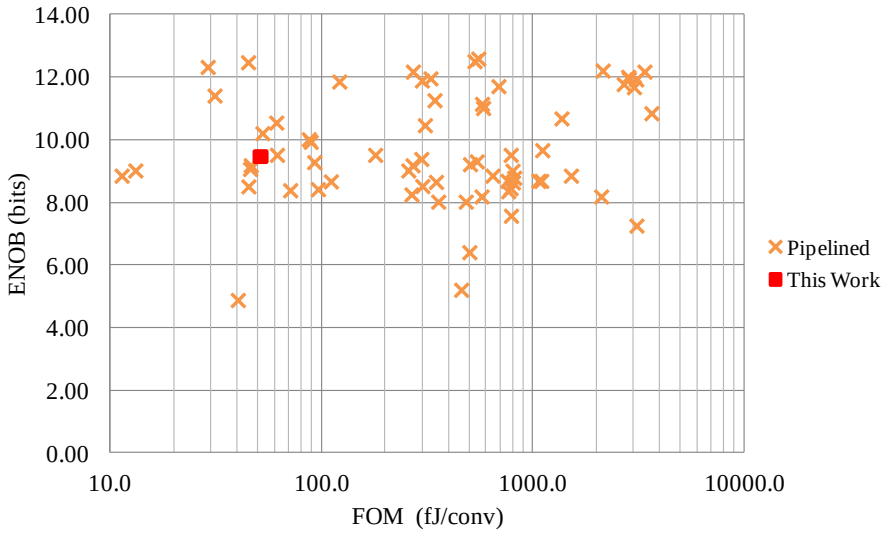


Figure 8.19 Comparison of proposed converter to all pipelined converters published in ISSCC and VLSI from 2004 to 2014.

low FOM. Many of the converters with a lower FOM were either fabricated in a much more modern CMOS process allowing them to experience less dynamic power consumption or took advantage of a non-opamp based approach [11].

Next, the proposed converter was compared to all analog-to-digital converters with a sampling rate of 20 MS/s or higher published in ISSCC and VLSI since 2009. The results, shown in Figure 8.20, reveal that only a handful of SAR and ΔΣ ADCs with an ENOB above 8 bits achieve a lower FOM than the converter presented in this work. These results confirm that an auto-adapting, reconfigurable pipelined converter can be realized with state-of-the-art performance. Lastly, the converter presented in this work was compared to all reconfigurable ADCs published in ISSCC and VLSI since 2009, and the results are shown in Figure 8.21. Only one converter achieves a lower FOM.

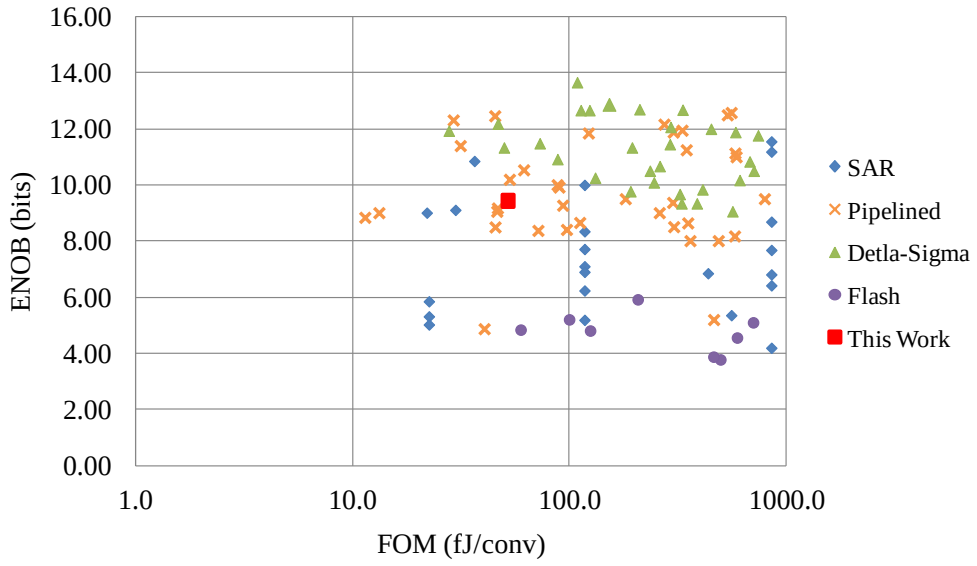


Figure 8.20 Comparison of proposed converter to all ADCs published in ISSCC and VLSI from 2009 to 2014.

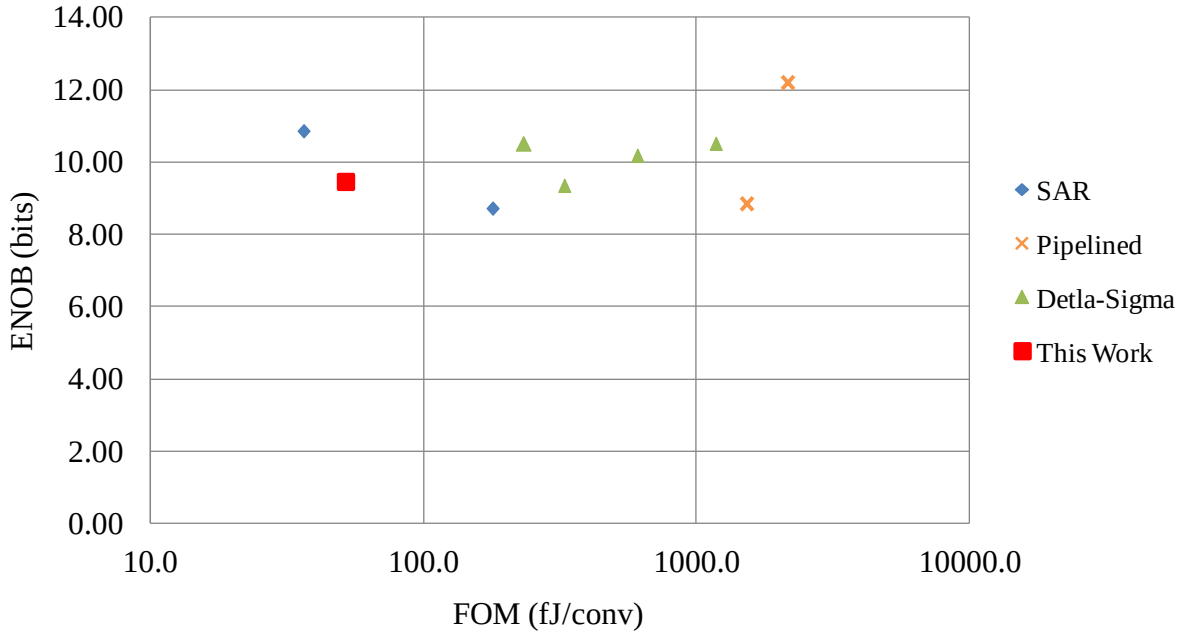


Figure 8.21 Comparison of proposed converter to all reconfigurable ADCs published in ISSCC and VLSI from 2009 to 2014.

Chapter 9 – Discussion and Conclusion

A discussion of the previously mentioned results and a few other unaddressed issues is given in this section. Finally, conclusions are drawn, the original contribution is discussed, and future works are presented.

9.1 Discussion

The resolution and reconfiguration schemes presented in this work can be expanded to a wide variety of applications. The system in this work was optimized for implantable bioimpedance applications, but the biasing and operating regions for the circuits used to implement the system can easily be altered for different applications. Using Equation 4.1, the bias current and storage capacitance can be set to make the range of the FVC appropriate for a given application. With the use of the elimination interference technique, the resolution configuration scheme is viable at high sampling frequencies and with smaller feature size processes. If more sampling rate options are required, more elaborate back-end circuitry after the FVC could be developed.

Since the target application for the proposed system is implantable electronics, no special attention was given to extreme temperature operation. In the development of each sub-circuit in the system, simulations were carried out at room temperature and 37 °C (human body temperature). There were no significant variations in the performance of each sub-block at 37 °C, so it is safe to assume that the overall converter will maintain proper functionality at this temperature as well.

Many of the reference signals such as the master clock, reference voltages, and bias currents were generated using off-chip components. A fully-integrated design would offer numerous benefits such as less noise, interference, and better temperature performance. While an on-chip, high-speed clock can be very power hungry; it can also be designed to have less jitter than an off-chip crystal oscillator. An on-chip clock generator will also have less opportunity to interfere with other important signals. The bias current generation circuit uses mostly on-chip components with the exception of the resistor which ultimately sets the current value. An integrated resistor along with precision trimming can ensure that the desired current values are generated. An alternative approach would be to use a constant-gm biasing scheme which would allow the system to be used in wider temperature range applications. There are four critical reference voltages in the design of the pipelined converter; all of which were generated off chip. They are the input common mode voltage, the output common mode voltage, and the two voltage levels used in the 1.5 bit per stage implementation. These references have to be incredibly stable since a LSB voltage is on the order of a few millivolts. On-chip voltage references would be less susceptible to outside noise and interference than discrete regulators. Buffers would be needed to keep the output impedance as low as possible since the converter can draw large amounts of transient current.

The histogram method used to determine INL and DNL is not the only way to determine the linearity of an analog-to-digital converter, so the results should be accepted but with some skepticism. There have been many different ADC testing methods published [96], [97], and either of them could produce better or worse results than the ones obtained from the histogram method. There are a number of factors that affect static performance measurement such as sample size. The single instance of captured samples from a logic analyzer cannot fully represent

the performance of a converter. This is why it is preferred to take a larger number of samples. The histogram method was used in this work because of its convenience and ease of implementation.

As mentioned earlier, since noncoherent sampling was used in the testing of the converter presented in this work, a window function must be applied to the signal before conducting an FFT analysis. Windowing of the input data is equivalent to convolving the spectrum of the original signal with the spectrum of the window. Different windows have different effects on resolution and spectral leakage. Hanning was chosen for this work for the previously mentioned reasons, but other popular windows include Hamming and flat top. It is possible that a different window or coherent sampling could lead to better results. A more in depth discussion on windowing can be found in [94].

9.2 Original Contributions

The most significant contribution of this work is the presentation of a reconfigurable, pipelined analog-to-digital converter that automatically adapts its resolution and sampling rate to the input signal to be sampled. Most previously reported reconfigurable ADCs require third party control to configure the converter. Another contribution of this work is demonstrating that a reconfigurable, pipelined ADC that utilizes weak-inversion biasing with competitive performance can be realized. Subthreshold data converters have been exhibited before, but never in a reconfigurable architecture. A novel automatic adaptation unit that is optimized for bioimpedance monitoring has been presented. Lastly, in-depth flicker noise analysis for a pipelined converter has been conducted.

9.3 Conclusion

A low-power, reconfigurable pipelined analog-to-digital converter has been presented. The converter is able to adapt its resolution and sampling rate according to requirements determined by the input signal amplitude and frequency. Furthermore, this adaptation happens automatically with the help of a simple circuit. The converter can output either 8 or 10 bit digital codes at a sampling rate of 100 kS/s or 20 MS/s. In 8-bit mode, the converter has a maximum integral nonlinearity and differential nonlinearity of +0.37/-0.79 LSB and +0.95/-0.74 LSB, respectively, while achieving 7.4 effective bits of resolution. In 10-bit mode, the converter has a maximum INL and DNL of +0.48/-0.50 LSB and +0.93/-0.75 LSB, respectively, while achieving 9.4 effective bits of resolution. The converter itself consumes 9.1 to 16.1 μW of power in slow mode and 440 μW to 1.06 mW in fast mode depending on the resolution with a supply voltage of 1.5 V. The core converter occupies 0.426 mm^2 in a standard 130 nm bulk CMOS process. The automatic adaptation unit consumes 31.8 μW and only occupies 0.014 mm^2 of chip real estate.

The figure of merit for the presented ADC is among the best for reconfigurable ADCs to date when compared to converters published in ISSCC and VLSI from 2009 to 2014. The proposed system offers an unconventional tradeoff between power efficiency, speed, and performance that is not characteristic of most implantable biomedical applications. Instead, the system has been optimized for bioimpedance monitoring which is a growing tool for biological and medical research.

9.4 Future Work

There are a lot of opportunities for future work in this project. First, the clock signals and reference voltages could be implemented on chip. For convenience and ease, all of the bias voltages and the two clock options are implemented off chip. This increases the chance for noise

and interference during testing. For a more compact and self-sufficient design, a low jitter global clock can be designed along with highly stable voltage references. The clock applied to the data converter determines the timing of the samples produced from the input signal. Basically, jitter describes the timing errors in the sampling operation caused by clock disturbances. Significant clock jitter can greatly degrade ADC performance, and so a well-designed oscillator would be required for the system. Similarly, highly stable, on-chip voltage references would improve the design of the system presented in this work. 1 LSB for a 10-bit converter is equal to ~1 mV. If the voltage references used to make decisions on the output bits of the final digital code fluctuate by more than this, then errors could show up in the output code, especially at higher frequencies.

Additional low power strategies could be employed to further reduce the power of the system. This design makes use of a front-end sample-and-hold amplifier, which helps increase accuracy at the cost of significant power and area, in 10-bit mode. The system could be re-designed without the use of a SHA in either mode, and special attention could be given to ensure that the accuracy of the system did not suffer too much. Also, current-modulated power scaling could be utilized along with adaptive biasing to greatly reduce the power consumption. CMPS was discussed earlier in Chapter 4, and it was mentioned that the method was not used because of the added complexity and area penalty. If the design were to be optimized strictly for low power, CMPS could be implemented. Another architectural change that would lead to power savings is opamp sharing. The combination of all of these techniques would greatly reduce the power consumption of the system but also make the system more complex. Both CMPS and opamp sharing have stringent timing requirements as to not introduce significant error in the final output code.

Finally, a non-opamp based pipelined converter would be another interesting development for this system. In Chapter 2, comparator-based and ring amplifier-based, pipelined stages were both mention. Coupling either of these two relatively new topics along with the reconfigurability of the system would make for an extremely power-efficient, versatile analog-to-digital converter.

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Appendix

Circuit Theory behind Bioimpedance

Impedance is a common term used in electrical systems, and it represents the relationship between voltage and current in a system. Impedance encompasses two elements, *resistance* and *reactance*. Resistance is the opposition to the flow of electrons. Similarly, reactance is also a measure of the opposition to electron flow but is also a function of frequency. A typical impedance measurement might be written as

$$267 + 130j\ \Omega$$

The above expression implies that there are 267 Ω of resistance and 130 Ω of reactance. The above expression also sheds some light on how resistance and reactance affect the relationship between current and voltage. Resistance has the same affect on DC and AC current. That is to say, when an AC current flows through a resistor, the corresponding voltage drop is in phase with the current. However, in terms of bioimpedance, reactance is caused by the presence of a capacitance. Capacitance is an expression of the extent to which an electronic circuit, component, or system stores and releases charge. DC current cannot pass through a capacitor whereas an AC current can because of the rapid flux of charge. The voltage drop across a pure capacitance will lag 90° behind the current through it; therefore, a voltage drop across a resistive and capacitive network will lag somewhere between 0 and 90° depending on how much of the impedance is resistive and reactive. The complex impedance can be converted to a magnitude and phase to give a more insightful measurement of impedance. For example,

$$267 + 130j = 296\ \Omega \text{ at } 26°$$

So the combination of 267 Ω of resistance and 130 Ω of reactance equates to voltage drop as if there was 296 Ω of resistance but lagging 26° behind the current.

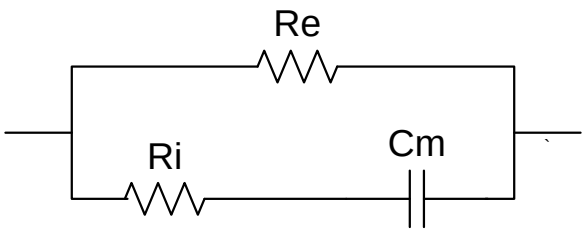

Figure A.1 Bioimpedance circuit component model. Re is the extracellular resistance, Ri is the intracellular resistance, and Cm is the cell membrane capacitance.

Impedance in Biological Tissue

Bioimpedance can be modeled as an extracellular resistance, an intracellular resistance, and membrane capacitance (Figure A.1). Both the intracellular and extracellular spaces are highly conductive because of the presence of salt ions; however, the lipid membrane of cells is an insulator which acts as a capacitor. At low frequencies, the measurement is purely resistive, and corresponds to the extracellular resistance as no current passes through the intracellular path because it cannot cross the cell membrane capacitance. At high frequencies, the current can pass through both intracellular and extracellular spaces and so a reactive element is introduced [98], [99]. This phenomenon is illustrated in Figure A.2.

The movement of current in the different compartments of the cellular spaces and the corresponding resistance and reactance values are best displayed on a Cole-Cole plot which is

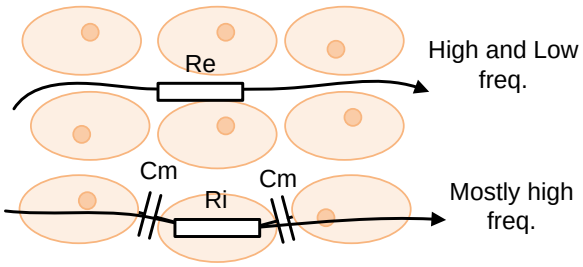

Figure A.2 Current flow through extracellular and intracellular space

illustrated in Figure A.3. Low frequency measurements are purely resistive as no current can pass through the cell membrane capacitance, and so these measurements correspond to the extracellular resistance. As the frequency increases, more current passes through the membrane; therefore, the phase angle of the voltage drop increases as well. At high frequencies, the membrane capacitance becomes negligible, so the measurement becomes purely resistive again. However, this time the measurement is due to the extracellular and intracellular spaces. At some frequency, the current passing through the capacitive path reaches a maximum; this point is called the center frequency.

Three frequency regions have been determined to describe the dielectric properties of biological materials. These properties effect bioimpedance measurements independent of the current amplitude and membrane capacitance because of dispersions of the conductivity and permittivity as seen in Figure A.4 [100].

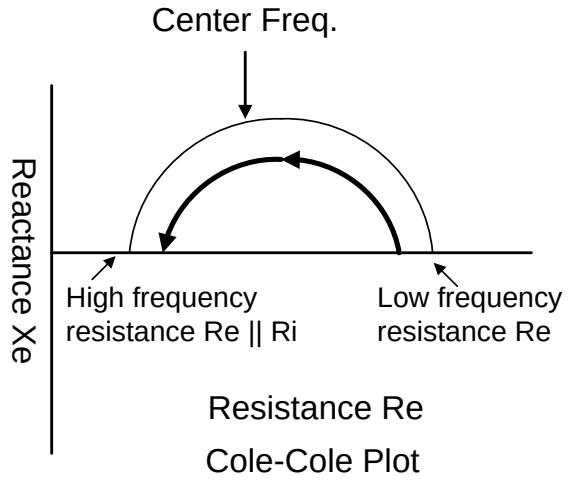

Figure A.3 Cole-Cole plot illustrating frequency effects on bioimpedance measurements.

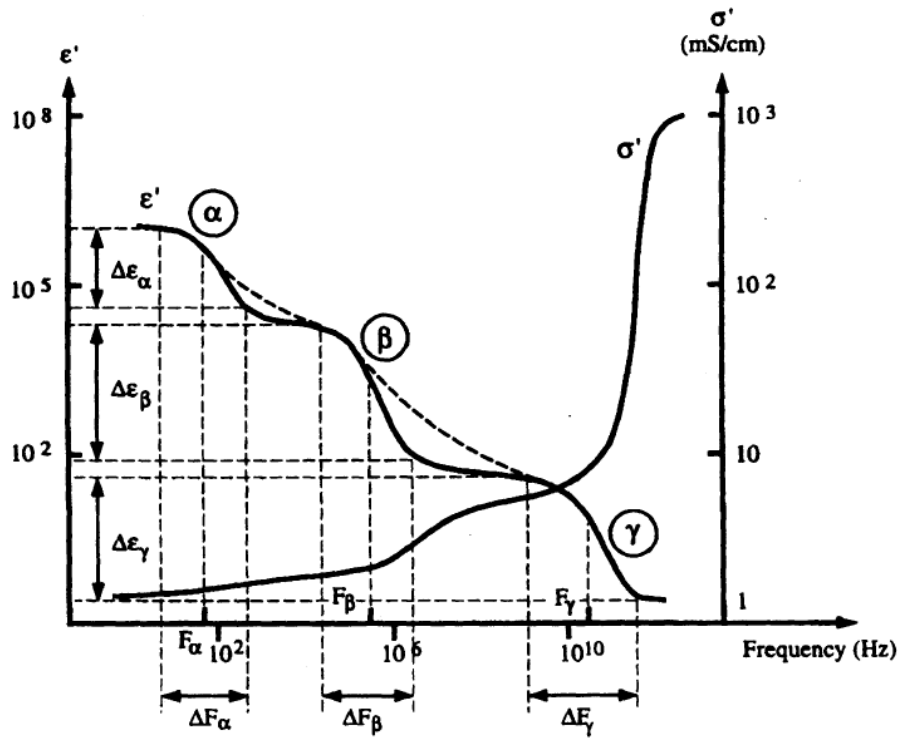

Figure A.5 Conductivity and permittivity changes over the three dispersion regions from [100].

The large dielectric dispersions that appear in the mHz – 1 kHz spectrum is known as alpha (α) dispersion. It is generally associated with the diffusion processes of ionic species, counterion effects near the membrane surface, and active cell membrane effects. Beta (β) dispersion is between 1 kHz and 100 MHz and is due to the dielectric properties of cell membranes and their interactions with extracellular and intracellular electrolytes. Lastly, gamma (γ) dielectric dispersion is mostly accredited to the dipolar mechanisms in water and the presence of salt and protein molecules. It is most prevalent at frequencies between 100 MHz and 100 GHz. Most changes in biological tissue happen in the alpha and beta dispersion spectra, so they are the focus for most bioimpedance studies [98], [99], [101].

It is necessary to define a parameter, constant phase element (CPE), in order to accurately fit the traditional capacitance model into actual bioimpedance measurements. The CPE is not

physically realizable with ordinary lumped components, but it is usually described as a capacitance that is a function of frequency. The value of CPE can be expressed as,

$$Z_{CPE}=\frac{1}{(j\cdot 2\pi\cdot f\cdot C)^{\alpha}}$$

The α parameter is usually between 0.5 and 1. Notice that when α = 1, the CPE behaves like an ideal capacitor. When CPE is included in the simple bioimpedance model depicted in Figure A.1, the expression of impedance becomes

$$Z=R_{\infty}+\frac{R_0-R_{\infty}}{1+(j\cdot 2\pi\cdot f\cdot \tau)^{\alpha}}$$

where R_{∞} represents the impedance at infinite frequency, R_0 is the impedance at 0 Hz, τ is the time constant (ΔR·Cm) where $\Delta R = R_{\infty} - R_0$, and α is the parameter from CPE. The above expression is known as the Cole-Cole equation and corresponds to the Cole-Cole plot in Figure A.3.

Impedance Measurement

Bioimpedance measurements are made by injecting an AC current into the target biological tissue and measuring the corresponding voltage drop. Usually, the four electrode method is used to bypass the inclusion of the electrode impedance in the measurement. Two of the electrodes belong to the current source while the other two electrodes belong to a high performance amplifier to read the voltage drop. A typical bioimpedance monitoring system is shown in Figure A.6. The in-phase multiplication of the instrumentation amplifier output produces the magnitude information, while the cos(90°) multiplication gives the phase information.

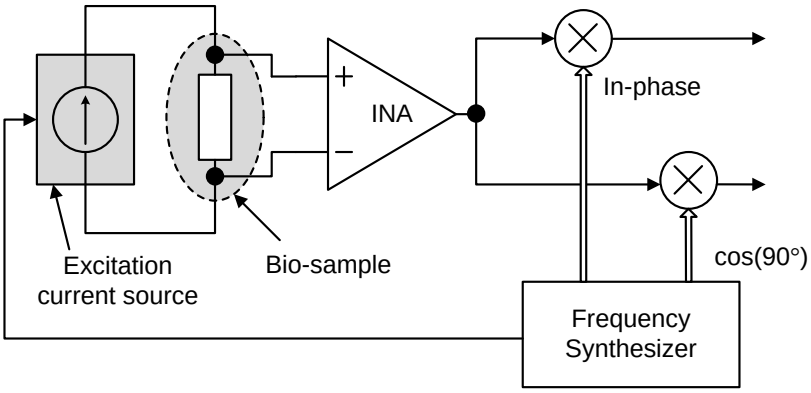

Figure A.6 Typical bioimpedance monitoring system.

Vita

Terence Randall was born in Memphis, TN to the parents of Danny and Sandra Randall. He is the second of two sons. He attended Crump Elementary until the second grade when he transferred to Germantown Elementary School. When he got to high school, he changed schools again to Cordova High School where he graduated in the top 20 of his class. Terence followed his older brother to the University of Tennessee, Knoxville for his undergraduate studies. The summer before his senior year, Terence worked as an intern for Shaw Industries in Chickamauga, GA. Terence graduated Summa Cum Laude with a bachelor's degree in electrical engineering in May 2010. Immediately after graduation, he accepted an NIH fellowship entitled Program for Excellence and Equity in Research (PEER) and entered the electrical engineering Ph.D. program and Analog, VLSI, and Devices Laboratory. Terence received his Ph.D. from the University of Tennessee, Knoxville in December 2014. He dreams of leading a circuit design team for a major electronics company in Austin, TX