12-2014

High-Efficiency Three-Phase Current Source Rectifier Using SiC Devices and Delta-Type Topology

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To the Graduate Council:

I am submitting herewith a dissertation written by Ben Guo entitled "High-Efficiency Three-Phase Current Source Rectifier Using SiC Devices and Delta-Type Topology." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

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High-Efficiency Three-Phase Current Source Rectifier Using SiC Devices and Delta-Type Topology

A Dissertation Presented for the

Doctor of Philosophy

Degree

The University of Tennessee, Knoxville

Ben Guo

December 2014

Acknowledgement

First of all, I would like to express my deepest gratitude to my advisor, Dr. Fred Wang, for his support and guidance during my Ph.D. study. With profound understanding of power electronics, Dr. Wang has provided me numerous valuable ideas and advices. Since the beginning of my Ph.D. study, he has shown great patience and trust to me. He taught me how to do a solid research, shared his passion with me, and then turned me loose. With enough freedom, I am able to think out of some innovative ideas.

I would like to thank Dr. Leon. M. Tolbert, for his suggestions on my research and encouragement. He gave me much assistance on reviewing my publications and supervising the industry project. He provided me many chances to present my work to the visitors and showed me how important the presentation was for my career. Also I would like to thank Dr. Benjamin. J. Blalock for his general suggestions.

I would like to thank Dr. Daniel Costinett and Dr. Ohannes Karakashian for kindly accepting my invitation as my Ph.D. committee members and giving me valuable suggestions on my dissertation.

I would like to thank ABB for the three-year support on my Ph.D. study. I would like to thank Dr. Rolando Burgos and Dr. Eddy Aeloiza for their challenging questions and valuable advices. I am really impressed by the professional attitude and diligence of Dr. Burgos. I still remember that Dr. Burgos had revised my first conference paper over 7 times before it was submitted.

I would like to thank all my colleagues in the power electronics lab in the University of Tennessee, Knoxville. They are Dr. Ming Li, Dr. Shengnan Li, Dr. Dong Jiang, Dr. Lijun Hang,

Dr. Jingxin Wang, Dr. Wenjie Chen, Dr. Xiaoling Yu, Dr. Wanjun Lei, Dr. Faete Filho, Dr. Mithat Can Kisacikoglu, Dr. Lakshmi Reddy Gopi Reddy, Dr. Zhuxian Xu, Mr. Bradford Trento, Dr. Bailu Xiao, Ms. Jing Wang, Ms. Yutian Cui, Mr. Yalong Li, Mr. Wenchao Cao, Mr. Yiwei Ma, Mr. Zhiqiang Wang, Ms. Xiaojie Shi, Ms. Liu Yang, Ms. Yang Xue, Mr. Bo Liu, Mr. Edward Jones, Mr. Siyao Jiang, Mr. Yiqi Liu, Dr. Xuan Zhang, Dr. Xiaonan Lu, Dr. Haifeng Lu, Dr. Sheng Zheng, Dr. Xiaohua Jiang, Mr. Fei Yang, and Mr. Ren Ren. Specially, I would like to thank Dr. Fan Xu, Mr. Zheyu Zhang, Dr. Jing Xue and Mr. Weimin Zhang for numerous brainstorming discussions we had together.

I would like to thank the staff members of the University of Tennessee. They are Mr. Robert B. Martin, Mr. William Rhodes, Ms. Judy Evans, Ms. Dana Bryson, Mr. Erin Wills, Mr. Adam Hardebeck, and Mr. Chris Anderson.

Finally, but most importantly I would like to express my heartiest thanks to my parents and my wife Shi Liu for their unconditional love. Special thanks to my wife Shi, she always gave me a warm hug whenever I met difficulties and felt frustrated. Without her support and encouragement, this work is never possible.

This dissertation made use of Engineering Research Center Shared Facilities supported by the Engineering Research Center Program of the National Science Foundation and the Department Of Energy under NSF Award Number EEC-1041877 and the CURENT Industry Partnership Program.

Abstract

In this dissertation, the benefits of the three-phase current source rectifier (CSR) in high power rectifier, data center power supply and dc fast charger for electric vehicles (EV) will be evaluated, and new techniques will be proposed to increase the power efficiency of CSRs.

A new topology, referred as Delta-type Current Source Rectifier (DCSR), is proposed and implemented to reduce the conduction loss by up to 20%. By connecting the three legs in a delta type on ac input side, the dc-link current in DCSR can be shared by two legs at the same time.

To increase the switching speed and power density, all-SiC power modules are built and implemented for CSRs. The switching waveforms in the commutation are measured and studied based on double pulse test.

Four different modulation schemes are compared for high efficiency CSR considering the switching characteristics of different device combinations. The most advantageous modulation scheme is then identified for each of the device combinations investigated.

A compensation method is proposed to reduce the input current distortion caused by overlap time and slow transition in CSRs. The proposed method first minimizes the overlap time and then compensates the charge gain/loss according to the sampled voltage and current. It is verified that the proposed method can reduce the input current distortion especially when the line-to-line voltage is close to zero.

The dc-link current will become discontinuous under light load in CSRs, when the traditional control algorithm may not work consistently well. To operate CSR in discontinuous current mode (DCM), the CSR is modeled in DCM and a new control algorithm with feed-forward compensation is proposed and verified through experiments.

A protection scheme with fast response time is proposed, analyzed and verified to protect SiC devices from overvoltage caused by current interruption in CSRs.

To deal with the harmonics and voltage sag in the input ac voltage, a new control algorithm is proposed. By adding ac current feedback control and proportional-resonant (PR) control, the proposed control algorithm can reduce the input current distortion and dc output voltage ripple under input voltage disturbance.

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1 Introduction

This chapter will introduce the application of the three-phase current source rectifier (CSR) in data center power supply, fast electric vehicle charger and high power rectifier. Then the motivation of the research is discussed. The organization of the dissertation is demonstrated afterwards.

1.1 Application Background

The consumption of the electricity in U.S. achieved nearly 3,856 billion kilowatt-hours (kWh) in 2011, which was more than 13 times greater than electricity use in 1950 [1]. As the concern increases about growing population and global warming caused by greenhouse gas, the countries such as U.S. starts to cut the usage of traditional fossil fuels and shift to renewable energy [2]. Power electronics becomes more important as an enabling technique to convert and control the flow of electrical energy [3]. As the cost of energy continuously increases, the efficiency of power conversion turns out to be the primary design goal in many applications [4]. This research focuses on three applications – high power rectifier (arc furnace, induction melting etc.), power supply for data center and dc fast charger for electric vehicle (EV).

1.1.1 High Power Rectifier

High power rectifiers with power semiconductors have over 50 years of development history [5][6]. They are widely applied in electrochemical industry such as electrowinning and refinery of copper and other nonferrous metals, as well as in application of dc arc furnace and plasma torch. In low-voltage (LV) and medium-voltage (MV) motor drives, they work as the front-end to establish the dc-link current [7][8]. These rectifiers are characterized by very large

load current (hundreds of kA) and comparatively low output voltage (less than several kV). The typical specification in different application is shown in Table 1-1 [5].

Table 1-1. Typical specification of high power rectifiers

Application	Output current (kA)	Output voltage (V)
Chemical electrolysis	5 – 150	40 – 1000
Aluminum potline	10 – 300	< 1300
DC arc furnace	50 – 130	600 – 1150
Graphitizing furnaces	20 – 120	50 – 250
Zinc/Lead electrolysis	5 – 100	100 – 1000
Copper refining	10 – 50	40 – 350
Traction substations	1 – 5	500 – 1500
LV motor drive	0 – 10	250 – 1000
MV motor drive	0 – 5	3400 – 6000

The dc arc furnace is a typical application for the high power rectifier. It was introduced into industry in 1984, about 30 years ago [9]. The electric arc is an electrical breakdown of a gas that produces an ongoing plasma discharge, resulting from a current through normally nonconductive media such as air [10]. The phenomenon was first described by Sir Humphry Davy when he transmitted current through two touching carbon rods and then pulled them a short distance apart [11]. The electric arc has very high temperature, capable of melting or vaporizing most materials. The structure of the dc arc furnace is shown in Fig. 1-1, where the two electrodes are connected with the output of the high power rectifier. The scrap is heated by the arc generated between two electrodes. The scrap can be charged through the charging door and the molten metal can be poured out through spout on the furnace.

Although developed about 70 years later than ac arc furnace, the dc arc furnace is the dominating type in scrap melting applications due to its simpler furnace structure, wider range of composition and lower cost [9][12]. Very large dc arc furnaces are currently in use in the steel

industry. In 2007, Tokyo Steel ordered the world's largest electric arc furnace from Danieli. It is a twin-cathode dc arc furnace with 175 MW operating power [13].

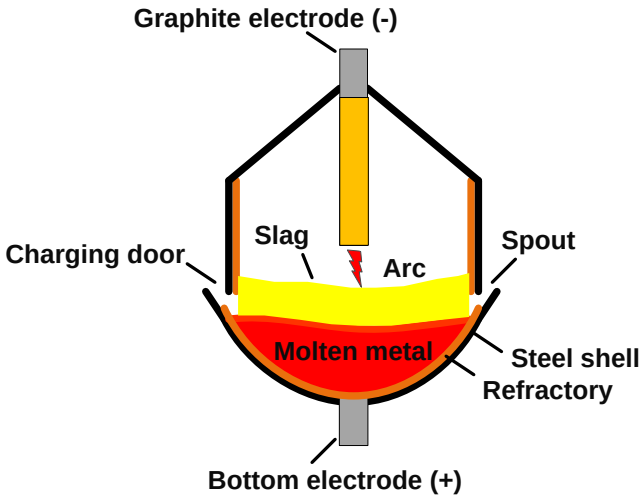


Fig. 1-1. Structure of dc arc furnace.

As semiconductor device technology develops in recent years, a lot of researchers are trying to find alternative solutions to the high power applications. Many restrictions and performance indices should be taken into consideration when different designs are compared [5]. On the utility side, the power factor and harmonic distortion should meet the industry standard such as IEEE standard 519 [14]. The power quality on the dc side is important to the process, including dc voltage/current operating range, ripple, regulation accuracy and regulation speed. Further decisive factors are system efficiency, reliability, cost and mechanical dimension.

The multi-pulse rectifiers are most widely used as high power rectifiers in industry products. A 12-pulse diode rectifier with transformer is shown in Fig. 1-2, including two diode bridges in parallel. The high voltage (HV) from the grid is stepped down to medium voltage (MV) through a HV/MV transformer. Then the 12-phase delta-delta-wye transformer is applied to realize phase

shift between the input voltages of the two rectifiers. With the multi-pulse rectifier, the input current harmonics can be significantly reduced. For 12-pulse rectifier, the 5^{th} and 7^{th} harmonics can be canceled in the input current on the primary side [15]. The diode rectifier is the simplest topology in the high power application. It does not offer any voltage adjustment capability. The output voltage can be changed with tap-changer of the transformer or saturable core reactor in the system [5]. On the primary side, there should be some static VAR compensator (SVC) or harmonic filter to compensate the reactive power and filter out the harmonic current. Because of its narrow output voltage range, the diode rectifier is not as popular as thyristor rectifier in Fig. 1-3.

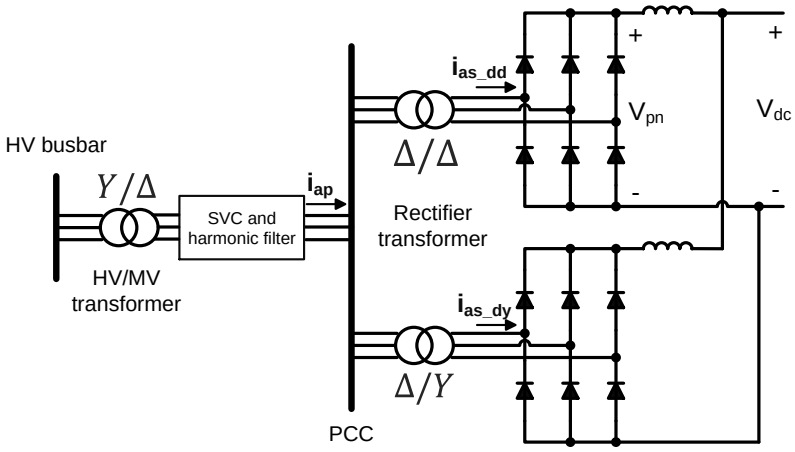


Fig. 1-2. 12-pulse diode rectifier.

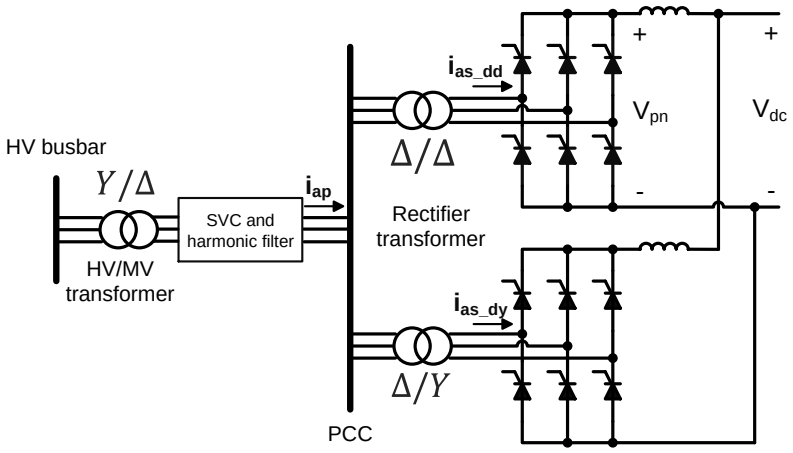


Fig. 1-3. 12-pulse thyristor rectifier.

The Silicon Controlled Rectifier (SCR) or thyristor rectifier has similar structure with diode rectifier. The diode is replaced with the thyristor so that the output voltage can be electronically controlled by changing the firing angle of the thyristor. Due to the simplicity, low cost, high efficiency and reliability, the thyristor rectifier is the most widely used configuration in high power rectifier application [5][6]. But the power factor is very low especially when the firing angle is large or the output voltage is low. So SVC is necessary in the thyristor rectifier, as shown in Fig. 1-3.

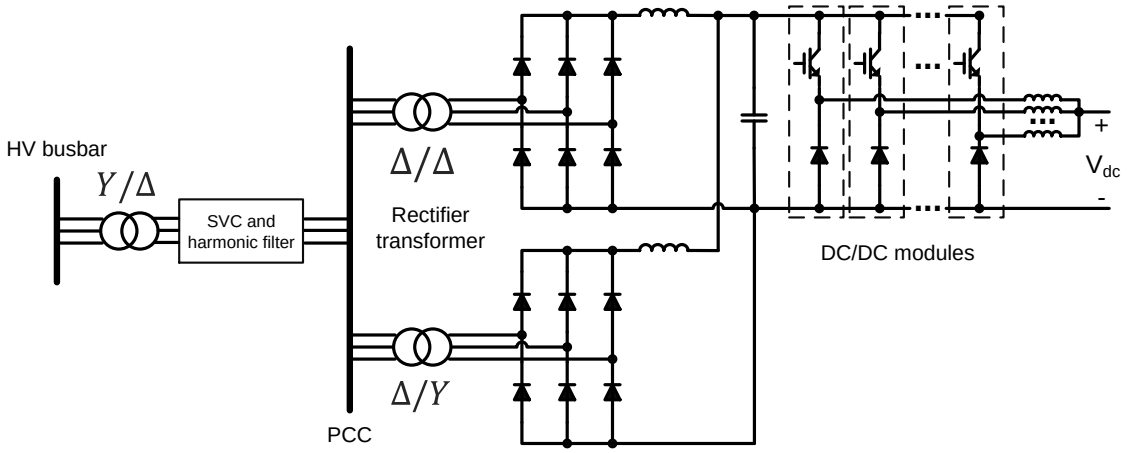


Fig. 1-4. Diode rectifier with dc-dc chopper.

The dc-dc chopper can be connected with the multi-pulse diode rectifier to construct a two-stage topology for high power application, as shown in Fig. 1-4 [5][6][7][8]. The output dc voltage can be regulated with the chopper stage. Multiple dc-dc modules can be paralleled to share the dc output current. Their PWM carriers can be interleaved to reduce the output dc current ripple. Because of the higher switching frequency and crossover frequency of the controller, the diode rectifier with dc-dc chopper has fast dynamic response than thyristor rectifier [6][16]. It can achieve close or even higher efficiency than the thyristor rectifier [6][17]. There have been some commercial products with this topology [6].

For the topologies with multi-pulse rectifier, the SVC and harmonic filter only improve the power factor and total harmonic distortion (THD) on the primary side. The current on the secondary side of the transformer still contains much harmonics, and large reactive power exists in the transformer. Other topologies with multi-pulse rectifier have been proposed in previous research, including the phase controlled sequential rectifier [18] and filter-less rectifier [19][20].

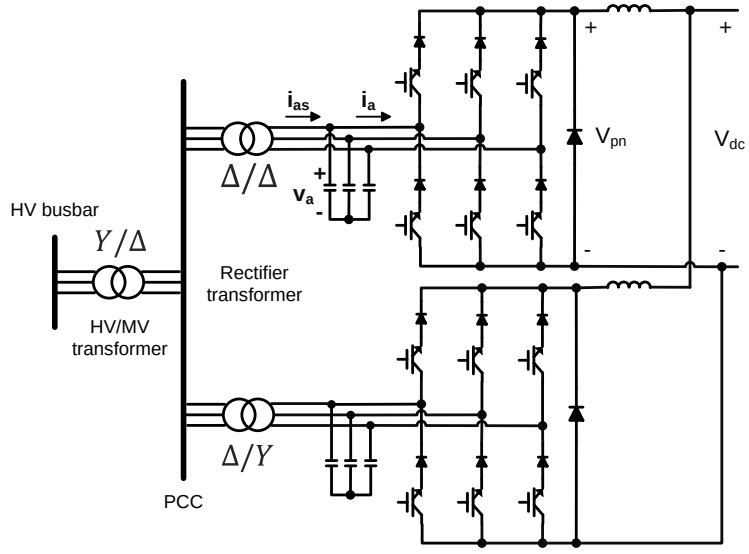


Fig. 1-5. Traditional current source rectifier for high power application.

While not yet available for practical application, the three-phase current source rectifier (CSR) is believed to be a promising topology of high power rectifier [5][6][21][22]. As an active rectifier, it can regulate the output current well while achieving nearly unity power factor on the input side. The traditional current source rectifier is shown in Fig. 1-5, where two rectifier units are paralleled. The filter capacitors are used on the input side to reduce the switching-frequency harmonics. With pulse width modulation (PWM) at high switching frequency, the filter size is much reduced compared with multi-pulse rectifiers. There is no need of SVC in this topology since the reactive power can be compensated through proper rectifier control. The freewheeling diode is usually added on the dc bus to reduce the conduction loss.

According to the specification of the high power rectifier, the semiconductor devices should have large current rating while low voltage rating in most applications. In recent years, the high power insulated-gate bipolar transistor (IGBT) has been developed dramatically, which enabling

the application of dc-dc chopper and current source rectifiers [6][7][8][21][22]. 1700 V/3600 A IGBT modules are available on the market [23][24]. With turn-off capability and high switching speed, the switching frequency of IGBT can be increased to higher than 1 kHz to reduce the filter size [6][21[22]. The gate turn-off thyristors (GTO) and integrated gate-commutated thyristors (IGCT) are applied as well in the high power rectifier [6][25]. They have higher power rating than IGBT, but their switching speed is lower than IGBT.

Table 1-2. Comparison of topologies in high power application

Topology	Diode rectifier	Thyristor rectifier	Diode rectifier with chopper	Traditional CSR
Transformer			✓	✓✓
Converter efficiency	✓✓	✓✓	✓	
Filter/SVC			✓	✓✓
Control complexity	✓✓	✓		
Regulation speed		✓	✓✓	✓✓
Regulation accuracy		✓	✓✓	✓✓
Device cost	✓✓	✓		
System reliability	✓	✓✓		

✓✓: More advantageous **✓: Advantageous**

The characteristics of the topologies in the high power application are summarized in Table 1-2 [5][6][20]. The loss and cost of the semiconductor devices are still much higher in CSRs than those in the thyristor rectifiers. But with power factor control and high switching frequency, the CSRs can save much loss and cost on transformer, filter and SVC.

1.1.2 Power Supply for Data Center

As the rapid development of information technology (IT), data centers with up to megawatt power level are built worldwide to process large amount of data. The power consumption of data center doubled from 2000 to 2005. In 2010, it accounted for 1.7% to 2.2% of the total electricity use in United States [26]. In a typical data center, less than half of the input power can be delivered to the compute load (microprocessors, memory and disk drives). The rest of power is dissipated in power conversion, distribution and cooling, resulting in high utility bill [27]. It is expected that the life time energy cost of a server will be higher than the initial investment on the server hardware [28]. So power efficiency is critical for the power supply system of the data center.

The traditional power architecture of the data center in U.S. is shown in Fig. 1-6, which is based on ac distribution [27]. It is burdened with many conversion stages, leading to low efficiency of the system. The double-conversion uninterruptible power supply (UPS) in the system converts 480 Vac to dc voltage to charge the energy storage component. Then the dc voltage is inverted back to 480 Vac and stepped down to 208 Vac with a transformer in power distribution unit (PDU), since the traditional power supply units (PSU) in U.S. can only take 90 – 264 Vac input voltage. In PSU, 208 Vac is converted to 12 Vdc through a two-stage conversion. After that, the voltage regulators (VR) steps down the voltage further to supply the electric loads. The efficiency of the traditional power supply system is around 67% [29], with typical efficiency of each stage listed in Fig. 1-6.

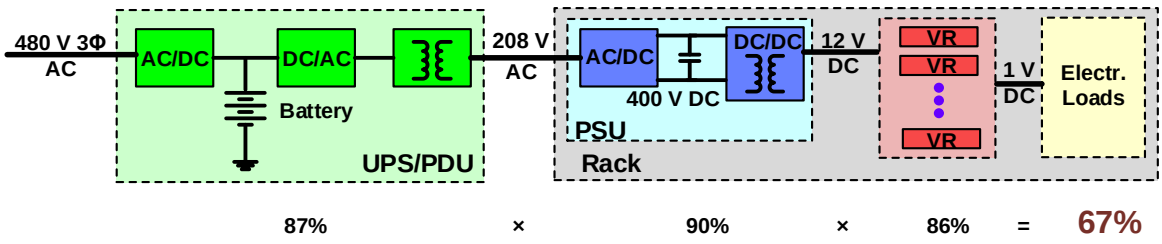


Fig. 1-6. Conventional ac-distribution power architecture of data center in United States.

To reduce the conversion stages and distribution loss in the conventional power architecture, the high voltage dc (HVDC) distribution architecture has been proposed by industry companies (IBM, Intel, Delta, NTT Facilities, Vicor, et al.) in recent years [27][28][29][30][31][32][33], as shown in Fig. 1-7. Compared with the traditional one in Fig. 1-6, the new architecture has reduced number of conversion stages. 400 Vdc after the dc UPS is directly feeding the rack, largely reducing the distribution loss and conversion loss. The distribution voltage level can be flexible between 300 V and 400 V [34]. PSU in this architecture steps down 400 Vdc to 12 Vdc. Since 2010, IBM, Syracuse University and New York State have cooperated to build a 780 kW new data center with 380 Vdc HVDC power architecture [35]. It has operated successfully for over three years and saved more than 50% energy cost than the traditional data center. More and more dc powered data centers arise in recent years worldwide [34].

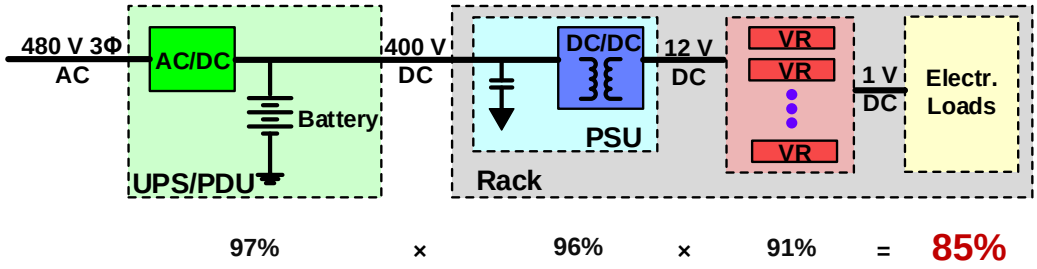


Fig. 1-7. HVDC power architecture of data center.

Addressing the potential market in HVDC data center, many companies have already released state-of-art produces for the new architecture. For 480 Vac to 400 Vdc stage, 97% peak efficiency at 15 kW is reached in EMERSON NetSure™ 802 DC Power System [36]. Delta DC UPS has 97.1% efficiency at full load (20 kW) and 97.8% efficiency at 35% load (7 kW) [31]. For PSU stages, Vicor bus converter module (BCM) has 96% full-load (325W) efficiency [33]. For VR stage, infineon products have 91% efficiency under 100 W output power. With the state-of-art products for each stage, the HVDC power architecture can reach 85% system efficiency, which is much higher than the efficiency of the traditional architecture.

Table 1-3. Typical specification of front-end rectifier in data center power supply

Parameter	**Value**
Input voltage	380 – 480 Vac, 50 – 60Hz
Output voltage	300 – 400 Vdc
Output power	15 – 20 kW each module 40 – 280 kW each cabinet
Input power factor	> 0.99
Input current THD	< 5%

Based on the requirements of the industry, the typical specification for the front-end stage is shown in Table 1-3. According to the specification, the output dc voltage is usually lower than the peak value of the input line-to-line voltage, so the front-end rectifier should have a step-down capability. Moreover, the input power factor should be close to unity, and the total harmonic distortion (THD) of the input current should be limited to less than 5%. Addressing all these requirements, the active rectifiers are preferred in this application, with controllability on both ac and dc side [38].

The phase-modular rectifiers are formed with two or three single-phase rectifier modules. They are attractive to the industry because the knowledge on single-phase system can be exploited to the three-phase system with low effort. The voltage stress in phase-modular rectifiers is lower than that in the direct three-phase rectifier. Another benefit of the phase-modular rectifier is the modularized design for large power supply system.

The topology of phase-modular boost rectifier is shown in Fig. 1-8, which is formed with three single-phase boost rectifiers [39]. Normal PiN diodes can be used in the diode bridge to reduce the conduction loss. The voltage stress on the switch is no more than 400 Vdc, so Si CoolMOS^{TM} [24] can be used as the switch. To reduce the reverse recovery loss, SiC Schottky diodes or Si fast-recovery diodes can be used as Da, Db and Dc. The outputs of three modules can not be connected together directly due to the interaction between different phases [40]. To feed the same load, an isolated DC/DC converter stage is necessary after the front-end rectifier for each module. To share the load equally in three phases, the power balance control is required between three modules [38]. Otherwise, there is large neutral current in this system.

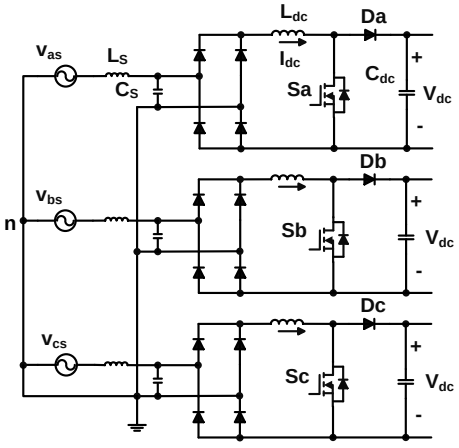


Fig. 1-8. Phase-modular boost rectifier for data center power supply.

Another phase-modular topology applied in the industry products is the three-phase buck-boost rectifier, as shown in Fig. 1-9 [30][31][41]. To reduce the cost and increase the power density, only two phase modules are applied in the topology [42]. With the neutral line, three phase currents can be controlled independently. The input currents of phase a and phase c are controlled by the upper module and the lower one respectively. Phase b is connected to both modules and its current can be regulated with the idle devices in both modules. Each phase module is a single-phase three-level buck-boost rectifier, where the voltage stress of devices can be reduced compared with two-level rectifiers. The input phase voltage is first stepped down in the module and then boosted up to around 400 V. In this way, the rectifier has wide input and output voltage ranges. The outputs of two modules are connected together to share the load and the power is well balanced between three phases. However, the conduction loss is high in this topology with many devices in series. The control is more complex than traditional single-phase rectifier.

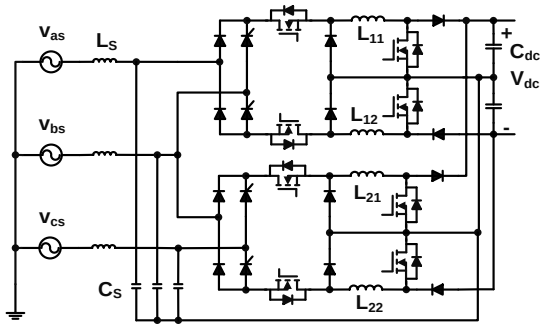


Fig. 1-9. Phase-modular buck-boost rectifier for data center power supply.

The phase-modular rectifiers are actually operated in a single-phase internally. So there is still power pulsation at twice the fundamental frequency in these topologies. Large electrolytic

capacitors are required to filter the low-frequency current at the output side, limiting the power density of the rectifier.

The direct three-phase rectifiers, including voltage source, current source and Z-source rectifiers, regulate all three-phase currents together with one controller and PWM modulator. The voltage source rectifier, also referred to as boost rectifier, is widely applied in power electronics field. It can boost the input ac voltage to higher dc voltage, which should be larger than the input line-to-line peak voltage. For the data center power supply, another dc-dc stage is needed if the boost rectifier is applied, leading to more loss, cost and control complexity. Z-source converters are proposed in [43], by introducing an impedance network (two inductors and two capacitors) to traditional voltage/current source converters. In this way, the rectifier can realize both voltage step-up and step-down functions. Moreover, it allows the shoot through state in the phase leg, which increases the noise immunity. But it has some drawbacks compared with traditional voltage/current source rectifiers. One of them is the higher switching loss of semiconductor due to introduced shoot-through state. The impedance network brings more loss, volume and control complexity to the rectifier.

Alternatively, the three-phase current source rectifier, also referred to as buck rectifier, is very suitable for application in data center power supplies for its step-down conversion function, smaller filter size and potential for high efficiency [44][45]. As shown in Fig. 1-10, the input ac voltage can be stepped down to dc voltage less than $\sqrt{3}/2$ of the line-to-line peak voltage. So it can accommodate to different input voltage ratings in Table 1-3 and output 400 Vdc for power distribution. The main drawback of the topology is the large device conduction loss due to series connection of a diode and a switch. But the conduction loss can be largely reduced with newly

developed semiconductor devices like Reverse Blocking IGBT (RB-IGBT) and SiC MOSFET [45].

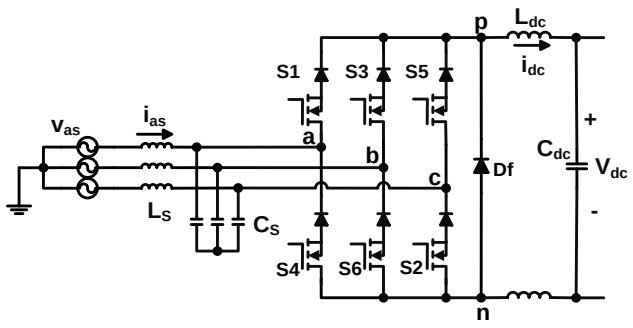


Fig. 1-10. Three-phase buck rectifier for data center power supply.

The characteristics of the topologies as front-end rectifiers in data center power supplies are summarized in Table 1-4. The three-phase CSR has more advantages over the phase-modular rectifiers in the industry.

Table 1-4. Comparison of topologies of front-end rectifier in data center power supply

Topology	Phase-modular rectifier		Three-phase CSR
	Boost	Buck-boost	
Three-phase load balance		✓	✓
Voltage stress	✓	✓	
Output/input voltage range		✓	✓
Control complexity	✓		✓
Device loss	✓		✓
DC capacitor size			✓

✓**: Advantageous**

1.1.3 Dc Fast Charger for Electric Vehicle

Concerning about the global climate change and rapidly increased consumption of fossil fuel storage, countries in the world are driving a movement back to the electric vehicles (EV), which was first invented in 1830s [46][47][48]. Of all the oil consumed in U.S., 70% of them is consumed in the transportation. It is predicted that by 2050 there may be as many as 1.5 billion cars on the load, almost doubled compared to 750 million in 2010 [49]. The federal regulations in U.S. have set the fuel-economy goal for the light-duty vehicle to improve from a combined average of 27.5 miles per gallon (mpg) in 2010 to 54.5 mpg by 2025 [46]. To meet such a challenging requirement in the near future, the automakers have invested much money to retool, expand or build new facilities to make EVs. Although the market for electric vehicle is still in its infancy, it is expected to account for 2% of U.S. car sales by 2017 [50]. In 2012, the global EV sales are doubled compared with that in 2011 [48].

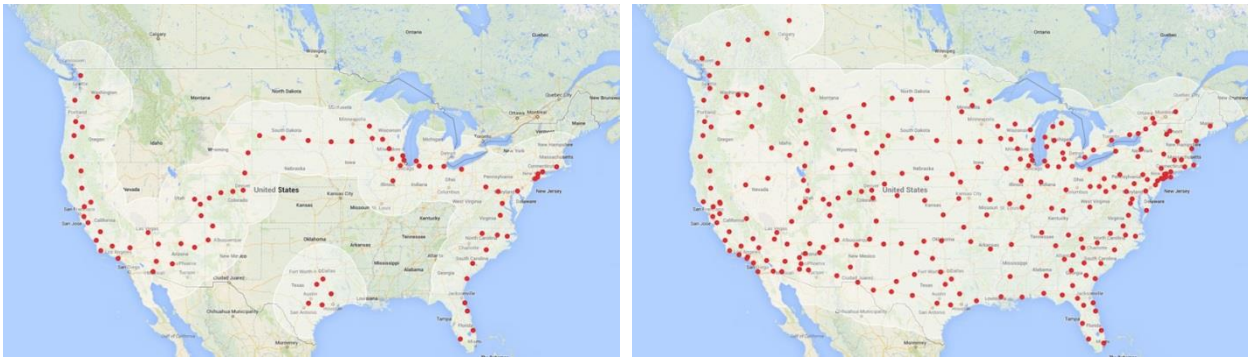
The charger infrastructure is crucial to the growth of EVs. Because the battery capacity is still not enough to support long distance (>200 miles) travel, EVs need to get charged in the charge station, which is similar to the gas station. Three levels can be divided for current EV chargers, as shown in Table 1-5 [51][52][53]. The level-1 and level-2 chargers usually have single-phase structure with low output power, resulting in slow charging speed. They are primary solutions for charging at home or in some public places like supermarkets. Because of their simple structure and low weight, they are usually integrated in the EVs as on-board chargers.

Level-3 charger, also referred to as dc fast charger, usually has three-phase 480 Vac input voltage and much larger power rating than level-1 and level-2 chargers. They are installed in large public charger station, analogous to a filling station. The battery of EVs can be fully

charger in less than 1 hour with dc fast chargers. Because of large power and weight, they are usually off-board chargers.

Table 1-5. Power levels of EV chargers

Power level	Charger location	Typical use	Expected power level	Typical miles per hour of charge
Level 1 120 Vac (US)	On-board 1-phase	Home or office	1.4 kW, 1.9 kW	2 – 5
Level 2 240 Vac (US)	On-board 1- or 3-phase	Private or public outlets	4 kW, 8 kW, 19.2 kW	10 – 20
Level 3 (Dc fast charger) 480 Vac (US)	Off-board 3-phase	Commercial, filling station	50 kW, 100 kW	60 - 80



(a) (b)

Fig. 1-11. Supercharger stations of Tesla Motors in U.S.: (a) Today; (b) End of 2015 [57].

Considering the huge potential demand of dc fast chargers, many companies have released their commercial produces in recent years [54][55][56]. Fuji has introduced its 25 – 50 kW dc fast charger station with more than 90% efficiency [54]. Delta EV dc quick charger has 50 kW maximum output power and 94% efficiency [55]. ABB released its 50 kW charge station with 92%

efficiency [56]. As shown in Fig. 1-11(a), Tesla Motors has built 81 supercharger stations nationwide, enabling their EVs to travel between west and east coasts uninterruptedly [57]. Their next-generation 120 kW supercharger can cut the charging time by 33%. The expected distribution of the Tesla supercharger stations in 2015 is shown in Fig. 1-11 (b), covering 98% of US population and part of Canada.

Most EV chargers are grid-to-vehicle (G2V) ones, which means they always consume power from the grid. Actually, one potential future technology allows vehicles to feed electricity back to the grid – vehicle-to-grid (V2G) technique. This technique can balance the demand of electricity in the grid [47]. The peak hours of electricity consumption occur in the day time when most EVs are usually idle. During late night, EVs can be charged when the electricity burden of the grid is light. With V2G technique, the EVs can send some extra energy back to the grid to meet large energy demand in the daytime.

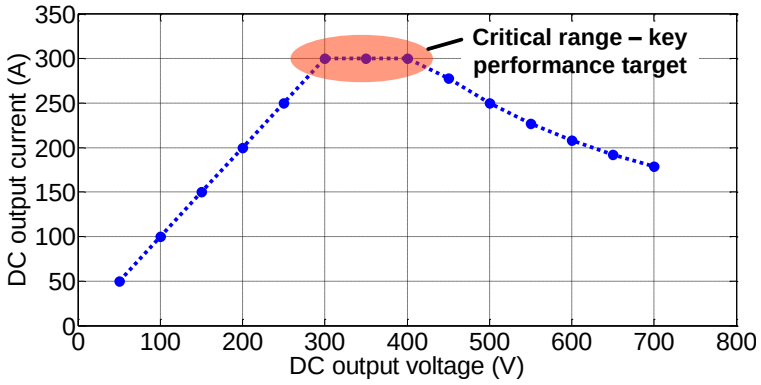


Fig. 1-12. Output current profile for a 125 kW dc fast charger.

The ideal battery charger must be efficient and reliable, with high power density, low cost, small input current THD and nearly unity power factor [51]. For dc fast charger, there are some

special requirements [58]. It should have wide output dc voltage range to accommodate different design voltages of the battery packs in different types of EVs. The output current profile for a 125 kW dc fast charger is shown in Fig. 1-12, where the output voltage varies between 50 V and 700 V [58]. Particularly, 250 V to 450 V is a critical voltage range, where the dc charger should be optimized on its performance [58][59]. Moreover, the output current ripple should be limited to less than 1% and the output voltage should be regulated to less than 5% variation [58].

Last but not least, safety is important in the charger design. The frame of EV should be grounded before the battery is being charged [51]. There is still a debate on battery pack grounding. Actually it is costly and nearly impossible to realize a completely floating battery pack in EVs, considering the distributed capacitor and electrostatic discharge (ESD). It is recommended that the battery pack is grounded with the EV frame with grounding fault interrupter [60]. The dc fast chargers in a charging station should have galvanic isolation from the distribution network, so that they will not interact with each other [58].

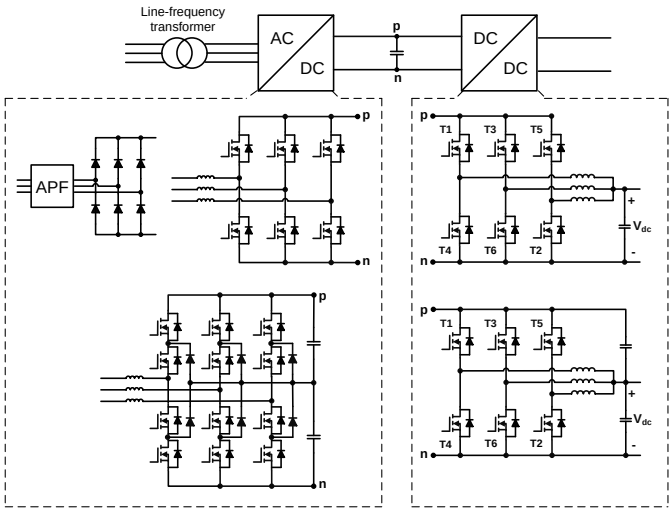


Fig. 1-13. Dc fast charger with line-frequency transformer.

There are mainly two ways to realize the isolation. The line-frequency transformer can be added before ac-dc stage, as shown in Fig. 1-13. Non-isolated topologies are applied in the ac-dc and dc-dc converters in this architecture. The other way is to apply the isolated dc-dc stage, as shown in Fig. 1-14. The high-frequency transformer in the dc-dc converter has much smaller size than the line-frequency transformer. In a comparison between these two architectures, the one with line-frequency transformer has higher efficiency due to lower loss in its dc-dc stage [58].

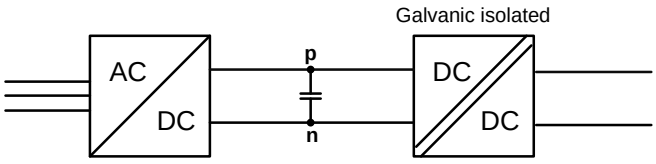


Fig. 1-14. Dc fast charger with isolated dc-dc stage.

The two-stage architecture is predominant in dc fast EV chargers. For the front-end ac-dc stage, the diode bridge can be applied with an active power filter (APF) to reduce the input current distortion [61][62], as shown in Fig. 1-13. The two-level voltage source rectifier (VSR) is the most popular front-end topology in fast EV charger [58][63][64] for its simplicity, as shown in Fig. 1-13. The three-level neutral-point-clamped rectifier (NPC) can also be applied as the front end [51][62][65], but it is not an economic way since the output voltage is not high in this application.

In the dc-dc stage, multi-phase buck converters are popular for their simplicity and high efficiency, as shown in Fig. 1-13. With interleaved PWM technique, the output current and voltage ripples are largely reduced, leading to smaller output filter size and loss [58][61][62]. The LLC resonant converter can be applied as galvanic-isolated dc-dc stage [63]. The phase-shift full-bridge converter is applied to provide isolation in dc-dc stage in [64].

Different topologies in ac-dc and dc-dc stages can be combined in the dc fast charger. In ABB product, the VSR is connected with multi-phase buck converters, as shown in Fig. 1-15.

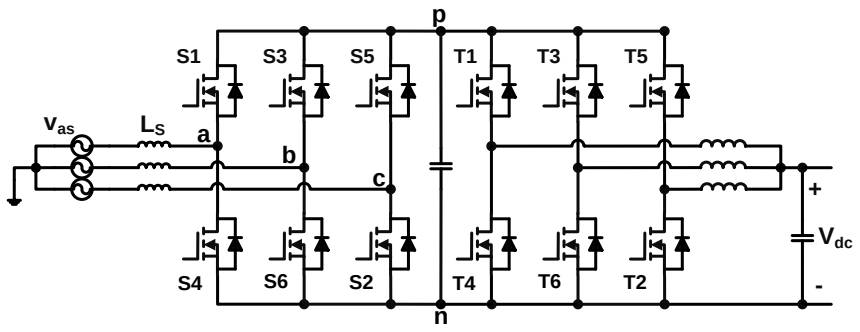


Fig. 1-15. Two-stage voltage source converter in ABB charger.

In the two-stage architecture, the input voltage is boosted to a high dc voltage and then stepped down to charge the battery. With three-phase CSR, the step-down function can be realized in a single stage, providing the opportunity to increase the efficiency [59][62].

1.2 Motivation

Based on the previous analysis, the three-phase CSRs are advantageous for application in high power rectifier, data center power supply and fast dc charger for EVs. They have great potential to increase the power density and efficiency in these applications. However, there are some challenging hurdles in the application of CSRs, which can not be overcome based on present techniques.

In [66], the back-to-back current source converter (BTB-CSC) was compared with the back-to-back voltage source converter (BTB-VSC), three-level boost rectifier (Vienna type) plus voltage source inverter (NTR-VSI) and 12-switch matrix converter on their weight in motor drive application. The comparison result of converter weight is shown in Fig. 1-16, where BTB-

CSC has the largest weight due to its heavy heatsink and dc inductor. Similar comparison results were got in [67][68].

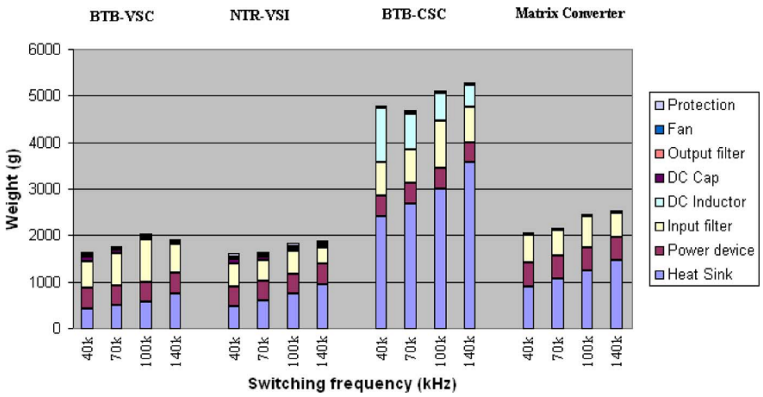


Fig. 1-16. Weight comparison of four topologies for ac-ac motor drive [66].

The switches in three-phase current source converters need to have reverse blocking capability to handle the ac voltage on them. Usually a diode is connected in series with an active device (IGBT etc.) to form one switch in CSRs. In this way, the dc-link current will flow through as many as four semiconductor devices in series, leading to much conduction loss. The conduction loss in CSRs usually accounts for over 50% total converter loss [45][67], requiring large heatsink size to cool devices.

The other challenge is the bulky dc inductor as energy storage component in CSRs, which contributed 20% loss [67] and over 40% weight [45]. The dc inductor needs to have large inductance to limit the current ripple. At the same time, it has high current rating.

The objectives of the research are to evaluate the potential benefits of the three-phase current source rectifier in high power rectifier, data center power supply and fast dc charger for EVs, and develop techniques to increase the power efficiency of the current source rectifier.

1.3 Dissertation Organization

The chapters in this dissertation are organized as follows.

- The state-of-art research is reviewed in Chapter 2 and the research challenges are given.
- To reduce the device conduction loss, a new topology of current source rectifier is proposed and implemented, which has delta connection on its input side and the dc-link current can be shared by multiple devices at the same time. Its principle of operation, suitable modulation schemes and design method are analyzed and discussed in Chapter 3.
- To evaluate the potential benefit of CSRs, they are compared with traditional topologies on efficiency and power density in high power rectifier (arc furnace, etc.), data center power supply and dc fast charger for EVs. The evaluation methods and comparison results are demonstrated in Chapter 4.
- To fully utilize the high-speed characteristics of SiC MOSFETs, all-SiC power modules are built and tested, including the phase-leg module and the converter module. The switching speed of SiC MOSFETs is pushed high with reduced parasitic inductance. Based on the test in the converter module, the commutation in the new topology is compared with the one in traditional topology. The design method and test result are given in Chapter 5.
- To reduce the switching loss of RB-IGBT in current source rectifiers, four different modulation schemes are compared. The RB-IGBT is compared with the standard IGBT on switching performance. The switching loss of the CSR is modeled considering different commutations. The analysis and comparison result are given in Chapter 6.
- To reduce the input current distortion caused by overlap time and slow transition, a compensation method is proposed. The charge loss/gain is modeled and compensated based

on the commutation model. The overlap time is minimized to accelerate the transition speed. The analysis and result are given in Chapter 7.

- To reduce the size and loss of the dc inductor, the impact of dc-link current ripple on device loss and filter size is evaluated. To operate the CSR under large dc-link current ripple, a control algorithm for discontinuous current mode (DCM) is proposed. The analysis and result are given in Chapter 8.
- To protect SiC devices from overvoltage caused by current interruption, a protection scheme is proposed and implemented. The response time of the protection is very short and the added protection circuit will not impact the switching speed in normal operation. The analysis and result are given in Chapter 9.
- To deal with the harmonics and voltage sag in the input ac voltage, a new control algorithm is proposed in Chapter 10. By adding ac current feedback control and proportional-resonant (PR) control, the proposed control algorithm can reduce the input current distortion and dc output voltage ripple under input voltage disturbance.
- The conclusions and future work will be given in Chapter 11.

2 Literature Review

2.1 Semiconductor Devices

The semiconductor technique is the fundamental force that drives the progress of power electronics industry. To reduce the conduction loss in the current source converters and matrix converters, the Reverse Blocking IGBT (RB-IGBT) has been developed in recent years.

The cross section of RB-IGBT is shown in Fig. 2-1. [69][70]. The structure is similar to the conventional Non-Punch-Through (NPT) IGBT, except that the p^+ layer in the collector is folded up by isolation diffusion from bottom to the top at the chip edge [69]. This enables the p^+-n^- junction to block the reverse voltage on the device, so that the RB-IGBT has symmetric voltage blocking capability on both collector-emitter and emitter-collector directions. The equivalent circuit of RB-IGBT can be seen as a PiN diode connecting in series with MOSFET, as shown in Fig. 2-1. [71]. There are commercial products of RB-IGBTs in the industry. IXYS has released its 1200 V RB-IGBT with 35 A maximum current rating [72]. Fuji has released 600 V RB-IGBTs with 300 A maximum current rating [73].

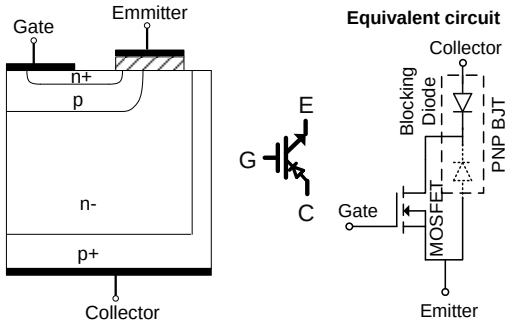


Fig. 2-1. Structure of RB-IGBT and its equivalent circuit.

Without additional external diode in series to block the reverse voltage, RB-IGBT can significantly reduce the conduction loss in current source converters. It has been successfully applied in matrix converters and current source converters. In [74], a 9 kW current source rectifier with 94% efficiency was built with 600 V/100 A RB-IGBTs. In [75], a 55 kW current source inverter was built with RB-IGBT and applied in Hybrid Electric Vehicle (HEV). In [75], a 15 kW current-fed quasi-Z-source inverter with 98% efficiency was built with RB-IGBT. The RB-IGBTs are also applied in matrix converters to save the conduction loss [77][78].

However, the switching speed of RB-IGBTs is much lower than that of standard IGBTs [70][71][77][78][79]. The reverse recovery current is large when RB-IGBT is reversely turned off [70]. Due to the large width of the lightly doped drift region, RB-IGBT has large resistance before the conduction modulation is established, causing voltage overshoot in the turn-on process [79]. To accelerate its switching speed, a special gate driver was designed for RB-IGBT in [71]. The modulation scheme should be carefully designed to avoid the transition with high switching loss [78][79].

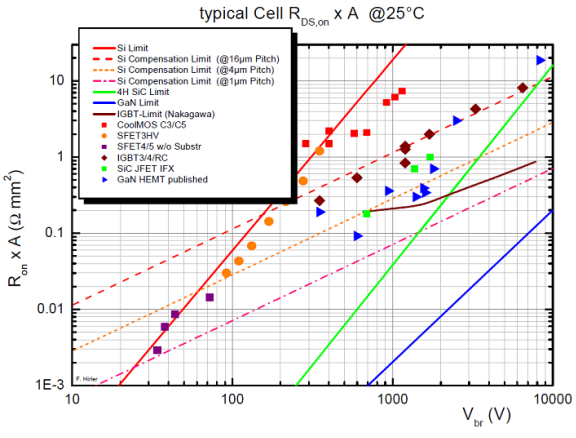


Fig. 2-2. Comparison of on resistance in different semiconductor devices [37].

The Wide-Band-Gap (WBG) devices, mainly including SiC and GaN devices, are considered to be the next-generation semiconductor devices for its high operating temperature, high blocking voltage, low on-resistance and fast switching speed [80][81]. The on resistances of different semiconductor devices are compared in Fig. 2-2 [37], where the SiC and GaN devices have much lower on resistance than Si IGBTs under high breakdown voltage.

Commercial SiC Schottky diodes have been released in the market for a long time. They have no reverse recovery current and are widely applied in power electronics application. CREE has released the first commercial SiC MOSFET in 2011 and kept improving its performance [82]. The latest discrete SiC MOSFET of CREE has 1200 V voltage rating, 60 A current rating and 25 mΩ on resistance. Infineon is supplying commercial SiC JFETs with 1200 V/ 35A rating [37].

In previous research, SiC devices have been applied in current source converters to reduce the device loss. Most of SiC JFETs are normally-on devices, which is suitable for application in current source converters. Because under fault conditions, SiC JFETs can be kept on to freewheel the dc-link current. In [83], a 2 kW, 150 kHz current source rectifier was built using SiC JFET and 91.4% efficiency was achieved. In [84], a 2 kW, 100 kHz current source inverter was built using SiC JFET and Schottky diode and 96.5% efficiency was achieved. In [85], a 3 kW, 200 kHz back-to-back (BTB) current source converter was built using SiC JFET and Schottky diode and achieved compact design with 92% efficiency. The SiC MOSFETs were paralleled in a 7.5 kW current source rectifier to realize 98.54% full-load efficiency [86].

The parasitics in the package and circuit are the main factor that limits the switching speed of fast SiC devices [87][88]. To minimize the parasitics, the SiC devices are suggested to be packaged in a compact power module. In [88], a SiC power module with only 600 pH loop inductance was constructed for one phase leg in the voltage source converters. Mitsubishi has

built 1200 V/1200 A all-SiC power module for high power application [89]. Since the commutation in the current source converter is much different from the well-understood voltage source converter, special attention should be paid when designing the power module for current source converters.

Another promising device is the lateral GaN power device. It is easy to obtain a bi-directional switch using the GaN lateral HEMTs [161]. Panasonic has developed a 650 V 3.1 $m\Omega cm^2$ GaN Gate Injection Transistor (GIT) [162][163] and applied in matrix converter [164]. It is possible to apply this 4-quadrant switch in CSR to reduce both the conduction loss and the switching loss in the future.

2.2 Topologies

In previous research, alternative topologies have been proposed for the current source rectifier. The three-switch current source rectifier is shown in Fig. 2-3, where only three switches are applied [90]. Compared with the traditional topology, the device cost can be reduced. However, the conduction loss will increase because the dc-link current flows through six devices in series.

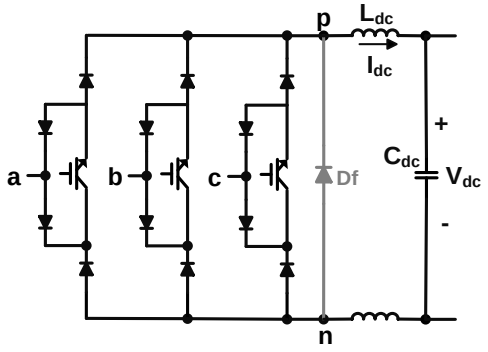


Fig. 2-3. Three-switch current source rectifier.

A four-pole current source rectifier was proposed in [91] to control the dc-link voltage and shape the converter input current into the sinusoidal wave. In this topology, another phase leg is added between positive and negative dc buses in the traditional topology and its center is connected with the neutral line. In this way, four voltage levels can be utilized to regulate the output voltage and input current. The output current ripple can be reduced [92].

The current-fed Z-source rectifier topology was proposed to realize buck-boost function [93]. An impedance network was added on the dc link of the traditional topology, including two capacitors and two inductors. By introducing the open zero state in the space vector PWM, the current-fed Z-source rectifier topology can realize boost function as well.

A three-phase buck-type third harmonic current injection rectifier, referred to as SWISS Rectifier, was proposed in 2012 [59], as shown in Fig. 2-4. In this topology, T_+ and T_- are switching under high switching frequency. Three four-quadrant switches S_{y1}, S_{y2} and S_{y3} are gated at twice the mains frequency to inject third harmonic current. T_+ and D_{F+} form a dc-dc buck converter, so does T- and D_{F-}. Since the dc-link current flows through at most five devices (D_{N+}, T_+, D_{F-} and S_{y2}) in series, the conduction loss in SWISS Rectifier is actually larger than traditional CSR.

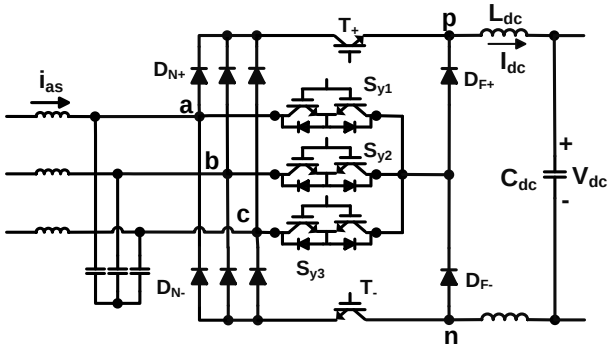


Fig. 2-4. SWISS Rectifier.

In previous research, there is no topology proposed for current source rectifier to effectively reduce the conduction loss.

2.3 Modulation Scheme

In previous research, most of the research focuses on the commutation in a phase leg of voltage source rectifier, where an IGBT is commutating with a diode under positive collector-emitter voltage. The commutations in current source rectifier are different from those in boost rectifier. The passive turn-on phenomenon of the IGBT has been shown when it is turned on under zero voltage in current source rectifier [125] and matrix converter [126]. Actually, the two devices connected in series will exhibit worse switching characteristics than a single device due to the superposition of the non-ideal semiconductor characteristics, especially when both of them are minority carrier devices. This phenomenon has not been studied in the previous research. The switching energy in current source rectifier would be under estimated if this phenomenon is not considered.

A modulation scheme with minimum switching loss was proposed in [94] and [95] for the three-phase current source rectifier. The semiconductor switching losses were derived analytically in [96] and [97]. In [94]–[96], the freewheeling diode Df was not considered in the analysis. When the freewheeling diode Df is added, the commutation in a current source rectifier becomes more complex. It involves two types of commutations, the one between two switches (switch-switch commutation) and the one between a switch and the freewheeling diode (switch-diode commutation). The switching energy in the switch-switch commutation is usually higher than the one in the switch-diode commutation, considering the passive turn-on loss of IGBT and the superposition of the non-ideal semiconductor characteristics. The difference on switching energy between these two types of commutations was neglected in the previous research [97].

Accordingly, the subtleties of the additional commutations were not fully analyzed in the loss calculation.

Moreover, in current source rectifier, the parasitic capacitance of the non-switching devices will affect the switching performance of the commutating devices, even though they are kept off during the transition [44][127]. The impact of the non-switching devices will be considered in the modeling of the switching loss in this dissertation.

2.4 Control Algorithm

2.4.1 Control in Discontinuous Current Mode

The dc-link inductor is the energy storage component in the buck rectifier. It usually has large volume because of high inductance and dc-link current. In order to increase the power density, the dc-link inductance needs to be carefully chosen for normal operation. Typically, it is designed to limit the current ripple within 15 % to 20 % of the dc current at full load [100][101].

Under light load condition the dc-link current ripple is larger than the dc current, in which case the buck rectifier works under discontinuous current mode (DCM). Higher switching frequency and dc-link inductance can reduce but not eliminate the DCM operating range. The converter dynamic behavior changes significantly in DCM, which renders control algorithms developed for continuous current mode (CCM) not usable [102][103]. For instance, the control in dq coordinates assumes a constant dc-link current [99], which induces error in large ripple applications. The gain of the converter dynamic also changes in DCM, which may cause instability for the input current control [104]. Additionally, the sampling of the dc-link current is a significant challenge in DCM. This problem also exists in the three-phase current-source

inverter and back-to-back current-source converter when the dc-link voltage is fixed under light load operating conditions.

DCM operation has been extensively modeled and analyzed in the boost rectifier and dc-dc converters [102][105]-[108]. In [103], a feed-forward control scheme was proposed for the three-phase VIENNA rectifier in order to compensate the current distortion on the ac inductor under DCM. Regarding control schemes for the latter, [83][109][129] proposed charge control as a cycle-by-cycle control technique for the buck rectifier. In [110], the amplitude of the carrier signal was adjusted according to the sensed dc-link current to compensate the duty cycle error caused by large ripple. Both control methods are suitable for buck rectifier with large dc-link current ripple. But they are all analog control methods, which are difficult to realize in digital controllers.

2.4.2 Compensation of Overlap Time

Overlap time is added in the gate signals of the buck rectifier to prevent dc current interruption [44][45][111]. The overlap time will cause error in the current control and increase the low-order harmonics in the input current [112]. The distortion caused by the overlap time is shown to be proportional to its duration and the carrier frequency [113]. A compensation method for the overlap time is proposed in [114], which adds overlap time to the gate signal of the switch that bears reverse voltage. It assumes that the transition time is much smaller than the pulse width and can be omitted. But this assumption is not precise when the sinusoidal voltage on the device is crossing zero or the current on the dc inductor is small at light load.

Another distortion comes from the modulation scheme. The 12-sector space vector modulation has been shown to have lower switching loss compared to traditional 6-sector

modulation schemes [94]-[97]. Two sub-sectors are divided according to the input current and voltage relationship in each 60˚ sector in Fig. 2. The vector arrangement will be changed to achieve lowest switching voltage in two sub-sectors. But this will produce irregular pulse distribution and cause input current distortion at the moment of sector change [83][114][128][130]. When the arrangement of the vectors alternates near the boundary of two sub-sectors, the interval between two pulses will become short on one switch and long on its complementary switch.

2.5 Protection

Large overvoltage occurs when the current of the dc-link inductor is interrupted in current source converters due to fault gate drive signals [115]. It causes avalanche breakdown and failure of the semiconductor devices [116]. When applying the SiC MOSFETs, the overvoltage will reach its breakdown voltage in a very short period due to its high switching speed. It is important to have a fast overvoltage protection scheme in the current source converter built with SiC MOSFETs.

In previous research, several overvoltage protection schemes have been proposed for IGBT-based converters. A diode bridge is applied to detect the overvoltage on the devices in [115][117]-[119]. Their difference lies on the voltage clamping circuit. In [117]-[119], a capacitor is used to absorb the energy in the inductor and reduce the overvoltage on the semiconductor devices. A special pre-charge process is needed for this protection circuit during converter start-up. Moreover the large capacitor in the protection circuit will worsen the switching performance of the switches in normal operation. In [115], the Si MOSFETs in the protection circuit are operated in avalanche breakdown to clamp the overvoltage. But they are not designed for this operation mode. An auxiliary IGBT is used in [115] to provide a

freewheeling path for the dc-link inductor. It can not protect the device when the currents on the positive and negative buses are not equal in some grounding faults.

2.6 Research Challenges and Approaches

- The conduction loss is high in CSR due to the devices connected in series. A new current source rectifier topology, Delta-type Current Source Rectifier (DCSR), will be proposed. It has delta connection on its input side and the dc-link current can be shared by more switches to reduce the conduction loss.
- It is unclear what the advantages of CSRs are over conventional voltage source converters and where CSRs should be applied. The CSRs will be compared with traditional topologies comprehensively on efficiency and power density in high power rectifier, power supply for data center and dc fast charger for EVs.
- The parasitics in the package and circuit are the main factor that limits the switching speed of fast SiC devices. To minimize the parasitics, the SiC devices will be packaged in a compact power module for CSR. The switching speed can be increased.
- The switching loss of Reverse Blocking IGBTs (RB-IGBT) is higher than standard IGBTs. To minimize its switching loss, the space vectors in the modulation should be arranged to eliminate the transitions with the highest switching losses. Four modulation schemes will be compared for different device combinations, showing which one is most efficient.
- The charge error caused by overlap time and slow transition will result in input current distortion. A modified pulse-based compensation method will be proposed to compensate the charge error and reduce the current distortion.

- Under low output power, the dc-link current will become discontinuous and the conventional control can not work consistently well. The three-phase CSR will be modeled in discontinuous current mode (DCM) and the modulation and control methods will be proposed for this operating mode to reduce the input current distortion and the output voltage ripple.
- Overvoltage will occur on semiconductor devices when the dc-link current is interrupted, leading to avalanche breakdown and damage of devices. A novel overvoltage protection scheme will be proposed for the three-phase current source rectifier built with SiC MOSFETs. It can clamp the overvoltage and dissipate the inductor energy safely.
- The input ac voltage will have harmonics and voltage sag. The rectifier is usually required to work normally under certain voltage disturbance. A control algorithm will be proposed to control the three-phase CSR under voltage disturbance and harmonics.

3 A New Topology for Current Source Rectifier

In this chapter, a new three-phase current source rectifier is proposed to reduce the device conduction loss. As shown in Fig. 3-1, the three phase legs in the rectifier are connected in a delta shape on the input side. In this way, the dc-link current can be shared by more legs during operation to reduce the conduction loss. Although it needs six more diodes, the current rating of each diode is only half of those in traditional CSR topology in Fig. 3-2. . The freewheeling diode Df can also be used to reduce conduction loss. The design of control algorithm, input and output filters are the same as that in traditional CSR. Since the output voltage must be positive, the energy can only be transferred unidirectionally in the proposed topology in Fig. 3-1. With the bidirectional topology in Fig. 3-3, the energy can be transferred in both directions.

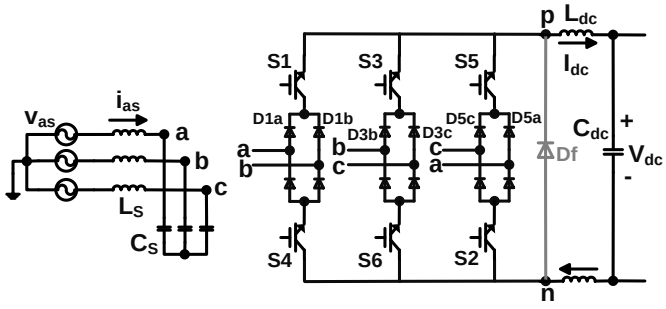


Fig. 3-1. Delta-type Current Source Rectifier.

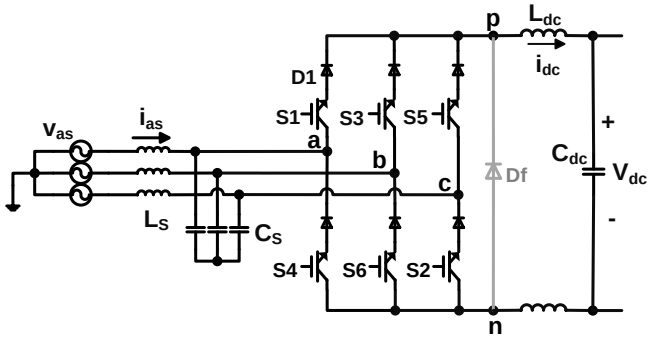


Fig. 3-2. Traditional three-phase CSR.

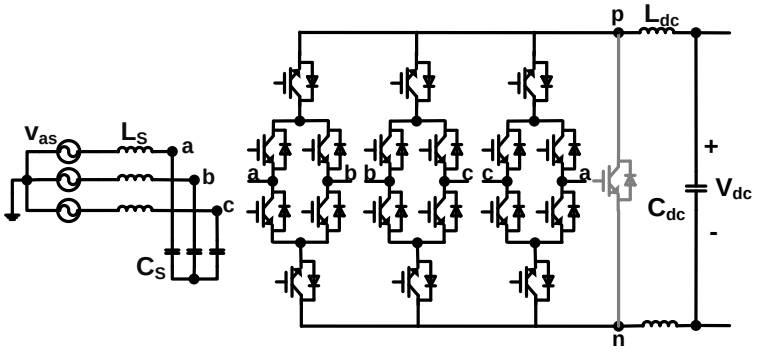


Fig. 3-3. Bidirectional Delta-type Current Source Rectifier.

3.1 Operation Principle

For the analysis of the rectifier, its input voltages v_a, v_b and v_c and the fundamental components i_{a1}, i_{b1} and i_{c1} of its input currents are defined in (3-1), where V_m and I_m are the peak values of the sinusoidal voltage and current respectively, ω is the mains angular frequency and φ is the phase difference between v_a and i_{a1}.

$$\begin{cases} v_a = V_m cos(\omega t + \varphi), i_{a1} = I_m cos(\omega t) \\ v_b = V_m cos\left(\omega t - \dfrac{2\pi}{3} + \varphi\right), i_{b1} = I_m cos\left(\omega t - \dfrac{2\pi}{3}\right) \\ v_c = V_m cos\left(\omega t + \dfrac{2\pi}{3} + \varphi\right), i_{c1} = I_m cos\left(\omega t + \dfrac{2\pi}{3}\right) \end{cases} \tag{3-1}$$

According to the relationship between the input voltage and current, 12 sectors are divided in Fig. 3-4 for the buck rectifier. On the space vector plane in Fig. 3-5, the input current space vector $i_{abc}^{*} = \sqrt{\frac{2}{3}}\left(i_{a1} + i_{b1}e^{j\frac{2\pi}{3}} + i_{c1}e^{j\frac{-2\pi}{3}}\right) = \sqrt{\frac{3}{2}}I_m e^{j\omega t}$ can be synthesized by six active space vectors $\overrightarrow{I_x}, x = 1, \ldots, 6$ and a zero vector $\overrightarrow{I_0}$. $[x, y], x, y = a, b, c, x \neq y$ denotes that the switch connected with phase a and phase c are conducting the dc-link current in a space vector. Considering both the switching loss and modulation index range, i_{abc}^{*} is usually composed by two consecutive active vectors and the zero vector in each sector [94][95][97]. In the following analysis, Sector 12 $(-\pi/6 \leq \omega t < -\varphi, V_a > V_c \geq V_b)$ will be selected as an example to demonstrate the operation principle of the new CSR.

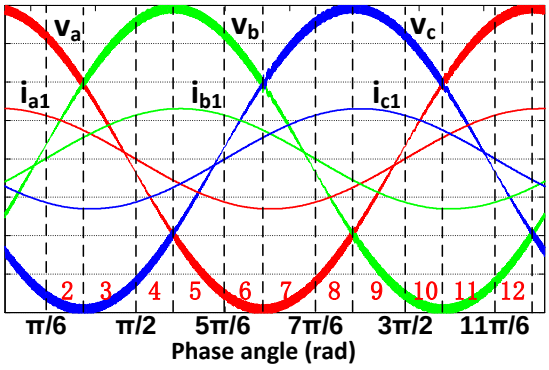


Fig. 3-4. Fundamental components of input current and voltage.

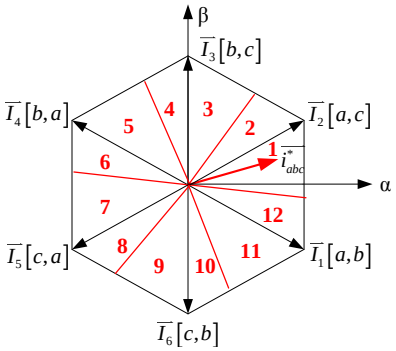


Fig. 3-5. Space vector plane.

3.1.1 Conduction States

The equivalent circuit is shown in Fig. 3-6 for the new CSR in Sector 12 according to the relationship of the input voltages. For example, the diode D1b is blocked and D1a is conducting since $V_a > V_b$. There are more conduction states in the new CSR than in the traditional CSR, as

shown in Fig. 3-7(a) and (b). In Sector 12, there are seven conduction states in Fig. 3-7 (a) for the space vector $\overrightarrow{I_1}$. $[S_x, S_y]$, $x, y = 1, \ldots, 6$ indicates the on state of the switches Sx and Sy in current conduction state. For example, the current flow path is shown in Fig. 3-8 for the conduction state $[(S_1S_5), (S_4S_6)]$. To realize the space vector $\overrightarrow{I_1}$, both S_1 and S_5 are turned on to share the current in phase a and both S_4 and S_6 are turned on to share the current in phase b. In this way, the dc-link current I_{dc} can be shared by two paralleled devices instead of one in traditional CSR. The conduction states will change in different sectors according to the relationship between input voltages. In Sector 1 ($-\varphi \leq \omega t < \pi/6, V_a > V_b \geq V_c$), the equivalent circuit and conduction states are shown in Fig. 3-9 and Fig. 3-10 respectively, which are different from that in Sector 12.

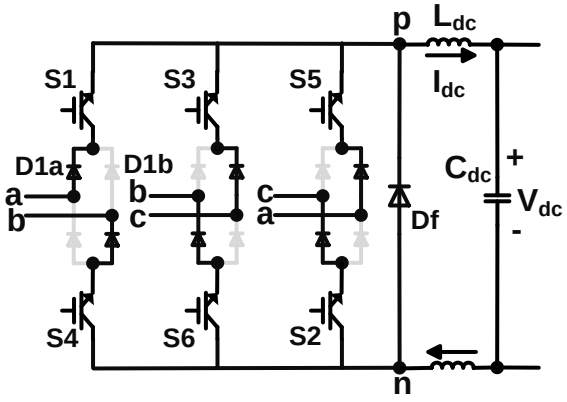


Fig. 3-6. Equivalent circuit of DCSR in Sector 12.

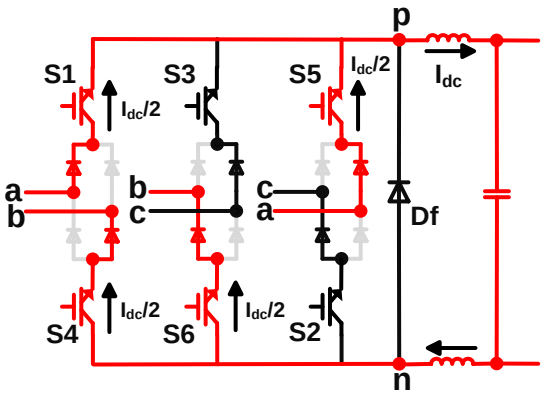
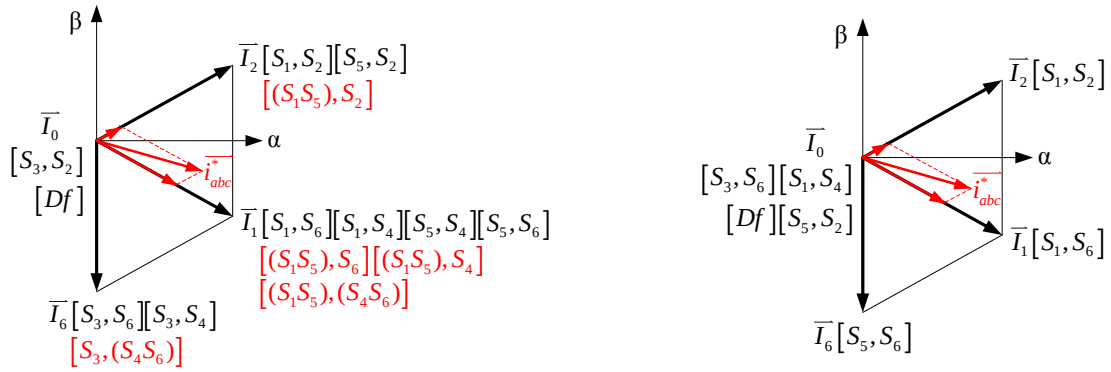


Fig. 3-7. Conduction state $[(S_1S_5),(S_4S_6)]$.



(a) (b)

Fig. 3-8. Different conduction states in Sector 12 in (a) DCSR and (b) traditional CSR.

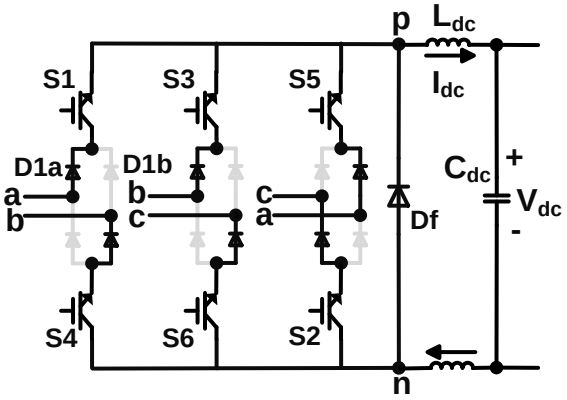


Fig. 3-9. Equivalent circuit of DCSR in Sector 1.

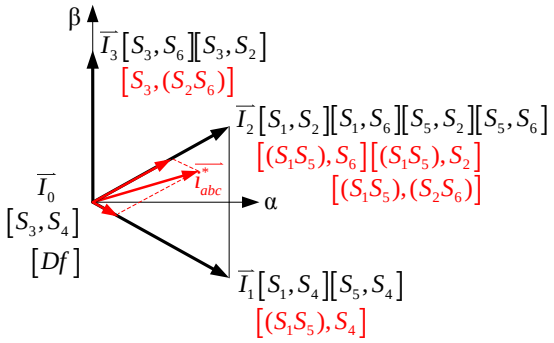


Fig. 3-10. Different conduction states in Sector 1.

3.1.2 Modulation Scheme

The modulation scheme in the traditional CSR can be easily transferred to the one in the new CSR. The “3-switch” and “4-switch” space vector modulation schemes, which contain three and four commutations in a switching period respectively, are most widely used in traditional CSRs because they achieve a good compromise between the switching loss and harmonic current level [98]. “Modified Fullwave Symmetrical Modulation (MFSM)” was introduced in [94]. The space vectors in MFSM are arranged to make the switching voltage the lowest, so that the

switching loss is assumed to be minimum [94][95]. The gate signals of six switches in the traditional CSR are shown in Fig. 3-11 for MFSM in Sector 12. The modulation scheme can be characterized through its output voltage v_{pn} and input currents i_a, i_b and i_c in Fig. 3-11.

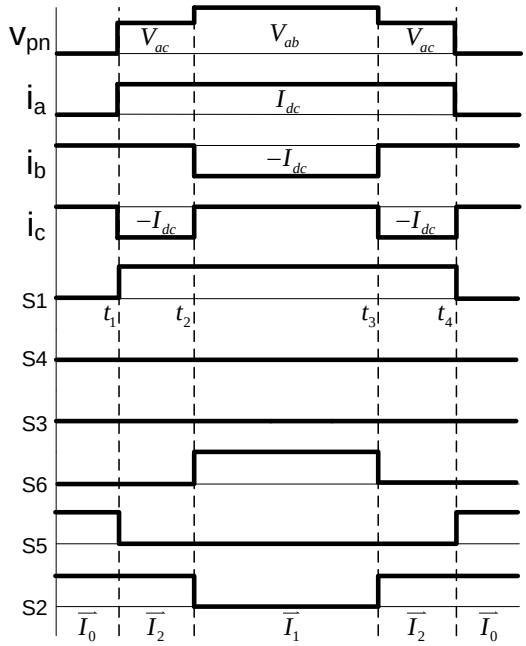


Fig. 3-11. Modulation scheme of traditional CSR in Sector 12.

The modulation scheme can be transferred to the new CSR simply by substituting the conduction state of each space vector with the new one. The modulation scheme for minimum conduction loss is demonstrated in Fig. 3-12(a). To reduce the conduction loss of the converter, it is recommended to use as many devices as possible to share the dc-link current. The conduction state $[(S_1S_5),(S_4S_6)]$ is selected for the space vector $\overrightarrow{I_1}$ instead of $[S_1,S_6]$, and $[(S_1S_5),S_2]$ is chosen for $\overrightarrow{I_2}$ instead of $[S_1,S_2]$. The switching loss will not change much if the switching energy is assumed to be proportional to the product of the switching voltage and current. At moment t_1,

both S_1 and S_5 are turned off. Their total switching energy is comparable to the respective one in Fig. 3-11 since they each carry only half dc-link current.

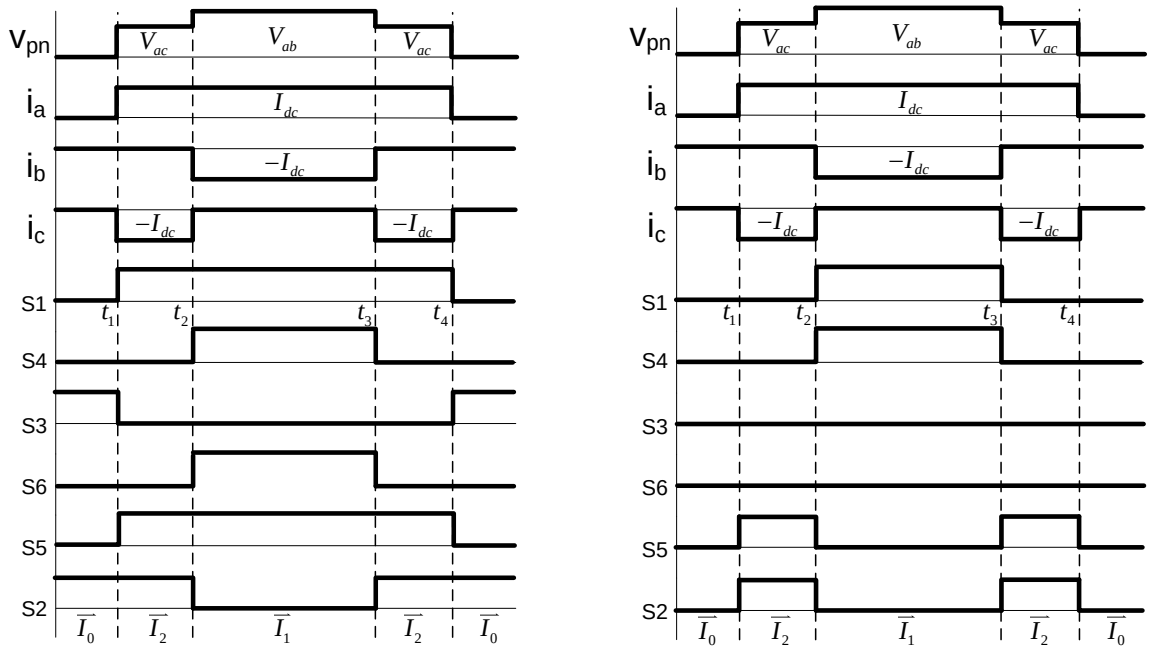


Fig. 3-12. Modulation schemes of DCSR in Sector 12 for (a) minimum conduction loss or (b) least gate signals.

The freewheeling diode Df is usually added to reduce the conduction loss during zero vector in buck rectifiers. Another modulation scheme is proposed in Fig. 3-12(b) to reduce the gate signals for the devices. As shown in Fig. 3-12(b), S1 and S4 have the same gate signals and S5 and S2 can share the same gate signal. The total gate signals can be reduced from six to three. The zero vector is realized by Df in this modulation scheme.

3.1.3 Control Algorithm

The control algorithm for the new CSR is the same as the one used in the traditional CSR. In three-phase CSRs, the controller is usually designed in dq rotating coordinate system where the converter model is time-invariant. Usually the digital controller includes two control loops as shown in Fig. 3-13 [99][38]. In the outer dc voltage control loop, the voltage on the output dc capacitor is fed back to the compensator to generate the dc current reference for the inner current control loop. In the current control loop, the current in the dc-link inductor is fed back to the current compensator to generate D_d, the duty cycle on the d axis. Then the space vectors are synthesized and the duty ratios d_1 and d_2 of two active vectors are calculated for modulator to generate PWM signal for each switch.

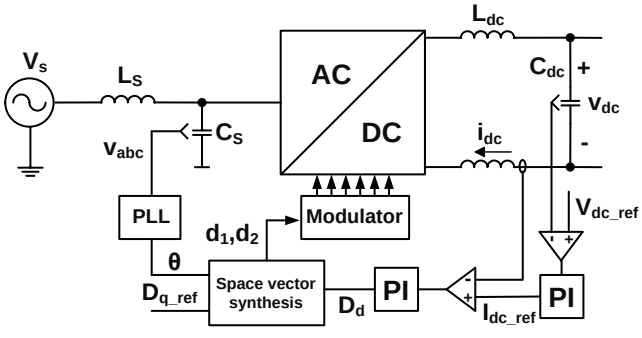


Fig. 3-13. Control algorithm of DCSR.

Table 3-1. Specification of DCSR

Output power	7.5 kW
Input voltage	480 Vac, 60Hz
Input inductor	110 μH each phase
Input capacitor	6.8 μF each phase
Output voltage	400 Vdc
Output capacitor	150 μF
Switching frequency	28 kHz
DC-Link inductor	1.9 mH

The simulation waveforms are shown in Fig. 3-14 for the new CSR with specifications listed in Table 3-1. The modulation scheme in Fig. 3-12(a) was applied in the simulation. The input current is almost sinusoidal and in phase with the input voltage. The currents of S_1 and D_{1a} have three levels (I_{dc}, $I_{dc}/2$ and 0), which can be predicted based on the previous analysis.

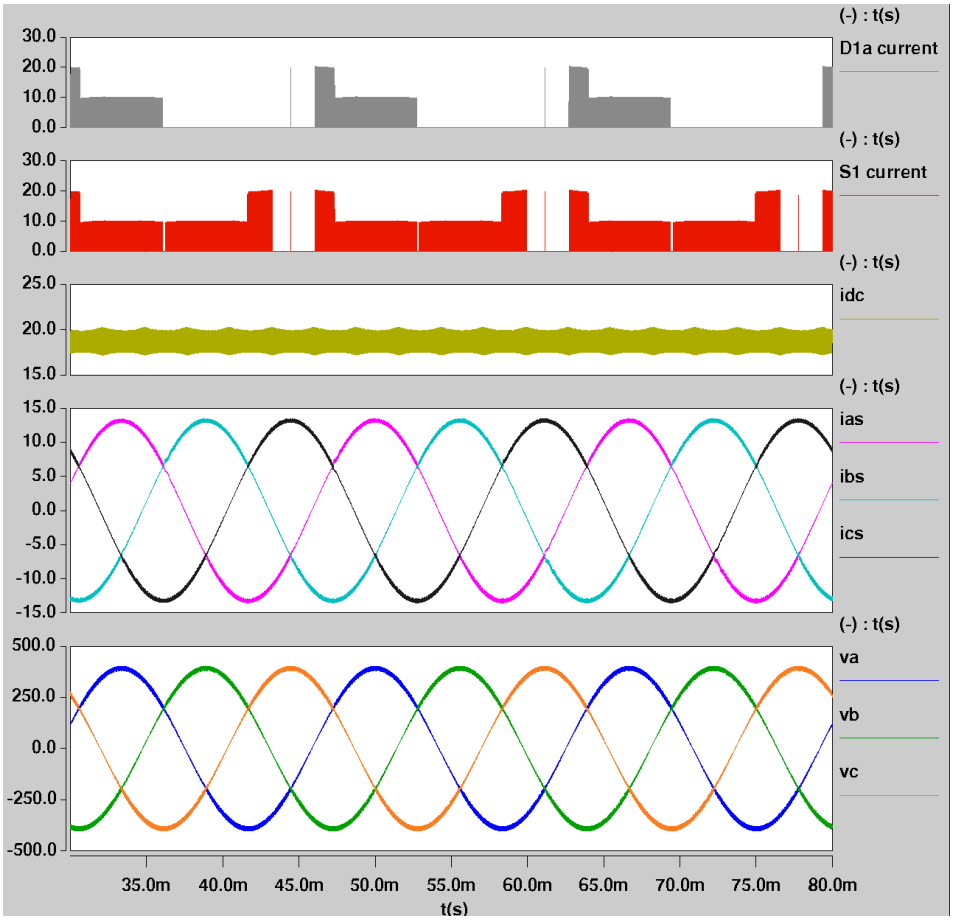


Fig. 3-14. Simulation waveforms of new CSR.

3.2 Component Stress and Loss Analysis

In this section, the stress of semiconductor devices and passive components will be analyzed in detail to provide the design guidelines for the new CSR. To simplify the analysis, several assumptions are specified:

- The input voltage on the input capacitor C_s is assumed to be pure sinusoidal, as defined in (3-1).
- The fundamental-frequency component of the input current of the buck rectifier has a phase difference φ from the C_s voltage, as defined in (3-1).

- The load current is constant I_{dc} and the load voltage is constant V_{dc}.
- The switching frequency f_s is assumed to be much higher than the line frequency f.
- The analysis is based on the modulation scheme in Fig. 3-12(a).
- The switching energy has a linear relationship with respect to the product of the switching voltage v_s and current i_s. The turn-on energy $E_{on} = k_{on}|v_s i_s|$. The turn-off energy $E_{off} = k_{off}|v_s i_s|$.

3.2.1 Stress of Semiconductor Devices

1) Switch S_1: The maximum voltage stress $V_{S_1,max,DCSR}$ on the switches in DCSR is 1.5 times of the maximum line-to-neutral ac voltage $V_{m,}$, which is given by (3-2).

$$V_{S_1,max,DCSR} = \frac{3}{2}V_m \tag{3-2}$$

The modulation index is defined as $M = \frac{I_m}{I_{dc}} = \frac{2V_{dc}}{3V_m cos\varphi}$. The average and rms currents of the switch can be derived by

$$\begin{aligned} I_{S_1,avg} &= \frac{1}{2\pi}\int_0^{2\pi} i_{S_1} d(\omega t) = \frac{I_{dc}}{3} \\ I_{S_1,rms} &= \sqrt{\frac{1}{2\pi}\int_0^{2\pi} {i_{S_1}}^2 d(\omega t)} = I_{dc}\sqrt{\frac{1}{3} - \frac{\sqrt{3}Mcos\varphi}{4\pi}} \end{aligned} \tag{3-3}$$

If the freewheeling diode Df is added to freewheel current during zero vector, the current stress of the switch will be reduced and can be written by

$$I_{S_1,avg} = \frac{I_{dc}M}{\pi}, I_{S_1,rms} = I_{dc}\sqrt{\frac{M\left(4 - \sqrt{3}cos\varphi\right)}{4\pi}} \tag{3-4}$$

With the current stress, the conduction loss of S1 can be derived by

$$P_{S_1,conduction} = I_{S_1,avg}V_{S_1,on} + {I_{S_1,rms}}^2 R_{S_1,on} \tag{3-5}$$

where $V_{S_1,on}$ and $R_{S_1,on}$ are the forward voltage drop and on resistance of the switch.

The switching loss for each switch is given by

$$P_{S_1,switching} = \frac{\sqrt{3}V_m f_s I_{dc}\left(k_{on} + k_{off}\right)}{2\pi} \tag{3-6}$$

2) Branch diodes D_{1a} and D_{1b}: The maximum voltage stress on the branch diodes is the maximum line-to-line ac voltage $\sqrt{3}V_m$. The average and rms currents of the branch diodes are given by

$$\begin{aligned}
I_{D_{1a},avg} &= \frac{1}{2\pi}\int_0^{2\pi} i_{D_{1a}} d(\omega t) = \frac{I_{dc}}{6} - \frac{I_{dc}Msin\varphi}{4\pi} \\
I_{D_{1a},rms} &= \sqrt{\frac{1}{2\pi}\int_0^{2\pi} {i_{D_{1a}}}^2 d(\omega t)} = I_{dc}\sqrt{\frac{4\pi - 6Msin\varphi - 3\sqrt{3}Mcos\varphi}{24\pi}} \\
I_{D_{1b},avg} &= \frac{1}{2\pi}\int_0^{2\pi} i_{D_{1b}} d(\omega t) = \frac{I_{dc}}{6} + \frac{I_{dc}Msin\varphi}{4\pi} \\
I_{D_{1b},rms} &= \sqrt{\frac{1}{2\pi}\int_0^{2\pi} {i_{D_{1b}}}^2 d(\omega t)} = I_{dc}\sqrt{\frac{4\pi + 6Msin\varphi - 3\sqrt{3}Mcos\varphi}{24\pi}}
\end{aligned} \tag{3-7}$$

If the freewheeling diode Df is added to freewheel current during zero vector, the current stress of the branches will be reduced and can be derived by

$$I_{D_{1a},avg} = \frac{I_{dc}M(2-sin\varphi)}{4\pi}, I_{D_{1a},rms} = I_{dc}\sqrt{\frac{M\left(4-\sqrt{3}cos\varphi-2sin\varphi\right)}{8\pi}}$$
$$I_{D_{1b},avg} = \frac{I_{dc}M(2+sin\varphi)}{4\pi}, I_{D_{1b},rms} = I_{dc}\sqrt{\frac{M\left(4-\sqrt{3}cos\varphi+2sin\varphi\right)}{8\pi}} \quad (3\text{-}8)$$

With the current stress, the conduction loss of the branch diode can be derived by

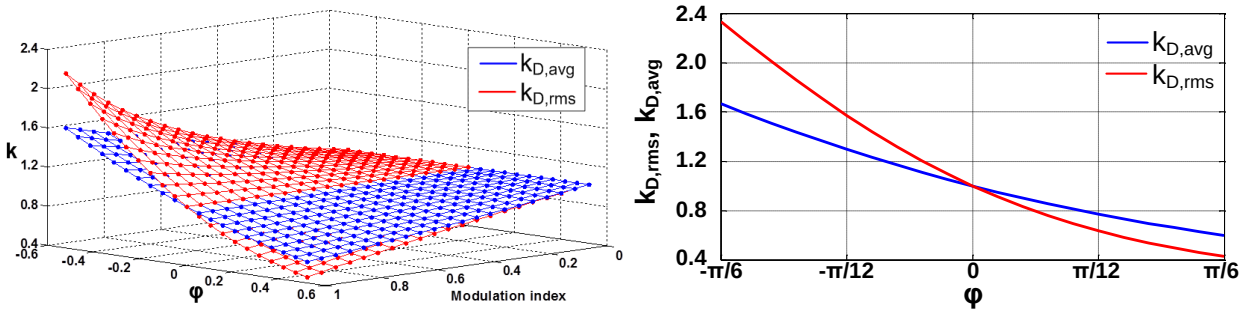
$$P_{D,conduction} = I_{D_{1a}/D_{1b},avg}V_{D,on} + {I_{D_{1a}/D_{1b},rms}}^2 R_{D,on} \quad (3\text{-}9)$$

where $V_{D,on}$ and $R_{D,on}$ are the forward voltage drop and on resistance of the branch diode.

The current stress is different on the two branches and is closely related to the phase angle φ as shown in (3-7) and (3-8). As φ deviates from zero, the range of each sector will change and the conduction period of the two branch diodes will be different. When $\varphi > 0$, D_{1a} has smaller current stress than D_{1b}. Otherwise, D_{1b} has smaller current stress. To show their difference, two parameters are defined as

$$k_{D,rms} = \frac{{I_{D_{1a},rms}}^2}{{I_{D_{1b},rms}}^2}, k_{D,avg} = \frac{I_{D_{1a},avg}}{I_{D_{1b},avg}} \quad (3\text{-}10)$$

The two parameters under different φ and modulation index are shown in Fig. 3-15. Without freewheeling diode, the difference of the current stress will become larger as modulation index increases or φ deviates from zero, as shown in Fig. 3-15(a). With freewheeling diode, $k_{D,rms}$ and $k_{D,avg}$ are only related with φ, as shown in Fig. 3-15(b).



(a) (b)

Fig. 3-15. $k_{D,rms}$ and $k_{D,svg}$ under different φ and modulation index (a) without or (b) with freewheeling diode Df.

3) Freewheeling diode Df: The maximum voltage stress on the freewheeling diode is the maximum line-to-line ac voltage $\sqrt{3}V_m$. The average and rms currents of Df are given by

$$I_{Df,avg} = I_{dc} - \frac{3I_{dc}M}{\pi}, I_{Df,rms} = I_{dc}\sqrt{1 - \frac{3M}{\pi}} \tag{3-11}$$

With the current stress, the conduction loss of the freewheeling diode can be derived by

$$P_{Df,conduction} = I_{Df,avg}V_{Df,on} + {I_{Df,rms}}^2 R_{Df,on} \tag{3-12}$$

where $V_{Df,on}$ and $R_{Df,on}$ are the forward voltage drop and on resistance of the freewheeling diode.

3.2.2 Stress of Passive Components

1) Dc-link inductor L_{dc}: The dc-link inductance is usually selected to limit the dc-link current ripple within 15% to 20% of the dc component at full load [100]. When $\varphi = 0$, the peak value of the ripple can be calculated by

$$\Delta i_{L_{dc},peak} = \frac{V_{dc}}{2L_{dc}f_s}\left(1 - \frac{\sqrt{3}V_{dc}}{3V_m}\right) < 7.5\% \cdot I_{dc} \tag{3-13}$$

When $\varphi = 0$, the rms current of the dc-link inductor can be derived by

$$i_{L_{dc},rms} = \sqrt{\left(\frac{1.11 \times 10^{-2}V_{dc}}{L_{dc}f_s}\right)^2 \left(\left(180\pi + 45\sqrt{3}\right)M^2 - \left(352 + 600\sqrt{3}\right)M + 240\pi\right) + {I_{dc}}^2} \tag{3-14}$$

2) Output capacitor C_{dc}: The maximum voltage stress of C_{dc} is the dc output voltage. When $\varphi = 0$, the rms current of the output capacitor can be approximated by

$$i_{C_{dc},rms} = \frac{1.11 \times 10^{-2}V_{dc}}{L_{dc}f_s}\sqrt{\left(180\pi + 45\sqrt{3}\right)M^2 - \left(352 + 600\sqrt{3}\right)M + 240\pi} \tag{3-15}$$

3) Input capacitor C_s: The maximum voltage stress of C_s is the maximum ac phase voltage V_m. The rms current of C_s is given by

$$i_{C_s,rms} = \sqrt{\frac{4{I_{dc}}^2 V_{dc}}{3\pi V_m cos\varphi} - \frac{{I_m}^2}{2}} \tag{3-16}$$

4) Input inductor L_s: When $\varphi = 0$, the rms value of the ripple current in the input inductor L_s is given by

$$\Delta i_{L_s,rms} = \frac{MI_{dc}}{{f_s}^2 L_s C_s}\sqrt{\frac{1}{36864}\left(25.6 - \left(96 + \frac{24\sqrt{3}}{\pi}\right)M^2 + \frac{398.76}{\pi}M^3 - \left(34 + \frac{13.5\sqrt{3}}{\pi}\right)M^4\right)} \tag{3-17}$$

For the input filter design, the total harmonic distortion is limited to less than 5%, which is written by

$$\Delta i_{L_s,rms} < 5\% \frac{I_m}{\sqrt{2}} \tag{3-18}$$

In Table 3-2, the stresses of the semiconductor devices and passive components have been calculated based on the derived equations and compared with the results from digital simulation with parameters shown in Table 3-1. The freewheeling diode is added to rectifier in both analysis and simulation.

Table 3-2. Component stress comparison

Component stress	**Analysis**	**Simulation**	**Deviation (%)**
$I_{S_1,avg}$	4.09 A	4.13 A	0.97
$I_{S_1,rms}$	6.61 A	6.71 A	1.49
$I_{D_{1a},avg}$	1.97 A	1.98 A	0.51
$I_{D_{1a},rms}$	4.51 A	4.61 A	2.17
$I_{D_{1b},avg}$	2.13 A	2.15 A	0.93
$I_{D_{1b},rms}$	4.83 A	4.93 A	2.03
$I_{D_f,avg}$	6.47 A	6.38 A	1.41
$I_{D_f,rms}$	11.02 A	10.95 A	0.64
$\Delta i_{L_{dc},peak}$	1.54 A	1.54 A	0.00
$i_{L_{dc},rms}$	18.77 A	18.77 A	0.00
$i_{C_{dc},rms}$	0.85 A	0.81 A	4.94
$i_{C_s,rms}$	8.45 A	8.68 A	2.65
$\Delta i_{L_s,rms}$	0.28A	0.28 A	0.00

3.3 Comparison with Traditional CSR

In this section, the new CSR will be compared with the traditional CSR on the current stress, conduction loss and switching loss of semiconductor devices.

3.3.1 Comparison of Device Current Stress

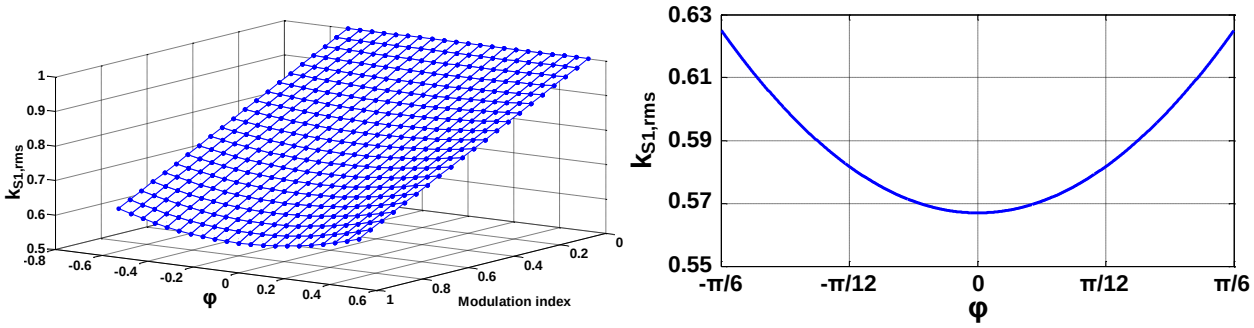
The analytical expressions of the device current stress have been derived in Section 3.2 for the new CSR. The design procedure has been well demonstrated for the traditional CSR [44][86]. The current stresses are listed in Table 3-3 for the traditional CSR with or without the freewheeling diode Df. Compared the current stresses of the devices in the two topologies, it can be seen that the rms current of the switch S_1 is reduced much in the new CSR. To demonstrate the difference of the rms currents, the parameter $k_{S_1,rms}$ is defined in (3-19), where $I_{S_1,rms,TR}$ is the rms current of S_1 in the DCSR and $I_{S_1,rms,SS}$ is the rms current of S_1 in the traditional CSR.

$$k_{S_1,rms} = \frac{{I_{S_1,rms,TR}}^2}{{I_{S_1,rms,SS}}^2} \tag{3-19}$$

The parameter $k_{S_1,rms}$ is related with the phase angle φ and the modulation index M, as shown in Fig. 3-16(a) when there is no freewheeling diode Df. In this case, $k_{S_1,rms}$ increases as the modulation index decreases. Because the zero vector will increase under low modulation index and the current is not shared by two devices in the zero vector. When the modulation index is fixed, $k_{S_1,rms}$ varies with φ and has minimum value when $\varphi = 0$. When the freewheeling diode Df is added, $k_{S_1,rms}$ is just related with φ as shown in Fig. 3-16(b). The rms current can be reduced by as high as 25% in the new CSR when $\varphi = 0$.

Table 3-3. Current stress in traditional CSR

	Without Df	**With Df**
Switch S_1	$I_{S_1,avg} = \frac{I_{dc}}{3},\ I_{S_1,rms} = I_{dc}\sqrt{\frac{1}{3}}$	$I_{S_1,avg} = \frac{I_{dc}M}{\pi},\ I_{S_1,rms} = I_{dc}\sqrt{\frac{M}{\pi}}$
Branch diode D_1	$I_{D_1,avg} = \frac{I_{dc}}{3},\ I_{D_1,rms} = I_{dc}\sqrt{\frac{1}{3}}$	$I_{D_1,avg} = \frac{I_{dc}M}{\pi},\ I_{D_1,rms} = I_{dc}\sqrt{\frac{M}{\pi}}$
Freewheeling diode Df	-	$I_{Df,avg} = I_{dc} - \frac{3I_{dc}M}{\pi}$ $I_{Df,rms} = I_{dc}\sqrt{1 - \frac{3M}{\pi}}$



(a) (b)

Fig. 3-16. $k_{S_1,rms}$ under different φ and modulation index (a) without or (b) with freewheeling diode Df.

3.3.2 Comparison of Device Conduction Loss

Based on the previous analysis, the conduction loss of the semiconductor devices can be calculated under different operation conditions. The comparison conditions are listed in Table 3-4. The 1200V SiC Schottky diode from CREE is selected as the branch or the freewheeling diode

[82]. The switches are realized with either 1200V SiC MOSFET from CREE or 1200V Si Trench and Fieldstop IGBT [37][82]. The two topologies will be compared under the same chip area of the semiconductor devices. To generalize the comparison to different power ratings, the chip area is assumed to have the linear relationship with the current rating of the devices [120]. The relationship can be derived based on the die datasheets and is given by (3-20), where $A_{Si\ IGBT,\ 1200V}$ is the chip area of Si IGBT, $A_{SiC\ MOSFET,\ 1200V}$ the chip area of SiC MOSFET, $A_{SiC\ diode,\ 1200V}$ the chip area of SiC Schottky diode, and I_N is the device current rating (2 times of the operating current).

$$A_{Si\ IGBT,\ 1200V} = (0.95I_N + 3.2)\ mm^2,\ A_{SiC\ MOSFET,\ 1200V} = (0.52I_N)\ mm^2,$$
$$A_{SiC\ diode,\ 1200V} = (0.45I_N + 0.59)\ mm^2 \tag{3-20}$$

In the calculation, the threshold voltages of the Si IGBT and SiC Schottky diode do not change with the device rating. The on resistance of the device is inversely proportional to its chip area. The voltage drop V_{on} of the device can be given by (3-21), where V_o is the threshold voltage, i the device current, R_o the on resistance when the chip area is A, and $R_{o,N}$ is the on resistance when the chip area is A_N.

$$V_{on} = V_o \cdot i + i^2 \cdot R_o,\ R_o = \frac{R_{o,N} \cdot A_N}{A} \tag{3-21}$$

Table 3-4. Conditions for conduction loss comparison

Topology	**New CSR**	**Traditional CSR**
Output power	0 – 100 kW	
Input voltage	480 Vac, 60 Hz	
Modulation index	0 - 1	
Phase angle φ	-π/6 – π/6	

The conduction loss of the device can be calculated with the process in Fig. 3-17. It is related with the output power level, modulation index and the phase angle φ. The comparison results are shown in Fig. 3-18 when Si IGBT is applied as the switches. The new CSR has 10% to 15% lower conduction loss than the traditional CSR according to this comparison. If SiC MOSFET is applied as the switches as shown in Fig. 3-19, the conduction loss reduction can reach 15% to 20% because SiC MOSFETs do not have threshold voltage.

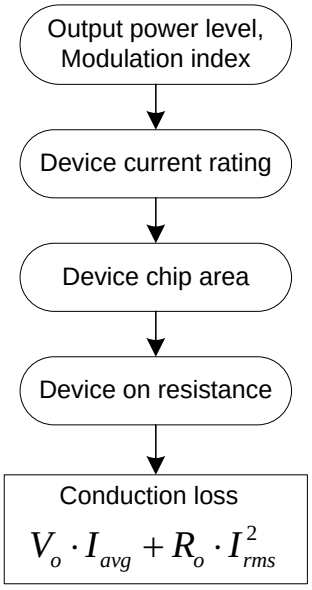
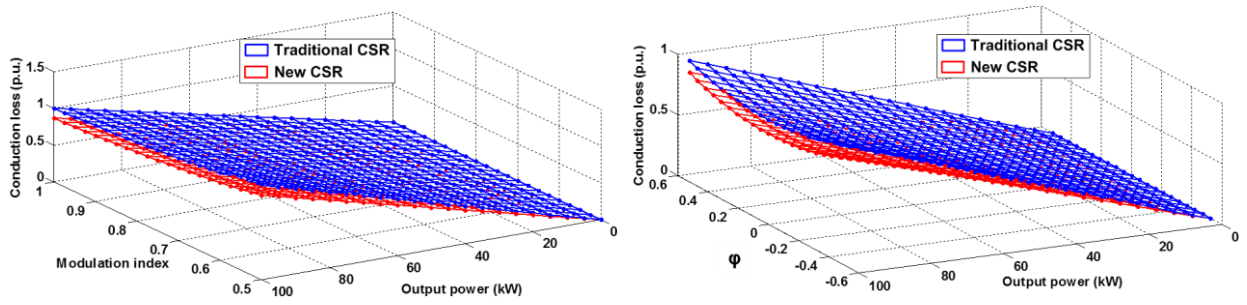
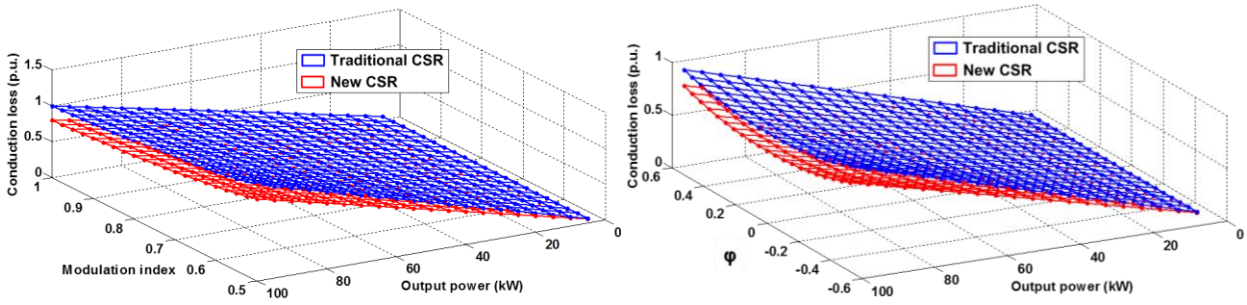


Fig. 3-17. Flow chart of conduction loss calculation.



(a) (b)

Fig. 3-18. Conduction loss comparison with Si IGBT when (a) φ = 0 or (b) M = 1.



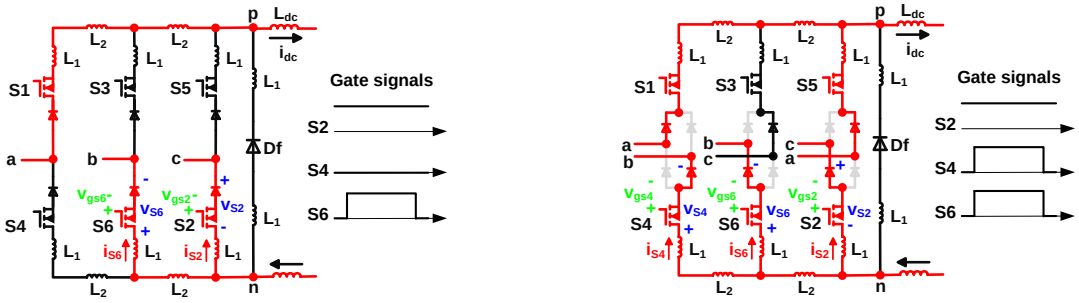
(a) (b)

Fig. 3-19. Conduction loss comparison with SiC MOSFET when (a) φ = 0 or (b) M = 1.

3.3.3 Comparison of Device Switching Loss

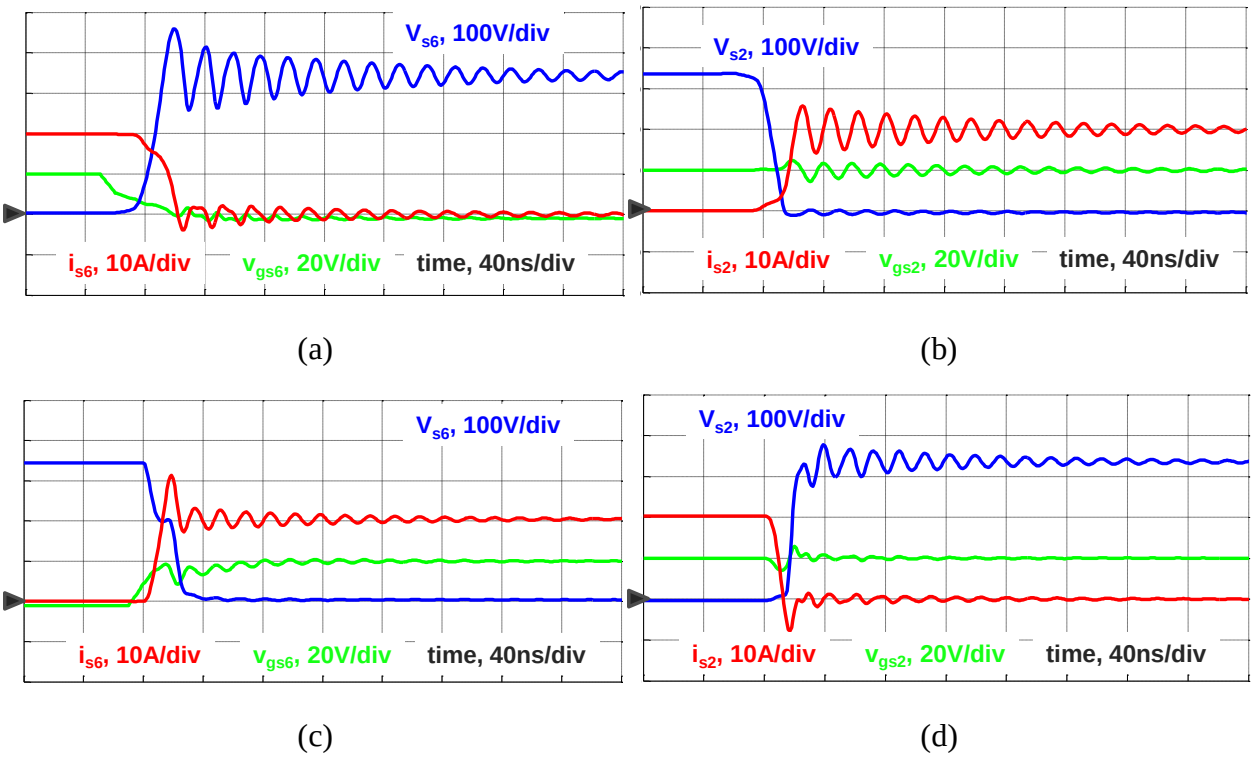
The commutation in the new CSR occurs between three switches rather than two in the traditional CSR. To analyze the difference on commutation and switching loss, the commutation circuit is modeled in Saber with the models of SiC MOSFET and Schottky diode from CREE [82]. In Sector 12 ($-\pi/6 \leq \omega t < \varphi, V_a > V_c > V_b$), the commutation circuits are drawn in Fig. 3-20(a) and (b) for the traditional CSR and the new CSR respectively. In Fig. 3-20(a), S_1 is kept on and S_6 is commutating with S_2. In Fig. 3-20(b), both S_1 and S_5 are kept on and S_4 and S_6 are

commutating with S_2 simultaneously. The parasitic inductance in the circuit is also modeled as L_1 = 20 nH and L_2 = 10 nH in the circuit.



(a) (b)

Fig. 3-20. Commutation circuits and gate signals in (a) traditional CSR and (b) new CSR.



(a) (b)

(c) (d)

Fig. 3-21. Switching waveforms of traditional CSR: (a) S_6 off (b) S_2 on (c) S_6 on (d) S_2 off.

The switching waveforms have more resonance in the new CSR, as shown in Fig. 3-22. In the turn-off process of S_4 and S_6 in Fig. 3-22(a), the voltage rise time is longer than that in Fig. 3-21(a) when only S_6 is turned off. Because the total junction capacitance of S_4 and S_6 is two times of that of S_6, it takes more time to charge it in Fig. 3-22(a). Also the resonance is worse due to the increased capacitance in the commutation loop. In the turn-on process of S_4 and S_6 in Fig. 3-22(c), both the current rise time and voltage fall time are less than those in Fig. 3-21(c) when only S_6 is turned on. Because the current is distributed in the two devices, the voltage level of miller plateau will decrease for each device. The resonance in Fig. 3-22 is damped slower than that in Fig. 3-21 because of the lower on resistance of device in the commutation circuit.

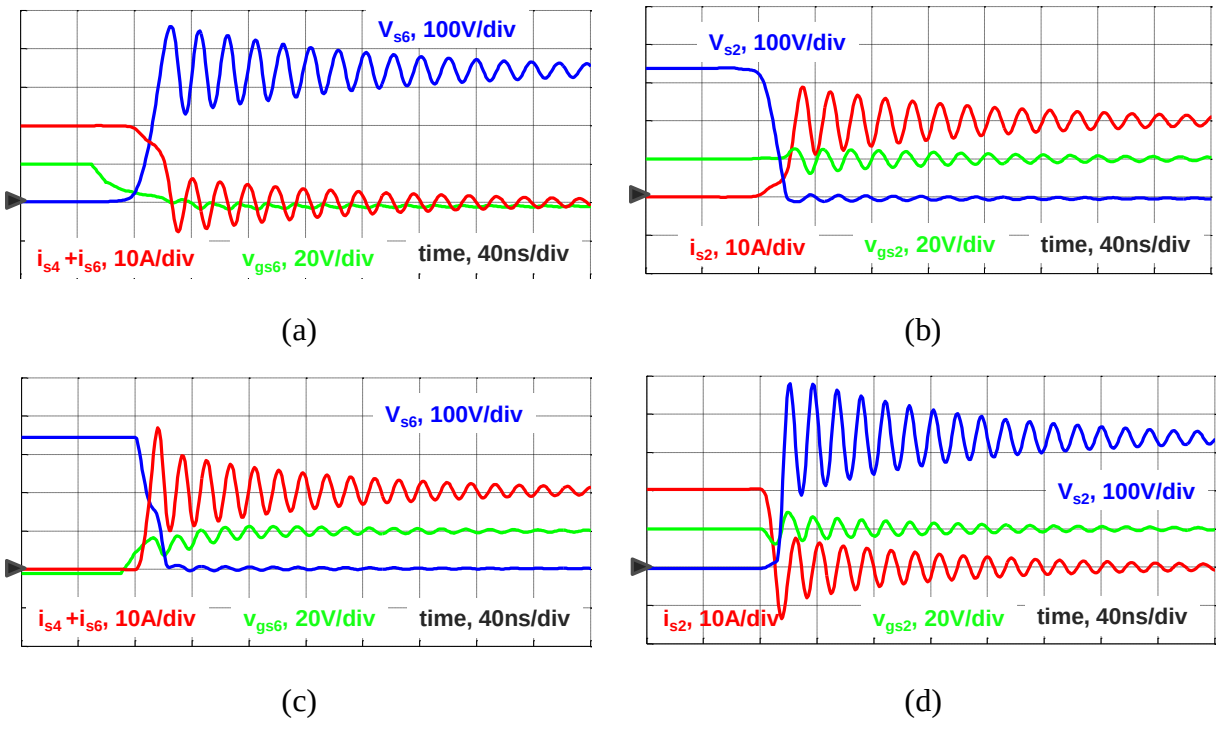


Fig. 3-22. Switching waveforms of new CSR
when (a) S_6 and S_4 off (b) S_2 on (c) S_6 and S_4 on (d) S_2 off.

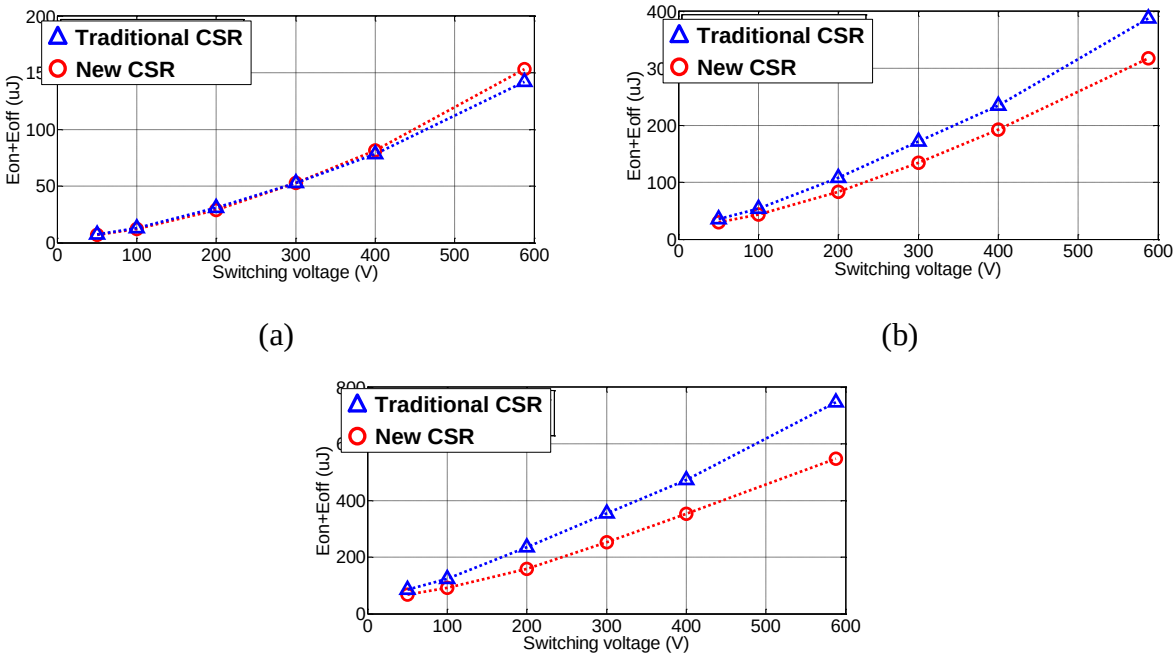


Fig. 3-23. Switching energy comparison when (a) $i_{dc} = 10\ A$ (b) $i_{dc} = 25\ A$ (c) $i_{dc} = 40\ A$.

The switching energy is calculated based on the simulation results under different voltage and current conditions. In Fig. 3-23(a), the new CSR has a little higher switching energy than the traditional CSR when $i_{dc} = 10A$. When the load current increases, its switching energy is less than the traditional CSR, as shown in Fig. 3-23(b) and Fig. 3-23(c). The advantage of the new CSR lies on its lower turn-on switching energy, which is more obvious under higher load current.

3.4 Device Current Sharing

The fundamental idea for reducing the conduction loss is to share the dc-link current in multiple legs in the new CSR. The current distribution depends on the on-state voltage drop of the paralleled devices. There might be as high as 50% difference between the on-resistances of two devices of the same type [82].

To study the impact of the current sharing to the conduction loss of the devices, the on-state voltage drops of the three phase legs are assumed to be $V_{S_1D_{1a}\ or\ S_1D_{1b}} : V_{S_3D_{3b}\ or\ S_3D_{3c}} : V_{S_5D_{5c}\ or\ S_5D_{5a}} = 1 : k_1 : k_2$, where $V_{S_xD_y}$ $(x = 1,3,5, y = 1a, 1b, 3b, 3c, 5c, 5a)$ is the total on-state voltage drop of the switch S_x and the branch diode D_y. The conduction loss changes with k_1 and k_2, as shown in Fig. 3-24. The conduction loss when $k_1 = k_2 = 1$ is selected as the base in the comparison. When $k_1 = k_2 = 1.5$, the conduction loss increases to 1.25 p.u.. When $k_1 = 1$ and $k_2 = 1.5$, it increases to 1.12 p.u.. In order to fully utilize the benefit of the new CSR, the devices in the rectifier should be selected to have close static characteristics in practice.

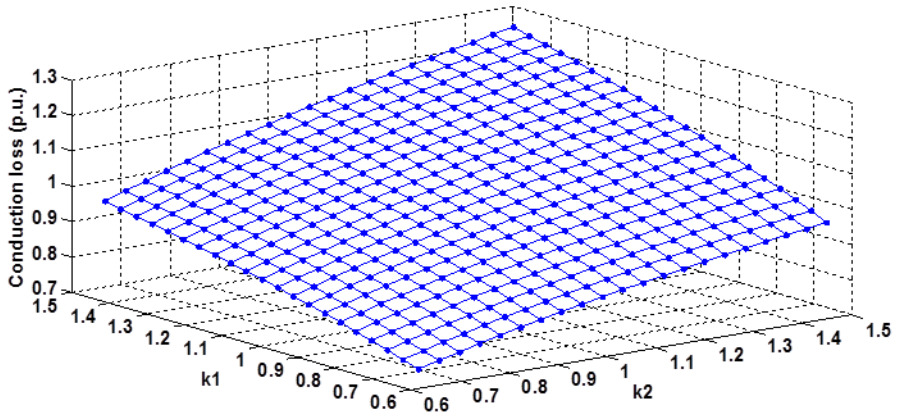


Fig. 3-24. Impact of current distribution on conduction loss.

3.5 Experimental Verification

As shown in Fig. 3-25, a 7.5 kW prototype of the new CSR was built with the specifications in Table 3-1. The size of the prototype in Fig. 3-25 is 9.125 in (L) × 6.875 in (W) × 5 in (H). The semiconductor devices and passive components used in the prototype are listed in Table 3-5.

1200 V/20 A SiC MOSFETs and 1200 V/ 18A SiC Schottky diodes are applied as the switches and diodes respectively in the prototype for their low on resistance and switching loss [82]. The switching frequency for the prototype is 28 kHz to balance between the efficiency and filter size [86].

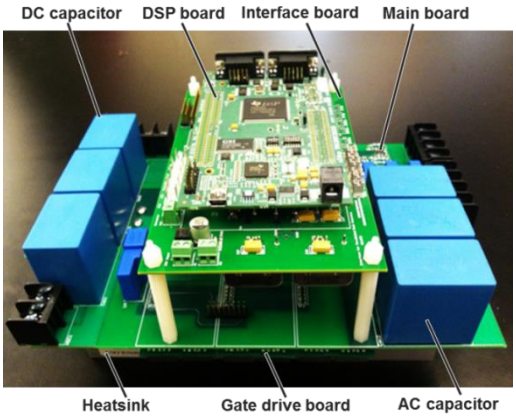


Fig. 3-25. 7.5 kW prototype of new CSR.

Table 3-5. Device and passive components in the prototype

Component	Description
Switches	SiC MOSFET, 1200 V/20 A, C2M0080120D, CREE
Branch and freewheeling diodes	SiC Schottky diode, 1200 V/18 A, C4D10120D, CREE
Input inductor	110 μH, Ferrite R, EE core, 0R45724EC, Magnetics, 13 turns of AWG#12 wire
Input capacitor	6.8 μF/330 Vac, film, B32916A3685, EPCOS
DC-link inductor	1.9 mH, Nanocrystalline, C core, MK Magnetics 42 turns of copper foil (cross section area = 12.9 mm^2)
Output capacitor	3×50 μF/450 Vdc, film, B32776G4506, EPCOS

The architecture of the prototype is drawn in Fig. 3-26. The Texas Instrument DSP F28335 is applied as the controller for the converter. The interface board is used for signal conditioning, auxiliary power supply and hardware protection. The main power is carried by the main board. The gate drive board is inserted between the semiconductor device and the main board. In this way, the common source inductance can be minimized to reduce the interference in the gate signals [121]. The photo of a single gate drive board is shown in Fig. 3-27(a) with one switch and two branch diodes on it. The three poles are used to connect with the ac and dc buses on the main board. There are six gate drive boards and one freewheeling diode board in the prototype converter, as shown in Fig. 3-27(b). With this structure, the prototype converter can also be configured as a traditional CSR. The two ac poles can be shorted on the gate drive board and connected to the same ac bus. It is convenient to compare the performance of the two topologies with single prototype converter.

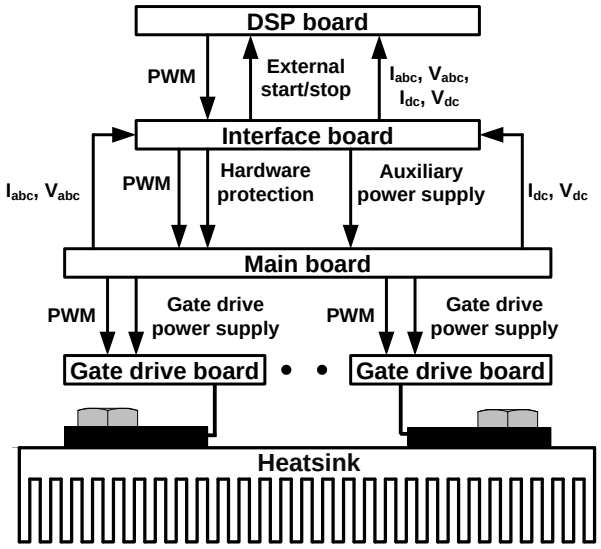
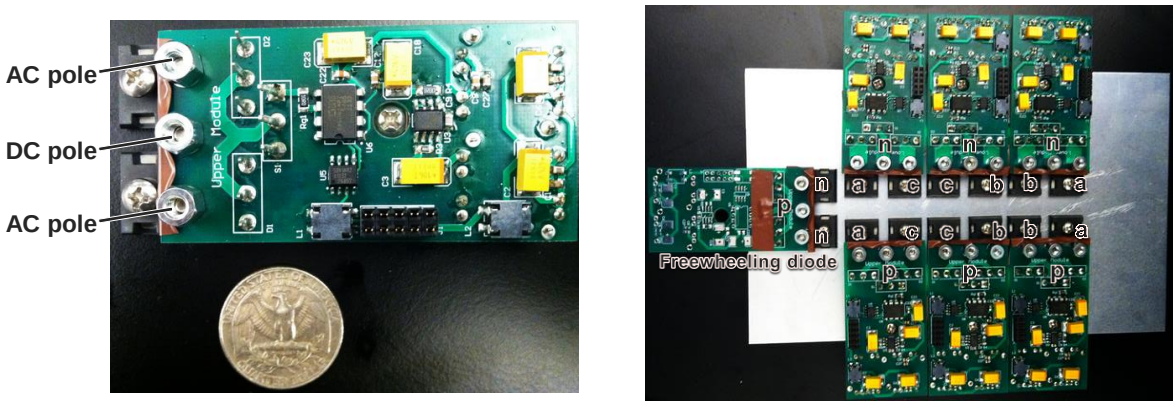


Fig. 3-26. Architecture of the prototype.



(a) (b)

Fig. 3-27. Gate drive board in the prototype: (a) Single board and (b) Assembled boards mounted on the heatsink.

In the experiments, the prototype converter is configured first as the new CSR then the traditional CSR and run up to the 8 kW output power. The experimental waveforms of the new CSR are shown in Fig. 3-28. The input current i_{as} has almost sinusoidal waveform and is in phase with the input voltage v_{as}. The dc-link current i_{dc} is controlled well at 20 A. The gate signal of the switch S1 is shown as v_{gs1} in Fig. 3-28 as well. The traditional CSR has similar experiment waveforms with the new CSR, as shown in Fig. 3-29.

The input current total harmonic distortion (THD) and the power factor are shown in Fig. 3-30 under different output power. The new CSR can achieve unity power factor and low input harmonics in most of the power range.

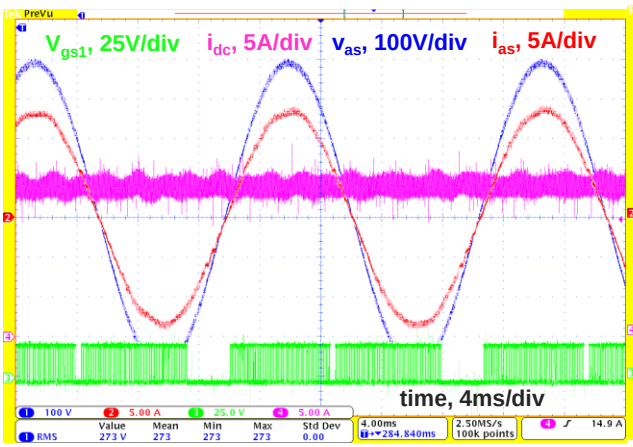


Fig. 3-28. Experiment waveforms of new CSR with 8 kW output power.

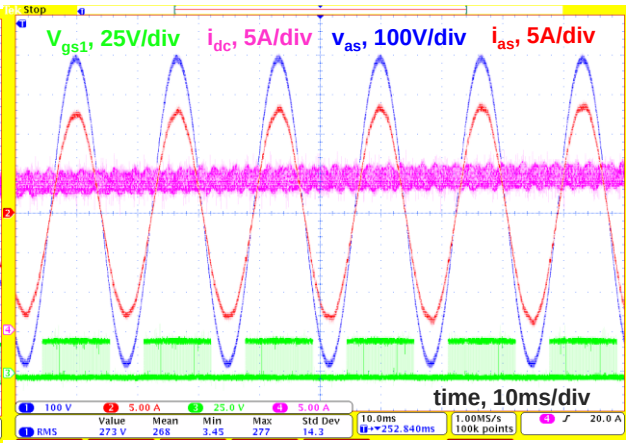


Fig. 3-29. Experiment waveforms of traditional CSR with 8 kW output power.

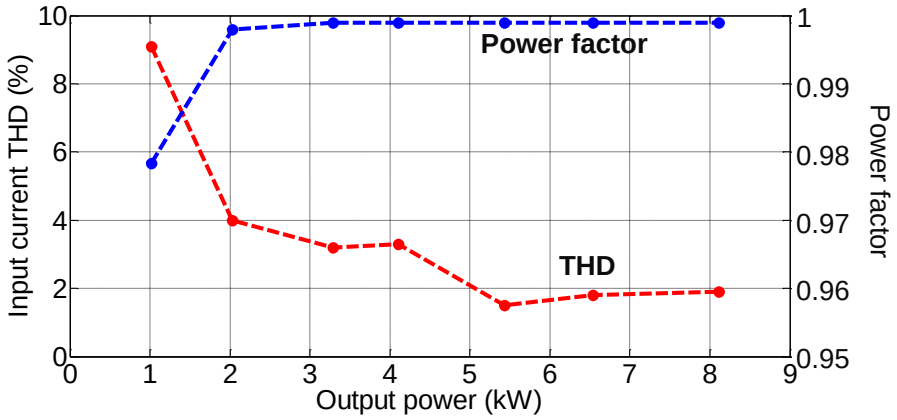


Fig. 3-30. Input current THD and power factor.

The semiconductor device loss of the new CSR and the traditional CSR can be calculated based on the analysis in previous sections. The loss of passive components can be calculated according to the method in [86]. The loss breakdown of the two topologies is shown in Fig. 3-31 based on the calculation when output power is 8 kW. The new CSR can save much conduction loss of the switches while keep other parts of loss comparable to the traditional CSR.

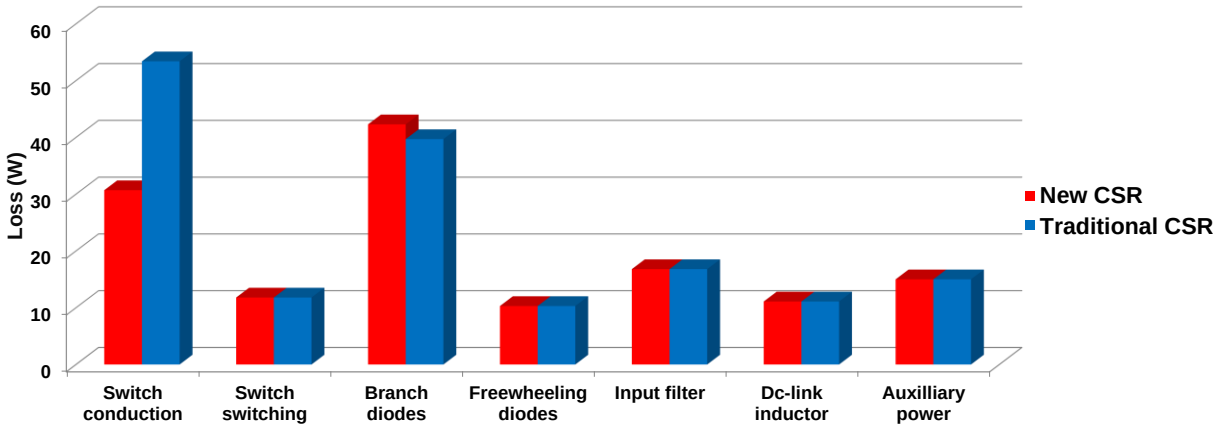


Fig. 3-31. Calculated loss breakdown and comparison.

The efficiency of both topologies is measured with YOKOGAWA PZ4000 and compared with the calculated efficiency under different output power in Fig. 3-32. The new CSR has higher efficiency over the whole power range.

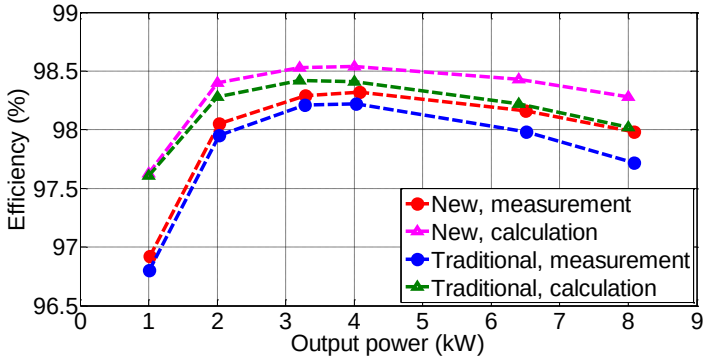


Fig. 3-32. Calculated and measured efficiency for the two topologies.

When the input voltage drops to 400 V, the conduction loss will increase, but the switching loss will decrease. As shown in Fig. 3-33, the loss breakdown of the two topologies is compared with the one under 480 V input voltage.

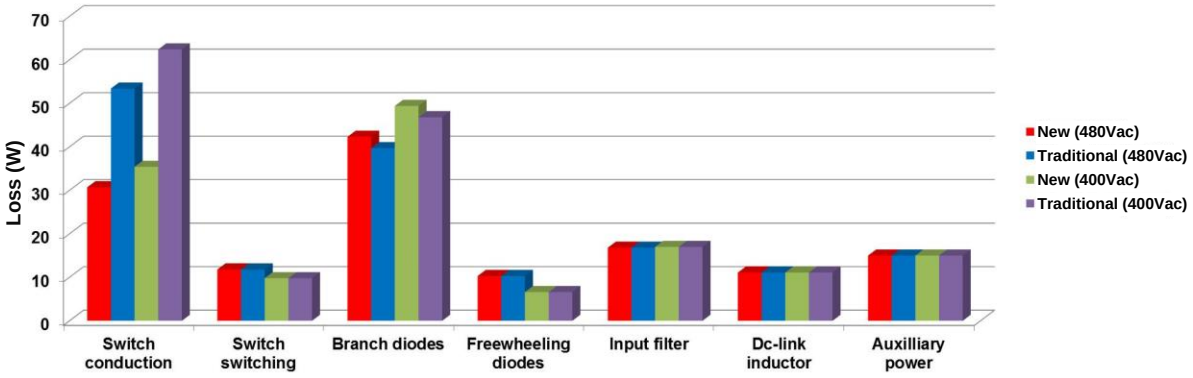


Fig. 3-33. Calculated loss breakdown and comparison with 480Vac or 400Vac input voltage.

The experimental waveforms under 400 V input voltage are shown in Fig. 3-34. With 400 V or 480 V input voltages, the measured efficiency curves are compared in Fig. 3-35. The new topology has higher efficiency than the traditional topology. For the same topology, the efficiency is higher when the input voltage is 400 V and the output power is low. The savings on the switching loss is higher than the increased conduction loss in these cases. When the output power is high, the efficiency will drop under 400 V input voltage due to the increased conduction loss.

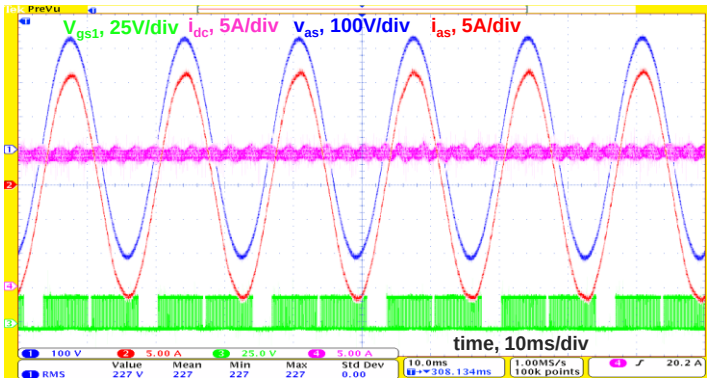


Fig. 3-34. Experimental waveforms under 400 V input voltage.

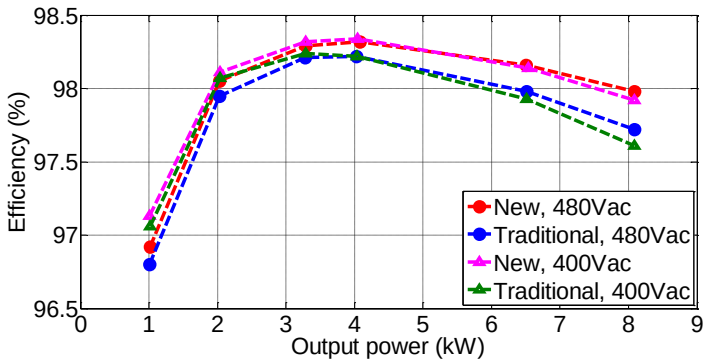


Fig. 3-35. Efficiency comparison with different input voltages.

The new topology is further tested and compared with the traditional one under different switching frequencies. The input voltage is 480 V and the output voltage is 400 V. As shown in Fig. 3-36 and Fig. 3-37, the dc-link current ripple is reduced as the switching frequency increases. The efficiency curves are measured and compared in Fig. 3-38 under different switching frequencies. The new topology has higher efficiency than the traditional one under different switching frequencies. The increased converter loss (mostly device switching loss) is shown in Fig. 3-39 when the switching frequency increases from 28 kHz to 46 kHz. In most cases, the new topology has lower loss incensement because of its higher switching speed.

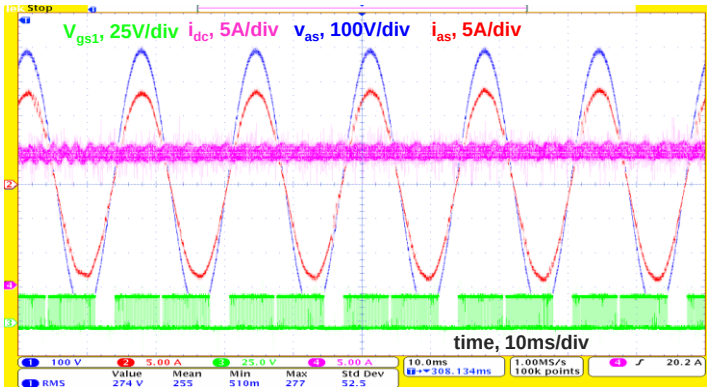


Fig. 3-36. Experimental waveforms under 35 kHz switching frequency.

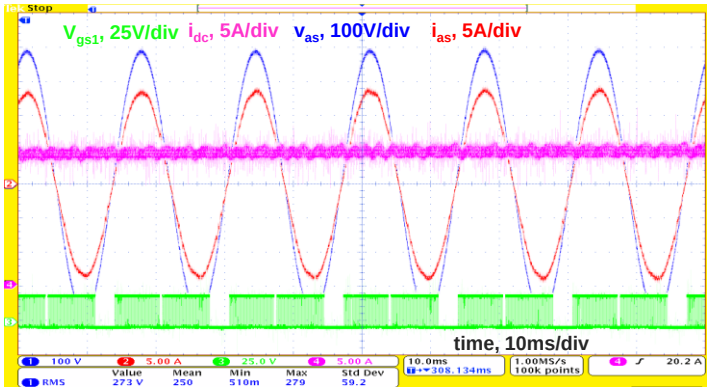


Fig. 3-37. Experimental waveforms under 46 kHz switching frequency.

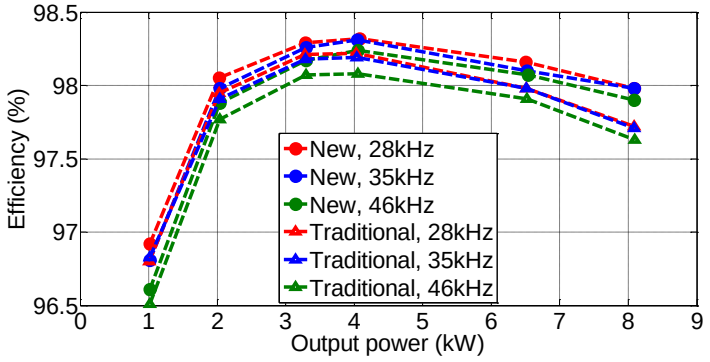


Fig. 3-38. Efficiency comparison with different switching frequencies.

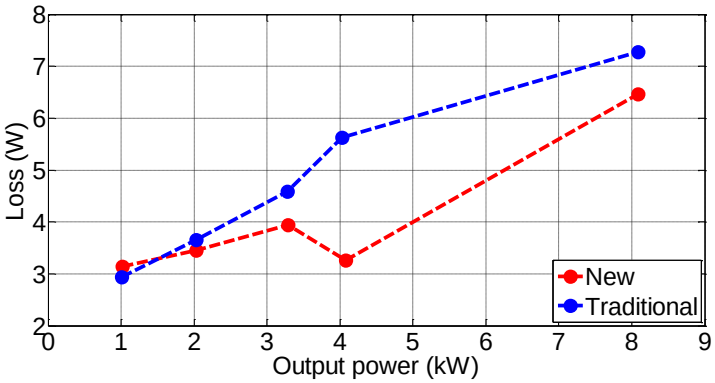


Fig. 3-39. Comparison of increased converter loss under different output power levels.

3.6 Conclusion

A new current source rectifier topology is proposed in this chapter. It has delta connection on its input side and the dc-link current can be shared by more switches to reduce the conduction loss. The conduction states and modulation schemes are analyzed for the new topology. The analytical equations of the current stress have been derived for the design of the new CSR. Compared with the traditional CSR, the proposed topology has lower device current stress and conduction loss. A 7.5 kW prototype was built to validate the performance of the proposed topology. It has been shown experimentally that the new CSR has higher efficiency over the traditional CSR.

4 Topology Comparison

The current source rectifier can be applied in high power rectifier (aluminum smelter, dc arc furnace, copper refinery, et al.), fast electric vehicle (EV) charger and data center power supply. In this chapter, the current source rectifier topologies will be compared with other wide-applied topologies on their efficiency and power density.

4.1 High Power Rectifier

In high power application, the rectifier usually has very high output current (up to hundreds kA) but comparatively lower output voltage (up to several kV). A step-down function is needed in these rectifiers and the output currents and voltages need to be well regulated in a wide range. The multiple-pulse thyristor rectifiers are widely applied in this application for its lower cost and high efficiency. Two current source rectifier topologies are compared with the 12-pulse thyristor rectifier in a 3.2 MW high power system, as shown in Fig. 4-1.

The specification of the system is listed in Table 4-1. The input voltage is stepped down from 22 kV at point of common coupling (PCC) to 750 V through a transformer. The output voltage will vary in the process of dc arc furnace. The converter loss only includes the semiconductor loss (switching and conduction loss) for efficiency calculation.

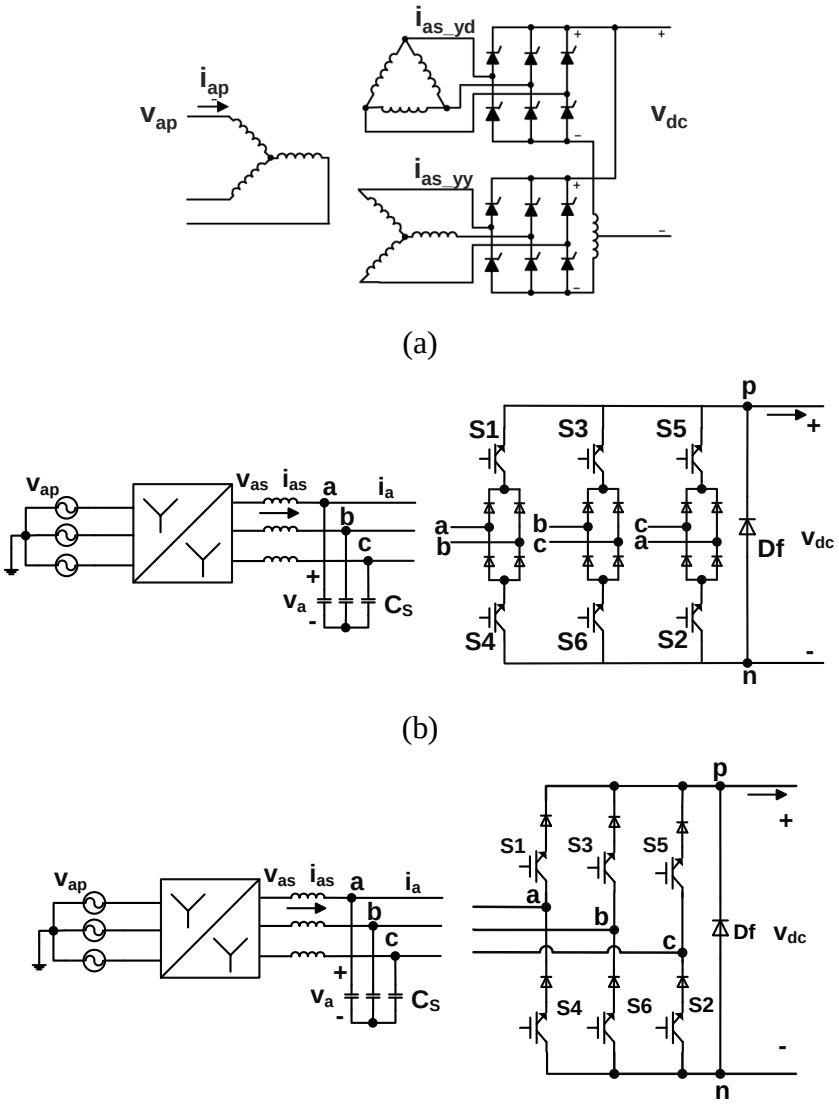


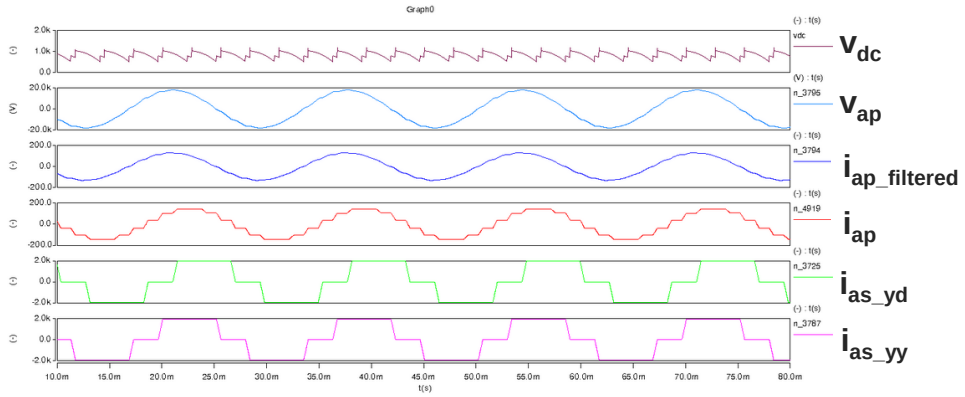
Fig. 4-1. Topologies for high power application: (a) 12-pulse thyristor rectifier; (b) DCSR; (c) Traditional CSR.

Table 4-1. High power rectifier specification

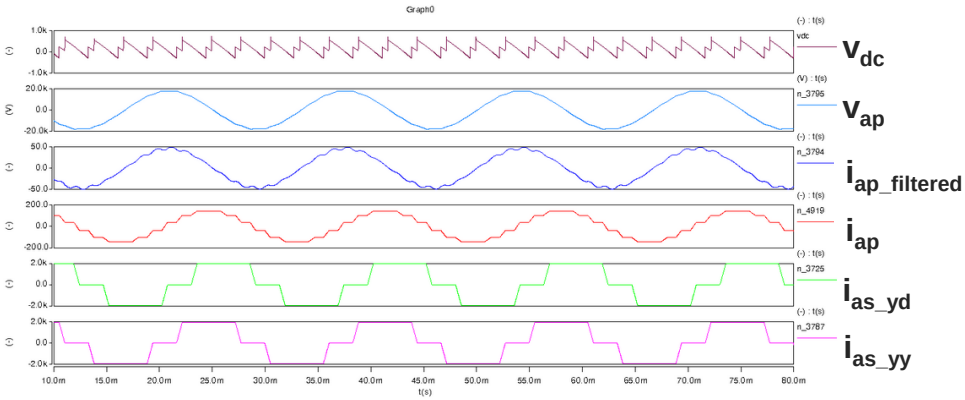
Topology	**12-pulse thyristor rectifier**	**Current source rectifier**	
		Traditional	**New**
Output Power	3.2 MW		
Input Primary Voltage	22 kVrms (line to line), 60 Hz		
Input Secondary Voltage	750 Vrms (line to line), 60 Hz		
Input Secondary Current	1240 Arms each phase each converter		
Output DC Current	3900 A		
Output Voltage	180 – 820 V		
Modulation Index	0.2 - 0.9		
PCC Power Factor	> 0.95		
PCC Current THD	< 5%		
PCC Voltage THD	< 2%		
Operating Temperature	50˚C		
Junction Temperature	125˚C		

The simulation waveforms of the 12-pulse thyristor rectifier are shown in Fig. 4-2. In Fig. 4-2(a), the modulation index is 0.9, the output voltage is 820 V, the firing angle is 34˚, and the output power is 3.2 MW (1 p.u.). The output voltage has sixth order harmonic. With the interleaved rectifiers, the harmonics can be largely reduced in the primary-side current i_{ap}. The harmonic filter can be added on the primary side of the transformer to reduce the total harmonic distortion (THD) and increase the power factor at PCC. But the power factor on the secondary side is only 0.81, indicating large amount of reactive power circulating in the transformer and rectifiers.

When the modulation index is 0.2, the output voltage is 180 V, the firing angle increases to 77˚ and the output power is 0.7 MW (0.22 p.u.) in Fig. 4-2(b). The power factor drops to only 0.17 on the secondary side of the transformer.



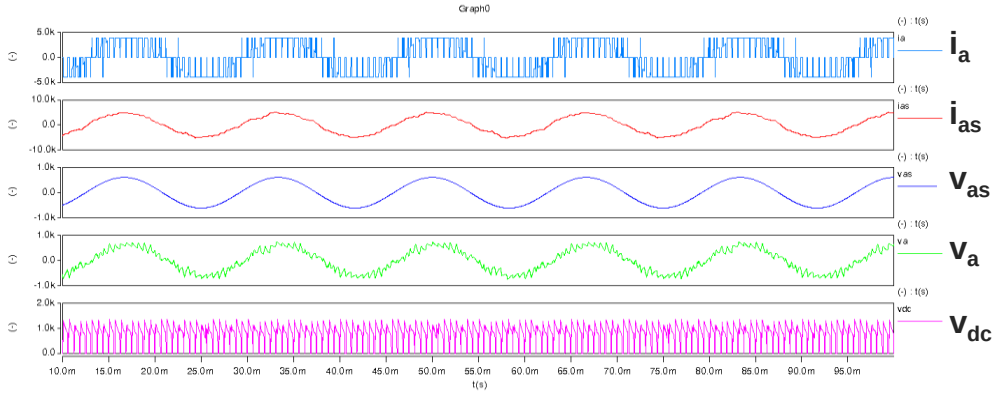
(a)



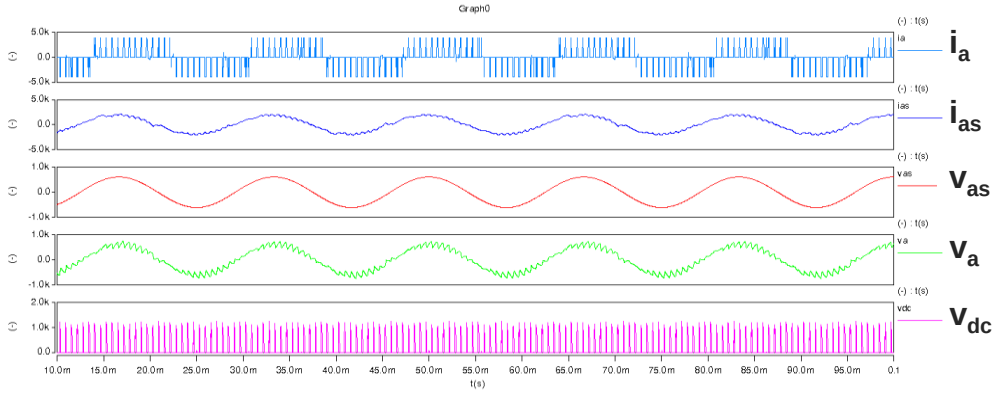
(b)

Fig. 4-2. Simulation waveforms of 12-pulse thyristor rectifier: (a) M = 0.9, Vdc = 820 V; (b) M = 0.2, Vdc = 180 V.

The simulation waveforms are shown in Fig. 4-3 for the PWM current source rectifiers. As shown in Fig. 4-3(a), the dc output voltage is in PWM shape with 1.6 kHz switching frequency. The harmonics can be easily filtered out with small dc-side filter. The current and voltage are in sinusoidal shape with small ac capacitors (0.1 p.u.). The power factor is 0.95 on both primary and secondary sides of the transformer.



(a)



(b)

Fig. 4-3. Simulation waveforms of current source rectifiers: (a) M = 0.9, Vdc = 820 V; (b) M = 0.2, Vdc = 180 V.

When the modulation index is reduced to 0.2 in Fig. 4-3(b), the power factor can be kept at 0.95 with reactive power control in the current source rectifiers.

In the 12-pulse thyristor rectifier, the phase control thyristor from ABB (5STP 30H1801, 1800 V/3108 A) is applied for each switch. The HiPak IGBT modules from ABB (5SNA 3600E170300, 1700 V/3600 A), as well as HiPak diode module from ABB (5SLA 3600E170300, 1700 V/3600 A), are connected in series as switches in the current source rectifiers. The device loss is listed in Table 4-2 for three different topologies. The switching frequency is 1.6 kHz for

the current source rectifiers to reach 99% converter efficiency. Without series-connected devices, the 12-pulse thyristor rectifier has much lower conduction loss than the current source rectifiers. The new current source rectifier has lower conduction loss than the traditional one.

The transformer and filter ratings are listed in Table 4-3. Since the 12-pulse thyristor rectifier generates much reactive power when the firing angle deviates from 0, its transformer rating is higher than that of CSRs and more capacitors are needed to compensate the power factor.

Table 4-2. Semiconductor loss comparison

Topology	Conduction loss	Switching loss	Total loss	Condition
12-pulse thyristor rectifier	8541 W (0.003 p.u.)	0	8541 W (0.003 p.u.)	M = 0.9 Pout = 3.2 MW (1 p.u.)
Traditional CSR	24628 W (0.008 p.u.)	7333 W (0.002 p.u. fs = 1600 Hz)	31961 W (0.01 p.u.)	
New CSR	19703 W (0.006 p.u.)	7333 W (0.002 p.u. fs = 1600 Hz)	27036 W (0.008 p.u.)	

Table 4-3. Transformer and filter rating comparison

Topology	Transformer rating	Filter rating
12-pulse thyristor rectifier	4.0 MVA (1.25 p.u.)	3.3 MVA (1.03 p.u.)
Traditional CSR	3.2 MVA (1 p.u.)	0.32 MVA (0.1 p.u.)
New CSR	3.2 MVA (1 p.u.)	0.32 MVA (0.1 p.u.)

Table 4-4. 4.0 MVA transformer loss in 12-pulse thyristor rectifier

Parameter	Value	Parameter	Value
Primary winding resistance	0.3954 Ω/phase	**Primary rated current**	105.0 A
Secondary winding 1 resistance	0.004893 Ω/phase	**Secondary rated current**	1540 A
Secondary winding 2 resistance	0.001631 Ω/phase	**Core loss**	3040 W
Primary rms current	105.6 A	**Secondary rms current**	1592 A
Primary eddy loss harmonic factor	2.862	**Secondary eddy loss harmonic factor**	5.600
Primary stray loss harmonic factor	1.083	**Secondary stray loss harmonic factor**	1.333
DC resistance loss	29220 W	**Eddy current loss**	13093 W
Other stray loss	3020 W	**Total loss**	48373 W (0.015 p.u.)

Table 4-5. 3.2 MVA transformer loss in CSRs

Parameter	Value	Parameter	Value
Primary winding resistance	0.4943 Ω/phase	**Primary rated current**	83.98 A
Secondary winding resistance	0.003059 Ω/phase	**Secondary rated current**	2464 A
		Core loss	2432 W
Primary rms current	84.09 A	**Secondary rms current**	2467 A
Primary eddy loss harmonic factor	1.3455	**Secondary eddy loss harmonic factor**	1.3455
Primary stray loss harmonic factor	1.0153	**Secondary stray loss harmonic factor**	1.0153
DC resistance loss	22114 W	**Eddy current loss**	2658 W
Other stray loss	2472 W	**Total loss**	29676 W (0.009 p.u.)

Based on the method proposed in IEEE Standard C57.18.10-1998, the transformer loss can be calculated, including dc resistance loss of windings, eddy current loss, core loss and other stray loss. The calculated transformer loss of the 12-pulse thyristor rectifier and the CSR are listed in Table 4-4 and Table 4-5 respectively. Because of lower harmonics and less reactive current, the transformer in CSRs has much lower loss than the one in 12-pulse thyristor rectifier.

The transformer loss and the semiconductor device loss are two main parts in the high power rectifiers. They are calculated in Table 4-6 and drawn in Fig. 4-4. The CSRs have higher device loss but lower transformer loss. The new CSR has comparable efficiency with the 12-pulse SCR rectifier. Considering larger power rating of the transformer and filter, the 12-pulse SCR rectifier will have lower power density than the CSRs.

Table 4-6. Transformer loss and semiconductor device loss comparison

Topology	Transformer loss	Device loss	Total loss and efficiency
12-pulse SCR rectifier	48373 W (0.015 p.u.)	8541 W (0.003 p.u.)	56914 W 98.22 %
Traditional CSR	29676 W (0.008 p.u.)	29923 W (0.009 p.u.)	59599 W 98.14 %
New CSR	29676 W (0.008 p.u.)	27036 W (0.008 p.u.)	56712 W 98.23 %

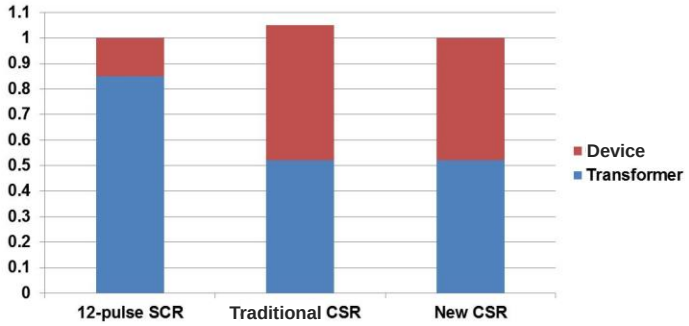


Fig. 4-4. Loss comparison chart for high power rectifiers.

4.2 Power Supply for Data Center

The architecture of the power supply system is shown in Fig. 4-5 for the next-generation data center. The active front end needs to step down three-phase 480 Vac to 400 Vdc. Instead of two-stage voltage source converter, the current source rectifiers can realize this function in a single stage, which has potential to increase the efficiency.

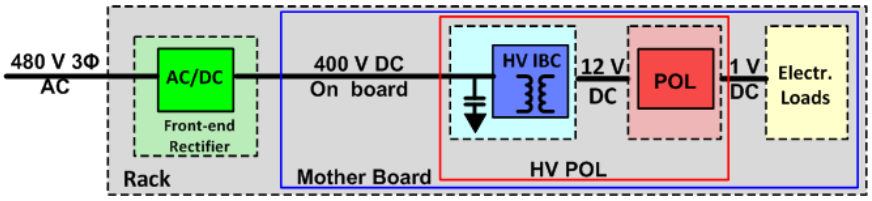
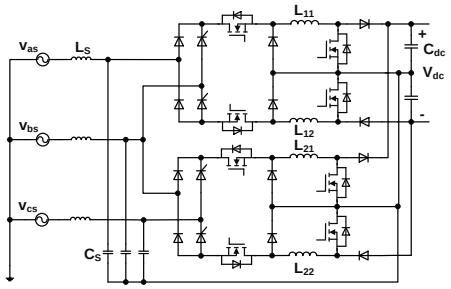
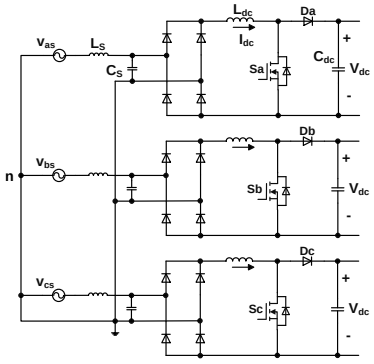


Fig. 4-5. Architecture of the power supply in data center.

The predominant topologies in the market are phase-modular rectifiers shown in Fig. 4-6(a) and Fig. 4-6(b), which is formed with two or three single phase rectifiers. The topology in Fig. 4-6(a) is proposed by Delta Electronics and applied as active front end in the next-generation data center of IBM. The topology in Fig. 4-6(b) is constituted by three single-phase boost rectifiers, which is widely applied in traditional data center power supply.



(a)



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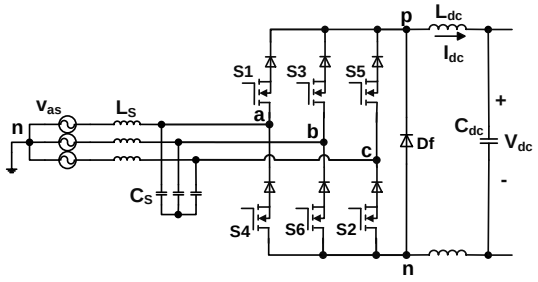
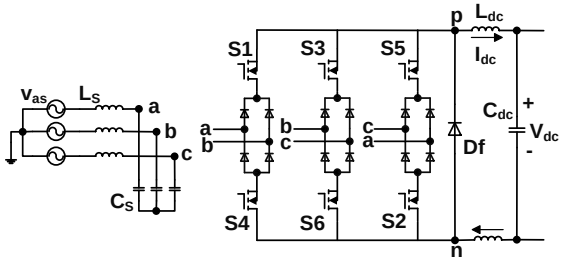


(c)



(d)

Fig. 4-6. Topologies for data center power supply: (a) Three-phase buck-boost rectifier; (b) Three single-phase boost rectifiers; (c) Traditional CSR; (d) New CSR.

Table 4-7. Topology cons and pros

Topology	Phase-modular rectifier		Three-phase CSRs
	Buck-boost	Boost	
Three-phase load balance			
Device voltage stress			
Output/input voltage range			
Control complexity			
Device loss			
Dc capacitor size			

The traditional and new current source rectifiers are drawn in Fig. 4-6(c) and Fig. 4-6(d) respectively. The four topologies have their cons and pros, which are listed in Table 4-7. Although the three-phase buck-boost rectifier has wide output/input voltage range, it has more control complexity and device loss (more devices in series). Three single-phase boost rectifiers will have large neutral current under unbalanced three-phase load. The dc capacitor size is larger in phase-modular rectifiers since they have to filter out low-frequency harmonics on the dc side. The device voltage stress is larger in CSRs. The specification of the designed rectifier is listed in Table 4-8.

Table 4-8. Front-end rectifier specification

Topology	**Phase-modular rectifier**		**Current source rectifier**	
	Buck-boost	**Boost**	**Traditional**	**New**
Output Power	15 kW			
Input Voltage	480 Vrms (line to line), 60 Hz			
Input Current	18 Arms			
Output Voltage	400 Vdc			
Output Current	37.5 A			
Output Voltage Ripple	< 5%			
Input Power Factor	> 0.99			
Input Current THD	< 5%			
Operating Temperature	50˚C			
EMC Standard	EN55022 ClassB			

All the four topologies are modeled and simulated. The simulation waveforms are shown in Fig. 4-7 for three-phase buck-boost rectifier. The current in the boost inductor is not constant and much low-frequency current is filtered out by dc capacitor.

The simulation waveforms are shown in Fig. 4-8 for the single-phase boost rectifier. Three of them can constitute a three-phase rectifier. The output voltage has second-order voltage ripple. The simulation waveforms are shown in Fig. 4-9 for the current source rectifiers.

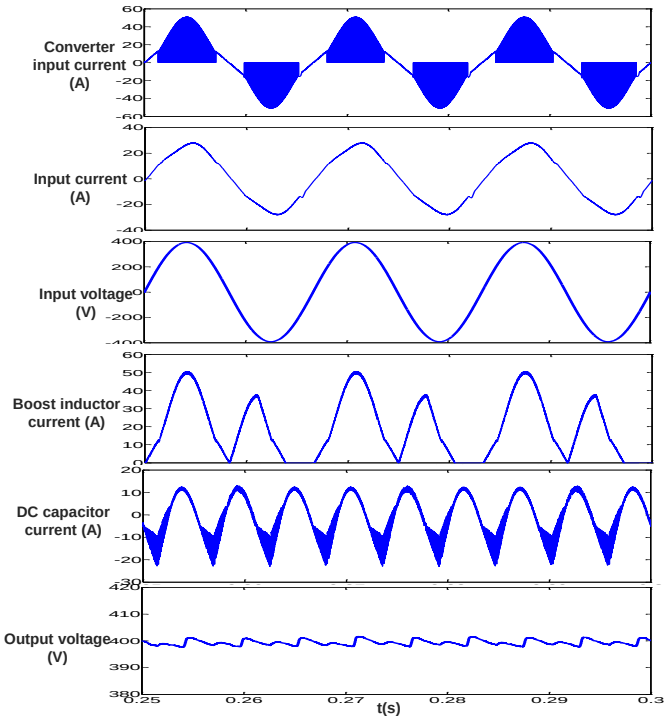


Fig. 4-7. Simulation waveforms of three-phase buck-boost rectifier.

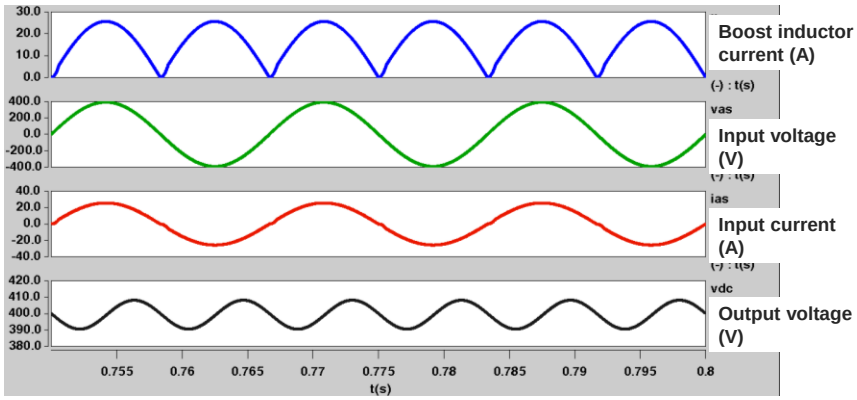


Fig. 4-8. Simulation waveforms of single-phase boost rectifier.

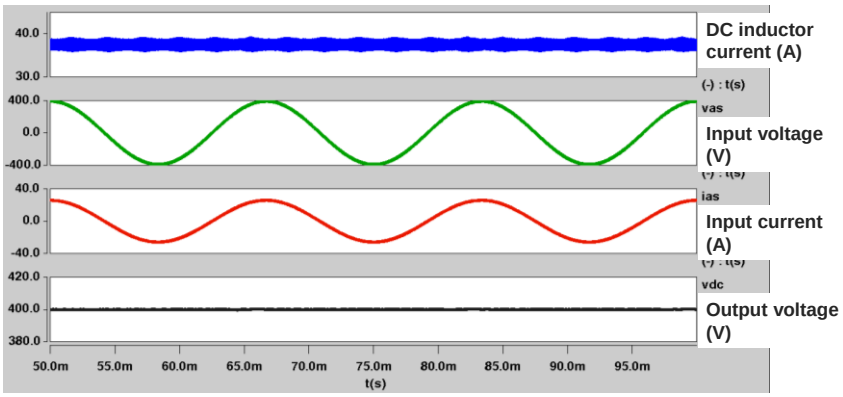


Fig. 4-9. Simulation waveforms of current source rectifier.

The primary design goal for the power supply is high efficiency. SiC devices are applied as switches and paralleled to reduce the conduction loss. As shown in Fig. 4-10, the device conduction loss can be calculated with different number of devices in parallel. Six SiC JFETs and six SiC diodes are paralleled in the current source rectifiers.

Another design variable is the switching frequency. The rectifier is designed under different switching frequency for high efficiency, as shown in Fig. 4-11. The size and loss of the filter decrease as the switching frequency increases in the rectifier. But the switching loss will increase. 28 kHz switching frequency is selected for the current source rectifiers. The design results are shown in Fig. 4-12.

Similarly, the other three topologies can be designed. The loss and solid volume of four topologies are compared in Fig. 4-13. The current source rectifiers have lower loss and solid volume. The new CSR has similar loss and volume with the traditional one. But its total device rating is much lower, indicating fewer devices are needed in it, as shown in Fig. 4-14.

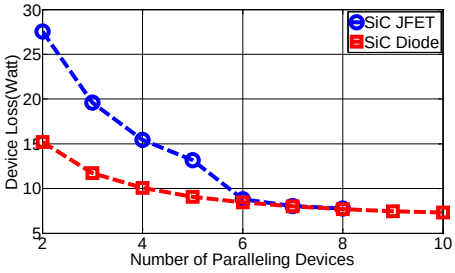


Fig. 4-10. Conduction loss vs. device number.

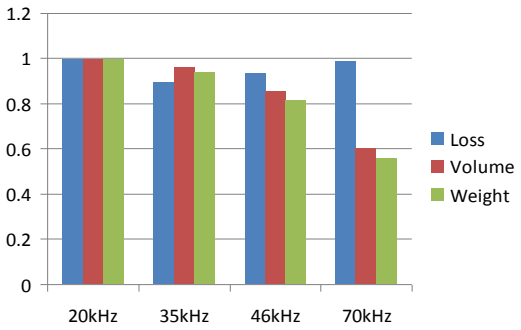


Fig. 4-11. Design under different switching frequencies.

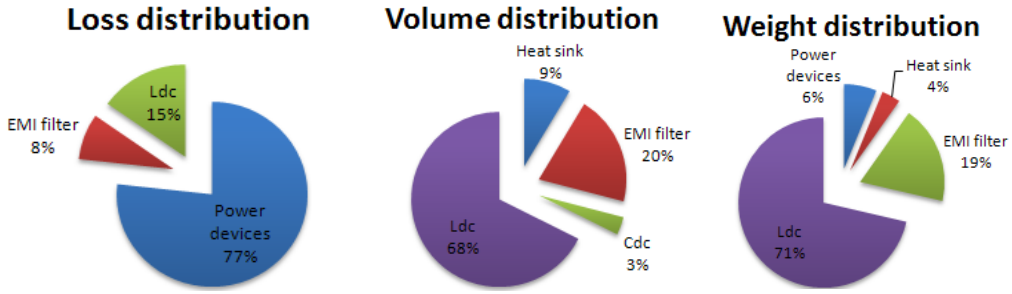


Fig. 4-12. Design results for traditional current source rectifier.

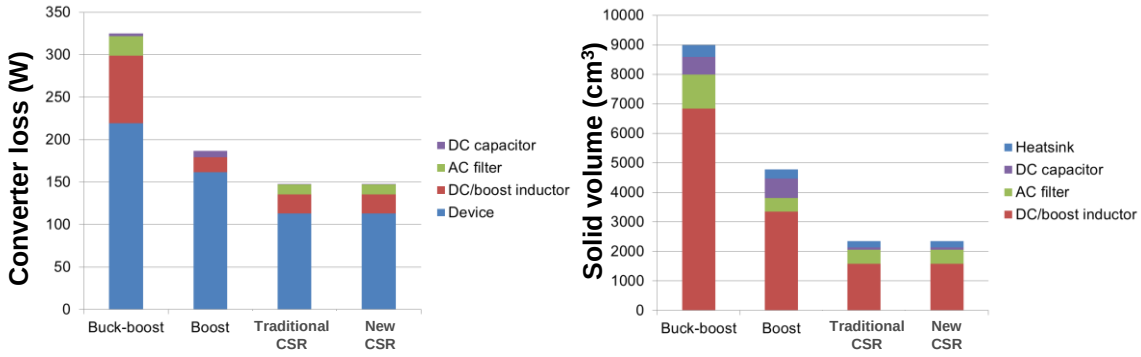


Fig. 4-13. Loss and solid volume comparison of four topologies.

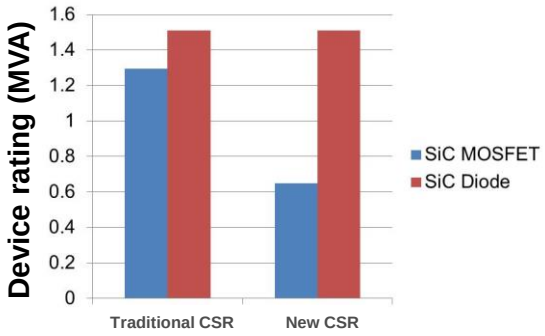


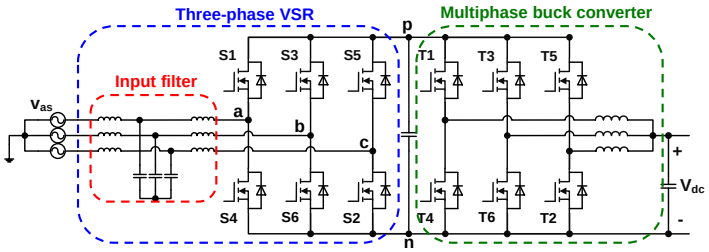
Fig. 4-14. Total device rating comparison.

4.3 Dc Fast Charger for EVs

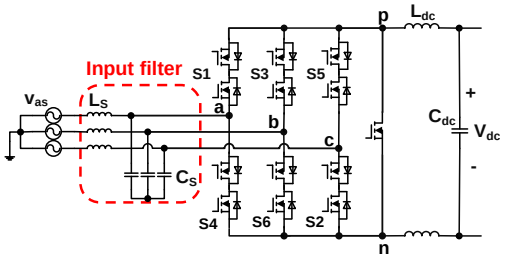
For off-board dc fast EV charger (Level 3), the input three-phase voltage needs to be stepped down to charge the battery in EVs. With traditional voltage source converters, the input voltage is boosted in the first stage and then stepped down in the second stage, leading to higher converter loss. With the three-phase current source rectifiers, this function can be easily realized in a single stage. In this part, the CSRs are compared with two-stage voltage source converter (VSC) for fast EV charger application.

Three topologies under comparison are shown in Fig. 4-15, including the two-stage VSC (three-phase voltage source rectifier + multiphase buck converter) in Fig. 4-15(a), the traditional

CSR in Fig. 4-15(b), and the new CSR in Fig. 4-15(c). Energy can be transmitted bidirectional in these topologies. In this section, three topologies are compared under certain constraints first. Then a multi-objective design method is proposed and the comparison is generalized under different constraints and design goals. The specification of the designed system is shown in Table 4-9.



(a)



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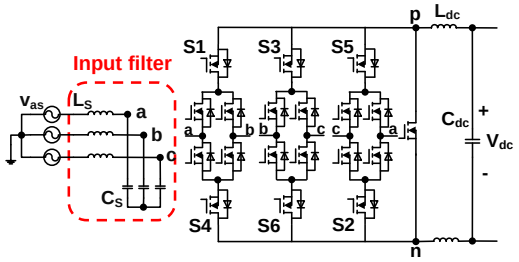


(c)

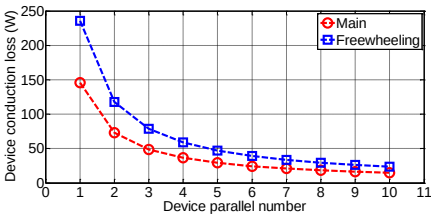
Fig. 4-15. Topologies for fast EV charger: (a) Two-stage VSC; (b) Traditional CSR; (c) DCSR.

Table 4-9. EV charger specification

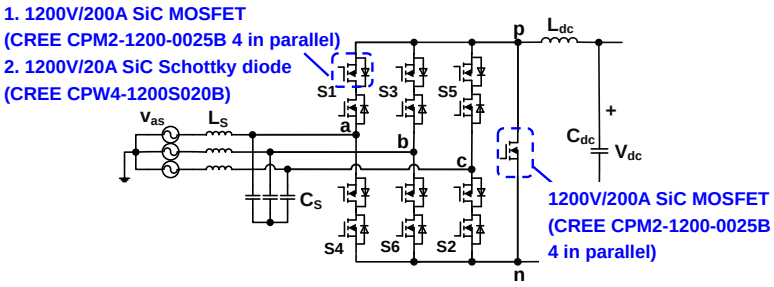
Topology	**Two-stage VSC**	**Current source rectifier**	
		Traditional	**New**
Max Output Power	50 kW		
Input Voltage	480 Vrms (line to line), 60 Hz		
Max Input Current	60 Arms		
Output Voltage	50 - 500 Vdc		
Max Output Current	125 A		
Output Voltage Ripple	< 0.5 V		
Input Power Factor	> 0.99		
Power Efficiency	> 98%		
Input Current THD	< 5%		
Operating Temperature	-10 - 50˚C		

4.3.1 An Example

In this design, the semiconductor device loss is 600 W for all three topologies. 1200V SiC MOSFET CPM2-1200-0025B and 1200 V SiC Schottky diode CPW4-1200S020B from CREE are applied in three topologies. To reduce the conduction loss, several devices can be paralleled in the design. The number of the paralleled devices can be selected based on the conduction loss curve, as shown in Fig. 4-16(a). According to this curve, 4 SiC MOSFETs are paralleled in the main and freewheeling switches, as shown in Fig. 4-16(b). Similar method is applied in the other two topologies, as shown in Fig. 4-17 and Fig. 4-18.

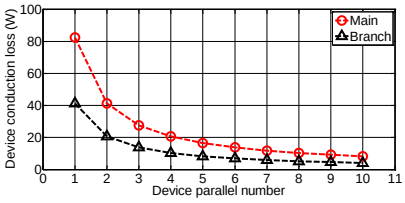


(a)

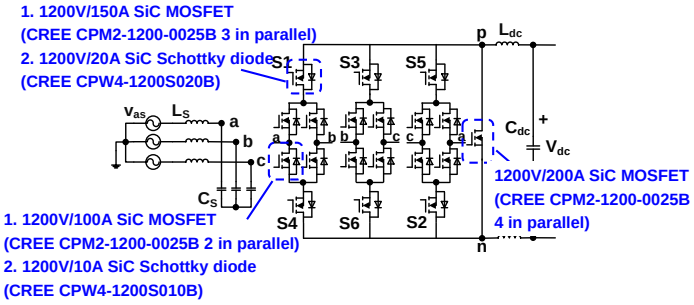


(b)

Fig. 4-16. Device selection in traditional CSR: (a) Conduction loss curve; (b) Device selection.

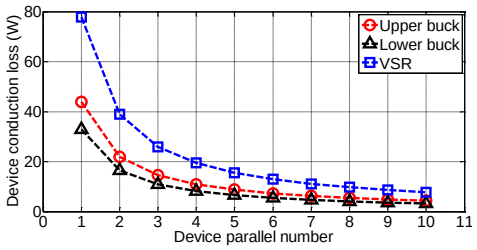


(a)

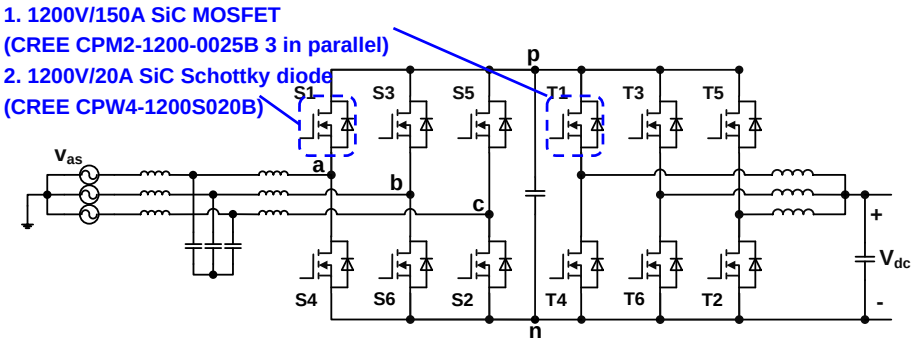


(b)

Fig. 4-17. Device selection in new CSR: (a) Conduction loss curve; (b) Device selection.



(a)



(b)

Fig. 4-18. Device selection in two-stage VSC: (a) Conduction loss curve; (b) Device selection.

Based on the selected devices, the conduction loss can be calculated. The switching frequency is selected for each topology to make the total device loss less than 600 W. The junction temperature is assumed to be 150℃ and the air flow is at 2 m/s for cooling. The extrusion heatsink 83250 from Aavid is used to cool the devices. The power stage designs are compared in Table 4-10 for three topologies, where $R_{th,sa}$ is the thermal resistance from heatsink to ambient. The conduction loss of two-stage VSC is much lower than that of CSRs. Compared with the traditional CSR, the new CSR has lower conduction loss and smaller die area.

The dc side filter includes the dc inductor and dc capacitor. The current ripple in the dc inductor is assumed to be 25 A (20% full load current). The peak current ripple appears when the output voltage is between 300 V and 400 V. The dc inductance needs to limit the current ripple under variable output voltage, as shown in Fig. 4-19.

Table 4-10. Power stage design comparison

Topology	Traditional CSR	New CSR	Two-stage VSC
Total conduction loss	496 W	471 W	233 W
MOSFET die area	1352 mm^2	1196 mm^2	936 mm^2
Switching frequency	24 kHz	30 kHz	VSR 80 kHz Buck 26.7 kHz
Total switching loss	104 W	129 W	367 W
Total device loss	600 W	600 W	600 W
$R_{th,sa}$ of heatsink	0.150℃/W	0.148℃/W	0.146℃/W

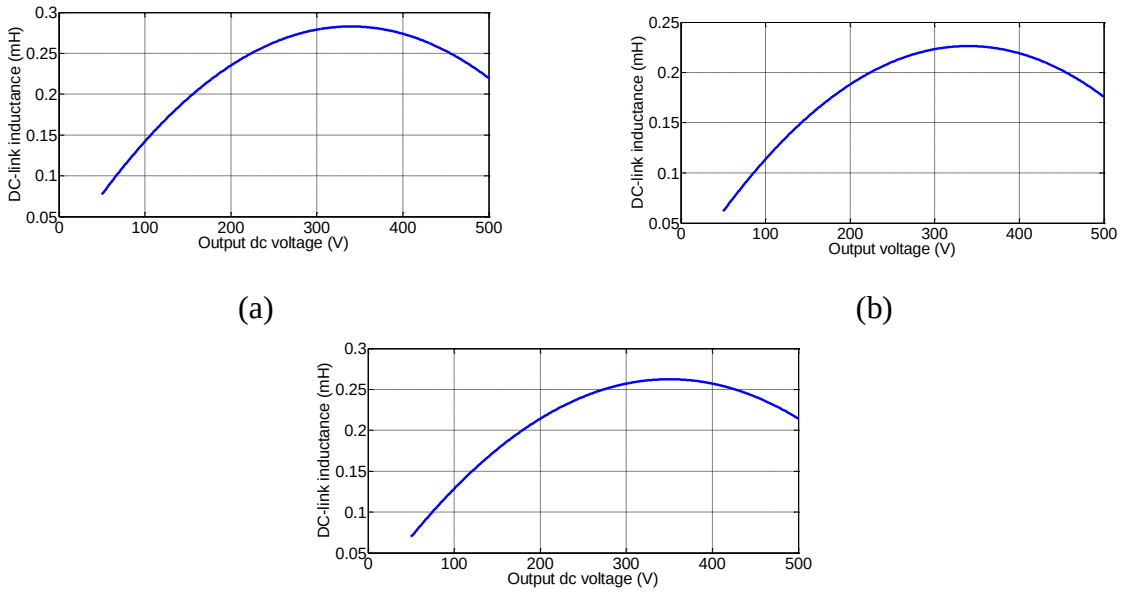


Fig. 4-19. Dc inductance requirement: (a) Traditional CSR; (b) New CSR; (c) Two-stage VSC.

The dc capacitor is selected to limit the output voltage ripple less than 0.5 V. For the two-stage VSC, the intermediate capacitor between two stages is designed to make the cascaded system stable. The designs of the dc filter are compared in Table 4-11 for three topologies.

Table 4-11. Dc filter design comparison

Topology	Traditional CSR	New CSR	Two-stage VSC
DC inductor	283 μH	226 μH	263 μH for each phase
DC capacitor	260 μF@500Vdc	208 μF@500Vdc	78 μF@500Vdc
Intermediate capacitor	-	-	32 μF@700Vdc
Total loss	135 W	88 W	160 W
Total volume	3131 cm^3	2847 cm^3	2751 cm^3

The ac filter is used to filter out the harmonics and keep the total harmonic distortion (THD) of the input current less than 5%. For CSRs, the ac capacitor is selected to limit the reactive power less than 5%. The input voltage ripple should be limited to be less than 15% for normal operation. For two-stage VSC, the input boost inductor is selected based on THD requirement. The grid inductance is assumed to be 10 μH. The designs of the ac filter are compared in Table 4-12.

Table 4-12. Ac filter design comparison

Topology	Traditional CSR	New CSR	Two-stage VSC
AC inductor	-	-	200 μH each phase
AC capacitor	20 μF each phase	16 μF each phase	-
Total loss	12 W	12 W	73 W
Total volume	396 cm^3	396 cm^3	2601 cm^3

The simulation waveforms of three topologies are shown in Fig. 4-20, Fig. 4-21 and Fig. 4-22. The converters work well with the designed filters, meeting the specification in Table 4-9.

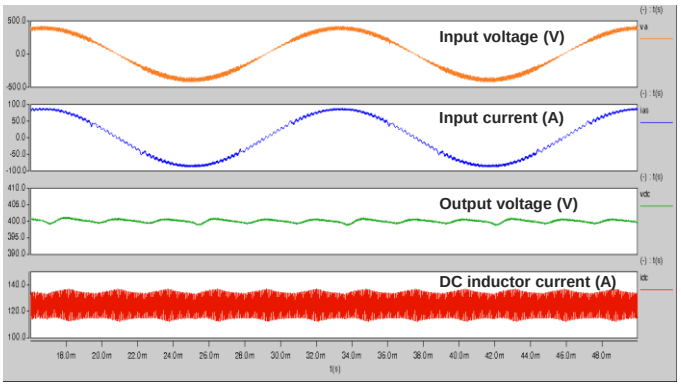


Fig. 4-20. Simulation waveforms of traditional CSR.

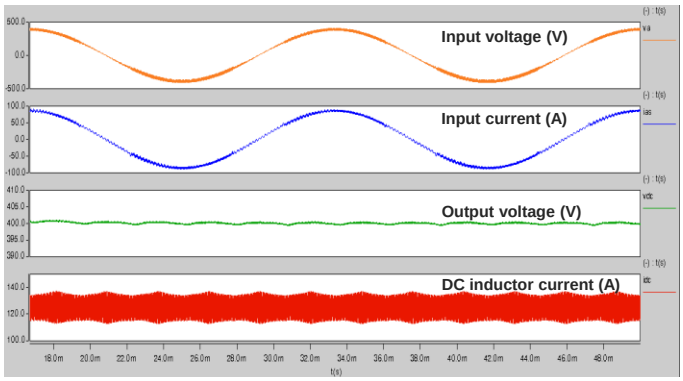


Fig. 4-21. Simulation waveforms of new CSR.

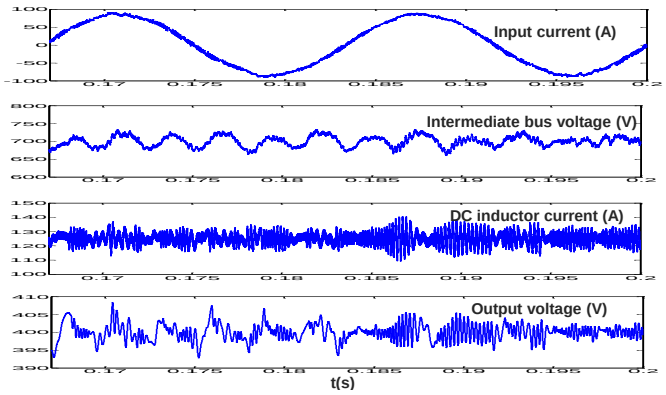


Fig. 4-22. Simulation waveforms of two-stage VSC.

The converter loss breakdown is shown in Table 4-13 and Fig. 4-23. The converter volume breakdown is shown in Table 4-14 and Fig. 4-24. The two-stage VSC has much lower

conduction loss than the CSRs. But its large boost inductor has much loss and volume. The new CSR has the highest efficiency and power density in this comparison.

Table 4-13. Loss breakdown

Topology	Traditional CSR	New CSR	Two-stage VSC
Device conduction	496 W	471 W	233 W
Device switching	104 W	129 W	367 W
DC inductor	135 W	88 W	157 W
Intermediate capacitor	-	-	3 W
AC inductor	-	-	73 W
AC capacitor	12 W	12 W	-
Total	747 W	700 W	833 W

Table 4-14. Volume breakdown

Topology	Traditional CSR	New CSR	Two-stage VSC
Heatsink	945 cm^3	978 cm^3	1011 cm^3
DC capacitor	359 cm^3	311 cm^3	101 cm^3
DC inductor	2772 cm^3	2536 cm^3	2550 cm^3
Intermediate capacitor	-	-	101 cm^3
AC inductor	-	-	2601 cm^3
AC capacitor	396 cm^3	396 cm^3	-
Total	4472 cm^3	4221 cm^3	6364 cm^3

Fig. 4-23. Loss comparison of three topologies.

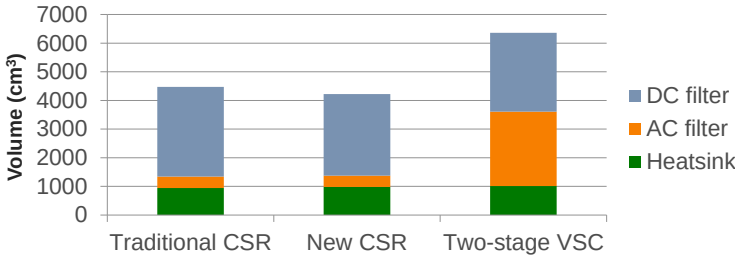


Fig. 4-24. Volume comparison of three topologies.

When the output voltage varies from 50 V to 500 V, the loss and efficiency are compared in Fig. 4-25. The new CSR has higher efficiency than the two-stage VSC when the output voltage is higher than 200 V. When it is lower than 200 V, the switching loss is largely reduced in VSC, leading to higher efficiency in VSC.

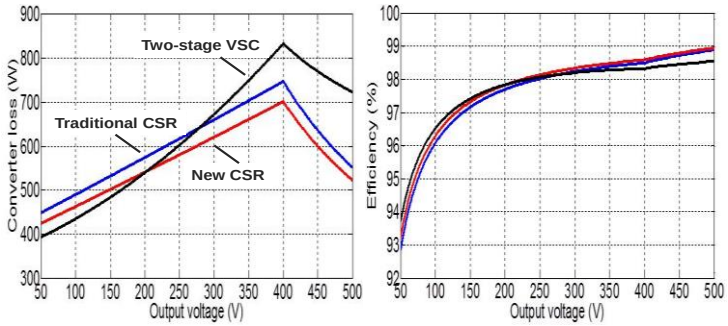


Fig. 4-25. Loss and efficiency under different output voltages.

4.3.2 Multi-Objective Converter Design

The previous comparison is under certain constraints and the conclusions may not be general. To generalize the comparison under other design objectives and constraints, a multi-objective converter design method is proposed in Fig. 4-26. The main performance indices of the converter are the efficiency, the power density and specific power. Two design variables are the semiconductor die area and the switching frequency f_s. Based on the database of commercial products, the capacitor and inductor can be optimized for either high efficiency or high power density.

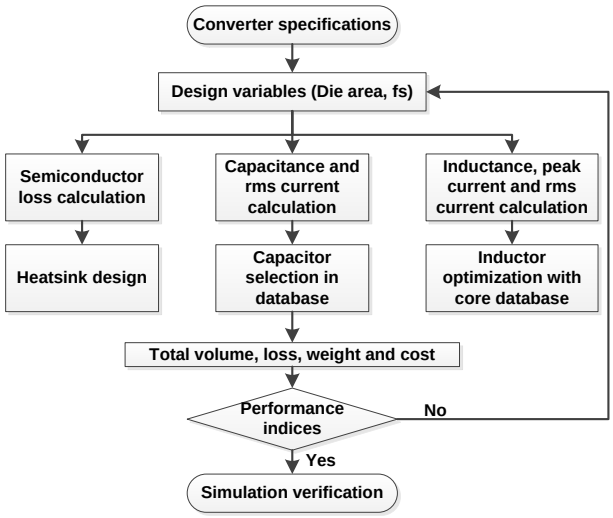


Fig. 4-26. Multi-objective design process.

Given converter specifications and performance indices, the multi-objective design program can automatically optimize the converter design. The whole method is based on the analytic model of the converters derived in previous research work. Without any real-time simulation, the

optimization runs very fast. To demonstrate the design process, three optimizations are carried for different design objectives.

The first optimization is for highest power density. Meanwhile, the converter efficiency should be kept higher than 98%. The device die area is the same in all three topologies. When die area = 1000 mm^2, the converter volume changes with the switching frequency, as shown in Fig. 4-27. For each point in the curve, the converter volume is minimized under corresponding switching frequency. As the switching frequency increases, the filter size decreases while the heatsink size increases. Because of lower conduction loss of VSC, it can be pushed to higher switching frequencies, as shown in Fig. 4-27(c).

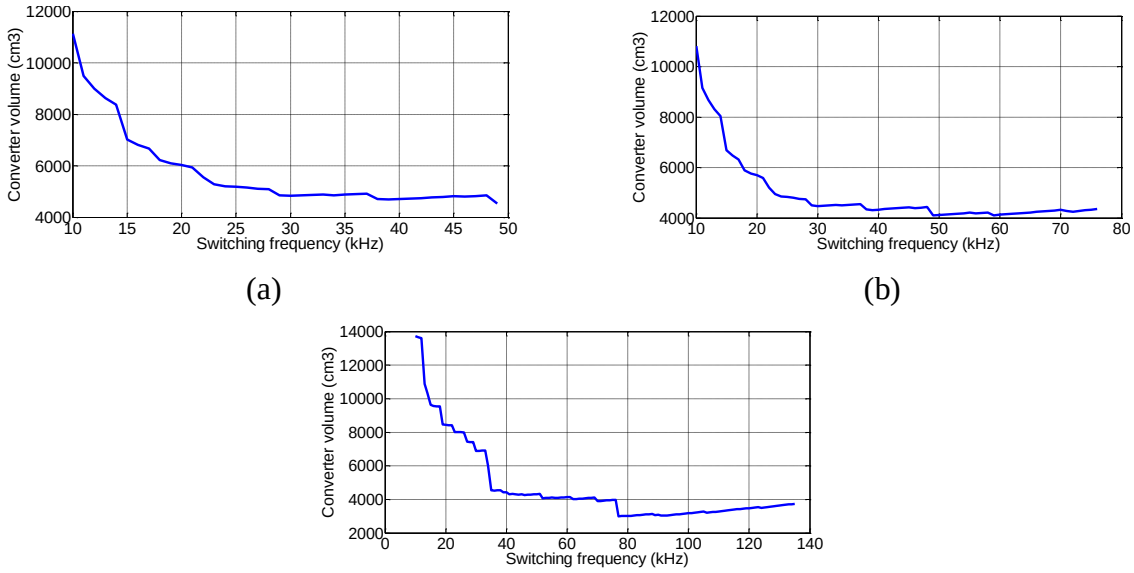


Fig. 4-27. Volume vs. Switching Frequency: (a) Traditional CSR; (b) New CSR; (c) Two-stage VSC.

The designs with minimum volume are listed in Table 4-15. With small device loss, the two-stage VSC saves much on heatsink volume. It has the highest power density in this case. With less conduction loss, the new CSR has smaller heatsink size than traditional CSR.

Table 4-15. Design for minimum volume

Topology	Traditional CSR	New CSR	Two-stage VSC
Heatsink	2224 cm^3	1796 cm^3	934 cm^3
DC capacitor	218 cm^3	218 cm^3	43.5 cm^3
DC inductor	1709 cm^3	1709 cm^3	1545 cm^3
Intermediate capacitor	-	-	100 cm^3
AC inductor	-	-	383 cm^3
AC capacitor	376 cm^3	376 cm^3	-
Total	4527 cm^3	4099 cm^3	3005 cm^3

The comparison can be carried out under different die area. The power density is compared in Fig. 4-28 and the volume breakdown is shown in Fig. 4-29. As the die area increases, the conduction loss becomes closer in three topologies and the heatsink size is reduced. With smaller filter size, the power density of the new CSR is higher than two-stage VSC when die area = 2500 mm^2.

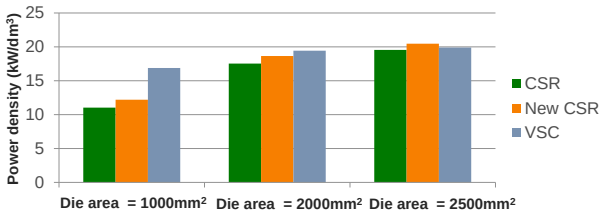


Fig. 4-28. Power density comparison with different die area.

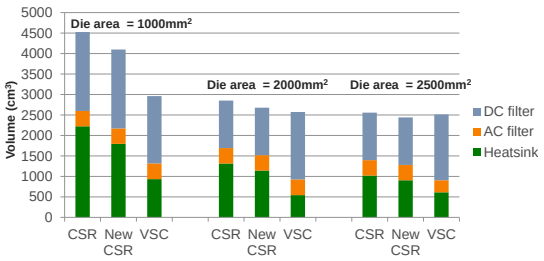
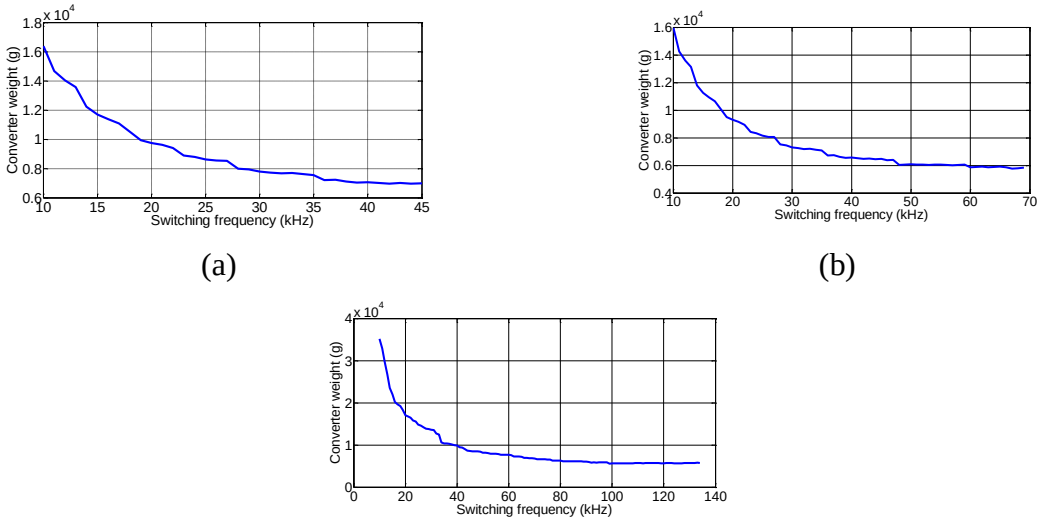


Fig. 4-29. Volume breakdown in the design for high power density.

The second optimization is for highest specific power. Meanwhile, the converter efficiency should be kept higher than 98%. The device die area is the same in all three topologies. When die area = 1000 mm^2, the converter weight changes with the switching frequency, as shown in Fig. 4-30. For each point in the curve, the converter weight is minimized under corresponding switching frequency. As the switching frequency increases, the filter weight decreases while the heatsink weight increases. Because of lower conduction loss of VSC, it can be pushed to higher switching frequency, as shown in Fig. 4-30(c).



(a) (b)

(c)

Fig. 4-30. Weight vs. Switching Frequency: (a) Traditional CSR; (b) New CSR; (c) VSC.

The designs with minimum weight are listed in Table 4-16. The new CSR has comparable specific power with the two-stage VSC. The comparison can be carried out under different die area. The specific power is compared in Fig. 4-31 and the weight breakdown is shown in Fig. 4-32. As the die area increases, the new CSR has higher specific power than the two-stage VSC.

Table 4-16. Design for minimum weight

Topology	Traditional CSR	New CSR	Two-stage VSC
Heatsink	2777 g	2824 g	2658 g
DC capacitor	120 g	80 g	20 g
DC inductor	3892 g	2705 g	2331 g
Intermediate capacitor	-	-	45 g
AC inductor	-	-	704 g
AC capacitor	171 g	171 g	-
Total	6960 g	5779 g	5758 g

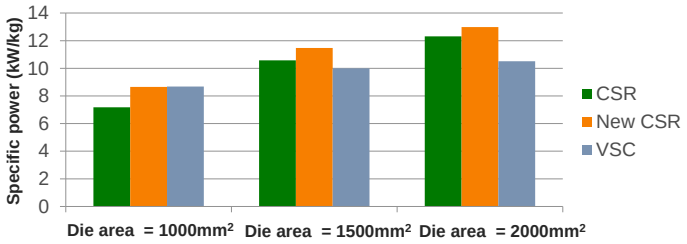


Fig. 4-31. Comparison of specific power with different die area.

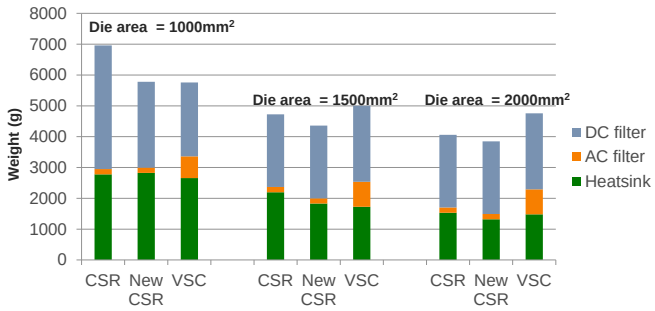


Fig. 4-32. Weight breakdown in the design for high specific power.

The third optimization is for highest efficiency. Meanwhile, the converter weight needs to meet the maximum weight constraint. The devices can be paralleled to reduce the conduction loss. The paralleling number of the device can be selected based on the conduction loss curves in Fig. 4-16(a), Fig. 4-17(a) and Fig. 4-18(a). When the maximum weight is 10 kg, the converter loss changes with the switching frequency, as shown in Fig. 4-33. For each point in the curve, the converter loss is minimized under corresponding switching frequency. As the switching frequency increases, the filter loss decreases while the device loss increases.

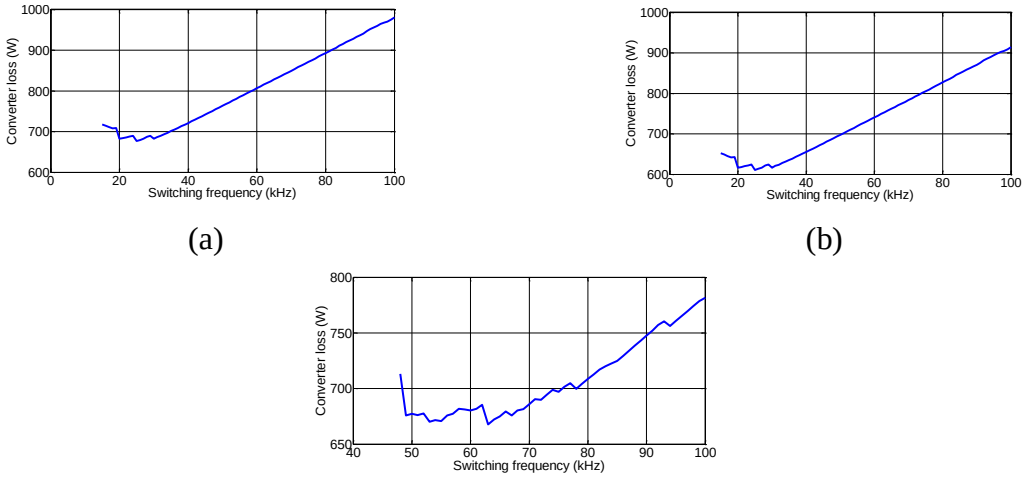


Fig. 4-33. Loss vs. Switching Frequency: (a) Traditional CSR; (b) New CSR; (c) VSC.

The comparison can be carried out under different weight constraints. The efficiency is compared in Fig. 4-34 and the loss breakdown is shown in Fig. 4-35. Without any weight constraint, the VSC has the highest efficiency. But its filter weight is more than 10 times of the one in CSRs in this case. With some weight constraints, the new CSR has the highest efficiency.

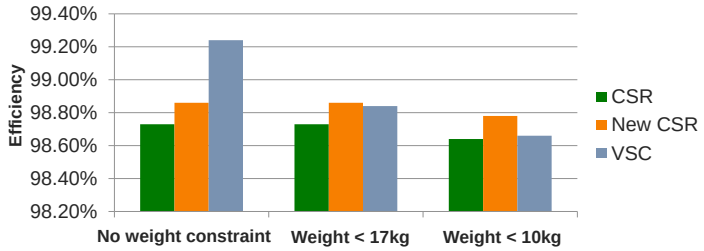


Fig. 4-34. Comparison of efficiency with weight constraints.

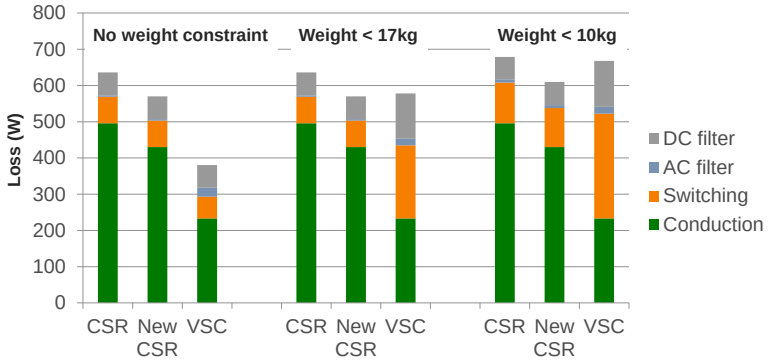


Fig. 4-35. Loss breakdown in the design for high efficiency.

The Pareto front can be drawn for three topologies on the efficiency-power density plane with the proposed design method. As shown in dash lines in Fig. 4-36, each point in the curve indicates an optimized design under corresponding efficiency and power density. Each Pareto front includes two curves. One is the "horizontal" curve, which indicates the maximum efficiency the converter can reach under certain power density constraint. The other is the "vertical" curve, which indicates the maximum power density the converter can reach under

certain efficiency constraint. The area enclosed by these two curves is the design space, which contains all the possible designs for the converter. The spots in Fig. 4-36 indicate the designs in Fig. 4-28 and Fig. 4-29. They are very close to the Pareto front.

When die area = 1000 mm^2, the CSRs has smaller design space than two-stage VSC. When the die area increases to 2000 mm^2, the design spaces of three topologies are comparable. When the die area increases further to 2500 mm^2, the new CSR has the largest design space. The new CSR always has more design space than the traditional one.

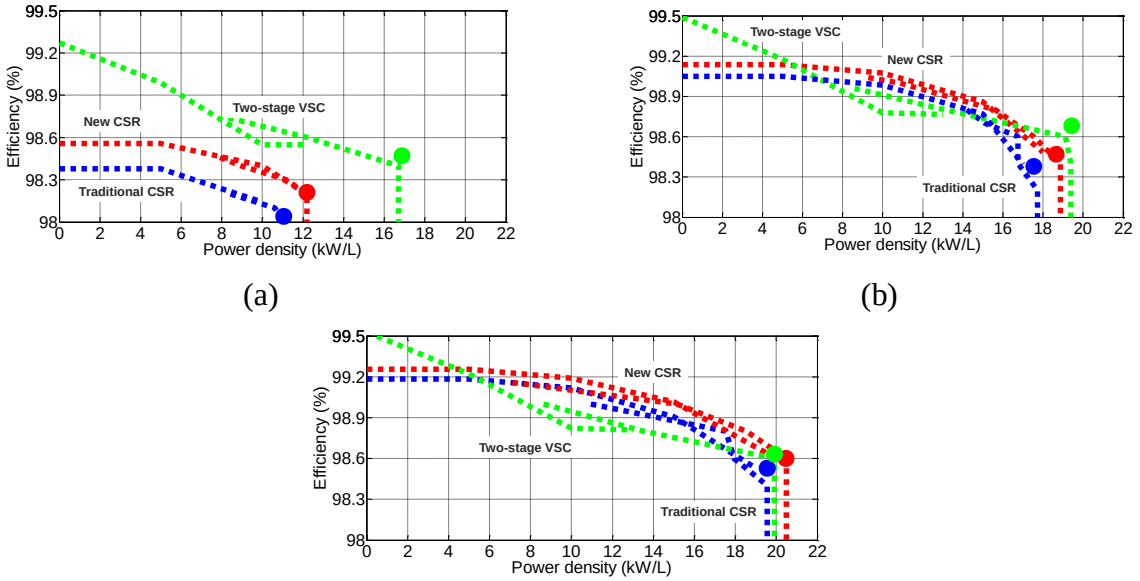


Fig. 4-36. Pareto front in efficiency-power density plane: (a) Die area = 1000 mm^2; (b) Die area = 2000 mm^2; (c) Die area = 2500 mm^2.

4.4 Conclusion

The new CSR has been compared with other predominant topologies on efficiency and power density in high power rectifier, power supply for data center and fast EV charger. It has

comparable efficiency and higher power density than the 12-pulse thyristor rectifier in high power rectifier application. It has higher efficiency than the phase-modular rectifiers in data center power supply. It has higher efficiency and power density than two-stage voltage source converter in fast EV charger when more die area is allowable in the design.

5 All-SiC Power Module for CSRs

5.1 Analysis of Switching Loss in VSR and CSR

The topologies of current source rectifier (CSR) and voltage source rectifier (VSR) are shown in Fig. 5-1 and Fig. 5-2 respectively. The commutation unit in CSR includes the upper or lower three switches, as shown in Fig. 5-1. They commutates with each other under ac voltage and dc current. A diode is usually connected in series with an active device to block the reverse voltage on the switch. The commutation in VSR includes an upper switch and a lower one in a phase leg, as shown in Fig. 5-2. They commutates with each other under dc voltage and ac current. A diode is usually connected in parallel with an active device to conduct the reverse current on the switch.

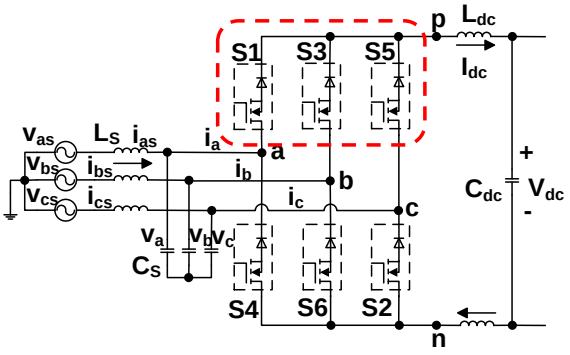


Fig. 5-1. Current source rectifier.

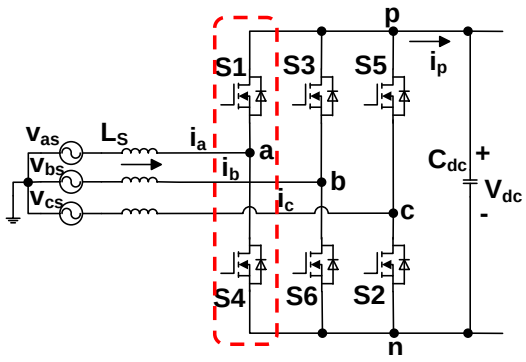


Fig. 5-2. Voltage source rectifier.

To compare the switching loss of CSR and VSR, the switching frequency is assumed to be much higher than the fundamental one. The input voltage is assumed to be sinusoidal and the dc-link current is constant in CSR. The input current is assumed to be sinusoidal and the dc-link voltage is constant in VSR. The switching energy is assumed to be proportional to the product of

the voltage and current at switching moment. The relationship is given by (5-1), where V_{ref} is the voltage at switching moment, I_{ref} the current at switching moment, $E_{VSR\_on\_ref}$ the switching energy in the turn-on process of VSR, $E_{VSR\_off\_ref}$ the switching energy in the turn-off process of VSR, $E_{CSR\_on\_ref}$ the switching energy in the turn-on process of CSR, $E_{CSR\_off\_ref}$ the switching energy in the turn-off process of CSR.

$$k_{VSR\_on} = \frac{E_{VSR\_on\_ref}}{V_{ref}I_{ref}}, k_{VSR\_off} = \frac{E_{VSR\_off\_ref}}{V_{ref}I_{ref}}$$
$$k_{CSR\_on} = \frac{E_{CSR\_on\_ref}}{V_{ref}I_{ref}}, k_{CSR\_off} = \frac{E_{CSR\_off\_ref}}{V_{ref}I_{ref}} \quad (5\text{-}1)$$

In this calculation, the modulation schemes are 60° discontinuous PWM (DPWM) and Modified Fullwave Symmetrical Modulation (MFSM) for VSR and CSR respectively. The switching loss of VSR with 60°DPWM can be given by (5-2), where I_m is the peak input current, V_{dc} the output dc voltage, M_{VSR} the modulation index, V_m the peak input voltage, T_s the switching period.

$$P_{VSR\_switching} = \frac{3I_mV_{dc}\left(k_{VSR\_on} + k_{VSR\_off}\right)}{\pi T_s}, M_{VSR} = \frac{\sqrt{3}V_m}{V_{dc}} \quad (5\text{-}2)$$

The switching loss of CSR with MFSM can be given by (5-3), where I_{dc} is the dc output current, V_{dc} the output dc voltage, M_{CSR} the modulation index, V_m the peak input voltage, φ the phase difference between input voltage and current.

$$P_{CSR\_switching} = \frac{3\sqrt{3}I_{dc}V_m\left(k_{CSR\_on} + k_{CSR\_off}\right)}{\pi T_s}, M_{CSR} = \frac{2V_{dc}}{3V_m cos\varphi} \quad (5\text{-}3)$$

The VSR switching loss in (5-2) is much different from the CSR switching loss in (5-3). To demonstrate their relationship, it is assumed that the modulation index is the same in both VSR and CSR. The switching energy coefficients are the same and input power equals the output power. The assumptions can be given by

$$\begin{aligned} M_{VSR} &= M_{CSR} \\ k_{VSR\_on} + k_{VSR\_off} &= k_{CSR\_on} + k_{CSR\_off} \\ P_{in} = \frac{3}{2} V_m I_m cos\varphi &= P_{out} = V_{dc} I_{dc} \end{aligned} \tag{5-4}$$

Then (5-2) and (5-3) can be simplified and they actually equal with each other, as given by

$$P_{VSR\_switching} = P_{CSR\_switching} \tag{5-5}$$

In practice, the switching energy does not always have linear relationship shown in (5-1). Also the switching energy coefficients may not be the same in VSR and CSR. Because of the difference in commutation loop and device connection, the switching speed and switching energy are different in two topologies. The specification of the design is shown in Table 5-1.

Table 5-1. Converter specification

Topology	**Voltage source rectifier**	**Current source rectifier**
Output Power	10 kW	
Input Voltage	480 Vrms (line to line), 60 Hz	
Input Current	12 Arms each phase	
Modulation Index	0.95	
DC-link	18 A dc-link current	715 V dc-link voltage
Input Power Factor	> 0.99	
AC Harmonics	Input current THD < 5%	

5.2 Simulation with Device Models

The commutation circuits in both VSR and CSR are modeled in Saber to analyze the commutations in them. In the simulation, the device models are 1200 V SiC MOSFET CMF20120D and 1200 V SiC Schottky diode CSD10120 from CREE. As shown in Fig. 5-3, the MOSFET is paralleled with the diode in VSR simulation circuit. Some parasitic inductance is placed in the simulation circuit. As shown in Fig. 5-4, the MOSFET is connected in series with the diode in CSR simulation circuit.

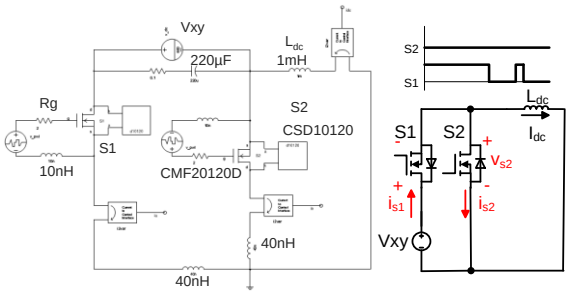


Fig. 5-3. VSR simulation circuit.

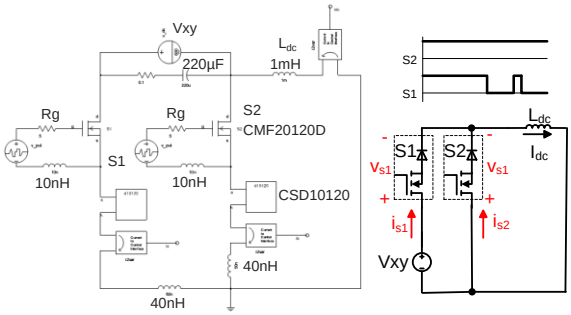
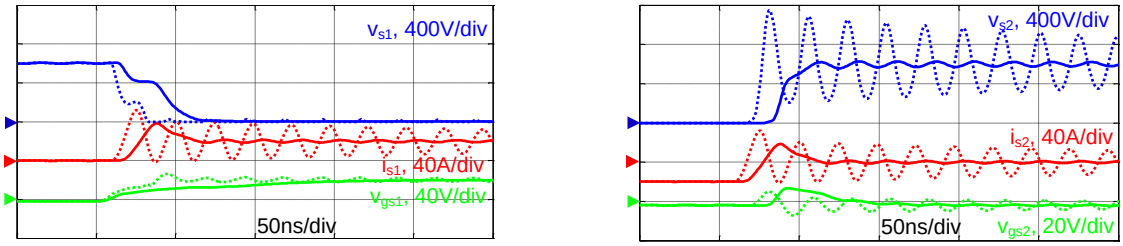


Fig. 5-4. CSR simulation circuit.

In the simulation, the external gate resistor is reduced to increase the switching speed. Two constraints are considered in this process – the voltage on the devices should be lower than 1200 V and the gate voltage of SiC MOSFET is within the range from -5 V to 25 V. According to the simulation results, the minimum external gate resistor is 0.3 Ω for VSR circuit and 0.5 Ω for CSR circuit.

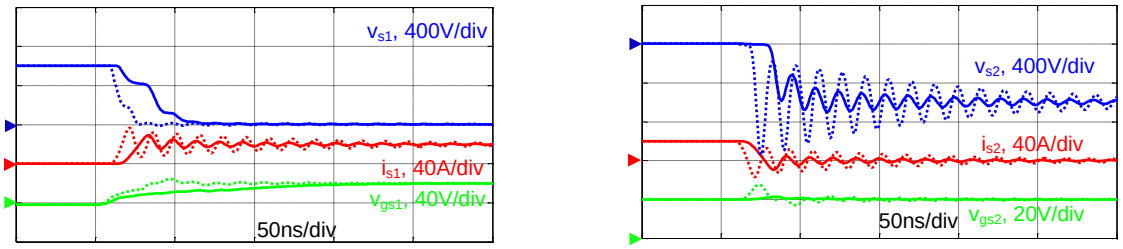
The switching waveforms of VSR are drawn in Fig. 5-5 when S1 is turned on and S2 is turned off. $V_{xy} = 600\,V$ and $I_{dc} = 20\,A$. The dash waveform is got with 0.3 Ω external gate resistor and the solid waveform is got with 10 Ω external gate resistor.

The switching waveforms of CSR are drawn in Fig. 5-6 when S1 is turned on and S2 is turned off. $V_{xy} = 600\,V$ and $I_{dc} = 20\,A$. The dash waveform is got with 0.5 Ω external gate resistor and the solid waveform is got with 10 Ω external gate resistor.



(a) (b)

Fig. 5-5. Switching waveforms of VSR: (a) S1 turn-on waveforms; (b) S2 turn-off waveforms.



(a) (b)

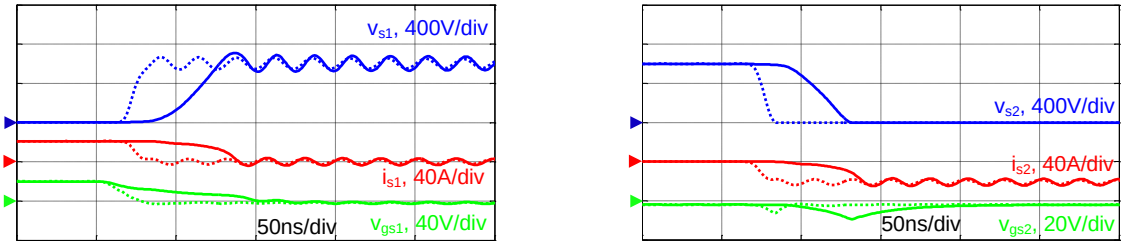
Fig. 5-6. Switching waveforms of CSR: (a) S1 turn-on waveforms; (b) S2 turn-off waveforms.

The resonance in the waveforms is caused by the oscillation between parasitic inductance and the device junction capacitance. The equivalent junction capacitance is lower in CSR because of series connection of devices. So the resonance frequency is higher in CSR. High

voltage spikes appear on S2 in this process. The resonance is damped faster in CSR because of larger on resistance.

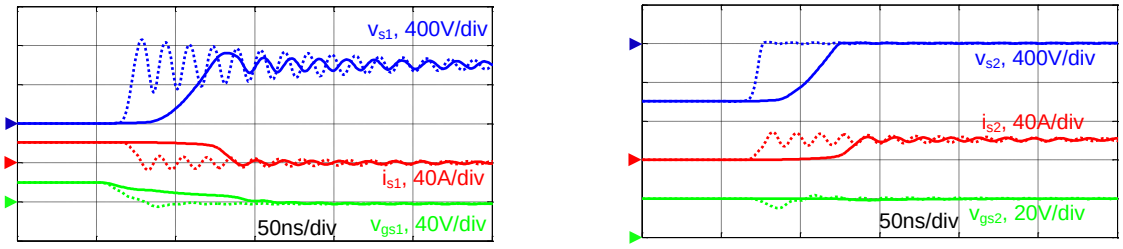
The switching waveforms of CSR are drawn in Fig. 5-7 when S1 is turned off and S2 is turned on. $V_{xy} = 600\,V$ and $I_{dc} = 20\,A$. The dash waveform is got with 0.3 Ω external gate resistor and the solid waveform is got with 10 Ω external gate resistor.

The switching waveforms of CSR are drawn in Fig. 5-8 when S1 is turned off and S2 is turned on. $V_{xy} = 600\,V$ and $I_{dc} = 20\,A$. The dash waveform is got with 0.5 Ω external gate resistor and the solid waveform is got with 10 Ω external gate resistor. The voltage spike appears on S1 when it is turned off. But it is much smaller compared with the one when S2 is turned off. The resonance frequency is also higher in CSR.



(a) (b)

Fig. 5-7. Switching waveforms of VSR: (a) S1 turn-off waveforms; (b) S2 turn-on waveforms.



(a) (b)

Fig. 5-8. Switching waveforms of CSR: (a) S1 turn-off waveforms; (b) S2 turn-on waveforms.

With 0.3 Ω external gate resistor, the switching energy in VSR can be calculated under different operation current, as shown in Fig. 5-9. With 0.5 Ω external gate resistor, the switching energy in CSR can be calculated under different operation voltage, as shown in Fig. 5-10.

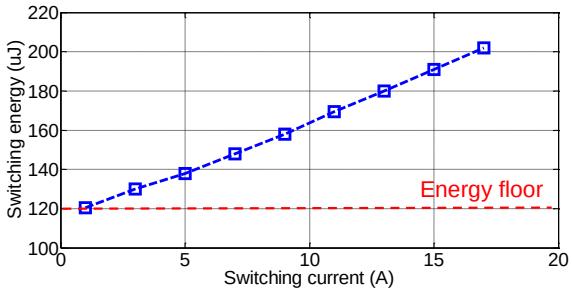


Fig. 5-9. Switching energy in VSR.

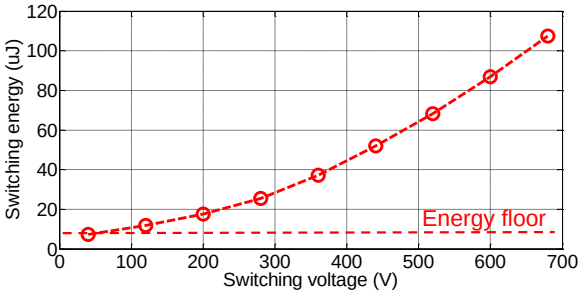


Fig. 5-10. Switching energy in CSR.

The switching loss of the converters can be calculated with the switching energy curves. The calculation is based on simulation, as shown in Fig. 5-11. The device voltage, current and gate signal waveforms are collected through converter simulation. The turn-on and turn-off processes can be judged through gate signals. The switching energy at each switching moment is summed to get the total switching loss. The calculated switching loss of CSR is 2.64 W, much lower than the VSR switching loss 15.36 W.

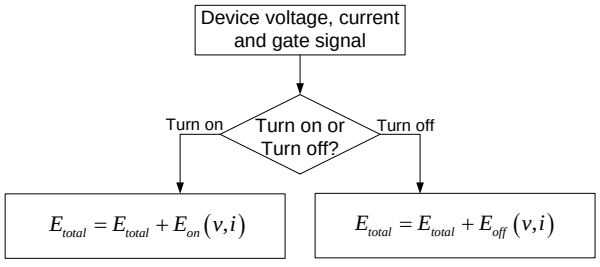


Fig. 5-11. Switching loss calculation process.

5.3 Analysis of Parasitic Loss

To understand the switching energy difference under high switching speed, the commutation circuits in VSR and CSR are simplified in Fig. 5-12 and Fig. 5-13 respectively. The MOSFET is modeled as a channel with three junction capacitors. The diode is modeled as an ideal diode paralleled with a junction capacitor.

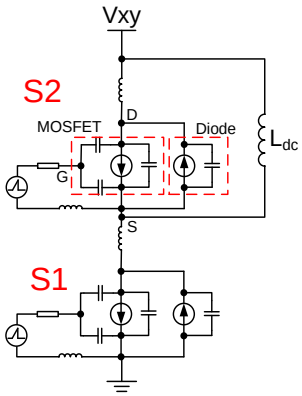


Fig. 5-12. Simplified commutation circuit in VSR.

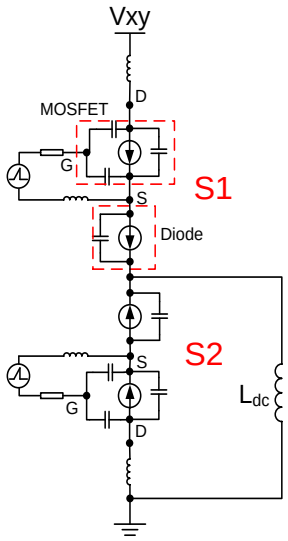


Fig. 5-13. Simplified commutation circuit in CSR.

The switching energy can be divided into two parts. One is the semiconductor loss, which is generated in the process to build up the channel and transmit the electrons. This part of loss can be reduced by increasing the switching speed with lower gate resistor. It is proportional to the operating voltage and current.

The other one is the parasitic loss, which is decided by the energy stored in parasitic capacitance and inductance in the commutation circuit. This part of loss can not be reduced with

small gate resistor. As the switching speed increases, it plays more and more important role in total switching loss.

Since the same devices are used in VSR and CSR, the semiconductor loss is very close in them. The difference on switching loss mainly comes from the parasitic loss. To analyze it, the switches are assumed to be turned on/off instantly without any semiconductor loss. The simplified commutation circuit of VSR is taken as an example. Similar analysis can be done for CSR circuit.

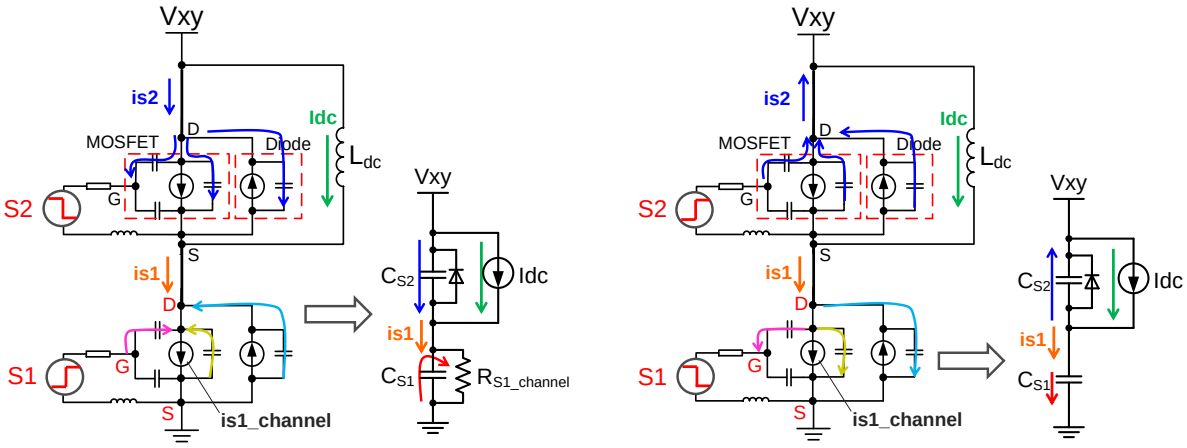


Fig. 5-14. Equivalent circuit with parasitic capacitance: (a) S1 turn-on process; (b) S1 turn-off process.

The impact of parasitic capacitance is analyzed first. As shown in Fig. 5-14(a), S1 channel is turned on instantly and simplified as the resistor $R_{S1\_channel}$. C_{S1} is the equivalent junction capacitance of S1. C_{S2} is the equivalent junction capacitance of S2. C_{S1} is discharged and C_{S2} is charged through $R_{S1\_channel}$. The switching energy lost in S1 channel can be given by

$$E_{on\_channel\_C} = \frac{1}{2} C_{S2} {V_{xy}}^2 + \frac{1}{2} C_{S1} {V_{xy}}^2 \tag{5-6}$$

When S1 is turned off in Fig. 5-14(b), its channel is shut down instantly. C_{S1} is charged and C_{S2} is discharged by I_{dc}. There is no energy lost in S1 channel, as shown in (5-7).

$$E_{off\_channel\_C} = 0 \tag{5-7}$$

The parasitic loss caused by parasitic capacitance can be given by

$$E_C = E_{on\_channel\_C} + E_{off\_channel\_C} = \frac{1}{2} C_{S2} {V_{xy}}^2 + \frac{1}{2} C_{S1} {V_{xy}}^2 \tag{5-8}$$

The impact of parasitic inductance is analyzed as well in Fig. 5-15. L_{S1} and L_{S2} are the parasitic inductance in the commutation circuit. When S1 is turned on in Fig. 5-15(a), its channel is turned on instantly and simplified as the resistor $R_{S1\_channel}$. L_{S1} is charged and L_{S2} is discharged. The high voltage is mainly distributed on the L_{S1} and L_{S2} rather than $R_{S1\_channel}$. So the switching energy lost in the channel is nearly zero, which is given by

$$E_{on\_channel\_L} = 0 \tag{5-9}$$

When S1 is turned off in Fig. 5-15(b), its channel is shut down instantly. L_{S1} is discharged and L_{S2} is charged, generating large voltage on $R_{S1\_channel}$. The switching energy lost on S1 is given by

$$E_{off\_channel\_L} = \frac{1}{2} L_{S2} {I_{dc}}^2 + \frac{1}{2} L_{S1} {I_{dc}}^2 \tag{5-10}$$

The parasitic loss caused by parasitic inductance can be given by

$$E_L = E_{on\_channel\_L} + E_{off\_channel\_L} = \frac{1}{2} L_{S2} {I_{dc}}^2 + \frac{1}{2} L_{S1} {I_{dc}}^2 \tag{5-11}$$

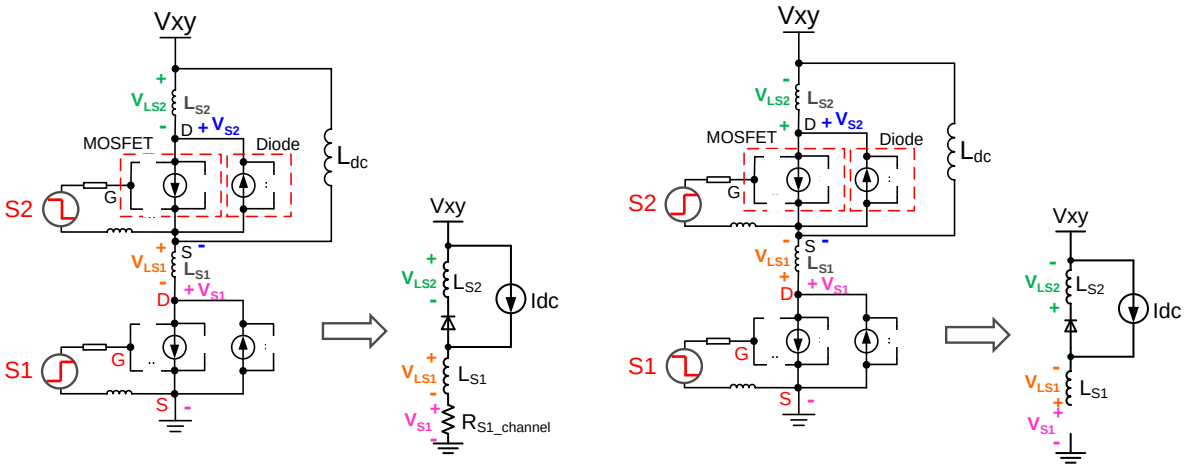


Fig. 5-15. Equivalent circuit with parasitic inductance: (a) S1 turn-on process; (b) S1 turn-off process.

With ac voltage on the switches and lower equivalent junction capacitance, the energy stored in the parasitic capacitance is lower in CSR. But it has larger inductance energy due to large dc-link current. For the converters in Table 5-1, the parasitic energy in VSR is much larger than the one in CSR. That is why the "energy floor" in Fig. 5-9 has higher level than the one in Fig. 5-10.

The parasitic loss in VSR and CSR can be compared under different operation conditions shown in Table 5-2. The output power and the switching frequency are two variables in the calculation. The device voltage rating is 1200 V. The junction capacitance is proportional to the die area, which is proportional to the current rating of the device. The parasitic inductance in the commutation circuit is fixed, which is 80 nH for VSR and 100 nH for CSR.

The calculation process is shown in Fig. 5-16. The capacitance and inductance losses are shown in Fig. 5-17(a) and Fig. 5-17(b) for VSR and CSR respectively. It can be seen that the capacitance loss is the majority of the parasitic loss in VSR, while the inductance loss is the majority in CSR. The total parasitic loss is shown in Fig. 5-18. The parasitic loss is proportional to switching frequency. When the output current is low, CSR has lower parasitic loss. VSR has lower parasitic loss when the output power is high.

Table 5-2. Operation conditions for parasitic loss comparison

Topology	**Voltage source rectifier**	**Current source rectifier**
Output Power	0 – 100 kW	
Input Voltage	480 Vrms (line to line), 60 Hz	
Modulation Index	0.95	
Dc Voltage	555 V	715 V
Switching Frequency	0 – 100 kHz	
Modulation Scheme	MFSM	60˚DPWM

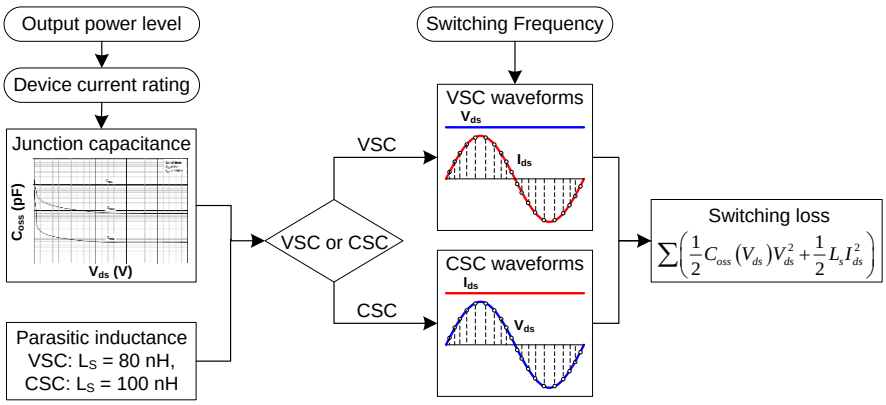
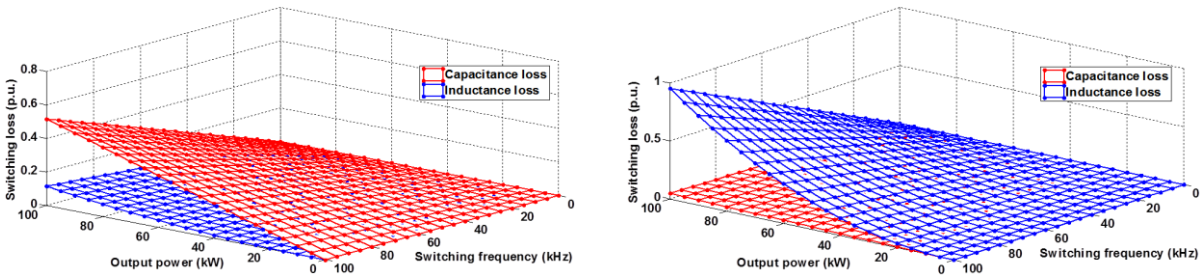


Fig. 5-16. Process of parasitic loss calculation.



(a) (b)

Fig. 5-17. Calculated capacitance and inductance loss: (a) VSR; (b) CSR.

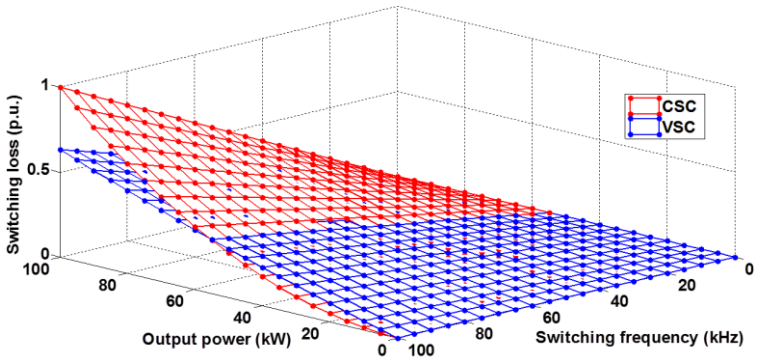
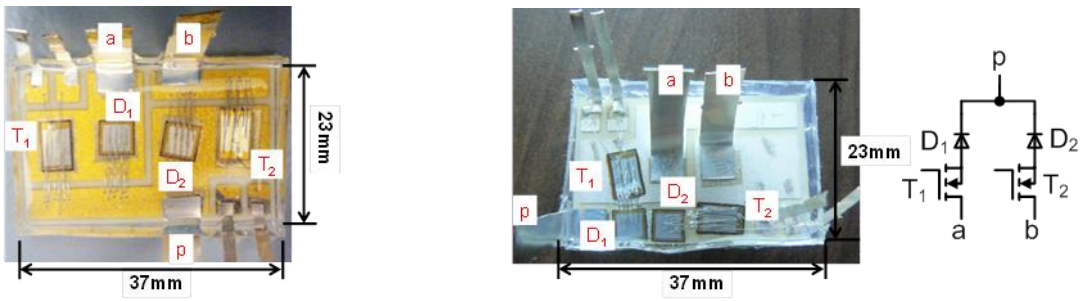


Fig. 5-18. Calculated parasitic loss.

5.4 Experiments with All-SiC Phase-Leg Modules

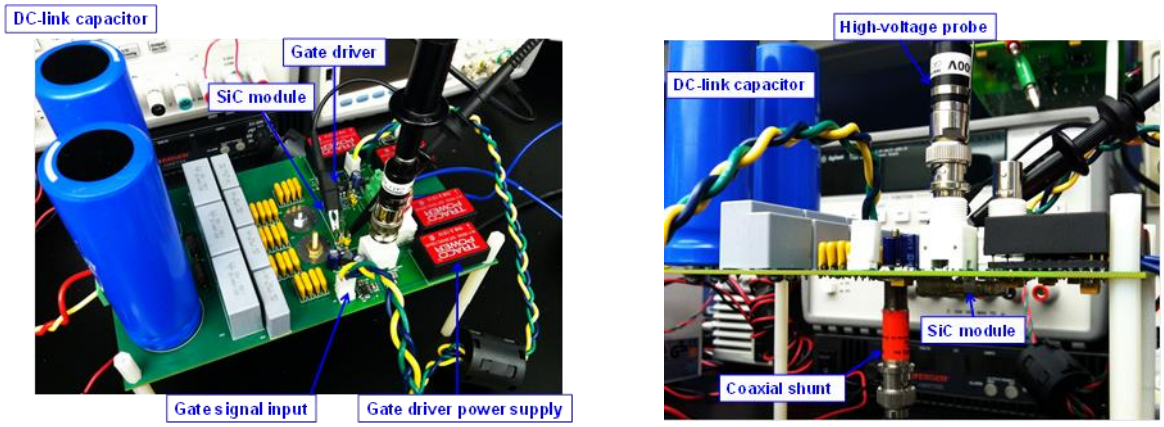
To further study the commutation, two phase-leg modules with all SiC devices are built for VSR and CSR, as shown in Fig. 5-19(a) and Fig. 5-19(b) respectively. 1200 V/50 A SiC MOSFET and SiC Schottky diode from CREE are used in both modules. The size of the phase-leg module is small, which is helpful to reduce the parasitic inductance in the commutation loop.



(a) (b)

Fig. 5-19. All-SiC phase-leg module: (a) VSR; (b) CSR.

A double pulse test board is designed and fabricated for the module test, as shown in Fig. 5-20. The test setup is shown in Fig. 5-21. Both VSR module and CSR module can be tested with the same setup. Tektronix passive probe P5100 (250 MHz bandwidth) is used for voltage measurement. The 15 mΩ coaxial shunt SDN-015 (1.2 GHz bandwidth) is used for current measurement.



(a) (b)

Fig. 5-20. Module test board: (a) Top view; (b) Side view.

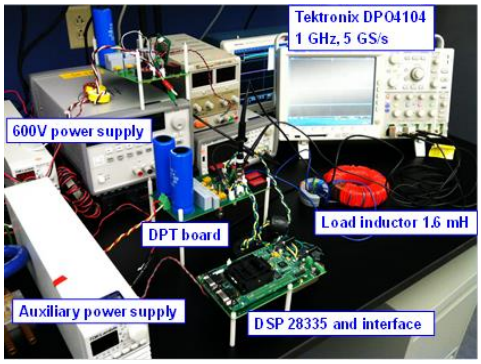


Fig. 5-21. Module test setup.

The test circuits for VSR module and CSR module are shown in Fig. 5-22(a) and Fig. 5-22(b) respectively, where L_p is the parasitic inductance on the test board and C_p is the equivalent parallel capacitance of load inductor. Their value can be measured with impedance analyzer. $L_p = 35\ nH$ and $C_p = 10\ pF$. The gate signals are also shown in Fig. 5-22.

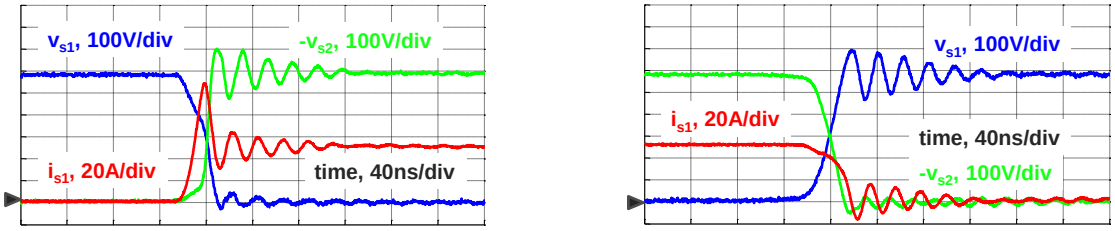
The switching waveforms of VSR module are drawn in Fig. 5-23 when $V_{xy} = 600\ V$, $I_{dc} = 50\ A$ and external gate resistor $R_g = 10\ \Omega$. The switching waveforms of CSR module are drawn in Fig. 5-24 under the same test condition.

(a) (b)

Fig. 5-22. Test circuit: (a) VSR; (b) CSR.

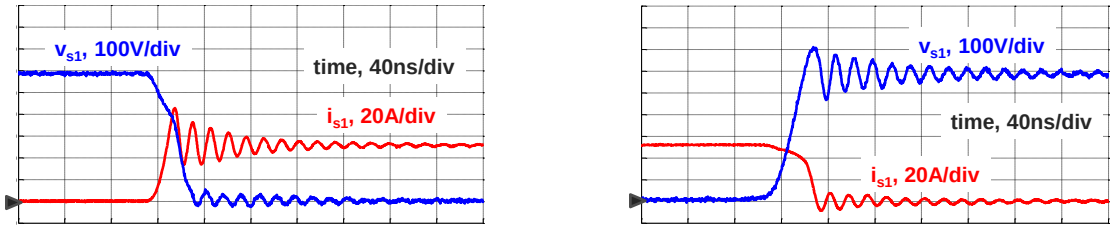
The switching waveforms of VSR module are drawn in Fig. 5-25 when $V_{xy} = 400\,V$, $I_{dc} = 34\,A$ and external gate resistor $R_g = 5\,\Omega$. The switching waveforms of CSR module are drawn in Fig. 5-26 under the same test condition.

In the turn on process, the VSR module has higher displacement current because of its larger junction capacitance. It has lower voltage spike on switches than CSR module. The resonance frequency is higher in CSR module.



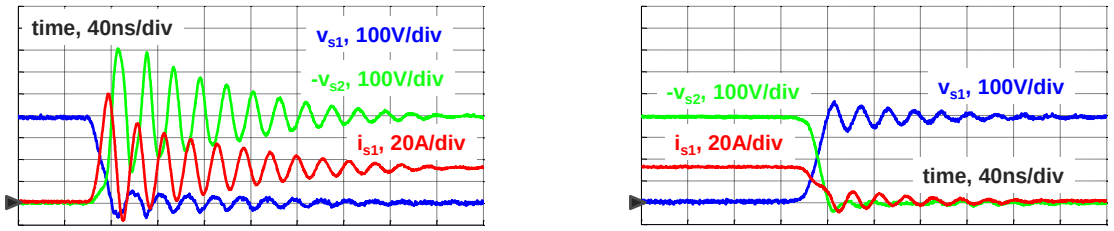
(a) (b)

Fig. 5-23. Switching waveforms of VSR module when $V_{xy} = 600$ V, $I_{dc} = 50$ A and $R_g = 10\,\Omega$: (a) S1 turn on; (b) S1 turn off.



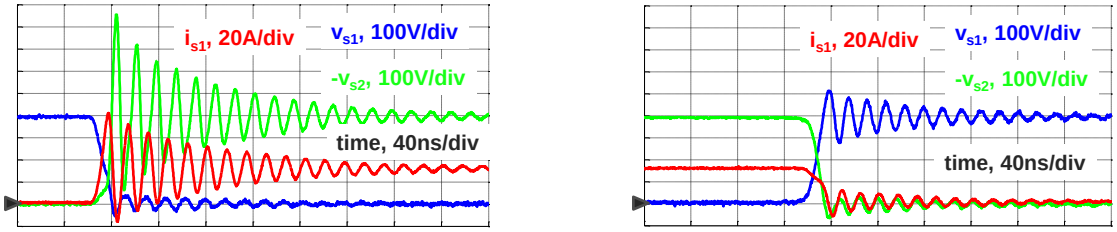
(a) (b)

Fig. 5-24. Switching waveforms of CSR module when $V_{xy} = 600$ V, $I_{dc} = 50$ A and $R_g = 10\,\Omega$: (a) S1 turn on; (b) S1 turn off.



(a) (b)

Fig. 5-25. Switching waveforms of VSR module when $V_{xy} = 400$ V, $I_{dc} = 34$ A and $R_g = 5\ \Omega$: (a) S1 turn on; (b) S1 turn off.



(a) (b)

Fig. 5-26. Switching waveforms of CSR module when $V_{xy} = 400$ V, $I_{dc} = 34$ A and $R_g = 5\ \Omega$: (a) S1 turn on; (b) S1 turn off.

The external gate resistor is further reduced in the CSR module to increase its switching speed, as long as the device voltage does not exceed the breakdown voltage. When $V_{xy} = 600\ V$ and $I_{dc} = 26\ A$, the voltage waveforms with different external gate resistors are compared in Fig. 5-27. The maximum voltage change rate is 200 V/ns and the maximum voltage occurs on S2 when it is turned off. The current waveforms with different external gate resistors are compared in Fig. 5-28. The maximum current change rate is 11 A/ns and the maximum current occurs on S1 when it is turned on.

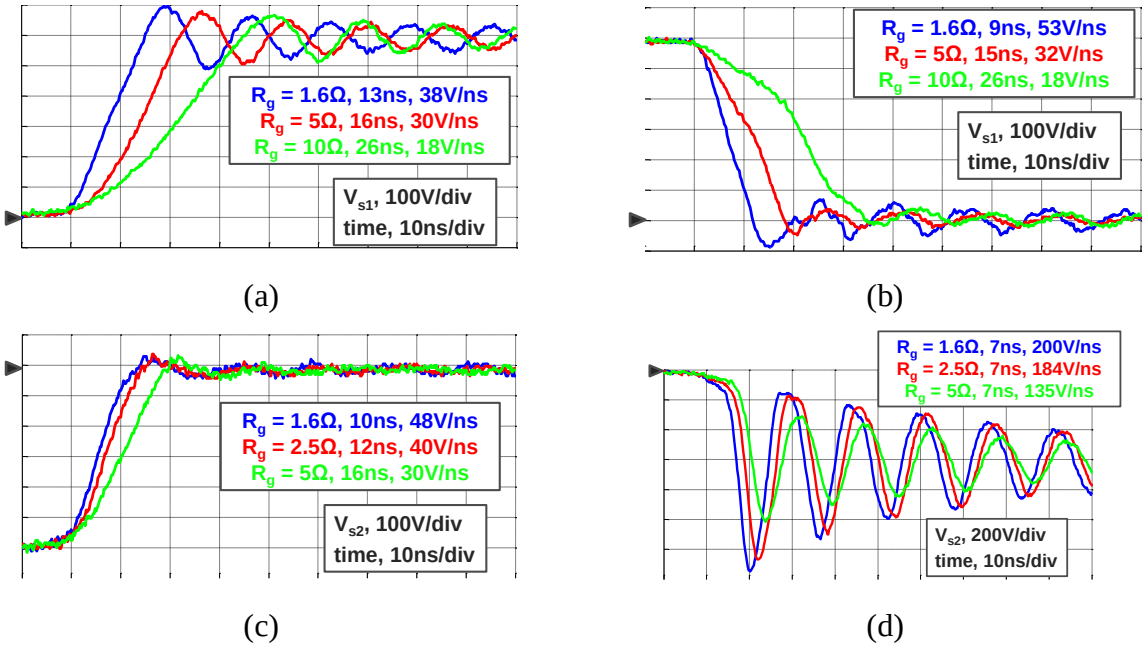


Fig. 5-27. Voltage waveforms of CSR module with different external gate resistors: (a) S1 turn off; (b) S1 turn on; (c) S2 turn on; (d) S2 turn off.

As the switching speed increases, the parasitic inductance becomes the main constraint for high speed switching. It resonates with the junction capacitance of the devices and causes large voltage overshoot. As shown in Fig. 5-29, the voltage spike on S2 is mainly caused by L_p on the test board.

To reduce the resonance in the switching process, three methods can be applied. First, a 0.1 μF/1 kV ceramic capacitor is soldered between the two terminals of the SiC module, as shown in Fig. 5-30. Its resonance frequency is 4 MHz and has 3.8 Ω impedance at 50 MHz. It provides a low-impedance loop for the resonance and by-passes L_p. Compared with the original waveforms in Fig. 5-31, the voltage resonance is largely reduced in Fig. 5-32.

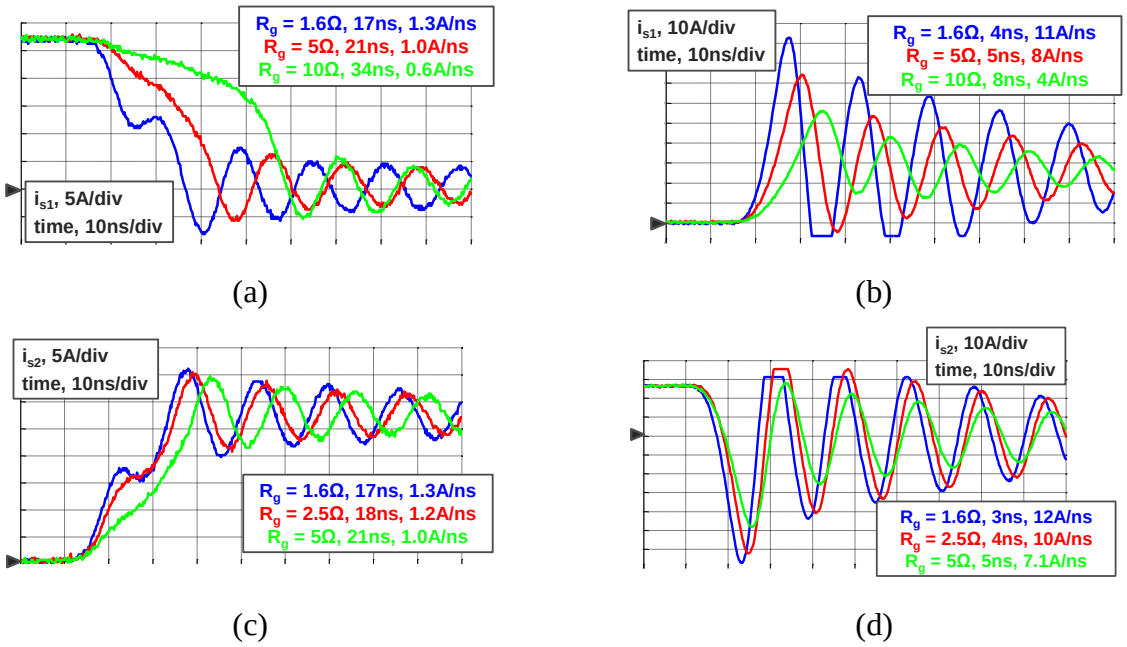


Fig. 5-28. Current waveforms of CSR module with different external gate resistors: (a) S1 turn off; (b) S1 turn on; (c) S2 turn on; (d) S2 turn off.

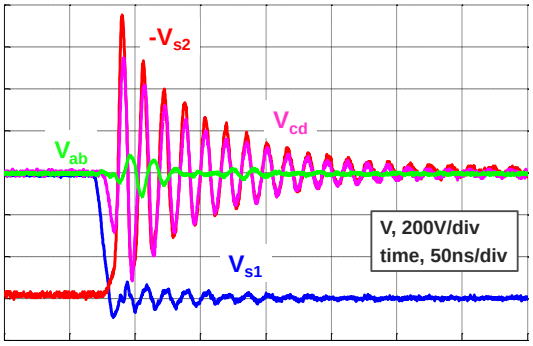


Fig. 5-29. Switching waveforms when S1 is turned on (V_{xy} = 600 V, I_{dc} = 26 A and R_g = 1.6 Ω).

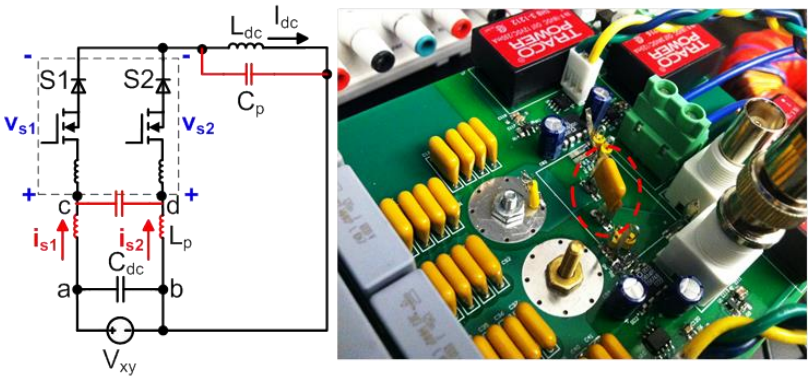
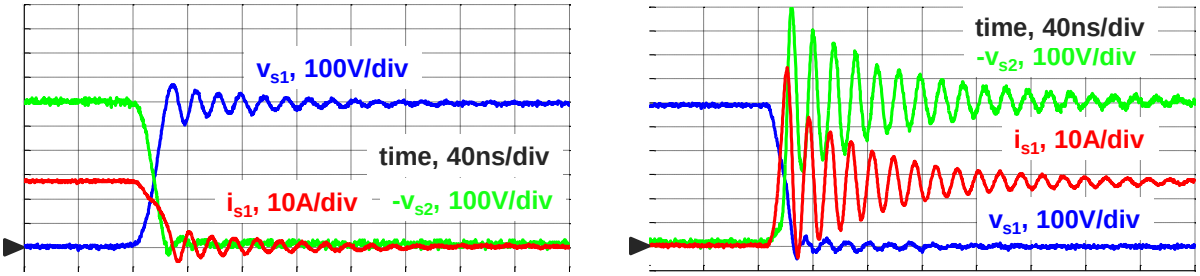
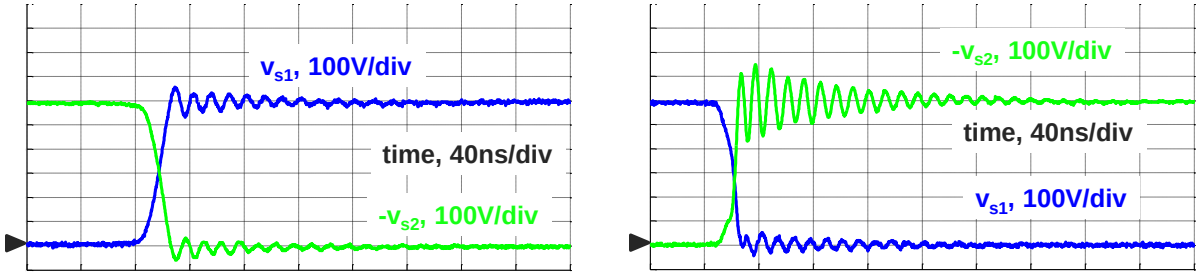


Fig. 5-30. Test circuit with decoupling capacitor.



(a) (b)

Fig. 5-31. Switching waveforms without any methods to reduce resonance: (a) S1 turn off; (b) S1 turn on.



(a) (b)

Fig. 5-32. Switching waveforms with decoupling capacitor: (a) S1 turn off; (b) S1 turn on.

Second, an 1 Ω resistor is added in series with the added decoupling capacitor to damp the resonance in the commutation loop, as shown in Fig. 5-33. It can help to attenuate the resonance

without increasing much loss. Compared with the waveforms in Fig. 5-32, the voltage resonance is damped faster in Fig. 5-34.

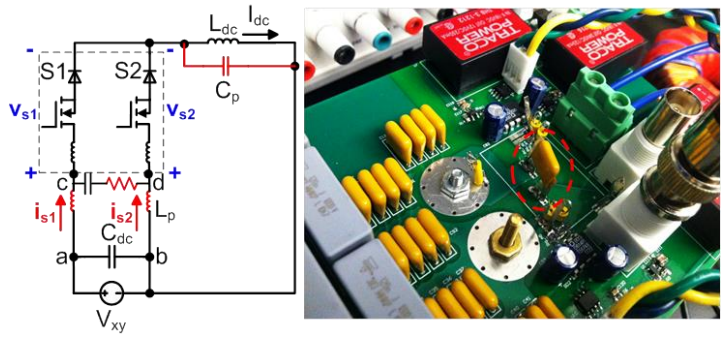
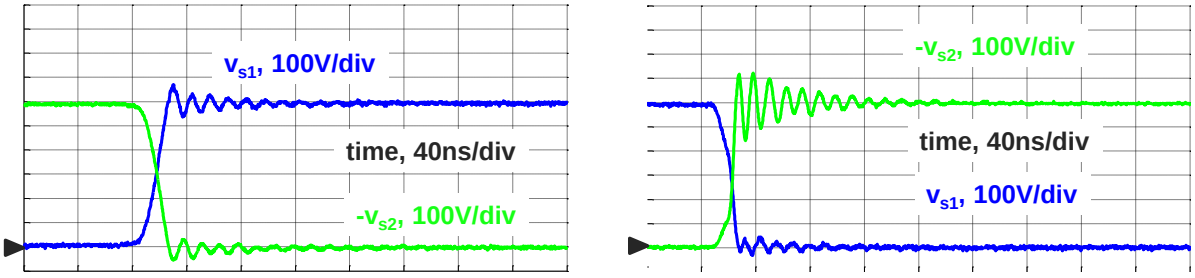


Fig. 5-33. Test circuit with damping resistor.



(a) (b)

Fig. 5-34. Switching waveforms with damping resistor: (a) S1 turn off; (b) S1 turn on.

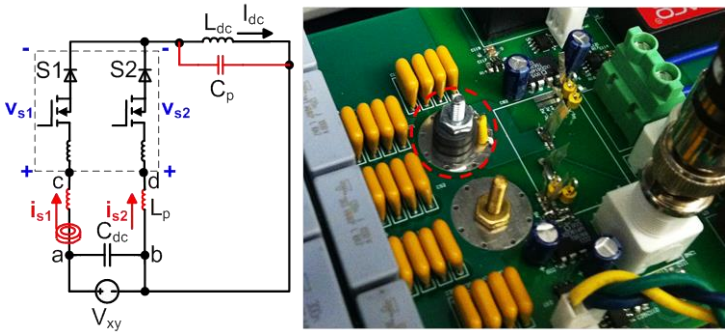
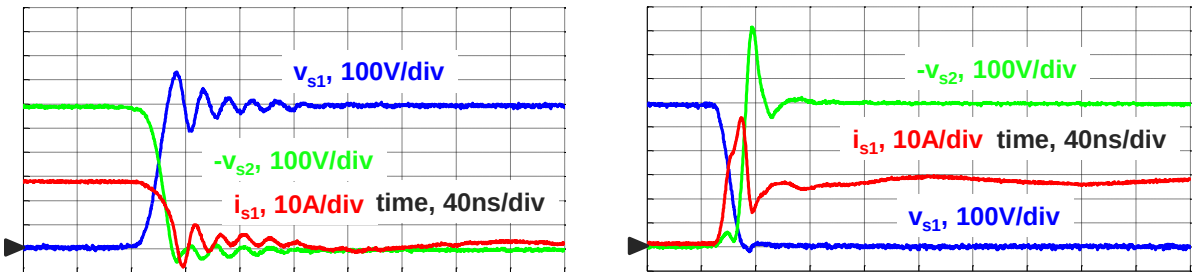


Fig. 5-35. Test circuit with magnetic beads.



(a) (b)

Fig. 5-36. Switching waveforms with magnetic beads: (a) S1 turn off; (b) S1 turn on.

Third, a magnetic bead (NiZn Ferrite 3W800) is added to the commutation loop to reduce the resonance during commutation. The bead has small dimensions and little impact on the commutation loop area, as shown in Fig. 5-35. The magnetic bead provides high impedance when the current is close to zero. It can reduce the resonance dramatically in turn-on process, as shown in Fig. 5-36(b). But it may cause a little higher voltage overshoot in turn-off process, as shown in Fig. 5-36(a). The voltage change rate, current change rate, peak voltage and switching energy are listed in Table 5-3. All three methods can reduce the resonance and peak voltage.

Table 5-3. Switching parameters comparison

Case	$E_{on}+E_{off}$	di/dt	dv/dt	Peak voltage
Original	254 μJ	8.0 A/ns	135 V/ns	1016 V
With one bead	234 μJ	3.0 A/ns	91 V/ns	914 V
With two beads	234 μJ	2.2 A/ns	55 V/ns	822 V
With decoupling capacitor	-	-	57 V/ns	748 V
With damping resistor	-	-	57 V/ns	722 V

5.5 All-SiC Converter Module

The power module can integrate more semiconductor dies and increase the power density of the converter. Moreover, it has lower parasitics in the commutation loop, compared with discrete devices. An all-SiC converter modules was designed and built, as shown in Fig. 5-37 and Fig. 5-38. 50 A SiC Schottky diode CPW5-1200-Z050B and 50 A SiC MOSFET CPM2-1200-0025B from CREE are used in the power module. It includes three lower switches, forming the commutation loop in the new topology. The semiconductor dies are plated on the direct bonded copper (DBC) substrate, with wire bonds for interconnection.

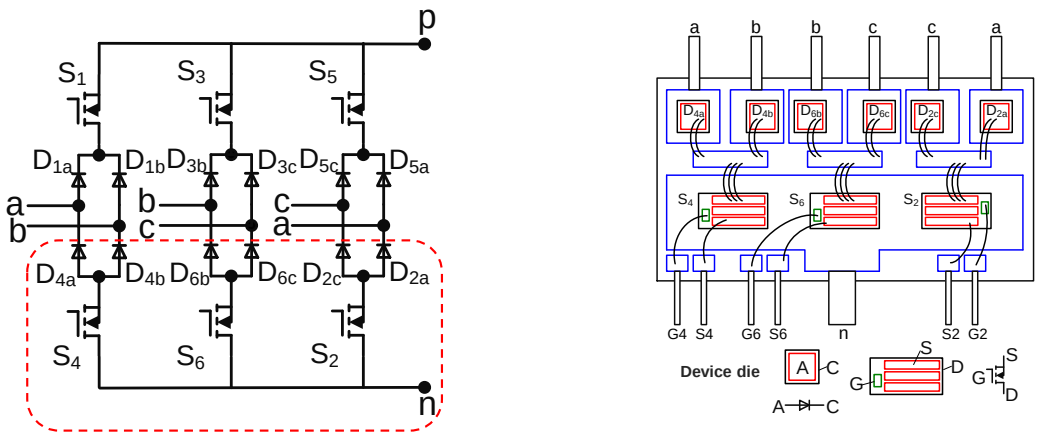


Fig. 5-37. Layout of the all-SiC converter module for new topology.

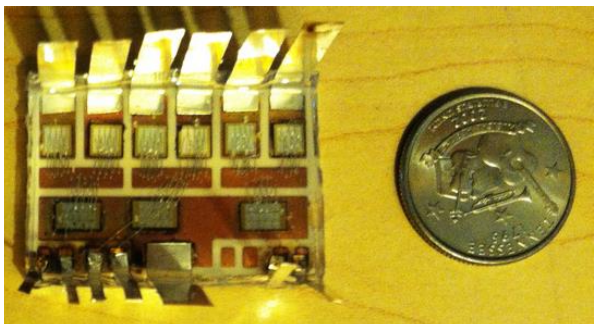


Fig. 5-38. Photo of the all-SiC converter module for new topology.

The converter module can also be configured as the traditional CSR topology, as shown in Fig. 5-39. The two pins connected with Dxa and Dxb (x = 4, 6, 2) are shorted with copper bars. In this way, the commutation in both the new topology and the traditional one can be measured and compared with the same converter module.

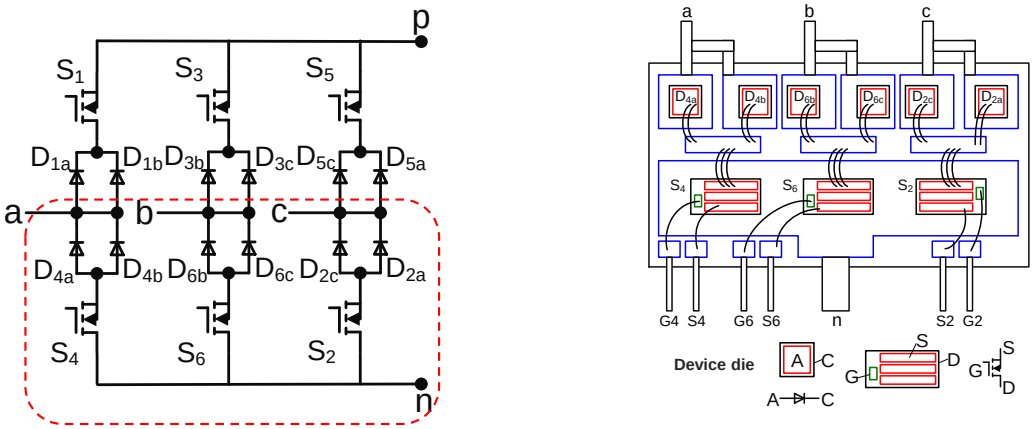


Fig. 5-39. Reconfigured converter module for traditional topology.

5.6 Static Characteristics

The static characteristics are measured on the power module with Tektronix curve tracer 371B. The breakdown voltage curves of SiC MOSFET and SiC Schottky diode are shown in Fig. 5-40 and Fig. 5-41 respectively. The output characteristics of the power module are shown in Fig. 5-42, with 20 V gate drive voltage.

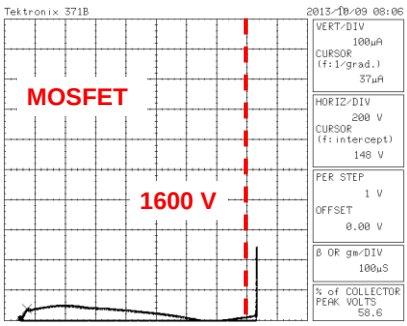


Fig. 5-40. SiC MOSFET breakdown voltage.

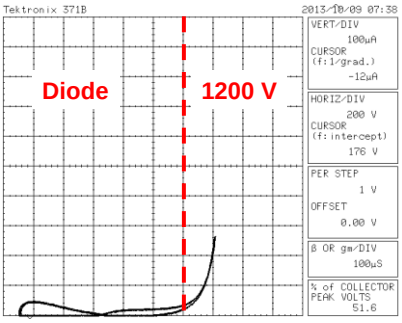


Fig. 5-41. SiC Schottky diode breakdown voltage.

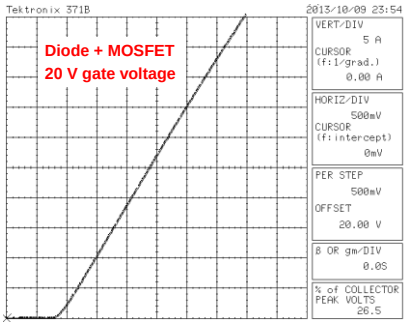


Fig. 5-42. Output characteristics.

5.7 Switching Characteristics

A test board was built to test the commutation in the power module, as shown in Fig. 5-43. The SiC power module is mounted on the back of the PCB. A 15 mΩ coaxial shunt SDN-015 with 1.2 GHz bandwidth from T&M Research is used for current measurement. A high-voltage differential probe THDP0200 with 200 MHz bandwidth from Tektronix is used for voltage measurement. The test setup is shown in Fig. 5-44, including a test board, an oscilloscope, a load inductor, a DSP board, 600 V power supply and an auxiliary power supply. The DSP board can generate the gate signals for driving the devices.

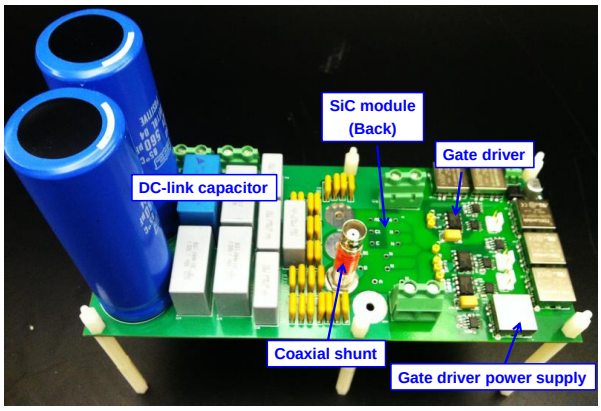


Fig. 5-43. Photo of the test board.

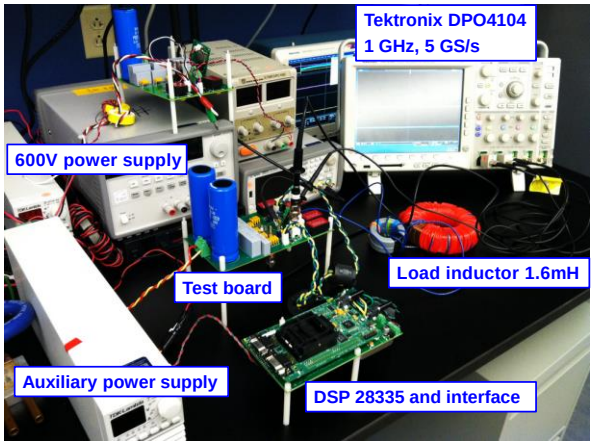


Fig. 5-44. Photo of the test setup.

As described in Chapter 3, the commutations in the new topology include three switches. Commutation loop 1 is shown in Fig. 5-45. When $v_c > v_b > v_a$, the equivalent circuit is shown in red lines. The gate signals shows that S6 will be kept on in the test. S2 and S4 are turned on in the first pulse and the dc power supply charges the load current I_{dc} to a given level. Then S2 and S4 are turned off simultaneously and I_{dc} is freewheeled through S6. In the second pulse, S2 and S6 are turned on simultaneously and kept on for a short time. In this process, the voltage and current waveforms on the switches can be collected on the test board. There are two minor commutation loops in parallel in the power modules, as drawn in Fig. 5-45. They are almost

symmetric, which is advantageous to reduce the equivalent parasitic inductance in the commutation loop.

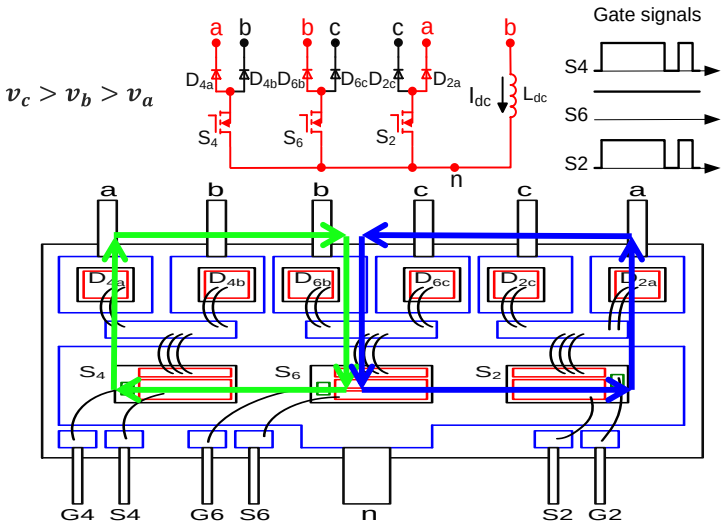
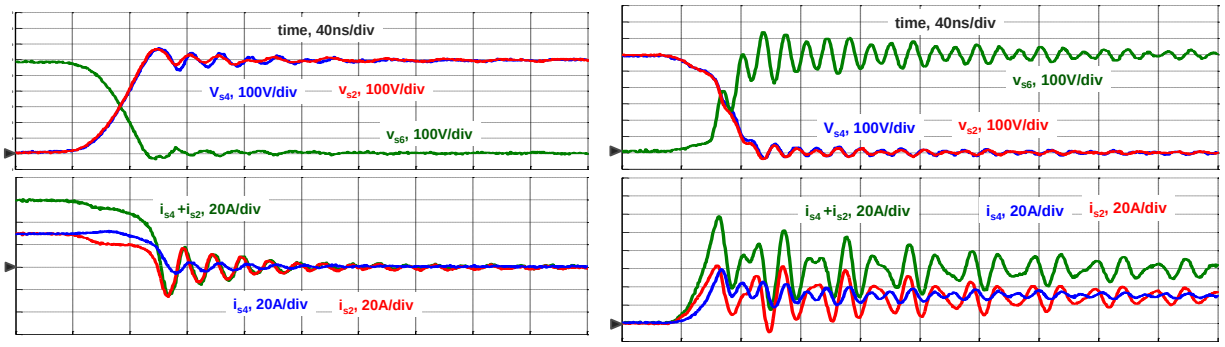


Fig. 5-45. Commutation loop 1 in new topology.

The switching waveforms of Commutation loop 1 are shown in Fig. 5-46 when $v_{ba} = 600\,V$ and $I_{dc} = 60\,A$. The external gate resistor is 20 Ω for each switch. The switching waveforms of S2 and S4 are not always the same. The current resonance is smaller in S4 than that in S2. S4 has longer delay time in both turn-on and turn-off processes. The speed difference between S2 and S4 comes from two aspects. The characteristics of the paralleled device dies are not the same and the module layout is not totally symmetric.



(a) (b)

Fig. 5-46. Switching waveforms in Commutation loop 1: (a) Turn-off; (b) Turn-on.

The other kind of commutation loop is shown in Fig. 5-47 in the new topology. In Commutation loop 2, S2 is kept on and S4 and S6 are sharing the load current. The two minor loops are not symmetric in Fig. 5-47, where the green one has larger area than the blue one.

The switching waveforms in Commutation loop 2 are shown in Fig. 5-48. The voltage and current spikes are more serious in Commutation loop 2 than those in Commutation loop 1. The resonance frequency is lower in Commutation loop 2, indicating higher parasitic inductance in the loop.

From the comparison of the switching waveforms in the two commutation loops, it can be demonstrated that symmetric commutation loop has lower parasitic inductance, voltage and current spikes.

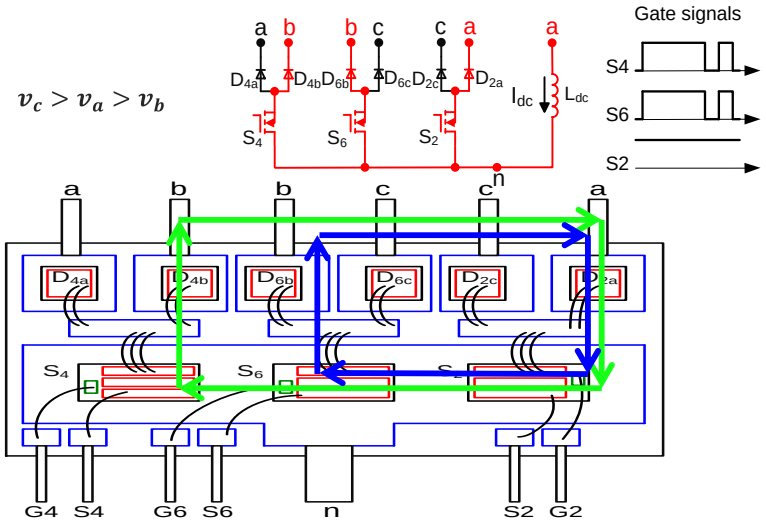
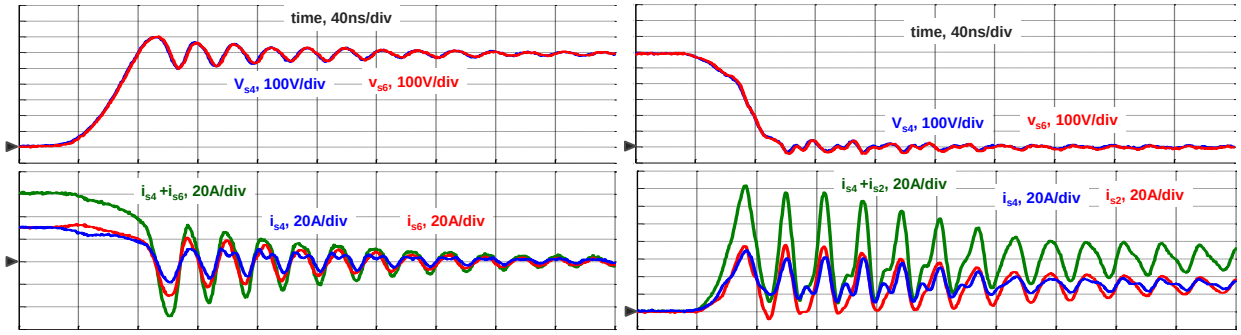


Fig. 5-47. Commutation loop 2 in new topology.



(a) (b)

Fig. 5-48. Switching waveforms in Commutation loop 2: (a) Turn-off waveforms; (b) Turn-on waveforms.

By configuring the power module in the way shown in Fig. 5-39, the switching waveforms in the traditional topology were measured with the same test setup. Commutation loop 3 is shown in Fig. 5-49, where S4 and S6 are commutating with each other. The two branch diodes are paralleled in this configuration, so the total die area is the same in both traditional and new topologies. The switching waveforms in Commutation loop 3 are shown in Fig. 5-50 when $v_{ba} = 600\ V$ and $I_{dc} = 60\ A$.

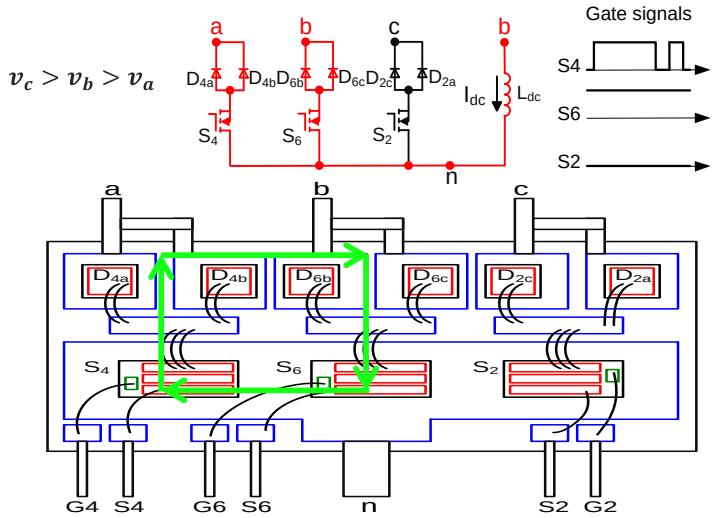
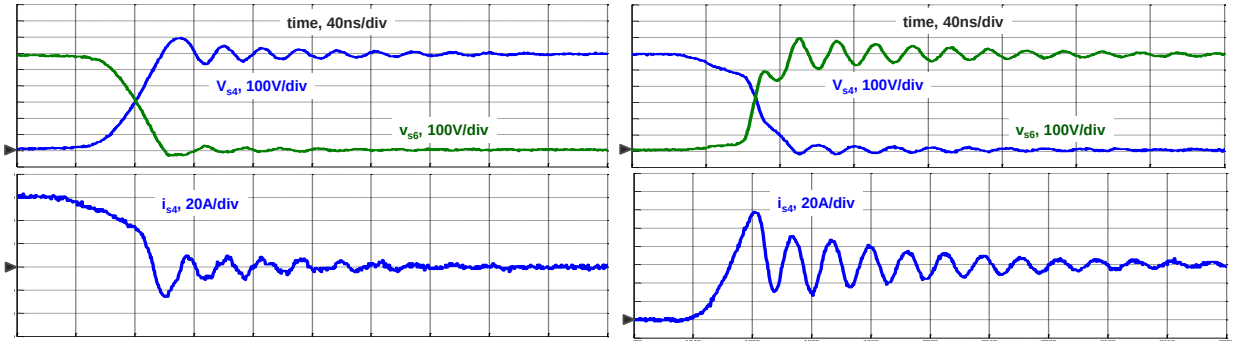


Fig. 5-49. Commutation loop 3 in traditional topology.

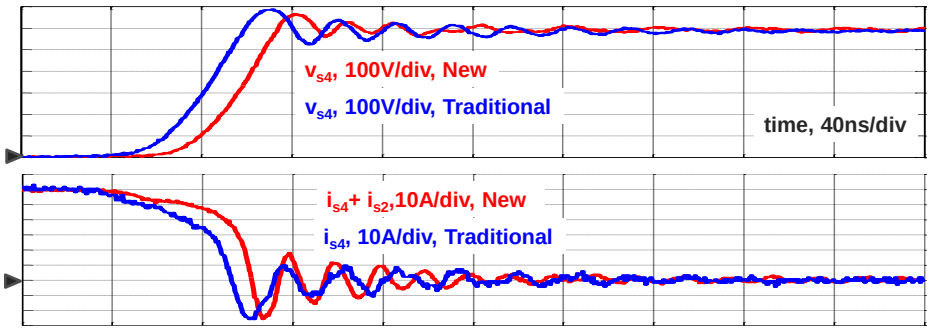


(a) (b)

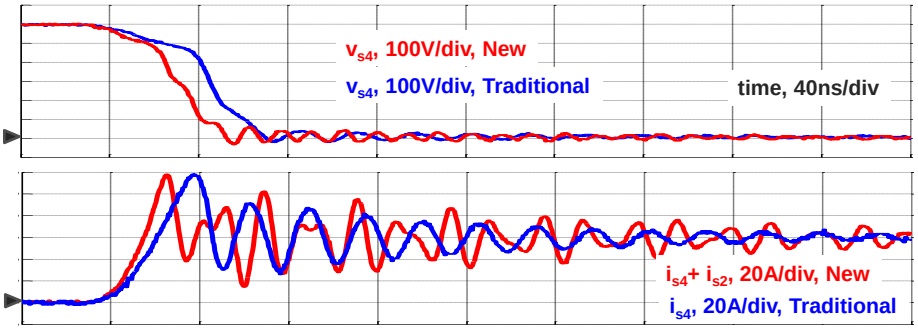
Fig. 5-50. Switching waveforms in Commutation loop 3: (a) Turn-off waveforms; (b) Turn-on waveforms.

The switching waveforms in the new topology and traditional one are compared in Fig. 5-51. The turn-off waveforms are compared in Fig. 5-51(a). The new topology has longer voltage rise time and higher voltage spike than the new topology in the turn-off process. The current rise time is also longer and the resonance frequency is higher in the new topology. Because the current is shared in two switches in the new topology, each switch has lower plateau gate voltage and

lower voltage charge rate, leading to longer voltage rise time and higher turn-off energy, especially when input voltage is high.



(a)

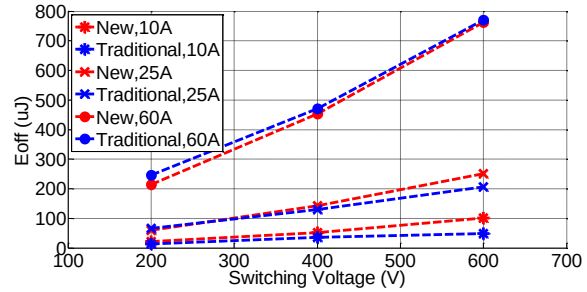


(b)

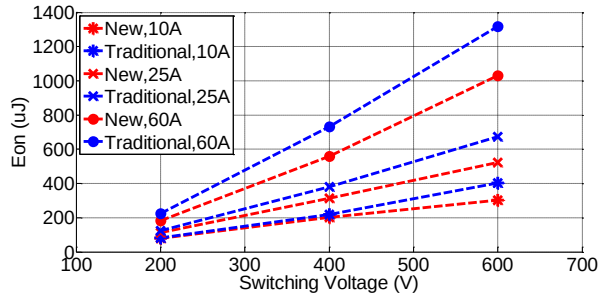
Fig. 5-51. Switching waveforms comparison: (a) Turn-off waveforms; (b) Turn-on waveforms.

The turn-on waveforms are compared in Fig. 5-51(b). The new topology has shorter voltage fall time and current rise time than the new topology in the turn-on process. Because the current is shared in two switches in the new topology, each switch has lower plateau gate voltage, higher current rise rate and higher voltage charge rate, leading to lower turn-on energy, especially when the load current is high. The amplitude of the resonance is comparable in the two topologies. The resonance frequency is higher in the new topology. Although the new topology has higher switching speed, it does not have obviously worse resonance because the equivalent parasitic inductance in the commutation loop is smaller in the new topology.

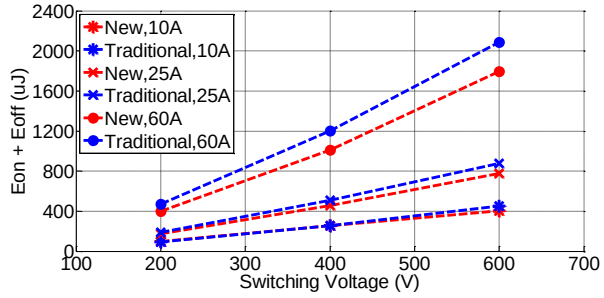
Under different voltage and current conditions, the switching energy is measured and shown in Fig. 5-52. The turn-off energy E_{off} of the two topologies is compared in Fig. 5-52(a). E_{off} is higher in the new topology, especially when the current is low and voltage is high (voltage rise time is much longer in the new topology). When the current is high, the current fall time is obviously lower in the new topology, leading to lower E_{off}.



(a)



(b)



(c)

Fig. 5-52. Switching energy comparison: (a) E_{off}; (b) E_{on}; (c) $E_{off} + E_{on}$.

The turn-off energy E_{on} of the two topologies is compared in Fig. 5-52(b). E_{on} is lower in the new topology, especially when the current and voltage are both high (current rise time is much less in the new topology). When the current is low, the current rise time tends to be the same and the switching energy is very close in both topologies.

The total switching energy is compared in Fig. 5-52(c). It is lower in the new topology, especially when the current and voltage are high. E_{on} contributes more to the total energy in these cases.

5.8 Conclusion

Two all-SiC phase-leg modules have been developed and characterized. The switching performance in CSR is compared with the one in VSR. Because of higher equivalent junction capacitance of the switches in VSR, it has higher current spike but lower voltage spike than CSR. When pushed to higher switching speed, the CSR module is more reliable without any shoot-through problem.

An all-SiC converter module has been designed and characterized for the new CSR. With current sharing in two phase legs, the switching speed is higher and the switching energy is lower in the new CSR than in the traditional one. The minor commutation loops are in parallel to reduce the parasitic inductance in new CSR.

6 Modulation Scheme Comparison

In this chapter, the commutations in the three-phase buck rectifier (CSR) with freewheeling diode are investigated in detail, based on the experiments with different device combinations as shown in Table 6-1. Then the switching loss of the buck rectifier is modeled and calculated, including two types of commutations and the impact of the non-switching devices. The comparison of the four commonly used space vector modulation schemes is made considering different device characteristics. Through the analysis in this chapter, the highest efficiency modulation scheme can be selected for the three-phase buck rectifier as a function of the semiconductors devices employed.

Table 6-1. Device combinations

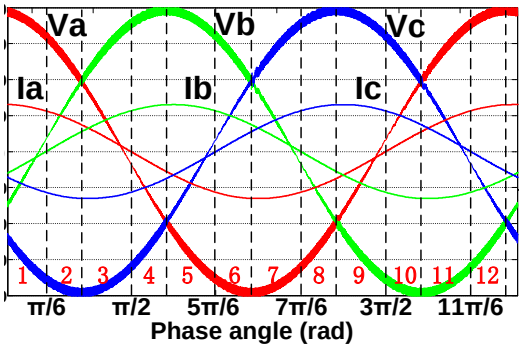
No.	Switch Sx	Df
1	RB-IGBT	SiC Schottky diode
2	IGBT and Si soft-recovery diode	
3	IGBT and SiC Schottky diode	

6.1 Modulation Schemes in Buck Rectifiers

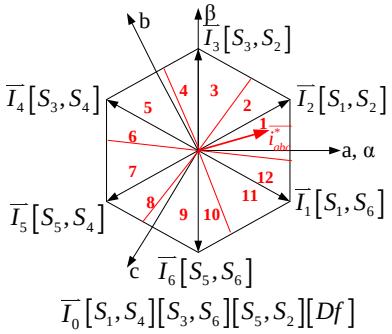
The input voltages v_a, v_b and v_c and the fundamental components i_{a1}, i_{b1} and i_{c1} of the input currents are defined in (6-1), where V_m and I_m are the peak values of the sinusoidal voltage and current respectively, ω is the angular frequency of the ac mains, and φ is the phase difference between v_a and i_{a1}.

$$\begin{cases} v_a = V_m cos(\omega t + \varphi) \\ v_b = V_m cos\left(\omega t - \frac{2\pi}{3} + \varphi\right) \\ v_c = V_m cos\left(\omega t + \frac{2\pi}{3} + \varphi\right) \end{cases}$$
$$\begin{cases} i_{a1} = I_m cos(\omega t) \\ i_{b1} = I_m cos\left(\omega t - \frac{2\pi}{3}\right) \\ i_{c1} = I_m cos\left(\omega t + \frac{2\pi}{3}\right) \end{cases} \quad (6\text{-}1)$$

According to the relationship between the input voltage and current, 12 sectors are defined for the buck rectifier as shown in Fig. 6-1 [94][95]. On the space vector plane in Fig. 6-1(b), the input current space vector $i_{abc}^* = \sqrt{\frac{3}{2}} I_m e^{j\omega t}$ can be synthesized by six active space vectors $\overrightarrow{I_x}, x = 1, \dots, 6$ and a zero vector $\overrightarrow{I_0}$. The symbol $[S_x, S_y], x, y = 1, \dots, 6$ denotes the on state of the switches S_x and S_y in a space vector. Considering both the switching loss and modulation index range, i_{abc}^* is usually composed by two consecutive active vectors and the zero vector in each sector [97].



(a) Fundamental components of input current and voltage



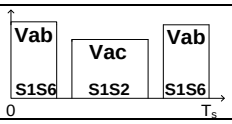
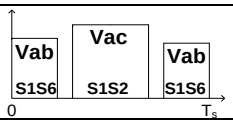
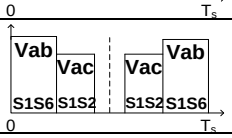
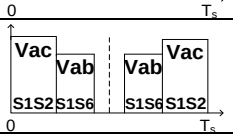
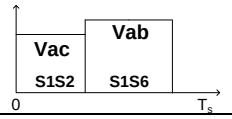
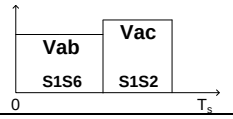
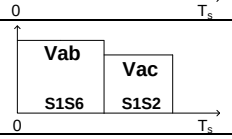
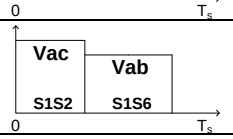
(b) Space vector plane

Fig. 6-1. Sector division in space vector PWM.

The “3-switch” and “4-switch” space vector modulation schemes, which contain three and four transitions in a switching period respectively, are most widely used in buck rectifiers, because they achieve a good compromise between the switching loss and harmonic current level [98]. Table 6-2 shows four modulation schemes under study in this chapter, including two symmetric “4-switch” schemes and two asymmetric “3-switch” schemes. The output voltage V_{pn} in two consecutive sectors (Fig. 6-1) is used to describe their difference regarding space vector arrangement.

All four modulation schemes have been proposed to reduce the switching loss [83][94][95][128][129]. Both symmetric schemes were introduced in [94], where Symmetric Scheme I (SS-I) is named “Half-wave Symmetrical Modulation (HSM)” and Symmetric Scheme II (SS-II) “Modified Full-wave Symmetrical Modulation (MFSM)”. The zero vector is placed between two active vectors in SS-I, and after the two active vectors in SS-II. The space vectors are arranged to make the switching voltage the lowest in SS-II, so that the switching loss is assumed to be minimum [94][95]. Asymmetric Scheme III (US-III) is first proposed in [128] to realize soft switching and reduce the switching loss. Asymmetric Scheme IV (US-IV) is applied in charge control of buck rectifier in [83] and [129].

Table 6-2. Modulation schemes for comparison

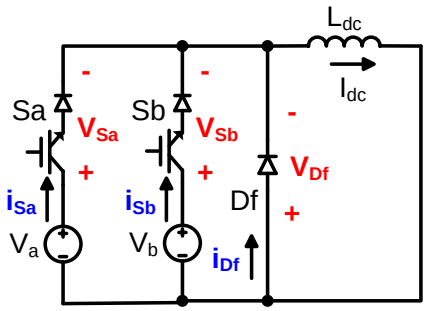
Modulation scheme	Output voltage Vpn		Number of different transitions			
			Switch-switch commutation		Switch-diode commutation	
	Sector12:Va>Vc≥Vb $-\pi/6 \le \omega t < -\varphi$	*Sector1: Va>Vb>Vc* $-\varphi \le \omega t < \pi/6$	Positive turn-off	Positive turn-on	Positive turn-off	Positive turn-on
Symmetric Scheme I (SS-I)			-	-	2	2
Symmetric Scheme II (SS-II)			1	1	1	1
Asymmetric Scheme III (US-III)			-	1	1	1
Asymmetric Scheme IV (US-IV)			1	-	1	1

There are two types of commutations in the buck rectifier, the one between two switches (switch-switch commutation) and the one between a switch and the freewheeling diode (switch-diode commutation). In each type of commutation, two kinds of transitions exist. When one switch is turned on under positive V_{ce} (positive turn-on), its complementary switch is turned off under negative V_{ce} (reverse turn-off), and when one switch is turned off under positive V_{ce} (positive turn-off), its complementary switch is turned on under negative V_{ce} (reverse turn-on). As shown in Table 6-2, SS-I has only switch-diode commutations, while SS-II includes both types of commutations. US-III has no positive turn-off transition, while US-IV has no positive turn-on transition in the switch-switch commutation. The number of different transitions in each modulation scheme is listed in Table 6-2.

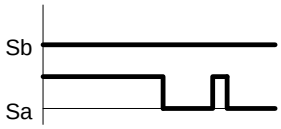
6.2 Device Characterization and Commutation Analysis

The commutation circuit in the buck rectifier can be simplified as drawn in Fig. 6-2(a), consisting of two switches Sa and Sb and a freewheeling diode Df. Sa and Sb represent any two switches in the upper (S1, S3 and S5) or lower (S2, S4 and S6) legs of the buck rectifier.

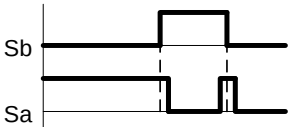
As shown in Fig. 6-3, an experimental circuit was built according to the circuit in Fig. 6-2. Two types of gate signals in Fig. 6-2(b) and (c) were used to test the commutation between Sa and Df, as well as the commutation between Sa and Sb. Sb is kept off when Sa is commutating with Df in Fig. 6-2(b).



(a) Commutation unit in the buck rectifier



(b) Gate signals when Sa and Df commutate



(c) Gate signals when Sa and Sb commutate

Fig. 6-2. Commutation unit and the device gate signal.

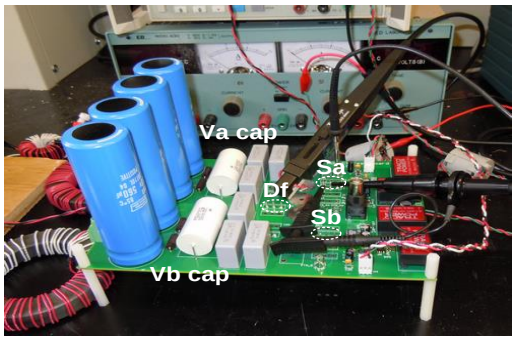


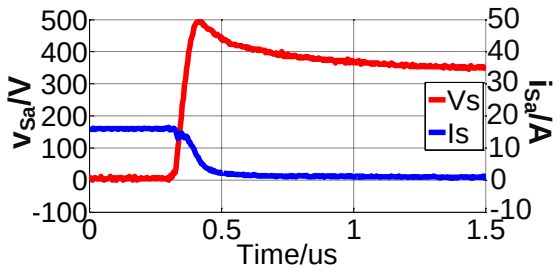
Fig. 6-3. Device double pulse test board.

In the experiments, IXYS 1200 V, 15 A RB-IGBT (IXRP15N120) and Infineon 1200 V, 15 A high-speed IGBT (IKW15N120H3) are used as switches. The diode in the circuit is realized by either a CREE 1200 V, 10 A SiC Schottky diode (C2D10120), or an IXYS 1200 V, 15 A Si soft-recovery diode (DSEP12-12A). The measurement equipment is listed in Table 6-3 with their bandwidths, critical information for measuring the switching waveforms accurately [122]. In the experimental circuit, the parasitic inductance in the commutation loop is well limited by careful PCB layout according to [123].

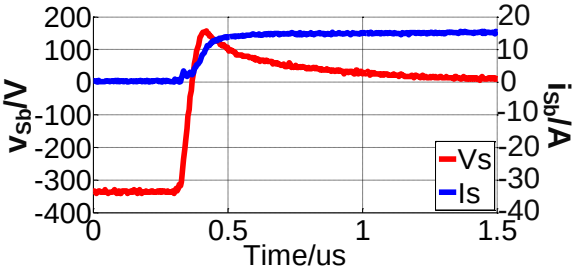
Table 6-3. Measurement equipment

Equipment	**Specification**
Tektronix DPO4104	Oscilloscope, 500MHz
Tektronix P5100	Passive high-voltage probe, 250MHz
Tektronix TCP0030	Current probe, 120MHz

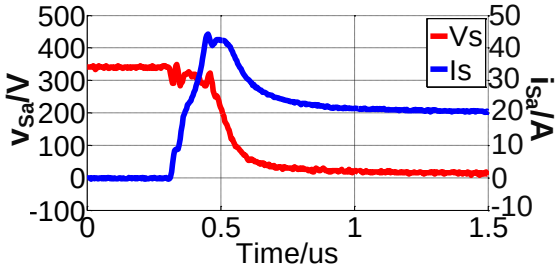
The device combinations in Table 6-1 are tested and their switching characteristics are compared. As an example, the switching waveforms in the commutation between two RB-IGBTs (Sa and Sb) are shown in Fig. 6-4 when $V_a = 680\ V$, $V_b = 340\ V$ and $I_{dc} = 15\ A$. Fig. 6-5 shows the waveforms in the commutation between the RB-IGBT Sa and the freewheeling diode Df when $V_a = 340\ V$ and $I_{dc} = 15\ A$.



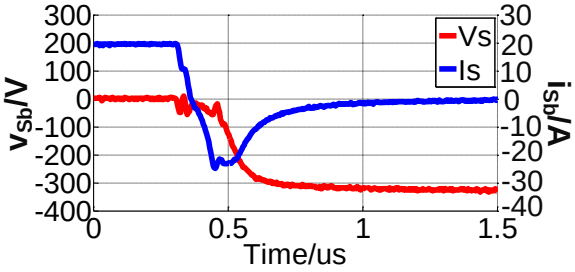
(a) Sa positive turn-off transition



(b) Sb reverse turn-on transition

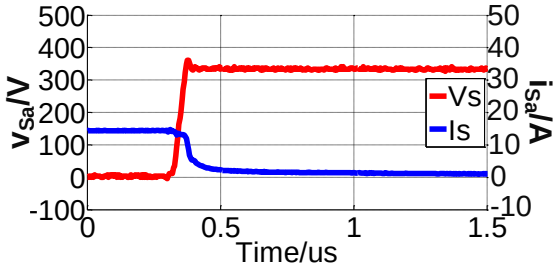


(c) Sa positive turn-on transition

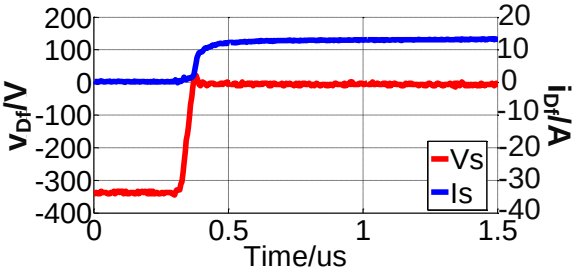


(d) Sb reverse turn-off transition

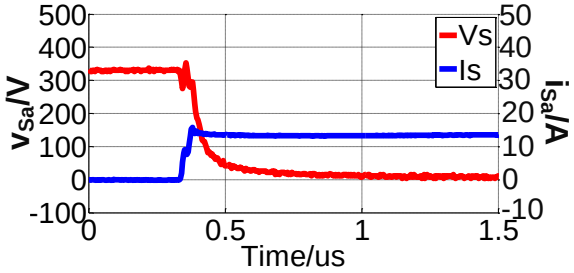
Fig. 6-4. Switching waveforms in the commutation between Sa (RB-IGBT) and Sb (RB-IGBT).



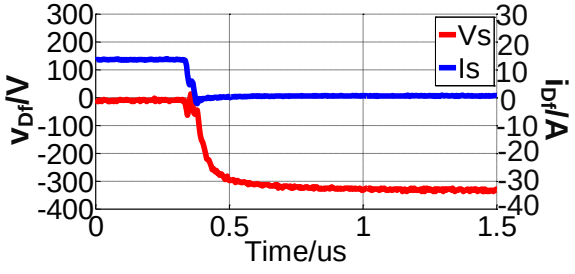
(a) Sa positive turn-off transition



(b) Df turn-on transition



(c) Sa positive turn-on transition



(d) Df turn-off transition

Fig. 6-5. Switching waveforms in the commutation between Sa (RB-IGBT) and Df (SiC Schottky diode).

6.2.1 Positive Turn-off and Reverse Turn-on

When Sa is turned off under positive voltage in Fig. 6-4(a) and Fig. 6-5(a), Sb (Fig. 6-4(b)) or the freewheeling diode Df (Fig. 6-5(b)) is turned on under reverse voltage. Also, as observed, there is a "tail current" on Sa due to the recombination of the accumulated carriers in the RB-IGBT, whose duration depends on the carrier lifetime and their recombination speed [124]. The voltage waveforms on the other hand have a large overshoot in the turn-on process of Sb due to the large ohmic resistance in RB-IGBT during the establishment of the conductivity modulation in the drift region [125][126], as shown in Fig. 6-4(b). It decays slowly to the on-state voltage once the charge carriers have been built up. There is no such phenomenon in Fig. 6-5(b) because the SiC Schottky diode Df is a majority carrier device.

The "tail current" of three different switches is compared in Fig. 6-6 when $V_{ab} = V_a - V_b = 340\ V$ and $I_{dc} = 10\ A$. The RB-IGBT has a larger "tail current" than the other two kinds of switches because of the longer carrier lifetime and the enhanced p+ layer on its collector [69][70][124]. Further, the amplitude of the voltage overshoot is closely related to the device physical characteristics as shown in Fig. 6-7, depicting the case when $V_{ab} = 340\ V$ and $I_{dc} = 15\ A$. Specifically, this figure shows how the minority carrier devices, such as Si PiN diode and IGBT, contribute to the voltage overshoot when the switch is turned on. This conduction modulation lagging effect is additive since a higher overshoot occurs when the IGBT is in series with a Si PiN diode than with a SiC Schottky. The higher overshoot of RB-IGBT in Fig. 6-7 is caused by the large width of the lightly doped drift region, which has higher resistance before the conduction modulation is established [126].

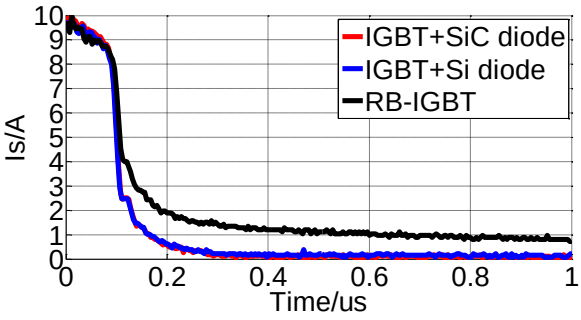


Fig. 6-6. "Tail current" comparison.

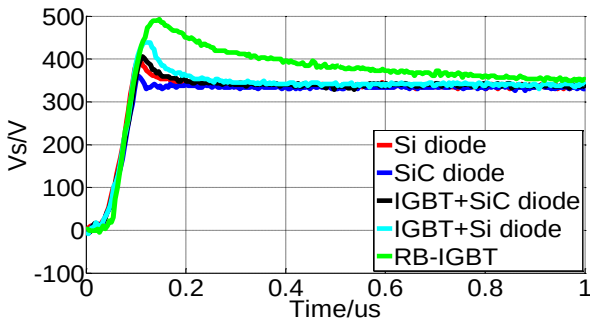


Fig. 6-7. Positive turn-off voltage comparison.

6.2.2 Positive Turn-on and Reverse Turn-off

When Sa is turned on under positive voltage in Fig. 6-4(c) and Fig. 6-5(c), Sb (Fig. 6-4(d)) or Df (Fig. 6-5(d)) is turned off under reverse voltage. As evinced, there is a large reverse recovery current when the RB-IGBT is reversely turned off in Fig. 6-4(d). On the contrary, since the SiC Schottky diode Df is a majority carrier device, it presents no reverse recovery process as shown in Fig. 6-5(d). As a result, the turn-on loss for Sa is high due to the current overshoot in Fig. 6-4(c), while much lower in Fig. 6-5(c).

Fig. 6-8 shows the turn-on current waveforms of Sa with different device configurations for the case when $V_{ab} = 340\ V$ and $I_{dc} = 17\ A$. As observed, the current overshoot is caused by reverse recovery process on Sb. The diode component in the switch arrangement, rather than the IGBT, has a larger influence on the current overshoot because it will take most of the reverse voltage. In the case of the RB-IGBT, there is a much larger current spike due to longer carrier lifetime that it exhibits when compared to the soft-recovery Si diode.

Further, in the turn-on waveforms in Fig. 6-4(c) and Fig. 6-4(c), the voltage on Sa has a steep drop at the beginning, which is caused by discharging the device junction capacitance. Then the voltage decays slowly to its on-state value, which is mainly due to the conduction

modulation establishment. The turn-on voltage decay of different switches is compared in Fig. 6-9, where the RB-IGBT showed the longest decay process when compared to conventional IGBTs.

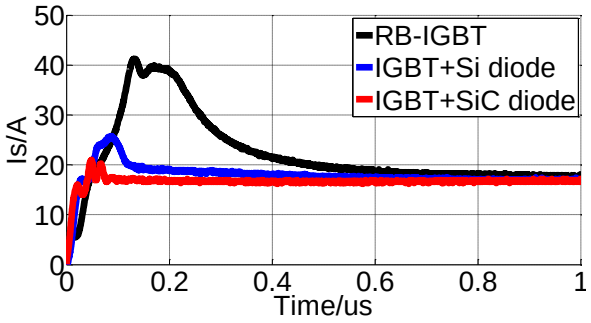


Fig. 6-8. Reverse recovery current comparison.

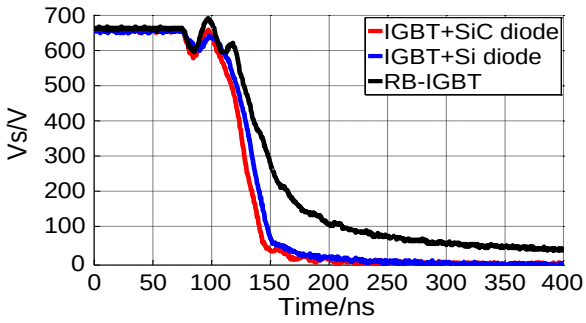


Fig. 6-9. Positive turn-on voltage comparison.

6.2.3 Switching Energy Comparison

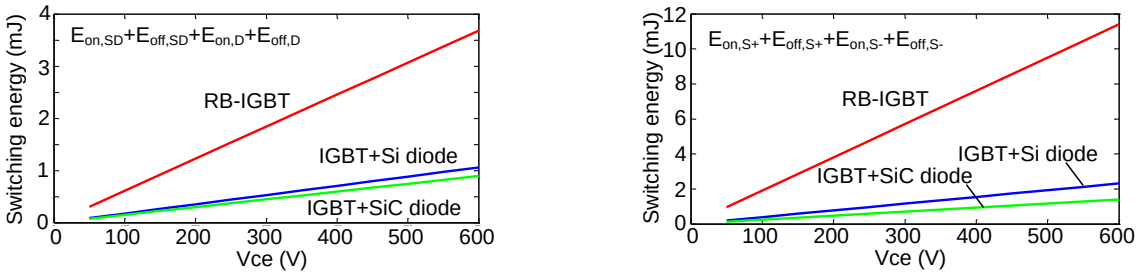
The switching energy under various commutation conditions are defined in Table 6-4. The measurement results under 15 A dc current and different device voltages are shown in Fig. 6-10.

Table 6-4. Switching energy in different commutations

Commutation condition		Turn-on	Turn-off
Between two switches	Switch ($v_{ce} \geq 0$)	$E_{on,S+}$	$E_{off,S+}$
	Switch ($v_{ce} < 0$)	$E_{on,S-}$	$E_{off,S-}$
Between switch and diode	Switch	$E_{on,SD}$	$E_{off,SD}$
	Diode	$E_{on,D}$	$E_{off,D}$

It can be seen that the RB-IGBT has the largest switching energy compared with the other two types of switches. The switching energy of the switch-switch commutation in Fig. 6-10(b) is

higher than that of the switch-diode commutation in Fig. 6-10(a). Based on the measurement results, the switching energy has a linear relationship with respect to the product of the device voltage v_{ce} and current i_{ce}, $E_x = k_x|v_{ce}i_{ce}|$, where k_x is the coefficient corresponding to E_x.



(a) Switch-diode commutation (b) Switch-switch commutation

Fig. 6-10. Switching energy comparison under different voltages.

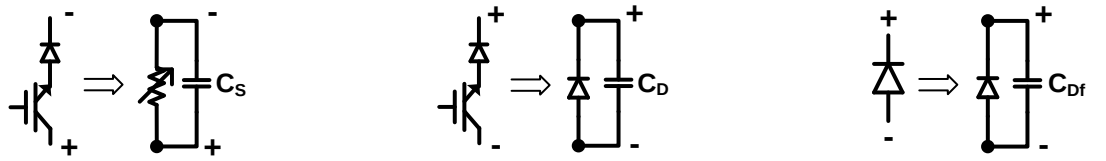
6.3 Switching Loss Model

To simplify the analysis, several assumptions and definitions are specified for the buck rectifier.

- The voltage on the input capacitor is assumed to be sinusoidal without switching ripple.
- The switching frequency f_s is much higher than the mains frequency $f = \frac{\omega}{2\pi}$.
- The dc-link current is assumed to be constant I_{dc}.
- The device junction capacitance does not exchange energy with the dc output since the switching transition takes place very quickly.
- The parasitic resistance in the circuit is negligible compared with the device on-resistance.
- The junction capacitance of semiconductor device is assumed to be constant in the analysis.

The analysis will cover both types of commutations in the buck rectifier. Besides, the junction capacitance of the non-switching devices will impact the performance of the switching devices in the rectifier [44][127]. Its contribution to the switching loss will be modeled as well.

In the analysis, the switch under positive voltage is modeled with a variable resistor and a capacitor C_S in parallel, as shown in Fig. 6-11(a). The resistor is used to calculate the real loss dissipated in the device channel and the capacitor is used to simulate the junction capacitance of the device. Under negative voltage, the switch can be seen as an ideal diode paralleled with its junction capacitor C_D, as shown in Fig. 6-11(b). Similarly, the freewheeling diode is modeled in Fig. 6-11(c).



(a) Switch under positive voltage

(b) Switch under negative voltage

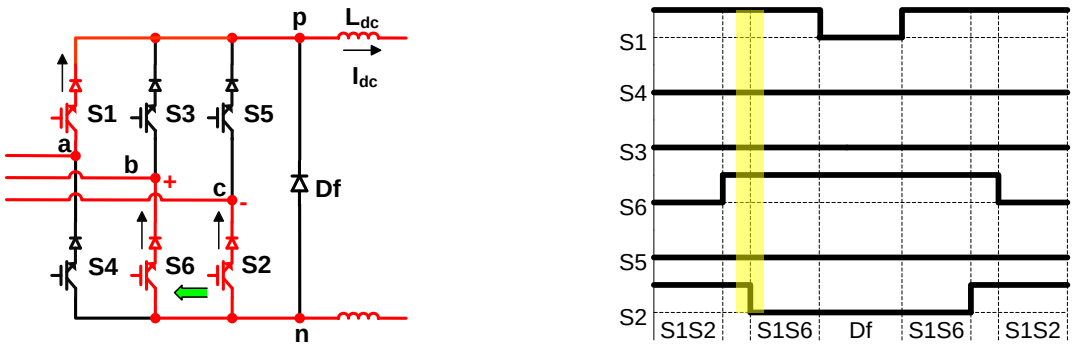
(c) Freewheeling diode

Fig. 6-11. Device equivalent circuits.

As an example, the transitions of the scheme SS-II are analyzed in Sector 1, where $-\varphi \leq \omega t < \pi/6, V_{ac} \geq V_{ab}$ and the space vector arrangement is $\overrightarrow{I_2} - \overrightarrow{I_1} - \overrightarrow{I_0} - \overrightarrow{I_1} - \overrightarrow{I_2}$.

1) Transition from S1S2 to S1S6

In this transition shown in Fig. 6-12, S2 is turned off under positive voltage, S6 is turned on under reverse voltage and S1 is kept on. The junction capacitance of S4 and the freewheeling diode Df will discharge from V_{ac} to V_{ab}.



(a) Commutation circuit (b) Device gate signals

Fig. 6-12. Transition from S1S2 to S1S6.

The analysis includes two steps in order to show the impact of the non-switching devices on the total switching loss. In the first step, only the commutating devices S2 and S6 are considered.

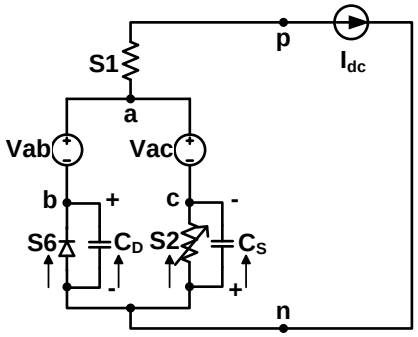


Fig. 6-13. Equivalent circuit of transition from S1S2 to S1S6 without non-switching devices.

The equivalent circuit of the transition is shown in Fig. 6-13. When S2 is turned off, its junction capacitance C_S is charged to V_{bc} and C_D in S6 is discharged to nearly zero. Then the diode in S6 starts to conduct and the current is commutated from S2 to S6. In this process, the dissipated energy E_{S1S2_S1S6} can be described by

$$E_{S1S2\_S1S6} = E_{on,S-} + E_{off,S+} + E_{S1,conduction} = E_{V_{ab}} + E_{V_{ac}} + E_{S6,C_D} - E_{S2,C_S} - E_{I_{dc}}$$

$$E_{S6,C_D} = \frac{1}{2} C_D V_{bc}^2$$

$$Q_{S6} = C_D V_{bc} \tag{6-2}$$

$$E_{S2,C_S} = \frac{1}{2} C_S V_{bc}^2$$

$$Q_{S2} = C_S V_{bc}$$

where E_{V_x} is the output energy of the voltage source $V_x, x = ac, ab, bc$. E_{Sx,C_D} is the energy stored in the junction capacitance C_D of the diode in the switch. E_{Sx,C_S} is the energy stored in the junction capacitance C_S of the IGBT. $E_{Df,C_{Df}}$ is the energy stored in the junction capacitance C_{Df} of the freewheeling diode. $E_{I_{dc}}$ is the output energy of the converter. $E_{Sx/Df,conduction}$ is the consumed conduction energy on Sx (x = 1,2,…,6) or Df. $Q_{Sx/Df}$ is the charge variation in the junction capacitance of the device Sx (x = 1,2,…,6) or Df.

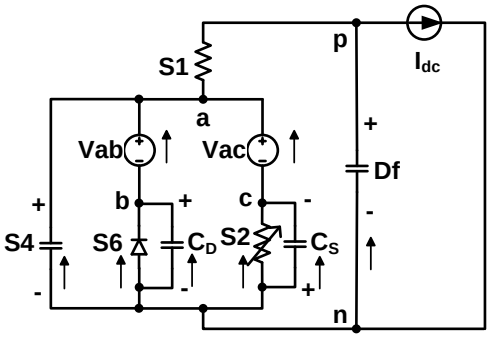


Fig. 6-14. Equivalent circuit of transition from S1S2 to S1S6 with non-switching devices.

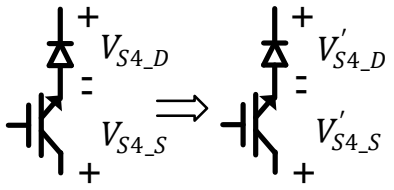


Fig. 6-15. Voltage change on S4.

When both the switching and the non-switching devices are taken into consideration, the equivalent circuit of the commutation can be redrawn as shown in Fig. 6-14, where S4 and Df

are modeled as a capacitor. Based on charge balance principle, the voltage change on S4 in Fig. 6-15 can be given by

$$\begin{aligned} V_{S4\_D} &= V_{ac} \\ V_{S4\_S} &= 0 \\ V'_{S4\_D} &= \frac{C_D V_{ac} + C_S V_{ab}}{C_D + C_S} \\ V'_{S4\_S} &= \frac{C_D V_{bc}}{C_D + C_S} \end{aligned} \tag{6-3}$$

The output energy of the source V_{ac} and the dissipated energy on S2 and S1 are reduced due to discharging current in the junction capacitance of S4 and Df. The dissipated energy E'_{S1S2_S1S6} in the transition can be given by

$$\begin{aligned} E'_{S1S2\_S1S6} &= E_{on,S-} + E'_{off,S+} + E'_{S1,conduction} \\ &= E_{V_{ab}} + E'_{V_{ac}} + E_{S6,C_D} - E_{S2,C_S} - E_{I_{dc}} + E_{S4,C_D} + E_{S4,C_S} + E_{Df,C_{Df}} \end{aligned}$$

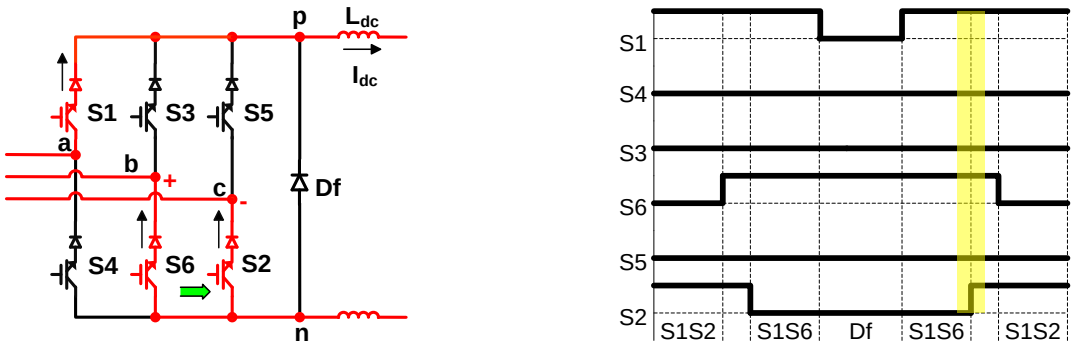
$$\begin{aligned} E'_{V_{ac}} &= E_{V_{ac}} - V_{ac}\left(Q_{S4} + Q_{Df}\right) \\ E_{S4,C_D} + E_{S4,C_S} &= \frac{C_D C_S (V_{ac}^2 - V_{ab}^2)}{2(C_D + C_S)} \\ E_{Df,C_{Df}} &= \frac{1}{2} C_{Df} (V_{ac}^2 - V_{ab}^2) \\ Q_{S4} &= \frac{V_{bc} C_D C_S}{C_D + C_S} \\ Q_{Df} &= C_{Df} V_{bc} \end{aligned} \tag{6-4}$$

Comparing (6-2) and (6-4), the reduced switching energy when considering the non-switching devices can be given by

$$\begin{aligned} \Delta E_{S1S2\_S1S6} &= E_{S1S2\_S1S6} - E'_{S1S2\_S1S6} = E_{V_{ac}} - \left(E'_{V_{ac}} + E_{S4,C_D} + E_{S4,C_S} + E_{Df,C_{Df}}\right) \\ &= \frac{(V_{ab} - V_{ac})^2 \left(C_D C_{Df} + C_D C_S + C_S C_{Df}\right)}{2(C_D + C_S)} \end{aligned} \tag{6-5}$$

2) Transition from S1S6 to S1S2

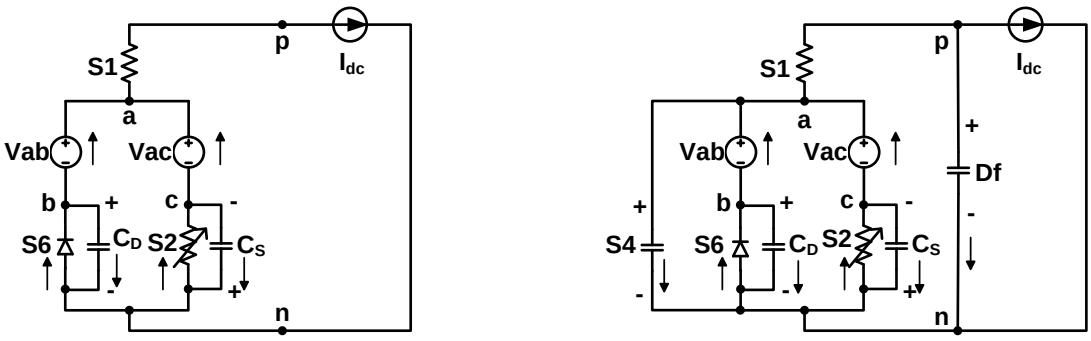
Complementary to the previous transition, S2 is turned on and S6 is turned off, as shown in Fig. 6-16. The junction capacitance of S4 and the freewheeling diode Df will be charged from V_{ab} to V_{ac}.



(a) Commutation circuit (b) Device gate drive signal

Fig. 6-16. Transition from S1S6 to S1S2.

The equivalent circuit with and without non-switching devices (S4 and Df) can be drawn in Fig. 6-17(a) and (b) respectively. The output energy of the source V_{ac} and the dissipated energy on S2 and S1 are increased due to the current that charges the junction capacitance of S4 and Df.



(a) Without non-active devices (b) With non-active devices

Fig. 6-17. Equivalent circuit of transition from S1S6 to S1S2.

In the circuit in Fig. 6-17(a), the dissipated energy E_{S1S6_S1S2} in the transition can be given by

$$E_{S1S6\_S1S2} = E_{off,S-} + E_{on,S+} + E_{S1,conduction} = E_{V_{ab}} + E_{V_{ac}} + E_{S2,C_S} - E_{S6,C_D} - E_{I_{dc}}$$

$$\begin{aligned} E_{S6,C_D} &= \frac{1}{2} C_D V_{bc}^2 \\ Q_{S6} &= C_D V_{bc} \\ E_{S2,C_S} &= \frac{1}{2} C_S V_{bc}^2 \\ Q_{S2} &= C_S V_{bc} \end{aligned} \tag{6-6}$$

With non-switching devices in Fig. 6-17(b), the dissipated energy E'_{S1S6_S1S2} can be given by

$$\begin{aligned} E'_{S1S6_{S1S2}} &= E_{off,S-} + E'_{on,S+} + E'_{S1,conduction} \\ &= E_{V_{ab}} + E'_{V_{ac}} + E_{S2,C_S} - E_{S6,C_D} - E_{I_{dc}} - E_{S4,C_D} - E_{S4,C_S} - E_{Df,C_{Df}} \end{aligned}$$

$$\begin{aligned} E'_{V_{ac}} &= E_{V_{ac}} + V_{ac}\left(Q_{S4} + Q_{Df}\right) \\ E_{S4,C_D} + E_{S4,C_S} &= \frac{C_D C_S (V_{ac}^2 - V_{ab}^2)}{2(C_D + C_S)} \\ E_{Df,C_{Df}} &= \frac{1}{2} C_{Df} (V_{ac}^2 - V_{ab}^2) \\ Q_{S4} &= \frac{V_{bc} C_D C_S}{C_D + C_S} \\ Q_{Df} &= C_{Df} V_{bc} \end{aligned} \tag{6-7}$$

With the two-step analysis, the increased energy dissipation caused by non-switching devices can be given by

$$\Delta E_{S1S6\_S1S2} = E'_{S1S6\_S1S2} - E_{S1S6\_S1S2} = \frac{(V_{ab} - V_{ac})^2 \left(C_D C_{Df} + C_D C_S + C_S C_{Df}\right)}{2(C_D + C_S)} \tag{6-8}$$

Comparing (6-5) and (6-8), $\Delta E_{S1S2\_S1S6} = \Delta E_{S1S6\_S1S2}$, $E_{S1S2\_S1S6} + E_{S1S6\_S1S2} = E'_{S1S2\_S1S6} + E'_{S1S6\_S1S2}$. The impact of the non-switching devices on the switching loss cancels

each other in the two complementary transitions. Similarly, the other two transitions can be analyzed and the total switching energy in a switching period of Sector 1 is given by

$$\begin{aligned} E_{Sector\ 1} &= E_{on,S-} + E_{off,S+} + E_{on,S+} + E_{off,S-} + E_{on,SD} + E_{off,D} + E_{off,SD} + E_{on,D} \\ &= \left(k_{on,S-} + k_{off,S+} + k_{on,S+} + k_{off,S-}\right)|V_{bc}I_{dc}| \\ &\quad + \left(k_{on,SD} + k_{off,D} + k_{off,SD} + k_{on,D}\right)|V_{ab}I_{dc}| \end{aligned} \tag{6-9}$$

In the same way, the switching energy can be derived in Sector 12 ($-\pi/6 \le \omega t < -\varphi, v_{ac} < v_{ab}$) as

$$\begin{aligned} E_{Sector\ 12} &= \left(k_{on,S-} + k_{off,S+} + k_{on,S+} + k_{off,S-}\right)|V_{bc}I_{dc}| \\ &\quad + \left(k_{on,SD} + k_{off,D} + k_{off,SD} + k_{on,D}\right)|V_{ac}I_{dc}| \end{aligned} \tag{6-10}$$

Considering the symmetry in the modulation scheme, the total switching loss can be calculated from these two consecutive sectors by

$$P_{switching} = \frac{3f_s}{\pi}\left(\int_{-\varphi}^{\pi/6} E_{Sector1}\, d(\omega t) + \int_{-\pi/6}^{\varphi} E_{Sector12}\, d(\omega t)\right) \tag{6-11}$$

The non-switching devices do cause higher switching loss in the asymmetric PWM schemes. The increased loss can be approximated by (6-12), assuming $\varphi = 0$. It is still very small compared with the total switching loss.

$$\Delta P_{switching} = \frac{9}{2\pi} V_m^2 C_S f_s \left(\frac{3}{4} - \frac{\pi}{6}\right) \tag{6-12}$$

The switching loss of all four modulation schemes is derived and the results are compared in Table 6-5, where the phase angle φ is within $-\pi/6$ to $\pi/6$ for non-regenerative applications.

Table 6-5. Switching loss equations of different modulation schemes

Modulation scheme	**Total switching loss**
Symmetric Scheme I (SS-I)	$P = (9V_m f_s I_{dc}/\pi)\left(k_{on,SD} + k_{off,SD} + k_{on,D} + k_{off,D}\right)cos\varphi$
Symmetric Scheme II (SS-II)	$P = \left(3\sqrt{3}V_m f_s I_{dc}/\pi\right)\left[\left(2-\sqrt{3}cos\varphi\right)\left(k_{on,S-} + k_{on,S+} + k_{off,S-} + k_{off,S+}\right) + \left(\sqrt{3}cos\varphi - 1\right)\left(k_{on,SD} + k_{on,D} + k_{off,SD} + k_{off,D}\right)\right]$
Asymmetric Scheme III (US-III)	$P = \left(3\sqrt{3}V_m f_s I_{dc}/\pi\right)\left[\left(2-\sqrt{3}cos\varphi\right)\left(k_{on,S+} + k_{off,S-}\right) + \left(\sqrt{3}cos\varphi - 1\right)\left(k_{on,SD} + k_{off,D}\right) + \left(k_{off,SD} + k_{on,D}\right)\right]$
Asymmetric Scheme IV (US-IV)	$P = \left(3\sqrt{3}V_m f_s I_{dc}/\pi\right)\left[\left(2-\sqrt{3}cos\varphi\right)\left(k_{on,S-} + k_{off,S+}\right) + \left(\sqrt{3}cos\varphi - 1\right)\left(k_{on,D} + k_{off,SD}\right) + \left(k_{on,SD} + k_{off,D}\right)\right]$

6.4 Comparison of Modulation Schemes Considering Different Device Combinations

From the derived switching loss equations in Table 6-5, it can be seen that the relative loss between modulation schemes is mainly determined by the phase angle φ and three following parameters

$$k_1 = \left(k_{on,S-} + k_{off,S+} + k_{on,S+} + k_{off,S-}\right)/\left(k_{on,SD} + k_{off,D} + k_{off,SD} + k_{on,D}\right)$$
$$k_2 = \left(k_{on,S+} + k_{off,S-}\right)/\left(k_{on,S-} + k_{off,S+}\right) \quad (6\text{-}13)$$
$$k_3 = \left(k_{on,SD} + k_{off,D}\right)/\left(k_{off,SD} + k_{on,D}\right)$$

k_1 is the ratio between the switching energy in the switch-switch commutation and the one in the switch-diode commutation under the same voltage and current conditions.

k_2 is the ratio between the switching energy in the positive turn-on process and the one in the positive turn-off process of the switch-switch commutation under the same voltage and current conditions.

k_3 is the ratio between the switching energy in the positive turn-on process and the one in the positive turn-off process of the switch-diode commutation under the same voltage and current conditions.

Fig. 6-18, Fig. 6-19 and Fig. 6-20 give the switching loss comparison of the four modulation schemes. The switching loss of SS-II when $k_1 = k_2 = k_3 = 1$ and $\varphi = 0$ is selected as the base for all three figures.

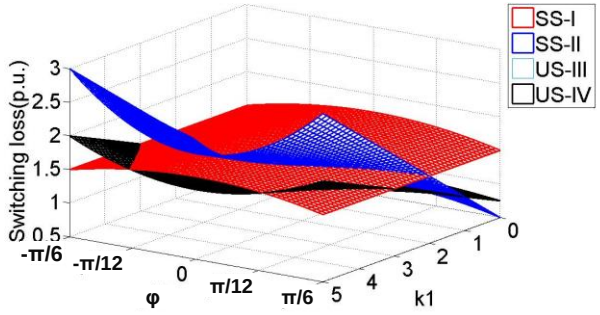


Fig. 6-18. Switching loss vs. k1 and φ.

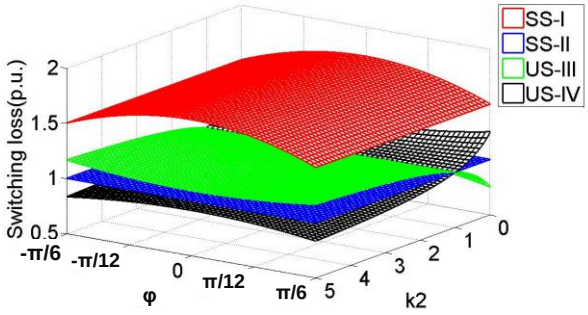


Fig. 6-19. Switching loss vs. k2 and φ.

In Fig. 6-18, the switching loss varies with k_1 and φ when $k_2 = k_3 = 1$. In this case, the switching loss of US-III and US-IV are the same. SS-I has lower loss than SS-II when k_1 becomes larger than 3, indicating that the switch-switch commutation has 3 times switching energy of the switch-diode commutation. Because SS-I has no commutations between switches, it can save much switching loss when k_1 is large.

Fig. 6-19 shows the variation of the switching loss with k_2 and φ when $k_1 = k_3 = 1$. In this case, the switching loss of SS-I is higher than the other three schemes. US-IV has the lowest loss when k_2 is larger than 1 since it has no positive turn-on process in the switch-switch commutation. It is suitable for application when some minority carrier device such as Si PiN

diode or RB-IGBT is used in the switch and there is large reverse recovery current in the positive turn-on transition (Fig. 6-8). Otherwise, US-III has lower loss because it has no positive turn-off process in the switch-switch commutation. The voltage overshoot (Fig. 6-7) and "tail current" (Fig. 6-6) will increase the switching loss in positive turn-off process. And Fig. 6-20 shows the variation of the switching loss with k_3 and φ when $k_1 = k_2 = 1$. The switching loss of US-III is the lowest when k_3 is larger than 1. Otherwise US-IV has the lowest switching loss.

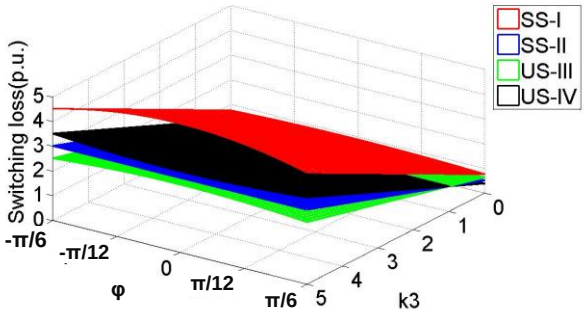


Fig. 6-20. Switching loss vs. k3 and φ.

For the three-phase buck rectifier without freewheeling diode, the switching loss expressions in Table 6-5 can be simplified by setting $k_1 = 1$ and $k_2 = k_3$. In this case, the switching loss of SS-II, US-III and US-IV are all the same, which is $\sqrt{3}$ times of that of SS-I.

Table 6-6. Coefficients of different device combinations

No.	Switch Sx	D	k1	k2	k3
1	RB-IGBT	SiC Schottky diode	3.10	1.51	0.37
2	IGBT and Si soft-recovery diode		2.18	0.83	0.55
3	IGBT and SiC Schottky diode		1.56	0.49	0.57

The coefficients k_1, k_2 and k_3 of three device combinations are calculated based on the measurement results and shown in Table 6-6. k_1 is larger than 1 in all the combinations. RB-IGBT has the largest k_1 because its switching speed is much lower than normal IGBTs, causing more loss in the switch-switch commutation. k_1 can be reduced by employing a majority carrier device, such as the SiC Schottky diode, in series with the switch. k_2 is larger than 1 for the RB-IGBT case, indicating that the positive turn-on loss is higher than the positive turn-off loss in the commutation between two RB-IGBTs, where the large reverse recovery current of the RB-IGBT contributes mostly to this loss. In other cases, $k_2 < 1$ and $k_3 < 1$.

The switching loss comparison of four modulation schemes with different device combinations is shown in Fig. 6-21 to Fig. 6-23, where the switching loss of SS-II when $\varphi = 0$ in Fig. 6-21 is selected as basis. In the two asymmetric modulation schemes, US-IV is advantageous for RB-IGBT and IGBT + Si diode cases as shown in Fig. 6-21 and Fig. 6-22 respectively. US-III is more efficient for IGBT + SiC diode as shown in Fig. 6-23.

In the two symmetric modulation schemes, SS-I has lower switching loss for RB-IGBT, especially when φ is far from zero. When normal IGBT are used, SS-II has lower switching loss because of its lower voltage stress.

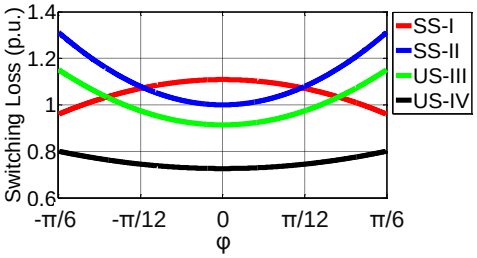


Fig. 6-21. Switching loss comparison with RB-IGBT.

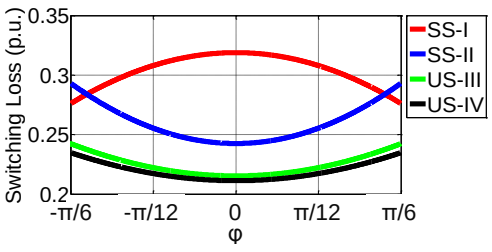


Fig. 6-22. Switching loss comparison with IGBT + Si diode.

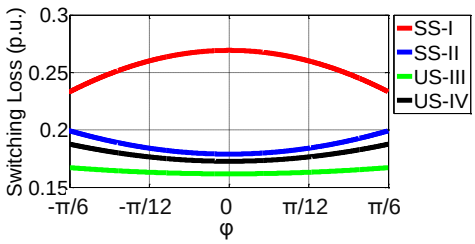


Fig. 6-23. Switching loss comparison with IGBT + SiC diode.

In the design of a unity-power-factor three-phase buck rectifier, the phase angle φ can be controlled to compensate the displacement factor caused by the input filter of the converter. For the buck rectifier with specifications per Table 6-7, the change of φ with output power is shown in Fig. 6-24, and the switching losses of the four schemes under different output power in Fig. 6-25. RB-IGBT devices were used in this case with SiC Schottky as freewheeling diode. It is shown that US-IV has lowest loss over the whole output power range.

Table 6-7. Buck rectifier parameters

Parameter	**Value**
Input line voltage	480 Vrms
Output dc voltage	400 V
Maximum output power	6 kW
Maximum dc current	15 A
Input capacitor C_i	6 μF
Input inductance L_i	110 μH
DC-link inductance L_{dc}	1.9 mH
Switching frequency f_s	10 kHz

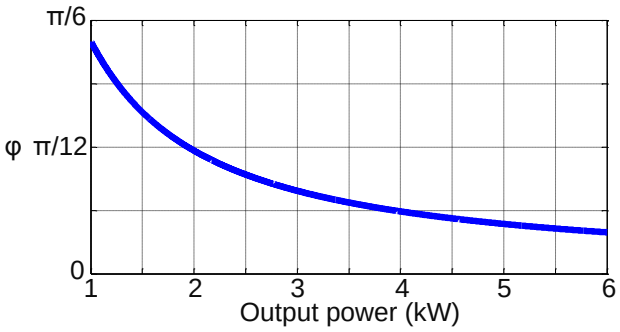


Fig. 6-24. Change of φ with output power.

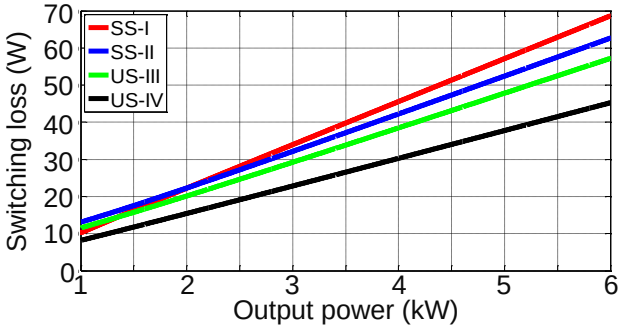


Fig. 6-25. Switching loss comparison in 6 kW buck rectifier.

6.5 Conclusion

In this chapter, the different commutation types of a three-phase buck rectifier with a freewheeling dc-bus diode were analyzed through experiments. The lossiest transition was accordingly identified for the different semiconductor device configurations considered. Then the switching loss of the buck rectifier was modeled, including both the switch-switch and switch-diode commutations, and the effect of the non-switching devices, where the latter was shown to be negligible compared to the total switching loss. Based on the derived switching loss equations, four modulation schemes were compared for different device combinations, showing how space vectors could be arranged to eliminate the transitions with the highest switching losses. Several guidelines were finally drawn for the selection of the highest efficiency modulation scheme for three-phase buck rectifiers, namely

- When minority carrier devices such as RB-IGBT and Si PiN diode are applied in the switches, the switching loss in the switch-switch commutation is usually much larger than that in the switch-diode commutation, due to severe reverse recovery current and the

conduction modulation lagging effect. A modulation scheme such as the Symmetric Scheme I with no switch-switch commutations is recommended in this case.

- When majority carrier devices such as SiC Schottky diodes are used in the switches, the loss difference between both types of commutations is marginal if noticeable. In this case, the voltage stress on the switches is the dominant factor deciding the switching loss. A modulation scheme such as the Symmetric Scheme II with minimized voltage stress will have higher efficiency in consequence.
- When the loss caused by the reverse recovery current is large in the positive turn-on process, the modulation scheme such as Asymmetric Scheme IV is recommended, because it has no positive turn-on process in the switch-switch commutation.
- When the loss caused by the "tail current" and conduction modulation lagging effect is large in the positive turn-off process, the modulation scheme such as Asymmetric Scheme III is recommended. Because it has no positive turn-off process in the switch-switch commutation.

7 Compensation of Input Current Distortion

In this chapter, the current distortion caused by the overlap time is analyzed first. A modified pulse-based method is proposed for the overlap time compensation. The commutation in the buck rectifier is modeled, and a minimized overlap time is proposed. Based on the model, the compensation pulse width can be generated under different switching voltage and current. The proposed method is verified through experiments in a 7.5 kW all-SiC buck rectifier.

7.1 Distortion Caused by Overlap Time

The commutation in the buck rectifier occurs between the upper three switches (S1, S3, and S5) or the lower three switches (S4, S6, and S2) in the buck rectifier. The basic commutation unit can be drawn in Fig. 7-1, containing two switches Sx and Sy. The voltage sources Vx and Vy indicate two phase voltages, and I_{dc} is the DC current on the inductor L_{dc}. In Fig. 7-2, a double pulse test circuit is built based on Fig. 7-1 to study the commutation under different operating conditions. The active switches are 1200 V SiC MOSFETs, CMF20120D, from Cree [82], and the series diodes are 1200 V SiC Schottky barrier diodes (SBDs), SDP60S120D, from SemiSouth.

Fig. 7-1. Commutation unit in buck rectifier: (a) Circuit schematic; (b) Gate signals.

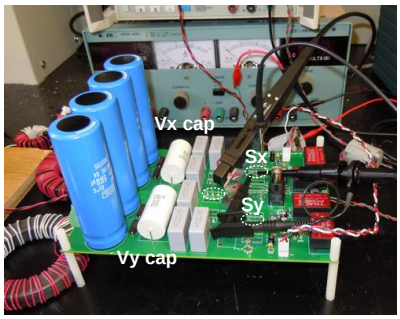


Fig. 7-2. Device double pulse test board.

The commutation between S1 and S3 in Sector 2 and 3 are taken as an example. The typical gate signals are shown in Fig. 7-3 for S1 and S3. The overlap time t_Δ is added on the reference gate signals of S1 and S3 to prevent the interruption of DC inductor current, as shown in Fig. 7-3.

When $v_{ab} \geq 0$, the transition happens when S1 switches at t_1 and t_6 rather than the ideal moment t_2 and t_5, resulting in a gain in the input current i_a and a loss in i_b. When $v_{ab} < 0$, the transitions occur at t_3 and t_4 when S3 switches, rather than the ideal moment t_2 and t_5, resulting in a loss in i_a and a gain in i_b. This gain and loss will cause distortion of the fundamental component of the input current in Fig. 7-4, where the effect of the overlap time toggles when v_{ab} or v_{ac} cross zero.

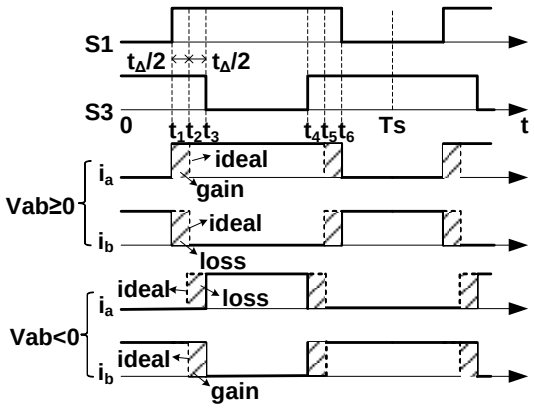


Fig. 7-3. Overlap time distortion.

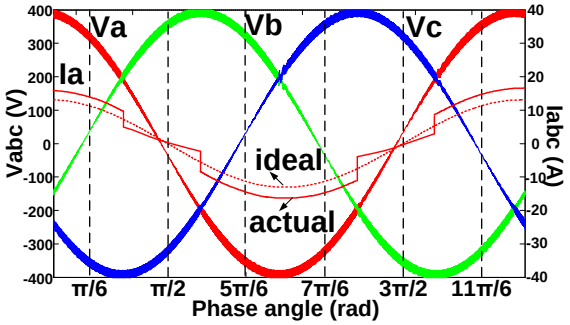


Fig. 7-4. Input current distortion.

7.2 Modified Pulse-Based Compensation Method

The traditional pulse-based compensation method adds the overlap time to the gate signal of the switch which bears reverse voltage. It depends on the polarity of the line-to-line voltage. As shown in Fig. 7-5, the gate pulse width of S3 is added by $2t_\Delta$ to compensate the overlap time in Sector 2 when $v_{ab} \geq 0$. The input current will have no distortion since the transition happens at the ideal moment t_2 and t_5. Similarly, the overlap time is added on the S1 gate signal in Sector 3 when $v_{ab} < 0$. The traditional compensation method assumes that the commutation time is much smaller than the pulse width and can be omitted.

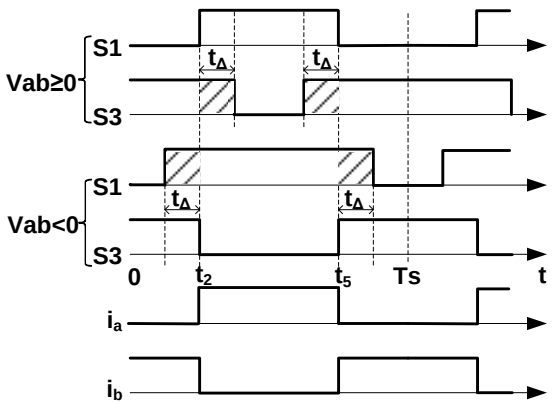


Fig. 7-5. Traditional compensation.

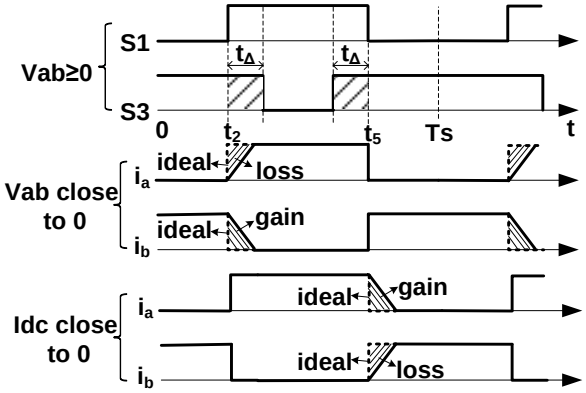
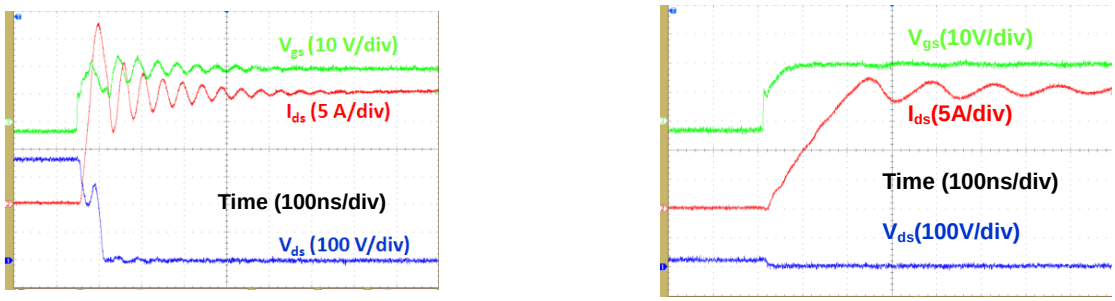


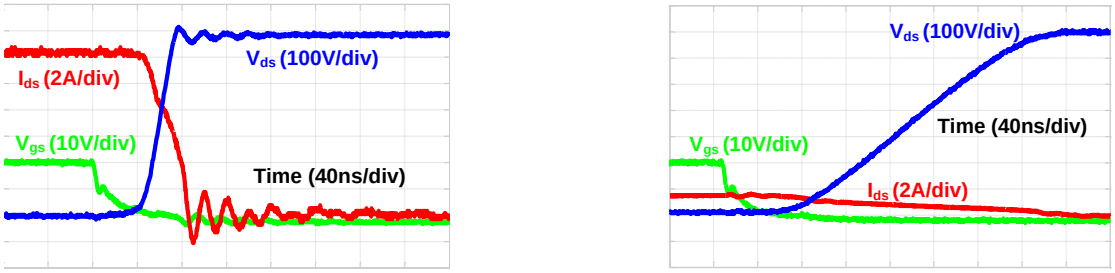
Fig. 7-6. Slow transition distortion.

However, the commutation time will become much longer and cannot be ignored when the line-to-line voltage is crossing zero or the DC current is small under light load, as shown in Fig. 7-6. Under these conditions, the traditional method is not enough to compensate for the overlap time effect. The turn-on waveforms of Sx are measured in the double pulse test (Fig. 7-1 and Fig. 7-2) and shown in Fig. 7-7(a) when v_{xy} = 340 V and I_{dc} = 20 A. In Fig. 7-7(b), v_{xy} = 10 V and I_{dc} = 20 A. The rise time of I_{ds} is more than 200 ns in Fig. 7-7(b), ten times of that shown in Fig. 7-7(a). The turn-off waveforms of Sx are shown in Fig. 7-8 when v_{xy} = 680 V. The fall time of I_{ds} is 40 ns when I_{ds}= 12 A in Fig. 7-8(a) while 280 ns when I_{ds} = 1.5 A in Fig. 7-8(b).



(a) (b)

Fig. 7-7. Measured turn-on waveforms: (a) v_{xy} = 340 V, I_{dc} = 20 A; (b) v_{xy} = 10 V, I_{dc} = 20 A.



(a) (b)

Fig. 7-8. Measured turn-off waveforms: (a) v_{xy} = 680 V, I_{dc} = 12 A; (b) v_{xy} = 680 V, I_{dc} = 1.5 A.

A modified pulse-based compensation method is proposed to compensate the overlap time. As shown in Fig. 7-9, two more modules are added to the traditional method. First, the minimum overlap time t_Δ is selected for the gate signal to speed up the transition and reduce the compensation effort. The commutation process is modeled to generate the compensation pulse width t_c according to line-to-line voltage v_{xy}, dc current I_{dc}, and the overlap time t_Δ. Finally the ideal reference pulse width t_x^* is added by $2t_\Delta$ and t_c to get the actual reference pulse width t_x, which is sent to the modulator.

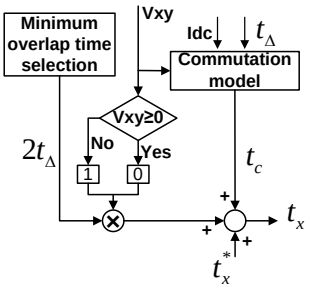


Fig. 7-9. Modified pulse-based compensation method.

7.3 Commutation Analysis in Buck Rectifier

To model the commutation in the buck rectifier, the theoretical turn-on waveform of Sx is shown in Fig. 7-10 when $v_{xy} \geq 0$ [124]. When the parasitic inductance $L_p$is not considered, the channel current of the MOSFET is proportional with the gate voltage from t_1 to t_2, as the solid line shown in Fig. 7-10. The gate charge time is proportional to the gate resistor R_G and the input capacitor C_{iss} (including gate-source capacitor C_{GS} and gate-drain capacitor C_{GD}).

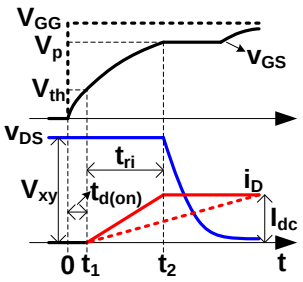


Fig. 7-10. Theoretical turn-on waveform of Sx.

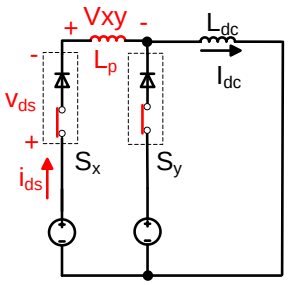


Fig. 7-11. Sx turn-on circuit with parasitic inductance.

When $L_p$is considered, the current rise time will be increased when the switching voltage is low, as the dash line shown in Fig. 7-10. In this case, the voltage v_{xy} is distributed on the parasitic inductance L_p in Fig. 7-11. The current rise time can be written as $I_{dc}L_p/v_{xy}$.

The current rise time t_{ri} of Sx is determined by the larger of the two and is given by $t_{ri} = max(2\tau, I_{dc}L_p/v_{xy})$, where $\tau = R_G(C_{GD} + C_{GS})$. When v_{xy} is small, t_{ri} is predominantly $I_{dc}L_p/v_{xy}$. The charge loss of Sx or the charge gain of Sy can be approximated by $t_{ri}I_{dc}/2$.

Conservatively, Sy should be kept on until current is fully commutated to Sx when $v_{xy} \geq 0$. The overlap time t_Δ should be larger than t_{ri}, which is long when v_{xy} is close to zero.

Actually it is possible to accelerate the turn-on process of Sx with careful selection of t_Δ . If t_Δ is set to the gate charge time 2τ, the gate of S1 has reached the turn-on voltage at the end of overlap time although its current has not reached I_{dc}. When Sy is turned off, the DC inductor will force the current to be commutated to Sx.

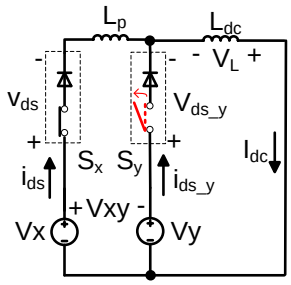


Fig. 7-12. Sx turn-on circuit with reduced overlap time.

The commutation with reduced overlap time can be described with the equivalent circuit in Fig. 7-12. When Sy is turned off, the related current and voltage in the commutation can be

expressed by (7-1) where g_{fs} is the transconductance of the MOSFET, v_{gs_y} the gate-source voltage of Sy, and V_{GG} the gate drive voltage.

$$\begin{cases} v_L + v_x = v_{ds} + L_p \dfrac{di_{ds}}{dt} \\ v_y + v_L = v_{ds\_y} \\ i_{ds} + i_{ds\_y} = I_{dc} \\ \dfrac{di_{ds\_y}}{dt} = g_{fs} \dfrac{dv_{gs\_y}}{dt} \\ v_{gs\_y} = V_{GG} e^{-t/\tau} \end{cases} \tag{7-1}$$

In this transition, the voltage on Sx has already dropped to a low value, so v_{ds} can be ignored in (7-1). The voltage spike on Sy can be given by (7-2) and is proportional to the gate turn off speed of Sy and the parasitic inductance L_p.

$$v_{ds\_y} = -L_p g_{fs} \frac{dv_{gs}}{dt} - v_{xy} < \frac{L_p g_{fs} V_{GG}}{R_G C_{iss}} - v_{xy} \tag{7-2}$$

The experimental waveforms of the turn on process under different overlap times are shown in Fig. 7-13, Fig. 7-14, and Fig. 7-15 when v_{xy} = 10 V and I_{dc} = 20 A. The overlap time, current rise time, and voltage spike on Sy are listed in Table 7-1. When overlap time is 550 ns in Fig. 7-15, there is no voltage spike on Sy.

Table 7-1. Switching characteristics with different overlap time

Overlap Time	**Current Rise Time**	**Voltage Spike on Sy**
10 ns	70 ns	70 V
150 ns	180 ns	25 V
550 ns	270 ns	-

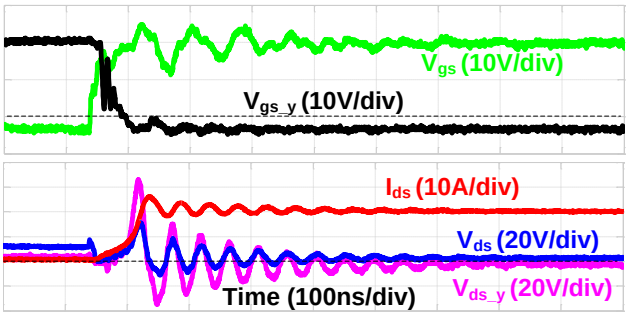


Fig. 7-13. Turn on with 10 ns overlap time.

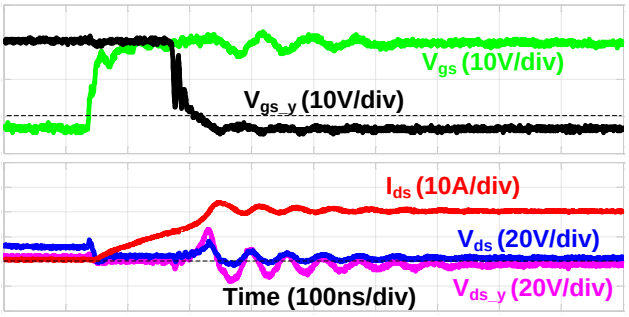


Fig. 7-14. Turn on with 150 ns overlap time.

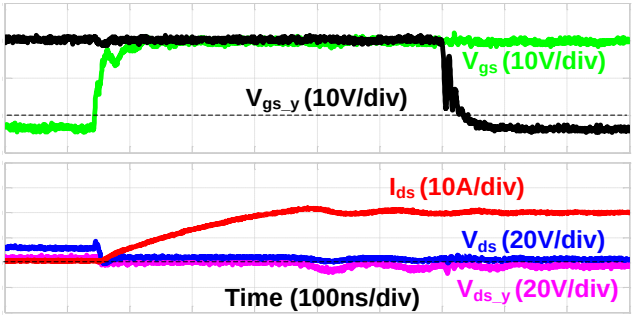


Fig. 7-15. Turn on with 550 ns overlap time.

In Fig. 7-13 and Fig. 7-14, it is obvious that the slope of I_{ds} will increase when Sy is turned off. The commutation is accelerated while the voltage spike is affordable.

With reduced overlap time, the commutation can be accelerated and the charge loss can be largely reduced. The compensation time for the turn-on process of Sx can be expressed by (7-3) when $v_{xy} \geq 0$.

$$ON\_offset(v_{xy}, I_{dc}) = \begin{cases} max\left(\tau, \frac{I_{dc}L_p}{2v_{xy}}\right), when\ \frac{I_{dc}L_p}{v_{xy}} \leq t_\Delta \\ max\left(\tau, t_\Delta\left(1 - \frac{t_\Delta v_{xy}}{2L_p I_{dc}}\right)\right), when\ \frac{I_{dc}L_p}{v_{xy}} > t_\Delta \end{cases} \quad (7\text{-}3)$$

The theoretical turn-off waveform of Sx is shown in Fig. 7-16 when $v_{xy} \geq 0$ [124]. Before Sx is turned off, Sy has been turned on although there is no current flowing in it. In this commutation, the overlap time should be long enough for the gate of S3 to be charged.

If the junction capacitor on Sy is not considered, Sx current will not drop until v_{ds} is charged to v_{xy}, as the solid line shown in Fig. 7-16. The channel current of the MOSFET in Sx is proportional with its gate voltage from t_1 to t_2. The current fall time t_{fi} can be approximated by 2τ.

But in the actual circuit, the junction capacitor on Sy will always delay the voltage increase on Sx, as the dash line shown in Fig. 7-16. The equivalent circuit can be drawn in Fig. 7-17, where C_{p1} and C_{p2} are mainly the output capacitance of the devices. C_{p1} includes the drain-source capacitance C_{DS} and gate-drain capacitance C_{GD} of the MOSFET. C_{p2} is the junction capacitance of the series diode. When Sx is turned off, C_{p1} will be charged and C_{p2} will be discharged by the DC current. The charge or discharge time can be approximated by $v_{xy}C_p/I_{dc}$, where $C_p = C_{p1} + C_{p2}$.

The current fall time t_{fi} of Sx is determined by the larger of the two and is given by $t_{fi} = max(2\tau, v_{xy}C_p/I_{dc})$. When v_{xy} is large and I_{dc} is small, t_{fi} is predominantly $v_{xy}C_p/I_{dc}$. The charge gain of Sx or the charge loss of Sy can be approximated by $t_{ri}I_{dc}/2 + t_{d(off)}I_{dc}$.

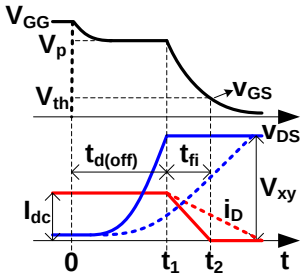


Fig. 7-16. Theoretical turns-off waveform of Sx.

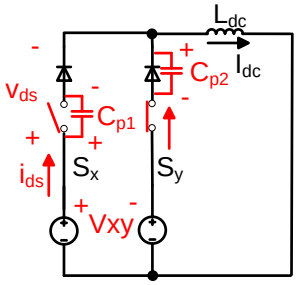


Fig. 7-17. Sx turn-off circuit with parasitic capacitance.

The compensation time for turn-off process of Sx can be expressed by (7-4) when $v_{xy} \geq 0$. Its pulse width should be reduced when $v_{xy} \geq 0$. The junction capacitance is a function of the voltage on the device [82]. A look-up table is built in a digital signal processor to estimate C_p under different voltage conditions.

$$OFF\_offset(v_{xy}, I_{dc}) = -t_{d(off)} - max\left(\tau, \frac{v_{xy}C_p(v_{xy})}{2I_{dc}}\right) \quad (7\text{-}4)$$

7.4 Application of Proposed Compensation Method

Based on the analysis above, the minimum overlap time t_Δ is the gate charge time $2R_G(C_{GD} + C_{GS})$ for both the turn-on and turn-off process. The compensation time t_c for Sx is $ON\_offset(v_{xy}, I_{dc}) + OFF\_offset(v_{xy}, I_{dc})$ when $v_{xy} \geq 0$. Meanwhile, the pulse width of Sy should be reduced by $ON\_offset(v_{xy}, I_{dc}) + OFF\_offset(v_{xy}, I_{dc})$ when $v_{xy} \geq 0$.

Take S1 as an example. S1 has switching behavior in 180° of a line period. The compensation pulse width in 6 sectors is listed in Table 7-2 for S1 and its complementary switch. The modulation scheme is Modified Fullwave Symmetrical Modulation (MFSM) [94].

Table 7-2. Compensation pulse width

Sector	Compensation Pulse Width		Voltage
10	S1	$-ON\_offset(v_{ca}, I_{dc}) - OFF\_offset(v_{ca}, I_{dc})$	$v_{ca} \geq 0$
	S5	$ON\_offset(v_{ca}, I_{dc}) + OFF\_offset(v_{ca}, I_{dc})$	
11	S1	$ON\_offset(v_{ac}, I_{dc}) + OFF\_offset(v_{ac}, I_{dc})$	$v_{ca} < 0$
	S5	$-ON\_offset(v_{ac}, I_{dc}) - OFF\_offset(v_{ac}, I_{dc})$	
12	S1	$ON\_offset(v_{ac}, I_{dc}) + OFF\_offset(v_{ac}, I_{dc})$	$v_{ca} < 0$
	S5	$-ON\_offset(v_{ac}, I_{dc}) - OFF\_offset(v_{ac}, I_{dc})$	
1	S1	$ON\_offset(v_{ab}, I_{dc}) + OFF\_offset(v_{ab}, I_{dc})$	$v_{ab} > 0$
	S3	$-ON\_offset(v_{ab}, I_{dc}) - OFF\_offset(v_{ab}, I_{dc})$	
2	S1	$ON\_offset(v_{ab}, I_{dc}) + OFF\_offset(v_{ab}, I_{dc})$	$v_{ab} \geq 0$
	S3	$-ON\_offset(v_{ab}, I_{dc}) - OFF\_offset(v_{ab}, I_{dc})$	
3	S1	$-ON\_offset(v_{ba}, I_{dc}) - OFF\_offset(v_{ba}, I_{dc})$	$v_{ab} < 0$
	S3	$ON\_offset(v_{ba}, I_{dc}) + OFF\_offset(v_{ba}, I_{dc})$	

7.5 Experimental Verification

A 7.5 kW all-SiC three-phase buck rectifier was built (Fig. 7-18) [86], whose parameters are shown in Table 7-3. 4-paralleled SiC MOSFETs and 2-paralled SiC Schottky diodes are connected in series for each switch in order to reduce the conduction loss.

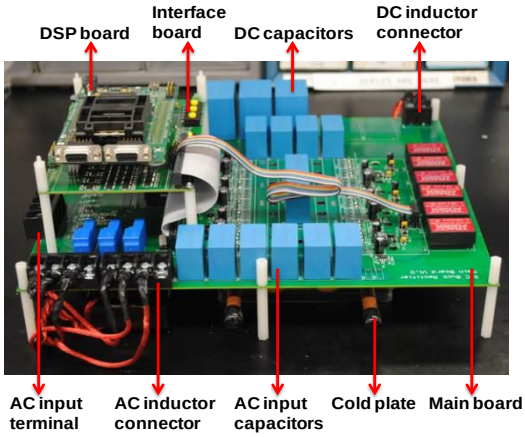


Fig. 7-18. 7.5 kW all-SiC buck rectifier.

Table 7-3. Three-phase current source rectifier parameters

Power Rating	7.5 kW
Input Voltage Rating	Three-phase line-to-line 480 $V_{ac,rms}$
Input Inductor	110 μH each phase
Input Capacitor	6 μF each phase
Output Voltage Rating	400 V_{dc}
Output Inductor	1.9 mH
Output Capacitor	150 μF
Switching Frequency	28 kHz
Efficiency	98.5 %
Power Factor	> 99 %

The parameters are listed in Table 7-4 for the compensation formula (6-3) and (6-4). The time constant and turn-off delay $t_{d(off)}$ are measured in the converter and the parasitic inductance L_p is estimated based on the PCB trace length. The parasitic capacitance C_p is estimated based on the junction capacitance value provided in the device datasheets [82]. It is shown in Fig. 7-19 that C_p decreases as the switching voltage increases.

Table 7-4. Compensation parameters in converter

Time Constant τ	10 ns for turn on process 20 ns for turn off process
Parasitic inductance L_p	100 nH
Turn-off delay $t_{d(off)}$	40 ns

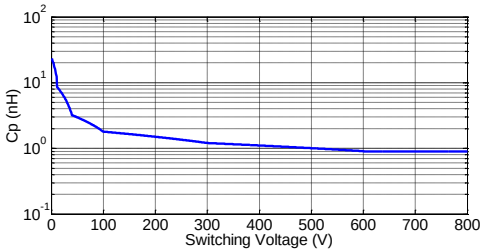


Fig. 7-19. Cp under different switching voltages.

Experiments were carried out to verify the proposed compensation method. As shown in Fig. 7-20, the input current will have much distortion when the overlap time is not compensated. With the proposed compensation method, the distortion is largely reduced.

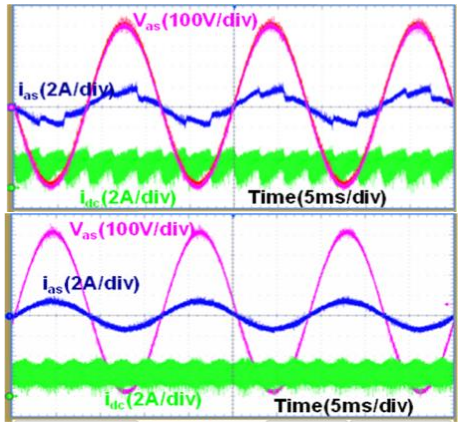


Fig. 7-20. Experiment results without (upper) and with (lower) overlap compensation (480Vac, 2.5A Idc).

In Fig. 7-21, Fig. 7-22, Fig. 7-23, and Fig. 7-24, the buck rectifier is operating under 208V input line-to-line voltage and 20A output current. In Fig. 7-21, the traditional compensation method is applied with 500 ns overlap time. The overlap time is chosen to be longer than the transition time when the voltage is small. The input current has resonance when the line-to-line voltage crosses zero.

Based on the previous analysis, the overlap can be largely reduced to accelerate the commutation. As shown in Fig. 7-22, the overlap time is only 100 ns, and the distortion is much less than that in Fig. 7-21. Their harmonic comparison is shown in Fig. 7-25. The total harmonic distortion (THD) decreases from 1.9% to 1.4% with the reduced overlap time.

In Fig. 7-23, though the overlap time is still 500 ns, it is compensated based on the commutation model proposed in this chapter. The distortion is reduced compared with Fig. 7-21. Their harmonic comparison is shown in Fig. 7-26. The THD decreases from 1.9% to 1.7% with the pulse compensation.

Small overlap time and the compensation based on the commutation model are both used in Fig. 7-24, and there is almost no obvious distortion in the current waveform. Their harmonic comparison is shown in Fig. 7-27. The THD decreases from 1.9% to 1.3% with the proposed method.

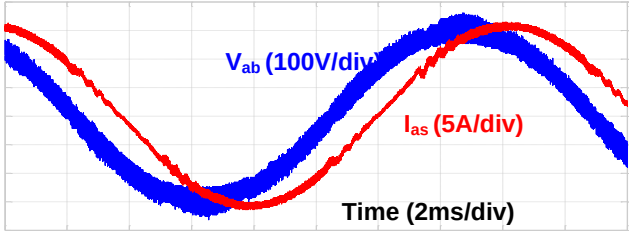


Fig. 7-21. Experiment results with traditional method (208 Vac, 20A Idc, 500 ns overlap time).

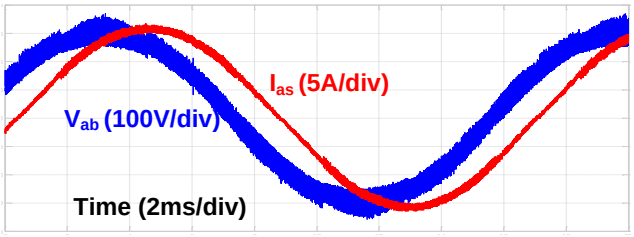


Fig. 7-22. Experiment results with reduced overlap time (208 Vac, 20A Idc, 100 ns overlap time).

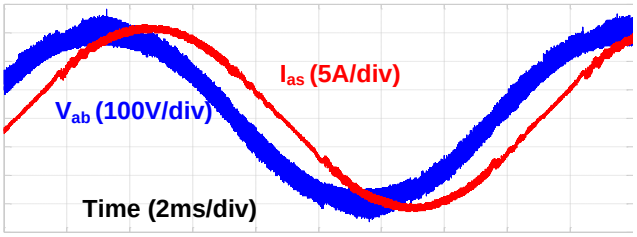


Fig. 7-23. Experiment results with pulse compensation (208 Vac, 20A Idc, 500 ns overlap time).

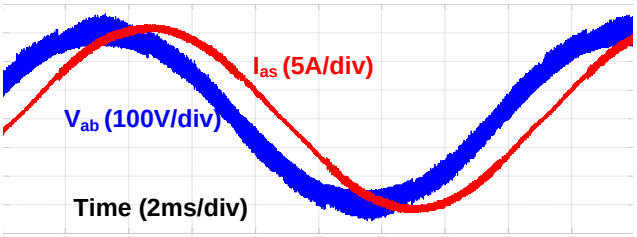


Fig. 7-24. Experiment results with proposed method (208 Vac, 20A Idc, 100 ns overlap time).

The compensation pulse width for S1 changes with v_{ab} in the experiment, as shown in Fig. 7-28. The turn-on compensation time T_{on} is largest when the voltage crosses zero. The turn-off compensation time T_{off} is small in this experiment because the turn-off speed of S1 is high in this case.

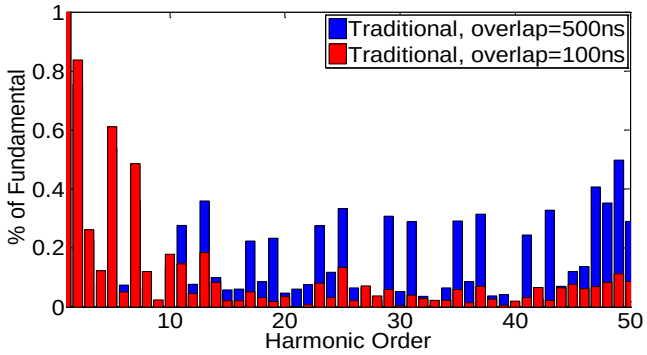


Fig. 7-25. Harmonic reduction with reduced overlap time (208 Vac, 20A Idc).

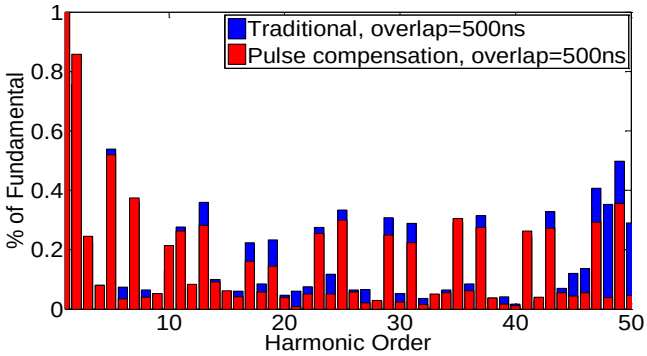


Fig. 7-26. Harmonic reduction with pulse compensation (208 Vac, 20A Idc).

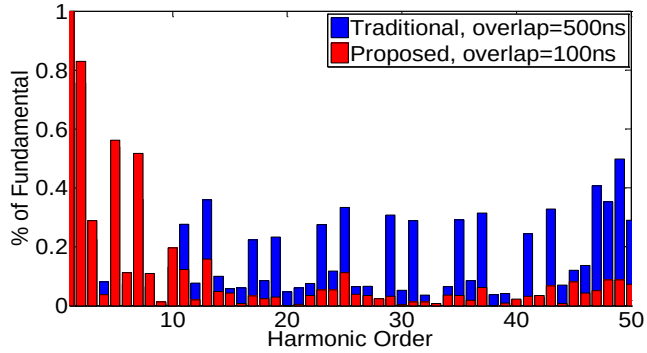


Fig. 7-27. Harmonic reduction with proposed method (208 Vac, 20A Idc).

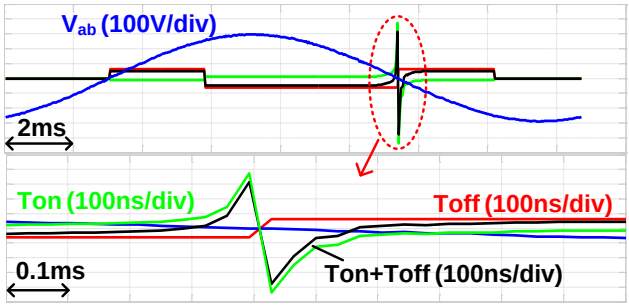


Fig. 7-28. Compensation pule width for S1 (208 Vac, 20A Idc, 500 ns overlap time).

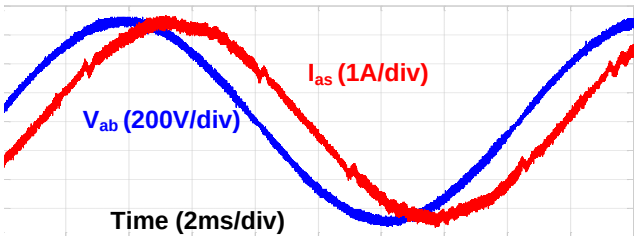


Fig. 7-29. Experiment results with traditional method (480 Vac, 5A Idc, 500 ns overlap time).

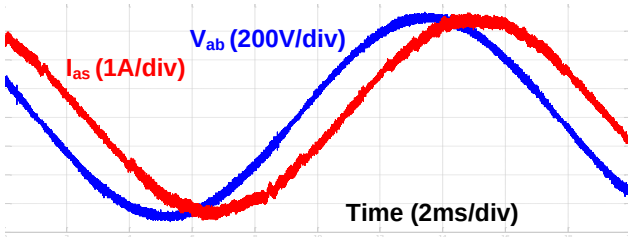


Fig. 7-30. Experiment results with proposed method (480 Vac, 5A Idc, 100 ns overlap time).

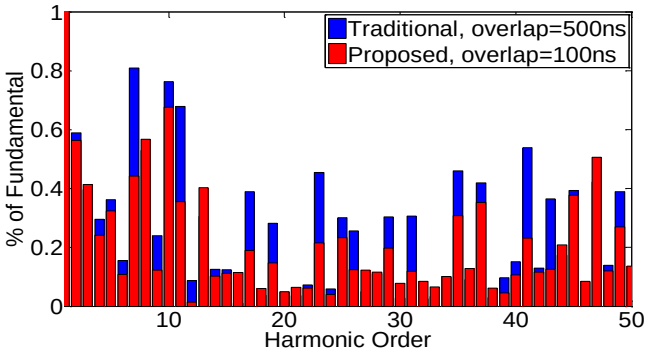


Fig. 7-31. Harmonic reduction with proposed method (480 Vac, 5A Idc).

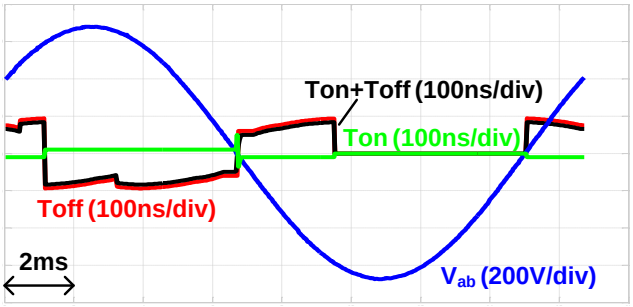


Fig. 7-32. Compensation pule width for S1 (480 Vac, 5A Idc, 100 ns overlap time).

In Fig. 7-29 and Fig. 7-30, the buck rectifier is operating under 480V input line-to-line voltage and 5A output current. The proposed method can reduce the distortion in the current waveform. Their harmonic comparison is shown in Fig. 7-31. The THD decreases from 2.5% to 2.0% with the proposed method.

In this case, the turn-off speed is low under large voltage and small current. The turn-off compensation time T_{off} changes with the voltage in Fig. 7-32.

Because of the fast switching speed of SiC devices, the compensation pulse width is usually less than 300 ns. The distortion will be more severe when some lower speed devices are used or the input capacitor is small or the converter is operating at higher switching frequency. In these applications, the proposed method will bring more improvement to the current waveform.

7.6 Conclusion

In this chapter, a modified pulse-based compensation method is proposed to compensate overlap time. In addition to the traditional method that places the overlap time based on the voltage polarity, the new method first minimizes the overlap time to reduce its effect and then compensates the pulse width according to the sampled voltage and current. The experiments

have demonstrated its advantages over traditional methods especially when the switching voltage is near zero.

8 Control Algorithm in Discontinuous Current Mode

In this chapter, the three-phase current source rectifier is modeled and analyzed in discontinuous current mode (DCM). It is demonstrated that the pole and gain of the transfer function that describe its intrinsic dynamic are significantly different from those under continuous current mode (CCM), which may exacerbate the control performance. Further, a new modulation scheme suitable for DCM is proposed for the CSR, where the space vector sequence is arranged as to assure that the dc current remains continuous during the active space vector time. Combined with the DCM modulation, a digital compensation method is applied to control the CSR in DCM. Simulation and experimental results are used to verify the significant reduction in input current distortion achieved by the proposed strategy.

8.1 Analysis of Dc-Link Current Ripple

To simplify the following analysis, several assumptions and definitions are specified: 1) The voltage on the input capacitor C_s, as defined in (8-1), is assumed to be sinusoidal without ripple and is constant in a switching period T_s. 2) The fundamental frequency component of the input current of the CSR has a phase difference φ with respect to the capacitor voltage C_s as shown in (8-1). 3) The switching frequency is much larger than the line frequency. 4) The load current is constant I_{dc} and the load voltage is constant V_{dc}. 5) All switches are ideal.

$$\begin{cases} v_a = V_m cos(\omega t + \varphi), i_{a1} = I_m cos(\omega t) \\ v_b = V_m cos\left(\omega t - \dfrac{2\pi}{3} + \varphi\right), i_{b1} = I_m cos\left(\omega t - \dfrac{2\pi}{3}\right) \\ v_c = V_m cos\left(\omega t + \dfrac{2\pi}{3} + \varphi\right), i_{c1} = I_m cos\left(\omega t + \dfrac{2\pi}{3}\right) \end{cases} \tag{8-1}$$

According to the relationship between the input voltage and current in (8-1), 12 sectors are divided in Fig. 8-1(a) for the buck rectifier. On the space vector plane in Fig. 8-1(b), the input current space vector $i_{abc}^{*} = \sqrt{\frac{3}{2}} I_m e^{j\omega t}$ can be synthesized by six active space vectors $\overrightarrow{I_x}, x = 1, \ldots, 6$ and a zero vector $\overrightarrow{I_0}$. $[S_x, S_y], x, y = 1, \ldots, 6$ denotes the on state of the switches S_x and S_y in a space vector. Considering both the switching loss and operational modulation index range, i_{abc}^{*} is usually composed by two consecutive active vectors and zero vector in each sector [97].

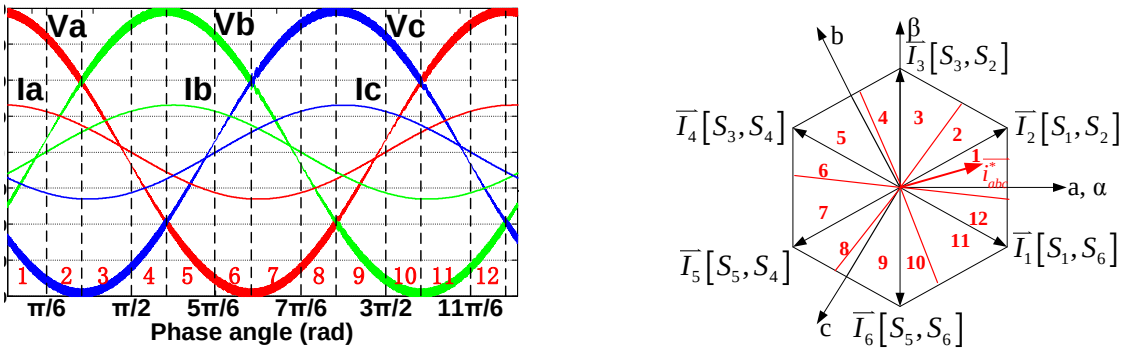
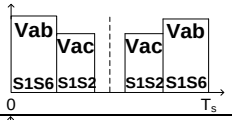
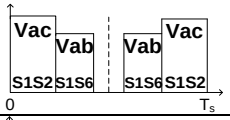
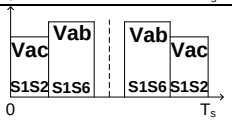
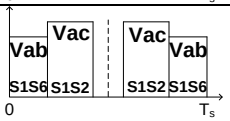
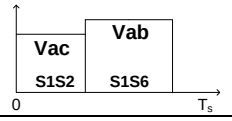
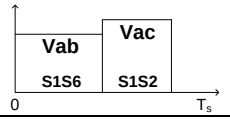
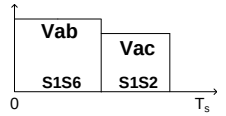
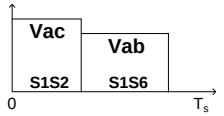


Fig. 8-1. Sector division in space vector PWM: (a) Input current and voltage; (b) Space vector plane.

Table 8-1 shows four modulation schemes under study in this chapter, including two symmetric "4-switch" schemes and two asymmetric "3-switch" schemes. The output voltage V_{pn} in two consecutive sectors is used to tell their difference on space vector arrangement. Symmetric Scheme II (SS-II) is proposed in [94] as "Modified Fullwave Symmetrical Modulation (MFSM)". Asymmetric Scheme III (US-III) is firstly proposed in [128] to realize soft switching and reduce the switching loss. Asymmetric Scheme IV (US-IV) is mentioned in

[129] and [130]. Symmetric Scheme III (SS-III) is a new symmetric modulation scheme specially designed for DCM operation.

Table 8-1. Modulation schemes of CSR

Modulation scheme	**Ouput voltage Vpn**	
	Sector12: $V_a > V_c \geq V_b$ $-\pi/6 \leq \omega t < -\varphi$	*Sector1:* $V_a > V_b > V_c$ $-\varphi \leq \omega t < \pi/6$
Symmetric Scheme II (SS-II)		
Symmetric Scheme III (SS-III)		
Asymmetric Scheme III (US-III)		
Asymmetric Scheme IV (US-IV)		

The envelope of the dc-link current ripple depends on the modulation scheme used in the CSR. Two modulation schemes, SS-II and US-IV, are considered in this analysis. The analysis circuit is shown in Fig. 8-2, where the output voltage V_{pn} depends on the space vector.

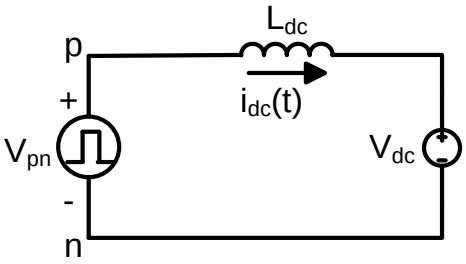


Fig. 8-2. Ripple analysis circuit.

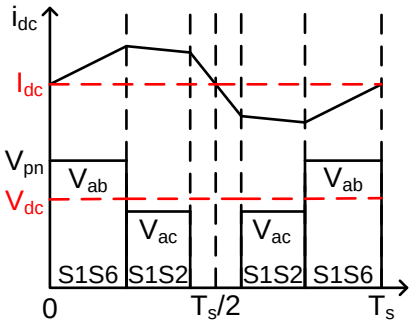


Fig. 8-3. Dc-link ripple in SS-II.

As shown in Fig. 8-3 and Fig. 8-4, the dc-link ripple changes with the output voltage in a switching period in Sector 12. Depending on the space vector arrangement, the piecewise formulas can be derived by (8-2) based on the current ripple in Fig. 8-4. The formula (8-2) is valid as long as the dc-link current is continuous. i_0 can be calculated assuming the voltage-second balance on the dc-link inductor in a switching period. The duty cycles d_1 and d_2 are given by (8-3) when $\Delta i_{dc} \ll I_{dc}$.

$$\Delta i_{dc} = \begin{cases} \dfrac{v_{ab} - V_{dc}}{L_{dc}} t + i_0, 0 \le t \le d_1 T_s \\ \dfrac{v_{ac} - V_{dc}}{L_{dc}} t + \dfrac{v_{cb}}{L_{dc}} d_1 T_s + i_0, d_1 T_s \le t \le (d_1 + d_2) T_s \\ \dfrac{-V_{dc}}{L_{dc}} t + \dfrac{v_{ac}}{L_{dc}} d_2 T_s + \dfrac{v_{ab}}{L_{dc}} d_1 T_s + i_0, \\ (d_1 + d_2) T_s \le t \le T_s \end{cases} \tag{8-2}$$

$$d_1 = \frac{|i_{b1}|}{I_{dc}}, d_2 = \frac{|i_{c1}|}{I_{dc}} \tag{8-3}$$

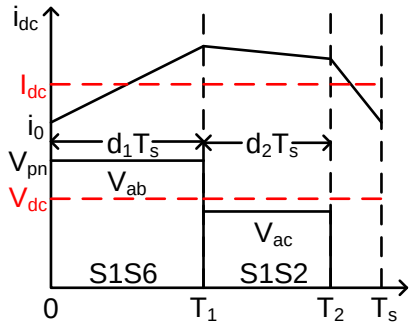


Fig. 8-4. Dc-link ripple in US-IV.

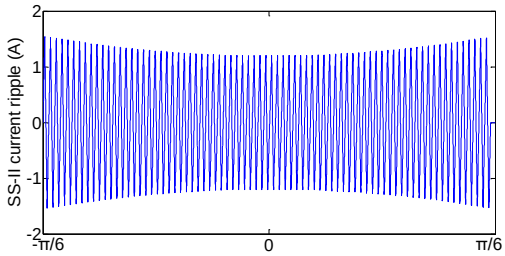


Fig. 8-5. Analysis result of current ripple with SS-II.

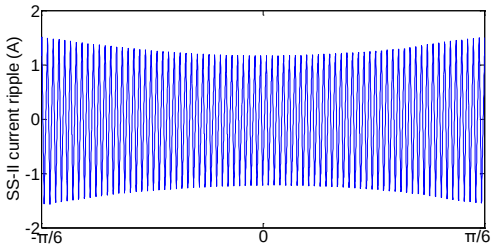


Fig. 8-6. Simulation result of current ripple with SS-II.

The period of the dc-link current ripple is 1/6 of the line period, so the analysis of two consecutive sectors is enough to predict the current ripple. The peak value of the ripple can be derived by $\Delta i_{dc-peak} = \frac{T_s V_{dc}}{2L_{dc}}\left(1 - \frac{\sqrt{3}V_{dc}}{3V_m}\right)$, when $\varphi = 0$. When $\Delta i_{dc-peak} > I_{dc}$, the dc-link current will become discontinuous.

Table 8-2. Three-phase buck rectifier parameters

Input Voltage Rating	480 V_{ac}
Input Inductor	110 μH each phase
Input Capacitor	6 μF each phase
Output Voltage Rating	400 V_{dc}
Output Capacitor	150 μF
Switching Frequency	28 kHz
Dc-Link Inductance	1.9 mH

The current ripples of SS-II and US-IV are analyzed and drawn in Fig. 8-5 and Fig. 8-7 respectively. The parameters are listed in Table 8-2 for this calculation. The dc-link current will become discontinuous when the output power is lower than 618 W. The simulation results with SS-II and US-IV are shown in Fig. 8-6 and Fig. 8-8 respectively, which agree well with the analysis.

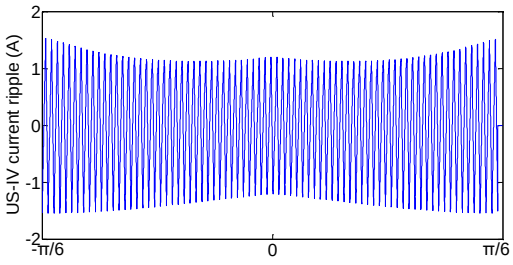


Fig. 8-7. Analysis result of current ripple with US-IV.

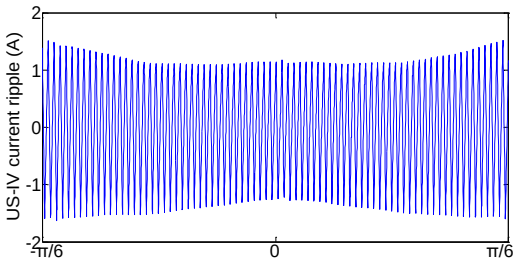


Fig. 8-8. Simulation result of current ripple with US-IV.

8.2 Modulation Schemes for DCM Operation

For normal operation in DCM, the space vectors should be arranged to ensure that the dc-link current keeps continuous in the active vectors. Otherwise, the pulse in the input current will be lost and cannot be compensated by the control algorithm.

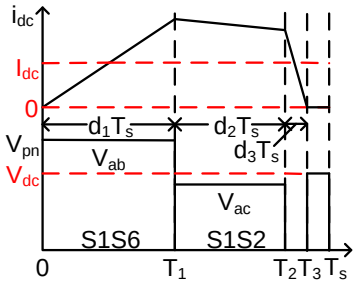


Fig. 8-9. Dc-link current ripple in DCM with US-IV.

In modulation US-IV in Table 8-1, the active vector which has the highest output voltage is arranged at the beginning of a switching period. Then the other one is arranged afterwards. The zero vector is put at the end of the period. In this way, the current will increase from zero in the first active vector and keep continuous in the second one, as shown in Fig. 8-9. The vector arrangement will alternate every 1/6 line period.

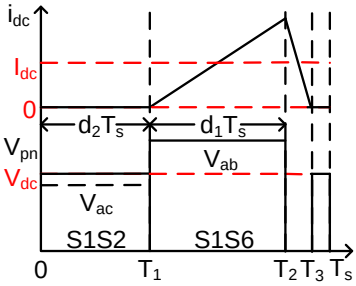


Fig. 8-10. Dc-link current ripple in DCM with US-III.

For US-III in Table 8-1, the space vectors are arranged in the opposite way of US-IV. As shown in Fig. 8-10, the dc-link current becomes discontinuous in vector S1S2 because $V_{ac} < V_{dc}$ when ωt is close to $-\pi/6$. Current pulse is lost in phase c, resulting in input current distortion.

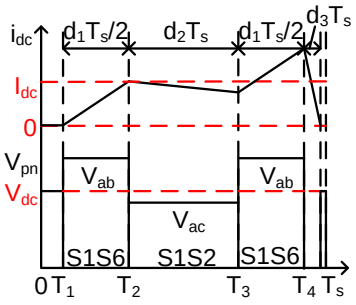


Fig. 8-11. Dc-link current ripple in DCM with SS-III.

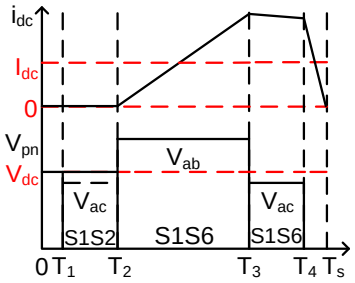


Fig. 8-12. Dc-link current ripple in DCM with SS-II.

Compared with the asymmetric scheme, the symmetric modulation schemes are more popular for its lower harmonics and fixed ripple-free points for dc-link current sampling. For the symmetric modulation schemes in Table 8-1, SS-III is able to keep the current continuous in active vectors in DCM, as shown in Fig. 8-11. But SS-II will lose half the active vectors S1S2 when $V_{ac} < V_{dc}$, as shown in Fig. 8-12.

Based on the analysis, the modulations SS-II and US-III cannot work consistently well in DCM unless V_{pn} is larger than V_{dc} during active space vectors.

8.3 Model of CSR in CCM and DCM

In this section, the small signal models will be derived for the CSR in DCM and compared with the CCM model. In this analysis, the modulation US-IV is considered for its simplicity. In a

switching period, two active switches and the freewheeling diode are involved in the commutation. The three-phase CSR can be simplified to the circuit in Fig. 8-13 where S2, S6 and D are commutating in Sector 12, $-\pi/6 \leq \omega t < -\varphi$.

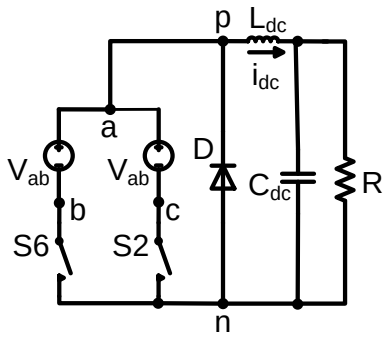


Fig. 8-13. Simplified commutation circuit.

8.3.1 CCM Model

In CCM, the dc-link current is shown in Fig. 8-4. The average model of the buck rectifier can be derived by averaging the state variables over a switching period. The voltage on the dc-link inductor can be derived by (8-4), where $\langle x \rangle_{T_s}$ is the average value of the variable x over a switching period T_s, d_{1-ccm} and d_{2-ccm} are the duty ratios of S6 and S2 respectively in CCM.

$$L_{dc}\frac{d\langle i_{dc}\rangle_{T_s}}{dt} = \langle v_{ab}\rangle_{T_s} d_{1-ccm} + \langle v_{ac}\rangle_{T_s} d_{2-ccm} - \langle v_{dc}\rangle_{T_s} \tag{8-4}$$

After the perturbation and linearization using Taylor expansion, the small signal model and the quiescent operation point are derived by (8-5), where $\hat{x}$ is the disturbance of the variable x near its quiescent operation point X. The transfer function can be derived from (8-5) using the Laplace transformation as given by (8-6) with a pole at the origin.

$$L_{dc}\frac{d\hat{\imath}_{dc}}{dt} = V_{ab}\hat{d}_{1-ccm} + V_{ac}\hat{d}_{2-ccm} + \hat{v}_{ab}D_{1-ccm} + \hat{v}_{ac}D_{2-ccm} - \hat{v}_{dc}$$
$$V_{ab}D_{1-ccm} + V_{ac}D_{2-ccm} - V_{dc} = 0 \tag{8-5}$$

$$\frac{i_{dc}(s)}{d_{1-ccm}(s)} = \frac{V_{ab}}{L_{dc}s}$$
$$\frac{i_{dc}(s)}{d_{2-ccm}(s)} = \frac{V_{ac}}{L_{dc}s} \tag{8-6}$$

8.3.2 DCM Model

In DCM, the dc-link current ripple is drawn in Fig. 8-9, where the current becomes discontinuous during zero vector. d_{1-dcm}, $d_{2-dcm}$and d_{3-dcm} are the duty cycles in DCM (Fig. 8-9) and d_{3-dcm} can be derived by (8-7).

$$d_{3-dcm} = \frac{\langle v_{ab}\rangle_{T_s}d_{1-dcm} + \langle v_{ac}\rangle_{T_s}d_{2-dcm}}{V_{dc}} - (d_{1-dcm} + d_{2-dcm}) \tag{8-7}$$

The voltage on the dc-link inductor can be derived by (8-8) in DCM.

$$L_{dc}\frac{d\langle i_{dc}\rangle_{T_s}}{dt} = \langle v_1\rangle_{T_s}d_{1-dcm} + \langle v_2\rangle_{T_s}d_{2-dcm} - \langle v_{dc}\rangle_{T_s}d_{3-dcm}$$
$$\langle v_1\rangle_{T_s} = \langle v_{ab}\rangle_{T_s} - \langle v_{dc}\rangle_{T_s}, \langle v_2\rangle_{T_s} = \langle v_{ac}\rangle_{T_s} - \langle v_{dc}\rangle_{T_s} \tag{8-8}$$

After substituting d_{3-dcm} with (8-7), (8-8) can be perturbed and linearized to get the transfer function in DCM as shown in (8-9) and (8-10), where $V_1 = V_{ab} - V_{dc}$ and $V_2 = V_{ac} - V_{dc}$.

$$\frac{i_{dc}(s)}{d_{1-dcm}(s)} = \left(\begin{array}{c} V_1 + \frac{2L_{dc}V_{dc}I_{dc}V_1}{T_s(V_1D_{1-dcm} + V_2D_{2-dcm})^2} + \\ \frac{V_{dc}(D_{1-dcm}^2V_1^2 + 2D_{1-dcm}D_{2-dcm}V_1V_2 + D_{2-dcm}^2V_1V_2)}{(V_1D_{1-dcm} + V_2D_{2-dcm})^2} \end{array}\right) / \left(L_{dc}s + \frac{2L_{dc}V_{dc}}{T_s(V_1D_{1-dcm} + V_2D_{2-dcm})}\right) \tag{8-9}$$

$$\frac{i_{dc}(s)}{d_{2-dcm}(s)} = \left(V_2 + \frac{2L_{dc}V_{dc}I_{dc}V_2}{T_s(V_1D_{1-dcm}+V_2D_{2-dcm})^2} + \frac{V_{dc}(D_{2-dcm}^2V_2^2 + 2D_{1-dcm}D_{2-dcm}V_1V_2 + 2D_{1-dcm}^2V_1^2 - D_{1-dcm}^2V_1V_2)}{(V_1D_{1-dcm}+V_2D_{2-dcm})^2} \right) / \left(L_{dc}s + \frac{2L_{dc}V_{dc}}{T_s(V_1D_{1-dcm}+V_2D_{2-dcm})} \right) \quad (8\text{-}10)$$

Comparing (8-9) with (8-5), it can be seen that the pole in the transfer function changes from zero in CCM to a non-zero value in DCM. The Bode diagrams of the inductor current to duty cycle are shown in Fig. 8-14 and Fig. 8-15. The gain decreases much under low frequency in DCM and the CCM control may become instable in DCM.

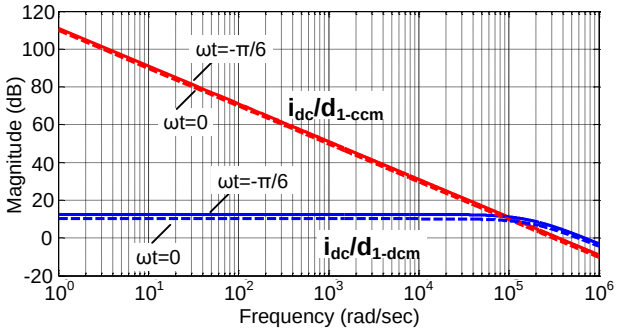


Fig. 8-14. Bode diagram of $i_{dc}/d_{1\text{-}ccm}$ and $i_{dc}/d_{1\text{-}dcm}$.

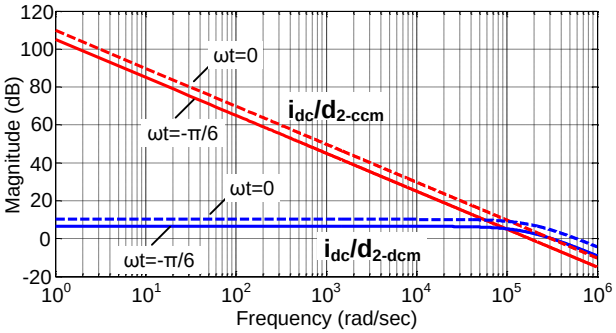


Fig. 8-15. Bode diagram of $i_{dc}/d_{2\text{-}ccm}$ and $i_{dc}/d_{2\text{-}dcm}$.

8.4 Feed-Forward Compensation in DCM

8.4.1 Conventional Digital Controller

In three-phase CSRs, the controller is usually designed in dq rotating coordinate system where the converter model is time-invariant [131]. Usually the digital controller includes two control loops as shown in Fig. 8-16 [99]. In the outer dc voltage control loop, the voltage on the

output dc capacitor is fed back to the compensator to generate the dc current reference for the inner current control loop. In the current control loop, the current in the dc-link inductor is fed back to the current compensator to generate D_d, the duty cycle on the d axis. Then the space vectors are synthesized and the duty ratios d_1 and d_2 are calculated for modulator to generate PWM signal for each switch.

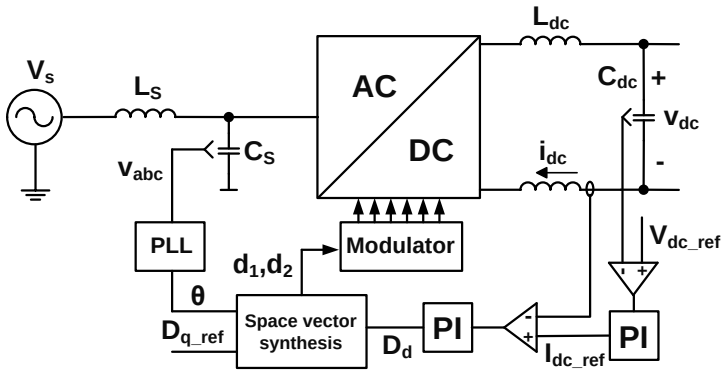


Fig. 8-16. Conventional digital controller.

When modeling the buck rectifier in dq coordinates, it is always assumed that the dc-link current is constant with negligible ripple. When Δi_{dc} is comparable with I_{dc}, the input current will have large distortion if the conventional controller continues to generate duty cycles based on CCM model. Moreover, the gain of the transfer function decreases much as shown in Section 8.3 when the converter enters DCM. The performance of the conventional controller will get worse or even unstable in DCM.

8.4.2 Feed-Forward Compensation Method for DCM

In DCM, the impact of the current ripple cannot be neglected. The steady-state DCM duty cycles d_{1-dcm} and d_{2-dcm} can be calculated by (8-11) for SS-III in Sector 12.

$$d_{1-dcm} = |i_{b1}| \sqrt{\frac{2L_{dc}}{T_s\left(|i_{b1}|(v_{ab} - V_{dc}) + |i_{c1}|(v_{ac} - V_{dc})\right)}}$$
$$d_{2-dcm} = |i_{c1}| \sqrt{\frac{2L_{dc}}{T_s\left(|i_{b1}|(v_{ab} - V_{dc}) + |i_{c1}|(v_{ac} - V_{dc})\right)}} \quad (8\text{-}11)$$

It can be seen that the duty cycle depends on the input voltage and current, the dc voltage, the switching period and the dc-link inductance, more complex than the formulas in CCM in (8-3). As shown in Fig. 8-17, the duty cycles have much difference between DCM and CCM. The output power varies and the converter parameters are listed in Table 8-2 for the calculation. When the output power is lower than 480 W in Fig. 8-17(a), $d_{1-dcm} + d_{2-dcm}$ is always smaller than $d_{1-ccm} + d_{2-ccm}$. The dc-link current is totally discontinuous in the case. The buck rectifier operates in DCM.

When the output power is between 480 W and 618 W, $d_{1-dcm} + d_{2-dcm}$ have two intersections with $d_{1-ccm} + d_{2-ccm}$, as shown in Fig. 8-17(b). The dc-link current is discontinuous when $d_{1-dcm} + d_{2-dcm} < d_{1-ccm} + d_{2-ccm}$. The buck rectifier operates in both CCM and DCM. When the output power is higher than 618 W in Fig. 8-17(c), $d_{1-dcm} + d_{2-dcm}$ is always larger than $d_{1-ccm} + d_{2-ccm}$. The dc-link current is totally continuous. The buck rectifier operates in CCM. So the relationship between $d_{1-dcm} + d_{2-dcm}$ and $d_{1-ccm} + d_{2-ccm}$ can be used to judge CCM and DCM.

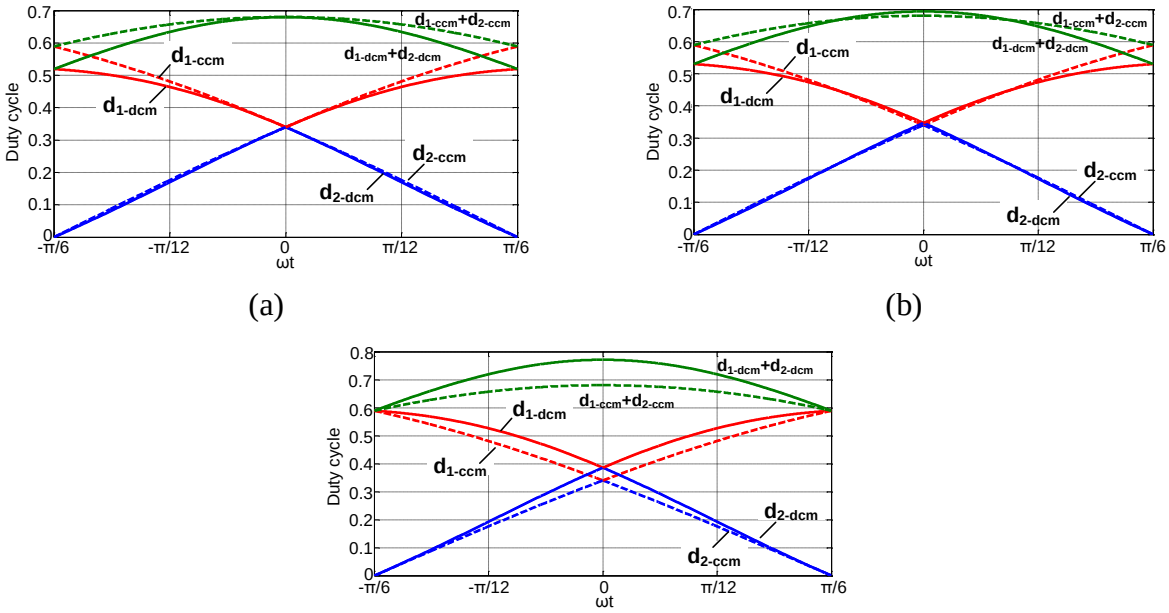


Fig. 8-17. Duty cycle comparison for SS-III in DCM and CCM: (a) P = 480 W; (b) P = 500 W; (c) P = 618 W.

In DCM, the duty cycles need to be compensated and a digitalized feed-forward compensation method is proposed in Fig. 8-18. It can be integrated to the conventional controller.

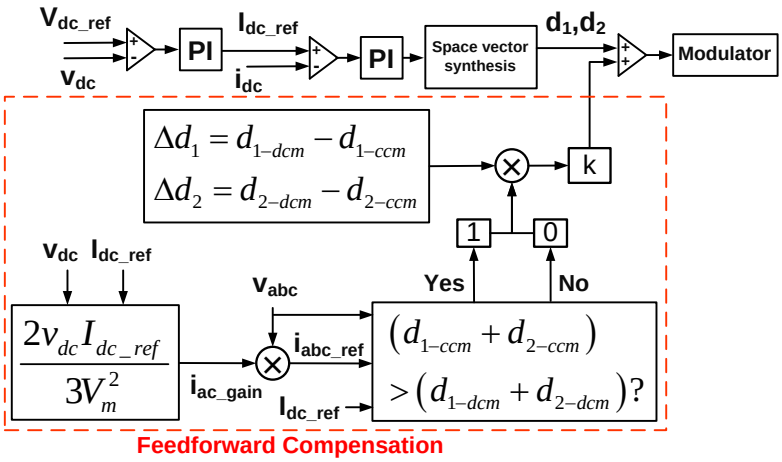
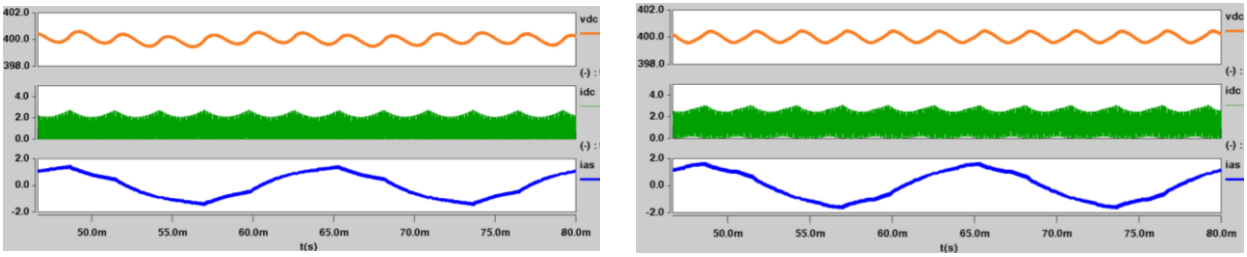


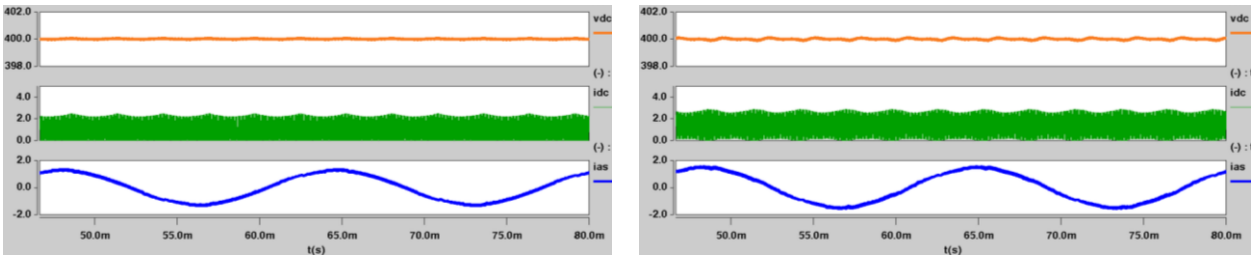
Fig. 8-18. Proposed feed-forward compensation.

As shown in Fig. 8-18, the offset Δd_1 and Δd_2 will be added to the conventional controller output to compensate the duty cycle error in DCM when $d_{1-dcm} + d_{2-dcm} < d_{1-ccm} + d_{2-ccm}$. In CCM, the compensator is not active.



(a) (b)

Fig. 8-19. Simulation without proposed compensation: (a) 400 W; (b) 550 W.



(a) (b)

Fig. 8-20. Simulation with proposed compensation: (a) 400 W; (b) 550 W.

Table 8-3. Input current THD in simulation

Output power	**Input current THD**	
	Without compensation	**With compensation**
400 W	7.6 %	4.1 %
550 W	6.8 %	4.2 %
1000 W	3.6 %	3.5 %

When applying the traditional control algorithm in DCM, the output voltage has low-order ripple and the input current has large distortion as shown in Fig. 8-19(a) and (b). With proposed feed-forward compensation, the output voltage ripple and input current distortion are both reduced obviously in Fig. 8-20(a) and (b). The feed-forward compensation does not affect the controller in CCM. The input current total harmonic distortion (THD) is listed in Table 8-3. With the proposed feed-forward compensation, the input current THD can be reduced much.

8.5 Experimental Results

To verify the DCM control with experiments, a 7.5kW all-SiC three-phase CSR has been built as shown in Fig. 8-21 [86]. The parameters of the converter are listed in Table 8-2. The experiment waveforms at full load are measured and shown in Fig. 8-22.

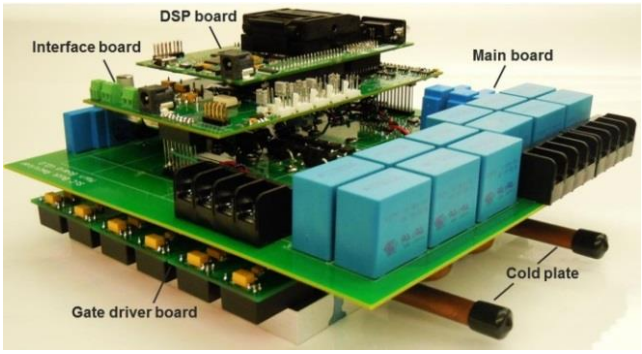


Fig. 8-21. 7.5 kW all-SiC three-phase buck rectifier.

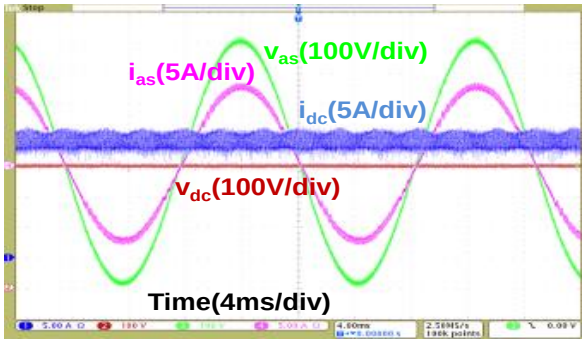
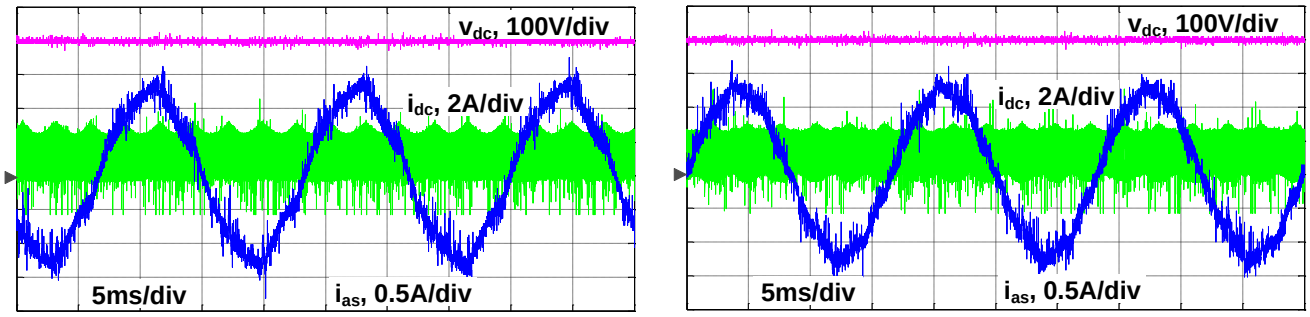
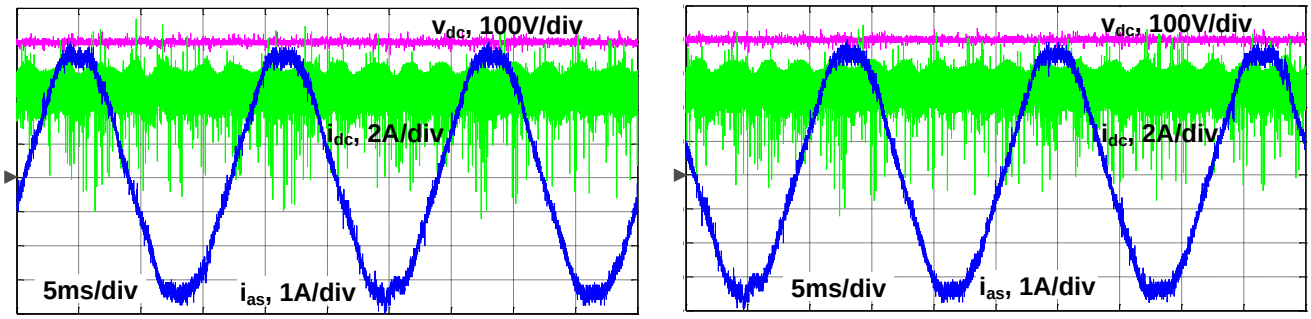


Fig. 8-22. Experiment waveforms at full load.



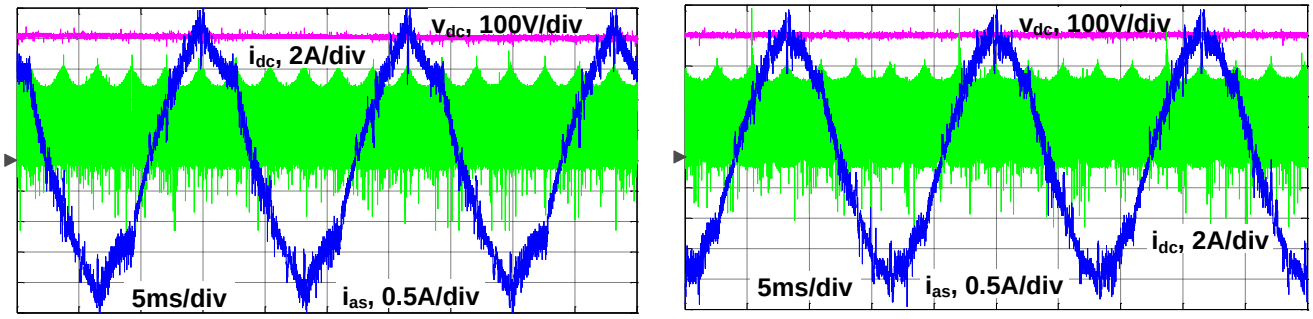
(a) (b)

Fig. 8-23. Experiment waveforms at 500 W with 1.7 mH dc-link inductor: (a) Without compensation; (b) With compensation.



(a) (b)

Fig. 8-24. Experiment waveforms at 2000 W with 1.7 mH dc-link inductor: (a) Without compensation; (b) With compensation.



(a) (b)

Fig. 8-25. Experiment waveforms at 1000 W with 0.85 mH dc-link inductor: (a) Without compensation; (b) With compensation.

The waveforms are shown in Fig. 8-23 under 500 W output power with 1.7 mH dc-link inductor. The dc-link current is completely discontinuous in this case. With the proposed compensation method, the input current distortion can be reduced in the waveforms in Fig. 8-23(b) compared with the one in Fig. 8-23(a). When operating in CCM as shown in Fig. 8-24, the proposed compensation method is not active and will not affect the conventional controller.

In Fig. 8-25, the dc-link inductance is reduced by half (0.85 mH). It is obvious that the current ripple will be doubled and the converter enters the DCM when the output power is as high as 1000 W. With the proposed compensation method, the input current distortion can be reduced in the waveforms in Fig. 8-25(b) compared with the one in Fig. 8-25(a).

The input current THD is listed in Table 8-4 under different operating conditions. It is shown that the input current THD is decreased with the proposed compensation method when the converter operates in DCM.

Table 8-4. Input current THD in experiments

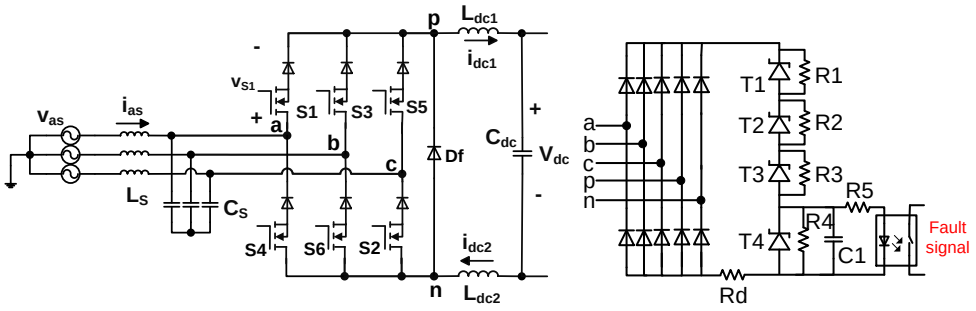
Output power	**Input current THD**		**Dc-link inductance**
	Without compensation	**With compensation**	
1000 W	8.5 %	5.8 %	0.85 mH
1143 W	9.1 %	8.8 %	
500 W	7.6 %	5.8 %	1.7 mH
615 W	8.4 %	8.3 %	
2000 W	3.3 %	3.3 %	
7500 W	2.9 %	2.9 %	

8.6 Conclusion

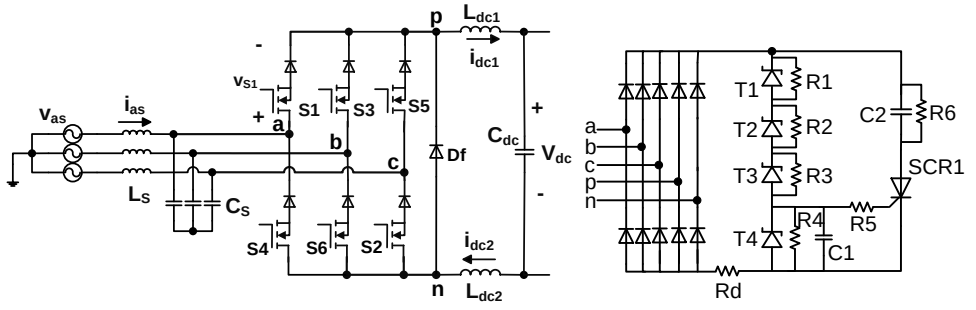
The three-phase CSR was modeled in DCM and a modulation and control method were proposed for this operating mode. The dc-link current ripple was analyzed first to identify the boundary between CCM and DCM. Then the small-signal models were derived for the buck rectifier in DCM. Compared with the CCM model, the gain of the transfer function was shown to change significantly in DCM, detrimentally affecting the control performance. To account for this, a DCM modulation scheme was proposed keeping the current continuous during the active space vectors. Lastly, a digital feed-forward compensation method was proposed to compensate the duty cycle error in DCM. It was shown that with the proposed DCM control method, both the output voltage ripple and the input current THD can be largely reduced.

9 Overvoltage Protection Scheme for SiC Devices

In this chapter, a novel overvoltage protection scheme is proposed in Fig. 9-1(a) for current source converters built with SiC MOSFETs. In the protection circuit, the diode bridge is used to detect the overvoltage on the devices, and the high-power TVS diodes are applied to clamp the overvoltage within 50 ns. The energy in the dc-link inductor can be dissipated in the TVS diodes when the energy is low. A capacitor in series with a thyristor can also be added to absorb large energy in Fig. 9-1(b). Moreover, the proposed protection scheme will not affect the switching performance of SiC MOSFETs in normal operation. Its effectiveness has been verified by experiments in both pulse test and converter test.



(a)



(b)

Fig. 9-1. Proposed overvoltage protection scheme (a) without thyristor and (b) with thyristor.

9.1 Overvoltage in Current Source Converter

The current source rectifier is taken as an example to explain the fault and protection scheme. The overvoltage on the devices may come from two sources. In the switching process of the devices, there will be voltage overshoot caused by the resonance between the parasitic inductance and junction capacitance of the device in the commutation loop. The overvoltage in this case does not last a long time since the energy in the parasitics is very small and will be damped quickly. It can be reduced with better layout design.

The most serious overvoltage appears on the devices when the current is interrupted in the dc-link inductor. As the energy storage component, the dc-link inductor is designed to have large inductance to limit the dc-link current ripple. The device can not handle the energy stored in the dc-link inductor and will fail when it is above its bearable avalanche energy. When the freewheeling diode Df is not added in the rectifier, one of the upper three switches and one of the lower three switches must be ON to provide a current path. The freewheeling diode Df is usually added in some non-regenerative applications to reduce the conduction loss. It can also perform as a protection scheme for dc-link current interruption when the switches are driven falsely.

The equivalent circuit during current interruption can be drawn in Fig. 9-2. C_{Ldc} is the equivalent parallel capacitance of the dc-link inductor L_{dc}. C_{oss} is the equivalent output capacitance of the upper three switches S1, S3 and S5. The ac capacitor C_s in the input filter and the dc capacitor C_{dc} can be assumed to be short in the transient since they are much larger than C_{oss} and C_{Ldc}. The switch $S_{1,3,5}$ is turned off and causes current interruption. The peak voltage spike on the semiconductor device can be given by (9-1), which is proportional to the device switching speed and the dc-link inductance.

$$v_s = L_{dc}\frac{di_{dc}}{dt} \tag{9-1}$$

In the worst case, the switch $S_{1,3,5}$ is turned off instantly. All the dc-link current will charge C_{oss} and C_{Ldc} and cause the device voltage to increase at a fast rate given by

$$\frac{dv_s}{dt} = \frac{i_{dc}}{(C_{oss} + C_{Ldc})} \tag{9-2}$$

For a 7.5 kW current source rectifier in [86], $L_{dc} = 1.9\ mH$, $C_{Ldc} = 38\ pF$, $C_{oss} = 441\ pF$ and $i_{dc} = 18.75\ A$ under full load. The voltage will increase from 0 V to 1200 V on the switch in less than 31 ns. To protect the device, the protection circuit needs to respond within tens of nanoseconds. It is not enough to just parallel a voltage clamping circuit with the dc-link inductor. The device voltage may be higher than the voltage on the dc-link inductor considering various input and output voltages [132].

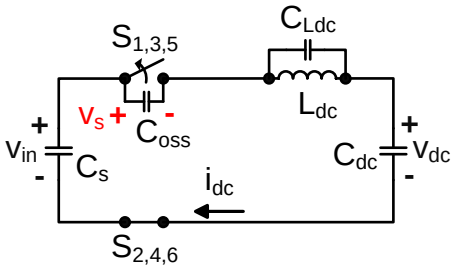


Fig. 9-2. Equivalent circuit for dc-link current interruption.

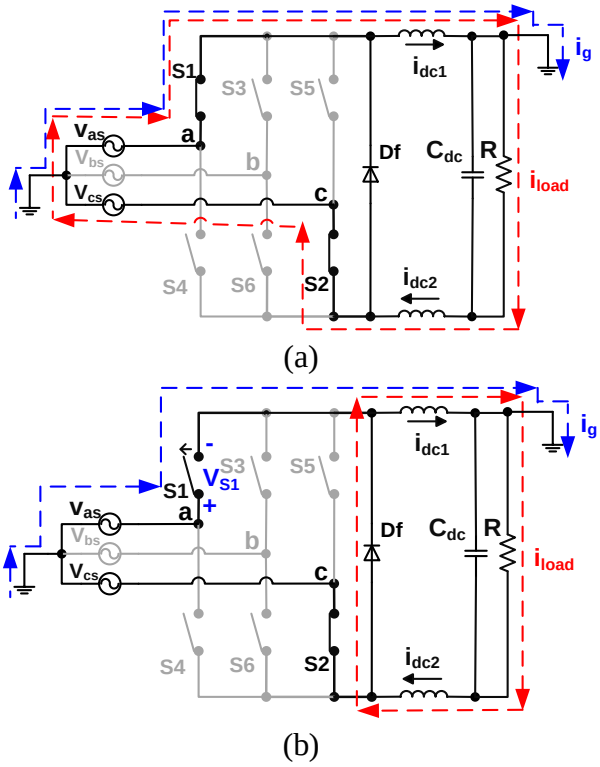


Fig. 9-3. Overvoltage caused by grounding fault on the dc side: (a) S1 is ON; (b) S1 is OFF.

In practice, the dc-link inductor is usually split into two parts placed on both positive and negative buses. In this way, it can help to reduce the common-mode noise or circulating current in the converters [44][133]. The current in the positive bus i_{dc1} may not equal to i_{dc2} in the negative bus in some grounding faults. One of the cases is shown in Fig. 9-3(a), where the positive dc bus is grounded by accident. Other than the output load current i_{load}, there is a grounding current i_g formed in the ground loop. i_{dc1}will be larger than i_{dc2} in this case. When S1 is turned off as shown in Fig. 9-3(b), the load current can freewheel through Df. But the grounding current is interrupted, which will still cause overvoltage on S1.

The equivalent circuit is shown in Fig. 9-4, where C_{CM} is the grounding capacitance on the ac side. The voltage spike on S1 can be given by $L_{dc1}\frac{di_g}{dt}$ and the voltage increases at a rate

$\frac{i_g}{(C_{oss}+C_{Ldc1})}$. The total energy caused by the grounding current can be written by $L_{dc1}\frac{i_g^2}{2}$, which can be overwhelming for the device.

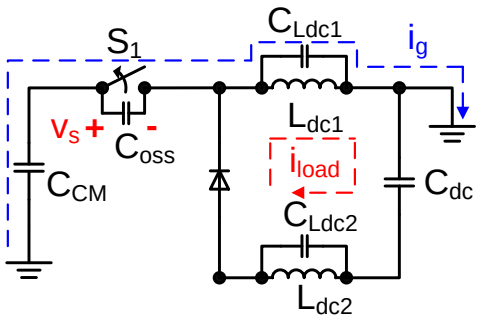


Fig. 9-4. Equivalent circuit for ground current interruption.

9.2 Proposed Overvoltage Protection Scheme

9.2.1 Operation Principle

The proposed overvoltage protection scheme is shown in Fig. 9-1(a). The diode bridge is connected to the three input nodes (a, b and c) and two output nodes (p and n) to detect the maximum voltage on the six switches. The ten diodes in the bridge carry only some leakage current during normal operation. While under overvoltage fault, they will conduct the full dc-link current. Therefore, these diodes do not need large average current rating but enough repetitive peak forward current rating to handle the fault current.

After detecting overvoltage, the protection circuit needs to clamp it in nanoseconds to prevent device failure [134]. The clamping circuit should have very fast response time and steep breakdown V-I curve [135][136].

The transient-voltage-suppression (TVS) diodes are suitable for such a fast transient because they can switch on within 50 ps and have sharp breakdown curve and low clamping factor [136]. Moreover, they have long expected life and short-circuit failure mode. The clamping voltage of TVS diodes is usually lower than 400 V. Various TVS diodes with different power and voltage ratings are available on the market [137]. The reverse stand-off voltage of the TVS diode should be higher than the converter operation voltage, so that it will not affect the normal operation of the converter. Its maximum clamping voltage should be smaller than the rated voltage of the device to be protected. Moreover, its maximum peak pulse current should be higher than the current in the dc-link inductor. For the converter in Table 9-1 with 1200 V SiC MOSFETs, the normal operation voltage is 680 V and the device rating is 1200 V. Three 30 kW TVS diodes 30KPA300A are connected in series to clamp the overvoltage around 1100 V [137].

Table 9-1. Three-phase current source rectifier parameters

Power Rating	7.5 kW
Input Voltage Rating	Three-phase line-to-line 480 $V_{ac,rms}$
Input Inductor	110 μH each phase
Input Capacitor	6 μF each phase
Output Voltage Rating	400 V_{dc}
Output Inductor	1.9 mH
Output Capacitor	150 μF
Switching Frequency	28 kHz
Efficiency	98.5 %
Power Factor	> 99 %

As shown in Fig. 9-1(a), T_1, T_2 and T_3 are three high-power TVS diodes connected in series to clamp the device overvoltage. T_4 is a low-power TVS diode to form and send the fault signal to the controller through an optocoupler. The converter will be shut down afterwards to prevent repetitive faults. The resistors R_1, R_2, R_3 and R_4 are paralleled with the TVS diodes for proper voltage distribution in steady state. R_d is a small resistor connected in the clamping circuit to damp the possible resonance. C_1 is used as filter capacitor and R_5 can limit the input current to the optocoupler. The components used in the protection circuit are listed in Table 9-2 for a 7.5 kW current source rectifier.

Table 9-2. Components of protection circuit

Diode Bridge	STTH512, 1200 V/5 A Ultrafast recovery diode
T_1, T_2 and T_3	30KPA300A, 300 V/30 kW TVS diodes
T_4	LCE15A, 15 V/1.5 kW TVS diode
R_1, R_2 and R_3	1 MΩ surface mount resistor
R_4	150 Ω surface mount resistor
R_5	10 kΩ surface mount resistor
R_d	2 Ω/2 W through hole resistor
C_1	0.1 μF/50 V surface mount capacitor
Optocoupler	HCPL-0611, 15 kV/μs common mode immunity

In the clamping state, the TVS diodes will take on breakdown voltage and large fault current at the same time. Its power rating should be carefully selected for different applications. When the converter output power is high, a thyristor can be added in the protection circuit to

handle the large power, as shown in Fig. 9-1(b). It takes advantage of the traditional crowbar structure, where a thyristor is used to dissipate the inductor energy [136]. After clamping overvoltage with TVS diodes, the thyristor is turned on to take the inductor current. Because of its low conduction voltage drop, its power dissipation is much lower than the TVS diodes. But in a traditional crowbar circuit, the thyristor will keep conducting and can not restore until its current is below the holding current. It will cause high transient current in this process.

To deal with this problem, a capacitor C_2 is connected in series with the thyristor SCR1 to absorb the inductor energy. SCR1 will be turned off automatically after C_2 is fully charged with the dc-link inductor energy. The resistor R_6 is paralleled with C_2 to dissipate its stored energy afterwards. The TVS diodes in Fig. 9-1(b) do not need high power rating since most power is absorbed on the capacitor C_2.

The proposed protection scheme in Fig. 9-1 does not include any active control circuit, so it can protect the devices even when the auxiliary power is down in the converter.

9.2.2 Simulation

The proposed protection scheme is modeled and analyzed in the simulation with Saber. The simplified simulation circuit is shown in Fig. 9-5, where L_p is the parasitic inductance, C_p is the parasitic capacitance and R_d is the damping resistor. In the simulation, S1 is turned on to charge the current i_{dc} to a given level. Then it is turned off to create an overvoltage in the circuit.

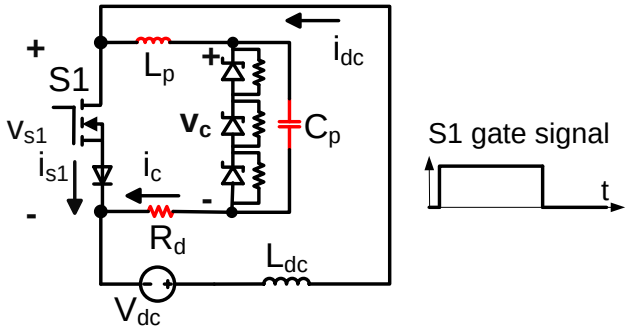
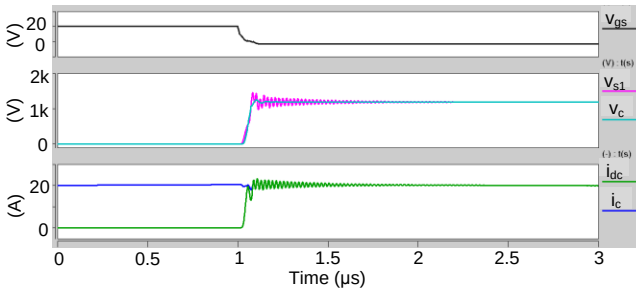
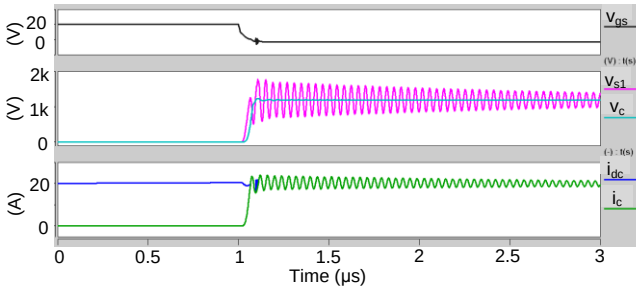


Fig. 9-5. Simulation circuit without thyristor.

Due to the parasitic inductance and capacitance, resonance is caused in the clamping circuit. As shown in Fig. 9-6(a) and (b), the voltage v_{S1} on S1 has much more resonance compared with the voltage v_c on the TVS diodes. As L_p gets larger, it becomes even worse in Fig. 9-6(b).



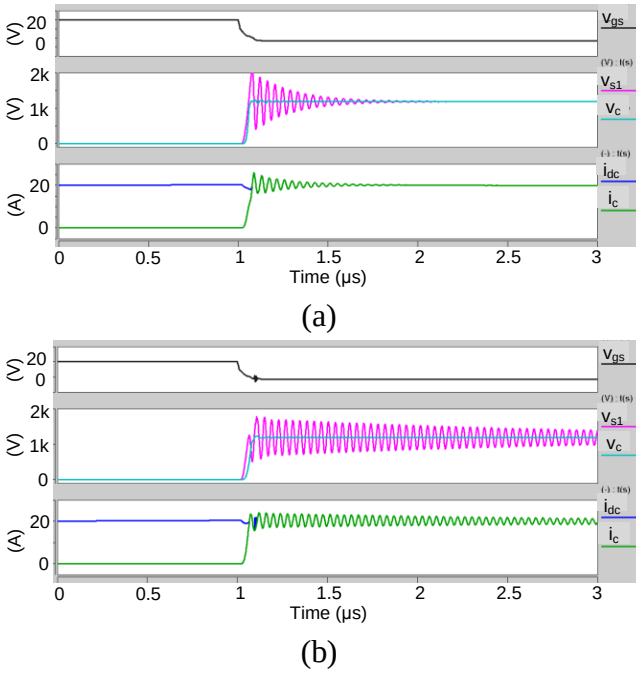
(a)



(b)

Fig. 9-6. Simulation results with different L_p: (a) 200 nH; (b) 1000 nH.

With different C_p, the simulation waveforms are compared in Fig. 9-7. The resonance becomes worse with larger C_p.

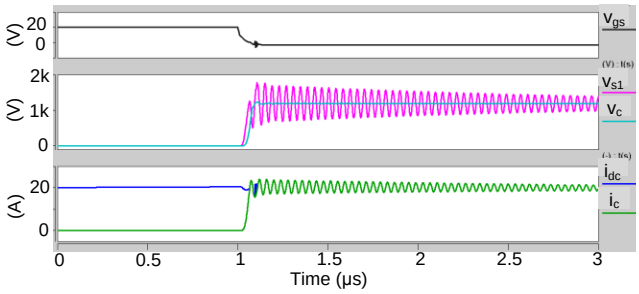


(a)

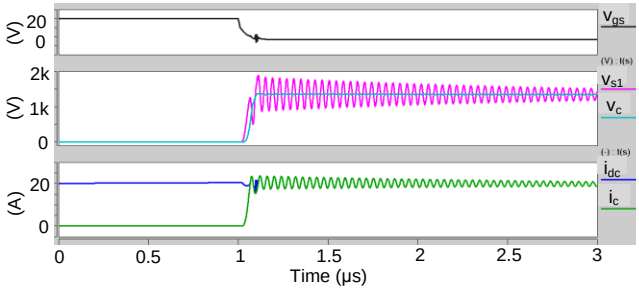
(b)

Fig. 9-7. Simulation results with different C_p: (a) 100 pF;(b) 500 pF.

With different R_d, the simulation waveforms are compared in Fig. 9-8. The resonance can be damped quickly with larger R_d. But larger R_d will cause more voltage drop on it, which will impact the clamping voltage.



(a)



(b)

Fig. 9-8. Simulation results with different R_d: (a) 2 Ω; (b) 10 Ω.

To reduce the resonance, the layout of the protection circuit should be well designed. It should be placed close to the devices under protection to reduce the trace length. Smaller package is preferred for the components in the protection circuit. Several TVS diodes are connected in series to reduce the parasitic capacitance. A small damping resistor R_d can be added to damp the resonance.

With the thyristor, the simplified protection circuit is shown in Fig. 9-9. When overvoltage fault occurs, the TVS diodes will clamp the voltage and turn on SCR1. Then the dc-link current is transferred to SCR1 and charges C_2. When i_{scr} drops below the holding current, SCR1 is naturally turned off. The energy stored in C_2 is discharged through R_6.

Two rules should be met when selecting proper C_2 and R_6 for this circuit. First, the voltage on C_2 should be less than the clamping voltage of the TVS diodes. Otherwise the fault current

may go through the TVS diodes rather than the thyristor. Second, the current i_{scr} should have a zero-cross point so that the thyristor can be naturally turned off.

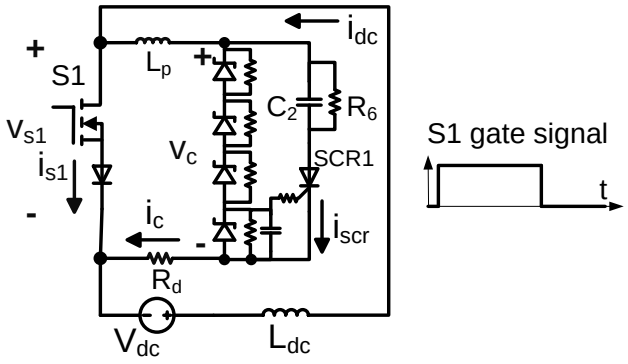


Fig. 9-9. Simulation circuit with thyristor.

After SCR1 is turned on, the protection circuit can be simplified to a typical L-C-R resonant circuit shown in Fig. 9-10.

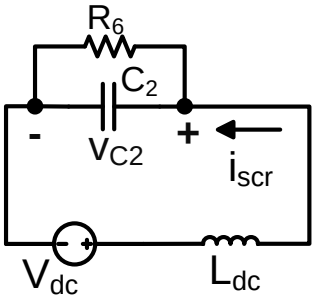


Fig. 9-10. Simplified circuit for the protection circuit with thyristor.

The differential equations and initial conditions can be given by (9-3). The equations for i_{scr} and v_{C2} can be derived in (9-4).

$$\begin{cases} i_{scr} = C_2 \dfrac{dv_{C2}}{dt} + \dfrac{v_{C2}}{R_6} \\ v_{C2} = V_{dc} - L_{dc} \dfrac{di_{scr}}{dt} \\ i_{scr}(0) = I_{dc} \\ v_{C2}(0) = 0 \end{cases} \tag{9-3}$$

With the analytical equations, the waveforms of i_{scr} and v_{C2} can be drawn with different C_2 and R_6. As shown in Fig. 9-11 when $V_{dc} = 680\ V$, $L_{dc} = 1.9\ mH$, $I_{dc} = 20\ A$ and $C_2 = 10\ \mu F$, the resistor R_6 is selected to be 35 Ω to meet both design rules in this case.

$$\begin{cases} v_{C2} = ae^{x_1 t} + be^{x_2 t} + V_{dc} \\ i_{scr} = \left(aC_2x_1 + \dfrac{a}{R_6}\right)e^{x_1 t} + \left(bC_2x_2 + \dfrac{b}{R_6}\right)e^{x_2 t} + \dfrac{V_{dc}}{R_6} \\ x_1 = \dfrac{-L_{dc} + \sqrt{L_{dc}^2 - 4L_{dc}C_2R_6^2}}{2R_6L_{dc}C_2} \\ x_2 = \dfrac{-L_{dc} - \sqrt{L_{dc}^2 - 4L_{dc}C_2R_6^2}}{2R_6L_{dc}C_2} \\ a = \dfrac{I_{dc} + V_{dc}C_2x_2}{C_2(x_1 - x_2)} \\ b = \dfrac{-I_{dc} - V_{dc}C_2x_1}{C_2(x_1 - x_2)} \end{cases} \tag{9-4}$$

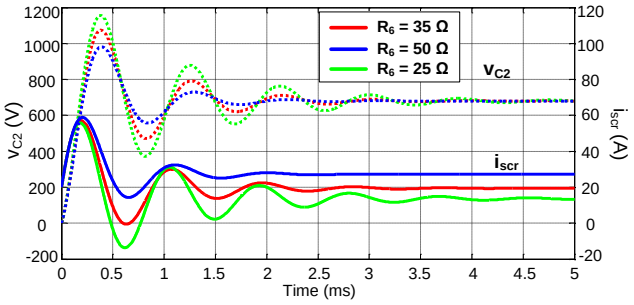
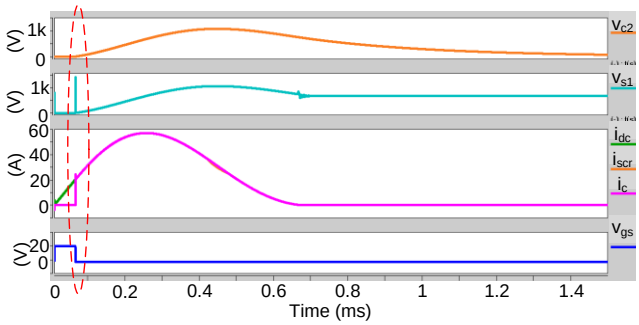
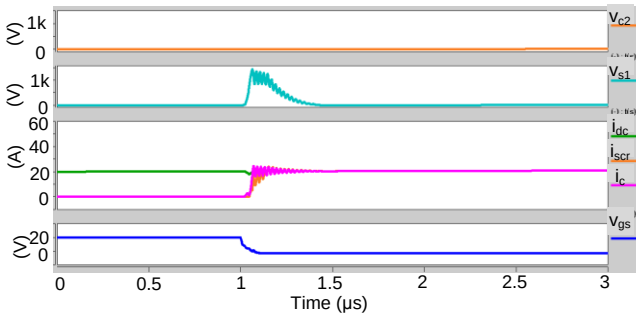


Fig. 9-11. Analysis with different R_6.

The simulation results with the thyristor are shown in Fig. 9-12(a) and (b). The protection circuit works well to clamp the overvoltage and dissipate the inductor energy.



(a)



(b)

Fig. 9-12. Simulation results with thyristor: (a) Overview; (b) Enlarged.

9.3 Experimental Verification

The performance of the proposed protection scheme is experimentally tested in both pulse test and converter test. In the pulse test, the function of the protection is verified and some layout issues related with the protection performance are studied. Then, it is examined in a 7.5 kW current source rectifier built with SiC MOSFETs.

9.3.1 Pulse Test

The simplified overvoltage protection is tested in the pulse test circuit in Fig. 9-13. The circuit includes a double pulse tester, which has two switches S1 and S2 commutating with each other [138]. The protection circuit is connected to the circuits on the nodes a, b and p. The Si

IGBT M1 with desaturation protection is connected in series with S1 as a circuit breaker to prevent overcurrent.

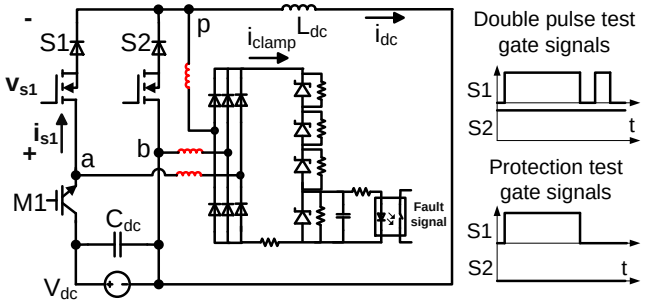


Fig. 9-13. Pulse test circuit for proposed protection.

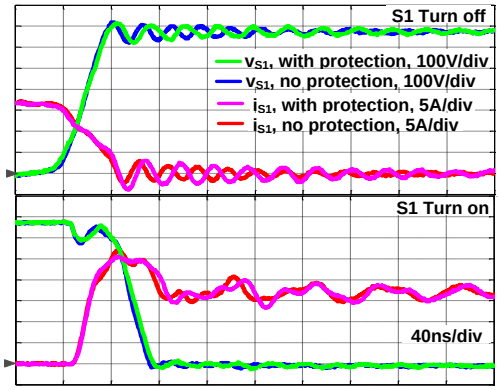


Fig. 9-14. Impact of the protection circuit to SiC MOSFETs.

First, the impact of the added protection circuit to the switching performance of the SiC MOSFETs is evaluated. The double pulse test is used to capture the switching waveforms on S1 with and without the protection circuit. The experiment is carried out when $V_{dc} = 680\,V$, $i_{dc} = 17\,A$ and the gate signals of two switches are shown in Fig. 9-13. As shown in Fig. 9-14, the turn-on and turn-off waveforms have a little larger resonance with the protection circuit. But they are very close in most parts. So the proposed protection scheme will not affect much the switching performance of SiC MOSFETs.

To test the overvoltage protection, S1 is gated with one pulse while S2 is kept off as shown in Fig. 9-13. The inductor current can be built up to the required level. When S1 is turned off, an overvoltage occurs on it. The typical waveform is shown in Fig. 9-15 when $V_{dc} = 300\,V$, $i_{dc} = 19\,A$. When S1 is turned off at t_1, the voltage is clamped at around 1130 V for 36 μs and the inductor energy is dissipated on the TVS diodes in the protection circuit. The enlarged waveforms at t_1 is shown in Fig. 9-16, where v_{S1} reaches the clamping voltage within 50 ns. The protection circuit works well to protect the SiC MOSFETs in the pulse test. There is some resonance in the voltage waveform in Fig. 9-16, which is caused by the parasitics in the clamping circuit. The trace length in the protection circuit should be minimized in the layout. Otherwise, the resonance will get even worse, as shown in Fig. 9-17 and Fig. 9-18.

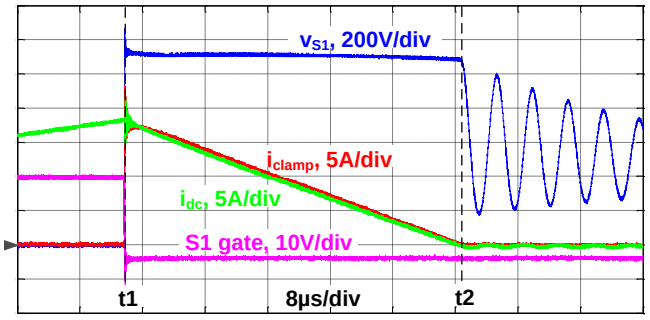


Fig. 9-15. Overvoltage protection waveforms in pulse test.

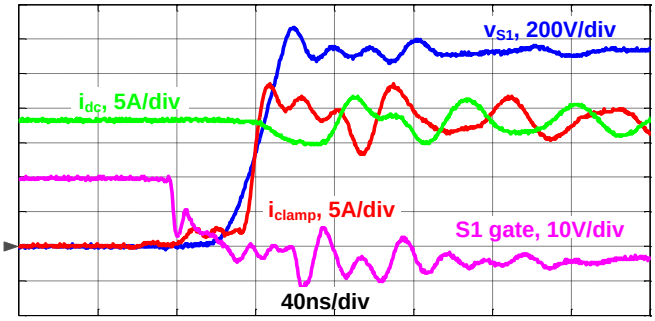


Fig. 9-16. Enlarged waveforms at t_1 in pulse test.

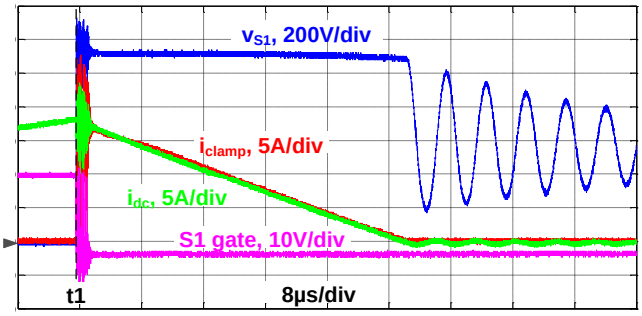


Fig. 9-17. Overvoltage protection waveforms with bad layout.

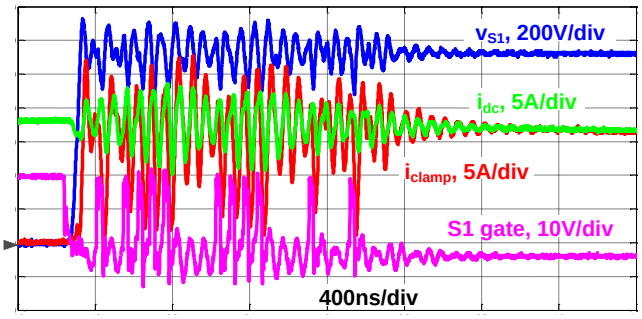


Fig. 9-18. Enlarged waveforms at t_1 with bad layout.

9.3.2 Converter Test

The proposed protection scheme is further tested in a 7.5 kW current source rectifier built with SiC MOSFETs [86]. The parameters of the rectifier and protection circuit are listed in Table 9-1 and Table 9-2 respectively. The photo of the converter prototype is shown in Fig. 9-19 and the proposed protection circuit has a small area on the PCB board as shown in Fig. 9-20. It is placed very close to the SiC MOSFETs so that the parasitic inductance in the clamping circuit will be well minimized. The waveforms are shown in Fig. 9-21 when the converter is operating at full load.

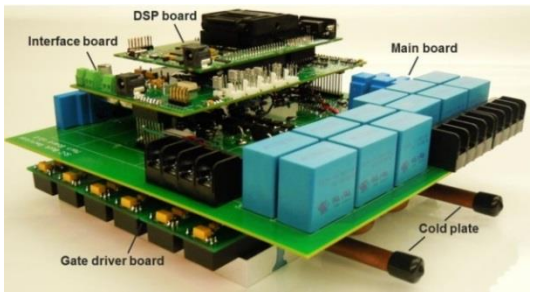


Fig. 9-19. 7.5 kW all-SiC current source rectifier.

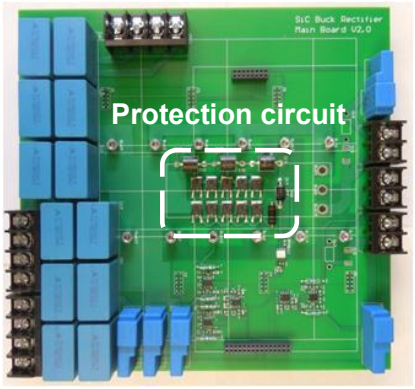


Fig. 9-20. Protection circuit.

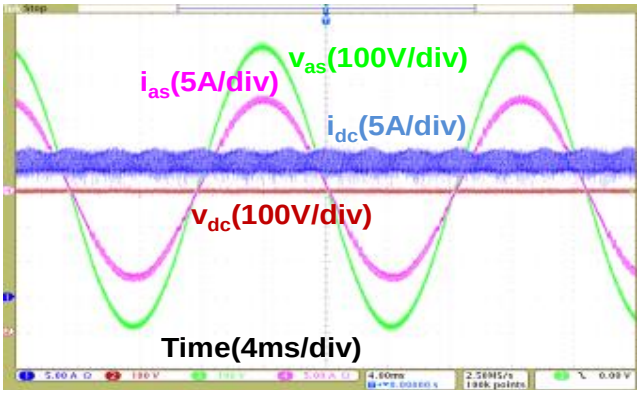


Fig. 9-21. Experimental waveforms of converter at full load.

To create an overvoltage fault in the converter, the freewheeling diode Df is removed from the rectifier. The converter is operating normally at full load, and then the upper three switches are turned off simultaneously to interrupt the dc-link current and generate overvoltage on the

devices. The experimental waveforms are shown in Fig. 9-22 and the enlarged waveforms at t_1 are shown in Fig. 9-23. S1 is turned off at t_1 and the dc-link inductor current is interrupted. The protection circuit can clamp the device voltage at 1170 V and dissipate the inductor energy safely.

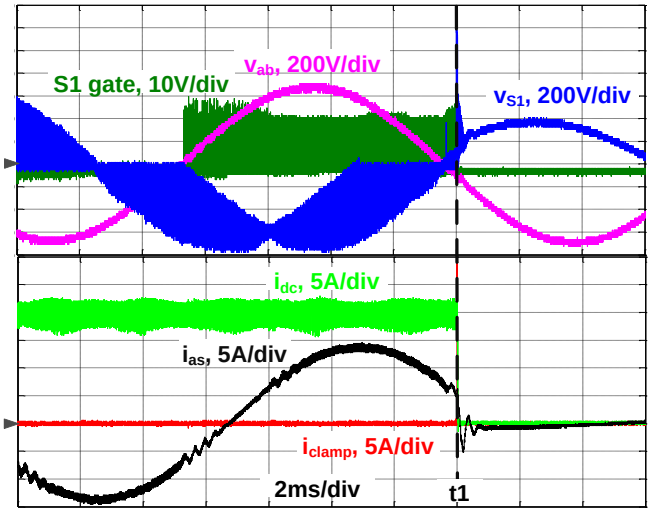


Fig. 9-22. Overvoltage protection waveforms in converter test.

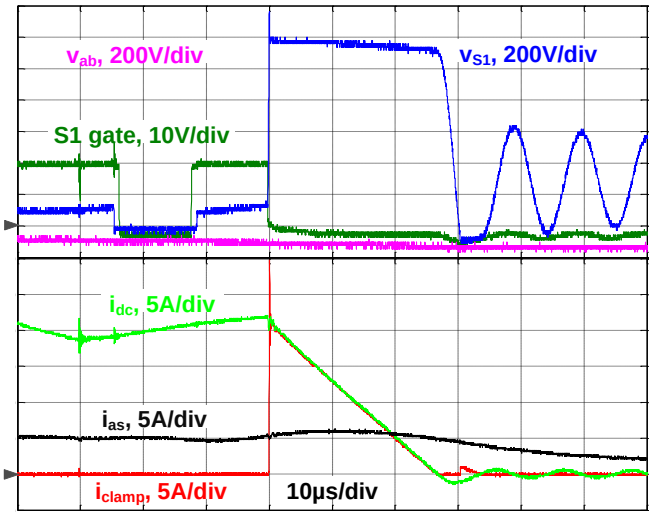


Fig. 9-23. Enlarged waveforms at t_1 in converter test.

9.4 Conclusion

In this chapter, a novel overvoltage protection scheme is proposed for the three-phase current source rectifier built with SiC MOSFETs. The diode bridge is used to detect the overvoltage on the devices. Then the TVS diodes can clamp it and send the error signal to the controller. A thyristor in series with a capacitor can further increase the power capacity of the protection circuit. It is verified in both pulse test and converter test that the proposed protection can clamp the overvoltage within 50 ns and protect the devices effectively. The proposed protection scheme can also be applied to the matrix converter and other types of converters to protect the devices from overvoltage caused by inductor current interruption.

10 Control under Input Voltage Disturbance and Harmonics

In this chapter, the control algorithm will be proposed for current source rectifier to deal with harmonics and voltage sag in the input ac voltage.

10.1 Nonideality in Ac Input Voltage

The three-phase ac voltages of CSR are not always ideally symmetric and sinusoidal. They usually include harmonics and voltage sag/swell, which will exacerbate the performance of the converter.

For various applications, the industry has come up with some standards for the converter to comply with. The International Electrotechnical Commission (IEC) has adopted the IEC 61000-3-2 harmonics standard to limit the harmonics of equipment [139]. The Institute of Electrical and Electronics Engineers (IEEE) has released the IEEE 519-2014 for harmonic control in electric power systems [140].

In Information Technology (IT) industry, the equipment is required to operate normally for certain amount of time under voltage sag/swell. The ITIC curve is shown in Fig. 10-1, where the equipment should operate without interruption within the blue area [141]. Some companies like IBM have their own internal standards on power line disturbance [142]. IEC releases the standard IEC 61000-4-34 to define the voltage dip test levels, including the phase-to-neutral dip and the phase-to-phase dip [143].

In the test of CSR, the input grid voltage is found to contain some harmonics, as shown in Fig. 10-2 [144]. There is 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonics in the grid voltage, leading to 3.3% voltage THD. Due to these harmonics, the input current of CSR is distorted, as shown in [144].

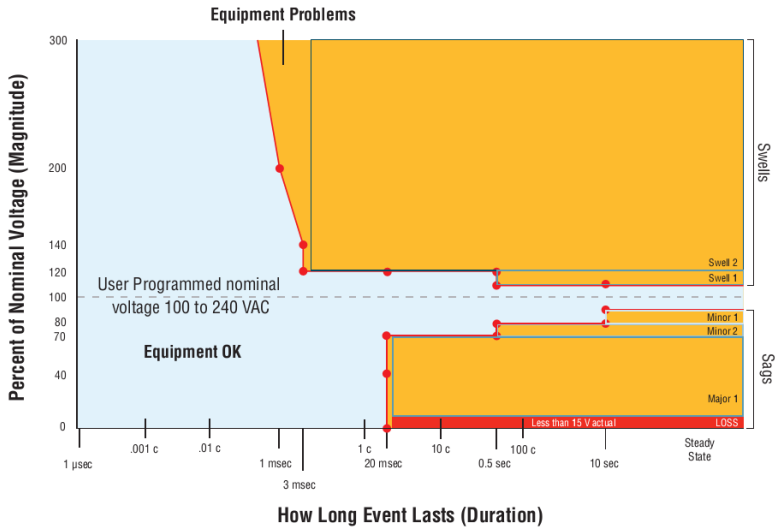
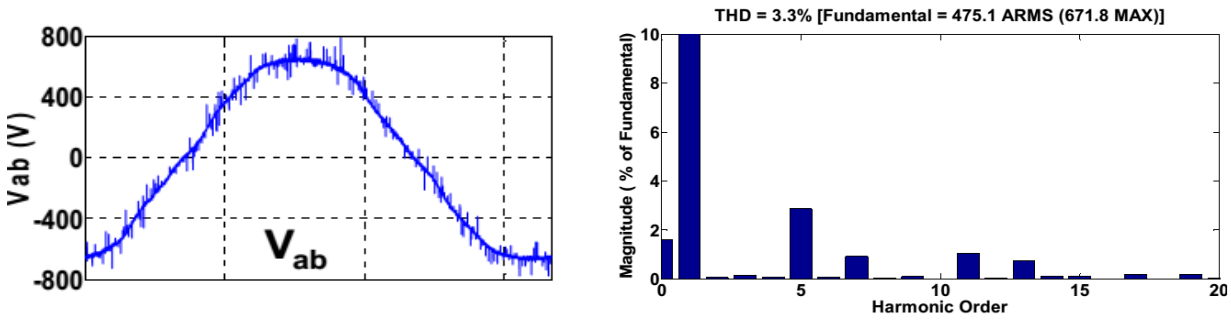


Fig. 10-1. ITIC curve [141].



(a) (b)

Fig. 10-2. Grid voltage with harmonics: (a) Voltage waveform; (b) Voltage Spectrum [144].

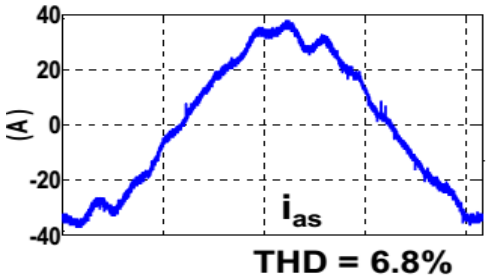


Fig. 10-3. Input current waveform of CSR with distortion [144].

10.2 Traditional Control Algorithm

10.2.1 Modeling of CSR

With the method proposed in [145], the average model of three-phase CSR is shown in Fig. 10-4 in abc coordinates, including three ac circuits and a dc circuit. The model can be expressed by (10-1), where d_a, d_b and d_c are the duty cycles of phase a, phase b and phase c respectively.

$$\begin{bmatrix} i_{as} \\ i_{bs} \\ i_{cs} \end{bmatrix} = C_s \begin{bmatrix} dv_a/dt \\ dv_b/dt \\ dv_c/dt \end{bmatrix} + \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}$$

$$\begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix} = L_s \begin{bmatrix} di_{as}/dt \\ di_{bs}/dt \\ di_{cs}/dt \end{bmatrix} + \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{10-1}$$

$$i_L = i_{dc} + C_{dc} \frac{dv_{dc}}{dt}$$

$$v_{dc} = d_a v_a + d_b v_b + d_c v_c - L_{dc} \frac{di_L}{dt}$$

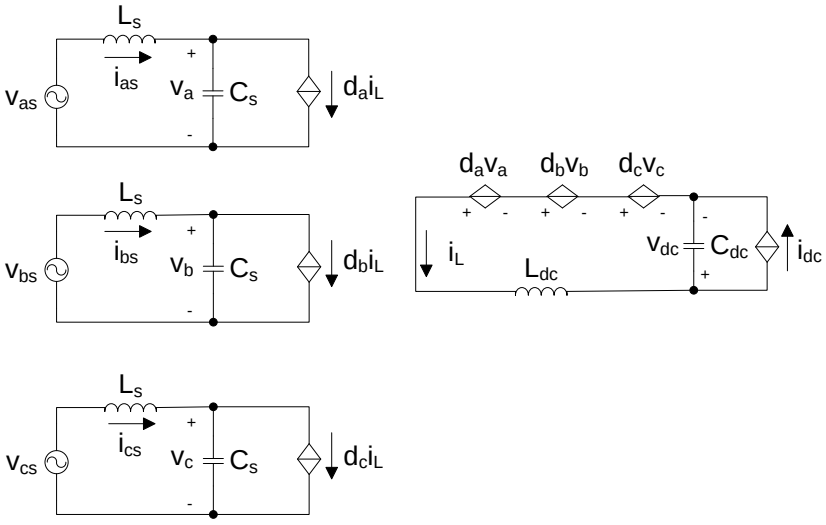


Fig. 10-4. Average model of three-phase CSR in abc coordinates.

Based on the coordinate transformation in (10-2), the average model of CSR in abc coordinates can be transformed into the one in dq0 coordinates, as shown in (10-3) and Fig. 10-5. The 0 channel is omitted in the modeling since its current is always zero.

$$T_{dq0/abc} = \sqrt{\frac{2}{3}}\begin{bmatrix} cos(\omega t-\theta) & cos\left(\omega t-\theta-\frac{2\pi}{3}\right) & cos\left(\omega t-\theta+\frac{2\pi}{3}\right) \\ -sin(\omega t-\theta) & -sin\left(\omega t-\theta-\frac{2\pi}{3}\right) & -sin\left(\omega t-\theta+\frac{2\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{10-2}$$

$$\begin{bmatrix} i_{ds} \\ i_{qs} \end{bmatrix} = C_s \begin{bmatrix} dv_d/dt \\ dv_q/dt \end{bmatrix} + \omega C_s \begin{bmatrix} -v_q \\ v_d \end{bmatrix} + i_L \begin{bmatrix} d_d \\ d_q \end{bmatrix}$$

$$\begin{bmatrix} v_{ds} \\ v_{qs} \end{bmatrix} = \omega L_s \begin{bmatrix} -i_{qs} \\ i_{ds} \end{bmatrix} + L_s \begin{bmatrix} di_{ds}/dt \\ di_{qs}/dt \end{bmatrix} + \begin{bmatrix} v_d \\ v_q \end{bmatrix} \tag{10-3}$$

$$i_L = i_{dc} + C_{dc}\frac{dv_{dc}}{dt}$$

$$v_{dc} = d_d v_d + d_q v_q - L_{dc}\frac{di_L}{dt}$$

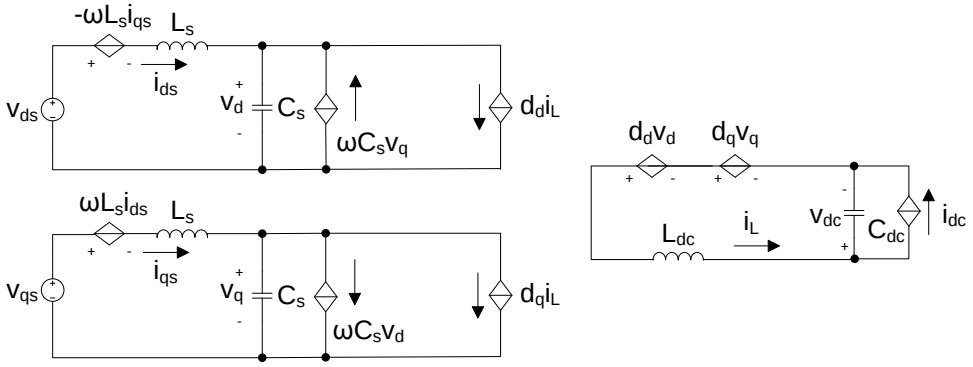


Fig. 10-5. Average model of three-phase CSR in dq coordinates.

After the perturbation and linearization using Taylor expansion, the small signal model and the quiescent operation point are given by (10-4) and (10-5) respectively, where $\hat{x}$ is the disturbance of the variable x near its quiescent operation point X.

$$\begin{bmatrix}\hat{\imath}_{ds}\\ \hat{\imath}_{qs}\end{bmatrix} = C_s\begin{bmatrix}d\hat{v}_d/dt\\ d\hat{v}_q/dt\end{bmatrix} + \omega C_s\begin{bmatrix}-\hat{v}_q\\ \hat{v}_d\end{bmatrix} + I_L\begin{bmatrix}\hat{d}_d\\ \hat{d}_q\end{bmatrix} + \hat{\imath}_L\begin{bmatrix}D_d\\ D_q\end{bmatrix}$$

$$\begin{bmatrix}\hat{v}_{ds}\\ \hat{v}_{qs}\end{bmatrix} = \omega L_s\begin{bmatrix}-\hat{\imath}_{qs}\\ \hat{\imath}_{ds}\end{bmatrix} + L_s\begin{bmatrix}d\hat{\imath}_{ds}/dt\\ d\hat{\imath}_{qs}/dt\end{bmatrix} + \begin{bmatrix}\hat{v}_d\\ \hat{v}_q\end{bmatrix}$$

$$\hat{\imath}_L = \hat{\imath}_{dc} + C_{dc}\frac{d\hat{v}_{dc}}{dt} \tag{10-4}$$

$$\hat{v}_{dc} = D_d\hat{v}_d + D_q\hat{v}_q + \hat{d}_d V_d + \hat{d}_q V_q - L_{dc}\frac{d\hat{\imath}_L}{dt}$$

$$\begin{bmatrix}I_{ds}\\ I_{qs}\end{bmatrix} = \omega C_s\begin{bmatrix}-V_q\\ V_d\end{bmatrix} + I_L\begin{bmatrix}D_d\\ D_q\end{bmatrix}$$

$$\begin{bmatrix}V_{ds}\\ V_{qs}\end{bmatrix} = \omega L_s\begin{bmatrix}-I_{qs}\\ I_{ds}\end{bmatrix} + \begin{bmatrix}V_d\\ V_q\end{bmatrix} \tag{10-5}$$

$$I_L = I_{dc}$$

$$V_{dc} = D_d V_d + D_q V_q$$

Table 10-1. Three-phase current source rectifier parameters

Power Rating	7.5 kW
Input Voltage Rating	Three-phase line-to-line 480 $V_{ac,rms}$
Input Inductor	110 μH each phase
Input Capacitor	10 μF each phase
Output Voltage Rating	400 V_{dc}
Output Inductor	1.9 mH
Output Capacitor	150 μF
Switching Frequency	28 kHz

With the small-signal model, the transfer function can be derived for CSR which is complicated due to the second-order filters on both ac and dc sides. With the SISO tool in Matlab/Simulink, the bode plot of the transfer function $\hat{\imath}_{dc}/\hat{d}_d$ is shown in Fig. 10-6, where 1.5 switching period delay is added considering the delay in the controller and modulator. The parameters of CSR are listed in Table 10-1.

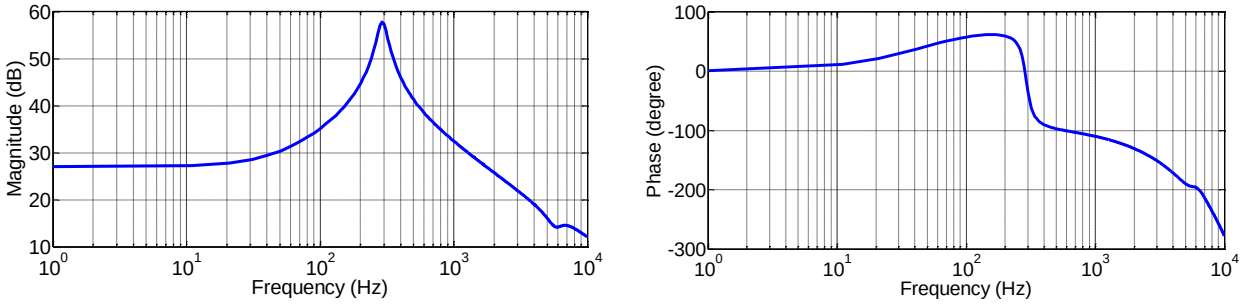


Fig. 10-6. Bode plots of transfer function $\hat{\imath}_{dc}/\hat{d}_d$.

10.2.2 Performance under Normal Input Ac Voltage

In three-phase CSRs, the controller is usually designed in dq rotating coordinate system where the converter model is time-invariant [131]. Usually the digital controller includes two control loops as shown in Fig. 10-7. In the outer dc voltage control loop, the voltage on the output dc capacitor is fed back to the compensator to generate the dc current reference for the inner current control loop. In the current control loop, the current in the dc-link inductor is fed back to the current compensator to generate D_d, the duty cycle on the d axis. Then the space vectors are synthesized and the duty ratios d_1 and d_2 are calculated for modulator to generate PWM signal for each switch.

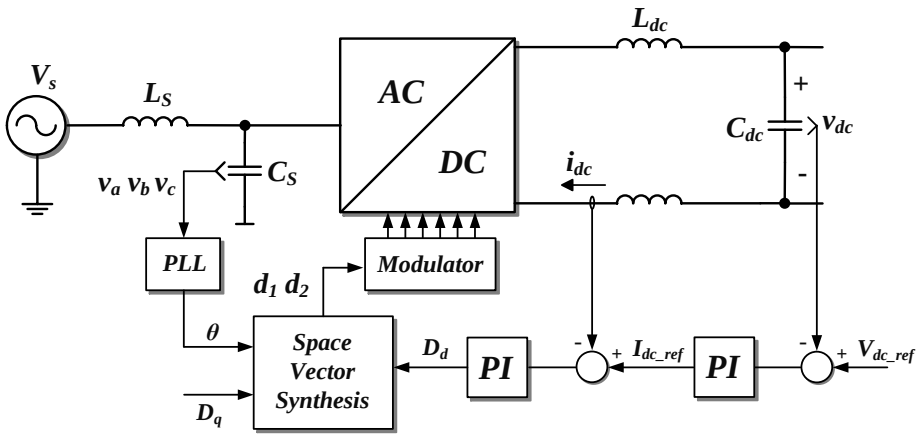


Fig. 10-7. Traditional control algorithm.

Proportional-integral controller (PI) is applied as the compensator in dc current control loop, as given by (10-6).

$$H_{i_{dc}} = k_{p\_i_{dc}} + \frac{k_{i\_i_{dc}}}{s} \tag{10-6}$$

When $k_{p\_i_{dc}} = 0.0116$ and $k_{i\_i_{dc}} = 14.298$, the bode plots of the loop gain in the dc current control loop can be drawn in Fig. 10-8. The phase margin is 61.2 degrees under 609 Hz, and the gain margin is 20.5 dB under 4.3 kHz.

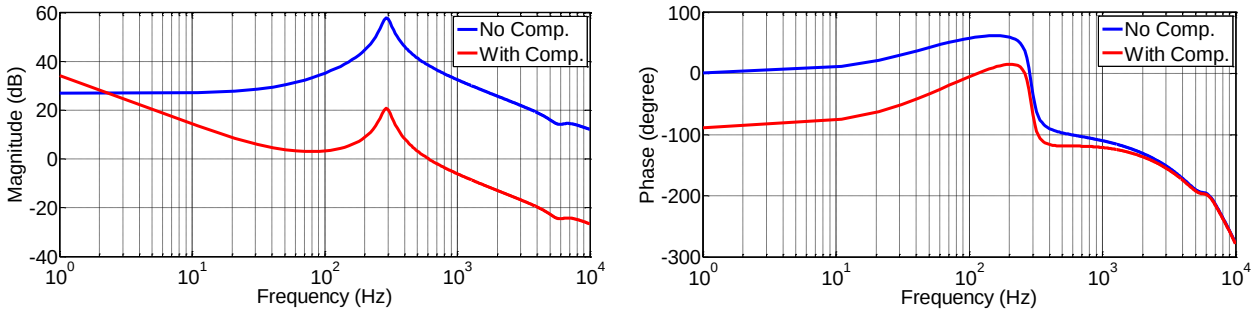


Fig. 10-8. Bode plots of transfer function $\hat{\imath}_{dc}/\hat{d}_d$ with current compensator.

The bode plots of the transfer function $\hat{v}_{dc}/\hat{\imath}_{dc}$ are drawn in Fig. 10-9.

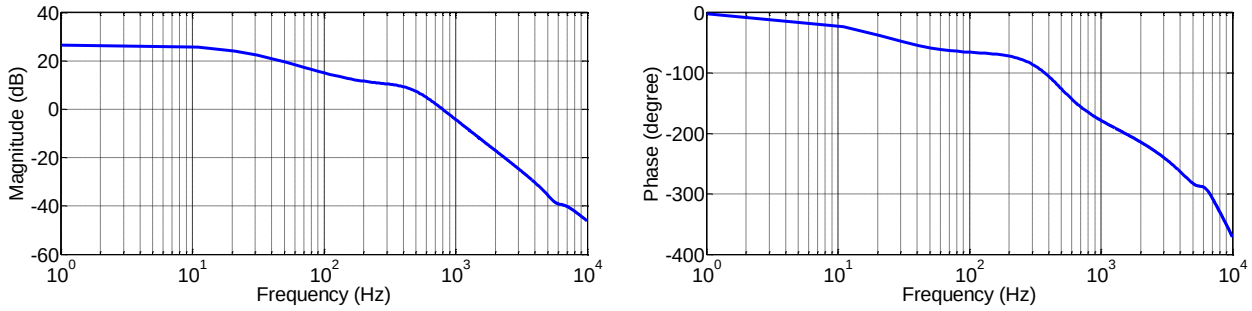


Fig. 10-9. Bode plots of transfer function $\hat{v}_{dc}/\hat{\imath}_{dc}$.

The dc voltage control loop should be much slower than the dc current control loop. PI controller is applied as the compensator in dc voltage control loop, as given by (10-7).

$$H_{v_{dc}} = k_{p\_v_{dc}} + \frac{k_{i\_v_{dc}}}{s} \tag{10-7}$$

When $k_{p\_v_{dc}} = 7.67 \times 10^{-3}$ and $k_{i\_v_{dc}} = 7.67$, the bode plots of the loop gain in the dc voltage control loop can be drawn in. The phase margin is 60 degrees under 20 Hz, and the gain margin is 43.3 dB under 863 Hz.

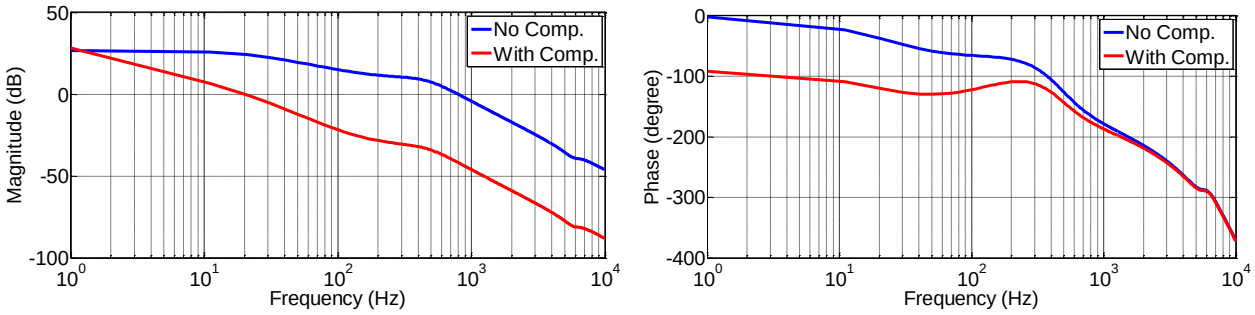


Fig. 10-10. Bode plots of transfer function $\hat{v}_{dc}/\hat{\imath}_{dc}$ with voltage compensator.

There is no feedback control of the input currents. The input current is decided by the dc-link current and the duty cycle. The traditional controller works well under normal operation when the three-phase input voltages are symmetric and sinusoidal, as shown in Fig. 10-11. The input current Total Harmonic Distortion (THD) is 5%.

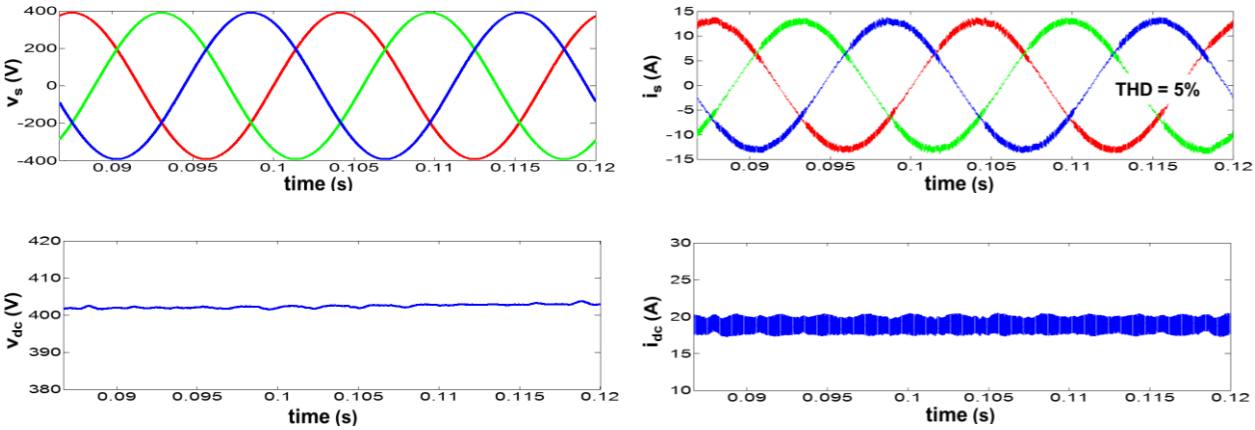


Fig. 10-11. Simulation waveforms with traditional controller under normal conditions.

At the step change of the load current, the waveforms are shown in Fig. 10-12.

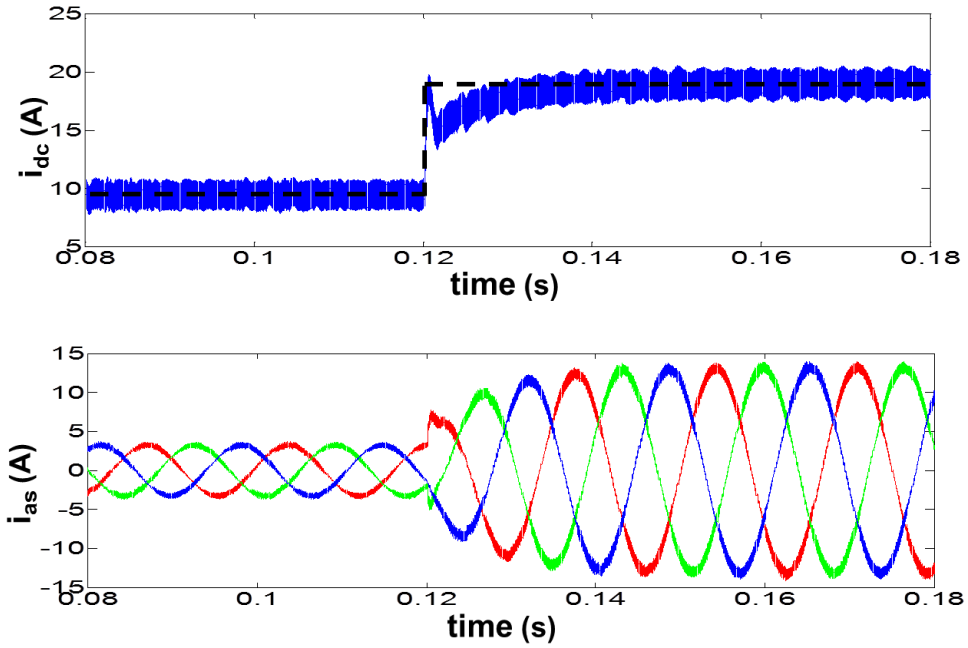


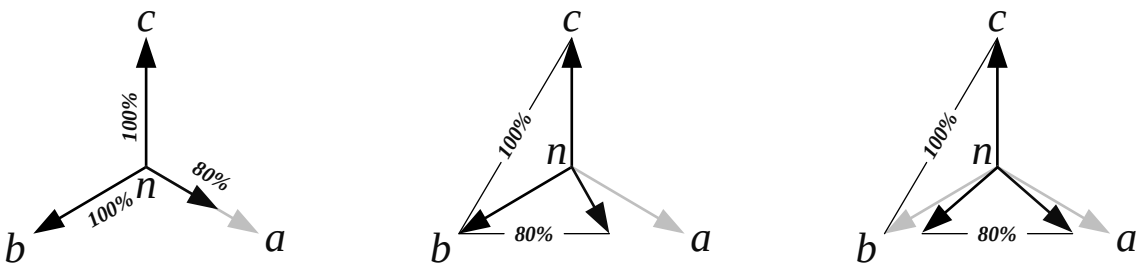
Fig. 10-12. Simulation waveforms with traditional controller under step change.

10.2.3 Performance under Ac Voltage Sag

It should be mentioned that the maximum amplitude of line-to-line voltage should be always larger than dc output voltage for step-down operation of CSR, which is given by (10-8).

$$max(|v_{ab}(t)|, |v_{bc}(t)|, |v_{ca}(t)|) > V_{dc} \tag{10-8}$$

When the ac voltage sag occurs, the three voltages are not symmetric. In this case, the traditional controller may not work consistently well. There are mainly three types of voltage sags defined in IEC 61000-4-34 [143], as shown in Fig. 10-13. Fig. 10-13(a) is the line-to-neutral voltage sag. Fig. 10-13(b) and Fig. 10-13(c) are two types of line-to-line voltage sags.



(a) (b) (c)

Fig. 10-13. Three types of ac voltage sag: (a) Type A; (b) Type B; (c) Type C.

Type A voltage sag is simulated in CSR with traditional control algorithm. The waveforms under Type A voltage sag are shown in Fig. 10-14. During the voltage sag, the input current THD increases from 5% to 6%.

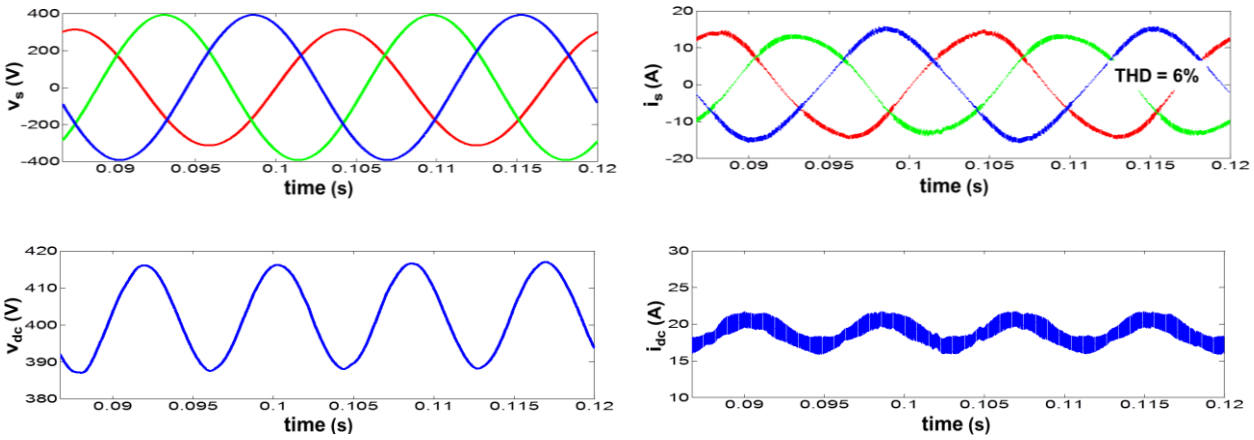


Fig. 10-14. Simulation waveforms with traditional controller under Type A voltage sag.

There is large second-order ripple in the dc voltage and current. It is caused by the negative sequence components in the input ac voltages [146][147][148]. The PI compensator in traditional

control can not track the reference well when there is second-order ripple, unless it has much higher cross-over bandwidth. The second-order ripple can not be attenuated much on the dc side.

10.2.4 Performance under Ac Voltage with Harmonics

With 5% 5th order harmonics in the three-phase ac voltages, the simulation waveforms with traditional controller are shown in Fig. 10-15. The THD of the input current increases from 5% to 13%. There is 6th order ripple in the dc voltage and dc-link current.

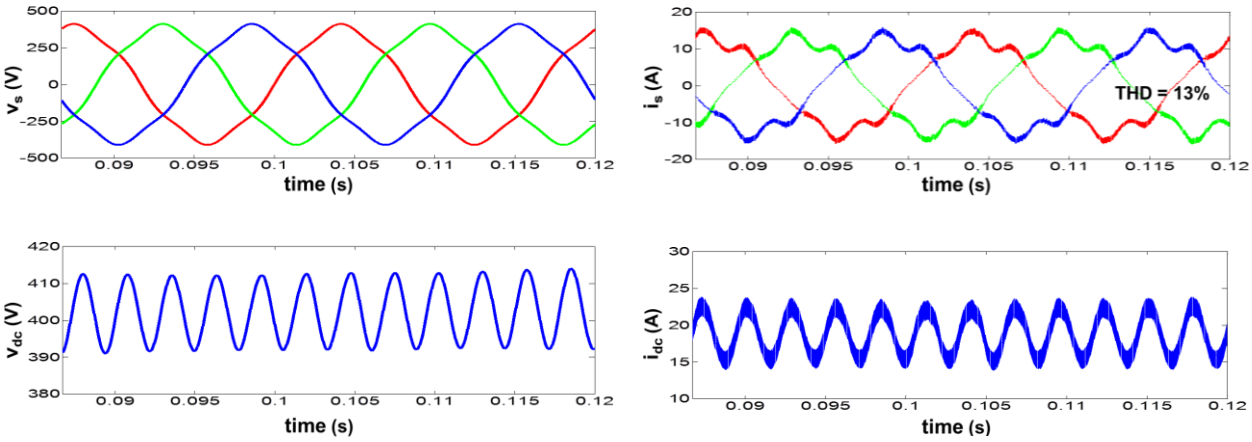


Fig. 10-15. Simulation waveforms with traditional controller under 5th order harmonics.

The 5% 5th order harmonics can be given by (10-9), which are negative sequence components. In dq rotating coordinates of the fundamental frequency, the 5th order harmonics in (10-9) turn to be 6th order ripple in both d axis and q axis.

$$\begin{cases} v_{as\_5th} = 5\% \cdot V_m cos(5\omega t) \\ v_{bs\_5th} = 5\% \cdot V_m cos\left(5\omega t + \frac{2\pi}{3}\right) \\ v_{cs\_5th} = 5\% \cdot V_m cos\left(5\omega t - \frac{2\pi}{3}\right) \end{cases} \tag{10-9}$$

There is no ac current compensator in traditional control algorithm to attenuate the harmonics.

10.3 Proposed Control Algorithm

To deal with the harmonics and the ac voltage sag, a new control algorithm is proposed, as shown in Fig. 10-16. In this control algorithm, the three-phase ac currents i_{as}, i_{bs} and i_{cs} are fed back and transformed into i_{ds} and i_{qs} in dq0 coordinates. Two ac current compensators, i_{ds} compensator and i_{qs} compensator, are added in the controller. Moreover, the proportional-resonant (PR) compensator is added to increase the gain and enhance the tracking performance near certain frequencies [149].

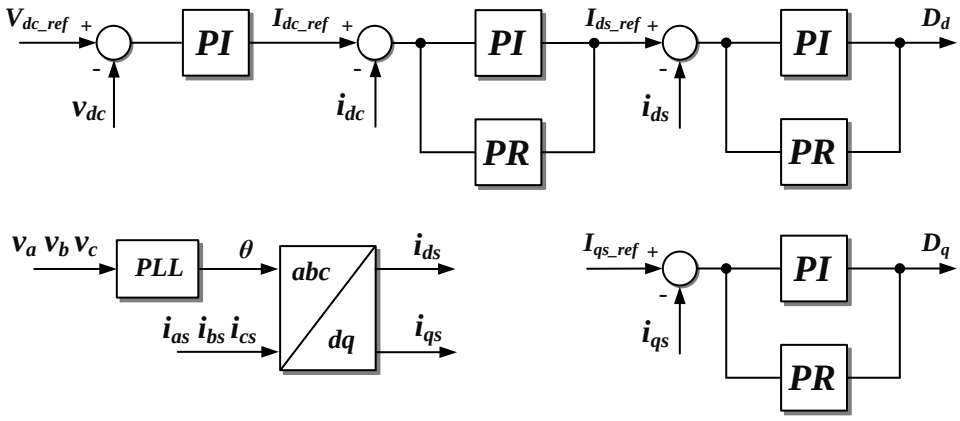


Fig. 10-16. Proposed control algorithm.

The main function of the i_{ds} and i_{qs} compensators is to attenuate the harmonics and track the reference currents I_{ds_ref} and I_{qs_ref} well. I_{ds_ref} is generated by the dc-link current compensator and $I_{qs\_ref} = 0$. As discussed in 10.2.4, the 5th order negative-sequence harmonic ac current appears to be 6th order ripple in i_{ds} and i_{qs}. The compensator needs large gain near 6th

order frequency (360 Hz), which can be provided by a PR compensator as shown in Fig. 10-17. The transfer function of PR compensator is given by (10-10), where ω_c is the bandwidth (5 - 15 rad/s), ω_h is the resonant frequency, k_r is the proportional coefficient [149]. In order to have a high gain around 6th order frequency, ω_h is selected to be $2\pi \times 360 = 2262$ rad/s. The parameters of the i_{ds} and i_{qs} compensators are listed in Table 10-2.

$$H_{PR} = \frac{2k_r\omega_c s}{s^2 + 2\omega_c s + {\omega_h}^2} \tag{10-10}$$

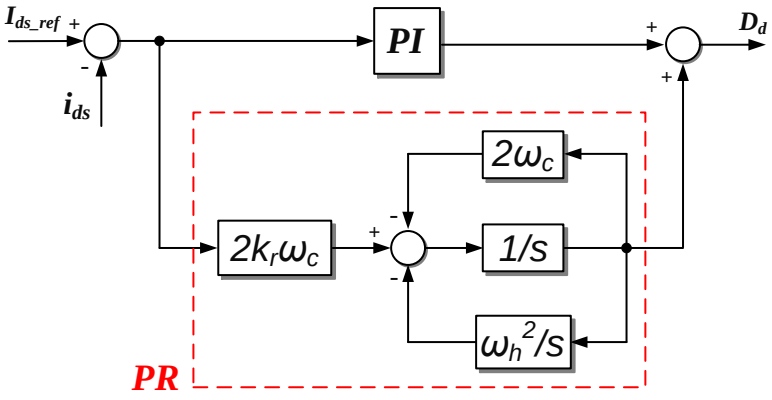


Fig. 10-17. PR compensator in i_d control loop.

Table 10-2. Parameters in i_{ds} and i_{qs} compensators

Control loop	PI compensator		PR compensator		
	k_p	k_i	k_r	ω_c	ω_h
i_{ds}	0.0135	50.0	2	10	2262
i_{qs}	7.11×10^{-4}	50.8	2	10	2262

The bode plots of the transfer function $\hat{\imath}_{ds}/\hat{d}_d$ are drawn in Fig. 10-18. The phase margin is 45 degrees under 900 Hz. The gain margin is 2.4 dB under 5.27 kHz. The bode plots of the transfer function $\hat{\imath}_{qs}/\hat{d}_q$ are drawn in Fig. 10-19. The phase margin is 88 degrees under 131 Hz. The gain margin is 17.6 dB under 4.16 kHz.

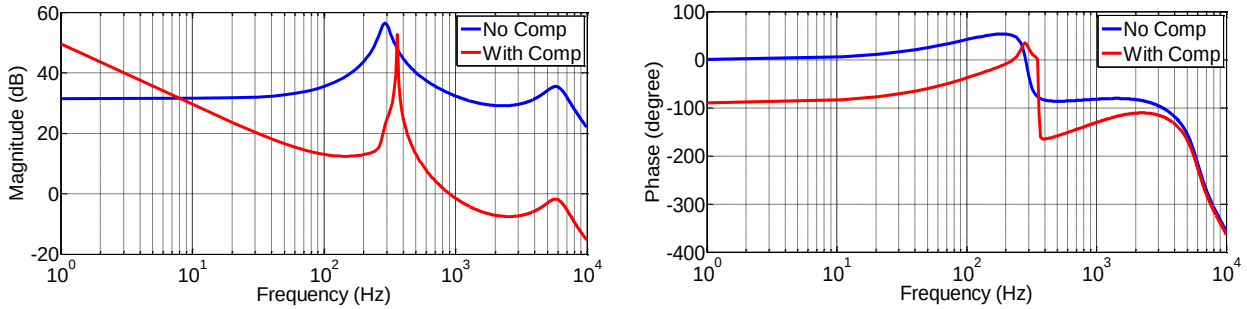


Fig. 10-18. Bode plots of transfer function $\hat{\imath}_{ds}/\hat{d}_d$ with compensator.

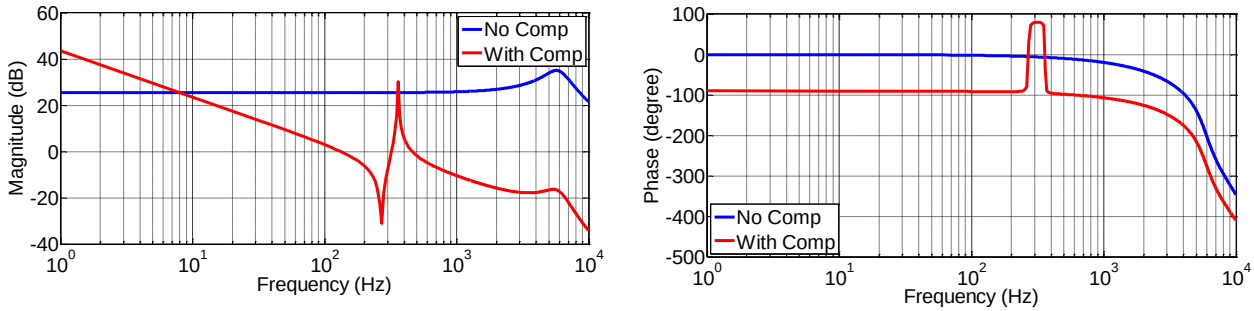


Fig. 10-19. Bode plots of transfer function $\hat{\imath}_{qs}/\hat{d}_q$ with compensator.

In the dc-link current i_{dc} control loop, the PR compensator can be applied to increase the gain at the 2nd order frequency. In this way, the controller can still track the reference dc current well in presence of 2nd order ripple when the three-phase ac voltages are not balanced. The PI compensator is utilized in dc voltage v_{dc} control loop. The parameters in i_{dc} and v_{dc} compensators are listed in Table 10-3.

Table 10-3. Parameters in i_{dc} and v_{dc} compensators

Control loop	**PI compensator**		**PR compensator**		
	$\boldsymbol{k_p}$	$\boldsymbol{k_i}$	$\boldsymbol{k_r}$	$\boldsymbol{\omega_c}$	$\boldsymbol{\omega_h}$
$\boldsymbol{i_{dc}}$	0.0269	128	1	10	754
$\boldsymbol{v_{dc}}$	0.0806	2.6	N/A	N/A	N/A

The bode plots of the transfer function $\hat{\imath}_{dc}/\hat{\imath}_{ds}$ are drawn in Fig. 10-20. The phase margin is 95 degrees under 11 Hz. The gain margin is 44 dB under 4.88 kHz. The bode plots of the transfer function $\hat{v}_{dc}/\hat{\imath}_{dc}$ are drawn in Fig. 10-21. The phase margin is 97 degrees under 16 Hz. The gain margin is 39.6 dB under 666 Hz.

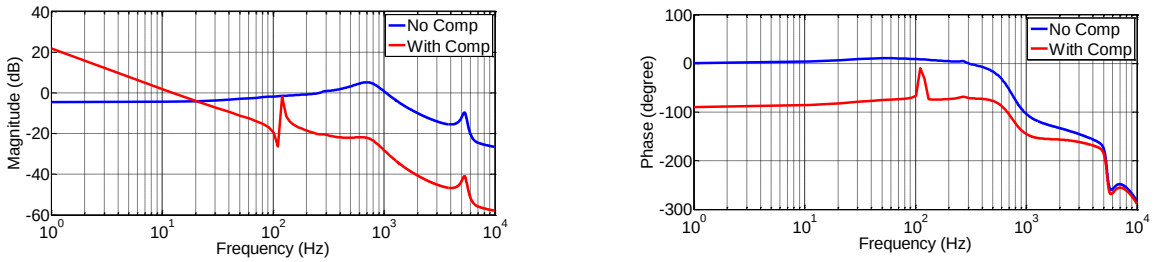


Fig. 10-20. Bode plots of transfer function $\hat{\imath}_{dc}/\hat{\imath}_{ds}$ with compensator.

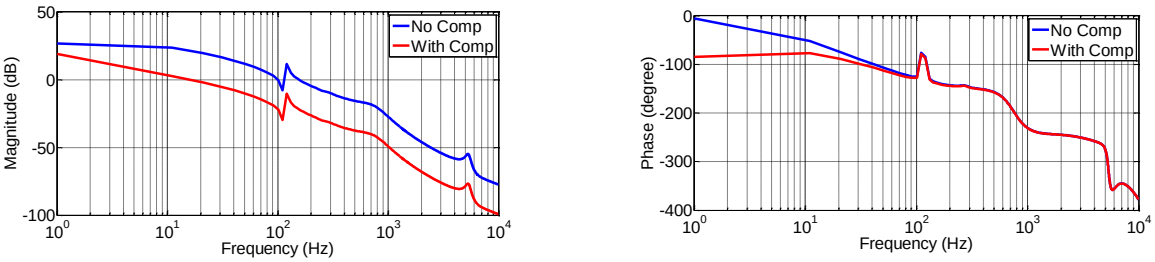


Fig. 10-21. Bode plots of transfer function $\hat{v}_{dc}/\hat{\imath}_{dc}$ with compensator.

10.3.1 Performance under Normal Input Ac Voltage

Under normal input ac voltages, the simulation waveforms of the proposed controller are shown in Fig. 10-22. The input current Total Harmonic Distortion (THD) is 5%.

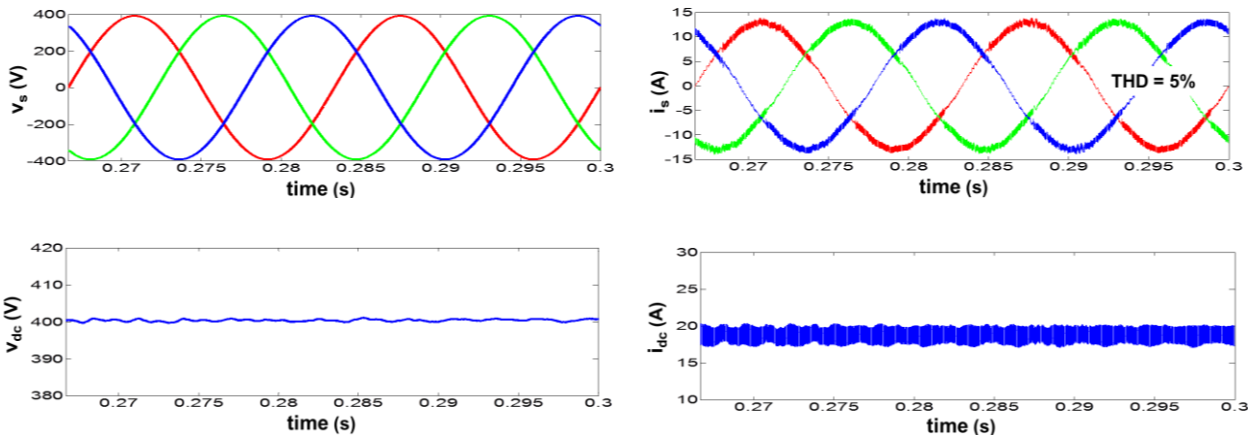


Fig. 10-22. Simulation waveforms with proposed controller under normal conditions.

At the step change of the load current, the waveforms are shown in Fig. 10-23. Since the bandwidth of i_{dc} control is much lower than that in the traditional controller, the transition takes longer in Fig. 10-23.

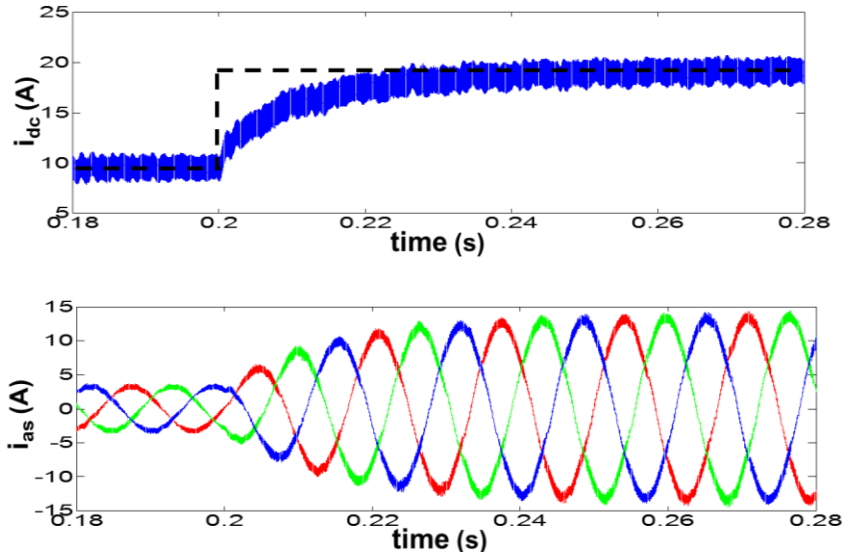


Fig. 10-23. Simulation waveforms with proposed controller under step change.

10.3.2 Performance under Ac Voltage Sag

The waveforms under Type A voltage sag are shown in Fig. 10-24. During the voltage sag, the input current THD is kept around 5%. The second-order ripple is largely reduced compared with that in Fig. 10-14.

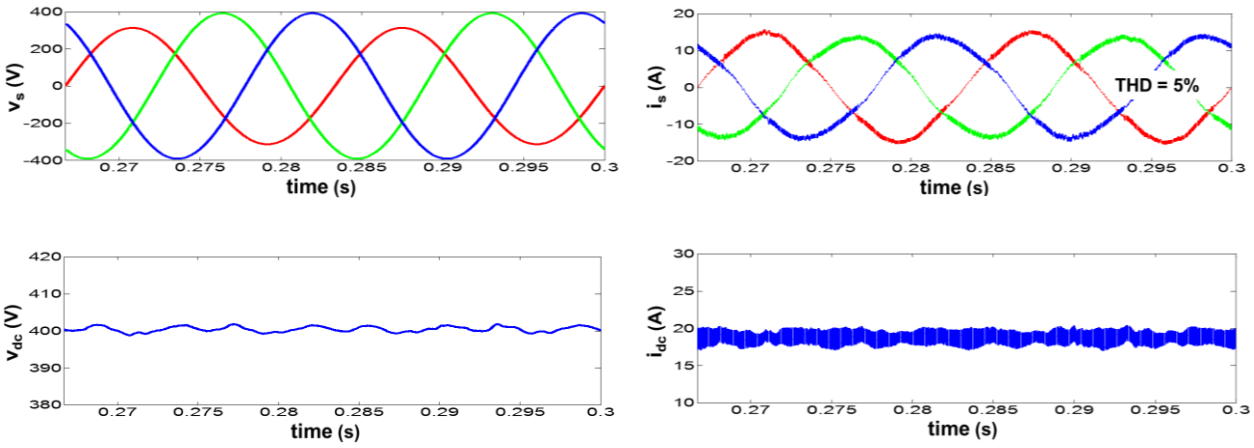


Fig. 10-24. Simulation waveforms with proposed controller under Type A voltage sag.

10.3.3 Performance under Ac Voltage with Harmonics

With 5% 5th order harmonics in the three-phase ac voltages, the simulation waveforms with the proposed controller are shown in Fig. 10-25. The THD of the input current is kept around 5%. The 6th order ripple on the dc voltage and dc-link current is largely reduced compared with that in Fig. 10-15.

It should be noticed that the proposed controller can be generalized to different orders of ac harmonics. The PR compensators corresponding to different harmonics can be added in the i_d and i_q control loops.

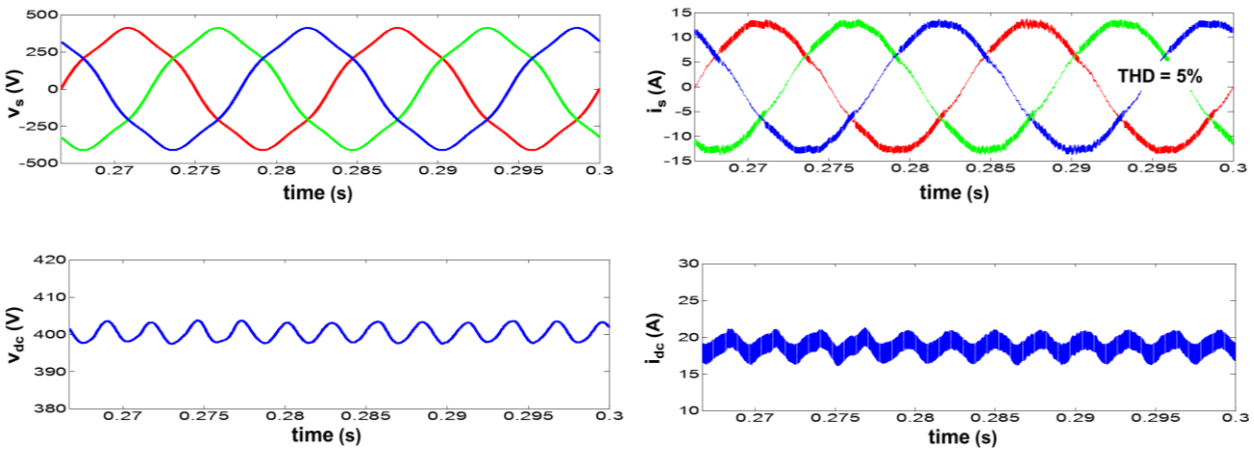


Fig. 10-25. Simulation waveforms with proposed controller under 5th order harmonics.

10.4 Conclusion

In this chapter, a control algorithm is proposed to control the three-phase CSR under voltage disturbance and harmonics. To control CSR under harmonics, two current control loops are added to control the ac currents. The proportional-resonant (PR) compensator is used to improve the tracking capability of the controller under harmonics. It is verified through

simulation that the proposed control can reduce the 2^{nd} order ripple on the dc side when ac voltage sag occurs. Moreover, the proposed control can reduce the input current THD when the ac input voltage contains harmonics.

In order for CSR to work under voltage sag, the maximum amplitude of line-to-line voltage should be always larger than dc output voltage for step-down operation of CSR. If one ac phase is lost, CSR can not support the dc bus voltage normally. In this case, a boost stage can be added after the dc-link inductor, as proposed in [150][151].

11 Conclusion and Future Work

11.1 Conclusion

In this dissertation, the potential benefits of the three-phase current source rectifier were evaluated in high power rectifier, data center power supply and dc fast charger for EVs. Then new techniques were proposed to increase the power efficiency and power density of the current source rectifier. The conclusions can be drawn as follows.

- A new current source rectifier topology, Delta-type Current Source Rectifier (DCSR), was proposed. It has delta connection on its input side and the dc-link current can be shared by more switches to reduce the conduction loss. The conduction states and modulation schemes were analyzed for the new topology. The analytical equations of the current stress were derived for the design of the DCSR. Compared with the traditional CSR, the proposed topology was shown to have lower device current stress and conduction loss. A 7.5 kW prototype was built to validate the performance of the proposed topology. It has been shown experimentally that the DCSR has higher efficiency over the traditional CSR.

- The CSRs was compared with traditional topologies on efficiency and power density in high power rectifier, power supply for data center and dc fast charger for EVs. It was shown that the DCSR had comparable efficiency and much reduced transformer and filter rating than the 12-pulse thyristor rectifier in high power rectifier application. In data center power supply, CSRs were shown to have higher efficiency than the phase-modular rectifiers. When applied in dc fast charger for EVs, CSRs were shown to have

higher efficiency and power density than two-stage voltage source converter when more die area was applied in the design.

- Two all-SiC phase-leg modules were developed and characterized. The switching performance in CSR was compared with the one in voltage source rectifier (VSR). Because of higher equivalent junction capacitance of the switches in VSR, it had higher current spike but lower voltage spike than CSR. When pushed to higher switching speed, the CSR module was more reliable without any shoot-through problem.

- An all-SiC converter module was designed and characterized for the DCSR. With current sharing in two phase legs, the turn-on switching speed was higher and the switching energy was lower in the DCSR than in the traditional CSR. The minor commutation loops were in parallel to reduce the parasitic inductance in DCSR.

- The different commutation types of a three-phase CSR with a freewheeling dc-bus diode were analyzed through experiments. The lossiest transition was accordingly identified for the different semiconductor device configurations considered. Then the switching loss of CSR was modeled, including both the switch-switch and switch-diode commutations, and the effect of the non-switching devices, where the latter was shown to be negligible compared to the total switching loss. Based on the derived switching loss equations, four modulation schemes were compared for different device combinations, showing how space vectors could be arranged to eliminate the transitions with the highest switching losses.

- A modified pulse-based compensation method was proposed to compensate the charge gain or loss caused by overlap time and slow transition. In addition to the traditional

method that placed the overlap time based on the voltage polarity, the new method first minimized the overlap time to reduce its effect and then compensated the pulse width according to the sampled operating voltage and current. The experiments demonstrated its advantages over traditional methods especially when the switching voltage was near zero.

- The three-phase CSR was modeled in discontinuous current mode (DCM) and the modulation and control methods were proposed for this operating mode. The dc-link current ripple was analyzed first to identify the boundary between continuous current mode (CCM) and DCM. Then the small-signal models were derived for CSR in DCM. Compared with the CCM model, the gain of the transfer function was shown to change significantly in DCM, detrimentally affecting the control performance. To account for this, a DCM modulation scheme was proposed keeping the current continuous during the active space vectors. Lastly, a digital feed-forward compensation method was proposed to compensate the duty cycle error in DCM. It was shown that with the proposed DCM control method, both the output voltage ripple and the input current THD could be largely reduced.

- A novel overvoltage protection scheme was proposed for the three-phase current source rectifier built with SiC MOSFETs. The diode bridge was used to detect the overvoltage on the devices. Then the transient-voltage-suppression (TVS) diodes clamped it and an error signal was sent the controller. A thyristor in series with a capacitor further increased the power capacity of the protection circuit. It was verified in both pulse test and converter test that the proposed protection was able to clamp the overvoltage within 50 ns and protect the devices effectively.

- A control algorithm was proposed to control the three-phase CSR under voltage disturbance and harmonics. To control CSR under harmonics, two current control loops were added to control the ac currents. The proportional-resonant (PR) compensator was used to improve the tracking capability of the controller under harmonics. It was verified through simulation that the proposed control was able to reduce the 2^{nd} order ripple on the dc side when ac voltage sag occurred. Moreover, the proposed control was able to reduce the input current THD when the ac input voltage contained harmonics.

11.2 Future Work

- Delta-type Current Source Rectifier (DCSR)

  To maximize the benefit of DCSR, the dc-link current should be shared equally between two legs. The current sharing depends on the characteristics of the semiconductor devices, as well as the layout of the commutation circuit [152][157].

  In previous research, some work has been done to balance current in paralleled devices (IGBTs and MOSFETs) in a single switch [155]-[157]. The problem is not totally the same in the DCSR, where two legs are in parallel to share the current. Moreover, the location of the paralleled legs depends on the input voltages and the modulation scheme.

  For DCSR design, first the device characteristics were measured with 371B curve tracer [158]. Then the devices with similar characteristics were selected and applied in the prototype. Three legs in DCSR were placed close to each other in PCB layout to reduce the parasitic inductance in the commutation loop. The decoupling capacitors were then distributed on three ac buses. The advanced power module package can be

implemented to further reduce the parasitic inductance in DCSR [159]. In the future, some active control methods invented previously can also be applied in DCSR to control the gate drive signals of the switches to balance the transient and static currents [155]-[157].

The DCSR should be compared in a comprehensive way with other three-phase buck-type rectifier topologies on the die area, efficiency and power density. Also the EMI filter should be designed and tested for DCSR.

Although DCSR can save the conduction loss on the active devices, the conduction loss on the diodes is not reduced. The total conduction loss is still higher than voltage source rectifier with the same power and voltage ratings. The multi-level CSR topology is a possible method to further reduce the conduction loss.

- Advanced reverse-blocking semiconductor device for CSR application

The large conduction loss can also be reduced with advanced reverse-blocking semiconductor device. The Revserse-Blocking IGBT (RB-IGBT) have been developed in recent years to save the conduction loss [69]-[73]. But the RB-IGBT from IXYS was found to have much lower switching speed compared with standard IGBTs in Chapter 6. In recent years, Fuji Electric keeps spending much effort to improve the switching performance of its RB-IGBTs. It is shown that the RB-IGBT can reach comparable switching loss with standard IGBT [73][160].

Another promising device is the lateral GaN power device. It is easy to obtain a bi-directional switch using the GaN lateral HEMTs [161]. Panasonic has developed a 650 V 3.1 $m\Omega cm^2$ GaN Gate Injection Transistor (GIT) [162][163] and applied in matrix

converter [164]. It is possible to apply this 4-quadrant switch in CSR to reduce both the conduction loss and the switching loss in the future.

- Advanced package technique for CSR

  The commutation in CSR usually involves three switches, which is different from that in voltage source converter. The layout proposed in Chapter 5 is limited to a 2-dimentional plane, which may cause the commutation loop to be asymmetric between three switches. For DCSR, the parasitic inductance in the commutation loop will impact the current sharing during switching transient. This problem is possible to be solved if the 3-dimentional layout can be implemented.

11.3 Publication List

Journal Papers

- B. Guo, F. Wang, R. Burgos, and E. Aeloiza, "Modulation scheme analysis for high efficiency three-phase buck rectifier considering different device combinations," Accepted by *IEEE Transactions on Power Electronics*.
- F. Xu, B. Guo, L. M. Tolbert, F. Wang, and B. J. Blalock, "An all-SiC three-phase buck rectifier for high efficiency data center power supplies," *IEEE Transactions on Industry Applications*, vol. 49, no. 6, pp. 2662-2673, Nov./Dec. 2013.

Conference Papers

- B. Guo, F. Wang, and E. Aeloiza, "A novel three-phase current source rectifier with delta-type input connection to reduce device conduction loss," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept. 2014, in press.
- B. Guo, F. Wang, and E. Aeloiza, "Modulation scheme for delta-type current source rectifier to reduce input current distortion," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept. 2014, in press.
- B. Guo, F. Wang, E. Aeloiza, P. Ning, and Z. Liang, "All-SiC power module for delta-type current source rectifier," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept. 2014, in press.

- B. Guo, F. Wang, R. Burgos, and E. Aeloiza, "Control of three-phase buck-type rectifier in discontinuous current mode," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept. 2013, pp. 4864-4871.
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- Z. Zhang, B. Guo, F. Wang, L. M. Tolbert, B. J. Blalock, Z. Liang, and P. Ning, "Methodology for switching characterization evaluation of wide band-gap devices in a phase-leg configuration," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2014, pp. 2534-2541.
- Z. Zhang, B. Guo, F. Wang, L. M. Tolbert, B. J. Blalock, Z. Liang, and P. Ning, "Impact of ringing on switching losses of wide band-gap devices in a phase-leg configuration," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2014, pp. 2542-2549.
- F. Xu, B. Guo, Z. Xu, L. M. Tolbert, F. Wang, and B. J. Blalock, "SiC based current source rectifier paralleling and circulating current suppression," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2013, pp. 402-409.
- F. Xu, B. Guo, L. M. Tolbert, F. Wang, and B. J. Blalock, "Design and performance of an all-SiC three-phase buck rectifier for high efficiency data center power supplies," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept. 2012, pp. 2927-2933.
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Utility Patents

- L. M. Tolbert, F. Wang, B. J. Blalock, F. Xu, and B. Guo, "Three-phase buck rectifier for power supplies," *U.S. Utility Patent Application No. 14/204,403*.
- F. Wang and B. Guo, "Three-phase current source rectifier for power supplies," *U.S. Utility Patent Application No. 14/511,809.*

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