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Low-Voltage Analog Circuit Design Using the Adaptively Biased Body-Driven Circuit Technique

Stephen Christopher Terry
University of Tennessee - Knoxville

To the Graduate Council:

I am submitting herewith a dissertation written by Stephen Christopher Terry entitled "Low-Voltage Analog Circuit Design Using the Adaptively Biased Body-Driven Circuit Technique." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

Benjamin J. Blalock, Major Professor

We have read this dissertation and recommend its acceptance:

Syed K. Islam, Charles L. Britton, Jr., M. Nance Ericson, Vasilios Alexiades

Accepted for the Council:

Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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A Dissertation
Presented for the
Doctor of Philosophy Degree

The University of Tennessee, Knoxville

Stephen Christopher Terry
August, 2005

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Most importantly I wish to acknowledge my family and friends for their support during my doctoral program. I would especially like to thank my wife, Becky, for providing much needed support and encouragement every step of the way.

Abstract

The scaling of MOSFET dimensions and power supply voltage, in conjunction with an increase in system- and circuit-level performance requirements, are the most important factors driving the development of new technologies and design techniques for analog and mixed-signal integrated circuits. Though scaling has been a fact of life for analog circuit designers for many years, the approaching 1-V and sub-1-V power supplies, combined with applications that have increasingly divergent technology requirements, means that the analog and mixed-signal IC designs of the future will probably look quite different from those of the past. Foremost among the challenges that analog designers will face in highly scaled technologies are low power supply voltages, which limit dynamic range and even circuit functionality, and ultra-thin gate oxides, which give rise to significant levels of gate leakage current.

The goal of this research is to develop novel analog design techniques which are commensurate with the challenges that designers will face in highly scaled CMOS technologies. To that end, a new and unique body-driven design technique called adaptive gate biasing has been developed. Adaptive gate biasing is a method for guaranteeing that MOSFETs in a body-driven simple current mirror, cascode current mirror, or regulated cascode current source are biased in saturation—independent of operating region, temperature, or supply voltage—and is an enabling technology for high-performance, low-voltage analog circuits. To prove the usefulness of the new design technique, a body-driven operational amplifier that heavily leverages adaptive gate biasing has been developed. Fabricated on a 3.3-V/0.35-μm partially depleted silicon-on-

insulator (PD-SOI) CMOS process, which has nMOS and pMOS threshold voltages of 0.65 V and 0.85 V, respectively, the body-driven amplifier displayed an open-loop gain of 88 dB, bandwidth of 9 MHz, and PSRR greater than 50 dB at 1-V power supply.

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Chapter 1

Introduction

"Solutions in active threshold regulation, substrate biasing, and novel design architecture will be required to extend the trend for lower supply voltages for mixed-signal applications."

—*International Technology Roadmap for Semiconductors*: Process Integration, Devices, and Structures Chapter, p. 25, 2001 edition; Radio Frequency and Analog/Mixed-Signal Technologies for Wireless Communications Chapter, p. 30, 2003 edition

1.1 Trends in Analog and Mixed-Signal Integrated Circuit Design

The scaling of MOSFET dimensions and power supply voltage, in conjunction with an increase in system- and circuit-level performance requirements, are the most important factors driving the development of new technologies and design techniques for analog and mixed-signal integrated circuits. Though scaling has been a fact of life for analog circuit designers for many years, the approaching 1-V and sub-1-V power supplies, combined with applications that have increasingly divergent technology requirements, means that the CMOS analog and mixed-signal IC designs of the future will probably look quite different from those of the past. Foremost among the challenges that analog designers will face in the highly scaled technologies of the future are very low supply voltages and ultra-thin gate oxides. Very low power supply voltages (< 1 V) are a challenge because

dynamic range and even circuit functionality are limited; whereas ultra-thin gate oxides are a challenge because they give rise to significant levels of gate leakage current.

Commensurate with the changing landscape of CMOS technology, there has been an explosion of interest in novel analog and mixed-signal design techniques that can deal with these challenges. Foremost among these design techniques are (in alphabetical order) body-driven MOSFETs, common-mode level shifting, floating-gate MOSFETs, and switched op-amp. Of these, no single design technique has emerged as the best in all situations; rather, each is useful in certain situations. For instance, switched-op-amp design is useful for low-voltage switched-capacitor circuits; whereas common-mode level shifting with resistors is useful for wide voltage dynamic range, continuous-time signal processing. While no design technique has emerged as the best in all situations, it is the opinion of this author that body driving is one of the least favored and yet one of the potentially most useful of all the low-voltage analog design techniques [1].

Body driving refers to using the MOSFET body terminal as a signal and/or bias input, and it is a useful low-voltage design technique because there is no threshold voltage associated with the body terminal, thus dynamic range is increased. The potential of body driving is illustrated by the fact that it can be used to implement a host of functions important to both continuous-time and discrete-time analog circuits—including a single polarity differential pair with rail-to-rail input common-mode range (ICMR) and simple current mirrors with input *and* output voltages close to V_{DSAT}. However, body driving also has several drawbacks; two of which, the possibility of excessively forward biasing the body–source junction and the roughly three times reduction in transconductance for a

body-driven MOSFET compared to a gate-driven MOSFET, are the among most often cited reasons for not using the body-driven design technique [2].

1.2 Research Goals

The goals of this research can be summarized as follows:

- to investigate the viability of body driving as a low-voltage analog circuit design technique,
- to develop, as necessary, novel body-driven circuit primitives (e.g., current mirrors and differential pairs) that will enable reliable, high-performance body-driven circuits, and
- to prove the usefulness of the new circuit techniques by successfully prototyping a high-performance body-driven operational amplifier.

To meet these ends, previous work in body-driven circuit design has been studied, and the fundamental problems which plagued body driving have been isolated and understood. In addition, a new design technique called adaptive gate biasing has been developed, which has led to the design of robust body-driven simple current mirrors, simple cascode current mirrors, and regulated cascode current mirrors—all of which are capable of operating within a 1-V power supply system. To prove the viability of this design technique an operational amplifier circuit has been designed that operates from a power supply voltage ranging from 1 V to 3.3 V, but which is fabricated on a 3.3-V/0.35-μm partially depleted silicon-on-insulator (PD-SOI) technology that has nMOS and pMOS

threshold voltages of 0.65 V and 0.85 V, respectively. This is the first operational amplifier to make almost exclusive use of body-driven analog primitives, including body-driven simple current mirrors, body-driven simple cascode current mirrors, and body-driven regulated cascode current sources. Furthermore, in terms of power efficiency, open-loop voltage gain, small-signal unity-gain bandwidth, slew rate, input common-mode range, common-mode rejection ratio, and power supply rejection ratio, this body-driven operational amplifier is competitive with other 1-V operational amplifiers that use various other design techniques—thus proving the viability of body driving as a low-voltage analog technique.

1.3 Overview of the Dissertation

This dissertation presents a study in the design of low-voltage analog and mixed-signal circuits using the body-driven circuit technique. Chapter 2 presents a review of scaling trends for CMOS technology, explores how these trends will affect analog circuit design, and then reviews the most promising design techniques for highly scaled CMOS. From this review it is shown that body driving has great potential as a low-voltage analog design technique. Chapter 3 presents a thorough introduction to the operation of body-driven transistors, including technology considerations, small-signal models, frequency performance, SPICE models, and temperature characteristics. In Chapter 4 a literature review describing previous work in body-driven current mirrors, differential pairs, and amplifiers is presented. Chapter 4 serves as both a review of the state of the art in body-driven circuit design, and an introduction to body-driven design techniques. Chapter 5 presents the original contributions of this research, including a detailed development of the adaptive gate bias technique, the design and characterization of two body-driven

operational amplifiers, and a comparison of the newly developed body-driven op-amp to other published low-voltage amplifiers. Chapter 6 presents a general discussion about the application of body-driven techniques in analog and mixed-signal systems. Finally, Chapter 7 concludes this dissertation. The conclusion includes both a summary of the contributions of this research, and a discussion of future directions for body-driven research.

Chapter 2

CMOS Technology Trends and Implications for Analog Circuit Design

2.1 Introduction

In 1965, on the basis of scant evidence, Gordon Moore predicted that the density of integrated circuits would double roughly every year for the next ten years [3]. In 1975, when this prophetic prediction proved true, it was codified as Moore's Law that the density of integrated circuits would continue to increase exponentially for the forseeable future [4], [5]. Quantitatively described by technology scaling or simply "scaling", this irresistible trend has defined the integrated circuit industry from its earliest times until today. While Moore's Law is a well-known quantity to circuit designers, its implications for modern CMOS technology and modern CMOS analog circuit design are perhaps less well known. Therefore at this time it is useful to present a brief review of the present and predicted future trends for CMOS technology, and to discuss the implications of these trends for analog circuit design. From this discussion it will be shown that, due to the significant challenges that highly scaled CMOS technologies pose for analog circuit design, novel design techniques, including body driving, will be required in the future.

Section 2.2 discusses MOSFET scaling trends for CMOS technology, highlighting those factors which have an impact on analog circuit design. In Section 2.3 the impact of scaling on analog circuit design, specifically the impact of reduced power supply voltages and gate leakage current, will be examined and the challenges facing analog circuit

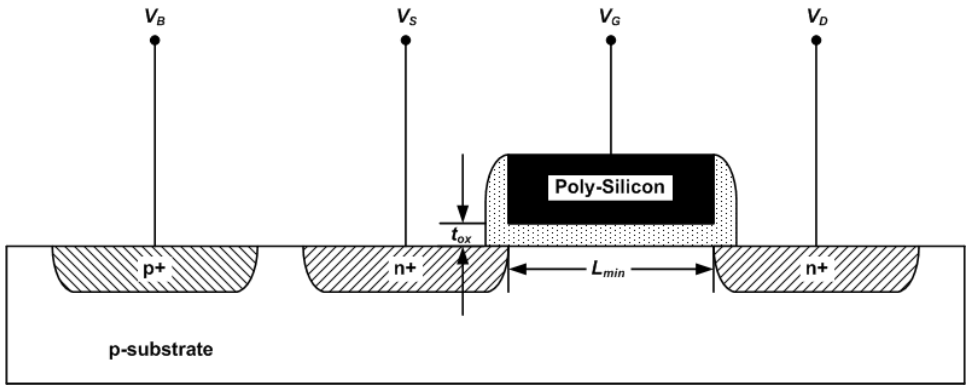

Figure 2.1: Cross section of a n-type bulk-Si MOSFET showing process parameters and device dimensions which are scaled

designers will be highlighted. In Section 2.4 the most promising new analog design techniques, including body-driven MOSFETs, common-mode level shifting, floating-gate MOSFETs, and switched op-amp, will be introduced and compared. From this discussion it will be shown that body driving is an extremely important design technique which has great potential for low-voltage analog applications. Finally, Section 2.5 concludes this chapter.

2.2 Scaling Trends for Digital and Analog CMOS Technologies

2.2.1 Introduction to Technology Scaling

Simply put, technology scaling refers to a reduction in MOSFET dimensions which allows increased packing densities and higher performance in integrated circuits. More than any other factor, it has been the ability to scale CMOS technology in a predictable and consistent manner that has led to the proliferation of CMOS ICs we see today [6]. In this section the fundamental trade-offs associated with technology scaling are reviewed, using the approximation of a long-channel MOSFET. Figure 2.1 presents a simplified dia-

gram of a bulk Si nMOSFET and shows the key device dimensions, gate-oxide thickness t_{ox} and minimum channel length L_{min}, which will be considered in this discussion of scaling. Not shown on the diagram are the important voltages related to MOSFET operation, power supply voltage V_{DD} and threshold voltage V_{TH}.

As the primary goals of scaling are to increase the density and improve the performance of digital integrated circuits, the main lever for achieving these improvements is the gate length. The general approach in scaling is to introduce a new generation roughly every three years, and for each generation to have a minimum gate length that is 30% smaller than the previous generation. If the aspect ratios of the devices within a given circuit are held constant, then a 30% reduction in gate length yields a roughly 50% reduction in gate area, or a doubling of the packing density. To gauge the increase in performance with scaling, a common figure of merit is the intrinsic MOSFET delay τ [7], given by

$$\tau = \frac{C_{tot} V_{DD}}{I_{DSAT}}, \tag{2.1}$$

where C_{tot} is the total gate capacitance of a MOSFET and I_{DSAT} is the maximum saturation current (that is, the saturation current at $V_{GS} = V_{DD}$). Using the MOSFET square-law equation, τ can be calculated as

$$\tau = \frac{C_{ox} W L V_{DD}}{\frac{\mu C_{ox}(W/L)}{2}(V_{DD} - V_{TH})^2} = \frac{2L^2}{\mu} \cdot \frac{V_{DD}}{(V_{DD} - V_{TH})^2}, \tag{2.2}$$

where C_{ox} is the gate oxide capacitance per unit area, μ is the MOSFET mobility, and W

and L are the MOSFET gate width and length, respectively. Equation 2.2 shows that the intrinsic MOSFET delay scales as L^2, assuming that V_{DD} and V_{TH} are constant.

While it is straightforward to improve MOSFET speed by decreasing L, this solution also creates the problem of increasing electric fields within the device. For instance, the maximum transverse (i.e., source–drain) electric field is given by

$$E_{T,\,Max} = \frac{V_{DD}}{L}\,. \tag{2.3}$$

If the electric fields within the device get too large, device lifetime and reliability will be compromised. Likewise, the dynamic power dissipation of a digital circuit is described by

$$P_D \propto f V_{DD}^2, \tag{2.4}$$

where f is the operating frequency of the circuit. To limit both electric field intensity within the device and dynamic power dissipation, it is typically necessary to scale the power supply voltage along with the channel length.

The final two parameters that will be considered are oxide thickness t_{ox} and threshold voltage. As V_{DD} is scaled down, the maximum vertical electrical field (i.e., gate–channel) will be reduced, which limits the transistor drive current. Therefore oxide thickness must be scaled along with power supply and channel length, in order to maintain drive current. Drive current is also dependent on gate-overdrive ($V_{DD} - V_{TH}$), which implies that V_{TH} should scale down with the other parameters. However, threshold voltage sets the

Table 2.1: Negative and positive effects of scaling critical MOSFET parameters

MOSFET Parameter Scaled	**Positive Effect**	**Negative Effect**
V_{DD}	reduces dynamic power dissipation, increases reliability	reduces speed
V_{TH}	increases speed	increases static power dissipation
t_{ox}	increases drive current	decreases reliability
L	reduces area, increases speed	decreases reliability

sub-threshold leakage current I_{SUB} (the drain current at V_{GS} = 0), which is given by [8]

$$I_{SUB} = 2n\mu C_{ox}(W/L)U_T^2 \exp\left(\frac{-V_{TH}}{nU_T}\right), \tag{2.5}$$

where n is the sub-threshold slope factor and U_T is the thermodynamic voltage (approximately 26 mV at room temperature). Sub-threshold current, which is exponentially dependent on threshold voltage and independent of power supply voltage, is the key factor in determining static power dissipation in digital circuits (at least for processes with gate lengths > 65 nm). In order to minimize static power dissipation, threshold voltage is typically not scaled, or scaled only very weakly, from one CMOS process generation to another.

Table 2.1 presents a summary of the negative and positive effects of scaling critical MOSFET parameters. This table considers scaling from a digital circuit perspective.

Each row in the table considers the effect of scaling one parameter, assuming that all other parameters are held constant.

2.2.2 Scaling Trends for Digital CMOS Technologies

The purpose of the previous section was to provide the reader with an understanding of the basic factors affecting technology scaling in digital circuits. In this section the scaling trends most important for circuit design: V_{DD}, V_{TH}, t_{ox}, and L_{min}, are presented. The data presented here span the years 2001–2009, and therefore represent the recent past, present, and predicted future trends for CMOS technology. The data comes from two sources: the 2003 *International Technology Roadmap for Semiconductors* (ITRS), which provided predictions about future trends, and a paper published in the *Proceedings of the IEEE*, which provided information about historical trends [6], [7].

Figure 2.2 presents the scaling trends for CMOS power supply voltage for the years 2001–2009. Looking at this plot, one will immediately notice that there are three different trends shown for power supply voltage. These three curves are labeled high performance (HP), low operating power (LOP), and low standby power (LSP), and they each represent a V_{DD} scaling trend that has been optimized for a distinct, but broad category of digital circuits. Thus, high performance refers to digital circuits whose primary concern is speed and that operate from an effectively unlimited power source; desktop and server computers are the best examples of HP applications. Low operating power refers to systems that still need to operate at high speeds, but also must operate within a limited power budget; laptop computers are a good example of an LOP application. Finally low

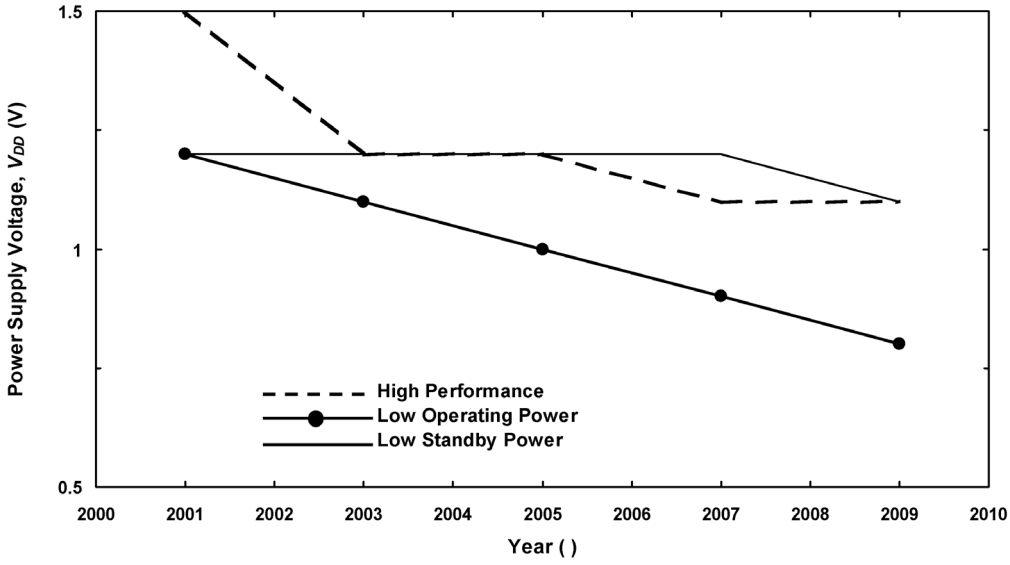

Figure 2.2: Scaling trend for digital CMOS power supply voltage

standby power refers to systems for which minimizing power dissipation, both static and dynamic, is of paramount importance; the digital circuits within a cellular telephone are a good example of an LSP application. Figure 2.3 presents the scaling trend over the same period for MOSFET threshold voltage, and also uses the designations of high performance, low operating power, and low standby power.

The main reason that CMOS technology is forced to offer multiple power supply and threshold voltages within a given technology generation is that V_{DD} and V_{TH} are now so low that it is not possible to meet the performance requirements of the wide range of differing applications with a single choice of operating voltages. As an example, note that in 2005 the V_{DD} for HP and LSP is 1.2 V, while it is only 1 V for LOP. Conversely the V_{TH} is 0.2 V for HP, 0.3 V for LOP, and 0.5 V for the LSP technology option. Thus we can see

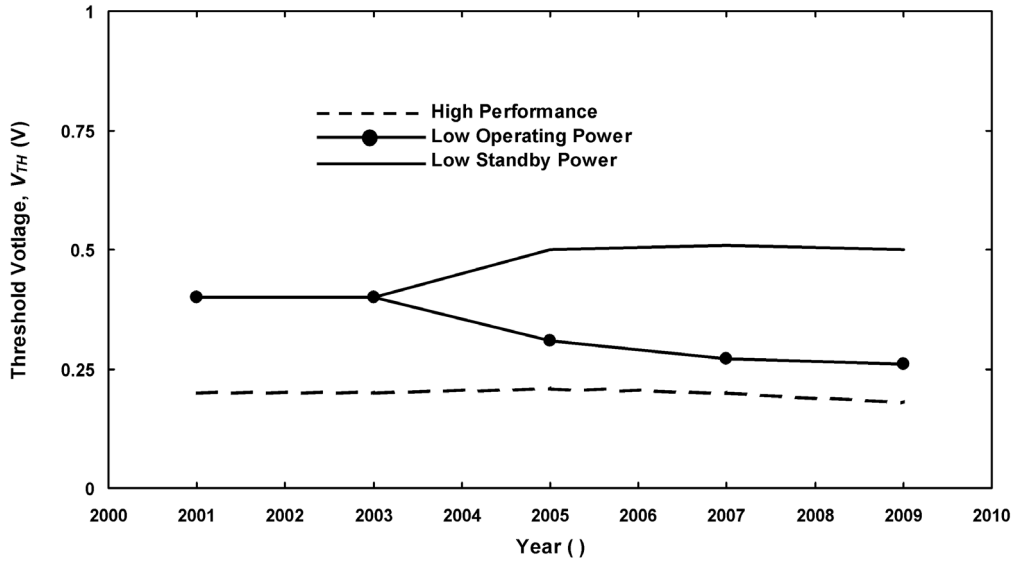

Figure 2.3: Scaling trend for digital CMOS threshold voltage

that the HP CMOS option has the highest V_{DD} and lowest V_{TH} to maximize speed, at the cost of increased power. LSP has a V_{DD} equal to the HP V_{DD}, but also has the highest V_{TH}, which allows it to minimize sub-threshold leakage at the cost of reduced speed. Finally the LOP option has the lowest V_{DD} and a V_{TH} in between the other two, resulting in moderate speed and moderate levels of leakage current. Considering the trends as a whole, V_{DD} is between 1.5 V and 1.2 V in 2001 and scales to values of 1.2 V and 0.8 V in 2009. On the other hand, threshold voltage scales very little because it must generally be chosen for leakage current minimization, which is independent of power supply voltage. From 2005 onwards the available threshold voltages will be close to 0.2 V, 0.26 V, and 0.5 V.

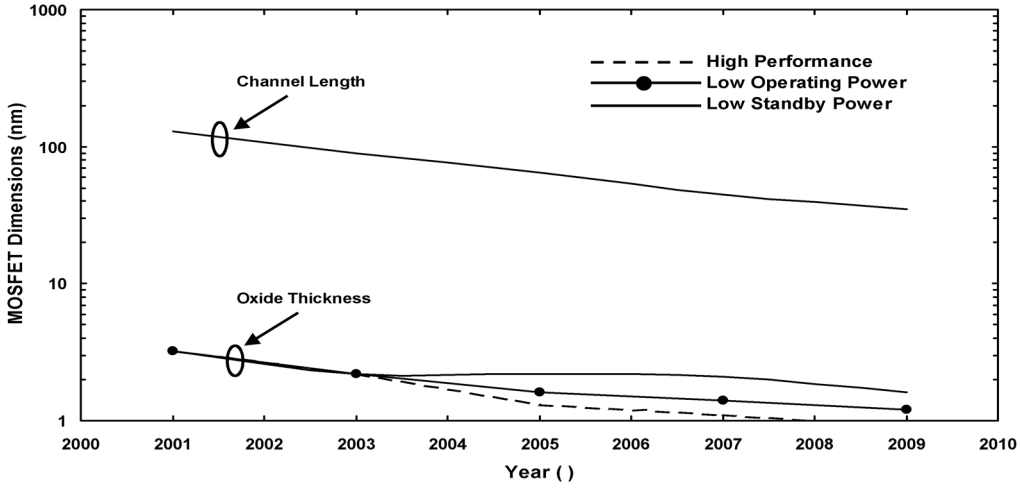

Figure 2.4: Digital CMOS scaling trend for channel length and oxide thickness

Figure 2.4 presents the scaling trends for both CMOS channel length and oxide thickness. The channel length runs from 120 nm in 2001 to only 35 nm in 2009. Oxide thickness starts at just above 3 nm in 2001, and then splits in 2003 to three different trends *as per* the HP, LOP, LSP discussion above. The gate oxide thickness in 2009 will range between 0.9 nm and 1.6 nm.

2.2.3 Scaling Trends for Analog CMOS Technologies

The previous discussions about the trade-offs inherent in technology scaling, and the scaling trends predicted for the future, referred to what can be called digital CMOS technology; that is, a CMOS technology which has been optimized for digital applications. This is an appropriate approach to the problem because CMOS technology is predominantly used for digital applications, and digital applications will always be the prime

mover for technology scaling. However, in recent years analog circuit applications, including high-performance ADCs and RF power amplifiers, have become essential components of mixed-signal systems and are increasingly being recognized as technology drivers in their own right [9]. The problem with including analog applications in the calculus of technology scaling is that the technology needs of digital and analog circuits are often at odds. Specifically, one of the major differences is that very low power supply voltages represent a major hurdle for analog circuits, while low power supply voltage is generally an advantage, or at least not a problem, for digital circuits.

One popular strategy for factoring analog (i.e., higher V_{DD}) considerations into the process flow is to include a thicker oxide option that would allow devices to operate at the higher V_{DD} needed by some analog applications. This thick-oxide option has the added purpose of allowing high-voltage I/O capability for interfacing off-chip with digital circuits that use a higher operating voltage. Figure 2.5 presents the power supply trend that will be required for proper operation of some analog circuits—specifically including higher performance ADCs and RF power amplifiers [9]. The two curves in this plot represent the upper and lower limits for analog power supply voltage, which are 2.5 V and 1.8 V, respectively, for most of the decade. Certainly this is much more manageable than the 0.8 V to 1.2 V range predicted for the digital technology options. However, the power supply data presented in Figure 2.2 and Figure 2.5 should not be considered equally realistic. The trends presented for digital CMOS technology are much more detailed, and since all CMOS technologies will be first optimized for digital applications, they will offer options very close to what was presented in Figures 2.2 and 2.3. On the other hand, the

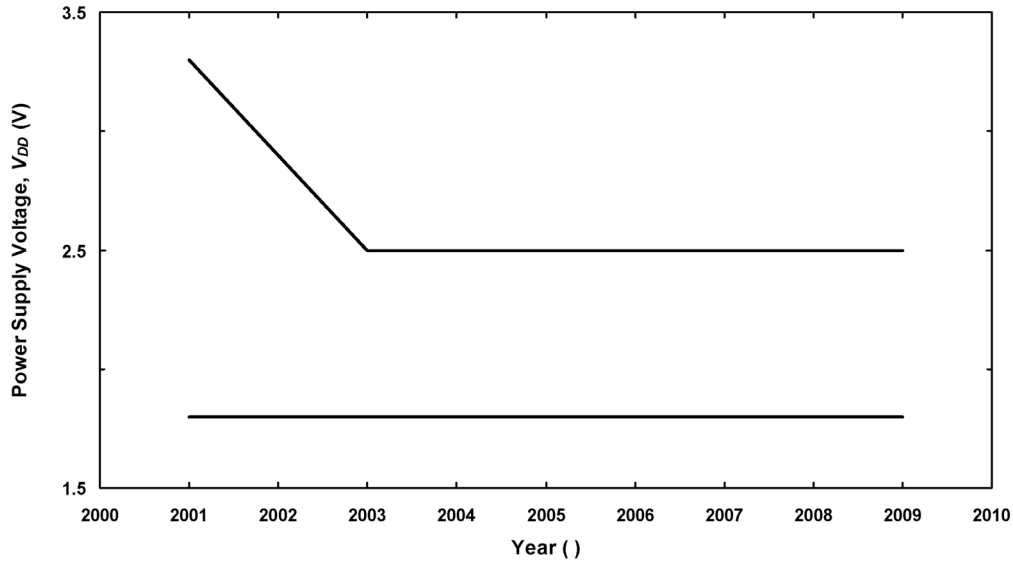

Figure 2.5: Required CMOS scaling trend for highest-performance analog applications

predictions for analog power supply only describe what will be needed for some analog design applications. There is no guarantee that an analog designer will have these power supply options to work with. Frequently, analog circuit designers will have to design within the power supply and threshold voltage constraints dictated by digital CMOS scaling trends. These issues will be described in more detail in the next section. Nonetheless, the fact that analog circuit needs are being factored into the technology roadmap is significant, and must be considered when trying to understand what the complete field of analog circuit design will look like in the future.

2.3 The Low-Voltage Challenge to Analog Circuit Design

In Section 2.2 the scaling trends that can be expected for CMOS technology were presented; in this section the implications of these scaling trends for analog circuit design

will be explored. Since analog circuit design is a broad field with many different applications that have different performance requirements and utilize different circuit topologies, it is not possible to exhaustively consider the effects of technology scaling on every aspect of analog circuit design. Instead, this section considers three of the most important consequences of scaling: how reduced power supply voltage affects power dissipation, how reduced power supply voltage affects circuit functionality, and how gate leakage current affects circuit functionality. In Section 2.3.1 an analysis of the relationship between power supply voltage and power dissipation in analog circuits is presented, and it is shown that for high-performance (i.e., high-speed, high-resolution) applications power dissipation is the limiting factor in determining power supply voltage. In Section 2.3.2 the limitations on analog circuit functionality due to reduced power supply voltage are analyzed by considering the power supply and threshold voltage requirements for several benchmark circuits. In Section 2.3.3 the levels of gate leakage current that will be present in highly scaled technologies, and the effects of gate leakage current on analog circuits, will be studied. Finally, in Section 2.3.4 some predictions about the future state of analog circuit design are made, based on the analysis presented in the previous sections.

2.3.1 Power Supply Voltage and Power Dissipation

Analog circuits can be differentiated from digital circuits by the fact that in analog circuits the precise values of input and output voltages are important. The fundamental limitation to the precision that an analog circuit can achieve is noise, which is present in all electronic systems due to the random thermal motion of electrons. A useful figure of merit for the precision of analog systems is the signal-to-noise ratio (SNR), which is essentially

the ratio of the maximum to minimum signal that an amplifier can resolve, and is quantitatively described by

$$SNR = \frac{P_{SIGNAL}}{P_{NOISE}}, \tag{2.6}$$

where P_{SIGNAL} is the maximum signal power at the output of a circuit, and P_{NOISE} is the noise power at the output of a circuit. In this section the relationship between power supply voltage and power dissipation is studied for a standard analog circuit, under the assumption that the SNR and bandwidth of the circuit are held constant. To proceed with this analysis, one must compute SNR in terms of the critical circuit parameters. Because of its generality, a single-pole operational transconductance amplifier (OTA) is used as the benchmark analog circuit in this study.

Figure 2.6 presents the schematic of a simple analog circuit, consisting of an OTA connected as a unity-gain follower and loaded by a capacitor, that will be used in this study. Assuming a single-tone input, the maximum, mean-square signal power at the output of

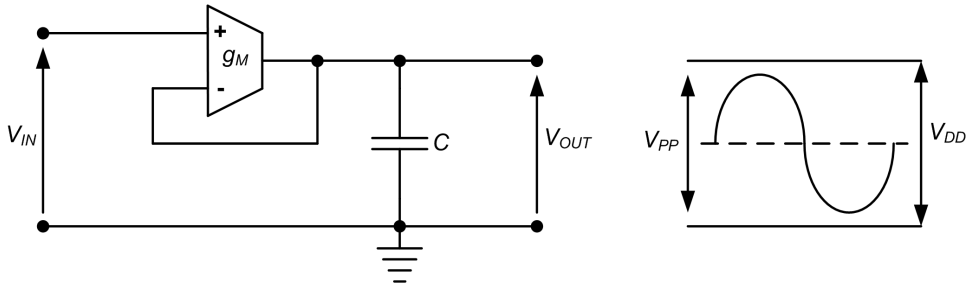

Figure 2.6: Simple analog circuit used to explore the relationship between SNR, power supply voltage, and power dissipation

this circuit can be calculated as

$$P_{SIGNAL} = \frac{V_{PP}^2}{8}. \tag{2.7}$$

The closed-loop frequency response of the circuit can be calculated as

$$H(f) = \frac{1}{1 + j\frac{f}{f_o}}, \tag{2.8}$$

where f_o is the small-signal unity-gain bandwidth given by

$$f_o = \frac{g_M}{2\pi C}, \tag{2.9}$$

and g_M is the transconductance of the OTA's input differential pair. The mean-square noise power at the output of the circuit can be calculated as

$$P_{NOISE} = \overline{e_{ni}^2} \int_0^\infty \frac{df}{1 + \left(\frac{f}{f_o}\right)^2}, \tag{2.10}$$

where $\overline{e_{ni}^2}$ represents the input-referred voltage noise density. Assuming that the input noise is dominated by the thermal noise of the input pair, it can be calculated as

$$\overline{e_{ni}^2} = 8kT\gamma\frac{1}{g_M}, \tag{2.11}$$

where *k* is Boltzmann's constant, *T* is absolute temperature, and γ is a constant roughly equal to 2/3. Finally, the output noise power can be calculated by evaluating the integral

in Equation 2.10

$$P_{NOISE} = \frac{2\gamma kT}{C}, \tag{2.12}$$

and the SNR can be expressed as

$$SNR = \frac{V_{PP}^2 C}{16\gamma kT}. \tag{2.13}$$

To understand how voltage scaling affects the power dissipation of an analog circuit, assume that $V_{PP} \approx V_{DD}$ and that V_{DD} is scaled by a factor $1/\alpha$ $(\alpha > 1)$. In this case the scaled peak-to-peak output swing V_{PPs} will be

$$V_{PPs} \Rightarrow \frac{V_{PP}}{\alpha}. \tag{2.14}$$

To maintain a constant SNR the load capacitance must scale as

$$C_s \Rightarrow \alpha^2 C, \tag{2.15}$$

and to maintain the bandwidth f_o, the g_M must also scale as

$$g_{Ms} \Rightarrow \alpha^2 g_M. \tag{2.16}$$

If we assume that the transconductance efficiency g_M/I_D of the input pair devices in the

transconductor remains constant, the bias current of the OTA must scale as

$$I_{Ts} \Rightarrow \alpha^2 I_T, \tag{2.17}$$

where I_T is the tail current for the OTA. Finally, if we assume that the OTA supply current is in direct proportion to the tail current, we can see how the power dissipation of this analog circuit will scale with power supply voltage, assuming SNR and bandwidth are constant:

$$P_{Ds} = (V_{DD}/\alpha)(\alpha^2 I_T) \Rightarrow \alpha P_D . \tag{2.18}$$

Equation 2.18 shows that the power dissipation of an analog circuit is inversely proportional to power supply voltage, assuming SNR and bandwidth are constant. This is a fundamental result of thermodynamics and is independent of circuit topology and device technology. Furthermore, although a simple OTA was used in this analysis, this basic relationship is true for all analog circuits [8]. The most significant conclusion that can be drawn from this analysis is that for the highest performance analog circuits, such as ADCs with resolution greater than 12 bits and operating speeds greater than 10 MHz, the power dissipation will become prohibitively large if the power supply voltage is scaled to one volt. It is for these applications that an analog power supply voltage in the range of 1.8 to 2.5 V has been defined, as in Figure 2.5.

2.3.2 Power Supply Voltage and Circuit Functionality

The previous section showed that for the highest performance analog circuits, power dissipation and operating speed will be the limiting factors in determining the allowable power supply voltage. However, there are many other analog circuits which perform at low to moderate speeds (e.g., DC to 10 MHz) and have an SNR in the 10- to 12-bit range. For these applications circuit functionality, instead of power dissipation, will often be the limiting factor in determining power supply voltage. Furthermore, since these applications can theoretically run at very low power supply voltages, it will be expected that they operate at the standard digital power supply voltages discussed in Section 2.2.2, and use the digital CMOS threshold voltages also described in that section. In this section the limitations of analog circuit functionality at low supply voltage will be studied by analyzing the power supply voltage required for several benchmark analog circuits.

2.3.2.1 Minimum Analog Power Supply Voltage

Figure 2.7 presents a schematic of a simple analog circuit, which has only two transistors connected in series between V_{DD} and V_{SS} and therefore shows the minimum required power supply voltage for an analog circuit. The minimum V_{DD} required for this circuit is

$$V_{DDmin} = V_{GS} + V_{DSAT} + 100mV, \tag{2.19}$$

where the 100 mV term is included to allow the internal high-impedance node adequate dynamic range to respond to an input signal, and to account for any shifts in threshold voltage over process. If we assume that all of the transistors are operating at the center

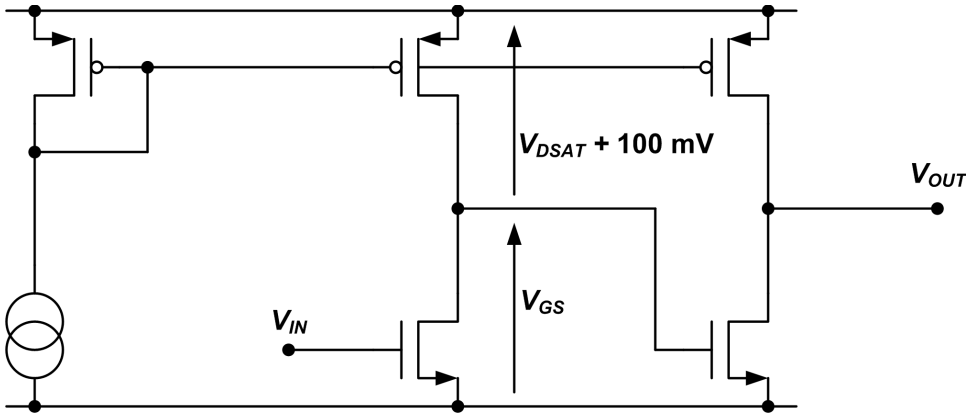

Figure 2.7: Circuit showing the minimum power supply voltage required for an analog circuit

of moderate inversion, then the V_{GS} is equal to V_{TH} + 25 mV and V_{DSAT} is equal to 150 mV, therefore the minimum power supply voltage can be calculated as

$$V_{DDmin} = V_{TH} + 275mV. \tag{2.20}$$

While it is true that a lower minimum power supply voltage would be allowed by operating one or more of the MOSFETs in weak inversion, the purpose of this analysis is simply to study the power supply requirements for analog circuits without reference to a specific application or design constraints. Moderate inversion is often a very wise choice for biasing circuits because it provides good power efficiency and dynamic range, while allowing much higher operating speeds and requiring less area than weak inversion operation [10]. Since it is so widely used, it is a good way to generalize the biasing of an analog circuit. Furthermore, it would be very unsound design practice to assume *a priori* that all of one's circuits must operate in weak inversion.

Table 2.2: V_{DD} and V_{TH} for HP, LOP, and LSP Digital Technologies at the 45-nm node

	V_{DD}	V_{TH}
HP	1.1 V	0.20 V
LOP	0.9 V	0.27 V
LSP	1.2 V	0.51 V

Decreasing V_{DD} →

Increasing V_{TH} ↓

	LSP V_{DD}	HP V_{DD}	LOP V_{DD}
HP V_{TH}	0.725 V	0.625 V	0.425 V
LOP V_{TH}	0.655 V	0.555 V	0.355 V
LSP V_{TH}	0.415 V	0.315 V	0.115 V

Figure 2.8: V_{DD} overhead ($V_{DD} - V_{DDmin}$) for the circuit of Figure 2.7 at the 45-nm node for all possible technology combinations

Table 2.2 presents V_{DD} and V_{TH} voltages which are predicted for the 45-nm node (that is, the year transistors with a minimum gate length of 45 nm will be introduced), which should be in use sometime around 2007. Using these numbers, we can consider how power supply and threshold voltage will limit analog circuit operation. First, note that analog circuit designers are not limited to choosing only one technology option (e.g., choosing LOP V_{DD} and LOP V_{TH}). Instead analog designers can consider a mix of different technology options (e.g., HP V_{DD} and LOP V_{TH}) that provides the best trade-offs for circuit functionality and performance. Figure 2.8 presents the V_{DD} overhead (defined as

$V_{DD} - V_{DDmin}$) for all possible technology combinations at the 45-nm node. In this table the columns represent V_{DD} technology options and the rows represent V_{TH} technology options. Each element in the table describes the V_{DD} overhead for the combination of two technology options; for instance, the value of 0.655 V in the left column, middle row is the V_{DD} overhead for the circuit of Figure 2.7 when the LSP V_{DD} (1.2 V) and the LOP V_{TH} (0.27 V) are used. Also note V_{DD} decreases in moving to the right, and V_{TH} increases moving down. Therefore in moving to the right or moving down, one is choosing technology combinations which result in reduced V_{DD} overhead, and hence more difficult analog circuit designs.

Considering the data presented in Figure 2.8, perhaps the most important result is that V_{DD} overhead is positive for all possible technology combinations. This is an important result because the minimum required V_{DD} described in Equation 2.20 can effectively be considered the minimum required V_{DD} for any analog circuit, independent of the design technique used. Thus, Figure 2.8 indicates that analog circuit design will still be possible in highly scaled digital CMOS technologies.

2.3.2.2 Differential Pair with Current Mirror Load

In the previous section the minimum power supply voltage required by an analog circuit was studied and it was shown that analog circuit design, at least the design of very simple analog circuits, will be possible in highly scaled technologies. In this section a more complex and useful circuit topology is analyzed. Figure 2.9 describes the power supply voltage required for the second benchmark analog circuit—a differential-input, single-

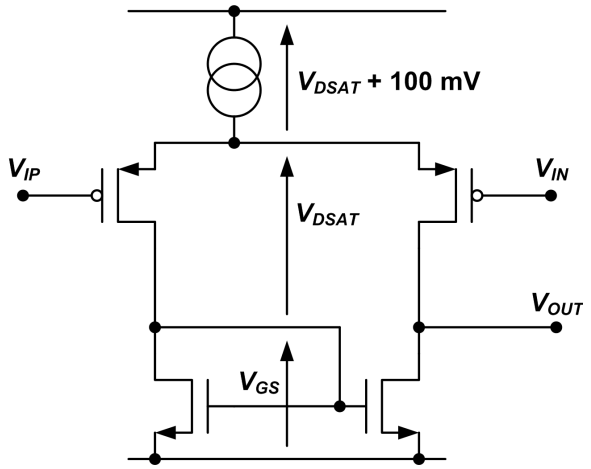

Figure 2.9: Power supply voltage required for a simple differential-input, single-ended output amplifier

ended output amplifier. Again assuming all devices are operating at the center of the moderate inversion region, the minimum required V_{DD} can be calculated for this circuit as

$$V_{DDmin} = V_{GS} + 2V_{DSAT} + 100mV = V_{TH} + 425mV. \quad (2.21)$$

Figure 2.10 presents the V_{DD} overhead for the circuit of Figure 2.9, for all possible technology combinations at the 45-nm node. While the table shows that this circuit can still operate with all technology combinations except for LOP V_{DD} and LSP V_{TH}, it is interesting to note that the V_{DD} overhead in this circuit is also equal to input common-mode range (ICMR). Therefore, even though this circuit can still operate for all but one combination of V_{DD} and V_{TH}, it will have a very limited ICMR in most cases.

Decreasing V_{DD}

Increasing V_{TH}

	LSP V_{DD}	HP V_{DD}	LOP V_{DD}
HP V_{TH}	0.575 V	0.475 V	0.275 V
LOP V_{TH}	0.505 V	0.405 V	0.205 V
LSP V_{TH}	0.265 V	0.165 V	–0.035 V

Figure 2.10: V_{DD} overhead ($V_{DD} - V_{DDmin}$) for the circuit of Figure 2.9 at the 45-nm node for all possible technology combinations

2.3.2.3 Complementary Differential Pair

Figure 2.11 presents the schematic of a complementary differential pair, another important benchmark analog circuit. This is the most common circuit used when designing op-amps with rail-to-rail ICMR, and is also a very difficult circuit to operate at low voltages because there are two threshold voltages in series between V_{DD} and V_{SS}. The voltage sources in this circuit represent the low-input impedance that the differential pairs would be driving in a folded-cascode topology, which is a common circuit architecture used in low-voltage circuit designs. Since the voltage sources are equal to V_{DSAT}, it is assumed that the low-voltage cascodes are biased at their minimum operating voltage, which is the typical condition for low-voltage circuit design. The minimum power supply voltage required by this circuit is

$$V_{DDmin} = 2V_{GS} + 2V_{DSAT} + 100mV = 2V_{TH} + 450mV. \quad (2.22)$$

Figure 2.12 lists the V_{DD} overhead for the circuit presented in Figure 2.11, for all combi-

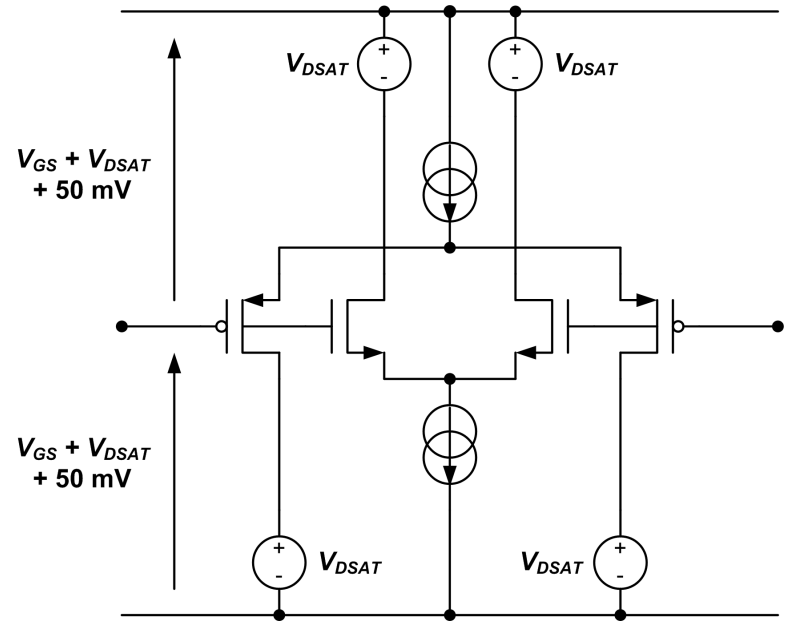

Figure 2.11: Power supply voltage required for a complementary differential pair

Decreasing V_{DD}

Increasing V_{TH}

	HP V_{DD}	**LSP V_{DD}**	**LOP V_{DD}**
HP V_{TH}	0.350 V	0.150 V	−0.060 V
LOP V_{TH}	0.210 V	0.110 V	−0.090 V
LSP V_{TH}	−0.270 V	−0.370 V	−0.570 V

Figure 2.12: V_{DD} overhead ($V_{DD} - V_{DDmin}$) for the circuit of Figure 2.11 at the 45-nm node for all possible technology combinations

nations of technology options at the 45-nm node. Clearly the complementary differential pair is the most limited, in terms of allowable technology options, of all the circuits studied in this section. However, Figure 2.12 shows that there are still several technology options for which the complementary differential pair will still be fully functional at the 45-nm node.

2.3.3 Gate Leakage Current

Up until this point in the discussion of the low-voltage challenge to analog circuit design, issues relating to analog circuits operating at reduced power supply voltages have been considered. It has been shown that power supply voltages greater than 1.8 V are required for only the highest performance analog applications; whereas for lower-speed applications power supply voltages of approximately 1 V should be sufficient, especially if one has access to devices with a threshold voltage less than 0.3 V (i.e., HP and LOP technology options). Indeed, from the discussion presented thus far, it might seem that circuit design in highly scaled technologies will not be such a great challenge after all, or at least not a greater challenge than designing in a technology with V_{DD} > 1.8 V and a 0.5-V threshold. However, we will now consider the effects of gate leakage current in highly scaled technologies, which in many cases will force the circuit designer to utilize the highest threshold voltage option available—thus greatly complicating the circuit design process. The purpose of this section is to qualitatively study MOSFET direct tunneling gate current. The aspects of gate current that will be considered are the relationship between oxide thickness and gate current, the magnitudes of gate current one can expect in highly scaled CMOS technologies, and the magnitude of gate current that will be present under standard analog bias conditions.

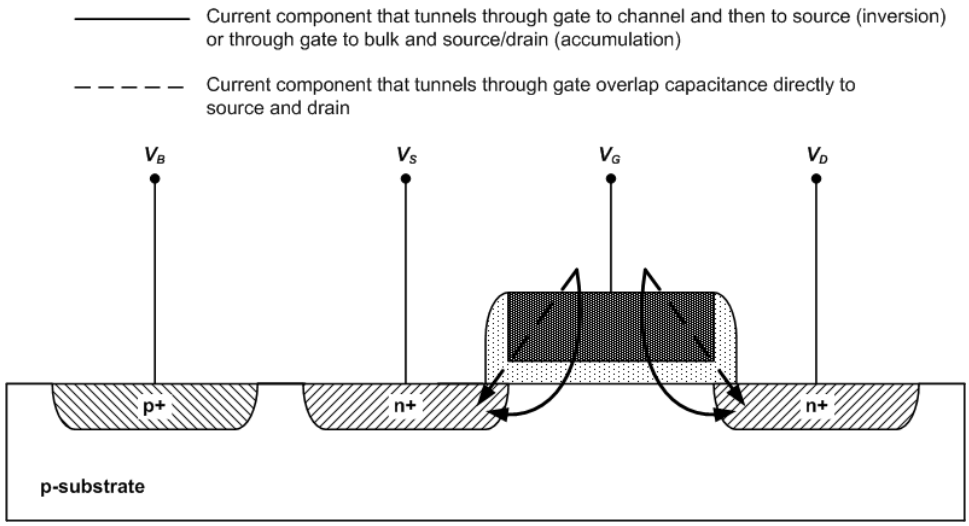

Figure 2.13: Cross section of a bulk CMOS MOSFET showing primary tunneling current components [12]

When a positive voltage is applied to the gate of an nMOSFET, quantum mechanics predicts that there is a non-zero probability that an electron from the channel will “tunnel” to the gate [11]. This effect is called direct tunneling, and each electron that tunnels across the oxide can (theoretically, at least) be measured at the gate as a current impulse. Direct tunneling can be differentiated from Fowler-Nordheim tunneling by the fact that direct tunneling occurs at low electric fields and is not damaging to the oxide [11]. Historically, direct tunneling has not been a problem in CMOS technologies because the oxides are thick enough that the probability of tunneling is very low and no appreciable current results. However, as gate oxides scale below 3 nm, the probability of an electron (or a hole) tunneling through the oxide is greatly increased, with the net result that “leaky” or “resistive” gates will be an important design concern for analog and digital circuits in the near future. Figure 2.13 presents a cross-section of a bulk nMOSFET showing the key

tunneling current components. Specifically, the tunneling current consists of components that tunnel from the gate through the overlap capacitances and directly to the source and drain, and components that tunnel through the oxide capacitance to the body and then are collected either by the source, drain, or body depending on whether the MOSFET is inverted or accumulated.

In the BSIM4 SPICE model, the gate–channel current (which could flow either to the source or drain), is shown to depend on oxide thickness in the following manner [12].

$$I_{GC} \propto \frac{e^{-t_{ox}}}{t_{ox}^{3}}. \tag{2.23}$$

Equation 2.23 shows that gate current is highly sensitive to oxide thickness, but does not show the magnitude of gate current that will be present. The complete BSIM4 equation for gate current contains several empirical parameters used for curve fitting and therefore does not provide much intuition about the levels of gate current one should expect. Therefore to study this problem further a generic BSIM4 model, which is distributed by the BSIM group for the purpose of benchmarking the model, was obtained and evaluated using the Eldo circuit simulator. Figure 2.14 presents the simulated gate current magnitude for a 10/0.5 nMOSFET with the V_{GS} swept from 0 to 1 volts, and the V_{DS} stepped from 0.1 V to 0.8 V in 0.1-V steps. The oxide thickness is equal to 1.8 nm, which approximately corresponds to a device at the 65-nm node. From this plot one can observe several important facts about gate current and MOSFET biasing. First, gate current is present in all MOSFET operating regions (weak, moderate, and strong inversion). In deep weak inversion and accumulation the gate current is highly sensitive to drain

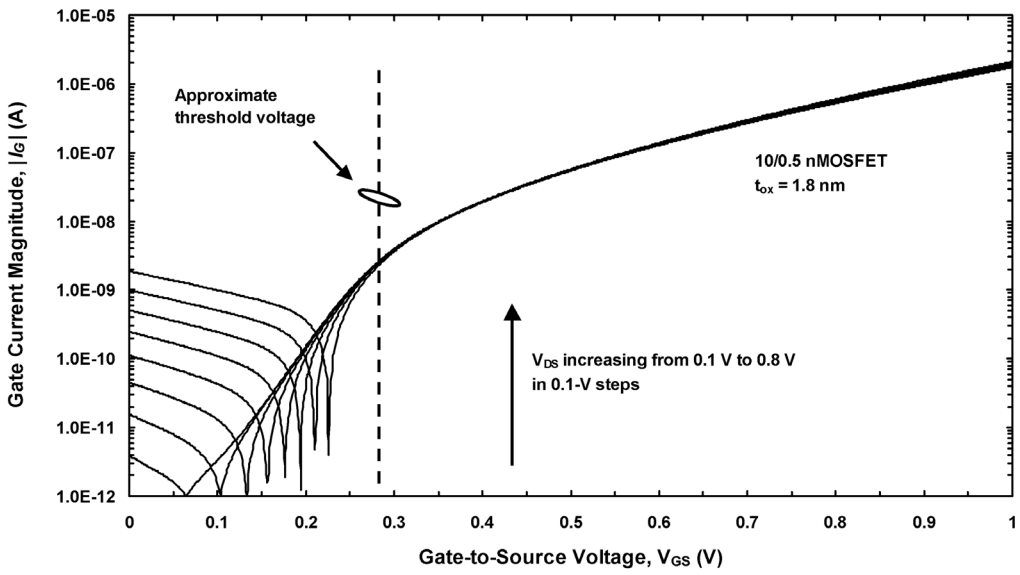

Figure 2.14: Simulated gate current versus V_{GS} and V_{DS} for a 10/0.5 nMOSFET with t_{ox} = 1.8 nm

voltage, because there is a significant drain–gate current component in this region. As the gate–source voltage is increased, with a constant drain–source voltage, the net current flowing into the gate $(I_G = -I_{GD} + I_{GS})$ will increase because I_{GD} decreases while I_{GS} increases. At some value of V_{GS}, which is dependent on the V_{DS}, the gate current will be approximately zero at the point where the drain–gate and gate–source currents cancel. As the gate–source voltage is increased beyond this point, the gate current is entirely dominated by the gate–source component and the gate current becomes relatively insensitive to drain voltage.

As one might imagine, gate tunneling current will become a critical factor in determining the off-state current in digital circuits in highly scaled technologies. Therefore, in keeping with the HP, LOP, and LSP designations previously discussed, future CMOS technolo-

Table 2.3: Gate oxide thickness for HP, LOP, and LSP digital Technologies at the 45-nm node

	t_{ox}	V_{TH}/t_{ox}
HP	1.1 nm	0.18 V/nm
LOP	1.4 nm	0.19 V/nm
LSP	2.1 nm	0.24 V/nm

gies must also provide several different oxide thicknesses to meet the static power dissipation requirements for each technology option. Table 2.3 presents the oxide thicknesses predicted for the HP, LOP, and LSP technology options at the 45-nm node, which is the same technology node discussed in the previous section. As one would expect, the oxide is thinnest for the HP option and thickest for the LSP option. It is also interesting to note that the ratio of threshold voltage to oxide thickness is nearly constant for all technology options at this node, which is a clear indication that the multiple threshold voltages are achieved through the different oxide thicknesses.

To better understand how the gate current will scale with oxide thickness, the parameters TOXE and TOXP (electrical and physical oxide thickness) in the BSIM4 model were set to 1.1, 1.4, and 2.1 nm and the gate current was again simulated. Of course this will not give a precise measure of the gate current for each option because the empirical fitting parameters should be chosen for each case based on measurement. However, the fitting parameters will only shift the gate current by a small factor, probably less than two. On the other hand, the different oxide thicknesses that were simulated shift the gate

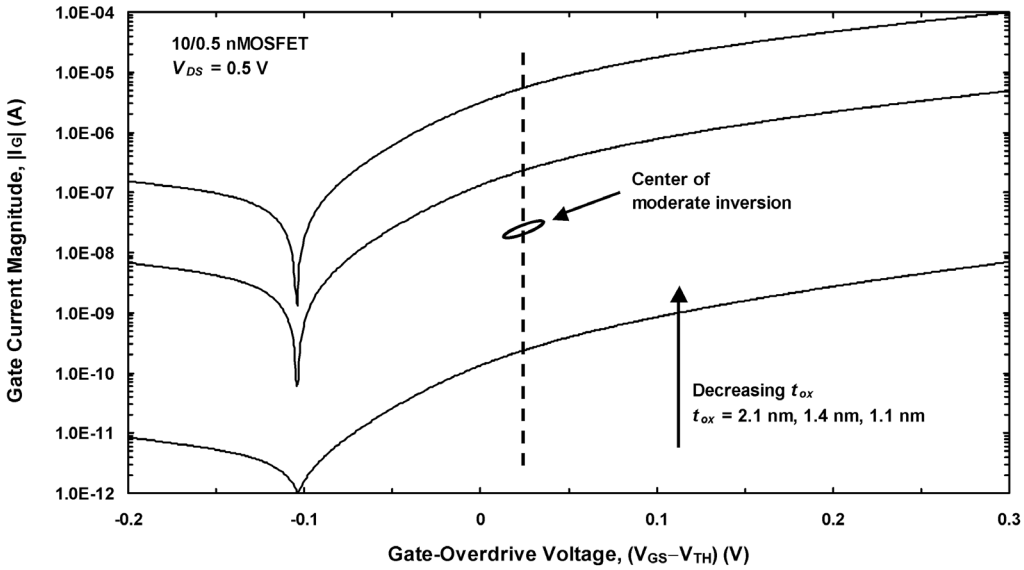

Figure 2.15: Simulated gate current versus gate-overdrive voltage ($V_{GS}–V_{TH}$) and t_{ox} for a 10/0.5 nMOSFET with V_{DS} = 0.5 V

leakage current by several orders of magnitude. Therefore the following simulation results can be taken as indicative of the gate current levels one can expect for analog circuits at the 45-nm node. Figure 2.15 presents the simulated gate current magnitude versus gate-overdrive voltage ($V_{GS}–V_{TH}$) for a 10/0.5 nMOSFET with a V_{DS} of 0.5 V and oxide thicknesses of 1.1, 1.4, and 2.1 nm. In this plot the gate-overdrive voltage is swept from –200 mV to +300 mV, which represents roughly the maximum range of V_{GS} values that can be used for low-voltage circuit design. As a reference point, a line marking the center of moderate inversion ($V_{GS}–V_{TH}$ = 25 mV) is shown, which is also the bias condition considered in the previous section. For this bias condition one can see that the gate current is 5.6 μA for the HP option, 0.24 μA for the LOP option, and 0.24 nA for the LSP option. Thus within a single technology generation, at a standard analog bias condition

($V_{GS} - V_{TH}$ = 25 mV, V_{DS} = 0.5 V) and a standard analog device size (10/0.5), one can expect gate current to vary by four orders of magnitude, depending on the technology option chosen.

Finally, it is important to consider how gate leakage current will affect analog circuit design. Several important issues to consider are

- gate leakage current will induce mismatch in current mirrors;
- gate leakage current will significantly inhibit the performance of switched-capacitor circuits;
- a “resistive gate” will cause accuracy problems for many CMOS circuits that require high source and load impedances; and
- due the discrete and random nature of the current flow, tunneling current gives rise to a shot noise component that will be extremely important in circuits that are driven from a high impedance.

There will of course be other problems caused by gate current, many of which will not be discovered until circuits are fabricated in highly scaled technologies and tested. Nevertheless, it is clear that gate tunneling current is an important problem that must be avoided as much as possible. From the standpoint of gate leakage current we can see that the LSP option is the best choice for analog circuit design in highly scaled technologies.

2.3.4 The Future of Analog Circuit Design

The previous sections presented an overview of the challenges facing analog circuit designers in highly scaled technologies, specifically including the relationship between power supply voltage and power dissipation, power supply voltage and circuit functionality, and gate leakage current. Regarding the nature of analog circuit design in the future, several important conclusions can be drawn from this study. Analog circuit designs in the future will probably be divided between those that require V_{DD} > 1.8 V because of dynamic range limitations, and those that can operate at voltages close to 1 V. For those applications that require V_{DD} > 1.8 V, design techniques will probably not have to change much. For instance, high-performance switched-capacitor circuits operating at 1.8 V can still use standard CMOS switches, folded cascode op-amps, and gate-driven differential pairs. However, it should also be noted that just because 1.8-V V_{DD} is available for some analog applications, it will by no means be available for all applications in highly scaled technologies. Though an effort will be made to include a 1.8-V analog V_{DD} on chip with 1-V digital circuits, the ITRS cautions [9]: “The analog power supply reduction trend may lag [the] digital backward compatibility trend for I/O such that a common thick gate oxide solution is not possible.” Therefore it must be assumed that analog circuits that do not intrinsically require a V_{DD} > 1.8 V will be expected to operate within the available digital power supply constraints. It is for these 1-V capable applications to which this research is primarily addressed.

Next we must consider what technology options should be used for designing the circuits that will operate close to 1-V V_{DD}. From the discussion of power supply voltage,

threshold voltage, and circuit functionality, it is clear that the minimum threshold voltage is the best choice. On the other hand, from the discussion of gate leakage current, it is clear that the maximum threshold voltage option (since it corresponds to the thickest oxide) is the best choice. The key question then is “Which issue is more important—circuit functionality limited by threshold voltage or circuit functionality limited by gate leakage current?” In many cases there will be an application specific answer to this question. For instance, there will be applications where gate leakage current is not a problem, so the HP threshold option will be chosen. Other times, gate leakage current will be an overriding concern, and the LSP threshold must be chosen. However, it seems obvious that gate leakage current will be a detriment (though in varying degrees) to any analog circuit. Therefore, what is needed are new analog design techniques that allow full circuit functionality using the highest threshold option in a technology, but which can still operate at the lowest V_{DD} used by the technology. The application of the body-driven circuit technique to this low-voltage challenge is the focus of this research.

2.4 Low-Voltage Analog Design Techniques

In the previous section it was shown that important changes are forthcoming in CMOS technology which, to a greater or lesser degree, will require novel analog design techniques. To meet these requirements analog circuit designers have been working to develop such new design techniques, and many important results have been reported in the literature over the last five years. Generally speaking, all of the new design techniques are trying to solve the same problem: How do we design analog circuits when the threshold voltages becomes a significant fraction of the total power supply voltage

$\left(\frac{|V_{TH}|}{V_{DD}} \geq 0.5\right)$. Of course, if all of the new design techniques are trying to solve the same problem, it immediately begs the question of which one is best. In this section a review of the most important new design techniques will be presented, and an answer to this question will be put forth.

Though the following classifications have not, to the best of the author's knowledge, been described in the literature, it is helpful to divide the new design techniques into two broad categories: circuit-level design techniques and transistor-level design techniques. As the names imply, circuit-level design techniques are those that enable low-voltage circuit design by modifying a design at the circuit or "block" level, while transistor-level design techniques are those that enable low-voltage circuit design at the transistor or device level. Furthermore, circuit-level design techniques typically show the following traits:

- application specific,
- use standard design techniques at the transistor level (e.g. current mirrors, gate-driven differential pairs), but novel design techniques at the circuit (or primitive) level, and
- low-voltage functionality typically enabled through novel method of coupling signals into/out of circuit.

Whereas transistor-level design techniques typically exhibit these complementary traits:

- application independent,
- use novel design techniques at the transistor level (e.g. body driving), but standard design techniques and interfaces at the circuit (and primitive) level, and
- low-voltage functionality enabled by removing threshold voltage from signal path.

In this section two examples of circuit-level design techniques, common-mode level shifting and switched op-amp, and two examples of transistor-level design techniques, floating-gate MOSFETs and body-driven MOSFETs, will be introduced and compared.

2.4.1 Circuit-Level Design Techniques

2.4.1.1 Common-Mode Level Shifting

Common-mode level shifting is a term that refers to a broad class of circuits that use passive elements to couple a signal into a circuit in such a way that wide voltage dynamic range is achieved. Common-mode level shifting is used in both continuous-time systems, where resistors are used for level-shifting, and discrete-time systems, where capacitors are used for level shifting. In this discussion only continuous-time level-shifting with resistors will be considered. Figure 2.16 presents a schematic of one implementation of common-mode level shifting [13]. In this example an op-amp is biased at a fixed common-mode voltage that is approximately one V_{DSAT} above V_{SS}. Next a fixed current source is used to level shift the output to V_{MID}, assuming the input is also at V_{MID}. This configuration allows the input and output voltage of this (closed-loop) amplifier to swing nearly rail-to-rail, and so enables wide dynamic range signal processing—even though

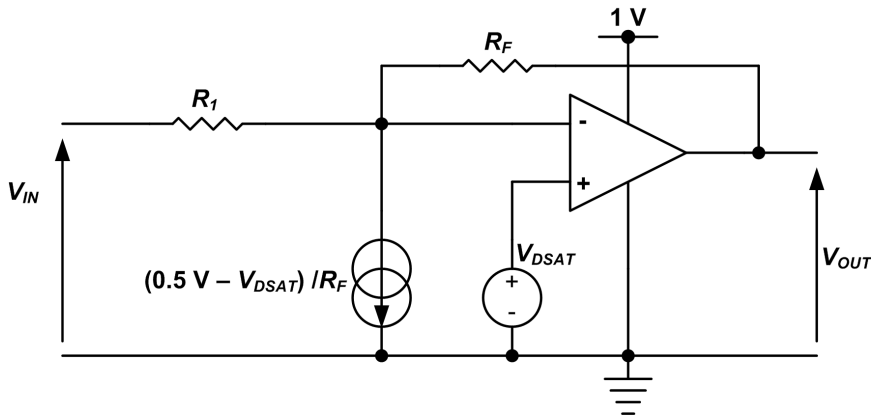

Figure 2.16: Simplified schematic of an op-amp circuit with common-mode level shifting at the input

the ICMR of the op-amp may be very limited (e.g., see Figure 2.10). Of course, this form of common-mode level shifting is only viable for systems that can drive a resistive load, and so its use is relatively limited.

Figure 2.17 presents a more elegant form of common-mode level shifting that is more appropriate for monolithic circuit designs [14]. In Section 2.3.2.3 it was shown that the required power supply voltage for a complementary differential pair was equal to approximately $2V_{TH}$ + 450 mV. If the total power supply voltage is less than this value, then there will be a “dead zone” in the middle of the ICMR where neither the nMOS or pMOS input pairs are turned on [15]. The common-mode level shifting solution to this problem is to separate the gates of the pMOS and nMOS transistors by an adaptively biased resistive level shifter. In Figure 2.17 this is achieved by a set of four resistors and four voltage dependent current sources, which are sensitive to the input common-mode voltage; the graph in Figure 2.17 shows how the bias currents vary with common-mode voltage. Spe-

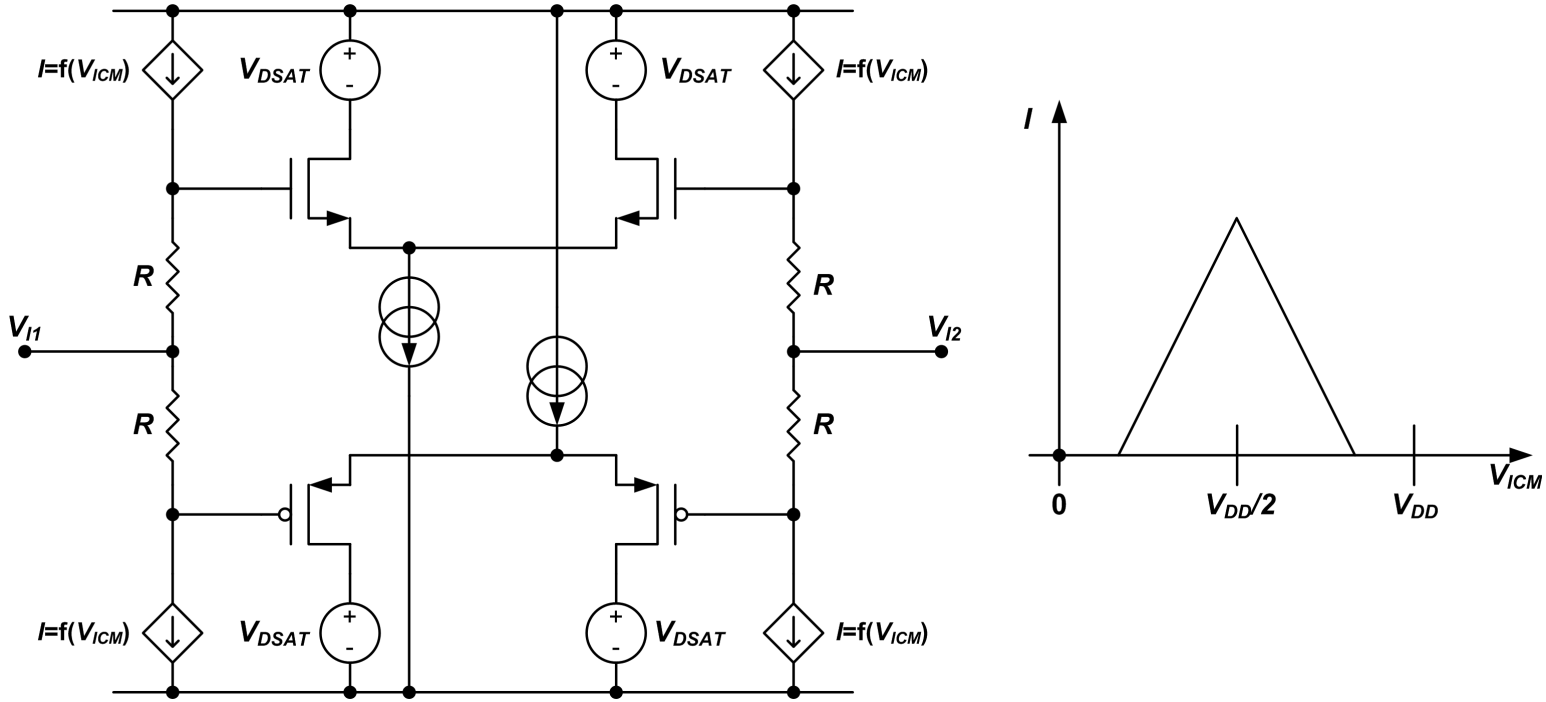

Figure 2.17: Common-mode level shifting for low-voltage complementary differential pairs

cifically, when V_{ICM} is approximately equal to V_{MID}, the bias current is at a maximum and the nMOS and pMOS input pairs are both active and tracking the input signal. If the common-mode voltage is increased or decreased, the bias current decreases such that at some point the input is directly driving one of the input pairs.

2.4.1.2 Switched Op-Amp

While common-mode level shifting is a useful low-voltage design technique for continuous-time, wide voltage dynamic range systems, switched op-amp design addresses the challenge of implementing switched-capacitor circuits in low-voltage systems. The fundamental problem with implementing low-voltage switched capacitor circuits is the “dead-zone” exhibited by CMOS switches, which are used to implement series switches in switched capacitor circuits [16]. Figure 2.18 presents a plot of the on-conductance of a CMOS switch versus input voltage that clearly displays the problem. In this plot the power supply voltage is 1 V, the threshold for both devices is 0.5 V, and the aspect ratio for both devices is 5/0.5. Note that while in future CMOS technologies there will be multiple threshold voltages, with nominal values of 0.2, 0.3, and 0.5 V, for most switched capacitor applications it will be necessary to use the 0.5 V option to minimize leakage current—thus this is a realistic simulation. As one can see in Figure 2.18, the problem with the low-voltage CMOS switch is that both MOSFETs are effectively turned off when V_{IN} is approximately equal to V_{MID}. Of course, the MOSFETs do not completely turn off in this case; however, the on conductance does decrease by more than two orders of magnitude as compared to its values at V_{IN} = 0 and V_{IN} = V_{DD}, which is a prohibitively

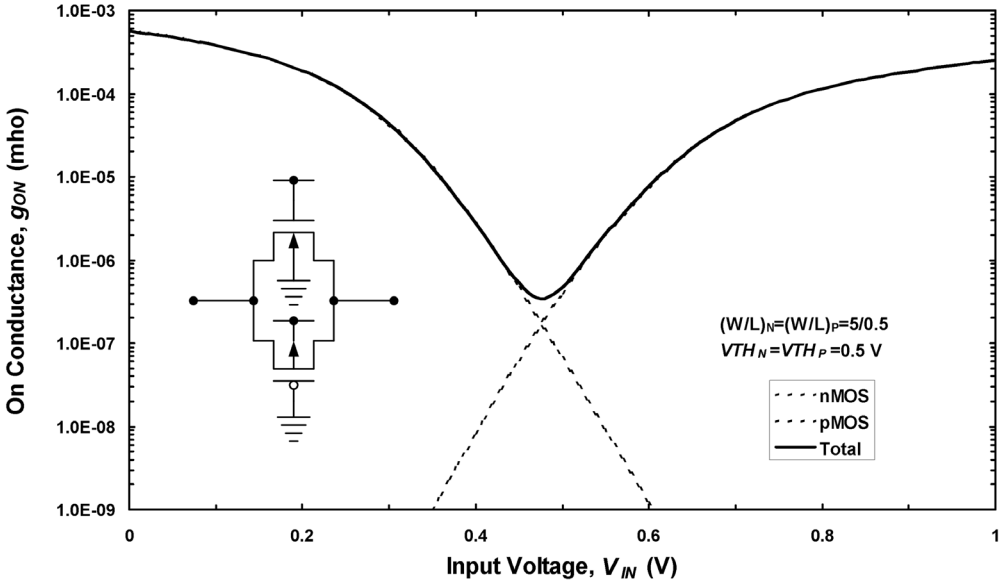

Figure 2.18: On conductance of a CMOS switch as a function of input voltage, V_{DD} = 1 V

large variation that would result in a significant degradation of settling time and a probable loss of circuit functionality.

One promising technique being considered to solve this problem is known as the switched op-amp design technique [16]. Switched op-amp is based on the observation that at low voltages it is always possible to implement shunt switches, the challenge lies in implementing series switches. To address this problem the switched-opamp technique replaces series switches with op-amps that are turned on and off. Figure 2.19 presents an example of a simple switched op-amp. In this case, when the digital signal V_{CLOCK} is high, the op-amp functions normally, but when V_{CLOCK} is low, the output voltage of the op-amp is floating. Figure 2.20 presents an example of a standard switched capacitor

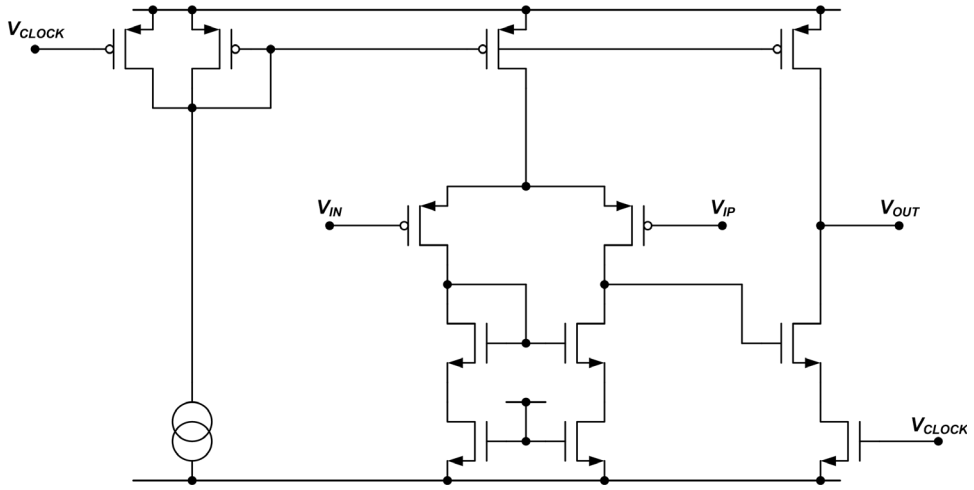

Figure 2.19: An example of a switched op-amp

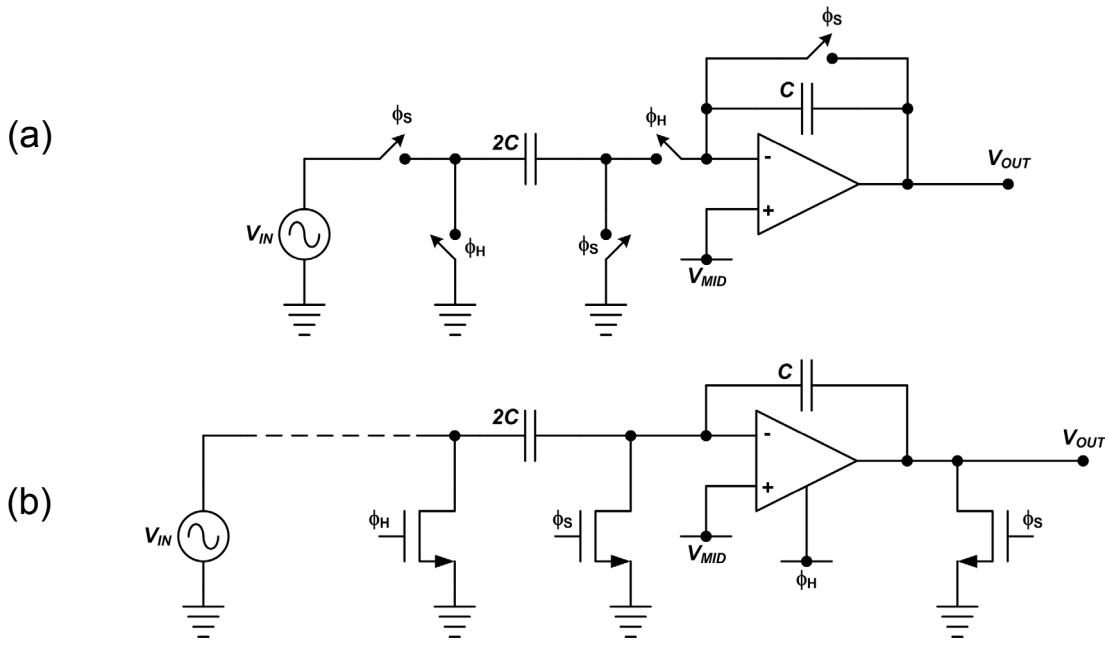

Figure 2.20: Example of (a) a standard switched-capacitor multiply-by-two stage and (b) a switched-opamp multiply-by-two stage with no series switches

multiply by two stage and a functionally equivalent switched op-amp multiply by two stage. Notice that the main difference between the two circuits is that in the sample phase of the switched-opamp circuit, the feedback capacitor is reset by turning off the op-amp and grounding (through nMOS switches) both sides of the feedback capacitor. It should also be noted that one important challenge in switched op-amp circuits is how to couple the input signal into the circuit. This issue has not been directly addressed in Figure 2.20, instead a dashed line is shown between the input voltage source and the switched-opamp circuit. In practice there are several different ways of achieving the input signal coupling, one example would be to use a resistor nominally equal to the on-resistance of the CMOS switches in place of the dashed line. This would allow the input signal to be sampled when ϕ_H is low, but would isolate the input signal from the capacitor when ϕ_H is high. Of course, it should be noted that this problem only applies to the very first block in the signal chain. After the first switched op-amp circuit, it can be assumed that all circuits in the signal path are switched op-amp, and there is no need for a serial element to couple the input signal into other circuits in the chain.

2.4.2 Transistor-Level Design Techniques

2.4.2.1 Floating-Gate MOSFETs

The first transistor level design technique that will be presented is floating-gate MOSFET design. Figure 2.21 presents a schematic representation and a schematic symbol of a dual-input floating-gate MOSFET, which is a useful device for analog circuit design [17]. The basic idea of this circuit is to capacitively couple two signals into the gate of a single MOSFET; the first signal is static and is used to reduce the effective threshold volt-

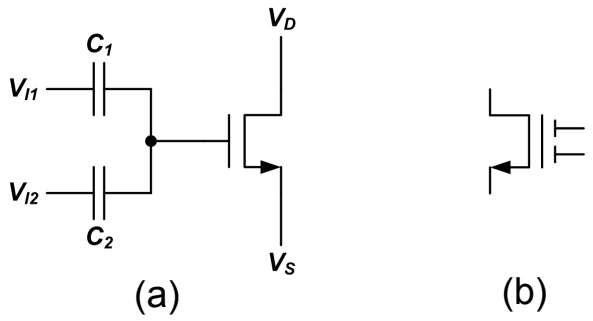

Figure 2.21: Floating gate MOSFET: (a) Schematic representation and (b) schematic symbol [17]

age of the MOSFET as seen at the second input terminal, which is the input used for processing dynamic signals. It is standard in floating-gate design for the capacitors C_1 and C_2 to be an order of magnitude larger than the MOSFET gate capacitance (which is an important drawback, as it results in poor area efficiency), in this case the effective threshold at the input V_{I2} is given by [17]

$$V_{TH(I2)} \approx V_{TH} + \frac{C_2}{C_1}(V_{TH} - V_{I1}), \tag{2.24}$$

where V_{TH} is the threshold voltage of the MOSFET. Equation 2.24 shows that it is possible, with bias voltages less than V_{DD}, to make the effective MOSFET threshold voltage very small or even negative. This ability to cancel the MOSFET threshold voltage has enabled a wide array of analog circuits and circuit primitives to be implemented at very low voltages [18]. Figure 2.22 presents schematics of a floating-gate current mirror and a floating-gate differential pair, circuit primitives that have been used to construct op-amps that operate with power supply voltages close to or equal to 1 V, with a standard digital

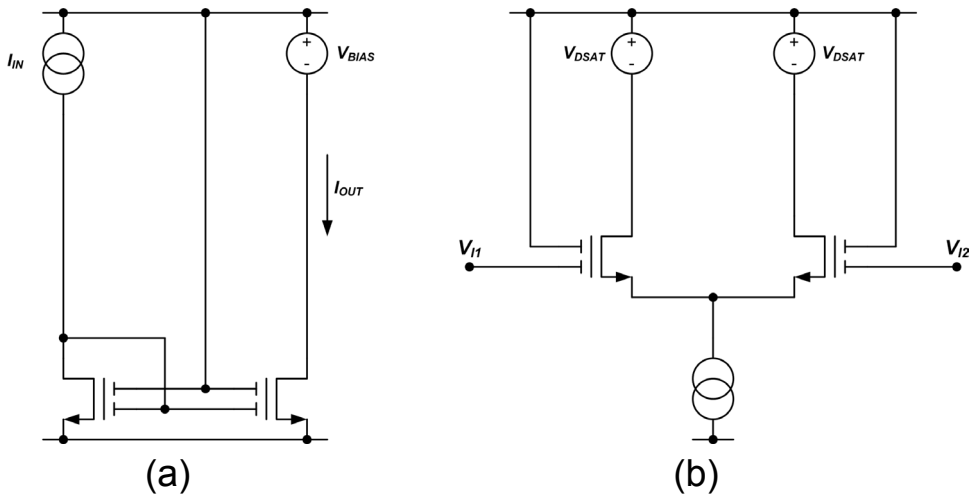

Figure 2.22: Schematics of (a) a floating-gate simple current mirror and (b) a floating-gate differential pair [17]

CMOS technology that has $V_{TH} \geq 0.5V$ [17]. It is interesting to note that by removing the threshold voltage from the signal path, the floating-gate technique effectively enables the use of standard circuit- and primitive-level design techniques within a high-V_{TH} technology option.

2.4.2.2 Body-Driven MOSFETs

The final low-voltage design technique that is considered here, which is also the primary focus of this dissertation research, is the body-driven design technique [19]. Like floating-gate design, the goal of body-driven design is to turn on the MOSFET with a static gate bias, and then to input the dynamic signal at a terminal which has a nearly zero threshold voltage. Unlike gate driving, a body-driven MOSFET requires no external capacitors for coupling the signal into the MOSFET. Figure 2.23 presents a schematic of a single body-driven MOSFET. In body driving the gate is typically biased at a static voltage, which is

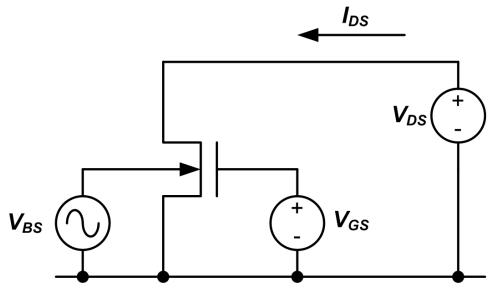

Figure 2.23: Schematic of a body-driven MOSFET

equal to or greater than the threshold voltage. This gate bias creates an inversion layer beneath the gate; at the same time a depletion region is formed between the inversion layer and the neutral body region. By varying the body voltage, one can vary the width of this depletion region, in turn modulating the MOSFET drain current. Thus the MOSFET body acts like an auxiliary gate, albeit a junction gate, and the body-driven MOSFET is similar to a junction field-effect transistor (JFET). The transconductance of the MOSFET body is typically 1/3 of the gate transconductance, which is important to consider when designing body-driven circuits. Figure 2.24 presents schematics of a body-driven simple current mirror and a body-driven differential pair. One will immediately notice that there are many similarities between the body-driven and floating-gate circuit primitives. Specifically, in both design techniques the MOSFET gate is biased at a static voltage to “cancel” the threshold voltage, and the dynamic signal is coupled to the MOSFET channel through an auxiliary input. Also, both design techniques allow the use of standard analog primitives by removing the threshold voltage from the dynamic signal path.

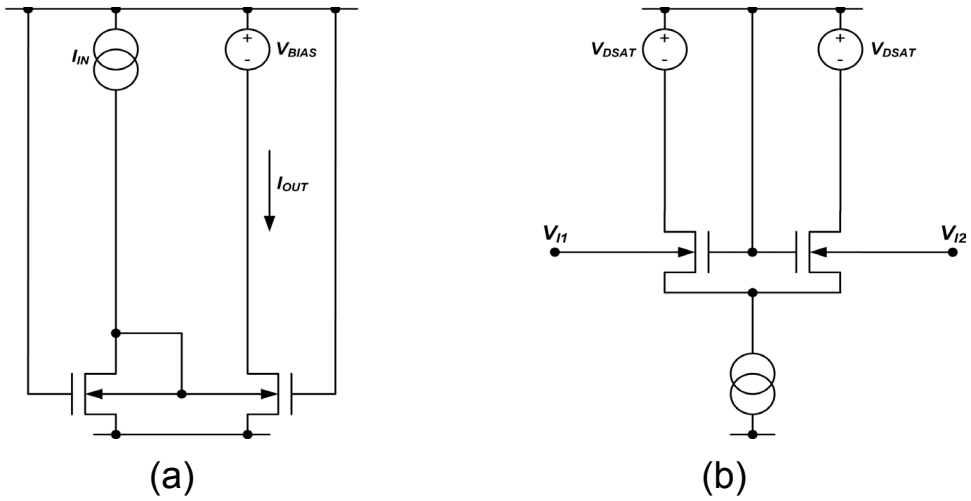

Figure 2.24: Schematics of (a) a body-driven simple current mirror and (b) a body-driven differential pair [19]

2.4.3 Comparison of the Low-Voltage Design Techniques

In this section the concepts of circuit-level and transistor-level design techniques have been introduced, and two examples of each design technique have been presented. It is now possible to consider the relative merits and demerits of each design technique. First, the clear distinction between circuit- and transistor-level design techniques should be reiterated. Perhaps the most important difference is that circuit-level design techniques address specific problems, while transistor-level design techniques address the general problem of removing the threshold voltage from the signal path. The difference between these two categories has not been noted in the literature, and so may have led to some conclusion about which design techniques are better. The specific problem with not categorizing the techniques is that a designer may think that he must choose one over the other (e.g., common-mode level shifting or body driving). However, it is the opinion of this author that this is the wrong way to look at the problem. Instead, it seems that circuit-level and transistor-level design techniques should enjoy a complementary relationship,

instead of a competitive one. Thus, common-mode level shifting looks at the specific problem of wide dynamic range differential pairs, but it in no way considers how to achieve low-voltage current mirrors, high-performance regulated cascode current sources, or low-voltage bias cells. The same argument applies to switched op-amp design. Switched op-amp is a very useful design technique, but at the same time it is very limited, as it does not address how one designs high-gain, high-performance operational amplifiers at low-voltages. Therefore it seems that it is not useful to compare circuit-level and transistor-level design techniques in terms of their utility for low-voltage circuit design, both are useful and important in their own way, and both should have an important place in highly scaled CMOS analog circuit design.

On the other hand, since both of the transistor-level design techniques purport to do the same thing—that is, remove the threshold voltage from the dynamic signal path—it is appropriate to compare these two design techniques. Without getting into too much detail, it is clear that one of the major drawbacks of floating-gate design is that there is an increase in circuit area of 10X as compared to gate driving. Conversely, body driving has a power efficiency that is 1/3 that of a gate-driven MOSFET. Furthermore, for a body-driven MOSFET to achieve the same transconductance as a gate-driven MOSFET, its bias current and aspect ratio must increase by a factor of 3. Thus a body-driven MOSFET has 1/3 the power efficiency and area efficiency of a gate-driven MOSFET. However, when compared to a floating-gate MOSFET, body-driving has 1/3 the power efficiency but 3X the area efficiency. On balance, it is not apparent which is better. With these considerations alone, there will typically be an application-dependent solution to the problem. However, this neglects the fundamental problem with implementing floating-

gate MOSFETs in highly scaled, standard digital CMOS technologies; namely, the presence of any gate leakage current in the MOS structure means that floating-gate design is not possible. Indeed, one important tutorial paper on floating-gate MOSFETs states that floating-gate design is predicated on “the long term retention characteristics of the charge injected into the floating-gate of an MOS transistor [17] …” Looking at Figure 2.22, it is clear that gate leakage current, even the low levels present in the LSP option described in Figure 2.15, make floating-gate design impossible in highly scaled technologies. Therefore, by default, body-driven circuit design becomes the most important transistor-level design technique for analog circuit design in highly scaled technologies.

2.5 Conclusion

This chapter has presented a very thorough discussion about the future of analog circuit design, and the place of body-driven circuits within that future. In Section 2.2 it was shown that within the current decade MOSFET scaling will force power supply voltage and threshold voltage to their minimum allowable levels (approximately 1-V for V_{DD} and 0.2 V–0.5 V for V_{TH}). Additionally, a V_{DD} in the range 1.8 V–2.5 V will be required for the highest performance analog circuits, regardless of the technology generation. In Section 2.3 an analysis of the problems scaling poses for analog circuit design was presented, and it was shown that for a large class of moderate-speed/moderate- to high-precision analog circuits, it will be necessary to use the highest threshold voltage (~0.5 V) available in a given technology generation. Finally, Section 2.4 described several recent design techniques, and made a distinction between those design techniques that operate at the transistor level, and those that operate at the circuit level. It was further shown that body driving is the most viable transistor-level design technique for highly scaled

technologies, and it should have a complementary relationship with the other circuit-level design techniques.

The most important conclusions that can be drawn from this chapter are

- CMOS technology scaling has forced V_{DD} so low that for many analog applications, standard design techniques will no longer be suitable.
- Body driving is the best transistor-level design technique and merits further attention as a low-voltage design technique for highly scaled technologies.

Chapter 3

Introduction to Body Driving

3.1 Introduction

Chapter 3 presents a thorough introduction to body driving by describing the characteristics of body-driven MOSFETs. In Section 3.2 technology choices for body driving, including standard bulk CMOS, twin-well bulk CMOS, and partially depleted SOI, are reviewed. Section 3.3 presents the bias characteristics of a body-driven MOSFET, including a plot that shows body driving is viable in the weak, moderate, and strong inversion regions. Section 3.4 presents a detailed description of the DC and AC small-signal models for body-driven MOSFETs. A comparison of the BSIM3V3 and EKV2.6 models for body-driven applications is presented in Section 3.5, and temperature characteristics of body-driven MOSFETs are explored in Section 3.6. Finally, Section 3.7 concludes this chapter.

3.2 Technology Choices for Body Driving

When first used as a low-voltage design technique, body driving was implemented on a standard digital CMOS technology [20]. At the time, it was possible to body drive only nMOS or only pMOS devices within a given technology (e.g., one could body drive pMOS devices within an n-well CMOS technology), as it is only possible to body drive a MOSFET if it has an isolated body. Historically, the lack of complementary body-driven MOSFETs in bulk CMOS has been an important drawback to the use of body-driven circuits. In fact, this limitation alone has motivated work on body driving in partially depleted silicon-on-insulator (PD-SOI) CMOS, which allows isolated body connections for both

polarities of MOSFETs [21]. However, an important trend in highly scaled CMOS technologies is the deep n-well option, also called triple-well [22], but which will be referred to in this dissertation as twin-well CMOS [23]. Twin-well CMOS is a technology option that allows the formation of a junction isolated p-well within an n-well technology (or vice-versa), and thus enables complementary body driving in a digital bulk CMOS technology. In this section a detailed description of each of these technology options will be presented, along with a justification for choosing PD-SOI technology for this research.

3.2.1 Standard Bulk CMOS

Figure 3.1 presents the layout and cross section of a 10/0.5 body-driven pMOSFET in a 0.5-μm n-well bulk CMOS process. As one can see, this layout structure is identical to that of a standard gate-driven MOSFET. Note that since the body is now a signal input, it is important to use a large amount of contacts to reduce body resistance (since body resistance contributes to noise and degrades the frequency response). From the cross section, it is obvious that one drawback of body driving in bulk CMOS is the n-well–p-substrate junction capacitance, which will limit frequency response in many applications.

3.2.2 Twin-Well Bulk CMOS

Figure 3.2 presents the layout and cross section of an isolated 10/0.5 nMOSFET and a 10/0.5 pMOSFET fabricated on a twin-well digital CMOS technology [23]. As seen in part (b) of Figure 3.2, the “second well” or the isolated p-well is implemented by using a deep n-well that allows isolation of the local p-well from the global p-substrate. Twin-well is a relatively new option in CMOS technology that provides isolation of noise-sensitive

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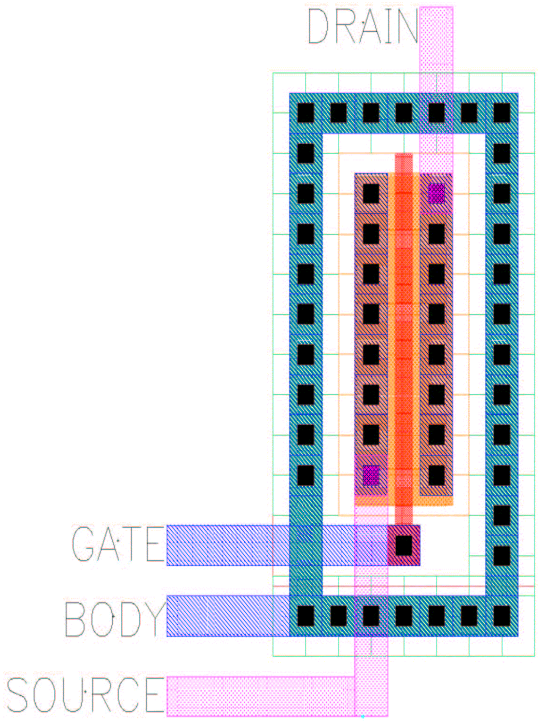

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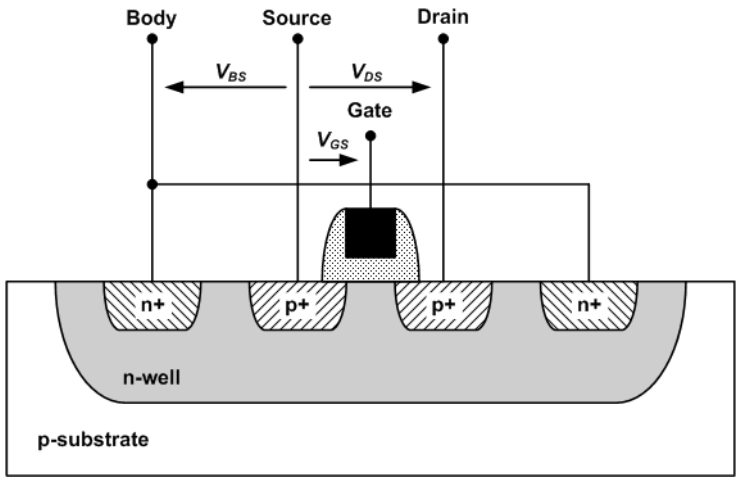
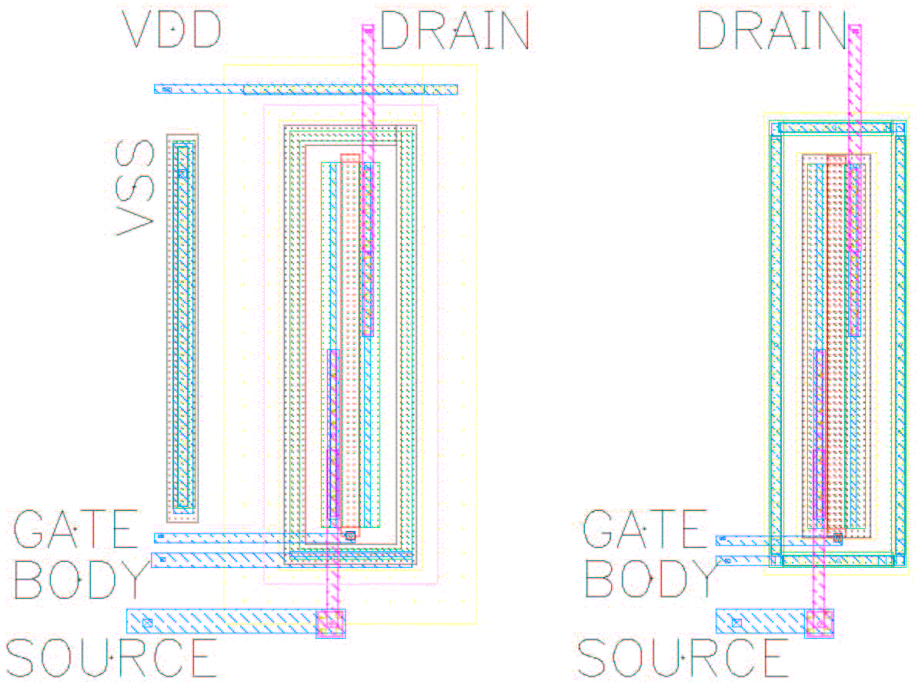


Figure 3.1: A 10/0.5 pMOS body-driven MOSFET on a 0.5-μm n-well bulk CMOS process: (a) layout and (b) cross section

(a)



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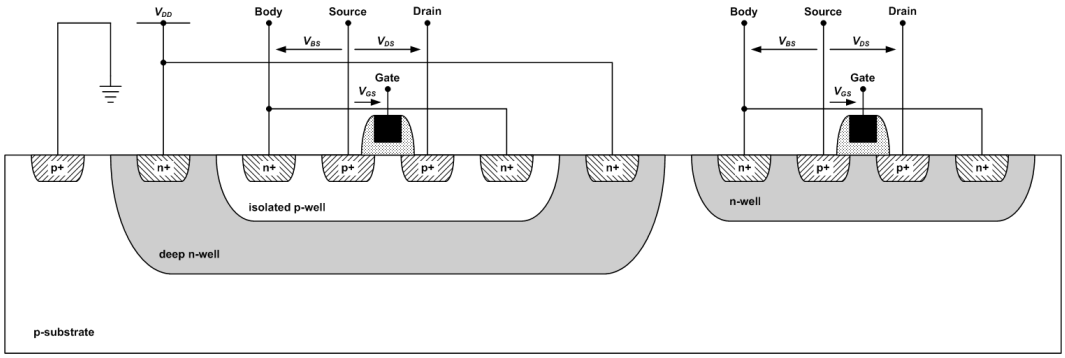


Figure 3.2: 10/0.5 nMOS and 10/0.5 pMOS body-driven MOSFETs on a 0.12-μm n-well (twin-well) bulk CMOS process: (a) layout and (b) cross section

nMOS transistors (e.g., analog and RF) from digital nMOS transistors that collectively discharge significant current to the substrate and thus generate “substrate noise” [24]. The availability of the twin-well option is a clear indication of the increasing importance of mixed-signal circuits in the technology roadmap. Further assuming the importance of mixed-signal will only increase in highly scaled technologies as ever increasing integration densities facilitate more complex systems-on-a-chip, it is clear that we can count on the availability of the twin-well option for the forseeable future. With regard to the parisitics in triple-well CMOS, it seems that they are comparable to the parasitics in standard CMOS. The parasitic capacitance in the body-driven pMOSFET is still dominated by the n-well–p-substrate capacitance. It can be assumed that the deep n-well structure used in the body-driven nMOSFET is held at an AC ground, so that the parasitic capacitance is dominated by the p-well–n-well junction capacitance.

3.2.3 Partially Depleted Silicon-on-Insulator

Before discussing PD-SOI body-driven MOSFETs in detail, it is useful to provide a brief description of PD-SOI MOSFET technology. Figure 3.3 is a diagram that describes the main steps in the Smart-Cut® process, which is the most popular methodology for fabricating SOI wafers and ICs [25]. As shown in Figure 3.3 (a), the starting point for this process is a silicon wafer with an oxide layer grown on top. From this, H^+ ions are implanted into the wafer, which forms micro-cavities in the silicon substrate. Next, the starting wafer (wafer A) is turned upside down and bonded to another silicon wafer (wafer B), which is called the handling wafer and which may or may not have a top oxide layer. After the two wafers are bonded, wafer A is broken along the line where the micro-cavities were

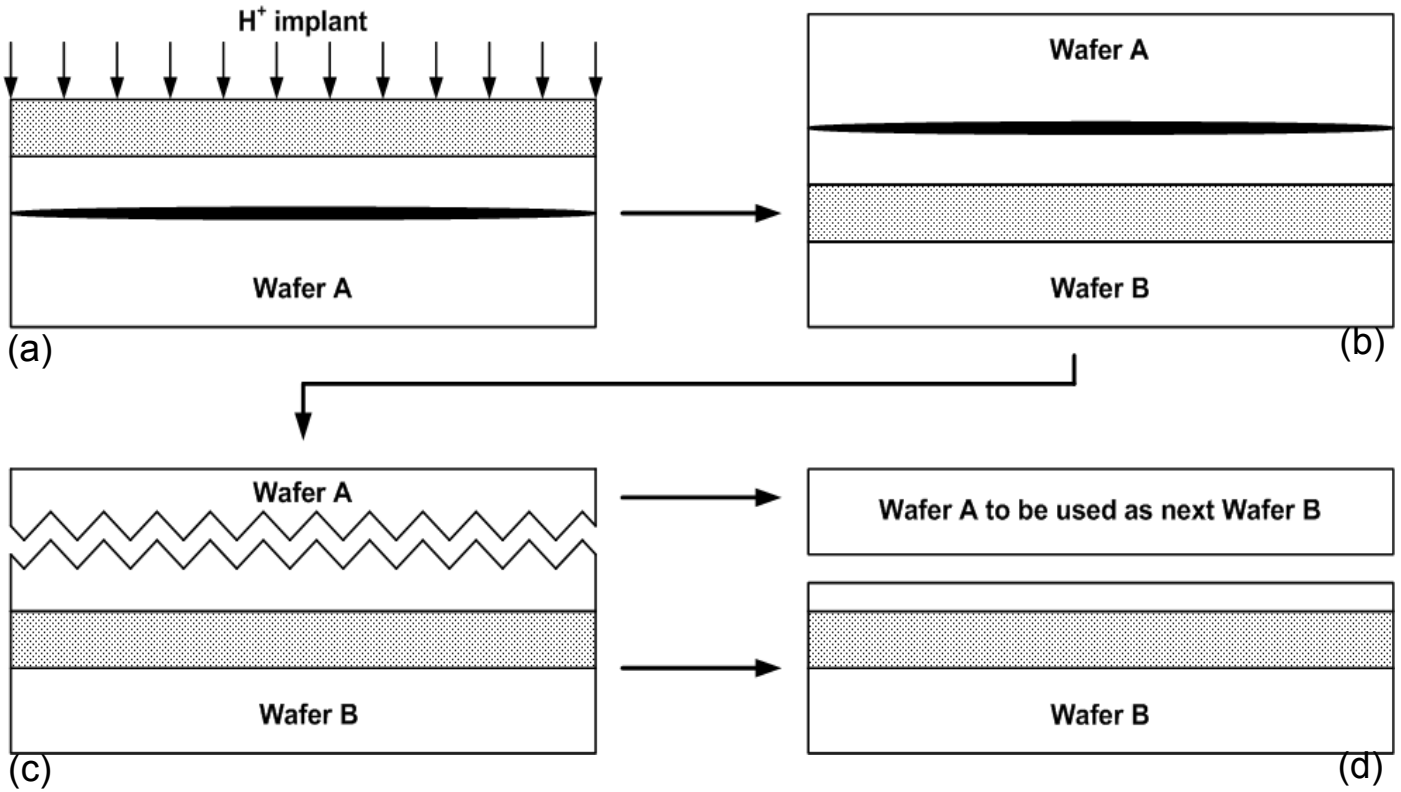


Figure 3.3: Steps in the Smart-Cut® process: (a) hydrogen implant, (b) wafer bonding, (c) wafer splitting, (d) polishing, and wafer A becomes future wafer B [25]

formed, and then the two resulting wafers are polished. The final results are a new handling wafer and an SOI wafer. The SOI wafer has a bottom silicon substrate which is used only for handling, and then a much thinner silicon substrate where transistors are formed. In between these two silicon layers is an oxide layer known as the buried oxide (BOX), which is typically 50 times thicker than the gate oxide. Using this SOI wafer, nMOS and pMOS transistors can be fabricated in the silicon substrate using standard bulk silicon processing techniques. The most important characteristics of SOI are that each transistor (or a group of transistors with a common body connection) is fabricated in their own local well and that this well is isolated on all sides by field oxide, on the top by field oxide, and on the bottom by the BOX.

Figure 3.4 presents the layout and cross section of a 10/0.5 nMOSFET and 10/0.5 pMOSFET fabricated on a 0.35-μm PD-SOI CMOS process. In this process an H-gate type layout structure must be used to allow for an explicit connection to the transistor body. Note also that an important characteristic of all SOI processes is that the source/drain implants go all the way down to the BOX. Generally speaking, the frequency response of body driving should be much better in PD-SOI than in bulk CMOS. The key difference between the two is that the body–substrate capacitance (i.e., body to handling wafer) is only present directly below the transistor gate, and since the dielectric in this case is an oxide layer 50X thicker than the gate oxide, this parasitic is practically negligible. The only junction capacitance present in this structure is the drain/source–body sidewall junction capacitance, which is an important parasitic, but is much less than the parasitics present in bulk CMOS. In terms of frequency response, the main draw-

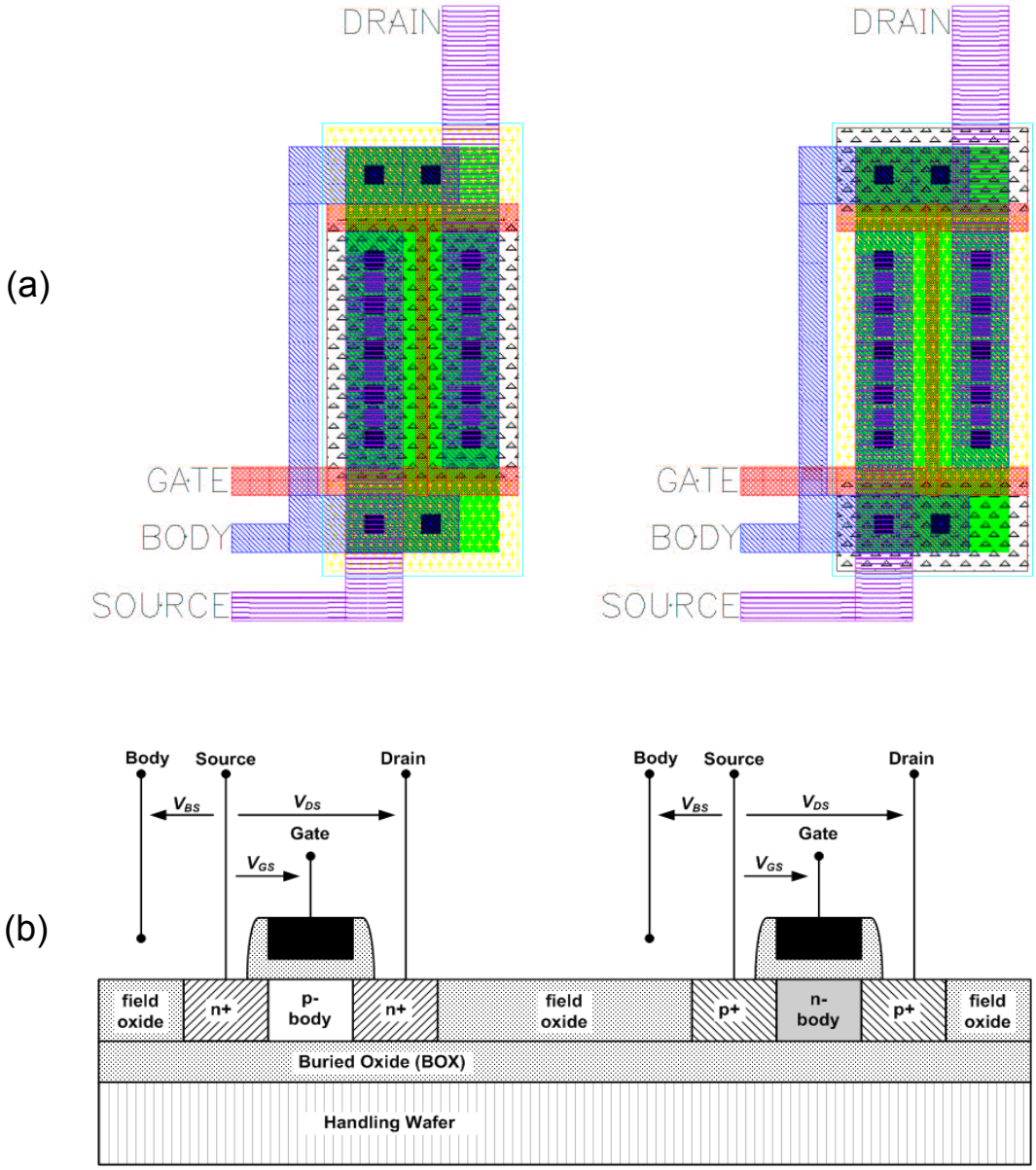


Figure 3.4: 10/0.5 nMOS and 10/0.5 pMOS body-driven MOSFETs on a 0.35-μm PD-SOI CMOS process: (a) layout and (b) cross section (Note that the body contact are at each end of the channel, but cannot be shown in the cross section.)

back of SOI as compared to bulk is that body resistance is much higher in SOI, since the body is only present directly underneath gate, as opposed to bulk CMOS where the body is the entire well. However, by keeping the gate width per finger small and using body contacts liberally, it is possible to minimize this effect.

3.2.4 Semiconductor Technology Chosen for This Work

Though complementary body driving is possible in both bulk CMOS (at the 0.18-μm node and below) and PD-SOI, it was decided in this work to use a 3.3-V/0.35-μm PD-SOI technology. This PD-SOI technology was chosen mainly because of its availability and low cost (our group regularly submits ICs for fabrication in this process), but also because PD-SOI technologies have significantly reduced junction capacitances when compared to bulk CMOS, which allows for higher frequency operation and/or reduced power dissipation. That being said, the body-driven design techniques developed in this work deal mainly with DC biasing considerations, and are directly applicable to both bulk and PD-SOI CMOS technologies.

3.3 DC Biasing Considerations

Figure 3.5, which presents the cross section of a MOSFET fabricated on a PD-SOI CMOS process and biased in strong inversion saturation, is a good starting point for studying body-driven analog circuit design. (Note also that in this figure the p-well body contact has been explicitly shown to facilitate the discussion of body driving.) To utilize the body terminal as a signal input, the gate must first be biased to create an inversion channel between the source and drain. As shown in Figure 3.5, there will also be a

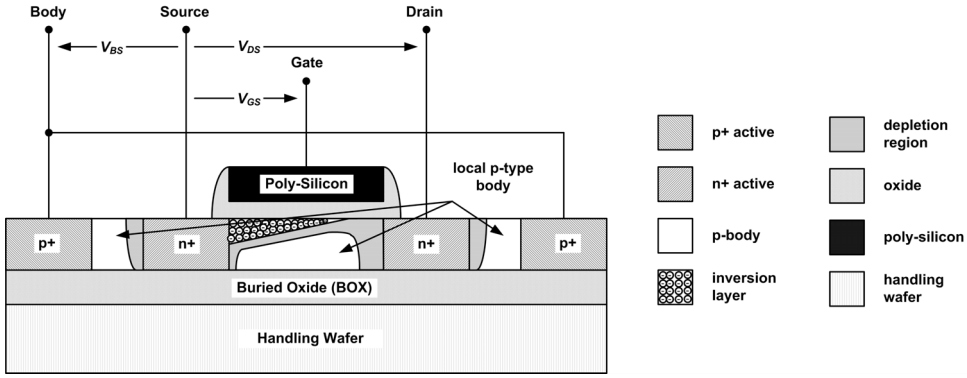


Figure 3.5: Cross section of a PD-SOI MOSFET biased in strong inversion, saturation [1]

depletion region in between the neutral body region and the inversion layer. By varying the body voltage one can vary the width of the depletion region, in turn varying the drain current. It is interesting to note that when biased in strong inversion, the operation of the body-driven MOSFET is very similar to that of a JFET. Conversely, in moderate and especially weak inversion, there is not a complete inversion layer formed under the gate, and the JFET analogy is not as applicable. However, one can still vary the MOSFET threshold voltage as a function of body bias in weak and moderate inversion, and body driving is just as effective in these operating regions [11].

Figure 3.6 presents the measured drain current versus body–source voltage (I_D–V_{BS}) with V_{GS} swept from 0.4 V to 1.0 V in 0.2-V steps, for an (8/0.5) M=16 (total W/L = 128/ 0.5) nMOSFET fabricated on the 3.3-V/0.35-μm PD-SOI process used in this work. The nMOS threshold voltage for this process is nominally 0.65 V. Several important details about body driving can be discerned from Figure 3.6. First, as the gate voltage is biased

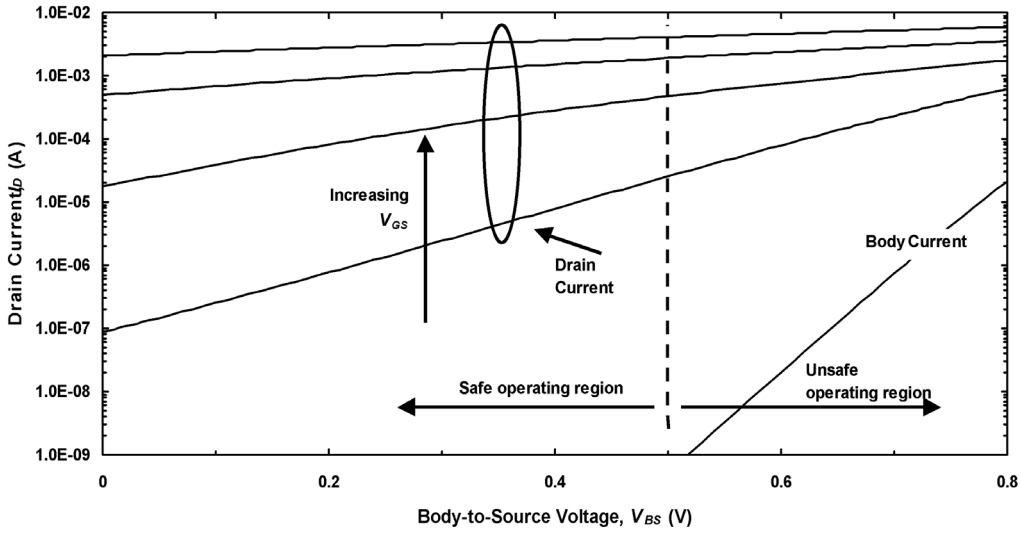


Figure 3.6: Measured I_D–V_{BS}–V_{GS} for a 8/0.5 M=16 (total W/L = 128/0.5) PD-SOI nMOSFET [1]

above, below, and nearly equal to the threshold voltage, this plot clearly shows that body driving is viable in the strong, weak, and moderate inversion regions. Second, this plot shows that the body current is insignificant even for relatively large forward bias voltages. Specifically, for a V_{BS} less than 0.5 V the body current is less than 1 nA. From this we can define a "safe operating region" whose demarcation line is the V_{BS} = 0.5-V point. Third, note that within the safe operating region it is possible to control the drain current over a four-decade range by manipulating both the gate and body voltages.

3.4 Small-Signal Models for Body-Driven MOSFETs

3.4.1 Complete Electrical Model

Small-signal modeling is the foundation of all analog circuit analysis. In this section the DC and AC small-signal models for a body-driven PD-SOI MOSFET will be presented.

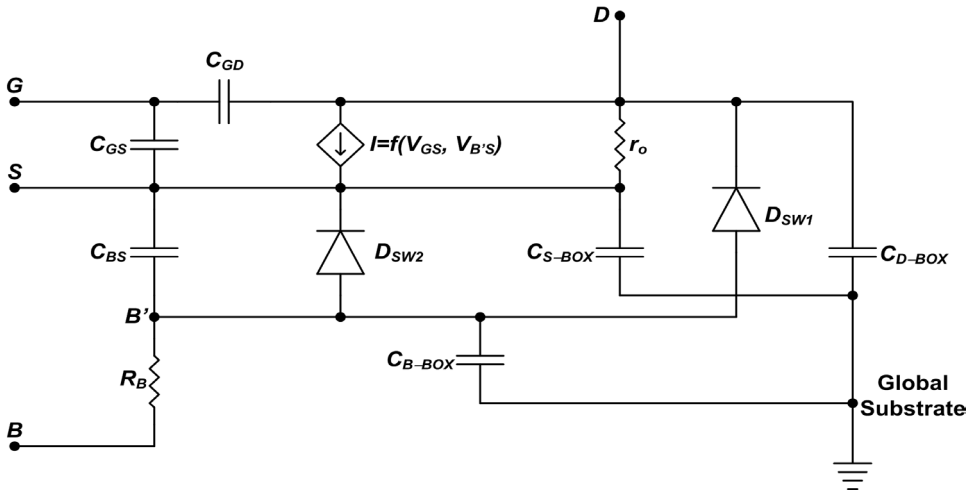


Figure 3.7: Complete electrical model for a PD-SOI MOSFET

Figure 3.7 presents the complete electrical model of a PD-SOI transistor, which is the basis for all of the models described here. There is a single current generator shown in the model which is controlled by both the gate–source and body–source voltages. Quantitatively, the drain current generator in strong inversion is described by

$$I_D = \frac{\beta}{2}(V_{GS} - V_{TH}(V_{B'S}))^2, \tag{3.1}$$

where β is the MOSFET transconductance factor given by

$$\beta = \mu C_{OX}(W/L). \tag{3.2}$$

$V_{TH}(V_{B'S})$ is the bias dependent threshold voltage given by

$$V_{TH}(V_{B'S}) = V_{TH0} + \gamma\sqrt{2\phi_F - V_{B'S}} - \gamma\sqrt{2\phi_F}, \tag{3.3}$$

where V_{TH0} is the zero-bias threshold voltage, γ is the body-effect coefficient, and ϕ_F is the Fermi potential [26]. Likewise, in weak inversion the relationship between body voltage and drain current is described by the bias dependent threshold voltage

$$I_D = 2n\mu C_{OX}(W/L)U_T^2 \exp\left(\frac{V_{GS} - V_{TH}(V_{B'S})}{nU_T}\right). \tag{3.4}$$

Thus in all MOSFET operating regions the body effect is modeled as a shift in the threshold voltage with body bias.

The device capacitances include C_{GS}, C_{GD}, and C_{BS}, which are the primary intrinsic components, C_{S-BOX} and C_{D-BOX} (the oxide capacitances between the source/drain and the handling wafer), and the sidewall junction capacitances, which are the primary extrinsic capacitances. Also included in this model is a body resistance, R_B. While body resistance is present in bulk CMOS transistors, it is typically very small and can be ignored. In contrast, the isolated nature of the SOI transistor body means body resistance could be significant, and it should always be considered during the design and layout of SOI circuits.

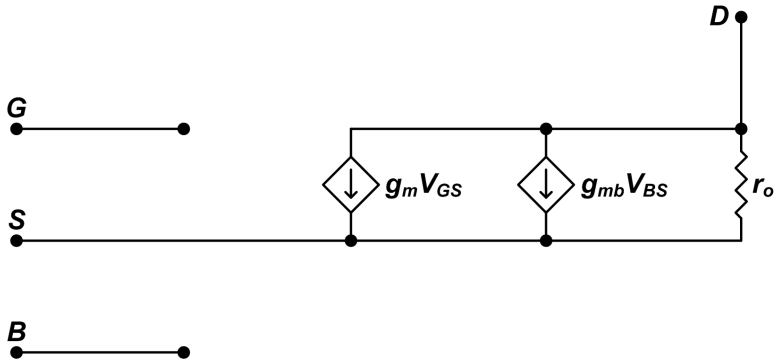


Figure 3.8: Small-signal DC model for a MOSFET

3.4.2 DC Model

Figure 3.8 presents the DC small-signal model for a body-driven PD-SOI MOSFET, which is identical to the standard small-signal model used in bulk MOSFET models. In this model there are two current generators, one controlled by the gate voltage and one controlled by the body voltage, allowing separate consideration of the two transconductnaces. Note also that since there is virtually zero DC body current, body resistance has no impact for DC and low-frequency applications and can be ignored. The small-signal body transconductance can be found by differentiating the drain current with respect to the body voltage, assuming that the gate and drain voltages are held constant. Thus, in strong inversion the body transconductance is calculated as

$$\begin{aligned} g_{mb} &= \left.\frac{\partial I_D}{\partial V_{BS}}\right|_{V_{DS},\, V_{GS}=c} = \beta(V_{GS} - V_{TH}(V_{BS}))\left(-\frac{dV_{TH}}{dV_{BS}}\right) \\ g_{mb} &= g_m\left(-\frac{dV_{TH}}{dV_{BS}}\right), \end{aligned} \tag{3.5}$$

where g_m is the gate transconductance. Likewise in weak inversion the body transcon-

ductance is given by

$$g_{mb} = \left.\frac{\partial I_D}{\partial V_{BS}}\right|_{V_{DS},\, V_{GS}\ const} = \frac{1}{nU_T}\exp\left(\frac{V_{GS} - V_{TH}(V_{BS})}{nU_T}\right)\left(-\frac{dV_{TH}}{dV_{BS}}\right)$$
$$g_{mb} = g_m\left(-\frac{V_{TH}}{V_{BS}}\right). \tag{3.6}$$

In both cases the body transconductance is equal to the gate transconductance multiplied by the derivative of the threshold voltage with respect to the body voltage. This derivative is labeled η, the body-effect parameter, and is critically important in body-driven circuit design as it describes the relationship between gate transconductance and body transconductance in all operating regions

$$\eta = -\frac{dV_{TH}}{dV_{BS}} = \frac{g_{mb}}{g_m}. \tag{3.7}$$

Differentiating V_{TH} from Equation 3.3 with respect to V_{BS}, η can be calculated as

$$\eta = \frac{\gamma}{2\sqrt{2\phi_F - V_{BS}}}. \tag{3.8}$$

η is typically close to $1/3$ at V_{BS} = 0, and will of course increase as V_{BS} is forward biased.

3.4.3 AC Model

It is of particular interest in the AC analysis of body-driven circuits to compare the frequency response of body-driven MOSFETs to gate-driven MOSFETs. In this section the

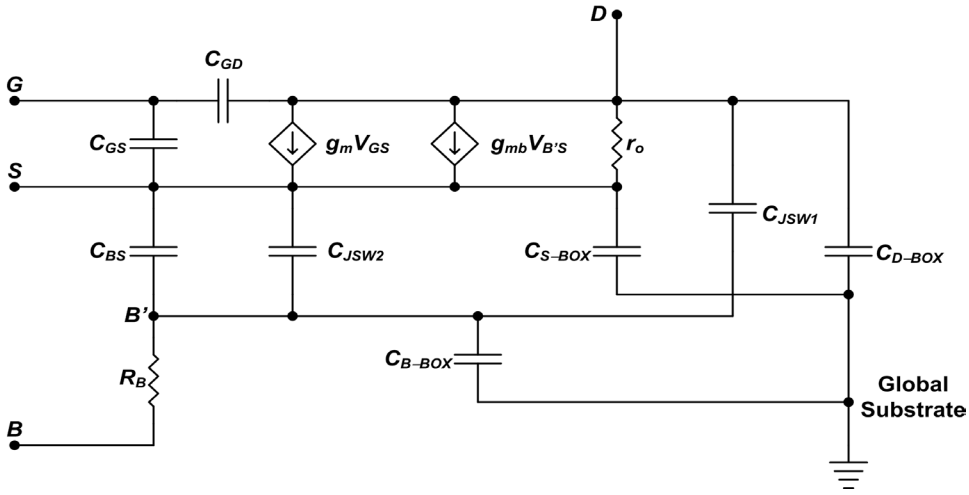


Figure 3.9: Small-signal AC model for a PD-SOI MOSFET

frequency response of body-driven and gate-driven transistors will be compared by analyzing the unity current gain frequency f_T for each. Additionally, the role of body resistance in determining the frequency response of a body-driven MOSFET will be studied using the concept of the –3-dB frequency for the body transconductance. Figure 3.9 presents the small-signal AC model for a PD-SOI MOSFET, including the important intrinsic and extrinsic device capacitances. It is of particular interest in the AC analysis of body-driven circuits to compare their high-frequency capability to that of a gate-driven MOSFET of the same size. Generally speaking, a body-driven MOSFET will always have a degraded frequency response when compared to a same size gate-driven MOSFET, though the degree of degradation will depend on the device sizing and technology chosen. Of course PD-SOI, with its low junction capacitance, will always be superior to a same generation bulk CMOS technology.

A common figure of merit for describing the high-frequency performance of a transistor is the current transfer unity-gain frequency f_T. For a gate-driven MOSFET, f_T is given by [26]

$$f_{T,GD} = \frac{g_m}{2\pi \cdot (C_{GS} + C_{GD})}, \tag{3.9}$$

where C_{GD} can generally be ignored because it is much smaller than C_{GS} when the MOSFET is saturated. For a body-driven MOSFET, the f_T can be defined by analogy

$$f_{T,BD} = \frac{g_{mb}}{2\pi(C_{BS} + C_{B-BOX} + C_{BD})}, \tag{3.10}$$

where C_{BS} + $C_{B–BOX}$ are the capacitances connected from the body to small-signal ground and replace C_{GS} in Equation 3.9, while C_{BD} replaces C_{GD}. Note however that in Equation 3.10 C_{BD} is a junction capacitance which could be large, and therefore cannot be ignored. The capacitances in the body-driven MOSFET structure are given by

$$C_{BS} = C_{BSi} + C_{JSW1}, \tag{3.11}$$

where C_{JSW1} is defined in Figure 3.9. C_{BSi} is the total intrinsic body–source capacitance and is given by [28]

$$C_{BSi} = \eta C_{GS}. \tag{3.12}$$

C_{JSW1} is the junction capacitance of the body–source diode and is equal to

$$C_{JSW1} = C'_{JSW} W X_J, \tag{3.13}$$

where C'_{JSW} is the sidewall junction capacitance per unit area, W is the MOSFET width, and X_J is the MOSFET source/drain junction depth. To compare the capacitances in the body-driven MOSFET to capacitances in the gate-driven MOSFET, Equation 3.13 can be re-written in terms of the MOSFET oxide-capacitance per-unit-area and channel length as

$$C_{JSW1} = C'_{OX} W L_{MIN} \cdot (X_J / L_{MIN}) \cdot (C'_{JSW} / C'_{OX}), \tag{3.14}$$

where L_{MIN} is the minimum channel length, or 0.35 μm for this technology. Using the values of X_J, C'_{JSW}, and C_{OX} presented in the vendor-supplied SPICE model, Equation 3.14 can be simplified to

$$C_{JSW1} \approx (1/3) \cdot C'_{OX} W L_{MIN} . \tag{3.15}$$

C_{BD} is dominated by the drain–body junction capacitance, which has the same physical dimensions as the body–source junction capacitance, and is therefore given by

$$C_{JSW2} \approx (1/3) \cdot C'_{OX} W L_{MIN} . \tag{3.16}$$

Finally, the body to handling-wafer capacitance, denoted C_{B-BOX}, can be ignored since the buried oxide layer is typically 50 times thicker than the gate oxide.

The f_T of a gate-driven and body-driven MOSFET can now be compared by first writing the gate-driven f_T as a function of channel length and gate-overdrive voltage (i.e., substitute the expression for MOSFET strong inversion transconductance as function of gate-overdrive voltage into Equation 3.9) [26]

$$f_{T,\,GD} \approx \frac{3\mu(V_{GS} - V_{TH})}{4\pi L^2}. \tag{3.17}$$

Similarly, substituting Equations 3.12, 3.15, and 3.16 into Equation 3.10 and writing f_T in terms of channel length and gate overdrive voltage, yields

$$f_{T,\,BD} \approx \frac{3\mu(V_{GS} - V_{TH})}{4\pi \cdot [L^2 + (2/(3\eta))(L \cdot L_{MIN})]}. \tag{3.18}$$

Equation 3.18 shows that the body-driven f_T is identical to the gate-driven f_T except for an additional term in the denominator which scales as L^1. This extra term represents the junction capacitances and it does not scale as L^2 because the junction capacitances depend on W and X_J and not L. Figure 3.10 presents a plot of the normalized f_T ($f_{T,BD}$/ $f_{T,GD}$) vs. normalized channel length (L/L_{MIN}) for a 0.35-μm PD-SOI nMOSFET. This plot shows that at minimum channel length the body-driven f_T is roughly one-third of the gate-driven f_T, while the body-driven f_T approaches the gate-driven f_T as channel length increases. The f_T of the body-driven and gate-driven MOSFETs converge because the

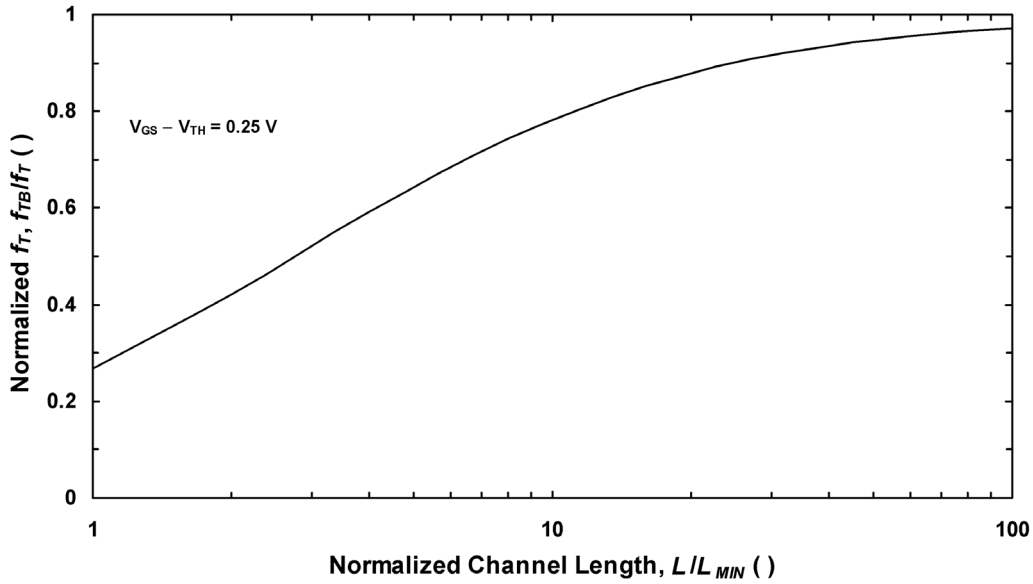


Figure 3.10: Normalized f_T ($f_{T,BD}/f_{T,GD}$) vs. normalized channel length (L/L_{MIN}) for a 0.35-μm PD-SOI nMOSFET

parasitic junction capacitances, which account for the reduction in body-driven f_T relative to the gate-driven case, are independent of channel length. Therefore as channel length increases the parasitic junction capacitances remain constant and become a progressively smaller percentage of the total intrinsic body capacitance. Figure 3.11 presents the calculated f_T for body-driven and gate-driven MOSFETs as a function of channel length. From this plot one can see that it is possible to achieve an f_T of roughly 5 GHz for a body-driven nMOSFET with L = 0.35 μm and a gate overdrive of 250 mV.

The final aspect of AC performance that will be considered is the effect of body resistance. Since the body resistance is in series with the body, it will have no effect on current gain. However, since MOSFETs are typically voltage driven, the body resistance will

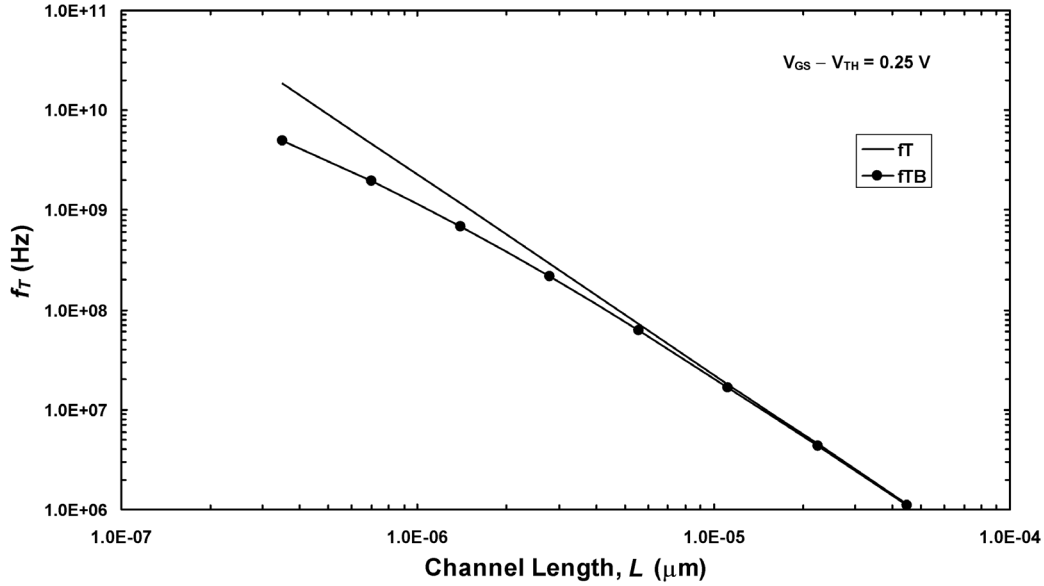


Figure 3.11: Body-driven and gate-driven f_T versus channel length for a 0.35-μm PD-SOI nMOSFET

create a pole in the voltage transfer function, which can be denoted f_{TV} where

$$f_{TV} = \frac{(1/R_B)}{2\pi \cdot (C_{BSi} + C_{JSW1} + C_{JSW2} + C_{B-Box})} . \tag{3.19}$$

Comparing Equations 3.10 and 3.19, it is clear that a body-driven MOSFET must be biased/sized such that $(1/R_B) < g_{mb}$ to ensure that the body resistance does not limit the frequency response.

3.5 SPICE Model

When designing complex circuits and systems in highly scaled CMOS technologies, it is essential to make use of a SPICE-based simulator to quickly predict how a circuit will function. Of course, the accuracy of any simulation is limited by the models used, and

since body driving is a non-standard operating mode for a MOS transistor, it is especially important to verify that one's standard MOS models can accurately describe body-driven transistors. In this section two aspects of MOS modeling will be considered—intrinsic models and extrinsic models. Intrinsic models describe characteristics of the core MOSFET, such as drain current, transconductance, threshold voltage, etc. Examples of intrinsic models are BSIM3V3 and EKV. On the other hand, extrinsic models describe parasitic components of the MOSFET including source/drain resistance, junction capacitance, and junction leakage current. Unlike intrinsic models, extrinsic models are typically provided by the simulator and shared in common among all MOSFET models [27].

3.5.1 Intrinsic Models—BSIM3V3 vs. EKV2.6

When beginning the design process for this research project, one of the first tasks undertaken was to verify the accuracy of the vendor supplied BSIM3V3 model. To this end, DC measurements were made for single body-driven transistors and compared to simulation. From this study it was found that BSIM3V3 shows significant errors when modeling the g_{mb} and η of MOSFETs with a forward biased body–source voltage—which is, of course, *the* standard operating region for body-driven transistors. The problem seems to be that BSIM3V3 applies an absolute value function to V_{BS} that causes an unrealistic discontinuity in η–V_{BS} at V_{BS} = 0, and also causes η to decrease with increasing V_{BS} under forward bias conditions.

To solve this problem, the EKV2.6 MOSFET model was utilized for most of the design process. Unlike the BSIM3V3 model, the EKV model guarantees that all primary vari-

ables (e.g., terminal voltages and currents) and their first derivatives (e.g., conductances and resistances) are continuous functions [28]. Therefore the EKV model does not show any discontinuity in η–V_{BS}. Since an EKV model was not available from the vendor, a custom EKV model was generated using the following process [29]:

- Start with a generic EKV model (one is available from the EKV website) [30].
- For a given measurement (e.g., I_D–V_{GS}) run a sweep using the vendor-supplied BSIM model and EKV model and compare the results. Modify the EKV parameter(s) which affect the measurement under consideration until the two curves match [29].
- Repeat this process for all critical DC measurements, which are I_D–V_{GS} log (for characterizing the weak-inversion region and sub-threshold slope), I_D–V_{GS} lin (for characterizing the strong-inversion region), and I_D–V_{DS} (for characterizing output impedance).
- Note that all fits are done with MOSFETs biased at V_{BS} = 0, which is a region where BSIM is accurate.

Although it may seem to be a very tedious task to generate a custom SPICE model, in fact it is straightforward to generate an EKV2.6 model because of the small number of parameters, and the very small degree of correlation among parameters. The small degree of correlation means that it is possible to optimize one characteristic of the model's performance by varying only one parameter. For example, the parameter GAMMA is used to set the sub-threshold slope, threshold voltage is set by matching I_D–

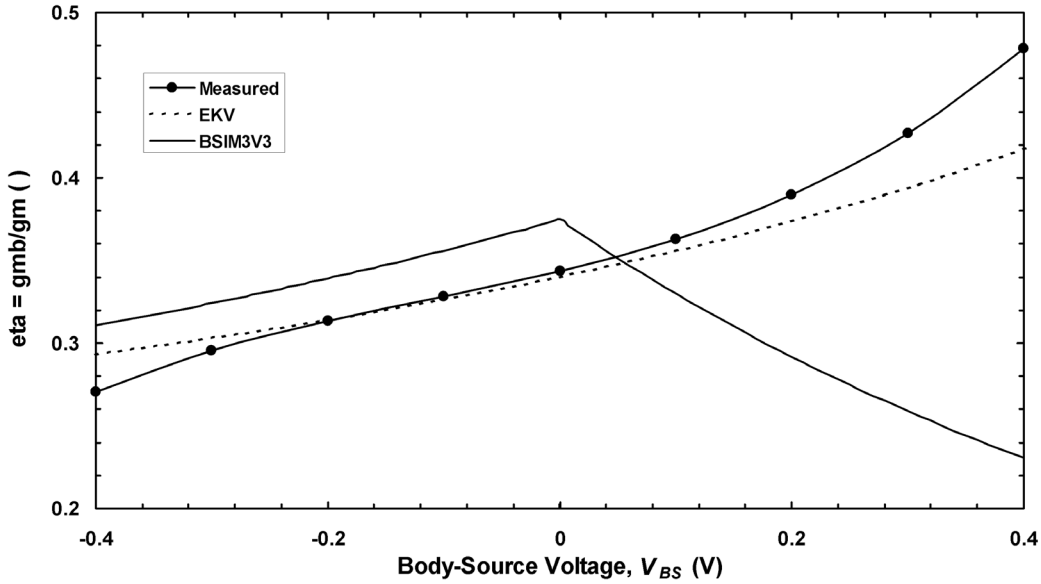


Figure 3.12: Comparison of measured and simulated (BSIM3V3 and custom generated EKV2.6) η–V_{BS} for an 8/0.5 M=16 PD-SOI nMOSFET

V_{GS} in weak inversion (i.e., log I_D), and mobility is set by matching I_D–V_{GS} in strong inversion. Figure 3.12 presents a comparison of the measured and simulated (BSIM3V3 and custom-generated EKV2.6) η–V_{BS} for an 8/0.5 M=16 PD-SOI nMOSFET. This plot clearly shows a discontinuity in the BSIM3V3 curve, and good agreement between the EKV2.6 and measured curves. As a final note to the reader interested in designing body-driven circuits, it should also be mentioned that the η–V_{BS} discontinuity was observed in a number of BSIM3V3 models taken from different foundries and different technology generations. Therefore this result is a problem with the BSIM3V3 model and not the extraction methodology. In addition, a similar characteristic was observed in a bench-mark BSIM4 model which was downloaded from the BSIM website [31].

3.5.2 Extrinsic Models

The second important aspect of SPICE models considered here is the extrinsic model, in particular the characteristics of the parasitic MOSFET drain–body and source–body diodes. Table 3.1 lists the key parameters which are used to describe the parasitic MOSFET diodes. These parameters can be divided into two broad groups. The first group, consisting of ACM, HDIF, PD/PS, and AD/AS, can be called the geometric parameters because they describe the dimensions of the diodes. The second group, consisting of JS, JSW, CJ, and CJSW, can be called the physical parameters because they describe the physical characteristics of the junctions, specifically they describe the junction leakage current and capacitance. In this section we will focus on how to determine the parameters in the second group.

First, it should be noted that in all SOI technologies, the source/drain implants extend all the way down to the BOX; therefore there is no bottom-plate junction in SOI and the parameters JS and CJ should be set to zero. CJSW, which is the primary parasitic junction capacitance for a body-driven MOSFET, is also important in gate-driven MOSFETs and should be determined by the vendor and included with the vendor-supplied SPICE model. The final parameter of interest is JSW, which models the leakage current of the parasitic diodes. In almost all gate-driven circuit designs, the drain–body and source–body diodes are reverse biased, and so the precise value of the diode saturation current is not important. For this reason the parameter JSW is typically not set in SPICE models, and a default parameter is used instead. However, in body driving the source–body

Table 3.1: Key parameters for extrinsic MOSFET model [27]

Parameter	Definition	Usage
ACM	area calculation method—defines how diode area and periphery will be calculated	set in model by vendor, set to 2 in this work
HDIF	roughly defines the width of a source/drain contact	must set if not set by vendor, set per standard transistor layout
PS, PD	source/drain periphery	set per a specific transistor layout
AS, AD	source/drain area	set per a specific transistor layout
JS	saturation current density for bottom-plate source/drain diode	set to zero for SOI
JSW	saturation current density for side-wall source/drain diode	must set based on measurement
CJ	zero-bias junction capacitance for bottom-plate source/drain diode	set to zero for SOI
CJSW	zero-bias junction capacitance for side-wall source/drain diode	will be set in model by vendor

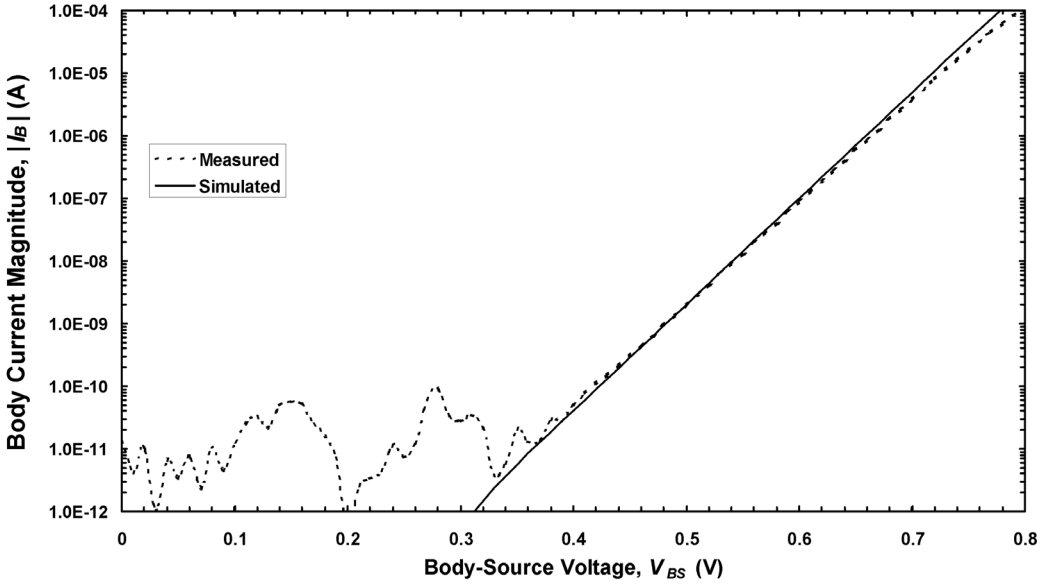


Figure 3.13: Comparison of measured and simulated (using a fitted parameter for JSW) I_B–V_{BS} for an 8/0.5 M=16 PD-SOI nMOSFET

diode is almost always forward biased which means that significant current levels could be present (e.g., nA to μA, as in Figure 3.6). The problem with using the default JSW parameter for body driving is that it always significantly overestimates the true levels of leakage current, and so would result in overly conservative circuit designs. Therefore when designing SOI body-driven circuits, it is critically important that one sets the JSW parameter based on device measurements (i.e., measurements of I_B–V_{BS}). Figure 3.13 presents a comparison of the measured and simulated (using a fitted parameter for JSW) leakage current of an 8/0.5 M=16 nMOSFET fabricated on the PD-SOI process used in this work.

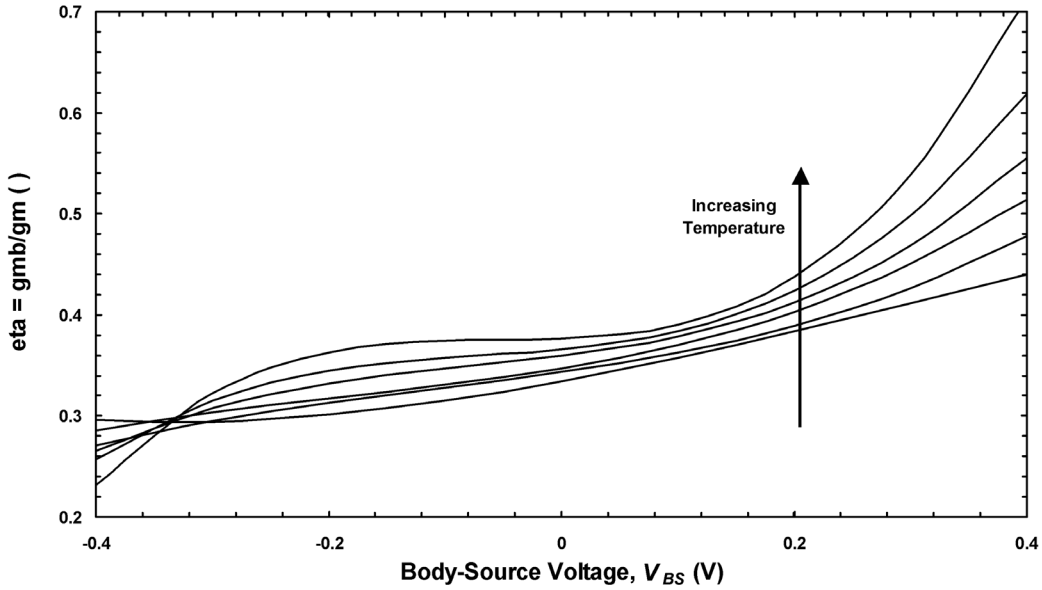


Figure 3.14: Measured η–V_{BS} for an 8/0.5 M=16 PD-SOI MOSFET; temperature is swept from 0°C to +125°C in 25°C steps

3.6 Temperature Characteristics

Temperature performance is the final aspect of body-driven MOSFET performance that will be considered in this chapter. Increased operating temperature primarily affects body-driven circuits in two ways, one of which results in improved performance and the other of which results in reduced performance. The first important effect associated with temperature is that the body–channel depletion region thickness shrinks as temperature increases, which means that the coupling of the body to the channel, and hence the transconductance efficiency (g_{mb}/I_D), increases with increasing temperature. Figure 3.14 presents the measured η–V_{BS} for an 8/0.5 M=16 PD-SOI nMOSFET with temperature swept from 0°C to +125°C in 25°C steps. In this plot η is measured by taking the derivative of the MOSFET threshold voltage with respect to body–source voltage, *as per* Equa-

tion 3.7, at several different body–source voltages. The threshold voltage was extracted by measuring the I_D–V_{GS} and g_m–V_{GS} for an Ohmic MOSFET (V_{DS} = 50 mV) and then finding the x-intercept point defined by [32]

$$V_{TH} = V_{GS(g_{max})} - \frac{I_{DS(g_{max})}}{g_{max}} - 50mV, \tag{3.20}$$

where g_{max} is the maximum transconductance achieved by the Ohmic MOSFET (which typically occurs at a gate overdrive voltage of roughly 300 mV). The data presented in Figure 3.14 show that η increases 10% in going from 0°C to +125°C at V_{BS} = 0.1 V, and 15% in going from 0°C to +125°C at V_{BS} = 0.2 V, which, as will be shown later, bounds the standard V_{BS} operating voltages for body-driven transistors.

The second important aspect of body-driven circuit performance that is affected by temperature is the junction leakage current. Figure 3.15 presents the measured I_B–V_{BS} for an 8/0.5 M=16 PD-SOI nMOSFET with temperature swept from 0°C to +125°C in 25°C steps. This plot shows that the 125°C temperature change results in a greater than four-decade increase in leakage current for a given body–source voltage. However, if we take 10 nA as the maximum allowable junction leakage current, this plot also shows that it is possible to operate with a V_{BS} of 0.3 V at +125°C. It will be shown in Chapter 5 that body-driven circuits will rarely ever need to operate with a V_{BS} greater than 0.3 V; thus body driving is possible even up to +125°C.

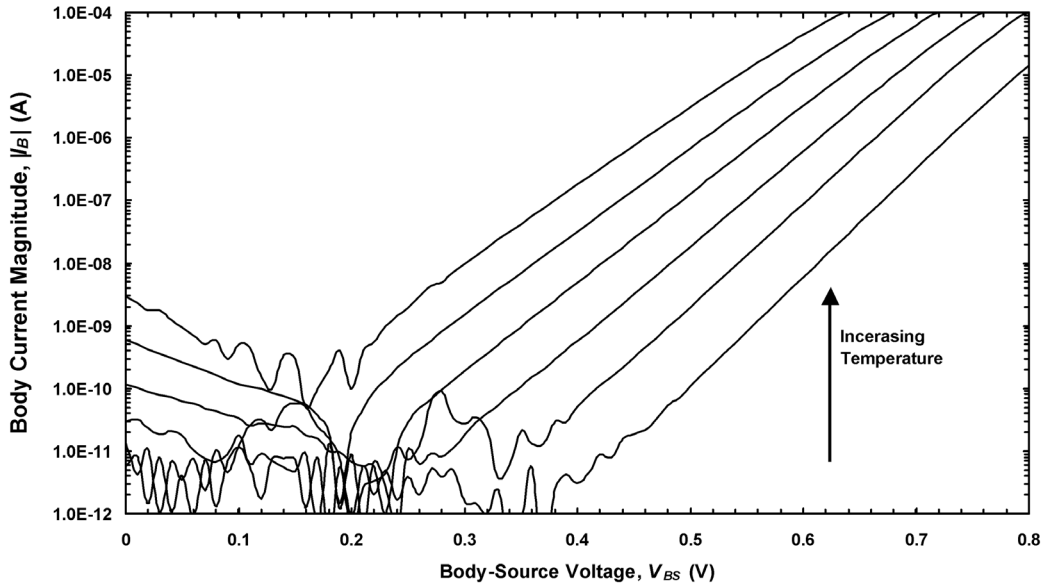


Figure 3.15: Measured I_B–V_{BS} for an 8/0.5 M=16 PD-SOI MOSFET; temperature is swept from 0°C to +125°C in 25°C steps

3.7 Conclusions

This chapter has presented a complete introduction to the operation and modeling of the body-driven transistor. In Section 3.2 different technology options for body driving were introduced, including triple-well bulk CMOS and partially depleted SOI CMOS, and it was shown that PD-SOI is ideal for body-driven applications because of the reduced junction area. Section 3.3 presented DC bias curves for a body-driven MOSFET and showed that it is possible to operate a body-driven transistor in weak, moderate, and strong inversion. In Section 3.4 the DC and AC small-signal models for the body-driven transistor were presented, and it was shown that the f_T of a body-driven transistor is typically one-third the f_T of a same-size gate-driven transistor, assuming $L = L_{MIN}$. SPICE modeling was discussed in Section 3.5, and it was shown that EKV2.6 is superior to BSIM3V3 for body-driven applications because EKV accurately models η–V_{BS} for positive V_{BS}.

Finally, the temperature characteristics of body-driven transistors were examined in Section 3.6, and it was shown body-driven transistors should be able to operate up to +125°C.

Chapter 4

Literature Review

4.1 Introduction

Chapter 4, which presents a literature review of body-driven circuits and primitives, serves two purposes. First, by reviewing the current state of the art in body-driven circuits and primitives, it is possible to explicitly show how this dissertation research advances the state of the art. Second, presenting multiple examples of body-driven circuits and primitives is probably the best way explain both the potential of and the design challenges associated with body-driven circuit design. In this chapter Section 4.2 presents a literature review of the current state of the art in body-driven current mirrors. Section 4.3 presents a literature review of the current state of the art in body-driven differential pairs, and Section 4.4 presents a literature review of the current state of the art for body-driven op-amps. Finally, Section 4.5 concludes this chapter.

4.2 Literature Review—Body-Driven Current Mirrors

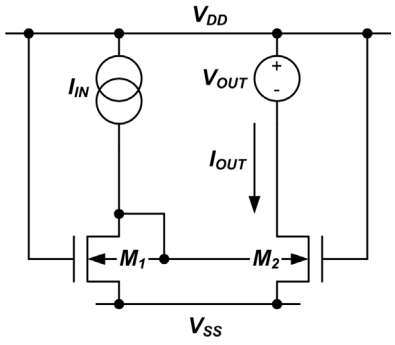
Now that the structure and biasing characteristics for single body-driven MOSFETs have been studied, we can consider the operation of body-driven analog primitives (that is, body-driven sub-circuits such as current mirrors and differential pairs) and body-driven op-amps. The first body-driven primitive that will be studied in this review is the current mirror. The body-driven current mirror is one of the potentially most useful, but also one of the most challenging to design, of all the body-driven circuit primitives. The utility of the body-driven current mirror lies in the fact that, since there is no threshold voltage

required for turn-on, it is possible to operate with input *and* output voltages of V_{DSAT}. This is in contrast to a gate-driven current mirror, which can have a minimum output voltage of V_{DSAT}, but requires an input voltage greater than $V_{TH} + V_{DSAT}$. Unfortunately, the advantages of the body-driven current mirror come at a cost—primarily design difficulty. The major challenge of designing body-driven current mirrors lies in the fact that the body-driven MOSFET is a depletion-mode or normally-on device; thus it is difficult to ensure that the reference MOSFET in a body-driven current mirror is biased in saturation. The other important drawback is the possibility of excessively forward biasing the body–source junctions, although this is generally much less of an issue than biasing the reference device in saturation. In this section several body-driven current mirrors will be presented to show how this circuit primitive works, and how others have dealt with the inherent design challenges. The circuits described in this section represent the state of the art for body-driven current mirrors.

4.2.1 Simple Current Mirror I

Figure 4.1 (a) presents the schematic of the first implementation of a body-driven simple current mirror [33]. As one can see, the MOSFETs are biased with $V_{GS} = V_{DD}$ to create an inversion channel between the source and drain. The reference MOSFET, M_1, is connected drain–body, and the body voltage is copied to the output device, M_2, to create the current mirror. It is clear that the body-driven current mirror is directly analogous to a standard gate-driven current mirror, with the body terminals acting as gates. However, while they may look similar, the DC performance of this simple body-driven current is quite different from that of a gate-driven current mirror.

(a)



(b)

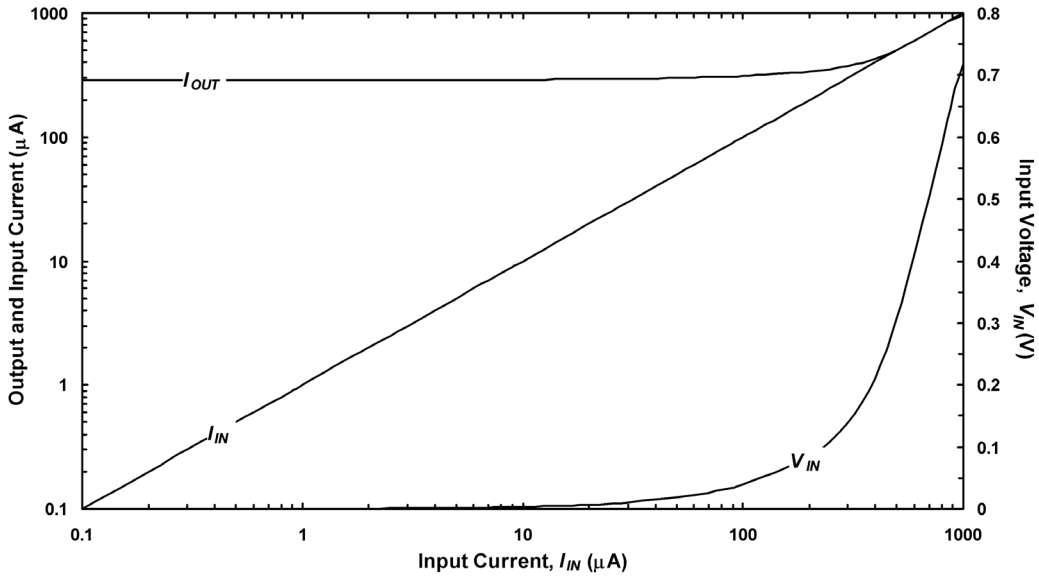


Figure 4.1: Body-driven simple current mirror with static gate bias: (a) schematic [33] and (b) simulated transfer characteristic

Figure 4.1 (b) presents the simulated I_{OUT}–I_{IN} transfer characteristic for this current mirror. Unless otherwise noted, all simulations in this chapter are run with V_{DD} = 1 V, and use the custom generated EKV model that describes the PD-SOI CMOS process used in this work (see Section 3.5.1). The zero-bias nMOS threshold voltage for this process is nominally 0.65 V. For all current mirror simulations run in this section the input current is swept over a four-decade range, from 100 nA to 1 mA. All of the current mirrors simulated are sized 8/0.5 M = 4 (total W/L = 32/0.5), and the nMOS technology current for this process is roughly 350 nA at room temperature, so the inversion coefficient (IC) is swept from roughly 0.05 to 50—a range that includes the weak, moderate, and strong inversion regions [10].

Looking at Figure 4.1 (b), one can immediately see the problem with this basic implementation of the body-driven current mirror. For most of the input range the output current is fixed at roughly 200 μA, it is not until the input current rises above 200 μA that the output current begins to track the input. The problem with this implementation of the current mirror is that the saturation current for M_1, which is set by the gate bias and device sizing as

$$I_{DSAT} = \frac{\beta}{2}(V_{DD} - V_{TH})^2, \tag{4.1}$$

is less than the input current for most of the input range. Clearly, if the input current is less than the saturation current the reference MOSFET will be operating in the Ohmic region and the output current will not be a faithful replica of the input. The V_{IN}–I_{IN} curve

in Figure 4.1 (b) confirms that the reference device is in the Ohmic region over most of the input current range.

Due to its low input voltage requirements, the body-driven current mirror has the potential to be an important element in analog circuit designs. However, in its simplest implementation, which could be called a body-driven current mirror with static gate bias, the depletion-mode characteristics of the body-driven MOSFET make this circuit unusable for most analog designs. Of course, one could shrink the mirror devices (i.e., shrink β) so that the current mirror enters saturation at a lower current level. While this would allow the current mirror to operate at lower current levels, it does not address the fundamental problem, namely that the current mirror will not enter the saturation region until $V_{IN} > V_{DD} - V_{TH}$. For a V_{TH} of 650 mV, this means that a 350-mV input voltage is required at 1-V V_{DD}. In a smaller feature size technology with a V_{TH} of 500 mV, a 500-mV input voltage would be required. Thus, it seems that the real problem with this circuit is that it is "voltage biased" as opposed to "current biased," which is the technique used in almost all robust analog circuits.

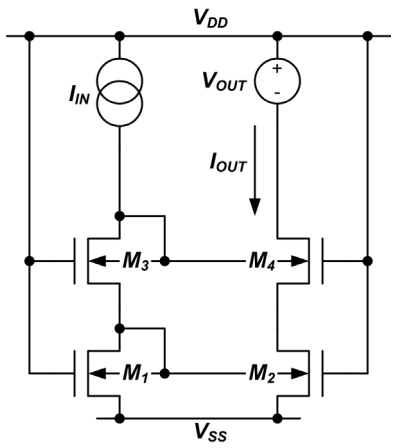
Nevertheless, even the small range over which this current mirror did operate properly highlights the potential of this circuit for low-voltage design. Additionally, it is important to understand and study this basic current mirror, as it forms the foundation of all other body-driven current mirrors. In fact, all of the prior-art current mirrors and the new current mirror techniques developed in this research are merely presenting methods for improving the performance of this basic current mirror. Finally, it should be noted that this current mirror was first implemented in a 2-μm CMOS process with a threshold voltage of

0.85 V, which is 200 mV higher than the 0.65-V threshold devices used in this work. Thus, when originally implemented, the current mirror would have entered saturation at a V_{IN} of approximately 150 mV when operated with a V_{DD} of 1 V, and would have been much more useful as a low-voltage current mirror.

4.2.2 Simple Cascode Current Mirror

Figure 4.2 (a) presents a schematic of the first body-driven simple cascode current mirror [34]. Like the body-driven simple current mirror just presented, this circuit is the body-driven equivalent of the gate-driven simple cascode current mirror. The purpose of the cascode devices is to improve output impedance, but also to improve linearity by allowing the input mirror devices to operate in the Ohmic region while the cascode devices operate in saturation. Since the top devices have less V_{GS} than the bottom devices, they will become saturated first and act to equalize the V_{DS} on the bottom devices, thus improving linearity. Figure 4.2 (b) presents the simulated I_{OUT}–I_{IN} transfer characteristic for this circuit. Though the devices are sized the same as the MOSFETs in the simple current mirror (8/0.5 M = 4), the saturation current is less and the current mirror enters saturation earlier. The saturation current is less because when the bottom devices are in the Ohmic region, the two series MOSFETs can effectively be considered as a single MOSFET whose channel length is the sum of two channel lengths, thus β is reduced by a factor of two with respect to the simple current mirror. The current mirror enters saturation earlier because only the cascode devices, which have a lower $V_{GS} - V_{TH}$ than the bottom devices, have to saturate for the mirror to act linearly.

(a)



(b)

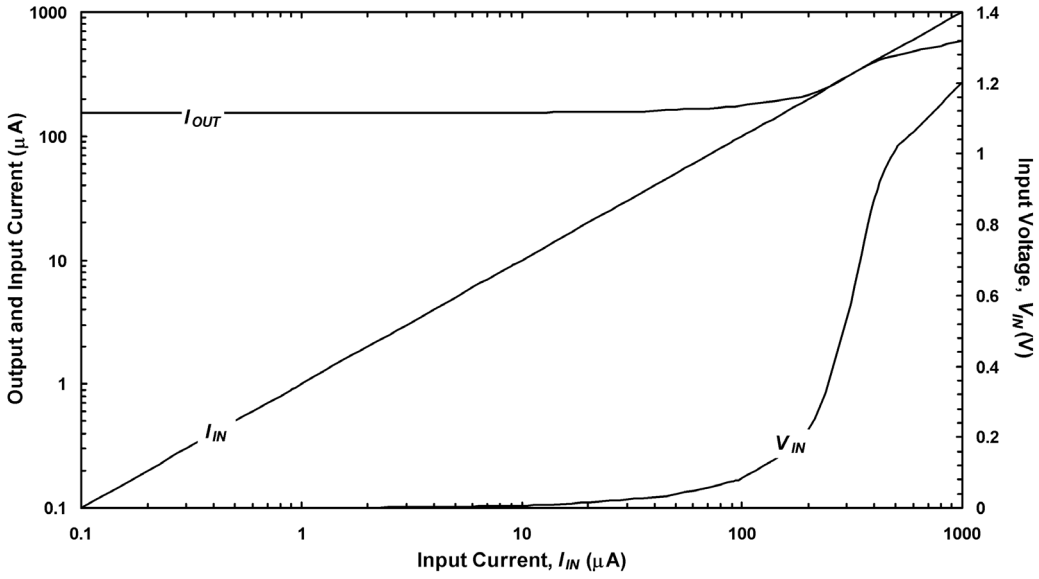


Figure 4.2: Body-driven simple cascode current mirror with static gate bias: (a) schematic [34] and (b) simulated transfer characteristic

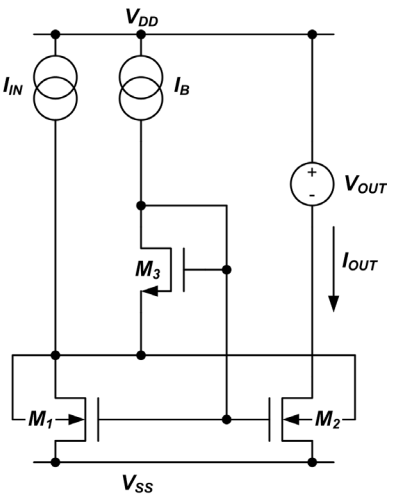
On the other hand, it seems that a key problem with this circuit is the large input voltage required for the MOSFETs to enter saturation, since there are now two V_{BS} in series. Thus, while this current mirror does seem to have some advantages over the simple current mirror, in terms of linearity, the large input voltage requirement reduces the usefulness of this circuit as a low-voltage current mirror. However, it should again be noted that this mirror was originally implemented in a 2-μm CMOS process with 0.85-V threshold voltages. In this case the mirror saturated at a much lower input voltage and was useful as a low-voltage circuit element (indeed, this mirror was used in the construction of a 1-V cascode OTA [34]).

4.2.3 Simple Current Mirror II

One interesting solution to the problem of body-driven current mirrors is presented in Figure 4.3 (a) [35]. The core of this circuit is the standard body-driven simple current mirror, but added to this is an nMOS level shifter biased at approximately $V_{GS} = V_{TH}$ and connected between gate and body terminals of the body-driven current mirror. By reducing the gate voltage to $V_{IN} + V_{TH}$, the saturation current is greatly reduced at low input currents, and the linear input range of the current mirror is greatly increased. Furthermore, since the level shift voltage is equal to V_{TH}, and independent of V_{DD}, this bias scheme will have low sensitivity to process and V_{DD} variations.

The simulated I_{OUT}–I_{IN} transfer characteristic is presented in Figure 4.3 (b). In this plot one can see that this mirror does have a much larger current range than body-driven cur-

(a)



(b)

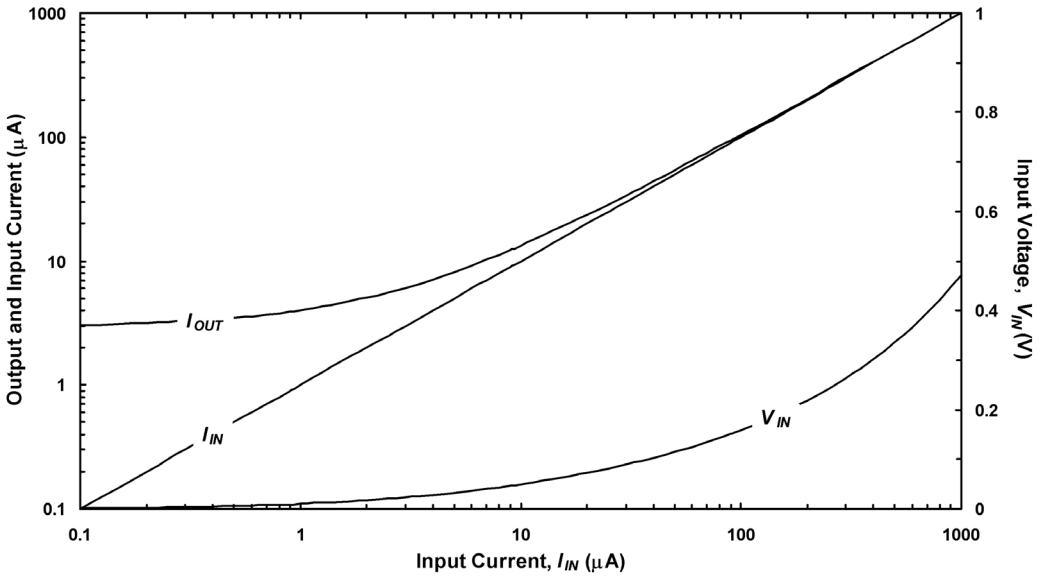


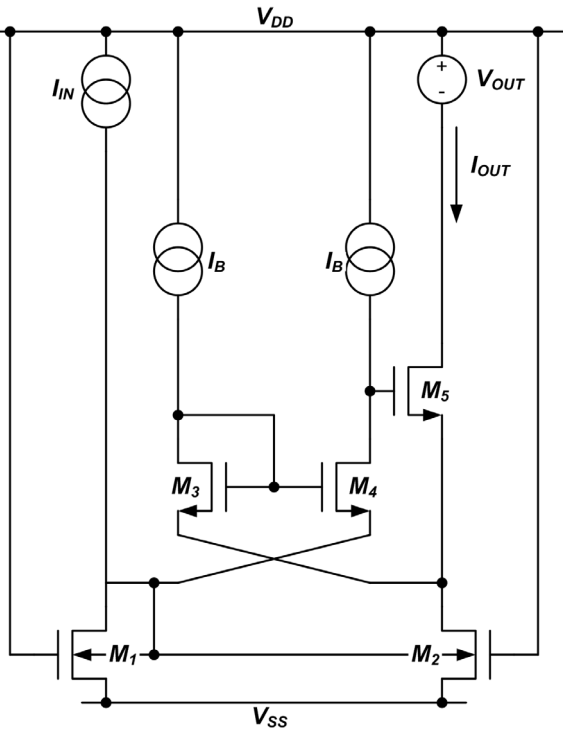
Figure 4.3: Body-driven simple current mirror with level-shifted, dynamic gate bias: (a) schematic [35] and (b) simulated transfer characteristic (Bias current I_B is 100 nA.)

rent mirrors that utilize static gate bias. However, it still cannot operate linearly over the entire input range. Furthermore, though it is possible to achieve better low-end performance by decreasing the V_{GS} of the level-shift device, this would necessarily reduce the high-end performance, and vice-versa. Another important drawback of this circuit is that the minimum required V_{DD} is roughly $(V_{IN} + V_{GS3} + V_{DSAT})$, which could be too high for some low-voltage applications. In Chapter 5, an original body-driven current mirror is presented that can operate over an even larger range and has a minimum required V_{DD} of only $V_{GS} + V_{DSAT} \cdot (1 - \eta)$.

4.2.4 Regulated Cascode Current Mirror

Figure 4.4 (a) presents the schematic of a body-driven regulated cascode current mirror which combines gate driving and body driving within the same circuit [36]. Like the body-driven simple cascode current mirror, this circuit attempts to operate the bottom devices in the Ohmic region, but achieves good linearity by using extra circuitry to match the V_{DS} for the mirror devices. In this case an active regulation amplifier is used to achieve V_{DS} matching and good linearity. Figure 4.4 (b) presents the simulated I_{OUT}–I_{IN} transfer characteristic for this circuit. This circuit has a wider linear range than any of the previous current mirrors; however, it still does not operate linearly over the entire input range. However, the main problem with this current mirror is that the gates are biased at V_{DD} for all input current levels. Thus, even though a regulation amplifier is used to improve matching, the input voltage will be too low at very low input currents to achieve good matching.

(a)



(b)

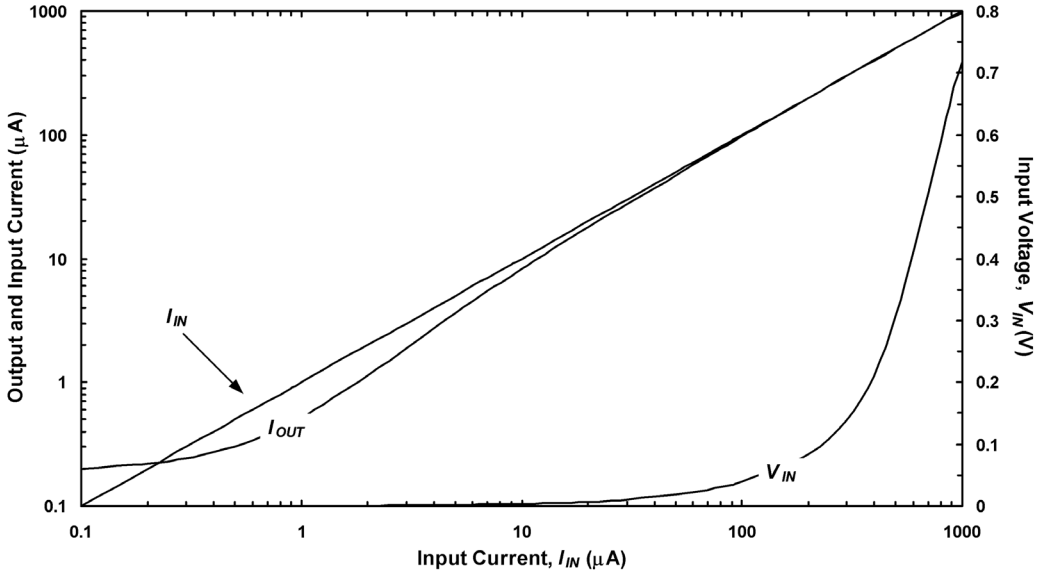


Figure 4.4: Body-driven regulated cascode current mirror: (a) schematic [36] and (b) simulated transfer characteristic (I_B is equal to 100 nA.)

4.2.5 Comparison of the Body-Driven Current Mirrors

Finally, it is important to summarize the literature review of body-driven current mirrors to explain where shortcomings exist and thus where opportunities for contributions to body-driven circuit design exist. Generally speaking, the utility of any circuit primitive can be expressed only insofar as it is able to meet the real needs of circuit designers. With respect to current mirrors, it is therefore necessary to first consider what the needs of circuit designers are. Paradoxically, one of the shortcomings of the prior art current mirrors presented is that the focus was always on developing a current mirror *per se*; that is, the focus has been on developing a circuit element which takes an input current and produces a single scaled replica of the input current at its output. However, for high-performance analog circuits, this is often not exactly what is needed. Instead, what is needed is a method for building arrays of high-impedance current sources, which are then used as tail current sources, loads for cascode gain stages, etc. In this respect, prior-art body-driven current mirrors do not meet the needs of low-voltage analog circuit designers.

To better understand the shortcomings of the prior-art current mirrors, first consider the regulated cascode current mirror presented in Figure 4.4 (a). While this circuit is relatively useful for taking an input current and producing one output current, it cannot be used to take one input current and generate multiple replicas of the output current. The reason for this is that the regulation amplifier is constructed such that for every output branch, a regulation amplifier and input reference branch would be required. Using this circuit, it is technically possible to generate several replicas of the output with unregulated cascode current sources. To do this copies of M_2 and M_5 could be arrayed, with the gate bias of M_5 being used as the cascode bias, and the body bias of M_1, M_2 used as

the body bias (the gate bias of all current source devices would be tied to V_{DD}). The problem with this is that the mirror devices would be in deep Ohmic and without a regulation amplifier this current source would not be any better than a simple current mirror. In considering the development of high-impedance current source arrays, the key problem with the level-shifted current mirror of Figure 4.3 (a) is somewhat different. In this circuit, the mirror device is saturated over a wide range; however, in using this bias technique it is difficult to ensure that the mirror device is biased precisely at $V_{DS} = V_{DSAT}$. This condition is critical for biasing low-voltage cascode current mirrors because any excess drain overdrive ($V_{DS} - V_{DSAT} > 0$) on the mirror devices is lost for dynamic signal swing on the drains of cascode devices. On the other hand, if the V_{DS} of the current source devices is biased less than V_{DSAT}, the output impedance of the cascode current sources would be compromised. Therefore it is important in low-voltage design to have a bias technique that guarantees the mirror devices are biased precisely at $V_{DS} = V_{DSAT}$. Finally, the current mirrors using static gate bias are important to study because they represent the foundation of body-driven current mirrors. However, since they use a gate bias that is sensitive to V_{DD} and process variations (i.e., V_{TH}), they will not be useful as elements in high-performance analog circuit designs.

It should also be noted that none of the body-driven current mirrors presented allow the designer to explicitly define the inversion coefficient of the transistors, while also guaranteeing that $V_{DS} = V_{DSAT}$. It is the opinion of this author that the inversion coefficient based design technique presented by Binkley *et al.* [10] is essential for the design of high-performance analog circuits, because it allows the designer to optimize the perfor-

mance trade-offs provided by the different transistor operating regions. Thus any body-driven design technique should also be applicable to all MOSFET operating regions and allow the designer to explicitly consider the MOSFET inversion coefficient.

From this discussion, it is clear that many opportunities exist for developing body-driven current mirror design techniques that will represent a contribution to the field of low-voltage, high-performance body-driven circuit design. Specifically, techniques are required that allow the designer to bias a body-driven MOSFET precisely at $V_{DS} = V_{DSAT}$ to optimize the trade-off between output impedance and signal swing at low voltages, but that also allow the designer to explicitly consider inversion coefficient as a design parameter.

4.3 Literature Review—Body-Driven Differential Pairs

In contrast to current mirrors, differential pairs constructed from depletion-mode devices are straightforward to design and function quite well—indeed often better than their enhancement-mode counterparts. In this section three different implementations of a body-driven differential pair are presented. These circuits represent the state of the art for body-driven differential pairs.

4.3.1 Differential Pair with Static Gate Bias

Figure 4.5 presents a schematic of a body-driven differential pair, which was first utilized in CMOS technology as a means of implementing very small transconductances for active CMOS filters with very long time constants [37, 38], and was later independently discovered as a means of implementing ultra-low-voltage analog circuits on standard

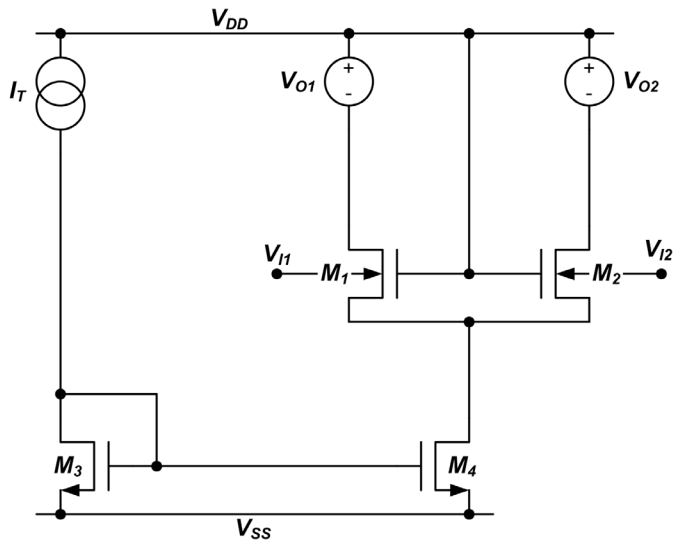


Figure 4.5: Body-driven differential pair with static gate bias [19]

CMOS technology [20]. The advantage of body driving in this application is that since there is no threshold voltage associated with the body, it is possible to achieve wide ICMR with a single-polarity differential pair. Figure 4.6 presents the simulated output current for M_1 and M_2 versus differential input voltage, with a common-mode input voltage of 0.5 V. In this plot we can see that the body-driven differential pair does indeed function just like a gate-driven pair, at least with respect to differential inputs. On the other hand, the main drawback of the body-driven differential pair is that the body transconductance will change as a function of common-mode level. Figure 4.7 presents the simulated body transconductance g_{mb} versus common-mode input voltage V_{ICM}. Over the common-mode range 0 to 1 V, the g_{mb} varies from roughly 200 μmho to 300 μmho, or 250 μmho +/– 20%. Another drawback of the variation in g_{mb} with V_{ICM} is that for a fixed threshold voltage mismatch between M_1 and M_2, the offset will vary as a function of com-

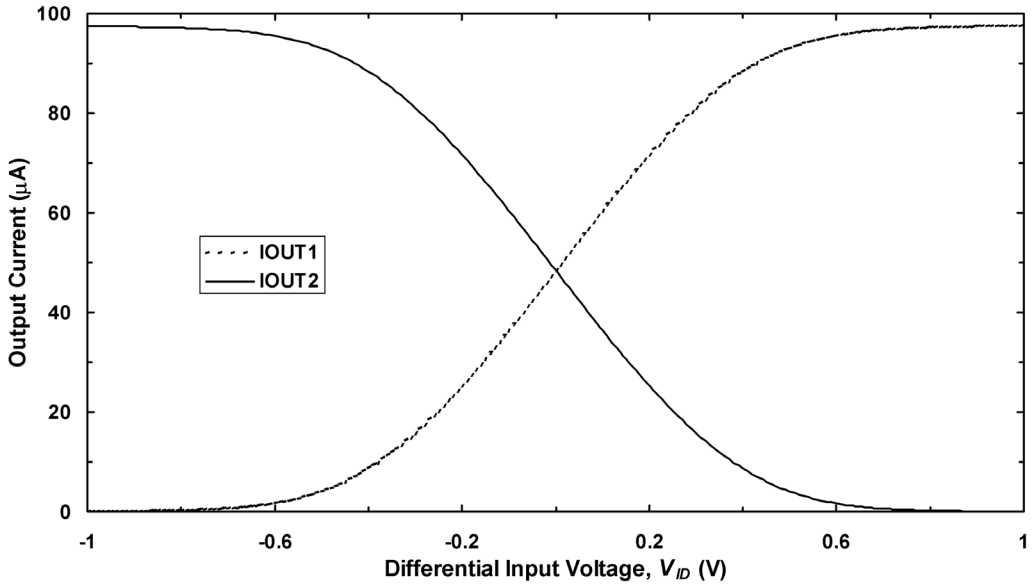


Figure 4.6: Simulated I_{OUT}–V_{ID} transfer characteristic for the body-driven differential pair with static gate bias (M_1 and M_2 are sized 8/0.5 M=4.)

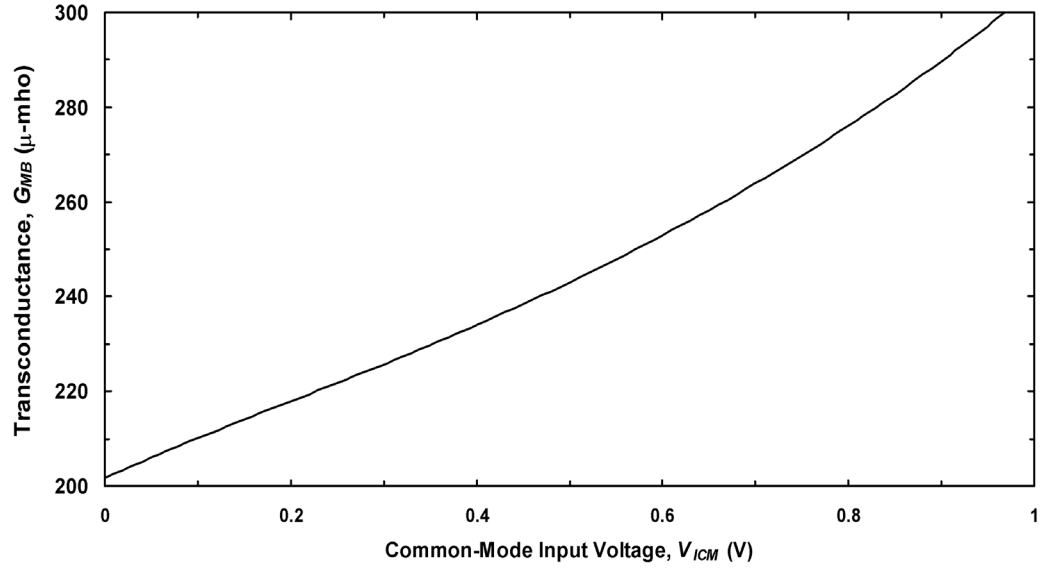


Figure 4.7: Simulated g_{mb}–V_{ICM} for the body-driven differential pair with static gate bias (M_1 and M_2 are sized 8/0.5 M=4.)

mon-mode level and thus degrade, and in fact often dominate, the CMRR. To alleviate this effect one must be certain to size the input pair devices large so as to minimize mismatch. Nevertheless, the low-voltage rail-to-rail ICMR capability of the body-driven differential pair outweighs the potential drawbacks for many applications. This is by far the most widely used body-driven primitive reported in the literature, and it will continue to be a useful element in low-voltage analog circuit designs.

4.3.2 Complementary Body-Driven Differential Pairs

While the body transconductance increases with increasing common-mode level in the n-type differential pair, the body transconductance of a p-type differential pair varies in a complementary fashion; that is, it decreases with increasing common-mode level. Therefore it is possible to compensate the variation of a single body-driven differential pair by connecting a complementary pair in parallel, as in Figure 4.8 [19, 39]. The simulated g_{mb}–V_{ICM} characteristic for the complementary differential pairs is presented in Figure 4.9. In this simulation the nMOS transconductance is 152 μmho +/– 20% over the ICMR, the pMOS transconductance is 86 μmho +/– 30% over the ICMR, while the aggregate transconductance is 242 μmho +/– 4%. Therefore the complementary body-driven pair can achieve constant bandwidth over a rail-to-rail ICMR. Additionally, since both pairs are turned-on for all common-mode inputs, the slew rate will be constant. The only drawback of the complementary input pair is that it will not help improve CMRR. However, this can be mitigated by using large input devices, common-centroid layout, etc. Also, since both pairs are always on, the offset voltage will vary continuously over the entire ICMR. This is in contrast to a standard complementary gate-driven differential pair, which will

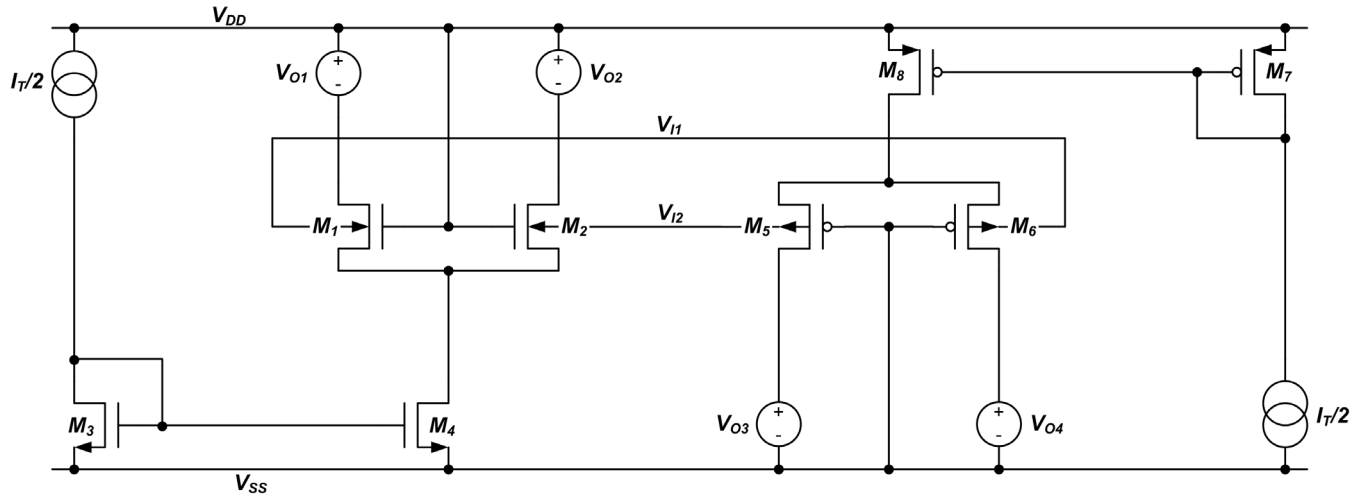


Figure 4.8: Complementary body-driven differential pairs with static gate bias [19]
M_1 and M_2 are sized 8/0.5 M=4, M_3 and M_4 are sized 8/0.5 M=10, and I_T = 100 μA.

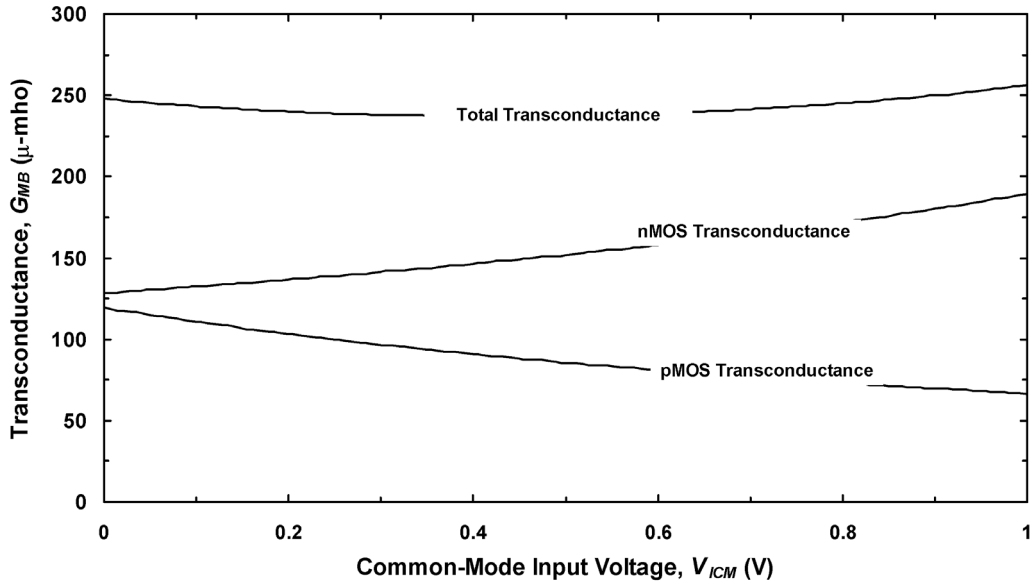


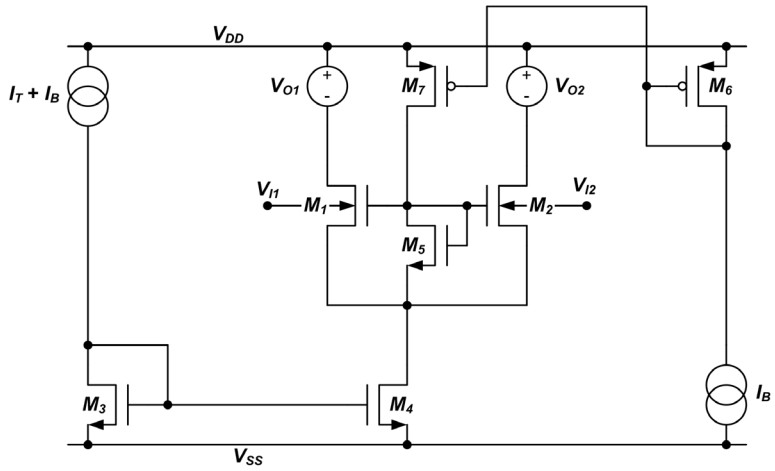
Figure 4.9: Simulated g_{mb}–V_{ICM} for complementary body-driven differential pairs

have a discontinuity in V_{OS}–V_{ICM} when operating at low supply voltages because there is only a very small range where both input pairs are turned on.

4.3.3 Differential Pair with "Floating Battery" Gate Bias

The final differential pair architecture that will be considered is the so-called "floating battery" gate bias [39], presented in Figure 4.10 (a). Instead of tying the MOSFET gates to the appropriate power supply, in this design the gate is dynamically biased by an nMOS V_{GS} level shifter connected from the common-source node to the common-gate node. In some ways this circuit is similar to the current mirror presented in Figure 4.3 (a), except in this design the nMOS level-shifter M_5 is matched to M_1 and M_2, and biased at the same current density. The goal is to keep the V_{GS} and I_D of the input pair devices constant, which also forces the V_{BS} and g_{mb} to be constant. One drawback of this structure

(a)



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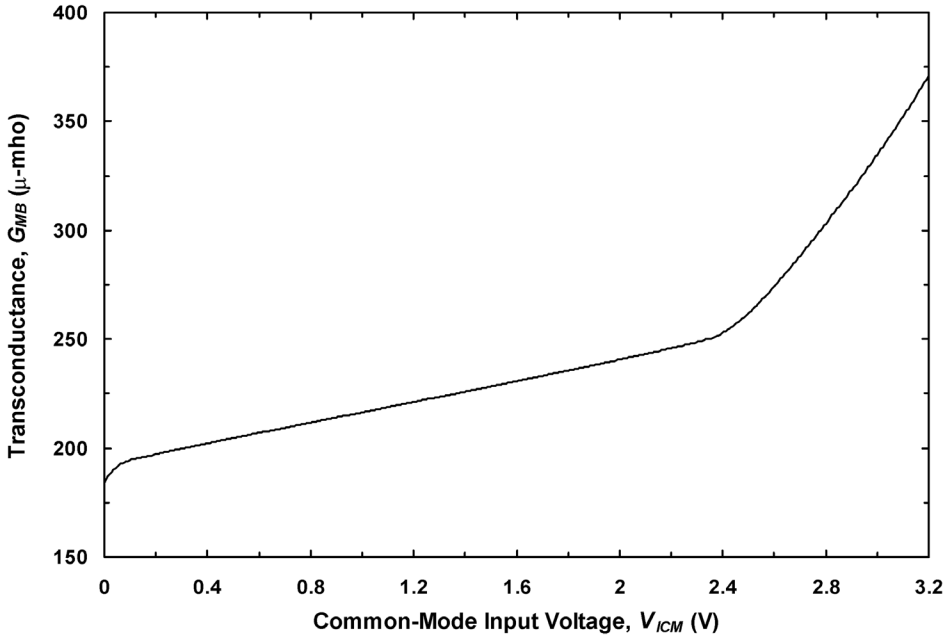

Figure 4.10: Body-driven differential pair with floating battery gate bias: (a) schematic [39] and (b) simulated g_{mb}–V_{ICM} (M_1 and M_2 are sized 8/0.5 M=4, M_3 is sized 8/0.5 M=2, I_T is equal to 100 μA, and I_B is equal to 25 μA.)

is that the total power supply voltage must now be higher than $V_{GS} + 2V_{DSAT}$. However, this circuit is very useful for systems that must operate over a wide power supply range (e.g., 1-V to 3.3-V V_{DD}). Figure 4.10 (b) presents the simulated g_{mb}–V_{ICM} for this circuit. Notice that g_{mb} increases rapidly when V_{ICM} is within 0.6 V of V_{DD}. This is because the gate of M_5 becomes clamped at V_{DD} for $V_{ICM} > V_{DD} - 0.6$ V.

4.3.4 Comparison of the Body-Driven Differential Pairs

In contrast to the body-driven current mirror, the body-driven differential pair in its simplest form is an extremely useful circuit element. While the complementary body-driven pair and differential pair with dynamic gate bias present advantages over the basic implementation, any one of the three might be chosen for a circuit design, based on the requirements of the application. Some new differential pairs can be quickly imagined, such as a combination of the complementary and dynamic gate bias structures to provide rail-to-rail, constant g_{mb} performance over a wide power supply range, and the use of offset correction signals fed to the gate terminals to minimize both offset and CMRR. Nevertheless it was not felt that the opportunities for advancing the state of the art in the design of body-driven differential pairs were as significant as in body-driven current mirror design, and the body-differential pair used in this work is directly based on prior-art differential pairs.

4.4 Literature Review—Body-Driven Operational Amplifiers

Now that the most important body-driven analog primitives have been presented, we can look at the application of the these cells to larger analog circuits. In this section three

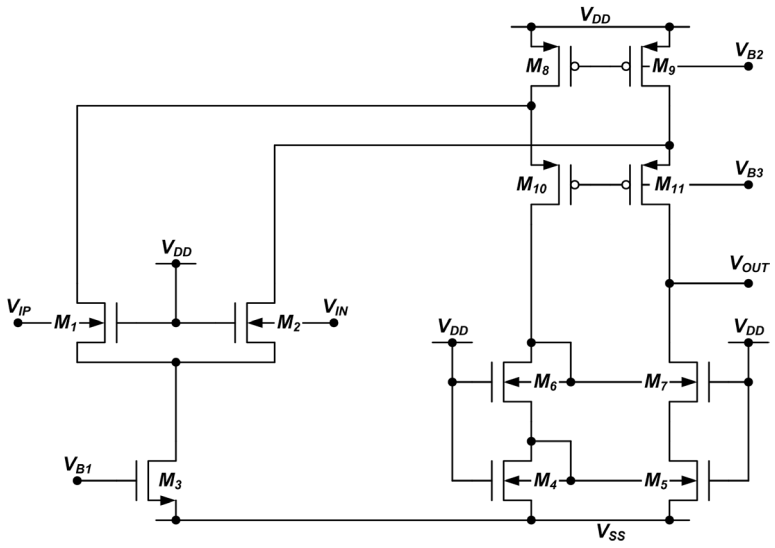

Figure 4.11: Early example of a body-driven OTA [34]

body-driven amplifiers, which represent the state of the art in body-driven analog design, will be presented.

4.4.1 Body-Driven OTA

Figure 4.11 presents one of the first examples of a body-driven operational transconductance amplifier (OTA) [34]. This circuit uses a standard folded cascode structure with nMOS input pair. However, it replaces the standard gate-driven input pair with a body-driven pair—thus achieving a wide ICMR. Likewise the nMOS current mirror in the output stage was replaced with a body-driven simple cascode mirror. The body-driven cascode current mirror has the dual advantages of reduced input voltage requirements (with respect to a gate-driven current mirror), and high output impedance. Note that as this circuit was implemented in a 2-μm CMOS technology with 0.85-V thresholds, it was much easier to utilize this current mirror with a low-input voltage, since the gate overdrive for

the current source devices was only 150 mV at 1-V V_{DD}. In fact, measurement results presented in [34] show that the current mirror operates linearly with input currents from 5 μA to 20 μA, with a corresponding input voltage over this range of 104 mV to 544 mV. Implemented in a p-well bulk CMOS technology, this OTA achieved a 1-MHz bandwidth at 10-pF load, 45-dB open-loop gain, 0.7-V ICMR, +/– 1-V/μs slew rate, and draws 120 μA from a 1-V power supply.

This OTA represents an important contribution to the field of body-driven circuit design because it clearly shows that body-driven primitives can be used to construct more complex and useful analog circuits. To this day, it is still the only body-driven circuit reported in the literature that makes use of two different types of body-driven primitives (i.e., body-driven differential pair and body-driven current mirror). On the other hand, the relatively low voltage gain shows that it is non-trivial to design body-driven circuits that approximate the performance of gate-driven circuits operating at higher power supply voltages.

4.4.2 Body-Driven Op-Amp I

Figure 4.12 presents a schematic of the first two-stage operational amplifier that utilized body-driven techniques. Fabricated in an n-well bulk CMOS technology, this amplifier uses a body-driven differential pair for an input stage but otherwise uses gate-driven transistors. In particular, note that the load for the differential pair is a gate-driven current mirror that uses bulk-CMOS compatible lateral PNP transistors as level shifters. Since the threshold voltage for this technology is roughly 0.85 V and the V_{EB} of the BJTs is roughly 0.7 V, it is straightforward to guarantee that M_1 and M_2 are biased in saturation.

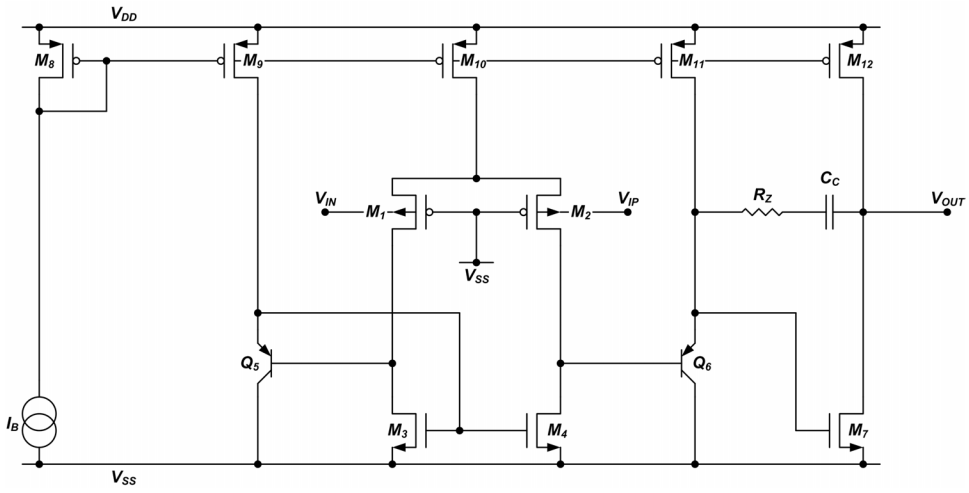

Figure 4.12: First two-stage body-driven op-amp [19]

With a total supply current of 300 μA, this op-amp achieved a bandwidth of 1.3 MHz, was capable of driving capacitive loads of 100 pF, and achieved an open-loop DC gain of 48 dB. One important limitation to the gain this amplifier could achieve is the necessity of low V_{DS} on devices M_3 and M_4, which would significantly compromise their output impedance.

4.4.3 Body-Driven Op-Amp II

Figure 4.13 presents an interesting example of a wide-ICMR input stage that utilizes depletion-mode, gate-driven nMOS transistors which are used as level shifters/buffers to drive a standard body-driven pMOS differential pair [41]. Note that, unlike the first two amplifiers, this circuit has been implemented in a CMOS technology that has special process options—specifically a zero-V_{TH} nMOS transistor. Generally speaking, it should be possible to achieve rail-to-rail ICMR with only an nMOS depletion-mode pair. This could

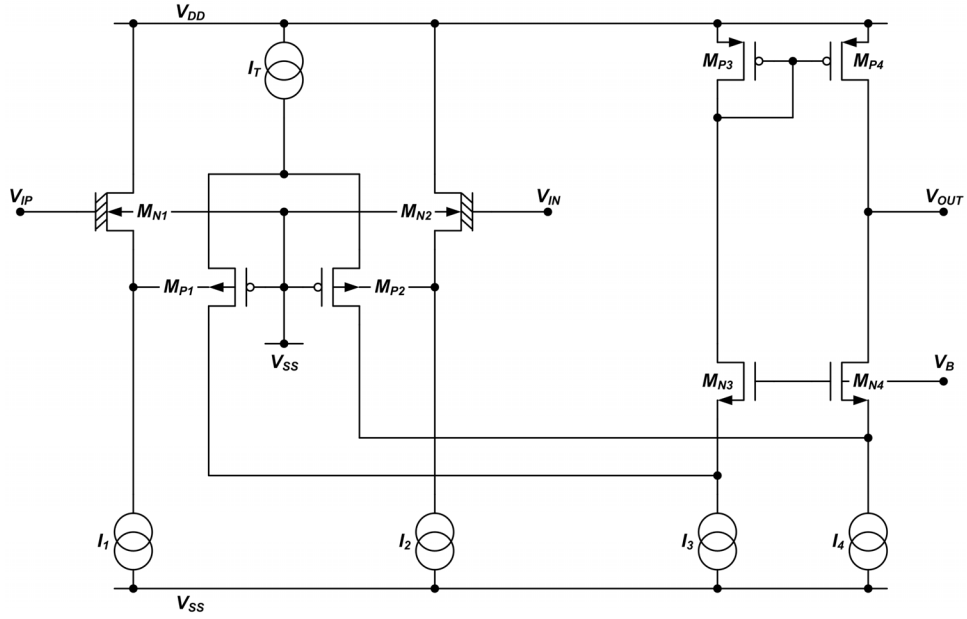

Figure 4.13: Wide-ICMR input stage utilizing depletion-mode, gate-driven nMOS and body-driven pMOS [41]

be done if the natural threshold voltage is more negative than −200 mV, thus allowing adequate V_{DS} on the tail current source at low V_{ICM}, while at high V_{ICM} body effect would shift the threshold voltage positive enough to allow the input pair to remain in saturation all the way up to $V_{ICM} = V_{DD}$. The problem with that strategy in this application is that the op-amp is specified to operate with a V_{DD} as low as 0.9 V, thus there will not necessarily be enough ICMR to sufficiently shift the threshold voltage of the nMOS pair at high V_{ICM}.

To address these problems the author in [41] decided to use the depletion-mode nMOSFETs as source followers to drive a pMOS body-driven differential pair. This approach would not add any low-end ICMR, but it does increase the high-end ICMR by approximately one V_{DSAT}. Of course, he could have simply dispensed with the nMOS input

devices altogether and used only the p-type body-driven differential pair. This strategy would have provided rail-to-rail ICMR, and would also have immediately improved noise performance by removing current sources I_1 and I_2 and MOSFETs M_{N1} and M_{N2}. In the paper he states that this path was not taken because of concerns about the input capacitance and leakage current of the body-driven input pair. It would have been especially interesting if he had fabricated both versions of the amplifier so that a comparison could be made. Unfortunately he did not.

Meant for portable, battery-powered applications, this amplifier uses only 500 nA supply current but has a corresponding bandwidth of only 5.6 kHz at C_L = 12 pF. The measured DC gain was between 70 and 79 dB, however the CMRR at 0.9-V V_{DD} is only 25 dB.

4.4.4 Comparison of the Body-Driven Amplifiers

Table 4.1 presents a comparison of the measured performance for the three body-driven amplifiers. While the data shows that it is certainly possible to design operational amplifiers using the body-driven circuit technique, the performance parameters listed here may not be sufficient for some applications. In particular, for the two Blalock amplifiers, relatively high bandwidth is achieved but the DC gain is less than 50 dB. On the other hand, the Stockstad amplifier achieves a voltage gain greater than 70 dB, but at a bandwidth of only 5.6 kHz. It seems likely that the use of very low bias currents in the Stockstad amplifier is an important component in achieving the high voltage gain. What has not been reported in the literature thus far is a 1-V body-driven operational amplifier that can achieve both wide bandwidth and high voltage gain. Moreover, what has also not been

Table 4.1: Measured performance parameters for state-of-the-art body-driven operational amplifiers

Parameter	Blalock OTA [34]	Blalock Op-Amp [40]	Stockstad Op-Amp [41]
DC Voltage Gain	45 dB	48 dB	70–79 dB
Small-Signal BW	1 MHz	1.3 MHz	5.6 kHz
SR^+	1 V/μs	0.7 V/μs	NA
SR^-	1 V/μs	1.6 V/μs	NA
I_{SUPPLY}	120 μA	287 μA	0. 5 μA
Power Supply Voltage	1 V	1 V	0.9–6 V
ICMR	0.7 V	966 mV	R2R

reported is an op-amp that utilizes high-impedance, body-driven cascode current sources and regulated cascode current sources to achieve good performance. It seems therefore that the construction of a 1-V body-driven amplifier that achieves high voltage gain and wide bandwidth through the use of high performance body-driven current sources would represent an important contribution to the field of low-voltage analog circuit design.

4.5 Conclusion

Chapter 4 has presented a review of the state of the art in body-driven analog circuit design. In Section 4.2 the state of the art for body-driven current mirrors was reviewed, and it was clearly shown that design techniques for body-driven current mirrors that are

suitable for the design of high-performance analog circuits have not yet been developed. In Section 4.3 the state of the art in body-driven differential pairs was reviewed. In this section it was shown that body-driven differential pairs are an extremely useful element for analog circuit design because they can achieve rail-to-rail ICMR with a single pair. Finally, Section 4.4 reviewed the state of the art in body-driven amplifiers. The amplifier review shows that body-driven op-amps have traditionally suffered from either poor bandwidth or low gain. Furthermore, it can be reasonably surmised that the lack of performance in body-driven amplifiers is due, at least in part, to the lack of high performance body-driven current sources.

Chapter 5

Design and Measurement of a High-Performance Body-Driven Operational Amplifier

5.1 Introduction

Chapter 5 presents the key contributions of this research, including the development of a high-performance body-driven op-amp. However, we will first begin with a review of what has been presented thus far. Chapter 2 presented a review of technology trends and showed that novel design techniques, including body driving, will be required to design high-performance analog circuits in highly scaled digital CMOS technologies. The primary purpose of Chapter 2 was to describe the current state of CMOS technology and to show why body driving is an important design technique. In Chapter 3 a detailed description of the operation and modeling of the body-driven transistor was presented. Chapter 3 was intended primarily as a tutorial explaining body-driven MOSFETs. Chapter 4 presented a detailed introduction to the design of body-driven circuits by examining several prior art current mirrors, differential pairs, and amplifiers. Besides being an introduction to the design of body-driven circuits, one of the key conclusions that can be drawn from Chapter 4 is that the development of high-performance body-driven current mirrors and current sources is essential to enable the design of high-performance body-driven analog circuits. Indeed, the poor voltage gain of the prior art body-driven amplifiers can be traced directly to the lack of high-impedance, body-driven current sources.

In this chapter, Section 5.2 describes the adaptive gate bias technique, which is the most important and fundamental contribution of this research. Adaptive gate biasing is a new technique for biasing body-driven current mirrors in saturation, and its purpose is to solve the problems shared by all of the prior art current mirrors discussed in Chapter 4. Section 5.3 describes the design and measurement of a body-driven operational amplifier. This op-amp heavily leveraged the adaptive gate bias technique and simultaneously achieved high open-loop gain and high bandwidth at 1-V power supply; however, this amplifier also showed poor PSRR and CMRR. In Section 5.4 the PSRR/CMRR problem is analyzed through the use of Monte Carlo analysis, and simple modifications which greatly improve the PSRR and CMRR are presented. The measurement results from a second body-driven op-amp that incorporates the proposed improvements are then presented. Section 5.5 presents a comparison of the body-driven amplifier developed in this research to several prior art op-amps to show that body driving enables true high-performance analog circuits. Finally, Section 5.6 concludes this chapter.

5.2 Designing Body-Driven Current Mirrors with Adaptive Gate Bias

Adaptive gate biasing is a new and unique circuit technique whose intended purpose is to enable the development of high-performance body-driven current mirrors and current sources, which will in turn lead to the development of high-performance body-driven amplifiers. The key characteristics of the adaptive gate bias technique can be summarized as follows:

- guarantees—independent of process, temperature, and power supply voltage—that the reference device in a body-driven current mirror will be biased with a V_{DS} equal to or just above the saturation voltage V_{DSAT},
- valid in all MOSFET operating regions, and
- allows the designer to explicitly consider MOSFET inversion coefficient as a design parameter.

In the rest of this section the development and application of the adaptive gate bias technique will be described.

5.2.1 A Universal MOSFET V_{DSAT} Extractor

5.2.1.1 EKV Model Review

The first step in developing the adaptive gate bias circuit is to build a sub-circuit that can extract the MOSFET saturation voltage in any MOS operating region. Such a circuit has been presented in various forms [42, 43], though it was best elucidated by Minch [44]. To understand this circuit we must first review some important concepts from the EKV model [33]. Instead of defining a single MOSFET drain–source current that is controlled by both the source and the drain, the EKV model defines two MOS currents—the forward current I_F, which is controlled by the source, and the reverse current I_R, which is controlled by the drain. The total drain current I_D is given by [28]

$$I_D = I_F - I_R . \tag{5.1}$$

If $I_F >> I_R$, then the MOSFET is operating in saturation. EKV uses these definitions because it allows the MOS structure to retains its inherent symmetry. For the circuit designer these concepts are useful because they often simplify the analysis of MOSFETs operating in the Ohmic region.

The forward and reverse currents in the EKV model are defined in terms of the terminal voltages in the following equations [28]

$$i_f = \left[\ln\left(1 + \exp\left(\frac{v_p - v_s}{2}\right)\right)\right]^2 \qquad (5.2)$$
$$i_r = \left[\ln\left(1 + \exp\left(\frac{v_p - v_d}{2}\right)\right)\right]^2,$$

where i_f and i_r are the normalized forward and reverse currents, respectively. Both currents are normalized by (W/L) and the so-called technology current I_0, as follows [10]

$$i_f = \frac{I_F}{I_0(W/L)}, i_r = \frac{I_R}{I_0(W/L)} \qquad (5.3)$$
$$I_0 = 2n\mu C_{OX}U_T^2.$$

Note that if a MOSFET is operating in saturation, then $I_D \cong I_F$ and i_f will be equivalent to the inversion coefficient (IC) defined by Vittoz [42] and later used by Binkley *et al*. [45].

v_p, v_d, and v_s are the normalized pinch-off, drain, and source voltages, respectively. A normalized voltage is defined simply as a terminal voltage (e.g., V_D) divided by the ther-

mal voltage U_T

$$v_i = \frac{V_i}{U_T}, \tag{5.4}$$

where *i* refers to any MOSFET terminal. Finally the pinch-off voltage V_P is a term unique to the EKV model, which is related to the gate overdrive voltage $V_G - V_{TH}$. However, the precise value of the pinch-off voltage is not important in the following analysis, it is only important to note that the pinch-off voltage is solely a function of the gate voltage. Therefore if two devices have the same gate voltage, they also have the same pinch-off voltage, regardless of their respective current levels, aspect ratios, or source/drain voltages. Note however that the EKV formulation uniformly assumes that all devices of the same polarity also have the same body voltage, which is typically the appropriate supply voltage. Thus if two devices have the same gate voltage but different body voltages, they will have different pinch-off voltages.

5.2.1.2 A Universal Definition for V_{DSAT}

Now that the EKV equations have been presented, it is possible to derive an expression for V_{DSAT} which is valid for all inversion levels. For this derivation, first recall that if $i_f >> i_r$, a MOSFET is operating in saturation. Conversely, if i_f is just slightly greater than i_r, the MOSFET is operating in the Ohmic region. It stands to reason then that there should be some minimum ratio $i_f / i_r > a$ for which the MOSFET is operating just at the edge of saturation. With this in mind, we can solve both of the equations in 5.2 for v_p and set them

equal to one another.

$$2nU_T \ln(\exp(\sqrt{i_r}) - 1) + V_D = 2nU_T \ln(\exp(\sqrt{i_f}) - 1) + V_S, \tag{5.5}$$

where the un-normalized terminal voltages have been used. Equation 5.5 can now be solved for V_{DS} as [44]

$$V_{DS} = 2nU_T \ln\left[\frac{(\exp(\sqrt{i_f}) - 1)}{(\exp(\sqrt{i_r}) - 1)}\right]. \tag{5.6}$$

Finally, by setting i_r equal to i_f/a, a definition of V_{DSAT} that is valid in all operating regions is obtained [44]

$$V_{DSAT} = 2nU_T \ln\left[\frac{(\exp(\sqrt{i_f}) - 1)}{(\exp(\sqrt{i_f/a}) - 1)}\right]. \tag{5.7}$$

Figure 5.1 presents a plot of Equation 5.7 with a = 17. It should be noted here that the MOSFET operating regions are defined in terms of the inversion coefficient as follows: IC < 0.1 defines the weak inversion region, 0.1 < IC < 10 defines the moderate inversion region, and IC > 10 defines the strong inversion region [10]. Looking at Figure 5.1, one can see that in weak inversion the V_{DSAT} is constant and equal to roughly 104 mV, or roughly four thermal voltages, in moderate inversion the V_{DSAT} becomes sensitive to inversion coefficient, while at the boundary between moderate and strong inversion V_{DSAT} is equal to roughly 216 mV. Note also that the saturation voltage in strong inversion is proportional to the square root of IC, or has a slope of +1/2 on a log-log scale,

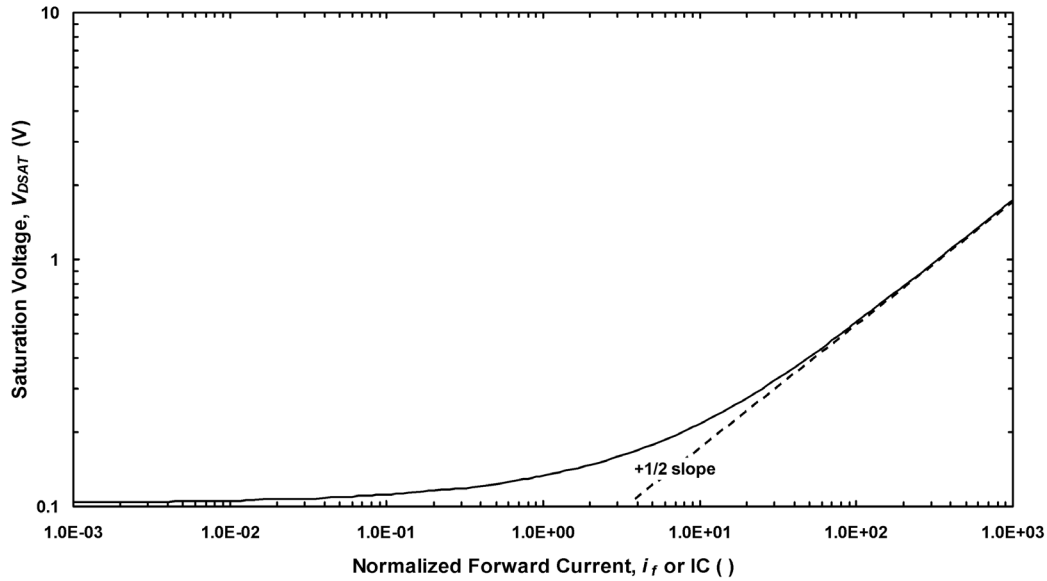

Figure 5.1: Plot of theoretical V_{DSAT}–IC, a=17

which also agrees with theory. Therefore Figure 5.1 shows that the V_{DSAT} definition presented in Equation 5.7 is valid in all operation regions.

Finally, it is important to note that the parameter *a* should be chosen based on achieving a certain output impedance and dynamic range trade-off. When V_{DSAT} is defined as in Equation 5.8, the boundary between the saturation and Ohmic regions becomes a design parameter. If one chooses a large *a*, then transistors will be biased farther out on the MOSFET saturation characteristic, resulting in higher output impedance but less output swing. Conversely, if one chooses a lower value of *a* the transistor will be biased closer to the “knee” region, and output impedance will be degraded while output swing will be increased. Generally speaking, a designer must find the value of *a* which best suits his design goals. In this work it was found that *a* = 17 provided a good trade-off between output impedance and signal swing.

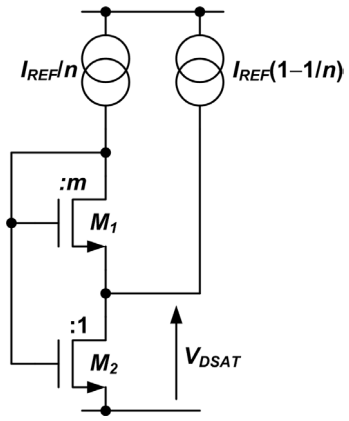

Figure 5.2: Circuit for extracting saturation voltage [44]

5.2.1.3 A Circuit for Defining i_f/i_r

The final step in developing a V_{DSAT} extractor is to build a circuit that can explicitly define the i_f/i_r ratio in a reference transistor. An example of such a circuit is presented in Figure 5.2 [44]. To understand how this circuit extracts the saturation voltage, we must calculate the i_f/i_r ratio in device M_2. Noting that $i_{f1}=i_{r2}$ since both devices have the same gate voltage (see Equation 5.2), we can write by inspection

$$\begin{aligned} i_{f1} &= \frac{I_{REF}}{nmI_0} \\ i_{d2} &= \frac{I_{REF}}{I_0} \\ i_{f1} &= i_{r2}\,. \end{aligned} \tag{5.8}$$

Next, Equation 5.1 can be applied to device M_2, and solved for i_{f2}/i_{r2} producing

$$\frac{i_{f2}}{i_{r2}} = 1 + \frac{i_{d2}}{i_{r2}} . \tag{5.9}$$

Lastly, substituting the equations of 5.8 into Equation 5.9 results in

$$\frac{i_{f2}}{i_{r2}} = 1 + nm . \tag{5.10}$$

Equation 5.10 shows that the circuit of Figure 5.2 defines the i_f/i_r ratio in a reference MOSFET (M_2), based only on the ratio of device sizes, and independent of temperature, operating region, power supply voltage, etc. If one chooses n = 4 and m = 4, then i_{f2}/i_{r2} will be equal to 17. Comparing Equations 5.10 and 5.7, it is clear that the V_{DS} of device M_2 must be equal to V_{DSAT} for any input current level.

5.2.2 Body-Driven Simple Current Mirror with Adaptive Gate Bias

5.2.2.1 Theory

As stated in the beginning of this section, the goal of adaptive gate biasing is to generate a gate bias that forces a MOSFET in a body-driven current mirror to operate at the edge of saturation. Put another way, the purpose of adaptive gate biasing is to enable the designer to explicitly define the saturation current in a body-driven MOSFET. One implementation of adaptive gate biasing for a simple current mirror is presented in Figure 5.3. In this circuit the current source on the left is the input for the user-defined saturation current, while the current source on the right is the input to the actual mirror. Note

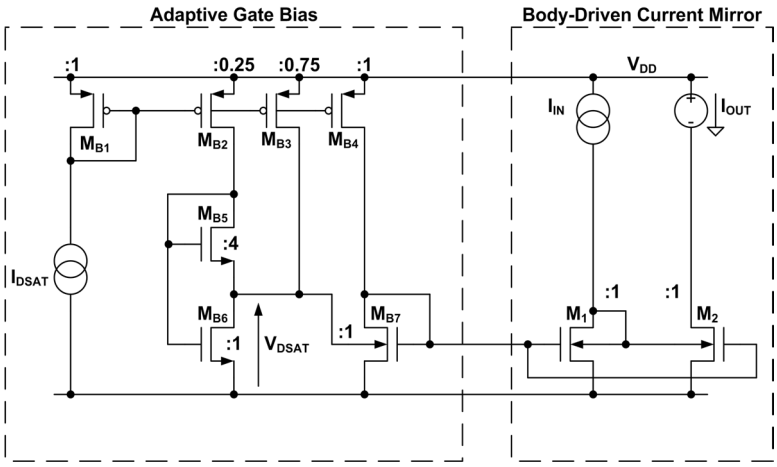

Figure 5.3: One implementation of a body-driven current mirror with adaptive gate biasing [1]

also that the relative device sizes are shown next to each transistor. The operation of this circuit can be understood as follows: The I_{DSAT} current source plus devices M_{B1}, M_{B2}, M_{B3}, M_{B5}, and M_{B6} are used to generate a V_{DSAT} voltage reference; the V_{DSAT} voltage reference is used to forward bias the body of device M_{B7}, which is otherwise connected as a MOS gate-driven diode (V_{GD} = 0 V) and biased at the desired saturation current; the gate voltage of device M_{B7} is used as the adaptive gate bias for the body-driven current mirror M_1, M_2. Now, assuming that M_1 is biased at the saturation current, and noting that it is matched to M_{B7} and biased at the same V_{GS} and I_D as M_{B7}, it must also have the same V_{BS} as M_{B7}, but since the V_{BS} of M_{B7} is equal to V_{DSAT}, the V_{BS} *and* V_{DS} of M_1 must also be equal to V_{DSAT}. Thus, the adaptive gate bias technique allows the designer to guarantee that a body-driven current mirror is operating in saturation at any current level. A functionally equivalent, but improved form of the adaptive gate bias technique is presented in Figure 5.4. The key improvements in the circuit of Figure 5.4 over

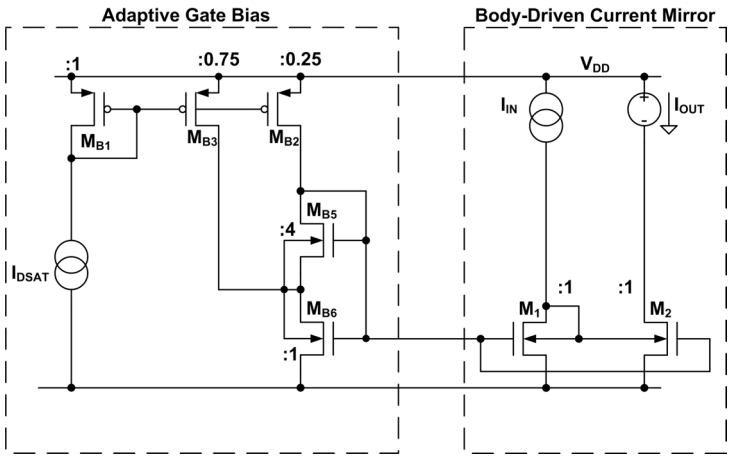

Figure 5.4: An improved implementation of a body-driven current mirror with adaptive gate biasing

Figure 5.3 are that there is one less current branch, so power is saved, and more importantly the drain–source voltages of M_{B6} and M_1 are now equal, so matching is improved. Of course, in this circuit the bodies of the nMOS devices are not tied to the supply rail, which might seem to violate the EKV formulation under which this circuit was derived. However, it is not actually necessary for the body terminals of all nMOS devices to be tied to V_{SS} for Equation 5.10 to be valid. Instead, the only requirement is for all nMOS devices have the *same* body voltage. While it is unusual in CMOS design to bias all nMOS bodies at a voltage other than V_{SS}, it is perfectly valid within the EKV formulation and compatible with PD-SOI technology—thus Equation 5.10 does apply to the circuit of Figure 5.4.

5.2.2.2 Simulation and Measurement Results

To verify that the adaptively biased current mirror functions as intended, the current mirror presented in Figure 5.4 was fabricated on the 3.3-V/0.35-μm PD-SOI process used in

this work. The current mirror devices were sized 8/0.5 M = 4 (total W/L = 32/0.5), and the *m* and *n* factors were both four. Figure 5.5 presents the measured and simulated I_{OUT}–I_{IN} for the adaptive gate bias current mirror. In addition, the simulated I_{OUT}–I_{IN} for the simple current mirror with static gate bias (SCM w/SGB, i.e., Figure 4.1 (a)), cascode current mirror with static gate bias (CCM w/SGB, i.e., Figure 4.2 (a)), simple current mirror with level shift (SCM w/LS, i.e., Figure 4.3 (a)), and the regulated cascode current mirror (RCCM, i.e., Figure 4.4 (a)) are presented. In this test the saturation current and input current were equal to another over the entire sweep for the adaptively biased current mirror. Therefore this plot shows the wide range of bias currents over which the adaptively biased current mirror can operate. When comparing to the other bias schemes, it is clear that adaptive gate biasing provides the optimum wide current dynamic range performance.

However, for high-performance, low-voltage analog design, the linearity of the current transfer characteristic only tells half the story. Equally important is the V_{IN}–I_{IN} characteristic for the current mirror. Figure 5.6 presents the measured and simulated V_{IN}–I_{IN} for the adaptive gate bias current mirror described in Figure 5.4, and also presents the simulated V_{IN}–I_{IN} for the current mirrors already discussed. This plot even more clearly highlights the shortcomings of the prior-art current mirror designs for high-performance analog. Note that while the input device is in saturation (i.e., $V_{DS} \geq 90mV$) over the entire current range for the adaptively biased mirror, the other current mirrors do not enter the saturation region until I_{IN} > 10 μA. For high-performance analog, this is critical because we are typically not interested in building current mirrors *per se*. Instead we are

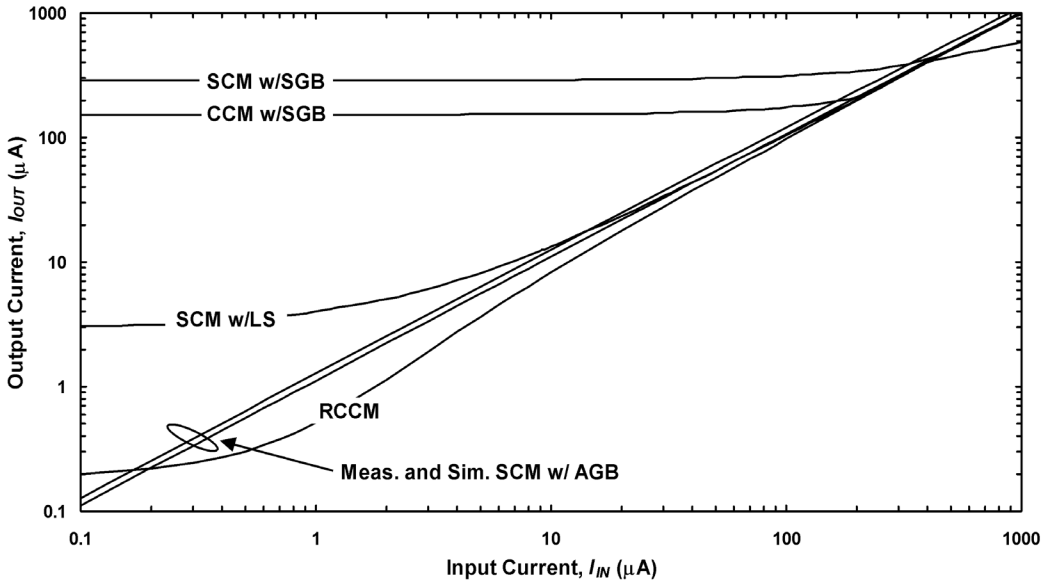

Figure 5.5: Simulated and measured I_{OUT}–I_{IN} for the adaptive gate bias current mirror and comparison to prior-art current mirrors

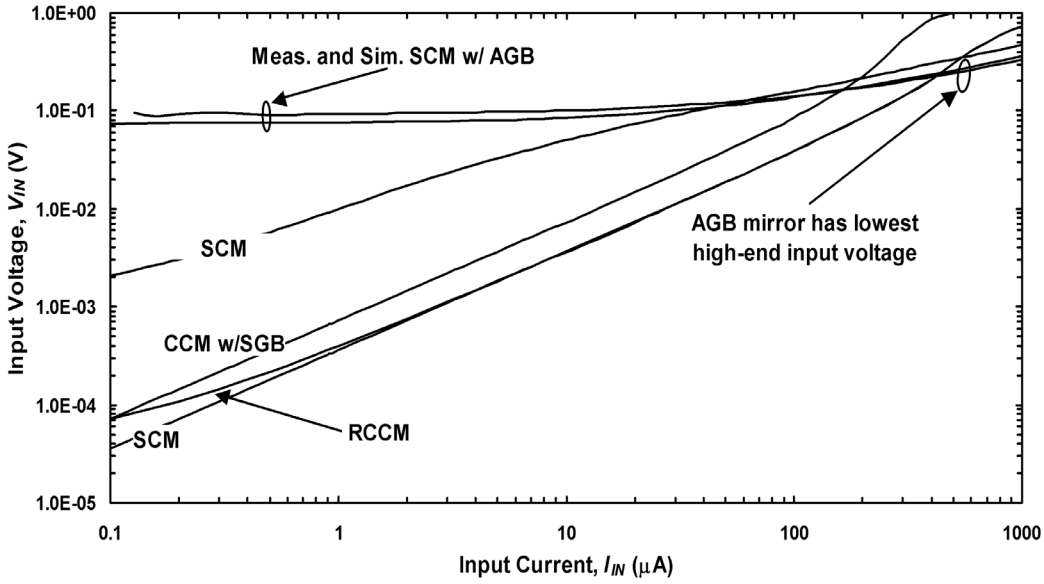

Figure 5.6: Simulated and measured V_{IN}–I_{IN} for the adaptive gate bias current mirror and comparison to prior-art current mirrors

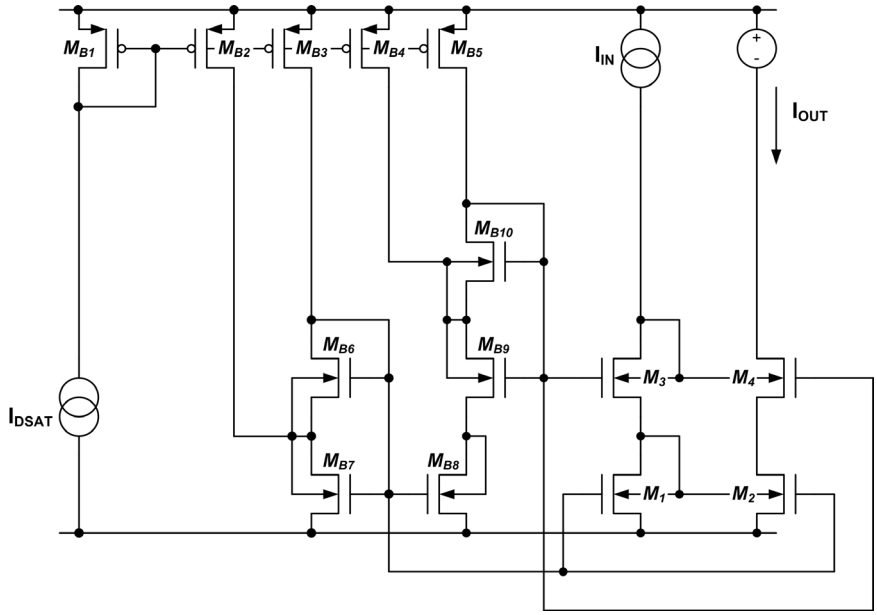

Figure 5.7: Schematic of a body-driven cascode current mirror utilizing adaptive gate biasing

interested in building arrays of high-impedance current sources, which are then used throughout op-amps as tail current sources, high-impedance loads, etc. Thus, the simple current mirror is the building block upon which we build cascode and regulated cascode current sources. However, if one cannot guarantee that the bottom current source device is in saturation, then cascoding will not result in high-impedance current sources.

5.2.3 Body-Driven Cascode Current Mirrors with Adaptive Gate Bias

Now that the adaptive gate bias technique has been presented and shown to be useful for designing wide current dynamic range simple current mirrors, it is straightforward to present the design of higher order current mirrors and current sources. Figure 5.7 presents a schematic of the adaptive gate bias technique applied to a body-driven cascode

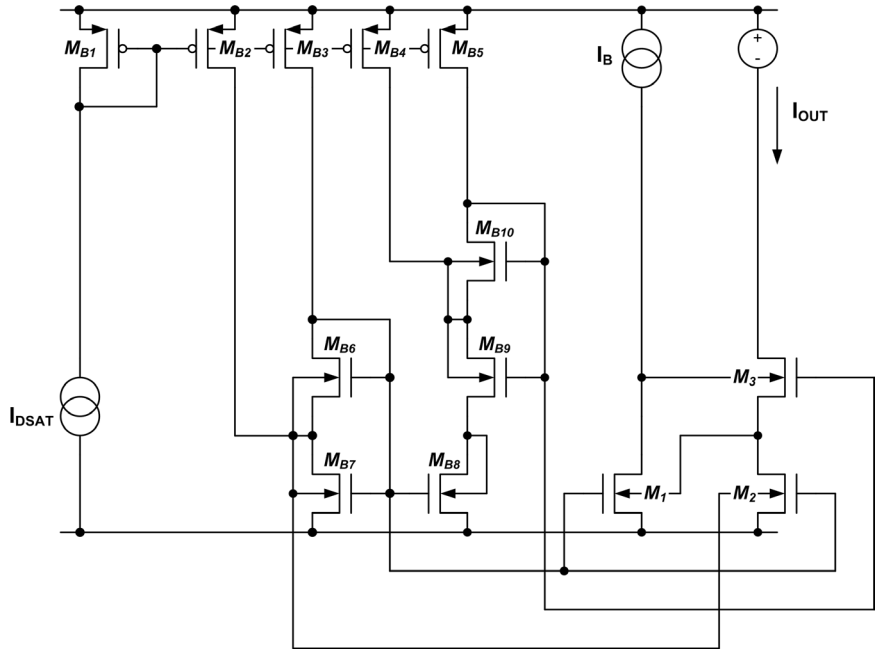

Figure 5.8: Schematic of a body-driven regulated cascode current source utilizing adaptive gate biasing

current mirror. In this circuit devices M_{B2}, M_{B3}, M_{B6}, and M_{B7} are used to generate the gate bias for the mirror devices M_1, M_2, while devices M_{B4}, M_{B5}, M_{B9}, and M_{B10} are simply a copy of the V_{DSAT} extractor used to bias the gates of cascode devices M_3 and M_4. Also included is diode connected device M_{B8} which is used as a level shifter so that devices M_{B9}, M_3 and M_4 all operate from the same source voltage.

Figure 5.8 presents a schematic of a body-driven regulated cascode current source that uses the adaptive gate bias technique. This circuit uses the same transistors for generating the mirror and cascode gate biases, the only differences between this circuit and the simple cascode are in the mirror and output branches. In this case the regulated cascode, consisting of devices M_1, M_2 and M_3, is based directly on the original implementa-

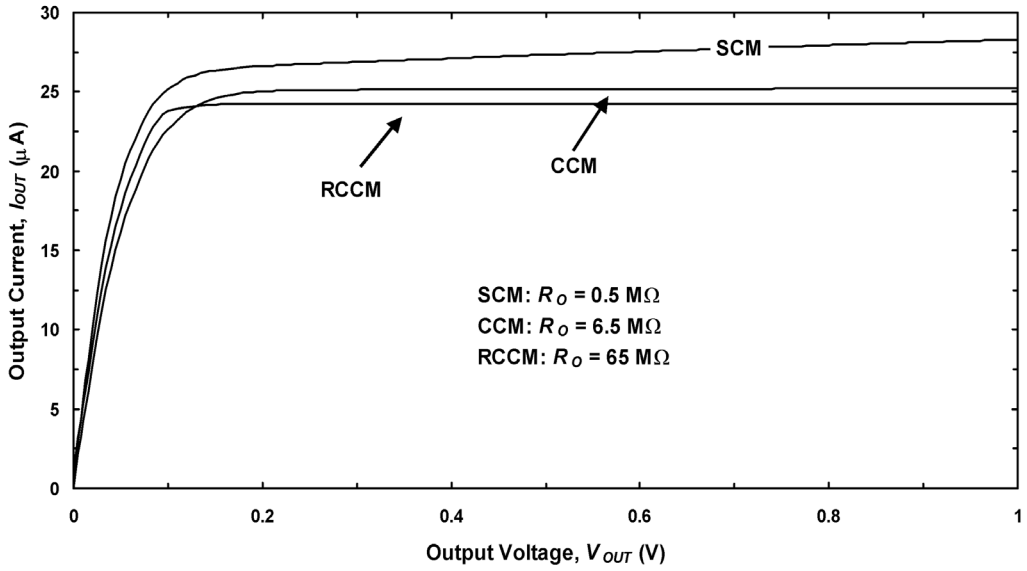

Figure 5.9: Simulated I_{OUT}–V_{OUT} for adaptively biased simple current mirror, cascode current mirror, and regulated current mirror biased at 25 μA

tion of the gate-driven regulated cascode [46]. The major difference between gate-driven and body-driven regulated cascode is the loop-gain (and therefore the impedance boost) of the body-driven circuit is reduced by a factor η^2 with respect to the gate-driven circuit. Figure 5.9 presents the simulated I_{OUT}–V_{OUT} at I_{DSAT} = I_{IN} = 25 μA for the adaptively biased simple current mirror, cascode current mirror, and regulated cascode current mirror. The simulated output resistance for the three current mirrors is 0.5 MΩ for the simple current mirror, 6.5 MΩ for the cascode current mirror, and 65 MΩ for the regulated cascode current mirror. Note also that there is a systematic offset for the regulated cascode current mirror. This is due to the V_{DS} mismatch between devices M_1 and M_{B7} in Figure 5.8. Unfortunately, the circuit performs much better if device M_1 is not cascoded (this effect will be described in detail in Section 5.4), so the systematic offset is something that must be tolerated.

5.3 Design and Measurement of Op-Amp I

5.3.1 Design Goals

While the fundamental contribution of this research is the development of the adaptive gate bias technique, it is necessary to apply adaptive gate biasing to the design of a complete op-amp to prove that it is a valid and useful design technique. However, since there were no target specifications and no intended applications for this body-driven amplifier, one must choose a somewhat arbitrary set of design goals. Therefore the goals set for this op-amp are as follows:

- to develop a body-driven op-amp whose performance far exceeds that of previously reported body-driven amplifiers, and in particular to achieve a high open-loop DC gain and wide unity-gain bandwidth,
- use to as high a degree as possible body-driven circuit primitives, including differential pair(s), current mirror(s), and regulated cascode current source(s),
- develop an op-amp that is useful for a wide array of applications by meeting performance goals over a wide input common-mode range and power supply range, and
- to use body-driven design techniques in a way that improves upon what can be achieved using standard gate-driven techniques at low voltages.

The first step then in this design process was to examine previously reported low-voltage circuit designs that use standard design techniques and see how they can be

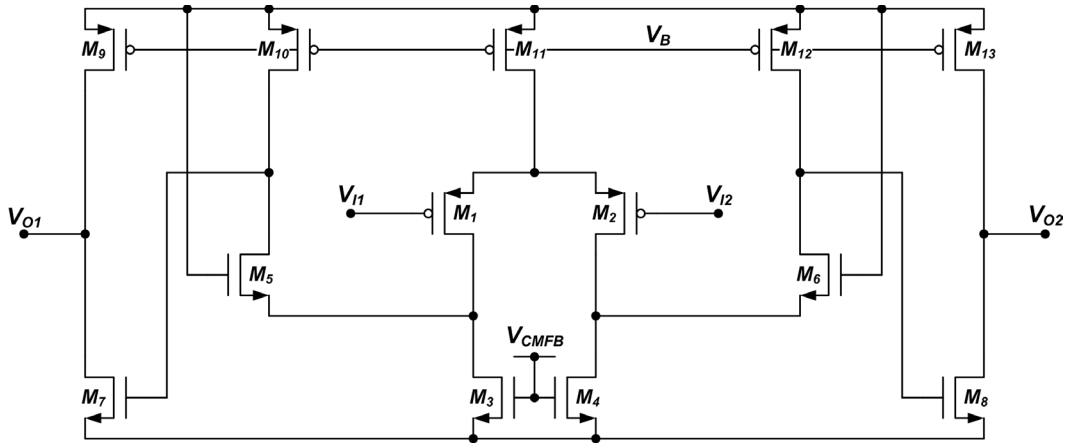

Figure 5.10: Example of a 1-V gate-driven op-amp [47]

improved with body-driven transistors. Figure 5.10 presents a schematic of a 1-V op-amp intended for use in a switched-capacitor circuit which was designed using standard gate-driven techniques [47]. Looking at this schematic, one can see at least two places where gate-driven transistors could be replaced with body-driven transistors to improve performance.

- The differential pair (M_1, M_2) cannot sense V_{MID}. Instead the op-amp is operated with a common-mode level of V_{SS}, and the feedback capacitors are pre-charged to shift the output common mode level to V_{MID}. Replacing M_1 and M_2 with a body-driven differential pair would improve performance by allowing the op-amp to operate with an input and output common-mode level of V_{MID}, thus simplifying the system-level design.

- The pMOS devices (M_{10}, M_{12}) limit the impedance at the output of the first gain stage, and therefore limit the gain of the op-amp. Replacing these devices with pMOS body-driven regulated cascode current sources would significantly improve the open-loop voltage gain.

The next step is, of course, to design a body-driven op-amp which makes use of the new design techniques. Towards this end, a body-driven operational amplifier was designed, laid out, and submitted for fabrication in January of 2004. The process used was the Honeywell 3.3-V/0.35-μm PD-SOI process which has been previously discussed. The name of the test chip was Macedonia.

5.3.2 Op-Amp Design

5.3.2.1 Op-Amp Schematics

For the circuit designer, one of the greatest advantages of body driving with adaptive gate biasing is that it enables the construction of standard circuit primitives (e.g., cascode current mirrors and regulated cascode current sources) that are low-voltage compatible. This means that low-voltage circuit designs can use standard design techniques, the only difference is that body-driven circuit primitives will replace gate-driven circuit primitives. Figure 5.11 presents the schematic of the core Macedonia amplifier. The lines shown on the top and bottom of the schematic represent the voltage-bias lines for the amplifier, which are generated using a second circuit called the bias voltage generator. The bias generator sets all the important gate and body bias voltages, *as per* the adaptive gate bias technique previously discussed. The schematic of the voltage bias genera-

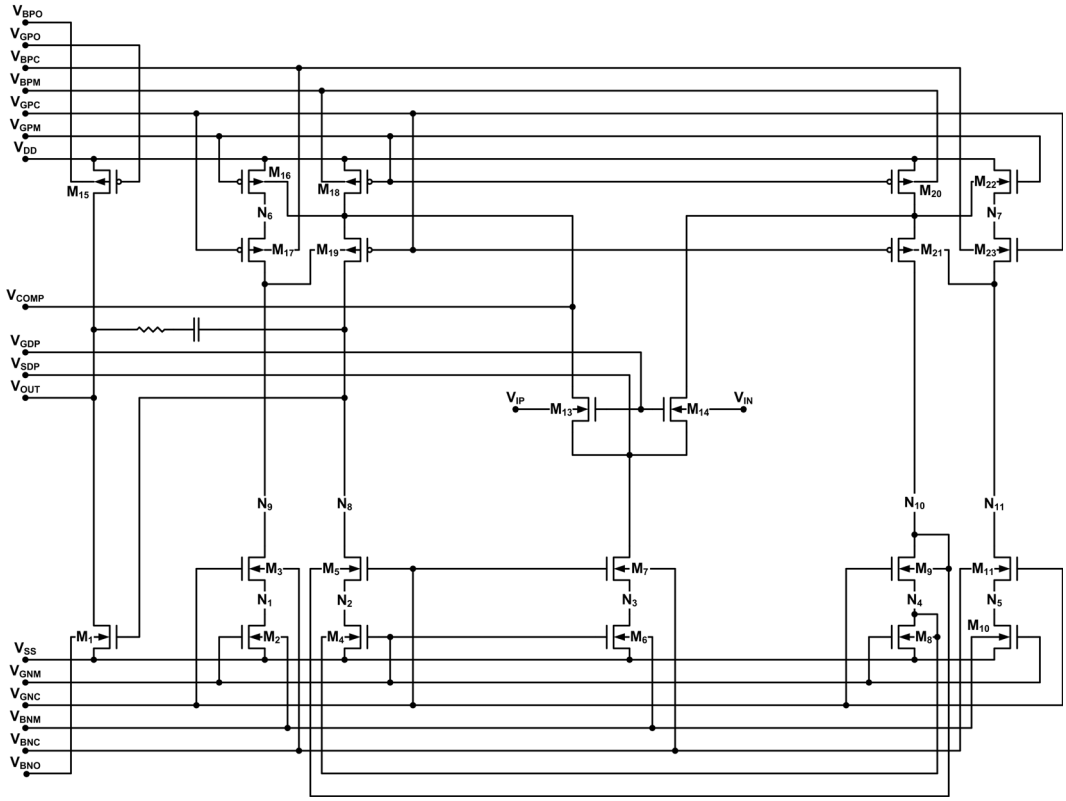

Figure 5.11: Schematic of the core amplifier from the Macedonia chip

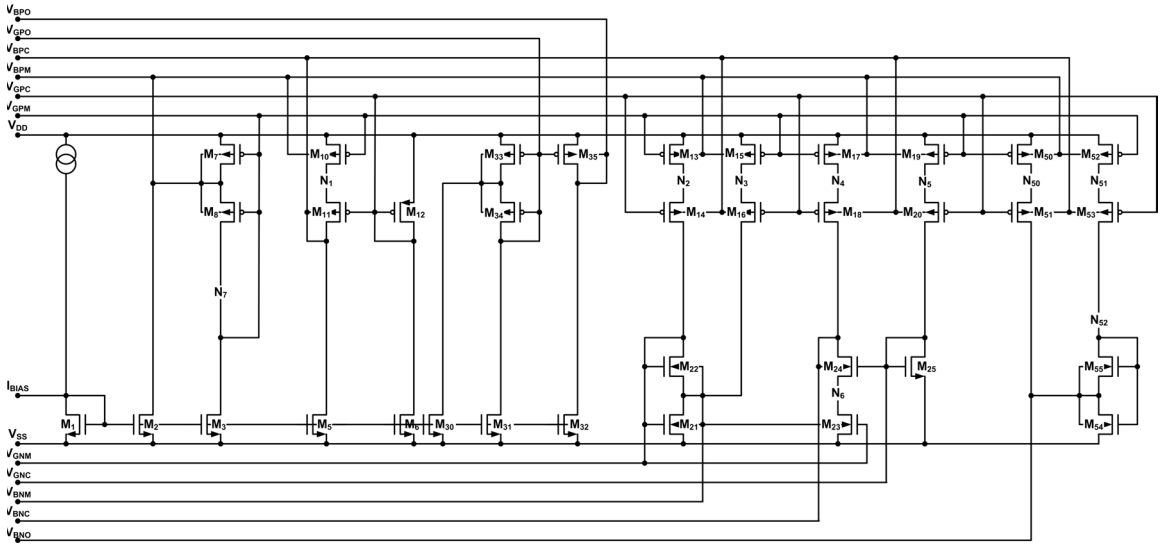

Figure 5.12: Schematic of the voltage bias generator from the Macedonia chip

tor is presented in Figure 5.12, it requires only one 25-μA input bias current to generate all of the necessary bias voltages.

Within the core amplifier, there are several things to note

- nMOS body-driven differential pair uses a tracking gate bias (not shown), similar to Figure 4.10 (a),
- op-amp uses a standard folded cascode architecture for wide ICMR,
- pMOS regulated cascode current sources comprised of devices M_{16}–M_{19} and M_{20}–M_{23} are used for high-gain,

- body-driven cascode current mirror comprised of devices M_4, M_5, M_8, and M_9 is used to perform differential to singled-ended conversion, and

- devices M_1 and M_{15} form a class-A output stage.

5.3.2.2 Unity-Gain Bandwidth and DC Open-Loop Gain

Two of the most important specifications for an op-amp are the unity-gain bandwidth and low-frequency open-loop voltage gain. Achieving a given bandwidth using a body-driven op-amp is straightforward (assuming the devices have adequate f_T), as it is determined by only two parameters, the transconductance of the input pair and the Miller capacitance

$$UGBW = \frac{g_{mb(13,\,14)}}{2\pi C_m}. \tag{5.11}$$

In this design the Miller capacitor was 10 pF, the tail current was 200 μA, and the g_{mb} of the input pair was approximately 600 μmho, for a unity-gain bandwidth of 10 MHz.

On the other hand, achieving high open-loop voltage gain at low supply voltages is very challenging for reasons that are entirely unrelated to body driving. The open-loop voltage gain of this amplifier is approximately given by

$$A_{OL} \approx \{g_{mb(13,\,14)} \cdot r_{o19} g_{m19} r_{o18} \cdot (1 + \eta^2 g_{m16} r_{o17} r_{o16})\} \cdot \{g_{m1} \cdot r_{o1} \parallel r_{o15}\}. \tag{5.12}$$

In Equation 5.12 the first bracketed term describes the gain of the first stage, that is, the gain from the body terminals of the input devices to the gate terminal of device M_1. The

first-stage gain is roughly equal to the transconductance of the input devices multiplied by the impedance seen looking back from the gate of M_1, while this impedance is equal to the output impedance of the regulated pMOS current source (M_{18}, M_{19} plus regulation amplifier) in parallel with the output impedance of the nMOS non-regulated cascode current source (M_4, M_5). However, in Equation 5.12 only the output impedance terms of the pMOS current sources are listed because the output impedance of the pMOS current sources is so much lower than the nMOS that they always dominate the output impedance seen looking back from the gate of M_1.

The low output impedance of the pMOS current sources is actually not due to the fact that they are pMOS devices, but is instead due to the available headroom on the pMOS current sources. To understand this problem, it is helpful to recall the concept of open-circuit voltage for a generalized current source. Open-circuit voltage is the theoretical voltage that one would measure at the output of a current source, if its output terminal could be open circuited but the current source still remain in the small-signal regime. For a single MOSFET, the open-circuit voltage is equal to the Early voltage, while for a general current source the open-circuit voltage is equal to

$$V_{OC} = I_{OUT}R_{OUT}, \tag{5.13}$$

where I_{OUT} is the large-signal bias current and R_{OUT} is the small-signal output resistance. Using the open-circuit voltage, we can re-write the gain equation for a standard

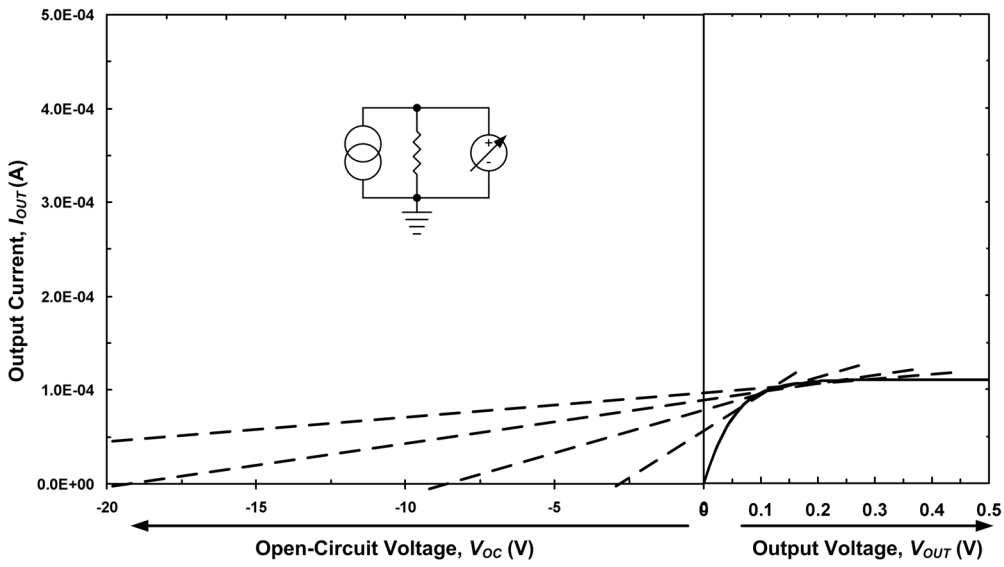

Figure 5.13: I_{OUT}–V_{OUT} transfer function for a generalized current source, and tangent lines showing the approximate open-circuit voltage

transistor amplifier as (considering only magnitude)

$$A_V = g_m R_{OUT} = \frac{g_m}{I_D} \cdot I_D R_{OUT} = \frac{g_m}{I_D} \cdot V_{OC}. \tag{5.14}$$

Thus, one reason that open-circuit voltage is a useful concept is that it allows gain equations to be written in a way that is independent of the bias current level. Second, open-circuit voltage is a useful way of graphically illustrating the effect of power supply voltage on voltage gain. Figure 5.13 presents the I_{OUT}–V_{OUT} transfer function of a generalized current source, along with superimposed tangent lines showing the approximate open-circuit voltage as a function output voltage. Considering Equation 5.14 in light of Figure 5.13, it is clear that maximizing the output voltage across a current source (or at least biasing a current source well into the saturation region) is critical for achieving high-voltage gains. With this thought in mind, one can now see why the pMOS current sources

limit the voltage gain in the body-driven amplifier. Looking again at the schematic of the body-driven amplifier, Figure 5.11, note that the total voltage across the pMOS regulated cascode current source (M_{18}, M_{19} plus regulation amplifier) is given by

$$V_{TOT} = V_{DD} - V_{GS1}, \tag{5.15}$$

which could be less than 300 mV assuming a power supply voltage of 1 V and an nMOS threshold voltage of 0.65 V. On the other hand, the nMOS current source consisting of devices M_4 and M_5 will be biased with a total output voltage of V_{GS1}, which is probably close to 700 mV—well into the saturation region.

From the above discussion, it is clear why low-voltage amplifiers have such poor voltage gain. This also explains why it is critical to be able to construct regulated cascode current sources at low voltages. In addition, it was found that there are other ways to use body driving to improve voltage gain. One simple but extremely effective technique that was discovered was to forward bias the body–source voltage of device M_1. With a positive V_{BS} for device M_1, the total voltage across the pMOS current source is given by

$$V_{TOT} = V_{DD} - V_{GSN1}\Big|_{V_{BS1}=0} + \eta V_{BS1}. \tag{5.16}$$

Based on Equation 5.16, it was decided to forward bias the body voltage of device M_1 by approximately 300 mV, which it has already been shown is within the safe operating area over all temperatures. The 300-mV bias voltage was conveniently available as the body bias voltage used for the cascode nMOS transistors, which is equal to $2V_{DSAT}$, or

approximately 300 mV for transistors biased at the middle of moderate inversion. Using this technique simulations showed that it was possible to increase the gain by more than 20 dB.

5.3.2.3 Op-Amp Layout

Another important difference between gate-driven and body-driven circuits is the layout style. When designing low-voltage circuits that must simultaneously exhibit high operating speeds and low power dissipation, it is generally necessary bias one's transistors in moderate inversion with large bias currents. Of course, this means that the transistors must be very wide, in order to be moderately inverted at the high bias current level. As an example, consider an nMOS transistor biased at I_D = 100 μA and IC = 1 with a channel length of 0.5 μm (this is in fact the bias condition used for the differential pair devices M_{13}, M_{14}). For the 3.3-V/0.35-μm process used in this work, this bias condition would necessitate a transistor with a gate width of [10]

$$W = L \cdot \frac{I_D}{IC \cdot I_0} = 0.5\mu m \cdot \frac{100\mu A}{1 \cdot 350 nA} \approx \underline{143\mu m} \; . \tag{5.17}$$

In bulk CMOS, a transistor with a total gate width of 143 μm could be fabricated using four parallel fingers of approximately 36 μm each. However, for the 0.35-μm PD-SOI process used in this work, the maximum gate width is limited by body resistance to less than 10 μm for nMOS transistors. Thus in SOI this transistor would have to be drawn with 14 gate fingers!

If one wanted to match an array of several transistors, the width of this array would be much larger than its height. As an example, assume that one wants to match an array of four such transistors and that the source/drain contact width is 1.5 μm. In this case the height of the array would be 10 μm (i.e., the “height” of the array is gate width of one transistor), while the width of the array would be

$$Width = (4) \cdot (14) \cdot (0.5\mu m + 1.5\mu m) = \underline{112\mu m}, \tag{5.18}$$

or an aspect ratio of 1:11.2. This is in contrast to the four-finger bulk CMOS case, where a four transistor array would have a height of 36 μm and a width of

$$Width = (4) \cdot (4) \cdot (0.5\mu m + 1.5\mu m) = \underline{32\mu m}, \tag{5.19}$$

or an aspect ratio of 1:0.88—nearly a perfect square.

When trying to match an array of transistors, it is standard practice to use a common-centroid structure to minimize the effect of process gradients. However, common centroid only cancels linear process gradients, while gradients will only be linear over finite distances. Generally speaking, it is a good rule to layout a set of matching transistors such that the complete set has an aspect ratio very close to unity. This minimizes the distance of any transistor to the common centroid, and thus maximizes the likelihood of true, linear process gradients. Therefore using a standard one-dimensional layout structure, it seems that SOI body-driven transistors will have much worse matching than their bulk CMOS counterparts. To solve this problem, a two-dimensional, single-body PD-SOI

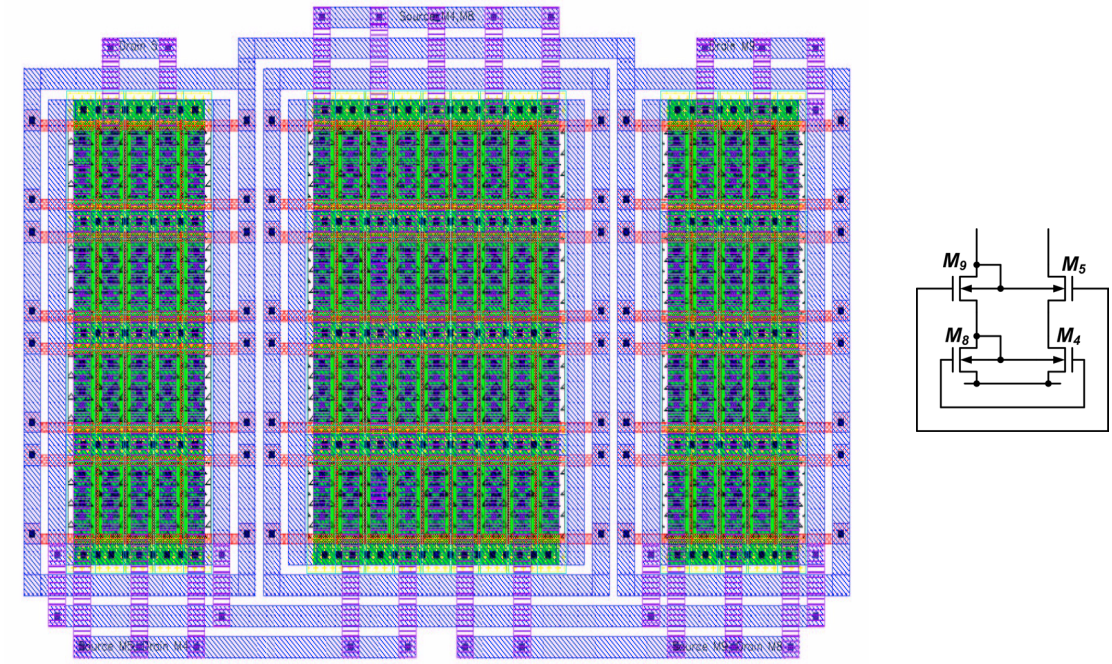

Figure 5.14: Layout and schematic of a body-driven cascode current mirror

layout structure was developed. An example of this layout structure applied to a body-driven cascode current mirror is presented in Figure 5.14. In this structure H-gate fingers are arrayed both vertically and horizontally. In the layout shown in Figure 5.14 the group of transistors in the middle are the mirror devices M_4, M_8. Horizontally, these transistors are laid out in a standard common-centroid $AABB|BBAA$; vertically, each transistor is continuous, with its body "tapped" every 10 μm. Having a body contact every 10 μm limits the body resistance and improves performance, while arraying the transistors vertically and horizontally helps optimize the aspect ratio of a given group of transistors and thus improves matching. The layout of the complete Macedonia amplifier is shown in Figure 5.15 and measures 800 μm X 350 μm.

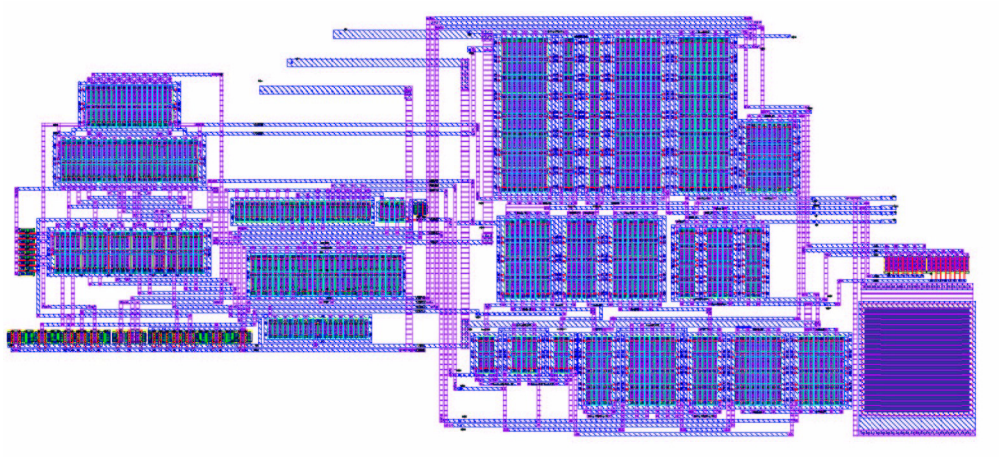

Figure 5.15: Layout of the complete Macedonia amplifier (dimensions are 800 μm X 350 μm)

5.3.3 Measurement Results

The Macedonia op-amp was received in May 2004 and was tested during the summer of 2004. The test results from the Macedonia op-amp were mixed. While the primary goals of achieving a high open-loop voltage gain and wide bandwidth were achieved, the amplifier displayed poor power supply and common-mode rejection, which calls into question its usefulness as a general purpose op-amp. Though a range of tests were run on the op-amp, only four will be presented in this section—open-loop gain, bandwidth, power-supply rejection ratio (PSRR), and common-mode rejection ratio (CMRR)—which together highlight the most important aspects of the amplifier's performance. The test setups used for these measurements are described in Appendix A.

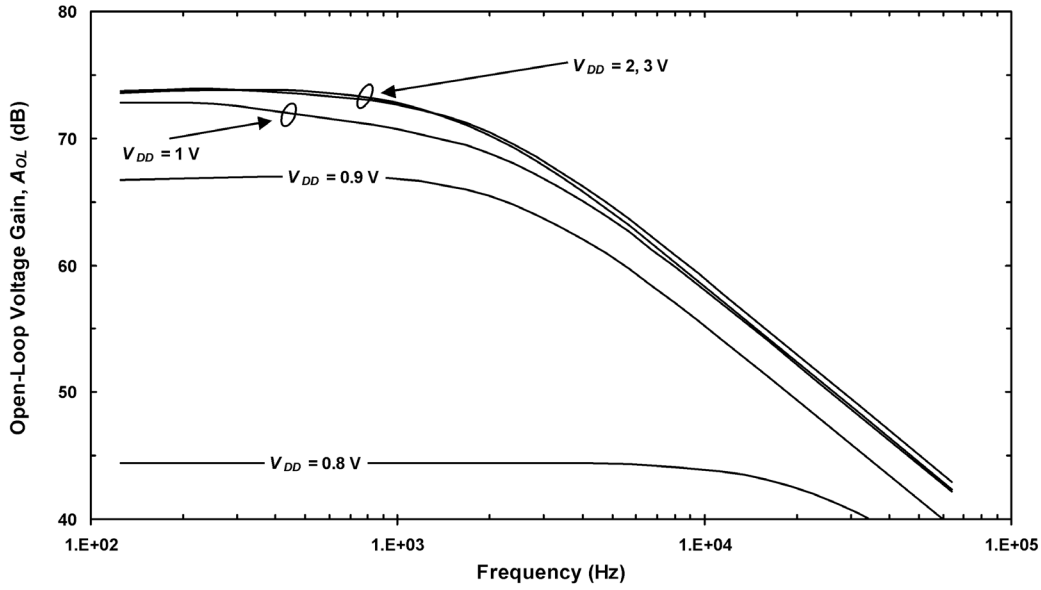

Figure 5.16: Measured open-loop gain (typical) versus frequency at several different operating voltages for the Macedonia amplifier

5.3.3.1 Open-Loop Gain

Figure 5.16 presents the measured open-loop voltage gain as a function of frequency for the Macedonia amplifier at V_{DD} values of 0.8 V, 0.9 V, 1.0 V, 2.0 V, and 3.0 V. The frequency sweep in this measurement starts at 125 Hz, which is well below the corner frequency, and goes to almost 100 kHz. The high-frequency limitation is imposed by the SR770 FFT network analyzer used for this measurement. However, this measurement is useful because it clearly shows the low-frequency gain and corner frequency of the amplifier, while step response measurements will show the unity-gain bandwidth.

The data presented in Figure 5.16 shows at least two important points about the amplifier's performance. First, note that the gain increases significantly in going from 0.8-V to

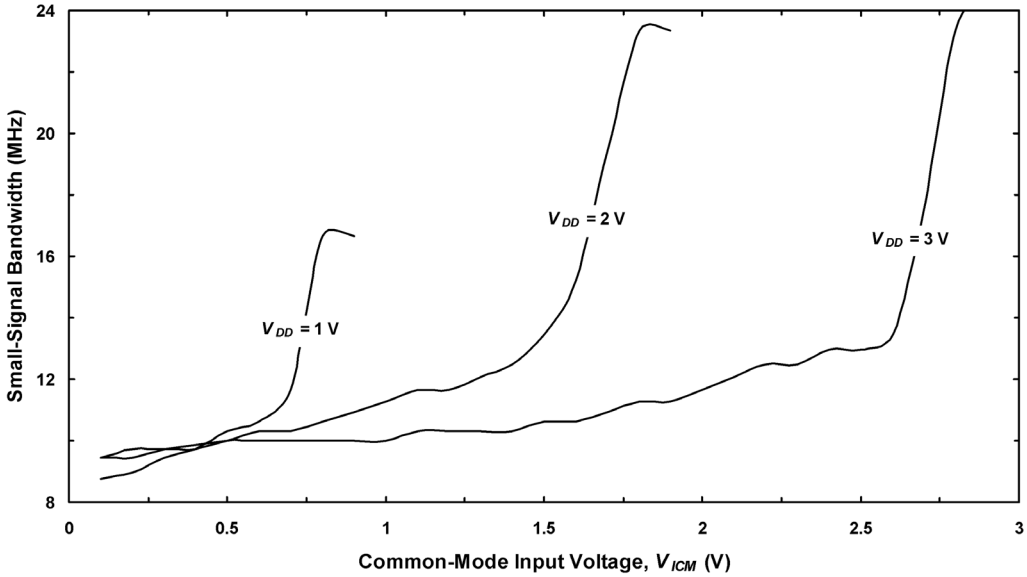

Figure 5.17: Measured unity-gain bandwidth (typical) versus common-mode input at V_{DD} = 1 V, 2 V, and 3 V for the Macedonia amplifier

1.0-V V_{DD}, while in going from 1.0 V to 3.0 V the gain increases by only a few dB. This shows that the amplifier achieves near constant gain over the V_{DD} range 1–3 V, and so the amplifier is working well at 1-V V_{DD}. Second, this plot shows that the amplifier achieves a roughly 75-dB open-loop voltage gain at 1-V V_{DD}. Therefore the amplifier meets the goal of high open-loop voltage gain.

5.3.3.2 Bandwidth

Figure 5.17 presents the measured unity-gain bandwidth versus common-mode input at V_{DD} = 1 V, 2 V, and 3 V for the Macedonia amplifier. Again there are several important aspects of the amplifier's performance that can be understood from this plot. First, notice that at low V_{ICM} the unity-gain bandwidth is close to 10 MHz, which is the target value.

Second, notice that for each curve the bandwidth is roughly constant with V_{ICM} until the common-mode input voltage gets within 0.5 V of the upper supply rail. Once V_{ICM} is within 0.5 V of V_{DD} the bandwidth becomes highly sensitive to common-mode level and in fact doubles over the input range $V_{DD} - 0.5 < V_{ICM} < V_{DD}$. This bandwidth increase is due to the action of the tracking gate bias used for the differential pair. Specifically, the gates of the differential pair devices track the common-source of the differential pair via a pMOS source follower. However, once the common-mode input gets within 0.5 V of V_{DD}, the gate terminals of the differential pair devices reach V_{DD} and can no longer track the common-mode input. When this happens the V_{BS} of the input pair devices increases with common-mode level, which causes the increase in g_{mb} with common-mode input. Note that this same effect was described in Section 4.3.3 and Figure 4.10.

5.3.3.3 PSRR

Unlike open-loop gain and bandwidth, which are universally considered op-amp parameters of first-order importance, PSRR is considered a second-order parameter for many applications. It is questionable then how important it is to characterize PSRR in this research, since the op-amp is not intended for a specific application. However, the measured PSRR for the Macedonia amplifier was extremely low, between 20 and 40 dB depending on the V_{DD} level, and so it must be considered. Furthermore, the reasons for the very low PSRR highlight an important aspect of body-driven circuit design, which makes PSRR an important parameter to study. Figure 5.18 presents the measured offset voltage versus power supply voltage for a typical Macedonia amplifier. Noting that it is shown in Appendix A.2 that PSRR is the inverse derivative of offset voltage with

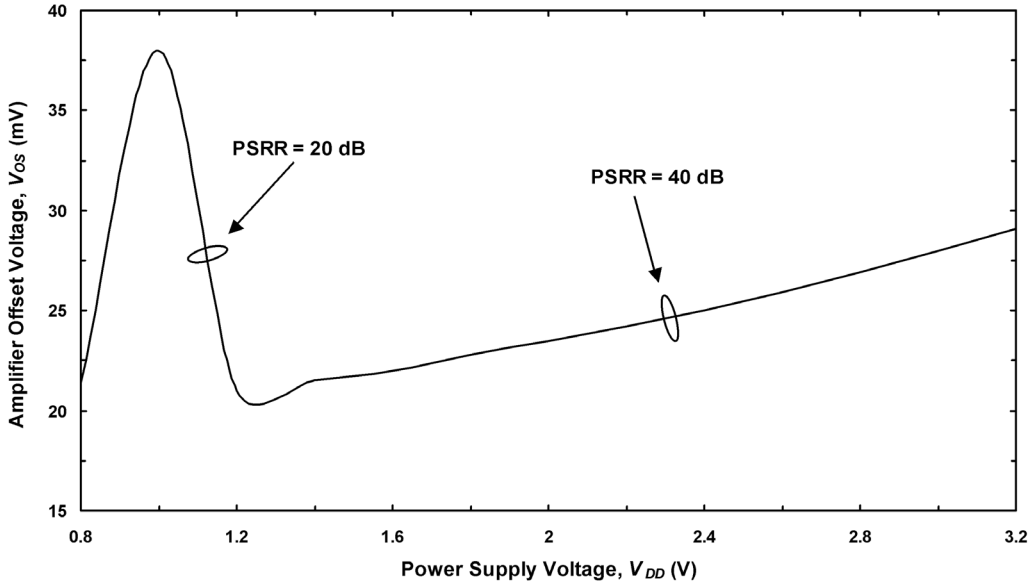

Figure 5.18: Measured offset voltage versus power supply voltage for the Macedonia amplifier

respect to power supply voltage, Figure 5.18 shows that the Macedonia amplifier has a very low power supply rejection. Specifically, the PSRR is roughly 20 dB over the V_{DD} range 1–1.2 V, while it is close to 40 dB over the V_{DD} range 1.2–3.2 V. While there is no specification for PSRR in this project, it is hoped that this amplifier will be useful for a broad range of analog applications. Unfortunately, the very low PSRR makes the amplifier unusable for many applications, especially at 1-V V_{DD}. The causes of the low PSRR, and solutions for improving it, will be studied in detail in Section 5.4.

5.3.3.4 CMRR

Like PSRR, low-frequency CMRR is determined primarily by random mismatches among groups of transistors (e.g., differential pair or current mirror) in an amplifier. Therefore considering that the PSRR for this amplifier is low, it seems logical that the CMRR will

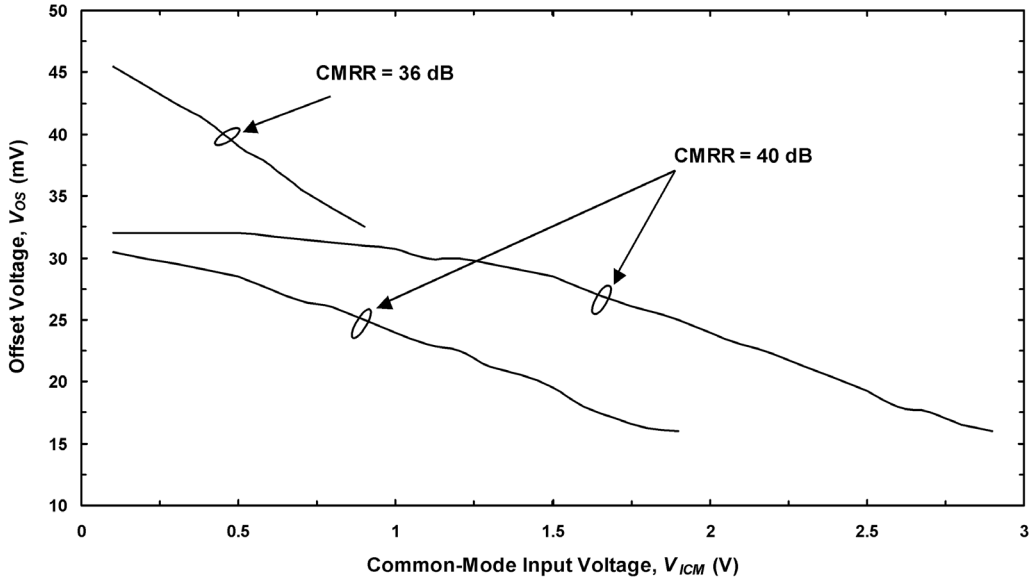

Figure 5.19: Measured offset voltage versus common-mode voltage with V_{DD} = 1 V, 2 V, and 3 V for the Macedonia amplifier

also be low. Figure 5.19 presents the measured offset voltage versus common-mode voltage for a typical Macedonia amplifier. As expected, this amplifier shows a high sensitivity to common-mode input. At 1-V V_{DD} the CMRR is only 36 dB, while at 2- and 3-V V_{DD} the CMRR is roughly 40 dB. Typically one would like to have at least 60 dB CMRR, so again something needs to be done to improve this problem. Fortunately, it is likely that the poor PSRR and CMRR have a common progenitor, and so fixing one should fix the other.

5.3.4 Conclusion

It was stated at the beginning of this section that a primary goal for this design was to develop a body-driven amplifier whose performance far exceeds that of previously reported body-driven amplifiers. Comparing the bandwidth and open-loop gain of the

Macedonia amplifier (75 dB/10 MHz) to the Blalock amplifier (48 dB/1.3 MHz) [40] and the Stockstad amplifier (70–79 dB/5.6 kHz) [41], it is clear that this amplifier does outperform the others in terms of gain and bandwidth. However, it is also important that this research develop a body-driven amplifier that is useful for a wide variety of applications. On this point it seems that the Macedonia amplifier has failed. The extremely low PSRR and CMRR will preclude this amplifier from being used in a number of applications. It is therefore a necessary component of this research to investigate the problems exhibited by the Macedonia amplifier, and if possible to solve them.

5.4 Design and Measurement of Op-Amp II

Regarding the PSRR and CMRR of the Macedonia amplifier, the key question that must be answered is, “Is the effect due to a problem in the design, or is it a fundamental consequence of designing circuits with body-driven transistors?” To answer this question a detailed study of the PSRR and CMRR of the Macedonia amplifier, including the use of Monte Carlo analysis techniques, was undertaken. From this analysis it was determined that the problem was in fact a consequence of the circuit topology chosen, and could be significantly improved with design modifications. To prove this hypothesis a second body-driven op-amp called Mysia was sent for fabrication in July 2004.

5.4.1 Op-Amp Design

5.4.1.1 Monte Carlo Analysis of PSRR

After observing the poor PSRR of the Macedonia amplifier, the first step taken was to simulate the PSRR to see if the root cause of the problem could be uncovered. Figure

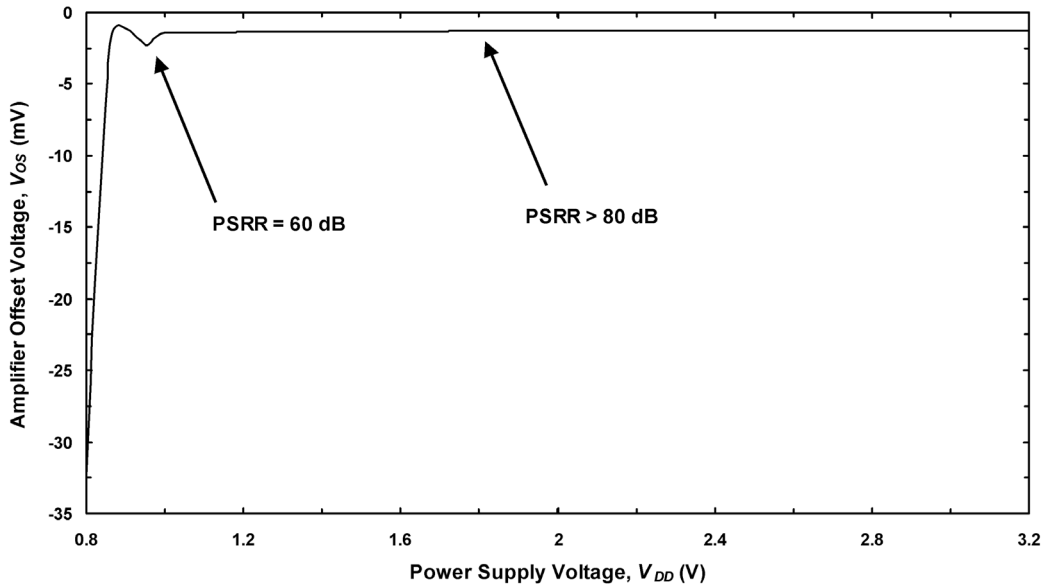

Figure 5.20: Simulated offset voltage versus power supply voltage for the Macedonia amplifier (does not include device mismatch)

5.20 presents the simulated offset voltage versus power supply voltage for the Macedonia amplifier. This simulation does not include random mismatch effects and also shows that Macedonia should have a very high PSRR. Since this simulation obviously sheds no light on the PSRR problem, it was decided to re-simulate the PSRR, but this time to include random threshold mismatch effects through the use of a Monte Carlo simulation. Monte Carlo analysis in this case simply means a circuit is simulated a certain number of times (say 200), and that in each simulation a parameter or set of parameters is chosen randomly, though over the entire set of simulations the random variation of this parameter will conform to a user-defined distribution (e.g., Gaussian). For the PSRR simulation the random parameter was transistor threshold voltage. Though all SPICE simulators can perform Monte Carlo analysis, it should be noted that proper modeling of MOSFET threshold mismatch is model dependent. EKV uses a physically realistic model

which describes the standard deviation of threshold mismatch as a user-defined parameter divided by the square root of the gate area of the transistor, or

$$\sigma_{V_{TH}} = \frac{A_{V_{TH}}}{\sqrt{M \cdot W \cdot L}}, \tag{5.20}$$

where $A_{V_{TH}}$ is a user-defined, technology-dependent mismatch parameter. This is in contrast to BSIM3V3, which cannot model area-dependent mismatch without the addition of a sub-circuit for each transistor.

A value of $15 \cdot 10^{-9} V \cdot m$ was chosen for $A_{V_{TH}}$, which is the same value used in the generic 0.5-μm EKV model available on the web [30]. Since, at the time of the Macedonia testing and Mysia design, only one Macedonia amplifier was available for characterization, it was not possible to choose a value for $A_{V_{TH}}$ based on measurement. Therefore the typical PSRR value for the Mysia amplifier could not be precisely predicted using Monte Carlo analysis. However, by using the same $A_{V_{TH}}$ to analyze the Macedonia amplifier and throughout Mysia design process, it was possible to show that the Mysia amplifier should have much better PSRR than the Macedonia amplifier, which was proven by subsequent measurement results.

Figure 5.21 presents the results of 200 runs from a Monte Carlo simulation of the Macedonia amplifier PSRR at V_{DD} = 1 V and 1.5 V. At 1-V V_{DD} this simulation shows an average PSRR of 27 dB, which is close to the measured value of 20 dB. Likewise at 1.5-V

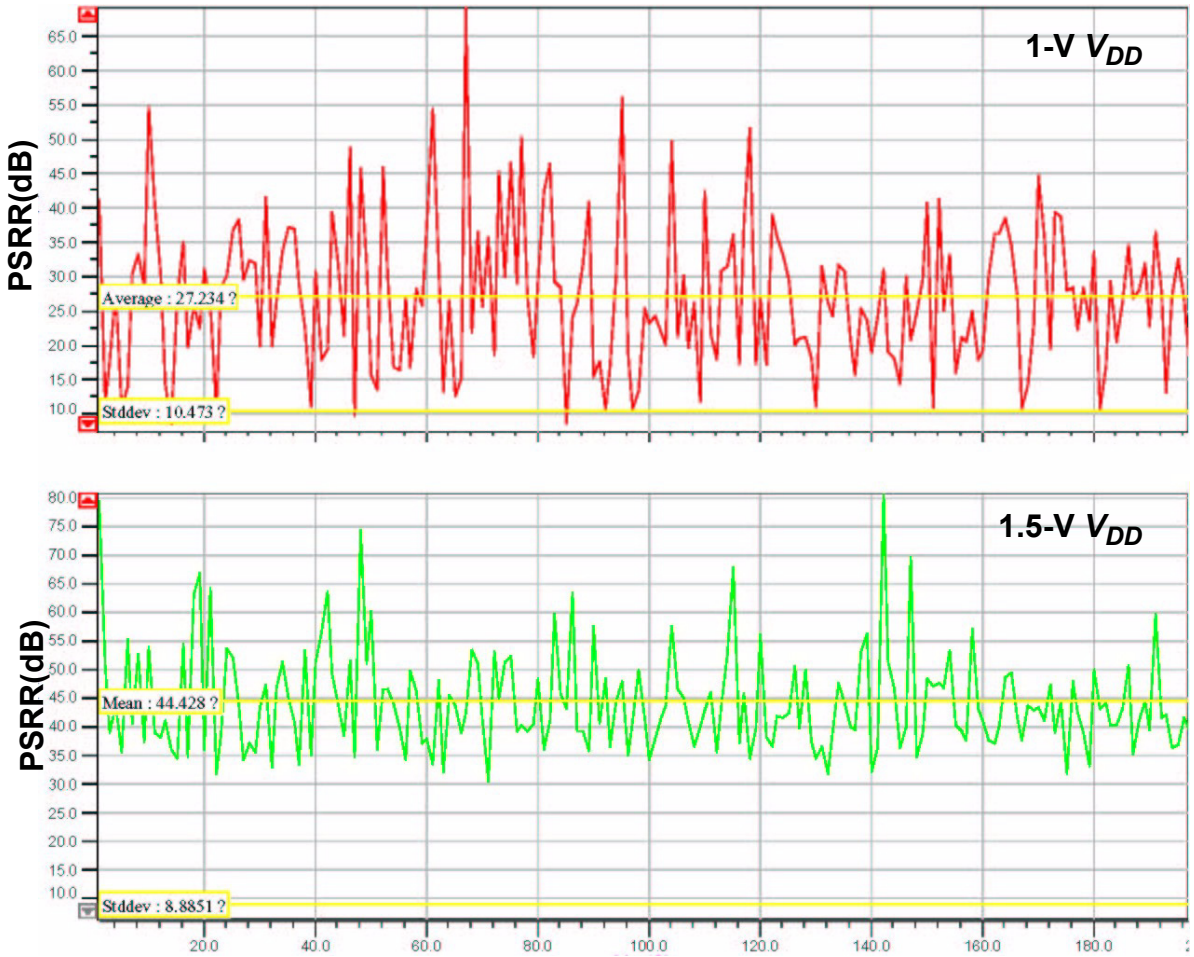

Figure 5.21: Monte Carlo simulation (200 permutations) of the Macedonia op-amp predicting PSRR at V_{DD} = 1 V and V_{DD} = 1.5 V

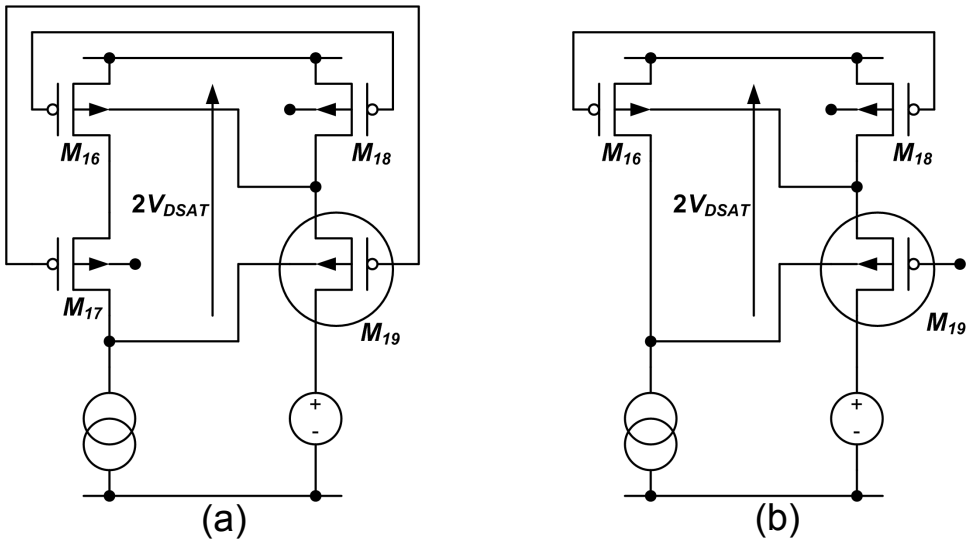

Figure 5.22: Schematic showing (a) the problem and (b) the solution for the body-driven regulated cascode current mirror

V_{DD} the simulation shows an average PSRR of 44 dB, which is very close to the measured value of 46 dB. This Monte Carlo simulation clearly shows that the PSRR problem is due to random mismatch effects. Once the problem was found, the next step was to try and isolate the devices or sets of devices which had the biggest impact on PSRR. The basic method for isolating the problem devices was to apply mismatch effects to only a few devices at a time, and then see which devices caused the greatest reduction in PSRR. The results of this study will be discussed in the following sections.

5.4.1.2 pMOS Regulated Cascode Current Sources

Figure 5.22 (a) presents one of the key problems that was discovered during the Monte Carlo simulations. The schematic on the left is an example of a pMOS regulated cascode current source used in the Macedonia amplifier. Note that in this configuration the total voltage across devices M_{16} and M_{17} is $2V_{DSAT}$, or each of these devices is biased just at

the edge of saturation. Now consider what would happen if device M_{19} had a threshold voltage that was 10 mV larger than it should be; that is, assume that the gate voltage of device M_{19} was 10 mV lower than it should be. To maintain the proper V_{DS} on device M_{18}, the body of M_{19} would have to move towards V_{DD} by a voltage equal to 10 mV/η, or about 30 mV. However, since M_{16} and M_{17} were biased just at the edge of saturation, at least one or perhaps both of these devices will be forced into the Ohmic region. Assuming that the complementary pMOS regulated cascode current source, consisting of devices $M_{20–23}$, has an error in the opposite direction, it becomes clear that a significant circuit imbalance could develop from this problem. Fortunately, the solution to this problem is relatively simple. Shown in Figure 5.22 (b), the body-driven regulated cascode current source can be made much more robust by removing device M_{17}. Doing this adds drain overdrive voltage ($V_{DS} - V_{DSAT} > 0$) to M_{16}, which allows the body of M_{19} to swing by +/– 50 mV without adversely affecting the performance of the circuit. Unfortunately, this solution does create a small error (e.g., see Figure 5.9) in the output current of the M_{18} and M_{20} current sources. However, this is a common-mode error and will not affect the amplifier's offset voltage.

5.4.1.3 Shut-down of Voltage Bias Generator

A second important problem that was found, which also relates to only the pMOS devices, affects the PSRR at power supply voltages close to 1 V. If one compares the measured Macedonia V_{OS}–V_{DD} presented in Figure 5.18 to the simulated (without mismatch) V_{OS}–V_{DD} presented in Figure 5.20, one will notice an important similarity between the two curves. Specifically, at power supply voltages close to 1 V there is a

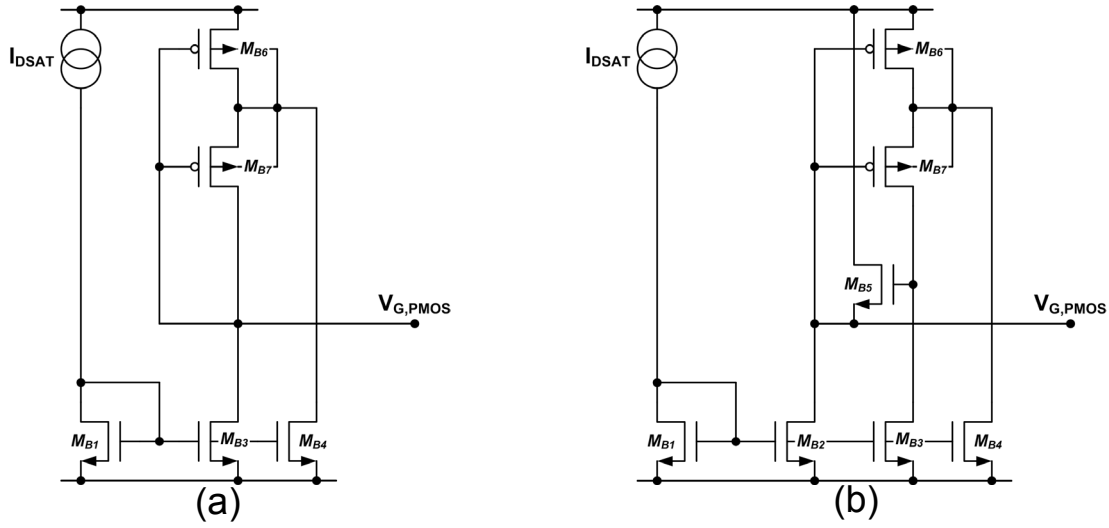

Figure 5.23: Schematic showing a pMOS adaptive gate bias generator (a) without and (b) with an nMOS level shifter

change in sign in the V_{OS}–V_{DD} curve which will result in a discontinuity in the PSRR–V_{DD} curve. Since this discontinuity occurs in both measurement and ideal simulations, it is clear that this must be a systematic effect. To understand this problem, first consider the pMOS adaptive gate bias generator shown in Figure 5.23 (a). Noting that the pMOS threshold voltage for this process is 0.85 V, one can see that if the pMOS devices M_{B6} and M_{B7} are biased close to IC = 1 (i.e., a gate overdrive voltage of approximately 25 mV) the V_{DS} of M_{B2} will be just over 100 mV. However, the bias generator (Figure 5.12) must also generate a gate bias for the pMOS cascodes, which will be at least 100 mV lower than the gate of M_{B6}. Of course, the problem with this is that the gate voltage of the pMOS cascode device will be nearly equal to V_{SS}, and once this happens the bias current will become extremely sensitive to V_{DD}. It seems that this is what is causing the low PSRR in the Macedonia amplifier close to 1-V V_{DD}. A simple solution to this prob-

lem is to add an nMOS level shifter (M_{B5}) to bias the pMOS devices M_{B6} and M_{B7}, as shown in Figure 5.23 (b). With the level shifter added, the current source device M_{B3} will remain in saturation, even when the gate voltage of the pMOS devices gets within a few milli-volts of V_{SS}. Simulations show that the addition of nMOS level shifters on all diode connected (V_{GD} = 0 V) pMOSFETs significantly improve PSRR in the region where V_{DD} was close to 1 V.

5.4.1.4 Op-Amp Schematics

The schematics for the core amplifier and voltage bias generator for the Mysia chip are shown in Figures 5.24 and 5.25, respectively. The key changes made to the core amplifier were to remove the cascode devices M_{17} and M_{23}, as described previously, and to convert the body-driven simple cascode current mirror composed of M_4, M_5, M_8, and M_9 to a gate-driven low-voltage cascode current mirror. This change was made to improve the V_{DS} matching on devices M_{19} and M_{21}. The key change made to the bias generator was the addition of three nMOS level shifters to the pMOS gate-driven diodes. Figure 5.26 presents the results of the Monte Carlo simulation of the Mysia amplifier's PSRR at V_{DD} = 1 V and 1.5 V. This simulation shows that the PSRR at 1 V has increased from 27 dB to 42 dB, while the PSRR at 1.5 V has increased from 44 dB to 62 dB, a significant improvement for both.

5.4.2 Op-Amp Measurement Results

The Mysia amplifier was received in January 2005 and tested during the Spring of 2005. Measurement results showed that while the amplifier still maintained high gain (in fact,

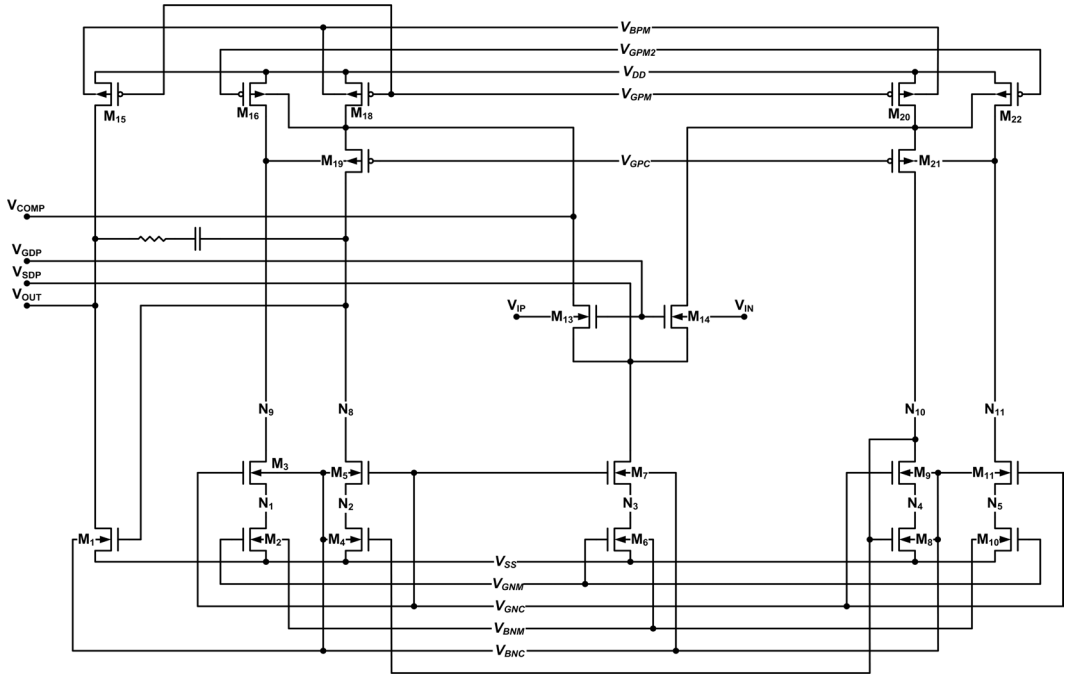

Figure 5.24: Schematic of the core amplifier from the Mysia chip

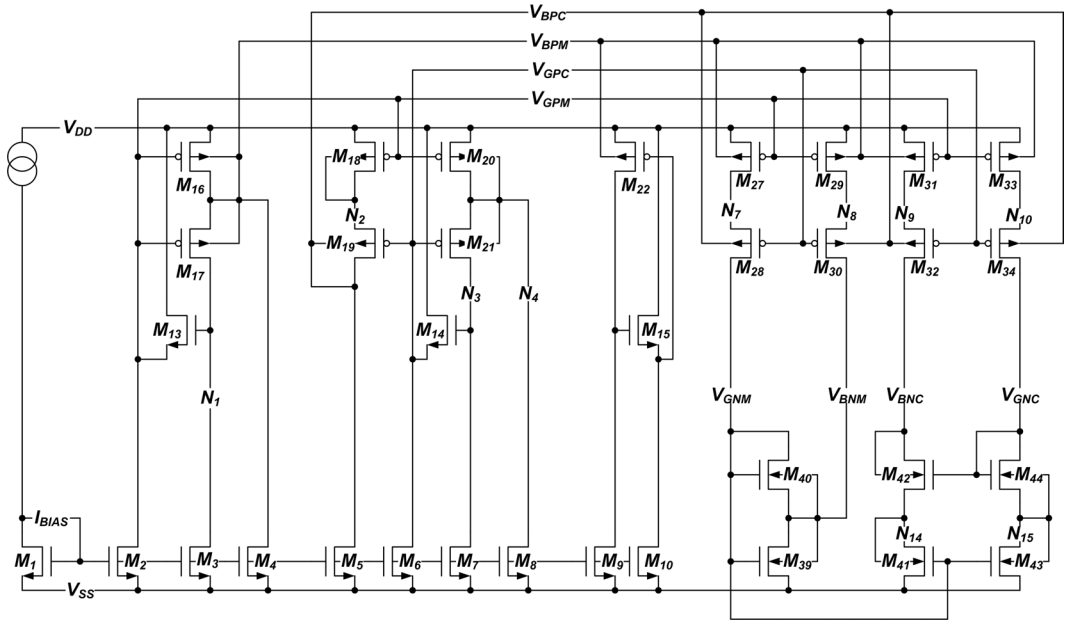

Figure 5.25: Schematic of the voltage bias generator from the Mysia chip

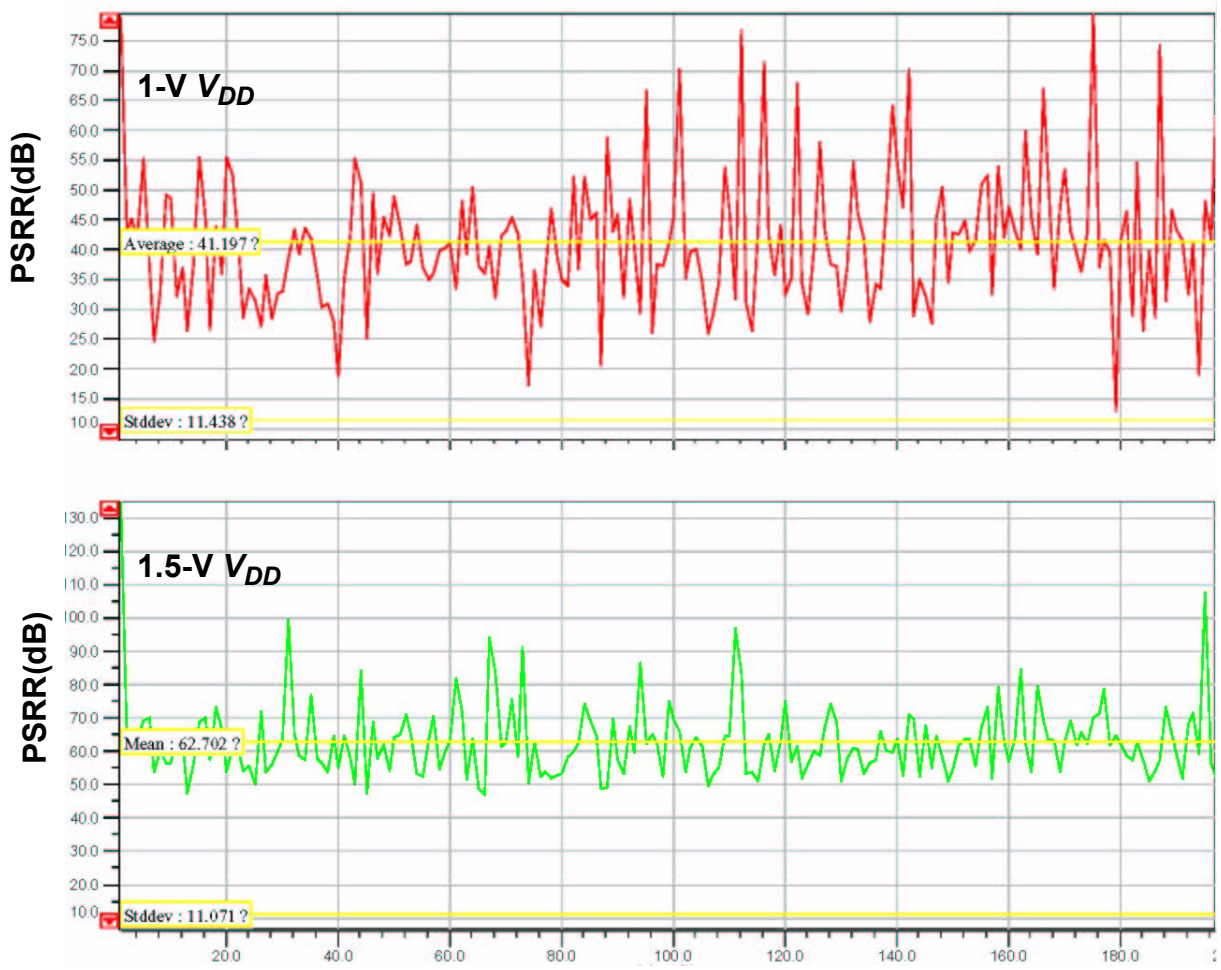

Figure 5.26: Monte Carlo simulation (200 permutations) of the Mysia op-amp PSRR at V_{DD} = 1 V and V_{DD} = 1.5 V

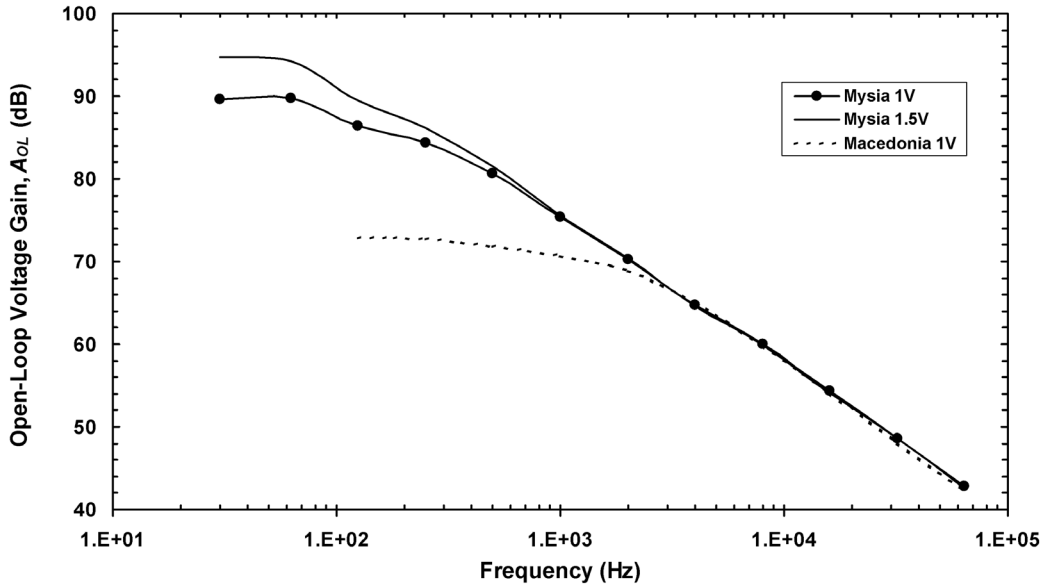

Figure 5.27: Comparison of the measured open-loop voltage gain for the Mysia and Macedonia amplifiers

the gain increased) and wide bandwidth, the PSRR and CMRR were significantly improved. In this section a complete set of characterization results for the amplifier will be presented, including open-loop gain, bandwidth, slew rate, PSRR, and CMRR.

5.4.2.1 Open-Loop Gain

Figure 5.27 presents a comparison of the measured open-loop gain for the Macedonia and Mysia amplifiers. Looking at this plot, one will immediately notice that the DC gain of the Mysia amplifier at 1-V V_{DD} is close to 90 dB, which is almost 15 dB higher than the measured gain of the Macedonia amplifier. The key reason for this improvement is the removal of the cascode devices M_{17} and M_{23}, which improved the loop-gain of the pMOS regulated cascode current sources, and thus directly improved the open-loop gain of the amplifier. In addition, this plot shows that the gain increases by about 5 dB in going

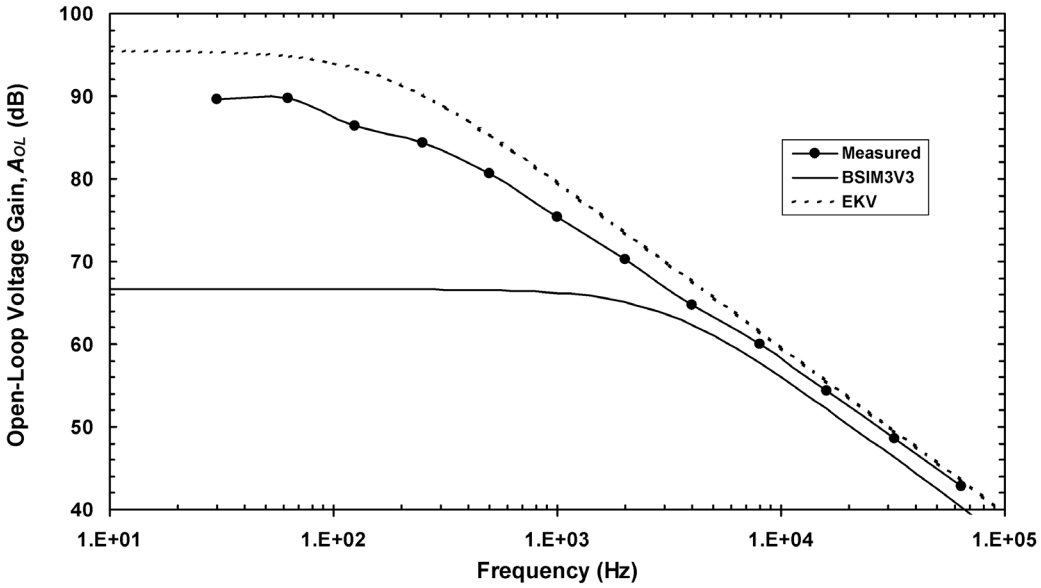

Figure 5.28: Comparison of simulated and measured open-loop gain for the Mysia amplifier

from V_{DD} = 1 V to V_{DD} = 1. 5 V. The gain boost is caused primarily by an increase in the voltage across the pMOS regulated cascode current source as V_{DD} is increased, and is an unavoidable consequence of low-voltage circuit design. As V_{DD} is increased beyond 1.5 V the gain stabilizes because all of the current sources are biased well into the saturation region. It is also important to note that beyond the corner frequency all three gain curves converge. This shows that the bandwidth of all three are the same (i.e., if one extrapolates these lines at 20 dB/decade to the 0-dB line they will all cross at the same point) and therefore the design changes made in going from the Macedonia amplifier to the Mysia amplifier did not adversely affect the bandwidth.

Figure 5.28 presents an interesting comparison of the measured and simulated (both BSIM3V3 and EKV) open-loop gain for the Mysia amplifier. This plot shows that EKV

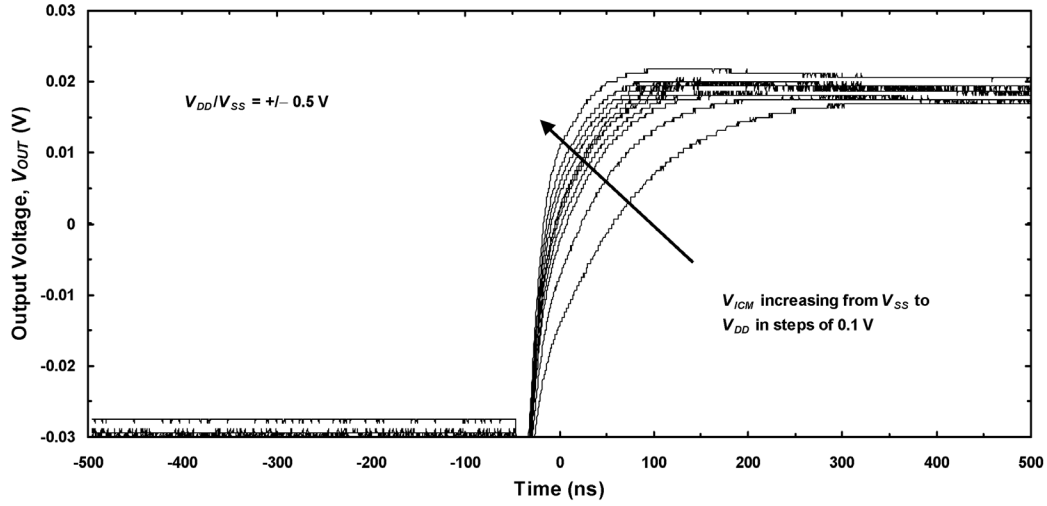

Figure 5.29: Measured small-signal step response of the Mysia amplifier as a function of common-mode level

overestimates the gain by roughly 8 dB, while the BSIM3V3 model underestimates the gain by almost 25 dB! It seems that the primary source of error in the BSIM3V3 simulation is that it underestimates the η of the pMOS devices in the regulated cascode current sources, which leads directly to a low value for the open-loop gain. It is also interesting to note that beyond the corner frequency the EKV simulated and measured gain match almost perfectly, which means that EKV is accurately calculating the transconductance of the body-driven input pair.

5.4.2.2 Step Response

Figure 5.29 presents the measured small-signal step response of the Macedonia amplifier as a function of common-mode level. In this measurement complementary power supplies of +/– 0.5 V were used, and the DC level of the input pulse was adjusted with each common-mode step so that the output offset was always close to zero. This plot

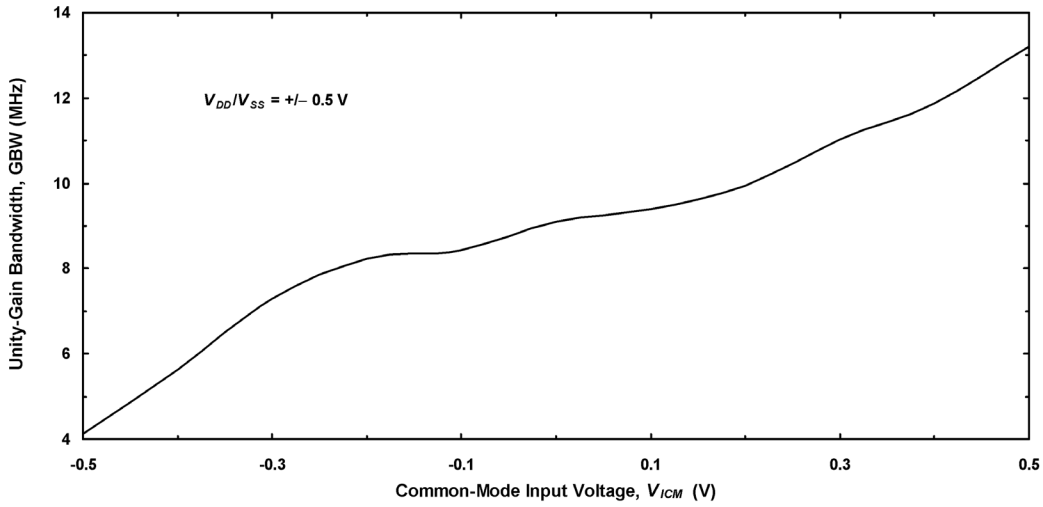

Figure 5.30: Measured unity-gain bandwidth versus common-mode level for the Mysia amplifier

shows that the op-amp *functions* over the full rail-to-rail common-mode input range. Therefore, in some sense it can be said that this amplifier has a rail-to-rail input common-mode range (ICMR). On the other hand, there is a significant drop-off in bandwidth when V_{ICM} is below (V_{SS} + 0.2 V), which calls into question how one can objectively define ICMR. One useful definition is to say that ICMR is the V_{ICM} range over which some minimum level of performance is maintained, which is typically quoted as a minimum CMRR (e.g., CMRR > 50 dB) but could also be quoted as minimum unity-gain bandwidth. Figure 5.30 presents a plot of the small-signal bandwidth as a function of common-mode level for the Mysia amplifier. For this plot the bandwidth was calculated from the risetime as [48]

$$BW = \frac{0.35}{t_{rise(10-90)}}, \tag{5.21}$$

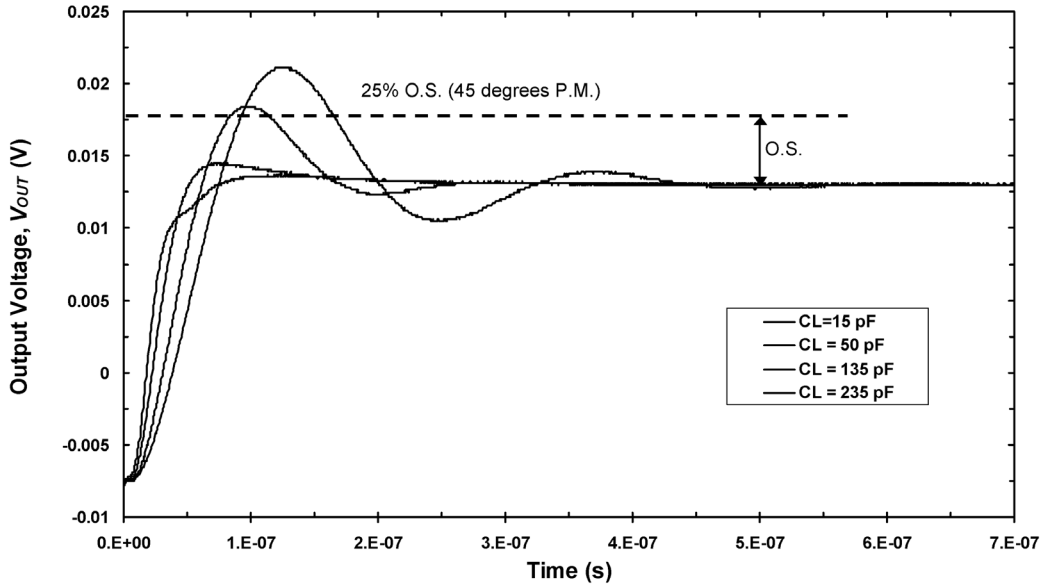

Figure 5.31: Measured small-signal step response as a function of capacitive load for the Mysia amplifier

which is a valid expression because the amplifier exhibited roughly 90° phase margin with the capacitive load used during this measurement. In Figure 5.30 we can see that the bandwidth at $V_{ICM} = V_{MID}$ is roughly 9 MHz, which is close to our target value, while at $V_{ICM} = (V_{SS} + 0.2\ V)$ the bandwidth is roughly 7.3 MHz, which represents a 20% reduction. It seems therefore that one can objectively say the amplifier has a nominal bandwidth of 9 MHz and an ICMR which extends from $(V_{SS} + 0.2V)$ to V_{DD}. This analysis of ICMR will be further bolstered by the CMRR measurements, which are presented in Section 5.4.2.4.

Another important aspect of transient performance is stability, and in particular the amplifier's stability as a function of capacitive load. Figure 5.31 presents the measured step response for the Mysia amplifier as a function of capacitive load. Since this amplifier

uses a two-stage, Miller compensated architecture, the phase margin is a direct function of C_L. A useful figure of merit that can be used when characterizing the stability of a Miller compensated amplifier is the stability number S, which is defined as the ratio of the non-dominant pole to the unity-gain bandwidth

$$S = \frac{f_2}{GBW} = \frac{\frac{g_{m2}}{2\pi C_L}}{\frac{g_{m1}}{2\pi C_M}} = \left(\frac{g_{m2}}{g_{m1}}\right) \cdot \left(\frac{C_M}{C_L}\right). \tag{5.22}$$

Here g_{m1} is the transconductance of the input pair, g_{m2} is the transconductance of the second-stage amplifier, C_M is the Miller capacitance, C_L is the load capacitance, and it is assumed that the right-half plane zero has been cancelled. Noting that the phase margin of a two-pole system is approximately 45° when the non-dominant pole frequency is equal to the unity-gain bandwidth, and noting that the only variable (once the amplifier has been fabricated) in Equation 5.22 is load capacitance, we can see that a useful characterization of the stability of a Miller compensated amplifier is the C_L for which phase margin equals 45°. Since a phase margin of 45° corresponds to an overshoot of 25% for a two-pole system, Figure 5.31 shows that a C_L of approximately 120 pF produces a phase margin of 45°.

The final aspect of transient performance that will be considered in this section is slew rate. Figure 5.32 presents a comparison of the measured and simulated large-signal step response for the Mysia amplifier. In this measurement the amplifier is biased with complementary power supply voltages of +/– 0.5 V, connected as a unity-gain follower, the capacitive load is approximately 20 pF, and the input is an 800-mV peak-to-peak pulse

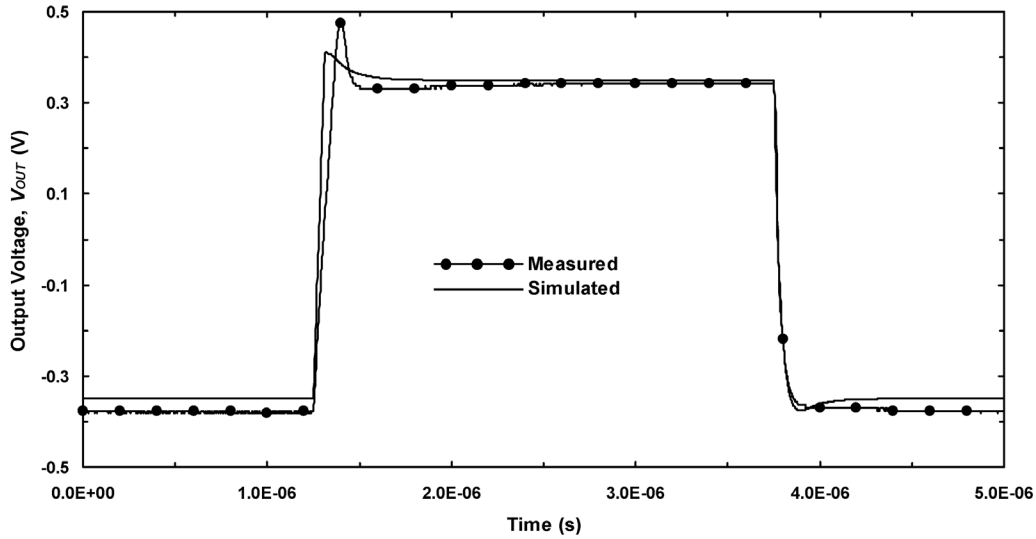

Figure 5.32: Measured and simulated large-signal step response for the Mysia amplifier

with zero offset. The measurement shows that the falling edge slew rate is 20 V/μs, while the rising edge slew rate is 10 V/μs. The rising edge slew rate is less because it is output stage limited by the pMOS current source M_{15}. In this design the output stage bias current (i.e., the drain current of M_{15} and M_1) is twice the tail current, and the Miller capacitance is 10 pF, so if the load capacitance is greater than 10 pF the rising edge slew rate will be output stage limited. Also, the large overshoot occurs on the rising-edge response because during a positive slewing event M_1 is turned off, so once the output reaches its correct value, a recovery time is required for M_1 to turn back on and bring the amplifier into small-signal operation.

5.4.2.3 PSRR

Up until this point in the discussion of the Mysia characterization results, we can see that the key performance parameters—open-loop gain and bandwidth—have been either

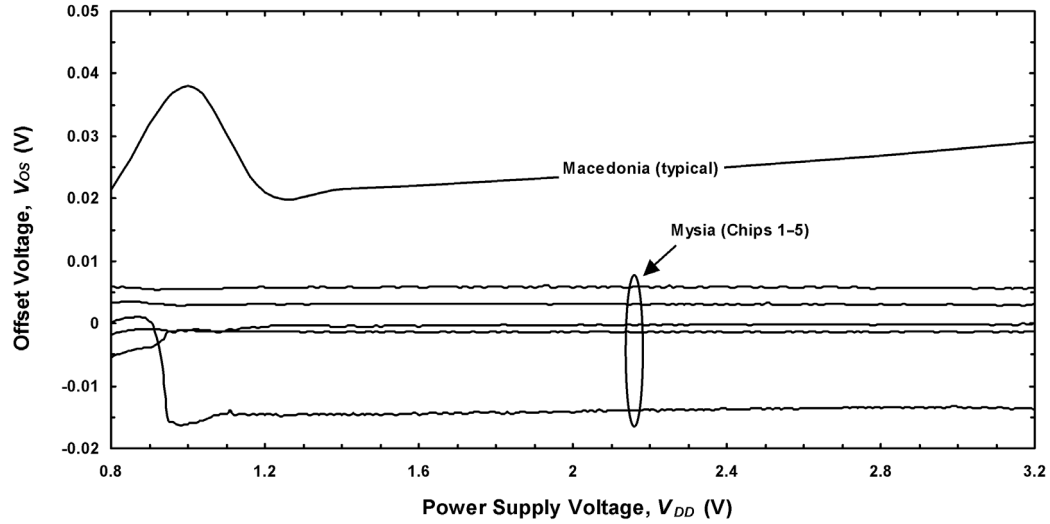

Figure 5.33: Measured V_{OS}–V_{DD} for five Mysia chips and comparison to a typical Macedonia amplifier

improved or at least not degraded by the design changes made in going from the Macedonia to Mysia amplifier. However, the main purpose in re-designing the body-driven amplifier was to improve the PSRR and CMRR; therefore these parameters are of a first-order importance for the Mysia amplifier. Figure 5.33 presents the measured V_{OS}–V_{DD} for the Mysia amplifier, along with the measured V_{OS}–V_{DD} for a typical Macedonia amplifier for comparison. Looking at Figure 5.33 one can clearly see that the PSRR is significantly improved. Whereas in the Macedonia amplifier the PSRR was close to 20 dB at 1-V V_{DD}, the Mysia PSRR at 1-V V_{DD} is between 45 and 65 dB; and whereas the Macedonia amplifier displayed a PSRR of roughly 45 dB at 1.5-V V_{DD}, the Mysia PSRR at 1.5-V V_{DD} is greater than 70 dB. Also, if one defines the allowable power supply voltage as the range of V_{DD} values for which a minimum (say 45 dB) PSRR is achieved, then it can

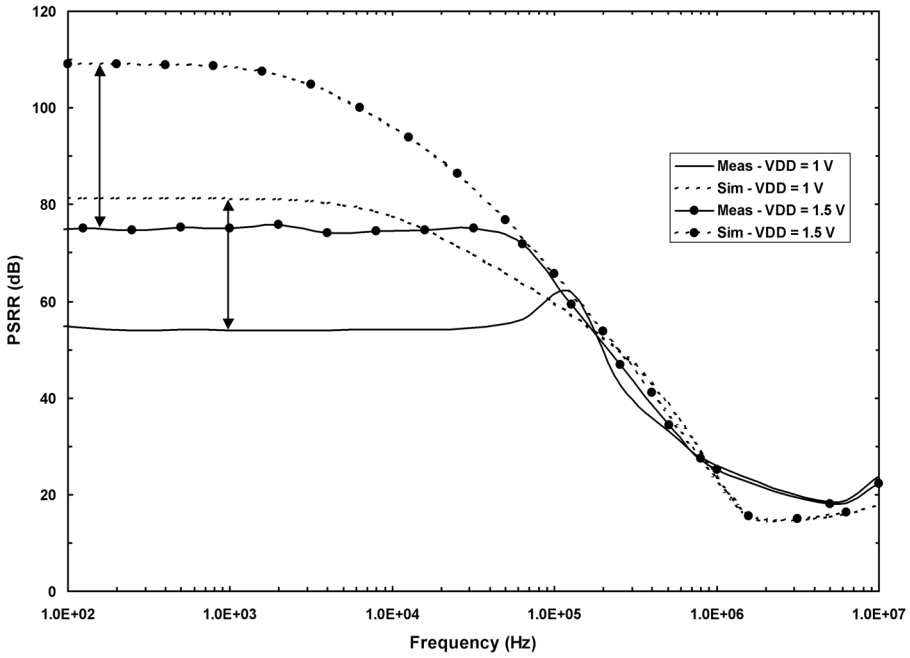

Figure 5.34: Comparison of measured and simulated (without mismatch effects) AC PSRR for the Mysia amplifier at V_{DD} = 1 V and 1.5 V

be stated with certainty that this amplifier can operate over the full power supply range of 1 V to 3.3 V.

After the Monte Carlo simulation study of PSRR that was previously presented, it is also interesting to consider whether or not it is meaningful to simulate PSRR without random mismatch effects. Figure 5.34, which is a plot of the measured and simulated (without mismatch effects) AC PSRR for the Mysia amplifier at 1-V and 1.5-V V_{DD}, provides an answer to this question. In looking at this plot, first consider the PSRR at low frequencies. For the 1-V case the low-frequency simulated PSRR is 80 dB, while the measured PSRR is 55 dB, a difference of 25 dB, or just over one order of magnitude. For the 1.5-V case the low-frequency simulated PSRR is 110 dB, while the measured PSRR is 75 dB,

a difference of 35 dB or almost two orders of magnitude. From the low-frequency results it is clear that the PSRR for this amplifier is dominated by random mismatch effects, which cannot be characterized without Monte Carlo analysis techniques. However, as frequency increases the measured and simulated curves eventually converge; for instance, all four curves show a PSRR of roughly 60 dB at 100 kHz. The reason that all of the curves converge at high frequencies is that at these frequencies the PSRR is dominated by parasitic capacitances and transconductances (i.e., AC voltage gains), both of which are always modeled, instead of DC offsets, which are only modeled in Monte Carlo analysis. Therefore it seems that if one wants to simulate PSRR at low frequencies Monte Carlo analysis is essential. On the other hand, if one is mainly interested in the high-frequency PSRR, say in an application where a circuit must reject high-frequency power supply noise from a switching regulator, then a standard AC SPICE simulation should suffice. Of course, these conclusions are drawn from the study of only one amplifier. However, it seems reasonable to assume that other amplifiers will follow these same basic trends.

5.4.2.4 CMRR

In Section 5.3.4 it was stated that the problems of poor PSRR and poor CMRR in the Macedonia amplifier have a common progenitor, and so fixing one should fix the other. It is now possible to test this hypothesis. Figure 5.35 presents the measured V_{OS}–V_{ICM} for five Mysia chips and a comparison to a typical Macedonia chip. Since the CMRR is dependent on random mismatch effects, it seems reasonable that a range of CMRR values will be observed, which is, in fact, the case. The best four Macedonia amplifiers dis-

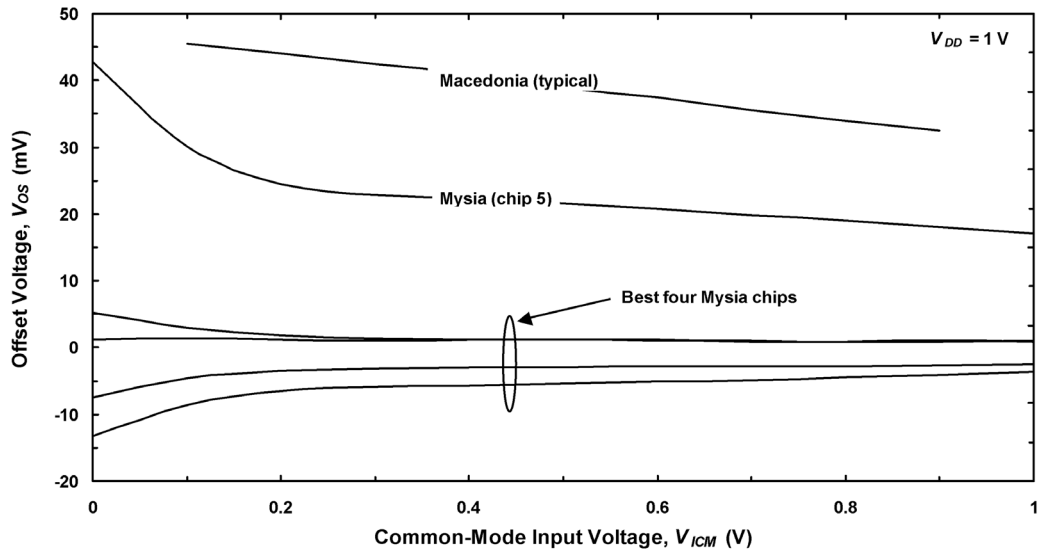

Figure 5.35: Measured V_{OS}–V_{ICM} for five Mysia chips and comparison to a typical Macedonia amplifier

played a CMRR at V_{ICM} = V_{MID} of 50 dB, 61 dB, 63 dB, and 66 dB, while the fifth amplifier displayed a CMRR of 43 dB. In comparison, the typical Macedonia amplifier displayed a CMRR of 36 dB at 1-V $_{VDD}$ and V_{ICM} = V_{MID}. Therefore we can see that CMRR has indeed increased along with the PSRR. In addition, one can also see a sharp change in V_{OS} and a commensurate reduction in CMRR below V_{ICM} = 0.2 V (this test was run with a single supply), which underscores the fact that the low-end ICMR for this amplifier is approximately $V_{SS} + 0.2V$.

While it is true that the design changes meant to improve the PSRR also improved the CMRR, it is also true that the improvements in CMRR were not as significant as those in PSRR. The reason for this is that there is another important limitation to CMRR that does not affect PSRR, and studying this limitation sheds light on another important aspect of

body-driven circuit design. Figure 5.36 presents the measured V_{OS}–V_{ICM} for Mysia chip 2 at V_{DD} values of 1 V, 2 V, and 3 V, and Figure 5.37 presents the measured CMRR–V_{ICM} (that is, the inverse derivative of Figure 5.36) for Mysia chip 2, also at V_{DD} values of 1 V, 2 V and 3 V. When looking at these plots, first consider the 3-V V_{DD} V_{OS}–V_{ICM} curve from Figure 5.36. In looking at this curve, one can see three distinct regions. The first region occurs from 0 < V_{ICM} < 0.2 V, where the CMRR is extremely low. The second region occurs from approximately 0.2 V < V_{ICM} < 2.5 V. In this region the CMRR is extremely high (> 60 dB) over the whole range. Finally, the third region occurs from 2.5 V < V_{ICM} < 3 V, where the CMRR is nearly constant at roughly 45 dB. In each of these regions the CMRR is set by the threshold mismatch of the input pair reflected through g_{mb} in the following way:

- Region 1 (0 V < V_{ICM} < 0.2 V): tail current source is shutting down, which causes a drop in g_{mb} with V_{ICM} and also causes the magnitude of the threshold voltage mismatch to increase significantly with reducing V_{ICM}.

- Region 2 (0.2 V < V_{ICM} < 2.5 V): In this region the tracking gate bias for the differential pair is active and holding the V_{BS} for the differential pair constant. This means that the g_{mb} is also constant, and so the offset changes little with V_{ICM}, resulting in high CMRR.

- Region 3 (2.5 V < V_{ICM} < 3 V): In this region the tracking gate bias for the differential pair reaches V_{DD}, and is no longer active. As V_{ICM} is increased the V_{BS} of the input

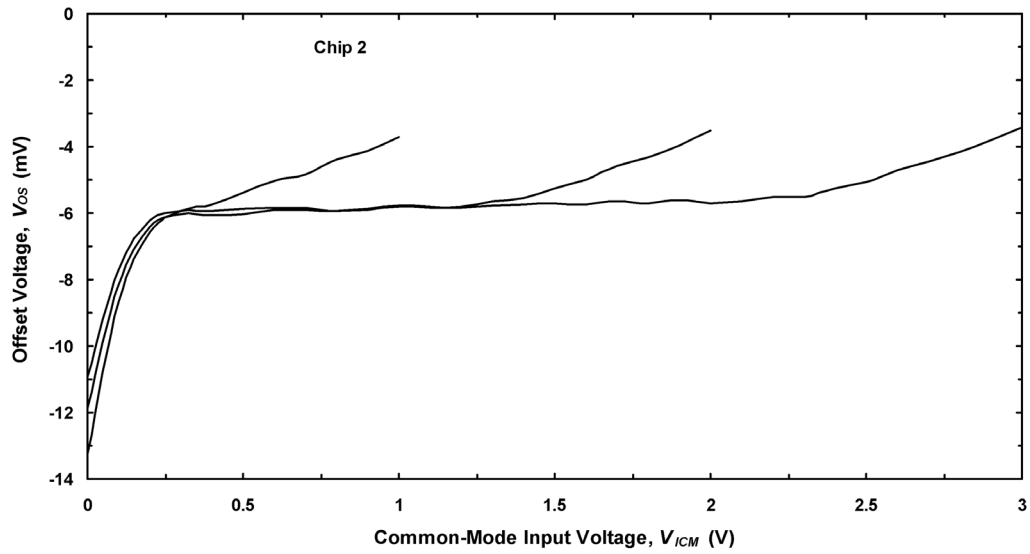

Figure 5.36: Measured V_{OS}–V_{ICM} for Mysia chip 2 at V_{DD} = 1 V, 2 V, and 3 V

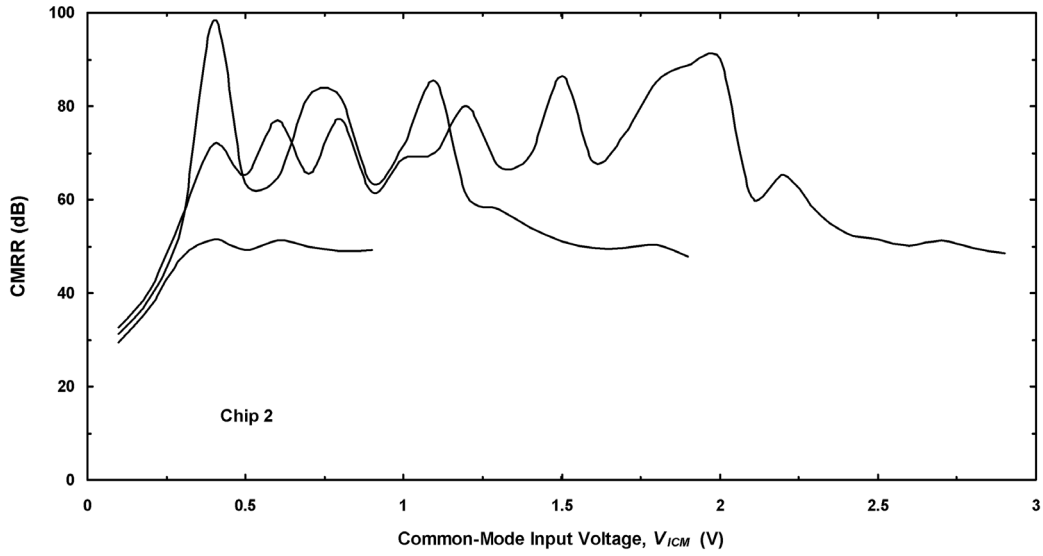

Figure 5.37: Measured CMRR–V_{ICM} for Mysia chip 2 at V_{DD} = 1 V, 2 V, and 3 V

pair becomes increasingly forward biased and the g_{mb} of the input pair increases with increasing common-mode level. The increasing g_{mb} decreases the magnitude of the offset voltage and thus affects the CMRR.

In looking at the V_{DD} = 1 V and 2 V curves in Figures 5.36 and 5.37, it is clear that all three regions are still present; however, in each case the size of region 2 is reduced by the amount that V_{DD} has been reduced.

Of course, if the CMRR is set by threshold mismatch in the input pair, then if one Mysia chip showed a very low offset voltage, it should have a correspondingly high CMRR. An example of such a case is presented in Figures 5.38 and 5.39, which present the measured V_{OS}–V_{ICM} and CMRR–V_{ICM} at V_{DD} values of 1 V, 2 V, and 3 V, for Mysia chip 4. Chip 4 displayed an offset voltage of roughly 1 mV, which is 6 times smaller than the 6 mV offset voltage displayed by chip 2. Moreover, the CMRR in region 3 is roughly 60 dB, or 15 dB higher (i.e., $20 \cdot \log(6)$) than chip 2. Note also that in both cases the region 2 CMRR is greater than 60 dB, for reasons already discussed.

5.4.2.5 Summary of the Measurement Results

Section 5.4.2 has presented a thorough characterization of the Mysia amplifier. Table 5.1 presents a summary of these measured results. When looking at Table 5.1, it is helpful to recall the design goals set for this amplifier at the beginning of Section 5.3:

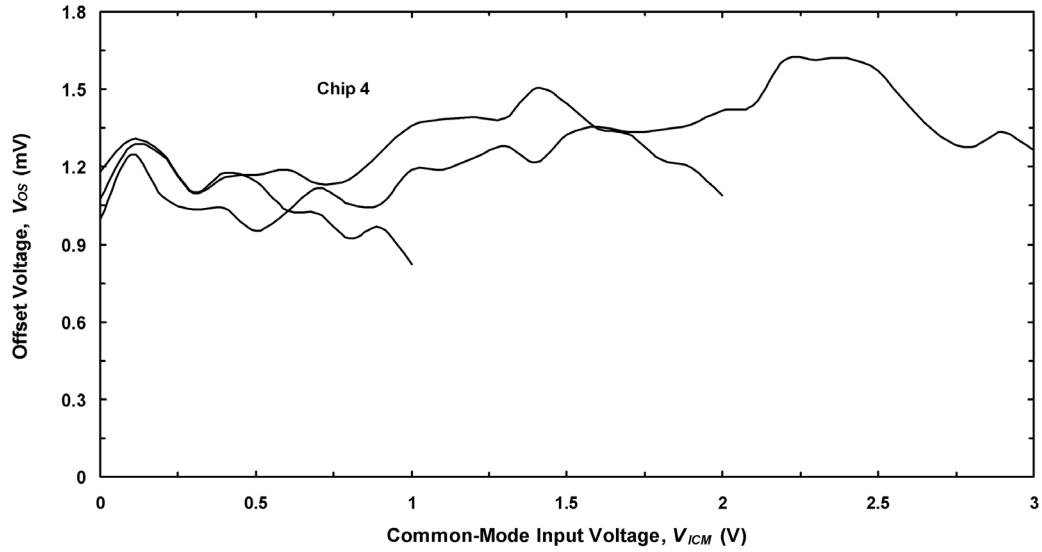

Figure 5.38: Measured V_{OS}–V_{ICM} for Mysia chip 4 at V_{DD} = 1 V, 2 V, and 3 V

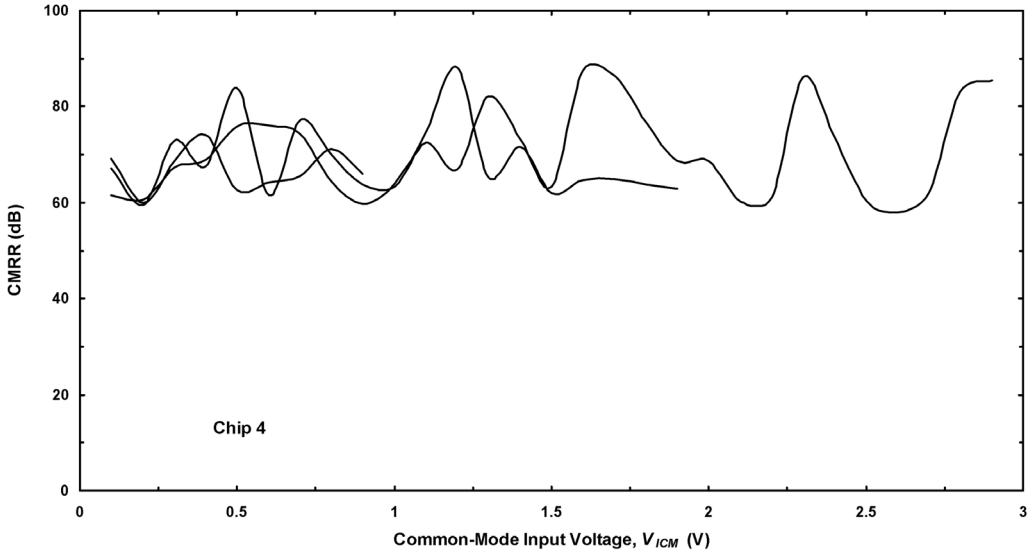

Figure 5.39: Measured CMRR–V_{ICM} for Mysia chip 4 at V_{DD} = 1 V, 2 V, and 3 V

Table 5.1: Summary of key measured parameters for the Mysia amplifier

Parameter	Measured Value
Power Supply Range	1–3.3 V
Supply Current	1.14 mA
ICMR	$(V_{SS} + 0.2) < V_{ICM} < V_{DD}$
Gain	88 dB
Unity-Gain Bandwidth	9 MHz
C_L (P.M. = 45°)	120 pF
Slew Rate (C_L < 10 pF)	+/– 20 V/μs
CMRR	45–65 dB
PSRR	55–75 dB

- to develop a body-driven op-amp whose performance far exceeds that of previously reported body-driven amplifiers, and in particular to achieve a high open-loop DC gain and wide unity-gain bandwidth,

- to use to as high a degree as possible body-driven circuit primitives, including differential pair(s), current mirror(s), and regulated cascode current source(s),

- to develop an op-amp that is useful for a wide array of applications by meeting performance goals over a wide input common-mode range and power supply range, and

- to use body-driven design techniques in a way that improves upon what can be achieved using standard gate-driven techniques at low voltages.

In light of these objectives, it seems clear that the op-amp development project has been successful.

Although, in addition to being simply a review of the op-amp performance characteristics, Sections 5.3 and 5.4 have highlighted many important aspects of body-driven and low-voltage circuit design. These include the following:

- In low-voltage circuit design it is essential to maximize the output voltage across current source loads in order to maximize gain.
- In designing body-driven circuits where MOSFETs are biased at the edge of saturation, it is essential to use Monte Carlo analysis to ensure that performance is maintained in the presence of random process variations.
- Minimizing op-amp offset voltage is essential to maximizing CMRR in a body-driven operational amplifier.

5.5 Comparison of the Body-Driven Op-Amp to Other Low-Voltage Op-Amps

As a final step in proving that body driving is a viable design technique, this section will present a comparison of the body-driven amplifier developed in this research to several other op-amps designed using various circuit techniques. The parameters that will be compared include operating power supply voltage, open-loop gain, bandwidth, slew rate, and PSRR. An additional figure of merit (FOM) that will be used to compare the op-amps is power efficiency, which is especially important for a body-driven amplifier since a commonly noted drawback of body driving is that body-driven transistors have one-third the

power efficiency of gate-driven transistors. Unfortunately, there is no commonly accepted definition of op-amp power efficiency that can be used for comparison, therefore this section will first begin by defining a power efficiency FOM. Then a table will be presented comparing the op-amps, along with some discussion.

5.5.1 Defining Op-Amp Power Efficiency

When attempting to define a power efficiency FOM for an amplifier, one must first ask the question, “What is the purpose, or key performance parameter, of the amplifier?” The FOM must then describe how efficiently the amplifier serves its purpose. For example, the classical definition of efficiency in a *power* amplifier is

$$\eta = \frac{P_{LOAD}}{P_{DC}}, \tag{5.23}$$

where P_{LOAD} is the power delivered to the load and P_{DC} is the power drawn from the DC supply. This is a useful FOM for characterizing power amplifiers, since the goal is to deliver power to a load as efficiently as possible. However, in many op-amp applications one is not interested in delivering power to a load, but is instead interested in meeting a bandwidth and/or capacitive load specification. In this case one must define a *small-signal* power efficiency FOM, which typically involves some form of a bandwidth-to-power efficiency ratio. Since the amplifier developed in this work is not intended to drive resistive loads, a measure of the small-signal power efficiency will be the most meaningful FOM. An additional consideration in using an FOM to compare small-signal amplifiers is that it is only meaningful to compare op-amps that have similar functionality. For instance, it is not a fair comparison to judge an op-amp with a limited ICMR against an

op-amp that has a rail-to-rail ICMR. The reason for this is that it takes an additional amount of power and circuitry, neither of which contribute to bandwidth, to take an op-amp from a limited ICMR to a rail-to-rail ICMR. Likewise it is not a fair comparison to judge a single-stage OTA against a two-stage operational amplifier. In this work the body-driven op-amp will be compared to other two-stage op-amps with rail-to-rail ICMR. The rest of this section will detail the development of a small-signal power efficiency FOM.

In trying to define a small-signal power efficiency FOM, one early low-voltage op-amp paper used the following bandwidth-to-power efficiency ratio [49]

$$FOM = \frac{BW}{P_{DC}} = \frac{BW}{I_{SUP}V_{DD}}, \tag{5.24}$$

where BW is the op-amp's unity-gain bandwidth and I_{SUP} is the DC supply current. In the context in which it was presented, Equation 5.24 was a useful FOM because a comparison was made between several amplifiers that were driving the same capacitive load. However, if one wants to compare amplifiers driving different capacitive loads, a modified FOM is required. In [50], a modified small-signal FOM was defined as

$$FOM = \frac{BW}{I_{SUP}V_{DD,\,Min}} \cdot \frac{C_L}{C_{REF}}, \tag{5.25}$$

where V_{DD} has been replaced by the term $V_{DD,Min}$, which is the minimum V_{DD} at which the amplifier can operate. Additionally, the FOM is multiplied by the ratio (C_L/C_{REF}), where C_{REF} is described as an "arbitrary" capacitive load.

The purpose of including the C_L/C_{REF} term was so that a comparison could be made between a reference amplifier, characterized at C_L = 10 pF, and another amplifier characterized at a different C_L. While it is a step forward to include C_L in the FOM definition, the value of the reference capacitance is anything but arbitrary. To understand why this is, consider the example of a two-stage Miller compensated op-amp (which is the architecture used by all of the op-amps in the comparison). Assuming that the right-half plane zero is cancelled, the unity-gain bandwidth and non-dominant pole frequency of the amplifier are defined as [26]

$$BW = \frac{g_{m1}}{2\pi C_M}, and \qquad f_2 \cong \frac{g_{m2}}{2\pi C_L}, \tag{5.26}$$

where g_{m1} is the transconductance of the first stage, g_{m2} is the transconductance of the second stage, and C_M is the Miller capacitance. From the location of the unity-gain bandwidth and non-dominant pole, the phase margin of a second-order system can be calculated as [51]

$$\begin{aligned} PM^\circ &= 90^\circ - \text{atan}\left(\frac{BW}{f_2}\right) \\ PM^\circ &= 90^\circ - \text{atan}\left(\frac{g_{m1}}{g_{m2}} \cdot \frac{C_L}{C_M}\right). \end{aligned} \tag{5.27}$$

Equation 5.27 shows that in a Miller compensated op-amp, phase margin is first-order dependent on load capacitance, this is why C_L in Equation 5.25 cannot be arbitrary. For instance, using Equation 5.25 it would be possible to show that the same op-amp has different power efficiency ratings when operated with a C_L that gives 60° PM as opposed to operating with a C_L that gives 45° PM. Clearly it is necessary to modify Equation 5.25

such that C_L is rated for a specific phase margin. Therefore, the small-signal power efficiency FOM that will be used in this work is defined as follows

$$FOM_{SCT} = \frac{2\pi BWC_{L,\,PM=45°}}{V_{DD,\,Min}I_{SUP}}, \tag{5.28}$$

where PM = 45° is used as the reference point for characterizing load capacitance.

5.5.2 Op-Amp Comparisons

Table 5.2 presents a comparison of the 1-V body-driven amplifier developed in this work to seven other 1-V operational amplifiers reported in the literature over a time period of more than a decade. Of the amplifiers listed, all utilize a two-stage Miller architecture and achieve a rail-to-rail input common-mode range; three of the amplifiers utilize common-mode level shifting to achieve rail-to-rail ICMR, while two of the amplifiers use body-driven input pairs, one of the amplifiers uses depletion-mode nMOSFETS, and one uses a combination of depletion-mode nMOSFETs and a body-driven input pair. In comparing the power efficiency of the amplifiers, one will notice that this amplifier achieves the highest power efficiency of any of the amplifiers reported. While it may seem surprising that a body-driven op-amp should achieve the highest power efficiency, there are at least two reasons for this:

- The amplifier developed in this work can be considered a “buffer.” In this context buffer means that the amplifier has been designed to drive a large capacitive load. In this situation the output stage dominates the amplifier’s power dissipation, so the reduced transconductance efficiency of the body-driven input pair would not

Table 5.2: Comparison of low-voltage amplifiers reported in the literature

Reference	VDD range (V)	I_{DD} (mA)	BW (MHz)	$C_{L,PM=45°}$ (pF)	FOM_{SCT} (V^{-2})	Gain (dB)	SR (V/μs)	ICMR	PSRR (dB)	Comments
[14]	1–6	0.75	0.45	133	0.501	100	0.17	R2R +	38–100	Si BJT, uses CMLS*
[52]	1–7.5	1.2	4.5	35	0.825	110	4	R2R	80	uses depletion-mode nMOS input, BiCMOS
[40]	1	0.287	1.3	34	0.968	49	1.6	R2R	NA	BD input, uses current mirror with LS
[15]	1	0.41	1.9	27	0.786	87	1	R2R	62	CMOS, uses CMLS
[15]	1	0.208	2.1	49	3.11	70.5	1.7	R2R	58	CMOS, uses CMLS
[53]	1	0.005	0.19	12	2.87	70	0.15	R2R	NA	BD input pair, similar to
[41]	0.9–6	0.0005	0.0056	22.6	1.59	70–79	NA	R2R	25–59	depletion-mode nMOS plus BD input pair
This work	1–3.3	1.1	9	120	6.17	88	20	0.2–V_{DD}	45–65	BD input pair and BD reg. cas. current source

*CMLS is common-mode level shifting (e.g., see Section 2.4.1.1)

significantly affect the overall amplifier power efficiency (at least when the power efficiency is defined as in Equation 5.28). The power efficiency of body-driven versus gate-driven amplifiers is studied in more detail in Section 6.2.

- In several of the op-amps a class-AB output stage is used, whereas a class-A output stage is used in the body-driven amplifier. Therefore one source of the extra power dissipation could be the more complex output stages. Note that while it is normally assumed that Class-AB output stages are more efficient than Class-A, this is actually only the case for a slew-rate limited output stage. If one considers an amplifier in terms of small-signal stability and capacitive load driving capability, as in Equation 5.28, then a Class-A driver does not represent a power penalty.

In comparing the rest of the parameters one will notice that the body-driven amplifier achieves a high-voltage gain and wide bandwidth, which have already been stated as important goals for this work. In addition, the PSRR of the body-driven amplifier is commensurate with other amplifiers. From this comparison, it seems clear that this body-driven amplifier has outperformed previously reported body-driven amplifiers, and also that body driving is competitive with other low-voltage design techniques. In Chapter 6 a discussion will be presented describing when body driving is preferred over other low-voltage design techniques.

5.6 Conclusions

Chapter 5 has presented a complete review of the adaptive gate bias technique and its application in the design of a high-performance body-driven operational amplifier. Section 5.2 described the new adaptive gate bias technique for body-driven current mirrors,

and presented design details for simple current mirrors, simple cascode current mirrors, and regulated cascode current mirrors. A comparison of this technique to other prior art body-driven current mirror techniques showed that it had superior dynamic range and enabled the designer to guarantee that MOSFETs in a body-driven current mirror were biased in saturation. In Section 5.3 the adaptive gate bias technique was applied to the design of a complete body-driven amplifier which was fabricated and tested. Measurement results from this first body-driven amplifier, named Macedonia, showed that it achieved high open-loop gain and wide bandwidth, but that is also had poor PSRR and CMRR. In Section 5.4 a study of the Macedonia amplifier's PSRR using Monte Carlo analysis was described. Based on the Monte Carlo analysis several design changes were made and a second amplifier, named Mysia, was sent for fabrication. Measurement results of the Mysia amplifier showed that it also achieved high open-loop gain and wide bandwidth, and exhibited significant improvement in CMRR and PSRR. Finally, in Section 5.5 it was shown that the body-driven amplifier developed in this research compares favorably to other 1-V amplifiers reported in the literature.

Chapter 6

The Application of Body-Driven Circuits to Analog and Mixed-Signal Systems

6.1 Introduction

It is the opinion of this author that this research has conclusively proven the proposition that high-performance analog circuits can be designed with body-driven techniques. What is less clear, however, is how body-driven circuits can best be applied in complex analog and mixed-signal systems. A good place to start in answering this question is to look at the drawbacks of body-driven circuits to see what applications are not amenable to body driving. The three most frequently listed drawbacks of body driving are

- the possibility of forward biasing the body–source junction,
- a reduced f_T with respect to a gate-driven transistor, and
- reduced power efficiency with respect to a gate-driven circuit.

As to the first point, it seems that this problem is not really much of a concern. Throughout this research numerous body-driven circuits have been simulated and tested without damaging any devices by forward biasing the body–source junction. It has already been shown how the adaptive gate bias technique sets the device V_{BS} close to V_{DSAT}, which is well within the safe operating range. In addition, within an amplifier all of the device bodies are driven by circuits that are current limited (i.e., current sources) so no damage

would result if a body did become forward biased briefly (e.g., in a large-signal transient condition).

The second point is entirely valid, a minimum-*L* body-driven nMOSFET in SOI technology will have roughly one-third the f_T of a same-size gate-driven nMOSFET. Of course, a body-driven nMOSFET will have nearly the same f_T as a gate-driven pMOSFET, so the problem is perhaps not as significant as it might seem. As in any circuit design, the general rule should be that if the advantages of using a body-driven circuit in a certain situation outweigh the drawbacks, then it should be used. While body-driven MOSFETs are not optimum devices for high-speed operation, they do have advantages for low-voltage operation that might warrant their use in a high-speed, low-voltage design. The key point is that a designer should not rule out, *a priori*, the use of body-driven transistors in a high-speed design. In fact, a recently reported mixer that operates at 2.2 GHz utilized body-driven MOSFETs in the RF signal path [54].

The final point, that body-driven circuits have lower power efficiency than gate-driven circuits, is perhaps the most difficult to address. In Section 5.5 it was shown that the body-driven amplifier developed in this research had a higher power efficiency than several other low-voltage op-amps reported in the literature, many of which used only gate-driven transistors. It would be incorrect, however, to assume from this one example that body-driven circuits will always achieve the same power efficiency as gate-driven circuits. Instead, power efficiency is application dependent; in some applications body-driven transistors will not represent a power penalty, while in others they will. However, reduced power efficiency is probably the single most important drawback for body-driven

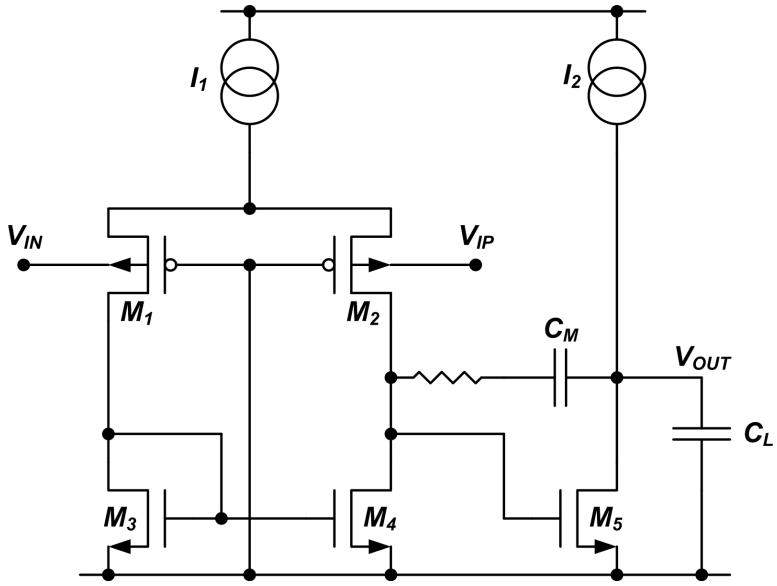

Figure 6.1: Schematic of a two-stage, Miller-compensated op-amp

circuits and should be considered in more detail. Therefore in the next section a detailed analysis of the power efficiency of a two-stage body-driven amplifier will be presented.

6.2 Power Efficiency of a Two-Stage Body-Driven Amplifier

Figure 6.1 presents the schematic of a two-stage, Miller compensated amplifier that will be used in this study of power efficiency. In Section 6.2.1 power efficiency will be analyzed assuming the amplifier is used as a buffer, where a buffer in this case is taken to mean an amplifier that must drive a large capacitive load. On the other hand, Section 6.2.2 analyzes the power efficiency of the amplifier when it is used in a high-resolution circuit—the specific example studied is the application of the amplifier to a pipeline analog-to-digital converter (ADC).

6.2.1 Power Efficiency of a "Buffer" Circuit

To analyze the power efficiency of a body-driven amplifier used as a buffer, we can first try to re-write the power efficiency FOM, defined in Equation 5.28, in terms of the transconductance efficiency of the body-driven input pair. First, note that when PM = 45°, the non-dominant pole location is the same as the unity-gain bandwidth. Therefore we can write

$$f_2 = BW = \frac{g_{m5}}{2\pi C_{L,\,PM=45^\circ}}, \tag{6.1}$$

which can be solved for C_L as

$$C_{L,\,PM=45^\circ} = \frac{g_{m5}}{2\pi BW}, \tag{6.2}$$

and substituted into Equation 5.28 to give

$$FOM_{SCT} = \frac{g_{m5}}{I_{SUP} \cdot V_{DD}} \ . \tag{6.3}$$

Next, assuming that $I_2 = 2I_1$ (a standard bias condition for a buffer) the total supply current for the amplifier is given by

$$I_{SUP} = I_2/2 + I_2 \Rightarrow I_2 = (2/3)I_{SUP}, \tag{6.4}$$

and g_{m5} can be written as

$$g_{m5} = \left(\frac{g_m}{I_D}\right)_5 \cdot (2/3) I_{SUP} \cdot \tag{6.5}$$

Finally, the FOM can simplified to

$$FOM_{SCT} = \frac{2}{3} \cdot \left(\frac{g_m}{I_D}\right)_5 \cdot \left(\frac{1}{V_{DD}}\right). \tag{6.6}$$

Equation 6.6 provides the somewhat surprising result that the power efficiency of the two-stage amplifier in no way depends on the transconductance efficiency of the input pair. Though this result may at first seem counterintuitive, in fact upon further consideration this result does make sense for the case of the buffer. For example, consider the following design problem for a two-stage op-amp

- Design a two-stage op-amp with 10-MHz bandwidth and 60° PM at C_L = 20 pF. Assume that the output stage bias current is twice the tail current. In addition, assume that the g_m/I_D of device M_5 is 19, while the g_m/I_D of devices M_1 and M_2 is either 19 (i.e., a gate-driven MOSFET operating at *IC* = 1) or 6.3 (i.e., a body-driven MOSFET operating at *IC* = 1). Compare the total supply current in each case.

Table 6.1: Comparison of the two buffer op-amp designs

Parameter	Gate-Driven Input Pair	Body-Driven Input Pair
I_2	114 μA	114 μA
$(g_m/I_D)_5$	19	19
g_{m5}	2.17 mmho	2.17 mmho
f_2 (C_L = 20pF)	17.3 MHz	17.3 MHz
$(g_m/I_D)_{1,2}$	19	6.3
$g_{m1,2}$	541.5 μmho	178.7 μmho
C_M	8.62 pF	2.84 pF
BW	10 MHz	10 MHz
PM (C_L = 20 pF)	60°	60°
I_{SUP}	171 μA	171 μA

The key calculations for the amplifier are as follows

$$
\begin{aligned}
f_2 &= \frac{10MHz}{\tan(90° - 60°)} = \underline{17.3MHz} \\
g_{m5} &= 2\pi \cdot 17.3MHz \cdot 20pF = \underline{2.17mmho} \\
I_2 &= 2.17mmho/19 = \underline{114\mu A} \\
g_{m1,2} &= \left(\frac{g_m}{I_D}\right)_{1,2} \cdot 28.5\mu A \\
C_M &= \frac{g_{m1,2}}{2\pi \cdot 10MHz}.
\end{aligned}
\tag{6.7}
$$

Using the equations presented in 6.7, the solutions presented in Table 6.1 are obtained. What this problem shows is that the transconductance efficiency of the input pair is not important because one can simply scale the Miller capacitor to achieve a desired band-

width, while the second-stage transconductance is important because load capacitance is typically a design specification in a buffer amplifier and therefore is fixed.

6.2.2 Power Efficiency of a High-Resolution Circuit

The previous example showed that if load capacitance is the key specification, then the power efficiency of the input pair is unimportant because the Miller capacitance can be scaled to achieve a certain bandwidth. However, in high-resolution applications the Miller capacitance cannot be chosen arbitrarily, because it defines the total thermal noise power at the output of the amplifier. To see why this is, assume that the input-referred noise of an op-amp is dominated by the input differential pair, which is the optimum case. The input referred noise voltage density for this case is given by

$$\overline{e_{ni}^2} = 8kT\gamma\frac{1}{g_M}, \tag{6.8}$$

which was previously presented in Chapter 2 in the context of an OTA. Assuming that the amplifier is connected as a unity-gain follower, the closed-loop transfer function is

$$H(f) = \frac{1}{1+j\frac{f}{f_o}}, \tag{6.9}$$

where f_o is the unity-gain bandwidth previously defined in Equation 5.26. Finally, noting that Equations 6.8 and 6.9 are the same as those presented in the OTA noise analysis in Section 2.3.1, the total noise power at the output of the amplifier will be given by

$$\overline{v_o^2} = \frac{2\gamma kT}{C_M}. \tag{6.10}$$

Equation 6.10 shows that the Miller capacitance represents a fundamental limitation to the noise performance that a circuit can achieve. For high-resolution circuits, this represents a limit for how small the Miller capacitance can scale, and in many high resolution circuits the input stage power dissipation will actually be larger than the output stage. In this case the transconductance efficiency of the body-driven input pair will affect the power efficiency of the complete amplifier, and the use of body-driven transistors will, to a greater or lesser degree depending on the application, cause a reduction in the amplifier's power efficiency.

Figure 6.2 presents the schematic of a flip-around multiply-by-two switched-capacitor stage that is commonly used in pipeline ADCs [55]. An op-amp design example highlighting the power efficiency of a high-resolution system will be presented using this circuit. The design problem is as follows:

- Using the circuit of Figure 6.1, design an op-amp to be used as part of a pipeline ADC, as shown in Figure 6.2. The ADC should have a clock rate of 10 MS/s, 10-bit resolution, and a full-scale voltage of 1 V. Assume that the g_m/I_D of device M_5 is 19, while the g_m/I_D of devices M_1 and M_2 is either 19 (i.e., a gate-driven MOSFET operating at $IC = 1$) or 6.3 (i.e., a body-driven MOSFET operating at $IC = 1$). However, note that the ADC must have adequate small-signal settling time *and* slew rate, the latter of which might necessitate reducing the g_m/I_D of the input pair and/or the output driver. Compare the total supply current in each case.

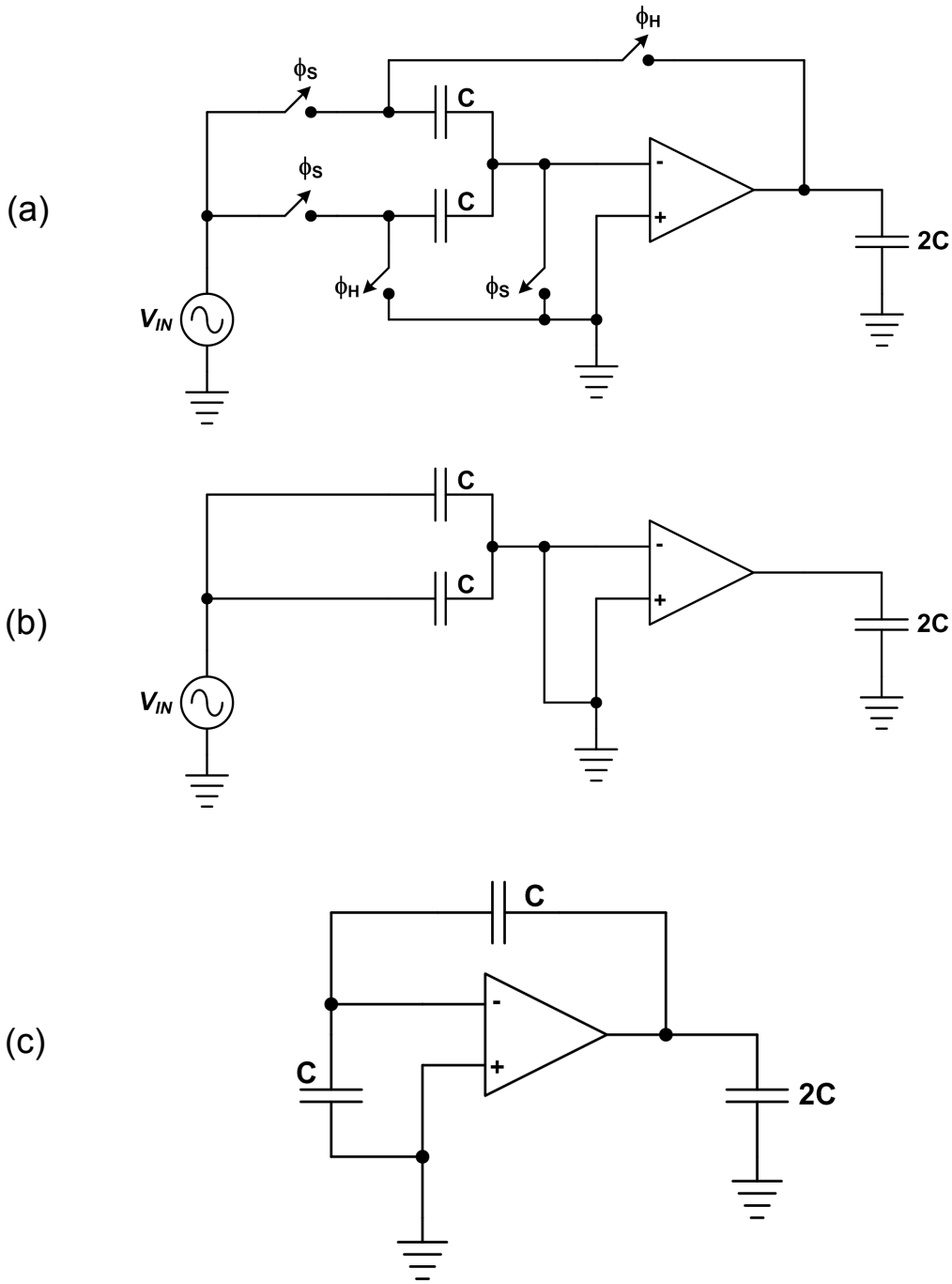

Figure 6.2: Flip-around multiply- by-two stage: (a) complete circuit, (b) in sample phase, and (c) in hold phase

6.2.2.1 Calculation of the Miller Capacitance and Sampling Capacitance

The first step in this problem is to calculate the required value of Miller capacitance and sampling capacitance by completing a noise analysis. Like all switched-capacitor circuits, this circuit operates in a sample phase and a hold phase, and the noise generated during each phase must be computed to complete the analysis. The noise generated during the sample phase is given by the well-known kT/C relationship

$$\overline{v_s^2} = \frac{kT}{2C}. \tag{6.11}$$

During the hold phase there are two noise components to consider—the noise from the sampling capacitors and the noise due to the op-amp. We will first consider the noise due to the sampling capacitors. When the top capacitor in Figure 6.2 flips around to the hold mode, the noise stored on it is reflected directly to the output with a gain of 1, while the noise stored on the second capacitor is transferred to the feedback capacitor, also with a gain of 1. The net result is that the total output noise due to the sampling capacitors is equal to the sum of the noise stored on each. The mean-square value of this noise can be calculated using the expectation operator [56]

$$\overline{v_{o,s}^2} = E[(v_s + v_s)^2] = 2\overline{v_s^2} + 2\rho\sqrt{\overline{v_s^2}}\sqrt{\overline{v_s^2}}, \tag{6.12}$$

where ρ is the correlation coefficient between the two samples. However, since the two samples are identical, they have a correlation coefficient of 1, and the total output noise due to the sampling capacitors is

$$\overline{v_{o,s}^2} = \frac{2kT}{C}. \tag{6.13}$$

On the other hand, the total output noise due to the op-amp is the mean-square noise given in Equation 6.10 multiplied by the square of the closed-loop non-inverting gain, and also multiplied by the β bandwidth reduction factor (1/2). Therefore the output noise due to the op-amp is

$$\overline{v^2_{o,amp}} = \frac{2.67kT}{C_M}, \tag{6.14}$$

where 2/3 has been substituted for γ. Finally, the total op-amp output noise at the end of the hold phase can be calculated as

$$\overline{v^2_{o,tot}} = \frac{2.67kT}{C_M} + \frac{2kT}{C}, \tag{6.15}$$

where there is no cross product because the two noise terms are uncorrelated.

The mean-square noise "generated" by an ideal ADC, which is referred to as quantization noise, is generally approximated as [57]

$$\overline{q^2} = \frac{LSB^2}{12}. \tag{6.16}$$

When designing an ADC a typical goal is that the errors due to device non-idealities (e.g., noise, finite settling time) should be less than 1/2 LSB. Using the 1/2 LSB criterion, the total op-amp output noise is given by

$$\frac{2.67kT}{C_M} + \frac{2kT}{C} \le \frac{((LSB)/2)^2}{12}. \tag{6.17}$$

Note that the design goal for the noise is not actually 1/2-LSB total RMS noise, but instead that the noise level is equivalent to the noise generated by an ideal ADC whose

LSB is one half the size of our LSB. Next, we can define that the op-amp and sampling switches/capacitors have equal noise contributions, which allows us to calculate the value of the Miller capacitance

$$\frac{2.67kT}{C_M} = \left(\frac{1}{2}\right) \cdot \left(\frac{LSB^2}{48}\right) = \left(\frac{1}{2}\right) \cdot \left(\frac{2^{-20}}{48}\right), \tag{6.18}$$

which gives a Miller capacitor value of 1.1 pF. Likewise, the sampling capacitor value can be calculated as 0.83 pF.

6.2.2.2 Calculation of the Unity-Gain Bandwidth and Non-Dominant Pole Location

The next step in the problem is to calculate required unity-gain bandwidth and the location of the non-dominant pole. The bandwidth and phase margin in this application must be chosen on the basis of settling to within a 1/2-LSB error within 1/2 clock cycle. For high-resolution applications, the optimum phase margin is that which limits the overshoot in the transient to less than 1/2-LSB, which is given by [51]

$$\phi_{M,\,Opt} = 90° - \text{atan}\left(\frac{1 + (\pi/(\ln 2^{-(n+1)}))^2}{4}\right), \tag{6.19}$$

where *n* is resolution in bits. For this 10-bit ADC design, the optimum phase margin is approximately 74°. The bandwidth for the amplifier is chosen based on the time to the peak. At 74° phase margin, the relationship between the unity-gain bandwidth of the amplifier's loop transmission and the peaking time is given by [51]

$$GBW_T \cong \frac{0.6}{t_p} = \frac{0.6}{T_{CLOCK}/2} = 1.2f_{CLOCK}, \tag{6.20}$$

where f_{CLOCK} is the ADC clock frequency. Using Equation 5.27, the non-dominant pole

location can be calculated as

$$f_2 = \frac{GBW_T}{\tan(90 - PM)} \cong 4.2 f_{CLOCK}. \tag{6.21}$$

Finally, it should be noted that the amplifier is connected with a closed-loop gain of –1, so the unity-gain bandwidth of the amplifier should be twice the unity-gain bandwidth of the loop transmission. Therefore the amplifier unity-gain bandwidth and non-dominant pole location can be calculated as follows:

$$\begin{aligned} GBW &= 2.4 f_{CLOCK} = \underline{24MHz} \\ f_2 &= 4.2 f_{CLOCK} = \underline{42MHz}. \end{aligned} \tag{6.22}$$

6.2.2.3 Final Calculations

Now that the capacitor values and critical frequencies have been calculated, it is straightforward to find the power dissipation of the op-amp. The first step is to calculate the total load capacitance, which has three components: first, the output will be driving 2C, which represents the sampling capacitance of the next stage; second, the output will be driving 0.5C which accounts for the feedback network; third, the op-amp will be driving another 0.5C that accounts for the common-mode feedback network that would be present in an actual implementation of a pipeline ADC [55]. Therefore the second-stage bias current can be calculated as

$$I_2 = \frac{2\pi f_2 \cdot 3C}{(g_m / I_D)_5}, \tag{6.23}$$

while the first-stage bias current is calculated as

$$I_1 = \frac{2\pi GBW \cdot C_M}{0.5 \cdot (g_m/I_D)_{1,2}} \cdot \tag{6.24}$$

Here $(g_m/I_D)_{1,2}$ is 19 or 6.3 depending on whether or not a gate-driven or body-driven input pair is used. However, the analysis up to this point has only considered small-signal performance. Equally important in an ADC is that the amplifier is able to slew the full-scale output range in 1/2-clock cycle, which for this case equates to a 20V/μs slew rate (i.e., 1-V full scale in 50 ns). Therefore the first- and second-stage bias currents must actually be chosen as

$$\begin{aligned} I_1 &= max\left(\frac{2\pi GBW \cdot C_M}{0.5 \cdot (g_m/I_D)_{1,2}}, C_M \cdot 20\frac{V}{\mu s}\right) \\ I_2 &= max\left(\frac{2\pi f_2 \cdot 3C}{(g_m/I_D)_5}, (3C + C_M) \cdot 20\frac{V}{\mu s}\right). \end{aligned} \tag{6.25}$$

Table 6.2 presents the final comparison of the two amplifier designs. The data in Table 6.2 actually present the solution to the pipeline ADC problem for two different cases, although the two different cases only affect the data listed in the supply current and transconductance efficiency rows. The first case assumes that the amplifier uses a fixed tail current and a class-A output driver, as shown Figure 6.1, this data is not in parentheses. The second case assumes that a class-AB output stage (i.e., both sourcing and sinking output stage drive currents can be much larger than the static bias current, e.g., see [58]) and a high slew rate input stage (i.e., the current charging the Miller capacitor

Table 6.2: Comparison of the two pipeline ADC op-amp designs
(design parameters based on only small-signal settling time shown in parentheses)

Parameter	Gate-Driven Input Pair	Body-Driven Input Pair
C_M	1.1 pF	1.1 pF
C	0.83 pF	0.83 pF
I_2	71.8 μA (34.6 μA)	71.8 μA (34.6 μA)
$(g_m/I_D)_5$	9.2 (19.3)	9.2 (19.3)
g_{m5}	657 μmho	657 μmho
f_2	42 MHz	42 MHz
I_1	22 μA (17.5 μA)	52.7 μA
$(g_m/I_D)_{1,2}$	15.1 (19)	6.3
$g_{m1,2}$	166 μmho	166 μmho
BW	24 MHz	24 MHz
PM ($A_{CL} = -1$)	74°	74°
I_{SUP}	93.8 μA (52.1 μA)	124.5 μA (87.3 μA)
Power Penalty	1	33% (68%)

can be much larger than the tail current, e.g., see [59]) are used, this data is enclosed within parentheses.

First considering the data not in parentheses, this table shows that the body-driven amplifier requires only 33% more supply current than the gate-driven amplifier. Again, this might seem surprising considering that the gate-driven input pair can achieve a transconductance efficiency that is fully three times higher than the body-driven pair. However, the key reason that the two solutions are so close is that the bias currents for

the gate-driven transistors had to be chosen based on slew rate considerations, which are independent of device transconductance efficiency. On the other hand, if one assumes that a class-AB output stage and a high slew rate input stage are used, then the body-driven amplifier requires 68% more current than the gate-driven amplifier. In the second case the bias currents are determined entirely by small-signal considerations, which is the theoretical minimum.

What then can be said, in general, about the power efficiency of a body-driven amplifier used in a high-resolution application? Clearly, determining the system-level power efficiency of a body-driven amplifier is a complex task. However, it seems clear that at least two general conclusions can be drawn. First, a body-driven amplifier used in a high-resolution application will have a lower power efficiency than a gate-driven amplifier. Second, the degree to which the body-driven amplifier will be less efficient is highly application dependent. However, perhaps the most important lesson that can be taken from this study is that using a body-driven amplifier in a high-resolution application, such as an ADC, will in many cases not require significantly more power dissipation than a gate-driven amplifier. Considering that a body-driven amplifier has never been applied in a pipeline or sigma-delta ADC (as of August 2005, based on the author's literature search), it is clear that more work needs to be done investigating how body-driven amplifiers can be applied to high-performance systems. Finally, it is also important to note that while the power efficiency of the body-driven amplifier is less than the gate-driven, body driving does provide at least two important advantages over gate driving for switched capacitor circuits.

- The use of the body-driven input pair allows the circuit to operate with input and output common-mode voltages of $V_{DD}/2$. Ultra-low voltage gate-driven switched-capacitor circuits must typically operate with an input common-mode level at V_{SS} or V_{DD} and then use common-mode level shifting to achieve an output common-mode level of $V_{DD}/2$.

- In highly scaled technologies gate-driven transistors may have much higher levels of input (i.e., gate) current than body-driven transistors.

6.2.3 Conclusion

Of all the drawbacks reported for body-driven transistors, that of reduced power efficiency is the most important to address. Generally speaking, there are so many different ways that an operational amplifier can be applied that it is impossible to always say that a body-driven amplifier will be a good or a bad choice in terms of power efficiency. However, as these two examples have shown, body-driven circuits can often achieve power efficiencies very close to that of gate-driven amplifiers. When this is coupled with the inherent advantages of body-driven circuit design, including the ability to operate at very low power supply voltages, it is clear that more research is warranted to study the application of body-driven circuits to high-performance analog systems of all kinds.

6.3 Body Driving with Absolute Minimum Circuits

While this chapter began by considering the most important drawbacks of body driving, it is equally important to consider the advantages. The overriding advantage of body driving is not only that it enables circuits to operate at the minimum supply voltage allowed

by a technology, it also enables significant functionality, including rail-to-rail input stages and regulated cascode current sources, at very low power supply voltages. As an example, the amplifier developed in this research implemented pMOS regulated cascode current sources at 1 V, while the threshold voltage was 0.85 V. Since all of the devices were operated with an IC of approximately 1, this means that the amplifier was operating at a power supply voltage of $|V_{TP}| + V_{DSAT}$. Since $|V_T| + V_{DSAT}$ is probably the minimum power supply voltage that any design technique will achieve, while still maintaining good performance, this shows that the body-driven techniques developed in this research enabled the design of a high-performance amplifier operating at the minimum supply voltage allowed by the technology. In considering the application of these design techniques to other circuit designs and especially other semiconductor technologies, it is important to answer the question, “what aspects of this research are technology independent and which are dependent on the specific technology used in this work.” In the rest of this section this topic will be addressed.

Adaptive gate biasing, examples of which are presented in Figures 5.4, 5.7, and 5.8, is the key low-voltage enabling design technique developed in this work, and it is applicable to any bulk CMOS or PD-SOI technology. However, there are at least two other low-voltage enabling design techniques used in this work: forward biasing the body of the nMOS output driver to increase the bias voltage on the pMOS load and thus increase the open-loop gain (described in Section 5.3.2.2), and the use of nMOS level-shifters in the pMOS bias circuitry (described in Section 5.4.1.3 and Figure 5.23). Of these two, the former is technology independent while the latter is not. The nMOS level shifters are technology dependent because they require a difference in nMOS and pMOS threshold

voltages (0.65 V versus 0.85 V) to maintain the pMOS devices in saturation. However, in many CMOS technologies the threshold voltages for the nMOS and pMOS devices will be nearly equal. In this case the design techniques presented thus far would only allow a circuit to operate at approximately $V_T + 2V_{DSAT}$. For the situation of a technology with nearly equal threshold voltages, new techniques will be required to enable fully functional circuits at operating voltages of $V_T + V_{DSAT}$.

To solve the problems just described, a modified form of adaptive gate biasing called absolute minimum biasing has been developed. The purpose of absolute minimum biasing is to enable body-driven circuits to operate at the absolute minimum power supply voltage possible within a given technology, assuming that the nMOS and pMOS threshold voltages are nearly equal. Unfortunately, this design technique was developed after the two amplifiers were submitted for fabrication, so no measurement results can be presented. However, simulation results will be presented, and considering the accuracy of the EKV model used in this work, the simulation results can be taken as very indicative of how the real circuit will perform. Figure 6.3 (a) presents a schematic of the standard bias circuitry for an nMOS cascode current source array and (b) presents the absolute minimum bias circuitry for the same current source array. In (a) one will notice that this circuit uses the same adaptive gate bias setup described in Figure 5.8. In part (b) all of the circuitry is the same except that body-driven diodes M_{B12} and M_{B13}, which are biased at the full saturation current I_{DSAT}, have been added. To understand the purpose of devices M_{B12} and M_{B13}, consider how the two circuits will perform as the power supply voltage is reduced close to $V_T + V_{DSAT}$. For the circuit of part (a) the pMOS current

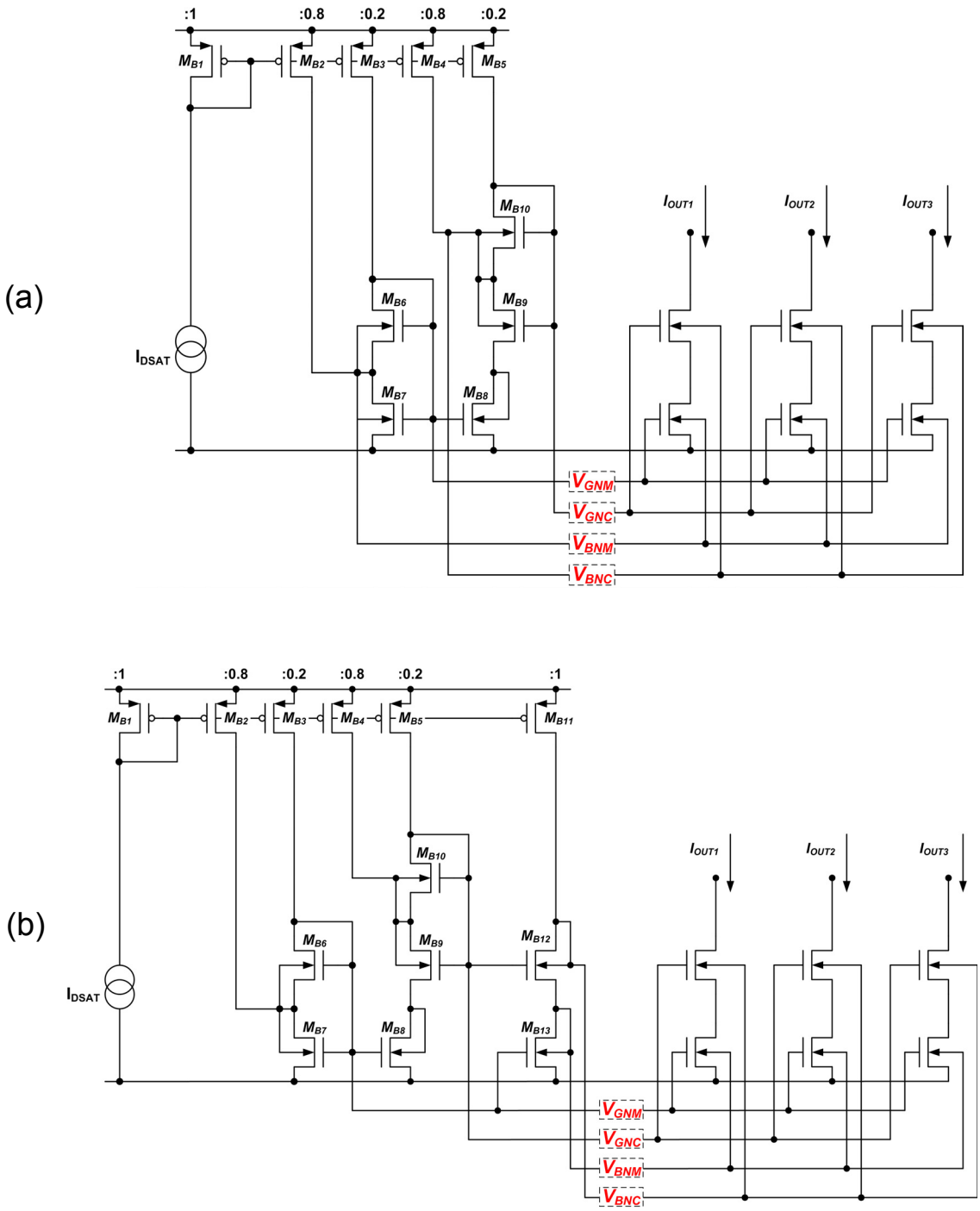

Figure 6.3: Bias circuitry for nMOS cascode current source array using (a) standard adaptive gate bias technique and (b) absolute minimum bias circuit

source M_{B5} will enter the Ohmic region, which will disturb the bias point of the circuit. On the other hand, in the circuit shown in part (b), the bias device M_{B5} will still enter the Ohmic region, and the gate bias for the nMOS cascode transistors will reach V_{DD} and saturate. However, the bias current will not be disturbed because the actual mirror branch is comprised of devices M_{B11}–M_{B13}. Since device M_{B11} is not driving a gate, it will remain in saturation even at very low power supply voltages and the bias point of the circuit will not be disturbed. Of course, the gate will no longer be biased at the optimum point which sets $V_{BS} = V_{DSAT}$. Instead the V_{BS} will now be larger than V_{DSAT}. However, this technique will allow the circuit to operate with a V_{DD} roughly one V_{DSAT} (probably a little more than 100 mV) lower than it otherwise could operate, which is significant at very low power supply voltages.

A second exciting application of the absolute minimum bias technique is in maintaining high open-loop voltage gain at low power supply voltages. Figure 6.4 presents a simplified schematic of the first and second gain stages for the Mysia amplifier, where the nMOS device on the left represents one half of the input differential pair, and the nMOS device on the right is the output driver M_1. As discussed in Section 5.3.2.2, one of the keys to achieving high open-loop gain is maximizing the output voltage $V_{P\text{-}SOURCE}$ on the pMOS current source. Upon first considering this circuit it seems that when operating at $V_{DD} = V_T + V_{DSAT}$ it will not be possible to achieve high open-loop gain because both of the pMOSFETs cannot remain in saturation. However, recall that to boost the gain the body of device M_1 was forward biased by approximately 300 mV, which increased the bias voltage across the pMOS current source by roughly 100 mV. In addi-

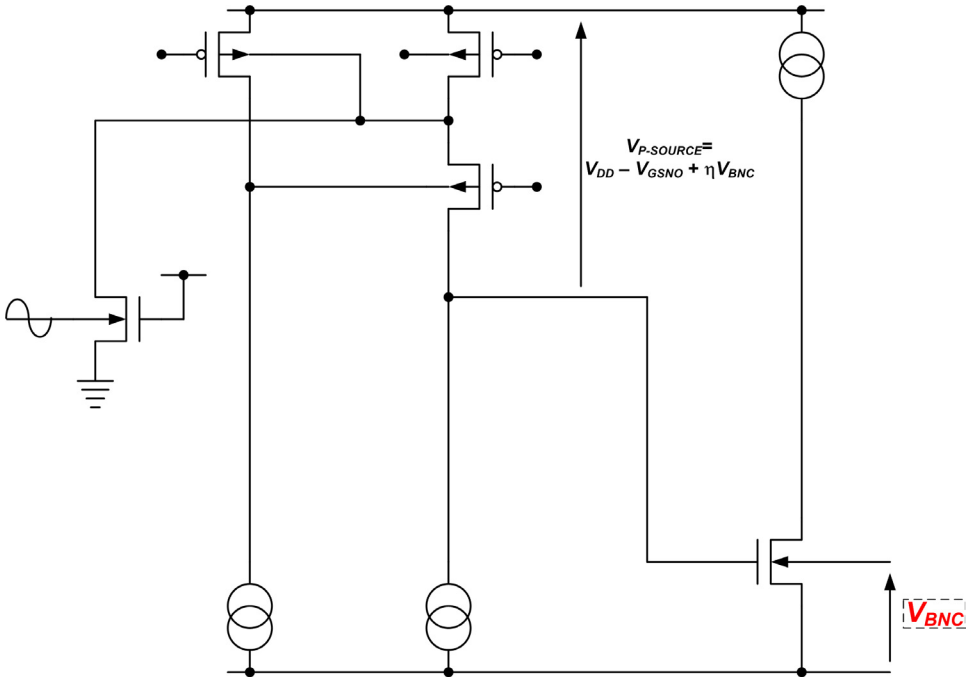

Figure 6.4: Simplified schematic of first and second amplifier gain stages

tion, the reference voltage generator for the 300-mV bias was simply the body bias for the nMOS cascode devices, which is labeled V_{BNC} in Figure 6.3.

With this in mind, now consider what the gain of the amplifier will do at very low voltages, say within the range

$$V_T + V_{DSAT} < V_{DD} < V_T + 2V_{DSAT}, \tag{6.26}$$

which is the key power supply region where it is especially difficult to build high-gain circuits. At $V_{DD} = V_T + 2V_{DSAT}$, the total voltage on the pMOS current source is given by

$$V_{P-Source}\Big|_{V_{DD} = V_T + 2V_{DSAT}} = V_{DD} - V_T + \eta V_{BNC} = \underline{2.67 V_{DSAT}}, \tag{6.27}$$

which is more than the minimum of $2V_{DSAT}$, and so is sufficient for achieving high open-loop gain. As V_{DD} is reduced below this level, the absolute minimum bias technique will maintain the bias currents at their correct level at least down to $V_{DD} = V_T + V_{DSAT}$, so the bias cell will not be disturbed in the V_{DD} region defined by Equation 6.26. Therefore it would seem that the key low-voltage problem is the voltage overhead on the current source will be reduced and the gain will be compromised. However, the absolute minimum bias circuit will actually compensate for the V_{DD} reduction and maintain a nearly constant $V_{P\text{-}Source}$ in the V_{DD} range defined by Equation 6.26. To understand how this works, refer to Figure 6.3 (b) and consider what the body bias for the nMOS cascode devices, labeled V_{BNC}, will do as V_{DD} is reduced. When V_{DD} is above $V_T + 2V_{DSAT}$, all devices in the bias cell are in saturation, and gate and body bias voltages for the nMOS cascode devices are equal to roughly $V_T + 2V_{DSAT}$ and $2V_{DSAT}$, respectively. As V_{DD} is reduced below $V_T + 2V_{DSAT}$, device M_{B5} will enter the Ohmic region and the gate bias for the nMOS cascode devices will clamp at roughly V_{DD}. In order to maintain the same bias current, the body bias for the nMOS cascode devices must increase to compensate for the reduced gate bias. For example, assume that V_{DD} has dropped by 50 mV, so that the gate bias on the nMOS cascodes is 50 mV lower than it should be. To maintain the same bias current the body of device M_{B12} must forward bias by roughly 150 mV (50 mV/η) to compensate. However, V_{BNC} is also the body bias for the nMOS output driver. This means that when V_{DD} drops by 50 mV the body bias of M_1 in Figure 6.4 will increase by 150 mV, and the threshold of M_1 will decrease by η times 150 mV, or 50 mV. Thus with the absolute minimum bias technique, the V_{GS} of M_1 will track V_{DD} in a way

that maintains a nearly constant $V_{P\text{-}Source}$ voltage, and hence maintains high gain at low power supply voltages.

To test the absolute minimum bias technique the custom generated 0.35-μm EKV model developed in this research was scaled to 0.18-μm, and the threshold voltages for both nMOS and pMOS devices was set to 0.5 V, which is meant to mimic the TSCM 0.18-μm process. In addition, the bias cell for the Macedonia amplifier, presented in Figure 5.25, was redesigned *as per* the absolute minimum bias technique. Figure 6.5 presents the schematic of the new bias cell. The new voltage bias generator was then used to bias the core Mysia amplifier shown in Figure 5.24, which was in no way changed for this simulation. Figure 6.6 presents the simulation results for the open-loop gain versus frequency and V_{DD} for this new amplifier. In this simulation the V_{DD} is stepped from 0.5 V to 1.0 V in 0.1-V steps. At V_{DD} values of 0.8 V, 0.9 V, and 1.0 V, the open-loop gain of the amplifier is close to 100 dB, while at 0.7 V (i.e., $V_T + 1.3V_{DSAT}$) the gain drops to 91 dB, and at 0.6 V (i.e., $V_T + 0.67V_{DSAT}$) the gain is 71 dB. In addition, the bandwidth is unchanged over the V_{DD} range 0.6–1.0 V, which attests to the fact that the absolute minimum bias technique is maintaining constant bias current over a wide V_{DD} range. Finally, the PSRR for this circuit was simulated using Monte Carlo techniques, and it was found that the PSRR at 0.6 V should be greater than 60 dB, while the PSRR above 0.8 V should be greater than 80 dB. These simulation results clearly show that body driving does enable high-performance circuits at the lowest power supply voltage supported by a given technology.

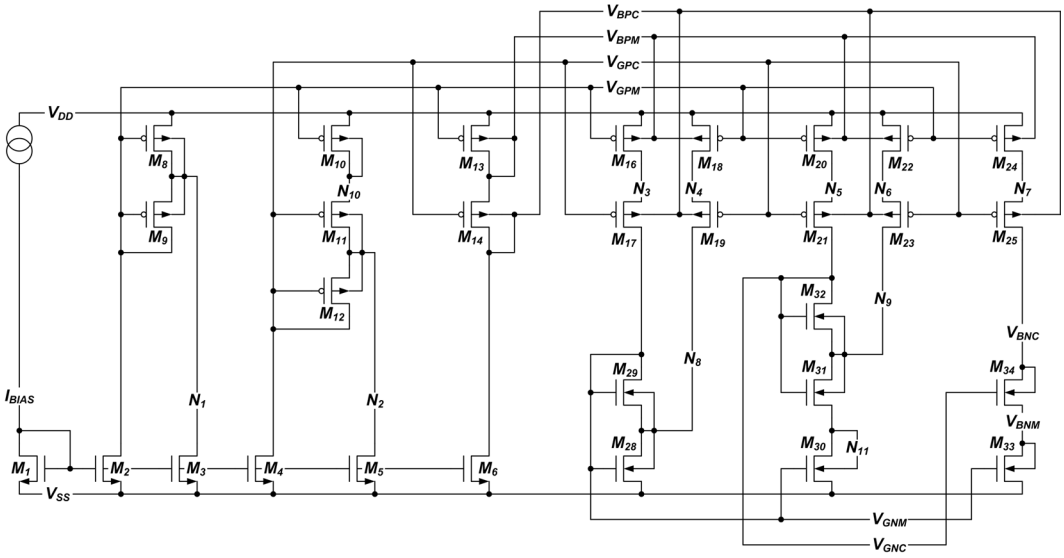

Figure 6.5: Amplifier bias cell developed using absolute minimum bias techniques

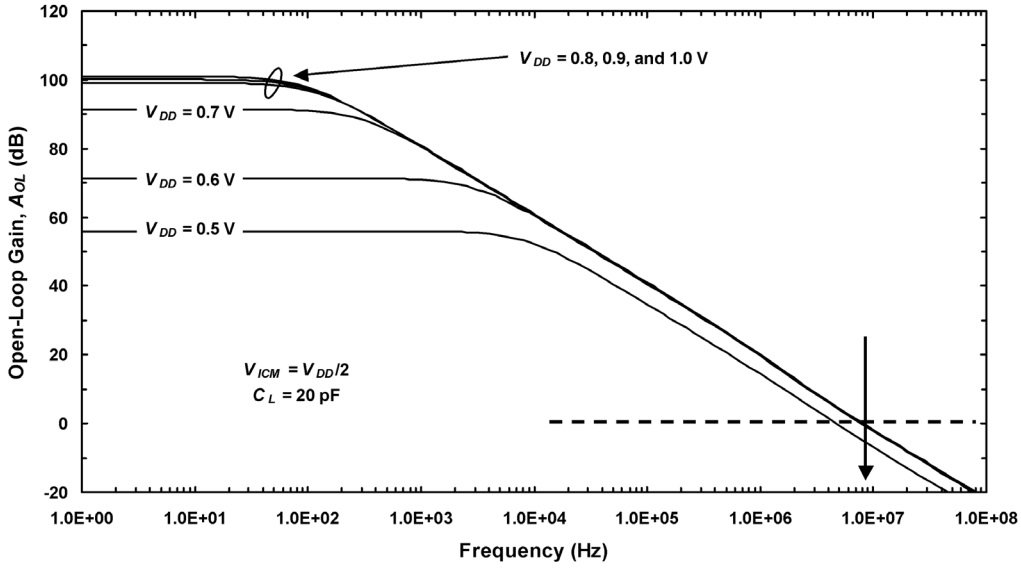

Figure 6.6: Simulated open-loop gain vs. frequency and V_{DD} for the core Mysia amplifier plus absolute minimum bias voltage generator

6.4 Body Driving and the Future of Analog Circuit Design

As a concluding note in this dissertation, this chapter has sought to address the question of where body driving can be applied to analog circuit designs and complex analog systems. Generally speaking, body driving is best applied in situations where it is of paramount important to achieve high-performance at very low power supply voltages. However, as shown by the amplifier developed in this research, body driving is versatile enough to enable high-performance circuits at the highest power supply voltages allowed by a given technology. Therefore body driving can also used to great effect in situations where an amplifier must operate over a wide range of power supply voltages, specifically including the minimum and maximum power supply voltages allowed by a given technology.

Another important question addressed in this chapter is the effect of body-driven transistors on amplifier power efficiency. To analyze the problem two specific cases were studied: the first was a two stage op-amp optimized to drive a large capacitive load, and the second was a two-stage op-amp optimized for high resolution and meant to be used in a pipeline ADC. In the first example it was shown that the use of a body-driven input pair has no effect on the power efficiency of the buffer, because the output stage, which must drive the large capacitive load, determines the power dissipation. In the second example it was shown that the body-driven amplifier required between 33% and 67% more supply current than the gate-driven amplifier, depending on the exact circuit configuration chosen. Therefore, it is not possible to conclusively say that body driving is a good choice or bad choice for all applications. However, what is perfectly clear is that body driving has great potential for a wide range of low-voltage applications. What is neces-

sary in the future is for designers to apply body-driven circuit techniques in different systems and find where they can be used to the greatest effect.

Chapter 7

Conclusion

7.1 Conclusion

CMOS technology scaling, which has continued in a consistent trend for the past thirty years, will soon force power supply and threshold voltages to their minimum allowable values. In addition, gate oxides will be so thin that in many cases the MOSFET gate will not represent a high input impedance. While several different design techniques have been developed to deal with these challenges, body driving is probably the least mature, but potentially most useful of all the available low-voltage design techniques. Therefore the goal of this dissertation was to develop new body-driven design techniques that would enable the construction of high-performance, low-voltage analog circuits.

The key design technique developed in this research is called adaptive gate biasing, which is a novel method for ensuring that the reference devices in a body-driven current mirror are biased in saturation, independent of current level, inversion level, temperature, or power supply voltage. The new adaptive gate bias technique was used to design a high-performance 1-V body-driven operational amplifier, which was fabricated on a 3.3-V/0.35-μm PD-SOI CMOS process that has nMOS and pMOS threshold voltages of 0.65 V and 0.85 V, respectively. The fabricated amplifier displayed an open-loop gain of 75 dB and a bandwidth of 9 MHz, but it also had a PSRR of only 20 dB at 1-V V_{DD}. To address the PSRR problem the amplifier was analyzed using Monte Carlo simulation techniques, and from this analysis several design changes were made. Next, a second body-driven

amplifier was fabricated, and this amplifier displayed an open-loop gain greater than 85 dB and a bandwidth of 9 MHz at 1-V V_{DD}. The new design achieved a PSRR at 1-V V_{DD} that was typically greater than 50 dB.

In addition to this work, the power efficiency of a body-driven amplifier was analyzed and it was shown that in many cases the use of a body-driven input pair would not result in a significant power penalty for analog circuits. Finally, a modified version of the adaptive gate bias technique, which is called absolute minimum biasing, has been proposed as an ultra-low-voltage enabling design technique for CMOS technologies whose nMOS and pMOS threshold voltages are nearly equal. Simulation results of an op-amp that uses the absolute minimum bias technique show that it is possible to achieve 90-dB open-loop voltage gain at 0.7-V V_{DD} using a technology that has 0.5-V thresholds. Taken together, the design techniques developed in this work represent an important contribution to the field of low-voltage analog circuit design, and they should pave they way for a host of new low-voltage, high-performance analog circuit applications.

7.2 Original Contributions of This Research

The original contributions of this research can be summarized as follows:

- a comparative study of the EKV and BSIM3V3 models for use in body-driven circuit design,
- the development of the adaptive gate bias technique for body-driven simple current mirrors,

- the application of the adaptive gate bias technique to body-driven cascode and regulated cascode current mirrors and current sources,

- the development of a high-performance body-driven operational amplifier that heavily leverages adaptive gate bias design techniques,

- Monte Carlo analysis of the PSRR of a body-driven op-amp, and

- the development of the absolute minimum bias technique and its application to an ultra-low voltage (< 0.8-V) operational amplifier.

7.3 Future Research Directions

In going forward with body-driven research there are a multitude of new directions which can be taken. Considering the op-amp alone, there are several opportunities:

- porting the op-amp to other semiconductor technologies using the absolute minimum bias technique,

- development of a low-voltage compatible class-AB output stage,

- use of complementary input pairs to maintain constant bandwidth over the input common-mode range,

- development of a technique for cancelling offset voltage by feeding correction signals to the MOSFET gates, and

- development of an offset correction technique that uses a charge pump approach that allows the gates of the input-pair MOSFETs to go above V_{DD}, which will allow a single pair to maintain constant g_{mb} over the entire input common-mode range.

In addition to the op-amp applications, there are many exciting system-level applications, including

- the use of body-driven amplifiers in ultra-low voltage (< 0.8 V) pipeline and sigma-delta ADCs,
- the use of body-driven transistors in developing very high-speed (> 1 GHz), low-voltage analog circuits,
- the use of body-driven transistors in extreme environments, including radiation and wide temperature range applications, and
- the use of body-driven transistors to create novel, ultra-low-voltage reference circuits.

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Appendices

Appendix A: Op-Amp Measurement Set-Ups

In this section the measurement setups for key op-amp tests will be described. Specifically, a description of those tests which the author feels will be the most helpful to the reader will be described.

A.1: Open-Loop Voltage Gain

The open-loop voltage gain of an op-amp is defined by the following equation

$$A_{OL} = \frac{V_{OUT}}{V_{\varepsilon}}, \qquad \text{A.1}$$

where V_{OUT} is the amplifier's output voltage, which is assumed to be zero when no input is present, and V_{ε} is the error voltage, which is also the amplifier's differential input voltage. Theoretically, open-loop gain is a straightforward measurement if one follows Equation A.1; practically, however, one is often limited by the resolution of the available test equipment. The fundamental difficulty in measuring open-loop gain is that one is trying to characterize the open-loop performance of the amplifier, while the amplifier must be kept in closed-loop configuration for reliable results to be obtained. Fortunately for this research project an SR770 network analyzer was available to the author, which enabled direct measurement of an amplifier's output voltage and error voltage.

The SR770 is an FFT network analyzer that has many important features that enable accurate measurement of the open-loop gain of amplifiers. First, the analyzer's data acquisition system consists of an 18-bit ADC, of which 16 bits are used, and provides a

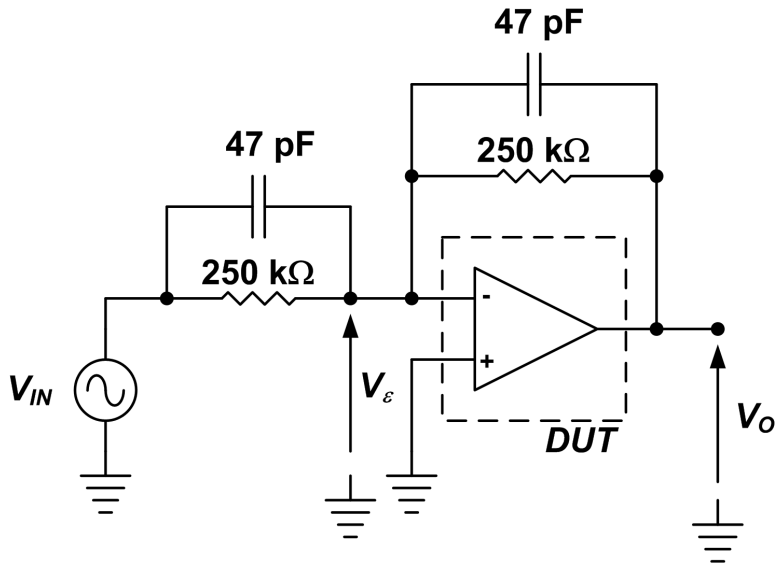

Figure A.1: Circuit for measuring open-loop gain

very high resolution voltage measurement. Second, the SR770 contains its own highly accurate sine-wave synthesizer which can be used as the op-amp input. Also, since the analyzer generates its own input, the generated sine wave is perfectly synchronized with the timing window of the FFT analyzer. This means that no window function is required for the FFT, and likewise no spectral leakage will occur from the FFT—this results in a very precise measurement of the op-amp's output.

Figure A.1 presents a schematic of the circuit used to measure open-loop voltage gain. Note that the op-amp is connected with an inverting closed-loop gain so that the common-mode level of the amplifier can be fixed, and therefore the finite open-loop gain can be differentiated from the finite CMRR. In addition, 250-kΩ feedback and input resistors are used so as not to load the op-amp's output. One problem with using such large resistors to achieve a closed-loop gain is that a low-frequency pole will be

generated between the input resistance and the op-amp's input capacitance, which could compromise stability. To cancel this effect, 47-pF input and feedback capacitors are included to provide a wideband closed-loop gain of –1. Since at high frequencies the feedback network is essentially capacitive, the input capacitance the op-amp's input capacitance will not affect stability. During a typical measurement, a 200-mV peak-to-peak sine was input to the amplifier, while the measured error signal could be as small as 6-μV peak-to-peak (given by 200 mV divided by the low-frequency open-loop gain of 90 dB).

A.2: Power Supply Rejection Ratio (PSRR)

PSRR is defined as the ratio of an op-amp's differential-mode gain to power supply gain, and can be written as

$$PSRR \equiv \frac{A_{DIFF}}{A_{PS}} = \frac{\frac{dV_{OUT}}{dV_{ID}}}{\frac{dV_{OUT}}{dV_{PS}}} = \frac{dV_{PS}}{dV_{ID}}. \qquad \text{A.2}$$

Equation A.2 states that DC PSRR is the inverse derivative of an amplifier's offset voltage versus power supply voltage characteristic. AC PSRR can be found by superimposing a small-signal sine wave on top of the power supply voltage, and then finding the ratio between the peak-to-peak power supply voltage and peak-to-peak amplifier offset voltage. In both cases it is assumed that the amplifier is connected in closed-loop configuration. Note also that what is important is the change in amplifier's offset voltage with power supply voltage, not the magnitude of the offset voltage. Figure A.2 presents a schematic of a circuit that can be used to characterize the DC PSRR. In this circuit the

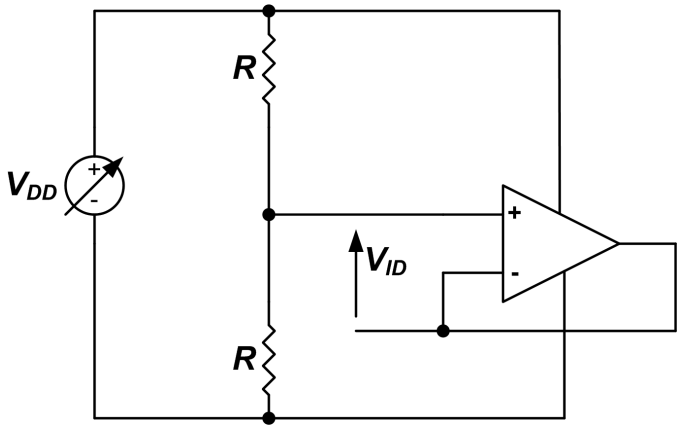

Figure A.2: Circuit for measuring PSRR

amplifier is connected as a unity-gain follower and the common-mode level is set $V_{DD}/2$. To measure PSRR the V_{DD} is swept and the amplifier's offset voltage is measured at each point. The PSRR can then be calculated as the inverse derivative of the V_{OS}–V_{DD} curve.

A.3: Common-Mode Rejection Ratio (CMRR)

The final measurement that will be described is CMRR, which is very similar to PSRR. CMRR is defined as

$$CMRR \equiv \frac{A_{DIFF}}{A_{CM}} = \frac{\frac{dV_{OUT}}{dV_{ID}}}{\frac{dV_{OUT}}{dV_{CM}}} = \frac{dV_{CM}}{dV_{ID}}. \qquad \text{A.3}$$

Similar to PSRR, DC CMRR can be measured by taking the inverse derivative of an amplifier's offset voltage versus common-mode voltage. A circuit for measuring DC CMRR is shown in Figure A.3. This circuit is useful because it allows one to arbitrarily set

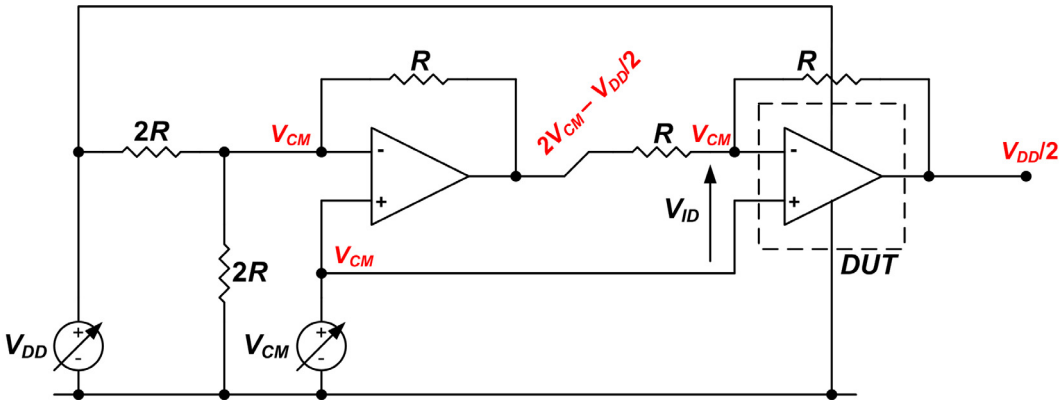

Figure A.3: Circuit for measuring CMRR (node voltages shown)

an op-amp's power supply and common-mode voltage, and have the output of the DUT be fixed at $V_{DD}/2$. Since the output is fixed for all common-mode levels, one can be certain to measure the change in offset due *only* to a change in common-mode level, and not to a change in the output voltage (i.e., a change in offset due to finite open-loop gain).

Vita

Stephen Christopher Terry was born in Abbington, Pennsylvania on August 16, 1978. He grew up in Germantown, Tennessee and graduated from Houston High School in 1996. Stephen earned the Bachelor of Science degree in Electrical Engineering in 2000 and the Master of Science degree in Electrical Engineering in 2002, both from the University of Tennessee. While a Master's student Stephen worked at both the Oak Ridge National Laboratory, Monolithic Systems Group, as a graduate research assistant involved in the development of high-temperature RF circuits, and at Concorde Microsystems (now Siemens Molecular Imaging) as a part-time consultant involved in the development of integrated circuits for medical imaging equipment.

Since January 2002 Stephen has been pursuing the Doctor of Philosophy degree with a major in Electrical Engineering at UT, under the advisement of Dr. Benjamin J. Blalock. While pursuing the Ph.D. Stephen has worked on a number of research projects, including a 2.5-V, 12-bit dual-slope ADC, a fully monolithic CMOS microluminometer, a simulation tool for time-domain noise analysis, wide-temperature range analog electronics, and ultra-low voltage amplifiers. During his time as a Ph.D. student Stephen been first author on eight conference papers and two journal papers. After graduation Stephen will join Agere Systems, Allentown, Pennsylvania, where he will work on the development of read-channel integrated circuits for hard disk drives.

Stephen is married to Rebecca Susan Terry, *nee* Moore, of Memphis, Tennessee.