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Active Harmonic Elimination in Multilevel Converters

Zhong Du
University of Tennessee - Knoxville

To the Graduate Council:

I am submitting herewith a dissertation written by Zhong Du entitled "Active Harmonic Elimination in Multilevel Converters." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

Leon M. Tolbert, Major Professor

We have read this dissertation and recommend its acceptance:

John N. Chiasson, Jack S. Lawler, Suzanne Lenhart

Accepted for the Council:
Dixie L. Thompson

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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Anne Mayhew

Vice Chancellor and
Dean of Graduate Studies

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Active Harmonic Elimination in Multilevel Converters

A Dissertation
Presented for the
Doctoral of Philosophy Degree
The University of Tennessee, Knoxville

Zhong Du

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Abstract

The modulation technique for multilevel converters is a key issue for multilevel converter control. The traditional pulse width modulation (PWM), space vector PWM, and space vector control methods do not completely eliminate specified harmonics. In addition, space vector PWM and space vector control method cannot be applied to multilevel converters with unequal DC voltages. The carrier phase shifting method for traditional PWM method also requires equal DC voltages. The number of harmonics that can be eliminated by the selective harmonic elimination method is restricted by the number of unknowns in the harmonic equations and available solutions.

For these reasons, this thesis develops a new modulation control method which is referred to as the active harmonic elimination method to conquer some disadvantages for the existing methods. The active harmonic elimination method contributes to the existing methods because it not only generates the desired fundamental frequency voltage, but also completely eliminates any number of harmonics without the restriction of the number of unknowns in the harmonic equations and available solutions for the harmonic equations. Also the active harmonic elimination method can be applied to both equal DC voltage cases and unequal DC voltage cases. Another contribution of the active harmonic elimination method is that it simplifies the optimal system performance searching by making a tradeoff between switching frequency and harmonic distortion.

Experiments on an 11-level multilevel converter validate the active harmonic elimination method for multilevel converters.

Table of Contents

List of Tables

List of Figures

1. Introduction

1.1. Background

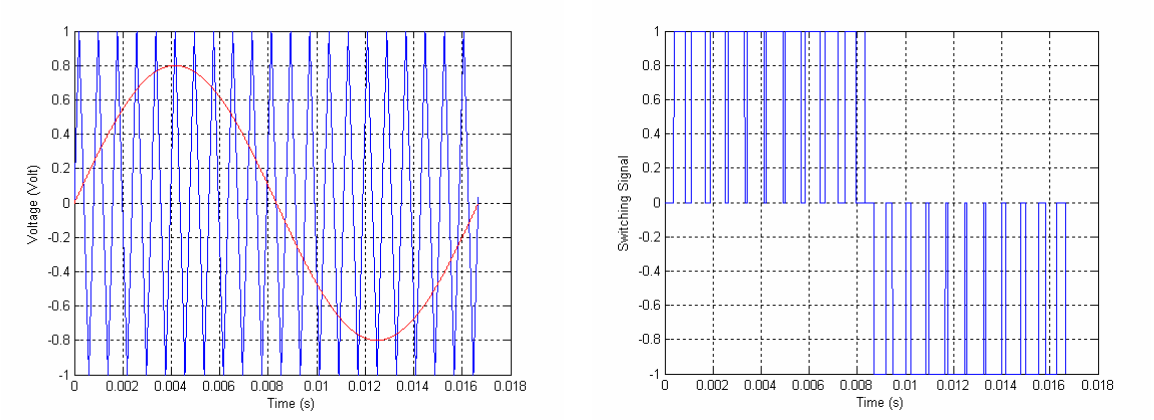
Electricity plays an important role in modern society since it was first used about one century ago. To utilize electricity for all kinds of tasks, many different electrical and electronic devices have been invented. Among these, the DC-AC converter is one of the most important power electronic devices.

One of the most widely used strategies for controlling the AC output of power electronic converters is the technique known as pulse width modulation (PWM), which varies the duty cycle of the converter switches at a high switching frequency to achieve a target average low-frequency output voltage or current. A traditional sine-triangle PWM is shown in Figure1.1.

Three significantly different PWM methods for determining the converter switching ON times have been usefully proposed for fixed-frequency modulation systems [1]. These PWM methods are:

1. Naturally sampled PWM: Switching at the intersection of a target reference waveform and a high-frequency carrier.
2. Regular sampled PWM: Switching at the intersection between a regularly sampled reference waveform and a high-frequency carrier.
3. Direct PWM: Switching so that the integrated area of the target reference waveform over the carrier interval is the same as the integrated area of the converter switched output.

Other PWM methods are variations of these three basic PWM methods. Even the well-known space vector modulation strategy, which is often claimed to be a completely different modulation approach, is really just a variation of regular sampled PWM which specifies the same switched pulse widths but places them a little differently in each carrier interval [1].



(a) (b)

Figure 1.1: Sine-triangle PWM control (a) sinusoidal reference signal and triangle carrier signal; (b) switching signal

In recent years, multilevel converters have been developed for several reasons.

1. Industry has begun to demand higher power equipment, which now reaches the megawatt level. Controlled AC drives in the megawatt range are usually connected to the medium-voltage network. Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids (such as 15 kV) [13].
2. Multilevel converters can solve problems with some present bi-level PWM adjustable-speed drives (ASDs). ASDs usually employ a front-end diode rectifier and a converter with PWM-controlled switching devices to convert the DC voltage to variable frequency and variable voltage for motor speed control. Motor damage and failure have been reported by industry as a result of some ASD converters' high-voltage change rates (dv/dt), which produce a common-mode voltage across the motor windings. High-frequency switching can exacerbate the problem because of the numerous times this common mode voltage is impressed upon the motor each cycle. The main problems are reported as "motor bearing failure" and "motor winding insulation breakdown" because of circulating currents, dielectric stresses, voltage surge, and corona discharge. The failure of some ASDs is because the voltage

change rate (dv/dt) sometimes can be high enough to induce corona discharge between the winding layers [2].

3. With the development of modern power electronic devices, these can switch at higher frequency and higher voltages, which can generate broadband electromagnetic interference (EMI). Although the high-frequency switching can increase the motor running efficiency and is well above the acoustic noise level, the (dv/dt) associated dielectric stresses between insulated winding turns are also greatly increased [2].

The multilevel converter is one of the more promising techniques for mitigating the aforementioned problems. Multilevel converters utilize several DC voltages to synthesize a desired AC voltage. For this reason, multilevel converters can reduce (dv/dt) to conquer the motor failure problem and EMI problem. Multilevel converters also have emerged as the solution for working with higher voltage levels. Multilevel converters include an array of power semiconductors and capacitor voltage sources, which generate output voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages.

One application for multilevel converters is distributed power systems. Multilevel converters can be implemented using distributed energy resources such as photovoltaic and fuel cells, and then be connected to an AC power grid. If a multilevel converter is made to either draw or supply purely reactive power, then the multilevel converter can be used as a reactive power compensator. For example, a multilevel converter being used as a reactive power compensator could be placed in parallel with a load connected to an AC system. This is because a reactive power compensator can help to improve the power factor of a load [14].

Another application for multilevel converters is to interconnect different power grids. For example, two diode-clamped multilevel converters can be used to produce such a system. One multilevel converter acts as a rectifier for the utility interface. The other multilevel converter acts as an converter to supply the desired AC load. Such a system can be used to connect two asynchronous systems and acts as a frequency changer, a

phase shifter, or a power flow controller.

1.2. Problem Statement

For many power converter applications, it is desirable for the converter to output a desired waveform with minimum distortion. For example, a DC-AC converter is desired to output a purely sinusoidal waveform. But for the practical converters, they can just output a series of rectangular waves. The key issues for the control of the converters are to get the modulation methods to control the output rectangular waves to synthesize the desired waveforms. Therefore, a modulation control method needs to generate desired fundamental frequency voltage and eliminate other higher order harmonics as much as possible.

After Jean Baptiste Joseph Fourier (1768 – 1830) discovered the Fourier Series, it is possible to represent periodic functions by an infinite sum of trigonometric functions that are harmonically related. In other words, each trigonometric term in this infinite series has a frequency equal to an integer multiple of the fundamental frequency of the original periodic function. To express these ideas in mathematical form, Fourier showed that a periodic function $f(t)$ could be expressed as

$$f(t) = a_0 + \sum_{n=1}^{\infty} c_n \cos\left(2\pi n f_o t + \varphi_n\right) \tag{1.1}$$

where n is the set of integer numbers $1,2,3,\ldots,\infty$, and φ_n is the initial phase for the n^{th} harmonic.

In (1.1), a_0 and c_n are called the Fourier coefficients. These terms are determined from $f(t)$. The term f_o is the fundamental frequency of the periodic function $f(t)$. The integer multiples of f_o, such as $2f_o$ and $3f_o$, are known as the harmonic frequencies of $f(t)$. Therefore, the term nf_o is the n^{th} harmonic of $f(t)$.

Today, the Fourier transformation method has been used to develop all kinds of modulation methods.

The most popular modulation method for bi-level converters is the PWM method. Traditional PWM methods employ switching frequencies on the order of several kHz.

The traditional PWM methods employ much higher switching frequencies for two reasons. The first reason concerns harmonics. Undesirable harmonics occur at much higher frequencies. Thus, filtering is much easier and less expensive. The second reason concerns audible noise. Several kHz is well above the acoustic noise level. Also, if the generated high frequency harmonics are above the bandwidth of some actual systems, there is no power dissipation due to these harmonics [14].

But as mentioned above, traditional PWM schemes have the inherent problems of producing electromagnetic interference (EMI). Rapid changes in voltages (dv/dt) are a source of EMI. The presence of a high dv/dt can cause damage to electrical motors. A high dv/dt produces common-mode voltages across the motor windings. Furthermore, higher switching frequencies can make this problem worse due to the increased number of times these common-mode voltages are applied to the motor during each fundamental cycle. Problems such as motor bearing failure and motor winding insulation breakdown can result due to circulating currents and voltage surges [2]. Also, long current-carrying conductors connecting equipment can result in a considerable amount of EMI.

Multilevel converters inherently tend to have a smaller dv/dt due to the fact that switching involves several smaller voltages. Furthermore, switching at the fundamental frequency will also result in decreasing the number of times these voltage changes occur per fundamental cycle.

The key issue for multilevel converter modulation is the harmonics elimination. The multilevel fundamental switching method inherently provides the opportunity to eliminate certain higher order harmonics by varying the times at which certain switches are turned "on" and turned "off", which is also called varying the switching angles. Harmonic elimination is performed for several reasons. The first reason is harmonics are a source of EMI. Without harmonic elimination, designed circuits would need more protection in the form of snubbers or EMI filters [14]. As a result, designed circuits would cost more. The second reason is that EMI can interfere with control signals used to control power electronics devices and radio signals. The third reason is that harmonics can create losses in power equipment. For example, harmonic currents in an electrical induction motor will dissipate power in the motor stator and rotor windings. There will

also be additional core losses due to harmonic frequency eddy currents. The fourth reason is that harmonics can lower the power factor of a load. Increased harmonic content will decrease the magnitude of the fundamental relative to the magnitude of the entire current. As a result, the power factor would decrease [14].

It was mentioned earlier that an increase in the number of DC voltages in a multilevel converter results in a better approximation to a sinusoidal waveform. Furthermore, the increased number of DC voltages provides the opportunity to eliminate more harmonic contents. Eliminating harmonic contents will make it easier to filter the remaining harmonic content. As a result, filters will be smaller and less expensive.

The second advantage of multilevel converters concerns switch ratings. Since multilevel converters usually utilize a large number of DC voltages, several switches are required to block smaller voltages. Since switch stresses are reduced, required switch ratings are lowered.

The third advantage of multilevel converters concerns system reliability. If a component fails on a multilevel converter, most of the time the converter will still be usable at a reduced power level. Furthermore, multilevel converters tend to have switching redundancies. In other words, there might be more than one way to produce the desired voltage [14].

The fourth advantage of multilevel converters concerns application practicality. As an example, consider designing a converter for a large HEV. Such an application would require excessively large components to deal with the relatively large working voltages and currents. These large components are expensive, bulky, and generally not reliable. However, multilevel converters allow for the utilization of smaller, more reliable components.

One disadvantage of multilevel converters is that they require more devices than traditional converters. The system cost may increase (part of the increased cost may be offset by the fact switches with lower ratings are being used). Using more devices also means the probability of a system failure will increase.

Another disadvantage of multilevel converters concerns control of the switches. The increased number of switches will result in more complicated control.

There are four kinds of control methods for multilevel converters. They are the selective harmonic elimination method, space vector control method, traditional PWM control method and space vector PWM method. The traditional PWM, space vector PWM and space vector modulation methods cannot completely eliminate harmonics. Another disadvantage is space vector PWM and space vector modulation methods can not be applied to multilevel converters with unequal DC voltages. The carrier phase shifting method for traditional PWM method also requires equal DC voltages. Until now, the number of harmonics the selective harmonic elimination method can eliminate is not more than the number of the switching angles in the transcendental equations. Due to the difficulty of solving the transcendental equations, real-time control of multilevel converters with unequal DC voltages is impossible now. No such method can be used to directly compute the output voltage pulses to eliminate any number of the harmonics without any restriction of the number of unknowns in the harmonic equations and available solutions for the equations.

For these reasons, in this thesis, a new modulation control method for multilevel converters is developed and referred to as the active harmonic elimination method.

The active harmonic elimination method contributes to the existing methods on it not only generates the desired fundamental frequency voltage, but also completely eliminates any number of the specified harmonics without the restriction of the number of unknowns in the harmonic equations and available solutions for the harmonic equations. Also the active harmonic elimination method can be applied to both equal DC voltage cases and unequal DC voltage cases. The method is referred to as the active harmonic elimination method because the converter itself can eliminate a specific harmonic. For a traditional bi-level converter, to eliminate a specific harmonic in the output voltage, a specific filter is required.

The second contribution of the active harmonic elimination method is it expands the scope of the traditional selective harmonic elimination method. In a traditional selective harmonic elimination method, the number of harmonics to be eliminated is limited by the unknowns in the harmonic equations and available solutions. If there are no solutions for some modulation index range, the traditional selective harmonic

elimination cannot be used. But for the active harmonic elimination method, if the harmonic equations have no solutions for a set of harmonics, they may have solutions for other sets of harmonics. The cost is just additional switchings.

The third contribution of the active harmonic elimination method is that it simplifies the optimal system performance searching by making a tradeoff between switching frequency and harmonic distortion since it can vary its switching frequency for different modulation indices.

The thesis is arranged as follows:

Chapter 2 presents a summary of the existing literature and the state-of–art in multilevel converter topologies and control technologies. The advantages and disadvantages of various multilevel converter topologies and control technologies are discussed. At the end of the chapter, a summary of "what is already done" and "what needs to be done next" will be given.

Chapter 3 explains the resultant method used to eliminate the low order harmonics for a multilevel converter, and develops the Newton Climbing method to eliminate higher order harmonics based on the harmonics elimination theory. The triplen harmonic compensation method to extend the modulation index range and decrease the required DC voltage level number is developed in this chapter, too.

Chapter 4 presents the active harmonic elimination method for equal DC voltage cases.

Chapter 5 extends the active harmonic elimination method for multilevel converters with unequal DC voltages.

Chapter 6 optimizes the active harmonic elimination method and improves its control performance. It can be seen in this chapter that the active harmonic elimination method dramatically expands the scope of the traditional selective harmonic elimination method.

Chapter 7 presents implementation of the active harmonic elimination method on an 11-level multilevel converter. Experiments validate the active harmonic elimination method.

Chapter 8 concludes the thesis's work and gives future research directions.

2. Literature Survey

In the previous chapter, the advantages and disadvantages of multilevel converters have been summarized briefly. Before going into system level studies, more information on the topologies and modulation techniques of multilevel converters is required to understand the systems research better. In this chapter, the present topologies and modulation techniques will be reviewed. Finally, a summary of previous research will be given and the remaining research work will be discussed.

2.1. Introduction

There are three main types of multilevel converters: diode-clamped, capacitor-clamped, and cascaded H-bridges [13]. The detailed advantages and disadvantages of the three multilevel converters will be discussed in this chapter.

Modulation techniques that have been proposed include traditional PWM method, space vector PWM method, space vector control method, and selective harmonics elimination method [13].

Applications that have been proposed include multilevel rectifiers, DC/DC converters, large motor drives, distributed energy applications (such as static volt-ampere reactive (VAR) compensation), back-to-back high-voltage intertie, and adjustable speed drives (ASD) [13].

2.2. Topology of Multilevel Converters

2.2.1. Diode-Clamped Converter

The simplest diode-clamped converter is commonly known as the neutral point clamped converter (NPC) which was introduced by Nabae *et al*. [4]. The NPC consists of two pairs of series switches (upper and lower) in parallel with two series capacitors where the anode of the upper diode is connected to the midpoint (neutral) of the capacitors and

its cathode to the midpoint of the upper pair of switches; the cathode of the lower diode is connected to the midpoint of the capacitors and divides the main DC voltage into smaller voltages, which is shown in Figure 2.1. In this example, the main DC voltage is divided into two. If the point *O* is taken as the ground reference, the three possible phase voltage outputs are -1/2V_{dc}, 0, or 1/2V_{dc}. The line-line voltages of two legs with the capacitors are: V_{dc}, 1/2V_{dc}, 0, -1/2V_{dc} or $-V_{dc}$. To generate a three-phase voltage, three phases are necessary.

The five-level output voltage can be generated by controlling the switches. Table 2-1 shows the proper switching states. The switches (S_{a1} and $S_{a'1}$) and (S_{a2} and $S_{a'2}$) are complementary pairs. When S_{a1} is on (S_{a1} = 1), $S_{a'1}$ is off ($S_{a'1}$ = 0). Other switch pairs are similar.

Figure 2.2 shows a two-phase diode-clamped multilevel converter.

Some disadvantages of the diode-clamped multilevel converter may be observed. Using extra diodes in series becomes impractical when the number of levels *m* increases, requiring *(m*-1*)(m*-2*)* diodes per phase if all the diodes have equal blocking voltages. Note that the voltages for diodes in different positions are not balanced. For example, diode D_{a2} must block two capacitor voltages, $D_{a(m-2)}$ must block *(m*-2*)* capacitor voltages. Also, the switch duty cycle is different for some of the switches requiring different current ratings. In addition, the capacitors do not share the same discharge or charge current resulting in a voltage imbalance of the series capacitors. The capacitor voltage imbalance can be controlled by using a back-to-back topology, connecting resistors in parallel with capacitors, or using redundant voltage states [4].

The advantages for the diode-clamped converter are the following:

(1) A large number of levels yields a small harmonic distortion.

(2) All phases share the same DC bus.

(3) Reactive power flow can be controlled.

(4) Control is simple.

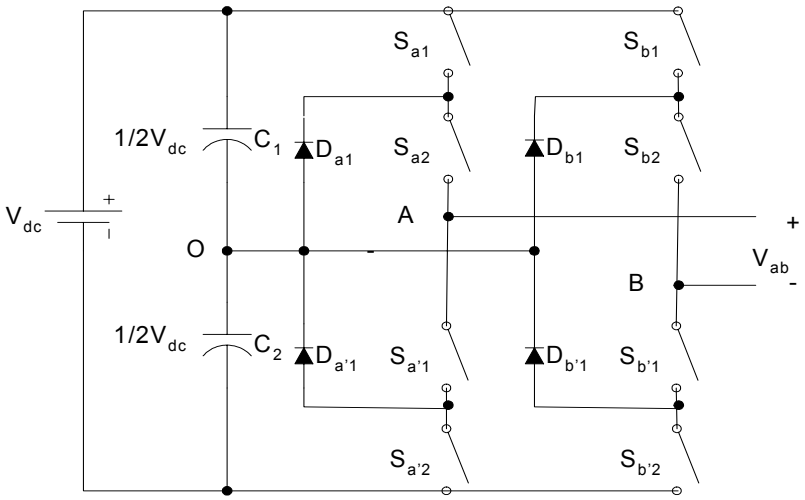


Figure 2.1: Neutral point diode-clamped converter

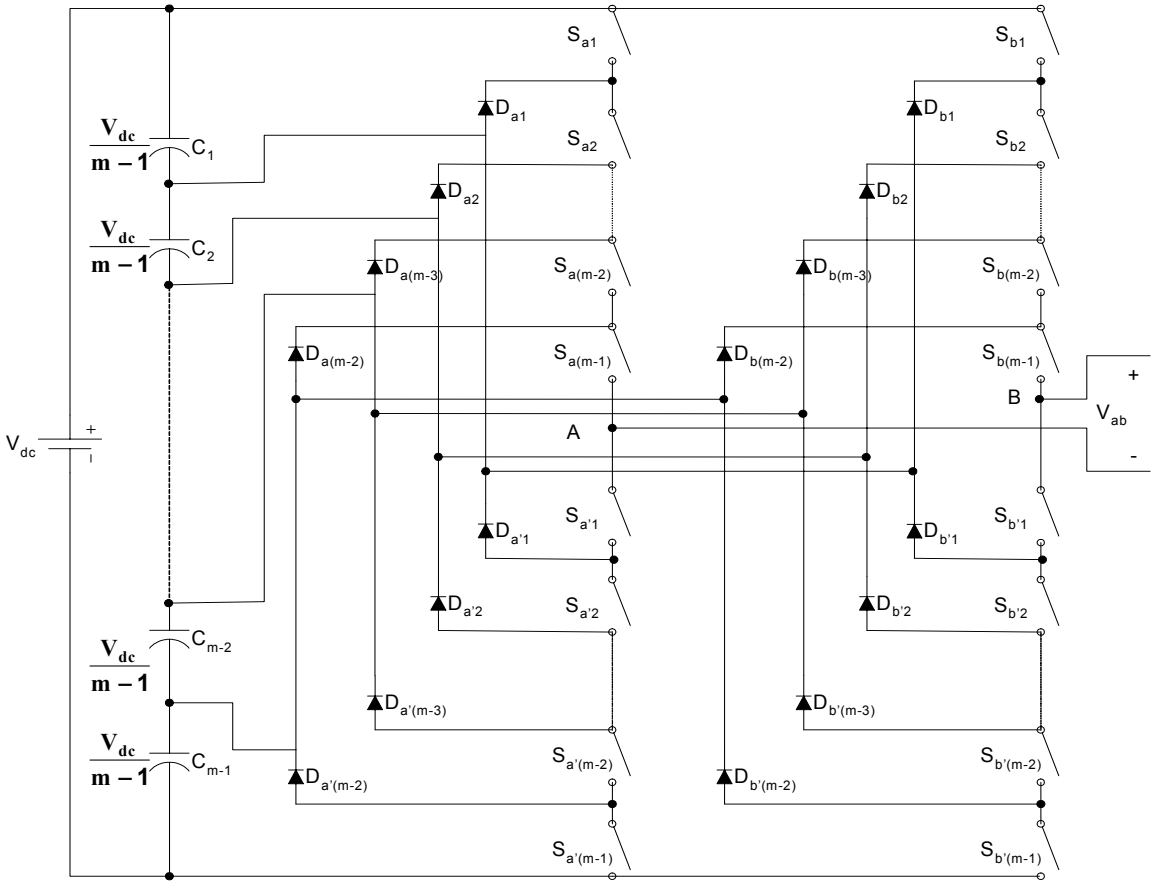


Figure 2.2: Two-phase diode-clamped multilevel converter

Table 2.1: Switch states and the output voltages for diode-clamped multilevel converter

S_{a1}	S_{a2}	$S_{a'1}$	$S_{a'2}$	S_{b1}	S_{b2}	$S_{b'1}$	$S_{b'2}$	V_{ao}	V_{bo}	V_{ab}
0	0	1	1	1	1	0	0	$-1/2V_{dc}$	$1/2V_{dc}$	$-V_{dc}$
0	0	1	1	0	1	1	0	$-1/2V_{dc}$	0	$-1/2V_{dc}$
1	1	0	0	1	1	0	0	$1/2V_{dc}$	$1/2V_{dc}$	0
0	0	1	1	0	0	1	1	$-1/2V_{dc}$	$-1/2V_{dc}$	0
0	1	1	0	0	0	1	1	0	$-1/2V_{dc}$	$1/2V_{dc}$
1	1	0	0	0	0	1	1	$1/2V_{dc}$	$-1/2V_{dc}$	V_{dc}

The disadvantages are the following:

(1) Different voltage ratings for clamping diodes are required.

(2) Real power flow is difficult because of the capacitors' imbalance.

(3) Different current ratings for switches are required due to their conduction duty cycle.

2.2.2. Capacitor-Clamped Converter

The capacitor-clamped multilevel converter or flying-capacitor converter [6], [12] is similar to the diode-clamped topology, which is shown in Figure 2.3. However, the capacitor-clamped multilevel topology allows more flexibility in waveform synthesis and balancing voltage across the clamped capacitors. For a three-level capacitor-clamped multilevel converter, if the *O* point is taken as the ground reference, a single phase can produce three output levels ($-1/2V_{dc}$, 0 and $1/2V_{dc}$). Likewise for the diode-clamped converter structure, a three-phase converter needs three phases.

The advantages of the capacitor-clamped multilevel converter are:

(1) Large *m* allows the capacitors extra energy during long discharge transient.

(2) Flexible switch redundancy for balancing different voltage levels

(3) A large number of levels yields a small harmonic distortion.

(4) Active and reactive power flow can be controlled.

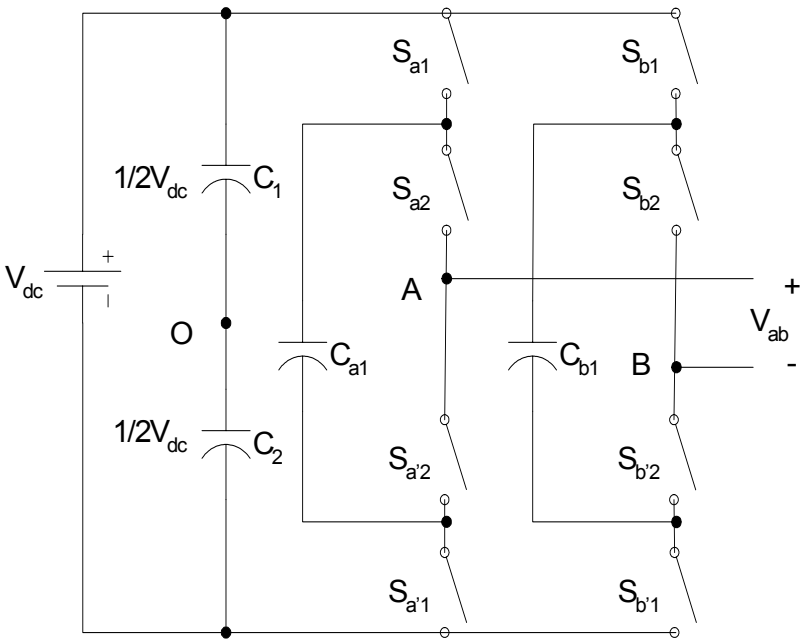


Figure 2.3: Topology of a capacitor-clamped multilevel converter

The disadvantages are:

(1) Large number of capacitors are bulky and more expensive than the clamping diodes used in the diode-clamped multilevel converter.

(2) Control for maintaining the capacitors' voltage balance is complicated.

(3) Poor switching utilization and efficiency for real power transmission.

Table 2.2 shows the possible switch combinations to generate the five-level output waveform. An output voltage can be produced by using different combinations of switches. The topology allows increased flexibility in how the majority of the voltage levels may be chosen. In addition, the switches may be chosen to charge or discharge the clamped capacitors, which balance the capacitor voltage.

The general m-level capacitor-clamped multilevel converter has an m-level output phase voltage. Thus, two phases would produce a $(2m-1)$ level output voltage, or line voltage, which is shown in Figure 2.4. Similar to the diode-clamped multilevel converter, the capacitors have different ratings. These capacitors result in a bulky, and expensive converter when compared to the diode-clamped converter.

Table 2.2: Switch states and the output voltages for capacitor-clamped multilevel converter

S_{a1}	S_{a2}	$S_{a'1}$	$S_{a'2}$	S_{b1}	S_{b2}	$S_{b'1}$	$S_{b'2}$	V_{ao}	V_{bo}	V_{ab}
0	0	1	1	1	1	0	0	$-1/2V_{dc}$	$1/2V_{dc}$	$-V_{dc}$
0	0	1	1	0	1	1	0	$-1/2V_{dc}$	0	$-1/2V_{dc}$
0	1	1	0	1	1	0	0	0	$1/2V_{dc}$	$-1/2V_{dc}$
1	0	0	1	1	1	0	0	0	$1/2V_{dc}$	$-1/2V_{dc}$
1	1	0	0	1	1	0	0	$1/2V_{dc}$	$1/2V_{dc}$	0
0	0	1	1	0	0	1	1	$-1/2V_{dc}$	$-1/2V_{dc}$	0
0	1	1	0	0	0	1	1	0	$-1/2V_{dc}$	$1/2V_{dc}$
1	1	0	0	0	1	1	0	$1/2V_{dc}$	0	$1/2V_{dc}$
1	0	0	1	0	0	1	1	0	$-1/2V_{dc}$	$1/2V_{dc}$
1	1	0	0	0	0	1	1	$1/2V_{dc}$	$-1/2V_{dc}$	V_{dc}

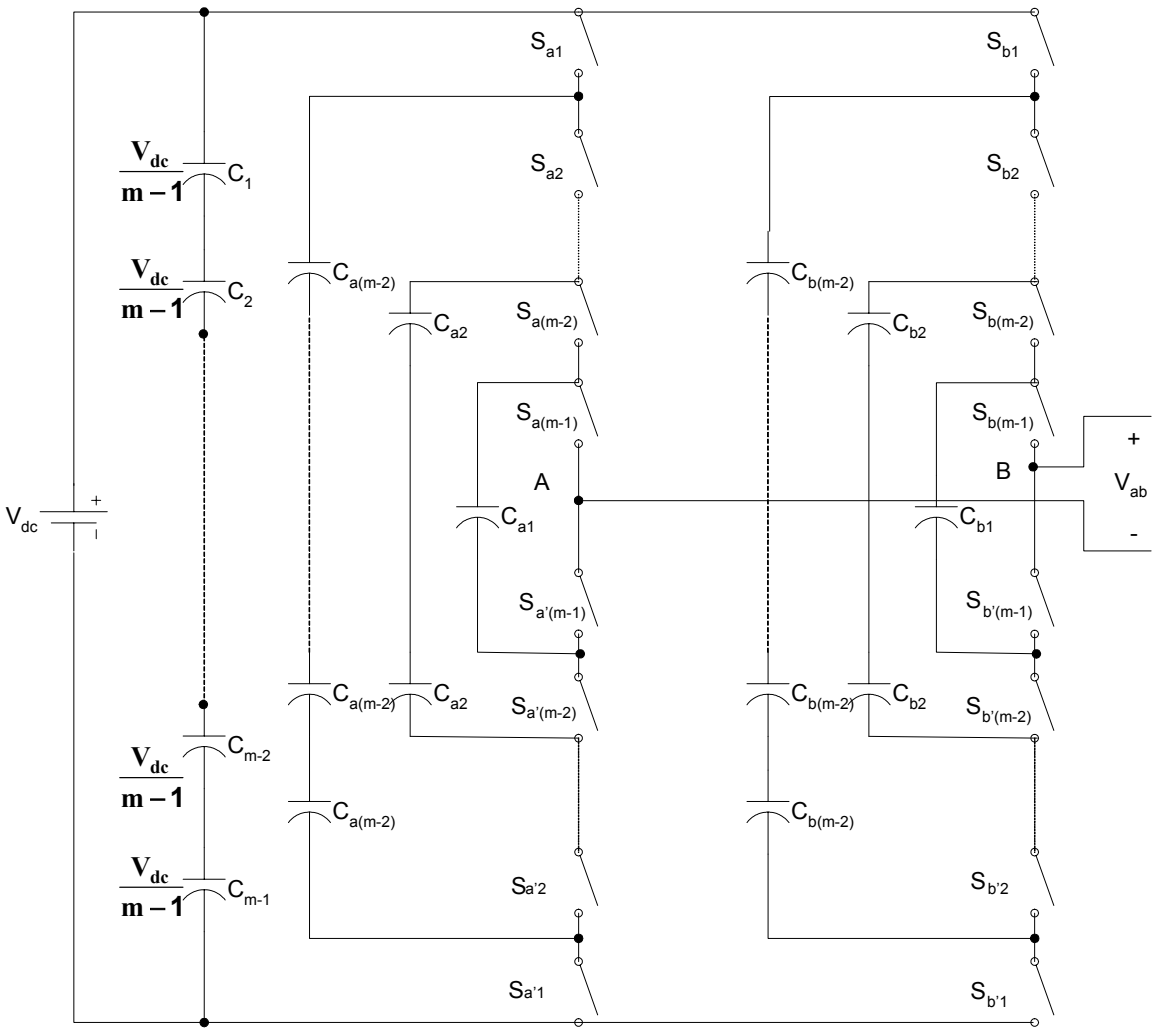


Figure 2.4: Two-phase capacitor-clamped multilevel converter

2.2.3. Cascaded H-bridge Converter

A cascaded H-bridge converter is several H-bridges in series configuration [2], [7], [8], [12]. A single H-bridge is shown in Figure 2.5.

A single H-bridge is a three-level converter. The four switches S_1, S_2, S_3 and S_4 are controlled to generate three discrete outputs V_{out} with levels V_{dc}, 0 and $-V_{dc}$. When S_1 and S_4 are on, the output is V_{dc}; when S_2 and S_3 are on, the output is $-V_{dc}$; when either pair S_1 and S_2 or S_3 and S_4 are on, the output is 0.

A H-bridge cascaded multilevel converter with s separate DC sources is shown in Figure 2.6.

A staircase sinusoidal waveform can be generated by combining specified output levels, which is shown in Figure 2.7. The number of output phase voltage levels m in a cascade converter with s separate DC sources is $m = 2s + 1$.

Load balance control for each H-bridge and each DC source can be acquired by rotating the switching angles to the H-bridges [2].

The advantages for cascaded multilevel H-bridge converter are the following:

(1) The series structure allows a scalable, modularized circuit layout and packaging due to the identical structure of each H-bridge.

(2) No extra clamping diodes or voltage balancing capacitors is necessary.

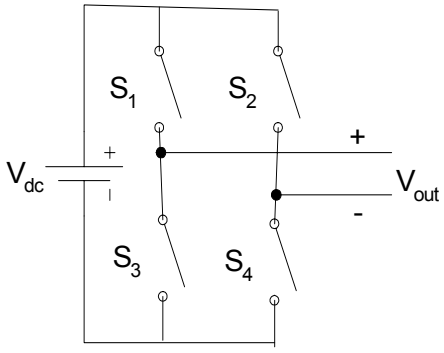


Figure 2.5: Single H-bridge topology

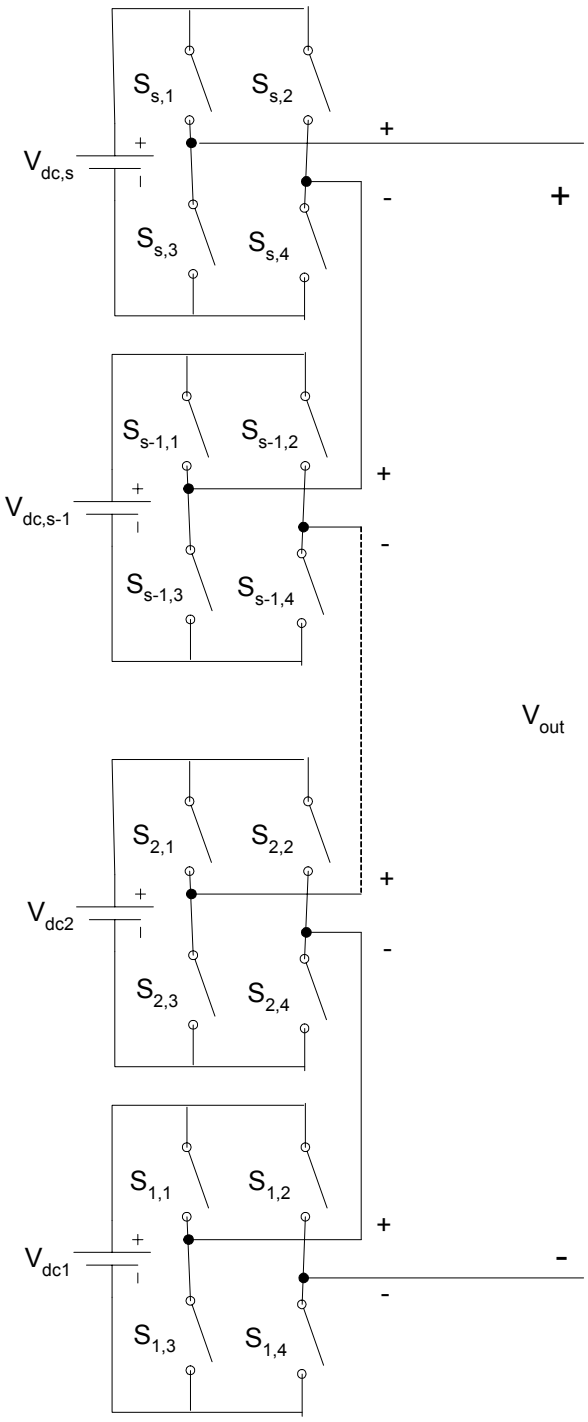


Figure 2.6: H-bridge cascaded multilevel converter with *s* separate DC sources

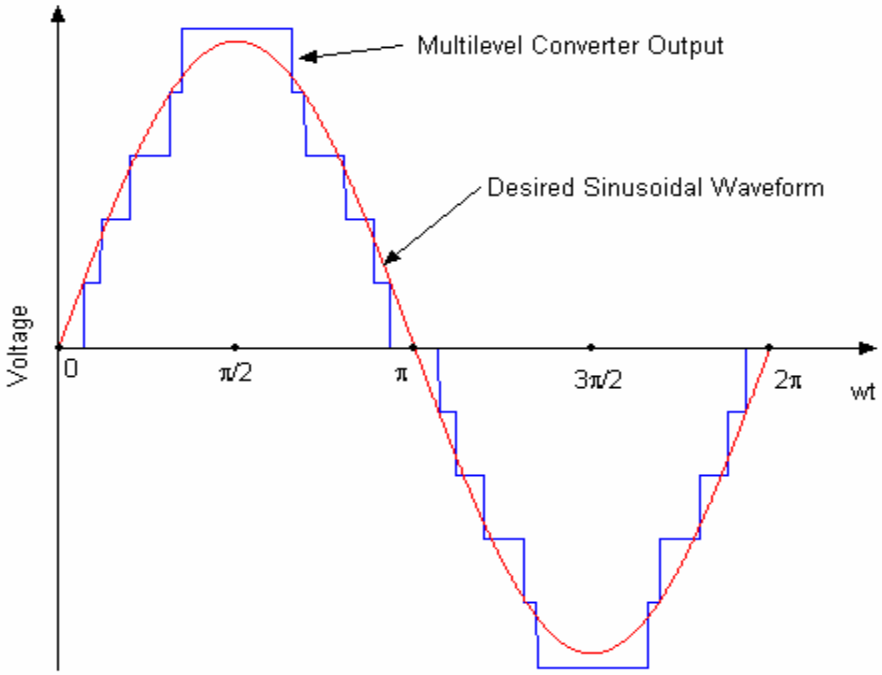


Figure 2.7: Staircase sinusoidal waveform generated by H-bridge cascaded multilevel converter

(3) Switching redundancy for inner voltage levels is possible because the phase voltage is the sum of each bridge's output.

The disadvantage for cascaded multilevel H-bridge converter is the following:

(1) Needs separate DC sources;

Another kind of cascaded multilevel converters with transformers using standard three-phase bi-level converters has recently been proposed [8]. The circuit is shown in Figure 2.8. The converter uses output transformers to add different voltages. In order for the converter output voltages to be added up, the outputs of the three converters need to be synchronized with a separation of 120° between each phase. For example, obtaining a three-level voltage between outputs *a* and *b*, the output voltage can be synthesized by $V_{ab} = V_{a1\text{-}b1}+V_{b1\text{-}a2}+V_{a2\text{-}b2}$. An isolated transformer is used to provide voltage boost. With three converters synchronized, the voltages $V_{a1\text{-}b1}$, $V_{b1\text{-}a2}$, $V_{a2\text{-}b2}$, are all in phase; thus, the output level can be tripled [13].

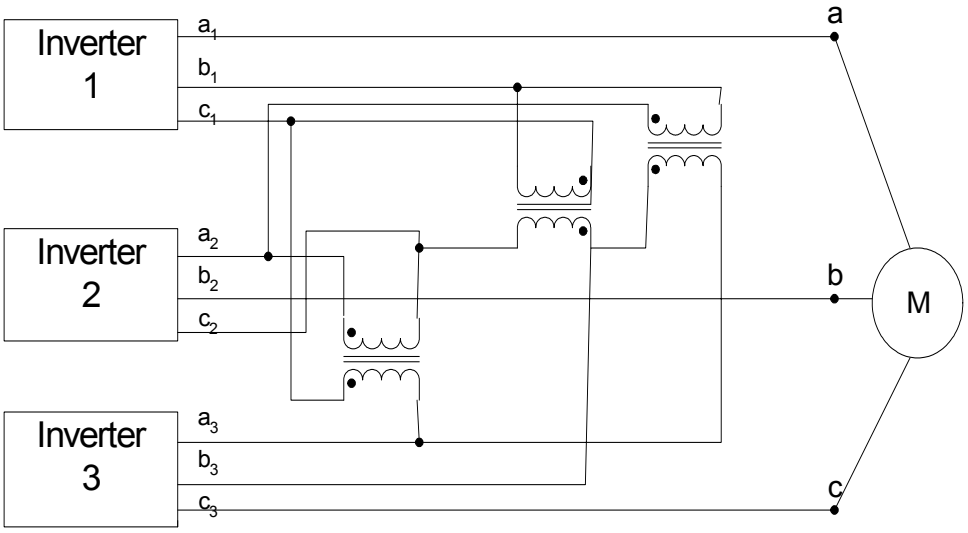


Figure 2.8: Cascaded multilevel converter with transformers using standard three-phase bi-level converters

The advantage for the cascaded multilevel converters with transformers using standard three-phase bi-level converters is the three converters are identical. So control would be simple. The topology has two disadvantages. The first is the three converters need separate DC sources; the second is it needs a transformer to add up the output voltages.

2.2.4. Cascaded DC Sources Multilevel Converter and Cascaded Transformers Multilevel Converter

There are other kinds of topologies for multilevel converters. Figure 2.9 is a cascaded DC sources multilevel converter [16]. The states of the switches S_{ia} and S_{ib} decide if the level is to be connected into the circuit. If S_{ia} is ON, S_{ib} is OFF: this level is connected into the circuit. If S_{ia} is OFF, S_{ib} is ON: this level is disconnected from the circuit. This topology is proposed for fuel cell applications. The output voltage of a fuel cell will decrease when the load increases, therefore control of the fuel cell number connected into the circuit can keep the output voltage constant [16].

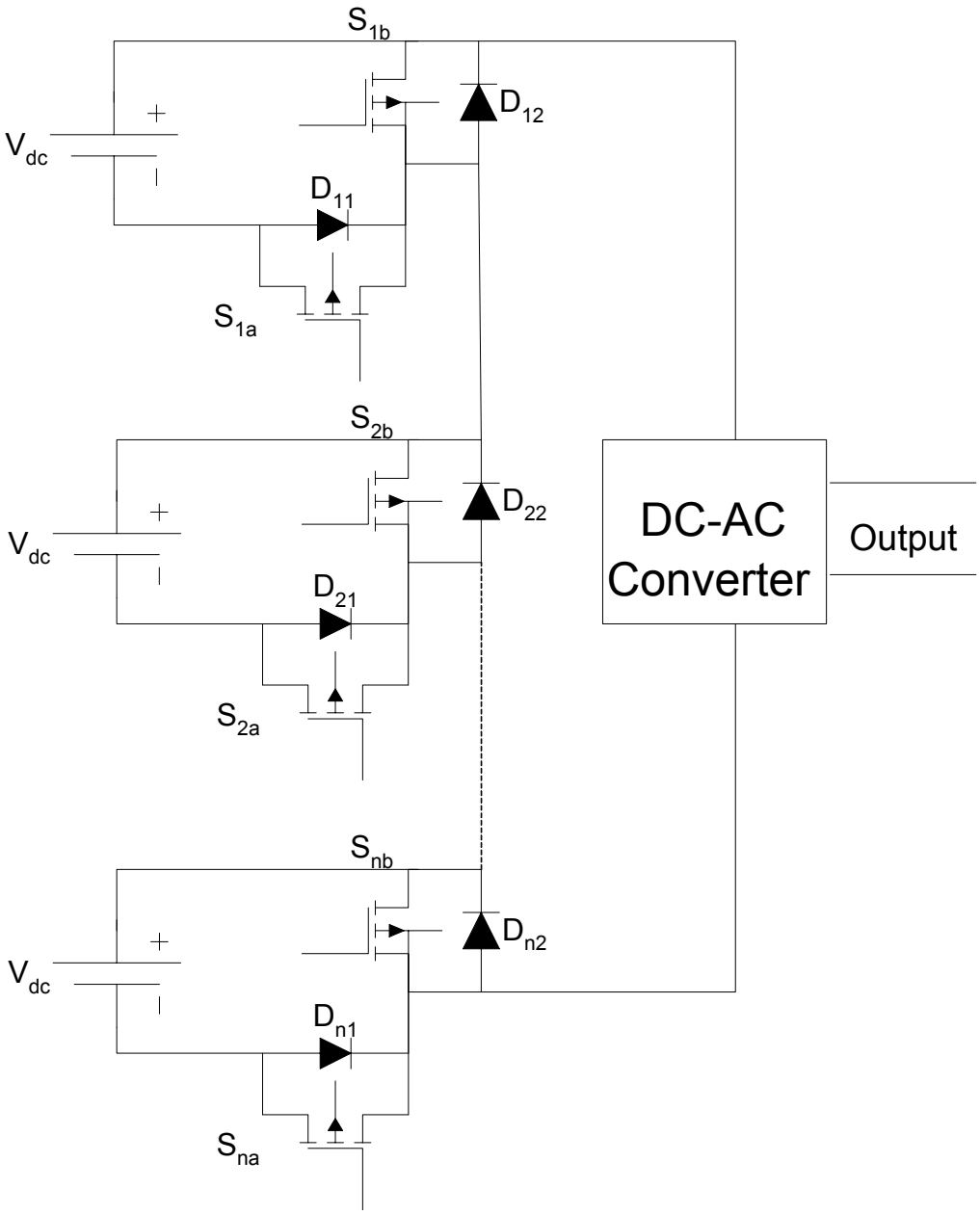


Figure 2.9: Topology of cascaded DC sources multilevel converters

The advantage of the topology is it can reduce the input voltage ripple for the output converter.

Another topology for multilevel converters is the cascaded transformer multilevel converter [15], which is shown in Figure 2.10.

This topology uses a single DC source and several transformers to generate high voltage output. The topology is similar to topology of the cascaded H-bridge multilevel converters [15].

The advantage for the topology is the system is simple and the converters could be identical. Therefore the control would be simple. Another advantage is that a single common DC voltage source is used. The disadvantage is that the system needs output transformers to add up the output voltages.

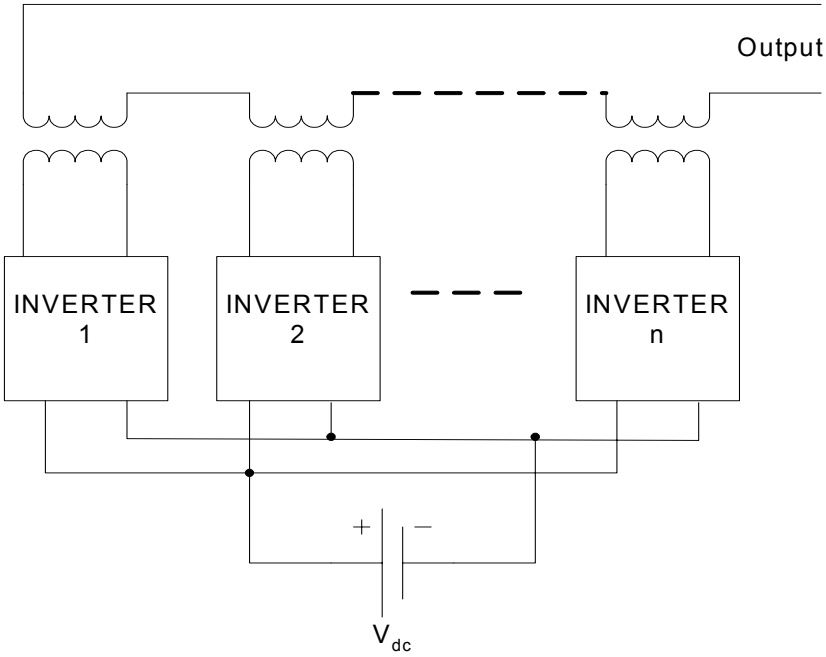


Figure 2.10: Topology of cascaded transformers multilevel converters

2.2.5. Generalized Multilevel Topology

Existing multilevel converters such as diode-clamped and capacitor-clamped multilevel converters can be derived from the generalized converter topology called *P2* topology proposed by Peng [9], which is shown in Figure 2.11. Moreover, the generalized multilevel converter topology can balance each voltage level by itself regardless of load characteristics, active or reactive power conversion, and without any assistance from other circuits at any number of levels automatically. Thus, the topology provides a complete multilevel topology that embraces the existing multilevel converters in principle.

Figure 2.11 shows the *P2* multilevel converter structure per phase leg. Each switching device, diode, or capacitor's voltage is 1 V_{dc}, i.e., 1*/(m*-1*)* of the DC-link voltage. Any converter with any number of levels, including the conventional bi-level converter can be obtained using this generalized topology [13].

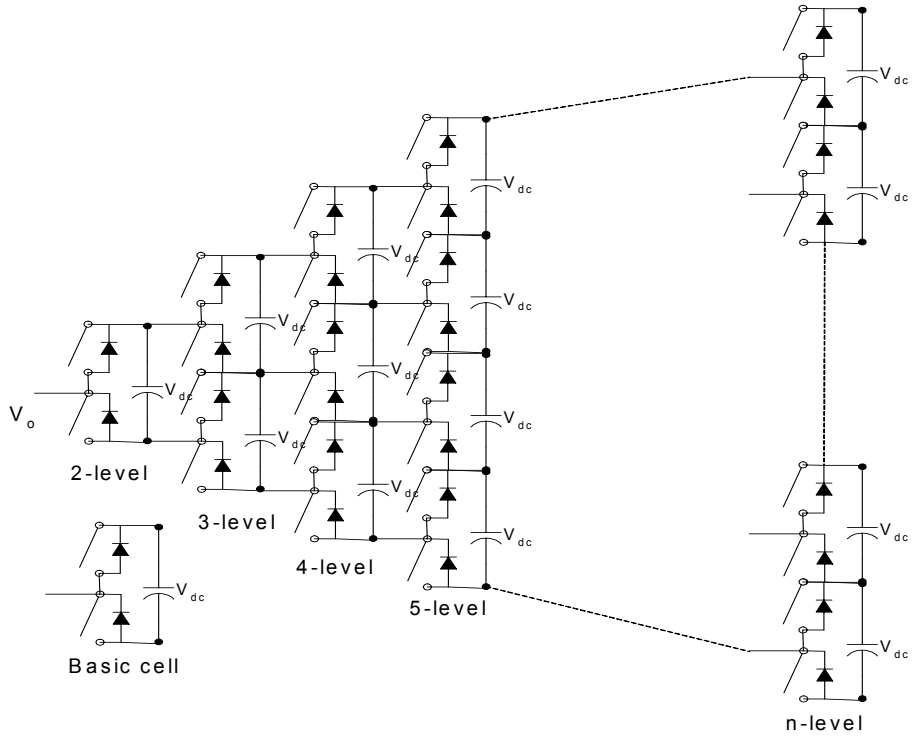


Figure 2.11: Generalized P2 multilevel converter topology

2.2.6. Mixed-Level Hybrid Multilevel Converter

To reduce the number of separate DC sources for high-voltage, high-power applications with multilevel converters, diode-clamped or capacitor-clamped converters can be used to replace the full-bridge cell in a cascaded converter [10]. An example is shown in Figure 2.12. The nine-level cascade converter incorporates a three-level diode-clamped converter as the cell. The original cascaded H-bridge multilevel converter requires four separate DC sources for one phase leg and twelve for a three-phase converter. If a five-level converter replaces the full-bridge cell, the voltage level is effectively doubled for each cell. Thus, to achieve the same nine voltage levels for each phase, only two separate DC sources are needed for one phase leg and six for a three-phase converter.

The configuration has mixed-level hybrid multilevel units because it embeds multilevel cells as the building block of the cascade converter.

The advantage of the topology is it needs less separate DC sources. The disadvantage for the topology is its control will be complicated due to its hybrid structure.

2.2.7. Unequal DC Sources Multilevel Converter

For some applications, it is possible to have different voltage levels among the cells [11]. Therefore the circuit can be called an unequal DC sources multilevel converter. The voltage levels depend on the availability of DC sources. This feature allows more possible output voltage levels to be produced, and thus it is possible to reduce the harmonic contents with less cascade cells required. For example, in Figure 2.13, V_{dc1}, V_{dc2},… V_{dcs} can be different from each other. This kind of topology is also called asymmetric cascade multilevel converters [13].

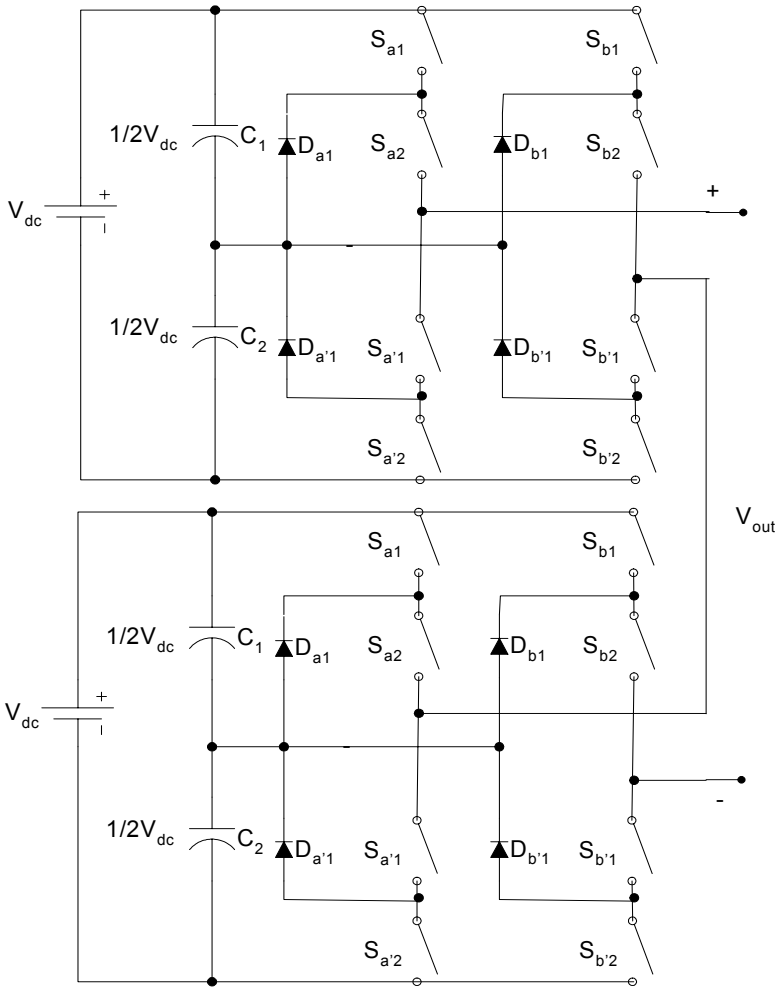


Figure 2.12: Mixed-level hybrid unit configuration using the three-level diode-clamped converter as the cascaded converter cell to increase the voltage levels

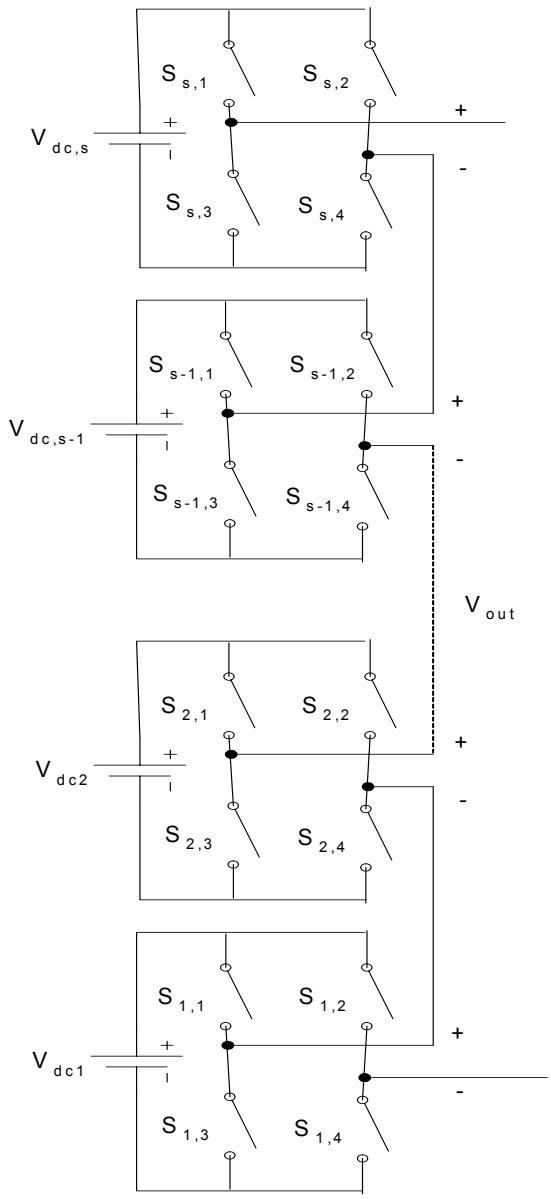


Figure 2.13: Unequal DC sources multilevel converter

Although it is possible to reduce the harmonic contents with less cascaded cells required for unequal DC sources multilevel converters, the control for unequal DC sources multilevel converters is very complicated. Until now, most of the available control methods are for equal DC sources multilevel converters. This is its main disadvantage.

2.2.8. Soft-Switched Multilevel Converter

Several soft-switching methods can be implemented for different multilevel converters to reduce the switching loss and to increase efficiency. For the cascaded converter, because each converter cell is a bi-level circuit, the implementation of soft switching is not at all different from that of conventional bi-level converters. For capacitor-clamped or diode-clamped converters, soft-switching circuits have been proposed with different circuit combinations. One of them is zero-voltage-switching types including auxiliary resonant commutated pole (ARCP), coupled inductor with zero-voltage transition (ZVT), and their combinations. [13].

2.3. Control and Modulation Techniques of Multilevel Converters

2.3.1. Classification of Modulation Strategies

The modulation methods used in multilevel converters can be classified according to switching frequency [13], [24], [25], as shown in Figure 2.14. Methods that work with high switching frequencies have many commutations for the power semiconductors in one cycle of the fundamental output voltage.

The popular methods for high switching frequency methods are classic carrier-based sinusoidal PWM (SPWM) [7], [26] and space vector PWM. The popular methods for low switching frequency methods are space vector modulation (SVM) method and selective harmonic elimination method.

A very popular method with high switching frequency in industrial applications is the classic carrier-based sinusoidal PWM (SPWM) that uses the phase-shifting technique to increase the effective switching frequency. Therefore, the harmonics in the load voltage can be reduced [27].

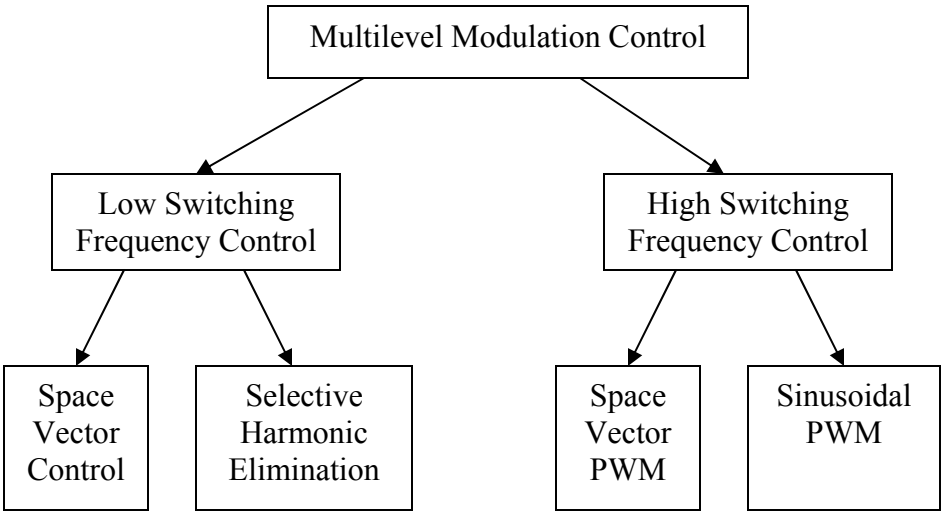


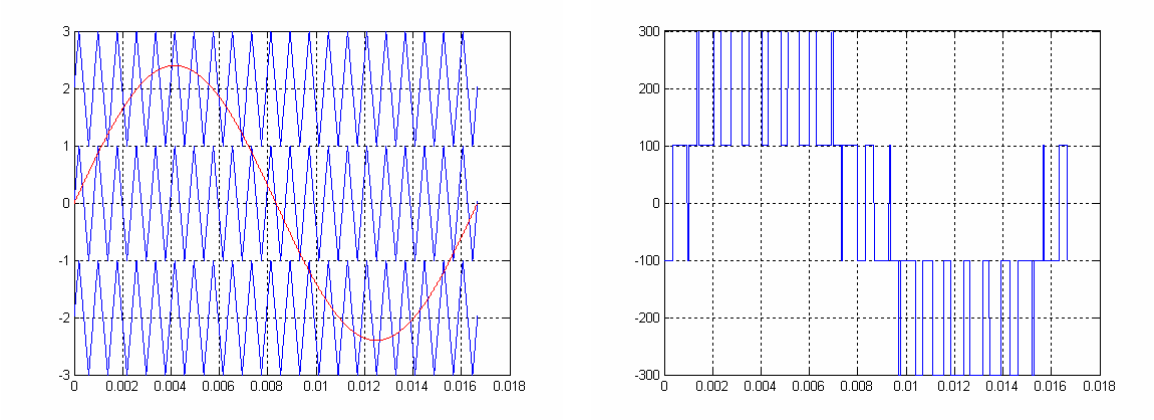
Figure 2.14: Classification of multilevel modulation methods

Another interesting method is the SVM strategy [24], which has been used in three-level converters. Methods that work with low switching frequencies generally perform one or two commutations of the power semiconductors during one cycle of the output voltages to generate a staircase waveform. Representatives of this family are the multilevel selective harmonic elimination [30], [31] based on elimination theory [3], [28], [29] and the space-vector control (SVC) [32].

2.3.2. Multilevel SPWM

Multilevel SPWM usually needs multiple carriers. Each DC source needs its own carrier. Several multi-carrier techniques have been developed to reduce the distortion in multilevel converters, based on the classical SPWM with triangular carriers. Some methods use carrier disposition and others use phase shifting of multiple carrier signals [12], [26], [33], [34].

This common SPWM method is the extension of bi-level SPWM. One reference signal is used to compare to the carriers. This can be shown in Figure 2.15 (a). If the reference signal is higher than the carrier, the corresponding converter cell outputs positive voltage; otherwise, the corresponding converter cell outputs negative voltage. The output voltage of the converter is shown in Figure 2.15 (b).



(a) (b)

Figure 2.15: Multi-carrier control (a) control signal and carrier signals; (b) output voltage

A number of cascaded cells in one phase with their carriers shifted by an angle and using the same control voltage produce a load voltage with the smallest distortion [27]. The effect of this carrier phase-shifting technique can be clearly observed in Figure. 2.16. This result has been obtained for the multi-cell converter in a seven-level configuration, which uses three series-connected cells in each phase. The smallest distortion is obtained when the carriers are shifted by an angle of 120°. A very common practice in industrial applications for the multilevel converter is the injection of a third harmonic in each cell to increase the output voltage [7], [10]. Another advantageous feature of multilevel SPWM is that the effective switching frequency of the load voltage is much higher than the switching frequency of each cell, as determined by its carrier signal.

The advantage of the method is it is very simple. But it has two disadvantages. The first is the method cannot completely eliminate the low order harmonics. Therefore the low order harmonics cause loss and high filter requirements. The second is the high switching frequency causes high switching loss and low efficiency.

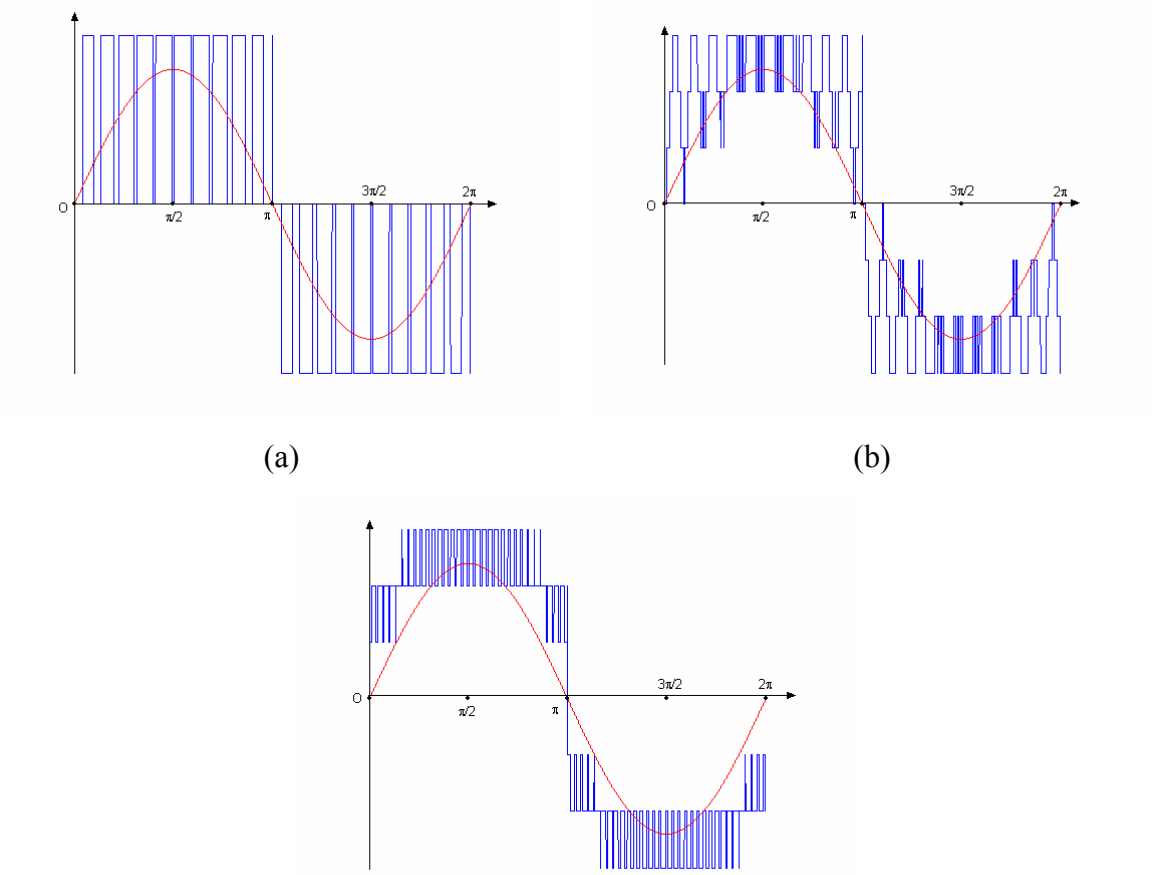


Figure 2.16: Output voltage with carrier phase shift (a) phase shift 0°; (b) phase shift 90°; (c) phase shift 120°

2.3.3. Space Vector PWM Modulation

The space vector PWM modulation technique is popular for bi-level PWM converter control. It can be extended to multilevel converters [35]-[41]. Figure. 2.17 shows space vectors for the traditional three-, five-, and seven-level converters. These vector diagrams are universal regardless of the topology of multilevel converter. Therefore it can be used for diode-clamped, capacitor-clamped, or cascaded converters. The adjacent three vectors can synthesize a desired voltage vector by computing the duty cycle for each vector according to the following:

$$\vec{V}^{*} = \frac{T_j \vec{V}_j + T_{j+1} \vec{V}_{j+1} + T_{j+2} \vec{V}_{j+2}}{T} \tag{2.1}$$

Space-vector PWM methods generally have the following advantages:

(1). Good utilization of DC-link voltage, low current ripple.

(2). Control is relatively easy, the hardware implementation can be easy by a digital signal processor (DSP).

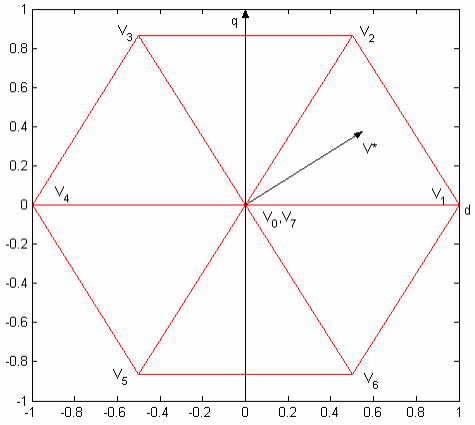
These advantages make it popular for converter control. But one disadvantage is as the number of levels increases, redundant switching states and the complexity of selecting switching states increase dramatically [13]. Another disadvantage is it cannot completely eliminate the low order harmonics.

To conquer the computation difficulty, some authors have used decomposition of the five level space-vector diagram into two three-level space-vector diagrams with a phase shift to minimize ripples and simplify control [38].

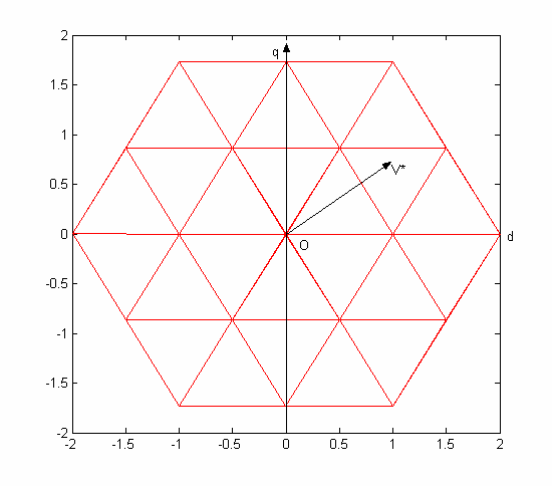
Additionally, a simple space-vector selection method, which was called space-vector control method, is introduced for multilevel converter control without duty cycle computation of the adjacent three vectors.

2.3.4. Space Vector Control

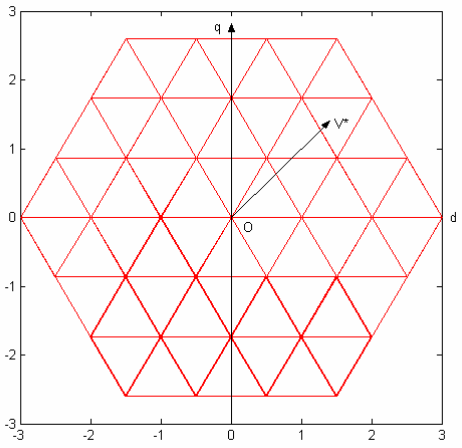
A conceptually different control method for multilevel converters, based on the space-vector theory, has been introduced, which is called space vector control (SVC) [25].



(a)



(b)



(c)

Figure 2.17: Space vector diagram (a) three-level; (b) five-level; (c) seven-level

The control strategy works with low switching frequencies but does not generate the mean value of the desired load voltage in every switching interval, which is the principle of space-vector PWM method. Figure. 2.18 shows the 311 different space vectors generated by a 21-level converter. The reference load voltage vector is also included in this figure. The key idea in SVC is to deliver to the load a voltage vector that minimizes the space error or distance to the reference vector. The high density of vectors produced by the 11-level converter will generate only small errors in relation to the reference vector; it is, therefore, unnecessary to use a more complex modulation method involving the three vectors adjacent to the reference. The hexagon of Figure 2.18 is the boundary of highest proximity, when the reference voltage is located in this area, the vector can be selected. Then the vector that has the greatest proximity to the reference is chosen. This method is simple and attractive for high number of levels. The advantages of SVC are the computation is very easy and the switching frequency is very low, near the fundamental switching frequency. But the disadvantage is as the number of levels decreases, the error in terms of the generated vectors with respect to the reference will be higher [13].

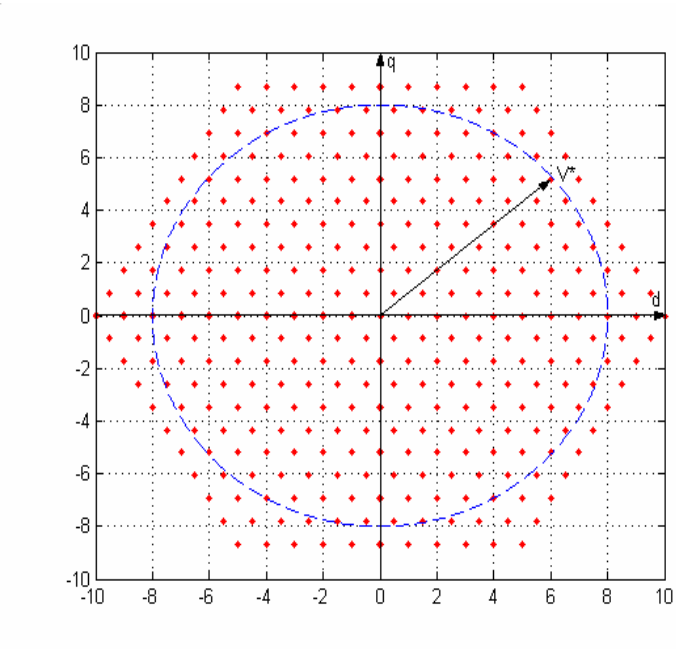


Figure 2.18: 21-level space vectors

2.3.5. Selective Harmonic Elimination

The popular selective harmonic elimination method is also called fundamental switching frequency method which is based on the harmonic elimination theory developed by Patel *et al* [28][29]. As shown in Figure. 2.7, a multilevel converter can produce a quarter-wave symmetric stepped voltage waveform synthesized by several DC voltages [2].

By applying Fourier series analysis, the output voltage can be expressed as

$$V(t) = \sum_{n=1,3,5...}^{\infty} \frac{4}{n\pi}(V_1 \cos(n\theta_1) + V_2 \cos(n\theta_2) + ... + V_s \cos(n\theta_s))\sin(n\omega t) \qquad (2.2)$$

where s is the number of DC sources, and V_1, V_2 ... V_s are the level of DC voltages. The switching angles must satisfy the condition $0 < \theta_1 < \theta_2 < \cdots < \theta_s < \frac{\pi}{2}$. However, if the switching angles do not satisfy the condition, this method no longer exists. If $V_1 = V_2 = ... = V_s$, this is called equal DC voltages case. To minimize harmonic distortion and to achieve adjustable amplitude of the fundamental component, up to s-1 harmonic contents can be removed from the voltage waveform. In general, the most significant low-frequency harmonics are chosen for elimination by properly selecting angles among different level converters, and high-frequency harmonic components can be readily removed by using additional filter circuits. To keep the number of eliminated harmonics at a constant level, all switching angles must satisfy the condition $0 < \theta_1 < \theta_2 < \cdots < \theta_s < \frac{\pi}{2}$, or the total harmonic distortion (THD) increases dramatically. Due to this reason, this modulation strategy basically provides a narrow range of modulation index, which is one of its disadvantages [13].

In order to achieve a wide range of modulation indexes with minimized THD for the synthesized waveforms, a generalized selective harmonic modulation method [30], [31] was proposed, which is called virtual stage PWM [14]. An output waveform is shown in Figure 2.19.

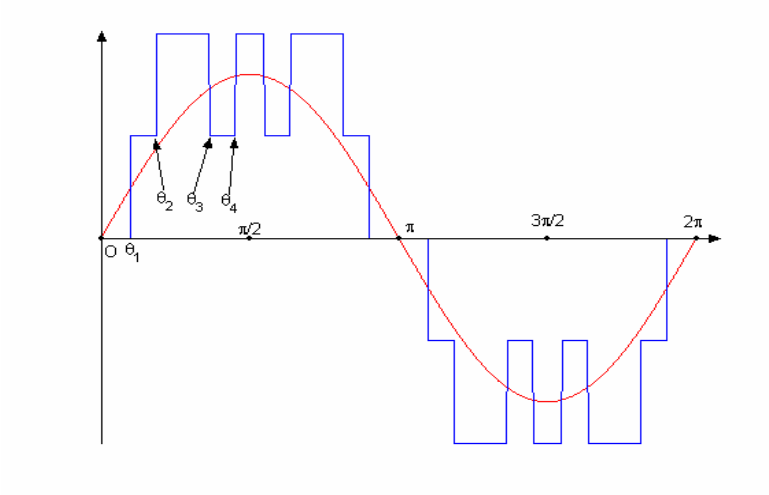


Figure 2.19: Output waveform of virtual stage PWM control

By applying Fourier series analysis, the output voltage can be expressed as

$$V(t) = \sum_{n=1,3,5\ldots}^{\infty} \frac{4}{n\pi}(V_1 \cos(n\theta_1) \pm V_2 \cos(n\theta_2) \pm V_3 \cos(n\theta_3) \pm \ldots \pm V_s \cos(n\theta_s))\sin(n\omega t) \tag{2.3}$$

where s is the number of switching angles, and V_1, V_2 ... V_s are the level of DC voltages. In this expression, the positive sign implies the rising edge, and the negative sign implies the falling edge. Similar to the fundamental switching frequency method, the switching angles must satisfy the condition $0 < \theta_1 < \theta_2 < \cdots < \theta_s < \frac{\pi}{2}$. However, if the switching angles do not satisfy the condition, this method no longer exists.

Therefore, the modulation control problem is converted into a mathematic problem to solve the following equations for a three-phase system. Here, m is modulation index.

$$\begin{aligned} &V_1 \cos(\theta_1) \pm V_2 \cos(\theta_2) \pm V_3 \cos(\theta_3) \pm \ldots \pm V_s \cos(\theta_s) = m \\ &V_1 \cos(5\theta_1) \pm V_2 \cos(5\theta_2) \pm V_3 \cos(5\theta_3) \pm \ldots \pm V_s \cos(5\theta_s) = 0 \\ &\qquad\qquad \vdots \\ &V_1 \cos(n\theta_1) \pm V_2 \cos(n\theta_2) \pm V_3 \cos(n\theta_3) \pm \ldots \pm V_s \cos(n\theta_s) = 0 \end{aligned} \tag{2.4}$$

The Virtual Stage PWM is a combination of Unipolar Programmed PWM and fundamental frequency switching scheme [14]. The output waveform of Unipolar Programmed PWM is shown in Figure 2.20. When Unipolar Programmed PWM is employed on a multilevel converter, typically one DC voltage is involved, where the switches connected to the DC voltage are switched "on" and "off" several times per fundamental cycle. The switching pattern decides what the output voltage waveform looks like.

When the multilevel fundamental switching method is used, all of the DC voltages are typically involved, where all of the switches are turned "on" and "off" only once per fundamental cycle. The multilevel fundamental switching method also refers to exactly one switching pattern.

For fundamental switching frequency method, the number of switching angles is equal to the number of DC sources. However, for the Virtual Stage PWM method, the number of switching angles is not equal to the number of DC voltages. For example, in Figure 2.19, only two DC voltages are used, whereas there are four switching angles.

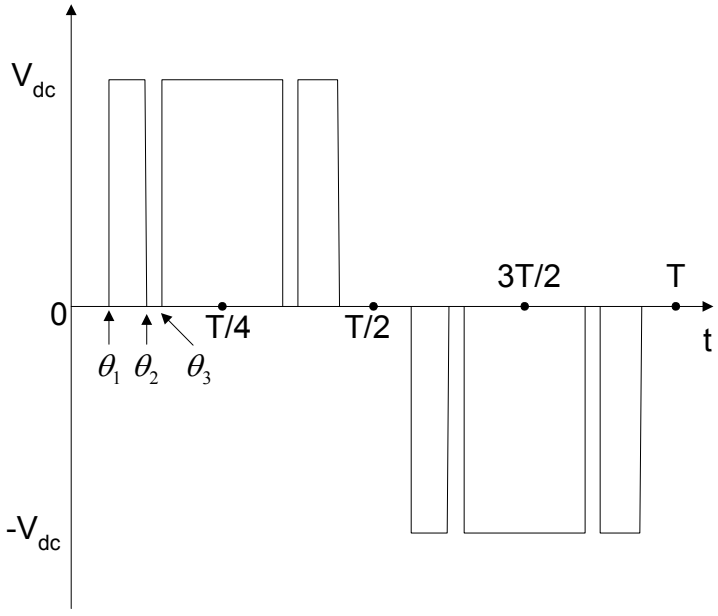


Figure 2.20: Unipolar switching output waveform

Bipolar Programmed PWM and Unipolar Programmed PWM could be used for modulation indices too low for the applicability of the multilevel fundamental frequency switching method. Virtual Stage PWM can also be used for low modulation indices. Virtual Stage PWM will produce output waveforms with a lower THD most of the time [14]. Therefore, Virtual Stage PWM provides another alternative to Bipolar Programmed PWM and Unipolar Programmed PWM for low modulation index control.

The major difficulty for selective harmonic elimination methods, including the fundamental switching frequency method and the Virtual Stage PWM method, is to solve the transcendental equations (2.4) for switching angles. Newton's method can be used to solve equations (2.4), but it needs good initial guesses, and solutions are not guaranteed. Therefore, Newton's method is not feasible to solving equations for large number of switching angles if good initial guesses are not available.

Recently, the resultant method [19], [20] has been proposed to solve the transcendental equations for switching angles. The transcendental equations characterizing the harmonic content can be converted into polynomial equations. Elimination theory (using resultants) has been employed to determine the switching angles to eliminate specific harmonics, such as the 5^{th}, 7^{th}, 11^{th}, and the 13^{th}. However, as the number of DC voltages or the number of switching angle increase, the degrees of the polynomials in these equations are large, and one reaches the limitations of the capability of contemporary computer algebra software tools (e.g., Mathematic or Maple) to solve the system of polynomial equations by using elimination theory [21].

2.4. Balance Control Problems in Multilevel Converters

The diode-clamped multilevel converter could not have balanced voltages for real power conversion without sacrificing output voltage performance. Thus, diode-clamped multilevel converters are suggested to be applied to reactive and harmonic compensation to avoid the voltage balancing problem [42]. The voltage unbalance problem could be solved by using a back-to-back rectifier/converter system and proper voltage balancing control [43]. Other references [44]-[46] suggested the use of additional voltage balancing circuits, such as DC choppers, etc.

The capacitor-clamped structure was originally proposed for high-voltage DC/DC conversions. It is easy to balance the voltages for such applications because the load current is DC. For the capacitor-clamped multilevel converter, voltage balancing is relatively complicated [5], [47]. It has been shown theoretically that the capacitor-clamped converter cannot have self-balanced voltage when applied to power conversion in which no real power is involved, such as reactive power compensation [13].

When the cascaded multilevel converter was introduced for motor drive applications, an isolated and separate DC source was needed for each H-bridge cell [7]. However, another paper presented the idea of using cascade multilevel converter for reactive and harmonic compensation, from which isolated DC sources can be omitted [42]. Additional work further demonstrated that the cascaded converter is suitable for universal power conditioning of power systems [22], [23]. The converter provides lower costs, higher performance, less EMI, and higher efficiency than the traditional PWM converter for power line conditioning applications, both series and parallel compensation. Although the cascaded converter has an inherent self-balancing characteristic, a slight voltage imbalance can occur because of the circuit component losses and limited controller resolution. A simple control method, which ensures DC voltage balance, has been proposed for reactive and harmonic compensation [13], [43].

2.5. The Next Steps

As discussed above, there are four popular modulation methods for multilevel converter control, space vector control method, selective harmonic elimination method, space vector PWM method and sinusoidal PWM method. Among these methods, space vector control method, space vector PWM method, and sinusoidal PWM method cannot completely eliminate the specified harmonics. Only selective harmonic elimination method can completely eliminate the specified harmonics. The space vector PWM method and sinusoidal PWM method will cause high switching loss and low efficiency due to the high switching frequency.

A disadvantage for the space vector PWM method and the space vector control method is that they cannot be applied to multilevel converters with unequal DC voltages.

The carrier phase shifting method for traditional PWM method also requires equal DC voltages. Until now, the number of harmonics the selective harmonics elimination method can eliminate is not more than the number of the unknowns in the equations, and the solutions are not available for the whole modulation index range. No such methods can be used to directly compute the output voltage pulses to eliminate the specified harmonics without any restriction of the number of the unknowns in the harmonic equation. Due to the difficulty of solving the transcendental equations, real-time control of multilevel converters with unequal DC voltage case is impossible now.

For these reasons, this dissertation focuses on the multilevel converter modulation control to completely eliminate any number of the specified harmonics, and this method can be applied to the whole modulation range under equal DC voltage case or unequal DC voltage case. The proposed method is called active harmonic elimination method because the harmonics are not filtered out by a passive output filter. This method also can be called computed PWM method because the output voltage pulses are directly computed.

Although the proposed method is based on harmonic elimination theory, the number of the harmonics can be eliminated is not restricted by the number of unknowns in the equations. One can control the number of harmonics to be eliminated based on the application requirements. Therefore, a small size filter is enough for applications because only very high frequency harmonics remain in the output voltage. The following chapters describe the development of the proposed method.

3. Fundamental Frequency Switching Control

In the previous chapter, the advantages and disadvantages of several modulation methods for multilevel converters have been summarized. In this chapter, the Fourier Series theory and Harmonics Elimination theory for the research will be discussed and applied to the harmonics elimination control for the multilevel converters.

In the first part of this chapter, the Fourier Series theory and harmonics elimination theory will be discussed briefly. Then the Fourier Series theory and Harmonics Elimination theory will be used to derive the transcendental equations for the fundamental frequency switching method for multilevel converters.

In the second part, resultant theory will be introduced and used to solve the transcendental equations for the fundamental frequency switching method for multilevel converters. The transcendental equations characterizing the harmonic content can be converted into polynomial equations. Elimination theory (using resultants) has been employed to determine the switching angles to eliminate specific harmonics, such as the 5^{th}, 7^{th}, 11^{th}, and the 13^{th}.

To conquer the computation difficulty for multilevel converters with high number of voltage levels, such as 15, 17, 19 voltage levels, Newton's method is used here to find the solutions for the switching angles. This is shown in the third part of the chapter.

3.1. Fourier Series and Harmonics Elimination Theory

After applying Fourier theory to the output voltage waveform of multilevel converters, which is odd quarter-wave symmetric, we can find the Fourier expression of the multilevel output voltage as (2.2). If the DC voltages are equal in the multilevel converter, the equation for the fundamental frequency switching control method can be expressed as:

$$V(t) = \sum_{n=1,3,5...}^{\infty} \frac{4V_{dc}}{n\pi}(\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3) + ... + \cos(n\theta_s))\sin(n\omega t) \quad (3.1)$$

From the equation, it can be seen that the output voltage has no even harmonics

because the output voltage waveform is odd quarter-wave symmetric. It also can be seen from (3.1) that the peak values of these odd harmonics are expressed in terms of the switching angles θ_1, θ_2, … and θ_s. Furthermore, the harmonic equations produced from (3.1) are transcendental equations.

Based on the harmonic elimination theory, if one wants to eliminate the n^{th} harmonic, then

$$\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3) + ... + \cos(n\theta_s) = 0 \tag{3.2}$$

That means to choose a series of switching angles to let the value of the n^{th} harmonic be zero. Therefore, an equation with *s* switching angles will be used to control the *s* different harmonic values. Generally, an equation with *s* switching angles is used to determine the fundamental frequency value, and to eliminate *s*-1 low order harmonics. For example, for an equation with three switching angles, (3.1) becomes

$$V(t) = \sum_{n=1,3,5...}^{\infty} \frac{4V_{dc}}{n\pi}(\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3))\sin(n\omega t) \tag{3.3}$$

Here, the fundamental peak value of the output voltage of V_1 should be controlled, and the 5th and 7th order harmonics should be eliminated. The resulting harmonic equations are:

$$\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) = \frac{\pi V_1}{4V_{dc}} \tag{3.4}$$

$$\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) = 0 \tag{3.5}$$

$$\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) = 0 \tag{3.6}$$

To simplify the expression, (3.4) can be written as

$$\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) = m \tag{3.7}$$

where

$$m = \frac{\pi V_1}{4V_{dc}} \tag{3.8}$$

is defined here as the modulation index. So

$$V_{1_{\max}} = \frac{4}{\pi} s V_{dc} \tag{3.9}$$

where s is the number of DC sources.

Here, the third harmonic has not been eliminated because the triplen harmonics can be automatically cancelled in the line-line voltages for balanced three-phase systems. Therefore, the triplen harmonics are not chosen for elimination in the phase voltage.

These harmonic equations (3.5)-(3.7) are transcendental equations. They are difficult to solve without using some sort of numerical iterative technique, such as Newton's method. However, by making some simple changes of variables and simplifying, these transcendental equations can be transformed into a set of polynomial equations. Then, resultant theory can be utilized to find all solutions to the harmonic equations.

3.2. Resultant Method for Transcendental Equations Solving

3.2.1. Resultant Theory

Suppose one has the following two polynomials in x_1 and x_2:

$$a(x_1, x_2) = a_3(x_1)x_2^3 + a_2(x_1)x_2^2 + a_1(x_1)x_2 + a_0(x_1) = 0 \tag{3.10}$$

and

$$b(x_1, x_2) = b_3(x_1)x_2^3 + b_2(x_1)x_2^2 + b_1(x_1)x_2 + b_0(x_1) = 0 \tag{3.11}$$

where $a_3(x_1)$, $a_2(x_1)$, $a_1(x_1)$, $a_0(x_1)$, $b_3(x_1)$, $b_2(x_1)$, $b_1(x_1)$, and $b_0(x_1)$ are polynomials in x_1. Also, define the following two polynomials in x_1 and x_2:

$$\alpha(x_1, x_2) = \alpha_2(x_1)x_2^2 + \alpha_1(x_1)x_2 + \alpha_0(x_1) \tag{3.12}$$

and

$$\beta(x_1, x_2) = \beta_2(x_1)x_2^2 + \beta_1(x_1)x_2 + \beta_0(x_1) \tag{3.13}$$

where $\alpha_2(x_1)$, $\alpha_1(x_1)$, $\alpha_0(x_1)$, $\beta_2(x_1)$, $\beta_1(x_1)$, and $\beta_0(x_1)$ are polynomials in x_1. Given a specific numerical value for x_1, it is can be seen from (3.10) thru (3.13) that $a(x_1, x_2)$ and $b(x_1, x_2)$ are not coprime if and only if there exist polynomials $\alpha(x_1, x_2)$ and $\beta(x_1, x_2)$ such that

$$\frac{a(x_1,x_2)}{b(x_1,x_2)}=\frac{\alpha(x_1,x_2)}{\beta(x_1,x_2)} \tag{3.14}$$

or,

$$b(x_1,x_2)\alpha(x_1,x_2)-a(x_1,x_2)\beta(x_1,x_2)=0 \tag{3.15}$$

If this equation is rewritten in the matrix form

$$S(x_1)V(x_1)=\vec{0} \tag{3.16}$$

where the coefficients of x_2^k, $k = 0, 1, ..., 5$, are equated to zero because this equation is satisfied for any x_2. The resulting matrix equation is [14] [20]:

$$\begin{bmatrix} b_0(x_1) & a_0(x_1) & 0 & 0 & 0 & 0 \\ b_1(x_1) & a_1(x_1) & b_0(x_1) & a_0(x_1) & 0 & 0 \\ b_2(x_1) & a_2(x_1) & b_1(x_1) & a_1(x_1) & b_0(x_1) & a_0(x_1) \\ b_3(x_1) & a_3(x_1) & b_2(x_1) & a_2(x_1) & b_1(x_1) & a_1(x_1) \\ 0 & 0 & b_3(x_1) & a_3(x_1) & b_2(x_1) & a_2(x_1) \\ 0 & 0 & 0 & 0 & b_3(x_1) & a_3(x_1) \end{bmatrix} \begin{bmatrix} -\alpha_0(x_1) \\ \beta_0(x_1) \\ -\alpha_1(x_1) \\ \beta_1(x_1) \\ -\alpha_2(x_1) \\ \beta_2(x_1) \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{3.17}$$

The 6×6 square matrix $S(x_1)$ in (3.17) is called the Sylvester Resultant Matrix. In general, the Sylvester Resultant Matrix will be $(d_1+d_2)\times(d_1+d_2)$, where d_1 and d_2 are the degrees of the two polynomials $a(x_1,x_2)$ and $b(x_1,x_2)$ in x_2, respectively.

Equation (3.16) is a homogeneous linear algebraic equation. Given a particular value for x_1, only the trivial solution $V(x_1)=\overline{0}$ solves (3.17) if $S(x_1)$ is nonsingular. In other words, $a(x_1,x_2)$ and $b(x_1,x_2)$ are coprime. However, if a particular value for x_1 results in a singular $S(x_1)$, then there are nonzero solutions to (3.17). In this situation, $a(x_1,x_2)$ and $b(x_1,x_2)$ are not coprime. Therefore, the determinant of $S(x_1)$ is zero:

$$R(x_1)=\det\left(\begin{bmatrix} b_0(x_1) & a_0(x_1) & 0 & 0 & 0 & 0 \\ b_1(x_1) & a_1(x_1) & b_0(x_1) & a_0(x_1) & 0 & 0 \\ b_2(x_1) & a_2(x_1) & b_1(x_1) & a_1(x_1) & b_0(x_1) & a_0(x_1) \\ b_3(x_1) & a_3(x_1) & b_2(x_1) & a_2(x_1) & b_1(x_1) & a_1(x_1) \\ 0 & 0 & b_3(x_1) & a_3(x_1) & b_2(x_1) & a_2(x_1) \\ 0 & 0 & 0 & 0 & b_3(x_1) & a_3(x_1) \end{bmatrix}\right)=0 \tag{3.18}$$

Here, $R(x_1)$, which is only a function of x_1, is called the Resultant Polynomial.

Now, the roots to (3.18) can be found since it is a polynomial of x_1; then substitute these roots into the equation

$$a(x_1, x_2) = 0 \tag{3.19}$$

to get the roots to (3.19). The common roots are the roots of equations (3.10) and (3.11).

In conclusion, the procedure to get the roots for two polynomials $a(x_1, x_2) = 0$ and $b(x_1, x_2) = 0$ has four steps [14], [20]:

1. Compute the roots x_{1k}, $k = 0, 1, ..., n_R$, of $R(x_1) = 0$, where n_R is the degree of $R(x_1)$.
2. Substitute these roots into $a(x_1, x_2) = 0$.
3. For $k = 0, 1, ..., n_R$, solve the equation $a(x_{1k}, x_2) = 0$ to get the roots x_{2kl}, $l = 0, 1, ..., n_a$, where n_a is the degree of $a(x_1, x_2)$ in x_2.
4. The common zeros of $a(x_1, x_2) = 0$ and $b(x_1, x_2) = 0$ are then the values (x_{1k}, x_{2kl}) that satisfy the equation $b(x_{1k}, x_{2kl}) = 0$.

From the above method, it can be seen that this method can find all the solutions for the equations $a(x_1, x_2) = 0$ and $b(x_1, x_2) = 0$.

3.2.2. Solutions to the Harmonic Equations by Resultant Theory

To solve the harmonic equations by resultant theory, they must be changed into polynomials. First, change the variables,

$$x_1 = \cos(\theta_1) \tag{3.20}$$

$$x_2 = \cos(\theta_2) \tag{3.21}$$

and

$$x_s = \cos(\theta_s) \tag{3.22}$$

Also, use the following trigonometric identities:

$$\cos(5\theta) = 5\cos(\theta) - 20\cos^3(\theta) + 16\cos^5(\theta) \tag{3.23}$$

$$\cos(7\theta) = -7\cos(\theta) + 56\cos^3(\theta) - 112\cos^5(\theta) + 64\cos^7(\theta) \tag{3.24}$$

$$\begin{aligned}\cos(11\theta) = &-11\cos(\theta) + 220\cos^3(\theta) - 1232\cos^5(\theta) \\ &+ 2816\cos^7(\theta) - 2816\cos^9(\theta) + 1024\cos^{11}(\theta)\end{aligned} \tag{3.25}$$

$$\begin{aligned}\cos(13\theta) = &13\cos(\theta) - 364\cos^3(\theta) + 2912\cos^5(\theta) \\ &- 9984\cos^7(\theta) + 16640\cos^9(\theta) - 13312\cos^{11}(\theta) + 4096\cos^{13}(\theta)\end{aligned} \tag{3.26}$$

and

$$\begin{aligned}\cos(17\theta) = &17\cos(\theta) - 816\cos^3(\theta) + 11424\cos^5(\theta) - 71808\cos^7(\theta) \\ &+ 239360\cos^9(\theta) - 452608\cos^{11}(\theta) + 487424\cos^{13}(\theta) \\ &- 278528\cos^{15}(\theta) + 65536\cos^{17}(\theta)\end{aligned} \tag{3.27}$$

Then, apply them to the transcendental harmonic equations above, and the following polynomial harmonic equations can be found.

For the fundamental frequency harmonic:

$$p_1(x_1, x_2, \cdots, x_s) = \sum_{n=1}^{s} x_n - m = 0 \tag{3.28}$$

For the 5th harmonic:

$$p_5(x_1, x_2, \cdots, x_s) = \sum_{n=1}^{s} \left(5x_n - 20x_n^3 + 16x_n^5\right) = 0 \tag{3.29}$$

For the 7th harmonic:

$$p_7(x_1, x_2, ..., x_s) = \sum_{n=1}^{s} \left(-7x_n + 56x_n^3 - 112x_n^5 + 64x_n^7\right) = 0 \tag{3.30}$$

For the 11th harmonic:

$$\begin{aligned}&p_{11}(x_1, x_2, ..., x_s) = \\ &\sum_{n=1}^{s} \left(-11x_n + 220x_n^3 - 1232x_n^5 + 2816x_n^7 - 2816x_n^9 + 1024x_n^{11}\right) = 0\end{aligned} \tag{3.31}$$

For the 13th harmonic:

$$\begin{aligned}&p_{13}(x_1, x_2, ..., x_s) = \\ &\sum_{n=1}^{s} \left(13x_n - 364x_n^3 + 2912x_n^5 - 9984x_n^7 + 16640x_n^9 - 13312x_n^{11} + 4096x_n^{13}\right) = 0\end{aligned} \tag{3.32}$$

and the 17th harmonic:

$$p_{17}(x_1, x_2, ..., x_s) = \sum_{n=1}^{s} \begin{pmatrix} 17x_n - 816x_n^3 + 11424x_n^5 - 71808x_n^7 + 239360x_n^9 - 452608x_n^{11} \\ + 487424x_n^{13} - 278528x_n^{15} + 65536x_n^{17} \end{pmatrix} = 0 \quad (3.33)$$

For these equations, the following situation must be satisfied,

$$0 \le \theta_1 \le \theta_2 \le \cdots \le \theta_s \le \frac{\pi}{2} \quad (3.34)$$

So the variables $x_1, x_2, \ldots, x_s$ must satisfy

$$0 \le x_s \le \cdots \le x_2 \le x_1 \le 1 \quad (3.35)$$

Now, the transcendental harmonic equations have been changed into polynomial equations in the variables $x_1, x_2, \cdots, x_s$. Resultant theory can be used to solve these polynomial equations to find the switching angles.

3.2.3. Solution Results

By applying the resultant method, the solution of fundamental frequency switching angles for 5-, 7-, 11- and 13-level can be obtained. In this thesis, the THD is computed throughout the 50th as $THD = \sqrt{\frac{V_5^2 + V_7^2 + \cdots + V_{47}^2 + V_{49}^2}{V_1^2}}$ for all the cases except indicated. The even and triplen harmonics are not computed in THD because they do not appear in the line-line voltages.

1. For 5-level multilevel converters, the harmonic equations are:

$$\begin{aligned} \cos(\theta_1) + \cos(\theta_2) &= m \\ \cos(5\theta_1) + \cos(5\theta_2) &= 0 \end{aligned} \quad (3.36)$$

The polynomial equations are:

$$\begin{aligned} p_1(x_1, x_2) &= \sum_{n=1}^{2} x_n - m = 0 \\ p_5(x_1, x_2) &= \sum_{n=1}^{2} \left(5x_n - 20x_n^3 + 16x_n^5\right) = 0 \end{aligned} \quad (3.37)$$

The solutions are shown in Figure 3.1 (a). The x-axis represents the modulation index. The y axis represents the switching angles in degrees. The THD for five-level fundamental frequency switching control is shown in Figure 3.1 (b). Because there are several sets of solutions, Figure 3.1 (c) shows the lowest THD for the fundamental frequency switching control.

From Figure 3.1, some features for the solutions can be derived:

(1). The modulation index *m* only has solutions in a range of modulation indices. For the 5-level case, *m* is from 0.9 to 1.9.

(2). For some modulation indices, there are more than one solution set.

(3). The THD is different for different solution sets; therefore, the low THD solution set should be chosen for practical application.

(4). Solution is not continuous for some modulation indices *m*.

2. For the 7-level multilevel converters, the harmonic equations are:

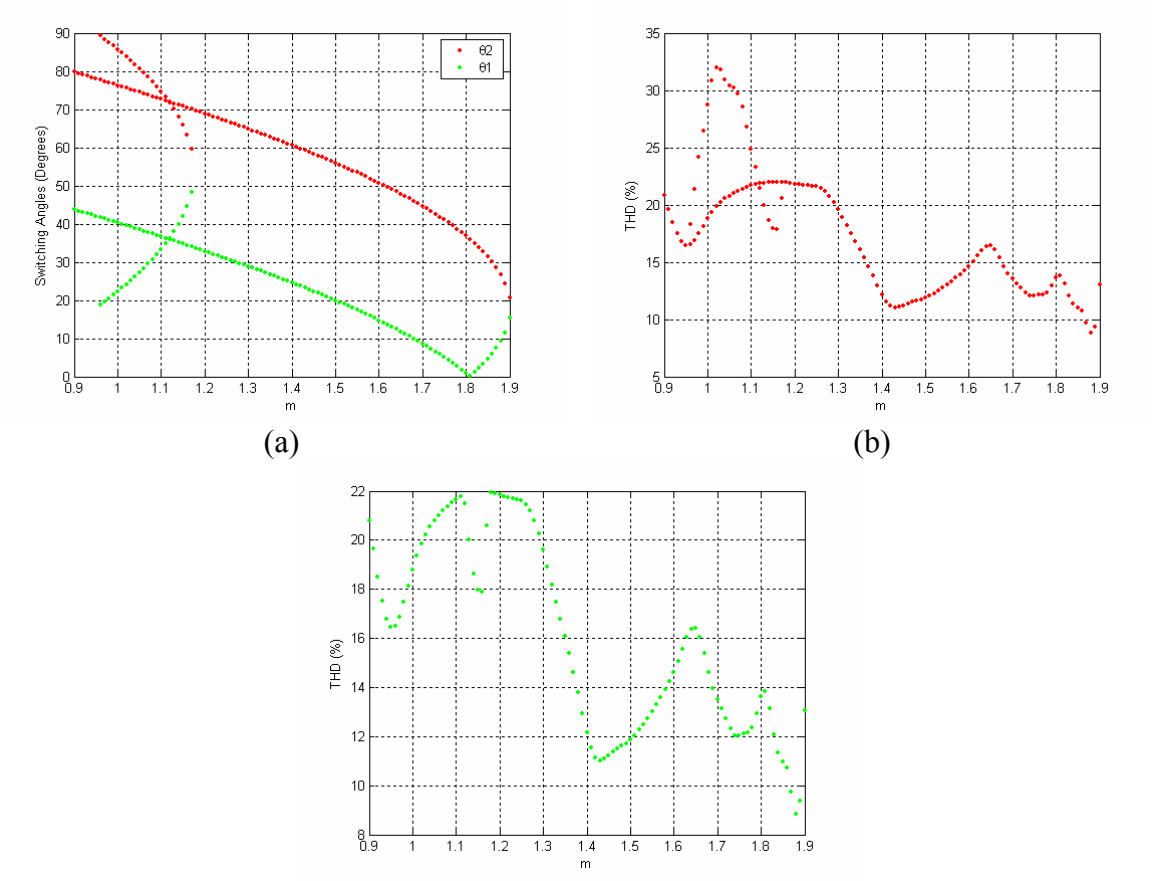
$$\begin{aligned} &\cos(\theta_1)+\cos(\theta_2)+\cos(\theta_3)=m \\ &\cos(5\theta_1)+\cos(5\theta_2)+\cos(5\theta_3)=0 \\ &\cos(7\theta_1)+\cos(7\theta_2)+\cos(7\theta_3)=0 \end{aligned} \tag{3.38}$$

The polynomial equations are:

$$\begin{aligned} &p_1(x_1,x_2,x_3)=\sum_{n=1}^{3}x_n-m=0 \\ &p_5(x_1,x_2,x_3)=\sum_{n=1}^{3}\left(5x_n-20x_n^3+16x_n^5\right)=0 \\ &p_7(x_1,x_2,x_3)=\sum_{n=1}^{3}\left(-7x_n+56x_n^3-112x_n^5+64x_n^7\right)=0 \end{aligned} \tag{3.39}$$

The solutions and THD are shown in Figure 3.2.

The features that can be derived from the solutions are similar to the 5-level case. Later, it can be seen that these features are common regardless of the number of the levels for the multilevel converters.



(a) (b)

(c)

Figure 3.1: Solutions for 5-level multilevel converter (a) switching angles; (b) THD for all solutions; (c) lowest THD

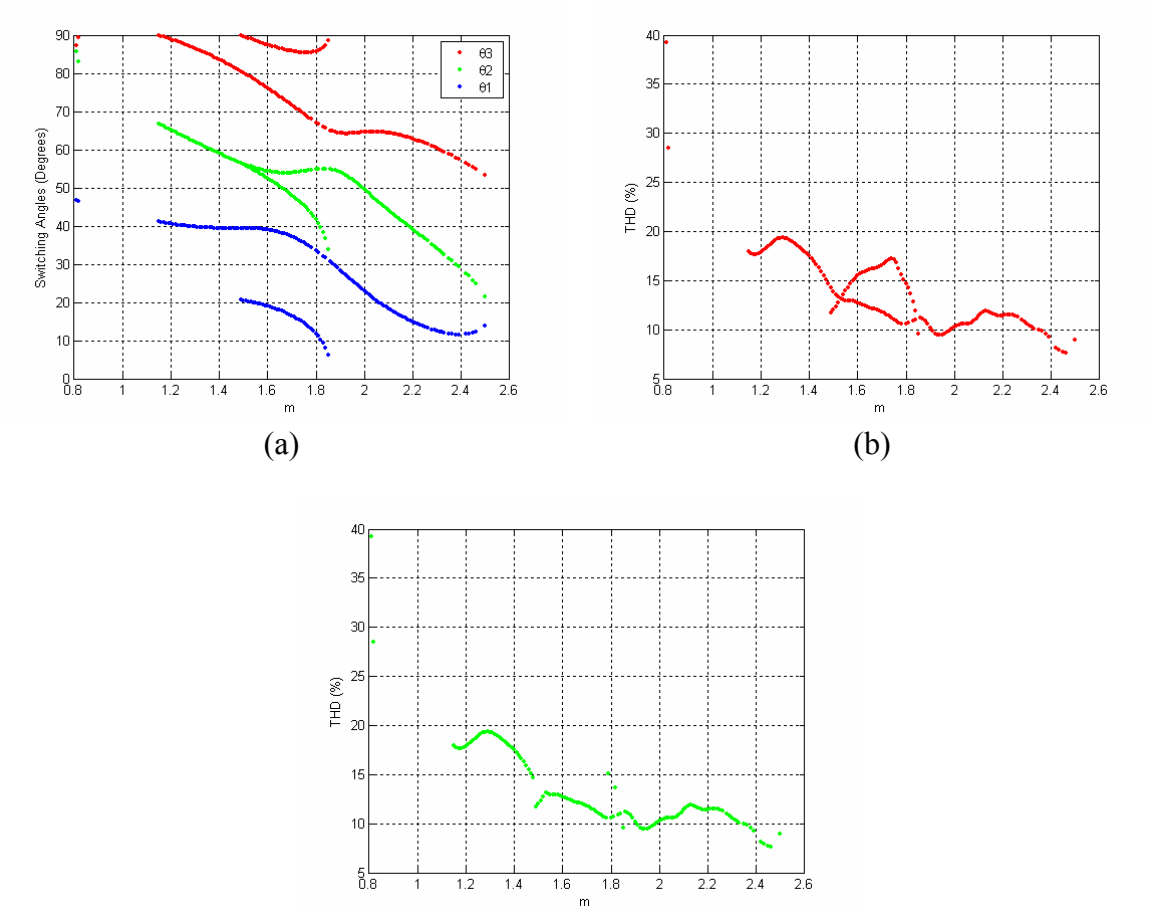


Figure 3.2: Solutions for 7-level multilevel converter (a) switching angles; (b) THD for all solutions; (c) lowest THD

3. For the 9-level multilevel converters, the harmonic equations are:

$$\begin{aligned}
&\cos(\theta_1)+\cos(\theta_2)+\cos(\theta_3)+\cos(\theta_4)=m\\
&\cos(5\theta_1)+\cos(5\theta_2)+\cos(5\theta_3)+\cos(5\theta_4)=0\\
&\cos(7\theta_1)+\cos(7\theta_2)+\cos(7\theta_3)+\cos(7\theta_4)=0\\
&\cos(11\theta_1)+\cos(11\theta_2)+\cos(11\theta_3)+\cos(11\theta_4)=0
\end{aligned} \tag{3.40}$$

The polynomial equations are:

$$\begin{aligned}
&p_1(x_1,x_2,x_3,x_4)=\sum_{n=1}^{4}x_n-m=0\\
&p_5(x_1,x_2,x_3,x_4)=\sum_{n=1}^{4}\left(5x_n-20x_n^3+16x_n^5\right)=0\\
&p_7(x_1,x_2,x_3,x_4)=\sum_{n=1}^{4}\left(-7x_n+56x_n^3-112x_n^5+64x_n^7\right)=0\\
&p_{11}(x_1,x_2,x_3,x_4)=\\
&\sum_{n=1}^{4}\left(-11x_n+220x_n^3-1232x_n^5+2816x_n^7-2816x_n^9+1024x_n^{11}\right)=0
\end{aligned} \tag{3.41}$$

The solutions and THD are shown in Figure 3.3.

4. For the 11-level multilevel converters, the harmonic equations are:

$$\begin{aligned}
&\cos(\theta_1)+\cos(\theta_2)+\cos(\theta_3)+\cos(\theta_4)+\cos(\theta_5)=m\\
&\cos(5\theta_1)+\cos(5\theta_2)+\cos(5\theta_3)+\cos(5\theta_4)+\cos(5\theta_5)=0\\
&\cos(7\theta_1)+\cos(7\theta_2)+\cos(7\theta_3)+\cos(7\theta_4)+\cos(7\theta_5)=0\\
&\cos(11\theta_1)+\cos(11\theta_2)+\cos(11\theta_3)+\cos(11\theta_4)+\cos(11\theta_5)=0\\
&\cos(13\theta_1)+\cos(13\theta_2)+\cos(13\theta_3)+\cos(13\theta_4)+\cos(13\theta_5)=0
\end{aligned} \tag{3.42}$$

The polynomial equations are:

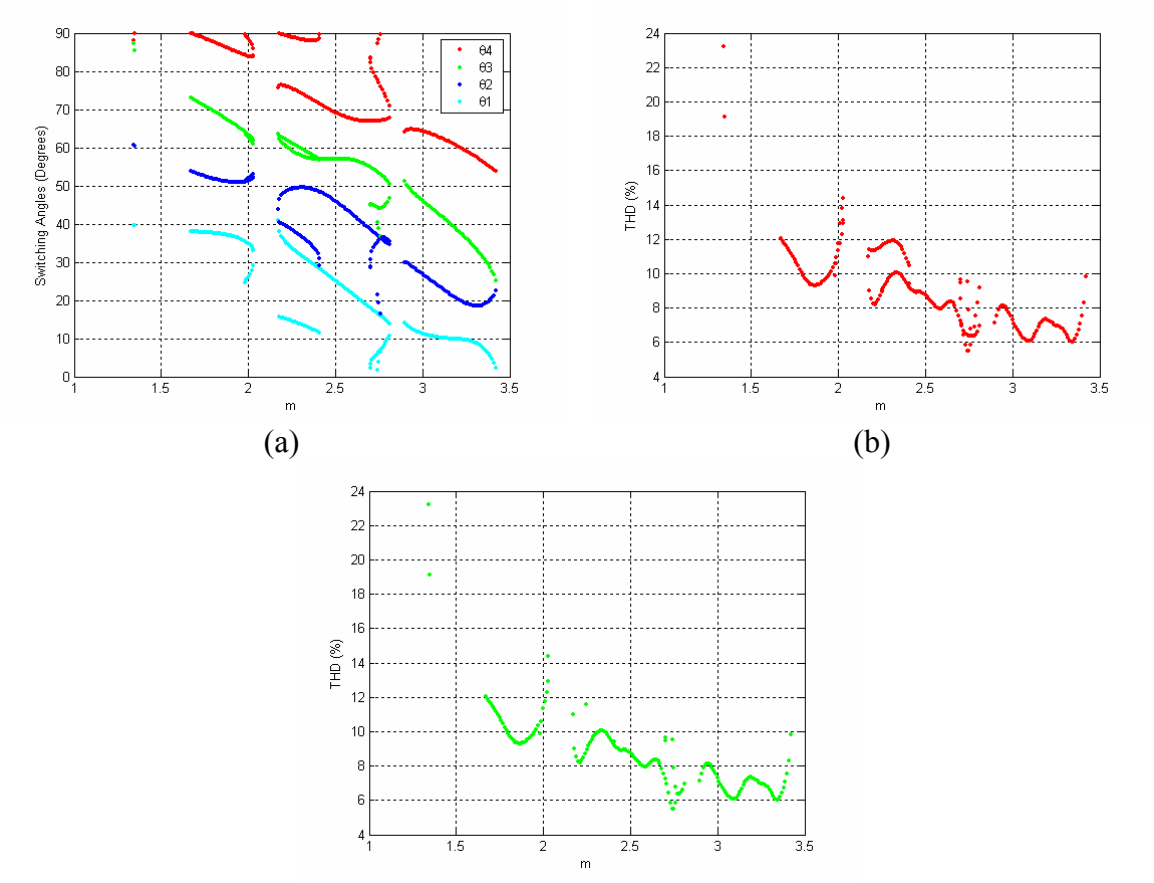


Figure 3.3: Solutions for 9-level multilevel converter (a) switching angles; (b) THD for all solutions; (c) lowest THD

$$p_1(x_1, x_2, x_3, x_4, x_5) = \sum_{n=1}^{5} x_n - m = 0$$

$$p_5(x_1, x_2, x_3, x_4, x_5) = \sum_{n=1}^{5} \left(5x_n - 20x_n^3 + 16x_n^5\right) = 0$$

$$p_7(x_1, x_2, x_3, x_4, x_5) = \sum_{n=1}^{5} \left(-7x_n + 56x_n^3 - 112x_n^5 + 64x_n^7\right) = 0$$

$$p_{11}(x_1, x_2, x_3, x_4, x_5) =$$

$$\sum_{n=1}^{5} \left(-11x_n + 220x_n^3 - 1232x_n^5 + 2816x_n^7 - 2816x_n^9 + 1024x_n^{11}\right) = 0$$

$$p_{13}(x_1, x_2, x_3, x_4, x_5) =$$

$$\sum_{n=1}^{5} \left(13x_n - 364x_n^3 + 2912x_n^5 - 9984x_n^7 + 16640x_n^9 - 13312x_n^{11} + 4096x_n^{13}\right) = 0$$

(3.43)

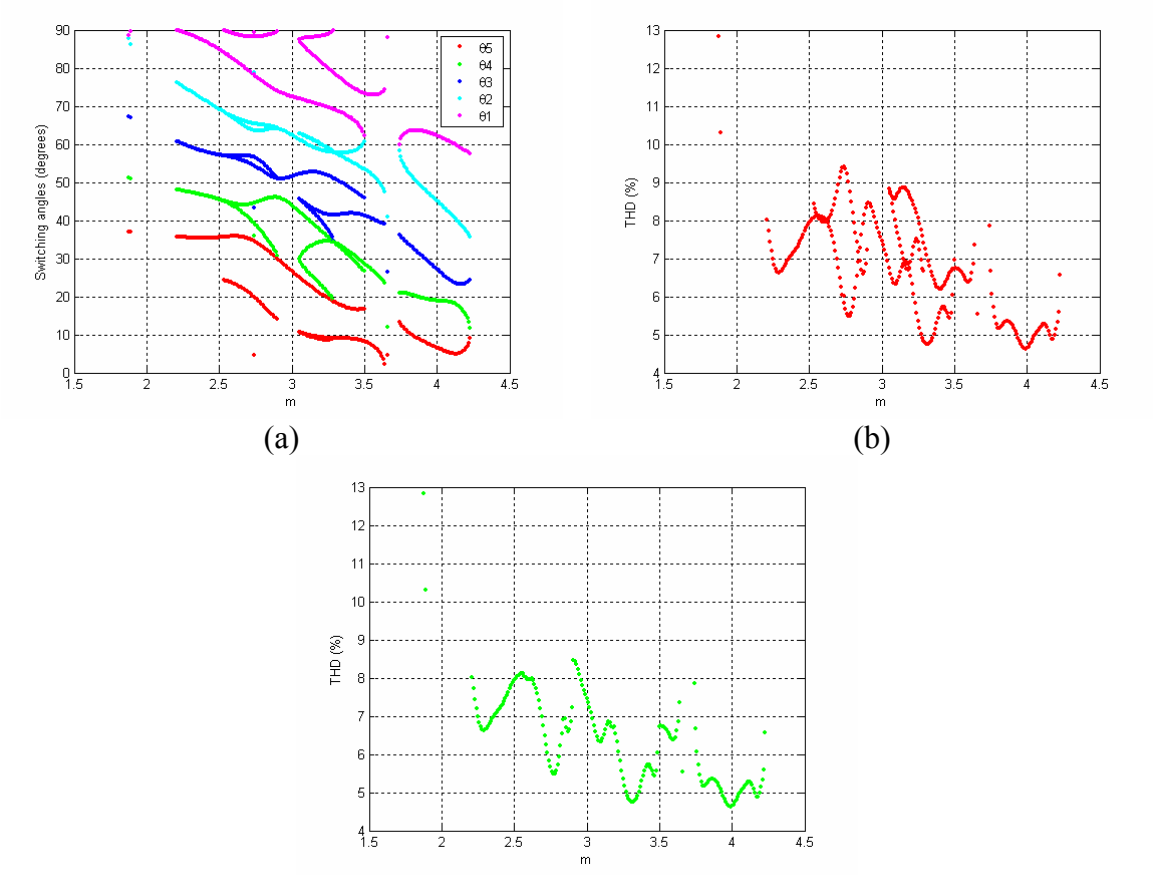
The solutions and THD are shown in Figure 3.4.

5. For the 13-level multilevel converters, the harmonic equations are:

$$\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4) + \cos(\theta_5) + \cos(\theta_6) = m$$
$$\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4) + \cos(5\theta_5) + \cos(5\theta_6) = 0$$
$$\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4) + \cos(7\theta_5) + \cos(7\theta_6) = 0$$
$$\cos(11\theta_1) + \cos(11\theta_2) + \cos(11\theta_3) + \cos(11\theta_4) + \cos(11\theta_5) + \cos(11\theta_6) = 0$$
$$\cos(13\theta_1) + \cos(13\theta_2) + \cos(13\theta_3) + \cos(13\theta_4) + \cos(13\theta_5) + \cos(13\theta_6) = 0$$
$$\cos(17\theta_1) + \cos(17\theta_2) + \cos(17\theta_3) + \cos(17\theta_4) + \cos(17\theta_5) + \cos(17\theta_6) = 0$$

(3.44)

The polynomial equations are:



(a) (b)

(c)

Figure 3.4: Solutions for 11-level multilevel converter (a) switching angles; (b) THD for all solutions; (c) lowest THD

$$p_1(x_1,x_2,x_3,x_4,x_5,x_6)=\sum_{n=1}^{6}x_n-m=0$$

$$p_5(x_1,x_2,x_3,x_4,x_5,x_6)=\sum_{n=1}^{6}\left(5x_n-20x_n^3+16x_n^5\right)=0$$

$$p_7(x_1,x_2,x_3,x_4,x_5,x_6)=\sum_{n=1}^{6}\left(-7x_n+56x_n^3-112x_n^5+64x_n^7\right)=0$$

$$p_{11}(x_1,x_2,x_3,x_4,x_5,x_6)=$$
$$\sum_{n=1}^{6}\left(-11x_n+220x_n^3-1232x_n^5+2816x_n^7-2816x_n^9+1024x_n^{11}\right)=0$$

$$p_{13}(x_1,x_2,x_3,x_4,x_5,x_6)=$$
$$\sum_{n=1}^{6}\left(13x_n-364x_n^3+2912x_n^5-9984x_n^7+16640x_n^9-13312x_n^{11}+4096x_n^{13}\right)=0$$

$$p_{17}(x_1,x_2,x_3,x_4,x_5,x_6)=$$
$$\sum_{n=1}^{6}\begin{pmatrix}17x_n-816x_n^3+11424x_n^5-71808x_n^7+239360x_n^9-452608x_n^{11}\\+487424x_n^{13}-278528x_n^{15}+65536x_n^{17}\end{pmatrix}=0$$

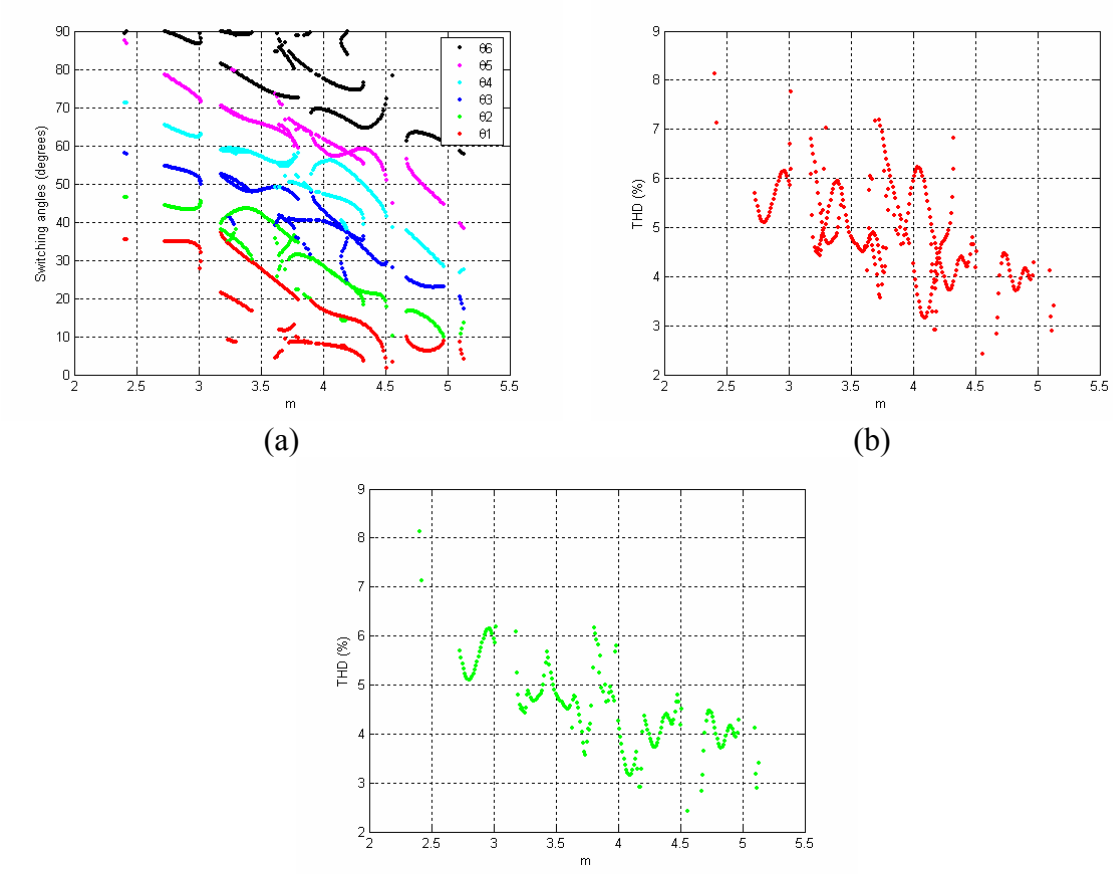
(3.45)

The solutions are shown in Figure 3.5.

6. Unipolar switching scheme

From the computation results, it can be seen that no solutions correspond to the modulation index less than 0.9. It is necessary to use three-level converters to extend the modulation index to below 0.9. But for three-level converters, the fundamental frequency switching method just can find a switching angle that produces a desired fundamental amplitude, and no additional harmonics can be eliminated. To conquer this problem, a unipolar switching method is used for the control of three-level converters. The output voltage waveform is shown in Figure 3.6.

The harmonic equations are:



(a) (b)

(c)

Figure 3.5: Solutions for 13-level multilevel converter (a) switching angles; (b) THD for all solutions; (c) lowest THD

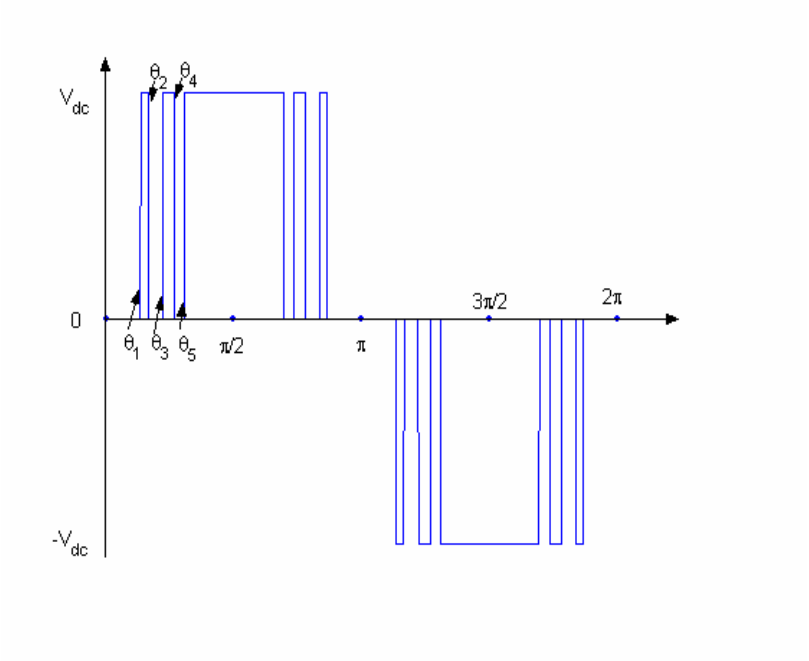


Figure 3.6: 5-angle unipolar converter output voltage

$$\begin{aligned}
&\cos(\theta_1)-\cos(\theta_2)+\cos(\theta_3)-\cos(\theta_4)+\cos(\theta_5)=m\\
&\cos(5\theta_1)-\cos(5\theta_2)+\cos(5\theta_3)-\cos(5\theta_4)+\cos(5\theta_5)=0\\
&\cos(7\theta_1)-\cos(7\theta_2)+\cos(7\theta_3)-\cos(7\theta_4)+\cos(7\theta_5)=0\\
&\cos(11\theta_1)-\cos(11\theta_2)+\cos(11\theta_3)-\cos(11\theta_4)+\cos(11\theta_5)=0\\
&\cos(13\theta_1)-\cos(13\theta_2)+\cos(13\theta_3)-\cos(13\theta_4)+\cos(13\theta_5)=0
\end{aligned} \tag{3.46}$$

The polynomial equations are:

$$p_1(x_1, x_2, x_3, x_4, x_5) = \sum_{n=1}^{5} (-1)^{n-1} x_n - m = 0$$

$$p_5(x_1, x_2, x_3, x_4, x_5) = \sum_{n=1}^{5} (-1)^{n-1} \left(5x_n - 20x_n^3 + 16x_n^5\right) = 0$$

$$p_7(x_1, x_2, x_3, x_4, x_5) = \sum_{n=1}^{5} (-1)^{n-1} \left(-7x_n + 56x_n^3 - 112x_n^5 + 64x_n^7\right) = 0$$

$$p_{11}(x_1, x_2, x_3, x_4, x_5) =$$

$$\sum_{n=1}^{5} (-1)^{n-1} \left(-11x_n + 220x_n^3 - 1232x_n^5 + 2816x_n^7 - 2816x_n^9 + 1024x_n^{11}\right) = 0$$

$$p_{13}(x_1, x_2, x_3, x_4, x_5) =$$

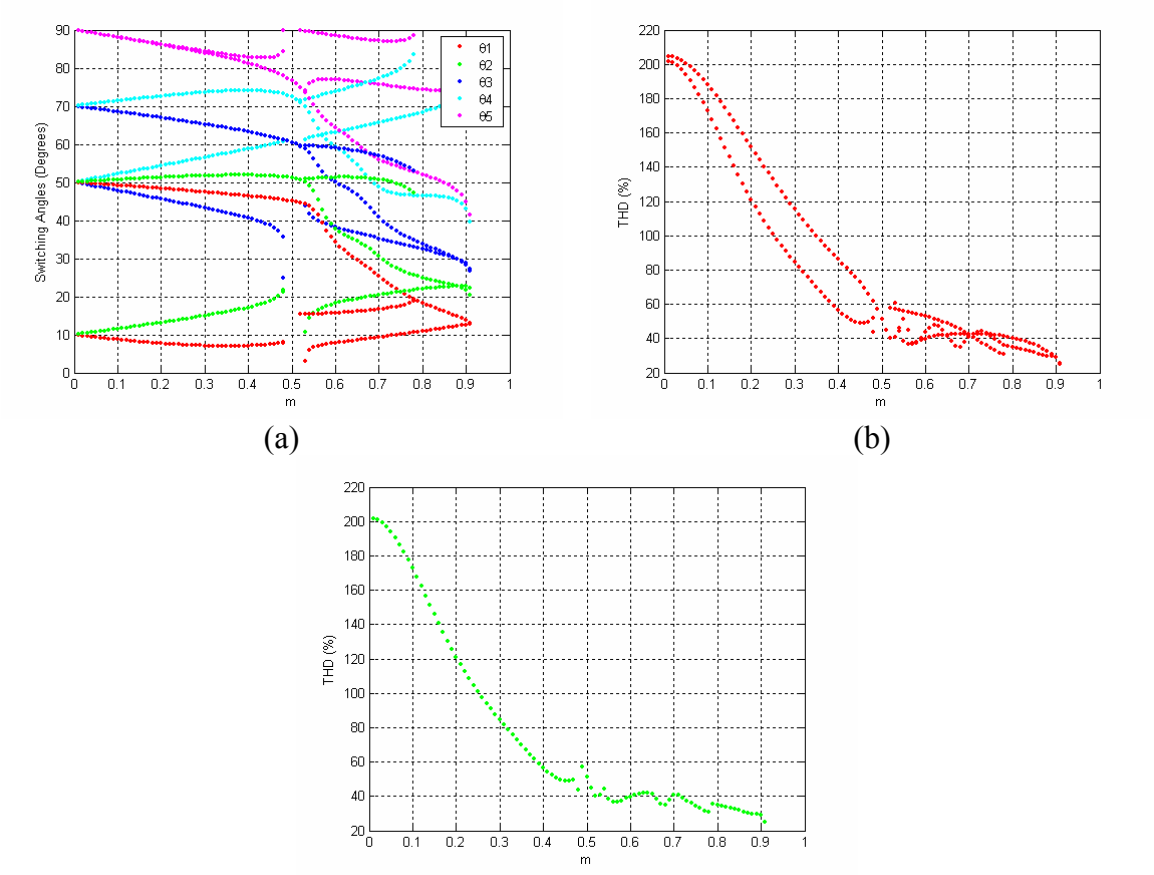
$$\sum_{n=1}^{5} (-1)^{n-1} \left(13x_n - 364x_n^3 + 2912x_n^5 - 9984x_n^7 + 16640x_n^9 - 13312x_n^{11} + 4096x_n^{13}\right) = 0 \quad (3.47)$$

The solutions and THD are shown in Figure 3.7.

3.3. Transcendental Equations Solving for Higher Order Harmonics Elimination

Until now, the transcendental equations characterizing the harmonic content have been converted into polynomial equations, and elimination theory (using resultants) has been employed to determine the switching angles to eliminate specified harmonics, such as 5^{th}, 7^{th}, 11^{th}, and the 13^{th} for up to 13-level multilevel converters. However, as the number of levels increase, the degrees of the polynomials in these equations are large and one reaches the limitations of the capability of contemporary computer algebra software tools (e.g., Mathematic or Maple) to solve the system of polynomial equations by using elimination theory.

To conquer this problem, the fundamental frequency switching angle computation is solved by Newton's method. The initial guess can be provided by the results of lower order transcendental equations by the resultant method. For example, *s* equations need *s* initial switching angles. The *s*-1 initial switching angles can be from the previous results of the *s*-1 equations. Only one initial guess is needed to be set. This method is referred to as the Newton climbing method since an *s* order equation needs solutions of an *s*-1 order equation as initial guesses.



(a) (b)

(c)

Figure 3.7: Solutions for unipolar converter (a) switching angles; (b) THD for all solutions; (c) lowest THD

The Newton iterative method for the fundamental frequency switching computation is:

$$x_{n+1} = x_n - J^{-1} f \tag{3.48}$$

where x_{n+1} is the new value, and x_n is the old value. J is the Jacobian matrix for the transcendental equations, and f is the transcendental equation function.

$$f = \begin{bmatrix} \sum_{n=1}^{s} \cos(h_1 \theta_n) \\ \sum_{n=1}^{s} \cos(h_2 \theta_n) \\ \vdots \\ \sum_{n=1}^{s} \cos(h_{s-1} \theta_n) \\ \sum_{n=1}^{s} \cos(h_s \theta_n) \end{bmatrix} \tag{3.49}$$

where $h = [1 \quad 5 \quad 7 \quad 11 \quad 13 \quad 17 \quad 19 \quad \cdots]$ is odd, non-triplen harmonic number.

The Jacobian matrix is:

$$J = \begin{bmatrix} -h_1 \sin(\theta_1) & -h_1 \sin(\theta_2) & \cdots & -h_1 \sin(\theta_{s-1}) & -h_1 \sin(\theta_s) \\ -h_2 \sin(h_2 \theta_1) & -h_2 \sin(h_2 \theta_2) & \cdots & \vdots & \vdots \\ \vdots & \vdots & & \vdots & \vdots \\ -h_{s-1} \sin(h_{s-1} \theta_1) & & & -h_{s-1} \sin(h_{s-1} \theta_{s-1}) & -h_{s-1} \sin(h_{s-1} \theta_s) \\ -h_s \sin(h_s \theta_1) & \cdots & \cdots & -h_s \sin(h_s \theta_{s-1}) & -h_s \sin(h_s \theta_s) \end{bmatrix} \tag{3.50}$$

The solutions of switching angles and THD to the 15-level case are shown in Figure 3.8.

The solutions of switching angles and THD to the 17-level case are shown in Figure 3.9.

The solutions of switching angles and THD to the 19-level case are shown in Figure 3.10.

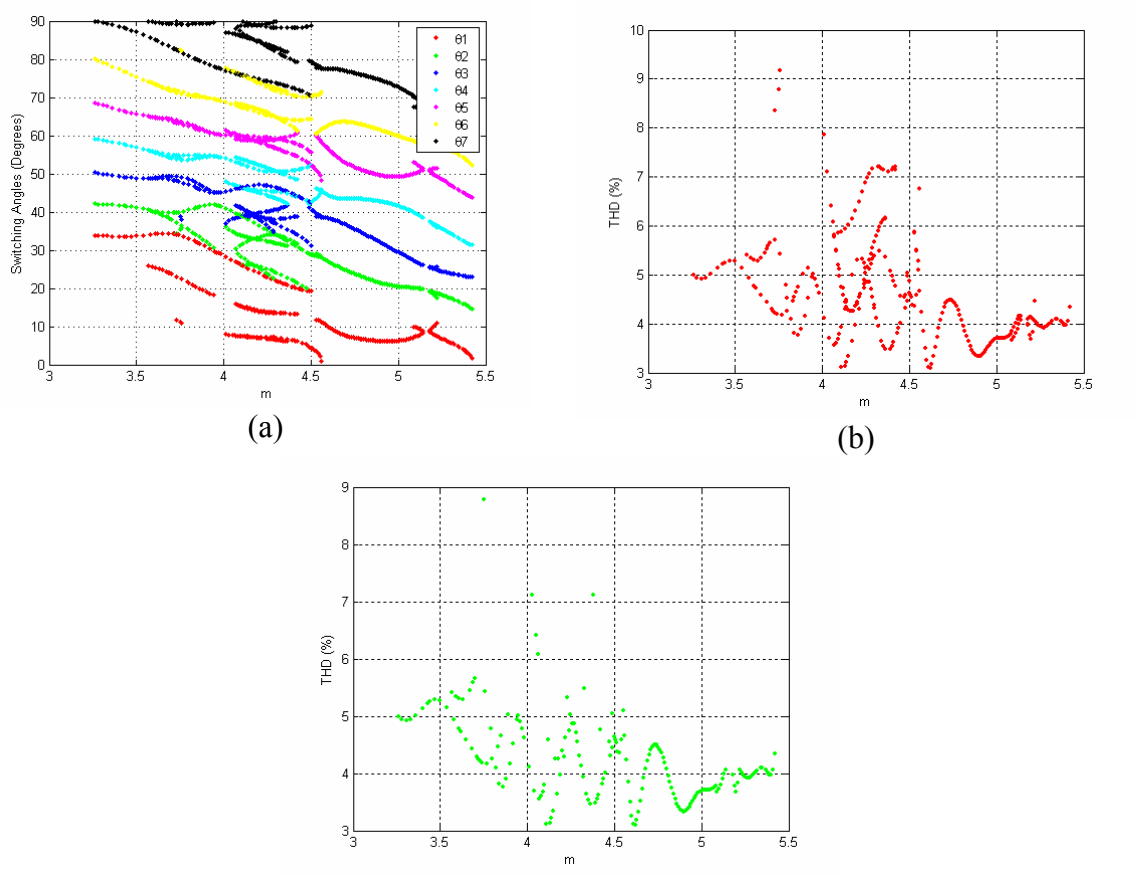
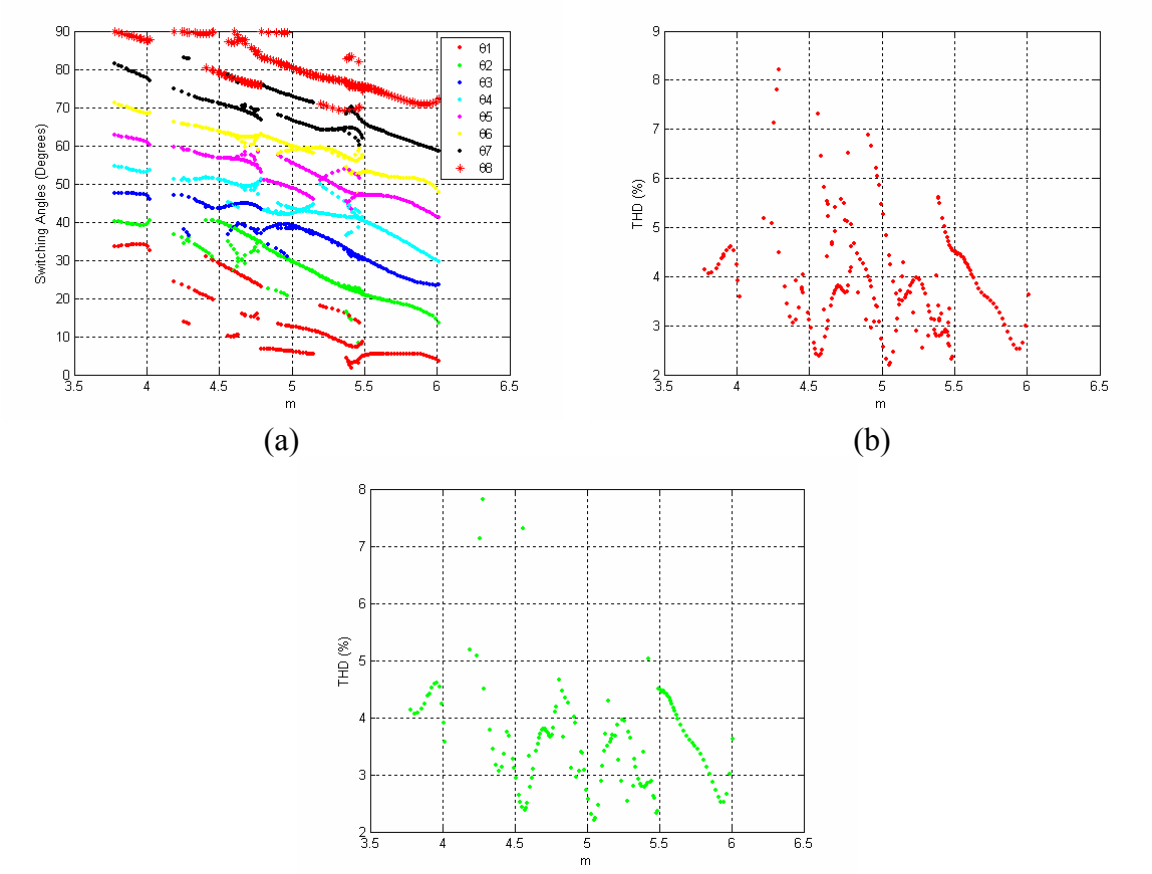


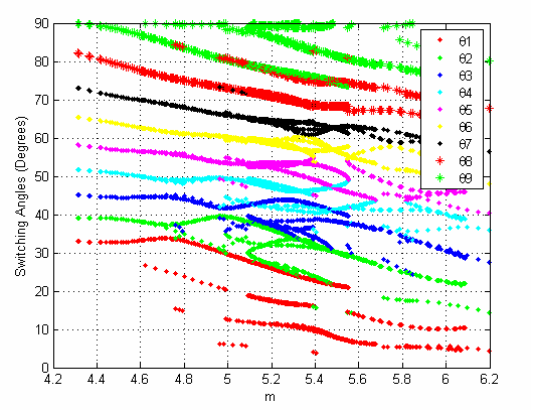
Figure 3.8: Solutions and THD for 15-level multilevel converter (a) switching angles; (b) THD for all solutions; (c) lowest THD



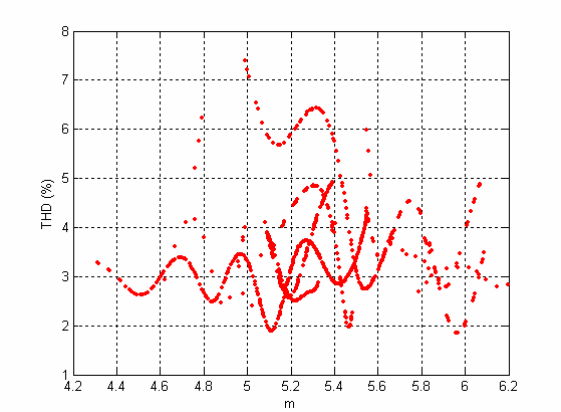
(a) (b)

(c)

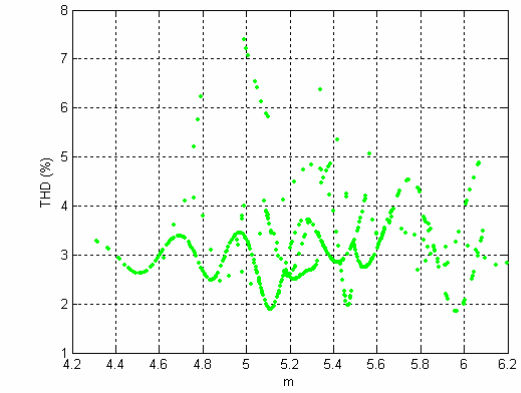
Figure 3.9: Solutions and THD for 17-level multilevel converter (a) switching angles; (b) THD for all solutions; (c) lowest THD



(a)



(b)



(c)

Figure 3.10: Solutions and THD for 19-level multilevel converter (a) switching angles; (b) THD for all solutions; (c) lowest THD

The solutions of switching angles and THD to the 21-level case are shown in Figure 3.11.

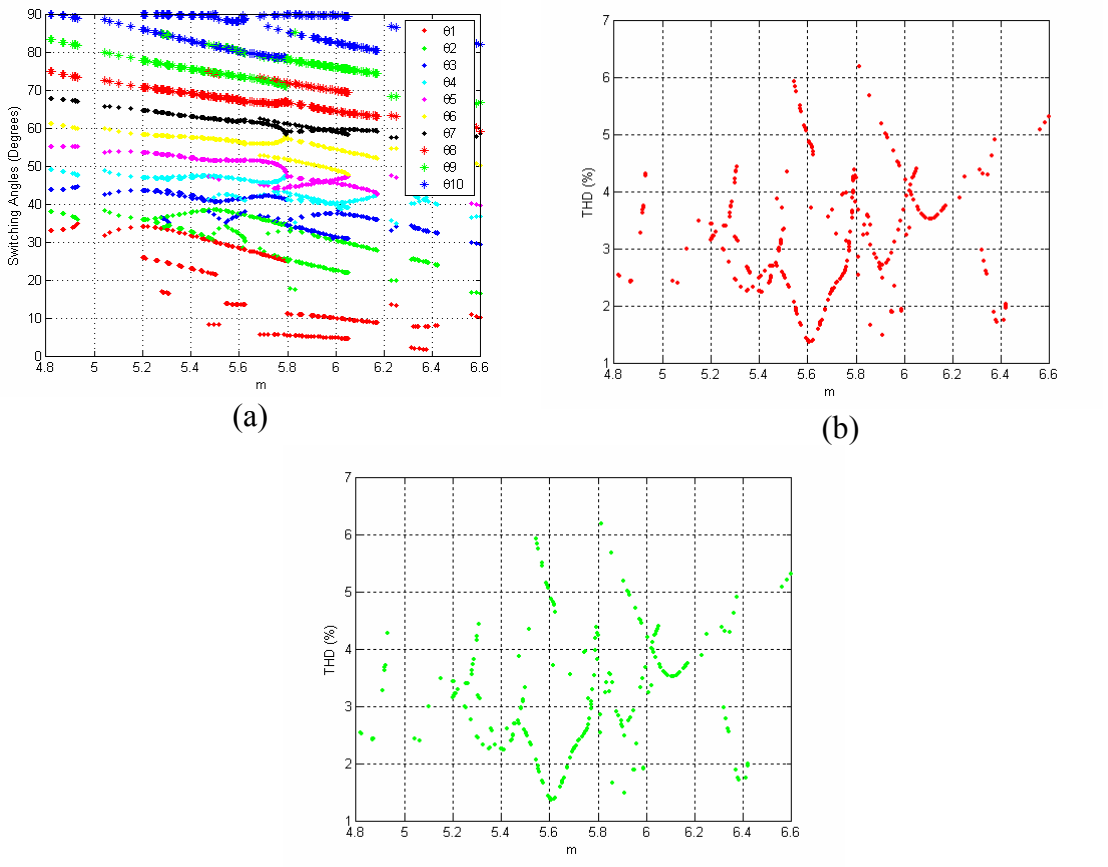
Until now, we have found the fundamental frequency switching angles of multilevel converters up to 21 levels. It can be seen that the THD is decreasing when the number of levels is increasing. This can be seen from the THD plot in Figure 3.12. The THD decreases steadily from 5-level to 11-level. After 11-level, the THD decreases slowly. From the THD figures, it can be seen that most of the THD is below 5% for high-level cases such as from the 11-level case to the 21-level case. If a small filter is used for the output voltage, the THD of the output voltage can reach the application requirement specified in IEEE-519 [18].

3.4. Compensation with the Triplen Harmonics

One disadvantage of the fundamental frequency switching control is its narrow modulation index as discussed in Chapter 2. To extend the linear range of operation for traditional PWM, one method is to inject the third harmonic [7] [10].

The fundamental frequency switching method also can inject triplen harmonics to increase the modulation index range.

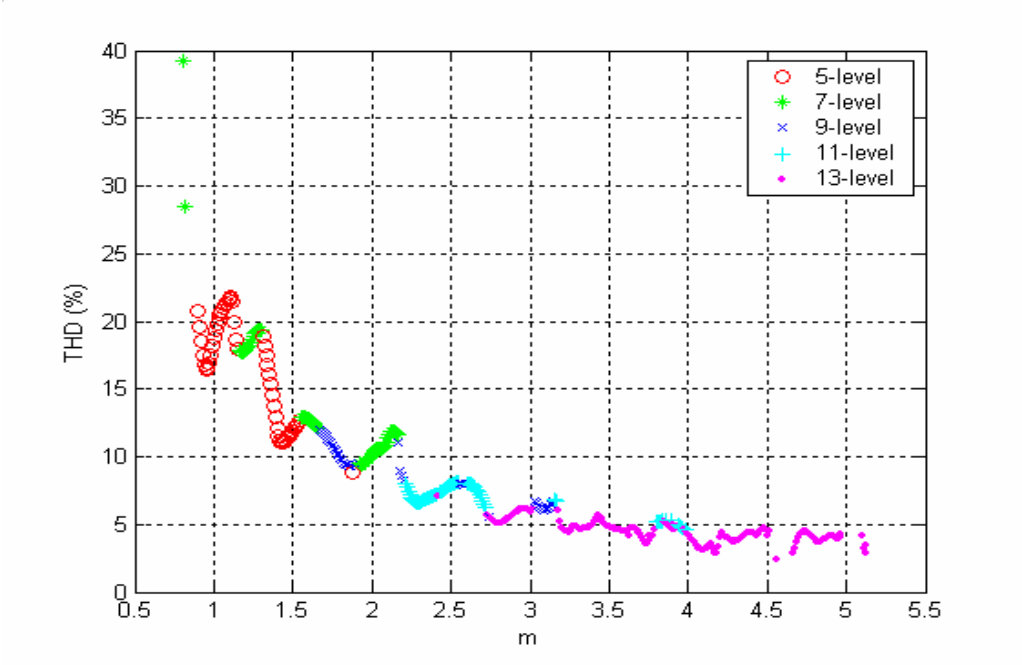
Assume the switching angles $\theta_1, \theta_2, \cdots \theta_s$ are ordered as $\theta_1 \le \theta_2 \le \cdots \le \theta_s$. The working principle is shown in Figure. 3.13. Before it is compensated, the output voltage waveform is shown in Figure 3.13(a): the triplen harmonic injected into the converter is shown in Figure 3.13(b). And the compensated voltage waveform is shown in Figure 3.13(c). It can be seen that to generate the required output voltage, a 5-level multilevel converter is necessary in Figure 3.13(a). But after it is compensated, a 3-level converter can generate the required output voltage waveform shown in Figure 3.13(c). The compensation can be done like this because the triplen harmonic voltage does not change the fundamental frequency content, and cancels in the line-line voltage.



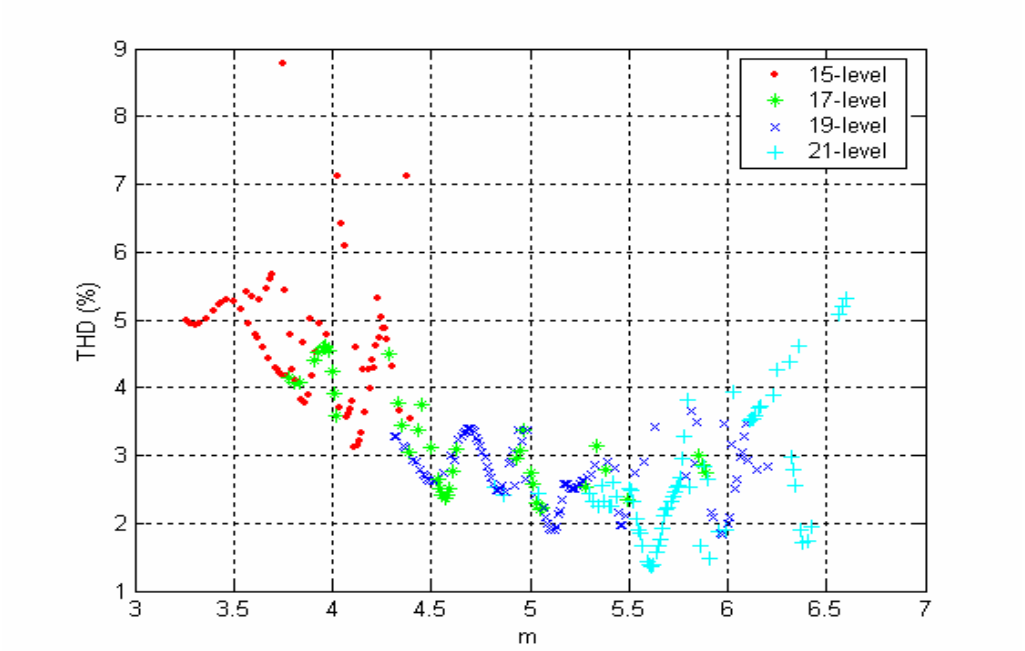
(a) (b)

(c)

Figure 3.11: Solutions and THD for 21-level multilevel converter (a) switching angles; (b) THD for all solutions; (c) lowest THD



(a)



(b)

Figure 3.12: THD for fundamental frequency switching control (a) lowest THD for 5-13 level multilevel converters; (b) lowest THD for 15-21 level multilevel converters

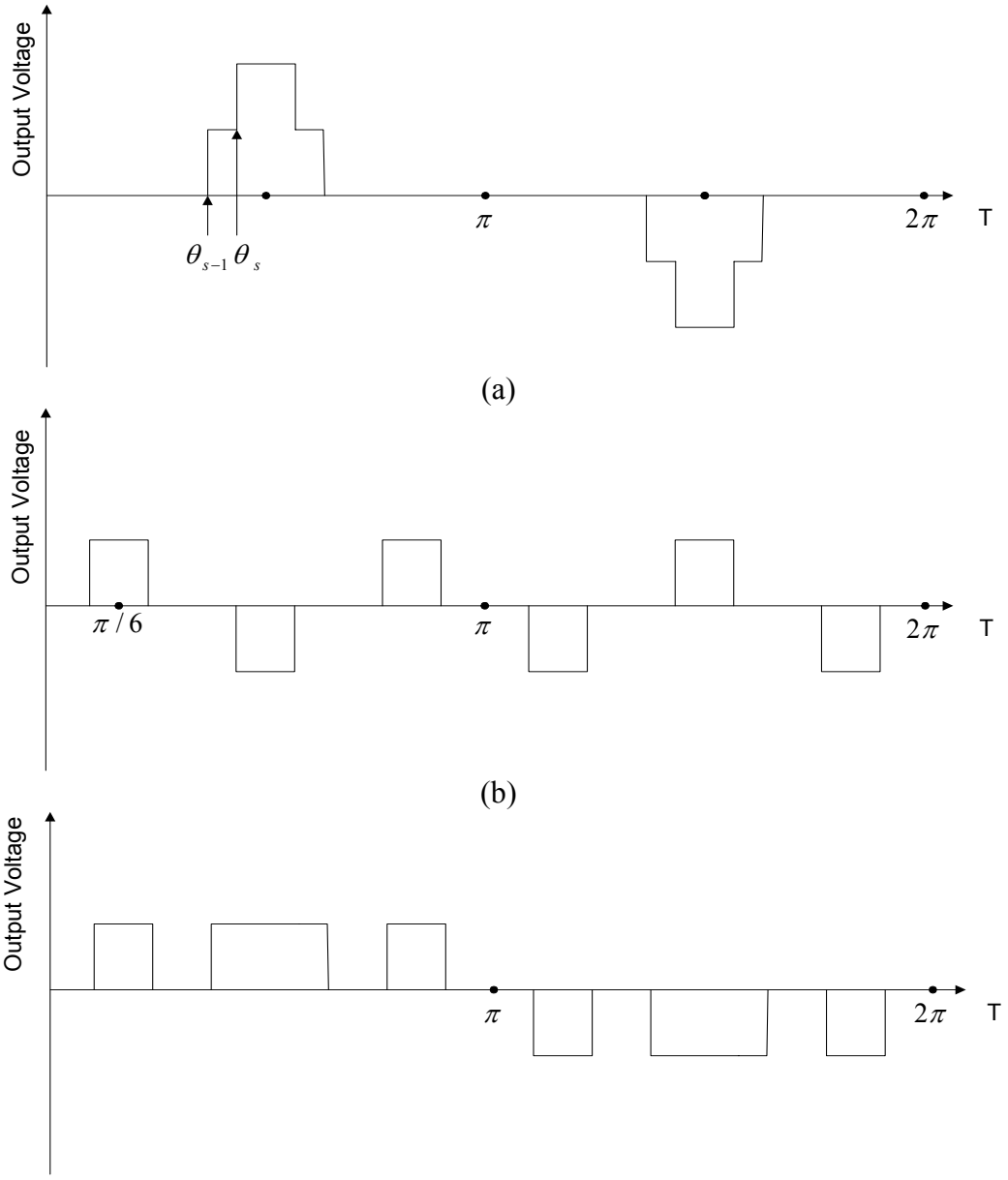


Figure 3.13: Triplen harmonics compensation for multilevel converter control (a) the output voltage waveform without triplen harmonic compensation; (b) the triplen harmonic for compensation; (c) the output voltage waveform with triplen harmonic compensation

From Figure 3.13, it can be shown that if the switching angles satisfy the condition.

$$\frac{2\pi}{3} - \theta_s \le \theta_{s-1} \tag{3.51}$$

Then, multilevel converters with 2*s*-3 voltage levels using tripling harmonic injection can replace multilevel converters with 2*s*-1 voltage levels to output the desired voltage. Similar to this, multilevel converters with $2s-5$ voltage levels using tripling harmonic injection can replace multilevel converters with $2s-3$ voltage levels to output the desired voltage with the condition.

$$\frac{2\pi}{3} - \theta_{s-1} \le \theta_{s-3} \tag{3.52}$$

Repeating this process, all the possible compensations can be found for the fundamental frequency switching angles.

From the compensation shown in Figure 3.13, it can be seen that the triplen harmonic compensation can reduce the required number of voltage levels. This increases the modulation index range. The modulation index range with and without the triplen harmonic compensation is shown in Table 3.1.

Table 3.1. Comparison of the modulation index range with and without triplen harmonic compensation

Level Number	5	7	9	11	13	15	17	19	21
m_{nc*}	0~ 1.9	0~ 2.5	0~ 3.42	0~ 4.23	0~ 5.13	0~ 5.42	0~ 6.01	0~ 6.20	0~ 6.60
m_{c**}	0~ 1.9	0~ 2.76	0~ 3.66	0~ 4.56	0~ 5.42	0~ 6.01	0~ 6.60	N/A	N/A

m_{nc*}: Modulation index range without triplen harmonic compensation using all voltage levels.

m_{c**}: Modulation index range with triplen harmonic compensation using all voltage levels.

From Table 3.1, it can be derived that the triplen harmonic compensation can help to implement a high-level modulation control on a low-level number multilevel converter. This can save the cost for additional hardware. For example, without triplen harmonic compensation, a modulation index m = 6.60 realization must use a 21-level converter, but with triplen harmonics compensation, such a modulation realization just needs a 17-level converter. This can decrease the hardware cost.

3.5. Simulation

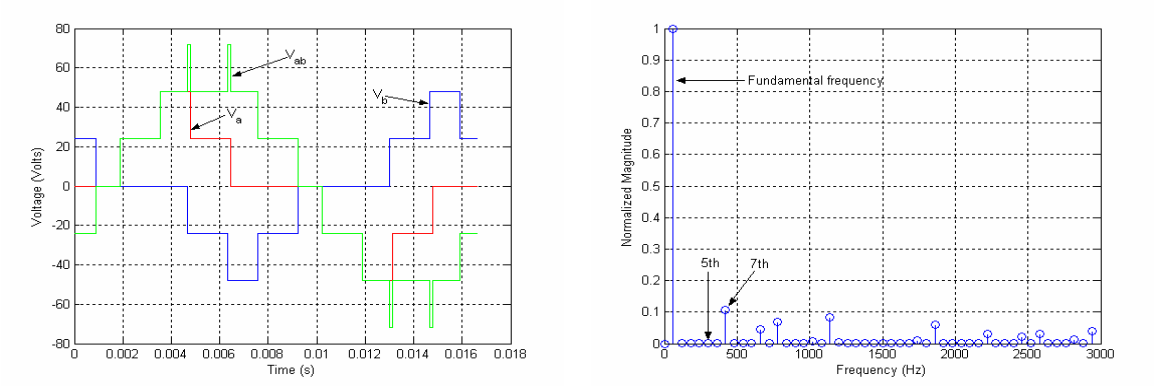
To verify the fundamental frequency switching control method and the third harmonic compensation method, an example for each level cases (5, 7, 9, 11, 13, 15, 17, 19 and 21 level) simulation studies have been implemented.

For practical applications, the voltage level number is fixed. If the required output voltage level number is not greater than that of the multilevel converter, the multilevel converter can output the voltage directly; if the required output voltage level number is greater than that of the multilevel converter, the multilevel converter can not output the voltage directly, and the triplen harmonic compensation is necessary to decrease the required voltage level number. Therefore, in the simulation study, 5, 7, 9, 11 level cases are simulated without triplen harmonic compensation; 13, 15, 17, 19 and 21 level cases are simulated for both with triplen harmonic compensation and without triplen harmonic compensation cases.

To compare the simulation results with the experimental results, the simulation step size is chosen to match the control resolution for the experiments.

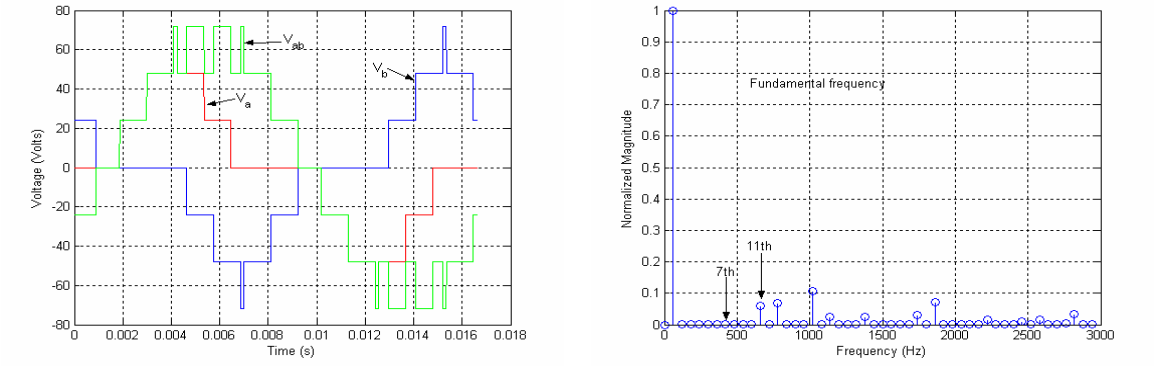
The simulation includes output waveforms and its FFT analysis. The simulation results are shown in Figures 3.14-3.22.

The simulation shows the output phase voltage waveform, output line-line voltage waveform, and normalized FFT analysis of the line-line voltage waveform. Corresponding to the theoretical computation, the harmonic content chosen to be eliminated and the triplen harmonic content should be zero in the normalized FFT analysis of the line-line voltage waveform.



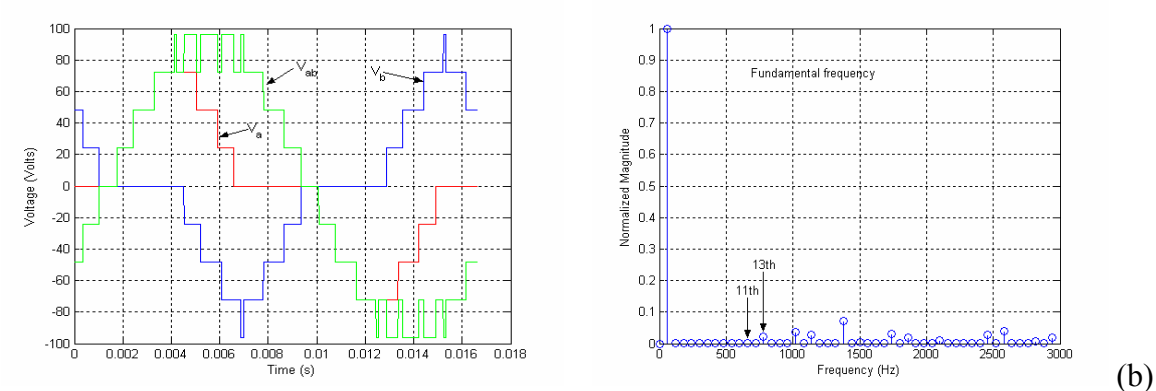
(a) (b)

Figure 3.14: Control simulation for 5-level multilevel converter ($m = 0.99$) (a) output voltage waveform; (b) normalized FFT analysis of line-line voltage



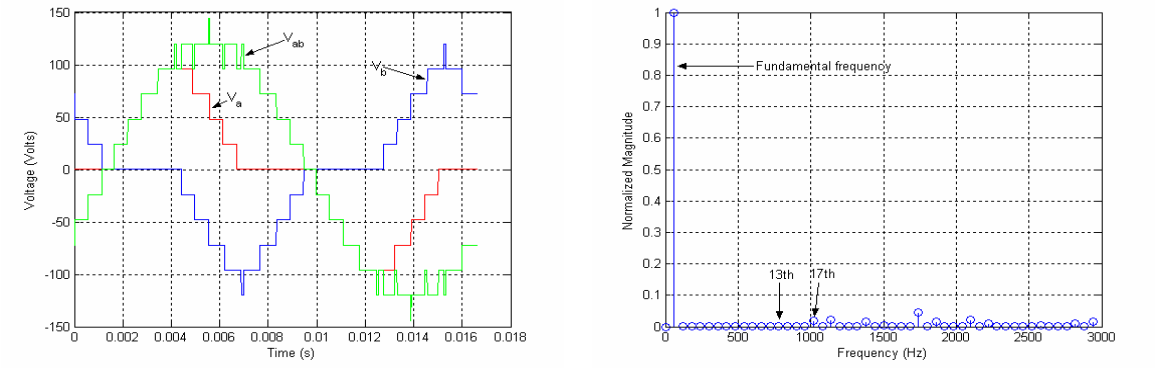
(a) (b)

Figure 3.15: Control simulation for 7-level multilevel converter ($m = 1.22$) (a) output voltage waveform; (b) normalized FFT analysis of line-line voltage



(a) (b)

Figure 3.16: Control simulation for 9-level multilevel converter ($m = 1.74$) (a) output voltage waveform; (b) normalized FFT analysis of line-line voltage



(a) (b)

Figure 3.17: Control simulation for 11-level multilevel converter ($m = 2.28$) (a) output voltage waveform; (b) normalized FFT analysis of line-line voltage

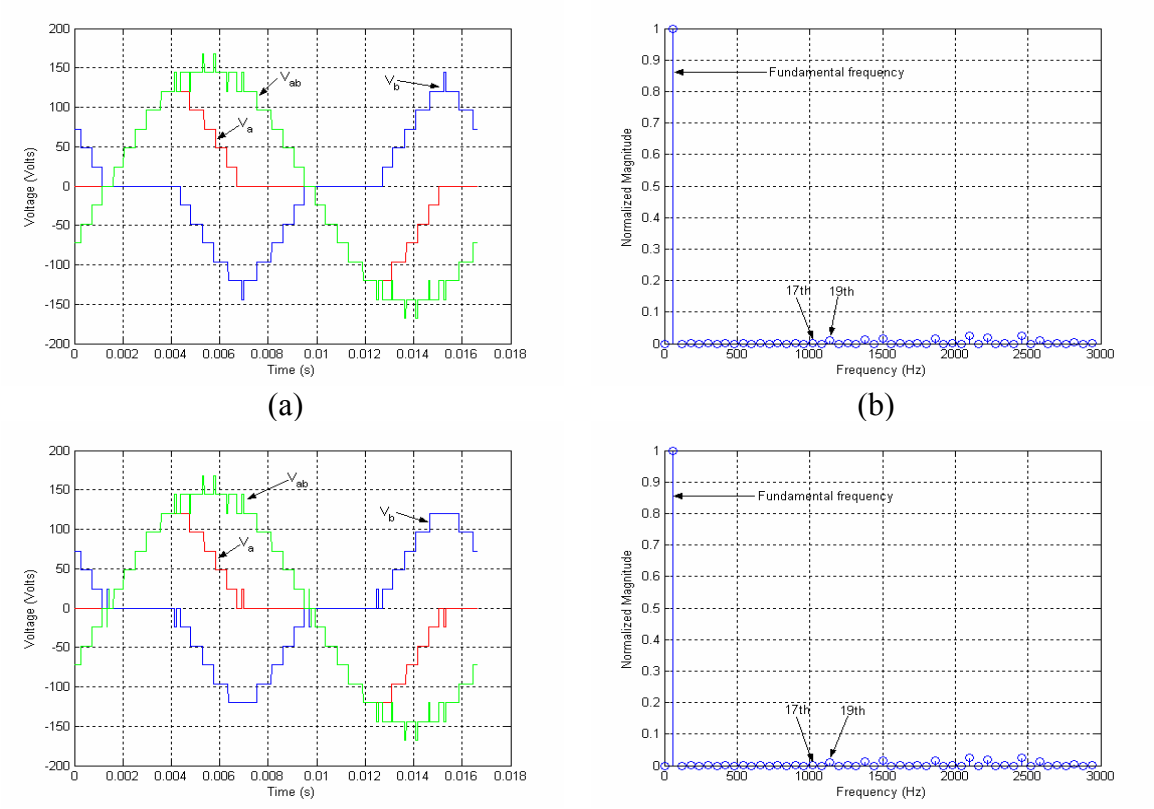


Figure 3.18: Control simulation for 13-level multilevel converter ($m = 2.80$) (a) output voltage waveform without triplen harmonics compensation; (b) normalized FFT analysisof line-line voltage without triplen harmonics compensation; (c) output voltage waveform with triplen harmonics compensation; (d) normalized FFT analysis of line-line voltage with triplen harmonics compensation

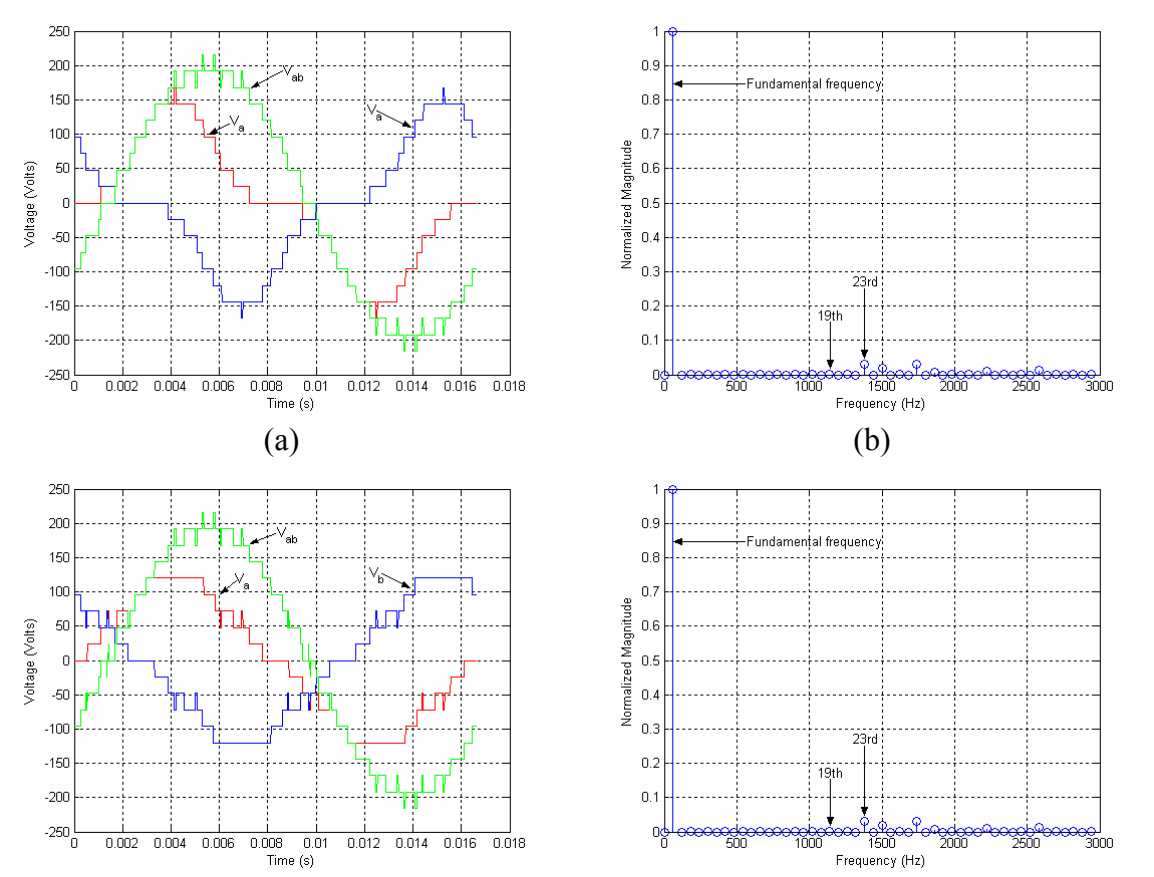


Figure 3.19: Control simulation for 15-level multilevel converter ($m = 3.50$) (a) output voltage waveform without triplen harmonics compensation; (b) normalized FFT analysis of line-line voltage without triplen harmonics compensation; (c) output voltage waveform with triplen harmonics compensation; (d) normalized FFT analysis of line-line voltage with triplen harmonics compensation

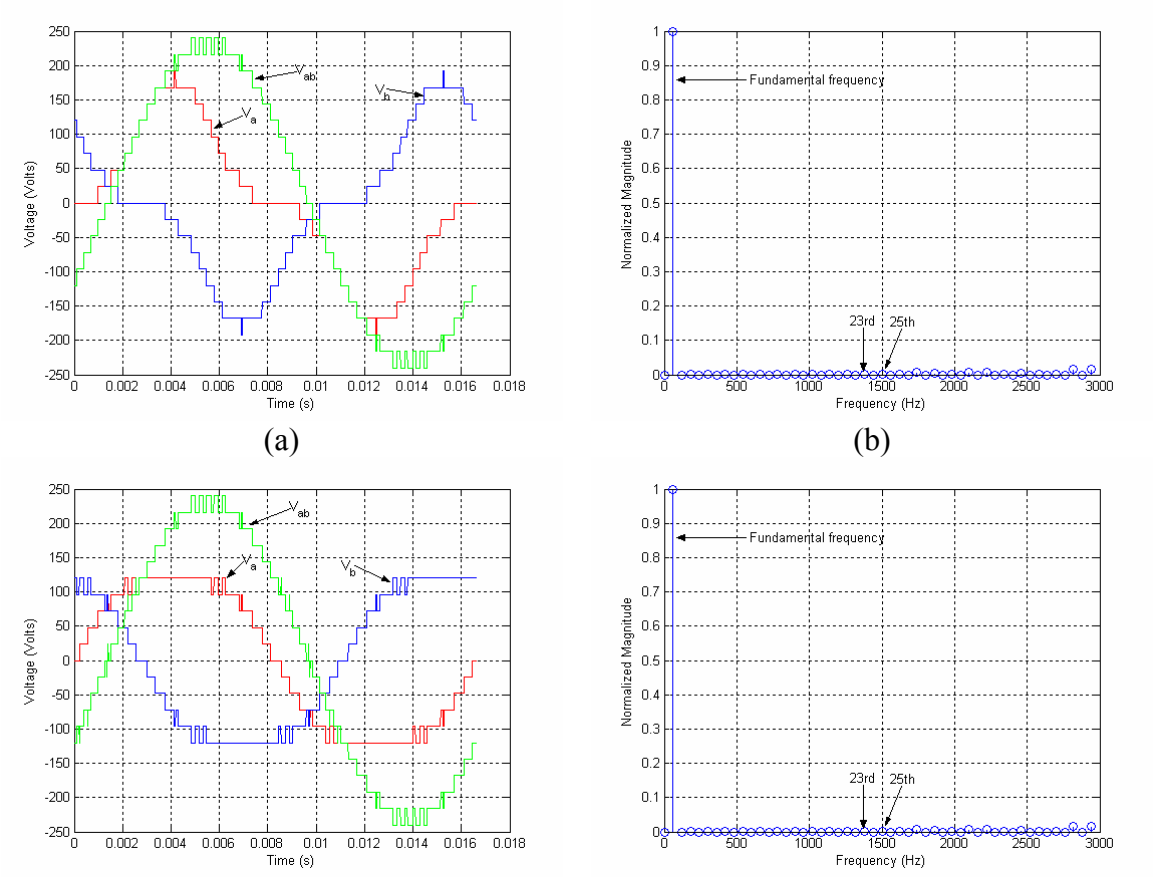


Figure 3.20: Control simulation for 17-level multilevel converter ($m = 3.95$) (a) output voltage waveform without triplen harmonics compensation; (b) normalized FFT analysis of line-line voltage without triplen harmonics compensation; (c) output voltage waveform with triplen harmonics compensation; (d) normalized FFT analysis of line-line voltage with triplen harmonics compensation

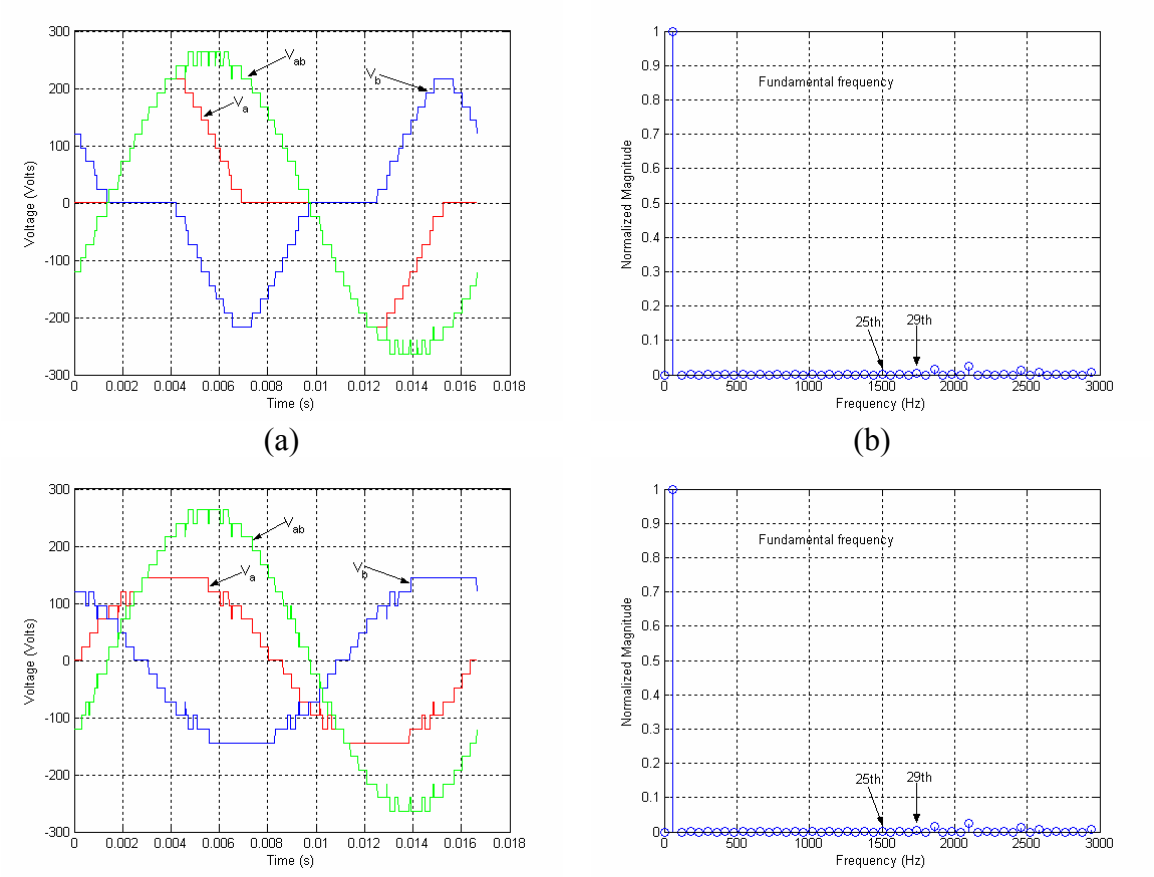


Figure 3.21: Control simulation for 19-level multilevel converter ($m = 4.67$) (a) output voltage waveform without triplen harmonics compensation; (b) normalized FFT analysis of line-line voltage without triplen harmonics compensation; (c) output voltage waveform with triplen harmonics compensation; (d) normalized FFT analysis of line-line voltage with triplen harmonics compensation

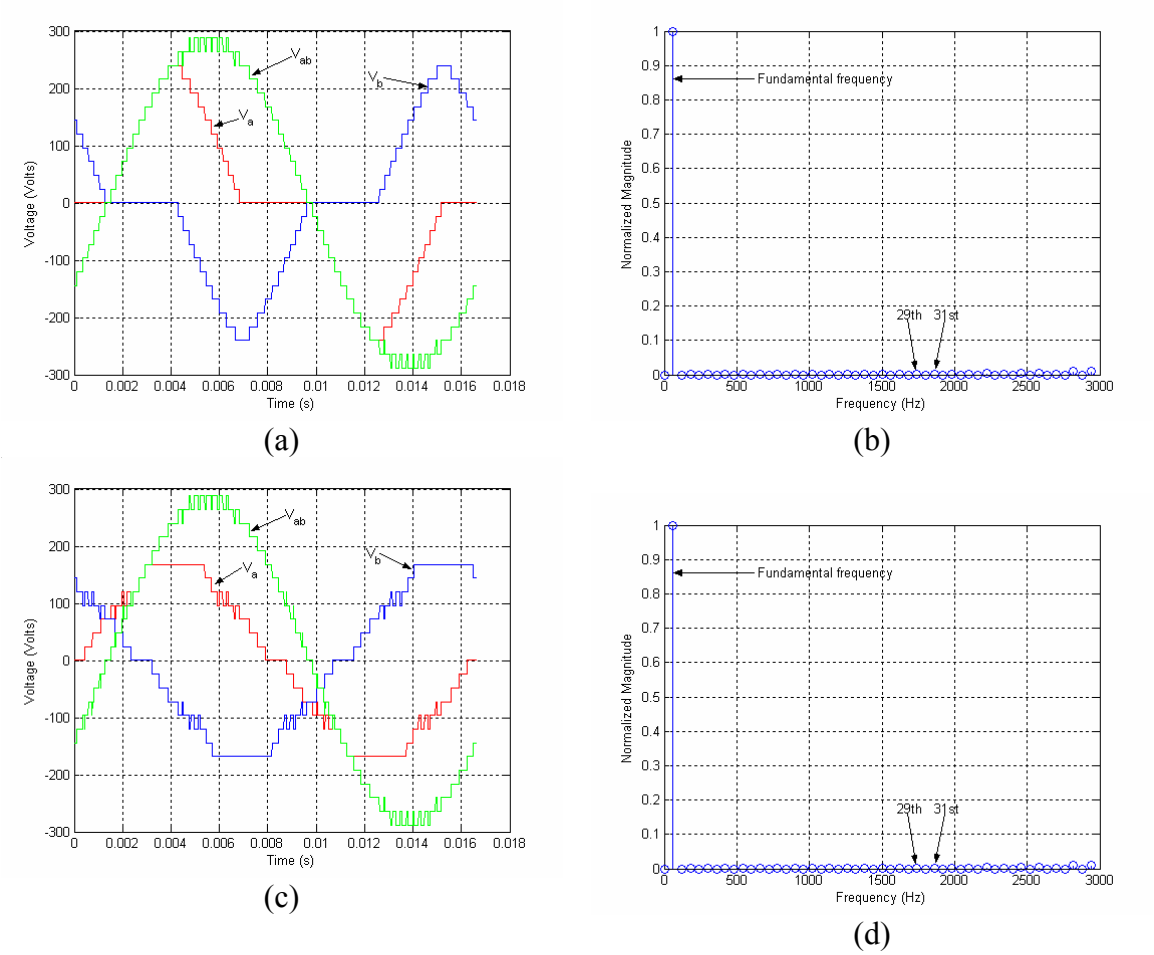


Figure 3.22: Control simulation for 21-level multilevel converter ($m = 4.92$) (a) output voltage waveform without triplen harmonics compensation; (b) normalized FFT analysis of line-line voltage without triplen harmonics compensation; (c) output voltage waveform with triplen harmonics compensation; (d) normalized FFT analysis of line-line voltage with triplen harmonics compensation

From the FFT analysis of simulation voltages for 5-21 level multilevel converters, it can be seen that the fundamental frequency switching control for 5-21 level multilevel converters eliminate a certain number of hamonics that correspond to the theoretical computation. The simulation results shown that the 13, 15, 17 level simulation cases can be implemented on an 11-level multilevel converter, the 19-level case can be implemented on a 13-level multilevel converter, and the 21-level case can be implemented on a 15-level multilevel converter. These results correspond well with the theoretical computation of triplen harmonics compensation.

Next, experiments are implemented to validate the simulation results.

3.6. Experiment

To experimentally validate the fundamental frequency switching method, an 11-level case without compensation and a 17-level case with compensation are implemented on an 11-level H-bridge multilevel converter and each level configured with 24 Volts. The detail of experiment setup is described in Chapter 7.

The experiments include the phase voltages, line-line voltages and their FFT analysis. The experimental results for the 11-level case without compensation are shown in Figure 3.23. In Figure 3.23, (a) and (b) are phase voltage and line-line voltages, respectively; (c) and (d) are normalized FFT analysis of the line-line voltage. It can be seen that the 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonics are all below 0.5%. The FFT analysis confirms that the 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonics are eliminated as expected.

The experimental results for the 17-level case with compensation are shown in Figure 3.24. In Figure 3.24, (a) and (b) are phase voltage and line-line voltage, respectively; (c) and (d) are normalized FFT analysis of line-line voltage. It can be seen that the 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, 19^{th}, 21^{st} and 23^{rd} harmonics are all below 0.2%. The FFT analysis confirms that the 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, 19^{th}, 21^{st} and 23^{rd} harmonics are eliminated as expected.

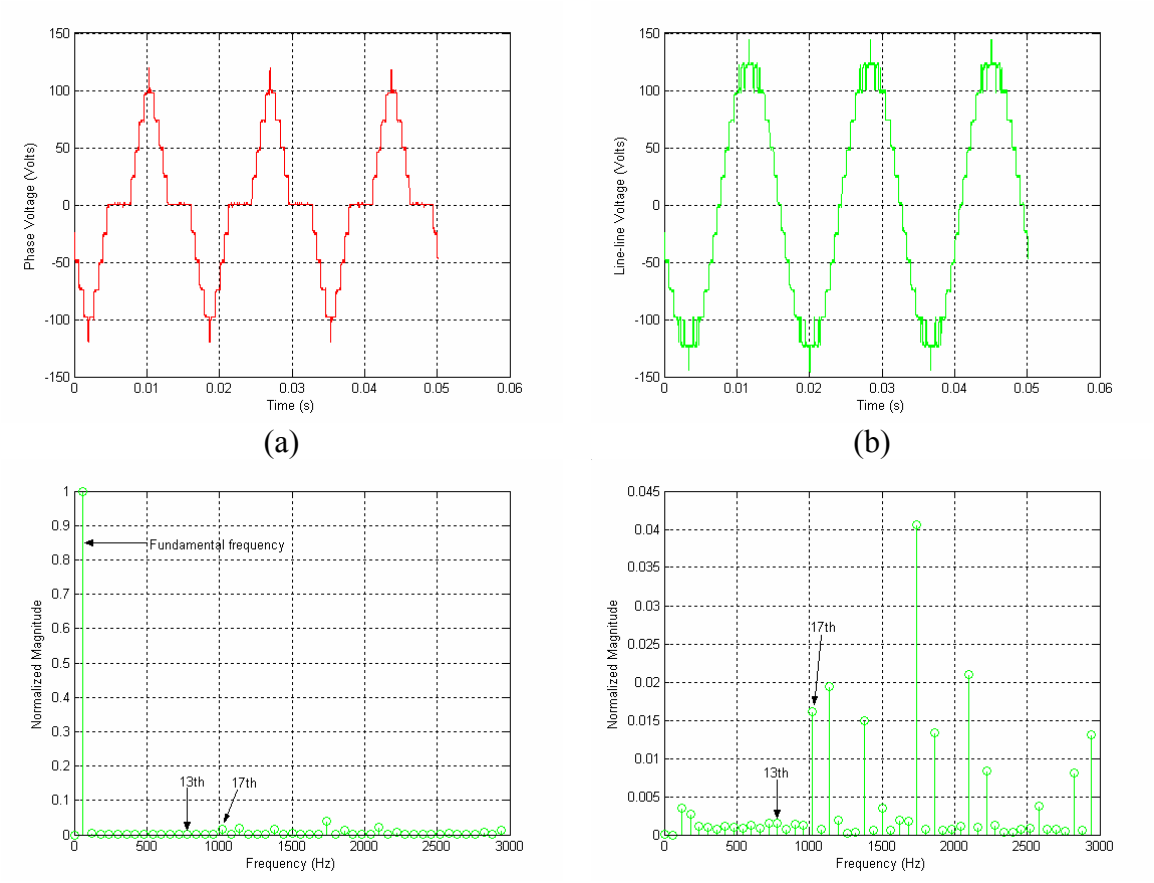


Figure 3.23: Experimental results of 11-level multilevel converter control ($m = 2.28$) (a) phase voltage; (b) line-line voltage; (c) normalized FFT analysis of line-line voltage; (d) normalized harmonic contents of line-line voltage with fundamental content removed

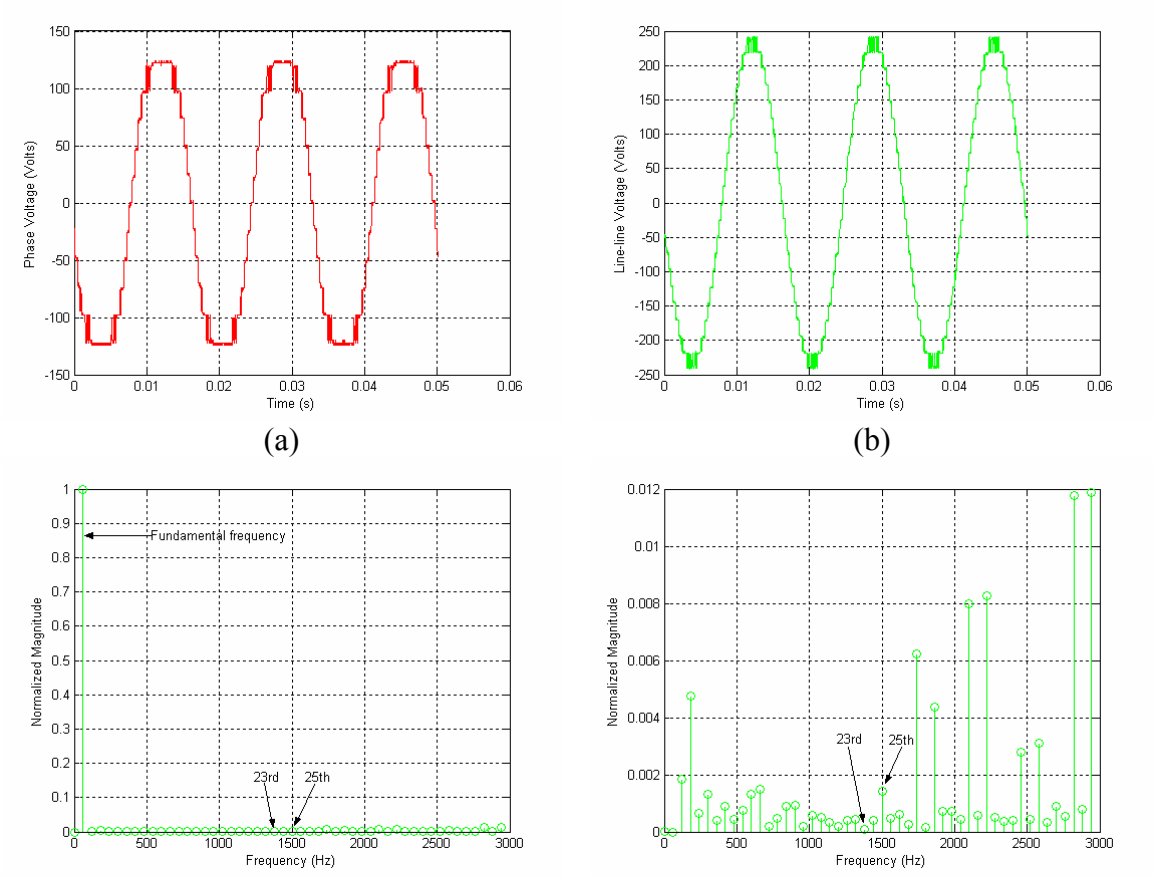


Figure 3.24: Experimental results of 17-level multilevel converter control with triplen harmonics compensation ($m = 3.95$) (a) phase voltage; (b) line-line voltage; (c) normalized FFT analysis of line-line voltage; (d) normalized harmonic contents of line-line voltage with fundamental content removed

From the experimental results of phase voltage, it also confirms that the 17-level voltage case can be implemented in an 11-level multilevel converter after the triplen harmonic compensation. Here, the experiment also validates that the triplen harmonic compensation method can increase the modulation index range.

3.7. Summary

In this chapter, the fundamental frequency switching angles of multilevel converters up to 21 levels have been found. It can be seen that the THD is decreasing when the number of levels is increasing. The THD decreases steadily from the 3-level case to the 11-level case. But the THD decreases slowly from the 13-level case to the 21-level case. Because low order harmonics have been eliminated, only a small filter is necessary to be used for the output voltage. It will be easy for the output voltage to satisfy the THD requirements in IEEE-519.

The triplen harmonic compensation method can be used to increase the modulation index range of the fundamental frequency switching control. The simulation results and experimental results validated the theoretical computation and the triplen harmonic compensation method.

The next chapter will present the method of eliminating harmonics for the low modulation index cases to decrease the THD beyond what is possible with fundamental frequency switching control.

4. Active Harmonic Elimination for Low Modulation Index Control

In the previous chapter, the switching angles for fundamental frequency switching control have been computed. From the computed THD, it can be seen that THD for low modulation index is higher than that of high modulation index. To decrease the THD for low modulation index cases, a new method must be developed to eliminate more harmonics.

In this chapter, the active harmonic elimination method is developed to eliminate more harmonics for multilevel converters based on the previous fundamental frequency switching control method.

In the first part of this chapter, resultant theory and harmonic elimination theory will be reviewed briefly. Then the active harmonic elimination method is presented.

In the second part of the chapter, the simulation results will be given for the proposed active harmonic elimination method.

In the third part of the chapter, experimental results will be used to validate the active harmonic elimination method.

4.1. Active Harmonic Elimination Method

4.1.1. Resultant Method for Multilevel Converter

As mentioned previously, a multilevel converter uses several DC voltages to synthesize a sinusoidal voltage wave. Thus, the control of the multilevel converter is to choose a series of switching angles to synthesize a desired sinusoidal voltage waveform. A typical multilevel converter output with fundamental frequency switching control is shown in Figure 2.7. The Fourier series expansion of the output voltage waveform is

$$V(t) = \sum_{n=1,3,5...}^{\infty} \frac{4V_{dc}}{n\pi}(\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3) + ... + \cos(n\theta_s))\sin(n\omega t) \quad (4.1)$$

where s is the number of DC voltages. Given a desired fundamental voltage V_1, one wants to determine the switching angles $\theta_1, \theta_2, \cdots, \theta_s$ so that $V(t) = V_1 \sin(\omega t)$, and specific higher order harmonics of V_h are equal to zero. For a three-phase application, the triplen harmonics in each phase need not be cancelled as they automatically cancel in the line-to-line voltages. For example, as mentioned in Chapter 3, in the case of $s = 5$ DC voltages, the 5th, 7th, 11th, 13th order harmonics can be cancelled. This is the control method that has been discussed in the previous chapters.

4.1.2. Active Harmonic Elimination Method

From equation (4.1), the voltage contents can be divided into four parts:

$$V(t) = V_{p1}(t) + V_{p2}(t) + V_{p3}(t) + V_{p4}(t) \tag{4.2}$$

1. Fundamental frequency voltage.

$$V_{p1}(t) = \frac{4V_{dc}}{\pi}[\cos(\theta_1) + \cos(\theta_2) + \cdots + \cos(\theta_s)]\sin(\omega t) \tag{4.3}$$

2. Triplen harmonic voltages.

$$V_{p2}(t) = \frac{4V_{dc}}{n\pi} \sum_{n=3,9,15,\cdots} [\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_s)]\sin(n\omega t) \tag{4.4}$$

3. Low order harmonic voltages that can be eliminated by applying resultant method or Newton's method.

$$V_{p3}(t) = \frac{4V_{dc}}{n\pi} \sum_{n=5,7,11,13} [\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_s)]\sin(n\omega t) \tag{4.5}$$

4. High order harmonic voltages that cannot be eliminated by applying resultant method or Newton method.

$$V_{p4}(t) = \frac{4V_{dc}}{n\pi} \sum_{n=17,19,23,\cdots} [\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_s)]\sin(n\omega t) \tag{4.6}$$

Using the resultant method or Newton's method, part (4.5) is eliminated using a fundamental frequency switching method. Assuming the application is a balanced three-phase system, part (4.4) need not be eliminated. This then leaves part (4.6), which is the source of THD in the multilevel converter output voltage.

Now, the fundamental problem is: how can the harmonics be eliminated? One basic idea is, if the harmonic magnitude and phase can be computed, one can generate a signal with same magnitude and the phase difference is 180°. Then the harmonic can be cancelled, and will not remain in the output voltages.

Fortunately, from the discussion above, the h^{th} harmonic can be computed as

$$V_h(t) = \frac{4V_{dc}}{h\pi}(\cos(h\theta_1) + \cos(h\theta_2) + \cos(h\theta_3) + ... + \cos(h\theta_s))\sin(h\omega t) \tag{4.7}$$

From (4.7), it can be seen that the harmonic magnitude is

$$A_h = \frac{4V_{dc}}{h\pi}(\cos(h\theta_1) + \cos(h\theta_2) + \cos(h\theta_3) + ... + \cos(h\theta_s)) \tag{4.8}$$

And the initial phase is:

$$\varphi = 0 \tag{4.9}$$

So a signal such as

$$V_{ch\_i}(t) = -A_h \sin(h\omega t) = -A_h \sin(\omega_h t) \tag{4.10}$$

is desired to be generated to cancel the h^{th} harmonic, and $\omega_h = h\omega$. For convenience, here, define

$$A_{h\_n} = \frac{A_h}{\frac{4V_{dc}}{\pi}} = \frac{1}{n}(\cos(h\theta_1) + \cos(h\theta_2) + \cos(h\theta_3) + ... + \cos(h\theta_s)) \tag{4.11}$$

as the normalized harmonic magnitude.

However, the practical multilevel converter cannot generate a sinusoidal signal like (4.10). A practical converter can just generate a square wave signal, which can be expressed by Fourier series expansion as

$$V_c(t) = A_h \sum_{n_c=1,3,5...}^{\infty} \frac{1}{n_c}\cos(n_c\theta_h)\sin(n_c\omega_h t) \tag{4.12}$$

Then subtract (4.12) from (4.6) and set $h = 17$,

$$\begin{aligned} V_{p4}(t) &= \frac{4V_{dc}}{n\pi} \sum_{n=19,23,\cdots} [\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_s)]\sin(n\omega t) \\ &- A_h \sum_{n_c=3,5...}^{\infty} \frac{1}{n_c}\cos(n_c\theta_h)\sin(n_c\omega_h t) \end{aligned} \tag{4.13}$$

It is obvious that the 17th harmonic has been eliminated, but new harmonics have been generated. The next harmonic of concern that is produced by (4.12) is the 5th harmonic, which is at 5×17 = 85. This harmonic and higher ones (7×17, etc.) are easy to filter using a low-pass filter.

To generate the compensation harmonic, the switching angle should be computed first. Because the compensation harmonic is generated by the multilevel converter itself, the voltage magnitude is V_{dc}. Therefore, the magnitude and switching angle are:

$$A_h = \frac{4V_{dc}}{h\pi}(\cos(h\theta_1) + \cos(h\theta_2) + \cos(h\theta_3) + ... + \cos(h\theta_s)) = \frac{4V_{dc}}{\pi}\cos(\theta_h) \quad (4.14)$$

where

$$\theta_h = \cos^{-1}(\frac{1}{h}(\cos(h\theta_1) + \cos(h\theta_2) + \cos(h\theta_3) + ... + \cos(h\theta_s))) \quad (4.15)$$

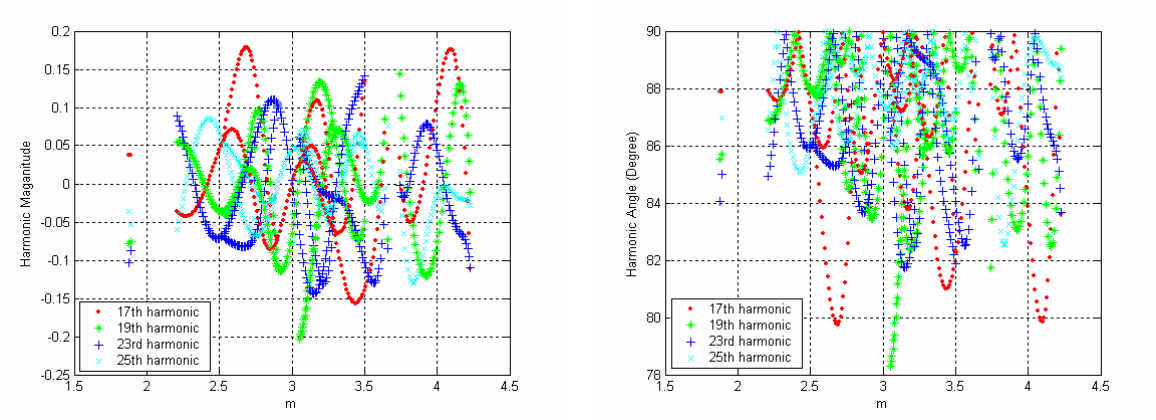
and the THD computation is defined as in chapter 3,

$$THD = \sqrt{\frac{V_5^{\,2} + V_7^{\,2} + \cdots + V_{47}^{\,2} + V_{49}^{\,2}}{V_1^{\,2}}} \quad (4.16)$$

For different modulation indices, the magnitudes of these harmonics are different. For example, the normalized 17th, 19th, 23rd, 25th harmonic magnitudes and harmonic angles are shown in Figure 4.1. An example of a generated signal to cancel 17th harmonic is shown in Figure 4.2.

The THD for fundamental frequency switching method with all solution sets and the THD for active harmonic elimination method that the harmonics are eliminated up to 31st are shown in Figure 4.3 (a). The lowest THD for fundamental frequency switching method and active harmonic elimination method are shown in Figure 4.3 (b).

From Figure 4.3, it can be seen that the THD for the active harmonic elimination method is much lower than that of fundamental frequency switching method. For most modulation indices, the active harmonic elimination method has THD less than 4%. Because the residual harmonics of the active harmonic elimination method are higher frequency than that of the fundamental frequency switching method, it will be easier to filter out the harmonics.



(a) (b)

Figure 4.1: Normalized the 17th, 19th, 23rd, 25th harmonic magnitude and their compensation switching angles (a) normalized magnitudes; (b) compensation angles

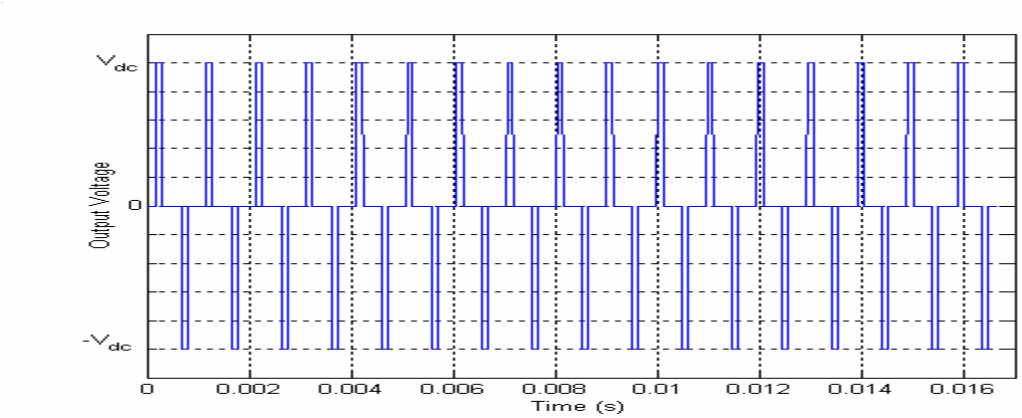
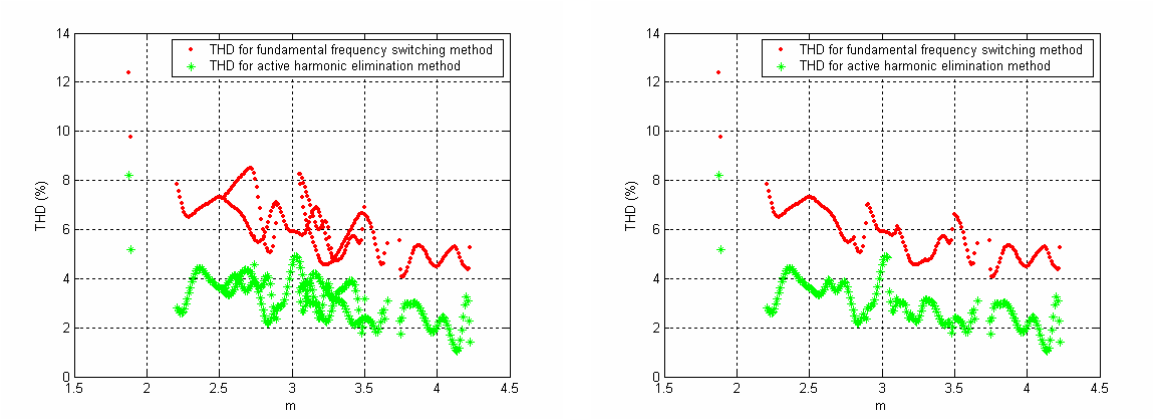


Figure 4.2: Example of compensation signal of the 17th harmonic



(a) (b)

Figure 4.3: THD for fundamental frequency switching method and active harmonic elimination method (a) THD for all solutions; (b) lowest THD

4.2. Simulation Study

4.2.1. Output Waveform Simulation and FFT Analysis

To verify the active harmonic elimination method, a simulation has been implemented. The simulation includes the output voltage waveform and its normalized FFT analysis.

1. Fundamental frequency switching case.

The simulation ($m = 2.28$) results are shown in Figure 4.4.

The THD for the simulation is 6.50%, which corresponds well to the theoretical computation of 6.52%. It also can be seen that the 5-13th odd, non-triplen harmonics in the FFT analysis of phase voltage and line-line voltage are zero.

2. Harmonic elimination up to 31st case.

The simulation ($m = 2.28$) results are shown in Figure 4.5.

The THD for the simulation is 3.30%, which corresponds well to the theoretical computation of 3.18%. It also can be seen that the 5-31st odd, non-triplen harmonics in the FFT analysis of phase voltage and line-line voltage are zero.

From Figure 4.5, it also can be seen that the simulation voltage is beyond the capability of an 11-level multilevel converter output. The voltage is too high for an 11-level multilevel converter to produce. To produce such a high voltage, at least a 13-level multilevel converter is necessary. This result is not what we want since now we are working on an 11-level multilevel converter case. We want to use an 11-level converter to produce the output voltage. To conquer this problem, the triplen harmonic compensation method developed in chapter 3 now is applied to the multilevel converter control. The phase output voltage is shown in Figure 4.6. The triplen harmonic compensation method does not change the line-line voltage and THD as mentioned in chapter 3.

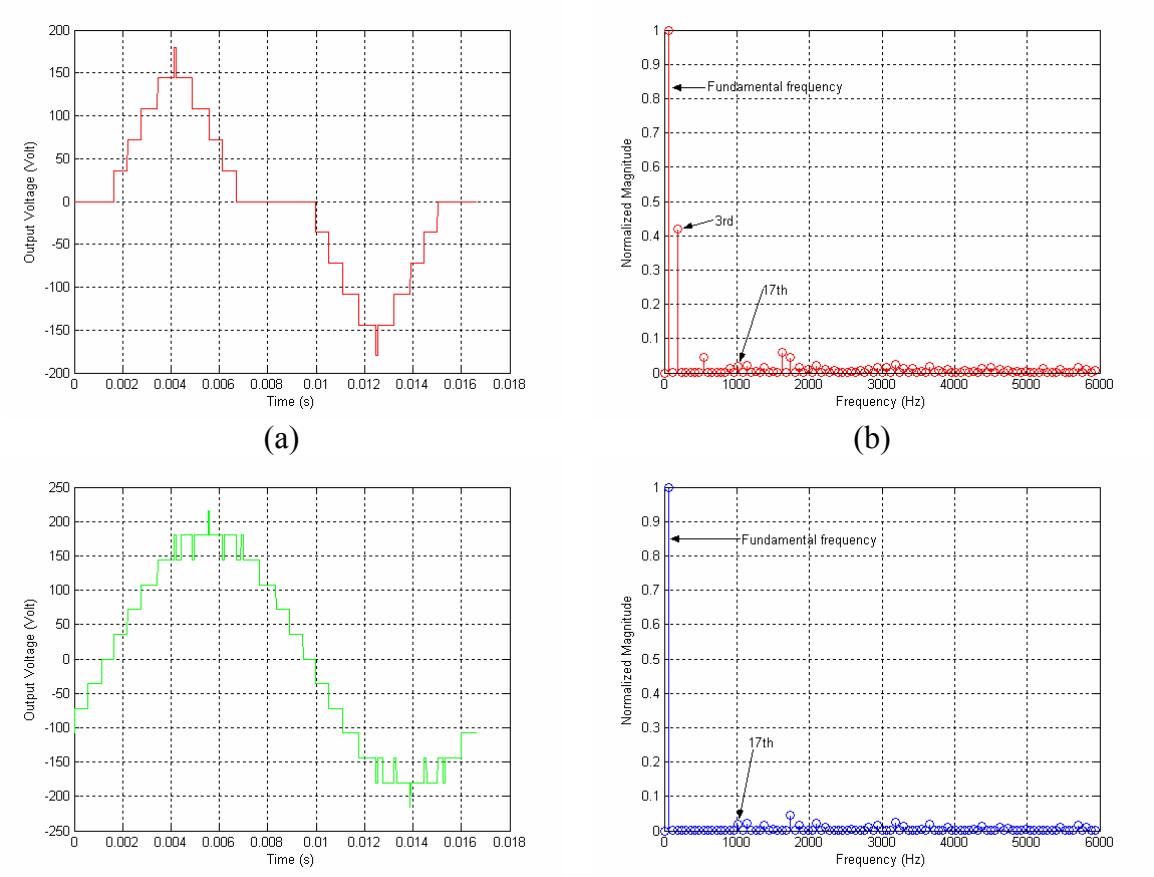


Figure 4.4: Fundamental frequency switching case simulation ($m = 2.28$) (a) phase voltage; (b) normalized FFT analysis of phase voltage; (c) line-line voltage; (d) normalized FFT analysis of line-line voltage

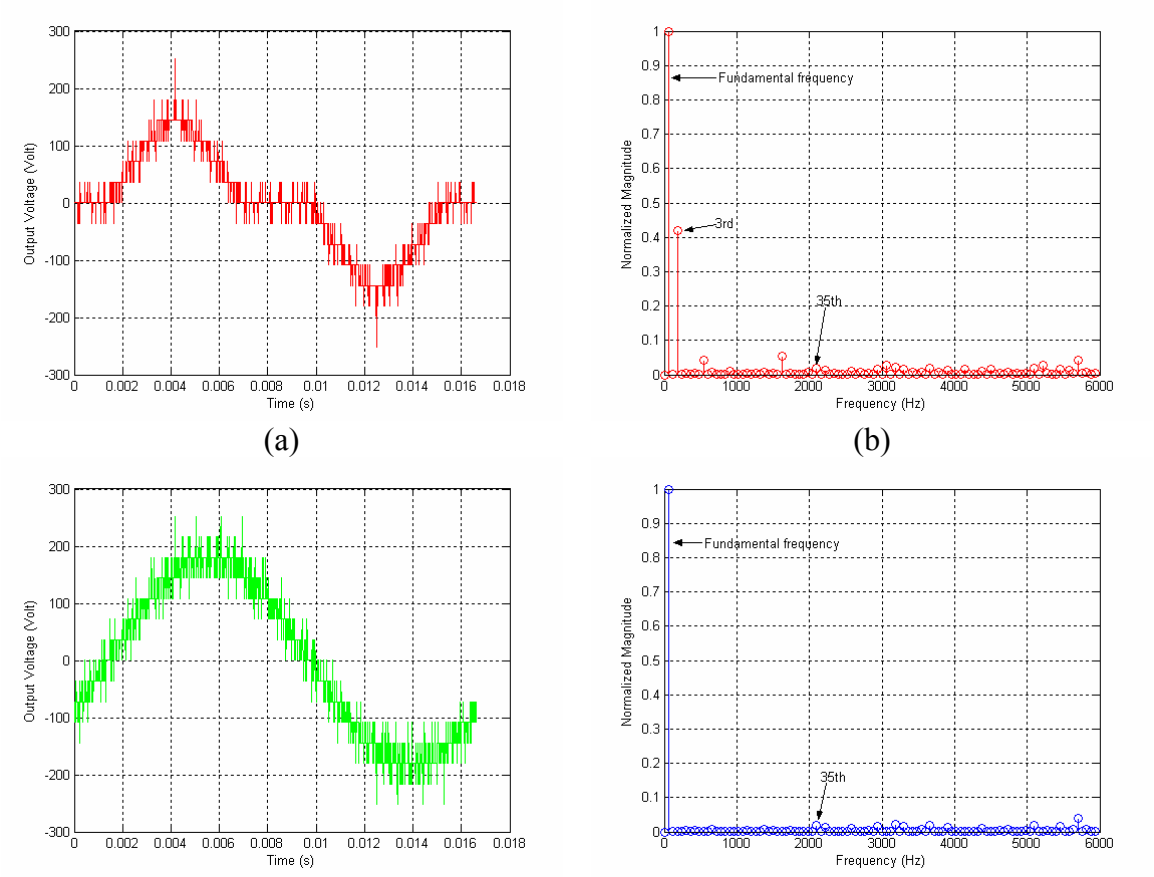


Figure 4.5: Harmonic elimination up to the 31st case simulation ($m = 2.28$) (a) phase voltage; (b) normalized FFT analysis of phase voltage; (c) line-line voltage; (d) normalized FFT analysis of line-line voltage

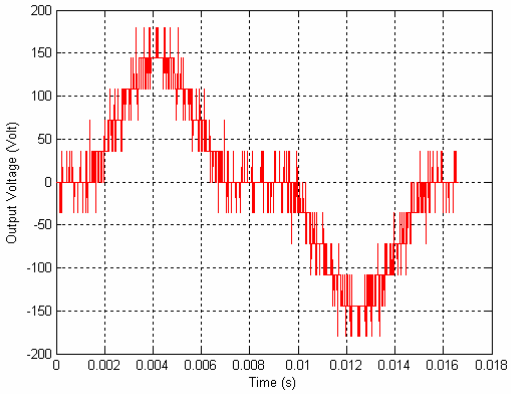


Figure 4.6: Phase voltage with the 5-31st odd, non-triplen harmonic eliminated with triplen harmonic compensation ($m = 2.28$)

3. Harmonic elimination up to 49th case.

The simulation ($m = 2.28$) results are shown in Figure 4.7. It also can be seen that the 5-49th odd, non-triplen harmonic in the FFT analysis of phase voltage and line-line voltage are zero. If we just compute THD up to the 50th harmonic, the THD is zero because all harmonics below the 49th have been eliminated. If we compute THD up to the 80th harmonic, the THD is 4.31%, which is from the higher order harmonics.

4.2.2. Switching Control Strategy

To balance the switching loss during a whole cycle, the first-on, first-off strategy is employed to control the switching here. The control flow chart is shown in Figure 4.8.

For example, the five switching control signals for an 11-level converter with 5 DC sources for $m = 2.28$ are shown in Figure 4.9.

From the figures of the switching signals, it can be seen that switching occurs in a whole cycle. This can help to balance the load and the switching loss between several levels. It also can be derived that this strategy distributes the switching times between several levels, so each level can get almost the same average switching times in a cycle.

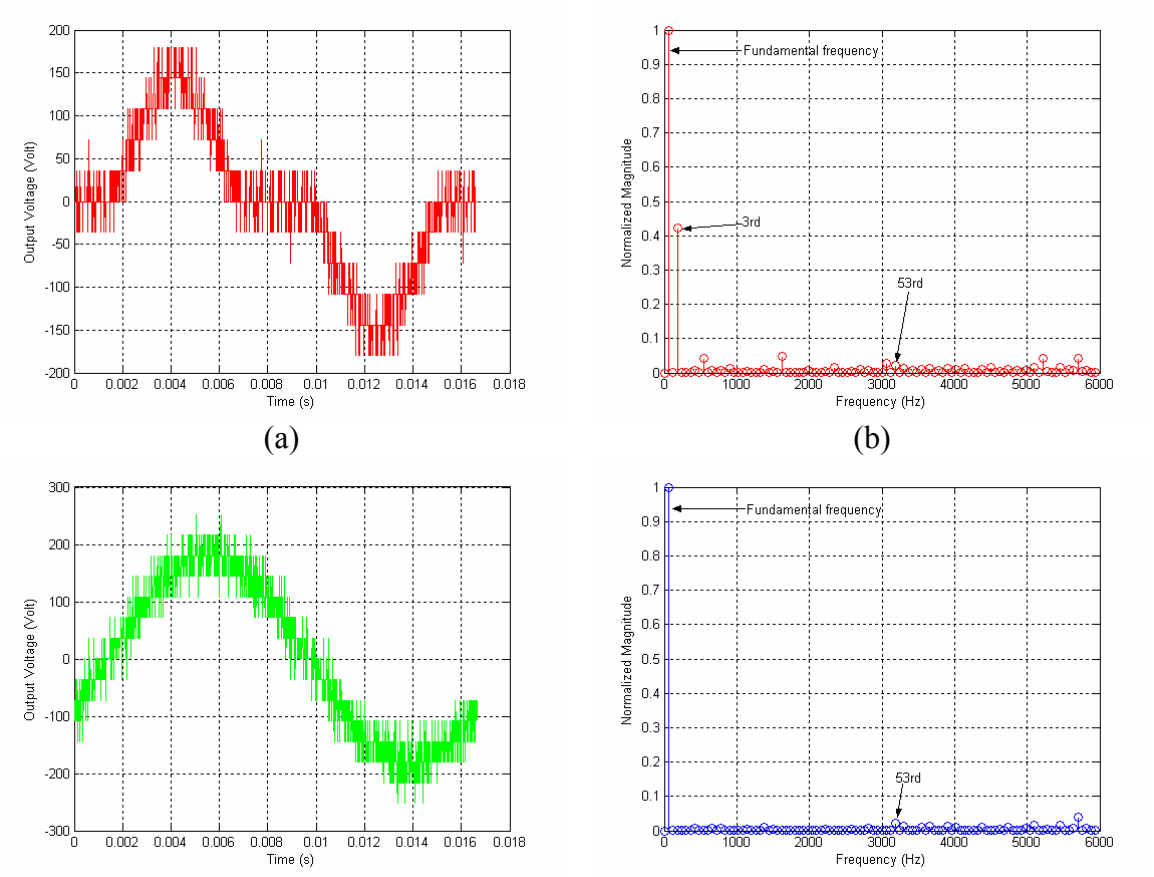


Figure 4.7: Harmonic elimination up to the 49th case simulation ($m = 2.28$) (a) phase voltage; (b) normalized FFT analysis of phase voltage; (c) line-line voltage; (d) normalized FFT analysis of line-line voltage

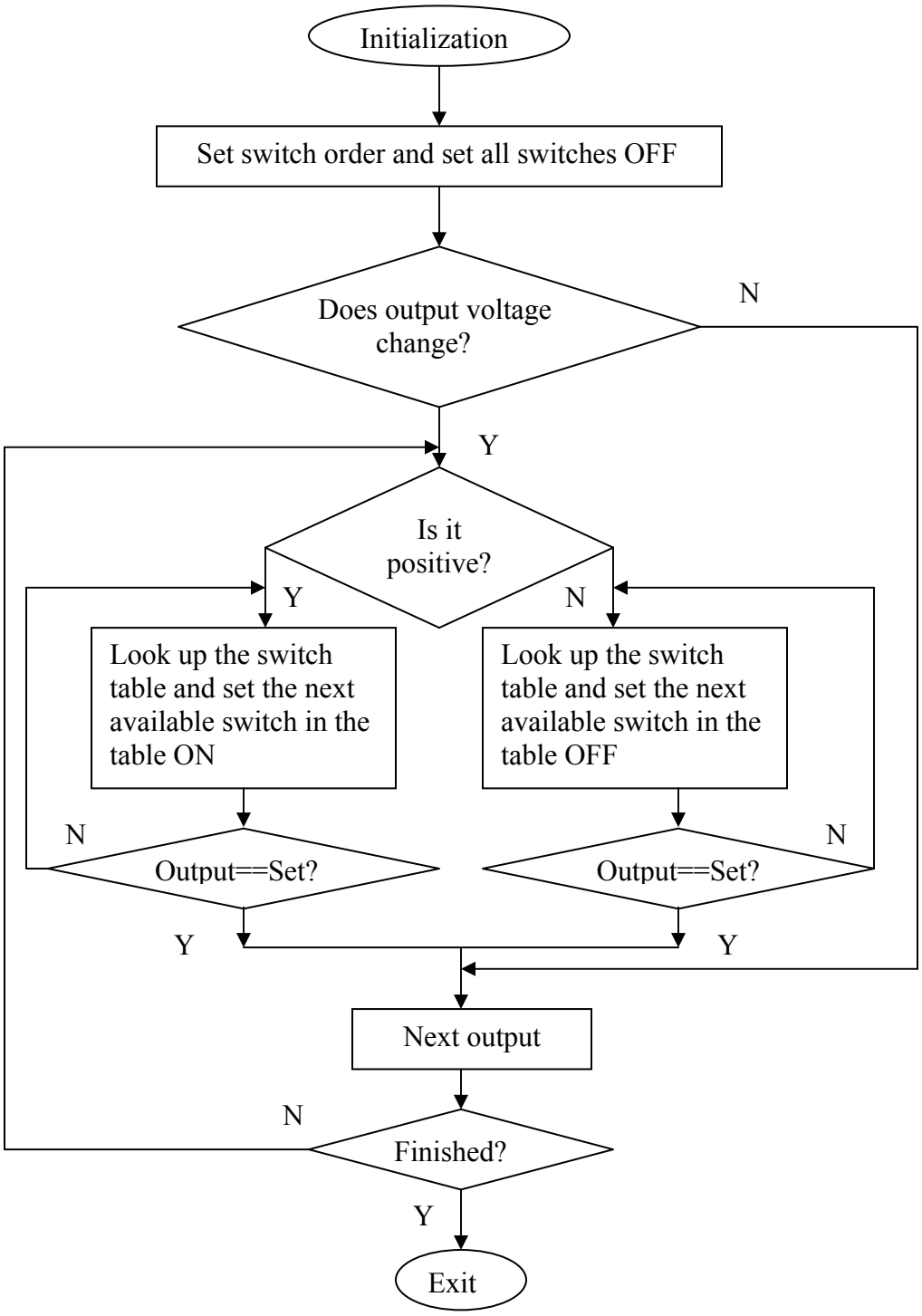


Figure 4.8: Control flow chart for first-on, first-off strategy

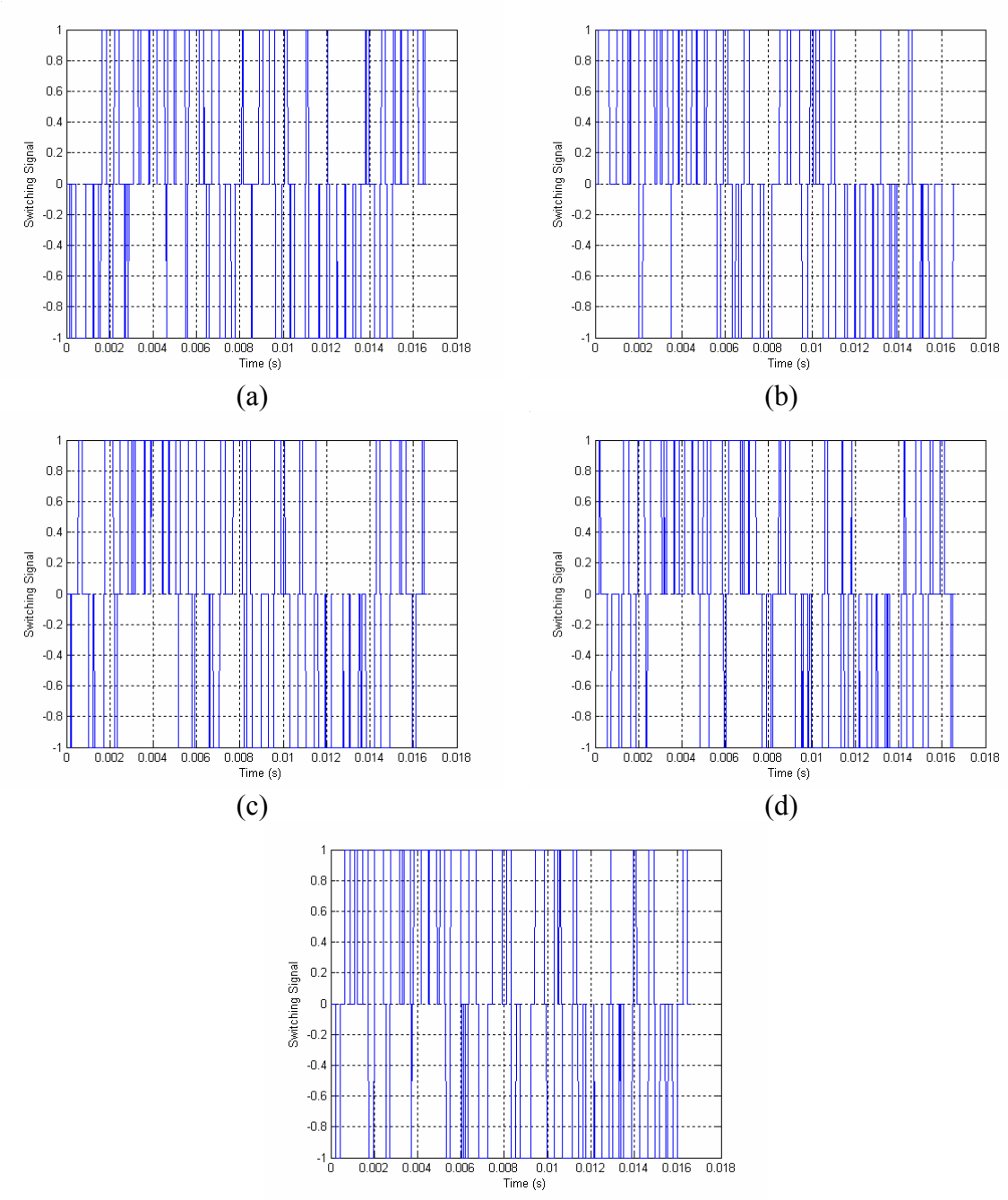


Figure 4.9: Switching signals based on first-on, first-off strategy (a) switching signal 1; (b) switching signal 2; (c) switching signal 3; (d) switching signal 4; (e) switching signal 5

4.3. Switching Number for the Control Strategy

In theory, to eliminate the n^{th} harmonic, the multilevel converter needs to switch n times in a cycle. So the switching number in a cycle for the active harmonic elimination method is $N_{sw} \le \sum_{n=17,19,23,\cdots} n$ where n is the harmonic number. However, if a harmonic amplitude is near zero, and the control resolution is lower than that required to eliminate the harmonic, then switching will not occur. Another situation is overlap. The first overlap case is one switching on time follows a switching off time immediately, then the switch will be on until next switching off occurs. The second overlap case is one switching off time follows a switching on time immediately, then the switch will be off until next switching on occurs. The overlap will decrease the switching times.

It is not easy to compute the second case except the switching signals will be used to count the switching times. But it is possible to compute the switching times for the first case. If the switching control resolution is set, the switching times can be computed by:

$$N_{sw} = \sum_{h_i \in \{17,19,23,\cdots\}} h_i \tag{4.17}$$

where h_i is the harmonic number that will be actively eliminated.

Figure 4.10 is the switching number computed by (4.17) in a cycle to satisfy the THD requirement of below 3% and the THD requirement of below 5%. It can be seen that the switching number for 3% THD requirement is higher than that of 5% THD requirement.

It can be derived from Figure 4.10 (c) that to decrease THD from 5% to 3%, more additional switchings are necessary except at a few modulation indices. From (d), the percentage of additional switchings is higher than 50%.

Instead of limiting the THD of the output voltage, the goal can be to eliminate a certain number of harmonics in the output voltage. For example, in the system, the harmonics lower than 31st will be eliminated, then the switching number for one cycle and its corresponding THD are shown in Figure 4.11. It can be seen that if one eliminates the harmonics up to the 31st, the THD will be below 5% except for a few low modulation indices.

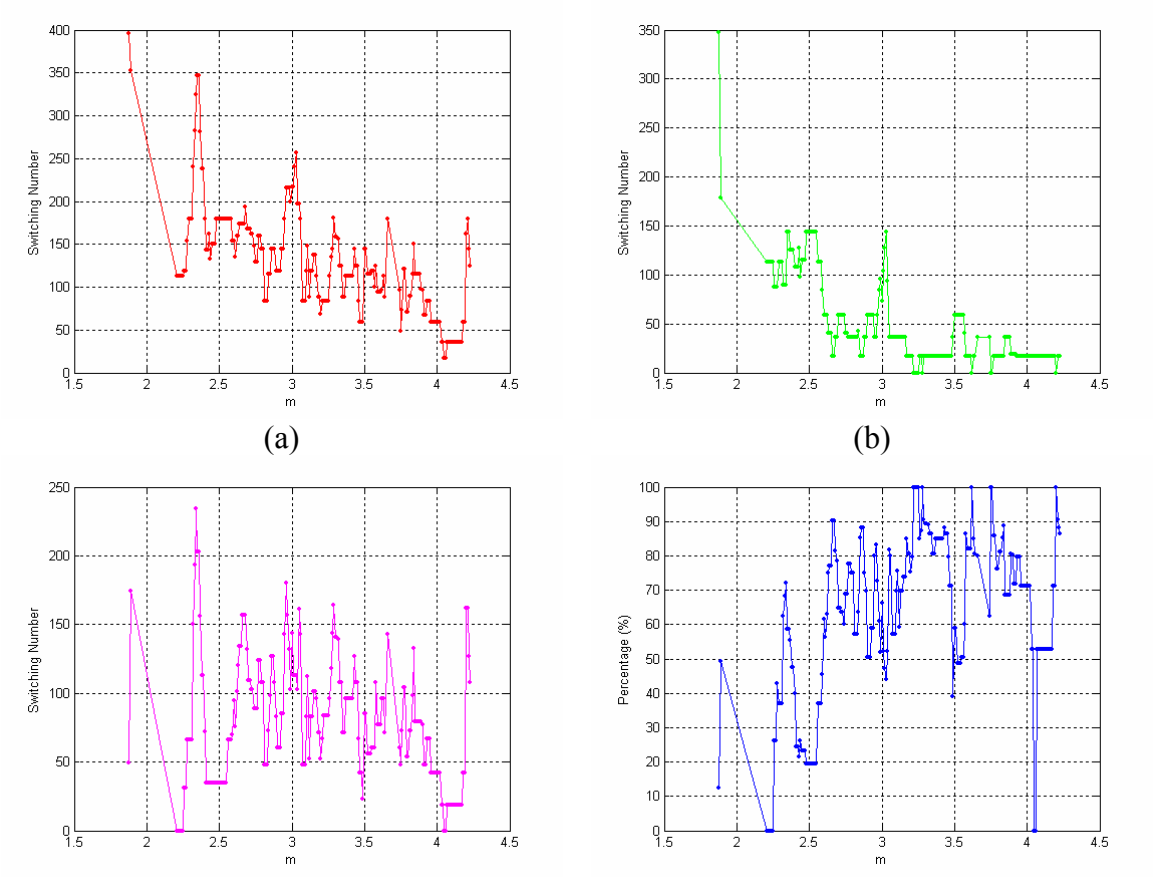
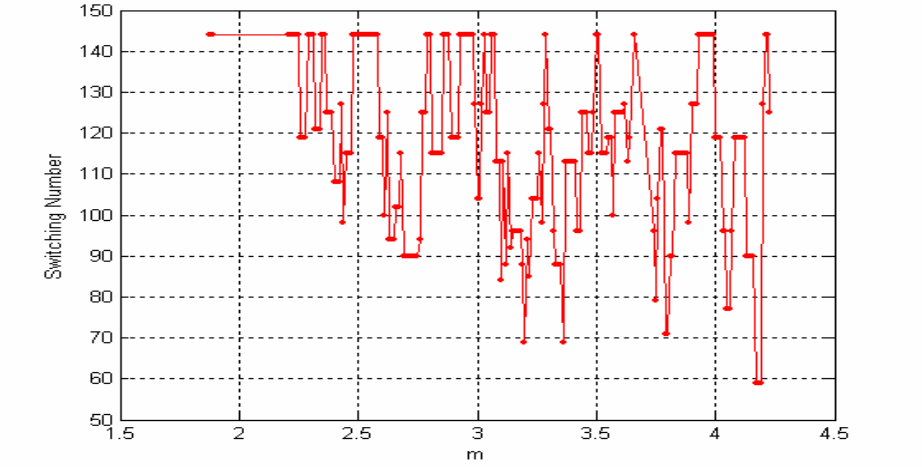
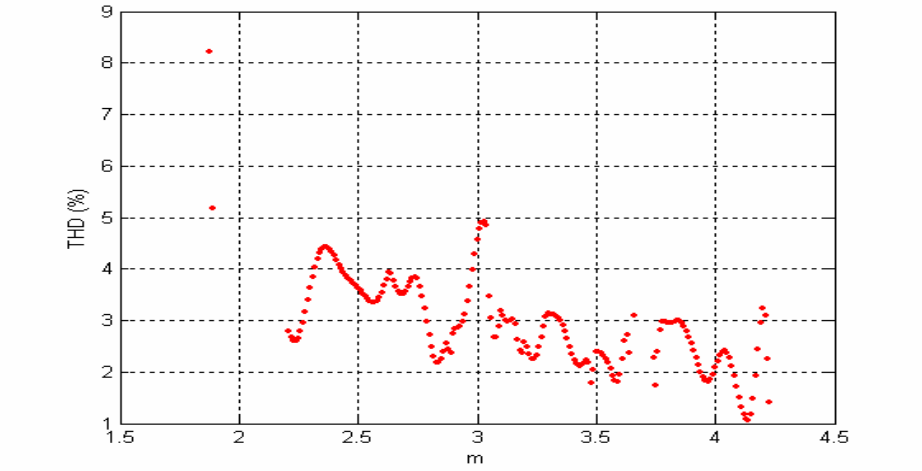


Figure 4.10: Minimum switching number in a cycle for different THD requirements (a) for 3% THD; (b) for 5% THD; (c) additional switching number for decreasing THD from 5% to 3%; (d) increased percentage of switching number for 2% THD decreasing



(a)



(b)

Figure 4.11: Switching number in a cycle to eliminate harmonics below the 31st and its corresponding THD (a) switching number; (b) THD

4.4. Experiment

To validate the proposed active harmonic elimination method, the simulation cases are implemented on an 11-level H-bridge multilevel converter.

Case 1: Harmonic elimination up to the 31st

From the FFT analysis in Figure 4.12 (c) and (d), it is clear that the harmonics up to the 31st have been eliminated. Although it can be seen that the 23rd and 25th harmonics are a little higher than 1%, this is because the control resolution is not infinitely small, and the switches are not ideal.

Case 2: Harmonic elimination up to the 49th

From the FFT analysis in Figures 4.13 (c), we can see the first non-zero harmonic is the 53rd harmonic. The harmonics up to the 49th have been eliminated. Some of the harmonics are a little higher than 1%, which is shown in (d). This is because the control resolution is not infinitely small and the switches are not ideal. They cannot be exactly zero.

Case 3: Harmonic elimination up to the 49th with a 10 μF capacitor filter

A further experiment to eliminate harmonics up to the 49th harmonic with a 10 μF capacitor paralleled at the output was implemented. The line-line voltage and its normalized FFT analysis are shown in Figure 4.14. It can be seen that the output voltage is very near a sinusoidal waveform. The THD is 2.26% when the harmonics are computed up to the 80th.

From the FFT analysis in Figure 4.14 (b), it is obvious that all the higher order harmonics are zero. The THD is from low order harmonics. This confirms the expectation that a small filter can filter out the higher order harmonics. So we do not worry about the higher order harmonics when we eliminate low order harmonics. A low THD voltage can be achieved easily.

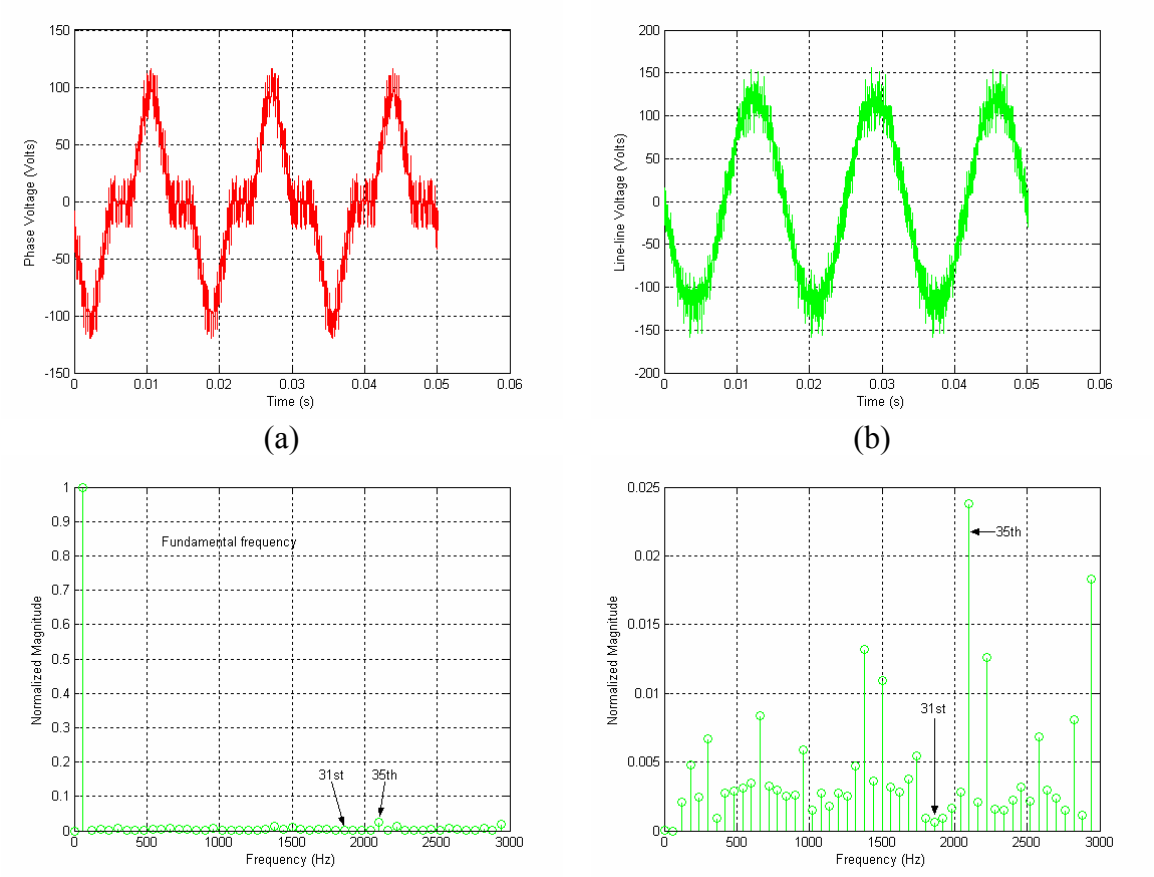


Figure 4.12: Experimental results for harmonic elimination up to the 31st (THD = 4.0%) (a) phase voltage; (b) line-line voltage; (c) normalized FFT analysis of line-line voltage; (d) normalized harmonic contents of line-line voltage with fundamental content removed

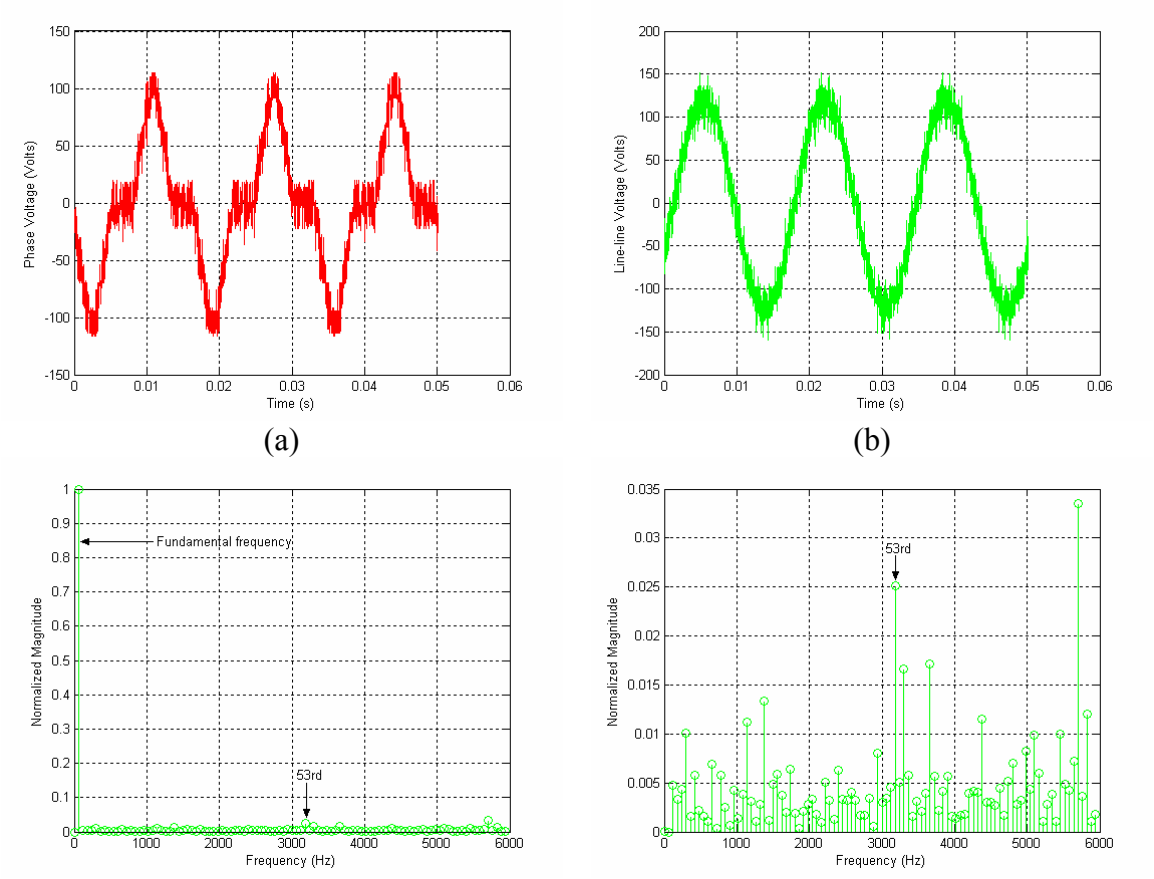
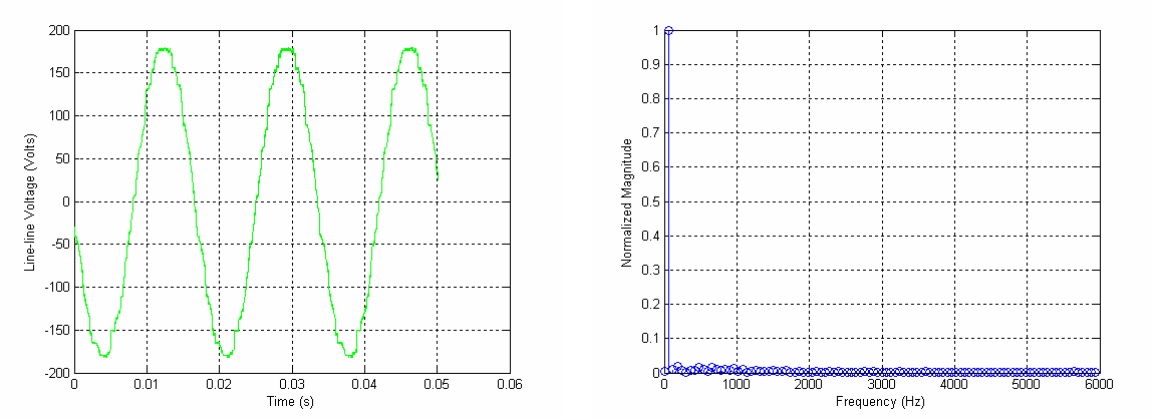


Figure 4.13: Experimental results for harmonic elimination up to the 49th (THD = 2.89%) (a) phase voltage; (b) line-line voltage; (c) normalized FFT analysis of line-line voltage; (d) normalized harmonic contents of line-line voltage with fundamental content removed



(a) (b)

Figure 4.14: Experimental results for harmonic elimination up to the 49th with a 10 μF capacitor filter (THD = 2.26%) (a) line-line voltage; (b) normalized FFT analysis of line-line voltage

4.5. Summary

In this chapter, the active harmonic method has been developed to eliminate any number of specified harmonics without the restriction of the number of unknowns in the harmonic equations.

To balance the switching loss during a whole cycle, the first-on, first-off strategy is employed to control the switching here. This strategy distributes the switching times between several levels, so each level can get an average switching time in a cycle. This strategy can also balance the load between several levels.

The simulation results and experimental results validated the active harmonic elimination method of elimination of additional harmonics.

The developed methods can only be used for multilevel converters with equal DC voltages, and cannot be applied to the multilevel converter with unequal DC voltages. The control method for multilevel converters with unequal DC voltages will be discussed in the next chapter.

5. Active Harmonic Elimination for Multilevel Converters with Unequal DC Voltages

In the previous chapter, the active harmonic elimination method for multilevel converter control with low modulation index has been developed.

Until now, most of the control methods developed for multilevel converters with equal DC voltages cannot be used for multilevel converters with unequal DC voltages. Space vector PWM, and space vector modulation methods cannot be applied to the multilevel converters with unequal DC voltages. The carrier phase shifting method for traditional PWM method also requires equal DC voltages. The existing control methods for multilevel converters with unequal DC voltages are more complicated than that for multilevel converters with equal DC voltages. For example, the resultant method can be applied to multilevel converters with fundamental switching frequency up to 6 equal DC sources, but it is very difficult to apply it to multilevel converters with 4 unequal DC sources [17].

This chapter extends the active harmonic elimination method for multilevel converters with equal DC voltages to multilevel converters with unequal DC voltages.

5.1. Resultant Method for Unipolar Switching Scheme Converters

Based on the harmonic elimination theory discussed in the previous chapters, the control method is to choose a series of switching angles to synthesize a desired sinusoidal voltage waveform. A typical five-angle unipolar switching output is shown in Figure 3.6, whose Fourier series expansion is

$$V(t) = \sum_{n=1,3,5\ldots}^{\infty} \frac{4V_{dc}}{n\pi}[\cos(n\theta_1) - \cos(n\theta_2) + \cos(n\theta_3) - \cos(n\theta_4) + \cos(n\theta_5)]\sin(n\omega t) \tag{5.1}$$

The control method is similar to the fundamental frequency switching control method. Given a desired fundamental voltage V_1, one wants to determine the switching

angles $\theta_1, \theta_2, \cdots, \theta_5$ so that $V(\omega t) = V_1 \sin(\omega t)$, and specific higher harmonics of $V_n(n\omega t)$ are equal to zero. For a three-phase application, the triplen harmonics in each phase need not be cancelled as they automatically cancel in the line-to-line voltages. In this example, the 5th, 7th, 11th, and 13th order harmonics can be cancelled. So the control needs to solve the following equations:

$$\begin{aligned}
&\cos(\theta_1) - \cos(\theta_2) + \cos(\theta_3) - \cos(\theta_4) + \cos(\theta_5) = m \\
&\cos(5\theta_1) - \cos(5\theta_2) + \cos(5\theta_3) - \cos(5\theta_4) + \cos(5\theta_5) = 0 \\
&\cos(7\theta_1) - \cos(7\theta_2) + \cos(7\theta_3) - \cos(7\theta_4) + \cos(7\theta_5) = 0 \\
&\cos(11\theta_1) - \cos(11\theta_2) + \cos(11\theta_3) - \cos(11\theta_4) + \cos(11\theta_5) = 0 \\
&\cos(13\theta_1) - \cos(13\theta_2) + \cos(13\theta_3) - \cos(13\theta_4) + \cos(13\theta_5) = 0
\end{aligned} \tag{5.2}$$

Here the resultant method is employed to find the solutions when they exist. The five-angle solutions are shown in Figure 3.7. The THD for the corresponding solution is also shown in Figure 3.7. Here the modulation index is defined as $m = \pi V_1 / (4V_{dc})$, and THD is defined as $THD = \dfrac{\sqrt{V_5^{\,2} + V_7^{\,2} + \cdots + V_{49}^{\,2}}}{V_1}$, as they are mentioned in Chapter 3.

From Figure 3.7, it can be seen that the solutions exist where the modulation index *m* is below 0.91. The THD is high for small *m* and low for large *m*. Unipolar converters generate not only the fundamental frequency voltage output, but also generate high order harmonics. Here, we call the normalized high order harmonic components $\pi V_n / (4V_{dc})$ vs *m* as the harmonic loci. The harmonic loci give us a sense for which harmonics dominate the THD in the output voltage. Figure 5.1 shows the harmonic loci for the odd non-triplen harmonics from the 17th to the 49th.

From the harmonic loci shown in Figure 5.1, it can be derived that the higher order harmonics vary with the modulation indices. The harmonics are positive for part of the modulation indices and negative for other parts of the modulation indices.

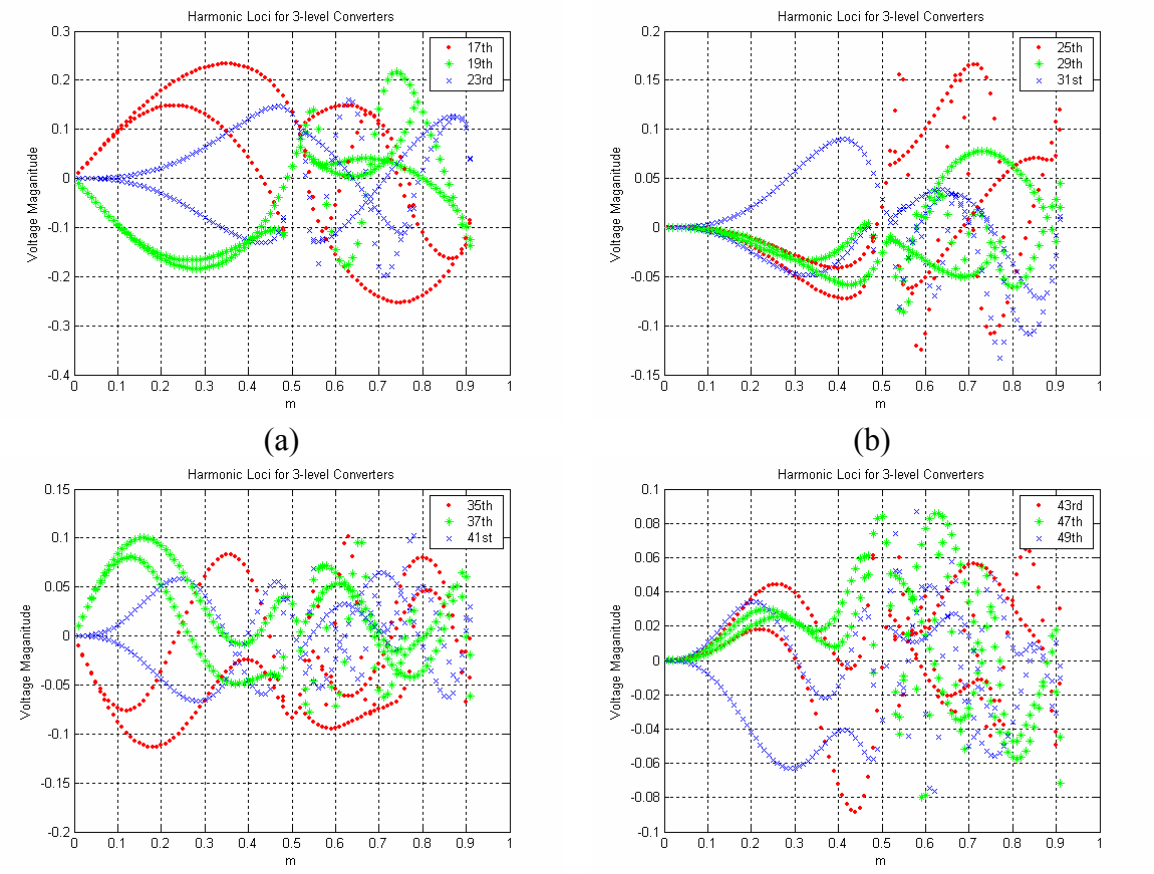


Figure 5.1: Harmonic loci for unipolar converter (a) 17th, 19th, 23rd harmonic loci; (b) 25th, 29th, 31st harmonic loci; (c) 35th, 37th, 41st harmonic loci; (d) 43rd, 47th, 49th harmonic loci

The property of the higher order harmonics shown in Figure 5.1 provides such a possibility to decouple the multilevel converter control into the control of several unipolar converters. The first unipolar converter generates a positive higher order harmonic, and the second unipolar converter generates a negative harmonic of the same frequency and the same phase, then the harmonics can cancel each other without additional switchings. If the harmonics cannot be cancelled completely, at least, the magnitude of the total harmonic will be decreased, and the THD of the output voltage will be low.

5.2. Optimal Combination Method for THD Control

Cascaded H-bridge multilevel converters could be viewed as several unipolar converters connected in series and can be controlled independently. The control method inherently cannot generate low order harmonics since each unipolar converter cannot generate low order harmonics under equal or unequal DC voltage cases.

Multilevel converters satisfy the following equations:

For each unipolar converter i:

$$\begin{aligned}
&\cos(\theta_{i1}) - \cos(\theta_{i2}) + \cos(\theta_{i3}) - \cos(\theta_{i4}) + \cos(\theta_{i5}) = m_i \\
&\cos(5\theta_{i1}) - \cos(5\theta_{i2}) + \cos(5\theta_{i3}) - \cos(5\theta_{i4}) + \cos(5\theta_{i5}) = 0 \\
&\cos(7\theta_{i1}) - \cos(7\theta_{i2}) + \cos(7\theta_{i3}) - \cos(7\theta_{i4}) + \cos(7\theta_{i5}) = 0 \\
&\cos(11\theta_{i1}) - \cos(11\theta_{i2}) + \cos(11\theta_{i3}) - \cos(11\theta_{i4}) + \cos(11\theta_{i5}) = 0 \\
&\cos(13\theta_{i1}) - \cos(13\theta_{i2}) + \cos(13\theta_{i3}) - \cos(13\theta_{i4}) + \cos(13\theta_{i5}) = 0
\end{aligned} \tag{5.3}$$

Therefore, the total modulation index $m = \sum_{i=1}^{s} c_i \frac{V_{dci}}{V_{dc}} m_i$, Here, V_{dc} is the nominal DC voltage, V_{dci} is the i^{th} DC voltage and $c_i (c_i \in \{-1,0,1\})$ is called a combination coefficient. For convenience, here define $k_i = \frac{V_{dci}}{V_{dc}}$, then $m = \sum_{i=1}^{s} c_i k_i m_i$.

As mentioned previously, the harmonic contents are positive for some modulation indices and are negative for other modulation indices. So it is possible to get a combination of several unipolar converters for each modulation index *m* of the multilevel converters with desired features, such as the lowest THD.

For different application requirements, we have different optimal goals. For example, here, we assume three cases:

Case 1: Minimum THD and eliminate the 5th, 7th, 11th and 13th harmonics.

The goal is to find a combination with $2s+1$ DC voltage levels with minimum THD:

$$THD = \frac{\sqrt{V_{17}{}^2 + V_{19}{}^2 + \cdots + V_{49}{}^2}}{V_1} \tag{5.4}$$

Case 2: Minimum THD and eliminate the 5th, 7th, 11th, 13th, 17th, 19th, 23rd and 25th harmonics.

The goal is to find a combination with $2s+1$ DC voltage levels with minimum THD:

$$THD = \frac{\sqrt{V_{29}{}^2 + V_{31}{}^2 + \cdots + V_{49}{}^2}}{V_1} \tag{5.5}$$

Case 3: Minimum THD and eliminate the 5-37th harmonics.

The goal is to find a combination with $2s+1$ DC voltage levels with minimum THD:

$$THD = \frac{\sqrt{V_{41}{}^2 + V_{43}{}^2 + \cdots + V_{49}{}^2}}{V_1} \tag{5.6}$$

1. Minimum THD search with equal DC voltage levels

In the Minimum THD search, with $s = 4$ and equal DC voltage level conditions, the minimum THD with optimal combination are shown in Figure 5.2.

From the computation results, it can be seen that the combinations for middle range *m* can achieve low THD. The number of combinations for the high range *m* is very few. Therefore the THD for high *m* is high.

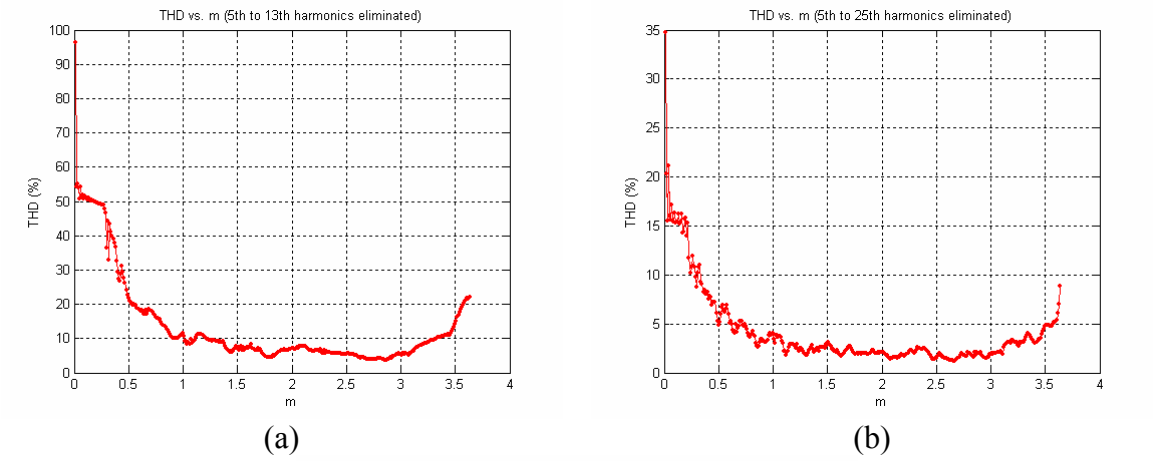


Figure 5.2: Minimum THD for equal DC voltages (a) harmonic elimination to the 13th; (b) harmonic elimination to the 25th; (c) harmonic elimination to the 37th

Here, Figure 5.2 is for 9-level multilevel converter control with equal DC voltages. It is of interest to compare the control performance with 9-level multilevel converter control by fundamental frequency switching method in Figure 3.3. A major difference between Figure 3.3 and Figure 5.2 is the modulation index range. The modulation index in Figure 5.2 is continuous, but it is discontinuous in Figure 3.3. A practical application generally needs a continuous modulation index range. For this reason, the control method proposed here is better than the fundamental frequency switching method.

2. Minimum THD search with unequal DC voltage levels

In the Minimum THD search, under $s = 4$ and unequal DC voltage level conditions, the THD with optimal combination are shown in Figure 5.3. In situation 1, $k_1 = 1.1617$, $k_2 = 1.0278$, $k_3 = 0.9722$, $k_4 = 0.9444$; in situation 2, $k_1 = 1.0556$, $k_2 = 1.0278$, $k_3 = 1$, $k_4 = 0.9444$.

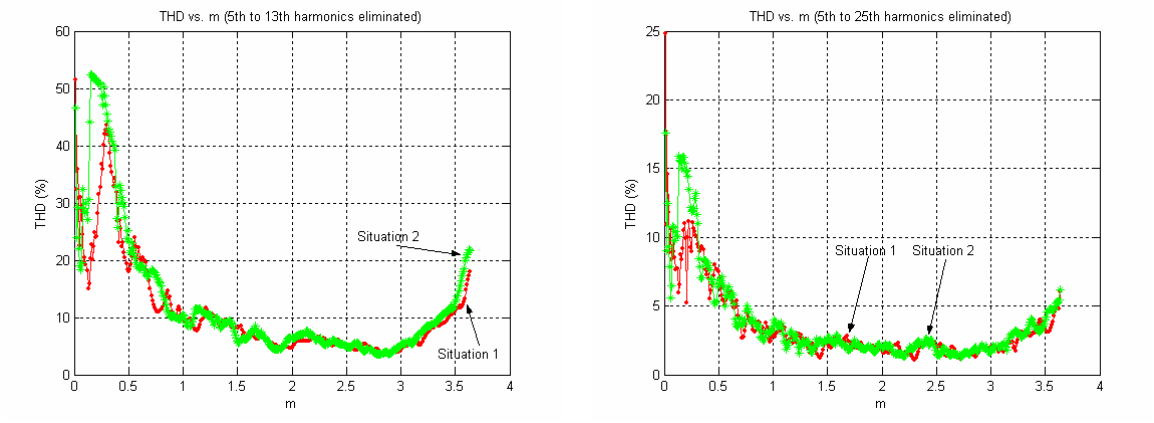
5.3. Active Harmonic Elimination Method

From the computational results, it can be seen that if just the 5th, 7th, 11th and 13th harmonics are eliminated, the THD is higher than 5%. To decrease the THD of the output voltage, the active harmonic elimination method can be used to eliminate higher order harmonics.

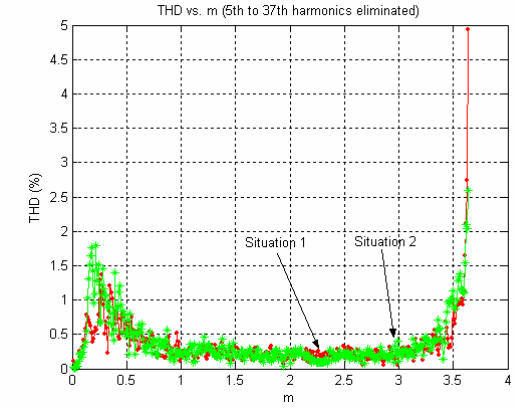
Similar to the fundamental frequency switching control method mentioned in chapter 4, from (4.1), the voltage contents can be divided into four parts:

1. Fundamental frequency voltage:

$$V_{p1}(t) = \sum_{i}^{s} \frac{4c_i k_i V_{dc}}{\pi} [\cos(\theta_{i1}) - \cos(\theta_{i2}) + \cos(\theta_{i3}) - \cos(\theta_{i4}) + \cos(\theta_{i5})] \sin(\omega t) \tag{5.7}$$



(a) (b)



(c)

Figure 5.3: Minimum THD for unequal DC voltages (a) harmonic elimination to the 13th; (b) harmonic elimination to the 25th; (c) harmonic elimination to the 37th

2. Triplen harmonic voltages:

$$V_{p2}(t) = \sum_{i}^{s} \sum_{n=3,9,15,\cdots} \frac{4c_i k_i V_{dc}}{n\pi}[\cos(n\theta_{i1}) - \cos(n\theta_{i2}) + \cos(n\theta_{i3}) - \cos(n\theta_{i4}) + \cos(n\theta_{i5})]\sin(n\omega t) \quad (5.8)$$

3. Low order harmonic voltages that can be eliminated by applying resultant method.

$$V_{p3}(t) = \sum_{i}^{s} \sum_{n=5,7,11,13} \frac{4c_i k_i V_{dc}}{n\pi}[\cos(n\theta_{i1}) - \cos(n\theta_{i2}) + \cos(n\theta_{i3}) - \cos(n\theta_{i4}) + \cos(n\theta_{i5})]\sin(n\omega t) \quad (5.9)$$

4. High order harmonic voltages that cannot be eliminated by applying resultant method.

$$V_{p4}(t) = \sum_{i}^{s} \sum_{n=17,19,23,\cdots} \frac{4c_i k_i V_{dc}}{n\pi}[\cos(n\theta_{i1}) - \cos(n\theta_{i2}) + \cos(n\theta_{i3}) - \cos(n\theta_{i4}) + \cos(n\theta_{i5})]\sin(n\omega t) \quad (5.10)$$

Assuming the application is a balanced three-phase system, the triplen harmonics (5.8) need not be eliminated. This then leaves V_{p4}. To eliminate these harmonics, the active harmonic elimination method developed in chapter 4 is used. A square wave is generated (one for each of these harmonics) whose fundamental is equal to the negative of the residual harmonic that is to be eliminated. For example, to eliminate the 17th harmonic, a square wave whose Fourier series expansion is

$$V(t) = -\sum_{i}^{s} \sum_{n=1,3,5\cdots} \frac{4c_i k_i V_{dc}}{n\pi}[\cos(nh\theta_{i1}) - \cos(nh\theta_{i2}) + \cos(nh\theta_{i3}) - \cos(nh\theta_{i4}) + \cos(nh\theta_{i5})]\sin(nh\omega t) \quad (5.11)$$

is generated, where $h = 17$. As mentioned in chapter 4, the $n = 1$ term of (5.11) cancels the $n = 17$ term of (5.10) and the next harmonic of concern that is produced by (5.11) is at 5×17 = 85. This harmonic and higher ones (7×17, etc.) are easy to filter using a low-pass filter. Repeating the above procedure to the multilevel converter, the 19th, 23rd …

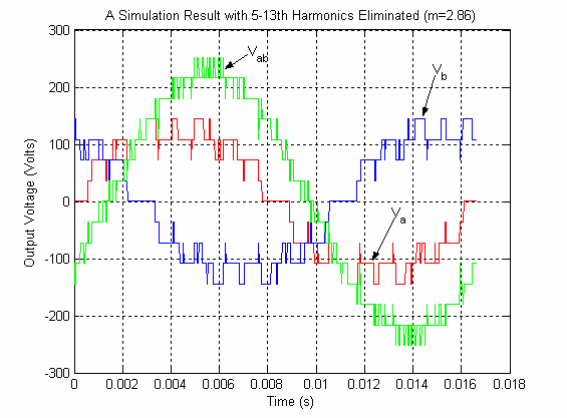
harmonics can all be eliminated. The net effect of this method is to remove the low order harmonics and to generate new higher order harmonics by increasing the switching frequency. By using the active harmonic elimination method, the $THD = \frac{\sqrt{V_5^{\,2} + V_7^{\,2} + \cdots + V_{49}^{\,2}}}{V_1}$ of the output voltage for different optimal combination versus m is shown in Figure 5.2 for equal DC voltages. For unequal DC voltages, the results are shown in Figure 5.3. The additional switching number in a cycle for the active harmonic elimination method is $N_{sw} \le \sum_{n=17,19,23,\cdots} n$, which is mentioned in chapter 4. For example, if the harmonics are eliminated through the 25th, the upper limit switching number is 84; if the harmonics are eliminated through the 37th, the upper limit switching number is 216. This has been discussed in chapter 4.

5.4. Simulation Study

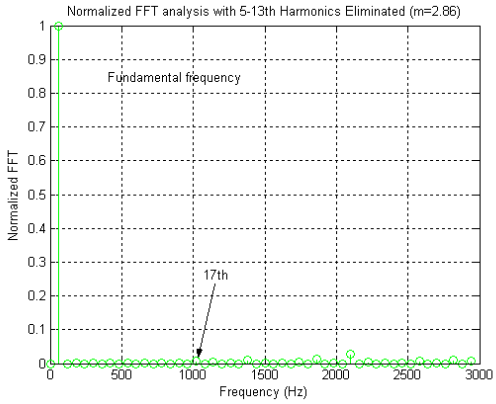
To verify the control method, an equal DC voltage case and an unequal DC voltage case simulation studies have been implemented. The simulation includes an output voltage waveform and its FFT analysis.

1. Equal DC voltage case ($m = 2.86$***).***

A phase voltage and line-line voltage simulation with the 5th, 7th, 11th and 13th harmonics eliminated is shown in Figure 5.4; its corresponding normalized FFT analysis of the line-line voltage is also shown in Figure 5.4. A phase voltage and line-line voltage simulation with the 5th to 25th harmonics eliminated is shown in Figure 5.5 with its corresponding normalized FFT analysis of the line-line voltage. A phase voltage and line-line voltage simulation with the 5th to 37th harmonics eliminated is shown in Figure 5.6 as well as a normalized FFT analysis of the line-line voltage.

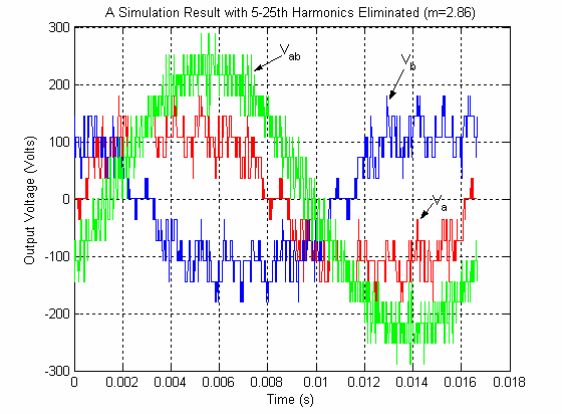


(a)

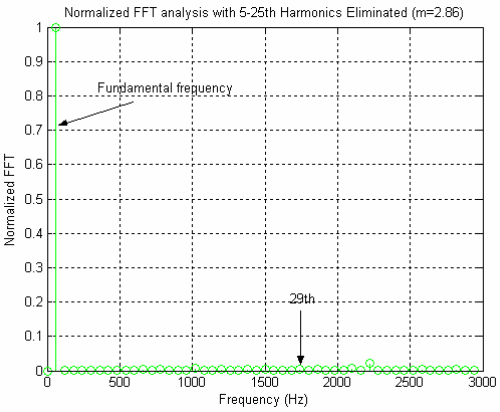


(b)

Figure 5.4: Simulation with the 5th to 13th harmonics eliminated (THD = 3.70%) (a) phase voltage and line-line voltage; (b) normalized FFT analysis of line-line voltage

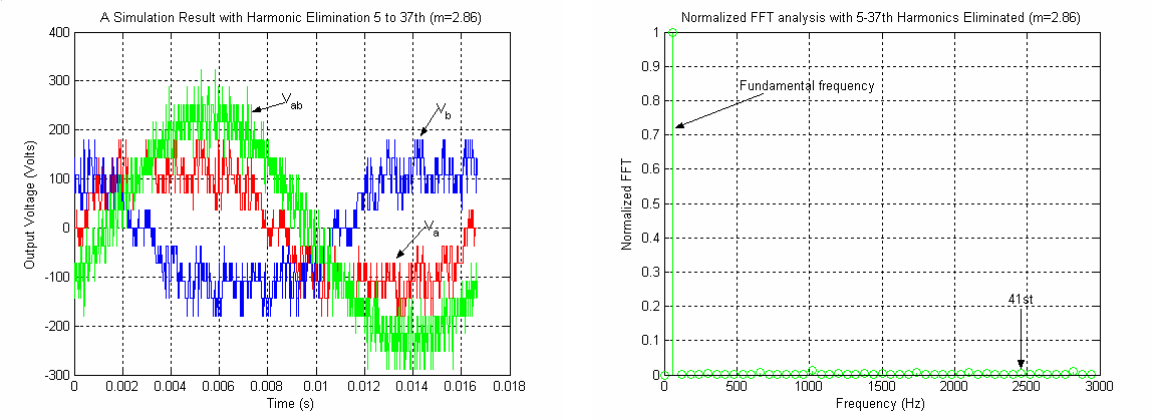


(a)



(b)

Figure 5.5: Simulation with the 5th to 25th harmonics eliminated (THD = 3.55%) (a) phase voltage and line-line voltage; (b) normalized FFT analysis of line-line voltage



(a) (b)

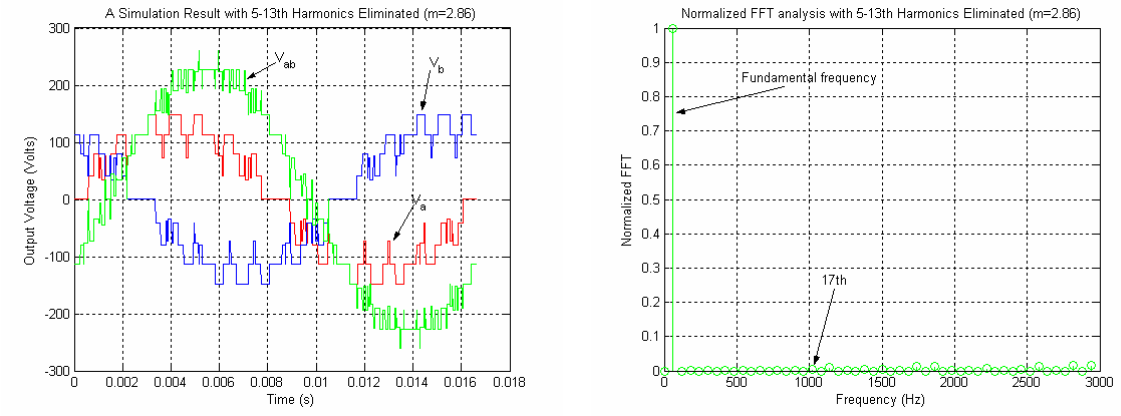
Figure 5.6: Simulation with the 5th to 37th harmonics eliminated (THD = 2.36%) (a) phase voltage and line-line voltage; (b) normalized FFT analysis of line-line voltage

From the simulation results, it can be seen that the unipolar converter control method can effectively eliminate the harmonics the 5-13th for equal DC voltages; the active harmonic elimination method can eliminate additional harmonics by adding more switchings. The corresponding THD computed through the 49th in theory for the above three cases are 3.72%, 1.83%, and 0.14%. The THD for the three simulation cases are 3.70%, 3.55%, and 2.36%, respectively. From the simulation, it can be seen that the THD of the simulation output voltage with the 5-13th harmonics eliminated is the same as in theory; the THD of the simulation output voltage with the 5-25th harmonics eliminated is a little higher than that of in theory; and the THD of the simulation output voltage with 5-37th harmonics eliminated is much higher than that of in theory. The reason is because the simulation step size is not infinitely small, and when the THD is small for a case, this makes a significant contribution to the THD error.

(2). Unequal DC voltage situation ***(*** $k_1 = 1.1617$, $k_2 = 1.0278$, $k_3 = 0.9722$, $k_4 = 0.9444$, $V_{dc} = 36\,V$, $m = 2.86$***).***

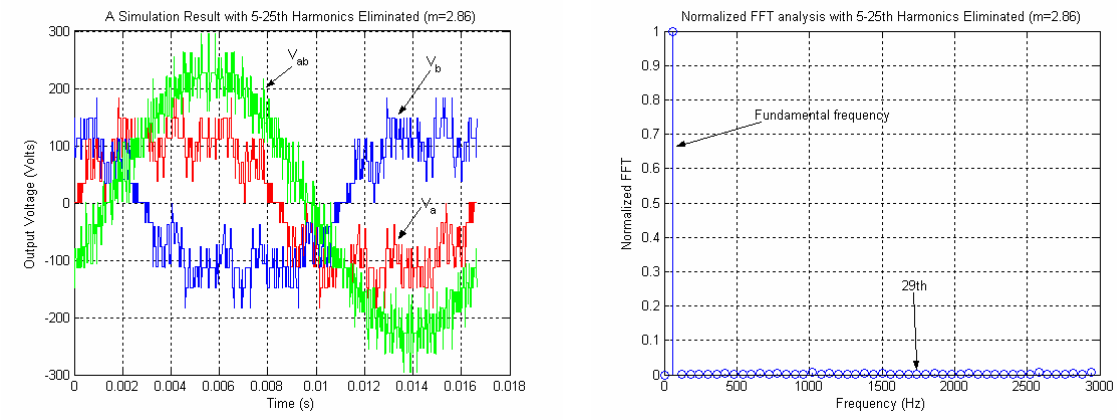
A phase voltage and line-line voltage simulation with 5th, 7th, 11th and 13th harmonics eliminated is shown in Figure 5.7. Its corresponding normalized FFT analysis of the line-line voltage is also shown in Figure 5.7. A phase voltage and line-line voltage simulation with 5th to 25th harmonics eliminated is shown in Figure 5.8 with its corresponding normalized FFT analysis of the line-line voltage. A phase voltage and the line-line voltage simulation with the 5th to 37th harmonics eliminated is shown in Figure 5.9 along with a normalized FFT analysis of the line-line voltage.

From the simulation results, It can be seen that the unipolar converter control method can effectively eliminate the 5-13th harmonics for multilevel converter with unequal DC voltages; the active harmonic elimination method can also eliminate additional harmonics by adding more switchings for multilevel converters with unequal DC voltages. The corresponding THD in theory for the above three cases are 3.65%, 1.31%, and 0.05%. The THD for the three simulation cases are 3.59%, 1.79%, and 1.65% respectively.



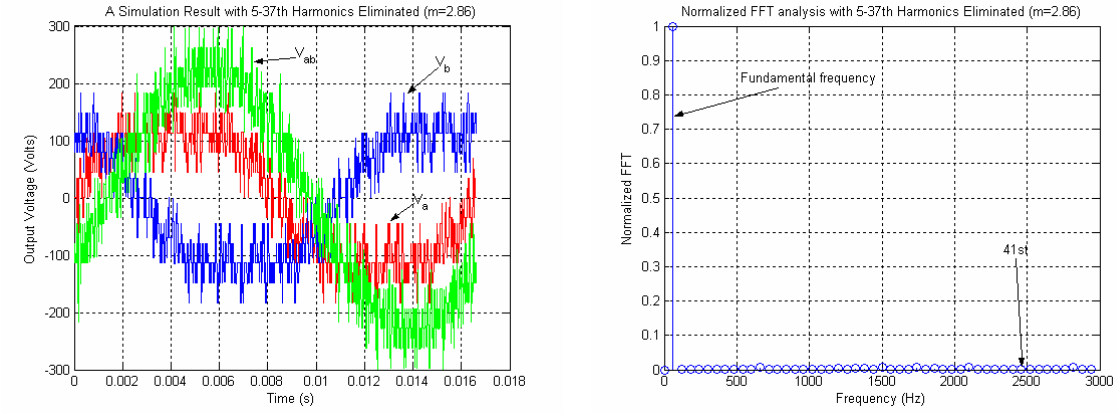
(a) (b)

Figure 5.7: Simulation with the 5th to 13th harmonics eliminated with unequal DC voltages (THD = 3.59%) (a) phase voltage and line-line voltage; (b) normalized FFT analysis of line-line voltage



(a) (b)

Figure 5.8: Simulation with the 5th to 25th harmonics eliminated with unequal DC voltages (THD = 1.79%) (a) phase voltage and line-line voltage; (b) normalized FFT analysis of line-line voltage



(a) (b)

Figure 5.9: Simulation with the 5th to 37th harmonics eliminated with unequal DC voltages (THD = 1.65%) (a) phase voltage and line-line voltage; (b) normalized FFT analysis of line-line voltage

From the simulation, we can see that the THD of the simulation output voltage with 5-13th harmonics eliminated is the same as in theory; the THD of the simulation output voltage with 5-25th harmonics eliminated is a little higher than that of in theory; and the THD of the simulation output voltage with the 5-37th harmonics eliminated is much higher than that of in theory. Again, the reason is because the simulation step size is not infinitely small, and when the THD is small for a case, this makes a significant contribution to the THD error.

5.5. Switching Control Strategy

For the equal DC voltage situation, the first-on, first-off strategy can be used to control the switching. The method can balance the switching loss during a whole cycle. This strategy also distributes the switchings between several DC levels, so each DC source can get an average switching time in a cycle, and balance the load between several DC levels.

For unequal DC voltage situation, the switchings for one DC voltage level cannot be switched by the other DC voltage levels. Therefore, first-on, first-off strategy cannot be used to control the multilevel converters. As mentioned above, to eliminate a harmonic, a negative harmonic must be generated by the multilevel converter. Because a specific voltage level is used to generate the negative harmonic, other voltage levels cannot be used to generate the harmonic because they have different voltage levels. One problem occurs if a voltage level cannot generate the negative harmonic based on its unipolar voltage waveform. To conquer the problem, the pulse-based switching control strategy is proposed here. A harmonic voltage is split into a series of pulses. If a voltage level cannot generate the necessary pulse, another voltage level is used to generate this pulse based on the following equation:

$$V_{dc1}\cos(\theta_1) = V_{dc2}\cos(\theta_2) \tag{5.12}$$

where θ_1 and θ_2 are the harmonic switching angles under voltage V_{dc1} and $V_{dc2.}$ Under this condition, two pulses are guaranteed to have same fundamental frequency contents. Repeat this process until all the necessary harmonic pulses have been generated. Then the output voltage will not contain the specified harmonics.

The switching control flow chart is shown in Figure 5.10.

5.6. Experiment

To validate the proposed active harmonic elimination method for multilevel converters with unequal DC voltages, the simulation cases are implemented on an 11-level H-bridge multilevel converter.

1. ***Equal DC voltage case (m = 2.86, V_{dc} = 36 V)***

Case 1: 5-13th harmonics eliminated.

From the FFT analysis in Figures 5.11(c) and (d), it is clear that the harmonics up to the 13th have been eliminated.

Case 2: 5-25th harmonics eliminated.

From the FFT analysis in Figures 5.12(c) and (d), it is clear that the harmonics up to the 25th have been eliminated.

Case 3: 5-37th harmonics eliminated.

From the FFT analysis in Figure 5.13(c), it is clear that the harmonics up to the 37th have been eliminated. Although it can be seen from Figure 5.13(d) that the 11th, 19th, and 29th harmonics are a little higher than 1%, this is because the control resolution is not infinitely small, and the switches are not ideal.

2. ***Unequal DC voltage case (m = 2.86, V_{dc1} = 42 V, V_{dc2} = 37 V, V_{dc3} = 35 V, and V_{dc4} = 34 V).***

Case 1: 5-13th harmonics eliminated.

From the FFT analysis in Figure 5.14, it is clear that the harmonics up to 13th have been eliminated.

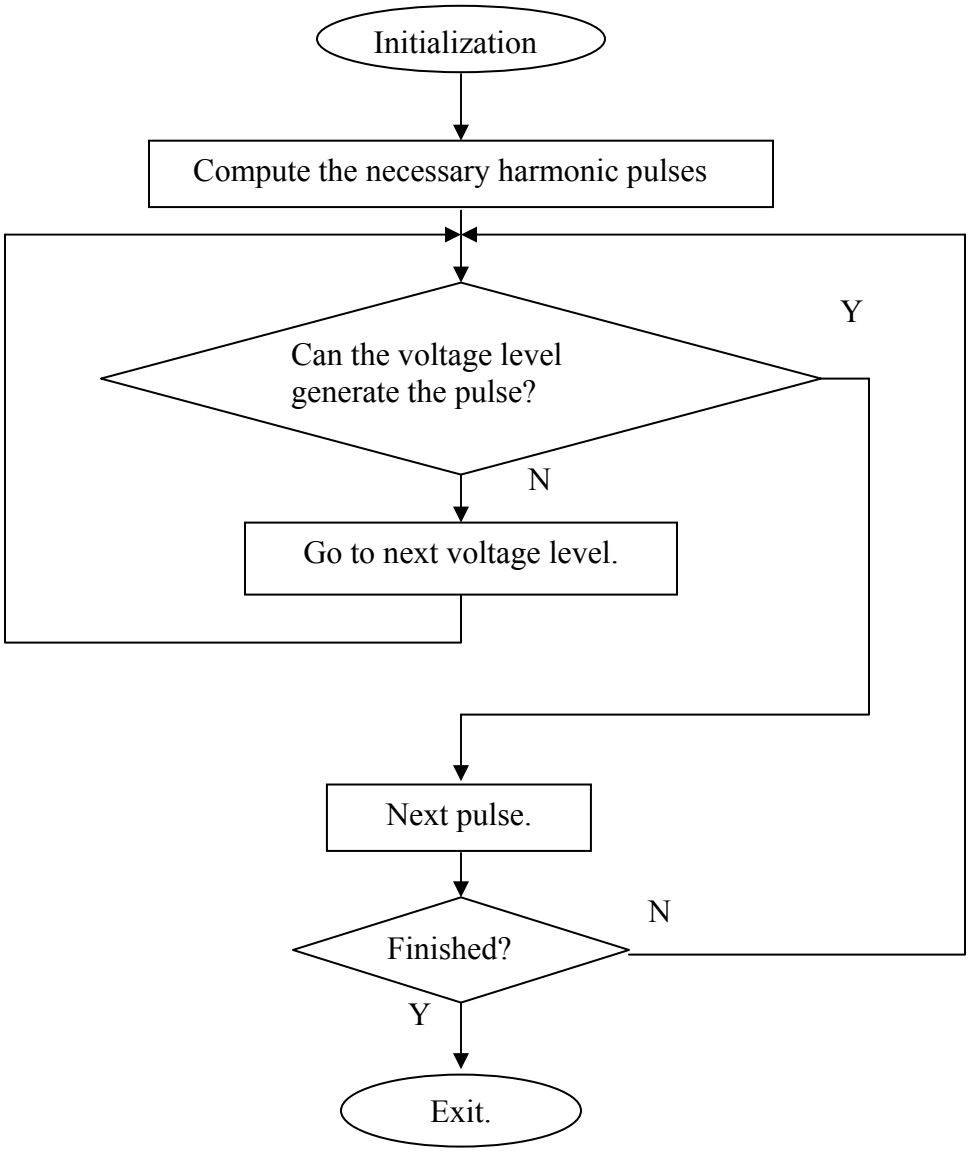


Figure 5.10: Switching control flow chart for multilevel converters with unequal DC voltage cases

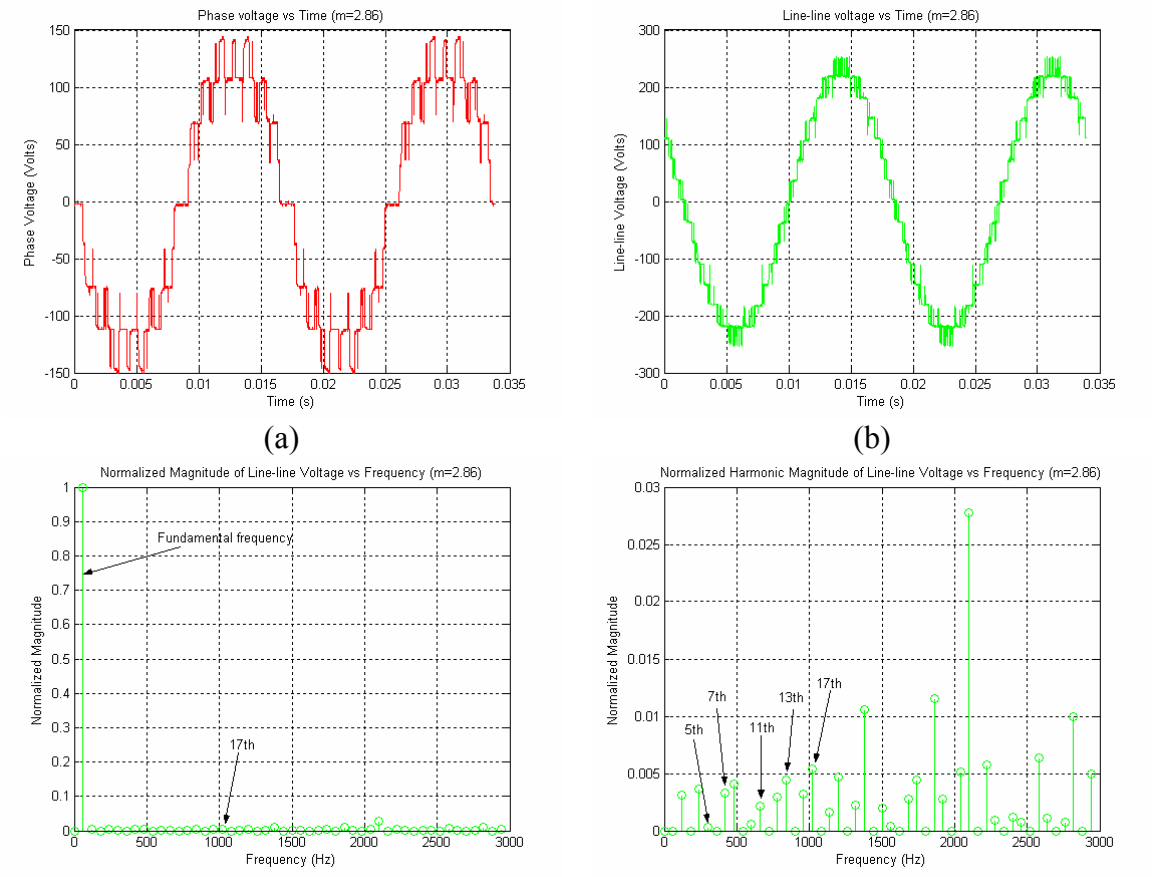


Figure 5.11: Experiment with the 5th to 13th harmonics eliminated with equal DC voltages (THD = 3.60%) (a) phase voltage; (b) line-line voltage; (c) normalized FFT analysis of line-line voltage; (d) normalized harmonic contents of line-line voltage with fundamental content removed

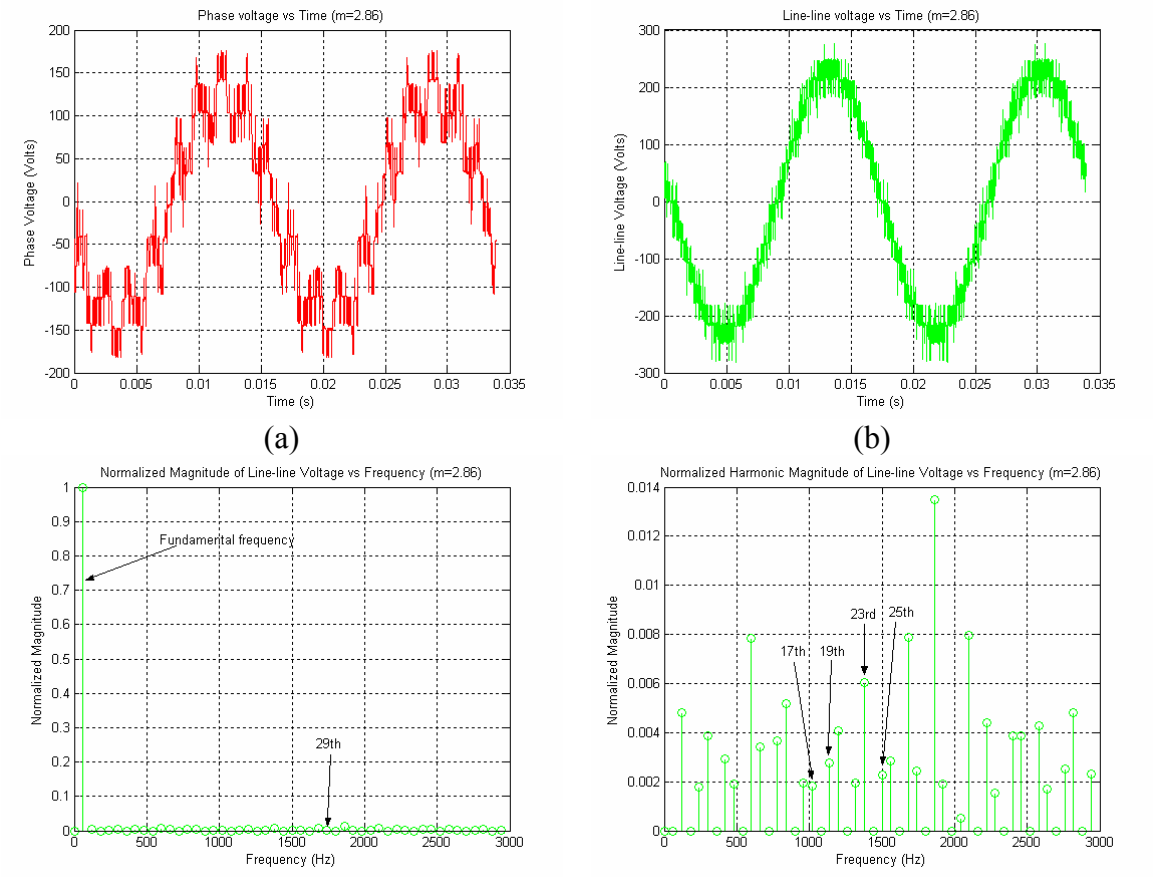


Figure 5.12: Experiment with the 5th to 25th harmonics eliminated with equal DC voltages (THD = 2.08%) (a) phase voltage; (b) line-line voltage; (c) normalized FFT analysis of line-line voltage; (d) normalized harmonic contents of line-line voltage with fundamental content removed

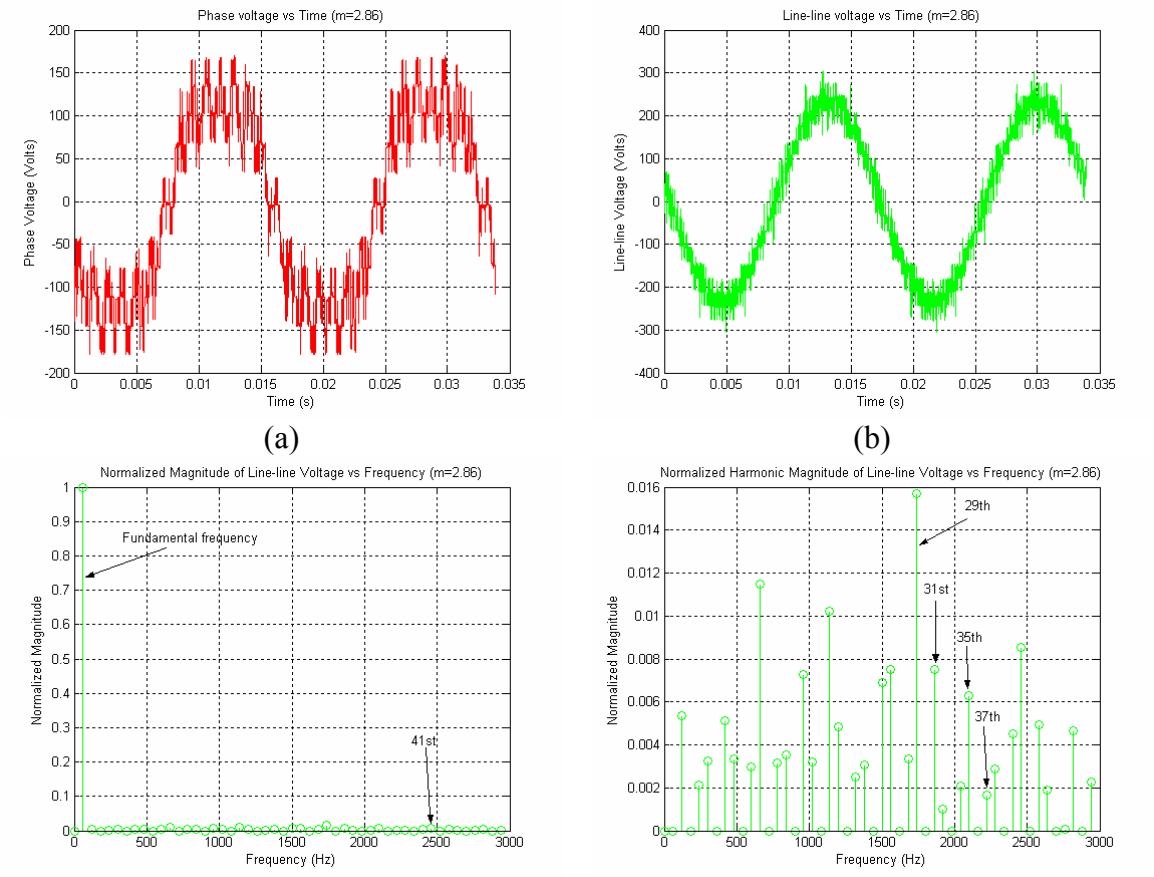


Figure 5.13: Experiment with the 5th to 37th harmonics eliminated with equal DC voltages (THD = 2.86%) (a) phase voltage; (b) line-line voltage; (c) normalized FFT analysis of line-line voltage; (d) normalized harmonic contents of line-line voltage with fundamental content removed

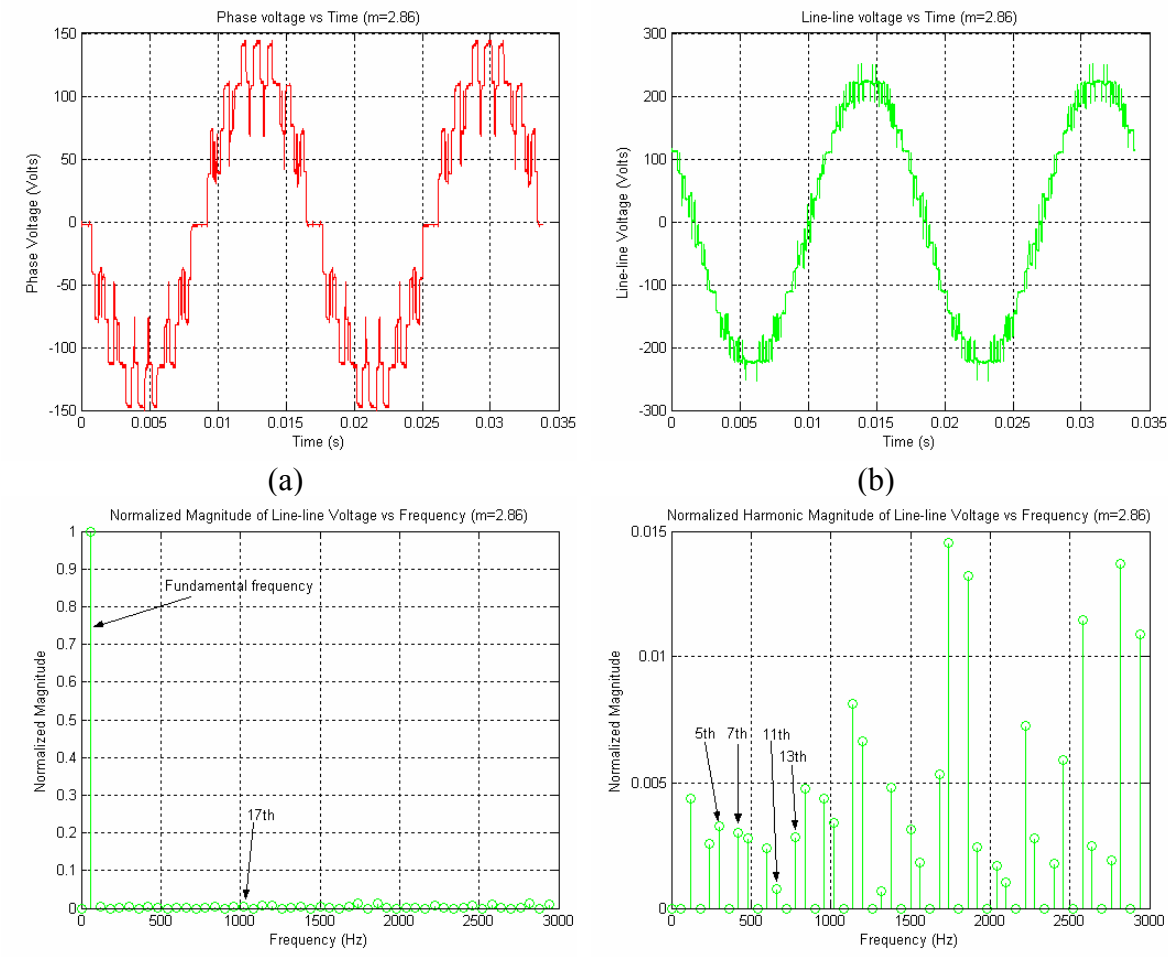


Figure 5.14: Experiment with the 5th to 13th harmonics eliminated with unequal DC voltages (THD = 3.24%) (a) phase voltage; (b) line-line voltage; (c) normalized FFT analysis of line-line voltage; (d) normalized harmonic contents of line-line voltage with fundamental content removed

Case 2: 5-25th harmonics eliminated.

From the FFT analysis in Figure 5.15(c), it is clear that the harmonics up to the 25th have been eliminated. Although it can be seen from Figure 5.15(d) that the 17th and 21st harmonics are a little higher than 1%, this is because the control resolution is not infinitely small, and the switches are not ideal.

Case 3: 5-37th harmonics eliminated.

From the FFT analysis Figure 5.16(c), it is clear that the harmonics up to the 37th have been eliminated. Although it can be seen from Figure 5.16(d) that the 35th harmonics are a little higher than 1%, this is because the control resolution is not infinitely small, and the switches are not ideal.

For convenience, the THD for all the situations are summarized in Table 5.1.

Table 5.1. $THD = \dfrac{\sqrt{V_5^{\,2} + V_7^{\,2} + \cdots + V_{49}^{\,2}}}{V_1} \times 100\%$ ($m = 2.86$) under different conditions

	Equal DC voltages			Unequal DC voltages		
	Theoretical	Simulation	Experiment	Theoretical	Simulation	Experiment
Case 1: 5-13th	3.72	3.70	3.60	3.65	3.59	3.24
Case 2: 5-25th	1.83	3.55	2.08	1.31	1.79	2.28
Case 3: 5-37th	0.14	2.36	2.86	0.05	1.65	3.59

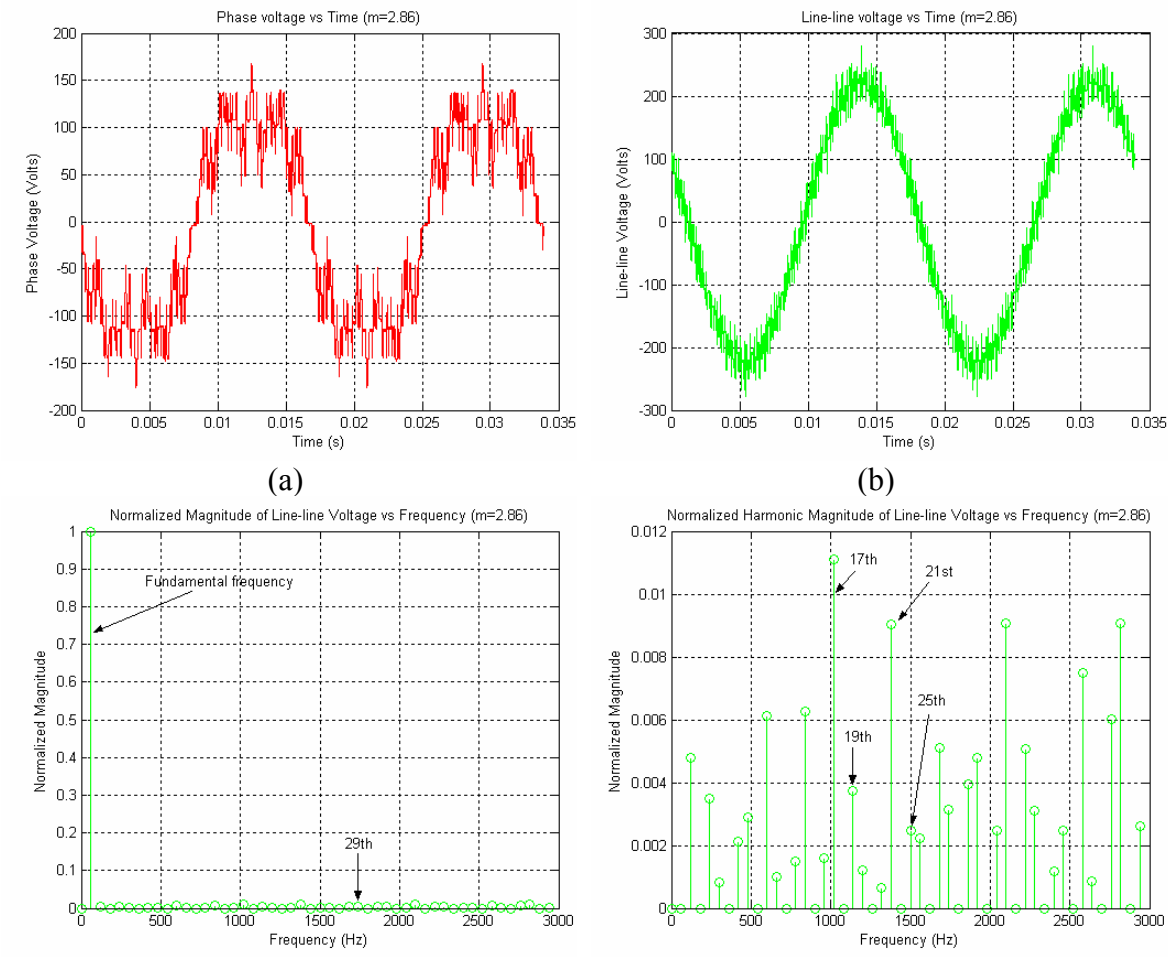


Figure 5.15: Experiment with the 5th to 25th harmonics eliminated with unequal DC voltages (THD = 2.28%) (a) phase voltage; (b) line-line voltage; (c) normalized FFT analysis of line-line voltage; (d) normalized harmonic contents of line-line voltage with fundamental content removed

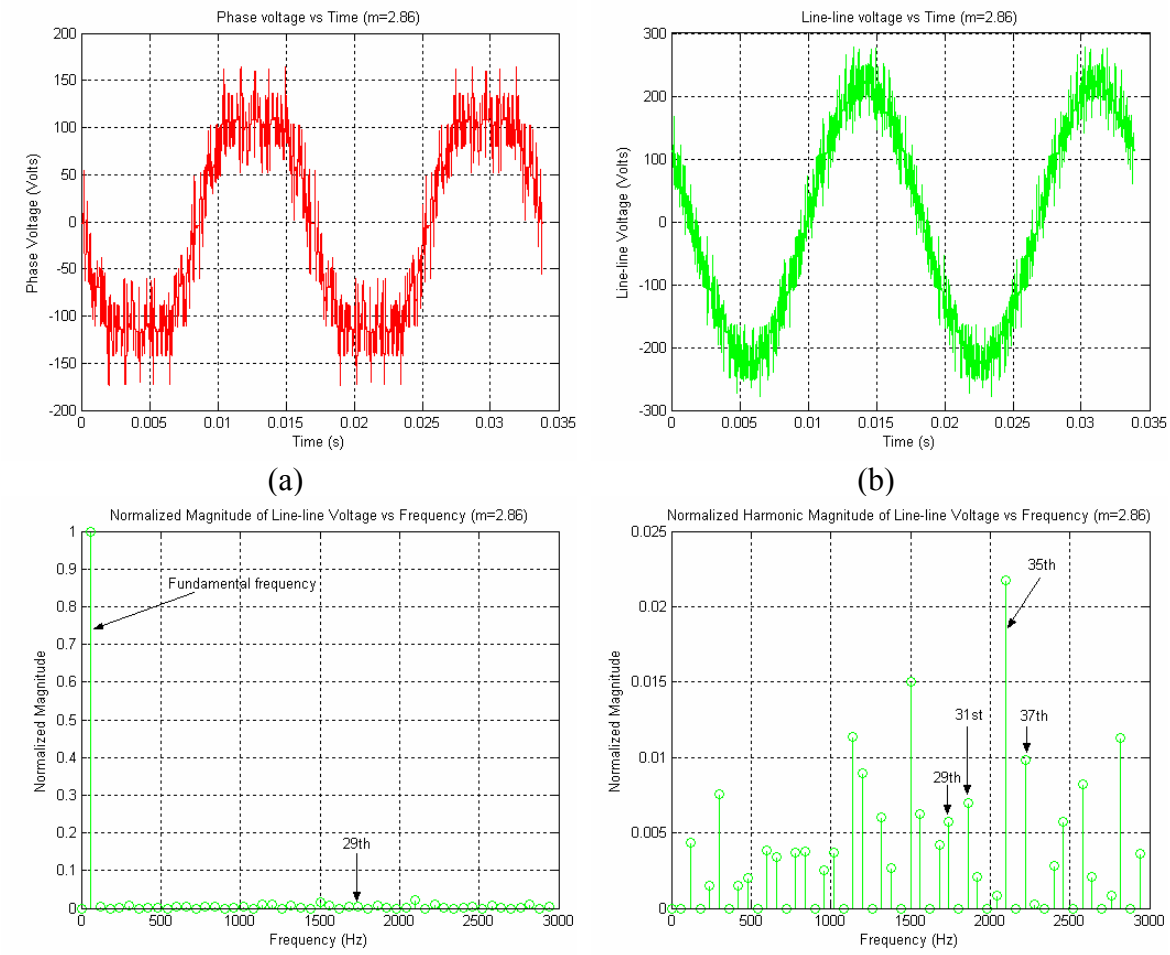


Figure 5.16: Experiment with the 5th to 37th harmonics eliminated with unequal DC voltages (THD = 3.59%) (a) phase voltage; (b) line-line voltage; (c) normalized FFT analysis of line-line voltage; (d) normalized harmonic contents of line-line voltage with fundamental content removed

From Table 5.1, it can be seen that the THD of experiment corresponds well with the THD of the theoretical and simulation for case 1 of harmonics elimination 5-13th. For case 2 of harmonics elimination 5-25th, the THD of the experiment is a little higher than the THD of the theoretical computation, but it corresponds well with the THD of the simulation. For case 3 of harmonics elimination 5-37th, the THD of the experiment is much higher than the THD of the theoretical, but it corresponds well with the THD of simulation. The reason that the THD of the experiments in case 2 and case 3 are higher than that of the theoretical computation is the control accuracy prevents the eliminated harmonics to be exactly zero, and the residues of these low order harmonics make a major contribution to the THD. This can be seen from the FFT analysis figures: the low order harmonics are not exactly zero although they are very small.

5.7. Summary

This chapter extends the active harmonic elimination method to multilevel converters with unequal DC voltages. First, the resultant method and harmonic elimination theory are used to determine switching angles for unipolar converters. Second, the unipolar converters are used to construct multilevel converters and the combination for optimal THD control is searched. Third, the active harmonic elimination method is used to eliminate higher order harmonics.

To apply this method to the multilevel converters with unequal DC voltages, the method is first developed for equal DC voltage cases. Then it is extended for unequal DC voltages. The simulation results show that the proposed control method is very effective in multilevel converters with equal DC voltages or unequal DC voltages.

6. Optimization of Active Harmonic Elimination

Harmonic elimination methods in multilevel converters presented in Chapter 4 and 5 has two procedures; the first is to use the fundamental frequency switching scheme or the unipolar switching scheme to eliminate low order harmonics, then to use the active harmonic elimination method to eliminate high order harmonics. The order of the two procedures results in high switching number in a cycle and high switching loss. If the fundamental frequency switching scheme or the unipolar switching scheme can be used to eliminate high order harmonics, and the active harmonic elimination method can be used to eliminate low order harmonics, the switching number in a cycle and switching loss will decrease. In this chapter, the fundamental switching scheme and the unipolar switching scheme are used to eliminate high order harmonics, and the active harmonic elimination method is used to eliminate low order harmonics. This method is compared to that in Chapter 4 for switching number and output voltage THD.

In Chapter 5, the active harmonic elimination method is extended to unequal DC voltage cases. This method also has a disadvantage of high switching frequency. To decrease switching frequency, the switching angles for the lowest harmonic distortion are proposed as initial guesses for Newton's method to find a new set switching angles to completely eliminate the specified harmonics. This optimized harmonic elimination method will have an advantage of lower switching frequency.

6.1. Optimization of Active Harmonic Elimination Method with Fundamental Frequency Switching Scheme

Based on the harmonic elimination theory discussed previously, the fundamental switching scheme with n switching angles can eliminate any specified n-1 harmonics. For example, in the 11-level multilevel converter case, any specified 4 harmonics can be cancelled. In this research case, the 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, 19^{th}, 23^{rd}, 25^{th}, 29^{th} and 31^{st}

harmonics will be eliminated. If we apply the active harmonic elimination method to the 11-level multilevel converter case, the 5^{th}, 7^{th}, 11^{th}, 13^{th} low order harmonics are cancelled by the fundamental frequency switching method, and the 17^{th}, 19^{th}, 23^{rd}, 25^{th}, 29^{th} and 31^{st} harmonics are eliminated by the active harmonic elimination method. To get the switching angles for the fundamental frequency method, the following equations need to be solved.

$$\begin{aligned}
&\cos(\theta_1)+\cos(\theta_2)+\cos(\theta_3)+\cos(\theta_4)+\cos(\theta_5)=m\\
&\cos(5\theta_1)+\cos(5\theta_2)+\cos(5\theta_3)+\cos(5\theta_4)+\cos(5\theta_5)=0\\
&\cos(7\theta_1)+\cos(7\theta_2)+\cos(7\theta_3)+\cos(7\theta_4)+\cos(7\theta_5)=0\\
&\cos(11\theta_1)+\cos(11\theta_2)+\cos(11\theta_3)+\cos(11\theta_4)+\cos(11\theta_5)=0\\
&\cos(13\theta_1)+\cos(13\theta_2)+\cos(13\theta_3)+\cos(13\theta_4)+\cos(13\theta_5)=0
\end{aligned} \tag{6.1}$$

where m is defined as the modulation index.

In this control case, the additional switching number required to eliminate the 17^{th}, 19^{th}, 23^{rd}, 25^{th}, 29^{th} and 31^{st} harmonics is:

$$N_{sw} \le \sum_{n\in\{17,19,23,25,29,31\}} n \tag{6.2}$$

where n is the harmonic number. As discussed in Chapter 4, if a harmonic is near zero, the control resolution is lower than that required to eliminate the harmonic, then switching will not occur. And the overlaps also will decrease the switching times. The upper bound of the additional switching number is 144.

To decrease the required switching number, the high order harmonics 31^{st}, 29^{th}, 23^{rd}, 19^{th} could be chosen to be eliminated by the fundamental frequency method, and the 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, and 25^{th} harmonics could be eliminated by the active harmonic elimination method. This method is referred to as the optimized active harmonic elimination method. Here, the 25^{th} harmonic cannot be chosen to be eliminated by the fundamental frequency switching method because the active harmonic method will generate a new 25^{th} harmonic when it is used to eliminate the 5^{th} harmonic.

Similar to the active harmonic elimination method, to find the switching angles for the optimized active harmonic elimination method, the following equations need to be solved.

$$\begin{aligned}
&\cos(\theta_1)+\cos(\theta_2)+\cos(\theta_3)+\cos(\theta_4)+\cos(\theta_5)=m\\
&\cos(19\theta_1)+\cos(19\theta_2)+\cos(19\theta_3)+\cos(19\theta_4)+\cos(19\theta_5)=0\\
&\cos(23\theta_1)+\cos(23\theta_2)+\cos(23\theta_3)+\cos(23\theta_4)+\cos(23\theta_5)=0\\
&\cos(29\theta_1)+\cos(29\theta_2)+\cos(29\theta_3)+\cos(29\theta_4)+\cos(29\theta_5)=0\\
&\cos(31\theta_1)+\cos(31\theta_2)+\cos(31\theta_3)+\cos(31\theta_4)+\cos(31\theta_5)=0
\end{aligned} \tag{6.3}$$

For the optimized active harmonic elimination method, the additional switching number required to eliminate the 5th, 7th, 11th, 13th, 17th, and 25th harmonics is:

$$N_{sw} \le \sum_{n\in\{5,7,11,13,17,25\}} n \tag{6.4}$$

The upper bound of the additional switching number is 78. It is about half of the switchings than when the active harmonic elimination method is used for high frequency harmonics. In theory, the optimized active harmonic elimination method has less switching number than that of the active harmonic elimination method.

Equation (6.1) can be solved by the resultant method and all the solutions can be found, but (6.3) cannot be solved by the resultant method because the degrees of its polynomials are too high.

To conquer this problem, the fundamental frequency switching angle computation of (6.3) is solved by the Newton climbing method developed in Chapter 3. The initial guess is from the solutions of (6.1). Although the Newton climbing method cannot find all the solutions for (6.3), if the solutions are continuous, it is still practical for applications because the THD difference for high-order solutions is low for different solution sets.

As expected, most of the continuous solutions can be found by this search method. The solutions of (6.3) vs. modulation index $m = \pi V_1/(4V_{dc})$ are shown in Figure 6.1. The lowest THD of active harmonic elimination method and optimized active harmonic elimination method is shown in Figure 6.2.

From Figure 6.1, it can be seen the modulation index range is from 2.15 to 4.14. The solutions are continuous. It also can be seen that for a specific modulation index, there are more solution sets for (6.3) than for (6.1). If the equation has higher harmonics, then it has more solution sets.

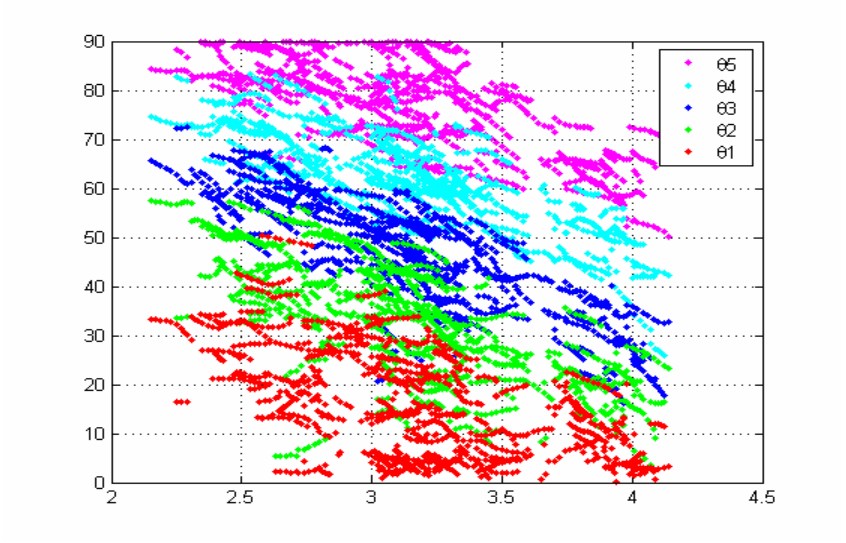


Figure 6.1: Solutions to 11-level multilevel converter case to eliminate the 19th, 23rd, 29th, 31st harmonics with fundamental frequency switching scheme

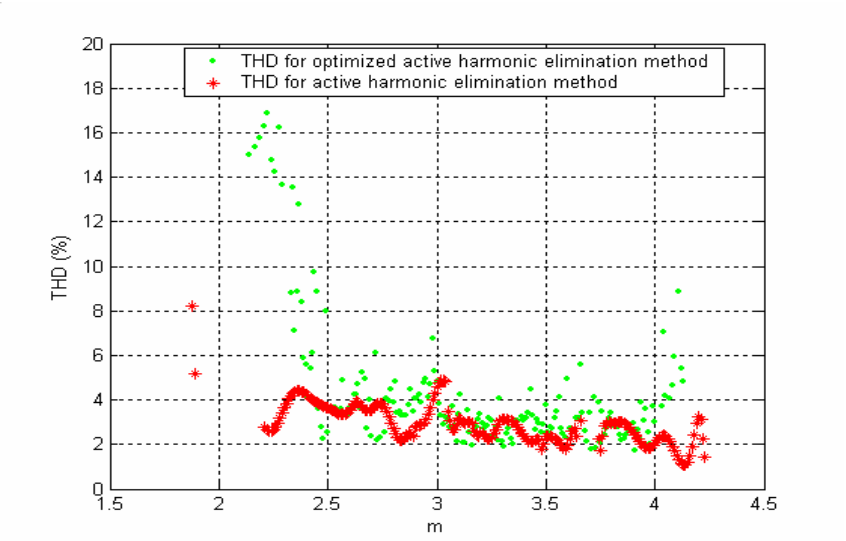


Figure 6.2: Lowest THD for active harmonic elimination method and optimized active harmonic elimination method

From Figure 6.2, it can be seen that for some low modulation indices and high modulation indices, the THD of the optimized active harmonic elimination method is higher than that of the active harmonic elimination method. For most of the range of the modulation indices, the difference in THD is very low.

The switching number in a cycle corresponding to the lowest THD situation for both the active harmonic elimination method and the optimized active harmonic elimination method is shown in Figure 6.3.

As discussed previously, the upper bound of the switching number for the active harmonic elimination method is 144 and 78 for the optimized harmonic elimination method. It can be derived that to eliminate the same harmonics and achieve a similar THD, the optimized harmonic elimination method needs less switching number than that of the active harmonic elimination method with fundamental frequency switching scheme. Therefore, the optimized active harmonic elimination method results in lower switching loss and higher efficiency.

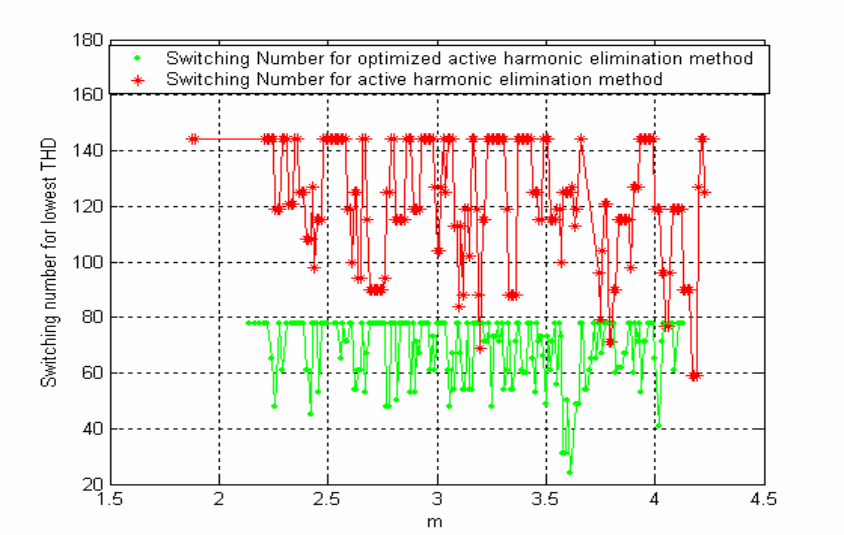


Figure 6.3: Switching number corresponding to the lowest THD for active harmonic elimination method and optimized active harmonic elimination method show in Figure 6.2

6.2. High Order Harmonic Elimination Optimization of Active Harmonic Elimination Method with Unipolar Switching Scheme

If the unipolar switching scheme is used for multilevel converter control with equal or unequal DC voltages, the optimization method could use the unipolar switching scheme to eliminate high order harmonics and use the active harmonic elimination method to eliminate low order harmonics to decrease switching frequency.

Figure 6.4 shows one example of using the five-angle unipolar switching scheme to eliminate high order harmonics. The equation for this method is:

$$\begin{aligned}
&\cos(\theta_1)-\cos(\theta_2)+\cos(\theta_3)-\cos(\theta_4)+\cos(\theta_5)=m\\
&\cos(19\theta_1)-\cos(19\theta_2)+\cos(19\theta_3)-\cos(19\theta_4)+\cos(19\theta_5)=0\\
&\cos(23\theta_1)-\cos(23\theta_2)+\cos(23\theta_3)-\cos(23\theta_4)+\cos(23\theta_5)=0\\
&\cos(29\theta_1)-\cos(29\theta_2)+\cos(29\theta_3)-\cos(29\theta_4)+\cos(29\theta_5)=0\\
&\cos(31\theta_1)-\cos(31\theta_2)+\cos(31\theta_3)-\cos(31\theta_4)+\cos(31\theta_5)=0
\end{aligned} \tag{6.5}$$

The equation is solved by the Newton climbing method with the initial guesses from the solutions to eliminate the 5th, 7th, 11th, and 13th harmonics using the resultant method.

The solutions to equation (6.5) are shown in Figure 6.4.

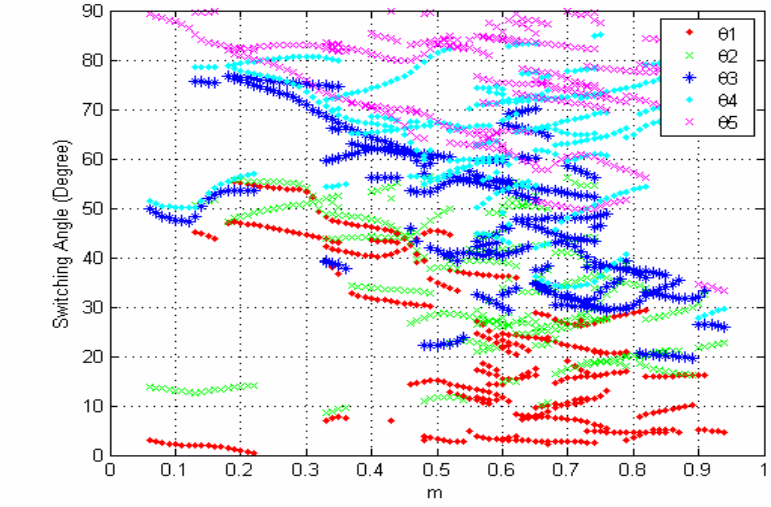


Figure 6.4: Switching angles for five-angle unipolar scheme to eliminate the 19th, 23rd, 29th, and 31st harmonics

From Figure 6.4, it also can be seen that even the Newton climbing method does not guarantee to find all the solutions. However, it still can find enough continuous solutions for practical applications. Therefore, the lowest THD combination search method and the active harmonic elimination method proposed in Chapter 5 could be used to eliminate the specified harmonics. The upper bound switching number for harmonic elimination to 31st is 5+7+11+13+17+25 = 78 instead of 17+19+23+25+29+31 = 144, which is required for the active harmonic elimination method. To further decrease the switching frequency, another optimization method with the unipolar switching scheme is proposed. This is described in the next section.

6.3. Optimization of Active Harmonic Elimination Method with Unipolar Switching Scheme Using the Newton Climbing Method

For multilevel converters, the second optimization method could be to search an initial guess for the Newton climbing method to solve harmonic equations to directly eliminate the specified harmonics. This method can further decrease the switching frequency.

As discussed in Chapter 5, the total modulation index is $m = \sum_{i=1}^{s} c_i \frac{V_{dci}}{V_{dc}} m_i$ for a multilevel converter when decouple control is applied to it. Here, V_{dc} is the nominal DC voltage, V_{dci} is the ith DC voltage, and $c_i (c_i \in \{-1,0,1\})$ is called the combination coefficient. For convenience, here let $k_i = \frac{V_{dci}}{V_{dc}}$, then $m = \sum_{i=1}^{s} c_i k_i m_i$.

Because the harmonic contents are positive for some modulation indices and are negative for other modulation indices, it is possible to get a combination of several unipolar converters for each modulation index *m* of the multilevel converter with the lowest harmonic distortion for the specified harmonics.

(1). Five-level case

The modulation index is

$$m = \sum_{i=1}^{2} c_i k_i m_i \tag{6.6}$$

The initial switching angle guess is found by searching for the lowest harmonic distortion:

$$HD = V_{17}{}^2 + V_{19}{}^2 + V_{23}{}^2 + V_{25}{}^2 + V_{29}{}^2 \tag{6.7}$$

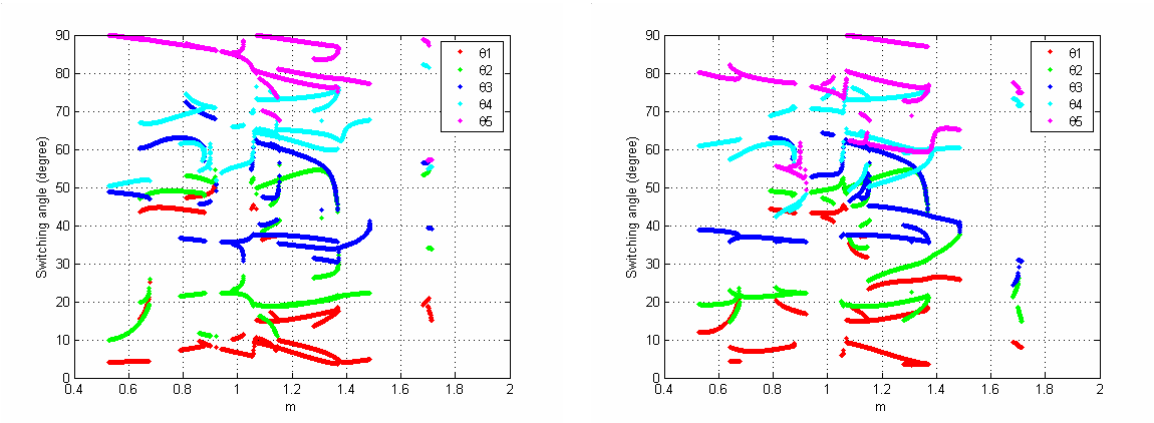
Here, V_n is the n^{th} harmonic which can be expressed as:

$$V_n = \sum_{i=1}^{s} \frac{4c_i k_i V_{dc}}{n\pi} [\cos(n\theta_{i1}) - \cos(n\theta_{i2}) + \cos(n\theta_{i3}) - \cos(n\theta_{i4}) + \cos(n\theta_{i5})] \tag{6.8}$$

The switching angle sets corresponding to the lowest harmonic distortion (HD_{min}) could be used as initial guesses to solve the equation:

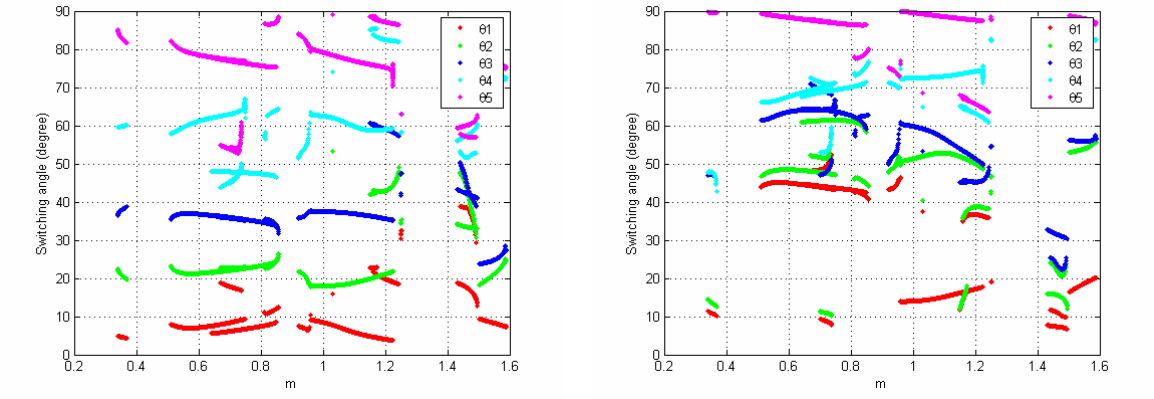
$$\begin{aligned}
&k_1 c_1 \sum_{i=1}^{5} (-1)^{i+1} \cos(\theta_{1i}) + k_2 c_2 \sum_{i=1}^{5} (-1)^{i+1} \cos(\theta_{2i}) = m \\
&k_1 c_1 \sum_{i=1}^{5} (-1)^{i+1} \cos(5\theta_{1i}) + k_2 c_2 \sum_{i=1}^{5} (-1)^{i+1} \cos(5\theta_{2i}) = 0 \\
&\vdots \\
&k_1 c_1 \sum_{i=1}^{5} (-1)^{i+1} \cos(25\theta_{1i}) + k_2 c_2 \sum_{i=1}^{5} (-1)^{i+1} \cos(25\theta_{2i}) = 0 \\
&k_1 c_1 \sum_{i=1}^{5} (-1)^{i+1} \cos(29\theta_{1i}) + k_2 c_2 \sum_{i=1}^{5} (-1)^{i+1} \cos(29\theta_{2i}) = 0
\end{aligned} \tag{6.9}$$

By using the proposed method, the equal case ($k_1 = k_2 = 1$) and three unequal cases ($k_1 = 0.8$, $k_2 = 1$; $k_1 = 0.75$, $k_2 = 1$; $k_1 = 0.67$, $k_2 = 1$) are computed. The switching angles are shown in Figures 6.5— 6.8.



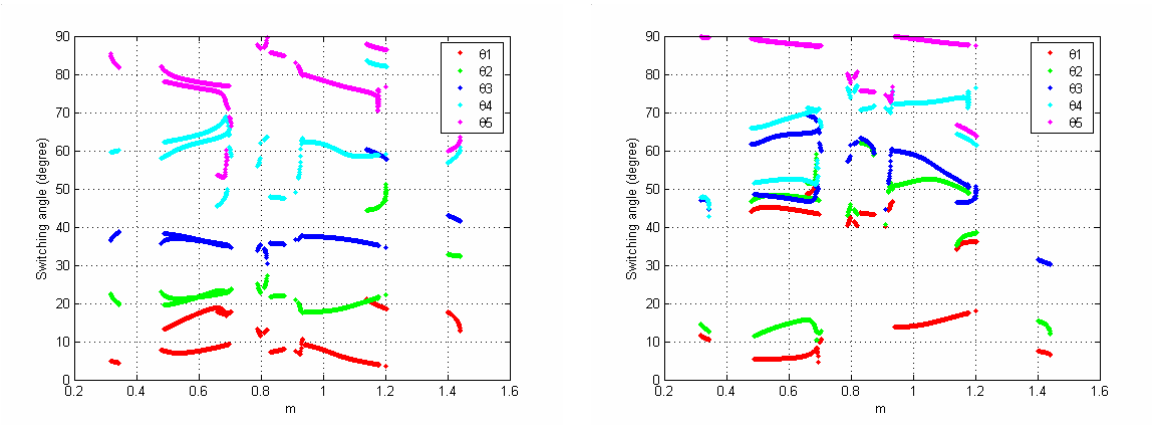
(a) (b)

Figure 6.5: Switching angles for five-level multilevel converter to eliminate harmonics below the 29th ($k_1 = k_2 = 1$) (a) switching angle set 1; (b) switching angle set 2



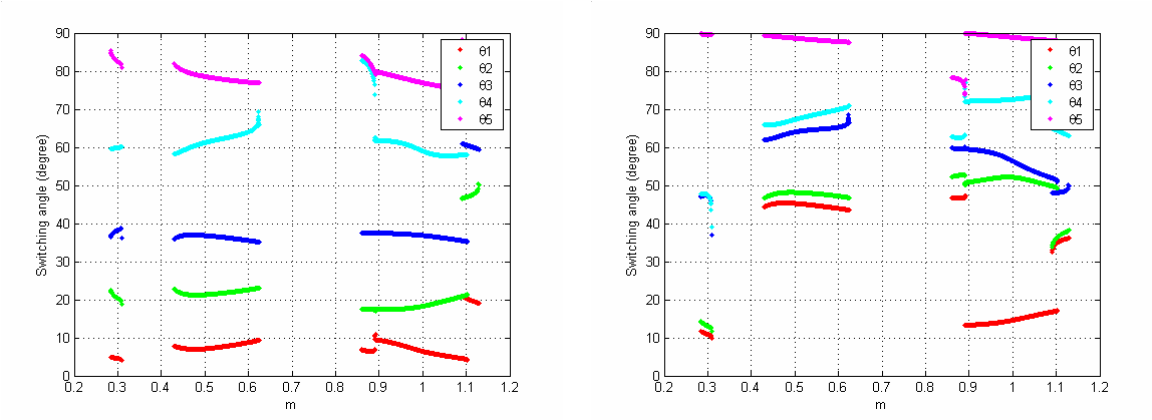
(a) (b)

Figure 6.6: Switching angles for five-level multilevel converter to eliminate harmonics below the 29th ($k_1 = 0.8$, $k_2 = 1$) (a) switching angle set 1; (b) switching angle set 2



(a) (b)

Figure 6.7: Switching angles for five-level multilevel converter to eliminate harmonics below the 29th ($k_1 = 0.75$, $k_2 = 1$) (a) switching angle set 1; (b) switching angle set 2



(a) (b)

Figure 6.8: Switching angles for five-level multilevel converter to eliminate harmonics below the 29th ($k_1 = 0.67$, $k_2 = 1$) (a) switching angle set 1; (b) switching angle set 2

From Figures 6.5 — 6.8, it can be seen that if the coefficients k_1 and k_2 are nearly equal, more solutions could be found and the solutions have wider modulation index range. For some modulation indices, no solution can be found by this method.

(2). Seven-level case

The modulation index is

$$m = \sum_{i=1}^{3} c_i k_i m_i \tag{6.10}$$

The initial switching angle guess is found by searching the lowest harmonic distortion:

$$HD = V_{17}{}^2 + V_{19}{}^2 + V_{23}{}^2 + V_{25}{}^2 + V_{29}{}^2 + V_{31}{}^2 + V_{35}{}^2 + V_{37}{}^2 + V_{41}{}^2 + V_{43}{}^2 \tag{6.11}$$

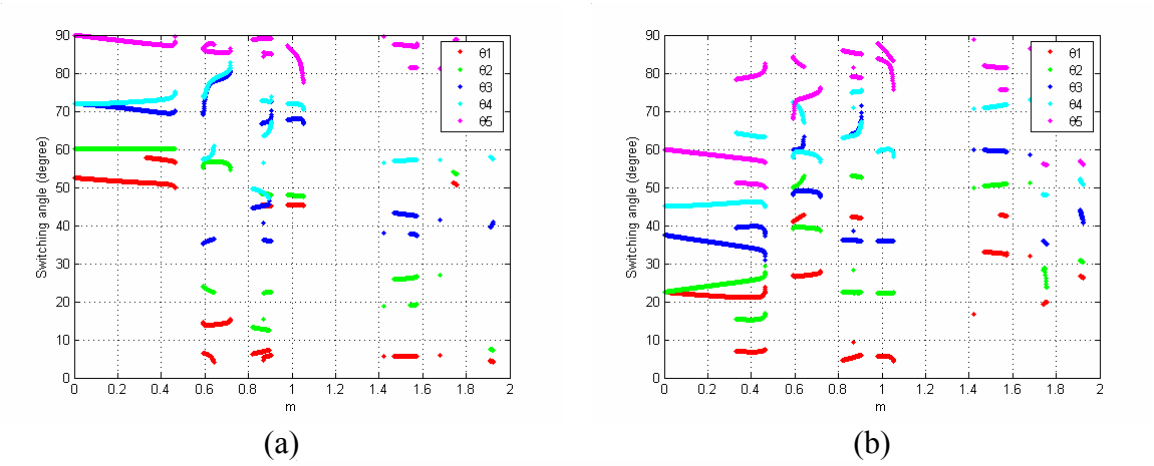
Here, V_n is the n^{th} harmonic which can be expressed as by (6.8).

The switching angle sets corresponding to the lowest harmonic distortion (HD_{min}) could be used as initial guesses to solve the equation:

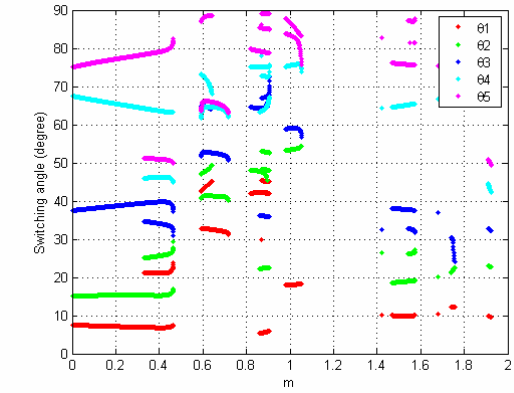
$$\begin{aligned}
&\sum_{j=1}^{3} k_j c_j \sum_{i=1}^{5} (-1)^{i+1} \cos\left(\theta_{ji}\right) = m \\
&\sum_{j=1}^{3} k_j c_j \sum_{i=1}^{5} (-1)^{i+1} \cos\left(5\theta_{ji}\right) = 0 \\
&\vdots \\
&\sum_{j=1}^{3} k_j c_j \sum_{i=1}^{5} (-1)^{i+1} \cos\left(41\theta_{ji}\right) = 0 \\
&\sum_{j=1}^{3} k_j c_j \sum_{i=1}^{5} (-1)^{i+1} \cos\left(43\theta_{ji}\right) = 0
\end{aligned} \tag{6.12}$$

By using the proposed method, the equal case ($k_1 = k_2 = k_3 = 1$) and two unequal cases ($k_1 = 0.9$, $k_2 = 0.95$, $k_3 = 1$; $k_1 = 0.6$, $k_2 = 0.8$, $k_3 = 1$) are computed. The switching angles are shown in Figures 6.9— 6.11.

From Figures 6.9—6.11, it also can be seen that if the coefficients k_1, k_2 and k_3 are close to the same value, more solutions can be found and the solutions have wider modulation index range. For some modulation indices, no solution can be found by this method.

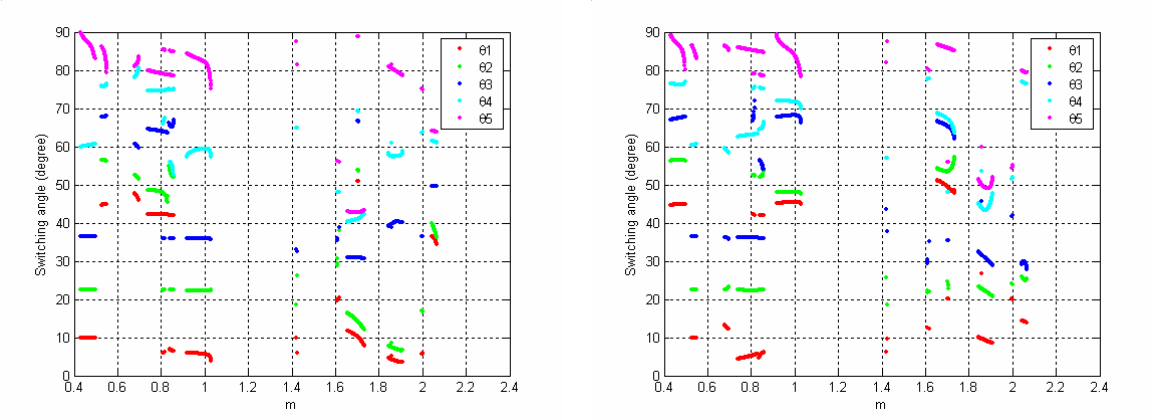


(a) (b)

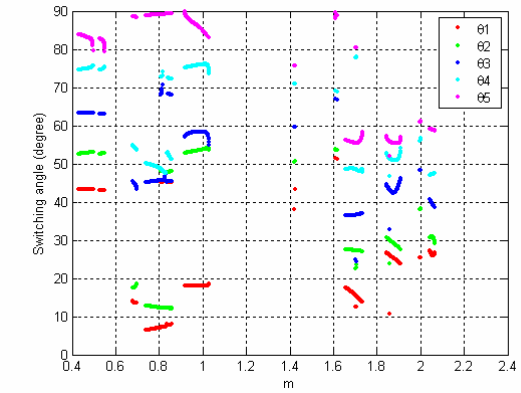


(c)

Figure 6.9: Switching angles for seven-level multilevel converter to eliminate harmonics below the 43rd ($k_1 = 1$, $k_2 = 1$, $k_3 = 1$) (a) switching angle set 1; (b) switching angle set 2; (c) switching angle set 3



(a) (b)



(c)

Figure 6.10: Switching angles for seven-level multilevel converter to eliminate harmonics below the 43rd ($k_1 = 0.9$, $k_2 = 0.95$, $k_3 = 1$) (a) switching angle set 1; (b) switching angle set 2; (c) switching angle set 3

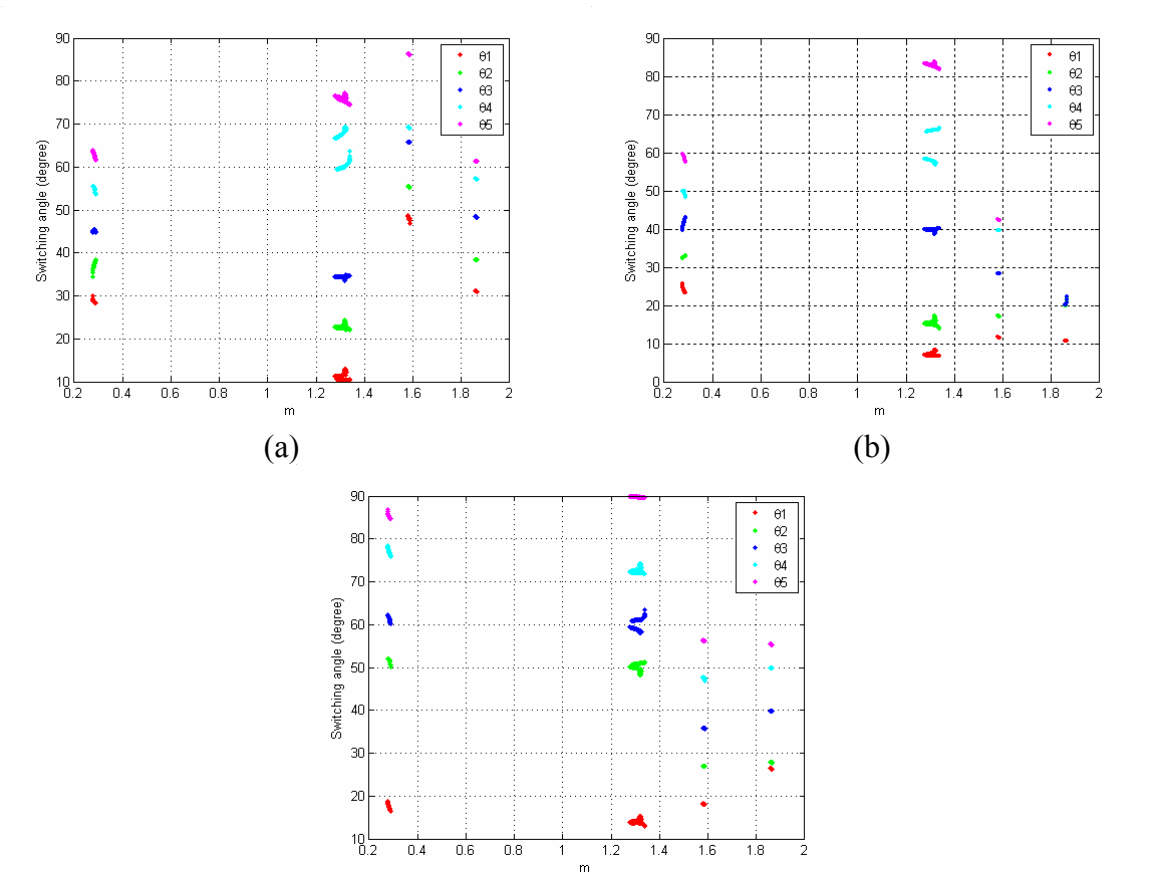


Figure 6.11: Switching angles for seven-level multilevel converter to eliminate harmonics below the 43rd ($k_1 = 0.6$, $k_2 = 0.8$, $k_3 = 1$) (a) switching angle set 1; (b) switching angle set 2; (c) switching angle set 3

Compared to the first optimization method, the second optimization method has lower switching frequency, but the solutions are not available for the whole modulation index range. The first optimization method can be applied to the whole modulation index range.

Therefore, for practical applications, the second optimization method is the first choice. If the second optimization method cannot find a solution for a specified modulation index, the first optimization method can be used.

6.4. Simulation

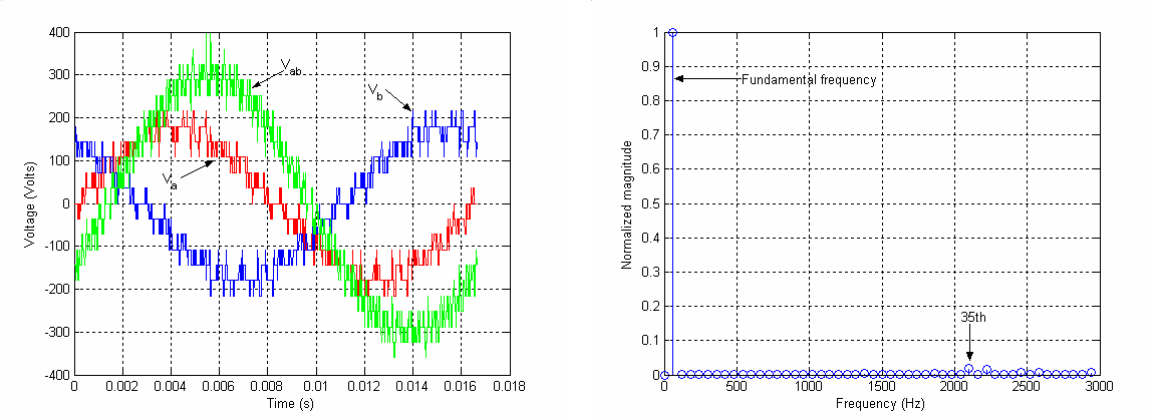
To verify the active harmonic elimination method, an equal DC voltage case and an unequal DC voltage case simulation studies have been implemented. The simulation includes output voltage waveform and FFT analysis, which are show in Figures 12—19.

6.5. Experiment

6.5.1. Experiment for Optimized Active Harmonic Elimination Method with Fundamental Frequency Switching Scheme

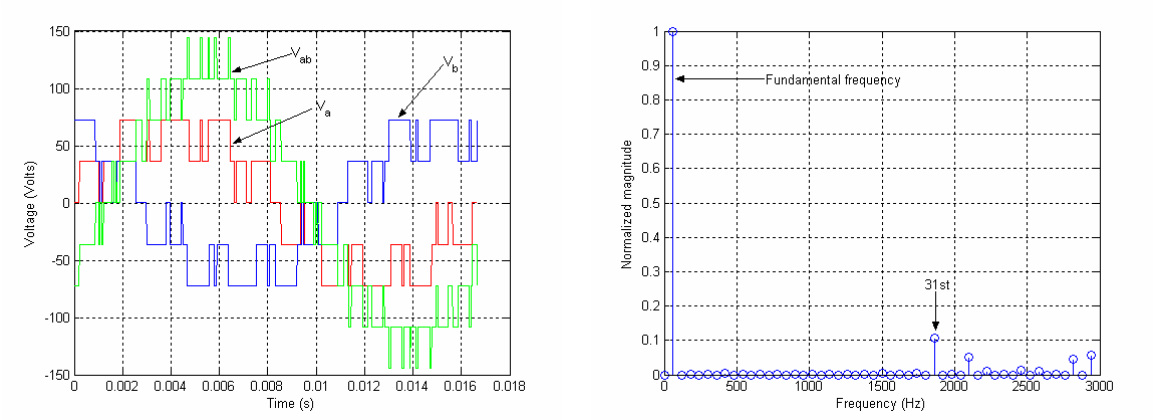
To validate the optimized active harmonic elimination method, the m = 3.79 case is chosen for optimized active harmonic elimination method with fundamental frequency switching scheme to implement on the multilevel converter. Figure 6.20 shows the experimental line-line voltage for the optimized active harmonic elimination method with fundamental frequency switching scheme and its corresponding normalized FFT analysis.

Form Figure 6.20, it can be seen that the harmonics have been eliminated up to the 31^{st} with the optimized active harmonic elimination method. The experimental THD is 3.52%. It corresponds very well with the theoretical computation of 3.15%. The switching number is 78 instead of 121 for the active harmonic elimination method.



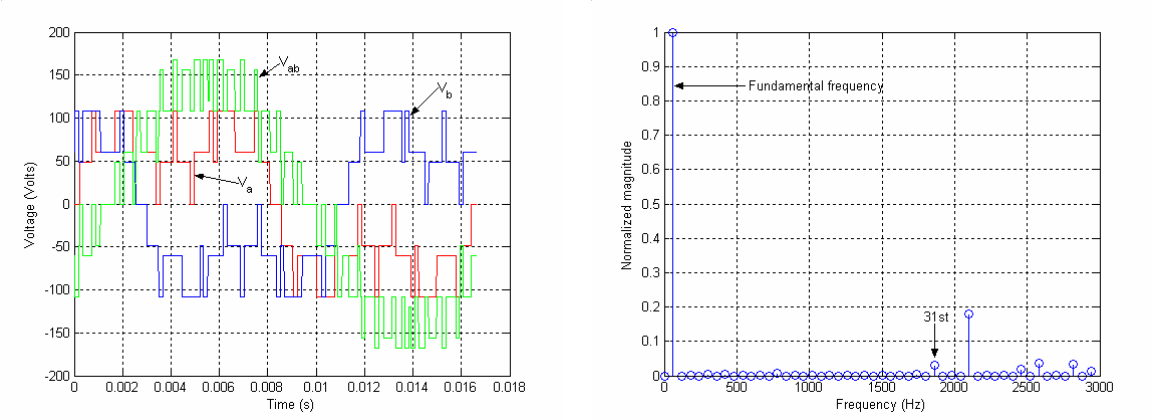
(a) (b)

Figure 6.12: Simulation of high order harmonic elimination optimization of active harmonic elimination method with fundamental switching scheme (a) voltage waveform; (b) normalized FFT analysis of line-line voltage (m = 3.79,THD = 3.03%)



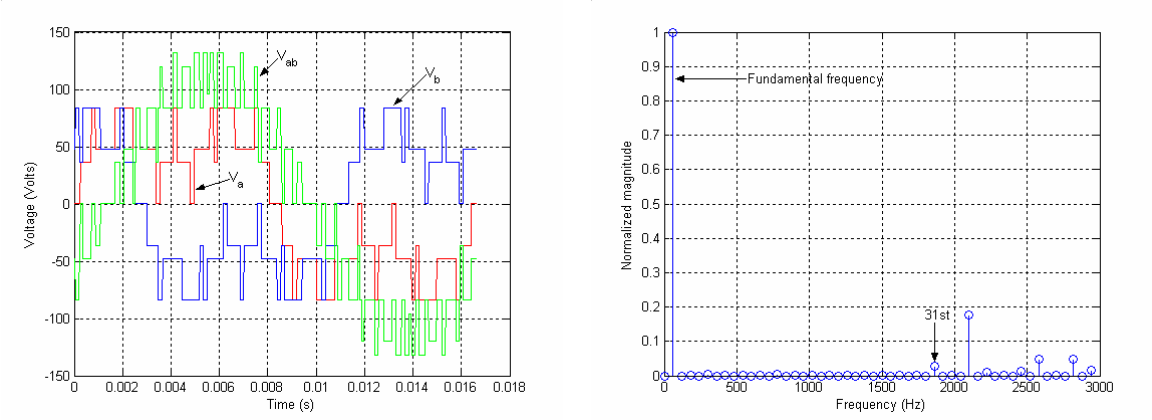
(a) (b)

Figure 6.13: Simulation of active harmonic elimination method with unipolar switching scheme (a) voltage waveform; (b) normalized FFT analysis of line-line voltage ($k_1 = k_2$, V_{dc} = 36 V, m = 1.460, THD = 14.1%)



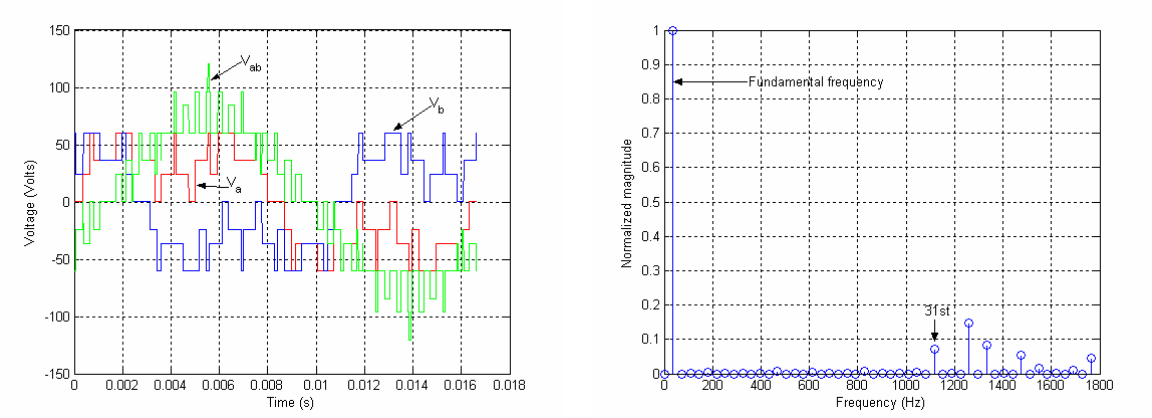
(a) (b)

Figure 6.14: Simulation of active harmonic elimination method with unipolar switching scheme (a) voltage waveform; (b) normalized FFT analysis of line-line voltage (k_1 = 0.8, k_2 = 1, V_{dc} = 60 V, m = 1.120, THD = 19.13%)



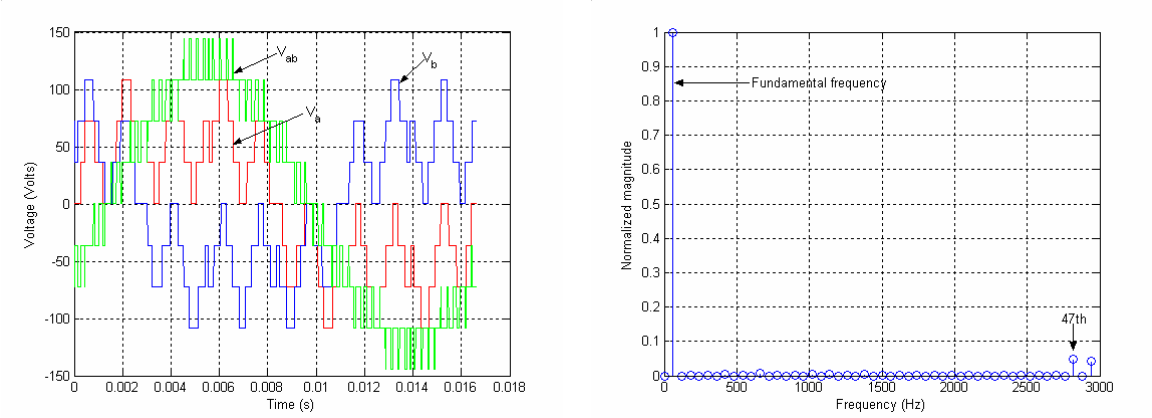
(a) (b)

Figure 6.15: Simulation of active harmonic elimination method with unipolar switching scheme (a) voltage waveform; (b) normalized FFT analysis of line-line voltage (k_1 = 0.75, k_2 = 1, V_{dc} = 48 V, m = 1.080, THD = 19.19%)



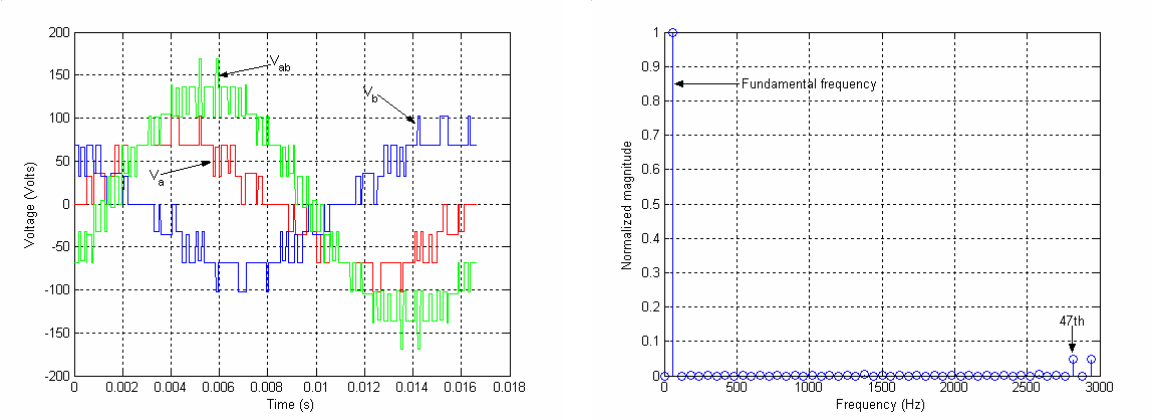
(a) (b)

Figure 6.16: Simulation of active harmonic elimination method with unipolar switching scheme (a) voltage waveform; (b) normalized FFT analysis of line-line voltage (k_1 = 0.67, k_2 = 1, V_{dc} = 36 V, m = 0.960, THD = 19.87%)



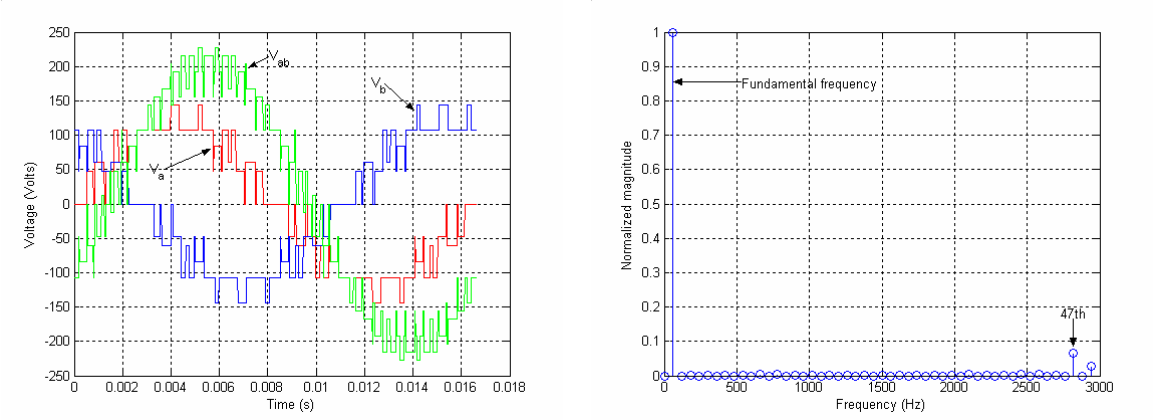
(a) (b)

Figure 6.17: Simulation of active harmonic elimination method with unipolar switching scheme (a) voltage waveform; (b) normalized FFT analysis of line-line voltage (k_1 = 1, k_2 = 1, k_3 = 1, V_{dc} = 36 V, m = 1.500, THD = 6.69%)



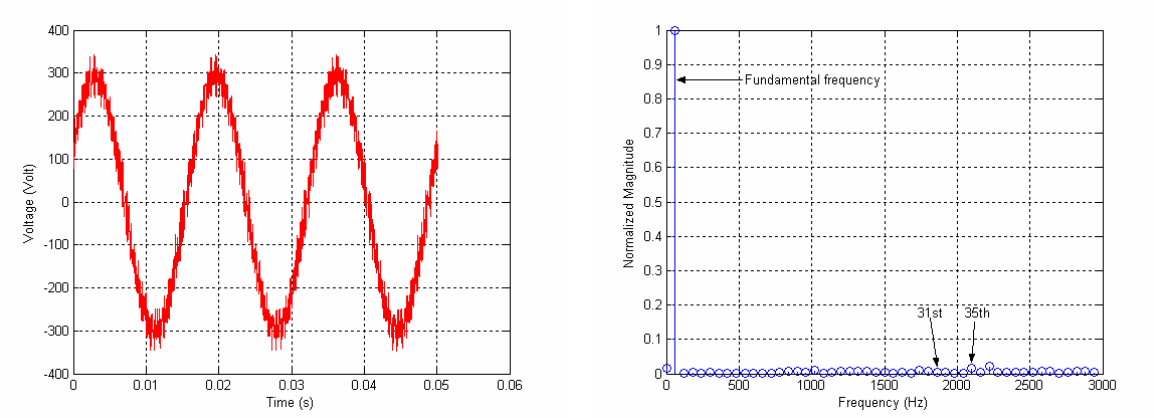
(a) (b)

Figure 6.18: Simulation of active harmonic elimination method with unipolar switching scheme (a) voltage waveform; (b) normalized FFT analysis of line-line voltage (k_1 = 0.9, k_2 = 0.95, k_3 = 1, V_{dc} = 38 V, m = 1.660, THD = 6.89%)



(a) (b)

Figure 6.19: Simulation of active harmonic elimination method with unipolar switching scheme (a) voltage waveform; (b) normalized FFT analysis of line-line voltage (k_1 = 0.6, k_2 = 0.8, k_3 = 1, V_{dc} = 60 V, m = 1.580, THD = 7.09%)



(a) (b)

Figure 6.20: Experiment of high order harmonic elimination optimization of active harmonic elimination method with fundamental switching scheme (a) line-line voltage; (b) normalized FFT analysis of line-line voltage (m = 3.79,THD = 3.52%)

6.5.2. Experiment for Optimized Active Harmonic Elimination Method with Unipolar Switching Scheme

The simulation cases have been implemented on a multilevel converter. The experiments are shown in Figures 6.21— 6.27.

For convenience, the THD for the theoretical computation, simulation, and experiment are summarized in Table 6.1.

From Table 6.1, it can be derived that the THD for theoretical computation, simulation, and experiment correspond very well. Therefore, the optimized active harmonic elimination method is confirmed by simulation and experiment.

6.6. Summary

This chapter developed the optimized active harmonic elimination method which eliminates high order harmonics by the fundamental frequency switching method and eliminates low order harmonics by the active harmonic elimination method for multilevel converter control.

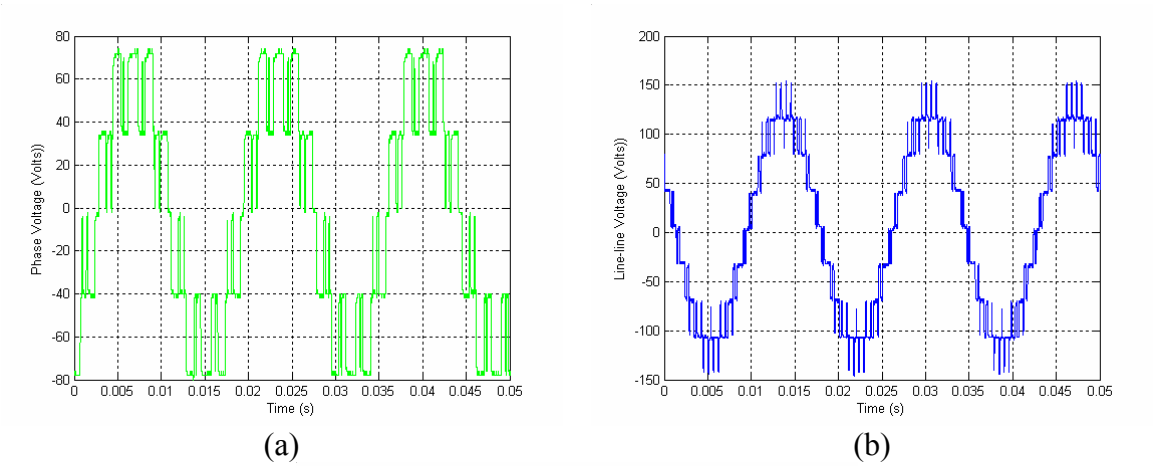


Figure 6.21: Experiment of active harmonic elimination method with unipolar switching scheme (a) phase voltage waveform; (b) line-line voltage; (c) normalized FFT analysis of line-line voltage ($k_1 = k_2$, V_{dc} = 36 V, m = 1.460, THD = 13.3%)

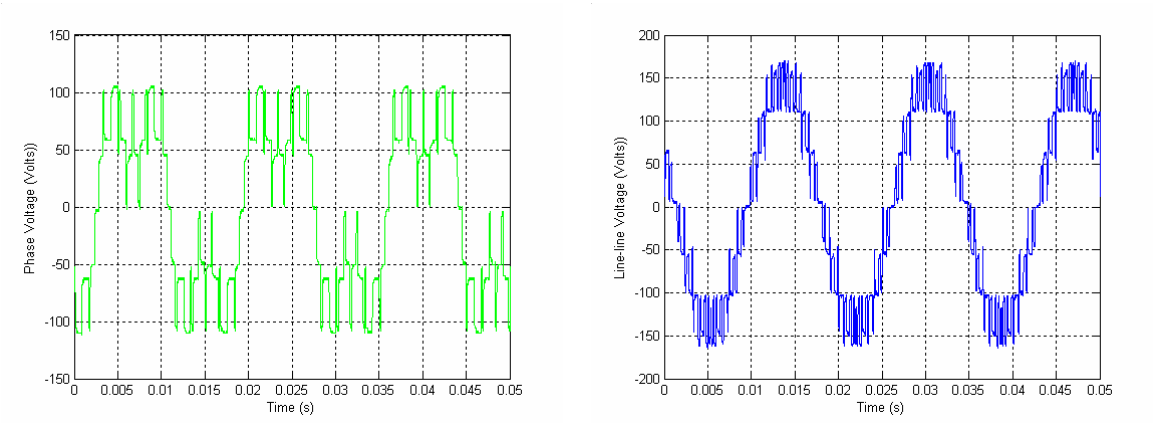


Figure 6.22: Experiment of active harmonic elimination method with unipolar switching scheme (a) phase voltage waveform; (b) line-line voltage; (c) normalized FFT analysis of line-line voltage (k_1 = 0.8, k_2 = 1, V_{dc} = 60 V, m = 1.120, THD = 15.8%)

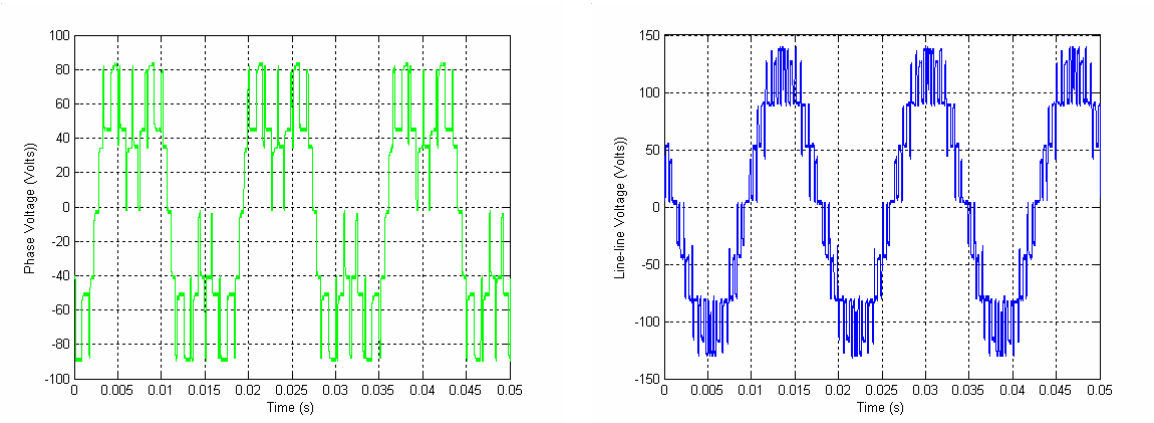


Figure 6.23: Experiment of active harmonic elimination method with unipolar switching scheme (a) phase voltage waveform; (b) line-line voltage; (c) normalized FFT analysis of line-line voltage (k_1 = 0.75, k_2 = 1, V_{dc} = 48 V, m = 1.080, THD = 17.4%)

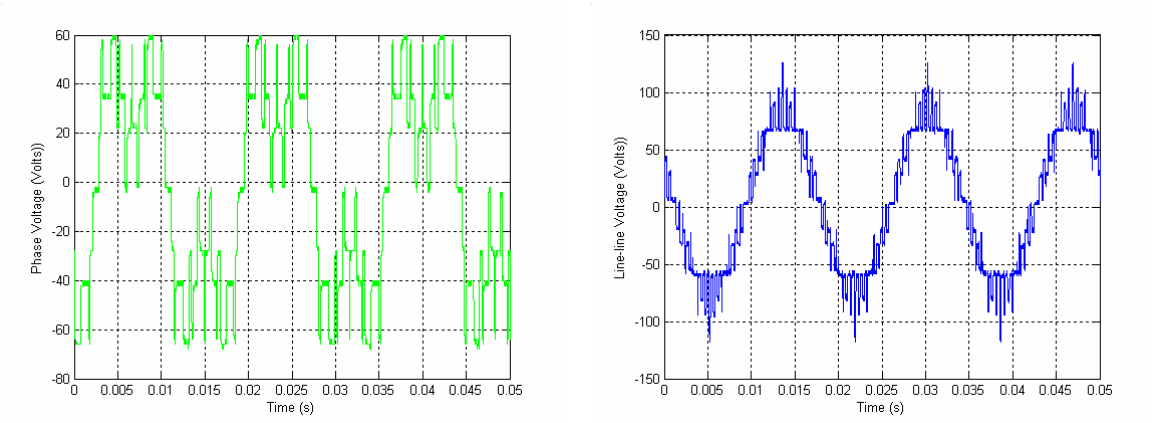


Figure 6.24: Experiment of active harmonic elimination method with unipolar switching scheme (a) phase voltage waveform; (b) line-line voltage; (c) normalized FFT analysis of line-line voltage (k_1 = 0.67, k_2 = 1, V_{dc} = 36V, m = 0.960, THD = 17.5%)

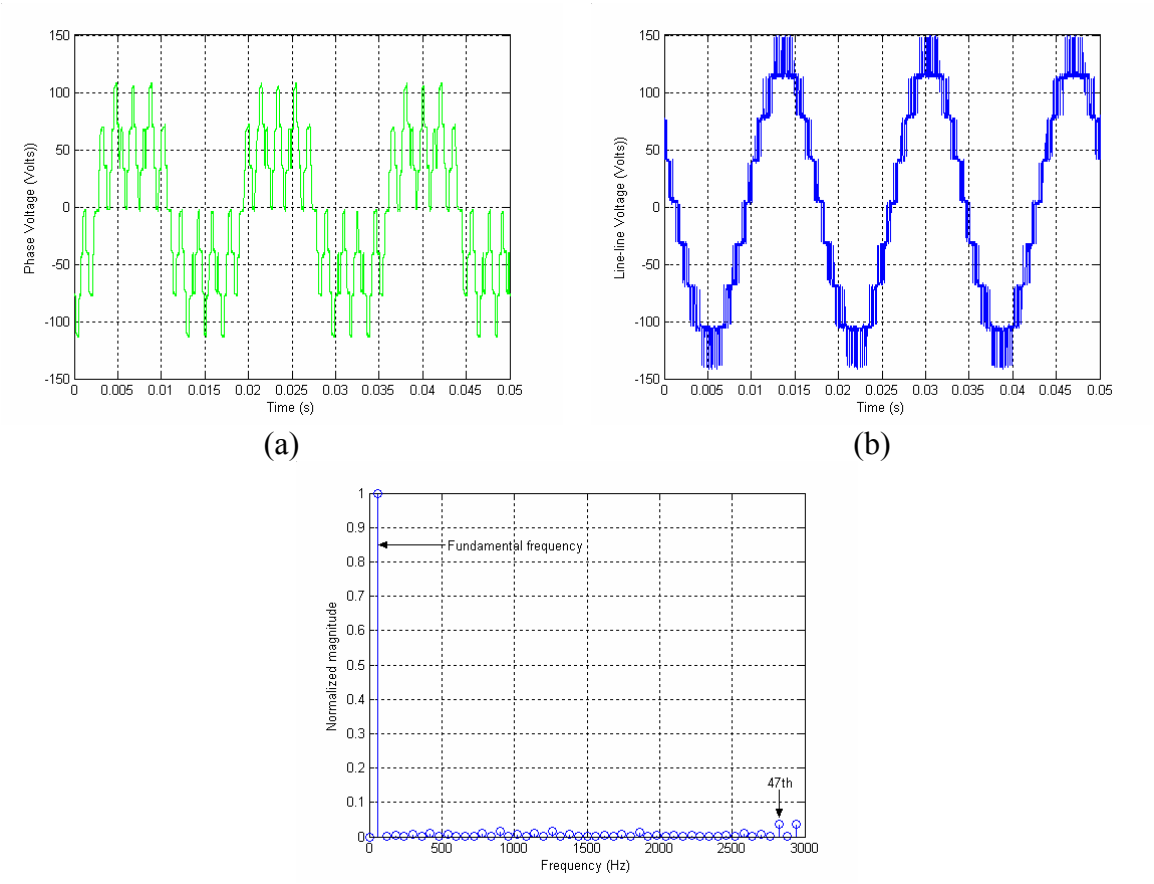


Figure 6.25: Experiment of active harmonic elimination method with unipolar switching scheme (a) phase voltage waveform; (b) line-line voltage; (c) normalized FFT analysis of line-line voltage ($k_1 = 1$, $k_2 = 1$, $k_3 = 1$, $V_{dc} =$ 36V, $m = 1.500$, THD = 5.87%)

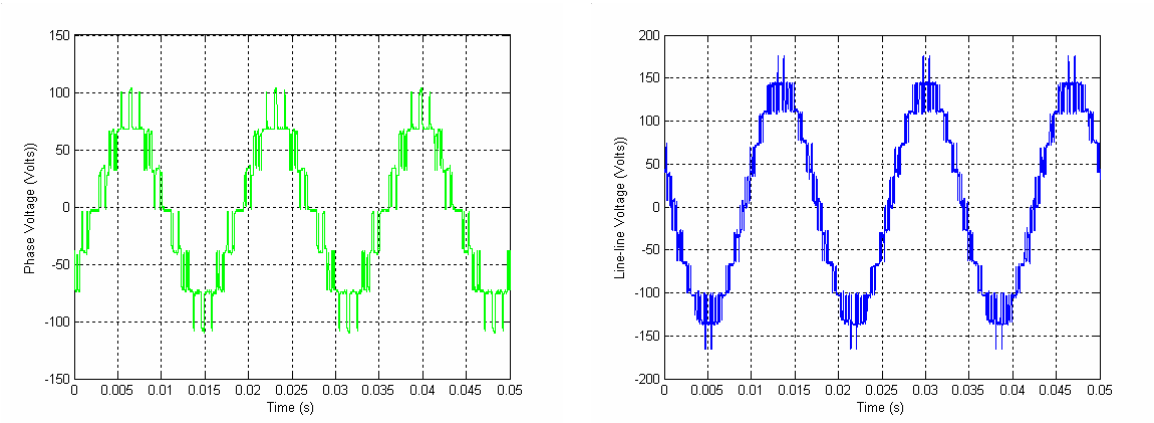


Figure 6.26: Experiment of active harmonic elimination method with unipolar switching scheme (a) phase voltage waveform; (b) line-line voltage; (c) normalized FFT analysis of line-line voltage (k_1 = 0.9, k_2 = 0.95, k_3 = 1, V_{dc} = 38V, m = 1.660, THD = 6.42%)

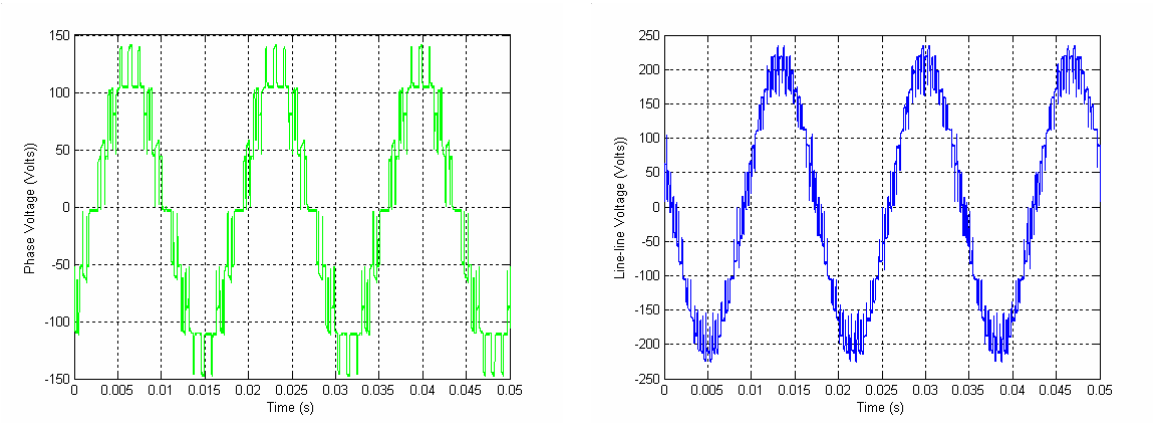


Figure 6.27: Experiment of active harmonic elimination method with unipolar switching scheme (a) phase voltage waveform; (b) line-line voltage; (c) normalized FFT analysis of line-line voltage (k_1 = 0.6, k_2 = 0.8, k_3 = 1, V_{dc} = 60V, m = 1.580, THD = 6.54%)

Table 6.1 THD for optimized active harmonic elimination method

Optimization Case		THD (%)		
		Theory	Simulation	Experiment
Eliminating high order harmonics with the fundamental switching scheme	$m = 3.79$ $V_{dc} = 36$ V	3.15	3.03	3.52
Eliminating harmonics with the unipolar switching scheme	$k_1 = k_2 = 1$ $m = 1.460$ $V_{dc} = 36$ V	14.24	14.1	13.3
	$k_1 = 0.8$ $k_2 = 1$ $V_{dc} = 60$ V $m = 1.120$	19.14	19.13	15.8
	$k_1 = 0.75$ $k_2 = 1$ $V_{dc} = 48$ V $m = 1.080$	19.34	19.19	17.4
	$k_1 = 0.67$ $k_2 = 1$ $V_{dc} = 36$ V $m = 0.960$	20.06	19.87	17.5
	$k_1 = 1$ $k_2 = 1$ $k_3 = 1$ $V_{dc} = 36$ V $m = 1.500$	6.52	6.69	5.87
	$k_1 = 0.9$ $k_2 = 0.95$ $k_3 = 1$ $V_{dc} = 38$ V $m = 1.660$	6.87	6.89	6.42
	$k_1 = 0.6$ $k_2 = 0.8$ $k_3 = 1$ $V_{dc} = 60$ V $m = 1.580$	7.10	7.09	6.54

The computational results show that the optimized active harmonic elimination method with the fundamental frequency switching scheme can reduce the switching frequency from that of the active harmonic elimination method developed in Chapter 4 and still achieve similar THD. The simulation and experiment validate that the optimized active harmonic elimination method can eliminate the harmonics as expected, and the switching frequency is lower than that of the active harmonic elimination method.

This chapter also extended the optimized active harmonic elimination method with the unipolar switching scheme to directly eliminate the specified harmonics with low switching frequency for unequal DC voltage case. The simulation and experiment also confirm this method.

7. Hardware Implementation

The active harmonic elimination method and the optimized active harmonic elimination method have been discussed in the previous chapters.

In this chapter, a controller will be developed to confirm the active harmonic elimination method for practical applications. As digital controllers are the trend for controller implementation, in this thesis work, a digital controller is used to verify the proposed methods.

Personal computers, DSPs and field programmable gate arrays (FPGA) could be used to do digital controller implementation. It is not easy for a personal computer to achieve high real-time control performance because it needs to run a complicated operating system. A DSP system has high real-time control performance but its cost is high. An FPGA system has advantages of high real-time control performance and low cost. For this reason, in this thesis, an FPGA controller is used to implement all of the proposed methods.

7.1. FPGA Controller Implementation

The real-time FPGA controller is based on Altera FLEX 10K FPGA. The block diagram of the controller is shown in Figure 7.1. The switching data are stored in a 12×1024 bits in-chip RAM. The RAM is used to store half cycle data up to a thirteen-level multilevel converter. An oscillator generates a fixed frequency clock signal, and a divider is used to generate the specified control clock signal corresponding to the multilevel converter output frequency. Three phase address generators share a public switching data RAM because they have the same switching data with different phase angles, and the switching data is only for one half cycle because the switching data is symmetric.

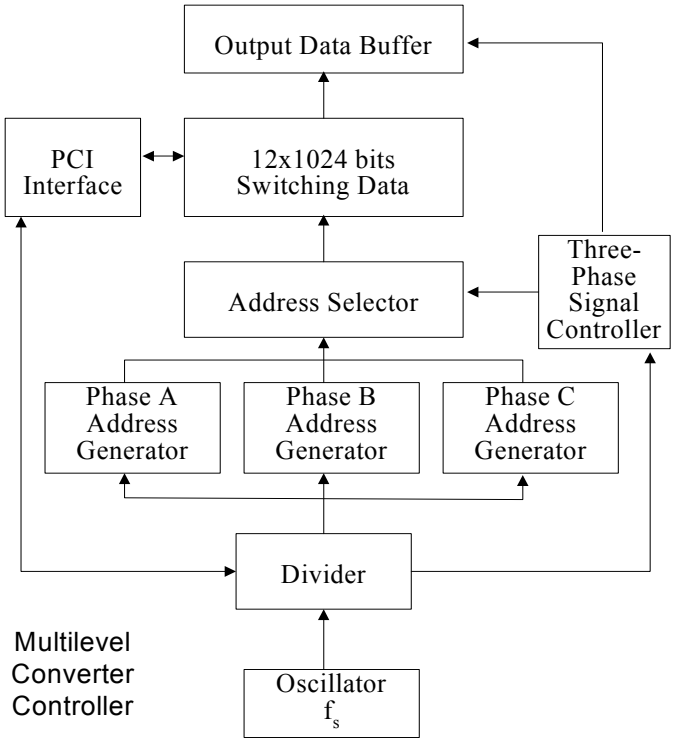


Figure 7.1: Block diagram for FPGA controller

For each step, the three-phase signal controller controls the address selector to fetch the corresponding switching data from the RAM to the output buffer. Assume the oscillator's frequency is f_s, the multilevel converter output frequency is f_0, and there are 2048 steps for each fundamental frequency cycle.

To vary the output fundamental frequency for applications such as motor drive, a divider is used to generate the desired frequency for the three-phase signal controller. The divider number N is:

$$N = f_s /(f_0 \times 2048) \tag{7.1}$$

The control resolution or the step size is:

$$T_s = 1/(f_0 \times 2048) \tag{7.2}$$

If the output frequency f_0 is 60 Hz, the control resolution by (7.2) is 8.138 μs.

For convenience of interfacing with an operator, the FPGA controller is designed as a card that can be plugged into a personal computer, which uses a peripheral component interconnect (PCI) bus to communicate with the personal computer. The whole system block is shown in Figure 7.2.

In this system shown in Figure 7.2, a personal computer is used to interface with the user, compute the switching data, and store the switching data into the RAM of the controller. The control signals are generated by FPGA hardware instead of software to guarantee real-time control performance. The system structure also guarantees low computational load of the microcomputer because it just computes the switching data once for each modulation index *m*, and its computational time cannot disturb the system's control performance.

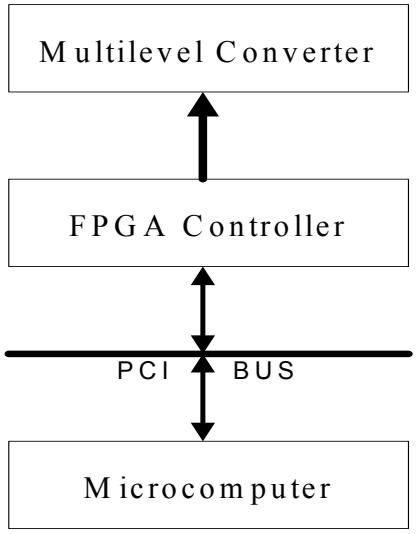


Figure 7.2: System block

A 10 kW prototype three-phase 11-level cascaded H-bridge multilevel converter is used for all the experiments. The multilevel converter is built by using 60 V, 70 A MOSFETs as the switching devices, which is shown in Figure 7.3 (a). The motor used for the experiments and the FPGA card are shown in Figure 7.3 (b) and Figure 7.3 (c), respectively.

All the experiments shown in the previous chapters are done by this FPGA controller.

7.2. Motor Load Experiments

To verify the function of the controller and the multilevel converter as a variable voltage variable frequency motor drive, several experiments have been implemented.

The multilevel converter was attached to a three phase induction motor with the following nameplate data:

Rated Horse Power = 1/2 hp

Rated Current = 1.6 A

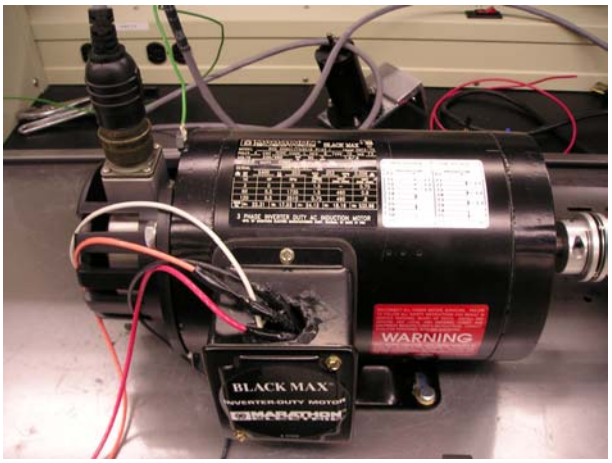
Rated Speed = 1735 rpm

Rated Voltage = 230 V (RMS line-line @ 60Hz)

Figure 7.4 shows four motor phase current waveforms with modulation indices 3.85, 2.06, 1.42, and 1.42 and frequencies 60 Hz, 60 Hz, 30 Hz, and 60 Hz. The experiments show that the controller can vary output voltage and frequency as expected.

It also can be seen from the experiments that three-phase currents are not well balanced. This is because the batteries used for the experiments are 1.2 Ah. The capacity is not very good to run a motor for long time, unbalance of batteries results in the unbalance of phase currents. The unbalance can be eliminated by using high capacity balanced batteries. Although the multilevel converter control methods with unequal DC voltages are proposed in this thesis, they are used for time-invariant unequal DC voltage systems. In the motor experiments, the unequal DC voltages are continuously dropping with time, and the proposed methods cannot be applied to it. Therefore, further research is needed for the time-variant unequal DC voltage systems. This is recommended in the next Chapter.

(a)



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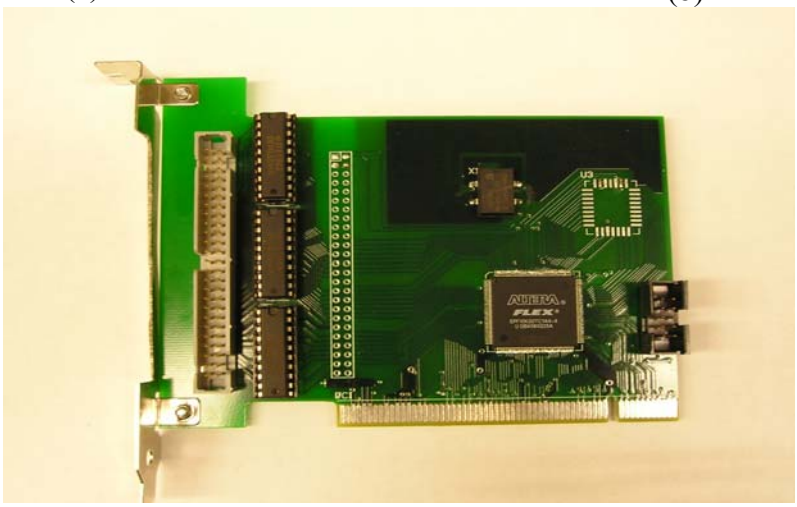
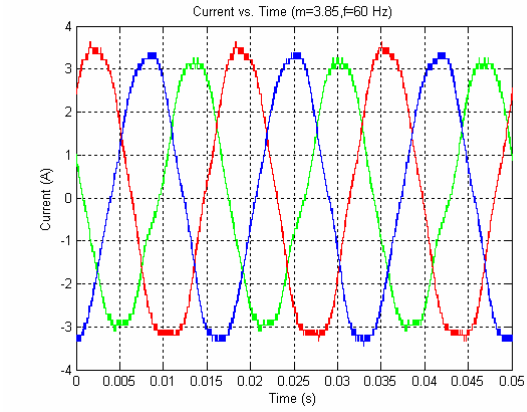
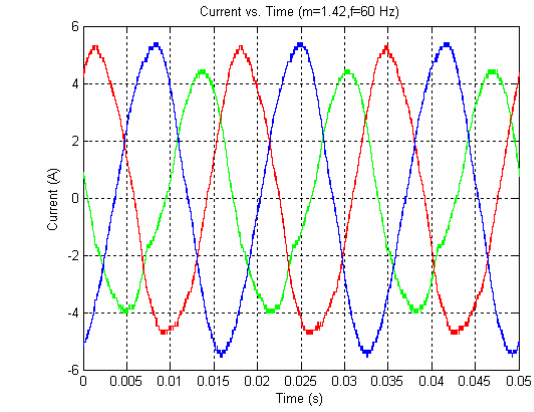


(c)

Figure 7.3: Experiment setup (a) 10 kW H-bridge multilevel converter prototype; (b) induction motor load; (c) FPGA controller board



(a)



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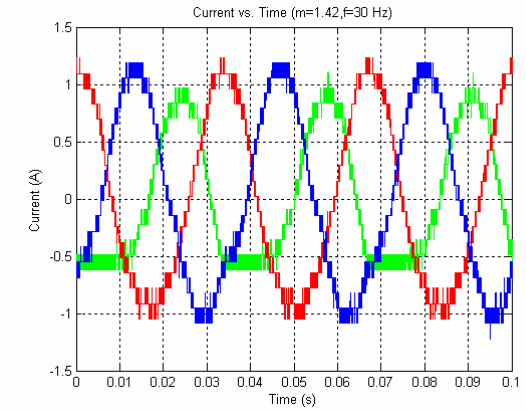
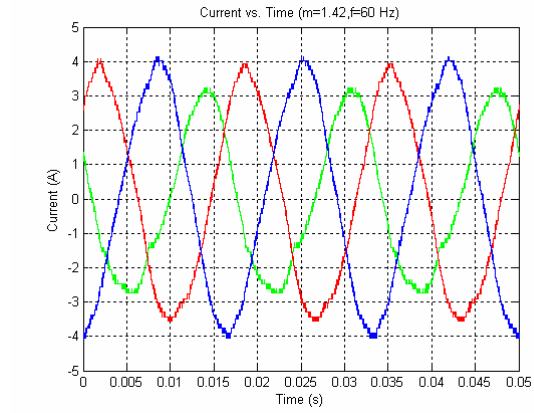


(c)



(d)

Figure 7.4: motor phase current waveforms with different modulation indices and different frequencies (a) $m = 3.85, f = 60$ Hz; (b) $m = 2.06, f = 60$ Hz; (c) $m = 1.42, f = 30$ Hz; (d) $m = 1.42, f = 60$ Hz.

7.3. Summary

This chapter develops a FPGA controller to implement all of the proposed harmonic elimination methods. The FPGA controller also can be used as a practical motor drive controller to control a multilevel converter to output voltages with variable modulation indices and variable frequencies.

All the experiments done in this thesis are implemented with the FPGA controller. Induction motor drive experiments also verified the functions of the controller.

8. Conclusions and Recommendations

8.1. Conclusions

The current trend of modulation control for multilevel converters is to output high quality power with high efficiency. For this reason, popular traditional PWM methods and space vector PWM methods are not the best methods for multilevel converter control due to their high switching frequency. The selective harmonic elimination method has emerged as a promising modulation control method for multilevel converters. But the major difficulty for the selective harmonic elimination method is to solve transcendental equations characterizing harmonics, the solutions are not available for the whole modulation index range, and it does not eliminate any number of specified harmonics to satisfy the application requirements. To conquer the problem for the selective harmonic elimination method, the resultant method is used to find all the solutions to the harmonic equations and the active harmonic elimination method is proposed to eliminate any number of harmonics and can be applied to the whole modulation index range for multilevel converters to satisfy the application requirements.

Generally, if the order of harmonics to be eliminated is low, the resultant method can be used to solve the transcendental equations by converting them into polynomial equations using trigonometric identities. The resultant method can find all the solutions if they exist. But if the order of harmonics to be eliminated is high, the resultant method is not possible for the transcendental equations. The Newton climbing method is proposed to conquer this problem. The Newton climbing method uses the solutions from the resultant method for low order equations as initial guesses to get solutions for high order equations. Although the Newton climbing method does not guarantee to find all the solutions, it works very well to find most of the solutions if the solutions are continuous. To extend the modulation index range for fundamental frequency switching scheme, the triplen harmonic compensation method is proposed. The triplen harmonic compensation

method can extend modulation index range by injecting triplen harmonics. This is shown in Chapter 3.

The active harmonic elimination method is proposed in Chapter 4. The switching angles solved by the resultant method or the Newton climbing method which eliminate low order harmonics can be used to compute magnitudes and phases of high order harmonics. A negative harmonic whose magnitude is equal to the harmonic to be eliminated is generated to cancel the harmonic. By using such a method, an actively generated harmonic can be used to eliminate a harmonic. Therefore, any number of specified harmonics can be eliminated. The number of eliminated harmonics is not limited by unknowns in the harmonic equations or available solutions.

The active harmonic elimination method can be extended to multilevel converters with unequal DC voltages for H-bridge multilevel converters. This is proposed in Chapter 5. To extend the active harmonic elimination method to multilevel converters with unequal DC voltages for H-bridge multilevel converters, first, the H-bridge multilevel converter control is decoupled into control of several bi-level converters with unipolar switching scheme; second, the lowest THD combination of the bi-level converters is searched; then the active harmonic elimination method is used to eliminate the specified harmonics.

The active harmonic elimination method can be optimized to decrease the switching frequency. This is proposed in Chapter 6. The first optimization method is to reverse the order of harmonic elimination. High order harmonics can be eliminated by solving harmonic equations, and low order harmonics can be eliminated by active harmonic elimination method. This optimization method can dramatically decrease the switching frequency. It has the advantage of easy computation, and can also be applied to multilevel converter with unequal DC voltages. The second optimization method is to search for low harmonic distortion combinations, and use the corresponding angles as initial guesses for the Newton climbing method by decoupling the multilevel converter control into control of several unipolar converters. The second method has lower switching frequency than that of the first optimization method. But solutions to the

second optimization method just can be found in part of the modulation index range while the first optimization method can be applied to the whole modulation index range.

To experimentally confirm the proposed harmonic elimination methods, a FPGA controller is proposed and developed. All of the proposed harmonic elimination methods are validated by experiments with the FPGA controller and a 10 kW H-bridge multilevel converter prototype. The FPGA controller can also be used as a motor drive controller to output three-phase variable modulation index voltages with variable frequencies. This is also confirmed by experiments.

8.2. Contributions

For this thesis work, the contributions made to the existing body of knowledge can be summarized as follows.

1. The resultant method is used to solve transcendental equations to eliminate low order harmonics. The resultant method can find all the solutions if they exist. Therefore, the lowest THD solution can be used for practical application for the best control performance.
2. The Newton climbing method is proposed for high order harmonic elimination. This method uses solutions from the resultant method as initial guesses for high order harmonic elimination and has fast convergence if a solution exists.
3. The triplen harmonic compensation method is proposed to extend the modulation index range for the fundamental frequency switching scheme by injecting triplen harmonics.
4. The active harmonic elimination method is proposed to eliminate any number of harmonics. This method eliminates harmonics by generating negative harmonics with switching angles from the resultant method or the Newton climbing method.
5. The active harmonic elimination method with unequal DC voltages is proposed, which is an extension of the active harmonic elimination method. This method decouples a cascaded H-bridge multilevel converter control into control of several bi-level converters with unipolar switching scheme, and eliminates any number of specified harmonics.

6. The optimized active harmonic elimination method is proposed to decrease the switching frequency for the active harmonic elimination method. The first optimization method is to eliminate high order harmonics using the fundamental frequency switching scheme or unipolor switching scheme, and to eliminate low order harmonics with the active harmonic elimination method. This method can be applied to the whole modulation index range and extended to unequal DC voltage cases. The second optimization method is to search for a low harmonic distortion combination, and use the corresponding angles as initial guess for the Newton climbing method. This method can also be extended to unequal DC voltage cases, but it is limited by the available solutions.
7. An FPGA controller is proposed and developed to experimentally validate all of the proposed harmonic elimination method with a 10 kW H-bridge multilevel converter. The FPGA controller is also developed as a variable voltage variable frequency motor drive controller and verified by three-phase induction motor experiments.

8.3. Recommendations for Future Work

This thesis work focuses on harmonic elimination for multilevel converters with a preset switching scheme. The major difficulty is to solve the transcendental equation for harmonic contents. The resultant method can solve low order harmonic equations, but cannot solve high order harmonic equations. The Newton climbing method does not guarantee to find all the solutions. Therefore, significant research work is required to find high efficiency, low cost algorithm to solve the high order harmonic equations.

The optimized active harmonic elimination method with the fundamental frequency switching scheme and the unipolar switching scheme has higher switching frequency and wider modulation index range than that of the optimized active harmonic elimination method using the Newton climbing method to directly search for the switching angles. The solutions to the second optimized active harmonic elimination method just exist in a limited range, especially for unequal DC voltage cases. It is recommended here to propose new algorithms to further decrease the switching

frequency for the first optimized active harmonic elimination method and to extend the modulation index range for the second optimized active harmonic elimination method.

In this thesis, switching angles for each bi-level converter are equal. If the switching angle numbers for each bi-level converter are not equal, it may be possible to find more solutions for a wider modulation index range. It is here recommended to propose new algorithms to eliminate harmonics with unequal switching angles for different bi-level converters.

In this thesis, switching scheme for the active harmonic elimination method with unequal DC voltages and the optimized active harmonic elimination method is 5-angle unipolar switching scheme. For practical applications, other switching scheme can also be used for computation. It is recommended to use several switching schemes for computation and choose the optimal one for practical systems.

All the proposed methods in this thesis are for time-invariant systems. This assumes all the equal or unequal voltages will not change with time. However, the voltages for practical systems will change with time. For example, in the motor experiments of the thesis, the voltages of the batteries are changing with time. Therefore, it is recommended to propose new real-time algorithms to eliminate harmonics for time-variant systems.

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Vita

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