5-2006

Materials Integration and Device Fabrication of Active Matrix Thin Film Transistor Arrays for Intracellular Gene Delivery

Seung-Ik Jun
University of Tennessee - Knoxville

To the Graduate Council:

I am submitting herewith a dissertation written by Seung-Ik Jun entitled "*Materials Integration and Device Fabrication of Active Matrix Thin Film Transistor Arrays for Intracellular Gene Delivery*." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Materials Science and Engineering.

Philip D. Rack, Major Professor

We have read this dissertation and recommend its acceptance:

Michael L. Simpson, David C. Joy, Thomas T. Meek

Accepted for the Council:

Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

To the Graduate Council:

I am submitting herewith a dissertation written by Seung-Ik Jun entitled *"Materials Integration and Device Fabrication of Active Matrix Thin Film Transistor Arrays for Intracellular Gene Delivery."* I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Materials Science and Engineering.

Philip D. Rack

Major Professor

We have read this dissertation and recommend its acceptance:

Michael L. Simpson

David C. Joy

Thomas T. Meek

Accepted for the Council:

Anne Mayhew

Vice Chancellor and
Dean of Graduate Studies

(Original signatures are on file with official student records.)

Materials Integration and Device Fabrication of Active Matrix Thin Film Transistor Arrays for Intracellular Gene Delivery

A Dissertation Presented for the

Doctor of Philosophy Degree

The University of Tennessee, Knoxville

Seung-Ik Jun

May 2006

Dedication

I would like to dedicate this Doctoral dissertation to my wife, Gun-Myong, whose unending support and encouragement during the course of my graduate study. There is no doubt in my mind that without her continued support I could not have completed this process. I also want to dedicate this work to my parents and parents-in-law, Jong-Hyub Jun, Byung-Lim Min, Noh-Hwan Park, and Kwi-Nam Lee for their continuous love and support throughout my study. Dedication is also to my daughter, Erin, making me more joyful since her birth.

Acknowledgements

I owe thanks to many people, whose assistance was indispensable in completing this study. First among them is Dr. Philip D. Rack, advisor and committee chair, for his thoroughness and deep scientific perspective in advising my work in progress. The members of my dissertation committee, Dr. Michael L. Simpson, Dr. David C. Joy, and Dr. Thomas T. Meek, have generously given their time and expertise to better my work. I am very appreciative of their contribution and their valuable support for me. I would like to thank the members of our research group in the University of Tennessee and Oak Ridge National Laboratory, Dr. Jason Fowlkes, Dr. Steven Randolph, Dr. Yuepeng Deng, Daryl Smith, Ryan Rucker, Jung-Won Park, Timothy McKnight, Dr. Anatoli Melechko, Kate Klein, Dr. Laura Edwards, Dale Hensley, Darrell Thomas, and Richard Kasica for whose help and support I am greatly appreciative. Without their efforts, this work would not be possible. Finally, I am especially grateful for the support and guidance from my undergraduate and graduate advisors in Korea, Dr. Sung-Sik Kim and Dr. Duck-Kyun Choi.

Abstract

Materials and process integration of a thin film transistor array for intra/extracellular probing are described in this study. A combinatorial rf magnetron sputter deposition technique was employed to investigate the electrical characteristics and micro-structural properties of molybdenum tungsten (MoW) high temperature electrodes as a function of the binary composition. In addition to the composition, the effect of substrate bias and temperature was investigated. The electrical resistivity of MoW samples deposited at room temperature with zero bias followed the typical Nordheim's rule as a function of composition. The resistivity of samples deposited with substrate bias is uniformly lower and obeyed the rule of mixtures as a function of composition. The metastable β-W phase was not observed in the biased films even when deposited at room temperature. High resolution scanning electron microscopy revealed a more dense structure for the biased films, which correlated to the significantly lower film resistivity.

In order to overcome deficiencies in sputtered silicon dioxide (SiO_2) films the rf magnetron sputtering process was optimized by using a full factorial design of experiment (DOE). The optimized SiO_2 film has a 5.7 MV/cm breakdown field and a 6.2 nm/min deposition rate at 10 W/cm^2 RF power, 3 mTorr pressure, 300 °C substrate temperature, and 56 V substrate bias. Thin film transistors (TFTs) were also fabricated and characterized to show the prospective applications of the optimized SiO_2 films.

The effect that direct current (DC) substrate bias has on radio frequency (RF)-sputter-deposited amorphous silicon (a-Si) films was also investigated. The substrate

bias produces a denser a-Si film with fewer defects compared to unbiased films. The reduced number of defects results in a higher resistivity because defect-mediated conduction paths are reduced. Thin film transistors (TFT) that were completely sputter-deposited were fabricated and characterized. The TFT with the biased a-Si film showed lower leakage (off-state) current, higher on/off current ratio, and higher transconductance (field effect mobility) than the TFT with the unbiased a-Si film.

The crystallization properties of amorphous silicon (a-Si) thin film deposited by rf magnetron sputter deposition with substrate bias have been thoroughly characterized. The crystallization speed can be increased and the crystallization temperature can be drastically lowered relative to unbiased a-Si even though the stress state of biased a-Si film is highly compressive. The substrate bias enhances defect formation (vacancies, dislocations, stacking faults) via ion bombardment during the film growth, which effectively increases the driving force for crystallization of the films.

The electrical and optical properties of sputter-deposited silicon nitride (SiN_x) and n^+ amorphous silicon (n^+ a-Si) films as a function of substrate bias during sputter deposition were investigated. The breakdown voltage of sputter-deposited SiN_x with 20 W (125 V) substrate bias is 7.65 MV/cm which is equivalent to that of plasma enhanced chemical vapor deposition (PECVD) SiN_x films. The conductivity of n^+ a-Si films are also enhanced by applying substrate bias during the sputter deposition. To verify the effect of substrate bias, amorphous silicon thin film transistors (TFTs) were fabricated with substrate biased thin films and compared their electrical properties with conventional sputter deposited TFTs.

Lastly, electrochemical measurements were analyzed using gold and pyrrole solution to verify the active addressability of the TFT array fabricated by entirely by sputter deposited thin films below 200 °C temperature.

Table of Contents

List of Tables

List of Figures

Chapter 1 Introduction

1.1 Microelectrode array (MEA) for extra/intracellular cell probing

1.1.1 Definition and application of Microelectrode arrays (MEA)

Microelectrode arrays (MEA) have been studied to investigate electrogenic cells and tissues by intra/extracellular stimulating and recording.[1] A microelectrode array (MEA) is an arrangement of typically more than a few tens of electrodes with 100 ~ 500 μm pitch allowing the probing of several sites for cell stimulation and extracellular recording at once (Fig. 1-1).[1] An extracellular recording system is composed of following components; signal source (cells or tissue), cell-sensor interface (biocompatible electrolyte), biosensor (MEA), filter amplifier, and recording hardware and software. In these days, the devices are fabricated by conventional semiconductor fabrication processes (thin film deposition, lithography, and wet / dry chemical etching) with a high density of electrodes.

The cell membrane is semi-permeable and is separated by different ion concentrations (charges) on the inner and outer side of the membrane. The cell membrane, therefore, has the electrical properties like a plate capacitor. The electrochemical gradient due to the concentration difference induces a membrane potential that can be measured directly by an intracellular (or extracellular) electrode. When ion channels are opened due to chemical or electrical stimulation, the resultant ions

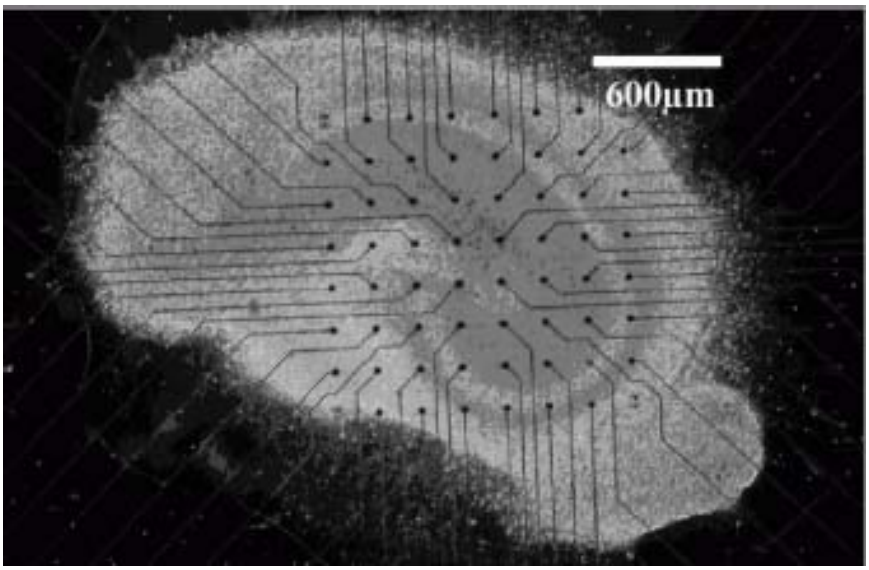


FIG. 1-1. Micrograph of a microelectrode array (MEA). Only the cells on the electrodes can be measured and the cells lying on between the electrodes are not analyzed.

V. Bucher, B. Brunner, C. Leibrock et al., Biosensors & Bioelectronics 16 (3), 205 (2001).

are moved along the electrochemical gradient. In other words, the resistance of the membrane is lowered, resulting in an inward or outward flow of ions measured as a trans-membrane current.

In the case of extracellular probing, the space between signal source (cells or tissue) and electrode is also conductive and the extracellular current results in a small voltage that can be measured with extracellular electrodes and reference electrode according to Ohm's law ($V = I \times R$, where V is voltage, R is resistance, and I is current). Extracellular signals are smaller than trans-membrane potentials measured by intracellular probing and the potential depends on the distance between the signal source and the extracellular electrode. Due to resistance properties of the extracellular space, the level of extracellular signal decreases with increasing distance of the signal source to the electrode. Therefore, a high spatial resolution of the electrode array corresponding to high electrode density and/or a close interface between electrode and cell membrane is a very important factor to get a high signal-to-noise (S/N) ratio.[2]

Over the past decades, non-invasive extracellular recording devices using multiple electrodes has been developed using standard microelectronic fabrication processes. Systems and methods have been greatly improved, leading to more features, lower costs, and higher throughput. Almost all excitable or electrogenic cells and tissues can be used for extracellular recording in vitro, for example, central or peripheral neurons, heart cells, retina, or muscle cells.[3,4,5]

MEAs can be used to inspect the activities of whole cells and tissues rather than simple single cell measurements and can measure the interaction of several cells in a

culture or in their natural environment or even in whole organs. The rising applications of monitoring biological signals generated during nerve excitation, quantitative release of molecules, and cell-to-cell communication has stimulated the development of new methodologies and materials for novel applications of bio-applicable devices in basic science, laboratory analysis and therapeutic treatments.[5]

The classical methods need complex and expensive micro-processes for electrode positioning, which are limited to 2 or 3 units per recording cells and produce inevitably serious damage to the interior of cell that limits the duration of the recording and reproductivity of the recording over the same cell. Solid-state microelectrode arrays overcome many of these drawbacks and allow several of the following advantages: 1) recording electrical signals with higher fidelity signal-to-noise ratios without destroying the intracellular domain, 2) monitoring simultaneously the activity of various cells belonging to a complex network, 3) repeating periodically the recordings on the same cells over long periods of time.

However, the main drawback of the MEA is that the only cells lying on the electrodes can be measured and the cells outside of the electrodes cannot be analyzed due to the still relatively low electrode density relative to the size of the cells. In addition, cells usually do not adhere exactly on the electrodes and cell-electrode contact is often very poor in this device. As a consequence, the signal to noise ratio is not optimized and often the signal is not detected properly.

1.1.2 Light-addressed extracellular probing device

To overcome the low electrode density of MEAs, V. Bucher *et al.* proposed an array of light-addressable sub-μm electrodes.[6,7] Each electrode, as shown in Fig. 1-2, can be addressed individually by switching a photoconductor layer by means of a focused laser beam. The array provides a great number of electrodes on a photoconductor layer (hydrogenated amorphous silicon). Each electrode in the device is operated under the illumination of laser light with 488 nm wavelength and the current can be induced to the electrode stimulating cells.

Although having higher density of electrode, it has several disadvantages due to in driving scheme. Firstly, the device needs additional equipment on the periphery to be driven due to its passive-addressed driving scheme; for instance a laser source, amplifier, addressing tools, and mounting tools.

Secondly, it is so hard to focus at a specific electrode to stimulate a cell because mechanical addressing to focus at a coordinate cannot be precisely controlled. The failure of a precise focus makes cross-talking and addressing delays a problem in the whole active area. To simplify the driving scheme while maintaining the high electrode density, we propose an active addressed microelectrode array using thin film transistors.

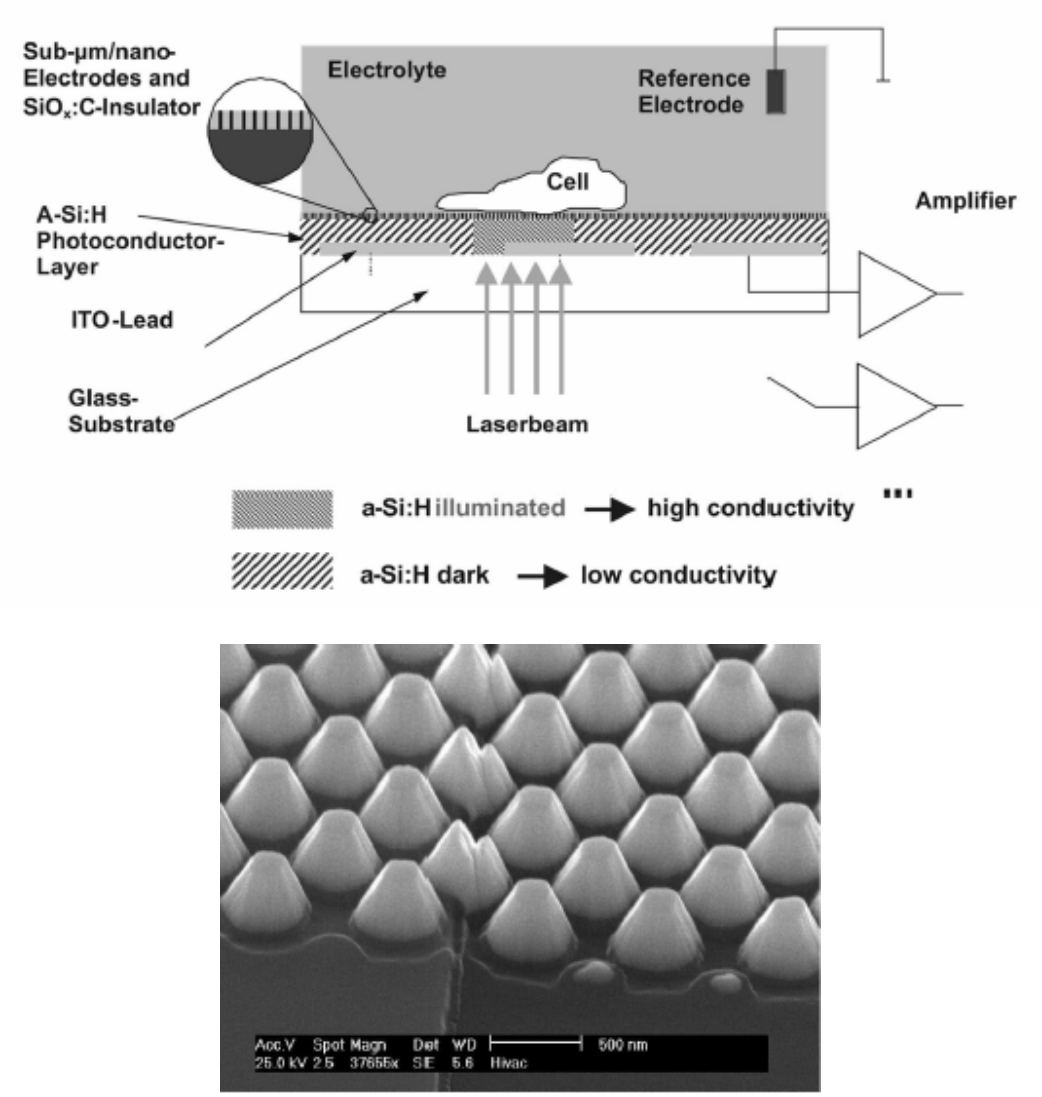


FIG. 1-2. Principle of light-addressed sub-µm contacting of excitable cells. Electrodes over the illuminated photoconductor are switched through.

V. Bucher, J. Brugger, D. Kern et al., Microelectronic Engineering 61-62, 971 (2002).

1.2 Active matrix addressing and Thin film transistor (TFT)

1.2.1 Definition of passive and active matrix addressing

The passive addressing is a scheme that the charge of a unit cell (pixel) is maintained by directly applied voltage on the row and column electrodes. Even though this has a very simple driving scheme and structure, it requires high driving voltages and complex peripheral devices relative to an active addressing scheme due to its inability to maintain charge on other pixel elements that are not simultaneously addressed.

For the active matrix addressing scheme, as shown in Fig. 1-3, each unit cell is attached to a switching device (TFT, Field effect transistor or FET) which actively maintains the cell state while other cells are being addressed. This scheme also prevents crosstalk from inadvertently changing the state of an unaddressed pixel. The active addressing scheme is usually used in the fabrication of flat panel display devices such as thin film transistor-liquid crystal displays (TFT-LCD) and TFT-organic electroluminescence display (TFT-OELD).

1.2.2 Amorphous silicon TFT and parameter extraction

Thin film transistors (TFTs) were proposed by Weimer in 1961.[8] The semiconducting layer and gate dielectric of the TFT were made of cadmium sulfide and

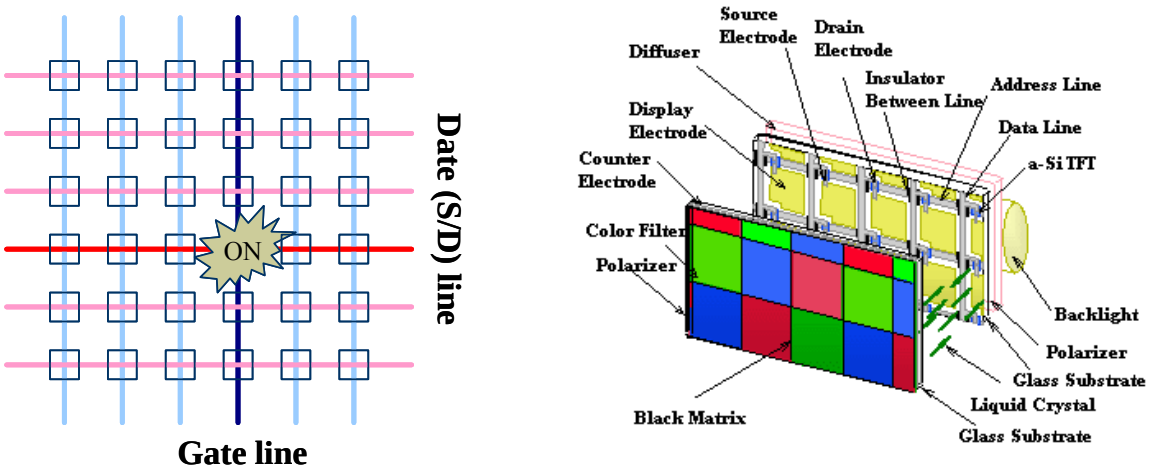


FIG. 1-3. Active matrix addressing scheme and one example of applications. Thin film transistor - liquid crystal display (TFT-LCD).

silicon monoxide by conventional evaporation. Soon after this, various semiconducting materials have been studied for example Cadmium Selenide (CdSe).

Hydrogenated amorphous silicon thin film transistors (a-Si:H TFTs) were initially proposed by LeComber as electronic switching devices in 1979.[9,10,11] It has been demonstrated that TFTs are effective driving and read-out devices in the microelectronic applications such as liquid crystal displays (LCDs) [12,13], optoelectronic sensors [14], and chemical/biological sensors.[15,16] Recently novel devices such as the radiation sensors [17], medical imaging sensors (Digital X-ray detector) [18,19], and MEMS (Micro Electro Mechanical Systems) [20] have been successfully fabricated on the basis of TFT technologies. Additionally, chemical and biological sensing devices driven by TFTs are currently being studied throughout the world.[15]

Fig. 1-4 shows various cross-sectional TFT structures. The staggered and inverted-staggered structures are used in a-Si:H TFTs. The inverted-staggered structure is more popular than the staggered structure because of the lower interfacial density of states between the gate dielectric and a-Si:H films.[21] An inverted-staggered TFT is usually fabricated with following mask steps; gate, active region, source/drain, and via hole. As shown in Fig. 1-4, electrons injected from the source electrode cross the a-Si:H layer, travel through the channel at the interface between the gate dielectric and a-Si:H, cross the a-Si:H layer again, and reach the drain electrode. Since the channel thickness is estimated to be several tens of nanometers, the interface properties between gate dielectric and a-Si:H play a critical role in TFT characteristics.[22]

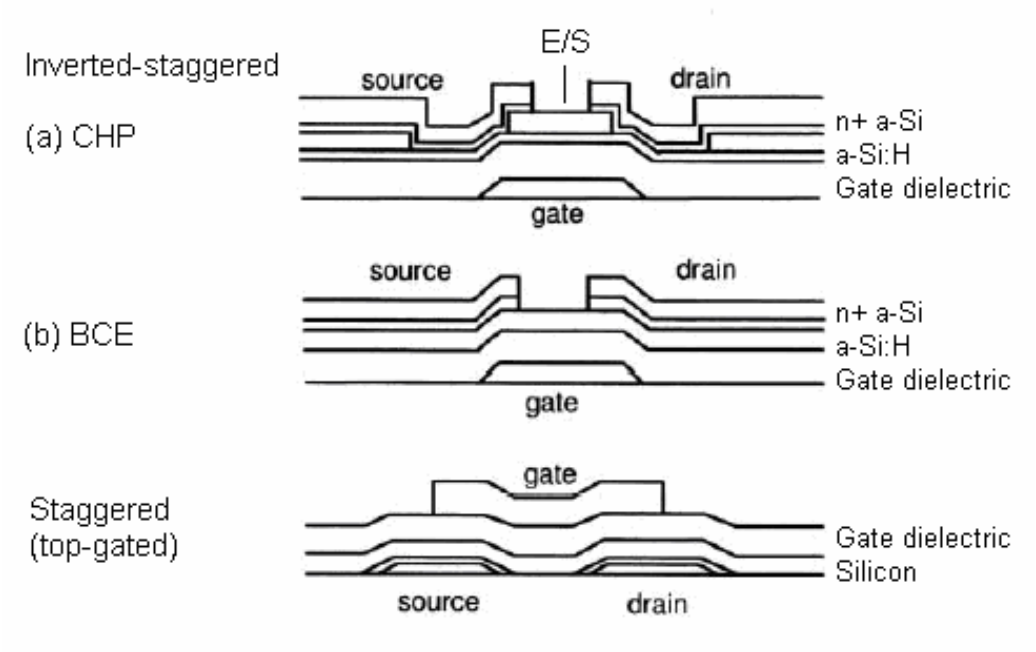


FIG. 1-4. Various cross-sectional structures of TFT. (a) Channel-passivated (CHP), (b) back-channel etched (BCE), and staggered (top-gated) TFTs.

Kuo Yue, Journal of the Electrochemical Society 142 (1), 186 (1995).

The basic current-voltage characteristics of a TFT can be analyzed in a similar fashion compared to a metal-oxide-semiconductor field effect transistor (MOSFET) and polycrystalline devices. The following assumptions are defined for the formulation; (1) the carrier mobility in the channel is constant, (2) the gate capacitance is constant and independent of the gate voltage, (3) the source and drain electrodes are electrically ohmic contacts to the semiconductor, (4) the initial charge density in the semiconductor is n_0, and (5) the gradual cannel approximation can be applied. The gradual channel approximation means that the transverse field in the channel is greater than the longitudinal field (E_x). To define TFT parameters, a coplanar TFT structure shown in Fig. 1-5 is used for the analysis. The coplanar structure is not common in a-Si:H TFT but this structure illustrates well how the TFT characteristics are extracted using this simple configuration.[23,24]

The application of a gate voltage V_g induces charge density $\Delta n(x)$ in channel region. This is given by;

$$e\Delta n(x) = \left(\frac{C_i}{t}\right)\left[V_g - V(x)\right]$$

where C_i is the gate capacitance per unit area ($=\varepsilon_i/d$), t is the a-Si:H thickness, d is the gate insulator thickness, and $V(x)$ is the drain voltage at distance x from the source. If the thickness t is assumed to be sufficiently small, the drain current I_d is given by

$$I_d = tW\left[\sigma_0 + \Delta\sigma(x)\right]E_x = tWe\mu_n\left[n_0 + \Delta n(x)\right]E_x$$

where σ_0 and $\Delta\sigma(x)$ are initial conductivity and incremental conductivity from $\Delta n(x)$, respectively. From combining above two equations, I_d is given by

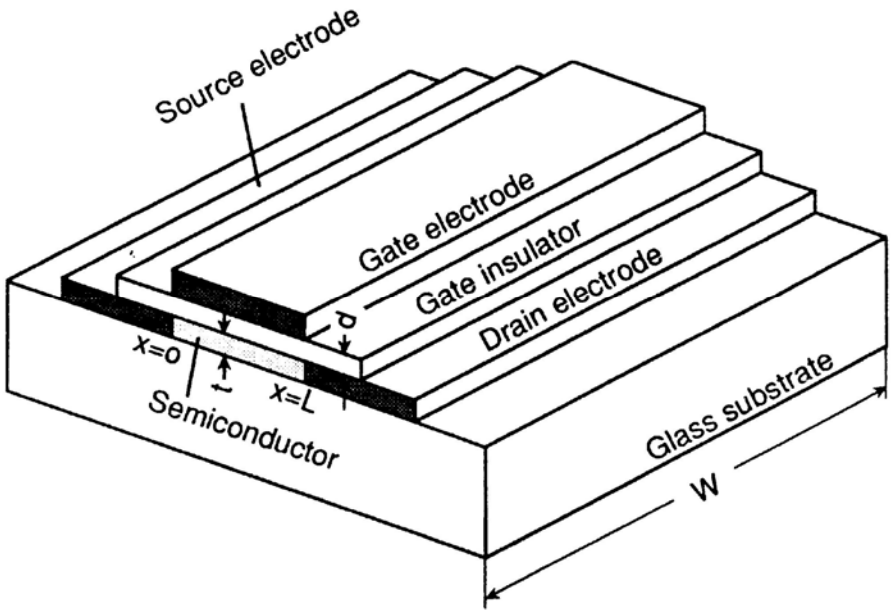


FIG. 1-5. The coplanar TFT structure used for electrical characterization. In a-Si:H TFTs, the staggered electrode configuration is generally adopted. Therefore, the analytical model is different from the actual device characteristics. However, the current-voltage characteristics from this device model can be described well by the analytical results obtained using this model.

Toshihisa Tsukada, "TFT/LCD: Liquid Crystal Displays Addressed by Thin-film Transistors-Japanese Technology Review," 29 (1996)

$$I_d = W\mu_n C_i \left[\left(\frac{etn_o}{C_i} \right) + V_g - V(x) \right] \left(\frac{dV(x)}{dx} \right)$$

$$I_d \int_0^L dx = W\mu_n C_i \int_0^{V_d} \left[\left(\frac{etn_0}{C_i} \right) + V_g - V(x) \right] dV(x)$$

Then, drain current is given by

$$I_d = \mu_n C_i \left(\frac{W}{L} \right) \left[(V_g - V_t) V_d - \left(\frac{{V_d}^2}{2} \right) \right]$$

where $V_t \approx -etn_0/C_i$. The threshold voltage V_t depends on the initial charge density n_0. This equation is valid for a voltage range of $0 \leq V_d \leq V_g - V_t$. Beyond this range, the current is assumed to be constant as in insulated-gate field effect transistor. Low V_d values correspond to the region of linear output characteristics where the drain conductance, g_d, and the transconductance, g_m, are given by

$$g_d = \frac{\partial I_d}{\partial V_d}\Big|_{V_d \to 0} = \mu_n C_i \left(\frac{W}{L} \right) (V_g - V_t)$$

$$g_m = \frac{\partial I_d}{\partial V_g} = \mu_n C_i \left(\frac{W}{L} \right) V_d$$

The drain conductance is a linear function of V_g, and the transconductance is proportional to V_d. Saturation of the drain current occurs when $\partial I_d/\partial V_d = 0$, due to pinch-off of the conducting channel in the region near the drain. In this case, the saturation current, I_{dsat}, is given by

$$I_{dsat} = \left(\frac{1}{2} \right) \mu_n C_i \left(\frac{W}{L} \right) (V_g - V_t)^2$$

For $V_d \geq V_g - V_t$, the transconductance in the saturation region is given by

$$g_m = \mu_n C_i \left(\frac{W}{L}\right)(V_g - V_t) = \left[2\mu_n C_i \left(\frac{W}{L}\right) I_{dsat}\right]^{1/2}$$

The typical operating scheme of a-Si TFT is shown in Fig. 1-6. TFT usually operates in the range of 20 ± 2 V for ON state and -5 ± 2 V for OFF state. The on/off current ratio is generally defined as the current ratio of the ON and OFF state.

1.3 Vertically aligned carbon nanofibers (VACNFs)

1.3.1 Definition and overview of VACNF

Carbon nanofibers (CNFs) can be defined as cylindrical or conical structures with diameters from a few to hundreds of nanometers and lengths ranging from less than a micron to millimeters. Fig. 1-7 (a) shows a graphene structure with covalently bonded carbon atoms arranged in a hexagonal network. There are two types of carbon nanostructures according to the angle between the fiber axis and the graphene sheet near the sidewall surface; stacked cone structure nanofiber and nanotube; Fig. 1-7 (a) and (b) respectively.[25,26]

Fig. 1-8 shows tunneling electron microscopy (TEM) image of carbon nanofiber and carbon nanotubes grown by direct current catalytic plasma enhanced chemical vapor deposition (DC C-PECVD); (a) with Ni catalyst, and (b) bamboo-type carbon nanofiber with Fe catalyst; (c) bundles of single-walled carbon nanotubes.

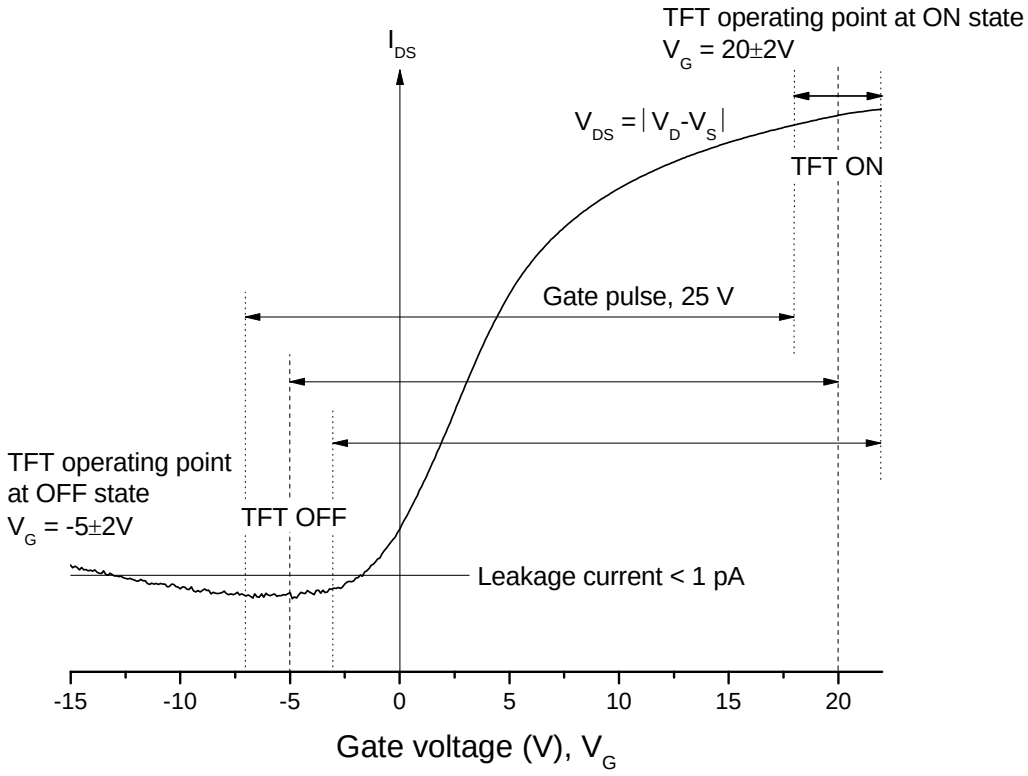


FIG. 1-6. Typical operating scheme of a-Si TFT.

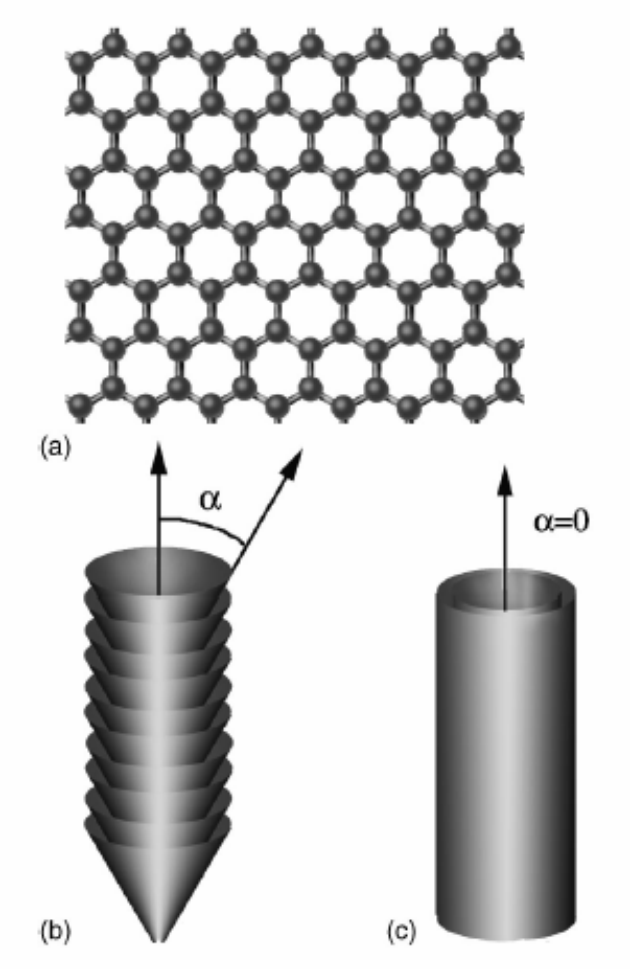


FIG. 1-7. Schematic diagrams of carbon nanofiber and nanotube. (a) Graphene layer, (b) stacked cone nanofiber, and (c) nanotube.

M. Endo, Y. A. Kim, T. Hayashi et al., Applied Physics Letters 80 (7), 1267 (2002).

A. Krishnan, E. Dujardin, M. M. J. Treacy et al., Nature 388 (6641), 451 (1997).

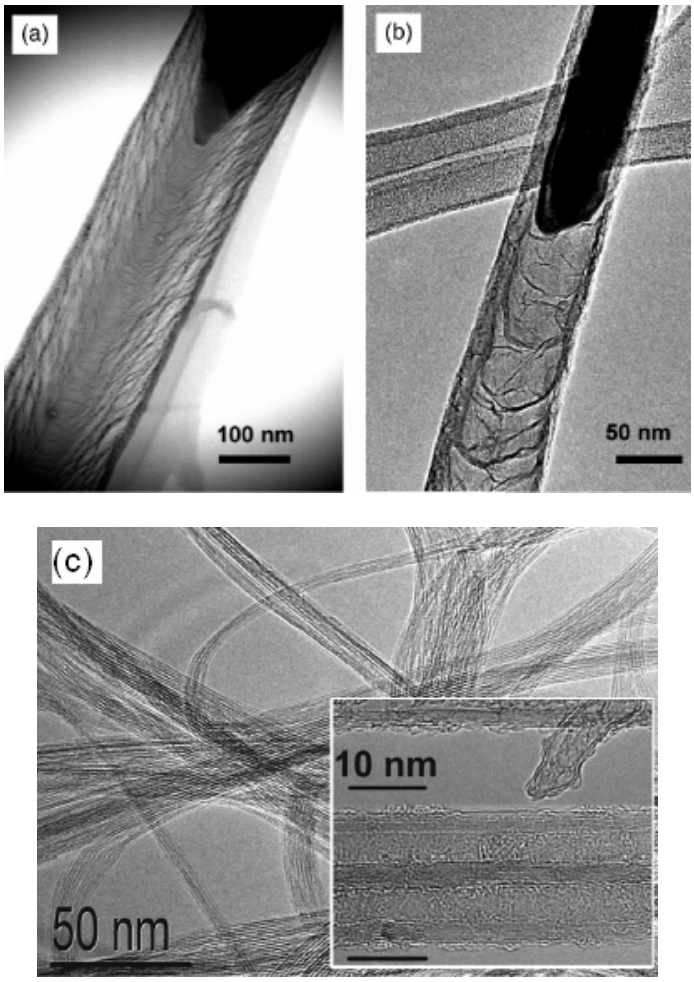


FIG. 1-8. STEM image of a carbon nanofiber grown by DC C-PECVD. (a) With Ni catalyst, (b) a bamboo-type carbon nanofiber grown with Fe catalyst, and (c) bundles of single-walled carbon nanotubes.

A. V. Melechko, V. I. Merkulov, T. E. McKnight et al., Journal of Applied Physics 97 (4), 41301 (2005).

1.3.2 Synthesis process and growth mechanism of catalytic thermal chemical vapor deposition

There are several methods for synthesizing carbon nanostructures; laser evaporated deposition,[27] arc discharge,[28,29] catalytic chemical vapor deposition (C-CVD), and catalytic plasma enhanced chemical vapor deposition (C-PECVD). In the case of laser ablation and arc discharge deposition, although they have several advantages of being high quality nanotube materials with high efficiency, controlling spatial arrangement of nanostructures is intractable using these deposition technologies. In addition to this drawback, extra purification processes are needed to remove amorphous carbon particles for highly purified materials. On the other hand, C-CVD and C-PECVD allow the controlled deterministic synthesis to achieve a specific location, alignment, size, shape, structure of individual carbon nanofibers.

In using conventional CVD, there are process sequence steps to deposit a condensed phase on substrate; desorption, evolution, and incorporation of vapor species on substrate. The conventional CVD deposition occurs by heat flux at high temperature, 400 to 1000 °C. C-CVD uses a catalyst in the decomposition of vapor species on the catalyst surface and somewhat differs from the conventional CVD.[30] There are two methods to introduce the catalyst onto the substrate; supported and floating catalyst. The supported catalyst is deposited onto the substrate directly and the floating catalyst is formed by flowing a reactive gas.[31,32] Carbon nanostructures have been successfully

synthesized by C-CVD and recently it has been used to successfully grow multi-walled carbon nanotubes (MWCNTs) [33] and single-walled carbon nanotubes (SWCNTs).[32]

The growth mechanism of carbon nanofibers has been widely studied by many researchers. Baker *et al.* showed small amount of metal particles generate carbon nanofibers during the decomposition of acetylene.[34] They used *in situ* electron microscopy to take images of the growth sequence and measured the growth rate to determine the kinetic parameters involved in the process. They conclude that the growth mechanism follows these steps (Fig. 1-9): (1) adsorption and decomposition of the reactive hydrocarbon molecule on the surface of catalyst, (2) dissolution and diffusion of carbon species through and around the metal particles, and (3) precipitation of carbon on the reverse surface of the catalyst particles to structure the nanofibers. In the step (3), the precipitation occurs on the bottom surface of the catalyst particle and then the particles are lifted up toward top of the carbon nanofiber remaining crystalline graphite. At the first stage of the study, the temperature gradient was regarded as the dominant kinetic factor of carbon diffusion through the catalyst due to exothermic reaction of decomposition on the catalyst surface.[34] Later, it turned out that the dominant driving force for diffusion of carbon into the catalyst is the concentration gradient. Kock *et al.* also suggested that the driving force for carbon diffusion is the concentration gradient of carbon content of sub-stoichiometric carbides, therefore the carbon content decreases with the direction of the metal-carbon interface.[35]

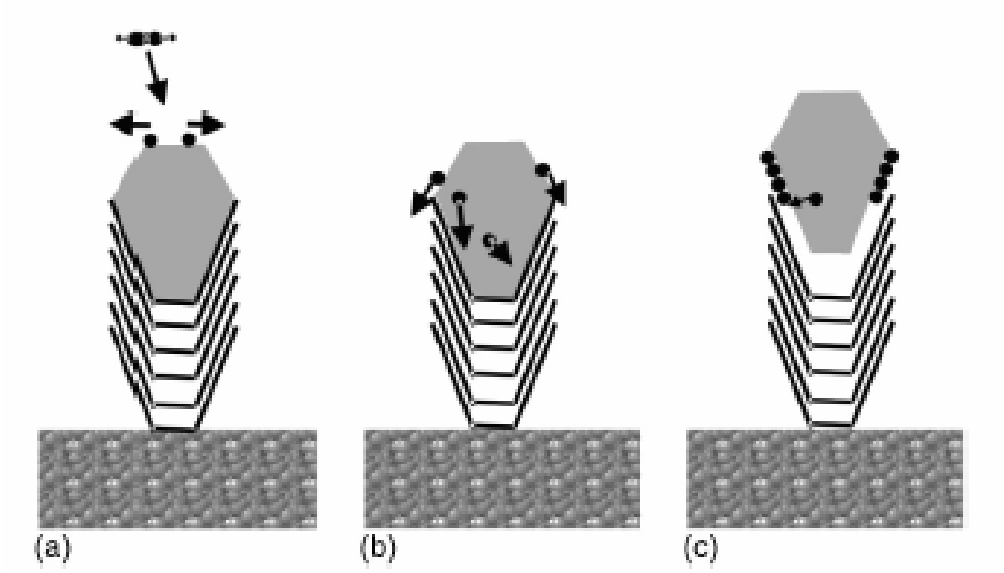


FIG. 1-9. Growth mechanism of carbon nanofiber. (a) Adsorption and decomposition of reactive hydrocarbon molecule on the surface with catalyst, (b) dissolution and diffusion of carbon species through or around metal particles, and (c) precipitation of carbon on the reverse surface of the catalyst particles and incorporation into graphite layers.

R. T. K. Baker, M. A. Barber, R. J. Waite et al., Journal of Catalysis 26 (1), 51-62 (1972).

1.3.3 Synthesis process and growth mechanism of catalytic plasma enhanced chemical vapor deposition (C-PECVD)

Plasma enhanced chemical vapor deposition (PECVD) is one of the widely used deposition techniques which utilizes a plasma to reduce activation energy. By decreasing the activation energy, the growth temperature of thin films can be also lowered and can be suitable for low temperature deposition. By introducing catalysts in PECVD system (C-PECVD), carbon nanostructures are successfully grown at low temperature relative to conventional CVD.[36] In recent study, Boscovic *et al.* suggested that a high field of radio frequency (rf) provides selective heating on catalyst particle in the growth of carbon nanostructures even though the substrate temperature is very low.[37] Other effects should be considered, however, as there are some possibilities of simple resistive (Joule) heating by induced current. That is, there is a possibility of Joule heating that contributes to the catalyst heating as well as the heating by high frequency movement of catalyst.

Prior to understanding the growth mechanism of carbon nanofibers, it is instructive to review the deposition theory of PECVD. PECVD is a technique commonly used in microfabrication to deposit insulating thin films amorphous or polycrystalline silicon. The plasma is used to stimulate a reaction on the substrate surface the species from the gas phase. The plasma helps break up the parent molecules and allows the reaction to deposit species at a lower temperature than conventional thermal CVD. The major advantage of PECVD is in fact, the lower temperature capability with respect to other systems such as conventional CVD. For example, while deposition temperatures of

500-900 °C are required for silicon deposition in CVD, temperatures in the range 250-350 °C are sufficient in PECVD systems. In the PECVD deposition process, a glow discharge plasma is sustained within vacuum chamber. The radio frequency ranging from 100 kHz to 40 MHz is usually employed as a power source at 50 mTorr to 5 Torr pressure range. When the plasma turns on, the density of electrons and positive ions are between 10^9 and 10^{12} /cm^3, and average electron energy is from 1 to 10 eV. The sufficiently energized discharge decomposes gas molecules into several kinds of species; electrons, ions, atoms, free radicals, and molecules in ground and excited states. PECVD is commonly utilized to deposit silicon dioxide (SiO_2) and silicon nitride (Si_3N_4) for insulating layer of microelectronics. SiO_2 films are formed by reacting silane and nitrous oxide gases. Si_3N_4 films are deposited either by reacting silane and ammonia gases or by reacting silane in a nitrogen discharge. The following is a reaction sequence for producing SiNH films from silane and nitrous oxide.

$$SiH_4 + 4N_2O \rightarrow SiO_2 + 4N_2 + 2H_2O$$
$$SiH_4 + NH_3 \rightarrow SiNH + 3H_2$$
$$2SiH_4 + N_2 \rightarrow 2SiNH + 3H_2$$

In the case of direct-current PECVD system to grow carbon nanofibers, the substrate is usually placed on a substrate heater that is a cathode. To grow isolated VACNFs, the metal catalyst is essential as described previously. Among many kinds of metal catalyst, patterned 40 nm dimeter Ni dots on a Si substrate is preferentially used to synthesize isolated VACNFs.[38] Fig. 1-10 shows dc-PECVD system to grow VACNFs. The process sequence to grow VACNFs is the following; 1) pump down to base pressure, 2) after reaching base pressure below 1×10^{-5} Torr, ammonia (NH_3) gas is introduced into

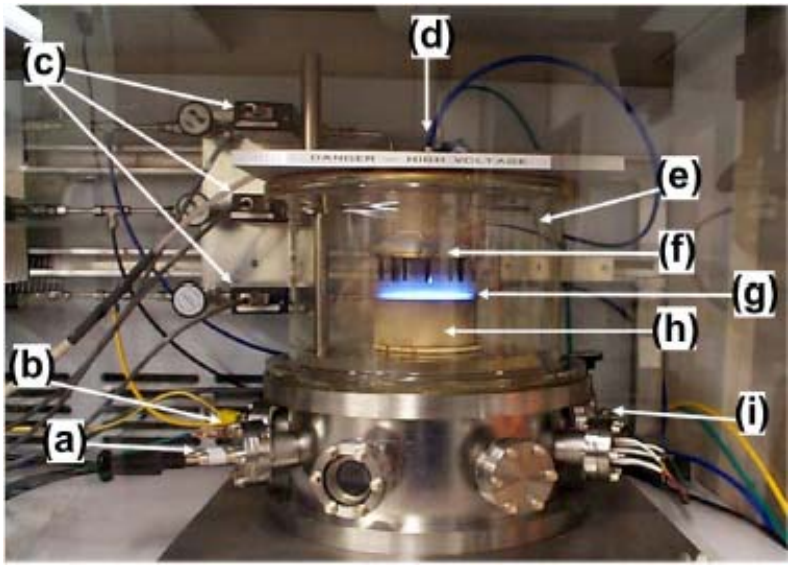


FIG. 1-10. DC-PECVD reactor for the growth of VACNFs. (a) High current heater wiring, (b) thermocouple wiring, (c) mass flow controllers for acetylene, ammonia, and other gases, (d) gas inlet, (e) glass cylinder vacuum chamber, (f) gas showerhead and anode, (g) cathode glow of acetylene/ammonia plasma above a 100-mm diam Si wafer, (h) substrate heater and cathode, and (i) pressure transducer.

A. V. Melechko, V. I. Merkulov, T. E. McKnight et al., Journal of Applied Physics 97 (4), 41301 (2005).

the chamber and the sample is pretreated with the NH_3 plasma. As a result of the treatment, discrete catalyst nanoparticles are formed from the deposited catalyst dot as shown in Fig. 1-11 (b). These nanoparticles play an important role of forming seeds for the catalytic growth of isolated VACNFs. After the pretreatment, 3) acetylene (C_2H_2) gas is introduced into the chamber with maintaining NH_3 plasma and then the growth of VACNF is initiated vertically. Fig. 1-12 shows SEM images of VACNFs with a tip-type and non-aligned base-type CNFs grown by dc PECVD. Melechko *et al.* showed that the kinetics of the CNF growth also plays a role in various kinds of growth mode; base-type and tip-type CNFs can be simultaneously grown on the same substrate and using same catalyst by changing the ratio of gas flow.[36]

1.3.4 Electrical and electrochemical properties

Lee *et al.* reported recently the electrical properties of individual VACNF by measuring current-voltage characteristics of suspended nanofiber bridge.[39] The nanofibers showed typical linear current-voltage characteristics at low applied voltage both positive and negative. The estimated range of resistivity was calculated to be from 10^{-6} to 10^{-5} Ω·m with the assumption that the electrical conductivity is equal within the entire cylindrical cross-sectional area of the nanofiber.

Carbon nanofibers have been widely used as electrodes in electrochemical measurements since it provides low fabrication cost, stability in aqueous solutions, and

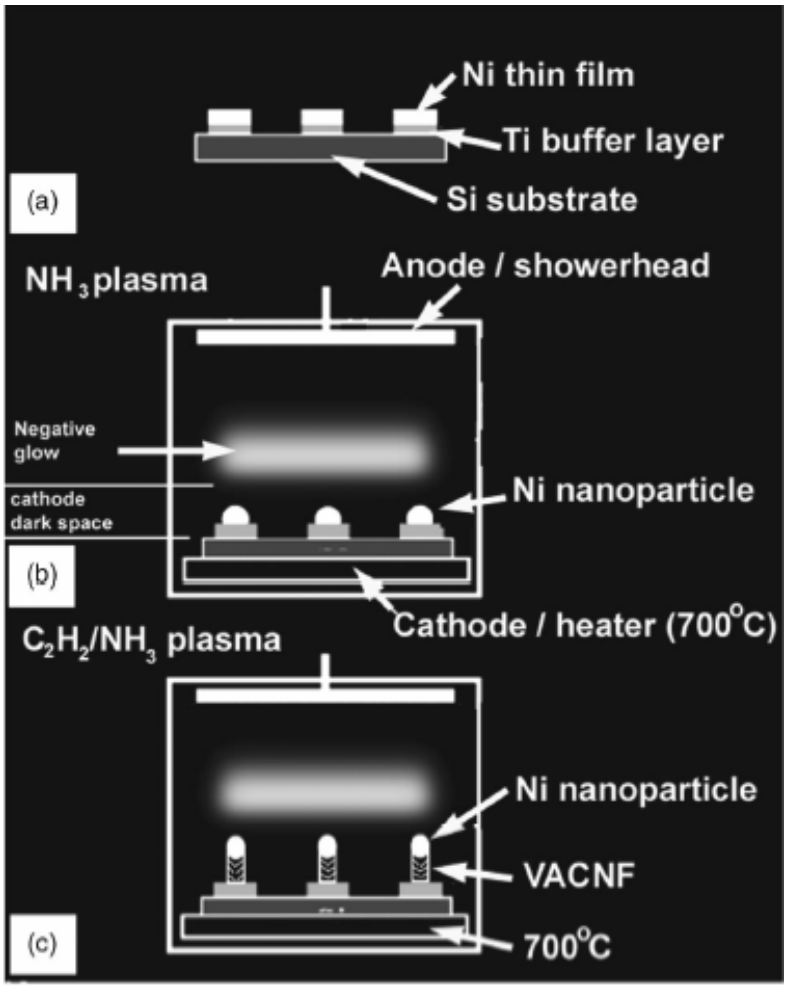


FIG. 1-11. Schematic representation of the PECVD process for growing VACNFs. (a) Catalyst deposition, (b) catalyst pretreatment / nanoparticle formation, and (c) growth of carbon nanofibers.

A. V. Melechko, V. I. Merkulov, T. E. McKnight et al., Journal of Applied Physics 97 (4), 41301 (2005).

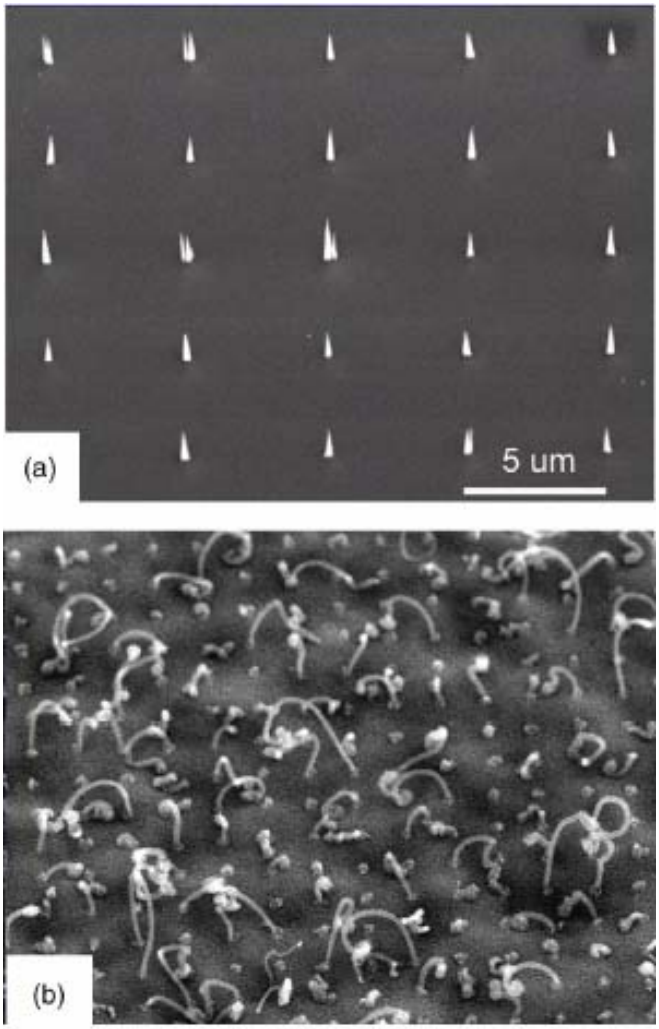


FIG. 1-12. SEM images of two types of carbon nanofibers. (a) Vertical alignment of carbon nanofibers in a tip-type growth mode, and (b) nonaligned growth of base-type carbon nanofibers by DC PECVD process.

A. V. Melechko, V. I. Merkulov, D. H. Lowndes et al., Chemical Physics Letters 356 (5-6), 527 (2002).

excellent electrochemical reactivity. McKnight *et al.* studied the electrochemical properties of VACNF electrodes as electrochemical probes which were grown by dc-PECVD using a Ni catalyst.[40] The VACNFs showed very prospective possibilities in the application of nanoscaled carbon electrodes into multi-element array such as individually addressable probing devices providing unique platforms to introduce a high level of parallelism into electro-physiological and electro-analytical techniques.

Recently, VACNFs were also used as gene delivering device to introduce genetic materials into live cells. In this application, individual VACNFs were used for the direct injection and delivery of genetic materials into the intracellular and nuclear domains of eukaryotic cells. McKnight et al. used VACNF arrays in the as a parallel microinjection-based method.[41]

Chapter 2 Materials integration issues for the active matrix thin film transistor array of intracellular probes

2.1 Gate electrode, molybdenum-tungsten (MoW)

2.1.1 Background

For TFTs to achieve high-speed, high-density, and low-power consumption, a low-resistivity gate and / or source-drain metal electrode is essential. As shown in Table 2-1, molybdenum (Mo) (and Mo alloys), aluminum (Al) (and Al alloys), and copper (Cu) are generally used as gate electrodes in manufacturing electronic displays and semiconductor devices. In choosing a metal material for the gate electrode, there is a trade-off between resistivity and thermal/chemical stability. Al and Cu, for example, have very low electrical resistivity and therefore have a significant advantage and attraction to applications in high speed and large-scaled thin film devices. However, their thermal stability is very poor, especially, for processing temperatures in excess of 500 °C. One of the main problems occurs during heat treatment of the Al (Cu)-Si contact because Al (or Cu)-Si inter-diffusion is significant above 500 °C. This interdiffusion can, for example, create silicon precipitates in Al which reduces the overall conductivity of the lines. In addition, Al can suffer from electromigration, which is a metal mass transport due to an electric current. Al atoms move in the direction of electron flow, toward the anode, and vacancies remain in the Al thin film. Consequently, Al whisker growth can

Table 2-1. Representative gate electrode materials for fabrication of TFTs.

Material	Resistivity (μΩ·cm)	Stress resistance	Taper angle in dry etching
MoTa	40-45	Excellent	Good
MoW	15-20 (conventional) 7-10 (our work)	Excellent	Excellent
Al alloy (AlNd)	5-7 (post-annealed)	Fair	Good (AlNd)
Al-Cu	4-5	Fair	Fair
Al	4-5	Poor	Fair
Cu	3-4	Good	Fair

be observed between Al and Si films. If the whiskers contact other layers, for example dielectric layers, they can cause additional device failures. When Al is passivated by a dielectric, hillock formation can cause cracking of such films. To prevent hillock formation, in the case of using Al as a gate electrode, a Mo layer can be added to form a Mo/Al bilayer.[42] The bi-layer deposition and dry etch processes, however, are more complicated. The dry etch process is particularly difficult because the Mo and Al etch chemistries are different.

When fabricating TFT devices, the etching profile of the gate electrode is also very important. This is especially true for an invert-staggered TFT structure where the gate electrode is the bottom layer (typically used in TFT-liquid crystal displays). These structures require a tapered etch profile for several reasons. Firstly, it provides better step-coverage in subsequent deposition patterning processes. Secondly, the sharp edged (undercut) gate is a main source of dielectric breakdown due to the concentration of electric field at this sharp-edged point. Thirdly, the tapered gate electrodes influence the electrical properties of a TFT and can lower threshold voltages and facilitate steep swing characteristics.

For the past several years, the molybdenum tungsten (MoW) alloy has been studied and used as gate electrodes by Thin Film Transistor-Liquid Crystal Display (TFT-LCD) manufacturing companies because of its excellent thermal and chemical stability, reasonably low resistivity, and easily controllable etch taper angle.[43],[44] In spite of its excellent properties, problems with larger substrate size and higher device driving speed have been encountered. Some of the problems include flicker, cross-talking, and line

delay due to relatively high resistivity of MoW (15~20 μΩ·cm). To compensate the high resistance, MoW thin films require wider and thicker patterns. The wider and thicker MoW causes some fabrication problems in large-scaled integration and planarization of the device which can also lead to device failure. Therefore a thorough investigation of the process-property relationships of the MoW alloy is necessary to extend the utility of this alloy to advanced semiconductor applications. Although MoW has many advantages in microelectronics, especially high temperature applications, there is not much published work on this thin film alloy. In this work, we present electrical and micro-structural properties as a function of the MoW composition for films sputtered under various process conditions (temperature and bias).

As shown in Fig. 2-1, the Mo-W binary system has complete solid solubility since they satisfy the requirements to make the complete solid solution; same crystal structure (body-centered cubic, BCC), similar electronegativity (Mo-2.16, W-2.36) and below 3 % of lattice parameter difference (Mo-0.3147 nm, W-0.3164 nm).

2.1.2 Experimental

The details of the sputtering conditions used to deposit the MoW specimens are shown in Table 2-2. An AJA ATC2000 RF magnetron sputtering system equipped with heated and DC biased substrate holder was utilized for the deposition of Mo, W, and MoW thin films (Fig. 2-2). The films were deposited on thermally oxidized SiO_2 (1 μm) / Si (100) substrates. The substrate holder can be rotated if uniform thickness and

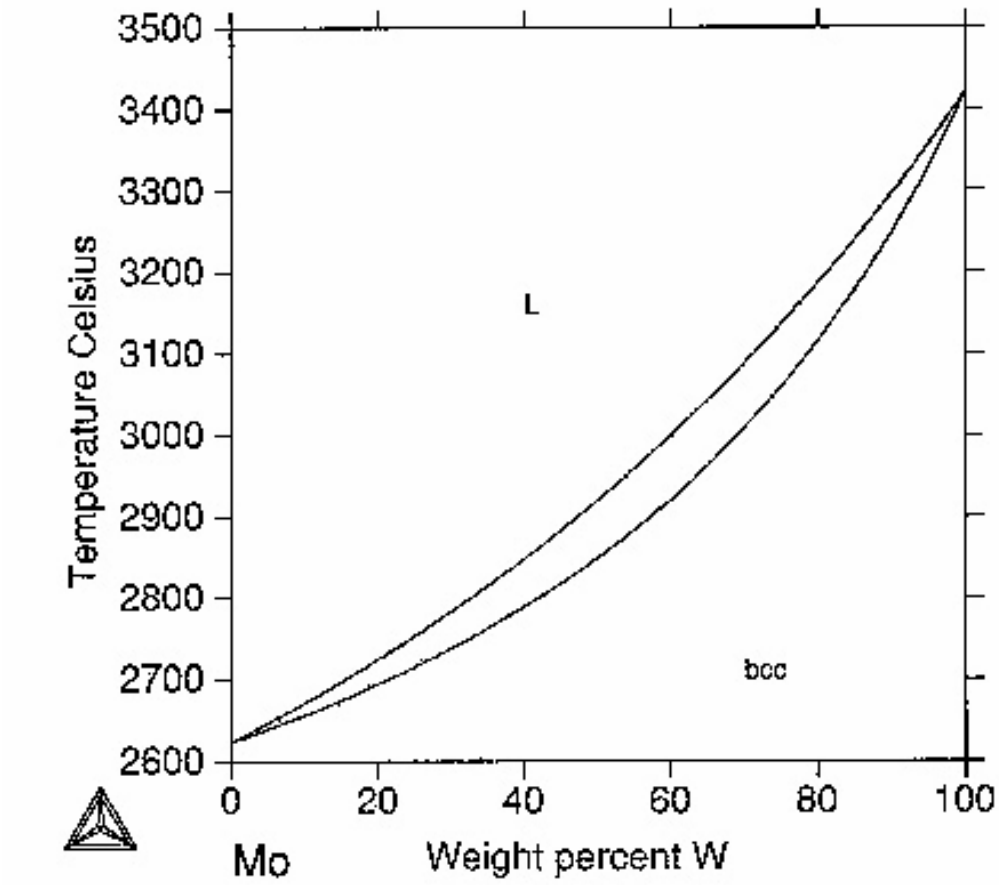


FIG. 2-1. Equilibrium phase diagram of Mo-W binary system.

(P. Gustafson et al., 79 (6), 1988, p388-396, SGTE Phase Diagram Collection at www.met.kth.se)

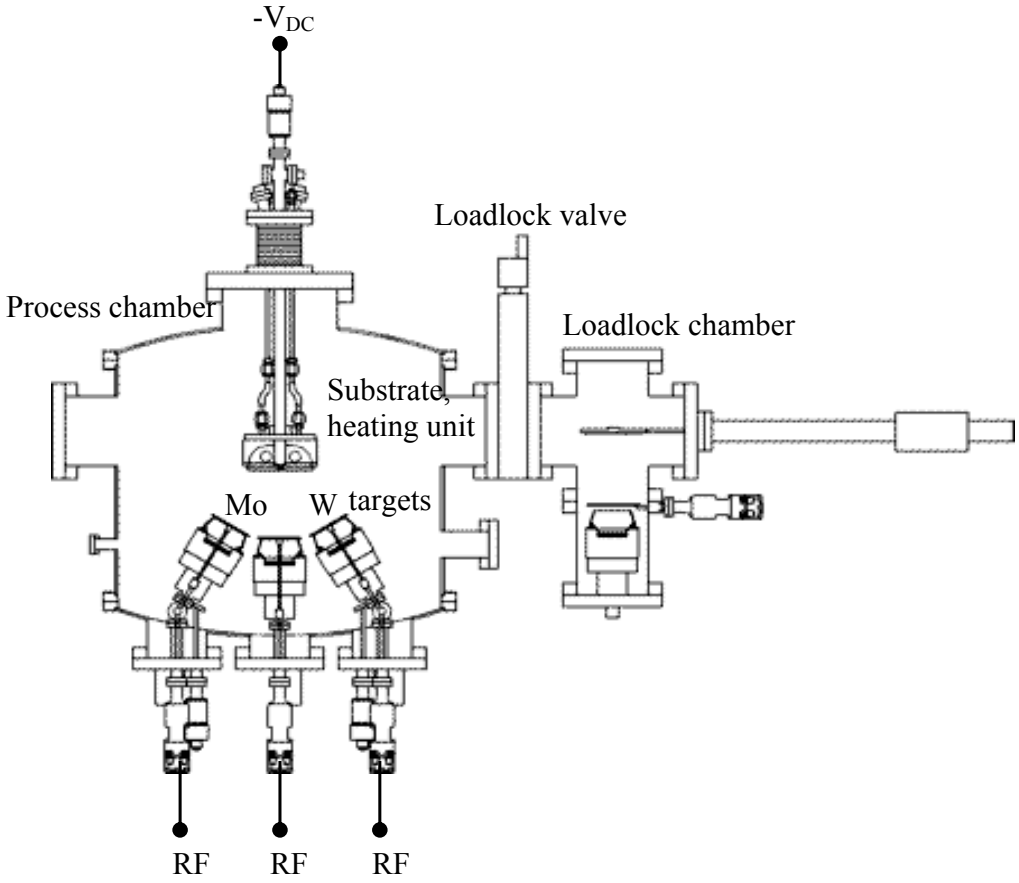


FIG. 2-2. Schematic diagram of an AJA ATC2000 RF magnetron sputtering system equipped with DC bias supply.

Table 2-2. Experiment conditions for the MoW work.

Run No.	ID	RF power (W)		DC bias (Watt / Volt)	Pressure (Pa)	Temp. (˚C)
		Mo	W			
1st series	(a)	200	160	0 / 0	0.66	RT
	(b)	200	160	0 / 0	0.66	250
	(c)	200	160	30 / 165	0.66	RT
	(d)	200	160	30 / 165	0.66	250
2nd series	(a)	200	0	0 / 0	1.06	RT
	(b)	200	0	15 / 140	1.06	RT
	(c)	200	0	30 / 165	1.06	RT
	(d)	200	0	45 / 190	1.06	RT
	(e)	0	200	0 / 0	1.06	RT
	(e)	0	200	15 / 140	1.06	RT
	(f)	0	200	30 / 165	1.06	RT
	(g)	0	200	45 / 190	1.06	RT
	(h)	200	200	0 / 0	1.06	RT
	(i)	200	200	15 / 140	1.06	RT
	(j)	200	200	30 / 165	1.06	RT
	(k)	200	200	45 / 190	1.06	RT

(Fixed parameters: 25 sccm Ar gas, 70 mm gap between substrate and target)

composition are desired and produces a $Mo_{1-x}W_x$ ($0.1 < x < 0.9$) gradient when the sample is not rotated (combinatorial mode). As shown in Fig. 2-2, the system has three targets each equipped with an rf matching network and power supply. The sources can be tilted and the z-position of the substrate holder can be varied in-situ to change the deposition profile. The sputtering targets have a 50 mm diameter and a 6 mm thickness. The base pressure prior to the sputtering deposition was below 5.0×10^{-6} Pa and the total flow rate of argon used in these experiments was fixed at 25 sccm for all conditions. The substrate is heated by quartz lamps and the temperature is controlled within ± 1 °C temperature range. The resistance was analyzed via four point probe measurements (Veeco FPP-5000) at a fixed film thickness (~300 nm). The crystal structure characteristics of the films were analyzed with a Phillips X-pert Pro X-ray diffraction (XRD) system, and the microstructure was analyzed by using a Hitachi S-4700 scanning electron microscope (SEM). The first series of experiments was designed to analyze electrical properties and microstructures as a function of Mo-W composition, applied bias, and substrate temperature. The second series was designed to explore the effects of the applied bias on the electrical and micro-structural properties of MoW.

2.1.3 Results and discussion

A. Films deposited without negative bias at room temperature and 250 °C

The electrical resistivity of the MoW alloy as a function of atomic fraction of W is shown in Fig. 2-3. In the figure, (a) and (c) are processed at room temperature and (b)

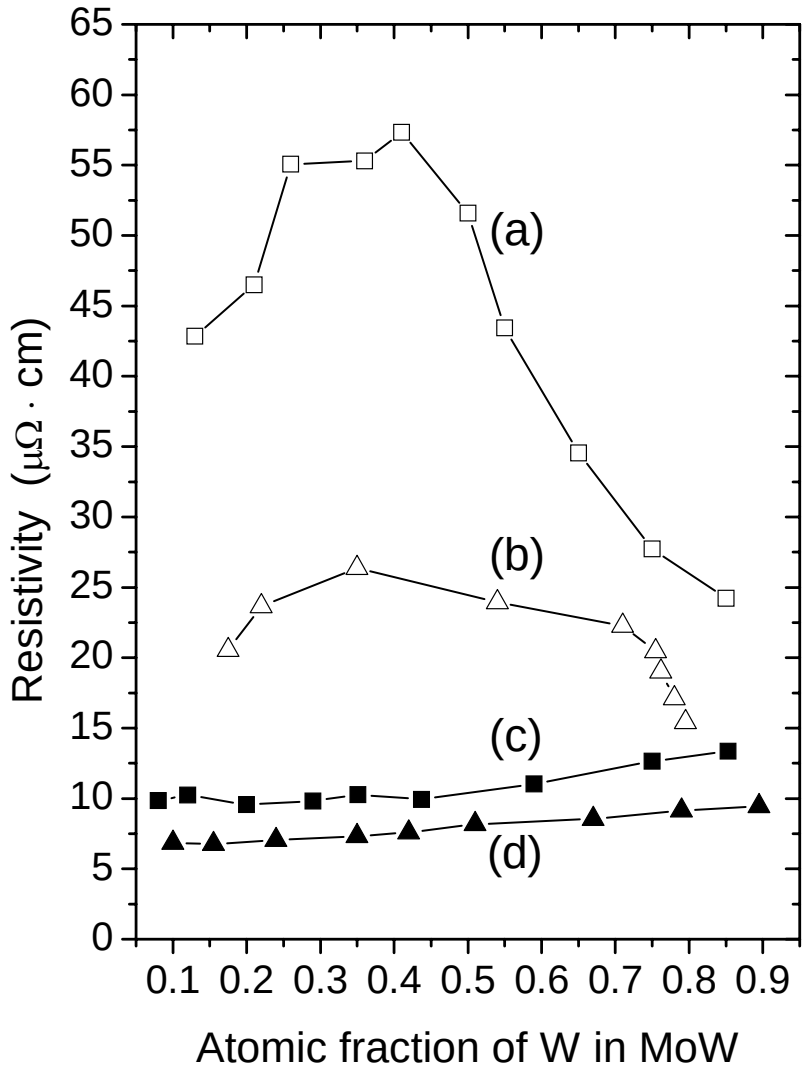


FIG. 2-3. Electrical resistivity of MoW as a function of composition, temperature, applied bias, and process pressure. (a) No bias / RT, (b) No bias / 250 ˚C, (c) 30 W (165 V) bias / RT, and (d) 30 W (165 V) bias / 250 ˚C from the 1st series.

and (d) are at 250 ºC. And (a) and (b) are processed without bias and (c) and (d) are under a 30W (165V) dc bias. The resistivity results as a function of W fraction for (a) and (b) samples that are processed without bias follow a typical Nordheim relationship. In a metallic material, the electron scattering due to the perturbations such as solute atoms, second phases, impurities, dislocations, vacancies, and grain boundaries increase electrical resistivity. As demonstrated in Fig. 2-3 (a) and (b), the electrical resistivity of the MoW binary system increases with increasing solute concentration, and it has the maximum at ~ 0.5 atomic fraction of solute atoms because of high electron scattering due to defects from mixing of the solid solution. The resistivity of binary alloys can be expressed by the well-known Nordheim's equation:

(1) $\rho_I = Cx(1-x)$

where x is the fraction of solute atoms and C is Nordheim coefficient. This expression is valid for binary systems having the same valency. Therefore, the total resistivity of the metal alloy can be described with Matthiessen's rule;

(2) $\rho = \rho_T + \rho_R + \rho_I$

Combining 1 and 2 yields:

(3) $\rho = \rho_T + \rho_R + Cx(1-x)$

where, ρ_T is the resistivity due to scattering from thermally activated vibration; ρ_R is the residual resistivity due to the scattering from crystal defects, dislocations, vacancies, and impurities, etc.; ρ_I is the resistivity arising from solute atoms. The Nordheim coefficients of (a) and (b) in Fig. 2-3 are 118 and 70 μΩ·cm, respectively. The sputtering temperature provides energy to the arriving species which enhances their surface mobility and allows

the species to occupy a lower energy state. This leads to a more ordered structure which reduces the electron scattering, and lowers the electrical resistivity.

Fig. 2-4 shows XRD results of MoW as a function of W fraction at several sputtering conditions; (a) room temperature with no bias, (b) room temperature with 30 W (165 V) bias, 250 ºC with no bias, and 250 ºC with 30 W (165 V) bias. The XRD result of Fig. 2-4 (b) is identical to the RT / 30 W bias, 250 ºC / no bias, and 250 ºC / 30 W bias sputtering conditions. In the XRD spectra, the strong peak around $2\theta = 40°$ is a confluence of several peaks from α-W (40.26°, 110 plane), β-W (39.89°, 210 plane), and Mo (40.51°, 110 plane). The weak peak around $2\theta = 38°$ is a noise signal from the aluminum sample holder. As shown in Fig. 2-4 (a), at room temperature and without bias, a second metastable phase (β-W) is observed which correlates well with the resistivity, i.e. higher β-W content correlates with higher resistivity. The intensity of β-W (200) changes significantly with the atomic fraction of W in MoW alloy and has a maximum at ~ 0.5 W. It is opined that the β-W fraction in MoW is highest at the ~ 0.5 W composition because the strain induced by the lattice mismatch between Mo and W is highest at ~ 0.5 W which helps nucleate the metastable β-W. The β-W has a 5.05 Å lattice constant and its lattice mismatch with α-W is about 37.3 % in transforming from β-W to stable α-W phase. It has an A15 crystal structure and W atoms are positioned at (0, 0, 0), (½, ½, ½), (¼, ½, 0), (¾, ½, 0), (0, ¼, ½), (0, ¾, ½), (½, 0, ¼), and (½, 0, ¾) sites.[45] It appears that the presence of metastable β-W causes electron scattering which increases the electrical resistivity of the MoW thin film. The relationship between the amount of β-W from the XRD results and electrical resistivity of the MoW is shown in Fig. 2-5. The relative

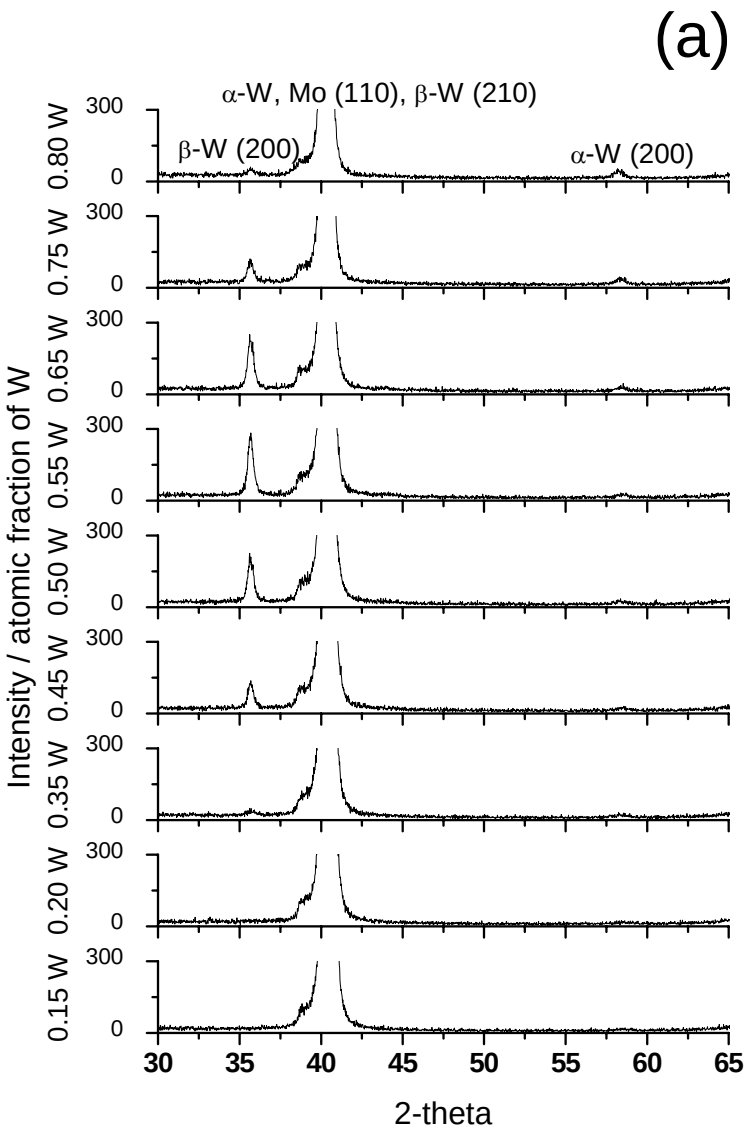


FIG. 2-4. XRD results of MoW as a function of W atomic fraction. (a) RT / no bias.

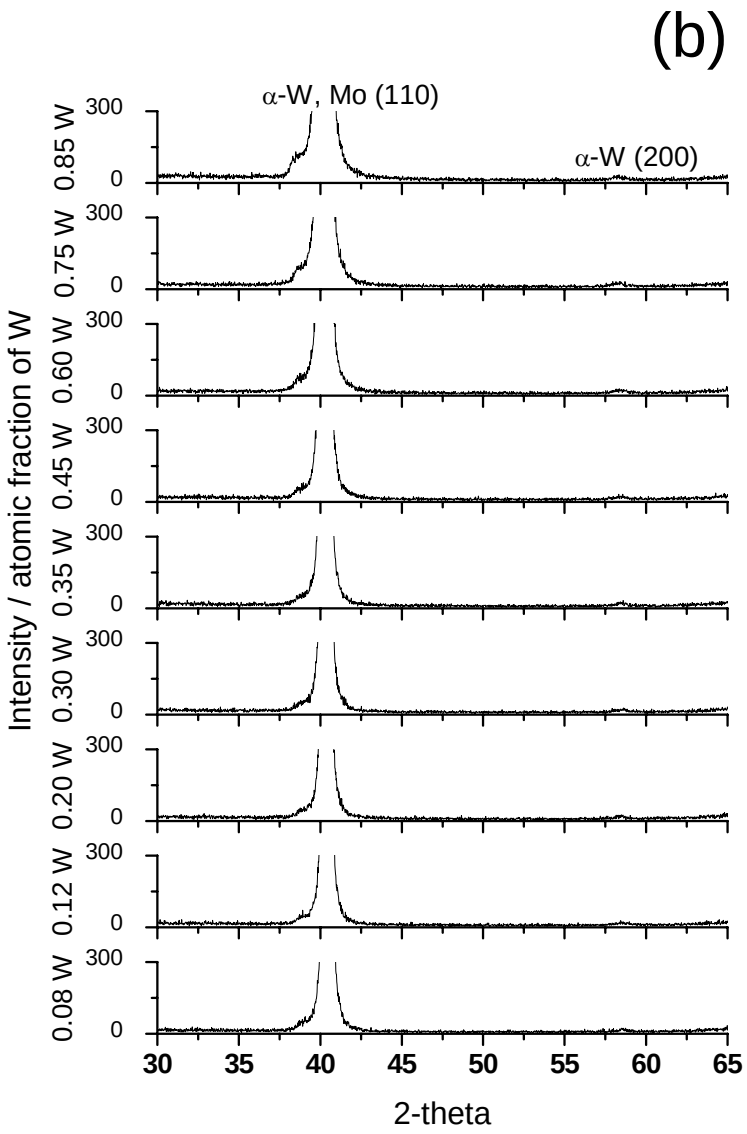


FIG. 2-4. Continued. (b) RT / 30 W bias.

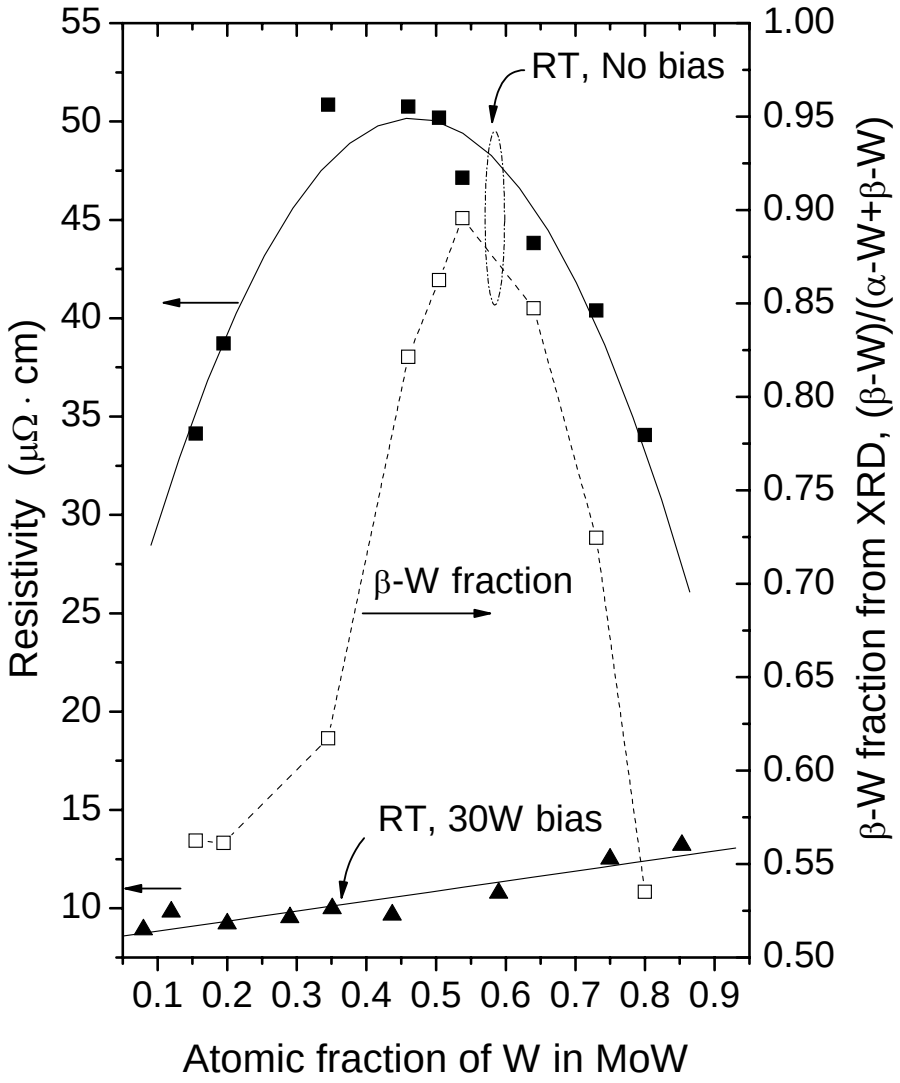


FIG. 2-5. The relationship between β-W fraction and electrical properties of MoW as a function of composition. (The β-W fraction at room temperature/30 W bias is zero because β-W phase is not present under all biased sputtering conditions even at room temperature sputtering.)

amount of β-W to α-W is calculated from the intensities of the (200) planes located at 58.27 ° (α-W) and 35.52 ° (β-W), respectively, and compared to the intensities expected from the standard diffraction patterns of each phase. This iteration was used because the (200) planes were the only peaks that did not have significant overlap with any other peaks. For the room temperature and un-biased sputter deposited sample, Fig. 2-5 shows that the presence of the second phase β-W significantly affects the resistivity. As the XRD peak intensity of β-W increases, the electrical resistivity also increases and has a maximum value at the point of ~ 0.5 atomic fraction W.

The sample deposited at 250 ^{o}C and un-biased does not contain the β-W phase over the entire composition range as illustrated in Fig. 2-4 (b). This correlates to Fig. 2-3 (c) which shows that resistivity of the 250 ^{o}C sample decreases relative to the room temperature deposited sample. This decrease is well correlated to the elimination of the second phase β-W. The higher temperature deposition could also induce a slightly more ordered lattice with fewer lattice defects which could also contribute to the lower resistivity. This contribution is not expected to be significant, however, due to the refractory properties of this alloy system. Therefore, the major factor that the 250 ^{o}C in-situ heating has on the MoW film is to slightly order the material and inhibit the metastable β-W phase from forming.

B. Films deposited with negative bias (30W, -165V) at room temperature and 250 °C

Comparing Fig. 2-3 (a) and (b) to (c) and (d), respectively, illustrates the effect that substrate bias has on the MoW alloy resistivity. A significant reduction in the film

resistivity over the entire composition range is realized for each condition. Unlike the un-biased samples, however, the resistivity of the biased samples do not follow Nordheim's rule. Rather, these samples obey a rule of mixtures relationship $\rho_{MoW} = x_{Mo}\rho_{Mo} + x_W\rho_W$ as a function of W fraction in MoW as shown in Fig. 2-3 (c) and (d). In this case the following relationship applies:

(4) $\rho = \rho_T + \rho_R + (x_{Mo}\rho_{Mo} + x_W\rho_W)$

where x_{Mo} and x_W are atomic fraction of Mo and W, respectively, and ρ_{Mo} and ρ_W are the resistivity of Mo and W, respectively.

With bias sputtering of ~ 30W (-165 V), the metastable β-W is not present, even at room temperature as shown in Fig. 2-4 (b). Fig. 2-6 shows a series of SEM images as a function of the tungsten fraction for samples deposited at room temperature with and without substrate bias. From the figure, it can be seen that the biased microstructure is denser and has less void space between grains. Table 2-3 illustrates the effect that substrate bias has on the lattice constant measured normal to the substrate. The substrate bias increases the lattice parameter of the MoW alloy and qualitatively it is shown that the induced strain in the z-direction is a result in a change in the bi-axial stress in the plane of the substrate which is tensile without substrate bias and compressive with substrate bias. While the magnitude of the stress was not specifically determined, thicker (1 μm) thick MoW films deposited with substrate bias peeled off subsequent to deposition, whereas un-biased 1 μm thick films did not.

Another interesting observation from Fig. 2-3 and Fig. 2-5 is that the biased tungsten-rich alloy has a higher resistivity than biased molybdenum-rich alloy, (c) and (d).

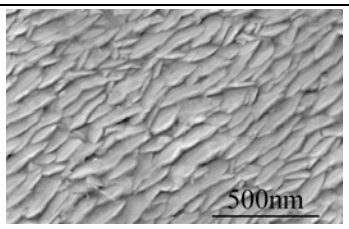
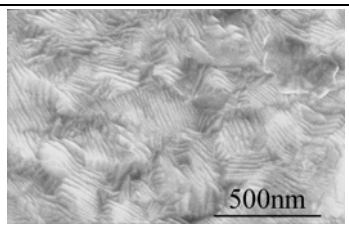
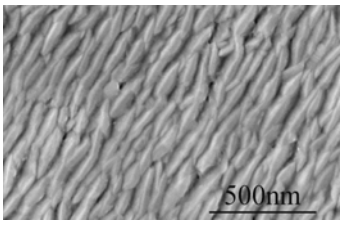
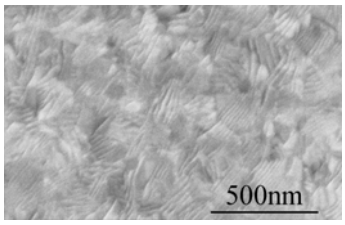
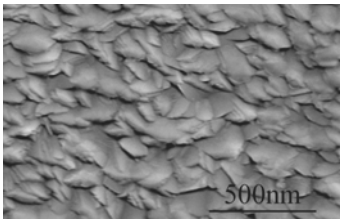
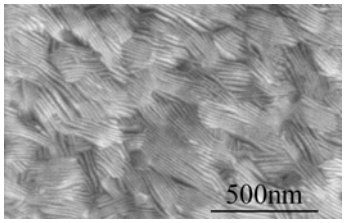
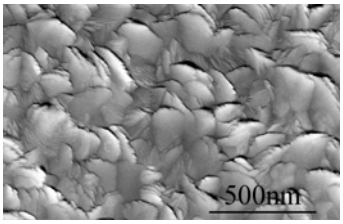
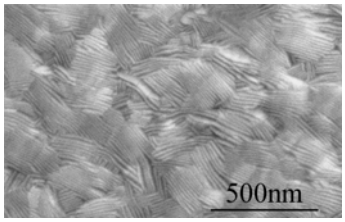
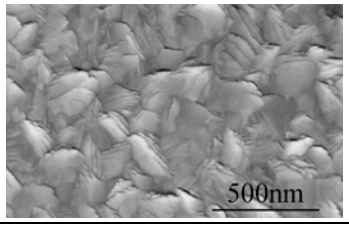
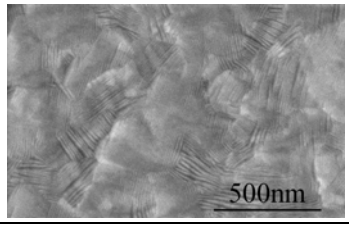
Atomic fraction of W	No bias	30 W (165 V) bias
0.10 W		
0.25 W		
0.50 W		
0.75 W		
0.90 W		

FIG. 2-6. SEM images of MoW surface morphology as a function of the W atomic fraction in MoW thin films for samples deposited at room temperature with and without substrate bias.

Table 2-3. Result summary of the 2nd experimental series.

	Applied bias Watts (V)	Resistivity μΩ·cm	Deposition rate nm/min	XRD (110) 2θ	[*1] Lattice constant nm
Mo	0	42.9	5.16	40.59	0.3141
	15 (140 V)	13.0	3.36	40.33	0.3161
	30 (165 V)	11.9	3.97	40.33	0.3162
	45 (190 V)	12.6	3.61	40.33	0.3161
W	0	18.7	5.50	40.37	0.3157
	15	13.1	4.43	40.17	0.3172
	30	13.1	4.16	40.15	0.3173
	45	14.8	3.64	40.15	0.3173
[*2] MoW	0	55.5	11.59	40.46	0.3150
	15	11.6	7.32	40.29	0.3163
	30	12.7	7.57	40.29	0.3163
	45	12.9	7.13	40.28	0.3164

[*1] Lattice constant of α-phase

[*2] 0.5 atomic fraction of W

Fixed parameters: 0.66 Pa, room temperature, 25 sccm Ar gas, 70 mm electrodes-gap

It is well known that the resistivity of bulk tungsten (α-W, 5.49 μΩ·cm) is slightly lower than that of molybdenum (Mo, 5.78 μΩ·cm) at room temperature. The reason for the higher resistivity for the tungsten-rich end of the biased samples can be explained by the dislocation density of tungsten relative to molybdenum. H. B. Shukvsky and L. D. Whitmire et al. showed that the dislocation resistivity of tungsten is higher than that of molybdenum. Specifically, the dislocation resistivity of tungsten and molybdenum are reported to be 6.7×10^{-11} and 5.8×10^{-13} $\mu\Omega\cdot cm^3$, respectively.[46],[47],[48] During sputter deposition on a biased substrate, the deposited MoW film is subjected to ion bombardment by highly energized ions and these ions can produce ion-radiated defects such as dislocation loops and point defects.[45] The electron scattering from dislocations in tungsten is nearly two orders of magnitude higher than molybdenum; therefore the tungsten-rich MoW alloy has a higher resistivity than the molybdenum-rich alloy. While the dislocation density in the films increases the resistivity of the tungsten-rich end, the overall effect of substrate bias improves the resistivity of the entire alloy. The substrate bias inhibits the β-W alloy from forming and produces a much denser film structure. While dislocations are likely generated by the impinging energetic species, the lattice structure has fewer vacancies and a more ordered overall structure.

In order to survey thermal stability of MoW (0.35 atomic fraction W), we investigated the current density and breakdown voltage of SiO_2 thin film with MoW electrodes after annealing up to 700 °C by using current-voltage measurement. The structure of these samples is MoW / PECVD SiO_2 / Si (100) and it was vacuum annealed at 100 °C to 700 °C (the upper limit of system) in 100 °C increments for 1 hour. There

were no changes in the current density and breakdown voltage between the as-deposited and annealed samples up to 700 ^{o}C which confirms the excellent high-temperature stability of MoW electrodes.

Fig. 2-7 shows dry etching profile of MoW (0.35 atomic fraction of W). A Trion Technologies Oracle reactive ion etching (RIE) system was used and the sample was etched under the process conditions of 120 W RF power, 16 Pa pressure, SF_6 / O_2 (25 / 35 sccm) gas flow rate. The etch profile is shown just before end point etching. This profile shows a slight tapered angle (~80 degrees) which can be significantly reduced (~ 30 degrees) by using a two step etch process or over etch process.[44]

2.1.4 Conclusion

For un-biased rf magnetron sputtered MoW films the electrical resistivity as a function of tungsten fraction follows a typical Nordheim relationship. The resistivity increases with the addition of solute atoms (tungsten) and it is maximum at ~ 0.5 atomic fraction of solute atoms. Films sputtered at room temperature without substrate bias contained a second metastable phase (β-W) and results in a significantly higher resistivity due to the lattice mismatch between stable α-W and metastable β-W. As sputtering temperature increases, the β-W does not form and the resistivity decreases over the entire composition range relative to the room temperature deposited sample. Thin films deposited with substrate bias had a considerably lower resistivity over the entire composition range and its resistivity as a function of composition obeys a rule of mixture

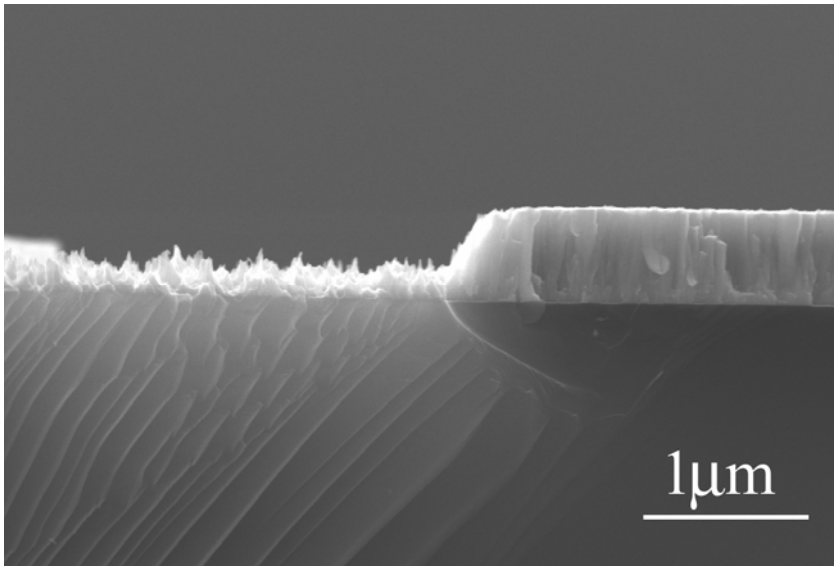


FIG. 2-7. Dry etching profile of MoW (0.35 atomic fraction of W) just before reaching the end point. (Reactive ion etching, 120 W RF power, 16 Pa pressure, SF_6 / O_2 = 25 / 35 sccm).

rule. Additionally, in the MoW film deposited with biased sputtering, the β-W phase is not present even at room temperature. From the SEM results, a denser and void-free structure is shown in the microstructure of biased thin films. Additionally, unlike bulk molybdenum and tungsten biased tungsten films had higher resistivity than biased molybdenum. This phenomenon is consistent with the fact that the dislocation resistivity of tungsten is two orders of magnitude higher than that of molybdenum.

2.2 Gate dielectric (I); silicon oxide (SiO_2)

2.2.1 Background

Sputtered silicon oxide has been widely studied and used as a dielectric insulator of electronic switching and sensing devices such as thin film transistors (TFTs) and metal-insulator-semiconductor (MIS) switching devices. Sputter deposition is a particularly attractive process as a low temperature large area fabrication process on transparent, flexible, and plastic substrates.[49],[50] While room temperature sputtered silicon oxide from a silicon dioxide target is possible, the film typically has a low breakdown field and is sub-stoichiometric (oxygen-deficient) relative to low temperature conventional chemical vapor deposition (CVD) silicon oxide films. Furthermore, sputtering from a silicon dioxide target has a low deposition rate since SiO_2 has an extremely low sputtering yield (0.13 atoms/ion for 1 KeV Argon). These disadvantages prohibit the adoption of this deposition technology for many manufacturing applications.

In order to enhance the electrical properties of sputtered silicon oxide, researchers have showed higher quality sputtered silicon oxide films with high breakdown field from a quartz target, using an argon and oxygen gas mixture, and low process pressure.[51] Its deposition rate, however, was still prohibitively low for industrial purposes. In the case of the reactively sputtered silicon oxide film from a silicon target with an argon and oxygen mixed gas, it typically has extremely low breakdown field because the film has high trap densities, non-stoichiometric composition, and other defects. In this work, we evaluated and optimized the silicon dioxide sputtering process with high breakdown voltage, high deposition rate, and ideal stoichiometric composition. The optimized silicon oxide from this work has a ~ 5.7 MV/cm breakdown voltage and ~ 6.2 nm/min deposition rate which is comparable to the deposition rate of refractory metal films (tungsten and molybdenum) at the same conditions in our sputtering system.[52] Lastly we fabricated and characterized a metal-insulator-semiconductor switching device that was entirely processed by RF magnetron sputtering deposition; bottom and top electrodes, silicon oxide, intrinsic and extrinsic silicon, and passivating silicon oxide.

2.2.2 Experimental

An AJA ATC2000 RF magnetron sputtering system equipped with three magnetron sources and heated and/or DC biased substrate holder was utilized for the deposition of silicon oxide, silicon, and metal films (Fig. 2-2). The base pressure before the sputter deposition was below 5.0×10^{-5} Pa and the mass flow rate of argon was fixed at

25 sccm for all conditions and the oxygen flow rate was varied. The gas delivery system preferentially delivers argon to the sputtering sources and delivers the reactive gas (oxygen) to the substrate, so as to extend the so-called "metallic" mode of reactive sputtering. A pure silicon target (99.9995 %) was used since its sputtering yield (S, atoms/ion) is much higher than that of quartz (S_{Si}=0.6 versus S_{SiO2}=0.13 for 1 KeV Argon). The silicon sputtering target has a 50 mm diameter and a 6 mm thickness. The film thickness was measured using a reflectometer (Filmeterics F20/40 Advanced Thin-Film Measurement System) and surface profiler (KLA Tencor Alpha-Step 500). The reported thickness is an average of at least five measurements over each deposited sample. In order to analyze the electrical properties, the silicon oxide film was deposited between the n-type silicon wafer and a tungsten film deposited with the sputtering system to form a metal-insulator-semiconductor structure; tungsten (200 nm), SiO_x (50 nm), and semiconductor (n-type Si wafer). The patterned top electrodes for current-voltage measurement were formed using a shadow mask with 50 μm-diameter circles with a 150 μm-pitch. The dielectric breakdown strength (breakdown voltage) was evaluated with an HP 4156A, Precision Semiconductor Parameter Analyzer and the reported values are an average of ten measurements over each sample. Finally, to show electrical stability characteristics of the silicon oxide film, we fabricated metal-insulator-semiconductor (MIS) switching device and evaluated the current-voltage characteristics of this switching devices.

2.2.3 Results and discussion

To evaluate the effects of the process factors in an efficient way, a design of experiment (DOE) was performed with a 2-level and 3-factor factorial design. The process target is high deposition rate with higher than 5 MV/cm breakdown field. Prior to the DOE, the hysteresis of the magnetron target voltage as a function of the oxygen fraction was analyzed in the sputtering gas in order to determine the ranges of "metallic" and "covered or oxide" sputtering modes that provide a proper range of oxygen fraction in the gas to achieve both modes of sputtering.[53] The abrupt decrease in target voltage, as shown in Fig. 2-8, shows that the plasma impedance increases with oxygen addition as the silicon oxide starts to form on the silicon sputtering target (oxide sputtering mode). The hysteresis did not changed with the sputtering temperature and substrate bias but changed with sputtering pressure. This indicates higher pressure causes the target to oxidize at lower oxygen flow rate because the effective oxygen partial pressure is higher even for lower flow rates because the throttle valve decreases the effective conductance of the pumping system. Therefore, the pressure was fixed at a low total pressure of 3 mTorr for all subsequent depositions. In addition to pressure, RF power can also shift the hysteresis loop to lower oxygen flow rates so the power was also fixed at 200 W (10 W/cm^2) for each deposition. Previous literature has shown that the oxygen flow rate significantly affects the silicon oxide properties, and has shown that higher oxygen partial pressures resulted in higher quality silicon oxide with high breakdown voltage and low current density.[51] On the other hand, the deposition rate decreases with increasing

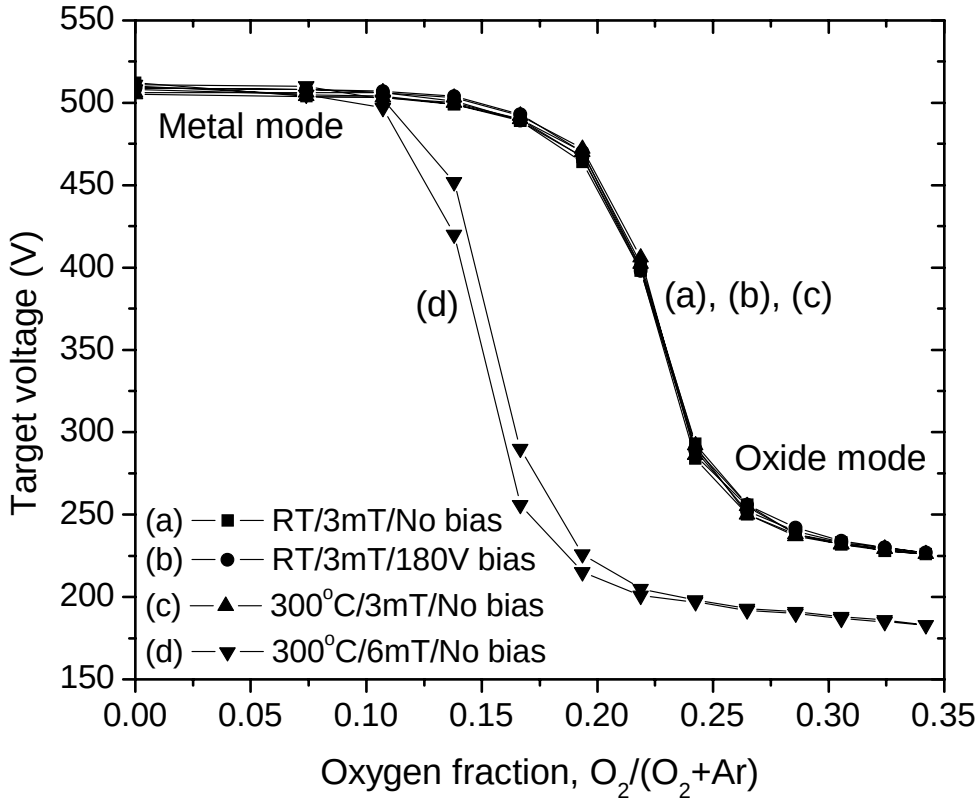


FIG. 2-8. Hysteresis of magnetron target voltage for a silicon target sputtered in Ar/O_2 mixed gas as a function of oxygen fraction.

oxygen partial pressure. In order to analyze both sputtering modes, the oxygen ratios (O_2/O_2+Ar) were set to 0.15 and 0.30; these represented metallic and oxide sputtering modes from the hysteresis curve, respectively. Table 2-4 shows the experimental conditions of variable factors and quantitative results of the responses. The factors of the DOE are temperature, oxygen ratio in the Ar-O_2 gas mixture, and substrate bias and all are two-level factorial designs. The measured responses were deposition rate, breakdown voltage, and oxygen ratio in the silicon oxide films as measured by x-ray photoelectron spectroscopy.

Fig. 2-9 shows the effects of temperature, oxygen ratio, and substrate bias on deposition rate, dielectric strength (breakdown field), and oxygen content in sputtered silicon oxide films. The results were analyzed and plotted by the IBM based statistical software, MINITAB®. Firstly, deposition rate, as we mentioned previously, depends mainly on the oxygen fraction in the sputtering gas as shown in Fig. 2-9 (a). The deposition rate drastically decreases as the oxygen partial pressure increases as there is a concomitant change from metal to oxide sputtering mode. The other factors, temperature and substrate bias, only slightly affect the deposition rate as the rate slightly decreases with temperature and substrate bias. It is suggested that densification of the silicon oxide film with increasing temperature and substrate bias causes the effectively lower deposition rate. The electrical properties of sputtered silicon oxide films, specifically breakdown field, are shown in Fig. 2-9 (b). As the temperature increases from room temperature to 300 ^{o}C, the breakdown field increases up to ~ 5.5 MV/cm. Also, as we expected, higher oxygen in the sputtering gas mixture has a positive factor on the

Table 2-4. Experimental conditions of variable factors and quantitative results of the responses for the sputtered silicon dioxide insulator study.

	Factors			Responses		
No	Temp., ^{o}C	Oxygen, O_2/O_2+Ar	Substrate bias, V	Deposition rate, nm/min	Breakdown field, MV/cm	Oxygen ratio in SiO_x, x
1	25	0.15	0	6.36	1.61	1.66
2	25	0.15	150	5.62	1.15	1.77
3	25	0.30	0	1.65	3.14	1.75
4	25	0.30	150	1.05	3.00	1.86
5	300	0.15	0	6.05	5.13	1.93
6	300	0.15	150	5.07	5.61	2.00
7	300	0.30	0	1.54	5.43	2.00
8	300	0.30	150	0.84	5.56	2.00
* 9	25	0.15	0	-	1.93	-
* 10	25	0.15	150	-	2.74	-

* Post-annealed after deposition: 300 ^{o}C, 5 hours in vacuum

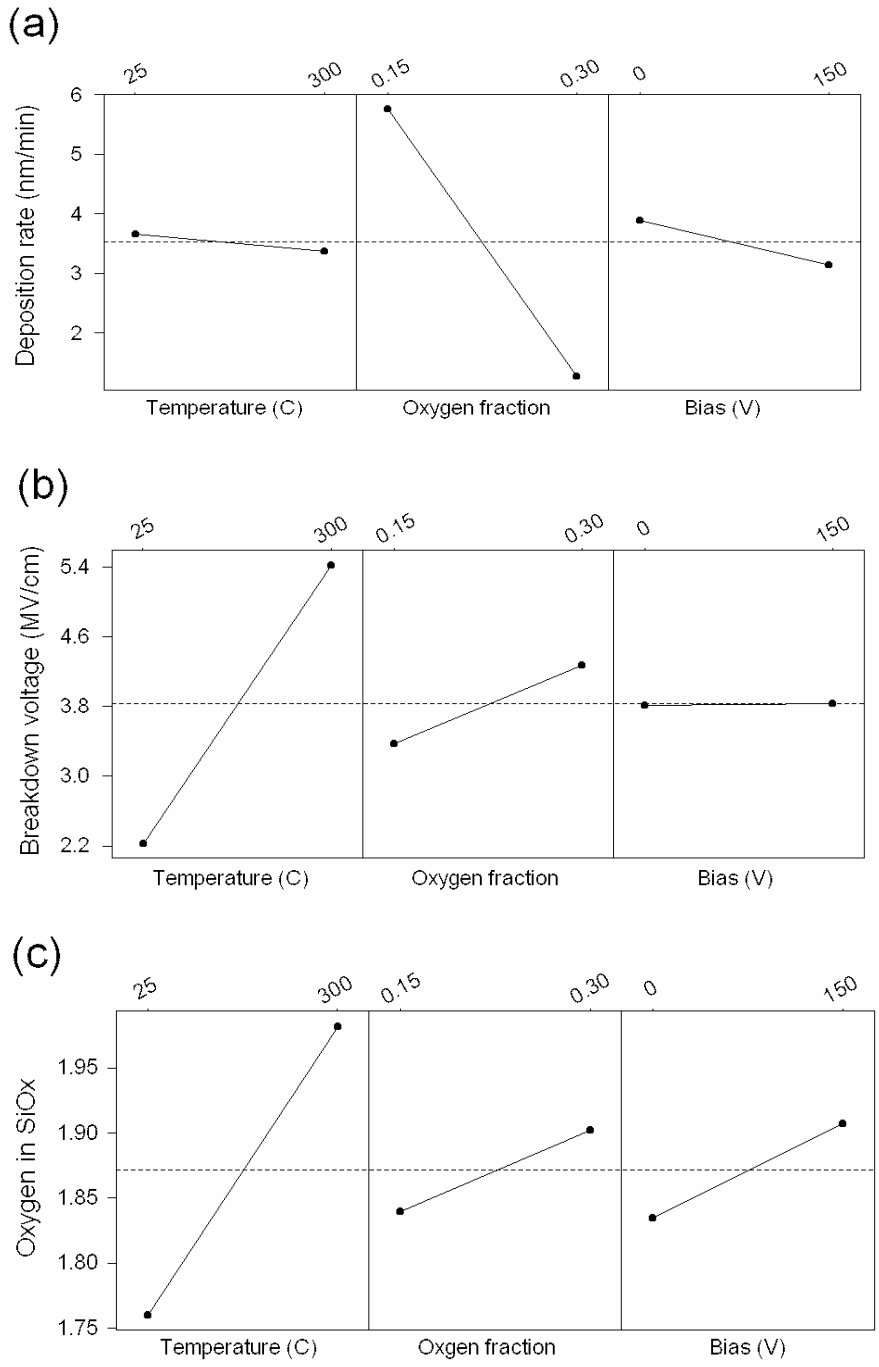


FIG. 2-9. Graphical expression of results from statistical design of experiments. (MINITAB® Statistical Software Release 13.4).

breakdown field. Both higher temperature and oxygen fraction reduce the defect density in the films; dangling bonds, vacancies and non-stoichiometric defects, etc. Counter to our expectation, the substrate bias does not affect the breakdown voltage. We speculate that substrate bias densifies the thin film by via energetic ion bombardment; however, these energetic ions can also produce ion-irradiated defects such as dislocation loops, point defects, and can change the stoichiometry by preferentially sputtering either the cation or anion species.[52] Any or all of these effects can deteriorate the electrical properties of the films. These defects induced by substrate bias can be released by post-annealing as shown in the results for sputtering condition (10) of Table 2-4, which has almost the same breakdown field as the unbiased sample after post-annealing. Before the annealing, as shown in Table 2-4 (1) and (2), the breakdown voltage of biased films is slightly lower than without substrate bias. After post-annealing at 300 ^{o}C for 5 hours in vacuum, the breakdown field was enhanced and the breakdown field was higher than that of the unbiased condition. This result shows that the substrate bias in sputtering provides densification and ion-radiated defects in the films at the same time. The ion-radiated defects can be easily released by post-annealing and its electrical properties are improved by the annealing resulting from relaxation of the bias-originated defects combined with amore densified film.

The concentration ratio of oxygen to silicon in sputtered silicon oxide film was analyzed by X-ray Photoelectron Spectroscopy (XPS). As shown in Fig. 2-9 (c), temperature, oxygen, and substrate bias are positive factors on the stoichiometric oxygen ratio of silicon oxide films. That is, the silicon oxide film becomes more stoichiometric

with increasing temperature, oxygen fraction, and substrate bias. From the results of Fig. 2-9 (b) and (c), the silicon oxide film is denser and more stoichiometric with applying substrate bias but, contrarily, the breakdown voltage is almost unchanged with substrate bias. It is surmised that the substrate bias provides ideal silicon oxide films with good stoichiometry and very dense. However, it causes micro-structural defects, for example dislocations, due to the highly energized ion bombardment.[45]

Table 2-5 (a) shows the optimized individual factors with higher deposition rate, higher breakdown voltage, and stoichiometric SiO_2 films by statistical software, MINITAB®. By doing an interpolation of the ideal sputtering parameters, as shown Table 2-5 (b), the optimized process conditions were obtained; 300 ^{o}C temperature, 0.15 oxygen fraction, and 56 V substrate bias. We also compared the predicted value done by the statistical program with the actual value by depositing the optimized film condition as shown in Table 2-5 (b). The actual values are slightly higher than the predicted in the deposition rate and breakdown voltage but are within an acceptable value of 10 % of the predicted values.

Fig. 2-10 shows a metal-insulator-semiconductor (MIS) array, which for the lithographic mask set has 20 column and 20 row electrodes. Each pixel can be individually addressed by applying an electric field on a specific pair of column and row electrodes. The MIS device is composed of a bottom electrode, insulator, intrinsic amorphous silicon, n^{+} doped amorphous silicon, and top electrodes. This MIS is normally used in chemical sensing devices and switching elements for detecting or turning on/off with the concentration change of specific gas in a mixed gas.[54,55] In this

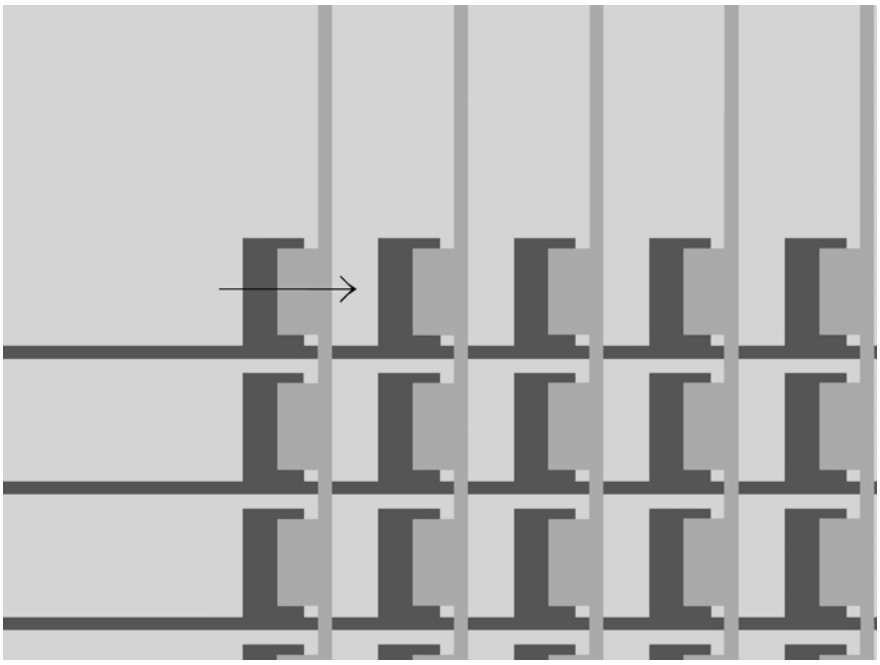
Table 2-5. Optimized process conditions of individual and mixed factors.

(a) Optimization of individual sputtered silicon dioxide factors.

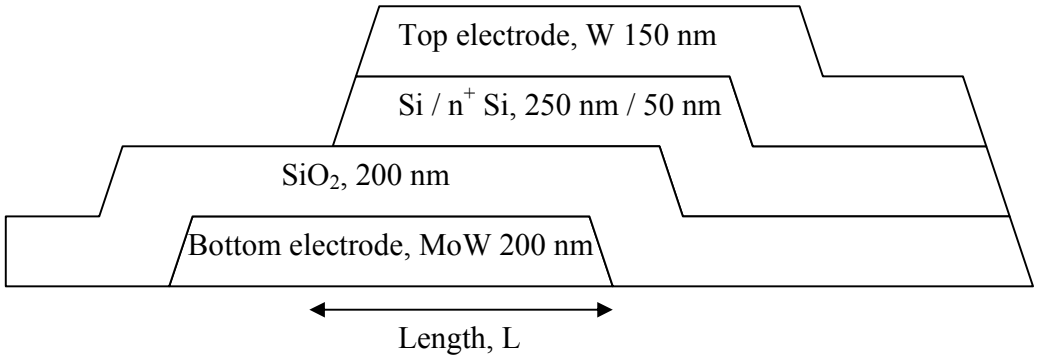
Process target	Temp. (^{o}C)	O_2 fraction	Bias (V)	Results
Max. deposition Rate	25	0.15	0	6.36 nm/min
Max. breakdown voltage	300	0.15	150	5.61 MV/cm
Optimum Stoichiometry x = 2.0 in SiO_x	300	0.30	150	2.0

(b) Optimized process conditions by statistical analysis and comparison of predicted and actual values.

	Process target	Temp. (^{o}C)	O_2 fraction	Substrate bias (V)	Predicted	Actual
Deposition rate	Maximum				5.68	6.26
Breakdown voltage	Maximum	300	0.15	56	5.31	5.70
x, SiO_x	2.0				1.95	-



(a)



(b)

FIG. 2-10. Device design for fabricating MIS switching device with 20 × 20 row and column electrodes. (a) Plane view of overall layout, (b) cross-sectional view of an unit pixel from left to right of arrow in (a).

work, molybdenum-tungsten (MoW) was used as bottom electrode to obtain a sloped etch taper angle for good step coverage.[52] The MoW was pattered by conventional lithography and reactive ion etching (RIE) using SF_6 + CF_4 + O_2 plasma gas. The deposition condition of the sputtered insulator, silicon oxide (SiO_x), is 200W RF power, 3 mTorr pressure, 300 ^oC temperature, 25.0 / 4.4 sccm Ar / O2 gas flow rate (O_2 / Ar+O_2 = 0.15), and 57 V substrate bias. The intrinsic silicon and n^+ doped silicon were deposited via sputtering at 200W RF power, 3 mTorr pressure, 300 ^oC temperature, 25 sccm Ar gas flow rate, and no substrate bias. Similar to the bottom electrodes, conventional lithography and reactive ion etching were utilized for pattering the top electrodes (W), n^+ doped silicon, and intrinsic silicon.

Fig. 2-11 demonstrates transfer characteristic of the MIS device by our sputtered silicon oxide, intrinsic silicon, and n^+ doped silicon in order to show the prospective of using the sputtered insulator films. The MIS device with sputtered Si and SiO_x shows dynamic transfer curves, however, the on-state current is relatively low. We speculate that the sputtered n+ silicon layer may not be doped as high as the target concentration, and consequently the contact resistance is higher than anticipated. The voltage margin at the off-state (zero-current) is from 1.5 to 3.0 V and its voltage-current transfer characteristics are quite similar to conventional Schottky-barrier diodes. From the results mentioned, we can conclude the optimized SiO_x film has very reasonable characteristics, high deposition rate and high enough breakdown field for fabricating microelectronic devices at relatively low temperature.

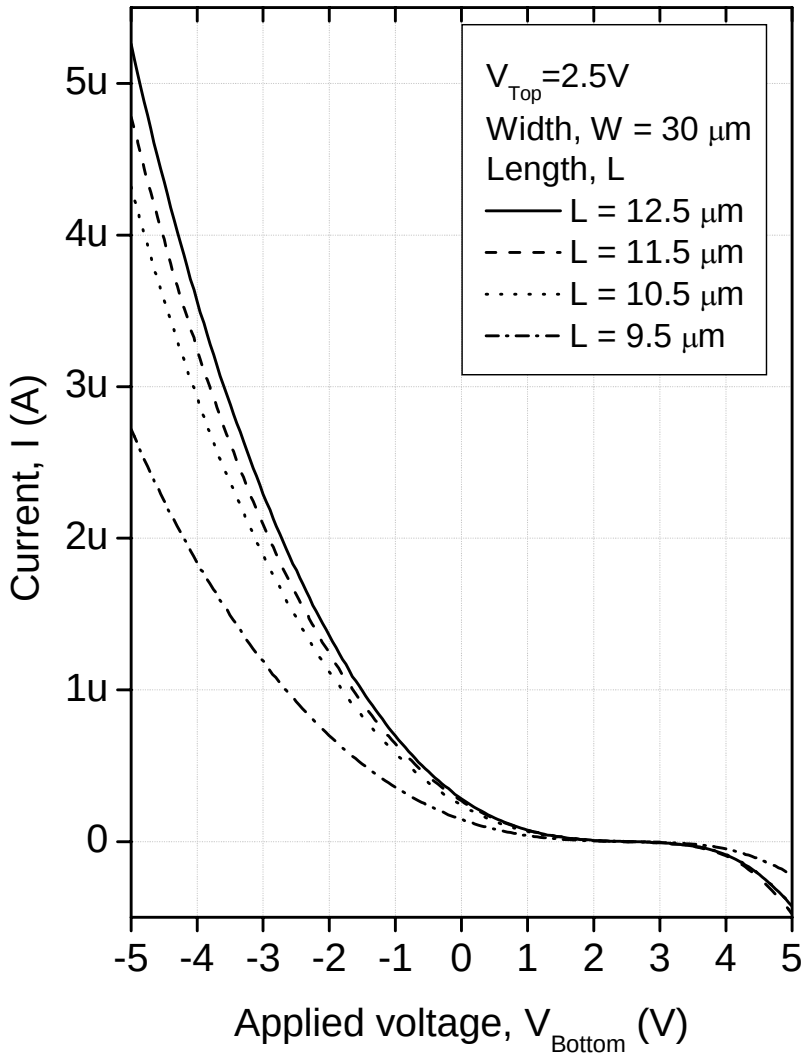


FIG. 2-11. Current-voltage transfer characteristics of MIS switching devices fabricated by sputtered silicon oxide, intrinsic silicon, and n^+ silicon.

2.3 Gate dielectric (II); silicon nitride (SiN_x)

2.3.1 Background

TFTs have a unique capability of being fabricated on a wide variety of substrates, even on plastic substrates. Currently, many researchers are focusing on developing flexible display devices for electronic books and wearable displays.[56] In addition to electronic display devices, TFTs on various substrates are actively being studied for bio-sensing and bio-interfacing microelectronic devices.[15] The most serious issue in fabricating TFTs on plastic substrates is that all of the fabrication steps have to be processed at low temperature, for instance below 150 ^{o}C for polyethylene terephthalate (PET) substrates. Plasma enhanced chemical vapor deposition (PECVD) is widely used for the deposition of semiconducting and dielectric thin films because of their adequate film properties and a capability for mass production. However, as PECVD deposition temperature decreases below 200 ^{o}C, one serious problem is particle formation from unstable byproducts resulting in eventual device failure such as a line open, exposure failure, and dielectric breakdown. In addition to particles, PECVD systems employ toxic gases such as SiH_4 and PH_3 and require equipment for burning and handling unreacted process gas. This can impose significant increases in equipment and maintenance costs with increasing substrate size. On the other hand, sputter deposition is an attractive alternative for deposition at low temperature relative to conventional PECVD and even room temperature.[57] Sputter deposition generates fewer particles at low temperature due

to its physical deposition characteristic and does not require toxic gases. If some particles are induced during the sputter deposition, the particles can be removed almost completely by adopting a horizontal sputtering scheme where the substrate and target are aligned parallel to each other and perpendicular relative to gravity. In addition to particle and toxic gas issues, the uniformity of PECVD thin films, the most important process factor for large-sized substrate applications, is typically degraded at lower temperature and larger substrate size. On the other hand, sputter deposition overcomes this serious issue by adopting a scanning (or passing) sputtering scheme with long rod-like targets and high density plasma (HDP) sources. It was reported that the thickness uniformity of a sputter deposited film is below 5 % on 1200 x 1300 mm substrate size at room temperature.[58] Consequently, for large-sized substrates, the scanning and horizontal sputtering mode of sputter deposition is utilized to improve the thin film uniformity and remove the particles on the substrate at the same time. The major process issue for low temperature TFT fabrication with fully sputter deposited films is how to overcome the poor thin film quality. In this work, we have characterized the electrical and optical properties of sputter deposited silicon nitride (SiN_x) as a function of DC substrate bias during sputter deposition.

2.3.2 Experimental

The SiN_x dielectric thin film was characterized by measuring the current density and breakdown voltage as a function of substrate bias during sputtering. The samples for

the measurement were prepared by fabricating a metal-insulator-metal (MIM) structure; top-metal (Mo, 200 nm), insulator (SiN_x, 40 nm), and bottom-metal (Mo, 200 nm). The circular top-electrodes were pattered using a shadow mask consisting of 50 μm diameter apertures during the top electrode sputter deposition. The deposited SiN_x thickness was 40 nm and the fixed sputter parameters are 100 W RF power, 200 ^oC temperature, Ar-H_2 (25 sccm), N_2 (25 sccm), and 5 mTorr pressure. The schematic diagram of the sample preparation for this measurement is shown in Fig. 2-12.

2.3.3 Results and discussion

Fig. 2-13 shows the current densities and breakdown voltages with the change in the applied substrate bias and Fig. 2-14 is a plot of the change in the breakdown with substrate bias. As shown in the figures, the SiN_x film without substrate bias, as expected, has a very low breakdown field of about 2 MV/cm. The breakdown field of the SiN_x films increases with increasing substrate bias and has a maximum at 20 W (125 V) substrate bias with 7.65 MV/cm breakdown field. The increase in the breakdown field corresponds to a decrease in the deposition rate, which suggests that the SiN_x film is denser. This densification is likely due to reducing the number of vacancies and pores that is known to improve the dielectric strength of a material. The breakdown field decreases slightly again at higher substrate bias up to ~ 40 W (155 V). We speculate that at higher substrate bias the ion bombardment during SiN_x growth is too severe and starts to induce defect generation by preferential re-sputtering or creating point and line defects.

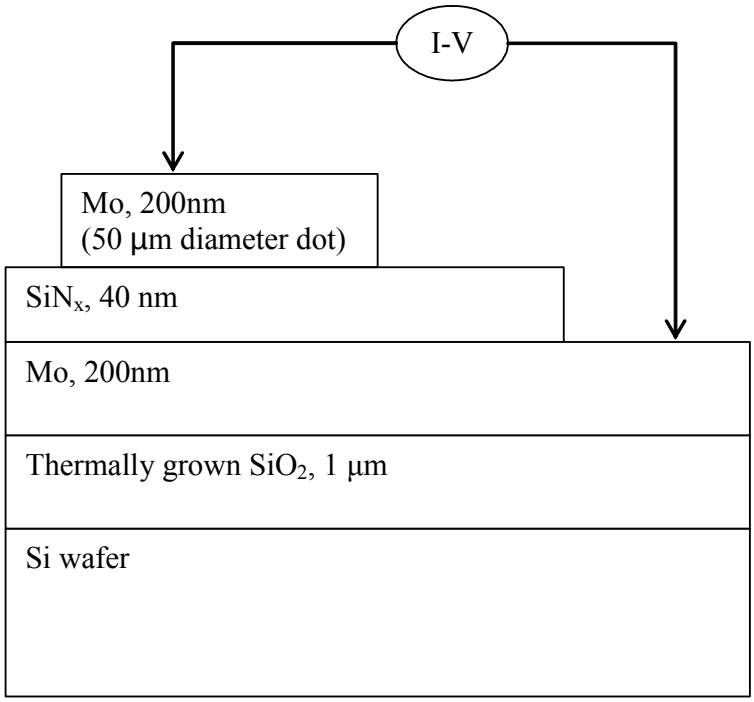


FIG. 2-12. Schematic diagram of sample preparation for current density and breakdown measurement.

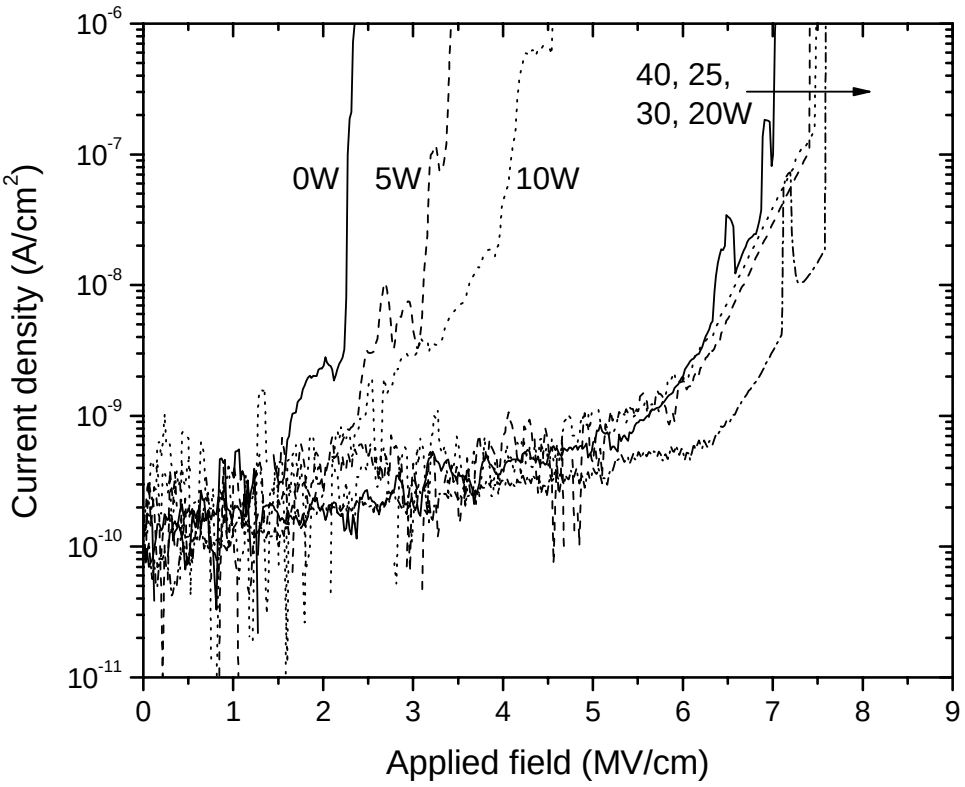


FIG. 2-13. Current densities versus applied field of sputtered SiN_x thin films as a function of DC substrate bias.

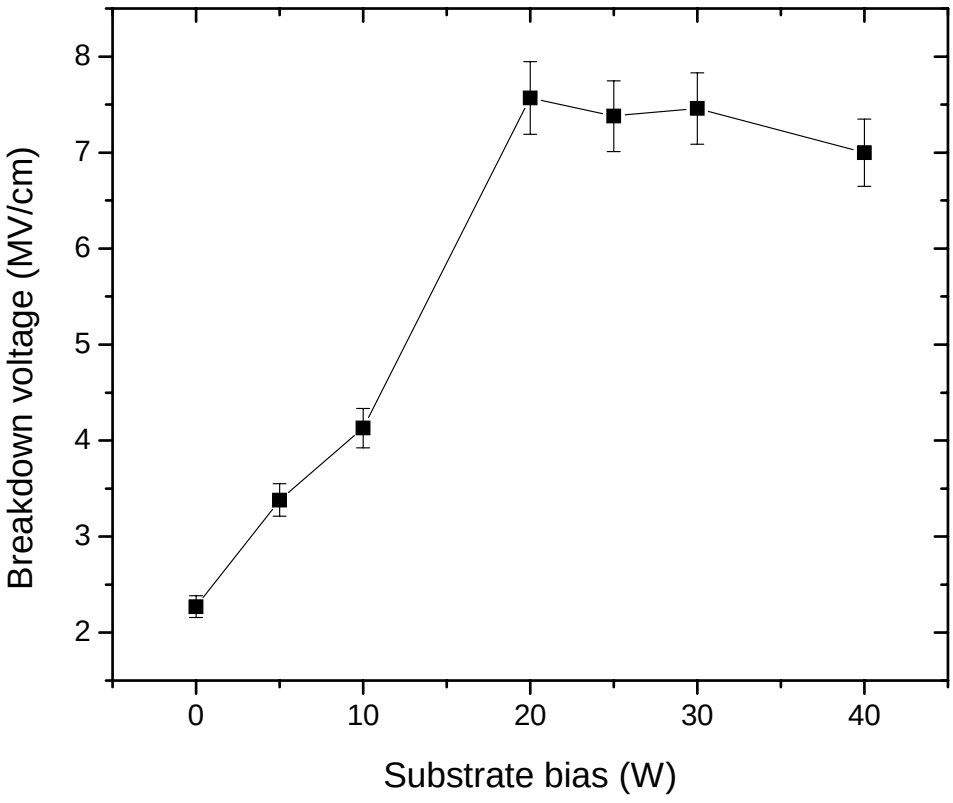


FIG. 2-14. The changes in breakdown field and deposition rate of sputtered SiN_x thin films as a function of substrate bias.

In previous work, it was demonstrated that the conductivity of molybdenum-tungsten (MoW) is enhanced by applying a moderate substrate bias, however, at excessively high substrate bias (45W) the conductivity decreased slightly.[52]

Fig. 2-15 shows the change in refractive indices of sputter-deposited SiN_x films as a function of N_2 / (Ar-H_2) sputtering gas ratio. All SiN_x films were prepared with the following conditions; 100 W RF power, 0 W substrate bias, 200 ^oC, 5 mTorr. The refractive index decreases from 2.82 to 1.92 (at 200 nm) with increasing nitrogen / (Ar+H_2) content from 0.1 to 2. T. Makino *et al* and E. Bustarret *et al* propose that the refractive index of Si_xN_y film can be represented as the bond-density-weighted linear combination of reference refractive indices taken at $y = 0$ and at $y / x = 4 / 3$.[59],[60]

$$\text{Refractive index, } n = \frac{[Si-N]n_{a-Si_3N_4} + [Si-Si]n_{a-Si}}{[Si-N]+[Si-Si]}$$

where [Si-N] and [Si-Si] are absolute bond densities per unit volume. The experimental refractive indices of a-Si_3N_4 and a-Si are 1.9 and 3.3 respectively.[59] The refractive index of SiN_x, as shown in Fig. 2-15, decreases to 1.9 with increasing nitrogen gas ratio (>1.0) in the visible wavelength range. It is assumed that the [Si-N] bond density also increases with N_2 addition in the sputter deposition resulting in the decrease in refractive indices of SiN_x films. Fig. 2-16 shows the deposition rate and refractive indices of sputter-deposited SiN_x films as a function of DC substrate bias. The refractive indices of SiN_x are virtually constant with the change in substrate bias even at zero substrate bias. We can speculate that the DC substrate bias does not significantly affect the optical properties (Si-N bond densities) of SiN_x films and the electrical properties are enhanced due to the densification and low defect densities by applying the substrate bias.

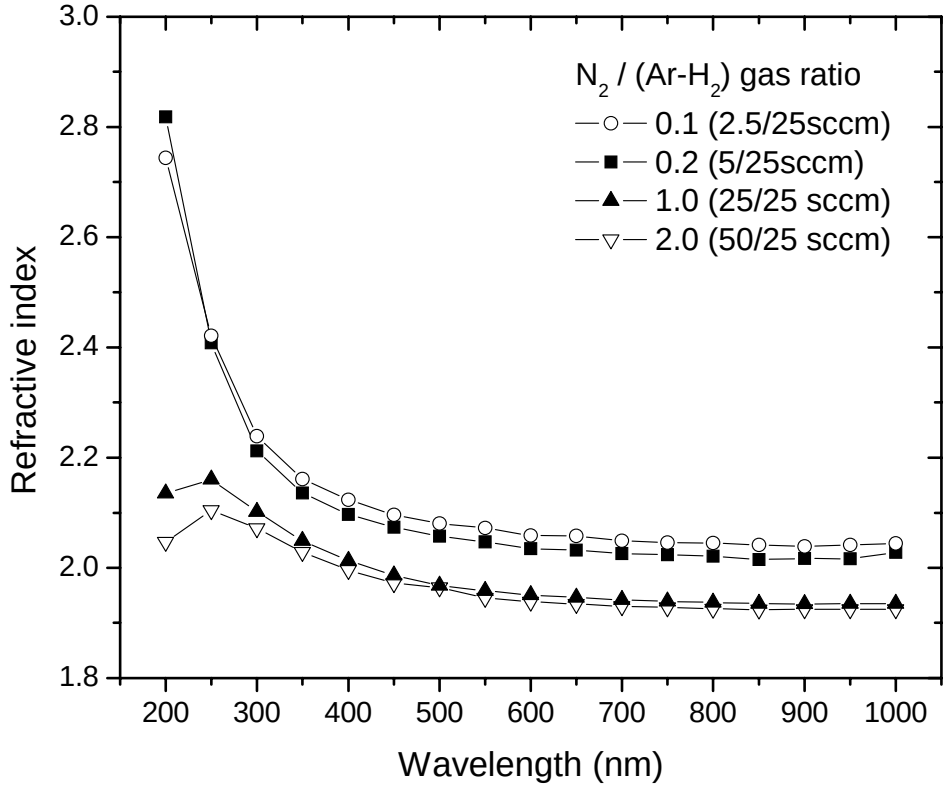


FIG. 2-15. The change in refractive index of sputter-deposited SiN_x films as a function of the N_2 / (Ar-H_2) sputtering gas ratio.

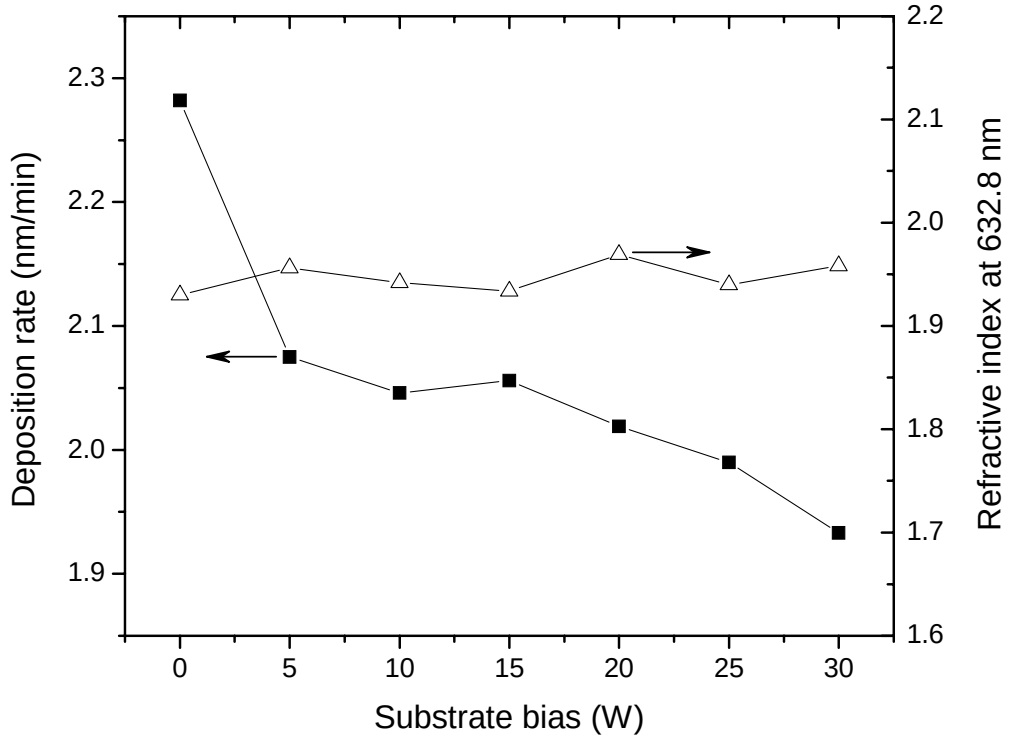


FIG. 2-16. Deposition rate and refractive index of sputter-deposited SiN_x films as a function of DC substrate bias during the sputter deposition.

2.3.4 Conclusion

In summary, the breakdown field of sputter-deposited SiN_x films is considerably enhanced by applying substrate bias during the sputtering deposition. The maximum breakdown field is 7.65 MV/cm with 20 W (125 V) substrate bias and the breakdown voltage slightly decreases at higher substrate bias up to ~ 40 W (155 V) due to increasing the number of defects caused by severe ion bombardment during SiN_x deposition.

2.4 Semiconductor (I); hydrogenated intrinsic amorphous silicon (a-Si:H)

2.4.1 Background

Amorphous silicon (a-Si) sputter deposition has been studied for the semiconducting layer of thin-film transistors (TFTs) and solar cells.[61] Sputter deposition is particularly attractive for low temperature large area fabrication processes on transparent, flexible, and plastic substrates.[49],[62] Sputtered a-Si films, however, typically have high trap densities which result in high off-state current when driving microelectronic devices.[57] For this reason, reasonable quality devices have not been demonstrated for sputter-deposited a-Si films. J. R. Abelson, *et al* studied the electrical and microstructural properties of sputter-deposited a-Si at ~350 ^{o}C.[57] In spite of having low defect densities compared to other research results, the films were deposited at even higher temperatures than what flexible display applications will allow. To achieve a low

temperature deposition process and high device performance, a polycrystalline silicon technology has been developed by annealing sputtered a-Si films.[63] In this study, a-Si films were initially deposited on flexible substrates by RF magnetron sputtering at low temperatures (as low as room temperature), and then, the a-Si films were crystallized by excimer laser annealing. The flexible substrate is not thermally degraded since the excimer laser anneals only the top surface of the a-Si films. Even though the quality of the films is high, the excimer laser anneal process is complex and costly. Consequently, it is desirable to obtain high quality a-Si thin films without any post-treatment, and low temperature sputter deposition is a logical candidate.

It is well known that direct current (DC) substrate bias makes thin films denser and can reduce defects, which can have a pronounced effect on the electrical properties of thin films. That is, thin films can be densified, and thus have a void-free microstructure even when deposited at room temperature by applying a substrate bias. We recently studied the effects of substrate bias on rf-sputter-deposited MoW [52] electrodes and SiO_2 [64] and SiN_x [65] insulators.

In this work, we evaluated the electrical properties of rf-sputter-deposited a-Si films with a substrate bias to show the effect of substrate bias on the electrical properties of a-Si films. Finally, to verify the effect of substrate bias, thin film transistors were fabricated with sputter-deposited a-Si with and without a substrate bias and their electrical characteristics were compared.

2.4.2 Experimental

An AJA ATC2000 RF magnetron sputtering system, equipped with four magnetron sources and a heated and/or DC biased substrate holder, was utilized for the a-Si thin film deposition (Fig. 2-2). The base pressure before the sputter deposition was below 5.0×10^{-5} Pa and the process pressure was 0.4 Pa with a mass flow rate of argon-hydrogen (5% H_2) fixed at 25 standard cubic centimeters per minute (sccm). The Si sputtering target has a 50 mm diameter and a 6 mm thickness. The film thickness was measured using a reflectometer (Filmeterics F20/40, Advanced Thin-Film Measurement System). The electrical properties were measured using an HP 4156A, Precision Semiconductor Parameter Analyzer. All reported property values are an average of ten measurements for each sample.

2.4.3 Results and discussion

Fig. 2-17 shows the current-voltage characteristics for the a-Si films grown in Ar-H_2 as a function of applied substrate bias. To observe the effects of hydrogen in the sputtering gas, an additional zero-bias film was sputter-deposited in pure Ar. The current of the a-Si film sputtered in an argon-hydrogen (5%) gas is lower than that of films sputtered in pure argon gas. It is well known that hydrogen atoms play an important role in a-Si:H films by compensating for defects such as dangling bond, vacancies, and

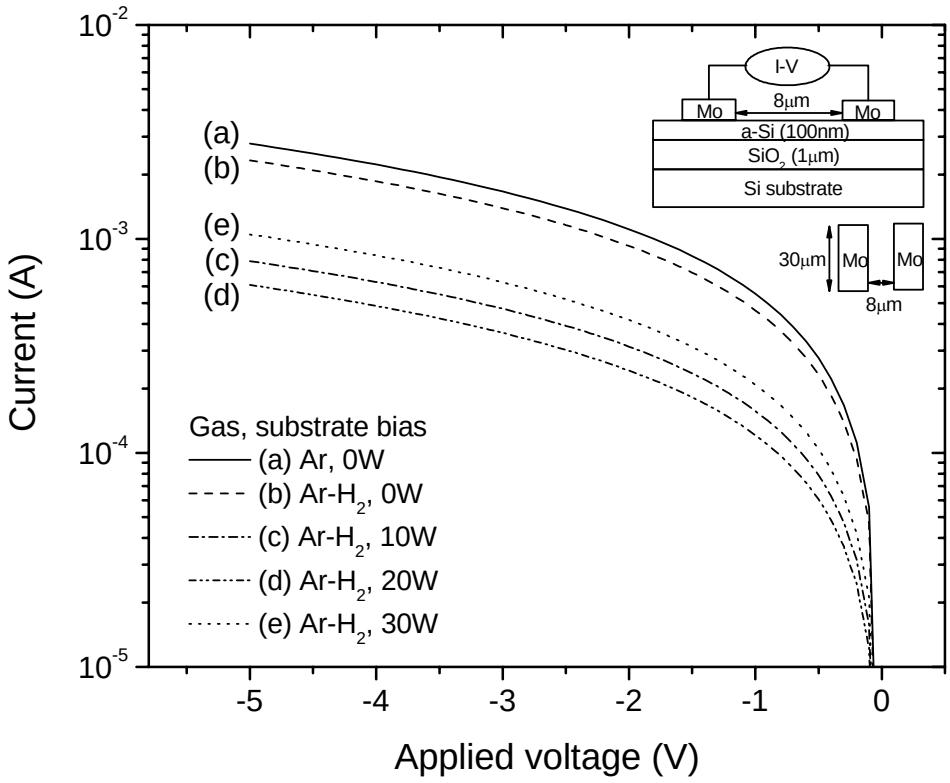


FIG. 2-17. Current-voltage characteristics of sputtered a-Si thin films in Ar (zero bias) and Ar-H_2 as a function of DC substrate bias during sputter deposition.

dislocations.[22] These defects create energy levels near the conduction and valence bands which produce conduction paths for electrons and holes, respectively. This, in turn, effectively increases the current carried by the a-Si. Our previous study of the effects of substrate bias on sputter-deposited MoW films showed that biased films are denser and have fewer defects, which reduces the resistivity of the metal films.[52] In the case of a-Si, however, the thin films with fewer defects have a higher resistivity because, as mentioned previously, defects mediate conduction in semiconductors by providing energy states for carriers in an otherwise forbidden gap. In metal films, these defects scatter or impede electron conduction, resulting in higher resistivity.

Fig. 2-18 shows the current at -3 V and the deposition rate for various sputtering conditions; gas mixture and substrate bias. The deposition rate decreases with increasing applied substrate bias. The lower deposition rate indicates that the films are denser, which is a result of energetic ion bombardment during growth. Fig. 2-18 also demonstrates the correlation between the deposition rate (i.e., film density) and the resistivity of the films. The films with the lower deposition rate (denser films) correlate with the lower current at a -3 V bias. To verify the short range order in a-Si film, the reflectance spectroscopy analysis was performed as shown in Fig. 2-19. (a) is the reference reflectance from a single crystal Si wafer, (b) and (c) is annealed Si at 700 °C from biased and unbiased sputter deposition, respectively, (d) is PECVD a-Si deposited at 400 °C, and (e) is sputtered a-Si without substrate bias at low temperature (room temperature). As shown in the figure, the reflectance spectra from annealed a-Si deposited with substrate bias (b) shows the characteristic peaks which indicate a

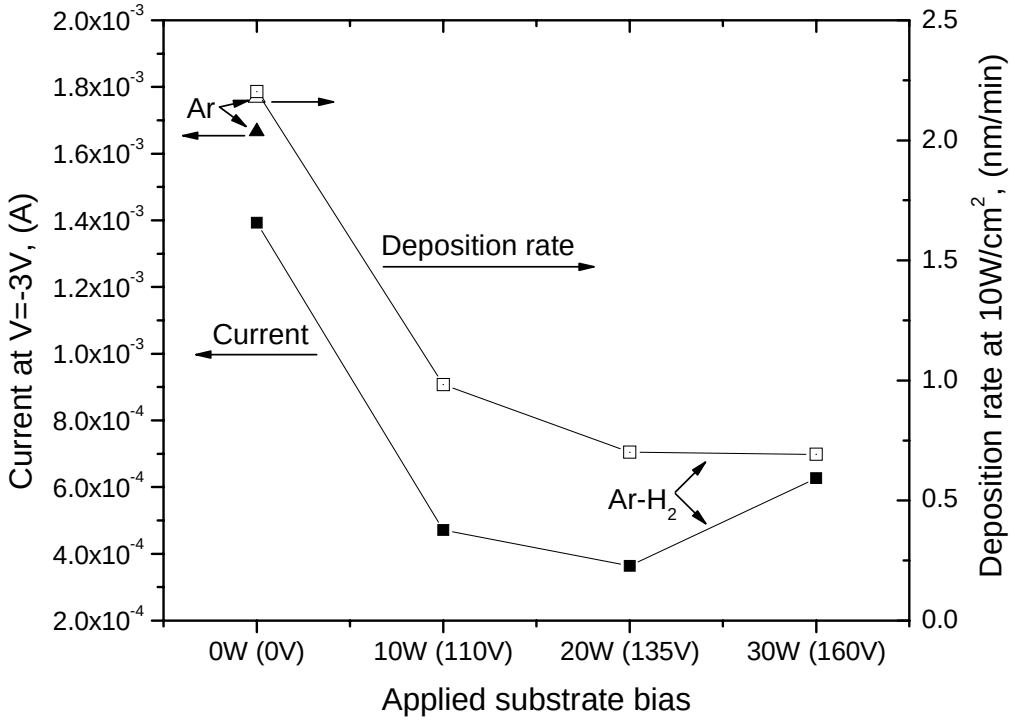


FIG. 2-18. Current (at –3V) and deposition rate changes as a function substrate bias for films sputter-deposited in Ar-H_2.

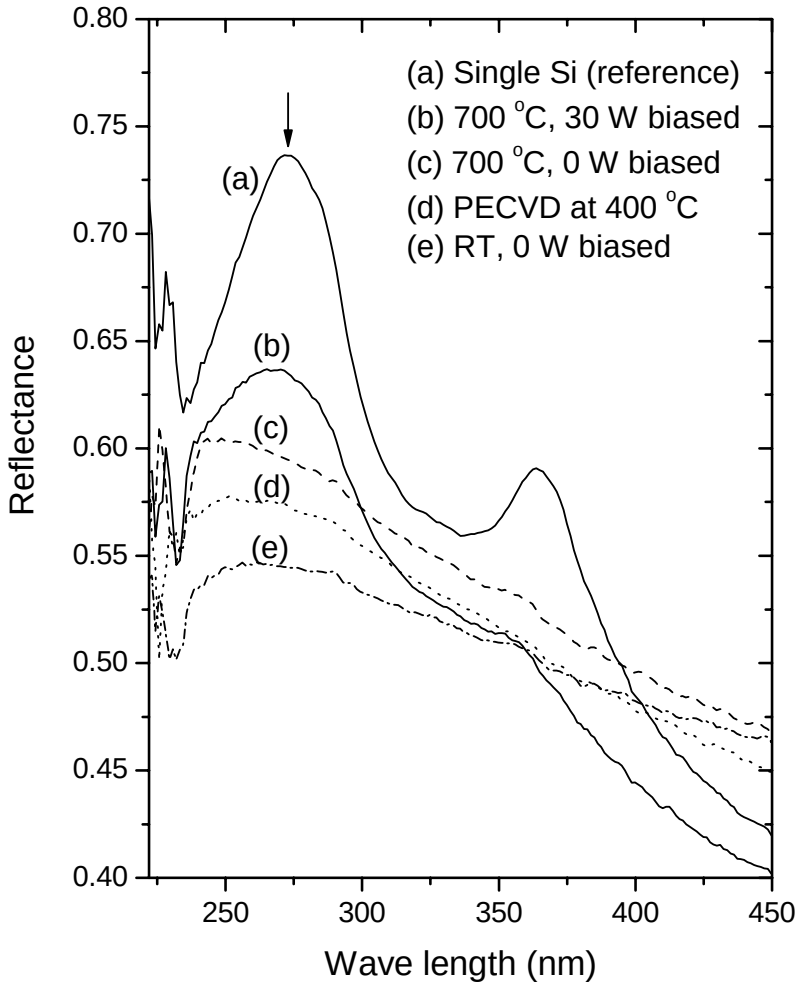


FIG. 2-19. UV reflectance spectra of Si films deposited by unbiased and biased sputter deposition at high temperature (700 °C).

recrystallization of a-Si. On the other hand, unbiased a-Si films (c, e) do not have any characteristic peaks indicating amorphous Si even for high temperature annealing (c). More detailed recrystallization properties of sputter deposited a-Si will be shown in section 3.4.

2.4.4 Conclusions

In conclusion, we surveyed and verified the effects of substrate bias on a-Si sputtered films. Biased a-Si films exhibit lower leakage current and a lower deposition rate because they are denser films with fewer defects as a result of the energetic ion bombardment that occurs during bias sputtering.

2.5 Semiconductor (II); extrinsic amorphous silicon (n^+ a-Si) for S/D ohmic contact

Fig. 2-20 shows the reflectance spectra of n^+ a-Si films with deposition conditions measured by Filmetrics thin film analyzer (F-20). The spectrum (h) is a single crystal (100) Si wafer for reference and has characteristic peaks at 273 nm and 360 nm which are closely related with direct optical transition at the critical points in crystalline Si.[66] The characteristic peaks indicate a short range order in Si and the intensity increases with an increase in the degree of crystallinity and Si-Si arrangement. Porous silicon for high efficiency photovoltaic cells, for instance, has a lower reflectance than that of crystalline or single Si.[67] In the case of amorphous silicon, broad and flat curves are obtained

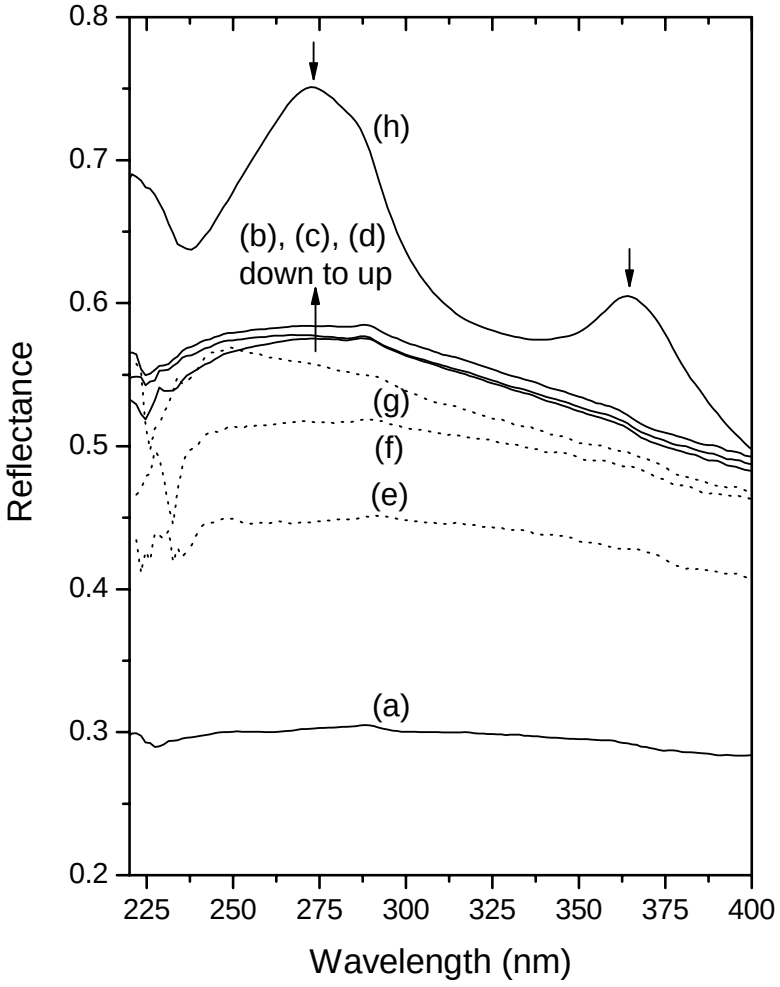


FIG. 2-20. UV reflectance spectra of sputter and PECVD deposited n^+ a-Si; 0W, 15W, 30W, 45W substrate biased sputter films. (a, b, c, d, respectively). PECVD n^+ a-Si, 1000, 2000, 3000 mTorr (e, f, g); Si wafer (h).

instead of the characteristic peaks in the crystalline Si. The reflectance spectra, both amorphous and crystalline Si, are strongly proportional to the absolute bond densities per unit volume of Si films.[59] The reflectance spectra of thesputter deposited n^+ a-Si films with biased and unbiased substrate and PECVD deposited n^+ a-Si films. All sample were prepared with 100 nm thicknesses of n^+ a-Si films on thermally oxidized silicon wafers (1 μm thick SiO_2). The sputter deposition parameters were 100 W RF power, 200 ^oC, 25 sccm Ar-H_2 , 5 mTorr pressure, and 0 W (a), 15 W (b), 30 W (c), 45 W (d) substrate bias. The PECVD n^+ a-Si deposition condition was $SiH_4/H_2/PH_3$ (40/7/70 sccm) gas flow rate, 350 ^oC, 200 W RF power, and 1000 mTorr (e), 2000 mTorr (f), 3000 mTorr (g) pressure. As shown in Fig. 2-20, the substrate biased sputter n^+ a-Si (b, c, d) shows higher reflectance than the unbiased film (a) and even higher than the PECVD films (e, f, g). To verify the effect of substrate bias on the electrical properties of n^+ a-Si films such as conductivity, the samples were prepared as shown in Fig. 2-21. The current between Cr electrodes across the n^+ a-Si films (100 nm thickness) were measured using a semiconductor parameter analyzer, HP 4156A. Fig. 2-22 shows the change of resistance (*dV/dI*) and reflectance as a function of the DC substrate bias. The resistance is drastically decreased with substrate bias and it indicates the number of defects such as vacancies that is one of the main sources of electron scattering is reduced by applying substrate bias resulting in higher conductivity n^+ a-Si films.

The conductivity of n^+ a-Si is enhanced by applying substrate bias and is attributed to densification and fewer induced defects in the films by the biased sputter deposition.

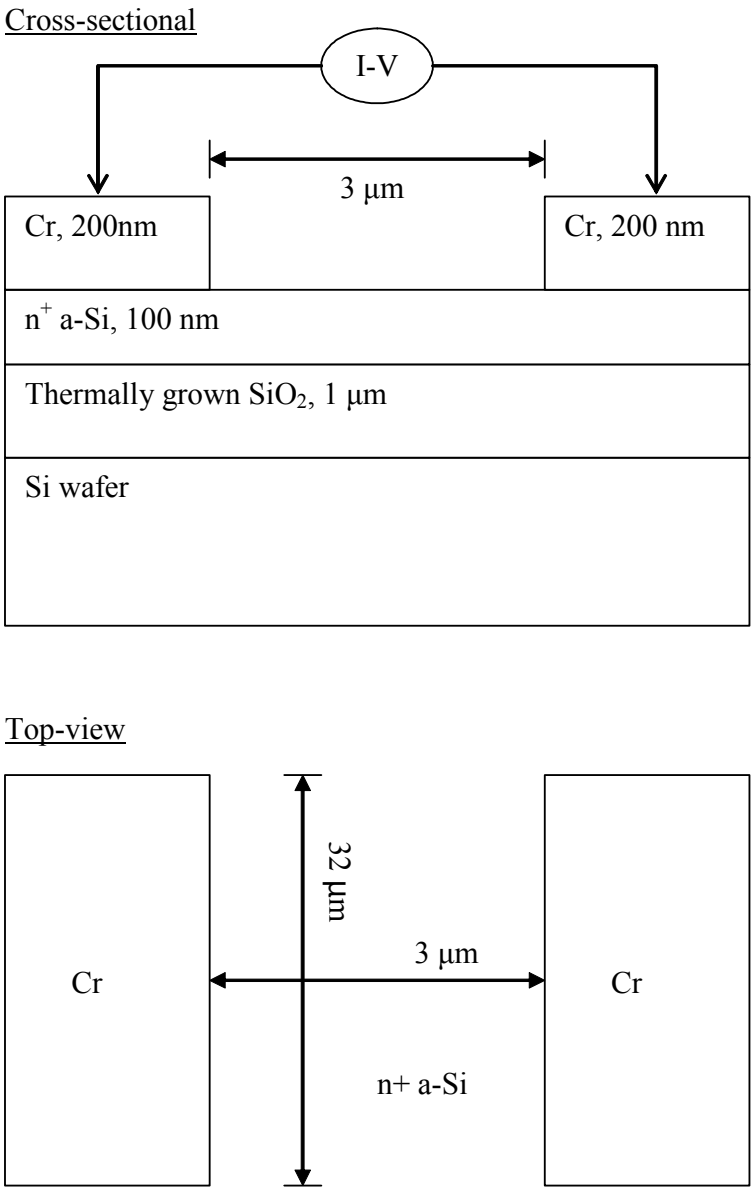


FIG. 2-21. Schematic diagram of sample preparation for resistance measurements of n^+ a-Si thin films.

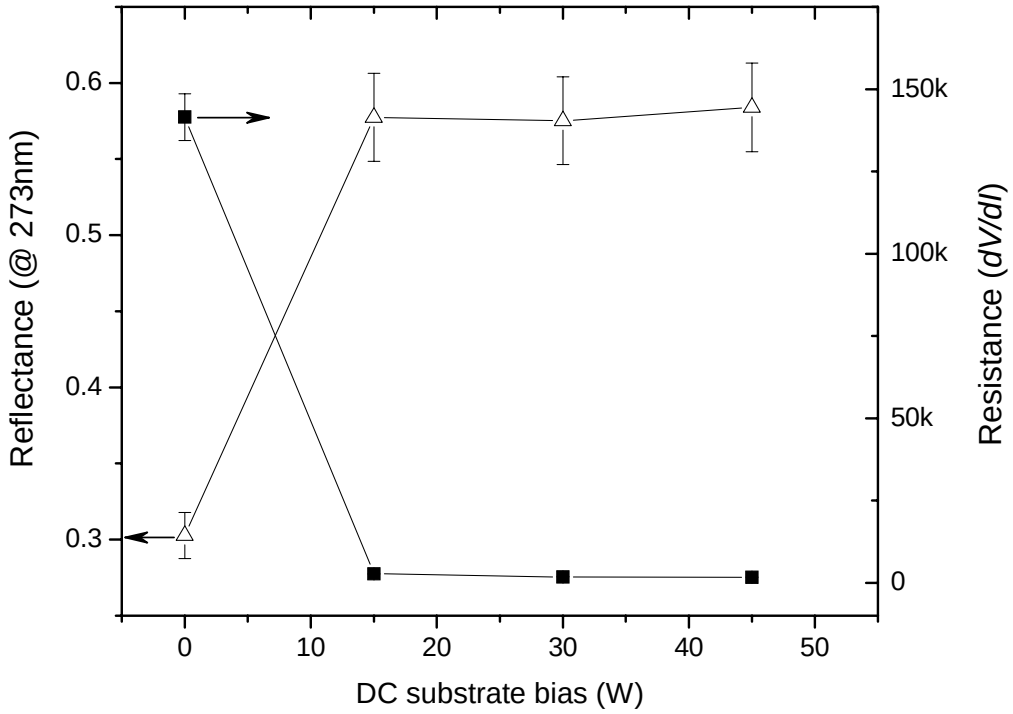


FIG. 2-22. The changes in reflectance and resistance of sputtered n^+ a-Si thin films as a function of substrate bias.

2.6 Low temperature crystallization of sputter deposited a-Si films

2.6.1 Background

Thin film transistors are widely used as a switching element for microelectronic applications and electronic display devices such as thin film transistor-liquid crystal displays (TFT-LCD).[68] Many applications are divided between two silicon TFT technologies which depend on the ordering of the semiconducting Si active region; hydrogenated amorphous silicon (a-Si:H) TFTs and polycrystalline silicon (poly-Si) TFTs. The a-Si:H TFT is currently utilized as a switching element for the most of TFT-LCD panels since it provides very stable properties and is suitable for mass production on glass due to its low temperature processing even though the field effect mobility is extremely low < 1 cm^2/V-sec. To improve the field effect mobility above 10 cm^2/V-sec up to 300 cm^2/V-sec for the applications of low power consumption, high driving speed, and integrated circuits on various low temperature substrates, the a-Si film is usually crystallized by post-annealing techniques such as solid phase crystallization (SPC),[69] metal induced crystallization (MIC),[70] metal induced lateral crystallization (MILC),[71] field aided lateral crystallization (FALC),[72] and excimer laser annealing (ELA).[73] In the case of MIC, a very small amount of metal such as nickel (Ni) or palladium (Pd) is used as a catalyst for the crystallization. The a-Si is crystallized under thermal annealing conditions and form an intermediate phase, a metal silicide, at lower temperature than intrinsic a-Si crystallization temperature ~ 650 °C. Even though MIC techniques have an

advantage in lower temperature processing as low as 300 °C, the electrical properties of TFT by MIC, for example threshold voltage and leakage current, are seriously degraded by metal residues in the channel region inevitably incorporated during the crystallization. In the case of MILC and FALC, the amount of metal residues in the channel region is extremely small because the lateral crystallization propagates from the metal-coated region (source / drain) to the uncoated channel region, however the crystallization temperature and crystallization time are relatively high, at least 500 °C and 5 hours for a 15 μm channel length. More recently, ELA has shown to be a very attractive crystallization technology since poly-Si crystallized by ELA has very large grain size with fewer defects relative to other techniques. This technology, however, is still not suitable for mass production since the shot speed is very slow due to the ~ 90 % overlapping exposure scheme required to improve the uniformity of the crystallized silicon. Furthermore, the processing cost of maintaining the large laser source is very high. To compensate the deficiencies of the aforementioned crystallization methods, a technique called continuous grain silicon (CGS) which combines ELA and MIC was recently introduced by Sharp and Semiconductor Energy Laboratory (SEL).[74] The process flow is very complicated and the net yield is very low due to the complex process scheme.

To better develop a lower temperature polycrystalline silicon process requires a fundamental understanding of the a-Si to poly-Si phase transition. Kimura *et al.* proposed that the crystallization characteristics of a-Si varies with the stress state of the as-deposited a-Si films.[75] The crystallization speed slows when the as-deposited a-Si is

under compressive stress which was induced with a silicon nitride (Si_3N_4) capping layer. Conversely, the crystallization speed is enhanced when the a-Si film is under tensile stress with a silicon oxide (SiO_2) capping layer. Hashemi *et al.* demonstrated a crystallization method called stress-assisted nickel-induced crystallization.[76] In this method, the crystallization properties of a-Si with a very thin nickel (Ni) film were varied with the effect of external stress imposed mechanically on an a-Si film. The crystallization temperature can be lowered and the speed enhanced by applying an external tensile stress on the a-Si films during the thermal annealing. On the other hand, the crystallization of a-Si with a compressive stress inhibits the a-Si crystallization mainly due to a buckling of the silicon network.

In our previous work, it was demonstrated that the properties of sputter deposited thin films such as metal [52], silicon oxide [64], and silicon [77] can be significantly changed with the addition of substrate bias during sputtering deposition. In this study, it will be demonstrated that that ion irradiation induced by substrate biased during sputter deposition of a-Si thin films enhances the kinetics of poly-Si nucleation even though the stress state of biased a-Si is highly compressive. It will be demonstrated that a-Si deposited with substrate biased sputter deposition can be crystallized at lower temperature with higher crystallization speed than intrinsic a-Si crystallization using conventional furnace annealing. If this approach can be extended to ELA, it could minimize thermal damage to the substrate and underlying thin films and could enable poly-Si TFT technology for use on commercial glass and flexible substrates such as soda-lime glass and plastic substrates, respectively. Additionally, the dehydrogenation process

after crystallization is not necessitated if only Ar gas is utilized during the a-Si sputter deposition.

To verify the effect of substrate bias on crystallization characteristics of a-Si sputter-deposited with and without DC substrate bias, we analyzed x-ray diffraction (XRD), Raman spectroscopy, and UV reflectance over a wide annealing temperature range. In addition to the quantitative analysis, the surface morphology of crystallized silicon measured with scanning electron microscopy (SEM) and atomic force microscopy (AFM) will be shown.

2.6.2 Experiment

An AJA ATC2000 RF magnetron sputtering system equipped with four magnetron sources and a heated and/or DC biased substrate holder was used for the a-Si film deposition.[52] The Si sputtering target has a 50 mm diameter and a 6 mm thickness with 99.999 % purity. The base pressure before the sputter deposition was below 4.0×10^{-5} Pa (3.0×10^{-7} Torr) and the process pressure was 0.666 Pa (5 mTorr) with a mass flow rate of argon-hydrogen (5% H_2) fixed at 25 standard cubic centimeters per minute (sccm). The RF power and deposition temperature for all were fixed at 200 W, 200 °C respectively and the substrate bias was 0 W (no substrate bias) and 30 W (215 V) during the deposition. The a-Si films were deposited on quartz substrates and the film thickness for all the samples was 500 nm. A quartz tube furnace was used for thermal annealing

and the conditions were atmosphere ambient and 600 °C to 900 °C every 100 °C for 20 hours.

2.6.3 Results and discussion

To verify the crystallinity of poly-Si after annealing, X-ray diffractograms of the annealed a-Si from 600 to 900 °C every 100 ^{o}C for 20 hours are shown in Fig. 2-23 and 2-24 collected by Philips X'Pert Diffractometer with an angle 2θ between 25° and 60° using $Cu_{K\alpha 1}$ X-ray with λ = 1.54056 Å in the θ-2θ and high resolution configuration (2θ = 0.01 step). The XRD result of crystallized Si without substrate bias, is shown in Fig. 2-23, and has a characteristic peak at 2θ = 28.5° corresponding to the (111) above 600 °C and the intensity of the XRD peak increases slightly with the annealing temperature. The intensity of the peak is very small and other characteristic peaks are not shown even high temperature annealing ~ 900 °C. We speculate that the crystallites are nanocrystalline with very small grain size. In contrast, the XRD spectra of crystallized Si deposited with substrate bias (30 W, 215 V), in Fig. 2-24, shows strong characteristic peaks at 2θ = 28.5°, 47.5°, 56.3° that correspond to (111), (220), (311), respectively. The intensity of crystallized Si deposited with substrate bias is much higher and sharper than those of crystallized Si deposited without substrate bias. Fig. 2-25 shows UV reflectance spectra of annealed a-Si deposited with and without substrate bias. The change in the profile and the shift in the peaks in the UV spectra indicate the modification of electronic density of states as a result of the long-range order. In the crystalline silicon, there are two main

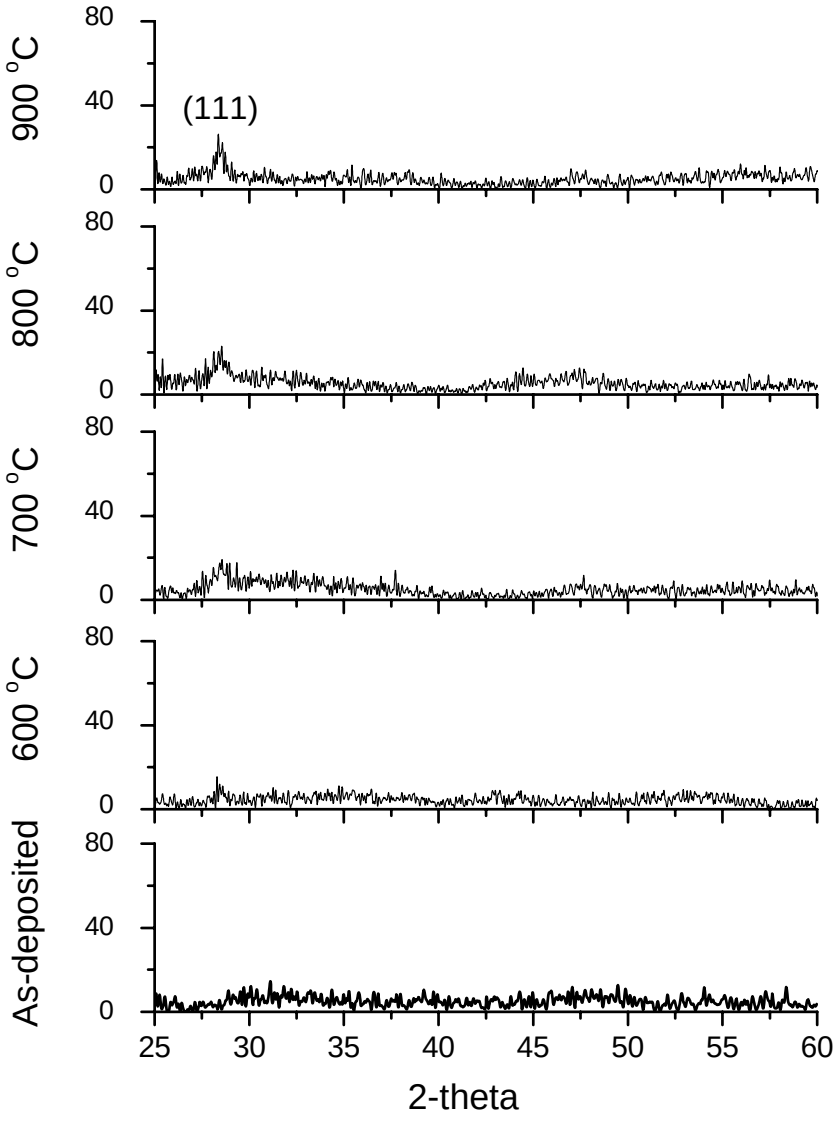


FIG. 2-23. XRD spectra of annealed Si films deposited by unbiased sputter deposition.

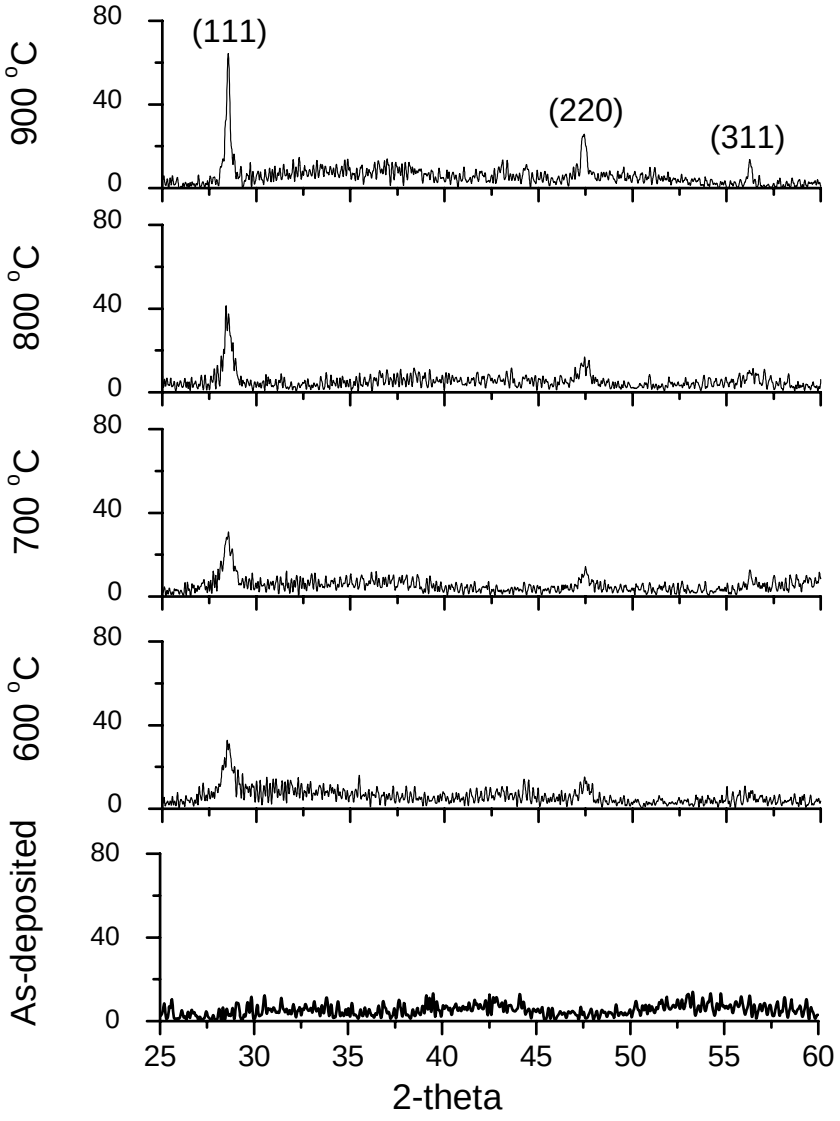


FIG. 2-24. XRD spectra of annealed Si films deposited by 30 W (215 V) biased sputter deposition.

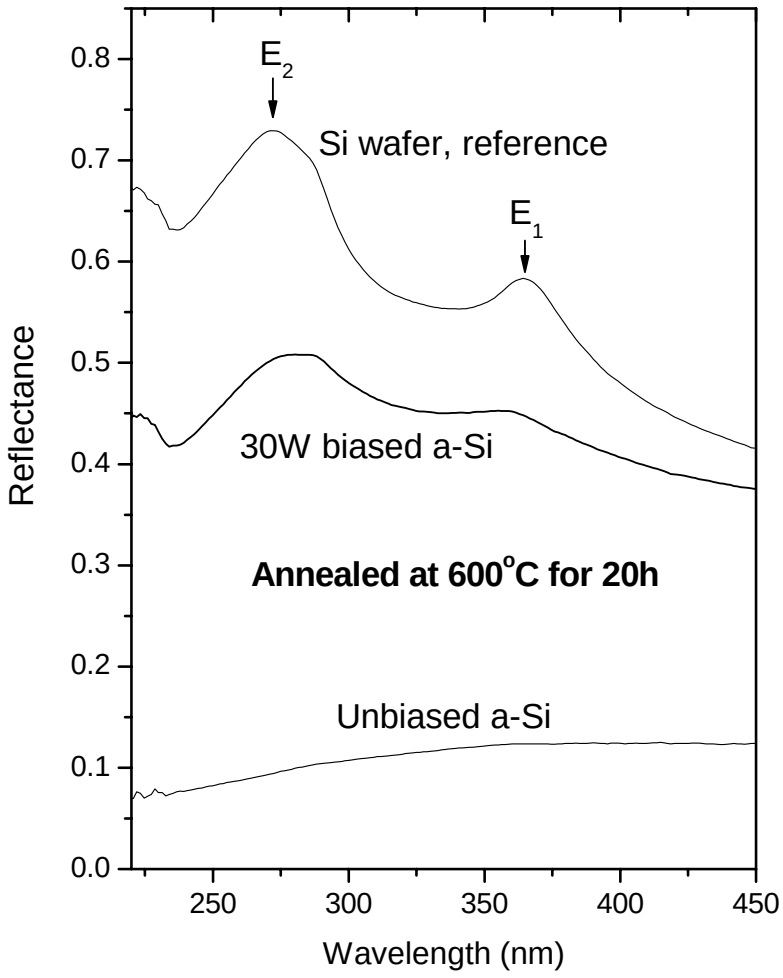


FIG. 2-25. UV reflectance spectra of annealed Si films deposited by unbiased and biased sputter deposition.

optical transition peaks; indirect transitions (E_1) at ~ 360 nm and direct transition (E_2) at ~ 273 nm, respectively.[78] As shown in the figure, the characteristic peaks at both 273 nm and 360 nm are clearly shown in crystallized Si deposited with substrate bias and though the intensity is lower it resembles the single Si reference spectrum. The characteristic peaks, however, are not observed in the annealed Si deposited without substrate bias, which indicates the Si film is almost amorphous or nanocrystalline at best.

Fig. 2-26 and 2-27 shows the Raman spectra obtained by Confocal micro-Raman Spectroscopy (Renishaw 1000 spectrometer). The crystalline fraction of poly-Si, χ was calculated roughly from the expression below,[79]

$$\chi = \frac{I_p}{I_p + \gamma I_a}$$

where I_p and I_a are integrated Raman scattering intensity of crystalline and amorphous silicon respectively, and γ is the ratio of the integrated Raman cross section for poly-Si to a-Si. Tsu *et al.* suggested the value of γ is 0.88 when the grain size or crystalline fraction is small.[79] The crystallinity of the Si films with biased and unbiased sputter deposition at 600 °C for 20 hours, as shown in Fig. 2-26, is 0.61 and 0.48, respectively. The net crystallinity of crystallized Si deposited by substrate bias, however, is likely higher than this calculation result because the grain size of the poly-Si is large and thus the γ value would be smaller than 0.88 that was used in the calculation (Fig. 2-28).

The Raman spectrum for the unbiased film annealed at 600 °C for 20 hours, has two characterized peaks; a sharp poly-Si peak at 520 cm^{-1} and a broad Raman shifted a-Si peak at 480 cm^{-1}. On the other hand, the crystallized Si from the 30 W biased a-Si film has only a sharp characteristic peak at 520 cm^{-1} representative of poly-Si. In the case of

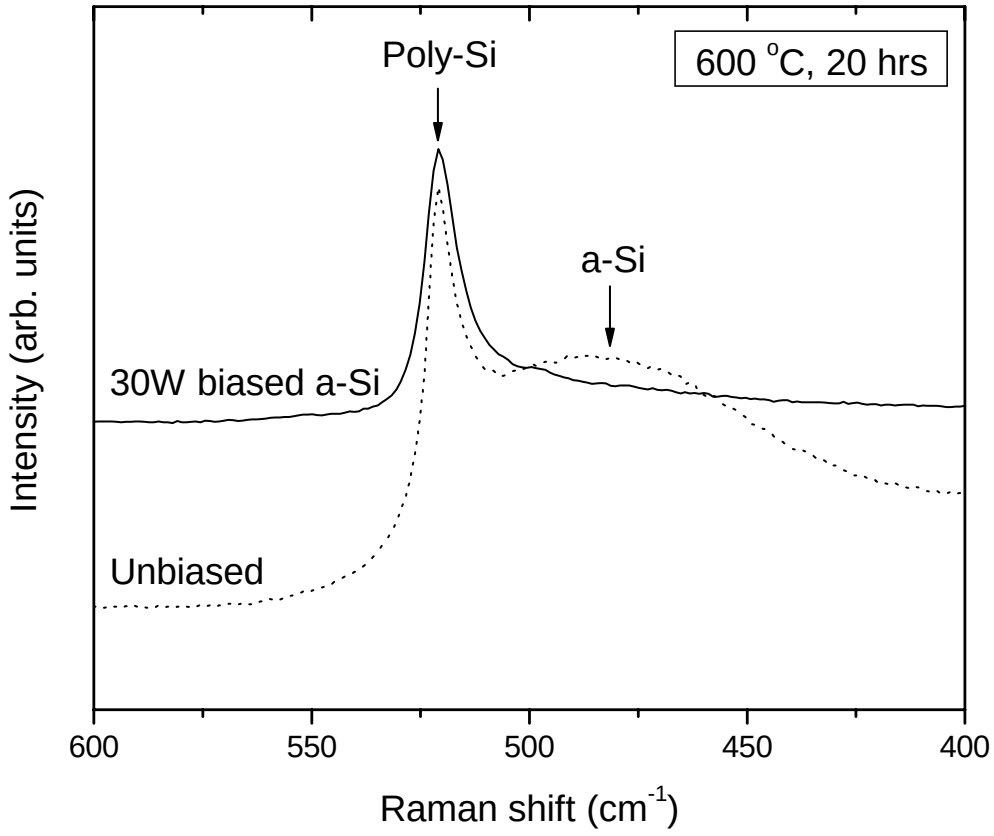


FIG. 2-26. Raman spectra of annealed Si films deposited by unbiased and biased sputter deposition. (annealed at 600 °C for 20 hours).

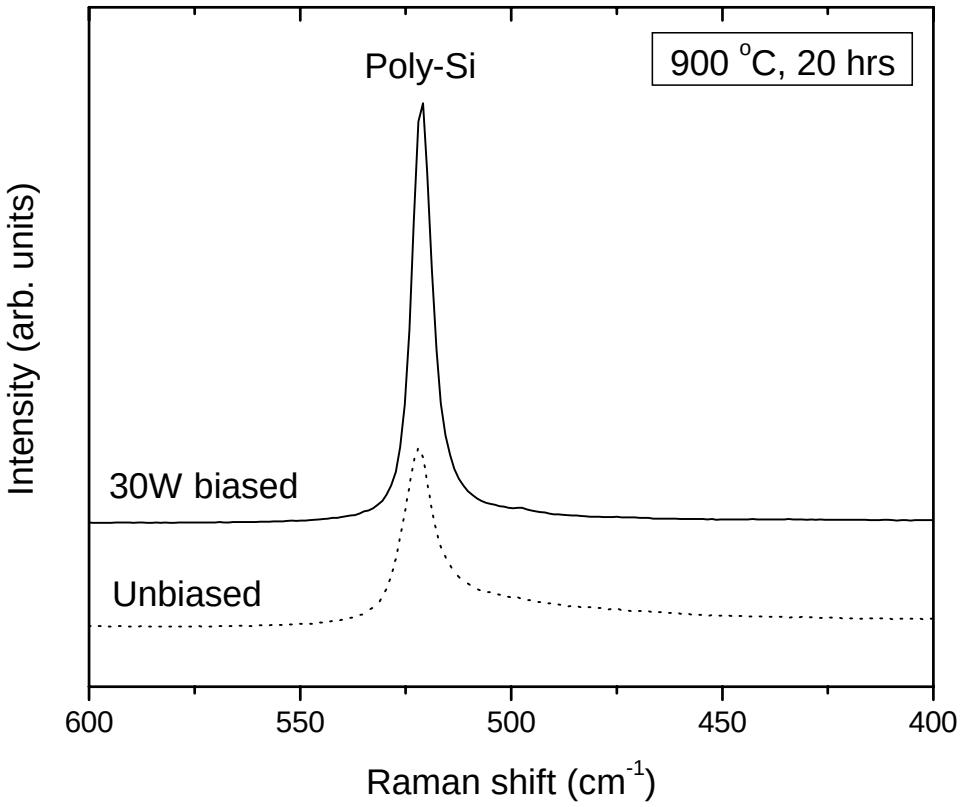


FIG. 2-27. Raman spectra of annealed Si films deposited by unbiased and biased sputter deposition. (annealed at 900 °C for 20 hours).

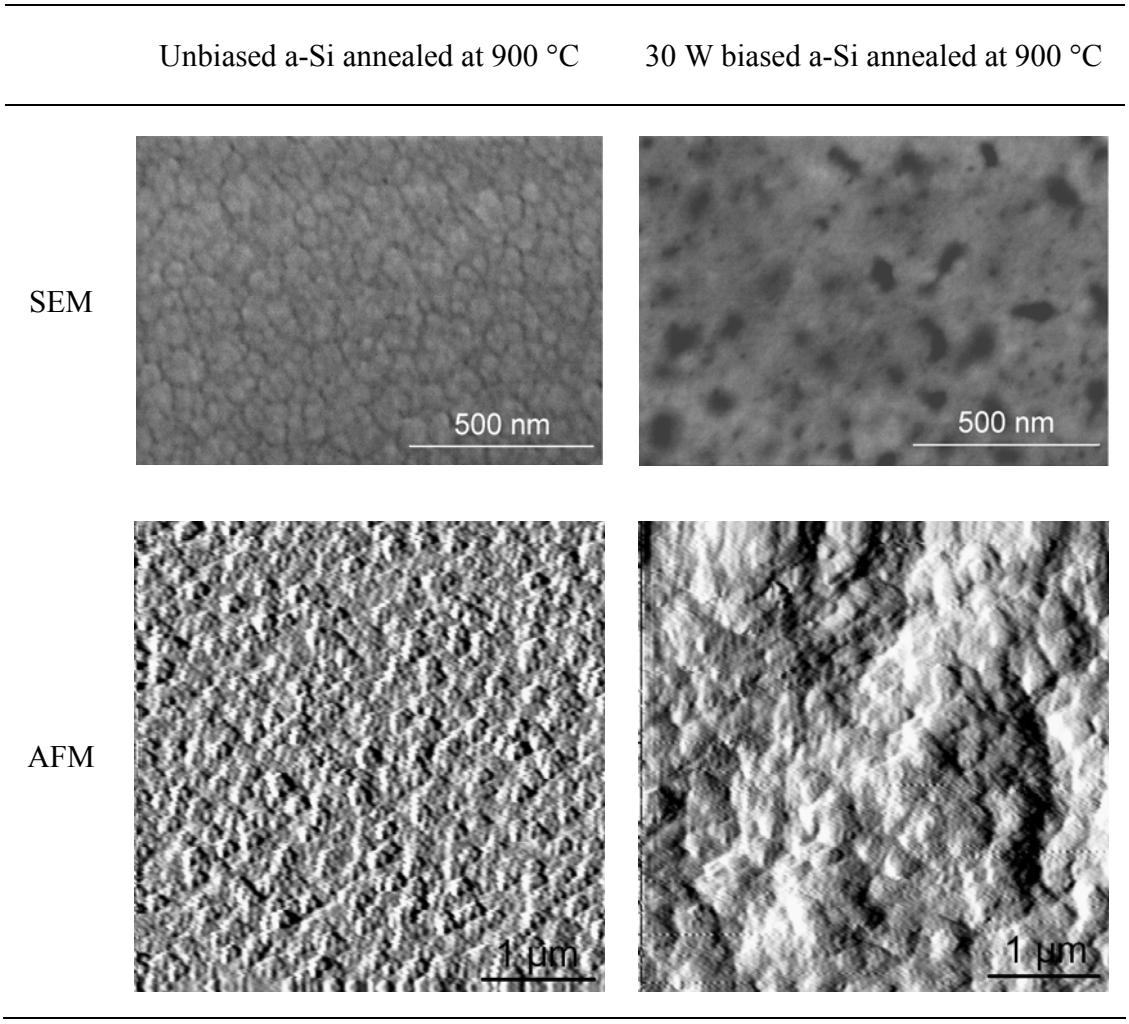


FIG. 2-28. Surface morphology of annealed Si films taken by SEM and AFM.

900 °C (20 hours), the a-Si peak is not shown in both crystallized films but the biased poly-Si film has a sharper and narrower peak than that of the unbiased film indicating the biased film is more crystalline under same annealing condition (Fig. 2-27).

To compare the microstructure of crystallized Si deposited with and without substrate bias, the surface morphology of the two films taken by SEM and AFM is shown in Fig. 2-28. The a-Si films were annealed and crystallized by SPC at 900 °C for 20 hours in atmosphere ambient of quartz tube furnace. The poly-Si film from substrate biased sputtering, as shown in the figure, has more condensed and larger grain size than those of the unbiased poly-Si film. Lager grain sized poly-Si is more desirable to fabricate poly-Si TFTs since larger grains have less electron scattering than smaller grains resulting and higher field effect mobility and lower threshold voltage.

In the crystallization of amorphous silicon, the phase transition from a-Si to poly-Si is processed via random nucleation of crystalline clusters surrounded by an amorphous phase. The nucleation and crystal growth kinetics are strongly influenced by impurities and defects in the amorphous Si film and these defects play an important role in the nucleation site. Spinella *et al.* suggested that ion irradiation induced by ion beam assisted deposition produces many kinds of internal defects such as vacancies and stacking faults within the amorphous network.[80] The free energy for the transition from a-Si to poly-Si, the driving force of the transition, is increased significantly as a result of the continuous defect generation in the a-Si network during the ion irradiation. Therefore, the thermodynamic barrier of nucleation is lowered and the nucleation kinetics is increased with ion bombardment of the deposited film. In the sputter deposition with substrate bias,

in general, the intense bombardment leads to the formation of larger amount of defects such as dislocations, vacancies, and stacking faults in the film relative to unbiased sputter deposition. These defects induced by ion irradiation are the main centers of nucleation and, as a result of the enhanced nucleation sites; the crystallization speed is increased and the crystallization temperature is decreased.

As we mentioned previously, in the case of tensile stress within or upon a-Si films, the residual elastic strain causes an increase in strain energy during the phase transition because the elastic modulus of poly-Si is larger than that of a-Si and then the difference of free energy between a-Si and poly-Si ($\Delta G_{a\text{-}Si \rightarrow poly\text{-}Si}$) is decreased by the transformation.[81] On the other hand, if there is residual or applied compressive stress in a-Si, the crystallization speed and temperature were compromised due to the buckling of the Si network.[75,76] Choi *et al.* showed the relative film density increases and the stress of film is highly compressed with increasing substrate bias during sputter deposition.[82] In this work, we showed the crystallization speed and temperature can be enhanced and lowered, respectively, by annealing substrates biased during a-Si deposition even if it is highly stressed compressively. This suggests that the enhanced number of nucleation sites induced by ion bombardment is a more dominant factor than the status of stress in low temperature crystallization of a-Si.

Chapter 3 Device processing issues

3.1 Design of photolithographic masks

Photolithographic masks were designed by Tanner L-Edit v8.3 based on an IBM PC. The processing issues on mask design will be described in this section with a process sequence of TFT-VACNF.

3.1.1 Mask design of alignment marks

GCA AutoStep 200 steppers is a system in which all masks and substrates are aligned to the optical column, but masks and substrates are not aligned directly to each other. Consequently, both masks and wafers require alignment marks. As shown in Fig. 3-1 (a), they are placed on the mask in specific locations to allow alignment of the mask to the optical column. The first level mask in a multilayer process must include special alignment marks on a base substrate wafer (normally thermally oxidized Si wafer) which match marks built into the stepper alignment microscope. Subsequent levels of lithography masks do not need alignment marks, unlike the case for contact aligner. There are mainly three kinds of alignment marks in using the stepper system; mask alignment marks, INSITU marks, and global alignment marks.

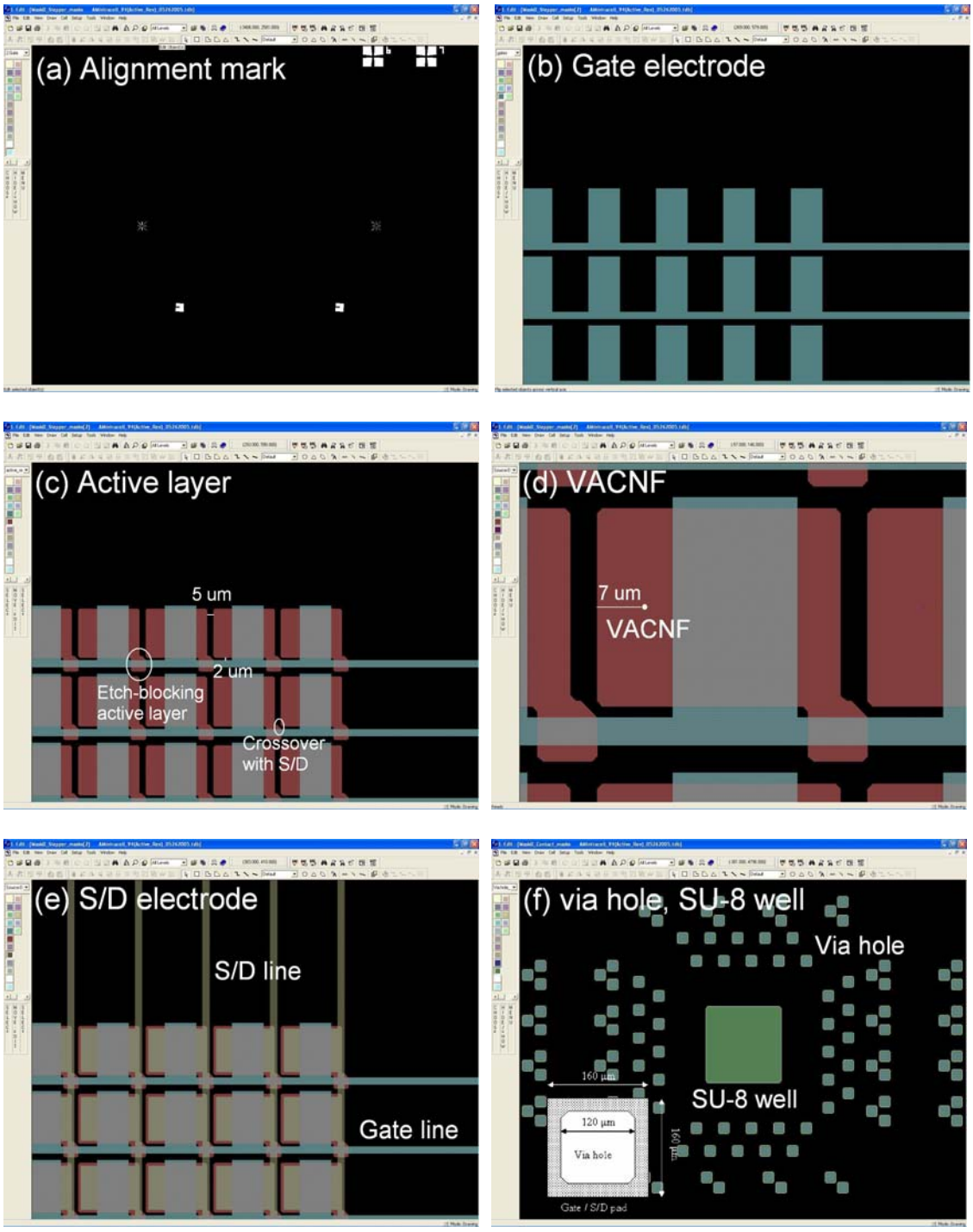


FIG. 3-1. Mask design for TFT-VACNF designed by Tanner L-Edit software.

3.1.2 Mask design of gate electrode

When designing the gate electrode, one needs to consider the critical dimension (CD) since the CD loss is usually > 1 μm if the electrodes are patterned by a wet chemical etch. The metal wet etch needs a higher over-etch ratio because of metal residues due to etch-byproducts called snow balls (or etch bubbles). Therefore, the gate mask must be designed with > 1 μm CD rule to compensate for the over-etch ratio. In the case of MoW gate, the gate is usually etched by dry etch based on SF_6/O_2 plasma with below ~ 0.5 μm of CD loss for 20 ~ 30 % over etch. The CD loss of Mo gate electrode patterned by wet etch, on the other hand, is very high usually 1.0 ~ 2.5 μm according to over etch. More CD loss causes narrow gate length resulting in high resistant electrode. Cr gate is usually has less CD loss (~ 1 μm) than Mo gate due to less hydrogen formation during etch process. One needs to make CD margin (1.0 ~ 1.5 μm) when designing the gate mask if one use either Cr or Mo gate electrodes. The designed length of gate line, as shown in Fig. 3-1, is 5 μm and the actual length of gate line will be ~ 4 μm (final inspection CD, FI CD) with 20 % over etch if Cr gate is used.

3.1.3 Mask design of active layer

In the case of using chrome (Cr) as gate and S/D electrodes, S/D etch is processed with acid based chemicals which can also attack the gate electrode if the active layer (n^+ a-Si / a-Si) is over etched resulting in a very thin gate dielectric (SiN_x) on the gate

electrode. The gate attack causes a gate-S/D short at the crossover area between gate and S/D lines. To prevent this gate-S/D short an etch-blocking buffer active layer on the area between gate and S/D line is essential when the active mask is designed. The blocking area must be designed with a polyhedral angle since it is a crossover area with S/D and gate electrode on which the step height of all layers is very high (~ 900 nm) from gate to S/D electrodes resulting in S/D open if the etch-blocking active is not designed well.

3.1.4 Mask design of VACNF

In the VACNF mask design, enough distance between the VACNF and the edge of S/D is required because the height of VACNF is several microns which can result in pattern distortion during photolithography. The distance from the VACNF to the S/D edge, as shown in Fig. 3-1 (d) and 3-2, must be at least 5 μm as observed during the inspection after the catalyst dot lithography. The designed diameter of VACNF dot was 0.5 μm and resulting diameter of grown VACNF was ~ 1.0 μm (Fig. 3-2). The standard VACNF mask is negative type which the VACNF area is a clear opening in the chrome background of the mask since VACNF patterning is processed by lift-off process with the negative mask.

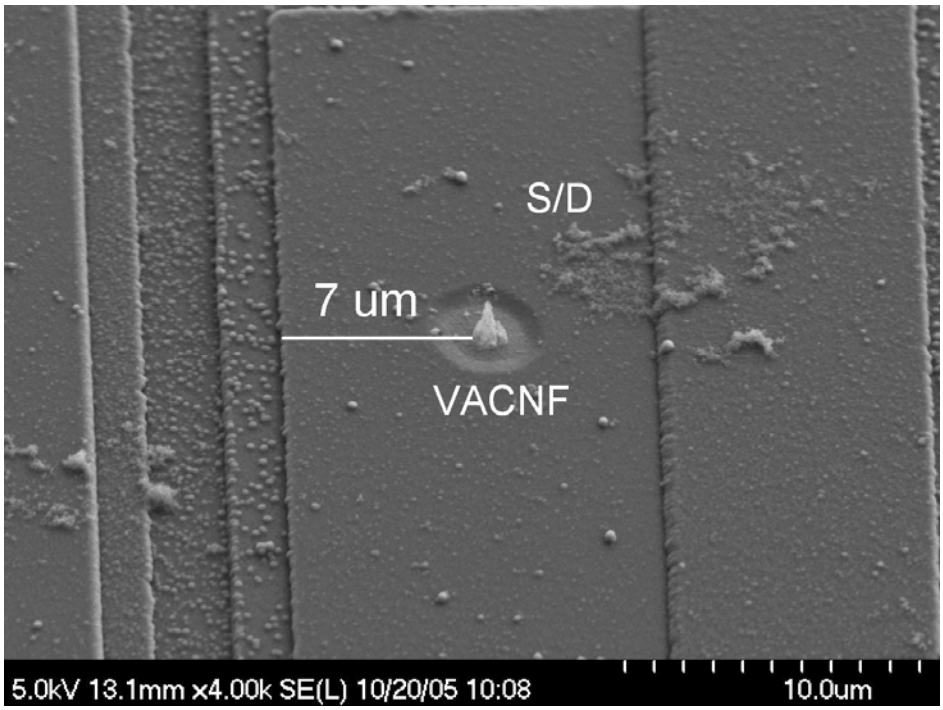


FIG. 3-2. Distance margin between VACNF and the edge of S/D electrode for precise S/D patterning. (No distortion in S/D patterning).

3.1.5 Mask design of S/D electrode

The actual length (FI CD) of S/D line should be higher than 3 μm if 300 nm Cr S/D is used since Cr has much higher resistance than other low resistant metals such as Al, Mo, and W. When designing S/D electrode, one have to consider and determine the channel length and width of TFT in active area. As the channel width increases, the on-state current also increases but pixel density is inversely decreased. The channel length is also important factor in designing TFT. The field effect mobility and on-state current is enhanced with decreasing the channel length but there is high possibility of S/D short with much narrowed channel length. Desirable channel length and width are 3 ~ 5 μm length and 25 ~ 35 μm width if considering TFT properties and process margin at the same time.

3.1.6 Mask design of passivation (via contact hole) and SU-8 well

When designing via hole mask for patterning passivation, CD bias also must be considered. The over etch ratio is over 50 % even 100 % if the passivation is etched by BOE wet etch and the CD bias will be above 1.0 μm each side of via hole (total at least 2 μm for both sides). The mask was designed as 40 μm of CD margin with S/D (gate) electrode and via hole as shown in Fig. 3-1 (f). That is, the length of gate and S/D pads is 160 μm and the length of via hole is 120 μm. The SU-8 well for storing electrolyte can be defined with the via hole mask on same mask design.

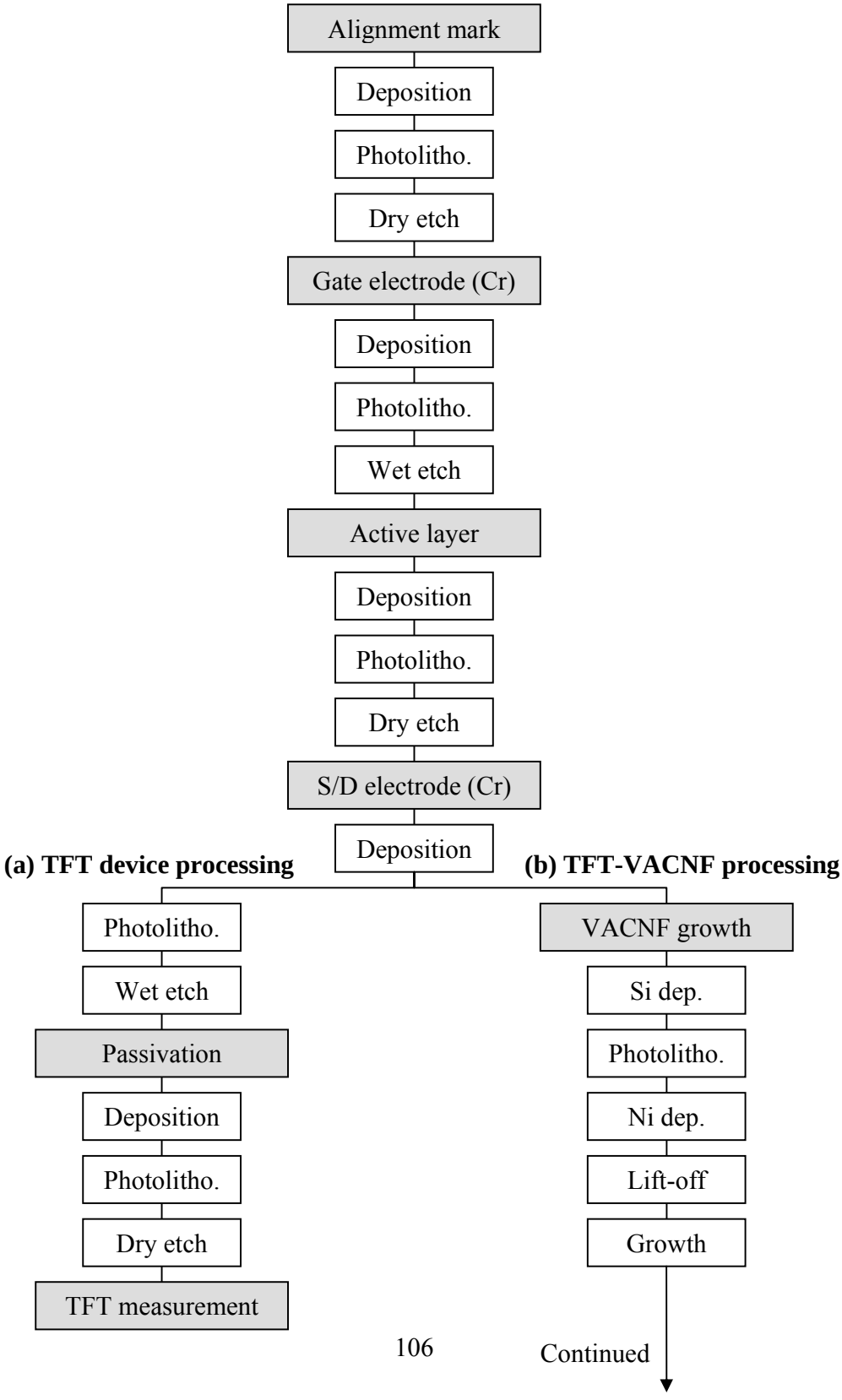
3.2 TFT device processing

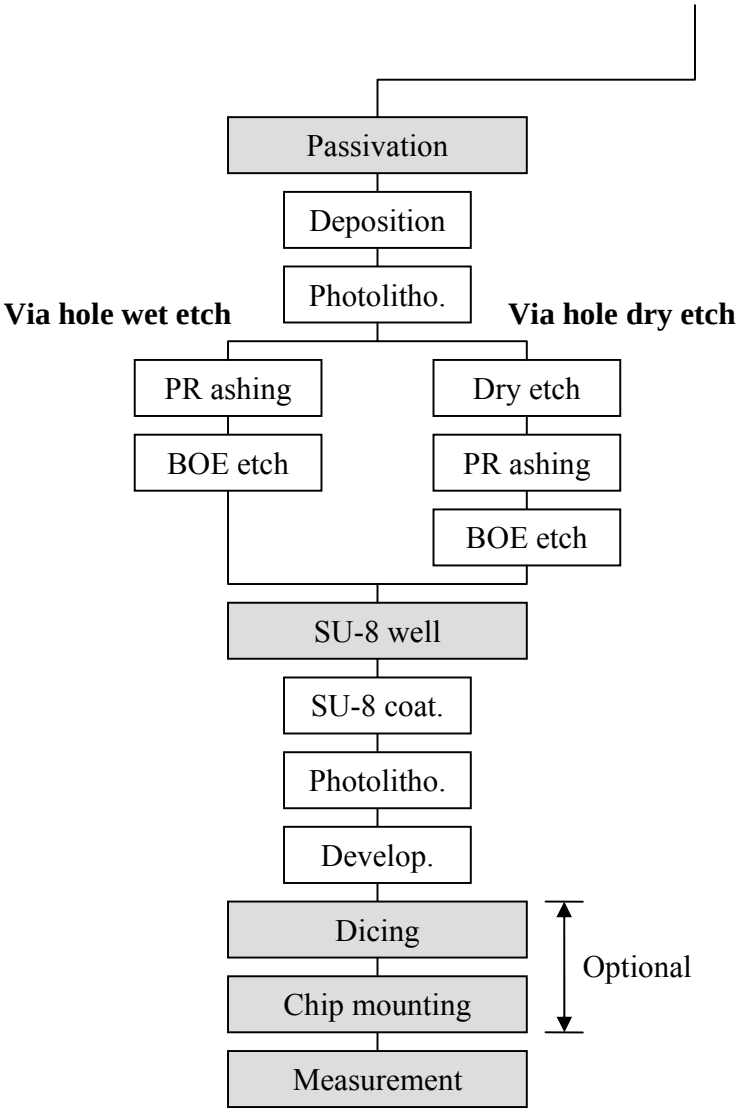
Fig. 3-3 shows overall device processing flow for (a) TFT device processing and (b) TFT-VACNF processing. In this section, the TFT device processing will be described with each detail process flow.

3.2.1 Alignment mark processing

Thermally oxidized water is utilized as a starting substrate. Before coating photoresist, HMDS priming process is essential to promote adhesion between photoresist and thermal oxide. The brief mechanism for the adhesion promotion by HMDS is shown in Fig. 3-4. The HMDS priming is processed in vacuum priming furnace at 90 °C for 25 ~ 30 minutes including pumping down, priming, purging, and venting. Slow complete cooling process is needed after the priming to prevent rapid hardening of subsequent photoresist. Spinning speed and time for photoresist coating is 3000 rpm and 60 seconds. The resultant thickness of photoresist will be ~ 1.6 μm for 955CM 2.1 and ~ 0.6 μm for 955CM-0.7. Developing photoresist is processed by CD-26 for 80 sec and then descum process based on oxygen plasma is needed to remove photoresist residues to be etched area for 30 seconds. The etched thickness of photoresist is below 50 nm. The thermal oxide film is etched by dry etch using RIE with a condition of 200 W RF power, CHF_3/O_2 (75/7), 200 mTorr pressure for 450 seconds. Resultant etch depth of SiO_2 after photoresist striping is ~ 600 nm and remained thickness of photoresist is 0.8 ~ 1.0 μm

FIG. 3-3. Overall process flow for TFT and TFT-VACNF. (a) TFT device processing, (b) TFT-VACNF processing


Alignment mark
Deposition
Photolitho.
Dry etch
Gate electrode (Cr)
Deposition
Photolitho.
Wet etch
Active layer
Deposition
Photolitho.
Dry etch
S/D electrode (Cr)
Deposition
(a) TFT device processing
(b) TFT-VACNF processing
Photolitho.
Wet etch
Passivation
Deposition
Photolitho.
Dry etch
TFT measurement
VACNF growth
Si dep.
Photolitho.
Ni dep.
Lift-off
Growth
Continued


Passivation
Deposition
Photolitho.
Via hole wet etch
Via hole dry etch
PR ashing
BOE etch
Dry etch
PR ashing
BOE etch
SU-8 well
SU-8 coat.
Photolitho.
Develop.
Dicing
Chip mounting
Measurement
Optional

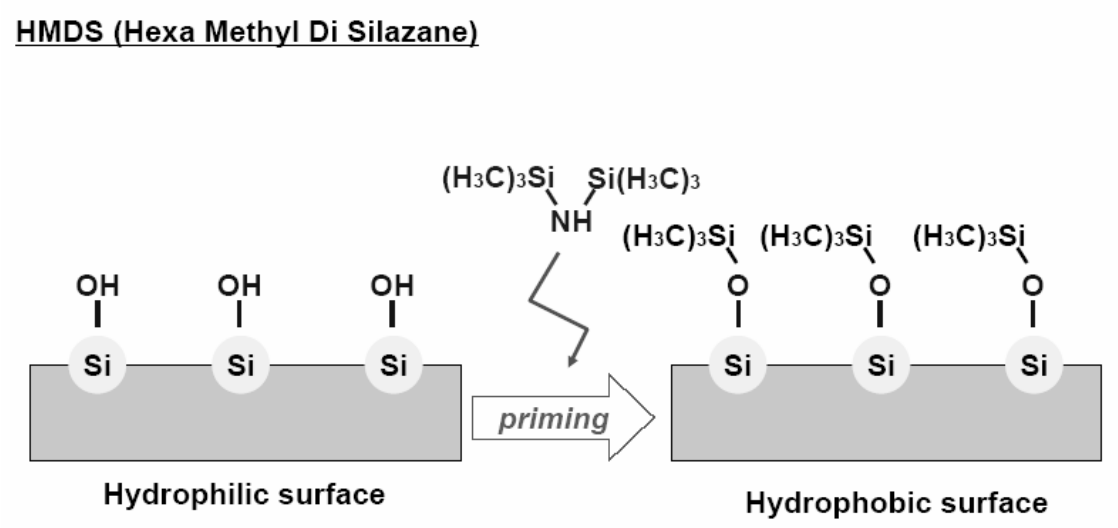


FIG. 3-4. Adhesion promotion by HMDS priming.

before photoresist striping. The photoresist hardened by highly generated ion bombardment is not removed easily by conventional wet strip process. A dry strip based on oxygen plasma generated by ICP and RF is required to strip residual photoresist completely after wet strip. The condition for the dry strip is 300 W ICP power, 50 W RF power, O_2 50 sccm, 350 mTorr pressure, and 120 seconds process time.

3.2.2 Gate electrode processing

In fabricating TFT devices, the etching profile of the gate electrode is a very important process issue. This is especially true for an inverted-staggered TFT structure where the gate electrode is the bottom layer. These structures require a tapered etch profile for several reasons. Firstly, it provides better step-coverage in subsequent deposition patterning processes. Secondly, a sharp edged (or undercut) gate can be a main source of dielectric breakdown due to the concentration of electric field at this sharp-edged point. Thirdly, the tapered gate electrodes influence the electrical properties of TFT and can lower threshold voltages and facilitate steep swing characteristics.[44] As shown in Fig. 3-5 (a), poorly patterned gate electrode causes the device failure due to chemical attack into a crack when it is chemically etched during the S/D wet etch process. Fig. 3-5 (b) shows dry etching profile of MoW (0.35 atomic fraction of W) by reactive ion etching (RIE) system under the process conditions of 120 W RF power, 16 Pa pressure, SF_6/O_2 (25/35 sccm) gas flow rate.[52] The etch profile is shown just prior to completing the metal etch. This profile shows a slight tapered angle (~80 degrees) which

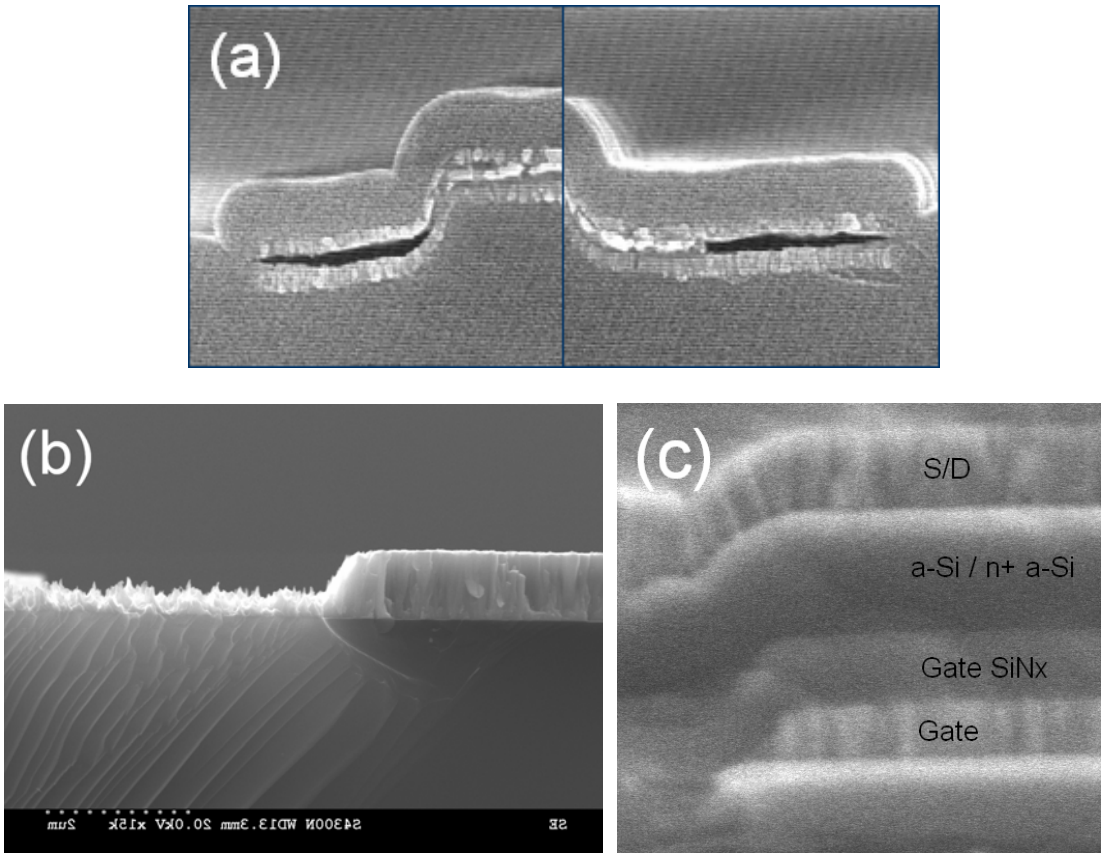


FIG. 3-5. Various SEM images of tapered gate electrodes. (a) chemical attack from crack caused by poor taper angle resulting in device failure, (b) well-tuned MoW gate electrode etched by plasma etch (etch end point), (c) excellent step-coverage in subsequent deposition layers (gate SiN_x, a-Si, and S/D) due to well-defined MoW gate.

can be significantly reduced (~ 30 degrees) by using a two step etch process or over etch process. The tapered angle of gate electrode can be controlled by changing the gas ratio of SF_6 and O_2. As the ratio of oxygen content increases, the etch tapered angle is usually lowered with increasing photoresist ashing rate.[44] The process pressure is another dominant factor to control the tapered angle. The tapered angle of MoW is lowered with increasing process pressure due to the increased reactivity between photoresist and etch radicals and short mean free path of ions and radicals resulting in lower ion bombardment (less anisotropic and more chemically etch results). The use of the MoW alloy as a gate electrode is very desirable to get very low etch tapered angle with reasonably low resistivity.

As shown in Fig. 3-2, the sputtering has four guns and RF sources which can sputter multi-compositional film such as MoW. To verify the deposition properties of Mo, W, and MoW films, the Mo and W targets were put on gun #1 and #3 respectively and a thermally oxidized wafer was placed on substrate holder without rotation for combinatorial MoW thin film synthesis which has a composition difference across the wafer. That is, the composition of Mo and W is changed with the position across the wafer. The substrate is rotated if one needs uniform composition on the whole wafer. Fig. 3-6 shows the deposition rate of MoW film with several positions across the water (actually composition), deposition temperature, and substrate bias. Lower temperature (RT) and unbiased condition has higher deposition rate than high temperature (250 °C) and 30 W biased deposition for the all positions. The atomic fraction of W, as shown in Fig. 3-7, is almost linearly increased with positions from one edge (Mo-rich) to another

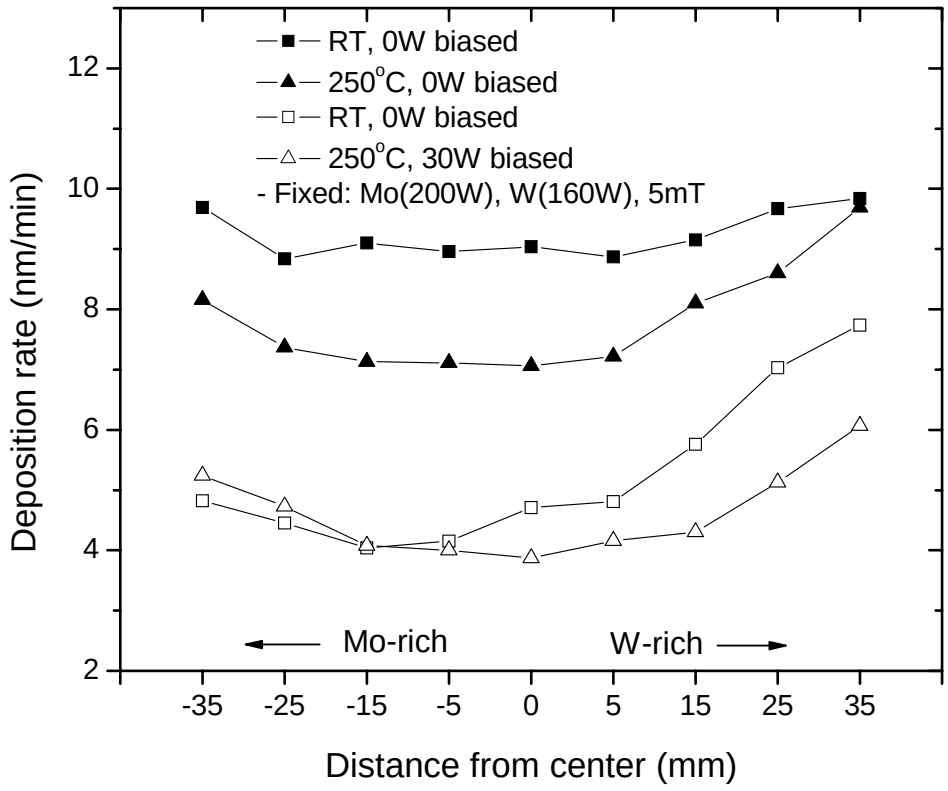


FIG. 3-6. Deposition of MoW as a function of position in a wafer for combinatorial analysis.

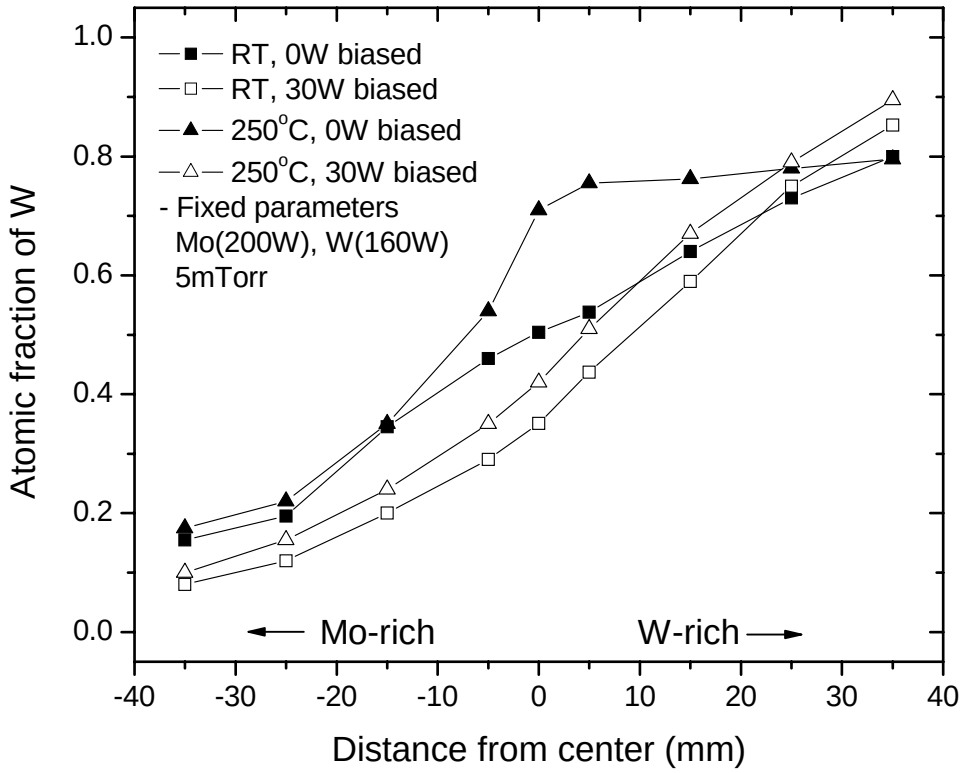


FIG. 3-7. Atomic fraction change of W with the distance from center for combinatorial analysis.

edge (W-rich). The fixed process parameters for these two figures (3-6, 3-7) were Mo (200 W), W (160 W) RF power, 5 mTorr pressure, 25 sccm Ar flow rate, and 70 mm electrode gap. As mentioned previously in Chapter 3, Fig. 3-8 and 3-9 show the electrical resistivity and deposition rate changes with applied substrate bias. The resistivity and deposition rate decrease drastically with increasing substrate bias and they are saturated above ~ 15 W substrate bias. At 0 W substrate bias condition, the resistivity of MoW is higher than those of Mo and W since the film is deposited at room temperature and has high content of metastable β-W phase which causes high resistivity in MoW film. The resistivity of Mo, W, and MoW becomes almost same when substrate bias is applied. The fixed parameters were room temperature, Mo (200 W), W (200 W), MoW (100 W, 100W respectively) RF power, 8 mTorr pressure, 25 sccm Ar flow rate, and 70 mm electrode gap. Fig. 3-10 shows the electrical resistivity change with process pressure, substrate bias as a function of atomic fraction of W. The resistivity of MoW deposited at high pressure is higher than that of MoW deposited at low pressure which indicates highly energized ions by low pressure makes the films with less-defect such as β-W phase in the MoW film. As described previously, the resistivity of unbiased MoW follows Nordeheim's rule with a change of composition but that of biased MoW shows linear relationship as a function of composition. The etch rate of MoW as a function of composition, as shown in Fig. 3-11, changes with deposition temperature. The conditions for dry etch by RIE were 120 W RF power, 120 mTorr pressure, SF_6/O_2 (25/35) gas ratio. The etch rate of high temperature deposited MoW is lower than that of RT deposited MoW which contains the metastable 2^{nd} phase such as β-W and more defects in the film.

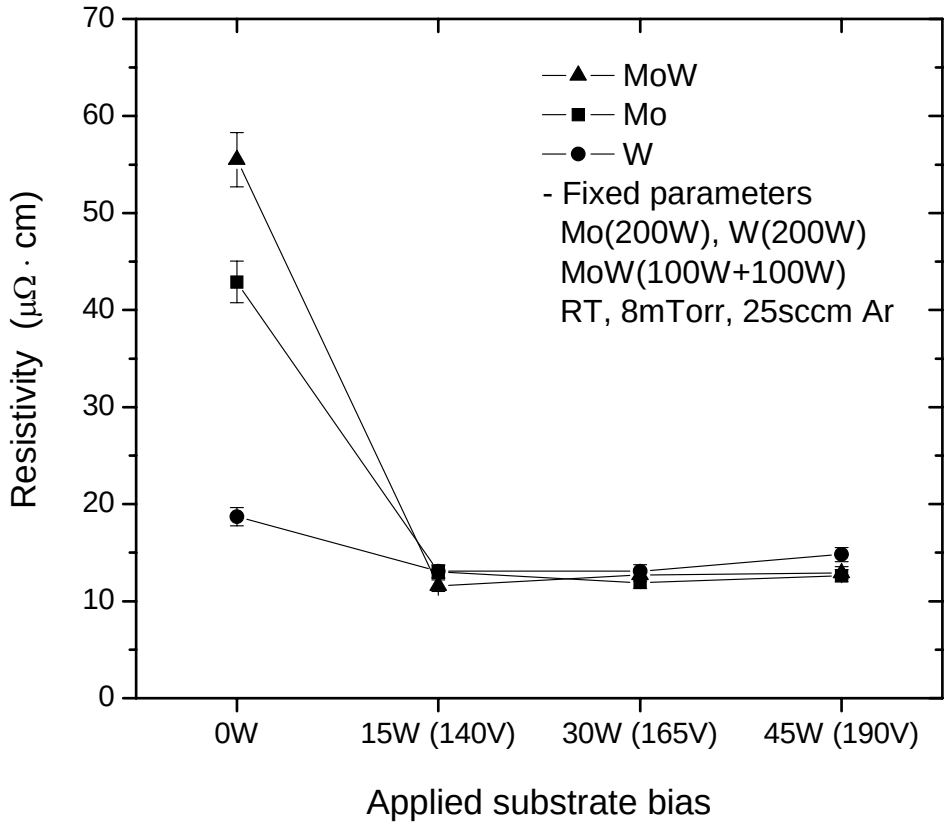


FIG. 3-8. Electrical resistivity change of Mo, W, and MoW as a function of substrate bias in sputter deposition.

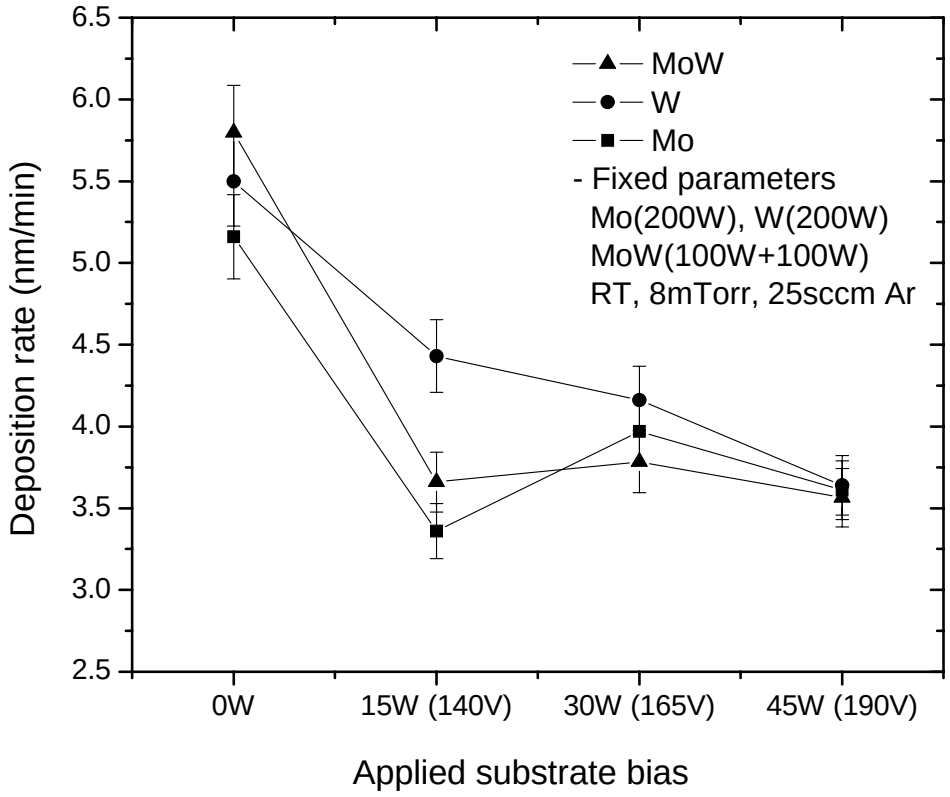


FIG. 3-9. Deposition rate change of Mo, W, and MoW as a function of substrate bias in sputter deposition.

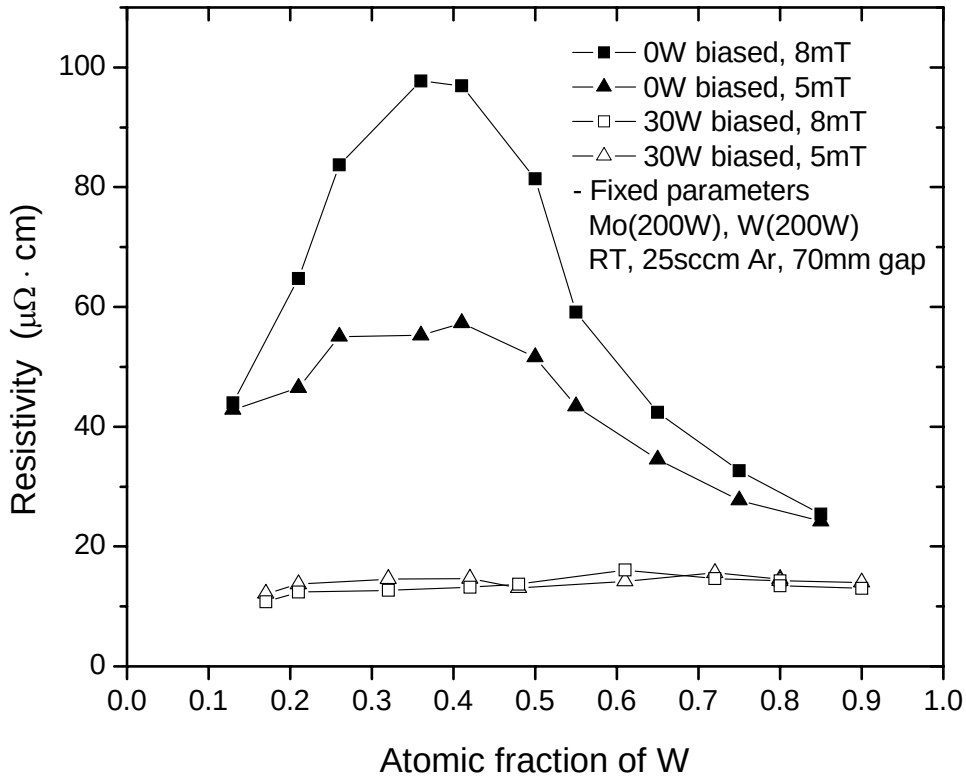


FIG. 3-10. Electrical resistivity of MoW as a function of atomic fraction of W in MoW films with a change of process pressure.

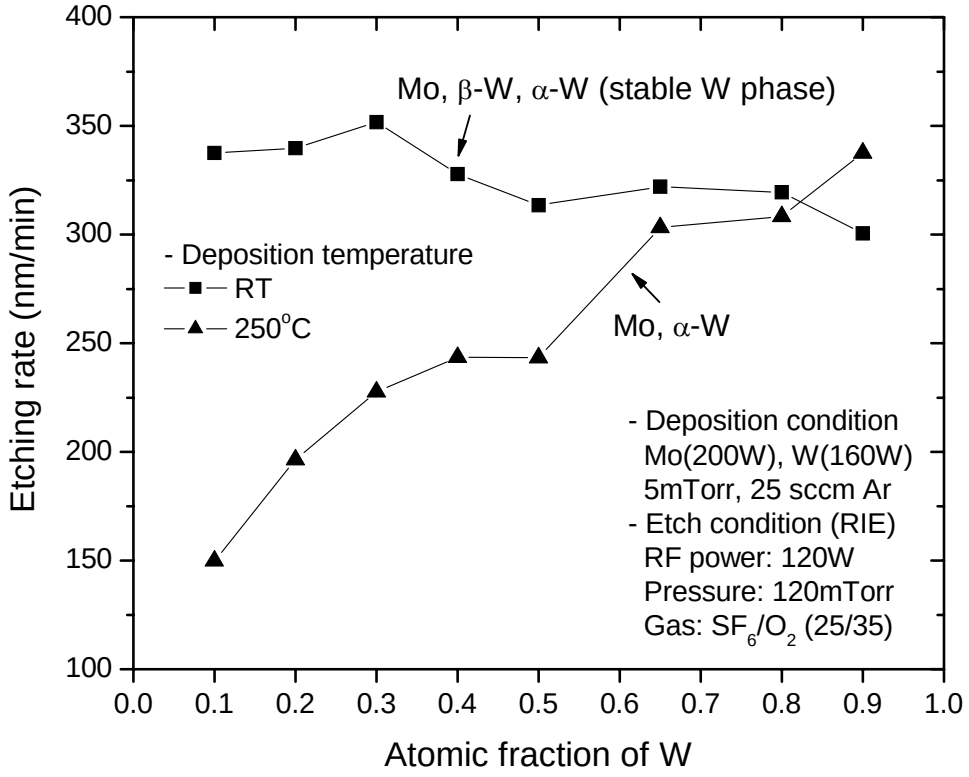


FIG. 3-11. Dry etch rate of MoW film as a function of composition in MoW film.

The etch rate of MoW film deposited at room temperature is almost constant somewhat decreases with increasing W fraction. On the other hand, the etch rate of high temperature deposited MoW film increase with increasing W fraction in MoW film. Usually the etch rate of W is higher that that of Mo in fluorine based dry etch. The etch rate result of MoW deposited at 250 °C is very reasonable as a function of W content in MoW film. But RT deposited MoW is not common with increasing W fraction. It seems to attribute to the complexity such as microstructure and the presence of metastable phase and more speculation is needed to understand this phenomena.

Even though MoW gate electrode provides excellent etch tapered angle and reasonably low electrical resistivity, it has very serious drawback if the dry etch for via hole (passivation etch) is not controlled precisely because fluorine-based gas plasma used for the passivation (SiO_2, SiN_x) etch can attack the MoW gate simultaneously. The etch selectivity of SiN_x to MoW in an SF_6 based plasma etch is at most 2:1 and thicker MoW or a low over etch ratio is needed to compensate the undesirable MoW attack in passivation etch (via hole etch).

To realize a better (nearly infinite) etch selectivity, chrome (Cr) gates can be utilized instead of MoW since Cr is not etched by fluorine-based plasma chemistry. The condition for Cr sputter deposition on gun #1 is 200 W RF power, 200 °C temperature, 3 mTorr pressure, and no substrate bias. Resulting deposition rate is 5.0 nm/min and the sheet resistance (R_S) ranges 0.92 to 1.02 Ω/□ for 250 nm thickness. If the deposition temperature is room temperature, the R_S value is increased to 1.2 ~ 1.35 Ω/□. In photolithography process, photoresist (955CM-2.1) is coated with a speed of 3000 rpm

for 60 seconds and then soft baked at 90 °C for 90 seconds. The exposure time by stepper should be range in 0.32 ~ 0.40 to prevent under/over exposure. Especially over exposure results in high loss of DI CD (developing inspection CD) resulting very narrowed gate length. Post exposure baking (PEB) was done by hot plate set at 120 °C for 90 seconds and developing time in CD-26 is 60 ~ 70 seconds. The method of Cr etch is usually wet etch or dry etch process based on chlorine plasma chemistry. In the case of CR-7 Cr etchant (Cyantek) containing *9%$(NH_4)_2Ce(NO_3)_6$+6%$(HClO_4)$+H_2O*, the etch rate of Cr is ~ 150 nm/min at a temperature of 45 °C with agitation. By switching to a chromium gate electrode a suitable over etch was possible to for the SF_6/O_3 plasma via hole etch. Furthermore, because the wet chemical chromium etch is relatively isotropic, a good taper angle was also realized. The etch mechanism for Cr by this wet etchant is,

$$HClO_4 \rightarrow H^+ + ClO4^-$$
$$(NH_4)2Ce(NO_3)_6 \rightarrow 2NH_4{}^+ + Ce_4{}^+ + 6NO_3{}^-$$
$$Cr + 6Ce_4{}^+ + 4H_2O \rightarrow CrO4^{2-} + 6Ce_3 + 8H^+$$

To remove the photoresist after the Cr gate wet etch, conventional wet strip was utilized based on carbitol (dietylene glycol monoethye ether), amine, NMP (normal methyl 2-pyrrolidone), and surfactant. Cr is not attacked with this kind of photoresist stripper, however, in the case of using an aluminum (Al) or multi-layered gate such as Al/Mo or Mo/Al/Mo, there is serious Al attacked by following process steps; 1) ionization of amine and OH^- formed, 2) Al attack with forming aluminum oxide reacting with H_2O. Plasma dry strip is recommended to remove photoresist after Al etching to protect Al gate line.

$$R - NH_2 + H_2O \rightarrow R - NH_3 + OH^-$$
$$2Al + 2OH^- + 2H_2O \rightarrow 2AlO_2 + 3H_2$$

3.2.3 Active layer processing

Active layer deposition; Prior to investigating sputter deposited active layers, several studies were performed to investigate PECVD Si, SiO_2, and Si_3N_4 active layers. While ultimately the sputter deposited films were used in the transistor fabrication, below are some of the processing issues encountered when studying the PECVD films.

Amorphous silicon (a-Si) active layers are typically deposited by PECVD using a SiH_4 gas plasma. The sequence of the deposition process is;

1) Activation of free electron; the free electron is accelerated by electric field in the plasma and the accelerated electrons collide with the source gas for the deposition.
2) Ionization of feed gas *($X \rightarrow X^+ + e^-$)*; electrons and ions are accelerated toward RF source and grounded substrate, respectively, by electric field in the plasma state.
3) Formation of precursor; the accelerated ions collide with source gas (SiH_4) and form four kinds of precursor for the deposition.

$$SiH_4 \rightarrow SiH_2 + H_2 \ (\Delta H = 2.2eV)$$
$$SiH_4 \rightarrow SiH_3 + H \ (\Delta H = 4.0eV)$$
$$SiH_4 \rightarrow Si + 2H_2 \ (\Delta H = 4.4eV)$$
$$SiH_4 \rightarrow SiH + H_2 + H \ (\Delta H = 5.9eV)$$

where ΔH is enthalpy needed to form precursor. The precursor reacts with the source gas and then 2nd precursors are formed as below,

$$H + SiH_4 \rightarrow SiH_3 + H_2 \ (\Delta H = -0.5eV)$$
$$SiH_3 + SiH_3 \rightarrow Si_2H_6 \ (\Delta H = -7.26eV)$$
$$SiH_2 + SiH_4 \rightarrow Si_2H_6 \ (\Delta H = -2.1eV)$$
$$H + Si_2H_6 \rightarrow SiH_3 + SiH_4 \ (\Delta H = -0.6eV)$$

4) Formation of film reacting with surface; SiH_3 reacts with surface after drift diffusion to the surface. The SiH_3 is bonded with Si dangling bonds resulting in high internal energy and then dehydrogenated (a-Si film formed).

As shown in Fig. 3-12 and 3-13, the deposition rate of PECVD a-Si increases with increasing RF power and process pressure because activation energy and chemical activity can be lowered and enhanced, respectively, by increased RF power and pressure. The UV reflectance spectra of a-Si as a function of process pressure are shown in Fig. 3-14. Higher reflectance with characteristic peaks indicates a shorter-range order in the a-Si film and the reflectance with peak is shown clearly at higher process pressure due to the condensed a-Si at higher pressure. Fig. 3-15 shows the deposition thickness of PECVD a-Si as a function of deposition time. The deposition condition was 100 W RF power, SiH_4 (250 sccm) gas flow, 2000 mTorr pressure, and 395 °C temperature.

SiN_x as a gate dielectric insulator is usually deposited by PECVD using SiH_4 and NH_3 or N_2 gas plasma. The sequence of deposition process is;

$$3SiH_4(g) + 4NH_3(g) \rightarrow Si_3N_4(s) + 12H_2(g)$$
$$SiH_4(g) + NH_3(g) \rightarrow SiNH(s) + 3H_2(g)$$

In forming precursor, NH_3 gas is more desirable than N_2 gas since ΔH to form precursors from N_2 gas is much higher than NH_3 (NH_3 ΔH = 3.9~4.5 eV, N_2 ΔH = 9.83

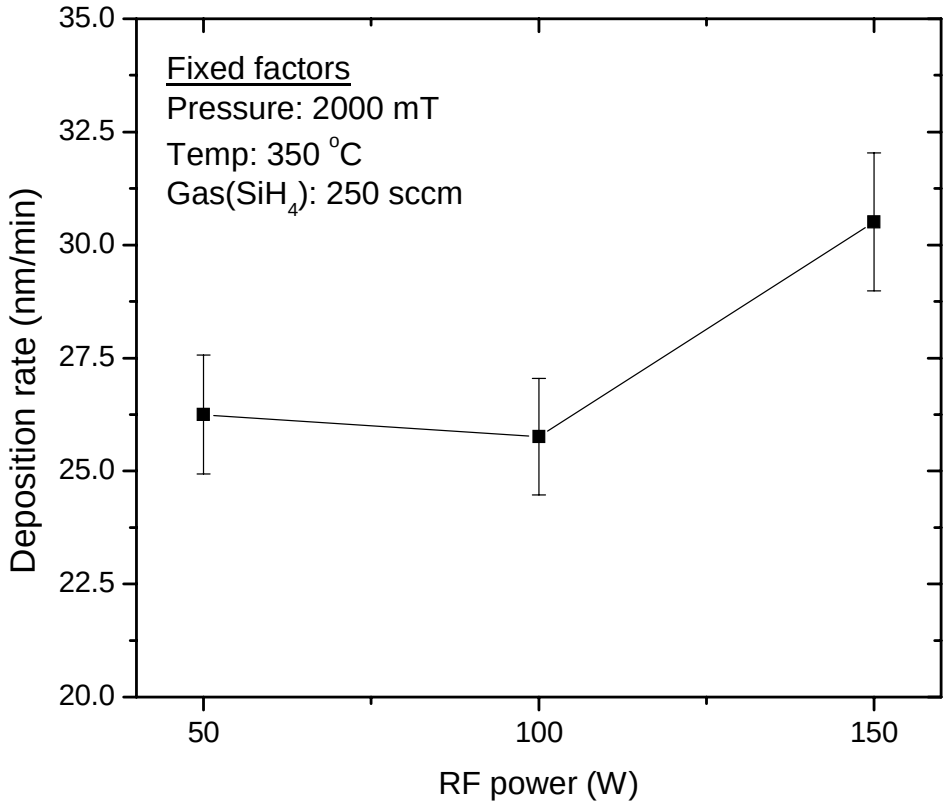


FIG. 3-12. Deposition rate of PECVD a-Si as function of RF power. (10-points-averaged)

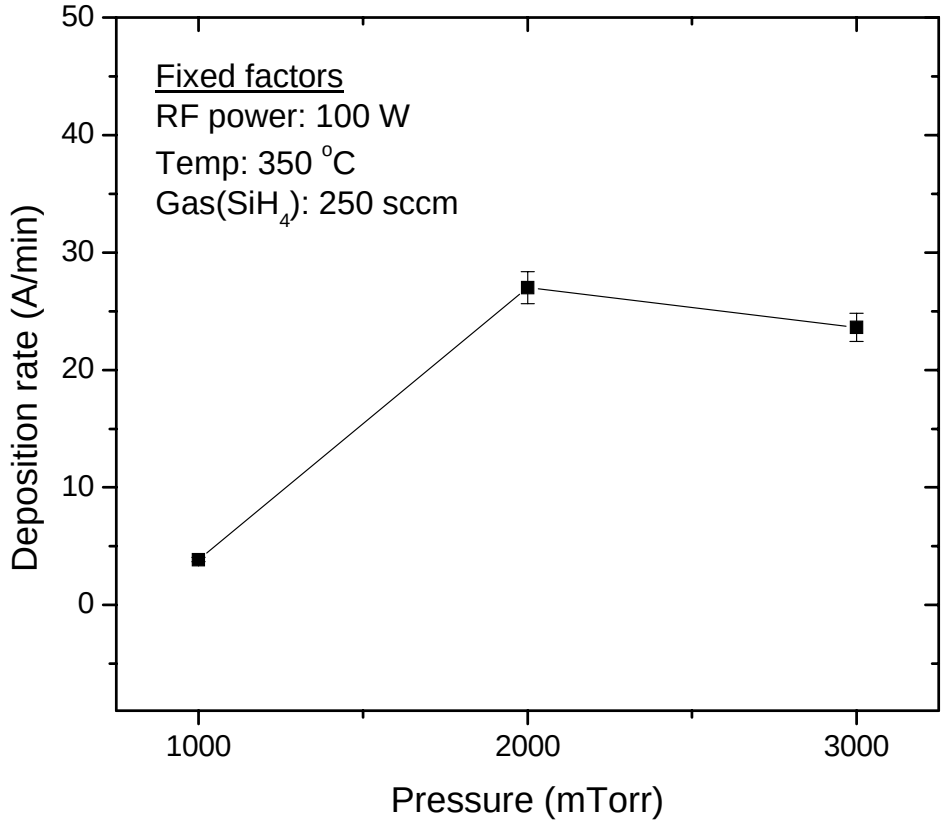


FIG. 3-13. Deposition rate of PECVD a-Si as function of process pressure. (10-points-averaged).

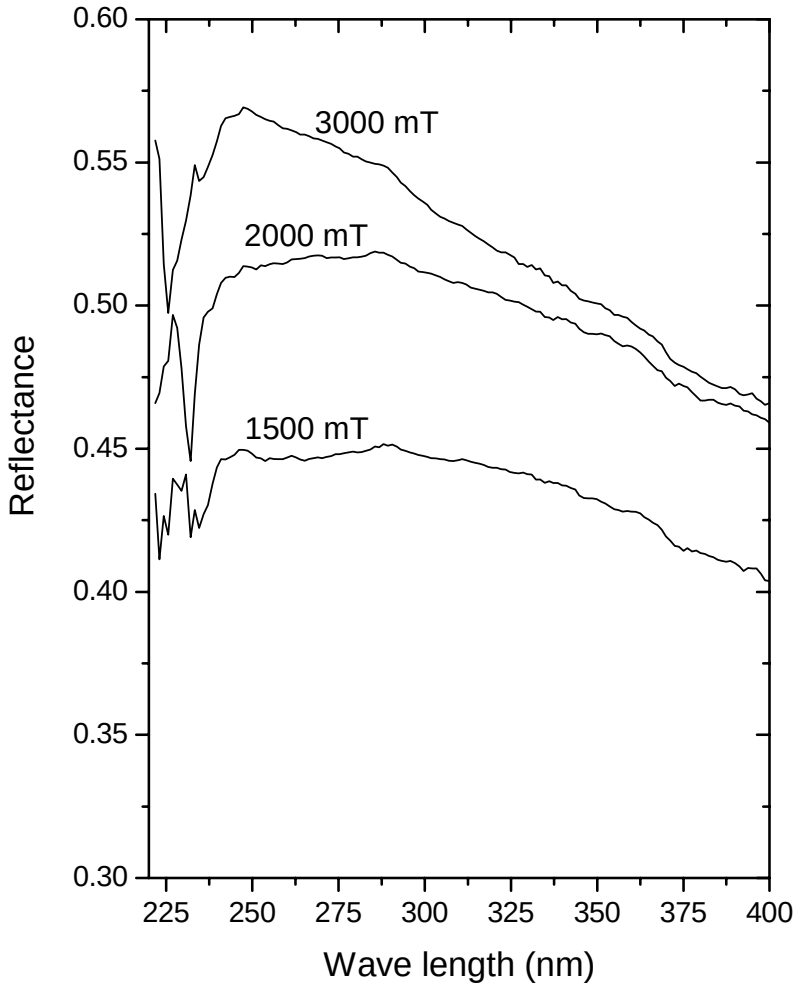


FIG. 3-14. Reflectance spectra of a-Si deposited by PECVD as a function of process pressure. 1500, 2000, and 3000 mT.

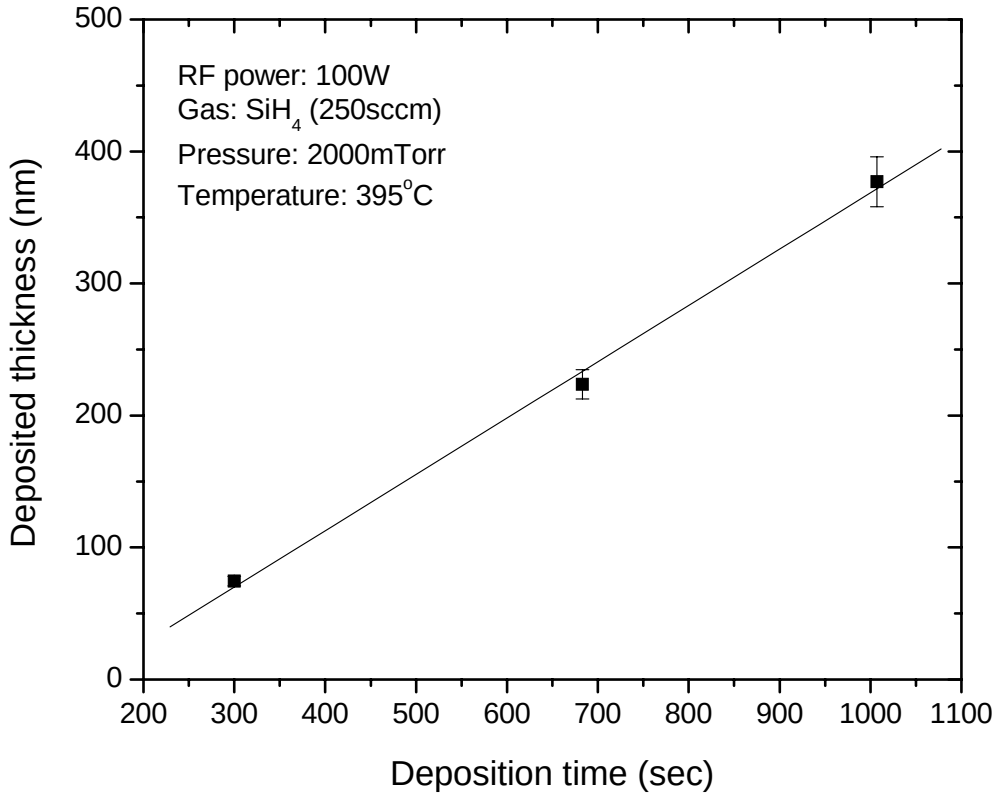


FIG. 3-15. Deposited thickness of PECVD a-Si:H film as a function of deposition time.

eV). The deposition condition for PECVD SiN_x film were 30 W RF power, 1200 mTorr pressure, $SiH_4/N_2/NH_3$ (160/100/30) gas flow, and 450 °C temperature. To characterize the electrical properties of PECVD SiN_x, current density is measured by patterning metal-insulator-metal using dot shadow mask. As shown in Fig. 3-16, the current density of PECVD SiN_x is much higher than that of PECVD SiO_2 film with same thickness (200 nm). The high current density attributes to many carriers resulting in low breakdown strength and device failure. As shown in previous chapter 3, PECVD SiO_2 and SiN_x have very low breakdown strength relative to reported values since the used source gas (SiH_4) is diluted with 95 % Ar. Usually 100 % of SiH_4 gas is utilized for the deposition of a-Si, SiO_2, and SiN_x with high quality in microelectronics manufacturing companies. Fig. 3-17 demonstrates the deposited thickness of PECVD SiO_2 as a function of deposition time and the condition was 75 W RF power, SiH_4/N_2O (80/120) gas, 1000 mTorr pressure, and 395 °C temperature.

As shown in previous Chapter 3, PECVD deposited SiO_2 and SiN_x has very low breakdown strength relative to reported ones and it might attribute to using highly diluted source gas and chamber contamination due to as-deposited residues onto chamber wall. In the case of PECVD a-Si film using the system, it is very hard to maintain properties of a-Si film such as thickness and even the properties are very poor relative to even sputter deposited a-Si. Because of several reasons in PECVD films, we optimized sputter deposited a-Si, SiO_2, and SiN_x films to achieve high film quality and low temperature process in fabricating TFT-VACNF.

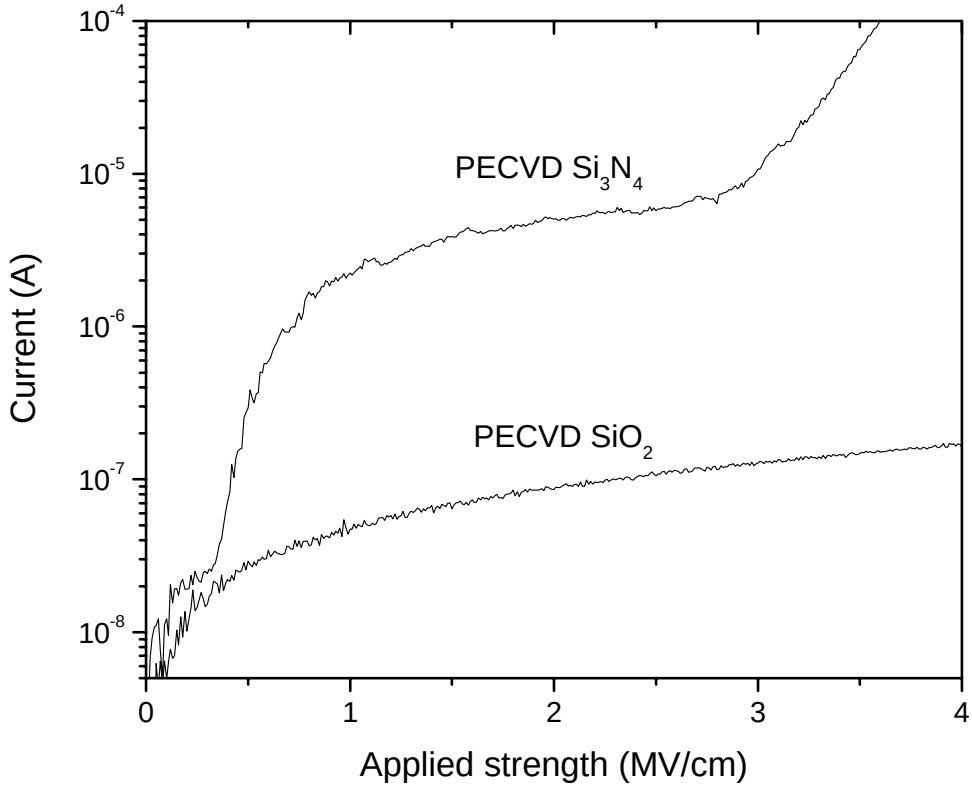


FIG. 3-16. Current changes of PECVD deposited SiN_x and SiO_2 films as a function of applied strength.

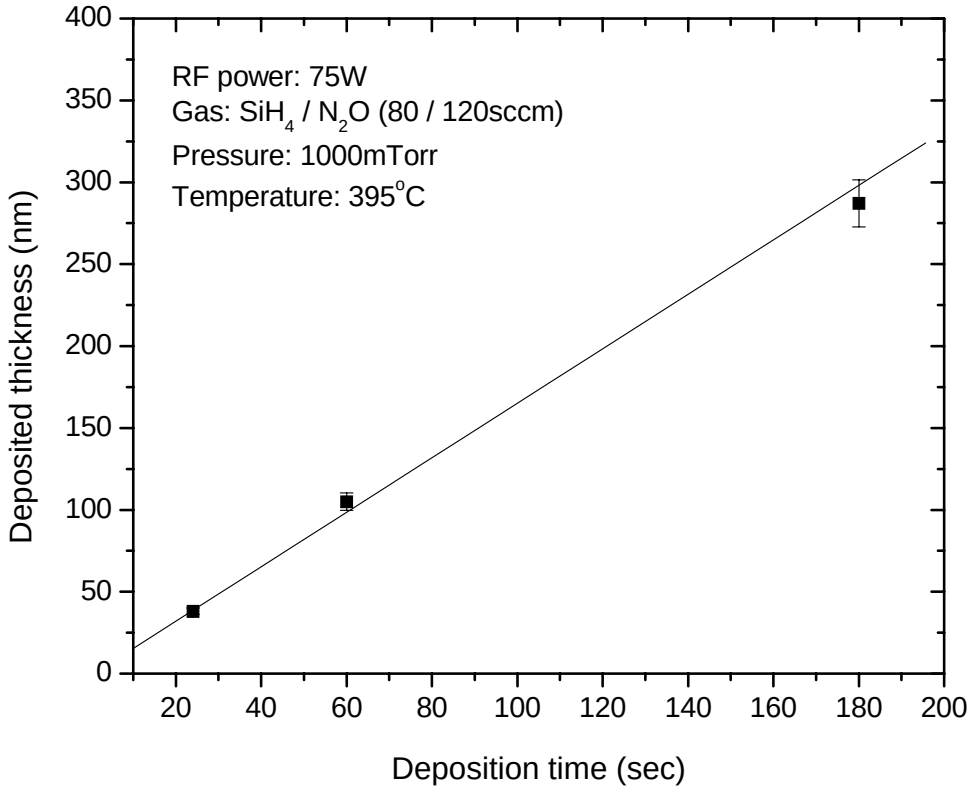


FIG. 3-17. Deposited thickness of PECVD SiO_2 film as a function of deposition time.

Fig. 3-18 shows the deposition rate of SiN_x film as a function of substrate bias in the sputter deposition. The deposition rate decreased with an increase of substrate bias and it is saturated above ~ 20 W bias. The deposition was done by the condition; 200 W RF power, 5 mTorr pressure, Ar-H_2/N_2 (25/35) gas flow, and 200 °C temperature. The thickness of SiN_x film is 250 or 300 nm and applied substrate bias was 10 W for TFT device fabrication. To maintain the vacuum state in sputter chamber for high quality films, a-Si film is deposited consecutively just after SiN_x deposition. Before a-Si deposition, 20 ~ 30 nm SiN_x with low RF power deposition was done to improve the interface state between SiN_x and a-Si films. The interlayer state between SiN_x and a-Si is most critical issue to improve TFT performance. The RF power was 50 W and other conditions were same as a-Si deposition for the rest of thickness. Fig. 3-19 shows the deposition rate of a-Si with substrate bias at two different temperatures (300 and 600 °C). From the figure, the some main factor effecting on the deposition rate is changed from ~ 15 W substrate bias. That is, the ion scattering due to increased temperature results in lower deposition rate at relative low substrate bias. On the other hand, highly adsorption process due to lowered activation energy results in higher deposition rate at high substrate bias. As same as a-Si deposition, n^+ a-Si film is deposited with maintaining vacuum state. The deposition rate change as a function of substrate bias is shown in Fig. 3-20. In the case of SiN_x and a-Si sputter deposition, as shown in Fig. 3-18 and 3-19, the deposition is drastically drop until ~ 20 W substrate bias and then saturated. On the other hand, unlike the case of SiN_x and a-Si, the deposition rate of n^+ a-Si is almost decreased linearly with an increase of substrate bias. Fig. 3-21 shows induced current of n^+ a-Si and

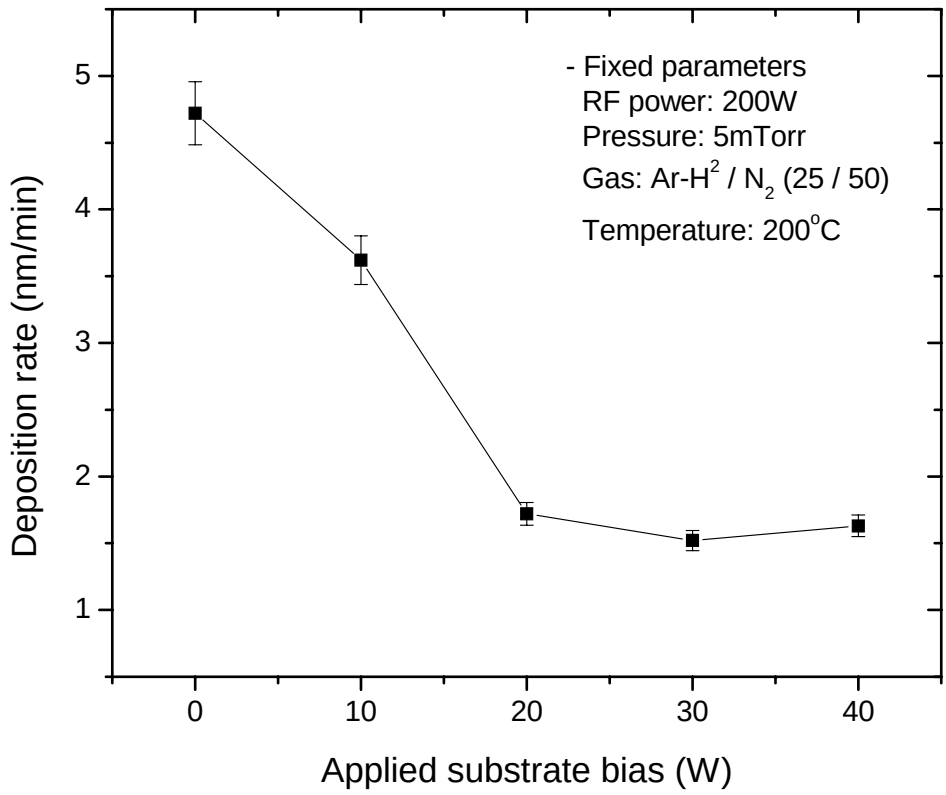


FIG. 3-18. Deposition rate of sputter deposited SiN_x as a function of DC substrate bias.

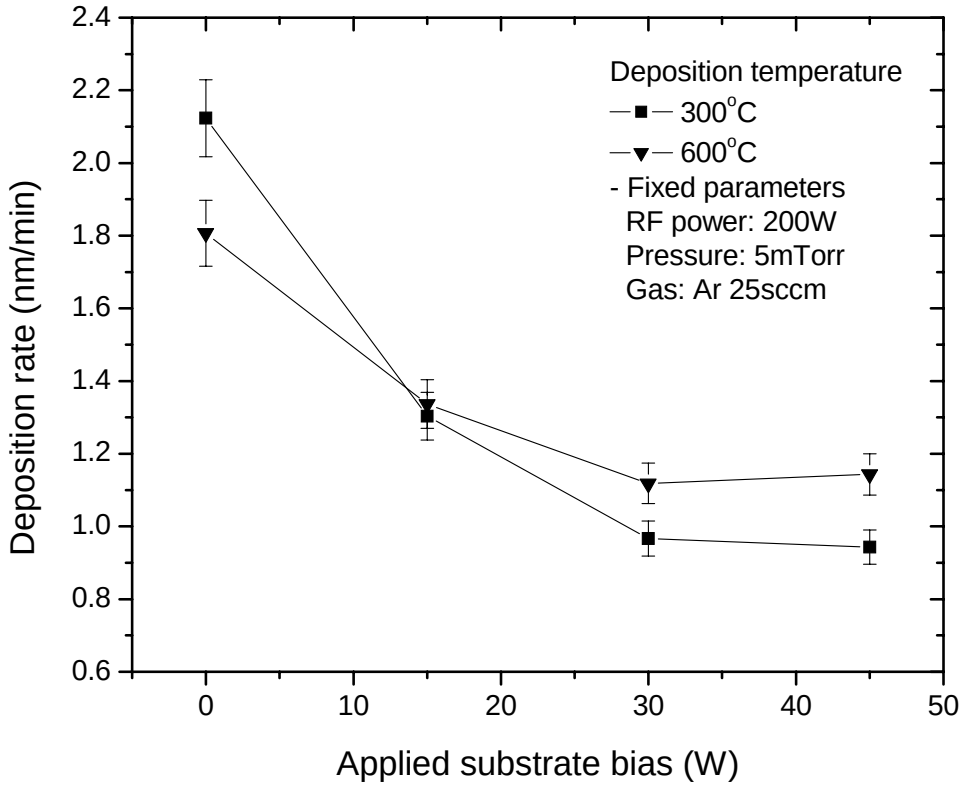


FIG. 3-19. Deposition rate of a-Si thin film as a function of DC substrate bias at two different temperatures.

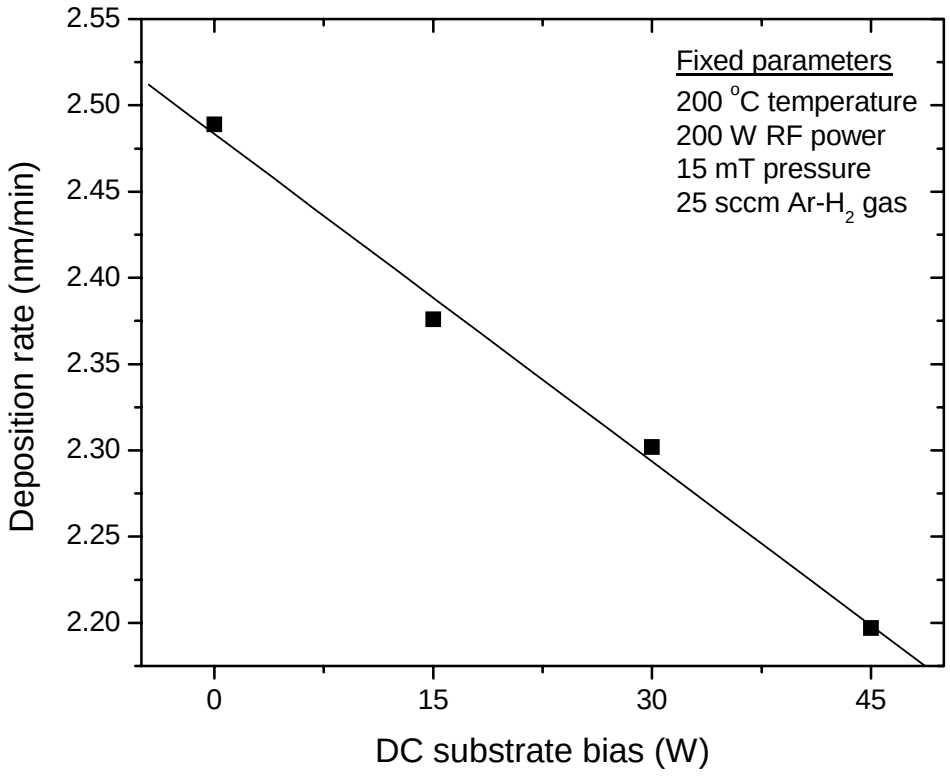


FIG. 3-20. Deposition rate of n^+ a-Si as a function of substrate bias.

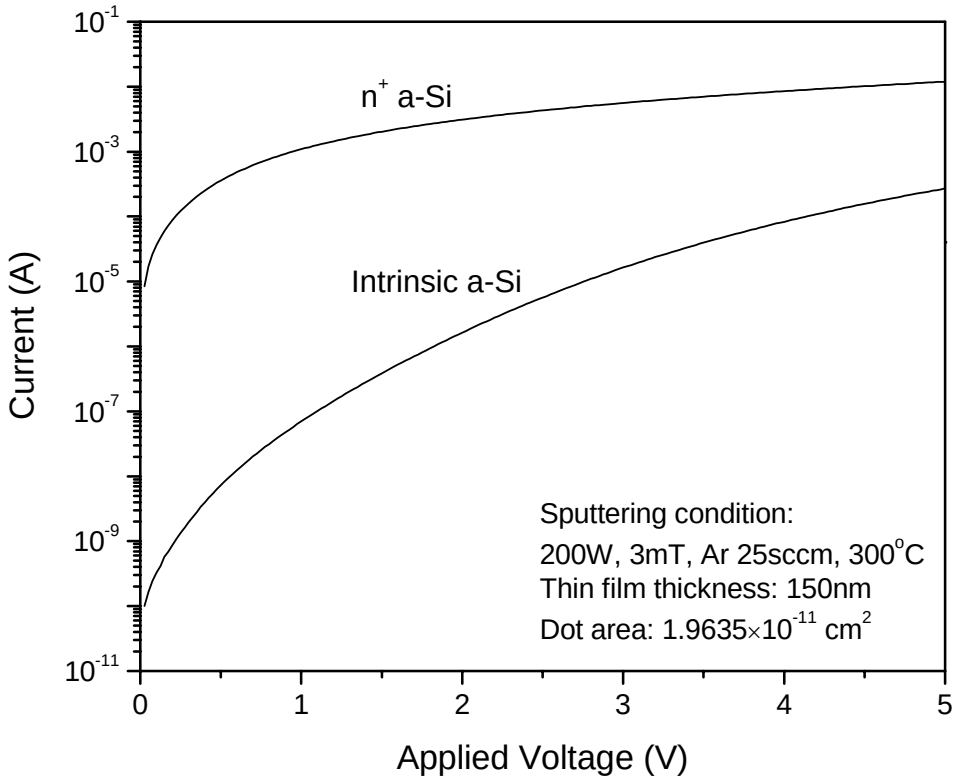
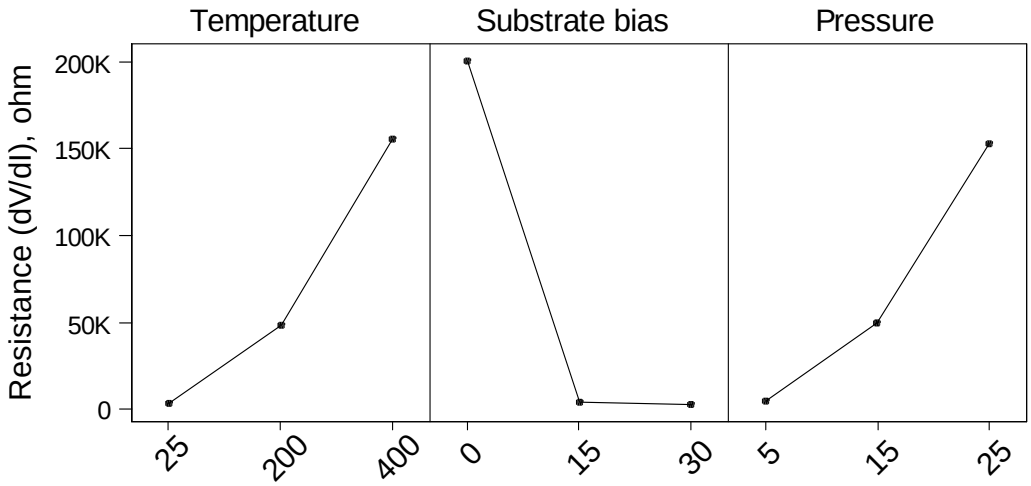


FIG.3-21. Induced current of n^+ a-Si and intrinsic a-Si thin films as a function of applied voltage.

intrinsic a-Si films deposited by sputter deposition with same deposition conditions. Surely n^+ a-Si has higher conductivity than that of intrinsic a-Si. To optimize the deposition condition of n^+ a-Si with low resistance, a design of experiment (DOE) was performed with 3 factors and 3 levels using by MINITAB statistical software. The DOE condition and the results are shown in Fig. 3-22. As shown in the figure, the electrical resistance of n^+ a-Si decreases with decreasing deposition temperature and pressure which might attribute to evaporation of p ions in sputtering. The substrate bias is a dominant factor affecting on the resistance of n^+ a-Si film and the resistance decreased drastically with increase of substrate bias which is agreed well with an experiment result in Chapter 3 (materials integration of n^+ a-Si).

Active layer photolithography; After active layer deposition, a conventional lithography is processed using 955CM-2.1 photoresist, stepper, and CD-26 developer. Before coating photoresist, a cleaning process is required to remove residual particles using deionized (DI) water rinsing. The substrate after wet cleaning is placed on hot plate set at 120 °C to remove completely residual DI water since water molecules on a-Si film causes very serious problem with photoresist adhesion with thin films. To improve adhesion between photoresist and a-Si film, a hexamethyldisilazane (HMDS) priming process is normally used. The HMDS typically forms a monolayer on the silicon film which bonds both to the silicon and the photoresist layer which improves photoresist adhesion as shown in Fig. 3-4. After soft baking at 90 °C for 90 seconds, UV exposure is done by stepper with 0.35 ~ 0.38 exposure time. The photoresist is baked at 120 °C for



No.	Temp. (°C)	DC bias (W)	Pressure (mT)	R (dV/dI)
1	25	0	5	6020
2	25	15	15	2287
3	25	30	25	1642
4	200	0	15	141496
5	200	15	25	1950
6	200	30	5	1917
7	400	0	25	454508
8	400	15	5	7006
9	400	30	15	4511

FIG. 3-22. Effect of process factors on electrical resistance of n^+ a-Si film analyzed by statistical method. (Taguchi, 3 factors, 3 levels).

90 seconds (PEB) and then developed by CD-26 for 70 seconds with agitation. PEB is essentially needed to get highly defined pattern in this process.

Active layer etch; In the case of using Cr as the gate and S/D electrodes, there are several process issues in designing active layer because an identical chemical etchant is used for both gate and S/D wet etching resulting in gate attack during the S/D wet etch if the active layer (n^+ a-Si / a-Si / SiN_x) is excessively etched. After the active layer is patterned by plasma etching, only a very thin SiN_x (gate dielectric) remains on the gate electrodes, occasionally < 100 nm depending on the etch uniformity if an over etch is > 50 %. The remaining SiN_x thickness depends on the initial thickness of SiN_x and the over etch ratio and typically a 30 % over etch is applied on this process. In designing the active layer mask, as shown in Fig. 3-1 (c) and 3-23, an etch-blocking buffer layer between the gate and source/drain electrodes at the crossover area must be formed to prevent a gate-source short.

The majority of dry etching processes for n^+ a-Si / a-Si (active layer) is based on CF_4 or SF_6 plasma chemistry; the chemical etch products for the reaction are silicon tetrafluoride. In the case of CF_4 chemistry, fluorocarbon molecules in the ground state are inert for Si and SiN_x. Etching only starts after the reaction gas has been ionized by ingniting a glow discharge. The subsequent etching of Si and SiN_x in CF_4 plasma can be illustrated by following equations,

$$CF_4 \rightarrow 2F + CF_2$$
$$Si + 4F \rightarrow SiF_4$$
$$Si + 2CF_2 \rightarrow SiF_4 + 2C$$

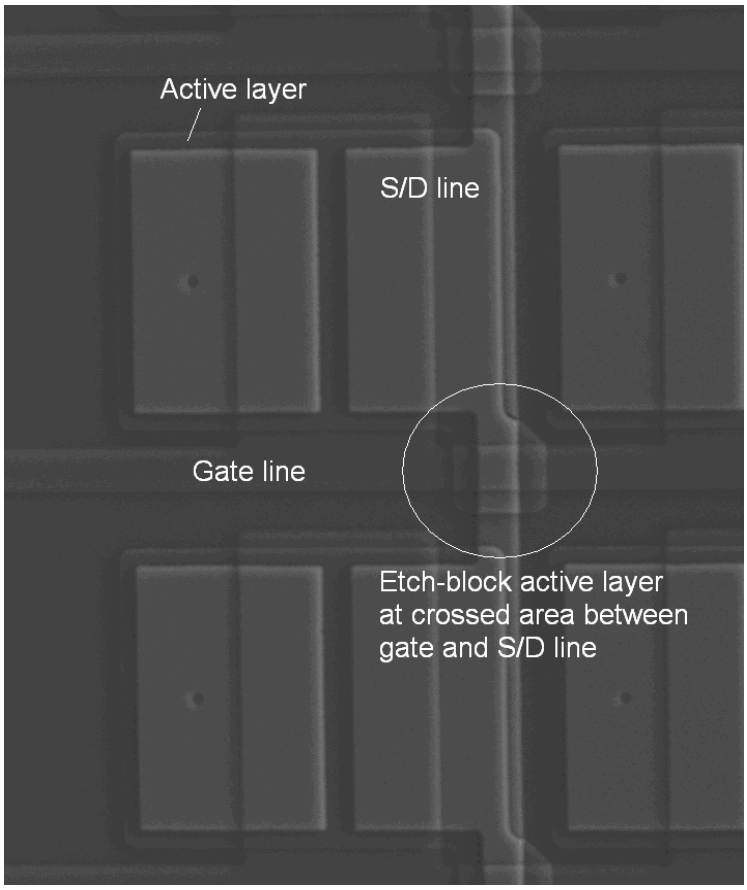


FIG. 3-23. Etch-block active layer at the crossed area between gate and S/D line (circled). The active layer protects gate electrodes from S/D etchant if gate and S/D are same materials. (show scale bar).

Adding oxygen into CF_4 glow discharge increases the amount of free radical F through the formation of oxyfluorides from fluorocarbons,

$$CF_4 + O \rightarrow COF_2 + 2F$$

The etch rate of a-Si in CF_4 and O_2 usually increase with an addition of O_2 to the ratio (O_2/CF_4) of ~ 0.3 but the etch rate drops drastically at higher O_2 concentration. It ascribes in part to a lowering in free radical F because of gas-phase recombination as below equation.

$$O_2 + F \rightarrow FO_2$$
$$FO_2 + F \rightarrow F_2 + O_2$$

In a-Si etch using SF_6 or CF_4 plasma chemistries, each etch chemistry has advantages and drawbacks simultaneously due to their properties. In the case of CF_4 chemistry, it usually provides low CD loss and higher tapered angle (anisotropic) due to polymerization with photoresist (low photoresist ashing rate). However, residual contamination on the etched surface is also due to unreacted (unstable) radicals reacting with oxygen such as CO_x. On the other hand, SF_6 can be more isotropic which lowers the taper angle due photoresist ashing. Consequently the CD loss is bigger for SF_6 than CF_4 based etch. In spite of the drawback of higher CD loss, the use of SF_6 based plasma is strongly recommended in order to get less-contaminated thin film and lower taper angle for stable step-coverage of subsequent layers (S/D and passivation). Similar to the gate process, the tapered angle of active layer is also an important process factor since there are possibilities of open-defects at the crossover area with subsequent S/D electrode due to bad step-coverage of the active layer. The dry etch condition for active etch by RIE is 100 W RF power, SF_6/O_2 (40/4) gas flow, and 100 mTorr pressure. The end point of dry

etch for 50 nm n^+ a-Si and 200 nm a-Si is about 40 second and 15 ~ 20 % over etch is applied.

After active dry etching, it is hard to remove the photoresist completely using conventional wet strip because the photoresist was hardened by ion bombardment during the dry etch. To remove the photoresist residues, plasma ashing processes based on inductive-coupled plasma (ICP) source and oxygen gas is needed after a wet strip for 60 ~ 100 seconds with 300 W ICP and 100 W RF power, O_2 (50) gas flow, and 150 mTorr pressure.

3.2.4 S/D electrode processing

The main factors affecting on electrical properties of the TFT are summarized in Table 3-1. The electrical properties of TFT are mainly affected by the properties of the a-Si, the interface between a-Si and gate dielectric, and the ohmic contact between n^+ a-Si and the S/D metal. Prior to S/D sputter deposition, a BOE (buffered oxide etchant) cleaning diluted with DI water should be treated to remove the native oxide on the n^+ a-Si which otherwise can be a source of high ohmic contact resistance resulting low on-state current and a threshold voltage shift. The recommended dilution and treatment time is 10:1 with DI water and BOE (10:1 diluted) for 15 seconds at room temperature. Sputter deposited Molybdenum (Mo) or chrome (Cr) was usually used as S/D electrodes and the deposition temperature was ~ 200 °C to prevent forming metastable metal phases with high resistivity at low temperature deposition. To get high dry etch selectivity to

Table 3-1. Major factors effecting on TFT characteristics.

Characteristics	Factor
On-state current	Channel width / length Electron mobility (transconductance) Interface semiconductor / gate dielectric Ohmic contact resistance Band gap state Back channel surface (BCE-TFT)
Off-state current	Channel width / length Fermi level of semiconductor Interface semiconductor / gate dielectric Back channel surface (BCE-TFT) Ohmic contact resistance Band gap state
Field effect mobility	Width of band tails Interface semiconductor / gate dielectric
Gate voltage swing (Threshold voltage)	Band gap state (defect state) Interface semiconductor / gate dielectric

passivation SiO_2, using Cr S/D is highly recommended. But Mo S/D is good enough if the passivation is etched by BOE wet etch since the contact resistance of Mo S/D with n^+ a-Si is lower than that of Cr S/D. In the case of wet etching for Cr S/D, the etch condition is the same as method for the Cr gate electrode. On the other hand, the etchant for Mo S/D etch is based on mixed chemical solution containing H_3PO4, CH_3COOH, HNO_3, and H_2O. Hydrogen bubbles formed during this etch process are generated on the S/D film and can block further etching. As a result of the generated bubbles, metal residues called snow balls can be introduced on the surface. Methods to remove the bubbles include: agitation treatment, spray etch mode, and the addition of a surfactant. The agitation treatment used in this work is recommended if the spray nozzle or surfactant is not available. In this process, dry etch for Mo S/D is not recommended because the control of etch stop at the end of Mo S/D is actually impossible due to a similar etch rate with a-Si and SiN_x gate insulator.

3.2.5 Back channel etch processing

The back channel etch used to separate the source and drain region is the most significant process in BCE-TFT. Under-etching causes a source-drain short and over-etching causes a source-drain open resulting in device failure. Subsequently, one needs to monitor the depth of BCE with etch process and etch time regularly since various materials are etched in RIE system and the etch rate varies depending on the system history. Fig. 3-24 shows the change of back channel etch depth of n^+ a-Si / a-Si

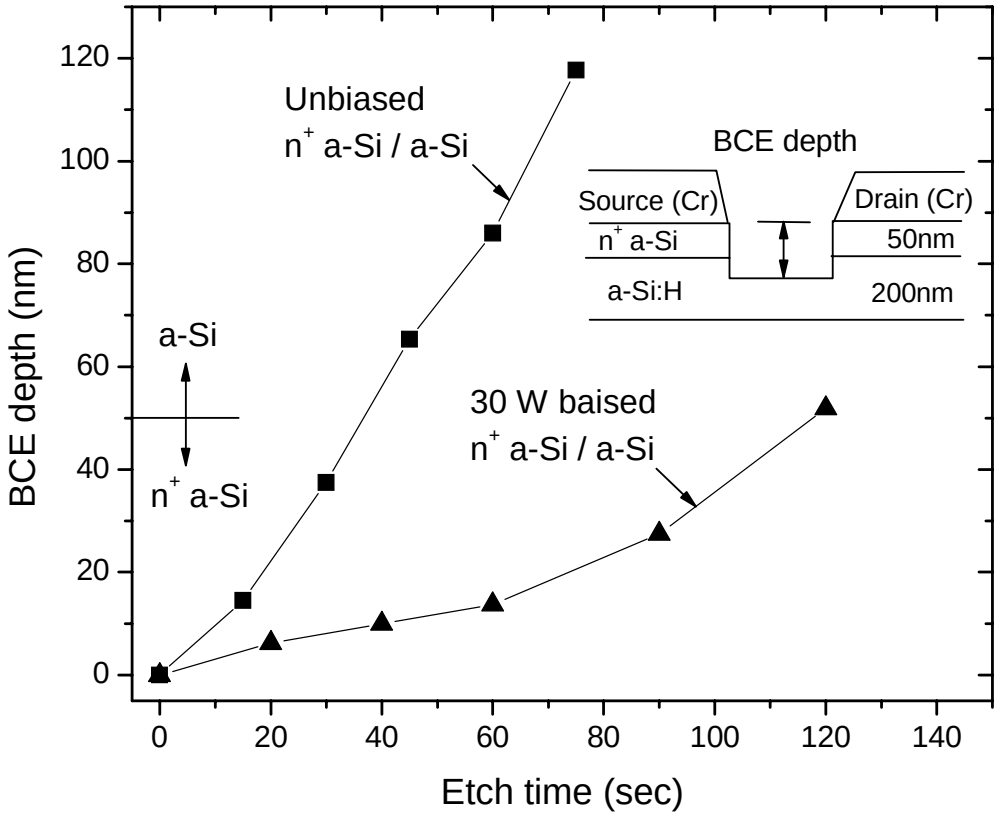


FIG. 3-24. Back channel etch depth of n^+ a-Si / a-Si deposited with/without substrate bias sputter deposition. (10-points-averaged).

deposited with and without substrate bias sputter deposition as a function of etch time. Both films have a linear etch rate with etch time. Low RF powered etch recipes (40 W) were used to minimize damage in the back channel region and the other etch conditions are $SF_6/O_2/CF_4$ (20/3/20) gas ratio, and 100 mTorr pressure. The etch rate of n^+ a-Si / a-Si deposited with substrate bias, as shown in the figure, is lower than that of n^+ a-Si / a-Si deposited without substrate bias since biased a-Si is a denser thin film. A low power RF ashing with an oxygen plasma is followed by the back channel etch in order to compensate defects such as dangling bonds generated by ion bombardment during the back channel etch. The post-etch process condition is 75 W RF power, 150 mTorr, O_2 50 sccm for 120 seconds. The desirable etch depth is 100 nm ± 20 nm (n^+ a-Si 50 nm / a-Si 50 nm ± 20 nm) and a deeper etch results in deterioration in TFT properties; high off-state current, low on/off current ratio, low field effect mobility due to an increased number of defects such as dangling bonds.[65] One needs to monitor the depth of back channel every 15 seconds to make sure the depth because the depth varies with the status and history of etch chamber.

3.2.6 Passivation (via contact hole) processing

The passivation SiO_2 film is deposited by PECVD to protect the device from chemical and physical attacks. In order to minimize the densities of states between back channel and passivation film, a two-step deposition process is introduced for the PECVD SiO_2 deposition; 1) low power deposition for minimizing the densities of states (25 W RF

power, 50 nm thickness), 2) high power for the rest of thickness (75 W, 250 ~ 300 nm). The other condition are same; SIH_4/N_2O (80/120), 1000 mTorr pressure, and 395 °C temperature. To make via hole for contacting with gate and S/D electrode pads, a dry etch is employed based on SF_6/O_2 plasma chemistry. As mentioned previously, unlimited etch selectivity to gate and S/D is obtained if Cr is used as the S/D electrodes. The etch chemistry of SiN_x dry etch is below and the etch condition is same as active etch process based on SF_6/O_2 plasma.

$$CF_4 \rightarrow 2F + CF_2$$
$$Si + 4F \rightarrow SiF_4$$
$$SiNx + 4F \rightarrow SiF_4 + nN$$

3.2.7 TFT characterization

To characterize electrical properties of TFT, current-voltage characteristics was extracted by semiconductor parameter analyzer (HP 4156A). The gate sweep voltage was from -20 V to +25 V with 0.1 ~ 0.5 V step interval and drain voltage is 0.1 ~ 10 V at this gate voltage. The raw data is saved as ASCII file and re-plotted by external plotting softwares such as ORIGIN or EXCEL. The methods to extract TFT parameters such as field effect mobility, threshold voltage, and on/off current ratio are described in Chapter 1.

3.3 TFT-VACNF processing for Intracellular probe

As shown in Fig. 3-3, (b) TFT-VACNF processing for intracellular probing will be described with each detail process flow. The process is same as TFT device processing from alignment mark processing to the S/D deposition.

3.3.1 Ni catalyst deposition and patterning

Thin Si film with ~ 10 nm thickness was deposited by sputter deposition. The deposition condition is same as that of active a-Si film. A conventional lithography process was followed by a-Si deposition. Used photoresist is 955CM-0.7 and spinning speed was 3000 rpm for 60 seconds resulting in 0.6 ~ 0.7 μm thickness. The exposure time was 2.5 second to prevent under exposure since the designed diameter of VACNF hole is just 0.5 μm. After exposure, PEB and developing processes were done consecutively. Ni thin film as a catalyst for VACNF growth was deposited by e-beam evaporation and thickness of the film was ~ 100 nm. To pattern the Ni dot, conventional lift-off process was done by using acetone for ~ 1 hour at room temperature. Resulting diameter of the Ni dot was proven to be ~ 1.0 μm.

3.3.2 VACNF growth and solution for device failure due to interlayer stress

VACNF was grown in DC-PECVD chamber with a condition of C_2H_2 (35) gas flow, 3000 mTorr, 400 mA current, and 550 °C temperature and total time for the growth was 1 hour. Fig. 3-25 shows a TFT-VACNF device failure during VACNF growth. The interlayer stress during the growth is main source of the breakdown. Understanding the stress state of the interlayer thin films is very important since the VACNF is usually grown at high temperature above 550 °C. There are two main factors affecting the stress state of thin films; 1) internal stress during film formation, 2) thermal stress formed by thermal gradients or thermal expansion coefficient differences between thin films. As described in previous, biased sputter deposition provides densified and lower defect thin films. On the other hand, the film has a significant amount of internal stress.[45] A typical growth temperature of VACNF is ~ 700 °C in DC-PECVD and the growth rate is normally proportional to the growth temperature. To minimize these stress factors, the VACNF was grown at 550 °C with slow growth rate and the cooling rate was as slow as possible after VACNF growth in DC-PECVD chamber (~ 10 °C/min) when it is integrated with TFT. Fig. 3-25 shows SEM images of TFT-VACNF showing a device failure due to internal stress from biased sputter deposition even though VACNF was grown at low temperature, 550 °C. The delamination between SiN_x and a-Si layers results from a significant amount of internal stress caused by biased sputter deposition. To prevent the device failure, unbiased sputter deposition must be employed for the TFT-VACNF integration with sacrificing high TFT properties even though the biased sputter

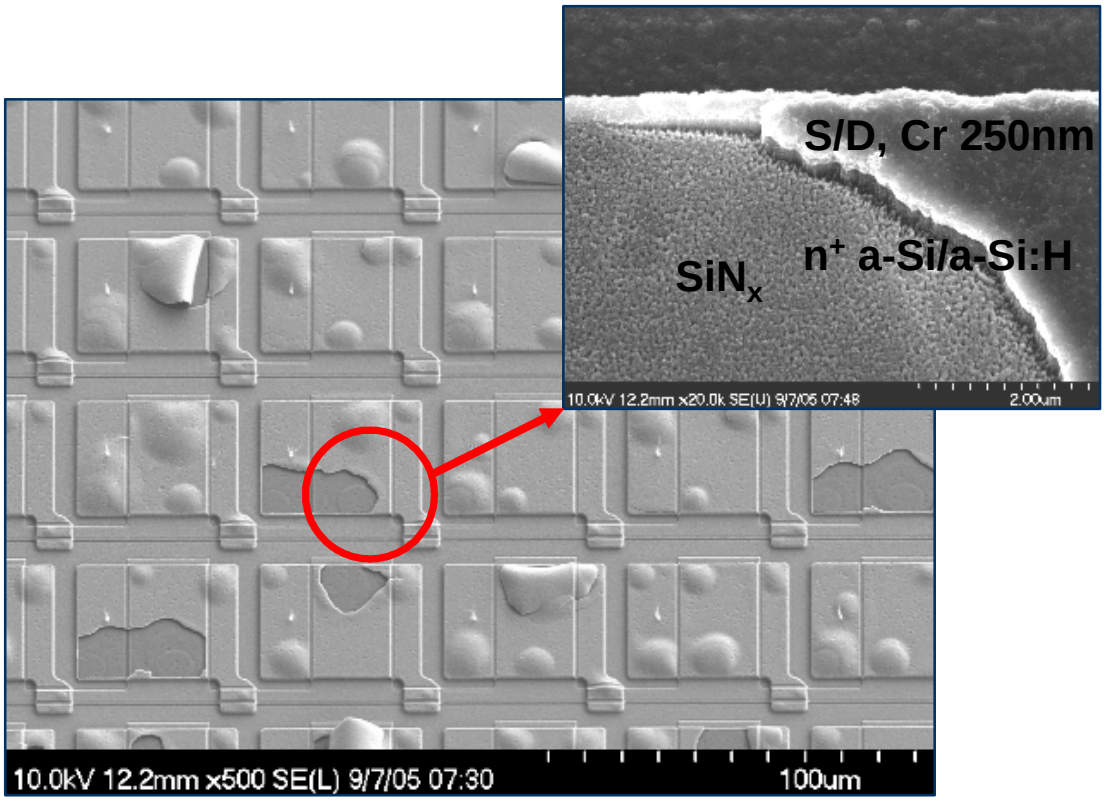


FIG. 3-25. SEM image of TFT-VACNF showing a device failure due to internal stress after VACNF growth at 550 °C. Biased sputter deposition induces a significant amount of internal stress which during the high-temperature VACNF growth causes delamination between the SiN_x and a-Si layers.

deposition provides high quality thin film. Fig. 3-26 shows a SEM image of TFT-VACNF after CNF growth at 550 °C fabricated with thin films deposited by fully unbiased sputter deposition. The figure shows that interlayer stress can be lowered by reducing the VACNF growth temperature and using unbiased sputter deposition. From these results, we need to adopt the unbiased sputter deposition if we fabricate TFT-VACNF devices for intracellular probing. On the other hand, in the case of extracellular probing devices where VACNFs are not required, we can use biased sputter deposition which enhances the device performance.

3.3.3 Passivation

The passivation lithography and etch process are critical processes to probe cells directly. Fig. 3-27 and 3-28 shows two different types of process sequence for the passivation lithography, photoresist ashing, and etch process to form the via contact hole on the S/D and gate electrodes and to expose the VACNF tips for cell probing. Fig. 3-27 is for passivation wet etch process and Fig. 3-28 is for passivation dry etch process. The passivation SiO_2 is usually deposited by PECVD and the thickness is 200 ~ 300 nm with a two step deposition to minimize the densities of states between back channel and passivation films; low and high RF power 50 ~ 100 nm, 200 ~ 250 nm respectively Fig 3-27 (a) and 3-28 (a). Next, a thin photoresist (600 ~ 700 nm, 955CM-0.7) is coated on the passivation film and then baked, and exposed by UV and then PEBed; Fig 3-27 (b) and 3-28 (b). In the case of passivation we etch (Fig. 3-27), after developing using CD-26

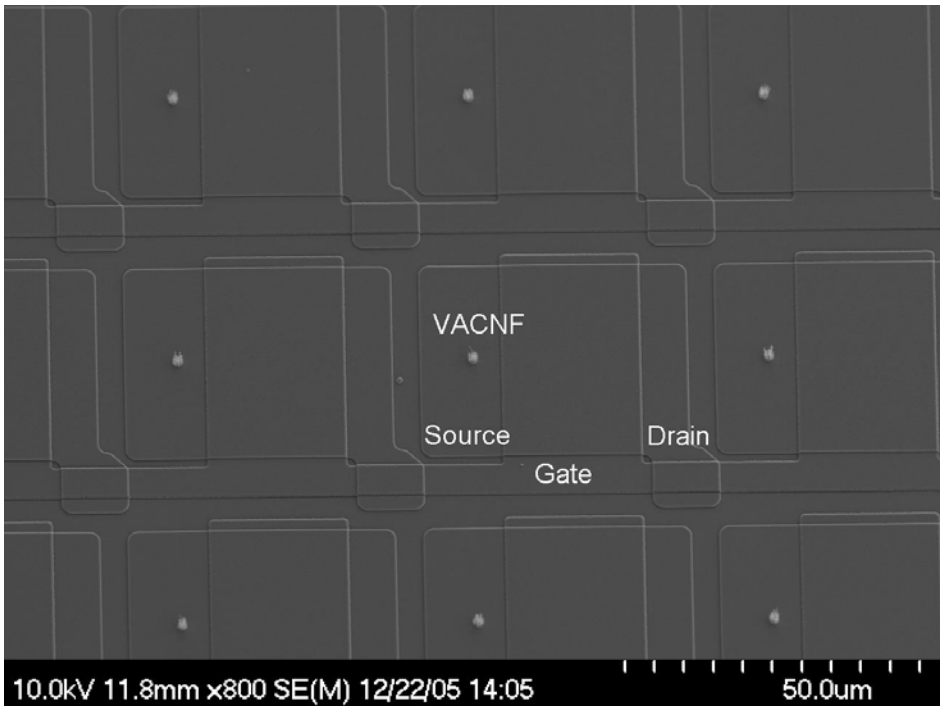


FIG. 3-26. Breakdown failure is not shown after VACNF growth at low temperature growth ~ 550 °C and on the unbiased n^+ a-Si / a-Si.

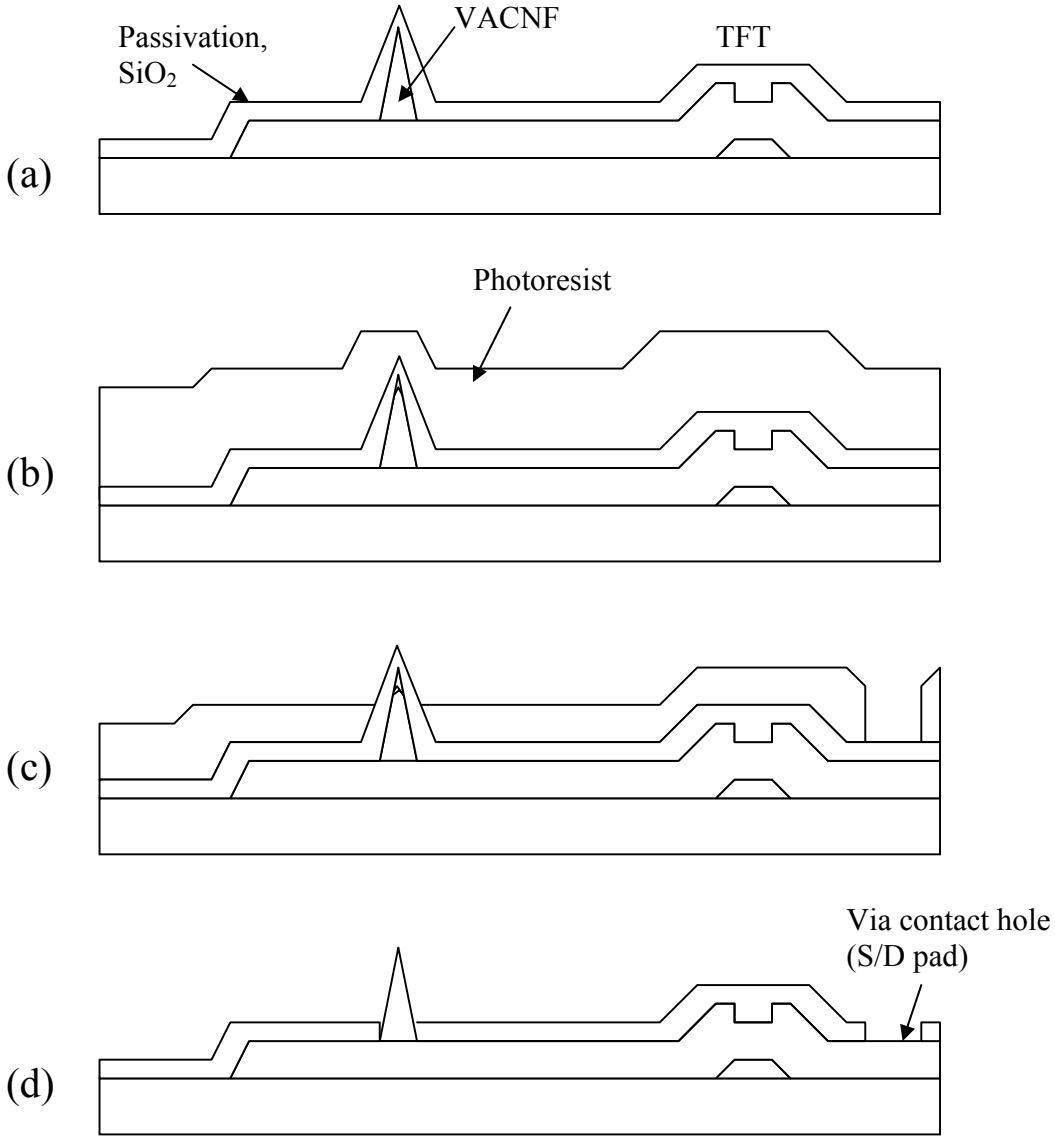


FIG. 3-27. Process sequence for TFT-VACNF passivation (I) for via hole etch and exposing tips of VACNF. (a) Passivation deposition, (b) photoresist coating, (c) developing and photoresist plasma ashing, (d) BOE wet etching to form via contact hole and to expose tips of VACNF striping photoresist.

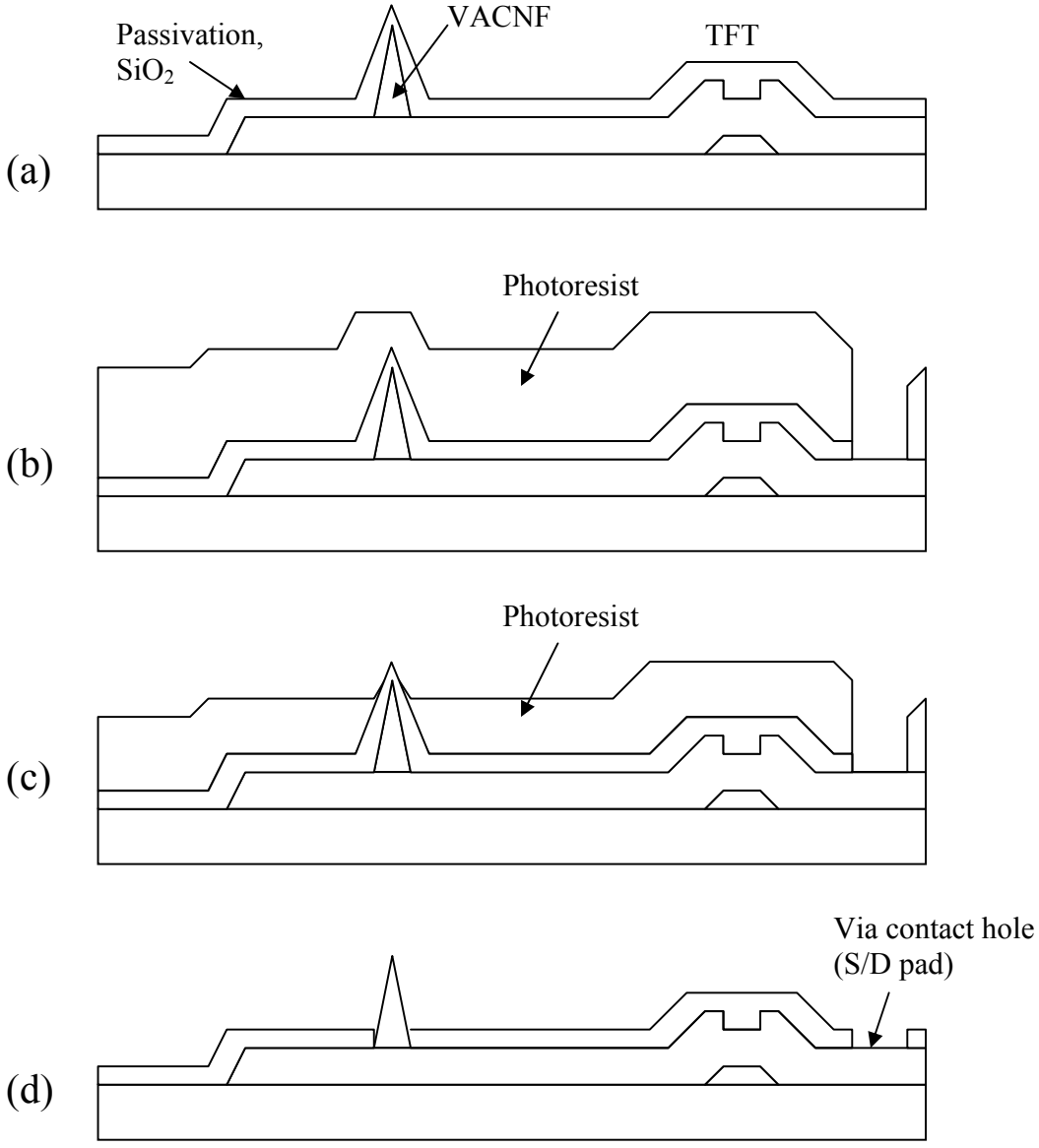


FIG. 3-28. Process sequence for TFT-VACNF passivation (II) for via hole etch and exposing tips of VACNF. (a) Passivation deposition, (b) photoresist coating, (c) developing photoresist, passivation dry etch, and photoresist plasma ashing, (d) BOE wet etching to expose tips of VACNF and striping photoresist.

developer, the photo resist is dry-etched by plasma ashing based using an oxygen plasma to etch back the photoresist on the tips of VACNF, Fig. 3-27 (c). Subsequently the passivation SiO_2 is etched with a 6:1 BOE instead of a dry etch because the VACNF is easily attacked by fluorine based plasmas. Lastly the photoresist is removed by conventional wet strip and plasma ashing based on oxygen plasma and then inspected by optical microscopy or SEM, Fig. 3-27 (d). The passivation wet etch process is good enough to pattern via hole but it is not suitable for exposing the VACNF tips because CD bias is very large. On the account of large CD bias, there is a serious possibility to expose S/D electrode with the VACNF tips. To minimize the CD loss, a passivation dry etch process was employed; Fig. 3-28. The condition for the dry etch is same as that of TFT device processing. After passivation dry etch using fluorine based plasma, the remained photo resist is dry-etched by oxygen plasma to etch back the photoresist on the tips of VACNF; Fig. 3-28 (c). Subsequently the passivation SiO_2 on the VACNF tips is etched with a 6:1 BOE and then the photoresist is removed by conventional wet strip and plasma ashing based on oxygen plasma and then inspected by optical microscopy or SEM; Fig. 3-28 (d).

Chapter 4 Electrical characterization of thin film transistors

4.1 Definitions and thin film transistor operation

First of all, the definitions of several terms for the TFT operation are introduced. Mobility is a proportionality constant which relates the drift velocity to the electric field in a semiconductor. Mobility is essentially a measure of how easily carriers such as electrons and holes can move through a semiconductor. Electrons move most easily through single-crystalline silicon because of the uniform periodic arrangement of the atoms. Unfortunately, single-crystalline films require high temperature processes. In poly-crystalline silicon (poly-Si), individual grains of crystalline Si are randomly oriented to one another. In this case, electrons can move easily through each crystalline grain, but are scattered at g grain boundaries. Electrons in amorphous silicon have the lowest mobility which has neither short nor long range atomic order.

Leakage current refers to the small amount of current flowing through a transistor when it is in its off state. In an ideal transistor, leakage current would be zero, but in practice, leakage current always has a finite value.

For all practical purposes, a TFT can simply be considered a switching element; when selected ‘ON’ it allows charge to flow through it and when ‘OFF’ it acts as a barrier preventing or restricting the flow of charge. Basically, a TFT behaves similar to a MOSFET (Metal Oxide Semiconductor Field Effect Transistor) device. The gate can be considered the "switch" of the transistor, which can turn the device ‘ON’, partially ‘ON’,

or ‘OFF’. The source and drain are essentially an entrance and exit of the TFT, respectively, for the charge that is to be passed through the switch. For the TFTs in this work, the source and drain metal electrodes are separated by an amorphous silicon (a-Si) semiconductor layer and it does not contain any charged carriers in the off state. Thus the a-Si layer acts as an insulator or resistor and prevents the flow of charge from the source to drain, thus isolating the unit cell from the rest of the cells. SiN_x or SiO_2 is the gate insulator and forms the gate dielectric that inhibits carrier transport from the gate line to the transistor. While current transport is minimized via the gate dielectric, a gate voltage is used to influence the charge distribution in the underlying semiconductor layer via a field effect. When a positive charge, in the case of n-type TFT, is placed on the gate line, electrons (negatively charged particles) begin to collect in the area above the gate on the other side of the SiN_x in the a-Si. When the charge on the gate is increased to a certain point, called the threshold voltage (V_T), enough electrons will have collected in the a-Si to change it from an insulator to a conductor. In other words, it builds up an electron channel, so if a potential is induced across the source (negative potential) and the drain (positive potential), the electrons will begin to move through the electron filled channel. The unique aspect of this device is the nonlinear current response after the TFT passes through V_T. The current exponentially rises (usually 5 to 7 orders of magnitude) over a very short modulation voltage which makes it very easy to turn a TFT on or off around the V_T value.

4.2 Thin film transistor fabrication and parameter extraction

4.2.1 Inverted-staggered back channel etched (BCE) thin film transistor fabrication

The TFT, as shown in Fig. 4-1, was fabricated by an inverted-staggered and back-channel etched (BCE) process on thermally oxidized wafers (1 μm SiO_2). The detail process flow for the TFT fabrication is illustrated in the appendix of the dissertation and the processing issues are discussed in chapter 3. Briefly, Molybdenum (Mo, 250 nm) or chrome (Cr, 250 nm) gate electrodes were deposited with the RF magnetron sputtering system at 200 °C. The Mo gate electrodes were lithographically patterned by conventional photolithography and reactive ion etching (RIE) based on $SF_6/CF_4/O_2$ chemistry or wet chemical etching *(Cyantek Al etchant, H_3PO_4+CH_3COOH+HNO_3)* at a temperature of 35 °C with agitation (a). The temperature should be below 40 °C since the *CH_3COOH* evaporates with easy at high temperature resulting in a change of etch properties. In the case of Cr gate electrodes, the gate is etched by *premixed CR-7 Cr etchant (Cyantek)* containing *9%$(NH_4)2Ce(NO_3)_6$+6%$(HClO_4)$+H_2O* and the etch rate of Cr is ~ 150 nm/min at a temperature of 45 °C with agitation. The silicon dioxide (SiO_2, 300 nm) or silicon nitride (SiN_x, 300 nm) gate insulator was also deposited by RF magnetron sputtering with substrate bias in argon-hydrogen (5 % H_2) and nitrogen gases. The sputter deposition condition of the SiN_x film was 100 W RF power, 20 W (125 V) substrate bias, 5 mTorr pressure, 25 sccm Ar-H_2, 25 sccm N_2 gas flows, at a temperature of 200 ^oC. Subsequently, the RF magnetron sputtering was also used to deposit a

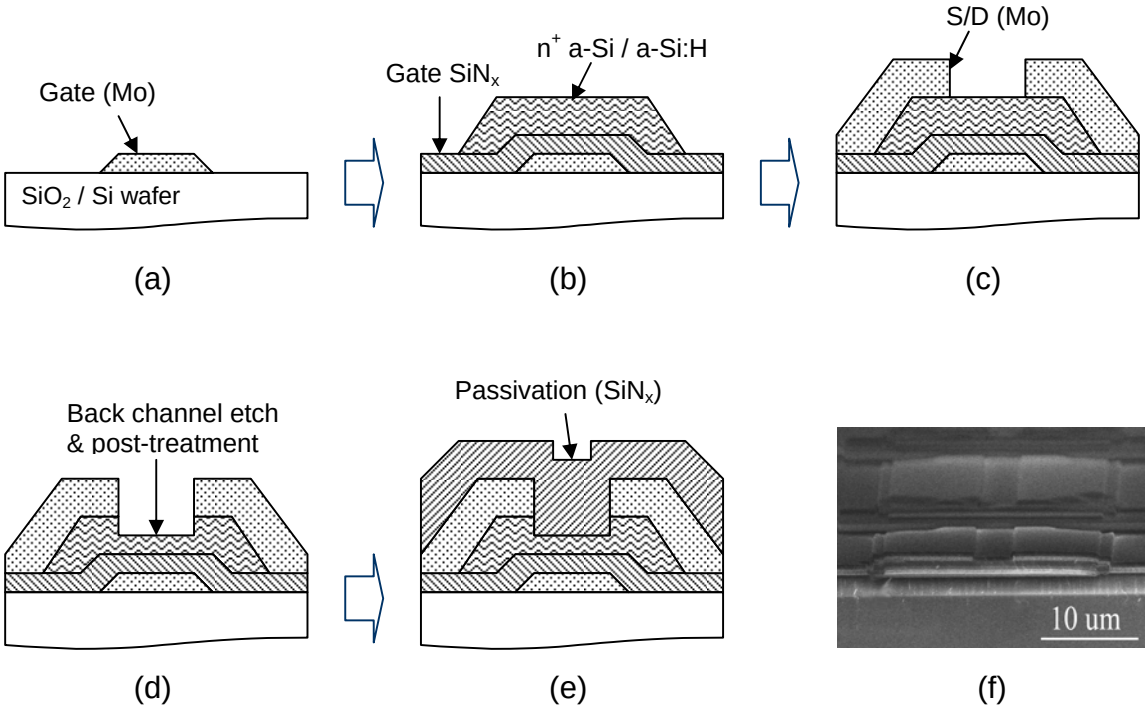


FIG. 4-1. Process sequence of TFT fabrication with back channel etch structure. (a) Gate electrode (Mo 200 nm), (b) active layers (gate SiN_x 300 nm, a-Si:H 200 nm, n^+ a-Si 50 nm), (c) source-drain electrode (Mo 300 nm), (d) back channel etch and post-treatment, (e) passivation (SiN_x 350 nm), (f) cross-sectional SEM image of inverted-staggered BCE-TFT.

semiconducting hydrogenated amorphous silicon, a-Si:H, thin film (200 nm) and a n^+ amorphous-Si contact layer (50 nm), respectively. The sputtering conditions for both films were 100 W RF power, 20 W (125 V) substrate bias, 5 mTorr pressure, 200 °C temperature, and 25 sccm Ar-H_2 gas flow. The n^+ a-Si and a-Si:H layers were photolithographically patterned and etched with an RIE (SF_6/O_2) using a single lithography and etch step (b). Next, Mo or Cr source-drain electrodes (250 nm thickness) were RF magnetron sputter deposited and lithographically defined and patterned by a wet etch process based on a mixed solution same as the etchant used in gate wet etch (c). In order to define the source and drain electrodes, a back channel etching (BCE) process was adopted with low damage (low RF power) etching on the back channel as this is a main source of leakage current of staggered BCE TFTs (d). Finally, to passivate the TFT array from chemical and mechanical attacks, a 350 nm SiN_x was sputter deposited with same conditions as the gate insulator. Finally, via holes were patterned for contacting the gate and source-drain electrodes (e). The electrical properties were measured using a semiconductor parameter analyzer, HP 4156A.

4.2.2 Staggered (top-gated) thin film transistor fabrication

Inverted-staggered BCE TFTs have several disadvantages in the fabrication process. First of all, it is very hard to control the depth of the BCE which can result in a S/D short or open if the depth is not controlled precisely. Secondly, the defects in the back channel resulting from BCE such as dangling bond cause high leakage currents and

threshold voltage shifts. In order to solve the problems in BCE TFT, a staggered (top-gated) TFT structure is introduced and the electrical properties for both TFTs are compared.

The brief process flow description is outlined below. Firstly, similar to the BCE TFT, Cr S/D (250 ~ 300 nm) is used for the S/D electrode deposited by RF sputter deposition. Ohmic contact n^+ a-Si (50 nm) is then deposited on the S/D electrodes without breaking vacuum in the sputtering system to enhance the ohmic contact properties. The condition of n^+ a-Si deposition is same as that of BCE-TFT. The S/D and n^+ a-Si is patterned by photolithography with the S/D mask and then etched by plasma etching based on SF_6/O_2 plasma for the n^+ a-Si and wet etched by Cr etchant for S/D electrodes, respectively (Fig. 4-2 (a)). The a-Si:H semiconducting layer is deposited by sputter deposition using the same conditions as the BCE-TFT. PECVD LPCVD or sputtering can be utilized for a-Si:H or poly-Si as a semiconducting layer respectively. The thickness of the film is 100 ~ 150 nm and a thinner semiconductor film is preferred to get higher transconductance and lower threshold voltage for ultimately higher TFT performance. The a-Si:H or poly-Si is patterned by conventional photolithography and dry etch based on an SF_6/O_2 plasma chemistry (b). Gate dielectric SiN_x is deposited by sputter deposition with substrate bias and the deposition condition is same as that of the BCE-TFT (c). Similar to the semiconducting layer, the gate dielectric also can be formed by PECVD or LPCVD. The Cr gate electrode is formed by sputter deposition at 200 °C and the thickness is 250 nm. The gate electrode is patterned by photolithography and etched with a Cr wet etchant (d). To passivate the device from external attacks, SiO_2

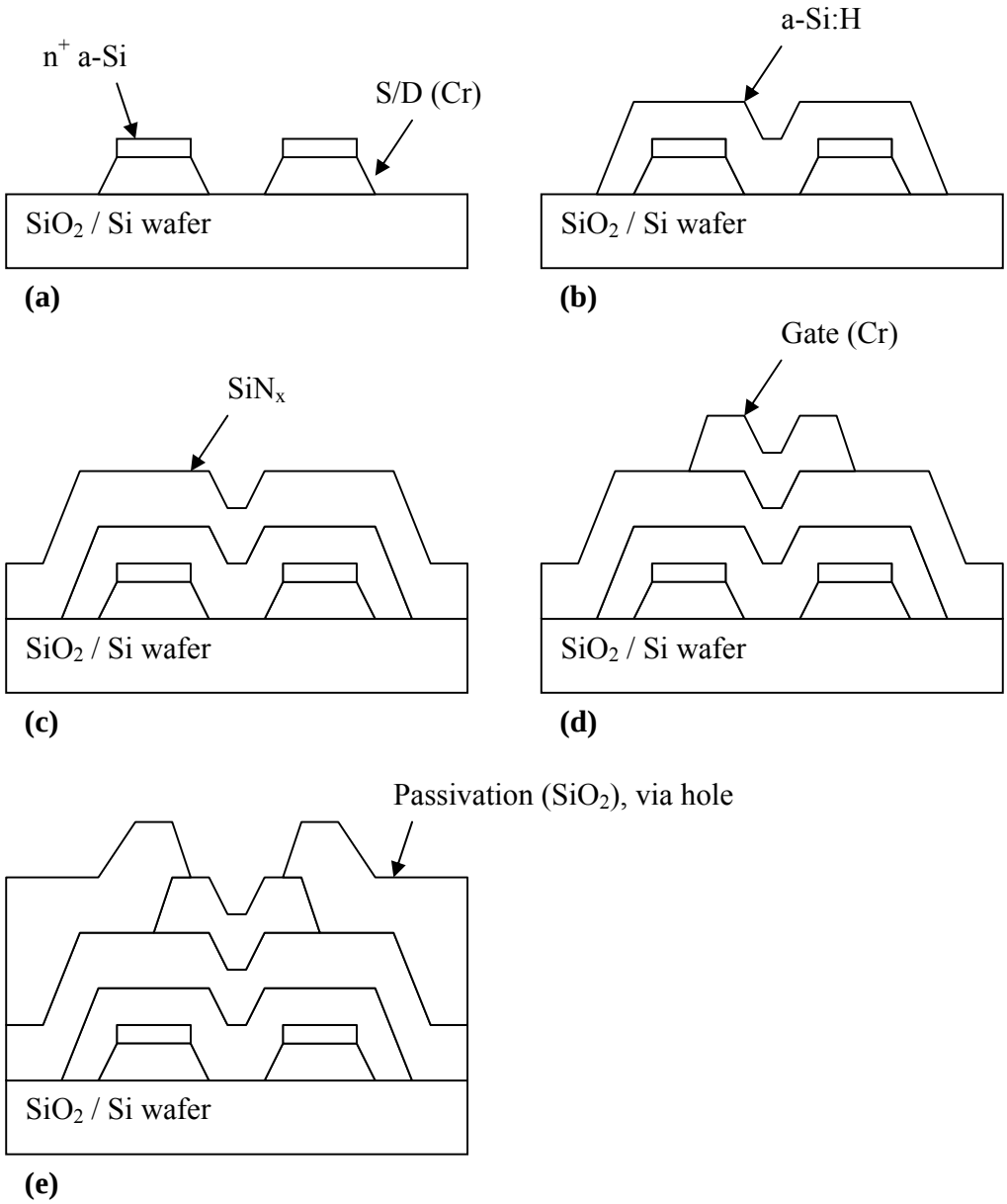


FIG. 4-2. Process sequence of TFT fabrication with staggered structure (top-gated). (a) S/D (Cr, 250 nm) and n^+ a-Si (50 nm) patterning, (b) a-Si (150 nm) patterning, (c) gate dielectric (SiN_x, 250 nm) deposition, (d) gate (Cr, 250 nm) patterning, (e) passivation (SiO_2, 300 nm) and via hole.

passivation is deposited by PECVD and patterned by photolithography and dry etched based on SF_6/O_2 plasma to form via holes for contacting the gate and S/D electrodes (e).

4.2.3 Parameter extraction

The electrical parameters such as field effect mobility and threshold voltage were obtained by the method and equations described below.

In the saturation region, transconductance is defined by;

$$g_m = \frac{\delta I_D}{\delta V_G} \cong \frac{W}{L} \mu C_i (V_G - V_T)$$

where I_D is drain current, V_G is gate voltage, W is channel length, L is channel length, μ is field effect mobility, C_i is capacitance per unit area, and V_T is threshold voltage.

Using the definition of the constant K given below, we can define g_m as given below as:

$$K = \frac{W}{L} \mu C_i, \quad g_m = \frac{\delta I_D}{\delta V_G} \cong K(V_G - V_T).$$

Therefore, in saturation $V_G = V_T$ *at* $g_m = 0$

The threshold voltage is obtained by two methods and then averaged.

First method; in the saturation region,

$$I_D = \frac{1}{2} K(V_G - V_T)^2, \quad \text{so} \quad \sqrt{I_D} = \sqrt{\frac{K}{2}}(V_G - V_T) \quad \text{and at} \quad \sqrt{I_D} = 0, \; V_G = V_T$$

Second method (Fig. 4-3); this is the most straightforward way to get threshold voltage without calculating a K value. The V_T is obtained by plotting I_D *vs* $[V_G - V_D/2]$ in

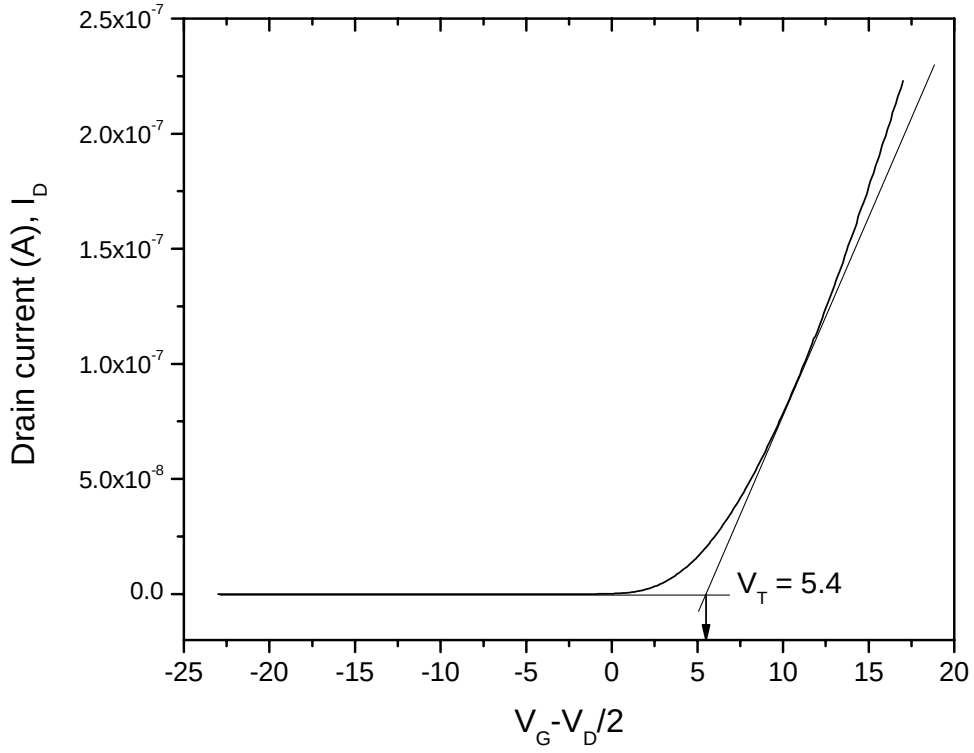


FIG. 4-3. Example of illustrating the calculation of threshold voltage. (By plotting I_D *vs* $[V_G\text{-}V_D/2]$ on the TFT operating region (linear region) and reading out the threshold voltage off the x-intercept).

the linear TFT operating region and then extrapolating the linear portion of the curve to the *x*-intercept. This method is widely used to get V_T since the first method has difficulties in calculating several variables such as the exact capacitance per unit area of the gate dielectric film, channel width, and length. Usually the channel length and width are different from the designed dimensions after device fabrication due to CD loss. The V_T from the second method is obtained from the current-voltage output of TFT itself without incorporating these variables. The equations to get V_T from the x-intercept described in this second method are described below.

$$I_D = K\left[(V_G - V_T)V_D - \left(\frac{1}{2}\right){V_D}^2\right]$$

$$I_D = K\left[\left(V_G - V_T) - \frac{V_D}{2}\right)\right]V_D = K\left[\left(V_G - \frac{V_D}{2}\right) - V_T\right]V_D$$

$$When \;\; I_D = 0, \quad V_T = \left(V_G - \frac{V_D}{2}\right)$$

4.3 Electrical property characterization of thin film transistor fabricated with substrate biased sputter deposition

4.3.1 Direct current substrate bias effects on the electrical characteristics of amorphous silicon thin film transistors

To show the effect of substrate biased films on the TFT performance; the electrical properties of TFTs with the a-Si active layer sputtered with (10W, 110V) and

without substrate bias are compared. Mo was used as gate and S/D electrodes for the TFT and the gate dielectric was SiO_2 deposited by sputter with 20 W of substrate bias. As shown in Fig. 4-4, the on-state current of the biased a-Si TFT (b) is slightly higher than that of an unbiased a-Si TFT (a), which means that the biased a-Si TFT has a higher transconductance and field effect mobility. Secondly, the leakage (off-state) current of the biased a-Si is much lower than that of unbiased a-Si TFTs. The defect density in the unbiased films likely causes the high leakage current in the unbiased a-Si TFTs. On the other hand, the biased a-Si TFT has an extremely low leakage current (less than a pico-ampere) because the biased a-Si is denser and has fewer defects.[77] As shown in the figure, the TFT properties using SiO_2 gate dielectric has very poor electrical characteristics such as low on/off current ratio and very high threshold voltage. To improve the transconductance and switching characteristics of the TFTs, a SiN_x dielectric film was introduced.

4.3.2 The effect of the TFT dimensions on the electrical characteristics of the TFTs

Fig. 4-5 shows the electrical characteristics of five TFTs measured in different die across the 4-inch wafer, which shows that the thin films are uniform across the entire wafer and the device characteristics are very stable. To characterize the TFTs, the gate voltage was swept from -20 V to 30 V at 0.5 V intervals and drain voltage was fixed at 7 V. As shown in the figure, the electrical properties of the TFTs within a 4-inch wafer are very uniform and the deviation in the electrical characteristic is below 2 % for every

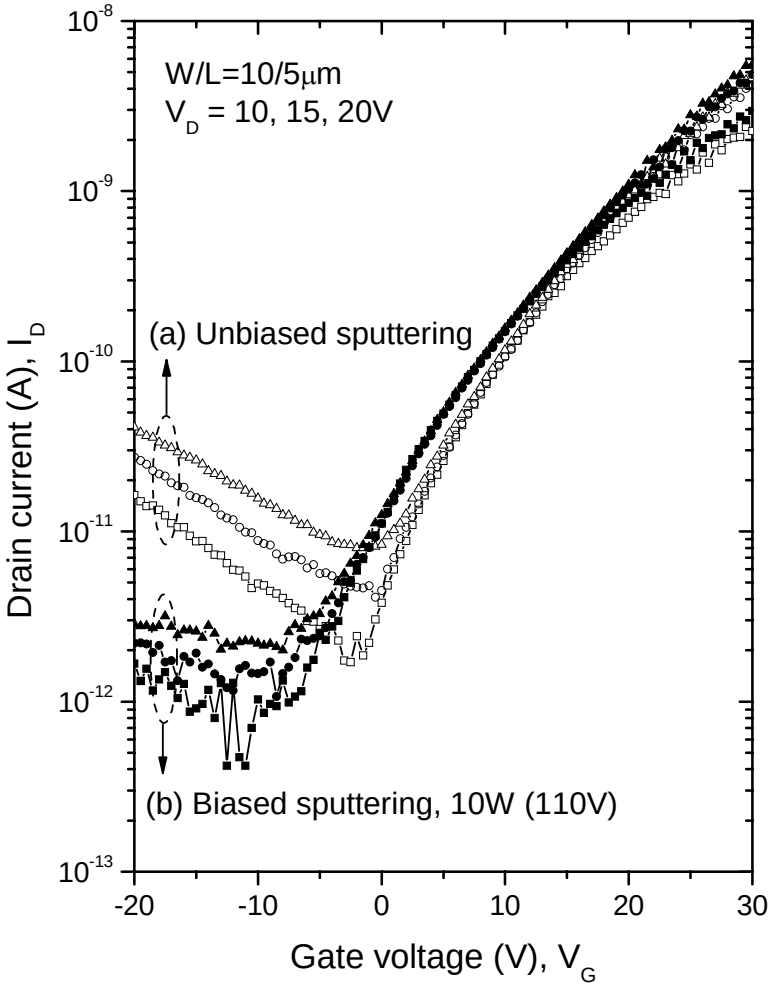


FIG. 4-4. Transfer characteristics of TFTs. (a) Unbiased a-Si TFT, (b) DC biased a-Si TFT (both are characteristics before annealing).

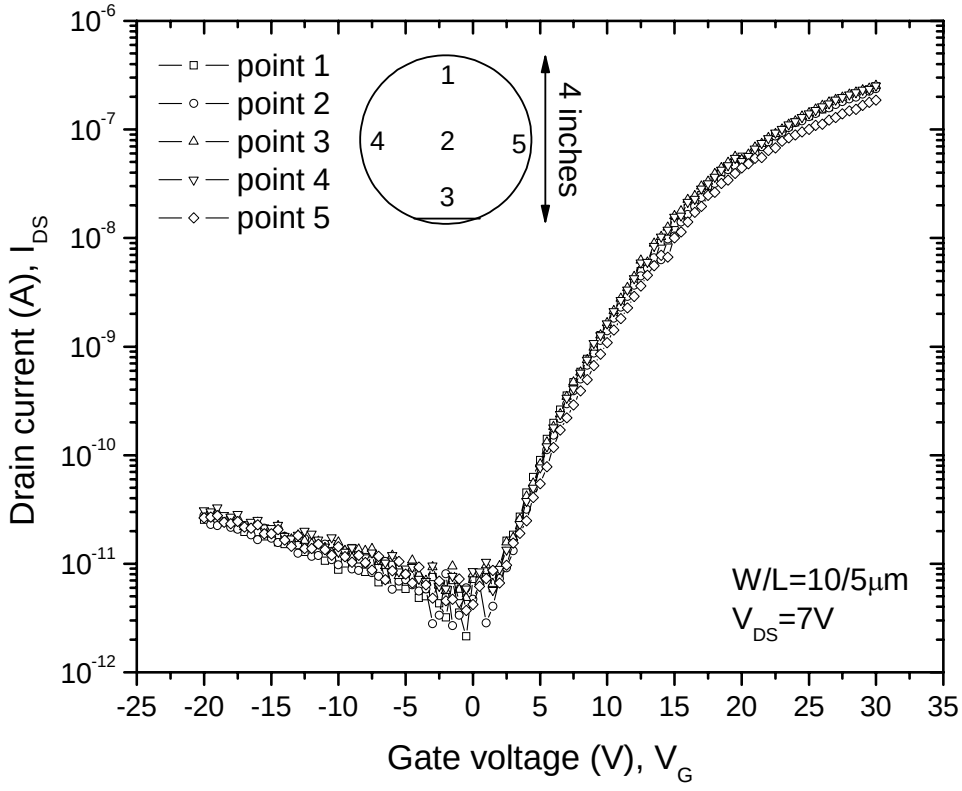


FIG. 4-5. Current-voltage characteristics of TFT devices as a function of the wafer position which illustrates the stability of the device characteristics.

point. The current-voltage characteristics of the TFT with a 20 W (125 V) biased SiN_x gate insulating film (300 nm) and 10 W (110 V) biased a-Si:H / n^+ a-Si are shown in Fig. 4-6. Cr was used as gate and S/D electrodes for this TFT. The channel width and length are 10 and 5 μm respectively and an applied drain voltage is 1 V to 9 V (2 V step). The TFT has the following electrical characteristics; 7.0 V threshold voltage, 0.38 cm^2/Vsec field effect mobility, greater than 10^5 on/off current ratio, and less than a pico-ampere off-current (leakage current) at V_G = -8 V and V_{DS} = 1, 3 V.

Fig. 4-7 and Fig. 4-8 show the electrical properties of the TFT with different channel lengths (2 to 8 μm) and widths (10 to 40 μm). The threshold voltage (V_T) in the Fig. 4-7 increases with increasing channel length, which likely results from the increase in the channel resistance as the channel length increases. The on-state current, as shown in Fig. 4-8, is increased slightly with increasing channel width and the threshold voltage decreases with an increase in channel width due to the increased field effect area at higher the channel widths.

4.3.3 The effect of post-annealing ambient on the electrical characteristics of the TFTs

Fig. 4-9 shows the electrical characteristics of the TFT with various annealing conditions. Of particular note in this figure is the change in the off-current with various annealing conditions after the TFT fabrication. The annealing was processed at 500 ^oC, and 5 mTorr pressure in Ar or Ar-H_2 (5 % H_2) ambient for 3 hours. The off-current of the TFT after annealing in Ar is higher than the device before annealing. This is

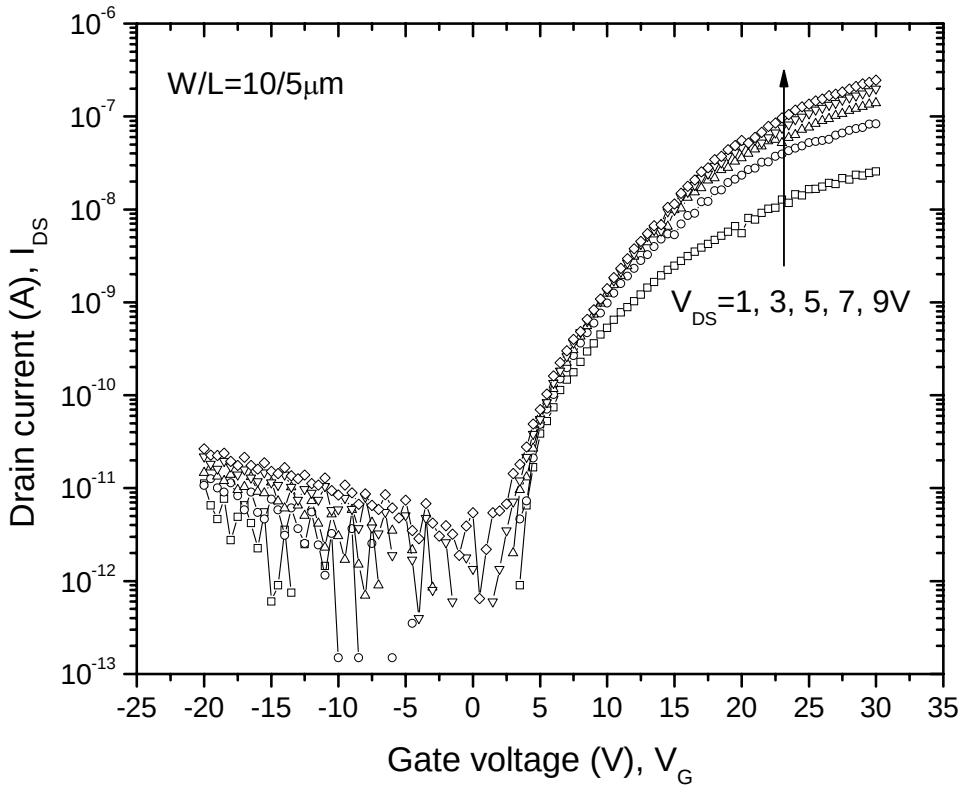


FIG. 4-6. Current-voltage characteristics of a fully sputtered TFT.

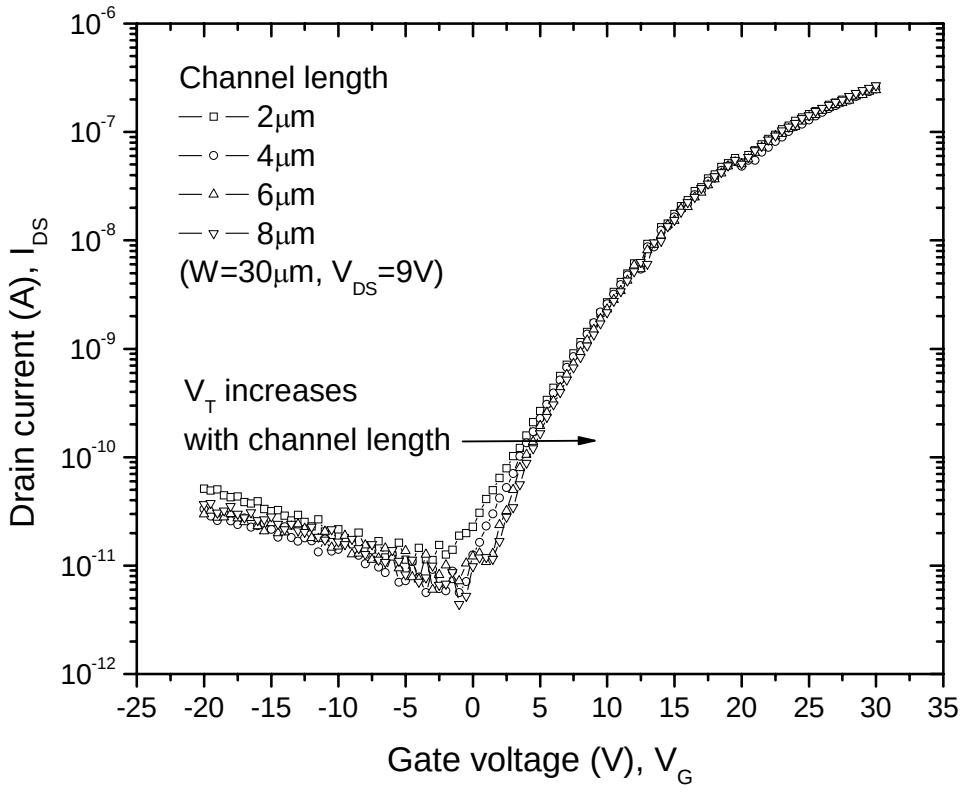


FIG. 4-7. Current-voltage characteristics of fully sputter-deposited TFTs as a function of channel length.

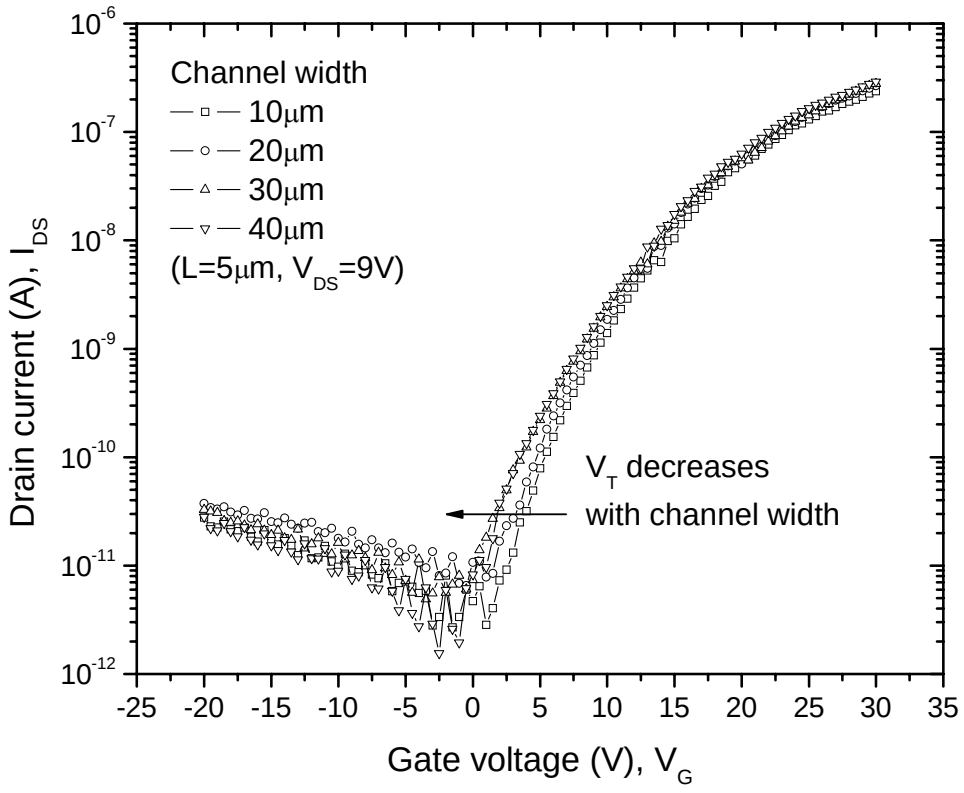


FIG. 4-8. Current-voltage characteristics of fully sputter-deposited TFTs as a function of channel width.

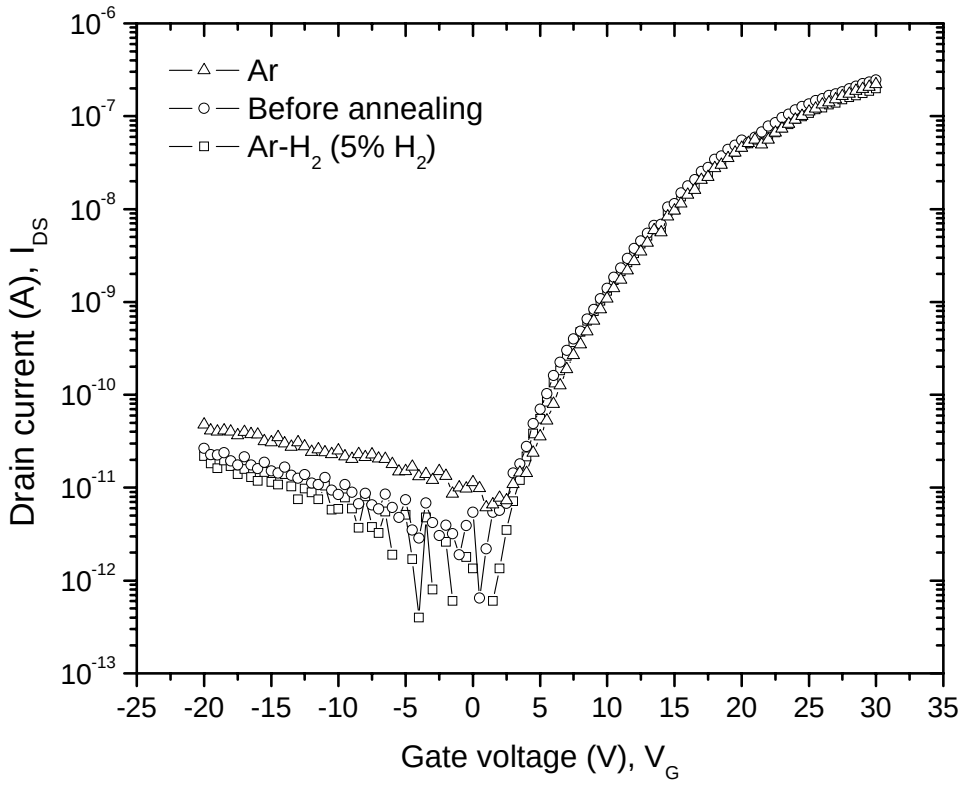


FIG. 4-9. The electrical properties of fully sputter-deposited TFTs as a function of the annealing ambient. (Ar and Ar-H_2 ambient).

attributed to dehydrogenation of the a-Si at relatively high temperatures ~ 500 ^{o}C. The annealing reduces the concentration of hydrogen in a-Si:H films and consequently degrades the electrical device performance of TFTs and solar cells unless the dangling bonds are also eliminated. Unpassivated dangling bonds are a main source of electron scattering and trapping in electron conduction. A publication reported that the properties of a-Si:H are changed with the annealing at 350 ^{o}C, 450 ^{o}C, and 575 ^{o}C corresponding to the conversion of SiH_3 to SiH_2 and SiH with dehydrogenation.[83],[84] On the other hand, after annealing in an Ar-H_2 ambient at 500 ^{o}C, the off-current is slightly lower than the as-deposited device. Hydrogen atoms in amorphous silicon films play an important role in compensating defects, for example dangling bonds and lattice defects. Hydrogen passivates these defects by combining and effectively neutralizing these defects which otherwise contribute to a high off-current. On the other hand, there are no significant changes in the on-current with the annealing conditions. This suggests that the dehydrogenation mainly occurs in the back channel, which is contacted with the passivation SiN_x film, rather than in the gate SiN_x / a-Si:H interface. Consequently, the dehydrogenation from the back channel a-Si:H / passivation SiN_x interface generates the high off-current and does not significantly effect the on-current.[83],[68]

4.3.4 The effect of back channel etch depth on the electrical characteristics of the TFTs

The electrical properties of the TFT as a function of the back channel etch depth are shown in Fig. 4-10. The off-state current increases and the on-state current decreases,

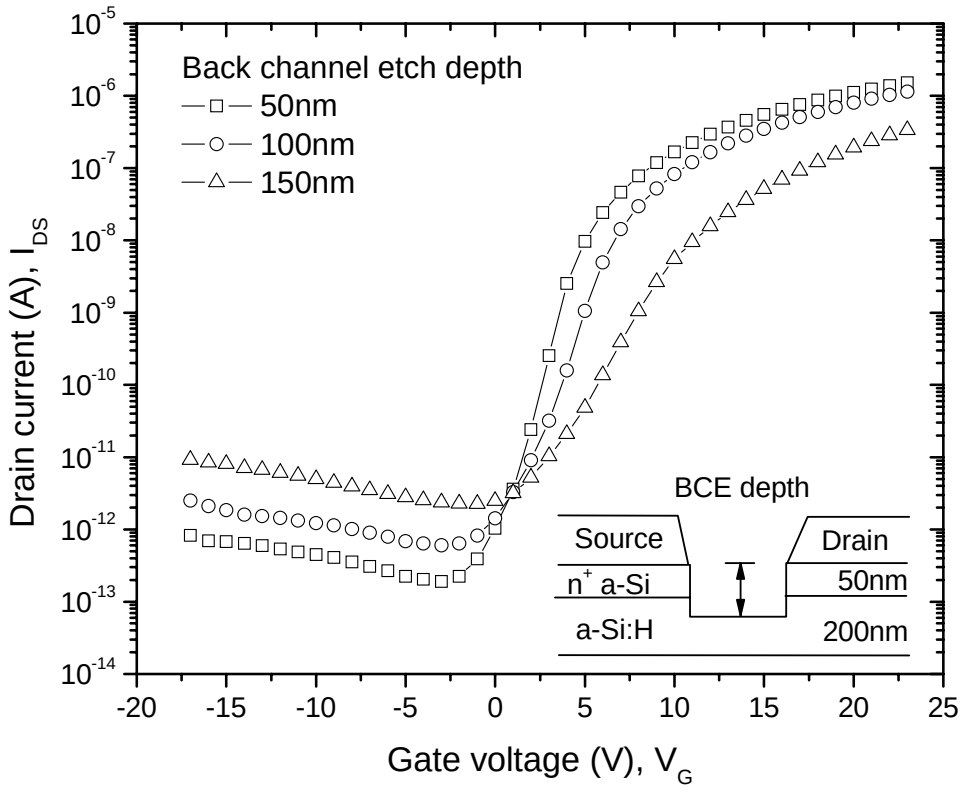


FIG. 4-10. Electrical property changes of fully sputter-deposited TFTs with back channel etch depth.

respectively, with an increase in the back channel etch depth. This means that the longer and deeper back channel etch damages this region and creates interface defects, which generates a higher off-current and decreases the on-current. Furthermore, the actual thickness of a-Si:H is also decreased with deeper etch and it results in lower on- current and lower on/off current ratio due to the thinning of the a-Si:H film. Additionally, an increase in threshold voltage is observed with increasing the back channel etch depth resulting in more electron trapping by interface defects with the deeper back channel etch. In the inverted-staggered TFT with a channel-passivated (CHP) structure, the off-current is largely controlled by hole injection from the drain electrodes at room temperature and in the dark state. That is, the off-current is strongly influenced by the ohmic contact resistance between a-Si:H and source-drain electrodes and not significantly affected by a-Si:H thickness.[85,86] The effect of a-Si:H thickness is mainly shown in photoconductivity measurements under illumination and the photocurrent generated by electron-hole pairs is directly related to the a-Si:H film thickness. The off-current, generally speaking, decreases with the thinning of the a-Si:H in the CHP TFT.[68] Unlike the CHP TFT, in the back channel etched (BCE) structure used in this study, the overall electrical properties including off-current at room temperature vary with the back channel etch depth (actual a-Si:H thickness). One can conclude that controlling the back channel etch process is one of most important process factors to control the TFT electrical characteristics. To further illustrate the importance of the back channel etch region, it was recently reported that the BCE-TFT properties can be enhanced by oxidizing the back channel by plasma treatment.[87]

4.3.5 The effect of gate dielectric thickness on the electrical characteristics of the TFT

Fig. 4-11 shows the electrical property change with gate SiN_x thickness. The TFT with the thin gate SiN_x has a lower threshold voltage, higher on-current, and higher on/off current ratio than TFT with thicker gate SiN_x. The threshold voltage, on/off current ratio, and field effect mobility are enhanced from 4.8 V to 1.2 V, 10^5 to 10^7, and 0.32 to 0.46 cm^2/Vs, respectively, with a decrease in the gate SiN_x thickness from 300 nm to 150 nm. To achieve more stable TFT processing, using a 300 nm thickness of SiN_x is recommended since there is high possibility a device failure due to an over-etched active layer such as gate attack and gate-S/D short.

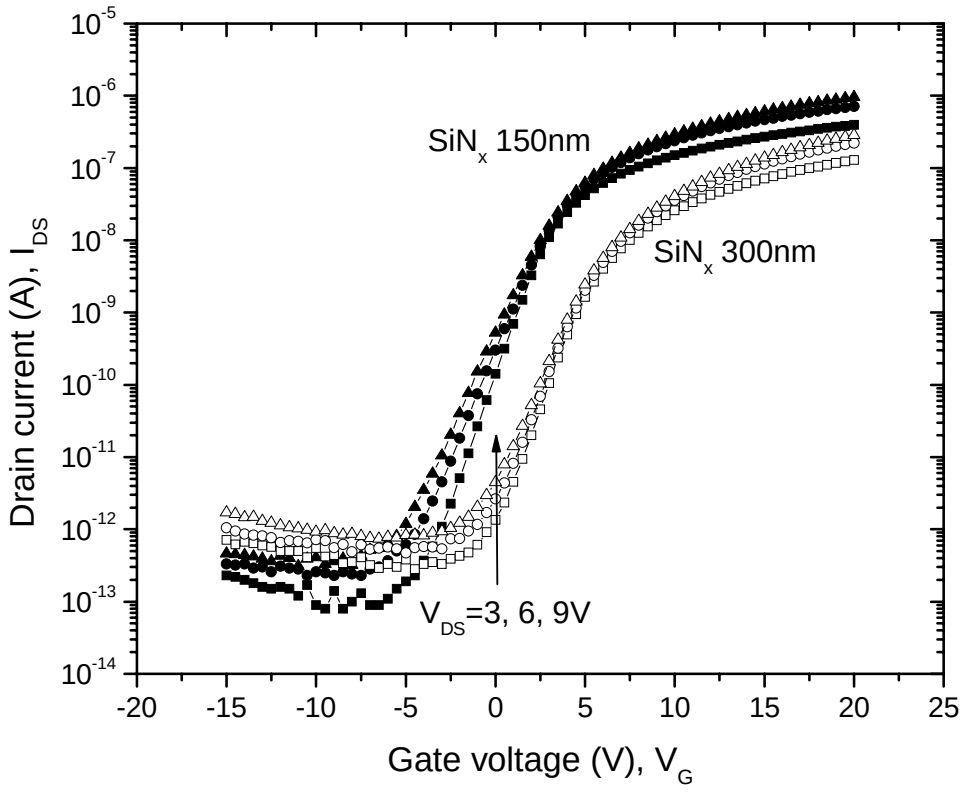


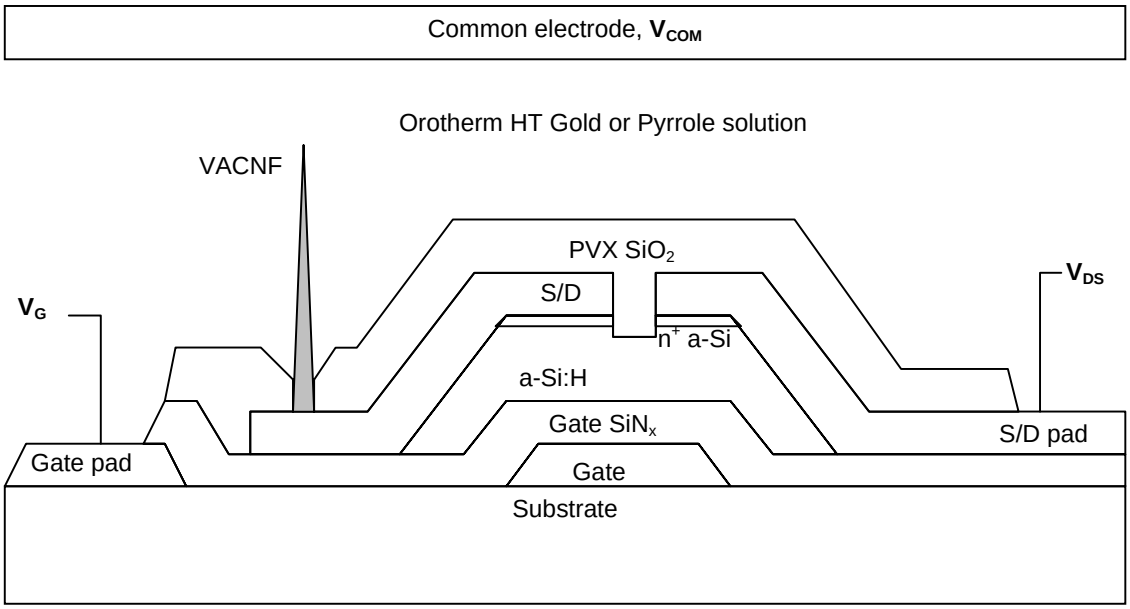
FIG. 4-11. Electrical property changes of fully sputter-deposited TFTs with gate SiN_x thickness.

Chapter 5 Electrochemical analysis

To show the addressability of thin film transistor array, electrochemical measurements were performed using gold and pyrrole solution. The metrology and characteristics for localized electrochemistry to demonstrate the addressability of the TFT array are described in this chapter.

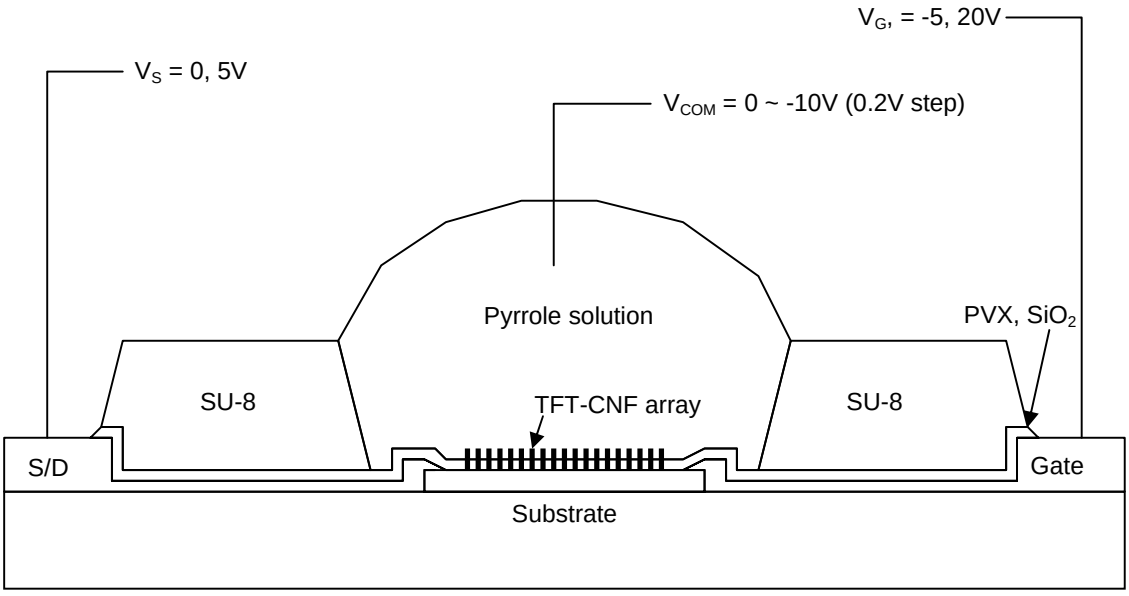
5.1 Electrochemistry analysis with TFT-VACNF using gold and pyrrole solution

Fig. 5-1 (a) shows a cross-sectional diagram of TFT addressed VACNF. A VACNF is grown on the drain of the TFT and Orotherm HT gold or pyrrole solution is filled between the TFT-VACNF and the common electrode. An overall diagram of electrochemical measurement is shown in Fig. 5-1 (b). A 15 μm thick SU-8 (2010) film is patterned on the 20×20 TFT active area to make a well for containing the solution. The coating condition of SU-8 was 3000 rpm, 60 seconds and then baked at 65 °C for pre-heating to minimize thermal shock and baked consecutively at 95 °C for 90 seconds. The soft-baked SU-8 was exposed by UV light with a 30 second exposure time on a contact mask aligner and then post-exposure-baked (PEB) with the same condition as soft-baking. The developing time was 70 seconds without agitation and then rinsed by Isopropyl Alcohol (IPA) and DI water. An optical photograph of the measurement is shown in Fig. 5-1 (c). The photography shows SU-8 passivation and active areas filled with



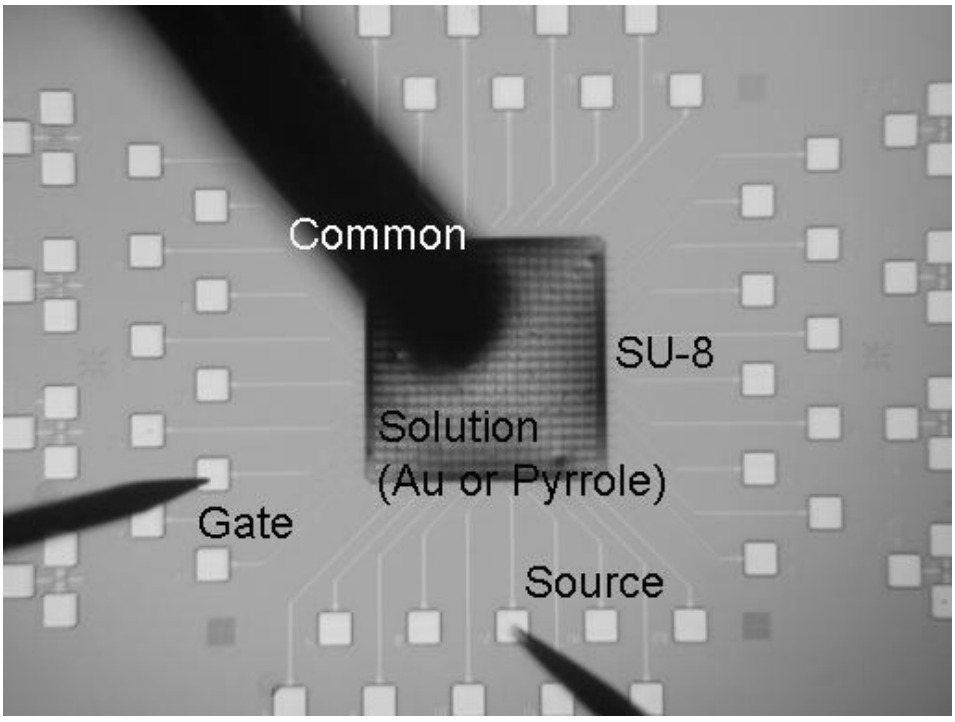
(a)

FIG. 5-1. A schematic diagram of TFT-VACNF for electrochemical analysis. (a) A cross-sectional diagram of TFT addressed VACNF.



(b)

FIG. 5-1. Continued. (b) An overall diagram of electrochemistry measurement.



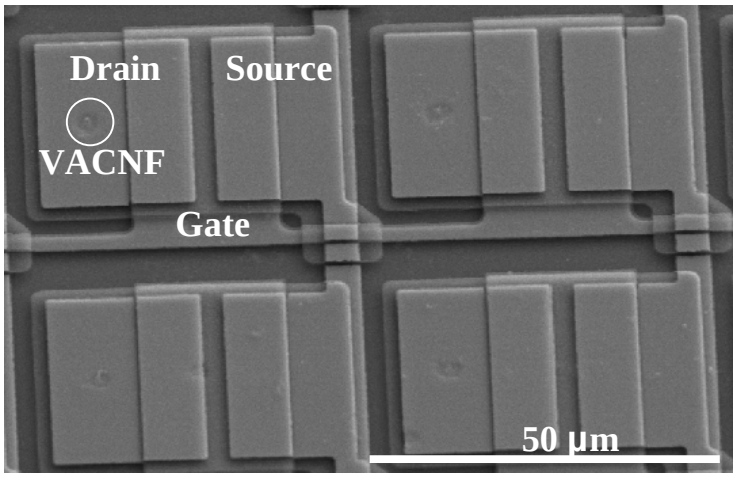
(c)

FIG. 5-1. Continued. (c) An optical photography of the measurement.

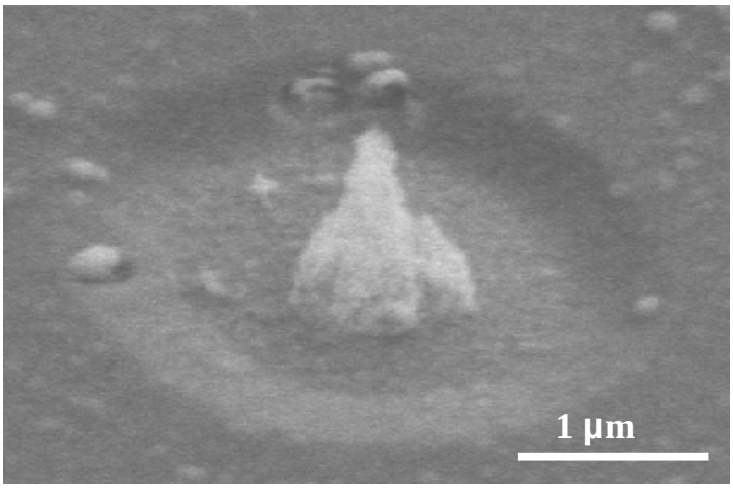
electrochemical solution. Electrical fields are applied on a specific gate and source (data) lines and the output current is collected on the common electrode.

Fig. 5-2 shows SEM images of the TFT-VACNF integrated device where the VACNF is covered with SiO_2 passivation except for the tip of the VACNF which is emancipated by the process as shown in chapter 3. The growth condition of VACNF and process sequence of TFT-VACNF integration is also described in chapter 3 (Fig. 3-27, 3-28). Fig. 5-3 shows the current change of the common electrode as a function of applied voltage on common electrode. Gold solution (Orotherm HT Gold) may be used to show electrochemical properties of individually addressed electrodes.[40] To measure the electrochemical properties of the gold solution with a grounded TFT, the applied gate and source voltages are all zero, that is, grounded and all others are floating states (not probing). The voltage applied on common electrode was swept from 3 V to -3 V with 0.02 intervals. As shown in the figure, there is a significant voltage drop at ~ ±2 V which means gold deposition is occurring on either the common electrode or the VACNF. Usually gold is deposited on negative electrode upon overpotentials ~ -1 V.[40] In the case of this analysis, the overpotentials indicated by the current spike is higher than the ~1V reported due to the higher resistance of TFT channel. In spite of current change illustrated in Fig. 5-3, SEM analysis of the VACNFs after the electrochemical analysis did not reveal any gold deposition on the fibers. It is speculated that deposition occurred on the common electrode.

Another solution for electrochemical analysis is pyrrole electrochemistry. Pyrrole is a conductive polymer and the conduction mechanism of pyrrole is due to interchain



(a)



(b)

FIG. 5-2. SEM images of TFT-VACNF. (a) TFT-VACNF, (b) VACNF on drain electrode of TFT.

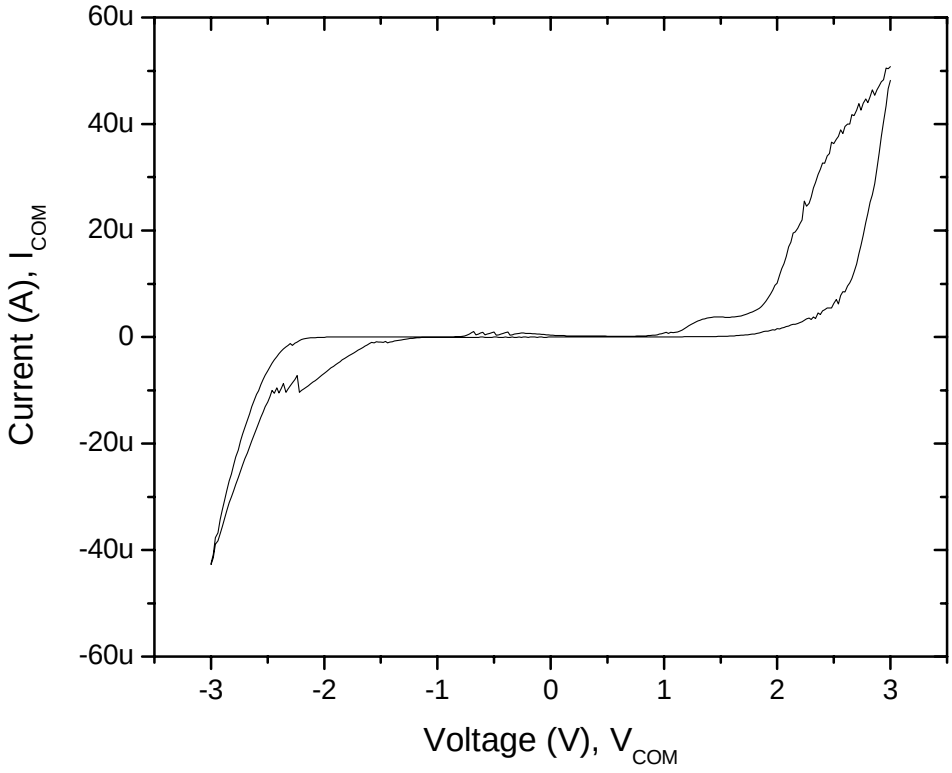


FIG. 5-3. Current change of common electrode as a function of applied voltage on common electrode.

hopping of electrons (Fig. 5-4). It provides an easy preparation for standard electrochemical techniques and surface charge characteristics of polypyrrole can easily be modified by changing the dopant anion (X^-) that is incorporated into the material during synthesis.

Fig. 5-5 shows the current-voltage characteristics on the common electrode as a function of pyrrole concentration. Pyrrole was diluted with *KCl* solution. The current through the common electrode induced by the applied voltage increases with an increase in pyrrole concentration.

Fig. 5-6 shows current-voltage characteristics of pyrrole electrochemistry with an applied voltage cycle. As reported, the growth of polypyrrole film begins at the potential of about 0.4 V which is shown with an abrupt increase in the current.[88] As shown in Fig. 5-6 (a) and (b), initially the current decreases with each cycle and then increases after few cycles. At the initial stage of forming polypyrrole, the current decreases with each cycle as shown in Fig. 5-6, (1), (2). This is attributed to a nucleation process of polypyrrole resulting in current decrease with each cycle. After few cycles, the current subsequently increases with each cycle and then saturates which indicates the formation of polypyrrole.[89]

5.2 Electrochemical analysis of TFT array with fully active addressed scheme

Active Matrix addressing involves the use of an electronic switch at every pixel. Once a pixel is switched on, the field can be maintained by the switch while other pixels

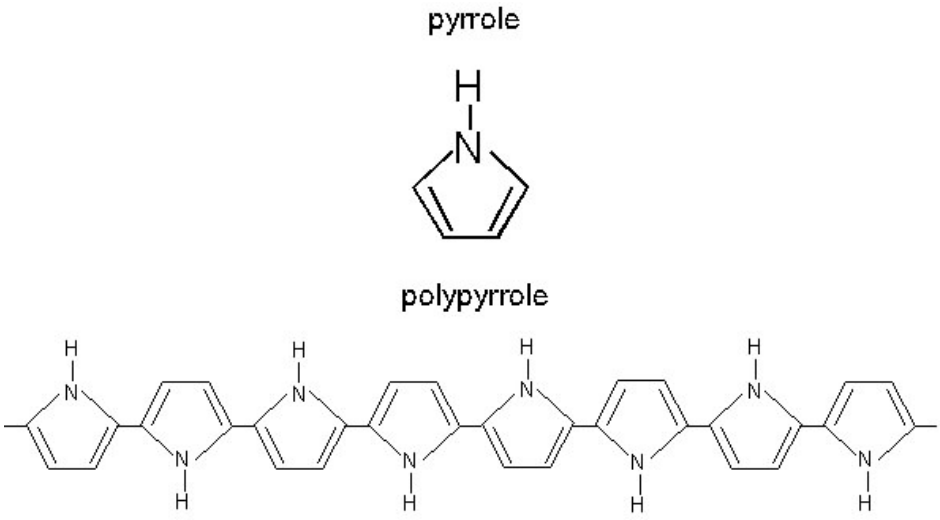


FIG. 5-4. Molecules structure of unit pyrrole (monomer) and polypyrrole.

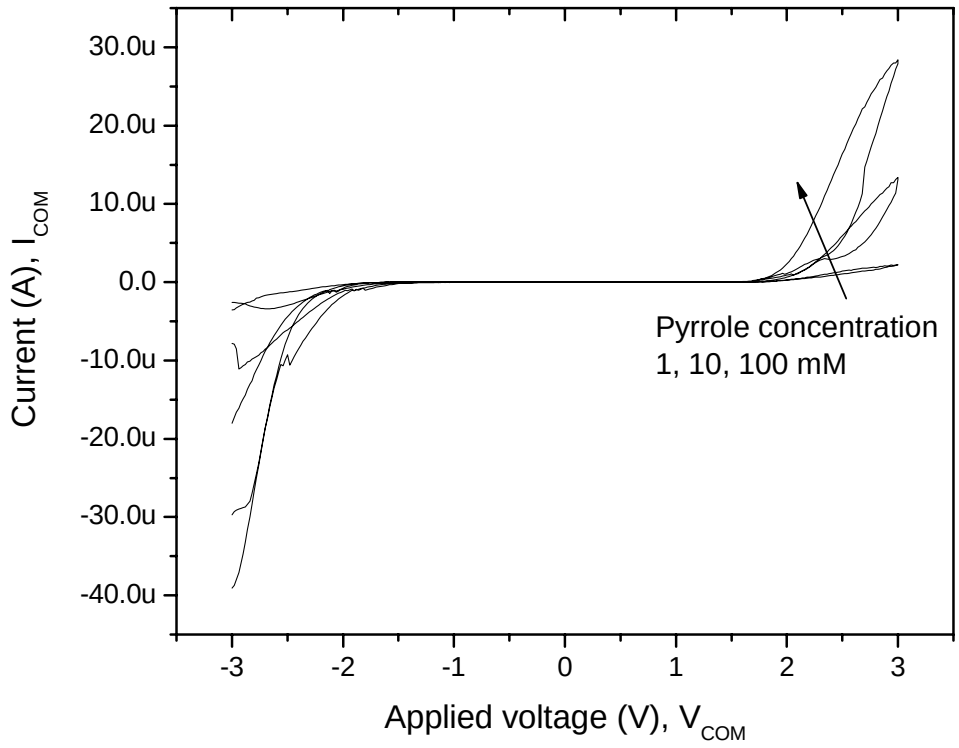
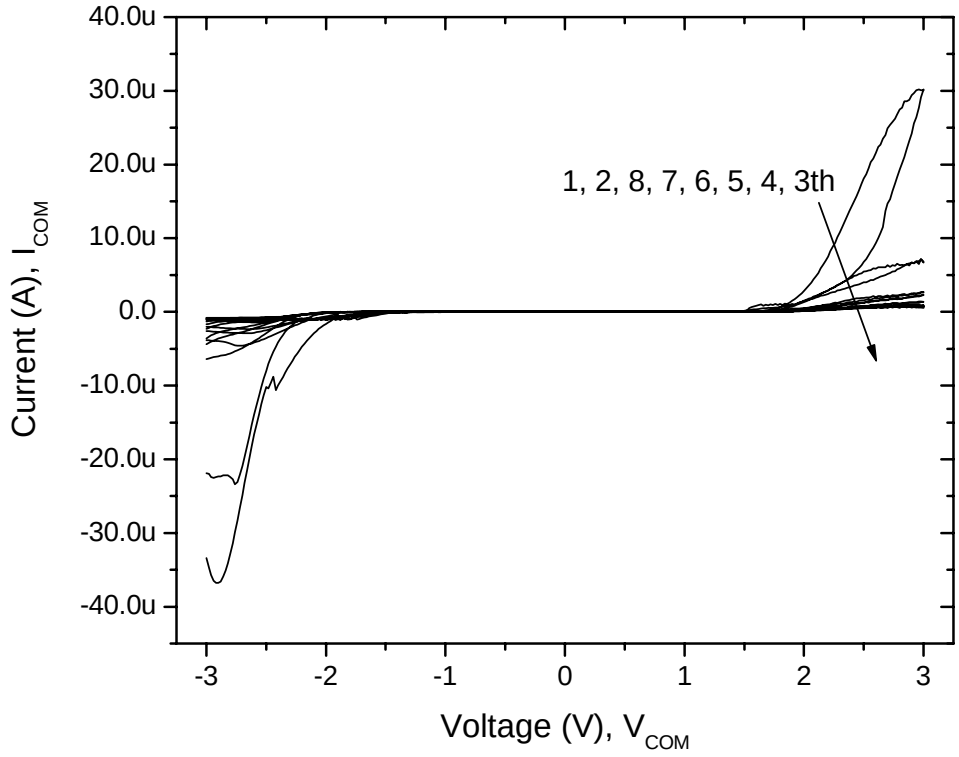
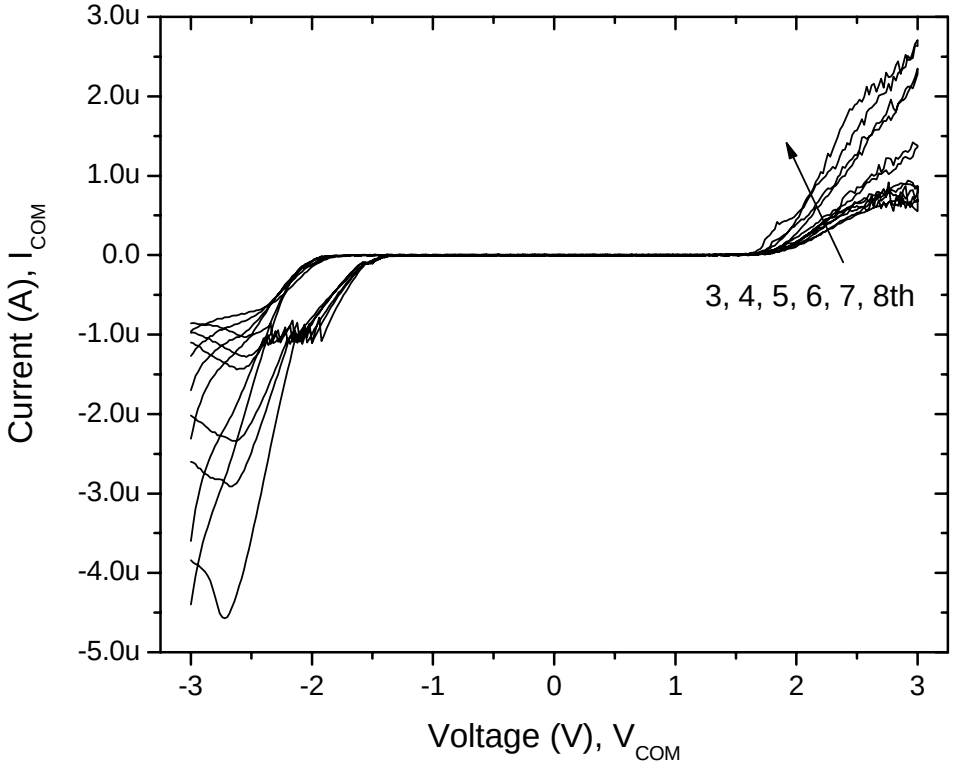


FIG. 5-5. Current-voltage characteristics on common electrode as a function of pyrrole concentration.



(a)

FIG. 5-6. Current-voltage characteristics of pyrrole electrochemistry with cycle analysis. (a) Full cycles.



(b)

FIG. 5-6. Continued. (b) From 3rd to 8th cycles.

are turned off. A TFT also isolates the pixel from the influence of adjacent pixels so that crosstalk isn't a problem either. In this section, the scheme and electrochemical result of active addressing using a TFT array will be described.

A typical current-voltage characteristic of TFT is shown in Fig. 5-7. The TFT operating voltage at 'ON' and 'OFF' states are 20 ± 2 V and -5 ± 2 V respectively. Usually on/off current ratio of a-Si TFT is $10^5 \sim 10^7$ and leakage current at -8 V gate voltage is below few pico-ampere. Fig. 5-8 shows a diagram of active addressing scheme using TFT array. There are two sets of addressing lines; horizontal gate lines and vertical data lines. A TFT is integrated at etch intersection of these addressing lines to turn on and off the voltage. To turn-on a specific TFT, a 20 V gate voltage is applied on a gate line to be addressed while the other gate lines are addressed with -5 V to be turned off. Then a source voltage (V_{DS}) is applied on the data line. The induced charge on the drain electrode of the TFT induces a potential difference with common electrode through electrolyte such as gold or pyrrole solution. Fig. 5-9 shows SEM images of 20×20 TFT array with via hole for electrochemistry. The size and depth of via hole are about 0.8 μm and 300 nm respectively. Fig. 5-10 shows a 20×20 TFT array chip after dicing, wire bonding, and mounting. To cut the finished substrates into individual die, a 4-inch wafer was diced by Disco Dad/2H6T Dicing Saw which all alignment to the substrate is performed by a split field video stereo microscope. After dicing the substrate into 5 mm × 5 mm chip, the chip was wire-bonded by K&S Wire Bonder with Aluminum (Al) wedge and Gold (Au) ball bonders. A melted and solidified epoxy was used to passivate a chip and isolate a chip from gold solution. Fig. 5-11 demonstrates a digital picture of

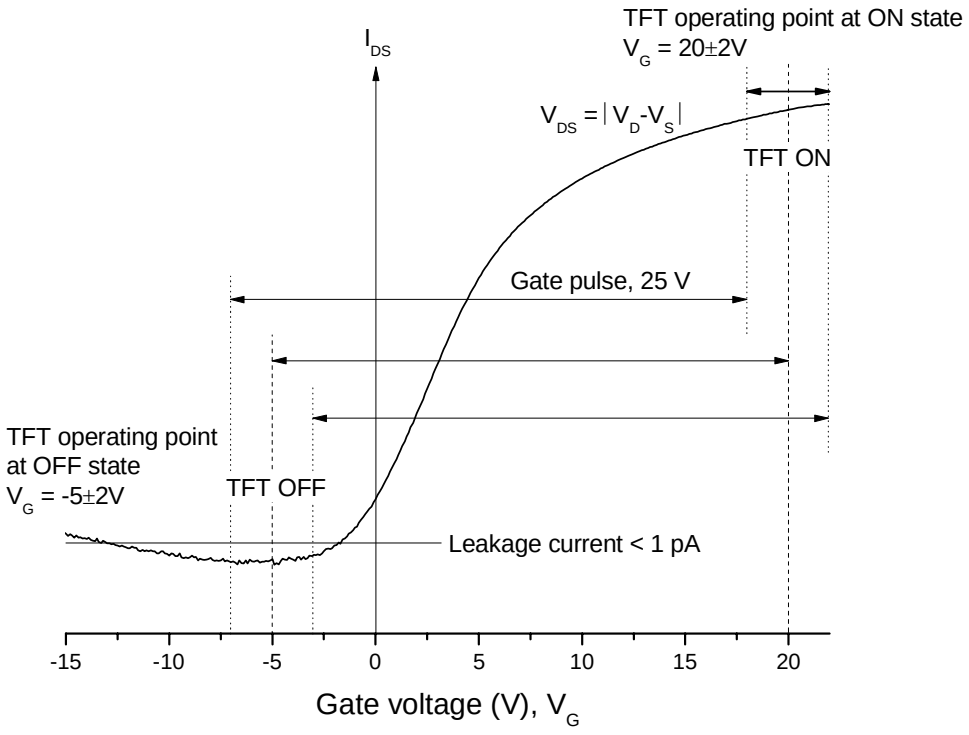


FIG. 5-7. A typical current-voltage characteristic of a-Si:H TFT.

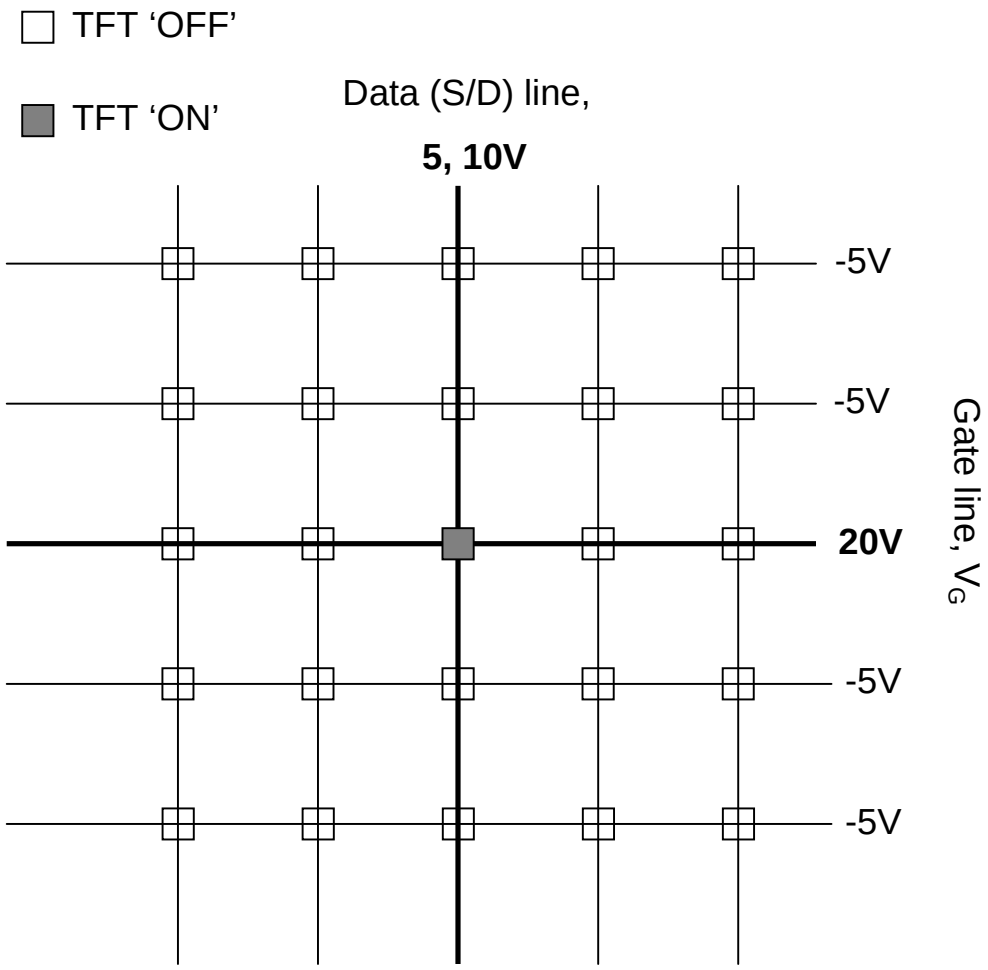
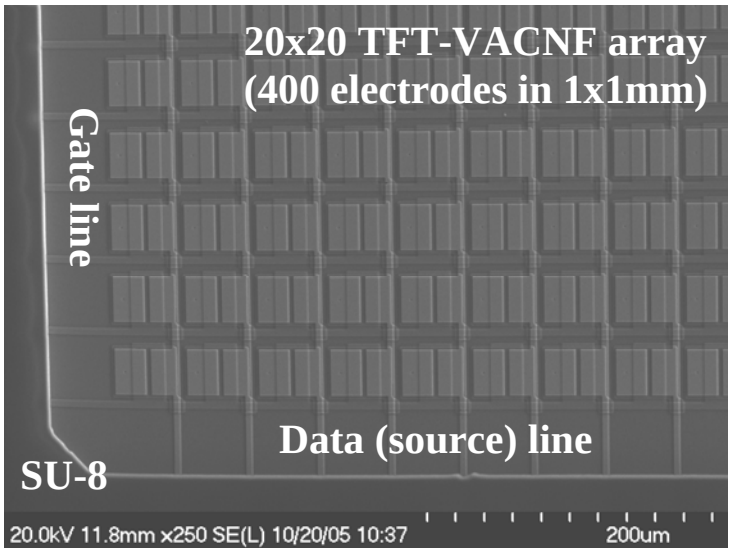
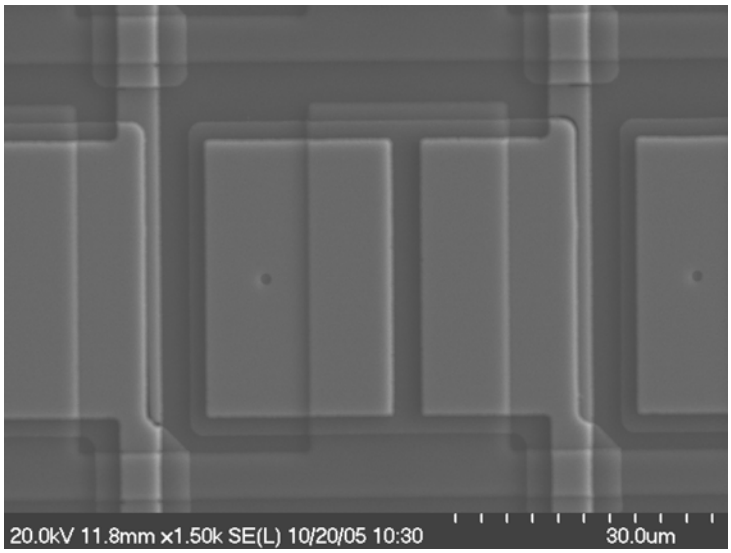


FIG. 5-8. A diagram of active addressing scheme using TFT array.

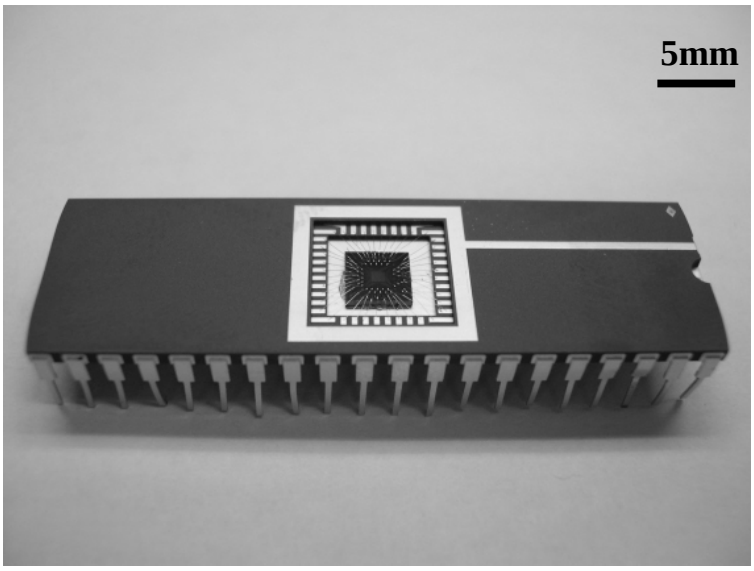


(a)

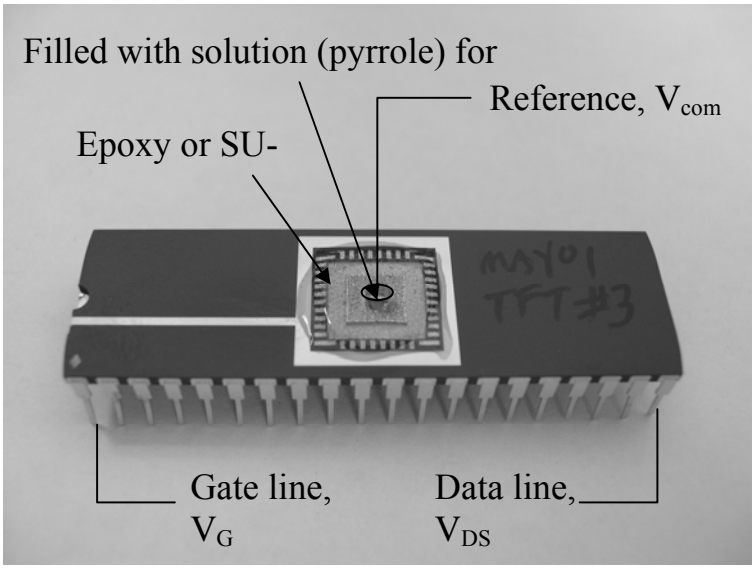


(b)

FIG. 5-9. SEM images of 20×20 TFT array with via hole for electrochemistry.



(a)



(b)

FIG. 5-10. 20×20 TFT array chip after dicing, wire bonding, and mounting.

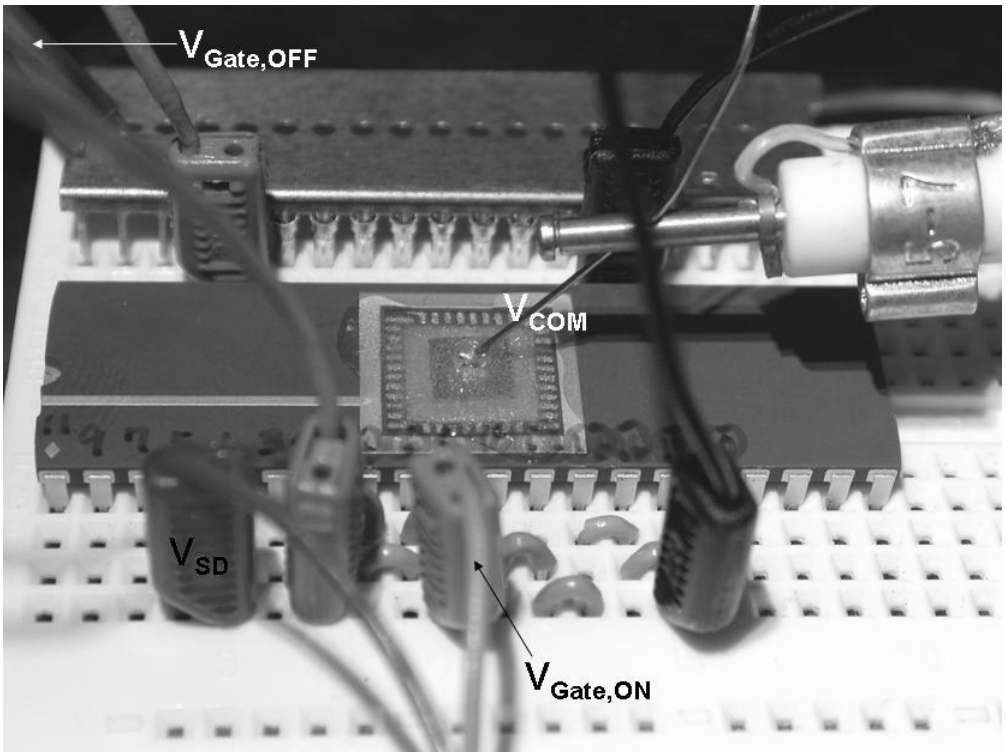


FIG. 5-11. A scheme picture of active addressing which is mounted on multi-functional slots.

the active addressing array which is mounted onto multi-functional slots. The applied gate voltage to turn on a specific TFT was 30 V ($V_{Gate, ON}$) and all others are -5 V for maintaining 'OFF' ($V_{Gate, OFF}$). Source-drain voltage (V_{DS}) is applied on a specific data line to be addressed and then the voltage on the common electrode was swept from -5 V to 5 V with 0.02 V intervals.

Fig. 5-12 show current-voltage characteristics of TFT array with the gold solution. There is a large change of current at TFT 'ON' with applied voltage around -5 V, which is attributed to the voltage drop between the common electrode applied negative voltage and the drain charged positively when the TFT is turned on. On the other hand, there is not much current change in TFT 'OFF' due to the cut-off current in TFT channel when the TFT was turned off. The increasing current both TFT 'ON' and 'OFF' with increasing applied voltage might result from leakage current due to TFT leakage and pinholes in the passivation layer.

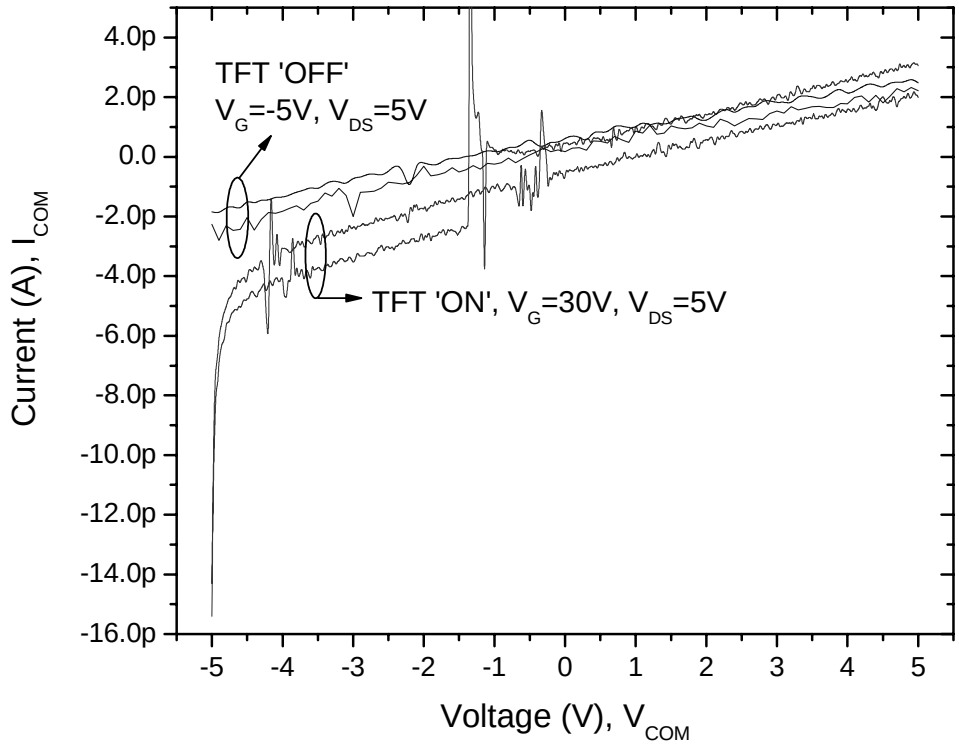


FIG. 5-12. Current-voltage characteristics of TFT array with gold solution.

Chapter 6 Conclusions

For un-biased rf magnetron sputtered MoW films the electrical resistivity as a function of tungsten fraction follows a typical Nordheim relationship. The resistivity increases with the addition of solute atoms (tungsten) and is maximum at ~ 0.5 atomic fraction of solute atoms. Films sputtered at room temperature without substrate bias contained a second metastable phase (β-W) and results in a significantly higher resistivity due to the lattice mismatch between stable α-W and metastable β-W. As sputtering temperature increases, the β-W does not form and the resistivity decreases over the entire composition range relative to the room temperature deposited sample. Thin films deposited with substrate bias had a considerably lower resistivity over the entire composition range and the resistivity as a function of composition obeys a rule of mixture rule. Additionally, in the MoW film deposited with biased sputtering, the β-W phase is not present even at room temperature. From the SEM results, a denser and void-free structure is observed in the microstructure of biased thin films. Additionally, unlike bulk molybdenum and tungsten biased tungsten films had a higher resistivity versus biased molybdenum. This phenomenon is consistent with the fact that the dislocation resistivity of tungsten is two orders of magnitude higher than that of molybdenum.

To overcome deficiencies of sputtered silicon oxide (SiO_x) films the rf magnetron sputtering process was optimized by using a full factorial design of experiment (DOE). The optimized SiO_x film has a 5.7 MV/cm breakdown field and a 6.2 nm/min deposition rate at 10 W/cm^2 RF power, 3 mTorr pressure, 300^{o}C substrate temperature, and 56 V

substrate bias. We also fabricated and characterized metal-insulator-semiconductor (MIS) switching devices to show potential and prospective applications of the optimized SiO_x films.

The breakdown field of sputter-deposited SiN_x films is considerably enhanced by applying a substrate bias during the sputtering deposition. The maximum breakdown field is 7.65 MV/cm with 20 W (125 V) substrate bias and the breakdown voltage slightly decreases at higher substrate bias up to ~ 40 W (155 V) due to increasing the number of defects caused by severe ion bombardment at higher biases during SiN_x deposition.

The effects that substrate bias has on a-Si sputtered films were also surveyed. Biased a-Si films exhibit lower leakage current and a lower deposition rate because they are denser films with fewer defects as a result of the energetic ion bombardment that occurs during bias sputtering. Additionally, we fabricated a fully sputter-deposited TFT with biased a-Si that exhibit very low leakage and superior transconductance values relative to films deposited with no bias. Similar to the results of a-Si, the conductivity of n^+ a-Si is enhanced by applying substrate bias and is attributed to densification and fewer induced defects in the films by the biased sputter deposition.

The crystallization speed and temperature can be enhanced and lowered, respectively, by annealing substrates biased during a-Si deposition even if it is highly stressed compressively. This suggests that the enhanced number of nucleation sites induced by ion bombardment is a more dominant factor than the induced stress in low temperature crystallization of a-Si.

The fully sputter-deposited TFTs fabricated with substrate biased SiN_x, a-Si, and n^+ a-Si films has reasonably good electrical properties up to 0.48 cm^2/Vs field effect mobility, 10^7 on/off current ratio, and below 1.2 V threshold voltage. The TFT properties were degraded with an increase in the back channel etch depth and this is attributed to interfacial defects that are generated during the back channel etch process. Finally, a lower threshold voltage, higher on-current, and higher on/off current ratio, are demonstrated with a thin gate SiN_x TFT (150 nm) versus a TFT with thicker gate SiN_x (300 nm).

A 20×20 active matrix thin film transistor array with integrated vertically aligned carbon nanofibers grown by Ni catalyst in DC-PECVD has been fabricated and characterized. This device provides great potential to perform direct cell sensing, probing, and recording with a high electrode density and active addressability. Consequently, actively addressed nanofiber arrays enable bidirectional interfacing with tissue matrices in a format that provides intercellular positioning of electrode elements as well as the potential for intracellular residence of probes within individual cells. In a near future study, we will be investigating the electrochemical characteristics of the TFT array in various biological electrolyte solutions to evaluate how the electrical properties of the array change with voltage and frequency. Finally, the fabrication and characterization of TFT-CNF devices for recording and stimulating live bio-cells with active addressability will be exploited.

References

[1] A. Mohr, W. Finger, K. J. Fohr et al., "Performance of a thin film microelectrode array for monitoring electrogenic cells in vitro," Sensors and Actuators B (Chemical) **B34** (1-3), 265 (1996).

[2] V. Bucher, M. Graf, M. Steizle et al., "Low-impedance thin-film polycrystalline silicon microelectrodes for extracellular stimulation and recording," Biosensors & Bioelectronics **14** (7), 639 (1999).

[3] Pierre Thiebaud, Cynthia Beuret, Milena Koudelka-Hep et al., "Array of Pt-tip microelectrodes for extracellular monitoring of activity of brain slices," Biosensors & Bioelectronics **14** (1), 61 (1999).

[4] E. Claverol-Tinture and J. Pine, "Extracellular potentials in low-density dissociated neuronal cultures," Journal of Neuroscience Methods **117** (1), 13 (2002).

[5] Conrad D. James, Andrew J. H. Spence, Natalie M. Dowell-Mesfin et al., "Extracellular recordings from patterned neuronal networks using planar microelectrode arrays," IEEE Transactions on Biomedical Engineering **51** (9), 1640 (2004).

[6] V. Bucher, B. Brunner, C. Leibrock et al., "Electrical properties of a light-addressable microelectrode chip with high electrode density for extracellular stimulation and recording of excitable cells," Biosensors & Bioelectronics **16** (3), 205 (2001).

[7] V. Bucher, J. Brugger, D. Kern et al., "Electrical properties of light-addressed sub- mu m electrodes fabricated by use of nanostencil-technology," Microelectronic Engineering **61-62**, 971 (2002).

[8] P. K. Weimer, "The TFT - a new thin-film transistor," Proc. IRE **50**, 1462 (1962).

[9] P. G. LeComber, W. E. Spear, and A Gaith, "Amorphous-silicon field-effect device and possible application," Electronics Letters **15**, 179 (1979).

[10] K. D. Mackenzie, A. J. Snell, I. French et al., "The characteristics and properties of optimised amorphous silicon field effect transistors," Applied Physics A (Solids and Surfaces) **A31** (2), 87 (1983).

[11] A. J. Snell, K. D. Mackenzie, W. E. Spear et al., "Application of amorphous silicon field effect transistors in addressable liquid crystal display panels," Applied Physics **24** (4), 357 (1981).

[12] M. Katayama, "TFT-LCD technology," Thin Solid Films **341** (1-2), 140 (1999).

[13] F. Morin, "Amorphous silicon TFTs and their applications," Microelectronic Engineering **19** (1-4), 171 (1992).

[14] Shunsuke Tomiyama, Takashi Ozawa, Hisao Ito et al., "Amorphous silicon thin film transistors and application to image sensors," Journal of Non-Crystalline Solids **198-200** (pt 2), 1087 (1996).

[15] P. Estrela, A. G. Stewart, F. Yan et al., "Field effect detection of biomolecular interactions," Electrochimica Acta **50** (25-26), 4995 (2005).

[16] L. Mariucci, G. Fortunato, A. Pecora et al., "Hydrogenated amorphous silicon technology for chemically sensitive thin-film transistors," Sensors and Actuators, B: Chemical **B6** (1-3), 29 (1992).

[17] A. M. Brockhoff, W. M. Arnoldbik, and F. H. P. M. Habraken, "Study of the permeability of thin films of a-Si:H using MeV ion beams," Nuclear Instruments and Methods in Physics Research, Section B: Beam Interactions with Materials and Atoms **190** (1-4), 226 (2002).

[18] Jean-Pierre Moy, "Recent developments in X-ray imaging detectors," Nuclear Instruments and Methods in Physics Research, Section A: Accelerators, Spectrometers, Detectors and Associated Equipment **442** (1-3), 26 (2000).

[19] Jean-Pierre Moy, "Large area X-ray detectors based on amorphous silicon technology," Thin Solid Films **337** (1-2), 213 (1999).

[20] H. Mahfoz-Kotb, A. C. Salaun, T. Mohammed-Brahim et al., Strasbourg, France, 2003 (unpublished).

[21] R. A. Street and M. J. Thompson, "Electronic states at the hydrogenated amorphous silicon/silicon nitride interface," Applied Physics Letters **45** (7), 769 (1984).

[22] Y. Kuo, "Plasma etching and deposition for a-Si:H thin film transistors," Journal of the Electrochemical Society **142** (7), 2486 (1995).

[23] Young Hee Byun, Michael Shur, Michael Hack et al., "New analytical polycrystalline-silicon thin-film transistor model for computer aided design and parameter extraction," Solid-State Electronics **35** (5), 655 (1992).

[24] Byun Young Hee, M. Shur, M. Hack et al., "New analytical polycrystalline-silicon thin-film transistor model for computer aided design and parameter extraction," Solid-State Electronics **35** (5), 655 (1992).

[25] M. Endo, Y. A. Kim, T. Hayashi et al., "Structural characterization of cup-stacked-type nanofibers with an entirely hollow core," Applied Physics Letters **80** (7), 1267 (2002).

[26] A. Krishnan, E. Dujardin, M. M. J. Treacy et al., "Graphitic cones and the nucleation of curved carbon surfaces," Nature **388** (6641), 451 (1997).

[27] H. W. Kroto, J. R. Heath, S. C. O'Brien et al., "C/sub 60/: Buckminsterfullerene," Nature **318** (6042), 162 (1985).

[28] S. Iijima, "Helical microtubules of graphitic carbon," Nature **354** (6348), 56 (1991).

[29] W. Kratschmer, L. D. Lamb, K. Fostiropoulos et al., "Solid C/sub 60/: a new form of carbon," Nature **347** (6291), 354 (1990).

[30] A. V. Melechko, V. I. Merkulov, T. E. McKnight et al., "Vertically aligned carbon nanofibers and related structures: controlled synthesis and directed assembly," Journal of Applied Physics **97** (4), 41301 (2005).

[31] M. J. Bronikowski, P. A. Willis, D. T. Colbert et al., "Gas-phase production of carbon single-walled nanotubes from carbon monoxide via the HiPco process: A parametric study," Journal of Vacuum Science & Technology A (Vacuum, Surfaces, and Films) **19** (4, pt.1-2), 1800 (2001).

[32] A. M. Cassell, J. A. Raymakers, Kong Jing et al., "Large scale CVD synthesis of single-walled carbon nanotubes," Journal of Physical Chemistry B **103** (31), 6484 (1999).

[33] W. Z. Li, S. S. Xie, L. X. Qian et al., "Large-scale synthesis of aligned carbon nanotubes," Science **274** (5293), 1701 (1996).

[34] R. T. K. Baker, M. A. Barber, R. J. Waite et al., "Nucleation and growth of carbon deposits from the nickel catalyzed decomposition of acetylene," Journal of Catalysis **26** (1), 51-62 (1972).

[35] A. Kock, P. K. De Bokx, E. Boellaard et al., Journal of Catalysis **96**, 468 (1985).

[36] A. V. Melechko, V. I. Merkulov, D. H. Lowndes et al., "Transition between 'base' and 'tip' carbon nanofiber growth modes," Chemical Physics Letters **356** (5-6), 527 (2002).

[37] B. O. Boskovic, V. Stolojan, R. U. A. Khan et al., "Large-area synthesis of carbon nanofibres at room temperature," Nature Materials **1** (3), 165 (2002).

[38] V. I. Merkulov, D. H. Lowndes, Y. Y. Wei et al., "Patterned growth of individual and multiple vertically aligned carbon nanofibers," Applied Physics Letters **76** (24), 3555 (2000).

[39] S. B. Lee, K. B. K. Teo, M. Chhowalla et al., "Study of multi-walled carbon nanotube structures fabricated by PMMA suspended dispersion," Microelectronic Engineering **61-62**, 475 (2002).

[40] T. E. McKnight, A. V. Melechko, D. W. Austin et al., "Microarrays of vertically aligned carbon nanofiber electrodes in an open fluidic channel," Journal of Physical Chemistry B **108**, 7115-7125 (2004).

[41] T. E. McKnight, A. V. Melechko, G. Griffin et al., "Intracellular integration of synthetic nanostructures with viable cells for controlled biochemical manipulation," Nanotechnology **14** (5), 551 (2003).

[42] H. Choe and Kim Sang-Gab, "Effects of the n/sup +/ etching process in TFT-LCD fabrication for Mo/Al/Mo data lines," Semiconductor Science and Technology **19** (7), 839 (2004).

[43] M. Ikeda, T. Oka, M. Atsuta et al., Hamamatsu, Japan, 1995 (unpublished).

[44] K. Okajima, T. Sato, T. Dohi et al., "Two-step-etching process of MoW gate metal on large TFT glass substrates," Vacuum **51** (4), 765 (1998).

[45] P. Petroff, T. T. Sheng, A. K. Sinha et al., "Microstructure, growth, resistivity, and stresses in thin tungsten films deposited by r.f. sputtering," Journal of Applied Physics **44** (6), 2545 (1973).

[46] H. P. Shukovsky, R. M. Rose, and J. Wulff, "The 1ow temperature electrical resistivity of lattice defects in deformed tungsten single crystal," Acta Metallurgica **14** (7), 830 (1966).

[47] R. C. Sun, T. C. Tisone, and P. D. Cruzan, "Internal stresses and resistivity of low-voltage sputtered tungsten films [microelectronic cct. conductor]," Journal of Applied Physics **44** (3), 1009 (1973).

[48] L. D. Whitmire and F. R. Brotzen, "The effects of deformation on the electrical resistivity of molybdenum single crystals," Transactions of the Metallurgical Society of AIME **239** (6), 827 (1967).

[49] C. S. McCormick, C. E. Weber, J. R. Abelson et al., "Low temperature fabrication of amorphous silicon thin film transistors by dc reactive magnetron sputtering," Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films **15** (5), 2770 (1997).

[50] S. Suyama, A. Okamoto, and T. Serikawa, "Electrical conduction mechanism and breakdown property in sputter-deposited silicon dioxide films on polycrystalline silicon," Journal of Applied Physics **65** (1), 210 (1989).

[51] T. Serikawa and S. Shirai, "Ultra-thin silicon-oxide films by sputter-deposition and their application to high-quality poly-Si TFTs," Vacuum **51** (4), 781 (1998).

[52] Seung-Ik Jun, P. D. Rack, T. E. McKnight et al., "Electrical and microstructural characterization of molybdenum tungsten electrodes using a combinatorial thin film sputtering technique," Journal of Applied Physics **97** (5), 54906 (2005).

[53] P. Carlsson, C. Nender, H. Barankova et al., "Reactive sputtering using two reactive gases, experiments and computer modeling," Journal of Vacuum Science & Technology A (Vacuum, Surfaces, and Films) **11** (4, pt.1), 1534 (1993).

[54] H. Aguas, E. Fortunato, V. Silva et al., "High quality a-Si:H films for MIS device applications," Thin Solid Films **403-404**, 26 (2002).

[55] J. W. Medlin, A. H. McDaniel, M. D. Allendorf et al., "Effects of competitive carbon monoxide adsorption on the hydrogen response of metal-insulator-

semiconductor sensors: the role of metal film morphology," Journal of Applied Physics **93** (4), 2267 (2003).

[56] S. D. Theiss, C. C. Wu, M. Lu et al., San Francisco, CA, USA, 1997 (unpublished).

[57] Y. H. Liang, N. Maley, and J. R. Abelson, "The improved stability of hydrogenated amorphous silicon films grown by reactive magnetron sputtering at high substrate temperature," Journal of Applied Physics **75** (7), 3704 (1994).

[58] Christine Algate, "PECVD and PVD Systems for TFT-LCD Manufacturing," FPD Update, Semiconductor Equipment and Materials International **2** (4), 9 (2002).

[59] E. Bustarret, M. Bensouda, M. C. Habrard et al., "Configurational statistics in a-Si/sub x/N/sub y/H/sub z/ alloys: a quantitative bonding analysis," Physical Review B (Condensed Matter) **38** (12), 8171 (1988).

[60] T. Makino, "Composition and structure control by source gas ratio in LPCVD SiN," Journal of the Electrochemical Society **130** (2), 450 (1983).

[61] Bae Sanghoon, A. K. Kalkan, Cheng Shangcong et al., "Characteristics of amorphous and polycrystalline silicon films deposited at 120 degrees C by electron cyclotron resonance plasma-enhanced chemical vapor deposition," Journal of Vacuum Science & Technology A (Vacuum, Surfaces, and Films) **16** (3), 1912 (1998).

[62] Y. Mishima, M. Takei, T. Uematsu et al., "Polycrystalline silicon formed by ultrahigh-vacuum sputtering system," Journal of Applied Physics **78** (1), 217 (1995).

[63] T. Voutsas, H. Nishiki, M. Atkinson et al., "Sputtering technology of Si films for low-temperature poly-Si TFTs," Sharp Technical Journal (80), 36 (2001).

[64] S. I. Jun, T. E. McKnight, A. V. Melechko et al., "Characterisation of reactively sputtered silicon oxide for thin-film transistor fabrication," Electronics Letters **41** (14), 822 (2005).

[65] Seung-Ik Jun, Philip D. Rack, Timothy E. McKnight et al., "Electrical characterization of amorphous silicon thin film transistors fabricated by rf magnetron sputtering with substrate bias," Journal of Applied Physics (2006).

[66] A. Straub, P. I. Widenborg, A. Sproul et al., "Fast and non-destructive assessment of epitaxial quality of polycrystalline silicon films on glass by optical measurements," Journal of Crystal Growth **265** (1-2), 168 (2004).

[67] S. Strehlke, S. Bastide, and C. Levy-Clement, "Optimization of porous silicon reflectance for silicon photovoltaic cells," Solar Energy Materials and Solar Cells **58** (4), 399 (1999).

[68] Kuo Yue, "PECVD silicon nitride as a gate dielectric for amorphous silicon thin film transistor. Process and device performance," Journal of the Electrochemical Society **142** (1), 186 (1995).

[69] G. Farhi, M. Aoucher, and T. Mohammed-Brahim, "Study of the solid phase crystallization behavior of amorphous sputtered silicon by X-ray diffraction and

electrical measurements," Solar Energy Materials and Solar Cells **72** (1-4), 551 (2002).

[70] Y. Z. Wang and O. O. Awadelkarim, "Metal-induced solid-phase crystallization of hydrogenated amorphous silicon: dependence on metal type and annealing temperature," Applied Physics A (Materials Science Processing) **70** (5), 587 (2000).

[71] A. R. Joshi, T. Krishnamohan, and K. C. Saraswat, "A model for crystal growth during metal induced lateral crystallization of amorphous silicon," Journal of Applied Physics **93** (1), 175 (2003).

[72] Seung-Ik Jun, Yong-Ho Yang, Jae-Bok Lee et al., "Electrical characteristics of thin-film transistors using field-aided lateral crystallization," Applied Physics Letters **75** (15), 2235 (1999).

[73] M. Miyasaka and J. Stoemenos, "Excimer laser annealing of amorphous and solid-phase-crystallized silicon films," Journal of Applied Physics **86** (10), 5556 (1999).

[74] T. Mizuki, J. S. Matsuda, Y. Nakamura et al., "Large domains of continuous grain silicon on glass substrate for high-performance TFTs," IEEE Transactions on Electron Devices **51** (2), 204 (2004).

[75] Y. Kimura, M. Kishi, and T. Katoda, "Effects of elastic stress introduced by a silicon nitride cap on solid-phase crystallization of amorphous silicon," Journal of Applied Physics **86** (4), 2278 (1999).

[76] P. Hashemi, J. Derakhshandeh, S. Mohajerzadeh et al., "Stress-assisted nickel-induced crystallization of silicon on glass," Journal of Vacuum Science & Technology A (Vacuum, Surfaces, and Films) **22** (3), 966 (2004).

[77] Seung-Ik Jun, Philip D. Rack, Timothy E. McKnight et al., "Direct-current substrate bias effects on amorphous silicon sputter-deposited films for thin film transistor fabrication," Applied Physics Letters **87** (13), 132108 (2005).

[78] Manuel Cardona and Fred H. Pollak, "Energy-Band Structure of Germanium and Silicon: The k·p Method," Physical Review **142**, 530 (1966).

[79] R. Tsu, J. Gonzalez-Hernandez, S. S. Chao et al., "Critical volume fraction of crystallinity for conductivity percolation in phosphorus-doped Si:F:H alloys," Applied Physics Letters **40** (6), 534 (1982).

[80] C. Spinella, S. Lombardo, and F. Priolo, "Crystal grain nucleation in amorphous silicon," Journal of Applied Physics **84** (10), 5383 (1998).

[81] W. A. Brantley, "Calculated elastic constants for stress problems associated with semiconductor devices," Journal of Applied Physics **44** (1), 534 (1973).

[82] H. M. Choi, S. K. Choi, O. Anderson et al., "Influence of film density on residual stress and resistivity for Cu thin films deposited by bias sputtering," Thin Solid Films **358** (1-2), 202 (2000).

[83] P. J. Jennings, J. C. L. Cornish, B. W. Clare et al., "Study of the effects of annealing and outgassing on hydrogenated amorphous silicon," Thin Solid Films **310** (1-2), 156 (1997).

[84] Kyung Hoon Jun, Koeng Su Lim, Sang Youl Kim et al., "Optical evidence of amorphous-network change in the initial-growth stage a-Si:H," Journal of Non-Crystalline Solids **275** (1), 59 (2000).

[85] G. E. Possin, Anaheim, CA, USA, 1991 (unpublished).

[86] M. J. Powell, J. A. Chapman, A. G. Knapp et al., "A 6-in. full-color liquid-crystal television using an active matrix of amorphous-silicon TFTs," Proceedings of the S.I.D **29** (3), 227 (1988).

[87] K. Takechi, A. N. Hirano, H. Hayama et al., "Back-channel-oxidized a-Si:H thin-film transistors," Journal of Applied Physics **84** (7), 3993 (1998).

[88] J. H. Chen, Z. P. Huang, D. Z. Wang et al., "Electrochemical synthesis of polypyrrole films over each of well-aligned carbon nanotubes," Synthetic Metals **125** (3), 289 (2001).

[89] Jee Yeon Lim, Woon-kie Paik, and In-Hyeong Yeo, "A study of ion transports and growth of conducting polypyrrole with electrochemical quartz crystal microbalance," Synthetic Metals **69** (1-3), 451 (1995).

Appendix Run sheet for TFT-VACNF processing

Run ID		Name	
Date of run start		Date of run end	
Purpose			

Date	Layer	Process	Equipment	Conditions/Spec.	Remark/Results
/	Thermal oxide	HMDS priming	YES oven #1	Recipe #2, 2 min (Total ~ 25 min)	
/	Align key	PR coating / Baking	Spinner	PR: 955CM-2.1 Coating: 3000rpm/60sec SB: 90°C/90sec	~ 1.5um
/		Exposure / Developing (1. Align)	Stepper	Recipe: INTRA\MARST EXP: 0.40sec PEB: 120°C/90s DEV: CD26/70s	
/		Descum	RIE #1	Recipe: DESCUM Time: 30sec	
/		Etching (Buffer SiO_2)	RIE #1	Recipe: OXIDE1 RF power: 200W Gas: CHF_3/O_2 (75/7) Press: 200mT Proc. time: 500sec	
/		PR wet strip	Strip bath	Temp.: 70C Time: 20min	
/		PR dry strip	RIE #1	Recipe: POLY-ICP ICP power: 300W RF power: 50W Gas: O_2 (50) Press: 350mT Proc. time: 180sec	

/	Gate	Deposition (Cr, 250nm)	Sputter	RF: 200W Pressure: 3mT Gas: 25sccm Ar-H_2 Temp: 200°C Proc. time: 50min	Gun #4 (or #1)
/		Rs measurement	Rs meter	Rs 0.97±0.2 ohm/sq.	
/		PR coating / Baking	Spinner	PR: 955CM-2.1 Coating: 3000rpm/60sec Soft baking: 90C/90sec	~ 1.5um
/		Exposure / Developing (2. Gate)	Stepper	Recipe: INTRA\LEADST EXP: 0.38sec PEB: 120C/90s DEV: CD26/70s	
/		Etching (Cr)	Wet etch	Cr etchant Temp: 40C Time: 2min30sec	
/		PR wet strip	Strip bath	Temp.: 70C Time: 20min	
/	Active	Deposition (SiN_x, 300nm)	Sputter	RF power: 200W Gas: Ar-H_2/N_2(25/50) Pressure: 5mT Temp.: 200°C DC bias: 30W Proc. time: 187min	Si target (Gun #2)
		(a-Si, 200nm)	Sputter	RF power: 200W Gas: Ar-H_2(25) Pressure: 5mT Temp.: 200°C DC bias: 30W Proc. time: 59min	Si target (Gun #2)

		(n+ a-Si, 50nm)	Sputter	RF power: 200W Gas: Ar-H_2(25) Pressure: 5mT Temp.: 200°C DC bias: 30W Proc. time: 15min	n^+ Si target (Gun #3) Resistivity = 3.9 Ωcm
/	HMDS	HMDS priming	YES oven #1	Recipe #2, 2min (Total ~25min)	Optional process
		PR coating / Soft baking	Spinner	PR: 955CM-2.1 Coating: 3000rpm/60sec Soft baking: 90C/90sec	
/		Exposure / Developing (3. Active ReV_2)	Stepper	Recipe: INTRA\LEADST EXP: 0.40sec PEB: 120°C/90s DEV: CD26/70s	
/		Dry etching (n+ a-Si/a-Si)	RIE #1	RF power: 100W SF_6/O_2 (40/2) Pressure: 100mT Proc. time: 45s	EPD+15 OE%
/		PR wet strip	Strip bath	Temp.: 70C Time: 20min	
/		PR dry strip	RIE	Recipe: POLY-ICP Proc.: 180sec	
/		BOE clean	Wet bath	20(H_2O) : 1(10:1 HF) 15sec dip	
/	S/D	Deposition (Cr, 250nm)	Sputter	RF: 200W Pressure: 3mT Gas: 25sccm Ar-H_2 Temp: 200°C Proc. time: 50min	Gun #4 (or #1)

/		Rs measurement	Rs meter	Rs 0.97±0.2 ohm/sq.	
	CNF	PR coating / Soft baking	Spinner	PR: 955CM-0.7 Coating: 3000rpm/60sec Soft baking: 90C/90sec	
/		Exposure / Developing (4. CNF)	Stepper (ORNL)	Recipe: INTRA\LEADST EXP: 1.5sec PEB: 120C/90sec DEV: CD26/70s	
/		Deposition (Ni, 10A)	E-beam evaporator (ORNL)	RF power: W Pressure: 5mT Gas flow rate: 25sccm Ar Temp: RT Process time: min	
/		Lift-off	Wet bath (ORNL)	Solution: Aceton Lift-off time: ~1h	
/		CNF growth	DC-PECVD (ORNL)	Temp: 600°C Gas: C_2H_2(35) Press: 3000mTorr Amp: 400mA Proc. Time: 1h	
/	S/D, N+ (BCE)	PR coating / Baking	Spinner	PR: 955CM-2.1 Coating: 3000rpm/60sec Soft baking: 90C/90sec	~ 1.5um

/		Exposure / Developing (5. S/D)	Stepper	Recipe: INTRA\LEADST EXP: 0.38sec PEB: 120C/90s DEV: CD26/70s	
/		Etching (Cr)	Wet etch	Cr etchant Temp: 40C Time: 2min30sec	
/		Back channel etching (n+ a-Si/a-Si)	RIE #1	RF power: 40W $SF_6/O_2/CF_4$ (20/3/20) Pressure: 100mT Total process time: 20s	Etched depth: ~110nm
		PR wet strip	Strip bath	Temp.: 70C Time: 20min	
/		PR dry strip	RIE	Recipe: POLY-ICP Process time: 180sec	
/	Via hole (1)	Deposition (1^{st} SiN_x, 25nm)	Sputter	RF power: 50W Gas: Ar-H_2/N_2(25/50) Pressure: 5mT Temp.: 200°C DC bias: 30W Proc. time: 35min	Si target (Gun #2)
		Deposition (2^{nd} SiN_x, 200nm)	Sputter	RF power: 200W Gas: Ar-H_2/N_2(25/50) Pressure: 5mT Temp.: 200°C DC bias: 30W Proc. time: 120min	Si target (Gun #2)
/		HMDS priming	YES oven #1	Recipe #2, 2min (Total ~25min)	

/		PR coating / Soft baking	Spinner	PR: 955CM-2.1 Coating: 3000rpm/50sec Soft baking: 90C/90sec	PR coating / Soft baking
/		Exposure / Developing (6. VIA1)	Stepper	Recipe: INTRA\LEADST EXP: 0.42sec PEB: 120C/90s DEV: CD26/70s	
/		Descum	RIE #1	Recipe: DESCUM Time: 30sec	
/		Dry etching (g-SiN_x, PVX SiN_x)	RIE #1	RF power: 100W SF_6/O_2 (40/4) Pressure: 100mT Proc. time: 360s	EPD+50 OE%
		PR dry ashing	RIE #1	Recipe: poly Gas: O_2(50) Proc. time: 85sec	
		BOE wet etch	Wet bath	10:1 BOE Temp: RT Proc. Time: 25sec	
		PR wet strip	Strip bath	Temp.: 70C Time: 20min	
/		PR dry strip	RIE	Recipe: POLY-ICP Process time: 180sec	
/	Via hole (2)	SU-8 coating / Soft baking	Spinner (for SU-8 and PMMA)	PR: SU-8 2010 Coating: 2000rpm/50sec Soft baking: 1st 65C/60s 2nd 95C/120s	~ 9 um

/		Exposure / Developing (7. VIA2)	Mask aligner	EXP: 25sec PEB: 1st 65C/60s 2nd 95C/75s DEV: SU-8 developer/70sec IPA rinse DI rinse	
	TFT measurement	I-V, capacitance	Probe station (ORNL)	Mobility: I_{on} (+10V): I_{off} (-8V): V_{th}: Subthreshold swing:	
	Inspection		Microscopy	Pass / Fail	
	Dicing		Disco Dad/2H6T Dicing Saw	5×5mm	
/	Device integration	Wire bonding	K&S Wire Bonders		
/	Chip Housing				

Vita

Seung-Ik Jun received the B.S. degree in Materials Science and Engineering from Hongik University in 1997 and the M.S. degree in Inorganic Materials Science Engineering from Hanyang University in 1999, Korea. His undergraduate work focused on thermodynamic calculation and modeling of ceramic and metallic binary system, while his graduate study of M.S. focused on the fabrication and characterization of polycrystalline silicon (poly-Si) thin film transistor (TFT) using field aided lateral crystallization (FALC). Following the completion of his Master of Science, he joined flat panel display R&D center, Hynix semiconductor, Inc., Korea as an associate process development engineer, where he worked on the process development of a-Si and poly-Si TFTs. In 2003, he jointed Dr. Rack's group of the University of Tennessee in pursuit of a Ph.D. in Materials Science & Engineering and Molecular-Scale Engineering and Nanoscale Technologies (MENT) Research Group of Oak Ridge National Laboratory (supervisor: Dr. Michael Simpson) as a graduate assistant. He has authored and coauthored more than 25 publications in referred journals and conference proceedings. He is a first inventor on over 20 registered patents in Korea and/or international patents. He is a member of the Materials Research Society and American Vacuum Society.