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A Low-Power, Highly Stabilized Three-Electrode Potentiostat Using Subthreshold Techniques

Melika Roknsharifi
mroknsha@utk.edu

To the Graduate Council:

I am submitting herewith a dissertation written by Melika Roknsharifi entitled "A Low-Power, Highly Stabilized Three-Electrode Potentiostat Using Subthreshold Techniques." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

Syed Kamrul Islam, Major Professor

We have read this dissertation and recommend its acceptance:

Benjamin J. Blalock, Jeremy Holleman, Mohamed Mahfouz

Accepted for the Council:
Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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A Low-Power, Highly Stabilized Three-Electrode Potentiostat Using Subthreshold Techniques

A Dissertation Presented for the
Doctor of Philosophy
Degree
The University of Tennessee, Knoxville

Melika Roknsharifi

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DEDICATION

I lovingly dedicate this thesis to my husband Ahamdreza Ghahremani and my parents Ghodsi Hamidi and Mehdi Roknsharifi, who supported me each step of the way, and also three of my great professors, Dr. Islam, Dr. Abrishamifar and Dr. Sharif bakhtiar.

I would also like to dedicate this work to all diabetic patients and I hope one day the improvement in science can help them enjoy a happy healthy life.

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ABSTRACT

Implantable micro- and nano- sensors and implantable microdevices (IMDs) have demonstrated potential for monitoring various physiological parameters such as glucose, lactate, CO_2, pH, etc. Potentiostats are essential components of electrochemical sensors such as glucose monitoring devices for diabetic patients. Diabetes is a metabolic disorder associated with insufficient production or inefficient utilization of insulin. The most important role of this enzyme is to regulate the metabolic breakdown of glucose generating the necessary energy for human activities. Diabetic patients typically monitor their blood glucose levels by pricking a fingertip with a lancing device and applying the blood to a glucose meter. This painful process may need to be repeated once before each meal and once 1- 4 hour after meal. Patients may need to inject insulin manually to keep the blood glucose level at 3.9-6.7 mmol [mili mol] /liter.

Frequent glucose measurement can help reduce the long term complication of this disease which includes kidney disease, nerve damage, heart and blood vessel diseases, gum disease, glaucoma and etc. Having an implanted close loop insulin delivery system can help increase the frequency of glucose measurement and the accuracy of insulin injection. The implanted close loop system consists of three main blocks: (1) an electrochemical sensor in conjunction with a potentiostat to measure the blood glucose level, (2) a control block that defines the level of insulin injection and (3) an implanted insulin pump.

To provide a continuous health-care monitoring the implantable unit has to be powered up using wireless techniques. Minimizing the power consumption associated with the implantable system can improve the battery life times or minimize the power transfer through the human body. The focus of this work is on the design of low-power potentiostats for the implantable glucose monitoring system.

This work addresses the conventional structures in potentiostat design and the problems associated with these designs. Based on this discussion a modification is made to improve the stability without

increasing the complexity of the system. The proposed design adopts a subthreshold biasing scheme for the design of a highly-stabilized, low-power potentiostats.

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CHAPTER 1 – Introduction

Diabetes is one of the body metabolic disorders that have affected millions of peoples in the United States and over 100 million people around the world. It is one of the leading causes of death in the United States responsible for more than hundred thousand deaths each year. According to American Diabetes Association (ADA) the cost associated with complications of the diabetes is more than 40 billion dollar [1]. These complications are mostly due to the poor glucose monitoring which result in inaccurate diagnosis of the condition of the patients. Therefore there are a number of research groups working on improving the quality of the glucose measurement and monitoring schemes as well as the quality of the life of the diabetic patients. This chapter provides a brief introduction to this disease and introduces potentiostat design in conjunction with a chemical sensor that can work in a close loop with implantable insulin pump as a solution for this dilemma.

1.1. Metabolism

Metabolism is the never-ending streams of chemical reactions that occur in the cells to sustain energy for living, grow, reproduce and maintain the cell structures from the food intake. Metabolism includes two different sets of reactions: catabolism and anabolism. Breaking down the organic molecules such as amino acids, sugars, nucleotides and lipids into energy is called catabolism and using this energy to construct the cells components such as nucleic acids and proteins is called anabolism.

These chemical reactions can normally occur only at very high temperatures that cannot exist inside the cell. Therefore for these reactions to happen, a catalyzer is required. Each reaction takes place using a different type of protein as catalyzer known as enzyme. Enzymes are crucial for metabolism pathway since they help these reactions proceed quickly and efficiently. Several enzymes may be used in one

metabolic pathway as illustrated in Fig. 1.1. For example, glucose metabolism is controlled by an enzyme called insulin. This enzyme is produced in response to the increase in the blood glucose levels. Then using a cascade of kinases enzyme, the cells can convert glucose into storage molecules such as glycogen and fatty acids.

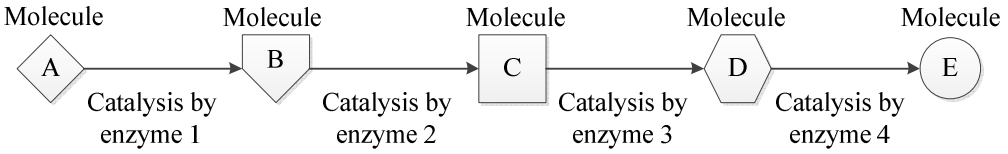


Fig. 1. 1. An example of metabolic pathway showing a set of enzymes acting in series to convert molecule A to molecule E. Each enzyme catalyzes a particular chemical reaction while the enzyme is left unchanged [2].

1.1.1. Regulation and Control

To maintain a constant condition inside the cells, while the environment of most of the organisms is constantly changing, the reactions of metabolism must be perfectly regulated. Metabolic pathways are controlled by two concepts: regulation and control. Regulation is the increase or decrease in enzyme activity in response to a signal (large changes mean high regulation) while 'control' refers to the effect of these changes in the overall rate of the pathway.

1.1.2. Metabolic Disorder

Metabolic disorders result in a large number of genetic diseases. Majority of these diseases are due to the defects of a single gene that represents the code for enzymes that is working as catalyzer in many metabolic reactions. The problem in most of these disorders is the accumulation of matters which are toxic or the reduced ability of synthesizing essential compounds. The metabolic disorders that are based on inborn genetic defect are known as congenital metabolic diseases or inherited metabolic diseases. In the past the inherited metabolic diseases were considered to only contain the disorders of carbohydrate, amino acid and organic acid metabolism. Recently many new inborn metabolisms have been discovered.

Diabetes is known to be the most common metabolic disorder that is a result of defect in the enzyme named insulin. In the rest of this chapter this disease will be studied in more details.

1.2. Diabetes

Diabetes is a metabolic disorder due to the defect in producing insulin, the digestive enzyme. The organ that is responsible for producing this enzyme is pancreas which is a small organ located below the stomach. This organ secretes insulin from 2% of its mass that is called islets and contains pancreatic beta cells. Insulin has many important roles in human body and therefore it is known as the master hormone of the body. The most important role of insulin is the regulation of the metabolic breakdown of glucose and generation of the energy required for all of the human activities. The beta cells help secreting the right amount of insulin by detecting the blood glucose concentration [3].

In diabetes, a misdirected autoimmune reaction can wash off some of the beta cells. This can prevent the pancreas form secretion of the right amount of insulin. Therefore some of the glucose cannot enter the cells resulting in glucose build up in the bloodstream. In severe type of diabetes, this can lead to a cellular starvation while there is extra glucose in the blood. This situation is known as hyperglycemia and can cause a serious health problem. To resolve this situation, the patient needs to manually inject insulin. But if the injected insulin is too much, the rapid fall in glucose concentration can lead to hypoglycemia or low blood glucose. Therefore the patient needs to adjust the insulin level constantly. Diabetes can also be the cause of many other health problems such as kidney failure, loss of vision etc. Presently diabetes is estimated to affect 2-4% of the population [3].

1.2.1. Different Types of Diabetes

There are two major types of diabetes, known as type 1 and type 2. The type 1 diabetes is due to the insufficient production of insulin or production of defective insulin (which is not common). The type 1 diabetes is also known as insulin dependent diabetes mellitus (IDDM) or juvenile onset diabetes mellitus.

Abnormal antibodies have been found in the body of patients with this type of diabetes that can be the cause of pancreas disorder. Type 1 diabetes usually occurs before the age of thirty. However there are some patients who can start to have this type of diabetes at older age.

Type 2 diabetes is due to the inability of cells to use insulin properly and efficiently. This problem mostly affects the muscular cells and fat tissues and is known as insulin resistance diabetes. The type 2 diabetes is also known as non-insulin dependent diabetes mellitus (NIDDM) or adult onset diabetes mellitus (AODM). Although the body still produces insulin, it is relatively inadequate due to insulin resistance or lack of sensitivity of the cells to the insulin. . Type 2 diabetes mostly occurs at the ages of thirty or higher but recently it has been reported to be more common in the children as well.

1.2.2. Home Monitoring of Blood Sugar

Testing the blood sugar at home is very important part of controlling the blood sugar levels in diabetic patients. Blood sugar is usually measured at bedtime, before meal and 1-4 hours after meal depending on the kind of the food served. The idea is to keep the glucose level of the blood near 70-120mg/dl which is a normal range and keep it below 140mg/dl two hours after the meal.

The blood sugar level measurement at home is normally performed by pricking a fingertip with a lancing device and applying the blood to a glucose meter which reads the glucose concentration. There are many different types of meters in the market today each of which has its own advantages and disadvantages. From the result of glucose measurement the patient can adjust his/her medicine, diets and physical activities.

At present, patients need to use “finger-sticking” for collecting a drop of blood many times a day to measure their blood glucose concentration. They need to check the measured glucose and keep it around the desired value by injecting the right amount of insulin. Injection can be performed either by syringes or insulin pen. The advantages of using the pen instead of syringe is that they are more convenient and easier to transport than traditional vial and syringe and are also more accurate and easier to use with less discomfort and pain. The problem with this method is that the level of blood glucose can change in less

than fifteen minutes and it not convenient for the patients to inject insulin more than twice a day, especially for parents who need to inject insulin to an infant.

1.2.3. Importance of Frequent Glucose Monitoring for Diabetes

Frequent glucose measurement in diabetes is very essential to prevent the long term complications that can affect many different parts of the human body. Long-term complications of diabetes are often the result of higher blood sugar level over a long period of time. The other important source of these problems can be found in genes. Some of these long-term problems happen after many years or decades of having diabetes, because these problems usually develop silently and gradually over time. Therefore even if the patients do not have any signs of long term complication there is still chance to develop them eventually.

The organs that can be affected by diabetes in the long time are eyes, kidneys, nerves, heart and blood vessels, gums and feet. A brief description of the problems that can be caused by diabetes in any of these organs is provided below [4]:

Eye Problems: Three different types of eye problem can be developed in patients with diabetes: cataracts, retinopathy and glaucoma.

- *Cataracts:* The thickening and clouding of the lens of the eye is called cataracts. The lens is the part of the eye that helps focusing. This disease can make the patient's vision blurry or make the vision weak at nights. Doctors believe that people with diabetes who have high blood sugar levels over a long period of time are more susceptible to develop cataracts. In advanced level of this problem patients need to go through surgery to improve their vision.
- *Retinopathy:* Retinopathy is the eyes problem that involves changes in the retina. Retina is the layer at the back of the eye that is light-sensitive. The source of these changes can be the damage or the problem growth in the small blood vessels of the retina. This disease normally does not show until several years with diabetes with high blood sugar levels over this long period of time. In advanced level of this problem, laser treatment may be needed to prevent vision loss.

- *Glaucoma:* Another eye problem that patients with diabetes are susceptible to is glaucoma. In glaucoma the pressure inside the eye goes high that results in decreasing blood flow to the retina and the optic nerves which can cause damage. Although it does not change the vision a lot at first but in long time it can cause loss of vision. This problem is more prevalent in older people with long history of diabetes. This case also requires a surgery to solve the problem.

Kidney Disease: The high level of sugar in the blood can cause damage to the blood vessels in the kidneys that can lead to kidney disease. If the patients with diabetes do not control their blood sugar for a long time, they are more likely to get kidney disease that is a serious health problem. The kidney problem can become worse by high blood pressure or using tobacco. If the kidney disease is detected early enough, the damage can sometimes be reversed with proper treatment. But in a very rare case that the kidney problem gets worse the patient may develop kidney failure and require kidney transplant or dialysis. Therefore to protect the kidneys it is important to control the blood sugar.

Nerve Damage: Diabetic neuropathy is the nerve damage that can happen to patients with long history of diabetes. Numbness, tingling, or sharp pains in the feet can be the symptoms of the diabetic neuropathy. The numbness can cause a simple cut to be a serious problem because the patient can not realize the existence of the cut. The nerve damage in any part of the body can cause problem in that organ that may include heart, eyes and urinary system.

Diagnosis of this problem is normally done by a physical exam or a biopsy and patients are advised to see a neurologist. Controlling the blood sugar level can help reduce the patient's risk of developing the nerve damage.

Heart and Blood Vessel Diseases: The patients with diabetes have a high risk of developing cardiovascular diseases that may include heart attack, stroke or blockage of blood vessels in legs and feet. Heart attack and stroke can be the result of a blockage in the blood vessels supplying blood to the heart or the brain. The blood sugar management is very important for controlling the blood vessel problems.

Gum Disease: Too much plaque on the teeth and not enough saliva and having higher level of sugar in the mouth can cause tooth decay. Also loss of collagen and poor blood circulation can cause gum

problems. Bleeding, sensitive and painful gums are the symptoms of the gum disease. Gum disease can also be prevented by managing the blood sugar levels.

Foot Problems: Poor flow of the blood and nerve damage in patients with diabetes can develop foot problems.

1.2.4. Using an Implantable System for More Frequent and More Convenient Glucose Measurement

A miniature implanted glucose sensor in the body can continuously record the blood glucose level and display the value on the external watch-like receiver. This device can be programed to warn the hyperglycemia or hypoglycemia condition while monitoring the blood glucose minute by minute. Eventually this device can be coupled to an implanted insulin pump to automatically deliver the required amount of insulin. The implantable insulin pump has already been developed and by developing the implantable glucose sensor, the close control of blood glucose can be achievable [3]. Fig. 1.2 Shows the idea of the closed loop glucose measurement and insulin delivery for diabetes introduced by El-Khatib et al. in 2010 [5]. The implanted close loop system consists of three main blocks: (1) an electrochemical sensor in conjunction with a potentiostat to measure the blood glucose level, (2) a control block that defines the level of insulin injection and (3) an implanted insulin pump. The focus of this work is on the glucose measurement block shown in Fig. 1.3. As shown in this figure, a glucose measurement block consists five main sub-blocks. 1) DC supply, 2) voltage reference, 3) potentiostat, 4) signal processing unit and 5) telemetry unit. The focus of this work is on analyzing and optimizing the design of the potentiostat and the signal processing unit.

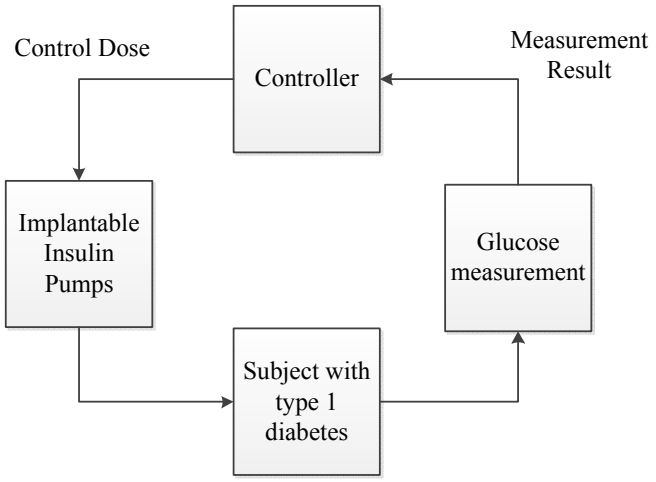


Fig. 1. 2. Close loop insulin delivery system that uses a computer to analyze the measured glucose value and sends a signal to the insulin pump to determine for the right amount of insulin to be delivered to the patient automatically. This process can be repeated every 5 minutes [6].

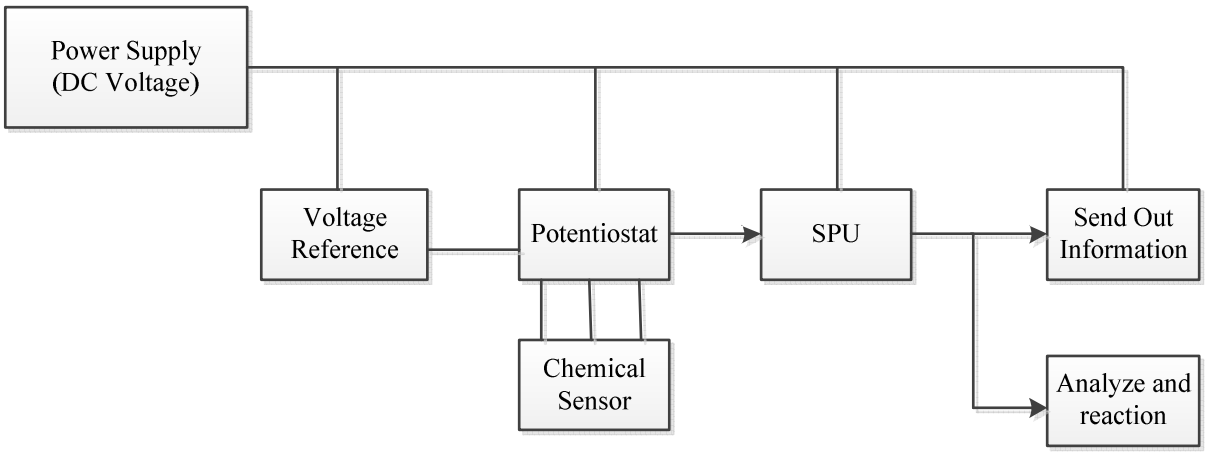


Fig. 1. 3. Schematic block diagram of the glucose measurement block.

1.2.5. Electrochemical Principle in Glucose Sensing

One promising method of glucose sensing involves the use of a family of biological catalyzer known as enzymes or glucose oxidase. Based on the type of the catalyzer the reaction might be different. The output of these reaction can contain H_2O (water) and H_2O_2 (hydrogen-peroxide).

One type of enzyme such as glucose oxidase (GOD), L-glutamate oxidase (GIOD) and cholesterol oxidase (COD) can be reduced by accepting two hydrogen atoms. Then the initial structure can be

restored by oxidizing the reduced enzyme. The reduced enzyme loses hydrogen that will combine with O_2 and with the loss of two electrons a H_2O_2 molecule can be created. Naming this group of enzyme, "flavin adenine dinucleotide (FAD)", the equation for these reactions can be written as below [7]:

$$FAD + substrate \rightarrow FADH_2 + product \quad (1)$$

$$FADH_2 + O_2 \rightarrow H_2O_2 + FAD \quad (2)$$

There is also another type of enzyme that is named "flavin mononucleotide (FMN)" that works the same way as FAD. The final product for both of these types is the reaction below [7]:

$$2H_2O_2 \rightarrow 2H_2O + O_2^+ + 4e^- \quad (3)$$

This reaction can take place by applying a difference potential to the electrochemical cell. In this case the function of the potentiostat is to provide this constant difference potential while collecting the generated electrons through its collecting electrode.

1.2.6. Measuring Other Blood Factors Using Potentiostat

Potentiostats can be used to measure other important blood factors such as oxygen and lactate. Measuring these parameters along with the blood glucose level is of a great importance to the patient with multiple diseases. Measuring of blood oxygen can be applied to any one suffering from unstable oxygenation such as patients with hypoxemia. In hypoxemia patients suffer from the partial drop of pressure in their blood. The high levels of oxygen can damage lungs and central nervous system while low levels of oxygen can cause anemia. In addition, monitoring of lactate is particularly useful for athletes to check if they are over working or not. Potentiostat can help measuring these factors by applying a different difference potential to the electrodes of the electrochemical sensor designed to measure these parameters.

1.3. Challenges in Designing a Potentiostat for an Implantable Glucose Sensor

There are three main challenges in designing a potentiostat working in conjunction with an implantable glucose sensor: (a) the total amount of power consumption, (b) the size of the chip which should be as small as possible to make it convenient for the patient to have it implanted and (c) the generated current should be sensed in a stable structure before it be sent to the telemetry system. In the following sections, the importance of decreasing the total amount of power consumption and increasing the stability of the system is discussed. To show the importance of having a potentiostat with low-power consumption, first a brief discussion over the possible methods for generating power is addressed here. In the next section, different techniques of low-power circuit design are also discussed. These techniques need to be applied to the circuits existing in all of the blocks of an implantable system.

1.3.1. Power Conditioning for Implantable Systems

To power up an implantable system, three different sources of power can be used: 1) battery, 2) inductive link and 3) optical power transfer using photodiodes/photo cells. A brief discussion on these powering techniques and their practical limitations are discussed below.

1.3.1.1. Powering System Using Battery

Batteries can be only used in cavity areas of the human body. However, they are typically bulky and pose a risk of leakage which is toxic and potentially can result is series health risks to the patient. In addition, the batteries need replacement after being used for a period of time. Decreasing the system power consumption can help increase the total battery life time and reduce the need for frequent replacement.

1.3.1.2. Powering System Using Inductive Link

In comparison with batteries, inductive links can be implemented using smaller area without introducing leakage issues. In addition, because they utilize the energy being supplied from outside of the body, they do not need replacement. But these advantages come at the expense of lower efficiency. Due to the transmission of large amount of energy between the input and the output inductors through the human tissues, the area of human tissue can heat up by these inductors which can cause a series health problem as well. Therefore decreasing the total system power consumption can decrease the amount of power transferred through the tissues and improve the safety level of the entire system.

1.3.1.3. Powering System via Optical Means

Optical coupling is another method for sending power to the implanted system through the human body. Similar to the inductive links, a high amount of power transfer through the tissues can cause heat accumulation and create tissue burn in the area of power transfer [8]. Therefore this method can be only used in very low power implantable systems.

From the above discussion, it can be concluded that providing a continuous health-care monitoring using an implantable unit requires low-power circuit design for the entire implantable system. The design requirements for the implantable system such as sensitivity, bandwidth, stability and input common mode range make the low-power circuit design for these applications more challenging [9]. Therefore in the next section different techniques used for the low-power circuit design are discussed.

1.3.2. Low Power Design Techniques

Four major techniques in low-power circuit design are: 1) bulk-driven technique, 2) floating gate technique, 3) subthreshold biasing technique and 4) low-voltage design techniques. These techniques are briefly discussed in this section. Among these techniques, subthreshold design is chosen for this project and is discussed in more details in chapter 2.

1.3.2.1. Bulk-Driven Technique

In the bulk-driven technique the gate voltages of the transistors are kept high enough to make sure that these MOSFETs are always on. Then the AC signal is applied to the body (substrate) of the transistors. In this technique there is no threshold voltage limiting factor and therefore this design can be employed in the low-voltage circuit design. The disadvantage of this technique is the lower body transconductance. In addition the input DC voltage should be kept in a range that the body diodes are completely off during the variation of the AC input signal.

1.3.2.2. Floating Gates Technique

Floating gate is a polysilicon gate surrounded by silicon dioxide. Charge on the floating gates can be stored permanently. Therefore this technique has been used for long term memories. The level of this charge can be controlled by ultraviolet light or a large voltage. The trapped charge can be used to reduce the threshold voltage of the transistor to decrease the DC supply voltage requirement and therefore decrease the total power consumption [10].

1.3.2.3. Subthreshold Biasing Technique

Subthreshold bias means applying a difference potential lower than the threshold voltage to the gate-source of the transistor as its DC bias voltage. This level of gate-source voltage can weakly invert the transistor channel and therefore this level of inversion is also known as weak inversion. In comparison with the strong inversion circuit design that requires that the gate-source voltage of the transistors be higher than the threshold voltage, this technique can achieve higher transconductance efficiency for the same level of current.

1.3.2.4. Low-Voltage Design Technique

The low-voltage design technique includes all of the different circuit techniques that are designed to work in lower level of DC power supply voltage. These techniques can be applied along with the other

low-power design techniques to reduce both the DC power supply voltage and the current consumption of the system. Among the first three techniques, subthreshold technique is chosen as the low-power technique for this design.

1.3.3. Design of a Stable Potentiostat

Another important challenge in potentiostat design is achieving the system stability for all ranges of change in electrochemical solution model. The instability in the system can show itself like a noise at the output and makes it hard to detect the data. The main source of instability is the wide range of change in the electrical behavior of the electrode and the charge transfer medium in the blood during the oxidation. The instability problem in potentiostats has been discussed by the authors in [11, 12]. The authors in [11] mentioned that due to a pole contributed of the electrode in the charge transfer medium there is a good chance of instability. Commercial electrochemical potentiostats often report of oscillatory behavior of the system and the need for adding a large capacitor to achieve the stability [13]. Therefore it is very important to analyze the stability of the closed loop potentiostat circuits particularly when it is working with a solution that has a variable electrical behavior. Therefore to measure the blood glucose using a potentiostat it is important to have a clear understanding of its electrical behavior or its equivalent electrical circuit model.

1.3.3.1 Finding the Electrical Circuit Model for the Human Blood

The difference potential that is required to be applied between the working and the reference electrodes of a glucose measurement system is usually in the range of several hundred milli-volts, while the generated current from the sensor is usually in the range of hundreds of nA that can vary widely. A number of different models have been reported for modeling the microelectrodes and the chemical solution. Once of the models includes a parallel combination of a current source (I_{WE}) and a parasitic lumped R-C impedance [2] and another is just a combination of passive elements like resistors and capacitors. These two models are shown in Fig. 1.4(a) and 1.4(b), respectively. In either of these models,

the impedance is the combination of the voltage dependent polarized electrode junction capacitance and the double-layer parallel plate. Fig. 1.5 displays an R-C impedance approximation model between the electrochemical sensing electrodes [12]. In Fig. 1.5(a) each RC branch represents the electronic model of each working and reference electrodes. The resistors and capacitors in each branch can be combined into one parallel R-C network as shown Fig. 1.5(b) and therefore the final structure can be represented by a simple R-C combination as shown in Fig. 1.5(c) and Fig. 1.5(d).

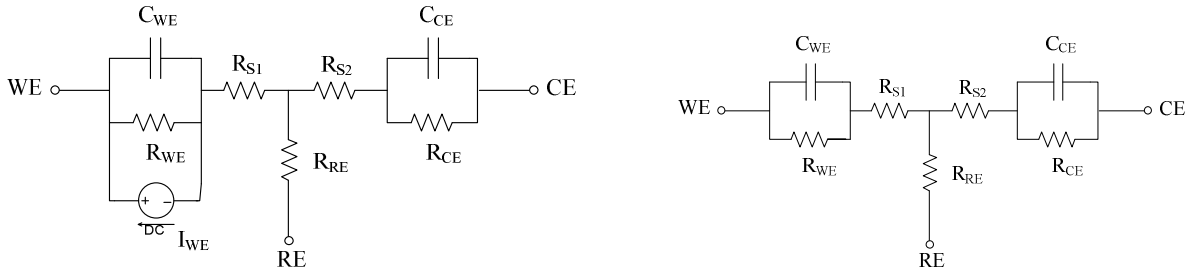


Fig. 1. 4. Two different electrical model for human blood chemical solution.

1.4. Research Goals

Based on the above discussion, using one of the low-power design techniques to reduce the implantable system power consumption as well as improving the stability of the potentiostat system are the goals of this research. The main focus of this work is on the potentiostat block and the signal processing unit block which are the central blocks of this system. These two blocks are also the major power consumers in this system.

Measurement block can be realized utilizing fiber optics [14]. But electrochemical biosensors (potentiostats) are more economical and convenient [15]. Therefore the main focus of this work is based on electrochemical potentiostats.

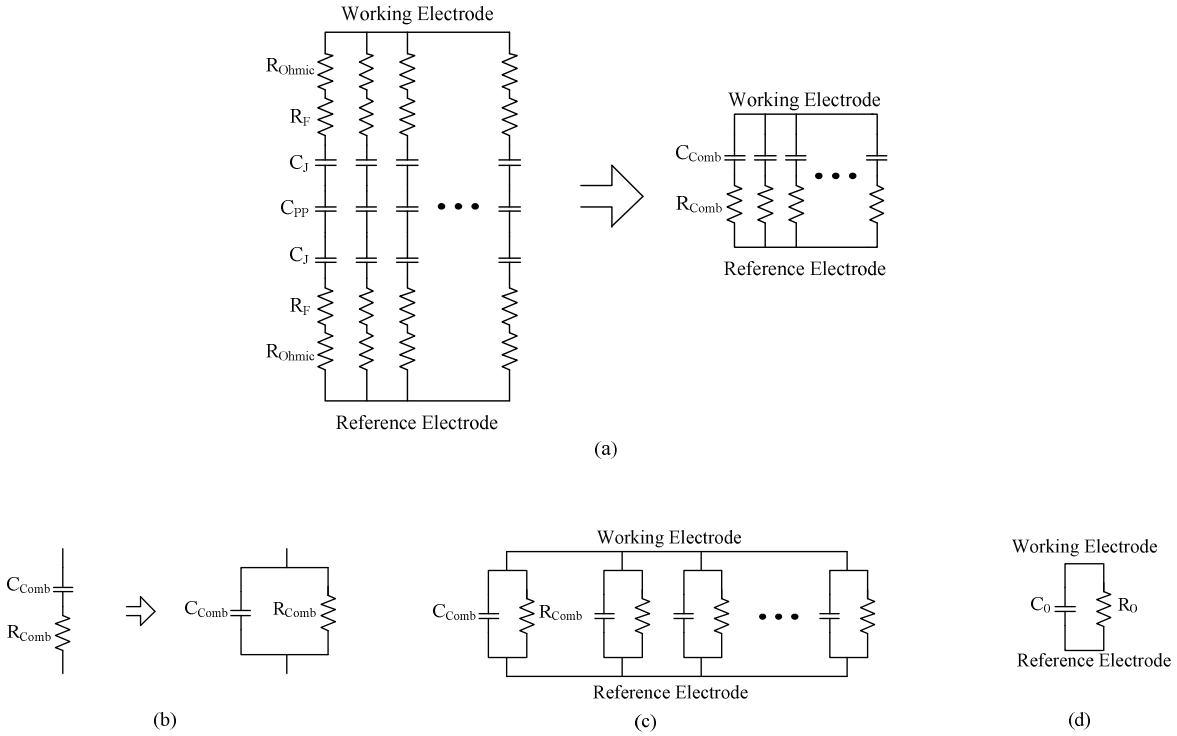


Fig. 1. 5. R-C modeling of the electrode–electrolyte setup: (a) model with series-connected R-C elements in each branch, (b) conversion of series-connected elements to parallel-connected elements, (c) model with parallel-connected R-C elements in each branch and (d) final lumped R-C model [12].

1.5. Original Contribution

In this work, a modification is applied to the traditional structure of potentiostat to solve its stability issue. The unconditional stability for wide range of current and models of chemical solution is achieved without adding any complexity or compensating technique. The simplicity of this structure and using fewer branches of current can help reduce the total power consumption of the implantable system.

This design also adopts the subthreshold biasing technique to reduce tremendous amount of power consumption and achieve the required stability. Correct sizing of transistors and redesigning the configuration of a folded cascode transconductance amplifier help this amplifier's open loop gain and its first dominant pole to be easily tunable. These important stability factors of this amplifier are set for maximum stability and minimum power consumption of the implantable potentiostat. In addition, the

accuracy of the electrochemical sensor current measurement is improved by designing a new current measurement technique.

1.6. Overview of the Dissertation

This dissertation is organized as follow: In chapter 2 subthreshold biasing technique which is the low-power design technique used in this work is introduced. In this chapter also the EKV model of transistors which is a dedicated model for low-voltage and low-current design including subthreshold design has been addressed. In chapter 3 an overview on conventional potentiostat structures is provided. In chapter 4, the stability problem of conventional designs is analyzed and the new structure is proposed. In chapter 5, the proposed signal processing unit has been introduced. Chapter 6 contains the design simulation and test results of the proposed circuits realized in 0.5µm and 0.35µm CMOS processes. Finally chapter 7 provides a conclusion of this work.

CHAPTER 2 – EKV Model and Subthreshold Design

For better understanding of the transistor behavior biased in subthreshold region, the EKV model is discussed first. The EKV model introduces an analytical model for transistors in all regions of operation. This model is also dedicated to the low-voltage and low-current designs. In this section, this model is discussed for better understanding of the subthreshold region of operation. Studying this model can help understand the physical reasons for the equations used in circuit design. Considering the effect of all of the physical parameters on the voltage and the current can improve the quality of the design and the robustness of the system.

2.1. EKV Model

EKV is a fully analytical MOS transistor model based on Enz, Krummenacher and Vittoz work in 1995 [16]. This model is dedicated to low-voltage, low-current designs. It also describes the behavior of the transistors in all levels of inversion with one unique equation. The elements in this model are all defined with respect to the body voltage. Therefore V_G means V_{GB}, the gate-body voltage and in the same way V_S means V_{SB} and V_D means V_{DB}. To derive the equation of the transistor current at any level of inversion, the accumulated charges around the gate in one tiny area have been surveyed first. The voltage under the gate in the semiconductor area (surface potential) for this small area can be considered constant. Different types of accumulated charges in this area are shown in Fig. 2.1. In this figure, $Q'_{inv} + Q'_B$ is the charge generated across C'_{ox} (C'_{ox} is the oxide capacitor (C_{ox}) divided by unit area). The voltage that gathers the charge across C'_{ox} includes the gate voltage, difference between metal and semiconductor work functions (flat band voltage (V_{FB})) and the surface potential (Ψ_s). The accumulated charge can be calculated from equation below:

$$Q'_B + Q'_{inv} = -C'_{ox}(V_G - V_{FB} - \Psi_s) \tag{2.1}$$

Here, Q'_{inv} is the inversion layer charge and is the part of the charges that can generate current. From equation (2.1) and considering $Q'_B = -\Gamma_b C_{ox}\sqrt{\Psi_s}$, this charge can be calculated to be:

$$Q'_{inv} = -C'_{ox}\left(V_G - V_{FB} - \Psi_s - \Gamma_b\sqrt{\Psi_s}\right) = -C'_{ox}(V_G - V_{TB}) \tag{2.2}$$

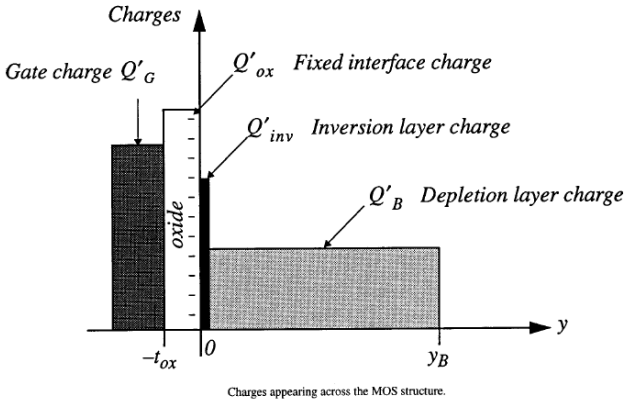


Fig. 2. 1. Charges accumulated across the gate of a MOSFET.

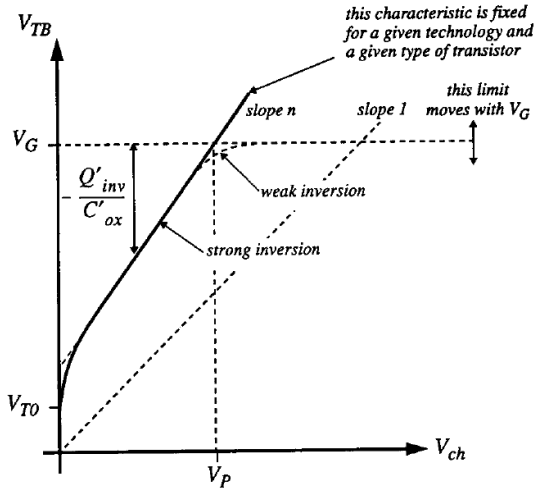


Fig. 2. 2. Illustration of equation (2.1)-(2.3).

Here V_{TB} can be defined to be:

$$V_{TB} = V_{FB} + \Psi_s + \Gamma_b\sqrt{\Psi_s} \tag{2.3}$$

where $\Gamma_b = \frac{\sqrt{2qN_b\epsilon_{si}}}{C_{ox}}$. From equation (2.3), it can be seen that as the voltage in the semiconductor area (Ψ_s) changes, the value of V_{TB} also changes. Fig. 2.2 shows the V_{TB} variation as a function of V_{ch} (which is the voltage under the gate area generated by the drain and the source voltages known as channel voltage ($V_{ch} = \Psi_s - \Psi_0$)) which is independent of the gate voltage (V_G). From equation (2.2), $V_G = V_{TB} - \frac{Q'_{inv}}{C'_{ox}}$ (Q'_{inv} is a negative number) and is shown in Fig. 2.2. From this figure, it is obvious that to bias a transistor in saturation region for a fixed V_G, the channel voltage (V_{ch}) needs to be reduced. Pinch-off voltage (V_p) is the value of V_{ch} at which no charges (or small charges) accumulate under the gate area. The transistor in this level of bias voltage represents "weak inversion" region.

From Fig. 2.2 the equation (2.3) can be linearized to the form below:

$$V_{TB} = V_{T0} + nV_{ch} \tag{2.4}$$

where n can be defined to be:

$$n = \frac{dV_{TB}}{d\Psi_s} = 1 + \frac{\Gamma_b}{2\sqrt{\Psi_s}} \tag{2.5}$$

In equation (2.4), V_{TB} is equal to V_G when V_{ch} is equal to V_P. Therefore V_P can be calculated to be:

$$V_p = \frac{V_G - V_{T0}}{n} \tag{2.6}$$

From semiconductor physics, Q_{inv} is proportional to an exponential function of Ψ_s, Φ_f and V_{ch} as shown below:

$$Q_{inv} \propto exp\frac{\Psi_s - 2\Phi_F - V_{Ch}}{U_T} \tag{2.7}$$

A derivation from this equation results in:

$$U_T \frac{dQ_{inv}}{Q_{inv}} = d\Psi_s - dV_{Ch} \tag{2.8}$$

Recalling from equation (2.5),

$$n = \frac{dV_{TB}}{d\Psi_s} = \frac{d^{Q'_{inv}}/_{C'_{ox}}}{d\Psi_s} = \frac{d^{Q_{inv}}/_{C_{ox}}}{d\Psi_s}|_{small\ area} \tag{2.9}$$

Substituting equation (2.9) in equation (2.8), it can be rewritten as below:

$$\frac{dV_{Ch}}{U_T} = \frac{dQ_i}{nU_T C_{ox}} - \frac{dQ_{inv}}{Q_{inv}} \tag{2.10}$$

If $v_{ch} = \frac{V_{Ch}}{U_T}$ and $q_i = {Q_{inv}}/{(-2nC_{ox}U_T)}$, the above equation can be simplified to the form:

$$-dv_{ch} = 2dq_i + dq_i/q_i \tag{2.11}$$

Integrating this equation results in:

$$Con_1 - v_{ch} = 2q_i + lnq_i \tag{2.12}$$

where Con_1 is a constant value. Here the boundary condition for V_p can be used to calculate Con_1 to be equal to V_P/U_T. Therefore defining $v_p = V_P/U_T$, the final equation is:

$$v_p - v_{ch} = 2q_i + lnq_i \tag{2.13}$$

Equation (2.13) defines the relationship between the accumulated charge and the voltage channel in each node of the channel. Therefore to calculate the current in the transistor channel, all the gathered charges under the gate area need to be integrated from the beginning node of the channel (source area) to its end (drain area) using the equation below:

$$I_D = \int_{v_s}^{v_d} q_i dv_{ch} \tag{2.14}$$

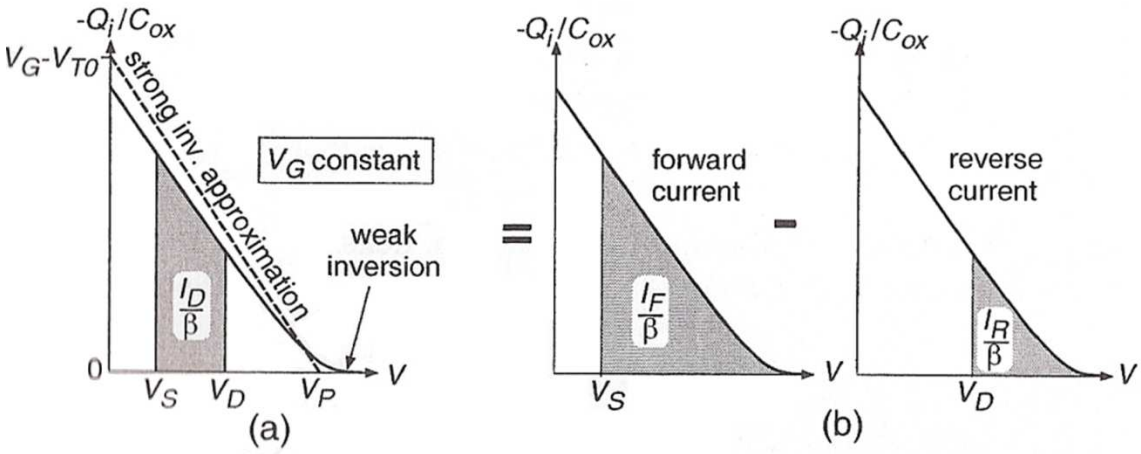


Fig. 2. 3. Current measurement as a subtract of forward and reverse current [17].

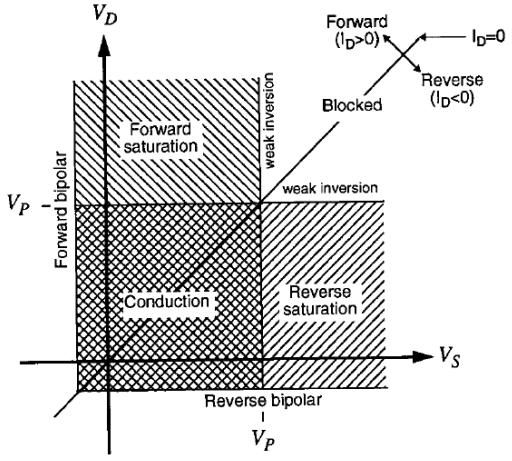


Fig. 2. 4. Summary of transistor modes of operation for different levels of source and drain voltages.

Another method of measuring the current is illustrated n in Fig. 2.3. In this figure it is assumed that V_S and V_D are both less than V_P. The small V_{DS} means that the transistor is biased in the linear region and because for a constant V_G, V_S is lot less than V_P, this transistor is biased in strong inversion. The summary of the transistor modes of operation based on its source and drain voltages is provided in Fig. 2.4. For calculations in each situation the current can be divided into two components: a forward current and a reverse current. For the forward current V_D is assumed to be equal to infinity and the current is measured just for the value of V_S from the equation below:

$$i_f = \frac{I_F}{I_{spec}} = \int_{v_s}^{\infty} q_i dv_{ch} \tag{2.15}$$

where $I_{spec} = 2n\mu C_{ox}\left(\frac{W}{L}\right)U_T^2 = 2n\beta U_T^2$ and W is gate width, L is gate length, μ is transistor mobility and $\beta = \mu C_{ox}\left(\frac{W}{L}\right)$. The reverse current can be calculated the same way by assuming V_S to be equal to infinity. Then the final transistor current I_D is calculated by subtracting these two currents.

By substituting dv_{ch} from equation (2.11) to equation (2.15), for both the forward and the reverse currents, one can find:

$$i_{f,r} = \int_0^{q_{s,d}} (2q_i + 1)dq_i = q_{s,d}^2 + q_{s,d} \tag{2.16}$$

where $q_{s,d}$ is charge density at node source or drain. From this equation $q_{s,d}$ can be calculated based on $i_{f,r}$ from the equation below:

$$q_{s,d} = \frac{\sqrt{1+4i_{f,r}}-1}{2} \tag{2.17}$$

From the equations (2.17) and (2.13), the relationship between the forward and the reverse currents with the source and the drain voltages can be found as follows:

$$v_p - v_{s,d} = \sqrt{1 + 4i_{f,r}} + \ln\left(\sqrt{1 + 4i_{f,r}} - 1\right) - (1 + ln2) \tag{2.18}$$

The reverse version of this equation can be estimated to be:

$$i_{f,r} = ln^2(1 + exp\frac{v_p - v_{s,d}}{2}) \tag{2.19}$$

From equation (2.19), two current values, one for forward current (i_f) and the other for reverse current (i_r), can be derived. The maximum value of this two is called "inversion coefficient (IC)" which defines the direction of current can be expressed as:

$$IC = \max(i_f, i_r) \tag{2.20}$$

In other modeling of NMOS transistors the drain current is the dominant current and therefore IC can be expressed as:

$$IC = i_d = \frac{I_D}{I_S} \tag{2.21}$$

From this equation it is evident that the drain current in strong and weak inversion regimes can be estimated as summarized in Table 2.1.

Table. 2. 1. Drain Current in Strong and Weak Inversion Regimes [17].

Mode	**Weak Inversion**	**Strong Inversion**
Conduction	$k_\omega . \beta . U_T^2 . e^{V_P/U_T} . \left[e^{-V_S/U_T} - e^{V_D/U_T}\right]$ for $\begin{cases} V_S > V_P \\ V_D > V_P \\ V_S \cong V_D \end{cases}$	$n.\beta.\left[V_p - \frac{V_S + V_D}{2}\right] . (V_D - V_S)$ for $\begin{cases} V_S \leq V_P \\ V_D \leq V_P \end{cases}$
Forward Saturation	$k_\omega . \beta . U_T^2 . e^{\frac{V_P - V_S}{U_T}}$ for $\begin{cases} V_S > V_P \\ V_D > V_P \\ V_D - V_S \gg U_T \end{cases}$	$\frac{n.\beta}{2} . (V_P - V_S)^2$ for $\begin{cases} V_S \leq V_P \\ V_D > V_P \end{cases}$
Blocked	0 for $\begin{cases} V_S \gg V_P \\ V_D \gg V_P \end{cases}$ or $V_S = V_D$	0 for $\begin{cases} V_S > V_P \\ V_D > V_P \end{cases}$

Using equation (2.19), the transconductance (g_m) of a transistor at all levels of inversion can be calculated. To calculate the g_m based on gate, drain and source voltages, the effect of small variation of each of these values on current variation need to be investigated as follows:

$$\Delta I_D = \frac{\partial I_D}{\partial V_G}\Big|_{V_S,V_D} \Delta V_G + \frac{\partial I_D}{\partial V_S}\Big|_{V_G,V_D} \Delta V_S + \frac{\partial I_D}{\partial V_D}\Big|_{V_s,V_G} \Delta V_D \tag{2.22}$$

By keeping V_S and V_D constant, g_m based on the gate variation can be calculated as below:

$$g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_S,V_D} \Delta V_G \cong \frac{{}^{I_D}/_{I_S} U_T}{\sqrt{{}^{I_D}/_{I_S} + {}^{1}/_{2}} \cdot \sqrt{{}^{I_D}/_{I_S}} + 1} \tag{2.23}$$

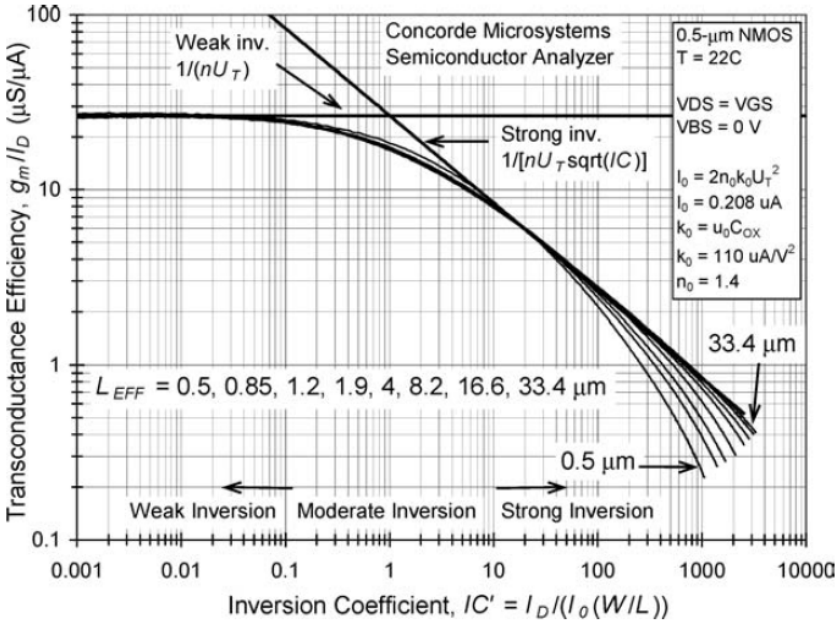


Fig. 2. 5. Transconductance efficiency in different regions of operation [18].

Based on equation (2.23), g_m for two conditions of strong inversion (S.I.) and weak inversion (W.I.) can be simplified as below:

$$g_m = \begin{cases} \sqrt{2n\beta I_D} & {I_D}/{I_S} > 10 \ \ (S.I.) \\ \frac{I_D}{nU_T} & {I_D}/{I_S} < 0.1 \ \ (W.I.) \end{cases} \tag{2.24}$$

Fig. 2.5 shows the transconductance efficiency (g_m/I_D) based on its level of conversion. From this figure it is evident that transistors achieve their maximum transconductance efficiency in W.I. Similar to the BISIM model the EKV model includes many second order effects such as mobility degradation due to vertical field, velocity saturation and channel length modulation [19].

2.2. Subthreshold Design Considerations

In this section the main important issues associated with MOSFETs operating in subthreshold region, such as mismatch, noise, drain induced barrier lowering (DIBL) and process- voltage-temperature (PVT) variation are discussed.

2.2.1. Mismatch

The two major source of mismatch in transistors are the difference between the threshold voltages (ΔV_T) and the difference between the current factors ($\Delta\beta$). These difference values have normal random distribution with zero mean value. The variance of these differences is dependent to the device size as presented by [20]:

$$\sigma^2(\Delta V_T) = \frac{A_{VT}^2}{W.L} \tag{2.25}$$

$$\left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 = \frac{A_\beta^2}{W.L} \tag{2.26}$$

where A_{VT} and A_{β} are technology dependent parameters. T. Mizuno et al [21] measured the threshold voltage (V_T) of 8000 transistors and derived the distribution histogram shown in Fig. 2.6. A. Asenov [22] estimated threshold voltage variance to be;

$$\sigma(\Delta V_T) = 3.19 \times 10^{-8} \frac{t_{ox} N_A^{0.4}}{\sqrt{L.W}} \tag{2.27}$$

To calculate the effect of mismatch on circuit performance, M_1 and M_2 can be considered to be a pair of matched transistors used in a current mirror where the threshold voltage of $M_{1,2}$ has a deviation of $\delta V_{T1,2}$ form its mean value of V_{T0}. Therefore $\Delta V_T = \delta V_{T1} - \delta V_{T2}$ and similarly, $\Delta\beta = \delta\beta_1 - \delta\beta_2$. In this case, the mismatch between M_1 and M_2 biased in saturation can be derived as:

$$\left(\frac{\sigma(\Delta I_{DS})}{I_{DS}}\right)^2 = \left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 + \left(\frac{g_m}{I_{DS}}\right)^2 \sigma^2(\Delta V_T) \tag{2.28}$$

$$\sigma^2(\Delta V_{GS}) = \sigma^2(\Delta V_T) + \left(\frac{I_{DS}}{g_m}\right)^2 \left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 \tag{2.29}$$

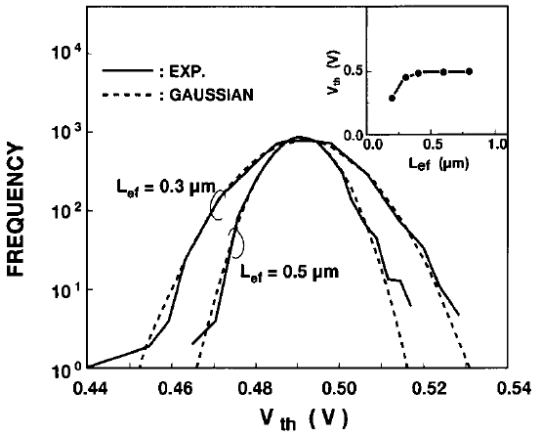


Fig. 2. 6. Threshold voltage distribution for 8000 MOSFETs in a 0.5µm and 0.3µm CMOS process [21].

From equations (2.28) and (2.29), the maximum g_m/I_{DS} achieved in W.I. improves voltage matching but it degrades the current matching.

Another source of mismatch is the gate leakage. Taking the gate leakage variation into account, the total current variation can be measured to be [23]:

$$\frac{\sigma^2_{Ids}}{I^2_{DS}} = \left(\frac{A_{VT}}{\sqrt{W.L}}.\frac{g_m}{I_{DS}}\right)^2 + \left(\frac{0.03}{\sqrt{W.L}}.\frac{I_G}{I_{DS}}\right)^2 \quad (2.30)$$

where I_G is the gate leakage current.

2.2.2. Noise

There are mainly two sources of noise: flicker noise and thermal noise. Flicker noise is generally important in low-frequency circuit design and is thought to be caused by crystal defects and contaminations [24]. Input referred flicker noise can be represented by:

$$\overline{v_i^2} = \left(\frac{K_f}{WLC_{ox}f}\right)\Delta f \quad (2.31)$$

From equation (2.31) it is obvious that increasing transistor size can help decrease this source of noise in low-frequency design. Another important source of noise is thermal noise, which is due to random thermal motion of electrons, and therefore it is directly proportional to the temperature (T). The input referred thermal noise of a MOSFET can be represented by [24]:

$$\overline{v_i^2} = 4kT\left(\frac{2}{3g_m}\right)\Delta f \quad (2.32)$$

From equation (2.32) it can be seen that the input referred thermal noise has a reverse relationship with transistor transconductance (g_m). Thermal noise can be decreased with higher values of power consumption.

For the same level of current, biasing the transistor in W.I. can help maximize g_m and improve the input referred noise. Besides, to bias the transistor in this level of inversion, the size of transistor need to be increased which also helps decreasing the flicker noise. Therefore subthreshold design can be a very good option for low noise, low-frequency designs.

To compare the efficiency of circuits based on their current consumption and their input referred noise a noise efficiency factor has been defined in [25] to quantify this tradeoff:

$$NEF = V_{rms,in}\sqrt{\frac{2.I_{tot}}{\pi.U_T.4kT.BW}} \tag{2.33}$$

where $V_{rms,in}$ is the input referred noise.

2.2.3. Drain Induced Barrier Lowering (DIBL)

In long channel devices the drain and the source are separated far enough so that their depletion regions do not affect each other. However, in shorter channel devices the drain voltage can influence the depletion region and change the channel potential. This can affect the leakage current by reducing the transistor threshold voltage. This phenomena is called drain induced barrier lowering (DIBL) [26]. Higher drain voltage or shorter channel length increases the DIBL effect. Therefore this phenomenon is more obvious in submicron technology. The bias current of MOS devices operating in subthreshold region considering DIBL and body effect can be modeled as below [27]:

$$I_{DS} = \mu_0 C_{ox}\frac{W}{L}(m-1)U_T^2 e^{\frac{V_G - V_T}{mU_T}}\left(1 - e^{\frac{-V_{DS}}{U_T}}\right) \tag{2.34}$$

where V_T is the threshold voltage, μ_0 is the zero bias mobility and m is the subthreshold swing coefficient (body effect coefficient) and is equal to:

$$m = 1 + \frac{C_{dm}}{C_{ox}} = 1 + \frac{\frac{\epsilon_{si}}{W_{dm}}}{\frac{\epsilon_{ox}}{t_{ox}}} = 1 + \frac{3t_{ox}}{W_{dm}} \tag{2.35}$$

where C_{dm} is the capacitance of the depletion layer, t_{ox} is the gate oxide thickness and W_{dm} is the maximum depletion layer width.

2.2.4. Process-Voltage-Temperature (PVT) Variation

From Table 2.1 and equation (2.6) for V_P, the transistor current in subthreshold region can be derived in the form as shown below:

$$I_{DS} = K_\omega \beta U_T^2 e^{\frac{V_G - V_{T0}}{n}} \left(e^{\frac{-V_S}{U_T}} - e^{\frac{-V_D}{U_T}} \right) \tag{2.36}$$

From equation (2.36) it can be seen that there is an exponential relationship between the drain current and the transistor gate voltage. Therefore a small change in the gate voltage or the threshold voltage can result in a large change in the drain current. This sensitivity can be useful in the circuits with wide current tuning range but it also represents high sensitivity to PVT variation [19].

2.3. Subthreshold Design Examples

From the above discussion it can be concluded that the subthreshold design can be used in low-power, low-noise and low-frequency circuit design. The exponential relationship between the drain current and the gate voltage makes this mode of operation suitable for wide current tuning range circuits but also makes them more susceptible to PVT variation. This exponential relationship (similar to BJT transistors) limits the input voltage linear range. For a simple operational transconductance amplifier (OTA) biased in subthreshold, this range can be as low as 80mV [28, 29]. Therefore this design scheme can be only applied to the circuits that have no or low linearity requirements. For circuits with more input

linear range requirement, linearization techniques can be applied. Some examples of this scheme are discussed in the following section.

2.3.1. Amplifier Design for Neural Recording

Small signal level of neural signal makes neural recording less sensitive to linearity and more sensitive to noise level [24]. Therefore subthreshold design can be a good option for neural recording circuit design. Fig. 2.7 shows a common structure in neural amplifier design. R. R. Harrison et. al [30] used OTA structure shown in Fig. 2.8 biased in subthreshold region to improve the noise efficiency factor (NEF) and reduce the power consumption of this structure. Although the circuit topology used for OTA is a standard design, the sizing of the transistors is critical for low-noise low-power design.

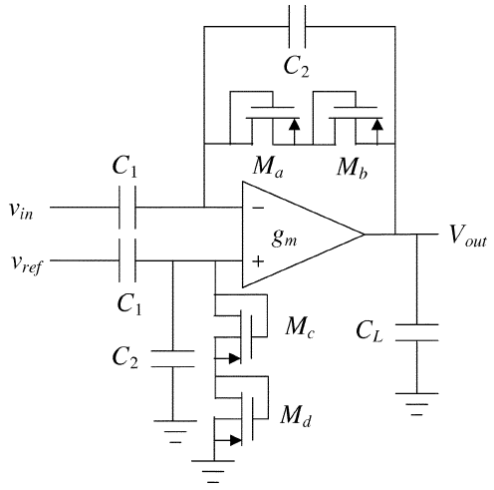


Fig. 2. 7. Schematic of a common neural amplifier [30].

To improve the efficiency of this structure (and decrease the NEF defined in equation (2.33)), the input referred noise must be designed to be as low as possible. For this circuit the input referred noise is calculated to be:

$$\overline{v_{in,thermal}^2} = \left[\frac{16kT}{3g_{m1}}\left(1 + 2\frac{g_{m3}}{g_{m1}} + \frac{g_{m7}}{g_{m1}}\right)\right]\Delta f \tag{2.37}$$

From equation (2.37) it is evident that improving the input referred noise requires high transconductance of the input transistors (g_{m1} and g_{m2}) and low transconductance of the current mirror transistors ((g_{m1} and g_{m2})>>(g_{m3} and g_{m7})). Therefore M_1 and M_2 are biased in subthreshold region to achieve the maximum transconductance efficiency and M_3 and M_7 are biased in strong inversion to get lower values of the transconductance. The thoughtful choice of the transistor sizing in this work reduces the input referred noise to 2.2µV_{rms} and the NEF to 2.9 with a power consumption of 80µW.

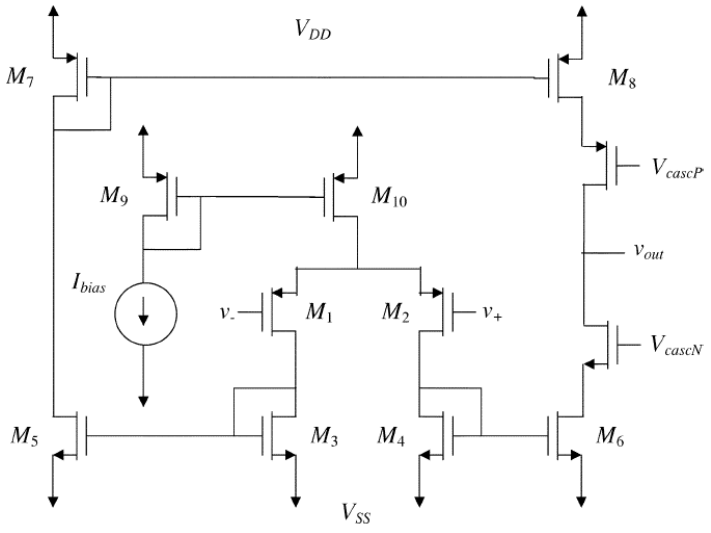


Fig. 2. 8. Schematic of OTA used in Fig. 2.7 [30].

2.3.2. Linearization Technique for Subthreshold Amplifiers

Many techniques have been proposed to improve the input linear range of the subthreshold amplifiers. An example using multiple input floating gate (MIFG) is discussed in [31]. Fig. 2.9 shows the OTA structure in this design. This design uses cubic-distortion-term-canceling technique for improving the linearity.

In the structure shown in Fig. 2.9, transistor M_3 is added to average the difference of the input voltages. All of the transistors are biased in subthreshold region of operation and their bodies are connected to ground. With $V_{pol1} = V_{pol2} = V_{pol3} = V_{dd}$ the current i_1, i_2 and i_3 can be expressed as:

$$i_1 = I_{D01}\exp\left(\frac{\kappa(\omega_1 V_+ + \omega_2 V_{dd}) - V_S}{U_T}\right) \tag{2.38}$$

$$i_2 = I_{D02}\exp\left(\frac{\kappa(\omega_1 V_- + \omega_2 V_{dd}) - V_S}{U_T}\right) \tag{2.39}$$

$$i_3 = I_{D03}\exp\left(\frac{\kappa\left(\frac{\omega_1}{2}(V_+ + V_-) + \omega_2 V_{dd}\right) - V_S}{U_T}\right) \tag{2.40}$$

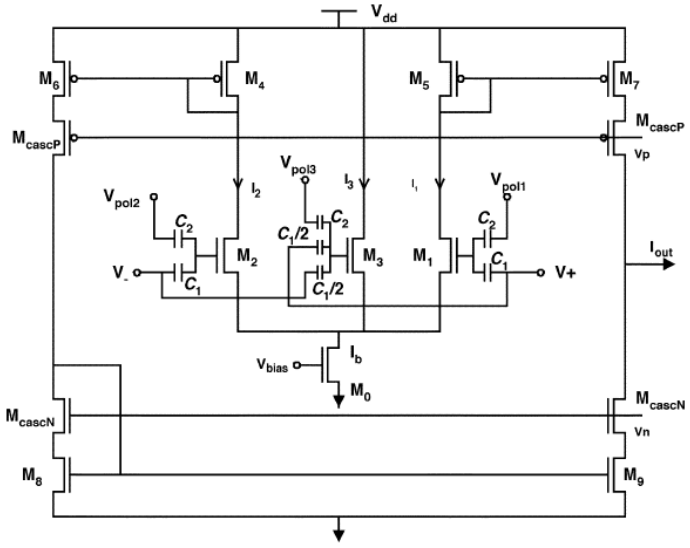


Fig. 2. 9. Subthreshold OTA using MIFG MOS transistors.

where κ is the electrostatic coupling coefficient between the floating gate and the channel, ω_i is given by C_i/C_T ratio and V_S is the source voltage. Therefore I_{out} can be calculated to be:

$$I_{out} = I_2 - I_1 = I_b \frac{\sinh(x)}{\cosh(x) + A} \tag{2.41}$$

Where $x = \omega_1(\kappa V_{id}/2U_T)$ and $A = \frac{(W/L)_3}{2(W/L)_{1,2}}$. Expanding equation (2.41) in the Taylor series gives:

$$I_{out} = \left(\frac{1}{1+A}\right) I_b \left[x + \left(\frac{1}{6} - \frac{1}{2(1+A)}\right) x^3 + \left(\frac{1}{120} - \frac{3}{24(1+A)} + \frac{1}{4(1+A)^2}\right) x^5 + \cdots\right] \quad (2.42)$$

From equation (2.42) it is obvious that the smaller values of input capacitive ratio (ω_i) will result in larger input linear range. In addition it is apparent that for A = 2, the cubic distortion term can be completely removed. The simulation results for different values of ω_1 are shown in Fig. 2.10.

Source degeneration is another example of linearity improvement technique. Different schemes of degeneration technique are introduced in [32]. Fig. 2.11 shows the diffusor degeneration technique along with symmetric diffusors degeneration technique. In this paper the differential current for diffusor degenerated technique is calculated to be:

$$I_{DM} = I_b tanh\left(\frac{\kappa V_{DM}}{2U_T} - tanh^{-1}\left[\frac{sinh\left(\frac{\kappa V_{DM}}{2U_T}\right)}{2m+cosh\left(\frac{\kappa V_{DM}}{2U_T}\right)}\right]\right) \quad (2.43)$$

where $I_{DM} = I_1 - I_2$, $V_{DM} = V_1 - V_2$ and $m = (W/L)_b/(W/L)_a$. With the same parameters, the differential current for symmetric degeneration technique is calculated to be:

$$I_{DM} = I_b tanh\left(\frac{\kappa V_{DM}}{2U_T} - tanh^{-1}\left[\frac{tanh\left(\frac{\kappa V_{DM}}{2U_T}\right)}{4m+1}\right]\right) \quad (2.43)$$

Fig. 2.12 shows the simulation results of input transconductance versus the input differential voltage plot for these two cases. In this figure the transistor transconductance is normalized to its maximum value.

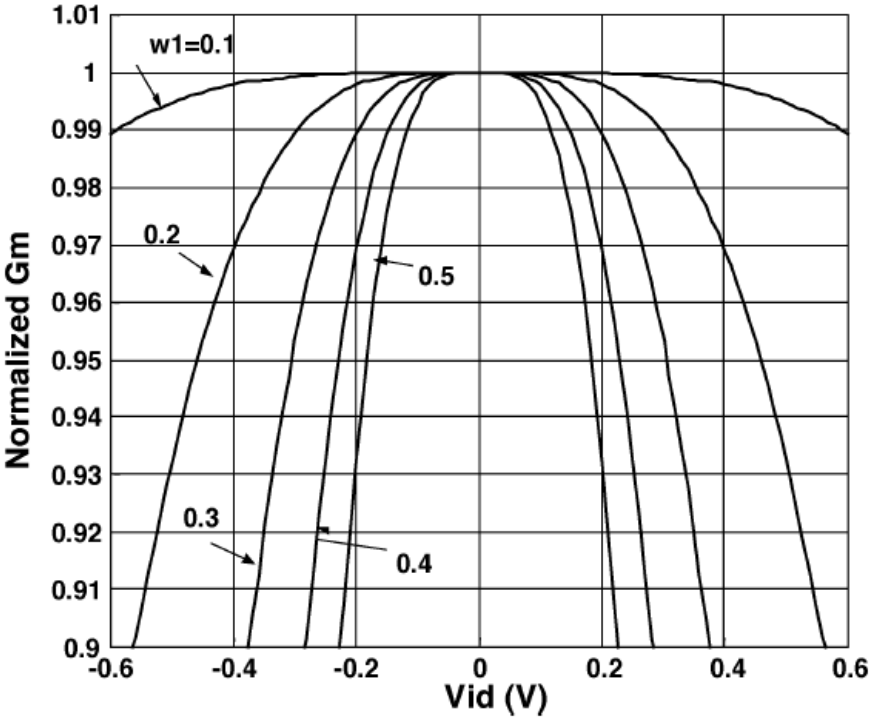


Fig. 2. 10. Normalized transconductance versus differential input for different values of $\boldsymbol{\omega_1}$.

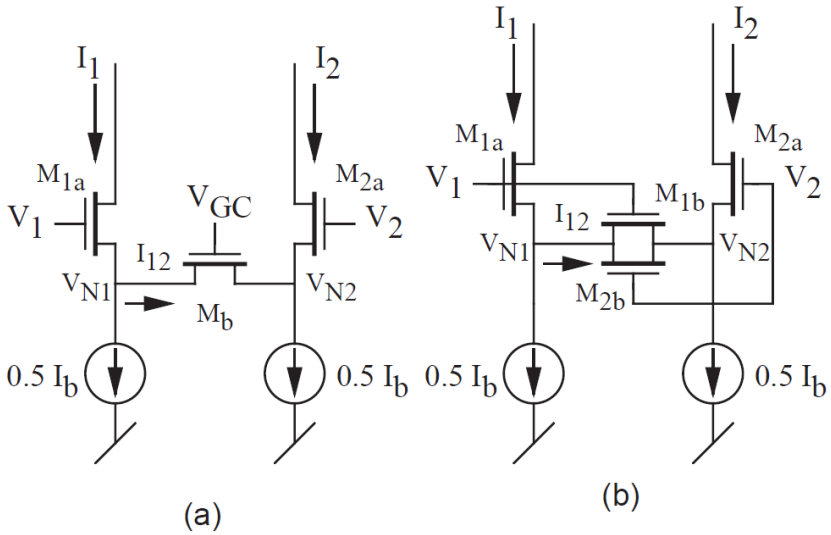


Fig. 2. 11. One differential pair degenerated with: (a) one diffusor and (b) symmetric diffusors.

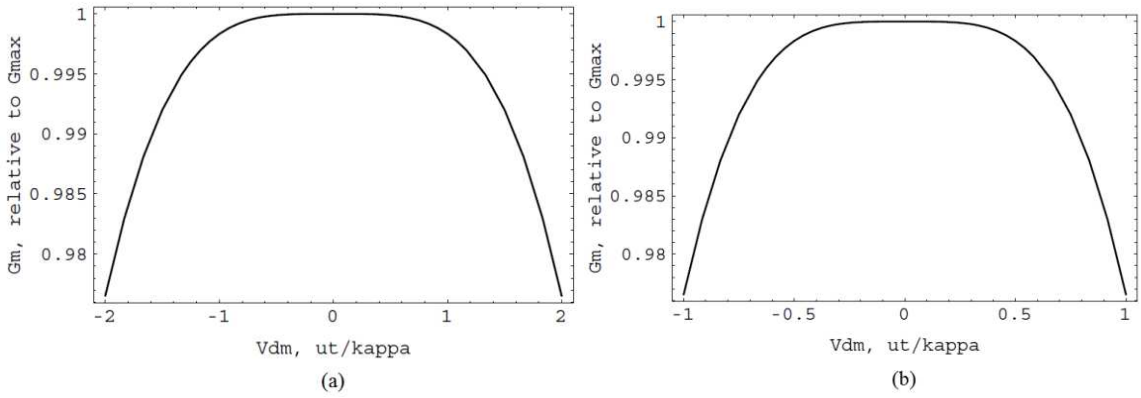


Fig. 2. 12. Simulation results for using degenerative technique via: (a) single diffusor and (b) symmetric diffusor.

In addition to these examples, number of other design schemes using subthreshold technique for very low-power filter design [33] and low-voltage OTA design [34] have been reported in literature.

CHAPTER 3 – Literature Review on Potentiostat

Potentiostat is a circuit that is directly in physical contact with the electrochemical sensor. These sensors consist of three electrodes: 1) working electrode (WE), 2) reference electrode (RE) and 3) counter electrode (CE). RE is used to measure the solution potential while CE is a conductor for supplying the required current for electrochemical reaction that take place at WE [35]. Potentiostat is responsible for maintaining a constant difference potential across the working and the reference electrodes.

The two major electromechanical biosensor structures are oxygen-electrode-based (O_2 based) and hydrogen-peroxide-electrode-based (H_2O_2-based) sensors. In O_2-based sensors, with a standard Ag/AgCl electrode used for RE, potentiostat has to provide a constant -600mV at WE with respect to RE. In this case, the reduction of oxygen at the surface of WE results in the output current. This output current direction is from CE to WE. However in H_2O_2-based sensors, the output current is the result of the oxidation of hydrogen peroxide at the surface of WE. This current direction is from WE to CE. For a standard Ag/AgCL electrode used for RE, the potentiostat has to provide +700mV at WE with respect to RE [35]. These two potentiostat configurations are shown in Fig. 3.1. In this structure an operational amplifier (opamp) is employed to provide a constant voltage between WE and RE.

For better analyzing the stability and the performance of these potentiostats, an electrical model is defined for the human electrochemical solution shown in Fig. 3.2. In this figure C_{CE} and C_{WE} represent the double-layer capacitance of the electrodes CE and WE. R_{CE}, R_{WE} and R_{RE} represent the charge transfer resistance of these electrodes and R_{S1} and R_{S2} represents the solution resistances which are very small and negligible [35].

The basic idea of a potentiostat structure is also shown in Fig. 3.1. A number of other structures are reported in literature for potentiostat design. These structures can be divided into three main groups: 1) resistive-based potentiostats, 2) capacitive-based potentiostat and 3) current mirror-based potentiostats. In

this section some examples of potentiostats using any of the different structures and their advantages and disadvantages over each other are briefly discussed.

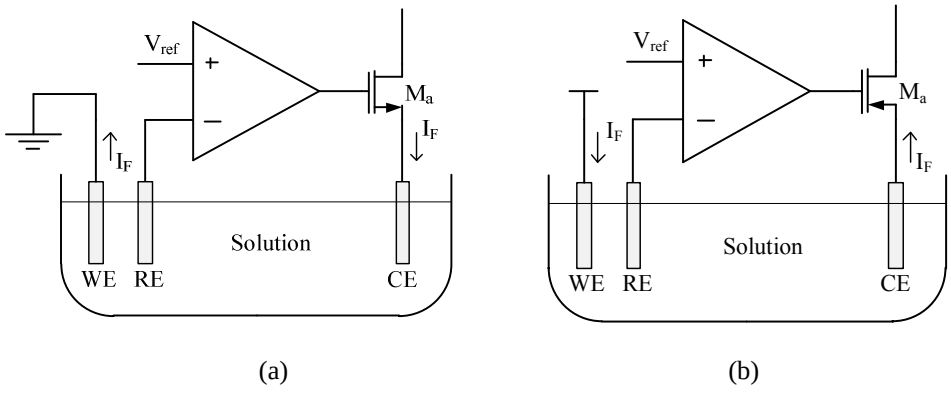


Fig. 3. 1. a) A three-electrode electrochemical solution and potentiostat for V_{WE}-V_{RE}>0, b) A three-electrode electrochemical solution and potentiostat for V_{WE}-V_{RE}<0.

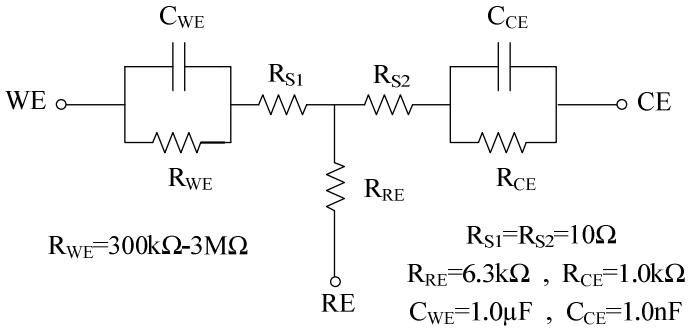


Fig. 3. 2. Generic equivalent circuit of an electrochemical cell [35].

3.1. Resistive-Based Potentiostat

Fig. 3.3 shows the first simple idea for potentiostat along with its signal processing unit which is composed of resistor and opamp. In this structure opamp provides a constant voltage between CE and RE and based on that the generated current can pass though the resistor and generate the output voltage proportional to the output current. The problem with this structure is that the input resistance of the transconductance amplifier increases with frequency and therefore it behaves as an inductive load. From the model of the chemical solution shown in Fig. 3.2, the solution behaves like a large capacitor in the

node of its connection to the signal processing unit. Therefore connecting the transconductance amplifier to the output of the chemical solution can cause instability. L. Busoni et al. [36] proposed the structure shown in Fig. 3.4 to solve the stability problem of Fig. 3.3. In this structure a compensation technique is used to improve the stability. This design employs two OPA627 for the opamps and the other elements are all off-chip and from the values of resistors in this circuit, it is evident that this circuit consumes a high level of power.

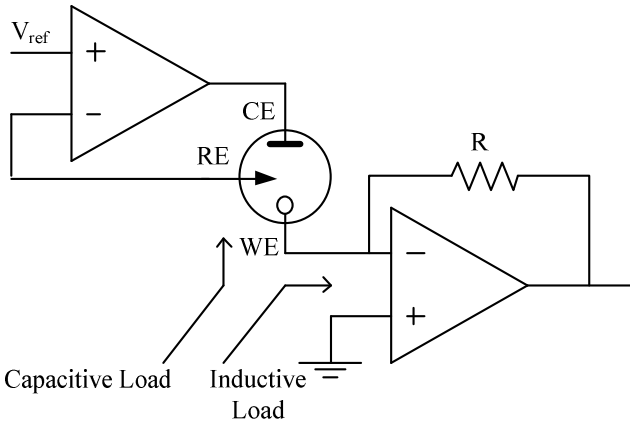


Fig. 3. 3. Basic current measurement configuration using resistor.

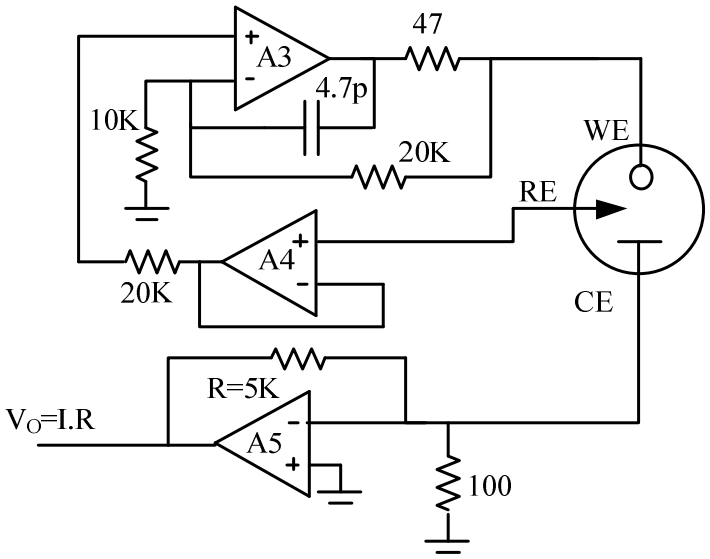


Fig. 3. 4. L. Busoni et. al [37] design for improving the stability in potentiostat design.

Another potentiostat design technique that is made of opamps and resistors is shown in Fig. 3.5. In this structure the working electrode is kept at virtual ground and the voltage at the reference electrode is controlled through the feedback. The fully differential version of this structure is shown in Fig. 3.6. This structure can help improve the dynamic range in comparison with the single-ended version [38]. This design is fabricated in a 0.18µm CMOS process. The single-ended structure is consuming 4.8mA with a power supply voltage of 1.8V and the differential structure consumes 8.8mA with the same power supply voltage.

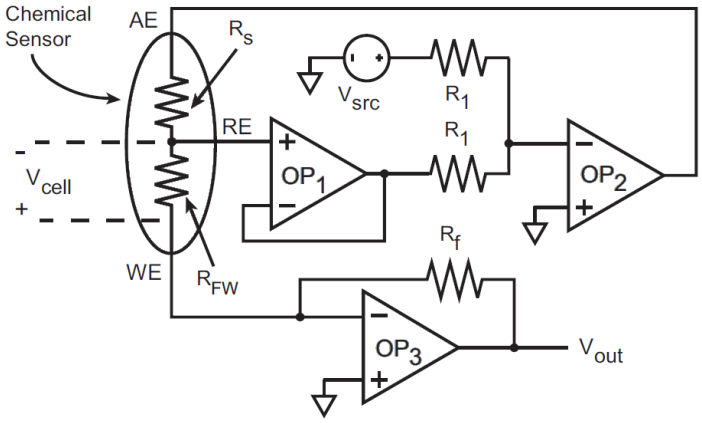


Fig. 3. 5. Schematic of a single-ended potentiostat [38].

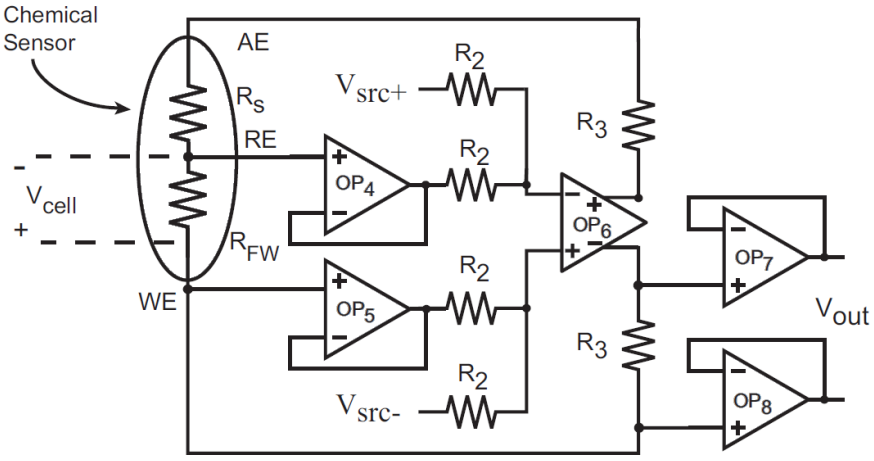
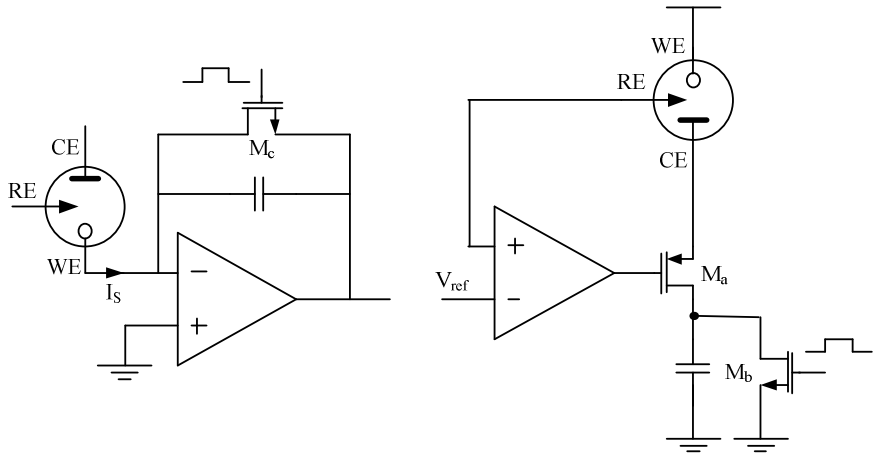


Fig. 3. 6. Schematic of a fully differential potentiostat [38].

Y. Temiz et al. [39] employed a compensation technique to improve the stability of the single-ended potentiostat shown in Fig. 3.5. C. Yang et al. [40] used the single-ended structure in an array. The array structure is fabricated using a 0.5µm CMOS process. The fabricated chip consumes 0.6mA of current with a power supply voltage of 5V. The same structure of potentiostat have also been used in different other applications. S. B. Prakash et al. [41] used this structure to control integrated MEMS. This circuit is fabricated using a 0.5µm CMOS process. S. Hwang et al. [42] used this structure for detection of heavy metal ions in water. This design was also fabricated using a standard 0.5µm CMOS process. The fabricated system consumes 3.8mA of current with a supply voltage of 5V.

3.2. Capacitive-Based Potentiostat

Resistors consume substantial chip area and huge amount of power. An alternative scheme of potentiostat design uses capacitors. This type of potentiostat generates the required difference potential by using just one opamp and uses a capacitor in the path of the sensor current to measure its value. The voltage across the capacitor is simply the integral of its current. Therefore the time required for the capacitor to be charged to some level of voltage can be used as a measurement tool of its current. In many of these structures, the capacitor is being discharged by using MOS switches when it reaches a certain level of voltage. In this case the frequency of the discharging of the capacitor can be used as the output of the current measurement block. The current integration using a capacitor can be performed by either of the techniques shown in Fig. 3.7. Using a capacitor instead of a resistor increases the range of the sensor current measurement. The small values of current generate a very low voltage across the resistor that makes it hard to detect and therefore for that level of current a larger resistor is needed. But the structures using capacitor does not need a larger value of the capacitor and the small amount of current can still charge the large capacitor but for longer time which leads to lower comparator output frequency and thus can easily be detected.



(a) (b)

Fig. 3. 7. a) Current integration mostly used in current measurement using delta-sigma modulator. b) Current integration with a path of discharge which will be activated after capacitor reaches certain level of voltage.

In some applications where the accuracy of the potentiostat current measurement is critical , the potentiostat is employed to measure the currents in the range of femto ampere using a delta-sigma modulator as a recovery block that can help achieve the required performance [43-45]. The building block of this structure is shown in Fig. 3.8. In these designers, the integral structure shown in Fig. 3.7(a) is used as the integrator block in the delta-sigma modulator structure.

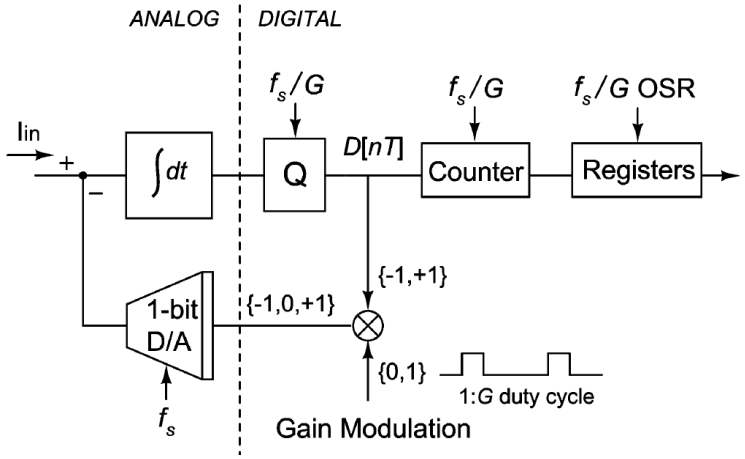


Fig. 3. 8. Block diagram of a delta-sigma current measurement block of an accurate potentiostat [44].

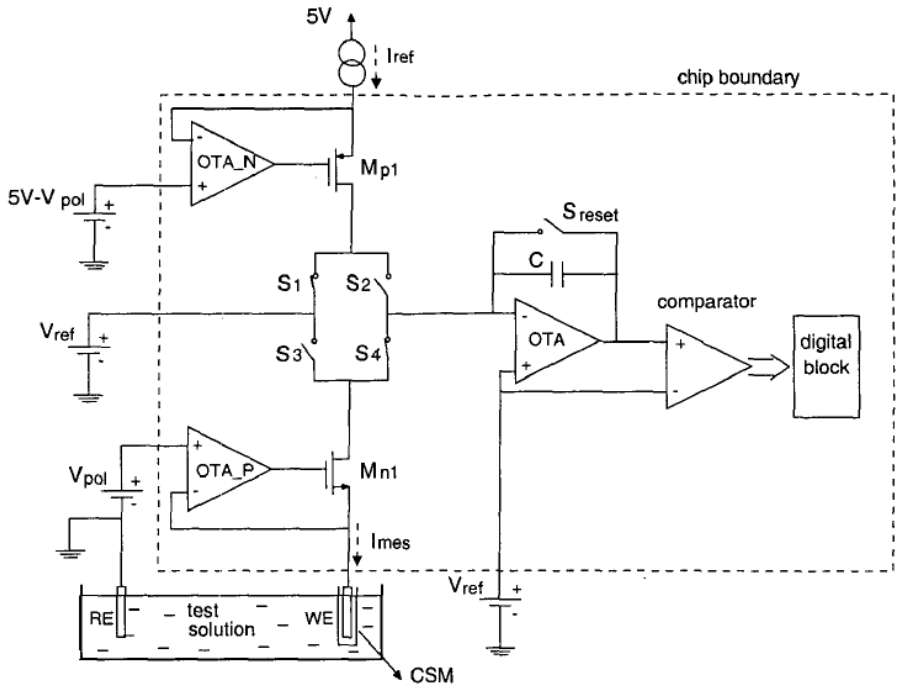


Fig. 3. 9. The current measurement technique according to M. Breten [46].

Another example that employs a capacitor for integrating the sensor current can be found in [46]. In this paper M. Breten et al. used Fig. 3.7(a) integrator to generate saw-tooth wave pulses by charging and discharging the capacitor. This configuration is shown in Fig. 3.9. In this configuration the sensor current (I_{mes}) charges the capacitor through switch S_4 for time t_{up} and a constant DC current source (I_{ref}) discharges the capacitor through the switch S_2 for time t_{down}. The voltage across the capacitor is shown in Fig. 3.10. The ratio of the charging time to the discharging time is proportional to the ratio of the sensor current to the current source current provided in this structure. This can be rewritten as:

$$I_{mes} = I_{ref} \frac{t_{down}}{t_{up}} \tag{3.1}$$

The other technique for integrating the current using a capacitor along with a discharging switch is shown in Fig. 3.7(b) [47-53]. The output signal of this technique is similar to the one discussed in Fig. 3.10. In each cycle the sensor current charges the capacitor until it reaches a certain level of voltage while

a comparator can detect this level of voltage and allow the transistor M_b to completely discharge the capacitor. The frequency of the control signal which is applied to the gate of the transistor M_b to discharge the capacitor is the output signal of this structure.

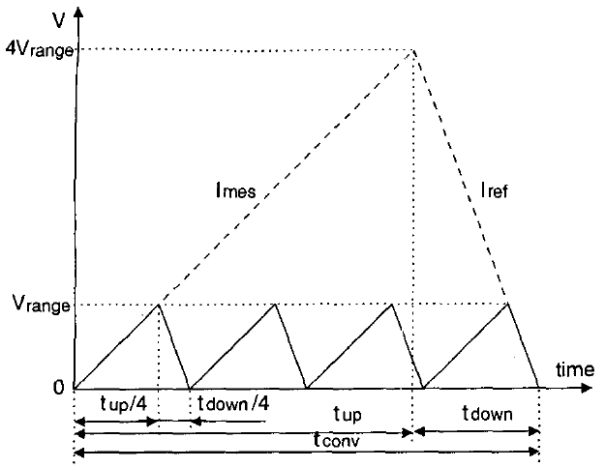


Fig. 3. 10. Voltage across the capacitor in structure shown in Fig. 3.9.

All of these examples use the capacitor as an element to integrate the generated current in the solution. Using the integrator with the technique shown in Fig. 3.7(b) in comparison with Fig. 3.7(a) can achieve three advantages. First; it needs only one opamp which leads to higher stability and less power consumption, second; the voltage across the opamp is not changing while the capacitor voltage is charging which helps to improve the stability and third; the opamp in this structure is not responsible for driving a huge resistive load and hence reduces the output stage current requirement which leads to lower power consumption. Using the capacitor instead of the resistors introduces a number of advantages, however, the stability is still an important issue in these designs which is discussed in [12, 50].

3.3. Current Mirror-Based Potentiostat

To further improve the stability and to prevent the discharging pulses from affecting the potentiostat system, a current mirror can be employed as shown in Fig. 3.11 [35, 54-59]. In this structure

a mirror of the original sensor current is used for current measurement which can be performed either by passing the current through a resistor or by integrating the current through a capacitor.

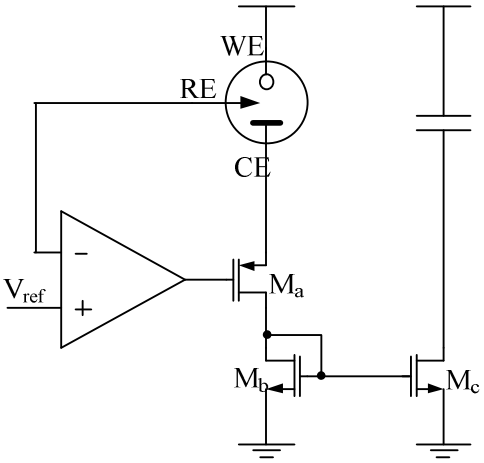


Fig. 3. 11. Current mirror configuration for separation between potentiostat and its current measurement (SPU) part.

Although this structure separates the current measurement block from the potentiostat and the electrochemical sensor, the variable pole in the chemical solution can still cause instability. R. Thewes et al. [54] employed a capacitor at the output node of the opamp to improve the stability and M. M. Ahmadi et al. [35] reported a modified version of this circuit to solve the start-up issue as shown in Fig. 3.12. The implementation of this structure is shown in Fig. 3.13.

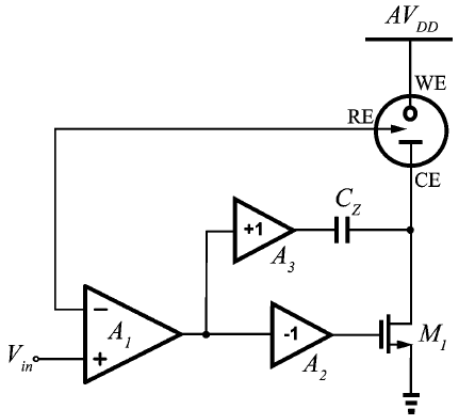


Fig. 3. 12. A poentiostat structure for improved the stability according to M. M. Ahmadi et al. [35].

In the next chapter, the current mirror- based potentiostat is analyzed and a solution for the stability problem is proposed.

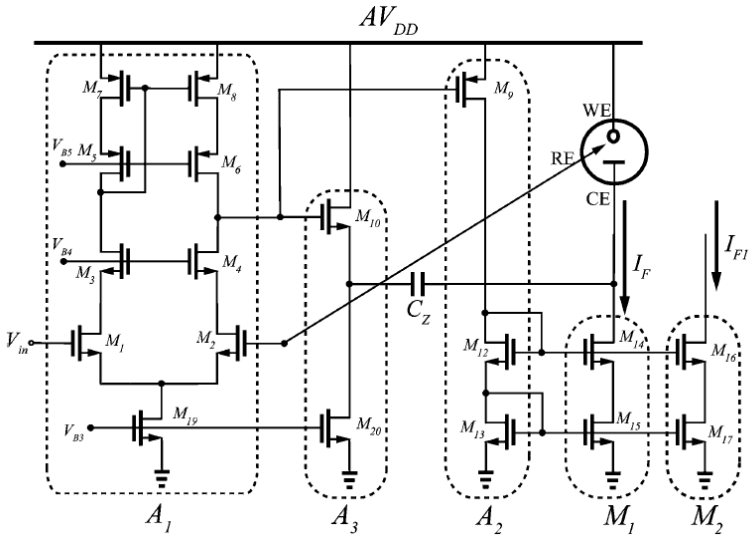


Fig. 3. 13. M. M. Ahmadi et al. [35] implementation of structure shown in Fig. 3.12.

CHAPTER 4 – Proposed Structure

As discussed in chapter 3, all of the conventional potentiostat structures have stability issues and need to employ a compensation technique for improving the stability. In this chapter the conventional structures are analyzed to find the main sources of instability. Then a modification to the conventional configuration that does not require any additional complexity is presented. The power consumption in the new modified structure is decreased up to seven times in comparison with the design introduced in [35]. This chapter contains a mathematical analysis for the position of poles and zeros in the proposed and the conventional structures. Using these equations, a modification to this configuration has been obtained and a new subthreshold opamp based on the modified circuit requirements is presented.

4.1. Analysis of the Conventional Design

The AC equivalent of a simple potentiostat shown in Fig. 3.11 is shown in Fig. 4. 1, here the solution module is replaced from Fig. 3. 2. In this model, C_{WE} is 1µF, C_{RE} is 1nF, R_{S1} and R_{S2} are 10Ω while R_{RE} is 1kΩ and R_{WE} is changing from 300kΩ to 10MΩ based on the solution concentration. In Fig. 4. 1, R_{S1} and R_{S2} which are negligible in comparison with R_{WE} and R_{CE} are neglected to simplify the equations. In addition, the amplifier is assumed to be a simple single-pole structure with the open loop gain of A_0 and a single pole located at P_A. Based on equations shown in Appendix-A the transfer function can be derived to be:

$$\frac{V_{out}}{V_{in}} = \frac{-g_{ma}A_0}{1+{}^{S}/_{P_A}} \cdot \frac{(1+R_{CE}C_{CE}S)}{(1+g_{ma}R_{CE}+R_{CE}C_{CE}S)\left(\frac{1+g_{ma}}{1+g_{ma}R_{CE}}+C_{WE}S\right)} \tag{4.1}$$

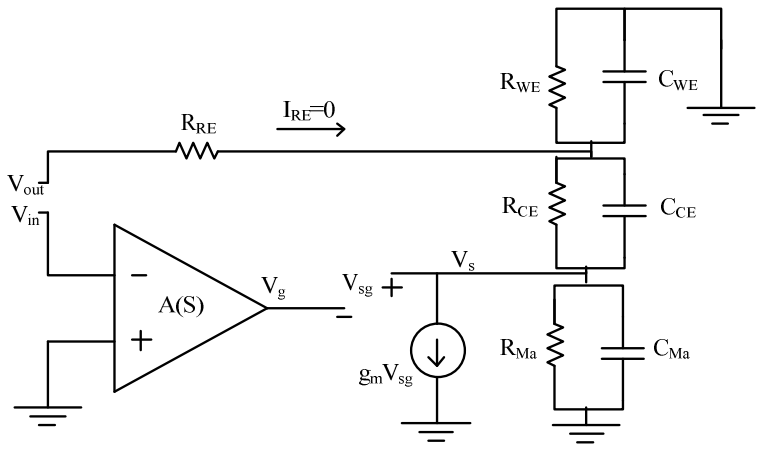


Fig. 4. 1. Schematic of the AC equivalent circuit of a potentiostat.

Based on equation above, this transfer function has one zero and three poles which are located at:

$$Z_1 = -\frac{1}{R_{CE}C_{CE}} \tag{4.2}$$

$$P_1 = -\frac{1}{C_{WE}\left(\frac{(R_{WE}||R_{Ma})(1+g_{ma}R_{CE})}{1+g_{ma}(R_{WE}||R_{Ma})}\right)} \tag{4.3}$$

$$P_2 = -P_A = -\frac{1}{R_{out}C_{out}} \tag{4.4}$$

$$P_3 = -\frac{1+g_{ma}R_{CE}}{R_{CE}C_{CE}} \tag{4.5}$$

From these equations, if $g_{ma}R_{CE}$ be designed to have a very small value, then Z_1 and P_3 can cancel each other. By considering this assumption the equation (4.1) can be further simplified as shown below:

$$\frac{\mathrm{V_{out}}}{\mathrm{V_{in}}} = \frac{-g_{ma}\mathrm{A_0}}{1+{}^{\mathrm{S}}/_{\mathrm{P_A}}} \cdot \frac{(R_{WE}||R_{Ma})}{(1+g_{ma}(R_{WE}||R_{Ma})+(R_{WE}||R_{Ma})C_{WE}S)} \tag{4.6}$$

The transfer function represented by equation (4.6) has two poles which are located at:

$$P_1 = -\frac{1}{C_{WE}((R_{WE}||R_{Ma})||(1/g_{ma}))} \cong \frac{-g_{ma}}{C_{WE}} \tag{4.7}$$

$$P_2 = -P_A = -\frac{1}{R_{out}C_{out}} \tag{4.8}$$

From equations (4.7) and (4.8) it can be concluded that the dominant pole is generated by C_{WE} and $1/g_{ma}$, where the value of $1/g_{ma}$ varies depending on the sensor current. This fact makes the first dominant pole a variable one while the second pole is the opamp pole and is not affected by the sensor current. Therefore for stability of this structure the opamp pole must be pushed to higher frequencies. This requires lower output resistance, R_{out}, which leads to lower opamp open loop gain (A_0). The size of M_a also needs to be reduced to decrease g_{ma} and push P_1 to lower frequencies. From equation (4.6), the open loop gain can be calculated to be:

$$A_{OL} = \frac{-g_{ma}A_0(R_{WE}||R_{Ma})}{1+g_{ma}(R_{WE}||R_{Ma})} \tag{4.9}$$

From the above equation it can be seen that decreasing both g_{ma} and A_0 decreases the open loop gain. Low open loop gain can lead to high offset and low accuracy.

4.2. Proposed Structure

From the above discussion, it can be concluded that it is difficult to achieve both high open loop gain and stability in the conventional structure at the same time. To solve this problem, transistor M_a is replaced by an NMOS shown in Fig. 4.2 [60]. In this new structure it is expected that the first pole located at the output node of the system moves to $1/C_{WE}R_{Ma}$ which is a non-variable, more-dominant first pole.

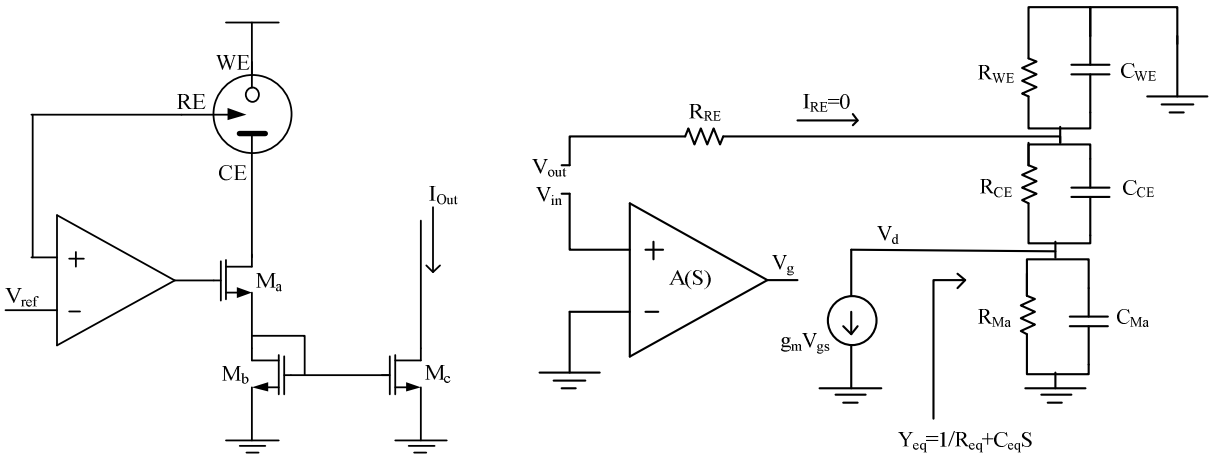
The proposed structure looks like a two-stage amplifier without any compensation capacitor. With respect to the analysis in Appendix-B the system transfer function of the modified design can derived to be:

$$\frac{\mathrm{V_{out}}}{\mathrm{V_{in}}} = -\frac{g_{ma}(R_{WE}||R_{Ma})\mathrm{A_0}}{1+{}^{S}/_{\mathrm{P_A}}} \cdot \frac{(R_{WE}||R_{Ma})}{(1+(R_{WE}||R_{Ma})C_{WE}s)} \tag{4.10}$$

Therefore in this structure the position of poles moves to:

$$P_1 = -\frac{1}{(R_{WE}||R_{Ma})C_{WE}} \tag{4.11}$$

$$P_2 = -P_A = -\frac{1}{R_{out}C_{out}} \tag{4.12}$$



(a) (b)

Fig. 4. 2. a) Proposed structure. b) AC equivalent circuit for calculating the open loop transfer function of the system.

In addition, from equation (4.10), the open loop gain can be calculated to be:

$$A_{OL} = -g_{ma}\mathrm{A_0}.(R_{WE}||R_{Ma}) \tag{4.13}$$

From equations (4.11) and (4.12), it is evident that in this structure there is no need to decrease the g_{ma} in order to separate the poles. In fact, R_{out} can be decreased to increase P_2 while keeping the same A_{OL} by increasing the g_{ma}.

4.2.1. Stability Analysis using Miller Capacitor

The effect of Miller compensation capacitor has been studied in [61]. Adding a compensation capacitor between two nodes represented by equivalent resistors and capacitors of R_1, C_1 and R_2, C_2 and a transconductance amplification of g_m from node 1 to node 2, result in changing the pole positions to the new locations as shown below:

$$P_1(new) \cong -\frac{1}{R_1(C_z(g_m R_2)+C_1)} \tag{4.14}$$

$$P_2(new) \cong -\frac{g_m}{C_1+C_2} \tag{4.15}$$

In the proposed potentiostat, node 2 can be the output node and the node 1 can be the output of the amplifier. Therefore C_2, the solution capacitor, is 1µF which is typically 10^7 times larger than the maximum capacitance at node 1 (0.1pF). Based on these equations, addition of a compensation capacitor moves the new second pole located at node 1 to lower frequencies while the change in the position of the first pole is negligible. Therefore in this structure the new positions of the poles intensely degrade the stability.

The next important point based on [61] is that the compensation capacitor, C_z generates a right half plane (RHP) zero which also degrades the stability. In order to move this zero to left half plane (LHP) a series resistor should be added next to the compensation capacitor.

Therefore to improve the stability in this structure Miller compensation technique cannot be effective since it degrades the stability and the only way to maintain the stability without adding any

compensation technique is to design the opamp pole far away from the first pole. In the next section a new subthreshold opamp is proposed that can achieve both low power dissipation and the required high-frequency pole.

4.2.2. Proposed Opamp for the Proposed Structure

To design the amplifier two stability factors need to be taken in to account: the open loop gain and the position of the first and the second poles. As illustrated in Fig. 4.3 in a system with a fixed position of the first pole (like the potentiostat system), the unity gain bandwidth (UGBW) can be increased by increasing the open loop gain. But the higher open loop gain results in reduction in the PM. Therefore while the open loop gain should not go higher than the required value, it still needs to be high enough to meet the required accuracy.

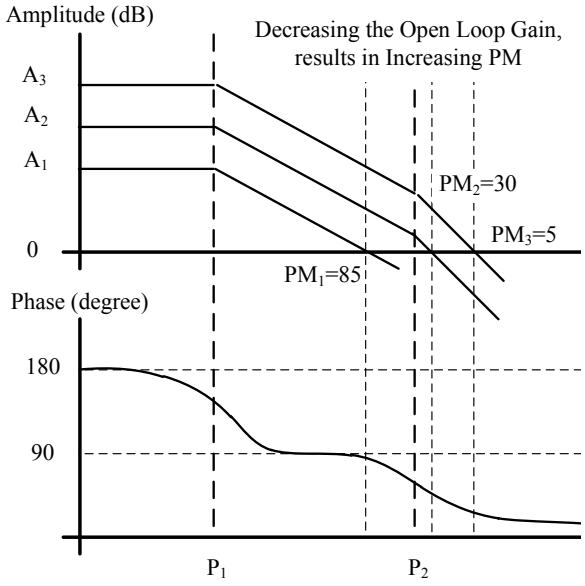


Fig. 4.3. The bode plot of an imaginary system with the fixed position of poles but variable gain. This figure illustrates the fact that in this system, higher open loop gain results in lower stability or phase margin.

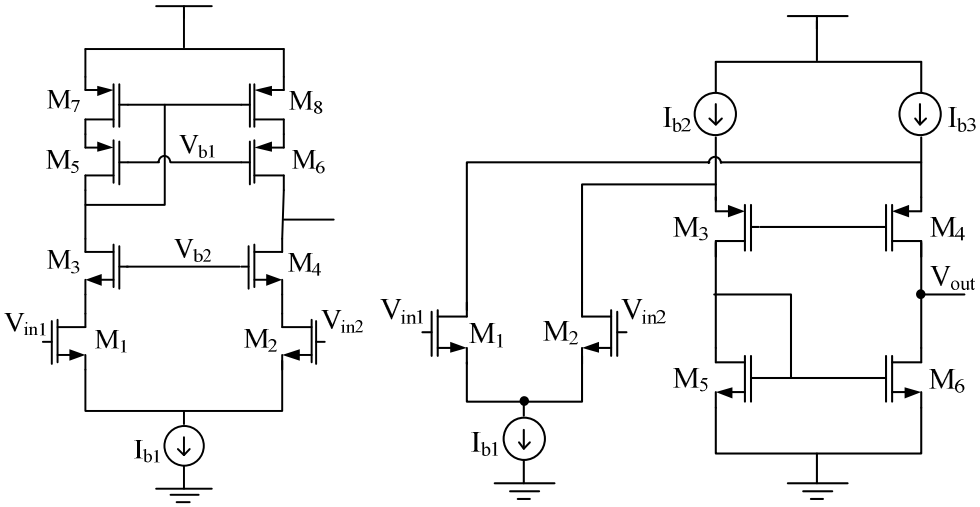


Fig. 4. 4. Schematic of : a) Telescopic amplifier structure, b) Folded cascode amplifier structure.

To design a low-power opamp, a telescopic opamp topology as shown in Fig. 4.4(a) is chosen for the start. To decrease the power consumption and to achieve the maximum efficiency in this amplifier, the input transistors are biased in subthreshold regime to provide the maximum g_m/I_D efficiency. Under this condition, g_m is proportional to I_D and can be measured from the equation below:

$$g_{mi} = g_m(input\ transistors) = \frac{I_D}{U_T} \tag{4.16}$$

Having the input transistors biased in subthreshold regime can also help decrease the flicker noise. The output resistor can be calculated from the equation below:

$$R_{out} = g_m r_o^2 \tag{4.17}$$

Therefore in telescopic transconductance amplifier the input and the output transistors share the same current and the gain can be calculated to be:

$$gain = g_{mi}R_{out} = g_m^2 r_o^2 = \left(\frac{I_D}{U_T}.\frac{1}{\lambda I_D}\right)^2 = \left(\frac{1}{\lambda U_T}\right)^2 \quad (4.18)$$

From this equation, it is obvious that the gain cannot be controlled by current and the only factor responsible for controlling the current is λ. Thus the only parameter responsible for increasing the gain is the channel length of the output transistors which increases the total output capacitance as well. Based on equation (4.12), to push the second pole (P_2) to higher frequencies, C_{out} and R_{out} of the amplifier must be minimized. However, increasing the length of the transistors increases both of these values. Therefore for the highest stability the output transistors should be as small as possible and the minimum length should be chosen for the output transistors.

Based on above discussion a telescopic opamp cannot provide the required gain while keeping the second pole far enough from the first pole. Therefore a folded cascode amplifier is chosen as shown in Fig. 4.4(b). In this structure the input and the output transistor currents are different. Then the gain can be controlled by increasing the transconductance (g_{mi}) of the input transistor without any effect on R_{out} or C_{out} of the amplifier. In this case the equation for gain can be calculated to be:

$$gain = g_{mi}R_{out} = \frac{I_{D1}}{U_T} \times \frac{1}{\lambda I_{D6}} = \frac{1}{\lambda U_T} \times \frac{I_{D1}}{I_{D6}} \quad (4.19)$$

The problem of using folded cascode structure with different current bias in its two branches is the need for providing a very accurate current source for I_{b2} and I_{b3}. Based on equation (4.19), to increase the gain in the structure shown in Fig. 4.4(b), I_{D1} must be increased while I_{D6} is kept constant. If I_{D1} is designed to be 10 times higher than I_{D6}, then I_{b2} and I_{b3} need to be biased at 1.1 times of I_{D1}.This accurate ratio may not be achieved during the fabrication. The mismatch between the transistors in the fabrication process may cause up to 20% change in the current compared to the designed values. In order to alleviate this problem in the standard folded cascode design both branches need to be biased with the same value of the current.

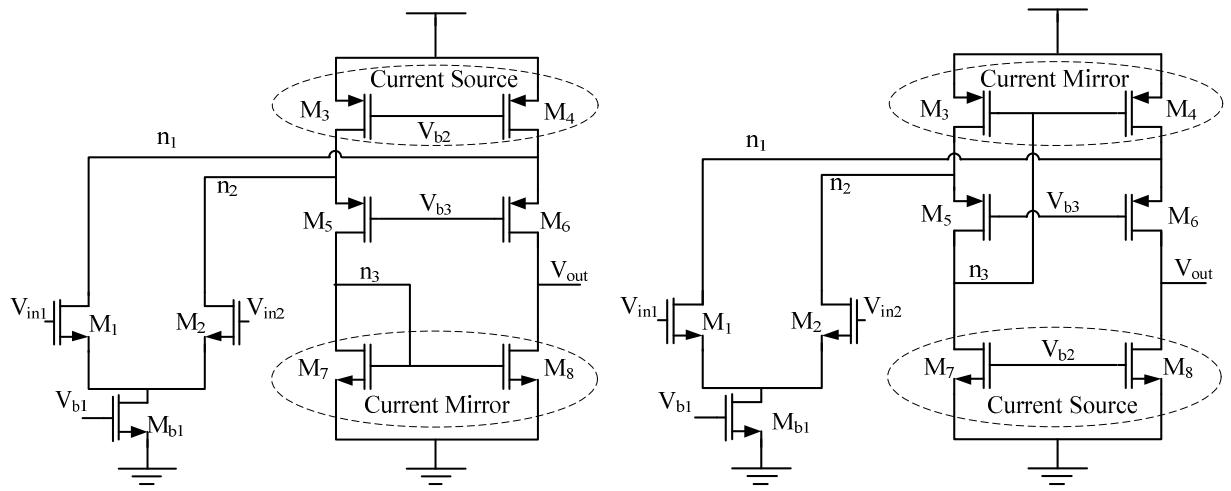


Fig. 4. 5. a) Folded cascode structure. b) Proposed transconductance amplifier by modifying a folded cascode Structure.

Based on the above discussion the folded cascode structure needs to be modified in a way that the accurate current mirror will not be required. Here a modification to the folded cascode structure is proposed that can help solve this issue. Fig. 4.5 demonstrates the applied change to the folded cascode structure. In the proposed structure the location of the current sources is switched by the location of the current mirrors and therefore there is no need for the accurate current mirrors. Based on the calculations in the Appendix-C the position of the poles and the zeros in the modified folded cascode structure can be derived from the transfer function below:

$$\frac{V_{out}}{V_{in}} = \frac{-1/2\left(g_{m1}+C_{gd1}+A_6\left(g_{m3}-C_{gd4}s\right)\right)}{A_1\left(C_{gd1}+C_t s+\frac{1}{r_{ot}}+C_{gd4}s\right)+\left(\frac{1}{r_{o7}}+C_7 s\right)+A_7\left(g_{m3}-C_{gd4}s\right)} \tag{4.20}$$

where the parameters used in this equation is defined in Table. 4.1. From equation (4.20) the DC gain can be calculated as follows:

$$\left.\frac{V_{out}}{V_{in}}\right|_{s=0} = \left(-1/2\right)\left(g_{m1}R_{out} + g_{m1}\left(\frac{1}{g_{m3}}\middle\| R_{out}\right)g_{m3}R_{out}\right) \tag{4.21}$$

Table. 4. 1. Defined Parameters Used in Equation (4.26)

Parameter	Expression
A_1	$\frac{\left(\frac{1}{r_{o7}}+\frac{1}{r_{o5}}+C_6 s+C_7 s\right)}{\left(g_{m5}+\frac{1}{r_{o5}}+C_6 s\right)}$
A_2	$\frac{\left(g_{m5}+\frac{1}{r_{o5}}+C_5 s\right)}{\left[(C_g+C_7)s+\frac{1}{r_{o7}}+\frac{1}{r_{o5}}+C_5 s+C_{gd4} s\right]}$
A_3	$\frac{A_1 C_{gd4} s}{\left[(C_g+C_7)s+\frac{1}{r_{o7}}+\frac{1}{r_{o5}}+C_5 s+C_{gd4} s\right]}$
A_4	$\frac{\left(g_{m1}+C_{gd1}\right)}{\left(C_{gd1}+C_t s+\frac{1}{r_{ot}}+(1-A_2)\left(\frac{1}{r_{o5}}+C_5 s\right)+A_2 g_{m3}+g_{m5}\right)}$
A_5	$\frac{A_3\left(C_5 s+\frac{1}{r_{o5}}-g_{m3}\right)}{\left(C_{gd1}+C_t s+\frac{1}{r_{ot}}+(1-A_2)\left(\frac{1}{r_{o5}}+C_5 s\right)+A_2 g_{m3}+g_{m5}\right)}$
A_6	$A_4 A_2$
A_7	$A_5 A_2 + A_3$
C_t	$C_1 + C_3 = C_2 + C_4 = C_{ds1} + C_{ds3} + C_{sg5}$
C_5	$C_{ds5} + C_{dg3}$
C_6	C_{ds6}
C_7 (C_8)	$C_{ds7} + C_{dg7} + C_{dg5}$
r_{ot}	$r_{o1} \| r_{o3} = r_{o2} \| r_{o4}$
Other assumptions	$r_{o7} = r_{o8}$, $C_{gd1} = C_{gd2}$, $g_{m3} = g_{m4}$, $g_{m5} = g_{m6}$

where

$$R_{out} = \left(g_{m5} r_{ot} (r_{o5} \| r_{o7})\right) || r_{o7} \tag{4.22}$$

From equation (4.21), the paths of the AC signal to the output can be estimated. In this structure there are two different signal paths. First one is the direct path from M_1 to the output and therefore the gain for this path is $g_{m1}R_{out}$. On the other hand the second path is first from M_2 to the node n_3 which is also the gate of

M_4 and then from the gate of M_4 to the output. Therefore the gain of this path is the product of the gain from M_2 to node n_3 which is $g_{m1}\left(\frac{1}{g_{m3}}\middle\| R_{out}\right)$ and the gain from M_4 to the output which is $g_{m3}R_{out}$.

Having two different paths for the AC signal can also be derived from equation (C.24) in Appendix-C. From this equation it can be seen that the two different paths of the AC signal to the output will cause two zeros and two poles that are close to one another. The two extra poles created from this path can be calculated from the equation below:

$$P(s) = \left(\frac{1}{A_2}\left(C_t s + \frac{1}{r_{ot}}\right) + \left(C_g + C_7\right)s + \frac{1}{r_{o7}} + g_{m3}\right) = 0 \tag{4.23}$$

While the extra zeros can be derived from the equation below:

$$z(s) = \left(\frac{1}{A_2}\left(C_t s + \frac{1}{r_{ot}}\right) + \left(C_g + C_7\right)s + \frac{1}{r_{o7}} + g_{m3}\right) + g_{m3} = 0 \tag{4.24}$$

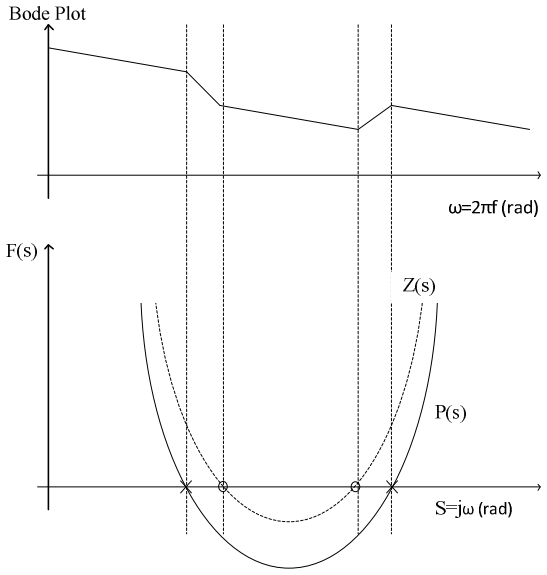


Fig. 4. 6. Bode plots showing that extra poles and zeros created from the different AC signal paths can cause a non-uniform structure in the AC frequency response of the system.

From equations (4.23) and (4.24), the extra poles and zeros are close to each other and therefore can be designed to cancel each other. Fig. 4.6 provides an illustration about the effect of these two poles and two zeros on the ac frequency response of the transimpedance amplifier. In this figure the location of zeros and poles are defined by the intersection of the two polynomials P(s) and Z(s) with the *s*- axis which changes the shape of the Bode plot as illustrated in this figure.

4.3. Design Considerations in the Complete System Structure

Fig. 4.7 shows the complete schematic of the proposed structure. The signal processing unit (SPU) used here is discussed in [56]. According to equation (4.11), increasing the output resistance of the potentiostat will result in pushing the dominant pole to lower frequencies which improves the stability. In order to increase the output resistance the length of transistor M_a is increased. The system output resistance in Fig. 4.6 can be calculated to be:

$$R_{Sout} = \frac{g_{ma} r_{oa}}{g_{mb}} || (R_{CE} + R_{WE}) \tag{4.25}$$

Therefore in this structure the gain can easily be controlled without any effect on the position of the pole by changing the ratio of the current in the first stage to the current in the second stage of the amplifier. This control can even be performed externally. The current mirror transistors in this amplifier should be biased in strong inversion to achieve the lowest capacitance at the output node. Besides, the current matching requirement for the current mirrors can be better achieved by using the transistors biased in strong inversion. Avoiding the cascade structure at the output stage of this amplifier helps the output resistance to stay as low as possible.

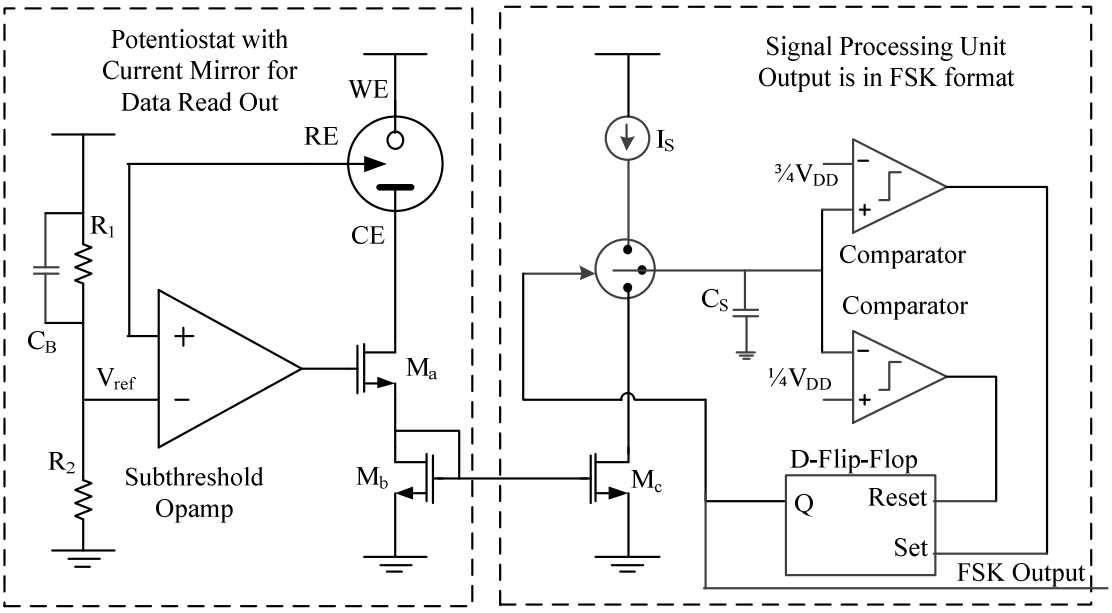


Fig. 4. 7. Schematic of the proposed potentiostat structure.

4.3.1. System Offset

One important parameter that needs to be taken into account is the offset generated between the two inputs of the opamp. This offset can be either the result of mismatch or due to non-symmetric structure. The offset generated by mismatch in this structure can be derived from the equation below:

$$V_{os} = V_{os1} + V_{os7}.\frac{g_{m7}}{g_{m1}} + V_{os3}.\frac{g_{m3}}{g_{m5}g_{m1}} \tag{4.26}$$

where V_{osn} represents the offset between transistor *n* and *n+1* and can be derived from the equation below:

$$V_{osn} = \frac{V_{GSn}-V_{THn}}{2}\left[\frac{\left(\frac{W}{L}\right)_{n+1}-\left(\frac{W}{L}\right)_{n}}{\left(\frac{W}{L}\right)_{n}}\right] - \left(V_{TH(n+1)} - V_{THn}\right) \tag{4.27}$$

In equation (4.27) the V_{TH} and (W/L) variation can be estimated based on process parameters from equations (2.25) and (2.26). Applying layout techniques can help reduce the mismatch offset. The

systematic offset in this structure is caused by having different V_{DS} values for M_7 and M_8. V_{DS7} is designed to be fixed at (V_{DD}-V_{GS3}), while V_{DS8} is changing based on the variation in V_{GS} of transistor M_a due to the variation in the sensor current.

4.3.2. System Noise

Another important parameter to be considered in circuit design is noise. Noise in this system will be filtered by the large capacitor existing in the electrochemical sensor. Based on the calculations and assumptions in Appendix-D the output noise of the potentiostat system can be calculated to be:

$$V_{nOut}^2 = \left[\left(I_{nRE}^2 + I_{nb}^2\right)\frac{g_{mc}}{g_{mb}} + I_{nc}^2 + I_{nRspu}^2\right]R_F \tag{4.28}$$

where

$$I_{nRE}^2 = V_{nRE}^2\frac{(1+R_W C_W s)}{R_W} \quad , \quad I_{nb}^2 = 4KT\gamma g_{ma} \quad , \quad I_{nc}^2 = 4KT\gamma g_{mc} \quad \text{and} \quad I_{nRspu}^2 = \frac{4KT}{R_{SPU}} \tag{4.29}$$

And

$$\overline{V_{nRE}^2} = \overline{V_{n1}^2}\left(\frac{A_0 G_{ma} R_W}{(1+s/P_1)(1+R_W C_W s)-A_0 G_{ma} R_W}\right)^2 + \overline{I_{nW}^2}\left(\frac{R_W(1+s/P_1)}{(1+s/P_1)(1+R_W C_W s)-A_0 G_{ma} R_W}\right)^2 \tag{4.30}$$

$$\overline{V_{n1}^2} = \frac{8KT\gamma(g_{m2}+g_{m4}+g_{m8})R_{Out}^2}{(g_{m2}R_{Out})^2} = \frac{8KT\gamma}{g_{m2}}\left(1+\frac{g_{m4}}{g_{m2}}+\frac{g_{m8}}{g_{m2}}\right) \tag{4.31}$$

$$G_{ma} = \frac{g_{ma}}{1+g_{ma}(\frac{1}{g_{mb}})} \qquad \text{and} \qquad I_{nW} = \frac{4KT}{R_{nW}} \tag{4.32}$$

4.3.3. System Power Supply Rejection Ratio (PSRR)

The last important parameter that needs to be analyzed is the effect of noise on the power supply known as power supply rejection ratio (PSRR). From the structure shown in Fig. 4.7, C_{WE} is a 1µF

capacitor that guides the noise from power supply to one input port of the opamp, while the resistor divider in the other input port of the opamp divides the noise by its ratio and provides a lower value of noise at this input port of the opamp. This will cause opamp to amplify the difference noise applied to the input ports of the opamp. This phenomenon can cause the presence of very large noise signal at the output of the opamp and at the mirror of the sensor current (current at M_c). This problem can be seen only in power supply low-frequency noise. In higher frequencies the gain of the opamp drops very fast that helps eliminate the high-frequency noise at the output of the opamp and the mirrored current. The power supply is mostly generated by accumulating high frequency signal through optical or inductive coupling and therefore the noise existing in the power supply would be the same high-frequency noise and will be eliminated. In this design a low drop out regulator (LDO) has been also used to eliminate any low-frequency noise that might appear in the system. If possible, putting a large capacitor of C_B can help provide the same value of noise to the inputs of the opamp and therefore reduce the effect of the low-frequency noise at the output.

CHAPTER 5 – Signal Processing Unit (SPU)

In this chapter a new signal-processing unit (SPU) for implantable biomedical sensors is proposed. The proposed scheme combines the advantages of the two main structures of conventional SPUs discussed in chapter 3 (delta-sigma modulator and charging capacitor in feedback). The preliminary design has been realized in a 0.35µm CMOS process. Test results validate the desired functionality of the system. In the following sections an additional modification to the SPU is proposed to facilitate simple frequency modulation. Simulation results in the same process confirm the linearity of the system corresponding to a wide range of sensor current.

5.1. Introduction

Combination of a potentiostat and a signal-processing unit (SPU) is a common approach for monitoring various human physiological parameters such as glucose, lactose, pH etc as it was discussed in chapter 3. The SPU unit has been realized in a number of different methods, which can all be categorized in two different main groups. The first group uses a capacitor in the path of the input current and measures the time that is required for the capacitor to charge to a specific voltage level [1-4]. The second group of SPU structures uses a delta-sigma analog-to-digital converter (ADC) [5-6]. The advantages of the first group include their relatively simple circuit topologies and the output signal frequency being proportional to the sensor current. However, these SPUs typically suffer from low accuracy, which makes them unsuitable for measuring small currents. On the other hand, the delta-sigma modulator has more complex structure and the output signal is a high frequency digital code that requires a low-pass filter (LPF) for decoding. In delta-sigma structures the error between the original and the modulated signals is added to the input signal in the next cycle. This method compensates for the error

and reduces the effect of random noise. In other words in a delta-sigma structure noise is shaped and is moved to higher frequencies. The simplest bipolar delta-sigma structure is a one-bit structure that needs to generate a "+1" and a "-1" current with exactly equal absolute values. In this chapter a simple SPU structure is presented that has the accuracy of the delta-sigma modulator and the simplicity of the charging capacitor. The proposed technique increases the reading range and the accuracy of the current measurement.

5.2. Proposed Structure

Based on the requirement of low power dissipation in biomedical implantable applications, a unipolar continuous time first order delta-sigma structure is proposed that achieves the measurement accuracy of a delta-sigma modulator while in comparison has a simpler structure and does not require the implementation of sink and source currents with the exact absolute values. The proposed technique saves the difference error and introduces it in the next cycle which is the technique used in delta-sigma modulators for achieving high accuracy.

To explain the idea, first the input current is represented as a multiple of an integer with a small magnitude. The value of this current defines the accuracy of the system. For example, for a system with required accuracy of 10nA, a current of 1.2μA can be represented by (120).(10nA) and 1.21μA can be represented by (121).(10nA). These integer numbers can be generated by a capacitance, which is charged by the input current for the time duration of (*T*) and discharged with the 10nA current for the time duration of (*nT*). In this case "*n*" is the output of this system. For this capacitor:

$$V = \frac{1}{C}\int_0^T I_s dt = \frac{I_s T}{C} = \frac{1}{C}\int_0^{nT} I_B dt = \frac{I_B nT}{C} \rightarrow I_s = nI_B \tag{5.1}$$

where, I_B is the 10nA source current and I_S is the input current. A comparator is used to check the voltage across the capacitor. A counter counts the number of discharging cycles starting from the activation time of I_B and ending at its deactivation time.

The problem here is that the generation of a small current of I_B is very difficult. In addition, connecting and disconnecting this small current accurately in presence of many parasitic parameters is a real challenge. To solve this problem, instead of using a very small current (I_B) and measure I_S as nI_B, I_B can be chosen to be a large number and I_S can be introduced as a fraction of I_B. Another option is to choose I_B in the same range as I_S and charge the capacitor with the input current (I_S) for the time duration of nT and discharge it with I_B for the time duration of mT in such a way that the capacitor be completely discharged by the end of the last cycle. In this case, I_S based on I_B can be derived to be:

$$V = \frac{1}{C}\int_0^{nT} I_s dt = \frac{nI_sT}{C} = \frac{1}{C}\int_0^{mT} I_B dt = \frac{I_B mT}{C} \tag{5.2}$$

$$\rightarrow\ I_s = \frac{m}{n} I_B = m\left(\frac{I_B}{n}\right)$$

This structure can be implemented using the configuration shown in Fig. 5.1. Therefore I_S can be calculated as any ratio of I_B or as before a multiple of an integer by small value (I_B/n). Therefore in this case the accuracy can be defined by I_B/n. Therefore, regardless of the value of I_B any accuracy can be achieved just by increasing the measurement time.

The output signal of this structure is very similar to the output of a one-bit delta sigma structure. The only difference is that the “ones” and the “zeros” do not represent the same absolute value of the current. In the next section an additional modification is applied to the structure that can convert the output digital codes so that they can be easily decoded.

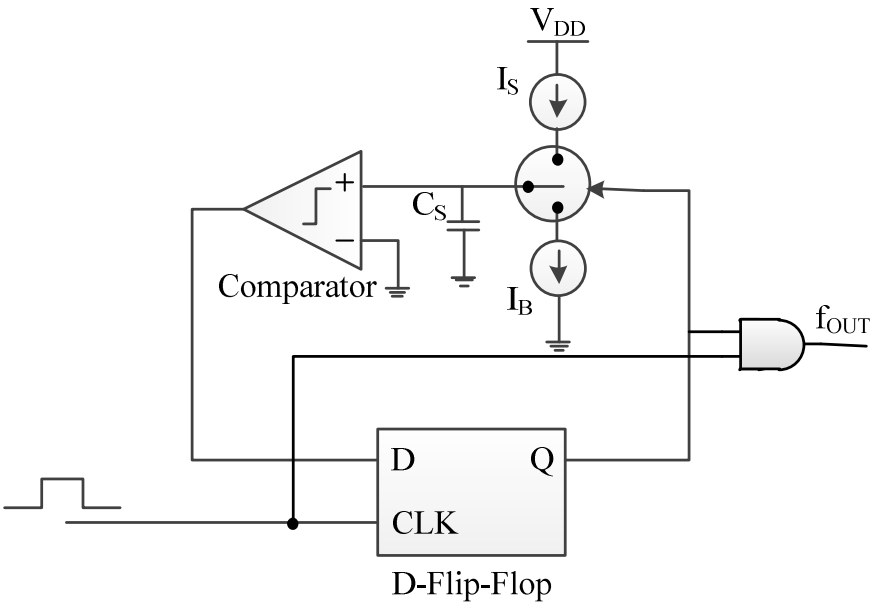


Fig. 5. 1. Schematic of the proposed SPU structure.

5.3. Demodulation Scheme

The output signal of the proposed structure can be demodulated using a counter. In this design, for any time interval of $(n+m)T$, there exist "n" ones and "m" zeros and therefore a counter can be used for demodulation. One solution is to use an additional counter to keep the track of the time and in each $(n+m)T$ the first counter is reset while the output data of the counter is stored in memory before each reset. To further simplify the demodulation scheme a method is developed which allows the output signal of the delta-sigma modulator to be directly demodulated just by using one counter. If a counter is used as a demodulator before the output, the frequency of the most significant bit (MSB) of the counter is proportional to the input current. This is because in each period of $(n+m)T$, the counter counts to n and for a b-bit counter, the frequency of MSB would be:

$$f_{MSB} = \frac{n}{n+m} \cdot \frac{1}{2^b} \cdot \frac{1}{T} \tag{5.3}$$

The problem with this simple method is that each cycle of counting can be started and ended at any time. Therefore the assumption that the charged voltage in capacitor is equal to its discharged value is not always correct. This will cause frequency fluctuation for the MSB output signal around the frequency calculated by equation (5.3). To solve this problem it is required to stop counting when the capacitor voltage is equal to its value at the beginning of the counting cycle. By choosing I_B to be at least three times larger than the maximum I_S, it can be assured that when the capacitor is charged by I_B it takes more than two cycles of I_S to discharge it. Thus for the duration of charging the voltage across the capacitor is slightly lower than the reference voltage of the comparator. Therefore each charging cycle generates a "one" which always follows a "zero" and the next signal after this "one" there is also always a "zero". Therefore counting always starts and ends at the time when "one" occurs which in this case represents almost the same value of the voltage across the capacitor. This can remove the output frequency fluctuation

For improving the accuracy further, the current I_S will never be turned off. This change can help reduce the parasitic effects resulting from the continuous connecting and disconnecting of I_B. Therefore the Fig. 5.1 can be modified to result in the structure shown in Fig. 5.2. Therefore here I_B - I_S is chosen to be three times larger than I_S or equivalently I_B is chosen to be $4I_S$.

In this system the number of bits in counter can be chosen based on the required accuracy. In a *b*-bit counter, when the counter counts to 2^b, the MSB signal changes its value twice. The MSB frequency is inversely proportional to this time interval ($f_{MSB} = 1/T_{MSB}$). Based on the previous discussion, during this time the capacitor has been charged with I_S during the entire time interval of $T_{MSB} = (n+m)T_{CLK}$ and has been discharged with I_B for the time nT_{CLK}, where T_{CLK} is the clock period. Based on the assumption that the voltage across the capacitor is almost constant at the beginning and at the end of each counting:

$$I_s(n+m) = I_B n \tag{4}$$

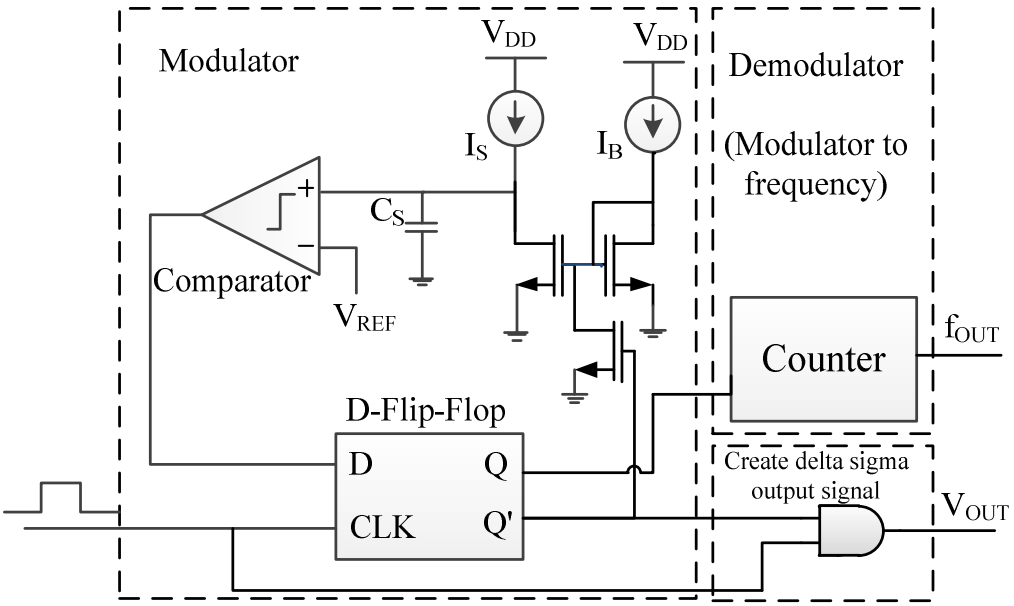


Fig. 5. 2. Schematic of the modified SPU structure.

Therefore:

$$m = n\left(\frac{I_B}{I_S} - 1\right) \tag{5.5}$$

From equation (5.5), T_{MSB} can be derived to be:

$$T_{MSB} = T_{CLK}(n+m) = nT_{CLK}\left(\frac{I_B}{I_S}\right) \tag{5.6}$$

Therefore the MSB frequency can be derived to be:

$$f_{MSB} = \frac{1}{T_{MSB}} = \frac{I_S}{nT_{CLK}I_B} = \frac{I_S}{2^b T_{CLK} I_B} \tag{5.7}$$

From equation (5.7), the frequency of the MSB is directly proportional to the input current. The accuracy of equation (5.7) is based on the accuracy of the equation (5.5). In this equation *m* and *n* are two integer

values and for a non-integer values of I_B/I_S, m would be equal to the integer part of $n(I_B/I_S - 1)$ which is more accurate for larger values of n or equivalently higher values of counter bits (b).

CHAPTER 6 – Simulation and Test Results

This chapter contains a summary of simulation and test results for the proposed opamp and potentiostat shown in Fig. 4.5(b), Fig. 4.2(a) and Fig. 4.7 fabricated in a 0.5 µm CMOS process and also simulation and test results for the proposed signal processing unit shown in Fig. 5.1 fabricated in a 0.35 µm CMOS process.

6.1. Opamp Simulation Result

In this part, the proposed opamp simulation results based on a 0.5µm CMOS process simulator is presented. A summary of the transistor sizing for this opamp shown in Fig. 4.5(b) and their bias currents are provided in Table. 6.1.

Table. 6. 1. Transistor Sizing and Bias Current for Folded Cascode Amplifier Shown in Fig. 4.5(b).

	M_1	M_2	M_3	M_4	M_5	M_6	M_{b1}	M_7	M_8
W (µm)	51	51	15	15	9	9	1.5	1.5	1.5
L (µm)	.6	.6	.6	.6	.6	.6	.6	2.4	2.4
Mult.	10	10	2	2	2	2	2	4	4
I_{bias}(µA)	0.9	0.9	1	1	.13	.13	1.7	.13	.13

6.1.1. Position of Poles and Zeros of the Proposed Opamp

Fig. 6.1 shows the simulation results for the Bode plot of the proposed opamp with different sizes of $M_{1\text{-}2}$ transistors. As evident from Fig. 6.1, the larger size of transistors $M_{1\text{-}2}$ can help reduce the effect of extra poles and zeros on the AC transfer function. The large sizes of transistors M_{12} have also a great

impact on the position of the first pole. Fig. 6.2 shows the effect of the control parameter (size of $M_{1\text{-}2}$) on the change in the position of poles in the proposed opamp). Based on the system design requirements the size of $M_{1\text{-}2}$ can be designed. Here, because the first pole of the opamp is the second pole of the system and the position of second and third pole does not affect the performance of the system, the smaller size of $M_{1\text{-}2}$ for achieving the highest position of the first pole is desirable.

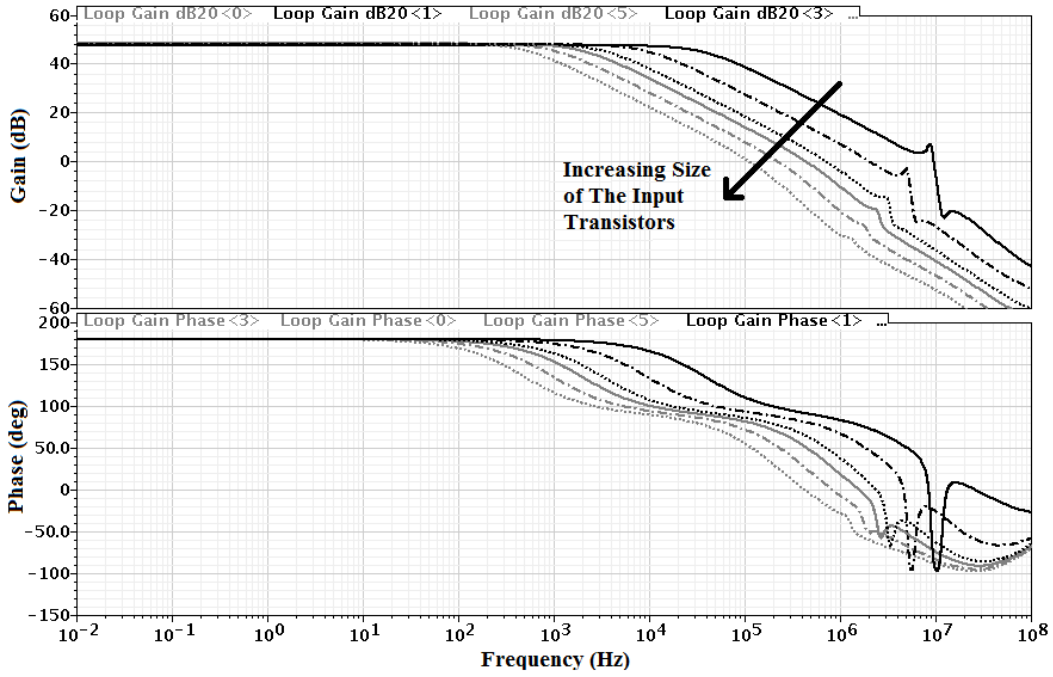


Fig. 6. 1. Bode plot of the proposed opamp with different sizes of $M_{1\text{-}2}$ transistors.

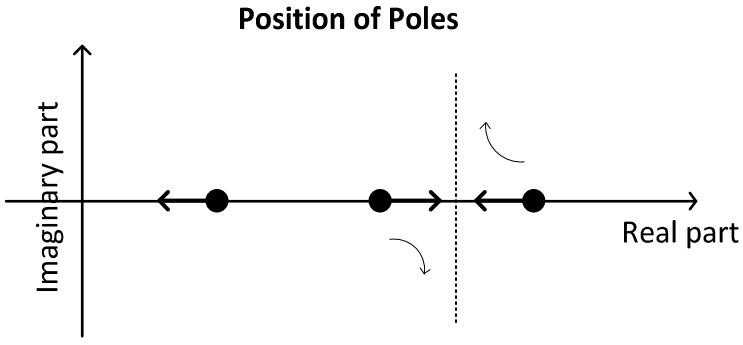


Fig. 6. 2. Change in position of poles with changing the sizes of transistors $M_{1\text{-}2}$.

Fig. 6.3 shows the simulation result for AC frequency response of the proposed folded cascode structure in comparison with the conventional folded cascode structure. From this figure the position of poles and zeros can be compared. Fig. 6.3 compares the proposed folded cascode with two different biasing of the conventional folded cascode structure. The first one is biased the same way as the proposed opamp and therefore as it is expected that both have the same first pole but different second poles. The second one has the same value of current in both branches. Therefore this folded cascode has lower gain but higher value of the first pole.

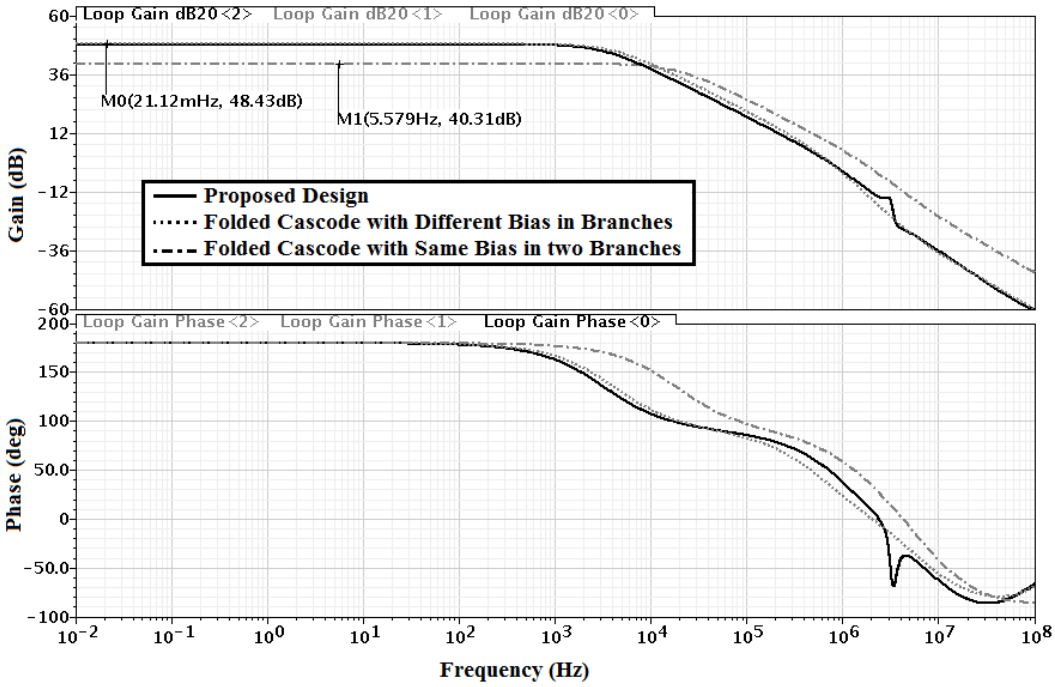


Fig. 6. 3. Comparison between the AC frequency response of the proposed folded cascode structure and the conventional folded cascode structure.

6.1.2. Noise Performance of the Proposed Opamp

Fig. 6.4 shows the simulation result for the output noise of the proposed opamp in unity feedback and in comparison with the conventional folded cascode opamp. As before in this figure, the proposed

opamp is compared with two different biasing conditions of the conventional folded cascode opamp. The input referred noise can be calculated by dividing the output noise with the gain of the amplifier. As evident from Fig. 6.4, the folded cascode opamp with the same biasing as the proposed opamp has almost the same value of the output noise. In addition, since these opamps have almost the same values of gain, the input referred noise for theses would almost be the same. However, the folded cascode opamp with higher value of current in the output branch has a higher output noise and lower gain which results in higher input referred noise.

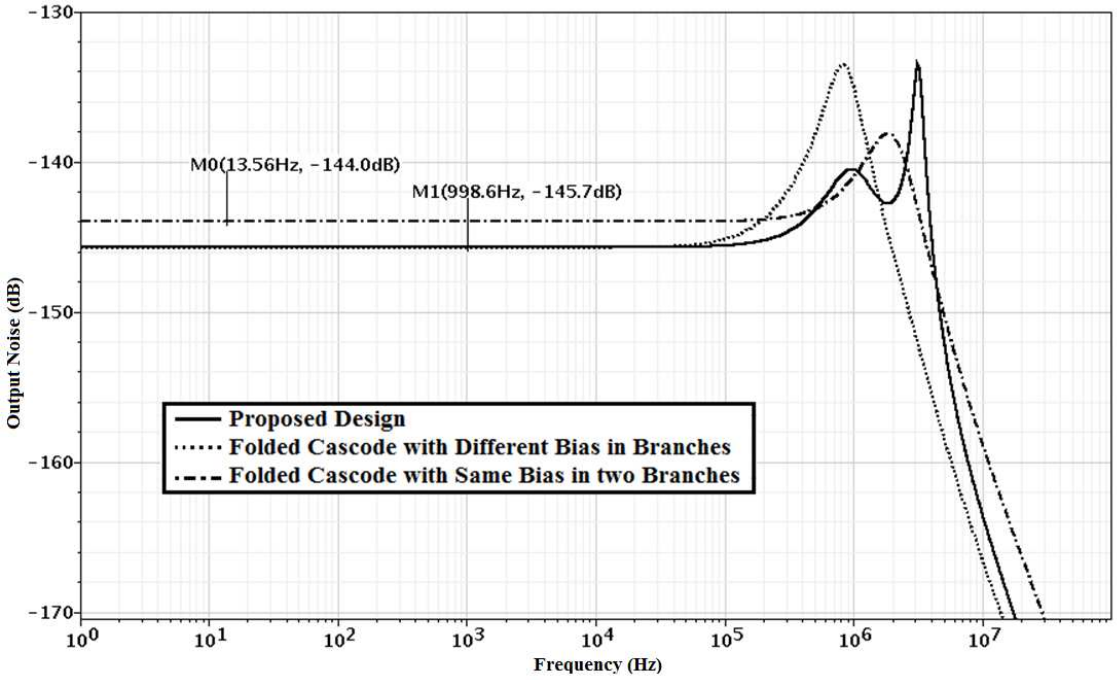


Fig. 6. 4. Noise performance comparison between the proposed opamp and the conventional folded cascode opamp.

6.1.3. Common Mode Rejection Ratio (CMRR) of the Proposed Opamp

CMRR is defined to be the differential-mode gain divided by the common-mode gain. Fig. 6.5 shows the simulation results of the common-mode gain for the proposed opamp in comparison with two different biasing condition of the conventional folded cascode opamp. It is evident from this figure that the proposed opamp provides a better rejection for the common mode signal. The reason for that can be

the more sharing of the paths for the two input signals from the differential input to the output. From Fig. 6.3 and Fig. 6.5, the CMRR values can be calculated as below:

Proposed opamp: 40.42dB + 48dB = 88.42dB,

Conventional folded cascode with different bias in branches: 24.47dB + 48dB = 72.47,

Conventional folded cascode with the same bias in branches: 35.8dB + 40.31dB = 76.11.

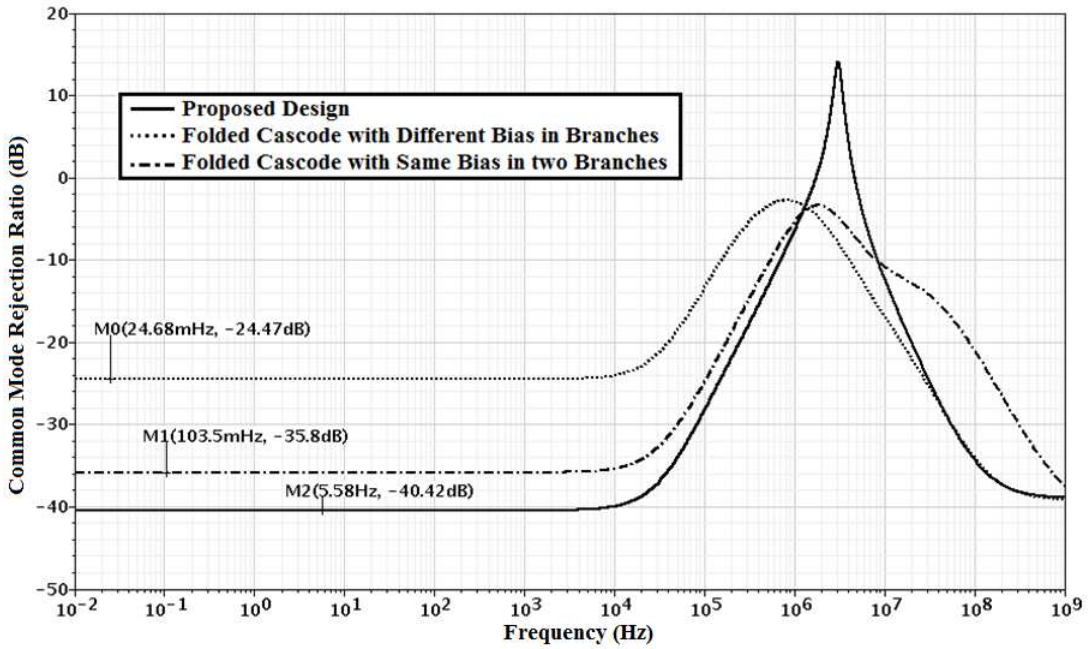


Fig. 6. 5. Comparison of CMRR result for the proposed opamp with the conventional folded cascode opamp.

6.1.4. Power Supply Rejection Ratio (PSRR) of the Proposed Opamp

Fig. 6.6 shows the PSRR simulation results for the proposed opamp in comparison with two different biasing condition of the conventional folded cascode opamp. It is evident from this figure that the proposed opamp provides a worse performance in power supply rejection in comparison with the conventional design. The reason for that is the extra path of noise from the power supply through the current mirror. Therefore this structure shows a better power supply rejection performance when a folded cascode with PMOS input transistors is needed.

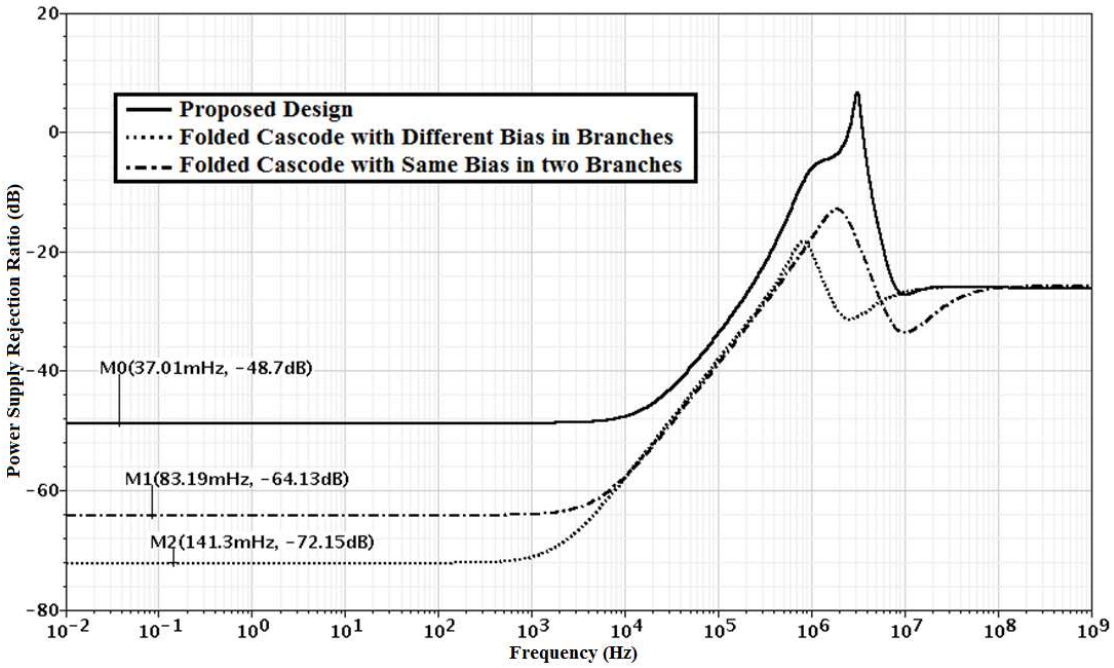


Fig. 6. 6. Comparison of PSRR result for the proposed opamp with the conventional folded cascode opamp.

6.2. Potentiostat Simulation and Test Result

In this section the simulation and the test results for the potentiostat block are presented. In addition, the test result for the entire system shown in Fig. 4.7 for four different chips fabricated in a 0.5µm CMOS process are presented.

6.2.1. Simulation Result for Open Loop Gain and Phase Margin

The system shown in Fig. 4.7 has been simulated in a 0.5µm CMOS process for three different values of the capacitor and the resistor of the chemical solution model shown in Fig. 3.2. Fig. 6.7 shows the simulation results for these three conditions. The value of the R_{WE} changes with the solution concentration and the value of C_{WE} can change from sensor to sensor. Due to higher solution resistance for low level of sensor current the second stage gain of the circuit is higher which leads to higher open loop gain. In addition, this high resistor moves the dominant pole to the lower frequency which improves the phase margin. The phase margin values of higher than 70° in all these conditions reflects high stability

performance of this system. The power consumption of the system in any of these three conditions has been summarized in Table. 6.2.

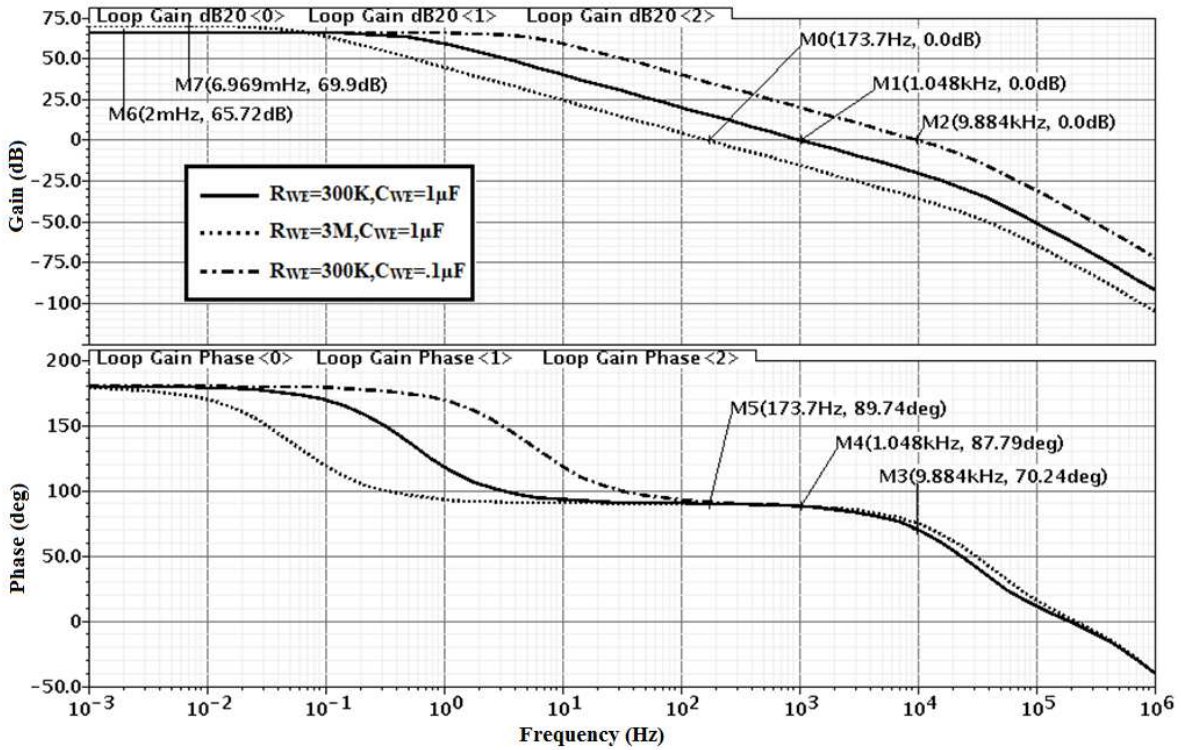


Fig. 6. 7. System stability response for three different solution models.

Table. 6. 2. Summary of Circuit Parameter for V_{DD} =1.8V (It also includes resistive divider power consumption)

	Open Loop Gain	**Phase Margin**	**Power consumption**
R_{WE}=300KΩ C_{WE}=1µF	69.9 dB	87.79º	10.20 µW
R_{WE}=3.6MΩ C_{WE}=1µF	65.72 dB	89.74º	6.44 µW
R_{WE}=300KΩ C_{WE}=0.1µF	69.9 dB	70.24º	10.20 µW

6.2.2. Test Results of the Complete System

The system configuration shown in Fig. 4.7 has been fabricated in a 0.5µm CMOS process. Fig. 6.8 shows the microphotograph of the fabricated chip realized in this process. The bias circuit, the potentiostat and the SPU are marked in this photo. The total area consumption for the entire system is 0.06mm^2 and the potentiostat area (without biasing) is 0.013mm^2. This circuit has been tested by connecting the three electrodes of the electrochemical sensor to the chip while the sensor is floating inside the glucose solution. As shown in Fig. 6.9, the generated sensor current increases with increase in the concentration of the glucose solution. Fig. 6.10 summarizes the experimental results based on the sensor current. The output signal generated form this system is a frequency signal. The output signal frequency is shown in Fig. 6.10. It is evident from this figure that the output frequency linearly increases with increasing levels of the sensor current.

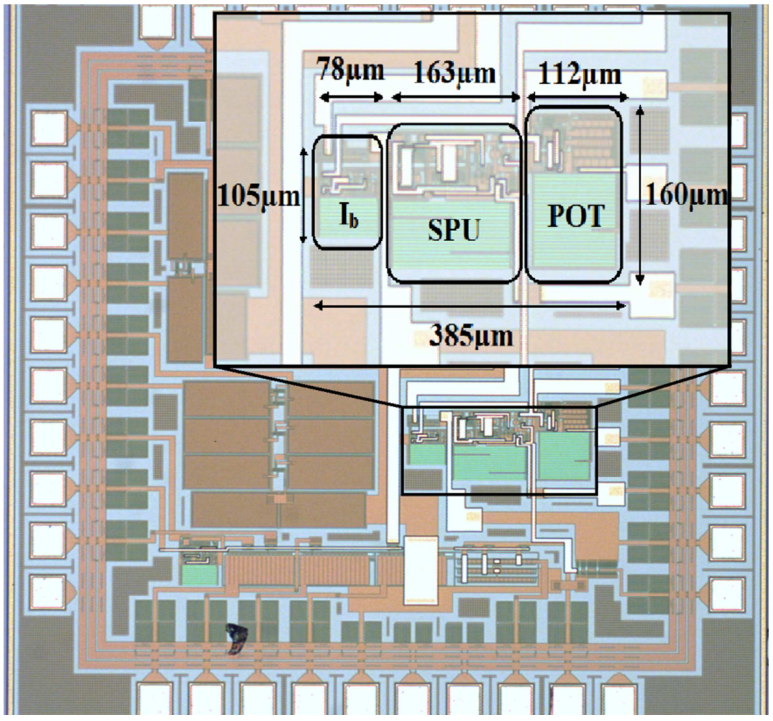


Fig. 6. 8. Chip microphotograph showing various system building blocks.

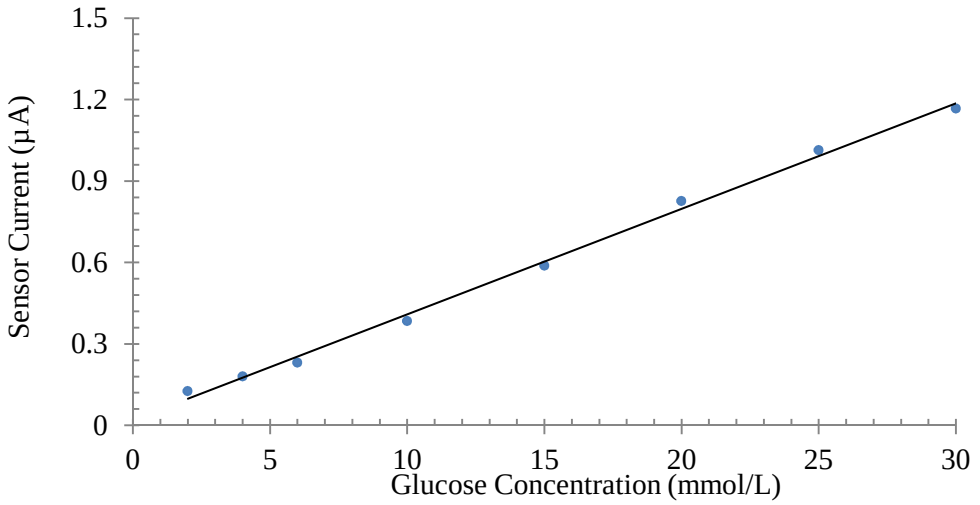


Fig. 6. 9. Sensor current based on glucose concentration in the solution.

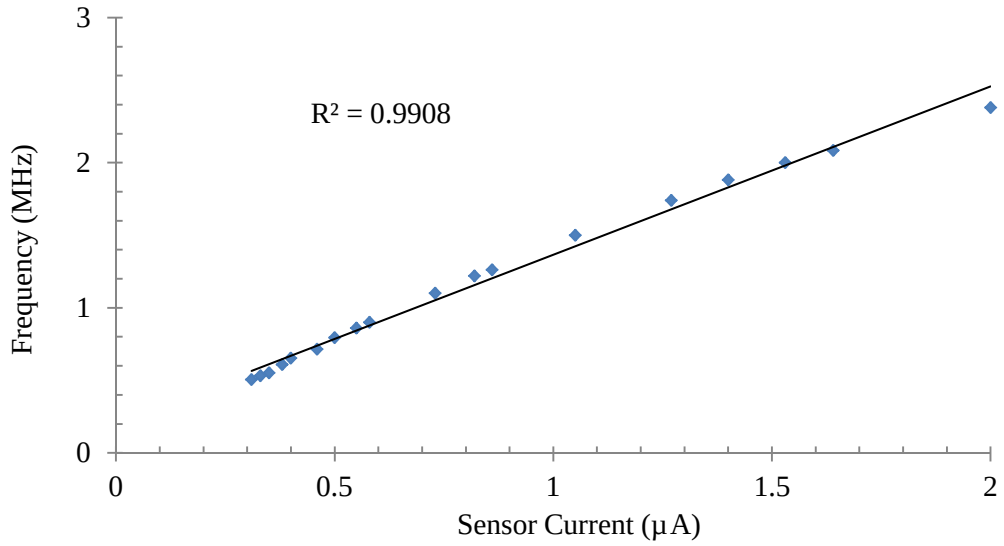


Fig. 6. 10. Measurement results of the output frequency for different values of the sensor current.

Fig. 6.11 shows the same test results presented in Fig. 6.10 for four different chips. Fig. 6.12 compares the test result of four chips in one plot. To see the contribution of potentiostat in the difference between the tests results seen in Fig. 6.12, three separate potentiostats fabricated in different chips are connected to the same SPU and the results are shown in Fig.13. It is evident in this figure that the process variation in potentiostat does not have a significant effect on the system output results.

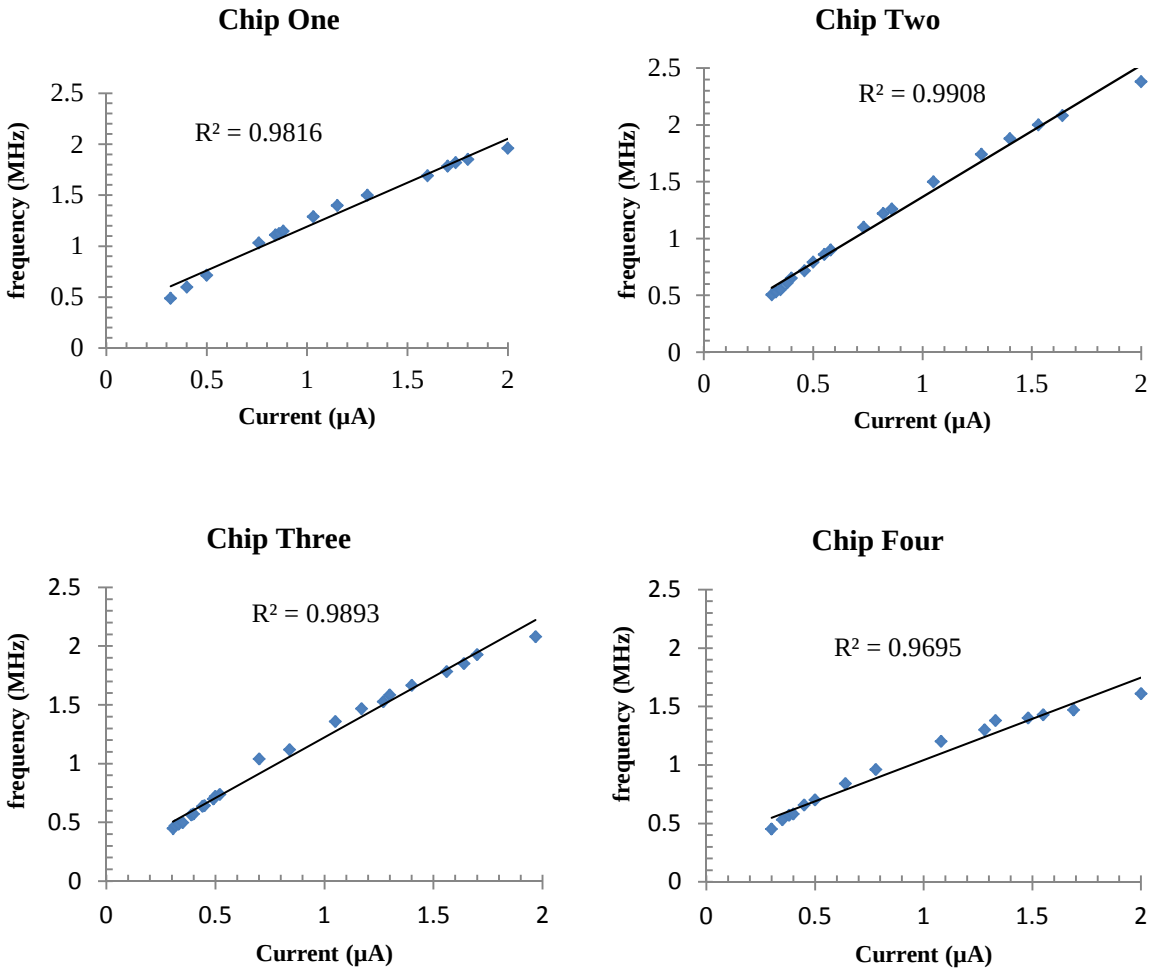


Fig. 6. 11. Chip output frequency result for different values of the sensor current for four different chips.

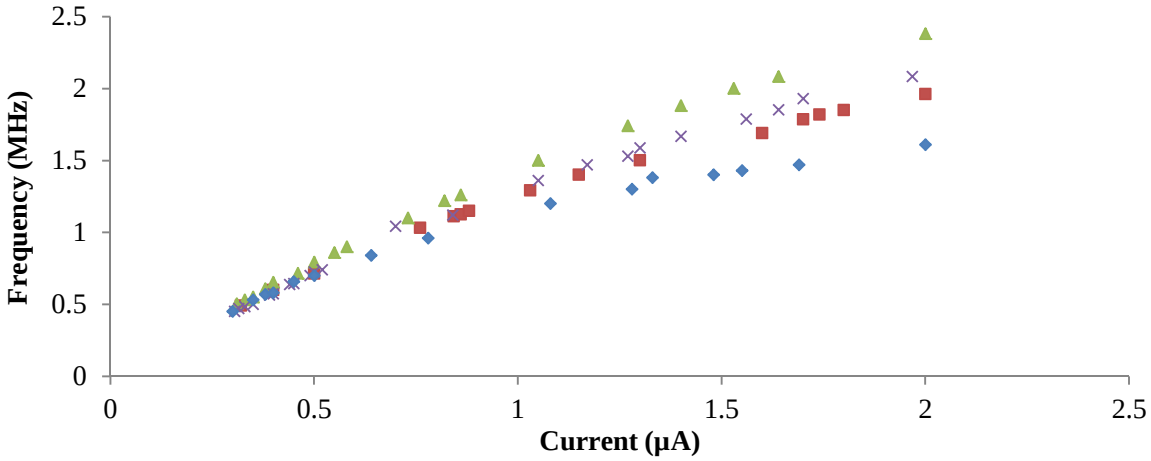


Fig. 6. 12. Comparison between the test results for four chips.

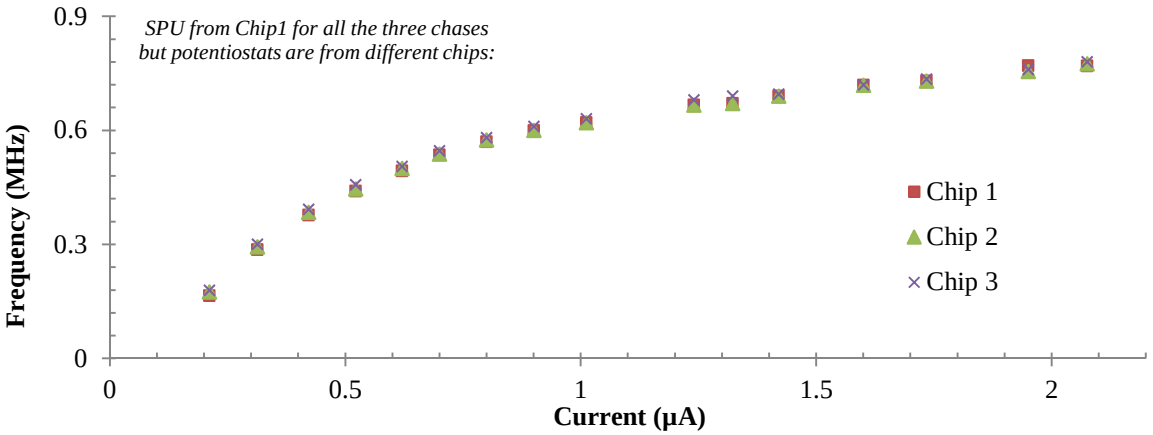


Fig. 6. 13. Effect of the process variation in potentiostat on the system output results.

6.2.3. Offset Simulation and Test Result

In this part the offset between the two input ports of the opamp in the potentiostat structure has been simulated using Monte Carlo process and mismatch simulation. This offset represents the variation of the (V_{WE}-V_{RE}) by process and mismatch variation. The simulation result is shown in Fig. 6.14. This result predicts a maximum mismatch of 30mV.

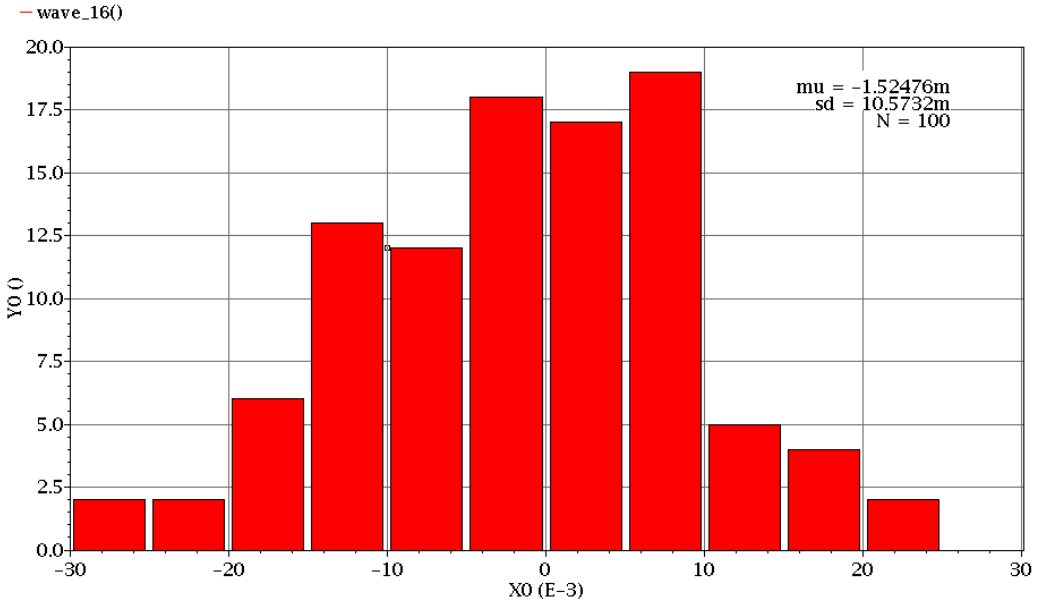


Fig. 6. 14. Offset between two inputs of the opamp in the potentiostat structure which also represents the variation of (V_{WE}-V_{RE}) by process and mismatch variation.

This offset value has also been measured for different values of sensor current. Fig. 6.15 shows the test results for the measured values of offset in three different chips. It is expected for each chip measurement that the offset increases with increase in the sensor current. The systematic offset which is due to the non-symmetric structure of this system and the finite gain of the opamp are the reasons for these variations. It can be seem from Fig. 6.15 that the offset voltage variation for each chip is less than 3.5mV while the offset resulting from the mismatch is changing from -13mV to 19mV.

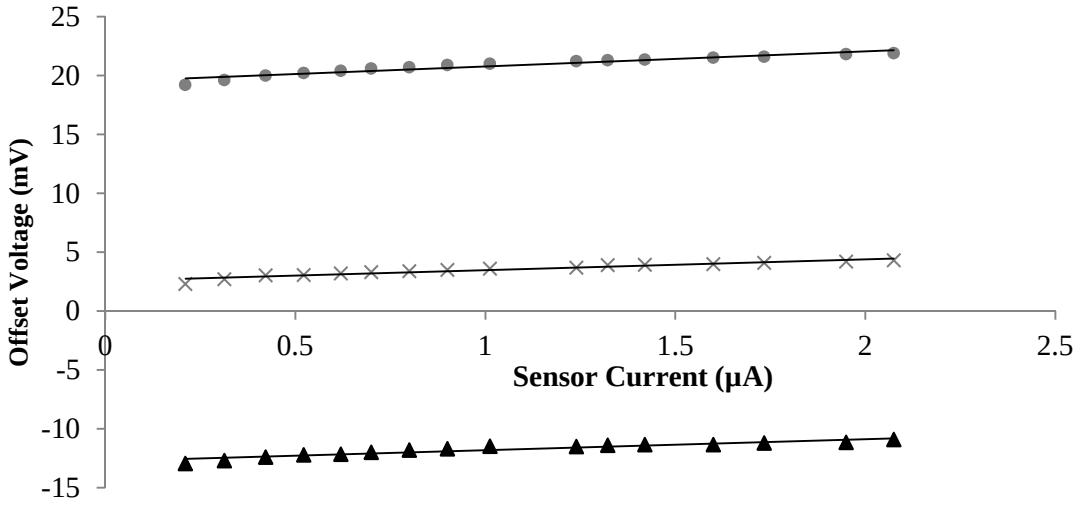
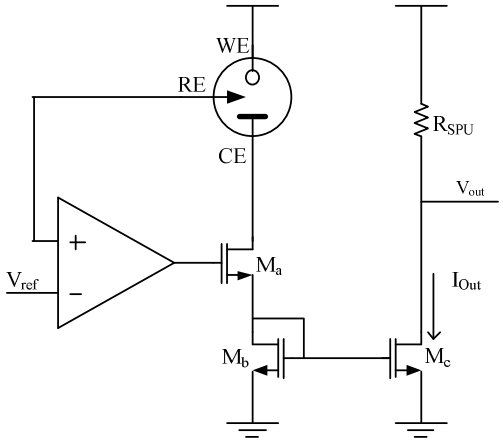


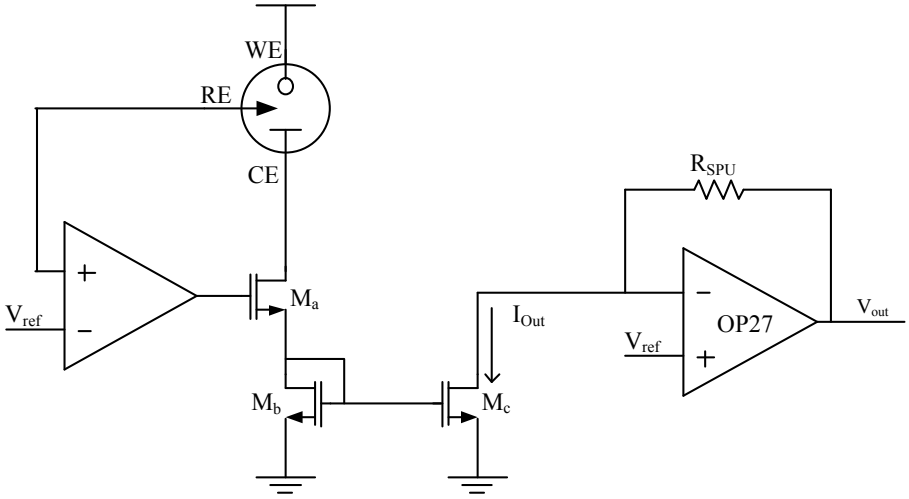
Fig. 6. 15. Offset measurement results for three different chips in a 0.5µm CMOS process.

6.2.4. Noise Performance Simulation and Test Result

The system noise performance has been simulated and tested for the chip fabricated in a 0.5µm CMOS process. In this system the output current noise defines the accuracy of reading in this system. To measure the output current noise, this current has been converted to voltage using a resistor and a transimpedance amplifier as shown in Figs. 6.16(a) and (b).



(a)



(b)

Fig. 6. 16. Circuit configuration for noise measurement.

The equation for the output voltage noise power density of the structure shown in Fig. 6.16(a) and the equation for the noise voltage power density at node RE are calculated in Appendix D. Fig. 6.17 shows the MATLAB simulation result based on these calculations. Fig. 6.18 shows the simulation result for the system output noise using the structure shown in Fig. 6.16(a) and the voltage at node RE under three different conditions to see the effect of feedback on the shape of the noise in the output current. The perfect match between the simulation results and the MATLAB simulation confirms the accuracy of these equations.

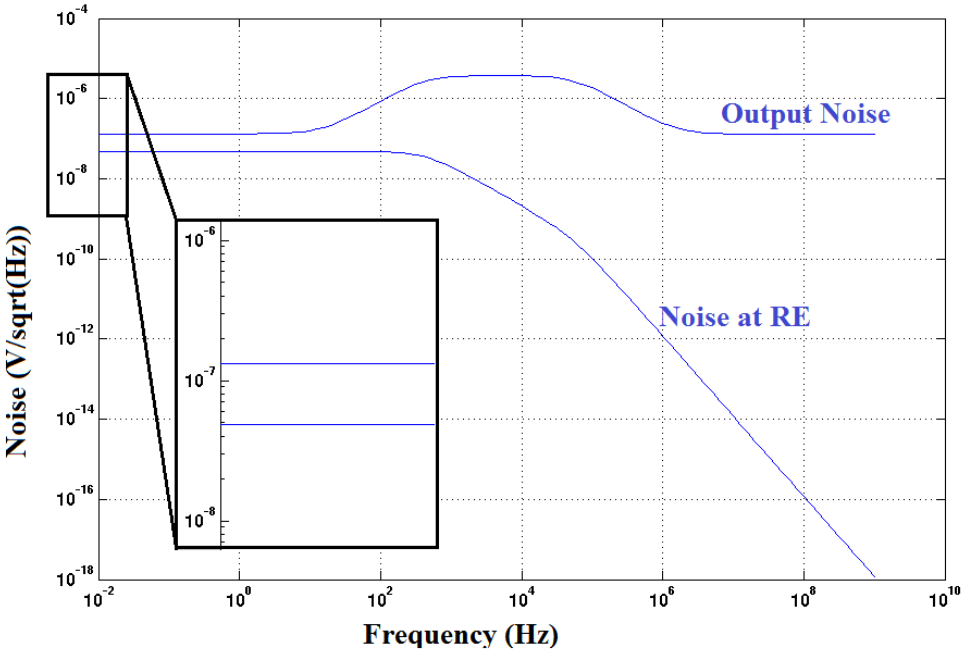


Fig. 6. 17. The MATLAB simulation result for the derived noise power density in Appendix D.

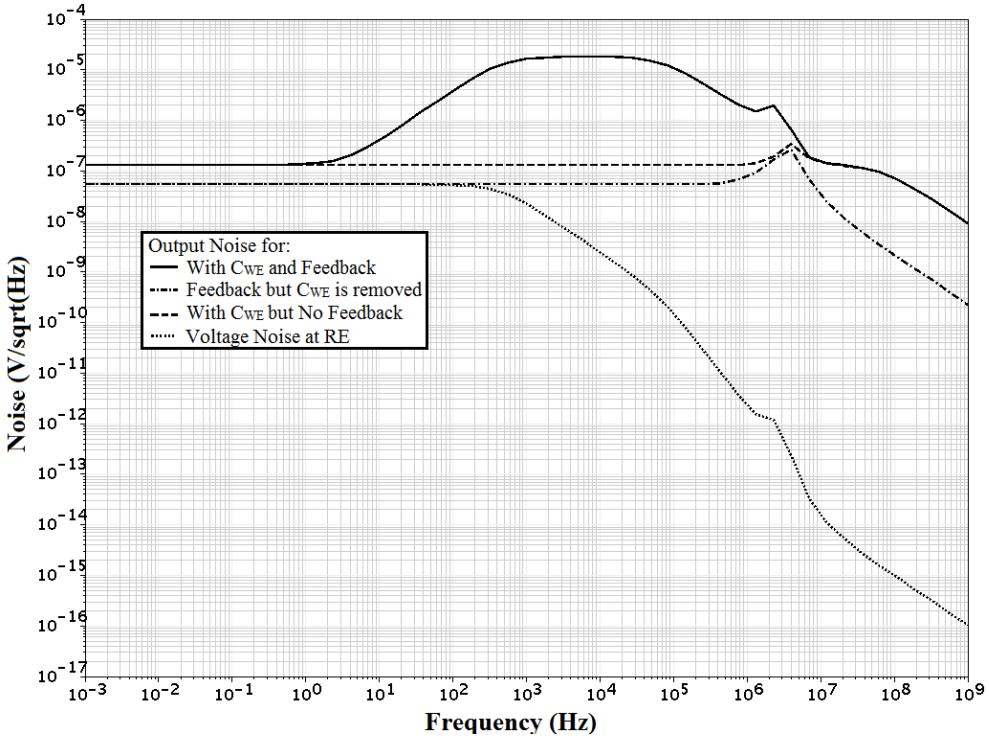


Fig. 6. 18. Simulation Result for current noise using a resistor in the path of the current.

Fig. 6.19 shows the test result for the output noise in the system using Figs. 6.16(a) and (b). The structure shown in Fig. 6.16(a) provides a pole at low frequencies in comparison with the structure shown in Fig. 6.16(b). The transimpedance amplifier forces a low impedance node at the output of the amplifier which increases the pole location at this node. Also the noise contribution of R_{SPU} at Fig. 6.16(a) is much noticeable than the noise contribution of R_{SPU} at Fig. 6.16(b). As expected, the noise contribution is decreased at low frequencies but because of the non-ideal connections, it is not as noticeable as it is in the simulation. In other words, in most ranges of the frequency, the noise in feedback has been delayed and the phase shift between the input and the output noise increases its value. This figure also shows the output noise seen at the output node RE and the output noise at opamp OP27 without connection to the circuit. The spikes existing in all the plots are the 60Hz wall noise and its harmonics. In this system the measurement is performed in less than 100ms and therefore the minimum frequency for measurement is chosen to be 1Hz, which is 10 times less than the requirement.

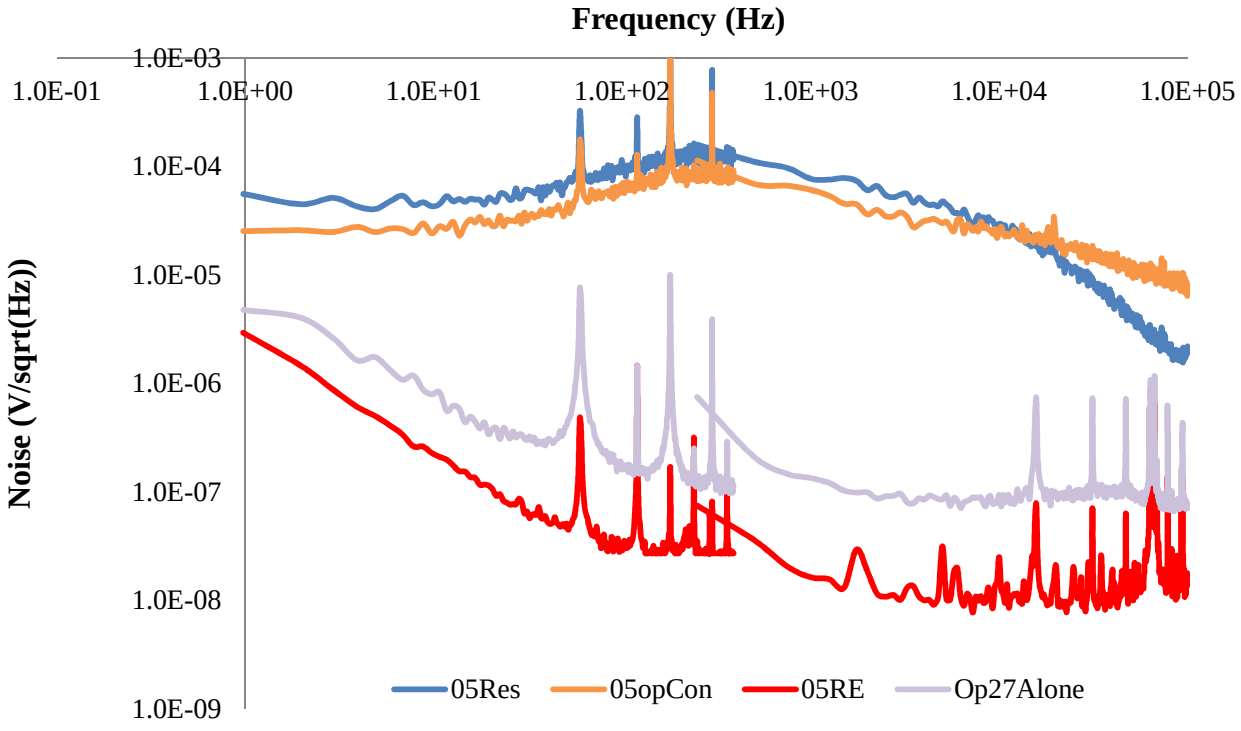


Fig. 6. 19. Test Result for current noise measurement using a resistor in the path of the current and OP27 with a resistor in feedback in the path of the current.

The integrated output noise using the transimpedance amplifier shown in Fig. 6.16(b) is as low as 6.039mV and it is 6.91mV for the structure shown in Fig. 6.16(a). The resistor used for this test is 100KΩ and therefore this voltage noise is equivalent to 0.06µA current noise. Based on Fig. 6.9, 1mmol/L (18mg/dl) change in the concentration of the solution is equal to 0.06µA change in sensor current. Therefore the accuracy of glucose measurement in this system with respect to noise is 18mg/dl.

6.3. Simulation and Test Results of the Signal Processing Unit

The structure shown in Fig. 5.1 has been fabricated using a 0.35µm CMOS process. The chip microphotograph is shown in Fig. 6.20 and the output signal of this structure is shown in Fig. 6.21. As shown in this figure, the output signal of this structure shows the behavior of the output of a one-bit delta-sigma structure. In the output of this structure, the "ones" and the "zeros" do not represent the same absolute value of the current.

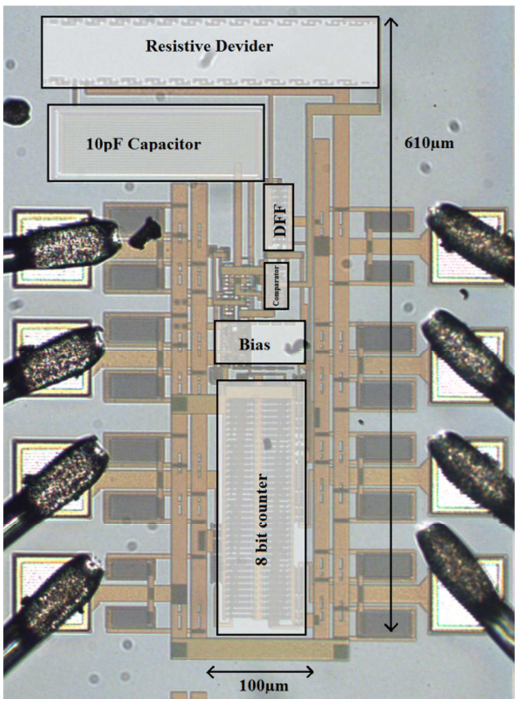


Fig. 6. 20. Chip microphotograph showing the signal processing unit in a 0.35µm CMOS process.

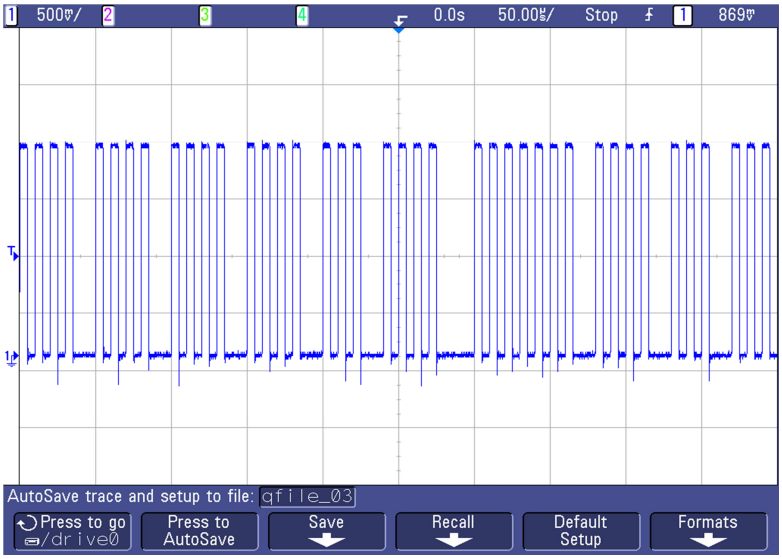


Fig. 6. 21. The measured output signal of the structure shown in Fig. 5.2.

To test the system performance shown in Fig. 5.1 an eight bit counter is added to the output of this structure and the test results are shown in Fig. 6.22. As shown in this figure, the output frequency linearly decreases with increasing input current. The bias I_b for this structure is set at 1μA.

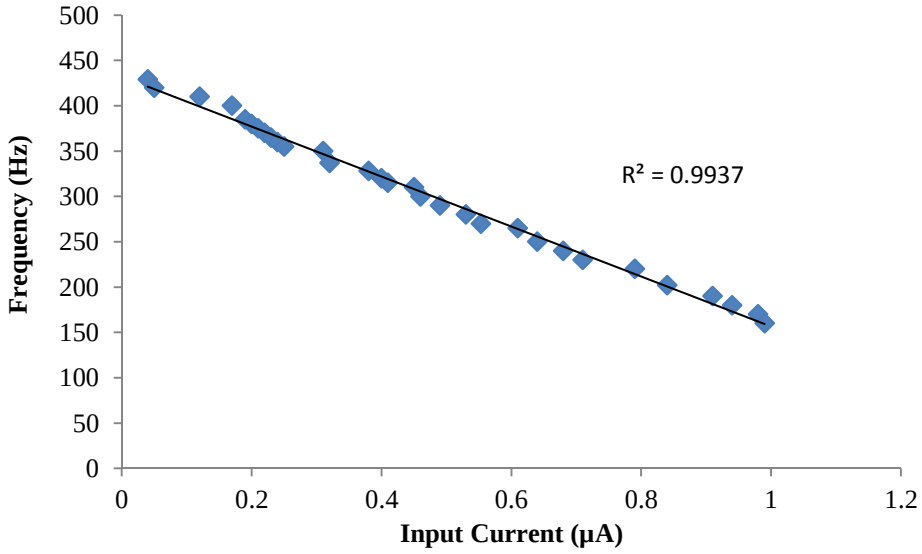


Fig. 6. 22. Chip test results after adding an eight-bit counter to the output.

Fig. 6.23 shows the simulation results of the voltage variation across the capacitor and the output signal of the comparator in Fig. 5.2 with I_b biased to be 4 times higher than I_S. As shown in this figure, each rising edge of the signal occurs separately and can be counted with less fluctuation in the output frequency.

The configuration shown in Fig. 5.2 has been simulated for different levels of current shown in Fig 6.24. For lower levels of current the clock frequency has been also reduced. The output results confirm the linearity and the accuracy of the proposed structure.

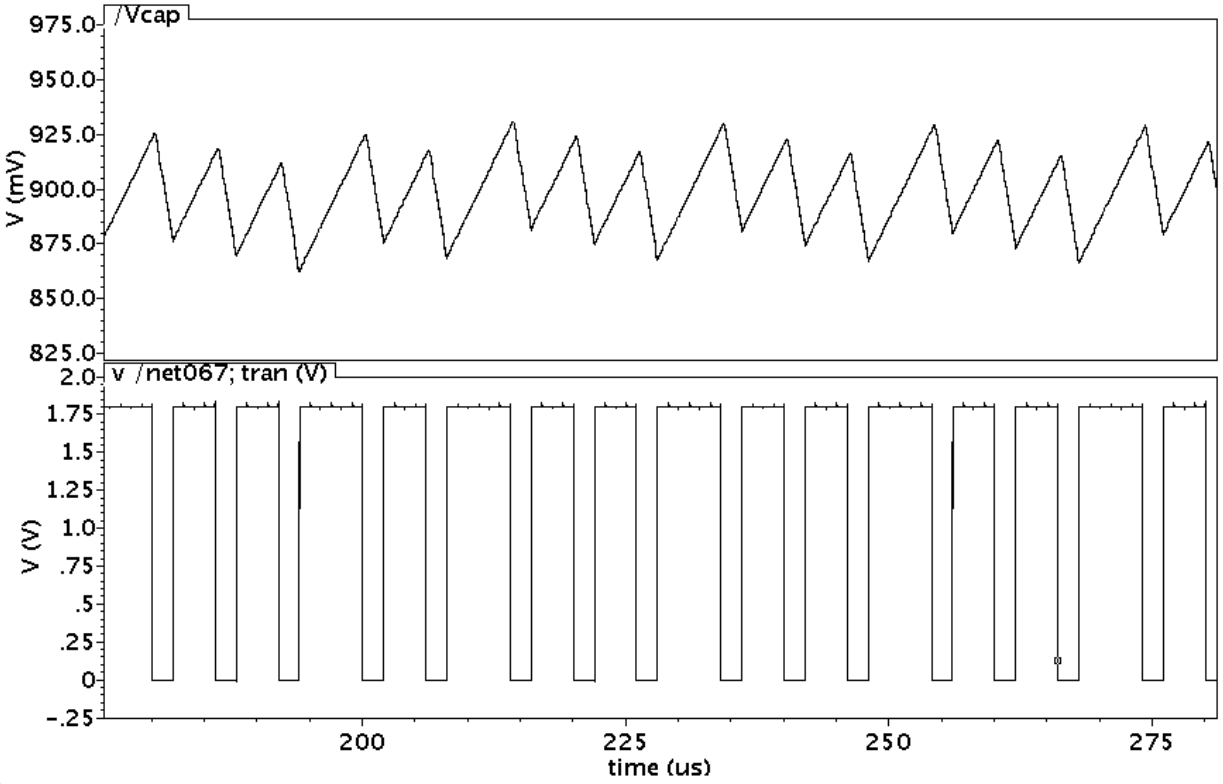


Fig. 6. 23. The capacitor voltage and the output signal of the comparator.

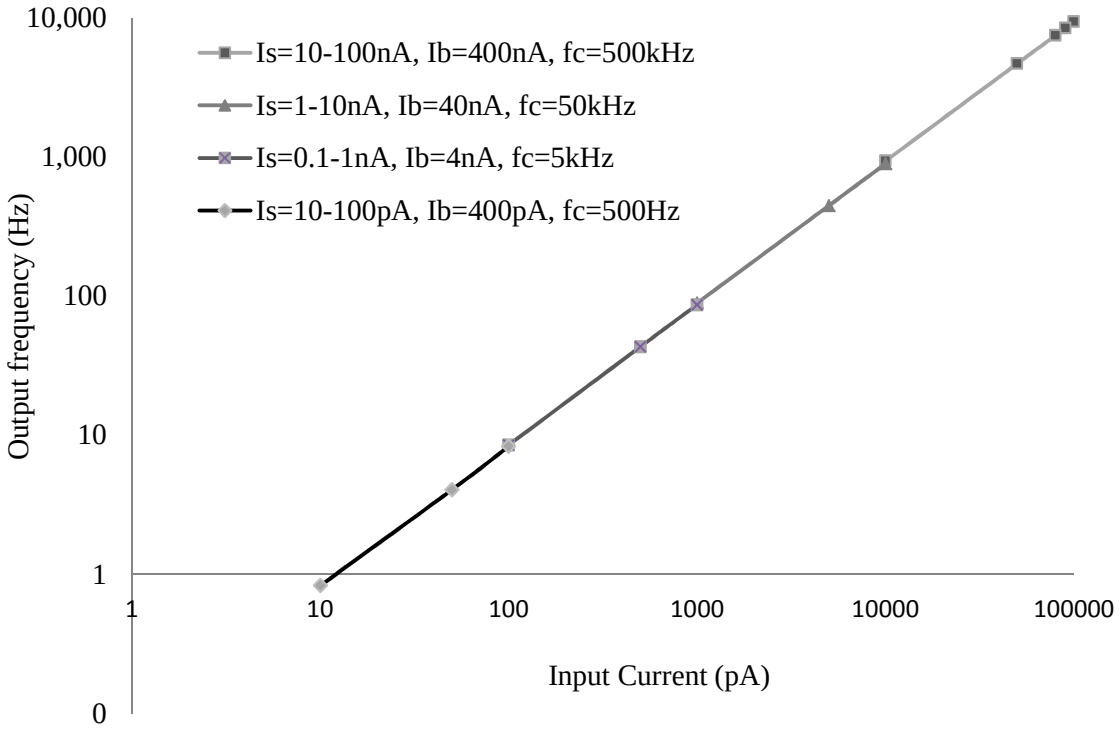


Fig. 6. 24. The modified SPU output frequency versus the input current.

CHAPTER 7 – Conclusion and Future Work

7.1. Conclusion

In this dissertation, a very low-power highly stabilized structure and its implementation circuit has been presented for a wirelessly powered implantable potentiostat. The design improvement is achieved both by modifying the conventional structure and also by using the subthreshold biasing technique. The proposed system is fabricated and simulated in a 0.35μm standard CMOS process. Simulation results show the power consumption of 3.5 μW for the sensor current of 0.2 μA and the power consumption of 10.1 μW for the sensor current of 2.4 μA. In addition, for all of the range of the resistors in the solution model introduced by [35] phase margin is simulated to be higher than 86º with open loop gain higher than 68 dB. Simulation also shows that the system can maintain stability even after moving the dominant pole 10 times further than the model introduced in [35]. Table 7.1 summarizes comparison between the results of this design with selected conventional structures. From this table it is evident that although this design employs an older CMOS fabrication process technology, it can achieve better performance in terms of the amount of power consumption.

This work also presents a modified structure for the signal processing unit of an implantable measurement sensor. The proposed structure achieves the accuracy of a delta-sigma modulator while keeping the simplicity of a capacitor in a feedback structure.

In Conclusion the original contributions of this work can be summarized as below:

1. Modifying the structure of potentiostat for achieving the high-stability while reducing the structure complexity.
2. Providing stability analysis of the potentiostat structure.

3. Employing the subthreshold technique to design an amplifier with controllable gain and first dominant pole.
4. Modifying the folded cascode structure based on the design requirement.
5. Providing a pole zero analysis for the proposed opamp.
6. Using subthreshold opamp design to reduce the power consumption of the potentiostat up to five times.
7. Providing noise analysis and noise measurement results for the potentiostat.
8. Providing the systematic and mismatch offset measurement of the potentiostat.
9. Proposing a wide range signal processing unit (SPU) for current measurement unit.
10. Improving the accuracy of reading in SPU to reduce the sensitivity to the floor noise and increase the ability of reading smaller values of current.
11. Deriving the equation for the SPU that proves the linearity of the SPU system for wide range of current measurement.

Table. 7. 1 Comparison Between the Proposed Design and Conventional Structures

	ISCAS 2004 [1]	**Sensors 2010 [2]**	**TCAS 2009 [3]**	**Proposed**
Technique	Resistor	Current Mirror	Current Mirror	Current Mirror
Process	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	0.35 µm CMOS
Supply Voltage	1.8	1.8	1.8	1.8
Power Consumption (µW)	8640	307-1248	35 (POT) +35 (SPU)	6.44-10.2 (POT) +36 (SPU)
Loop Gain (dB)	N/A	N/A	N/A	78-68
Sensor Current Range	N/A	.5nA-10µA	1nA-1µA	5nA-2µA

7.2. Future Work

This work includes designing three different structures that each can be improved separately. Therefore the future works can be summarized as below:

- Redesign the opamp for opamp general applications.
- Use the opamp as the main building block of a flexible filter with controllable parameters.
- Reconfigure the potentiostat to remove the PSRR problem.
- Improve the system accuracy by improving the noise performance of the potentiostat.
- Improve the linearity of current reading in signal processing unit.
- Improve the accuracy of current reading in signal processing unit.

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Appendix A

The AC equivalent of a simple potentiostat is shown in Fig.4.1. In this figure R_{S1} and R_{S2} are negligible in comparison with R_{WE} and R_{CE} and are eliminated to simplify the equations. To avoid complexity and keep the equations meaningful the output loads are combined together and is named to be $Y_{eq} = 1/Z_{eq}$. To calculate the open loop gain, the feedback is opened in Fig.4.1 and therefore the output can be calculated from the equation below:

$$V_{out} = V_s \frac{Y_{CE}}{Y_{WE}+Y_{CE}} = V_s \frac{1}{1+Y_{WE}/Y_{CE}} \tag{A.1}$$

For less source of instability the amplifier is assumed to have a simple one pole structure with the open loop gain of A_0, then the amplifier transfer function can be written as below:

$$A(S) = \frac{A_0}{1+S/P_A} \tag{A.2}$$

Therefore the gate voltage is equal to:

$$V_g = -\frac{A_0}{1+S/P_A} V_{in} \tag{4.3}$$

And there V_s can be calculated to be:

$$V_s = g_m V_{gs} \left(\frac{1}{Y_{eq}}\right) = g_m \left(-\frac{A_0}{1+S/P_A} V_{in} - V_s\right)\left(\frac{1}{Y_{eq}}\right) \tag{A.4}$$

Therefore:

$$V_s\left(Y_{eq} + g_m\right) = -\frac{g_m A_0}{1+{}^{S}/_{P_A}} V_{in} \tag{A.5}$$

From equations (A.1) and (A.5) the open loop transfer function can be calculated to be:

$$\frac{V_{out}}{V_{in}} = -\frac{g_m A_0}{1+{}^{S}/_{P_A}} \cdot \frac{1}{Y_{eq}+g_m} \cdot \frac{1}{1+Y_{WE}/Y_{CE}} \tag{A.6}$$

Where in this equation:

$$Y_{eq} = \frac{1}{R_{eq}} + C_{eq}s$$

$$Y_{WE} = \frac{1}{R_{WE}} + C_{WE}s$$

$$Y_{CE} = \frac{1}{R_{CE}} + C_{CE}s$$

Putting these values in equation (4.6), and considering $R_{CE}<<R_{WE}$ and $C_{CE}<<C_{WE}$, the open loop transfer function which is defined based on the values of resistors and capacitors can be summarized as below:

$$\frac{V_{out}}{V_{in}} = \frac{-g_m A_0}{1+{}^{S}/_{P_A}} \cdot \frac{(R_{WE}||R_{Ma})(1+R_{CE}C_{WE}s)}{(1+g_m R_{CE}+R_{CE}C_{CE}s)\left(\frac{1+g_m(R_{WE}||R_{Ma})}{1+g_m R_{CE}}+(R_{WE}||R_{Ma})C_{WE}s\right)} \cdot \frac{(1+R_{CE}C_{CE}s)}{(1+R_{CE}C_{WE}s)} =$$

$$\frac{-g_m A_0}{1+{}^{S}/_{P_A}} \cdot \frac{(R_{WE}||R_{Ma})(1+R_{CE}C_{CE}s)}{(1+g_m R_{CE}+R_{CE}C_{CE}s)\left(\frac{1+g_m(R_{WE}||R_{Ma})}{1+g_m R_{CE}}+(R_{WE}||R_{Ma})C_{WE}s\right)} \tag{A.8}$$

Appendix B

The proposed system transfer function can be calculated the same as Appendix-A. The AC equivalent of this system is shown in Fig. 4.2. In this figure, with the same assumption as appendix-A, V_{out} can be calculated to be:

$$\mathrm{V_{out}} = \mathrm{V_d}\frac{\mathrm{Y_{CE}}}{\mathrm{Y_{WE}+Y_{CE}}} = \mathrm{V_d}\frac{1}{1+\mathrm{Y_{WE}/Y_{CE}}} \tag{B.1}$$

Here the equation for V_d can be derived to be:

$$\mathrm{V_d} = -\mathrm{g_m V_{gs}}\left(\frac{1}{\mathrm{Y_{eq}}}\right) = -\mathrm{g_m}\left(\frac{\mathrm{A_0}}{1+{}^{\mathrm{S}}/_{\mathrm{P_A}}}\mathrm{V_{in}}\right)\left(\frac{1}{\mathrm{Y_{eq}}}\right) \tag{B.2}$$

From equations (B.1) and (B.2) the open loop transfer function can be calculated to be:

$$\frac{\mathrm{V_{out}}}{\mathrm{V_{in}}} = -\frac{\mathrm{g_m A_0}}{1+{}^{\mathrm{S}}/_{\mathrm{P_A}}}\cdot\frac{1}{\mathrm{Y_{eq}}}\cdot\frac{1}{1+\mathrm{Y_{WE}/Y_{CE}}} \tag{B.3}$$

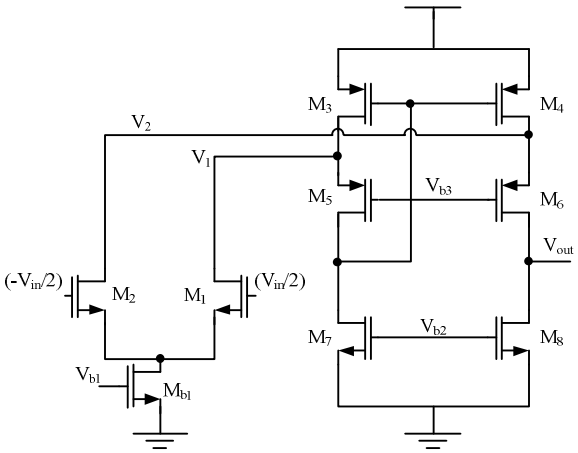
By replacing the Y_{WE}, Y_{CE} and Y_{eq} with their actual values on the equation (A.6), this equation can be rewritten to the equation below:

$$\frac{\mathrm{V_{out}}}{\mathrm{V_{in}}} = -\frac{\mathrm{g_m A_0}}{1+{}^{\mathrm{S}}/_{\mathrm{P_A}}}\cdot\frac{(R_{WE}||R_{Ma})(1+R_{CE}C_{WE}S)}{(1+R_{CE}C_{CE}S)(1+(R_{WE}||R_{Ma})C_{WE}S)}\cdot\frac{(1+R_{CE}C_{CE}S)}{(1+R_{CE}C_{WE}S)}$$

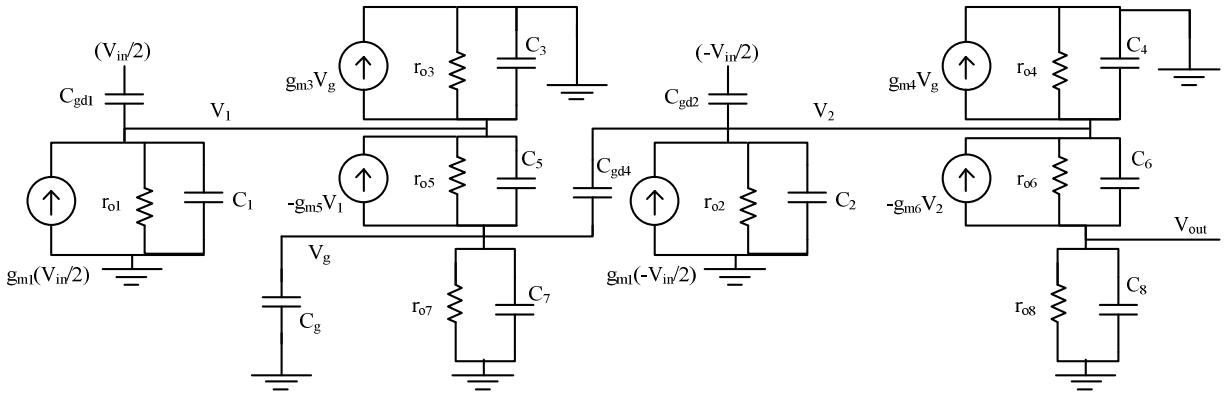
$$= -\frac{\mathrm{g_m}(R_{WE}||R_{Ma})\mathrm{A_0}}{1+{}^{\mathrm{S}}/_{\mathrm{P_A}}}\cdot\frac{(R_{WE}||R_{Ma})}{(1+(R_{WE}||R_{Ma})C_{WE}S)} \tag{B.4}$$

Appendix C

To calculate the position of poles and zeros in the proposed transimpedance amplifier structure, the small signal model of this amplifier is shown in Fig. C.1(b).



(a)



(b)

Fig. C. 1. a) The proposed transconductance amplifier. b) The small signal model for the proposed structure.

In Fig. C.1(b), it can be assumed that:

$$C_t = C_1 + C_3 = C_2 + C_4 = C_{ds1} + C_{ds3} + C_{sg5} \quad \text{(C.1)}$$

$$C_5 = C_{ds5} + C_{dg3} \qquad C_6 = C_{ds6} \qquad C_{gd1} = C_{gd2} \quad \text{(C.2)}$$

$$C_7 = C_8 = C_{ds7} + C_{dg7} + C_{dg5} \quad \text{(C.3)}$$

$$\text{and} \quad r_{ot} = r_{o1} \| r_{o3} = r_{o2} \| r_{o4} \qquad r_{o7} = r_{o8} \qquad g_{m3} = g_{m4} \qquad g_{m5} = g_{m6} \quad \text{(C.4)}$$

From Fig. C.1(b), the equations below can be derived:

$$\left(V_1 - {}^{V_{in}}/_{2}\right) C_{gd1} + V_1 C_t s + \frac{V_1}{r_{ot}} + \frac{V_1 - V_g}{r_{o5}} + (V_1 - V_g) C_5 s + g_{m3} V_g + g_{m5} V_1 = g_{m1} \left({}^{V_{in}}/_{2}\right) \quad \text{(C.5.E1)}$$

$$V_g (C_g + C_7) s + \frac{V_g}{r_{o7}} + \frac{V_g - V_1}{r_{o5}} + (V_g - V_1) C_5 s + (V_g - V_2) C_{gd4} s = g_{m5} V_1 \quad \text{(C.5.E2)}$$

$$\left(V_2 + {}^{V_{in}}/_{2}\right) C_{gd1} + V_2 C_t s + \frac{V_2}{r_{ot}} + \frac{V_2 - V_{out}}{r_{o5}} + (V_2 - V_{out}) C_6 s + g_{m3} V_g + g_{m5} V_2 + (V_2 - V_g) C_{gd4} s =$$

$$-g_{m1} \left({}^{V_{in}}/_{2}\right) \quad \text{(C.5.E3)}$$

$$V_{out} C_7 s + \frac{V_{out}}{r_{o7}} + \frac{V_{out} - V_2}{r_{o5}} + (V_{out} - V_2) C_6 s = g_{m5} V_2 \quad \text{(C.5.E4)}$$

From equation (C.5.E4), it can be derived that:

$$V_{out} \left(\frac{1}{r_{o7}} + \frac{1}{r_{o5}} + C_6 s + C_7 s\right) = V_2 \left(g_{m5} + \frac{1}{r_{o5}} + C_6 s\right) \quad \text{(C.6)}$$

By defining a parameter A_1 as below:

$$A_1 = \frac{\left(\frac{1}{r_{o7}}+\frac{1}{r_{o5}}+C_6 s+C_7 s\right)}{\left(g_{m5}+\frac{1}{r_{o5}}+C_6 s\right)} \tag{C.7}$$

The equation (C.6) can be simplified to:

$$V_2 = A_1 V_{out} \tag{C.8}$$

From equation (C.5.E2), it can be derived that:

$$V_g\left[(C_g + C_7)s + \frac{1}{r_{o7}} + \frac{1}{r_{o5}} + C_5 s + C_{gd4} s\right] = V_1\left(g_{m5} + \frac{1}{r_{o5}} + C_5 s\right) + A_1 V_{out} C_{gd4} s \tag{C.9}$$

By defining parameters A_2 and A_3 as below:

$$A_2 = \frac{\left(g_{m5}+\frac{1}{r_{o5}}+C_5 s\right)}{\left[(C_g+C_7)s+\frac{1}{r_{o7}}+\frac{1}{r_{o5}}+C_5 s+C_{gd4} s\right]} \quad \& \quad A_3 = \frac{A_1 C_{gd4} s}{\left[(C_g+C_7)s+\frac{1}{r_{o7}}+\frac{1}{r_{o5}}+C_5 s+C_{gd4} s\right]} \tag{C.10}$$

The equation (C.9) can be reduced to:

$$V_g = A_2 V_1 + A_3 V_{out} \tag{C.11}$$

From equation (C.5.E1), it can be derived that:

$$\left(V_1 - {V_{in}}/{2}\right) C_{gd1} + V_1 C_t s + \frac{V_1}{r_{ot}} + \frac{V_1 - (A_2 V_1 + A_3 V_{out})}{r_{o5}} + (V_1 - A_2 V_1 - A_3 V_{out}) C_5 s + g_{m3}(A_2 V_1 + A_3 V_{out}) + g_{m5} V_1 = g_{m1}\left({V_{in}}/{2}\right) \tag{C.12}$$

And therefore:

$$V_1\left(C_{gd1}+C_t s+\frac{1}{r_{ot}}+(1-A_2)\left(\frac{1}{r_{o5}}+C_5 s\right)+A_2 g_{m3}+g_{m5}\right)=\left({}^{V_{in}}/_{2}\right)\left(g_{m1}+C_{gd1}\right)+$$

$$(A_3 V_{out})\left(C_5 s+\frac{1}{r_{o5}}-g_{m3}\right) \qquad \text{(C.13)}$$

Now two new parameters A_4 and A_5 can be defined as below:

$$A_4=\frac{\left(g_{m1}+C_{gd1}\right)}{\left(C_{gd1}+C_t s+\frac{1}{r_{ot}}+(1-A_2)\left(\frac{1}{r_{o5}}+C_5 s\right)+A_2 g_{m3}+g_{m5}\right)}$$

$$\&\quad A_5=\frac{A_3\left(C_5 s+\frac{1}{r_{o5}}-g_{m3}\right)}{\left(C_{gd1}+C_t s+\frac{1}{r_{ot}}+(1-A_2)\left(\frac{1}{r_{o5}}+C_5 s\right)+A_2 g_{m3}+g_{m5}\right)} \qquad \text{(C.14)}$$

The equation (C.13) can be reduced to:

$$V_1=\left({}^{V_{in}}/_{2}\right)A_4+V_{out}A_5 \qquad \text{(C.15)}$$

And from equation (C.11) and (C.15):

$$V_g=\left({}^{V_{in}}/_{2}\right)A_4A_2+V_{out}(A_5A_2+A_3)=\left({}^{V_{in}}/_{2}\right)A_6+V_{out}A_7 \qquad \text{(C.16)}$$

where

$$A_7=A_5A_2+A_3 \qquad A_6=A_4A_2 \qquad \text{(C.17)}$$

From equation (C.5.E3), it can be derived that:

$$V_2\left(C_{gd1}+C_t s+\frac{1}{r_{ot}}+\frac{1}{r_{o5}}+C_6 s+g_{m5}+C_{gd4}s\right)+V_g\left(g_{m3}-C_{gd4}s\right)=-{}^{V_{in}}/_{2}\left(g_{m1}+C_{gd1}\right)+$$

$$V_{out}\left(\frac{1}{r_{o5}}+C_6 s\right) \qquad \text{(C.18)}$$

Therefore:

$$V_{out}\left[A_1\left(C_{gd1}+C_t s+\frac{1}{r_{ot}}+\frac{1}{r_{o5}}+C_6 s+g_{m5}+C_{gd4}s\right)-\frac{1}{r_{o5}}-C_6 s+A_7\left(g_{m3}-C_{gd4}s\right)\right]=$$

$$-{}^{V_{in}}/_{2}\left(g_{m1}+C_{gd1}+A_6\left(g_{m3}-C_{gd4}s\right)\right) \quad \text{(C.19)}$$

Based on equation (C.7) for A_1, equation (C.19) can be rewritten as below:

$$V_{out}\left[A_1\left(C_{gd1}+C_t s+\frac{1}{r_{ot}}+C_{gd4}s\right)+\left(\frac{1}{r_{o7}}+\frac{1}{r_{o5}}+C_6 s+C_7 s\right)-\frac{1}{r_{o5}}-C_6 s+A_7\left(g_{m3}-C_{gd4}s\right)\right]=$$

$$-{}^{V_{in}}/_{2}\left(g_{m1}+C_{gd1}+A_6\left(g_{m3}-C_{gd4}s\right)\right) \quad \text{(C.20)}$$

Therefore the equation (C.19) can be simplified to the below equation:

$$V_{out}\left[A_1\left(C_{gd1}+C_t s+\frac{1}{r_{ot}}+C_{gd4}s\right)+\left(\frac{1}{r_{o7}}+C_7 s\right)+A_7\left(g_{m3}-C_{gd4}s\right)\right]$$

$$=-{}^{V_{in}}/_{2}\left(g_{m1}+C_{gd1}+A_6\left(g_{m3}-C_{gd4}s\right)\right) \quad \text{(C.21)}$$

From the equation (C.21) the transfer function between V_{out} and V_{in} can be derived. It is obvious that the equation (C.21) is very complicated and it is very hard to find the position of poles and zeros from this equation. The complexity in this equation is mainly because of the drain-gate capacitance (C_{dg}) of the transistors that in most cases are negligible. Therefore to get an idea about the position of poles and zeros, this equation is simplified by assuming that all drain-gate capacitors are negligible and can be neglected. In this case, it can be derived that:

$$C_5 = C_6 \qquad \text{and} \qquad A_3 = 0 \Rightarrow\ A_5 = A_7 = 0, \quad A_g = A_2 V_1 \tag{C.22}$$

$$A_6 = A_4 A_2 = \frac{g_{m1}}{\left(\frac{1}{A_2}\left(C_t s + \frac{1}{r_{ot}} + \frac{1}{r_{o5}} + C_5 s + g_{m5}\right) - \frac{1}{r_{o5}} - C_5 s + g_{m3}\right)} =$$

$$\rightarrow\ A_6 = \frac{g_{m1}}{\left(\frac{1}{A_2}\left(C_t s + \frac{1}{r_{ot}}\right) + (C_g + C_7)s + \frac{1}{r_{o7}} + \frac{1}{r_{o5}} + C_5 s - \frac{1}{r_{o5}} - C_5 s + g_{m3}\right)} = \frac{g_{m1}}{\left(\frac{1}{A_2}\left(C_t s + \frac{1}{r_{ot}}\right) + (C_g + C_7)s + \frac{1}{r_{o7}} + g_{m3}\right)} \tag{C.23}$$

Therefore the equation (C.21) reduces in to:

$$V_{out}\left[A_1\left(C_t s + \frac{1}{r_{ot}}\right) + \frac{1}{r_{o7}} + C_7 s\right] = -{}^{V_{in}}\!/_{2}\,(g_{m1} + A_6 g_{m3}) =$$

$$-\left({}^{V_{in}}\!/_{2}\right) g_{m1}\left(1 + \frac{g_{m3}}{\left(\frac{1}{A_2}\left(C_t s + \frac{1}{r_{ot}}\right) + (C_g + C_7)s + \frac{1}{r_{o7}} + g_{m3}\right)}\right) \tag{C.24}$$

To calculate the dc gain from equations above, the dc values of above parameters can be calculated by assumption of $s = 0$.

$$A_1 = \frac{1}{A_2} = \frac{\frac{1}{g_{m5}} \| r_{o5}}{r_{o5} \| r_{o7}} \approx \frac{1}{g_{m5}(r_{o5} \| r_{o7})} \tag{C.25}$$

And therefore from equation (C.24):

$$V_{out}\left[\frac{1}{g_{m5} r_{ot}(r_{o5} \| r_{o7})} + \frac{1}{r_{o7}}\right] = -\left({}^{V_{in}}\!/_{2}\right) g_{m1}\left(1 + \frac{g_{m3}}{\left(A_1\left(\frac{1}{r_{ot}}\right) + \frac{1}{r_{o7}} + g_{m3}\right)}\right) \tag{C.26}$$

Where the output resistance can be derived from the equation below:

$$\frac{1}{R_{out}} = \frac{1}{g_{m5} r_{ot} (r_{o5} \| r_{o7})} + \frac{1}{r_{o7}} \tag{C.27}$$

Therefore the DC gain can be rewritten as:

$$DC\ gain = \frac{V_{out}}{V_{in}}\Big|_{s=0} = -(1/2) g_{m1} R_{out} \left(1 + \frac{g_{m3}}{\frac{1}{R_{out}} + g_{m3}}\right) = -(1/2) g_{m1} R_{out} \left(1 + g_{m3} \left(\frac{1}{g_{m3}} \Big\| R_{out}\right)\right)$$

$$= -(1/2) \left(g_{m1} R_{out} + g_{m1} \left(\frac{1}{g_{m3}} \Big\| R_{out}\right) g_{m3} R_{out}\right) \tag{C.28}$$

Appendix D

Here the noise equation has been derived for the potentiostat structure as shown in Fig. D.1. In this figure the R_{CE} and C_{CE} are neglected based on their small contribution in the output current noise. The $(V_{n1})^2$ in this figure represents the input referred noise of the opamp. A is the finite gain of opamp and P_1 is the first dominant pole of the opamp.

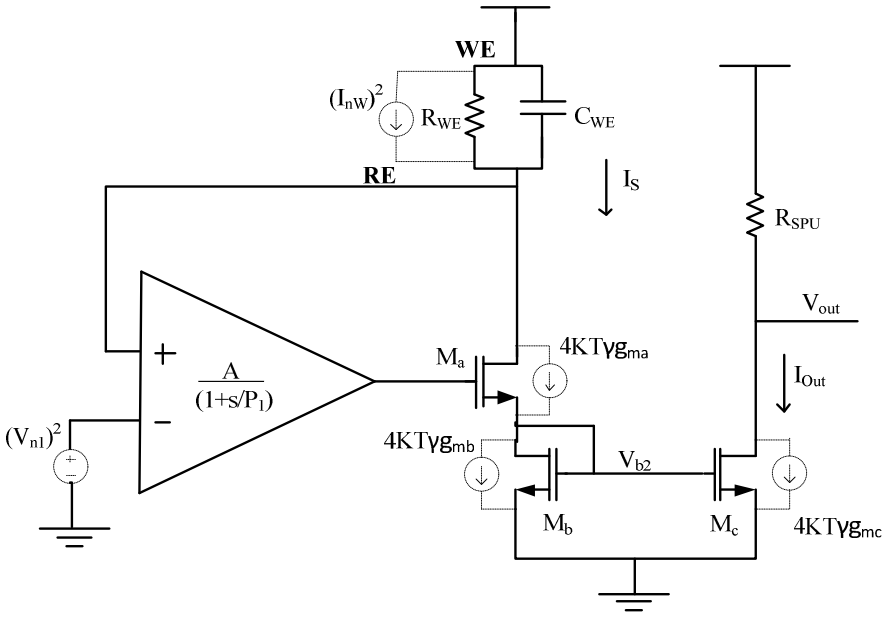


Fig. D. 1. Simplified potentiostat structure with the feedback for noise measurement.

To measure the input referred noise, the opamp structure is shown in Fig. D.2. In this circuit the voltage noise existing at node V_{nOut} can be calculated to be:

$$\overline{V_{nOut}^2} = 4KT\gamma(g_{m2} + g_{m4} + g_{m8})R_{Out}^2\Delta f + 4KT\gamma(g_{m1} + g_{m3} + g_{m7})\left(\left(\frac{1}{g_{m3}}\middle\| R_{O2}\right)^2 g_{m3}^2\right)R_{Out}^2\Delta f \quad \text{(D.1)}$$

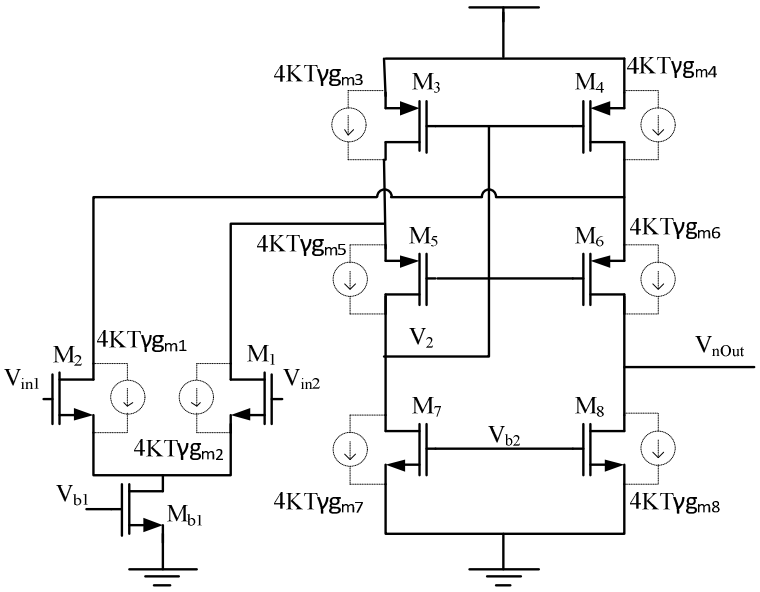


Fig. D. 2. Potentiostat structure with the demonstration of the thermal noise on the transistors.

In this equation it can be assumed that:

$$g_{m1} = g_{m2} \text{ and } g_{m3} = g_{m4} \text{ and } g_{m7} = g_{m8} \text{ and } \left(\frac{1}{g_{m3}} \middle\| R_{O2}\right)^2 g_{m3}^2 \cong 1 \tag{D.2}$$

Therefore the equation (D.1) can be simplified to the equation below:

$$\overline{V_{nOut}^2} = 8KT\gamma(g_{m2} + g_{m4} + g_{m8})R_{Out}^2\Delta f \tag{D.3}$$

In this circuit the input referred noise can be calculated by dividing the output noise of the opamp from equation (D.3) by the gain of opamp as below:

$$\overline{V_{n1}^2} = \frac{8KT\gamma(g_{m2}+g_{m4}+g_{m8})R_{Out}^2}{(g_{m2}R_{Out})^2} = \frac{8KT\gamma}{g_{m2}}\left(1 + \frac{g_{m4}}{g_{m2}} + \frac{g_{m8}}{g_{m2}}\right) \tag{D.4}$$

In the structure shown in Fig.D.1, the transfer function from the input $(V_{n1})^2$ to the node (RE) can be calculated as below:

$$\left[(V_{RE}-V_{n1})\frac{A}{1+s/P_1}G_{ma}+I_{nW}\right]\left(R_w \left\| \frac{1}{C_w s}\right.\right)=V_{RE} \tag{D.5}$$

where

$$G_{ma}=\frac{g_{ma}}{1+g_{ma}(\frac{1}{g_{mb}})} \qquad \text{and} \qquad I_{nW}=\frac{4KT}{R_{nW}} \tag{D.6}$$

therefore:

$$V_{RE}\left[\frac{AG_{ma}R_W}{(1+s/P_1)(1+R_WC_Ws)}-1\right]=V_{n1}\left(\frac{AG_{ma}R_W}{(1+s/P_1)(1+R_WC_Ws)}\right)-I_{nW}\frac{R_W}{(1+R_WC_Ws)} \tag{D.7}$$

Or equivalently:

$$V_{RE}=(-V_{n1})\left(\frac{AG_{ma}R_W}{(1+s/P_1)(1+R_WC_Ws)-AG_{ma}R_W}\right)+I_{nW}\frac{R_W(1+s/P_1)}{(1+s/P_1)(1+R_WC_Ws)-AG_{ma}R_W} \tag{D.8}$$

Therefore from equation (E.8) the noise power density can be derived to be:

$$\overline{V_{nRE}^2}=\overline{V_{n1}^2}\left(\frac{AG_{ma}R_W}{(1+s/P_1)(1+R_WC_Ws)-AG_{ma}R_W}\right)^2+\overline{I_{nW}^2}\left(\frac{R_W(1+s/P_1)}{(1+s/P_1)(1+R_WC_Ws)-AG_{ma}R_W}\right)^2 \tag{D.9}$$

From there the noise power density at the V_{out} can be derived to be:

$$V_{nOut}^2 = \left[\left(I_{nRE}^2 + I_{nb}^2\right)\frac{g_{mc}}{g_{mb}} + I_{nc}^2 + I_{nRspu}^2\right]R_F \qquad \text{(D.10)}$$

where in this equation I_{nb} and I_{nc} are the current noise from transistors M_b and M_c and I_{nRE} is the equivalent current noise for the calculated voltage noise V_{nRE}. These current noises can be calculated from the equations below:

$$I_{nRE}^2 = V_{nRE}^2\frac{(1+R_W C_W s)}{R_W} \quad , \quad I_{nb}^2 = 4KT\gamma g_{ma} \quad , \quad I_{nc}^2 = 4KT\gamma g_{mc} \quad \text{and} \quad I_{nRspu}^2 = \frac{4KT}{R_{SPU}} \qquad \text{(D.11)}$$

VITA

Melika Roknsharifi was born in Tehran, Iran in 1984. She received her B.S. degree in the major of electrical engineering from Iran University of Science and Technology (IUST), Tehran, Iran in 2006 where she received the honor award for achieving the second highest total GPA in four years of undergrad school. She received her M.S. degree from Sharif University of Technology, Tehran, Iran in the major of microelectronics in 2008. She started as Ph.D. student in The University of Tennessee in 2010. Her research interest is analog and mixed signal IC design in CMOS process.