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Low-Voltage Bulk-Driven Amplifier Design and Its Application in Implantable Biomedical Sensors

Liang Zuo
lzuo1@utk.edu

To the Graduate Council:

I am submitting herewith a dissertation written by Liang Zuo entitled "Low-Voltage Bulk-Driven Amplifier Design and Its Application in Implantable Biomedical Sensors." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

Syed Islam, Major Professor

We have read this dissertation and recommend its acceptance:

Jeremy Holleman, Benjamin J. Blalock, Laurence F. Miller

Accepted for the Council:

Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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Low-Voltage Bulk-Driven Amplifier Design and Its Application in Implantable Biomedical Sensors

A Dissertation Presented for the
Doctor of Philosophy
Degree
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Liang Zuo

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ABSTRACT

The powering unit usually represents a significant component of the implantable biomedical sensor system since the integrated circuits (ICs) inside for monitoring different physiological functions consume a great amount of power. One method to reduce the volume of the powering unit is to minimize the power supply voltage of the entire system. On the other hand, with the development of the deep sub-micron CMOS technologies, the minimum channel length for a single transistor has been scaled down aggressively which facilitates the reduction of the chip area as well. Unfortunately, as an inevitable part of analytic systems, analog circuits such as the potentiostat are not amenable to either low-voltage operations or short channel transistor scheme. To date, several proposed low-voltage design techniques have not been adopted by mainstream analog circuits for reasons such as insufficient transconductance, limited dynamic range, etc.

Operational amplifiers (OpAmps) are the most fundamental circuit blocks among all analog circuits. They are also employed extensively inside the implantable biosensor systems. This work first aims to develop a general purpose high performance low-voltage low-power OpAmp. The proposed OpAmp adopts the bulk-driven low-voltage design technique. An innovative low-voltage bulk-driven amplifier with enhanced effective transconductance is developed in an n-well digital CMOS process operating under 1-V power supply. The proposed circuit employs auxiliary bulk-driven input differential pairs to achieve the input transconductance comparable with the traditional gate-driven amplifiers, without consuming a large amount of current. The prototype measurement results show significant improvements in the open loop gain (A_O) and the unity-gain bandwidth (UGBW) compared to other works.

A 1-V potentiostat circuit for an implantable electrochemical sensor is then proposed by employing this bulk-driven amplifier. To the best of the author's knowledge, this circuit represents the first reported low-voltage potentiostat system. This 1-V potentiostat possesses high linearity which is

ABSTRACT

comparable or even better than the conventional potentiostat designs thanks to this transconductance enhanced bulk-driven amplifier. The current consumption of the overall potentiostat is maintained around 22 microampere. The area for the core layout of the integrated circuit chip is 0.13 mm^2 for a 0.35 micrometer process.

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CHAPTER 1

INTRODUCTION

1.1 Motivations

Patients can benefit greatly from monitoring of physiological factors such as pH level in tissues [1], glucose [2] and lactose [3] in bloodstreams, etc. Invasive medical devices such as small lancets are used to collect substances from human body for test and diagnostic purposes. These devices not only increase the risk of infection, but also perform very simple discrete measurements in the human body which are not sufficient under some situations such as monitoring of diabetic patients.

Recent developments in biomedical sensors and CMOS processing technologies have led to the realization of minimally invasive monitoring devices such as implantable biosensors for continuous monitoring of the patients with reduced risk of infection. A continuous monitoring system is a significant improvement over the discrete measurement devices and allows the doctors to examine in real time the medical data from patients anytime and anywhere via the internet. This method of monitoring enables the doctors to perform necessary actions according to the need of the patients. The gathered data from frequent monitoring also helps the hospitals to efficiently record the medical history of the patients for future references. Fig. 1.1 illustrates a typical implantable wireless biosensor system network.

Fig. 1.2 depicts a detailed implantable biosensor system platform integrating biosensors with integrated circuits (ICs) designed to be deployed inside the human body (i.e. under the skin). The sensor electronics can be implanted using standard CMOS technologies. CMOS technologies have advantages such as small volume and reliable operation which are both vital for implantable biomedical applications. Biosensors on this platform include glucose sensor, lactate sensor, oxygen sensor and pH sensor, etc.

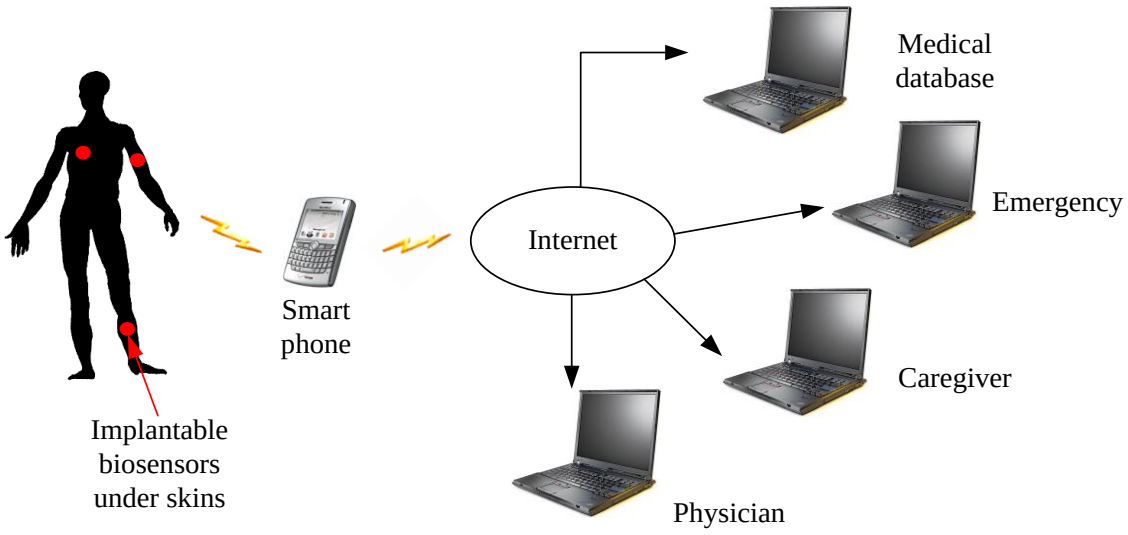

Fig. 1.1 Implantable biosensor system network.

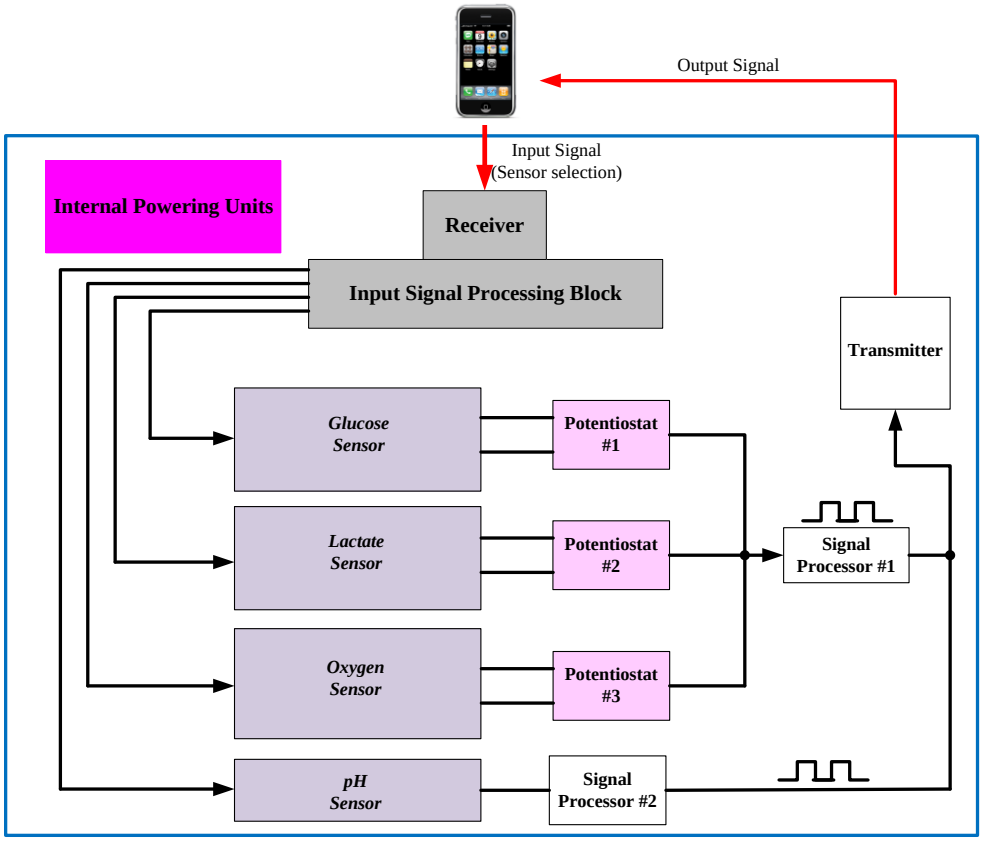

Fig. 1.2 Implantable biosensor system (inside blue rectangle).

Usually, these electrochemical or electrocatalytic sensors generate electrical analog signals which correspond to the presence of a particular target substance. Readout electronics including potentiostats accurately deliver these signals to the signal processor unit (SPU). Data is then transmitted outside via a transmitter to a smart phone. Peripheral ICs such as powering units, input signal processing block, etc. are also employed to realize this scheme on a system-on-a-chip (SoC) platform.

The current development of the implantable biosensor system focuses on miniature size and light weight for easy integration and biological safety [4]. On one hand, the development of deep sub-micron CMOS processes brings down the overall chip area greatly; On the other hand, since powering units usually consume a substantial part of the overall system, minimizing the power source on chip is also capable of reducing the chip area. This can be achieved by developing more efficient wireless powering methods or developing ICs with low-voltage and low-power operations. Compared to a battery-charged system, wireless powering does not have the issue of replacing the power source every once in a while, and is thus considered to be noninvasive with minimal or no risk of infection [4][5]. Both inductive coupling (i.e. inductive link) and optical coupling (i.e. solar cells) have been adopted as wireless powering methods as previously reported in literatures [4][6].

Nevertheless, from circuit designers' point of view, developing ICs using short-channel transistors with low-voltage and low-power operations is an appealing and efficient method to reduce the SoC chip area. Fortunately, the power supply voltage downscales in a similar fashion with the reduction of transistor channel length over the years. Otherwise the robustness and reliability of devices will deteriorate due to hot electron effect and time-dependent dielectric breakdown (TDDB) [7]. However, unlike the shrinkage of the power supply voltage (V_{DD}), the threshold voltage (V_T) reduces much less aggressively to maintain on/off characteristics of the MOS transistors [8]. Fig. 1.3 shows the trend of the power supply voltage (V_{DD}) and the threshold voltage (V_T) versus the transistor minimum channel length ($L_{effective}$) for the past 30 years [9][10].

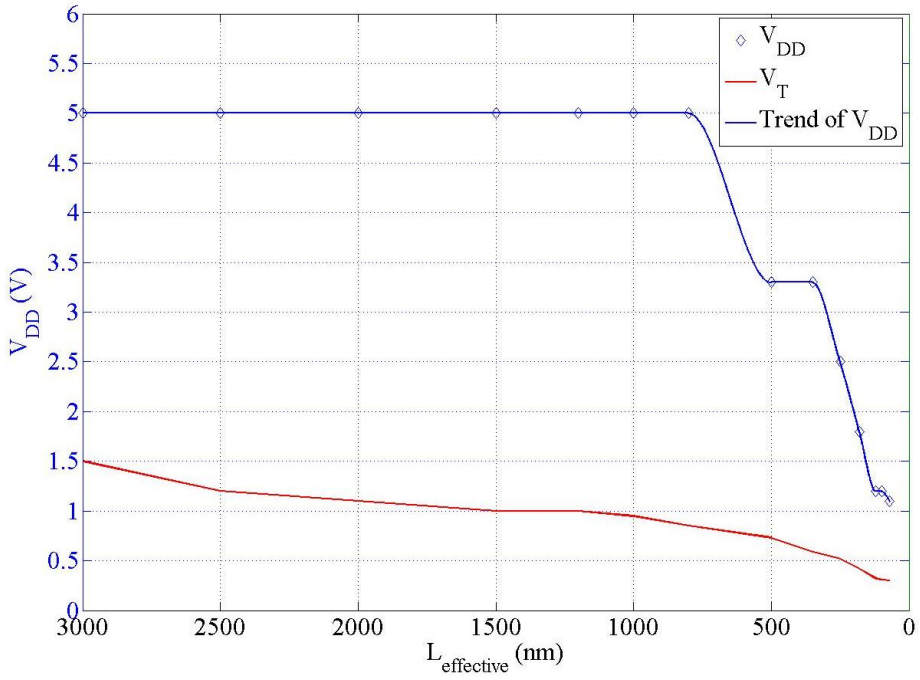

Fig. 1.3 Transistor power supply voltage and threshold voltage change with the effective channel length [9][10].

Thanks to the V_{DD} scaling, the power consumption of digital circuits decreases almost quadratically according to Eq.(1.1),

$$\boldsymbol{P_{Digital}} = \frac{1}{2} \times \boldsymbol{V_{DD}^2} \times \boldsymbol{C_L} \times \boldsymbol{f_{clk}} \tag{1.1}$$

where C_L is the load capacitance, f_{clk} is the clock frequency. Although the reduced V_{DD} will slow down the circuit speed, the smaller technology node compensates that to some extent.

However, compared to their digital counterparts, analog circuits such as amplifiers benefit much less from the scaling of CMOS technologies. The short channel devices typically yield worse offset, larger leakage current and smaller output impedance (r_o) compared to the long channel devices. Thus usually long channel transistors are extensively employed in analog designs, so as the work proposed in this dissertation. In addition, the low-voltage operation further complicates the designs of analog circuits.

Inherently, all low-voltage analog circuits suffer from inferior signal-to-noise ratio (SNR) due to the limited signal swing. For example, with half of the signal swing of an OpAmp, quadratically increasing its current consumption is a common solution to maintain the same SNR. Both of these limitations indicate that the volume reduction of the implantable biosensor system mainly depends on its analog components.

Analog circuits without employing any low-voltage design techniques limit their power supplies to the turn-on voltage of MOSFET (V_{GS}) plus the required signal swing [11][12][13]. For a 0.35 μm long channel CMOS process, a $|V_{GS}|$ of ~0.9 V is quite normal for a standard V_T PMOS biased in strong inversion. A general purpose gate-driven OpAmp design using this process operates at least under 1.8 V in order to achieve necessary signal swing. Thus OpAmp working under 1 V in a similar long channel process is considered to be low-voltage operation.

Research efforts have been encouraged to develop low-voltage analog circuit design techniques in standard long channel CMOS processes, in order to avoid the analog circuits on the SoC be the limiting factor of the overall power supply voltage. In this work, efforts have been focused on the development of an innovative low-voltage and low-power potentiostat circuit inside a biosensor system as shown in Fig. 1.2. Amplifiers are extensively employed in many potentiostat structures [4][14]-[16] and are considered as the fundamental circuit blocks among the entire analog ICs. Thus the development of a low-voltage and low-power amplifier is clearly the first step towards bringing down the supply voltage of the potentiostat and subsequently, of the entire system.

1.2 Research Goals

The purpose of this research is to develop a low-voltage and low-power potentiostat for the electrochemical sensors which will be used in an implantable biosensor system as shown in Fig. 1.2. A general purpose low-voltage (i.e. 1 V) low-power amplifier is implemented at first in a standard long

channel CMOS process to achieve comparable performance with amplifiers operating under nominal V_{DD}. The 1-V potentiostat is then designed including the proposed low-voltage low-power amplifier. The proposed design demonstrates high linearity and stability as evidenced by the measurement results.

1.3 Original Contributions

A low-voltage general purpose amplifier including novel bulk-driven input differential pairs is presented and analyzed in this work. The effective input transconductance $G_{m\_in\_eff}$ of this amplifier is significantly improved without greatly increasing the power consumption. This enhanced $G_{m\_in\_eff}$ is comparable to traditional gate-driven amplifiers. As a result, the circuit performance such as the circuit bandwidth and the open loop gain also benefit from this improvement.

The amplifier is then employed as the core of an electrochemical biosensor potentiostat which belongs to an implantable biomedical sensor system. The proposed potentiostat features a very low-voltage, low-power and high-linearity operation.

1.4 Overview of the Dissertation

In Chapter 1, an implantable biosensor system and the corresponding circuit composations are introduced. This is followed by a discussion on the importance of the low-voltage and low-power operation for an implantable biosensor system. A low-voltage potentiostat is set to be the research goal of this dissertation. In Chapter 2, various types of biosensors are introduced, which is followed by the discussion of different topologies of the potentiostat. In Chapter 3, several low-voltage design techniques to obtain low-voltage operations are compared. Following the selection of the appropriate bulk-driven technique, problems associated with several recent bulk-driven circuit works are discussed. To provide novel bulk-driven circuit design techniques for solving these problems, the details for the implementations of the bulk-driven OpAmp are presented in Chapter 4. The subsequent design of the

potentiostat is treated in Chapter 5. Simulations and measurements of the proposed bulk-driven OpAmp and the potentiostat are shown in Chapter 6. In the end, conclusions and future work are presented in Chapter 7.

CHAPTER 2

LITERATURE REVIEW: BIOSENSORS AND POTENTIOSTAT SYSTEM

In this chapter, different types of biomedical sensors and their working principles are introduced in Section 2.1. Among them, the amperometric sensors and their fabrication methodologies are explained in detail. The equivalent circuit models of these sensors for improvement of the design of the potentiostat system are presented. In Section 2.2, previous literatures on popular potentiostat topologies are reviewed and their performances are compared. Finally, the effects of the low-voltage and low-power operation of the potentiostat system are discussed in Section 2.3.

2.1 Introduction to Biomedical Sensors

Micro-fabricated electrochemical sensors are widely used inside the biomedical sensing system. They are generally categorized as conductivity/capacitance, potentiometric, amperometric and voltammetric sensors [17]. Each of these sensors is developed to detect the presence of one particular electrolyte and its concentration.

The conductivity/capacitance sensors are utilized to measure the conductance of the specific analyte. Albeit a very straightforward sensing method these sensors employ, the detection is often interfered by the Faradaic current (I_F) and the effect of the double layer formed at each electrode surface. I_F measures the rate of Faradaic process, which originates from either oxidation or reduction occurring at

the surface of electrode. Potentiometric sensor, on the other hand, is capable of accurately measuring the change of potential at the electrode-electrolyte interface when a redox reaction occurs at the electrode surface (half-cell reaction [17]), which can be used to determine the concentration of the analyte. Unfortunately, the interferences from other ions and the long-response time of these sensors (due to the employment of the electrometer with high input impedance) limit their usage for biomedical purpose [17].

Voltammetric and amperometric sensors are based on the relationship between the concentrations of the analyte and the corresponding Faradic current (I_F) and potential (E_i). The value of the Faradaic current depends on the concentrations of the analyte of interest. This concentration cannot be accurately characterized until the Faradic current reaches a limit set by the potential E_i across the electrochemical cell. This limiting current has a linear relationship with the analyte concentration under the conditions such that potential E_i does not increase beyond a specific required value (i.e. to avoid unrelated Faradaic processes associated with other substances). These two types of the sensors are quite widely used because of their effectiveness and well established fundamentals [17]. For an amperometric sensor, I_F is usually measured by fixing the potential E_i between electrodes. While for a voltammetric sensor, E_i is varied in different fashions, such as linear or cyclic, when Faradic current is quantified. Amperometric sensor is considered in [17] as a subclass of the voltammetric sensor, but can be more easily managed and designed, since other Faradaic or non-Faradaic currents can be generated if the potential E_i varies too much. Therefore, amperometric sensors are used throughout this work which requires a fixed E_i.

To develop amperometric sensors, at least two micro-fabricated electrodes are required: a working electrode (WE) and a reference electrode (RE) which are configured as shown in Fig. 2.1 (a). The working electrode is defined as the electrode at which the oxidation or the reduction reaction of interest takes place. The materials of this electrode can be Au, Hg, C, Pt and Ag etc. depending on the analyte of detection. The reference electrode is deployed to provide a stable reference to ensure that the potential E_i between these two electrodes is constant and within the requirement, irrespective of the

continuous transient Faradaic reaction inside the electrochemical cell. The reference electrode is mostly made of Ag/AgCl for biomedical applications. In the two electrode system, the RE is also responsible for electrically balancing the charges generated/replaced at the surface of the working electrode, without affecting its reaction. A potentiostat system is used to work in conjunction by controlling these two electrodes and effectively carrying out the Faradaic current from reduction or oxidation.

It is very difficult for a potentiostat system to control an electrode by supplying a constant voltage and a varying current at the same time. Therefore, modern amperometric-based sensing methodologies typically employ a three-electrode sensor system, where the aforementioned reference electrode is divided into two separate electrodes: the reference electrode (RE) and the counter electrode (CE). As shown in Fig. 2.1 (b), a potentiostat system controls the RE to act as a reference node to maintain sufficient potential E_i with respect to the WE and draws no currents, while the CE generates the opposite current occurring at the surface of the WE in order to keep the charges neutral. This three-electrode electrochemical cell can also be modeled by physical resistors and capacitors as shown in Fig. 2.2.

Here, the value of resistors R_{WE}, R_{RE} and R_{CE} represent the Faradic resistances of the working, reference and counter electrodes, respectively, while the value of resistors R_{S1} and R_{S2} represent the solution (analyte) resistances. The resistance of R_{WE} can be calculated in Eq.(2.1) as,

$$\boldsymbol{R_{WE}} = \frac{\boldsymbol{E_i}}{\boldsymbol{I_F}} \tag{2.1}$$

The resistance of R_{CE} is much smaller than that of R_{WE} since the size of the counter electrode is normally developed to be much smaller than that of the working electrode. The resistances of R_{S2} and R_{S1} are even more negligible compared to the rest. The value of capacitors C_{WE} and C_{CE} correspond to the electrode double-layer capacitances. They are proportional to the surface areas of each electrode.

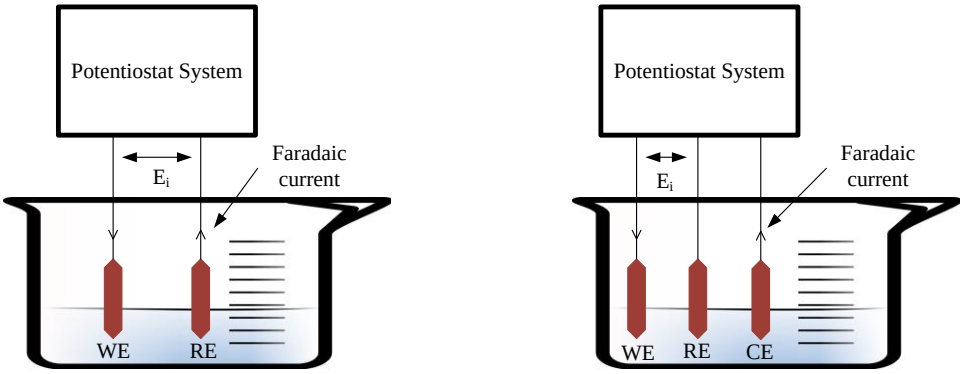

Fig. 2.1 (a) Two-electrode sensor system; (b) Three-electrode sensor system.

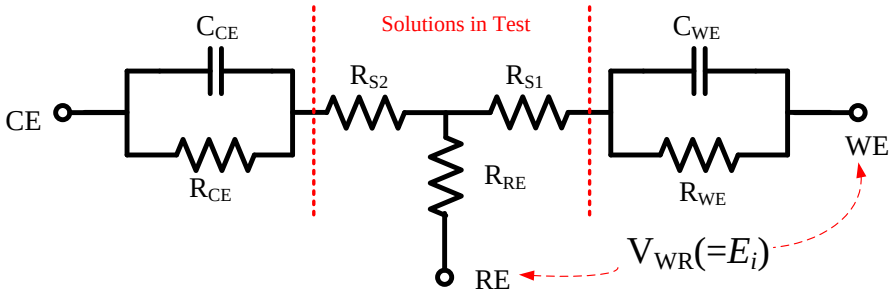

Fig. 2.2 Equivalent circuit model of a three-electrode electrochemical cell.

2.2 Comparisons of the Existing Potentiostat Structures

The purpose of the potentiostats for the voltammetric/amperometric biosensor systems is to generate adequate potential difference E_i between the working and the reference electrodes such that a specific analyte can be detected in the solution. It also should be able to accurately deliver sensor current (i.e. Faradaic current) through the counter electrode to the signal processing unit (SPU) so that the output signal of the system can be a reflection of the analyte concentrations.

2.2.1 Existing Configurations of the Potentiostats

The potentiostats for either voltammetric or amperometric biosensor systems inherently have similar configurations since they both measure the relationship between the potential E_i and the Faradaic

current I_F. Voltammetric potentiostats may need more dynamic range and involves more complicated designs. Several previously reported potentiostat utilized switched-capacitor circuitries for high-speed and high-accuracy detection [18]-[21]. However, in biomedical applications, system stability, power consumption and accuracy are the top priorities compared to the operating speed [22], which is why more recent and popular potentiostats have adopted only continuous OpAmps due to their simple structures and pure analog operations [23]-[36].

2.2.1.1 General Potentiostat Topologies

There are primarily two different configurations [37] of potentiostats, namely, 1) grounded WE or RE and 2) grounded CE. Fig. 2.3(a) illustrates a potentiostat with grounded WE configuration where grounded RE will result in a similar topology while Fig. 2.3 (b) represents a potentiostat with grounded CE configuration [37]. Under both circumstances, the potential between WE and RE (V_{WR}) is equal to E_i. It should be noticed that the potential E_i can be either positive as shown in the following potentiostats, or negative, which can be easily converted from the positive E_i potentiostat topologies.

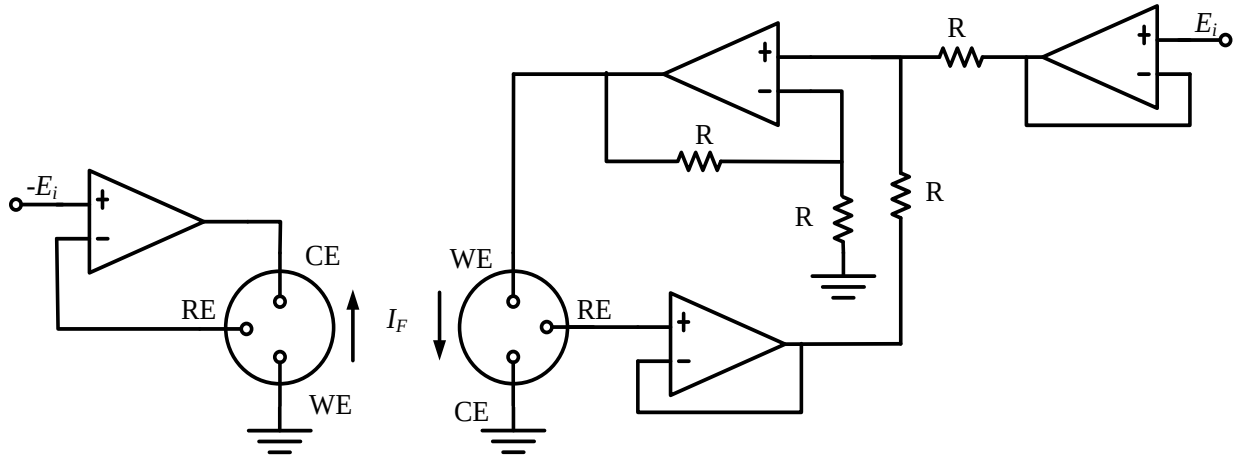

Fig. 2.3 (a) Potentiostat with grounded WE configuration; (b) Potentiostat with grounded CE configuration.

The circuitry in Fig. 2.3 (a) involves only one amplifier which results in low power consumption, small area and low noise. This circuit topology has been widely used in previous literatures compared to the circuitry in Fig. 2.3 (b). However, the grounded CE configuration in Fig. 2.3 (b) has better protection of the working electrode by shielding it from any ground noise or external electromagnetic interference (EMI), despite the fact that it employs several more active and passive components (i.e. more power consumption) and feedback loops [37].

2.2.1.2 Potentiostat Topologies in Previous Literatures

Ahmadi et al. proposed current-mirror-based potentiostats as shown in Fig. 2.4 (a) and (b) which are based on grounded WE configuration [14]. The transistor M_2 can simply mirror the sensor current (i.e. Faradaic current I_F) flowing through the transistor M_1. The topology shields WE by connecting it to a true AC ground potential. However, the circuit in Fig. 2.4 (a) is essentially a two-stage control amplifier (i.e. OTA A1 and common-source stage with the transistor M_1) which leads to two low-frequency poles (p_1 and p_2) existing inside the feedback loop. The design can be more difficult considering that the sensor current varies in magnitudes. As a result, the impedance at the output of OTA A1 cannot be too high in order to place its pole at higher frequencies. This design limitation could compromise the linearity and the power consumption of the overall system. Another similar work [26] proposed by the same authors managed to increase the open loop gain of the OTA to a degree by using partial positive feedback OTA but at the expense of additional current required for the operation. Further limitations of the partial positive feedback circuit are discussed in the following chapter. The circuit in Fig. 2.4 (b), on the other hand, uses the transistor M_1 as the source follower to eliminate the two low-frequency pole problem to some extent. However, it seriously limits the signal swing even under a nominal power supply voltage.

Haider et al. presented another potentiostat structure [4] based on the grounded CE configuration. Fig. 2.5 reveals its topology. It employs more amplifier blocks than the one in Fig. 2.3 (b), hence more lo-

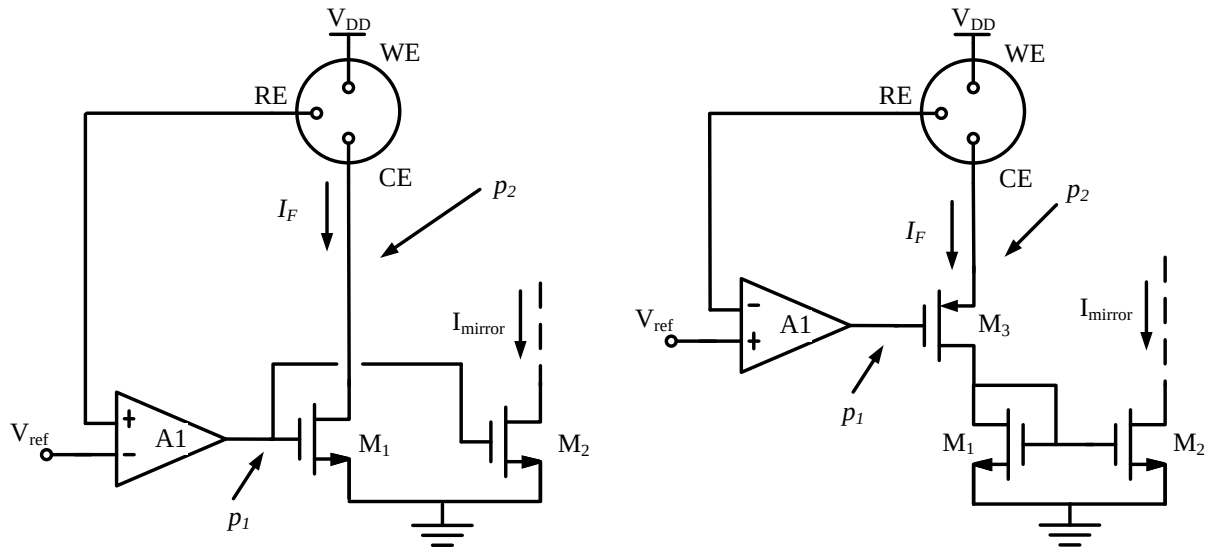

Fig. 2.4 (a) and (b) Current-mirror-based potentiostats in [14].

-op gain and better linearity. The power consumption of this circuit is relatively high due to the involvement of four amplifiers. In addition, the feedback loop inside this circuit is relatively hard to maintain stability.

Martin et al. proposed a fully differential (FD) potentiostat [33], which substantially increased the dynamic range compared to the previously reported single ended (SE) versions. This is particularly important for detecting chemical substances which require high potential E_i, such as Bromide (Br-) or Lead, etc. It is also very suitable for voltammetric sensors demanding high dynamic range. The fully differential potentiostat (shown in Fig. 2.6) can provide high precision and stable voltage reference between the electrodes, although typically more than one amplifier are employed in the design. Besides, to provide the required potential E_i, two voltage regulators are needed to provide adequate drive capability.

2.2.2 Existing Methods for Sensor Current Measurement

How to precisely deliver the sensor current externally or convert it to easy-to-process signals is

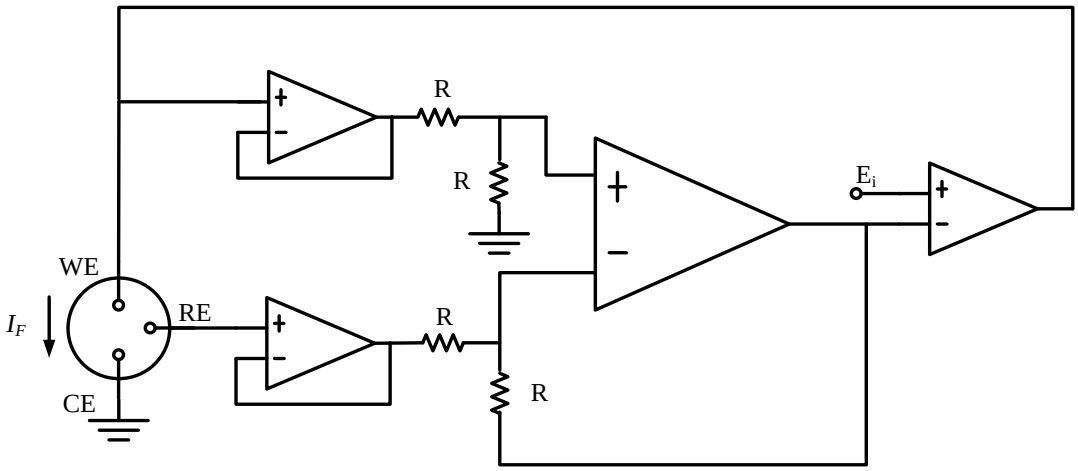

Fig. 2.5 Grounded CE based potentiostat presented in [4].

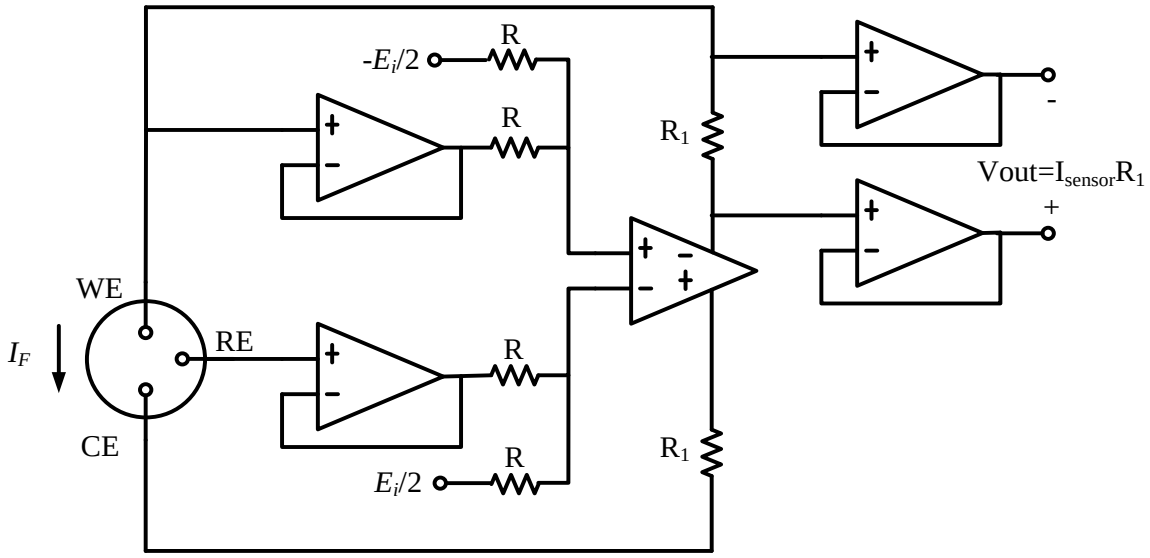

Fig. 2.6 Fully differential potentiostat in [33].

also very crucial in designing the overall potentiostat system. Several methods have been proposed up to date. The most common one involves connecting a trans-impedance amplifier (TIA) to the WE or the CE instead of directly grounding it.

In Fig. 2.7, either WE or CE is held at virtual ground, and the sensor current is converted to a

voltage signal. Either a large resistor can be used for the conversion [28] or a switched capacitor circuits can be arranged in order to save chip layout area [18]. The voltage signal normally requires a power hungry analog-to-digital converter (ADC) [23] to process the data which is not amenable to implantable biosensor systems. Although this configuration is very simple to implement and is capable of detecting very small sensor current, it poses a number of problems as mentioned in [14] and [33], such as unshielded and noisy WE, elevated input impedance of TIA at high frequencies and limited dynamic range, etc.

Another method to handle the sensor current is to convert it into a frequency signal without any help of ADCs but with the employment of a current-to-frequency (*I-F*) converter [4][14]. The topologies in these works are revealed in Fig. 2.8 and Fig. 2.9. Both of these *I-F* converters operate in similar manners. The circuit takes in I_F and the mirrored current charges the integrating capacitor C_{INT} until the voltage across it exceeds a specific fixed voltage (i.e. V_{DD}- $V_{T,Schmitt\_trigger}$ in Fig. 2.8 or V_{ref} in Fig. 2.9). Then another current path turns on (PMOS M_5 in Fig. 2.8 or NMOS M_4 and current source I_{REF} in Fig. 2.9) to discharge the C_{INT}. The charging rate or the integrating time τ is proportional to the mirrored current of I_F and the discharging rate is relatively fast in both cases. The period of the output data T can be expressed in Eq.(2.2) as,

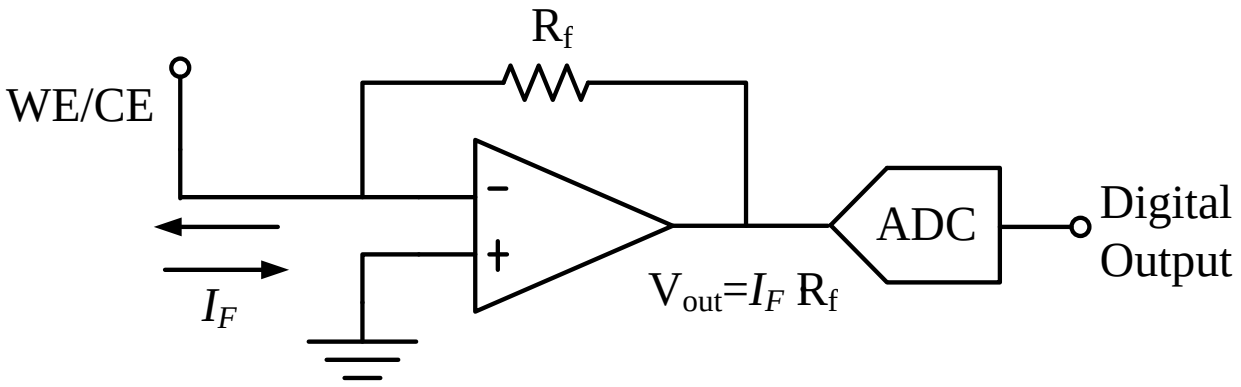

Fig. 2.7 Sensor current measurement circuit using TIA.

$$T \propto \frac{C_{INT}}{I_F} V_{TSchmitt\_trigger}\left(V_{ref}\right) \tag{2.2}$$

where $V_{Tschmitt\_trigger}$ is the Schmitt trigger threshold voltage in Fig. 2.8 and V_{ref} is the reference voltage in Fig. 2.9.

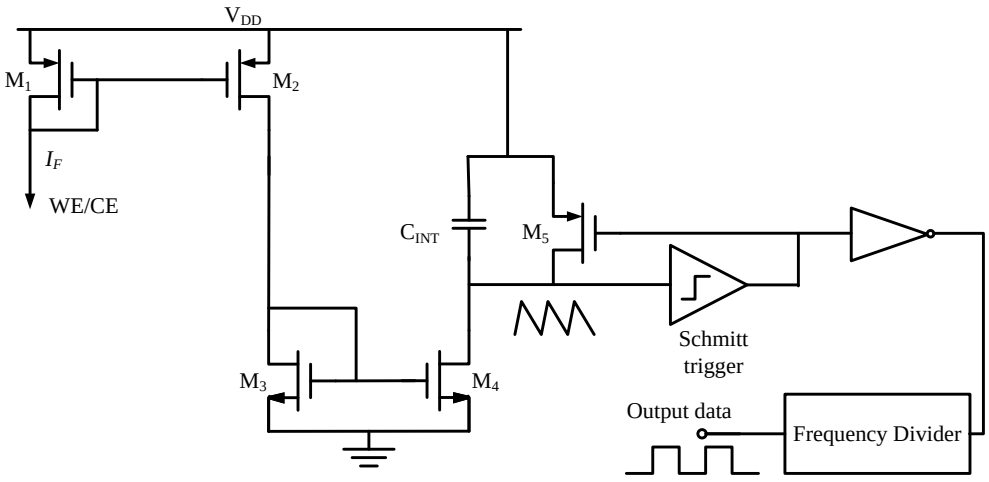

Fig. 2.8 Current to frequency (*I-F*) converter utilized in [4].

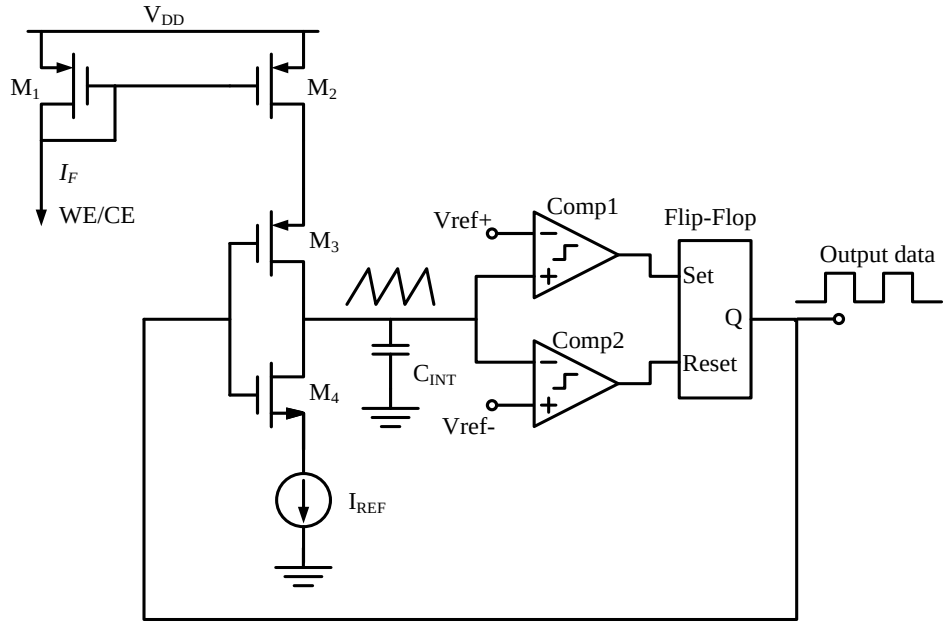

Fig. 2.9 Current to frequency (*I-F*) converter utilized in [14].

2.2.3 Discussions on Previous Structures

Table 2.1 summarizes the performance of each work discussed in the previous section. These works feature different potentiostat topologies and consequently different design complexities and current consumptions. In the potentiostat design, the selections of structures mostly depend on the requirements of linearity, power consumption and chip area for the specific applications. Apparently, for an implantable biosensor system, lower power consumption and smaller chip areas are top priorities. Most of the potentiostats reported in the literatures tried to limit power consumption by either reducing the number of active or passive components or designing circuit bandwidth no more than what is required. However, even more power can be saved if the power supply voltage can be reduced without much degradation of the circuit performance.

2.2.4 Impacts of the Low-Voltage Operations on Potentiostats

The low-voltage operation of the potentiostat system seems to be an unexplored research area in recent years. Several concerns prevent researchers from designing potentiostats using the low-voltage circuit design techniques.

Table 2.1 Comparisons of the Potentiostats Performance in Previous Literatures

	Process	**Supply voltage**	**Potentiostat power consumption**	**Linearity**	**Detected sensor current Range**	**Topology**
[4]	0.35 µm n-well CMOS	1.5 V	400 µW (Including SPU)	R^2= 0.999	200 nA->2 µA	SE
[14]	0.18 µm n-well CMOS	1.8 V	32.4 µW	R^2= 0.9984	1 nA -> 1 µA	SE
[26] (Simulation)	0.18 µm n-well CMOS	1.8 V	80 µW	N/A	1nA->200nA	SE
[33]	0.18 µm n-well CMOS	1.8 V	15840 µW	R^2= 0.98	N/A	FD
[36]	0.18 µm n-well CMOS	1.8 V	307 µW	N/A	10nA -> 10 µA	SE

1) A fixed potential E_i is mandatory between WE and RE for the amperometric biosensors. It is noted in [32] and [33] that for detecting most water-based heavy metal ions, this E_i is required to be between 0 V to |1.5 V|. Although for the O_2 or H_2O_2 based biomedical sensors such as glucose, lactate and glutamate, etc., the absolute value of E_i about 0.5 V to 0.7 V is usually sufficient for accurate detections. This potential decides the required voltage dynamic range of the potentiostat which limits the scaling of the overall power supply voltages.

2) Like other analog circuits, potentiostats with reduced power supplies suffer from gain degradations, either because of the insufficient transconductance or the limited use of stacked transistors. Low gain inevitably leads to poor linearity, which hurts the accuracy of the analyte detection. On the other hand, circuit techniques to boost the amplifier gain usually complicate the design and generate more poles and zeros in the overall feedback loop inside the potentiostat which introduce noise and cause instability.

However, the overall sensor system still benefits greatly from the reduction of the power supply voltages. As mentioned previously, the overall power source volume can be reduced given that current consumption is still maintained at a low level. Considering either on-chip solar cell or inductive link is employed as a power source, this power supply reduction can scale down the size of an implantable sensor system and makes it easier and safer to be deployed inside the human body. Since every potentiostat topology presented above and in past literatures employs amplifiers, therefore, developing a high performance low-voltage and low-power amplifier is clearly the first step towards the full implementation of a low-voltage and low-power potentiostat circuit.

CHAPTER 3

LOW-VOLATGE ANALOG CIRCUITS

In this chapter, various low-voltage analog circuit design techniques are introduced and compared in Section 3.1. Among them, the bulk-driven low-voltage design technique is discussed in Section 3.2. The advantages and disadvantages of this technique are also presented. In Section 3.3, bulk-driven amplifiers reported in previous literatures which target to increase the effective input transconductance ($G_{m\_in\_eff}$) are reviewed. Their performances are also compared.

3.1 Comparisons of the Low-Voltage Design Techniques

Potentiostats or generally speaking all analog circuits require operating voltages in the vicinity of the gate-to-source voltage (V_{GS}) to keep the transistors in strong inversion and provide necessary signal swing as discussed in the previous chapter. Since amplifiers are widely involved in any potentiostat system designs, the minimum power supply for an amplifier design has been specifically discussed in [38]. For example, powering of a push-pull output stage demands at least the sum of NMOS and PMOS threshold voltages (i.e. $V_{DD}+|V_{SS}|> V_{TN}+|V_{TP}|$), without using any low-voltage design techniques. Although some processes offer low V_T transistors at additional cost and turn-around time or zero V_T devices which are not well modeled[8], standard V_T transistors are still favored by analog designers primarily because they tend to give much lower sub-threshold leakage current and better noise immunity [7][13].

Several techniques have been proposed so far to design amplifiers operating under or around $V_{TN} + |V_{TP}|$ without employing low V_T or zero V_T transistors, such as bulk-driven MOSFET [11] [38], floating

gate MOSFET[39], sub-threshold design [40], level shift techniques [41], etc. Each of these techniques is briefly introduced and analyzed below.

If the gate terminal is biased properly to turn on the MOSFET, the signal can be applied between the bulk-to-source junction of the MOSFET so that the drain-to-source current is modulated, a scheme known as "bulk-driven technique". Obviously, the dynamic range of the amplifier is increased since there is no threshold voltage associated with the bulk terminal which allows a very low-voltage operation. However, the main problem with the bulk-driven technique is that the bulk transconductance (g_{mb}) is substantially smaller than the gate transconductance (g_m). This insufficient transconductance will affect the performance of the amplifier, such as bandwidth, open loop gain, input referred noise, etc.

Floating gate (FG) devices were first found popular use in digital storage elements such as EPROMs, EEPROMs and flash memories. Recently, analog circuits such as amplifiers and filters have also utilized multi-input floating gate (MIFG) devices as an integral part of the circuits [13]. The gate of a FG device is electrically isolated by high resistive materials thus creating a floating node. Secondary gates are deposited above the FG acting as inputs. The charge in the device channel is then modulated by the input signals via capacitive dividers. Therefore, two polysilicon layers in a standard CMOS process are used for developing the FG devices. Amplifiers employing MIFG transistors can be used in ultra low-voltage operation while still exhibiting large input swing and high input linear range thanks to the capacitive coupling. However, its input transconductance is attenuated due to the capacitive coupling, which results in similar disadvantages as the bulk-driven amplifiers.

Sub-threshold design exploits the sub-threshold operating region of the MOSFET devices. Low-voltage operation is possible since the gate-to-source voltage (V_{GS}) of the transistor is smaller than V_T and the saturation voltage ($V_{DS,sat}$) is only around 100 mV. Sub-threshold circuit features extremely low current consumption since the channel current is dominated by diffusion of the carriers instead of drift. On the other hand, the bandwidth and the slew rate of the circuit are severely limited. Sub-threshold

current is also very sensitive to process, voltage and temperature (PVT) variations due to the exponential relations between V_{GS} and V_T. Overall, analog circuits designed in sub-threshold region are theoretically expected to fit in the implantable biomedical application quite well. However, usually only a few transistors (i.e. input differential pairs) inside a typical amplifier are designed to be in this region to avoid either mismatch or instability issues [42]. Hence, sub-threshold circuit designs can sometimes be hybrid with other low-voltage design techniques.

Dynamic level shifting circuit provides a feasible solution to low-voltage differential input pairs. It utilizes resistors to level shift the common mode input voltage (V_{CM}) of the amplifier to the operating zone of the input transistors. The modified input pairs still maintain sufficient transconductance compared to the previous techniques, but suffer from low input impedance and considerable resistor area which are undesirable in modern CMOS circuits and limit their usage in the implantable biomedical system. Other level shift circuits consisting of only active components can be employed to accommodate either current mirrors (CMs) or amplifier output stages for low-voltage operations.

Other low-voltage design techniques have also been proposed for individual analog circuit blocks [43]. For example, active input structures can be adopted to develop low-voltage current mirrors and self-cascode MOSFETs can be configured to increase the output impedance of current mirrors while providing large voltage headroom.

For low-voltage operations, each aforementioned technique has certain performance limitations, such as circuit bandwidth, input referred noise, and offset etc. Depending on the power and the supply voltage budget or the circuit bandwidth requirement, specific application usually has its best low-voltage design technique candidates. Table 3.1 presents some performance comparisons of the low-voltage design techniques mentioned in this section.

This work mainly adopts the bulk-driven circuit design technique to develop the low-voltage amplifier and subsequent potentiostat system, since they have been exploited extensively in recent years.

Table 3.1 Techniques in Low-Voltage Analog Circuit Design

Technique	Bandwidth	Supply voltage	Power requirements	Technology requirements
Sub-Threshold	Low	$< V_{TN}+\|V_{TP}\|$	Low	Standard
Bulk-Driven	Low	$< V_{TN}+\|V_{TP}\|$	High	Standard
Floating Gate	Medium	$< V_{TN}+\|V_{TP}\|$	High	Standard
Level Shift	High	$< V_{TN}+\|V_{TP}\|$	Medium	Standard
Other Techniques	High	$> V_{TN}+\|V_{TP}\|$	Medium	Standard

Meanwhile, some of the aforementioned techniques are also employed, such as level shift technique, etc.

Although for a typical bulk-driven amplifier, limited bandwidth or insufficient gain can affect its performance, new topologies are proposed in this work to overcome these shortcomings, and make it suitable for the implantable biomedical applications.

3.2 Introduction of the Bulk-Driven Technique

Bulk-driven MOSFET is first adopted in [38] by Blalock et al in a standard n-well CMOS process where only PMOS transistors can be used as the bulk-driven transistors. The operation of a bulk-driven MOSFET is similar to a JFET [11] as depicted in Fig. 3.1. Once the inversion layer beneath the transistor gate is formed by sufficient gate-to-source biasing voltage, the channel current can be modulated by varying the bulk-to-source junction potential (V_{BS}). This operation eliminates the threshold voltage limitation of the gate-driven MOSFET since the bulk-to-source junction can be positive, zero, or slightly negative biased and still acts as the high impedance node as long as the junction diode is not turned on.

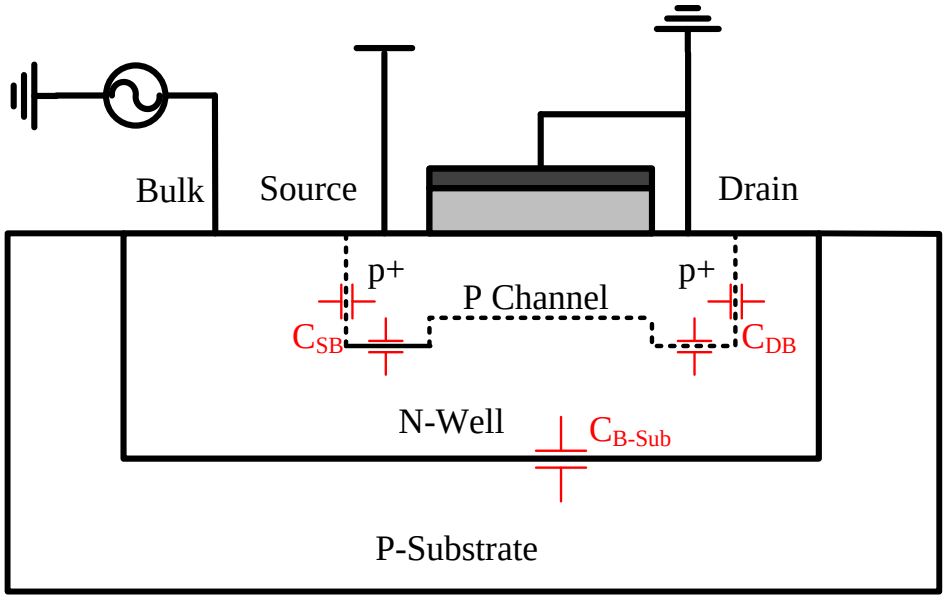

Fig. 3.1 Bulk-driven PMOS transistor.

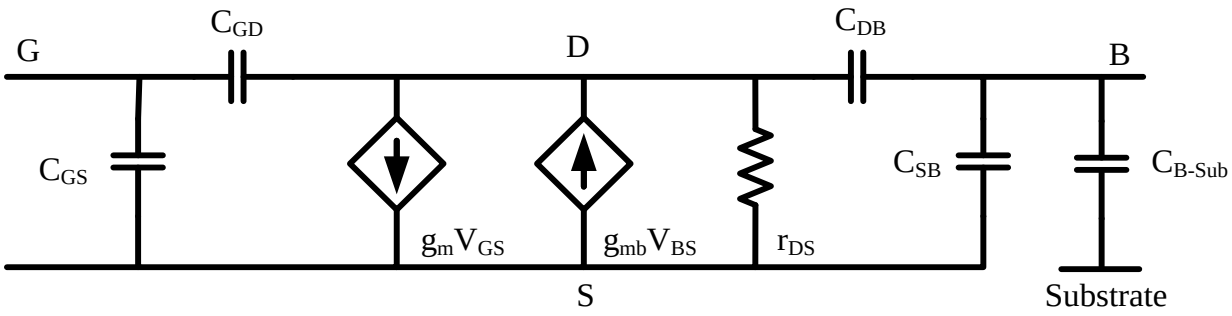

Fig. 3.2 Small signal model of the PMOS transistor.

Fig. 3.2 illustrates a small signal model of the PMOS device.

The square law equation for the PMOS transistor in saturation can be applied in Eq. (3.1) to describe the relationship between the output drain current (I_D) and the bulk-to-source voltage (V_{BS}) without any channel length modulation.

$$I_D = \frac{1}{2}\beta\left(V_{SG} - V_{THP0} - \gamma_P\left(\sqrt{2\phi_F + V_{BS}} - \sqrt{2\phi_F}\right)\right)^2 \tag{3.1}$$

where V_{THP0} is the threshold voltage of PMOS at zero substrate voltage, φ_F is the bulk Fermi potential, γ_P is a constant describing the substrate bias effect, V_{SG} is the fixed source-to-gate voltage.

The bulk transconductance g_{mb} can be then derived in Eq.(3.2) by taking derivatives of I_D to V_{BS}.

$$g_{mb} = \frac{dI_D}{dV_{BS}} = \left| -\beta\left(V_{SG} - V_{THP0} - \gamma_P\left(\sqrt{2\phi_F + V_{BS}} - \sqrt{2\phi_F}\right)\right)\frac{\gamma_P}{2\sqrt{2\phi_F + V_{BS}}}\right| \tag{3.2}$$

where g_{mb} can be further related to g_m in Eq. (3.3).

$$g_{mb} = g_m \frac{\gamma_P}{2\sqrt{2\phi_F + V_{BS}}} = g_m \bullet \eta \tag{3.3}$$

where η is the ratio from g_{mb} to g_m, which maintain constant at the same V_{BS}. Reportedly, if the bulk-to-source junction is not fully turned on, the ratio of g_{mb} to g_m only ranges from 0.2 to 0.4 depending on the bulk-to-source voltage and the specific process parameters [11]. For example, typical values for γ_P and $2\varphi_F$ in a 1μm CMOS process are 0.6 and 0.7, respectively, for PMOS devices [44]. Therefore, at zero V_{BS} biasing, the bulk transconductance g_{mb} is about 0.36 times of the gate transconductance g_m. This becomes a limiting factor for the bulk-driven circuit designs.

With only the bulk terminal being modulated, the input capacitance includes the capacitances with respect to the drain and the source terminals (C_{DB} and C_{SB}) and the N-well-to-P-substrate capacitance ($C_{B\text{-}Sub}$) as labeled in both Fig. 3.1 and Fig. 3.2. These capacitances (C_{DB}, C_{SB} and $C_{B\text{-}Sub}$) consist of the depletion capacitances of their respective junctions and sidewalls. They are expressed in Eq.(3.4), Eq.(3.5) and Eq.(3.6),

$$C_{SB} = \left(A_{channel} + A_{source}\right)C_{js} + P_s C_{j-sw} \tag{3.4}$$

$$C_{DB} = A_{drain} C_{jd} + P_d C_{j-sw} \tag{3.5}$$

$$C_{B-Sub} = A_{well} C_{jwell} + P_{well} C_{j-well-sw} \tag{3.6}$$

where A_{source}, A_{drain} and A_{well} are the areas, P_s, P_d and P_{well} are the length of the perimeters (P_s, P_d are excluding the side facing the channel), C_{js}, C_{jd} and C_{jwel} are the depletion capacitances per unit area of the

source-to-bulk, drain-to-bulk, and well-to-substrate junctions, respectively. $C_{j\text{-}sw}$ and $C_{j\text{-}well\text{-}sw}$ are the sidewall depletion capacitances per unit length of these three junctions. The value of C_{SB} also involves the channel-to-bulk capacitance whose area is given by $A_{channel}$ (i.e. $A_{channel}=W\times L$).

The depletion capacitances per unit area or per unit length (C_{js}, C_{jd}, C_{jwell}, $C_{j\text{-}sw}$ and $C_{j\text{-}well\text{-}sw}$) have a relationship with the square root of their respective junction voltages, as described in Eq.(3.7),

$$C_j = \frac{C_{j0}}{\sqrt{1-V_{SB}/\phi_j}} \tag{3.7}$$

where the C_{j0} is the depletion capacitance at 0-V bias voltage, whose value depends on the doping densities of the source, drain, well and substrate.

The overall input capacitance of the bulk-driven MOSFET is around 3.8 times that of the gate-driven MOSFET input capacitance (mostly C_{GS}) in a 1μm CMOS process as calculated in [11]. This ratio only decreases by a factor of $\sqrt{S}$, where S is the CMOS technology scaling factor. Considering the inferior bulk transconductance to the gate transconductance, the transition frequency f_t of the bulk-driven MOSFET is much less than that of the gate-driven one, where Eq.(3.8) and Eq.(3.9) reveal both of their expressions:

$$f_{t,bulk-driven} = \frac{g_{mb}}{2\pi\left(C_{SB}+C_{DB}+C_{B-Sub}\right)} \tag{3.8}$$

$$f_{t,gate-driven} = \frac{g_m}{2\pi C_{GS}} \tag{3.9}$$

Fig. 3.3(a) shows one typical application of a bulk-driven PMOS as in a differential pair. The gates of the transistors $MI_{A\text{-}B}$ are biased to the negative power supply to ensure that both devices are operating in saturation region. The subscript A and B represents the two symmetric transistors having the same geometry and may be neglected in the rest of this dissertation for simplicity. Extensive experiments have been done in [11] proving that the input common mode voltage (V_{CM}) can swing almost rail-to-rail

without strongly turning on the bulk-to-source junction diode. This is because while the threshold voltage V_T is reduced with the decreasing V_{CM}, the voltage at the common source terminals of the input pair also moves nearer to the input voltage, which compensates the elevated V_{SB}. As a comparison, the gate-driven differential pair in Fig. 3.3(b) has the limited V_{CM} range due to the high threshold voltage. The maximum V_{CM} in Fig. 3.3(b) is defined by Eq. (3.10) as,

$$\boldsymbol{V}_{\max,\boldsymbol{CM}} = \boldsymbol{V}_{\boldsymbol{DD}} - \boldsymbol{V}_{\boldsymbol{DS},\boldsymbol{sat}(\boldsymbol{M}_{\boldsymbol{TAIL}})} - \boldsymbol{V}_{\boldsymbol{T}} \tag{3.10}$$

where $V_{DS,sat\ (MTAIL)}$ is the onset of saturation voltage for the transistor M_{TAIL}, where ~0.15 V is normally sufficient. In a standard 0.35μm n-well CMOS process, the threshold voltage for a PMOS is ~0.65V in typical corner, thus $V_{max,\ CM}$ of ~0.2V is even difficult to achieve with the 1-V operation.

Another drawback of this bulk-driven input pair is that the ground-connected gate terminals of the input pair will pick up any noise generated by the negative power supply. Therefore, the power supply rejection has poor performance.

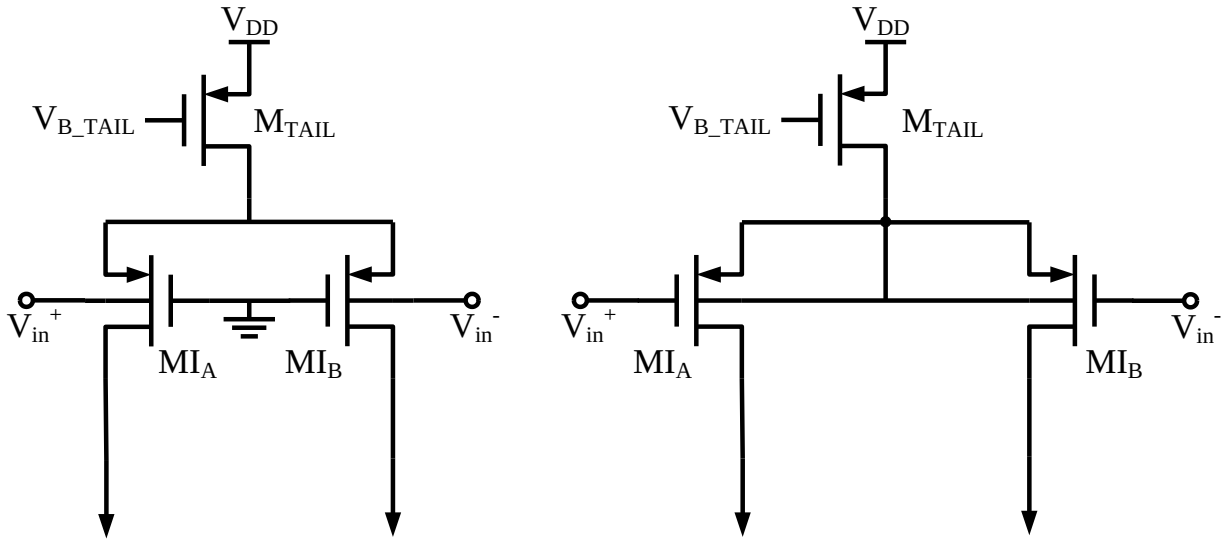

Fig. 3.3 (a) Conventional bulk-driven PMOS differential pair; (b) Simple gate-driven PMOS differential pair.

3.3 Bulk-Driven Amplifier Design Examples in Prior Arts

In recent years, researchers have put their efforts in developing various solutions to the bulk-driven-based low-voltage amplifiers. However, most of the proposed designs focused on either boosting the open loop gain [45]-[49], minimizing the current consumption [50][51], or further scaling down the power supply voltage [12][52][53]. Only a few works provided methods to increase the effective input transconductance ($G_{m\_in\_eff}$) of the bulk-driven amplifiers. Schematics involving the partial positive feedback loop into the input stage have been adopted by most of them.

This work focuses on the increment of the $G_{m\_in\_eff}$ of the bulk-driven amplifier for two reasons:

1). It aims to develop a general purpose bulk-driven low-voltage low-power amplifier with its performance comparable to a gate-driven amplifier, such as open loop gain (A_O), unity gain bandwidth product (UGBW), power consumption, etc.

2). Developing an amplifier with the enhanced $G_{m\_in\_eff}$ helps the development of the chosen potentiostat topology as discussed in the following chapters.

3.3.1 Carillo's Design

The partial positive feedback is first proposed in [54] to improve the transconductance of low-power gate-driven OTAs. It is then utilized in bulk-driven low-voltage OpAmps to boost the low input stage transconductance [55]-[57] .

Fig. 3.4 illustrates the bulk-driven amplifier input stage with enhanced $G_{m\_in\_eff}$ by employing the partial positive feedback. Transistors $MI_{A\text{-}B}$ form the conventional bulk-driven differential pairs with their gates tied to ground, while transistors $MB_{2A\text{-}B,\ 3A\text{-}B,\ 4A\text{-}B}$ are placed such that there is a positive feedback loop working as an active load. The positive feedback loop gain (ξ) is equal to the transconductance ratio of devices $MB_{2A\text{-}B}$ to $MB_{3A\text{-}B}$ (i.e. $g_{m,MB2}/g_{m,MB3}$). In other words, if the ratio $(W/L)MB_{3A\text{-}B}/(W/L)MB_{2A\text{-}B}$ (i.e. equals to ξ) is smaller than unity, the stability of the loop can be assured.

Analysis of this circuit topology shows that the transconductance of this bulk-driven input stage is,

$$G_{m\_in\_eff} = \frac{B}{1-\xi} \times g_{mb,MI} \tag{3.11}$$

where B is gain of current mirrors formed by devices MB_{1A-B} and MB_{2A-B}, and $g_{mb,MI}$ is the bulk transconductance of devices MI_{A-B}.

The circuit configuration proposed in this work successfully boosts the effective input transconductance by $B/(1-\xi)$ times compared to the conventional bulk-driven input stage, where B is due to the current gain. Unfortunately, this partial positive feedback loop increases the impedance at node A by the factor $1/(1-\xi)$ as well, which introduces a non-dominant pole at the node A. This limits the frequency response of the overall amplifier and the maximum $G_{m\_in\_eff}$ enhancement this circuit can achieve.

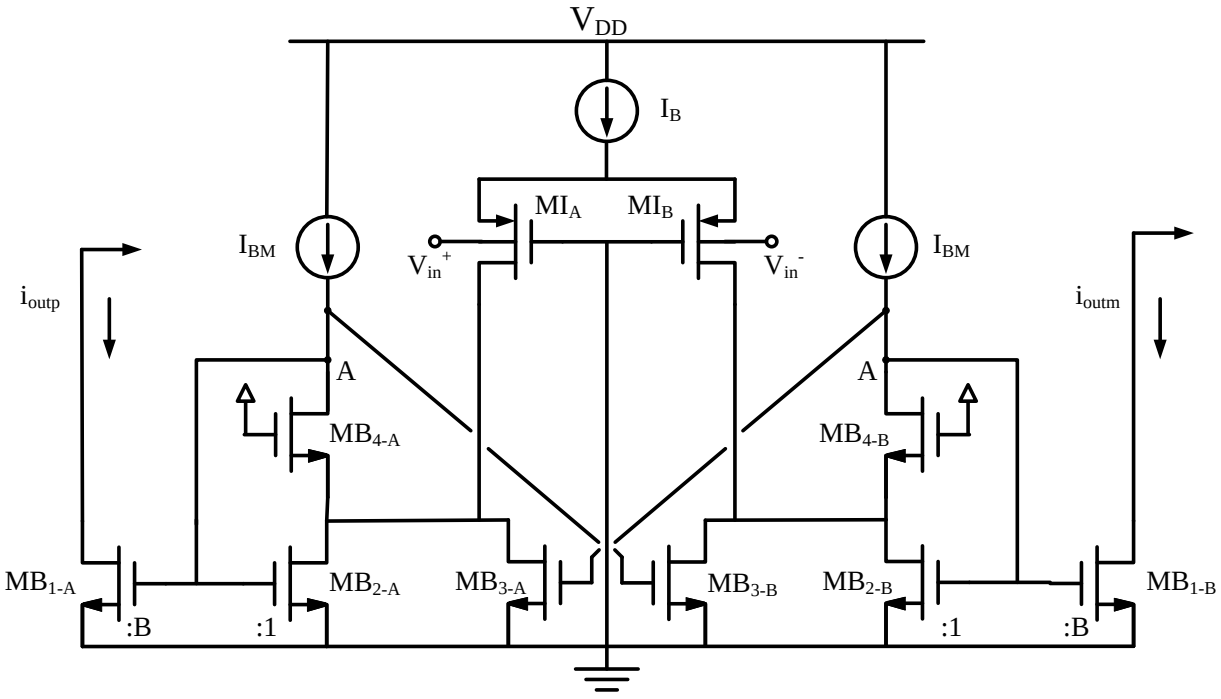

Fig. 3.4 Bulk-driven input stage with transconductance enhancement proposed in [55][56]and [57].

3.3.2 Raikos' Design #1

In [58], G. Raikos et al proposed a modified bulk-driven input stage by employing the positive feedback loop directly into the input differential pair instead of being a part of the active load. Fig. 3.5 exhibits the circuit configuration of this bulk-driven input stage. The positive loop gain is calculated as ξ which is equal to $g_{m,MI}/g_{m,MC1}$. Thus the effective input transconductance is analyzed in the following equation:

$$G_{m\_in\_eff} = g_{mb,MI} \times \frac{1}{1-\xi} \tag{3.12}$$

This bulk-driven input stage achieves similar transconductance enhancement to the previous work. However, its frequency response also suffers from elevated output resistance at the node A. An advantage of importing the partial feedback into the input differential pairs is that the gates are no longer connected to the ground which could avoid any ground noise problem. Consequently, this amplifier has better negative power supply rejection ratio (PSRR-).

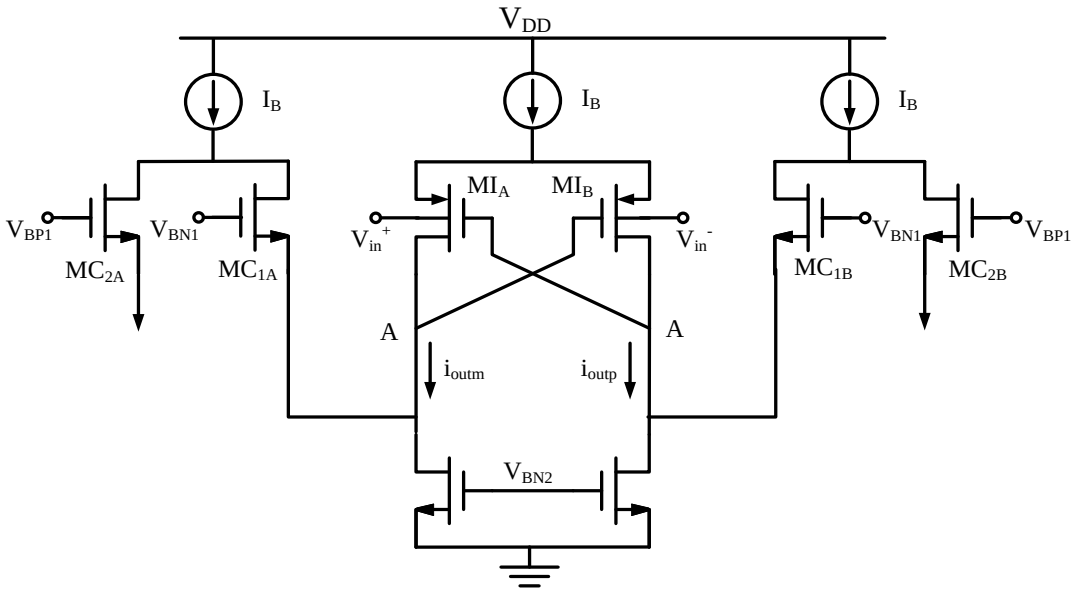

Fig. 3.5 Bulk-driven input stage with transconductance enhancement proposed in [58].

3.3.3 Raikos' Design #2

In order to mitigate the effect of process variations on the transconductance increment circuitry in Fig. 3.5, G. Raikos et al presented an improved version of the bulk-driven input stage described in [59][60] as shown in Fig. 3.6. The source terminals of the input differential pairs in Fig. 3.6 are explicit biased by the source terminal of the transistor MC.

The positive loop gain is calculated as ξ is equal to g_{MI1}/g_{MI2}. Thus the effective input transconductance is analyzed in the following equation:

$$G_{m\_in\_eff} = g_{mb,MI1} \times \frac{2}{1-\xi} \tag{3.13}$$

Since more bulk-driven transistors are involved in the input stage, this topology produces further transconductance enhancement while consuming more power. It has similar advantages and disadvantages as the circuit described in Fig. 3.5.

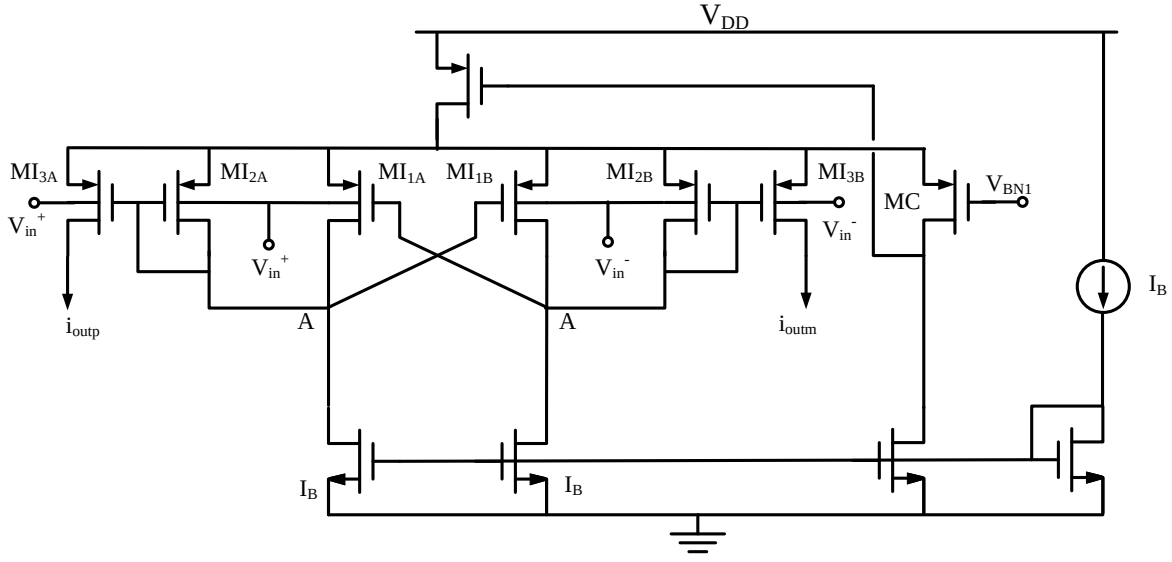

Fig. 3.6 Bulk-driven input stage with transconductance enhancement proposed in [59][60].

3.3.4 Summary of Prior Arts

Table 3.2 summarizes the performance of the bulk-driven amplifiers with input transconductance enhancement presented in prior arts. In summary, the proposed designs in prior arts all have sub 1-V operations. The boosted transconductance in them is mainly determined by the positive feedback loop gain. Once the gain is designed to be close to unity, the effective transconductance can be maximized. However, due to device mismatches and process variations, a loop gain that is too close to unity could cause serious stability issues inside the input stage because of the positive feedback. Therefore, the effective enhanced transconductance in these works is mostly less than eight times of that of the conventional bulk-driven amplifier.

In addition, the impedance at the output node of the positive feedback loop is boosted by the loop gain as well. The non-dominant pole associated with it degrades the frequency response of the amplifier, which is another limitation to the achievable transconductance.

Table 3.2 Performance Summary of the Amplifiers in Prior Arts

References	**[55]**	**[56]**	**[58]**	**[59][60]**
Process	0.35 µm standard nwell CMOS	0.35 µm standard nwell CMOS	0.18 µm standard nwell CMOS	0.35 µm standard nwell CMOS
Simulation/Measurement	Simulation	Measurement	Simulation	Simulation
Topology	Single ended OTA	Single ended OpAmp	Fully differential OpAmp	Fully differential OpAmp
Load	15 pF	1 MΩ // 17 pF	20 pF	16 KΩ//20 pF
V_{DD}	1-V	1-V	0.8-V	1-V
Theoretically $G_{m\_in\_eff}$ enhancement	4 (w/o current gain)	3 (w/o current gain)	6.58	8
Input stage current consumption (µA)	90 (w/o current gain)	53 (w/o current gain)	40	40
Achieved $G_{m\_in\_eff}$(µA/V)	N/A	763 (w/ current gain)	240	80
Current consumption ratio of input stage w/ and w/o $G_{m\_in\_eff}$ enhancement	1.8	2.12	2	2.5
Amplifier power consumption (µW)	200	358	100	130
Input current (nA)	N/A	2.15	N/A	< 10
SR+/SR- (V/ µs)	8.9/8.3	2.74/5.02	N/A	0.7
Open loop gain (dB)	41.7	76.2	56	55
Unity gain bandwidth (MHz)	10	8.1	3.2	1.6
Phase margin	58˚	60˚	45˚	36˚
Input offset (mV)	N/A	-2.88±1.26 (Vos±σ)	36 (3σ)	10 (σ)
Input referred noise (nV/$\sqrt{Hz}$)	461 @ 1KHz	903 @ 1KHz	408 @ 10 KHz	160 @ 100 KHz
CMRR (dB)	N/A	70.5 @DC	100 @ 5KHz	68 @100 KHz
PSRR± (dB)	N/A	45 /40.5 @DC	88 @ 10KHz	70 @ 10KHz

CHAPTER 4

DESIGN OF THE BULK-DRIVEN OPERATIONAL AMPLIFIER (OPAMP) WITH IMPROVED TRANSCONDUCTANCE

In this chapter, a biasing circuitry for the bulk-driven input differential pair is first proposed in Section 4.1. This biasing circuitry can also act as an auxiliary amplifier which doubles the original bulk-driven input transconductance g_{mb}. In Section 4.2, an improved version of this auxiliary amplifier is proposed to boost the effective input transconductance ($G_{m\_in\_eff}$) even more. In the end, a general purpose low-voltage bulk-driven OpAmp is presented with the innovative input stages. The performance of the input stage alone and the OpAmp are also discussed in detail in this chapter.

4.1 Low-Voltage Bulk-Driven Input Stage and Its Cascode Bias Circuit

Fig. 4.1 illustrates the schematic of the first proposed bulk-driven input stage. In this circuit, transistors $MI_{A,B}$ and $ME_{A,B}$ consist of the input stage core circuit, of which, transistors $MI_{A,B}$ operate similarly to the conventional bulk-driven differential pair shown in Fig. 3.3 (a) except that their gates are cross-biased by $ME_{B,A}$, respectively.

4.1.1 Biasing Circuitry

The biasing circuitry formed by transistors $ME_{A,B}$, $MB_{1,2,3,4}$ and $MC_{1,2}$ is a modified version of the

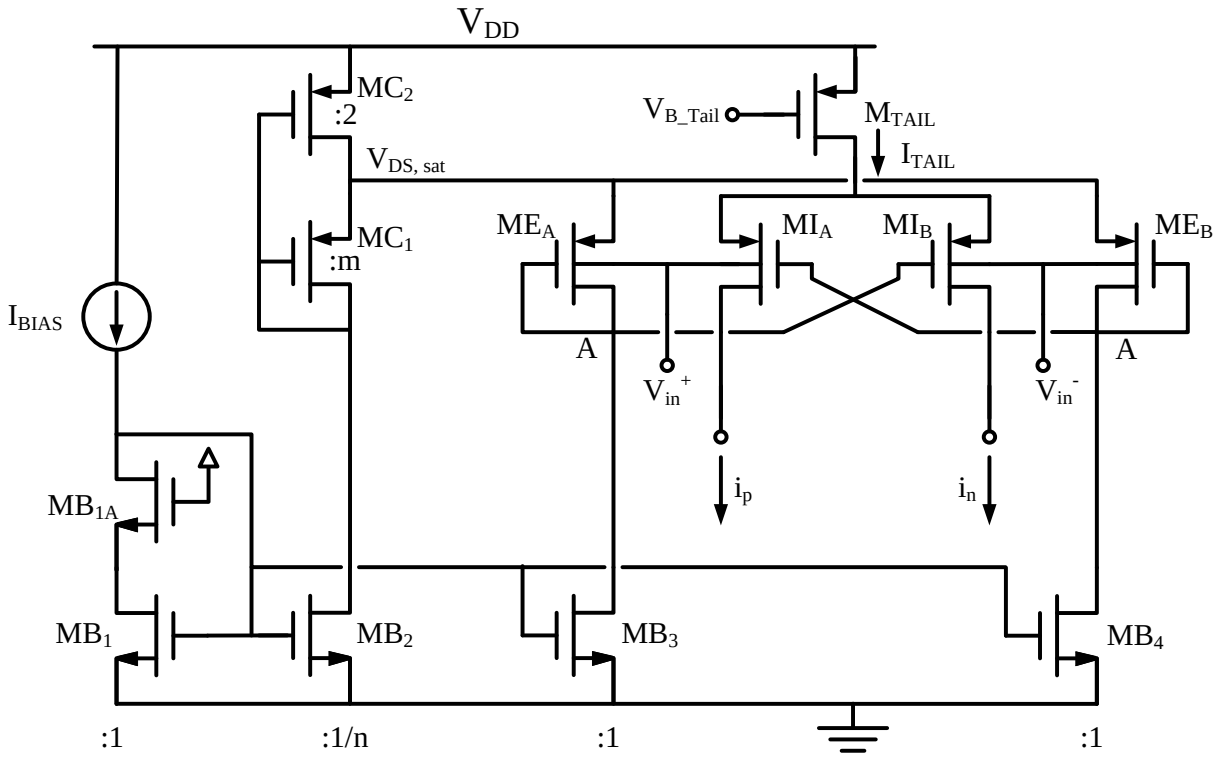

Fig. 4.1 Proposed input stage with modified low-voltage cascode biasing.

topology first proposed in [61] which is based in EKV models. In EKV MOS transistor models, the overall current I_{tot} flowing through one single transistor is the difference of the forward ($I_{Forward}$) and the reverse ($I_{Reverse}$) channel currents, where $I_{Forward}$ is controlled by the gate-to-source voltage and $I_{Reverse}$ is controlled by the gate-to-drain voltage [62]. Both of the equations can be expressed by Eq.(4.1) as,

$$\boldsymbol{I_{Forward(Reverse)} = \frac{W}{L} I_S \log^2\left(1+e^{\left(\kappa(V_G - V_{TH0}) - V_{S(D)}\right)/2U_T}\right)} \tag{4.1}$$

where U_T is thermal voltage; I_s is given by $I_s = 2\mu C_{ox} U_T^2/\kappa$, and κ is the reciprocal of the sub-threshold slope factor. The onset saturation voltage $V_{DS,sat}$ of a MOS transistor is expressed using $I_{Forward}$ and $I_{Reverse}$ in [61] as expressed by Eq. (4.2),

$$V_{DS,sat} = 2U_T \log\left(\frac{e^{\sqrt{I_{Forward}/(W/L)I_s}} - 1}{e^{\sqrt{I_{Reverse}/(W/L)I_s}} - 1}\right) \tag{4.2}$$

If $I_{Forward} >> I_{Reverse}$, an onset saturation voltage $V_{DS,sat}$ can be generated no matter how much current is flowing through the device.

The ratio of $I_{Forward}$ to $I_{Reverse}$ in transistor MC_2 is analyzed in Appendix A.1 and expressed by,

$$\frac{I_{Forward,MC_2}}{I_{Reverse,MC_2}} = 1 + \frac{m}{2}(1 + 2n) \tag{4.3}$$

If the values of m and n are properly chosen (e.g. m = 4, n = 4), the forward current will be much larger than the reverse current, where a $V_{DS,sat}$ can be expected across the drain-to-source terminals of transistor MC_2 independent of the biasing current flowing through it. As a result, the gate voltages of $ME_{A,B}$, which are one diode drop below $V_{DS,sat}$, can be used to bias the gates of the input pair $MI_{A,B}$. For accurate biasing, transistors inside the biasing circuitry, such as $MI_{A,B}$ and $ME_{A,B}$, have identical channel lengths, and their overdrive voltages V_{OV} (i.e. $V_{OV} = V_{GS}-V_T$) are designed to be the same. This is also the case for the transistors MC_2 and M_{TAIL}, where the gate voltage V_{B_Tail} of M_{TAIL} is biased at the same level as that of MC_2.

According to $g_m = I_D/(V_{GS}-V_T)$ and the previous Eq. (3.3), the gate and bulk transconductance ratio of transistors MI to ME is equal to $I_{DS,MI}/I_{DS,ME}$ (i.e. $I_{DS,MI}/I_{DS,ME} = g_{mb,MI}/g_{mb,ME} = g_{m,MI}/g_{m,ME}$).

4.1.2 Enhanced Effective Input Transconductance $G_{m\_in\_eff}$

The cross-biased devices ME_A and ME_B also form one auxiliary differential pair whose outputs can modulate the gates of the transistors $MI_{A,B}$. In this way, both the bulk and the gate terminals of $MI_{A,B}$ are modulated directly or indirectly by the input signals. Small signal equivalent circuit of this input stage is analyzed without considering the second-order effect of MOS devices such as their output resistance. The effective input transconductance ($G_{m\_in\_eff}$) is given by,

$$G_{m\_in\_eff}(s) = \frac{g_{mb,ME}}{g_{m,ME}} \bullet g_{m,MI} \bullet \frac{1}{1 + \frac{s}{g_{m,ME}/C_A}} + g_{mb,MI} \tag{4.4}$$

where $g_{mb,MI}$, $g_{mb,ME}$ are the bulk transconductance of transistors MI and ME, $g_{m,MI}$ is the gate transconductance of transistors MI. There is also a non-dominant pole associated with the node A in Fig. 4.1. C_A is the parasitic capacitance at this node, where the gate-to-source capacitances (C_{GS}) of both transistors ME and MI contribute to most of this parasitic capacitance. According to Eq.(3.3), since the transistors ME and MI possess the same source-to-bulk voltage, the ratio of $g_{mb,ME}$ to $g_{m,ME}$ is equal to that of $g_{mb,MI}$ to $g_{m,MI}$. Thus at DC, the effective transconductance can be further simplified in Eq.(4.5),

$$G_{m\_in\_eff,DC} = 2 \times g_{mb,MI} \tag{4.5}$$

It can be concluded that the DC value of the $G_{m\_in\_eff}$ is doubled irrespective of the g_m or g_{mb} of the auxiliary differential pair.

In frequency domain, however, one zero-and-pole doublet (z_A and p_A, both located at the left half plane) is introduced because there are two signal paths between the input signal node and the output of the circuit. The doublet can be expressed as,

$$z_A = -\frac{2g_{m,ME}}{C_A},\ p_A = -\frac{g_{m,ME}}{C_A} \tag{4.6}$$

Fortunately, the zero and pole can cancel each other to a degree in the Bode plot since they are fairly close. However, a low frequency doublet does degrade the transient response of the overall circuit. Thus, they are preferred to be pushed away from the bandwidth of interest [63], which also means that the transconductance of the transistors ME cannot be designed to be too small.

4.1.3 Common-Mode Voltage Gain and ICMR

The input common mode gain A_{CM} is also reduced due to this biasing topology. Since it cannot be intuitively noticed from the schematic, the expression of A_{CM} is given in Eq. (4.7) with proper

approximations as,

$$A_{CM} \approx \frac{g_{mb,MI} \times R_{out}}{1+g_{mb,MI} \times R_{TAIL}} - \frac{g_{mb,MI} \times R_{out}}{1+g_{m,MI} \times R_{TAIL}} \tag{4.7}$$

where R_{OUT} is the output resistance of the proposed input stage and R_{TAIL} is the output resistance of the tail transistor M_{TAIL}. Obviously, the first term is equal to the input common mode gain of a conventional bulk-driven input stage and the second term results from another common mode signal path from the auxiliary differential pair. According to Eq. (3.3) and the aforementioned ratio of g_{mb} to g_m (0.2~0.4), A_{CM} can be decreased by 20% to 40% compared with that of conventional topology.

One concern regarding the proposed input stage is the relatively limited input common mode range (ICMR) compared to the conventional one. Since the source-to-bulk junction of MOSFET can be reverse biased, the maximum V_{CM} can be moved toward V_{DD} by carefully sizing the transistors such that the elevated threshold voltage of MI will not push M_{TAIL} and $MB_{3,4}$ out of saturation. The lower limit of V_{CM}, nevertheless, is constrained by the turn-on voltage of the forward biased source-to-bulk junction, and it can be given by,

$$V_{CM,\min} = V_{DD} - \left|V_{DS,sat,MC_2}\right| - V_{forward} \tag{4.8}$$

where $V_{forward}$ is the diode turn-on voltage of a PMOS device. According to measurements, the voltage drop smaller than 0.55 V for $V_{forward}$ is a good practice for keeping the input bias current of the circuit within tens of nano-amperes.

4.2 Modified Bulk-Driven Input Stage with Improved Input Transconductance

4.2.1 Modified Bulk-Driven Input Stage Structure

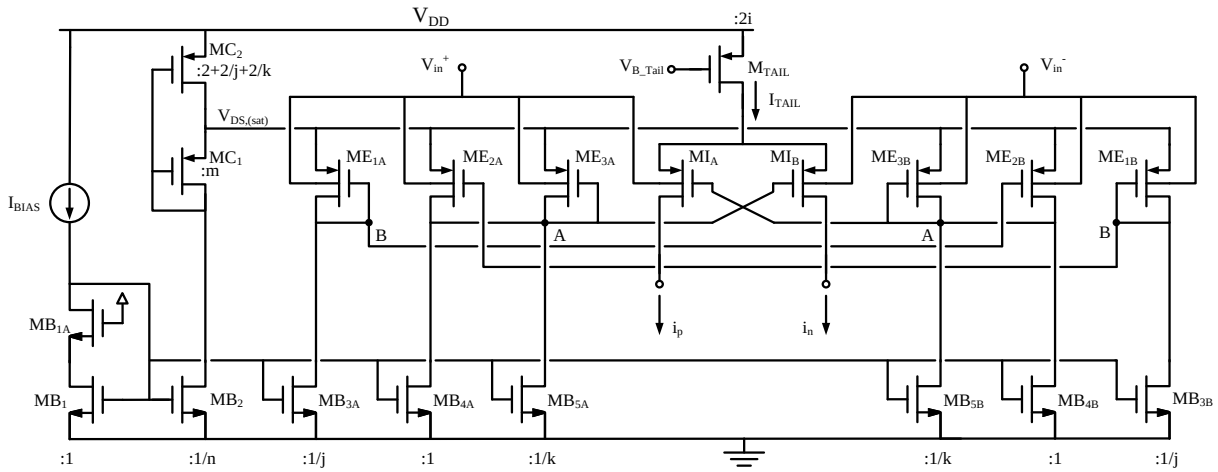

Fig. 4.2 Improved structure based on the circuit in Fig. 4.1.

An improved version of the input stage topology is proposed, as described in Fig. 4.2 to achieve even more effective input transconductance $G_{m\_in\_eff}$ with a similar biasing scheme. The basic idea is to use more auxiliary differential pairs to improve the voltage gain from the differential inputs to the gates of transistors $MI_{A\text{-}B}$. As a result, the transistors ME_{1A}, ME_{2B} and ME_{1B}, ME_{2A} form another cross biasing scheme, where both the gate and the bulk terminals of $ME_{2A\text{-}B}$ are modulated. Similar to the previous structure, all input pairs possess the same channel lengths while their widths are scaled according to their drain-to-source current (I_{DS}) to keep the overdrive voltage V_{OV} of each transistor the same.

The core input differential pair $MI_{A\text{-}B}$ are designed with drain currents being i times of those of the transistors $ME_{2A\text{-}B}$ (i.e. $i = I_{DS,MI}/I_{DS,ME2} = g_{mb,MI}/g_{mb,ME2} = g_{m,MI}/g_{m,ME2}$). In order to save additional power and transistor counts, the drain current and the transconductance of $ME_{1A\text{-}B}$ can as well be scaled j times smaller than that of $ME_{2A\text{-}B}$ (i.e. $j = I_{DS,ME2}/I_{DS,ME1} = g_{mb,ME2}/g_{mb,ME1} = g_{m,ME2}/g_{m,ME1}$), since it is indicated in Eq. (4.5) that the effective transconductance is simply double the value of $g_{mb,ME2}$ regardless of the value of j. The diode-connected PMOS transistors $ME_{3A\text{-}B}$ are employed to increase the impedance at the node A in Fig. 4.2 by scaling their drain currents k times smaller than that of the transistors $ME_{2A\text{-}B}$. This also means the gate or the bulk transconductance ratio ($g_{m,ME2A\text{-}B}/g_{m,ME3A\text{-}B}$ or $g_{mb,ME2A\text{-}B}/g_{mb,ME3A\text{-}B}$) is

equal to the value *k*. In addition, the voltage gain can be further improved by connecting the bulk terminals of ME_{3A-B} to the input signals.

The ratio of $I_{Forward}$ to $I_{Reverse}$ of the transistor MC_2 in this improved version of the bulk-driven input stage is calculated in Appendix A.1 using the parameters *m*, *n*, *j*, *k*. The final expression is in Eq.(4.9),

$$\frac{\boldsymbol{I_{Forward,MC_2}}}{\boldsymbol{I_{Reverse,MC_2}}} = 1 + \frac{\boldsymbol{m}}{2}\left(\frac{1}{1+1/\boldsymbol{j}+1/\boldsymbol{k}} + 2\boldsymbol{n}\right) \tag{4.9}$$

4.2.2 Enhanced Effective Input Transconductance $G_{m\_in\_eff}$

Neglecting any output resistance of the MOS devices, the effective input transconductance $G_{m\_in\_eff}$ is deducted in Appendix A.2 as,

$$\boldsymbol{G_{m\_in\_eff}}(\boldsymbol{s}) = \boldsymbol{g_{mb,MI}} \frac{2\boldsymbol{k}+1+(\boldsymbol{k}+1)\dfrac{\boldsymbol{s}}{\boldsymbol{g_{m,ME1}}/\boldsymbol{C_B}}}{\left(1+\dfrac{\boldsymbol{s}}{\boldsymbol{g_{m,ME1}}/\boldsymbol{C_B}}\right)\left(1+\dfrac{\boldsymbol{s}}{\boldsymbol{g_{m,ME3}}/\boldsymbol{C_A}}\right)} + \boldsymbol{g_{mb,MI}} \tag{4.10}$$

where $g_{m,ME1}$ and $g_{m,ME3}$ are the gate transconductance of transistors ME_1 and ME_3; $g_{mb,MI}$ is the bulk transconductance of MI, *k* is the parameter which is equal to $g_{m,ME2}/g_{m,ME3}$ or $g_{mb,ME2}/g_{mb,ME3}$, C_A and C_B are the parasitic capacitances associated with the nodes A and B in Fig. 4.2, and are expressed in Eq.(4.11) and Eq.(4.12),

$$\boldsymbol{C_A} = \boldsymbol{C_{GS,ME3}} + \boldsymbol{C_{GS,MI}} + \boldsymbol{C_{DS,ME2}} \tag{4.11}$$

$$\boldsymbol{C_B} = \boldsymbol{C_{GS,ME2}} + \boldsymbol{C_{GS,ME1}} + \boldsymbol{C_{DS,ME1}} \tag{4.12}$$

At DC, the $G_{m\_in\_eff}$ is simply,

$$\boldsymbol{G_{m\_in\_eff}} = (2\boldsymbol{k}+2)\,\boldsymbol{g_{mb,MI}} \tag{4.13}$$

Clearly, similar to the first proposed input stage, the transconductance does not depend on the g_m

or g_{mb} values of the auxiliary differential pairs ME_1, ME_2, ME_3 without considering any frequency dependent components or second-order effects. Hence minimizing them by downsizing the aspect ratios and the drain-to-source currents (I_{DS}) of these devices will improve the input stage performance from the power consumption point of view. As a determinant factor of this transconductance enhancement methodology, the value k can also be designed relatively large by further scaling down the g_m of the transistors ME_3.

Nevertheless, the zero-pole doublets associated with the nodes A and B ($z_{A,B}$ and $p_{A,B}$) can be found in Eq. (4.14) and Eq. (4.15) as,

$$z_{A,B} = -\frac{g_{m,ME3}}{C_A}\frac{k+2}{2} - \frac{g_{m,ME1}}{2C_B} \pm \frac{1}{2}\sqrt{\left(\frac{g_{m,ME3}}{C_A}\right)^2 (k+2)^2 + \left(\frac{g_{m,ME1}}{C_B}\right)^2 - (6k+4)\frac{g_{m,ME1}}{C_B}\cdot\frac{g_{m,ME3}}{C_A}} \tag{4.14}$$

$$p_A = -\frac{g_{m,ME3}}{C_A} \quad p_B = -\frac{g_{m,ME1}}{C_B} \tag{4.15}$$

For simplifying the analysis, the g_m of the transistors ME_1 and ME_3 is normalized to that of the core input pair MI since their drain currents (I_{TAIL}) are usually determined according to the specifications of the OpAmp. In the meantime, the capacitances of C_A and C_B are normalized to $C_{GS,MI}$ (gate-to-source capacitances of the transistors MI). The normalizations are both performed in Appendix A.3. To rather not complicate the circuit design procedure, the drain-to-source currents of the transistors ME_1 and ME_3 are designed to be the same, indicated by the parameter j to be equal to k.

In Table 4.1 and Table 4.2, the normalized frequencies of the zeros $z_{A,B}$ and the poles $p_{A,B}$ are calculated based on various values of parameters i and k. Conclusions can be drawn that only when i is equal to 1, the frequencies of both zeros stay in real value, where z_B decreases as k increases, and z_A is unchanged. However, as the parameters i and k increase, the location of the pole p_A moves close to lower frequencies while the pole p_B only decreases with increment of parameter k. Several tradeoffs can be

Table 4.1 Normalized Frequencies of the Zeros $z_{A,B}$

Normalized $z_{A,B}$ *i* / *k*	1	2	3	4	5
1	1.00,1.00	0.75 ±0.32i	0.63 ±0.33i	0.55 ±0.31i	0.50 ±0.29i
2	1.00,0.67	0.57 ±0.28i	0.45 ±0.28i	0.39 ±0.27i	0.35 ±0.25i
3	1.00,0.50	0.48 ±0.23i	0.37 ±0.24i	0.32 ±0.23i	0.28 ±0.21i
4	1.00,0.40	0.43 ±0.19i	0.33 ±0.21i	0.28 ±0.20i	0.24 ±0.19i
5	1.00,0.33	0.40 ±0.14i	0.30 ±0.18i	0.25 ±0.18i	0.22 ±0.17i

Table 4.2 Normalized Frequencies of the Poles $p_{A,B}$

Normalized $p_{A,B}$ *i* / *k*	1	2	3	4	5
1	0.50, 0.50	0.33, 0.50	0.25, 0.50	0.20, 0.50	0.17, 0.50
2	0.33, 0.33	0.20, 0.33	0.14, 0.33	0.11, 0.33	0.09, 0.33
3	0.25, 0.25	0.14, 0.25	0.10, 0.25	0.08, 0.25	0.06, 0.25
4	0.20,0.20	0.11, 0.20	0.08, 0.20	0.06, 0.20	0.05, 0.20
5	0.17, 0.17	0.09, 0.17	0.06, 0.17	0.05, 0.17	0.04, 0.17

noted for optimizations of the values of *i* and *k* given that I_{TAIL} is kept constant:

1) The increment of *k* enhances the input transconductance $G_{m\_in\_eff}$ while a smaller value of *i* leads to more power consumption.
2) To achieve an optimal transient response when being employed in the overall OpAmp design, the non-dominant poles $p_{A,B}$ of the proposed input stage are favored to be pushed further away to high frequencies. The frequencies of the zeros $z_{A,B}$ have similar requirements, and can be

used to cancel the non-dominant poles.

Apart from these tradeoffs, larger tail current I_{TAIL} can always be dumped into transistors MI such that these non-dominant poles and zeros are pushed outside the bandwidth of interest, while at the cost of the increased power consumption and $G_{m\_in\_eff}$. In addition, these unwanted non-dominant poles and zeros can be compensated by use of the short channel devices to minimize parasitic capacitances C_A and C_B, although the minimum channel length of these transistors is limited by the matching considerations.

4.2.3 Input Referred Noise

The input referred noise for the bulk-driven MOSFET is usually worse than the gate-driven ones due to the smaller input transconductance but the same noise sources. Neglecting the thermal noise contribution of the series gate and bulk resistances, the noise contributions of the transistors MI, $ME_{1,2,3}$ and $MB_{3,4,5}$ at the input stage are calculated in Appendix A.4. Then the input referred thermal noise and the flicker noise expressions for the bulk-driven input stage in Fig. 4.2 are derived as,

$$\overline{V_{n,th}^2} \approx 4k_B T\gamma \times \frac{g_{m,MI}^2}{\left((2k+2)g_{mb,MI}\right)^2} \times \frac{1}{g_{m,ME3}^2} \times \left(\frac{g_{m,ME2}^2 3}{g_{m,MI}} + \frac{g_{m,ME2}^2}{g_{m,ME1}} + g_{m,ME2} + g_{m,ME3} + g_{m,MB3}\frac{g_{m,ME2}^2}{g_{m,ME1}^2} + g_{m,MB4} + g_{m,MB5} \right) \tag{4.16}$$

$$\overline{V_{n,1/f}^2} \approx \frac{g_{m,MI}^2}{\left((2k+2)g_{mb,MI}\right)^2} \times \frac{1}{g_{m,ME3}^2} \times \left(\frac{g_{m,ME3}^2}{W_{MI}L_{MI}} + \frac{g_{m,ME2}^2}{W_{ME1}L_{ME1}} + \frac{g_{m,ME2}^2}{W_{ME2}L_{ME2}} + \frac{g_{m,ME3}^2}{W_{ME3}L_{ME3}} + \frac{g_{m,MB3}^2}{W_{MB3}L_{MB3}}\frac{g_{m,ME2}^2}{g_{m,ME1}^2} + \frac{g_{m,MB4}^2}{W_{MB4}L_{MB4}} + \frac{g_{m,MB5}^2}{W_{MB5}L_{MB5}} \right) \times \frac{K_f}{C_{ox}^2}\frac{1}{f} \tag{4.17}$$

where k_B is the Boltzmann constant, T is the temperature, γ is the gamma noise factor, K_f is the process dependent flicker noise constant. It is obvious that the auxiliary differential pairs have great contributions to the total input referred thermal and flicker noise. However, the enhanced $G_{m\_in\_eff}$ attenuates them by

(2 *k*+2) times. One effective way to minimize the thermal noise is to increase the current consumption of the auxiliary amplifiers, while enlarging the transistors sizes will achieve better flicker noise performance.

4.2.4 Mismatch and Offset Voltage

In the square law equation shown in Eq. (3.1) without considering channel length modulation, the threshold voltage at zero substrate voltage V_{THP0}, the current factor $\beta = C_{ox}\mu W/L$ and the constant γ_P are the sources of substantial random mismatches in the MOSFET. The commonly accepted standard deviations of these three parameters of the long channel transistor are expressed in [64] which are also listed in Eqs. (4.18), (4.19) and (4.20) as shown below,

$$\sigma^2\left(V_{THP0}\right) = \frac{A^2_{V_{THP0}}}{WL} + S^2_{V_{THP0}} D^2 \tag{4.18}$$

$$\sigma^2\left(\gamma_P\right) = \frac{A^2_{\gamma_P}}{WL} + S^2_{\gamma_P} D^2 \tag{4.19}$$

$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{A^2_{\beta}}{WL} + S^2_{\beta} D^2 \tag{4.20}$$

where A_{VTHP0}, $A\gamma$ and A_β are the area proportionality constant for each parameter, S_{VTHP0}, S_γ and S_β are the variations of each parameter with the spacing D between two devices. The second terms in these equations are relatively small compared to the first terms [64].

Sources of random mismatches inside the proposed bulk-driven input stage are introduced by the four input transistor pairs and the biasing transistors M_{TAIL} and $MB_{3,4,5}$. The mismatches from M_{TAIL} and $MB_{3,4,5}$ result in the mismatches between the biasing current fed to the four input differential pairs. Their expressions are similar to other conventional OpAmps and therefore are not calculated in this work.

As for the mismatches between the bulk-driven input pairs, it is very difficult to completely analyze their offset voltage (V_{offset}). However, all the bulk-driven input transistors can be considered as one basic bulk-driven input pair as shown in Fig. 3.3 (a) and the overall transconductance can be assumed

to be $(2k+2)\ g_{mb,MI}$. The offset voltages due to the mismatches of V_{THP0}, β and γ_P respectively are shown in Eqs. (4.21), (4.22) and (4.23),

$$V_{offset,V_{THP0}} = \frac{2\sqrt{2\phi_F + V_{BS}}}{(2k+2)\gamma_P}\Delta V_{THP0} \tag{4.21}$$

$$V_{offset,\gamma_P} = \frac{2\sqrt{2\phi_F + V_{BS}}}{(2k+2)\gamma_P} g_{m,MI}\left(\sqrt{2\phi_F + V_{BS}} - \sqrt{2\phi_F}\right)\Delta\gamma_P \tag{4.22}$$

$$V_{offset,\beta} = \frac{\Delta\beta}{\beta}\frac{I_D}{g_{m,MI}}\frac{2\sqrt{2\phi_F + V_{BS}}}{(2k+2)\gamma_P} \tag{4.23}$$

Combining Eqs. (4.21), (4.22) and (4.23) and substituting the variables from Eqs.(4.18), (4.19) and (4.20), the standard deviation of the offset voltage for the proposed 1-V bulk-driven input stage can be expressed in Eq.(4.24) as,

$$\begin{aligned}\sigma^2\left(V_{offset}\right) = &\left(\frac{A^2_{V_{THP0}}}{WL} + S^2_{V_{THP0}}D^2\right)\left(\frac{\sqrt{2\phi_F + V_{BS}}}{(k+1)\gamma_P}\right)^2 \\ &+\left(\frac{A^2_{\gamma_P}}{WL} + S^2_{\gamma_P}D^2\right)\left(\frac{\sqrt{2\phi_F + V_{BS}}}{(k+1)\gamma_P} g_{m,MI}\left(\sqrt{2\phi_F + V_{BS}} - \sqrt{2\phi_F}\right)\right)^2 \\ &+\left(\frac{A^2_{\beta}}{WL} + S^2_{\beta}D^2\right)\left(\frac{I_D}{g_{m,MI}}\frac{\sqrt{2\phi_F + V_{BS}}}{(k+1)\gamma_P}\right)^2\end{aligned} \tag{4.24}$$

Obviously, since constant biasing current is either sourcing or sinking the input differential pairs, the gate transconductance g_m is kept constant irrespective of the changes of the input voltage. Thus, the standard deviation of the offset voltage for the bulk-driven input pair increases as the bulk-to-source voltage (i.e. V_{BS}, also the input common mode voltage since the source terminal voltages of the input pairs are fixed.) increases. With increased parameter k and width and length of the input pairs, the standard

deviation also gets smaller.

Overall, compared with the input stage proposed in the previous section, the circuit in Fig. 4.2 still possesses the similar advantages and disadvantages, except that it manages to improve the effective transconductance by ($2 \cdot k$ +2) times at the expense of a few more transistors at the input stage.

4.3 1-V Operational Amplifier Prototype Implementation

4.3.1 1-V OpAmp Schematic Design

A 1-V bulk-driven general purpose operational amplifier is implemented on a 0.35 μm standard n-well CMOS process. It has employed the proposed transconductance enhanced input stage in Fig. 4.2, a folded cascode second stage and a class-AB output stage which uses level shift low-voltage design technique to accommodate 1-V operation. The schematic of the OpAmp is shown in Fig. 4.3. The bias current for the overall circuit is provided by a single external current source set to 2.5 μA. The node V_{B_TAIL} is biased so that 10 μA tail current is supplied to the core differential pair $MI_{A\text{-}B}$.

In order to have maximum input transconductance, while still keeping the non-dominant pole-zero doublets at higher frequencies and moderate power consumption for the input stage, relatively large aspect ratios are chosen for all input differential pairs. Another object of this design is to keep the consequent V_{SG} small which leaves more room for the transistors $MB_{3,4,5}$ to be biased into saturations even at high input voltages. The gate transconductance of ME_1 and ME_3 is designed to be one fourth of the g_m of the core input differential pair MI and the transconductance ratios j, k are then selected to be equal to 4. In addition, the currents flowing through devices MI are set to be the same as the drain currents of devices ME_3 (i.e. i = 1). Theoretically, the effective transconductance ($G_{m\_in\_eff}$) can be expected to be ten times that of the conventional bulk-driven amplifier (i.e. g_{mb}). To further improve frequency response, relatively short channel length is selected for the input stage transistors (MI, ME_1, ME_2, and ME_3). A saturation voltage around 200 mV is designed to be across MC_2. The overall current consumption of this input stage

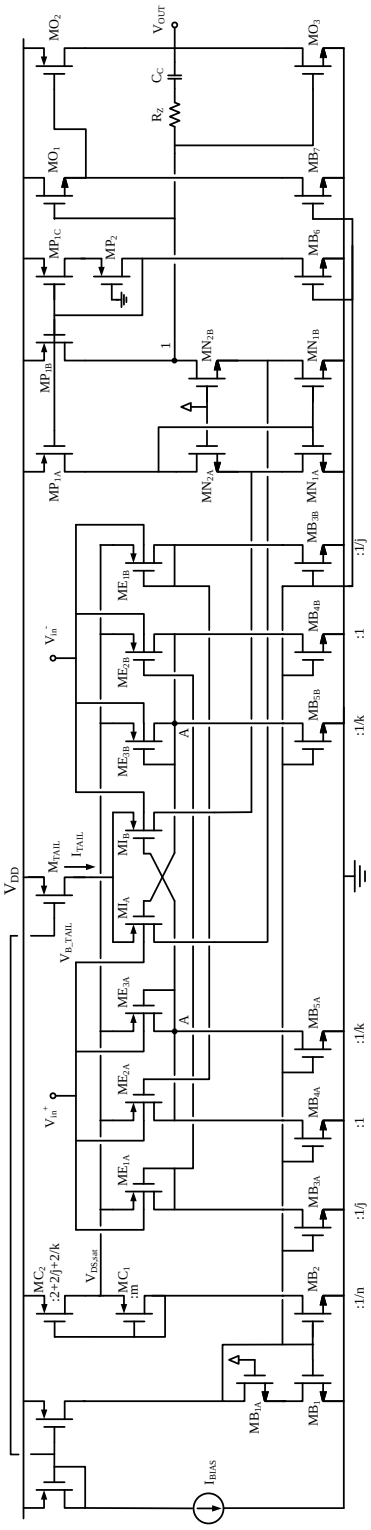

Fig. 4.3 Schematic of the 1-V operational amplifier.

is about 25μA, which is 2.5 times that of the standalone bulk-driven input stage without any enhancement.

The proposed bulk-driven input stage is connected to a folded cascode stage formed by transistors MN_{1A-B}, MN_{2A-B} and MP_{1A-B}. The impedance at node 1 is formed by the output resistance of cascode NMOSs and one single PMOS in parallel. To compensate this impedance imbalance, the channel lengths of the PMOSs MP_{1A-B} are designed to be much longer than those of the NMOSs MN_{1A-B} and M_{N2A-B}. Transistors MO_2 and MO_3 with large *W*/*L* ratios form one push-pull output stage to supply a sufficient amount of current to the load. To accommodate the limited power supply, one NMOS level shifter MO_1 is placed between the output of the second stage and the input of the PMOS MO_2. However, since the bulk terminal of MO_1 has to be tied to the negative power supply, the voltage drop across the level shifter is increased due to the elevated threshold voltage, which will potentially bring current source transistor MB_7 out of saturation and lower the overall output stage gain. Therefore, MO_1 is sized with large *W*/*L* ratio in order to keep its gate-to-source voltage small. The detailed aspect ratios of the main transistors in Fig. 4.3 are given in Table 4.3.

Table 4.3 Transistors Aspect Ratio of the OpAmp in Fig. 4.3

Transistor	***W*/*L* (μm/μm)**	**Transistor**	***W*/*L* (μm/μm)**	**Transistor**	***W*/*L* (μm/μm)**
MI	54.4/0.5	**MB_2**	2/1	**MN_2**	9.6/0.8
ME_1	13.6/0.5	**$MB_{3,5}$**	2/1	**$MP_{1A,B}$**	34.4/2.4
ME_2	54.4/0.5	**MB_4**	8/1	**MP_{1C}**	17.2/2.4
ME_3	13.6/0.5	**MC_1**	244.8/2.4	**MO_1**	64/0.5
M_{TAIL}	108.8/2.4	**MC_2**	163.2/2.4	**MO_2**	252/0.8
MB_1	4/1	**MN_1**	6.8/1.2	**MO_3**	50.4/0.8

4.3.2 Open Loop Gain A_O and Frequency Response of the 1-V OpAmp

The open loop gain A_O for this 1-V bulk-driven OpAmp is calculated as,

$$A_0 \approx (2k+2)\, g_{mb,MI} \times \left(r_{o,MN1} g_{m,MN2} r_{o,MN2} \,\|\, r_{o,MP1}\right) \times \left(g_{m,MO3} + g_{m,MO2}\right)\left(r_{o,MO3} \,\|\, r_{o,MO2}\right) \quad (4.25)$$

which includes the gain from the input stage, the cascode stage and the output stage, respectively. Here, r_o is the output resistance of the corresponding transistor.

A capacitor C_C is placed inside the output stage to establish the dominant pole which is associated with the node 1 in Fig. 4.3. Its frequency is pushed to a lower value due to "Miller effect" of the capacitor C_C and is derived as,

$$p_1 \approx -\frac{1}{r_{o,MN1} g_{m,MN2} r_{o,MN2} \,\|\, r_{o,MP1}} \cdot \frac{1}{C_{gs,MO3} + C_{gs,MO1} + C_C \cdot \left(g_{m,MO3} + g_{m,MO2}\right)\left(r_{o,MO3} \,\|\, r_{o,MO2}\right)} \quad (4.26)$$

where the first term represents the impedance at node 1 in Fig. 4.3 and the second term is the total capacitance at the same node. $C_{gs,MO3}$ and $C_{gs,MO1}$ can be further neglected since they are much smaller than the "Miller capacitor". Resistor R_Z is used as "nulling resistor" and is sized to be larger than $1/(g_{m,MO2} + g_{m,MO3})$ to remove the RHP zero and provide lead compensation [44]. The value of compensation capacitor C_C is set to 4.7 pF and the resistor R_Z is sized to be 3.3 KOhm. This zero is shown in Eq.(4.27) as,

$$z_1 \approx -\frac{1}{\left(R_Z - \frac{1}{g_{m,MO2} + g_{m,MO3}}\right)} \cdot \frac{1}{C_C} \quad (4.27)$$

The secondary pole is designed to be at the output node of this OpAmp. "Pole splitting" effect pushes its frequency further away to higher frequencies. Given that the output capacitor C_L and feedback capacitor C_C are much larger than the gate-to-source junction capacitances of MO_2 and MO_3, this non-dominant pole can be expressed by,

$$p_{out} \approx -\frac{1}{\left(g_{m,MO2} + g_{m,MO3}\right)} \bullet \frac{1}{C_L} \tag{4.28}$$

Another non-dominant pole results from the node at the source terminal of the transistor MO_1 since it is designed with large *W*/*L*.

When integrating the proposed input stage into the overall operational amplifier, the design tradeoff has to be taken into consideration on the non-dominant poles and zeros. Their frequencies should be designed to be as high as possible so that the total phase margin (PM) of more than 60° can be achieved.

4.3.3 Mismatch and Offset Voltage of the 1-V OpAmp

The offset voltage of this OpAmp results from both random offset and systematic offset. The random offset from the proposed bulk-driven input stage is explained in the previous section, which varies with the input voltage. Moreover, since the layout of the bulk-driven input stage tends to cover a large area when they are in different n-wells, this as well creates substantial random offset. In order to mitigate the random offset special attentions are paid to the layout of the OpAmp. For example, common centric layout techniques are used for the bulk-driven input stages.

The folded cascode stage and the level shift class-AB output stage, on the other hand, are major sources of systematic offset when driving various loads. They originate from any mismatch between the output stage PMOSs and NMOSs. The risk of the transistors $MB_{3,4,5}$ and MB_7 being pushed into triode region, especially at high input/output voltages or driving heavy loads, also contributes to the OpAmp offset voltage variations.

4.3.4 1-V OpAmp Layout and Chip Micrograph

The layout of the 1-V bulk-driven OpAmp is shown in Fig. 4.4. The micrograph of the fabricated chip is shown in Fig. 4.5. The overall area for the circuit excluding the ESD pads is 525 μm×300 μm.

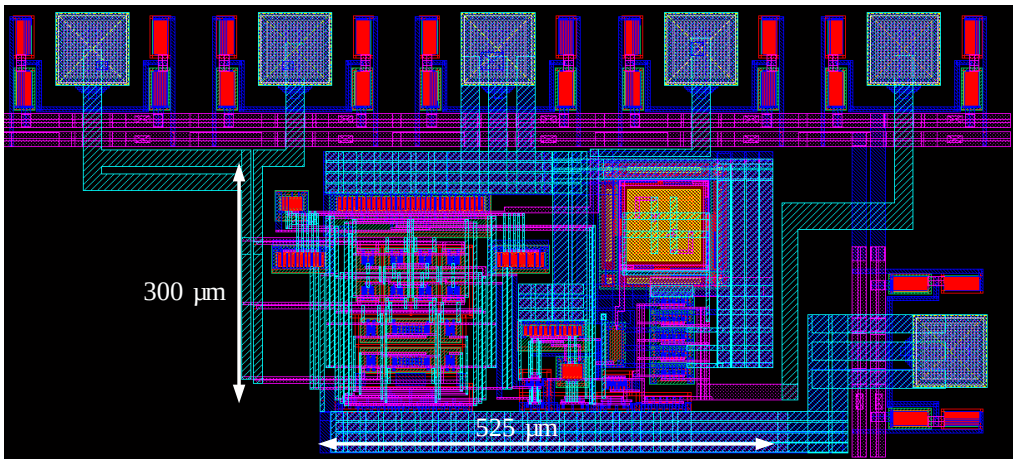

Fig. 4.4 Layout of the 1-V OpAmp.

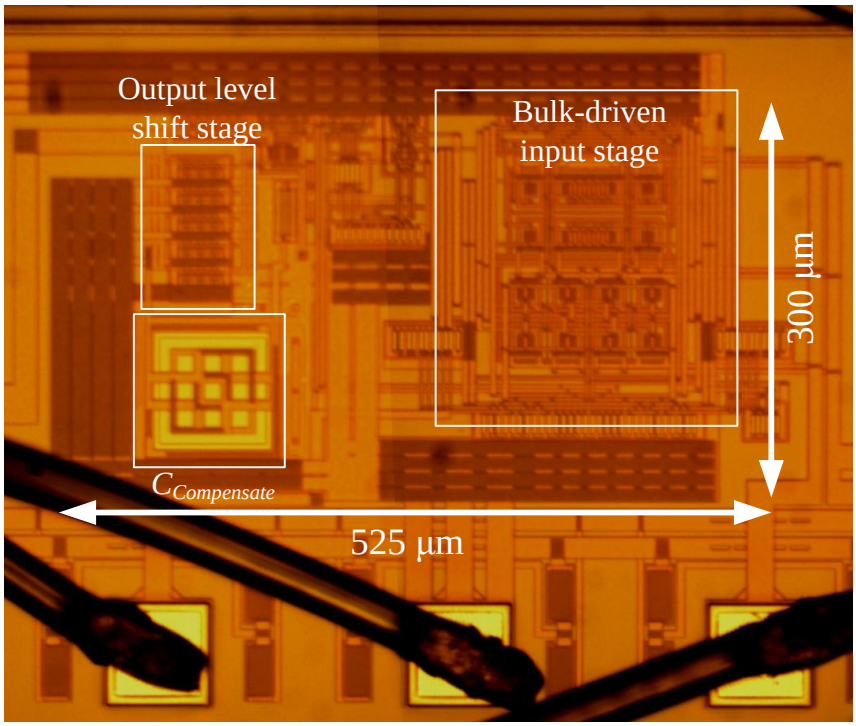

Fig. 4.5 Chip micrograph of the 1-V OpAmp.

CHAPTER 5

DESIGN OF THE 1-V POTENTIOSTAT FOR THREE-ELECTRODE ELECTROCHEMICAL SENSORS

In this chapter, the 1-V potentiostat design is introduced in Section 5.1, where the 1-V bulk-driven transconductance enhanced input stage is employed. In Section 5.2, various performances of this 1-V potentiostat are analyzed.

5.1 1-V Potentiostat Design

The potentiostat proposed in this work is designed to detect biomedical substances inside the human blood, such as glucose, lactate and glutamate, etc. The circuits are implemented on a 0.35 μm n-well digital CMOS process. As discussed in Chapter 2, the biomedical sensors normally require the absolute potential E_i between WE and RE to be within 0.5 V ~ 0.7 V. This potential window makes a 1-V potentiostat achievable with sufficient dynamic range provided by the proposed 1-V $G_{m\_in\_eff}$ enhanced bulk-driven amplifier.

The proposed 1-V potentiostat design adopts the general potentiostat topology in [14]. Fig. 5.1 and Fig. 5.2 describe two block diagrams of these 1-V potentiostat circuits suitable for positive (Fig. 5.1) and negative (Fig. 5.2) potential E_i (i.e. $V_{WR}>0$ or $V_{WR}<0$) biosensors. Both of these circuits feature the same topology, except in Fig. 5.1 the N-type transistor MO_1 is sinking the sensor current while the

transistor MO_2 mirrors it. Vice versa, the P-type transistor MO_1 is sourcing the sensor current while the transistor MO_2 copies it as shown in Fig. 5.2. A signal processing unit (current-to-frequency converter) presented in [4] can be deployed here to process this current signal (Fig. 2.8). The *I-F* converter takes in

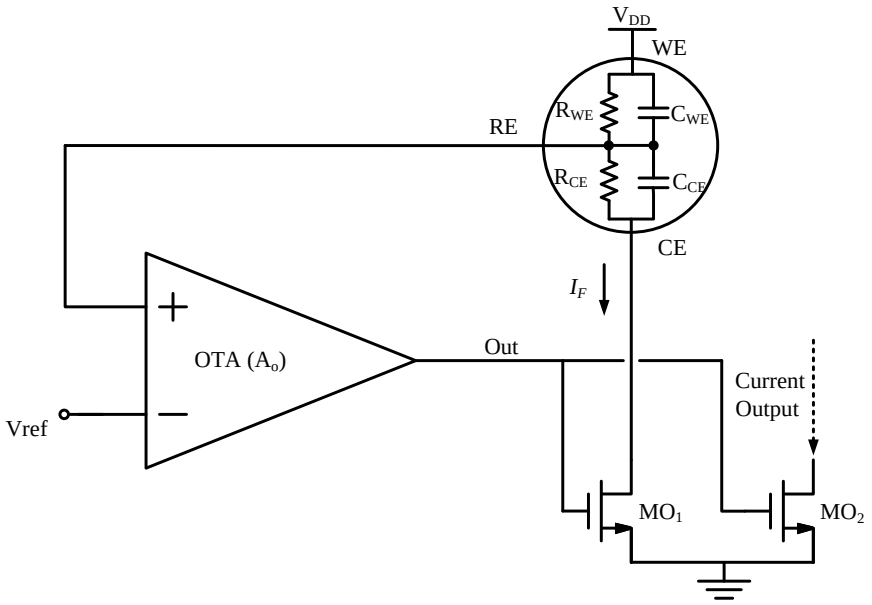

Fig. 5.1 Schematic block diagram of the proposed 1-V potentiostat with positive E_i.

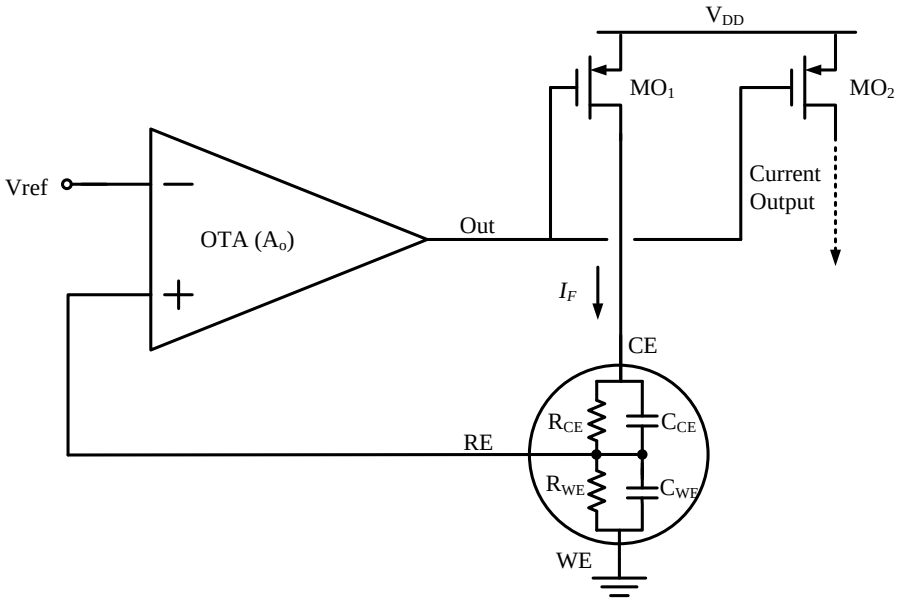

Fig. 5.2 Schematic block diagram of the proposed 1-V potentiostat with negative E_i.

any sensor current signal and converts it into an amplitude-shift-keying (ASK) signal. A programmable frequency divider is incorporated into the circuit to set the ASK envelope frequency within the audio frequency range. Then the output frequency can be transmitted outside.

The sensor model is illustrated in schematics without negligible solution resistances R_{S1}, R_{S2} and Faradic resistance R_{RE}. This topology suffers from the aforementioned feedback problem. But apart from this, this circuit can consume much less power since there is one amplifier inside and the output current signal is also more efficient to process than normal voltage signal used in other potentiostat topologies. The most important aspect of this topology is that it can operate under low power supply voltage (i.e. 1-V) given that the OTA itself is low-voltage compatible. Since the resistance of the counter electrode (R_{CE}) is much smaller than that of the working electrode (R_{WE}), the voltage drop across RE-CE can be neglected. If merely 0.5 V~ 0.7 V is necessary for biasing WE-RE or RE-WE, an adequate voltage headroom can be allocated to transistor MO_1 for its saturation operation. The required reference voltage V_{ref} at the inputs of the OTA is equal to V_{DD}-V_{WR} in Fig. 5.1 while V_{ref} is equal to V_{WR} in Fig. 5.2.

A conventional 1-V bulk-driven OTA is not an ideal candidate in this topology due to its low open loop gain A_O. Use of the gain boosting techniques is problematic as will be discussed later. The proposed 1-V bulk-driven amplifier greatly improves A_O at the input stage. Thus the design of the OTA involved in this potentiostat is derived from the proposed 1-V OpAmp excluding the output push-pull stage.

5.2 1-V Potentiostat Prototype Implementation

Fig. 5.3 shows the detailed schematic of Fig. 5.1 with the 1-V OTA. Essentially, this potentiostat is capable of working with any biosensors that require a potential E_i from 0 V up to ~|0.8 V|(i.e. by tuning the $V_{DS,sat}$ voltage in Fig. 5.3) as long as the source-to-bulk voltage V_{SB} of the input bulk-driven pairs is designed not to exceed 500 mV, so there is less than nano-ampere input current.

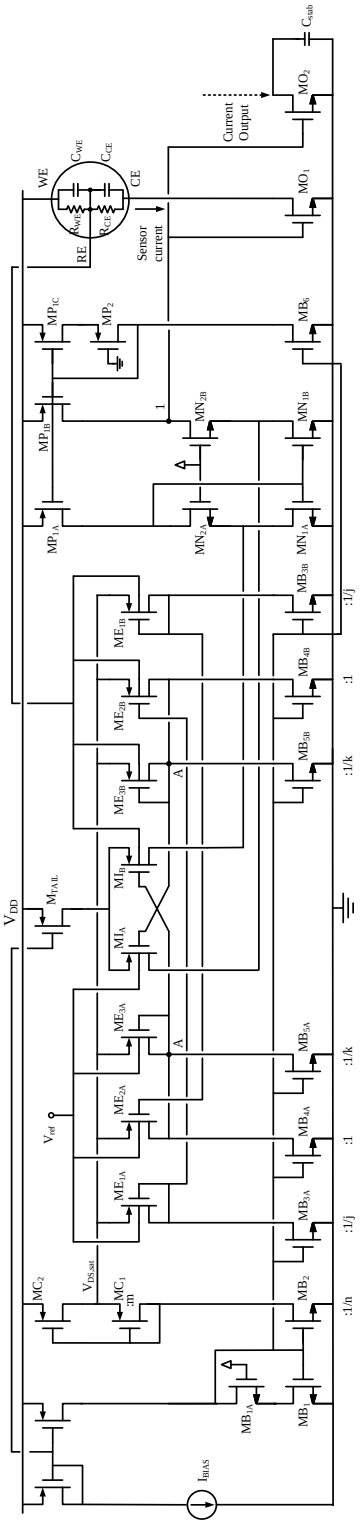

Fig. 5.3 Schematic of the proposed 1- V potentiostat with detailed OTA circuits.

It is worth pointing out that the temperature behavior of this input current is not studied as the environment temperature tends to be stable inside the human body. A capacitor (C_{stab}) is placed at the sensor current output to ensure the stability between the potentiostat and the SPU interface.

The frequency response of the 1-V potentiostat is analyzed by considering the 1-V OTA as a single circuit block with open loop gain being A_O and the aforementioned zero-pole doublets existing inside. The loop gain can be calculated as,

$$\boldsymbol{A_{Loop} = A_O \times g_{m,MO_1} \frac{r_{o,MO_1} R_{WE}}{r_{o,MO_1} + R_{WE} + R_{CE}} \times \frac{(1+s/z_1)(1+s/z_2)(1+s/z_3)}{(1+s/p_1)(1+s/p_2)(1+s/p_3)(1+s/p_4)(1+s/p_5)}} \quad (5.1)$$

where $g_{m,MO1}$ and $r_{o,MO1}$ are the transconductance and output impedance of the transistor MO_1, the poles and zeros are listed in the following:

$$\boldsymbol{p_1 \cong -\frac{1}{C_{WE}(R_{WE} \parallel (R_{CE} + r_{o,MO_1}))}} \quad (5.2)$$

$$\boldsymbol{p_2 \cong p_{Out}} \quad (5.3)$$

$$\boldsymbol{p_3 \cong -\frac{1}{C_{CE}(R_{CE} \parallel r_{o,MO_1})}} \quad (5.4)$$

$$\boldsymbol{p_4 \cong p_{OTA,1}} \quad (5.5)$$

$$\boldsymbol{p_5 \cong p_{OTA,2}} \quad (5.6)$$

$$\boldsymbol{z_1 = -\frac{1}{C_{CE} R_{CE}}} \quad (5.7)$$

$$\boldsymbol{z_2 = z_{OTA,1}} \quad (5.8)$$

$$\boldsymbol{z_3 = z_{OTA,2}} \quad (5.9)$$

The Bode plot of the loop gain frequency response is shown in Fig. 5.4. The pole p_1 is the dominant pole whose frequency depends on the double layer capacitance of the working electrode and the sensor current while the pole p_2 is located at the output node of the transconductance enhanced bulk-driven OTA. Normally p_2 is expected to be a low-frequency pole as well. Doublets p_3 and z_1 are created by the sensor itself. They can almost cancel each other due to the much lower value of R_{CE} than $r_{o,MO1}$.

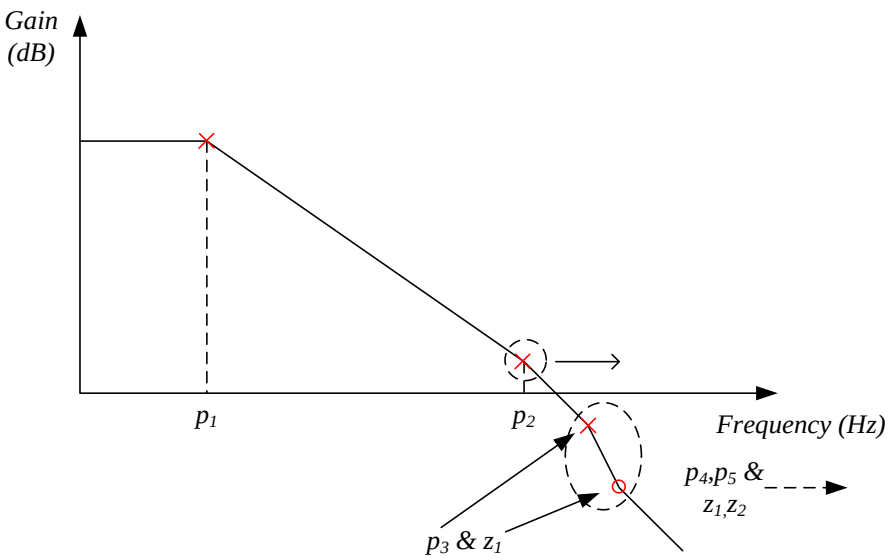

Fig. 5.4 Bode plot of the 1-V potentiostat loop gain.

The poles p_4, p_5 and the zeros z_2, z_3 are doublets from the 1-V bulk-driven OTA as discussed in the previous chapter and they are at fairly high frequencies and are thus not capable of significantly affecting the overall frequency response. Obviously, to guarantee that only one dominant pole can exist inside the loop, a bulk-driven OTA with second stage gain boosting is not plausible in this structure as the open loop gain of the OTA is limited to prevent pole p_2 interfering the frequency response. However, by employing the proposed bulk-driven amplifier, this problem can be solved since the enhanced input transconductance compensates the low output impedance of the OTA. As a result, sufficient gain can be attained.

The current consumption of this 1-V bulk-driven amplifier is, however, reduced to approximately half. This is due to the relaxed operating speed requirement of the biomedical applications (i.e. depends on the pole p_1 frequency). The biasing circuitry is implemented under 1-V power supply to provide bias current for this 1-V potentiostat. A common low-voltage bias circuitry [44] is employed. Fig. 5.5 illustrates the schematic of this biasing circuit. A compensation capacitor is placed at the high impedance node to stabilize the feedback loop inside.

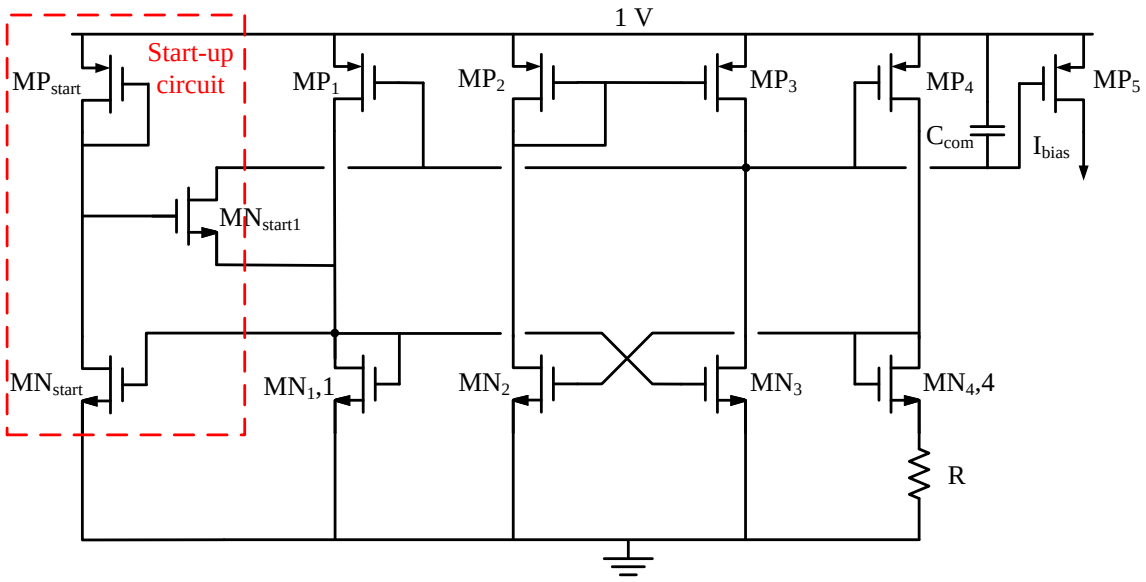

Fig. 5.5 Schematic of the biasing circuitry.

The impedance at the OTA output node in Fig. 5.1 and Fig. 5.2 and the node capacitance need to be kept at a moderate value to maintain a non-dominant pole. Consequently, moderate channel length is used for the folded cascode current mirrors and their loads. The aspect ratios of transistors MO_1 and MO_2 are designed to be small in order to match two currents well. The detailed aspect ratios of transistors inside this potentiostat are given in Table 5.1.

Table 5.1 Transistors Aspect Ratio of the 1-V Potentiostat in Fig. 5.3

Transistor	***W/L* (μm/μm)**	**Transistor**	***W/L* (μm/μm)**	**Transistor**	***W/L* (μm/μm)**
MI	57.6/0.5	**M_{TAIL}**	19.2/1.2	**MN_1**	2/0.8
ME_1	14.4/0.5	**$MB_{3,5}$**	2/1.5	**MN_2**	2.2/0.5
ME_2	57.6/0.5	**MB_4**	8/1.5	**MP_1**	6/0.7
ME_3	14.4/0.5	**MC_2**	28.8/1.2	**$MO_{1,2}$**	1.2/0.6

The signal to noise ratio (SNR) is calculated in Eq.(5.10) as,

$$SNR = \frac{\left(I_{sensor} R_{WE}\right)^2}{\overline{v_n^2} + \overline{i_{nO_1}^2} R_{WE}^2} \tag{5.10}$$

where v_n is the equivalent input referred noise voltage of the OTA and i_{nO1} is the drain-to-source noise current of the transistor MO_1. It can be concluded that the SNR is mainly decided by the noise performance of the 1-V OTA, whose input referred noise is shaped by the improved $G_{m\_in\_eff}$.

The layout and micrograph of this 1-V potentiostat are show in Fig. 5.6 and Fig. 5.7, respectively. The layout techniques used for the potentiostat are similar to the OpAmp discussed earlier. Two capacitors cover a substantial amount of the chip area and are used to stabilize the interface between the potentiostat and the SPU (not shown). The overall chip area excluding the ESD pads is 0.13mm^2, and the power consumption is about 22 μW.

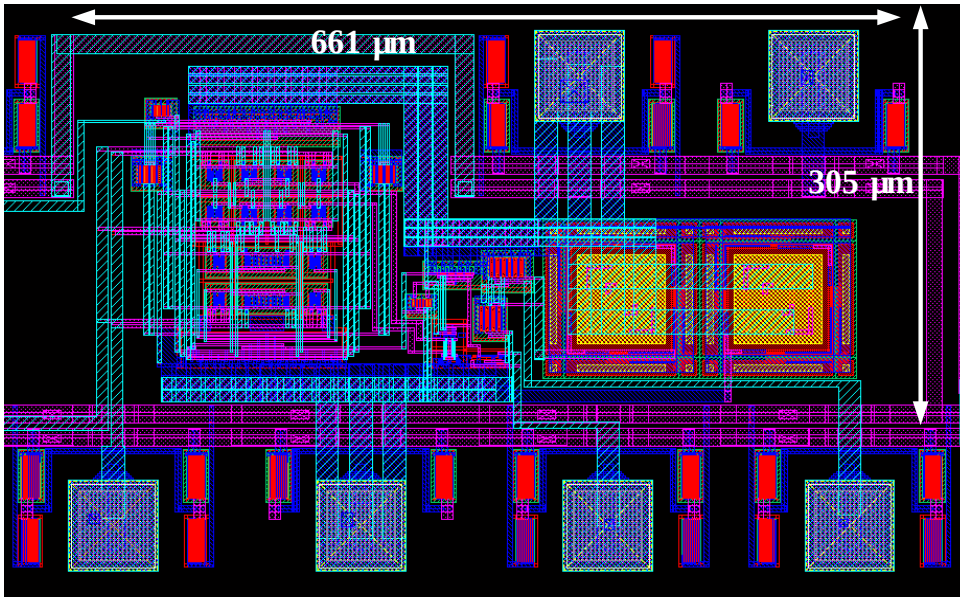

Fig. 5.6 Layout of the 1-V potentiostat.

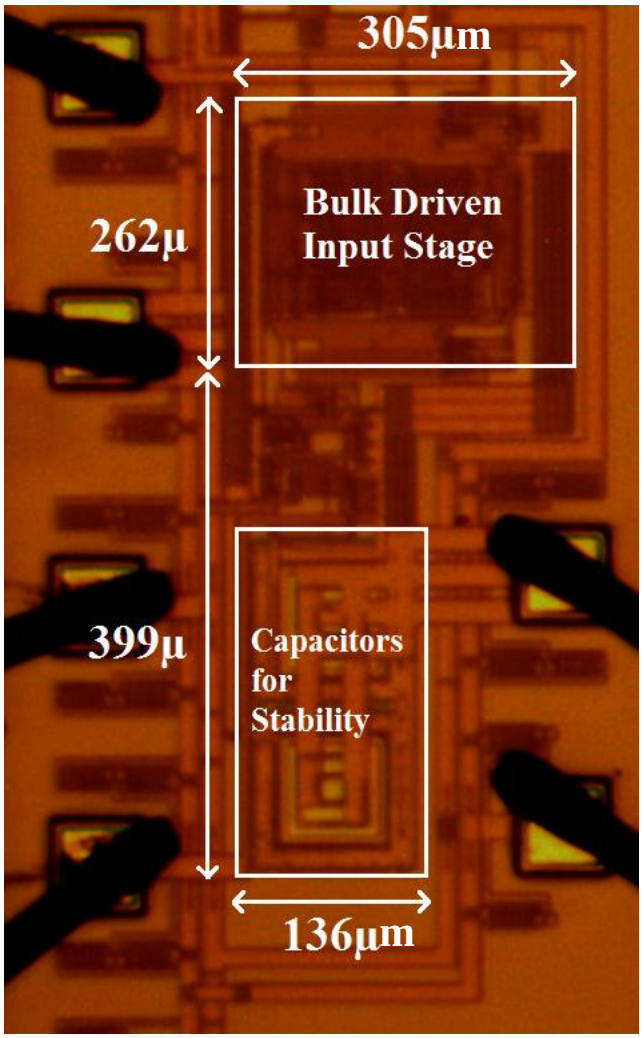

Fig. 5.7 Chip micrograph of the 1-V potentiostat.

CHAPTER 6

PROTOTYPE MEASUREMENTS

In this chapter, the test equipments including both the hardware and the software are introduced in Section 6.1, so as the test setup for the 1-V OpAmp. The characterizations of a single bulk-driven MOSFET are then presented in Section 6.1, which are followed by the performance discussion of the proposed 1-V general purpose OpAmp derived from the characterization results and comparisons with the simulation results. In Section 6.2, the measurement results of the proposed 1-V potentiostat are discussed. Then the measured data of the 1-V potentiostat with both the sensor models and the micro-fabricated biosensors are revealed. The performance of the 1-V OpAmp and the 1-V potentiostat are summarized and compared with the other state of arts at the end of each section.

6.1 Characterizations of the 1-V OpAmp and Its Sub-Circuits

6.1.1 1-V OpAmp Test Environment

Typical OpAmp characterizations include its power consumption, open loop gain (A_o), frequency response, transient response, input common mode range (ICMR), noise, power supply rejection ratio (PSRR) and common mode rejection ratio (CMRR) measurements. In this work, a single bulk-driven MOSFET and the standalone 1-V bulk-driven transconductance enhanced input stage are separately laid out and characterized to provide useful design guidelines for the OpAmp implementation and obtain the input transconductance of the proposed OpAmp. Except for the single bulk-driven MOSFET, all the other circuits are implemented on an n-well 0.35 μm digital CMOS process.

A printed circuit (PC) board (Vector board) is used to characterize the 1-V bulk-driven OpAmp under the room temperature. The test circuit is shown in Fig. 6.1. Power supply bypassing capacitors are soldered next to power supply pins to filter out AC ripples and the power supply noise. Specifically, an electrolytic capacitor of 100 μF (on the back of the board), a polypropylene capacitor of 4.7 μF and a ceramic capacitor of 0.47 μF are utilized to cover different bandwidth of the power supply noise. The bias current for this 1-V OpAmp or the standalone input stage can be either supplied externally through a dedicated pin or connected to an on chip biasing circuitry as shown in Fig. 5.5.

In order to characterize the DC parameters of the circuits, the Keithley 2400 source meters are extensively employed, which are controlled by the software Labtrace 2.0 developed by Keithly Instruments Inc. as well. In addition, OpAmp characterization software developed by the ISCAL group led by Dr. Blalock at the University of Tennessee is used to evaluate most of the performance for the 1-V bulk-driven OpAmp. Other measurement hardware such as low-noise amplifier, spectrum analyzer, high precision power supplies, etc. are also employed. Table 6.1 shows all the equipments used to characterize the single MOSFET, the bulk-driven input stage alone and the 1-V OpAmp. The detail test setups are presented in the following sub-sections.

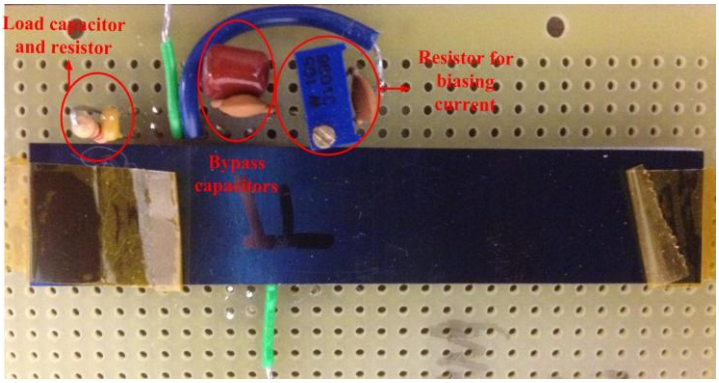

Fig. 6.1 The test board for the 1-V bulk-driven OpAmp characterizations.

Table 6.1 Equipments Used to Characterize the Single MOSFET, the Standalone Bulk-Driven Input Stage, and the 1-V Bulk-Driven OpAmp

Type	Features
Agilent E3631A Triple Output DC Power Supply	0~6V;-25V~25V
Spectrum/Network Analyzer HP 3589A	10 Hz to 150 MHz frequency range;80dB~112dB dynamic range
Source Meter Keithley 2400	Five instruments in one (IV Source, IVR Measure)
Agilent MSO6052A Mixed Signal Oscilloscope	500MHz Bandwidth, 4Gsample per second.
Agilent 33220A Waveform Generator	Maximum 20 MHz Sine wave.
Agilent 34401A Digit Multimeter	6.5 bits
Perkin Elmer 5184 Preamplifier	60 dB gain up to 1MHz; 800pV/Hz$^{1/2}$
GPIB Cables	Shielded
Lenovo Laptop	With National Instruments GPIB device driver

6.1.2 Characterizations of the Bulk-Driven MOSFET

To achieve the best bulk-driven circuit performance, it is necessary to start with the single bulk-driven P-type MOSFET characterizations. The comparisons between the measurements and the simulations are able to provide insights for subsequent circuit implementations.

The basic source-to-bulk junction *I-V* curve is measured by using source meters to sweep the bulk-to-source voltage (V_{BS}) and obtain the junction current (I_{BS}). Fig. 6.2 reveals the characterizations of the PMOS source-to-bulk junction in a 0.5 μm digital n-well CMOS process from both simulation and measurements. All comparisons are conducted with the same 6 μm/ 3 μm diode-connected PMOSs where their V_{GS} are kept at -1.2 V. Berkeley Short-channel IGFET Model (BSIM) 3 spice model is used in the simulation. The measurements are performed on four chip samples. It can be noticed that the measured data on each chip is very consistent and the junction currents I_{BS} reach -2 nA at the voltage V_{BS} equal to -

600 mV. The simulation, however, shows similar trend except that the I_{BS} already reaches around -2 nA at V_{BS} of -450 mV, which means more than 150 mV higher turn-on voltage of the junction can be expected from measurements to simulation. This characterization is particularly important for designing the proposed bulk-driven amplifier regarding to the achievable input common mode voltage range. Clearly, for V_{BS} larger than -600 V, the bulk-driven MOSFET still exhibits high input impedance.

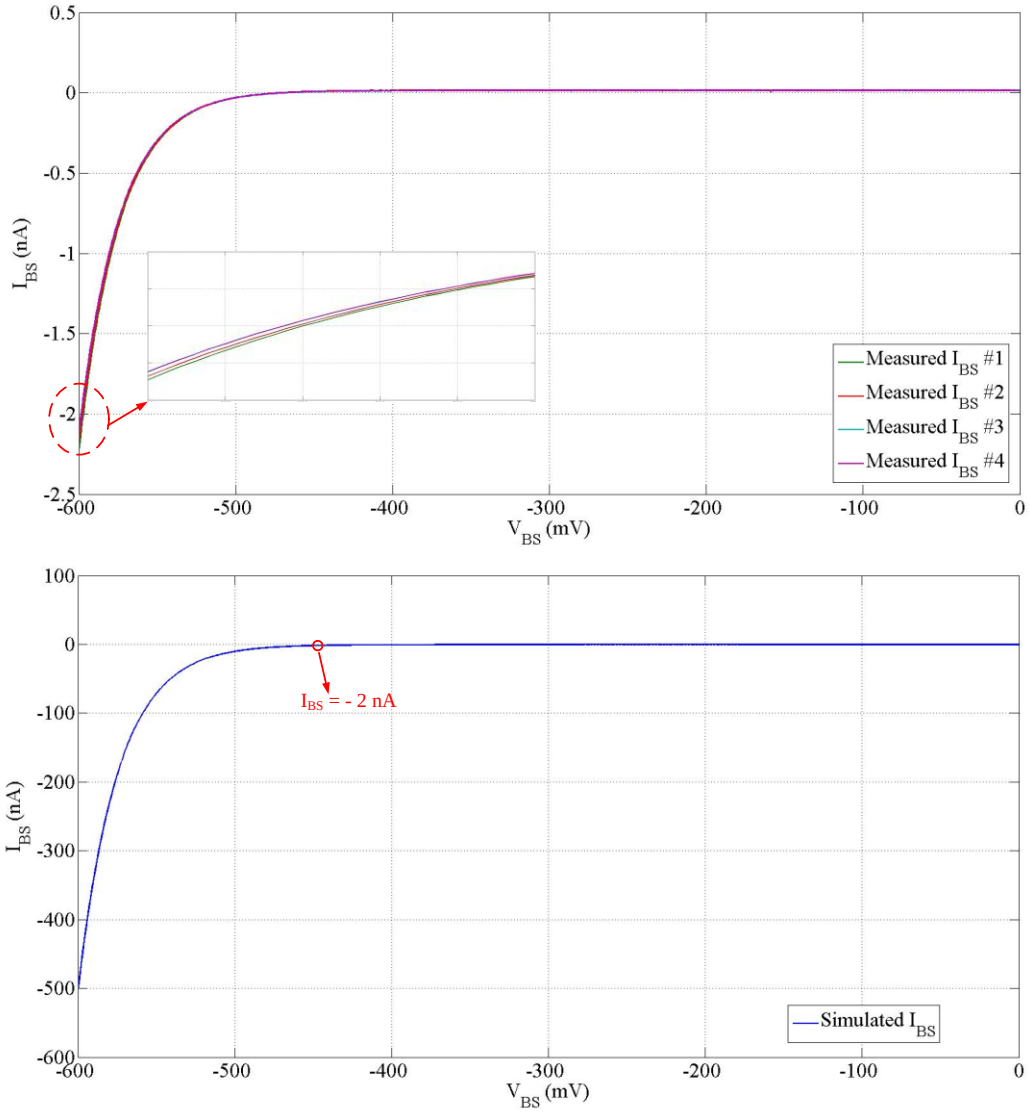

Fig. 6.2 Measured and simulated I_{BS} versus V_{BS} for the bulk-driven PMOS.

By using source meters, Fig. 6.3 (a) is able to show the measured PMOS source-to-drain current (I_{SD}) variations with increasing V_{BS} in comparison with the simulation result. The measurement setup is the same with the one in Fig. 6.2 with V_{GS} kept constant at -1.2 V. It shows that for V_{BS} larger than -200 mV, the drain currents decrease at the similar rate between the measurements and the simulation with increasing V_{BS}, while below -200 mV the measured I_{SD} increase more rapidly than the simulated one with descending V_{BS}.

This behavior also implies that the bulk transconductance g_{mb} in the measured MOSFET is larger than the simulated one. Fig. 6.3 (b) shows the calculated bulk transconductance g_{mb} from the measurement results using MATLAB. It reveals that, compared to simulation result, the measured g_{mb} can achieve much larger value with further forward biasing of V_{BS}. Particularly, the measured g_{mb} is about two times of the simulated one at V_{BS} of -400 mV, while more than five times at V_{BS} of -600 mV. The trend is also quite different between the measurements and the simulation, where measured g_{mb} drops with increasing V_{BS} and simulated g_{mb} behaves the opposite. This measurement results also match the relationship of g_{mb} with V_{BS} derived in Eq. (3.2).

6.1.3 Characterizations of the Standalone Bulk-Driven Input Stage

The proposed 1-V bulk-driven input stage with the enhanced transconductance is laid out separately (i.e. the circuit in Fig. 4.2) and necessary nodes are pinned out so a conventional 1-V bulk-driven input stage can be formed and characterized. In order to achieve a fair comparison, the bias conditions of the core input pairs for both circuit topologies are kept the same. The simulations and characterizations of both the proposed and the conventional bulk-driven input stage are done by biasing the negative input at the voltage V_{input}, then sweeping the voltage on the positive input in small increments (e.g. 100 μV) around V_{input} as shown in Fig. 6.4. Complementary power supplies, which provide ± 0.5 V, are used to power both input stages.

The effective input transconductance ($G_{m\_in\_eff}$) can be obtained using Eq. (6.1) as,

$$G_{m\_in\_eff} = \frac{d\left(I_{out+} - I_{out-}\right)}{dV_{sweep}} \tag{6.1}$$

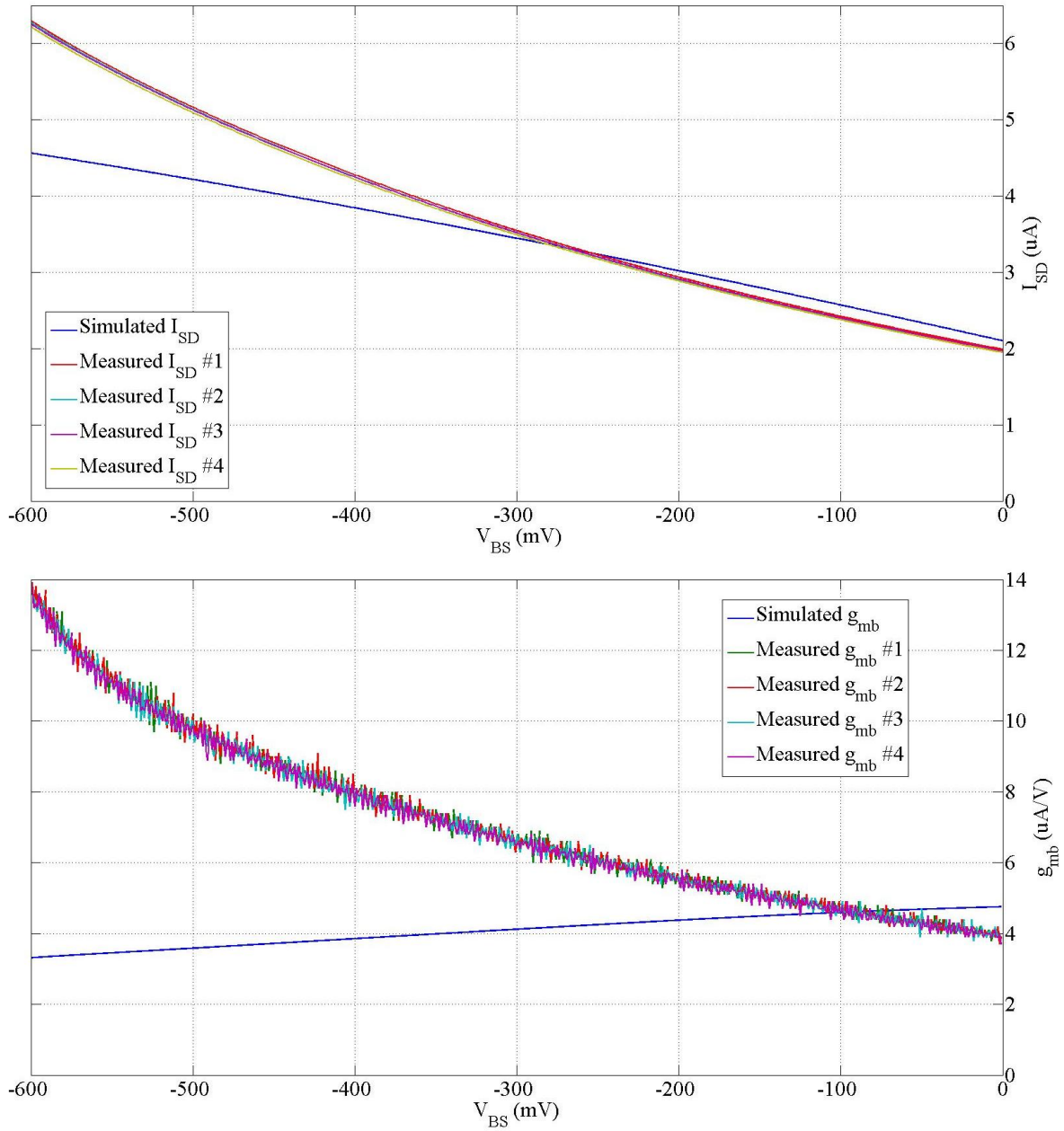

Fig. 6.3 (a) Measured and simulated I_{SD} variations with the change of V_{BS}; (b) Measured and simulated g_{mb} variations with the change of V_{BS}.

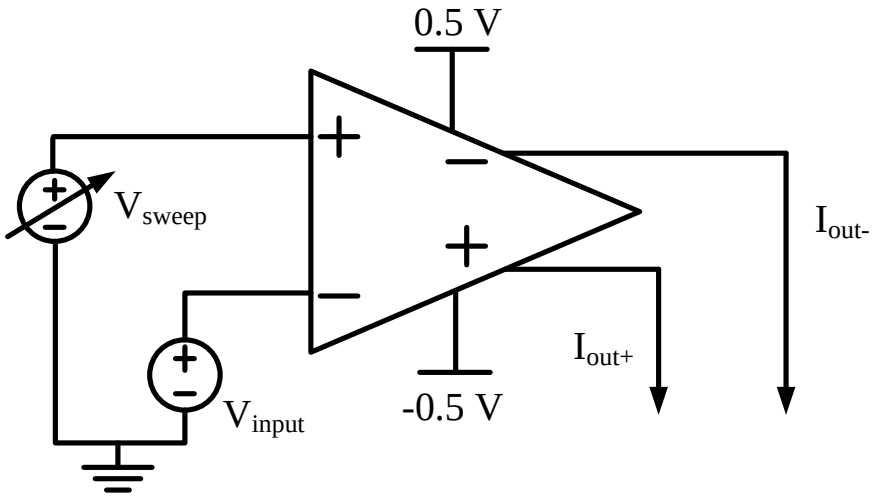

Fig. 6.4 Test setup for charactering the 1-V bulk-driven input stage.

where I_{out+} and I_{out-} are the output currents in Fig. 6.4**.** Simulation results in Fig. 6.5 show the comparison of the $G_{m\_in\_eff}$ between the proposed circuit and the conventional one at different input voltages V_{input}**.** Since there is the aforementioned lower limitation of the common mode input voltage for the proposed input stage, simulations are only conducted for V_{input} more than -200 mV. The source-to-bulk voltage V_{SB} of the input transistors is given by,

$$\boldsymbol{V_{SB,input} = V_{DD} - V_{input} - V_{DS,sat}} \tag{6.2}$$

where $V_{DS,sat}$ is mentioned in the previous chapters which is designed to be around 200 mV. The maximum $G_{m\_in\_eff}$ of the proposed bulk-driven stage is equal to 142 μA/V when V_{input} is around 320 mV (i.e. V_{SB} is close 0 V) while the $G_{m\_in\_eff}$ of the conventional bulk-driven input stage peaks at the similar input voltage with a value of 18.5 μA/V.

The measured input transconductance of both the proposed and the conventional 1-V bulk-driven input stages are shown in Fig. 6.6 where both peak at input voltage of -200 mV. The maximum $G_{m\_in\_eff}$ the proposed circuit can achieve is 518.2 μA/V where that of the conventional circuit is 56.4 μA/V.

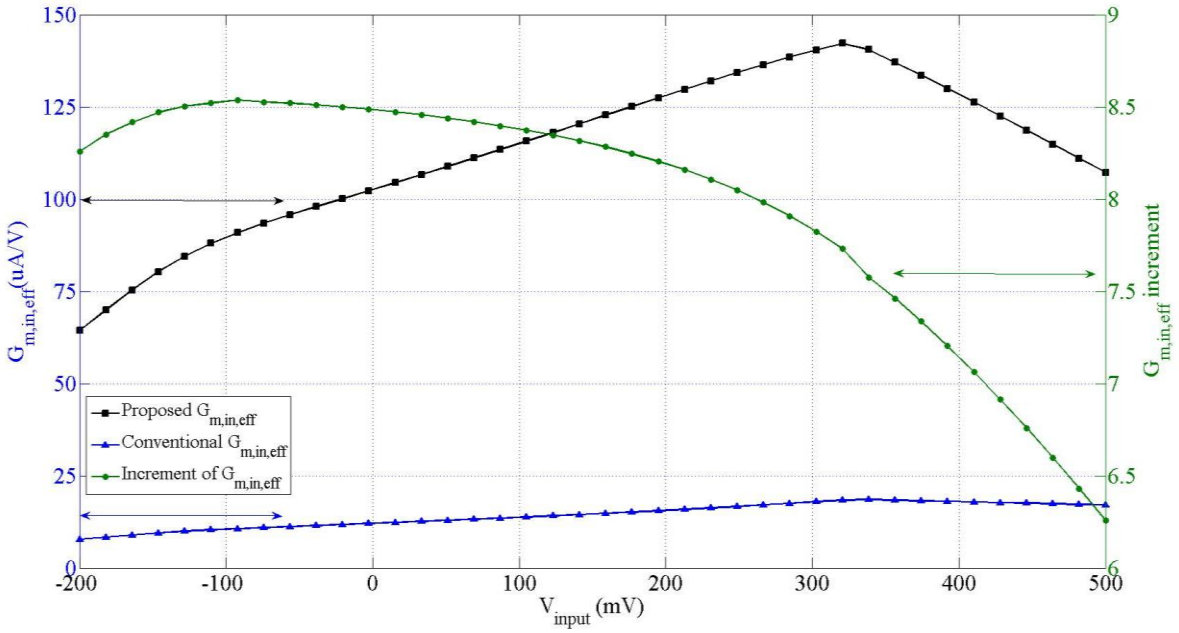

Fig. 6.5 Simulated transconductance ($G_{m\_in\_eff}$) of the proposed and the conventional bulk-driven input stage and its increments.

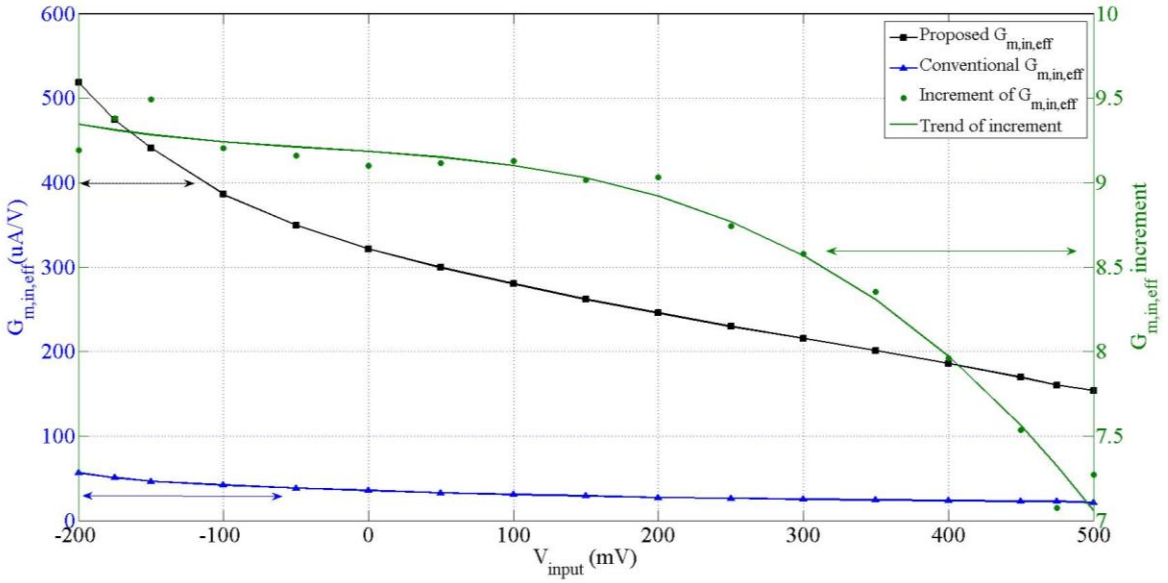

Fig. 6.6 Measured transconductance ($G_{m\_in\_eff}$) of the proposed and the conventional bulk-driven input stage and its increments.

Several differences can be observed from Fig. 6.5 and Fig. 6.6.

1) The measured $G_{m\_in\_eff}$ of the conventional and the proposed input stages are much larger than the simulated ones particularly at lower values of V_{input}. The trend shows the measured conventional and enhanced $G_{m\_in\_eff}$ drops with elevated V_{input} while the simulated ones increase with elevated V_{input} except at high input voltages. This agrees with the characterization results of a single PMOS transistor.

2) The ratio of $G_{m\_in\_eff}$ from the proposed bulk-driven input stage to the conventional one is also calculated in these two figures (labeled as $G_{m\_in\_eff}$ increment). The theoretical increment is 10 times since parameter k is designed to be 4 while the actual increment is smaller than that due to the second-order effect of the transistors. In the simulation, within the overall input range, the $G_{m\_in\_eff}$ increment to the conventional bulk-driven stage is 8.5 times at most and more than 6 times in the worst case scenario. While in the measurement, the increment is 9.5 times at most and 7 times at least. The increments decrease at elevated V_{input} in both simulation and measurement because the source-to-gate voltage of the input pair transistors also increases with V_{input} which pushes the biasing transistors $MB_{3,4,5}$ more into the triode region.

In addition, the offset voltage (V_{offset}) for the proposed bulk-driven input stage can be calculated based on the previous measurements. By taking the voltage difference between the positive and the negative inputs when the output currents are equal, the offset voltages are obtained as shown in Fig. 6.7. From measurements, it can be noticed that V_{offset} increases with elevated V_{input}. This confirms the offset voltage analysis in the previous chapter. Another contribution to the varied V_{offset} is the pushed-to-triode biasing transistors particularly at high input voltages.

The input current is measured on the proposed bulk-driven input stage which can be regarded as the input biasing current of the following 1-V bulk-driven OpAmp since they have identical geometries. Fig. 6.8 reveals that the input current is below 10 nA at V_{input} more than -200 mV. It further drops below 100 fA after V_{input} increases beyond -50 mV.

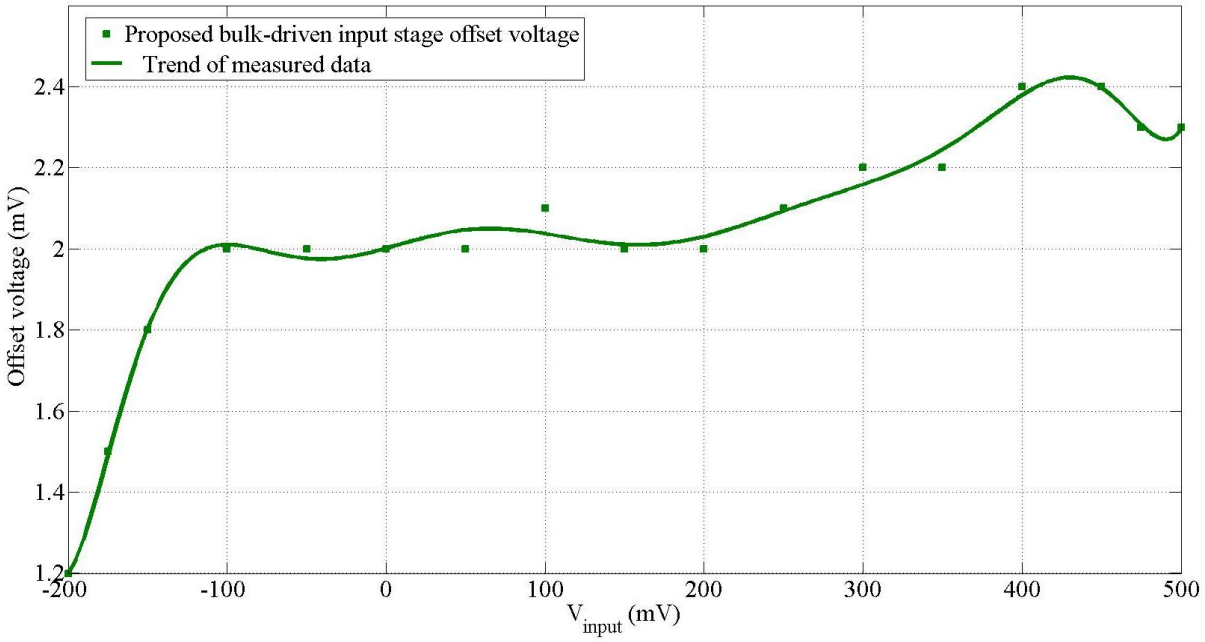

Fig. 6.7 Measurement of the proposed bulk-driven input stage offset voltage.

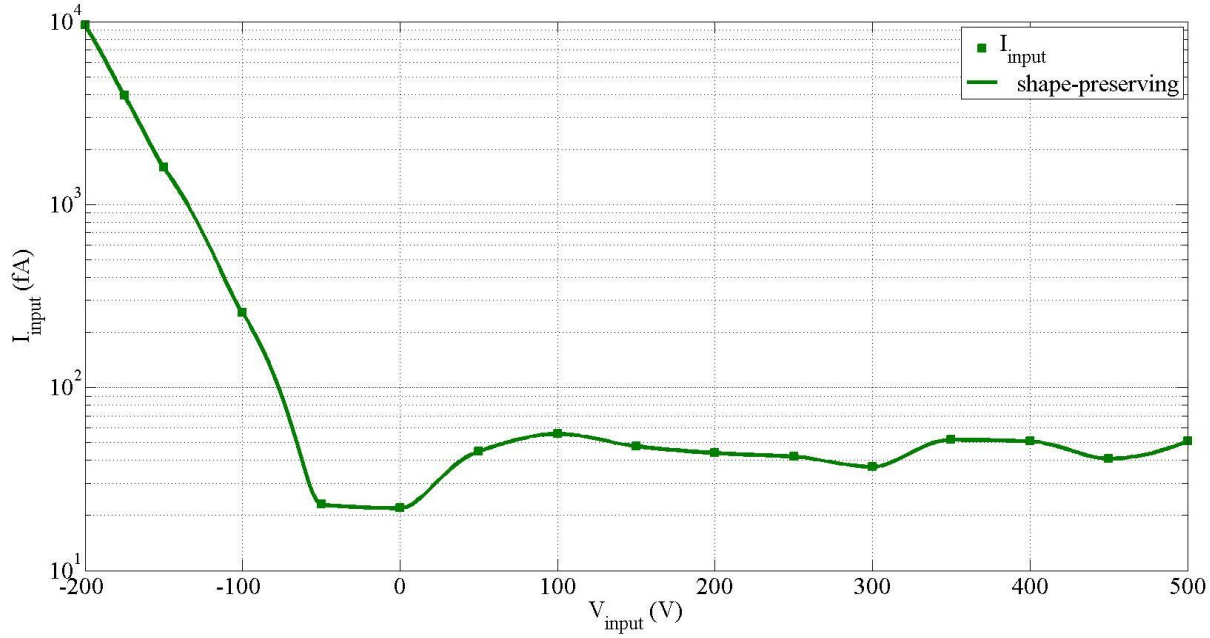

Fig. 6.8 Measured input current of the proposed bulk-driven input stage.

6.1.4 Characterizations of the Proposed 1-V Bulk-Driven OpAmp

Typical OpAmp performance such as power consumption, offset voltage, input common mode range (ICMR), open loop gain (A_o), unity-gain bandwidth (UGBW), noise, power supply rejection ratio (PSRR) and common mode signal rejection ratio (CMRR), etc. have been measured. Comparisons with simulation results are also presented in this section. Complementary power supplies, which provide ± 0.5 V, are used for most of the measurements conducted in this section unless noted otherwise.

This OpAmp is generally tested under two load conditions, namely, the light load and the heavy load. The light load originates from the loading of an oscilloscope probe, where 15 pF capacitance and 1MOhm impedance can be found. The heavy load is created by connecting the output to a 35pF capacitor (which adds up to 50 pF including the probe capacitance) and a 3.3 KOhm resistor. However, if an oscilloscope probe is not used in certain measurements, physical capacitors and resistors are added to mimic both loads.

6.1.4.1 OpAmp ICMR, Offset Voltage and Power Consumption

The input common mode range (ICMR) for an OpAmp is defined as the maximum input voltage range that all transistors work in saturations. Additionally, for bulk-driven OpAmps, the input impedance needs to be high (e.g. $I_{input} < 10$ nA). The ICMR of this 1-V OpAmp can be measured using the test setup in Fig. 6.9 where the OpAmp is in unity-gain, non-inverting configuration. The voltage at the positive input (V_{input}) is swept from -200 mV to 500 mV to avoid turning on the source-to-bulk junction diode. The offset voltage (V_{offset}) can be calculated by taking the difference between the input voltage (V_{input}) and the output voltage (V_{out}) at each point.

The ICMR and the offset voltage measurements are conducted under both the light load and the heavy load situations. Fig. 6.10 and Fig. 6.11 show the measurement results. Under the light load, the proposed 1-V OpAmp shows ICMR from -200 mV to 500 mV where it still maintains high linearity and

input current smaller than 10 nA. Measurements also reveal that ICMR can be extended lower to -250 mV for input current as low as 38 nA. The offset voltage changes from 3.9 mV to 16 mV in one sample, and -6.7 mV to -13.2 mV in anther sample.

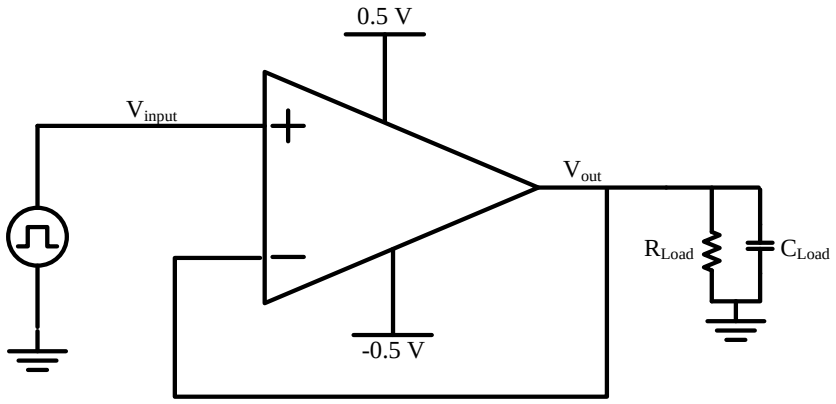

Fig. 6.9 Test setup for the OpAmp ICMR measurement.

On the other hand, under the heavy load, ICMR values from -200 mV to 400 mV still keeps the OpAmp in high linear operation and high impedance input. The offset voltage varies from 7.4 mV to 16.6 mV in one sample and -7.7 mV to -14.4 mV in another sample.

The offset voltage of this 1-V OpAmp changes along with the input voltage for the following reasons:

1) The offset voltage variations inside the input stage (due to random mismatches).
2) Systematic mismatches inside the OpAmp cascode stage and output push-pull stage.
3) The risk of the triode operation of the transistors inside the input stage and the output push-pull stage. This could result in gain decrements particularly at high input/output voltages or driving heavy loads.

The power consumption of this 1-V OpAmp is measured using the same test setup driving both loads. Its comparison with the simulated power consumption is shown in Table 6.2.

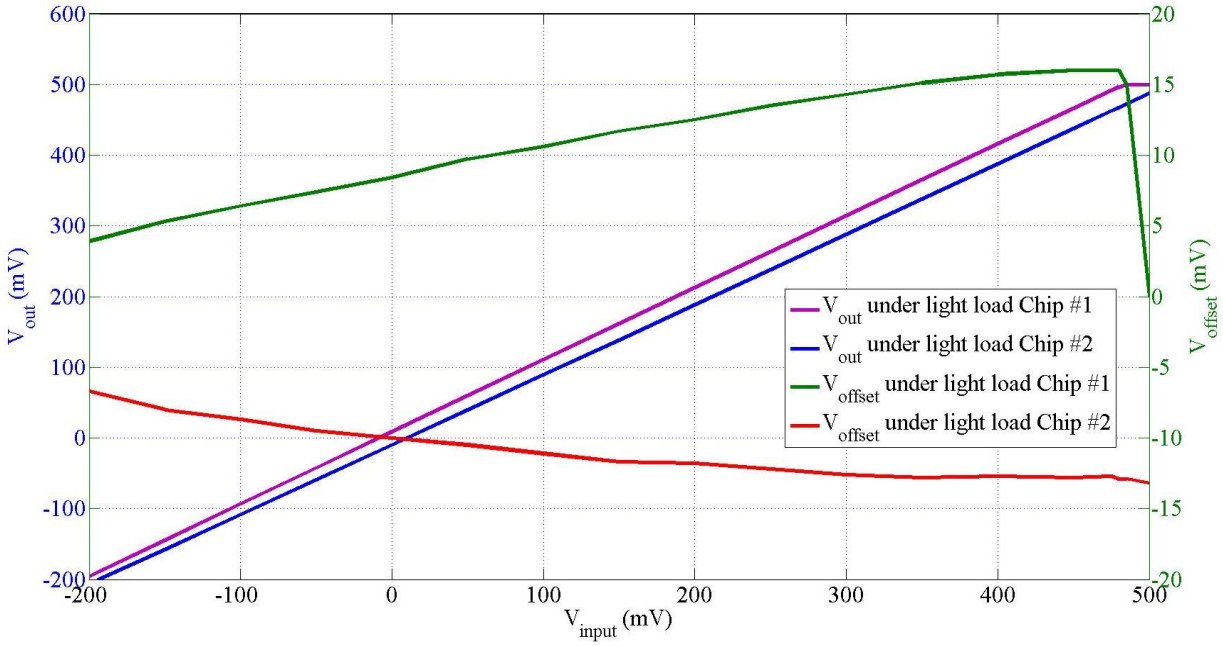

Fig. 6.10 ICMR and offset measurements of the proposed 1-V OpAmp under the light load.

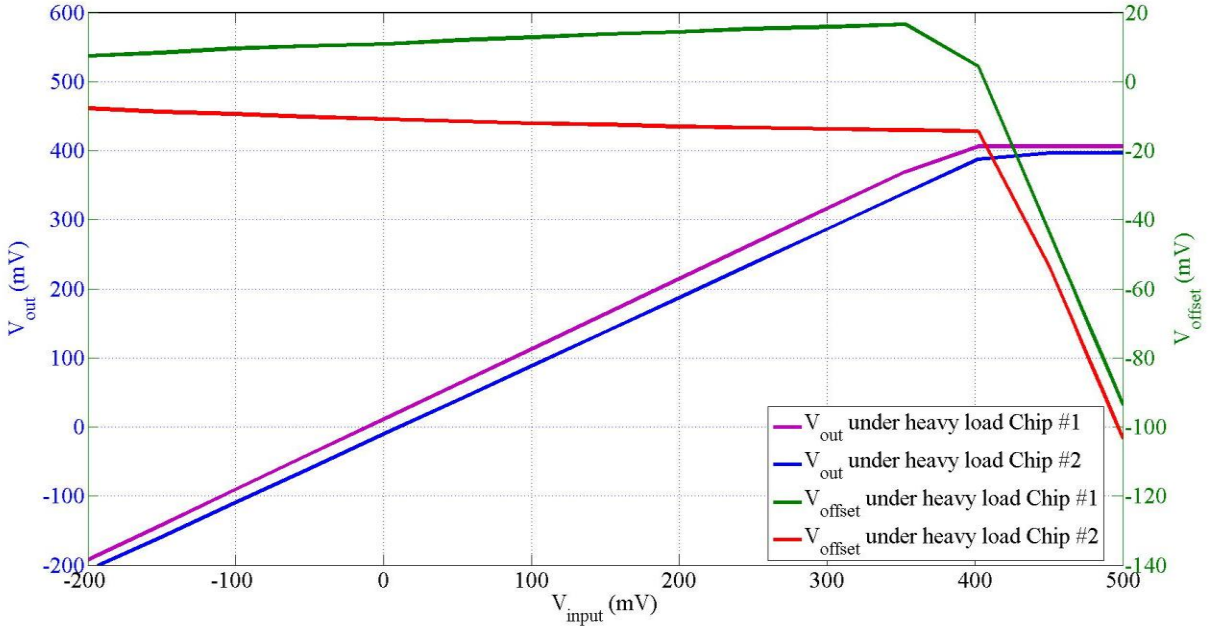

Fig. 6.11 ICMR and offset measurements of the proposed 1-V OpAmp under the heavy load.

Table 6.2 1-V OpAmp Power Consumptions

	Simulations		**Measurements**	
Load	1MOhm//15pF	3.3KOhm//50pF	1MOhm//15pF	3.3KOhm//50pF
V_{input} **(V)**	0	0	0	0
Power Consumption (µW)	180	261	197	254

6.1.4.2 OpAmp Open Loop Gain (A_o)

The open loop gain (A_o) is another important parameter of any OpAmp as it directly decides its linearity. For OpAmps with open loop gain less than 60 dB, an open loop configuration is sufficient to measure their A_o. However, high-gain OpAmps require the close loop configuration with unity-gain and inverting topologies. The test setup for measuring the open loop gain is illustrated in Fig. 6.12. Large feedback resistors of 470 KOhm are used to reduce their effects on loading the OpAmp output. By applying a 200 mV V_{PP} sinusoidal signal using a network analyzer, the open loop gain A_o can be calculated as,

$$A_o = \frac{V_{out}}{V_e} \tag{6.3}$$

where V_e is the error voltage measured at the negative input of the OpAmp at one specific frequency. The network analyzer has an internal sine-wave synthesizer, which prevents any spectral leakage during the FFT analysis of the output of the OpAmp. The probing of this error voltage at the OpAmp input introduces a stray capacitance, which forms a low-frequency pole in the feedback loop. Therefore, a feedback capacitor of 10 pF is also required to cancel this low-frequency pole.

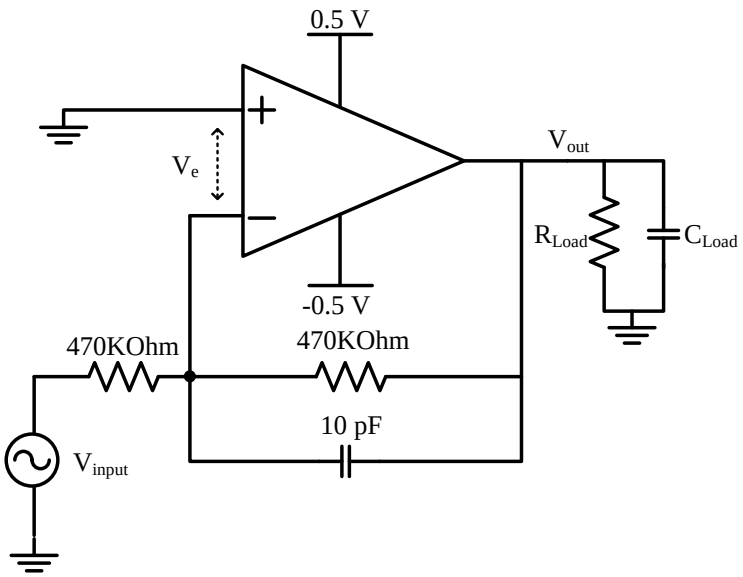

Fig. 6.12 Test setup for measuring the open loop gain.

The open loop gain of this OpAmp is characterized for frequencies ranging from 100 Hz to 10 KHz under both the light load and the heavy load conditions. The unity-gain bandwidth (UGBW) can be derived by extrapolating the plot with a -20 dB/decade slope to cross the 0 dB line and assuming this OpAmp to be an ideal single pole system. Fig. 6.13 and Fig. 6.14 show the measured (Blue dot) and the simulated (Green curve) open loop gains under both loads at the common mode input of 0 V. The measured data is also extrapolated as displayed by the blue curve. The measured A_o at DC are 88.3 dB and 70 dB under different loads which are about 4.5 ~ 5 dB larger than the simulated ones. The extrapolated UGBW are 10 MHz and 7.7 MHz, respectively, which is around 2.5 ~ 2.7 times that of the simulated ones. The larger-than-simulation results originate from both the underestimated bulk transconductance in the model and the process variations from the foundry.

The open loop gain A_o is also characterized at different common mode voltages V_{input} under both loads for two chip samples. In Fig. 6.15, under the light load, the common mode input range is swept from -200 mV to 400 mV, while under the heavy load; V_{input} is swept from -200 mV to 300 mV. These ranges are selected based on the previously measured ICMR of this OpAmp under both loads.

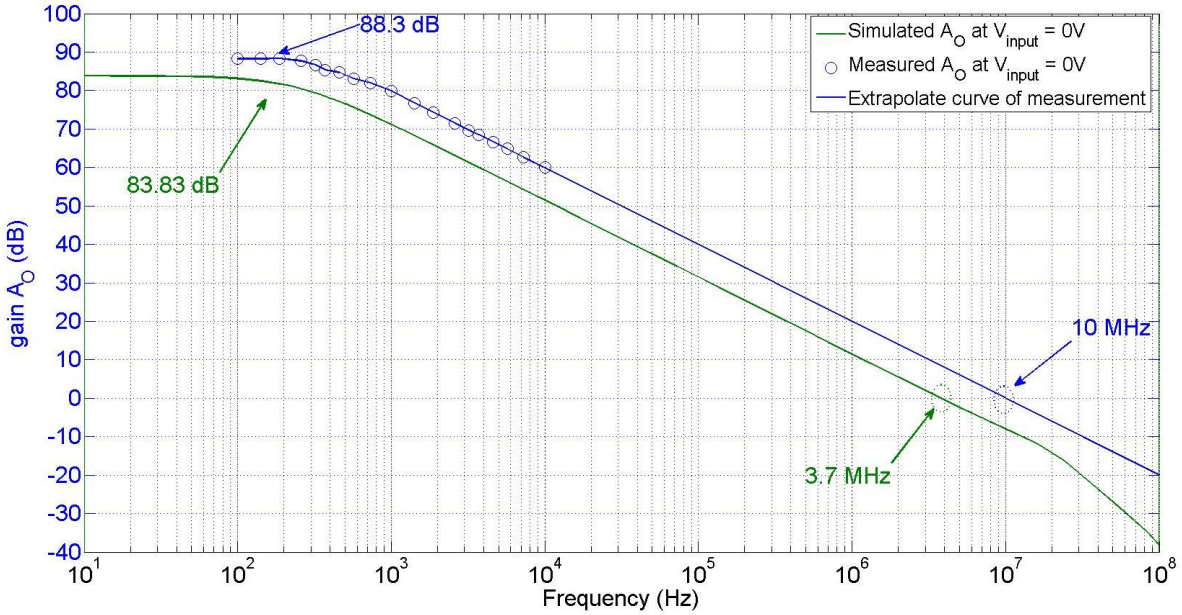

Fig. 6.13 Measured and simulated open loop gain A_o at V_{input} = 0 V under the light load.

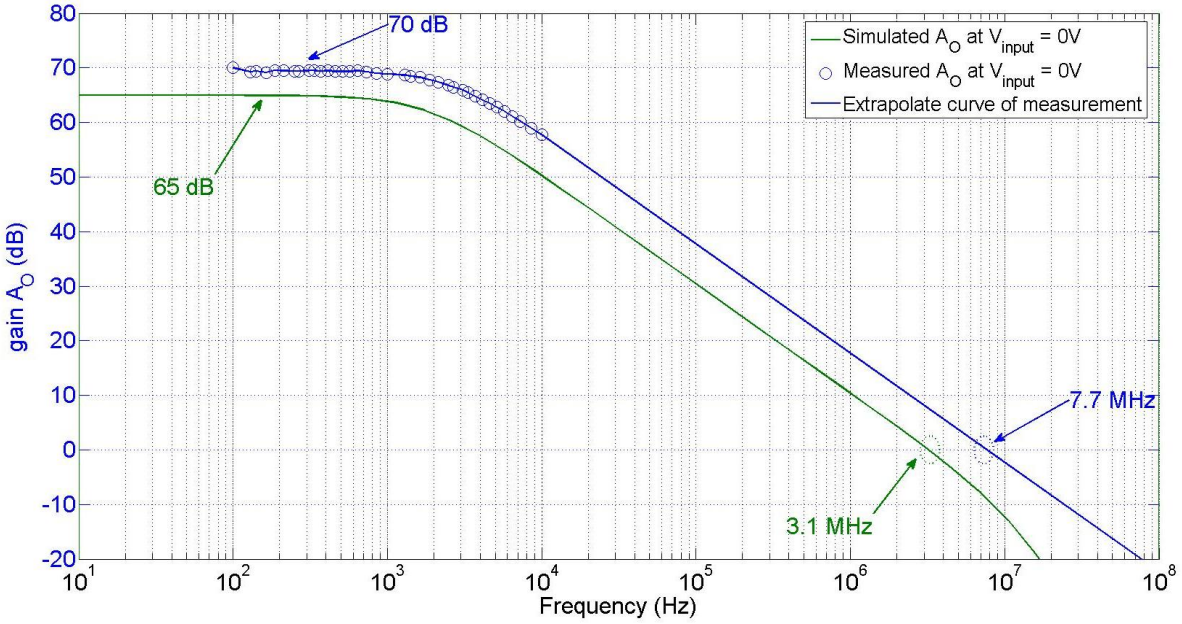

Fig. 6.14 Measured and simulated open loop gain A_o at V_{input} = 0 V under the heavy load.

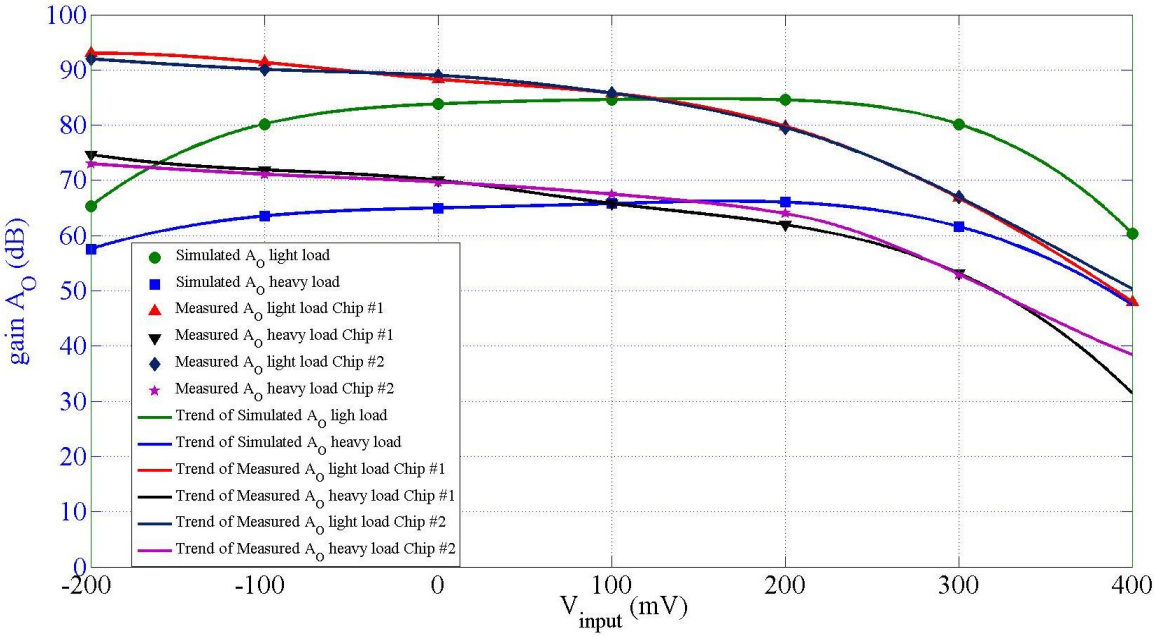

Fig. 6.15 Open loop gain A_o at different V_{input} under both loads.

The extrapolated UGBW from each gain measurement in Fig. 6.15 are also compared with the simulation results as shown in Fig. 6.16. The results from two chip samples show significant improvement of the UGBW from measurements to simulations. This mostly comes from the underestimation of the input transconductance $G_{m\_in\_eff}$ in simulations. The rough estimations of the UGBW by ignoring non-dominant poles and zeros effect also contribute to this discrepancy.

Both the trends of the measured and the simulated A_o and UGBW along with the input voltage are quite consistent with the input transconductance measurements and simulations presented in Fig. 6.5 and Fig. 6.6, respectively, where the measured highest open loop gain A_o and UGBW occur at the input voltage of -200 mV, while the simulated A_o and UGBW reach their peak at input voltage of ~200 mV. On the other hand, the measured A_O drops below the simulated ones at high V_{input}. This is due to the aforementioned potential gain deteriorations from the biasing transistors inside the input stage and the level shift inside push-pull output stage at high input/output voltages.

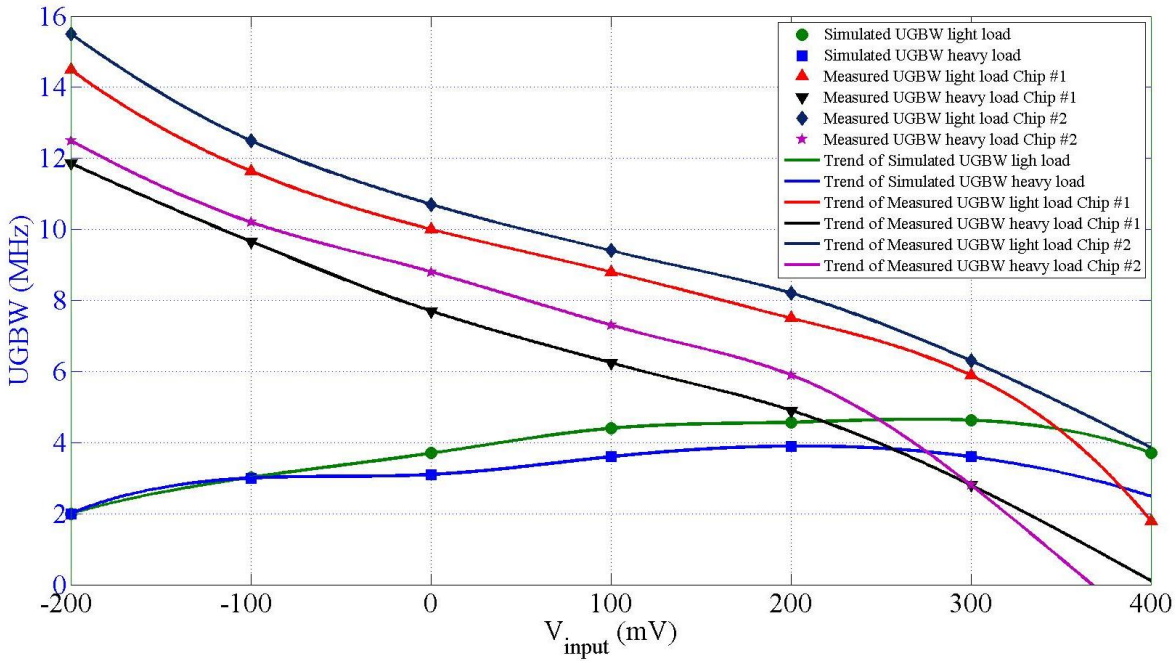

Fig. 6.16 UGBW at different V_{input} under both loads.

6.1.4.3 Small Signal and Large Signal Transient Response

Important parameters such as rise time, fall time and slew rate can be obtained by applying small or large transient signals to the positive input of the unity-gain non-inverting configured OpAmp and measuring the output transient response. The test setup for the transient response measurements can be referred to the one in Fig. 6.9. A function generator and an oscilloscope are employed to create transient signals and capture the transient output signals.

For the small signal analysis, a square wave of 50 mV V_{pp} is generated by the function generator at 10 KHz. Transient signals are measured under the light load and the heavy load, respectively. Fig. 6.17 and Fig. 6.18 specifically reveal the rising and the falling edges of the small signal responses at the input voltage of 0 V under both loads. The purple curves are the input square wave signals and the green curves are the output transient responses.

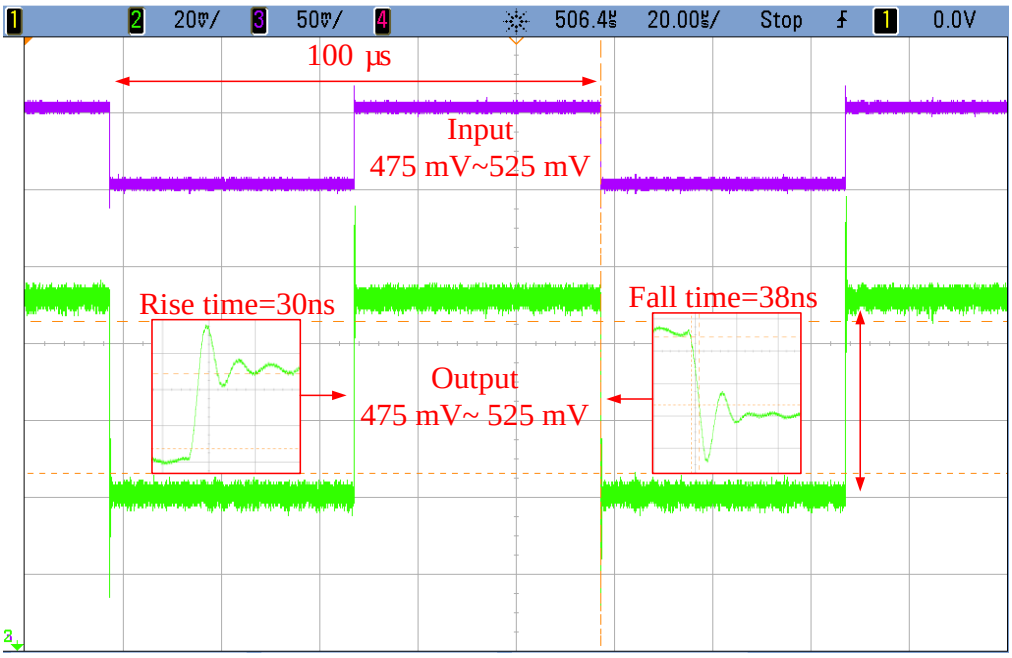

Fig. 6.17 Small signal response measurement under the light load at V_{input} = 0 V.

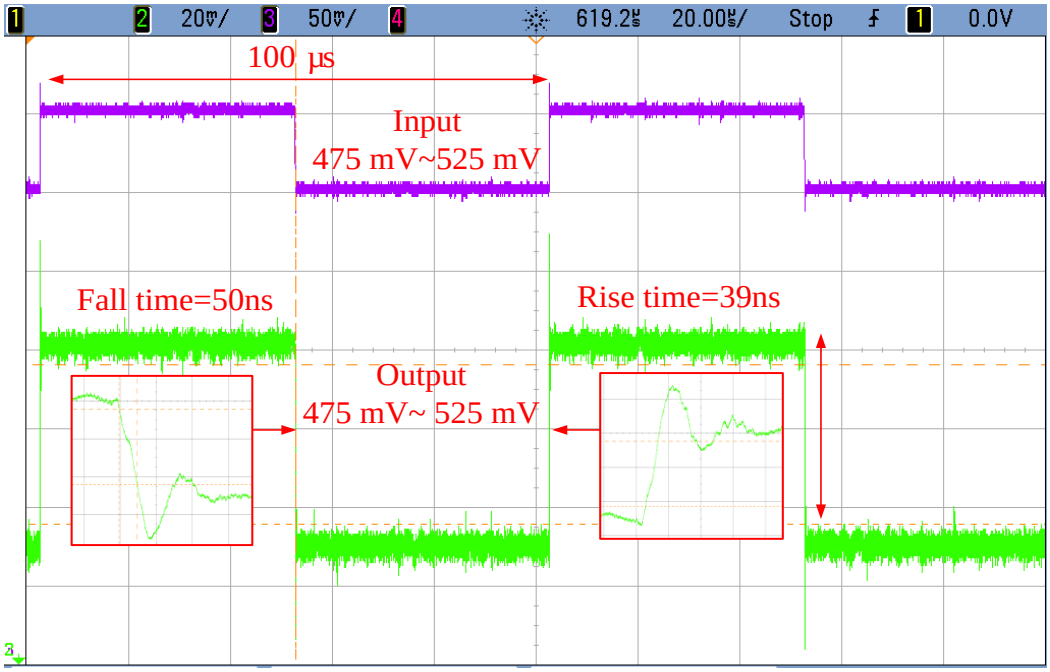

Fig. 6.18 Small signal response measurement under the heavy load at V_{input} = 0 V.

The UGBW can be calculated using Eq. (6.4) based on the rise time of the small signal response. The UGBW is more accurate than the one measured in Fig. 6.16 since it includes the effects from non-dominant poles and zeros existing close to the bandwidth.

$$\boldsymbol{UGBW} = \frac{0.35}{\boldsymbol{t_{rise}}(10\%-90\%)} \tag{6.4}$$

The UGBW at different input voltages are then calculated after obtaining various small signal transient responses under both loads. Fig. 6.19 reveals their values. They generally descend as the input voltage increases which conforms to previous measurements.

For the large signal transient response, a 0.6 V V_{pp} input square wave signal is applied to the OpAmp at 10 KHz under the light load, while a 0.55 V V_{pp} input square wave signal is applied under the heavy load. Fig. 6.20 and Fig. 6.21 show the large signal transient responses under both loads, respectively. The purple curves are the input square wave signals, and the green curves represent the output transient responses. Both positive and negative slew rates can be characterized from the measurements of the rise and fall times.

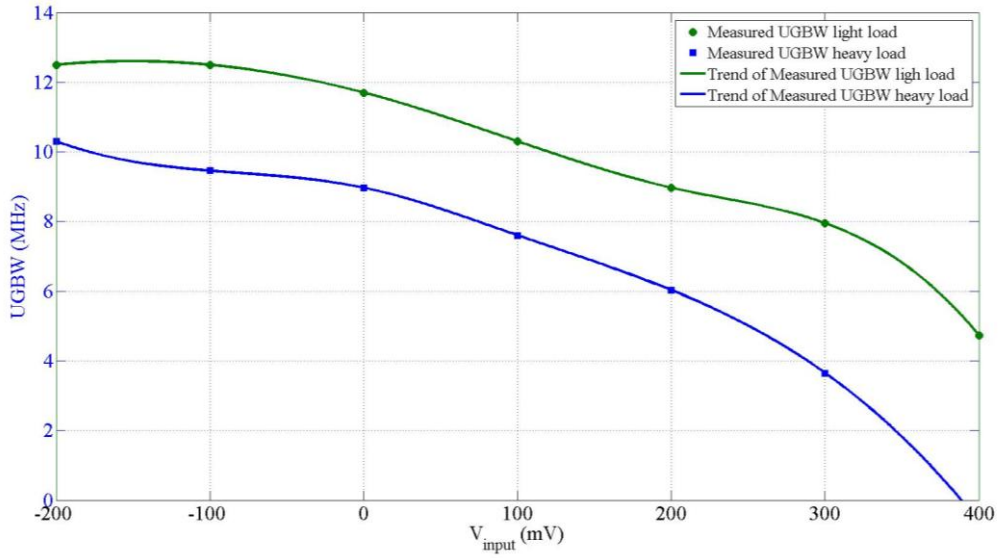

Fig. 6.19 UGBW calculated from the measured small signal responses.

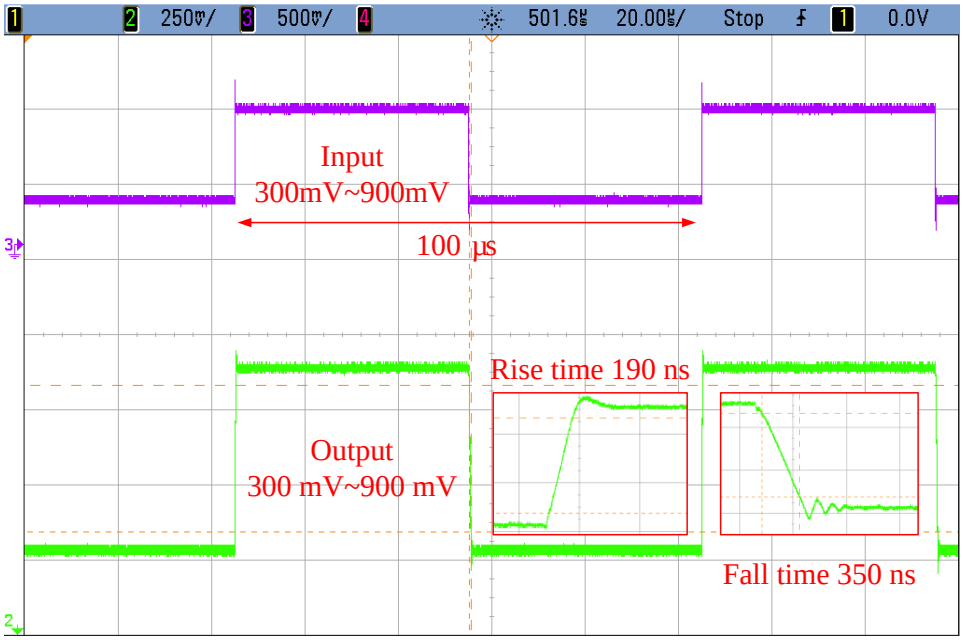

Fig. 6.20 Large signal transient response under the light load.

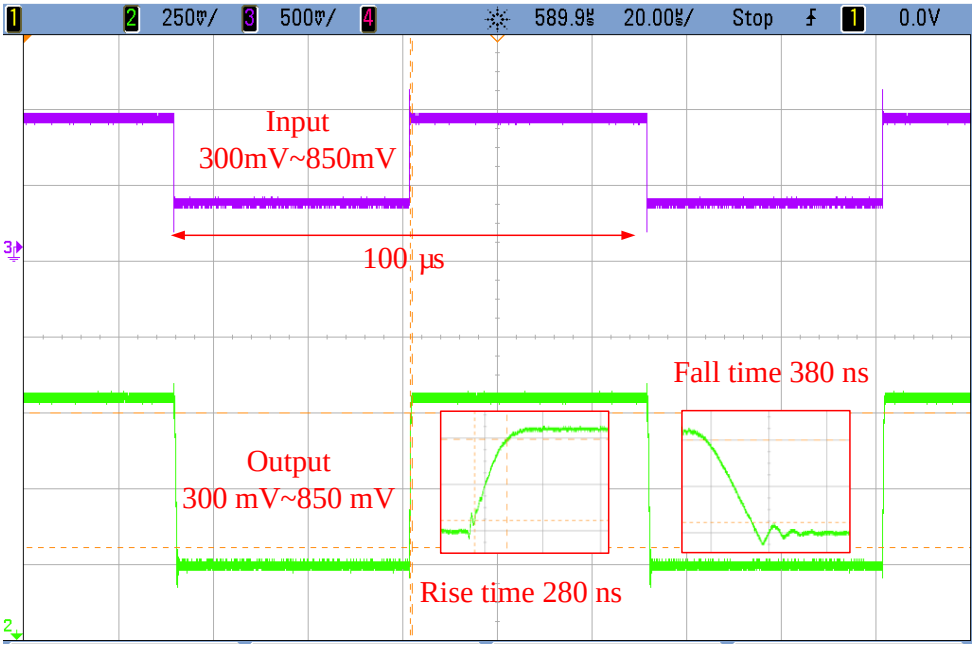

Fig. 6.21 Large signal transient response under the heavy load.

Table 6.3 compares the simulated and measured slew rates. Considering the power consumptions are fairly consistent between simulations and measurements, the higher-than-simulation slew rates result from the process, especially the capacitance variations from chip to chip.

6.1.4.4 Noise Characterization

The input referred noise is measured using the test setup in Fig. 6.22. The OpAmp is configured as a non-inverting buffer whose input is tied to ground. Due to the noise level in the spectrum analyzer, it is better to measure the OpAmp output noise by amplifying it first. A low-noise preamplifier (LNA) is used where its gain maintains 60 dB up to 1 MHz and its output impedance is 450 Ohm. Since the input impedance of spectrum analyzer is 50 Ohm, the output noise of the OpAmp can be amplified by 100 times up to 1MHz. The Labview program is used to capture the noise data. In Fig. 6.23, the noise measurement is performed between 1 KHz to 1 MHz by averaging more than 10 sets of the noise data. The measured output noise, combining both the flicker noise and the thermal noise, of the proposed bulk-driven OpAmp is substantially smaller than the simulated one thanks to the underestimated $G_{m\_in\_eff}$ in simulations. The averaged thermal noise is less than 60 nV/$\sqrt{Hz}$ at 1 MHz.

Table 6.3 Simulated and Measured Slew Rates

	Positive slew rate (mV/ns)	**Negative slew rate (mV/ns)**
Simulation (Light load)	2.01	1.04
Measurement (Light load)	2.53	1.37
Simulation (Heavy load)	1.63	0.91
Measurement (Heavy load)	1.57	1.16

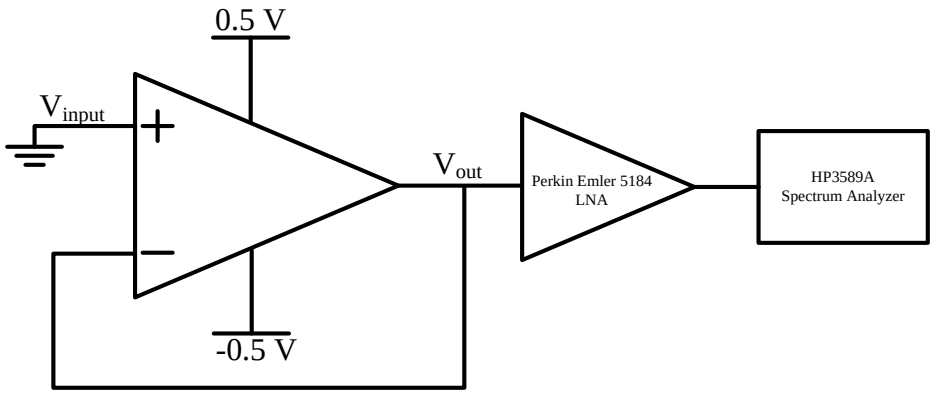

Fig. 6.22 Test setup for the noise measurement.

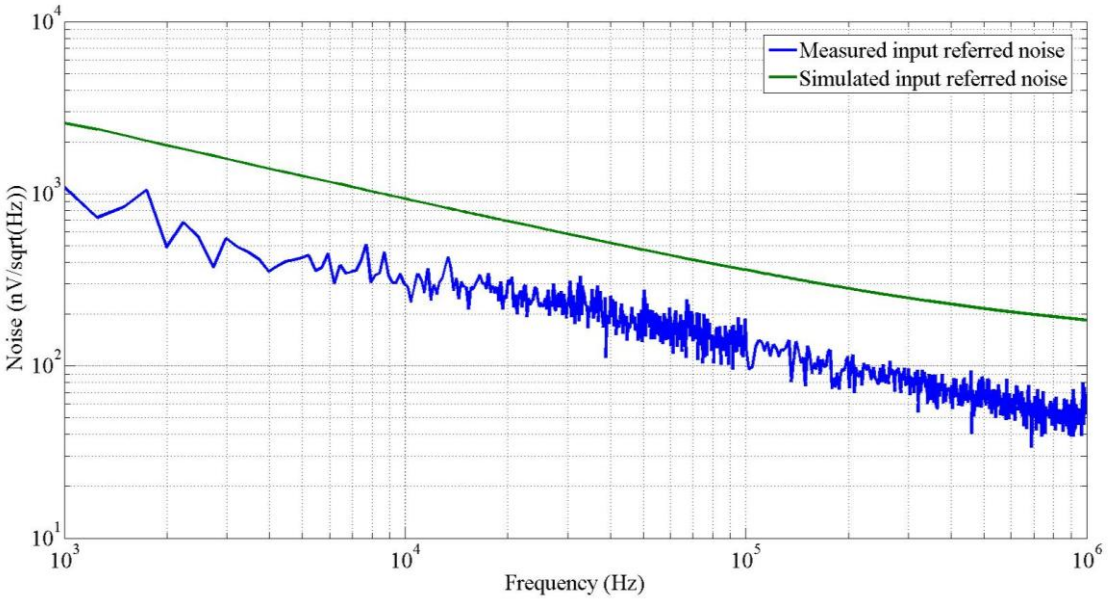

Fig. 6.23 Input referred noise comparison between the measurement and the simulation.

6.1.4.5 PSRR Measurements

The power supply rejection ratio (PSRR) characterizes the ability of the OpAmp to reject the noise on the power supply rails. In this work, PSRR at DC is measured at both positive and negative power supply rails. The test setup is illustrated in Fig. 6.24, where the OpAmp is configured as unity-gain and non-inverting. The complimentary power is supplied by the Keithley 2400 source meters. The

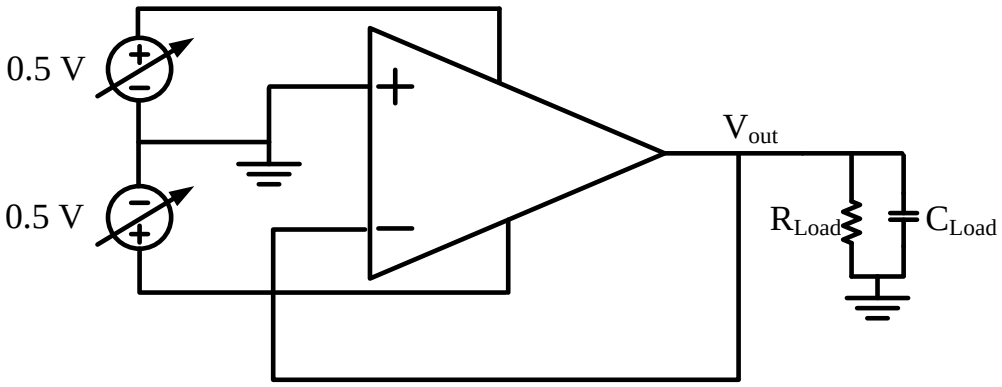

Fig. 6.24 Schematic of the OpAmp PSRR measurement setup.

variations on the OpAmp output under the light load can be measured by sweeping either one of the power supplies.

Fig. 6.25 shows the measured PSRR± under the light load with common mode input voltage of 0 V and ±20% variations on the complimentary power supplies. The power supply rejection ratios are also characterized under different input common mode voltages from -200 mV to 400 mV as shown in Fig. 6.26. Compared with the simulation results, inferior power supply rejection ratios are obtained at positive and negative power rails (i.e. 5dB~10dB less) thanks to the process variations during chip fabrications.

6.1.4.6 CMRR Measurements

Common mode rejection ratio (CMRR) is another important performance of an OpAmp, which can characterize its ability to reject common mode signals at its inputs. Specifically, it represents the ratio of the differential open loop gain to the common mode open loop gain. At DC, CMRR can be measured using the close loop test setup in Fig. 6.27. In this configuration, a driver OpAmp with very low offset (i.e.OP-27) is employed by maintaining its output ($V_{out,driver}$) at $2\times V_{input}$, which is expressed in Eq. (6.5). The output of the 1-V OpAmp is then fixed at 0 V. Fixing the 1-V OpAmp output voltage can reduce the effect of power supply variations on the OpAmp output.

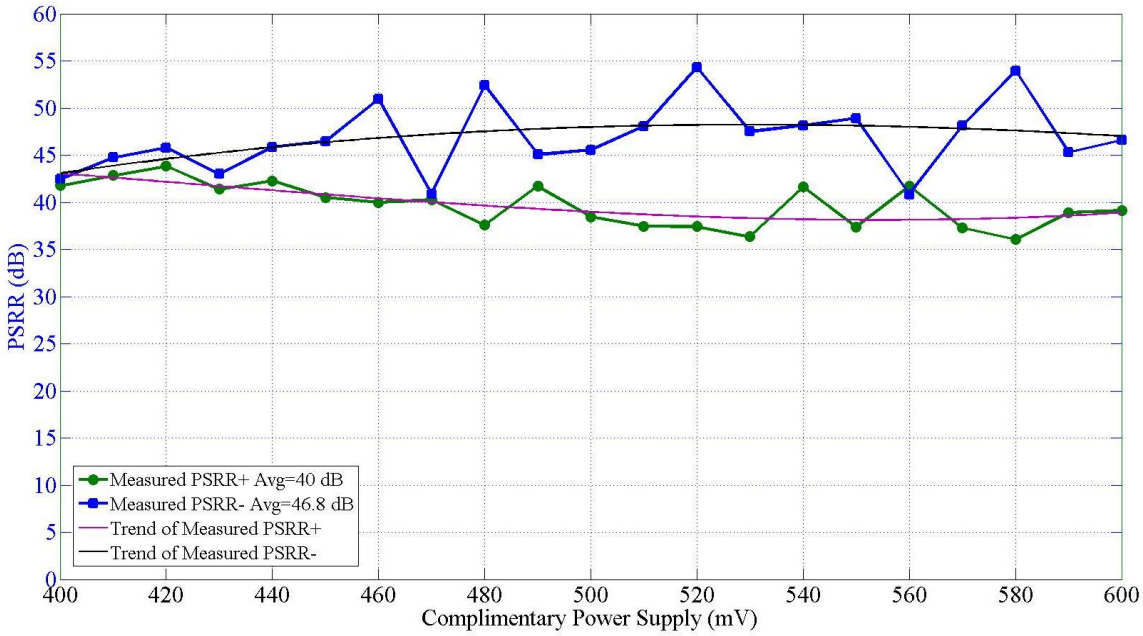

Fig. 6.25 PSRR ± measurements at input voltage of 0 V.

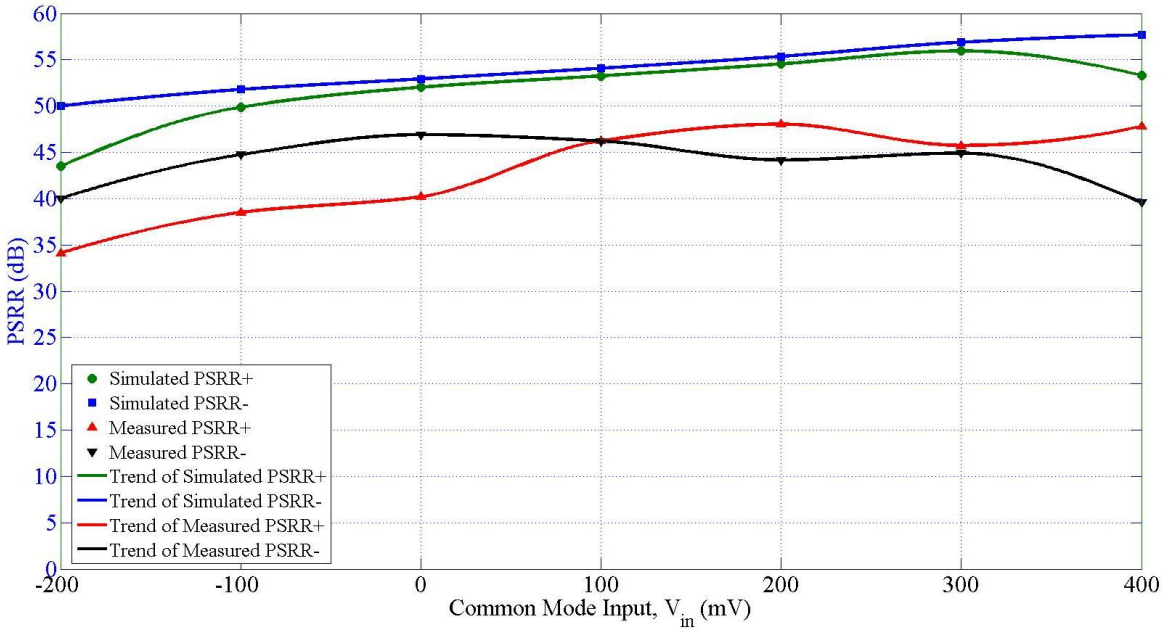

Fig. 6.26 Simulated and measured PSRR ± under different input voltages.

$$\boldsymbol{V_{out,driver}} = \frac{330\boldsymbol{KOhm}}{660\boldsymbol{KOhm}}(\boldsymbol{V_{input}} + 0.5\boldsymbol{V} - 0.5\boldsymbol{V} + \boldsymbol{V_{input}}) + \boldsymbol{V_{input}} = 2 \bullet \boldsymbol{V_{input}} \tag{6.5}$$

By sweeping the V_{input}, the error voltage V_{ID} is varied accordingly. The CMRR can be calculated using Eq. (6.6) as,

$$\boldsymbol{CMRR} = \frac{\dfrac{\boldsymbol{dV_{out}}}{\boldsymbol{dV_{ID}}}}{\dfrac{\boldsymbol{dV_{out}}}{\boldsymbol{dV_{input}}}} = \frac{\boldsymbol{dV_{input}}}{\boldsymbol{dV_{ID}}} \tag{6.6}$$

The CMRR of the 1-V OpAmp is measured under the light load by sweeping the overall ICMR from -200 mV to 500 mV. The result is then curve fitted and compared with the simulation data in Fig. 6.28. It can be concluded that the measured CMRR is lower than the simulated ones especially at input voltages from -100mV to 300 mV. This is because of the aforementioned variations of the offset voltage at different input common mode voltages, which further result from both the random and the systematic mismatches in this OpAmp circuit.

6.1.4.7 Summary of the 1-V OpAmp Performance

Table 6.4 summarizes the performance of the proposed 1-V bulk-driven OpAmp. The measurement results listed here are all performed at the common mode input voltage of 0 V given that a complimentary power supplies ± 0.5 V are applied. According to these results, the proposed OpAmp is able to maintain more than 70 dB open loop gain while having sufficient phase margin to guarantee stable operations under both the light load and the heavy load. Due to the low-voltage class AB output stage employed in this design, the power consumption changes greatly at various loads.

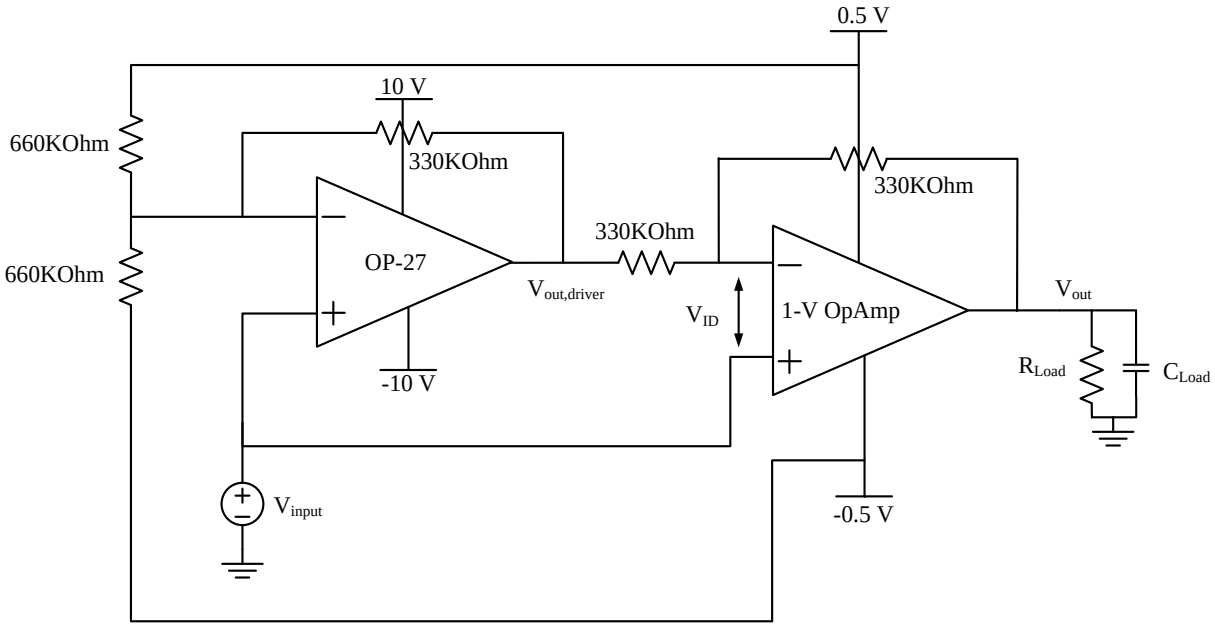

Fig. 6.27 Schematic of the test setup for CMRR measurements.

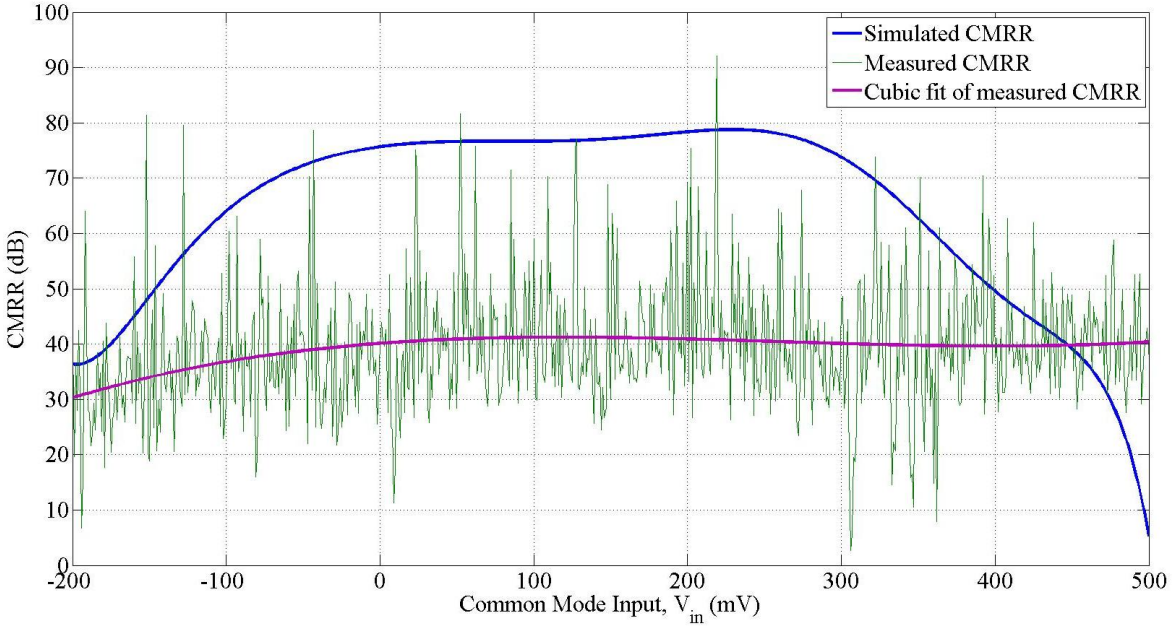

Fig. 6.28 Measured CMRR over ICMR, and its comparison with the simulation.

Table 6.4 Performance Summary of the Proposed OpAmp

Technology (0.35μm, ±0.5 V Supply)	**Units**	**Load**	
		1 MΩ || 15 pF	3.3 KΩ||50 pF
DC Open loop gain	dB	88.3	70
UGBW	MHz	11.67	8.97
SR+/SR-	V/μs	2.53/1.37	1.57/1.16
ICMR	mV	700	660
Offset Voltage*	mV	8.4,10	10,10.9
Input Current	nA	<10	
Power Consumption	μW	197	254
Noise (@1 MHz)	$nV/Hz^{1/2}$	<60	
CMRR@DC	dB	40	
PSRR+/PSRR-@DC		40/46.8	

*Two chip samples

6.1.5 1-V OpAmp Comparisons with the State of the Arts

The performance of the proposed 1-V bulk-driven OpAmp are also compared with previous bulk-driven amplifier works [56][60] in Table 6.5 with the input common mode voltage at the middle of the power supplies. Both works proposed transconductance boosting techniques employing positive feedback configurations in a 0.35 μm n-well CMOS process.

In addition, a figure of merit (FOM) is also used for performance comparisons of some sub 1-V amplifiers proposed in recent years in Fig. 6.29. The FOM is expressed in Eq. (6.7),

$$\boldsymbol{FOM} = 100 \times \frac{\boldsymbol{UGBW \bullet C_L}}{\boldsymbol{I}} \tag{6.7}$$

where *I* is the overall circuit current consumption. Apparently, this FOM is able to present the bandwidth and drive capability of the amplifiers proposed in different years. Amplifiers with larger UGBW, heavier loading capacitance, and smaller current consumption demonstrate better FOM values. The performance of the 1-V OpAmp is among the tops in Fig. 6.29. The only two works with higher FOM are not general

purpose amplifiers and are with gate-driven input stages.

Table 6.5 Comparisons Between the Bulk-Driven Amplifiers with Transconductance Enhancement

	Proposed(Measurement)		**[56] (Measurement)**		**[60] (Simulation)**	
Process	0.35 μm n-well CMOS					
Supply voltage (V)	1					
Load	1 MΩ || 15 pF	3.3 KΩ||50 pF	1 MΩ || 17 pF	3.3 KΩ||50 pF	320KΩ|| 1pF	16KΩ|| 20pF
Power consumption (μW)	197	254	358		130	
Open loop gain (dB)	88.3	70	76.2	59.1	64	55
Unity gain bandwidth (MHz)	11.67	8.97	8.1	5.9	1.93	1.6
SR+/SR- (V/μs)	2.53/1.37	1.57/1.16	2.74/5.02	2.66/4.51	0.7	
ICMR(mV)	700	600	1000	930	700	700
Offset Voltage(mV)	8.4,10	10,10.9	2.88±1.26(1σ)	2.91±1.23(1σ)	10 (1σ)	
Offset Tuning Circuit	No		Yes		No	
Maximum Input Current (nA)	<10		2.15		<10	
Phase margin	-	-	-	-	44˚	36˚
Theoretical $G_{m\_in\_eff}$ enhancement	10		3 (w/o current gain)		8	
Input stage current consumption (μA)	25		53 (w/o current gain)		40	
Noise (nV/ $Hz^{1/2}$) @1MHz	<60		< 300		165	
CMRR (dB) @DC	40		70.5		-	
@ 100KHz	-		-		68	
PSRR ± (dB)@DC	40/46.8		45.0/40.5		-	
@ 10KHz	-		-		70	
Die Area (μm* μm)	525 300		140 380		250 250	

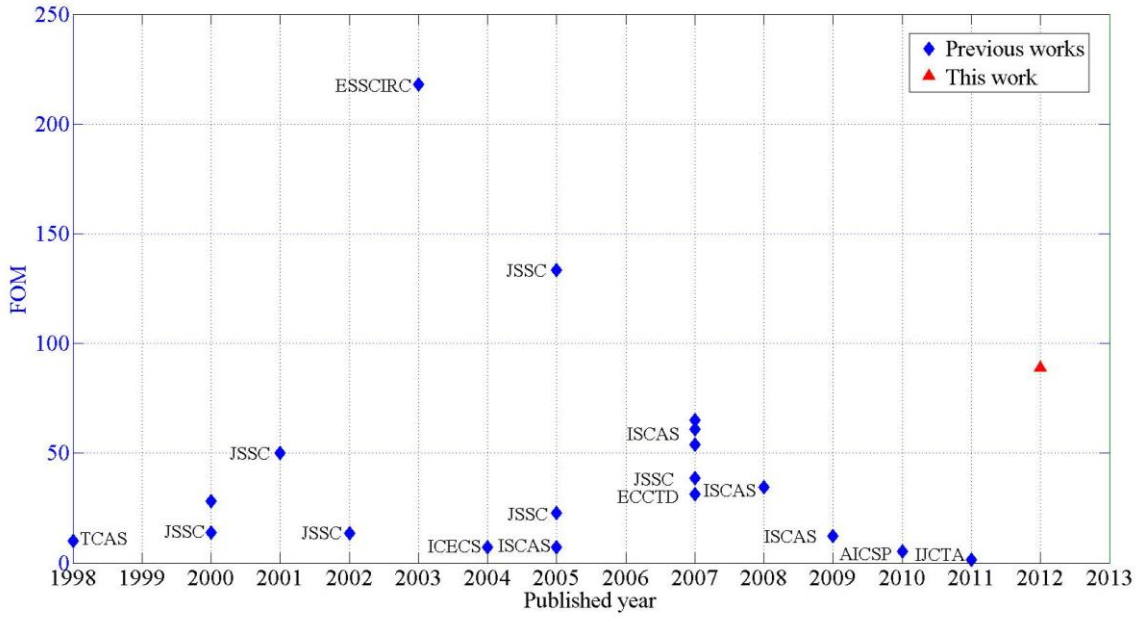

Fig. 6.29 FOM versus the year of publication.

6.2 Characterizations of the 1-V Potentiostat

In this work, the 1-V potentiostat is characterized by employing it in continuous glucose monitoring with an implantable glucose sensor. The three-electrode sensor is developed by our collaborators at the University of Connecticut. The working and the reference electrodes are made by coiling 125 μm platinum (Pt) wire and silver (Ag) wires close to the working electrode. The surface of the silver wire is then converted to AgCl through galvanometry in HCl solution on a stirring plate where the Ag/AgCl reference electrode is fabricated. Another Pt coil forms a counter electrode by placing it next to the reference electrode.

6.2.1 1-V Potentiostat Test Environment

The 1-V potentiostat circuit is tested on a Vector PC board. Since the signal process unit (i.e. *I-F* converter) is taken from the circuit proposed in [4], different power supplies are required for these two

circuits. This potentiostat is not only tested with the sensor models composing of physical resistors and capacitors, but also with the O_2 based glucose detection sensor in the stirred Phosphate-Buffered Saline (PBS) solution (pH 7.4) maintained at 37 ˚C. The test board with its connections of the sensors dipped in the solution is shown in Fig. 6.30. Other equipments employed in this test are listed in Table 6.6.

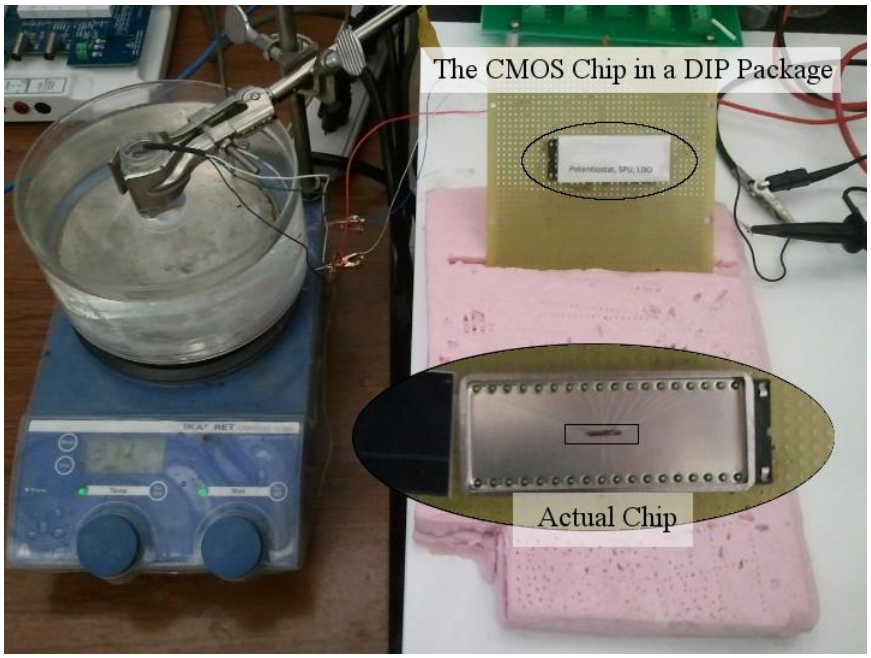

Fig. 6.30 Test setup for the 1-V potentiostat with a glucose sensor.

Table 6.6 Test Equipments for the 1-V Potentiostat

Type	Features
Agilent E3631A Triple Output DC Power Supply	0~6V;-25V~25V
Source Meter Keithley 2400	Five instruments in one (IV Source, IVR Measure)
Agilent MSO6052A Mixed Signal Oscilloscope	500MHz Bandwidth, 4Gsample per second.
Stirring Plates	N/A
AD8512	Low offset and low input bias current Amplifier

6.2.2 Simulations and Measurements of the 1-V Potentiostat with Resistor and Capacitor Sensor Models

The physiologically observed glucose concentration inside human bloodstream is from 2 mM/Liter to 22 mM/Liter. This glucose concentration corresponds to 0.1 μA to 1.5 μA of the sensor current. To leave some margin, this 1-V potentiostat is designed to provide sensor current with dynamic range from 70 nA to 2.6 μA.

As shown in Fig. 2.2, considering the potential E_i is 700 mV (i.e. V_{WR}=700 mV) for the working electrode to get oxidized, the sensor model resistance of R_{WE} could vary from 10 MOhm to 250 KOhm while the model resistance R_{CE} is usually constant at 10 KOhm. The capacitance of both the working and the counter electrodes are also modeled as C_{WE} is around 300 nF, and C_{CE} is about 10 nF. In this work, this potentiostat is initially simulated and measured using a glucose sensor model consisting of only resistors and capacitors.

Fig. 6.31 illustrates the simulation data versus the measurement data of the 1-V potentiostat connecting with the aforementioned sensor model. Two chips are characterized and both the simulated and the measured output signal periods (reciprocal of output frequency) varied linearly with the increment of the resistor modeled as R_{WR} (reciprocal of sensor current). The linear regression factors (R^2) of all these curves are calculated to be more than 0.997. The slight discrepancies between the simulated and the measured results are due to the on-chip variations of the integrating capacitor inside the current-to-frequency converter developed in [4].

The variations of the voltage between the working and the reference electrodes are also measured in Fig. 6.32. Two low-offset and high-input-impedance commercial amplifiers are configured as the unity-gain non-inverting buffers to output the voltage difference so that any resistive load of the working and the reference electrodes can be avoided. Fig. 6.32 shows that the potential E_i is maintained relatively constant over the whole range of R_{WR}. The small deviations from the ideal 700 mV are due to the offset in

the potentiostat system, which are in the error range. The variations of the V_{WR} are negligible which prove good linearity of the proposed potentiostat.

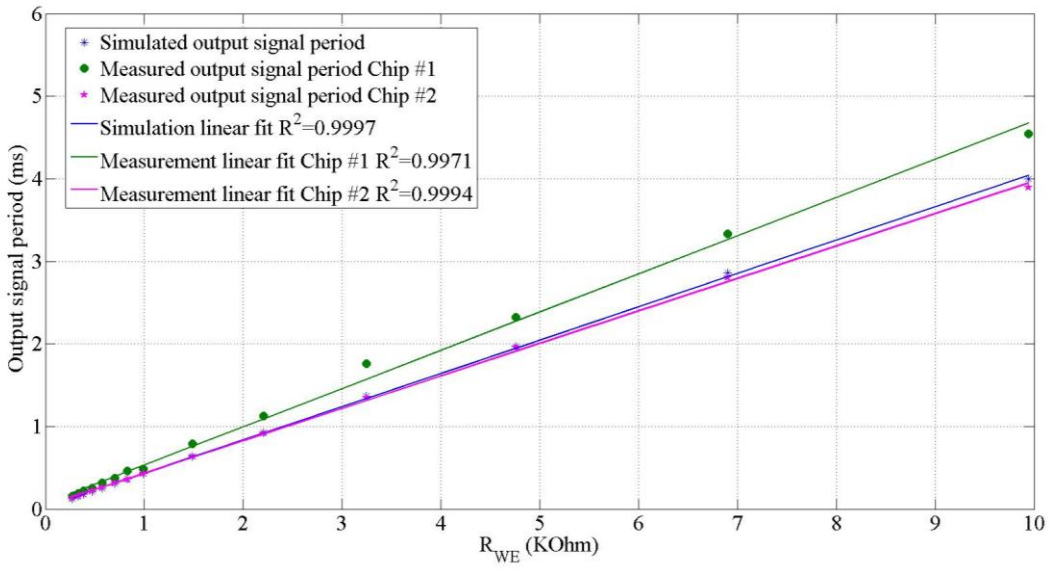

Fig. 6.31 Simulation and measurements of the 1-V potentiostat output signal period with variations of $R_{WE.}$

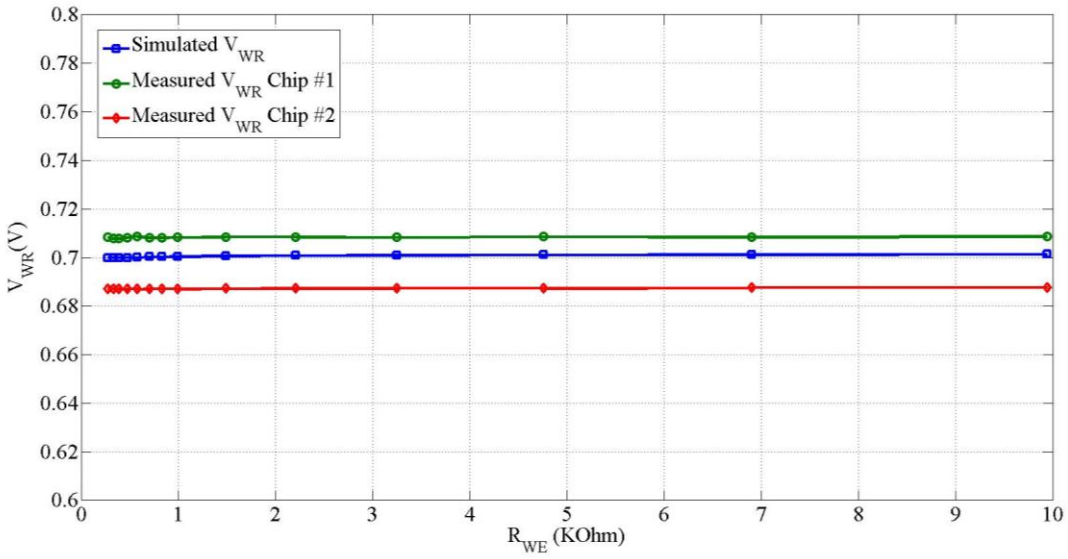

Fig. 6.32 Simulation and measurements of the potential E_i applied between the working and the reference electrodes.

6.2.3 *in vitro* Measurements of the 1-V Potentiostat with a Biosensor

This potentiostat is measured with the aforementioned three-electrode glucose sensor. The sensor current is obtained by raising the glucose level in the PBS solutions from 0 mM/Liter to 30 mM/Liter. The glucose is added 2 mM every 100 seconds before an initial background stabilization period of around 8 minutes.

The measured output frequency with the variation of the glucose concentration is shown in Fig. 6.33 Overall, the 1-V potentiostat exhibits good linearity within the glucose concentration up to 30 mM/Liter, which is well beyond the physiological range inside the human body (i.e. 2 mM/Liter to 22 mM/Liter). The measured output frequency shows better than 0.6% accuracy.

6.2.4 Comparisons Between this Work and Prior Arts

The performance of the 1-V potentiostat is compared with other works in Table 6.7. The proposed work shows significant reduction in the power consumption and the supply voltage while still maintaining comparable linearity.

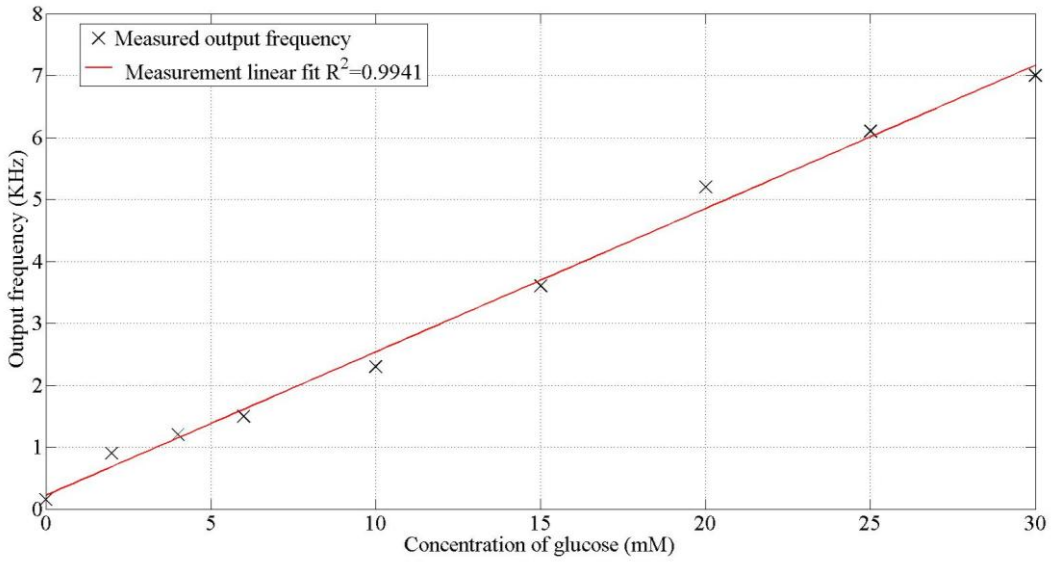

Fig. 6.33 Measurement of the 1-V potentiostat with a three-electrode glucose sensor.

Table 6.7 Comparisons Between Proposed Work and Previous Literatures

	Process	**Supply voltage (V)**	**Power consumption of the potentiostat**	**Linearity**	**Detected sensor current Range**	**Topology**
Proposed work	0.35 µm n-well CMOS	1	22	R^2=0.9941	70 nA -> 2 .6µA	SE
[4]	0.35 µm n-well CMOS	1.5	400 (Including SPU)	R^2= 0.999	200 nA->2 µA	SE
[14]	0.18 µm n-well CMOS	1.8	32.4	R^2= 0.9984	1 nA -> 1µA	SE
[26] (Simulation)	0.18 µm n-well CMOS	1.8	80	N/A	1nA->200nA	SE
[33]	0.18 µm n-well CMOS	1.8	15840	R^2= 0.98	N/A	FD
[36]	0.18 µm n-well CMOS	1.8	307	N/A	10nA -> 10µA	SE

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

In this dissertation, the importance of the low-voltage and low-power operation of the implantable biosensor system is first discussed. Consequently, a 1-V potentiostat working with electrochemical sensors is developed. The potentiostat includes a 1-V bulk-driven amplifier as the core. The presented a 1-V bulk-driven amplifier is designed to improve its effective input transconductance. Innovative low-voltage bulk-driven design techniques have been proposed to boost the transconductance. The performances of the amplifier such as UGBW and open loop gain are all improved. The amplifier can also connect to 1-V compatible push-pull output stage which can drive a heavy load. The circuit has been implemented using a 0.35μm standard CMOS process.

7.2 Future Work

7.2.1 1-V OpAmp Offset Tuning Circuit

An offset tuning circuit is useful for the 1-V bulk-driven OpAmp. The overall offset voltage varies with the common mode input voltage in the proposed OpAmp. Offset tuning circuits can be developed to tune the offset of the input stage or the output stage of the OpAmp without degrading the performance too much. Specifically, an offset tuning circuit has been developed in [56] for compensating the offset generated by the output push-pull stage. The basic idea is to tune the level-shift transistor drain current so that the output push-pull stage static biasing conditions can be changed.

7.2.2 Bandgap Reference (BGR) for the 1-V Potentiostat

A reference circuit can be used in this work to generate necessary reference voltage for the potentiostat. Fig. 7.1 illustrates the topology of the reference circuit [44]. The idea behind it involves adding both proportional to absolute temperature (PTAT) and complementary to absolute temperature (CTAT) currents together to a resistor such that a constant reference voltage can be generated. Instead of using cascode current mirrors to precisely mirror current and force voltages at node A and B equal an OpAmp circuit is utilized to achieve the same function.

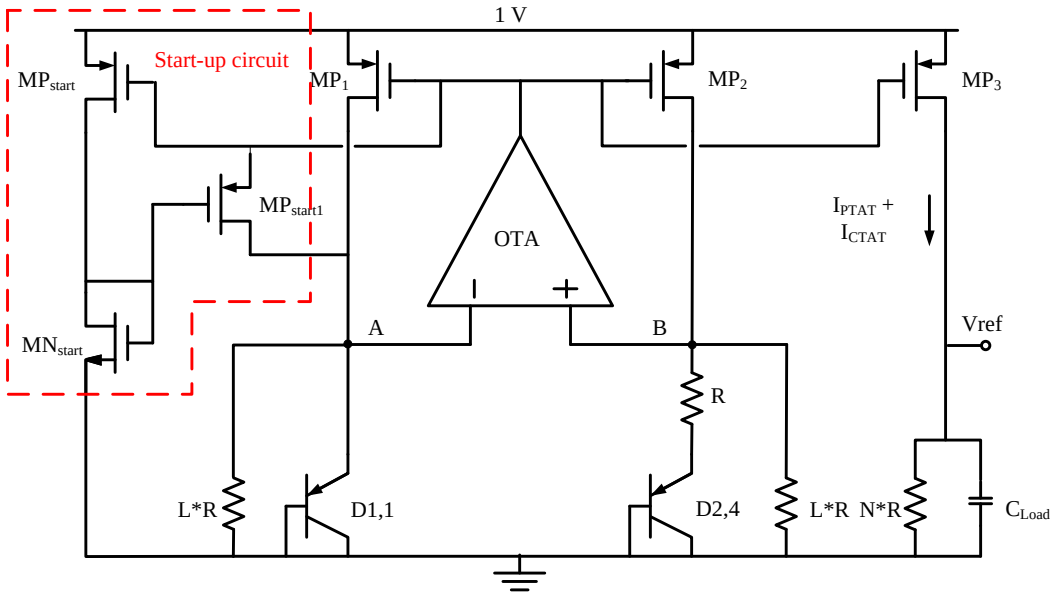

Fig. 7.1 Schematic of the 1-V reference circuit.

The PTAT current is generated by diodes *D1*, *D2* and resistor *R*. It can be calculated as follows,

$$\boldsymbol{I_{PTAT}} = \frac{\boldsymbol{nV_T} \times \ln 4}{\boldsymbol{R}} \tag{7.1}$$

where n is the emission coefficient, V_T is the thermal voltage which is given by $k_B \times T/q$ where k_B is Boltzmann's constant and T is the temperature in Kelvin.

The CTAT current is due to *D1* and resistor *L* R*, which is given by,

$$\boldsymbol{I_{CTAT}} = \frac{\boldsymbol{V_{D1}}}{\boldsymbol{L} \times \boldsymbol{R}} \tag{7.2}$$

The sum of both currents is mirrored and supplied to the resistor $N \times R$. Thus the reference voltage can be expressed in as,

$$\boldsymbol{V_{ref}} = \boldsymbol{nV_T} \times \ln 4 \times \boldsymbol{N} + \frac{\boldsymbol{N}}{\boldsymbol{L}} \times \boldsymbol{V_{D1}} \tag{7.3}$$

The first term has a temperature coefficient (TC) of 0.085 mV/C, while the second term has a TC of -1.6 mV/C. By tuning the value *L*, those two terms can be cancelled out leaving the reference voltage relatively constant throughout the operating temperature range. Then by selecting desired *N* an output voltage of 300 mV can be achieved.

For the OpAmp circuit inside, a conventional gate-driven amplifier is difficult to implement to achieve 1-V operation under this long channel CMOS process. Therefore, a simple bulk-driven folded cascode structure is adopted as shown in Fig. 7.2. The output stage of this OpAmp is merely unity gain level shift circuit. A compensation capacitor is placed at high impedance node to make the feedback loop inside the reference circuit stable.

7.2.3 1-V Signal-Processing Unit (SPU)

The overall 1-V biosensor system is complete if the signal processing unit (such as the *I-F* converter displayed in Fig. 2.8 or Fig. 2.9) is 1-V compatible. Two solutions are proposed for this problem. The first is to implement a novel low-voltage circuit technique for the *I-F* converter. However, the simpler method is to utilize the short channel transistors with the low V_T, since digital circuits comprise most of this block and they suffer much less from the disadvantages brought by this type of transistors.

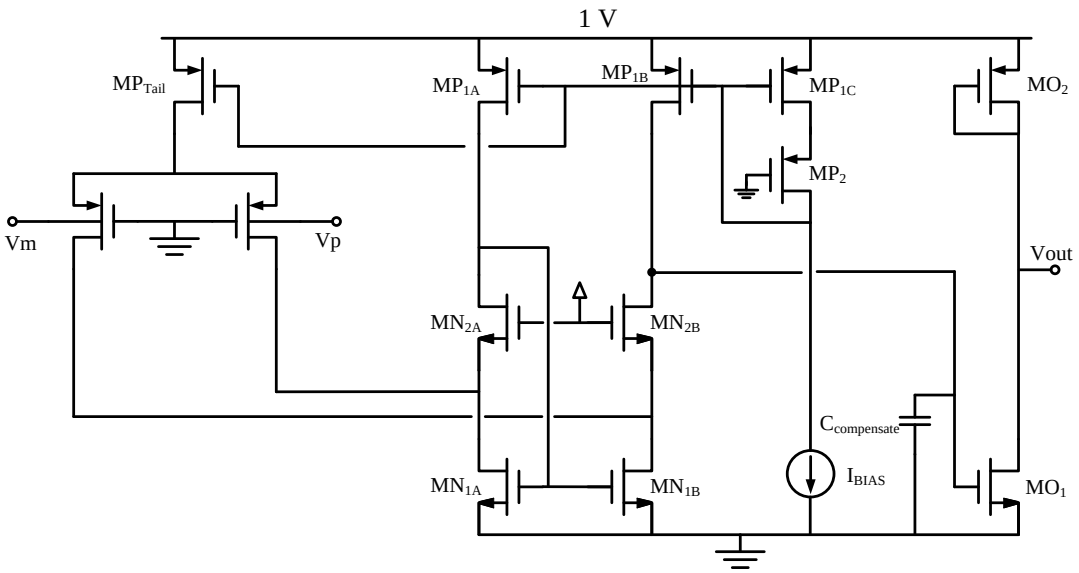

Fig. 7.2 Schematic of the bulk-driven OTA inside the 1-V reference circuit.

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APPENDICES

A.1 Calculations of the 1-V Bulk-Driven Input Stage Biasing Using EKV Model

The biasing circuitry proposed in [61] can be analyzed using EKV model invented by C.C. Enz et al. Since the transistor MC_1 is diode connected, the reverse current $I_{Reverse,MC1}$ controlled by the drain terminal can be neglected according to Eq.(4.1). As a result,

$$\boldsymbol{I}_{\boldsymbol{tot},\boldsymbol{MC}_1} \approx \boldsymbol{I}_{\boldsymbol{Forward},\boldsymbol{MC}_1} \tag{A.1}$$

On the other hand, because the gates of transistors MC_1 and MC_2 are connected, so as the source of MC_1 and the drain of MC_2, the following equations can be deducted,

$$\boldsymbol{I}_{\mathrm{Re}\boldsymbol{verse},\boldsymbol{MC}_2} = \frac{\boldsymbol{I}_{\boldsymbol{Forward},\boldsymbol{MC}_1}}{\frac{\boldsymbol{m}}{2}} \approx \frac{\boldsymbol{I}_{\boldsymbol{tot},\boldsymbol{MC}_1}}{\frac{\boldsymbol{m}}{2}} \tag{A.2}$$

where $m/2$ is the size ratio of transistors MC1 to MC2 (i.e. $W/L_{MC1}/W/L_{MC2} = m/2$). Meanwhile, the overall currents flowing through MC_1 and MC_2 respectively are supplied by the current sources MB_2, MB_3 and MB_4.Their relationship is expressed in Eq.(A.3),

$$\boldsymbol{I}_{\boldsymbol{tot},\boldsymbol{MC}_2} = \left(2\boldsymbol{n}+1\right)\boldsymbol{I}_{\boldsymbol{tot},\boldsymbol{MC}_1} \tag{A.3}$$

By substituting $I_{tot,MC2}$ derived in Eq.(A.2) and Eq. (A.3) into Eq.(A.4),

$$\boldsymbol{I}_{\boldsymbol{tot},\boldsymbol{MC}_2} = \boldsymbol{I}_{\boldsymbol{Forward},\boldsymbol{MC}_2} - \boldsymbol{I}_{\boldsymbol{Reverse},\boldsymbol{MC}_2} \tag{A.4}$$

Eq.(A.5) can be calculated as,

$$(2\boldsymbol{n}+1)\frac{\boldsymbol{m}}{2}\boldsymbol{I}_{\boldsymbol{Reverse},\boldsymbol{MC}_2} = \boldsymbol{I}_{\boldsymbol{Forward},\boldsymbol{MC}_2} - \boldsymbol{I}_{\boldsymbol{Reverse},\boldsymbol{MC}_2} \tag{A.5}$$

After rearranging it, the ratio of $I_{Forward}$ to $I_{Reverse}$ in transistor MC_2 can be expressed by,

$$\frac{I_{Forward,MC_2}}{I_{Reverse,MC_2}} = 1 + \frac{m}{2}(1 + 2n) \tag{A.6}$$

Similarly, the improved version of the bulk-driven input stage in Fig. 4.2 can be analyzed. Eqs.(A.2) and (A.3) are revisited according to the modifications of the size of transistor MC_2 and the overall current flowing through it. The modified equations are expressed as,

$$I_{Reverse,MC_2} = \frac{\frac{I_{Forward,MC_1}}{m}}{2 + 2/j + 2/k} \approx \frac{\frac{I_{tot,MC_1}}{m}}{2 + 2/j + 2/k} \tag{A.7}$$

$$I_{tot,MC_2} = \left(2n + \frac{2n}{k} + \frac{2n}{j} + 1\right) I_{tot,MC_1} \tag{A.8}$$

As a result, the ratio of $I_{Forward}$ to $I_{Reverse}$ in transistor MC_2 can be expressed by,

$$\frac{I_{Forward,MC_2}}{I_{Reverse,MC_2}} = 1 + \frac{m}{2}\left(\frac{1}{1 + 1/j + 1/k} + 2n\right) \tag{A.9}$$

A.2 Calculations of the Enhanced Transconductance $G_{m\_in\_eff}$ in Fig. 4.2

The proposed 1-V bulk-driven input stage in Fig. 4.2 increases the $G_{m\_in\_eff}$ even more by employing a more complex auxiliary differential pairs than the one in Fig. 4.1. The auxiliary differential pairs consist of transistors $ME_{1,2,3}$ in Fig. 4.2. Among them, transistors ME_1 and ME_2 are similar to the bulk-driven differential pair in Fig. 4.1 with the output current being the drain current of transistor ME_2, where the transconductance G_{m_inter} is expressed in Eq.(A.10) as,

$$G_{m\_inter}(s) = \frac{g_{mb,ME1}}{g_{m,ME1}} \bullet g_{m,ME2} \bullet \frac{1}{1 + \frac{s}{g_{m,ME1}/C_B}} + g_{mb,ME2} \tag{A.10}$$

Similarly, one pole associated with the node B in Fig. 4.2 is found. With this G_{m_inter}, the auxiliary gain A_{aux} from inputs to the node A is calculated including transistor ME3 and one pole associated with

node A as shown below,

$$A_{aux}(s)=\left(G_{m\_inter}\frac{1}{g_{m,ME3}}+g_{mb,ME3}\frac{1}{g_{m,ME3}}\right)\frac{1}{1+\dfrac{s}{g_{m,ME3}/C_A}} \tag{A.11}$$

Therefore, the overall $G_{m\_in\_eff}$ is derived in a similar fashion as the calculation of G_{m_inter} and can be expressed as,

$$G_{m\_in\_eff}(s)=A_{aux}g_{m,MI}+g_{mb,MI} \tag{A.12}$$

By substituting G_{m_inter} and A_{aux} in Eqs.(A.11) and (A.12), the detailed expressions of A_{aux} and $G_{m\_in\_eff}$ are shown in Eqs.(A.13) and (A.14):

$$A_{aux}(s)=\left(\frac{g_{mb,ME1}}{g_{m,ME1}}\bullet g_{m,ME2}\bullet\frac{1}{1+\dfrac{s}{g_{m,ME1}/C_B}}+g_{mb,ME2}+g_{mb,ME3}\right)\frac{1}{g_{m,ME3}}\bullet\frac{1}{1+\dfrac{s}{g_{m,ME3}/C_A}} \tag{A.13}$$

$$G_{m\_in\_eff}(s)=\left(\frac{g_{mb,ME1}}{g_{m,ME1}}\bullet g_{m,ME2}\bullet\frac{1}{1+\dfrac{s}{g_{m,ME1}/C_B}}+g_{mb,ME2}+g_{mb,ME3}\right)\frac{g_{m,MI}}{g_{m,ME3}}\bullet\frac{1}{1+\dfrac{s}{g_{m,ME3}/C_A}}+g_{mb,MI} \tag{A.14}$$

Since $g_{mb,ME2}/g_{mb,ME3}$ and $g_{m,ME2}/g_{m,ME3}$ are equal to parameter k and g_{mb}/g_m are constant between transistors $ME_{1,2,3}$ and MI, $G_{m\_in\_eff}$ can be further simplified as,

$$G_{m\_in\_eff}(s)=g_{mb,MI}\frac{2k+1+(k+1)\dfrac{s}{g_{m,ME1}/C_B}}{\left(1+\dfrac{s}{g_{m,ME1}/C_B}\right)\left(1+\dfrac{s}{g_{m,ME3}/C_A}\right)}+g_{mb,MI} \tag{A.15}$$

At DC, the $G_{m\_in\_eff}$ is simply,

$$G_{m\_in\_eff}=(2k+2)g_{mb,MI} \tag{A.16}$$

A.3 Calculations of the Zeros and Poles inside the Bulk-Driven Input Stage

The zeros and the poles can be found inside the proposed bulk-driven input stage (Fig. 4.2) by converting the Eq.(4.12) to fraction and equating the numerator and denominator to zero respectively. As a result, they are expressed in Eqs.(A.17) and (A.18) as,

$$z_{A,B} = -\frac{g_{m,ME3}}{C_A}\frac{k+2}{2} - \frac{g_{m,ME1}}{2C_B} \pm \frac{1}{2}\sqrt{\left(\frac{g_{m,ME3}}{C_A}\right)^2 (k+2)^2 + \left(\frac{g_{m,ME1}}{C_B}\right)^2 - (6k+4)\frac{g_{m,ME1}}{C_B}\cdot\frac{g_{m,ME3}}{C_A}} \quad \text{(A.17)}$$

$$p_A = -\frac{g_{m,ME3}}{C_A} \quad p_B = -\frac{g_{m,ME1}}{C_B} \quad \text{(A.18)}$$

For simplifying the analysis of the zeros and the poles, the gate transconductance of the transistors ME_1 and ME_3 are normalized to that of the core input pair MI, and the capacitances of C_A and C_B are normalized to that of $C_{GS,MI}$. Relating the aforementioned $i = g_{m,MI}/g_{m,ME2}$, $j = g_{m,ME2}/g_{m,ME1}$ $k = g_{m,ME2}/g_{m,ME3}$, and neglecting the drain-to-source capacitance, the $g_{m,ME1}$, $g_{m,ME3}$, C_A and C_B can be derived as,

$$g_{m,ME_1} = \frac{1}{ij} g_{m,MI} \quad \text{(A.19)}$$

$$g_{m,ME_3} = \frac{1}{ik} g_{m,MI} \quad \text{(A.20)}$$

$$C_A = \left(\frac{1}{ik} + 1\right) C_{GS,MI} \quad \text{(A.21)}$$

$$C_B = \left(\frac{1}{i} + \frac{1}{ij}\right) C_{GS,MI} \quad \text{(A.22)}$$

To rather not complicate the circuit design procedure by dealing with these non-dominant poles and zeros, the drain-to-source current of the transistors ME_{1A} and ME_{3A} are sized to be the same which

also indicates that the parameter j is equal to k. Then $z_{A,B}$ and $p_{A,B}$ are derived with respect to $g_{m,MI}/C_{GS,MI}$ as well,

$$z_{A,B} = \left(\frac{k+2}{2(1+ik)} + \frac{1}{2+2k} \pm \frac{1}{2}\sqrt{\left(\frac{k+2}{1+ik}\right)^2 + \frac{1}{(1+k)^2} - (6k+4)\frac{1}{(1+ik)(1+k)}} \right) \frac{g_{m,MI}}{C_{GS,MI}} \quad \text{(A.23)}$$

$$p_A = \frac{1}{1+ik}\frac{g_{m,MI}}{C_{GS,MI}} \quad \text{(A.24)}$$

$$p_B = \frac{1}{1+k}\frac{g_{m,MI}}{C_{GS,MI}} \quad \text{(A.25)}$$

where parameter j is substituted with k.

A.4 Calculations of the Input Referred Noise of the Bulk-Driven Input Stage

The thermal noise and flicker noise of the transistors MI, $ME_{1,2,3}$ and $MB_{3,4,5}$ contribute to the overall output noise inside the proposed bulk-driven input stage in Fig. 4.2. Calculations of the noise current $i_{n,th}$ flowing out of the proposed input stage are performed. The noise contribution of each transistor is shown in the following while ignoring the series gate and bulk resistance noise for simplicity.

For the transistor MI, the thermal noise current and flicker noise current are expressed as,

$$\overline{i_{MIn,th}^2} = 4k_B T\gamma g_{m,MI} \quad \text{(A.26)}$$

$$\overline{i_{MIn,1/f}^2} = \frac{K_f}{C_{ox}^2 W_{MI} L_{MI} f} g_{m,MI}^2 \quad \text{(A.27)}$$

where k_B is the Boltzmann constant, T is the temperature, γ is the gamma noise factor, K_f is the process dependent flicker noise constant.

For the transistor ME_3,

$$\overline{i_{ME3n,th}^2} = 4k_B T\gamma \frac{1}{g_{m,ME3}} g_{m,MI}^2 \tag{A.28}$$

$$\overline{i_{ME3n,1/f}^2} = \frac{K_f}{C_{ox}^2 W_{ME3} L_{ME3} f} g_{m,MI}^2 \tag{A.29}$$

For the transistor ME_2,

$$\overline{i_{ME2n,th}^2} = 4k_B T\gamma \frac{g_{m,ME2}}{g_{m,ME3}^2} g_{m,MI}^2 \tag{A.30}$$

$$\overline{i_{ME2n,1/f}^2} = \frac{K_f}{C_{ox}^2 W_{ME2} L_{ME2} f} \frac{g_{m,ME2}^2}{g_{m,ME3}^2} g_{m,MI}^2 \tag{A.31}$$

For the transistor ME_1,

$$\overline{i_{ME1n,th}^2} = 4k_B T\gamma \frac{1}{g_{m,ME1}} \frac{g_{m,ME2}^2}{g_{m,ME3}^2} g_{m,MI}^2 \tag{A.32}$$

$$\overline{i_{ME1n,1/f}^2} = \frac{K_f}{C_{ox}^2 W_{ME1} L_{ME1} f} \frac{g_{m,ME2}^2}{g_{m,ME3}^2} g_{m,MI}^2 \tag{A.33}$$

For the transistor MB_3,

$$\overline{i_{MB3n,th}^2} = 4k_B T\gamma g_{m,MB3} \frac{1}{g_{m,ME1}^2} \frac{g_{m,ME2}^2}{g_{m,ME3}^2} g_{m,MI}^2 \tag{A.34}$$

$$\overline{i_{MB3n,1/f}^2} = \frac{K_f}{C_{ox}^2 W_{ME1} L_{ME1} f} g_{m,MB3}^2 \frac{1}{g_{m,ME1}^2} \frac{g_{m,ME2}^2}{g_{m,ME3}^2} g_{m,MI}^2 \tag{A.35}$$

For the transistor MB_4,

$$\overline{i_{MB4n,th}^2} = 4k_B T\gamma g_{m,MB4} \frac{1}{g_{m,ME3}^2} g_{m,MI}^2 \tag{A.36}$$

$$\overline{i_{MB4n,1/f}^2} = \frac{K_f}{C_{ox}^2 W_{ME1} L_{ME1} f} g_{m,MB4}^2 \frac{1}{g_{m,ME3}^2} g_{m,MI}^2 \tag{A.37}$$

For the transistor MB_5,

$$\overline{i_{MB5n,th}^2} = 4k_B T \gamma g_{m,MB5} \frac{1}{g_{m,ME3}^2} g_{m,MI}^2 \tag{A.38}$$

$$\overline{i_{MB5n,1/f}^2} = \frac{K_f}{C_{ox}^2 W_{ME1} L_{ME1} f} g_{m,MB5}^2 \frac{1}{g_{m,ME3}^2} g_{m,MI}^2 \tag{A.39}$$

The overall output noise current is the sum of the previous equations. Then the input referred noise voltage of this input stage from both thermal noise and flicker noise are calculated as,

$$\overline{v_{n,th}^2} = \frac{\overline{i_{MIn,th}^2} + \overline{i_{ME3n,th}^2} + \overline{i_{ME2n,th}^2} + \overline{i_{ME1n,th}^2} + \overline{i_{MB3n,th}^2} + \overline{i_{MB4n,th}^2} + \overline{i_{MB5n,th}^2}}{(2k+2)^2 g_{mb,MI}^2} \tag{A.40}$$

$$\overline{v_{n,1/f}^2} = \frac{\overline{i_{MIn,1/f}^2} + \overline{i_{ME3n,1/f}^2} + \overline{i_{ME2n,1/f}^2} + \overline{i_{ME1n,1/f}^2} + \overline{i_{MB3n,1/f}^2} + \overline{i_{MB4n,1/f}^2} + \overline{i_{MB5n,1/f}^2}}{(2k+2)^2 g_{mb,MI}^2} \tag{A.41}$$

The detail expressions are in Eqs.(4.16) and (4.17).

VITA

Liang Zuo was born in Nanjing, Jiangsu, P.R. China in 1985. He received his B.S degree in School of Microelectronics from Shanghai Jiao Tong University in 2008. His research interest is analog and mixed signal IC designs in CMOS process.