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To the Graduate Council:

I am submitting herewith a dissertation written by Shengnan Li entitled "Packaging Design of IGBT Power Module Using Novel Switching Cells." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

Leon M. Tolbert, Major Professor

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Fred Wang, Benjamin J. Blalock, Rao V. Arimilli

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Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

Packaging Design of IGBT Power Module

Using Novel Switching Cells

A Dissertation Presented for the
Doctor of Philosophy Degree
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Abstract

Parasitic inductance in power modules generates voltage spikes and current ringing during switching which cause extra stress in power electronic devices, increase electromagnetic interference (EMI), and degrade the performance of the power converter system. As newer power devices have faster switching speeds and higher power ratings, the effect of the parasitic inductance of the power module is more pronounced. This dissertation proposes a novel packaging method for power electronics modules based on the concepts of novel switching cells: P-cell and N-cell. It can reduce the stray inductance in the current commutation path in a phase-leg module and hence improve the switching behavior.

Taking an insulated gate bipolar transistor (IGBT) as an example, two phase-leg modules, specifically a conventional module and a P-cell and N-cell based module were designed. Using Ansoft Q3D Extractor, electromagnetic simulation was carried out to extract the stray inductance from the two modules. An ABB 1200 V / 75 A IGBT model and a diode model were built for simulation study. Circuit parasitics were extracted and modeled. Switching behavior with different package parasitics was studied based on the Saber simulation.

Two prototype phase-leg modules were fabricated. The parasitics were measured using a precision impedance analyzer. The measurement results agree with the simulation very well. A double pulse tester was built in laboratory. Several approaches were used to reduce the circuit and measuring parasitics. From the switching characteristics of the two modules, it was verified that the larger stray inductance in the layout causes higher voltage overshoot during turn off, which in turn increases the turn off losses.

Multichip (two in parallel) IGBT modules applying novel switching cells was also designed.

The parasitics were extracted and compared to a conventional design. The overall loop inductance was reduced in the proposed module. However, the mismatch of the paralleled branches was larger.

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1 Introduction

Power semiconductor modules play a key role in a power electronic system, such as switching mode power supply, motor drive, UPS, and so on. Generally, a power semiconductor module may be defined as a device which contains more than one semiconductor chip and provides an electric path and a heat flux path [1]. The first power semiconductor module was established in the mid seventies of the past century. For the first time, two chips were combined by being soldered together with electrical contacts on metalized ceramic substrates and by being put in a common plastic housing. Power electronic systems became much more compact, cost efficient and reliable, which necessitated advanced device packaging and integration technology. As decades went by, power device and module packaging technology has evolved through multiple generations, each with incremental improvements in performance and reliability. However, the requirements for lower cost, small size, light weight and more reliable power modules have not ceased.

1.1 Background

At present, the insulated gate bipolar transistor (IGBT) has become the device of choice for a wide range of industrial power conversion applications because of the superior switching characteristics, low losses, and simple gate drive. IGBTs make up 43% of the power module market [1] with 56% of the IGBT applications being motor drives. Figure 1.1 shows a series of IGBT modules from SEMiX in this application area, it offers rectifiers and IGBTs for 15 kW to 150 kW in a package outline with standard 17 mm terminal height. Another application is traction, which is the highest power condition an IGBT can handle.

IGBT modules for traction are shown in Figure 1.2 (Photo of ABB Semiconductors). Intelligent power module (IPM) as shown in Figure 1.3 (Photos of Fairchild Semiconductors, International Rectifier, Mitsubishi Electric) is another popular application area. Moreover, two emerging market segments will be highlighted as well. One is power modules for renewable energy applications, in particular wind power, and the other is automotive applications. Power modules in wind power are basically similar as in traction. However in automotive, thermal behavior is critical because of the vehicle environment, hence the IGBT module packaging is usually of high temperature. As an example, Figure 1.4 shows a commercial automotive module designed by Semikron.

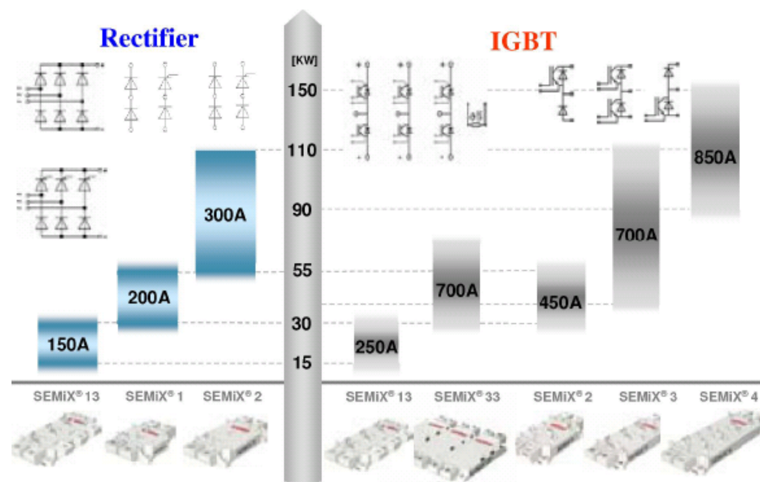


Figure 1.1. SEMiX product family.

Figure 1.2. 1200 A, 3300 V IGBT module.

Figure 1.3. Fully integrated intelligent power module in single-in-line and dual-in-line housing.

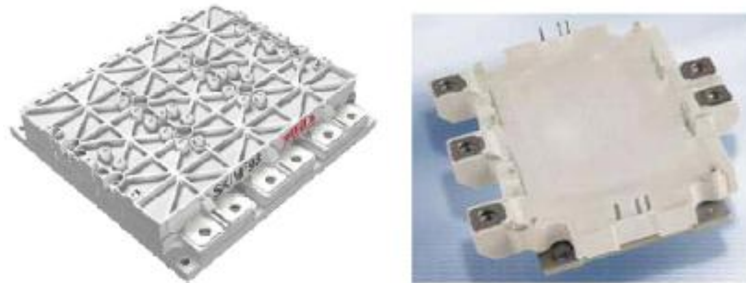


Figure 1.4. SKiM63 (300 A, 1200 V) and HybridPack (400 A, 600 V).

High reliability and long term stability are essential in high power applications. According to [8], a 30-year lifetime, 338,000 long-term cycles, and 12 million short-term temperature changes are required for traction applications. As stated above, IGBTs are being extensively used for relatively high current and high frequency applications. A scenario that is commonly used to explain the IGBT failure is the coefficient of thermal expansion (CTE) mismatch between the silicon and substrate during thermal cycling. Actually, in application, some failures are caused by parasitic effects. One example is the voltage spike during switching, which is a function of total dc loop inductance. It can only be controlled effectively by the gate resistance of the other commutated IGBT at the expense of high turn-on loss. After the IGBT fails, it is commonly found, that one or two bonding wires were opened, or the chip surface at the bonding joints is cracked [19].

Excessive overshoot voltage is harmful to the IGBT safe operation area and even causes IGBT destruction. In addition to the voltage spikes, another problem is current ringing due to

the resonance of the parasitic inductance in the power module and the parasitic capacitance of the devices. It is a source of electromagnetic interference (EMI) and leads to extra power loss. Last but not the least is the current sharing problem in multichip modules because of the discrepancy of the parasitics.

In order to solve the problems mentioned above to the most extent, it is important to reduce module internal inductance [7]. Much research work has been done to study the parasitics in the power module, basically the parasitic inductance is distributed in the terminal leads, bonding wires and substrate.

1.2 Motivation and Strategy

As the demand of power rating and switching speed of the power electronics devices increases, the current slope, *di*/*dt*, is getting larger, the role of the stray inductance inside the module is more and more important. The objective of this work is to design the packaging layout based on the concepts of two novel switching cells to reduce the stray inductance to the most extent.

The dominant technology in power module packaging will still be wire bond technology. Therefore, this technology is used as the packaging method in this dissertation. Power IGBT modules will be the focus of discussion owing to its rising popularity. However, the results of this work are general and can be used in other types of power devices and package technology as well.

First, the IGBT module will be modeled using electromagnetic field simulation software Q3D Extractor from Ansoft, which is a 3-D and 2-D parasitic extraction software tool for designing printed circuit boards (PCB), electronic packaging, and power electronic

equipment. Specifically, Method of Moments (integral equations) and Finite Element Methods were used to compute capacitance, conductance, inductance, and resistance matrices [9]. With this simulation tool, the design process will be much easier and cost effective, since the parasitics can be studied in detail before the module prototype is fabricated.

After the layout design was done and all the parasitics were extracted, circuit simulation was carried out to characterize the circuit behavior. Synopsys Saber is used as the simulation tool in this case. Saber was a multi-domain modeling and simulation environment that enables full-system virtual prototyping for applications in analog/power electronics, electric power generation/conversion/distribution and mechatronics. Saber has been used for design validation and optimization for automotive, aerospace, and industrial systems [10]. In this work, IGBT turn-on and turn-off behaviors were selected as the index for the electrical evaluation, since the packaging parasitics mainly affect the switching behavior. A double pulse tester (DPT) which is the standard circuit for switching characterization was used in the simulation.

After a clear picture of the parasitics in power modules and the circuit behavior under the module parasitics was obtained from the simulations, real power modules were fabricated and tested. The module internal parasitics were measured and an experimental DPT was built and tested to verify the proposed concept and simulation.

The novel switching cells concept was next extended to the multichip power modules. The same approaches were used to study the effects of the module stray inductance.

1.3 Dissertation Outline

According to the strategy discussed above, the outline of the dissertation is listed as follows.

Chapter 2 is the literature survey. The dominant packaging technology nowadays, wire-bonding technology, is discussed in the beginning. Then the techniques of layout design and other considerations in terms of power module electrical behaviors are reviewed.

Chapter 3 presents the layout design of the power module. This layout design originates from the concepts of P-cell and N-cell. A conventional phase-leg module and the proposed phase-leg module are built in Q3D extractor.

Chapter 4 is the DPT Saber simulation under the extracted parasitics. The turn-on and turn-off overshoot voltages and ringing current are compared for two different packages. Also, analytical modeling and analysis for both turn-on and turn-off is done.

Chapter 5 is the module parasitic measurement and experimental results of DPT.

Chapter 6 discusses stray inductance in modules with paralleled devices. Based on the parasitics extraction and the circuit simulation, both the advantages and disadvantages of the proposed design layout is discussed.

Chapter 7 concludes the work that has been done in the dissertation, summarizes the main contributions and the possible future work.

2 Literature Review

Power electronics packaging technology has been developed for several generations, involving material upgrading, structure improvement, and interconnection technique innovation. For instance, in high power situations, a press pack is used to reduce bonding wires and solder attachment. Also, planar technology has gained much interest in certain applications (such as hybrid electric vehicles) since double sided cooling is enabled. In most commercial modules, nevertheless, wire bonding is still the main choice of packaging due to its maturity and reliability.

2.1 Wire Bonding Technology

In general, a power module construction is composed of different layers, as shown in Figure 2.1 [11]. The base layer is the baseplate, which is a thick layer of metal used for mechanical fixation and heat transfer. Direct bonded copper (DBC), which consists of two copper layers and one ceramic layer, is soldered on the baseplate. Power semiconductor dice and terminals are then soldered on the top layer of the DBC. Moreover, aluminum wires are used for interconnection of dice and terminals. The module is put in a plastic case. Finally, encapsulant such as silicone gel is filled in the case for protection and insulation. In fact, power module fabrication involves many different processes and techniques, and several key factors of them will be discussed in detail in this chapter.

2.1.1 Material Selection

The materials involved in a power module design cover a wide range from insulators, conductors, and semiconductors to organics. Since these materials behave differently under

various environmental, electrical, and thermal conditions, proper selection of these materials and the assembly processes are critical.

A. Substrate selection

Substrate as shown in Figure 2.1 is one of the most important parts in a power module. Typically, there are three layers for the substrate, i.e., two conduction layers and an insulation layer in between. Specially, the top metal layer is the printed circuit of the power module. The insulation layer serves as the supporting structure for the circuitry [12]. This layer is mechanically a base to support all active and passive chip components, and electrically an insulator to isolate various conductive paths of the circuit. The bottom metal layer is for thermal expansion balancing.

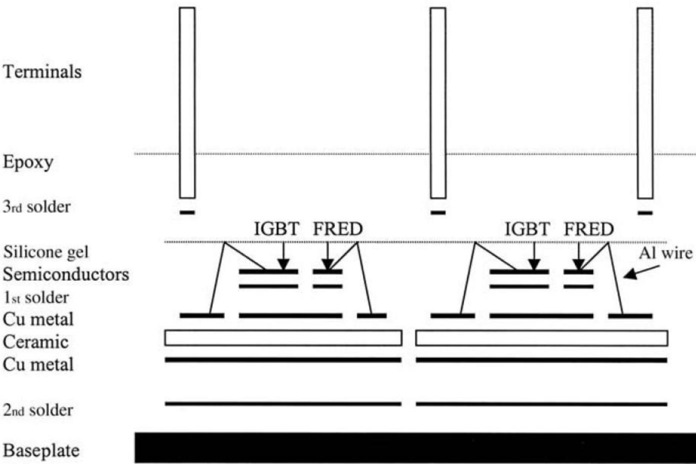


Figure 2.1. Structure of an IGBT power module.

Two commonly used materials for the substrate are Aluminum Nitride (AlN) and Alumina (Al_2O_3). The properties of concern are listed in Table 2.1.

Table 2.1. Properties of Insulating Substrate

Material		Al_2O_3 (96%)	Al_2O_3 (99%)	AlN
Electrical	Resistivity (W-cm)	$> 10^{14}$	$> 10^{14}$	$> 10^{14}$
	Dielectric Strength (kV/mm)	12	12	15
	Dielectric Constant at 1 MHz	9.2	9.9	8.9
Thermal	Thermal conductivity (W/m ˚K)	24	33	150-180
	CTE (ppm/˚C)	6.0	7.2	4.6
	Heat Capacity (J/kg-˚C)	765	765	745
	Maximum Use Temperature (˚C)	1600	1600	>1000
	Melting Point (˚C)	2323	2323	2677
Mechanical	Tensile Strength (MPa)	127.4	206.9	310
	Flexural Strength (MPa)	317	345	360
	Density (kg/m^3)	3970	3970	3260
	Elastic Modulus (GPa)	310.3	345	310
	Hardness	2000K	9MH	1200K
	Surface Finish (μm)	1.0	1.0	1.0
Others	Metalizability	All, except thin film	All	All, except thick film
	Machine ability	Good	Good	Good
	Relative cost	1	2	4

The top and bottom metallization also have some requirements for power electronics application. Some of the key requirements are listed below [11]:

– High thermal conductivity (> 200 W/k-m).

–High current density.

– Strong adhesion to the substrate.

– Photoetchable.

According to the requirements above, DBC becomes the most popular choice for the

substrate. DBC technology uses a high-temperature process to achieve an intimate bond between the copper and the ceramic. There is no solder or any other catalyst used in the interface between the copper and the ceramic surface. Here, the combination of copper and ceramic is heated to a temperature of about 1070°C which is slightly below copper's melting point, in a nitrogen atmosphere. At this temperature, the copper oxide forms a eutectic melt that wets and, when cool, produces a strong bond between copper and ceramic. Copper thickness is typically 8 to 20 mils.

B. Bonding material

Besides substrate, bonding materials also play a key role in a power module. It provides the vital functions of mechanical, thermal, and electrical linkages between the power semiconductor chips, the terminals, the insulating substrates, and the metal base plate. Therefore, bonding must be properly designed to ensure that the power IGBT module is a mechanically reliable and thermally efficient system.

Solder becomes the bonding choice after comparing with other materials such as epoxy and silver filled glass. Solders are essentially alloys of two or more metals. When these metals are alloyed together, the melting point of the alloy can be considerably less than the melting point of either of the individual starting metals (a phenomenon which makes the soldering process possible). In the soldering process, the solder is placed between two metal surfaces to be soldered. During melting, the molten solder dissolves a portion of these two surfaces and, when the solder cools, a junction or solder joint is formed, joining the two metal surfaces.

Selection of the solder alloys is based on the following criteria [13]:

• Melting temperature range in relation to service temperatures. Due to the CTE mismatch between the power chip, the insulating substrate, and the metal base plate, the processing temperature of the solder should be as low as possible and is preferred to be at or below 350°C. This processing or soldering temperature is typically 20 ºC to 40ºC above the solder melting temperature. Usually, Tj of the IGBT chip can be as high as 150ºC. Thus, the solder melting temperature must be at least 10ºC higher to prevent any remelting.

– Processing restrictions. Usually, the power chips are first attached to the insulating substrate using a high temperature solder. The insulating substrate is then attached to the metal baseplate with a lower-temperature solder to avoid remelting of the first solder. This is done so that the two solder attachments can be optimized independently. These two soldering temperatures should be at least 40ºC apart. According to this, the melting temperature ranges for the two solders should be as follows: first solder - 200˚C to 310˚C, and second solder - 160˚C to 270˚C.

• Availability. The solder should be available in both preform and paste form.

• Compatibility with the metallization of the power chips, the insulating substrate, and the metal baseplate.

Also, the criteria include high mechanical strength, low elasticity, high-creep, high-fatigue resistance and so on.

The most commonly used alloy systems in semiconductor assembly are:

• Gold/Tin hard solder

• Tin/lead soft solder

C. Power interconnection material

The interconnection part in a power module is bonding wires that are used between the top aluminum metallization of the IGBT/Free-wheel diode (FWD) surface and the electroplated substrate, and terminal leads, which are used to connect to outside circuit.

Aluminum wire is preferred for wire bonding because of its low electrical resistivity, reliable attachment to the chip metallization surface and substrate, and also its affordable price. The standards for aluminum wire selection is listed in Table 2.2.

Table 2.2. Maximum Current for Aluminum Wire Size

Material	Diameter (Inch)	Maximum Current (A)	
		L < 0.040"	L > 0.040"
Aluminum (Al/1%Mg)	0.001	0.7	0.5
	0.002	2.0	1.4
	0.005	7.8	5.4
	0.008	15.7	10.9
	0.012	28.9	20.0
	0.015	40.4	28.0
	0.022	71.8	49.6

In terms of terminal connections, the requirements for this material are high conductivity, high mechanical strength, and elasticity for molding and so on. Copper based alloys such as beryllium/copper (BeCu, C170, C172) and phosphor/bronze, are commonly used because of the property of low resistivity, high tensile strength, ease of fabrication and reshape, high fatigue endurance and wear resistance. The terminals are formed by soldering to the substrate or by integrating into the case, and connect to the chip or substrate using aluminum wires.

2.1.2 Fabrication Process

The procedures of the fabrication process include cleaning the devices, soldering, wire bonding and encapsulating. This session reviews the major techniques: soldering and wire bonding.

Devices and terminals soldering

As mentioned briefly earlier, the common method for component attachment in IGBT module assembly is a two-solder process. First, power chips will be soldered to the substrate using the first solder. After the chips are put at the correct position on the substrate with the solder preform, the assembly is moved automatically onto the conveyer belt of the reflow oven for soldering. Ceramic substrate, power terminal and connecting bridge attachments are usually done manually by using a graphite fixture or a graphite fixture with alignment sheets. A graphite fixture is in the shape of a block with detachable parts for the placement of base plate, ceramic substrate terminals, and bridges. Solder can be either screen-printed or dispensed onto the baseplate and ceramic substrate. For graphite fixture with alignment sheets, it is a flat graphite plate about 10 mm thick with guided pins that are in line with the mounting holes of the baseplate and the sheets. The sheets or frames are metallic, usually stainless steel of 1 to 4 mm thick, and have windows etched out for the placement of different components. The guided pins are designed with stops to control the height of these sheets above the base plate.

The second solder is for attaching the terminals/connecting bridges to the ceramic substrate and the ceramic substrate to the metal base plate. Generally, the first solder has a melting temperature of about 25˚C to 40˚C higher than the second solder [11].

Ultrasonic wire bonding

After the solder attachment is finished, the interconnection inside the module will be done using wire bonding. A bonding machine and aluminum wires are involved in this process. During bonding, the wedge presses the wire against the metal termination pad, and ultrasonic energy (usually 20 to 60 kHz) is applied to the wedge. The wire is rubbed against the contact, causing local heating and a metallurgical weld. The thin oxide coating on the aluminum wire is ruptured, and the oxide tends to help the friction heating process, giving a very reliable bond.

2.2 Study on Parasitics Induced by Packaging

Parasitic inductance exists from the IGBT chip collector and emitter to their terminal connections, no matter what kind of packaging technique is used. The parasitic inductance stores energy whenever the current flows through the interconnections inside the module when the IGBT is on. When it turns off, the energy is released directly as a voltage spike if there is no external snubber capacitor in the current loop. This spike is a function of inductance and di/dt rate. Even with careful layout of the power stage, a snubber capacitor is usually needed to absorb this energy. If the snubber loop equivalent series resistance (ESR) is small, a high oscillatory current is produced. If the ESR is large, the current waveform is improved, at the expense of circuit loss and heating. Although the IGBT is designed to remove the conventional heavy-duty snubbers such as resistor-capacitor-diode, it cannot survive without some form of snubber circuit in most applications. How to deal with the parasitics effect will ultimately affect the EMI, efficiency, and performance of the converter [19]. In the design and layout of IGBT packages and power stages with both high switching speed and high power handling requirements, reducing parasitics is extremely important.

The package stray inductance can be classified into three categories, as follows [6]:

1. Inductance due to DBC substrate pattern;

2. Inductance due to bonding wires;

3. Inductance of electrode.

The substrate inductance is the smallest among the three. The inductance in the bonding wires depends on the length. Usually, the length of wire is minimized and hence the induced inductance is not a big concern. The terminal conductors have a relatively large dimension, thus the largest inductance exists in this part. Table 2.3 lists the parasitics in a 300 A 1200 V commercial power module [19], which provides a rough idea of the scale and how the parasitics are distributed in a power module.

Table 2.3. Summary of Parasitic Inductance in Power Modules

	Bonding wire	Emitter conductor trace	Collector conductor trace	Terminal conductors
Parasitic inductance	10-15 nH	5-7 nH	4-5 nH	30-40 nH

Although the stray inductance induced by the bonding wires is not the biggest concern in the module parasitics, there is a special issue with the paralleling of the wires. Table 2.2 shows the current capabilities of the different aluminum wires. 12 mil and 15 mil diameter wires are most commonly used for IGBT modules. Very often, the length of the wire connection is longer than 40 mils. Therefore the current capability of a single wire is 20 A for 12 mil wire and 28 A for 15 mil wire. A single IGBT die can have current capability up to 300 A. Considering no overload margin, twenty 15 mil thick wires are needed to parallel for a 300 A IGBT. The paralleling of the bonding wires can cause the following problems [19]:

1. Proximity Effects between Bonding Wires

In the transients where the current rises and falls quickly, the equivalent high frequency contents are concentrated. At this moment, the mutual coupling effect between the paralleled wires become so significant that the wires in the edge appear as a low impedance path compared to the middle wires. Those wires carry more current than the others. Meanwhile, because of the non-uniform bonding wires on the chip, the steady state current distribution is affected. This can possibly load the IGBT cells inside the silicon differently. The current distribution in different wires during transient is illustrated in [19]. The turn on current overshoot in the wire in the edge can be as large as three times of that in the middle wire.

2. Mechanical Stress on Bonding Wires

It is known that a magnetic force will be generated on a conductor carrying current when it is exposed to a magnetic field. The force generated on a particular wire can be regarded as:

$$f_i = \mathrm{B} i_i L_i$$

where, i_i and L_i, are the current and the length of the i-th wire, and B is the magnetic flux density at that position The magnetic flux density is the sum of the flux density generated by all the other bonding wires, if we assume that the wires are perfectly in parallel, and its length is much longer compared to their distance. The flux density contributed by wire *k* to *i* can be written as:

$$B_{i,k}=i_k\mu_0/(2\pi\delta_{i,k})$$

where $\delta_{i,k}$ is the distance between the two wises, i_k is the current magnitude in wire *k*. With this simplified model, the magnetic force generated on the bonding wires can be simulated. The amplitude of the stress applied to the bonding wires may not be a significant number. But under temperature change and power cycling, with this repetitive switching frequency

lateral force, there is a bonding fatigue mechanism as the wires try to peel the metallization off the chip surface, which can increase the on-voltage drop of the device. This explains why the wire-bond modules are more fragile under large repetitive transient current.

High reliability and long term stability are essential in high power applications. Therefore, reducing package stray inductance is an important issue. There are several considerations and improvements in the structure of the package to reduce the parasitics of the module. They are discussed as follows:

1. Terminal arrangement

As stated previously, in a power module the dominant stray inductance is the terminal. Several methods were proposed to reduce this stray inductance. For example, a laminated structure has smaller self inductance. Also, when paralleling the positive and negative terminals, it enables the coupling of the two inductors to the most extent. Theoretically, the equivalent loop inductance equals the two self-inductances minus the mutual inductance. A larger mutual inductance will give smaller total equivalent loop inductance. Therefore, when designing the terminals, the best way is to put two parallel laminated bus bars as close as possible.

2. Bond wires consideration

First, the interconnection of bond wires should be as short as possible. Second, the direction of substrate current, which flows under the emitter bonding wires, is designed to be opposite to the direction of current flow in bonding wires. This wiring construction on the substrate is also achievable by employing multi-layered DBC technology. Consequently, the

bonding wires effect on the module internal inductance can become practically negligible.

3. Utilizing the substrate area

Although the substrate has the smallest inductance, large substrate area can still make the inductance considerably large. It is especially true for high power modules because the paralleling of the power devices enlarges the substrate area. To accommodate the bonding wire connection, the substrate area has to be larger than the footprint of the semiconductor dice. When doing the substrate layout, maximum utilization of the full substrate area should be done.

4. The "U-package" technology [6]

Mitsubishi made a major improvement on the bus bar structure in the sense of reduced stray inductance in 1996. Specifically, the bus bars are molded into the sides of the case, aluminum wires are used to connect the substrate or die to the terminal. Paralleling the main electrodes and narrowing the space are easily made. The distance between both electrodes can be reduced to benefit from the eddy current effect. This also relieves "S" bends that are needed in the electrodes of conventional modules. Elimination of these "S" bends helped to further reduce the electrode inductance. Overall, as a result of these inductance reducing features, the new package has about one third the inductance of conventional modules. Table 2.4 shows the package inductance comparison between conventional and the new concept of U series.

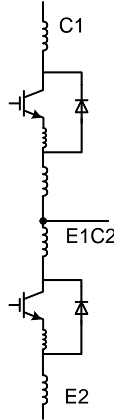


Figure 2.2 Package inductance

Table 2.4. Comparison of Parasitics in Conventional and U-series Power Module

Inductance between terminals	Conventional	U series
C1-E1C2	51	17
E1C2-E2	34	24
C1-E2	58	16

For ease of reference, some general rules to reduce the parasitic inductance are summarized in Table 2.5 [6].

Table 2.5. Summary of Methods to Reduce Inductance

Classification	Inductance reduction methods
DBC substrate pattern	1. Widen the pattern width 2. Shorten the pattern length
Bonding wires	1. Shorten the wire length 2. Increase the number of Al-wires 3. Increase the diameter of the wires
Inductance of electrode	1. Shorten the length 2. Increase the width 3. Parallel the main electrodes and reduce the space between the main electrodes 4. Use eddy current effect

People are making every effort to reduce the stray inductance inside the module. However, one important issue has been neglected, i.e., the effective stray inductance while the module is operating. Actually, the stray inductance is everywhere in a module, the focus is that in the conduction path during switching on and switching off. The following chapter will introduce concepts of two basic switching cells in power converters, reveal the mechanism of how the switching cell works as a functional unit, and show how it can affect power module packaging.

3 Layout Design of IGBT Phase-leg Module

As the basic elements, switching devices (mainly MOSFET and IGBT) and diodes along with inductors and capacitors are used in power electronic circuits to perform dc-dc, dc-ac, and ac-ac power conversion. In a piece-wise fashion, many circuits have been invented, proposed, and demonstrated to perform these power conversion uses [20]. The classical dc-dc converters like buck, boost, buck-boost and Ćuk converters are used in various applications, and the modeling of these various structures is very important to design the control circuits for these converters [20]-[28]. However, these circuits have rarely been examined and investigated in terms of their relationships, topological characteristics and their basic building blocks. After examining the basic building blocks of these dc-dc converters and dc-ac inverters, two basic switching cells are proposed [29].

These basic switching cells function as the fundamental elements in power electronic circuits, which cannot be further broken down or apart and should be used as the basis for manufacturing/layout of single, dual, and 6-pack modules that semiconductor manufacturers are producing. Actually, existing well-known circuits can easily be represented and configured from the basic switching cells. Moreover, some new conversion topologies can be derived by rearrangement of basic switching cells.

3.1 Introduction of P-cell and N-cell

3.1.1 Definition of P-cell and N-cell

The introduction of the switching cell concept started with the canonical cell [31][32], where an inductor, a capacitor, and a single-pole double throw switch form a basic canonical

switching cell as shown in Figure 3.1. This cell has three terminals A, B and C, and each of them can be used as an input/output/common terminal. For instance, if terminal A is used as an input, B as an output and C as the common terminal, the canonical circuit forms one type of dc-dc converter. Six different combinations can be formed by changing the function of the three terminals for different combinations [20]. Among these six combinations, only three distinct effective circuits are found whereas the others are functionally the same. Thus, using these three combinations, the buck, boost and buck-boost converters can be formed.

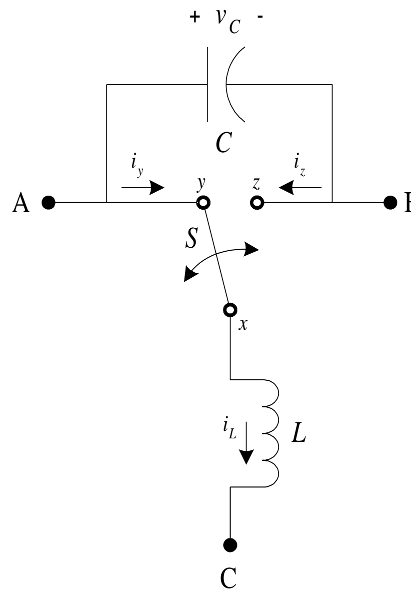


Figure 3.1. Basic canonical cell.

Besides the canonical switching cell, there are many reported methods of modeling power electronic converters out of some switching modules or blocks. According to [32], the classical converters can be grouped into two major converter families - buck converter and boost converter. The buck family converters' small signal models can be expressed in terms of h-parameters, while those for the boost families are expressed by g-parameters. When a unity feedback is applied in the buck converter, the buck-boost converter is obtained.

Using the technique presented in [33], the classical PWM converters can be represented by only the buck and boost converter connected in cascaded arrangement. This method is reported as the graft scheme, which presents a unified and systematic method to synthesize and model transformer-less PWM dc-dc converters. To do that, 4 different basic unit cells were presented where the cells are made from two transistors. Then using the graft scheme, the diode-transistor realization of those 4 cells was derived.

Figure 3.2 shows the two basic switching cells defined in this paper. Each cell consists of one switching device (a MOSFET or IGBT) and one diode connected to three terminals: (+), (-), and (→) /or (←). Each cell has a common terminal which is shown as (→) /or (←) on the schematic. For the P-cell, this common terminal is connected to the positive terminal of a current source or an inductor. For the N-cell, this common terminal is connected to the negative of a current-source or an inductor. The active switching device in a P-cell is connected between the (+) and common terminal, whereas in an N-cell, the switching device is connected between the (-) terminal and the common terminal. Thus, the P-cell is essentially the mirror circuit of the N-cell and vice versa [29][30].

The aforementioned basic switching cells are the practical implementation of the canonical switching cell found in [20]. Although the switching cells have only two components, they can be connected in different combinations to create various power electronic circuits.

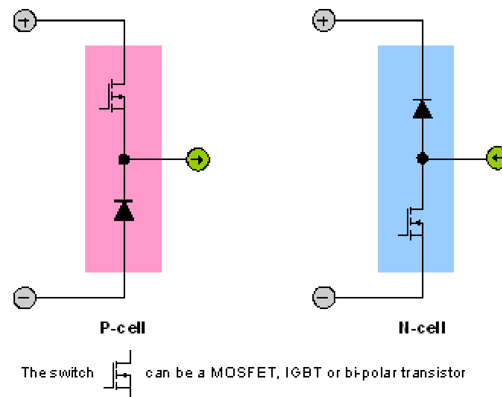


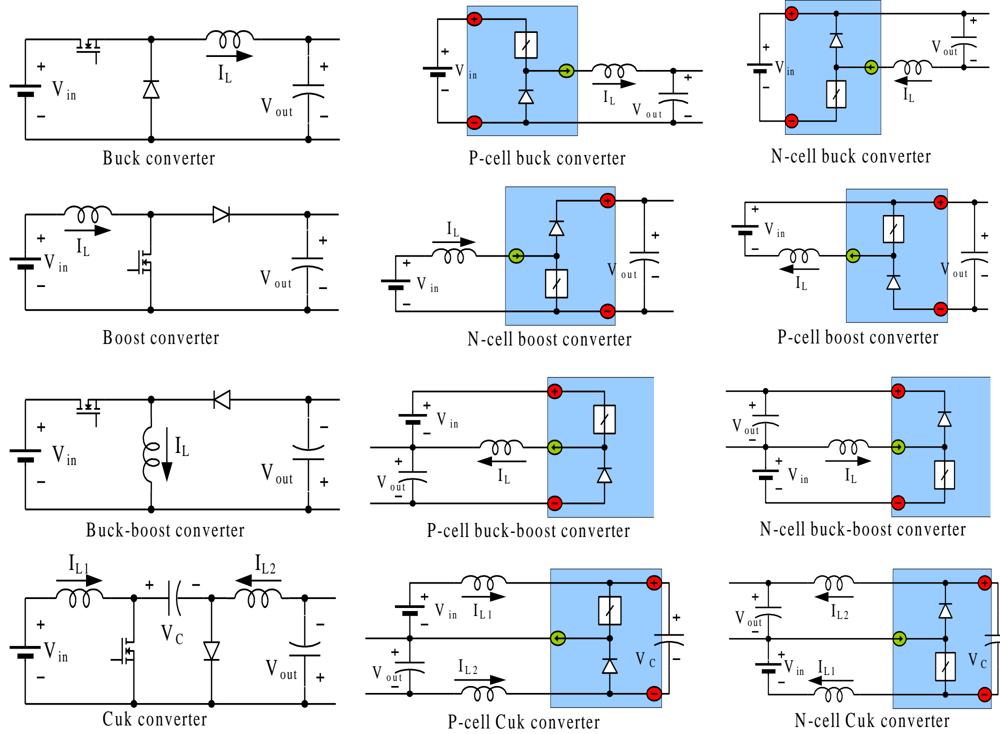
Figure 3.2. Two basic switching cells: P-cell and N-cell.

3.1.2 DC-DC Converters Constructed from P-cell and N-cell

Figure 3.3 summarizes the four classical converters and their cell structures. In Figure 3.3, there are three columns and each column has 4 figures. The figures in the left most column show the four major classical converters. These converters are made from inductors, capacitors, diodes and controlled switches. Each of these conventional converters can be expressed using the basic switching cells and the corresponding circuits are summarized in the middle column. The converters in this column are made from either N-cell or P-cell. Thus it is seen that except the boost converter, all of the conventional converters have an inherent P-cell structure where the active switching element is connected to the positive power supply terminal. The conventional boost converter is inherently an N-cell boost converter.

Theoretically, all of these classical converters also have a mirror circuit representation. When the P-cell in a buck converter is replaced with an N-cell, the circuit takes a different configuration. In this way, the classical boost converter can be re-constructed using a P-cell, rather than an N-cell. The buck and boost converters can be easily decomposed into a P-cell and N-cell based circuit, respectively. However, this procedure is not so obvious for the buck-boost and Ćuk (boost-buck) converters; they inherently take the P-cell structure. The

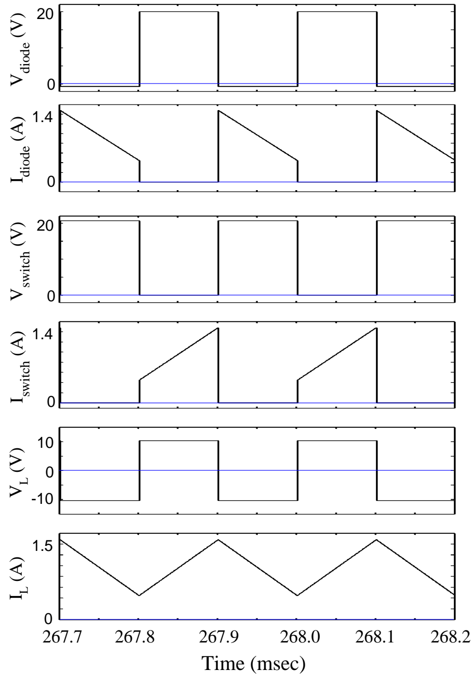
mirror circuit representation of each dc-dc converter is shown in the rightmost column of Figure 3.3.



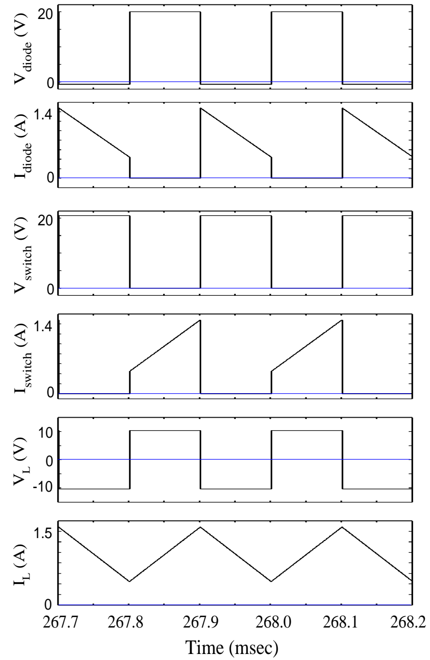
(a) Classical dc-dc converters, (b) Formation by the basic cells, (c) Mirror circuits.

Figure 3.3. Four classic DC-DC converters and their P-cell and N-cell representation

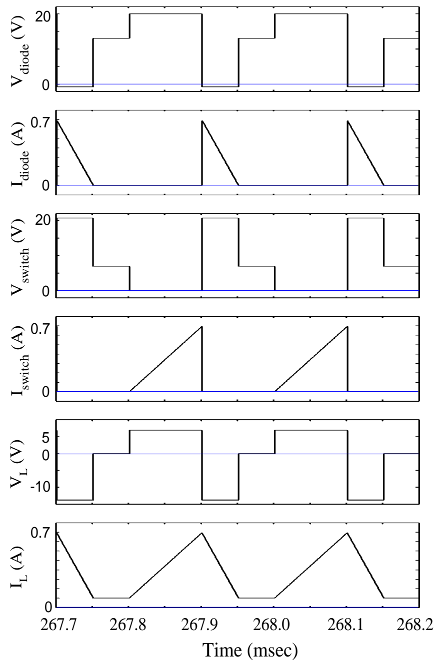
To validate the concept of the P-cell and N-cell mirror relationship, a buck converter was simulated and tested under continuous and discontinuous conduction mode. The simulations were done in PSIM, and the results are shown in Figure 3.4. Actually, there was no difference found in the simulation results, implying that there is a mirror relationship between the N-cell and P-cell structures. Then for further verification, a pair of buck converters (one P-cell and one N-cell) were constructed from discrete components and tested in the lab in continuous conduction mode. The operating and loading conditions of the N-cell buck converter and the P-cell circuit were the same, but some minor differences were observed in their output voltage. The test results are shown in Figure 3.5.



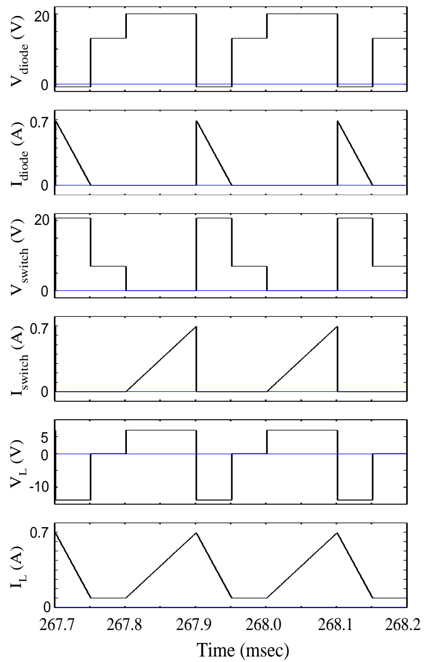
(a) N-cell buck converter at continuous conduction mode (CCM)



(b) P-cell buck converter at CCM



(c) N-cell buck converter at discontinuous conduction mode (DCM)



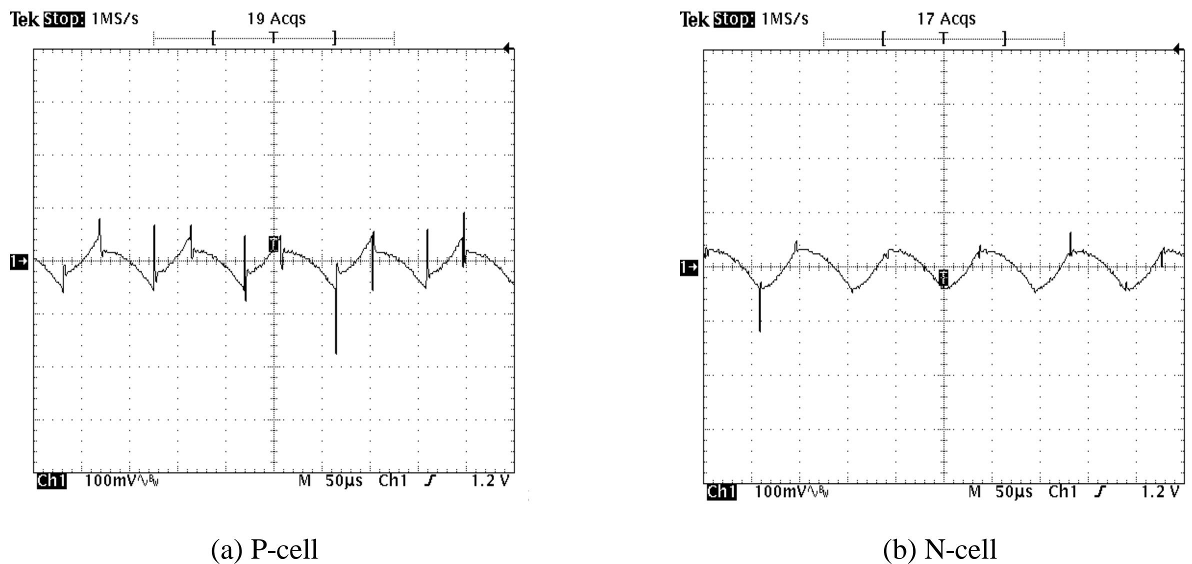
(d) P-cell buck converter at DCM

Figure 3.4. Simulation results for P-cell and N-cell buck converter.

The parameters of the test setup are as follows: V_{in} = 20 V, D = 0.4, f_S = 10 kHz, C_1 =

100 μF, L_1 = 1 mH, D_1 = MURB1020CT-1, S_1 = IRG4BC30U and R_L = 20 Ω.

For an input voltage of 20 V and duty cycle of 0.4, the dc output voltage for the N-cell structure was 6.82 V and for the P-cell buck converter, it was 7.07 V. Figure 3.5 (a) and (b) show the output ripple components of the P-cell and N-cell structures respectively. The fundamental frequency component present in the ripple was the same for both topologies. However, the N-cell structure produces a cleaner output because of the ground-referenced gate drive circuit.



(a) P-cell (b) N-cell

Figure 3.5. Experimental output voltage ripple (100mV/div) of buck converter.

The conventional Ćuk converter has an especially unique structure [23]. A Ćuk converter has continuous input and output current, and the energy is transferred from the input to the output side by means of a capacitor. The classical Ćuk converter has an inherent P-cell structure, and the N-cell Ćuk converter can also be achieved. A Ćuk converter is shown in Figure 3.3 (a), and the switching cell realization is shown in Figure 3.3 (b). The main limitation of the Ćuk converter is that it uses one additional inductor and capacitor. However, simplification can be done using the basic switching cells and a new version of

Ćuk converter can be obtained. In Figure 3.3 (a), during the time when S_1 is on, the rate of change of currents in L_1 and L_2 is the following [34]:

$$dI_{L1}/dt = V_{in}/L_1 \quad (1)$$

$$dI_{L2}/dt = [-V_{out} - (-V_C)]/L_2 = (V_C - V_{out})/L_2 \quad (2)$$

where $V_{out} = (t_{on} / t_{off})V_{in}$ (3)

and

$$V_C = (T / t_{off})V_{in} \quad (4)$$

Inserting (4) into (2), we get

$$dI_{L2} / dt = (1 / L_2)[(TV_{in} - t_{on}V_{in}) / t_{off}] = V_{in} / L_2 \quad (5)$$

Using the same procedure, the rate of change of currents in L_1 and L_2 can be found while S_1 is off. Specifically, when S_1 is off,

$$dI_{L1} / dt = -(1 / L_1)(t_{on} / t_{off})V_{in} \quad (6)$$

$$dI_{L2} / dt = -(1 / L_2)(t_{on} / t_{off})V_{in} \quad (7)$$

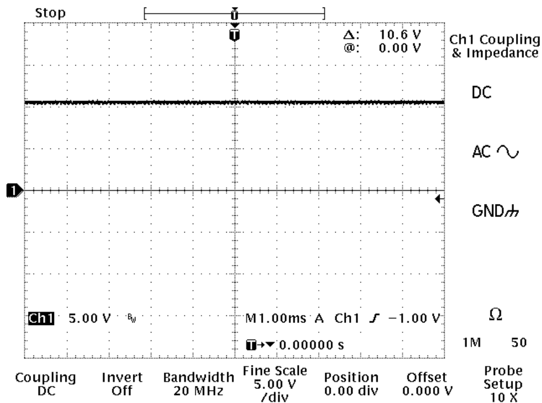
Thus, from (1) and (5) - (7), it is concluded that if $L_1 = L_2$, the rate of change of currents in L_1 and L_2 are the same. Moreover,

$$I_{L1(avg)} / I_{L2(avg)} = I_{in} / I_{out} = D / (1 - D) \quad (8)$$

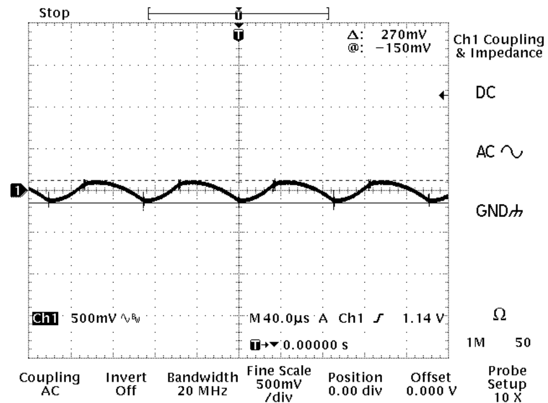
From (8), it is found that, for a specific case when the duty ratio D is 0.5, both inductors will have the same average value of current. If $L_1 = L_2$, they will have the same current slope. Hence, the two inductors can be equivalently moved to the center rail and consolidated into one inductor. If the converter is not operating at $D = 0.5$ or if $L_1 \neq L_2$, there will be a current

mismatch between L_1 and L_2, and the new Ćuk converter configuration will perform slightly differently from the original Ćuk converter. Figure 3.6 shows the output voltages of these converters for a 20 Ω resistive load with a supply voltage of 20 V. The duty cycle of the gate drive was kept at approximately 0.33, and for this duty cycle, the output voltage of a Ćuk converter should be around 10 V. In Figure 3.6 (d) - (f), the output ac ripple is shown by zooming the dc output voltage.

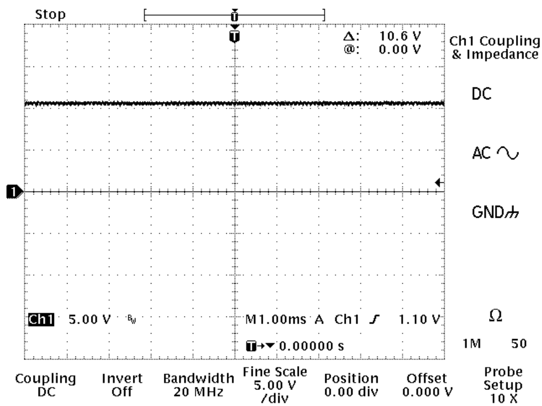
Figure 3.6 shows that these three converters are fairly equivalent. For the same duty cycle, the P-cell and the N-cell structures produce a 10.6 V dc output, while the new combined inductor topology produces 10.1 V dc output. These are shown in Figure 3.6 (a), (b) and (c) respectively. The ripple component in the N-cell circuit has the lowest amplitude of 220 mVp-p, compared to the P-cell structure producing 270 mVp-p. However, the new topology with the two combined inductors produces a ripple of 340 mVp-p, which is slightly higher than the other two topologies. Figure 3.6 (d)-(f) show the ripple components in the three configurations.



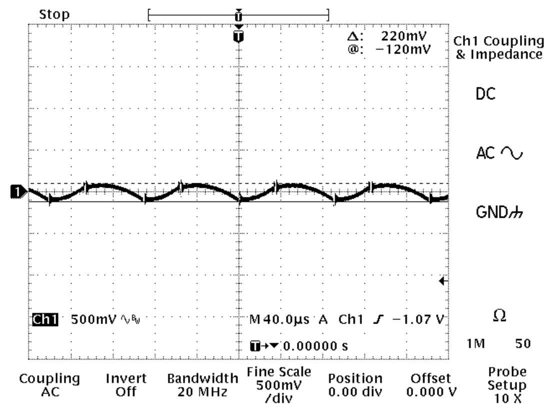
(a) P-cell Ćuk converter dc output voltage



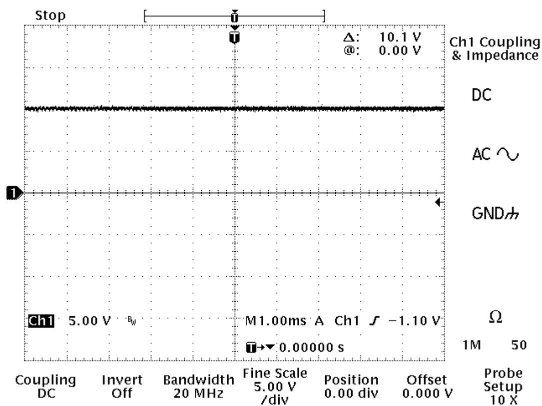
(d) Output ripple of P-cell Ćuk converter



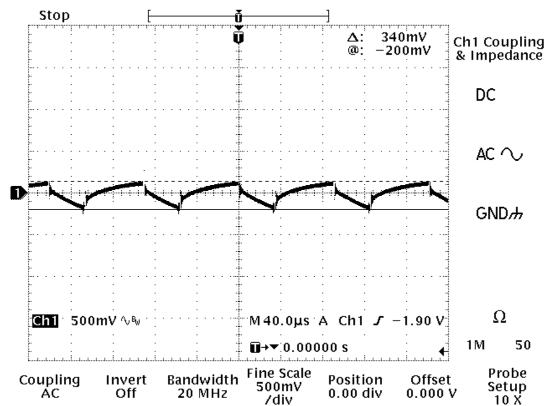
(b) N-cell Ćuk converter dc output voltage



(e) Output ripple of N-cell Ćuk converter



(c) New Ćuk converter dc output voltage



(f) Output ripple of new Ćuk converter

Figure 3.6. Experimental output voltage of Ćuk converters.

3.1.3 Constructing Voltage Source Inverters from the P-cell and N-cell

Like the dc-dc converters, inverters can be constructed by the use of basic cells in a similar way. Figure 3.7 (a) shows that the parallel combination of the P- and N- cells creates

a phase-leg providing bi-directional current flow. Figure 3.7 (b) shows the conventional anti-parallel diode/transistor configuration to create a bi-directional current flow. The parallel connection of a P-cell and an N-cell shown in Figure 3.7 (a) has some distinct advantages over the conventional IGBT with an anti-parallel diode.

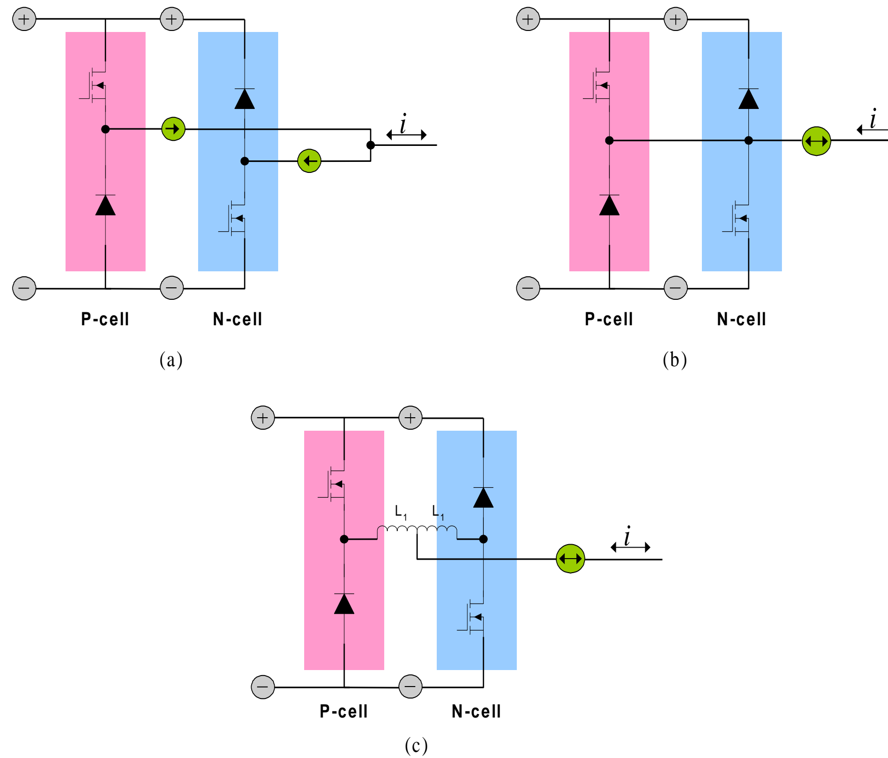


Figure 3.7. Topologies of phase-legs: (a) An inverter phase-leg with bidirectional current flow by paralleling the P- and N-cells, (b) Conventional connection of anti-parallel diode, (c) Placing two inductors between P-cell and N-cell common terminals to control the current.

To create a bi-directional current port in a VSI, two transistors in a phase-leg are switched periodically. However, there is a requirement of dead time between the switching periods of the two transistors that prevents a short circuit of the dc link. When an inductor is placed in the paralleled P-cell and N-cell configuration, it takes the shape of Figure 3.7 (c). In this case, a dead time is not required because the additional inductor and the stray inductance of the interconnections limit the current if there is any overlap in the switching of the P-cell and N-cell devices. Therefore, IGBT-diode modules configured as the P- and N-cell are

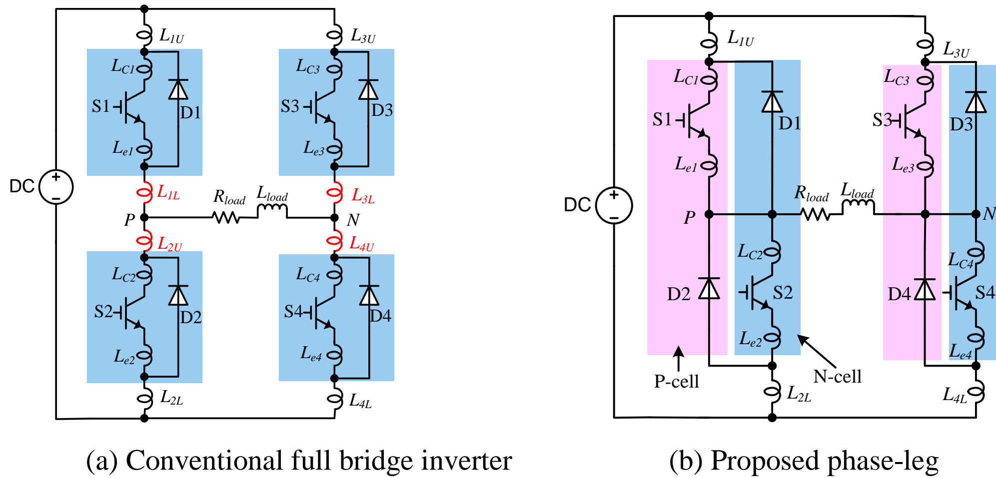
better suited for inverter operation, and at any instant of time, the load current only goes through the P-cell during the positive half cycle and through the N-cell during the negative half cycle of the current. Moreover, for a modulation scheme that can detect the direction of current to the load, only the switch that provides the current path needs to be switched while the other can be kept off. In the VSI circuit shown in Figure 3.7 (b), when the current is going to the load, the transistor in the P-cell is switched on and the transistor in the N-cell is kept off. In the same way, when the current is coming back from the load, it flows through the transistor in the N-cell which is switched on, and the transistor in the P-cell is kept off.

The basic switching cell concept creates a new vision to analyze the conventional power electronic converters by segregating them into smaller modular blocks. This modeling approach is not limited to the use of basic switching cells for analysis of existing power electronic circuits. Rather, it is a means to find different modular patterns in power electronic circuits, which can lead to several new circuit topologies.

3.2 Package Layout Design Using the Novel Switching Cells

As discussed above, a P-cell and a N-cell can construct a phase-leg that has some benefits compared to the traditional anti-parallel phase-leg. Figure 3.8 shows the diagrams of the two different inverter configurations, one uses conventional phase-leg while the other uses P-cell and N-cell phase-leg. Under inductive load condition, current commutation is between S_1 and D_2 as shown in Figure 3.8(a) when current direction is from load terminal P to N, or between S_2 and D_1 when current is from N to P. Therefore, in terms of natural current commutation pass, it is more reasonable to construct a phase-leg by P-cell and N-cell, as shown in Figure 3.8(b). Load current flows into the phase-leg through an N-cell and goes out of the phase-leg through a P-cell. Figure 3.8 also shows the stray inductance within each

phase-leg module. This stray inductance model is referred from [37]. L_{1U} and L_{2L} are introduced by terminal leads; L_{1L} and L_{2U} are the stray inductors of internal bus connecting the upper and lower unit; the values of these four inductors are relatively large. L_{C1}, L_{e1}, L_{C2} and L_{e2}, are associated with the die and wire bond, which are relatively small. Since the physical distance between the two commutating devices is reduced, the inductance is thus reduced. Comparing Figure 3.8 (a) and (b), inductances L_{1L} and L_{2U} introduced by the internal bus for the left phase-leg are reduced in the cell structure.



(a) Conventional full bridge inverter (b) Proposed phase-leg

Figure 3.8. Full bridge inverter with package parasitics.

The switching cells are the basic building blocks of almost all power electronics converters in terms of topology characteristic and operating unit, and they should be used as the base for manufacturing layout of single, dual and 6-pack modules that semiconductor manufacturers are produce.

Building power modules and verifying the concept proposed in last section are extremely expensive and time consuming. However, this process can be simplified by the aid of simulation. Also, modifying and optimization of the design can be carried out. Ansoft Q3D Extractor is used to do this job. The software uses Method of Moments (integral

equations) and Finite Element Method to compute capacitance, conductance, inductance and resistance matrices. Providing the correct dimensions, material properties (resistivity of conductors and permittivity of insulators) and boundary conditions (the conductors and current paths), the software can extract the structural impedances of any arbitrary geometry. Thus, the module parasitics can be understood thoroughly before modules are fabricated.

3.2.1 Electromagnetic Simulation Methodology

Q3D Extractor is software from Ansoft. It conducts electromagnetic field simulation employing a combination of the finite element method and the method of moments. In general, the finite element method divides the full problem space into smaller regions (tetrahedral elements) and represents the field in each sub-region with a local function. The method of moments divides the surface (or volumes) of conductors and dielectrics into many triangular (or tetrahedral) elements to represent the charges and currents present [38].

A finite element solver stores the value of a field quantity (such as electric potential) at each mesh node of a triangular or tetrahedral element. Inside each element, the field is interpolated from the values stored at the mesh nodes using local finite element basis functions. Maxwell's partial differential equations of the field quantities are linearized and can be transformed into a sparse matrix of linear algebraic equations that can be solved using traditional direct or iterative numerical methods. In the method of moments, field quantities are also interpolated over elements, but typically with simpler basis functions than in the finite element method. For capacitance problems, the field quantity of interest is the charge density on the surface of a conductor or dielectric interface. Triangular elements are used, and the charge density is approximated with a piecewise-constant basis function. For inductance problems, the field quantity is a vector (current density), and again piecewise-

constant basis functions are used. For DC inductance problems, the elements are tetrahedra (volume currents), and for AC inductance problems the elements are triangles (surface currents.) Green's function is used to represent the electrical interaction between any pair of elements. Using integrals of the Green's function and the basic functions, a dense matrix of linear equations is derived. An iterative method is used solve large problems.

The procedures of conducting the simulation are described in the following subsection.

3.2.2 Layout Design Using Q3D Extractor

A. Build the three dimensional model of the power device module and specify material

The three dimensional model can be drawn in Q3D Extractor or imported from other software, such as Auto CAD or Protel. Any of the following formats can be opened and edited: 3D Modeler file (*.sm3), SAT file (*.sat), STEP file (*.step,*. stp), IGES file (*.iges, *.igs) and ProE files (*.prt, *.asm) in Q3D Extractor.

The proposed phase-leg and the conventional phase-leg are drawn using Q3D Extractor. The diagrams of the phase-legs are shown in Figure 3.9, the marked loop1 and loop 2 are two current commutation loops in a phase-leg, that is, from upper IGBT to lower diode and from lower IGBT to upper diode. In a conventional module, the upper leg devices S_1 and D_1 are seated at one side, while the lower leg, namely S_2 and D_2 are seated at the other side. The layout designs are shown in Figure 3.9. The purpose here is to compare the stray inductance in the modules, therefore the base plate, case and encapsulant, which do not affect the electrical characteristic of the module, are neglected in the drawings. In the three dimensional modules, the bottom layer is DBC, the semiconductor dice are seated on the DBC, the black lines represent the bonding wires. The terminals are marked as in the figures. The physical

distance for loop1 is shown as the red trace in Figure 3.9 (b). It starts from lead C1 and passes through S_1, two groups of bond wires, output bus E1C2 and more wires to D_2. Loop2 is shown as the green line, and the length for loop2 is similar with loop1. In the proposed P-cell and N-cell modules in Figure 3.9 (b), the two devices in the commutation loop are seated at the same side. Thus, the physical length of the commutation loop is reduced. For example, loop1 shown as the red trace also starts from C1, goes through only one group of wires, and then reaches D_2. This is much shorter than the same loop in a conventional module. For a better comparison purpose, the two modules are similar in terms of substrate size and lead frame position. The physical size is listed in Table 3.1.

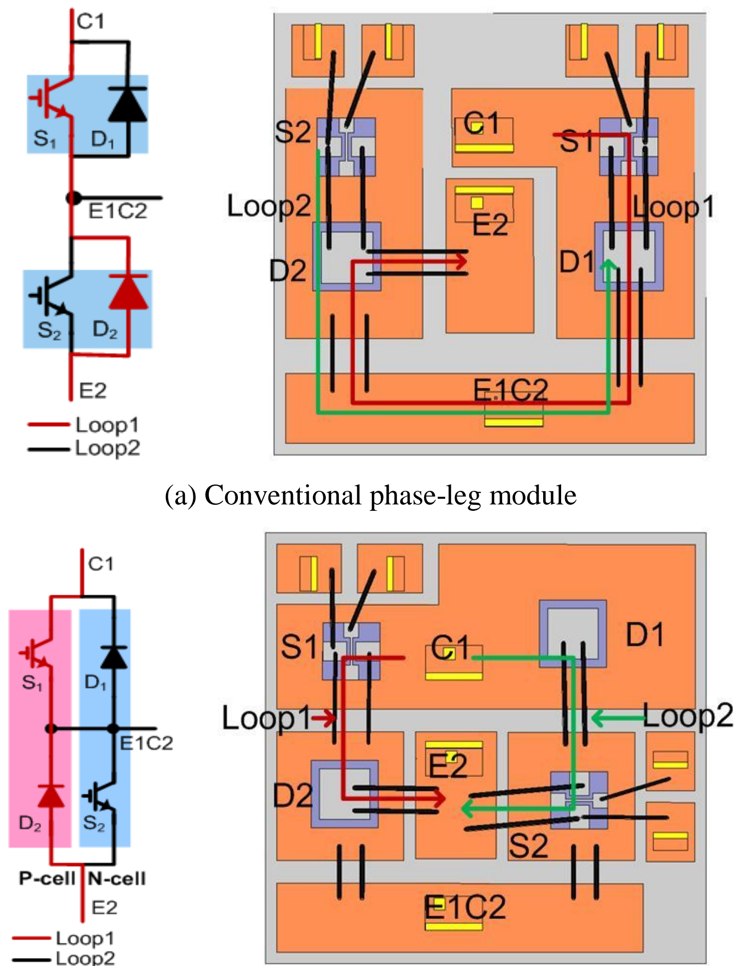
After the geometries of the modules are built in Q3D Extractor, materials for each of the components are assigned, which are shown in Table 3.2.

B. Analysis Setup

The next step is to assign excitations, which includes source and sink, representing the current in terminal and current out terminal, respectively. The parasitics of the path between source and sink is calculated. If there are multiple paths, the mutual parasitics between the paths will also be calculated. The results are stored in a matrix. Specifically, the items in the diagonal line are the self inductance (capacitance or resistance), and others are mutual values. It is necessary to point out that the size of the excitations can affect the results. For example, the larger the area of the excitations, the smaller the parasitic inductance is. Although it is not a dominant factor, to have the similar condition, it is better to draw the area as the real excitation contact area in the measurement.

When setting up the solver, there are options for DC or AC excitation source. When

using DC excitation, current is distributed evenly in the geometry, while using AC excitation, skin effect is considered. The default frequency for AC excitation is 100 kHz, the parasitic inductance is not affected when changing frequency, and capacitance does not change either; only resistance is scaled with the factor of $(f_{new}/f_{old})^{1/2}$. For inductance, which is the focus in this work, the DC result is larger than the AC result because the volume considered in DC simulation is larger.



(a) Conventional phase-leg module

(b) Proposed phase-leg module

Figure 3.9. Phase-leg module layout.

Table 3.1. Power Module Components Dimensions

	Conventional module	Proposed module
DBC size (mm)	37.0×38.0	37.5×38.5
DBC thickness (mil)	8(Cu), 25(Alumina)	8(Cu), 25(Alumina)
IGBT (mm)	5×5	5×5
Diode (mm)	5.85×5.85	5.85×5.85
Bond wires (diameter×number)	8 mil×5	8 mil×5

Table 3.2. Power Module Materials

Components	Materials
DBC insulator	Alumina, permittivity 9.2
DBC metallization	Copper, conductivity 58000000S/m
Dice	Silicon, permittivity 11.9
Bond wires	Aluminum, conductivity 38000000S/m

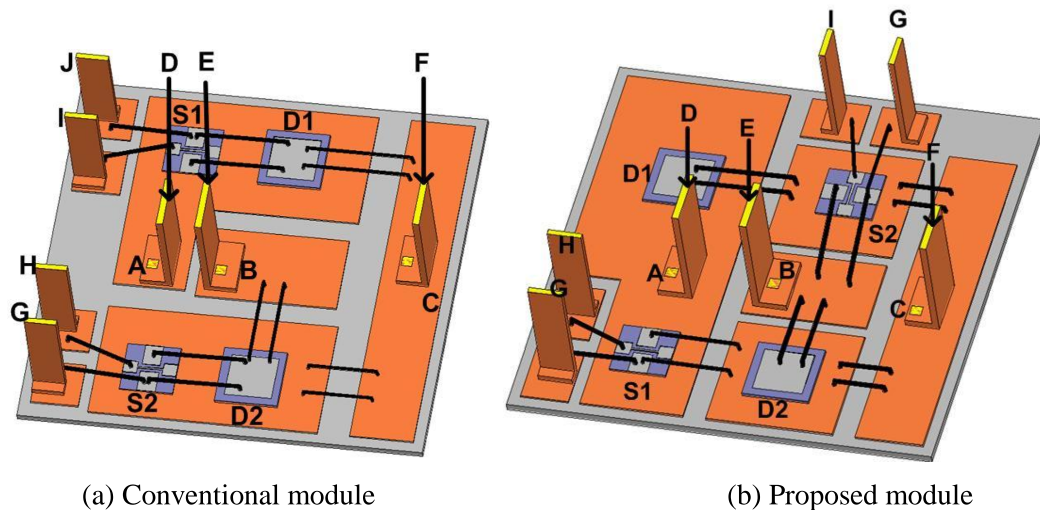
3.2.3 Simulation Results

The parasitic inductance associated with the module is studied thoroughly. The source and sink points are shown in Figure 3.10 as the yellow area. The simulation results are listed in Table 3.3.

The path from point A to point B is the commutation loop from the positive bus to the negative bus. There are two conduction paths: through S1-D2 which is loop1 shown in Figure 3.9, and through S2-D1 which is loop2. The simulation is conducted this way: when calculating loop1, the materials of S1 and D2 are set to copper while S2 and D1 is set to silicon, so that only the S1-D2 path conducts; the other path is calculated the same way. The inductance of the bus bar is also calculated separately. The path from A to D is the positive

bus bar, the path from B to E is the negative one, and the path from C to F is the AC output bus bar. They should have the same value since the same structure is used. In a commercial module, bus bars usually have larger dimensions and complex shape, however to simplify the fabrication process, the simulation uses a simpler copper bar. From H to G and from J to I are the gate drive loops.

It can be seen that the commutation loop inductances in the conventional module are both around 20 nH, while in the proposed module they are less than 10 nH. As expected, the rearrangement of the dice layout has an obvious effect on reducing the inductance of the DBC trace. For the other values, there are no large differences.



(a) Conventional module (b) Proposed module

Figure 3.10. Phase-leg modules with measuring points.

Table 3.3. Simulation Results of the Phase-leg Module Stray Inductance

	Conventional Layout		Proposed Layout	
	DC Value (nH)	AC Value (nH)	DC Value (nH)	AC Value (nH)
A-B (Loop1)	38.3	18.0	11.7	7.2
A-B(Loop2)	38.3	18.5	14.4	8.6
A-D (also B-E or C-F)	4.2	3.5	4.2	3.5
G-H	16.6	13.5	16.6	13.5
I-J	16.6	13.5	16.6	13.5
E-C (via S2)	24.4	16.7	18.4	12.4
E-C (via D2)	21.4	14.6	15.8	11.3
C-D (via D1)	24.3	15.9	24.4	15.8
C-D (via S1)	27.1	20.8	20.9	14.7

3.3 Summary

This chapter first introduces the concepts of P-cell and N-cell, and how they work as the basic function units in power converters. From packaging view point, the novel switching cells make it convenient to build power converters, by reducing the commutation loop parasitic inductance compared to the anti-parallel cells. Based on the topology analysis, a new packaging layout design of phase-leg module based on the novel switching cells is proposed. The proposed layout design as well as a conventional design is built using Ansoft Q3D Extractor. Electromagnetic simulation is conducted to study the module package parasitics. The detailed stray inductances inside the phase-leg modules are extracted. The simulation results show that the commutation loop inductance in the proposed module is largely reduced compared to the conventional module. This can benefit the IGBT switching behavior, which will be discussed in the next chapter.

4 Electrical Evaluation Based on Simulation

After the extraction of the module parasitics, mainly the stray inductance, electrical evaluation is performed under the influence of these parasitic elements for the two different power module layout cases. In power electronics, the most common actions are turning off and turning on of a switch. Thus the switching characteristic has been chosen to identify the performance of the two modules. In order to test the switching characteristic, the detailed parasitics in a test circuit has to be identified, which are mainly the stray inductance of the circuit trace and the parasitic capacitance of the power semiconductor devices. Fabricating a power module and building testing circuits are time consuming, but simulation can greatly accelerate the process. This chapter discusses the switching characterization using Synopsys Saber.

4.1 Parasitics Extraction from PCB

As mentioned previously, the DC bus connection also brings parasitic inductance to the commutation loop that cannot be neglected. The DC power comes from the power supply and a large aluminum electrolytic capacitor, and then goes to the PCB. Usually, several low ESR decoupling film capacitors are used to compensate the ESL of the cable. Therefore only the inductance from the capacitor to the DC bus needs to be considered. The printed circuit board (PCB) is shown in Figure 4.1. The decoupling capacitors and the power module are shown in the figure. The traces (polygon) between them are the ones which should be counted for the parasitics. To estimate the value, this part is analyzed using Q3D Extractor. Specifically, the top and bottom layers of the PCB design are exported to Q3D Extractor, the

gate drive parts are deleted for simplification. Figure 4.2 shows the shapes of the two traces after simplification.

The PCB design is firstly exported from Altium Designer as DWG or DXF file which can be imported in Q3D Extractor. However, there are several problems with the interface of these two software. First, Q3D cannot recognize the layer position, therefore each layer has to be imported one by one, and the position has to be edited manually. Second, some of the shapes of the polygon or wire in the PCB are complex. Q3D cannot deal with the very complicated objects, which turn into non-model objects. This has to be healed before conducting the simulation.

After the material is assigned, the thickness is set and the space between different layers is adjusted correctly, the parasitics can be extracted. For this specific design, the parasitic inductance is 28.4 nH.

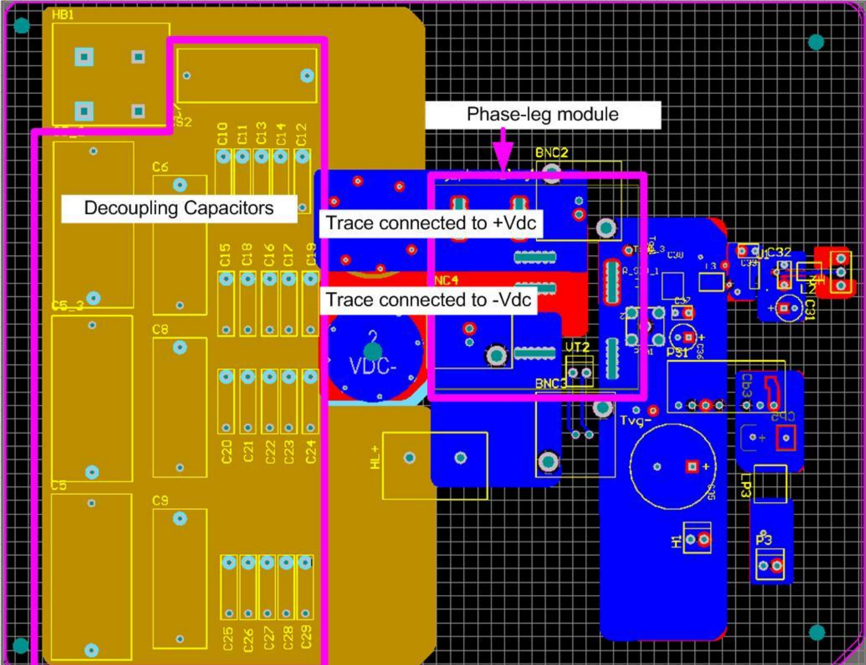


Figure 4.1. PCB used for double pulse tester.

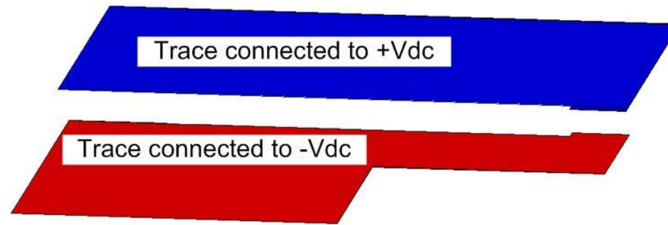


Figure 4.2. DC link in double pulse tester PCB.

4.2 IGBT and Diode Device Modeling

The switching behavior is more related to the device itself instead of the parasitics in the circuit. Therefore to study the module switching characteristic, a proper device model is very important. The devices used for this work are ABB soft punch through IGBT 5SMY12J1280 and fast recovery Diode 5SLY12F1200. Saber has a Model Architect tool to model semiconductor devices, magnetic components, thermal impedance, and battery and so on, as shown in Figure 4.3. The semiconductor modeling tools provide general physical level models and allow modification of characteristics and parameters. The tool allows interactive tuning of the parameters through graphical widgets directly placed on the model characteristics (Anchor Objects). An optimizer is also provided to help match the model characteristics with experimental data. These models are well suited for examining switching transients and losses in power supplies. In this dissertation, Saber Model Architect tool is used to model the tested IGBT and diode.

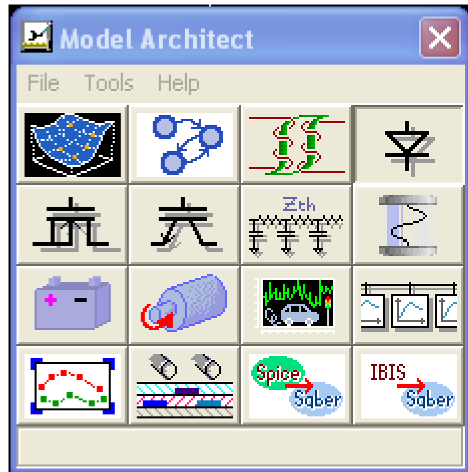


Figure 4.3 Saber tool: Model Architect

4.2.1 Modeling of Diode 5SLY12F1200

Saber provides a basic diode model dp, which is extensible to any specific diode as shown in Figure 4.4. The tool supports the following model features: forward I-V characteristic, junction capacitance, reverse recovery, and dynamic thermal. Since the purpose of this work is to compare the electrical behavior under different parasitic. The dynamic thermal behavior of the devices is not considered. All the characteristics are under nominal temperature 25℃.

The first step is to get the forward I-V characteristic from the datasheet. The software provides Scanned Data Utility to load curve from experiment or datasheet. In this work, both the IGBT and diode are modeled based on ABB datasheets [39] [40]. Figure 4.5 shows the scanned data utility. The Scanned Data Utility provides an interactive way of importing data from a scanned graph, thus avoiding the tedious process of point-by-point coordinate entry into a spreadsheet. After defining the range and scale of each axis, curves are defined by mouse-clicking on selected points. After the reference I-V curve is loaded, the Toggle Anchor Objects is used to tune the actual I-V curve of the model to match the reference as

shown in Figure 4.6, the purple curve is the imported one, and the yellow is the real I-V curve of the model.

The junction capacitance versus voltage and reverse recovery waveform are modeled using the same method. However, since no junction capacitance can be found in [40], this information is taken from another 75 A diode from ABB. The reverse recovery waveform in [40] is under 125°C. The reverse recovery waveform is tuned using the listed data: di/dt, I_{rr} and t_{rr}. Therefore, this diode model can be modeled more accurate using experimental data or waveform.

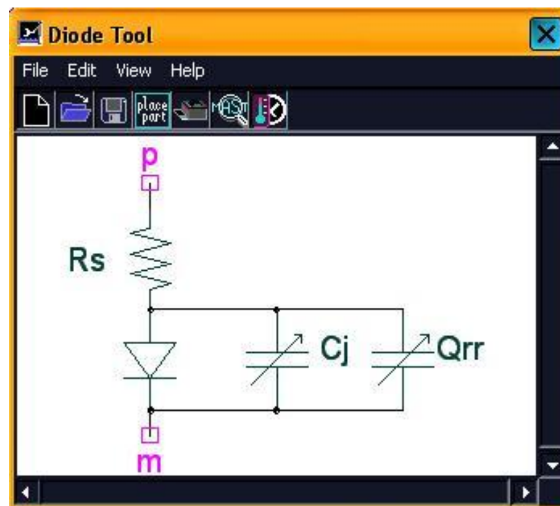


Figure 4.4. Saber diode model user interface.

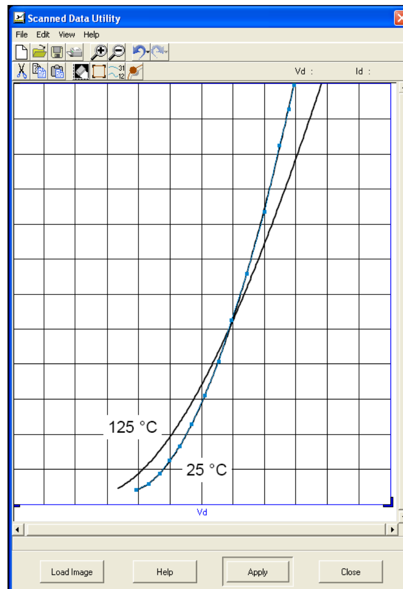


Figure 4.5. Scanned I-V curve from datasheet.

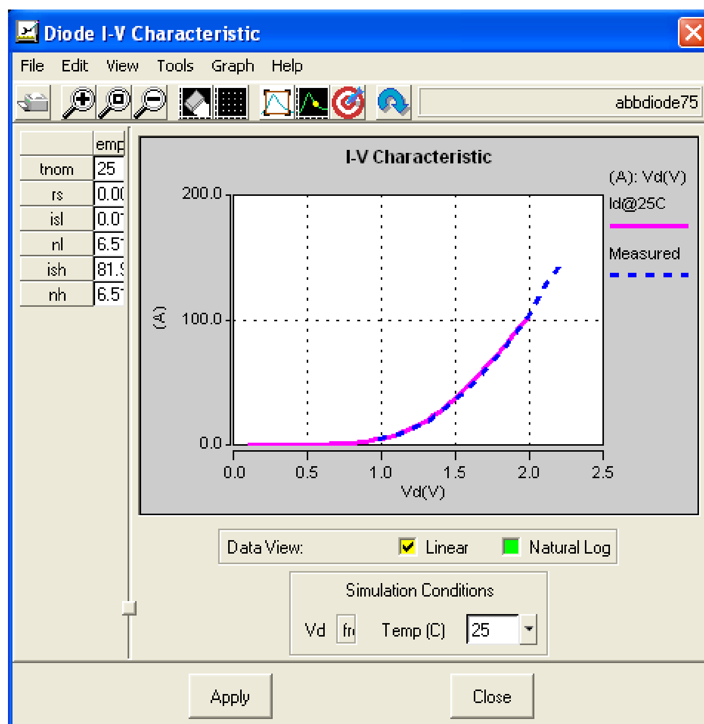


Figure 4.6. Diode I-V characteristic after curve fitting from the loaded I-V curve.

4.2.2 Modeling of IGBT 5SMY12J1280

The IGBT characterization tool and model is a simplification of the Hefner IGBT model. The Hefner IGBT model is a highly accurate physics-based model widely accepted in

industry. However, because it is very complicated to fully describe the detailed physical parameters that go into a Hefner model, the Saber model library provides a more generic and proven level-1 IGBT model.

The IGBT model is shown in Figure 4.7. The characterization tool is more complicated than for a diode. It has the following features to characterize: I_c versus V_{ge} and I_c versus V_{ce}, C_{oes}, C_{ies}, C_{res}, gate charge verification, switching performance verification, temperature characterization for DC and Transient characteristics, flexible diode selection and specification options for IGBTs that include anti-parallel diodes in the package.

DC characteristics and capacitance curve are scanned and imported from datasheet [39]. Using curve fitting as described in section 4.2.1, these features can be characterized. The transient characteristic to be adjusted is the shape of the tail current. There is no such information in the datasheet. Therefore it is characterized using current fall time t_f. Further modification needs experimental results for curve fitting.

The tool provides two approaches via simulation from within the tool to verify the IGBT model. First one is gate charge waveform. This function can generate the waveform of V_{GE} to compare with the datasheet waveform. It is mainly related to the three junction capacitance, the capacitance curve should be adjusted back and forth to match the gate charge waveform. The matched result is shown in Figure 4.8. The blue one is imported from datasheet; the green one is generated from the IGBT model.

The other verification is the switching behavior as shown in Figure 4.9. The test circuit is provided by the tool. The test conditions can be configured to match the datasheet. The switching time and loss agree with the datasheet value.

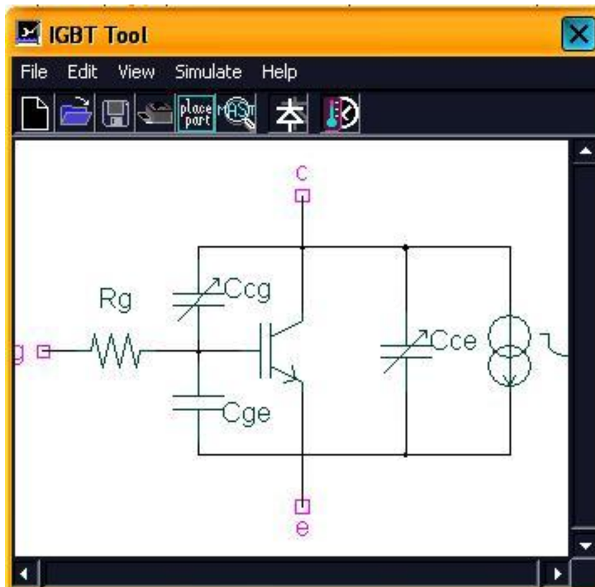


Figure 4.7. Saber IGBT model user interface.

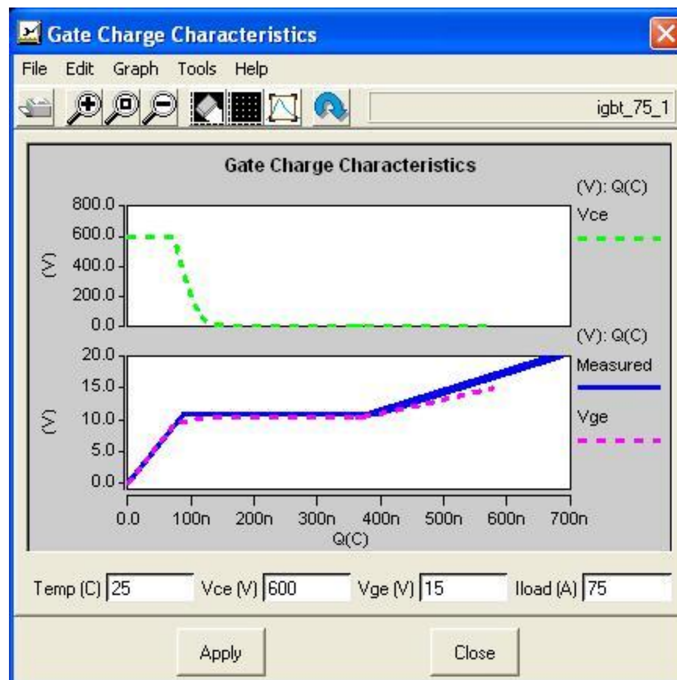
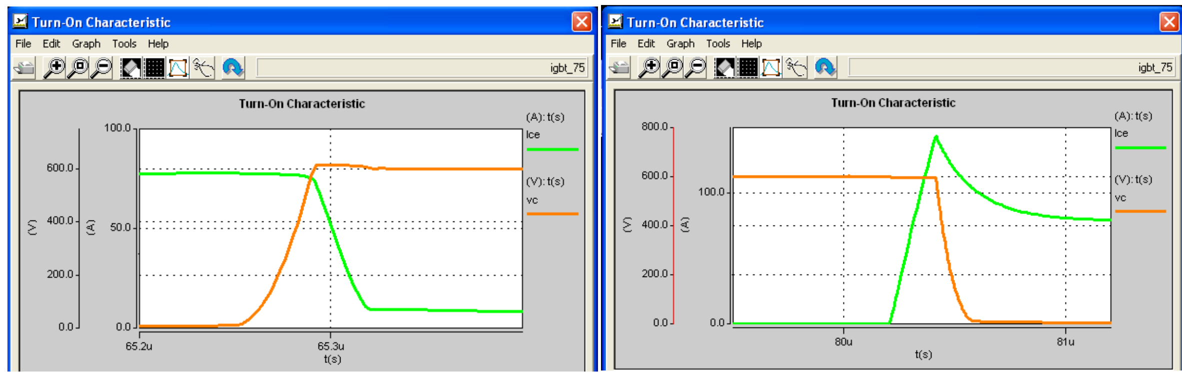


Figure 4.8. Verification of gate charge.



(a) Turn on waveform (b) Turn off waveform

Figure 4.9. Verification of switching waveform.

4.3 Switching Characterization

A double pulse tester is used to carry out switching characterization under the influence of the module parasitics. As shown in Figure 4.10, it is essentially a step down converter. The major components include one IGBT and one diode inside the module and an inductive load L_{load}. The parameters used in the double pulse tester are shown in Table 4.1. The stray inductance includes DC bus stray inductance L_{esl} and the module stray inductance l_1, l_2, l_3 and l_4. The module stray inductance not only involves the layout but also the terminal leads. The sum of l_1, l_2, l_3 and l_4 is the loop inductance (loop2) plus two terminal-leads inductances (i.e. A-D and B-E) listed in Table 3.3. The simulation is conducted under 300 V/ 75 A.

The typical waveforms of double pulse tester are shown in Figure 4.11. As can be seen, only two pulses are needed. The first pulse is used to obtain the desired current. The switch turns off at the desired current, current commutates to the diode, and turn-off behavior can be observed accordingly. After a short while, the switch is turned on at the second pulse. Due to the existence of the large inductive load, the current does not change much, and turn-on behavior under the desired current can be observed. Here, the double pulse tester is implemented in Synopsys Saber.

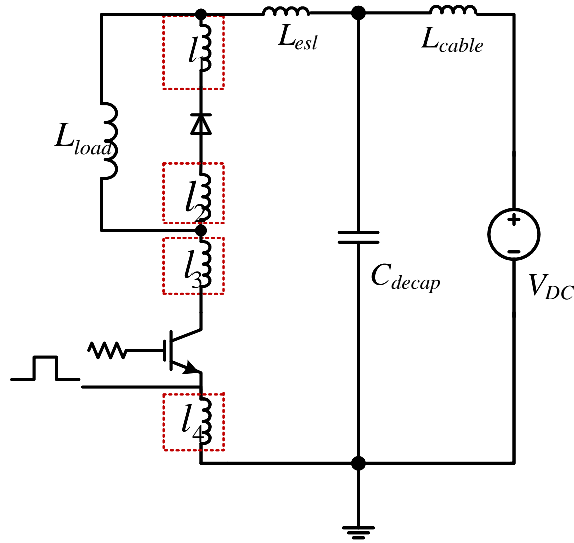


Figure 4.10. Schematic of double pulse tester.

Table 4.1. Parameters in Double Pulse Tester

Parameters	Values
L_{load}	47.2 μH
IGBT 5SMY12J1280	1200 V, 75 A
Diode 5SLY12F1200	1200 V, 75 A
DC source voltage	300 V
L_{esl}, C_{decap}	28.4 nH, 3.38 μF
l_1+ l_2+ l_3+ l_4 in conventional module	25.5 nH
l_1+ l_2+ l_3+ l_4 in proposed module	15.6 nH

Simulation results from the double pulse tester show the superiority of the proposed module comparing to the conventional one. The voltage across the IGBT during turn off is shown in Figure 4.12 (a). After the voltage rises to the DC link voltage, there is an abrupt drop of the IGBT current, high di/dt causes a voltage drop across the stray inductance, which is applied on the IGBT and causes voltage overshoot and oscillation. As can be seen, the voltage overshoot is 75 V in the conventional module, while that in the proposed module is

60 V. The turn off switching loss is also different for the two cases as shown in Figure 4.12 (c). During turn-on, after the IGBT current reaches the load current, the diode reverse recovery begins, and the IGBT turn-on current has an overshoot. After that, this current rings between the parasitic inductance and the diode parasitic capacitance. This phenomenon is shown in Figure 4.12 (d). The ringing damps fast in the proposed module as a result of the reduced inductance.

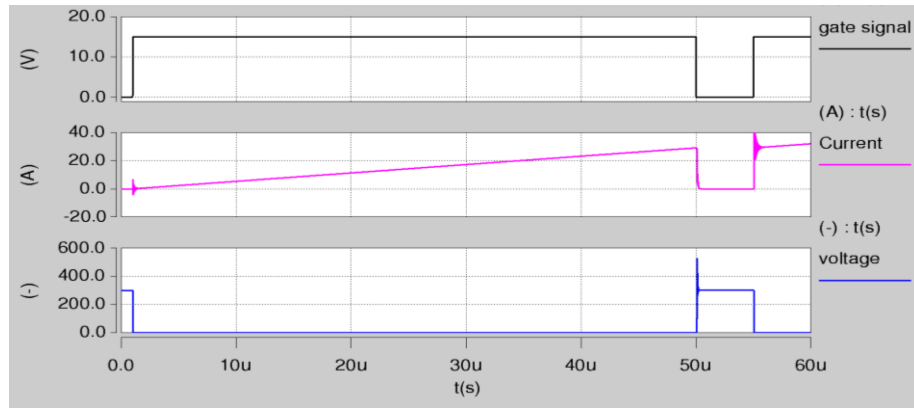
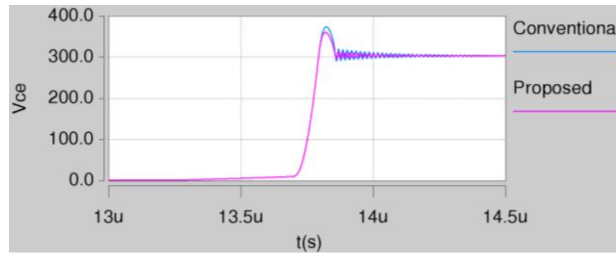
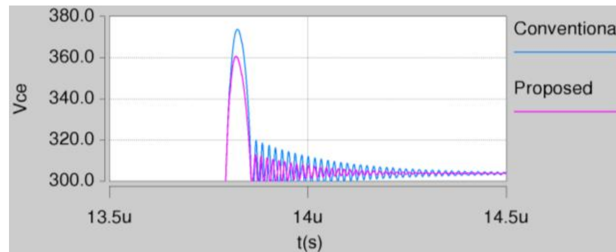


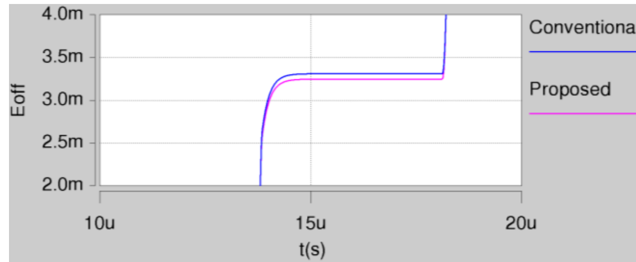
Figure 4.11 Typical waveforms of double pulse tester.



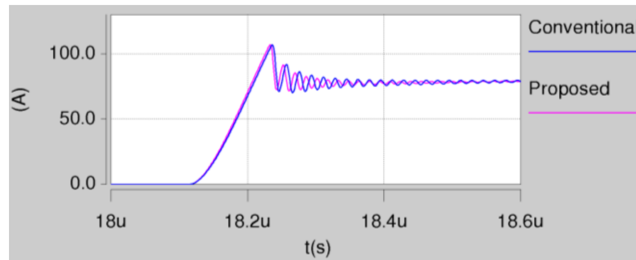
(a) Voltage waveform across IGBT at turn-off.



(b) Overshoot voltage zoom out



(c) Turn off switching loss



(d) IGBT current waveform at turn-on.

Figure 4.12. Switching behaviors under module parasitics.

4.4 Modeling and Analysis of Switching Behaviors

The oscillation during turn-on and turn-off process is triggered by not only the stray inductance but also the device capacitance in the IGBT and diode [41][42][43]. The stray

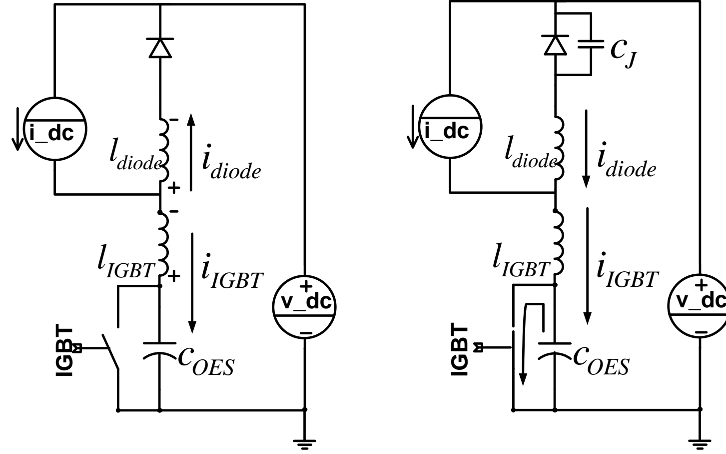
inductance introduced by the package and the capacitance of the device compose a resonant circuit that causes voltage and current oscillation at switching. This section looks into the different current paths during turn-on and turn-off.

1. Identification of Turn-Off Resonance Circuit

The turn-off resonance sets up after the IGBT voltage reaches the dc source voltage. When the diode conducts current, the diode body capacitor C_J is bypassed. Resonance occurs between stray inductances l_{diode}, l_{IGBT} and IGBT output capacitor C_{OES}, as shown in Figure 4.13 (a). l_{diode} is the sum of stray inductance connected to the cathode and anode of the diode, which is 13.7 nH in the conventional module and 7.7 nH in the proposed module from Table 4.1. and l_{IGBT} is the sum of stray inductance connected to the collector and emitter of the IGBT, which is the same value as l_{diode}.

2. Identification of Turn-On Resonance Circuit

The turn-on oscillation occurs after the IGBT current reaches the load current. The voltage across the IGBT starts to drop, while the diode voltage increases. There is discharge current from capacitor C_{OES}. However, since the IGBT is already turned on, this current goes through the IGBT and does not resonate with the stray inductance. On the other hand, the diode capacitor C_J is also discharged. Therefore, it is calculated that the resonance is between the stray inductance and C_J, as shown in Figure 4.13 (b).



(a) Turn-off equivalent resonant circuit (b) Turn-on equivalent resonant circuit

Figure 4.13. Switching transient circuit model.

4.5 Summary

This chapter is phase-leg module switching behavior simulation and analysis under the influence of package and circuit parasitic inductance. First, the DC link stray inductance is extracted from the test board using Q3D Extractor. The semiconductor devices are selected from ABB. Since there is no device model available from the company, the IGBT and diode are modeled in Synopsys Saber using the built in tool Model Architect. A double pulse tester is built using Saber. The turn-off over shoot voltage and turn-on current ringing are observed through simulation. The advantage of the proposed module with less stray inductance is shown in the switching characteristic. The overshoot voltage is reduced and the current ringing is damped compared to the conventional module. Then, the turn-on and turn-off transient equivalent circuits are established. The resonance between the parasitic inductance and capacitance associated with the switching is explained.

5 Experimental Verification

5.1 Parasitics Measurement

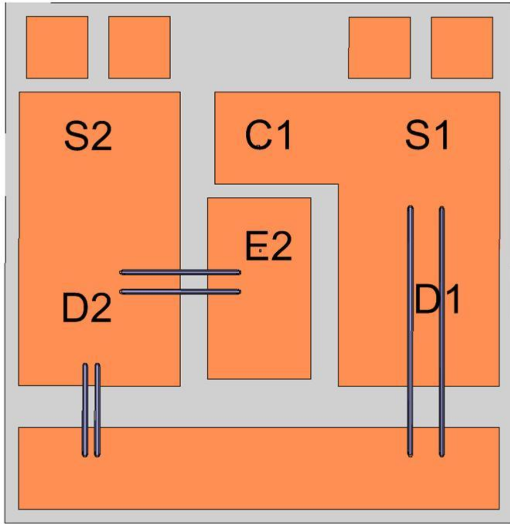
To verify the results of the parasitic extraction based on the simulation by Q3D Extractor, the two phase-leg modules in terms of conventional and P-cell and N-cell based layouts are fabricated and measured in laboratory.

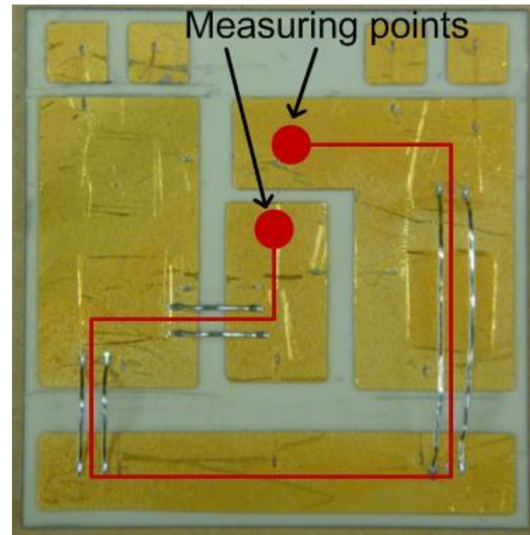
The nano-henry level power module stray inductance measurement can be challenging. The first challenge is that since IGBT is a normally off device, the commutation loop is not conducting by nature. In literature [47], the commutation loop is formed by applying a gate voltage to the active device MOSFET. As we know that MOSFET has three layers, take an n-type MOSFET for example, if a positive gate voltage is applied to the gate, a conducting channel is established at the p body layer; the source layer and the drain layer are both n layer, therefore the electrons can move back and forth freely in the device under a small alternating voltage. However, this method doesn't work for IGBTs. There is one more p layer in the structure of IGBT, which forms a pn junction at the collector side. This pn junction cannot conduct when it is reverse biased. The measuring tools, both multi-meter and impedance analyzer, use small alternating current as a measuring signal. Therefore, an IGBT cannot conduct under small AC signal, and the commutation loop cannot be formed by simply applying gate voltage.

Thus, the inductance should be measured part by part. However, the inductance is too small to be accurate in this way. Also, it does not take the coupling effect between the pieces into account. In the previous simulation, the devices are set to copper to get a conductive

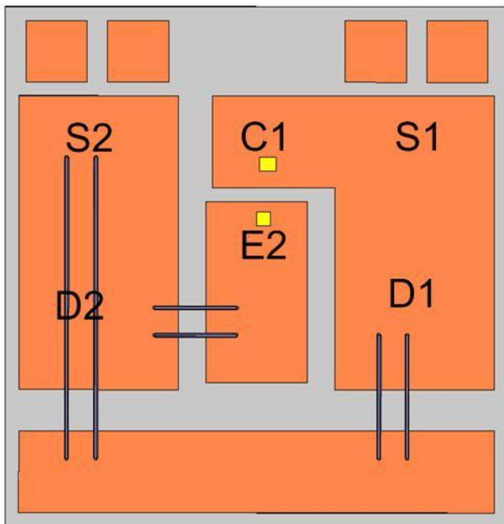
commutation loop. Actually, they have the same effect as the devices are set to conductor and the wires bonded directly to DBC. Therefore, in the measurement, modules without devices are fabricated, in which the wires are bonded directly to DBC. Taking the conventional module loop1 in Figure 3.9 (a) as an example, to measure this loop inductance, S1 and D2 need be conducting, so that the wires are bonded directly to the DBC where S1 and D2 seat as shown in Figure 5.2 (a). The conducting trace actually is from terminal C1 through DBC copper trace to S1, and through a group of bonding wires to the DBC where output terminal seats, and then through another set of wires to D2, from D2, through another group of wires to the negative terminal E2. The simulated result for this arrangement is very close to the values shown in Table 3.3.

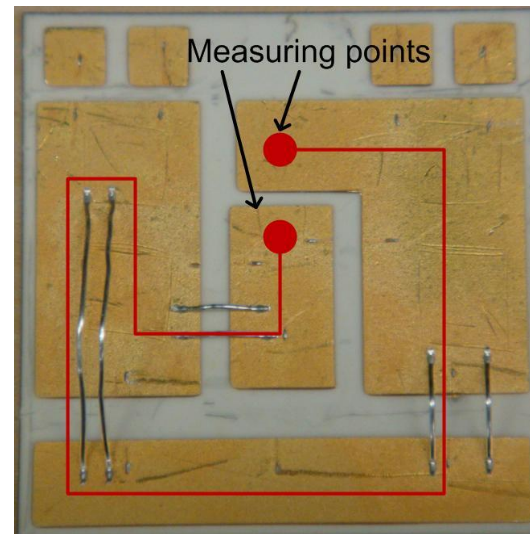
Taking the same method, commutation loop2 in the conventional phase-leg and commutation loop1 and loop2 in the proposed phase-leg are fabricated as shown in Figure 5.2 (b), and Figure 5.2 (c) and (d). Basically, they are the etched DBC patterns with wires which are bonded to the position of the devices that should conduct in the commutation loop. The commutation loops are made conductive this way and the stray inductance is measured.





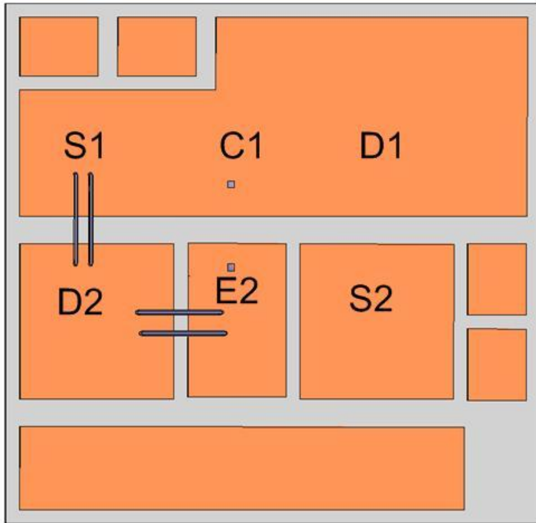
(a) Conventional module loop1

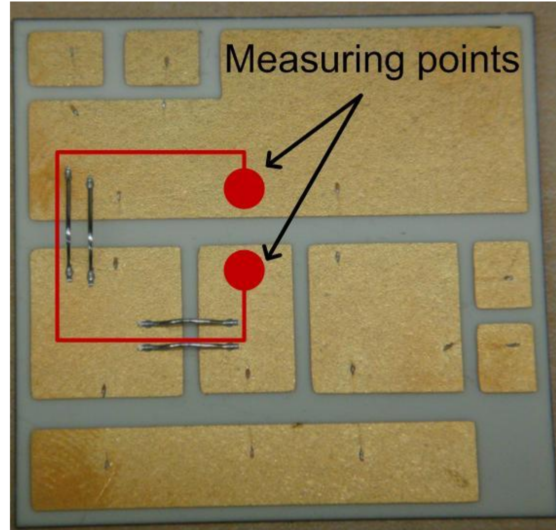




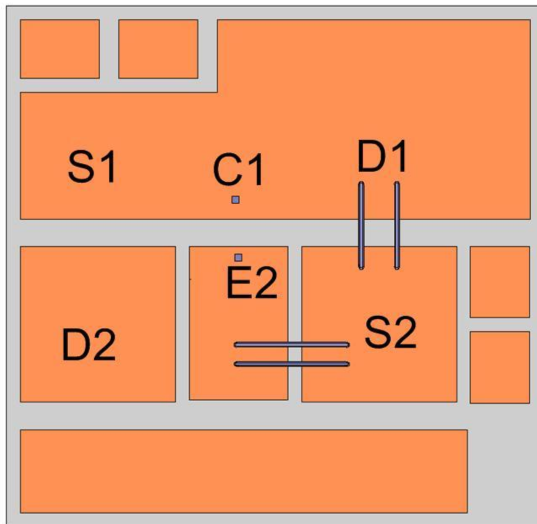
(b) Conventional module loop2

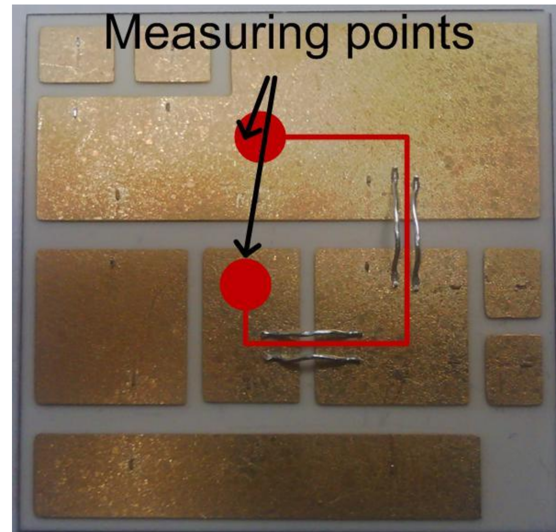
Figure 5.1 Conventional module DBC pattern with bonding wires designed for parasitic measurement.





(a) Proposed module loop1





(b) Proposed module loop2

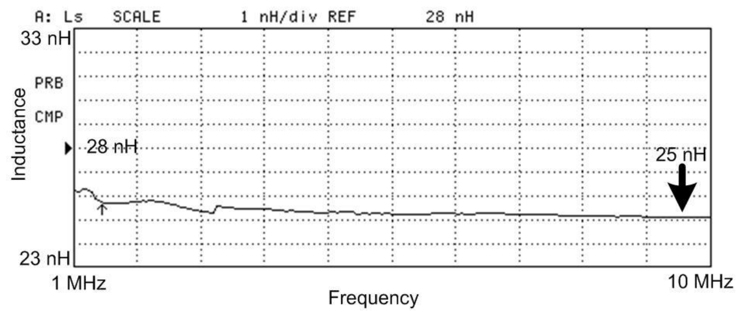
Figure 5.2. Proposed module DBC pattern with bonding wires designed for parasitic measurement.

Another challenge is the measuring equipment. Since the inductance is very small, Agilent precision impedance analyzer 4294A is used as shown in Figure 5.3. It has a wide measurement frequency range: from 40 Hz to 110 MHz. High frequency is necessary for the small inductance to have a measurable impedance. The frequency used in this case is from 1 MHz to 10 MHz, the estimated impedance for the module parasitic should be 50 mΩ to 0.5 Ω. So that when a current is applied to the inductance, sufficient voltage, 10 mV or larger, is

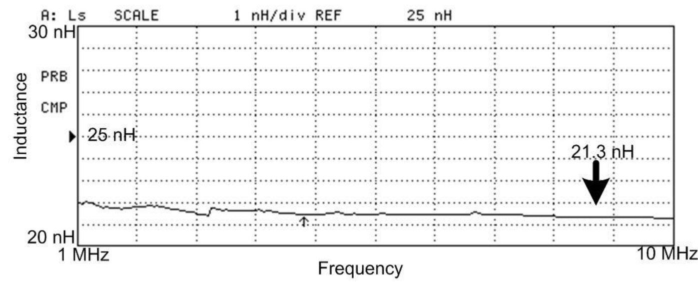
ensured, therefore the accuracy of the measurement is guaranteed. Since the measurement uses alternative current, this result should compare to the AC simulation results listed in Table III. Meanwhile, using the correct probe fixture is also critical in this measurement. The commonly used alligator probe is not proper in this condition. The wires with the alligator probe introduce parasitics that are comparable to the one under test, and even larger. Here we use a pin probe; the shape of the probe is fixed. The parasitics with this probe is small and can be completely compensated using calibration.

Figure 5.4 shows the measured results. The testing frequency range is from 1 MHz to 10 MHz, where the impedance of the module is inductive. The level of the solid triangle in the left of the graph is the reference inductance value, which is shown in the top. The scale of the division is also shown in the top. With the reference and the scale, the value of the measurement line can be decided. For example, in Figure 5.4 (a), the measured line is two to three divisions below the reference value, which is 28 nH, therefore the measured value is between 25 nH to 26 nH. The complete comparison of the measurement and simulation is listed in Table 5.1. The measurement value should compare with the AC simulation results, because in measurement, AC excitation is used.

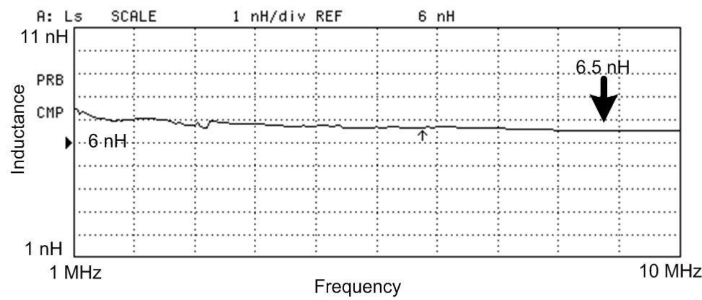
Figure 5.3. Impedance analyzer and probe fixture for parasitic measurement.



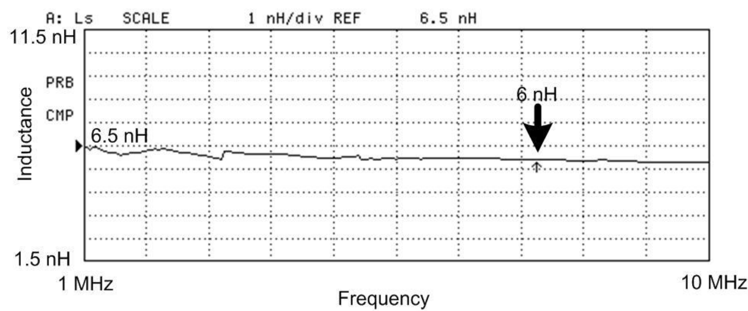
(a) Measured result of stray inductance for conventional module loop1



(b) Measured result of stray inductance for conventional module loop2



(c) Measured result of stray inductance for proposed module loop1



(d) Measured result of stray inductance for proposed module loop2

Figure 5.4. Measured results.

Table 5.1. Stray Inductance Comparison of the Measurement and Simulation

		Simulation Result (nH)	Measurement Result (nH)
Conventional Module	Loop 1	20.5	25
	Loop 2	20.3	21
Proposed Module	Loop 1	7.2	6.5
	Loop 2	8.6	6.0

5.2 Static Characteristics Testing

The two phase-leg modules, both conventional and proposed layout designs are fabricated as shown in Figure 5.5. For simplicity, base plate and case are neglected, because they do not affect the electrical behavior in a relatively short time.

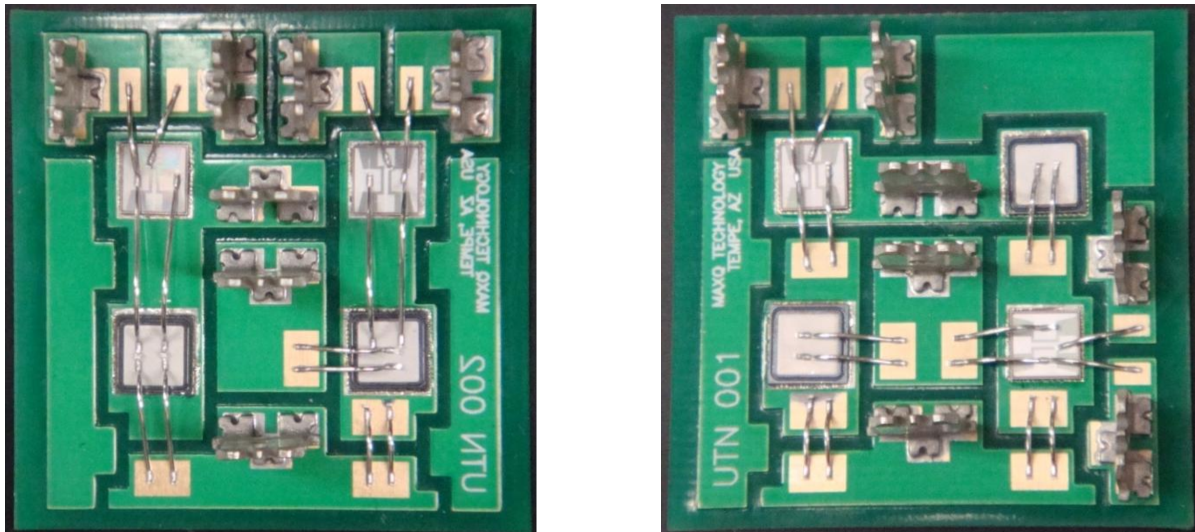


Figure 5.5. Fabricated modules (Conventional one on the left and the proposed one on the right).

Static and dynamic switching testing are the two basic aspects of power semiconductor devices characterization. Static characteristics include output characteristic (I-V curve), transfer characteristic for transistors (I_S vs V_{GE} at certain V_{CE}), leakage current, break down voltage, threshold voltage, etc. These characteristics can be obtained using a Tektronics

model 317B curve tracer. In this work, the static characteristic testing also serves another purpose, testing the functionality of the module. The yield rate of the power module is not one hundred percent ensured, especially for the custom design. The two major factors that cause failure are destroyed dice and broken bonding wires. The dice are delicate and can be cracked during fabrication, especially when bond wires on it. The wire bond connections are not that strong, they can break off the device or DBC. Therefore, electrical testing is necessary after fabrication; using a curve tracer to do static testing is one way to check the devices.

Tektronix 371B curve tracer and the probe kit are shown in Figure 5.6. Output characteristic for IGBT is measured as shown in Figure 5.7(a). Two different gate drive voltages are used, 10 V and 15 V, respectively. As can be seen, I_C is zero when V_{CE} is very small, and starts to grow when V_{CE} is around 0.7 V. When the current reaches 15 A, the $V_{CE(on)}$ is around 2.7 V. While for the same V_{CE}, current is larger at higher gate voltage. However, these curves include the test probe fixture resistance and are not very accurate; therefore the fixture wire I-V characteristic, which is the resistance, is measured as shown in Figure 5.7(b). The calculated resistance is 0.02 Ω. The output characteristic after adjustment is shown in Figure 5.7(c). After compensation, $V_{CE(on)}$ is 2.2 V, which is the same as in the datasheet. The output characteristic in the datasheet is shown in Figure 5.8(a) and (b) for comparison. The FWD I-V curve is also measured, as shown in Figure 5.9.

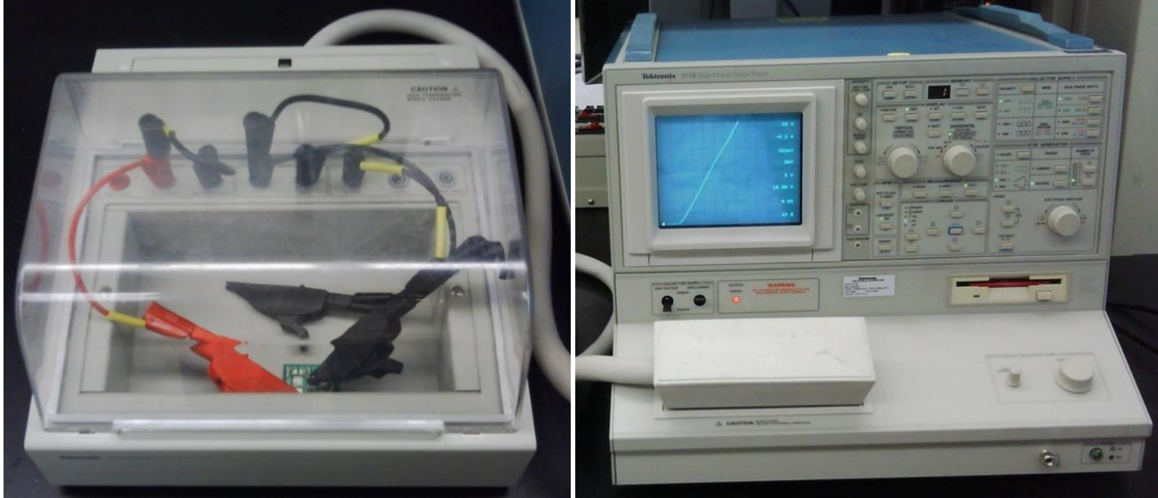
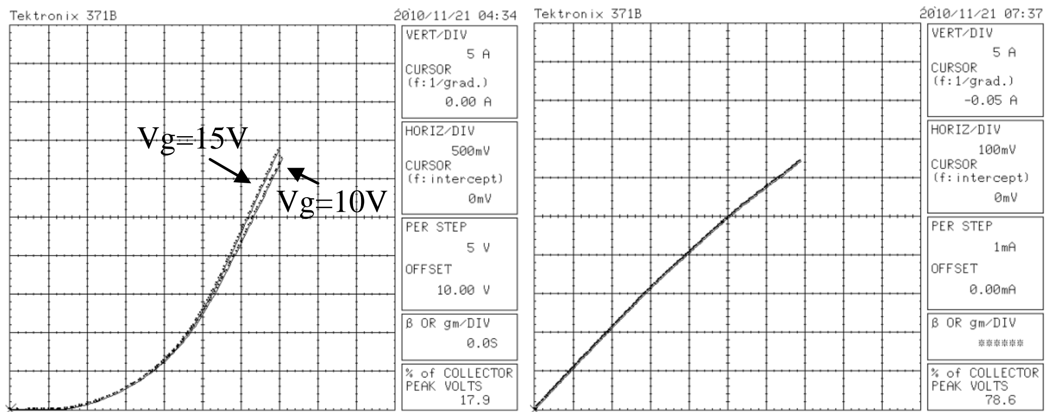
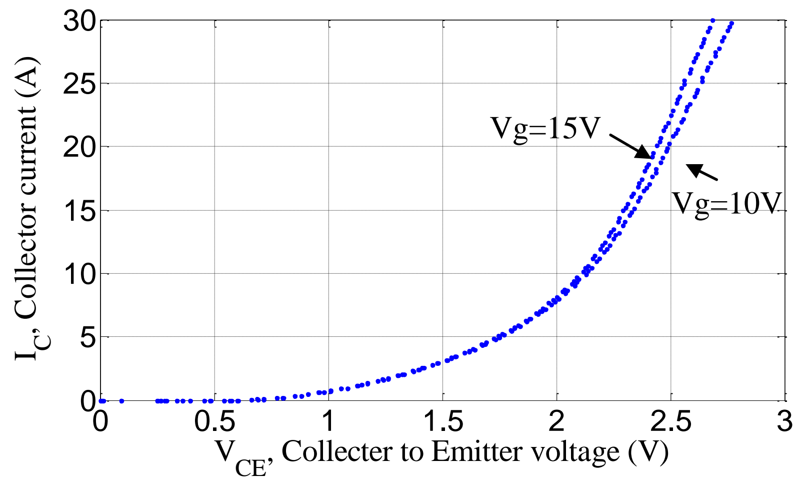


Figure 5.6. Tektronix 371B curve tracer.

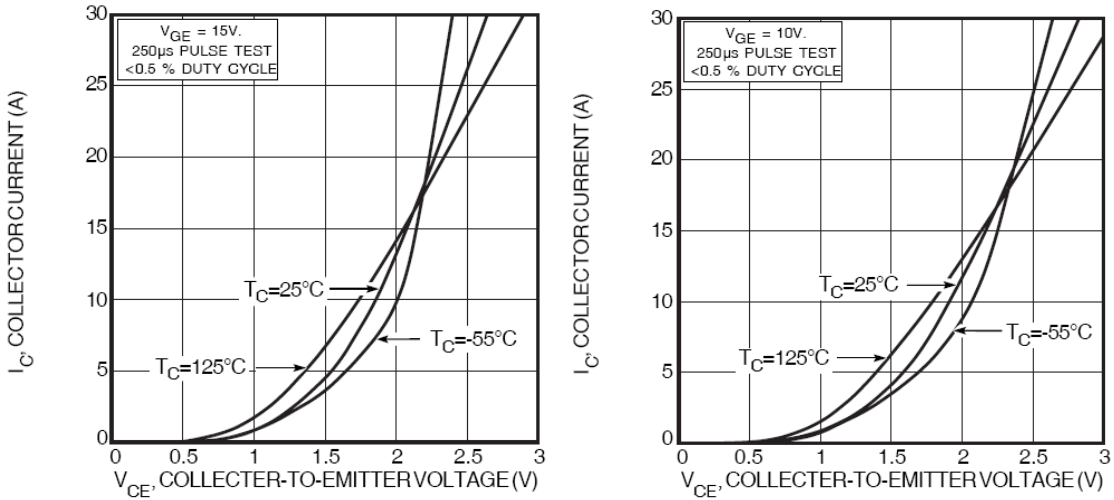


(a) IGBT tested output characteristic (b) Testing fixture short circuit I-V curve



(c) IGBT output characteristic after compensation

Figure 5.7 Measured IGBT output characteristic.



(a) datasheet I-V curve (at 15V gate voltage) (b) datasheet I-V curve (at 10 V gate voltage)

Figure 5.8. IGBT output characteristic from datasheet.

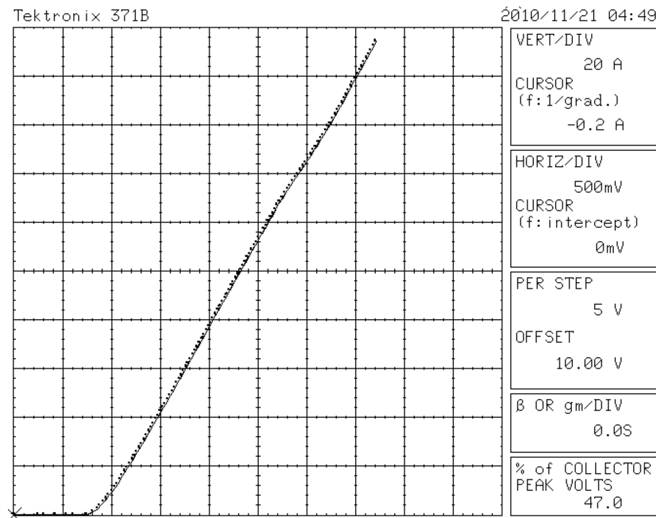


Figure 5.9. FWD I-V curve.

5.3 Switching Characterization

The circuit parameters and testing conditions are shown in Table 5.2.

Table 5.2. Circuit parameters

Parameters	Value/ Rating
DC electrolytic capacitor C_{bulk}	1000 μF/450 V
DC decoupling capacitors C_{dec}	2.9 μF
Gate resistor	3 Ω
IGBT 5SMY12J1280	1200 V, 75 A
Diode 5SLY12F1200	1200 V, 75 A
Load inductor	47 μH
Testing condition	300 V/ 75 A, room temperature

5.3.1 Double Pulse Tester

Switching characterization can be conducted with only two pulses instead of a practical converter. The first pulse is used to charge the load inductor to the testing current, and then the device under test (DUT) is turned off. As a result, the turn off characteristic can be captured. After a few microseconds the device is turned on and turn-on characteristic is obtained. The circuit diagram and operating principle was discussed in Section 4.2. This section focuses on the experimental setup and relevant practical concerns.

Figure 5.10 shows the printed circuit board of the DPT. A 450 V/ 1000 μF electrolytic cap is soldered at the back of the board. Three low inductance 300 nH film caps and 20 100 nH ceramic capacitors together work as decoupling capacitors. A shunt resistor is used to measure current. The power module is attached at the back of the board. Also, the gate drive circuit is also on the same board and close to the gate terminal of the power module. BNC connectors are for accurate voltage measurement.

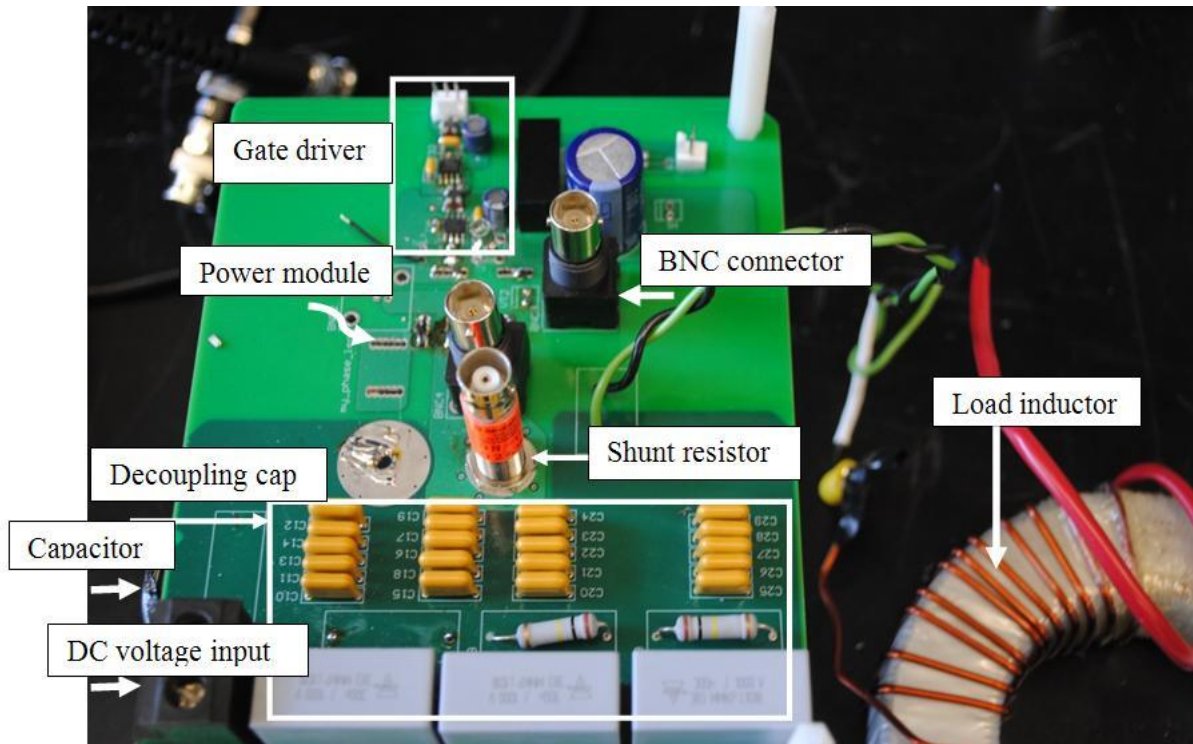
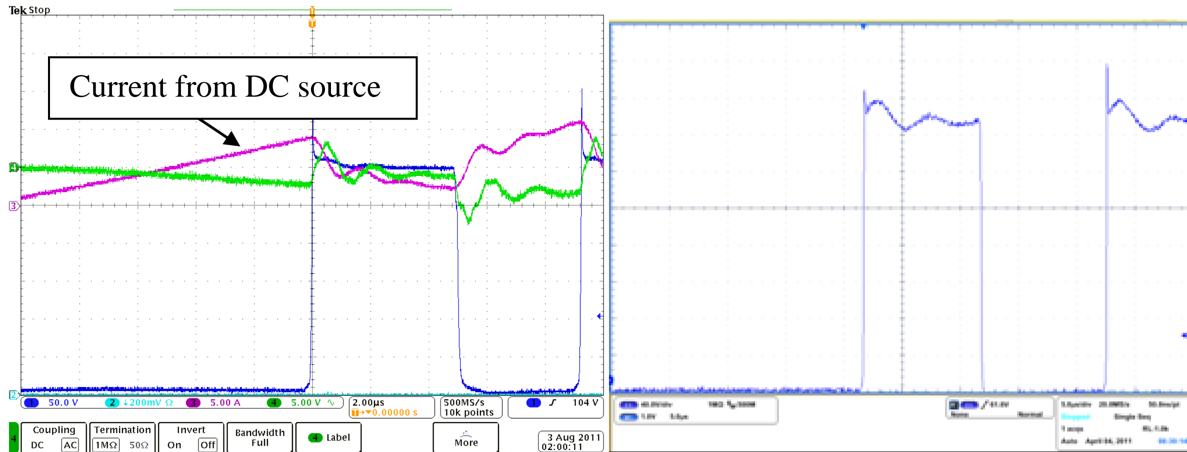


Figure 5.10. Printed circuit board of DPT.

The electrolytic capacitor is necessary as energy storage. Actually, a large part of the load current draws from this capacitor, since there is usually a long cable connected from the DC voltage source and impedance is much higher. Figure 5.11 (a) shows the measured current from the DC source, which is only 9 A in a 75 A test, while the other 66 A is from the capacitor on board. This capacitor should be as close as possible to the decoupling capacitors and the power module to reduce the stray inductance from the connection. Otherwise, the parasitic inductance and the decoupling capacitor form a resonant circuit, which causes a low frequency oscillation after switching transition, as shown in Figure 5.11 (b).

During switching transitions, DC source and C_{bulk} will not be able to provide adequate energy quickly enough due to high values of ESR and ESL, leading to large ringing of the voltage across the positive and negative buses. Capacitors with low ESR and ESL are added to provide a low impedance path for the transient current. During transients, most of the

current will flow in the loop formed by the decoupling capacitor and the power module. In this way, C_{dec} decouples this loop from the rest of the circuit [48]. Film and ceramic capacitors, which have low ESR and ESL, are chosen to serve this purpose. Paralleling of the decoupling capacitor is also useful, to reduce the ESR and ESL of the decoupling capacitors themselves.



(a) Current drawn from voltage source (b) V_{CE} with distortion

Figure 5.11. Demonstration of the cable stray inductance effect.

The current measuring tool should be carefully chosen to get an accurate result. The current measured here is IGBT current I_C. During transition the current slope is very sharp, from the datasheet of the ABB IGBT, the rise time is 50 ns while the fall time is 75 ns. This equals a frequency of $f = \frac{0.25}{t_r} = 5\,MHz$ [48]. Typically a 5 times margin should be left, implying that the current sensor should have a bandwidth of at least 25 MHz. The tools most widely used for oscilloscope measurements are current transformers, Rogowski coils, surface mount resistors, and coaxial shunts. Rogowski coil has a bandwidth typically under 1 MHz. Current transformers have similar bandwidth. Therefore, these two categories are not sufficient to measure transient current. Surface mount resistors have enough bandwidth ideally. However, usually, the parasitics with surface mount resistors are significant at high

frequency. When measuring the voltage drop on the resistors, the measured signal includes both the resistors and parasitics, which usually has a very different shape with a lot of oscillations. On the other hand, coaxial shunt resistor has a special structure to avoid the parasitics. An outer layer provides shielding from the magnetic field generated by switching. There is an inner resistive layer where the current flows through. The measuring wires are in the middle of the tube; therefore, not much inductive coupling occureswith the shunt current. The connection to the oscilloscope is through a coaxial cable, which eliminates the probe connection. The voltage across the resistor has to be less than 10 V, since there is no attenuation for the coaxial cable. This voltage is directly connected to oscilloscope. In this experiment, the testing current is 75 A, during reverse recovery, the current can be as high as 150 A. The resistance should be less than 0.06 Ω. In this experiment a 0.025 Ω shunt resistor from T&M research is chosen. The bandwidth is 1200 MHz, the power rating is 3 mJ.

The gate drive circuit is shown in Figure 5.12. The double pulse signal is fed to an isolator to separate the signal ground and gate driver ground. Dual channel isolator with isolated integrated DC-to-DC converter ADuM5240 is used. The gate driver is IXDI409, with 9 A peak capacity. To provide an isolated power supply for the gate driver, another isolated DC to DC converter is used. It has a 24 V input and can provide ±15 V. Several surface mount common mode chokes are used in the signal path or the power supply, to avoid common mode noise.

The voltage is measured in several places in the circuit. V_{CE} is measured using a high voltage probe Tektronix P5100. V_{GE} is measured using active probe P6139. DC bus voltage and free-wheeling diode voltage are also measured, using a differential probe P5205A. Except for the differential probe, the references of all the other probes are connected

internally together to the earth ground including coaxial cable. When using these probes at the same time, it must be ensured that all the reference terminals connect to the same electrical point.

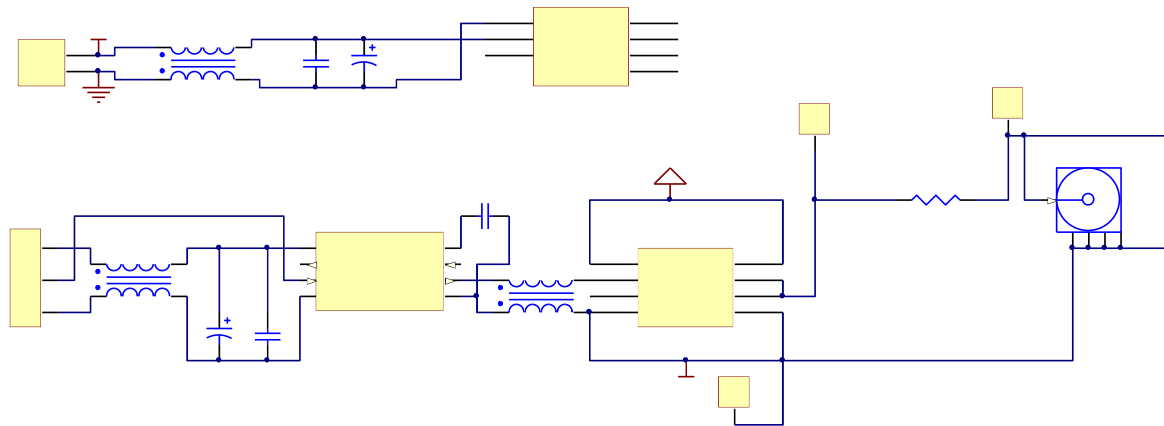


Figure 5.12. Gate drive circuit.

The input impedance of the voltage probe can be modeled as a capacitor of around 10 nF and a resistor of 10 MΩ in parallel. The ground lead of the voltage probe introduces stray inductance, which forms an LC resonant circuit with the input capacitor. If there is a step voltage applied at the probe, high frequency resonance can occur. Then the detected voltage is not the step voltage itself but the resonance at the capacitor. This phenomenon is obvious when measuring high dv/dt. For accurate voltage measurement, in this experiment, the grounding leads are removed, tip adaptors are used. When measuring gate voltage using P6139, a tip adaptor Tek 131 5031 00 is used, as shown in left picture of Figure 5.13. The high voltage probe has a different tip to BNC adaptor Tek 013 0291 01. Then a BNC jack is used on the PCB board, as shown in the right picture in Figure 5.13. The use of tip adaptor eliminates the grounding lead, which reduces the stray inductance in the probe.

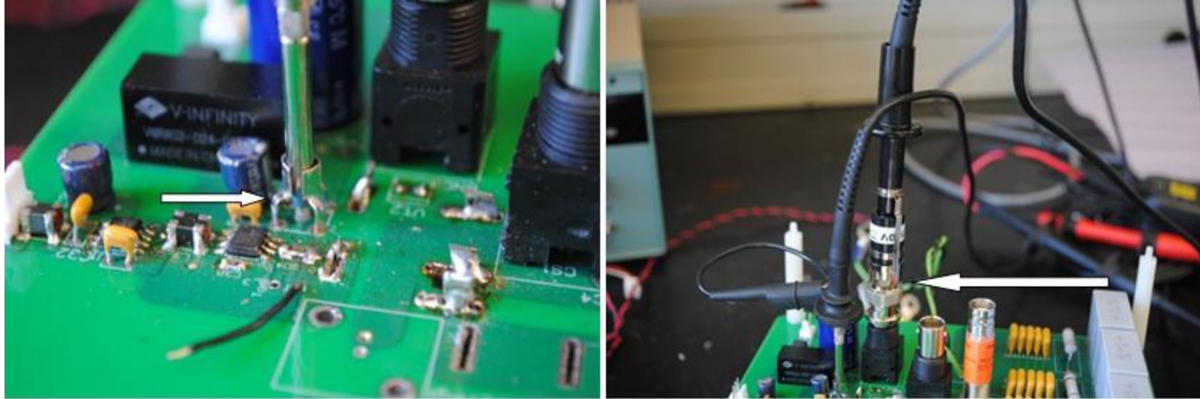


Figure 5.13. Reduced tip-to-ground loop using a probe-tip adaptor.

The equipment used in this experiment include a 600 V/ 10 A DC voltage supply from Magna to provide DC voltage; oscilloscope DPO4104 from Tektronix for current and voltage measurement; an arbitrary function generator 33522A from Agilent to generate two adjustable pulses; a power supply to provide 5 V for the isolator ADuM5240 and 24 V for the isolated DC to DC converter.

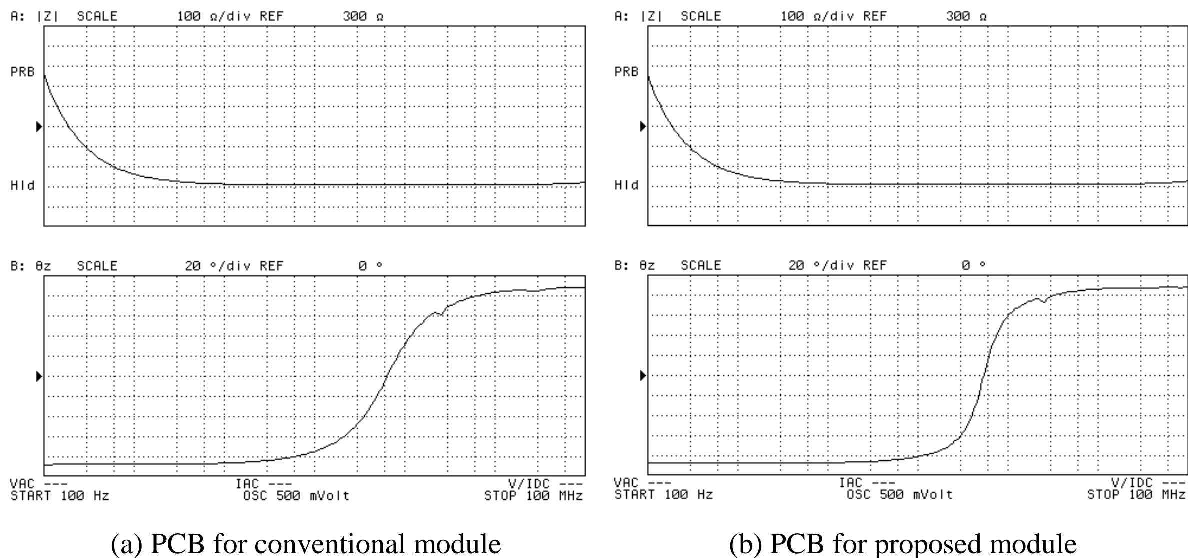
5.3.2 On Board Inductance Calibration

Two different DPT boards described above are fabricated since the footprints of the two modules are slightly different. The inductance inside the modules is tens of nano-Henry level, from the measurement of the inductance in section 5.1, the difference is around 10 nH. To compare the small difference, there should be a same base. In the commutation loop, the DC bus on the PCB board also contributes to the loop inductance. It should be ensured that the two boards have the same DC bus inductance.

The DC bus inductance is measured using an impedance analyzer. First, the electrolytic capacitor is detached. Second, the positive and negative leads of the module are shorted. Third, the load inductor is also removed. There are only the decoupling capacitors and DC bus stray inductance left in the loop. The loop is broken from one of the shunt resistors by

removing this resistor. The impedance is measured using an impedance analyzer.

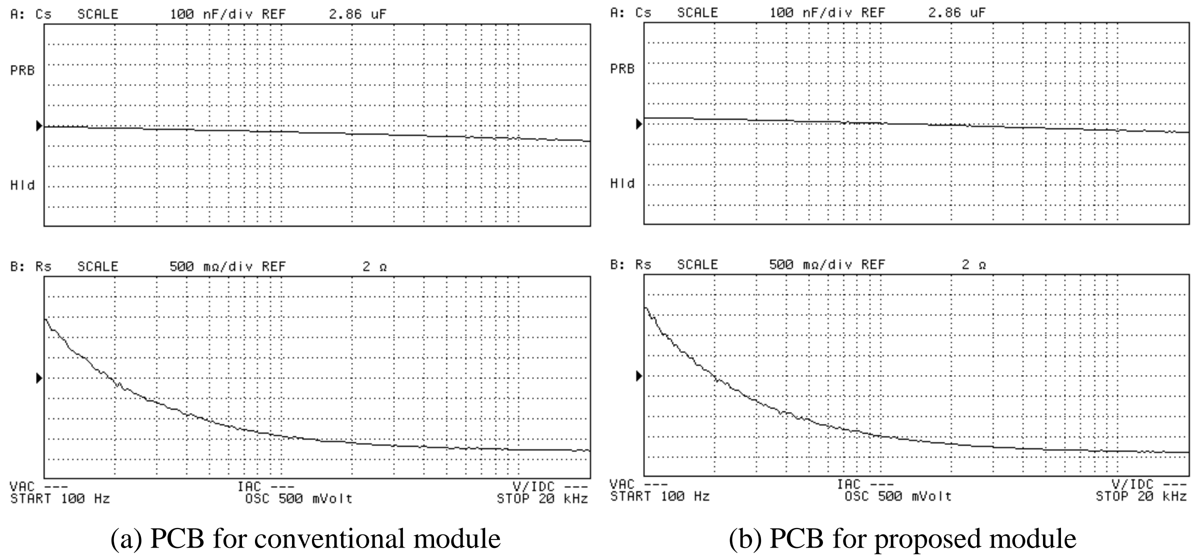
Figure 5.14 shows the amplitude and phase plot of the impedance from 100 Hz to 100 MHz. The left figure is the measurement result for the conventional module and the right figure is of the PCB for the proposed module. Both phase plots show that at low frequency the phase is around -90 degrees, which means that the DUT is capacitive, while in high frequency the phase is around 90 degrees, which means that the DUT is inductive. This is reasonable since the measured components are a series connection of the decoupling capacitors and stray inductance of the DC bus.



(a) PCB for conventional module (b) PCB for proposed module

Figure 5.14. Measurement result of the bus impedance.

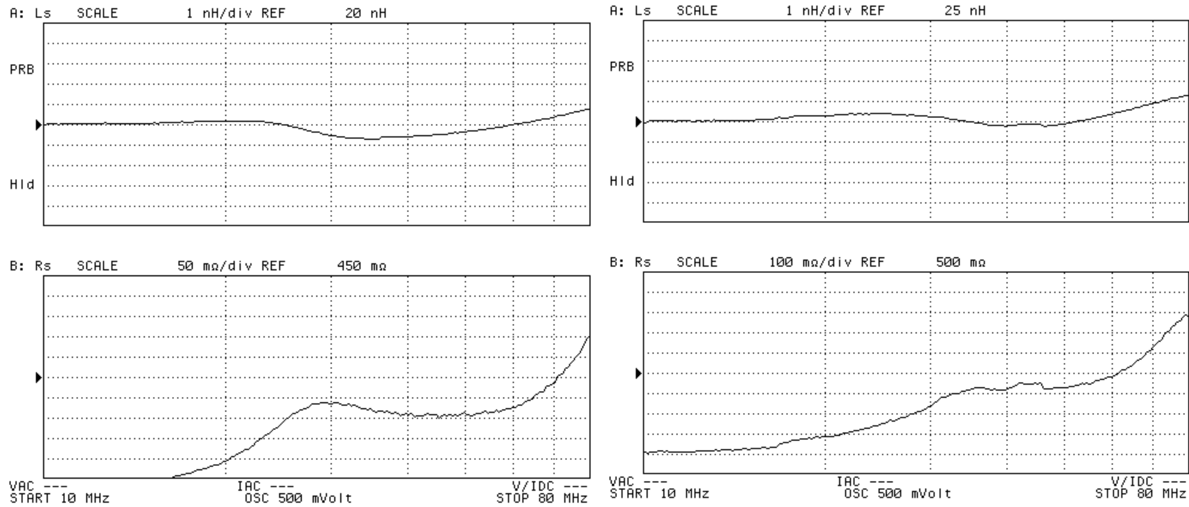
Figure 5.15 shows the measurement results in low frequency from 100 Hz to 20 kHz. From the previous phase plot, which is -90 degrees, we can figure out that the impedance in this range is capacitive, which means the capacitance plays the main role while the inductance can be ignored. The solid triangle shows the reference value which is 2.86 μF in both figures. The measured lines are very close to the reference value. This agrees with the actual decoupling capacitors used on the board.



(a) PCB for conventional module (b) PCB for proposed module

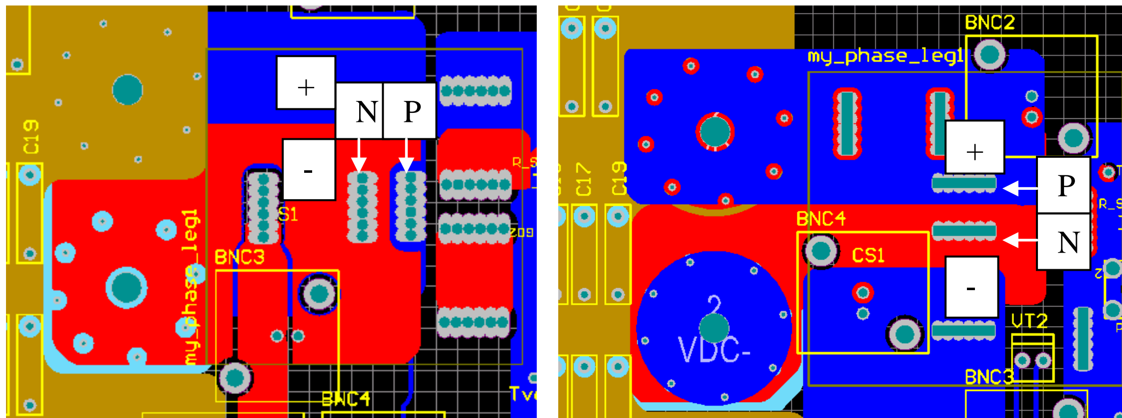
Figure 5.15. Measurement results of decoupling capacitance on board.

Figure 5.16 shows the measurement results in the frequency range of 10 MHz to 100 MHz. In this range, the stray inductance in the DC bus dominants the impedance. The stray inductance in the board for a conventional module is around 20 nH in the frequency range, while in the other board the inductance value is around 25 nH. Meanwhile, the layouts of the PCBs are investigated. Figure 5.17 shows the DC bus connection from the decoupling capacitor to the module. The reason that the left one has less stray inductance is that the bus is wider and the positive and negative buses are overlapped for the most part, the positive and negative connection in the right one is a little bit thinner and there is no overlap. It is known that the lamination structure can reduce inductance.



(a) PCB for conventional module (b) PCB for proposed module

Figure 5.16. Stray inductance measurement results of the PCB.



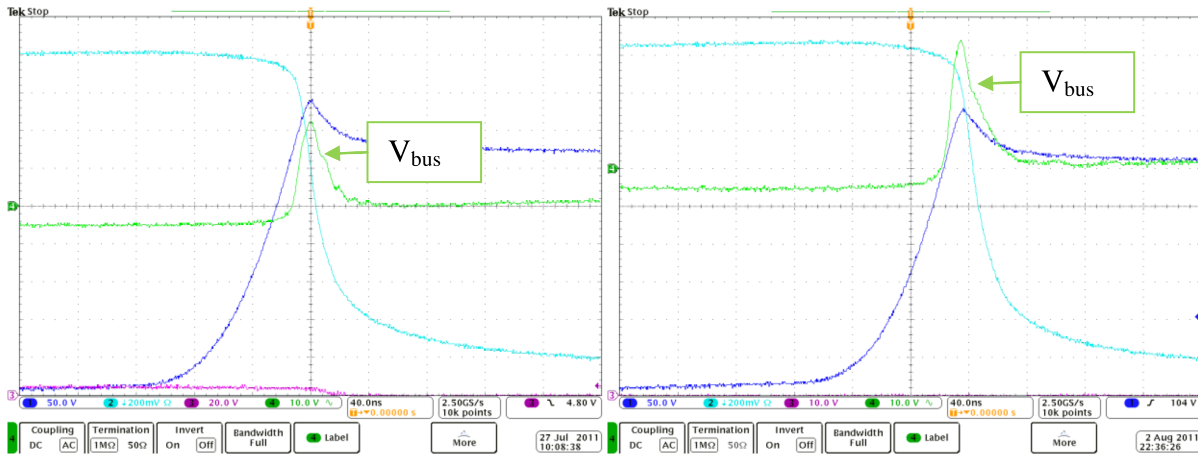
(a) PCB for conventional module (b) PCB for proposed module

Figure 5.17. Layout of DC bus in PCB.

This difference in the DC bus will compromise the improvement in the module inductance. For example, the stray inductance can cause voltage drop during turn off, and this voltage drop accumulates on the device. The voltage at the positive and negative buses of the power module as the points shown in Figure 5.17 is the DC voltage source plus voltage drop at bus. This voltage should be 300 V plus a spike during switching. This voltage is measured as shown in the green waveform in Figure 5.18. To enlarge the spike, AC coupling of the measurement mode is used. The voltage resolution is set at 10 V/division. From the

waveform we can see that in the PCB for the conventional module, the voltage spike on module terminal during turn off is around 29 V, while in the PCB for the proposed module, the voltage spike is around 39 V.

To ensure the same DC link inductance of the two boards, a short wire is added to the board with less inductance. After adding the short wire, the module terminal voltage is measured again as shown in Figure 5.19. The voltage drop at the DC link now is also 39 V, indicating the same stray inductance with the other board.



(a) PCB for conventional module (b) PCB for proposed module

Figure 5.18. Voltage on module terminals during turn off.

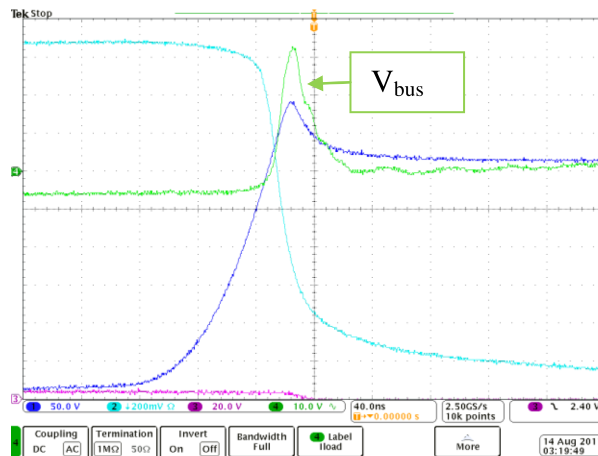


Figure 5.19. Voltage on module terminals during turn off after correction.

5.3.3 IGBT Die Voltage Measurement

Previously in this dissertation, any voltage measurement is from the terminals of the module or device as illustrated by V_{lead} in Figure 5.20. However, when comparing the voltage difference caused by parasitics inside the power module, measuring from the terminals can not serve the purpose. The reason is that V_{lead} does not take the voltage drop on l_3 and l_4 into account, but only the voltage on decoupling capacitors plus the voltage drop on l_1, l_2 and l_{esl}, while the purpose is to compare the difference of the voltage drop on l_1, l_2, l_3 and l_4. Therefore, the voltage that should be measured here is the true stress on the IGBT die, V_{die} as illustrated in Figure 5.20.

To access the die, probe station system with microscope is used. Basically, it has long and thin pin probes to touch the die to obtain the signal, and then the signal can be connected to an oscilloscope or other measuring equipment. However, this only works for static characteristic measurement but not for transient characteristic, because the probe introduces a large stray inductance into the measurement loop, which will affect the measurement accuracy if the signal is high frequency.

A new method is proposed to measure the die voltage. Two wires are attached to the collector and emitter side of the die. Then the wires are twisted and connected to the board where the BNC connector and adapter are used to connect to the oscilloscope. Specifically, one wire is soldered to the DBC near the IGBT die under test to get the collector signal as shown at point A in the left figure of Figure 5.21. Since the top emitter pad cannot be soldered, the other wire is soldered to the auxiliary emitter for the gate signal, as shown of at point B. Attention should be paid here that there are two groups of bonding wires that connect out from the emitter side of the die, power emitter and auxiliary emitter. The gate

drive current is very small, point B can represent the voltage of the IGBT emitter, while there is some voltage drop on the wires where the power current goes through.

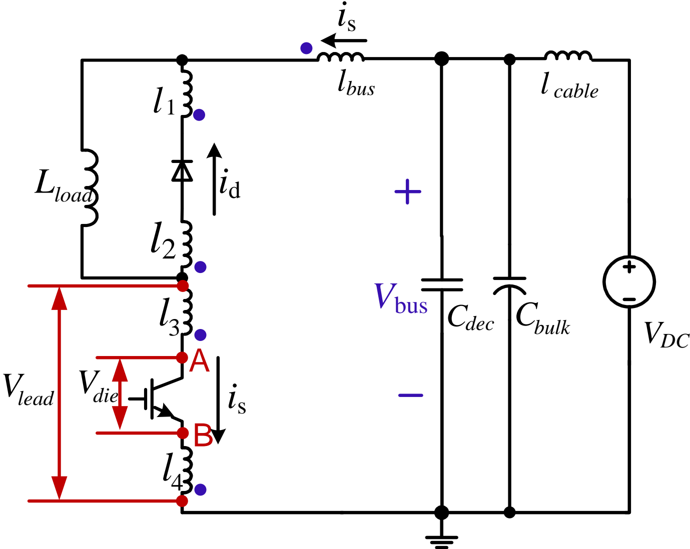


Figure 5.20. Illustration of measuring points.

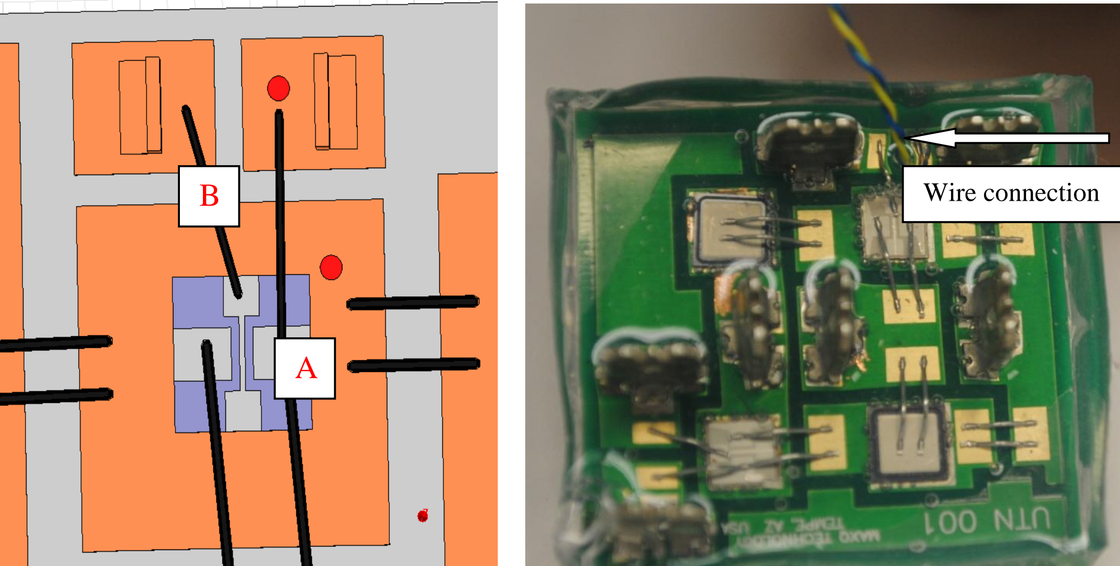
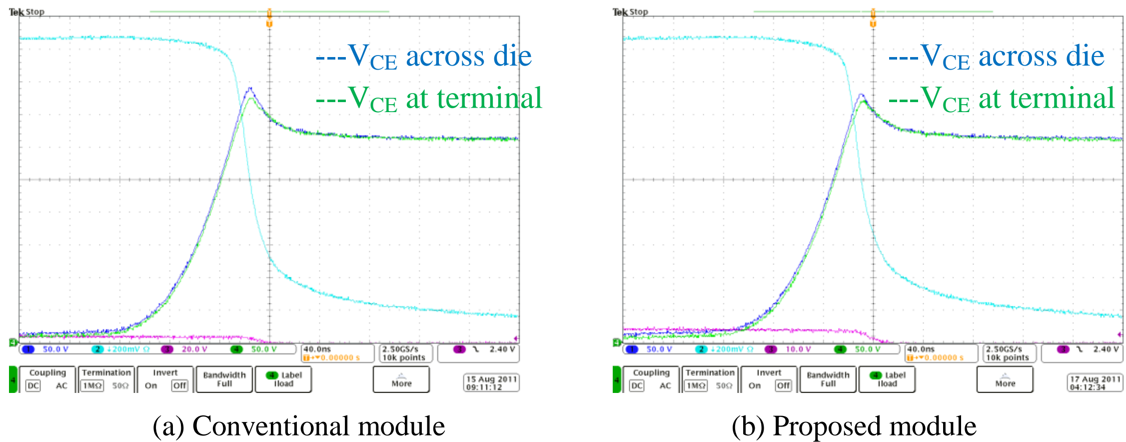


Figure 5.21. Module with wire connection from IGBT die.

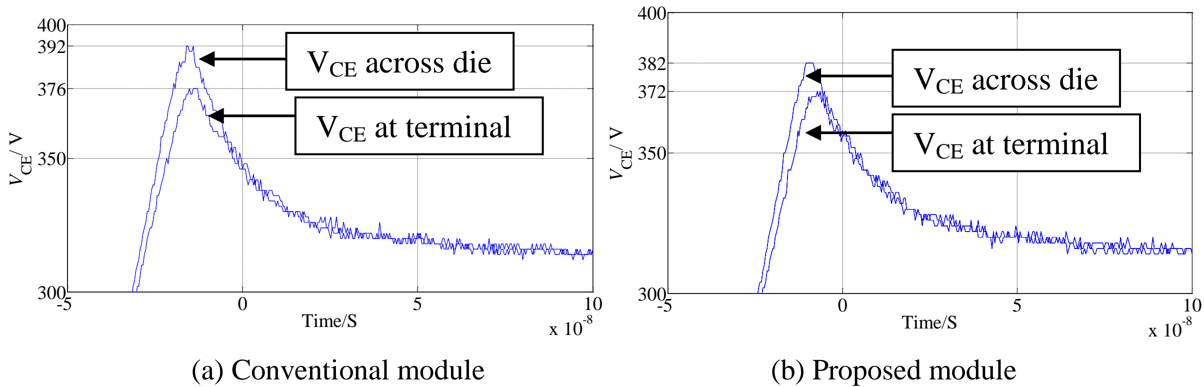
Using the method described above, the voltage is measured across the IGBT die. At the same time, voltage across the terminals is also measured as shown in Figure 5.22. The blue waveform is measured using the wires, the green one is measured from the terminal. There is

some difference between the two waveforms. The voltage overshoot is enlarged as shown in Figure 5.23. Take the measurement for the conventional module as an example. The voltage across the IGBT die is 392 V, while the voltage at the terminal is 376 V, which indicates that there is 16 V voltage drop due to the module stray inductance l_3 and l_4. It is the same for the proposed module measurement as shown in Figure 5.23(b). Since the module stray inductance in the proposed module is reduced, the difference is only 10 V.



(a) Conventional module (b) Proposed module

Figure 5.22. Turn off voltage of IGBT at different measuring points.



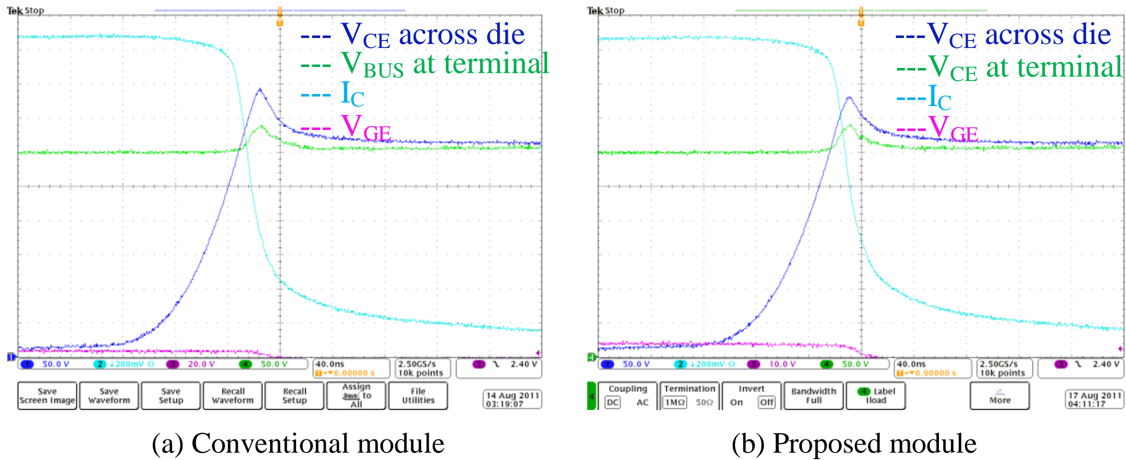
(a) Conventional module (b) Proposed module

Figure 5.23. Enlarged waveform of turn off voltage of IGBT at different measuring points.

5.3.4 Experimental Results

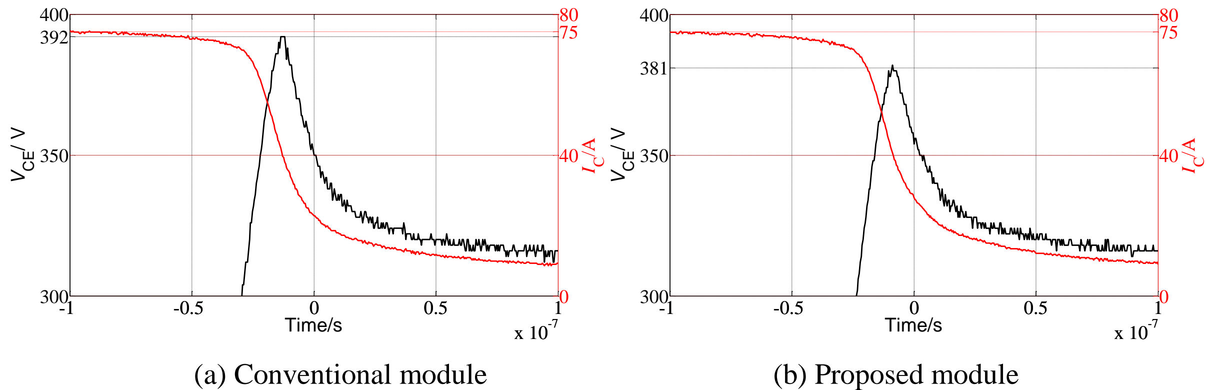
The turn off current and voltage waveforms for both conventional module and proposed module are shown in Figure 5.24. At the test condition 300 V, 75 A, and room temperature,

the overshoot voltage in the conventional module is higher than that in the proposed module. The current and overshoot voltage are enlarged in Figure 5.25. It is clear in these two figures that the overshoot voltage is 92 V and 81 V respectively.



(a) Conventional module (b) Proposed module

Figure 5.24. Turn off voltage and current.



(a) Conventional module (b) Proposed module

Figure 5.25. Close-up view for voltage overshoot during turn off.

The turn off current slope is also calculated as shown in Figure 5.26. In both cases, the current slew rate is around 2.16 A/*n*s. From the slop of the turn off current and the overshoot voltage, the stray inductance can be calculated using the following equation:

$$L_{stray}=\Delta V/(di_C/dt)$$

The calculated results from the experiments are 37.5 nH for the proposed module and 42.6 nH for the conventional module. It should be noted that the inductance calculated using

the experimental data includes both the DC bus stray inductance and the module stray inductance. The simulated values and the measured values for the sum of the two parts are listed in Table 5.3 for comparison.

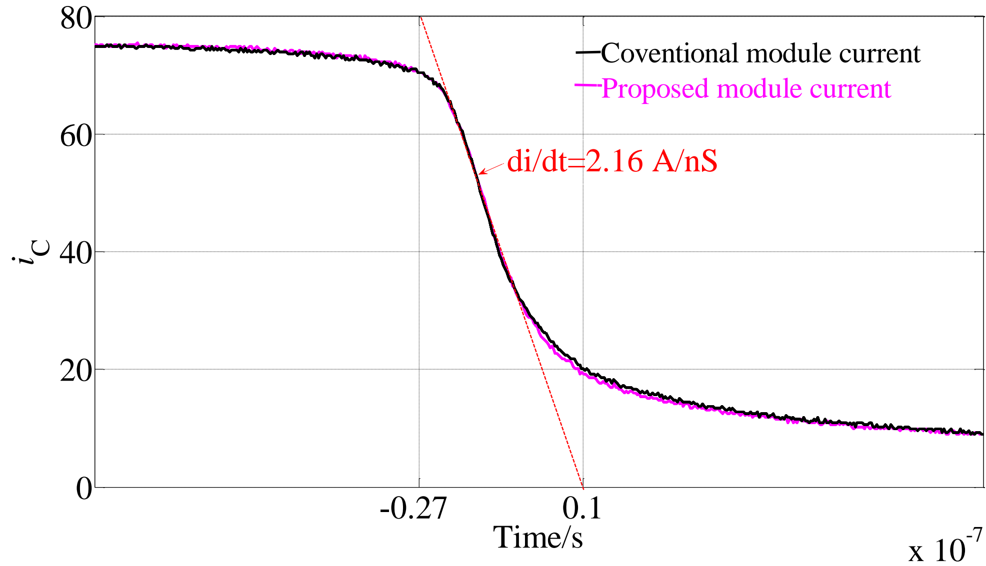


Figure 5.26. Slope of the turn off current.

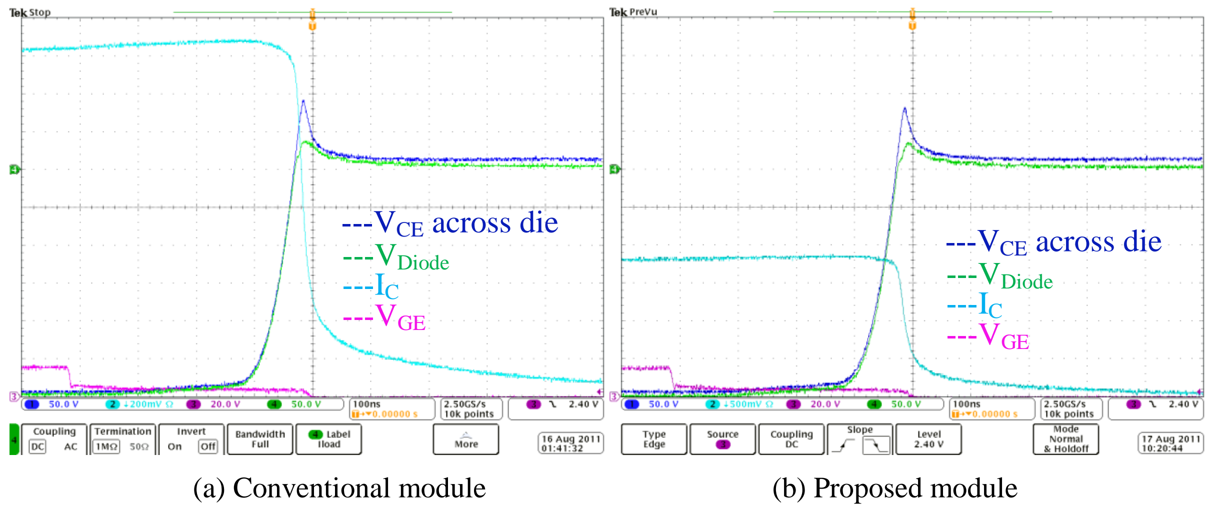
Table 5.3 Comparison of measured and calculated inductance.

(nH)	Simulated value	Measured	Calculated from experiment
Conventional	28+18.5=46.5	25+21=46	42.6
Proposed	28+8.5=36.5	25+6.5=31.5	37.5

During turn on, two physical processes occur in sequence. First, the space charge stored in the depletion region because of the large reverse-bias voltage is removed by the forward current. Then the excess-carrier distribution in the drift region grows. As the forward current grows in time, there is an increasingly large voltage drop across the drift region, since there is no conductivity modulation of the region until the space charge layer is discharged to its thermal equilibrium value. This voltage drop is shown as the green waveform in Figure 5.27. It is around 40 V. This voltage is measured at the module terminals; therefore, it also

includes the voltage drop due to the module stray inductance. It is difficult to separate the two parts.

The voltage drop across the DC bus stray inductance, diode dice, and the module stray inductance compose the turn off overshoot voltage across the IGBT die.



(a) Conventional module (b) Proposed module

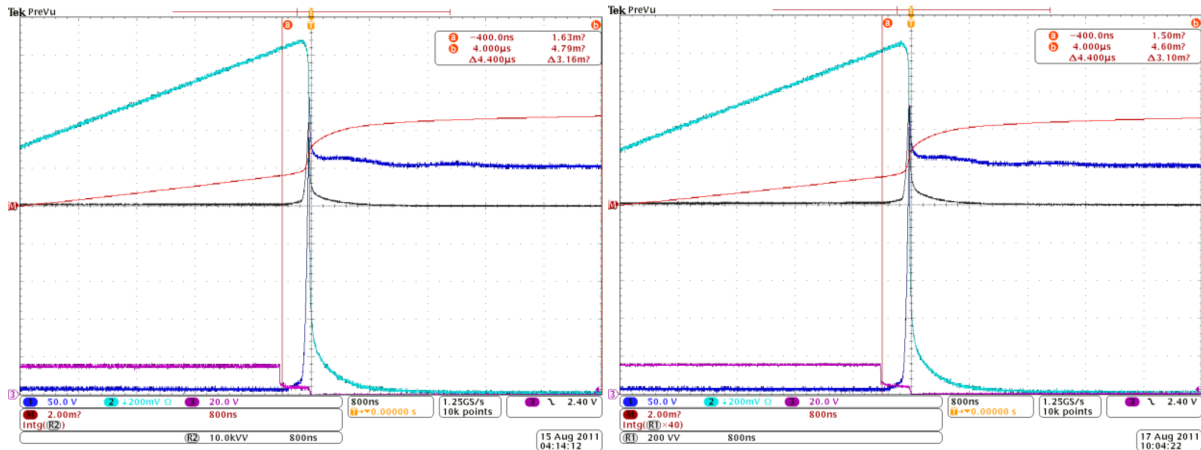
Figure 5.27. Voltage across diode.

The switching loss is calculated using the math function of the oscilloscope. To get an accurate measurement of the loss, the synchronization of the voltage (channel one) and current signal (channel 2) is necessary. The propagation delay of the high voltage probe P5100 can be detected automatically by the scope, which is 14.9 ns. The current is converted via a shunt resistor to voltage and then connected to the oscilloscope through a coaxial cable. The delay on the shunt resistor is neglected. The delay of the coaxial cable is measured manually. By connecting both channels to the probe compensation output and zooming out of the rising or falling edge, the difference of the delay can be determined. In this case, the propagation delay of the current channel is 7.4 ns.

From the data sheet of IGBT and diode, the turn off loss is calculated using the following equation:

$$E_{off} = \int_{t3}^{t4} (i_c(t) \times v_{CE}(t))dt$$

The start time for the integration is defined as the time when the gate voltage has reached 10% of its final value. The integration end is when the current or voltage reaches zero. Here for turn off, it is 4 μs, and for turn on it is 800 ns. First, the voltage and current are multiplied using math function, and saved to R1. Then R1 signal is integrated as the red waveform in Figure 5.28. The energy increase from the cursor 'a' to cursor 'b' is the turn off loss. In the conventional module it is 3.16 mJ and in the proposed module it is 3.10 mJ.



(a) Conventional module (b) Proposed module

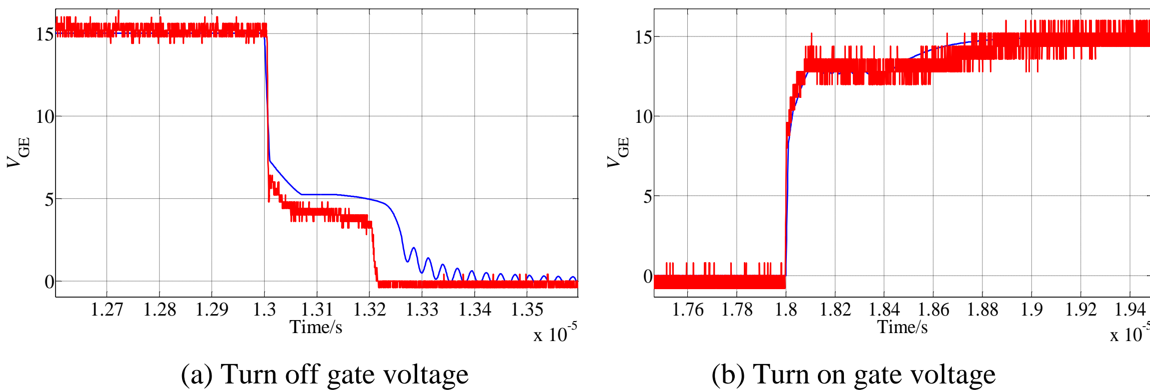
Figure 5.28. Turn off loss calculation.

5.3.5 Comparison of Experiment with Simulation results

The experiment result and the simulation using Saber are compared in Figure 5.29 to Figure 5.31. The turn on and turn off delay match with each other. The turn on and turn off voltage slops, and current slops also match, as well as the reverse recovery current. However, there are more oscillations in the simulation. This could be caused by the limitations of the modeling tool.

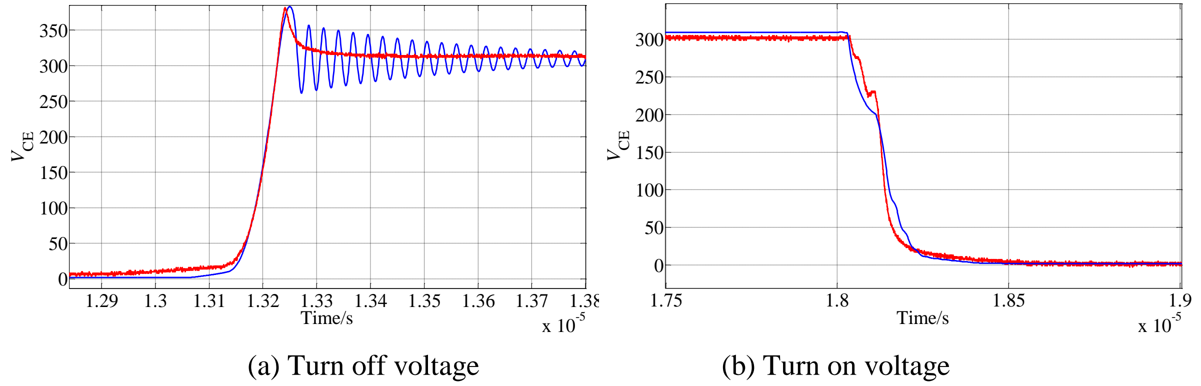
For diode, the turn on process is simplified. In fact, there is an overshoot voltage across the diode due to the conductivity modulation is not built while the current increasing. However, this phenomenon is not modeled in Saber model architect.

For IGBT, the capacitances are modeled as *C*ce, *C*gc and *C*ge from the datasheet information of *C*ies, *C*oes and *C*res as shown in Figure 5.32 (b). While the capacitance *C*gc is composed of the series connection of implicit emitter-base capacitance and gate-drain capacitance, *C*ce is composed of the combination of the implicit emitter-base capacitance, drain source depletion capacitance and collector emitter redistribution capacitance, as shown in Figure 5.32 [51]. The other difference of the Saber model tool is that the current is MOSFET current plus a tail current, while the real current in an IGBT is the bipolar junction transistor current plus the parasitic MOSFET current.



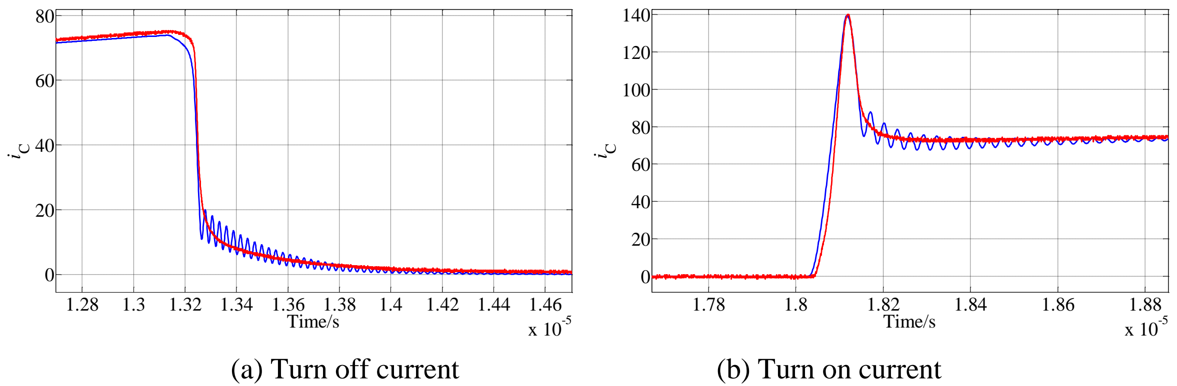
(a) Turn off gate voltage (b) Turn on gate voltage

Figure 5.29. Comparison of experiment and simulation of gate voltage (red is experiment; blue is simulation).



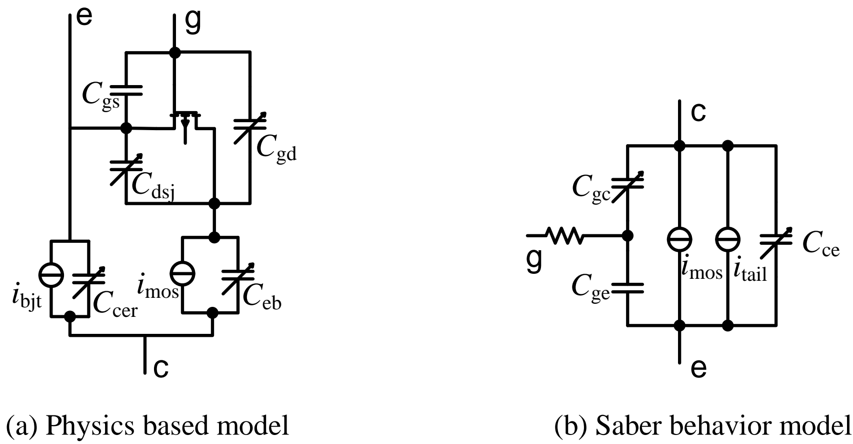
(a) Turn off voltage (b) Turn on voltage

Figure 5.30. Comparison of experiment and simulation of IGBT voltage.



(a) Turn off current (b) Turn on current

Figure 5.31. Comparison of experiment and simulation of IGBT current.



(a) Physics based model (b) Saber behavior model

Figure 5.32. Analog circuit representation of IGBT model.

5.4 Summary

This chapter focuses on measurement of the stray inductance inside the power module

and the experimental work on characterizing the switching performance of the power module. Since the package stray inductance is relatively small, a precision impedance analyzer model 4294A from Agilent is used for measurement. To get a conducting commutation loop, some modules without dice on them are fabricated. The aluminum wires are directly bonded on the DBC to represent the conducting dice. The measurement results of the stray inductance agree with the simulation results; the commutation loop inductances in the proposed layout design are around 50% of them in the conventional layout. Moreover, power modules with dice are also fabricated. The static characterization of the devices is done.

The experimental setup for DPT was built. Several methods are used to improve the accuracy of the measurement. To measure the voltage drop on the stray inductance, two wires were attached as close as possible to the collector and emitter of the IGBT die. Voltage was measured at both across die and across module terminal. There was more than 10 V difference for the two measurements, which shows the effectiveness of this method. The experimental results show 11 V less overshoot voltage during IGBT turn off in the proposed module than in the conventional module, which benefits from the reduction of the module stray inductance.

6 Utilizing Novel Switching Cells in Multichip IGBT Module

In mid or high power areas, such as HEVs, many IGBT and diode chips are connected in parallel inside the module to increase the current capability. In the package of multichip IGBT modules, in addition to reducing loop stray inductance, another concern is the mismatch of the parameters of the two paralleled loops. More uniform parasitics and die characteristic in the module offers more even distribution of current and commutation voltage conditions between chips, which help to keep the components inside the module at similar temperatures and enables better use of silicon and minimizes potential early-wear out failures due to degradation over module lifetime [45].

In this chapter, power modules with two devices in parallel are studied. A conventional layout is designed according to a commercial module. Then, a multichip module using the concept of P-cell and N-cell is designed. The parasitics are extracted for both modules. Saber simulation is conducted for electrical characteristics under different parasitics.

6.1 Layout Design of Multichip Power Modules Based on Novel Switching Cells

Figure 6.1 shows a commercial module from a hybrid electric vehicle [53]. The left part is one phase leg of a motor inverter. The layout of the module is indicated in the figure. Two IGBTs and two diodes are in parallel in both the upper cell and the lower cell. According to this layout, a similar one is drawn using Q3D Extractor, as shown in Figure 6.2. The anti-paralleled IGBT and diode form the upper cell and the lower cell. The upper cell is in one piece of the DBC, while the lower cell is at another DBC. The IGBT and diode dimension is from the datasheet of ABB dice.

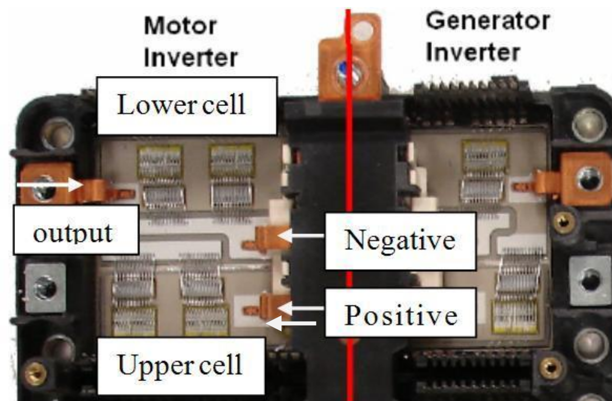


Figure 6.1. A commercial inverter IPM.

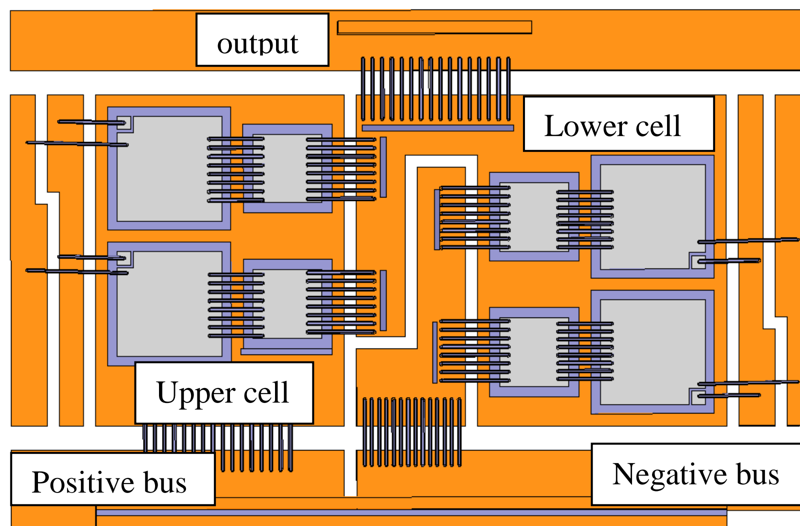


Figure 6.2. Conventional layout of an IGBT module with paralleled dice.

The parasitic model of the multichip power module is shown in Figure 6.3. The parasitic model is based on the physical layout. The parasitic inductance is extracted piece by piece. The commutation loop inductance can be calculated by adding them together, the smallest loop has 24 nH, and largest loop has 25.4 nH. The mismatch of the inductance is 1.4 nH. The parasitic resistance is also extracted. Since the resistance does not affect transient behavior much, while it affects the steady state current distribution, the resistance is extracted under the condition of DC excitation. The resistances of the paralleled upper branch are 1.0 mΩ and 1.1 mΩ; while in the two lower branches, they are 0.9 mΩ and 1.0 mΩ, respectively.

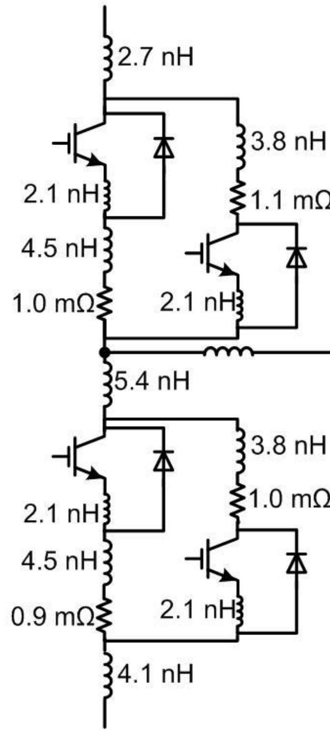


Figure 6.3. Parasitics extraction of the conventional multichip module.

Another layout utilizing P-cell and N-cell is also designed as shown in Figure 6.4. In this design, the commutating IGBTs and diodes, identified as P-cell or N-cell are arranged together. The parasitics is modeled differently from the conventional module, as shown in Figure 6.5. In this arrangement, the stray inductance has been reduced to some extent. In P-cell the loop inductances are 14.2 nH and 24.3 nH respectively, in N-cell, the loop inductances are 21.4 nH and 16.5 nH respectively. The DC resistance is also extracted and reflected in the model. It is worth to point out that the resistance is between the output and positive or negative bus. For example, if the IGBTs in P-cell are conducting, the paths are shown in Figure 6.4 as the white and black lines. From the layout, it can be seen that the two conducting paths have similar length. Therefore, the resistance in the paralleled branches is similar, which is around 1 mΩ.

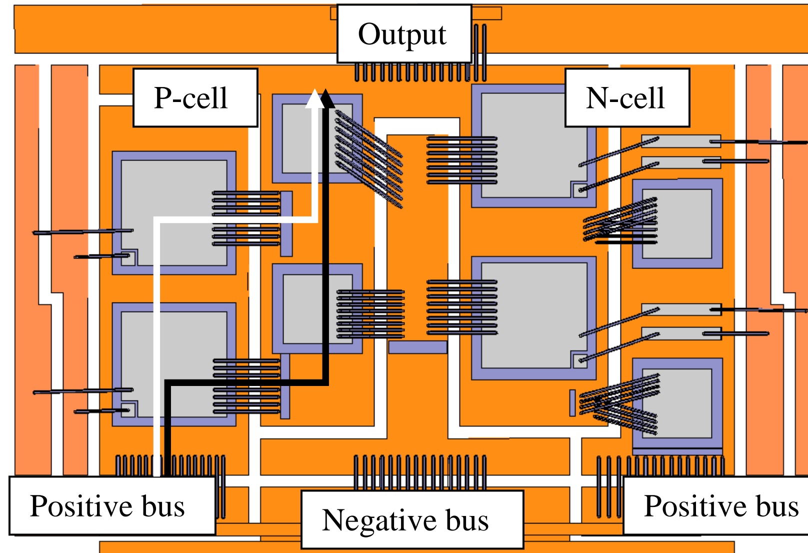


Figure 6.4. Layout design of a paralleled IGBT module using novel switching cells.

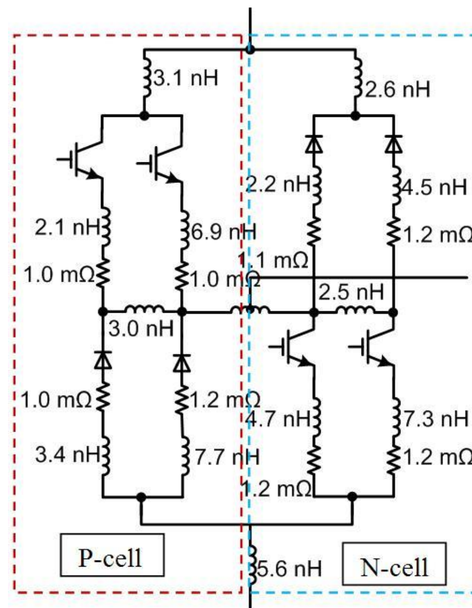


Figure 6.5. Parasitics extraction of the conventional multichip module.

By comparing the two layouts, we can conclude that, in general, the proposed method has short commutation loops for some branches, however, the length of each paralleled loop is different, this creates inductance mismatch. The mismatch can become serious as the paralleled branches increase. The conventional layout has similar loop length for each parallel loop, although the stray inductance value is at the level of the largest in the proposed

layout. As to the DC resistance, the two layouts have similar values, and there is no mismatch for both designs. The effect during the transient activity is studied in the next section.

6.2 Switching Characteristic of Multichip Power Module

To study the switching behavior of the multichip modules under different parasitics, DPT with detailed module parasitics is built in Synopsys Saber. The simulation condition is listed in Table 6.1.

Table 6.1. Test Condition of DPT

Parameters	Values
DC voltage	300 V
Testing current	150 A
Load inductor	47 μH

The transient voltage and current on the IGBTs and diodes are shown in Figure 6.6-Figure 6.9. In each figure, there are four waveforms, which are the two paralleled device in two layouts. The green and orange lines are from the conventional design, and the blue and purple lines are for proposed layout. The turn off voltage on the IGBTs are shown in Figure 6.6. The overshoot voltage is higher in the conventional layout. The reason is that there is some common stray inductance between the upper and lower cell, the whole current 150 A flows through this part, and so the voltage drop is higher. While in the proposed layout, the two paralleled paths and their parasitics are relatively separated. The turn off voltage on the two devices of the proposed module is different, which is caused by the mismatch of the parasitic inductance of the two loops. Although it is not serious, it might cause loss mismatch in the long run. This compromises the benefit of the proposed layout.

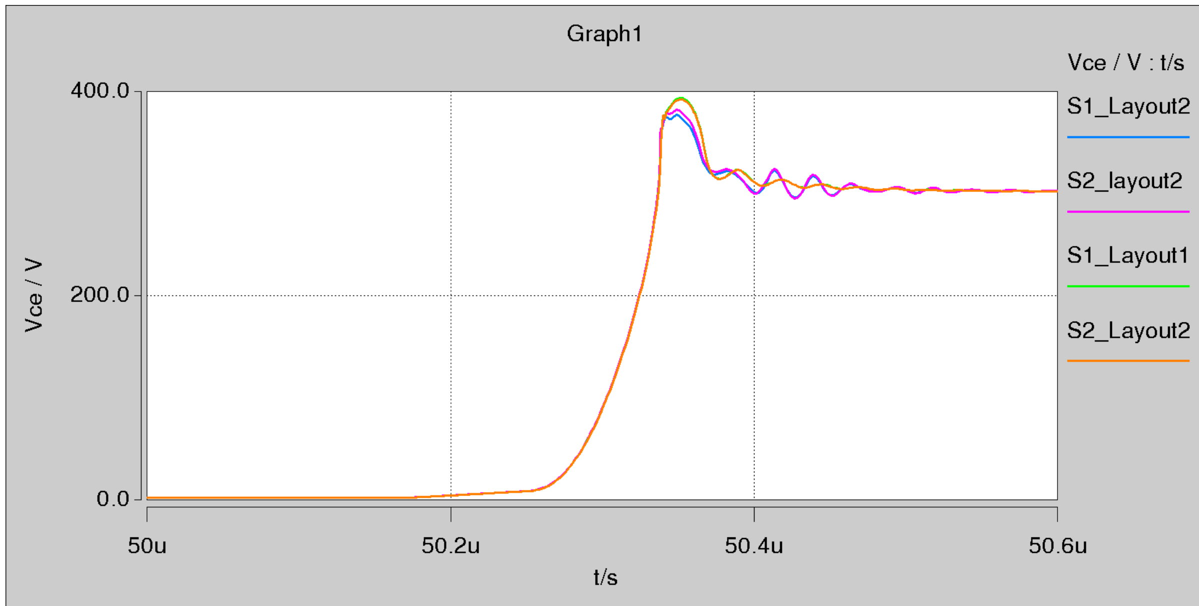


Figure 6.6. Turn off voltage of IGBTs.

The turn on current of the IGBTs is shown in Figure 6.7. The current peak due to the reverse recovery is higher and the oscillation after turn on is more severe in the conventional module. However, as expected there is some mismatch for the transient current in the proposed module.

The turn on current of the diodes is shown in Figure 6.8. It can be seen that the diode current is significantly affected by the stray inductance. Therefore, the mismatch between the two devices in the proposed layout is around 25 A. Since the two paralleled loops in the conventional module are not identical, there is also some mismatch in this module. The turn off current of the diodes in Figure 6.9 also show the same result that the mismatch in the proposed module is higher.

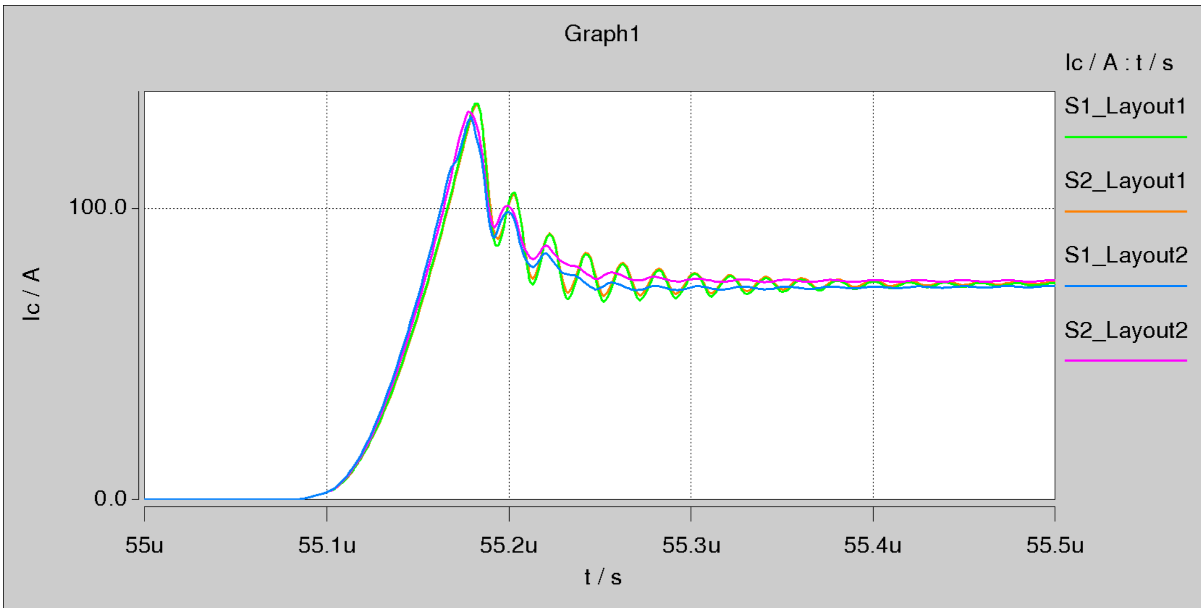


Figure 6.7. Turn on current of IGBTs.

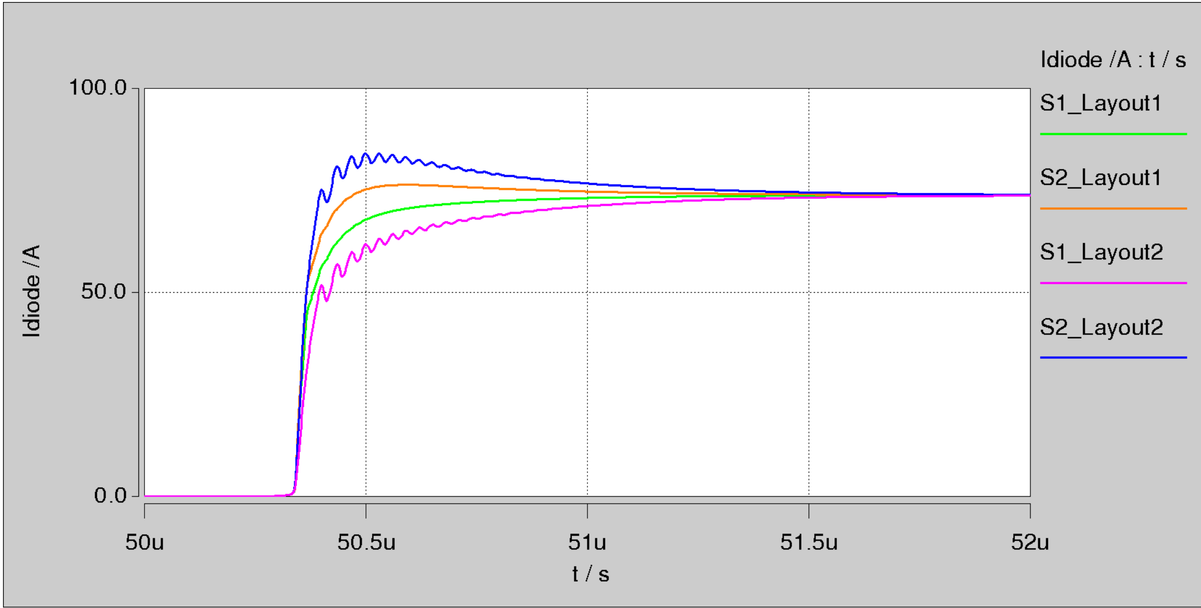


Figure 6.8. Turn on current of diodes.

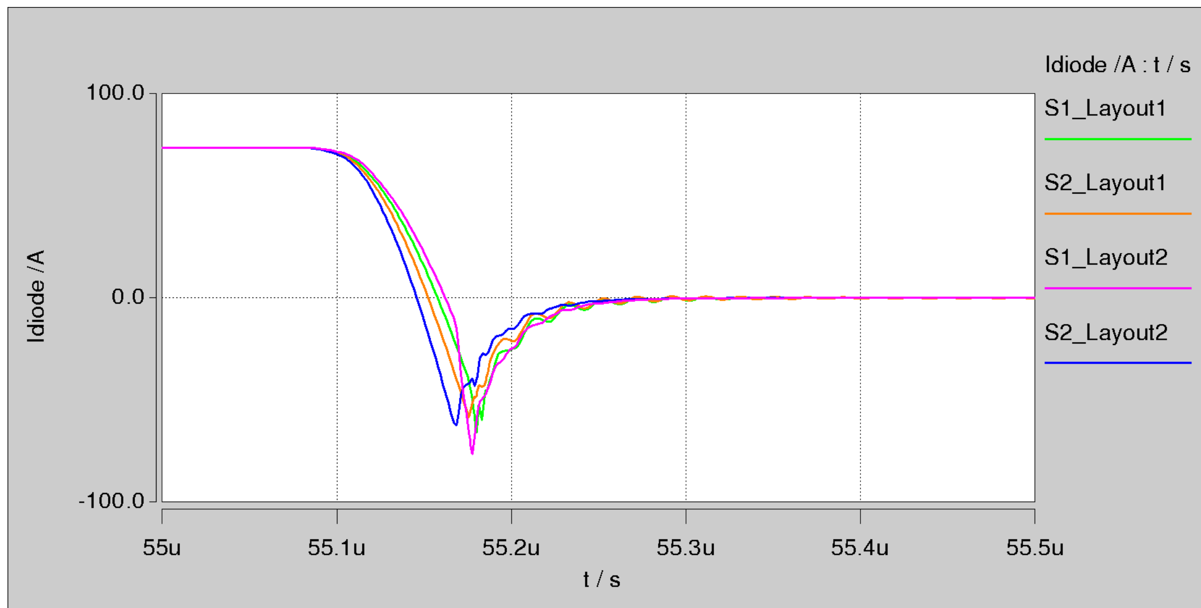


Figure 6.9. Turn off current of diodes.

6.3 Measurement of the Parasitics in the Multichip Power Modules

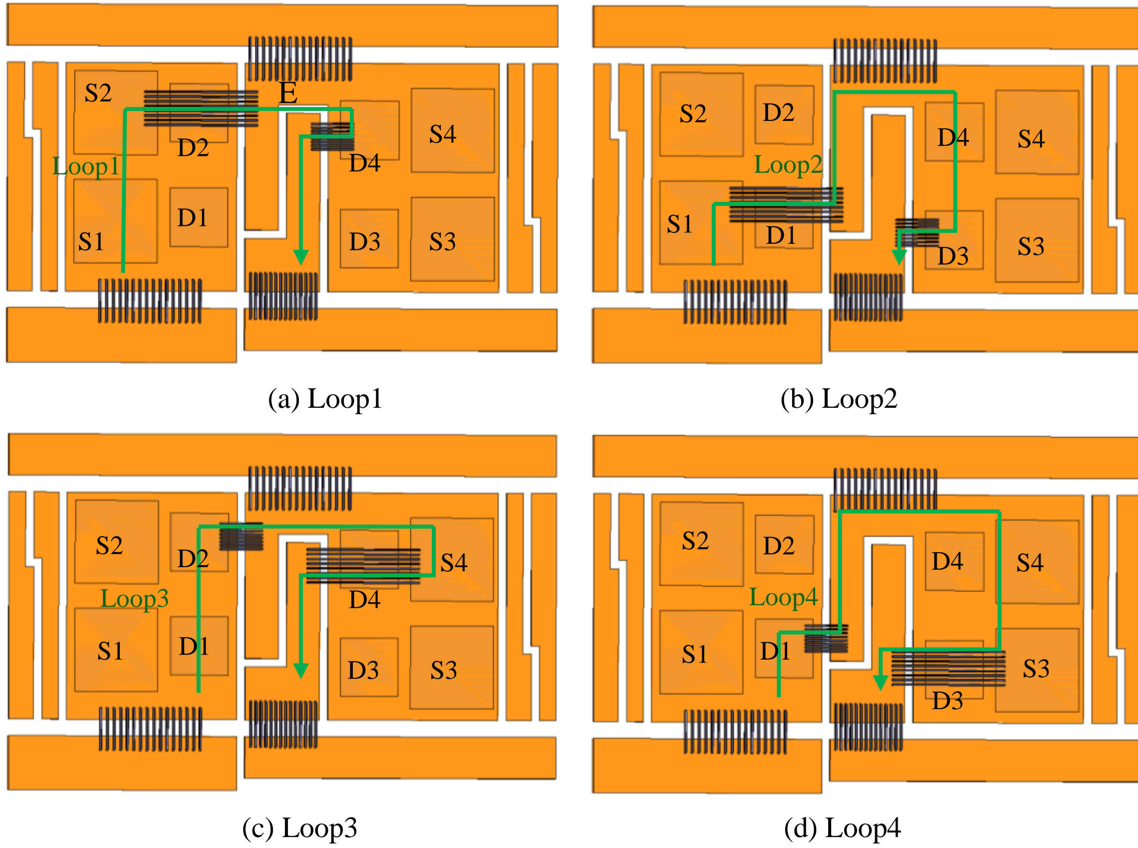
Since the IGBT is a normally off device and the diode does not conduct when applying small signal, the measurement is done by removing the devices from the substrate and bonding the wires on the DBC trace, in a pattern as discussed in the section on measuring the single chip module stray inductance in chapter 5.

Figure 6.10 shows different commutation loops in the conventional layout design. To ease the measurement, the bus bars are removed and only the substrate inductance is taken into account. It should be mentioned that the identified loops are not exactly the current path. For example, in Figure 6.10 (a), the current which goes through IGBT A, does not exactly pass diode B. It would be more accurate to model the module inductance as shown in Figure 6.3, however, it is not realistic to measure the stray inductance part to part in practice. The loop in Figure 6.10, somehow, can represent the inductances in Figure 6.3 added together. Figure 6.10 (a) and (b) show the two paralleled paths loop1 and loop2 that are formed by

devices A, B and C, D. Figure 6.10(c) and (d) show the other two paralleled loops loop3 and loop4.

Figure 6.11 shows the different loops in the proposed layout design. Figure 6.11(a), (b), (c) and (d) represent the four commutation loops respectively. It is obvious that in this design the two paralleled loops, for example loop1 in Figure 6.11(a) and loop2 in Figure 6.11(b), have different covered areas, and therefore the stray inductance for the two loops is different. It is the same thing for the two paralleled loops in N-cell as shown in Figure 6.11(c) and (d).

The two designed substrate patterns are etched and the wires are bonded as Figure 6.10 and Figure 6.11 for measurement. Figure 6.12 shows loop1 of the conventional design, and Figure 6.13 shows the loop1 and the loop4. The measurement tool is a precision impedance analyzer 4294A with pin probe 42941a. The measurement frequency is 10 MHz to 100 MHz. Some of the measurement results are shown in Figure 6.14. The two paralleled loops in the conventional layout are around 22.2 nH and 20.1 nH, while the inductance in the proposed layout are 18.6 nH and 12.7 nH. The detailed simulation and measured inductance are listed in Table 6.2.



(a) Loop1 (b) Loop2

(c) Loop3 (d) Loop4

Figure 6.10. Commutation loops in the conventional layout.

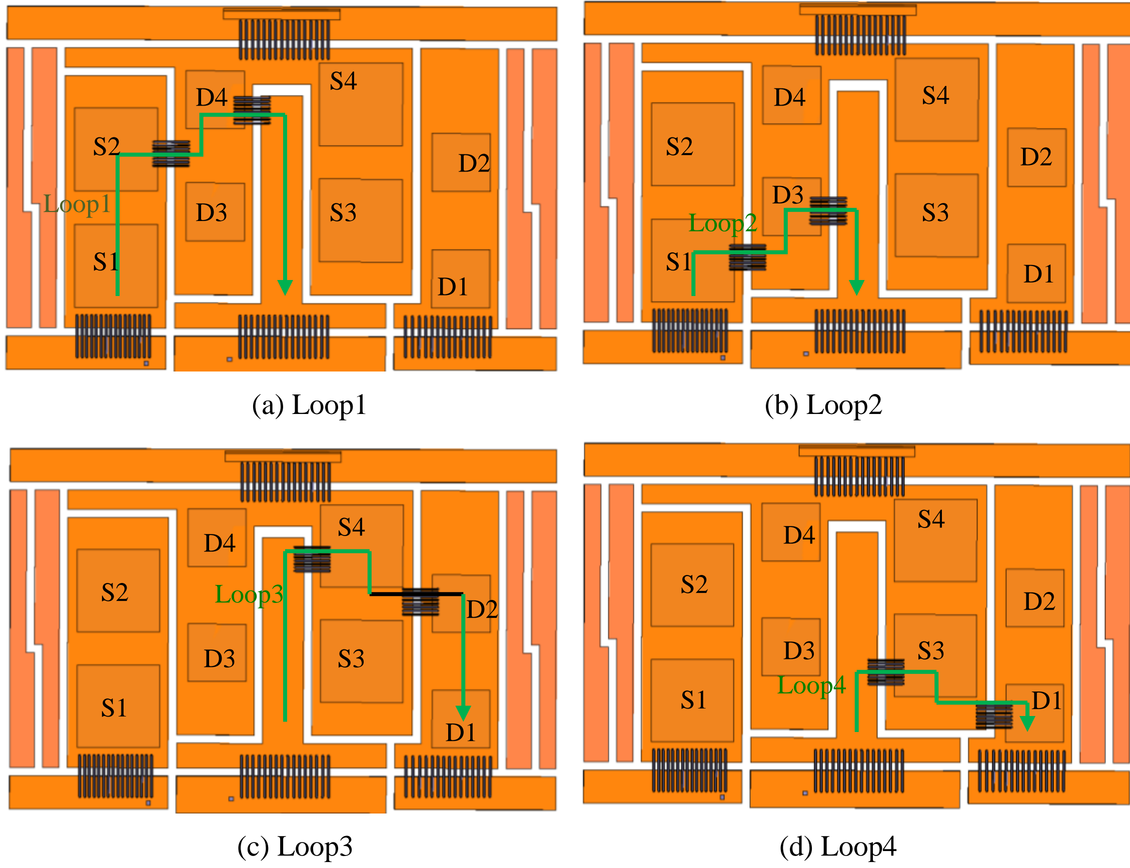


Figure 6.11. Commutation loops in the proposed layout.

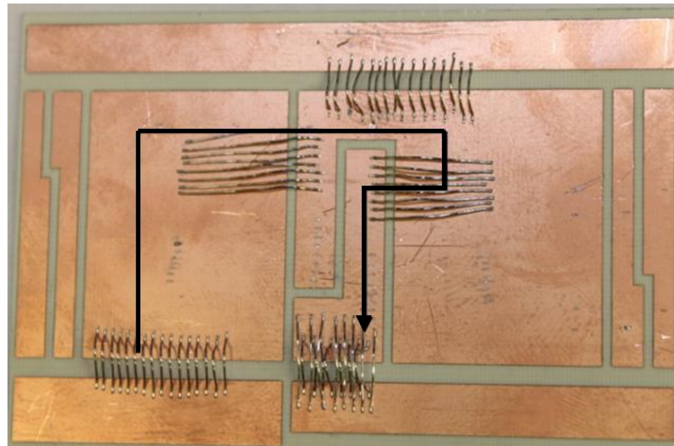


Figure 6.12. Fabricated commutation loops in the conventional layout.

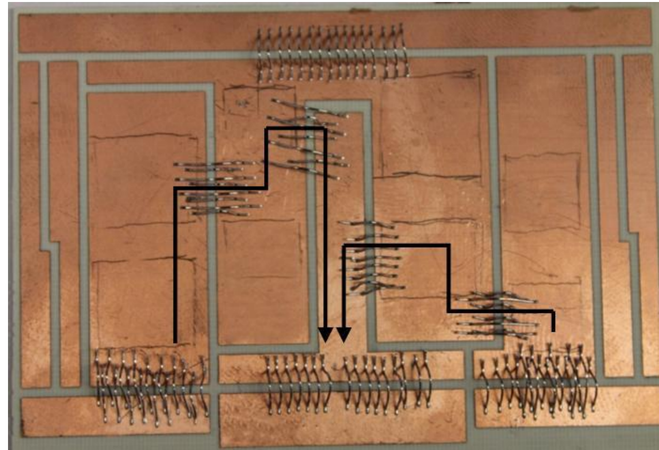
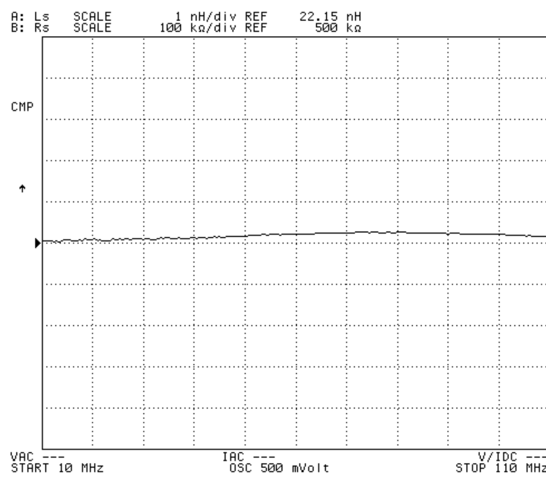
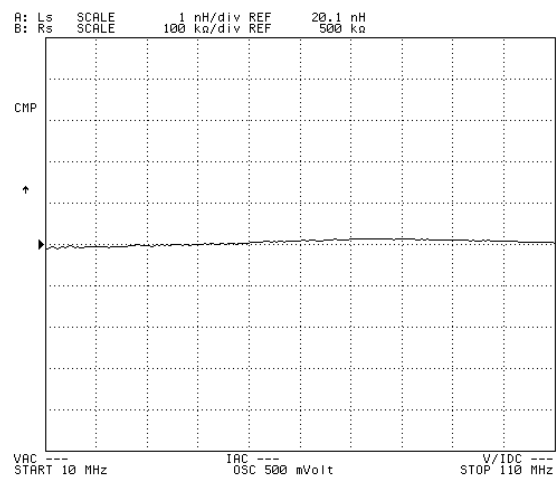


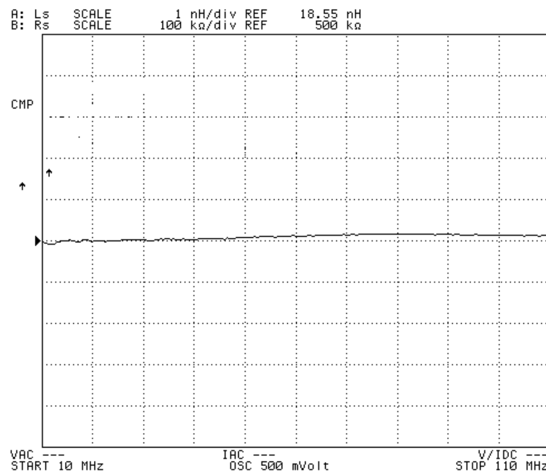
Figure 6.13. Fabricated commutation loops in the proposed layout.



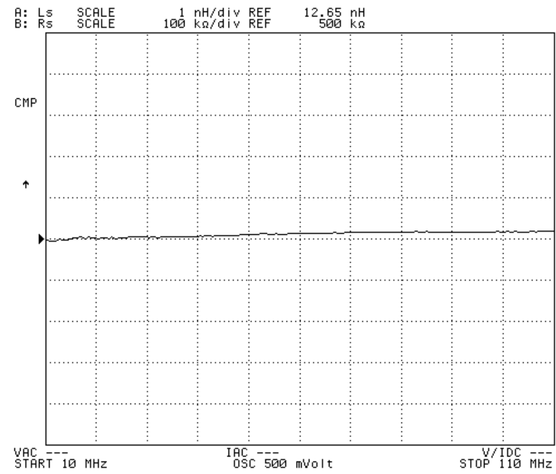
(a) Loop1 in conventional design



(b) Loop2 in conventional design



(c) Loop1 in proposed design



(d) Loop2 in proposed design

Figure 6.14. Stray inductance measurement results.

Table 6.2. Comparison of the simulation and measurement results.

	Conventional Layout (nH)		Proposed Layout (nH)	
	Simulation	Measurement	Simulation	Measurement
Loop1	23.4	22.2	21.8	18.6
Loop2	21.6	20.1	13.0	11.8
Loop3	21.3	19.8	20.5	17.9
Loop4	22.0	20.2	13.5	12.7

6.4 Summary

In this chapter, the novel switching cell concept is applied to a multichip module. The proposed layout and a conventional layout are designed in Q3D extractor. Under this layout design, the DC buses are arranged at one side of the module, this causes the proposed layout to have a disadvantage of uneven loop inductance. Although the loop inductance can be reduced, the effect is not significant. The mismatch in the parasitics causes unbalance of the switching voltage and current of the paralleled branches.

The other disadvantage of the proposed module is that it takes more substrate area. The reason is that the current die metallization is made in a certain pattern: the collector of IGBT and the cathode of the diode are made of silver alloy for solder attachment; the emitter of the IGBT and the anode of the diode are made of Al alloy for wire bonding. This requires the two devices in P-cell and N-cell to be arranged on separate DBC, which takes more substrate area.

7 Conclusion and Future Work

7.1 Conclusion

7.1.1 Summary of the Work

This dissertation focuses on IGBT power module package layout design based on the P-cell and N-cell concepts to reduce stray inductance inside the module.

In chapter 2, first, the dominant packaging method, wire bonding technology is studied. Then, the stray inductance issue in the power modules is reviewed. The significance of reducing stray inductance is pointed out. Some general rules to reduce inductance are summarized.

In chapter 3, the concepts of the P-cell and the N-cell are introduced. The implication and application in DC-DC converters and DC- AC inverter are discussed. Then the reduction of stray inductance in a commutation loop for a phase-leg is explained. A conventional anti-parallel phase-leg module and a proposed P-cell and N-cell phase-leg module are modeled in Ansoft Q3D Extractor, and then the corresponding stray inductance is extracted. The electromagnetic simulation results verify the prediction of reducing inductance using the new concepts.

The switching behavior of the power module under parasitic inductance is studied using Synopsys Saber in Chapter 4. First, the under tested IGBT and diode are modeled using Saber Architect. Then, turn-on current ringing and turn-off voltage overshoot are observed during switching. With smaller stray inductance in the proposed phase-leg, the switching characteristic is improved.

In chapter 5, to verify the proposed concept and the parasitic extraction using software, modules with different layout designs are fabricated specifically for parasitic inductance measurement. The parasitic inductance is measured using precision impedance analyzer 4294a and pin probe 42941a. The measurement results agree well with Q3D simulation results and confirm the reduction of the stray inductance using proposed layout. In order to verify the advantage of the switching characteristic in the proposed phase-leg module package over the conventional module, a double pulse tester is built in the laboratory. Several methods are adopted to reduce the parasitics in the printed circuit board and optimize the voltage and current measurement. To measure the voltage across the IGBT die, a new method is proposed. Two thin wires are soldered as close as possible to the die, and connected to the voltage probe of the oscilloscope. The voltage drop on the module stray inductance can be detected. The experimental results show an 11-V reduction in the turn off voltage overshoot, while the total voltage overshoot is around 90 V. Also, there is some reduction in the turn off switching loss.

In chapter 6, the P-cell and N-cell concepts are extended to the multichip phase-leg modules. In high power application, to increase the current ability of the module, paralleling dice is very common. Multichip modules are more complex compared with single device modules because of the current sharing problem, which degrades the reliability of the power modules. The P-cell and N-cell phase-leg module and a conventional phase-leg module are designed and the parasitics are extracted. Both simulation and measurement show some improvement of the total loop inductance in the proposed module. However, the mismatch of the module stray inductance is more severe in the proposed module than in the conventional. The Saber simulation shows the imbalance of the switching voltage and current due to the

parasitic mismatch. This compromises the advantage of the proposed layout.

7.1.2 Power Module Design Considerations and Influence of Parasitics

Through the study of the power module parasitics and the device switching characteristics in this dissertation, several module layout design rules and the influence on the switching behavior are summarized as following:

- In module substrate layout design, the commutation loop should always be considered. The two commutating devices should be as close to each other as possible. The p-cell and n-cell concepts help to enhance the recognition of commutation loop and minimize stray inductance.
- Attention should be paid to module terminal leads. The terminal lead is simplified in this study. In practice, due to the requirement on the mechanical strength, connection interface, and fabrication easiness, they are large and complex, and the stray inductance associated with the leads is large. To reduce the stray inductance, the positive and the negative leads should be laminated and arranged to be as close as possible. These layout techniques are to reduce the loop covered area and cancel the magnetic fluxes associated with the two leads.
- In most cases, the stray inductance in the DC bus bar from decoupling capacitors to the module is also significant. If a cable is used for the DC bus, it should be twisted or arranged as close as possible; if copper sheets are used, lamination is necessary.
- The switch overshoot voltage is proportional to the total loop inductance and the current slope.
- The parasitic capacitance has a significant influence on switching behavior. The dice

junction capacitance is the main contribution to the module parasitic capacitance.

- The Miller capacitance Cres affects the turn off voltage (*Vce*) slope. The capacitance (*Vce* > 10) increases, the turn off voltage slope reduces.
- *Cge* affects gate voltage. Decrease *Cge*, the turn on and turn off delay time reduced. It also affects *Vce* transient behavior. The turn off oscillation period reduces and the oscillation amplitude decreases.
- *Cce* has the same effects on *Vce* transient behavior.
- Gate resistance affect the IGBT current rise and fall time. Gate resistance also affects the gate plateau voltage level; thus by reducing the gate resistance, one can lower the turn off plateau, and increase the turn on plateau.

7.1.3 Contributions of This Dissertation

The contributions of this work is summarized as follows:

- Adopted a series of simulation tools, measuring and experimental methods studied the concept of packaging using novel switching cells. The reduction of the stray inductance of the p-cell n-cell layout is verified. The disadvantage of the layout in modules with paralleled devices is pointed out.
- The methods of measuring nano-Henry level inductance inside a power module were explored, including picking the correct equipments and fabricating modules with conducting commutation loops.
- Proposed a new method to measure dynamic voltage across dice. The essence is to separate the measurement loop from the power path. Using this method, the true voltage across die is obtained, which also makes the calculation of the switching loss

more accurate.

7.2 Future Work

The following issues can be studied for possible future work:

1. The proposed multichip module in this work has asymmetric paralleled loops, which compromises the advantage of the stray inductance reduction. This is caused by the arrangement of the bus bar. The bus bar can be arranged in the middle of the module instead of the side to ensure the two paralleled loops can be symmetric. However, the substrate layout and the bus bar should be designed carefully, to trade off the stray inductance reduction in the layout, laminated bus bar and balanced paralleled branches.

2. The P-cell N-cell arrangement decouples the two commutation loops. It allows adding some inductance in between the two cells, while this added inductance does not affect the commutation loop. This can reduce the requirement for dead time and reduce the effect of a short between the upper and lower IGBTs. There are two issues with is idea, one is what kind of inductance is proper to serve the purpose, and the other is to ensure no side effects will be introduced by adding inductance between the cells.

3. The stray inductance problem is more critical for faster semiconductors like MOSFET or JFET. One reason is the much higher switching speed, and the other is because of the smaller parasitic capacitance of the die. Based on experimental experience, the switching waveform is degraded much more severely than IGBT because of stray inductance. The novel switching cell concept can be extended to MOSFET or JFET modules.

The commercial dice nowadays are metalized as Al on the top side for wire bonding purpose and silver on the bottom side for soldering purpose. Then the active device and the

freewheeling diode in the P-cell or N-cell have to be soldered on separate DBCs, this adds additional wire connections and requires larger substrate area. If the metallization of the dice can be changed, there will be more benefit for the novel switching cells.

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