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A Current-Mode Multi-Channel Integrating Analog-to-Digital Converter

Neena Balakrishnan Nambiar
University of Tennessee - Knoxville

To the Graduate Council:

I am submitting herewith a dissertation written by Neena Balakrishnan Nambiar entitled "A Current-Mode Multi-Channel Integrating Analog-to-Digital Converter." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

Benjamin J. Blalock, Major Professor

We have read this dissertation and recommend its acceptance:

Milton N. Ericson, Michael J. Roberts, Suzanne Lenhart

Accepted for the Council:
Dixie L. Thompson

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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A Current-Mode Multi-Channel Integrating Analog-to-Digital Converter

A Dissertation

Presented for the

Doctor of Philosophy

Degree

The University of Tennessee, Knoxville

Neena Nambiar

August 2009

Dedication

I would like to dedicate this work to my parents. I would also like to dedicate this work to my long-standing friend Qi Lin. The encouragement and support that I got from her throughout my program helped me complete this research work.

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I take this opportunity to express my deepest gratitude to my advisor Dr. Benjamin Blalock for providing constant encouragement, advice, and support throughout my PhD program. Without his valuable guidance and persistent help this dissertation would not have been possible. I am grateful to Dr. Nance Ericson for his valuable advice, help, and mentoring during my research. I would like to thank Dr. Charles Britton for his many helpful suggestions during the course of my study. I would like to thank Dr. Michael Roberts and Dr. Suzanne Lenhart for being on my committee and giving me their constructive suggestions while working towards my final dissertation.

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Abstract

Multi-channel analog to digital converters (ADCs) are required where signals from multiple sensors can be digitized. A lower power per channel for such systems is important in order that when the number of channels is increased the power does not increase drastically. Many applications require signals from current output sensors, such as photosensors and photodiodes to be digitized. Applications for these sensors include spectroscopy and imaging. The ability to digitize current signals without converting currents to voltages saves power, area, and the design time required to implement I-to-V converters.

This work describes a novel and unique current-mode multi-channel integrating ADC which processes current signals from sensors and converts it to digital format. The ADC facilitates the processing of current analog signals without the use of transconductors. An attempt has been made also to incorporate voltage-mode techniques into the current-mode design so that the advantages of both techniques can be utilized to augment the performance of the system. Additionally since input signals are in the form of currents, the dynamic range of the ADC is less dependant on the supply voltage.

A prototype 4-channel ADC design was fabricated in a 0.5-micron bulk CMOS process. The measurement results for a 10Ksps sampling rate include a DNL, which is less than 0.5 LSB, and a power consumption of less than 2mW per channel.

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LIST OF ABBREVIATIONS

ADC	Analog-to-Digital Converter
BJT	Bipolar Junction Transistor
CFA	Current Feedback Amplifier
CMOS	Complementary Metal-Oxide Semiconductor
CS	Common Source
DAC	Digital-to-Analog Converter
DAQ	Data Acquisition
DIP	Dual In-line Package
DNL	Differential Nonlinearity
ESD	Electrostatic Discharge
FFT	Fast Fourier Transform
FGMOS	Floating Gate Metal-Oxide Semiconductor
FPGA	Field Programmable Gate Array
GPIB	General Purpose Interface Bus
INL	Integral Nonlinearity
JTAG	Joint Test Action Group
LDO	Low Dropout
LSB	Least Significant Bit
LVDS	Low Voltage Differential Signaling
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
MSB	Most Significant Bit
NMOS	N-Channel Metal-Oxide Semiconductor
NOTA	N-Input Operational Transconductance Amplifier
OTA	Operational Transconductance Amplifier
PMOS	P-Channel Metal-Oxide Semiconductor
POTA	P-Input Operational Transconductance Amplifier
PROM	Programmable Read Only Memory
RMS	Root Mean Square
SAR	Successive Approximation Register

SI	Switched Current
SMA	Sub-Miniature A
SNDR	Signal to Noise and distortion Ratio
SNR	Signal to Noise Ratio
THD	Total Harmonic Distortion

Chapter 1

Introduction

Even though many systems have completely converted to digital, the real world is still primarily analog. The real world does not observe binary signals but rather continuous signals such as voice, temperature, color, movement, etc. Thus, the analog world is more fascinating, colorful, and challenging than its binary equivalent. Thus, it is important to be able to collect analog information, process it, and control it. Therefore, in order to interface digital systems with the analog real world various forms of data converters are required. Analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) are required in every system that interfaces to the natural world. ADCs have applications in communications, industrial process control, instrumentation systems, and nearly every field where analog signals are present.

1.1 Statement of Research

The primary goal of this research is to investigate, design, implement, and test a multi-channel integrating current-mode ADC. This circuit provides an interface to photodiodes and minimizes the dependence of the dynamic range of a conventional ramp ADC on the supply voltage.

The following sections explain the history, background, and motivation of this research.

1.2 Types of Analog-to-Digital Converters

ADCs are categorized and classified by their performance characteristics. These include resolution, bandwidth, sampling rate, power consumption, and the effective number of bits the converter demonstrates after test and measurement. A variety of ADC topologies are proposed for the different

applications and requirements. Commonly used architectures include the successive approximation register (SAR), the flash ADC, the pipeline ADC, and the sigma-delta ADC.

1.2.1 History of ADCs

Numerous ADC architectures exist that meet the ever increasing demands of data acquisition. The first successive-approximation ADC was built and tested with vacuum tubes in 1954 by Bernard Gordon [1]. It uses a single comparator, an internal DAC, a reference voltage, and multiple conversion cycles to perform a conversion. Since multiple conversion cycles are required, the SAR has a lower conversion speed. The flash ADC was originally developed in the 1940s for use in one of the earliest pulse height analyzers of nuclear physics instrumentation [2]. The flash ADC uses multiple comparators, but a single cycle to perform a conversion. It has the highest speed among ADCs, but it is not as area or power efficient as some other architectures, since for an *n* bit resolution it requires $2^n - 1$ comparators. The pipeline ADC has its origins in the sub-ranging ADC, which was designed with tubes and transistors in [3]. The sigma-delta ADC originated from [4] and was called fast high resolution predictive analog-to-digital converter. Among integrating ADCs, the dual slope ADC and the single slope ADC are both based on Reeve's counting ADC, patented in 1939 [5].

1.2.2 Comparison of ADC specifications

Figure 1.1 shows the types of ADCs and compares the numbers of bits each achieves to the sampling rate. The flash ADC achieves the highest sampling rate, but has the lowest resolution, as opposed to the sigma delta and the integrating ADC which have high resolution, but a lower conversion rate. Hence, a tradeoff needs to be made between speed and resolution when selecting the type of ADC that suits the targeted application. In addition to the speed and resolution, the power consumption must also be taken into consideration in the selection of the topology. Higher speed ADCs, like the flash ADCs, require additional power mainly due to the number of comparators used in the architecture. A

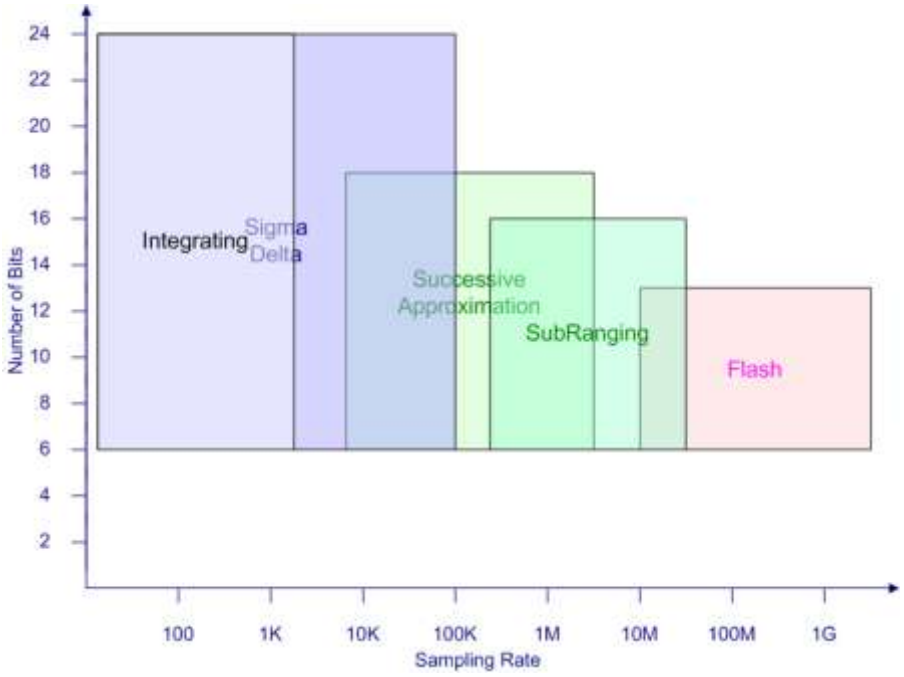

Figure 1.1 Comparison of Resolution vs. Speed for Different Types of ADCs

study is summarized in [6] comparing the different types of ADCs by a figure of merit which is based on the sampling rate and power dissipation.

In addition to these conditions, the required supply voltage must be taken into consideration. As the minimum gate length reduces, the supply voltage also reduces. Thus, the ADC topology selected needs to be able to support a lower supply voltage. This may also increase circuit complexity to an extent and in turn, the power consumption.

1.3 Multi-channel ADCs

A small number of multi-channel ADC designs have been proposed to provide the capability to digitize multiple analog signals simultaneously. Multi-channel ADCs are required in sensor array systems, medical applications where data from multiple electrodes is analyzed, and in chemical analyzers. These allow data conversion from multiple inputs and hence can be processed simultaneously. A high

sampling rate is not required in most of these applications since the changes are slow. Another area of application for multi-channel ADCs is in imaging systems where multiple pixels can be converted simultaneously to digital. Converting multiple analog signals simultaneously requires a reasonable sampling rate with low power consumption, but makes achieving area efficiency a challenge. For most multi-channel ADCs, time interleaving the outputs costs speed, and results in inefficient usage of area.

1.3.1 Wilkinson Multi-channel ADC

The Wilkinson ADC is an integrating type single slope ADC [7] which supports multiple channels. The ADC consists of a single ramp generator and a counter. Each channel consists of a comparator, a latch, and a register. Since the ramp and the counter are shared by all the channels, considerable power savings and area efficiency are achieved by using this architecture compared to using a single ADC per sensor input. A functional block diagram of a 16-channel Wilkinson ADC is shown in Figure 1.2.

The analog inputs to the ADC are connected to the comparators. During the sampling phase, the comparators, while auto-zeroing the output, sample the analog input. Since the comparator performs the dual functions of comparing and sampling, additional power savings are attained when the sample and hold block is eliminated. In the second phase, the comparator input is tied to the ramp generator. The ramp generator generates a linear voltage from 0 to 1.2 V. This range may vary depending on the design of the ADC's ramp generator and the supply voltage. The linearity of the ramp is required to be 12 bits in order to achieve a 12-bit accuracy. Linearity of the ramp is defined here as the deviation of the ramp from the best fit straight line. The counter counts from 0 to 4095 as the ramp linearly rises from 0 to 1.2 V. At the instant the voltage on the ramp reaches the input voltage, the comparator trips and the count on the counter is stored on the latch.

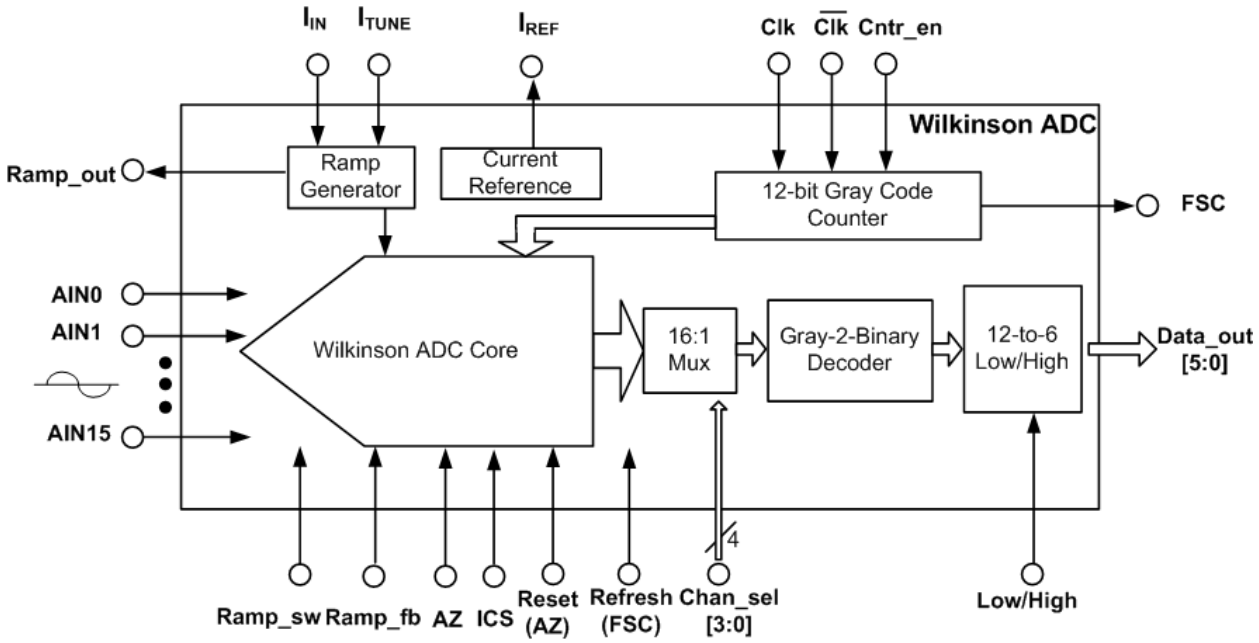

Figure 1.2 16 Channel Wilkinson ADC

During the next sampling phase, the contents of the latch are read into a register while the next set of data is sampled. The data in the register is then read out, channel by channel, while the ramp integrates from 0 to 1.2 V. A Gray code counter is used to eliminate the errors and glitches which can arise from multiple bits changing at the same time. The ramp generator uses a tuning current, controlled externally to vary the range of the ramp.

1.4 Motivation

1.4.1 Sensors and Electrodes

Many sensors used for medical, as well as chemical analysis, provide current signals. These signals can be processed as currents, or converted to voltages using transimpedance amplifiers, and then processed. Converting currents to voltages uses additional chip area. In addition, parameters of the amplifier, such as offset, bandwidth, and nonlinearity, are required to be within certain specifications so

that they do not affect the accuracy of the data acquired. Unnecessary signal conversion steps (for example current to voltage conversion) only add to the system complexity and cost and reduce system efficiency.

Photodetectors, such as photodiodes, are used in various applications. When photons are incident on photodiodes, they produce an electron-hole pair, resulting in a current across the p-n junction of the photodiode.

A current mode ADC is advantageous for such applications as the current from the sensor can be directly processed and converted to digital without passing through an intermediate stage of current to voltage conversion. The multi-channel current-mode ADC proposed in this work is even more efficient in terms of power consumption and conversion speed than the multi-channel current-mode ADCs that have been implemented in the past, which are described in Chapter 2.

1.4.2 CMOS Scaling and Effects

Moore's Law (1965) states that "The number of transistors that can fit onto a square inch of silicon doubles every 12 months". Miniaturization is an important trend on the CMOS roadmap [9]. As CMOS continues on this trend, a number of hurdles need to be overcome. Feature size is the minimum distance between the drain and the source which is achieved in fabrication. Increased miniaturization implies that reducing feature size reduces gate length. In order to reduce the transistor gate length L, the depletion width is reduced. This may be achieved by increasing the substrate doping concentration and decreasing the reverse bias. To achieve the latter under any circuit operating conditions, the supply voltage must also be decreased. Additionally, increasing the doping concentration increases the threshold voltage and makes it difficult to turn on the device. This is overcome by reducing the oxide thickness. Considering electrostatic effects, maintaining the reliability of devices, i.e., constant aging rate requires

limiting the maximum electric field in the channel. This is practically achieved by reducing the supply voltage as well as by modifying the drain channel junction to control the maximum electric field. [10].

1.4.3 Conclusion

In conclusion, a reduced feature size necessitates a low supply voltage. Consider the Wilkinson ADC of Section 1.3.1 at a low supply voltage. A 12-bit resolution and a wide input voltage range depend strongly on the ramp generator which generates a linear voltage from 0 to 1.2 V in that example. As the supply voltage reduces, so does the range and linearity of the ramp.

The above disadvantage is of prominent concern, but other drawbacks to the configuration exist as well. Since at the input to each channel is a comparator which is connected to the same ramp generator, the output impedance of the ramp generator plays an important role. Each comparator exhibits a kickback when it changes state from *low* to *high*, or when the reference input exceeds the input voltage. Kickback is defined as a disturbance or noise at the input of the comparator due to a change in voltage level at the output of the same comparator. Since multiple comparators are connected to the same node on the ramp generator, this kickback causes a disturbance in the ramp, creating errors in the conversion.

A current mode Wilkinson ADC provides the solution to both of the important issues presented above. The current ramp is not dependant on the supply voltage, since the ramp is a linearly changing *current* signal rather than a voltage signal. Many sensors demonstrate a current change as opposed to a voltage change. The input signal range is thus not limited by the supply voltage. Since the ramp is a current signal, the ramp is mirrored out to the different channels. The separation of the ramp signal reduces coupling between the different channels without a large increase in power by having completely independent ramp generators for each channel. Current comparators are implemented to compare the ramp with the input signal.

A current-mode design has its own disadvantages, such as mismatch caused by the current mirrors. This mismatch does reduce the resolution of the converters. Additionally, a constant dc bias current is required to maintain transistors in their saturation region. Hence, there is an increase in power consumption, which is well managed by proper design.

1.5 Research Goals

Considering all the above concerns, the goals of this research are as follows:

1. To design a medium-speed multi-channel ADC to simultaneously digitize sensor outputs.
2. To design a current-mode ADC to support current output sensors including photodiodes.
3. When considering the lowering of the supply voltage with the gate length, this ADC is required to support a lower supply voltage without an increase in circuit complexity or power consumption.
4. To design a Gray code counter that is able to support a high rate of counting without missing codes, and with low power consumption.
5. To design both a current-ramp generator and a comparator to support 12-bit accuracy.
6. To test the ADC for functionality and the different parameters of the ADC are to be measured.
7. Determine possible applications of this novel architecture ADC.

1.6 Thesis Chapter Overview

This work presents a study of current-mode techniques and the design, implementation, and testing of a novel current-mode integrating ADC. Chapter 2 is an introduction to the design blocks used in current-mode design. It further presents a literature review of the existing current-mode ADC designs including sigma-delta, folding and interpolating, successive approximation, and two multi-channel current-mode ADCs. Chapter 3 describes the architecture and design of the novel current-mode ADC with the main design blocks of the ADC, the digital section, and the timing of the signals. Chapter 4

explains the characterization of the ADC. The various parameters that describe the characteristics and performance of the ADC are defined. A description of the design of the test board used to characterize the converter is provided and the method used to debug the test system is explained, in addition to the tests used to characterize the ADC. Chapter 5 describes the applications of the ADC for spectroscopy and similar applications. Further, future research work investigating methods to improve performance is detailed, along with a plan to expand the architecture to add functionality for specific applications. Finally, Chapter 6 concludes this work with a summary of the results and original contributions. The Appendix includes the Verilog code and the Labview block diagram used to test the ADC.

Chapter 2

Literature Review

As the device channel length reduces, the gate thickness reduces and hence, the supply voltage is reduced in order to ensure device reliability. A reduction in power of the digital circuits is also achieved by reducing the supply voltage. This holds true since the dynamic power consumption of the digital circuits is directly proportional to the square of the supply voltage and the frequency of operation of the circuit. The dynamic power consumption of a digital circuit is given in equation 2.1.

$$P = fC_L V_{DD}^2 \tag{2.1}$$

For analog circuits, a reduction in the supply voltage does not reduce power consumption since the power in analog circuits is mainly determined by the signal-to-noise ratio and the frequency of operation. Signal levels need to be maintained well above the thermal noise in order to achieve a reasonable dynamic range. For lower-feature-size processes with low supply voltages, the available voltage headroom is proportionally lower. Device stacking cannot be implemented due to the available voltage headroom. To improve the performance characteristics, folded topologies such as folded cascodes are used. For voltage-mode circuits, the complexity of the circuit increases for low supply voltages. Hence, they require more branch currents and power dissipation.

With current-mode design, lower voltages can be supported without increasing the complexity of circuits since the signals are in the form of currents. Current-mode design, however, requires a dc current to flow through it, which may increase power dissipation. Combining both techniques improves the

design and performance of the circuits, and increases the capabilities of a mixed signal system, as far as the dynamic range and supply voltage limitations are concerned. A voltage-mode design can utilize techniques from current-mode for both low voltage and low power consumption operation. At the same time, a classical voltage-mode design technique, such as the Miller compensation, can be used in circuits that process current signals [11].

2.1 Current-Mode Circuits

Figure 2.1, which is an illustration adapted from [12], depicts the blocks of current-mode circuits and applications. Some of the building blocks include current-copiers which act as memories to store current, switched current integrators which are used in filters, and translinear circuits which use the

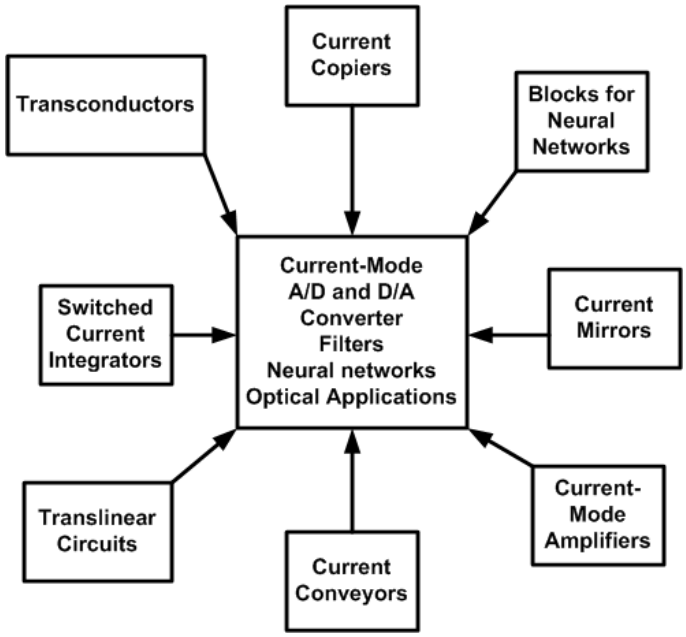

Figure 2.1 Current-Mode Circuits and Applications

nonlinear properties of bipolar junction transistors (BJTs) and metal-oxide semiconductor field-effect transistors (MOSFETs) in weak inversion to generate the required signals. Current conveyors, current-mode amplifiers, switched current integrators, current mirrors and transconductors are elements of a

current-mode system. Neural networks are an example of a current-mode system and include blocks such as current adders and current thresholders.

Current-mode A/D and D/A converters as well as filters use these blocks to achieve the required operation. The primary applications of current-mode systems are optical systems and neural networks. The following sections describe in brief these current mode building blocks.

2.1.1 Current Copiers

Current copiers are useful when the sampling and storing of currents are important. A basic current copier is shown in Figure 2.2. Switches S1 and S2 are initially closed. The capacitor C1, charges

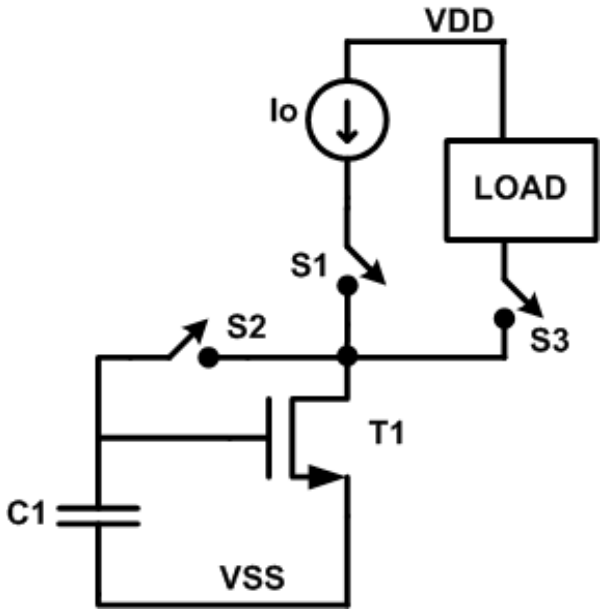

Figure 2.2 Basic Current Copier [12]

with the help of the current source Io, through switches S1 and S2. The capacitor charges to a voltage that will bias the gate voltage of the transistor T1, so that a drain current equal to Io may flow through the transistor. Switches S1 and S2, are then opened and the switch S3, is closed to let a current of Io flow

through the load. The clock feed-through of the switches, the leakage current, and channel length modulation are the main sources of error in a basic current copier circuit. Advanced copiers can reduce or eliminate these sources of error.

2.1.2 Transconductors

Traditionally, all signal processing is carried out in the form of voltages. To maintain compatibility between voltage and current modes, it may be necessary at times to convert the voltages to currents or vice versa. If the input signals are in the form of voltages, they may need to be converted to currents for further processing. This is achieved with the help of a transconductor. After all processing is performed, the output is converted back to currents. with the help of transresistors. Transconductors are, however, used more frequently and have stringent specifications which include low noise, high linearity, and low quiescent power dissipation. A simple differential pair can be used as a transconductor. More complex topologies are used to improve the linearity and noise performance of the transconductors.

2.1.3 Switched Current Integrators

Switched capacitor integrators are used in filters, A/D converters, D/A converters, sample and hold circuits, as well as other applications. The switched capacitor circuits require linear floating capacitors. When algorithms are required to compute values depending on past and present voltages, switched capacitor circuits are used. As the supply voltages are lowered, a number of problems arise, including gate leakage. These issues do not allow optimal performance for switched capacitor circuits. Switched current circuits were introduced partially to overcome several of these challenges.

Switched-current (SI) integrators replace switched capacitor integrators except that the processing is achieved in current signals instead of voltage signals. Current memories, as described in Section 2.1.1,

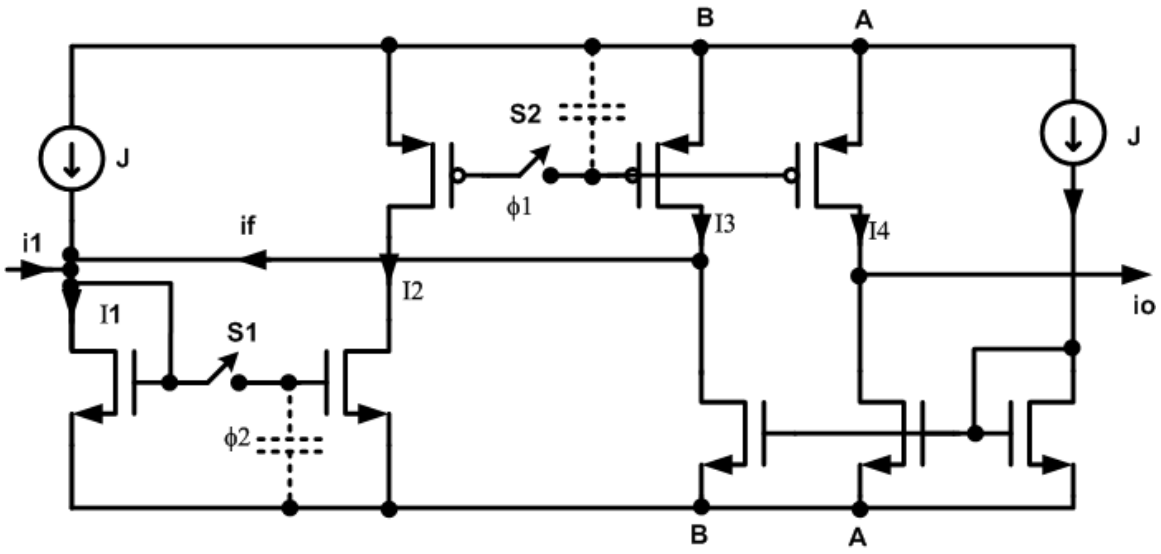

Figure 2.3 First Generation Non-Inverting Switched-Current Integrator [12]

are used within the SI integrators. Figure 2.3 shows an example of a switched current integrator. This is a first generation non-inverting switched-current integrator. Branches A and B are weighted output stages. Branch A supplies the output current whereas, branch B is fed back to the input stage. During the first phase, at time *(n-1)*, switch S2 is closed and the output current is given as *io(n-1).*

During the Φ2 phase of the clock cycle *(n-1)*, S1 is closed, S2 is open, and the output is held at the same value as in the first phase. The feedback signal from stage B results in current *I1*, which is given in Equation 2.2.

$$I1 = J + i1(n-1) + \frac{B}{A} io(n-1) \tag{2.2}$$

The output current, during the first phase of the *n*th clock cycle, is given in Equation 2.3.

$$io(n) = Ai1(n-1) + Bio(n-1) \tag{2.3}$$

If a z-transform of the equation is calculated, the transfer function of the equation is given as in Equation 2.4 .

$$H_1(Z) = \frac{io(Z)}{i1(Z)} = \frac{AZ^{-1}}{1 - BZ^{-1}} \tag{2.4}$$

This is the transfer function of a non-inverting integrator. Hence, a switched current integrator is implemented using currents as signals. This is a simple example of an SI integrator. This topology has several shortcomings which are addressed in the second generation SI integrators. SI differentiators may also be implemented using a similar method.

2.1.4 Translinear Circuits

The term translinear was coined in 1975 [12]. This type of circuit is based on the operation of a BJT where the transconductance of the BJT is linearly proportional to the collector current, hence, the term "trans-linear" [12]. The relationship between the collector current I_c, and the base to emitter voltage of the BJT, $V_{BE,}$ is the heart of the BJT which is given in Equation 2.5.

$$\boldsymbol{I_C = I_S(T)\left(e^{V_{BE}/V_T} - 1\right)} \tag{2.5}$$

This equation plays an important role in the evolution of translinear circuits. The collector current is dependent on the base to emitter voltage. By differentiating the equation of $I_{c,}$ with respect to $V_{BE,}$ it can be shown that the transconductance of a BJT exhibits linearity with respect to the collector current over a large current range. An example of a translinear circuit is a simple current mirror. Another example of a translinear circuit, the basic multiplier cell, is shown in Figure 2.4. Using equation 2.5, and assuming that the four transistors have equal saturation currents and emitter areas, the relationship between currents flowing in the four branches of the cell is given as Equation 2.6.

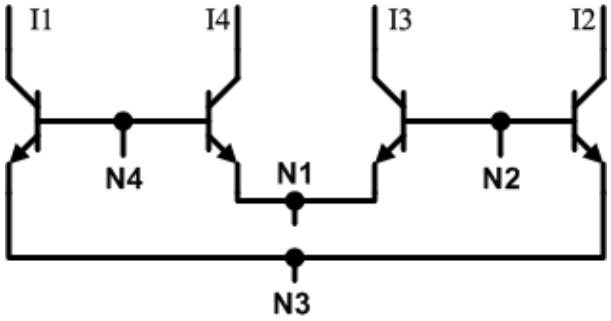

Figure 2.4 Translinear Circuit – Multiplier [12]

$$\boldsymbol{I}_1\boldsymbol{I}_3 = \boldsymbol{I}_2\boldsymbol{I}_4 \tag{2.6}$$

The implementation of squaring circuits, dividers, and square root calculators can be carried out using similar techniques.

MOS transistors in weak inversion show the same logarithmic relationship of I_{DS} to V_{GS} as the BJTs. Hence, MOS transistors in weak inversion are also used in translinear circuits. The translinear principle is stated as "In a closed loop containing an even number of forward biased junctions, arranged so that there are an equal number of clockwise-facing and counterclockwise facing polarities, the product of the current densities in the clockwise direction is equal to the product of the current densities in the counterclockwise direction" [12]. When applying this principle to the multiplier cell in Figure 2.4, the same relation as stated in Equation 2.6 can be obtained.

2.1.5 Current Conveyors

Current conveyors are four or five terminal circuit blocks which, when integrated with other blocks, perform various useful signal processing operations. For example, they are used in filters. The first generation current conveyors consist of three terminal blocks. Figure 2.5 shows the simple form of a first-generation current conveyor. The operation of this block is such that an input voltage at terminal Y appears at terminal X. Current input at terminal X is copied to terminal Y and also appears at terminal Z.

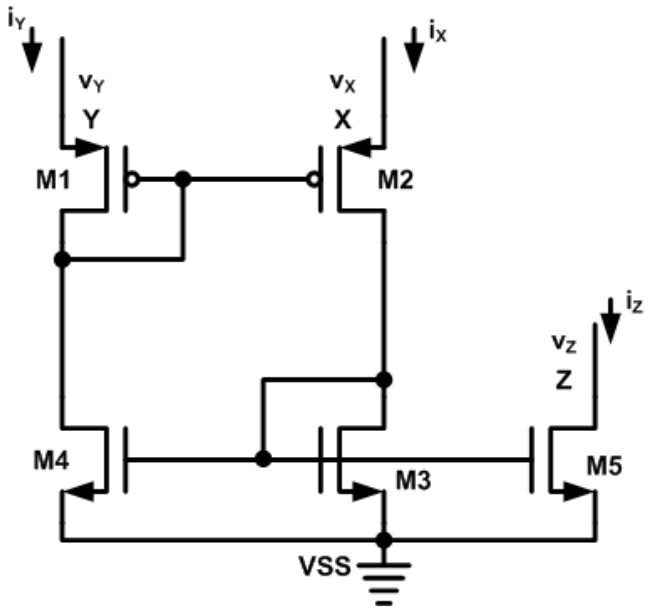

Figure 2.5 First Generation Current Conveyor [12]

Second-generation current conveyors are such that zero current flows through terminal Y, hence, terminal Y has an infinite input impedance. The current flowing through terminal X is only copied to terminal Z.

For filter circuits, inductors may be required. Inductors occupy a large area on-chip, so in order to save area on the chip, active circuits are used to emulate the inductor. This is done with the help of a gyrator circuit. The gyrator is implemented by connecting two current conveyors of opposite polarity. The other applications of current conveyors include oscillators, precision rectifiers, and current feedback amplifiers.

2.1.6 Current-Mode Amplifiers

Operational amplifiers have been used for a long time and exhibit many nearly ideal characteristics such as high input impedance, low output impedance, high gain. With the development of current conveyors and translinear loops, current-mode amplifiers come into the picture. Current-mode

amplifiers have been realized from translinear loops and current conveyors with differential current inputs and outputs.

More familiar to the industry, however, among the amplifiers using currents as signals, are the current feedback amplifiers. These amplifiers have a zero or low input impedance as opposed to traditional operational amplifiers. This implies that the input terminals have currents flowing in them. A model of a current feedback amplifier (CFA) is shown in Figure 2.6. The non-inverting input terminal sees the input of a buffer and the inverting terminal sees the output node of the buffer. Output voltage varies depending on the current flowing between the input nodes. Current feedback amplifiers are used in video amplifiers since they are capable of wide bandwidth of operation.

2.1.7 Current Mirrors

Current mirrors play an integral role in current mode circuits. They have many applications in a wide variety of circuits such as biasing and the generation of multiple current sources or sinks from a single source. Matching between current mirror transistors plays an important role in the accuracy of

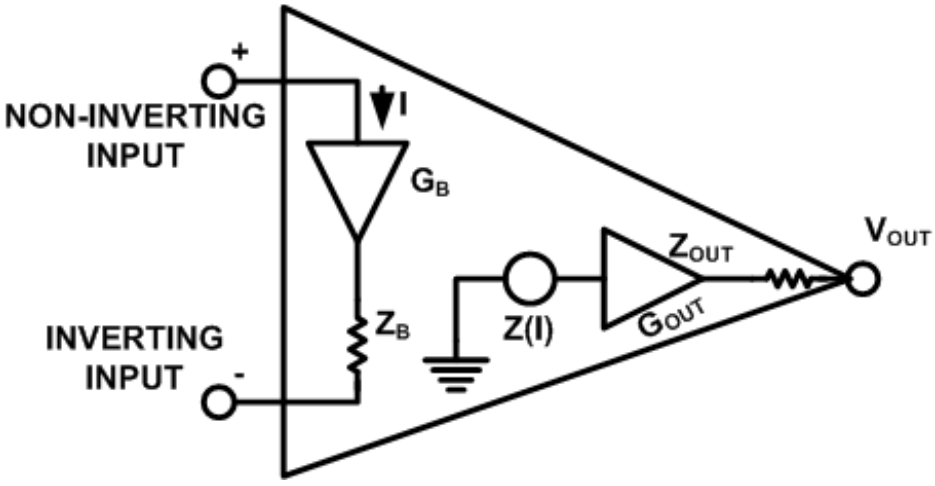

Figure 2.6 Current Feedback Amplifier Model [13]

current-mode circuits. This is discussed in further detail in Section 3.2. Different types of current mirrors exist for varying applications, such as the Wilson current mirror, cascoded current mirror, wide swing current mirror, and many more. Current mirrors applied to BJTs may be more complex than those implemented with MOSFETS since BJTs require a base current for operation. Base current compensation is required to offset the error in current mirroring. Current copiers, described in Section 2.1.1, are a form of dynamic current mirrors.

2.1.8 Neural Networks

The human brain has enormous computational ability. Neural networks are used to emulate various abilities of the human brain [12]. Analog storage is required for this purpose. Unlike digital storage, analog storage is more challenging due to the effects of leakage. Analog storage is not restorable, so nonvolatile floating gate transistors may be used for this purpose. These transistors have extra layers on the gate to trap the stored charges, so the degradation of analog storage is slower than that of a normal MOSFET.

Current-mode signal processing is attractive for neural networks since it offers simpler circuits for addition or subtraction. Figure 2.7 shows a programmable synaptic element. This basic block provides storage with the help of the floating-gate metal-oxide-semiconductor (FGMOS) and provides an output which is weighted times the input. Current adders, subtractors, and current thresholders are implemented with simple topologies to implement neural networks. Transistors in the subthreshold region have been used to implement circuits for neural network applications which save power.

2.2 Current-Mode ADCs

Different building blocks for current-mode systems are described above. These blocks are used in applications such as A/D and D/A converters, filters, optical systems, and neural networks. Various types

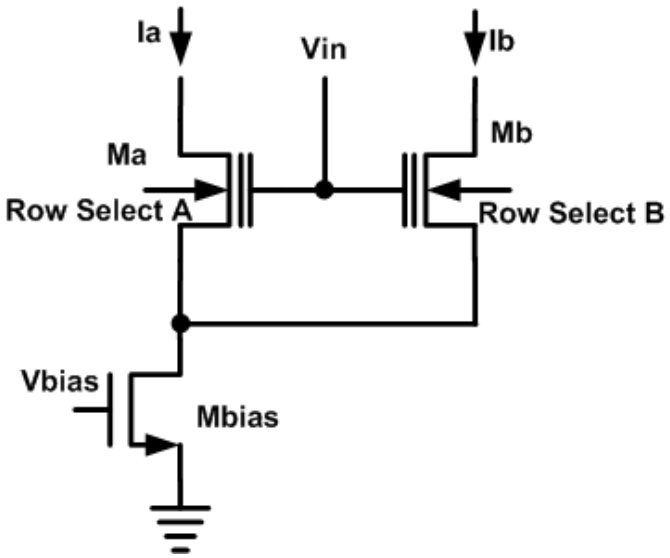

Figure 2.7 Programmable Synaptic Element [12]

of ADCs are described in this section.

For analog-to-digital converters, the dynamic range specification implies the total signal amplitude, which the converter can resolve. For a reduced voltage supply, the dynamic range is highly reduced or the A/D converter requires a complicated design to achieve specifications similar to the specifications of a converter with a higher supply voltage. Furthermore, when the signals are widely distributed with respect to voltage, the parasitic capacitors charge and discharge with the voltage swings. This reduces the frequency of operation. It is difficult to avoid these signal swings in current-mode circuits. However, the nodes usually have a lower parasitic capacitance. It is challenging to convert a given range of signals, and to obtain a resolution of 10 or 12 bits with a low supply voltage. To some extent, using current-mode ADCs is a solution for this concern. Furthermore, a simpler design is obtained using current mode circuits.

2.2.1 Folding and Interpolating ADC

A few previous current-mode ADC designs utilize the different topologies already existing in voltage mode. A folding and interpolating ADC offers the speed of a flash ADC at a fraction of the area and the power consumption [14]. A folding and interpolating ADC, which folds the input into a number of steps in the form of a sawtooth waveform, is implemented. The upper MSB bits are decided by a coarse ADC, which dictates within which fold the input lies. A flash ADC then decides the LSB bits within the folds. Hence, the number of comparators used in a folding ADC is a fraction of the number used in the flash ADC.

A current-mode folding and interpolating ADC was first proposed in [14]. The 8-bit converter has a 100 MHz sampling rate, and a power dissipation of 55 mW. The block diagram of this ADC is shown in Figure 2.8. If only folding is used to implement the ADC, a large number of folders are required and the

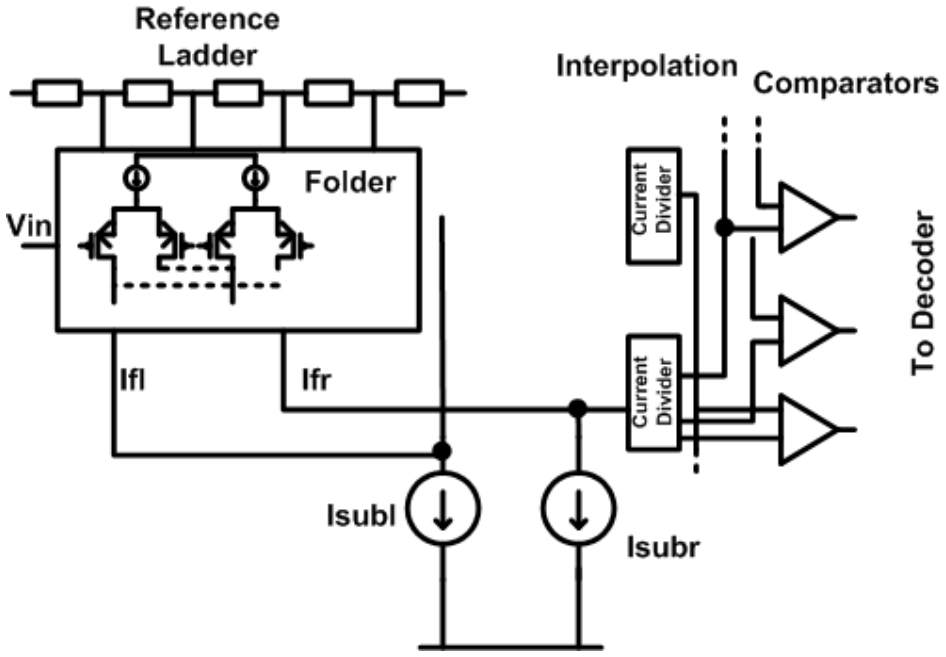

Figure 2.8. Block Diagram of Folding and Interpolating ADC [14]

power dissipation increases greatly. Interpolation is introduced for a finer resolution that would increase the power dissipation and area otherwise. Parallel offset folders are used to fold the input signal. Current dividers are used to interpolate the folded signals. The outputs of the interpolators then become the input to the comparators. The comparator outputs form a cyclic thermometric code. A decoder is then used to decode this code to produce an ADC output. This ADC was investigated to reduce power dissipation and improve the number of bits in [15].

2.2.2 Algorithmic Converter

Algorithmic converters are used where medium-speed ADCs are required. N-bit algorithmic converters require N stages with each stage consisting of an adder and a comparator.

Each stage doubles the output of the previous stage and compares this signal to a reference signal. The sign of the reference signal depends on the comparator output of the previous stage.

A current-mode algorithmic converter is reported in [16]. The equation of one stage of the current-mode algorithmic ADC is given in Equation 2.7.

$$I_i = 2I_{i-1} - b_{i-1}I_{REF} \tag{2.7}$$

$$\text{where } b_{i-1} = \begin{cases} +1 & if \quad I_{i-1} > 0 \\ -1 & if \quad I_{i-1} < 0 \end{cases}$$

The current of the preceding stage is doubled. The doubled current is then compared with the reference current multiplied by the comparator output of the previous stage.

Since current-mode ADCs rely primarily on the accuracy of current mirrors, the effects of mismatch are taken into consideration in [16]. The mismatch in current mirrors is mainly caused by the

mismatch in β and the threshold voltage mismatch V_T. For CMOS devices operating in the saturation region, the relative current error due to mismatch is expressed as in Equation 2.8 [17]

$$\frac{\Delta I}{I_{IN}} = \frac{\Delta\beta}{\beta} - \Delta V_T \left(\frac{2\beta}{I_{IN}}\right)^{1/2} \tag{2.8}$$

where ΔI is the difference in the currents between current mirror input and output, I_{IN} is the input current to the current mirror, β is the average gain constant of the mirroring devices, $\Delta\beta$ is the difference in the gain constants of the mirroring devices, and ΔV_T is the difference in the threshold voltage of the devices.

[16] proposes the active current mirror technique in order to reduce the input resistance of the mirror and the current mismatch between devices. This is a 6-bit ADC with a conversion time of 2 μs. The ADC exhibits a power dissipation of 63 mW while occupying an area of 0.74 mm^2. A block diagram of the algorithmic ADC is shown in Figure 2.9.

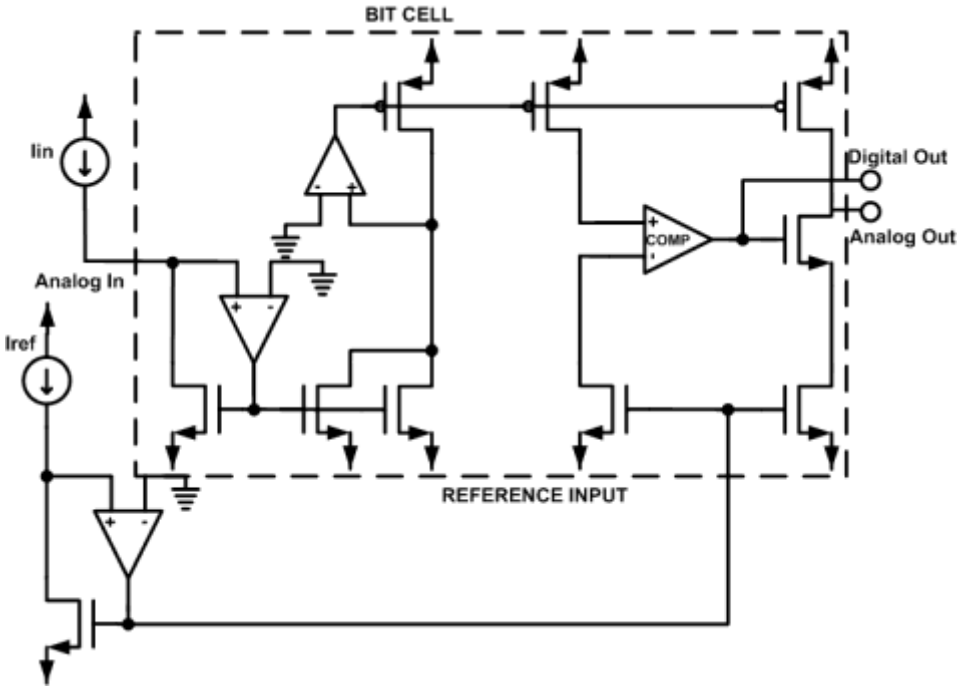

Figure 2.9 1- bit cell of the Algorithmic ADC using active current mirrors [16]

When using simple current mirrors, the resolution is limited to 6 bits. The accuracy of this ADC is improved to 12 bits by using active current mirrors to overcome the issue of mismatch effects. The mirror input resistance is reduced by a factor of A, which is the gain of the amplifier used to improve matching to a large extent. The algorithmic ADC is further investigated to reduce power in [18]. A combination of transistors in subthreshold and current mode techniques is used to reduce power in the topology of [18].

2.2.3 Successive Approximation ADC

A current-mode successive approximation register (SAR) technique was first proposed in [19]. It is based on a switched current (SI) design. The operation is a three-step process and is insensitive to component mismatches. The topology of this ADC is shown in Figure 2.10. The architecture of this ADC consists of an operational amplifier, a current comparator, capacitors, and switches.

During the first phase, the input current is sampled on capacitor C1 using switches S1, S2, and S3. The V_{DS} difference, due to channel length modulation, is reduced using the operational amplifier with a bias voltage *Vbias*, at the positive input. In the second phase, the input current is sampled on capacitor C2 using switches S4, S2, and S5. The rest of the switches are open during this phase. During the third phase, switches S4 and S6 are closed. Both transistors P1 and N1, act as current copiers, memorizing the current flowing through them using capacitors C1 and C2. The sampled current is compared with the reference current during this phase. The comparator trips and changes its state to a high level during this time if the sampled current is greater than the reference current. This technique of current-mode data conversion is independent of transistor or capacitor matching. However, no test or measurement results are provided for this technique.

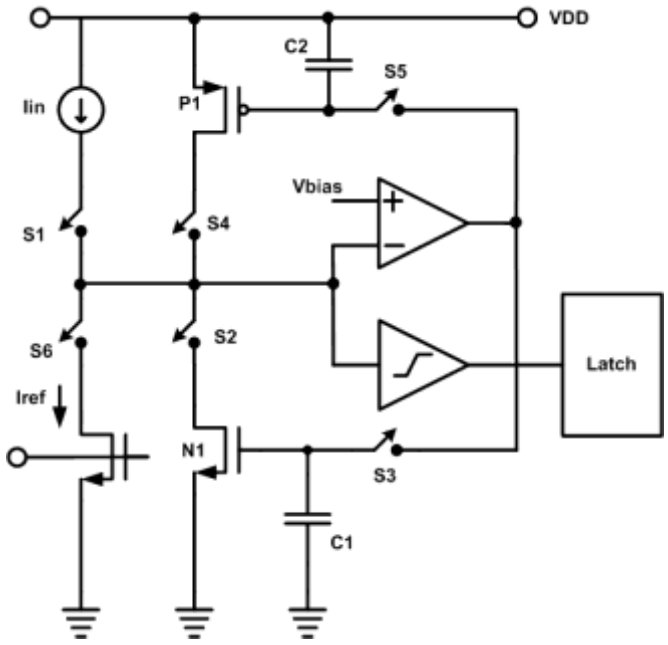

Figure 2.10 Current-Mode Successive Approximation ADC [19]

An interleaved current mode 8-bit SAR is proposed in [20]. This ADC consumes an extremely low power of 3.1 μW at a sampling rate of 100 Ks/s and a supply voltage of 1 V. However, its resolution is only 8 bits, owing to the mismatch in current mirrors.

2.2.4 Sigma-Delta Converter

A switched-current (SI) sigma-delta converter was first reported in [21]. The topology proposed in this work uses current-copier cells to implement the converter. This architecture is shown in Figure 2.11, with the modulator architecture shown in (a) and the balanced copier shown in (b). Switched capacitor integrators need highly linear capacitors to achieve an acceptable resolution. The switched current technique does not require the highly linear capacitors to achieve the required resolution. The integrator implemented is shown in Figure 2.11(b). It uses a transconductor, switches, and MOS capacitors. The switch phases are depicted to the right of the block diagram. $\phi 1$ and $\phi 1s$ are closed initially, allowing the

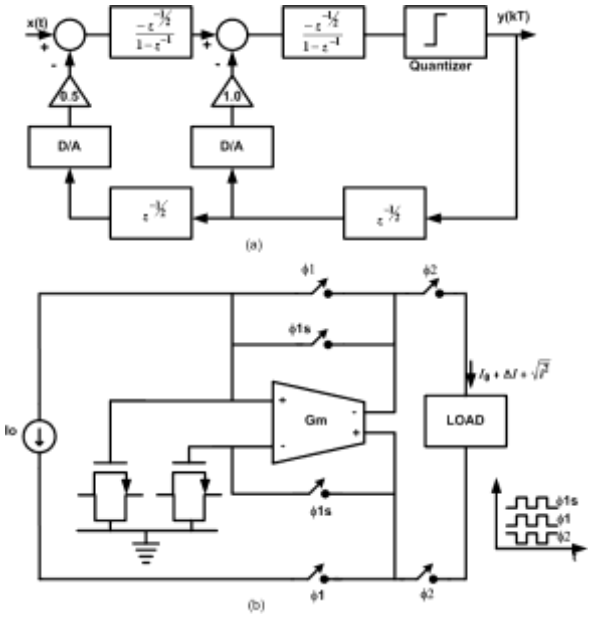

Figure 2.11 Switched Capacitor Sigma-Delta Converter (a) Modulator Architecture (b) Balanced Current Copier [21]

capacitors to charge with the help of the current Io. These two sets of switches are then opened, and $\phi 2$ is closed to allow the current flowing in the transconductor to flow through the load. Hence, a switched current integrator is implemented.

A sigma-delta converter is reported in [22] that uses switched current techniques. These A/D converters work at a supply voltage as low as 1.2 V. However, their dynamic range is much lower than their switched-capacitor counterparts due to larger thermal noise in the SI circuits.

2.2.5 Multi-Channel ADCs Prior Art

Minimal research exists on multi-channel current-mode ADCs. Some of the references on multi-channel ADCs are detailed in this section. They include a sigma-delta ADC and an integrating ADC. The sigma-delta ADC finds its application in arrays of sensors that measure electrochemical detection of electroactive neurotransmitters. The integrating ADC is used with photosensor arrays.

2.2.5.1 16-Channel ΣΔ ADC

A multi-channel first order sigma-delta ADC is proposed in [23]. For the purpose of the analysis of electrochemical activity of neurotransmitters, the required current-range of this ADC is between picoamperes and microamperes. The topology of a single channel is shown in Figure 2.12. The designed ADC architecture is a first-order, single-bit, delta-sigma modulator with a programmable oversampling ratio [23]. Each channel consists of an analog integrator, a comparator, a 1-bit digital-to-analog (D/A) converter, a counter, and a shift register. The input current is integrated first. The integrated output is input to a comparator which compares the input to a reference. The output of the comparator is modulated using a sampling frequency clock fs. The 1-bit D/A converter employs a time modulated input to subtract the current from the input current of the integrator. Depending on the output of the modulator, the current is either subtracted or added to the input current. A counter is used to count the pulses and a shift register is used to output the required channel data.

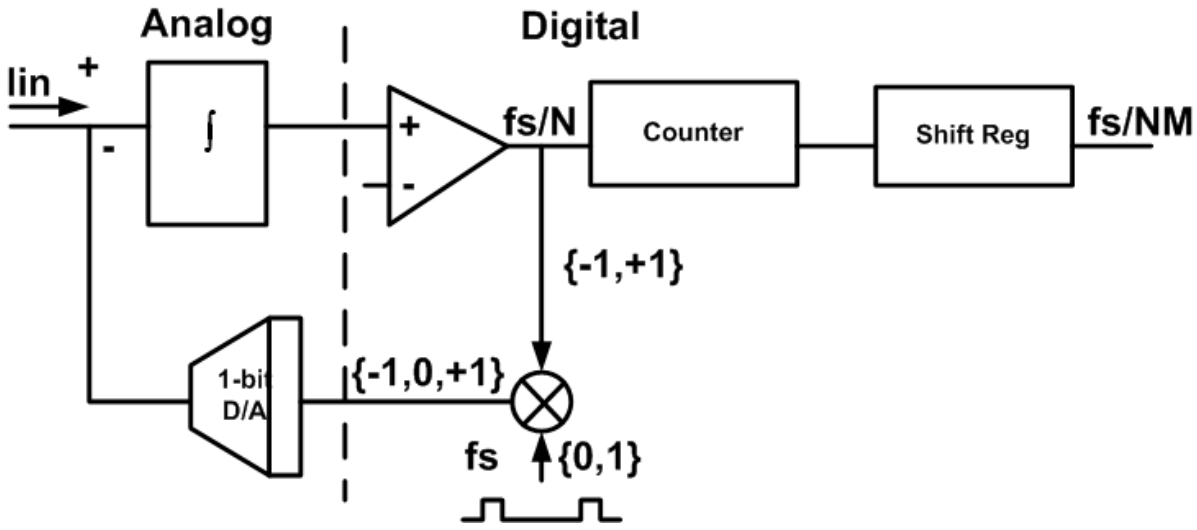

Figure 2.12 Single Channel of 16-Channel Sigma-Delta ADC[30]

2.2.5.2 Integrating ADC

There are few publications on integrating or ramp-type current-mode ADCs. An integrating ADC is proposed in [23]. The block diagram of the topology of this ADC is shown in Figure 2.13. This design allows the conversion of currents down to the subpicoampere range. This is achieved using a single transistor which integrates and amplifies the input current.

The switch S1 is first closed to reset the transistor and the capacitor Cint. The constant current Io, flowing in the transistor T1, charges the capacitor Cint. The switch S1 is then opened and the switch S2 is closed. The input current Iin causes a decreasing charge on the capacitor Cint. Assuming that the input current is linearly changing with time and the gate voltage does not change, the output current Iint resembles a current ramp. A window current comparator is implemented at the output of the transistor. The comparator trips when the current ramp crosses the lower nonzero level, and then resets to zero when the ramp crosses the non-zero upper level of the window comparator. The time between the two transitions is recorded by the counter at the output of the comparator.

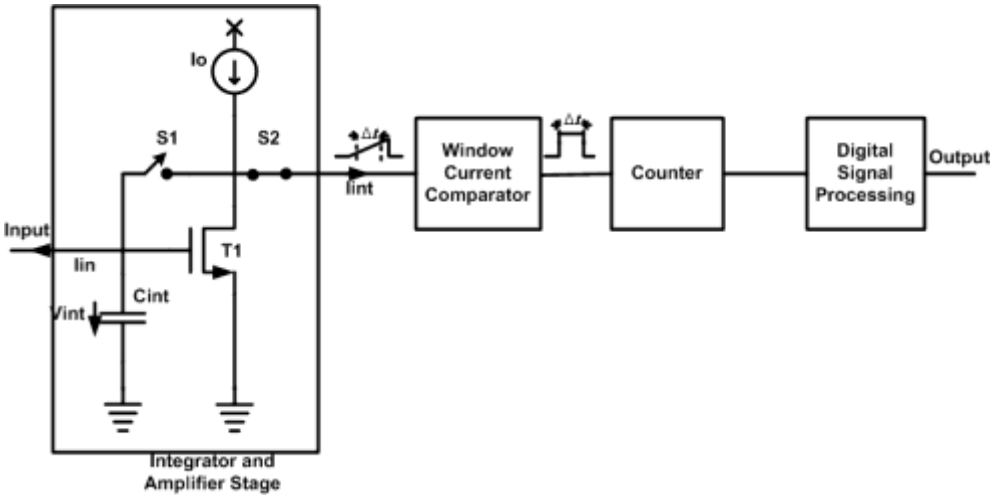

Figure 2.13 Block Diagram of the Integrating ADC [12]

For multiple channel operation this topology results in area efficiency, and the possibility of operations at a very low supply voltage. In addition, it enables a wide dynamic range of operation [23]. However, a counter at the output of each channel implies that a considerable amount of power is consumed by each channel, resulting in the large total amount of power consumption.

2.3 Summary of Prior Art

Table 2-1 shows the different Nyquist rate current-mode ADCs with parameters such as power, type, number of channels, feature size, area occupied, supply voltage, speed and resolution. As deduced from the table, literature on multi-channel current-mode ADCs is sparse. One is a 42-channel ADC, with each channel of the sigma-delta type. The range on this ADC is low (on the order of −100 nA to 100 nA). The power dissipation reported in the ADC is also low (11 μW per channel) for a sampling rate of 250 MHz. The second multi-channel ADC was reported in 2003. This is an integrating ADC with a window comparator. It reports a 64-channel ADC with a wide range and high sensitivity. The resolution of this ADC is 16 bits. However, the power dissipation of the ADC is high (approximately 250 mW) and increases with the clock frequency. The architecture also uses a counter per channel of the ADC, since a window comparator is used. A tradeoff has to be made, either to use multiple counters or to use a subtractor with two sets of registers.

Based on the limited number of multi-channel current-mode ADCs reported in literature, there is an apparent need for further exploration in this arena to enable merging the current-mode techniques into the existing architectures. This work describes the design, test, and measurement results for a multi-channel current-mode ADC that allows lower voltage operation, as well as has the ability to process multiple current signals and their digital conversion.

2.4 Conclusion

In this chapter, the current-mode design is explained. Different building blocks for current-mode designs are listed and explained. Further details of different types of ADCs, including multi-channel ADCs using the current-mode approach, are also provided. A summary of current-mode ADCs, including the on-chip area, the power consumption, the resolution, the speed, and the number of channels, have been tabulated. It can be observed from this table that only two of the previously reported designs support more than one channel. The following chapters will demonstrate the design and testing of the current-mode multi-channel integrating ADC.

Table 2-1 Summary of Prior Art on Current-mode ADCs

Reference	Type	No. of Chan.	CMOS Process Feature Size	Area (mm^2)	Supply (V)	Power (W)	Speed (Sps)	Res. (bits)
Bhat *et al.* `04	Flash	1	0.7µmCMOS		5	78m	80M	7
Bell *et al.* `01	Interpolating Flash	1	0.5 µmCMOS		5	93.5m	200M	5
Senger *et al.* `02	Folding Interpolating	1	0.35 µmCMOS	2	3.3	150m	75M	8
Kim *et al.* `99	Folding Interpolation	1	0.8 µmCMOS	3.5	5	33.6m	10K	8
Flynn *et al.* `96	Folding Interpolation	1	1 µmCMOS	4	5	225m	150M	8
Martins *et al.* `04	Folding Interpolation	1	0.8 µmBiCMOS	7.7	5	550	10M	8
N. Moeneclaey *et al.* `96	Sigma Delta	1	0.8 µmCMOS	6	5	136m	625K	14
Aboushady *et al.* `99	Sigma Delta	1	0.6 µmCMOS	0.35	3.3	9.1m	26M	12
Daubert *et al.* `92	Sigma Delta	1	0.9 µmCMOS	1.3	5	75m	3.4K	13
Tan `96	Sigma Delta	1	0.8 µmCMOS	1	3.3	40m	312K	9
Leme *et al.* `96	Sigma Delta	1	0.8 µmCMOS	0.25	5	4.5m		12
Dlugosz *et al.* `07	SAR	1	0.18 µmCMOS	0.1	0.55	3.5µ	200M	8
Luong *et al.* `98	Pipeline	1	0.5 µmCMOS		2.4	22m	20M	8
Gustavsson *et al.* `97	Pipeline	1	0.6 µmCMOS	0.4	2.7	10m	10M	5
Yoshii N. *et al.* `07	Pipeline	1	0.25 µmCMOS		2	60m	25M	7.6
Nairn *et al.* `88	Algorithmic	1	3 µmCMOS	0.371	5	5m	200K	6
Nairn *et al.* `90	Algorithmic	1	3 µmCMOS	0.74	5	8.7m	570K	8
Fong *et al.* `94	Algorithmic	1	1.2 µmCMOS	0.02	2.5	.5m	4.5M	4
Correia *et al.* `96	Algorithmic Pipeline	1	1.2 µmCMOS	0.655	5	50m	1M	8
Agarwal *et al.* `05	Algorithmic Pipeline	1	0.18 µmCMOS	0.0475	0.65	6 µ	125K	6
Uster *et al.* `03	Integrating	64	0.6 µm CMOS	3.04	5	265m	50	16
Gore *et al.* `04	Sigma Delta	42	0.5 µm 2P3M CMOS	9	3.3	432µ	250K	10
Vesalainen *et al.* `04	Gray Code	1	0.18 µmCMOS	.007		200 µ		8
Kim *et al.* `02	Cyclic	1	3 µmCMOS		5	500 µ	450K	8

Chapter 3

Design of Current-Mode Integrating ADC

A current-mode multi-channel Wilkinson ADC was designed to support a sampling rate of 10 KSps, and a current range of 10 µA to 150 µA with a supply voltage of 5 V. In this chapter, the first section discusses the advantages and disadvantages of current-mode and voltage-mode design. Following this, the effects of transistor mismatch are described. The design of the current-mode multi-channel Wilkinson ADC is then demonstrated. The design of each block, the current ramp generator, the current comparator, and the Gray code counter are described in detail, along with the prior art. Finally, the system level design, including the digital section and the timing diagram, are explained.

3.1 Current-mode and Voltage-mode Design

Current-mode is defined as a circuit design technique in which the signals are processed as currents. In this work, the input signals are in the form of currents rather than voltages. Current-mode design has certain advantages and disadvantages. Advantages include faster processing at lower supply voltages and lower power consumption due to the lower complexity of the circuits. A combination of the two design techniques, current-mode and voltage-mode, where the advantages of both modes are used shows a vast scope of possibilities. This work tries to incorporate voltage-mode techniques within the current-mode design in various ways to improve the design and thus, attempts to use advantages of both design types.

A significant part of the circuits in this work includes current mirrors. Mismatch in current mirrors is discussed in Section 3.2. In order to improve matching, active mirrors are used. This involves

differential pairs, or operational transconductance amplifiers (OTAs), to increase the output impedance. Since the OTAs, in conjunction with the mirror transistor, form a two stage amplifier, feedback loop stability becomes an issue. A Miller compensation capacitor can assist with loop stability. Calculations and magnitude and phase plots are given in Section 3.3.2. Both the OTA usage and the Miller compensation are voltage mode techniques which, together with the current mirror, improve the performance of the ADC to a large extent. Figure 3.1 shows an active mirror. The equation for the current mirror is shown in Equation 3.9 [17]. The equation indicates that the higher the gain *A* of the amplifier is, the better is the matching between the input and output currents i_{in} and i_{out} respectively.

$$\frac{i_{out}}{i_{in}} = \frac{r_o}{r_o + \frac{1}{Ag_m}} \tag{3.9}$$

Two additional examples of voltage-mode design used in this work are the comparator and the ramp generator. The first is the nonlinear feedback mechanism in the comparator which is used to improve the accuracy and speed of the comparator. The offset current compensation of the ramp generator is a second example where offset current is stored in the ramp reset phase so as to reduce offset current of the ramp. Aspects of these are detailed in Section 3.3.

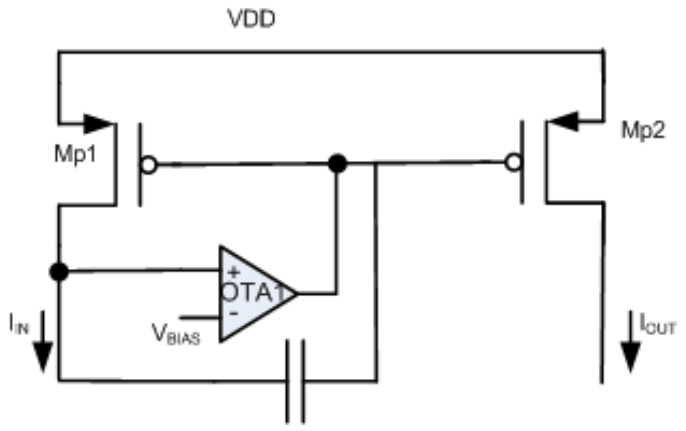

Figure 3.1 Active Mirror

3.2 Effects of Mismatch

Mismatch is a process which causes random variations in the physical properties of identically designed devices. Mismatch is a limiting factor in analog and digital signal processing. The drain current I_D of CMOS devices varies as a result of process variations. This variation of $I_{D,}$ caused by process variations, causes random offset effects. The approximate drain current of a long-channel device in saturation region is given in Equation 3.10. [17]

$$I = \frac{K}{2} \left(V_{GS} - V_T \right)^2 \tag{3.10}$$

The threshold voltage V_T and K, play the most significant role in contributing to mismatch. V_T mismatch is partly caused by the variation in body doping. The variations in dimensions, channel mobility, and gate oxide capacitance per unit area impact K, which is the conductance constant [17]. The standard deviation of threshold voltage due to random mismatch is shown in Equation 3.11 [43]

$$\sigma_{\Delta VT} = \frac{A_{VT}}{\sqrt{WL}} = \frac{qt_{ox}\sqrt{2Nt_{depl}}}{\varepsilon_0 \varepsilon_{ox}\sqrt{WL}} \tag{3.11}$$

where $\sigma_{\Delta VT}$ is the standard deviation of the threshold voltage mismatch, q is the charge, t_{ox} is the thickness of gate oxide, N is the number of active doping atoms in the depletion layer, t_{depl} is the depletion width, and ε_0 and ε_{ox} are the permittivities of vacuum and the oxide layer respectively. As observed from Equation 3.11, the variation in threshold voltage is inversely proportional to the square root of the area of the device. Threshold voltage matching improves as the device parameters W and L are increased. Figure 3.2 is a plot of the standard deviations of threshold voltage versus the inverse square root of the area. It is observed from the plot that the standard deviation reduces as the inverse square root of the area reduces.

For the design of the blocks of the ADC, care was taken to use large L values, since the accuracy of the ADC depends to a large extent on current mirrors and, hence, the matching between devices.

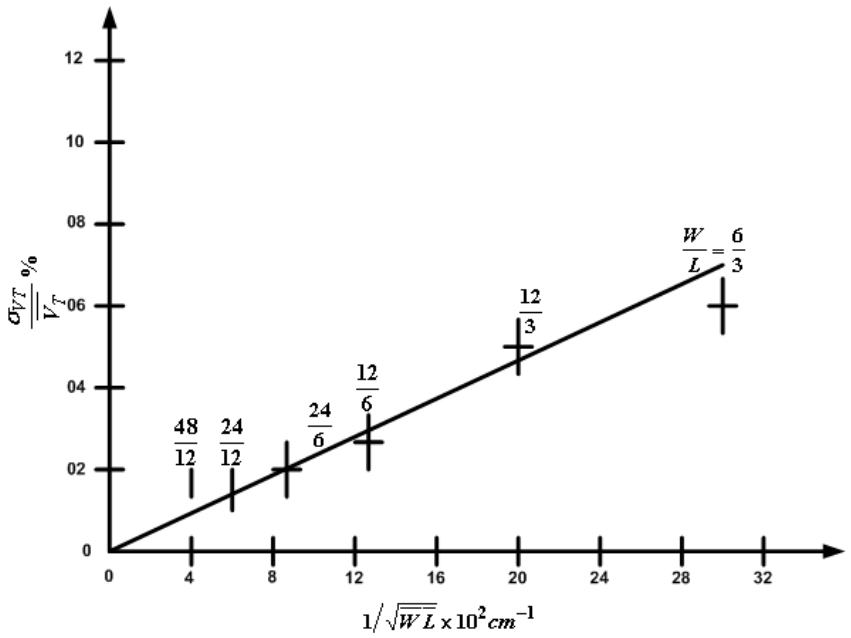

Figure 3.2 Standard Deviation of Threshold Voltage vs. Inverse Square Root of Area for NMOS Device [17]

Additionally, active mirrors are used where matching is critical so that the drain current is more accurately controlled.

3.3 Multi-channel Current-Mode ADC

As explained in Chapter 1, the key blocks of the ADC are the ramp generator, the current comparator, and the Gray code counter. The architecture of the multi-channel current-mode ADC incorporates a single ramp generator, a single Gray code counter, and the number of comparators equal to the number of channels. It also includes two sets of latches, a multiplexer, and a Gray code-to-binary converter. The following sections explain the primary circuit blocks.

3.3.1 Current Ramp Generator

3.3.1.1 Prior Art

The current ramp generator selected for this work is based on [44]. The current ramp generator of [44] is shown in Figure 3.3. The capacitance charging current in this current ramp generator topology is given as R_e/R_g^2. However, since the capacitor is directly connected to the drain of the PMOS that forms the current mirror, increasing the voltage on that node causes channel length modulation of the transistor. This varying V_{DS} causes variation in the charging current due to channel length modulation, and in turn, creates nonlinearity in the output current ramp. The new architecture of the current ramp generator addresses the cause of this nonlinearity by using a common gate transistor between the charging capacitor and the current source, hence isolating the drain of the source transistor from the varying capacitor voltage. In addition to the nonlinearity, the accuracy of the charging current, which is related to the matching between current mirror transistors, is improved.

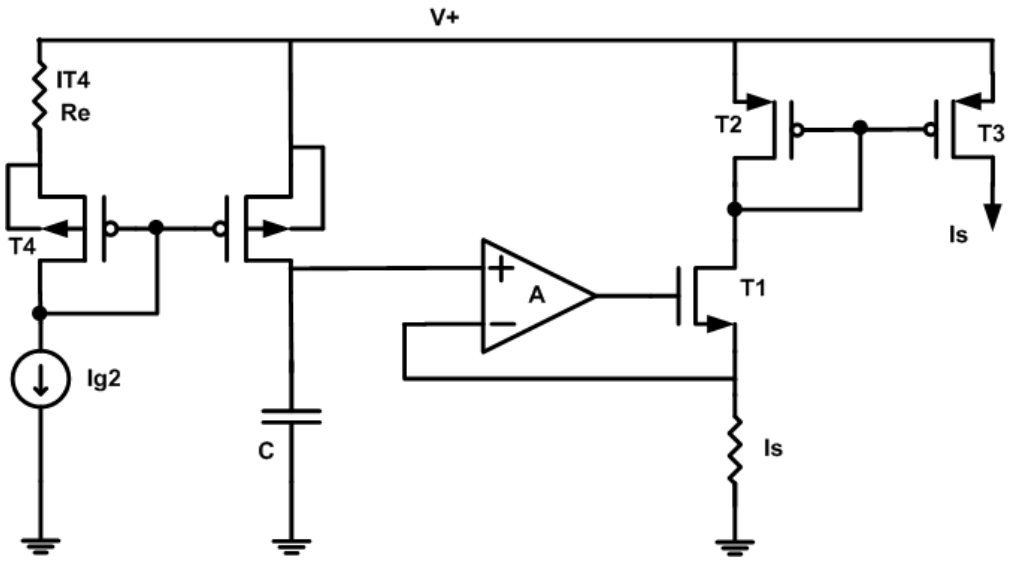

Figure 3.3 Current Ramp Generator [44]

3.3.1.2 Current Ramp Generator

The ramp generator used in this work, adapted from [44], is shown in Figure 3.4. A negative feedback loop establishes a V_{tune}/R_1 current through Mp1 that is reflected by Mp2 through Mp1CG to charge C1. Voltage at R1 is equal to voltage V_{tune}. The voltage (V_{tune}) is adjusted to vary the range of the ADC. The current flowing through this resistor is copied to the Mp2 branch. OTA1 is used to improve the accuracy of the current mirror. The current flowing through Mp1 and Mp1CG charges the capacitor C1.

Mp1CG is used to isolate the capacitor node from the drain node of Mp2. This transistor, in addition to serving as a pseudo-cascode configuration, also aids in reducing the nonlinearity of the ramp due to the drain voltage modulation of Mp2. Mp1CG acts as though it is configured in common gate configuration. Figure 3.5 shows the current through the source Mp2 in the absence of the common gate transistor Mp1CG. It is observed that the charging current varies linearly with the voltage on the drain of the transistor. The variation is 62nA. The variation is caused by the V_{DS} variation of the transistor Mp2.

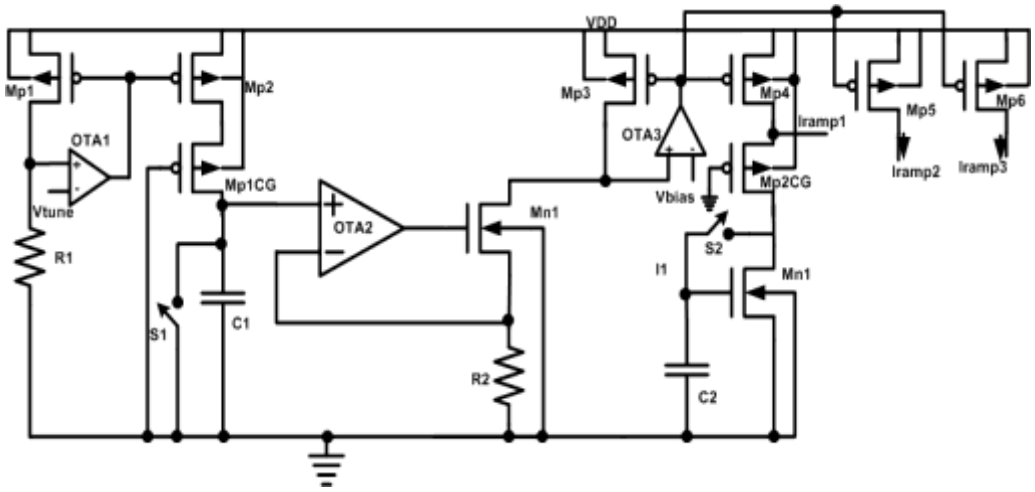

Figure 3.4 Current Ramp Generator

Figure 3.6 shows the variation of the current charging the capacitor, with the common gate transistor isolating the drain node of the PMOS transistor from the capacitor. Note that the variation of the current is in less than 1nA, which is much smaller than the variation without the isolation transistor improving the linearity of the ramp generator.

Switch S1 is used to reset the capacitor. The terminal Vtune is padded out for test purposes. OTA2 copies the ramp voltage to the top of resistor R2. The linear voltage ramp is thus converted to a linear current ramp. Mn1 must be sized such that it will remain linear over the entire range. Mp3, Mp4, and Mp5 are the current ramp branches. Each *Iramp* branch goes to a current comparator of each channel. Since the current ramps are separated, there is less coupling between the channels, and expanding the number of channels does not impact the loading of the voltage ramp. OTA3, similar to OTA1, helps improve current mirror accuracy. Large OTA gain increases the accuracy as shown in equation 3.9.

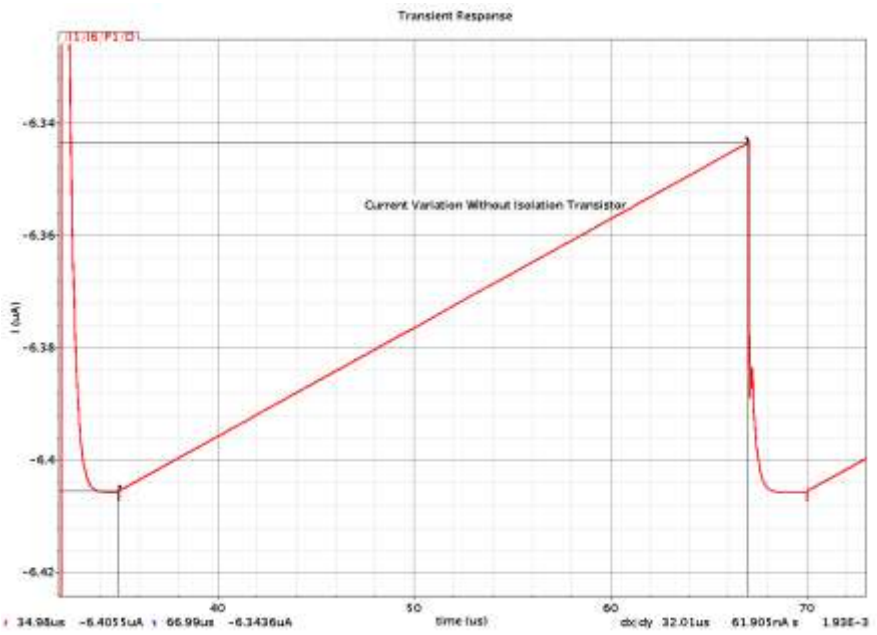

Figure 3.5 Charging Current Variation in the Absence of the Isolation Transistor

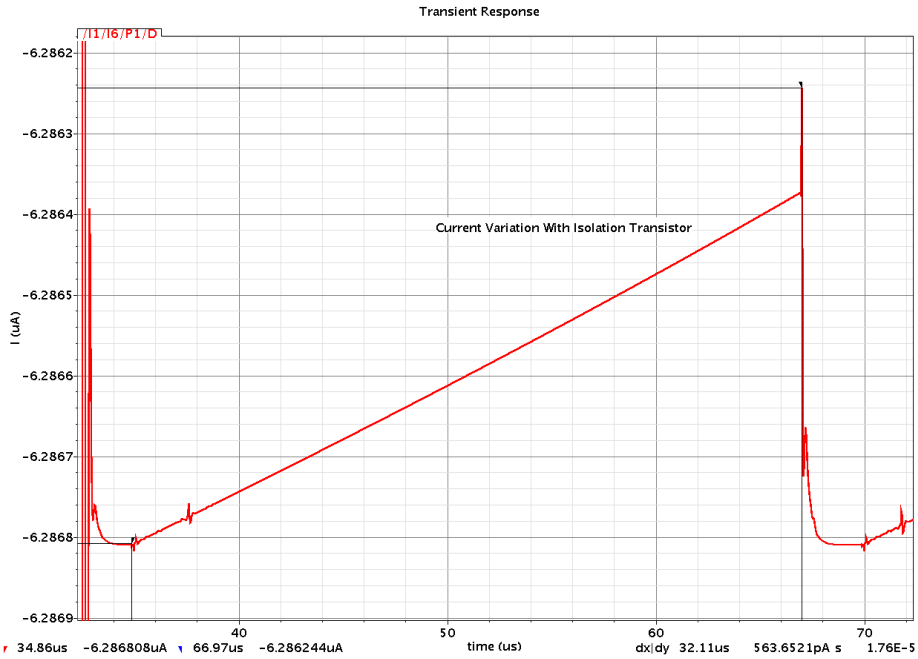

Figure 3.6 Charging Current with the Common Gate Transistor

OTA1 and OTA3, with Mp1 and Mp3, respectively, form two-stage amplifiers. These amplifiers require frequency compensation. Frequency compensation is done by introducing capacitors between the gate to the drain nodes of Mp1 and Mp3. Utilizing the Miller effect, these capacitors are multiplied by the gain of the transistor and provide adequate compensation for each two-stage amplifier. Further explanation regarding compensation is given in Section 3.3.2.3.

The NMOS transistor Mn1 with capacitor C2 and switch S2 provides an offset compensation for the ramp generator. In offset removal mode, switch S2 is closed, enabling any current flow due to the offset of OTA2 to be stored on the capacitor C2. Another common gate stage is introduced between the NMOS transistor Mn1 and transistors Mp4, Mp5, and Mp6 to provide isolation between the offset compensation transistor and the input of the comparator. Mp2CG, Mn1, S2, and C2 are repeated for each channel.

The temperature dependence of the ramp generator is calculated using resistors R1, R2, and C1. As shown in Equation 3.12, the current flowing through resistor R1 and the capacitor charging current is calculated, where R_1 is dependant on temperature and denoted as $R_1(T)$.

$$I_{charge} = \frac{V_{tune}}{R_1(T)} \tag{3.12}$$

Voltage through the capacitor is derived via Equation 3.13 and used to obtain Equation 3.14

$$\frac{V_{tune}}{R_1(T)} = C_1 \frac{dV_{C1}}{dt} \tag{3.13}$$

$$V_{C1} = Kt \tag{3.14}$$

where, $K = \frac{Vtune}{R_1(T)C_1}$ and t is time. Hence, output current flowing through resistor R2 is given as in Equation 3.15

$$I_{R2} = \frac{1}{R_2(T)} V_{C1} = \frac{Kt}{R_2(T)} = K_1 t \tag{3.15}$$

where, $K_1 = \frac{V_{tune}}{R_1(T)R_2(T)C_1}$. The temperature dependence of this ramp is obtained by differentiating Equation 3.15 over temperature T. This is provided in Equation 3.16. As a result, Equation 3.17 describes the variation of the current ramp over temperature. In this equation, time is assumed to be constant.

$$\frac{dI_{R2}}{dT} = \frac{d}{dT}(K_1 t) = \frac{V_{tune} t}{C_1} \frac{d}{dT}\left(\frac{1}{R_1(T)R_2(T)}\right) \tag{3.16}$$

$$\therefore \frac{dI_{R2}}{dT} = \frac{V_{tune} t}{C_1}\left(\frac{-R_1 \frac{dR_2}{dT} - R_2 \frac{dR_1}{dT}}{(R_1 R_2)^2}\right) \tag{3.17}$$

From equation 3.17, if V_{tune} and C_1 are assumed to be relatively constant over temperature, the second term in the parentheses describes the variation of the ramp over temperature. In order to calculate the approximate numerical value of the variation of the current ramp over temperature, the values of the different variables are substituted in Equation 3.17. The approximate variation of the resistor values over temperature are used from [10]. The values of the variables within the parentheses are given in Equation 3.18.

$$R_1 = 400\times10^3 \; R_2 = 10\times10^3$$
$$\frac{dR_1}{dT} = \frac{dR_2}{dT} = -2000 ppm/°C \tag{3.18}$$

For the temperature range of -55ºC to 125ºC, the variation of resistance is calculated as shown in Equation 3.19.

$$\frac{dR_1}{dT} = \frac{dR_2}{dT} = -2000\times10^{-6}\times(125+55) = -0.36 \tag{3.19}$$

By substituting Equations 3.18 and 3.19 into Equation 3.17, the value of the variation in the current ramp is obtained as in Equation 3.20.

$$\left(\frac{-R_1\frac{dR_1}{dT} - R_2\frac{dR_2}{dT}}{R_1R_2}\right) = \left(\frac{-(400\times10^3\times-0.36) - (10\times10^3\times-0.36)}{400\times10^3\times10\times10^3}\right) = 9.225\times10^{-15} \tag{3.20}$$

For the range of 10 µA to 150 µA, a 12-bit resolution implies that a minimum current of 34nA has to be deciphered. The magnitude of the variation, as obtained in Equation 3.20, is negligible when compared to this current, showing the advantage of the current ramp over the voltage ramp. From Equation 3.15, the range of the ramp current depends on the values of R1, R2, the ramp capacitor C1, and the tuning voltage. Hence, varying the tuning voltage facilitates tuning the ramp and input current ranges.

Simulations of the ramp generator show a 10-bit accuracy for a ramp range of 10 µA to 200 µA. The simulation also shows a 12-bit accuracy for the lower range of 10µA to 100µA. Further improvements on the ramp generator which improve linearity are described in Chapter 5.

3.3.2 Current Comparator

The current comparator is an important building block of the ADC. Different types of current comparators include the resistive input and capacitive input comparators [45]. One current comparator for each channel is used in the current-mode Wilkinson ADC. Low power on this block reduces the overall power consumed by the ADC. Current comparison depends on the accuracy of current mirrors which in turn depends on process variation, threshold voltage mismatch, and layout. These parameters affect current mirrors and reduce the accuracy to 8 bits or lower. Active current mirrors are proposed in [16]. The accuracy of current mirrors is improved using active current mirrors [16].

3.3.2.1 Prior Art

The current mirror comparator is the first current comparator proposed in [46] . This comparator has a slow response time and depends to a certain extent, on the input level of the current. The Traff current comparator proposed in [47] is a high-speed current comparator owing to its positive feedback. Figure 3.7 shows the Traff comparator. The input stage of the comparator is a source follower. This ensures low input impedance to the comparator. The inverter and source follower are arranged so that positive feedback is created. [47]

In addition to positive feedback, the Traff comparator also offers low input impedance. A disadvantage of this topology, however, is the nonzero quiescent current that flows through the output transistors M3 and M4 since the input voltage does not slew rail to rail. The non-zero quiescent current results in a higher power dissipation.

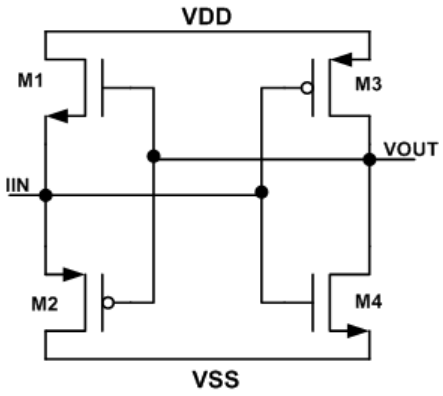

Figure 3.7 Traff Current Comparator [47]

[45] classifies the current comparators into two categories based on whether their input sensing node is resistive or capacitive. The resistive input comparators show good speed at large current levels, but are inaccurate. The capacitive input comparator improves the resolution considerably when compared to the resistive input, but lowers the speed of operation. A variety of topologies are proposed which combine the advantages of the capacitive and resistive input architectures. The two different types of comparators in this class are the current-switching comparator and the current-steering comparator.

The current-switching comparator is shown in Figure 3.8. Non-linear feedback allows the topology to have capacitive input at low current levels and a resistive input at high current levels. As a result of the Cgs capacitance, there is coupling between the input and the output of the amplifier. Isolating the input and output nodes help improve the performance of the comparator. Using the source node of the devices at the input side presents low input impedance to the current subtractor stage. The current subtractor subtracts the input current from the reference current. This enables the difference current to flow into the current comparator. If the difference current is greater than zero, the output of the comparator changes to *high.*

The current-switching comparator has a disadvantage. The Miller capacitance of the NMOS and PMOS feedback transistors couples the input to the output. A different configuration is proposed in [45] that eliminates the input to output coupling. A current-steering comparator assists in isolating the input and output nodes. This topology has the sources of the feedback transistors tied to the input node. Instead of connecting the transistors' gates to the output of the amplifier, the drains are connected to the output of the amplifier. The Miller capacitance effect is thus eliminated, which coupled the input to the output in the current-switching comparator. Figure 3.9 depicts a current steering comparator. The biasing of the transistors is shown in Figure 3.10.

This topology uses a differential pair followed by a current starved inverter as an amplifier. The feedback transistors are biased by the voltages E1 and E2. Vbp and Vbn are used to bias the current mirrors and set the current flowing through the amplifier. These four biases are generated as shown in Figure 3.10. The current steering comparator shown in the figure uses a dual supply so that the ground is at mid-supply voltage.

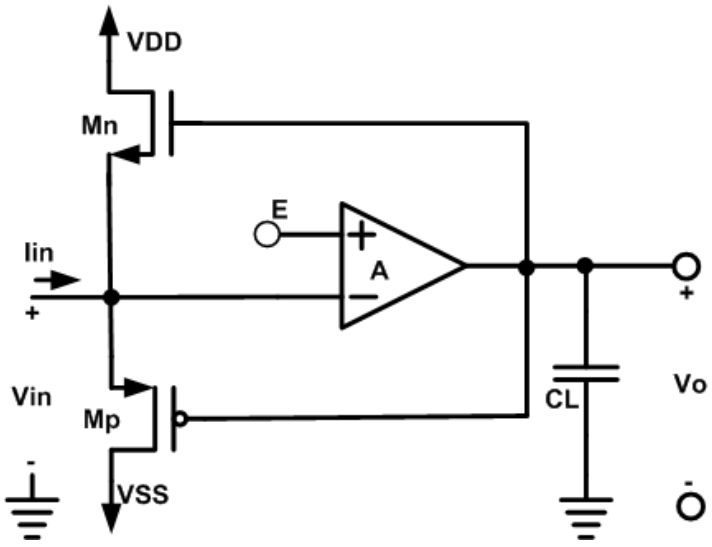

Figure 3.8 Current-Switching Comparator [45]

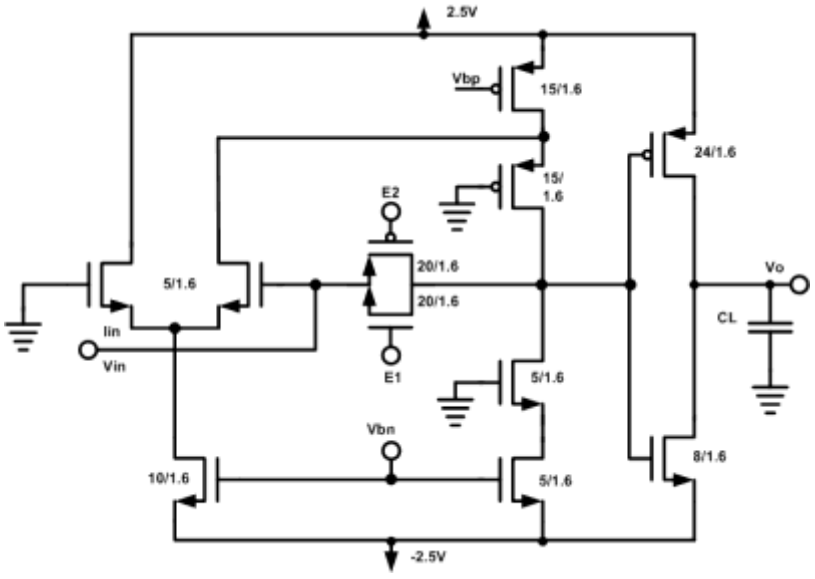

Figure 3.9 Current Steering Comparator [45]

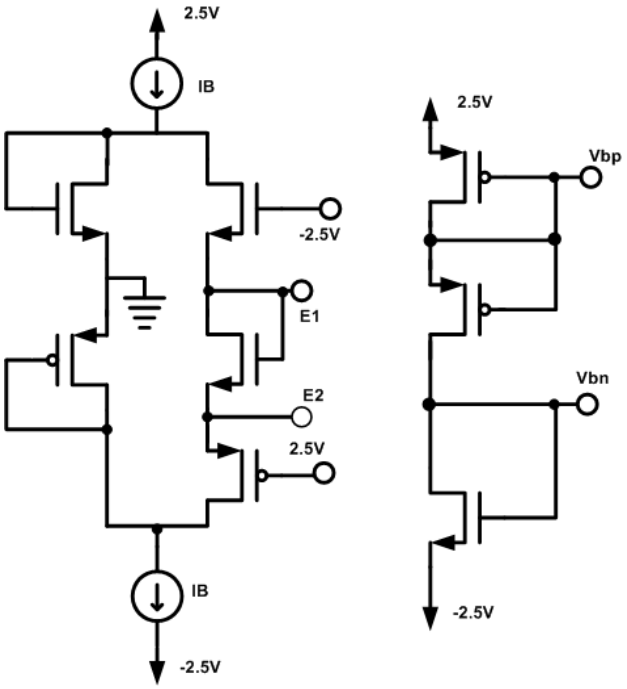

Figure 3.10 Current Steering Comparator Biasing Scheme [45]

3.3.2.2 Current Comparator with Differential Pair as Amplifier

The current comparator circuits described in the prior art assume an input current to the current comparator that is ideal. They also assume that the current is referenced to ground. None of the prior art work discusses the current subtractor which has to be implemented at the input if the current is not referenced to ground or, the current mirrors required. Nor does it discuss the effects of mismatch that accompany the usage of current mirrors. Furthermore, for usage of these comparators in data converters, a sample and hold block is required before the comparator. This issue is not addressed. Current mirrors used in the current comparator are discussed in Section 3.2. The sampling function, an integral part of the comparator, is explained in this section along with the current comparator.

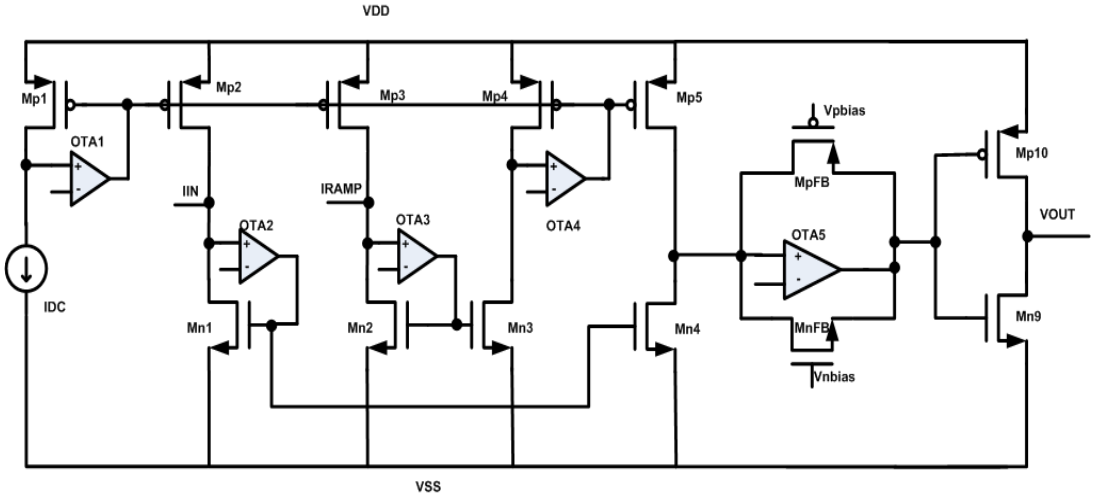

Figure 3.11 Current Steering Comparator with OTA Amplifier.

In contrast to the approach in Figure 3.9, this work employs a differential pair as an amplifier in place of the current starved inverter. The amount of current flowing in the block is reduced, which implies better controlled power consumption. Figure 3.11 shows the current comparator with an OTA as the feedback amplifier.

The current-mode ADC does not require a sample and hold circuit since the function sampling is performed in the comparator. Figure 3.12 shows a more detailed schematic of the transistors Mp1 and Mp2. The gate of transistor Mp2 is tied to a sampling capacitor and the switch S1. The other end of switch S1 is tied to the gate of transistor Mp1. In the sampling phase, switch S1 is closed and stores the gate voltage of the transistor Mp1 on the gate of Mp2. This topology is in the form of a current copier, (Section 2.1.1). The current flowing in Mp1 is copied to Mp2. At the end of the sampling period, the switch S1 is opened. Then the gate voltage stored on Mp2 allows the same current to flow until the start of the next sampling period. As for any switched capacitor circuit, however, there may be a small amount of error due to clock feedthrough, leakage, and other similar effects.

In Figure 3.11, OTAs 1 and 4 are NMOS input OTAs, whereas OTAs 2, 3, and 5 are PMOS input OTAs. Figure 3.13 (a) and (b) illustrates the NOTA and POTA used in the current comparator topology. The

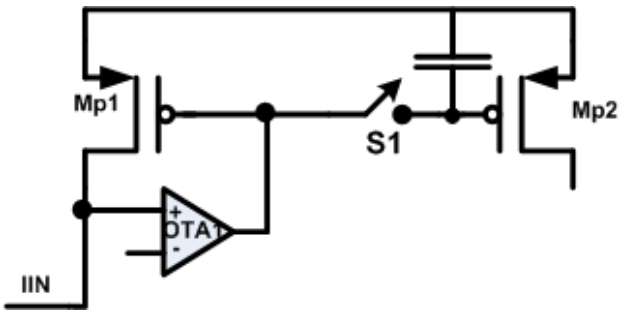

Figure 3.12 Current Sampling Comparator

OTAs used in the active current mirrors improve the matching between the devices to obtain at least 10

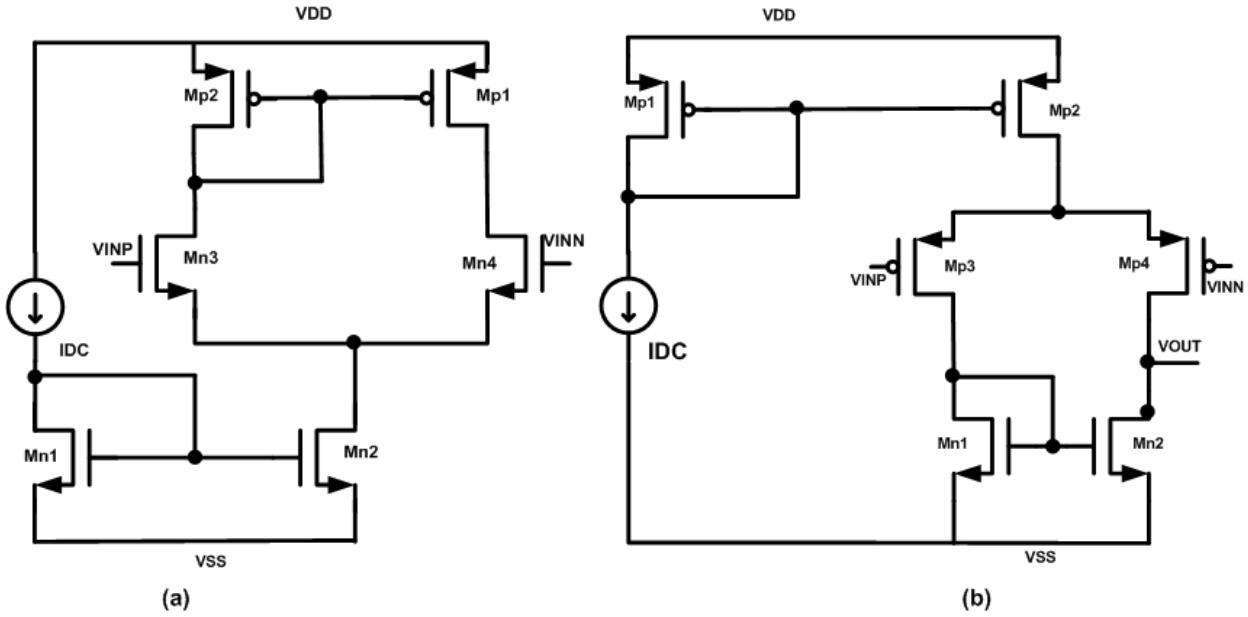

Figure 3.13. (a) NOTA (b) POTA

bits. The higher is the gain of the OTAs, the greater is the current matching. OTA5, along with transistors MpFB and MnFB, performs a nonlinear feedback when the ramp current is greater than the input current. When the input current is low, it acts as a capacitive input comparator and provides a higher accuracy at low current levels. As the ramp current exceeds the input current, the feedback loop is closed. Hence, the structure acts more as a resistive input, thereby combining the advantages of both the resistive and capacitive input architectures.

The current comparators show a 10-bit accuracy based on the simulation. However, simulation accuracy relies heavily on the models used. Further details of the testing and measurement results are provided in Chapter 4.

3.3.2.3 Differential Pair Frequency Compensation

The differential pairs are used in both the current mirrors and the amplifier. The gain of the OTA pair is calculated to provide an estimate of the speed, and to determine the compensation capacitor required to stabilize the active current mirror. The active current mirror consists of the OTA and the transistor across which the OTA is connected.

Figure 3.14 illustrates the POTA with the current mirror load. Transistors Mn3, Mn4, Mp5, and Mp6 form the current mirror loading the OTA. The current mirror is redrawn to calculate the required gain and compensation. The gain of the POTA is given by Equation 3.21. A capacitance of 1pF is introduced to compensate the configuration. Values of *gm* and *rds*, for the computation of gain and poles, are obtained from the DC operating point calculated by Spectre, the simulation tool used for design.

$$Av_{dp} = gm_{P3} \times (rds_{N1} \| rds_{P3})$$
$$Av_{dp} = 12.48 \times 10^{-6} \left(\frac{1}{26.85 \times 10^{-9}} \left\| \frac{1}{44.34 \times 10^{-9}} \right. \right) = 175.3 \qquad (3.21)$$

When the OTAs are used in conjunction with the current mirror transistor, they form a two stage amplifier. The second stage is a common source (CS) amplifier. The gain of the CS amplifier is given in Equation 3.22.

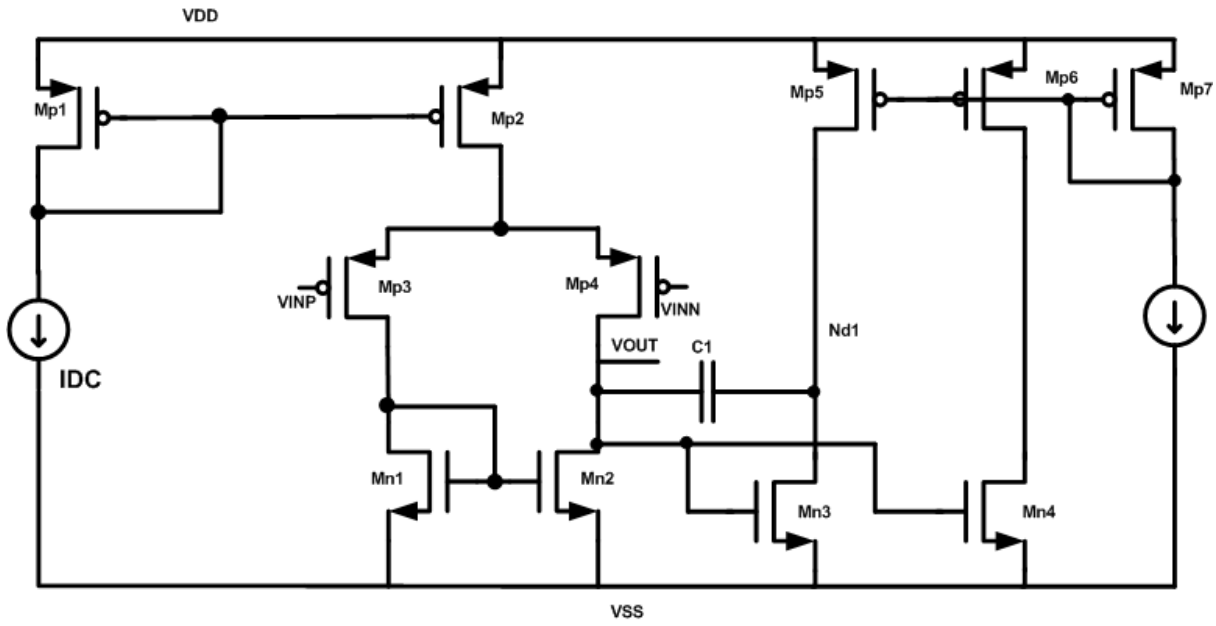

Figure 3.14 POTA with Current Mirror Load

$$Av_{CS} = gm_{N3} \times \left(rds_{N3} \| rds_{P5} \right)$$
$$Av_{CS} = 36.46 \times 10^{-6} \left(8.09 \times 10^{6} \| 11.7 \times 10^{6} \right) = 174.5 \quad (3.22)$$

For frequency compensation, the dominant pole node is identified and is labeled as *Vout* in Figure 3.14. The total capacitance at the node is calculated in Equation 3.23.

$$C_{Vout} = Cds_{N2} + Cds_{P4} + Cgd_{P4}\left(1 - \frac{1}{Av_{N2}}\right) + Cgd_{P4}\left(1 - \frac{1}{Av_{P4}}\right)$$
$$+ Cgs_{N3} + Cgs_{N4} + Cgd_{N3}\left(1 - Av_{N3}\right) + Cgd_{N4}\left(1 - Av_{N4}\right) \quad (3.23)$$
$$C_{Vout} = 0.968pF$$

The total resistance at the node, and hence the pole frequency, is calculated in Equation 3.24.

$$R_{Vout} = rds_{N2} \| rds_{P4} = 14.046M\Omega$$
$$f_{Vout} = \frac{1}{2 \times \pi \times C_{Vout} \times R_{Vout}} = 11.7KHz \quad (3.24)$$

The magnitude and phase plot of the uncompensated 2-stage amplifier formed by the OTA and the current mirror is shown in Figure 3.15. The cutoff frequency of the first pole, obtained by hand analysis, is approximately equal to the plot obtained using the simulator. The red plot represents the phase plot while the blue plot represents the magnitude plot. The phase margin, as shown in the simulation, is more than 180º, which implies that the configuration is unstable and needs frequency compensation for operation.

The addition of a 1pF capacitor between the gate node of transistor Mn3 and the drain of the same transistor achieves the required compensation by reducing the frequency of the dominant pole. The net capacitance at the node *Vout* is given by Equation 3.25.

$$C_{Vout} = Cds_{N2} + Cds_{P4} + Cgd_{P4}\left(1 - \frac{1}{Av_{N2}}\right) + Cgd_{P4}\left(1 - \frac{1}{Av_{P4}}\right) + Cgs_{N3} + Cgs_{N4} + Cgd_{N3}\left(1 - Av_{N3}\right) + Cgd_{N4}\left(1 - Av_{N4}\right) \quad (3.25)$$

$$C_{Vout} = 175.468pF$$

With this value of node capacitance, the dominant node moves to the frequency given by Equation 3.26.

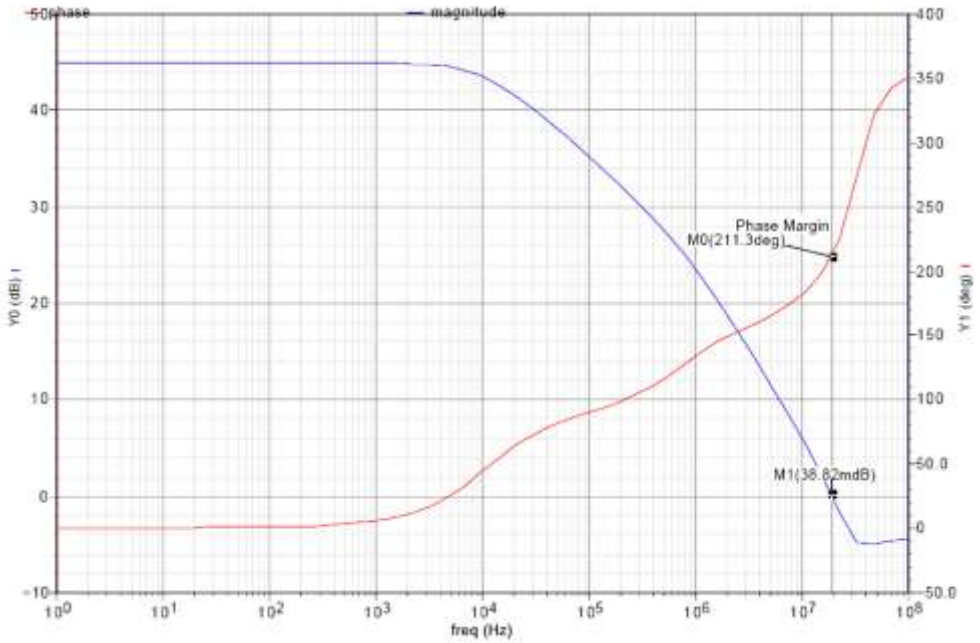

Figure 3.15 Phase and Magnitude Plot for 2-Stage Amplifier with No Compensation.

$$f_{Vout} = \frac{1}{2 \times \pi \times 175.468 \times 10^{-12} \times 14.046 \times 10^{6}} = 64.5Hz \qquad (3.26)$$

The phase and magnitude plot of the configuration is shown in Figure 3.16. Again, the red plot represents the magnitude plot and the blue plot represents the phase plot. The phase margin obtained using capacitor compensation is 57.5º. This phase margin, which is greater than 45º, is adequate to compensate the active current mirrors and guarantee stability.

3.3.2.4 Output Stage

The output stage consists of OTA5 with positive feedback and an inverter. OTA5 is the POTA. The feedback transistors, MpFB and MnFB, form a positive feedback. The inverter at the output of this stage gives a sharp edge to the comparator. Another inverter is added at the output of the first inverter to invert the output. The transistors MnFB and MpFB are biased using 3 diodes a PMOS diode at the top followed by two NMOS diodes. Figure 3.17 shows the voltages applied to bias the feedback transistors.

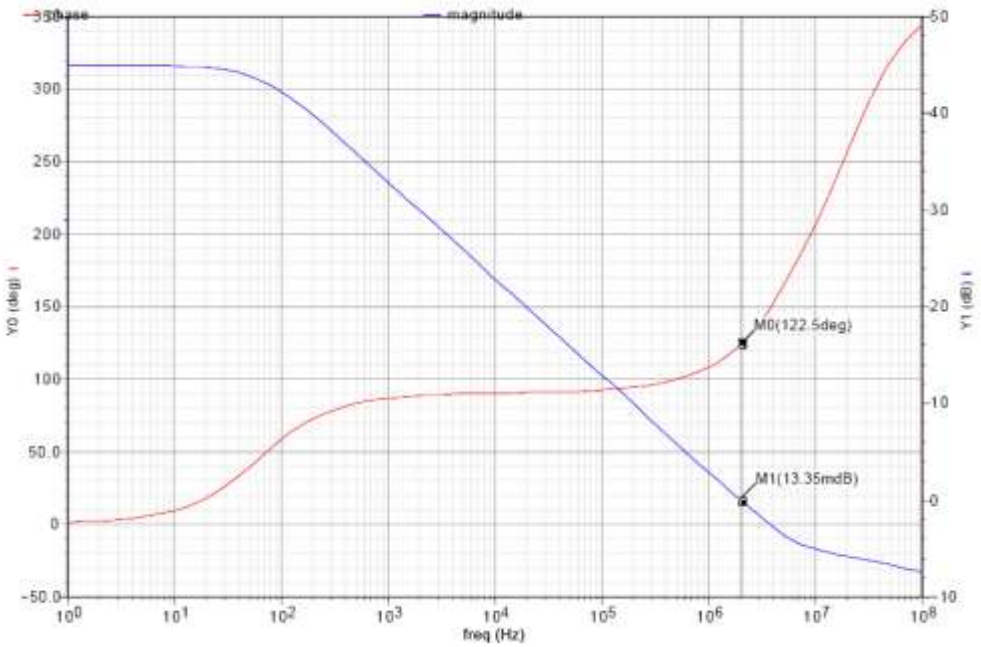

Figure 3.16 Phase and Magnitude Plot for 2-Stage Amplifier with Compensation

3.3.3 Gray Code Counter

After the current ramp generator and the current comparator, the Gray code counter plays a key role in the operation of the ADC. Binary counters have multiple bits changing at the same time. A delay in a bit changing may cause missing codes in the ADC. Missing codes in an ADC results in glitches in the DNL and causes nonlinearity. Since only one bit changes at a time [48], Gray code counters show better results than binary counters. One of the main problems faced in the design of Gray code counters is the frequency of operation.

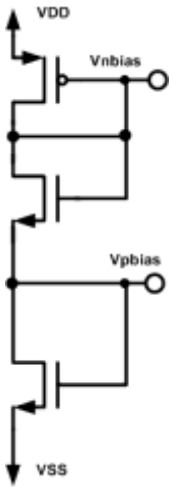

Figure 3.17 Current Comparator Output Stage Bias

Generally, Gray code counters have feedback from the higher bit stages to the lower bit stages, and feedforward networks from lower significant bits to upper significant bits. [49] proposes a Gray code counter without feedback. However, each stage of the counter increases in complexity as compared to the previous stage. As the number of bits of the counter increases, the number of logic gates also increases. Each stage has a unique logic gate configuration of its own, which increases complexity as the number of bits increases. This feedback, feedforward, and complexity limit the frequency of operation of the counter. As a result, increasing the number of the bits of the Gray code counter reduces the frequency of operations even further.

A Gray code counter is proposed in [50]. The Gray code counter is shown in Figure 3.18. This Gray code counter eliminates the feedback from the more significant bits to the less significant bits and improves the speed of operation. This topology takes advantage of the relationship between binary codes and Gray codes. When the counter output increases, a bit in the binary count changes from logic “0” to logic “1”. The corresponding bit in the Gray code changes state from logic “0” to logic “1”.

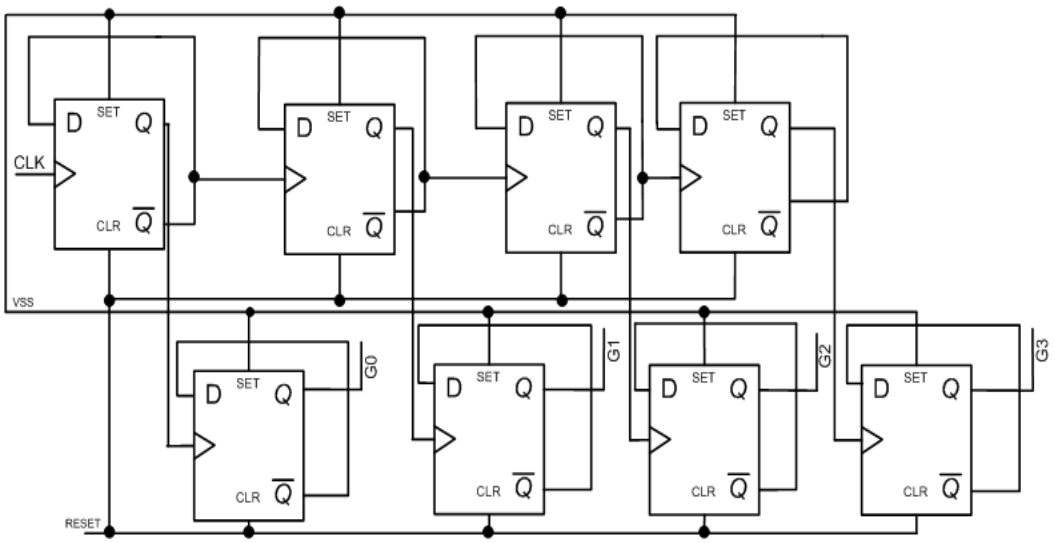

Figure 3.18 Gray Code Counter [50]

Similarly, when the counter output is decreasing, a bit in the binary code changes from logic "1" to logic "0". The corresponding bit in the Gray code changes from logic "1" to logic "0. Two sets of D-flip-flops are used. This is advantageous since adding number of bits does not add to the complexity to the circuit. Also, no feedback or feedforward is involved in this architecture.

In this topology, the clock to each stage is fed from the output of the preceding stage flip-flop. The propagation delay of each flip-flop results in a clock skew effect. Hence, the larger the number of bits, the greater is the delay in the clock reaching the higher bits. This effect is defined as clock skew. Missing codes may result from this clock skew effect.

To perform synchronous operation, the counter must be converted. This is implemented by the addition of two logic gates per stage. The addition of the XOR and the AND gate per stage does not increase the complexity and at the same time, improves the maximum frequency of operation of the Gray code counter by reducing the clock skew effect. The clock skew effect is caused by the propagation delay of the flip-flops. The output of the XOR gate, which drives the D input of the flip-flop, reduces in width

as the number of stages increases. As a result, several missing codes are observed. To fix this issue, the clock input of the stages G2 through G8 are driven by the output of stage G1. The clock input of G9 through G11 is fed from the output of G8.

The Gray code counter, used in the current-mode ADC, does not include the complicated feedforward and feedback network. Figure 3.19 illustrates the first four stages of the Gray code counter architecture. The Gray code counter is based on [50]. It is modified to reduce the probability of missing codes resulting from clock skew effect by using a carry-look-ahead technique. The complexity of the counter topology is lower, therefore it uses lower power and has the capability to count without missing codes at higher frequencies. Simulations of the 12-bit counter show no missing codes up to a 200 MHz frequency.

3.3.4 Digital Section

In any mixed signal system the digital blocks have to perform in conjunction with the analog section. The digital section in this ADC consists of a number of blocks. The operation of the digital section, excluding the counter, is explained in this section, followed by the timing diagram.

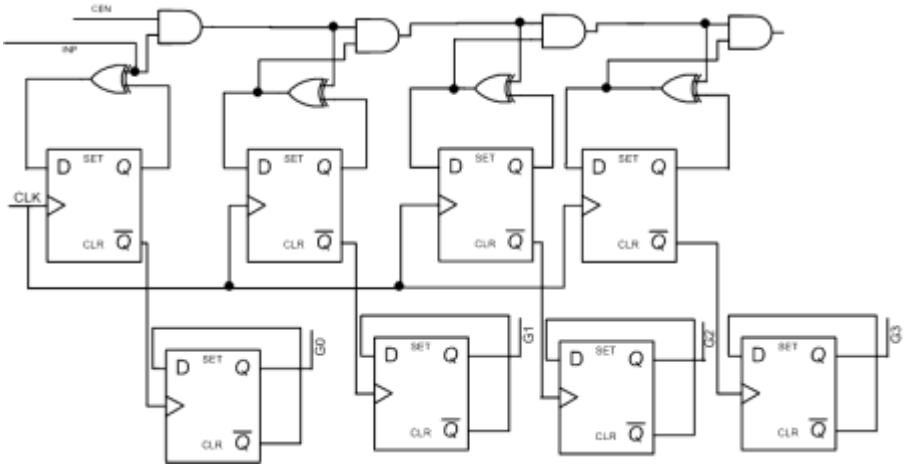

Figure 3.19 Gray Code Counter

3.3.4.1 Digital Blocks

The digital section consists of latches, tristate buffers, a multiplexer, and a Gray code to binary decoder. Figure 3.20 shows the block diagram of the digital section of the ADC. The current comparators, COMP1 through COMP4, drive the first set of latches. Each latch shown in the figure consists of 12 D-flip-flops for 12 bits. These latches are fed by the counter. When the comparator changes state, the latches store the output of the counter at that time instant. The latch in each channel contains data corresponding to the analog input to the adjacent comparator. During the next sample and conversion cycle, the data is transferred to the second set of latches. This occurs when the REFRESH signal becomes *high*. The data in one cycle is read in the following cycle. After the second set of latches has locked the data, the first set of latches is reset with the help of the RESET signal.

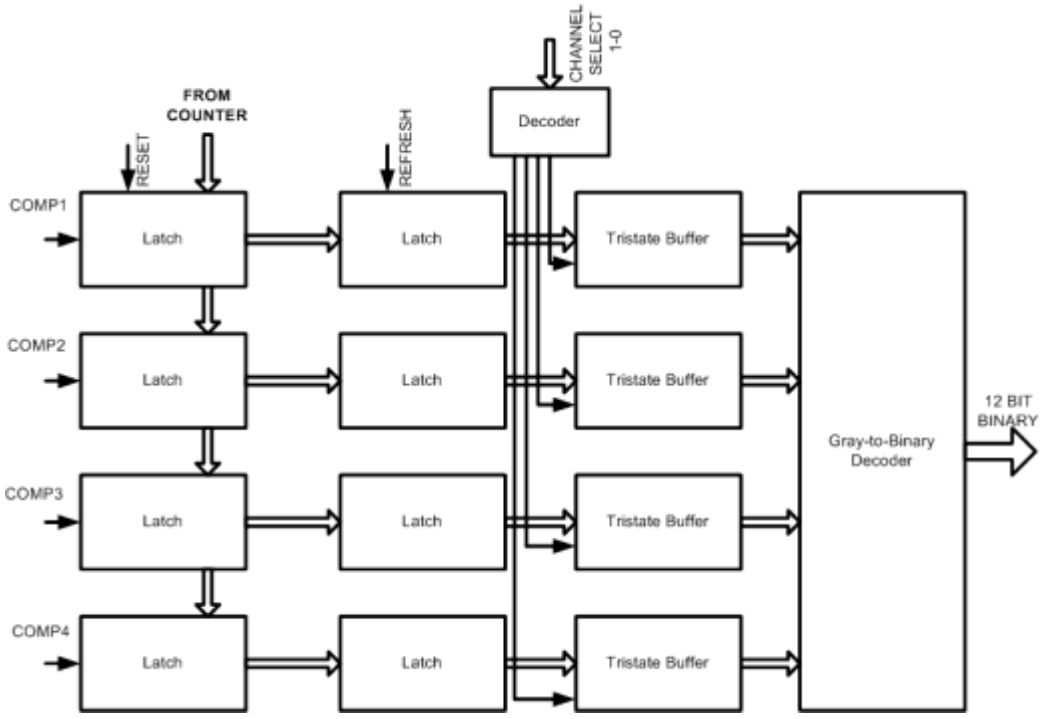

Figure 3.20 Digital Section ADC

The output of the latches is the input to the tristate buffers. The tristate buffers are fed the output of a decoder. The input to the decoder is the CHANNEL SELECT signals, varied from 00 to 11 to select all four channels. Depending on the input to the decoder, the tristate buffers output data. The output of the tristate buffers is Gray code. For ease of testing, the Gray-to-binary decoder is used. The output of the Gray-to-binary decoder is 12-bit binary data. The Gray-to-binary converter is a set of XOR gates.

3.3.4.2 Timing Diagram

The timing diagram for the functionality of the ADC is illustrated in Figure 3.21. Timing t1 to t4 is the sampling cycle where the input is sampled and the digital section is made ready for the next sample and conversion cycle. In the sampling cycle, the ramp is first disconnected from the comparator. Following this, the input sampling (ICS) and ramp discharge switch (RAMP F/B SWITCH) are set to *high*. The ICS enables input current sampling and the RAMP F/B SWITCH resets the ramp capacitor. Next, the REFRESH LATCH signal is set to *high* so that the data in one set of latches is transferred to the

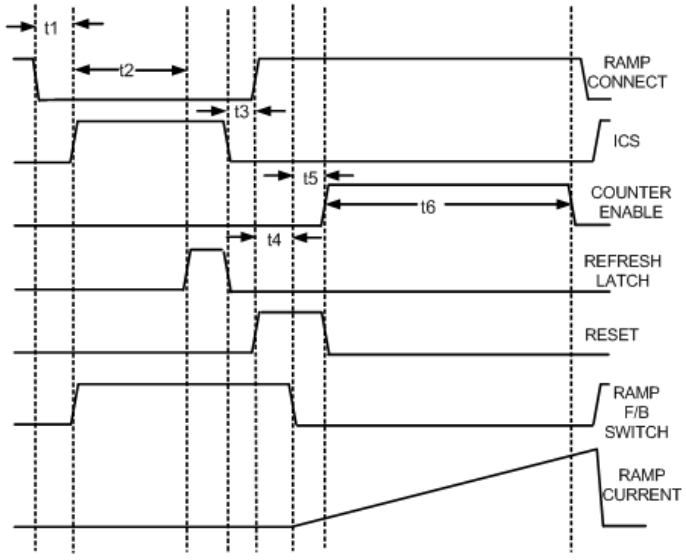

Figure 3.21 ADC Timing Diagram

second set of latches. This pulse is short. After the REFRESH signal goes to *low*, the RESET signal is set to *high* in order to reset the first set of latches. The RAMP F/B SWITCH then goes to *low* which starts charging the capacitor. Following the RAMP, the COUNTER_ENABLE signal is set to *high* so that the counter may start counting. Flexibility is achieved for the timing of this signaling using a FPGA (Chapter 4). The last waveform shows a linearly increasing ramp current which starts when the RAMP F/B SWITCH is set to *low* and goes to *zero* when this switch is set to *high*.

3.4 AMI 0.5 Layout

A four-channel ADC is simulated, designed, and fabricated in the AMI 0.5-micron CMOS process available through MOSIS [51]. Figure 3.22 is an image of the final layout of the current-mode ADC with a 40-pin padframe. The top half of the layout shows the Gray code counter and the ramp generator. The lower left block is the set of four comparators. The block on the lower right is the digital section which includes the latches, the tristate buffers, and the Gray-to-binary decoder.

The available area on the chip was 1mm x 1mm. The integrating capacitor is implemented off-chip due to the limitations of the available area on the chip. For testing purposes, a 100pF off-chip capacitor is used. The chip microphotograph is shown in Figure 3.23.

3.5 Conclusion

The design of the current-mode integrating ADC is described in this chapter with an explanation of the design of the key blocks of this topology. The ramp generator circuit is explained in detail. This includes a derivation of the temperature dependence of the ramp current. The current comparator circuit and the novel Gray code counter topology are described as well as the system level design with the digital section, the timing diagram, the final layout, and the chip microphotograph.

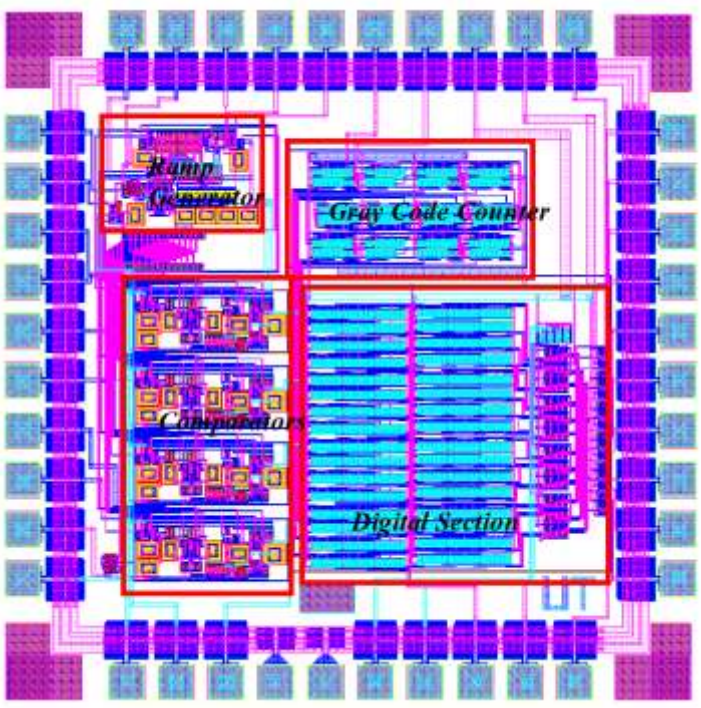

Figure 3.22 Current Mode ADC Layout (1.5 mm x1.5 mm)

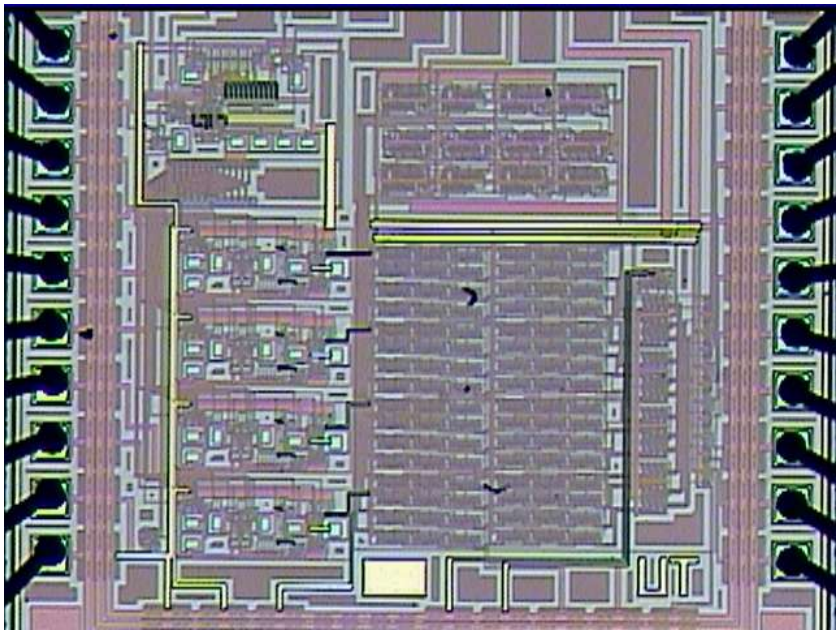

Figure 3.23 Die-photo of Current-Mode Multi-channel ADC

Chapter 4

Measurement Setup and ADC Testing

Data converters are described using different specifications. Several of these specifications are critical to define the resolution of the ADC and its performance. Testing data converters for these parameters is essential to verify that the converter functions well for its necessary requirements. In the life cycle of a data converter, 20% of the time is needed to design the converter, and 80% of the time is occupied with testing the data converter to obtain the required specifications. In this chapter, the first section describes the different specifications of an ADC followed by the design of the test board and finally, the test setup and measurement results are provided followed by improvements which are implemented on the test system to obtain even better results.

4.1 Specifications of Analog-to-Digital Converters

ADCs have different applications, and their specifications are defined based on the type of application. ADCs are tested for these key specifications. Following are the definitions of the terms used to specify this ADC.

4.1.1 Differential Nonlinearity (DNL)

Differential nonlinearity is defined as the difference between two adjacent analog signal values compared to the step size (LSB weight) of a converter generated by transitions between adjacent pairs of digital code numbers over the full range of the converter. The DNL for an analog-to-digital converter is written as Equation 4.27

$$DNL = A_{input}(Q_{m+1}) - A_{input}(Q_m) - 1LSB \tag{4.27}$$

where Q_{m+1} and Q_m are two adjacent quantization levels. $A_{input}(Q_n)$ is the analog input voltage corresponding to the quantization level Q_n [52]. Figure 4.1 shows the transfer curve of an 8-bit converter. A comparison is given between the ideal transfer function and the actual transfer function of an 8-bit ADC. The figure depicts an example of where the DNL = −1 is a result of a missing code.

4.1.2 Integral Nonlinearity (INL)

Integral nonlinearity is defined as the maximum deviation of the transfer function from the ideal line drawn between 0 and the full scale value [53]. The integral nonlinearity results from the effect of the curvature of the transfer function from the ideal straight line. This definition is, however, a conservative one and defined as an end-point INL. The best fit line of the integral nonlinearity is used for the purpose of this work. A converter is always monotonic when the INL specification is less than or equal to $\pm 1/2$ LSB. Figure 4.1 illustrates an example of the INL when a wider code width leads to a larger value of integral nonlinearity.

4.1.3 Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio (SNR) is the most important dynamic specification of a converter. SNR is defined as the root mean square (RMS) power of the signal to the RMS power of the noise expressed in decibels (dB) [53]. This excludes noise caused by distortion, but includes quantization noise, thermal noise, 1/f noise, and other types of noise. The maximum source of noise on data converters is due to the quantization noise. The theoretical noise is calculated, shown in Equation 4.28, where N is the number of bits of the ADC.

$$SNR = 6.02 \times N + 1.76 \tag{4.28}$$

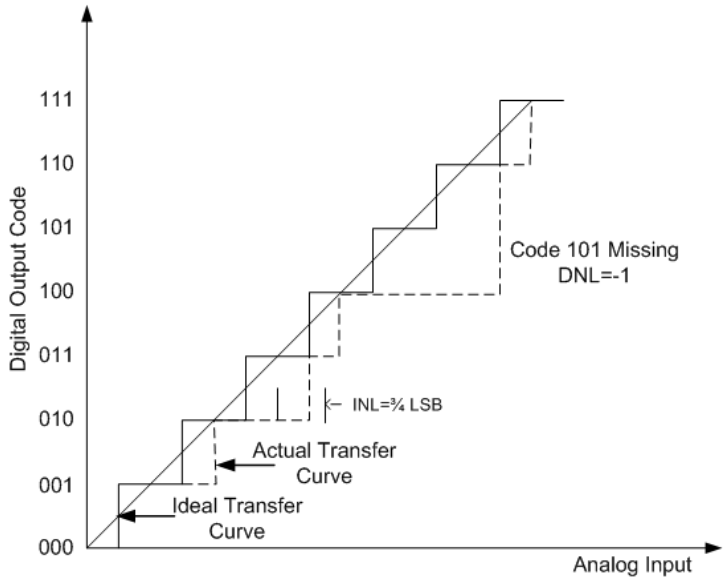

Figure 4.1 Transfer Curve of an 8-bit ADC with DNL and INL

4.1.4 Total Harmonic Distortion (THD)

When a single test tone is passed through a circuit under test, the harmonic distortion components appear at integer multiples of the test tone's frequency (f_t) which is the fundamental tone. Distortion that is symmetrical about the x-axis gives rise to only the odd harmonics. Asymmetrical distortion, such as clipping on only the lower or upper portion of the waveform, gives rise to both odd and even harmonics [53]. The total harmonic distortion refers to the addition of RMS power within all these harmonics.

4.1.5 Signal-to-Noise and Distortion Ratio (SNDR)

The specification of SNDR includes the noise and distortion in one parameter. This is given by the ratio of the RMS of the signal power to the sum of the RMS power of the noise and distortion. Signal-to-noise and distortion is given by the formula in Equation 4.29

$$SNDR = \frac{S}{THD + N} \tag{4.29}$$

where, *S* is the signal power, *THD* is the total harmonic distortion, and *N* is the noise. Nonlinearity in the transfer function of a converter causes distortion. A larger value of INL implies a larger SNDR, since the nonlinearity results in harmonics in the Fourier transform.

4.2 Test Setup Components

A general purpose test board was designed to provide all of the required digital signals from an FPGA. This motherboard has 50-pin headers to facilitate the interface to the daughter cards. A daughter card was designed to supply and provide analog signals to test the functionality of the current-mode ADC. The following sections provide a detailed description of the two test boards, the FPGA components, and the data acquisition system.

4.2.1 Board Design

Figure 4.2 illustrates the test setup block diagram including the mother board, the daughter card, and the signaling between the two boards. It also depicts the regulators required for the mother board and the daughter card, and the clock generator. Both voltage and current bias are required for the current-mode ADC. The four analog input channels are shown. There are also additional signals which are provided by the DIP switches to the FPGA.

Figure 4.3 shows the top level block diagram of the test setup. It includes the ADC test board which consists of the motherboard with the FPGA and the daughter card. It also incorporates the data acquisition card which receives data from the test board. The general purpose interface bus (GPIB) is used to interface with the instruments. LabView is used to program the Audio Precision, which is the low distortion waveform generator utilized to output a sine wave of the required frequency and amplitude. It is also used to program the Keithley current source to output the required amount of current.

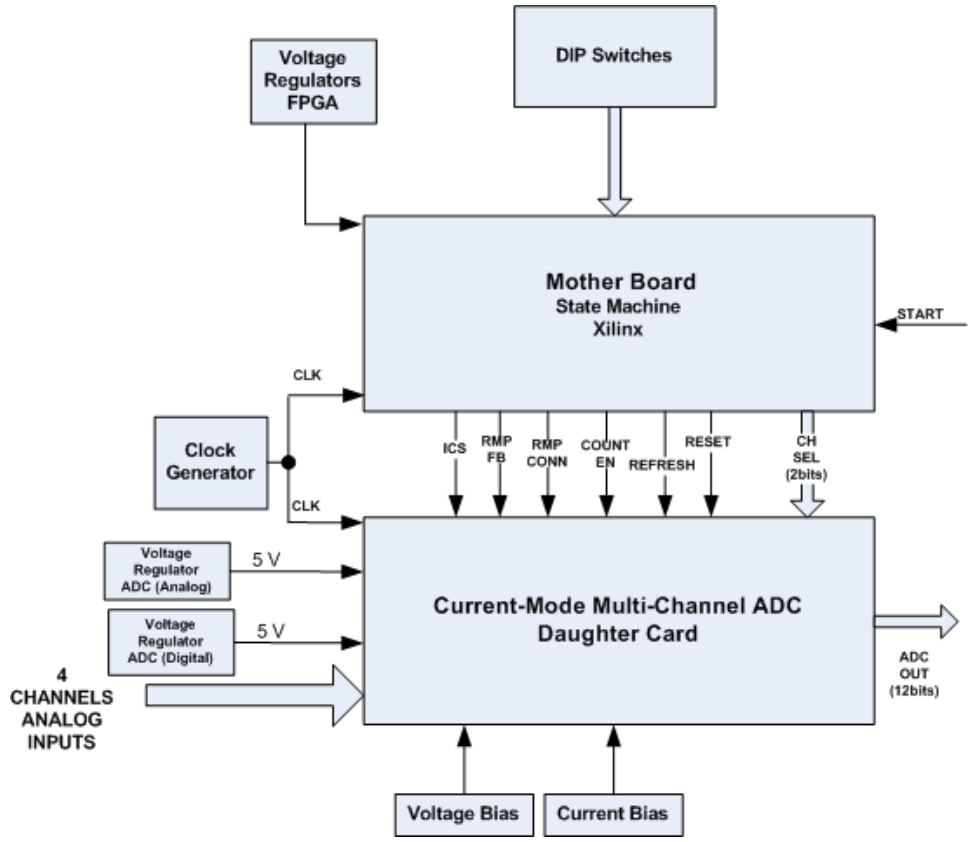

Figure 4.2 Block Diagram of the Test Board Setup

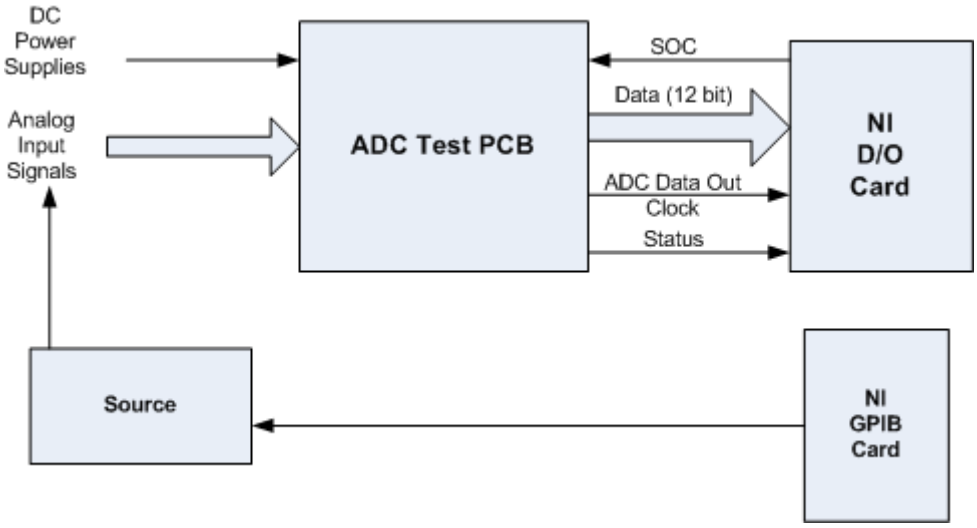

Figure 4.3 Top Level Block Diagram of Test Setup

Both of these functions are achieved using the GPIB port. The ADC output data and the clock signal to the DAQ card allow the card to obtain data and to sense when to retrieve the data.

4.2.2 Ground Plane Partitioning

Mixed signal testing involves handling a quiet analog section coupled with a noisy digital section. Thus, it is important to isolate the noisy digital section from the quiet analog section in order to produce better results. This is achieved if the supplies to the analog and the digital sections are separated, and if the grounds to the two sections are shorted at a single point. Figure 4.4 depicts an example of ground plane partitioning. The two grounds are shorted on the left side where the two circles are marked.

Multilayer boards are used to obtain isolation between the digital and analog circuits. Four-layer boards are used for both the mother and the daughter board. Two of the four layers are used solely for power and ground. One layer is used for analog signal routing, and one for digital signal routing. Power is routed as a plane to the integrated circuits since it assists in reducing the inductance of the trace going from the regulator output to the chip, and reduces the resistance of the path.

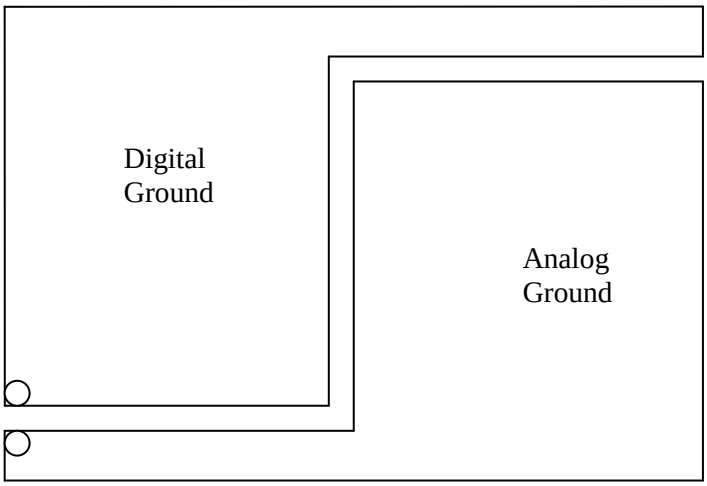

Figure 4.4 Ground Plane Partitioning

The loop area is minimized by utilizing planes. The loop area is defined as the area traced by the signal and the return path of that same signal. If the reference plane of a signal is directly below the signal trace, the loop area is the smallest. Crosstalk between signal traces is reduced by having the reference plane as close to the signal as possible. The capacitance between the appropriate planes also helps in adding to the decoupling capacitance. Figure 4.5 illustrates the cross-section of the 4-layer PCB.

Supplies to the analog and digital sections are kept isolated using separate regulators whose inputs are from the same power supply source. The digital switching signals produce a large amount of ground currents which contaminate the ground owing to their return path. If the analog circuits in the ADC are connected to the same ground, the noise caused by the switching digital signals causes inaccuracies and hence, reduces the resolution and the signal-to-noise ratio of the ADC. Separate analog and digital ground planes are hence maintained. They are single-point-grounded at the daughter board. A tight ground strap is included in the daughter board to eliminate the inductive effect which arises from using a banana plug. The next few sections provide a more detailed description of the test boards and the components used therein.

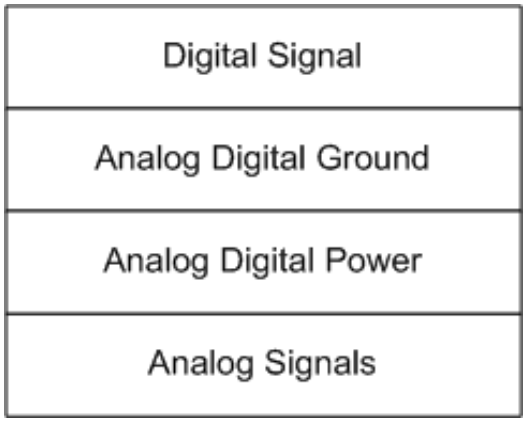

Figure 4.5 Cross Section of 4-Layer PCB

4.2.3 Motherboard

The motherboard was designed to support switched capacitor analog circuits which require additional digital signals from an external FPGA. The two 50-pin headers on the board also facilitate temperature testing of the circuits. This allows the FPGA to operate external to the temperature chamber. The primary components on the motherboard include the FPGA, the multiple regulators to support the FPGA, and the daughter card. In addition, support for programming the FPGA is provided through a PROM and JTAG.

Figure 4.6 is a photograph of the mother board. The regulators powering the FPGA are to the left. The FPGA is the block labeled in the center. DIP switches on the right of the FPGA provide certain signals to start or stop the state machine. The SMA connectors below the FPGA provide the clock to the FPGA.

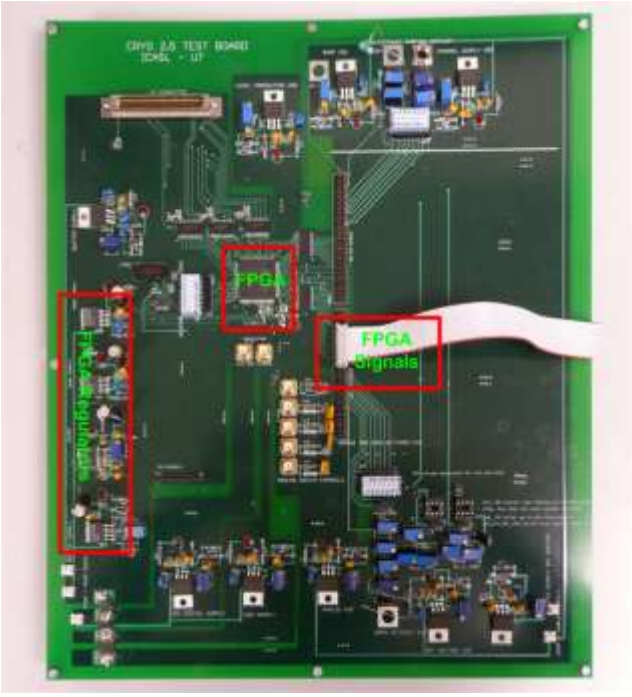

Figure 4.6 Photograph of Mother Board

The ribbon cable on the right carries the FPGA signals from the mother board to the daughter card. A tight ground strap is provided at the lower left corner of the board to avoid banana plugs and long inductive loops. Multiple voltage and current biases are provided to interface any daughter card with the help of this board. The plane splits are also depicted in the photograph.

4.2.3.1 FPGA and PROM

Multiple phase and non-overlapping clocks are required by the ADC in order for it to function. The FPGA is used to generate these clocks using Verilog code that is programmed into the FPGA. Different factors are considered prior to selecting the FPGA. First, the ADC sampling rate is dependant on the counter running at high speeds of 40 MHz to approximately 100 MHz. The maximum frequency of operation of the FPGA needs to be taken into account to support these frequencies.

The Xilinx Spartan 3E family was chosen because it is a relatively low-cost family. This family has a larger number of logic cells per I/O as compared to the Spartan 3 family, and it supports a wide frequency range (5 MHz to 300 MHz). Among the different types available in the Spartan 3E family, the selected XC3S250E provides an adequate number of logic cells, I/O, and block RAM for testing the ADC. This FPGA has 250K gates, 5,508 logic cells, 172 I/O, and 216K block RAM bits [54]. A TQ144 (thin quad flat package with 144 pins) was chosen since it has an adequate user I/O as well as easily accessible pins on the surface of the test board for probing. Additionally, the software Xilinx ISE Webpack is available on the web to support programming the FPGA.

The FPGA is required to provide digital signals to support the switched capacitor circuits, as well as digital circuits on the ADC. Spartan 3E FPGAs are programmed by loading configuration bits into static, reprogrammable CMOS latches that collectively control all functional and routing resources [54]. A PROM based programming implemented on the board simplifies the programming of the FPGA and allows retention of the configuration bits even if the power to the board is switched *off*. The PROM is a

nonvolatile storage medium. For the chosen FPGA, the recommended PROM is XCF02S. The Master Serial mode is used to program the FPGA. Figure 4.7 shows the FPGA configuration using the master serial mode with the platform flash PROM.

This particular class of Xilinx SPARTAN 3E FPGAs has six dedicated configuration pins. Included are the DONE and the PROG_B pins, and the four JTAG boundary scan pins which are TDI, TDO, TMS, and TCK. The FPGA supplies the CCLK from its internal oscillator to the attached platform flash PROM. The PROM then provides the bit serial data to the FPGA DIN data input, and the FPGA accepts this data on each rising CCLK edge. The DONE pin is an indicator pin used to tell the user that the configuration is completed. This pin is *low* during configuration and goes to *high* when the FPGA has successfully finished.

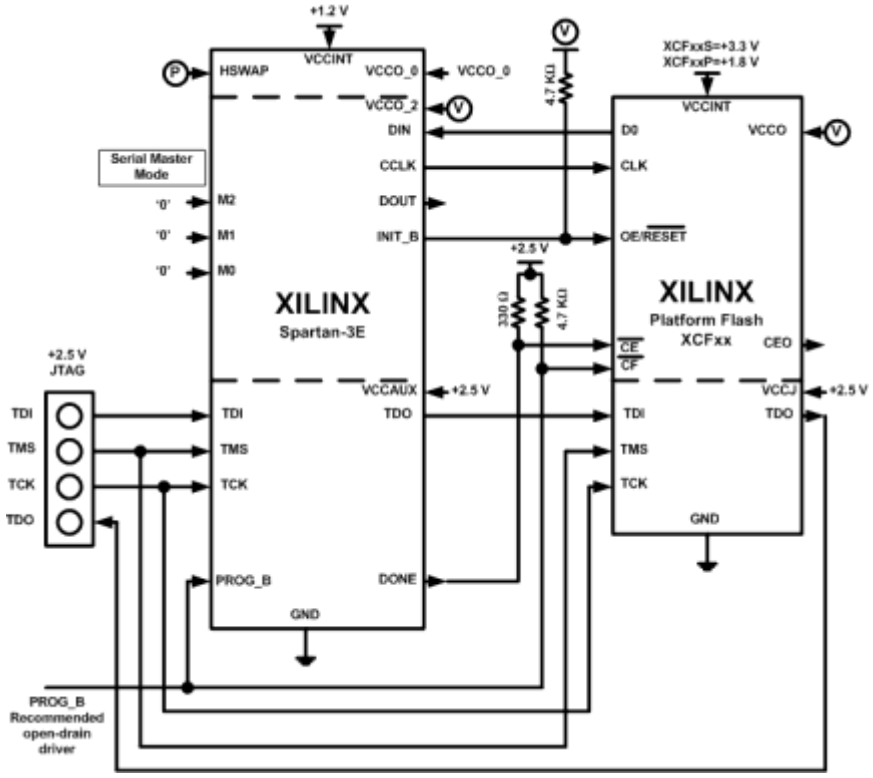

Figure 4.7 Master Serial Mode Using Platform Flash PROM [54]

The DONE pin requires an external pull-up resistor. It is connected to the Chip Enable ($\overline{CE}$) pin of the PROM. This signal enables the PROM during configuration and disables the PROM after configuration. This pin is asserted *low* to force the FPGA to restart the configuration process and reset both the DONE and the INIT_B pins. During configuration, this pin is pulled to *high* to enable configuration. It is connected to the PROM's Configuration Pulse ($\overline{CF}$) pin allowing the JTAG PROM programming algorithm to reprogram the FPGA. [54]

Signals are available on the FPGA that decide which mode the configuration is performed. These are the M2, M1, and M0 pins. Pulling these three pins *low* enables the FPGA to program in Master Serial mode. This configuration mode also implies the usage of the internal CCLK for programming the FPGA. The status of these pins is sampled when the INIT_B pin of the FPGA goes to *high*. The INIT_B pin is an initialization indicator. At the start of configuration, the INIT_B goes to *low*. Memory is cleared during this process and the pin is released at the end of the memory clearing process. This pin requires an external pull-up resistor to V_{CCO_2} which is a supply to the FPGA. The supplies required by the FPGA and the PROM are explained in Section 4.2.3.2. The INIT_B pin is connected to the PROM's OE/ $\overline{RESET}$ pin during configuration.

The HSWAP pin is an additional pin that is required to be at a well-defined potential during initialization and configuration. The HSWAP pin defines whether the FPGA I/O pins have an external pull-up resistor connected to their associated V_{CCO} supply. For the purpose of this test-board, the I/O pins do not have external pull-up resistors and therefore, the HSWAP pin is defined as *high* during configuration so that that all I/O pins are in a high-impedance state during configuration.

4.2.3.2 FPGA Supplies

The FPGA requires three different supply voltages. They are V_{CCINT} and V_{CCAUX} for internal logic functions, and a separate V_{CCO} for each of the four bank supplies. The FPGA provides the capability to interface with different I/O voltages and standards so that the bank supply is varied depending on the requirements. For the purpose of this testing, the internal and the auxiliary supplies are maintained at 1.2 V and 2.5 V respectively. The bank supplies for the four different banks are supplied at 3.3 V. Table 4-1 provides descriptions for the different supply voltages.

Table 4-1 FPGA Supply Voltages

Supply	**Description**	**Supply Voltage**
V_{CCINT}	The internal core supply voltage which supplies all the internal logic functions including the CLBs, the block RAM, and the multipliers.	1.2 V
V_{CCAUX}	The auxiliary supply voltage which supplies the clock manager, the differential drivers, the dedicated configuration pins, and the JTAG interface.	2.5 V
V_{CCO_1}, V_{CCO_2}, V_{CCO_3}, V_{CCO_4}	The I/O supply voltage which supplies the different I/O banks of the FPGA. They supply the top, right, bottom, and left of the FPGA, respectively.	3.3 V

4.2.3.3 Regulators and Supply Requirements

The output of a linear power supply varies with the input. Noise or spurs injected into the input of the power supply also appear at the output. The output also varies as the load current varies. It is important that any circuit connected to the power supplies is isolated from random noise, variations which are caused by load current changes and different frequencies picked up by the power supply.

Linear regulators are used on test boards to provide increased noise filtering and a stable supply voltage to the powered chip. In addition, the chip is protected in the event that the connected supply is in the reverse polarity. From the available regulators, linear regulators are preferred over switching regulators since the linear regulator has lower noise characteristics. In addition, fewer components are required for linear regulators and no inductor is necessary.

The regulators used on the board are selected using the National Instruments guide to power management of the Xilinx FPGA. LP3964 is used for the bank supply V_{CCO} and the PROM supply. This regulator is an ultra low dropout (LDO) regulator which functions over an input voltage range of 2.5 V to 5 V. It can source a maximum output current of 0.8 A, which is sufficient for the FPGA I/O banks. Like any LDO regulator, the LP3964 requires external capacitors to provide stability. Input and output capacitors are connected externally. The latter is required primarily to maintain the loop stability of the LDO. The equivalent series resistance (ESR) of the output capacitor is important since it provides the required phase lead to stabilize the loop. Both the SHUTDOWN ($\overline{SD}$) and the Error pin are actively terminated using a 10 KΩ resistor to supply for proper functionality. [55]

The LP3875 is selected to supply the 2.5 V to V_{CCAUX}. The output voltage is set by the two resistors which are at the output of the regulator circuit. The output is determined by Equation 4.30.

$$V_{out} = 1.216 \times \left(1 + \frac{R_1}{R_2}\right) \tag{4.30}$$

As for the LP3964 regulator, input and output capacitors are required to maintain the stability of the LDO regulator. A feedforward capacitor is also added to improve loop compensation. [56]

LP38853 supplies the V_{CCINT}. This regulator provides an output voltage range of 0.8 V to 1.8 V, and is a good candidate to supply V_{CCINT}. In addition, since all internal logic is powered by this regulator, it requires the ability to supply an increased amount of current. The LP38853 has the capacity to supply up to 3 A of current which is suitable for this purpose. Again, input and output capacitors are required in addition to the feedforward capacitor. This maintains stability and loop compensation. [57]

The rest of the supplies on the mother board and the daughter card are supplied using an LM317 regulator. This regulator can supply 1.5 A of current. These regulators supply the buffers on the mother board, the ESD supply of the chip, and the digital and analog supplies on the chip. The output voltage on this three-terminal regulator is determined by the two resistors at the output of the regulator and the equation to calculate the output voltage (Equation 4.30).

4.2.3.4 Buffers

The mother board is interfaced with a daughter card using the two 50-pin headers. A ribbon cable is required for this interface. Ribbon cables introduce capacitance. The capacitance introduced by the ribbon cable increases per unit length of the cable. The FPGA may not have the ability to drive the amount of capacitance at higher frequencies. For this reason, buffer/driver chips are added at the output of the FPGA which drive one set of signals from the FPGA to the daughter card, and another set of signals from the FPGA to the data acquisition card located in the computer.

The SN74AVC16244 chips are used to drive signals from the FPGA to the daughter card. This chip provides a minimum rise time and propagation delay to suit the requirements for this design. The AVC logic family achieves the minimum propagation delay of 2 ns. The 74LVC244 octal buffers drive

the FPGA signals to the 5 V data acquisition card. Additionally, the propagation delay and rise and fall time are taken into account to suit the requirements of this design.

4.2.3.5 Terminations and Bypassing

Power supply bypassing is important in test board design. The output impedance of the regulators increases with frequency, which is modeled as an inductor at the output of the regulator. Additionally, there may be a long trace running from the output of the regulator to the chip it is supplying. This adds to the inductance. As the load changes, current requirements (di/dt) change in the trace. This results in a noise voltage across the trace. This effect is reduced by decreasing the rate of change of current through the trace. Therefore, bypassing the power supplies at the pin of the chip is important. It reduces the spurious noise introduced and provides a cleaner power supply. Capacitors in at least two different ranges are maintained at the chip pins to remove noise in all the frequency ranges. Multiple parallel capacitors at each pin assist in reducing the equivalent series inductance of the capacitors. [58]

Clocks are also important for the operation of the FPGA and the ADC chip. Both the FPGA and the ADC require a high frequency 40 MHz clock for 10 KSps operation. An RG-52 cable is used to drive the clock from the pulse generator to the test board. The RG-52 cable has a characteristic impedance of 50 Ω and is a capacitive load. The output impedance of the pulse generator is 50 Ω. In order for the signal to be transmitted cleanly without reflections, terminate the clock on the board with a 50 Ω resistor. Matched impedances are important for transmission lines. These termination resistances improve the signal quality of the clock with a small time period.

4.2.4 Daughter Board

The daughter board includes the same components as the motherboard, LM317 supply regulators, the bypassing capacitors, and termination resistors. The 40-pin current-mode ADC chip is located on the

daughter card. In addition, it includes the connector for the data acquisition system card. The details of this system are described in Section 4.2.5. This board also includes the connectors for the input currents to the 4 channels of the ADC and the biasing resistors for the bias voltages and currents required for the ADC. A male header is provided to receive signals from the mother board. The ability to add termination resistors to these digital signals is also provided on the board.

Figure 4.8 is a photograph of the daughter card. The left side shows the regulators for the digital section of the ADC and the supply for the buffers. On the upper side is the NI connector. The ADC chip is located in the middle of the board. On the left of the chip is the SMA connector which receives the high frequency clock to drive the counter. To the far right are the regulators which supply the analog and the ESD pads on the chip.

Some dc voltages and currents are required to bias the different circuits of the ADC. V_{bias} biases

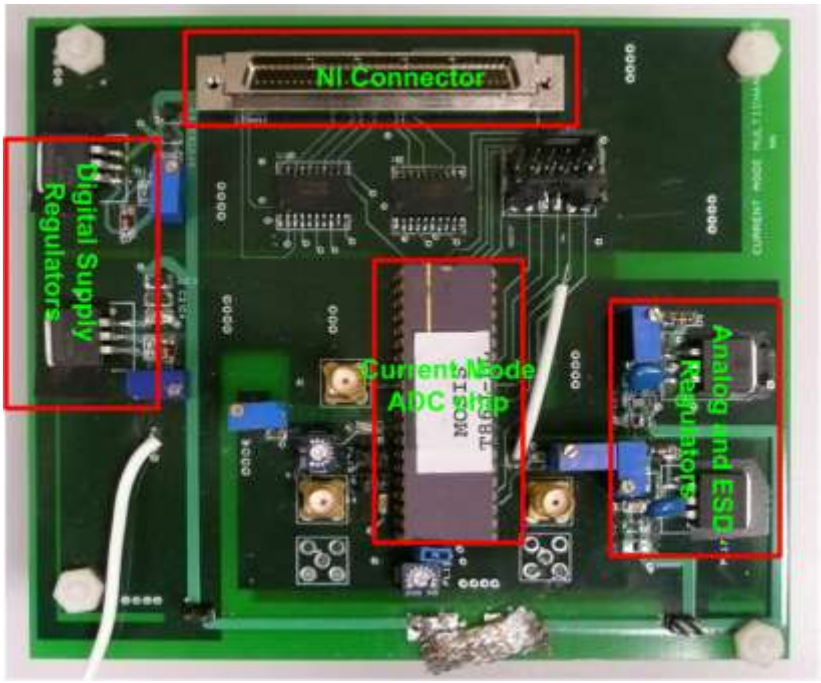

Figure 4.8 Photograph of Daughter Card

the input of the comparator. I_{dc} biases the input branch of the comparator so that the input transistors are maintained in saturation. The V_{tune} bias voltage is required to bias the input of the ramp generator. It is a constant voltage required to charge the charging capacitor in order to maintain the correct sampling rate and input range. These three biases are provided on the daughter card to avoid external sources. All the biases are generated with the help of resistors to avoid the noise produced by the Keithley current source since the Keithley current source is based on a switched mode power supply. Jumpers are provided at these nodes to enable alternatively the usage of a power supply or a current source instead of the resistor biases.

Additional buffers are included on the board to enable the chip to drive the data acquisition card. Sets of vias are provided on the board and are connected to ground. These vias allow the user to probe the ground at different sections. Additionally, the plane splits are clearly visible in the photograph.

4.2.5 Data Acquisition System

The analog-to-digital converter outputs data for every sample. It is important to capture the output data of the ADC and process it in order to calculate the various parameters of the ADC and evaluate the performance of the ADC. This data is obtained and stored with the help of a National Instruments Data Acquisition (DAQ) card. A 68-pin connector on the daughter card is used to connect the DAQ card to the ADC. The data collected by the card is then stored and processed using either LabView or Matlab data processing software.

A PCI 6534 card is used as the DAQ card to interface the ADC data to the computer. The PCI 6534 has 32 individually configurable input/output ports. It also has a maximum data transfer rate of 20 MHz, which is adequate for this application. The ports are divided into four 8-bit ports. This card has a number of different methods of data transfer. The methods include receiving data at regular externally clocked signals, transferring data using handshaking or burst mode, and the change-detection method

where the digital data is acquired every time the state of a line changes. For the purpose of this work, the latter method is used when one dedicated line is used to inform the NI card that data is available at the output of the ADC, and it is ready to be retrieved and processed. The card has an onboard memory of 32 MB. For computing the DNL, a large amount of data is required (approximately four million samples). The buffer memory on the card is not sufficient for this amount of data. Thus, a finite transfer method is not suitable. A continuous sampled method is used where blocks of data are taken in and transferred to the computer memory.

The finite transfer method implies that the card will transfer a finite amount of memory to or from the computer and then stop the operation. The continuous sampled method implies that the data is transferred from the onboard buffer to the computer memory continuously in a loop [59]. In order to save CPU time and produce accurate measurements, it is adequate for the DAQ card to acquire data from the input lines only when data is ready at the input. For this purpose, a change-detect signaling method for data acquisition is used and supported by a PCI 6534 card. The card obtains data from the input only when a certain line, or a set of lines, changes state. In order for this to occur, the FPGA drives another signal to inform the DAQ card that it is time to take the next set of data from the input.

To get the 12-bit data for the ADC, two ports (port 0 and 1), are configured as input ports to the PCI card and together they define 16 lines from the daughter card to the DAQ card. One line (line 0 on port 0) is configured as a change-detect line. Labview is programmed to help the interface. When the signal on the change-detect line changes state, data is collected from the ADC. This 16-bit data is then reduced to 12 bits for further processing.

The operations of data acquisition and processing are possible only with the state machine in the FPGA and the Labview program working simultaneously. Descriptions and flow-charts for both software implementations are described in Section 4.2.6.

4.2.6 Software: Verilog and Labview

4.2.6.1 Verilog State Machine

The timing of the signals driving the switches and the digital circuits on the ADC is defined by the state machine on the FPGA. Figure 4.9 is a flowchart depicting an overview of the state machine. The state machine is coded in Verilog, which is a hardware description language (HDL). The code is written in a synthesizable format so that it is realized physically, then mapped and placed on to the Xilinx FPGA on the mother board.

The following bullets provide a more detailed description of each state. Before the state machine is entered, a Chip Enable switch is checked for *high* so that the state machine is disabled when required. The FPGA cycles through the state machine using an inbuilt counter which sets the timing. The code is given in 0.

- The DONE_WAIT state is entered when all switching for one sample cycle is completed and the state machine is waiting for the next sample cycle to begin. This is determined by the ramp time.
- The RMP_INP_OPEN state disconnects the ramp generator from the comparator and resets the charging capacitor.
- The SAMPLE_VGOFF_OPEN state defines the state of two different switches. The sampling switch is closed so that the input current is sampled. The VGOFF switch is also closed so that the offset voltage on the OTA used in the ramp generator is stored on a capacitor. The REFRESH switch is closed, during this cycle so that the data on the latches is moved to the adjacent set of registers. Then the next conversion cycle can start.
- The RESET_VGOFF_OPEN state defines two different switches. This state resets the latches and opens the VGOFF switch.

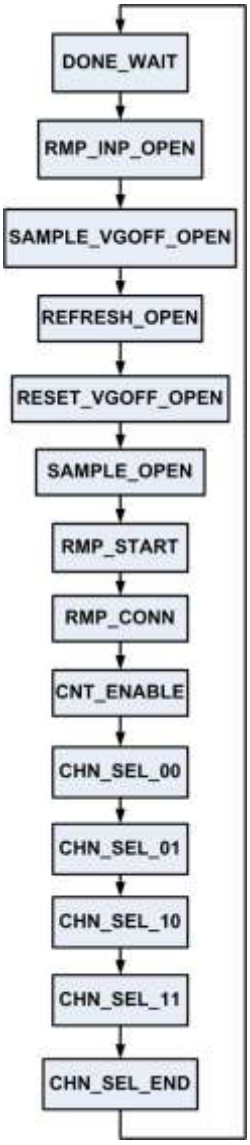

Figure 4.9 Flow Chart of State Machine

- The SAMPLE_OPEN state switches off the gate sampling the current.
- The RMP_START opens the switch shorting the charging capacitor, thus starting the ramp current.
- The CNT_ENABLE state enables the counter. This state is maintained separate from the RMP_START to provide more flexibility to the system and to remove any glitches appearing when the ramp current starts up.
- The CHN_SEL_00 selects the first channel so that the data from the previous cycle is read via the second set of latches.
- The CHN_SEL_01 selects the second channel.
- The CHN_SEL_10 selects the third channel.
- The CHN_SEL_11 selects the fourth channel.

4.2.6.2 LabView Program

Labview is a graphical user interface tool that assists the computer interface with the hardware and instruments. In this test system, Labview is used primarily to accomplish the following three tasks:

- An instrument is programmed to give an input signal to the data converter. This is implemented using a General Purpose Interface Bus (GPIB) card.
- The data from the ADC is retrieved from the test board and transferred to the computer. This is achieved using the DAQ card.
- The data collected from the ADC is processed further.

Figure 4.10 is an illustration of the flow of the program in LabView. At first, the sine wave generator, or the Keithley current source, is initialized. In the case of the sine wave generator, the amplitude and frequency of the sine wave are set. When the Keithley current source is used as an input to the ADC, the step size and the range of the current are adjusted. Depending on the user input value of the number of

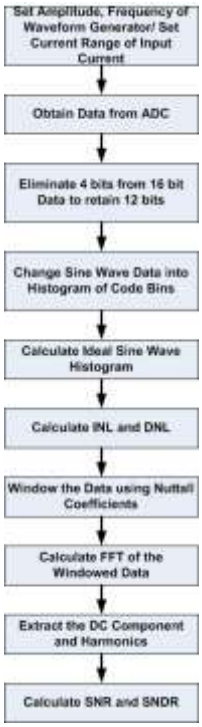

Figure 4.10 Flow Chart of Labview Program

samples collected, the data is obtained and stored using the continuous transfer method. The data is obtained from 2 ports, each of size 8 bits. The 12-bit data is then extracted from 16 bits for further processing.

For the calculations of the DNL and INL, the data obtained from the ADC is processed. Initially, the histogram of the acquired data is computed. From the peak values of this histogram, the ideal sine wave histogram is determined. The details of this calculation method are given in Section 4.3. From these two sets of data, the DNL and INL of the ADC are calculated. For SNR and SNDR calculations, the data obtained is windowed using Nuttall coefficients. A fast Fourier transform (FFT) of the data is then computed. The DC component and the harmonics of the signal are extracted from the FFT data and then the SNR and SNDR are computed.

4.3 Parameter Measurement

The parameters described in Section 4.1 are measured using different methods. In the following subsections, details of each testing method are discussed.

4.3.1 Differential Nonlinearity Measurement

Numerous methods are used to characterize the DNL of an ADC. Two commonly used methods include the linear ramp histogram method and the sinusoidal histogram method. In the linear ramp histogram method, a slowly rising or falling ramp is applied to the input of the ADC. The output codes are recorded at the output of the ADC. The ramp is applied at a speed relatively slower than the sampling rate so that each code is hit a considerable number of times. The number of times each code is hit is called the code width. A histogram of the output is plotted. The DNL and INL are calculated from this histogram.

The sinusoidal histogram method is preferred over the linear histogram method because a ramp generator that has a higher linearity than the ADC under test is required to perform the measurement using the latter method. On the other hand, low distortion pure sine wave generators are easily available. In addition, a different linearity is possibly observed depending on whether the ramp is rising or falling. Also, the ramp method is a static characterization of the ADC. With a sine wave, a dynamic measurement is performed. For a linear ramp, there is even distribution of the input voltage or current. A sinusoidal waveform spends more time at the top and bottom of the wave. However, since the characteristics of the histogram of the sine wave are known, it is easy to compensate for this nonlinear distribution of codes [53].

For this test, a current sine wave is required instead of a conventional voltage sine wave. The current sine wave is generated by applying a sine wave in series with a resistance tied to the input to the

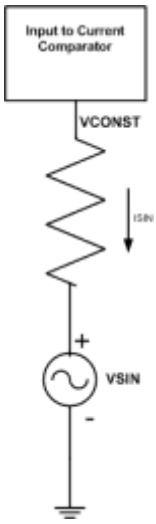

Figure 4.11 Generation of Current Sine Wave

ADC. One end of the resistor is held at a constant voltage since it is connected to the input of the comparator which is biased by an OTA. The other end is a continuously varying sine voltage. Hence, a continuously varying sine wave current is generated flowing through the input of the ADC. Figure 4.11 shows a schematic of the current sine wave generation that is implemented on the test board. The sine wave amplitude is adjusted to produce a full-scale range in order to ensure that all codes are covered. The lower end of the sine wave corresponds to a higher current, and the upper end of the sine wave corresponds to a low current.

The code density is defined as the number of times each code occurs. For an ideal ADC, an equal number of codes are expected in each bin. The number of codes in each bin, divided by the total number of samples, gives the fraction of the code width with respect to the full scale. Ideally, the ratio of the bin width to the ideal bin width is equal to one. Subtracting one from this ratio gives the differential nonlinearity. Equation 4.31 describes the calculation of DNL using the ideal histogram and the measured histogram as

$$DNL(i) = \frac{H(i)/N_t}{P(i)} - 1 \qquad (4.31)$$

where, *H(i)* is the number of codes in bin *i*, N_t is the total number of samples, *P(i)* is the ideal bin width, and *DNL(i)* is the differential nonlinearity of code *i*. [60]

For a sine wave test, it is important that the input is sampled randomly. To ensure this, it is important that the sampling frequency and the input sine are not harmonically related. That is, the input sine wave frequency should be prime relative to the sampling frequency. A sine wave frequency of 11.11 Hz is used for this requirement.

An equation is defined to calculate the minimum number of samples required for an accurate estimate of the DNL. A percentage confidence interval is first defined as $100(1-\alpha)$. The measured DNL is then defined to lie within the interval $\mu - Z_{\alpha/2}\sigma, \mu + Z_{\alpha/2}\sigma$ with $100(1-\alpha)$ probability. α is chosen for the desired confidence level. The minimum number of samples required is given by the Equation 4.32

$$N_t \geq \frac{{Z_{\alpha/2}}^2 \pi 2^{n-1}}{\beta^2} \tag{4.32}$$

where β is the number of bits of precision, and n is the number of bits which is 12 for this converter.

In order for this 12-bit converter to calculate the number of samples required to obtain an accurate estimate of the DNL, the confidence level is initially fixed as 98%. For this value of confidence level

$$\begin{aligned} \alpha &= 0.02 \\ \frac{\alpha}{2} &= 0.01 \end{aligned} \quad . \tag{4.33}$$

From the standard distribution table, the value of Z is obtained as in Equation 4.34.

$$\therefore Z_{\alpha/2} = 2.33 \tag{4.34}$$

For a 12-bit ADC *n*=12 and for a 0.1 bit precision $\beta = 0.1$. Substituting all the values into Equation 4.32, the number of samples is derived and shown in Equation 4.35.

$$N_t \geq \frac{2.33^{-2} \times \pi \times 2^{11}}{0.1^{-2}} \qquad (4.35)$$
$$\therefore N_t \geq 3.49 \times 10^6$$

To satisfy the above requirement, a total number of 4 million samples is taken in order to obtain an accurate estimate of the DNL.

Figure 4.12 shows the DNL measurement for four chip samples at room temperature. As seen from the figure for the entire range of the ADC from 0 to 4096, a DNL of less than 0.5 LSB is observed providing a differential nonlinearity of 12 bits. Additionally, there are no missing codes. However, there is a trend in the DNL which will be presented in more detail in the discussion in Section 4.1.2.

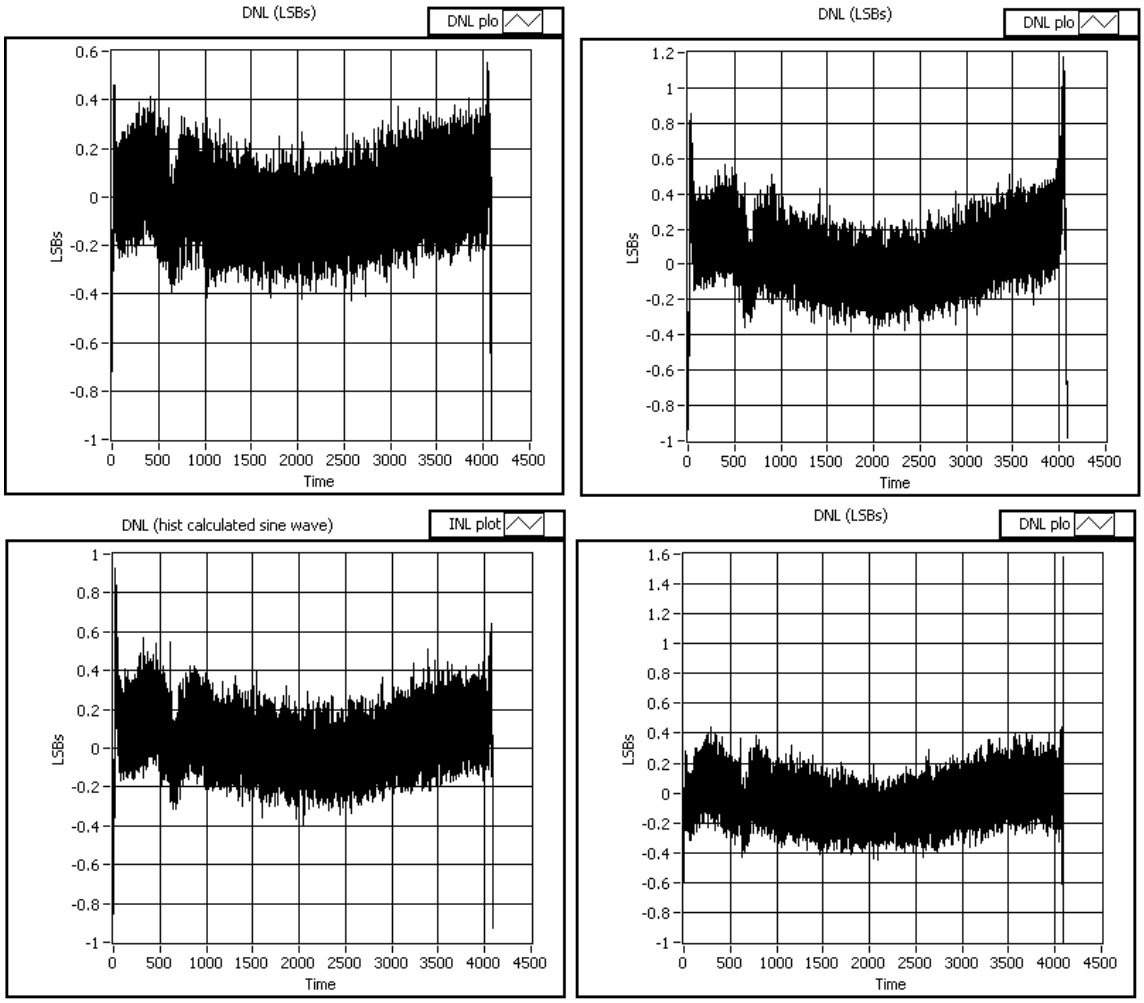

Figure 4.12 DNL Measurement for Chips 1-4

4.3.2 Integral Nonlinearity Measurement

INL is calculated by the running sum of the DNL. INL is calculated as shown in Equation 4.36.

$$INL(i) = \sum_{k=1}^{i-1} DNL(k), \quad i = 1,2,\ldots,2^N - 2 \tag{4.36}$$

As for the DNL, different methods are used to measure the INL. One frequently used method includes the ramp histogram method, but the ramp histogram method requires the source generator to be extremely linear. A current source is used to supply the current to measure the INL. However, a known issue with this form of measurement is that the source will go through multiple ranges to incorporate the entire current range of the ADC. When the range of the current source changes, the precision changes. As the range increases, the precision reduces. This change in precision is not desirable during linearity measurement since the linearity of the source itself is changing.

A sine histogram method is used to measure the INL. Unlike DNL, the INL values calculated using this method are sensitive to the amplitude and offset of the ideal sine wave used, as compared to the sine wave that is input to the ADC. The amplitude and offset of the ideal sine wave used for comparison is thus calculated from those of the digitized sine wave. These are calculated using the Equation 4.37

$$\begin{aligned} C_1 &= \cos\left(\pi \times \frac{H(2^N - 1)}{N_S}\right) \\ C_2 &= \cos\left(\pi \times \frac{H(0)}{N_S}\right) \\ offset &= \left(\frac{C_2 - C_1}{C_2 + C_1}\right)(2^{N-1} - 1) \\ peak &= \frac{2^{N-1} - 1 - offset}{C_1} \end{aligned} \tag{4.37}$$

where $H(0)$ and $H(2^N-1)$ are the number of times the lower code is hit and the number of times the upper code is hit, respectively. From these values, C_1 and C_2 are calculated. The offset and peak of the ideal sine wave are also calculated. From the values of the offset and peak, the ideal sine wave distribution of code hits is calculated, as in Equation 4.38.

$$H_{sinewave}(i) = \frac{N_s}{\pi}\left[\sin^{-1}\left(\frac{i+1-2^{N-1}-offset}{peak}\right)-\sin^{-1}\left(\frac{i-2^{N-1}-offset}{peak}\right)\right], \quad (4.38)$$

$$i = 1,2,\ldots,2^N-2$$

The DNL is calculated from the above equations, and the INL is calculated from the running sum of the DNL [53].

Figure 4.13 shows the INL measurement for four chips. A considerable amount of nonlinearity, on the order of 60 LSB, is observed on the INL. This is attributed to the ramp generator. Ramp linearity is improved as discussed further in Chapter 5.

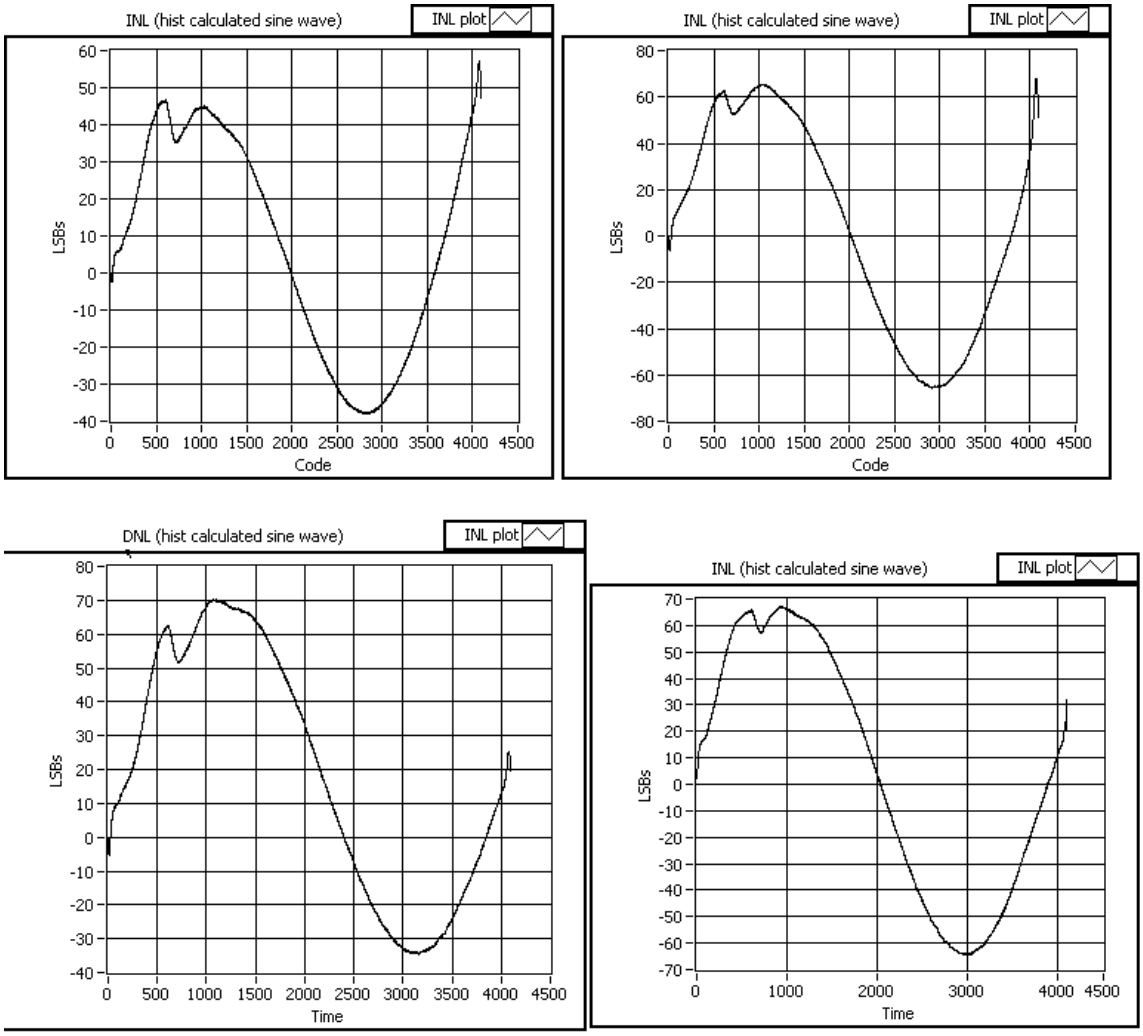

Figure 4.13 INL Measurement for Chips 1-4

4.3.3 Signal to Noise Ratio and THD Measurements

A sine wave with a frequency that is prime relative to the sampling rate, is required to measure the SNR. The frequency is chosen such that it is significantly greater than DC, and below the sampling rate of the ADC. A frequency of 71.11 Hz is chosen for the testing of the ADC. This signal is larger than DC, and well below the Nyquist rate of sampling. Also, the frequency of this signal is relatively prime and is not a factor of the sampling frequency. The data collected is windowed using a Nuttall window. This window has good side lobe characteristics. The windowed data has the power distributed over a narrow band of frequencies. A fast Fourier transform (FFT) is calculated on this windowed data in order to obtain the power spectral density (PSD) of the digitized signal. The different frequency components of this signal are thus isolated.

From the FFT output, the DC component is first removed, and the harmonics of the input signal are separated to calculate the signal-to-noise ratio (SNR) of the digitized signal. Figure 4.14 depicts the

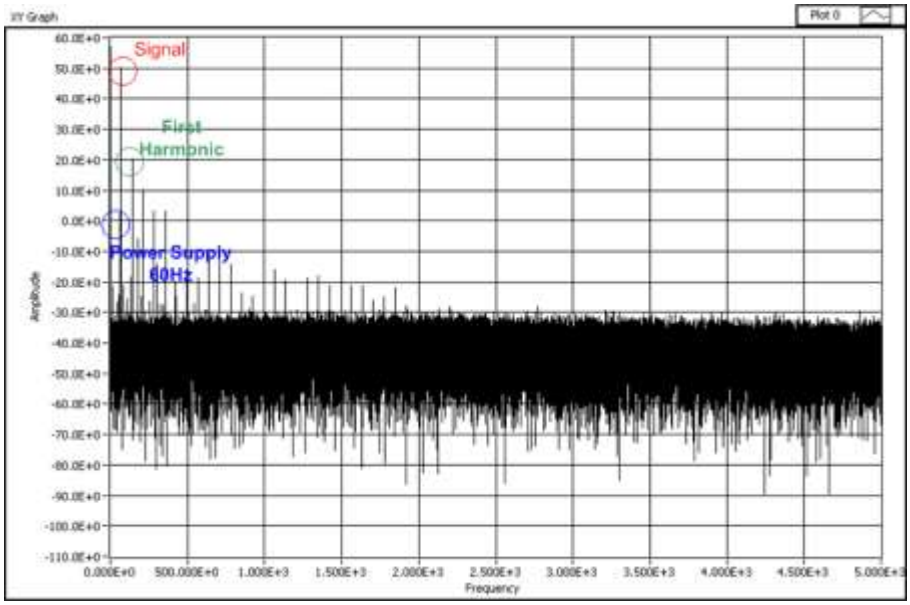

Figure 4.14 Fast FourierTransform(FFT) Chip 3

FFT of the digitized signal. The power supply noise is the blue encircled peak. The signal peak is encircled in red, and the first harmonic is encircled in green. Relative to the peak of the signal level a noise floor of approximately -30 dB is observed.

A large amount of noise is injected into the ground. This is caused by the high frequency clock which enables the operation of the counter. Further discussion on improvements of the test setup is discussed in Section 4.5. Table 4-2 provides the measured values of the SNR, SNDR, and THD for the five sample chips.

4.3.4 Input Referred Noise Measurement

Different types of noise in circuits have origins both inside and outside the circuit. White noise has a constant magnitude of power over frequency. Pink noise, or $1/f$ noise as the name suggests, has higher power at lower frequencies. Thermal noise, primarily generated by resistors, is temperature dependant noise. Other types of noise include shot noise and generation-recombination noise, both of which are caused by transistors. The three dominant ADC noise sources are quantization noise, ac noise and wideband noise. The input-referred noise is measured when the input is tied to a static signal.

Table 4-2 SNR, SNDR and THD Measurements on 5 Chips

Chip	SNR	SNDR	THD
1	39.54	33.0188	6.5212
2	39.7294	33.1174	6.6120
3	40.3776	36.2445	4.1331
4	39.9711	34.1626	5.8085
5	35.7752	30.7633	5.0119

Quantization noise appears primarily when the ADC is processing time-varying signals. This is modeled as a noise source connected in series with the input of a noise-free ADC [61].

To measure the input-referred noise of the ADC, the input channel is connected to ground, or to a constant voltage source which is heavily decoupled. For testing purposes, the input referred signal is measured by connecting the input to a constant voltage. The histogram of the output is then calculated. Figure 4.15 shows a histogram of the output of the ADC when tied to a constant input voltage. The Central Limit Theorem states that "the sum of a large number of *n* mutually random variables approaches a normal distribution". Based on the Central Limit Theorem, the distribution of the noise has a Gaussian shape. The Gaussian shape of the ADC output histogram, with a dc input, indicates that no significant problems exist in the ADC design, the layout, or the board layout. The RMS input-referred noise is computed with the help of this histogram.

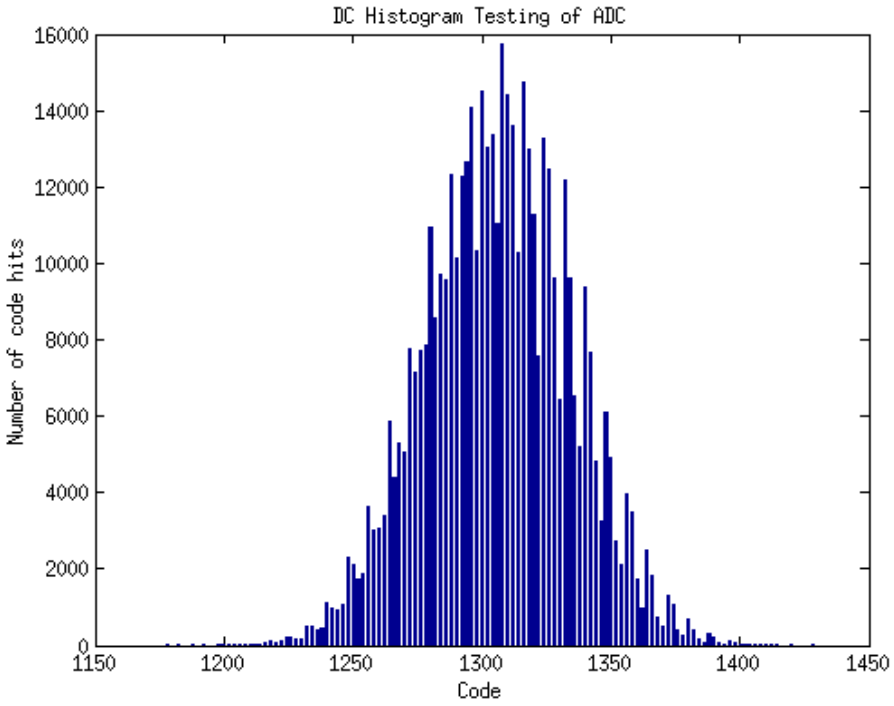

Figure 4.15 ADC Input Referred Noise Measurement

The code with the maximum number of hits is used as the central code. All the code hits around it are summed to calculate the total tail area of the Gaussian histogram. The RMS noise is calculated from this data set. The RMS noise is equivalent to the standard deviation of the data set. The standard deviation of the data set is computed and is shown in Equation 4.39

$$\sigma = \sqrt{\frac{\sum_{i=1}^{N} p_i (x_i - \bar{x})^2}{\sum_{i=1}^{n} p_i}} \quad . \qquad (4.39)$$

$$\bar{x} = \frac{\sum_{i=1}^{N} p_i x_i}{\sum_{i=1}^{N} p_i}$$

where p_i is the number of code hits of code x_i, and $\bar{x}$ is the mean of the values. Using this method the standard deviation is calculated as in Equation 4.40.

$$\sigma = 28.6LSB \qquad (4.40)$$

This value of σ is the input referred noise of the ADC and is a large value due to the noise on the chip, as well as to the noise on the board. Using this RMS input-referred noise, the effective resolution is computed in Equation 4.41 [61].

$$Effective\,\mathrm{Re}\,solution = \log_2\left(\frac{2^N}{rms\,input\,noise(LSBs)}\right)$$
$$Effective\,\mathrm{Re}\,solution = \log_2\left(\frac{4096}{28.6}\right) = 7.16LSB \qquad (4.41)$$

This further proves that the signal-to-noise ratio is augmented by improvements to the testing environment and changes on the chip. These improvements are described in Chapter 5.

4.4 Milestones in Testing

The ADC requires external support with the FPGA board at one end and the data collection hardware and software at the other end. To acquire ADC output data and process it, the FPGA, the ADC and DAQ must work together in unison. This requires each problem within the link to be located and debugged. This section covers several important milestones achieved in debugging the system.

The first run of the ADC with the sine wave input showed outputs with no particular pattern. The cause of this issue was found on the chip. Figure 4.16 illustrates the flow of data from the counter to the output. The Gray code counter data (12 bit) is fed into the latches. The latches then feed into the tristate buffers. The tristate buffers select which channel data to output, depending on the status of the CHANNEL SELECT signals. The tristate buffer outputs are then converted to binary code with the help of the Gray code-to-binary decoder (GCD). The output of the GCD drives the DAQ through buffers.

The tristate buffers integrated on the chip act as inverters instead of buffers. The Gray code is thus inverted and converted to binary. Consequently, this binary output does not show any pattern and appears garbled. Software was then written in LabView to change the data back to the inverted Gray code format. This data is then inverted yet again to revert to the original Gray code. It is then converted back to binary. Computation of the DNL and INL requires large amounts of data. This implies that large arrays of

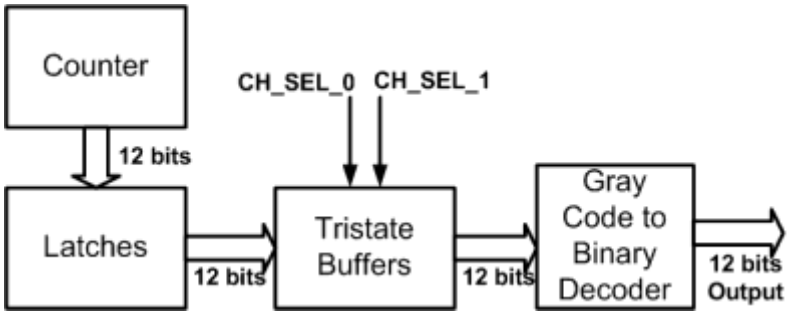

Figure 4.16 Flow of Data from the Counter to Output

data need to be processed. This is difficult to achieve without depleting the system memory. An alternative method is devised to avoid the conversion from binary to Gray and back to binary. This method proves to be faster and more efficient.

Figure 4.17 shows the upper four bits of the conversion from Gray code to binary. The inverters placed at the input of the XOR gates represent the tristate buffers that inverted the Gray code. For Gray code to binary conversion, the most significant bit (MSB), or bit 11 of the Gray code, is equal to the corresponding binary bit. Since this bit is inverted, inverting the MSB results in the correct binary bit. The property of XOR gates is such that if both bits are of the same value, the output is 0; whereas, if the two inputs are of different values, the output is 1. To compute bit 10, both inputs of the XOR gate are inverted. If both inputs of the XOR gate are inverted, the result is the same as if they were not inverted. As a result, bit 10 is valid.

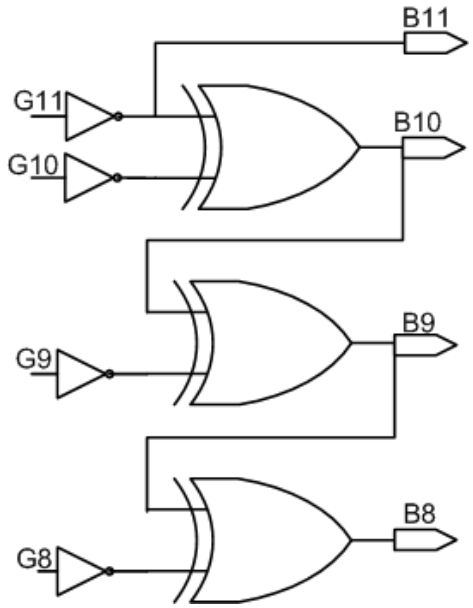

Figure 4.17 Gray Code Inverted to Binary Decoder

To produce bit 9, the two inputs to the XOR gate are binary bit 10, and the Gray code bit 9. Bit 10 is a valid bit and hence only one input bit is inverted. Subsequently, the output of the XOR gate that is bit 9 has to be inverted to obtain the correct binary value. Since both inputs to the XOR gate are inverted for bit 8 (similar to bit 10), the output is correct.

The same procedure is followed for the rest of the bits. The above analysis proves that if the inputs to a Gray-to-binary decoder are inverted Gray code, the accurate binary code is obtained by inverting alternate outputs of the GCD, starting at the inverted MSB. Figure 4.18 shows the method used to correct the binary output of the ADC.

Before the circuits were tested, all supply regulators are verified to ensure that they are working before the circuits are tested. In this case, all the regulators were verified with multi-meters. The respective potentiometers were adjusted to give a 5 V supply to the chip. However, after further complications, the regulators were checked with the oscilloscope. The regulator powering the ESD supply showed an RMS value of 5 V, but the output was oscillating. This regulator was then replaced to obtain a sine wave at the output of the ADC when the input is given a current sine wave.

Even thought a sine wave was observed, there were more issues since missing codes were seen at

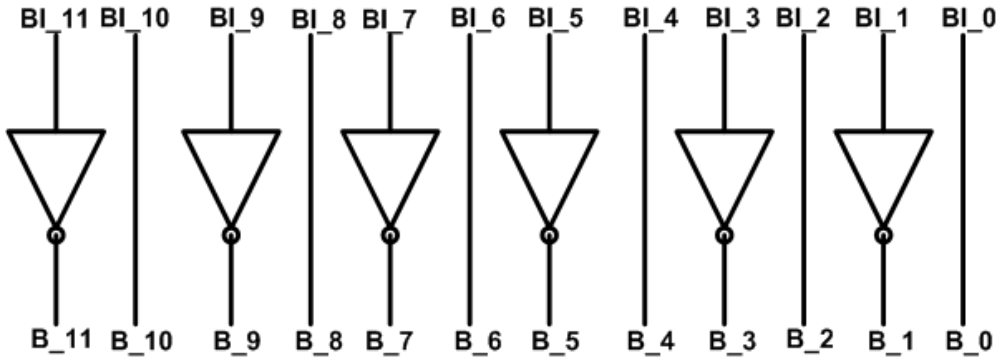

Figure 4.18 Correction of Binary Outputs of the ADC

the output. A regular frequency was observed in the missing codes. Different ranges of values were then recorded with the codes present as well as when the codes were not present. These values were then analyzed. The corrected binary was changed back to the garbled binary to identify the real cause of the problem. After processing, it was apparent that there was no change in bit 3 hence, the ranges of missing codes was observed. Probing on the testboard revealed that a bit on the buffer was nonfunctional, which implied the replacement of a bad commercial component. Replacement of the malfunctioning buffer finally produced binary results which are valid and demonstrate a good DNL with no missing codes at the 5 V supply. Further changes in the Verilog code and the Labview software gave reliable results for the INL. Additional changes are required on the test setup to improve the results for the signal-to-noise ratio. These changes are discussed in Section 4.5.

4.5 Test Setup Changes to Improve Measurements

A good test setup plays an important role in achieving the required characteristics of a data converter. Noise added to the signals from the test system, including supplies and the other instruments, corrupts the input signal. Digital signals have sharp rising and falling edges. These sharp edges cause rapid surges in the current through the ground pin and add noise. If this noise in the digital ground plane is coupled with the analog ground plane, the signal-to-noise ratio reduces because the noise floor rises. It also corrupts the input signal going into the ADC and causes a higher distortion.

The current test setup has a motherboard-daughter card arrangement. Even though the boards are connected, they have different ground planes. Digital signals are transmitted from the mother board to the daughter card. The current setup has single-ended signals generated by the FPGA which is transmitted via a ribbon cable to the daughter board and then to the chip. If differential signaling is implemented, the common mode noise component which appears on both positive and negative signals cancel each other, and reduces the noise entering the daughter card from the FPGA board.[62]

The high frequency clock, which drives both the FPGA and the ADC counter, is generated by a LeCroy pulse generator. This clock is split in two using a T-BNC connector with one cable connected to the ADC chip, and the other to the FPGA board. This results in the clock terminating twice. Thus, the reflections increase and as a result, noise increases. This pulse generator produces a clock of 5 V amplitude to drive the counter. The large amplitude and sharp edges of the clock cause deterioration in the test setup. Additionally, in order to obtain better results, the amplitude is reduced to 3 V, and the rise and fall time is reduced to 3 ns for a 10 ns pulse width. To further improve the noise performance of the ADC, LVDS receivers need to be implemented on the chip. This is discussed in future chapters of this work.

The digitized output of the ADC drives the buffers, which in turn drives the cable to the data acquisition card. This card recognizes a 5 V amplitude digital signal. In order to test the ADC for low voltage capability, incorporate level translators on the board. These level shift the low amplitude digital signals to the 5 V level required by the DAQ card.

The daughter card has a number of temperature dependant components. Resistors are used to convert the voltage signals into currents. The value of the resistors varies over temperature. Additionally, the daughter card has the NI connector which transfers data to the PC. Regulators on the daughter card are rated for a limited temperature range. These factors make temperature testing a challenge, but multiple modifications on the test board help ease the task of characterizing the ADC over temperature.

Additional changes are required on the chip to improve the functionality of the ADC in terms of the INL and the signal-to-noise ratio. These changes are discussed more later.

Chapter 5

Applications and Future Work

Chapter 3 describes the design of the current-mode integrating ADC. The testing procedures and the measurement results obtained for the ADC are discussed in detail as well. It is important however, for any novel architecture, or circuit to find application in industry or additional research. New research is valuable when it provides an application that will considerably improve current state-of-the-art methods. In this chapter, the application of the ADC is discussed in detail.

Research on this current-mode ADC is in an emergent state and requires further improvements in order to achieve the desired specifications. More importantly, the resolution of the ADC needs improvement. Issues with the ramp generator are explained in Section 3.3.1.2. In addition, different methods of generating a current ramp are discussed as future work to improve resolution.

5.1 Applications

The current-mode integrating ADC supports four channels and can be expanded as required. Since the ramp currents are mirrored to the different channels, increasing the number of channels does not increase loading on the ramp generator. Multiple sensors can be connected to the ADC input and the digitized output can be monitored. Many sensors have a current output. These include temperature sensors, vibration, and pressure sensors. These current output sensors are interfaced directly to the ADC input without an intermediate current-to-voltage conversion stage. An added advantage of this architecture is that multiple channels can be configured to support different ranges. Since the ramp is mirrored to the different channels, scale the mirrored currents to support different ranges of current,

providing an added flexibility. Among the most important type of sensors that are targeted to interface to the ADC are photodiodes, and phototransistors, or in generally photodetectors. Photodetectors show the potential for use in a wide variety of applications. A more detailed description of photodetectors, the types, and the applications supported are included in this section.

5.1.1 Optical Detectors

Photodetectors, or photon detectors, are devices that detect the amount of optical power incident on them by producing an electrical signal proportional to the incident power. In general there are two classes of detectors, photon/quantum detectors and thermal detectors [62]. Thermal detectors absorb the incident optical power and convert it into heat. The incident optical power on photon detectors causes changes in the charge carrier states of the material of the photon detectors.

There are three types of photon detectors: photoconductors, photovoltaic, and photoemissive. Photoconductors change their resistance depending on the amount of optical power incident upon them. Photoemissive detectors release electrons during the detection process and provide a large gain. Photovoltaic detectors use p-n junction semiconductors to detect photons and are used in either one of two ways:

1. Photoconductive mode: In this mode of operation the diode is reverse biased. The device responds in the form of a photocurrent instead of a voltage. Most applications require a transimpedance amplifier to convert this photocurrent to voltage. This mode has advantages such as lower capacitance, higher speed, and better linearity [62]. It also shows the ability to process decades of light illumination. However, this mode shows a higher dark current.
2. Photovoltaic mode is used in low frequency applications up to 350 KHz and low-light level applications. In this mode of operation, the photodiode is operated without bias, or

the open circuit voltage obtained upon irradiation [64] is further processed for digitization. This configuration also requires a transimpedance amplifier for most applications.

Avalanche photodiodes are photoconductive detectors. Avalanche photodiodes provide a higher gain than p-n junction diodes. This internal gain not only reduces the signal-to-noise ratio of the system, but also reduces the gain requirement on the transimpedance amplifier employed at the output of the photodiodes to improve the signal level.

Both photovoltaic (voltage-mode) and photoconductive (current-mode) circuits require an amplifier to amplify the voltage (photovoltaic), or to convert it to a voltage signal and amplify (photoconductive) the signal output of the photodetector. Figure 5.1 provides an example, of the circuit configuration used for photovoltaic as well as photoconductive mode of operation.

Both modes of operation require an amplifier, and particularly in the latter case, a conversion from current to voltage is required. In order to digitize the data from these detectors, an additional component, the transimpedance amplifier, is added at the input to the data converter. To maintain the

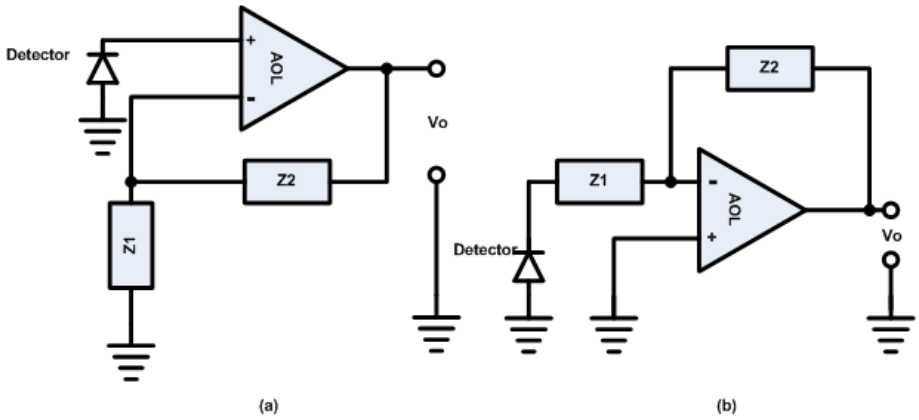

Figure 5.1 (a) Circuit Configuration for Photovoltaic Mode (b) Circuit Configuration for Photoconductive Mode [63]

linearity and accuracy of the converter, stringent requirements must be met by the amplifier with respect to bandwidth, linearity, and gain. This adds complexity to the converter and increases power consumption. The usage of the current-mode integrating ADC with photodetectors is thus suitable as it eliminates the transimpedance amplifier completely, saving power, area, and complexity of design.

5.1.2 Spectroscopy

Section 5.1.1 explains the different types of photodetectors. Photodiodes are used in a wide variety of applications. These include position sensing, biomedical applications, bar code readers, laser printers, and spectroscopy. The photodiode is biased depending on the application. Spectroscopy is an application, which may require an analog-to-digital converter with multiple channels and, where a lower speed suffices.

Atoms, molecules and ions absorb light. Photons have energy associated with them which is directly proportional to the frequency or inversely proportional to the wavelength. This energy, when absorbed, causes excitation of electrons in atoms, or rotational or vibrational changes, which are associated with the molecules [65]. As a result, different types of substances have different atomic or molecular configurations and hence, varying energy levels are required to cause any of the above mentioned changes. The extent to which any material absorbs light depends upon the wavelength of light. The absorption spectra is used to analyze chemicals or gases to determine their composition and concentrations.

The absorbance spectrum of a substance is a plot of the absorbance versus the wavelength. It is characterized by the wavelength at which the absorbance is the greatest for a specific group or chemical compound. Beer's Law states that "absorbance is directly proportional to the path length through which the light of a specific wave length passes and the concentration of the analyte. This is given in Equation 5.1 as

$$A = \varepsilon \times c \times t \qquad (5.1)$$

where A is the absorbance, ε is the molar absorptivity, c is the concentration of the analyte and t is the path length."

Figure 5.2 shows examples of the absorption spectra of common molecules. From the figure, it is clear that different compounds absorb light at different wavelengths. Monitoring the changing environment and the different gases present in the atmosphere is important in view of the health risks involved caused by pollution and climate change. Monitoring the ozone level in the atmosphere is especially important given that a depleting ozone layer implies less filtering of ultraviolet light and additional health risks to all living things. The other applications of spectroscopy include finding the bandgap of semiconductors using the absorbance information, and Raman and vibrational spectroscopy to identify materials. Spectroscopy is identified as one of the primary applications of this ADC.

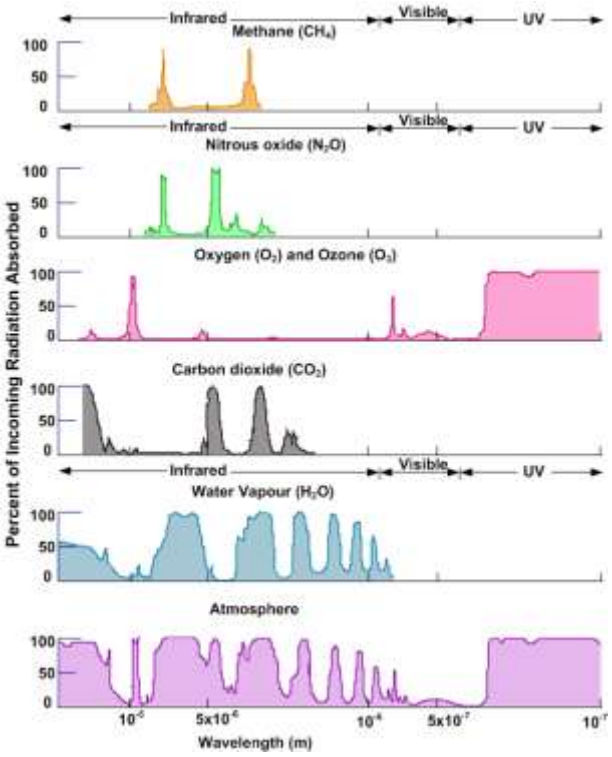

Figure 5.2 Example Absorption Spectra [66]

Light is divided into different ranges depending on the wavelength. The ranges are ultraviolet, visible, and infrared. Figure 5.3 shows the different optical bands. Ultraviolet has the lowest wavelength, followed by the visible region. Finally, the infrared section occupies the longest wavelength region. Photodiodes are available and used in all the three regions of operation. The material utilized to manufacture the semiconductor device is varied depending on the specific wavelength that is to be detected.

Spectroscopy is performed in all three regions of the optical band. Present techniques in spectrophotometers convert the photocurrent to voltage for further processing. As explained in Section 5.1.1, this conversion requires additional components, such as operational amplifiers that cause additional bandwidth issues and noise limitations. The work in [68] shows the use of the integrating ADC with photocurrents from multiple channels converted into voltages using OTAs.

The current mode ADC in this work can process the photocurrent directly and convert it to digital without the intermediate stage of converting the photocurrent to a voltage. This avoids nonlinearities, bandwidth issues, and the offset caused by the added intermediate transimpedance stage.

5.1.3 Other Applications

Many sensors have current output. In applications, the current output is converted to voltage using transimpedance amplifiers. The voltage is then processed and converted to digital. Examples of

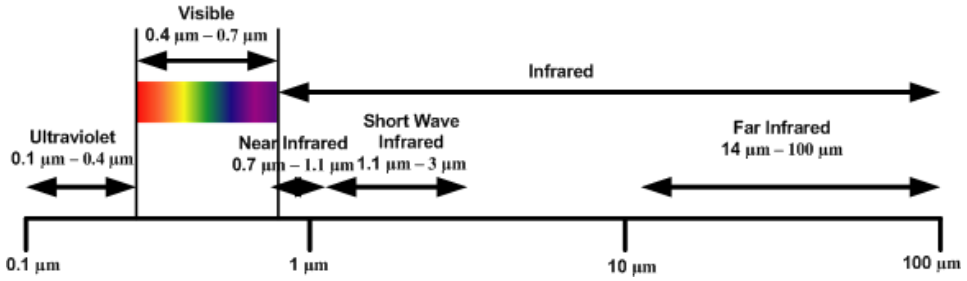

Figure 5.3 Optical Bands

current output sensors include pressure sensors and level sensors for fluid level in industry. Another area of application is biomedical with electrodes that output current signals. The output current of electrodes is converted to voltage for digitization. The electrodes are directly connected to the current-mode ADC. This method is also used in the pH determination of chemicals.

An additional advantage of this ADC is that the voltage mode and the current mode integrating ADC can be used concurrently. If the timing is the same for both, the same counter may be used, saving chip area. This also allows the interface of both types of sensors.

5.2 Future Work

5.2.1 Ramp Generator Issues

In Section 3.3.1.2, the current ramp generator is discussed. This circuit is designed and tested as part of the current-mode integrating ADC. The measurement results of the ADC show a 12-bit DNL, but an INL that is not 12-bit. The INL result is attributed to the current ramp generator. The current ramp generator is simulated and the voltages and currents at the different nodes recorded. The data collected is used to calculate the linearity. A best fit line is plotted through the ramp. The deviation of the ramp current from the best fit line is then computed and plotted. Figure 5.4 shows the plot of the variations in the current with respect to the best fit line passing through the current ramp.

For a 12-bit resolution, the minimum current that is to be resolved is given by Equation 5.2.

$$MinCurrent = \frac{CurrentRange}{4096} = \frac{180 \times 10^{-6}}{4096} = 43 \times 10^{-9}\, A \qquad (5.2)$$

The current variation, as shown in the above figure, is much larger than the value provided by Equation 5.2. Hence, the causes for this deviation, and possible solutions to resolve this nonlinearity, are investigated.

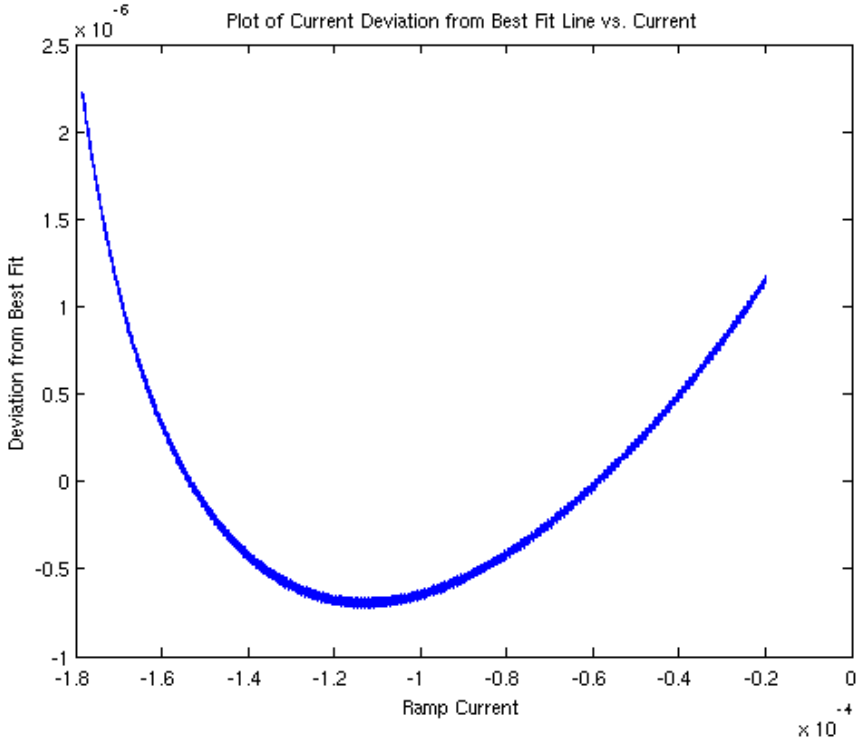

Figure 5.4 Ramp Nonlinearity

The main cause of the nonlinearity is the transconductance amplifier used in the ramp generator. A high linearity OTA is required to convert the voltage across the capacitor into the required current. A p-input differential pair is used as a transconductance amplifer. As the capacitor is charging, following the virtual ground rule, the positive input is linearly increasing and the negative input follows the positive input. Figure 5.5 shows the two plots. The positive input plot shows the deviation of the input of the OTA with respect to the best fit line. This input indicates a linearity of more than 12-bits. The negative input plot depicts the deviation of the negative input of the OTA from the best fit line. A comparison of the two inputs show that the negative input does not perfectly follow the positive input and demonstrates less than a 12-bit linearity. Therefore, the OTA is the primary cause of nonlinearity.

When the switch discharging the capacitor is closed, the voltage at the top of the capacitor becomes 0V. The transistor at the output of the OTA, which is Mn1 from Figure 3.4, leaves the saturation

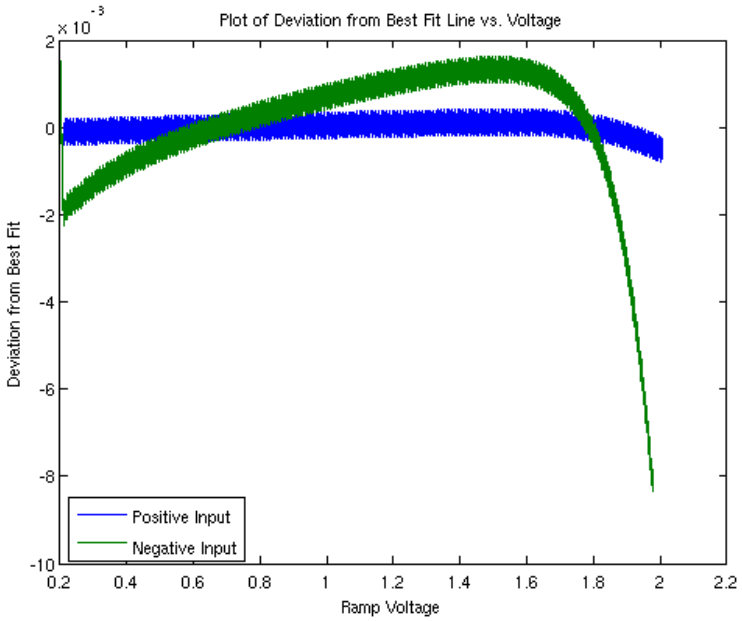

Figure 5.5 Deviation of the Negative Input of the OTA from the Positive Input and Best Fit Line

region since the gate voltage of the transistor reduces to below the threshold voltage. Hence, the startup of the ramp current shows a glitch which lasts until this transistor returns to saturation.

Alternatives to the current ramp generator are investigated to improve the performance and linearity of this circuit block. The next section discusses possible topologies that may require further investigation to achieve the needed specifications.

5.2.2 Active Inductor Gyrator Current Ramp

Similar to the capacitor which generates a linear voltage with respect to time when supplied by a constant current source, the inductor generates a linear current with respect to time when supplied by a constant voltage source. Figure 5.6 shows an example of the inductor generating a current ramp when supplied by a constant voltage source.

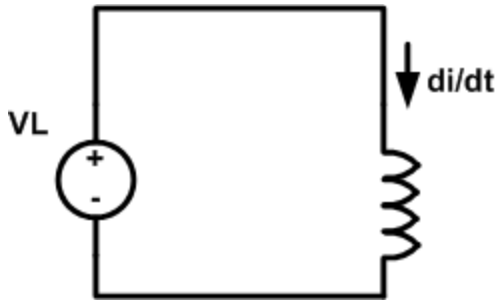

Figure 5.6 Inductor Current Ramp

The equation of the inductor is shown in Equation 5.3. If the voltage source and the value of the inductor are constant, the slope of the current with respect to time is constant.

$$VL = L\frac{di}{dt} \tag{5.3}$$

Inductors occupy a large amount of space on the chip. The larger the value of the inductor, the more space it occupies on the chip. Active inductors are proposed which make use of current conveyors to emulate the properties of the inductor. Figure 5.7 is an example of a floating impedance inverter using three transconductance amplifiers.

The possibility of using an active inductor to generate the current ramp requires further investigation. The active inductor value can be changed with the help of external biases and offers tunability.

5.2.3 Current Ramp with MOSFETs in Weak Inversion

A more promising alternative to generating the current ramp uses MOSFETs in weak inversion to generate a linearly increasing current. This circuit is adapted from [70]. In [70] the ramp is a triangular waveform controlled by the minimum and maximum currents which control the charging and discharging of the capacitor. In this case, only the current ramp in one direction is required for the operation of the

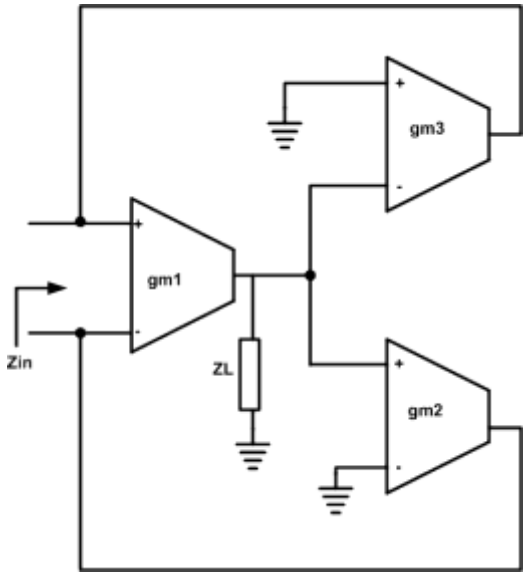

Figure 5.7 Floating Impedance Inverter [69]

ADC; therefore, the additional circuitry requiring the rise and fall rate as well as the minimum and maximum current comparison is eliminated.

Figure 5.8 shows the circuit of the current ramp generator. The reference current *Iref* generates *Vref* which is the compressed voltage. The transistor Mw1-5 is biased in the weak inversion. The transistor Mw1 acts as a compressor, whereas the transistor Mw5 acts as the log-domain expander. Mp7 sources the tuning current *Itune* to the transistor Mw4. Transistors Mn1 and Mn2 act as level shifters. Equations for producing the ramp current are derived in the following paragraphs.

The large signal model of a NMOS transistor in weak inversion is given in Equation 5.4

$$I_D = I_S e^{\frac{V_{GS} - V_T}{nU_T}} \tag{5.4}$$

where I_D is the drain current, V_{GS} is the gate to source voltage of the transistor, V_T is the threshold voltage, I_S is the saturation current, n is the subthreshold slope, and U_T is the thermal voltage, given in Equation 5.5 as

$$U_T = \frac{kT}{q} \quad . \tag{5.5}$$

Equation 5.4 assumes that the bulk voltage is 0 V. Let V_2 be the source voltage of transistors Mw2 and Mw5. Let V_1 be the source voltage of transistors Mw3 and Mw4. Using Equation 5.4, the drain current of Mw4 is shown as Equation 5.6. The source voltage of the Mw4 transistor is derived in Equation 5.6

$$\begin{aligned} I_{tune} &= I_S e^{\frac{Vtri - V_1 - V_T}{nU_T}} \\ \therefore V_1 &= Vtri - V_T - nU_T \ln \frac{I_{tune}}{I_S} \end{aligned} \tag{5.6}$$

where *Vtri* is the voltage at the top of the charging capacitor. Similarly, let the current flowing through Mw2 be I_{ref}. This current is given by Equation 5.7, and the source voltage V_2 is derived as in Equation 5.7.

$$\begin{aligned} I_{ref} &= I_S e^{\frac{Vref - V_2 - V_T}{nU_T}} \\ \therefore V_2 &= Vref - V_T - nU_T \ln \frac{I_{ref}}{I_S} \end{aligned} \tag{5.7}$$

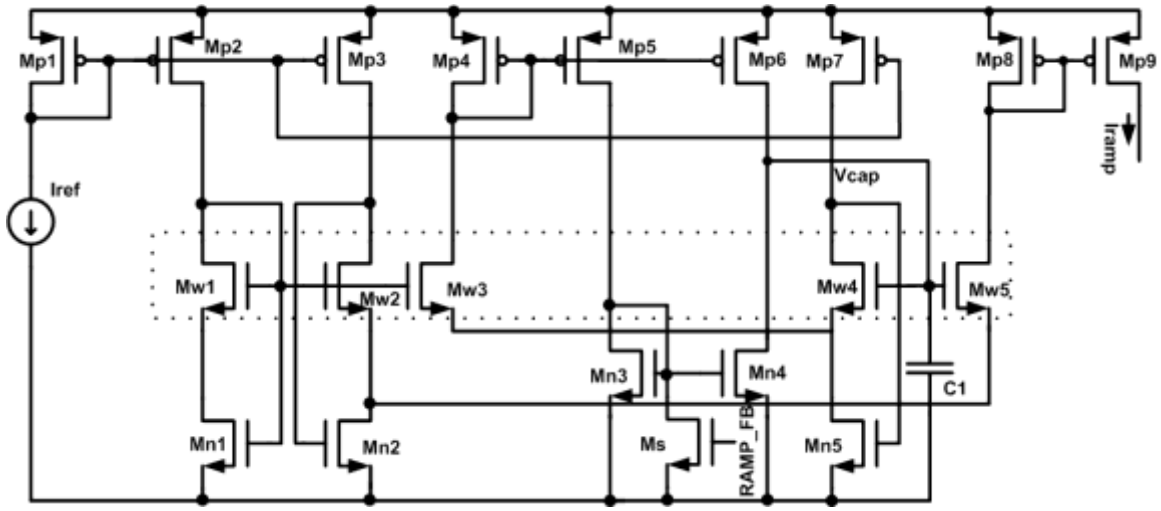

Figure 5.8 Ramp Generator Using NMOS Transistors in Weak Inversion [70]

The current charging the capacitor at the gate node of Mw5 is mirrored from transistor Mp4 to transistors Mp5 and Mp6. This charging current is derived using the drain current equation of transistor Mw3. This current is derived in Equation 5.8.

$$I_{cap} = I_S e^{\frac{Vref - V_1 - V_T}{nU_T}} \tag{5.8}$$

By substituting for V_1 from Equation 5.6 into Equation 5.8, the charging current is given as Equation 5.9.

$$\begin{aligned} I_{cap} &= I_S e^{\frac{Vref - \left(Vtri - V_T - nU_T \ln\frac{I_{tune}}{I_S}\right) - V_T}{nU_T}} \\ I_{cap} &= I_S e^{\frac{Vref - Vtri}{nU_T}} \times \frac{I_{tune}}{I_S} \\ I_{cap} &= C\frac{dVtri}{dt} = I_{tune} e^{\frac{Vref - Vtri}{nU_T}} \end{aligned} \tag{5.9}$$

To obtain a linear ramp current at the transistor Mw5, assume the equation of the derivative of the current with respect to current as in Equation 5.10 [70] where τ is a time constant.

$$\frac{dItri}{dt} = \frac{Iref}{\tau} \tag{5.10}$$

Using Equation 5.4 to define $I_{tri,}$ Equation 5.11 is written. From Equation 5.11 V_{tri} is derived as shown in Equation 5.12.

$$Itri = I_S e^{\frac{Vtri - V_S - V_T}{nU_T}} \tag{5.11}$$

$$Vtri = nU_T \ln\left(\frac{Itri}{I_S}\right) + V_S + V_T \tag{5.12}$$

Differentiating Equation 5.12 with respect to time, Equation 5.13 is obtained.

$$\frac{dVtri}{dt} = nU_T \times \frac{I_S}{Itri} \times \frac{1}{I_S} \frac{dItri}{dt} \tag{5.13}$$

Substituting from Equations 5.11 and 5.10 into Equation 5.13, Equation 5.14 is written as

$$\frac{dVtri}{dt} = nU_T \times \frac{Iref}{\tau} \times \frac{e^{-\frac{Vtri - V_S - V_T}{nU_T}}}{I_S} \quad . \tag{5.14}$$

The equation for *Iref* is written as in Equation 5.15. The source voltage V_S of the transistor with drain current *Iref* is equal to that of the transistor with the drain current *Itri.*

$$Iref = I_S e^{\frac{Vref - V_S - V_T}{nU_T}} \tag{5.15}$$

By substituting from Equation 5.15 into Equation 5.14, the equation is written as Equation 5.16.

$$\frac{dVtri}{dt} = nU_T \times \frac{I_S e^{\frac{Vref - V_S - V_T}{nU_T}}}{\tau} \times \frac{e^{-\frac{Vtri - V_S - V_T}{nU_T}}}{I_S}$$
$$\therefore \frac{dVtri}{dt} = \frac{nU_T}{\tau} e^{\frac{Vref - Vtri}{nU_T}} \tag{5.16}$$

Equation 5.16 is equal to that obtained from Equation 5.9. Comparing the two equations, it is derived that the value of current Itune is as shown in Equation 5.17 [70].

$$I_{tune} = \frac{CnU_T}{\tau} \tag{5.17}$$

Since Equations 5.16 and 5.9 are equal, it is shown that a linear current ramp is obtained by using transistors in weak inversion in the above topology.

The topology in [70] is used to generate a triangular wave with the upper and lower limits set by current sources. Hence, the charging and discharging rates are equal. This topology is modified since a sawtooth wave is required for the current-mode ADC. The discharging rate of the capacitor is required to be faster when compared to the charging rate. The capacitor charges through the PMOS transistor Mp6

and discharges through transistor Mn4. The current flowing through the Mn4 transistor is determined by the sizing of transistors Mp5, Mn3, and Mn4. Mp5 is scaled higher than Mp4 and Mn4 is again scaled to a larger size when compared to Mn3. Instead of the minimum and maximum set level current, an externally timed RAMP FB switch is used to charge and discharge the capacitor. When this switch is ON, the gate of transistor Mn3 is pulled *low* and the capacitor charges through transistor Mp6. When the switch is turned OFF, the current mirror Mn3, Mn4 become active and the capacitor discharges.

An additional advantage of this topology is the possibility of using the same circuit in BiCMOS processes, where the NMOS transistors in weak inversion are replaced with BJTs, achieving better performance characteristics. Further investigation into this topology is required to calculate linearity and offset.

5.2.4 Other Improvements

An alternative topology for the current ramp generator is described in Section 5.2.3. Another drawback of the ramp generator is that the capacitor has to be implemented off chip because of the area constraint. Implementing an on-chip capacitor reduces nonlinearity caused by the bond pad and the bond-wire inductance.

A bias voltage is needed by the comparator to bias the OTAs that form the active current mirrors. Generating reference voltages on the board, with the help of resistors, results in temperature dependence. If these voltages are generated with supplies, additional testing overhead also increases measurement error. Generating this voltage on-chip with a voltage reference will reduce the number of components required for testing this ADC and produce better noise characteristics as well.

The counter that is needed for the operation of the ADC requires a high frequency clock to operate. The clock is scaled with the sampling rate of the ADC. For a 5 V supply, the clock swings from 0 to 5 V. The fast edges of the clock inject noise into the system and largely reduce the signal-to-noise ratio.

Using LVDS receivers on the chip will help reduce this noise. The advantages of LVDS signaling include a low voltage so the fast edges have a smaller swing when compared to a 5V clock. An added advantage of using LVDS is the differential voltages which imply that the noise on one clock is cancelled by the noise on the other.

The switched capacitor circuits on the ADC and the digital section require digital signals. These signals are now provided externally to the chip using an FPGA. Synthesizing this state machine on chip will help reduce the overhead and will also help reduce noise injected by the FPGA into the ground. This will enable testing of the current-mode ADC at low voltages.

For the applications described, future research can include the implementation of photodiodes on-chip interfaced to the ADC. This also requires the characterization and measurement of the on-chip photodiodes to estimate the required current range that is to be digitized.

Conclusion

5.3 Summary and Conclusion

Multi-channel ADCs are commonly used in applications where multiple sensors need to be interfaced and digitized. Multi-channel ADCs require a lower power consumption and for the purpose of sensor interface, do not require a high sampling rate. A background of current-mode circuits is provided in this work. As well as a thorough literature review of the various types of current-mode ADCs. An example of each different type of architecture is described and two multi-channel current ADCs are described with their advantages and disadvantages.

This research was performed in phases. Initially, current-mode circuits were investigated. A unique way was identified to incorporate these design techniques into the existing Wilkinson ADC so that the advantages of this mode of circuit design can be used to overcome certain problems existing in voltage-mode architecture. The applications of this architecture are then defined. The sub-blocks of the architecture are defined and designed according to the required specifications. The current-mode ADC is fabricated using an AMI 0.5 µm CMOS process. Next, test boards were designed to characterize the ADC. The circuits were tested at room temperature for each of the different parameters. This is the methodology followed to complete the goals of this research.

The contents of this dissertation includes a comparison of current-mode versus voltage-mode, This work describes a current-mode multi-channel ADC. The main blocks of the ADC are described and include the current ramp generator, the current comparator, and the Gray code counter. The current ramp

generator is designed to mitigate the effects of nonlinearity. A novel Gray code counter was designed to support a frequency of counting up to 200 MHz. A description of the digital section of the ADC, including the latches, and the Gray code to binary converter are provided. Issues with the current digital section are described and include inversion of the Gray code. The method used to correct the inverted Gray code, in Labview, without reversing the conversion to binary is explained.

The parameters of the ADC, including the DNL, the INL, the SNR, and the SNDR, are discussed. The test board designed to test the current-mode ADC is described, along with the layer setup. This test setup includes two boards, a motherboard, including an FPGA to generate the digital signaling, and a daughter card with the ADC chip and supply regulators.

DNL is measured using the histogram method, by taking a large number of samples. INL is then computed using the DNL values. Both the SNR and SNDR are measured using FFT. Improvements in the current test setup are suggested. Table 5-1 provides a summary of the measured parameters of the ADC.

Table 5-1 Summary of ADC Measurement Results

Parameter	**Current-mode ADC**
Process	CMOS 0.5µ
Supply	5 V
Channels	4
Area	1mm x 1mm
DNL	<0.5 LSB
INL	<70 LSB
SNR	>35 dB
SNDR	>30 dB
THD	<7 dB

To further this research, possible applications of this ADC are described. These include spectroscopy using photodiodes as sensors to interface to the inputs of the ADC. Future work, involving a new ramp generator circuit for better linearity and other improvements, are explained.

5.4 Original Contributions

Section 1.4 outlines the motivation for this work. Since the general trend is towards low voltage circuits, this work provides insight into additional techniques for accommodating existing technology into low supply voltages. The original contributions of this work are listed below.

- A novel multi-channel current-mode ADC architecture is proposed. This architecture has a wide scope of applications, especially when photosensor currents need to be digitized.
- A current ramp generator is designed to provide good linearity and stability over temperature.
- A novel Gray code counter architecture is used. It shows a capability of counting at a higher speed by eliminating feedback from the more significant bits to bits of lower significance. A concern involving missing codes at higher frequency counting is dealt with by utilizing the carry look-ahead technique and thus, avoiding the effects of clock skew in the latter stages.

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Appendices

Appendix A

Verilog Code

This verilog code is used to generate the digital timing signals between the ADC chip and the FPGA.

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
//////
// Company:
// Engineer:
//
// Create Date:    11:31:16 09/25/2008
// Design Name:
// Module Name:    CM_ADC_test
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
//////
module cm_adc_1(
            Clock,       //Clock input
            SOC,         //Start of conversion
            EOC,         //End of Conversion (full scale count)
            Chip_Enable, //Chip Enable
            S1_samp_sw, //Feedback of the ramp circuit
            S2_vgoff, //Controls input to the comparator from the ramp
            S3_rmpfb, //External input signal
            S4_rmpcn,  //Feedback of the comparator
            cen, //Start gray code counter
            Refresh, // Transfer contents of the latch to register
            Ch_select,  //Select output channel to read
            Reset,
            chgdet
```

```
            );


`define CQ 1
`define COUNT_4095_MAX  16'hFFFF

// *** state DEFINITIONS

`define ST_DONE_WAIT          4'b0000
`define ST_RMP_INP_OPEN       4'b0001
`define ST_RMP_DISC           4'b0010
`define ST_SAMP_VGOFF_CLOSE   4'b0011
`define ST_REF_OPEN     4'b0100
`define ST_RES_VGOFF_OPEN     5'b0101
`define ST_SAMP_OPEN    4'b0110
`define ST_RMP_START          4'b0111

`define ST_RMP_CN       5'b1000
`define ST_CNT_ENABLE 5'b1001
`define ST_CH_SEL_00          4'b1010
`define ST_CH_SEL_01          4'b1011
`define ST_CH_SEL_10          4'b1100
`define ST_CH_SEL_11          4'b1101

`define ST_CH_SEL_END         5'b1110

`define COUNT_RMP_INP_SWO     16'h0004
`define COUNT_SAMP_SWCO 16'h0081 //014B
`define COUNT_REF_OFF   16'h0090 //0154
`define COUNT_RESET_VGOFF_OPEN      16'h00110 //0159
`define COUNT_SAMP_OFF  16'h014F //16'h015E
`define COUNT_RMPFB_OPEN      16'h017F //16'h016A
`define COUNT_RMPCN 16'h036F  //16'h01C4
`define COUNT_CEN 16'h0370
`define COUNT_CH_SEL_00       16'h05CD//16'h021E
`define COUNT_CH_SEL_01       16'h05E1       //16'h0278
`define COUNT_CH_SEL_10       16'h0610//16'h02D2
`define COUNT_CH_SEL_11       16'h0649//16'h032C

`define COUNT_CH_SEL_END 16'h0D13//16'h081E


output S1_samp_sw, S2_vgoff, S3_rmpfb, S4_rmpcn, cen, Refresh,Reset;
output chgdet;
//
output [1:0] Ch_select;
//output S2_vgoff, Refresh;

reg S1_samp_sw, S2_vgoff, S3_rmpfb, S4_rmpcn, cen, Refresh,Reset, chgdet;
reg [1:0] Ch_select;

// *** INTERNAL REGISTERS
```

```
reg [3:0] state;

reg [11:0] ADC_out;
reg start_cnt4095;                    // To start the 16bit counter

reg start_cnt_counter;
reg [15:0] count_4095;
reg [11:0] count_cntr4095;
reg  enable, start, EOC_sig, EOC_edge;


// *** INTERNAL WIRES
input Clock,SOC,EOC,Chip_Enable;
initial
begin
#`CQ state = 4'b0000;
end

always @(posedge Clock)
begin
      #`CQ enable = Chip_Enable;
end

always @(posedge Clock)
begin
      #`CQ start = SOC;
end


always @(posedge Clock)
begin
if(enable==1)
 begin
 if(start==1)
      begin

      case (state)
      `ST_RMP_INP_OPEN:  // Open switch between ramp and comparator 20ns
    begin
            #`CQ S4_rmpcn = 1'b0;
            #`CQ S1_samp_sw = 1'b0;
            #`CQ S2_vgoff = 1'b0;
            #`CQ S3_rmpfb = 1'b1;
            #`CQ cen = 1'b0;
            #`CQ Refresh = 1'b0;
            #`CQ Ch_select = 2'b00;
            #`CQ Reset = 1'b1;
            #`CQ chgdet = 1'b0;
             if (count_4095 == 16'h0008)//'COUNT_RMP_INP_SWO)
              begin
              #`CQ state = `ST_SAMP_VGOFF_CLOSE;
              end
```

```
            else
             begin
             #`CQ state = `ST_RMP_INP_OPEN;
             end
    end

      `ST_SAMP_VGOFF_CLOSE: //Closes both switches autozero and input sample
and ramp feedback 1.83us
               begin
            #`CQ S1_samp_sw = 1'b1;
            #`CQ S2_vgoff = 1'b1;
            #`CQ Refresh = 1'b1;
            #`CQ chgdet = 1'b0;
             if (count_4095 == `COUNT_SAMP_SWCO)
              begin
              #`CQ state = `ST_REF_OPEN;
              end
             else
              begin
              #`CQ state = `ST_SAMP_VGOFF_CLOSE;
              end

               end

      `ST_REF_OPEN:  //Opens autozero switch 50ns
            begin
            #`CQ Refresh = 1'b0;
       if (count_4095 == `COUNT_REF_OFF)
       begin
             #`CQ state = `ST_RES_VGOFF_OPEN;
             end
            else
             begin
             #`CQ state = `ST_REF_OPEN;
             end
            end

      `ST_RES_VGOFF_OPEN:  //Opens sampling switch of the comparator 30ns
            begin
            #`CQ S2_vgoff = 1'b0;
            #`CQ Reset = 1'b0;
            if (count_4095 == `COUNT_RESET_VGOFF_OPEN)
              begin
              #`CQ state = `ST_SAMP_OPEN;
              end
             else
              begin
              #`CQ state = `ST_RES_VGOFF_OPEN;
              end
            end

      `ST_SAMP_OPEN:  // Closes switch between ramp and comparator 20ns
```

```
            begin
            #`CQ S1_samp_sw = 1'b0;
            #`CQ Reset = 1'b1;
             if (count_4095 == `COUNT_SAMP_OFF)
              begin
              #`CQ state = `ST_RMP_START;
              end
             else
              begin
              #`CQ state = `ST_SAMP_OPEN;
              end
            end

      `ST_RMP_START:   // Opens feedback switch of the ramp generator ramp
starts

            begin
            #`CQ S3_rmpfb = 1'b0;
            if (count_4095 == `COUNT_RMPFB_OPEN)
              begin
              #`CQ state = `ST_RMP_CN;
              end
             else
              begin
              #`CQ state = `ST_RMP_START;
              end
            end

      `ST_RMP_CN:  // Connects ramp to the comparator
            begin
            #`CQ S4_rmpcn = 1'b1;
            if (count_4095 == `COUNT_RMPCN)
              begin
              #`CQ state = `ST_CNT_ENABLE;
              end
             else
              begin
              #`CQ state = `ST_RMP_CN;
              end
            end

      `ST_CNT_ENABLE:   //Enables Counter
            begin
            #`CQ cen = 1'b1;
            #`CQ start_cnt_counter = 1'b1;
            #`CQ Ch_select = 2'b00;
            #`CQ chgdet = 1'b1;
            if (count_4095 == `COUNT_CEN)
              begin
              #`CQ state = `ST_CH_SEL_00;
              end
             else
```

```
        begin
        #`CQ state = `ST_CNT_ENABLE;
        end
      end

`ST_CH_SEL_00: // Reads first channel
      begin
      #`CQ Ch_select = 2'b00;
      #`CQ chgdet = 1'b1;
       if (count_4095 == `COUNT_CH_SEL_00)
        begin
        #`CQ state = `ST_CH_SEL_01;
        end
       else
        begin
        #`CQ state = `ST_CH_SEL_00;
        end
      end

`ST_CH_SEL_01: // Reads second channel
      begin
      #`CQ Ch_select = 2'b01;
       #`CQ chgdet = 1'b0;
       if (count_4095 == `COUNT_CH_SEL_01)
        begin
        #`CQ state = `ST_CH_SEL_10;
        end
       else
        begin
        #`CQ state = `ST_CH_SEL_01;
        end
      end

      `ST_CH_SEL_10: // Reads third channel
      begin
      #`CQ Ch_select = 2'b10;
      #`CQ chgdet = 1'b0;
       if (count_4095 == `COUNT_CH_SEL_10)
        begin
        #`CQ state = `ST_CH_SEL_11;
       end
       else
        begin
        #`CQ state = `ST_CH_SEL_10;
        end
      end

`ST_CH_SEL_11: // Reads fourth channel
      begin
       #`CQ Ch_select = 2'b11;
       #`CQ chgdet = 1'b0;
       if (count_4095 == `COUNT_CH_SEL_11)
```

```
        begin
        #`CQ state = `ST_CH_SEL_END;
        end
       else
        begin
        #`CQ state = `ST_CH_SEL_11;
        end
      end


`ST_CH_SEL_END: // All channels read wait for ramp to end
      begin
       #`CQ Ch_select = 2'b00;
      if(count_cntr4095==12'hFFE)
      begin
       #`CQ Refresh = 1'b0;
       #`CQ start_cnt_counter = 1'b0;
       #`CQ state = `ST_DONE_WAIT;
       #`CQ S3_rmpfb = 1'b1;
       #`CQ cen = 1'b0;
       end

 end

`ST_DONE_WAIT: // End of conversion
      begin
      #`CQ S4_rmpcn = 1'b0;
      #`CQ S1_samp_sw = 1'b0;
      #`CQ S2_vgoff = 1'b0;
      #`CQ S3_rmpfb = 1'b0;
      #`CQ cen = 1'b0;
      #`CQ Refresh = 1'b0;
      //#`CQ Ch_select = 2'b00;
      #`CQ Reset = 1'b1;
      #`CQ chgdet = 1'b0;
      #`CQ state = `ST_RMP_INP_OPEN;
      end

      default: // End of conversion
      begin
      #`CQ S4_rmpcn = 1'b0;
      #`CQ S1_samp_sw = 1'b0;
      #`CQ S2_vgoff = 1'b0;
      #`CQ S3_rmpfb = 1'b0;
      #`CQ cen = 1'b0;
      #`CQ Refresh = 1'b0;
      #`CQ Ch_select = 2'b00;
      #`CQ Reset = 1'b0;
      #`CQ chgdet = 1'b0;
      #`CQ state = `ST_RMP_INP_OPEN;
      end
```

```
endcase
end
else begin
      #`CQ chgdet = 1'b0;
      end

end
else
            begin
            #`CQ S4_rmpcn = 1'b0;
            #`CQ S1_samp_sw = 1'b0;
            #`CQ S2_vgoff = 1'b0;
            #`CQ S3_rmpfb = 1'b0;
            #`CQ cen = 1'b0;
            #`CQ Refresh = 1'b0;
            #`CQ Ch_select = 2'b00;
            #`CQ Reset = 1'b0;
            #`CQ chgdet = 1'b0;
            #`CQ state = `ST_RMP_INP_OPEN;
            end

end

always @(posedge Clock)
begin
if(enable==1)
   begin
         if(start==1)
         begin
               if (count_cntr4095>=12'hFFE) //(EOC_sig == 1)
            begin
             #`CQ start_cnt4095 = 1'b1;
             #`CQ count_4095 = 16'h0000;
            end
             else
             begin
                  #`CQ count_4095 = count_4095 + 1'b1;
             end
          end
    else
            begin
                  #`CQ count_4095 = 16'h0000;
            end
      end
else
      begin
      #`CQ start_cnt4095 = 1'b0;
      #`CQ count_4095 = 16'h0000;
      end
end
//
```

```
always @(posedge Clock)
begin
if(enable==1)
   begin
         if(start==1)
         begin
               if(start_cnt_counter == 1)
            begin
              #`CQ count_cntr4095 = count_cntr4095 + 1'b1;
             end
                        else
                        begin
                        #`CQ count_cntr4095 = 12'h000;
                        end
            end
            else
            begin
                  #`CQ count_cntr4095 = 12'h000;
          end
       end
       end

endmodule
```

Appendix B

Labview Program

The Labview program is written to interface the computer with the instruments. These include the Audio Precision waveform generator and the Keithley current source. Figure B.1 depicts the first block of the Labview program. The data is collected using the change detection method. If the current source is used as an input, this block also allows the current source to be stepped through the range of values while the data is collected.

Figure B.2 illustrates the block which controls the Keithley current source and provides the ability to generate the steps of current. Figure B.3 shows the block which is used to process the acquired

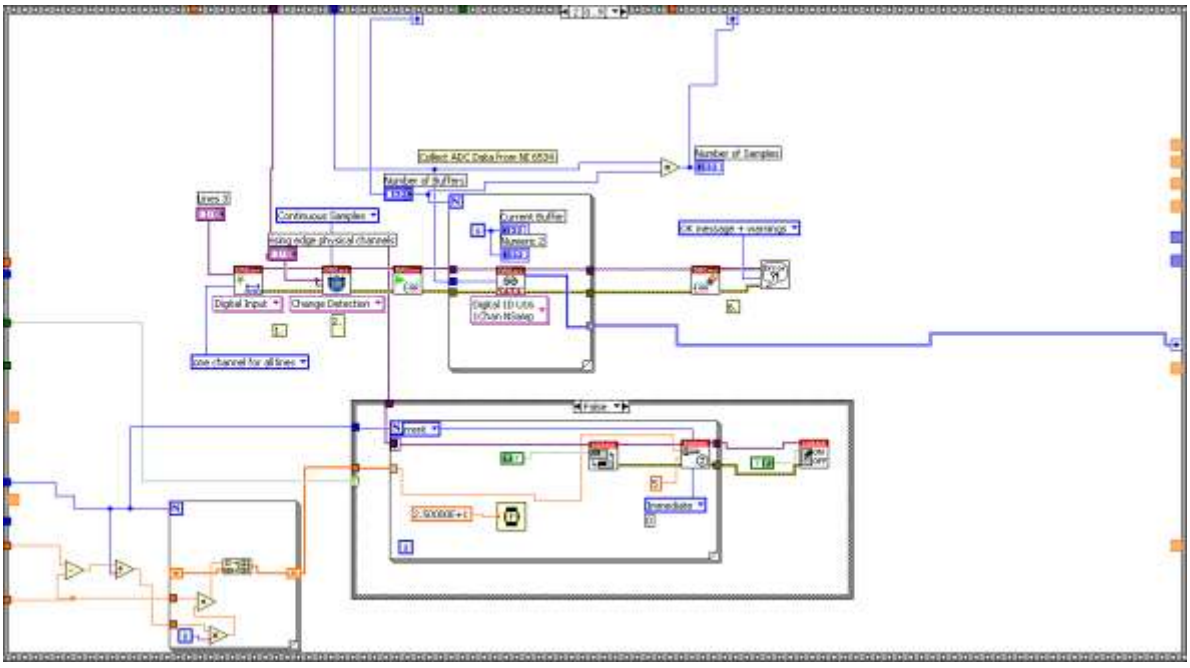

Figure B.1 Data Collection

data. 12-bit data is extracted from the 16-bit data that is captured. In order to calculate DNL using the histogram technique the histogram of an ideal sine wave is calculated using the block depicted in Figure B.4.

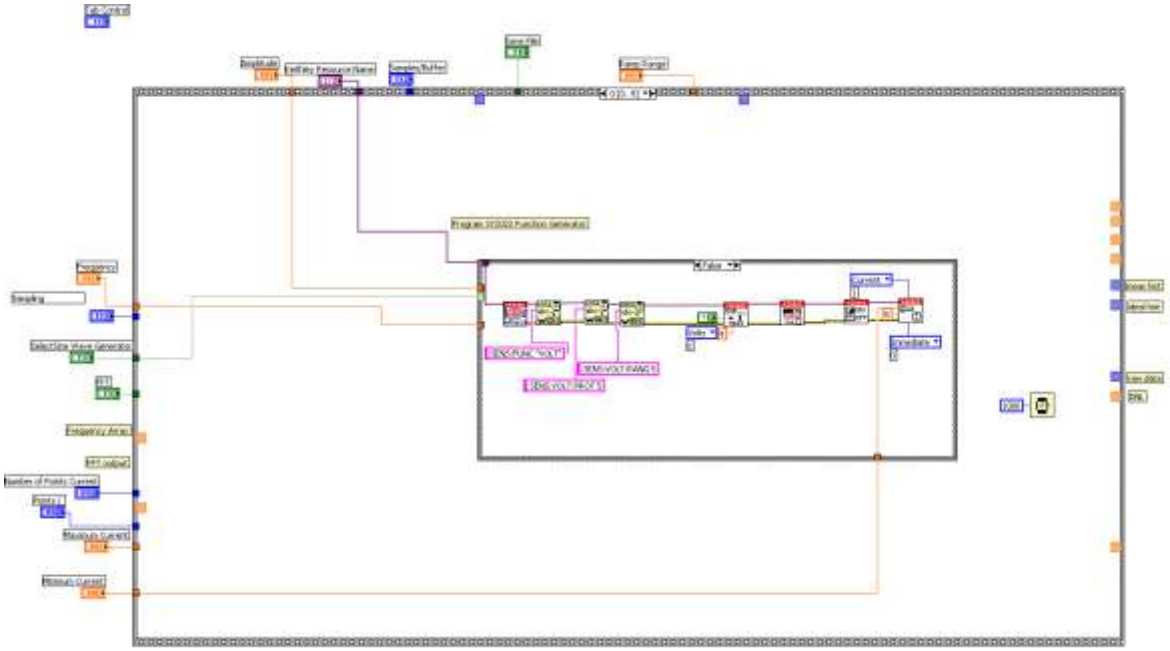

Figure B.2 Programming Keithley Current Source

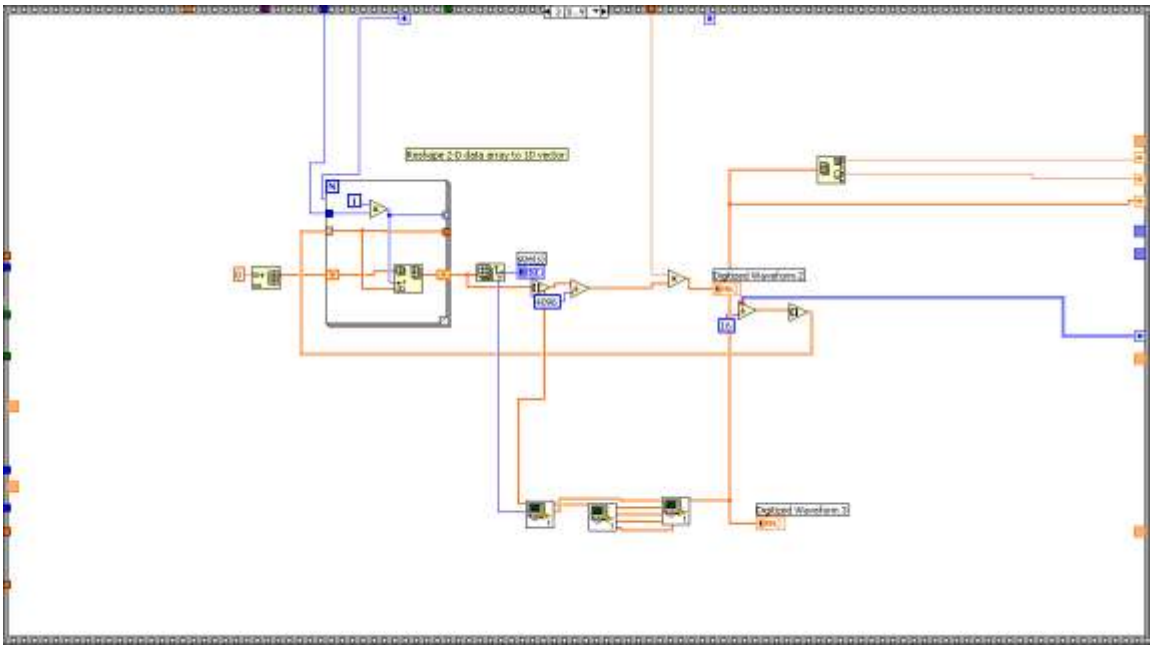

Figure B.3 Processing Acquired Data Arrays

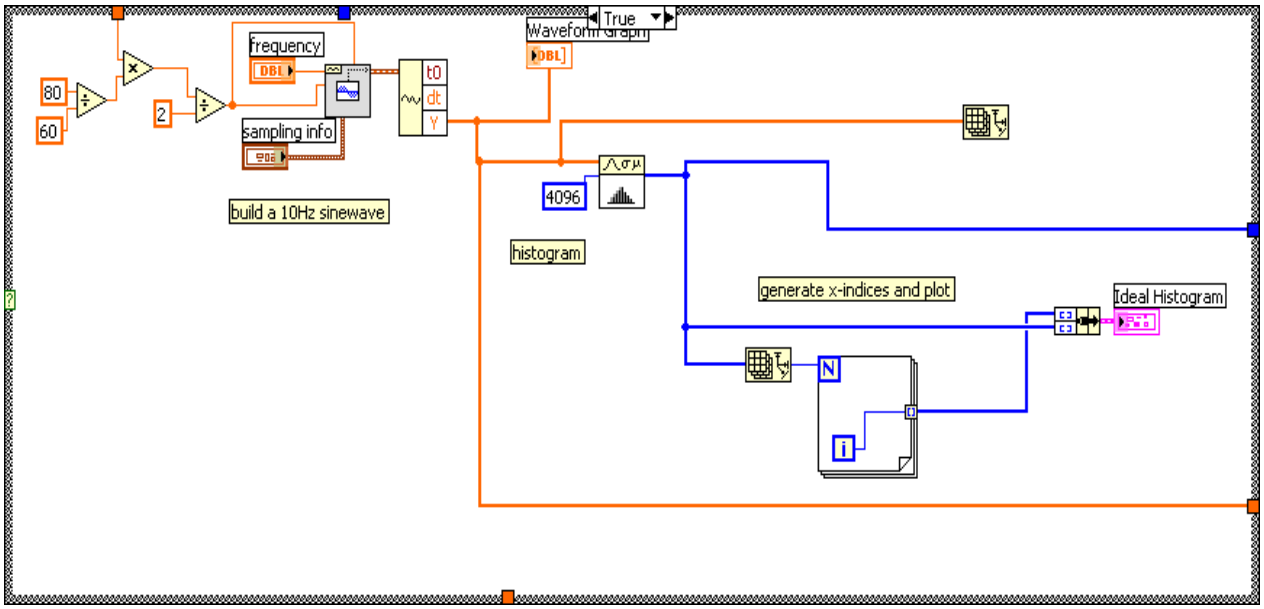

Figure B.4 Generation of Ideal Sine Wave Histogram

In case the current source is used as an input an ideal linear ramp is required to be generated. Figure B.5 shows the block used to generate the ideal ramp. Figure B.6 presents the block used to calculate the DNL using the histogram method. In order to calculate the INL, the best-fit DNL is calculated. Figure B.7 demonstrates the block used to calculate the INL. Both end-point INL and best-fit INL are computed using this block.

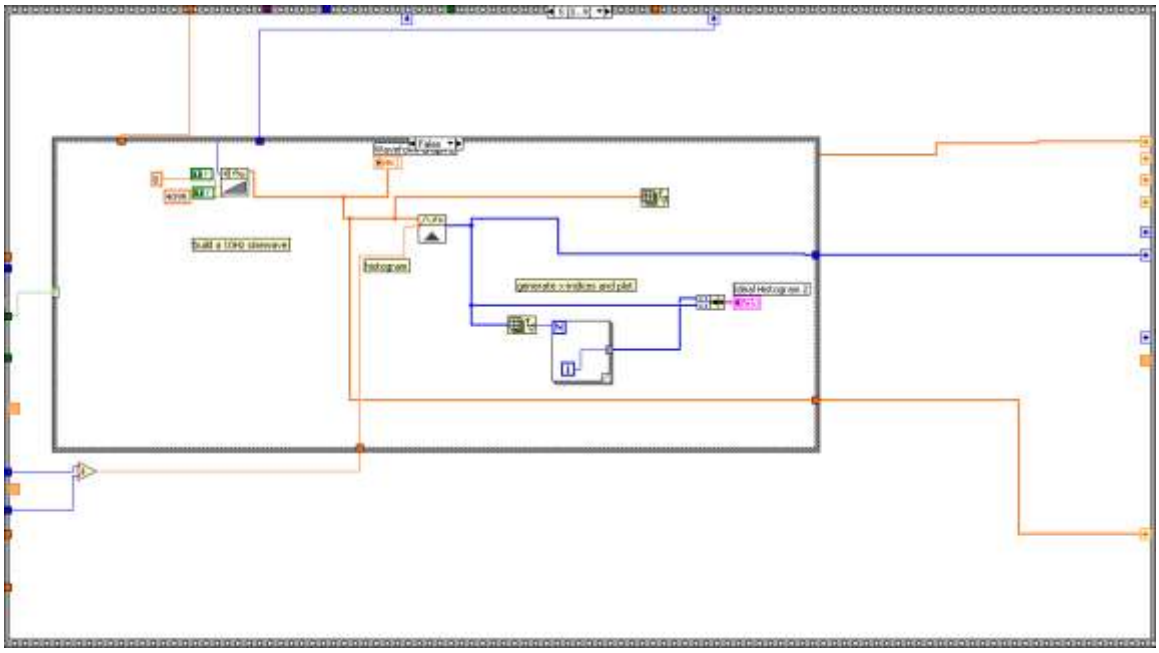

Figure B.5 Generation of Ideal Ramp

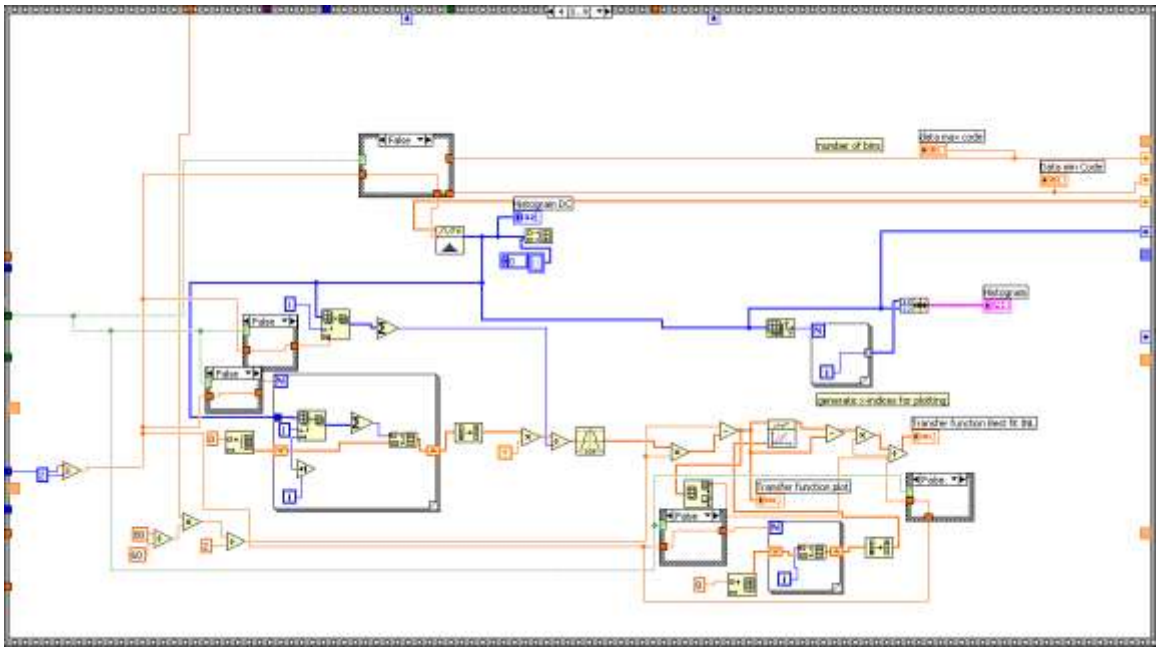

Figure B.6 DNL Computation

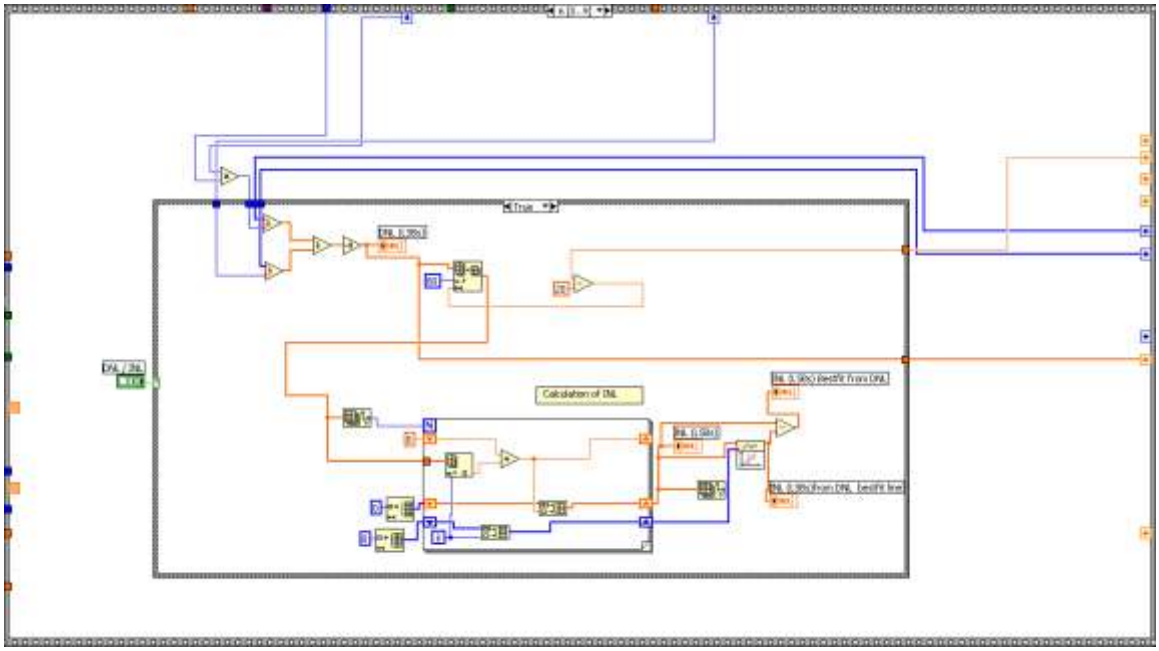

Figure B.7 INL Computation

Figure B.8 depicts the block used for calculation of the FFT. A Nuttall window is used to obtain optimum sidelobe characteristics. Figure B.9 shows calculation of the SNR, SNDR and THD. The DC component of the FFT is first removed. The total power in the signal peak is calculated using 10 points before and after the peak. The total power in the harmonics is calculated in the same way using 10 points before and after the peaks of the harmonics. The power in the noise floor is then calculated by subtracting the signal power and the power in the harmonics from the total power. From these elements then the three parameters SNR, SNDR and THD are computed. Figure B.10 illustrates the subVI used for conversion from binary to decimal. Figure B.11 presents the subVI used in the conversion from binary to decimal.

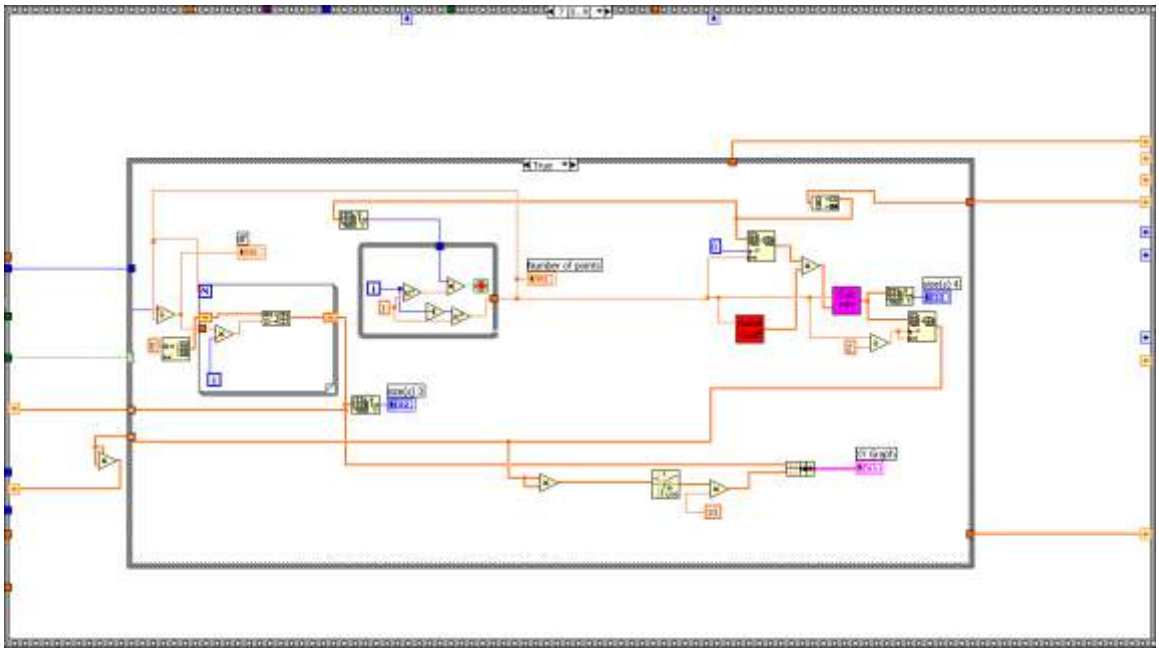

Figure B.8 Calculation of FFT

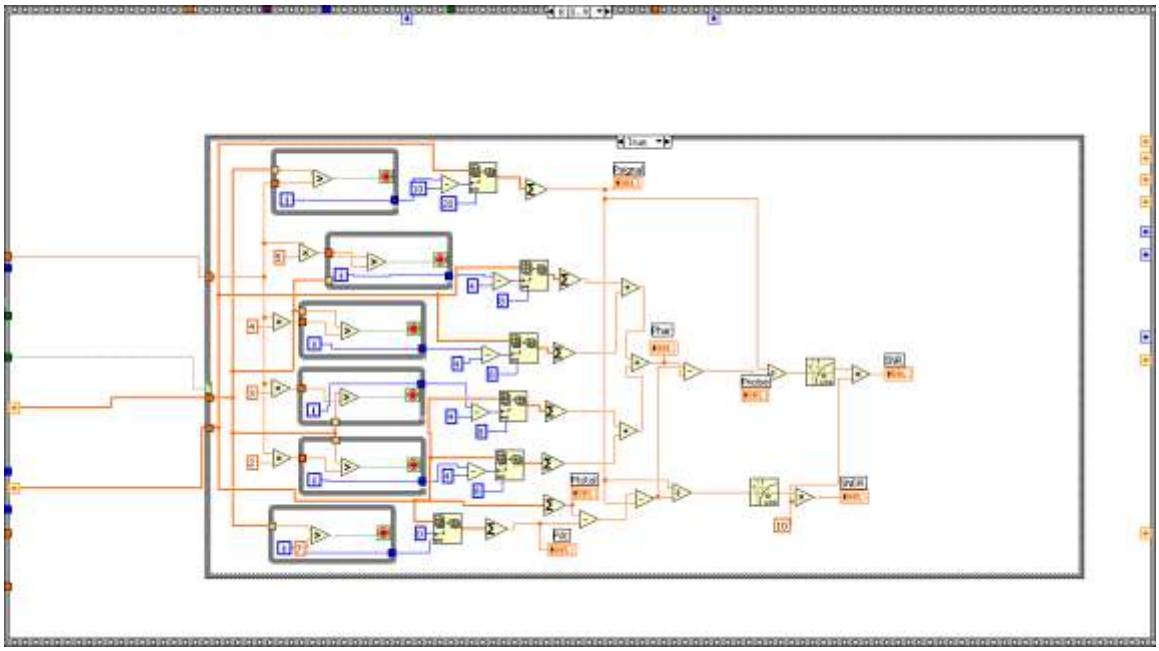

Figure B.9 SNR, SNDR and THD Calculation.

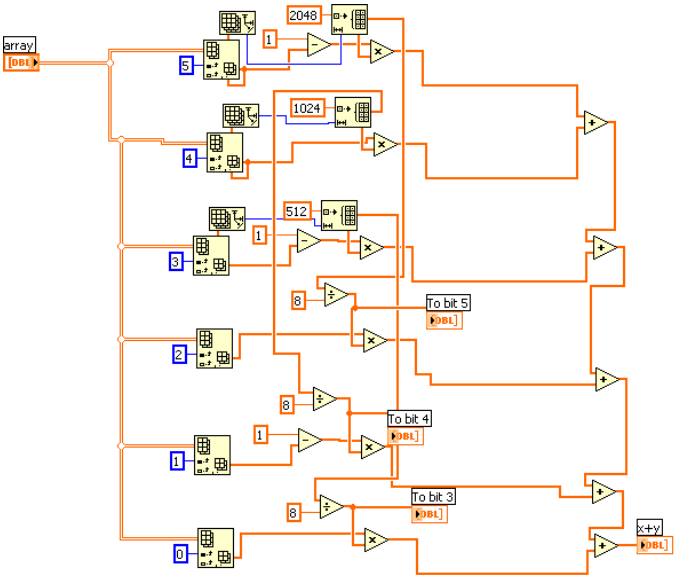

Figure B.10 Conversion of Binary to Decimal.

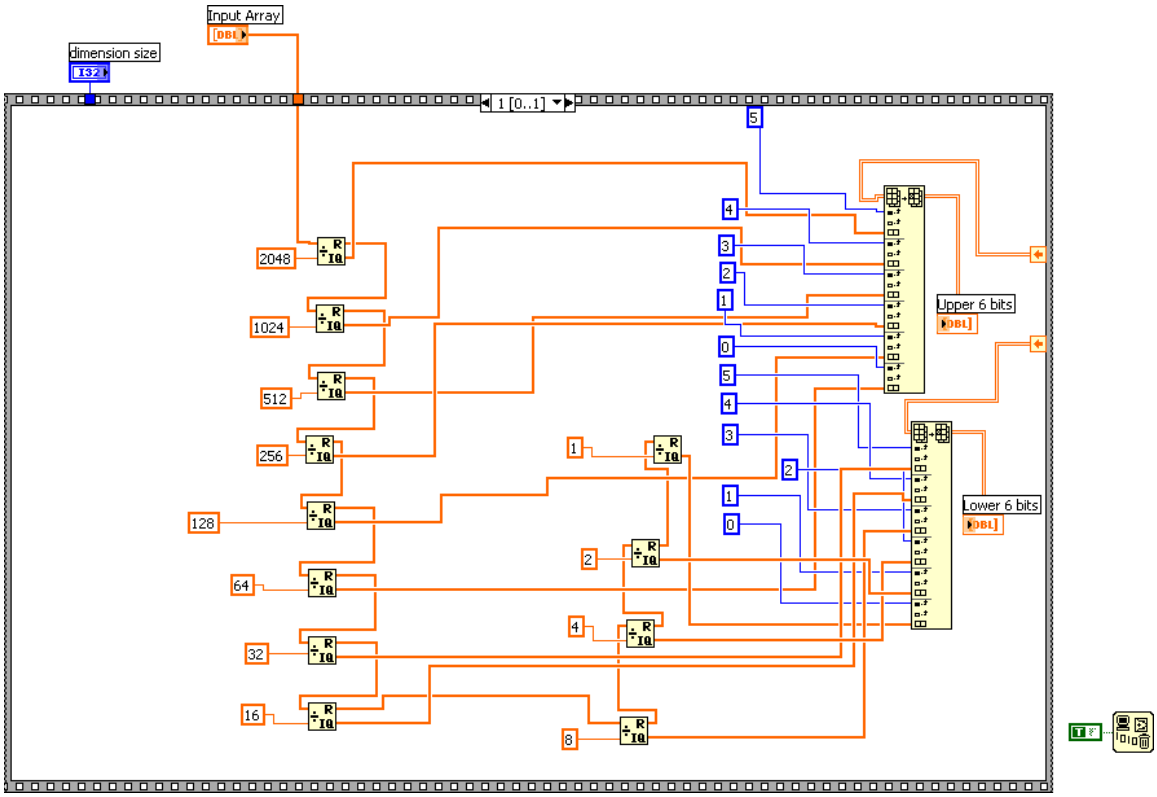

Figure B.11 Conversion of Decimal to Binary.

Vita

Neena Nambiar was born in Pune, Maharashtra, India. She graduated from St. Joseph's High School, Pashan, Pune in 1995 and from Fergusson College in 1997. She obtained a degree of Bachelor of Engineering in Electronics and Telecommunications from Pune University, India in August 2001. She obtained a Master of Science degree in Electrical Engineering from the University of Tennessee, Knoxville in December 2004. She joined the Ph.D. program at the University of Tennessee, Knoxville in August 2004. Her research interests include analog-to-digital converters, low dropout regulators and current-mode design.