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Characteristics of Heteroepitaxial SI-BP Structures Grown at a Single Growth Temperature

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July 31, 1987

To the Graduate School:

Herewith is submitted a dissertation written by Perry J. Robertson entitled "Characteristics of Heteroepitaxial Si-BP Structures Grown at a Single Growth Temperature." I recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

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Dissertation Advisor

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CHARACTERISTICS OF HETEROEPITAXIAL SI-BP STRUCTURES GROWN AT A SINGLE GROWTH TEMPERATURE

A Dissertation

Presented to

the Graduate School of

Clemson University

In Partial Fulfillment

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Doctor of Philosphy

Electrical Engineering

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by

Perry J. Robertson

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ABSTRACT

In this dissertation, MOS device quality silicon was grown on boron phosphide layers using a newly developed, single temperature process. Electron channeling patterns, used to investigate crystal quality, indicated high quality crystal growth for both silicon and BP layers. Changes induced in the BP layer following heating were also examined. It was shown that high resistivity ($\approx 10^6$ Ω-cm) BP can be grown on silicon without heat treatments using single temperature growth conditions.

MOS devices were fabricated on 1 to 5 μm n-type silicon layers grown on 0.2 and 0.4 μm BP layers to electrically characterize the epitaxial silicon layers. It was impossible to fabricate properly operating MOS transistors on silicon layers thinner than 2.0 μm due to high leakage currents between the source and drain contacts which shorted the device. On the 1.0 and 2.0 μm layers, the background concentrations were on the order of 10^{20} cm^{-3} while the doping concentration fell to a minimum of $5x10^{15}$ cm^{-3} for silicon layers thicker than 5 μm. Transistor characteristics on 5 μm silicon layers were comparable to those fabricated on bulk silicon. Effective field effect mobilities in the linear region of transistor operation on the 5 μm silicon layers were as high as 245 $cm^2/V\text{-}s$ with subthreshold currents as low as 10^{-11} amperes and subthreshold slopes of 95 mV/dec. The mobility in the

saturation region was 150 $cm^2/V\text{-}s$. From the results, it was concluded that the saturation mobility was limited by scattering at the silicon-oxide interface under the gate. Threshold voltages on 1, 2 and 3 μm silicon layers could not be measured due to high subthreshold currents. The average threshold voltage measured on 4 and 5 μm silicon layers was -2.0 V. The average measured threshold voltage value was within 6.5% of the theoretical value.

It was shown that good devices can be fabricated on Si-BP structures grown at a single temperature if the top silicon layer was at least 5 μm thick and the reactor tube was cleaned following BP growth and prior to silicon growth.

ACKNOWLEDGMENTS

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CHAPTER I

INTRODUCTION

It has been previously shown that multiple silicon-boron phosphide-silicon (Si-BP-Si) films can be grown on (100) silicon substrates [1] [2]. This material combination, with up to five layers of Si-BP-Si on silicon substrates and two layers on SOS substrates, has been used as a substrate for PMOS integrated circuits [3]. These circuits had properties similar to circuits fabricated on SOS material.

Several problems were associated with the growth of Si-BP films and the use of BP in a silicon integrated circuit process. Attempts to solve these problems were met with varied levels of success. The need for multiple growth temperatures for the silicon and BP layers was eliminated by the development of a single temperature growth process. Autodoping of the silicon layers continued to be a problem making it necessary to clean the reactor tube following BP growth and prior to silicon growth. It was necessary to grow silicon layers thicker than 5 μm in order to reduce the autodoping from an underlying BP layer to a level appropriate for MOS devices.

A process has been developed for growing both silicon and BP layers at single growth temperature. A single growth temperature was desirable because it eliminated the long waiting periods between epitaxial growths necessary to

stabilize the susceptor at the new growth temperature. Using this process, lightly doped silicon films suitable for MOS devices were grown on BP films.

It was determined that boron phosphide was not the ideal material for SOI applications due to the possibility of autodoping of the silicon by either boron and/or phosphorus during growth of the films and subsequent integrated circuit processing. The silicon layer had a graded doping profile with a doping concentration that decreased as the silicon thickness increased.

The characteristics of devices on Si-BP-Si layers were examined as a function of silicon epitaxial layer thickness using the MOS device characteristics in order to determine the feasiblilty of using the silicon layers as substrate material. PMOS devices were fabricated on 1.0 or 2.0 μm silicon layers but did not operate properly due to high leakage currents and high background doping concentrations. It has been shown that MOS devices fabricated on the 5.0 μm silicon layers had characteristics similar to devices fabricated on bulk silicon made during the same process run. Thus the single temperature Si-BP-Si structure has been shown to have characteristics that make it useful as an MOS substrate material when the top silicon layer is thicker than 5.0 μm.

CHAPTER II

HISTORICAL DEVELOPMENTS IN HETEROEPITAXIAL SI-BP-SI TECHNOLOGY

The preparation of boron monophosphide (BP) was first reported by Besson [4] and Moissan [5] in 1891. Besson prepared BP by the combination of BBr_3 and PH_3 resulting in a solid brown material. Moissan reported that BP could be prepared by the reduction of PBI in hydrogen. Work on boron phosphide lay apparently dormant until 1952 when Welker [6] reported that BP had interesting semiconductor properties.

In 1956, Welker and Weiss [7] predicted that BP could be crystallized with a cubic zinc blende structure. The next year, Popper and Ingles [8] reported the preparation of BP with a zinc blende structure by the reaction of boron and red phosphorus in an evacuated, sealed silica tube at 1100°C. The lattice constant of the cubic, zinc blende BP was found to be 4.538 Å [9].

During the early sixties, several researchers began investigating BP. The decomposition of BP into B_6P_2 at high temperature was reported by Williams in 1959 [10]. Cubic BP was reported to have a very large band gap of 6 eV by Stone and Hill in 1960 [11]. Stone was later awarded a patent for his process of preparation of BP (1961) [12]. The preparation of $B_{13}P_2$ reported by Matkovich in 1961 [13] involved the reaction of aluminum phosphide and amorphous boron powder.

The resulting material was a fine powder with a rhombohedral unit cell with a = 5.984 Å and c = 11.850 Å. In 1962, Sclar's empirical formula for the band gap of III-V compounds was applied to BP with a resulting value of 6.2 eV [14]. A smaller band gap of 4.5 eV was reported by Samsonov and Tithov in 1963 [15]. Archer (1964) measured the optical properties of cubic BP and used the results to determine that the band gap structure is indirect with a band gap of 2.0 eV [16] which is now the accepted value.

The first general review of the properties of boron monophosphide appeared in 1964 [17]. A second more general review of boron-phosphorus compounds was published in 1975 [18].

Work on boron phosphide as a semiconductor compound increased when, in 1972, Nishinaga, et al. [19], reported the first successful epitaxial growth of BP on (100) and (111) silicon substrates by the pyrolytic decomposition of BBr_3 and PCl_3 in hydrogen from 900-1100°C.

Research into the growth of heteroepitaxial BP continued in 1973 when Takigawa, et al. [20], described the growth of $B_{13}P_2$ on (100) and (111) silicon substrates by the pyrolytic decomposition of diborane (B_2H_6) and phosphine (PH_3) diluted in hydrogen. The layers were grown in a water cooled, horizontal, rf heated, quartz epitaxial reactor. The crystallographic orientation of BP on silicon was found to be $B_{13}P_2(11\bar{2}0)//Si(100)$, $B_{13}P_2(11\bar{2}0)//Si(110)$ and $B_{13}P_2(10\bar{1}0)//Si(111)$. It was also reported that boron phosphide was a

transparent film with a resistivity greater than 10^8 Ω-cm at room temperature. They suggested that BP would be an insulator on silicon substrates.

In 1974, Takigawa, et al. [21], reported on the effects of the variation of growth parameters on the quality of the single crystal BP layer. Over the temperature range from 950-1050°C, BP layers were found to have a cubic orientation. Both n-type and p-type BP layers were produced at growth rates from 100-700 Å/min. Hall mobilities of BP films over the carrier concentration range from 10^8-10^{20} cm^{-3} varied from 150-80 cm^2/V-s, similar to bulk silicon. Takenaka and Shohno [22] showed that silicon could be grown on $B_{13}P_2$ using silane (SiH_4) in hydrogen. Multiple layers were grown. The $B_{13}P_2$ layers were found to be rhombohedral with a = 5.984 Å and c = 11.850 Å. The silicon layers grown at 950°C were n-type, (100) orientation, with a carrier concentration of $3.6x10^{15}$ cm^{-3} and were p-type with a carrier concentration above 10^{20} cm^{-3} when grown above 1020°C. Hall mobilities on the n-type silicon layers were reported as high as 480 cm^2/V-s.

Shohno, et al. [23], reported that boron monophosphide could be grown by varying the growth parameters in the PH_3/B_2H_6 system. The crystallographic orientation of the BP was the same as that of the silicon substrate. The best n-type BP layers had mobilities near 140 cm^2/V-s with a carrier concentration of $4x10^{18}$ cm^{-3}.

Between 1975 and 1978, several authors reported on the development of epitaxial boron monophosphide on silicon

process and its electrical properties. Epitaxial BP layers as thick as 30 μm were grown [24]. It was shown that BP could be selectively removed by masking and applying a 30-50 volt, one second dc pulse to the substrate while submerged in 4N aqueous sodium hydroxide [25]. The dielectric constant of BP was reported as 11 while the index of refraction was 3.1 [26]. Three types of imperfections were found in the early growth stages of the BP layer: {111} twinnings, {211} twinnings and {111} planar defects [27]. The optimum substrate orientation for minimizing imperfections was 2° off oriented (100) silicon face in the direction of a (110) plane. BP grown thicker than 400 Å had a high level of crystalline perfection. A wide gap window solar cell, wide gap emitter transistor and diode structures were proposed using the BP-pSi-nSi structure [28].

The diffusion layer formed beneath the BP layer in the silicon substrate during BP growth was examined by Takenaka, et al., in 1978 [29]. The concentration of boron and phosphorus in the diffusion layer was controlled by the flow rate of PH_3 during BP growth. The diffusion source was present only very early in the growth of the BP layer. The BP layer protected the silicon surface from the gaseous diffusion source and did not act as a diffusion source itself.

Multiple layers of Si-BP-Si were first reported in 1980 by Nonaka, et al. [2]. They succeeded in growing 10 layers (five BP and five silicon) by employing BP layers less than

1000 Å thick and carrying out the growth of both layers in the same epitaxial reactor. The BP layers were grown at 950°C using a B_2H_6-PH_3-H_2 system. The temperature was raised to 1050°C and silicon was grown on the BP using SiH_4-H_2. Heterojunctions were created between n-BP and n-Si or p-Si layers with carrier concentrations in the BP less than 10^{18} cm^{-3} and electron mobilities of around 50 cm^2/V-s. The BP layers had a zincblende structure with a lattice constant $a = 4.53$ Å.

A BP (100)-c(2x2) surface structure was reported by Shono and Kim in 1982 [30] for BP layers from 400-6000 Å. The silicon layer was found to have a high degree of crystallinity in electron diffraction patterns and indicated by hole mobilities as high as 230 cm^2/V-s in PMOS transistors fabricated on the silicon layer with a carrier concentration of $2x10^{16}$ cm^{-3} [31]. The characteristics of other devices such as a unique Si-BP-Si double heterojunction have been examined [32]. A more detailed crystallographic examination of the Si-BP-Si heteroepitaxy was presented by Amano, et al. [33].

Kim and Shono [34] proposed that the Si-BP structure could be used to develop a three dimensional technology which takes advantage of silicon layers isolated by a wide band gap, high resistivity BP layer. The resistivity of the BP layer was controlled by heat treatments. A BP layer with an initial resistivity of 0.01 Ω-cm which was subsequently covered by 500 Å of Si_3N_4 had its resistivity increased to

over 10^{11} Ω-cm after heating at a temperature, T = 1050°C for two hours. Stoichiometric BP layers heated at T < 1050°C became n-BP while layers heated at T > 1050°C became p-BP.

The silicon quality for multiple Si-BP-Si layers was studied by Sugiura, et al. [3] in 1985. They reported the characteristics of MOS devices manufactured on the top silicon layer of one to four Si-PB-Si layered wafers. Silicon of reasonably high quality was found even on the fourth layer. PMOS transistors were found to have mobilities as high as 180 $cm^2/V-s$. Subthreshold slopes on the first layer were comparable to bulk silicon values but degraded by the fourth layer. Threshold voltages were slightly higher than bulk values due to autodoping from the BP layer.

A summary of the activities in heteroepitaxial Si on BP by Shono Laboratory, Sophia University, Tokyo, Japan, was published in 1985 [35].

Since previous results were reported for silicon and BP layers grown at different temperatures, a single temperature growth process was developed and wafers were processed to determine if the film quality would be sufficiently high for MOS device fabrication. It was proposed that the crystalline quality of the film would improve as the film became thicker, similar to SOS devices, and would have lower doping concentrations due to the increased distance between the film surface and the underlying BP film.

High quality lightly doped silicon films were grown on BP by cleaning the reactor prior to silicon growth. A single

temperature process was developed and used to grow layers of silicon 1 to 5 μm thick on 0.2 and 0.4 μm BP films grown on (100) silicon substrates. MOS devices fabricated on the 5 μm films were found to have characteristics comparable to those of devices fabricated on bulk silicon wafers processed at the same time. No differences were found between the crystal quality of silicon films grown on 0.2 and 0.4 μm BP wafers.

CHAPTER III

REACTOR DESIGN AND CONSTRUCTION

An epitaxial reactor was designed and built to grow the Si-BP structures. The reactor consisted of the gas cabinet, reactor chamber, the gas flow system, the temperature monitor system, and the exhaust system. The wafers were heated by reactive coupling of a graphite susceptor to an rf generator operating at 10 kHz. A gas cabinet was designed and constructed to house all of the reactor plumbing except the exhaust system. The various parts of the epitaxial reactor will be described in detail.

Gas Cabinet

The epitaxial reactor was constructed with the aim of growing various heteroepitaxial insulator/conductor structures. The reactor consisted of a gas cabinet which contained the epitaxial gases (B_2H_6-H_2, SiH_4-H_2, PH_3-H_2, C_2H_6-H_2, HCl, H_2O-H_2), regulators, flow meters, valves and plumbing, water-cooled quartz chamber, rf coil and infrared pyrometer. Purified hydrogen and nitrogen were supplied externally to the gas cabinet. Hydrogen was purified by passing it through a palladium diffusion cell. Nitrogen was passed through a catalytic gas dryer before entering the cabinet. A schematic diagram of the gas cabinet has been shown in Figure 1.

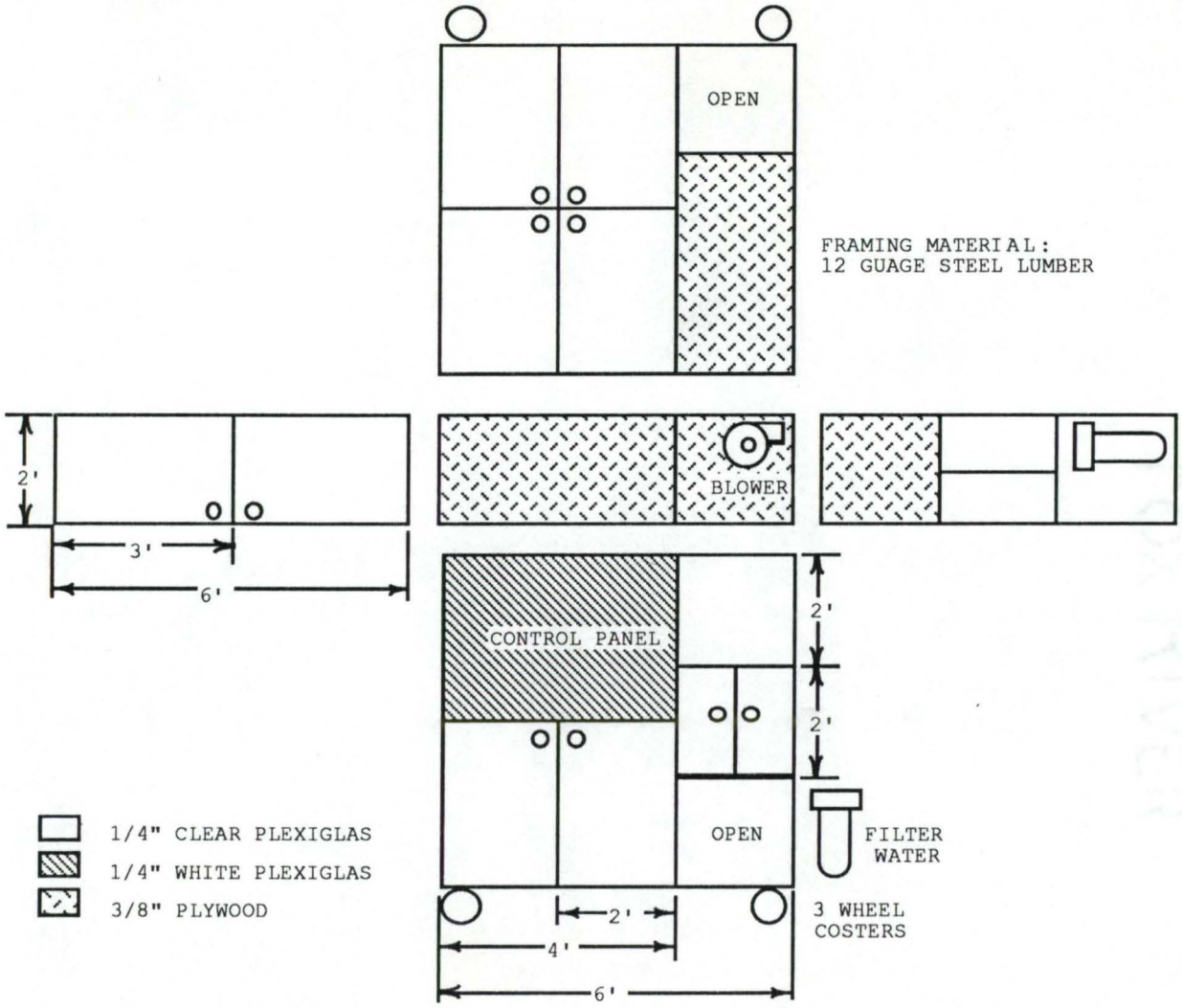


Figure 1. Diagram of the Gas Cabinet. The frame of the cabinet was constructed of steel shelving materials.

Reactor Chamber

Individual gas bottles were located on the left side of the cabinet behind the control panel. Each gas had a regulator which controlled the delivery pressure to individual flow meters mounted on the panel. Each regulator was equipped with a purge line which allowed for the flushing of each regulator and flow meter with nitrogen prior to and following a run.

The water-cooled vertical quartz chamber was mounted in the right side of the gas cabinet. Gas was provided from the mixing chamber into the side of the top of the quartz tube. Hot exhaust gases were removed from the cap at the bottom of the quartz chamber. The rf coil consisted of 7 turns of 1/4 inch copper tubing surrounding the outside of the water jacket on the quartz tube and located outside the susceptor.

It was decided to use a vertical chamber with the wafer mounted perpendicular to the flow of the gas. Initially an air cooled single walled reactor was used. However, excessive gas phase decomposition of the reactor gases, contamination of the reactor walls, and the slow cycle time of the air cooled reactor indicated that a double walled, water cooled reactor would be preferable. Early runs of BP were plagued by the leaking of phosphine into the lab from the joint which connected the exhaust line and quartz cap. This problem led to the placement of a plastic shroud over the joint and a blower which would suck the unwanted exhaust out of the lab. It was concluded that the leaking was coming from a bad weld

in the 1/2 inch flexible stainless steel tubing used in the exhaust line. A combination of Swagelok and Ultratorr fittings finally provided a leak-tight, quick disconnect joint which allowed for the easy removal of the cap and pedestal from the tube. The final configuration of water cooled quartz reactor with quick disconnect fittings proved to be a good design for all types of epitaxial work. A sketch of the final quartz reactor design has been shown in Figure 2.

The vertical water cooled fused quartz chamber had an inside diameter of three inches and is capable of handling up to two inch diameter wafers. The reactor chamber consisted of two parts, the vertical tube and wafer pedestal and cap. The vertical chamber was 20 inches in length with a 12 inch long water jacket. A clear, polished, fused quartz window was installed in the top of the tube to allow direct temperature measurement of the surface of the wafer via an infrared pyrometer. The susceptor and wafer were supported on a pedestal which was attached to the center of the base of the cap. Quartz hooks were fabricated onto the tube and cap so that the cap may be held onto the tube by two lightweight springs. A ground glass joint was provided to join the cap and tube opening. Silicon vacuum grease was applied to the ground glass joint to eliminate back diffusion of oxygen into the chamber and ease the removal of the cap.

Susceptors

Several different silicon carbide coated graphite susceptors were used in this project. They were all 2-1/4

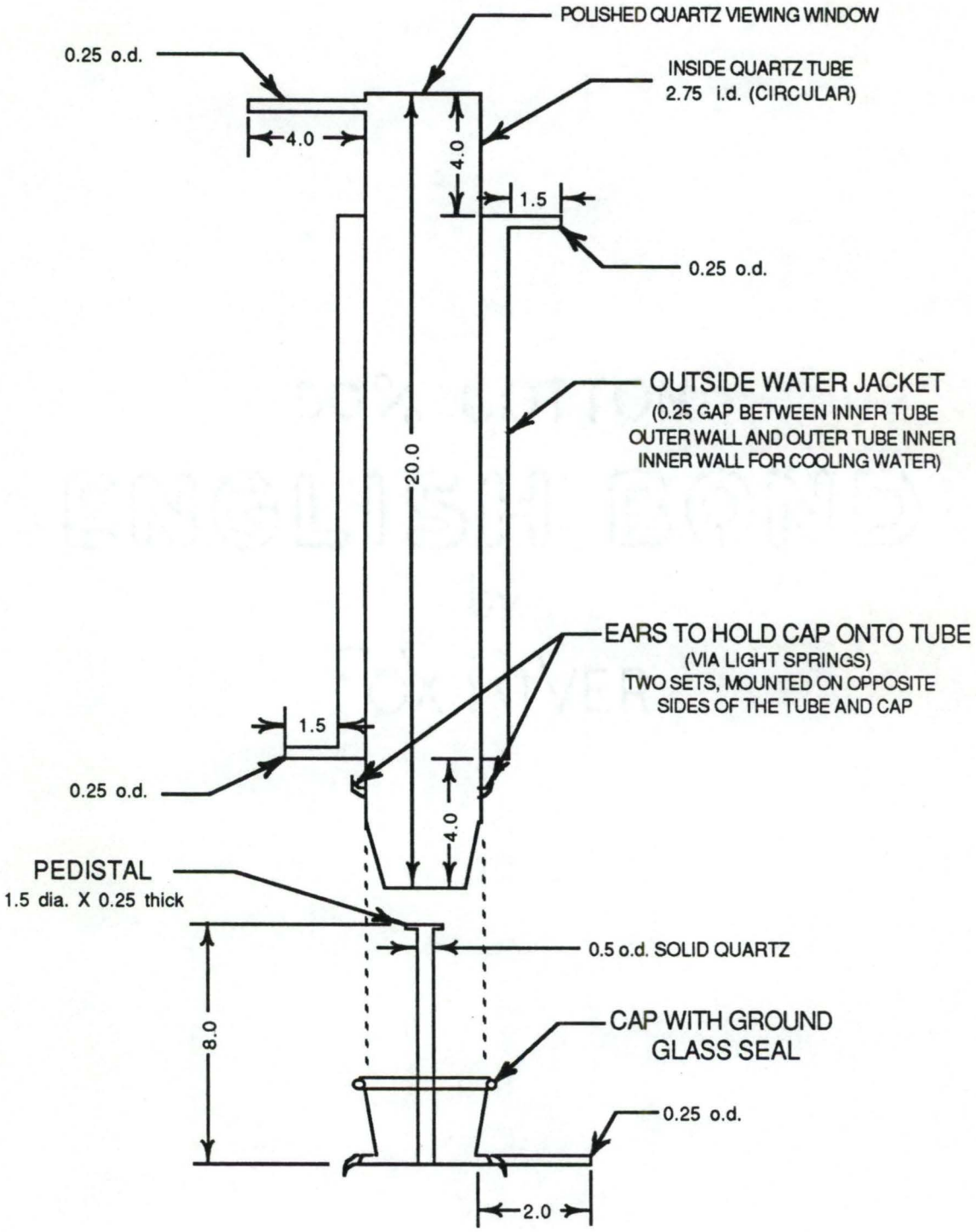


Figure 2. Quartz Epitaxial Reactor Tube. The susceptor is positioned horizontally in the center of the chamber by a fused quartz pedestal. All dimensions are in inches.

inches outside diameter with thicknesses varying from 1/4 to 1 inch as shown in Figure 3. Separate susceptors were used for growing BP and silicon-on-BP in order to reduce cross-contamination between processes. A shallow depression was machined into the top of the susceptor to keep the wafer from sliding off the susceptor during processing. A slightly deeper and smaller diameter depression was cut into the bottom of the susceptor to center the susceptor on the quartz pedestal. The diameter of this depression was large enough to prevent binding during heating due to differences in coefficients of expansion of graphite and fused quartz and to allow leeway for the centering of the susceptor when the pedestal was not mounted exactly in the center of the tube. This was important because a susceptor that was placed too close to one side of the reactor would not heat uniformly and would cause boiling of water inside the cooling water jacket.

Initially, a poly-silicon wafer holder was set on the SiC susceptor. This combination susceptor had trouble attaining temperatures above 1200°C due to the thermal gradient which existed between the two susceptor pieces and the lack of coupling of the silicon to the rf source. The thermal gradient was from 100°C to 200°C depending upon flow rates and power setting of the rf generator. In order to attain temperatures above 1200°C, graphite susceptor temperatures approached 1400°C. At one point, the poly-silicon susceptor on top of the graphite susceptor began to melt. The use of the poly-silicon susceptor was abandoned after this incident.

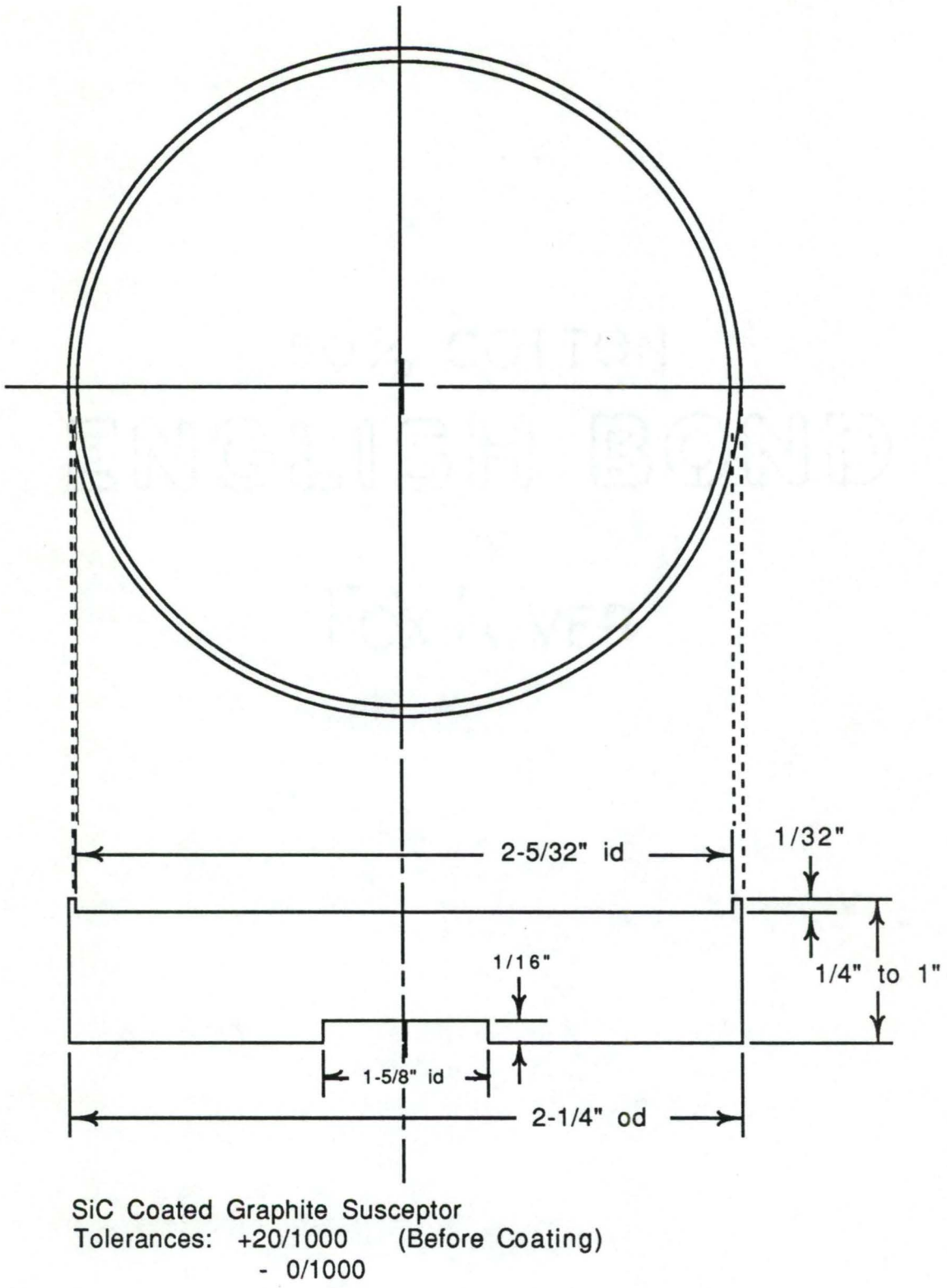


Figure 3. Silicon Carbide Coated Graphite Susceptor Design.

Gas Flow System

A schematic sketch of the reactor gas flow system has been shown in Figure 4. The hydrogen was purified by passage through a palladium diffusion cell. The nitrogen was purified by passage through a catalytic reactor. There were provisions for six reactor gases in the gas cabinet. The flow rates of all gases were measured by rotameters. The needle valves on the rotameters were located at the outlets so that the gas flow rates would be independent of down stream pressure changes, provided that the inlet pressures remained constant at 15 psig. Filters at appropriate places in the gas lines keep contaminants such as silicon dioxide in the silane from entering the reactor chamber. After construction of the reactor gas system, the system was checked for leaks by pressurizing the system and measuring the pressure change over a 24 hour period. The system was considered leak-tight when the pressure dropped less than 5 psi from the initial 50 psi setting in 24 hours.

Temperature Monitoring System

The temperature of the wafer was monitored in two ways. An optical pyrometer was used as the primary temperature reference. The pyrometer was sighted between the rf coils through the water jacket at about a 30 degree angle from the vertical. An optical window was provided in the top of the reactor for an infrared pyrometer to monitor the wafer surface infrared emission. The infrared pyrometer was not calibrated and was used primarily to determine the in situ growth

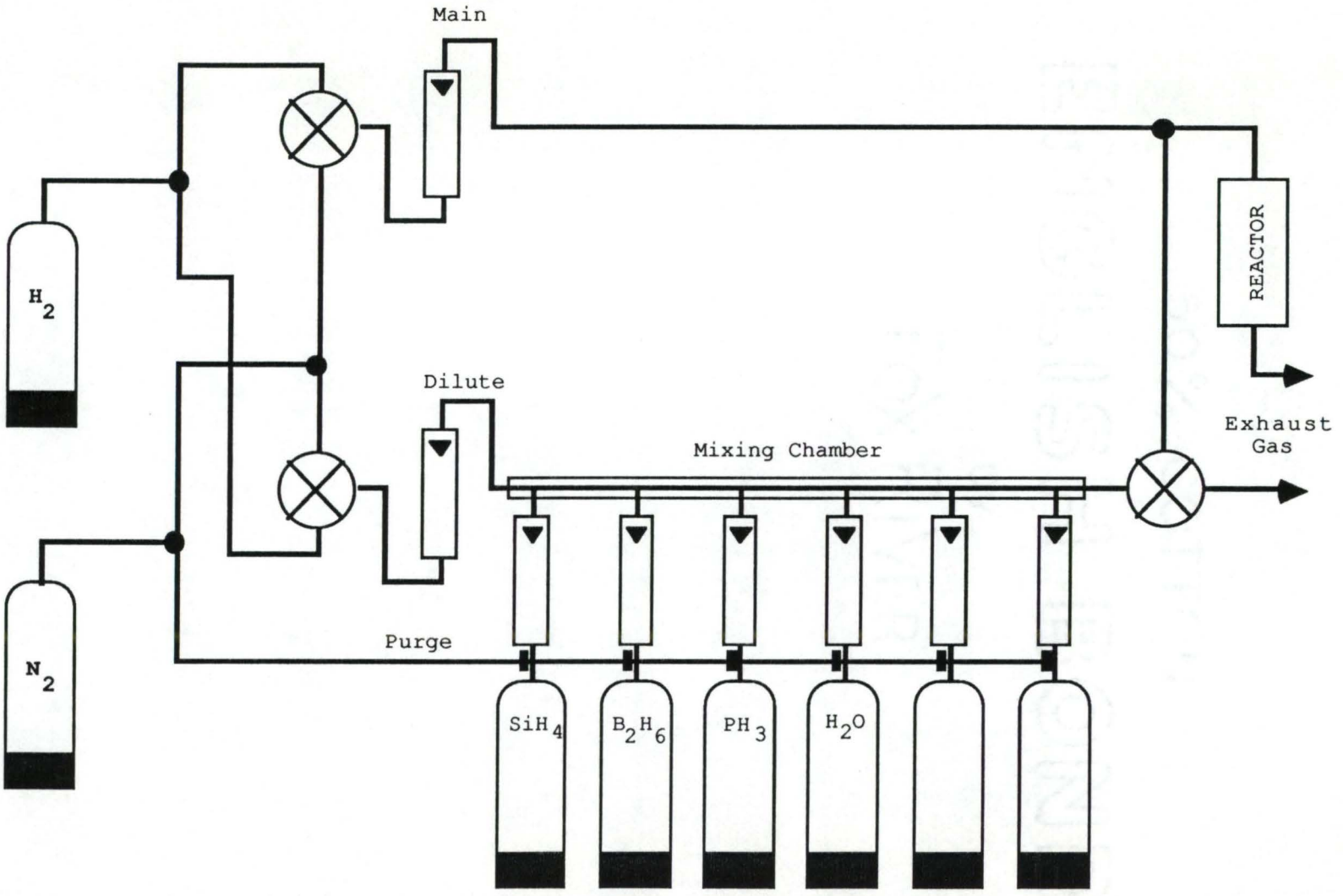


Figure 4. Schematic of Reactor Gas Flow System.

rates. The emissivity setting on the ir pyrometer remained at .99 throughout the experiments. A schematic diagram of the infrared pyrometer has been shown in Figure 5.

The film thickness was monitored, in situ, using a technique first described by Dumin in 1967 [36]. Film thickness was measured using an infrared pyrometer coupled to a chart recorder as shown in Figure 5. Constructive and destructive interference from reflections from the front epitaxial surface varied the intensity of the transmitted radiation depending upon the thickness of the film. The oscillation pattern on the chart recorder damped out as the thickness increased due to absorption by the growing layer.

Exhaust System

The reactor gas exhaust system consisted of three parallel lines running to the outside of the building to a double walled burn chamber. The gas from the reactor was mixed with the bypass gas line and the bleed line from the hydrogen purifier in the burn chamber. A resistive heated wire provided enough heat to ignite the hydrogen mixtures.

Gas mixtures which passed through the reactor chamber were exhausted via a 1/4 inch flexible stainless steel tube into a 1/2 inch copper tube and onto the exhaust burner. The outside fixture was an 18 inch long, 4 inch diameter steel pipe. The pipe was mounted outside a window near the gas cabinet. The exhaust lines terminate at the center of the pipe. The small wire heating coil was mounted at the opening of the exhaust pipes. When the coil was attached to a

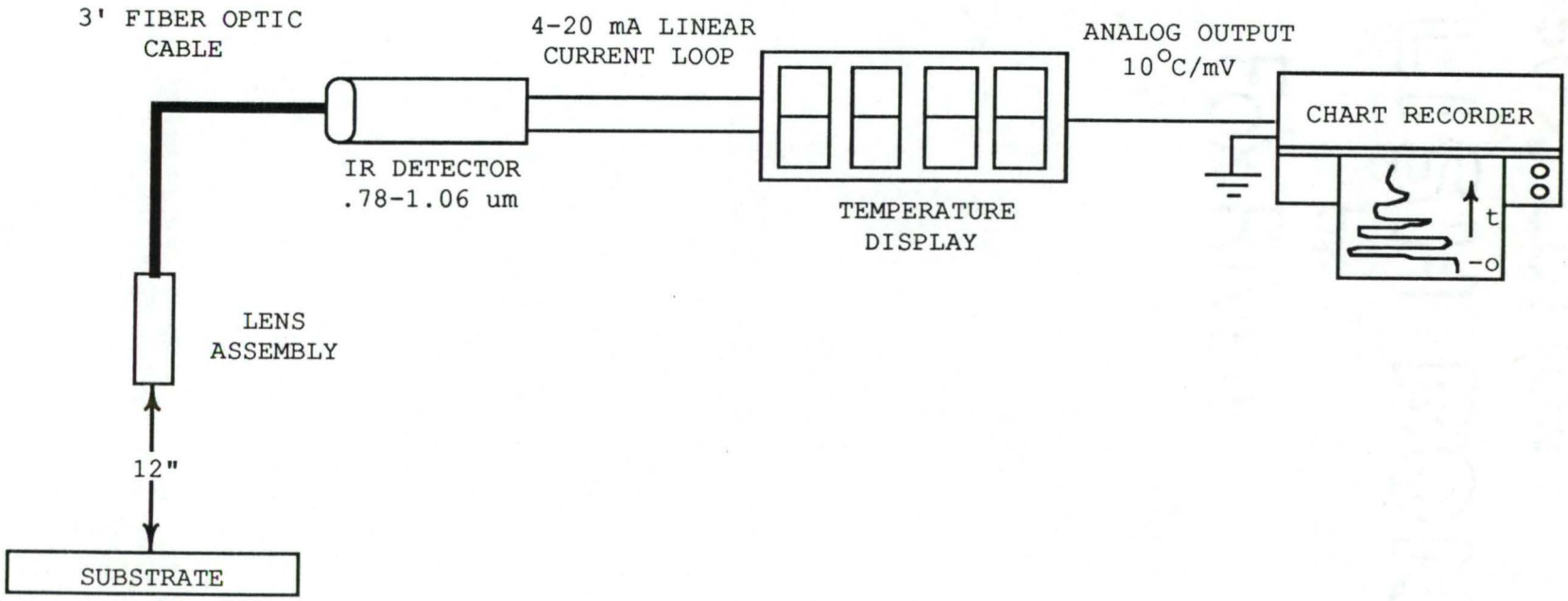


Figure 5. Schematic Diagram of the IR Pyrometer. The peak detectivity of the ir detector was found to be 0.9 μm.

rheostat, set to approximately 16% of the 110 volt input, it would glow red. The wire temperature was then hot enough to ignite the hydrogen. Once ignited, the power was turned off. The constant flow of hydrogen kept the exhaust gases burning.

CHAPTER IV

GROWTH OF THE FILMS

Silicon and boron phosphide films were grown using the epitaxial reactor described in CHAPTER III. The substrates used in this experiment were (100) p-type 6-10 Ω-cm two inch silicon wafers. An explanation of the cleaning, processing and inspection of these wafers follows.

Wafer Cleaning

Silicon wafers were cleaned using a modified RCA etch consisting of:

1. cotton swab with detergent;
2. distilled water rinse;
3. hydrogen peroxide/sulfuric acid, 1:1;
4. distilled water rinse;
5. water/hydrofluoric acid, 7:1;
6. distilled water rinse;
7. blow dry with nitrogen.

The wafers were cleaned immediately prior to their use to minimize contamination and oxide growth on the silicon. No problems with wafer contamination were observed if care was taken during the cleaning operation.

Epitaxial Growth Sequence

After the wafers were cleaned one was loaded into the reactor chamber. During the loading process, nitrogen

continuously flowed through the reactor chamber and hydrogen continuously flowed through the mixing chamber and was exhausted to the burner. The cap was secured and nitrogen was allowed to purge the reactor tube. After five minutes of flushing the reactor chamber with a high flow of nitrogen, hydrogen was switched into the chamber. After one minute, rf power was applied to the rf coil. It usually took about five minutes to bring the wafer up to the desired growth temperature.

While the susceptor and wafer were being brought up to temperature, the mixing chamber was continuously purged with hydrogen and the desired flow rates for the epitaxial gases were established. Once the wafer temperature had stabilized, the reaction gases were switched into the growth chamber and the growth was monitored for the desired time. After film growth, the reaction gases were switched back to the exhaust line. The wafers were held at growth temperature for sufficient time to clear the reactor of the reaction gases, usually 20 seconds. The rf power was then removed.

When the wafers cooled below 900°C nitrogen was switched back into the reactor chamber. The wafer was removed from the reactor when cool. For films in which multiple growths of different materials were required, the same general sequence was followed except for changes in the gas composition and temperature in the mixing chamber.

Single Temperature Growth of Si-BP Films

A single growth temperature process was developed for the growth of silicon and BP films. The growth temperature of 1000°C was chosen as a compromise between the growth of BP at 950°C and silicon at 1050°C in previously published results [2]. The use of a single growth temperature eliminated much of the time spent readjusting the rf power setting to achieve the required growth temperatures for the silicon and BP layers. The result was a faster turn around time for each epitaxial growth sequence. The gas flow rates were chosen experimentally to give the best film quality with the highest growth rate. Boron phosphide was grown at 0.1 μm/min using 1% B_2H_6-H_2 and 5% PH_3-H_2 at 150 and 4200 cm^3/min. Silicon was grown at 2.0 μm/min using 5% SiH_4-H_2 at 1000 cm^3/min. The dilute and main hydrogen lines were set at 500 and 9000 cm^3/min for both BP and silicon epitaxial growths.

Film Inspection

The general condition of the film was noted after film growth. The film resistivity and type was measured using a four point probe. Some samples were angle lapped at one degree to verify film thickness. Some films were taken to the Jeol-848 SEM for electron backscattering measurements to determine crystallinity of the films.

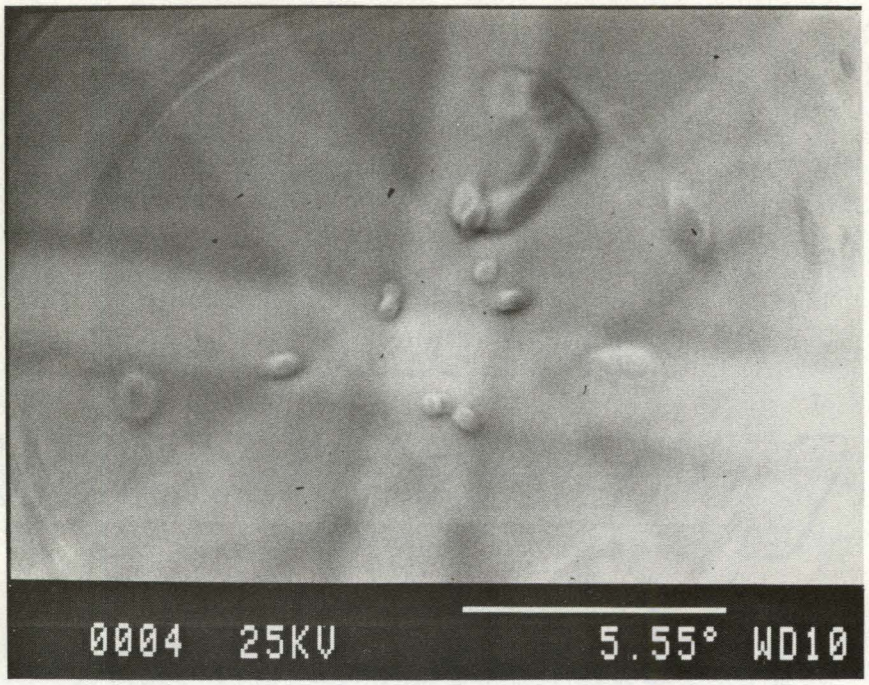
CHAPTER V

EXAMINATION OF SILICON FILM QUALITY ON BP VERSUS BP FILM THICKNESS USING ELECTRON CHANNELING PATTERNS

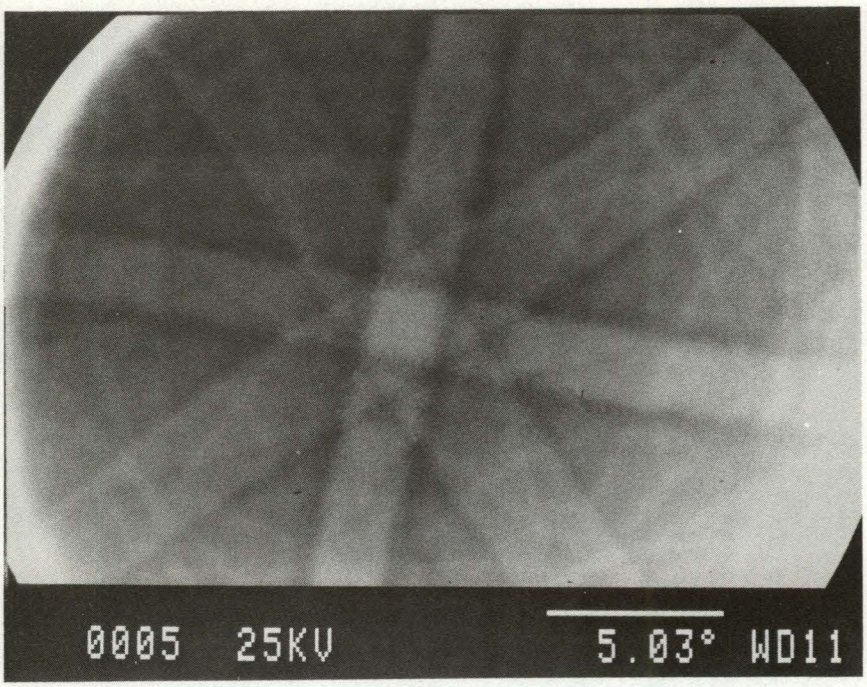
It was proposed that the quality of the BP film would improve with increasing thickness as has been demonstrated with SOS films [37]. The partial self annihilation of defects would lead to improved crystal quality for the surface layer for thicker silicon films grown on BP films. Previously published data indicated that the crystal quality of BP films grown thicker than 400 Å were relatively good with only slight improvement for thicker BP films [27]. However, no data has been published concerning the film quality of silicon layers grown on thick BP layers.

The single temperature Si-BP growth process was used to fabricate five wafers with 0.05, 0.1, 0.2, 0.5 and 1.0 μm BP layers covered by a 1.0 μm silicon layer. Electron channeling patterns (ECP) were used to determine relative crystal quality.

The ECP were obtained using a Jeol-848 SEM in backscatter mode with an accelerating voltage of 25 kV at a working distance of 10-11 mm. The ECP photographs of the top silicon layers are shown in Figures 6-8. All photographs indicate relatively high quality silicon. The pattern from the silicon layer on 0.2 μm BP wafer suffered from a lack of

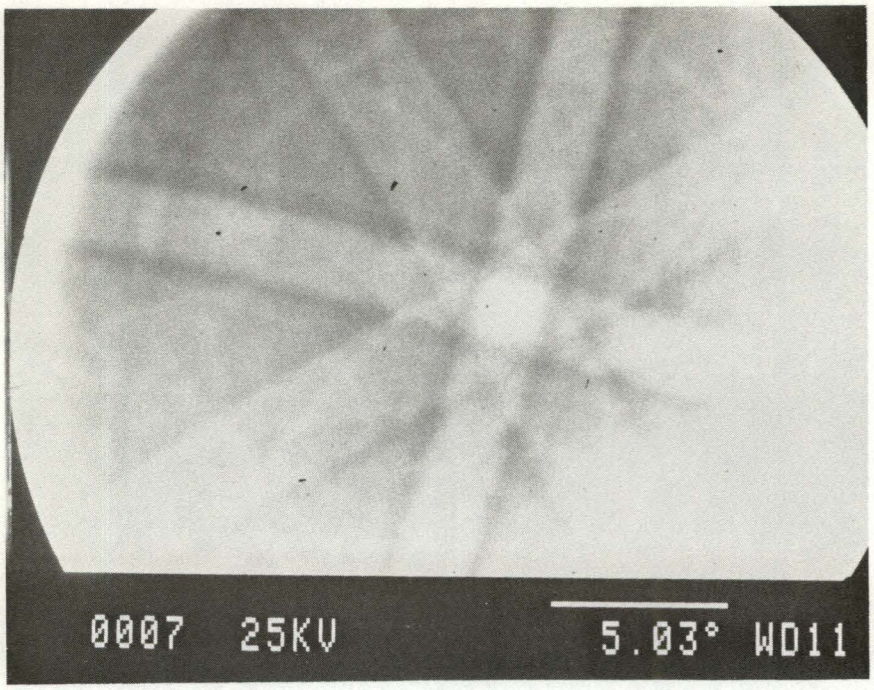


(a)

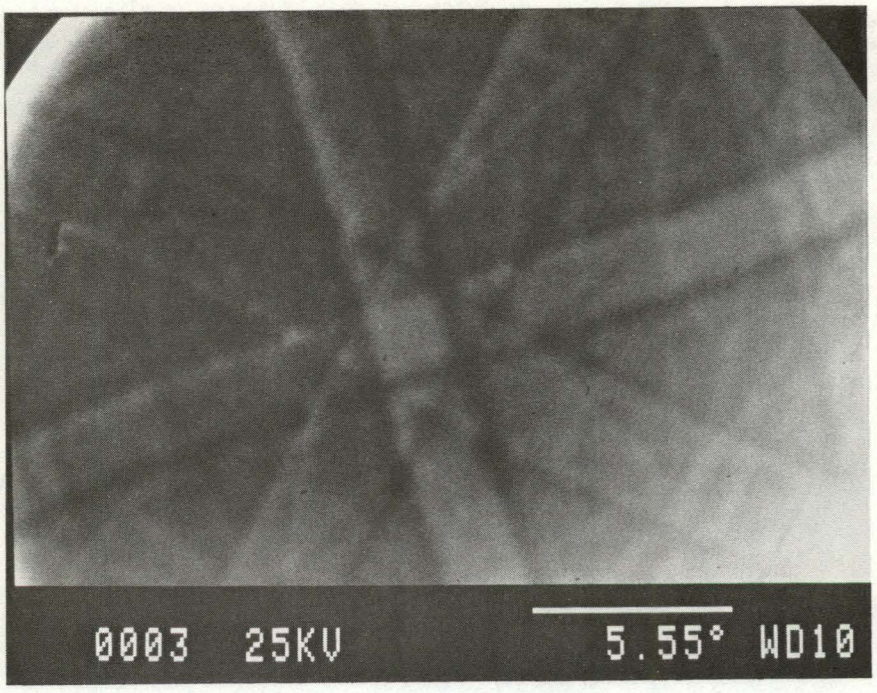


(b)

Figure 6. Electron Channeling Patterns of Silicon on (a) 0.05 and (b) 0.1 μm BP Layers.



(a)



(b)

Figure 7. Electron Channeling Patterns of Silicon on (a) 0.2 and (b) 0.5 μm BP Layers.

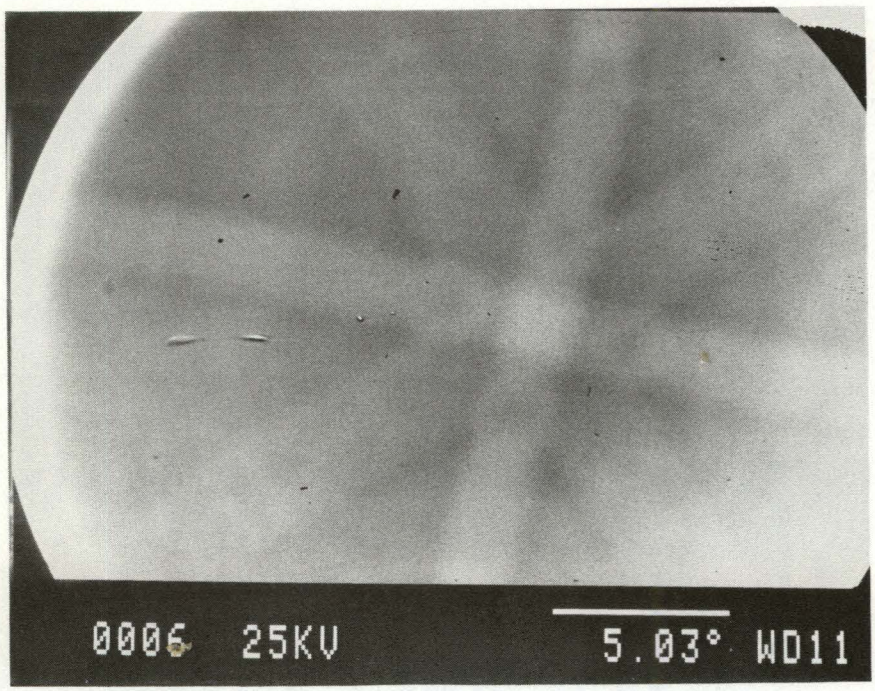


Figure 8. Electron Channeling Patterns of Silicon on 1.0 μm BP layer.

contrast due to the increased rocking angle of the electron gun. The quality of the silicon film remained about the same as determined from the ECP photographs as the thickness of the BP layer increased in agreement with results reported by Hirai and Shohno [27]. The crystal quality of the silicon layer was about the same for all samples as determined by the ECP. There was not a large change in the crystal quality of silicon grown on BP layers as thick as 1.0 μm. Optical microscopic examination of the surface revealed no differences between samples, all having a slightly roughened pebbled surfaces. While the surface was not uniformly smooth, the silicon layer was single crystal having a (100) orientation. High quality silicon layers can be grown on BP layers as thick as 1.0 μm. Examination of the silicon layer via ECP patterns proved that the layers were single crystal. Later, it will be shown that the silicon layers grown thicker than 5.0 μm on BP layers are suitable for use as substrate material for MOS devices.

CHAPTER VI

EXPERIMENTS LEADING TO THE GROWTH OF HIGH RESISTIVITY BP AT 1000°C

During the development of the single temperature Si-BP growth process, resistivity of as grown BP versus heating duration at 1050°C was examined for comparison with previously published results for BP grown at 950°C [34]. Kim and Shono reported an increase in BP resistivity to around 10^{11} Ω-cm after heating at 1050°C for two hours.

In the case of samples grown at Clemson University, the heating of the Si-BP-Si sandwich at 1050°C was found to increase the BP resistivity by less than an order of magnitude. The BP resistivity was found to be as high as 10^{6} Ω-cm following growth of the BP at 1000°C. Four point probe measurements of the resistivity of the surface of the BP layer lead to the discovery of an n^{+} silicon layer beneath the BP layer. The n^{+} silicon layer shorted any measurement of the horizontal resistivity of the BP layer as explained in Appendix B. The variation of BP resistivity versus growth temperature was found to change by a factor of ten over the range from 960°C to 1070°C. A detailed explanation of these results follows.

Heat Treatment of BP at 1050°C

Five wafers were prepared with 0.05, 0.1, 0.2, 0.5 and 1.0 μm of BP on silicon wafers. The reactor tube was cleaned following BP growth to remove excess boron and phosphorus

from the walls so that higher resistivity silicon could be grown on the BP layers. This cleaning would aid in the examination of the diffusion of excess boron and phosphorus from the BP layer into the silicon epitaxial layer during heat treatment. The BP layers were capped with a 1.0 micrometer layer of silicon. The wafers were broken into four pieces after growth of all of the layers. One quarter of each sample was heated at 1050°C for 30, 60, 90, and 120 minutes respectively.

Diffusion of Phosphorus into the Silicon Layer

Four point probe measurements of the top silicon layer indicated that phosphorus had diffused into the silicon during the heat treatment. The sheet resistance of the surface silicon following heating is shown in Figure 9. For all but the thickest BP samples, the surface sheet resistance of the silicon layer fell from around 500 Ω/sq to less than 10 Ω/sq after 120 minutes of heating at 1050°C. This sheet resistance corresponded to an impurity concentration of over 10^{19} cm^{-3} [38, p. 32]. All samples were doped n-type.

Attempts to measure both the horizontal and vertical resistance of the BP layer were thwarted by problems with the etching of silicon islands on the BP, thus making the measurement of the cross sectional area of each island impossible. Therefore, the resistivity was calculated from four point probe measurements of the BP surface and thickness measurements of the BP layer and plotted in Figure 10.

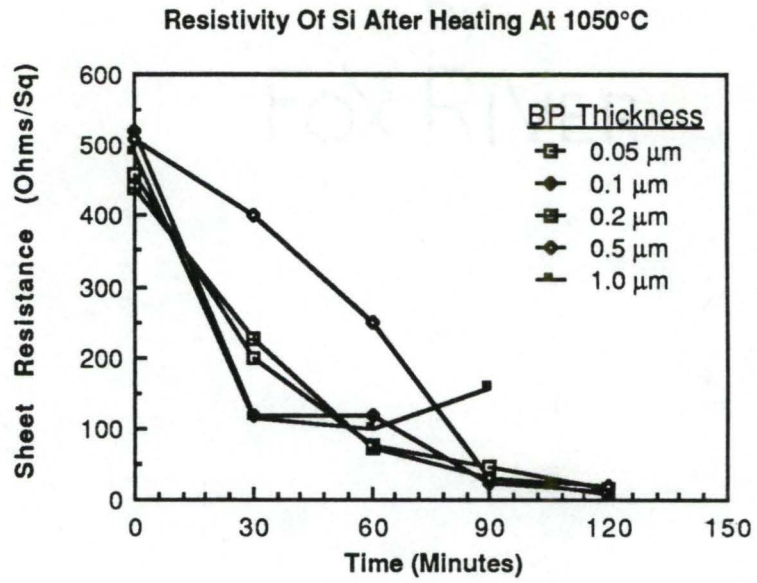


Figure 9. Resistivity of Top Silicon Layer after Heating at 1050°C. The top silicon layer is auto doped by the underlying BP layer as the sample is heated.

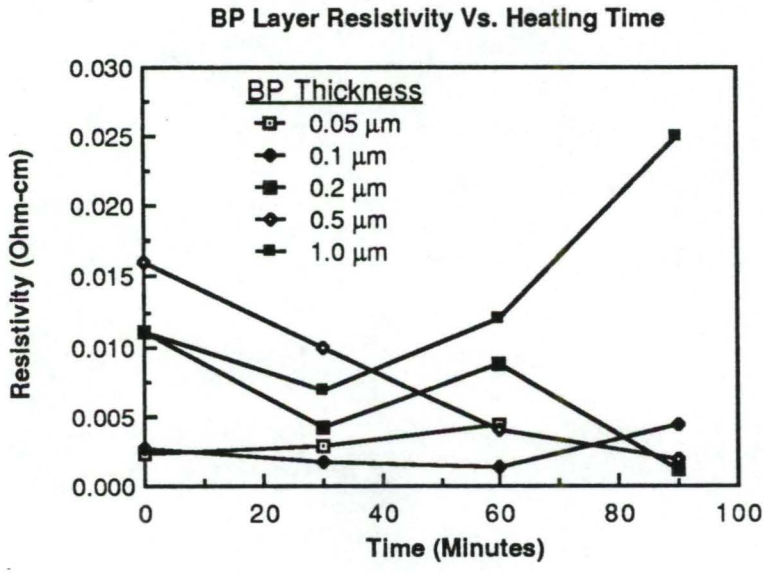


Figure 10. Resistivity of BP Layers after Heating at 1050°C. The measurements were shorted by n-type silicon at the Si-BP interface.

The horizontal resistivity measurements were shorted by the underlying n^+ layer as described previously. Only the resistivity of the thickest BP layer (1.0 μm) appeared to have increased. This increase was due to an increase in the vertical BP resistance down to the n^+ silicon layer beneath each contact probe. Only the 1.0 μm sample was thick enough to observe an increase in resistivity.

High Resistivity BP Grown at 1000°C

Two silicon substrates were covered with 0.2 and 0.5 μm BP layers respectively. Following cleaning of the phosphorus from the tube, each wafer was coated with 1.0 μm of silicon and heated at 1050°C. Small chips were scribed and broken from each half wafer sample after 30, 60, 90 and 120 minutes of heating. The area and both forward and reverse vertical resistance of each chip was measured. The chips were then lapped and the thicknesses of the BP layers were measured.

The forward and reverse vertical resistivities of the BP layers were calculated and have been plotted in Figure 11 and 12. The resistivities of the BP layers were found to be very high ($\cong 10^6$ Ω-cm) even before heat treatment. The BP layers grown at 1000°C had resistivities of the same order of magnitude as those grown by Shono at 950°C and subsequently heated for over 100 minutes at 1050°C [34]. Thus, it was possible to grow a high resistivity BP layer covered by an epitaxial silicon layer. Unless a BP resistivity higher than 10^7 Ω-cm is required, no heat treatment would be necessary following

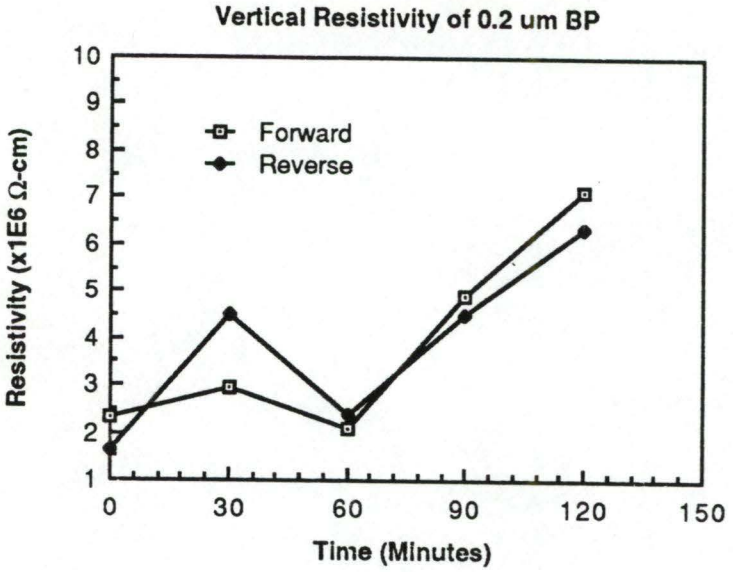


Figure 11. Vertical Resistivity Measurements of the 0.2 μm BP Layer. The resistivity of the BP was found to be very high even before heat treatment.

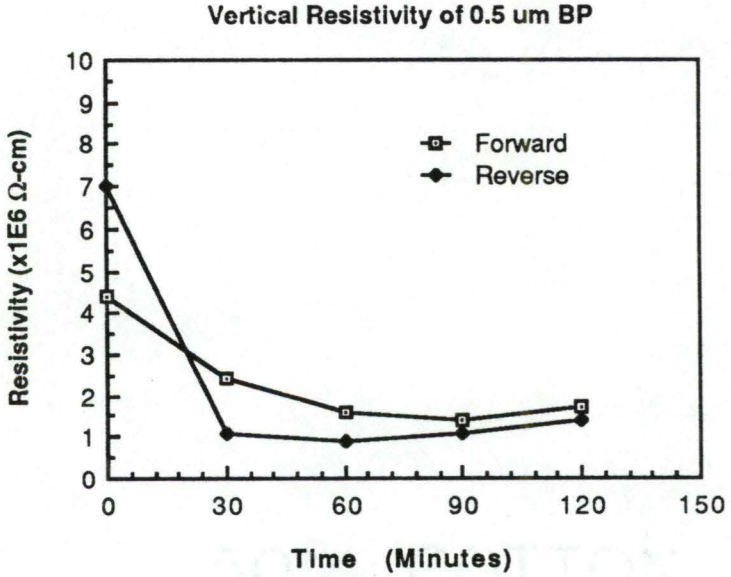


Figure 12. Vertical Resistivity Measurements of the 0.5 μm BP Layer. The resistivity has decreased slightly with time.

the film growth. Thus the diffusion of boron and phosphorus into the top epitaxial silicon layer would be limited to some extent when the heat treatment was eliminated.

BP Resistivity Versus Growth Temperature

In order to further characterize the growth of BP with respect to process parameter variations, an examination was made of the as-grown resistivity of BP versus growth temperature. Six wafers were prepared with 0.2 μm BP layers on (100) silicon substrates. The growth temperatures were 959, 978, 997, 1027, 1055 and 1070°C.

The forward and reverse vertical resistivities for these wafers have been plotted in Figure 13. The resistivity varied from a minimum of 0.6 MΩ-cm at 975°C to over 5.0 MΩ-cm at approximately 1040°C. All BP films were n-type. Slight differences in forward and reverse vertical resistivities at 1055°C indicated the presence of a possible heterojunction barrier between the BP epitaxial layer and the silicon substrate.

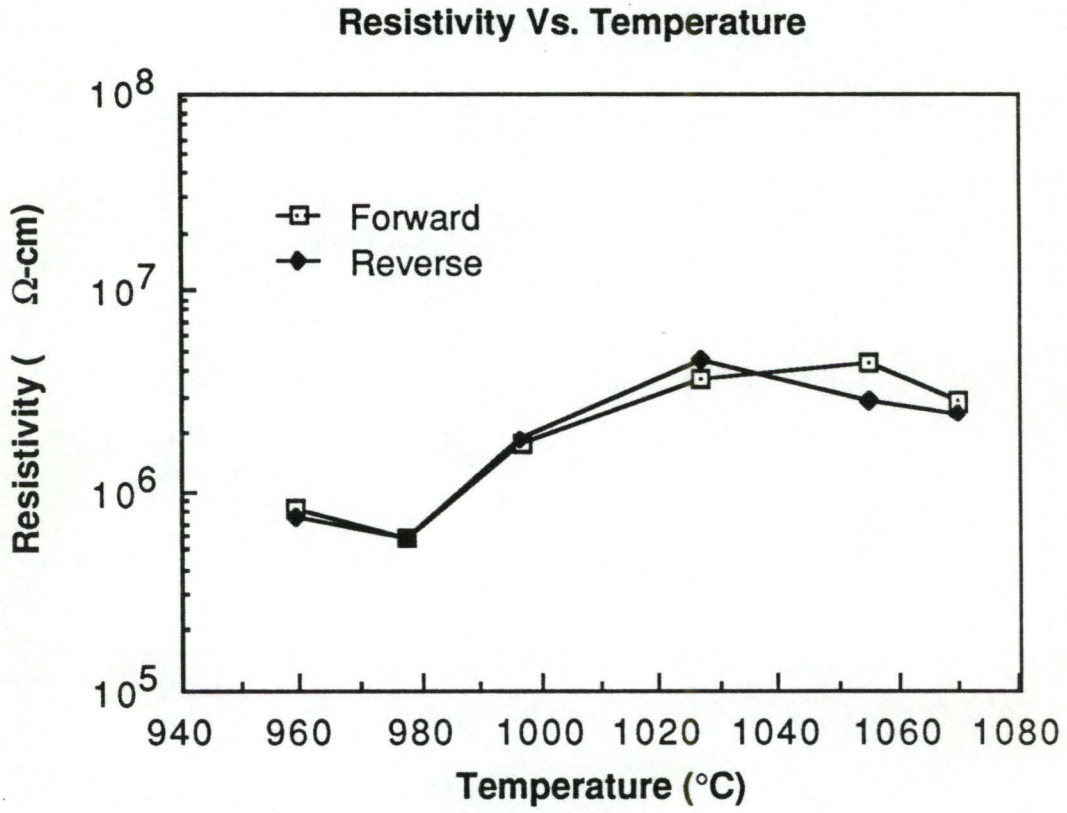


Figure 13. Forward and Reverse Resistivity Measurements of 0.2 μm BP Wafers #364-#370 Grown at Temperatures from 950°C - 1075°C. There is a maximum resistivity of 5×10^6 Ω-cm for films grown at around 1040°C.

CHAPTER VII

QUALITY OF SILICON LAYER VERSUS THICKNESS FOR SI-BP STRUCTURES GROWN AT 1000°C

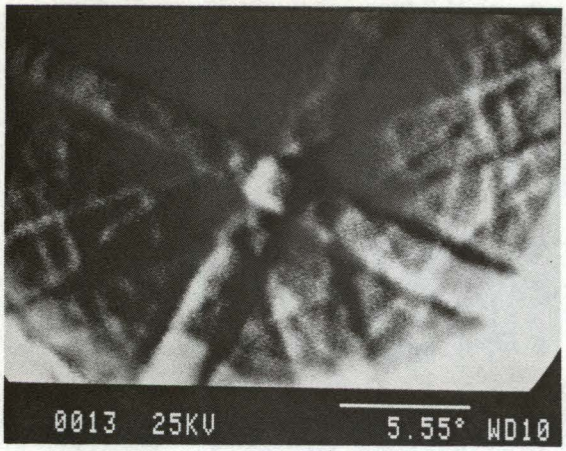
The quality of the silicon layer grown on a BP layer was examined as a function of the thickness of the two layers. Single crystalinity of the epitaxial layers has been examined using ECP patterns. The suitability of the epitaxial silicon layer to serve as substrate material for MOS devices has been examined using common MOS device parameters.

Si-BP Wafer Fabrication

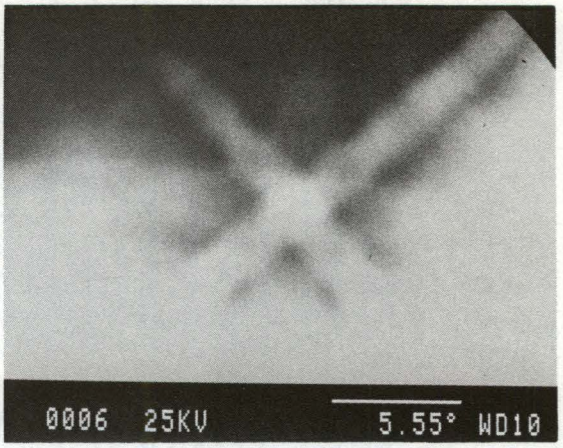
Two sets of five Si-BP-Si wafers were prepared with 0.2 and 0.4 μm BP on ten (100) p-type 6-10 Ω-cm silicon wafers grown at 1000°C. The reactor tube was cleaned of excess boron and phosphorus after the growth of each of the BP films. One to five micrometers of silicon was grown on top of the BP layers at 1000°C.

Electron Channeling Patterns

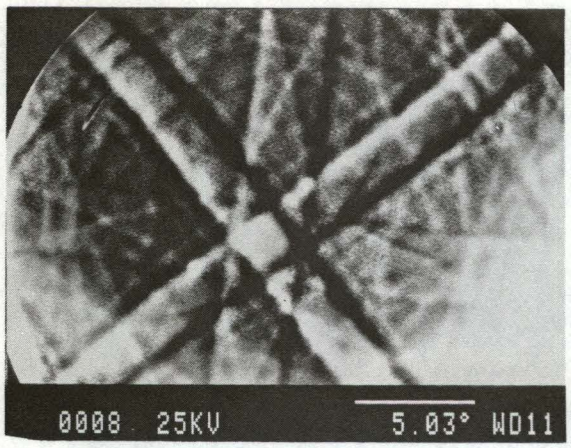
The surface silicon layers were examined following fabrication using electron channeling patterns. The ECP patterns for the surface silicon layer of the ten Si-BP-Si wafers have been shown in Figures 14 and 15. The general features of the patterns were very similar to the signature patterns from a clean (100) bulk silicon wafer shown in Figure 16. The ECP patterns were compared in order to



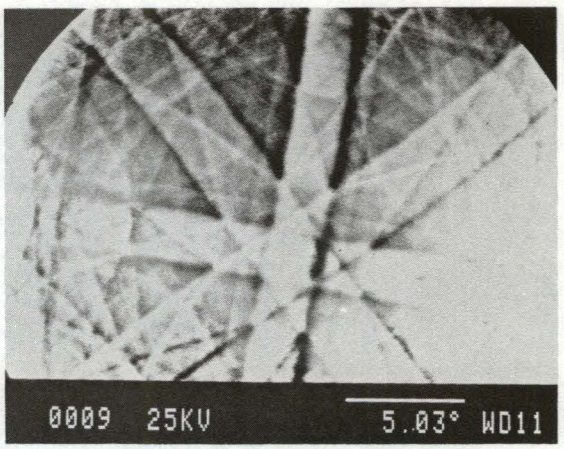
1



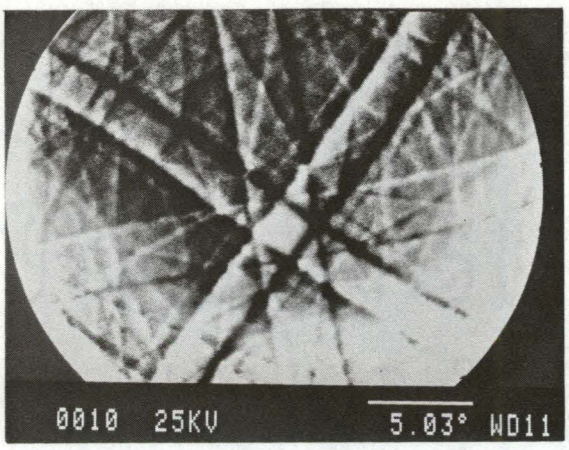
2



3

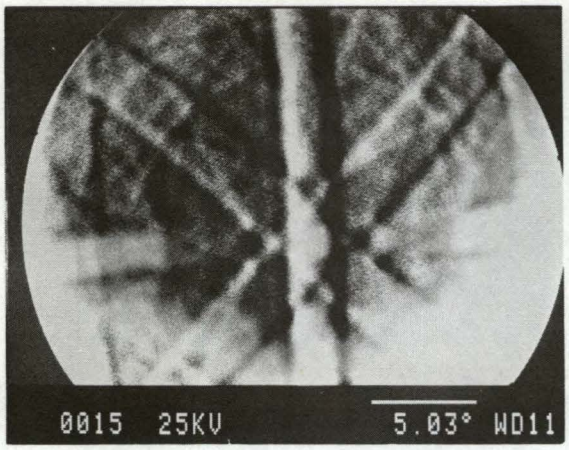


4

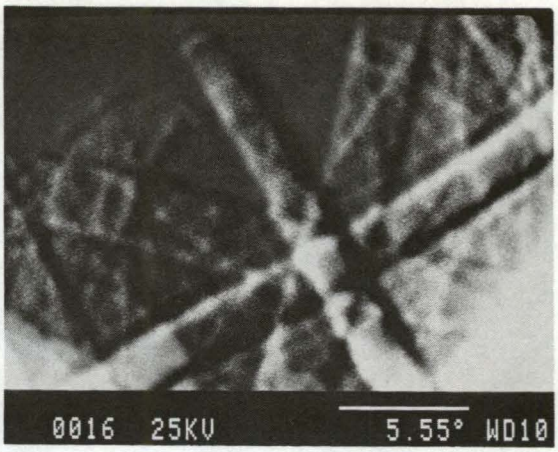


5

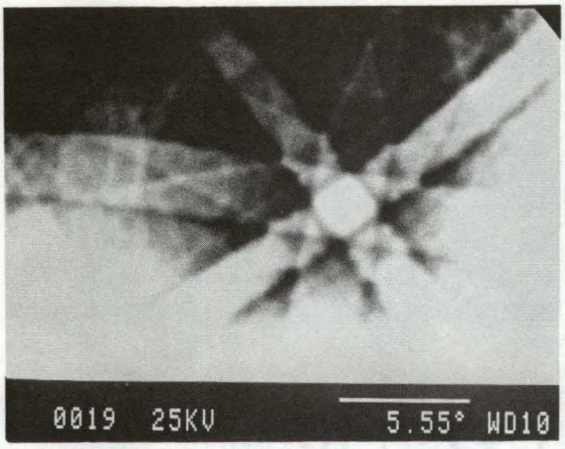
Figure 14. Electron Channeling Patterns of Silicon on BP for Wafers #285-#289. These patterns are for 1, 2, 3, 4 and 5 μm of silicon on 0.2 μm BP.



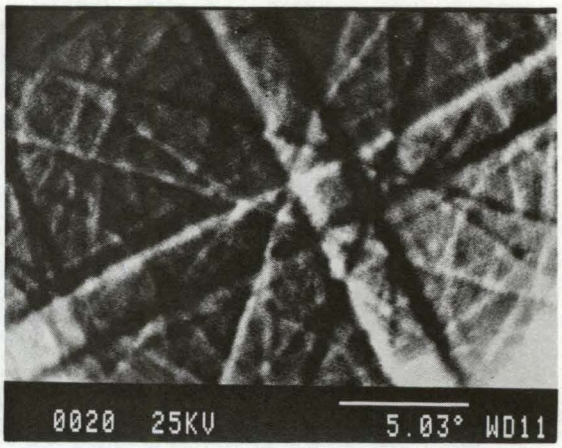
1



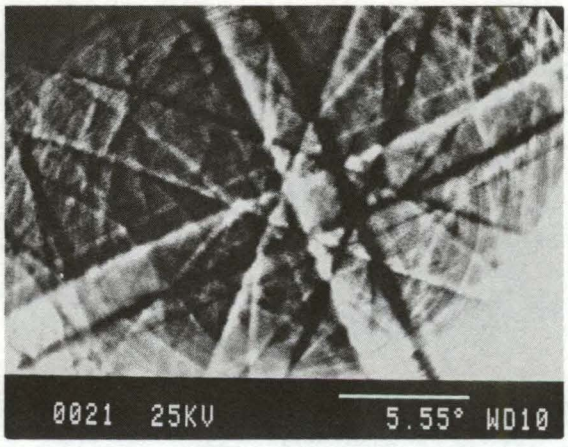
2



3

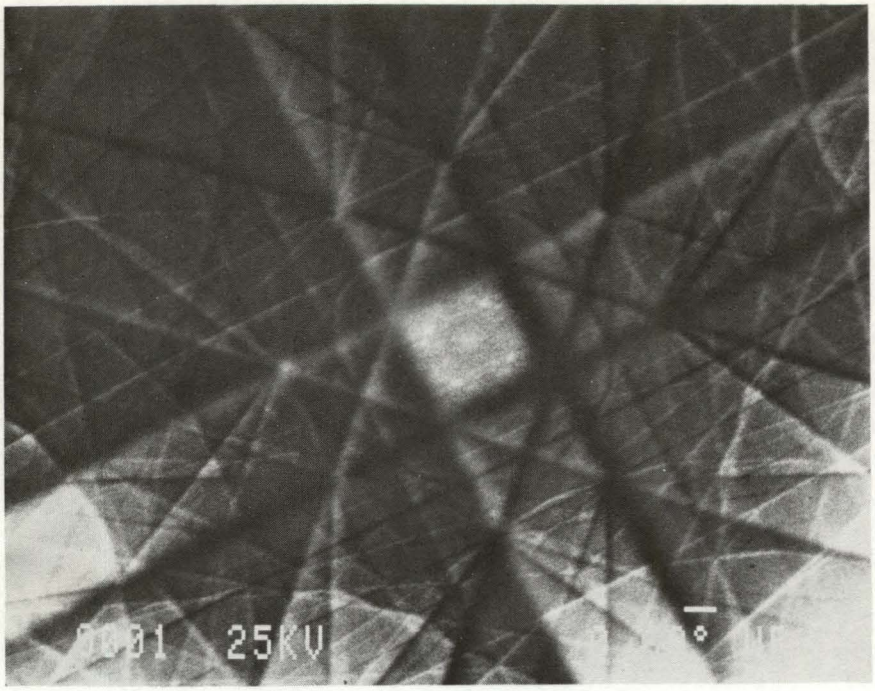


4

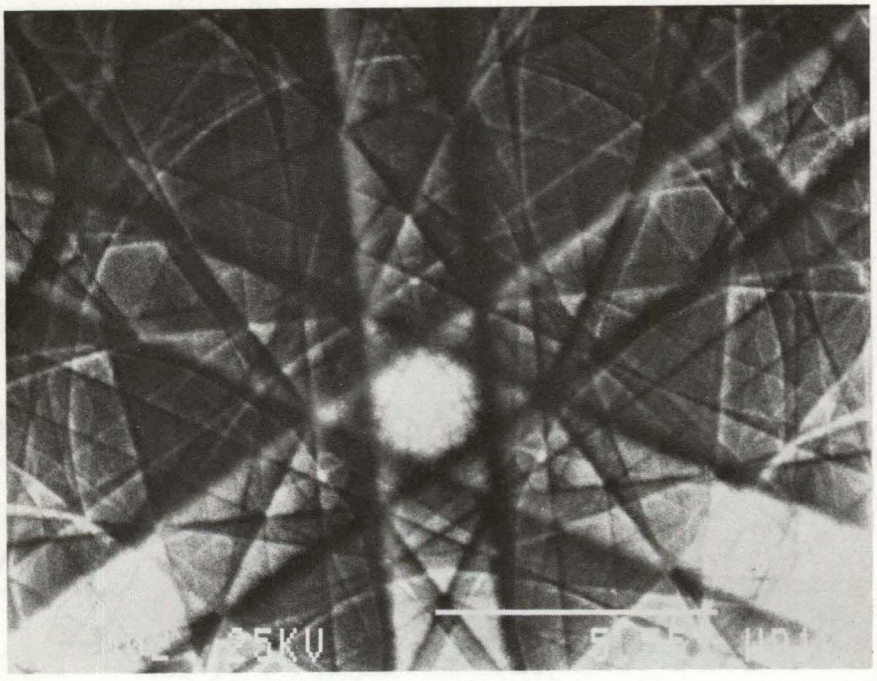


5

Figure 15. Electron Channeling Patterns of Silicon on BP for Wafers #298-#302. These patterns are for 1, 2, 3, 4, and 5 μm of silicon on 0.4 μm BP.



(100)



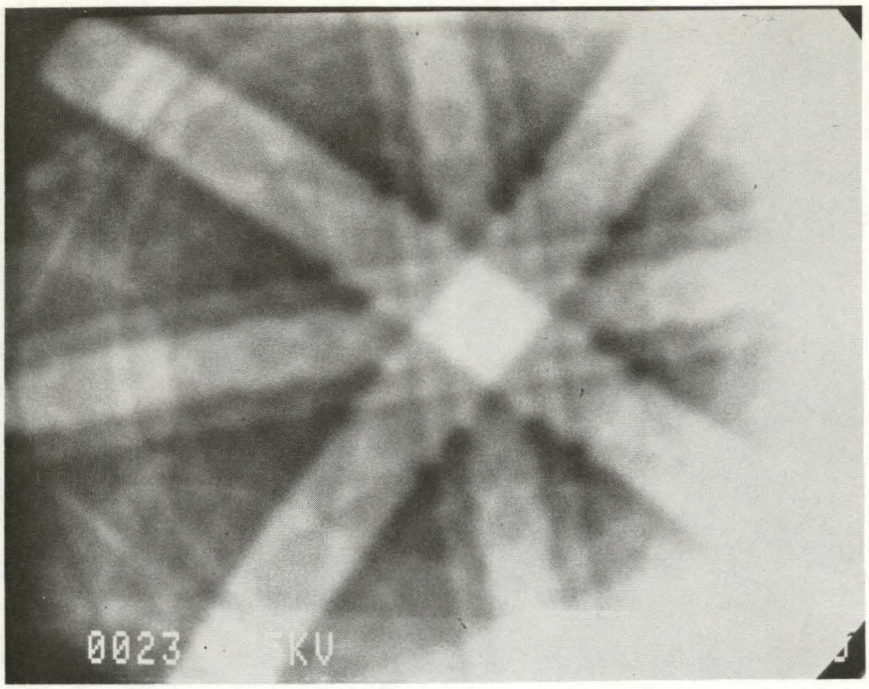
(111)

Figure 16. Electron Channeling Patterns for (100) and (111) Bulk Silicon Wafers.

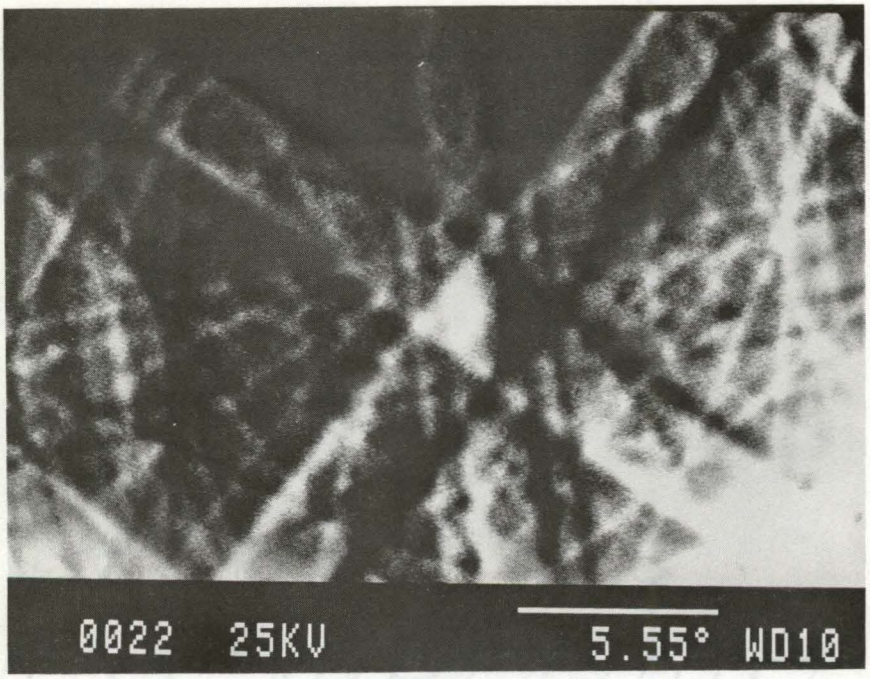
determine relative epitaxial crystal quality. Electron channeling patterns were taken of the surface silicon layers using a Jeol-848 SEM in backscatter mode. The electron channeling patterns were obtained using an accelerating voltage of 25 KV at a working distance of ten to eleven millimeters.

The silicon on BP layers did not show as high a degree of crystallinity as exhibited in ECP patterns of SOS samples tested earlier. In general, the silicon layers grown on the 0.4 μm BP layers had slightly sharper ECP patterns than those grown on the 0.2 μm BP layers. Silicon crystalline quality was largely determined by the growth conditions. The apparent lack of long range crystallinity seen in the 2.0/0.2 and 3.0/0.4 ECP photos indicated that these wafers probably had low quality silicon following epitaxial growth. These wafers also had hazy surfaces which was characteristic of an inferior quality of the epitaxial silicon layer.

The electron channeling pattern of the 0.2 μm BP layer has been shown in Figure 17. This ECP had a slightly different pattern than the (100) silicon layer. Still present was the strong (100) characteristic of the crystal lattice with its associated two fold axis of symmetry. Additional reflections in the pattern indicated some irregularity in the crystal structure of the BP layer as compared to the clean lines of the bulk silicon ECP patterns. The irregularities may have been caused by differences in the scattering cross sections of boron and phosphorus atoms within the crystal lattice.



(a)



(b)

Figure 17. Electron Channeling Pattern of Uncoated 0.2 μm BP Wafer #293. Picture (a) shows strong (100) pattern. Picture (b) was taken in composition mode to increase image contrast.

MOS Devices

MOS transistors and capacitors were fabricated on the above Si-BP-Si wafers and on a bulk silicon wafer by the National Bureau of Standards. These devices were used to help characterize the crystal quality of the epitaxial silicon layers. The bulk silicon wafer was processed under the same conditions as the Si-BP-Si wafers and was used for comparison. The transistors were aluminum gate PMOS devices with a gate width of 240 μm and gate length of 32 μm. The gate oxide varied from 870 to 900 Å thick. The drain and source regions were boron implants with a surface concentration of 10^{20} cm^{-3} and a junction depth of 0.5 μm. The capacitors were circular with a gate area of 0.0065 cm^2. Processing was carefully designed to limit thermal excursions thereby minimizing shifts in the doping profile of the top silicon layer during IC processing.

The subthreshold characteristics, drain characteristics, effective surface field effect hole mobilities in both the linear and saturation regions and threshold voltage of the devices on the Si-BP-Si wafers were measured and compared to bulk silicon values. The transistor and capacitor characteristics were examined to determine doping concentration, threshold voltage, surface state density and effective generation lifetime. Quasistatic capacitance-voltage (C-V) measurements were used to determine the surface state density as a function of the surface potential. High frequency C-V

measurements were used to determine the surface doping concentrations of the epitaxial silicon layers.

Surface Doping Concentration

Doping concentrations were derived from surface resistivity measurements, reverse breakdown voltage measurements and high and low frequency C-V measurements. The results of the doping concentration measurements have been compiled and plotted in Figure 18.

Thicker silicon layers were found to have lower average doping concentration. The drop in resistivity with increasing silicon thickness was a direct result of autodoping by the underlying BP layer as it was being covered with epitaxial silicon. The doping concentration had a lower limit of approximately $5x10^{15}$ cm^{-3} for silicon layers thicker than five micrometers.

Doping concentrations determined from reverse breakdown voltages were found to be two to three times higher than values from 4-point probe measurements probably due to higher background doping concentration at the 0.5 μm junction depth. The doping concentrations derived from C-V measurements were approximately an order of magnitude lower than doping concentrations derived from reverse breakdown voltages and 4-point probe measurements. The doping concentration values from 4-point probe measurements were higher than actual surface doping concentration due to the averaging over the graded concentration of the silicon layer used to determine the values from 4-point probe measurements.

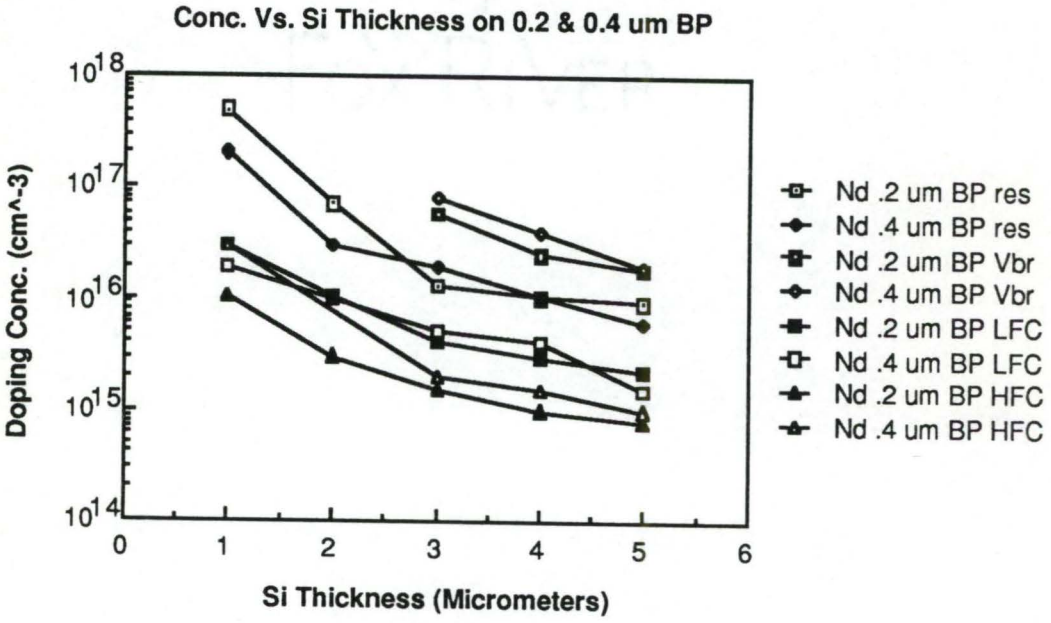


Figure 18. Impurity Concentration of Silicon Layers on 0.2 and 0.4 μm BP Layers. Measurements were taken from resistivity measurements, reverse breakdown voltages and high and low frequency C-V measurements.

MOS Device Properties

Transistors fabricated on 1.0 and 2.0 μm silicon layers did not operate properly due to the high background doping concentration and shorting between the source and drain regions. These shorts could have been caused by spikes through the diffusion layer. The current-voltage (I-V) drain characteristics of these devices were ohmic with an average resistance of 165 Ω, 291.3 Ω and 350 Ω for 1.0 and 2.0 μm silicon on 0.2 μm BP and 1.0 μm silicon on 0.4 μm BP layers respectively. The gate voltage was varied from 0 to 9 volts with no effect on the I-V characteristic. Operating characteristics for transistors on 3-5 μm silicon layers improved as the silicon layers became thicker.

The subthreshold conduction currents for MOS transistors on epitaxial layers have been shown in Figures 19 and 20. The subthreshold current, at a gate voltage V_g = 0 volts, increased as the silicon thickness decreased due to the increased doping concentration and increased defect density. Thus, the subthreshold slope could not be measured for devices fabricated on 1.0 and 2.0 μm silicon layers due to their ohmic I-V characteristics. Subthreshold currents at V_g = 0 V in many of the devices on the 5.0 μm silicon layers were as low as 10^{-11} A. This was comparable to the current measured on the bulk silicon devices.

Surface state densities were determined from quasistatic C-V curves shown in Figures 21 and 22 and have been plotted in Figures 23 and 24 [39]. These surface state density

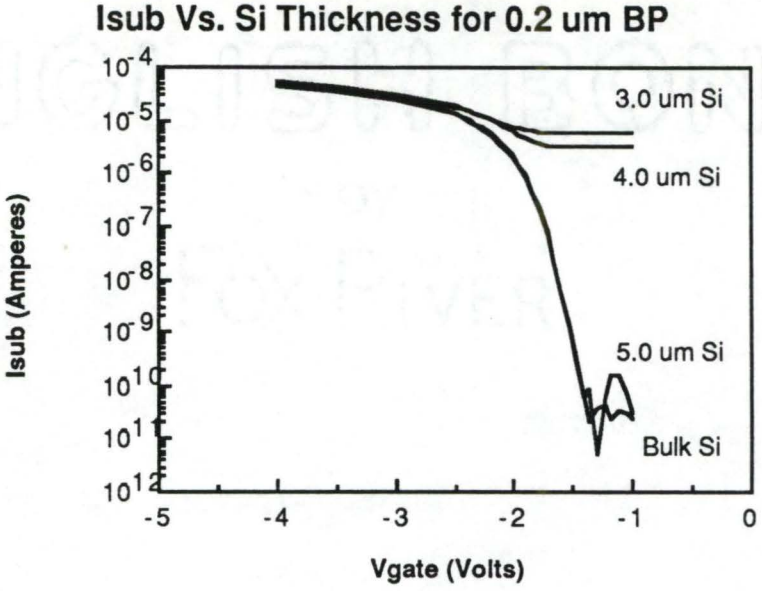


Figure 19. Subthreshold Characteristics of 3-5 μm Silicon Layers on 0.2 μm BP. The effects of high background doping concentration are evident in the high subthreshold currents on the 3 μm layer. The 5 μm curve is similar to that of bulk silicon.

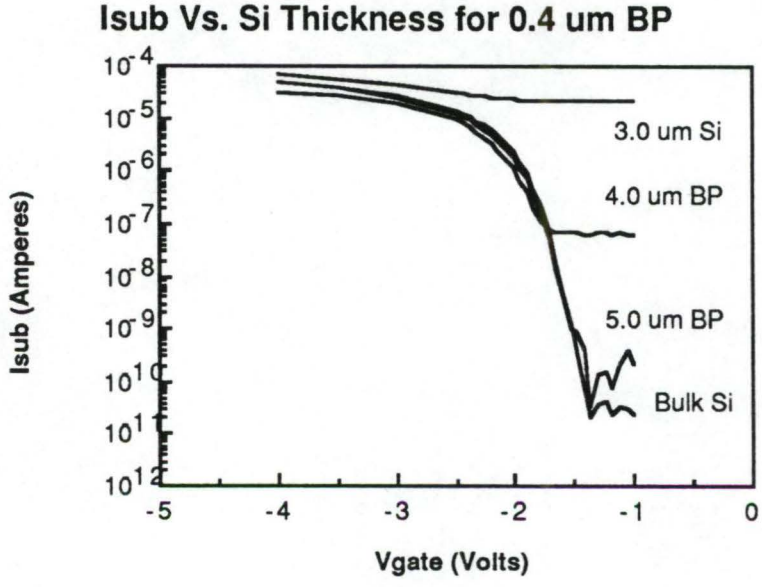


Figure 20. Subthreshold Characteristics of 3-5 μm Silicon Layers on 0.4 μm BP. The effects of high background doping concentration are evident in the high subthreshold currents on the 3 μm layer. The 5 μm curve is similar to that of bulk silicon.

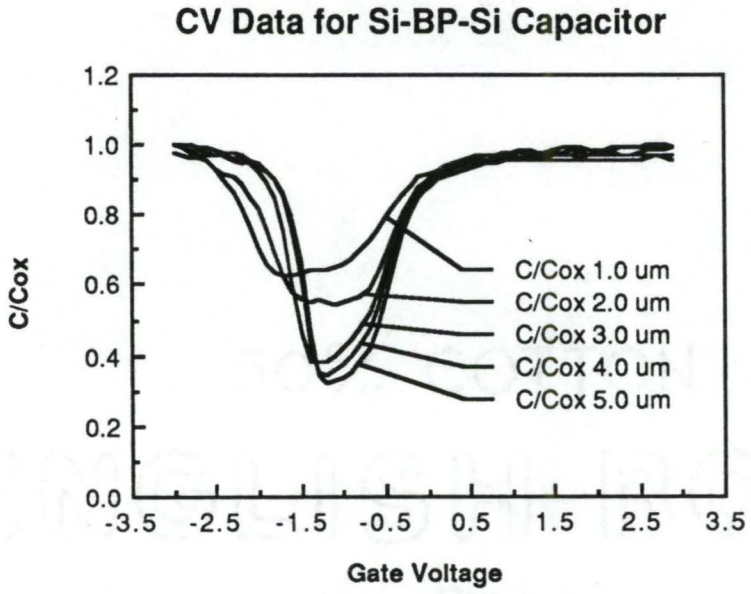


Figure 21. Quasistatic Capacitance Versus Voltage Measurements for 0.2 μm BP Wafers.

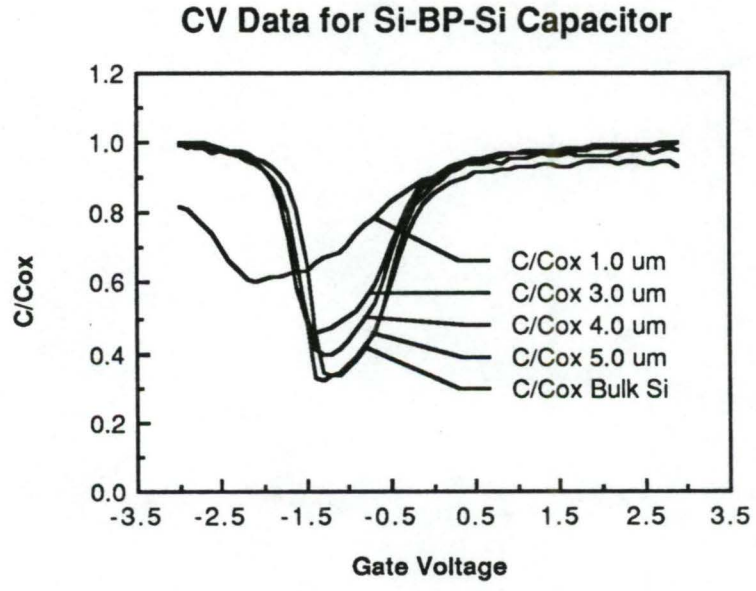


Figure 22. Quasistatic Capacitance Versus Voltage Measurements for 0.4 μm BP Wafers.

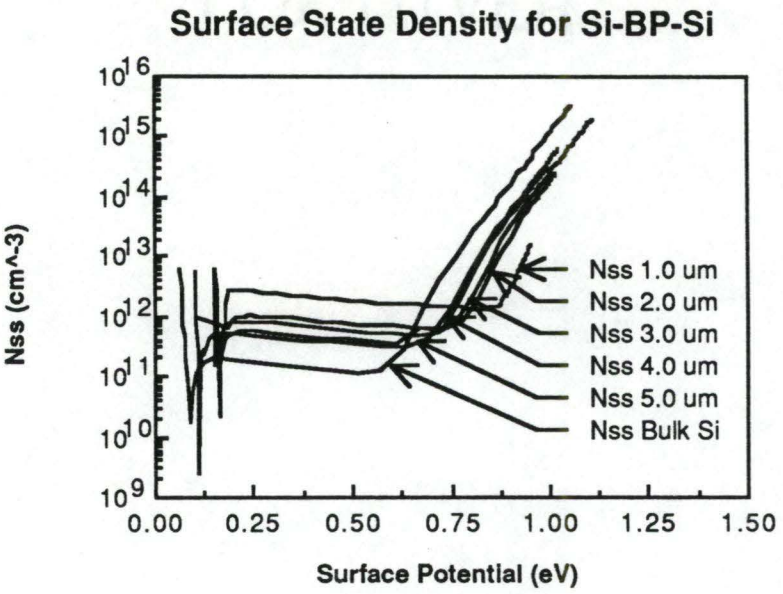


Figure 23. Surface State Density as a Function of Silicon Thickness for 0.2 μm BP.

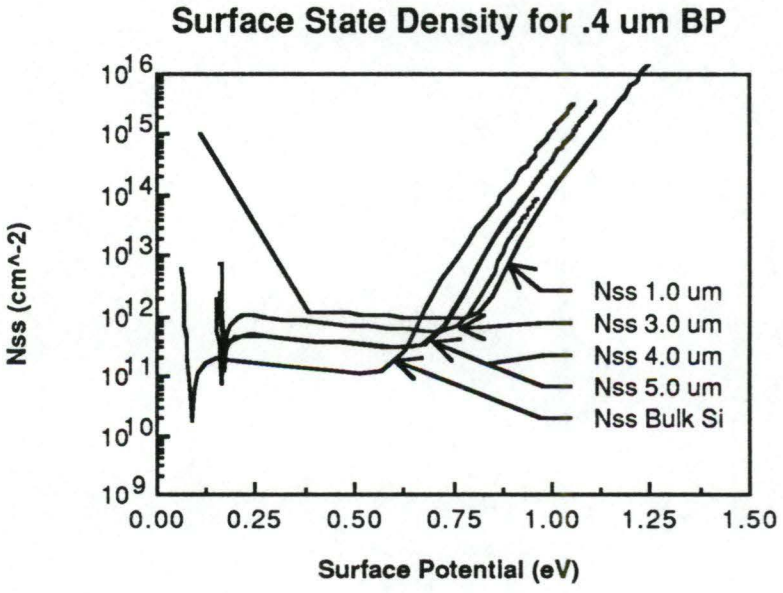


Figure 24. Surface State Density as a Function of Silicon Thickness for 0.4 μm BP.

values were of the same order of magnitude as the surface state densities derived from the subthreshold slope measurements which were $1.4x10^{11}$, $2.7x10^{11}$, $3.8x10^{11}$ cm^{-3} for 3, 4, and 5 μm silicon on 0.2 μm BP and $5.1x10^{11}$, $5.0x10^{11}$ cm^{-3} for 4 and 5 μm silicon on 0.4 μm BP.

High frequency (1 MHz) C-V data of capacitors on the 0.2 and 0.4 μm BP wafers were measured. This data has been plotted in Figures 25 and 26. High frequency and quasistatic curves for the 5.0 μm silicon layer on 0.4 μm BP layer have been compared in Figure 27. The curves were the same in the depletion region. Both of the 5.0 μm layer curves were similar to the bulk silicon curve but had a slightly greater C/Cox ratio in the inversion region due to higher doping concentrations. The slope of the bulk silicon, high frequency C-V curve in the inversion region was greater than the Si-BP-Si counterpart due to greater generation lifetimes. The surface doping concentrations for the top silicon layers shown in Figure 18 were derived from the high frequency C-V curves in Figures 25 and 26 [37, p. 374].

The effective generation lifetimes for 0.2 and 0.4 μm wafers and bulk silicon were determined from capacitance-time (C-t) measurements [40-43] and have been plotted in Figure 28. The maximum lifetimes on Si-BP wafers were found to be 0.18 μS. This value was over an order of magnitude lower than lifetime found on bulk silicon. In general, the lifetime decreased with decreasing silicon thickness to a minimum of 0.04 μS on 3.0 μm silicon layer. Lifetime measurements

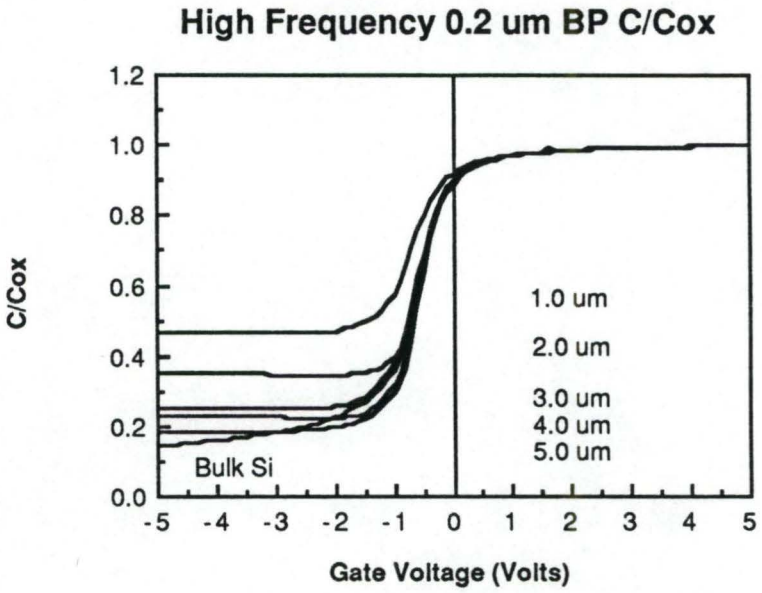


Figure 25. High Frequency C-V Measurements for 0.2 μm BP Wafers. The frequency was 1 MHz.

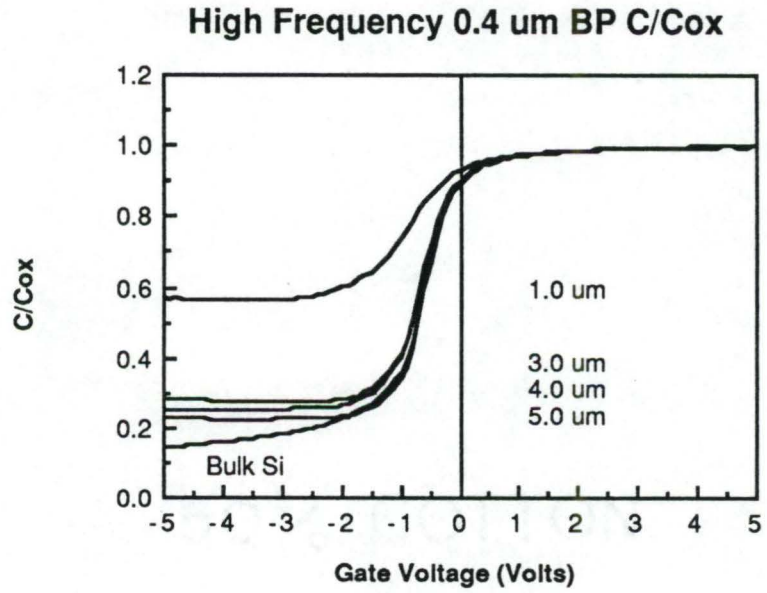


Figure 26. High Frequency C-V Measurements for 0.4 μm BP Wafers. The frequency was 1 MHz.

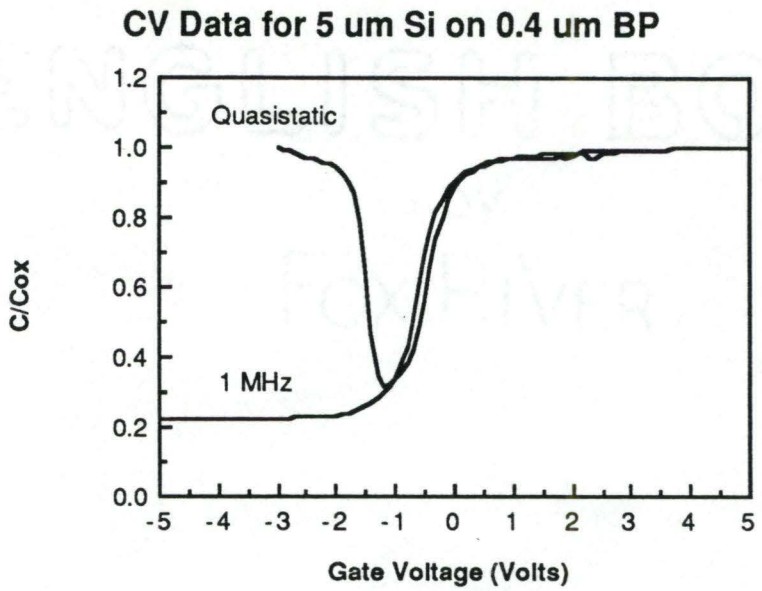


Figure 27. Comparison of Quasistatic and High Frequency C-V Curves for a Capacitor on 5.0 μm Silicon on 0.4 μm BP Layers. The curves are the same in the depletion region.

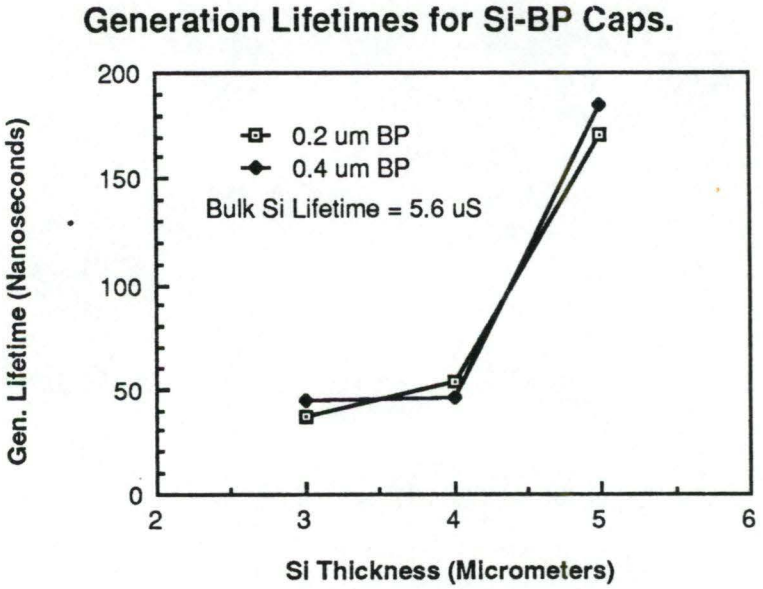


Figure 28. Effective Generation Lifetimes for Silicon on 0.2 and 0.4 μm BP Derived from C-t Measurements.

could not be made on the 1.0 and 2.0 μm silicon layers due to instrument limitations. Generation lifetimes could not be measured shorter than 10 ns.

The average effective surface hole mobility in the linear region of MOS devices was 230 $cm^2/V-s$ while the average mobility, in the saturation region was 150 $cm^2/V-s$. Mobilities varied little with respect to silicon layer thickness. The mobilities were lower than bulk silicon values at these doping concentrations due to surface defects but slightly higher than previously published data on a two step silicon layer on BP [16].

The threshold voltages were not measurable on the devices fabricated on 1, 2 or 3 μm silicon layers due to high subthreshold currents mentioned previously. The average threshold voltage, V_t = -2.0 V on the 4 and 5 μm silicon layers having with very little variation from wafer to wafer. The small variation in V_t was expected since it was previously shown that the surface doping concentration, N_d, and surface state density, N_{ss}, on the 4 and 5 μm silicon layers were approximately equal. Using a value of $N_{ss} = 3x10^{11}$ states-cm^{-3} and $N_d = 10^{15}$ cm^{-3}, the theoretical value of V_t was found to be -2.14 volts [44]. The experimental value was within 6.5% of the actual value.

Summary of Device Properties

The ECP of both the BP and silicon epitaxial layers showed strong (100) orientation. Extra reflections were noted in the BP photographs. The BP crystal quality was very

good showing little variation in the surface crystal quality between the 0.2 and 0.4 μm layers. The silicon layers were shown to have (100) orientation with very good crystal quality up to 5 μm thick.

All silicon layers were found to be n-type due to auto doping from excess phosphorus in the underlying BP layer. Surface doping concentrations were as low as $5x10^{15}$ cm^{-3} with a surface state density as low as $5x10^{11}$ $ev^{-1}cm^{-2}$ on 5 μm silicon layers. Subthreshold currents at V_g = 0 volts were as low as 10^{-11} amperes on 5 μm silicon layers. Devices manufactured on 1.0 and 2.0 μm silicon layers had ohmic I-V characteristics. Devices manufactured on thicker silicon layers worked well having I-V and C-V characteristics as good as those of devices fabricated on bulk silicon processed at the same time. Thus, the quality of the silicon layer grown on BP using the single temperature process was relativity good. The previous results indicate that it was possible to grow MOS device quality silicon on BP using the single temperature Si-BP structure when the top silicon layer was thicker than 5.0 μm.

CHAPTER VIII

CONCLUSIONS

A single temperature heteroepitaxial process was developed for the growth of silicon on BP on bulk silicon. It has been shown that boron phosphide can be grown on silicon as a high resistivity epitaxial layer. In addition, device quality silicon can be grown on the high resistivity BP layer by cleaning the reactor tube of excess boron and phosphorus after BP growth. The resistivity of the BP layer was not high enough to serve as the insulating layer in a SOI structure and the presence of boron and phosphorus, both dopants in silicon, preclude the use of BP for most silicon processes. It does not appear possible, at this time, to heteroepitaxially grow multiple Si-BP layers with both high resistivity BP and low doping of the silicon layer during the same epitaxial run without cleaning the reactor between film growths.

MOS devices were fabricated on the top epitaxial silicon layer. Operating transistors were fabricated on silicon layers thicker than 3.0 μm. Characteristics of transistors on the 5.0 μm silicon layers were similar to those on bulk silicon processed at the same time. Subthreshold currents were as low as 10^{-11} amperes. Surface state densities were on the order of 10^{11} states/cm^2. Surface doping concentrations were as low as 10^{15} cm^{-3} on 5 μm epitaxial silicon layers.

Linear and saturation effective mobilities were as high as 250 and 150 $cm^2/V-s$ respectively. Reverse diode breakdown voltage was shown to be a function of silicon thickness reaching a maximum of 35 volts on the 5.0 μm silicon wafers. The previous results indicated that MOS device quality silicon layers were grown on BP layers.

In 1978, Takenaka [29] concluded that the BP layer did not act as a diffusion source in the creation of a n+ silicon layer beneath the BP layer. In 1985, Sugiura [3] reported threshold voltage shifts in devices fabricated on multiple Si-BP layers were due to autodoping from the BP layer. Sugiura's conclusions have been confirmed in this paper. Results have shown that there was significant autodoping of the silicon layer from the underlying BP layer during normal MOS processing.

Analysis of the ECP patterns indicated that good quality silicon films were grown on BP films. The apparent lack of crystal quality in the ECP patterns from 2.0/0.2 and 3.0/0.4 μm Si-BP layers, indicated in Chapter VII, was due to the process parameters which drifted out of specification during the film growths. Exactly which parameters were affected was not determined.

Based on previous results [1-35] and the work presented in this dissertation, it would appear that MOS device quality silicon films can be grown on BP films when the silicon layers were grown thicker than 5 μm and the reactor tube was cleaned prior to silicon growth. The increase in silicon

film quality can be expected to continue in thicker silicon films in the range of 5 to 10 μm. Several MOS device characteristics such as subthreshold current and surface state density have apparently reached process limits in 4 and 5 μm silicon layers while other parameters still have room for improvement.

The overall conclusion was that there were better materials available for use as a semi-insulating layer between silicon layers used for MOS devices than BP. Solutions to some of the autodoping problems were not conducive to mass production of semiconductor devices thus limiting the usefulness of the BP layer in the typical MOS process.

Other uses of boron phosphide might be investigated. It has been shown that BP is a very hard material which might serve in some applications as a scratch resistance coating. In addition, micro-machining could produce hanging structures of BP over silicon pits by the etched removal of the underlying silicon substrate material. Such structures could have promising uses as transducers in the measurement of sound, heat or pressure. The use of BP as a compatible material with other III-V semiconductor compounds such as GaAs could be investigated. The addition of a few molar percent of other III-V elements such as Al, N, In and Sb might be expected to adjust in the band structure of BP similar to changes observed in GaAs when these elements are added. It might be that in certain applications, the presence of a graded doping structure in the silicon layer might be useful.

APPENDICES

Appendix A

Calculation of the Index of Refraction of BP

Introduction

The index of refraction of the BP films grown at Clemson University was found by examining a lapped sample under monochromatic light. Wafers #309 and #310, with 0.5 and 1.0 μm of BP respectively were covered by a layer of silicon and had sufficiently thick BP layers making measurement of the index of refraction of the BP layer possible. The average index of refraction for these BP samples was found to be 2.8.

Experimental Procedure

The index of refraction was found by measuring the distance between dark fringes in a BP layer covered by silicon and comparing the relative distances in the silicon and BP layers. As shown in Figure A-1, when lapped at a shallow angle (approximately one degree) and illuminated by monochromatic light (λ = .546 μm) light and dark fringes appear across the lapped portion of the sample due to constructive and destructive interference. Dark fringes occured when

$$D_{Si} = \frac{\lambda (n-1)}{2 \eta} \qquad \text{(A-1)}$$

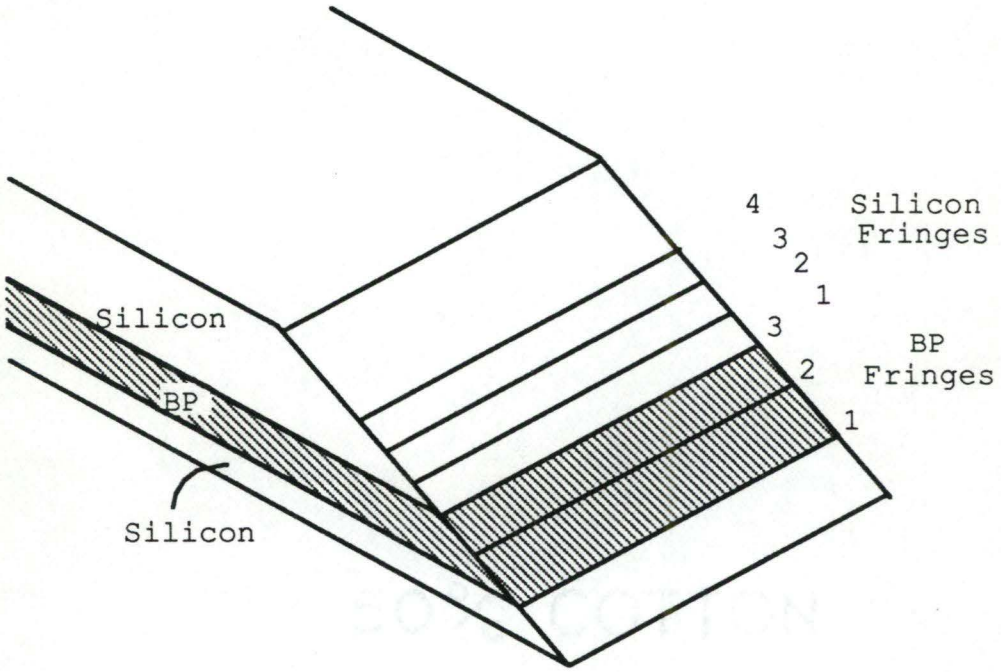


Figure A-1. Measurement of the Lapping Angle.

where

D_{Si} = thickness perpendicular to the dark fringes,

η = refractive index,

n = # of fringes (first fringe occurs where the film thickness is zero),

λ = wavelength of illuminating light.

The lapping angle, Θ, was then calculated by

$$\Theta = \sin^{-1}\left(\frac{D_{Si}}{d}\right) \tag{A-2}$$

where d = distance between the n dark fringes. The magnification, M, of the thickness due to lapping was M = $1/\sin \Theta$.

Since the index of refraction of silicon was known to be 3.42, the silicon layer on top of the BP was used to find the lapping angle, Θ, and magnification factor, M, for each sample. The distance between fringes in the BP, D_{BP}, was measured and substituted into the equation below to find the index of refraction

$$\eta = \frac{\lambda M (n-1)}{2 D_{BP}} \tag{A-3}$$

where the variables have the same meanings as before.

The above procedure was used to find the index of refraction of eight samples from two wafers that had been heated at 1050°C for 30, 60, 90 and 120 minutes. All refractive index data was in the range 2.5 to 3.1 with the exception of two samples which had questionable measured

values of 5.2 and 3.8. No correlation was found between the index of refraction and heat treatment duration. The average index of refraction of the samples (with the exception of the 5.2 and 3.8 cases) was 2.8. This value corresponded closely to previously published values for BP [26].

For this method of in situ film thickness measurement, BP thickness per oscillation, t, was found from the equation

$$t = \frac{\lambda}{2\eta} = \frac{0.9}{2(2.8)} = 0.16\,\mu m/\text{oscillation}. \tag{A-4}$$

In the above equation, λ = peak detectivity of our infrared pyrometer and η = index of refraction of BP as found above. Experimental values were found to be 0.2 μm/oscillation which is approximately the calculated value. The index of refraction has been assumed to be independent of temperature for this calculation.

Appendix B

Horizontal Resistivity Measurements of BP on N^+ Silicon

Introduction

The measurement of horizontal resistivity of the BP layer was complicated by the presence of an n^+ silicon layer below the BP layer. An undoped silicon layer was grown initially to provide a clean surface on which to grow the BP. The silicon was doped n-type with a carrier concentration of around 10^{20} cm^{-3} by the presence of excess phosphorus in the reactor during growth of the BP and silicon films.

Resistivity data taken from BP layers with a four point probe was consistently lower than corresponding vertical resistivity values. It appeared that the underlying n^+ silicon layer had effectively shorted the BP layer. The resultant resistance measured in the BP layer was largely determined by the resistivity of the silicon layer which was found to be at lease an order of magnitude smaller than any of the other parallel layer resistivities. In this Appendix, the problem of making a horizontal resistivity measurement is examined using an equivalent resistance model.

Equivalent Resistance Model

The Si-BP-Si sandwich is schematically shown in Figure B-1. The substrate was p-type 10 Ω-cm silicon covered with a 0.5 μm n-type 0.03 Ω-cm silicon and a 0.5 μm n-type 0.3 Ω-cm

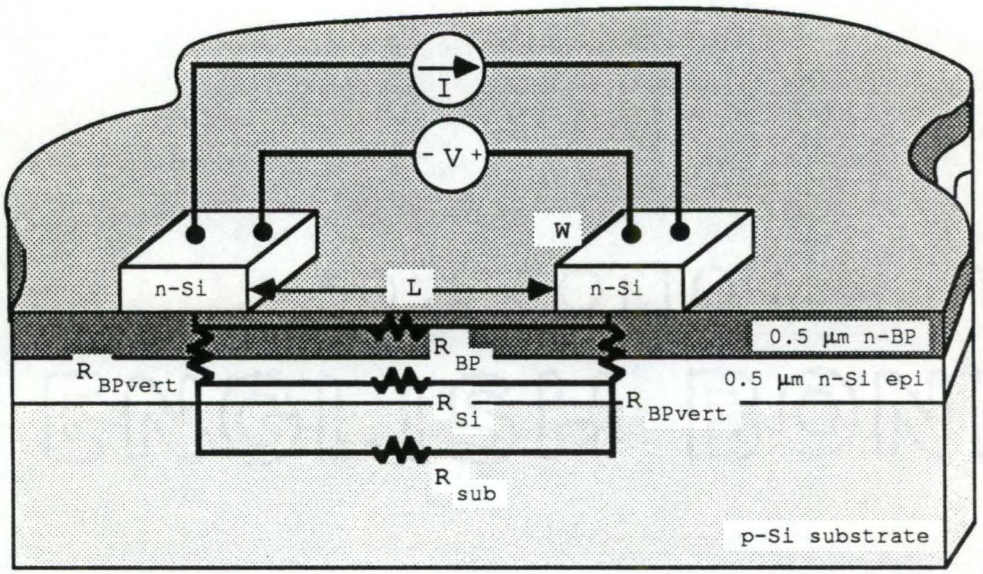


Figure B-1. Equivalent Resistance Model for the Si-BP-Si Sandwich. The horizontal resistance between the two contact pads is essentially the resistance of the n+ silicon layer.

BP layer. A covering silicon layer was etched to produce silicon islands on the BP that were used as contacts. The resistance between the contacts was measured by passing a known current through the layers and measuring the resulting voltage drop.

The proposed electrical model consisted of a network of five resistors. Three horizontal resistors in the BP and silicon epitaxial layers and silicon substrate had approximate dimensions of LxWxt. Two vertical BP resistors under each silicon contact connected the BP and epitaxial silicon resistors.

The substrate resistance can be neglected because it is in parallel with the smaller epitaxial silicon resistor. The measured parallel resistance is then given by

$$R = \frac{1}{\frac{1}{2R_{BPvert} + R_{Si}} + \frac{1}{R_{BP}}} \qquad \text{(B-1)}$$

where R_{BPvert}, R_{Si} and R_{BP} were shown in Figure B-1. The value of W is over one millimeter therefore the ratio $t/WxW < 5x10^{-3}$ cm^{-1}. The vertical resistors were neglected since $R_{BPvert} \ll R_{Si}$.

The model was reduced to two resistors with approximately the same dimensions, LxWxt. Since

$$R = \rho \frac{L}{W t} \qquad \text{(B-2)}$$

it can be shown that the parallel equivalent resistance is proportional to

$$R \propto \frac{\rho_{Si}\,\rho_{BP}}{\rho_{Si} + \rho_{BP}} \qquad \text{(B-3)}$$

where ρ_{Si} and ρ_{BP} were the resistivities of the epitaxial silicon and BP layers respectively. Since $\rho_{BP} \gg \rho_{Si}$, the equivalent resistance seen between the two silicon contacts was approximately equal to the resistance of the epitaxial silicon layer.

The structure of the Si-BP-Si can thus be modeled by a five resistor network. Due to geometry and relative resistivities of the layers, the network can be reduced to a measurement of the resistance of the n^+ epitaxial silicon layer. Thus, measurements of the horizontal resistivity of the BP layer using a four point probe will be shorted by the underlying n^+ silicon layer.

Appendix C

Calculation of the Generation Carrier Lifetime from C-t Measurements

The program "CVPLOT" was modified to include a measurement of capacitance versus time (C-t) of a MOS capacitor using the HP4280A High Frequency C-V Meter. The program supplied all control commands for intializing the measurement and acquiring the data. The five parameters supplied to control the C-t measurement were:

1. Pulse_v,
2. Meas_v,
3. No_read,
4. Pulse_width,
5. Sdelay_t.

Figure C-1 displays the relationship of each parameter to the overall measurement.

The procedure followed for making the C-t measurements was the same as that reported by Heiman [41] and Hofstein [42] but utilizing the rapid interpretation technique reported by Pierret [40]. A more complete theoretical coverage of the lifetime measurement was published by Zechnall and Wermer [43].

Measurements of the C-V and C-t characteristic of a MOS capacitor were made using the "CVPLOT" program. The two data sets were plotted as C/Cox versus voltage where Cox was the oxide capacitance and C/C_F versus time where C_F was the value

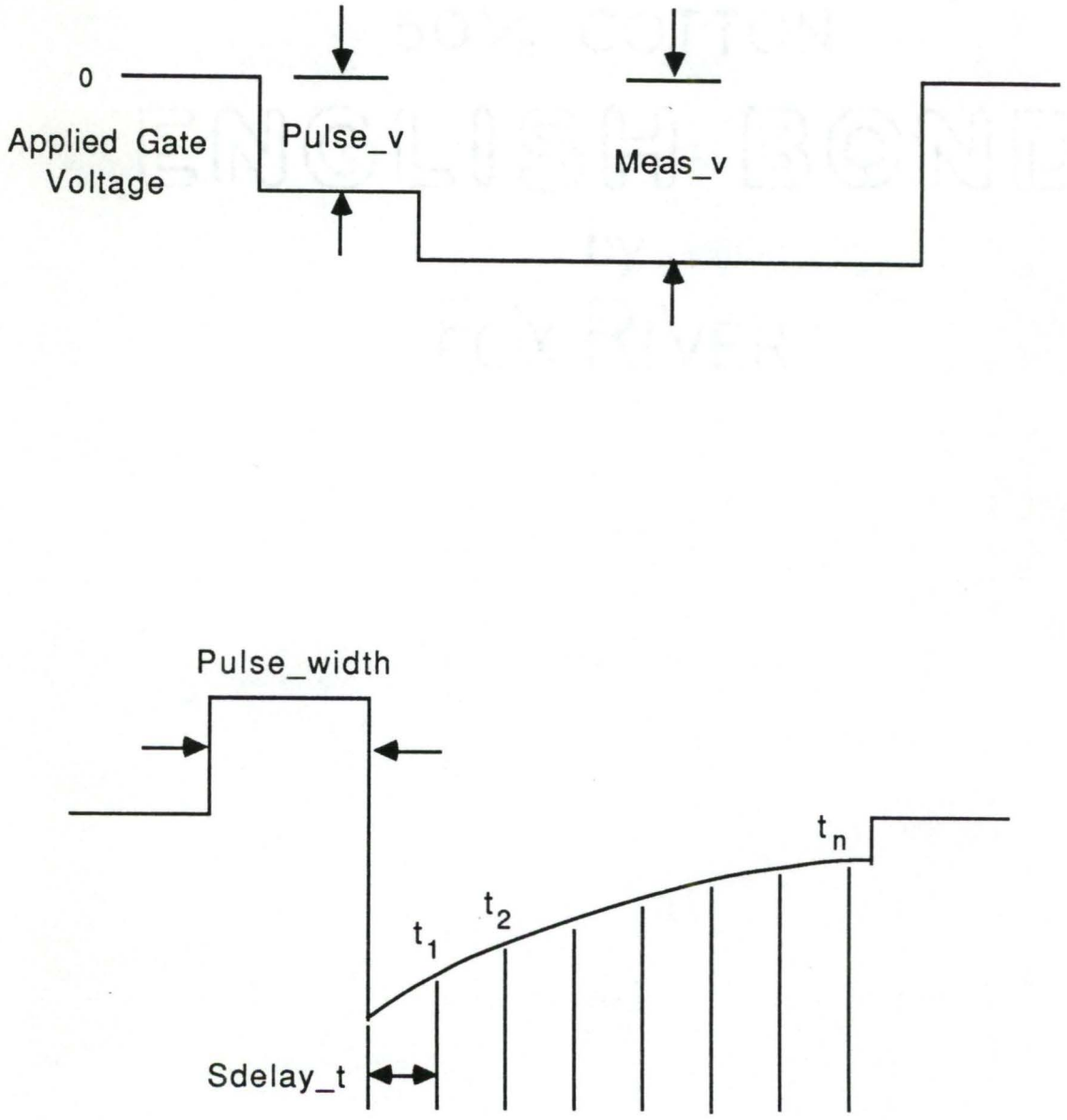


Figure C-1. C-t Measurement Parameters.

of measured capacitance after a long delay time. The actual data for each measurement were listed along with the values for C_F and Cox.

Using the results published by Pierret [40], the delay time, t_o, was linearly interpolated from the C/C_F data as the point corresponding to a value of $C/C_F = 0.67$ (corresponding to $C_F/C(t_o) = 1.5$). Two additional times, t_1 and t_2, were found in a similar manner from C/C_F values of 0.78 and 0.89 respectively. These values were determined from the equations

$$\frac{C(t_1)}{C_F} = \frac{C(t_0)}{C_F} - \frac{1}{3}\left(1 - \frac{C(t_0)}{C_F}\right) \qquad \text{(C-1)}$$

$$\frac{C(t_2)}{C_F} = \frac{C(t_0)}{C_F} - \frac{2}{3}\left(1 - \frac{C(t_0)}{C_F}\right) \qquad \text{(C-2)}$$

where the values for t_1 and t_0 were shown in Figure C-2. Values of $C_F/C(t_0)$ equal to 2.0, 2.5 or 3.0 may be used to better match the linear region of the C-t plot as explained by Pierret [40].

The value for $(t_1-t_0)/(t_2-t_0)$ was calculated and used along with Figure C-3 to find the value of χ. The generation lifetime, T, was then found from the equation

$$T = \frac{t_1 - t_0}{2\,\chi\,(N_B/n_i)(C_{ox}/C_F)} \qquad \text{(C-3)}$$

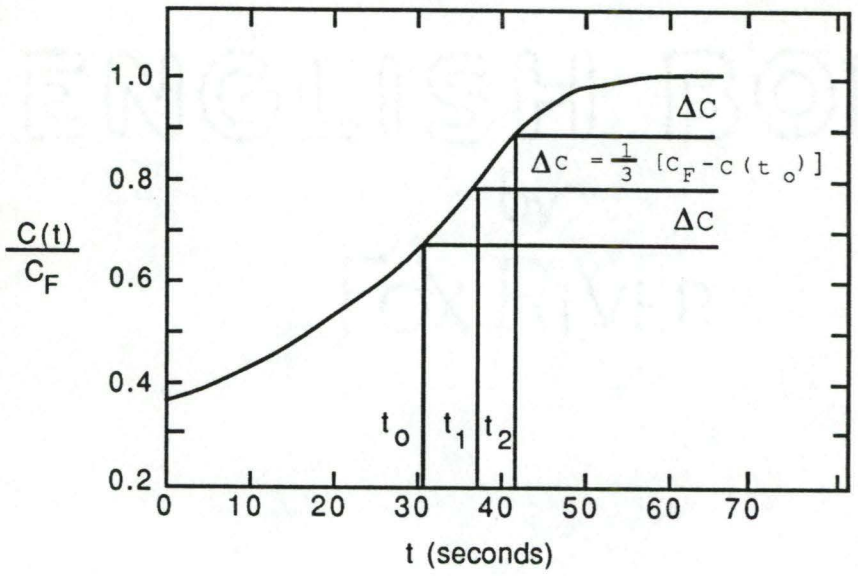


Figure C-2. Sample of C-t Data.

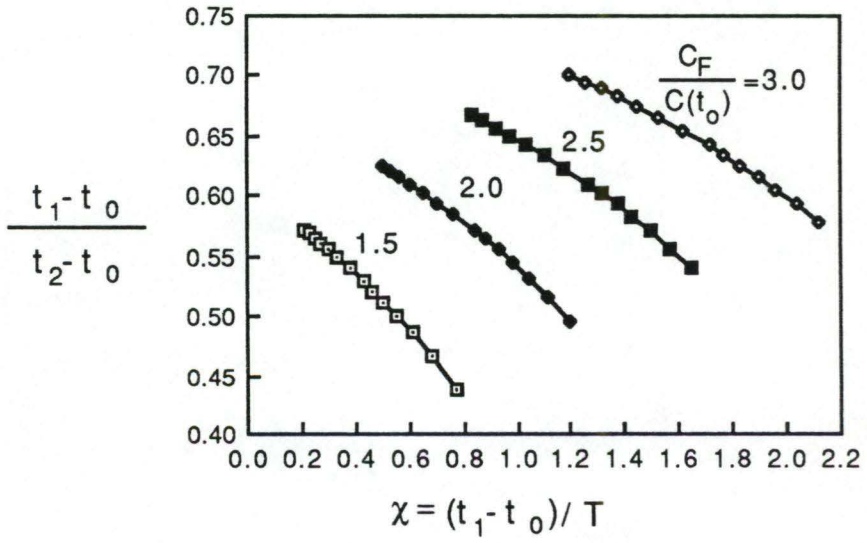


Figure C-3. Plot Used to Determine Generation Lifetime.

where

N_B = background doping concentration,

n_i = intrinsic carrier concentration,

C_{ox} = oxide capacitance.

The actual calculations were not included in the computer program.

Appendix D

Determination of Surface State Density from Quasi-Static C-V Measurements

The computer program "CVPLOT" used the following procedure to derive the surface state density from quasi-static C-V measurements.

The surface state density was given by [37, p. 382]

$$N_{ss} = \frac{C_{ox}}{q}\left[(d\Psi_s/dV_a) - 1\right] - \frac{C_D}{q} \qquad (cm^{-2}eV^{-1}) \tag{D-1}$$

where

C_{ox} = oxide capacitance,

C_D = semiconductor surface capacitance,

V_a = applied voltage,

Ψ_s = surface potential.

Neglecting oxide charges and mobile ionic charges, and given that $dQ = CdV$, it can be shown that

$$\frac{d\Psi_s}{dV} = 1 - \frac{C(V_a)}{C_{ox}} . \tag{D-2}$$

By integrating Equation (D-2), Ψ_S versus V_a was evaluated and used to determine N_{SS}. The surface state density was derived using an iteration process described below.

First, ideal C-V curves were generated given the field plate area, oxide capacitance and doping density. Next, the measured C-V curve was integrated from strong accumulation, V_{acc}, to strong inversion in order to find $\Psi_S(V_a)$ to within a difference, Δ. The surface potential was then given by

$$\Psi_s(V_a) = \int_{Vacc}^{Va} \left[1 - \frac{C(V_a)}{C_{ox}} \right] dV_a + \Delta \,. \tag{D-3}$$

The overall change in surface potential was compared to 1.1 eV to determine if gross nonuniformities existed. Finally, the change in Ψ_s versus V_a was used to determine the surface state density in Equation (D-1).

Appendix E

Derivation of Mobility from MOS Transfer Characteristics

The drain current in an MOS transistor was given by [37, p. 440]

$$I_{ds} = \frac{Z}{L} \mu C_{ox} \left\{ \left(V_{gs} - 2V_b - \frac{V_{ds}}{2} \right) - \frac{2}{3} \frac{2 E_s q N_B}{C_{ox}} \right.$$

$$\left. [(V_{ds} + 2V_b)^{2/3} - (2V_b)^{2/3}] \right\} \qquad \text{(E-1)}$$

where

Z = gate width,

μ = effective mobility,

C_{ox} = gate capacitance per unit area,

L = gate length,

V_{gs} = gate-to-source voltage,

V_b = built-in voltage,

V_{ds} = drain-to-source voltage,

E_s = permittivity of silicon,

N_B = channel doping,

q = electron charge.

Equation (E-1) can be simplified in the linear region to

$$I_{ds} = \frac{Z \mu C_{ox}}{L} (V_{gs} - V_t) V_{ds} \qquad \text{(E-2)}$$

when $V_{ds} < (V_{gs} - V_t)$ where V_t = threshold voltage. By rearranging terms

$$I_{ds} = \left(\frac{Z \mu C_{ox} V_{ds}}{L}\right) V_{gs} - \left(\frac{Z \mu C_{ox} V_{ds}}{L}\right) V_t \qquad \text{(E-3)}$$

where C_{OX} = Es/d, E_S = 1.1x10-12 F/cm and d = thickness of the gate oxide. The slope, M, of the Ids versus Vgs curve can be used to determine mobility as

$$\mu = \frac{M L}{Z C_{ox} V_{ds}} \quad (cm^2/V\text{–}s). \qquad \text{(E-4)}$$

In the saturation region, the drain current is given by the approximation

$$I_{ds} = \frac{Z \mu C_{ox}}{2 L} (V_{gs} - V_t)^2. \qquad \text{(E-5)}$$

By taking the square root of both sides of Equation (E-5), as shown in Equation (E-6),

$$(I_{ds})^{1/2} = \left(\frac{Z \mu C_{ox}}{2 L}\right)^{1/2} (V_{gs} - V_t) \qquad \text{(E-6)}$$

the slope, M, of the square root of the drain current versus gate voltage curve can be used to find the saturation mobility where

$$\mu = \frac{2 M^2 L d}{Z E_s} \quad (cm^2/V\text{–}s). \qquad \text{(E-7)}$$

Appendix F

Measurement Techniques

The measurement of various physical quantities in this dissertation were performed with the utmost care to insure the accuracy of each measurement. Techniques used in these measurements have been described in this Appendix. In each case, data values were presented in a form which represented a conservative number of significant figures. Relative magnitudes of compared data values were maintained throughout.

Temperature Measurement

The temperature of the substrates were measured using an optical pyrometer. The pyrometer was sighted through the water jacket of the quartz reactor tube onto the surface of the hot substrate at a 60° angle.

An infrared pyrometer was used to determine in situ film thickness. The actual temperature of the susceptor was determined by the simultaneous measurement of temperature using both the optical and infrared pyrometers. The infrared pyrometer was sighted through a polished quartz window at the top of the reactor tube at a 90° angle to the surface of the substrate. The emissivity dial was set to .99 for all temperature measurements.

Stated growth temperatures were average values. Often, the rf power setting would drift slightly, changing the

susceptor temperature during the epitaxial growths. These temperature variations were a small percentage of the absolute temperature and made no difference in the final results.

Film Thickness Measurement

Film thickness was measured in situ using the recorded diffraction patterns from the infrared pyrometer. This technique was first reported by Dumin [36] in 1967. The accuracy of this technique was verified using one to five degree angle lappings of representative samples. Film thickness was measured to within ± 0.005 μm.

Resistivity Measurement

Resistivity was measured via four-point probe measurements on the surface of the films. An HP 6920B Meter Calibrator was used as a current source and was set to 0.450 ± 0.001 mA. The voltage drop was measured using a Micronta Digital Multimeter with an accuracy of ± 0.1 mV.

C-V/C-t Measurement

The high frequency C-V data were measured using an HP 4280 1 MHz C Meter/C-V Plotter. Quasi-static C-V and C-t data were measured using an HP 4140B pA Meter/DC Voltage Source. Both of these instruments were controlled via an HP 9000/236 Computer.

MOS Transfer Characteristics

MOS transfer characteristics such as drain-to-source current, Ids, versus drain-to-source voltage, Vds, for a given gate-to-source voltage, Vgs, were measured using an HP 4145A Semiconductor Parameter Analyzer. In addition, Ids versus Vgs, at constant Vds, measurements were performed using the HP 4145A.

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