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Modeling and Tracking Degradation in Electronic Components

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MODELING AND TRACKING DEGRADATION IN ELECTRONIC COMPONENTS

A Dissertation
Presented to
the Graduate School of
Clemson University

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy
Electrical Engineering

by
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December 2017

Accepted by:
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ABSTRACT

This dissertation develops models for electrical components that are useful for describing or predicting their behavior in certain applications. The three models presented are physics-based models that not only describe the behavior, but provide valuable insight as to how the component design relates to the electrical behavior.

In the first chapter of this dissertation, ringing in a power inverter circuit is analyzed and used to track degradation that occurs to the inverter transistors. This is accomplished via the Matrix Pencil Method, which extracts frequency and damping information from the complex poles of a system response. A shift in the pole location of a system response is indicative of transistor degradation.

The second chapter explores modeling multi-layer ceramic capacitors (MLCCs). A simple, accurate model is developed which is based on the physical construction of the capacitor. This model utilizes frequency-dependent resistance terms and mutual inductance to model the frequency-dependent behavior of the capacitor impedance and equivalent series resistance (ESR).

The final chapter studies the contribution of non-linear behavior of MLCCs to the ESR of the capacitor. MLCCs are known to exhibit non-linear behavior in which their capacitance varies with the applied voltage. This causes distortion in the time domain and harmonics in the frequency domain. Power is shifted from the fundamental frequency to harmonics of the fundamental frequency, which will appear as a loss at the fundamental under most circumstances. In some cases, the apparent loss at the fundamental may be comparable to the ESR of the capacitor.

DEDICATION

This dissertation is dedicated to my family, but especially my wife and son.

ACKNOWLEDGMENTS

I would like to thank Dr. Todd Hubing for serving as my advisor and mentor on this long journey. Through Dr. Hubing, I have not only learned about the field of electromagnetic compatibility, but also the foundations of gaining an intuitive knowledge of the topic at hand and having a feeling for the order of magnitude of the solution. Studying under Dr. Hubing was a privilege that I am very grateful for. I hope that I one day have the opportunity to pay it forward.

I would also like to thank the other professors that served on my Ph.D. committee: Drs. Pingshan Wang, Richard Groff, Rod Harrell, and Venkat Krovi. Thank you all for your support and guidance.

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CHAPTER ONE

MONITORING TRANSISTOR DEGRADATION IN POWER INVERTERS THROUGH POLE SHIFTS

Abstract

In a power inverter configuration with pull-up and pull-down transistors, ringing that occurs on the high-to-low and low-to-high transitions can be used to track aging or degradation of the transistors and potentially predict failures. Changes in a transistor's equivalent resistance and capacitance can affect the frequency and damping factor of the characteristic ringing detected on the inverter's output. In this paper, the Matrix Pencil Method is used to locate the poles associated with this ringing and detect shifts in position that indicate transistor degradation.

1.1 Introduction

When an inverter circuit has both pull-up and pull-down transistors, some ringing will occur on both the high-to-low and low-to-high transitions of the output. This ringing is due to the resistance, capacitance, and inductance of a current loop formed by the inverter pair [1]–[3].

As the transistors in the inverter age or are damaged, changes in their capacitance and resistance can cause a change in the frequency and damping of the inverter's characteristic ringing. In [4]–[7], a Fast Fourier Transform (FFT) or Discrete Fourier Transform (DFT) was used to monitor changes in MOSFET frequency responses that would indicate device degradation. While this can be a useful approach for tracking changes in device capacitance, it does not directly provide information on changes in device resistance.

Spread Spectrum Time Domain Reflectometry (SSTDR) is a technique that can be used in-situ to track changes in resistance or capacitance, but it requires its own hardware and an applied signal to ascertain information on the transistor [8]–[10].

Custom on-chip monitoring solutions can provide useful information about device lifetime, especially for integrated MOSFETs, but they require either a customized chip or extra monitoring circuitry added to an existing chip design. Furthermore, these solutions are often specialized to only look for specific modes of device degradation [11]–[13].

An Advanced Gate Drive (AGD) is another approach that facilitates making voltage and current measurements to establish prognostic information; however, this approach requires an advanced gate drive capable of making and reporting measurements of several device voltages and currents [14]–[17].

An FPGA can be configured to monitor discrete transistors in ways analogous to those used in [11]–[17], but one must be available with enough logic to implement such a scheme.

Charge Pumping is yet another method that can track device degradation [18]–[19]; however, it is not performed in-situ and requires monitoring the substrate current, which may not be accessible in all applications.

The Matrix Pencil Method (MPM) is a technique for plotting the pole locations associated with a ringing waveform. The MPM has an advantage of only requiring one voltage or current to be measured. It can then characterize the measured signal in terms of its complex pole locations that contain both frequency and damping information. Shifts in the pole locations can be indications of device degradation.

The ringing characteristics depend on the manner of operation. For example, in Fig. 1.1 when Q1 is on and Q2 is off, the output is in a high state. Turning off Q1 results in a high-to-low transition. A transistor that has been switched on is modeled as the resistance $R_{DS(ON)}$. A transistor that is off is modeled as the series combination of its output capacitance, C_{OSS} , and resistance, R_{OSS} [1], [2]. The lower body diode (LBD) of Q2 is modeled as a current-dependent resistance. When the LBD isn't conducting, its equivalent resistance is very high. When it is conducting, its equivalent resistance is relatively low and is a function of the amount of drain current.

When the circuit of Fig. 1.1 is implemented on a circuit board, the ringing current loop has a finite area resulting in a loop inductance. This loop inductance acts in conjunction with the transistor resistance and capacitance to produce ringing on V_o . If the LBD is still switched on during the low-to-high transition, the series combination of resistance and capacitance of the lower transistor is in parallel with the low LBD impedance. The PWM switching frequency used for the measurements in this study was 5 kHz. Because the LBD was off during the time that ringing occurred, it is not included in the equivalent circuits discussed in the following section. Further details about the effects of the LBD can be found in [20].

1.3 Ringing Equivalent Circuit

A board layout corresponding to the circuit in Fig. 1.1 is shown in Fig. 1.2. A picture of the test bed is provided in Fig. 1.3. While the size of the loop responsible for the ringing inductance is relatively small as implemented in this circuit board, the transistor sockets that facilitated the rapid testing of multiple transistors added a little inductance. The loop inductance with the transistor sockets included was approximately 10 nH.

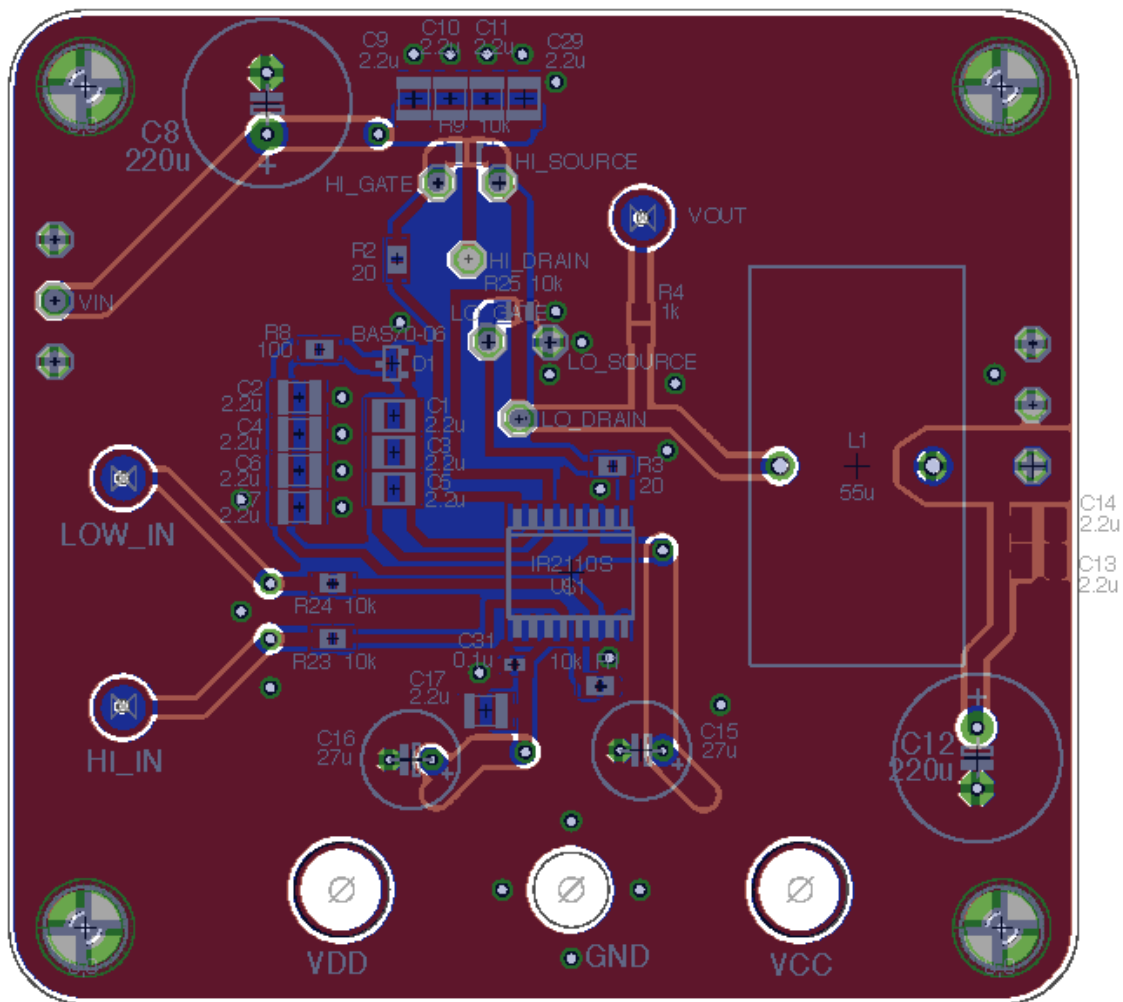


Fig. 1.2. Board layout of MOSFET test bed.

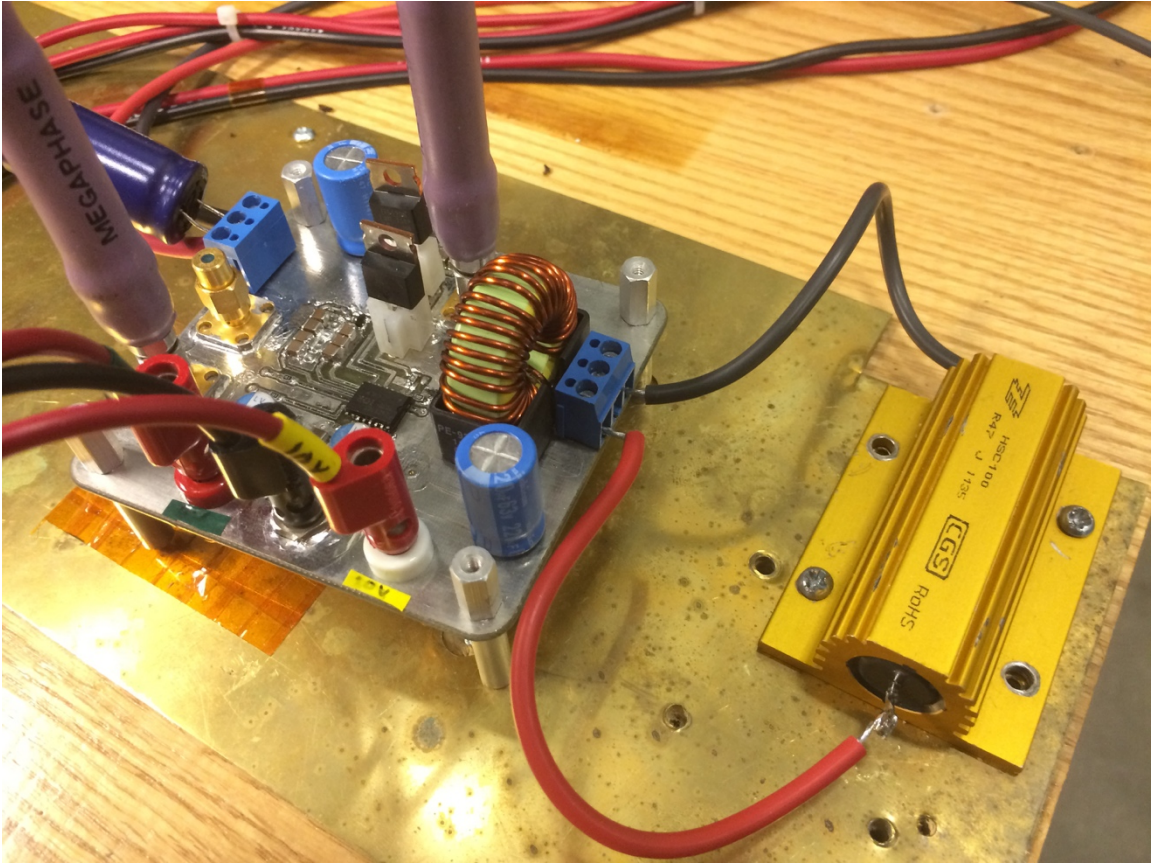


Fig. 1.3. Constructed MOSFET test bed.

While the loop inductance is a very important factor contributing to the ringing, it does not change over time or with transistor degradation. It is also the same for both high-to-low and low-to-high transitions. The equivalent resistance and capacitance of the loop depend on transistor age, damage, operating voltages, and on which transition is monitored. Fig. 1.4 shows the equivalent circuit for a low-to-high transition of V_o .

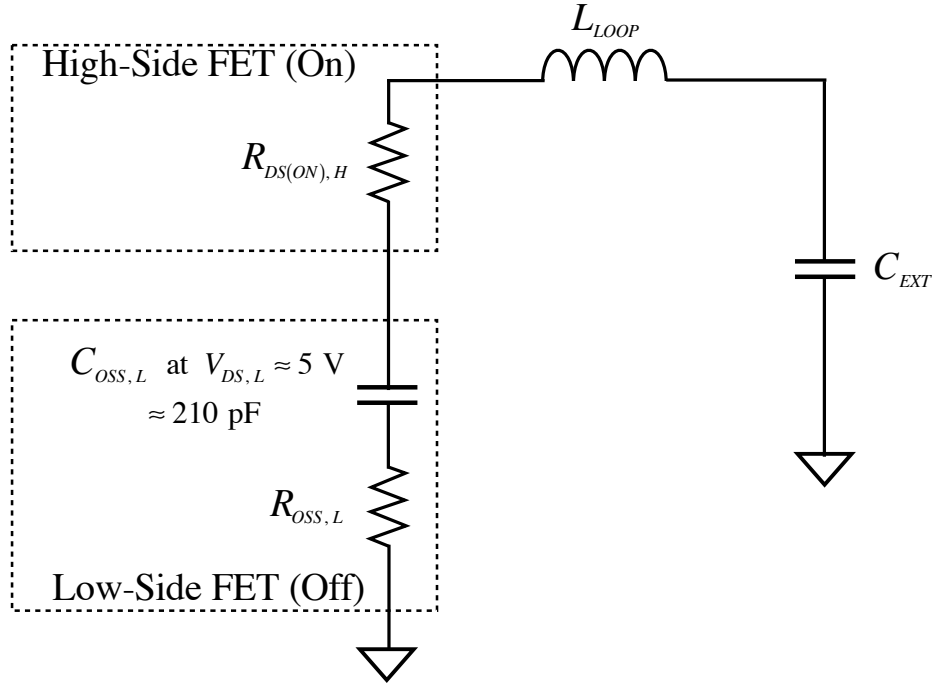


Fig. 1.4. Equivalent circuit for low-to-high transition of inverter output.

For this transition, the high-side transistor is switched on while the low-side transistor remains in its permanent (for this application) off state. The low-side transistor can be modeled as a series R_C . With the chosen PWM period and duty cycle, the LBD was not conducting on the subsequent pulse and the effect of the LBD was neglected. The high-side transistor is on for this transition and can be modeled simply as a resistor. The decoupling capacitance, C_{EXT} , is large compared to C_{OSS} , and since it is in series with C_{OSS} , it can be neglected in most circumstances. C_{OSS} is dependent upon V_{DS} , which is approximately 5 V for the lower transistor on the low-to-high transition. In the case of the low-to-high ringing, the ringing frequency is approximately

$$f_{lh} \approx \frac{1}{2\pi \sqrt{L_{LOOP} \cdot C_{COSS,L} (V_{ds} \approx 5 \text{ V})}} \quad (1)$$

while the damping coefficient can be approximated by

$$\alpha_{th} \approx \frac{R_{DS(ON),H} + R_{OSS,L}}{2L_{LOOP}}. \quad (2)$$

For the high-to-low transition, the equivalent circuit is shown in Fig. 1.5.

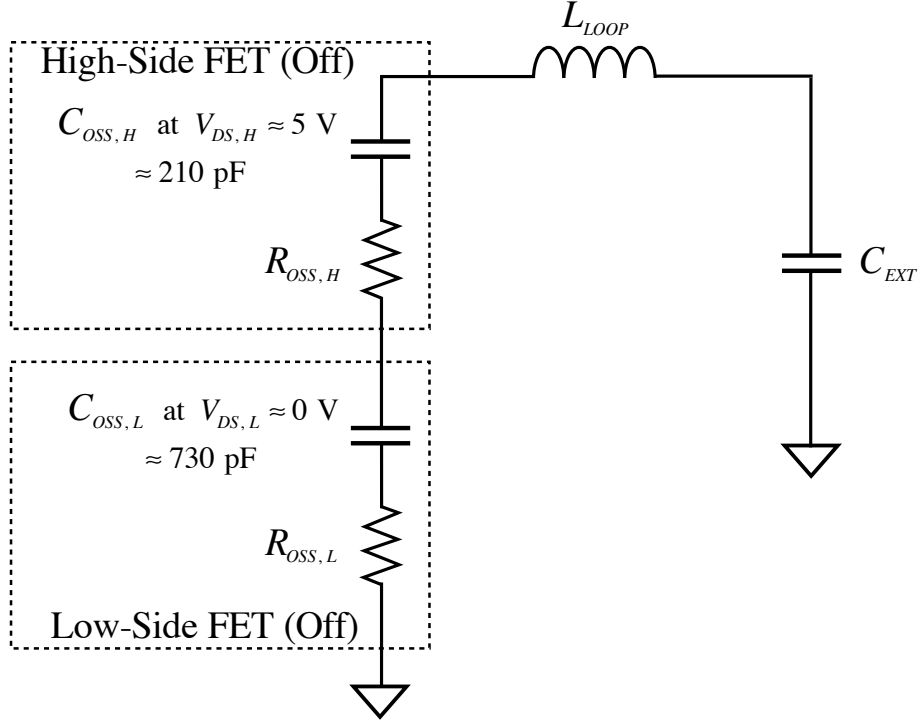


Fig. 1.5. Equivalent circuit for high-to-low transition of inverter output.

As with the low-to-high transition, the low-side transistor can be modeled as a series R_C , neglecting the LBD. Because the high-side transistor is off for this transition, it can also be modeled as a series R_C . For the high-to-low transition, the $V_{DS,L}$ is different than that of the low-to-high transition. This means that the low-side transistor will not have the same equivalent capacitance for both transitions; however, the high-side transistor on the high-to-low transition will have approximately the same equivalent capacitance as the low-side transistor during the low-to-high transition. L_{LOOP} again represents the

equivalent inductance of the loop, and C_{EXT} can be ignored because of its relatively large value. Similar to the low-to-high case, the frequency of the high-to-low transition can be approximated by

$$f_{hl} \approx \frac{1}{2\pi \sqrt{L_{LOOP} \cdot \left[\frac{(C_{OSS,H} (V_{ds} \approx 5V))(C_{OSS,L} (V_{ds} \approx 0V))}{(C_{OSS,H} (V_{ds} \approx 5V)) + (C_{OSS,L} (V_{ds} \approx 0V))} \right]}} \quad (3)$$

and the damping coefficient is approximately

$$\alpha_{hl} \approx \frac{R_{OSS,H} + R_{OSS,L}}{2L_{LOOP}}. \quad (4)$$

1.4 Description of the Matrix Pencil Method

A decaying transient response can be represented by a linear combination of complex exponentials. The Matrix Pencil Method is a technique for extracting the complex poles associated with these waveforms [21]. It is similar to the Pencil of Functions approach, but has improved noise immunity. It also has better performance than the polynomial method [22]. The extracted pole locations indicate both the ringing frequencies and damping factors associated with the spectral components. In the case of complicated systems with multiple resonances, the Matrix Pencil Method is able to extract more than one pole at a time. The exact number of poles that can be extracted is determined by the noise floor, and is closely related to the precision of the measured data.

In our tests, the output voltage of the inverter circuit was recorded with a 21:1 probe connected to the 50- Ω input of an oscilloscope. The signal was digitized and processed in Matlab. The captured waveforms were windowed and filtered before the matrix pencil method was applied to calculate the complex poles. Some of the poles

extracted were due to noise and slight, low frequency variations in the waveform. Based on the estimated resistance, capacitance, and inductance of the ringing current loop, the main pole of interest was separated from the rest. The real part of the pole represents its damping factor, while the imaginary part represents its ringing frequency.

The plot in Fig. 1.6 shows an output voltage waveform from the test bed in Fig. 1.3 when an unaged transistor was placed in the high-side transistor socket. The PWM used to drive the circuit had a period of $200\ \mu\text{s}$ and a 3% duty cycle. Fig. 1.6 shows a spike in V_o at roughly $50\ \mu\text{s}$, when the LBD stops conducting, which is before the subsequent pulse.

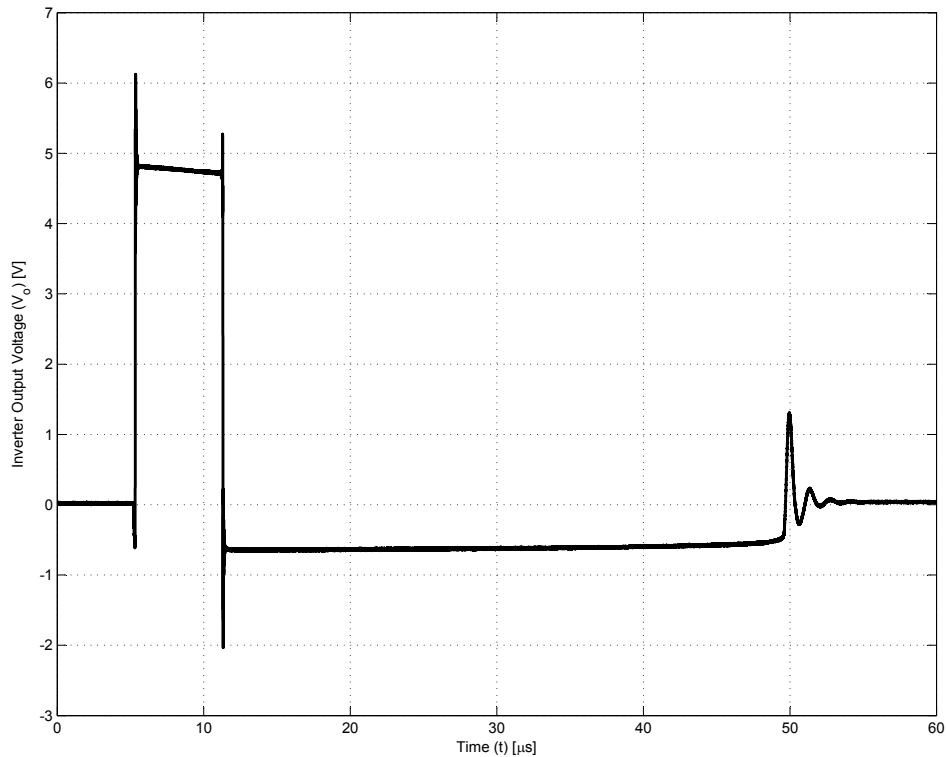


Fig. 1.6. Output voltage of the inverter test bed for an undamaged transistor.

Fig. 1.7a shows a zoomed-in view of the ringing after the low-to-high transition in Fig. 1.6, while Fig. 1.7b shows a zoomed-in view of the ringing after the high-to-low transition.

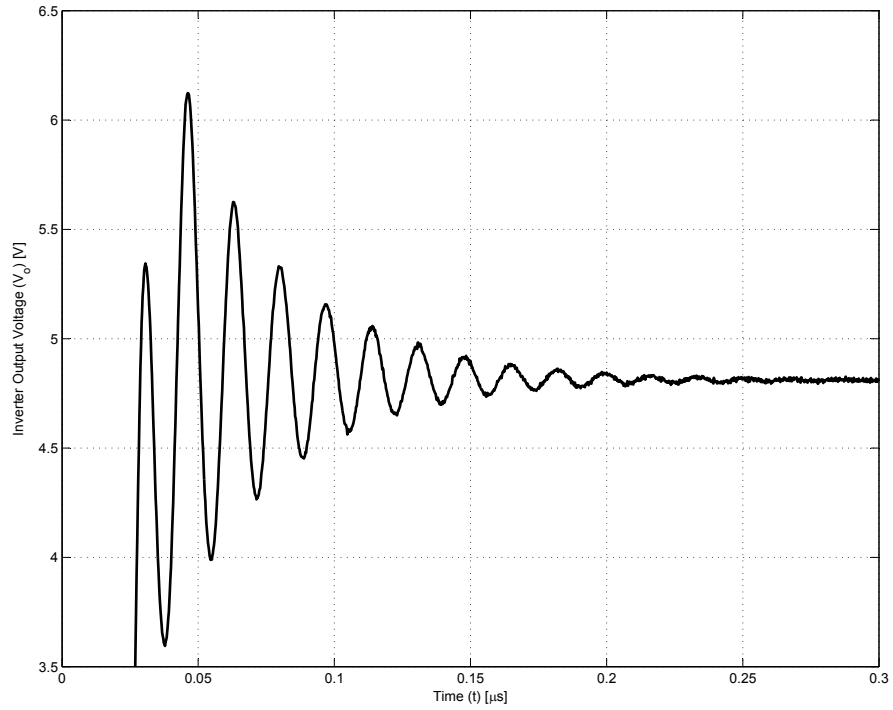


Fig. 1.7a. Low-to-high ringing of an undamaged transistor.

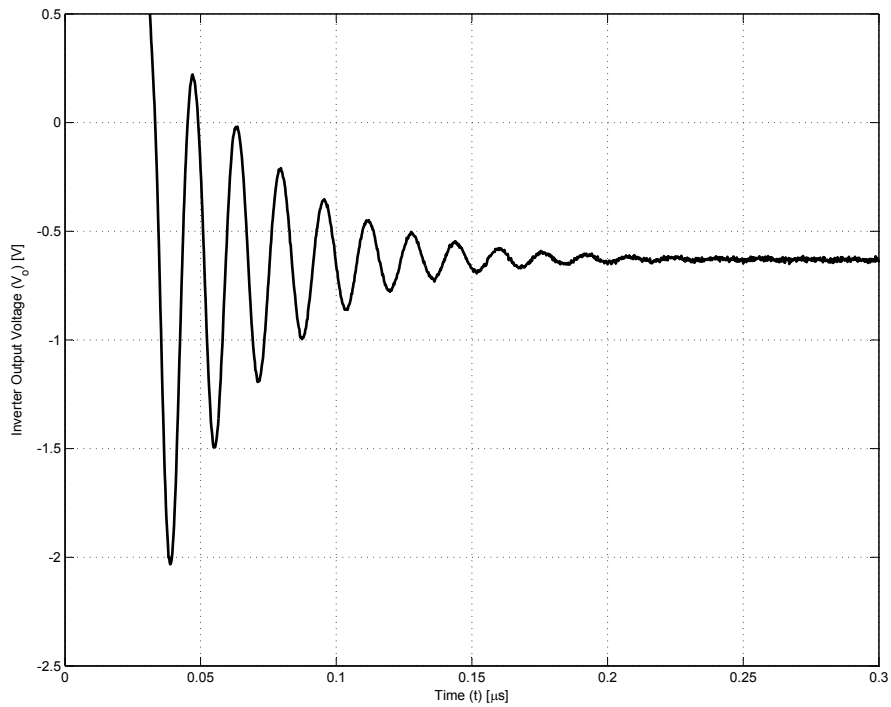


Fig. 1.7b. High-to-low ringing of an undamaged transistor.

The ringing waveforms in Figs. 1.7a and 1.7b were recorded and processed with the MPM. Fig. 1.8a shows the main pole of interest from the low-to-high transition, and Fig. 1.8b shows the main pole of the high-to-low transition. Note that the ringing characteristics in Figs. 1.7a and 1.7b are different due to differing equivalent circuits for each transition of the inverter output.

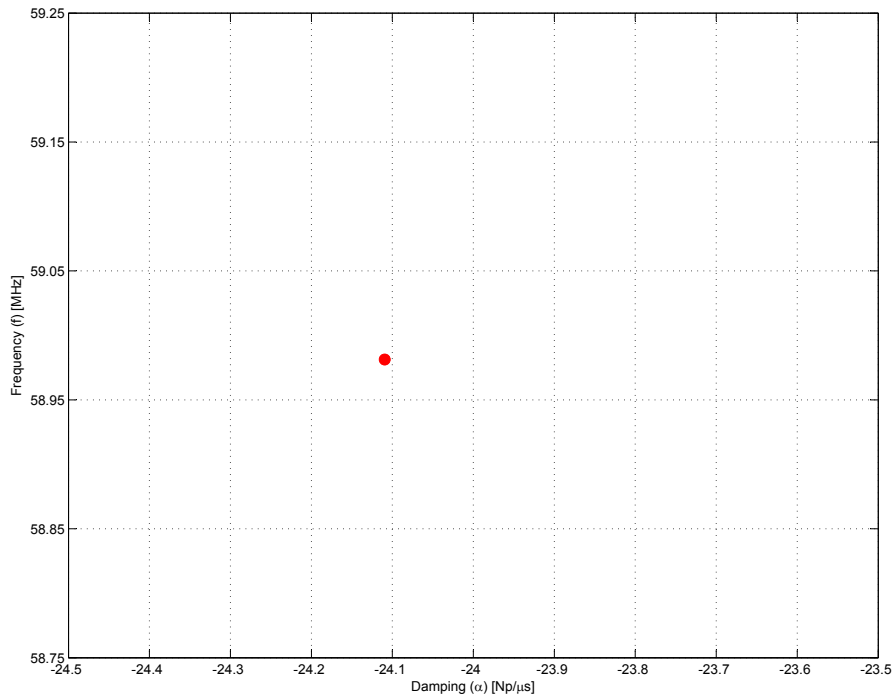


Fig. 1.8a. MPM pole of the low-to-high ringing of an undamaged transistor.

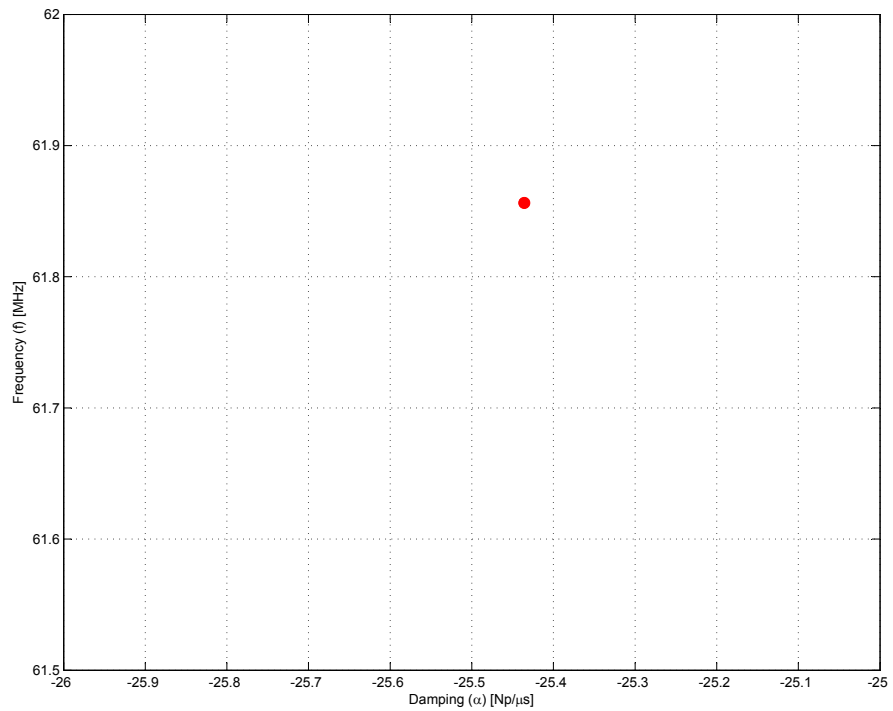


Fig. 1.8b. MPM pole of the high-to-low ringing of an undamaged transistor.

1.5 Method of Artificially Aging Transistors

There are many different methods that can be used to artificially age transistors. Transistors can be subjected to a variety of stresses, including rapid thermal cycling, overvoltage (including ESD), and overcurrent. Simulating an ESD event replicates a real-world occurrence that can degrade or even destroy a MOSFET. By tweaking the method of discharge, voltage, and number of discharge events, MOSFET transistors can be effectively degraded but not destroyed.



Fig. 1.9. Setup used to perform ESD degradation of MOSFET transistors.

The setup used in this work to degrade MOSFETs is shown in Fig. 1.9. The ESD simulator was a Kikusui KES4021. The transistor was placed with its tab contacting a

grounded metal table top. The contact discharge tip was placed on the discharge gun, which was placed in a stand on the table. The contact tip was placed in the center of the epoxy package, and 4 pulses at 20 kV were applied to the transistor. This procedure was generally found to provide enough degradation to be detectable without destroying the transistor. There is an inherent amount of inconsistency with the ESD event in this process. Slight misalignment of the discharge tip from the center of the package could cause the discharge to either be more or less destructive than desired.

1.6 Measuring Drain Leakage Current and Threshold Voltage

In order to confirm that transistor degradation had occurred, the drain-to-source leakage current of each transistor was measured before and after ESD degradation. To measure the drain leakage current, a drain-to-source bias voltage was applied to the transistor. This voltage was determined by measuring the drain-to-source voltage of the transistor in situ in the test bed circuit. For the high-side transistor, the bias voltage was approximately 5.7 VDC. With this bias applied, the gate was shorted to the source, and the amount of drain current was measured. The schematic for this setup is shown in Fig. 1.10. By measuring the voltage across the 1-k Ω resistor, the drain leakage current was able to be determined.

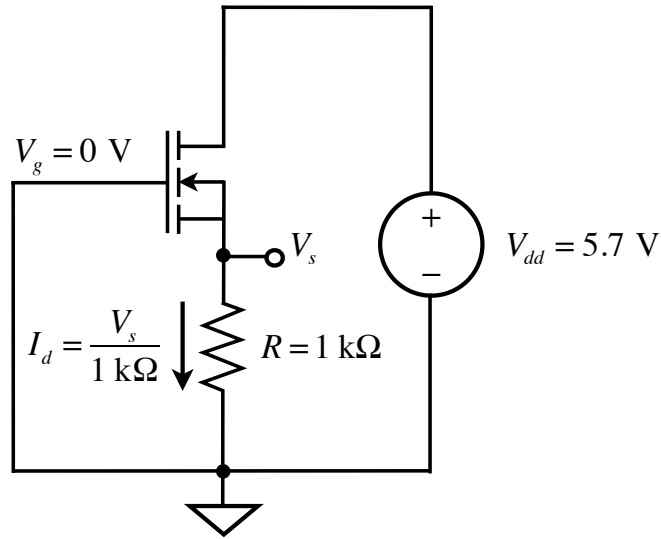


Fig. 1.10. Drain leakage current measurement schematic.

The threshold voltage of each transistor was also measured before and after ESD degradation. This measurement was performed as described in the datasheet for the IRF520NPbF [23]. The gate of the transistor was shorted to the drain, while a gate-to-source voltage was applied. As this gate-to-source voltage increased, the threshold voltage was defined as the gate-to-source voltage at which the drain current reached 250 μ A. Fig. 1.11 shows the schematic for making threshold voltage measurements. The drain current was again determined by measuring the voltage across the 1-k Ω resistor.

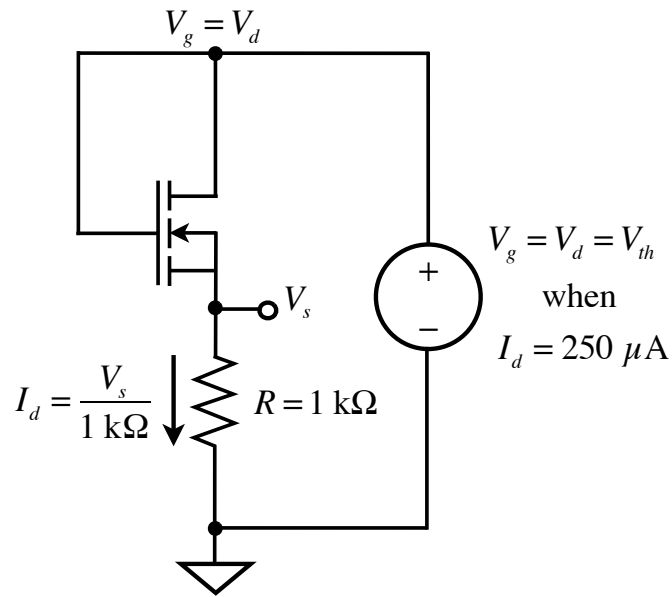


Fig. 1.11. Threshold voltage measurement schematic.

It should be noted that the threshold voltage determined by the setup shown in Fig. 1.11 is not the exact threshold voltage of the transistor, but it provides a voltage that is well correlated to the actual threshold voltage.

Table 1.1 below shows the drain leakage current before and after ESD degradation. Note that the noise floor for these current measurements was $1 \mu\text{A}$, but all undamaged transistors measured below this threshold.

Table 1.1. Change in drain leakage current due to ESD degradation.

Transistor	Survive ESD?	Drain Leakage Current Before ESD	Drain Leakage Current After ESD
T1	No	< 1 μ A	1.5 mA
T2	Yes	< 1 μ A	1.3 mA
T3	Yes	< 1 μ A	1.3 mA
T4	No	< 1 μ A	4.9 mA
T5	Yes	< 1 μ A	1.1 mA
T6	Yes	< 1 μ A	2.2 mA
T7	Yes	< 1 μ A	2.2 mA
T8	Yes	< 1 μ A	920 μ A
T9	Yes	< 1 μ A	1.4 mA
T10	No	< 1 μ A	1.5 mA

As indicated in Table 1.1, the drain leakage current of all transistors increased after ESD degradation. Transistors T1 and T4 did not survive the degradation, meaning that they no longer functioned when placed in the test bed. Table 1.2 shows the threshold voltage before and after ESD degradation.

Table 1.2. Change in threshold voltage due to ESD degradation.

Transistor	Survive ESD?	Threshold Voltage Before ESD	Threshold Voltage After ESD
T1	No	3.7 V	700 mV
T2	Yes	3.7 V	700 mV
T3	Yes	3.7 V	800 mV
T4	No	4.7 V	300 mV
T5	Yes	4.9 V	900 mV
T6	Yes	4.6 V	3.5 V
T7	Yes	4.9 V	3.7 V
T8	Yes	4.5 V	1.1 V
T9	Yes	4.8 V	700 mV
T10	Yes	4.6 V	800 mV

As indicated in Table 1.2, all transistors suffered a decrease in threshold voltage after degradation. While most transistors showed an appreciable decrease in threshold

voltage, T6 and T7 did not decrease as much as the rest, and their threshold voltages remained close to that of undamaged transistors.

1.7 Pole Shifts Due to Transistor Degradation

To evaluate changes in the ringing waveform due to transistor degradation, each of the ten transistors were placed in the test bed before ESD degradation and operated for five minutes before their pole location was determined. Next, the transistors were subjected to ESD degradation as described in Section 1.5. The transistors were then placed back in the test bed. If they still operated, their pole locations were again determined. Ringing on the output voltage from a typical ESD degraded transistor is shown in Figs. 1.12a and 1.12b.

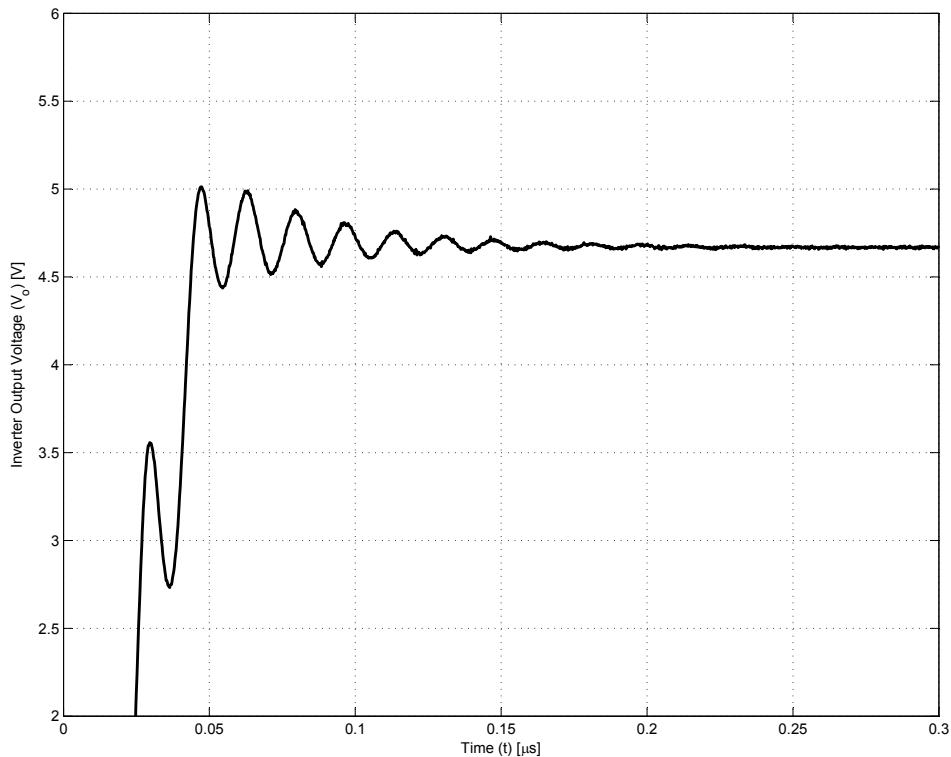


Fig. 1.12a. Low-to-high ringing of transistor after ESD degradation.

Fig. 1.12a shows the low-to-high transition of the inverter output voltage, while Fig. 1.12b shows the high-to-low transition of V_o .

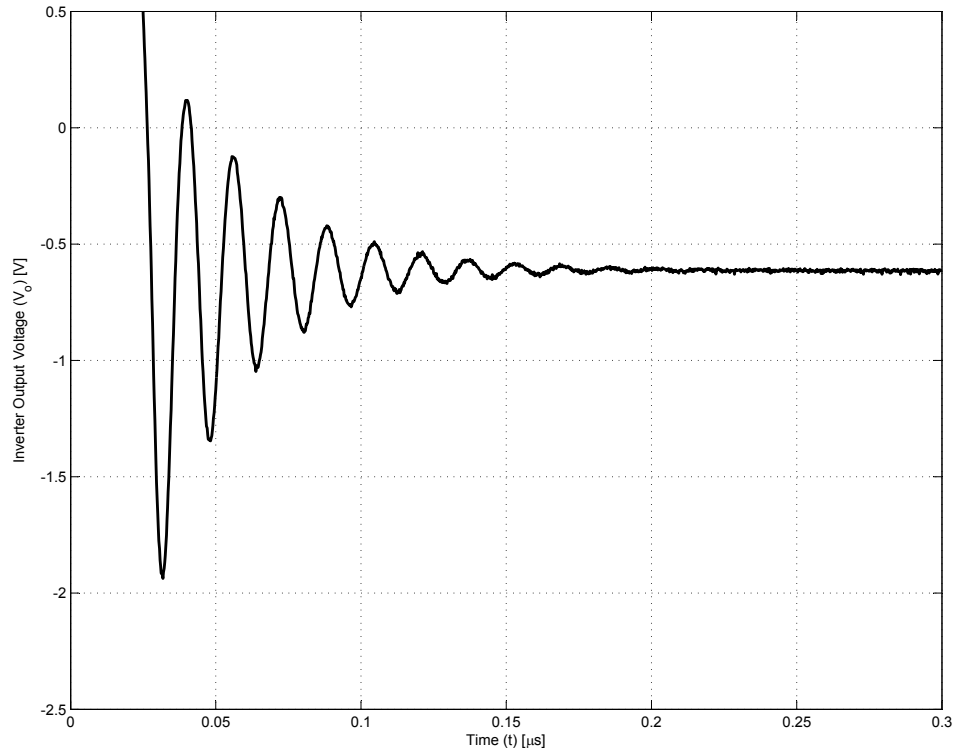


Fig. 1.12b. High-to-low ringing of transistor after ESD degradation.

When comparing the time-domain ringing waveforms before and after ESD degradation, a clear difference in the waveforms from Figs. 1.7a,b and Figs. 1.12a,b can be seen. A plot of both unaged and aged pole locations for the transistors in Tables 1.1 and 1.2 is shown in Fig. 1.13. Since the high-side transistor was subjected to degradation, only the high-to-low ringing was monitored. Again, note that two of these transistors did not survive ESD degradation. The pole locations corresponding to those transistors are only shown for the undamaged case.

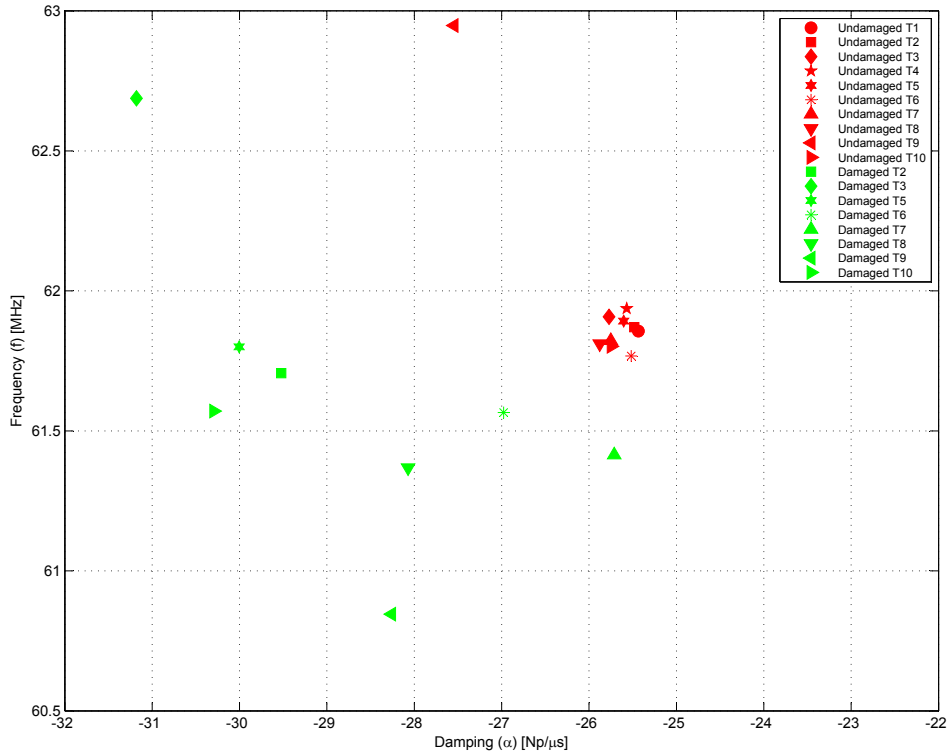


Fig. 1.13. MPM poles of ten transistors before and after ESD degradation.

From Fig. 1.13, it is clear that the ESD degradation had a negligible effect on the ringing frequency, but most transistors exhibited a measurable increase in damping after degradation. Comparing the results of Table 1.1 to the poles of Fig. 1.13, no clear trend can be seen between drain leakage current and pole shifts; however, when comparing threshold voltage changes from Table 1.2 to the pole shifts of Fig. 1.13, a more clear relationship is observed. The transistors that demonstrated an increase in damping also suffered a noticeable decrease in threshold voltage after ESD degradation. Those that had very little increase in damping did not show a significant change in the measured threshold voltage.

According to (1.4), an increase in damping corresponds to an increase in the series resistance, R_{OSS} , of the damaged transistor. From (1.3), the insignificant change in

frequency indicates that there was very little change in the capacitance, C_{OSS} , of these transistors when they were damaged.

1.8 Conclusion

As a MOSFET transistor ages or becomes damaged, changes can occur that will affect the equivalent resistances and capacitances of the transistor. This paper demonstrates how the Matrix Pencil Method can be used to plot the pole locations associated with the ringing on the outputs of transistors in a power inverter.

In this study, MOSFETs degraded by ESD exhibited significant shifts in the location of their primary poles.

After degradation, the poles shifted to the left, indicating an increase in damping, but there was no significant change in frequency. This increase corresponds to an increase in the high-side R_{OSS} and no change in the high-side C_{OSS} . While the ESD did not change C_{OSS} in this case, there are other processes that can degrade the C_{OSS} of a MOSFET and potentially cause the ringing frequency to shift. If normal aging or device degradation cause changes in either of these parameters, these changes can be detected as a shift in extracted pole locations.

In this study, the increase in damping corresponded to a decrease in the measured threshold voltage. While there was an increase in drain leakage current after ESD degradation, no clear linear relationship between pole shifts and changes in drain leakage were observed. An increase in leakage current was always accompanied by an increase in damping, but higher leakage current did not necessarily accompany a more damped pole location.

While damping information can be extracted from an FFT, the MPM provides accurate values of the damping coefficient directly. Through examination of the pole shifts in Fig. 1.13, there was on average an 11% increase in damping and a 0.6% decrease in frequency after the ESD aging.

The measurements described in this paper can be performed on switching transistors while they are operating normally. This approach can be used to monitor the health of power inverters without disrupting the operation of the systems that employ them.

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CHAPTER TWO

MODELING A MULTI-LAYER CERAMIC CAPACITOR WITH LOSSES BASED ON PHYSICAL PHENOMENA

Abstract

Multi-layer ceramic capacitors (MLCCs) in surface-mount packages are generally composed of a number of conducting plates stacked vertically. At high frequencies, when mounted on a printed circuit board, most of the current will only flow in the lower plates. The capacitor can be thought of as having a low-frequency equivalent circuit and a high-frequency equivalent circuit. Losses at lower frequencies are dominated by the dielectric. Losses at higher frequencies are dominated by skin effect losses in the electrodes. An eight-element circuit is proposed that models the behavior of surface-mount MLCCs over a wide band of frequencies.

2.1 Introduction

It can be beneficial to have access to a fast, accurate model of a multi-layer ceramic capacitor (MLCC). To better understand the behavior of a circuit utilizing an MLCC, the model of the MLCC should be based on what is physically happening in the body of the capacitor.

An MLCC can be difficult to model accurately because the effective resistance, capacitance, and inductance of the capacitor will vary with frequency [1]. Also, the internal inductance of the capacitor cannot be determined independently from the connection geometry.

Over the years, many models of MLCCs have been developed. Perhaps, the most common MLCC model is the series RLC circuit shown in Fig. 2.1. This model is commonly found in textbooks and capacitor datasheets.

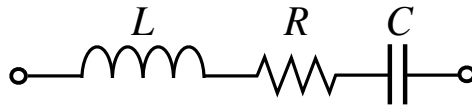


Fig. 2.1. Simple RLC model.

The resistance in this model is referred to as the equivalent series resistance (ESR) of the capacitor, while the inductance represents the equivalent series inductance (ESL). The capacitance in this model is generally the nominal capacitance of the capacitor [2]–[3].

To increase the accuracy of the series RLC model, a resistance in parallel with the capacitance, which models the dielectric losses of the capacitor, is sometimes added [2]–[3]. This model is shown in Fig. 2.2, and will be referred to as an RLCR model.

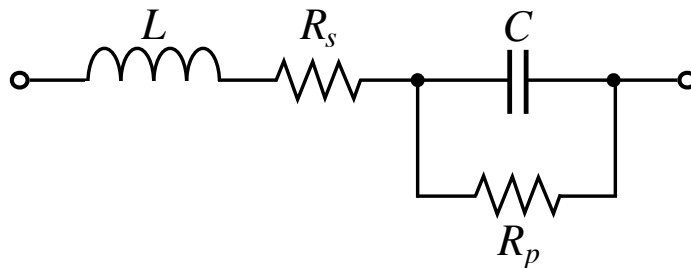


Fig. 2.2. RLC model with added parallel R.

These models do a good job of modeling the gross behavior of MLCCs, but their accuracy is limited. The optimum value of each element in these models is frequency dependent. The model shown in Fig. 2.3 [4]–[6] adds additional elements to the RLC model in an attempt to increase the accuracy of the model over a wide range of

frequencies. These added parameter values are generally determined through curve-fitting to match measured data. This yields a very accurate model that is more complex than the RLC or RLCR models. Since the structure of the model is not based on the physical properties of the capacitor, this type of model is generally only useful for modeling the specific capacitor that was measured.

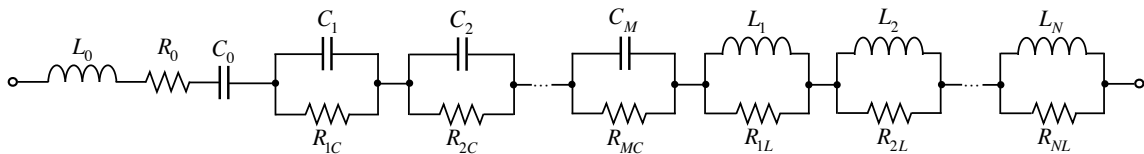


Fig. 2.3. Curve-fit model of MLCC.

Fig. 2.4 shows a model developed by a capacitor manufacturer. This model is similar to the curve-fitted models discussed above, but is much closer to representing the physical construction of the MLCC. In this model, there are many parallel RC branches mimicking the plate pairs of an MLC capacitor [7].

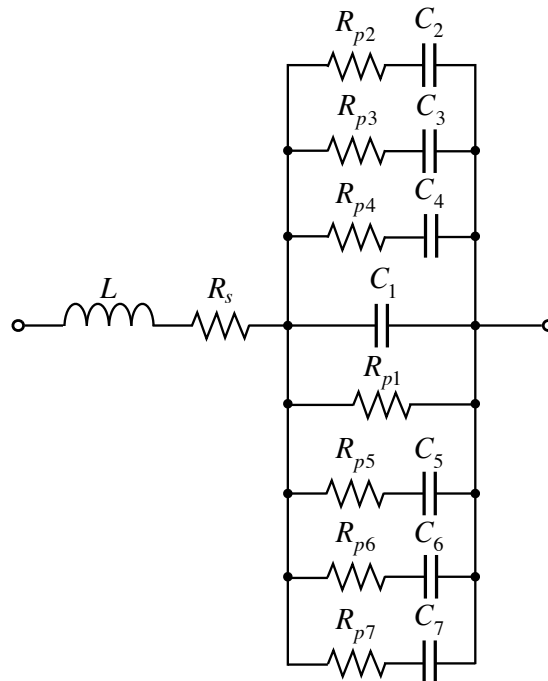


Fig. 2.4. Model developed by capacitor manufacturer.

Prymak developed the model of Fig. 2.5 and several derivatives for KEMET in [6], [8]–[9].

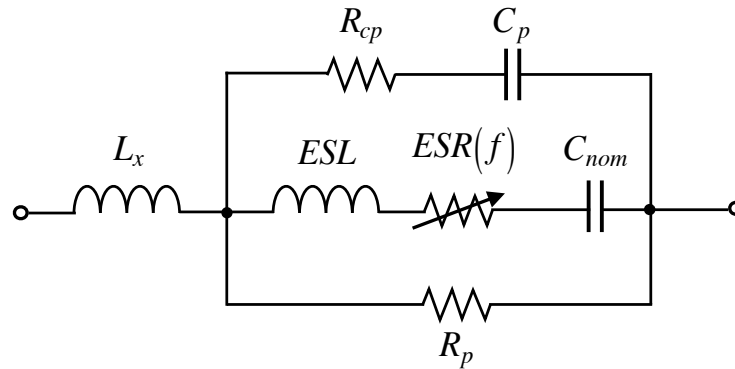


Fig. 2.5. Prymak MLCC model.

This model is also based on the physical construction of the capacitor. Furthermore, it accounts for the frequency dependence of the resistance term, but the dependence is fit rather than attributed to any physical phenomena.

The model presented in Fig. 2.6 was developed by Smith and Hockanson in [10]–[11], and represents the stacked plate pairs of the MLCC. In the instance of the particular model shown in Fig. 2.6, the modeled capacitor contains ten plate pairs.

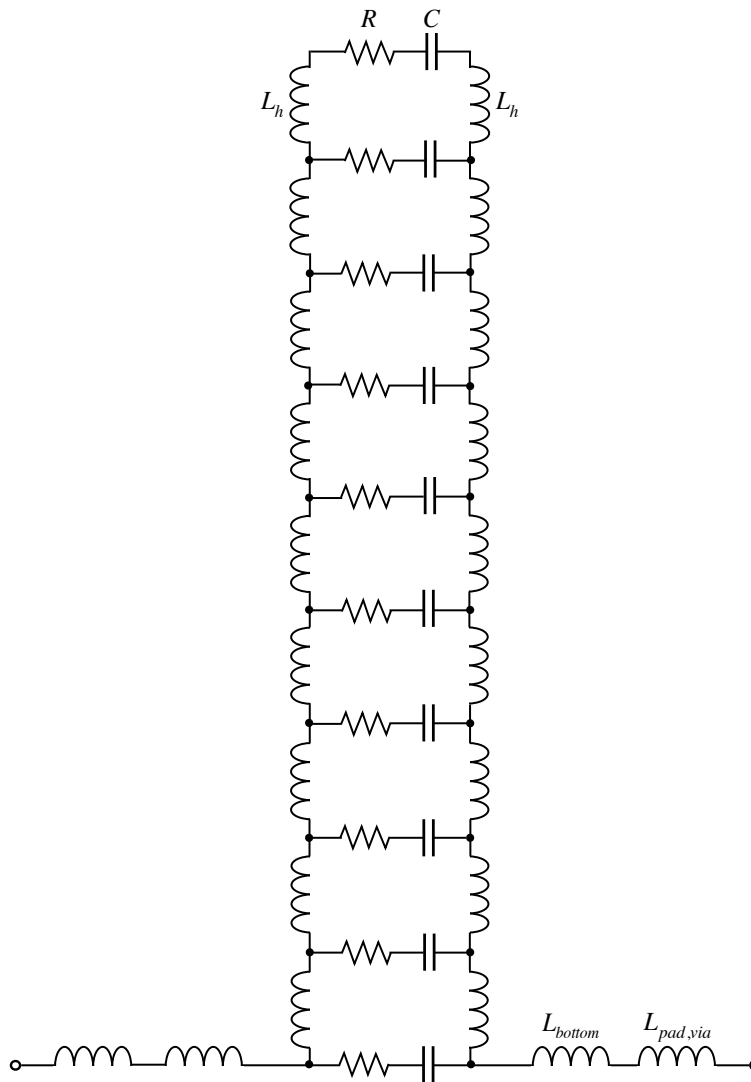


Fig. 2.6. Smith-Hockanson MLCC model.

The model above uses parallel RC branches interconnected with inductance terms to model the plates of the capacitor. For every plate pair in the capacitor, there is an RC branch in the model. The inductance terms represent the partial inductances associated with getting current to the subsequent plate. Each branch uses the same parameter values, because each plate of the capacitor has essentially the same geometry. The Smith-

Hockanson model is based on the physical construction of the capacitor and is more accurate than the RLC or RLCR models; however, it is more complex.

Somewhat of a simplification of the models from [10]–[11], the model of [12], shown in Fig. 2.7, uses three RLC branches to model the MLCC. The authors show that a three-branch model provides improved accuracy over the single-branch RLC model without adding a large amount of complexity.

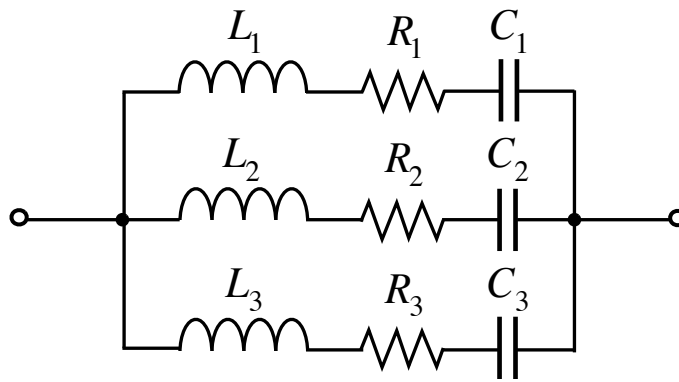


Fig. 2.7. Three-branch MLCC model.

The model proposed in this paper more accurately describes the physical phenomena of an MLC capacitor. It is accurate over a broader frequency range than the simple models from [2]–[3], achieves this accuracy with minimal added complexity, and is simpler than many of the models proposed in [4]–[12].

2.2 Model Features

At low-frequencies, current will flow equally in all the plates of an MLCC; however it has been demonstrated in [13]–[15] that most of the high-frequency current in an MLCC flows on the lower plates of the capacitor when the current enters and exits the package from below. The transition occurs at frequencies where the impedance at the terminals of the capacitor is dominated by the inductance of the current path. Fig. 2.8

illustrates the paths that currents in a standard-electrode MLCC take at low and high frequencies.

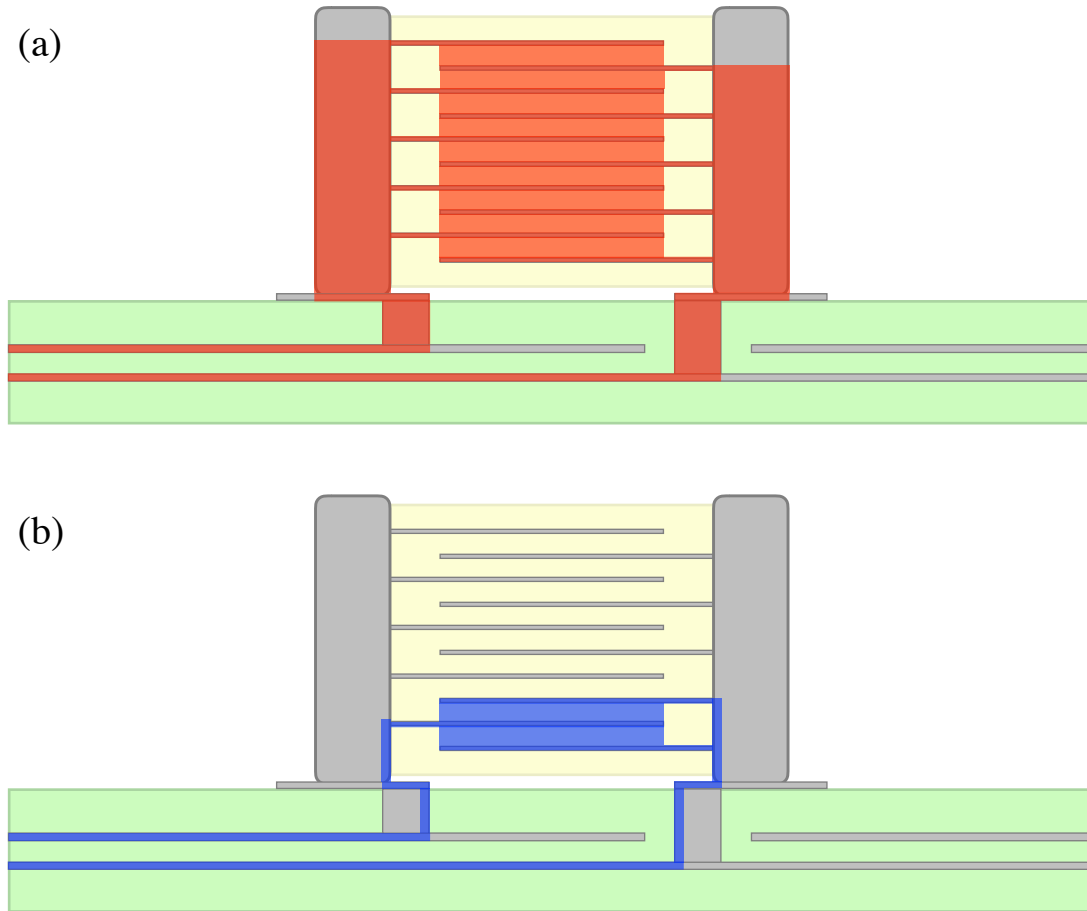


Fig. 2.8. Current path in a standard electrode MLCC at low frequencies (a) and high frequencies (b).

Another common configuration of MLCC is the floating-electrode design. Fig. 2.9 illustrates the current paths in a floating electrode MLCC at low and high frequencies. For capacitors with the same physical size and number of plate pairs, the electrode design will have an effect on the capacitor equivalent circuit parameters.

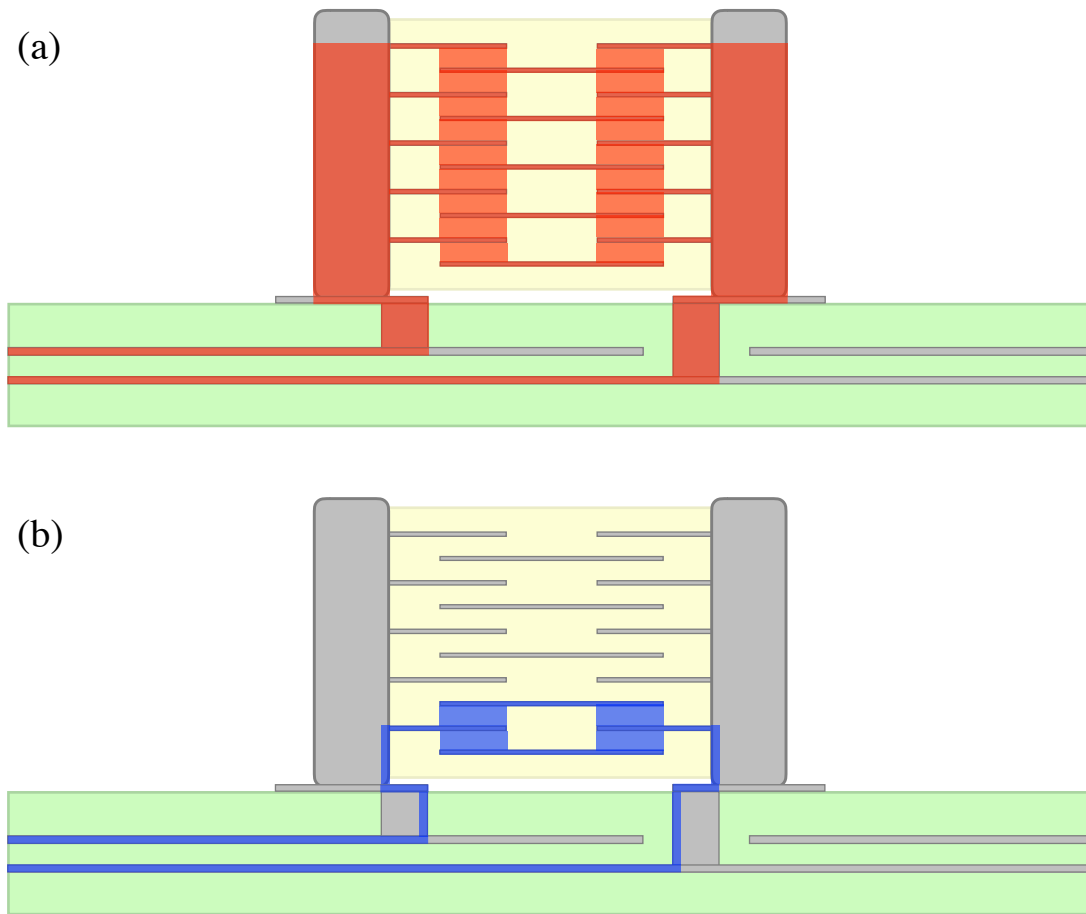


Fig. 2.9. Current path in a floating electrode MLCC at low frequencies (a) and high frequencies (b).

The proposed model for surface mount MLCCs has two branches: one branch represents an equivalent circuit at low frequencies, while the other branch represents the equivalent circuit at high frequencies. Together, the two branches model the MLCC over a broad frequency range. For ease of understanding, the branches will be referred to as the low-frequency branch and the high-frequency branch, respectively. For clarity, let the “self-resonant” frequency be defined as the frequency at which the primary LC resonance between the connection inductance and the nominal capacitance occurs.

The low-frequency branch is comprised of a series RLC circuit with a frequency-dependent resistance term. This resistance varies inversely with frequency and represents the dielectric losses, which are the dominant losses in an MLCC at lower frequencies [16]–[18]. The capacitance in the low-frequency branch will be a majority of the nominal capacitance, as it represents the capacitance of the plates that are not “seen” by high-frequency current. The inductance term of the low-frequency branch characterizes the inductance associated with the current path shown in Figs. 2.8a or 2.9a, depending on the capacitor electrode construction.

The high-frequency branch similarly consists of a series RLC circuit with a frequency-dependent series resistance term; however, the resistance term in this branch is proportional to the square root of frequency. This resistance simulates the skin effect losses of the plates, which are the dominant losses in the capacitor at high frequencies [16]–[17]. The capacitance of the high-frequency branch will be the capacitance of only one or two layers of the capacitor, since these are the layers that will carry the majority of the high-frequency current. The inductance of the high-frequency branch is that of the current path shown in Figs. 2.8b or 2.9b. The high-frequency inductance will be smaller than the low-frequency inductance due to the smaller loop area associated with the high-frequency current path. The higher inductance of the low-frequency branch effectively forces high-frequency current to flow through the high-frequency branch. The inductance terms of both branches include the inductance associated with the connection to the capacitor, which will depend on the manner in which the capacitor is mounted to the circuit board. Because the two branch inductances will share most of the same loop area,

there is a large mutual inductance between the inductance terms of the high- and low-frequency branches.

Two additional resistance terms are in series with the two branches of the model. One of these terms is constant while the other is proportional to the square root of the frequency. These resistances represent the constant and skin effect losses associated with the connection to the capacitor. Fig. 2.10 shows the proposed model of an MLC capacitor.

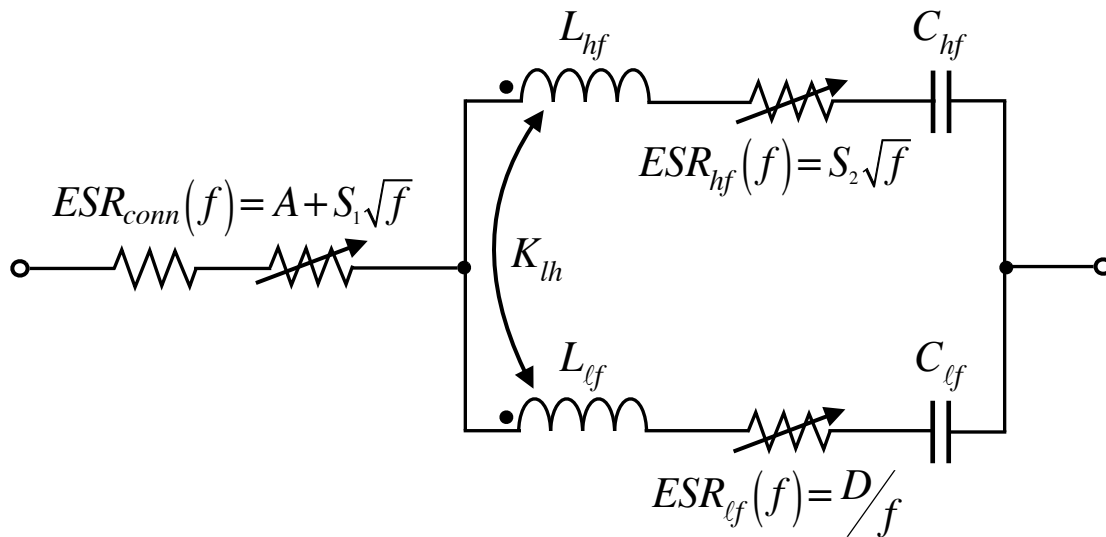


Fig. 2.10. Proposed MLCC model.

At low frequencies, the ESR of the capacitor is dominated by the dielectric loss term found in the low-frequency branch. From [18], the relationship between ESR and dielectric loss is found to be

$$ESR = \tan \delta \cdot \frac{1}{2\pi fC} \quad (2.1)$$

For cases where the dielectric loss is non-negligible, the ESR at low frequencies will naturally decrease with increasing frequency as described in (2.1). The impedance at low frequencies is dominated by the nominal capacitance.

At high frequencies, the ESR of the capacitor is dominated by the two skin effect terms, which are referred to as ESR_{conn} and ESR_{hf} in Fig. 2.10. The high-frequency impedance is dominated by the connection inductance of the capacitor.

2.3 MLCC Measurement Features

The ESR and impedance magnitude, $|Z|$, of X7R and NP0 MLC capacitors from three different manufacturers with a range of nominal capacitances were measured with an Agilent 4291B impedance analyzer connected to an Agilent 16092A test fixture. The available measurement frequency range of this combination is 1 to 500 MHz. Fig. 2.11 shows the equipment used to measure the capacitor properties.

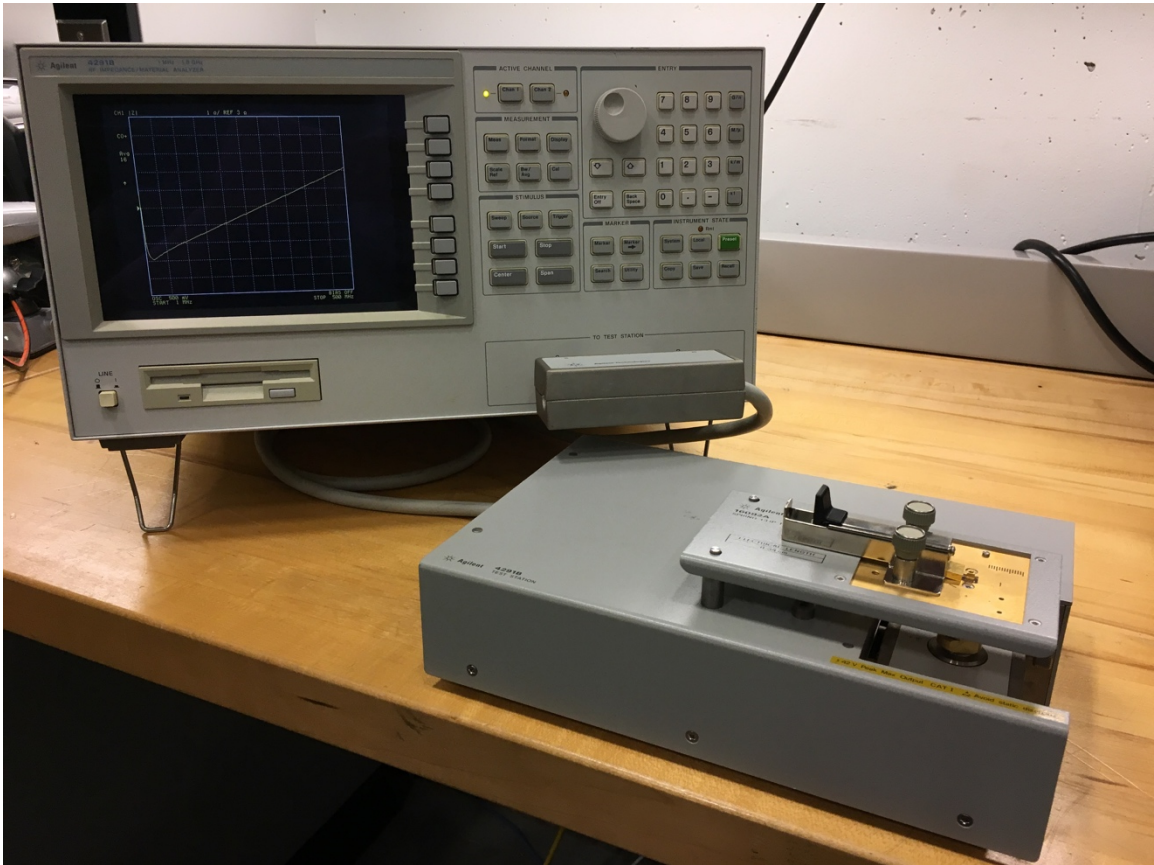


Fig. 2.11. Capacitor measurement setup.

Fig. 2.12 shows the measured impedance of a typical 47-nF X7R capacitor. In this plot, the impedance at lower frequencies is that of the nominal capacitance. The connection inductance of the capacitor is dominant at higher frequencies. In between the two is the self-resonant frequency of the capacitor.

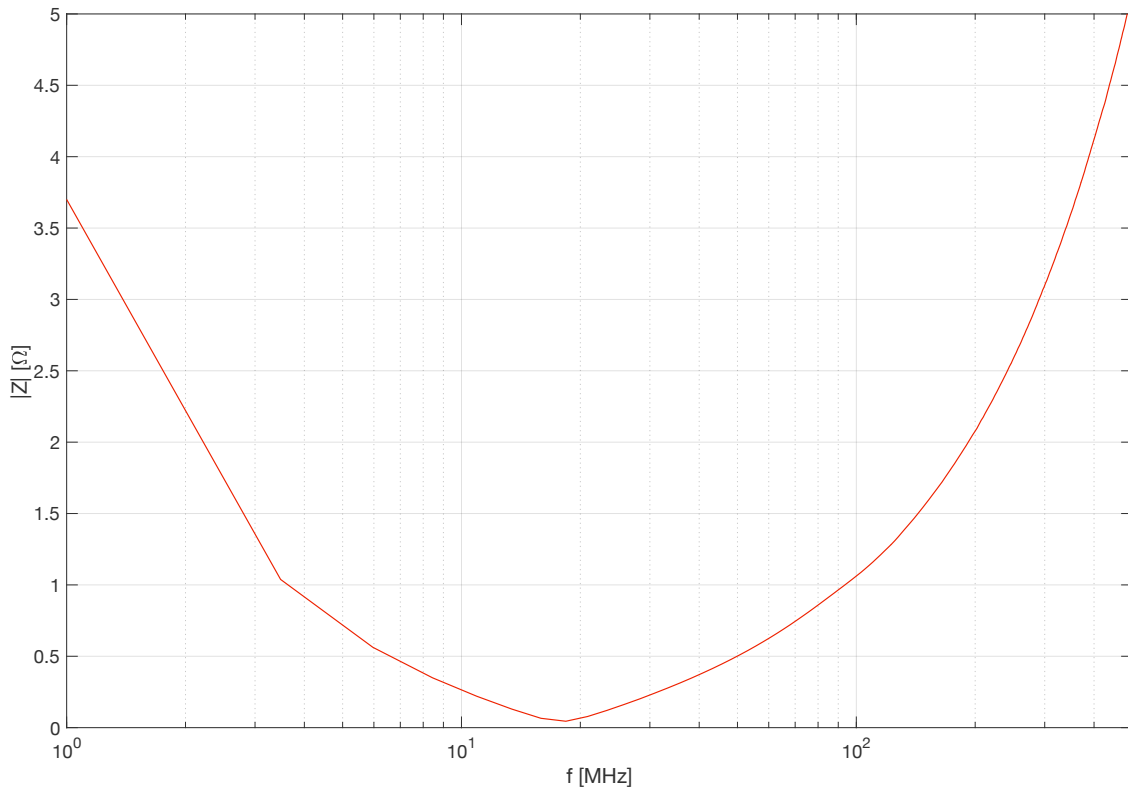


Fig. 2.12. Measured $|Z|$ of a 47-nF X7R capacitor.

A plot of the ESR of a typical 47-nF X7R capacitor is shown in Fig. 2.13. Like the impedance, the ESR of an MLCC can also be broken into two distinctive regions. At lower frequencies, the series losses are dominated by the losses in the dielectric of the capacitor. The dielectric losses are inversely proportional to frequency. At higher frequencies, the losses tend to be dominated by skin effect losses in the capacitor plates which are proportional to the square root of frequency. The ESR curve exhibits a resonance between the two regions, around 100 MHz in Fig. 2.13, which is caused by internal resonances within the body of the capacitor.

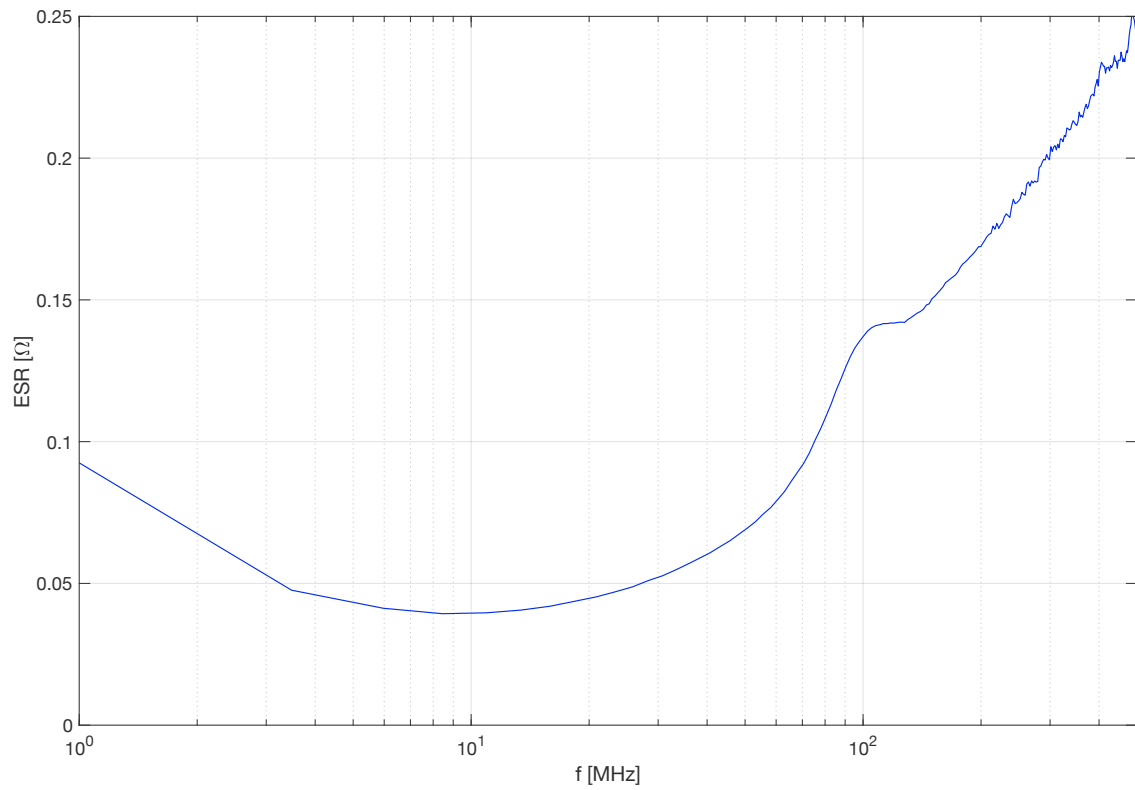


Fig. 2.13. Measured ESR of a 47-nF X7R capacitor.

The lossiness of the dielectric also plays a large role in determining the overall characteristics of the ESR curve. In Fig. 2.14, the ESR of a typical 10-nF X7R capacitor is compared to that of a typical 10-nF NP0 capacitor from the same manufacturer.

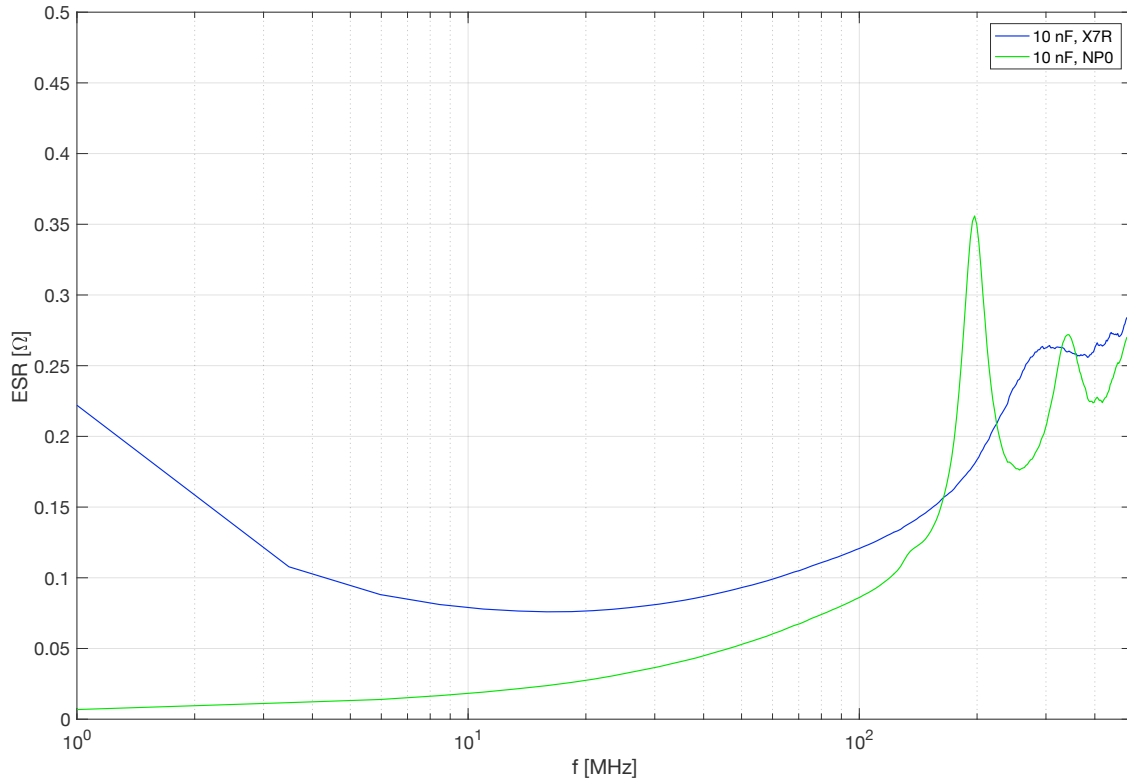


Fig. 2.14. Comparison of measured ESR for 10-nF X7R and NP0 capacitors.

The X7R dielectric is more lossy than NP0. One direct effect of the lossiness of the dielectric to the ESR curve is the value of ESR at low frequencies. From Fig. 2.14, the lossier dielectric, X7R, has much higher losses at low frequencies. From (2.1), it is expected that the ESR of a dielectric with negligible dielectric loss will not show a strong frequency-dependence at lower frequencies where dielectric losses are dominant. This is reflected in Fig. 2.14 in the ESR of the NP0 capacitor.

In addition to affecting the low-frequency ESR, the lossiness of the dielectric plays a role in determining the damping of the transition between the two major regions of the ESR curve. Fig. 2.14 shows resonances in both X7R and NP0 ESR curves around 200–300 MHz; however, the resonances in the ESR curve of the NP0 capacitor have much lower damping than those in the ESR curve of the X7R capacitor. Also, the NP0 ESR curve clearly contains multiple resonances in this region whereas the X7R curve only displays one. The author speculates that these resonances are due to internal resonances within the body of the capacitor.

2.4 Comparison with Measured Data

To evaluate the accuracy and physical relevance of the model from Fig. 2.10, three different X7R capacitors were selected such that the package size and spacing between layers were the same. The nominal capacitances selected were 10, 47, and 100 nF. All three capacitors selected were produced by the same manufacturer.

Fig. 2.15 shows the proposed model of a 10-nF X7R capacitor.

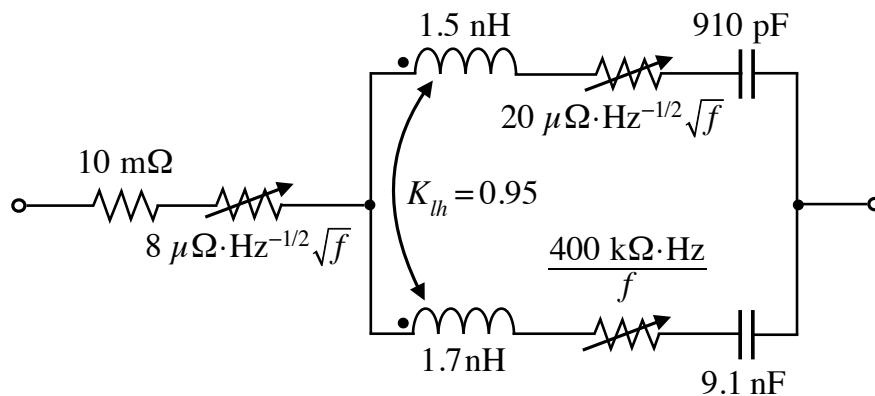


Fig. 2.15. Proposed model of 10-nF X7R MLC capacitor.

According to the manufacturer, the 10-nF X7R capacitor has an approximate capacitance per layer of 454 pF and is comprised of 22 active layers. Given the assumption that high-frequency current only flows in a couple of layers, the capacitance of the high-frequency branch of the model was determined by doubling the single-layer capacitance. Consequently, the low-frequency branch capacitance was determined to be the remainder of the nominal capacitance. The mutual inductance between the loops was estimated to be 0.95 due to most of the loop area being shared by both branches. The package size, estimated loop area, and capacitor self-resonant frequency were used to estimate the inductance terms. The low-frequency inductance was first determined, and the high-frequency inductance was selected to be slightly less than the low-frequency inductance. The dielectric loss term was selected to provide good agreement with the measured data. The constant series resistance of the electrodes was estimated to be 10 m Ω . Both of the skin effect terms were determined by adjusting their constant while comparing to the modeled data.

ESR and impedance plots were generated for the model of Fig. 2.15 and were compared to measured data. In Fig. 2.16, the measured ESR of a 10-nF, X7R capacitor is compared with the ESR generated by the SPICE model of Fig. 2.15.

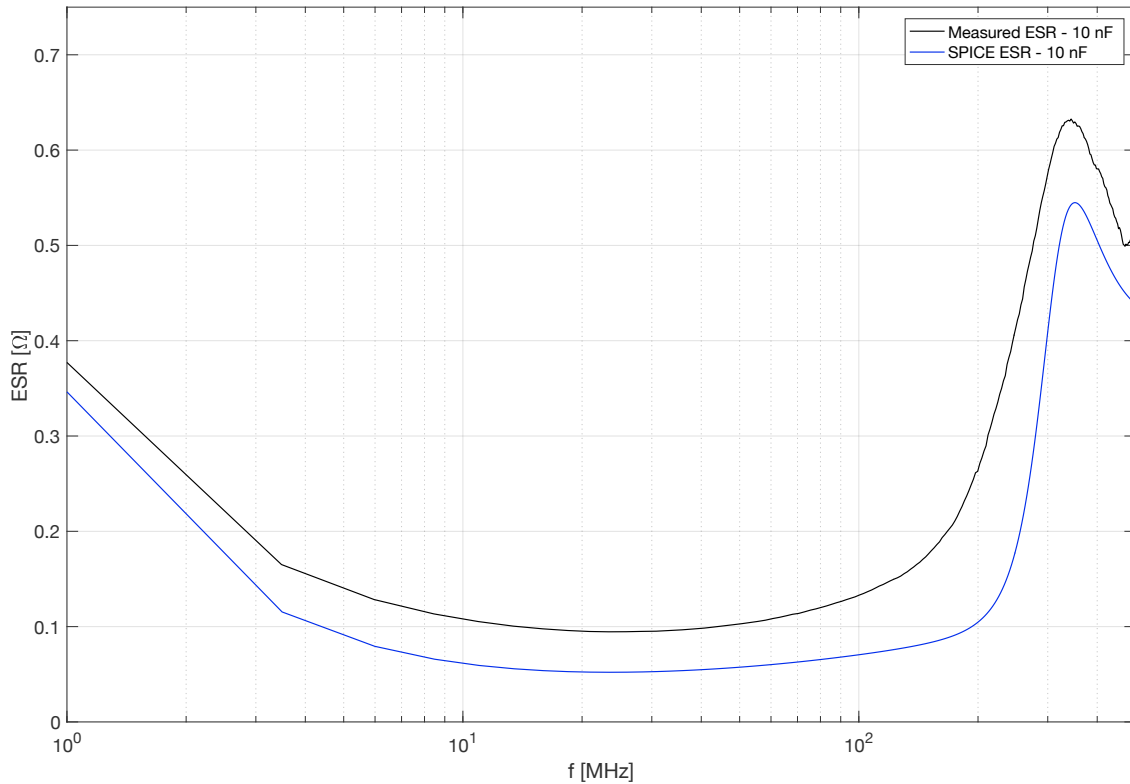


Fig. 2.16. Comparison of measured ESR with that of a SPICE model for a 10-nF X7R capacitor.

While the accuracies of each SPICE model could be improved upon what is presented here, the accuracies of the individual models were sacrificed for improved accuracy across all three models with parameter differences between the three models consistent with the physical differences between the three capacitors.

Throughout the measured frequency range, the SPICE model is on average within 35% of the measured ESR of the 10-nF, X7R capacitor. At worst, around 200 MHz, the agreement is within 60% of the measured value.

It was found that the model without mutual inductance frequently over-predicted the ESR at the resonance around 350 MHz in Fig. 2.16. When the mutual inductance term was added, the agreement at this resonance was improved for all modeled capacitors.

Fig. 2.17 shows the measured $|Z|$ of a 10-nF, X7R capacitor compared to the $|Z|$ of the SPICE model from Fig. 2.15.

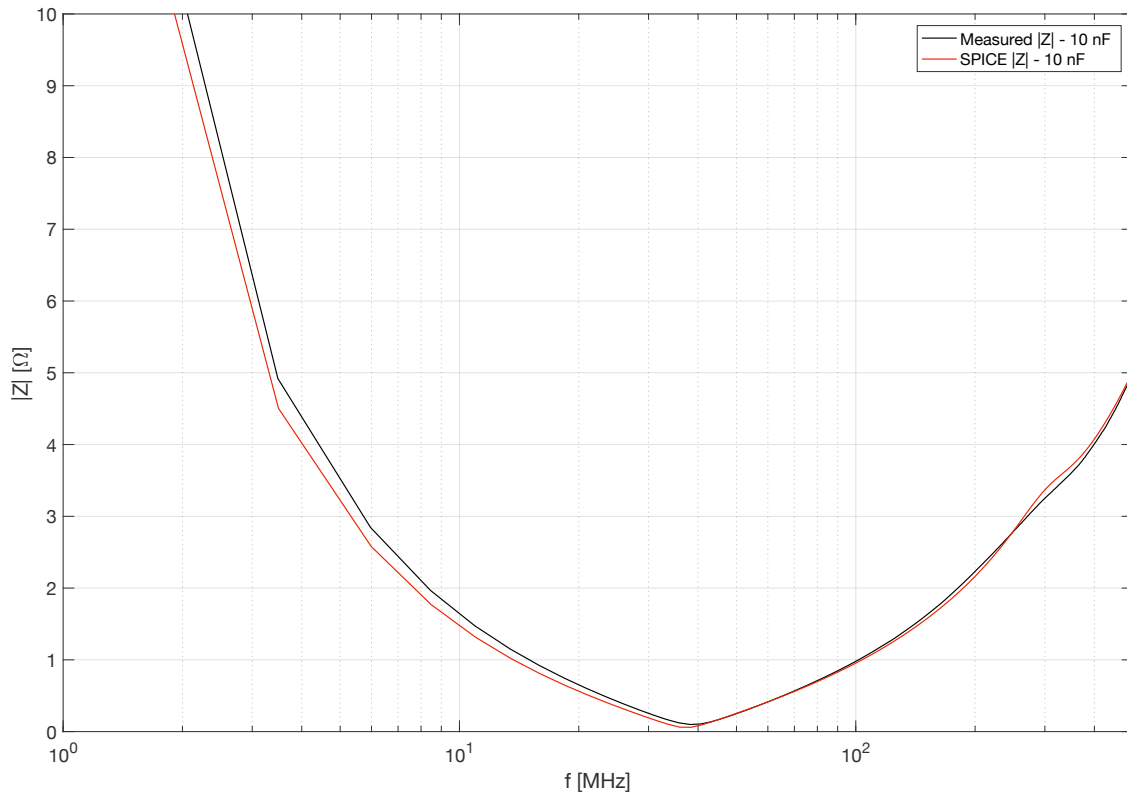


Fig. 2.17. Comparison of measured $|Z|$ with that of a SPICE model for a 10-nF X7R capacitor.

In Fig. 2.17, there is a slight resonance in the $|Z|$ plot around 300 MHz. This echoes the much larger resonance seen in the ESR plot of Fig. 2.16. In the $|Z|$ plot, this resonance is internal to the body of the capacitor and is generally damped by the mutual inductance and losses within the capacitor. The mutual inductance opposes the flow of circulating currents between the plates of the capacitor and tends to suppress any internal resonances that occur. The model slightly exaggerates the resonance seen in the measured data, but apart from this and a slight error in the self-resonant frequency, the model accurately predicts the $|Z|$ of the measured capacitor.

Fig. 2.18 shows the SPICE model of a 47-nF X7R capacitor. The 47-nF capacitor assessed has an approximate capacitance per layer of 2.04 nF and is comprised of 23 active layers. Thus, using the same assumption as with the 10-nF model, the high frequency capacitance is twice the single-layer capacitance and the low-frequency capacitance is the remainder of the nominal capacitance. Since the number of layers is nearly the same as that of the 10-nF capacitor, the inductance of the high- and low-frequency branches and the mutual inductance between them remains unchanged from the 10-nF model. Since there is no difference between the end electrodes, there is also no change to the resistance terms in series with both branches.

It was observed that dielectric losses decrease with increasing nominal capacitance for the X7R capacitors evaluated. This is predicted by (2.1). Due to this effect, the dielectric loss term of the 47-nF capacitor model is lower than that of the 10-nF model. Since the high-frequency model still assumes that high-frequency current is flowing in the same number of plates, the skin effect losses in the high-frequency branch will be the same as those in the 10-nF model. The proposed model for a 47-nF, X7R capacitor is shown in Fig. 2.18.

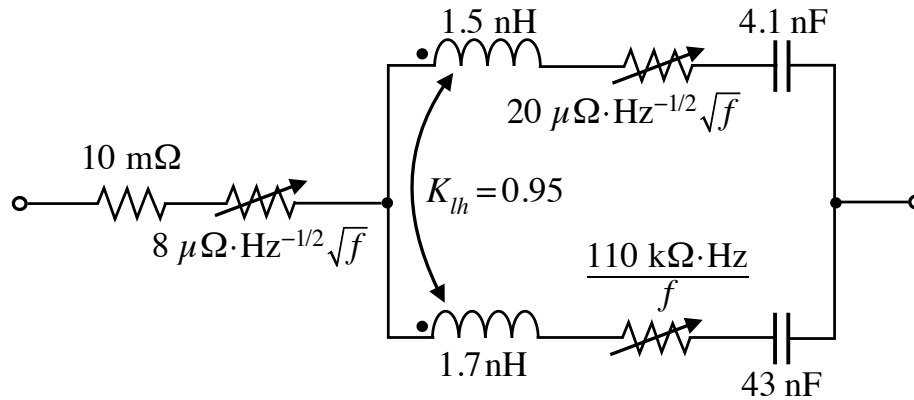


Fig. 2.18. Proposed SPICE model of a 47-nF X7R MLC capacitor.

The modeled ESR is compared to the measured ESR of a 47-nF, X7R capacitor in Fig. 2.19. For this capacitor, the model accurately predicts the behavior of the measured ESR at low frequencies. At higher frequencies, the model overestimates the losses, but is within one-and-a-half times the measured ESR. Fig. 2.20 compares the modeled $|Z|$ to measured $|Z|$ for the 47-nF, X7R capacitor. The agreement between measured and modeled impedance curves in Fig. 2.20 is good.

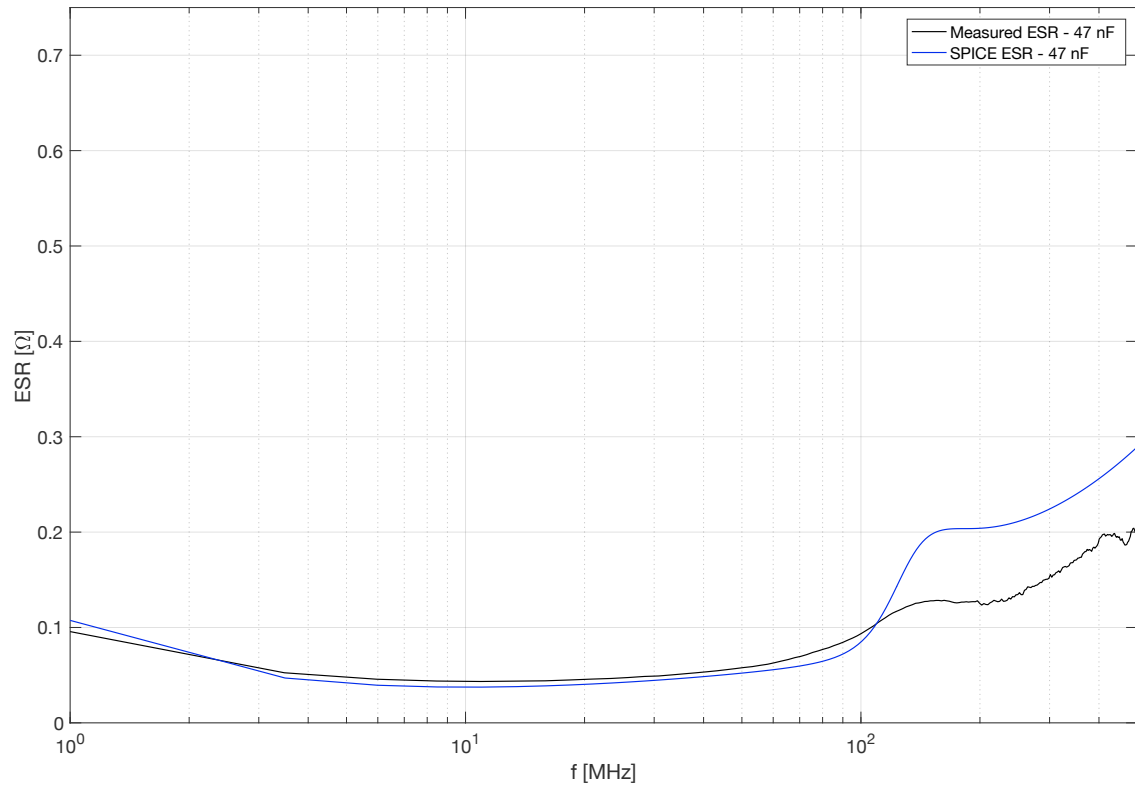


Fig. 2.19. Comparison of measured ESR with that of a SPICE model for a 47-nF X7R capacitor.

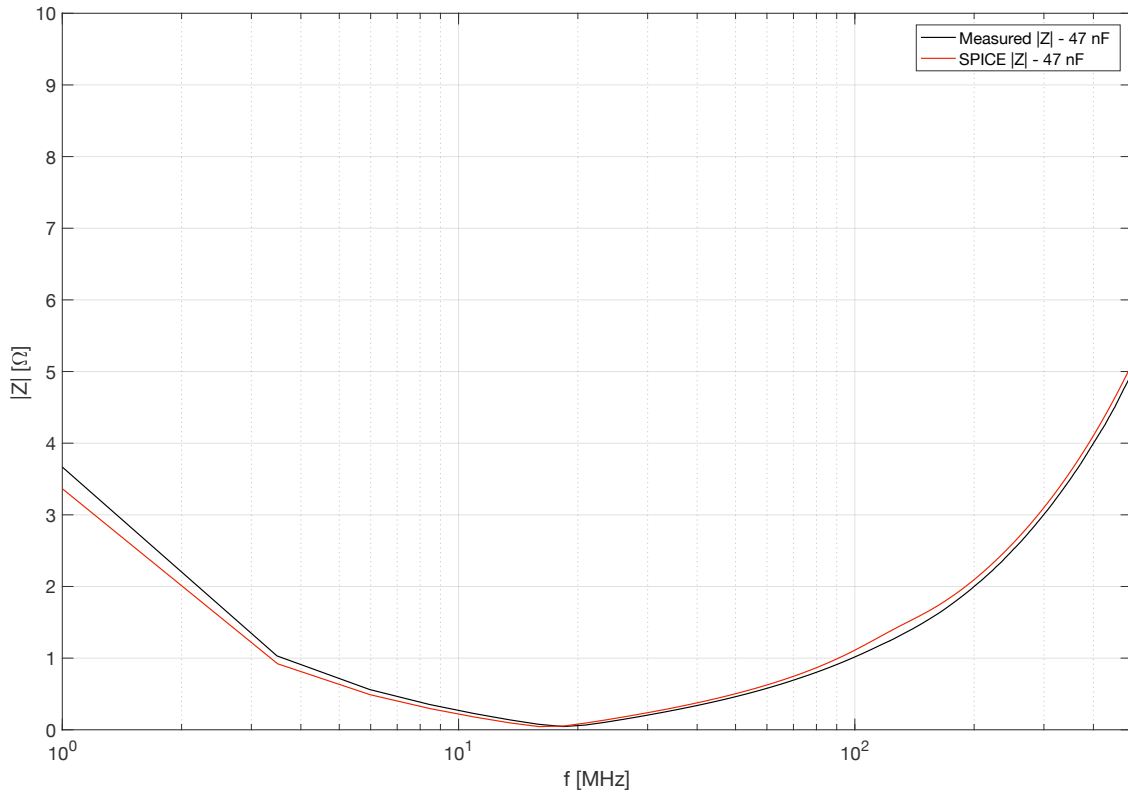


Fig. 2.20. Comparison of measured $|Z|$ with that of a SPICE model for a 47-nF X7R capacitor.

The 100-nF capacitor selected has a capacitance per layer of 37 nF and is comprised of 37 active layers. Thus, the low-frequency inductance is lower than the other capacitors modeled because there are more plates in parallel. With more plates in the stackup but a comparable package height, the lower plates will be closer to the bottom of the capacitor body [19]. This causes the high-frequency inductance to also be lower than the other capacitors modeled. As with the models of the other two capacitors, the high-frequency capacitance is twice the single-layer capacitance, and the low-frequency capacitance is the remainder of the nominal capacitance. Since a similar amount of loop area is shared between the two current paths, there is no change in mutual inductance from that of the other two models. Like the difference between the 10-nF model and the

47-nF model, the dielectric losses of the 100-nF capacitor will be lower than those of the 47-nF capacitor. Again, there is no change to the resistance terms in series with both branches. Fig. 2.21 shows the proposed SPICE model for a 100-nF, X7R capacitor.

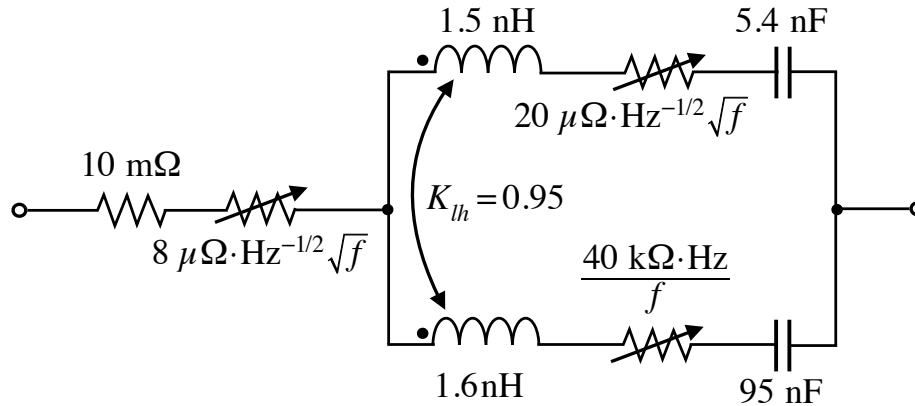


Fig. 2.21. Proposed model of a 100-nF X7R MLC capacitor.

Fig. 2.22 compares the modeled ESR to the measured ESR for a 100-nF X7R, and Fig. 2.23 compares the modeled $|Z|$ to measured $|Z|$ for the same capacitor. Similar to the ESR of the 47-nF capacitor, Fig. 2.22 shows that the model of the 100-nF capacitor matches the measured data very well at low frequencies, but overestimates within one-and-a-half times the ESR at high frequencies.

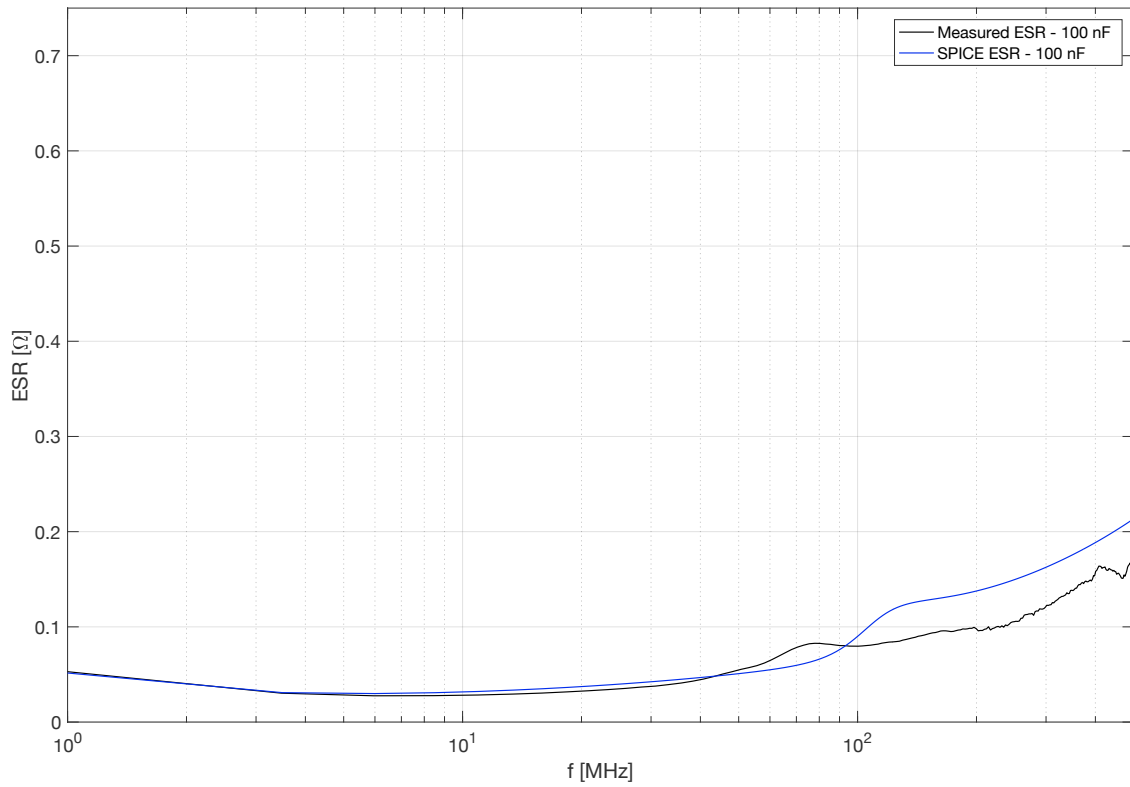


Fig. 2.22. Comparison of measured ESR with that of a SPICE model for a 100-nF X7R capacitor.

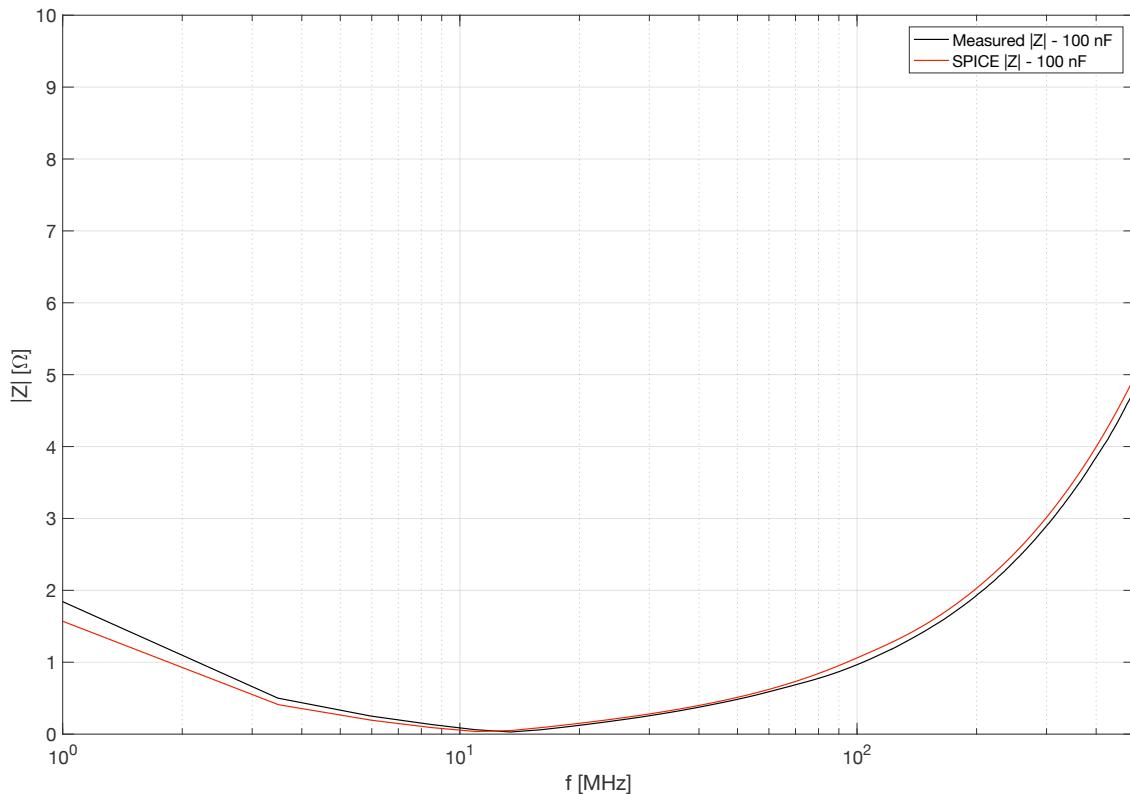


Fig. 2.23. Comparison of measured $|Z|$ with that of a SPICE model for a 100-nF X7R capacitor.

Also like the 47-nF capacitor, Fig. 2.23 shows an accurate prediction of the $|Z|$ for all the measured frequency range.

2.5 Conclusion

The model proposed in this paper demonstrates a simple yet accurate way of modeling the impedance and series resistance of surface-mount multi-layer ceramic capacitors. The proposed model is based on physical phenomena. The model accounts for the transition from low frequencies where the current flows equally in all plates to high frequencies where current flows primarily in the lower plates. At lower frequencies, frequency-dependent dielectric losses dominate the ESR. Conversely, at higher frequencies, frequency-dependent skin effect losses are dominant. The model provides a

natural transition between these two forms of loss by way of its two branches and their differing inductances. Mutual inductance between the two branches, caused by the shared loop area between high- and low-frequency currents, helps damp the internal resonance observed in both the model and measurements.

Measurements of the impedance magnitude and ESR of 10-, 47-, and 100-nF X7R capacitors were taken and compared to modeled data. This paper demonstrates that the proposed model closely matches measured data for several X7R capacitors with differing nominal capacitances. Thus, the proposed two-branch model with mutual inductance and frequency-dependent resistances provides an effective way of modelling multi-layer ceramic capacitors while accounting for the physical phenomena that contribute to losses.

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CHAPTER THREE

INVESTIGATING THE CONTRIBUTION OF NON-LINEAR BEHAVIOR TO LOSSES IN MULTI-LAYER CERAMIC CAPACITORS

Abstract

Multi-layer ceramic capacitors can exhibit a non-linear response when subjected to a sinusoidal stimulus. This non-linear response shifts energy from the fundamental frequency to harmonics of the fundamental. The loss of energy at the fundamental frequency may be interpreted by a measuring system as a resistive loss and might contribute to an increase in the apparent equivalent series resistance (ESR) of the capacitor at that frequency. The non-linear behavior of X7R and NP0 capacitors is investigated and compared to SPICE models of linear and non-linear capacitors. It is determined that the non-linearity does not contribute significantly to the measured ESR under most practical circumstances, but in some cases may be non-negligible.

3.1 Introduction

Multi-layer ceramic capacitors (MLCCs) are known to exhibit non-linear behavior, where the capacitance is a function of the applied voltage. Some MLCC dielectrics are more non-linear than others. Dielectric losses are the dominant losses in MLCCs at lower frequencies [1]. At high frequencies, the dominant losses of the capacitor are due to skin effect losses in the electrodes [1].

Fig. 3.1 shows typical ESR curves for 10-nF X7R and NP0 capacitors [1]. Because the X7R dielectric is lossier than the NP0 dielectric, the ESR of the NP0 capacitor is generally lower than that of the X7R capacitor.

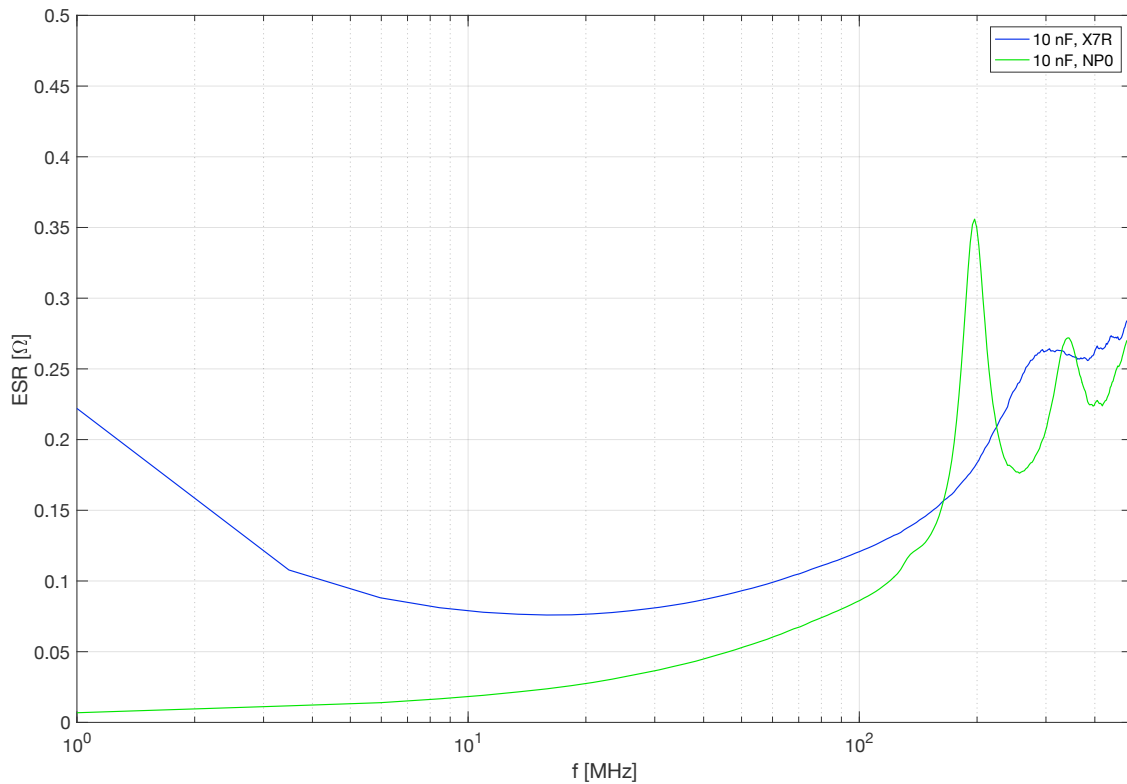


Fig. 3.1. ESR of 10-nF X7R and NP0 capacitors.

Some MLC dielectrics are known to demonstrate non-linear behavior. These capacitors exhibit a capacitance that varies with the applied DC voltage [2]. If this non-linear behavior flattens out a sinusoidal waveform in the time-domain, that affects the harmonics of the waveform in the frequency domain. This paper seeks to investigate whether non-linear behavior of MLCCs causes energy to shift from a fundamental frequency to its harmonics, and whether that energy shift contributes to the apparent ESR of the capacitor at the fundamental frequency.

3.2 Contribution of Frequency Conversion to Apparent Losses

When a multi-layer ceramic capacitor is excited by a sinusoidal source at a given fundamental frequency, power can be shifted into harmonics of the fundamental by the non-linear response of the dielectric. The stronger the excitation, the more non-linear the behavior and the more power that is shifted into the harmonics. This effect is dependent upon not only the strength of the excitation but on the dielectric of the MLCC and the thickness of the dielectric layer. Some dielectrics like X7R exhibit more non-linear behavior than others. Damage to a capacitor may also increase the non-linearity of the capacitor [3]. A thinner dielectric layer will exhibit more non-linearity due to the higher electric field strength for a given applied voltage. The thickness of the dielectric layer is related to the voltage rating of the capacitor.

To investigate this, a test setup is created in which the capacitor under test (CUT) is subjected to a sinusoidal source of 2 MHz and approximately 7.1 V_{rms}. Using a special coaxial cable with a break in the middle, the CUT is soldered between the center conductor and shield of the cable. At the other end of the coaxial cable is a spectrum analyzer. Thus, the capacitor forms a low-pass filter between the function generator and the spectrum analyzer. Fig. 3.2 shows a picture of the test setup, and Fig. 3.3 shows the special coaxial cable and an 0603-size CUT.

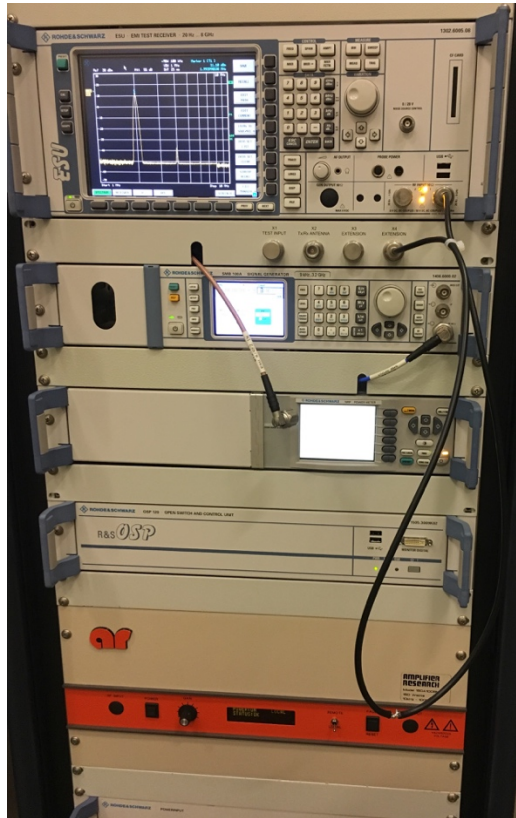


Fig. 3.2. Test setup used to measure capacitor response.

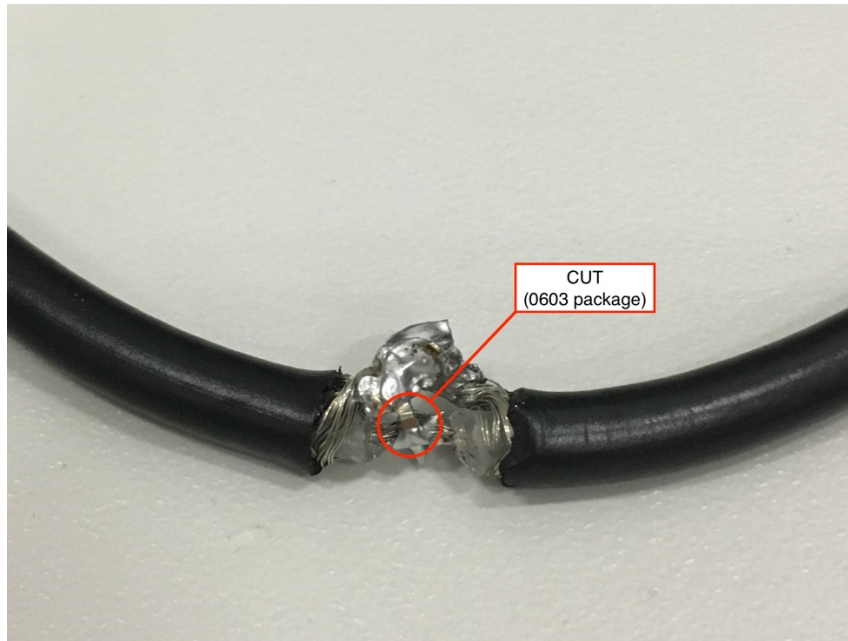


Fig. 3.3. Special coaxial cable fixture used for measuring capacitor response.

The power at the fundamental frequency and its harmonics are measured with a spectrum analyzer using the special cable both with and without the shunt capacitor. The expected attenuation of the CUT at each frequency is calculated and compared to the measured attenuation. Fig. 3.4 illustrates the equivalent circuit of the test setup.

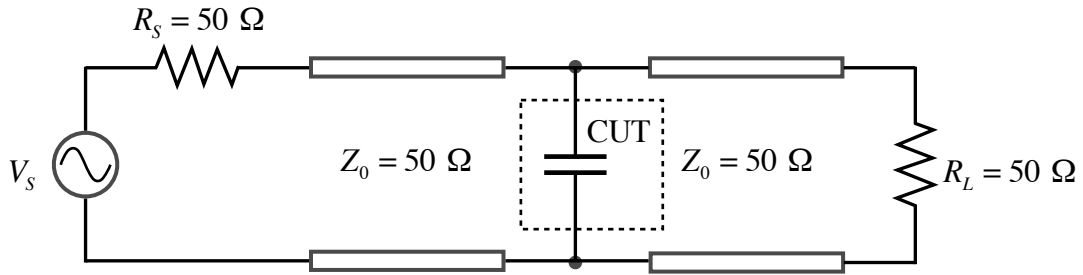


Fig. 3.4. Equivalent circuit of measurement setup.

From [4] and Fig. 3.4, the expected attenuation at a given frequency, f , due to a shunt 10-nF capacitor in a 50-Ω system is determined by

$$\alpha \text{ (dB)} = 20 \log_{10} \left(\sqrt{1 + (\pi f \cdot 50 \text{ } \Omega \cdot 10 \text{ nF})^2} \right) \quad (3.1)$$

Using the special coaxial cable without a CUT, Fig. 3.5 shows the through measurement, which characterizes the standard response of the test setup shown in Figs. 3.2 and 3.3.

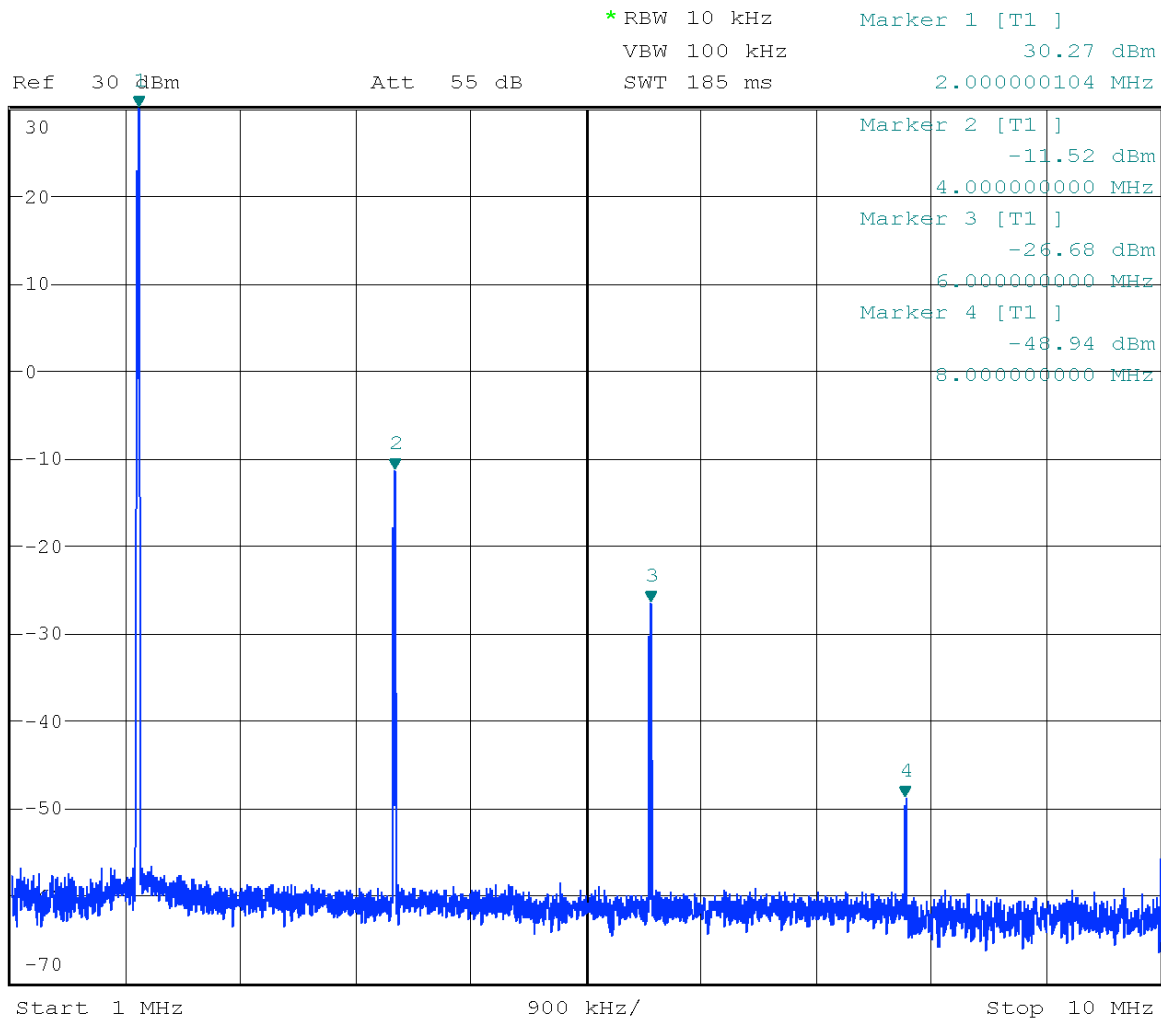


Fig. 3.5. Through measurement with test setup.

It should be noted that Fig. 3.5 shows harmonics of the fundamental that are produced by the source itself; however, the highest of these harmonics is approximately 40 dB down from the fundamental, which is negligibly small for the purposes of this investigation.

Fig. 3.6 shows a measurement of the response of a 10-nF, 50-V X7R capacitor using the test setup shown in Figs. 3.2 and 3.3.

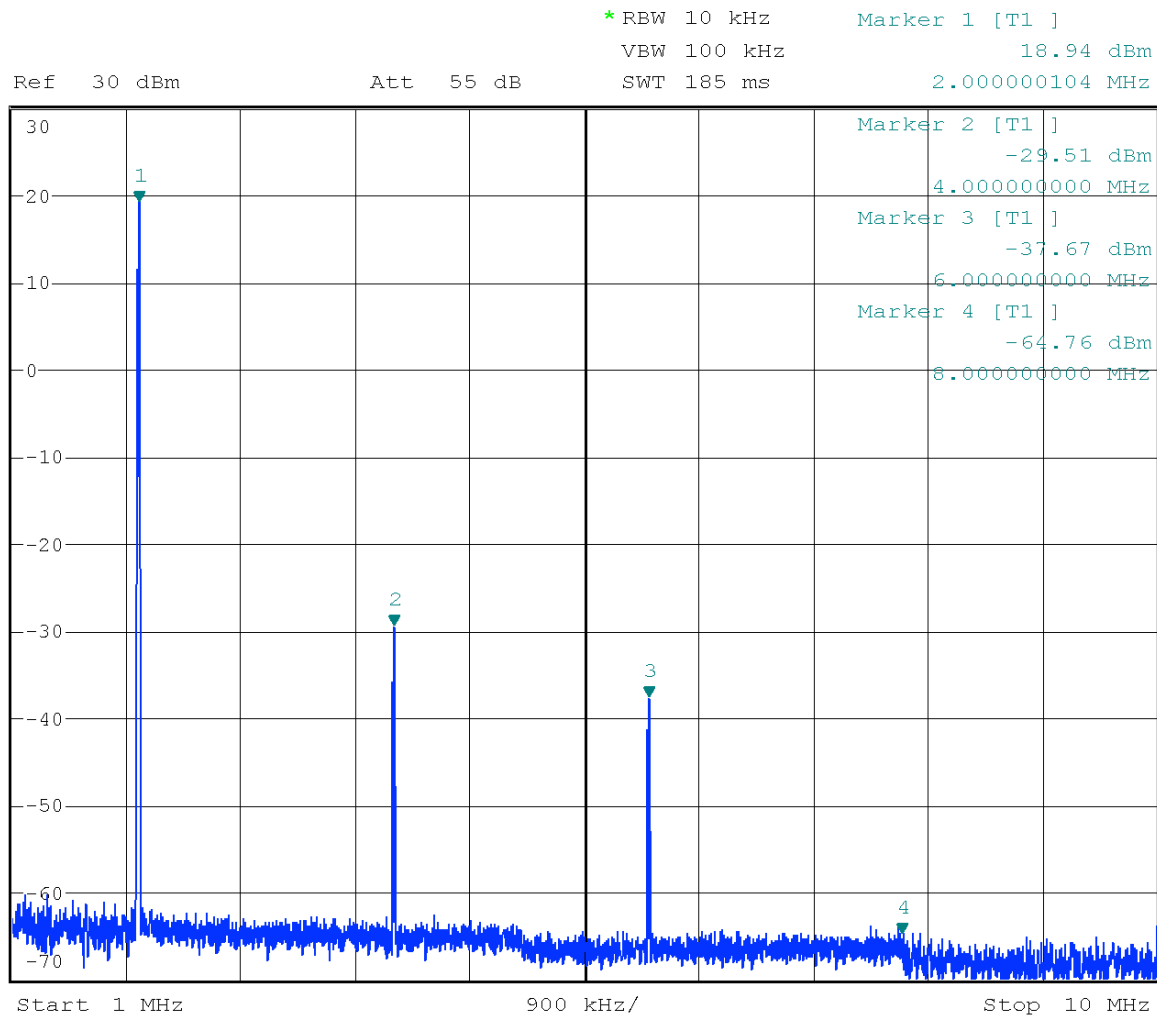


Fig. 3.6. Measurement of 10-nF X7R capacitor with test setup.

After measuring the attenuation of a 10-nF X7R capacitor, the same is done for 10-nF, 50-V NP0 capacitor. This is shown in Fig. 3.7.

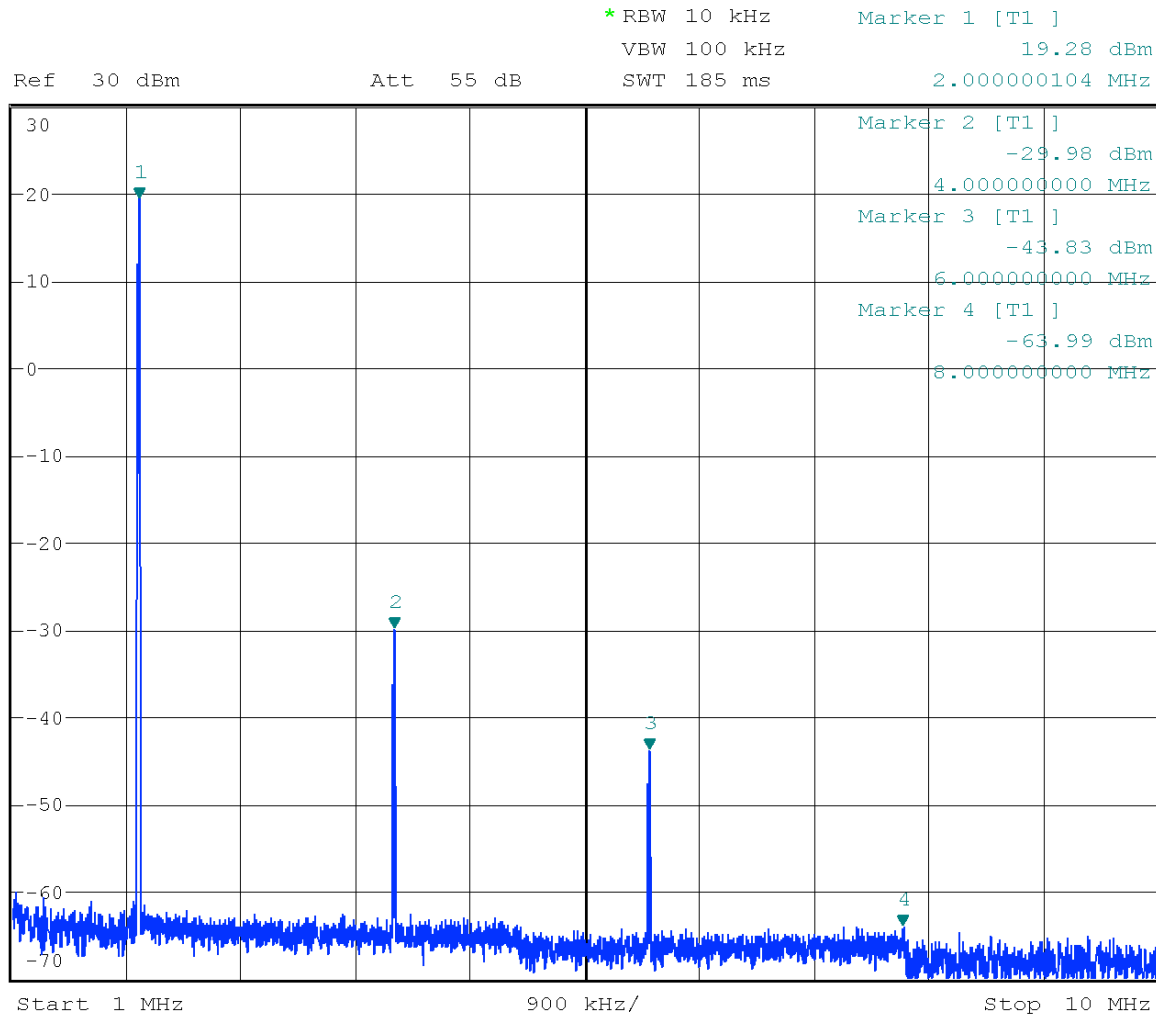


Fig. 3.7. Measurement of 10-nF NP0 capacitor with test setup.

Both the X7R and NP0 capacitors are expected to have the same attenuation, since (3.1) does not take into account the dielectric of the capacitor.

In the case of the 10-nF X7R capacitor, the strength at the fundamental frequency of 2 MHz is within 0.1 dB of the expected value; however, the third harmonic, 6 MHz, is

9 dB higher than expected. The expected value at each frequency was determined by evaluating (3.1) at that particular frequency.

For the 10-nF NP0 capacitor, the strength at the fundamental is 1 dB lower than expected, but the strength at the third harmonic is 3 dB higher than expected.

This indicates that some power is shifted from the fundamental frequency to the third harmonic for both dielectrics, but the effect is not as perceptible with the NP0 capacitor.

To determine if the apparent losses at the fundamental due to this shift in power are appreciable compared to the overall ESR of the capacitor, the ESR required to dissipate the same amount of power that was shifted to the third harmonic is calculated. From Fig. 3.6, the power measured with the spectrum analyzer at the fundamental frequency is 18.9 dBm, or approximately 78 mW. This corresponds to a voltage of

$$P_L = \frac{V_L^2}{50 \Omega} \rightarrow V_L = \sqrt{50 \Omega \cdot 78 \text{ mW}} \cong 2.0 \text{ V}$$

The current through the CUT at the fundamental frequency is then found by

$$\begin{aligned} I_C &= \frac{V_L}{X_C} = 2\pi \cdot V_L \cdot f \cdot C \\ &= 2\pi \cdot (2.0 \text{ V}) \cdot (2 \text{ MHz}) \cdot (10 \text{ nF}) \cong 250 \text{ mA} \end{aligned}$$

A worst-case approximation would assume that all of the power at the third harmonic was shifted from the fundamental due to the non-linear response of the capacitor. This power could be equated to an apparent resistance at the fundamental frequency. Thus, the value of this apparent ESR may be determined by dividing the

power of the third harmonic by the square of the current through the capacitor at the fundamental frequency. Harmonics higher than the third are neglected due to their negligible contribution. From Fig. 3.6, the power at the third harmonic is -37.7 dBm, or approximately 170 nW. The apparent ESR caused by non-linear effects of the capacitor is then approximated by

$$P_{ESR} = I_C^2 \cdot ESR \rightarrow ESR = \frac{170 \text{ nW}}{(250 \text{ mA})^2} \cong 2.7 \mu\Omega$$

From this result, the amount of apparent ESR caused by non-linearity in the capacitor under these circumstances is negligibly small in comparison to the actual measured ESR at the fundamental, which is approximately 100 mΩ as determined by Fig. 3.1.

3.3 Using SPICE to Investigate the Apparent Losses of Non-Linear Capacitors

SPICE models of both linear and non-linear capacitors can be used to determine if a non-linear capacitor with no additional modeled resistance will have an effective resistance in comparison with a linear capacitor model. To do so, a 10-nF capacitor is modeled with dependent sources in PSPICE as shown in [5]. By modeling a capacitor in this manner, non-linearity is created by varying the device capacitance with the voltage across the capacitor. One difference from the example in [5] is that non-linear behavior is extended to include negative bias voltages.

To model a non-linear capacitor, the SPICE model for the non-linear capacitor loses half of its nominal capacitance at a ±10-V bias with linear interpolation of the device capacitance between the 0-V and ±10-V bias points. An extreme case, referred to

as a “very non-linear” capacitor, was also evaluated in which the capacitor loses 90% of its nominal capacitance at a ± 10 -V bias. A linear capacitor is simulated with the same model, but the capacitance does not depend on the voltage across the capacitor.

These capacitor models are placed in parallel with a $50\text{-}\Omega$ load and driven by a $50\text{-}\Omega$ sinusoidal source. The source is characterized by a 40-V amplitude and a 2-MHz frequency. This circuit simulates the equivalent circuit of the physical measurement shown in Fig. 3.4. Fig. 3.8 shows a time-domain comparison of the voltage across the parallel combination of the CUT and load resistor for one linear and two non-linear cases.

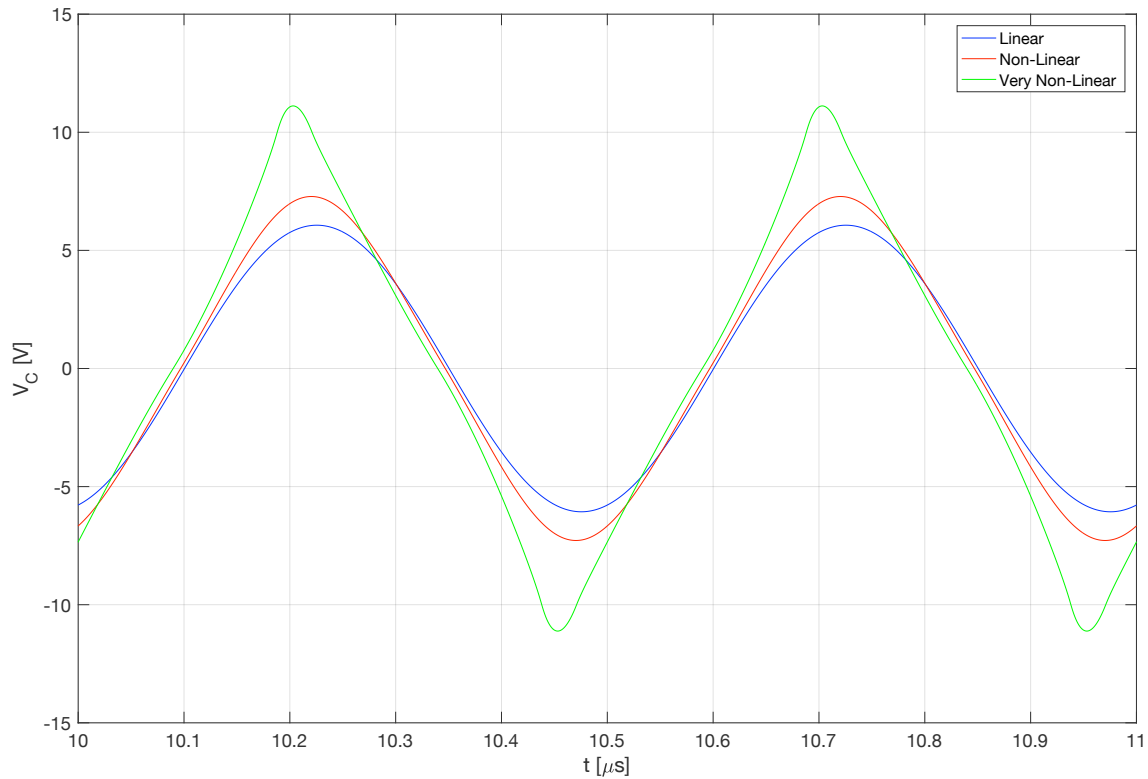


Fig. 3.8. Time-domain comparison of linear and non-linear 10-nF capacitors.

The voltage across the linear capacitor appears to demonstrate a perfect sinusoidal waveform. As nonlinearity increases, the waveform becomes more distorted. For the very

non-linear case, the waveform is clearly no longer a pure sine wave. The voltage waveforms of Fig. 3.8 are transformed with an FFT and plotted as power to provide a comparison in the frequency domain. This power is plotted in dBm in Fig. 3.9.

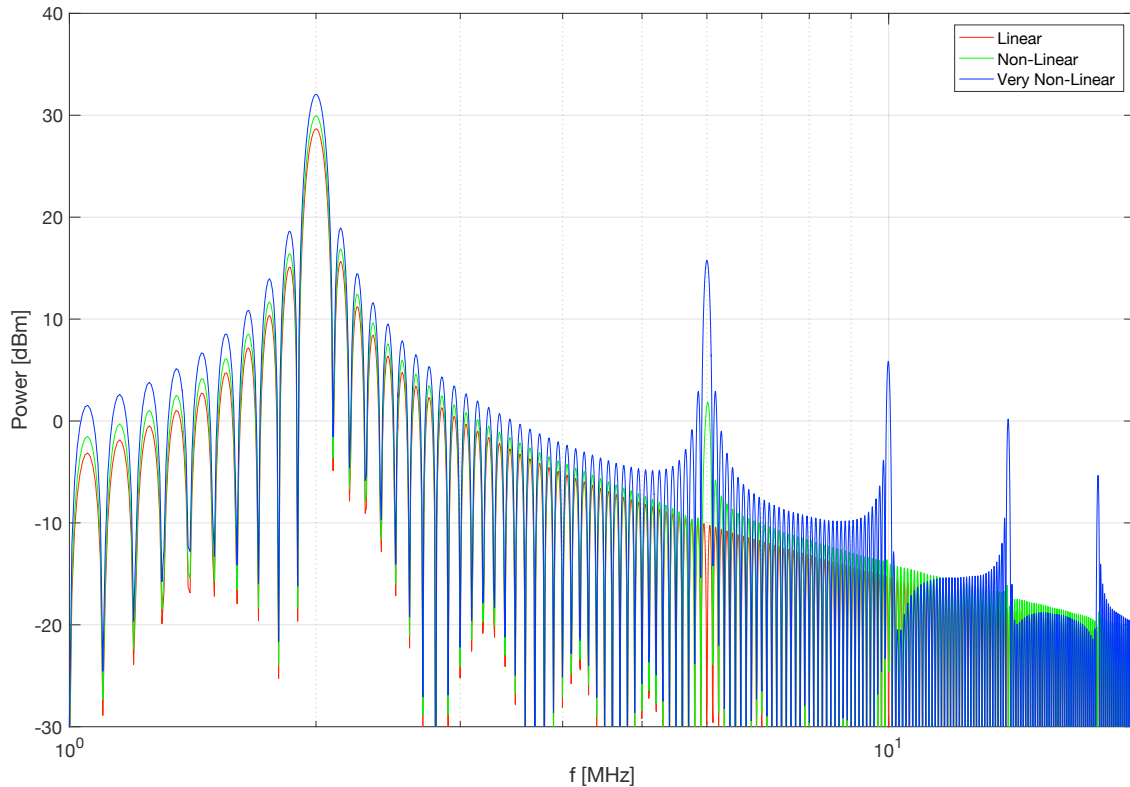


Fig. 3.9. Frequency-domain comparison of linear and non-linear 10-nF capacitors.

The linear capacitor shows a strong response at the fundamental frequency, but displays no harmonic content beyond that. This is characteristic of a pure sine wave. The non-linear capacitor demonstrates a third harmonic that has become significant, but no appreciable harmonics exist beyond the third harmonic. As non-linearity increases further, the very non-linear case shows odd harmonics up to the ninth harmonic that are non-negligible. The increase in harmonic amplitudes as non-linearity increases corresponds to increased distortion in the time-domain waveform. The strength of the

harmonics shown in Fig. 3.9 is inversely proportional to frequency squared, so harmonic contribution becomes negligible at the higher harmonics.

Using the power displayed in Fig. 3.9, the calculations from Section 3.3 are performed for the worst-case, very non-linear capacitor SPICE model:

$$\text{At 2 MHz, } P_L = 32.06 \text{ dBm} \cong 1.6 \text{ W}$$

$$P_L = \frac{V_L^2}{50 \Omega} \rightarrow V_L = \sqrt{50 \Omega \cdot 1.6 \text{ W}} \cong 9.0 \text{ V}$$

$$\begin{aligned} I_C &= \frac{V_L}{X_C} = 2\pi \cdot V_L \cdot f \cdot C \\ &= 2\pi \cdot (9.0 \text{ V}) \cdot (2 \text{ MHz}) \cdot (10 \text{ nF}) \cong 1.1 \text{ A} \end{aligned}$$

$$\text{At 6 MHz, } P_L = 15.75 \text{ dBm} \cong 38 \text{ mW}$$

$$\text{At 10 MHz, } P_L = 5.851 \text{ dBm} \cong 3.8 \text{ mW}$$

$$\text{At 14 MHz, } P_L = 0.1848 \text{ dBm} \cong 1.0 \text{ mW}$$

$$\text{At 18 MHz, } P_L = -5.339 \text{ dBm} \cong 0.29 \text{ mW}$$

$$\text{Thus, } P_{ESR} = 38 \text{ mW} + 3.8 \text{ mW} + 1.0 \text{ mW} + 0.29 \text{ mW} = 43 \text{ mW}$$

$$P_{ESR} = I_C^2 \cdot ESR \rightarrow ESR = \frac{43 \text{ mW}}{(1.1 \text{ A})^2} \cong 39 \text{ m}\Omega$$

From these calculations performed on the worst-case non-linear SPICE model, the extreme non-linear behavior contributed 39 mΩ of apparent ESR to the capacitor. In this case, the apparent losses caused by non-linear behavior are comparable to typical ESRs of MLCCs at 2 MHz.

3.4 Conclusion

It has been shown that, while non-linear behavior in X7R and NP0 capacitors will shift some power from a fundamental frequency to its harmonics, the effective contribution to ESR due to this non-linear behavior under most practical circumstances is negligible. The magnitude of the non-linear effects depends on the voltage rating of the capacitor, which determines the thickness of the dielectric layers, and the strength of the applied voltage. For an applied voltage that is small relative to the voltage rating of the capacitor, non-linear effects will make a negligible contribution to the apparent ESR of the capacitor.

Under extreme circumstances, a very non-linear capacitor may exhibit a capacitance that is strongly dependent upon the applied voltage. If such a capacitor is driven with a signal that is large relative to its voltage rating, the capacitor may show a non-negligible contribution to the capacitor ESR due to the non-linear behavior of the capacitor.

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