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Characterization of Polymer Hermetic Sealed Tantalum Capacitors Using Thin-film Devices

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CHARACTERIZATION OF POLYMER HERMETIC SEALED TANTALUM CAPACITORS USING THIN-FILM DEVICES

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ABSTRACT

Polymer Hermetic Sealed (PHS) capacitors are advanced polymer capacitors with a hermetic seal enclosing the materials inside a metal enclosure. Their primary features include leakage current stability, high volumetric efficiency, and low weight compared to both wet and solid-state polymer tantalum capacitors. However, Life Tests performed on these capacitors have revealed a failure to withstand their rated voltage in a working temperature range over the long-term. There are also other interesting properties which have been observed such as Breakdown voltage (BDV) exceeding the Formation Voltage (V_f), anomalous transient currents, and a larger than expected capacitance dependence on temperature, C(T).

A primary goal in this research is to understand whether the observed characteristics of PHS capacitors are a result of their complex structure or due more to the nature of interactions between the organic and inorganic material layers present. C(T) and BDV measurements were performed on thin-film MIS capacitors representing the material layers of PHS capacitors. Measurements were performed in the voltage range (0V-100V), a temperature range (-55^0C to 125^0C), with varying frequency (20-10kHz), under both humid and dry conditions. Furthermore, one sample went through a curing process referred to as "Heat Treatment", which is thought to improve device stability. Results from these measurements show that thin-film devices can be reasonable representatives of discrete PHS capacitors, and the properties observed in PHS capacitors are significantly dependent on the material layers in the capacitors. Thus, the thin-film MIS capacitor is shown to be a useful test structures for investigating physical phenomena observed in the more complex polymer Ta capacitor structure.

DEDICATION

To my brother, Srinivas Chinnam, for constantly inspiring me be to a better person and encouraging me all along.

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CHAPTER 1

INTRODUCTION

PHS Tantalum Capacitors

Polymer Hermetic Sealed (PHS) Tantalum(Ta) capacitors are advanced solid Tantalum capacitors with a Ta anode, tantalum pentoxide (Ta_2O_5) dielectric, and a conducting polymer as the cathode. These capacitors are hermetically sealed to maintain the humidity inside the metal enclosure. A picture of a PHS Ta capacitor is shown in the Figure 1.1. PHS capacitors have superior properties compared to traditional Ta capacitors with liquid electrolytic cathodes, referred to as wet Ta capacitors. PHS capacitors possess a high volumetric efficiency of capacitance, weigh less, and exhibit an improved capacitance retention at low temperature (below 0^0C) and high frequency (10Khz), compared to wet Ta capacitors [1]. Moisture retention in the PHS capacitors, achieved by forming hermetic seal, has contributed to stabilization of leakage current in polymer Ta capacitors. Owing to these advantages, PHS Ta capacitors are primarily used in space applications such as satellites and missiles.

Figure 1.1: Commercial grade PHS Tantalum Capacitor by KEMET electronics corporation [35].

Long term testing has revealed that these capacitors failed to withstand their rated voltage and working temperature range. Also, recently KEMET discovered a new property in a variant of

PHS capacitor which was never observed before, where the Breakdown Voltage(BDV) of these capacitors exceeded their Formation voltage(V_f). Phenomenon of BDV > V_f is possible and previously observed in Wet Ta capacitors and Polymer Ta capacitors due to extension of dielectric[28]. Though, in such cases the capacitance loss is observed due to an increase in dielectric thickness and more capacitors are used in the applications to compensate the capacitance loss. This combination of BDV>V_f without capacitance loss and open failure mode is critical for the applications where there is a limitation on space and number of capacitors and where short circuit current can prove to be costly. But there is a lack of understanding of this high breakdown voltage phenomenon. To fully exploit this phenomenon and to improve long term stability it is necessary to investigate the properties of Polymer Ta capacitors through their characterization.

These PHS Ta capacitors represent a complex structure made from special flawless technology anodes [2], coarse tantalum powder, thin dielectrics, and pre-polymerized PEDOT cathodes sealed with internal humidity. Here the primary question is to understand whether the characteristics of PHS capacitors are a result of the special manufacturing process and the resulting complex structure involved or if it is primarily due to the nature of interactions between the organic and inorganic material layers present. If it is due to the nature of interactions between the materials involved, then the capacitor properties can best understood by preparing thin-film representations of these PHS capacitors with varying specifications and then find ways to improve PHS Ta capacitors. Otherwise, it can be concluded that the complex structure and the technology used to fabricate these capacitors is the primary contributor to the observed properties. In either case, fabricating thin-film devices similar to PHS capacitors and comparing the properties with properties discrete PHS capacitors will be helpful to understand and ultimately improve the performance and applications of PHS Ta capacitors.

Summary of Chapters

In Chapter 2, we review basic capacitor theory and review the evolution of Ta capacitors from wet Ta capacitors to solid Ta capacitors.

In Chapter 3, intrinsically conducting polymers will be introduced and the history of how they came to replace MnO_2 in solid Ta capacitors will be reviewed. We will also review the advancements made in polymer Ta capacitors in the form of the transition from in-situ to pre-polymerized Ta capacitors. PHS Ta capacitors will be introduced towards the end of this chapter, concluding with discussion of the motivation for studying these capacitors.

In Chapter 4, the measurement procedures performed on PHS capacitors will be presented thoroughly along with some background on the particular capacitors used for these measurements. The detailed measurement procedures, reasoning behind this procedure, and the detailed setup used for these measurements will be presented. The experimental results obtained will be discussed and analyzed in order to lay out the next steps for understanding the results. Chapter 4 is concluded with a discussion on the motivation to perform measurements on thin-film devices replicating the structure of polymer Ta capacitors.

In Chapter 5, experimental investigations on thin-film devices will be presented starting with the structure of these devices, followed by a description of the procedures for fabrication of the thin-film devices. The measurement setup and the procedures followed are then explained in detail. Finally, the results of the measurements are presented and discussed in detail.

In Chapter 6, the results of the measurements performed on the thin-film devices are discussed. Analysis of these results will be used to improve our understanding of the behavior of

PHS capacitors. This chapter will be concluded with the major observations and conclusions obtained from this research along with ideas for further research in this area.

CHAPTER TWO

REVIEW OF CAPACITOR THEORY AND THE EVOLUTION OF TANTALUM CAPACITORS

Capacitor Theory

A capacitor is a two terminal device which can temporarily store charge. In its simplest form, it has two electrical plates or electrodes separated by an insulator (dielectric). The positively charged plate is called the anode and the negatively charged plate, the cathode. An illustration of parallel plate capacitor is shown in Figure 2.1[4]. Two parallel conducting plates of area 'A' are separated by a dielectric of thickness 'd'. While one conducting plate serves as cathode, the other serves as the anode. An increase in the electric field across a dielectric increases the charge accumulated on the plates in-turn increasing the potential difference between the plates. The ability of the capacitor to store the charge is described by its capacitance. Capacitance is given by the ratio of the magnitude of charge to the magnitude of the potential difference between the plates. Capacitance is proportional to the area (A) of the conductors and the electrical permittivity of the dielectric obtained by the product of electrical permittivity ('ε') of free space and the dielectric constant ('k') of the insulating material. It is inversely proportional to the distance (d) between the plates [2, 3]. Capacitance of a parallel plate capacitor is thus given by equation 2.1.

$$C = \frac{\varepsilon \cdot k \cdot A}{d} \tag{2.1}$$

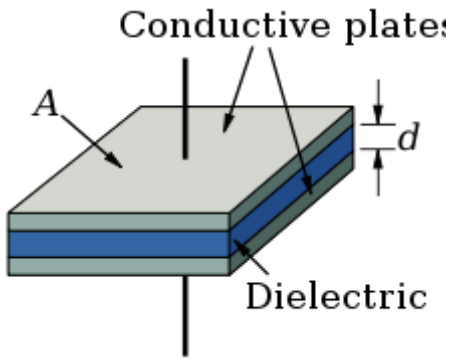

Figure 2.1: An illustration of parallel plate capacitor [4]

Energy(E) stored in a capacitor due to an electric field is given by

$$E = 0.5 \cdot C \cdot V^2 \tag{2.2}$$

It implies energy storage is dependent on area and dielectric thickness. Sometimes more charge or energy must be stored in capacitors of very small size, a quality measured in terms of energy stored per unit volume, defined as Energy density. High energy density is achieved by increasing surface area, improving dielectric quality, or decreasing dielectric thickness.

All manufactured capacitors have certain parasitic elements. An Equivalent Series Resistance (ESR) exists in capacitors because the conducting plates are not perfect conductors and because of the loss associated with the dielectric. An Equivalent series inductance (ESL) is created when current is restricted to follow a defined physical path. The current must be crowded into the available paths, and greater restriction over a longer path increases the ESL. The general electrical performance of a capacitor can be defined as a series arrangement of these elements with the ideal capacitor as shown in Figure 2.2[6]. These parasitic elements are influenced by type, quality, type of processing, and packaging that goes into the fabrication of these capacitors. [6]

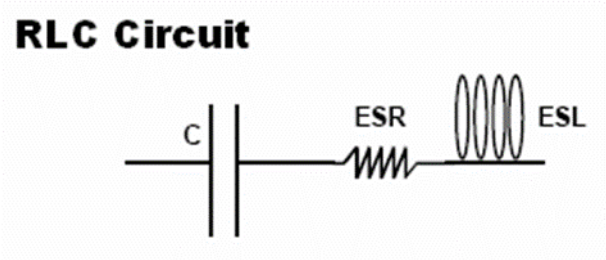

Figure 2.2: Parasitic elements of a capacitor [6]

Ideally, capacitors should not conduct DC current. Since the capacitors are not perfect some DC current always flows through the capacitor, which is defined as Leakage Current. The amount of this DC leakage current depends on the quality and thickness of the dielectric, anode and cathode material. When the DC voltage across the capacitor is sufficiently high, very high leakage current flows through the capacitor which can damage the dielectric. The voltage at which this breakdown occurs is defined as the breakdown voltage of that capacitor (BDV). This BDV indicates the upper limit of the operation for a capacitor. Under normal circumstances, devices are operated well below the BDV, but within a range specified by the manufacturer referred to as the Working Voltage range. A capacitor is expected to operate at its intended level of performance within this range [5].

Electrolytic Capacitors

Electrolytic capacitors are a very common type of capacitor used in certain applications where there is a need for high capacitance in a very small volume. They are called electrolytic due to the fact that either or both of their conductive plates is an electrolyte. An electrolyte is typically a solution that conducts electricity via the ions present in the solution, and the dielectric is formed by inserting the anode in an electrolytic bath and having current pass through the system [5]. Here

the electrolytic bath acts as a cathode. Due to the oxidation process, a thin layer of metal oxide is formed on the surface of the anode, which will serve as the dielectric [6]. The voltage at which this oxidation of the anode (referred to as Anodization) takes place is called the Formation Voltage (V_f) of that capacitor. Dielectrics formed this way are thin, rough and perfectly conforming to the surface of the metal anode. While keeping the size of the electrode the same, the surface area of the dielectric can be increased by starting with an anode with an uneven surface. Since the cathode is a liquid electrolyte it easily conforms to the uneven surface of the dielectric resulting in a higher capacitance. We can see a clear difference between a standard parallel plate capacitor in Figure 2.1 and an electrolytic capacitor with a larger dielectric contact area in Figure 1.3[7]. In electrolytic the capacitor the anode is etched with an uneven surface, whereas the anode (A) in parallel plate has smooth surface. As seen in the Figure 2.3 this uneven surface in electrolytic capacitor results in large surface area in contact with dielectric. One benefit from using a liquid electrolyte is that ionic current through the electrolyte helps to maintain the integrity of dielectric. It helps by healing any dc leakage damage sites through reformation of the dielectric (healing) in a fashion similar to how it was originally formed [2].

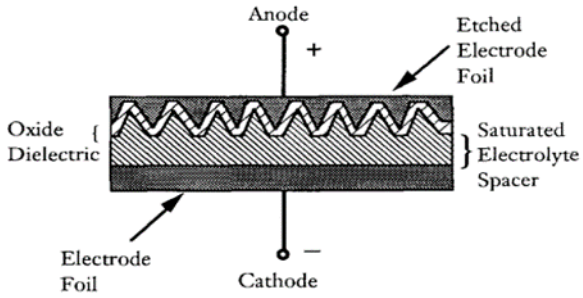

Figure 2.3: Electrolytic capacitor showing a large anode surface area [7]

Tantalum Capacitors

Historically, aluminum was used in electrolytic capacitors for the anode. However, Tantalum gained prominence owing to the significant improvements in terms of the range of operating temperature and chemical stability of the metal and its anode [8]. Despite these improvements, there were still limitations associated with all wet electrolytic capacitors, such as large volume, low temperature limitations resulting from solidification of the electrolyte, and a limited shelf life [6,8]. Another drawback is due to the use of a caustic solution, which generates gases and cannot withstand thermal cycles of a surface mount assembly [9].

Then came a breakthrough in the form of manganese dioxide, MnO_2, acting as a cathode. MnO_2 is a semiconducting solid with good electrical conductivity and long-term stability to act as a cathode. The main advantage of MnO_2 is that it can be applied as a Manganese Nitrate solution to anodized tantalum by a series of dips with drying cycles in between. The chemical equation showing the formation of solid Manganese dioxide from Manganese nitrate using pyrolysis carried out at 250 to 350^0C, is shown below [9]: MnO_2 as a cathode is solid, occupies much less volume, has better temperature characteristics and shelf life, but still conforms to the surface of the dielectric much like a liquid electrolyte [9].

$$Mn(NO3)2 . 6H2O \rightarrow MnO2 + 2NO2 + 6H2O \qquad (2.3)$$

Construction

Construction of solid Ta capacitors starts with fine tantalum powder in the form of spherical grains. Technical advancements in tantalum powder move towards shrinking the diameter of the grains which increases the surface area or capacitance per unit volume. The anode is formed by pressing the powder into a pellet, a compact collection of tantalum powder grains, around a tantalum wire. Within the pellet, as particles are pressed together they form an electrical contact, though there is still a large amount of open volume. The tantalum wire serves as a common electrical contact for all particles in the pellet [11].

To increase the contact area between the grains in the pellet and the tantalum wire, the anode (pellet +Ta wire) is sintered in vacuum at $1350\ ^{0}C$ for 10 minutes[12]. This sintering process also helps to drive out any contamination that was introduced during the pressing process. The result is a pure porous Tantalum pellet with large amounts of surface area within a confined volume [9,11].In the next step the oxide layer is formed on the pellet by submerging it in an electrolytic bath and passing current through it. Liquid electrolyte enters all voids and channels and makes contact with the Tantalum particles and Tantalum wire. Oxygen from the electrolyte combines with Ta when the current is passed through the system to form the dielectric, Ta_2O_5. The thickness and consistency of the dielectric depends on the formation voltage, V_f, the current, and the time for which these are applied.

The cathode material applied is in a liquid form so that it penetrates the porous anode structure. $MnHNO_3$ is a liquid in which the Ta pellet is dipped, and then heated to dry. $MnHNO_3$ is converted to solid MnO_2 in the drying process. This dip and dry process is continued until the desired cathode thickness is achieved. MnO_2 thus penetrates into the porous Ta and covers the outside surface. On top of MnO_2 a graphite layer followed by silver paint is applied to achieve a

low resistance interface. The structure of a capacitor with all the above-mentioned components is illustrated in Figure 2.4[13]. On the left end is the Tantalum wire to which electrically continuous spherical Tantalum particles are connected. Other layers are labeled accordingly in Figure 2.4. The last step before encasing the capacitor is to connect a lead frame to the silver paint with conductive epoxy in order to make an external cathode connection, while the Ta wire serves as the anode [11]. Figure 2.5[14] shows an illustration of a completed chip-type tantalum capacitor.

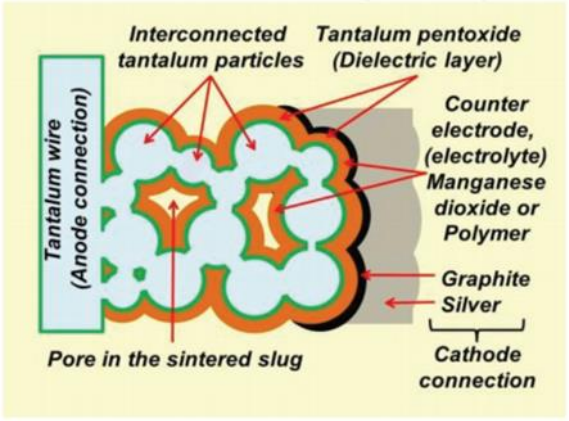

Figure 2.4: Structure of solid Ta capacitor with MnO_2 cathode [13]

Figure 2.5: Finished surface-mount Tantalum capacitor [14].

Failure Mechanism of Ta-Ta2O3¬-MnO2¬ Capacitors

Manufacturers of Ta capacitors often recommend de-rating of 50% for these devices. So, even if the capacitor is rated to work at a specific operating voltage it is still recommended to operate below 50% of that voltage. This cautionary measure is recommended to limit the high turn-on and infant mortality rates observed in solid Tantalum capacitors.

According to one theory, the reason for these failures is the stress-induced defects in the dielectric. During the dip and dry process of the Ta anode, liquid Manganese nitrate enters small channels and openings in the Ta pellet. This process involves dipping the pellet in manganese nitrate at room temperature and then heating at 270^0C to dry. This process is repeated several times to achieve full coverage. As three materials of different coefficients of thermal expansion are involved (Ta, Ta_2O_5, and MnO_2), repeated cycles of heating can create mechanical stress and ultimately lead to cracks in the dielectric. Figure 1.6 is an image of a constricted channel inside a porous anode where MnO_2 is contributing to stress on the dielectric layer [15].

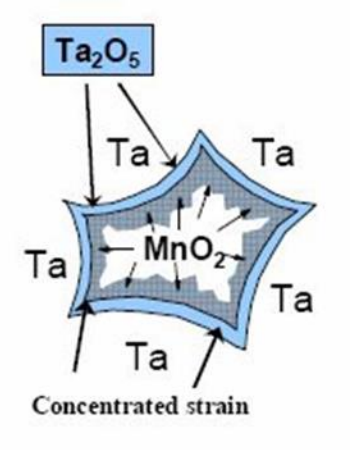

Figure 2.6: MnO_2 as contributing force to cracks [15]

It is impossible to create a perfect and continuous dielectric because of impurities that will be present even in the purest of Tantalum metal and electrolyte solutions available [16]. These impurities along with stressed areas created during the processing create weakened sites in the dielectric. When subjected to high voltage these sites collapse and create a path for leakage current [11]. Due to this current, MnO_2 present at the leakage sites will start heating up. Eventually, this heat will increase and reach temperatures sufficiently high to cause conversion of MnO_2 to its other oxide form of Mn_2O_3. This lower oxide form of Manganese has very high resistance and thus will close the current path. This process is called Self-healing in Ta-MnO2 capacitors, though the dielectric is not actually healed [6,11]. This self-healing process is illustrated in Figure 1.7[6].

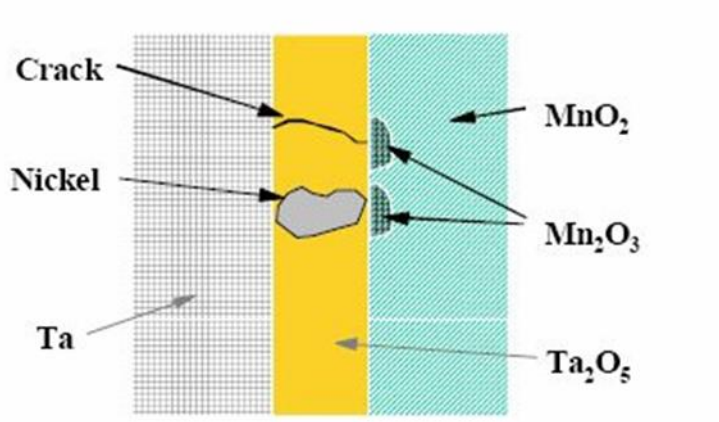

Figure 2.7: Self-healing property of MnO_2 [6]

All the manufactured solid Ta capacitors have defects in their dielectric. Before selling, these capacitors are stressed to a high voltage to activate the above self-healing mechanism. This process, referred to as aging of the capacitors, will remove many fault sites and reduce leakage current. This process of healing will continue long after the aging process as the application life increases [11].

In the self-healing process, at a temperature slightly higher than that required for self-healing, the dielectric itself will start heating up and convert from an amorphous to a crystalline structure. However, the crystalline form of this oxide is almost 1000 times more conductive than the amorphous structure. So, this crystallization process eventually results in an increase in the leakage current. On the other hand, the cathode material MnO2 is going through a reduction process because of the same heat. This reduction process generates free oxygen which can act as fuel to the heat. More heat generated will help spread the crystallization to the whole dielectric. Eventually, oxygen and heat cause ignition of the whole device. This mechanism is illustrated in figure 1.8. [6,11,16]

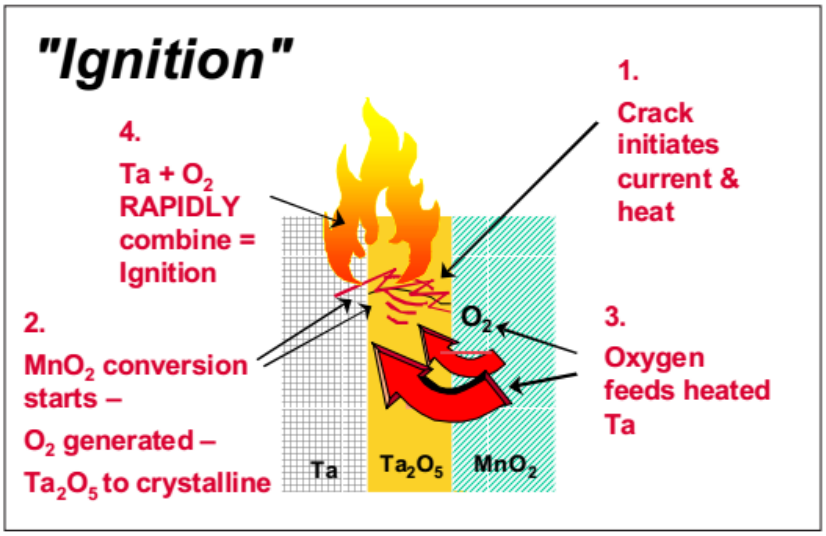

Figure 2.8: Theoretical ignition failure sequence [6].

This ignition reaction causes the capacitors to fail visibly with fire. The self-healing property of MnO2 is the reason for wide use of solid Ta capacitors. However, the excess oxygen in MnO2 readily serves as a source of failure in these capacitors. Also, high ESR of Tantalum

capacitors is also due to MnO2. So, for further improvement in performance of Solid Ta capacitors there was a need to find a substitute for MnO_2.

Conclusion

This chapter explains the basic capacitor theory, electrolytic capacitors, Tantalum capacitors with liquid electrolyte, and finally solid Ta capacitors. The disadvantages of Solid Ta capacitors with MnO_2 along with the growing demand for smaller and better performing capacitors has led to the next level of innovation in Tantalum capacitors. In the next stage, MnO_2 will be replaced by intrinsically conducting Polymers (ICP).

CHAPTER THREE

POLYMER TANTALUM CAPACITORS

Intrinsically Conducting Polymers

Intrinsically conducting polymers have conducting properties, unlike traditional polymers, with conductivity ranging between metals and insulators. These polymers have a conjugated structure, meaning alternate double and single bonds in the polymer chain, which are responsible for charge carrier conduction. Some examples of conducting polymers are Polyaniline, Polypyrrole, Polythiophene, Polyethylenedioxythiophene (PEDOT), Poly(p-phenylene ethylene)s [17].

Compared to inorganic semiconductors, these polymers have significantly different mechanisms for conduction. Carbon atoms in the polymer chain have SP_2-Pz hybridized orbitals and there two types of bonds involved in the polymer chain. Figure 3.1(a) [18] shows top view of two carbon atoms forming a sigma bond between their SP_2 hybrid orbitals. Three SP_2 orbitals of each carbon in the chain form sigma bonds with three adjacent carbon atoms. Figure 3.1(b) shows Pz orbitals involved in a π bond with an adjacent carbon atom and one carbon atom can form a π bond with only one atom at any instance. The π bonds shown in Figure 3.1 are present between adjacent atoms throughout the polymer molecule to form a delocalized electron cloud as shown in the Figure 3.2[19]. Solid blue line in the picture represents the polymer chain, with Carbon atom at each corner, and every carbon atom is bonded to the adjacent carbon atom with a sigma(σ) bond. Pi(π) bonds between the atoms throughout the molecule forms an electronic cloud represented by the yellow chain of ellipses above and below the carbon atom chain. Charge transport in this electron cloud takes place by a mechanism called hopping where the electrons hop from orbital of one atom to orbital of adjacent atom.

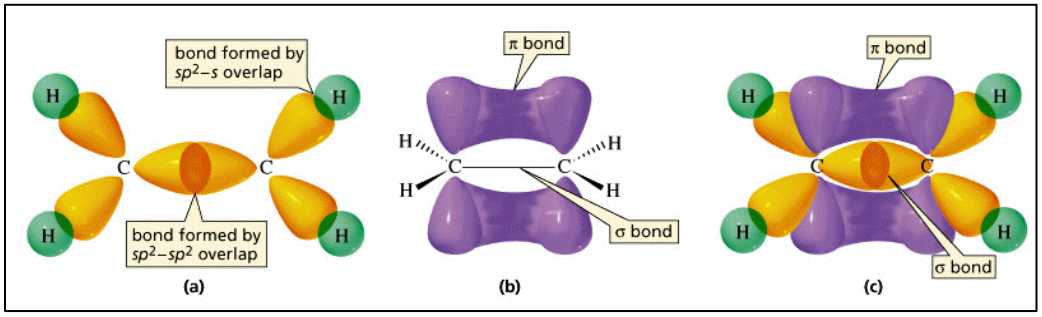

Figure 3.1: Sigma and Pi bonds between adjacent carbon atoms [18].

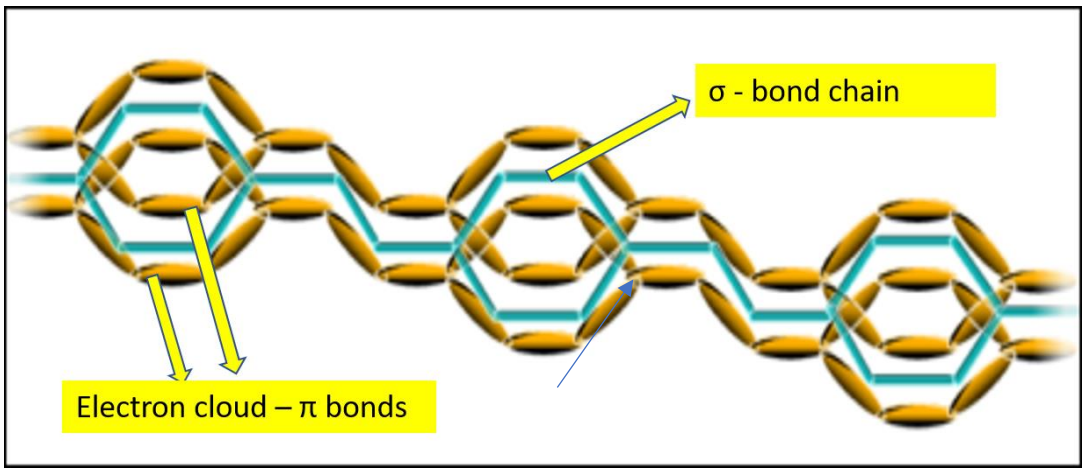

Figure 3.2: Delocalized electron cloud. Charge transport in the polymer chain takes place through hopping in the electron cloud. [19].

Conjugated polymers in their undoped or pristine state are semiconductors or insulators. Undoped conjugated polymer, such as polythiophene or polyacetylene, has a conductivity of around 10^{-10} to 10^{-8} S/cm. Upon doping, there is a rapid increase in electrical conductivity of several orders of magnitude up to values of around 10^{-1} S/cm, even at a very low level of doping such as < 1 % of polymer weight. Further doping of the conducting polymers result in a saturation of the

conductivity at values around 100-10,000 S/cm for different polymers. The highest values reported to date are for the conductivity of stretch oriented polyacetylene, with confirmed values of around 80,000 S/cm[20]. Considering the fact that the traditional polymers are insulators, the discovery and development of conducting polymers came as a major breakthrough for which three scientists A.J. Heeger, A.G. MacDiarmid and H. Shirakawa were awarded Noble Prize in 2000 [21].

Polymer as a Substitute For MnO_2

Though many advancements have been made to produce Ta caps with low ESR, MnO_2 remained the primary reason for high ESR. It has a resistivity of 2 to 6 Ohm-cm. Conducting polymers, which showed properties of high conductivity, looked promising to replace MnO_2 as cathode in Ta Capacitors. Poly (3,4-ethylenedioxythiophene), or PEDOT, is a well-known conducting polymer with high conductivity up to 500 S/cm and electrochemical stability. A water dispersion of PEDOT (typically at 1-3% wt. solids) doped with poly(styrenesulfonate) (PSS) to increase conductivity of PEDOT, is commercially available and considered for used in Polymer Ta capacitors [22]. PEDOT Polymer Ta capacitors showed much lower ESR over a range of frequencies (10kHz to 1000kHz) compared to Ta-MnO_2 capacitors[23].

PEDOT in polymer Ta capacitors also exhibits the self-healing effect, which is responsible for reformation of dielectric in electrolytic capacitors. There are two possible explanations for self-healing in polymer Ta capacitors, illustrated in Figure 3.3 [24]: (1) Evaporation of conductive polymer layer: Heat generated at the fault site causes evaporation of polymer layer, thus vacating the fault area and preventing further leakage current and dielectric damage; or (2) Oxidation of polymer layer: The heat generated near dielectric leakage paths causes a change of oxygen levels in the polymer resulting in an oxidized polymer with higher resistivity[24]. In either case a fault

correction mechanism is present in the polymer which served as another reason to replace MnO_2 with polymer as cathode in Ta capacitors. Thus, polymer began to replace MnO_2 as cathode.

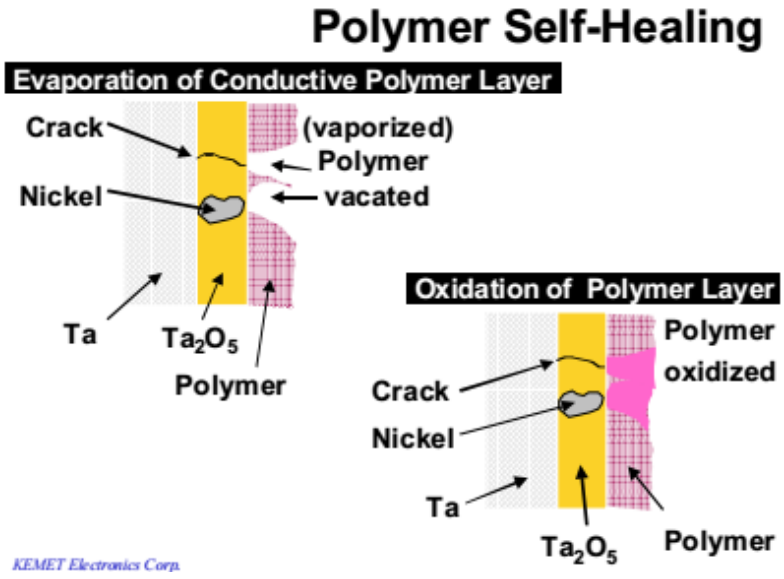

Figure 3.3: Self-Healing property of Ta capacitor with polymer cathode [24]

In-situ and Prepolymerized PEDOT Ta Capacitors

Traditionally, PEDOT is deposited by polymerization of 3,4-ethylene-dioxy-thiophene in the presence of iron III toluenesulfonate. Ta capacitors with the polymer deposited in this process are referred to as In-situ Ta polymer capacitors. As shown in Figure 3.4 [24], maximum working voltage of wet Ta capacitors was at 150V and MnO_2 based solid tantalum capacitors at 50V with the least working voltage belonging to in-situ Ta polymer capacitors was at 25V. As mentioned in Construction of Ta capacitors in Chapter 2, increasing the Formation Voltage should increase thickness of dielectric, which in turn should increase Breakdown Voltage. However, increasing the formation voltage in polymer Ta capacitors did not improve their breakdown voltage. BDV levelled off around 50V despite an increase in dielectric thickness [26]. This levelling of breakdown voltage

limited the working voltage, since the working voltage cannot be more than 50% of BDV in order to provide long-term stability and reliability [16].

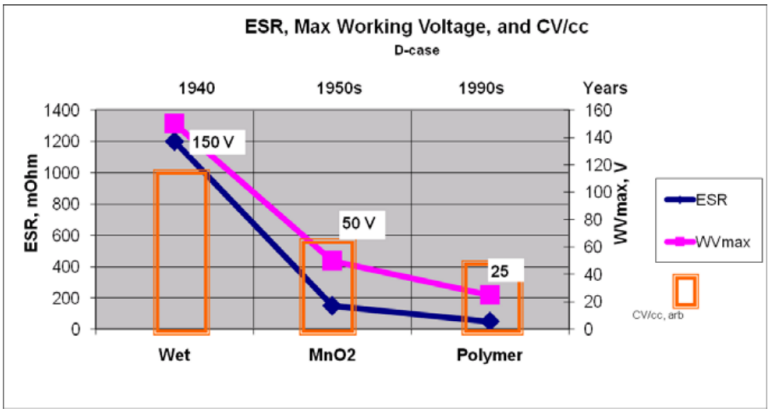

Figure 3.4: Maximum working voltage of Ta capacitors [24].

Eventually, this problem was solved by using a different polymerization technique. In this method, the PEDOT is polymerized before it is applied to the Ta pellets through a dip and dry process. This technique, referred to a pre-polymerization of PEDOT, resulted in a decrease in leakage current which in turn increases the BDV. Figure 3.5 shows the leakage current density in Pre-polymerized capacitors that remained low compared to current in In-situ Polymer Ta capacitors, which increased with bias. The pre-polymerization process possibly eliminated the stressing of the anode through repeated polymerization cycles as in the In-situ process, and this evidently increased the BDV [25]. Alternatively, since the particle size of polymer in pre-polymerized PEDOT is greater than in In-situ PEDOT pre-polymerization prevents penetration of PEDOT into dielectric macro defects [27].

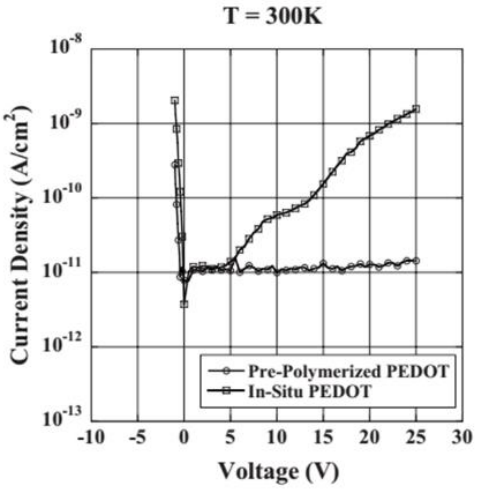

Figure 3.5: I-V characteristics of polymer Ta capacitors with in situ and prepolymerized PEDOT cathodes at T = 300 K. Anodic oxide film thickness was 200 nm [26].

MIS Model for Polymer Ta Capacitors

As discussed previously, several attempts have been made to explain the difference between In-situ and Prepolymerized Ta capacitors at a fundamental level [25,26]. At the material level, Ta capacitors essentially consist of numerous spherical Ta particles covered with oxide and then with PEDOT. That is; a metal anodized with an amorphous oxide which is then covered with a semiconducting polymer. This structure is well illustrated in Figure 3.6 where the capacitor is shown as combination of numerous spherical particles in 3.6(a), the detail of each spherical particle and the layers of metal (Ta), insulator (Ta_2O_5) and semiconductor (polymer) respectively shown in 3.6(b) & 3.6(c). This concept of the Metal-Insulator-Semiconductor (MIS) structure, as illustrated in Figure 3.6(c) is new to the capacitor industry, although it is familiar and well characterized in the microelectronics industry. This structure is similar to MOS capacitor structure studied in microelectronics, where gate is metal, SiO_2 is oxide and n or p-doped silicon serves as

semiconductor. Conducting C-V measurements on polymer Ta capacitors also concluded that these function essentially as MIS devices and also helped explain the better performance of pre-polymerized a capacitor compared to in-situ Ta capacitors [26].

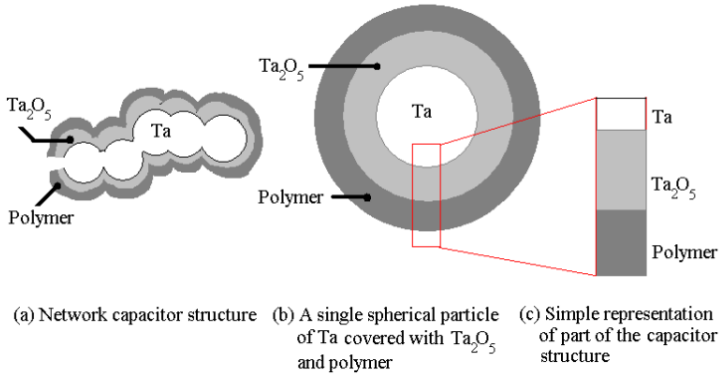

Figure 3.6: Simplified Ta capacitor structure for analysis [12]

Polymer Hermetic Sealed (PHS) Ta Capacitors

After Prepolymerized PEDOT, the next big leap in technological development came in the form of Polymer Hermetic Sealed (PHS) Ta capacitors. PHS capacitors are polymer tantalum capacitors with moisture sealed inside capacitor via hermetically sealing the device inside a package. After applying carbon and silver layers over the PEDOT layer, the capacitors go through a humidification process at a temperature of 85^0C and 85% relative humidity. This hermetic seal helps in maintaining the moisture inside the capacitor for long-term use. Retaining moisture inside the capacitor has also improved properties of DC leakage, ESR and stability [1].

A variant of PHS capacitors, referred to as low voltage PHS Ta capacitors, are formed at low formation voltage with thinner dielectric, uses finer tantalum powder and a hybrid polymerization technique involving both in-situ and pre-polymerization. Recently, KEMET discovered a new property of low voltage PHS Ta capacitors which was never seen before. This

property is Breakdown Voltage exceeding the Formation Voltage. Figure 3.7[1] shows breakdown test results of PHS capacitor formed at 28V, shown in red dotted line, and breakdown occurred at 50V. Such a phenomenon was never observed before in the 75 years of manufacturing and testing of Ta capacitors. BDV of a capacitor is directly dependent on thickness of dielectric among other factors, with BDV increasing with dielectric thickness. Since the dielectric thickness is proportional to Formation voltage, in theory, breakdown voltage is always less than formation voltage

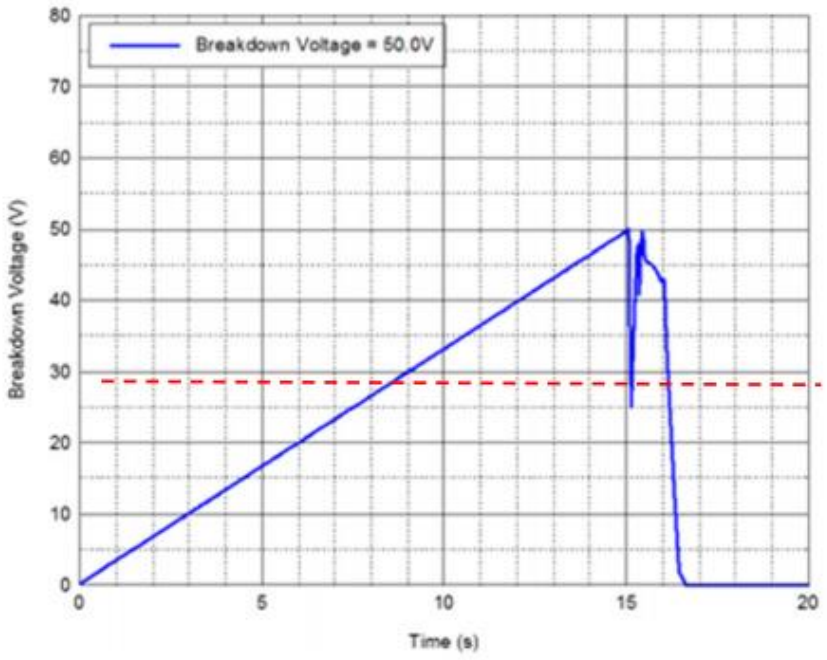

Figure 3.7: Breakdown test for PHS Ta Capacitor with V_f = 28V [1]

Phenomenon of BDV > V_f is possible and previously observed in Wet Ta capacitors and Polymer Ta capacitors due to extension of dielectric[28]. Though, in such cases the capacitance loss is observed due to an increase in dielectric thickness and more capacitors are used in the applications to compensate the capacitance loss. In the low voltage PHS Ta capacitors, even after breakdown the resistance of the capacitor was in the range of 0.1 – 1Mohms, an open failure mode

of capacitors in which current through the capacitor is cutoff unlike in a shorted failure where the current potentially destroys other components in the circuit. This combination of BDV>V_f without capacitance loss and open failure mode is critical for the applications where there is a limitation on space and number of capacitors and where short circuit current can prove to be costly.

Conclusion

Conducing polymer was reviewed in this chapter, detailing the advantages associated with replacing MnO_2 with PEDOT polymer. Advances in polymer capacitors and the analogy between polymer Ta capacitors and MIS devices was discussed. PHS capacitors was introduced along with some interesting aspects associated with these capacitors. In the next chapter we shall start with the reasoning for this research on PHS Ta capacitors and move onto measurements on capacitors provided by KEMET Electronics Corporation.

CHAPTER FOUR

CHARACTERIZATION OF PHS TANTALUM CAPACITORS

Background

As discussed in Chapter 3, Polymer Hermetic Sealed (PHS) Tantalum capacitors are the best Polymer Ta capacitors available today. PHS capacitors are being commercially produced and available in the market [29]. One of the crucial characterization methods used on PHS Capacitors, known in the industry as "Life Tests", are often performed on a random sample of capacitors to test their long-term operational stability and reliability under typical application conditions. Life Tests conducted in KEMET typically consists of subjecting the capacitors to their working voltage at 125^0C for 2000hrs. They are monitored and DC leakage current along with ESR were recorded at regular time intervals. Results are represented in the form of plots showing percentage of capacitors against the current or the ESR. For example, a point at (30%,10mA) on the plot represents that 30% of the capacitors have leakage current less than 10mA in the given set of capacitors. Results of the Life Test conducted in KEMET on one random sample of PHS Tantalum capacitors are illustrated in Figure 4.1 & Figure 4.2. Figure 4.1 shows the DCL characteristics of the capacitors, with a legend on the right side of plot detailing the icons for representing different stages at which leakage current was measured and the corresponding temperature. Current was measured before the experiment, after 250 hours, 500 hours, 1000 hours and 2000 hours. HOT stands for DC leakage measured at 125^0C and AMB stands for measurement at ambient temperature. Per the plot in Figure 4.1 after 500 hours, at ambient temperature 80% of the capacitors have a DCL current of 10μA or less and the remaining 20% reached 100mA. This high current indicates a dielectric breakdown and capacitor damage. From here the capacitors among this 20% will be referred to as capacitors which failed Life Test or failed capacitors.

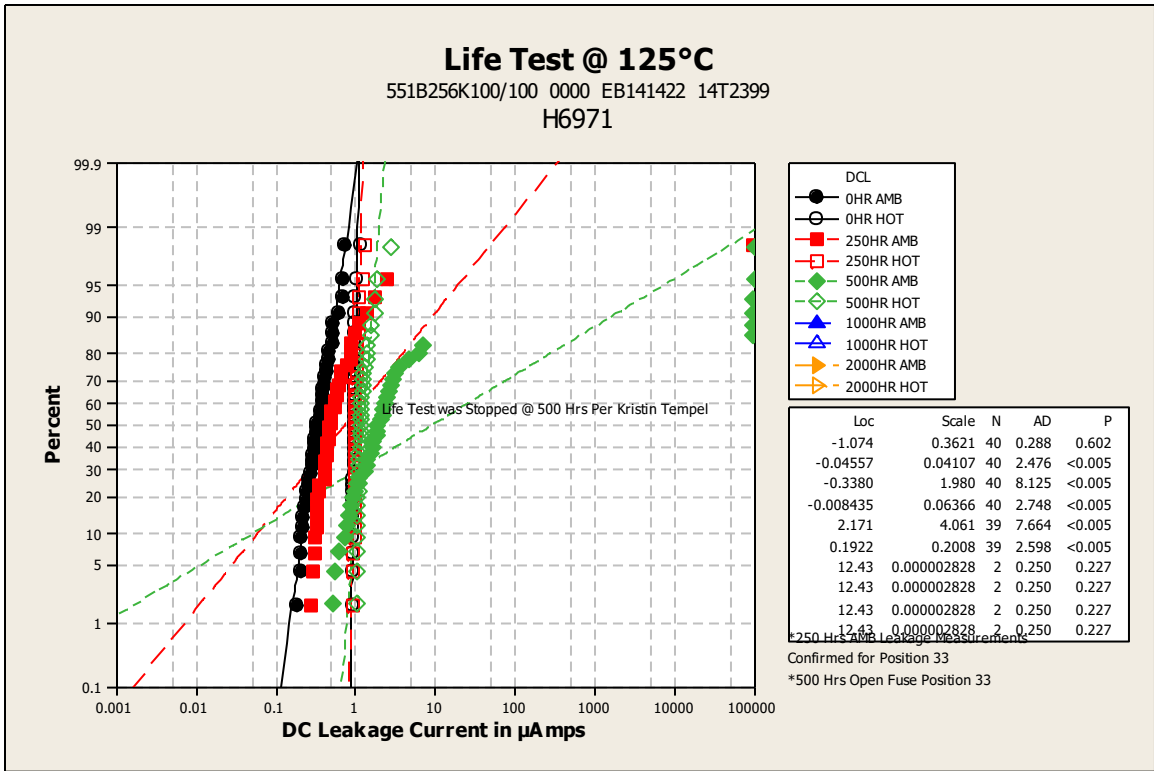

Figure 4.1: DC Leakage measured during Life Test. DCL after 500 hours in 80% of capacitors is less than 10µA, while in remaining 20 % it reached 100mA [Provided by KEMET]

In Figure 4.2 we see the ESR results of the same Life Test. The ESR in all capacitors remained less than one ohm even when the DC leakage current increased significantly. This type of capacitor failure with high DC leakage current and low ESR is called high-leakage/short failure mode in capacitors. It implies that whenever these capacitors see a dielectric breakdown, the anode and cathode terminals will get shorted and act as a path for high current. This uncontrolled high current has the potential to damage other components in the circuit and thus undesirable.

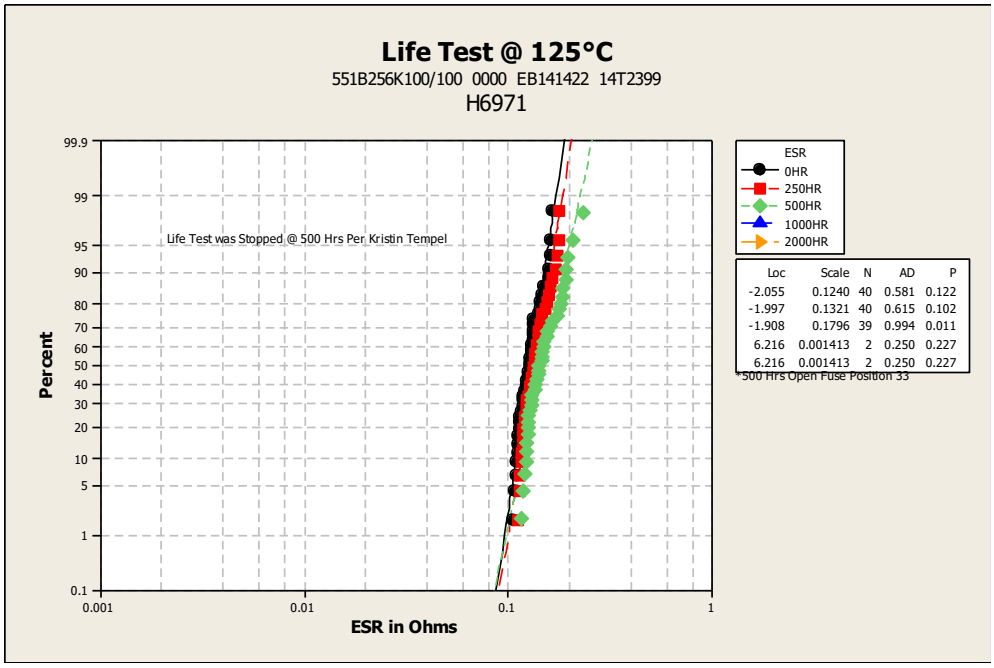

Figure 4.2: ESR of all capacitors remained less than 1Ohm after 500hrs even when 20% of these capacitors showed high DCL current. [Provided by KEMET]

This 20% failure rate shown in Figure 4.1 is considered very high by industry standards. To investigate this failure rate, a further study of these capacitors was considered necessary. The point of interest is to perform certain measurements to determine whether the capacitors which did not fail the test will still meet their specifications after the Life Test and if the failed capacitors behaviour was temporary or if they are damaged for sure. Results of these measurements are then compared with results from same measurements performed on Virgin samples, samples which did not go through Life Test, to determine if there are any inherent failure mechanisms present even before the Life Test was performed. Measurements at different temperatures with applied voltage will test the ability of dielectric in resisting breakdown failure and studying DC leakage at these

conditions would help understanding failure mechanisms. For this purpose, a plan was created to investigate current-voltage characteristics of these capacitors at different temperatures.

Measurement Procedure

Three sets of capacitors were provided by KEMET:

Set 1 : Capacitor samples which passed life test – "Good Samples".

Set 2 : Capacitor samples which failed life test – "Bad Samples".

Set 3 : Capacitor samples without life test – "Virgin Samples".

A measurement plan was created for the above three sets of capacitors at their rated voltage and at different temperatures. Rated voltage(U_R) is the "labelled" voltage of the device (capacitor), and it is defined as the maximum voltage at which the device can be safely operated at the rated temperature. As a standard industrial practice, Ta capacitors are usually operated at 50% of the rated voltage, a practice called as derating, to improve the long-term reliability and initial power on performance of the devices. The Rated temperature(T_R) is the temperature at which the device is expected to normally operate without lowering the voltage rating on the device. The device can also operate at temperatures higher than the rated temperature; however, in this case the capacitor voltage rating must be lower than the Rated Voltage. The maximum recommended operating temperature of a device is defined as the Category Temperature(CT), devices at this temperature must be operated by lowering the voltage rating than the Rated Voltage [30]. Maximum voltage the capacitor can be subjected to, at Category Temperature, is referred to as Category Voltage. The Category Temperature of the capacitors from KEMET is 125^0C, and Rated Temperature is 85^0C, the Rated voltage is 100V and the Category Voltage is 67V. The lower end of operating temperature

is -55^{0}C for these samples. All three sets of samples received from KEMET were measured at the full voltage and temperature range in the following manner:

1. 0-100V at Room temperature.
2. 0-100V at 85^{0}C.
3. 0-67V at 125^{0}C.
4. 0-100V in Liquid Nitrogen (LN2).

The focus is to obtain I-V characteristics of the capacitors under the conditions stated above. Leakage current in the capacitors in the range of milliamps would imply significant damage, and the devices would be classified as failures. I-V characteristics cannot be obtained by using the standard voltage sweep because in capacitors, at any voltage, when the voltage is changed the current will decay with time before reaching a steady state value, and so we must allow the current to stabilize before determining the DC leakage current. When the current stops decaying significantly with time, the capacitor system is assumed to have reached steady state. Time to reach steady state must be experimentally determined using an I-time(I-t) measurement, during which a constant voltage is maintained across the capacitor. The I-t characteristics taken for one hour for one of the samples measured at five different voltages was obtained and is shown in Figure 4.3. In Figure 4.3, current is decaying exponentially with time at a constant voltage following the standard relation between current and time in capacitors given by $I \, \alpha \, e^{-t/RC}$. To strike a balance between the measurement time required and the accuracy of the steady-state current, a delay of 600 seconds was selected for performing the measurements. So, at each voltage, the current was allowed to stabilize for 600 seconds before recording the current. Then, I-V characteristics of the devices were plotted.

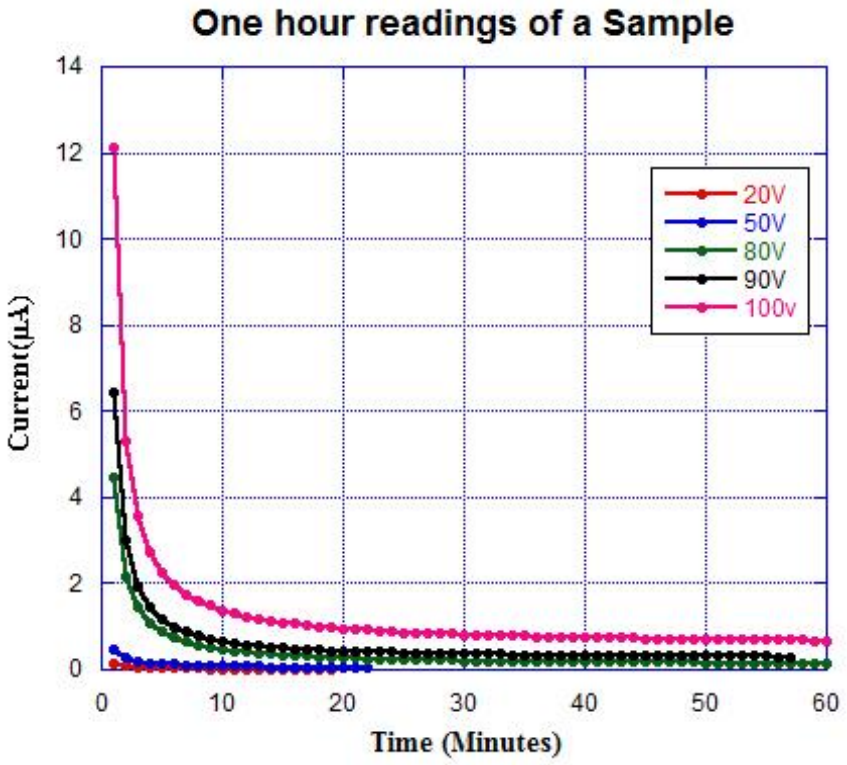

Figure 4.3: I-time measurement performed for one-hour to observe current decay.

Process automation

Since multiple capacitors needed to be characterized, which is a very time-consuming process, an automated system was used to collect the data. Schematic representation of the complete system is shown in Figure 4.4. As shown in Figure 4.4, capacitors were connected in parallel and a 100Ω resistor was placed in series with each capacitor to limit the current flowing through the capacitor. To implement this automated plan, capacitors were soldered onto a test board, resistors were soldered onto a separate perf-board and both connected in series. They are soldered on separate boards to keep the circuit board compact and have flexibility to transfer

capacitors to high temperature or low temperature setup. By using the Data Acquisition System(DAQ) - HP 3421A [31] it is easy to automate measuring voltage across several discrete components, for example, resistors. So, the voltage across each resistor, in series with each capacitor, was recorded by connecting the DAQ to a PC. The voltage measured across the resistor is then divided by resistance to obtain the current through the respective capacitor in series. Figure 4.4 illustrates the setup used to measure the voltage across resistors. Capacitor(C1) & resistor (R1) are in series, voltage across R1 is measured by connecting a line to port(P1) of the DAQ. Similarly, voltage across resistor in other capacitor-resistor combinations is measured by connecting to remaining ports of DAQ. This voltage data is transmitted to computer where the current in each branch is computed and stored to a text file. This data is then plotted by importing the data into the graphics tool, KaleidaGraph [32].

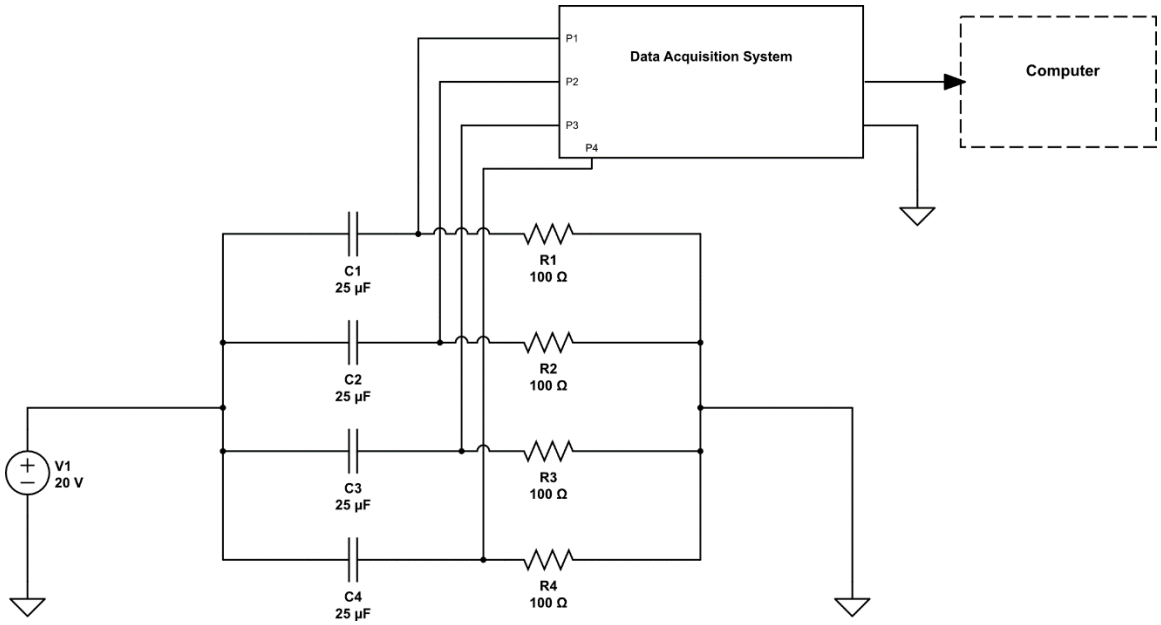

Figure 4.4: Automated system setup to measure voltage across the resistors, which was the used to measure DC leakage current through the capacitors.

High-Temperature Measurements:

High-temperature measurements were performed by placing flexible heaters insulated with polyimide film [33] above and below the test board in a vacuum container. Figure 4.5 shows the setup where a glass closing is placed on a platform, air is sucked from this closing using a vacuum pump through a hole in the platform. The temperature was controlled using the voltage applied to these heaters and temperature was monitored using a direct contact surface thermometer scale [34]. Figure 4.6 shows the test board with PHS capacitors soldered on them and a flex heater below it. Another flex heater will be placed over the test board during the experiment.

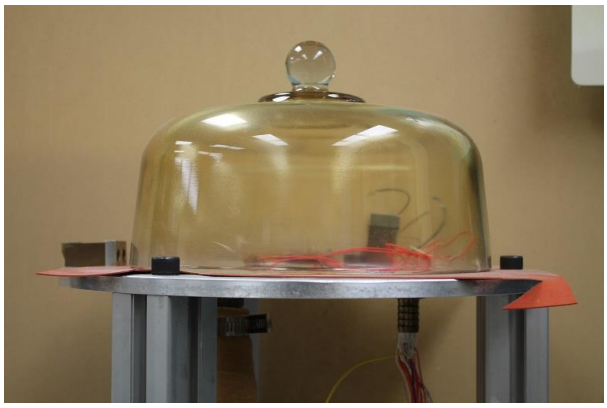

Figure 4.5: A vacuum chamber is created with this setup using glass closing and removing the air using vacuum pump.

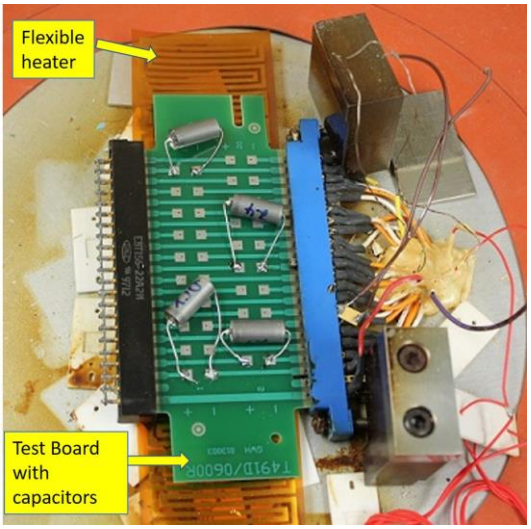

Figure 4.6: Flexible heater is place below the test board soldered with capacitors. During the measurements, another flex heater is placed over the test board.

Low-temperature measurements:

Low temperature measurements are similar to high temperature measurements except that the test board with capacitors placed in vacuum chamber was placed in liquid nitrogen. Liquid nitrogen was taken in a flask and the test board with capacitors was completely immersed in Liquid Nitrogen to expose capacitors to the low temperature. The temperature of the liquid nitrogen was monitored using a thermocouple. Voltage across the resistors and thus current through capacitors was then measured using the setup illustrated in Figure 4.4.

Results

I-V measurements were performed first on Set-1(Good Samples) followed by Set-2(Bad Samples) &3(Virgin Samples). Each set consisted of 3 capacitors which will be referred to as samples from now. Measurements were started under conditions where the scope for damaging the samples is minimal towards the more stressing conditions. Room temperature measurements will be performed first and last to compare and understand the effect of measurements on capacitors. The steps followed in the order are:

1. I-V measurements from 0 to 100V at Room temperature.
2. I-V measurements from 0 to 100V in LN2.
3. I-V measurements from 0 to 100V at 85^0C.
4. I-V measurements from 0 to 67V at 125^0C.
5. I-V measurements from 0 to 100V at Room temperature.

Set - 1

I-V measurements were performed at room temperature on Good Samples and the result of the measurement on Good Sample -1 is shown in Figures 4.7 & 4.8. In Figure 4.7, we see that the current reached a steady state after approximately 600 seconds. For each input voltage – 20V, 40V, 60, 80V & 100V, the corresponding current is recorded and then the corresponding I-V curve was plotted. The I-V plot for all three Good Samples is shown in Figure 4.8 and shows the current increased with the applied voltage. This is in line with a normal capacitor behaviour and this result imply that at room temperature Good Samples are in good working condition. The difference between the three capacitors is owing to differences in individual variations and the stress they have gone through during Life Test.

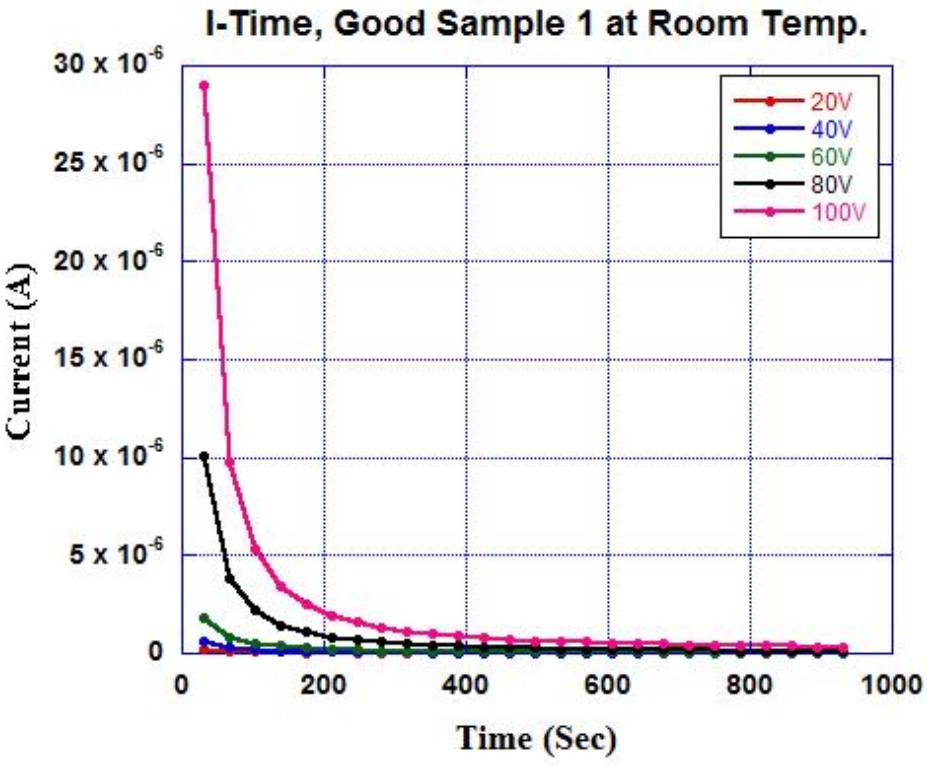

Figure 4.7: I-t of Good Sample-1 at Room Temperature for at different voltages.

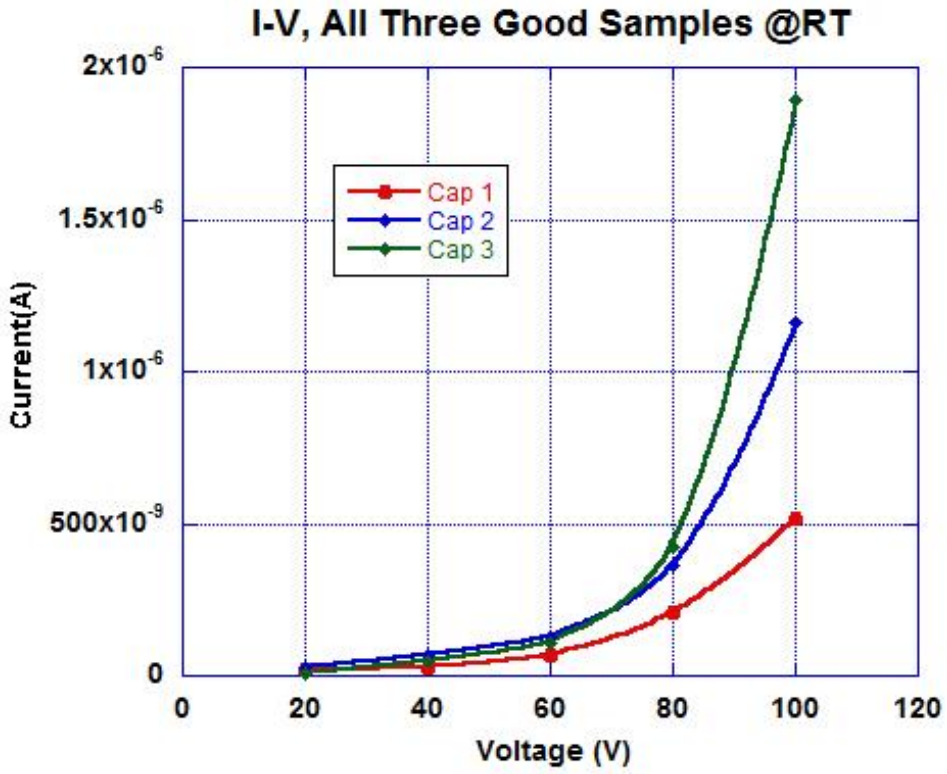

Figure 4.8: I-V of all Good Samples derived from I-time curves shown in Figure 4.7.

After the measurements at room temperature, the same I-time and I-V measurements were performed at 85C. The plots for these measurements are shown in Figure 4.9 and Figure 4.10. Plotting I-time measurements at 85C was expected to give exponential decaying curves as at room temperature similar to the plot in Figure 4.7 and obtained the same as shown in Figure 4.8. However, in Figure 4.9 notice that current at 100V in Capacitors 1 & 2 went down after 80V and in capacitor-3 the current at 100V reached the milliamp range and showing that point in plot would change the scale of plot and make the other curves difficult to interpret. The reason for current in Samples 1&2 at 100Vwas unknown at this stage but later figured out, it will be explained by the end of this chapter.

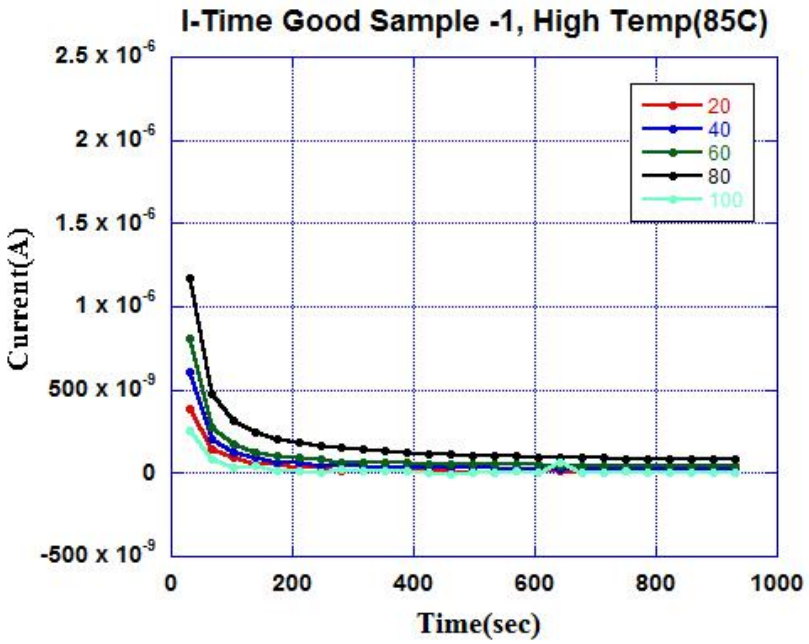

Figure 4.9: I-time of Good Sample-1 at 85^{0}C at different voltages.

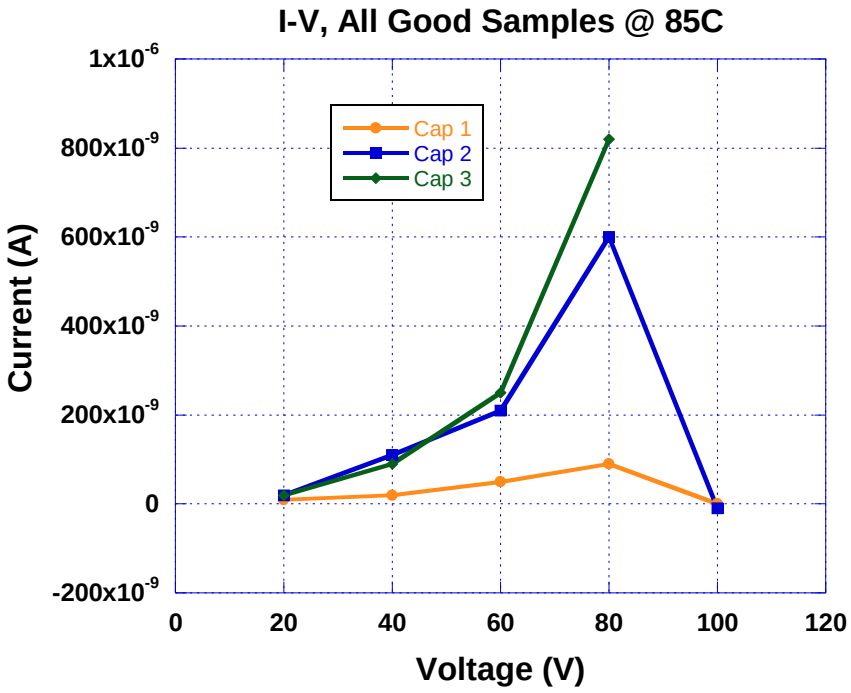

Figure 4.10: I-V of all Good Samples at 85^{0}C. Current for capacitor-3 reached milliamp range and not shown here.

I-time plots for Capacitor -1 at 125^0C and in Liquid Nitrogen are shown in Figure 4.11 and Figure 4.12 respectively. These results also represent of results for Capacitor – 2. At both temperatures, current remained below a milliamp. However, the current in Capacitor -3 continued to be in the milliamp range as can be seen in Figure 4.13 and Figure 4.14 for 125^0C and Liquid Nitrogen respectively. While the behaviour of Capacitors 1& 2 is not understood, leakage current in capacitor implies a dielectric breakdown. All these results will be later understood by end of this chapter.

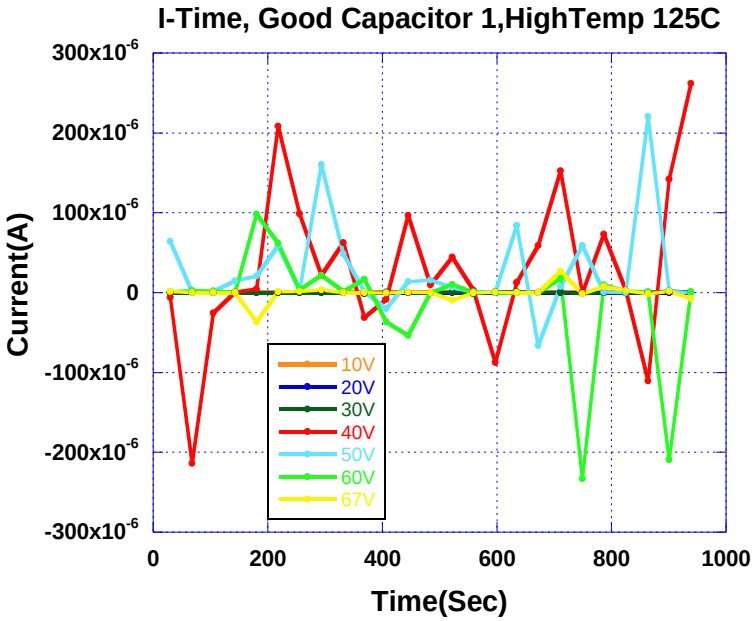

Figure 4.11: I-t of Good Sample-1 @125C. Current magnitude is irregular, and less than a micro-amp.

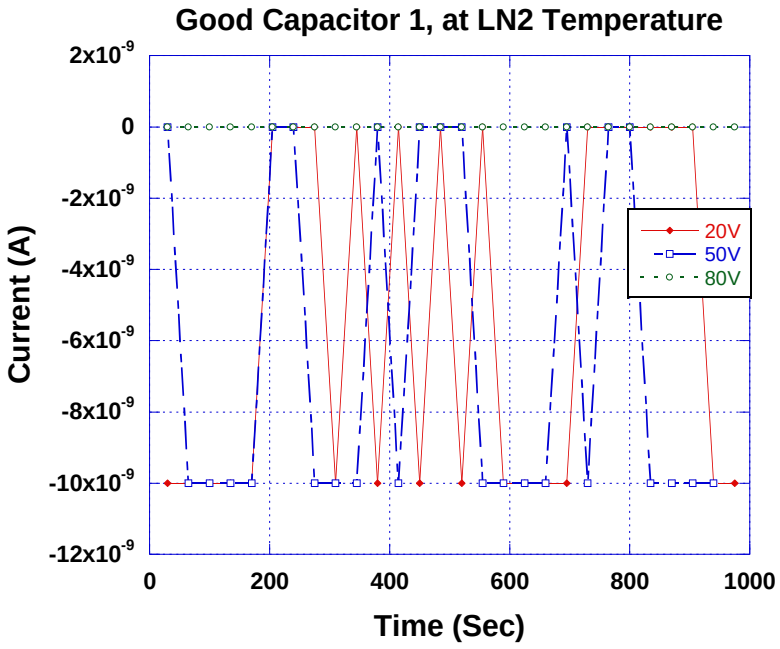

Figure 4.12: I-time of Good Capacitor-1 in Liquid Nitrogen. Current is in nanoamp range and irregular.

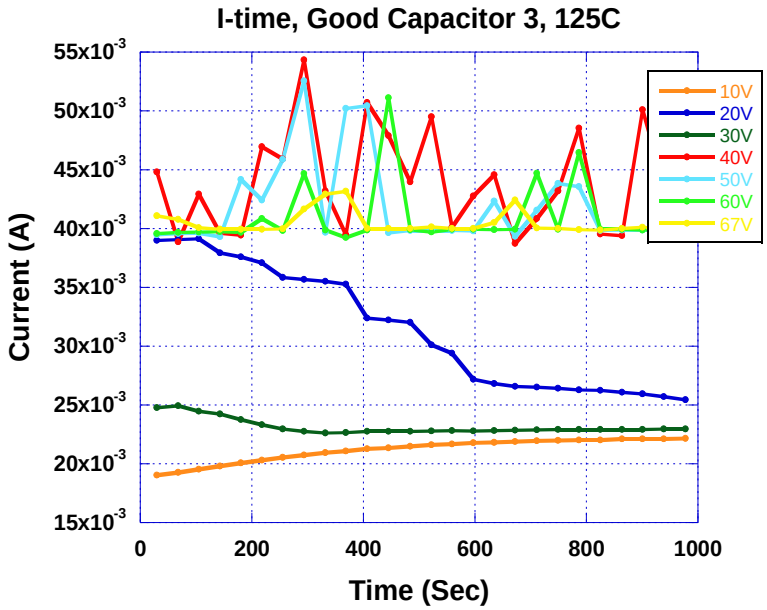

Figure 4.13: I-t of Good Sample-3 at 125^0C. Current pattern is irregular and in a milliamp range.

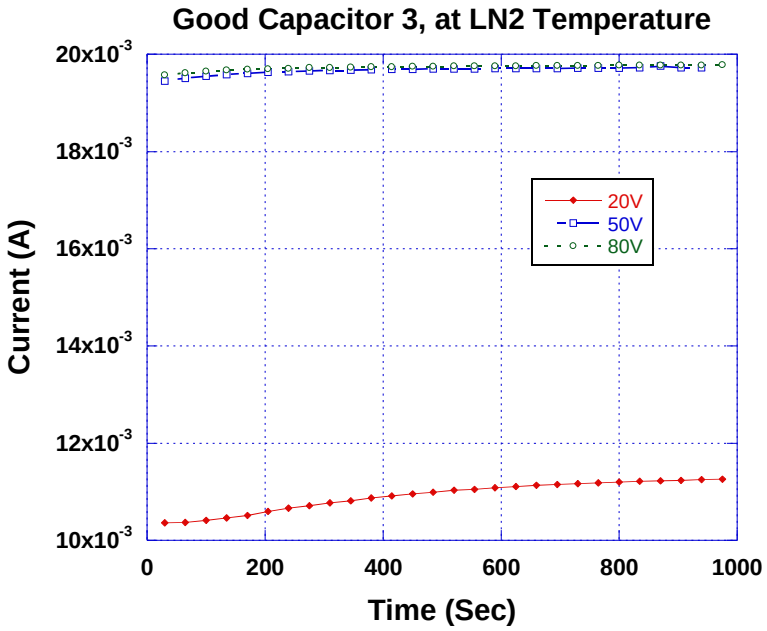

Figure 4.14: I-t of Good Sample-3 in Liquid Nitrogen. Current pattern is irregular and in a milliamp range.

Set 2

Measurements like the above were conducted on Set 2 - Bad Samples. Figure 4.15 shows I-t plot of Bad Sample-1 at Room Temperature. Unlike the typical exponential decay, current remained constant at any given voltage but increased with voltage. Similar behaviour was observed in other two capacitors in this set and at 85^0C and 125^0C. Plotting the current against the voltage and trying to correlate the current and voltage by using curve fitting in KaleidaGraph gave a correlation factor of more than 90%. This results shows the current and voltage are linearly correlated, an Ohmic behaviour like a resistor. The resulting plot is shown in Figure 4.16. Also, the current in all three capacitors is in milliamp range, indicating a dielectric breakdown. All these results of measurements on Bad Samples indicate that Bad Samples were definitely damaged during the Life Test and the impact of Life Test was not temporary.

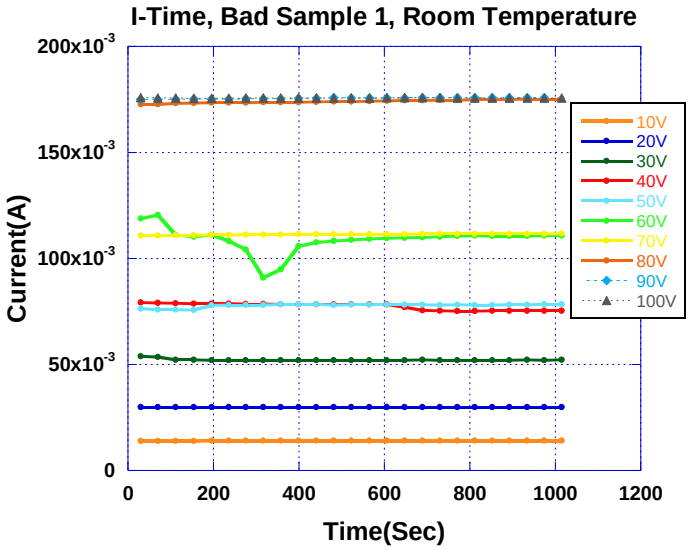

Figure 4.15: I-time of Bad Sample-1 at Room Temperature. Current all voltages is in milliamp range.

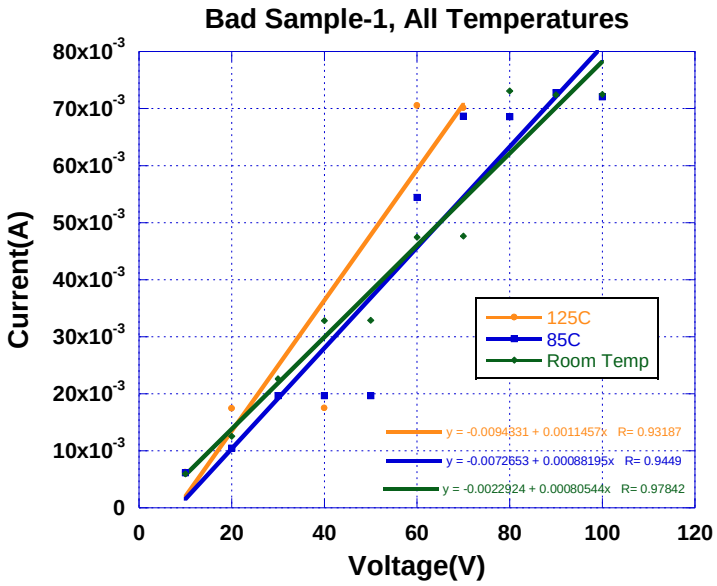

Figure 4.16: I-V of Bad Sample-1 at all temperatures. There is a linear correlation between current and voltage

Set - 3

This set of capacitors are Virgin samples which did not go through life test. Performing electrical measurements at Room Temperature, 85^0C, 125^0C and in Liquid Nitrogen, an exponential current decay was observed in the I-t measurements. The corresponding I-V curves at each temperature are shown in Figure 4.16. Leakage current is very low, in nanoamp range, indicating a reliable operation in a circuit. The non-exponential I-V curve is possibly influenced by noise associated with very low leakage current, and the sensitivity of the setup involved in measuring this leakage current.

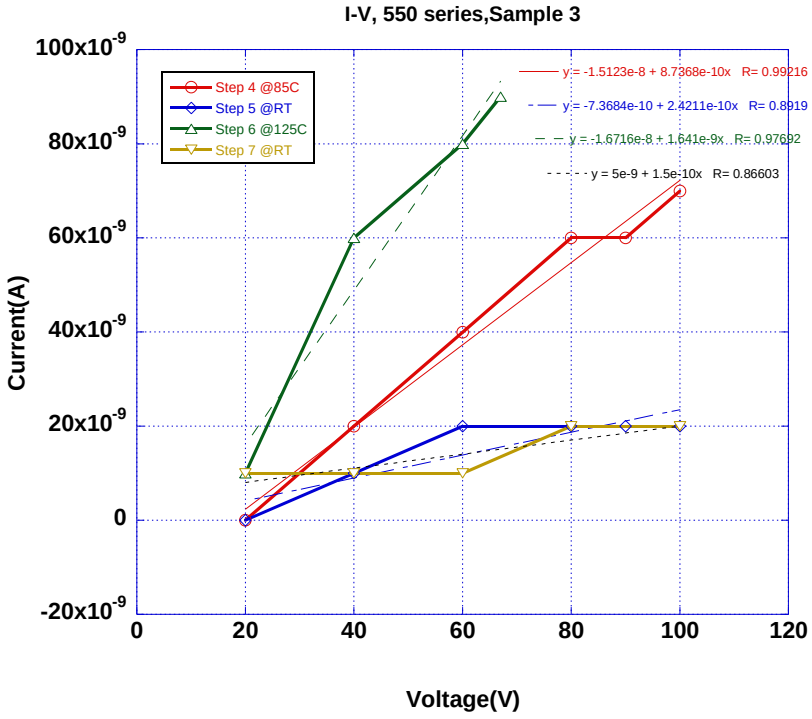

Figure 4.17: I-V at all temperatures, Virgin Sample – 3

Set – 4

Since the behaviour in Set 1 was not clearly understood, another set of Good capacitors which went through life test but did not fail the test were obtained and retested. This set will be referred to as Set 4. Number of steps in the measurements were increased to include room temperature measurements after every different temperature condition to understand the effect of previous step. Changes include taking readings not only when increasing voltage from 20V to 100V, but also from 100V to 20V to observe any hysteresis. Sequence of steps followed for the measurements are:

Step 1: Room temperature.

Step 2: In Liquid Nitrogen.

Step 3: Room temperature.

Step 4: At 85^0C.

Step 5: At room temperature.

Step 6: At 125^0C.

Step 7: Room temperature.

Figure 4.17 shows the result of Step 1 for sample 1. It's clear that the current increased with increasing voltage until 100V, however, there was a sudden drop in current after that. In Figure 4.18, at the same 100V, sample 2 current increased dramatically into milliamps range. The sudden increase in current in Sample 2 is because of dielectric breakdown. Both samples showed a sudden change in current at the same voltage. Close examination of the circuit revealed that the parallel connection of the capacitors in Figure 4.4 is the reason for the behaviour. At 100V when capacitor 2 got damaged (dielectric breakdown) it started drawing all the current serving as a short path to current in the circuit. So, the current in other samples dramatically decreased. When sample-2 was removed from test board to test the other samples, Sample-1 once again exhibited leakage current in nano-amp range. This explanation also helps understand the behaviour of capacitors in Set-1. In Figure 4.10 Capacitor 3 got damaged and shorted the circuit drawing all the current from remaining

two capacitors. All subsequent steps were influenced by capacitor-3 and current through remaining capacitor can be considered noise in the setup. In this set-4 all the samples got damaged in the subsequent steps revealing that even the good capacitors were effected by Life Test negatively.

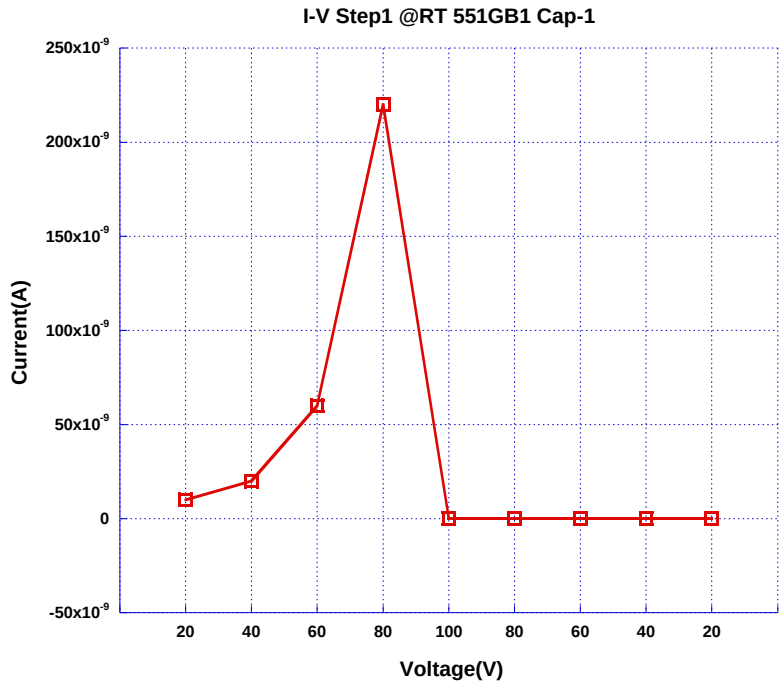

Figure 4.18: I-time of Good Sample-1 of set-4 at room temperature. Current at 100V dropped to zero and remained zero amps.

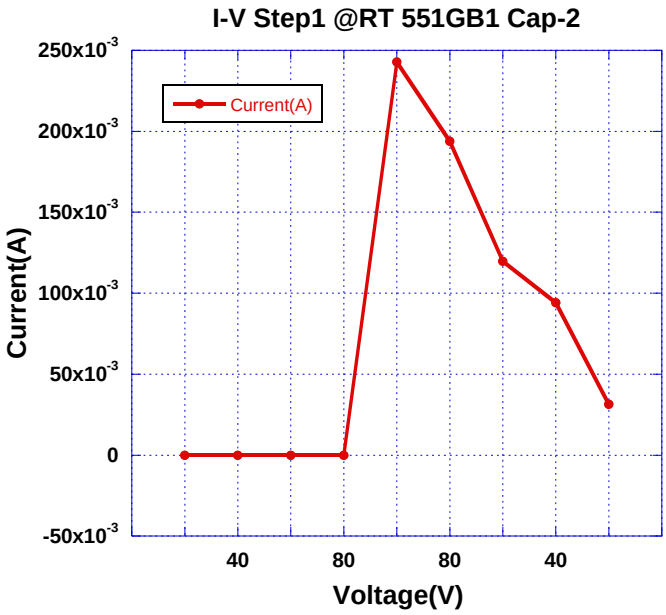

Figure 4.19: I-time of Good Sample-2 of Set-4 at Room Temperature. Dielectric breakdown occurred at 100V conducting milliamps of current.

Conclusion

The outcome of the measurements on 4 sets of Life tested PHS Ta capacitors is that bad samples are damaged for sure, and even the good samples that did not fail life test were negatively affected by Life Test. All the capacitors go through aging procedure to remove any manufacturing induced faults in the capacitor. By this aging, it is expected that the capacitors will have a long lifetime and operate at varied temperatures. However, even after aging process, the above samples failed during or after Life Test. It emphasizes the fact that a study of the fundamental structure of these capacitors is necessary.

CHAPTER FIVE

CHARECTARIZAION OF THIN-FILM SAMPLES

Motivation for Investigating Thin-Film Samples

By end of Chapter Four it was concluded that PHS Ta Capacitors, provided by KEMET, failed after going through Life Test to withstand their rated voltage over the temperature range under consideration. This emphasizes the need for improvement in fabricating these capacitors. Also, the high BDV of PHS Ta capacitors, as seen in Chapter 3, is an extraordinary phenomenon and has many practical applications, such as over-voltage capability without capacitance loss and open failure mode. But there is a lack of understanding of this high breakdown voltage phenomenon. To fully exploit this phenomenon and to further understand the observations from Chapter 4, it is necessary investigate the properties of Polymer Ta capacitors through their characterization.

First order modeling, such as depletion layer thickness near the IS (Insulator-Semiconductor) interface observed in MIS devices as a function of applied bias, is insufficient to understand this behavior [26]. These pre-polymerized PHS Ta capacitors represent a complex structure made from special F-tech anodes [36], coarse tantalum powder, thin dielectrics, and pre-polymerized PEDOT cathodes sealed with internal humidity. The primary question is to understand whether the characteristics of PHS capacitors are a result of the special manufacturing process and the resulting complex structure involved, or if it is primarily due to the nature of interactions between the organic and inorganic material layers present. If it is primarily due to the nature of interactions between the materials involved, then the properties of PHS capacitors can best understood by preparing thin-film representations of these PHS capacitors; and recreating the

material interactions without involving the complex structure. Otherwise, it can be concluded that the complex structure and the technology used to fabricate these capacitors is the primary contributor to the observed properties. In either case, the results from thin-film devices will be will be helpful to understand and ultimately improve the performance and applications of PHS Ta capacitors.

Fabrication of thin film devices

The stacking of material layers in the thin-film device should represent the real PHS capacitors as closely as possible. The structure of the thin-film device is shown in Figure 5.1(a). All the material layers are formed on a silicon wafer which essentially is the mechanical support for the devices. The starting material is a silicon substrate, and Ta is sputtered on its surface to serve as the anode. Subsequent layers of Tantalum oxide and polymer will be formed and finally a silver or aluminum contact over carbon surface will serve as the cathode, as shown in Figure 5.1(a).

4-inch intrinsic silicon wafers were purchased from University Wafer and forwarded to Georgia Tech for metal deposition. Tantalum was sputtered onto these Silicon wafers which were then diced into rectangular samples as shown in the Figure 5.1(b) at Institute of Electronics and Nanotechnology at Georgia Tech. Two sections of a 4 inch silicon wafer, which will be referred to as Flat Samples, were used for the current research. Both the flat samples, referred to as Flat Sample-1(FS1) and Flat Sample-2(FS2), were subjected to anodization in sulphuric acid at 85^0C with a 44V Formation Voltage(V_f). The formation voltage of 44V resulted in forming a dielectric of thickness 88nm at the rate of 2nm/Volt. After anodization, FS2 was subjected to heat treatment a procedure involving heating the samples at a predefined temperature for a fixed amount of time specified by KEMET Electronics Corporation. Later, PEDOT solution was deposited on both the

flat samples at four locations on each sample surface in the form of drops using a dropper and allowed to dry at room temperature for 24 hours. The four dots of PEDOT on each sample effectively form four capacitors with a common Tantalum metal anode. Carbon and silver layers were deposited by using a dropper to enhance the conductivity at the interface and to create a low resistance contact with external copper wires respectively. Flat samples were then heated to a temperature specified by KEMET. Capacitance of each capacitor on Flat samples was measured using an Agilent E4980A LCR meter and compared to the capacitance calculated using the known parameters.

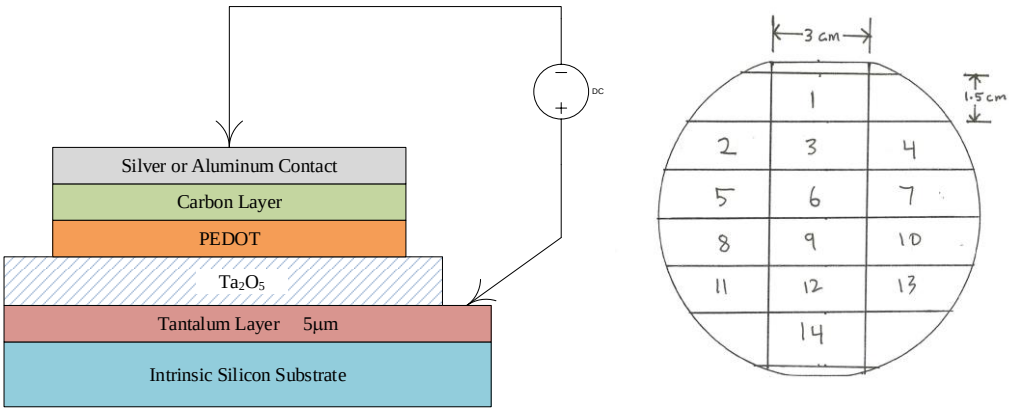

Figure 5.1: (a) Layers in the thin film device; (b)Dicing pattern for the Si wafers.

Figure 5.2 is photograph of Flat Sample – 1(FS1) with the four capacitors labeled along with their measured and calculated capacitances. The four capacitors are the four silver dots visible on the upper half of the flat sample. The other silver dot is the common anode. Kapton tape was used to separate the capacitors before applying the PEDOT preventing any contact between capacitors and to surround the epoxy cover the edges of the sample. Epoxy was used to prevent any

moisture come in contact with edges of the sample near the capacitors. We will adopt a convenient labeling such that, Capacitor-1 on Flat Sample -1 will be referred to as FS1-C1 and others are referred to similarly as FS1-C2, FS1-C3, and FS1-C4. The measured capacitance in the figure is measured at 120Hz using an Agilent E4980A Precision LCR meter. Calculated capacitance is estimated with the parallel plate model equation given by Equation 5.1, where $\varepsilon = 8.854 \times 10^{-12}$ F/m is the permittivity of free space - the dielectric constant is k = 26, the oxide thickness is d=88nm at 2nm/V_f ,and areas are A1 = 0.207×10^{-4} m^2, A2 = 0.12×10^{-4} m^2, A3 = 0.182×10^{-4} m^2, and A4 = 0.193×10^{-4} m^2 for capacitors C1, C2, C3 & C4 respectively. Areas were approximated by measuring the diameter of dots using a microscope and by assuming the dots are in circular shape. While C2, C3 and C4 showed consisted capacitance values with repeated measurement, the capacitance of C1 was not consistent. So FS1-C1 was not considered for any measurements.

$$C = \frac{\varepsilon * k * A}{d} \tag{5.1}$$

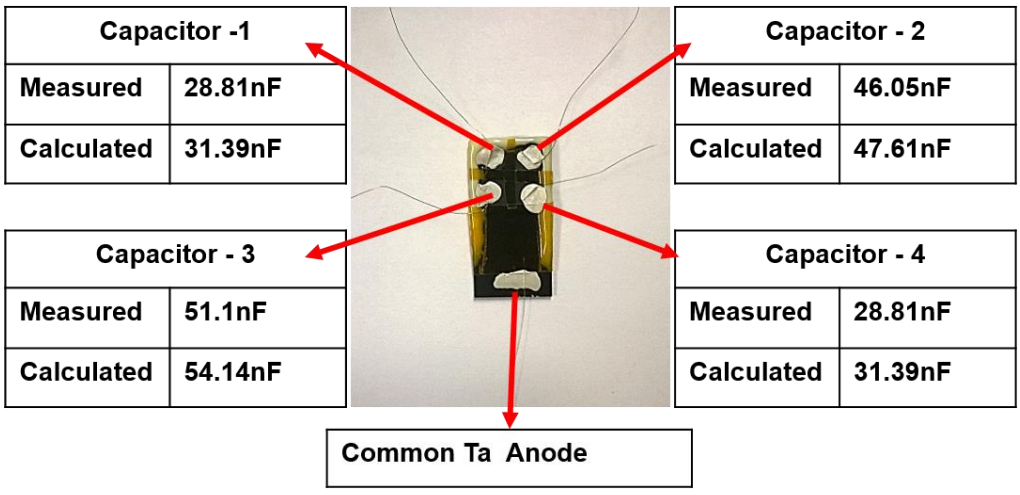

Figure 5.2: Flat Sample -1 showing 4 capacitors and their capacitance.

Figure 5.3 shows Flat Sample-2 (FS2) along with measured, and calculated capacitance values of each capacitor – FS2-C1, FS2-C2, FS2-C3 and FS2-C4. This flat sample, FS2, has gone through heat treatment similar to discrete commercial capacitors in KEMET facility. For FS2, only C2 and C4 showed consistent capacitance values upon repeated measurement, so all the measurements were performed only on these two capacitors. Approximate area of $0.2*10^{-4}m^2$ for each capacitor was used for calculating capacitance.

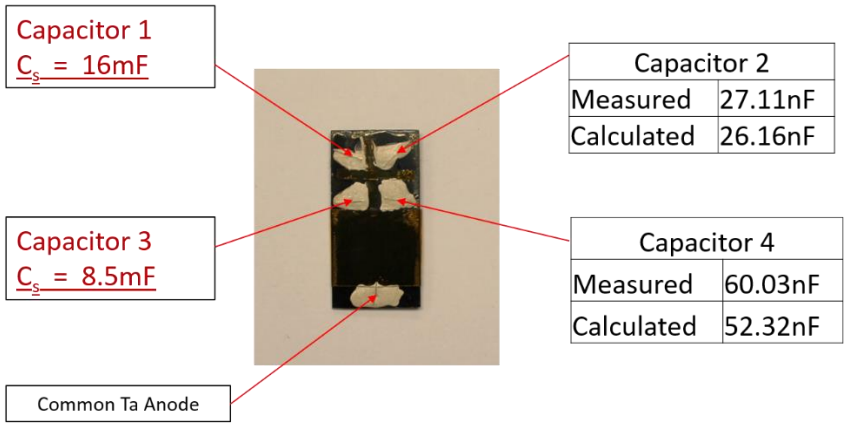

Figure 5.3: Flat Sample -1 showing 4 capacitors and their capacitance.

Experimental Procedure

The primary goal for this part of the research is to observe the behavior of these thin-film capacitors over the temperature, -55^0C to 85^0C, and voltage range, 0V to breakdown voltage of that capacitor. To protect the samples from damage, the order of measurements will be arranged to start with the procedure which will most likely cause the least amount of stress. I-V measurements drive current through the dielectric of the capacitor, and therefore have potential to cause dielectric

breakdown. Since the breakdown voltage is unknown in these virgin devices and experimental measurements could lead to dielectric breakdown, I-V measurements were performed last. Measurements of capacitance change with temperature was performed first. Capacitance was measured at 20Hz, 120Hz, and 1Khz both in low temperature range (Room temperature to -55^0C) and high temperature range (Room temperature to 85^0C). The results from both high temperature and low temperature measurements were normalized to room temperature and plotted as C(T) curves.

High Temperature Measurement Procedure

The flat sample was inserted into a plastic test tube and air sealed using a rubber stopper. Connecting wires and a thermocouple were inserted through the rubber stopper. The test tube and rubber stopper with a flat sample inside it are shown in Figure 5.4, without the thermocouple. The oven shown in Figure 5.5 was used to create a high temperature environment for the measurements. This oven reaches and maintains a temperature inside by regularly heating and circulating air. Oven temperature can be set by a resolution of 1^0C using the controls on the oven, highlighted in the picture. It has a provision for inserting a test tube, a circular hole of one inch diameter on the oven surface (not shown in picture), through which the test tube with the flat sample will be inserted as shown in Figure 5.5 . The temperature inside the tube was constantly monitored by using a thermocouple which was monitored using a digital multimeter. This setup is shown in the figure 5.4, where the equipment on the left is the heating oven into which the test tube is inserted by using a holding stand. The digital multimeter is visible in the picture in front of the stand with the thermocouple inserted into the test tube. For measurements, temperature was slowly changed using the controls on oven and at regular intervals the capacitance was recorded using an LCR meter.

Figure 5.4: Test tube used for high and low temperature measurements. White rubber stopper through the cap is used to maintain the temperature inside the tube.

Figure 5.5: High temperature measurement setup. The oven is on the left, and the tube with the flat sample is inserted into the oven. Oven controls highlighted in box.

Low Temperature Measurement Procedure

The low temperature measurement setup is similar to that of the high temperature measurement setup, except that the test tube was inserted into a low temperature chemical mixture prepared in a flask. The flat sample was sealed in the same test tube and contact terminals were pulled out through holes made in the rubber stopper. To achieve low temperatures, a mixture of Ethyl alcohol and dry ice was used. Since the surface temperature of dry ice is -78.5^0C and the freezing point of ethyl alcohol is -114.1^0C, when mixed together and stabilized we obtain a solution at temperature close to -78.5^0C. Ethyl alcohol was poured into a flask; dry ice was broken into small transferable pieces and slowly added to the flask and the dry-ice would start melting. We keep adding dry ice until the mixture reaches a stable state when dry ice stops melting and the flask is filled with the mixture. The tube was slowly inserted into the stable mixture, and the temperature inside the tube varied with the depth of immersion in the mixture. The temperature was monitored using a thermocouple attached to a digital Multimeter. Temperature in this setup doesn't remain constant very long due to the fact that the dry ice continues to melt; and either dry ice or ethanol are added to change the mixture temperature or the level of the test tube is raised or lowered to vary temperature inside the tube. The temperature was slowly changed, and at regular intervals the capacitance was recorded. This setup is shown in the Figure 5.6, where the dry ice and ethanol mixture are prepared in the blue flask shown.

Figure 5.6: Low temperature measurement setup. Chemical mixture is prepared in the blue flask on the left.

Results

Flat Sample -1

Measurements were started with Flat Sample-1 which did not go through the heat treatment. Capacitance variation with temperature, C(T), for each capacitor on the flat sample was measured following the procedure described in the previous two sections: High Temperature Measurement Procedure and Low Temperature Measurement Procedure. C(T) measurements were first performed at 120Hz, then at 20Hz and 1000Hz. C(T) results are presented in a plot along with a normalized C(T) plot, normalized with respect to room temperature(20^0C) capacitance, as shown in Figure 5.7 & Figure 5.8 respectively. Both figures show C(T) plots for FS1-C4, and these results are representative of the other capacitors on Flat Sample-1.

From Figure 5.7 we see that at low temperatures the loss in capacitance is less than 20%; however, at higher temperatures the capacitance increases at a much higher rate with high dependence on frequency. At 20 Hz, the change in capacitance is highest at more than 300%, while at 120Hz and 1000Hz it is around 200% and 50% respectively. The percentage change in capacitance at this rate was never observed before and needs to be explored to understand the reason.

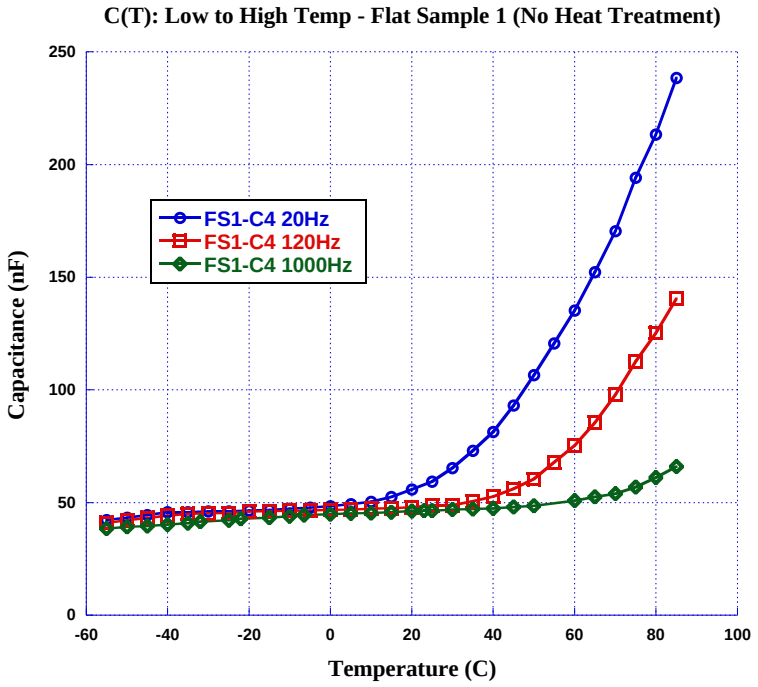

Figure 5.7: C(T) of capacitor-4 in Flat Sample-1.

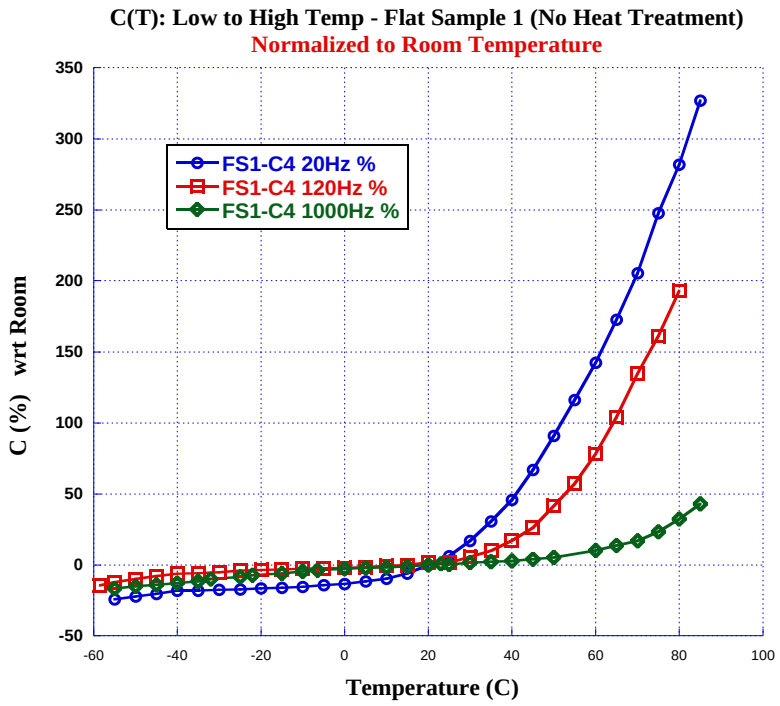

Figure 5.8: %C vs Temperature for capacitor-4 in Flat Sample-1

C(T) was not measured in any particular order of frequency or choice of capacitor on the flat sample. Since the sample went through repetitive heating during separate testing of the three capacitors on same flat sample, the high capacitance change could be because of cumulative heating. The next logical step was to investigate this possible cumulative effect and also verify the reliability of these measurements by repeating them. The equipment and the setup remained the same, and only the procedure was varied. For the next measurements the capacitance was measured at the same time for all three capacitors on the Flat sample-1, and at all three frequencies, while maintaining the temperature. Maintaining the same temperature while recording capacitance of all capacitors and at all three different frequencies was a challenge since the temperature was slowly changing. Instead of trying to reach a very specific temperature, the temperature was allowed to

completely stabilize close to desired value before any measurements were recorded. For this reason, measurements were recorded at non-uniform intervals. Measurements were recorded from room temperature to high temperature or low temperature, and then back to room temperature.to observe the presence of hysteresis. Results of these measurements are shown in Figure 5.9 and Figure 5.10. They show C(T) and percentage change in C(T) for capacitors FS1-C2 & FS1-C4 at 120Hz. Both figures show the high capacitance change of more than 100% at high temperature. During the measurements, the copper wire connected to the cathode of FS-C3 came off and could not be restored, so results of only two capacitors out of three are shown in these Figures. Finally, the primary observations from all the measurements on Flat Sample-1 are:

1. Capacitance change is very large at high temperatures compared to low temperatures.
2. All the results are repeatable.
3. Capacitance change is also significantly dependent on frequency.

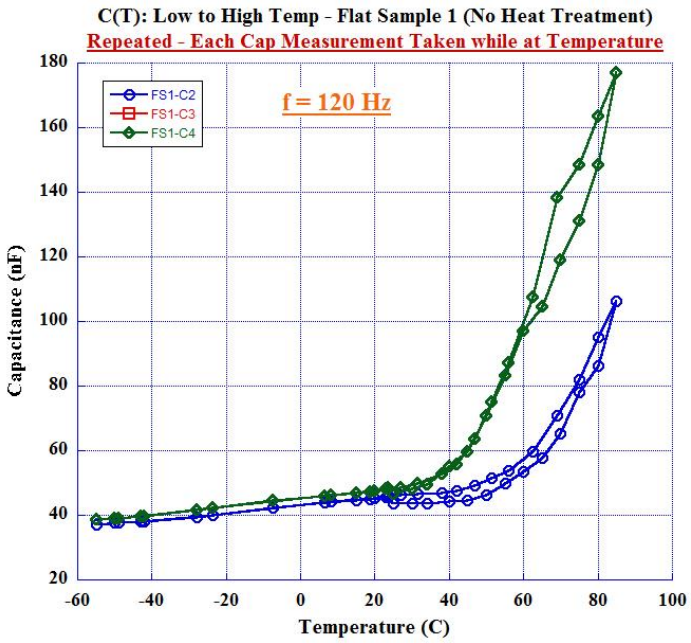

Figure 5.9: C(T) of –Flat Sample 1, repeated measurements

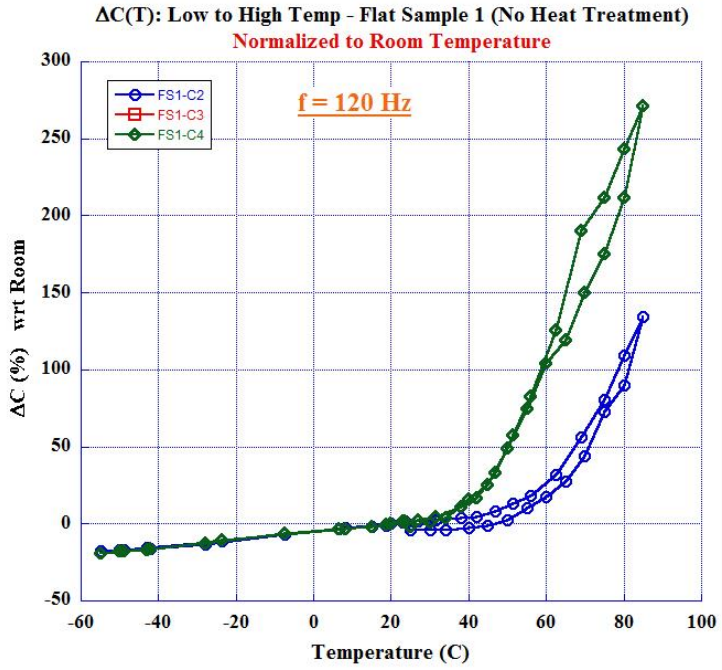

Figure 5.10: ΔC(T): Low to High Temp, Flat Sample 1, repeated measurements

Flat Sample - 2

The same procedure established for sample 1 was followed for Flat Sample-2. Sample-2 is different from FS1 in that FS2 has gone through the heat treatment, the process in which the sample was heated for a period and at temperature specified by KEMET before PEDOT was deposited and after oxide was formed. The capacitance as a function of temperature of two capacitors, C2 and C4 on sample-2, was measured at same time, at 20Hz, 120Hz, 1000Hz and 10kHz frequencies from room temperature to high and room temperature to low and back again to room temperature in both cases to show any hysteresis effects. The results are shown in Figures 5.11, 5.12, 5.13 & 5.14. At both the high temperature, Figure 5.11, and low temperature ranges, Figure 5.12, FS2-C2 showed less than a 20% change in capacitance with little dependence on frequency. However, for FS2-C4, shown in Figure 5.13 and 5.14, anomalous result were observed at low frequency yielding a high capacitance. This anomaly disappeared when the same measurements were performed after drying the samples. Any residual moisture present in sample might have contributed to this behavior which disappeared after heating. These results are significantly different from the results observed in FS1 where there was a much stronger effect of temperature and frequency. This difference is most likely due to the heat treatment performed on Flat Samle-2.

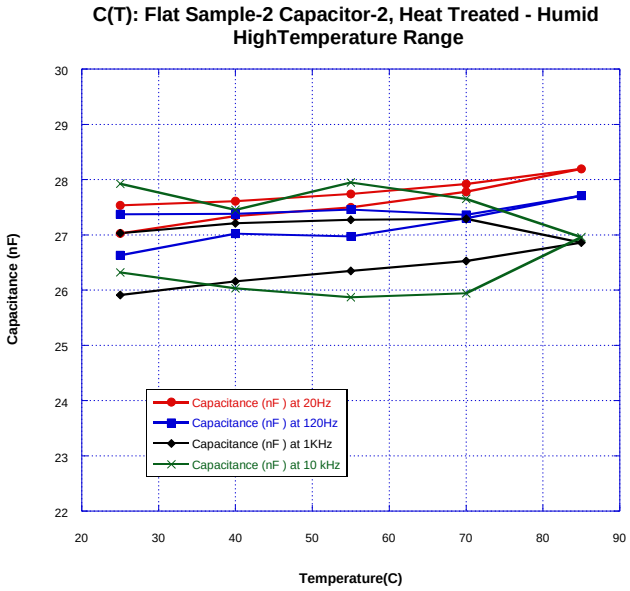

Figure 5.11: C(T) of FS2-C2 at High Temperature. Change in capacitance is less than 20%

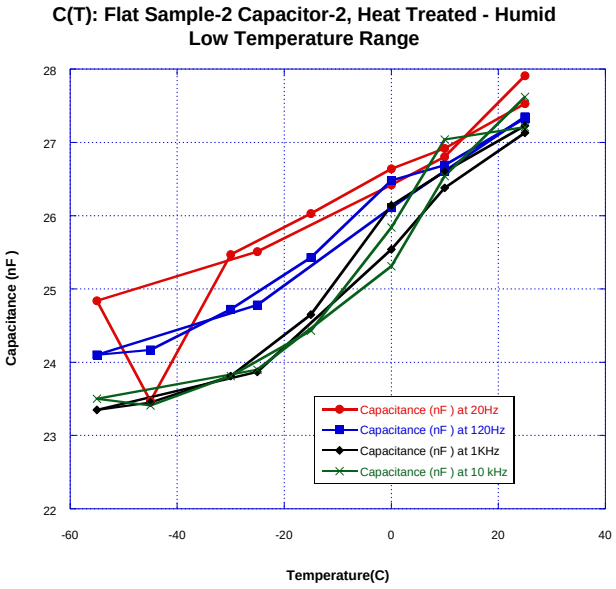

Figure 5.12: C(T) of FS2-C2 at Low Temperature. Change in capacitance is less than 20%

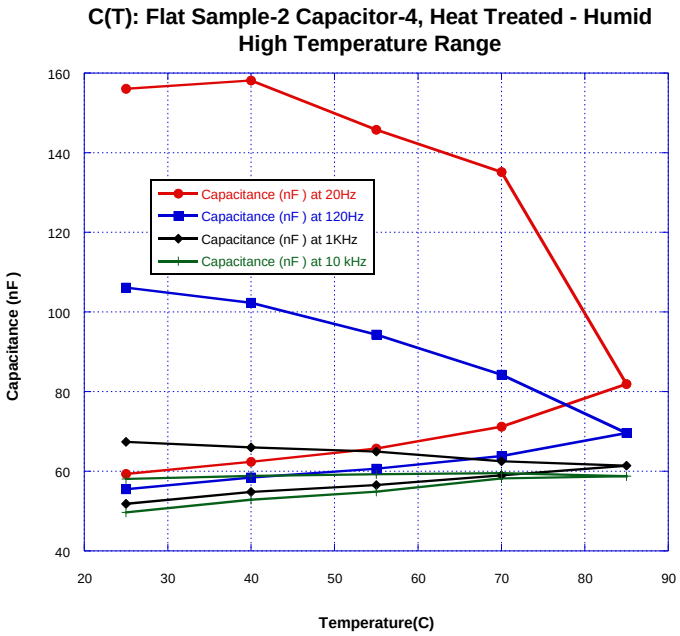

Figure 5.13: C(T) of FS2-C4 at high temperature. Capacitance at 20Hz is very high.

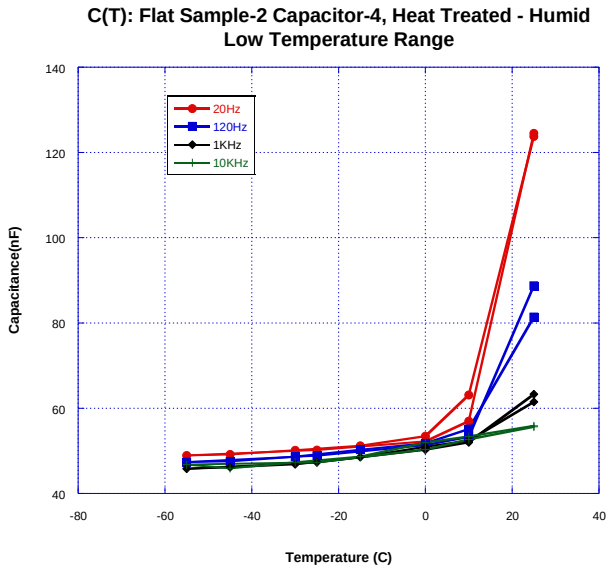

Figure 5.14: C(T) of FS2-C4 in low temperature range. The unusually high capacitance at 20Hz disappeared after drying the sample.

Drying the samples

To test the effects of humidity on the behavior of these thin-film capacitors, it was decided to dry the samples and then compare the results with those before drying. For the drying process, samples were left in a dry cabinet filled with Nitrogen gas for 24hrs to remove all moisture from the samples. All the measurements performed on Flat Sample-1 and Flat Sample-2 before drying were repeated on the dried samples. To further investigate the correlation between capacitance and frequency, capacitance was also measured at 10kHz. Here the results are compared between one capacitor on FS1 and one capacitor from FS2. Comparing the results yielded new insights.

Figure 5.15 shows the measured C(T) results from FS1-C4 after drying, while Figure 5.7 shows C(T) of the same sample before drying. In both cases, there is an increase in capacitance with heating as well as a dependence on frequency. The capacitance change is much less in the dry sample than in the humid sample. For example, at 20Hz frequency the measured capacitance was just below 150nF for the dry sample, while it was nearly 250nF before drying. Although the frequency dependence observed for all samples both dry and humid was a decrease in capacitance variation with temperature as frequency increased, the sensitivity was reduced significantly in the dry samples.

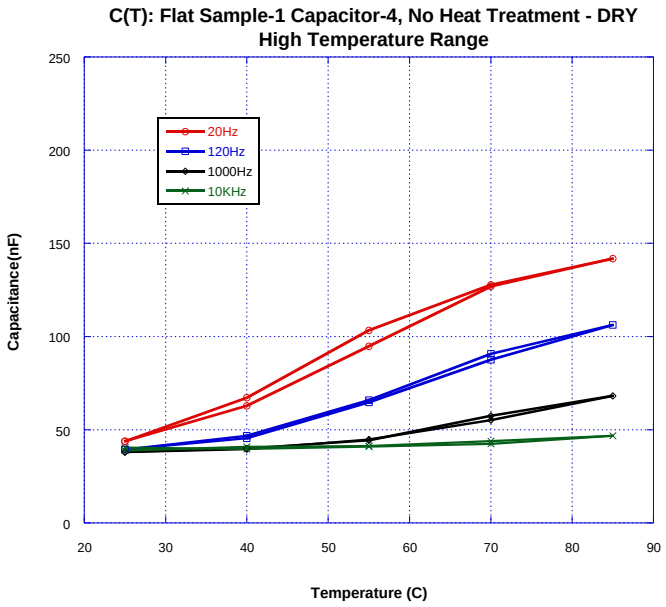

Figure 5.15: C(T) of FS1-C4 in the high temperature range with drying

Similarly, Figure 5.16 shows the measured C(T) results for FS2-C2 after drying in the high temperature range. Comparing Figure 5.16 and FS2-C2 results before drying, shown in Figure 5.11 it is observed that there is essentially no difference in the capacitance change with temperature between these two figures and so there is no significant effect of drying on this heat-treated sample. The result is similar even in low temperature range, compare Figure 5.12 and Figure 5.17. However, comparing results of FS2-C4 after drying, shown in Figure 5.16 with results before drying, shown in Figure 5.12, and comparing Figure 5.13 with Figure 5.18 shows that drying the sample removed the high capacitance anomaly observed in this capacitor at low frequency. Any traces of moisture near the capacitor must have contributed to this behavior. Finally, it is clear that removing moisture from samples by drying has an effect of decreasing the capacitance change, especially at low frequency. In the heat-treated FS2, the effect of drying is less compared to that of the humid FS1. All the observations of C(T) measurements will once again be summarized at the end of this chapter.

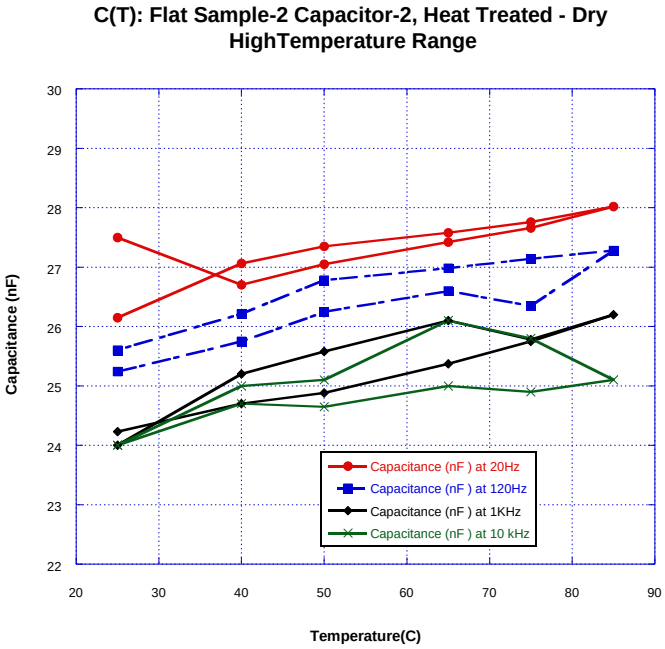

Figure 5.16: C(T) of FS2-C2 in the high temperature range after drying

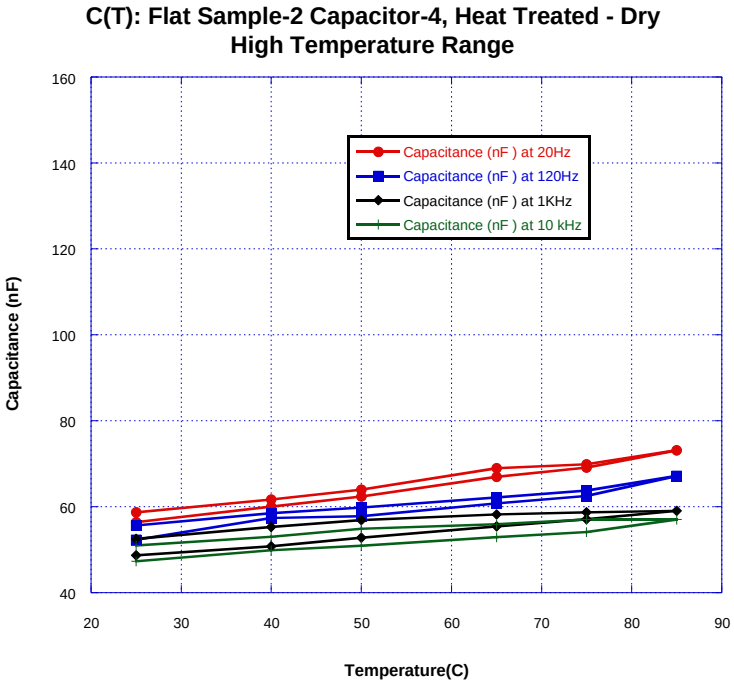

Figure 5.17: C(T) of FS2-C4 in high temperature range after drying

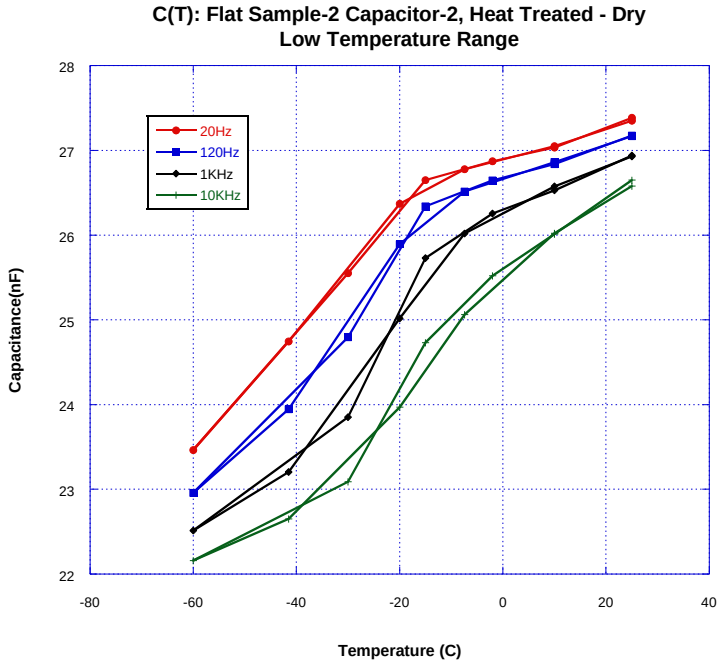

Figure 5.18: C(T) of FS2-C2 in low temperature range after drying

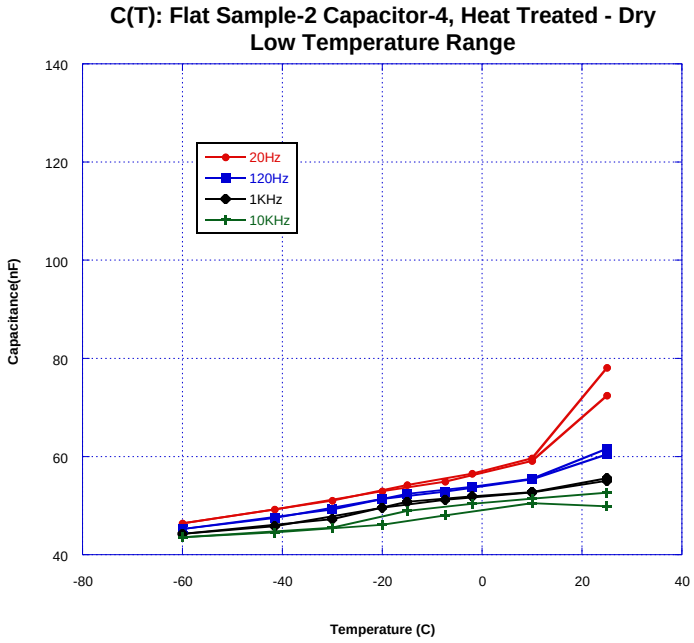

Figure 5.19: C(T) of FS2-C4 in low temperature range after drying

Breakdown Voltage

Breakdown voltage is another point of interest, to know if property of breakdown voltage exceeding formation voltage is inherent to materials involved or the complex structure of PHS Ta capacitors. Before stressing the devices to voltage, leakage will be measured to determine if the dielectric layer in intact. Leakage current in and above milliamp range will be considered an indication of dielectric damage. Leakage current was measured using an HP 4156B Precision Semiconductor Parameter Analyzer. A quick measurement with +2V bias resulted in leakage current between 30nA-50nA, indicating stable dielectric in all four capacitors – FS1-C2, FS1-C4, FS2-C2 & FS2-C4. Determining the breakdown voltage was started with FS1-C2, sample without heat treatment. Since the breakdown voltage is unknown, a voltage sweep of 0V to 10V was applied. When breakdown did not occur, voltage sweep was increased by 10V increments. Leakage current from 0-50V for FS1-C2 is show in Figure 5.18. Leakage current remained low until about the 20-30V range, after which it started to increase approximately linearly until about 50V, which was the maximum voltage set in the parameter analyzer. Repeating this I-V measurement but setting the maximum voltage to 60V led to dielectric breakdown at 57.5V with the leakage current reaching milliamp range. Corresponding I-V plot is shown in Figure 5.19 with the parameter analyzer set to stop the measurements at 5mA. The Breakdown voltage (BDV) for the remaining capacitors was determined by allowing the voltage to increase until the breakdown occurs. BDV for all four available capacitors is shown in Table 5.1. Capacitors without heat treatment (FS1), which are similar to PHS Ta capacitors, had a BDV greater than the Formation Voltage of 44V, as observed in PHS Ta capacitors. Breakdown voltages in capacitors with heat treatment were observed below the Formation Voltage.

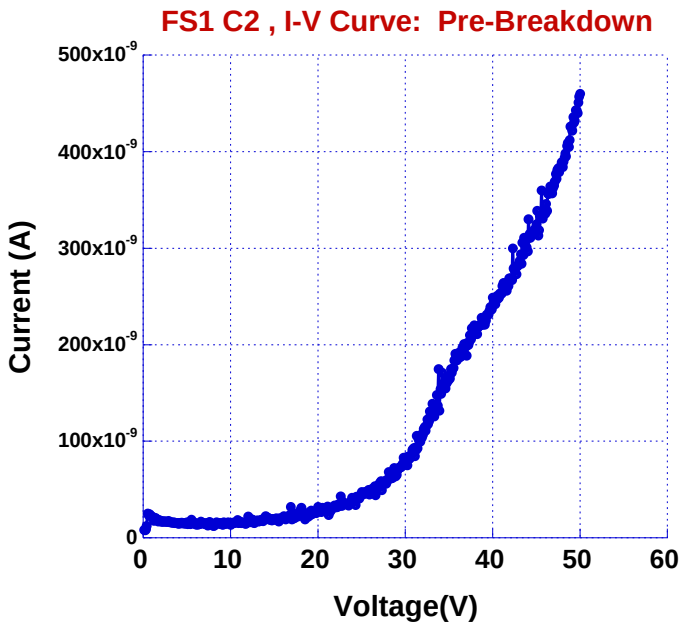

Figure 5.20: Pre-breakdown current in FS1-C2, no heat treatment, Humid.

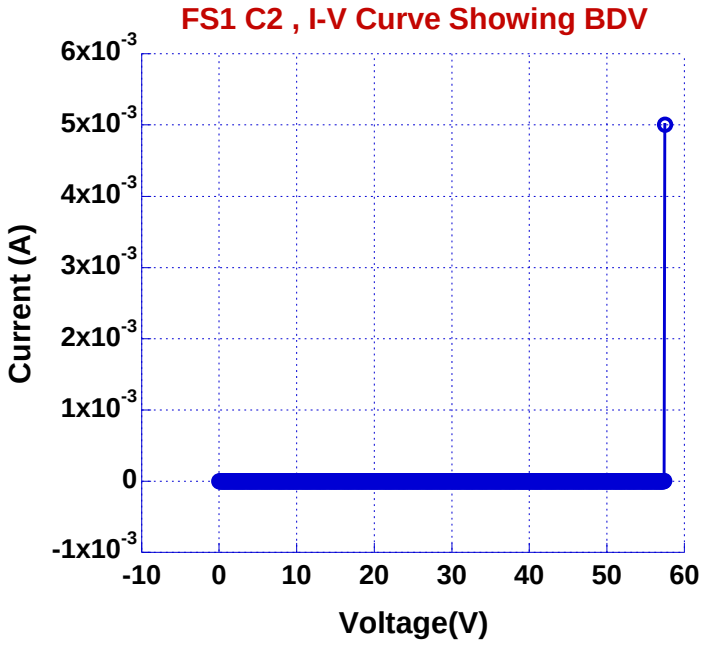

Figure 5.21: I-V plot showing the breakdown at 57.5V in FS1-C2, no heat treatment, Humid.

Capacitor	Breakdown Voltage
FS1-C2	57.5
FS1-C4	57.0
FS2-C2	5.5V
FS2-C4	30V

Table 5.1 : Capacitors with their corresponding BDV. FS2 is heat treated. Measured at humid condition

Conclusion

Capacitance variation with temperature C(T) and breakdown voltage determination measurements were performed on thin-film devices, referred to as Flat Samples. Setup used for measurements, procedure followed and the results of the measurements performed were presented in this chapter. Some observations are: the Flat sample without heat treatment (FS1) exhibited a large capacitance dependency on temperature. The Flat Sample without heat treatment (FS2) also exhibited a capacitance dependency on temperature, but not as high compared to FS1. Drying the samples resulted in little effect on the heat treated sample FS2, but there was a significant effect on the non-heat treated sample FS1 where we observed decrease in the sensitivity of the capacitance with temperature. The change in capacitance increased with a decrease in the signal frequency used to measure this capacitance. FS1showed breakdown characteristics similar to PHS Ta capacitors with BDV greater than the Formation voltage. However, in the heat treated FS2 breakdown occurred much below formation voltage. In the next chapter, we shall discuss these results further along with the mechanisms involved, in detail, to explain these results.

CHAPTER SIX

SUMMARY AND CONCLUSIONS

Summary

Primary goal of this research was to improve the long-term stability, capacitance dependence on temperature and understand breakdown behavior of PHS capacitors. So it is necessary investigate the properties of Polymer Ta capacitors through their characterization. The primary question is to understand whether the characteristics of PHS capacitors are a result of the special manufacturing process and the resulting complex structure involved or if it is primarily due to the nature of interactions between the organic and inorganic material layers present. This research started with the Polymer Hermetic Sealed (PHS) Tantalum (Ta) capacitors provided by KEMET Electronics Corporation, taken from a set of capacitors which exhibited a failure rate of 20% after life test. This failure rate is very high compared to industry standards, undesirable and must be reduced. In order to understand the effect of life test on the dielectric, measurements have been performed on these same capacitors in our lab in their working voltage and temperature range. Three sets of samples were characterized: (1) “Bad Samples” which failed the life test; (2) “Good Samples” which did not fail life test; and (3) “Virgin Samples” which did not go through life test. I-V measurements at low, high and room temperatures revealed that both Good and Bad Samples were definitely damaged based on their leakage current, which reached milliamp range during these measurements. However, Virgin Samples were able to withstand the measurements in the lab without any apparent damage.

In order to improve the performance of these PHS Ta capacitors, it is necessary to understand the observed high failure rate, including other unexplained properties such as high Breakdown Voltage and large temperature dependence of capacitance. MIS modelling or leakage

mechanisms did not fully explain the observed properties of PHS Ta capacitors [12]. Due to their complex structure, other models and theories are necessary to explain the properties of these devices. It might yield more meaningful insights if this capacitor is modeled by performing measurements on a thin-film device made of the same layer materials. These insights might include understanding if the properties are inherent to the complex structure of the KEMET capacitor or if it is because of the nature of interactions between the materials involved. This understanding would help narrow down the reasons for PHS capacitors' behavior and thus help find ways to improve these capacitors.

For this purpose, thin-film polymer Ta capacitors were fabricated – one set with heat treatment and another without heat treatment. It was decided to begin with measurements which will have less chance of damaging the samples, therefore we started with capacitance dependence on temperature(C(T)). It was expected that the results would be similar to behavior of Ta capacitors made using KEMET's finest Ta power, in which capacitance dependence on temperature is minimal compared to capacitors made from a coarser powder. However, for samples without heat treatment, the ΔC(T) results showed a very high dependence of capacitance on temperature, especially at high temperatures, on a scale which was never observed before. Results were repeatable and there was no cumulative effect of heat stress, demonstrating that these results are not the result of any error in measurement. ΔC(T) was smaller in samples with heat treatment compared to samples without heat treatment. While the capacitance change without treatment is less than 20% at all frequencies, it increased as much as 300% in FS1-C4 at 20Hz.

Later the samples were left to dry in a Nitrogen dry box for 24hrs to get rid of moisture and carefully transferred to air tight test tubes making sure they not exposed to humidity in air. Measurements were repeated on these dried samples and ΔC(T) was observed to be lower after

drying the sample compared to before drying the sample. Effectively, samples with heat treatment after drying (Figure 5.x) showed the least amount of temperature dependence of capacitance, while the sample without heat treatment before drying (Figure 5.15) showed the highest dependence of capacitance on temperature. So it is clear that the presence of moisture and heat treatment played a significant role in this high ΔC while heat treatment playing the most significant role. Additionally, the frequency at which the capacitance was measured showed a profound effect. ΔC(T) was very high at low frequency and it slowly decreased as frequency increased. Even after all this high and low temperature stress on the thin-film devices, the leakage current in the capacitors remained in the range of Nano amps (nA). This current is relatively low and indicates that the dielectric did not breakdown.

We will first consider the role of moisture and signal frequency in this phenomenon. Moisture is present only in the polymer, because the other two components are continuous solid layers. Earlier research on this topic indicated that moisture plays the role of a plasticizer in the PEDOT polymer [1], which means the moisture aids in polymer chain rotation by increasing their mobility.

The PEDOT and PSS macromolecules carry strong dipoles on polymer chains [1]. These dipoles can respond to changes in direction of the electric field across the polymer. If the time period of voltage signal(t_{signal}) applied across the polymer is less than the response time of polymer chain(t_{poly}), then the polymer chain will have insufficient time to respond. Therefore, the mobility of the polymer chain is very low at this high frequency. Conversely, at low frequency, when $t_{poly} < t_{signal}$, the polymer chain has sufficient time for complete reorientation. At low frequency, polymer chain responds quickly and allows charge penetration causing a change in charge (ΔQ) at the cathode-dielectric interface. This change in the charge stored w.r.t the change in applied

voltage(ΔV) is component of Capacitance. Thus, a low frequency signal across a capacitor which contains moisture in the cathode could be resulting in high capacitance. At high frequency, the capacitance is lower because of low charge penetration in the cathode. Apart from moisture and frequency, the temperature had a significant effect on ΔC. It has been observed that the mobility of polymer chains increases with temperature [1]. This explains the increase in capacitance with temperature.

Now the only remaining factor to consider is the heat treatment. Heat treatment was carried out before the cathode layer (PEDOT) was applied. So this procedure did not affect the polymer cathode directly. However, the heat treatment would have affected the dielectric, the surface of which would act as dielectric-polymer interface. According to [28], when a porous Tantalum anode was sintered in a deoxidizing condition, referred to as D-sintering, any anomalous current was eliminated. D-sintering and heat treatment are similar processes in terms of subjecting the material to high temperatures. This observation deserves further study to understand the effects of heat treatment, sintering, and similar treatment to the anode & dielectric at the interface between the anode and polymer.

Measurements performed on thin film devices provided results that are consistent with the behavior of discrete PHS Ta capacitors. We have also seen an I-V curve (Fig: 5.18) similar to that obtained on discrete capacitors which points out that these thin-film devices are reliable replicas of discrete capacitors. Breakdown Voltage for non-heat treated samples was observed to be around 57V, which is higher than their formation voltage of 44V. This indicates that the property of $BDV > V_f$ is not a consequence of the complex PHS Ta capacitor structure, but is due to interactions between the materials involved. Thin-film device behavior was also analogous to real capacitors in terms of behavior for C(T) at Humid Vs Dry conditions. Capacitance loss at low temperature for these devices is also within specifications (below 20%) for both Humid and Dry conditions.

There is an improvement in terms of capacitance change because of heat treatment in flat samples, a phenomenon similarly observed in the porous capacitors with sintering [28]. Understanding the way in which chain mobility is affected by sintered anodes and dielectrics may play a role in understanding the high BDV observed.

Conclusions

Flat samples showed properties similar to porous capacitors. This authenticates the fact that flat samples are useful devices with which to study mechanisms in porous capacitors. Furthermore, these results show that capacitor properties including very high variation of capacitance at high temperature, the effect of heat treatment and moisture on ΔC, and high BDV are inherent to the material in the devices and these properties can be studied effectively using flat samples.

This work turned out to be more promising than expected. There is a motivation to carry forward this work by fabricating more flat samples for measurements and modelling the results. Further study could include delving more deeply into the effect of heat treatment on the dielectric, investigating effects of different formation voltages (V_f) or dielectric thickness (T_{ox}), and studying the effects of temperature and humidity. Finally, correlation of these results with I-V and BDV measurements to study BDV > V_f can be very beneficial.

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