8-2016

Bi-Directional Grid-Tied Power Converter with GPS Capability

Anup Thapa
Clemson University, athapa@g.clemson.edu

Bi-directional grid-tied power converter with GPS capability

A Thesis
Presented to
the Graduate School of
Clemson University

In Partial Fulfillment
of the Requirements for the Degree
Master of Science
Electrical Engineering

---

by
Anup Thapa
August 2016

Accepted by:
Dr. Keith A. Corzine, Committee Chair
Dr. Richard E. Groff
Dr. Elham B. Makram

Abstract

This work proposes a bi-directional grid-tied converter with Global Positioning System (GPS) capability for smart-grid applications. The novelty of this converter is that time-stamped grid voltage angle received via network communication channels has been used to synchronize the converter to the grid. Therefore, all grid-tied converters in a microgrid with this development will not require line voltage sensing and phase-locked loops. The power section and modulation was built on a CompactRIO 9064 that also had a GPS timesource. In a larger power system, a nearby Phasor Measurement Unit (PMU) can be used for the time source. In a microgrid, a PMU capable controller is placed at the point of common coupling to measure the electrical angle. The electrical angle is time stamped with absolute time received via a GPS receiver and communicated to the power converter which is then used for grid synchronization. This thesis presents the results obtained from the study and operation of the PMU capable converter in both rectifying mode and inversion mode.

Acknowledgments

The immense support of my parents, Shyam and Laxmi Thapa, and my sister Anu Thapa is the reason this work exists today. I would not have reached this milestone without their continuous encouragement. I also thank Sneha Neupane for being by my side then, now and forever.

I thank my advisor Dr. Keith A. Corzine for trusting me with this work. I am very grateful to him for taking a chance on me and letting me be a part of his research team. His guidance, support and patience throughout my study at Clemson University have been extremely helpful.

I also thank Dr. Elham B. Makram for being a kind and excellent teacher and for agreeing to serve as my committee member. Likewise, I thank Dr. Richard E. Groff for his patience and acceptance to be my committee member.

I thank all my colleagues and the fellow students in my group for the many fruitful discussions that we have shared throughout my years at Clemson. My knowledge in electrical engineering has grown because of them.

Table of Contents

List of Figures

Chapter 1

Introduction

Modern society's dependence on electricity has been increasing and rapidly making it a critical infrastructure for sustaining world economy. The energy system of the future will have greater degree of integration of renewable energy sources in order to meet the demand for sustainable and environmentally friendly energy. The future of electric grid is expected to be intelligent and smart providing greater visibility and pervasive control of assets connected to the grid [1].

This vision for a smart grid has led to rapid inclusion of distributed generation (DG) sources to the existing grid. The energy sources for DG may include solar PV cells, wind generators, hybrid electric vehicles (HEV), etc. This has led to a greater presence of smart inverters in the electric power grid. The penetration of smart inverters in the traditional power grid is expected to keep increasing. As more power conversion systems are being added to the traditional utility grid, the capabilities of controllers associated with the power conversion systems have also increased greatly. Communication interface, additional sensors, energy storage and real time control are crucial features that inverters will require in order to realize a smart grid. These added abilities are enabling features for advanced control of power converters and the electrical grid.

Attention is now being drawn towards utilizing the advanced features that smart inverters have to offer that did not traditionally exist. In prior research, a smart PV in-

verter controller ready to offer auxiliary functions while also providing PMU capability has been proposed [2]. The added PMU capability of a power converter is certainly an advantage. However neither GPS data nor the network communication capability has been used towards improving converter control itself. The use of time-stamped phasor information for power converter control is also presented in [3]. Here the controller is communicatively coupled to a PMU and at least partial use of received phasor information towards control of the power converter is suggested.

The main objective of this work is to enhance power conversion capabilities of energy systems by utilizing GPS data and the communication media interface. The ability to transmit time-stamped values of critical analog signals in the synchronous reference frames to-and-from a higher-level control and its potential advantages is being explored in this work. Electrical angle of the utility grid is time-stamped and transmitted to local controllers for synchronization to the grid. The time-stamped data is being transmitted via IP network communication channels. Delays associated with such communication channels are nondeterministic and hence cannot be accurately predicted. The impacts of network-induced delays, data packet dropouts and data packet disordering in wide-area measurement systems (WAMS) has been discussed in [4]. Such delays impose an even greater problem while controlling power converters as the set points for the converter including reference angle, voltage, and frequency must be available in every control cycle. The accuracy of these signals have a very high influence in overall performance of the system [5]. In light of this fact, this paper proposes employing GPS time data as a method to compensate for errors that may be introduced due to network communication delays.

Figure 1.1 shows the overall schematic for the advanced power converter system proposed in this thesis work. A modern day smart power converter is shown along with typical peripheral features such as supervisory control, internet connection, analog sensor inputs and digital I/Os. GPS capability is added to the smart inverter for this work. In a large power system a nearby PMU may serve as the GPS time source. An attempt has been made to utilize these existing features of smart inverters for improving power conversion and

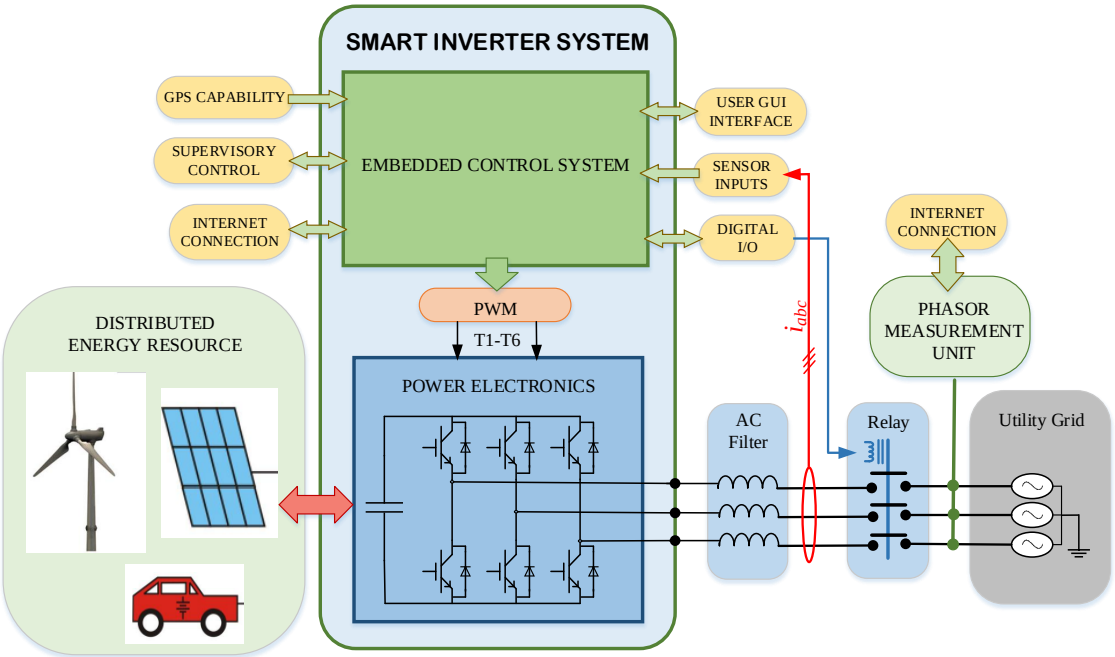

Figure 1.1: High-level schematic for proposed smart inverter grid integration

control. Particularly this work focuses on synchronization of power converters in remote or isolated locations with the utility grid or even with another power converter based on synchronized GPS time and data communication channels.

In this thesis work a new power converter control system has been proposed. Pre-existing capabilties within a smart inverter, like IP network communication capability, additional sensors, and energy storage along with added GPS sensor has been utilized for grid-synchronization. In the proposed system, the time difference between current absolute time from the GPS receiver module and the time-stamped data received via communication channels is calculated in every control cycle. This time difference along with the grid angle value received is used to estimate the current grid angle based on nominal grid frequency. The new angle estimate obtained is then used to synchronize the power converter to the grid and as reference angle for voltage oriented control of the power converter. Such capability can allow synchronization of power converters even with no physical connection and in the absence of local voltage sensors. This novel synchronization technique may even

be extended towards synchronization of microgrids to the utility grid. It can also assist in transitioning from islanded mode to grid connected mode of operation for microgrids and grid-forming power converters.

The ability to synchronize power converters to the grid based on internet connection and GPS data can be very useful in microgrids. Figure 1.2 shows a microgrid with several GPS capable converters for renewable energy integration. Solar, wind, HEV and battery energy storage has been shown as the energy systems in the grid. In such a system where there is also a PMU installed on the substation, none of the power converters will require voltage sensing or phase lock loop code. This means that the converters can be synchronized to the substation voltage while still maintaining complete galvanic isolation.

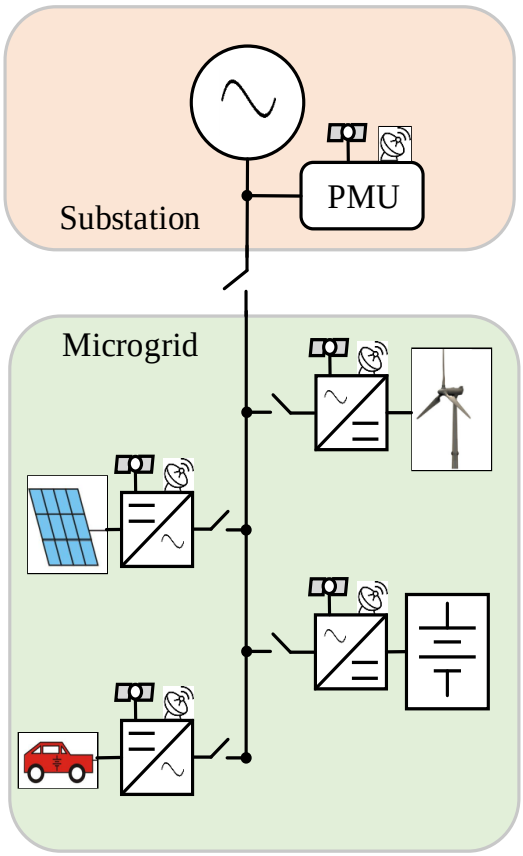

Figure 1.2: Microgrid with GPS capable converters for distributed generation integration

A GPS capable three phase bi-directional power converter with the features described above was built for this thesis work. The constructed power converter was synchronized to the utility grid solely based on the measurements received from a separate controller placed on the utility grid side. The latter controller, referred as the Grid Side Controller (GSC) was communicatively coupled with the power converter controller and also has capabilities similar to the smart inverter. Although synchronization based on phasor data transmitted from a PMU installed on the grid was intended, it was not possible for using an actual PMU for lab experiments. Instead time-stamped phase-lock loop (PLL) data is used for synchronization. The GSC makes voltage measurement of the grid and runs the synchronous reference frame phase locked loop (SRF-PLL) algorithm. Along with phase locked loop code execution, the GSC acquires absolute time information from the GPS module. The PLL data is timestamped with the GPS absolute time and transmitted to the smart inverter controller, or the Converter Side Controller (CSC). This data was then used for grid-synchronization of the power converter system.

The proposed power converter synchronization approach was experimentally verified on an FPGA based CompactRIO controller. A grid side controller, based on NI cRIO-9076 constructed and was placed on the utility side. A converter side controller, based on NI cRIO-9064 was also constructed along with a power-stage to serve as the smart inverter. Both the controller were communicatively coupled to each other and also had access to the GPS absolute time. In this work, a stiff utility grid has been assumed for the study of the proposed GPS capable converter. The grid frequency is assumed to be a constant 60 hz (377 rads/s) with 170 V peak phase voltage. Also it is assumed that there is no significant harmonics in the utility voltages.

Chapter 2

Grid-Tied Converter System

2.1 Reference Frame Theory and Voltage Oriented Control

While studying several electrical systems that include rotating and stationary electrical components, complex differential equations governing such systems are encountered frequently. However a change of the electrical variables often helps reduce the complexity of these differential equations [6]. This change in variable is obtained with the help of reference frame transformation. There are several change of variables used based on the electrical system under study, however all changes of variables used for transformation are contained within one general transformation equation. Only the speed of rotation of the reference frame may be unique to each.

Reference frame theory was first introduced by R. H. Park in 1929 to model synchronous machines [7]. When the variables associated with voltages, currents, and flux linkages of the stator windings of a synchronous machine are transformed to a reference frame rotating with the rotor, the rotor position-dependent inductances are eliminated from the voltage equations. This greatly simplifies the study of the synchronous machine. This was the approach proposed by Park in [7]. The equations that resulted from this transformation can be thought of as those associated with a set of fictitious windings rotating at the electrical angular velocity of the rotor of the machine.

Similarly G. Kron proposed a change of variables that eliminated the position-dependent mutual inductances of a symmetrical induction machine transforming the stator and rotor equations to a synchronously rotating reference frame [8]. Soon after, D. S. Brereton et. al. proposed transforming the induction machine variables to the reference frame aligned with the rotor of the machine [9]. This further eliminated the varying mutual inductances of a symmetrical induction machine thereby further reducing the complexity for machine study.

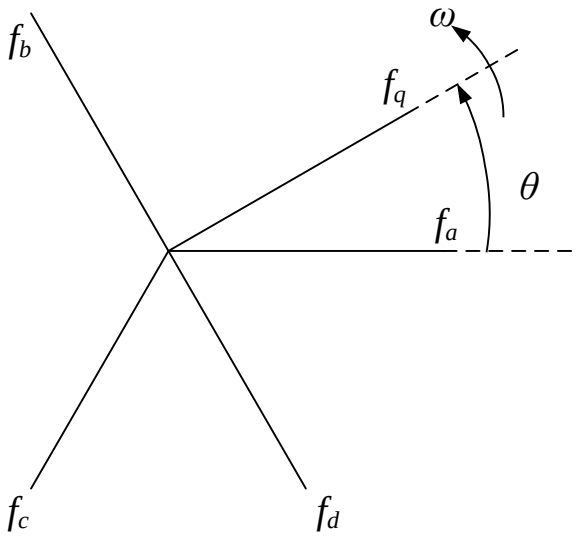

Figure 2.1: Transformation from the stationary to an arbitrary reference frame [6]

All the transformations mentioned above and others can be obtained by simply using the appropriate speed of rotation for the arbitrary reference frame. Figure 2.1 is a convenient way of portraying variable transformation where the direction of f_{as}, f_{bs}, and f_{cs} may be thought of as the direction of the magnetic axes of the stator winding of electric machines [6]. The equations for change of variables from the abc reference frame to the

arbitrary reference frame is given by equation 2.1.

$$\begin{bmatrix} f_q \\ f_d \\ f_0 \end{bmatrix} = K_s \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \tag{2.1}$$

where K_s is given by,

$$K_s = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \sin\theta & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{2.2}$$

In equation 2.1, f may be the voltage, current, flux linkage, or any other electrical variable. The inverse of equation 2.1, given by equation 2.3, is used to transform the changes variables back to the original abc reference frame.

$$\begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} = K_s^{-1} \begin{bmatrix} f_q \\ f_d \\ f_0 \end{bmatrix} \tag{2.3}$$

where K_s^{-1} is given by,

$$K_s^{-1} = \begin{bmatrix} \cos\theta & \sin\theta & 1 \\ \cos(\theta - \frac{2\pi}{3}) & \sin(\theta - \frac{2\pi}{3}) & 1 \\ \cos(\theta + \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) & 1 \end{bmatrix} \tag{2.4}$$

For the study of grid tied power converter it is most preferred that the variables be transformed to the reference frame that is synchronously rotating at the electrical angular velocity of the grid at the point of common coupling (PCC). This allows for a simplified decoupled vector control of the voltage, current, active power, and reactive power. The transformation equation required for this can be simply obtained by replacing θ in equa-

tion 2.1 by θ_e which is the electrical grid-angle at PCC. This is also called voltage oriented control (VOC).

In this thesis work, voltage oriented control (VOC) is employed for inverter control. VOC is similar to field oriented control for induction motors where the reference frame orientation is choosen such that decoupled control of the q- and d-axis current is possible. In this method there is an outer control loop followed by a faster inner current control loop. The control variable used for the outer loop determines the operation mode for the power converter. The schematic diagram for the voltage oriented control is shown in figure 2.2.

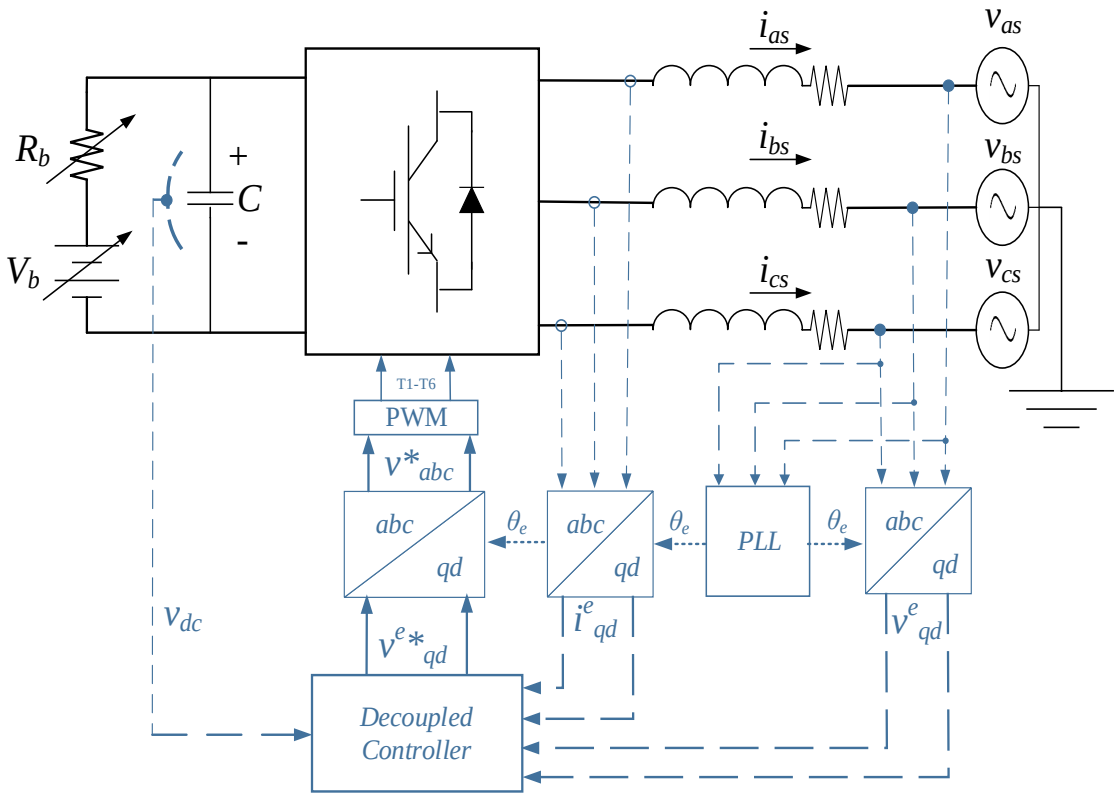

Figure 2.2: Voltage oriented control of grid-tied power converter

2.2 Grid-Tied Converter Control

Figure 2.3 shows the circuit diagram for the proposed grid-tied power converter topology. The voltage balance across the filter inductor is given by equation (2.5) where L is the filter inductance and R is the resistance. Subscript i is used to denote the voltage quantities at the inverter side of the filter while subscript s is used to denote voltage quantities at the point of common coupling (PCC).

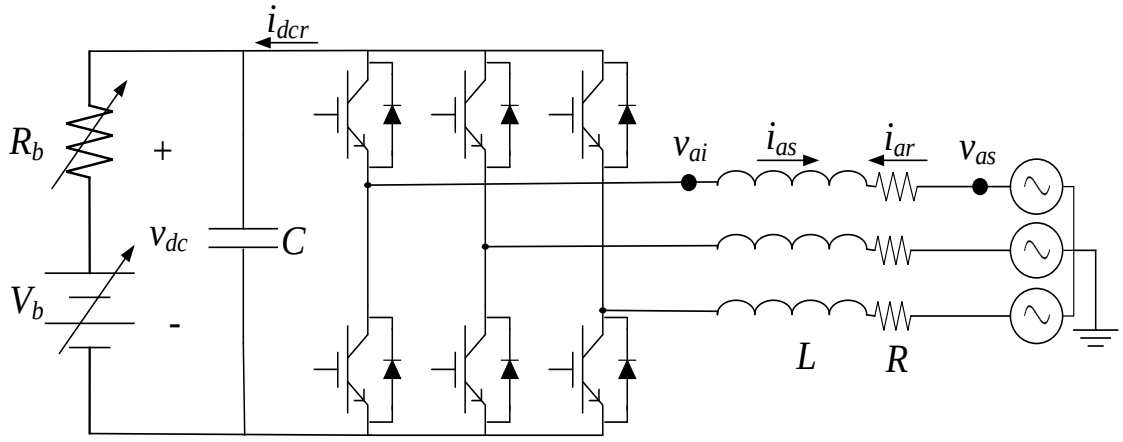

Figure 2.3: Grid-tied converter topology

$$\begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix} = \begin{bmatrix} v_{ai} \\ v_{bi} \\ v_{ci} \end{bmatrix} - R \begin{bmatrix} i_{as} \\ i_{bs} \\ i_{cs} \end{bmatrix} - L\frac{d}{dt} \begin{bmatrix} i_{as} \\ i_{bs} \\ i_{cs} \end{bmatrix} \tag{2.5}$$

When the grid side voltages are balanced with negligible harmonic content, it can be shown that they are DC quantities in the synchronous reference frame. Here, since it is a three-wire system without neutral wire for the zero-sequence current to flow, the system analysis in the synchronous reference frame reduces to just two q-axis and d-axis quantities. The zero-sequence circuit can be completely neglected. The reference frame orientation used in this work is similar to the one used in [6]. Transforming equation (2.5)

from abc-reference frame to synchronous reference frame yields equation (2.6).

$$\begin{bmatrix} v_{qs}^e \\ v_{ds}^e \end{bmatrix} = \begin{bmatrix} v_{qi}^e \\ v_{di}^e \end{bmatrix} - R \begin{bmatrix} i_{qs}^e \\ i_{ds}^e \end{bmatrix} - L\frac{d}{dt} \begin{bmatrix} i_{qs}^e \\ i_{ds}^e \end{bmatrix} - \omega_e L \begin{bmatrix} i_{ds}^e \\ -i_{qs}^e \end{bmatrix} \tag{2.6}$$

Because the inverter output voltages v_{qi}^e and v_{di}^e are the control variable in this application, equation 2.6 can be rearranged as shown in equation 2.7.

$$\begin{bmatrix} v_{qi}^e \\ v_{di}^e \end{bmatrix} = \begin{bmatrix} v_{qs}^e \\ v_{ds}^e \end{bmatrix} + R \begin{bmatrix} i_{qs}^e \\ i_{ds}^e \end{bmatrix} + L\frac{d}{dt} \begin{bmatrix} i_{qs}^e \\ i_{ds}^e \end{bmatrix} + \omega_e L \begin{bmatrix} i_{ds}^e \\ -i_{qs}^e \end{bmatrix} \tag{2.7}$$

It can be seen from equation 2.7 that there is a crosscoupling between the q and d components because of the flux linkage terms. This is diagrammatically illustrated in figure 2.4. Such crosscoupling can affect the dynamic response of the system and hence decoupling schemes must be employed. Feedforward decoupling control method has been used in this thesis work for independent control of the q and d components of the power converter.

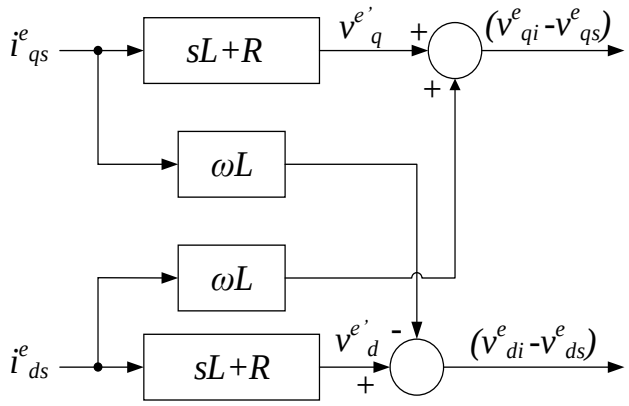

Figure 2.4: Crosscoupling between the q and d axis components

The feedforward decoupling control method can be realized by adding $\omega_e L i_{ds}^e$ and $-\omega_e L i_{qs}^e$ to the output of the PI controllers of the q and d axis currents respectively [10]. The plant

transfer function for both q- and d-axis current is thus given by equation (2.8).

$$T(s) = \frac{i^e_{qs}(s)}{v^{e'}_q(s)} = \frac{i^e_{ds}(s)}{v^{e'}_d(s)} = \frac{1}{Ls + R} \tag{2.8}$$

As the transfer function in equation 2.8 represents a first order system in the q- and d-axis reference frame, a simple PI controller is enough for the inner current control loop. If K_{pc} and K_{ic} are the proportional and integral gain for the current control loop PI, then the follow holds true,

$$\begin{bmatrix} v^{e'}_q \\ \\ v^{e'}_d \end{bmatrix} = (K_{pc} + \frac{K_{ic}}{s}) \begin{bmatrix} i^{e*}_{qs} - i^e_{qs} \\ \\ i^{e*}_{ds} - i^e_{ds} \end{bmatrix} \tag{2.9}$$

Finally the reference voltages for the inverter outputs can be calculated as equation (2.10).

$$\begin{bmatrix} v^{e*}_{qi} \\ \\ v^{e*}_{di} \end{bmatrix} = \begin{bmatrix} v^e_{qs} \\ \\ v^e_{ds} \end{bmatrix} + \begin{bmatrix} v^{e'}_q \\ \\ v^{e'}_d \end{bmatrix} + \omega_e L \begin{bmatrix} i^e_{ds} \\ \\ -i^e_{qs} \end{bmatrix} \tag{2.10}$$

For any demand current in the quadrature axis and/or the direct axis, equation (2.10) can be used to calculate the required inverter output voltage. This, in the synchronous reference frame is given by v^{e*}_{qi} and v^{e*}_{di}. Theses reference voltages transformed back to

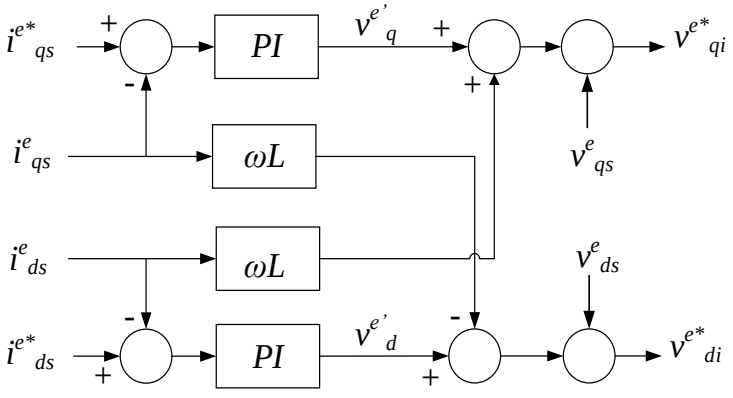

Figure 2.5: Feedforward decoupled q and d axis current control scheme

the abc reference frame are used for sinetriangle modulated gate signals for the six IGBT switches of the inverter. The decoupled current control strategy described in this section is illustrated in figure 2.5.

As mentioned earlier, the current control loop forms the inner loop of the converter control structure. In order to independently control the outer and inner loop, it is required for the inner loop to be much faster than the outer. One simple method to achieve this is by having higher PI gains for the inner loops than those for the outer loop. Further the control variable used for the outer loop depends on the application of the converter. In this work, dc voltage control mode is done for the rectifier mode of operation. However, for inverter mode of operation the outer loop has been removed and replaced by constant demand current in the q and d axis. Both these modes of operations are discussed here.

2.2.1 Rectifier Mode

For analysis of the converter in rectifier mode, subscript r is used to denote the current whose polarity is positive going into the converter as shown in figure 2.3. In this mode, V_b is set to zero thus reducing the dc-side circuit to a load resistor R_b in parallel with the dc-link capacitor C. Equation (2.11) gives the current-voltage relationship on the dc side of the converter, where C is the dc link capacitance and R_b is the resistance equivalent to the dc side load. Neglecting switching and converter losses, equation (2.12) relates the dc side to the ac side.

$$C\frac{d}{dt}v_{dc} = i_{dcr} - \frac{v_{dc}}{R_b} \tag{2.11}$$

$$i_{dcr} = \frac{3}{2}\left(\frac{v^e_{qs}i^e_{qr} + v^e_{ds}i^e_{dr}}{v_{dc}}\right) \tag{2.12}$$

Since in the synchronous reference frame v_{ds} is zero, equation 2.13 can be derived from equations 2.11 and 2.12.

$$\frac{v_{dc}^2}{i_{qs}} = \frac{3}{2} v_{qs}^e \left(\frac{1}{Cs + \frac{1}{R}} \right) \tag{2.13}$$

This is a first order transfer function to show that the dc-link voltage error can be put through a PI controller for q-axis demand current. Simultaneously setting d-axis current to zero ensures unity power factor for the power converter in rectifier mode of operation. If K_{pv} and K_{iv} are the proportional and integral gain for the dc voltage control loop PI, then for rectifing mode of operation at unity power factor the follow holds true,

$$i_{qs}^* = (K_{pv} + \frac{K_{iv}}{s})(v_{dc}^* - v_{dc}) \tag{2.14}$$

$$i_{ds}^* = 0 \tag{2.15}$$

2.2.2 Inverter Mode

In inverter mode the power converter acts as a power source, injecting active or reactive power into the grid. For inverters in grid feeding mode, q- and d- axis current injection demand can be obtained from active or reactive power mismatch. For grid-tied converters in grid supporting mode, the q-axis demand current maybe obtained from grid-frequency error and the d-axis current maybe obtained from grid voltage error [5]. However in this work, the outer control loop was removed completely. Instead the outer loop was replaced by a constant q-axis current injection.

For analysis of the converter in inverter mode, subscript s is used to denote the current whose polarity is positive going from the converter to the grid. In this mode, R_b is set to zero thus reducing the dc-side circuit to a constant dc source V_b in parallel with the dc link capacitor C. The real and reactive power flowing into the grid is governed by

equation 2.16, where P and Q represent the real and reactive power flow respectively.

$$\begin{bmatrix} P \\ \\ Q \end{bmatrix} = \frac{3}{2} \begin{bmatrix} v_{qs}^e & v_{ds}^e \\ \\ -v_{ds}^e & v_{qs}^e \end{bmatrix} \begin{bmatrix} i_{qs}^e \\ \\ i_{ds}^e \end{bmatrix} \tag{2.16}$$

When the reference frame is aligned with the positive sequence grid-voltage, v_{ds}^e is zero. In such a case, active power and reactive power get decoupled allowing independent control of either. The power flow equation in such a case is given by (2.17). This principal allows the use of active power error for q-axis demand current and reactive power error for d-axis demand current. Based on the selected current direction, the converter works as an active power source for positive q-axis current (i_{qs}). At unity power factor the current is in phase with the grid voltage. For a positive q-axis demand current the power converter is sourcing active power to the grid while for a negative q-axis demand current it is sinking active power.

$$\begin{bmatrix} P \\ \\ Q \end{bmatrix} = \frac{3}{2} v_{qs}^e \begin{bmatrix} i_{qs}^e \\ \\ i_{ds}^e \end{bmatrix} \tag{2.17}$$

Active power error for q-axis demand current and reactive power error for d-axis demand current allows operation of the converter as a source or a sink for both active and reactive power. If K_{pv} and K_{iv} are the proportional and integral gain for the outer control loop PI, then for a grid-feeding converter with P^* and Q^* as the active reactive power demand the following holds true,

$$\begin{bmatrix} i_{qs}^{e*} \\ \\ i_{ds}^{e*} \end{bmatrix} = (K_{pv} + \frac{K_{iv}}{s}) \begin{bmatrix} P^* - P \\ \\ Q^* - Q \end{bmatrix} \tag{2.18}$$

In both rectifying and inverting modes it requires that the dc-link voltage be greater than the maximum line-to-line grid voltage. This is because the power converter configuration is a boost rectifier type. The six anti-parallel diodes are forward biased for dc voltages lower than the maximum grid voltage. Instead it is required that the diodes always be

reversed biased and only serve as the return path for inductive current. Therefore the minimum dc link voltage must be $\sqrt{6}v_s$, where v_s is the rms phase voltage.

Equally important for successful operation and control of a grid-tied converter is synchronization to the grid voltage. It is imperative that the grid voltage magnitude and phase angle be known with high accuracy in every cycle of the control loop [11]. This makes phase locked loop (PLL) a crucial component for converter control [12]. The SRF-PLL is a popular phase locked loop technique used for grid-tied inverter applications and is explained in section 2.3

2.3 Synchronous Reference Frame PLL (SRF-PLL)

Synchronization of the power converter to the grid is essential for proper control of active and reactive power exchange between the converter and the grid. Several phase-locked loop techniques exist for the detection of positive sequence voltage component at the fundamental grid frequency. The synchronous reference frame phase locked loop (SRF-PLL) is one of the most extensively used PLL techniques for grid synchronization of power converters [13].

Figure 2.6 shows the block diagram for the implementation of a three phase SRF-PLL. The instantaneous phase angle θ_e is identified by synchronizing the rotating reference frame to the utility voltage vector [14]. In the first stage the voltage vector is transformed to the stationary reference frame using Clarke's transformation. On the second stage they are transformed to the synchronously rotating reference frame using Park's transformation. The transformation equations for Clarke's transformation and Park's transformation are given by 2.19 and 2.20 respectively.

$$\begin{bmatrix} v_{\alpha s} \\ v_{\beta s} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix} \tag{2.19}$$

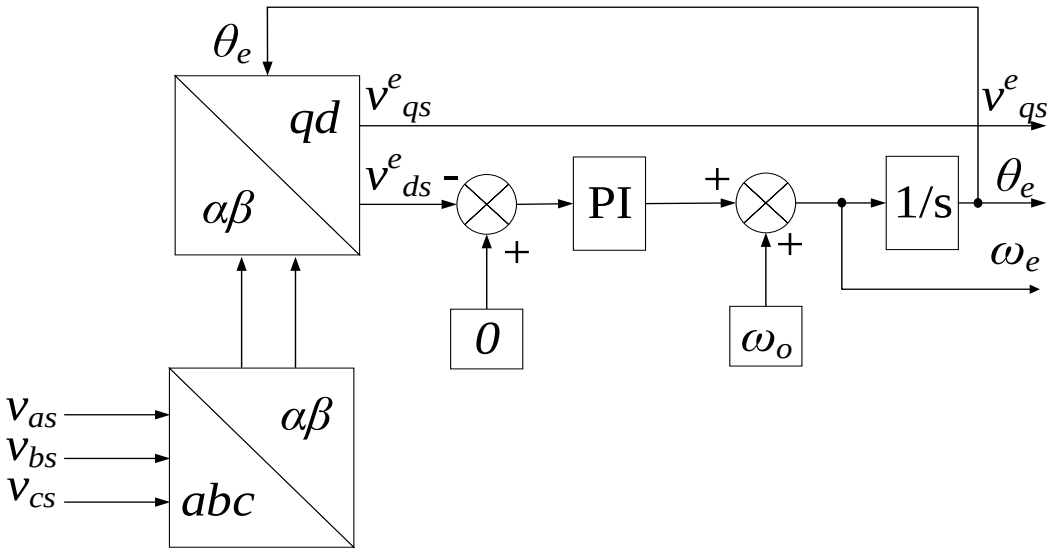

Figure 2.6: Block diagram of SRF-PLL

$$\begin{bmatrix} v_{qs} \\ v_{ds} \end{bmatrix} = \begin{bmatrix} \cos\theta_e & -\sin\theta_e \\ \sin\theta_e & \cos\theta_e \end{bmatrix} \begin{bmatrix} v_{\alpha s} \\ v_{\beta s} \end{bmatrix} \tag{2.20}$$

Following the change of variables, a PI controller commands the direct axis voltage component to zero. This, in effect, locks the reference frame orientation to the grid voltage vector. Therefore at steady state the quadrature-axis voltage component obtained from the PLL block is the grid voltage amplitude. The base grid frequency of 377 rads/sec is added to the PI output as a constant dc offset to obtain the grid electrical frequency, ω_e, which is then integrated for grid phase angle, θ_e.

2.4 GPS Capable Converter

In 1978, US Department of Defense launched the first Block I satellite and thus initiated the Global Positioning Systems (GPS) technology. The GPS is a satellite-based navigation system that uses a network of 24 satellites that are in orbit of the earth, as shown in figure 2.7. Although this system was initially launched for military applications, in the 1980s the US government made it available for civilian use.

The global positioning systems were primarily intended for determination of loca-

Figure 2.7: GPS satellites in orbit of the earth

tion coordinates on the earth. However in power systems GPS has extensively been used to obtain synchronized measurements for applications in wide-area monitoring. Particularly the one pulse-per-second (PPS) is used to obtain synchronized phasor measurements from several points within a large power system. This pulse as received by any GPS receiver is coincident with all other received pulses within 1 microsecond [15], although much higher accuracy can be acheived. The GPS satellites keep track of accurate clocks in order to provide the PPS. Therefore GPS receivers also acquire this synchronized absolute time that can then be used to synchronize other clocks to a common reference.

A GPS capable smart power converter is being proposed in this thesis work. The

proposed smart power converter system can synchronize to the grid without requiring direct line voltage measurements. This converter makes use of time-stamped phase-locked loop data received via network communication channels to synchronize to the utility grid. With this development, grid-tied converters can be brought up to speed with grid frequency and be synchronized with the voltage vectors while still remaining electrically isolated. This work intends to use already existing features of smart inverters like communication interface, real-time control and added sensors for improved converter control.

In the work in this thesis, NI 9467 GPS Time and Synchronization Module is used as the GPS receiver. This GPS module boosts a PPS accuracy of $\pm 100\ ns$. Mainly the obtained absolute time, or the International Atomic Time (TAI) accurate to $\pm 100\ ns$, is used in the proposed grid-synchronization technique.

A controller with a GPS connection measures the grid voltages and runs the SRF-PLL algorithm. The positive sequence voltage magnitude and angle is measured with the phase locked loop. This controller, henceforth called the *grid side controller* (GSC), is constantly measuring the grid voltage and calculating the phase angle at a very high rate. The electrical grid angle thus obtained is time-stamped with absolute time received from the GPS time source. In a larger power system a PMU installed on the grid can be used instead of the GSC used here. The data from the GSC is transmitted via network communication channels to the power converter controllers where it is used for grid synchronization.

Similarly, the GPS capable power converter requires a controller with reliable GPS connection and network communication capability along with other standard features of a power converter. This local controller, henceforth called the *converter side controller* (CSC), implements control algorithms for the power exchange between the converter and the grid. It measures the lines current at the controller end but does not make grid voltage measurements. Instead it receives time-stamped data from the GSC. Based on the current absolute time received from the GPS time source, CSC estimates the angle for grid synchronization of the converter. Based on local current measurements and remote voltage measurements, the CSC generates gate signals for the IGBT switches and thus controls the

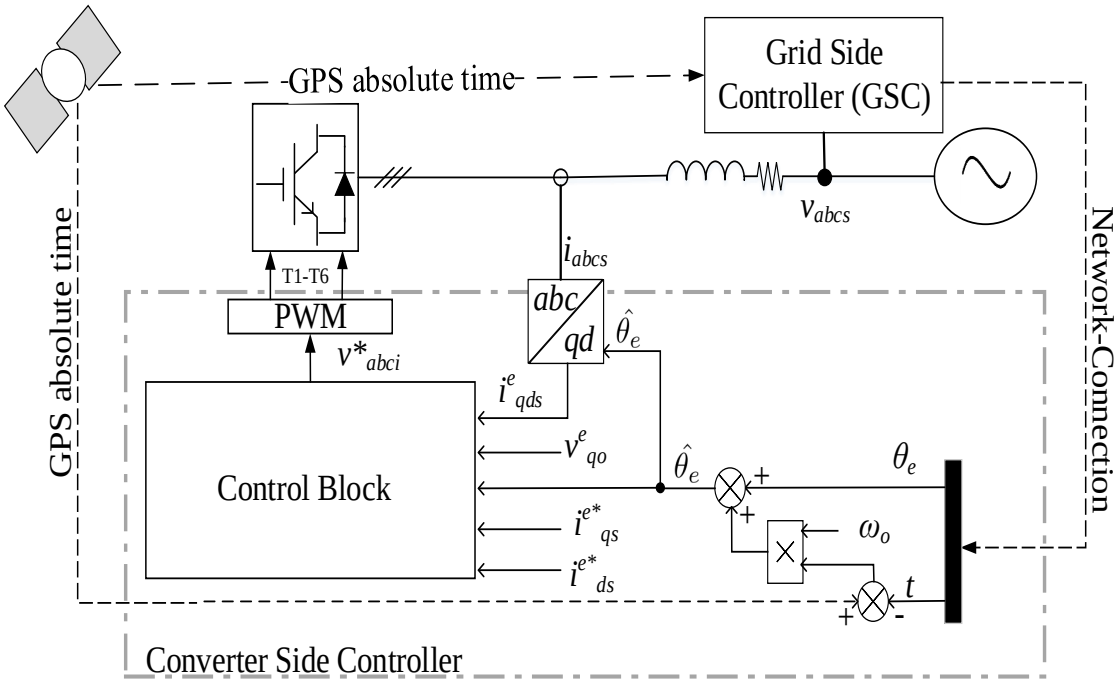

Figure 2.8: Low-level schematic of proposed Converter Side Controller (CSC)

grid-tied power converter.

The low-level schematic for the control of the GPS capable power converter is shown in figure 2.8. As previously mentioned, the converter side controller is communicatively coupled with the grid side controller. This control strategy only requires local current sensing but does not require voltage sensing.

Chapter 3

Simulation Work

Before the hardware for lab experiment of the power converter was put together a system simulation in software environment was imperative. Although network communication delay and GPS time-stamping cannot be accurately modeled in Simulink, the performance of a typical grid-tied power converter needed to be studied. With this in mind a simulation system was designed in Matlab^{TM}. The details of this Matlab simulation and the obtained results are discussed in subsequent sections of this chapter.

3.1 Simulation Model and Control

The top-level block diagram of the system model that was assembled in Simulink environment is shown in figure 3.1. Each block item that is seen in the figure represents a physical item in the experimental setup, except for the *Main Controls* block. The Main Controls block can be thought of as being analogous to the power converter controller. All the codes within this block were eventually programmed in LabVIEW FPGA for the NI FPGA based controllers used.

The three phase ac-source in the simulation represents the utility grid. It was configured as 208V 3ϕ, which is the rated grid voltage available in the lab. The V-I measurement block seen in the figure measured the line voltages and line currents of the three

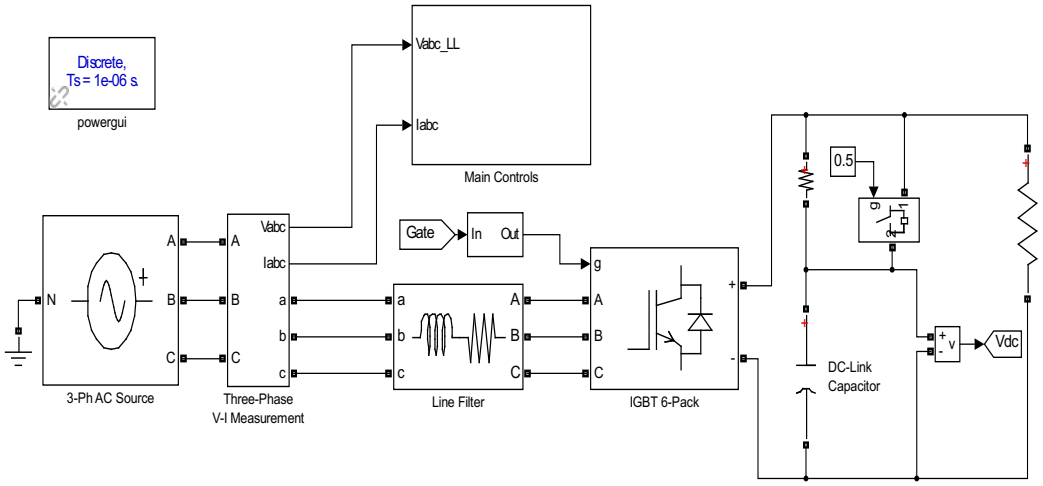

Figure 3.1: Top-level simulation model as built on Simulink for rectifying mode

wire system. As mentioned earlier, the setup is a three wire system without a neutral connection. Meaning that only line-to-line voltages could be measured during the hardware experiment. In order for the simulation to closely match the experiment, line-voltage measurements were made instead of phase voltage measurements. Phase to neutral voltages was calculated from phase to phase voltage using equation 3.1. In employing equation 3.1 for phase voltage calculations it is assumed that the three phases are balanced and that their vector addition equals zero.

$$\begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix} \begin{bmatrix} v_{abs} \\ v_{bcs} \\ v_{cas} \end{bmatrix} \tag{3.1}$$

A filter inductor of 4.2 mH was placed between the power converter output terminal and the utility grid. A 10 Ω resistor was placed in series with the 4700 μF dc link capacitor for precharge. In absence of the 10 Ω precharge resistor a very large current transient occurs through the anti-parallel diode rectifier on startup. This in-rush current can be in the range of hundreds of amperes and can cause breakdown of the anti-parallel diodes due

to overcurrent rendering the IGBT power modules useless. The precharge resistor helps limit the in-rush current through the power module thereby protecting them. Once the capacitor is charged to a high enough voltage the resistor must be removed to avoid power loss in the circuit. It was observed that the capacitor took around 0.3 seconds to charge to 275 V. At this voltage there is no risk of a high current transients and hence the precharge resistor was shorted at 0.5 secs.

PARAMETER	***SYMBOL***	***VALUE***
rated r.m.s. grid voltage	v_{lls}	208 V
filter inductance	L	4.2 mH
filter resistance	R	0.01 Ω
dc link capacitor	C	4700 μF
dc voltage Source	V_b	400 V
baseload	R_b	100 Ω
switching frequency	f_{sw}	10 kHz
simulation time step	T_s	2 μsec
precharge resistor	R_p	10 Ω
outer loop proportional gain	K_{pv}	1
outer loop integral gain	K_{iv}	1.5
inner loop proportional gain	K_{pc}	15
inner loop integral gain	K_{ic}	100

Table 3.1: Simulation System Parameters

A 100 Ω resistor was placed in parallel with the dc capacitor as the baseload, or dc load equivalent. For simulation of the power converter in inverter mode of operation the base load resistor is removed and replaced with a constant dc source of 400 V. This is shown in figure 3.2. The system parameters used in the matlab simulation are listed in table 3.1. Figure 3.3 shows the block diagram immediately inside the Main Controls block of figure 3.1. As mentioned above, first the line voltages are converted to phase voltages using equation 3.1. The phase quantities are transformed to the synchronous reference frame in a two step process. In the first step they are tranformed to the stationary reference frame by Clarke's transformation given by equation 2.19. Because it is a three wire system without the neutral connection, zero sequence components can be neglected. The three

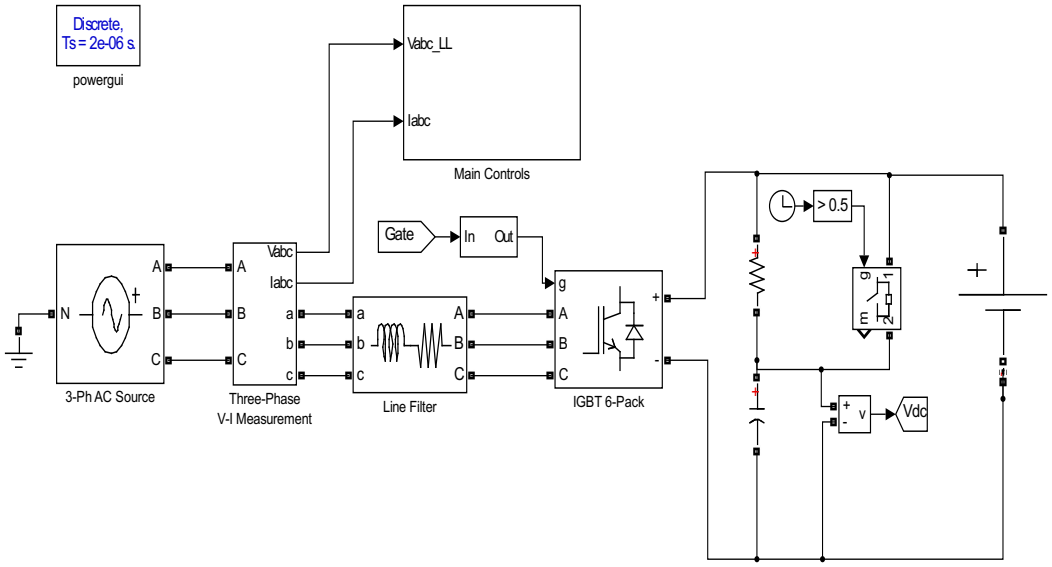

Figure 3.2: Top-level simulation model as built on Simulink for inverting mode

phase voltages reduce to two sinusoidal alpha-beta quantities. In the second step these alpha-beta quantities are transformed from the stationary to the synchronous reference frame with Park's transformation, given by equation 2.20. The voltage phase angle required for Park's transformation is obtained from the SRF-PLL block, as seen in figure 3.3.

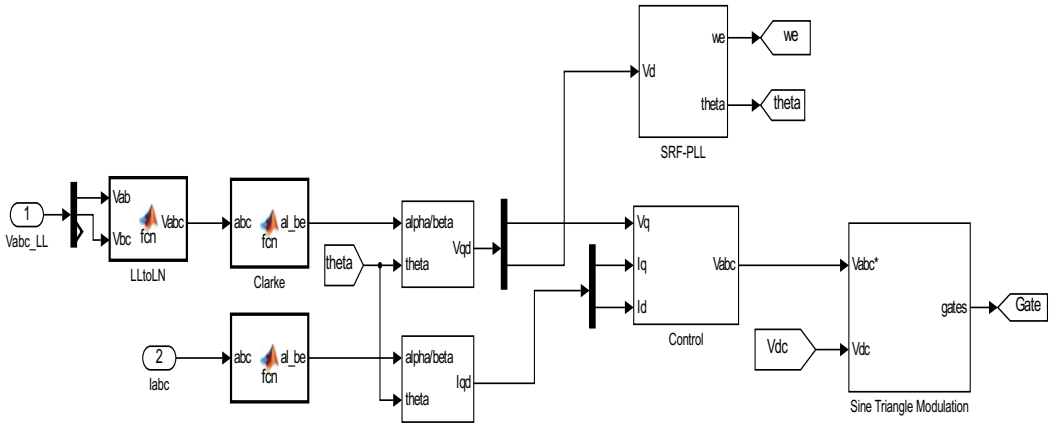

Figure 3.3: Main Controls block diagram

The voltage and current control loops are the main part for the control of the power converter. Figure 3.4 shows the control loop block diagram built in matlab for dc voltage control mode of the power converter. Here the dc-link voltage error is passed through a PI controller to obtain q-axis reference current. This forms the slower outer voltage loop of the control system. Meanwhile the d-axis current reference is set to zero for unity power factor operation. Both the q-axis current error and the d-axis current error is further passed through another PI controller to form the inner control loop. The inner current loop must be faster than the outer current loop for good dynamic response of the system. The outer voltage control loop can easily be replaced by a constant q-axis current reference instead of the dc voltage control loop. In fact, only small changes are needed for this system in order to operate the power converter in other modes of operation.

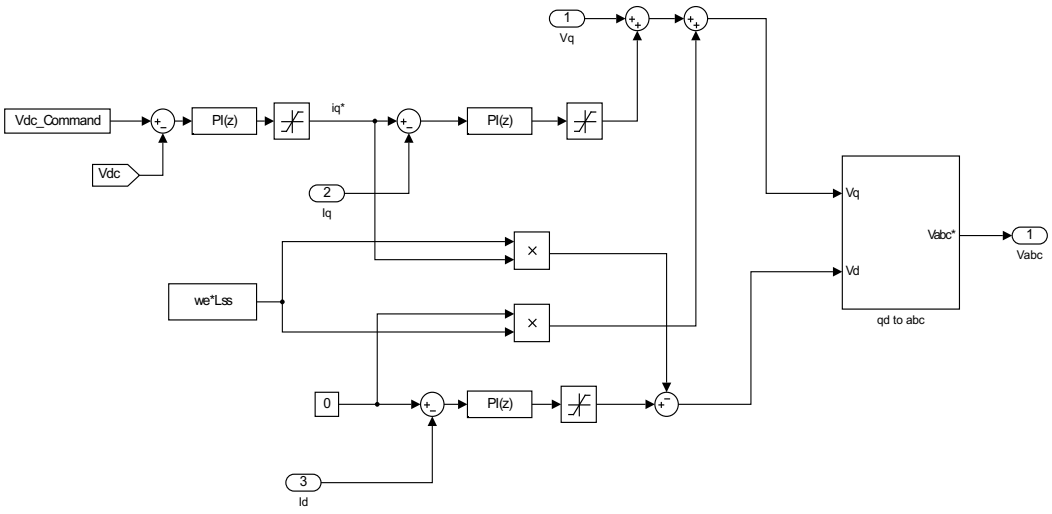

Figure 3.4: DC voltage control and current control block diagram

3.2 Simulation Results

The graph in figure 3.5 shows the voltage across dc-link capacitor during start-up. At start-up the converter is connected to the grid with all IGBTs switched-off. In such a case, the anti-parallel diodes across the IGBTs are forward biased. Therefore the converter operates as a passive three phase diode-rectifier. This explains the non-sinusoidal current seen in figure 3.5. The 10 Ω precharge resistor placed in series with the capacitor limits the in-rush current during the initial capacitor charging stage. As a consequence of limiting the inrush current, the capacitor voltage rises slowly. Once it has reached a safe value the precharge resistor is shorted out. This eliminates the precharge resistor from the circuit and helps avoid unwanted losses in the system. In this simulation work, the precharge resistor was shorted out after 0.5 secs of start-up. At this time the capacitor voltage has reached to around 275 V eliminating the danger for high current transient.

At 0.5 sec, while simultaneously shorting the precharge resistor, 350 V dc voltage was commanded and the gate signals were applied to the IGBTs. The transient response for the system under this condition is shown in figure 3.6. The current waveform before 0.5 sec is non-sinusoidal for the reasons discussed above. However after applying the gate signals, the current transients die out. The steady-state current waveform becomes sinusoidal after 0.04 seconds of gate signal application as seen in figure 3.7.

At 0.7 seconds a step change in dc voltage from 350 V to 400 V is commanded to the converter. The transient response of the power converter is shown in figure 3.8. The steady state response of the converter for 400 V commanded dc voltage can be seen in figure 3.9.

In figure 3.10, the steady-state response of the power converter in inverter mode is shown. Here 7 amps of q-axis current and zero d-axis current is flowing from the converter to the grid. In this mode the power converter is sourcing 1.785 kW of active power to the utility at unity power factor.

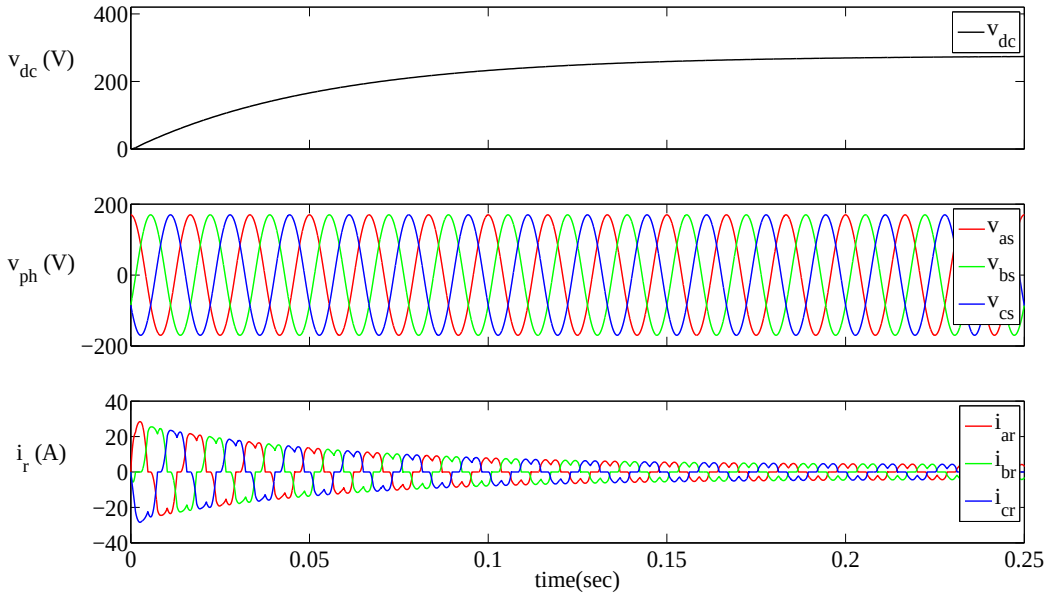

Figure 3.5: Capacitor charging action during startup for rectifying mode

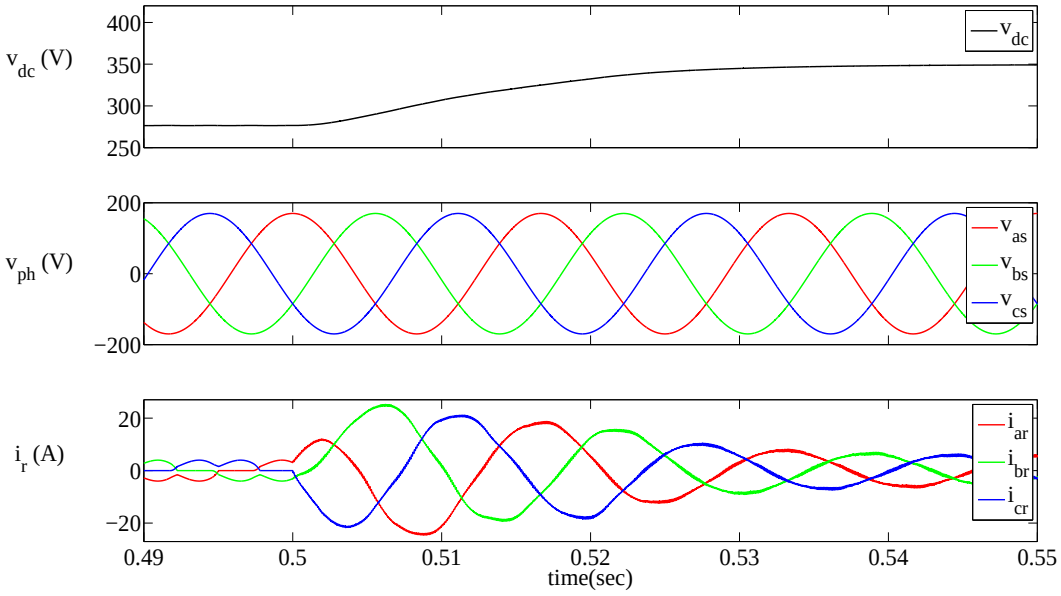

Figure 3.6: Response after gate signals turn on and 350 V commanded dc voltage

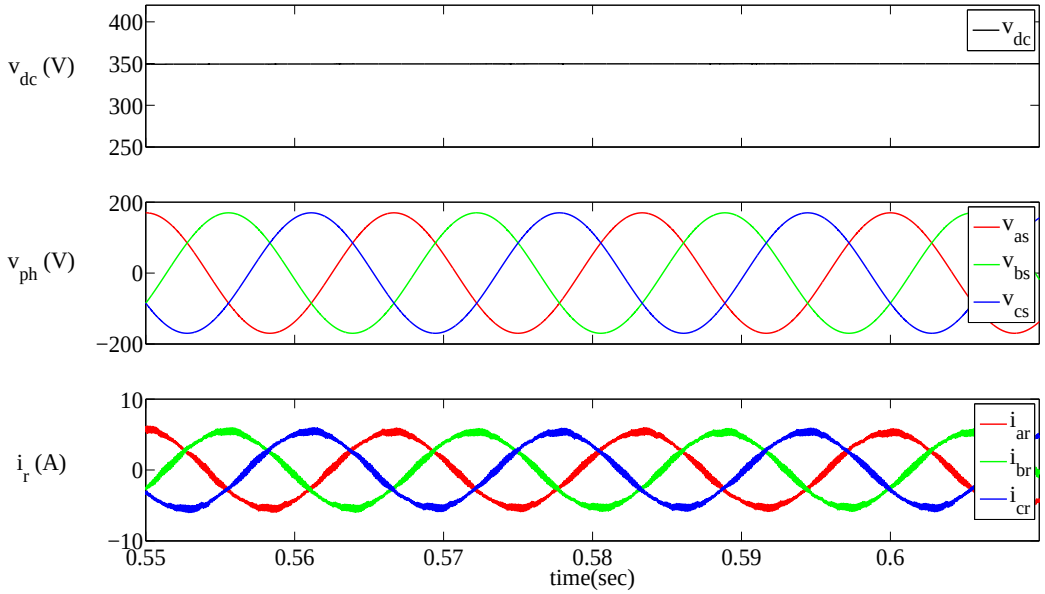

Figure 3.7: Steady state response for rectifying mode for 350 V commanded dc voltage

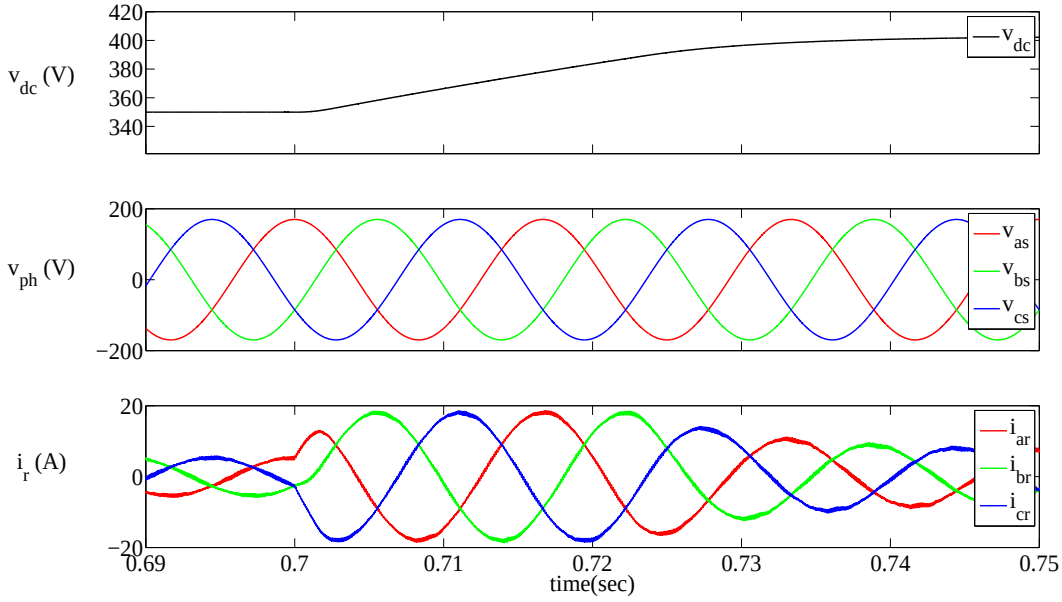

Figure 3.8: Response due to step change in commanded dc voltage from 350 V to 400 V

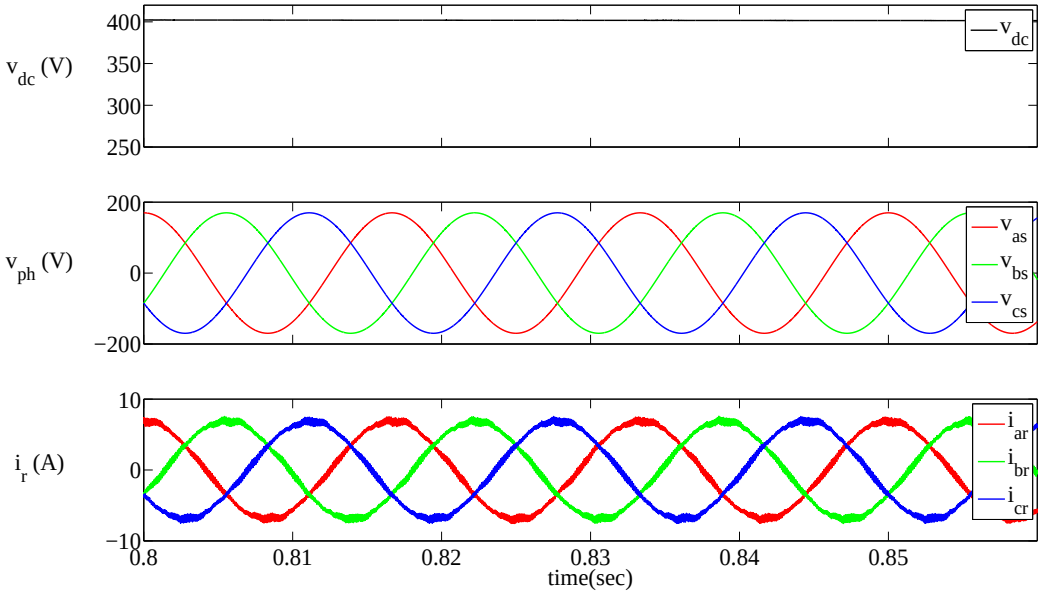

Figure 3.9: Steady state response for rectifying mode for 400 V commanded dc voltage

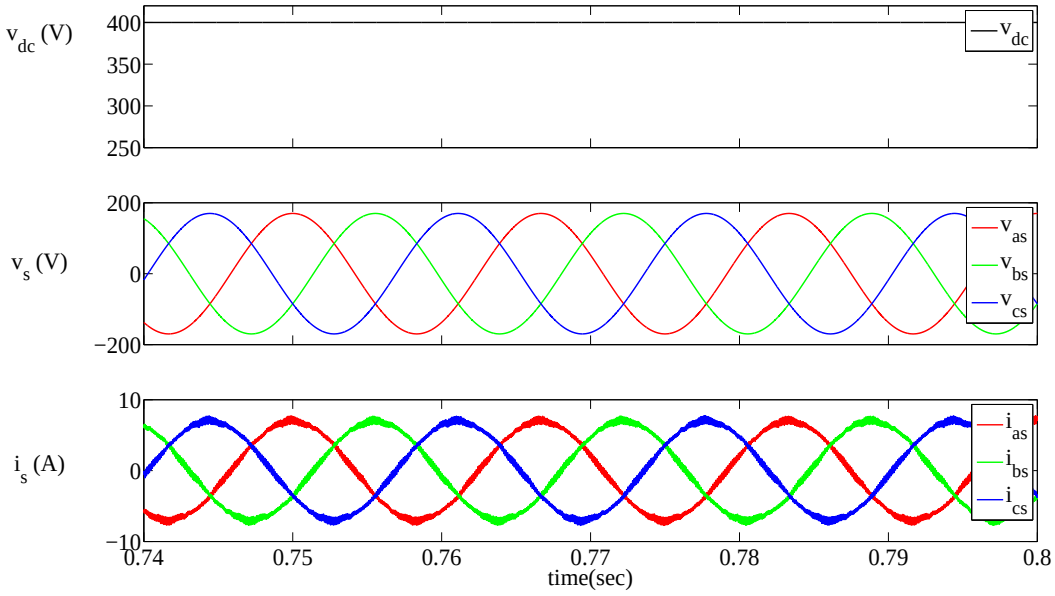

Figure 3.10: Steady state response for inverting mode of power converter operation

Chapter 4

Experimental Setup

4.1 NI FPGA Hardware

In power electronics the popular trend has been to use digital signal processors (DSPs) or microcontrollers (μCs) for digital control applications. However in recent years field programmable gate arrays (FPGA) based control platforms have started to penetrate the power electronic scene. Both DSP and FPGA have advantages and disadvantages associated with their applications. FPGAs, as the name suggests, have a reconfigurable hardware and therefore the developer must first design the hardware layer and only then proceed to develop the software layer for control applications. This implies that designing a control system on an FPGA platform has one added level of complexity than its DSP based counterpart. Due to the built-in processors and peripherals that are readily available on-board a DSP, they offer a great out-of-the-box experience allowing the system designer to develop the application software straight away.

FPGAs on the other hand, can acheive very high computational speed compared to a DSP. This is due to parallel execution capabilities of the reconfigurable hardwares on an FPGA chip. While the number of operations per cycle on a DSP is limited to the number of cores on-board, FPGAs can easily be programmed to execute multiple operations on every clock cycle. The limitation here is not the number of operations per cycle but instead the

limited hardware resources available. Proper design techniques must be used in order to achieve the right execution speed while minimizing the FPGA resource usage.

The cumbersome machine-level programming language like Verilog and VHDL along with difficult debugging procedures is the greatest disadvantage for using an FPGA. However in recent years FPGA vendors have started to provide intellectual property (IP) cores that reduces the hardware development phase to its minimum. Many vendors provide IP cores that are easy to use with most FPGA boards that are available in the market. With the FPGA and IP core approach system developers now have the liberty to select IP components that are tailored to suit individual application requirements. This has reduced the programming complexity associated with the machine-level codes and greatly reduced the overall development time.

National Instruments (NI) have developed NI FPGA hardware products that are built on a reconfigurable I/O (RIO) architectures [16]. The NI FPGA systems feature floating-point processors, reconfigurable FPGAs, and modular I/Os. Further, these reconfigurable hardware can easily be programmed in NI LabVIEW which is a graphical user interface (GUI) based high-level system design tool. This makes using NI FPGA hardware architectures for advanced control, monitoring, and test applications much simpler compared to other similar systems. NI Single board RIO (sbRIO) General Purpose Inverter Controller (GPIC) is an FPGA based controller that was specifically designed for applications in power electronics [17]. It combines the power of both an FPGA and a DSP while also providing peripheral I/O ports ideal for controlling power converters. Figure 4.1 shows the general purpose inverter controller developed by NI where the sbRIO FPGA board can be seen on top. Before the GPS-synchronization technique could be tested it was important to properly control a simple power converter using NI FPGA hardware. Therefore a typical phase-locked loop based grid-synchronized power converter was designed and studied in the lab. This converter was based on the sbRIO-9607 Zynq-7020 General Purpose Inverter Controller (GPIC), similar to what is shown in figure 4.1.

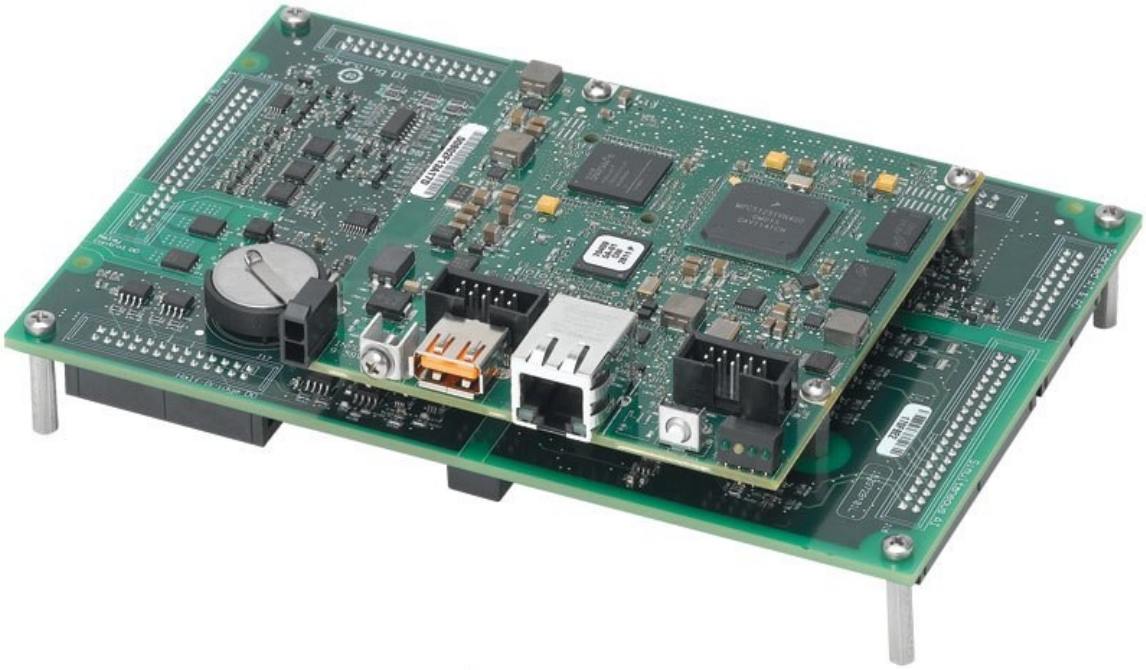

Figure 4.1: NI sbRIO General Purpose Inverter Controller (GPIC) [17]

4.2 Grid-tied Power Converter

Firstly a grid-tied power converter was built based on the general purpose inverter controller (GPIC). This was a standard power converter that used the local phase-locked loop for grid-synchronization as opposed to the GPS-based synchronization technique that is proposed in this work. In order to setup this converter, an interface board was required for proper use of the analog and digital channels on the GPIC.

4.2.1 Interface Board

A 4-layer PCB was designed in EAGLE as the interface board for expansion of the GPIC pins and for analog signal conditioning. EAGLE is a powerful PCB design software that offers high-level circuit board design functionalities and is easy to use. The interface board was designed such that board-to-board mating with the GPIC was possible. As seen in figure 4.2, the designed board connects with the GPIC on its bottom side while the voltage and current sensors rest on the top side. Voltage transducer LV 25-P was used

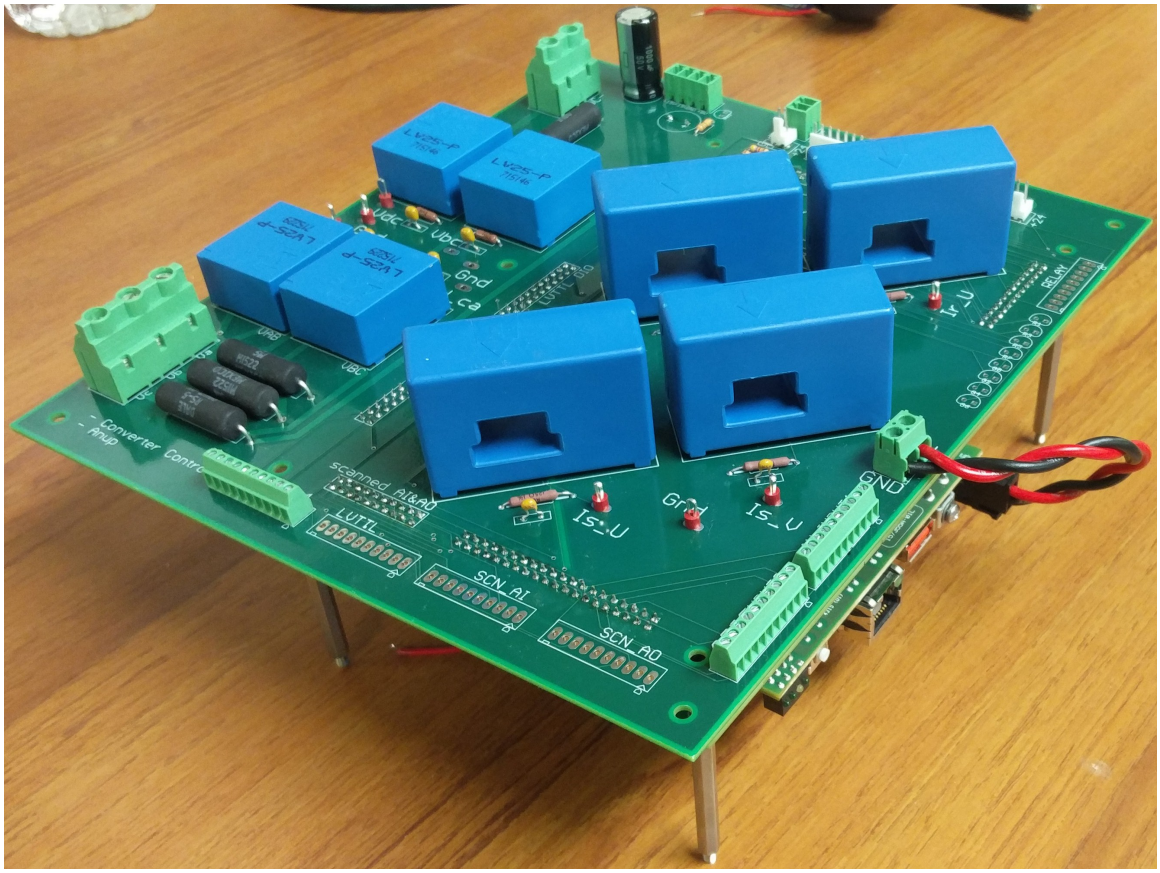

Figure 4.2: Top view of the interface board with the sbRIO GPIC below

for the voltage measurements both on the AC as well as DC side. Current transducer LA 125-P was used for current measurement. Both these voltage and current sensors are Hall effect type closed loop current transducers with excellent accuracy, good linearity, high bandwidth, and low reponse time. Small ceramic capacitors were placed on the output pins of each of these transducers for filtering high frequency noise. PC test point loops were also placed for easy access to the analog signal for probe connections. 4 red LEDs and 4 green LEDS were also placed on the board for possible fault or status indication.

Figure 4.3 shows the bottom view of this board where the GPIC and the heat sink for the sbRIO can be seen. Accurate dimensions of the GPIC available on the datasheet was used to place the connector receptacles at proper locations for easy interface with the GPIC header pins.

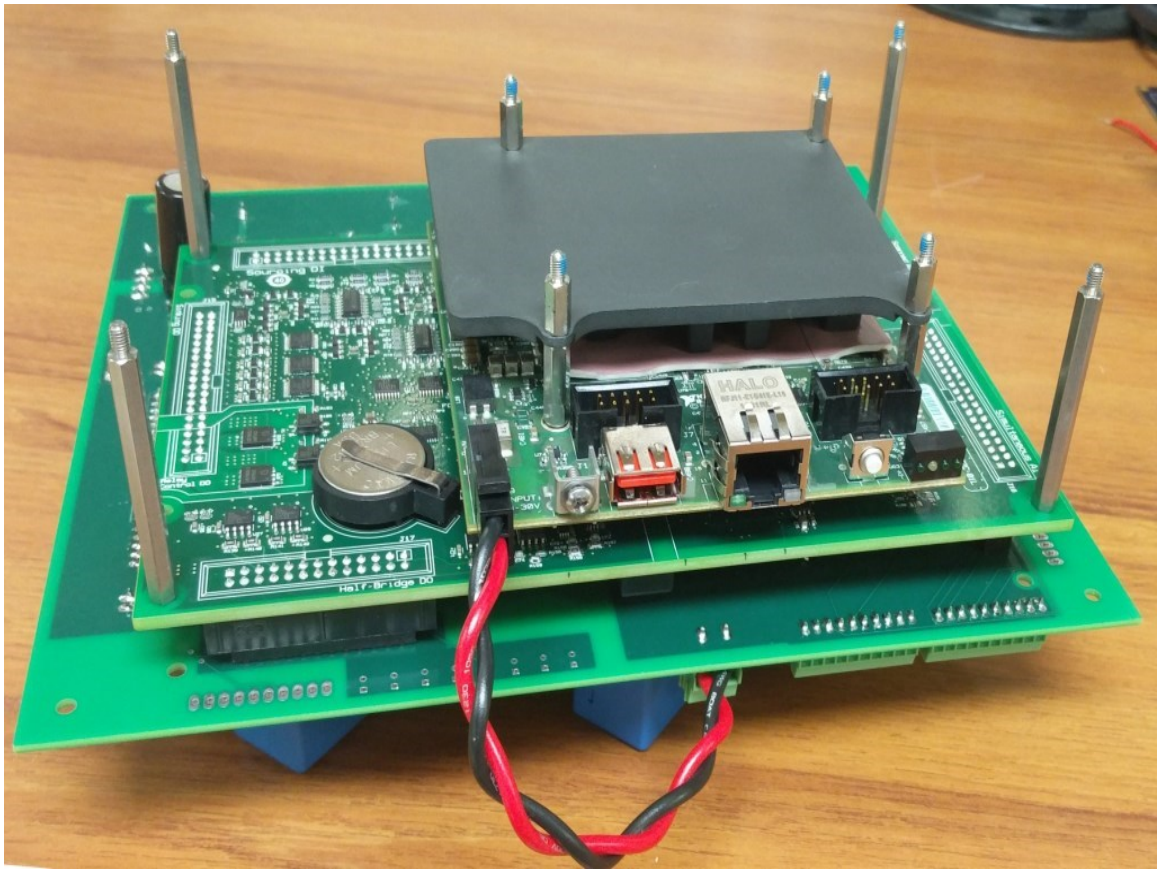

Figure 4.3: Bottom view of the designed interface board with the sbRIO GPIC on top

4.2.2 Power Stage

The first major piece in the construction of the power stage of the power converter is the IGBT switch module. Powerex® Intellimod® Module (IPM) PM75RSA060 was used for the power stage of the converter. This IPM consists of 7 IGBTs with anti-parallel diode across each of them. Six of the IGBTs form the two-level three phase inverter while the seventh IGBT is meant for braking circuit. The brake leg has not been used in this experimental work. The outline drawing of the IPM is shown in figure 4.4. It shows the internal layout and the on-board IGBT driver circuit on the PM75RSA060 [18]. As seen, it has six external power connections - two for dc-link connection, three for the inverter output, and one for the brake resistor.

The PM75RSA060 is rated for 75 A current and 600 V dc bus voltage. The maxi-

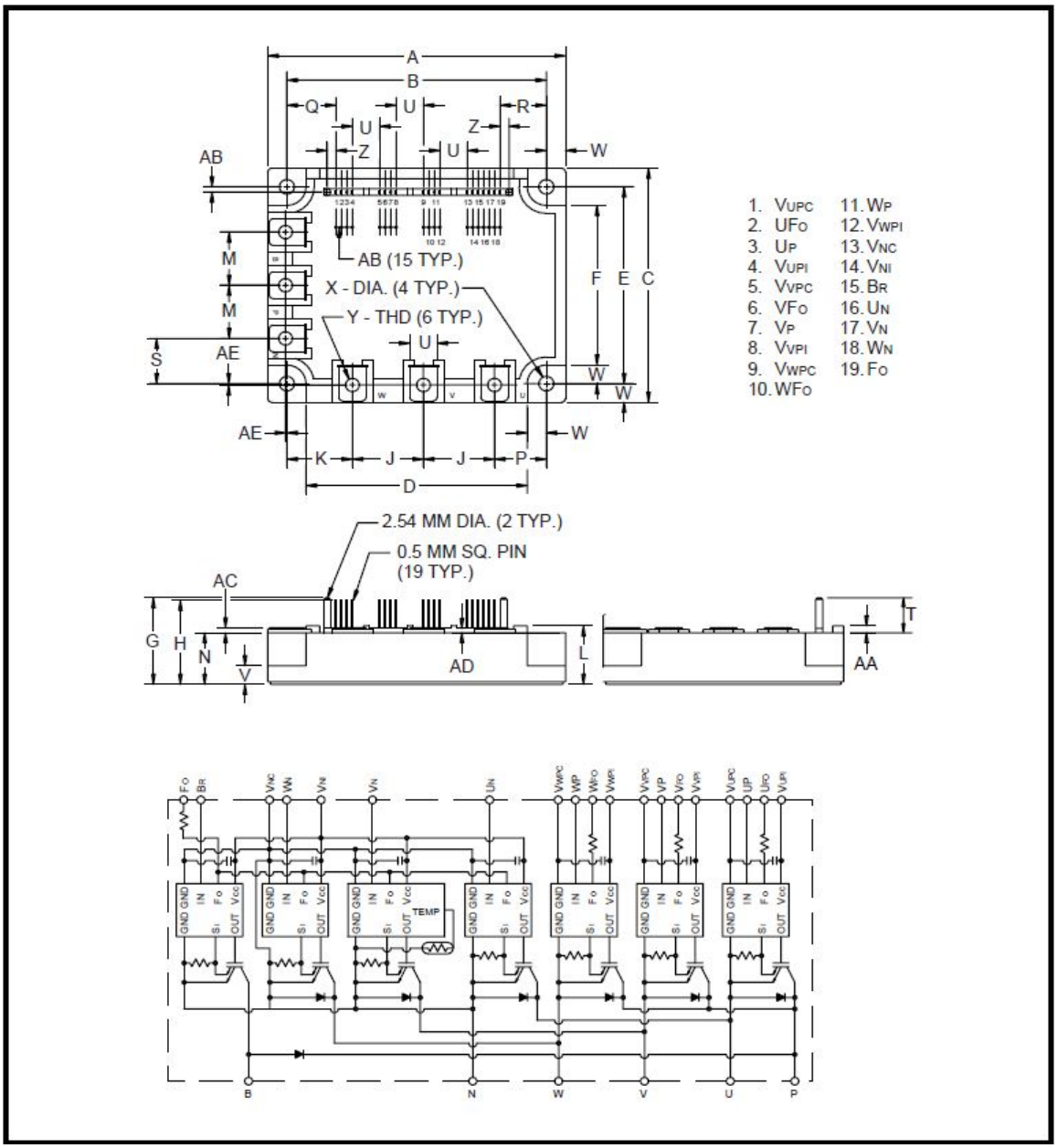

Figure 4.4: Circuit diagram for Powerex® Intellimod® PM75RSA060 IPM [18]

mum switching frequency allowed is 20kHz. Because the IPM may generate significant heat, enough to destroy the IGBT switches, the IPM was mounted directly on top of a heat sink.

As mentioned above, the PM75RSA060 IPM has a built in control circuit that reduces the need for an external gate driver. However it does require 4 isolated 15 V dc power

supplies - one each for the upper IGBT switches and one for all other IGBTs and the brake switch. The gate signals too must be isolated 15 V active-low gating. Therefore BP7B IPM interface boards by Powerex® was used for the interface between the controller and the IPM. The BP7B is a readily orderable interface board that offers complete isolation circuit for use with six and seven pack power IPMs.

The switching frequency for the converter was selected as 20 kHz. A 4700 μF dc-link capacitor was placed on the dc side of the power converter. A 100 Ω resistive dc-load was also placed on the dc side circuit to resemble the dc equivalent of the load seen by the converter. 4.2 mH filter inductor was used to connect the inverter setup to the 208 V three phase utility gird. The parameter used for the experimental setup for this work is given in table 4.1.

PARAMETER	***SYMBOL***	***VALUE***
rated r.m.s. grid voltage	v_{lls}	208 V
filter inductance	L	4.2 mH
filter resistance	R	0.01 Ω
dc link capacitor	C	4700 μF
dc voltage Source	V_b	400 V
baseload	R_b	100 Ω
switching frequency	f_{sw}	20 kHz
deadtime	t_{dead}	3 μsec
precharge resistor	R_p	10 Ω
outer loop proportional gain	K_{pv}	1
outer loop integral gain	K_{iv}	40
inner loop proportional gain	K_{pc}	15
inner loop integral gain	K_{ic}	1000

Table 4.1: System Parameters for Experimental work

Once the hardware setup was complete, the GPIC was programmed in labVIEW and the operation of the grid-connected power converter in both inverter mode and rectifier mode was verified. Finally the same principles were applied to the GPS capable converter as discussed below.

4.3 GPS Capable Power Converter and Controllers

After proper control of the grid-tied power converter was acheived using the GPIC, the GPS capable converter was built as part of the next phase. Experimental verification of the GPS capable converter required that the converter controller have access to a GPS time-source. Because connecting a GPS module to the GPIC board was outside the scope of this work, a CompactRIO (cRIO) platform was considered ideal for this use. A cRIO is another NI FPGA based reconfigurable I/O controller designed by National Instruments [19].

The cRIOs are FPGA based RIO devices with an embedded real-time controller and network communication capabilities along with multiple slots for C series modules. The flexibility offered due to the C series modules makes them ideal for the proposed experiment. These controllers offer a powerful control and are designed for ruggedness, reliability and I/O flexibility. Just like the GPIC, cRIOs are also programmed in LabVIEW environment. They provide a powerful combination of the FPGA and the RT-module that can work independently from each other. While control algorithms that require fast and deterministic execution are run on the FPGA along with the peripheral I/O functions, slower control algorithms can be run on the RT. The RT target on the cRIO are also capable of network communication. These features were ideal for building the GPS capable power converter where a GPS time-source along with network communication are crucial.

A prototype each for a grid side controller (GSC) and a converter side controller (CSC) were built in the laboratory for experimental verification of the proposed GPS capable power converter.

4.3.1 Grid Side Controller (GSC)

CompactRIO-9076 by National Instruments with C series modules NI 9225 for voltage sensing and NI 9467 for GPS time source was used for the proposed grid side controller. The grid side controller built for this experiment is shown in figure B.1. NI 9467 is a GPS timestamping and synchronizatoin module with a pulse per second accuracy of $\pm 100\ ns$ sourcing the absolute time synchronized to TAI. FPGA Timekeeper VI provided by National Instruments was used to acquire the time from NI 9467 to the FPGA. A screen shot of this timekeeper VI is provided in figure A.4 in the appendices section. Grid voltages were sampled at 50 kHz using NI 9225 which is a delta-sigma type analog-to-digital controller. The SRF-PLL algorithm was run at the same rate of 50 kHz as the analog sampling . The obtained phase angle of the grid was timestamped and transferred to the local controller, or the converter side controller, via network-published shared variable [20].

4.3.2 Converter Side Controller (CSC)

To verify the performance of the GPS capable power converter a three phase inverter prototype was built based on NI cRIO-9064 controller. The converter side controller built for this experiment is shown in figure B.2. NI 9467 was used for GPS timesource, NI 9220 was used for acquiring analog signals for the voltage and currents and NI 9401 was used for the digital I/O pins for gating the six switches on the power converter. The real-time controller on the cRIO 9064 reads the network-published shared variable to acquire timestamped angle measurement of the utility grid that was written by the GSC. Based on the time difference between the time-stamp on the received data and the current absolute time the current commanded phase angle is calculated as explained in earlier chapters.

The cRIO 9064 and the sbRIO-9607 GPIC have the same Zync-7020 FPGA hardware. This made transfer of converter control codes from the GPIC to the cRIO rather simple. Only minor changes were needed to implement the same type of control as used for the GPIC based power converter discussed earlier. The GPIC has a 12-bit simultaneous

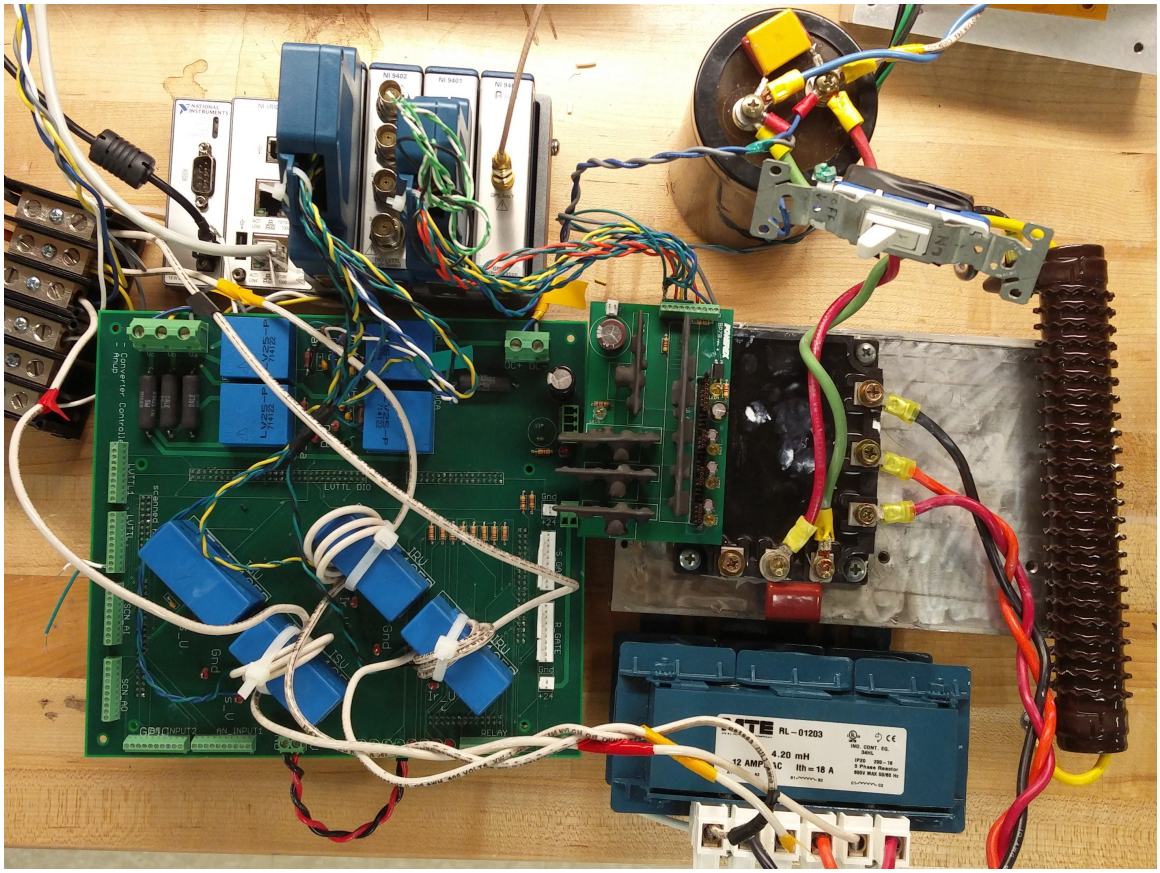

Figure 4.5: Laboratory setup of the Converter Side Controller and the power stage

analog input channel with analog voltage sensing range of ± 10 V. A similar analog input modules was used with the cRIO 9064 as well. NI 9220, a 16-bit simultaneous analog input C series module, was used for analog input sensing on the cRIO. Further because the NI 9220 has the same analog input sensing range of ± 10 V, the same interface board was used for signal conditioning. The hardware setup of the constructed grid side converter is shown in figure 4.5.

Chapter 5

Lab Results

This chapter presents the lab results that were obtained during the operation of the power converter built in the lab. All the experimental were carried out in the lab, so the converter was connected to the available 208 V three phase outlet on the lab and not directly on the utility side. First the results obtained with the GPIC based grid-tied power converter is presented. Results during system start-up, step responses, and steady state responses have been presented. Once the grid-tied inverter was operational, the local PLL codes were replaced by the GPS based PLL technique. The experimental results for the GPS-based grid-tied power converter have also been presented in this section. Both the converters were studied in rectifying mode and in inverting mode and the results have been presented for both modes of operation.

In the rectifying mode, the converter was run on dc voltage control mode where the command input is the dc bus voltage. For inverting mode, the outer voltage loop, or the dc voltage command loop, was removed completely. Instead constant 7 A of q-axis current and 0 A of d-axis current was commanded. These values were chosen so that the current waveform in both rectifying mode and inverting mode were comparable to one another for 400 V dc bus voltage. The results obtained during the experiment has been presented and conclusions that were drawn from the results have been presented at the end of this section.

5.1 Grid-tied Power Converter

5.1.1 Rectifying mode of operation

The system response during the start-up process of the converter is shown in figure 5.1. For operation in rectifier mode, the converter is first connected to the grid with all six IGBTs switched off. A 10 Ω precharge resistor is placed in series with the dc link capacitor to prevent in-rush currents and a 90 Ω resistor is placed as base load on the dc bus. As soon as the contactor is closed the capacitor voltage starts to rise gradually. The current magnitude is maximum at the start and reduces corresponding with the capacitor voltage rise. Once the capacitor has charged to about 275 V the transient current dies out. With the IGBT switches turned-off, the converter operates as a passive three phase diode-rectifier. This is why the current waveform in figure 5.1 is non-sinusoidal with a low power factor.

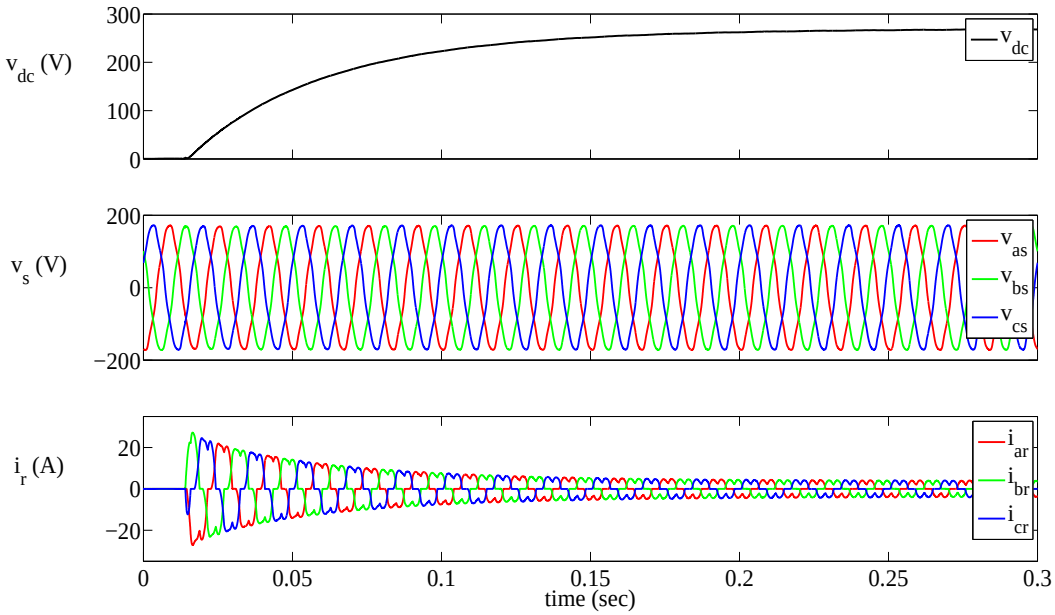

Figure 5.1: Converter response during start-up as passive rectifier

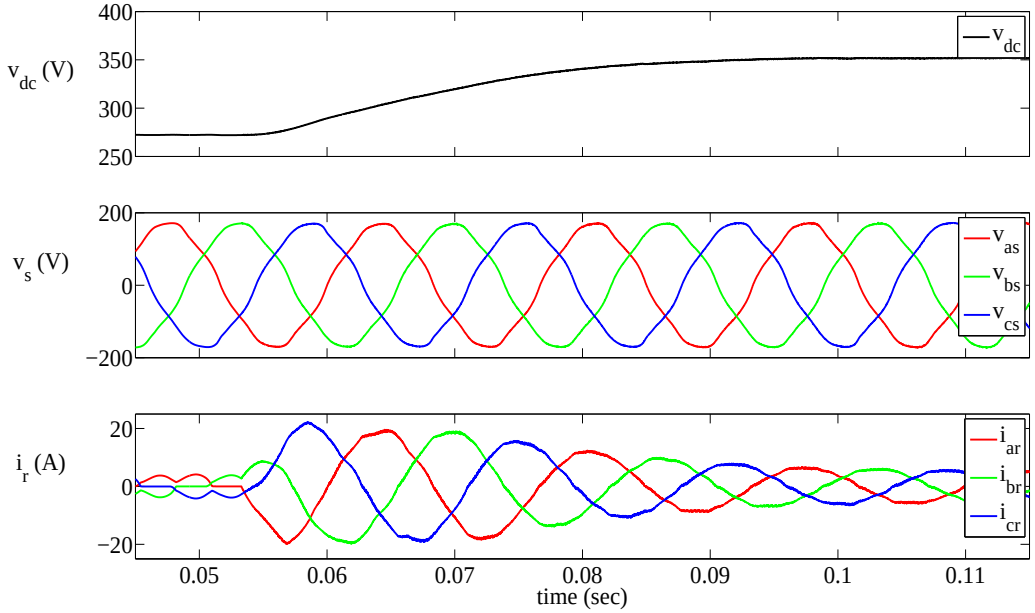

Figure 5.2: Converter response for gate turn on and 350 V commanded dc voltage

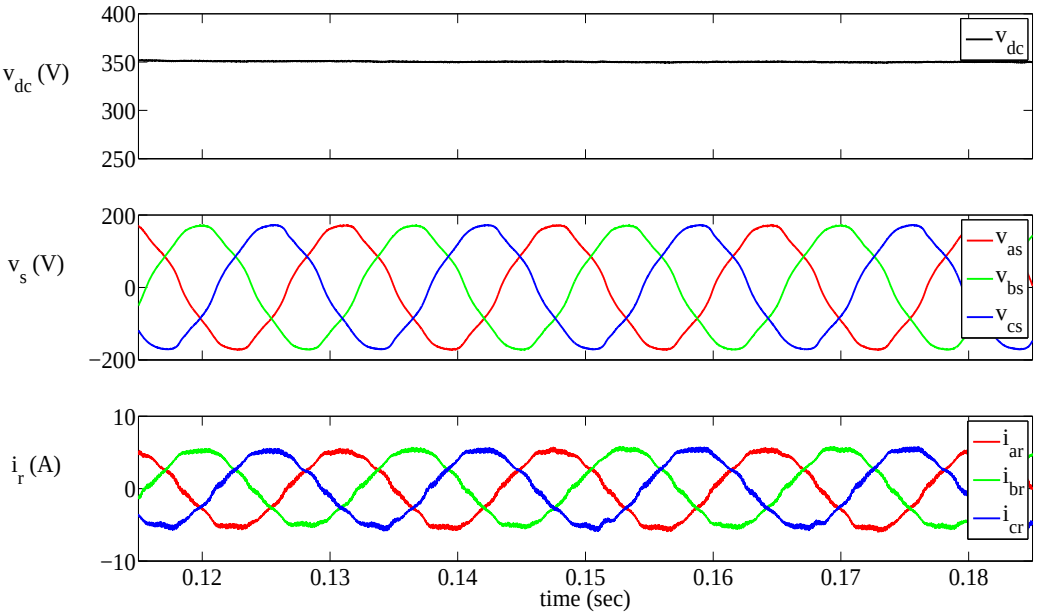

Figure 5.3: Steady state response of the converter for 350 V commanded dc voltage

After the capacitor had acquired a high enough voltage the precharge resistor was shorted out in order to avoid losses. Then the power converter was ready to operate in dc voltage control mode. Initially 350 V was commanded on the dc bus and the gate signals were turned on.

The transient response of the system during the turn on process is shown in figure 5.2. It can be seen that the transient current dies out in about 0.04 seconds and the dc bus voltage reached the commanded value of 350 V.

The steady state response of the system for a command of 350 V dc voltage is shown in figure 5.3. As expected, the power factor of the converter is very close to unity as the current waveforms are in phase with the voltage waveforms. In other words, the power converter is operating at unity power factor similar to a purely resistive load drawing only active power from the grid.

The system response for a step change in commanded dc bus voltage is shown in figure 5.4. Initially the converter dc bus voltage was 350 V, then a step change to 400 V was commanded. As seen in the figure, the current transient again only lasts for about 0.04 second. This is also the same time taken by the dc bus voltage to reach the commanded value of 400 V. The steady state response for the power converter for 400 V dc voltage is shown in figure 5.5.

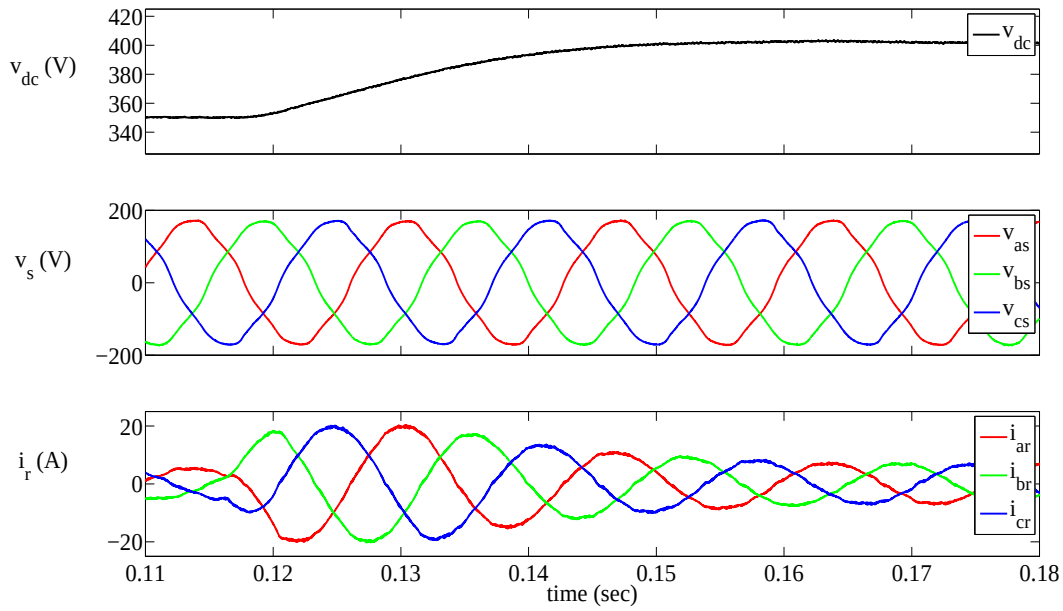

Figure 5.4: Step response for a step change in dc voltage from 350 V to 400 V

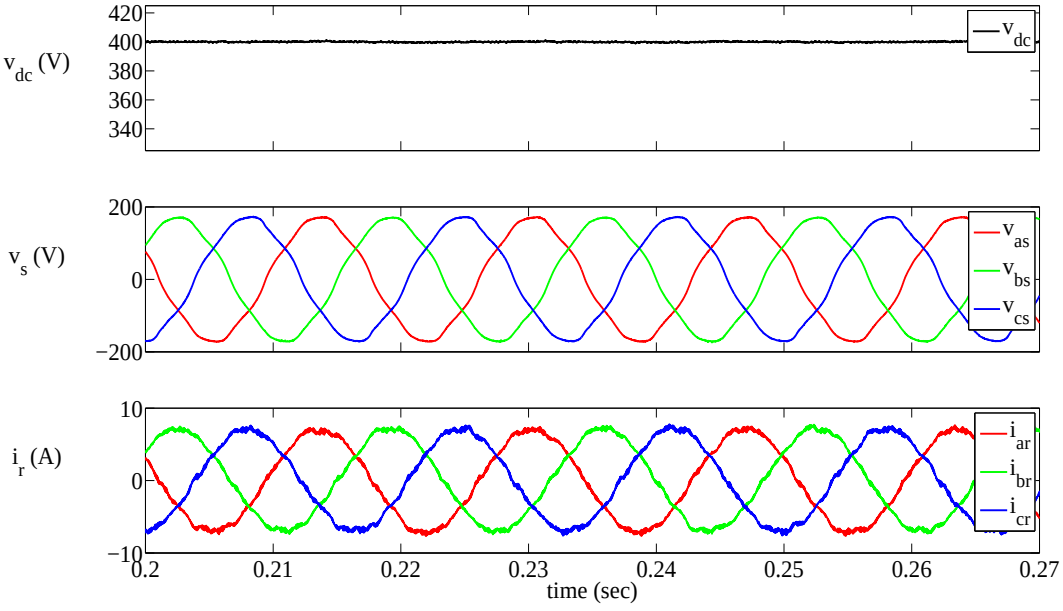

Figure 5.5: Steady state response of the converter for 400 V commanded dc voltage

5.1.2 Inverting Mode of Operation

For the study of the grid-tied power converter in inverter mode, the base load of 90 Ω was removed. Instead a 5 kW dc power supply was placed on the dc bus. The dc voltage output of the power supply is set at 400 V. In this work for the inverter mode study of converter, the outer control loop has been replaced by constant q- and d-axis demand current. Here constant 7 A q-axis current (i_{qs}) is commanded into the grid, while 0 A in commanded in the d-axis (i_{ds}).

Figure 5.6 showns the observed response of the power converter system in inverter mode. First the converter is synchronized to the grid. At the moment of contactor closing, 0 A of current is commanded. Only after 1 msec of the contactor closing, q-axis demand current is stepped to 7 A from 0 A. The high-frequency noise seen in the current waveform is due to the switching frequency noise on the dc bus votlage introduced by the dc power supply.

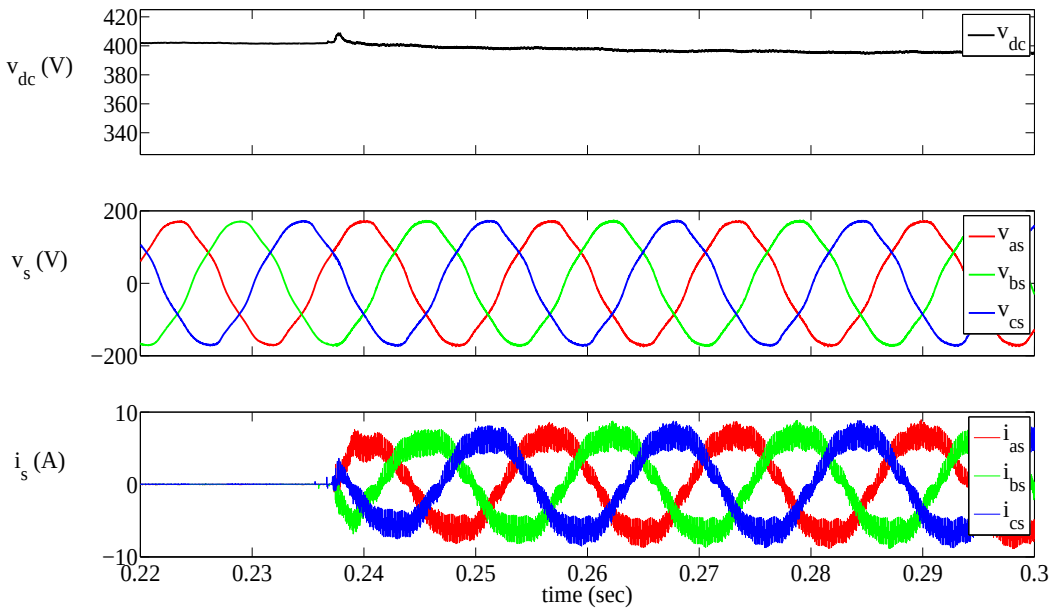

Figure 5.6: Three phase voltages and currents in inverting mode for 7 A commanded i_{qs}

5.2 GPS Capable Power Converter

As already mentioned in previous chapter, for the study of GPS capable power converter a laboratory prototype of a grid side controller (GSC) and a converter side controller (CSC) was built. The GSC was based on NI cRIO 9076 while the CSC was based on NI cRIO 9064. To verify that a smart inverter may be synchronized to the grid even with complete absence of grid-voltage sensors or a local PLL algorithms, the prototyped GPS capable converter was tested for similar conditions as the grid-tied converter discussed above. The results obtained have been presented in this section. In the plots presented, the phase angle estimate ($\hat{\theta_e}$) based on the GPS data along with estimated network delay (dT) has also been plotted.

5.2.1 Rectifying mode of operation

For the rectifier mode of operation, the initial capacitor charging phase has not been shown. Figure 5.7 shows the operation of the GPS capable converter during start-up. The plot is comparable to the one shown in figure 5.2. The system reaches steady state very quickly and dc voltage acquires the commanded value of 350 V. The steady state response of the converter for 350 V dc voltage is shown in figure 5.8.

Figure 5.9 shown the response of the GPS capable converter in rectifying mode for a step change in commanded dc voltage. The transient response of the sytem can be clearly observed for a step change in command from 350 V to 400 V dc. The steady state response of the power converter for 400 V commanded dc voltage is also shown in figure 5.10.

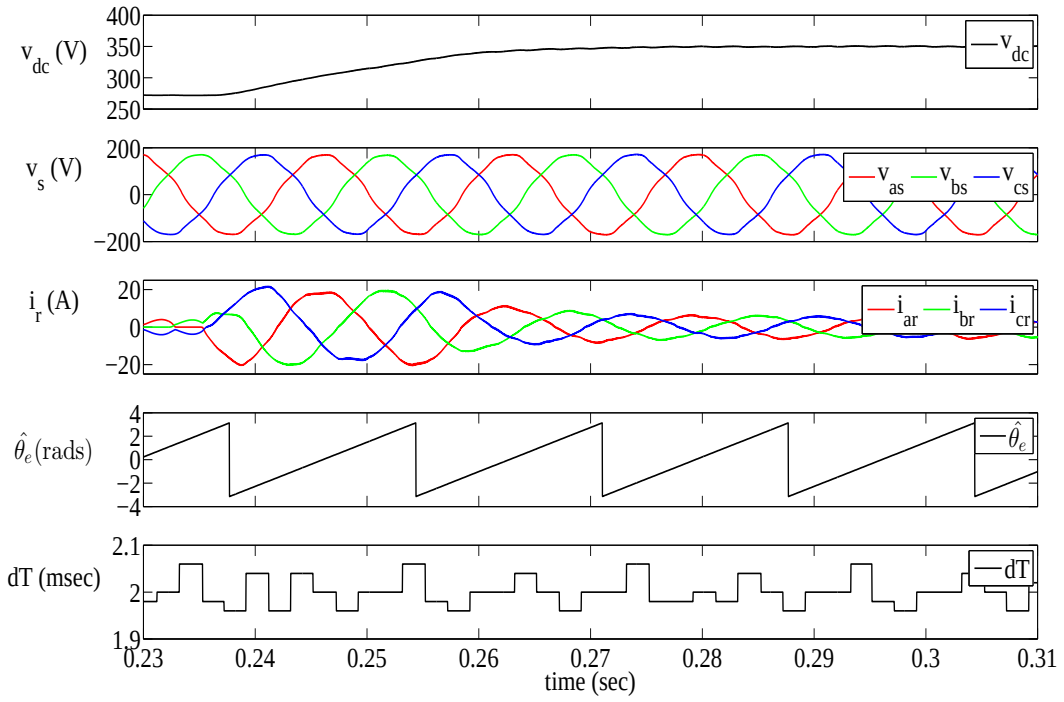

Figure 5.7: GPS capable converter response during gate turn on and 350 V dc command

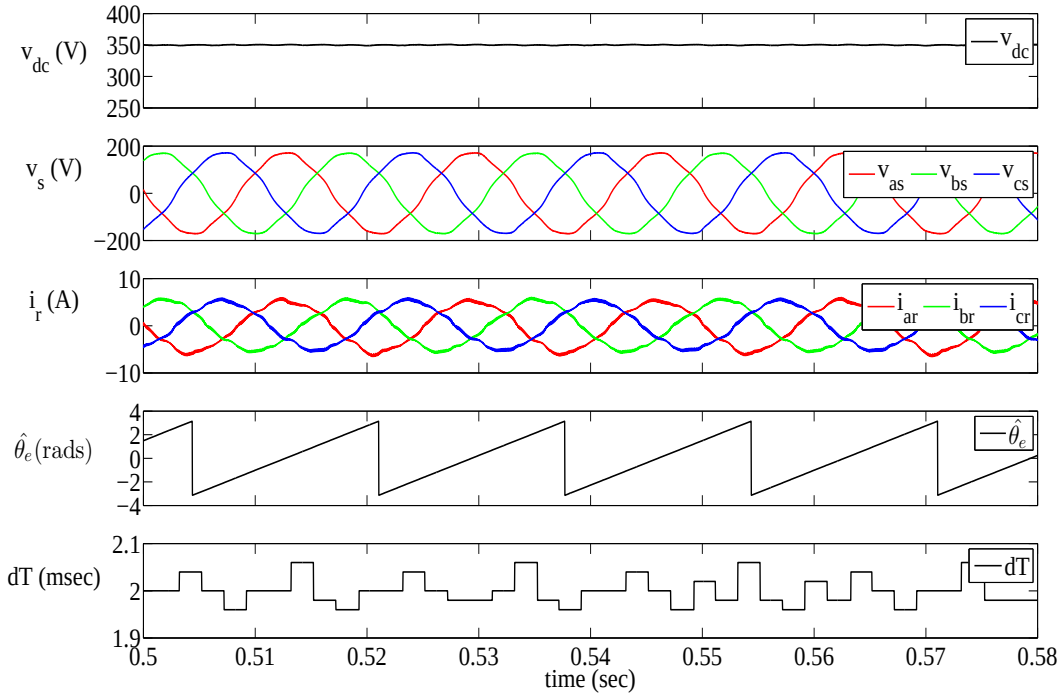

Figure 5.8: Steady steady response of GPS capable converter for 350 V commanded dc voltage

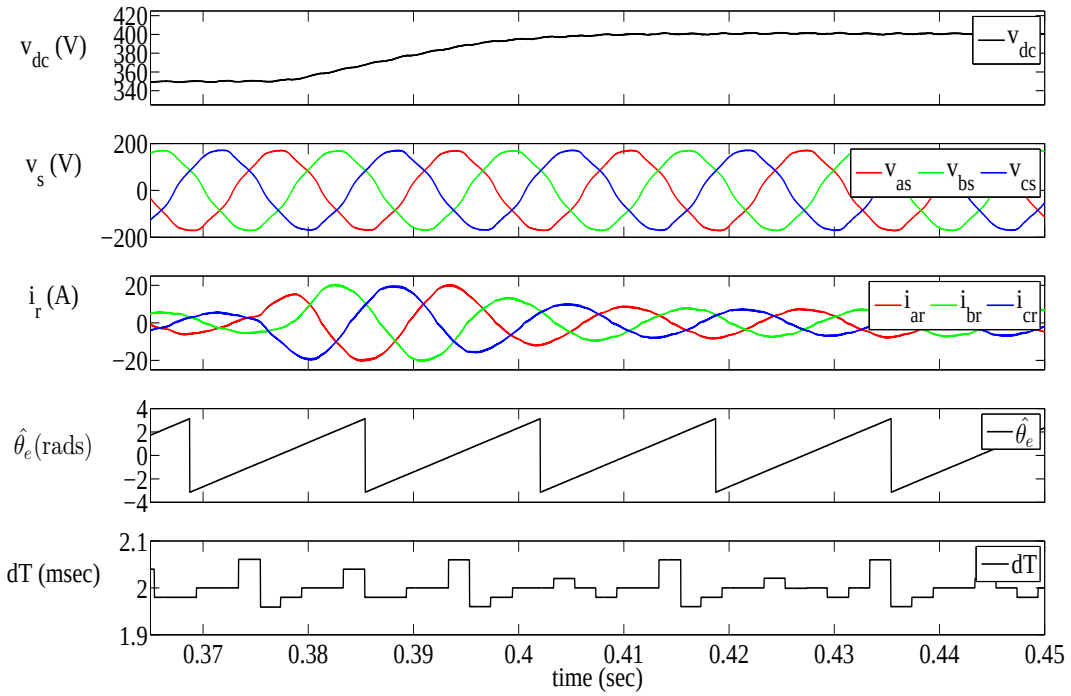

Figure 5.9: Step response of GPS capable converter step change from 350 V to 400 V dc command

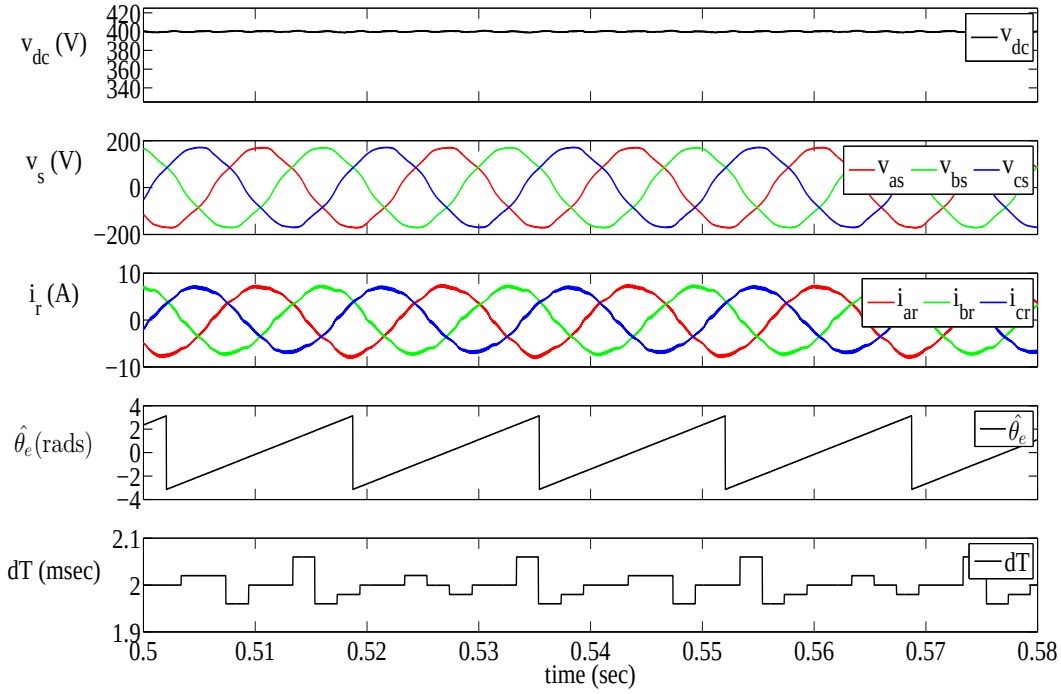

Figure 5.10: Steady steady response of GPS capable converter for 400 V commanded dc voltage

5.2.2 Inverting Mode of Operation

Figure 5.11 shows the plots for converter in inverting mode of operation. Here again, the outer voltage control loop has been replaced by constant current demands. The results presented is for 7 A of q-axis current and 0 A of d-axis current injection from the converter to the utility grid. The total power flowing from the converter into the grid was calculated as 1.785 kW and the power factor was close to unity.

For the inversion mode, a 5 kW programmable dc power supply was used to source the inverter on the dc side. The dc voltage was set as 400 V. While we have assumed that v_{qs}^{e} is a constant 170 V and v_{ds}^{e} is zero, this is almost never true in reality. Also because the connection was made on the lab voltage and not directly on the utility side, their was presence of harmonics on the voltages at the point of coupling. This is due to the non-linear loads connected to the lab voltages. Due to the presence of harmonics, the q- and d-axis quantities will have a harmonic ac quantity superimposed on the expected dc quantities. This harmonics in the grid voltage waveform induce harmonics in the current as well which is seen in the current plot for inverting mode.

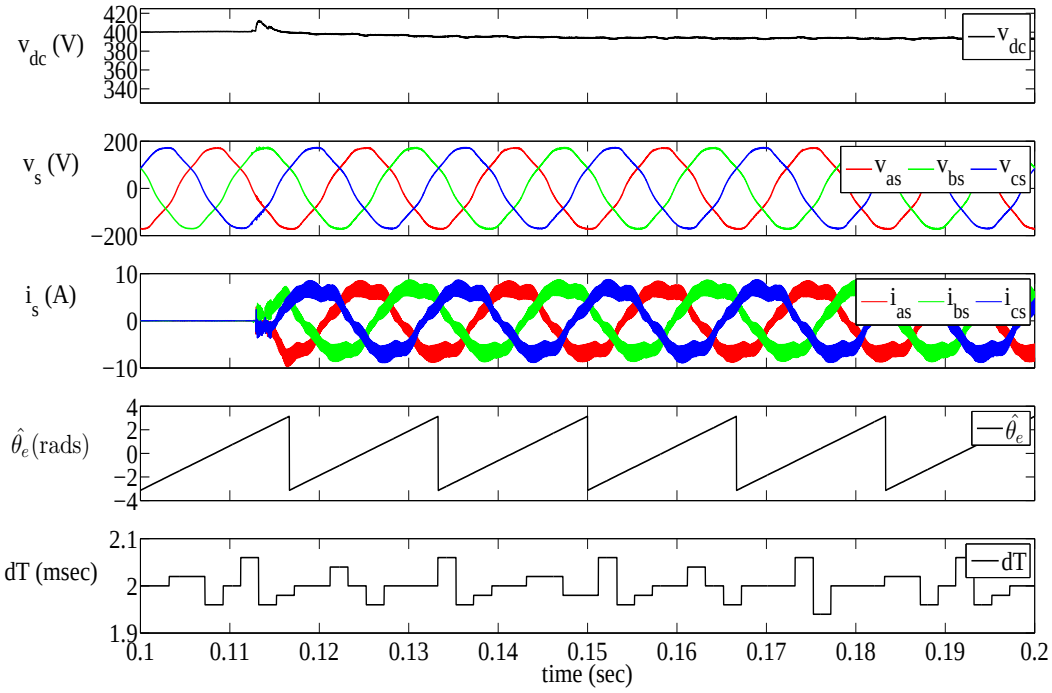

Figure 5.11: Response of the GPS capable converter in inverting mode of operation

5.3 Summary of Lab Results

This chapter presented the results for the experimental tests that were performed for both the grid-tied power converter and the GPS capable power converter. Figures 5.1, 5.2, 5.3, 5.4, 5.5 and 5.6 validate the control methods for the grid-tied power converter discussed in this thesis work for both rectifying mode of operation and inverting mode of operation. The intended unity power factor operation on the converter was successfully acheived in both the modes. Also a very good dc voltage regulation was observed in the dc voltage control mode. The same can be stated for inverting mode of operation. However, in the inverting mode a high current ripple was observed. This is believed to be because of the switching noise of the dc power supply that was used for clamping the dc bus voltage in inverting mode.

The results obtained for the GPS capable power converter were also presented in this section. Figures 5.7, 5.8, 5.9, 5.10 and 5.11 show that the GPS based grid-synchronization techniques suggested in this thesis work can be used for proper converter synchronization. Further the three phase currents and voltages waveforms in shown figures 5.7, 5.8, 5.9, 5.10 and 5.11 closely match those in figures 5.1, 5.2, 5.3, 5.4, 5.5 and 5.6. The estimated grid angle based on GPS data has also been plotted for the GPS capable power converter case. The results obtained validate that both local PLL technique and GPS based synchronization technique can be used for grid-synchronization of smart inverters.

Chapter 6

Conclusion

A GPS capable bi-directional power converter has been proposed in this thesis work. A prototype of a grid side controller and a converter side controller were built using National Instrument's CompactRIO controllers. NI cRIO 9076 was used as the grid side controller while NI 9064 was used as the converter side controller. It was experimentally verified that a reliable GPS time-source along with IP network communication capabilities can be used to synchronize converters at remote locations even in the absence of local voltage sensors and phase-locked loop code. This opens up the possibility for any new power converter placed in a microgrid to come online using IP communication and a GPS time-source which are commonly built into present-date smart inverters. Further this also opens the possibility of utilizing phasor measurement unit (PMU) data in power electronic applications. In fact when the grid side converter is replaced by a PMU, positive sequence voltage angle, grid frequency and rate of change of frequency will be available to the smart inverter. These added measurement can directly be used to improve the angle estimation algorithm used in this work, thus improving the overall performance of such a converter. As more and more PMU are being installed in the grid, and with the recent development of the μPMU technology for the distribution system, a GPS capable converter can be a new feature of the smart grid technology.

Appendices

Appendix A LabVIEW FPGA Codes

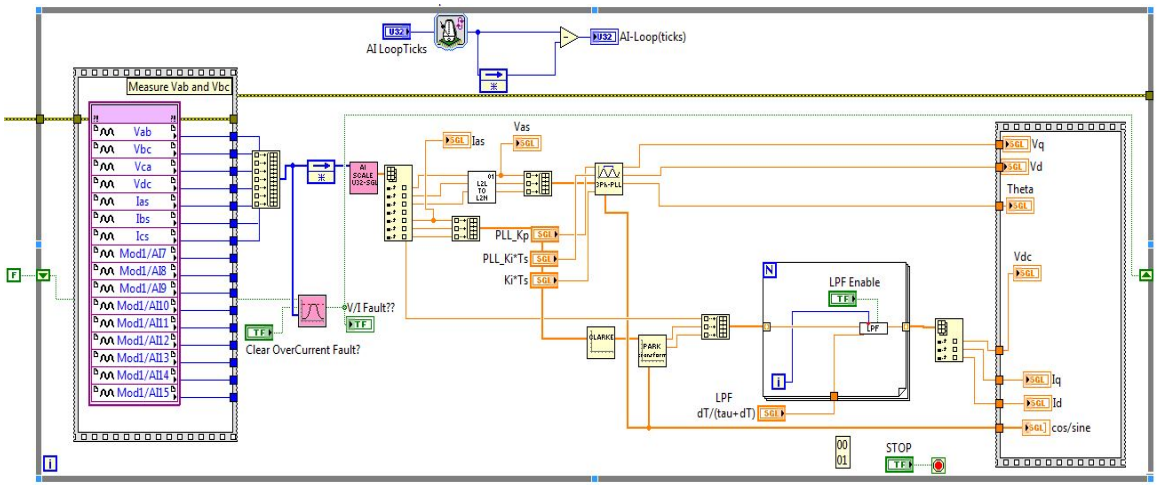

Figure A.1: Analog sensing and abc-to-qd reference frame transformation loop

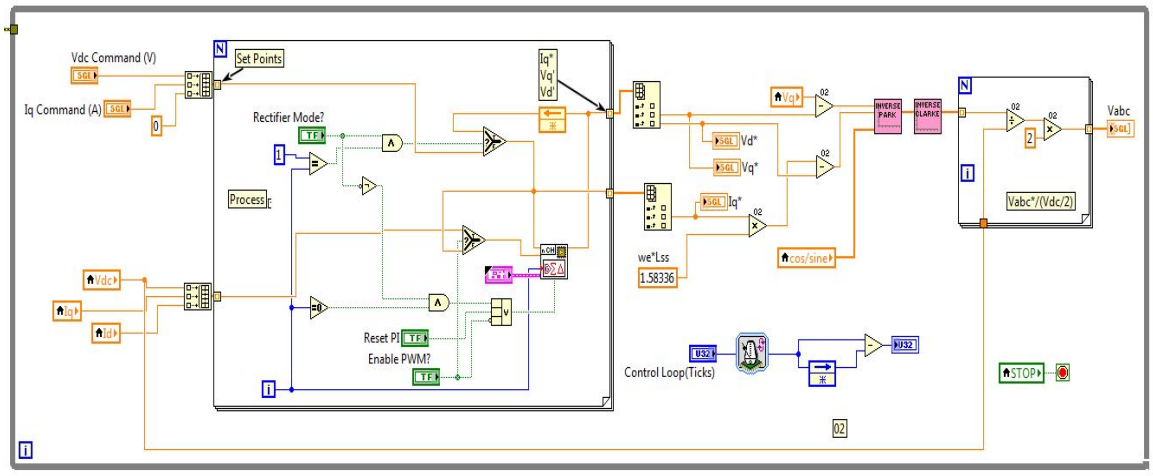

Figure A.2: Post transformation converter control loop

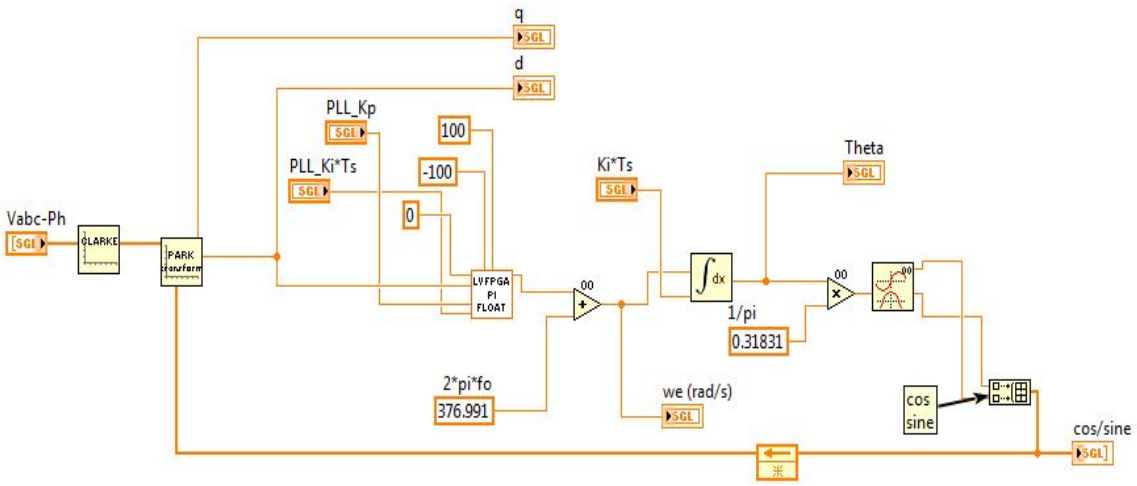

Figure A.3: LabVIEW codes for $3-\phi$ SRF-PLL subVI

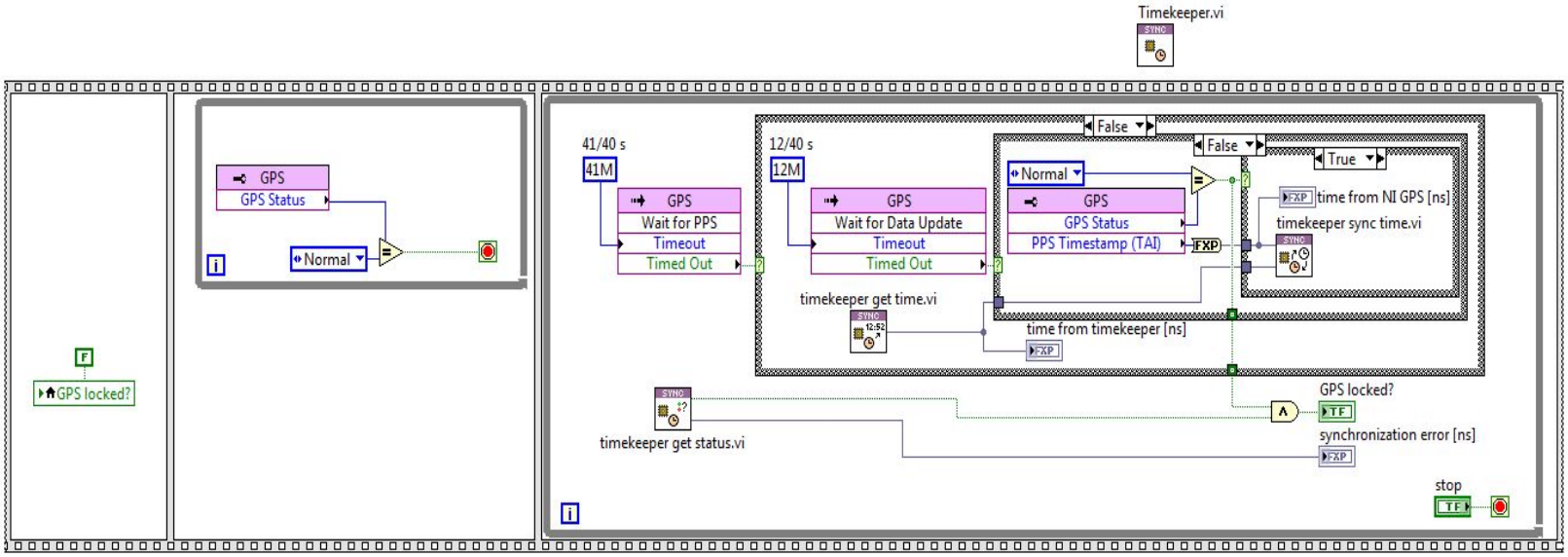

Figure A.4: Timekeeper VI for GPS time acquisition from NI 9467 GPS Timestampping and Synchronization Module

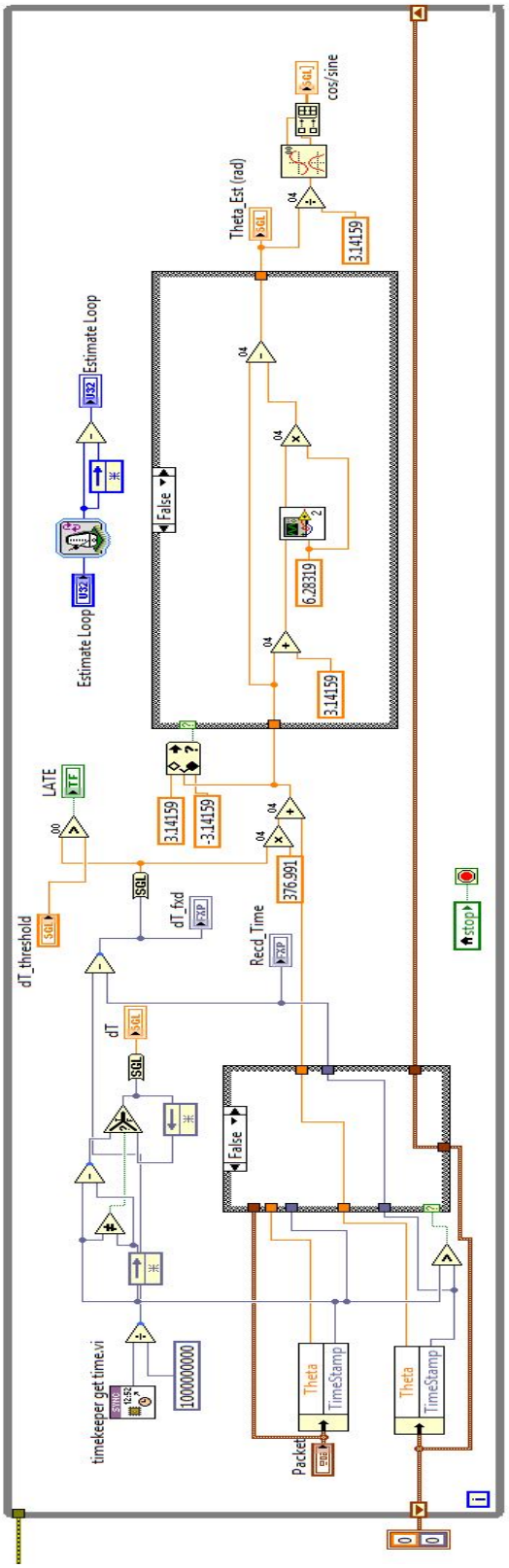

Figure A.5: GPS-time based angle estimation loop

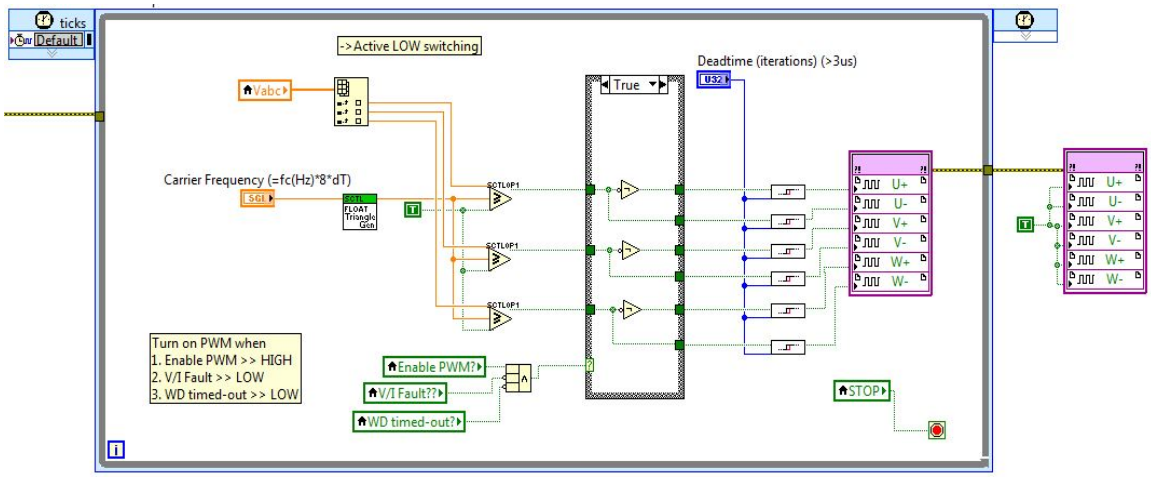

Figure A.6: Sine-triangle PWM loop

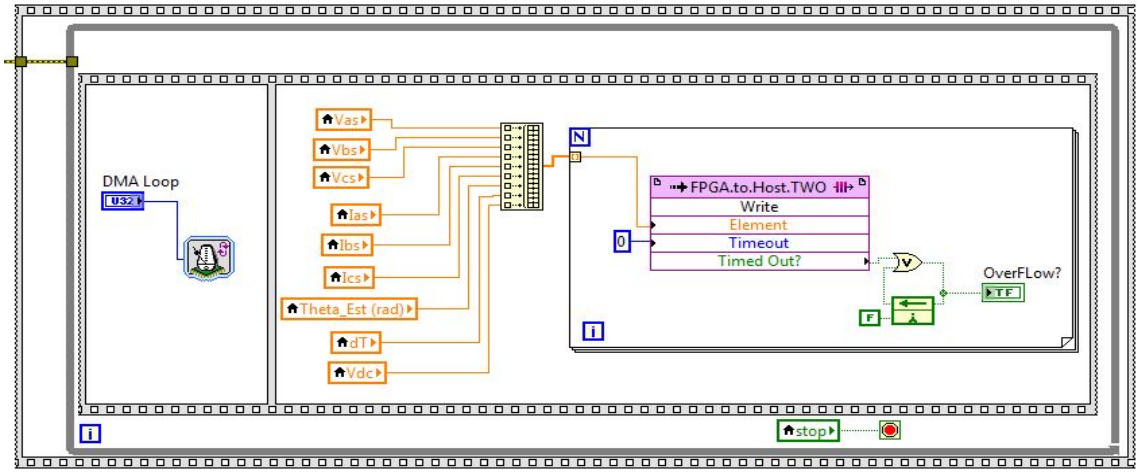

Figure A.7: Analog data stream loop with DMA FIFO

Figure A.8: Front Panel view of labVIEW FPGA VI

Appendix B Experimental Setup Pictures

Figure B.1: NI CompactRIO 9076 used for *Grid Side Controller* prototype with C series modules NI 9225, NI 9402 and NI 9467

Figure B.2: NI CompactRIO 9064 used for *Converter Side Controller* prototype with C series modules NI 9220, NI 9401 and NI 9467

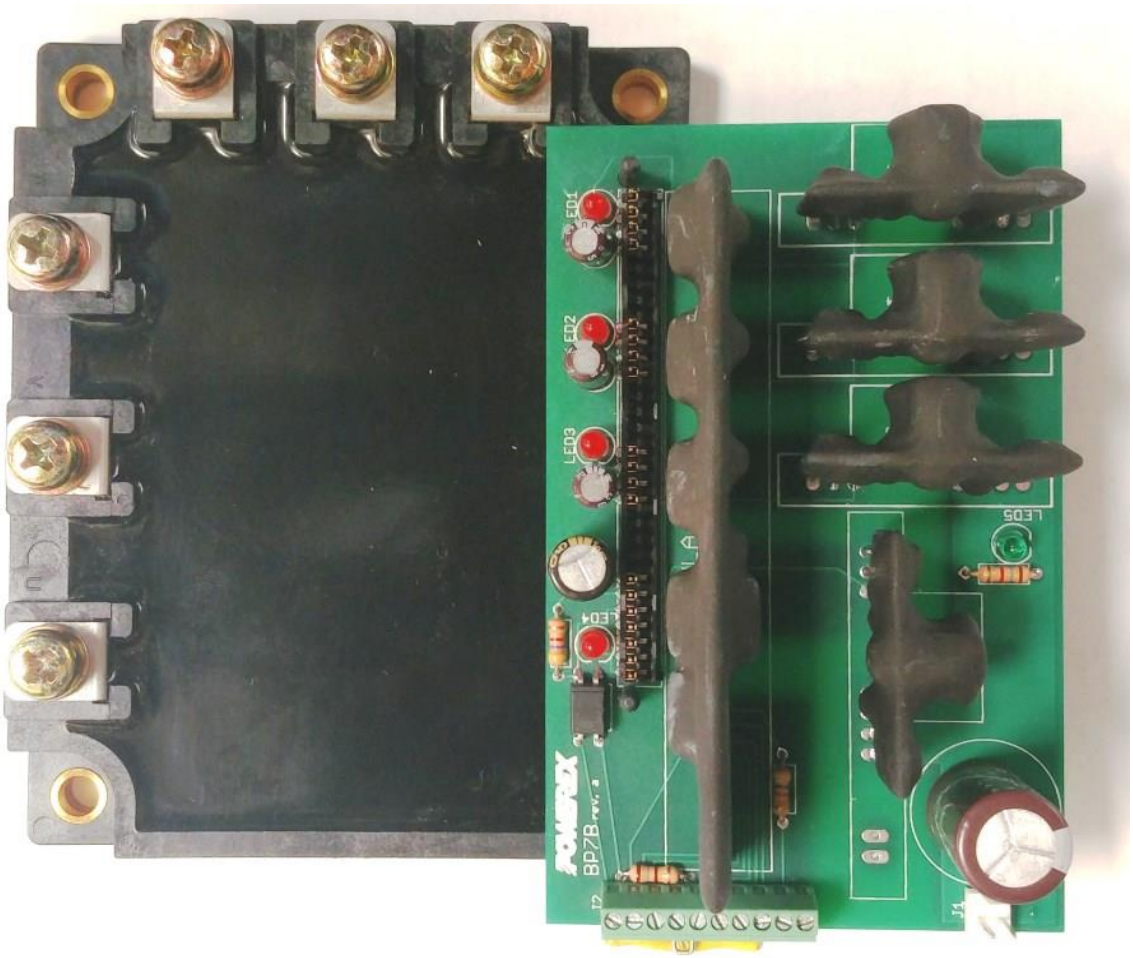

Figure B.3: Intellimod® Module PM75RSA060 used as IGBT 6-pack and IPM driver BP7B

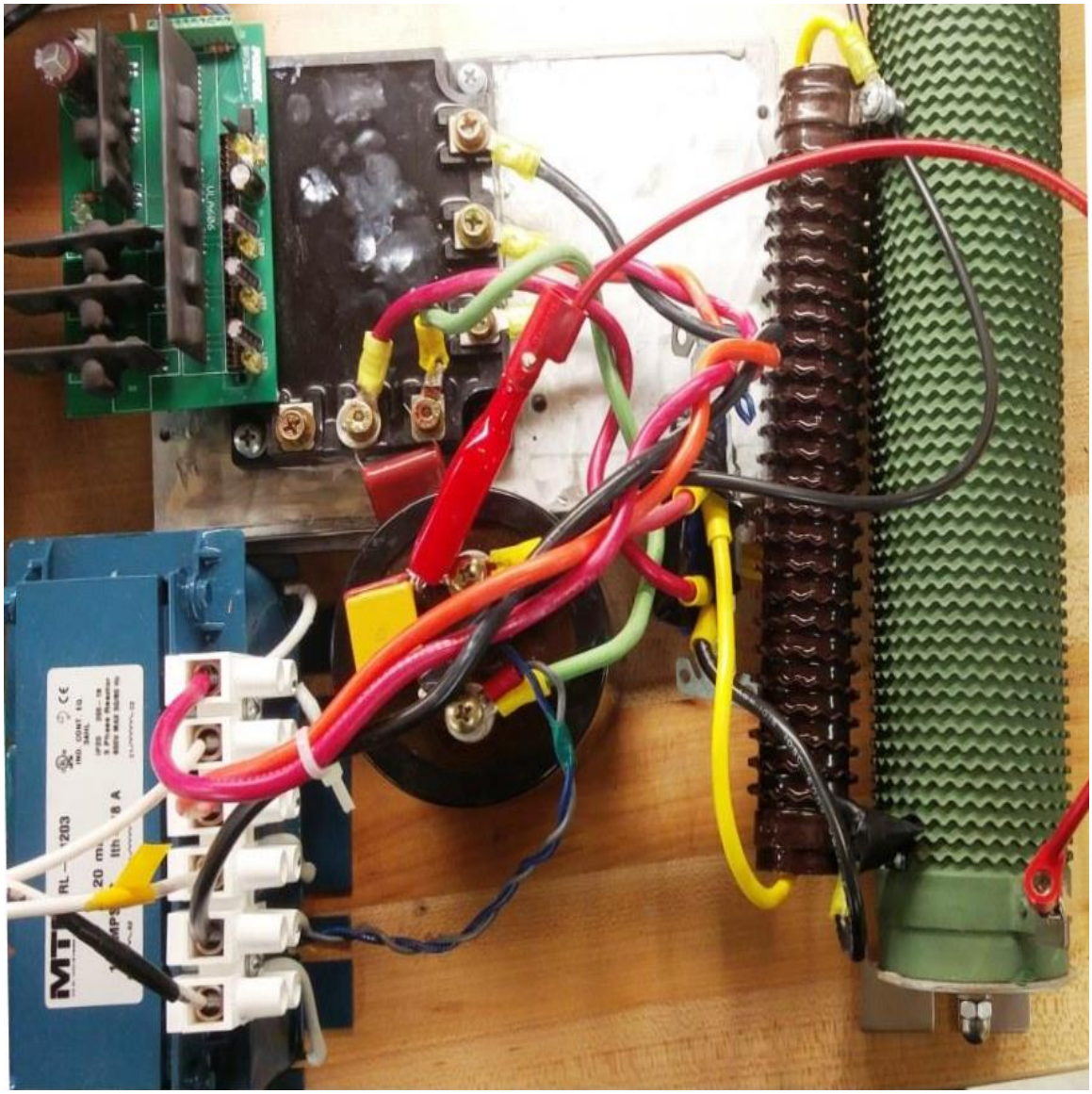

Figure B.4: Power Stage of the converter setup with filter inductor, IGBT 6-pack, precharge resistor and baseload resistor shown

Bibliography

[1] H. Farhangi. "The path of the smart grid," *Power and energy magazine, IEEE*, 8(1):18–28, 2010.

[2] R Nicolosi, L Piegari, and Benigni A. "A smart pv inverter controller with pmu capability," in *Clemson Power System Conference*, 2016.

[3] W. Ren, R. W. Delmerico, K. A. O'brien, and Y. Pan. "Power converter and methods of controlling the same," January 27 2015. US Patent 8,942,856.

[4] S. Wang, X. Meng, and T. Chen. "Wide-area control of power systems through delayed network communication," *Control Systems Technology, IEEE Transactions on*, 20(2):495–503, 2012.

[5] J. Rocabert, A. Luna, F. Blaabjerg, and P. Rodriguez. "Control of power converters in ac microgrids," *Power Electronics, IEEE Transactions on*, 27(11):4734–4749, 2012.

[6] P. C. Krause, O. Wasynczuk, S. D. Sudhoff, and S. Pekarek. *Analysis of electric machinery and drive systems*, volume 75. John Wiley & Sons, 2013.

[7] R. H. Park. "Two-reaction theory of synchronous machines generalized method of analysis-part i," *American Institute of Electrical Engineers, Transactions of the*, 48(3):716–727, 1929.

[8] G. Kron. *Equivalent circuits of electric machinery,*. J. Wiley & Sons, 1951.

[9] D. S. Brereton, D. G Lewis, and C. C Young. "Representation of induction-motor loads during power-system stability studies," *Power Apparatus and Systems, Part III. Transactions of the American Institute of Electrical Engineers*, 76(3):451–460, 1957.

[10] R. W. De Doncker and J. P. Lyons. "Control of three-phase power supplies for ultra low THD," in *Appl. Power Electron. Cong.*, Dallas, TX, Mar. 10-15, 1991.

[11] T. C Green and M Prodanović. "Control of inverter-based micro-grids," *Electric Power Systems Research*, 77(9):1204–1213, 2007.

[12] P. Rodríguez, J. Pou, J. Bergas, J. I. Candela, R. P. Burgos, and D. Boroyevich. "Decoupled double synchronous reference frame pll for power converters control," *Power Electronics, IEEE Transactions on*, 22(2):584–592, 2007.

[13] G. -C. Hsieh and J. C. Hung. "Phase-locked loop techniques. a survey," *Industrial Electronics, IEEE Transactions on*, 43(6):609–615, 1996.

[14] X. -Q. Guo, W. -Y. Wu, and H. -R. Gu. "Phase locked loop and synchronization methods for grid-interfaced converters: a review," *PRZEGLAD ELEKTROTECHNICZNY (Electric Rev)*, 87(4):182–187, 2011.

[15] A. G. Phadke and J. S. Thorp. *Synchronized phasor measurements and their applications*. Springer Science & Business Media, 2008.

[16] National Instruments The LabVIEW RIO Architecture : A Foundation for Innovation. http://www.ni.com/white-paper/10894/en/

[17] National Instruments Single Board RIO - General Purpose Inverter Controller. http://www.ni.com/singleboard/gpic/

[18] Powerex Inc., "PM75RSA060 Datasheet". *Intellimod® Modules*. Sep. 2000. http://www.pwrx.com/pwrx/docs/pm75rsa060.pdf

[19] National Instruments CompactRIO - reconfigurable controller. http://www.ni.com/compactrio/

[20] National Instruments - Using the LabVIEW Shared Variable. http://www.ni.com/white-paper/4679/en/