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High Frequency Devices and Circuit Modules for Biochemical Microsystems

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HIGH FREQUENCY DEVICES AND CIRCUIT MODULES FOR BIOCHEMICAL MICROSYSTEMS

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ABSTRACT

This dissertation investigates high frequency devices and circuit modules for biochemical microsystems. These modules are designed towards replacing external bulky laboratory instruments and integrating with biochemical microsystems to generate and analyze signals in frequency and time domain. The first is a charge pump circuit with modified triple well diodes, which is used as an on-chip power supply. The second is an on-chip pulse generation circuit to generate high voltage short pulses. It includes a pulse-forming-line (PFL) based pulse generation circuit, a Marx generator and a Blumlein generator. The third is a six-port circuit based on four quadrature hybrids with 2.0~6.0 GHz operating frequency tuning range for analyzing signals in frequency domain on-chip. The fourth is a high-speed sample-and-hold circuit (SHC) with a 13.3 Gs/s sampling rate and ~11.5 GHz input bandwidth for analyzing signals in time domain on-chip. The fifth is a novel electron spin resonance (ESR) spectroscopy with high-sensitivity and wide frequency tuning range.

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CHAPTER ONE

INTRODUCTION

Over the past 25 years, there is a rapid development and increasing interest of micro total analysis systems (μTAS) [1.1]-[1.5]. Micro total analysis system, sometimes called lab-on-a-chip, is used to integrate one or several laboratory functions on a single chip. In 1975, the first analytical miniaturized device [1.6], a gas chromatographic analyzer, was developed to separate a simple mixture of compounds in a matter of seconds. In 1990, a miniaturized open-tubular liquid chromatograph based on silicon chip technology was presented by Manz and co-workers [1.7]. At the same time, the concept of "miniaturized total chemical analysis system" or μTAS was proposed by Manz, in which silicon chip analyzers incorporating sample pretreatment, separation, and detection devices were used to integrate a capillary electrophoresis on a chip [1.8]. Applications of micro total analysis systems span basic-science research, clinical medicine, diagnostics, environment, cellular studies, and field work. During the last several years, micro total analysis systems have extended their usefulness into many new fields. They are relatively new group of analytical tools, capable of analyzing DNA, proteins, cells, macromolecules, toxins or pathogens [1.9]. The ability of performing laboratory functions on a chip has opened new ways in modern analytical chemistry, medicine, genetic, cell biology and many other research areas.

Recently, microfluidic and nanofluidic devices are as a subject of extensive research, for molecular analysis, biodefence, molecular biology and microelectronics [1.10]. They can obtain high sensitivity and high resolution by using very small volumes

of samples and fluids, which are regarded as the most powerful advantage of μTAS or lab-on-chip. For organism studies, microfluidic devices have provided controllable and sensitive analysis of small organisms, such as plants, protozoa, zebrafish, and worms [1.11]. Recent microfluidic technology has generated on chip mimics of angiogenesis and mechanical stimuli of organ systems [1.12]-[1.13]. Microfluidic and nanofluidic devices have been used for wide range of practical applications, including drug screening, drug synthesis, packaging, and formulation, water testing, biomedical science, cell biology, and chemistry [1.14]-[1.15]. Until now, successful microfluidic and nanofluidic devices have been used for clinical analysis with the following functions: handing of soluble, detecting pathogens in blood, and analysis of intact cells [1.16].

Although micro total analysis systems have gradually gained maturity, many of them need to connect to off-chip bulky instruments, including sampling units, electronic units and detector units, which cannot realize true lab-on-a-chip. A true lab-on-a-chip should not require an external laboratory to support its operation. These external units are used to provide signals to μTAS and analyze signals generated by μTAS in frequency and time domain. Thus, the benefits of small size and low complexity that have contributed to the popularity of microsystems have been somewhat lost. For further developing and minimizing μTAS, some external instruments for generating and analyzing signals are needed to be demonstrated to realize on chip. When fully developed, micro total analysis systems, which in themselves are completely equipped laboratory units applied to diagnostic, point-of-care (POC), clinical and environmental laboratory, are claimed to be low-cost, easy-to-use, portable and equipment-free. In the

developing countries, with limited resources, the healthcare infrastructure is less well developed. In this case, μTAS that do not rely on complicated instrumentation for result interpretation are extremely useful platform to provide affordable disease diagnosis and environmental monitoring to people living in the developing world.

Up to this time, our group members have successfully reported label-free and non-invasive detection methods for the development of micro-total-analysis-systems. In [1.17], a high-sensitive on-chip radio frequency (RF) device is proposed to detect small dielectric property changes in microfluidic channels. In [1.18], Yang demonstrated a simple, ultra sensitive RF sensor to detect a single yeast cell and distinguish its viability in a microfluidic channel. In [1.19], Cui reported a tunable and highly sensitive RF sensor with tunable attenuators and phase shifters to measure the permittivity of materials in a microfluidic channel or nanofluidic channel. These proposed sensors are suited for biochemical applications, bio-analysis, biomedical, cell biology studies and clinical disease diagnostics. In the dissertation, a few integrated RF/microwave circuits and devices have been designed and demonstrated for the development of on-chip analytical tools, pulse generators and electron paramagnetic resonance (EPR) spectroscopy. These RF circuits, instead of some external bulky laboratory instruments, can be integrated with our biochemical microsystems and sensors to generate and analyze signals in frequency and time domain, which is great interest of the development of laboratory chips fully equipped laboratory units.

Below is an outline of this dissertation, each chapter covers a high frequency circuit or device topic:

Chapter II presents charge pump circuits with modified triple well diodes as charge transfer switches. Model parameters of the modified triple well diode are extracted based on measured diode characteristics.

Chapter III presents three types of CMOS pulse generation circuits, including a PFL-based pulse generation circuit with the stacked-MOSFET high voltage switch, an on-chip Marx generator and a Blumlein pulse generator. Generating high voltage short pulses is important for functionality integration, such as micro/nano electromechanical systems (MEMS/NEMS) actuation, electrophoresis, electroporation. The high voltage switch and the PFL-based pulse generation circuit are modeled and analyzed. All these pulse generators are implemented in a 0.13 μm CMOS process.

Chapter IV presents a highly reconfigurable, low-power, and compact directional coupler. The active inductors and varactors are used in this directional coupler to tune operating frequencies and coupling-coefficients. The noise, noise figure, nonlinearity, and power consumption of the proposed directional coupler are analyzed and measured. A six-port circuit based on four quadrature hybrids is also proposed, designed and simulated for analyzing signals in frequency domain on chip.

Chapter V presents a high-speed sample-and-hold circuit based on spatial sampling with CMOS transmission lines (TLs) for analyzing signals in time domain on chip. This circuit contains three main parts: an on-chip meandered coplanar waveguide for signal transmission, a clock signal generator, and elementary samplers. Each elementary sampler has an N-type field effect transistor as the sampling switch, a charge

holding capacitor, and a charge amplifier. Signal propagation on periodically loaded CMOS TLs is analyzed and simulated.

Chapter VI presents a novel electron paramagnetic resonance spectroscopy with high sensitivity and multi-frequency operation for the development of micro-total-analysis-systems. A radio frequency sensor with tunable attenuators and phase shifters is designed to simultaneously address the sensitivity and multi-frequency operation challenges in the development of EPR techniques. The EPR signals of 60 μg 1,1-diphenyl-2picrylhydrazyl (DPPH) are measured from 1 GHz to 10 GHz.

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CHAPTER TWO

HIGH VOLTAGE CHARGE PUMP WITH TRIPLE WELL DIODES IN A 0.13 μm BULK CMOS PROCESS

This chapter presents charge pump circuits with modified triple well diodes as charge transfer switches for charging on-chip pulsed-power systems in a low-voltage bulk CMOS process. Guard-rings and isolation deep n-wells are used to improve the breakdown voltages and reduce leakage currents of the diodes. Model parameters of the triple well diode are extracted based on measured diode characteristics. These parameters are then used to analyze our charge pump. The proposed charge pump circuits are implemented in a commercial 0.13μm bulk CMOS process. The output voltage of the four-stage charge pump circuit can be up to 18.1V, which is much higher than the n-well/p-substrate breakdown voltage (~10V) of the given process.

2.1 Introduction

Charge pump circuits are often used to generate high voltages from a low voltage supply for a variety of applications, including driving nonvolatile memories [2.1], actuating MEMS devices [2.2] and charging on-chip pulsed-power systems [2.3]. In addition to high power transfer efficiencies, high output voltages are critical for charge pump circuits.

A Dickson charge pump [2.4] is the most common charge pump circuit topology, in which charge transfer switches are critical components. Traditionally, diode-connected MOSFETs are used as the switching devices. However, the increase of threshold voltages

due to body effects [2.5] degrades circuit performance. Several methods are proposed to reduce such effects at the cost of auxiliary circuits and more power consumption [2.5]-[2.8]. A floating-well technique [2.9] can also help reduce body effects, but it may generate substrate currents and affect other circuits on the same chip. Pn-junction diodes are also widely used in charge pump circuits. Yet, the output voltage level is limited by the breakdown of parasitic p-n junctions between the n+ region and the p-substrate [2.10]. The silicon-on-insulator (SOI) process [2.11] and polysilicon diodes [2.10] overcame such limitations. However, the intrinsic polysilicon layer [2.10] is not available in standard bulk CMOS processes, and the SOI CMOS process [2.11] is more expensive. Therefore, developing new circuit techniques in bulk CMOS processes for high voltage generation is of great interest.

In this chapter, a charge pump circuit utilizing triple well diodes with guard rings as charge transfer switches is presented. Compared with standard triple well diodes that were attempted in a charge pump [2.12] to obtain 6-10 V output voltages from a 3.3V power supply, guard rings improve the breakdown voltages. Additionally, the anode and cathode of the diodes are completely isolated from bulk substrate by a buried deep n-type layer. Thus, the proposed charge pump circuit is not limited by the breakdown of parasitic p-n junctions and their leakage currents. The analysis of the modified triple well diode is presented in Section 2.2. Section 2.3 gives the results of the circuits implemented in a commercial 0.13μm bulk CMOS process. Section 2.4 concludes the chapter.

2.2 Modified Triple Well Diodes

Fig. 2.1 shows the cross section of our triple well diode, which derives from the single photon avalanche diode (SPAD) [2.13]-[2.18]. A deep n-well layer is used for substrate isolation. The parasitic vertical p-n-p bipolar transistor, which consists of p-well, deep n-well and p-substrate, is off since the base and emitter are tied together. As a result, substrate leakage current that exists in conventional p-n junctions is suppressed.

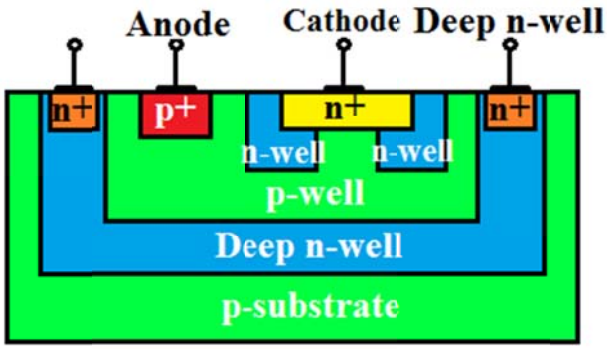

Figure 2.1 The cross section of n+/p-well CMOS triple well diode with a guard-ring.

The triple well diode (n+/p-well diode) consists of an n+/p-well junction surrounded by low-doping-level n-well, which acts as a guard ring to prevent edge breakdown [2.13]-[2.15] and improve diode breakdown voltages. Such improvement is important for high-voltage generations. However, appropriate separations between the n-well regions are needed to prevent full depletion of the area under n+ cathode [2.16]-[2.17]. P+ and n+ implantations in Fig. 2.1 are surrounded by Shallow Trench Isolation (STI) [2.18]. The deep n-well fully isolates n+ cathode and p+ anode from p-substrate. Therefore, the triple well diodes can be applied to the charge pump circuit without the limitation of the parasitic junctions.

The proposed triple well diodes with different n+ cathode area have been fabricated in IBM 0.13µm CMOS technology. Fig. 2.2 shows a photograph of a triple well diode with 10µm×10µm n+ cathode area. Fig. 2.3 shows the I-V characteristics of the diodes. The cut-in voltages are almost the same (~0.52 V) for diodes of different n+ cathode areas. The reverse breakdown voltages of these diodes are also similar (~10.1 V).

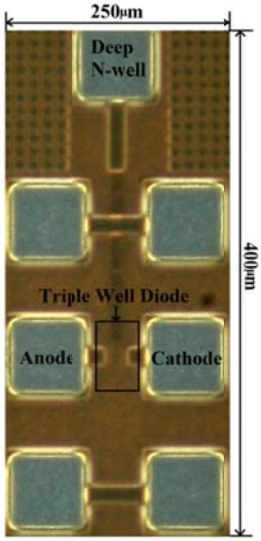

Figure 2.2 A photograph of the triple well diode.

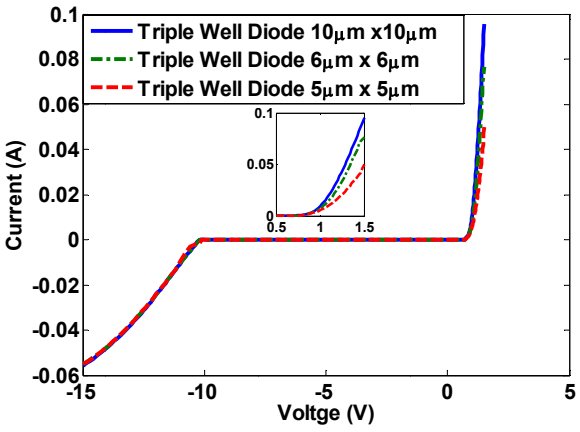

Figure 2.3 Measured I-V curves of the triple well diodes with different n+ cathode area.

The diode model parameters, shown in Table 2.1, are extracted for circuit simulations. The initial values of these parameters were calculated from measured diode characteristics, including recombination, high-level injection, and series resistance effect. Then these values are globally optimized by curve fitting with a modified least squares method, which greatly improves extraction accuracy and efficiency. Fig. 2.4 shows a comparison between simulated and measured diode characteristics. The simulation is based on the parameters listed in Table. 2.1. These curves are almost identical, which shows that the extracted model parameters can accurately describe the DC behavior of the triple well diodes. Fig. 2.5 shows the relationship among n+ cathode area, ideality factor N and series resistance R_S. It also shows that when the n+ cathode area increases, the recombination current and resistance in the space charge region between the n guard ring and the p-well under the n+ cathode have the less effect on the characteristics of the triple well diodes.

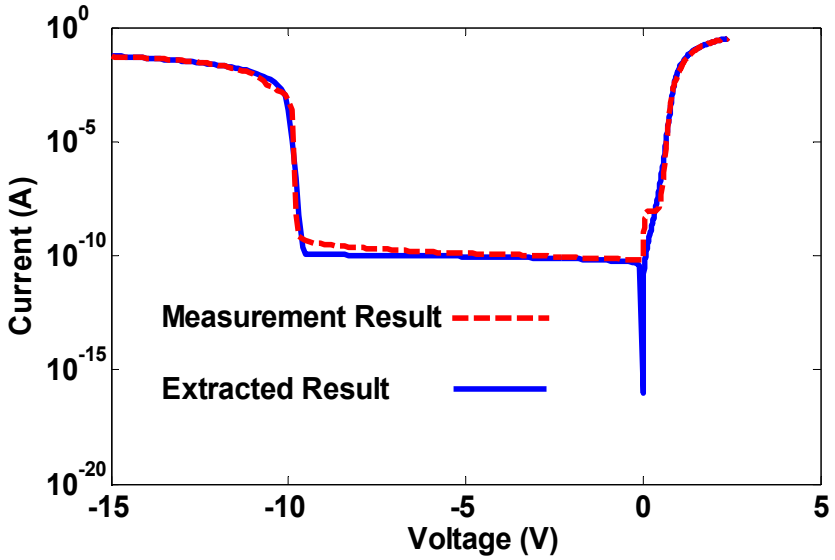

Figure 2.4 Measured and simulated triple well diode characteristics.

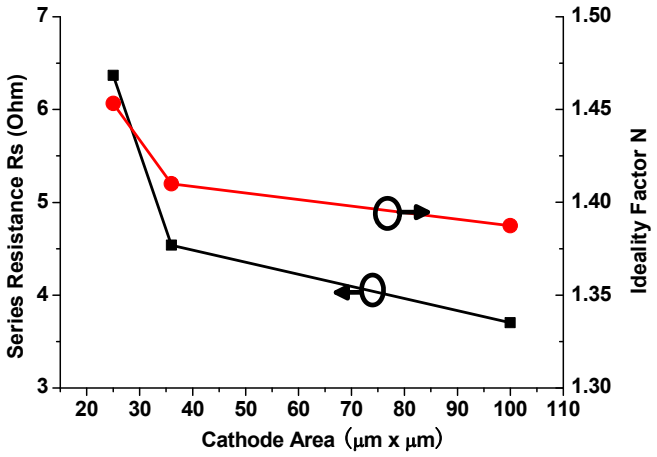

Figure 2.5 Relationship among cathode area, ideality factor and series resistance.

TABLE 2.1
MODIFIED TRIPLE WELL DIODE MODEL PARAMETERS

Model Parameter	Value
I_S	1.39 pA
N	1.3874
R_S	3.7033 Ω
IKF	4.76 mA
ISR	46.8 pA
NR	2.4944
BV	10.06 V
IBV	5.81 mA

2.3 Charge Pump Circuit Implementation

2.3.1 Circuit Design

Fig. 2.6 shows an eight-stage charge pump circuit with 9 triple well diodes. *CLK* and *CLKB* are two out-of-phase clocks with an amplitude V_{CLK} equivalent to V_{DD}. Because the breakdown voltage of the capacitors in our CMOS process is ~7V, stacked capacitors are used for higher voltages.

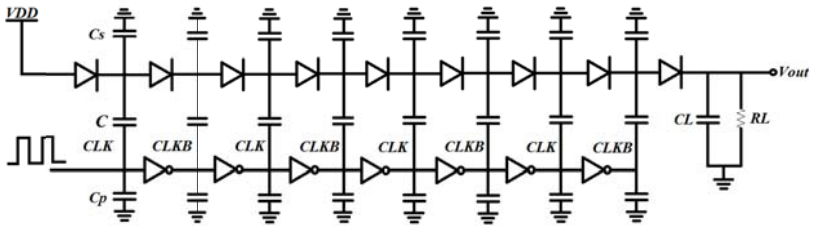

Figure 2.6 Eight-stage charge pump circuit realized with 9 triple well diodes.

The output voltage of the charge pump circuit can be expressed as [2.19]

$$V_{out} = V_{DD} + N\left[\left(\frac{C}{C+C_s}\right)V_{CLK} - V_D - \frac{I_{out}}{(C+C_s)f}\right] - V_D \,. \tag{2.1}$$

where V_{CLK} is the voltage amplitude of the clock signal, C is pumping capacitance, C_S is parasitic capacitance at each switching node, I_{out} is the output current, V_D is the cut-in diode voltage, N is the number of stages in the charge pump circuit, and f is the clock frequency.

The switching node parasitic capacitance C_S and the clocked-plate parasitic capacitance C_P increase the energy loss in a charge pump circuit. To maximize the output voltage, clocking the bottom plate of the stage capacitors is chosen as the connection method in our charge pump. In the bottom-plate connection, C_S is the combination of the top-plate parasitic capacitance and the triple well diode parasitic capacitance. C_P consists of the bottom-plate parasitic capacitance, which is generally more than an order of magnitude larger than that of the top plate [2.20]. And the parasitic capacitance in the triple well diode is lower than that in the p+/n-well diode [2.21]. From (2.1), only the switch-node parasitic capacitance C_S affects the output voltage. Since C_S is small, clocking the bottom plate results in more output voltage. Assuming that I_{out} is small enough and V_{CLK} is the same as V_{DD}, we have

$$V_{out} = (N+1) \times (V_{DD} - V_D) . \tag{2.2}$$

And the power efficiency of the charge pump is defined as [2.20]

$$\eta = \frac{V_{\text{out}} \times I_{out}}{V_{DD} \times I_{DD}} \tag{2.3}$$

The total current consumption of an N-stage charge pump can be expressed as [2.11]

$$I_{DD} = (N+1) \times I_{OUT} + N \times I_P + (2N+1) \times I_S \tag{2.4}$$

where I_p is the current charging and discharging the clocked-plate parasitic capacitance, and I_S is the current charging and discharging the switch-node parasitic capacitance. Also, I_p and I_S for our proposed charge pump can be respectively given by [2.11]

$$I_P = C_p \times V_{CLK} \times f \tag{2.5}$$

$$I_S = C_S \times \Delta V_n \times f \tag{2.6}$$

where ΔV_n is the voltage swing across the pumping capacitor, C_P is the bottom-plate parasitic capacitance and C_S is the combination of the top-plate and diode parasitic capacitance. As the bottom plate is driven by the clock in our charge pump, C_S is small enough to neglect I_S in (4) and the bottom-plate parasitic capacitance can be expressed as

$$C_P = \frac{I_{DD} - (N+1) \times I_{OUT}}{N \times V_{CLK} \times f} \tag{2.7}$$

2.3.2 Measurement Results

Four-stage, eight-stage and twelve-stage charge pump circuits with 6-pF metal-insulator-metal (MIM) pumping capacitors, a 6-pF MIM load capacitor and triple well

diodes with 10μm×10μm n+ cathode area have been fabricated in an IBM 0.13μm CMOS process. The photograph of the twelve-stage charge pump circuit is shown in Fig. 2.7.

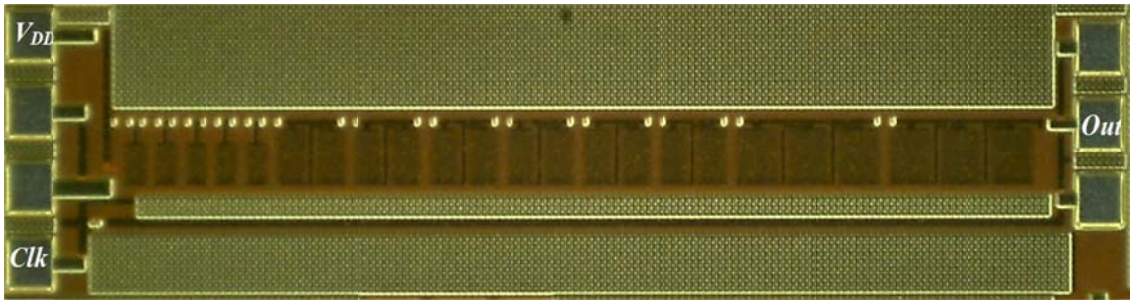

Figure 2.7 A photograph of the twelve-stage charge pump with triple well diodes. The fabricated chip is 570 μm ×2485 μm.

Fig. 2.8 shows the measured output voltage of the four-stage, eight-stage and twelve-stage charge pump circuits with different power-supply voltages to drive the capacitive output load. The output voltage of the twelve-stage charge pump circuit is as high as 12.3 V from 1.6 V power supply voltage corresponding to a voltage gain of ~7.7, which is much higher than the n-well/p-substrate junction breakdown voltage (~10V), which is also the maximum junction breakdown in the given 0.13μm bulk CMOS process. At 12.3 V, the voltage across each triple well diode doesn't exceed the reverse breakdown voltages of the triple well diodes. Fig. 2.9 shows the measured output voltages of the four-stage and eight-stage circuits under different clock frequencies, where the power supply voltage is 1.6 V. When the clock frequency is increased, the output voltages of the charge pump circuit are also increased due to less charge leaking to parasitic capacitors.

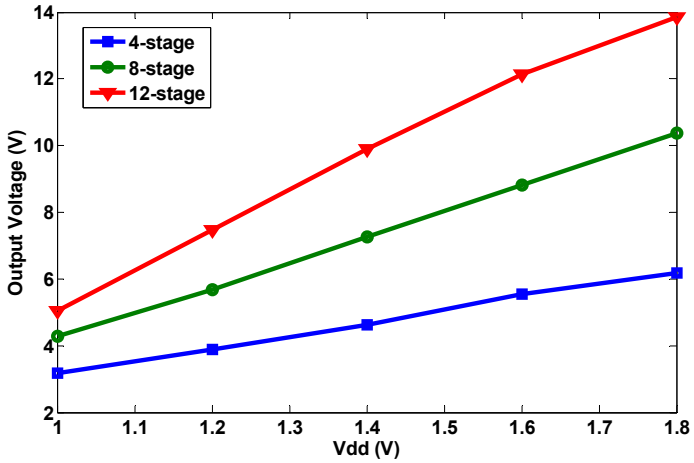

Figure 2.8 Measured output voltages of the charge pump circuits with triple well diodes to drive capacitive loads under different V_{DD}. The clock frequency is 5MHz.

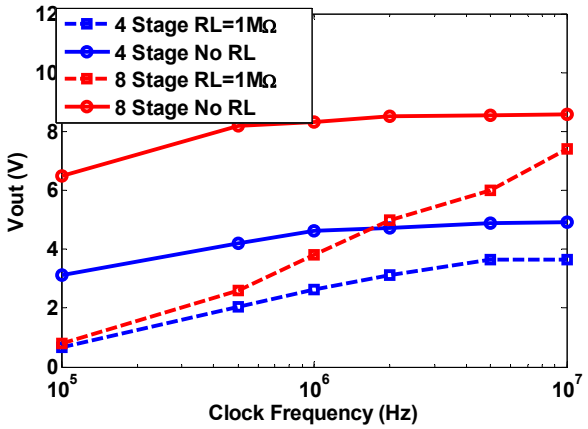

Figure 2.9 Measured output voltages of the four, and eight-stage charge pump circuits for different clock frequencies. The power supply is 1.6V.

Fig. 2.10 shows the measured output voltage of the four-stage circuit with 1MΩ output resistors and without output resistor at a 5MHz clock frequency. In Fig. 2.10, the output voltage of the charge pump circuit realized with the triple well diodes can be as high as ~18.1 V. Fig. 2.11 shows the measured power efficiency of the proposed four-

stage and eight-stage charge pump. The measured peak power efficiencies of these two charge pumps are about 42.59% at I_{OUT} of 5 µA and about 41.92% at I_{OUT} of 7 µA, respectively. From (2.3), the clocked-plate parasitic capacitance C_p has the main effect on the power efficiency. In a bottom-plate connection, a large bottom parasitic capacitance of stage capacitors results in lower power efficiency. Clocking the top plate of the stage capacitors will reduce C_p, which can result in higher power efficiency. Also, this top-plate connection will cause the decrease in the voltage gain of each stage of the charge pump, which results in a lower output voltage.

Currents I_{DD} and I_{OUT}, I_{DD}=81.75 µA and I_{OUT}=7 µA, for the eight-stage charge pump shown in Fig. 2.7 are measured with a Keithley 2612 system source meter, where the clock frequency is 5 MHz and the power supply is 1.6 V. From (2.7), C_P can be calculated as 0.85 pF, which is used for a proposed charge pump simulation.

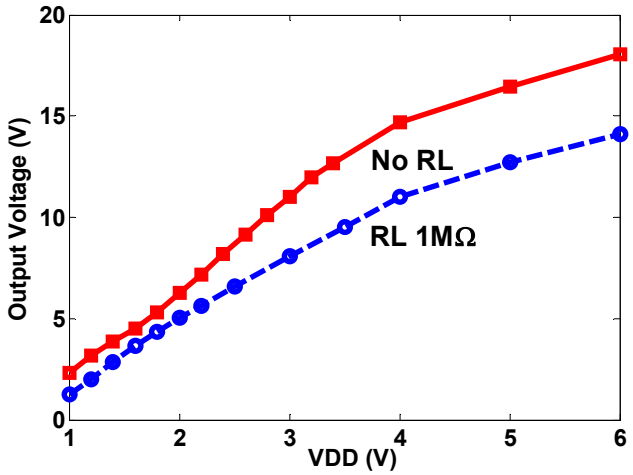

Figure 2.10 Measured output voltages of the four-stage charge pump circuits with the 1MΩ resistor and without the resistor under different V_{DD}. The clock amplitude is always equal to V_{DD}.

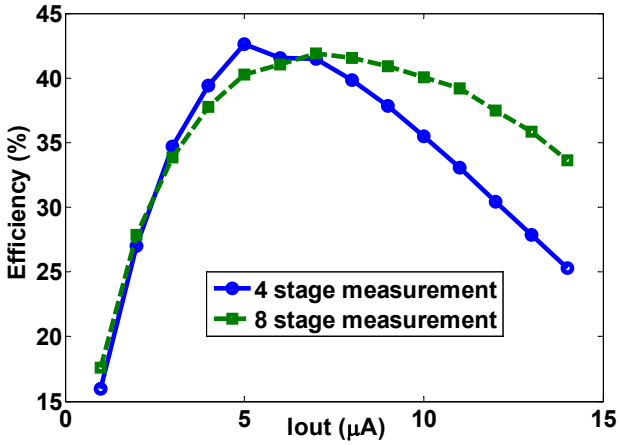

Figure 2.11 Measured power efficiency of the proposed four-stage and eight-stage charge pump circuits.

2.3.3 Discussion

The model parameters of the triple-well diode in Table 2.1 and the parasitic capacitance, C_p=0.85 pF, are used to obtain the simulation results in Fig. 2.12. It shows that results from simulations and measurements agree with each other reasonably well. This further validates our model parameter extraction (Table 2.1) and circuit design processes. Compared with ideal charge pumps, the measured output voltage increase is ~16% lower while the simulated voltage increase is only ~6% lower when the supply voltage increases by ΔV. This discrepancy is likely due to the leakage currents from parasitic capacitors of triple well diodes and the voltage loss caused by the measurement system including contact pads, probes, connectors and cables.

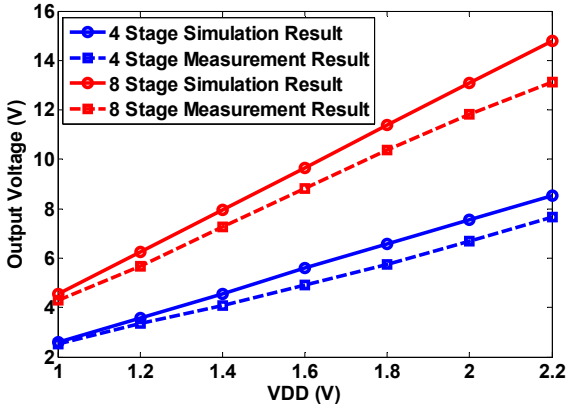

Figure 2.12 Measured and simulated output voltages of the proposed four-stage and eight-stage charge pump circuits to drive capacitive loads.

Fig. 2.13 shows a comparison of our charge pump circuit with circuits that use diode-connected MOSFETs and Schotty diodes as switches in the same technology. The simulations were conducted with 1.6V V_{DD} for a different number of stages. It shows that for 5-stages or less, the circuit with Schottky diodes has higher output voltages due to lower cut-in voltages (~0.3V). When the number of stage increases, our circuit generates much higher voltages. For diode-connected MOSFETs, the increase of threshold voltage (V_{th}) due to body effects affects the output voltage and power efficiency. For Schotty diode circuits, the output voltage is limited by the breakdown of parasitic p-n junctions and leakage current to the substrate. Thus, the voltage gain per stage in the charge pump circuits with diode-connected MOSFETs or Schotty diodes decreases as the number of stages increases as discussed in the introduction. The output voltage of our proposed charge pump circuit is not limited by the breakdown voltages of the parasitic p-n junctions. Although the power efficiency of our charge pump is adversely affected by the

bottom-plate parasitic capacitance and high cut-in voltage of the diodes. As shown in Fig. 2.10, the output voltage of our circuit can drive a purely capacitive load up to ~18.1V.

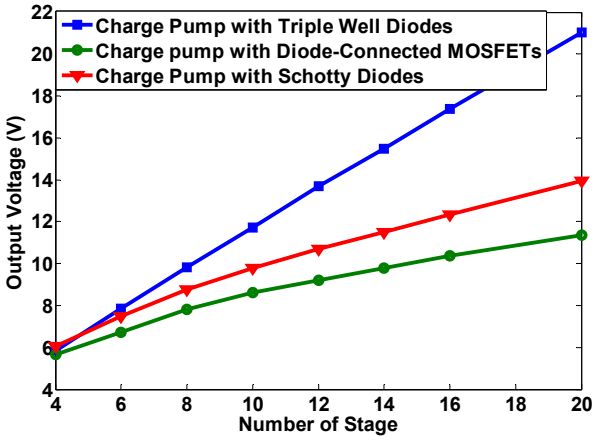

Figure 2.13 A comparison of the simulated output voltages of the charge pump circuits with triple well diodes, diode-connected MOSFETs and Schotty diodes as the number of stage increases. The clock frequency is 5 MHz.

2.4 Conclusions

Triple well diodes with guard rings and deep n-well isolation are designed and modeled for high-voltage operation in standard bulk CMOS processes. Four-stage, eight-stage and twelve-stage charge pump circuits with triple well diodes as charge transfer switches have been implemented in a commercial 0.13μm bulk CMOS process. Compared with circuits that use diode connected FETs and Schottky diodes as switches, our circuits generate much higher output voltages. When a 6-pF capacitor is used as the load, the measured output voltage can be up to 18.1V, using a 5MHz two-phase nonoverlapping clock. The achieved voltage is much higher than the p-n junction breakdown voltages of the given processes.

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CHAPTER THREE

CMOS HIGH VOLTAGE SHORT PULSE GENERATORS

We present three types of on-chip pulse generation circuits. The first is based on CMOS pulse-forming-lines (PFLs). It includes a four-stage charge pump, a four-stacked-MOSFET switch and a 5 mm long PFL. The circuit is implemented in a 0.13 μm CMOS process. Pulses of ~1.8 V amplitude with ~135 ps duration on a 50 Ω load are obtained. The obtained voltage is higher than 1.6 V, the rated operating voltage of the process. The second is a high-voltage Marx generator which also uses stacked MOSFETs as high voltage switches. The output voltage is 11.68 V, which is higher than the highest breakdown voltage (~10 V) of the CMOS process. The third is a CMOS Blumlein generator including a two-stacked-MOSFET high voltage switch, a Blumlein PFL network, and an on-chip Klophenstein taper. Gaussian-like pulses of 725 mV peak-to-peak amplitude, ~126 ps duration and 3.18 GHz bandwidth are measured on a 50 Ω load. After de-embedding the connection system and Klophenstein taper, the pulses of 1.88 V and 114 ps duration are obtained. These results significantly extend high-voltage short pulse generation capabilities of CMOS technologies.

3.1 Introduction

Generating high voltage short pulses on chip is important for functionality integration, such as micro/nano electromechanical systems (MEMS/NEMS) actuation [3.1], electrophoresis [3.2], electroporation [3.3] and cellular investigation [3.4]-[3.5]. Short electrical pulse is also important for various other applications, such as clocking

high-speed analog-to-digital converters (ADC) [3.6], synthesizing ultra-wideband (UWB) signals for UWB communications [3.7], and developing inexpensive terahertz (THz) pulse technologies. Nevertheless, techniques for high voltage pulse generations on chip are still under exploration.

Digital circuits generate pulses with V_{dd} as the maximum available output voltages and fan-out-four (FO4) propagation delay as the shortest pulses on a load of 4-inverters, which are usually much lighter than a 50 Ω load. Traditional analog circuits could generate higher voltage pulses, but limited by V_{dd} and breakdown voltages of the given technology. High-voltage CMOS processes may not be able to exploit the high-speed capabilities of standard digital CMOS processes without incurring higher costs. Photoconductive switching [3.8] and transmission line discontinuities [3.9] generate short pulses. However, it is difficult to implement these circuits in a standard CMOS process. Nonlinear transmission lines (NLTL) [3.10]-[3.11], which consist of long transmission lines and dozens of varactors, can sharpen pulse edges. But these circuits occupy large chip areas and their high-voltage generation capabilities need to be demonstrated. The CMOS UWB pulse generators, which are based on a pulsed oscillator and a pulse shaping filter [3.12] or a distributed waveform generator [3.13], generate pulses with high bandwidth (4.5 GHz [3.12] and 6 GHz [3.13]). These circuits are also not applied for high voltage generations. In [3.14]-[3.15], we proposed a pulse-forming-line (PFL) based CMOS generator, which significantly extends the high voltage short pulse generation capabilities of CMOS technologies. Nevertheless, the obtained pulses are modest, with 180 mV voltages and ~160 ps full-width-at-half-magnitude (FWHM) on a

50 Ω load. A 0.13 μm CMOS technology was used for circuit implementation.

In this effort, we further expand our previous work to generate high output voltages. We also present a high-voltage CMOS Marx generator circuit and an on-chip Blumlein generator. Such circuits have not been reported so far. This chapter is organized as follows. Section 3.2 presents the proposed CMOS PFL-based pulse generation circuit, including a charge pump circuit, a high voltage switch and a PFL network. Section 3.3 proposes a study of reducing the timing jitter induced by power-supply and ground noise in PFL-based pulse generation circuits. Section 3.4 presents an on-chip Marx generator. Section 3.5 presents a CMOS Blumlein generator with an on-chip Klophenstein taper. Section 3.6 concludes this chapter.

3.2 CMOS PFL-based High Voltage Pulse Generation Circuit

The basic idea of a CMOS high voltage pulse generation circuit is to achieve high voltage (e.g. higher than 10 V, the breakdown voltages of N-well/Substrate of our given CMOS process) by exploiting the much higher voltage handling capabilities of the dielectric insulation layers between interconnect metals [3.16]. Figure 3.1 shows the on chip PFL-based high voltage pulse generation circuit, including a four-stage charge pump, a four-stacked-MOSFET switch and a 5 mm PFL. The four-stage charge pump is used as a high voltage source to generate the DC voltages higher than the power-supply voltage (V_{dd}). The four stacked MOSFET switch can operate at $4\times V_{dd}$ (6.4 V) to overcome the limitation of breakdown voltages of MOSFETs, where V_{dd} (1.6 V) is the rated voltage of our given process [3.17]-[3.20]. When the switch is turned on by the

trigger signal, which is sharpened by a trigger pulse generator, the PFL discharges through load R_L (50 Ω). The output pulse is then generated with an ideal amplitude of 3.2 V and 77 ps FWHM.

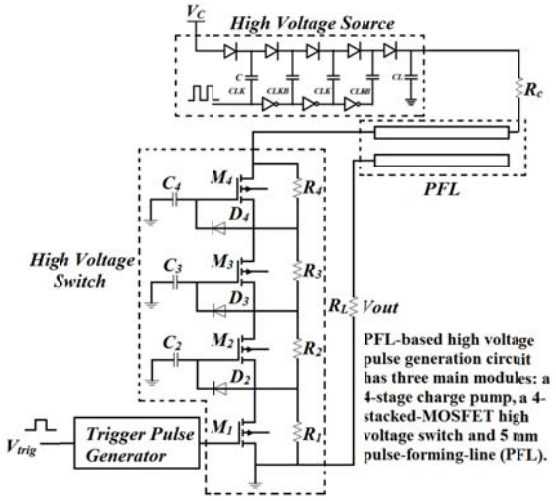


Figure 3.1 An on-chip PFL-based high-voltage pulse generation circuit.

3.2.1 Charge Pump Design and Analysis

The charge pump module in Fig. 3.1 is connected to a pulse forming line network. A Dickson charge pump [3.21] topology is used. Zero V_{th} MOSFETs are used as charge transfer switches due to their lower cut-in voltages (~0.1 V). The output capacitor, C_L, at the end of the charge pump in Fig. 3.1, acts as a local power source and filter that reduces noise generated from the power supply.

The output voltage of the charge pump is [3.22]-[3.23]

$$V_{out} = V_{dd} + N\left[\left(\frac{C}{C + C_s}\right)V_{CLK} - V_D - \frac{I_{out}}{(C + C_s)f}\right] - V_D, \tag{3.1}$$

where V_{CLK} is the voltage amplitude of the clock signal, C is the pumping capacitance, C_S is the parasitic capacitance at each switching node, I_{out} is the output current, V_D is the cut-

in diode voltage, N is the number of stages in the charge pump circuit, and f is the clock frequency.

The reliable operation of the stacked-MOSFET switch determines the maximum charge pump output voltage. For the four stacked MOSFETs in Fig. 3.1, the pulse forming line network can be charged to $4 \times V_{dd}$ (~6.4 V). Thus a four-stage charge pump is chosen to obtain ~6.4 V output voltages from a 1.6 V power supply even though the ideal output voltage from this charge pump is 8 V. The voltage loss is due to charge loss through the current path formed by the voltage division resistors of the switch and the transmission lines. The output current (simulated) of the charge pump when imbedded in the circuit in Fig. 3.1 is shown in Fig. 3.2. It shows that the output current depends on the input power supply to the charge pump. Therefore, it is necessary to take into account this load effect when generating a given voltage. Fig. 3.3 shows the comparison of output voltage between analysis and simulation with different output currents. It is seen that the analysis results agree reasonably well with simulation results. Thus, Eq. (3.1) accurately describes the output voltage behavior of the charge pump circuit.

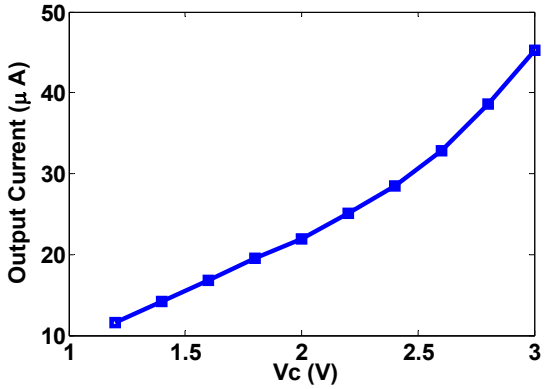


Figure 3.2 Simulated output current from the charge pump to ground with different V_{dd} voltages.

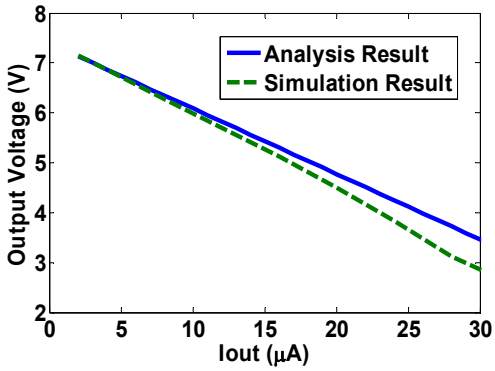


Figure 3.3 Comparison of output voltage between analysis and simulation with different output currents. The power supply voltage is 1.6 V and the clock frequency is 5 MHz.

Fig. 3.4 shows the required V_{dd} for a targeted V_{out} and a given load (i.e. I_{out}), obtained from Eq. (1), of the charge pump circuit. For 6.4 V output voltage, V_{dd} is less than 2.5 V, and the maximum output current is less than 30 μA. In our experimental test in section 3.4, a 2.4 V V_{dd} was chosen. Figure 3.4 shows that I_{out} is less than 30 μA and the output voltage is 6.6V, which is 0.2 V above 6.4 V. It should be pointed out that the 2.4V V_{dd} is above the 1.2 V-1.6 V operating voltage of our given 0.13 μm CMOS process. Nevertheless, the MOSFETs in the stacked switch operate around 1.6 V. Furthermore, the breakdown voltage between gate/drain/source and the body of the MOSFETs in the technology is ~4.0 V. Thus, a 2.4 V V_{dd} does not cause breakdown issues in the charge pump circuit module.

Higher output voltages can be achieved without using V_{dd} larger than 1.6 V. One approach is to add more stages in the charge pump circuit module. However, due to body effect for diode-connected MOSFETs [3.24] or breakdown of parasitic p-n junctions for diodes [3.25], output voltages of charge pump circuits are limited and cannot be a linear

function of the number of stages. Thus, modified triple well diodes are used as charge transfer switches to help solve this problem. In chapter two, we used modified triple well diodes in a 12 stage charge pump circuit and obtained as high as ~12.3 V output voltages to drive the 6 pF capacitive load from a 1.6 V_{dd} supply without breakdown concerns, which is much higher than the n-well/p-substrate junction breakdown voltage (~10 V). From Fig. 3.2, when V_{dd} is 1.6 V, the 8 stage charge pump with modified triple well diodes can generate ~6.4 V under ~12 μA output current to ground.

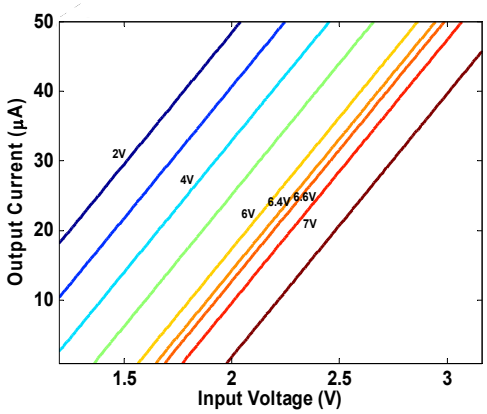


Figure 3.4 Determination of input voltage to the charge pump for the given requirements.

3.2.2 High Voltage Switch Design and Analysis

Fig. 3.5 shows the high voltage switch with N stacked-MOSFETs, which can switch $N \times V_{dd}$. Before the bottom M_1 is turned on, the resistors (R_1~R_N) equally divide $N \times V_{dd}$ into V_{dd} across each MOSFET. When M_1 is turned on, its drain is discharged. Thus, its drain voltage is decreased. Then M_2 is on, and similarly all the other MOSFETs (M_2~M_N) are turned on. Through setting the turn-on capacitance, the gate-source voltage for each transistor in the stack can be expressed as [3.17]

$$V_{gs(i)} = \frac{C_{(i)}}{C_{(i)} + C_{p(i)}} \times \left((i-1) \times \left(\frac{V_{ddh}}{N} \right) - V_{diode} \right) + \frac{C_{(i)}}{C_{(i)} + C_{p(i)}} \times (-V_{diode}), i = 2 \sim N, \tag{3.2}$$

where N is the number of transistors in the stack, i is the specific device being considered, V_{ddh} is the desired high voltage ($N \times V_{dd}$), V_{diode} is the voltage across the diode (D_2~D_N), C is the turn-on capacitance, and C_p is the total parasitic capacitance across the gate-source of each MOSFET in series.

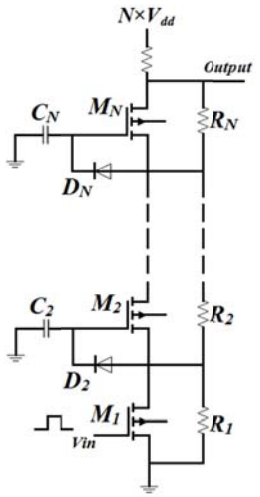


Figure 3.5 Schematic of N stacked-MOSFET high-voltage switch

Assume that each MOSFET in the switch has equal size and turn-on gate-source voltage, the turn-on capacitances can be defined as [3.17]

$$C_{\mathrm{i}} = C_{p(i)} \left(\frac{V_{gs} + V_{diode}}{(i-1) \times \left(\frac{V_{dd}}{N} \right) - \left(V_{gs} + V_{diode} \right)} \right), i = 2 \sim N. \tag{3.3}$$

The operating process of the high voltage switch can be divided into two regions, Region I and Region II. During Region I, the MOSFETs (M_1~M_{N-1}) are turned on and discharge capacitances at each drain node without affecting the output node in Fig. 3.5. During Region II, M_N is turned on, pulling the output node to ground.

Region I: Transistor M_N is off and transistors M_1 to M_{N-1} are all non-saturated. For Region I, the high voltage switch can be modeled as the equivalent circuit shown in Fig. 3.6. Resistors (R_{M1}~R_{MN-1}) represent the on-resistances from MOSFETs (M_1~M_{N-1}). The capacitors (C_{M1}~C_{MN-1}), which represent the capacitance at the drain nodes of MOSFETs in series, can be expressed as

$$C_{M(i)} = C_{db(i)} + C_{gd(i)} \times (1 - A_{v1}) + C_{ds(i)} \times (1 - A_{v2}), i = 1, 2, \cdots, N-1, \tag{3.4}$$

where i is the i_{th} drain capacitance being considered, A_{v1} and A_{v2} are used to approximate the Miller effect resulting from C_{gd} and C_{ds}.

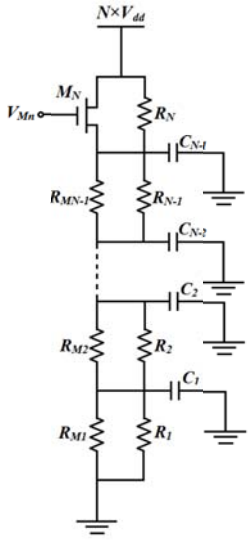


Figure 3.6 An equivalent circuit for the high voltage switch in region I.

In region I, the voltage across M_N increases from V_{dd} to ~$N \times V_{dd}$, which is a monotonic transient response and can be expressed as

$$V_{dsN}(t) = V_N - V_{N-1}, \tag{3.5}$$

where V_N and V_{N-1} are the drain voltages of M_N and M_{N-1}, respectively. Then T_1 in region I can be approximately expressed as [3.26]-[3.27]

$$T_1 = \int_0^{\infty} t V'_{dsN}(t)dt. \tag{3.6}$$

Figure 3.7 shows the transient response $V_{ds4}(t)$ for the switch with four stacked MOSFETs. Its derivative $dV_{ds4}(t)/dt$ is shown in Fig. 3.8. The definition of T_1 is illustrated in Fig. 3.8 [3.27].

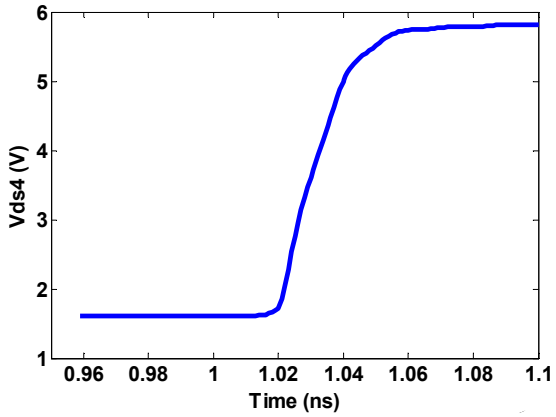


Figure 3.7 Transient response $V_{ds4}(t)$ for the switch with four stacked MOSFETs.

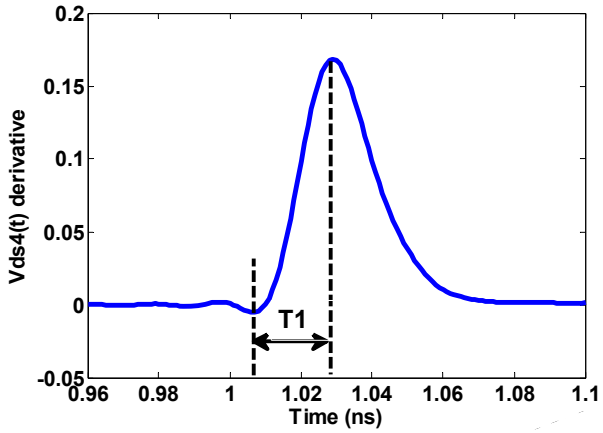


Figure 3.8 Derivative of transient response $V_{ds4}(t)$.

The transfer function for the equivalent circuit shown in Fig. 3.6 can be defined as

$$T(s) = \frac{1 + a_1 s + a_2 s^2 + \cdots + a_n s^n}{1 + b_1 s + b_2 s^2 + \cdots + b_m s^m}. \tag{3.7}$$

By dividing the numerator with the denominator of the transfer function, Eq. (3.7) becomes

$$T(s) = 1 - (b_1 - a_1)s + (b_1^2 - a_1 b_1 + a_2 - b_2)s^2 + \cdots. \tag{3.8}$$

If a unit impulse is applied to the circuit in Fig. 3.6, the transfer function has the relationship with $dV_{ds4}(t)/dt$ through Laplace transformation as

$$T(s) = \int_0^\infty V'_{dsN}(t) \times e^{-st} dt. \tag{3.9}$$

Expanding e^{-st} in a power series in *st*, Eq. (3.9) becomes

$$T(s) = 1 - s\int_0^\infty t \times V'_{dsN}(t)dt + \frac{s^2}{2!}\int_0^\infty t^2 \times V'_{dsN}(t)dt - \cdots. \tag{3.10}$$

Comparing Eq. (3.8) and Eq. (3.10), we have

$$T_1 = b_1 - a_1 = \int_0^\infty t V'_{dsN}(t)dt, \tag{3.11}$$

where b_1 and a_1 are the sum of the pole and zero at each node in the high voltage switch, respectively. Assuming that a_1 is zero, T_1 can be obtained as

$$\begin{aligned} T_1 = {} & \frac{(R_{M1}//R_1)\times(R_{M2}//R_2 + \ldots + R_N)}{(R_{M1}//R_1 + R_{M2}//R_2 + \ldots + R_N)} \times C_{M1} + \frac{(R_{M1}//R_1 + R_{M2}//R_2)\times(R_{M3}//R_3 + \ldots + R_N)}{(R_{M1}//R_1 + R_{M2}//R_2 + \ldots + R_N)} \times C_{M2} \\ & + \ldots + \frac{(R_{M1}//R_1 + R_{M2}//R_2 + \ldots + R_{MN-1}//R_{N-1})\times(R_N)}{(R_{M1}//R_1 + R_{M2}//R_2 + \ldots + R_N)} \times C_{MN-1}. \end{aligned} \tag{3.12}$$

When the MOSFETs in series are the same size, the on-resistances and drain capacitances are all equal.

$$R_{M1} = R_{M2} = \ldots = R_{MN-1} = R_{on} \tag{3.13}$$

$$C_{M1} = C_{M2} = \ldots = C_{MN-1} = C \tag{3.14}$$

Assuming that the dividing resistances R_i are much larger than the on-resistances R_{Mi}, based on Eq. (3.13) and Eq. (3.14), Eq. (3.12) can be simplified as [3.26]

$$T_1 = \frac{R_{on} \times C \times N \times (N-1)}{R_N + (N-1) \times R_{on}} \left[\frac{R_N}{2} + R_{on} \times \left(\frac{N}{6} - \frac{1}{3} \right) \right]. \tag{3.15}$$

Region II: After Region I, M_N is turned on and the series transistors start discharging the load capacitance at the drain node of the topmost transistor. When the load capacitance is large compared to the drain/source capacitance, a Sakurai model is used to model time T_2 in Region II [3.28]. In a Sakurai model, the delay degradation factor F_D, defined as the ratio of the delay of series-connected MOSFETs to the delay of a single MOSFET, can be calculated as [3.28]

$$F_D = \frac{I_{dsat}}{I_{dN}} = 1 + \frac{1}{2} \times \alpha \times \frac{V_{dsat}}{V_{dd} - V_{th}} \times (1 + \gamma_1) \times (N-1), \tag{3.16}$$

where γ_1 is the body-bias factor and I_{dN} is the current for N series-connected MOSFETs.

During time T_2, the current discharging C_L can be calculated from Eq. (3.16), therefore,

$$T_2 = \frac{C_L \times V_{dd}}{I_{dN}} = \frac{C_L \times V_{dd} \times F_D}{I_{dsat}}. \tag{3.17}$$

Now the α-power law is used to model the topmost MOSFET M_N. The I-V equations are [3.28]

$$I_{ds} = I_{dsat} \times \left(2 - \frac{V_{ds}}{V_{dsat}} \right) \times \frac{V_{ds}}{V_{dsat}} \qquad \text{triode region} \tag{3.18a}$$

$$I_{ds} = I_{dsat} \times \left(\frac{V_{gs} - V_{th}}{V_{dd} - V_{th}} \right)^{\alpha}, \qquad \text{saturation region} \tag{3.18b}$$

where I_{dsat} is the drain current when $V_{gs}=V_{ds}=V_{dd}$, V_{dsat} is the drain saturation voltage

when $V_{gs}=V_{dd}$, and α is the velocity saturation index and is closely related to the velocity saturation of carriers.

The differential equation that describes the discharge of the drain capacitance of the topmost transistor in the stacked switch is given by

$$C_{MN}\frac{dV_{out}}{dt}=C_{gdN}\frac{dV_g}{dt}-I_{dsN}, \tag{3.19}$$

where C_{MN} is the capacitance at the drain node of M_N and V_{out} is the drain voltage at the output node in Fig. 3.6. To solve Eq. (3.19), V_g and V_{gs} of M_N can be modeled as

$$V_g(t)=k_1t+b_1, T_1<t<T_1+T_2 \tag{3.20}$$

$$V_{gs}(t)=k_2t+b_2, T_1<t<T_1+T_2, \tag{3.21}$$

where k_1, k_2 and b_1, b_2 are constants. Therefore, the operation of the high voltage switch during T_2 can be analyzed as follows:

(a) When $V_{th}<V_{gs}<V_{ds}+V_{th}$, and the topmost MOSFET operates in the saturation region, Eq. (3.19) becomes

$$C_{MN}\frac{dV_d}{dt}=C_{gdN}\frac{dV_g}{dt}-I_{dsat}\left(\frac{V_{gs}-V_{th}}{V_{dd}-V_{th}}\right)^{\alpha}. \tag{3.22}$$

Then, Eq. (3.22) can be solved as

$$V_{d1}=-\frac{I_{dsat}}{C_{MN}(\alpha+1)k_2(V_{dd}-V_{th})^{\alpha}}\times\left(k_2t+b_2-V_{th}\right)^{\alpha+1}+\frac{C_{gdN}k_1}{C_{MN}}t+c. \tag{3.23}$$

(b) When $V_{gs}>V_{ds}+V_{th}$, and the topmost MOSFET operates in the triode region and its drain current rises until I_{dsmax}. I_{dsmax} can be expressed as

$$I_{ds\max}=\frac{V_{DD}}{R_L+Z_o+N\times R_{on}}, \tag{3.24}$$

where R_{on}, the on-resistance of the MOSFET in switch, is

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L}\left(V_{gs} - V_{th}\right)}. \tag{3.25}$$

Since the drain current keeps the maximum value I_{dsmax} in this region, the V_d reaches the minimum value

$$V_d = N \times R_{on} \times I_{ds\max}. \tag{3.26}$$

With Eq. (3.15), (3.17), (3.23) and (3.26), the modeled output voltage for the high voltage switch with four stacked MOSFETs is shown in Fig. 3.9. The simulation result agrees reasonably well with the modeling result. The discrepancy is mainly caused by C_M calculation errors. However, the errors do not significantly affect the output pulse modeling. Table 3.1 compares the modeled and simulated performance of the high voltage switch for different MOSFET sizes. The modeled results are nearly the same with the simulated ones, which confirms the validity of the switch modeling method. From Fig. 3.10, it shows that the fall time of the switch can reach minimum values between 200 μm and 300 μm MOSFET width, while the voltage loss on the switch is less than 0.6 V.

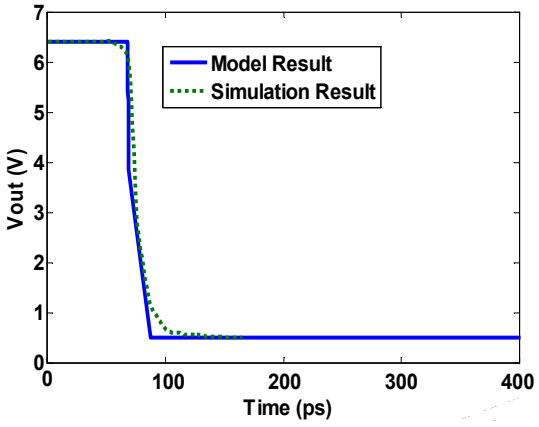


Figure 3.9 Simulated and modeled output voltage of the high voltage switch.

TABLE 3.1 Modeled and simulated parameters for high voltage switch

MOS Width (μm)	Result	Fall Time (ps)	Voltage Loss on Switch (V)
100	Modeled	51.0	1.21
	Simulated	56.9	1.31
200	Modeled	32.8	0.63
	Simulated	34.5	0.642
300	Modeled	32.1	0.399
	Simulated	31.0	0.434
400	Modeled	34.1	0.319
	Simulated	32.1	0.331
500	Modeled	37.2	0.268
	Simulated	34.3	0.28

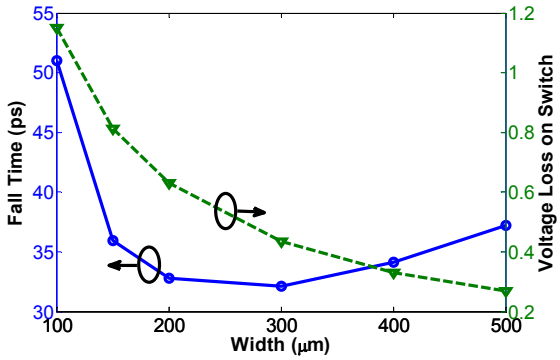


Figure 3.10 Modeled switch performance with different MOSFET sizes.

3.2.3 Output Pulse Analysis

The current that passes through the PFL network and the load impedance R_L can be expressed as [3.29]

$$i_l(t) = \frac{V_{DD}}{Z_o + R_L + R_{sw}} \times \{1 - U(t-2\delta) - \frac{Z_o - (R_L + R_{sw})}{Z_o + (R_L + R_{sw})} \times [U(t-2\delta) - U(t-4\delta)] + \left[\frac{Z_o - (R_L + R_{sw})}{Z_o + (R_L + R_{sw})}\right]^2 \times [U(t-4\delta) - U(t-6\delta)] \cdots\}, \quad (3.27)$$

where δ is the propagation time of the signal on transmission line, R_{sw} is the resistance from the high voltage switch, and U is the Heaviside step function. These are given as

$$R_{sw} = (N-1) \times R_{on} + R_{eqMN}(t) \tag{3.28}$$

$$U(\Delta t) = \begin{cases} 1, & \Delta t > 0 \\ 0, & \Delta t < 0 \end{cases} \tag{3.29}$$
$$\Delta t = (t - n\delta), \quad n = 2, 4, 6 \cdots$$

where $R_{eqMN}(t)=V_{dsMN}(t)/I_{dsMN}(t)$.

The output voltage on the load impedance R_L is

$$V_{out}(t) = -R_L i_l(t). \tag{3.30}$$

With Eq. (3.30), the output pulse for the on-chip PFL-based high voltage pulse generation circuit with four stacked MOSFET switch is modeled and shown in Fig. 3.11. The obtained pulse agrees reasonably well with the simulated one, which validates the high voltage switch and output pulse modeling method.

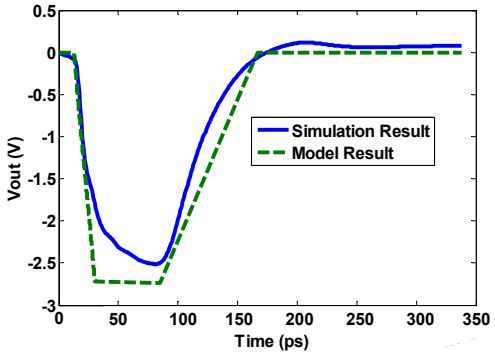


Figure 3.11 Modeled and simulated output voltage for PFL-based high voltage pulse generation circuit.

3.2.4 PFL-Based Pulse Generation Circuit Implementation and Measurement Results

The proposed charge pump circuits in PFL-based pulse generation circuits are implemented in a commercial 0.13 μm bulk CMOS process. Fig. 3.12 shows the measured output voltages of the charge pump with diode-connected zero V_{th} MOSFETs

under different power supply voltages. The output current for Fig. 3.12 is 30 µA. With a 2.4 V power supply, the corresponding output voltage is ~6.414 V.

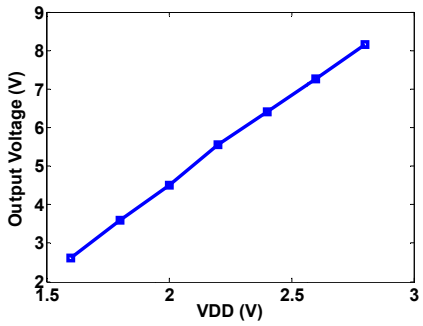


Figure 3.12 Measured output voltages of the charge pump with diode-connected zero V_{th} MOSFETs under different power supply voltages. The clock frequency is 5 MHz.

The on-chip PFL-based high voltage pulse generation circuit with a four stacked MOSFET switch is fabricated in an IBM 0.13 µm CMOS process. Figure 3.13 shows a micrograph of the circuit with 5 mm meander transmission line. It occupies 1072 µm×600 µm without the measurement pads. The four stacked MOSFETs used in the proposed system can switch $4\times V_{dd}$ (6.4 V). Thus, the theoretical output pulse has 3.2 V amplitude and 77 ps FWHM.

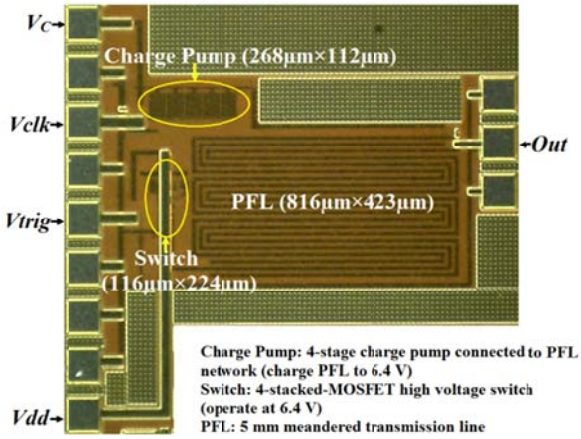


Figure 3.13 Micrograph of the on-chip PFL-based high voltage pulse generation circuit.

The simulated output pulse shown in Fig. 3.14 has 93 ps FWHM. The 16 ps difference mainly comes from the slow switching process and the parasitic capacitances of the stacked MOSFETs. And the obtained pulse amplitude is ~2.51 V, which is ~0.69 V less than $V_{dd}/2$. The difference is likely due to on-resistances of stacked MOSFETs and slow trigger pulse rise time.

The output pulse was measured with a Tektronix DSA8200 sampling oscilloscope with an 80E06 sampling module which has 70+GHz bandwidth. The measured output pulses are shown in Fig. 3.15. From Fig. 3.15 (a), the output pulse amplitude is ~925 mV with ~141 ps pulse width under Average Acquisition Mode. Fig. 3.15 (b) shows the measured output pulse with ~1.13 V amplitude under Envelope Acquisition Mode. A connection system with probes, cables and connectors is used to bring the output pulses to the 50 Ω terminated oscilloscope. This connection system is characterized with the two-port R&S ZVA50 vector network analyzer which has 50 GHz bandwidth. The obtained frequency response of the connection system is shown in Fig. 3.16, which results in a voltage loss on the output pulse.

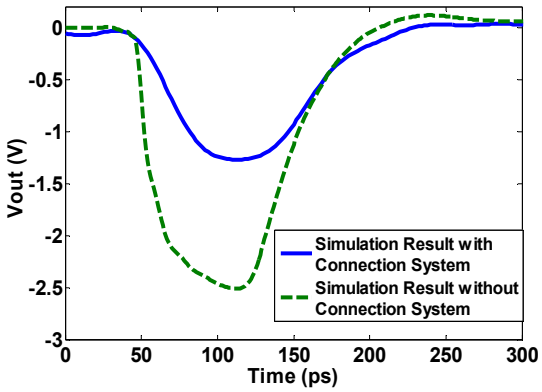
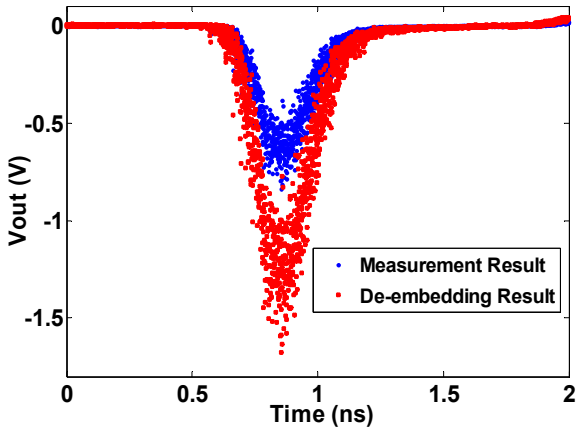
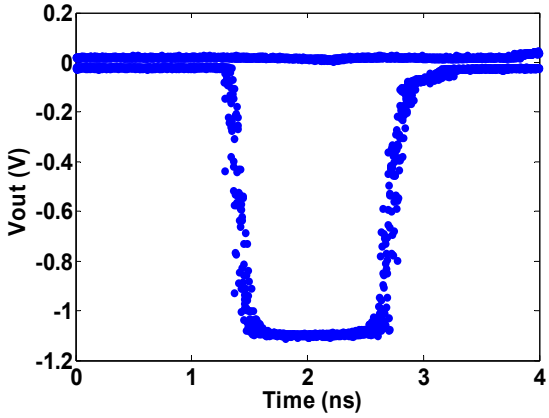


Figure 3.14 Simulated output pulse with and without measurement connection system.



(a)



(b)

Figure 3.15 Measured output pulses (a) under Average Acquisition Mode and (b) under Envelope Acquisition Mode.

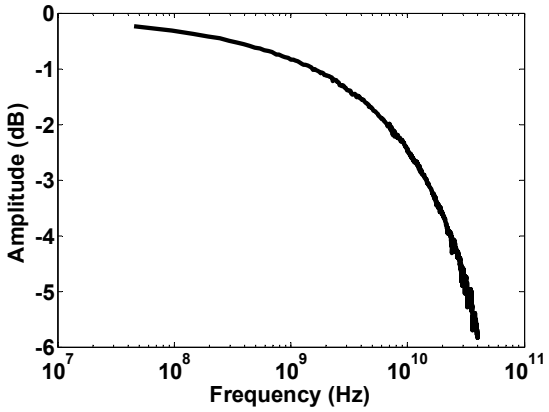


Figure 3.16 Frequency response of the connection system.

TABLE 3.2 Simulated output pulse with and without connection system

	Amplitude (V)	Duration (ps)	Fall time (ps)	Rise time (ps)
Before Attenuation	2.51	93	43.5	57.5
After Attenuation	1.27	95	45.5	70

MATLAB simulation shows that if the simulated output pulse in Fig. 3.14 is used as the input of the connection system, the output shown in Fig. 3.14 is attenuated to half of the input mainly caused by the connection system. The output pulse of ~1.27 V with ~95 ps FWHM is obtained by taking into account the connection effect. The comparison between the input and output pulse is summarized in Table 3.2. It indicates that the connection system attenuates the output pulse by a factor of ~2. To de-embed the connection system effect for the measured pulse under Average Acquisition Mode shown in Fig. 3.15 (a), the pulse of ~1.8 V with 135 ps is obtained. We estimate that the output amplitude, under Envelope Acquisition Mode shown in Fig. 3.15 (b), is ~2.26 V before being attenuated by the connection system, which is about 90% of the simulation value.

The measured results in Fig. 3.15 (a) are far from the ideal output of 3.2 V and 77 ps FWHM. The results are also worse than the simulated results, 2.51 V amplitude with 93 ps pulse duration. The on-resistances and parasitic capacitances of the stacked MOSFET switch cause voltage loss and slower on and off switch time, which reduces pulse amplitude and increase pulse width. Nevertheless, the output pulse is higher than the rated V_{dd} of the process with a pulse width close to $2\times\tau_{FO4}$ on a 50 Ω load. The circuit performance can be further improved for higher voltages and shorter pulses. For instance, MOSFETs with compact waffle layout, instead of the conventional multi-finger layout used in Fig. 3.13, can be used for switch layout. The waffle MOSFETs offer about 50%

reduction in gate resistance, 50% reduction in source/drain to substrate capacitance, 30%-40% reduction in area, and 30%-50% enhancement in f_{max} [3.30]-[3.31], for the same device width. Charge pumps with modified triple-well diodes in the same process can be used to generate 12.3 V from 1.6 V, much higher than 6.4 V in Fig. 3.13. Thus, higher outputs can be expected even though more MOSFETs are needed for the switch. Additionally, more advanced CMOS technologies will boost the speed of the switch further, which is effective to generate shorter pulses on a 50 Ω load. Therefore, our PFL circuit techniques have the potential to generate picosecond pulses.

3.3 Reducing Power-Supply and Ground Noise Induced Timing Jitter in PFL-Based Pulse Generation Circuits

Recently, we proposed pulse-forming-line (PFL) based short pulse generation circuits shown in Fig. 3.17 [3.15], [3.32], which significantly extends the short pulse generation capabilities of CMOS technology. The circuit has three main components: a trigger pulse generator in Fig. 3.18, a switch and a PFL network. In [3.15], an NFET switch is used to generate ~168 mV and ~116 ps pulses on a 50 Ω load under 1.6 V V_c. Nevertheless, the measured pulse duration and fall/rise times are much longer than simulation results due to timing jitters. Since the time properties of the trigger pulse generator are easily affected by any change in the power or ground. The jitters are mainly induced by power-supply and ground noise disturbances in the trigger pulse generator consisting of conventional CMOS inverters and NAND gates, which causes pulse murky rise and fall edges and measurement uncertainty.

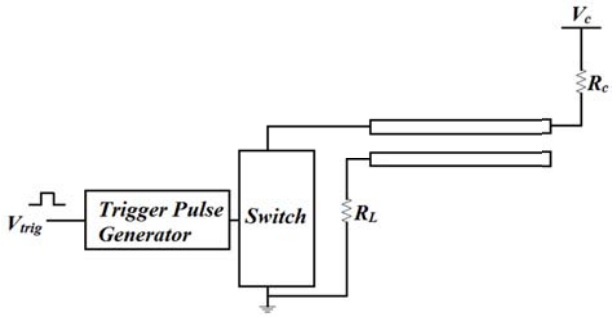


Fig. 3.17 A schematic of a PFL based on-chip short pulse generator.

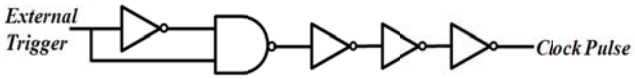


Fig. 3.18 On-chip trigger pulse generator.

In high-speed systems, jitter caused by power supply and ground noise can be reduced by using differential signaling. Similarly, MOS current-mode logic (MCML) circuits have better immunity to power-supply and ground noise than conventional CMOS logic circuits, due to fully differential structures [3.33]. In addition, MCML circuits have high speed due to small output-voltage swings, and low power supply noise generation due to constant current sources. To reduce the timing jitter of PFL-based pulse generation circuits, MCML inverters and NAND gates are used to replace conventional CMOS circuits in the trigger pulse generator.

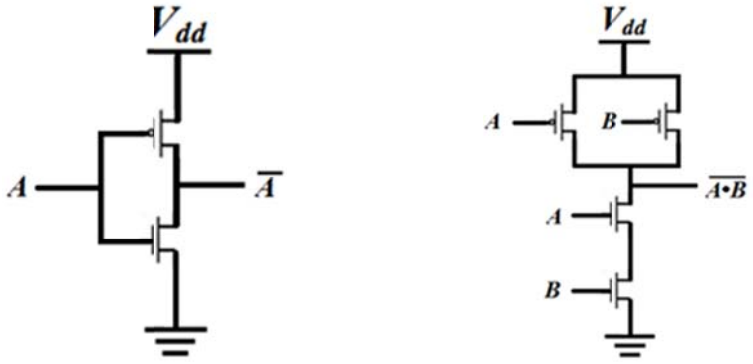
3.3.1 Time Jitter of Trigger Pulse Generator Using Conventional CMOS Inverter and NAND Gate

Fig. 3.19 shows the schematic diagrams of the conventional CMOS inverter and NAND gate. To analyze the timing jitter of these CMOS logic blocks induced by power-

supply and ground noise, Matlab was used to create the power-supply and ground noise vectors $\{\delta_V, \delta_G\}$, which has Gaussian functions with zero means and standard deviations $\{\sigma_V, \sigma_G\} \in [0, 0.1] \times V_{dd}/3$ [3.34]. Then Cadence was used to simulate these conventional CMOS circuits together with generated power-supply and ground noise, based on 0.13 μm CMOS technology. The circuit blocks were simulated for 1000 clock cycles while the power and ground noise were randomly changed. The obtained propagation delays t_{pd}, defined as the time required for a signal traveling from the inputs of circuits to the outputs, were compared with the ideal propagation delay without power-supply and ground noise, and the variations can be calculated as

$$\Delta t_{pd} = t_{pd}(\delta_G, \delta_V) - t_{pd}(0,0). \tag{3.31}$$

The obtained propagation delay variations were plotted into histograms. To deduce the timing jitter root mean square (RMS) induced by power-supply and ground noise, the standard deviation of the variations was extracted from the spread of the histograms.

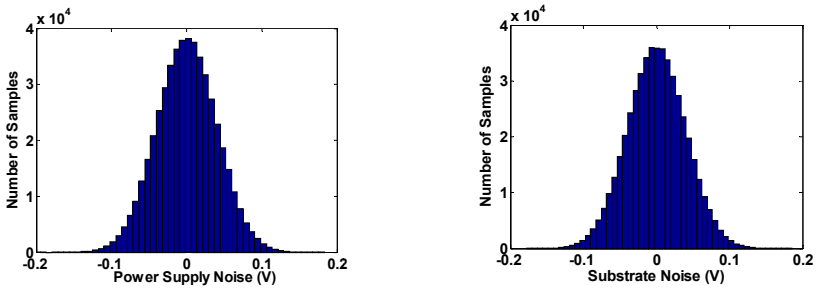


(a) (b)

Fig. 3.19 Schematic of conventional CMOS (a) inverter (b) NAND gate.

Fig. 3.20 shows the histograms of the power-supply and ground noise. The Cadence simulation results, where the variations in propagation delay of the trigger pulse

generation circuit using conventional CMOS inverters and NAND gates have been obtained, are shown in Fig. 3.21. The Δt_{pd} histograms have the similar Gaussian shape as the power-supply and ground noise. A Gaussian distribution is used to fit the propagation delay variations Δt_{pd} of the CMOS trigger pulse generator and extract the standard deviation σ (9.78×10^{-13}s) of Δt_{pd} as jitter RMS. Three-sigma rule says that the 6σ standard deviation is approximately 99.7 percent of data points within ±3σ of the mean for a Gaussian distribution. Thus, the peak to peak (p-p) jitter of the CMOS trigger pulse generator can be defined as 6σ (5.87×10^{-12}s), meaning the full width of the Δt_{pd} histogram.



(a) (b)

Fig. 3.20 Histogram of (a) power-supply noise (b) ground noise.

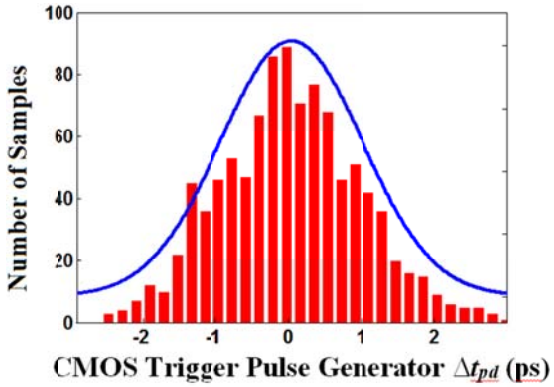


Fig. 3.21 Histogram of the propagation delay variations for CMOS trigger pulse generator.

3.3.2 Time Jitter Model for PFL-Based Pulse Generation Circuits

The response surface model (RSM) combined with latin hypercube sampling (LHS) is proposed as the surrogate model for analyzing the timing jitter of short pulse generation circuits. LHS, a space filling design, is used to uniformly sample points in the whole design space [3.35]. Cadence simulations are used to obtain the timing jitters at different sets of sampling points. Then the RSM of the timing jitter is built on these sampling points.

To model the timing jitter characteristics of short pulse generators, power supply V_{dd}, power-supply noise standard deviation σ_V and ground noise standard deviation σ_G are used as input variables. Table I summarizes the LHS design for 8 sampling points on each of these three inputs.

A response surface model can be represented as [3.36]

$$y = \beta_0 + \sum_{i=1}^{k} \beta_i x_i + \sum_{i=1}^{k} \beta_{ii} x_i^2 + \sum_{i=1}^{k} \sum_{j \neq i}^{k} \beta_{ij} x_i x_j \ , \tag{3.32}$$

where k is the number of independent input variables. Based on the sampling points listed in Table 3.3, the corresponding timing jitters for the CMOS short pulse generator can be simulated through Cadence. The RSM of the timing jitter is built as

$$\begin{aligned} \sigma_{CMOS} = {} & 8.81606 - 6.729 \times \frac{(V_{dd} - 1.45)}{0.15} + 3.24644 \times \frac{(\sigma_V - 0.04)}{0.04} + 2.9571263 \times \frac{(\sigma_G - 0.04)}{0.04} \\ & + 3.8778 \times \left(\frac{(V_{dd} - 1.45)}{0.15} \right)^2 - 1.9640731 \times \frac{(V_{dd} - 1.45)}{0.15} \times \frac{(\sigma_V - 0.04)}{0.04} \\ & - 3.07825574 \times \frac{(V_{dd} - 1.45)}{0.15} \times \frac{(\sigma_G - 0.04)}{0.04} - 1.65087 \times \frac{(\sigma_V - 0.04)}{0.04} \times \frac{(\sigma_G - 0.04)}{0.04} \end{aligned} \tag{3.33}$$

The RSM of the CMOS short pulse generator timing jitter shows good agreement with the Cadence simulations, as shown in Fig. 3.22. Based on Eq. (3.33), the timing jitter as function of V_{dd}, σ_V and σ_G shown in Fig. 3.23 can be obtained. Fig. 3.23 shows

that as V_{dd} increases, the power-supply and ground noise have less effect on the timing jitter.

TABLE 3.3 LHS Design for Timing Jitter Modeling

N	σ_V (V)	σ_G (V)	V_{dd} (V)
1	0.03428571	0	1.47142857
2	0.05714286	0.05714286	1.34285714
3	0.02285714	0.02285714	1.3
4	0.01142857	0.04571429	1.6
5	0.08	0.01142857	1.38571429
6	0	0.06857143	1.42857143
7	0.04571429	0.08	1.51428571
8	0.06857143	0.03428571	1.55714286

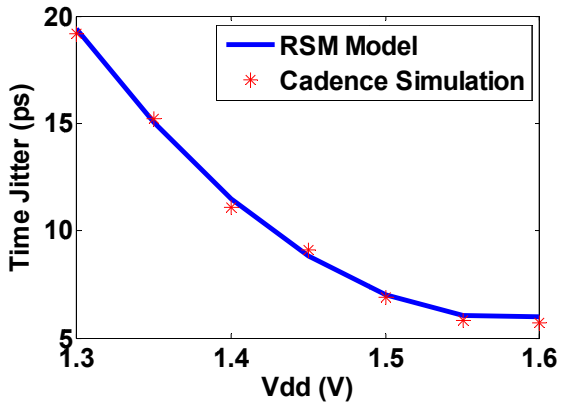
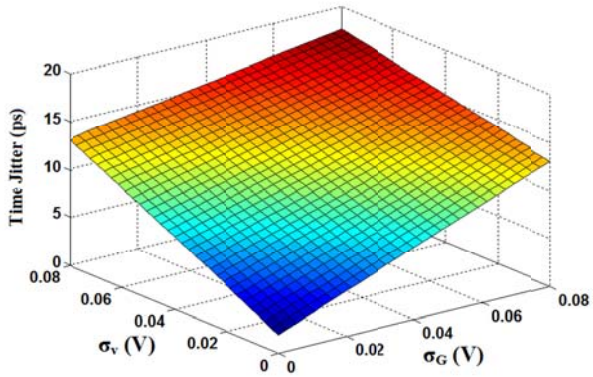
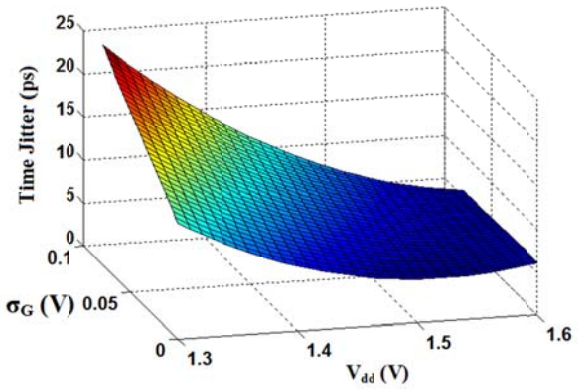


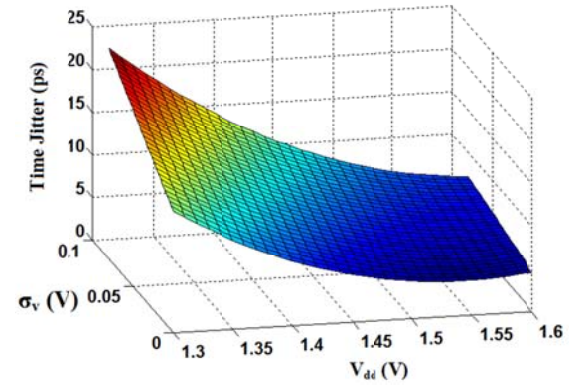
Fig. 3.22 Comparison of timing jitters obtained by RSM and Cadence simulations when σ_V=0.04 V and σ_G=0.04 V.



(a)



(b)



(c)

Fig. 3.23 CMOS short pulse generator timing jitter function (a) V_{dd}=1.4 V (b) σ_V=0.04 V (c) σ_G=0.04 V.

3.3.3 PFL-Based Pulse Generation Circuit Using MCML Inverter and NAND Gate

In order to reduce the timing jitter induced by power-supply noise and ground noise, the conventional CMOS inverter and NAND gate can be replaced with MCML inverter and NAND gate, shown in Fig. 3.24, in the trigger pulse generator to generate short pulse on chip. This is because MCML logic circuits achieve higher speed, consuming less power, and have higher noise immunity than conventional CMOS circuits. A typical MCML circuit consists of the current source (M_3), the logic block based on the

differential pair circuit ($M_{1,2}$), and the active pMOS loads (M_{p1}). For the MCML inverter in Fig. 3.24 (a), M_1 operate in the saturation region and the pMOS loads M_{p1} operate in the triode region. The equivalent resistance of M_{p1} is given by

$$R_p = \frac{1}{[\mu_p C_{ox} \frac{W_p}{L_p}(V_{dd} - |V_{Th,p}|)]}. \tag{3.34}$$

The propagation delay t_{pd} of the MCML inverter is approximated by

$$t_{pd} = 0.69 R_p C, \tag{3.35}$$

where C is the total load capacitance.

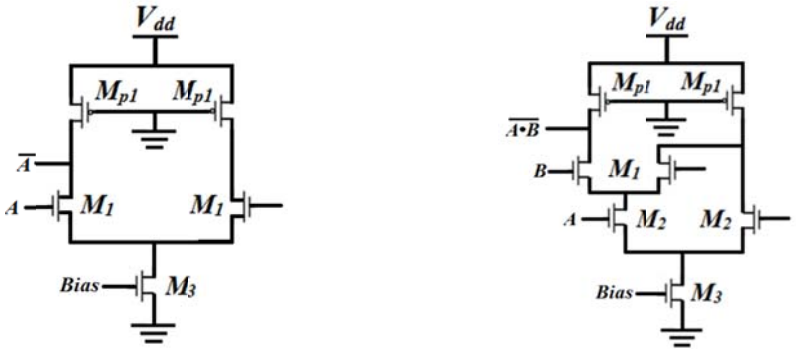


Fig. 3.24 Schematic of MCML (a) inverter (b) NAND gate.

The determination of the timing jitter of the trigger pulse generator using MCML inverters and NAND gates is similar to the CMOS case, shown in Section 3.3.1. The standard deviation of the propagation delay variations Δt_{pd} for the MCML trigger pulse generator is extracted as jitter RMS (6.83×10^{-13}s) from the histogram shown in Fig. 3.25, a 30% improvement over the trigger pulse generator based on conventional CMOS logic circuits. And the p-p jitter can be defined as 6σ (4.1×10^{-12}s), which is 1.77×10^{-12}s lower

than CMOS designs. These improvements are mainly due to the differential structure and high switching speed of MCML logic circuits, which has better immunity to power-supply and ground noise.

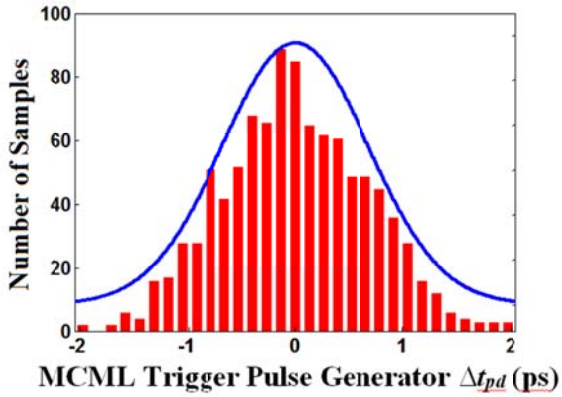
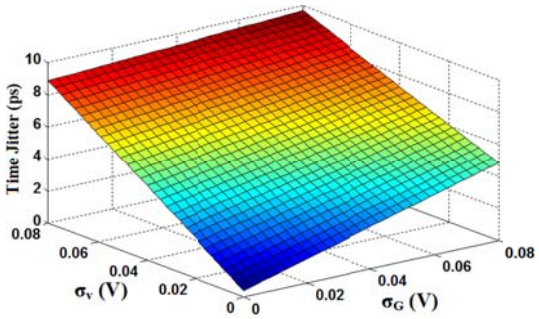


Fig. 3.25 Histogram of the propagation delay variations for MCML trigger pulse generator.

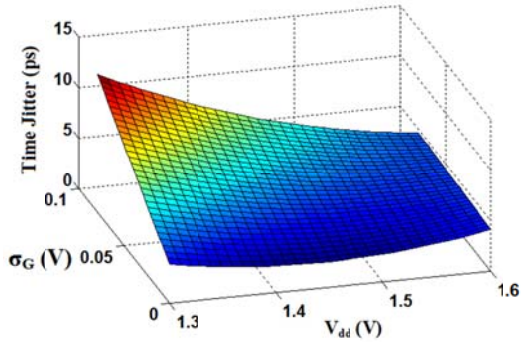
Based on the LHS design listed in Table 3.3, the RSM of the timing jitter in the short pulse generator using the MCML inverters and NAND gates can be expressed as

$$\begin{aligned}\sigma_{MCML} = {} & 5.076835 - 2.1484 \times \frac{(V_{dd} - 1.45)}{0.15} + 0.96783 \times \frac{(\sigma_V - 0.04)}{0.04} + 2.57391 \times \frac{(\sigma_G - 0.04)}{0.04} \\ & + 1.47149 \times \left(\frac{(V_{dd} - 1.45)}{0.15} \right)^2 - 1.0445871 \times \frac{(V_{dd} - 1.45)}{0.15} \times \frac{(\sigma_V - 0.04)}{0.04} \\ & - 2.3021 \times \frac{(V_{dd} - 1.45)}{0.15} \times \frac{(\sigma_G - 0.04)}{0.04} - 0.8958 \times \frac{(\sigma_V - 0.04)}{0.04} \times \frac{(\sigma_G - 0.04)}{0.04}\end{aligned} \tag{3.36}$$

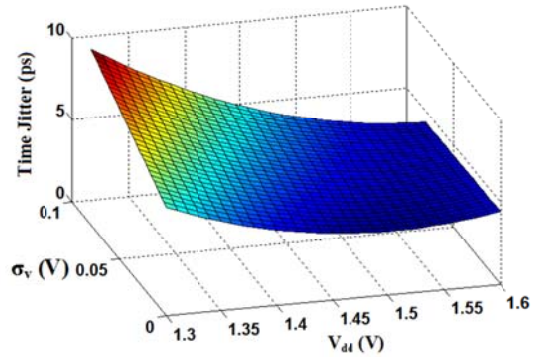
According to Eq. (3.36), the timing jitter of MCML short pulse generator as function of V_{dd}, σ_V and σ_G shown in Fig. 3.26 can be obtained. The maximum timing jitters under the corresponding conditions for the CMOS and MCML short pulse generation circuit are summarized in Table 3.4. The worst cases are shown in bold. From Table 3.4, compared with the conventional CMOS designs, the power-supply and ground noise induced timing jitter of the MCML short pulse generation circuits can be reduced by up to 50%.



(a)



(b)



(c)

Fig. 3.26 MCML short pulse generator timing jitter function (a) V_{dd}=1.4 V (b) σ_V=0.04 V (c) σ_G=0.04 V.

TABLE 3.4 Maximum Timing Jitter

	V_{dd}=1.4 V	σ_V=0.04 V	σ_G=0.04 V
CMOS Maximum	17.72 ps	**25.46 ps**	24.63 ps
MCML Maximum	9.72 ps	**13.57 ps**	10.71 ps

3.3.4 Conclusions

This section presents an investigation of the timing jitter induced by power-supply and ground noise in proposed PFL-based pulse generation circuits. And the response surface model combined with latin hypercube sampling is used to model the timing jitter. In order to reduce the timing jitter in short pulse generators, MCML logic circuits are implemented in the trigger pulse generator. Moreover, it is shown that the power-supply and ground noise induced timing jitter generated by the MCML short pulse generation circuit has a 50% improvement over the conventional CMOS designs.

3.4 On-chip Marx Generator

Marx generators, which generate high-voltage high-power electrical pulses from low-voltage and low-power supplies, are a common module in pulsed power systems [3.37]. The capacitors in a Marx generator is charged in parallel and then discharged in series, effectively increasing the output voltage to $N \times V_c$, where N is the number of capacitors and V_c is the charging voltage. Therefore, it is of great interest to develop on-chip Marx generators, which have not been reported so far, to overcome the voltage and power limitation of CMOS technologies.

A potential application of such Marx generator circuits is to realize a truly portable lab-on-chip system that need high-voltage and high-power electrical pulses, which are not available with standard CMOS devices and circuits [3.2], [3.38]. For instance, pulsed field electrophoresis requires a field intensity of 1-10 kV/m across a ~ 10-100 μm microfluidic channel. Thus, voltages of 10 V to 100 V, which are much

higher than the transistor breakdown voltages, need to be generated. Additionally, high-voltage high-power sources are needed to drive sensors and improve system-on-chip integration capabilities [3.39].

In this section, an on-chip Marx generator using stacked MOSFETs as high voltage switches is presented. Compared with conventional ones [3.37], [3.40], short connection wires and switch current paths yield smaller inductances, thus reduce voltage loss. Low on-resistances of switches result in fast recovery time, which leads to high repetition rate operations. Additionally, our circuit occupies small areas, leading to easy implementation for system integration.

3.4.1 On-chip Marx Generator Design Consideration

Fig. 3.27 shows the schematic of our 3-stage on-chip Marx generator. The main switches (S_{w1}~S_{w2}) in Fig. 3.27 are implemented with stacked MOSFETs in series. The resistors R_C are used to charge the stage capacitors C in charging mode and provide isolation in discharging mode. Higher R_C values lower system loss.

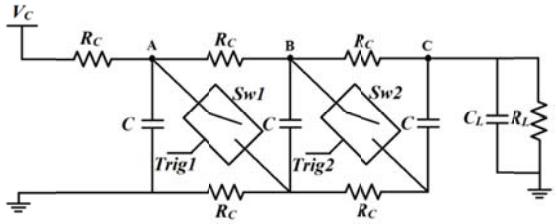


Figure 3.27 The schematic of the proposed 3-stage CMOS Marx generator.

In charge mode, the high voltage switches S_{w1}~S_{w2} are off, the input voltage V_c charges each stage capacitor C through R_Cs. Figure 3.28 shows the equivalent circuit, in which R_{Sw} represents the effective resistances of the switches.

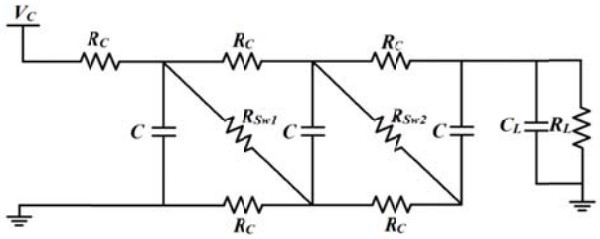


Figure 3.28 Equivalent circuit of Marx generator under charging mode.

The charging time of the Marx generator can be approximately expressed by [3.41]

$$t_r = N^2 R_C C, \tag{3.37}$$

where C is the stage capacitance, R_C is the charging resistance, and N is the number of stages.

In discharge mode, the switches are turned on simultaneously. The stage capacitors are switched into a series configuration, delivering a maximum voltage of $N \times V_c$ to the load. The Marx generator can be simplified into an equivalent circuit in Fig. 3.29. All the stage capacitors are lumped into a single capacitor C_{eq}, which can be expressed as

$$C_{eq} = \frac{C}{N}. \tag{3.38}$$

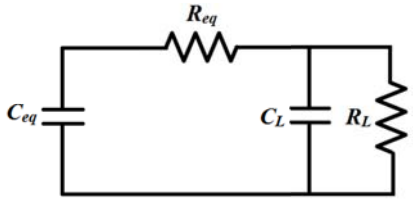


Figure 3.29 Equivalent circuit of Marx generator under discharging mode

And R_{eq} represents the total on-resistances from high voltage switches. If the voltage on the equivalent capacitor is V, the voltage on the load $V(s)$ is [3.29], [3.42]

$$V(s) = \frac{V}{R_{eq}C_L} \times \frac{1}{s^2 + s\left[\frac{1}{R_L C_L} + \frac{1}{R_{eq}C_L} + \frac{1}{R_{eq}C_{eq}}\right] + \frac{1}{R_{eq}R_L C_{eq}C_L}}. \tag{3.39}$$

Assuming R_L is much larger than the series resistor R_{eq} and the load capacitance C_L is smaller than the equivalent capacitance C_{eq}, the inverse transform of Eq. (3.39) gives [3.29]

$$v(\mathrm{t}) = \frac{V}{\left(\frac{1}{R_{eq}C_L} - \frac{1}{R_L C_{eq}}\right)R_{eq}C_L} \times \left[\exp\left(-\frac{t}{R_L C_{eq}}\right) - \exp\left(-\frac{t}{R_{eq}C_L}\right)\right]. \tag{3.40}$$

The rise time of the output is controlled by the on-resistances of the high voltage switches and the load capacitor. And the duration of the output can be tuned by changing the duration time of the trigger signals.

3.4.2 Stacked MOSFETs As High Voltage Switches

Fig. 3.30 shows the high voltage switch with four stacked MOSFETs since the breakdown voltage of a single MOSFET is limited. Table 3.5 shows the design parameters for capacitors (C_2~C_4) obtained from Eq. (3.3). Fig. 3.31 shows the simulation result of 4 stacked MOSFETs switch. When the stack turns on, all the four devices turn on almost simultaneously, pulling the output to low voltage level. Due to ON resistance of four devices in series, the output voltage does not fall to zero. In Fig. 3.31, the four stacked MOSFETs switch is biased with 6.4 V supply. When the stacked MOSFETs are turned off, each device supports an even 1.6 V share of the 6.4 V supply.

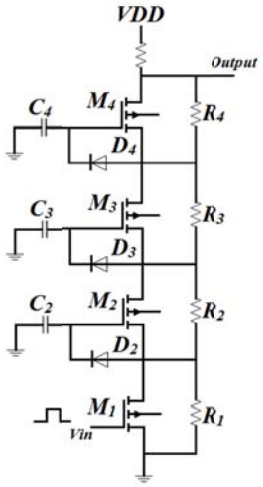


Figure 3.30 Four stacked MOSFET high voltage switch.

TABLE 3.5
DESIGN PARAMETERS FOR CAPACITORS IN SWITCH

Capacitor	Value
C2	2.5pF
C3	800.27fF
C4	400.14fF

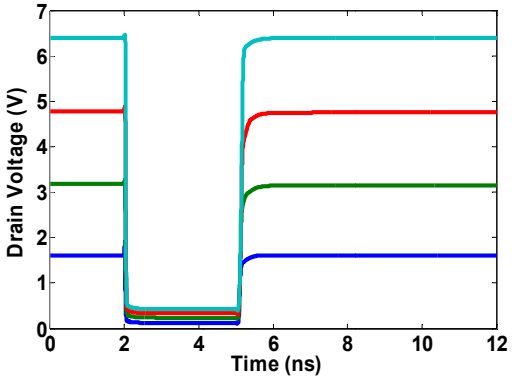


Figure 3.31 Simulation results of stacked MOSFETs in series.

3.4.3 On-chip Marx Generator Measurement

Fig. 3.32 shows a micrograph of an on-chip Marx generator in a 0.13 μm CMOS process. The stage capacitors are 100 pF metal-insulator-metal (MIM) capacitors. Four

stacked MOSFETs are used as high voltage switches. The 3.3 V I/O NFETs of the process are used as the bottom switch transistor to improve high voltage performance. As a result, the four stacked MOSFETs can operate under $4\times V_{dd}$ (4.8~6.4 V).

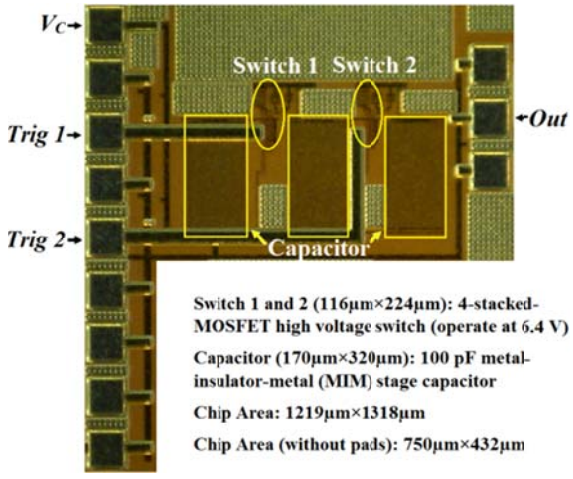


Figure 3.32 Micrograph of the on-chip Marx generator.

For V_c=8 V, which could be provided by a charge pump circuit, simulation and calculation show that the charging voltages at nodes A, B and C in Fig. 3.27 are 6.4 V, 5.6 V and 5.4 V respectively. The charging resistors, R_C, and the resistors in the switch, cause voltage loss. Ideally, the output voltage is 17.4 V. Fig. 3.33 shows the measured results when the load is a parallel combination of 1 MΩ resistor and a 13 pF capacitor. The obtained 11.68 V is ~2/3 of maximum result. The discrepancy is likely due to currents leaking through the switch resistors and voltage loss caused by the measurement setup, which includes contact pads, probes, connectors and cables. The rise time and fall time of the output pulse are 1.35 ns and 1.64 ns, respectively. Fig. 3.34 shows that the output voltages can be varied from 7.12 V to 11.95 V with different V_C. These voltage values are close to the highest breakdown voltage of the process. They are also sufficient

for many on-chip applications, such as electrophoresis requiring a field intensity of 1-10 kV/cm across a ~10-100 μm microfluidic channel, and sensor drivers.

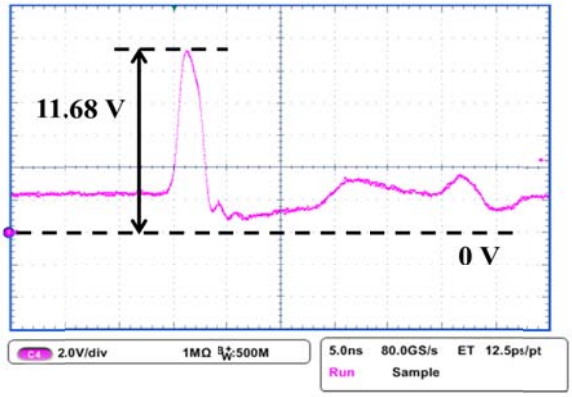


Figure 3.33 Measured waveform of 3-stage Marx generator circuit.

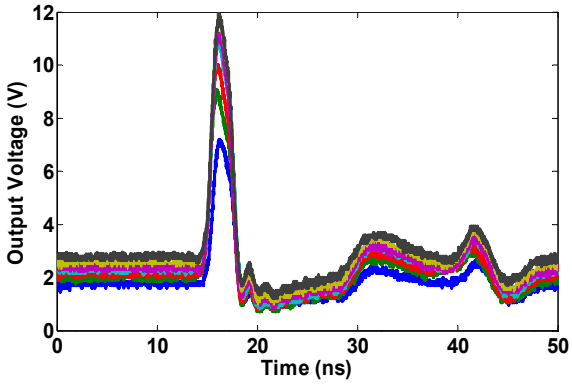


Figure 3.34 Output voltages under different charging voltages.

3.5 An On-chip Blumlein Pulse Generator

Among pulse-forming-line (PFL) based pulse generators, the Blumlein PFL configuration is considered an effective approach, since it is able to form pulses with the same voltage as the charging one and is adequate for generating pulses of short duration. The Blumlein PFL includes two identical transmission lines (TLs) connected to a high-voltage source (V_c) in series with the load. Once the TL is charged to the desired high

voltage and the switch is triggered, it discharges to generate a V_c pulse across a matched load Z_L, where V_c is the charging voltage [3.29]. Therefore, it is of great interest to develop on chip Blumlein generators, which have not been reported so far. Yet, high-impedance loads are not matched to 50 Ω-terminations oscilloscopes typically have. The mismatch leads to voltage loss during measurements. This work also introduces an on-chip Klophenstein taper to convert the load Z_L to 50 Ω, which helps avoid reflections. The Blumlein pulse generator is simple and compact since it does not need extra pulse shaping networks and can generate pulses directly from a DC-voltage input.

3.5.1 On-chip Blumlein Pulse Generator Design Consideration

Fig. 3.35 shows the schematic diagram of the on chip Blumlein generator with a Klophenstein taper and a stacked-MOSFET high voltage switch. The transmission line characteristic impedance Z_o is related to the load Z_L by the relation Z_o=45Ω=Z_L/2=90Ω/2 [3.43]. The Klophenstein impedance taper with 11 sections is used to match 50 Ω load of an oscilloscope in order to avoid reflections. The first section of the taper acts as the load Z_L. Because coplanar waveguide (CPW) provides higher operating frequencies, minimizes crosstalk and noise, and is easier for on-chip fabrication. On-chip CPWs are chosen for our circuit. In this work, the high voltage switch is a two-stacked-MOSFETs. The switch can operate under $2\times V_{dd}$ (3.2 V), where V_{dd} (1.6 V) is the rated highest operating voltage of our given process. A high voltage source (V_c=3.2 V), which can be easily provided by charge pump circuits, is used to charge Blumlein PFL network. When the switch is turned on by the trigger signal, which is sharpened by a trigger pulse

generator, the Blumlein PFL discharges through its load. The output pulse is then generated with an ideal amplitude of 3.2 V.

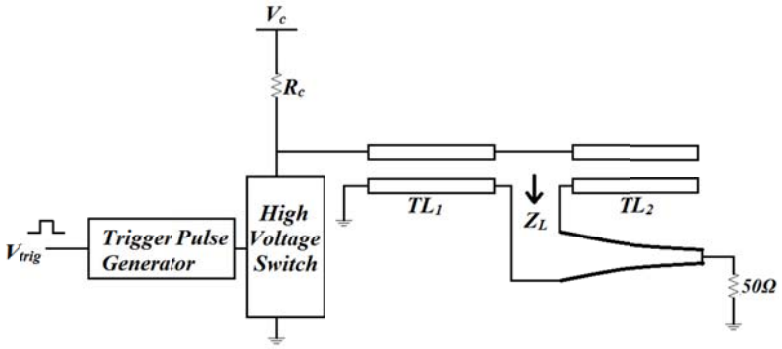


Fig. 3.35 Proposed on-chip Blumlein generator with a Klophenstein taper

3.5.2 On-chip Klophenstein Taper

Compared with other impedance tapers, the Klophenstein taper has the minimum reflection coefficient in the pass band for a specified taper length, and, similarly has the minimum length for a specified maximum reflection coefficient [3.44]. Therefore, on chip Klophenstein transmission line taper is chosen to convert high-impedance 90 Ω load to 50 Ω, which is suitable for measurements. The logarithm of the characteristic impedance variation for the Klophenstein taper is given by [3.45]

$$\ln Z(z) = \frac{1}{2}\ln Z_o Z_L + \frac{\Gamma_o}{\cosh A} A^2 \phi(2z/L - 1, A), for 0 \le z \le L \tag{3.41}$$

$$A = \cosh^{-1}\left(\frac{\Gamma_o}{\Gamma_m}\right) \tag{3.42}$$

where $\phi(z, A)$ is defined as the integral of a modified Bessel function, Γ_o is the reflection coefficient at zero frequency, Γ_m is the maximum ripple in the passband, and L is the length of Klophenstein taper.

The passband for the Klopfenstein taper is defined as $\beta L > A$. And the resulting reflection coefficient is given by

$$\Gamma(\theta) = \Gamma_o e^{-j\beta L} \frac{\cos\sqrt{(\beta L)^2 - A^2}}{\cosh A}, for\, \beta L > A \tag{3.43}$$

Fig. 3.36 shows the simulated reflection coefficient for our taper. From Fig. 3.36, the taper gives the desired response of $|\Gamma| < 0.02$ for $f > 10$ GHz.

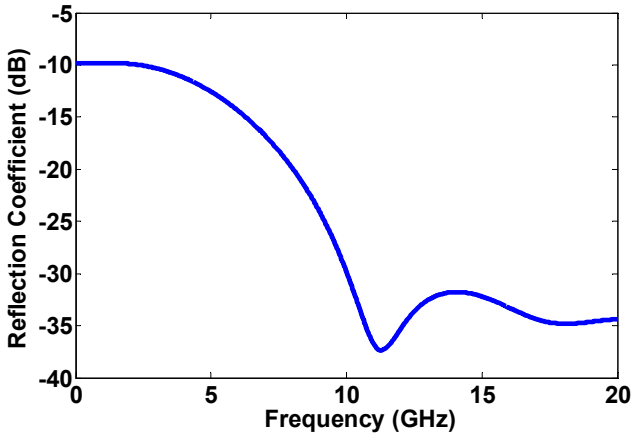


Fig. 3.36 Simulated result of on-chip Klophenstein taper

3.5.3 On-chip Blumlein Pulse Generator Measurement Results

The on-chip Blumlein generator is fabricated in an IBM 0.13 μm CMOS process. Fig. 3.37 shows a micrograph of the generator with two 3.75 mm meander transmission lines and a Klophenstein taper. It occupies an area of 1125 μm×1140 μm without the measurement pads. The two stacked MOSFETs used in this circuit can switch $2\times V_{dd}$ (3.2 V). Therefore, the ideal output has 3.2 V amplitude and 60 ps full-width-at-half-maximum (FWHM).

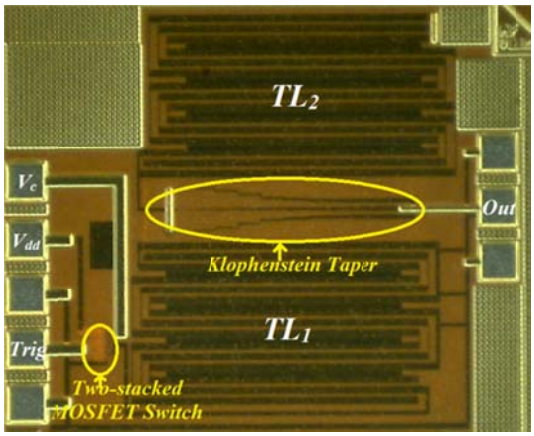


Fig. 3.37 A micrograph of on-chip Blumlein generator with an on-chip Klophenstein taper

The output pulse was measured with a Tektronix DSA8200 sampling oscilloscope (70+GHz bandwidth) with an 80E06 sampling module. The measured output pulses of ~725 mV with ~126 ps FWHM under Average Acquisition Mode are shown in Fig. 3.38. A connection system, including probes, cables, and connectors, is used to transmit the output pulses to the oscilloscope. The obtained frequency response of the connection system measured with the two-port R&S ZVA50 vector network analyzer is shown in Fig. 3.16, which results in the reduction of the amplitude of output pulses by a factor of ~2. After de-embedding the connection system effects, the obtained pulses are of ~1.41 V with 114 ps FWHM, shown in Fig. 3.38. If we further take into account the Klophenstein taper, it indicates that 725 mV on the oscilloscope corresponds to 1.88 V on a 90 Ω Z_L on-chip, which is still worse than the ideal output of 3.2 V and 60 ps FWHM as well as the simulated results of 2.67 V amplitude and 70 ps FWHM. The stacked-MOSFET switch and Klophenstein taper reduce pulse amplitude and increase pulse width. Nevertheless, the output pulse is higher than the rated V_{dd} of the process.

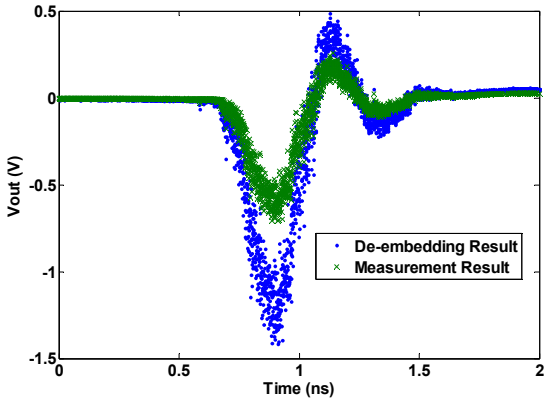


Fig. 3.38 Measured output pulses of on-chip Blumlein generator

The power spectral density (PSD) of the measured pulse from Fig. 3.38 was calculated by using the Fourier transform, shown in Fig. 3.39. It is seen that the 10 dB pulse bandwidth is 3.18 GHz.

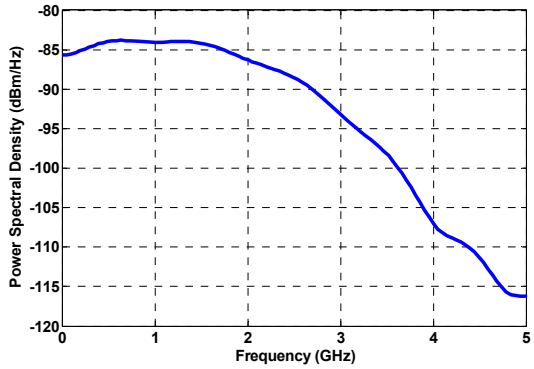


Fig. 3.39 Power spectrum of the output of on-chip Blumlein generator

3.6 Conclusions

In summary, a PFL-based high voltage short pulse generation circuit is implemented in a commercial 0.13 μm CMOS technology. The circuit includes a charge-pump module, a switch, and a pulse forming line. The high-voltage switch consists of

four-stacked-MOSFETs and operates under 6.4 V with ~9 Ω on resistance and ~33 ps fall time. Output pulses of ~1.8 V with ~135 ps FWHM on a 50 Ω load are obtained. The obtained voltage is higher than the rated-operating voltage (1.2-1.6 V). The pulse FWHM is close to $2\times\tau_{FO4}$.

An on-chip 3-stage Marx generator is designed and implemented in CMOS process. When a parallel combination of 1 MΩ and 13 pF is used as the load, the measured output voltage is up to 11.68 V with 1.35 ns rise time and 1.64 ns fall time. The voltage is well above the breakdown voltages of the FET (3.3V) and well-substrate junction 10 V of the given technology.

In this chapter, we also describe an on-chip Blumlein generator, including a two-stacked-MOSFET switch, a Klophenstein taper, and a Blumlein PFL network. A Klophenstein taper is included for broadband impedance transformation. The circuit is implemented in a standard 0.13 μm CMOS process. The measured output pulses on a 50 Ω load are 725 mV with ~126 ps FWHM and 3.18 GHz bandwidth. The pulse repetition rate can be up to 125 MHz. After de-embedding the effects of the connection system and Klophensein taper, pulses of ~1.88 V and ~114 ps can be obtained. The obtained voltage is higher than the rated V_{dd} (1.2-1.6 V) of the process.

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CHAPTER FOUR

A HIGHLY RECONFIGURABLE LOW-POWER CMOS DIRECTIONAL COUPLER AND SIX-PORT CIRCUIT

A CMOS broadband six-port circuit based on four quadrature hybrids is designed and proposed for analyzing signals in frequency domain. To realize the tunable and broadband six-port circuit, this chapter also presents a highly reconfigurable, low-power, and compact directional coupler. The coupler uses varactors and novel active inductors to achieve wide tuning ranges of operating frequencies and coupling coefficients. The use of a low-pass circuit architecture with only two inductors minimizes chip area, power consumption, and noise. The coupler is implemented in a 0.13 μm CMOS process. It occupies an area of 350 μm×340 μm and consumes 40 mW or less power. The obtained 1-dB compression point is -3.2 dBm, and the measured noise figure is ~23 dB. These parameters compare favorably with previously published reconfigurable couplers. The measured coupling coefficient can be tuned from 1.3 dB to 9.0 dB at 4 GHz with 32 dB or better isolation and 15 dB or better return loss. The operating center frequency can be tuned from 2.0 GHz to 6.0 GHz for a nominal 3-dB operation. These results agree with theoretical predictions and simulations reasonably well.

4.1 A Highly Reconfigurable Low-power CMOS Directional Coupler

Directional-couplers are widely used in various microwave systems, including balanced mixers, balanced amplifiers, phase shifters, filters, and phase array antennas

[4.1]-[4.5]. Conventional directional couplers, such as branch-line couplers, Lange couplers and coupled-line couplers, are realized with distributed transmission lines. At lower giga-hertz frequencies, these lines lead to large areas, which are a challenge in integrated microwave circuit development. Hence, various lumped-element directional-couplers are proposed to address the problem [4.6]-[4.8]. Additionally, reconfigurable directional-couplers, which have tunable coupling coefficients [4.9]-[4.12] and operating frequencies [4.13]-[4.17], are under development for applications in sequential amplifiers, reconfigurable antenna arrays and multi-standard systems.

Tuning elements, such as varactors and inductors, are needed to build reconfigurable couplers. Different circuit architectures, which are mostly derived from distributed transmission-line (TL) counterparts, determine the number of tuning components and the performance of the couplers. For instance, varactors were used to tune coupling-coefficients in [4.9]-[4.12] with large bias voltages (up to 30V in [4.9] and 25V in [4.10]). The couplers occupy large areas when compared to lumped-element ones. Varactors were also used to tune the center frequency of couplers in [4.13]-[4.16]. The circuits therein also occupy large areas and need large bias voltages. RF MEMS switches were used to build directional-couplers in [4.17]. However, the switches are not standard CMOS devices and have many challenges of their own. Therefore, fully integrated CMOS hybrids have been investigated. These CMOS circuits use active inductors and varactors to tune operating frequencies [4.18] and coupling-coefficients [4.19]. Nevertheless, current CMOS hybrids have limited frequency tuning range and significant power consumption.

In this section, we present a highly reconfigurable, low-power, and compact CMOS directional coupler, which only uses two active-inductors. Compared with the couplers in [4.18]-[4.19], our coupler achieves much larger frequency and coupling coefficient tuning ranges, mainly due to the use of minimum number of inductors, a novel active inductors design, and paired coupling varactors. The analysis of the proposed coupler is presented in Section 4.1.1. Section 4.1.2 gives the circuit implementation and measurement results. Section 4.1.3 concludes this section.

4.1.1 Circuit Analysis

The proposed lumped-element directional coupler exploits the low-pass architecture [4.6] in Fig. 4.1, which uses two inductors, half the amount of inductors used by the high-pass topology in [4.19]. Minimizing the number of inductors is critical since inductors are expensive in CMOS technology in terms of area and energy consumption.

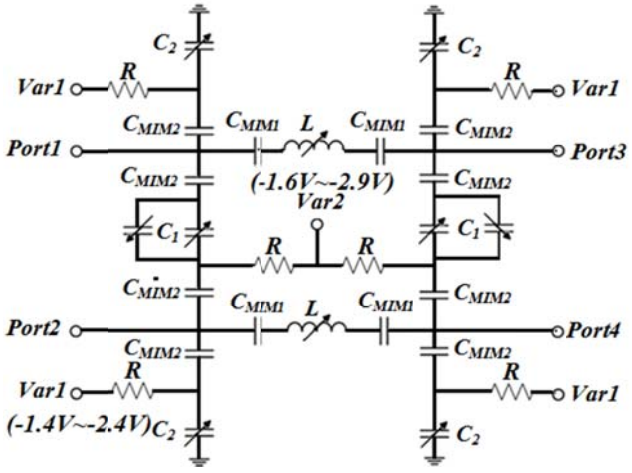


Figure 4.1 The proposed directional coupler circuit. C_1 and C_2 are varactors; C_{MIM1} and C_{MIM2} are isolation capacitors; V_{ar1} and V_{ar2} are control voltages.

Ignoring the isolation capacitors C_{MIM1} and C_{MIM2}, the even-odd mode analysis technique [4.20] gives the scattering parameter matrix of the hybrid as

$$S_{11} = \frac{\Gamma_e + \Gamma_o}{2} \tag{4.1}$$

$$S_{21} = \frac{T_e + T_o}{2} \tag{4.2}$$

$$S_{31} = \frac{T_e - T_o}{2} \tag{4.3}$$

$$S_{41} = \frac{\Gamma_e - \Gamma_o}{2} \tag{4.4}$$

where $T_{e,o}$ and $\Gamma_{e,o}$ are the transmission and reflection coefficients of the even- and odd-mode partial circuits, respectively. They are

$$T_e = \frac{2}{\left[2(1 - B_2 X_L) + j\frac{X_L}{Z_o} + jZ_o(2B_2 - B_2^2 X_L)\right]} \tag{4.5}$$

$$\Gamma_e = \frac{j\frac{X_L}{Z_o} - jZ_o(2B_2 - B_2^2 X_L)}{\left[2(1 - B_2 X_L) + j\frac{X_L}{Z_o} + jZ_o(2B_2 - B_2^2 X_L)\right]} \tag{4.6}$$

$$T_o = 2 / \{\, 2[1 - (2B_1 + B_2)X_L] + j\frac{X_L}{Z_o} + jZ_o[2(2B_1 + B_2) - (2B_1 + B_2)^2 X_L]\} \tag{4.7}$$

$$\begin{aligned} \Gamma_o = \{ & j\frac{X_L}{Z_o} - jZ_o[2(2B_1 + B_2) - (2B_1 + B_2)^2 X_L]\} / \{2[1 - (2B_1 + B_2)X_L] \\ & + j\frac{X_L}{Z_o} + jZ_o[2(2B_1 + B_2) - (2B_1 + B_2)^2 X_L]\} \end{aligned} \tag{4.8}$$

where B_1 and B_2 are susceptances of capacitors C_1 and C_2, respectively; X_L the reactance of the inductors L and Z_o=50 Ω the system impedance. To achieve low reflection coefficient and high isolation, we have

$$S_{11} = S_{41} = 0 \tag{4.9}$$

which yields

$$\omega_o^2 = \frac{1}{L(C_1 + C_2)} \tag{4.10}$$

$$2\omega_o^2 C_1 C_2 + \omega_o^2 C_2^2 = \frac{1}{Z_o^2} \tag{4.11}$$

where ω_o is the center frequency of the hybrid.

The transmission coefficient S_{21} and S_{31} are

$$S_{21}(\omega = \omega_o) = -j\sqrt{1 - \frac{C_1^2}{(C_1 + C_2)^2}} \tag{4.12}$$

$$S_{31}(\omega = \omega_o) = \frac{-C_1}{C_1 + C_2} \tag{4.13}$$

A. Coupling Coefficients

The coupling coefficient of the proposed directional coupler at f_o is

$$C = -20\log|S_{31}| = -20\log\frac{C_1}{C_1 + C_2} \tag{4.14}$$

which is independent of inductor L. Therefore, MOS varactors C_1 and C_2 can be used to tune the coupling coefficient independently as the calculation results shown in Fig. 4.2. Fig. 4.2 also shows the coupling coefficients ($|S_{31}|$) obtained from Cadence Spectre simulation with the extracted coupler circuit of Fig. 4.1. It shows that theoretical predictions agree with simulation results reasonably well; an 8.0dB coupling-coefficient tuning range (f_o=4GHz) can be achieved. To keep ω_0 unchanged, matching conditions satisfied, and isolation performance unaffected, Fig. 4.3 (a) shows the choice of inductor

L for different C_1 and C_2. Fig. 4.3 (b) shows explicit L curves versus C_1 for a few C_2 values.

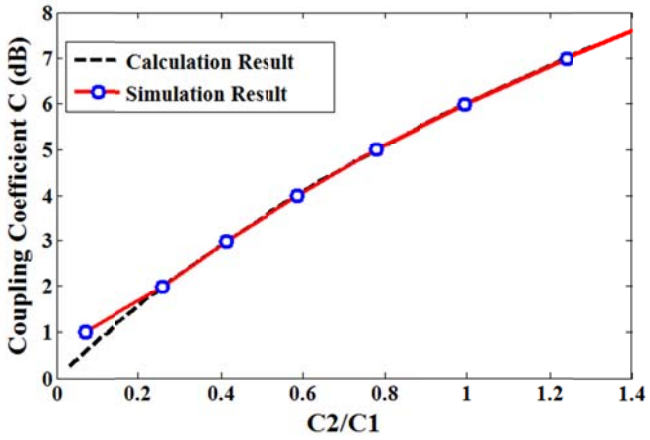
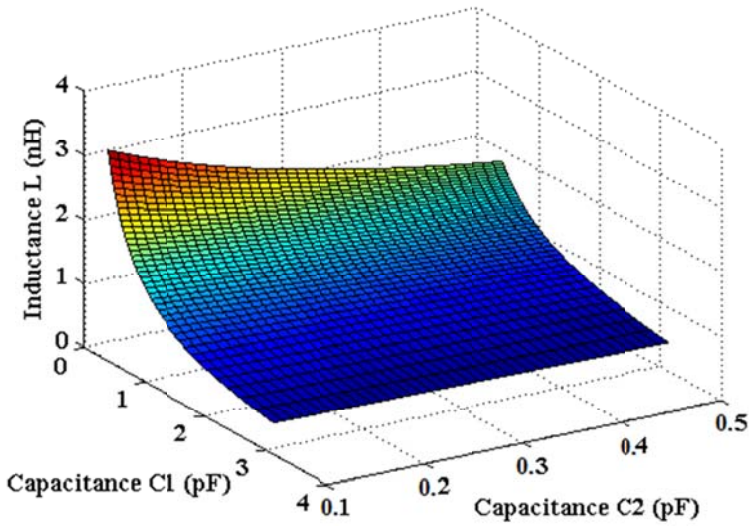
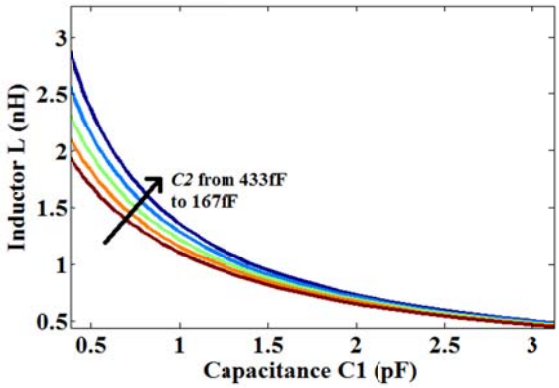


Figure 4.2 Coupling coefficients of the proposed directional coupler. Calculation results are obtained from (4.14) with ideal capacitors C_1 and C_2. Simulation results $|S_{31}|$ of Fig. 4.1 are obtained with varactors from our chosen CMOS process. C_1 is tuned from 300fF to 1.35pF, C_2 from 210fF to 549fF.



(a)



(b)

Figure 4.3 (a) The relationship of C_1, C_2 and L for f_o=4GHz and high isolation while coupling coefficient is tuned independently in Figure 4.2. (b) Inductor for different C_1 and given C_2 values.

B. Operating Frequencies

The operating frequency of the directional coupler can be tuned by changing the inductors (L), as indicated in Fig. 4.4. To keep the coupling coefficient a constant, C_1 and C_2 should satisfy (4.14), which yields

$$C_2 = (\sqrt{2} - 1) \times C_1 \tag{4.15}$$

for 3dB operations. The capacitors (C_1 and C_2) also need to be tuned accordingly to maintain low reflection coefficient, constant coupling coefficient, and high isolation. Substituting (4.10) into (4.11), we have

$$\frac{C_2}{L} + \frac{C_1 C_2}{L(C_1 + C_2)} = \frac{1}{Z_o^2} \tag{4.16}$$

Fig. 4.5 shows C_2 and L when C_1 is tuned. Fig. 4.4 shows reasonable agreement between the calculated results from (4.16) and simulated results with the real coupler

circuit, which will be further discussed later. Inductance L is varied to tune the operating frequency of the coupler. The discrepancy is mainly caused by parasitic components of circuit elements, such as poly-Si gate resistance of MOS varactors, parasitic resistance and capacitance of active inductors. Nevertheless, it shows that a 5GHz tuning range can be obtained.

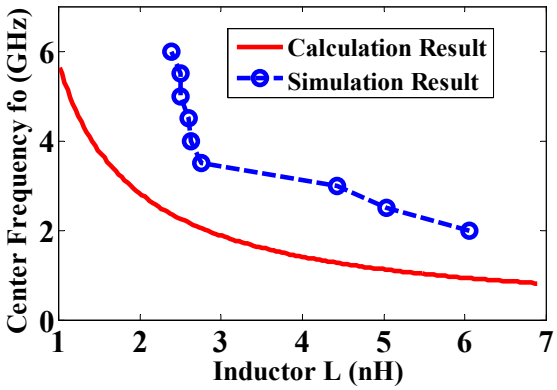


Figure 4.4 The operating center frequency for a 3dB nominal coupling-coefficient. L is calculated from (4.16). The simulation results are obtained by tuning varactors C_1, C_2 and active inductors L in Fig. 4.1.

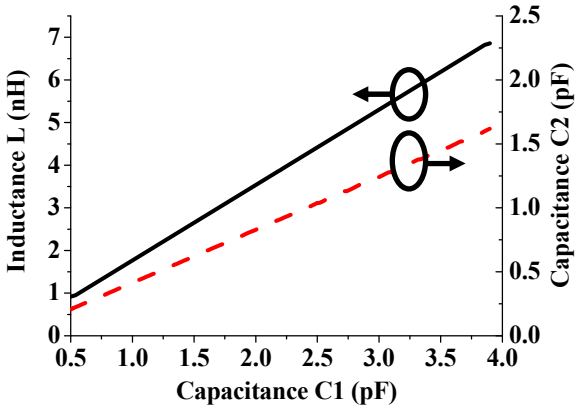


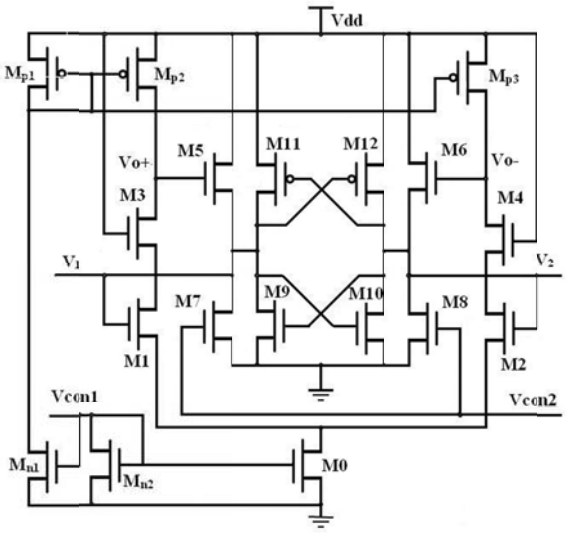
Figure 4.5 The tuning of C_2 and L with C_1 for the 3dB coupling coefficient operations in Fig. 4.4.

The above analysis shows that our chosen coupler in Fig. 4.1 has independent f_o and coupling coefficient tuning capabilities. In our chosen CMOS process, the coupling coefficient can be tuned from ~0.5dB to ~8dB, and the operating frequency can be tuned from ~2GHz to ~6GHz.

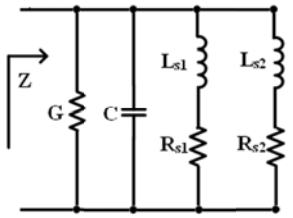
4.1.2 Circuit Implementation and Measurement Results

The directional coupler in Fig. 4.1 is implemented in a 0.13μm CMOS process. MOS varactors are used for C_1 and C_2. Capacitor C_1 is tunable from 250 fF to 1.1 pF and the capacitor C_2 from 145 fF to 610 fF. The use of a paired coupling capacitors for C_1 improved the reciprocity (i.e. symmetry) of the circuit, therefore, the coupler performance. C_{MIM1} and C_{MIM2} are for DC isolation. MOS varactors can be approximated by a resistor (R_S) in series with a nonlinear capacitor. R_S is dominated by the poly-Si gate resistance. This series resistance has a strong impact on the coupler's insertion loss.

The inductors in Fig. 4.1 are critical for the coupler operation. We employ the novel active inductor proposed in [4.21]-[4.22], as shown in Fig. 4.6 (a), while the design parameters are listed in the Table 4.1. Based on a gyrator-*C* architecture, two transconductance amplifiers are used to convert the susceptance of the gate-source capacitance of *M5* and *M6* to inductive impedance. *M9*, *M10*, *M11* and *M12* are the feedback pairs which can improve the self-resonant frequency, inductance value and *Q* factor of the active inductor. The equivalent circuit model in Fig. 4.6 (b) gives the input impedance as [4.22]



(a)



(b)

Figure 4.6 (a) The active inductor for the proposed coupler. (b) Equivalent circuit of the inductor. V_{con1} and V_{con2} are used to tune the active inductor parameters.

TABLE 4.1
CIRCUIT PARAMETERS OF THE ACTIVE INDUCTOR

Transistors	Size (μm /μm)
M_1, M_2	156/0.2
M_3, M_4	13/0.12
M_5, M_6	117/0.18
M_7, M_8	39/0.12
M_9, M_{10}	13/0.12
M_{11}, M_{12}	13/0.12
M_0	58.5/0.12
M_{p1}, M_{n1}	3.9/0.12
M_{p2}, M_{p3}	13/0.12
M_{n2}	0.64/0.12

$$Y_{in} = G + sC + \frac{1}{R_{s1} + sL_{s1}} + \frac{1}{R_{s2} + sL_{s2}} \tag{4.17}$$

$$L_{s1} = \frac{2C_{gs5}}{g_{m1}g_{m5}}, L_{s2} = \frac{2C_{gs3}}{g_{m1}g_{m3}} \tag{4.18}$$

$$R_{s1} = -\frac{2\omega^2 C_{gs3}C_{gs5}}{g_{m1}g_{m3}g_{m5}}, R_{s2} = \frac{1}{g_{m1}} \tag{4.19}$$

The fabricated coupler is shown in Fig. 4.7. It occupies 350µm×340µm without the measurement pads. The majority of the area is taken by the active inductors, which are 2×270µm×45µm. The directional coupler was measured with the two-port R&S ZVA50 vector network analyzer.

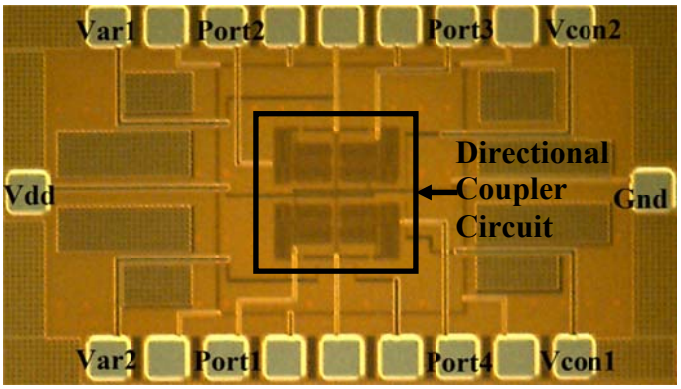


Figure 4.7 A die micrograph of the CMOS directional coupler. The bias voltage V_{ar2} and V_{ar1} are used to tune varactors C_1 and C_2, respectively. The fabricated chip is 1450µm×950µm.

A. Coupling Coefficients

Fig. 4.8 shows the measured coupling coefficients for different bias voltages at 4GHz. The corresponding isolation is shown in Fig. 4.9. It is shown that the coupling

coefficient of the proposed coupler can be tuned from 1.3dB to 9.0dB while the isolation is better than 30 dB on a 40MHz bandwidth. Therefore, 74%-9% of the input power at port 1 is transmitted to port 3. Moreover, the return loss is better than 15dB, as shown in Fig. 4.10. The insets of Fig. 4.8, 4.9 and 4.10 show the comparison of S_{31}, S_{41} and S_{11} magnitudes from calculation, simulation and measurement at 4GHz with 2.2dB coupling coefficient. These results agree with each other reasonably well. The directional coupler draws approximately 18mA dc current from a 1.6V voltage supply. The power consumption is 28.8mW. Across the entire coupling coefficient tuning range, the insertion loss is less than ~2dB.

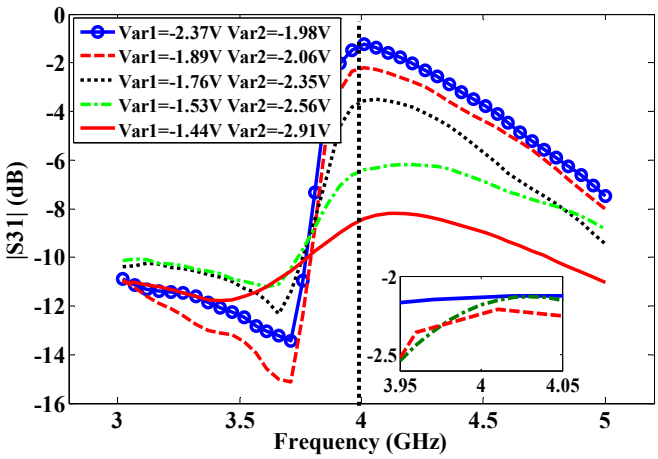


Figure 4.8 Tuning the coupling coefficients at f_o=4GHz with different bias voltage V_{ar1} and V_{ar2}. The blue straight line in inset represents theoretical result, the green dash-dot line represents simulation result and red dash line represents measurement result.

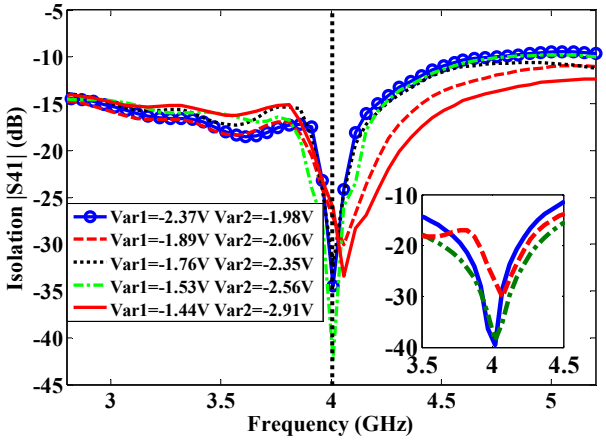


Figure 4.9 Measured isolation $|S_{41}|$ for the coupling coefficients in Fig. 4.8.

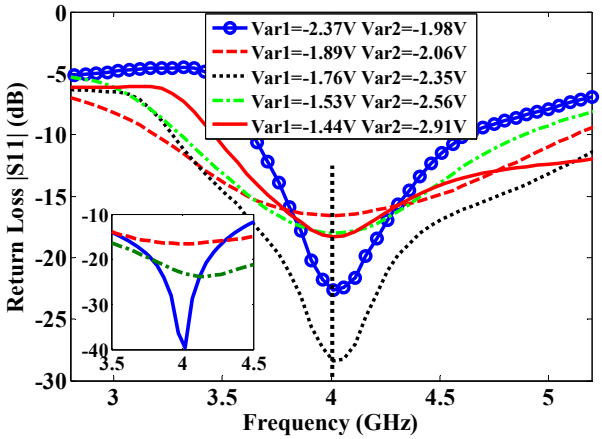


Figure 4.10 Measured return loss for the coupling coefficients in Fig. 4.8.

B. Center Frequency

Fig. 4.11 shows $|S_{21}|$, $|S_{31}|$ versus frequency for different center frequencies. The cross point values of $|S_{21}|$ and $|S_{31}|$ are shown in Fig. 4.12 [4.23]. And Fig. 4.12 presents the measured insertion loss $|S_{21}|$, $|S_{31}|$ and phase differences $\angle S_{21}$-$\angle S_{31}$ when f_o is tuned from 2GHz to 6GHz for a nominal 3-dB operation. Their magnitudes fluctuate from -3.18dB to -4.33dB. So the worst insertion loss is 1.33dB, and with the phase differences between port2 and port3 from ~88° to ~92°. Thus, the output phase error is less than 2°.

Fig. 4.13 shows the measured isolation under different bias conditions. Fig. 4.14 shows the corresponding return loss, which is maintained greater than 25dB. For the entire frequency tuning-range, the coupler circuit draws a dc current from 12.4mA to 24.5mA, which corresponds to power dissipation from 19.84mW to 39.1mW. From (4.10) and (4.14), if C_1, C_2 and L vary a lot for large bias voltage variations, the center frequency and coupling coefficient for our coupler will change. However, stable coupler operation has been achieved in our measurements in which the voltage tolerance was ~10mV.

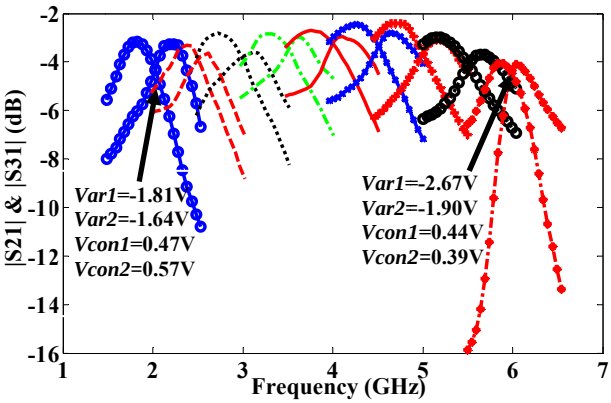


Figure 4.11 Measured magnitude S_{21} and S_{31} versus frequency for different operating frequencies (f_o). The bias voltages for f_o=2GHz and 6GHz are shown in the figure, respectively.

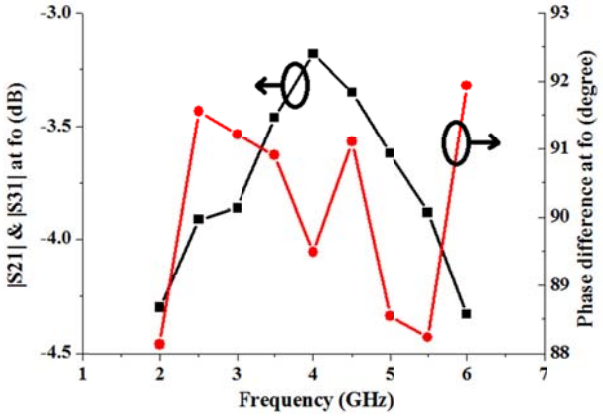


Figure 4.12 Measured S_{21} and S_{31} at different operating frequencies (f_o).

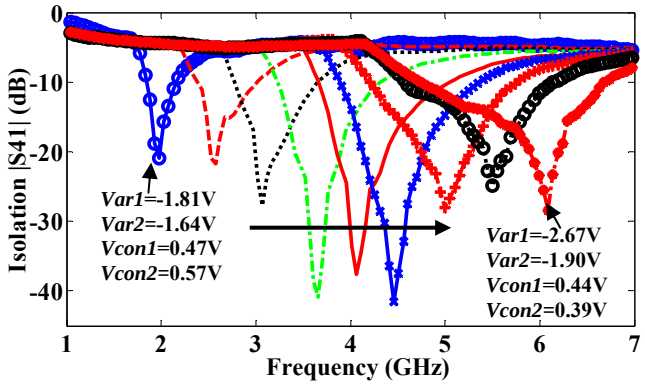


Figure 4.13 Measured isolation $|S_{41}|$ versus frequency for different f_o in Fig. 4.11.

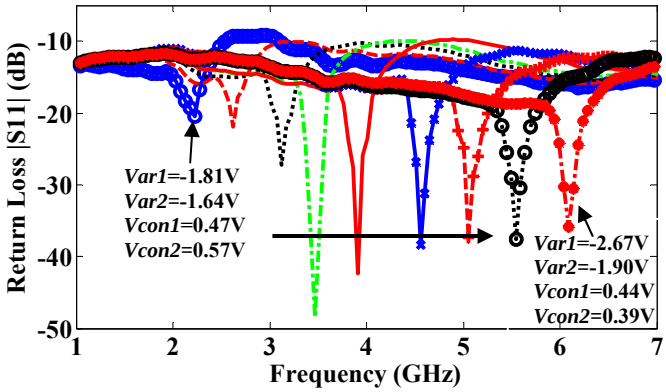


Figure 4.14 Measured return loss $|S_{11}|$ for different f_o in Fig. 4.11.

C. 1-dB Compression Point and Noise

Fig. 4.15 shows $|S_{21}|$ and $|S_{31}|$ at f_o=4GHz versus input power level from -30 dBm to 5 dBm. When ports 3 and 4 terminated 50Ω loads, the 1dB compression point of the coupler is -3.2dBm. Compared with the coupler proposed in [4.18]-[4.19], our coupler has higher 1dB compression point [4.24], due to the use of differential active inductors.

Fig. 4.16 shows all the noise current sources of the proposed coupler. The noise contribution of varactors C_1 and C_2 are modeled by a shunt noise current source i_{nc1} and i_{nc2x}, respectively [4.25], where x is the port number. We have

$$\overline{i_{nc}^2} = 4kT\gamma g_{d0} \tag{4.20}$$

where k is the Boltzmann constant, T is temperature, γ is the channel noise factor, and g_{d0} is the drain-source conductance at zero V_{DS}.

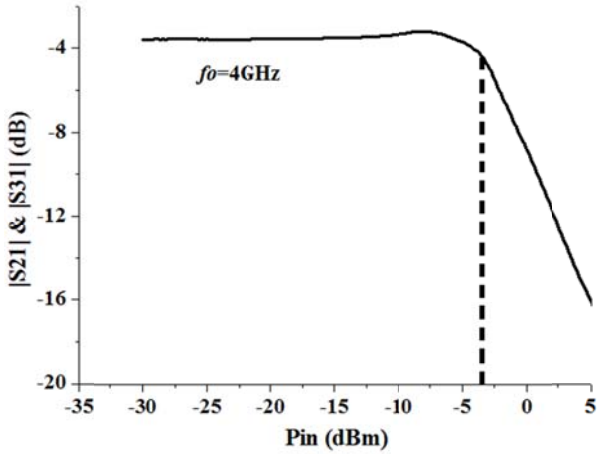


Figure 4.15 Measured $|S_{21}|$ and $|S_{31}|$ with different input power.

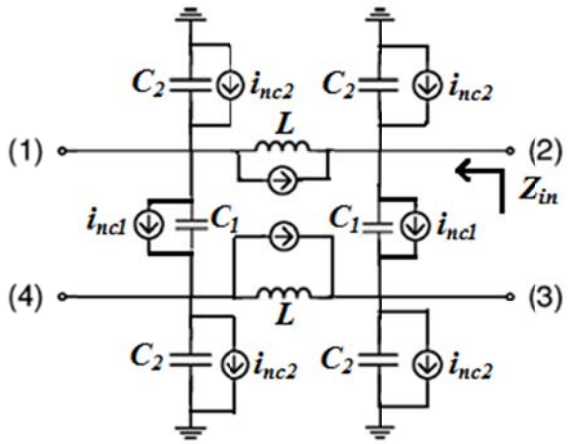


Figure 4.16 Noise current sources for the analysis of the proposed directional coupler.

For the active inductor circuits, the output referred noise voltage and current can be expressed as [4.22]

$$\frac{\overline{V_{L,total}^2}}{\Delta f} = \sum_{i=1}^{6} \left| \frac{N_{ngi}}{\left(M_{ngi} + (\frac{1}{R_{s1}} + sL_{s1}) \right)} \right|^2 \frac{\overline{I_{ngi}^2}}{\Delta f} + \sum_{i=1}^{6} \left| \frac{N_{ngi}}{\left(M_{ndi} + (\frac{1}{R_{s1}} + sL_{s1}) \right)} \right|^2 \frac{\overline{I_{ndi}^2}}{\Delta f} \tag{4.21}$$

$$\frac{\overline{I_{L,total}^2}}{\Delta f} = \frac{\overline{V_{L,total}^2}}{\Delta f (R_{s1}^2 + L_{s1}^2)} \tag{4.22}$$

To obtain the output referred noise of the proposed coupler for port 2 and port 3, we first calculate the impedance at each port. The impedance is a parallel combination of Z_o and the input impedance Z_{in} of the port. Based on even and odd mode half circuit analysis, Z_{in} at port 2 can be expressed as [4.26]

$$Z_{in} = \frac{V_2}{I_2} = \frac{V_2^e + V_2^o}{I_2^e + I_2^o} \tag{4.23}$$

where V_2^e and V_2^o are the even and odd mode voltage at port 2, respectively, and I_2^e and I_2^o are the currents through port 2. Then, the output noise voltage at port 2 is

$$\overline{V_{n2}^2(\omega)} = \frac{\left[Z_o // Z_{in}(w) \right]^2}{2} \times [\overline{i_{nc1}^2(\omega)} + \overline{i_{nc21}^2(\omega)} + 2\overline{i_{nc22}^2(\omega)} + \overline{i_{nc24}^2(\omega)} + 2\overline{I_{total}^2(\omega)}] \tag{4.24}$$

Fig. 4.17 shows the measured and simulated output noise voltages when f_o is 4GHz. Simulation results agree reasonably well with that from (4.24). The measurements, conducted with a spectrum analyzer with FS-noise software, yield slightly higher noise voltages. This discrepancy is likely due to the effects of the contact pads and repeatability of probe-pad contacts, since multiple probe-tip-pads contacts are needed for the measurements. Fig. 4.18 shows measured output noise at port 2 for different f_o. Compared with the coupler in [4.19], our coupler has less output noise (less than 4.0 *nV/√Hz*).

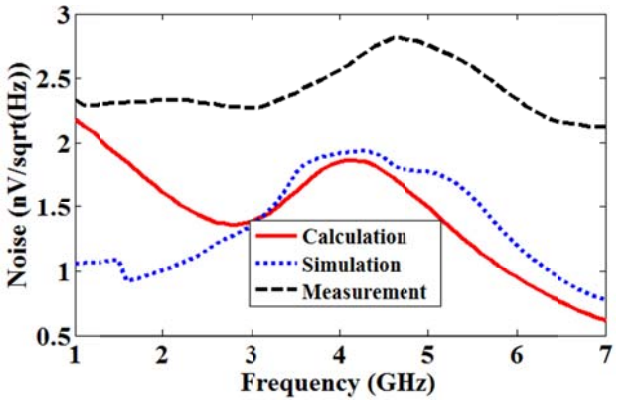


Figure 4.17 Calculated, simulated and measured output noise voltages at port 2.

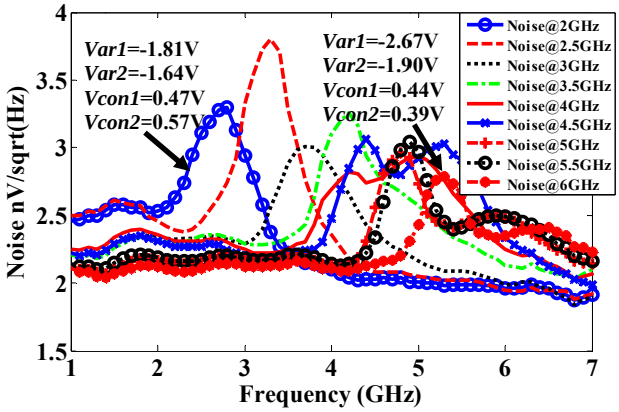


Figure 4.18 Measured noise for different f_o. As center frequency changes, the peak of output noise shifts from 2GHz to 6GHz.

To further characterize its noise performance, we measured the noise figure (*NF*) of the coupler with the reference to [4.27]. An attenuator (30dB attenuation) and a preamplifier (B&Z BZP114UB with 33dB gain) are used to overcome the *NF* measurement difficulty [4.18]. The 30dB attenuator guarantees that the input power of the coupler, the pre-amplifier and the network analyzer is 10dB below their 1dB compression point. After power calibration and noise figure calibration, ZVA50 vector network analyzer is used to measure the noise figure. The obtained *NF* is shown in Fig.

4.19. Also shown is the *NF* obtained with a Y-factor method, which is extracted from the following equation [4.28]-[4.29]

$$F = \frac{N + kT_o G_s}{kT_o G_s} \tag{4.25}$$

where F is the noise figure, N is the added noise of the whole system, G_s is the power gain. The obtained *NF* from these two measurements agrees with each other reasonably. Fig. 4.20 shows measured output noise figure at port 2 at different center frequencies. The obtained *NF* is large. Simulation analysis shows that the active inductors are the main noise source. Nevertheless, low noise amplifiers [4.30] can be used to suppress noise [4.31]-[4.33] for applications. Simple amplifiers [4.34] could also be used in conjunction with the coupler. Compared with using LNAs, total chip areas are smaller, but with higher noise figure.

Table 4.2 summaries the performance of the coupler in this work and compares with other published couplers. A few observations can be made. First, our coupler has a frequency tuning range that is a few times wider than previously published CMOS couplers. The tuning range is comparable with the coupler in [4.15], which has a fixed coupling coefficient. The coupler in [4.15] reported the widest frequency tuning range so far, but occupies much larger area. Second, compared with other CMOS couplers, our coupler has much wider coupling coefficient tuning range. Third, compared with the coupler in [4.19] our coupler occupies 1/4 of the area and consumes ~1/10 of the power. At the same time, our coupler has higher 1-dB compression point and less noise.

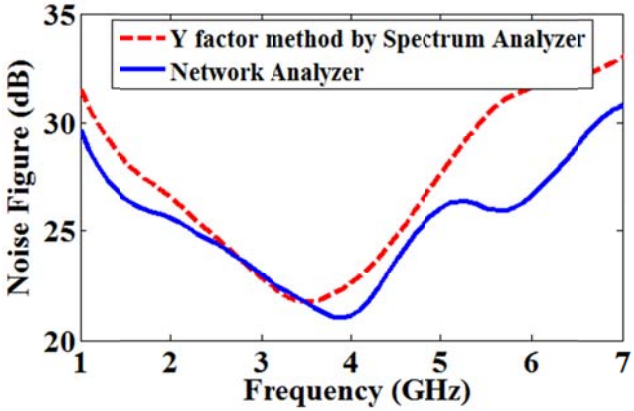


Figure 4.19 Noise figure measured by a Y-factor method and a network analyzer for f_o=4GHz, respectively.

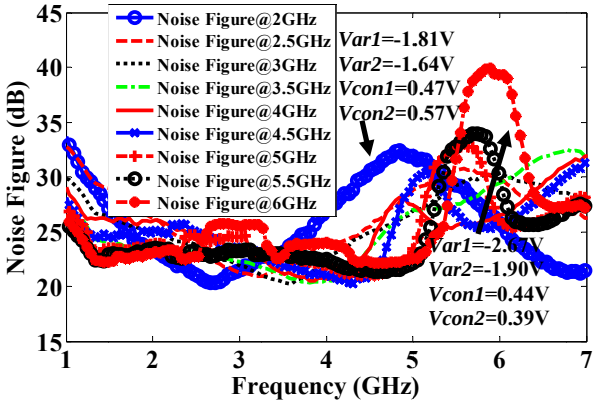


Figure 4.20 Measured noise figure for different operating center frequencies.

TABLE 4.2

COUPLERS WITH COUPLING COEFFICIENTS AND TUNABLE CENTER FREQUENCIES

Specification	[4.15]	[4.18]	[4.19]	This work
Technology	Lumped	0.18µm CMOS	0.13µm CMOS	0.13µm CMOS
Freq. tuning range	1.5 to 7.0GHz	3.2 to 4.7GHz	2.1 to 3.1GHz	2.0 to 6.0GHz
Coupling Coefficient	Fixed 3dB	Fixed 3dB	Tunable 1.4 to 7.1dB	Tunable 1.3 to 9.0dB
Return loss	>10dB	21 to 28dB	15.8 to 43dB	25 to 42dB
Isolation	>10dB	14 to 18dB	34 to 50dB	20.53 to 48.43dB
Insertion loss	0.15dB	0.2 to 0.4dB	0.3 to 1.4dB	0.18 to 1.33dB
Max bias voltage	9.6V	1.8V	2.0V	3.0V

Power dissipation	-	17.6 to 24.6mW	132 to 316mW	19.84 to 39.1mW
Size	7mm×10mm	400×200 μm	730×600 μm	350×340 μm
1dB compression point	-	-16dBm	-4.16dBm	-3.2dBm

4.1.3 Conclusions

A highly reconfigurable, low-power, and compact directional coupler is proposed, analyzed and implemented in a 0.13μm CMOS process. Varactors and novel active inductors are used as the tuning components. The operating center frequency of the coupler is tunable from 2.0GHz to 6.0GHz with return loss better than 15dB and isolation better than 32dB. The coupling coefficient can be tuned independently from 1.3dB to 9.0dB. The measured 1-dB compression point is -3.2dBm. These parameters are much better than previously published couplers. This coupler consumes 40mW or less power, which is much lower than that of similar couplers.

4.2 A Broadband and Highly Reconfigurable CMOS Six-port Circuit

Many microwave applications need to measure the reflection coefficient of a device-under-test (DUT) over a specified frequency range. Vector network analyzers (VNA) are often used to perform this task. Nevertheless, their excellent performance is offset by high cost and bulky size.

In [4.35], Engen proposed a six-port reflectometer as an alternative to the conventional network analyzer for the first time. The six-port, shown in Fig. 4.21, is used to measure the complex reflection coefficient of a DUT by using four power readings and

mathematical calculations of the power data [4.36]. Compared with the heterodyne network analyzer, the six-port circuit is simpler and less expensive. Besides regarding the six-port as a reflectometer, it can be used for other applications, such as receiver for communications, determining material permittivity, wireless sensing, and precise phase measurements for radar [4.37].

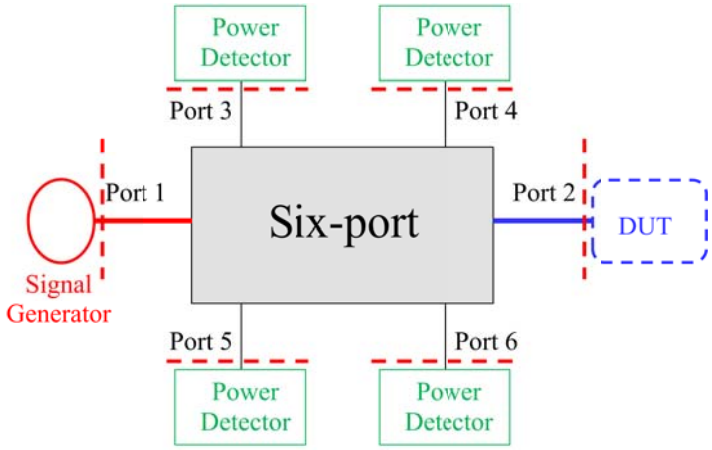


Figure 4.21 A six-port network. The red dashed lines are the reference planes for calibration and measurement.

Most of six-port structures are based on transmission lines [4.38]-[4.39]. However, the frequency performance of these circuits is limited. A solution is to consider a resistive structure [4.40]. This circuit can provide larger bandwidth, but introduces considerable losses. In order to overcome these limitations, a broadband CMOS six-port circuit is proposed, which can be used for biological and chemical sensing in frequency domain through microwave dielectric spectroscopy. This six-port circuit is based on four proposed directional couplers (section 4.1) which can operate as 3-dB quadrature hybrids from 2 GHz to 6 GHz.

The basic configuration of the proposed six-port circuit is shown in Fig. 4.22. The measurement is performing by measuring the powers at four ports (P_3, P_4, P_5, and P_6). The power P_i can be expressed as

$$P_i = |K_i|^2 |b_2|^2 |\Gamma_L - q_i|^2, i = 3,5,6 \tag{4.26}$$

where K_i is a coefficient determined by power levels, Γ_L is the reflection coefficient to be measured, and complex q_i is SPR q-point, which determines measurement accuracy. Ideally, the magnitude of q_i should be ~ 1.5; the argument differences between two q-points should be ~120°. For the proposed six-port circuit, when port 4 is considered as the reference, the q points at port 3, port 5 and port 6 are $q_3=2\angle 270°$, $q_5=\sqrt{2}\angle 45°$, and $q_6=\sqrt{2}\angle 135°$, respectively [4.41], which satisfies the six-port design criterion.

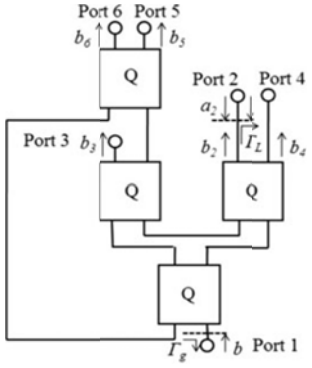


Figure 4.22 The schematic of the proposed six-port circuit [4.41].

The proposed six-port circuit was implemented in a 0.13 μm CMOS process. Fig. 4.23 shows its micrograph. The quadrature in Fig. 4.22 was designed by using lumped elements, as shown in Fig. 4.1, which is discussed in Section 4.1. The operating frequency of the six-port circuit can be tuned by introducing active inductors and varactors into the design of quadrature. When the directional coupler operates as a

quadrature, its operating center frequency can be tuned from 2 GHz to 6 GHz. Therefore, the six-port circuit can also be tuned from 2 GHz to 6 GHz. To demonstrate its tuning range, Cadence is used to simulate our six-port circuit. Powers at different ports (P_3, P_4, P_5, and P_6) can be obtained from simulation analysis. The simulation results shown in Fig. 4.24 indicate that reflection coefficients calculated from powers for 2 GHz and 6 GHz agree with expected ones reasonably well. Thus, the proposed six-port circuit can be integrated on-chip and provide wide operating frequency range.

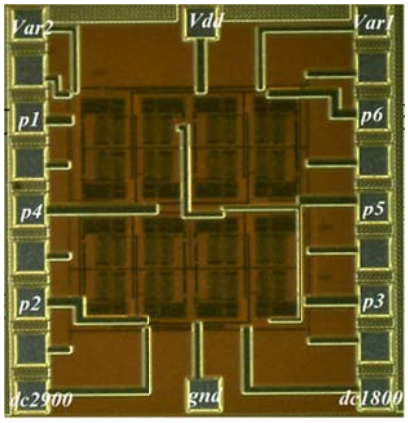
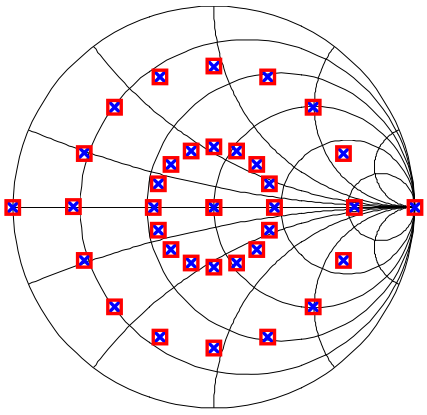
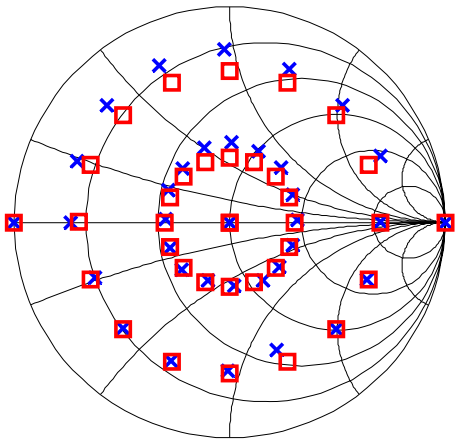


Figure 4.23 The micrograph of the proposed six-port circuit.



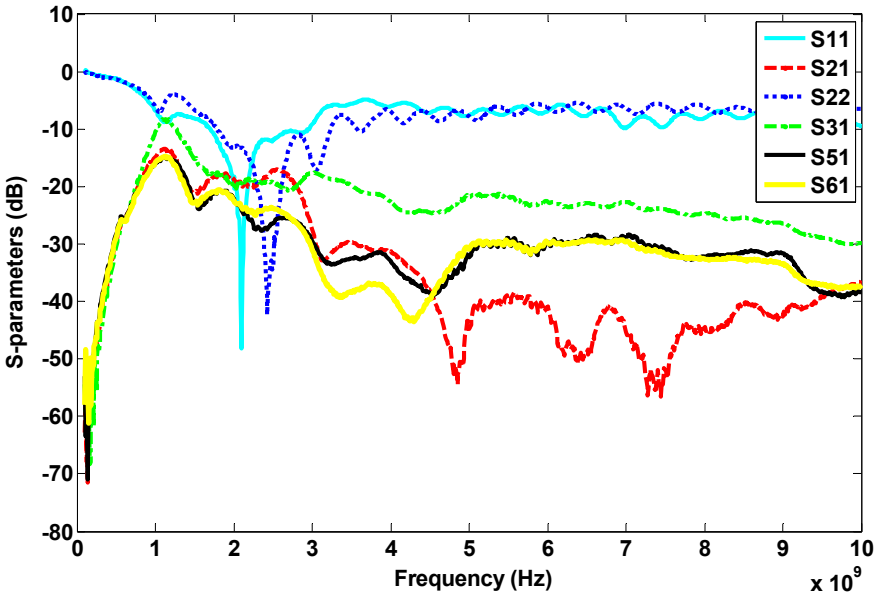
(a)



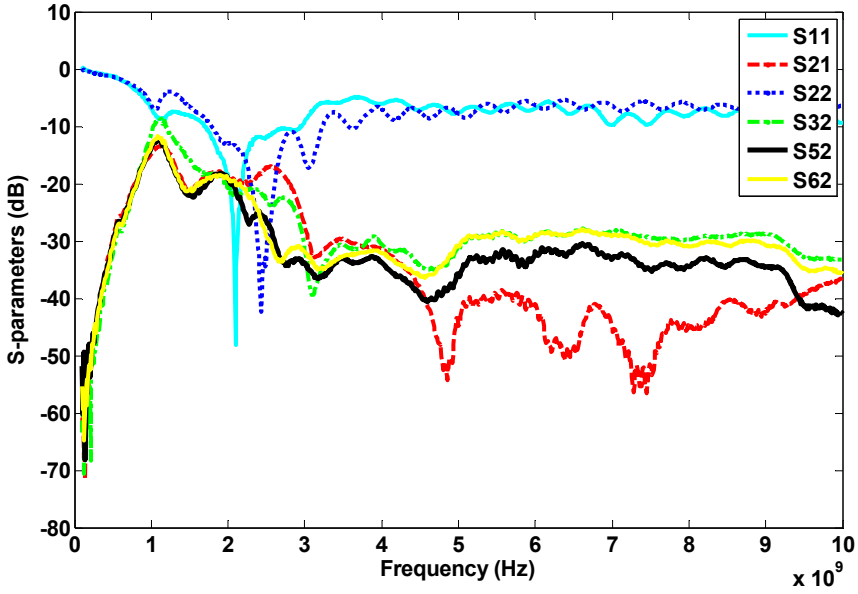
(b)

Figure 4.24 Simulation results of six-port circuit at (a) 2 GHz and (b) 6 GHz.

Fig. 4.25 shows the measured transmission coefficients from port 1 to port i (i=2, 3, 4, 5, 6) and from port 2 to port i (i=3, 5, 6) by ZVA50 vector network analyzer. Compared with the expected transmission coefficients from port 1 to port i (i=2, 3, 4, 5, 6), which are -6 dB for S_{21}, S_{31}, and S_{41}; -9 dB for S_{51} and S_{61}, the worst insertion loss can be up to ~16 dB. Thus, the q-point distribution of the CMOS six-port circuit was seriously affected. Fig. 4.26 shows $|S_{31}|$ and $|S_{61}|$ at 2 GHz versus input power level from -40 to 10 dBm. The 1-dBm compression point of the six port circuit is ~-15 dBm. Based on the non-linearity of the six-port circuit, the maximum input power should be smaller than -15 dBm. Therefore, the powers at port i (i=3, 4, 5, 6) are too small to obtain by Gigatronics 8651A power meters with 80421A power sensors.

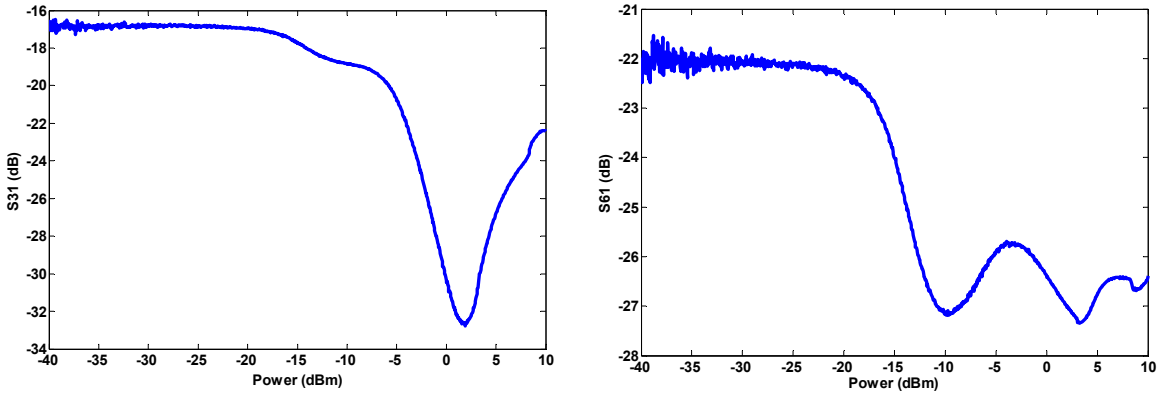


(a)



(b)

Figure 4.25 Measured transmission coefficients from (a) port 1 to port i (i=2, 3, 4, 5, 6) (b) port 2 to port i (i=3, 5, 6)



(a) (b)

Figure 4.26 Measured (a)| S_{31}| (b) |S_{61}| with different input power.

The performance of the CMOS six-port circuit was seriously affected by large insertion loss and power measurement limitation. Nonetheless, simulations show that our six-port circuit can be used to measure on-chip scattering parameters and tuned from 2 GHz to 6 GHz. Therefore, future works are needed to reduce the insertion loss and improve input dynamic range and power detection capability. The performance of the tunable and integrated six-port circuit will be demonstrated through measuring dielectric changes of water and other chemical agents.

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CHAPTER FIVE

A SPATIAL SAMPLING BASED 13.3 Gs/s SAMPLE-AND-HOLD CIRCUIT

This chapter presents a high-speed sample-and-hold circuit (SHC) for very fast signal analysis. Spatial sampling techniques are exploited with CMOS transmission lines (TLs) in a 0.13 μm standard CMOS process. The SHC includes on chip coplanar waveguides (CPW) for signal and clock pulse transmission, a clock pulse generator, and three elementary samplers periodically (L=7.2 mm) placed along the signal propagation line. The SHC samples at 13.3 Gs/s. The circuit occupies an area of 1660 μm×820 μm and consumes ~6 mW at a supply voltage of 1.2 V. The obtained input bandwidth is ~11.5 GHz.

5.1 Introduction

Many experimental domains, such as high-power microwaves (HPM) lasers, optics, pulsed range radars, and ultra-wide-band (UWB) communications, often need to measure very short pulses in real-time since the pulses are non-repetitive or at a low repetition rate [5.1]-[5.2]. High-speed analog-to-digital converters (ADCs) are critical in these applications [5.3]. But, the performances of such ADCs are often limited by their sampling rate and jitter. Therefore, laser-based digitizers and photonic approaches have been explored to achieve high sampling rates and high time resolutions, such as the 10 Tsample/s real-time digitization [5.4], 100 Gs/s ADCs [5.5], and 15 fs low jitter operations [5.6]. However, these techniques are not compatible with CMOS technologies. ADCs in InP HBT technologies [5.7] and SiGe BiCMOS processes [5.8] can achieve

sampling rates up to 40Gs/s. But it is difficult for these ADCs to capture single short pulses. The processes are also more expensive than standard CMOS processes. Time-interleaving strategies (6-bit 16 Gs/s ADC in Ref. [5.9], 40 Gs/s ADC in Ref. [5.10]) and flash ADC technologies (6 bit 25 Gs/s flash interpolating ADC in Ref. [5.11]) are effective approaches to develop high-speed and high-resolution CMOS ADCs. However, the clock distribution networks consume significant power and pose design challenges to meet the stringent clock skew requirements. Meanwhile, clock jitter becomes a major factor limiting the progress of such ADCs for higher sampling rates and resolutions. Hence, exploring new approaches that can further reduce jitter is necessary. Since high-speed sample-and-hold circuits (SHCs) are commonly the first stage and the key for high performance ADCs, therefore, developing high-speed CMOS SHCs is of great interest.

In this work, we propose a spatial-sampling based CMOS SHC. Previously, such spatial sampling techniques have been explored with InP and GaAs MMIC technologies [5.12]-[5.13]. Our SHC exploits on-chip transmission lines (TL) to capture and store single short signal pulses as well as clock pulses. Only one clock pulse is needed to obtain multiple sampling points. Thus, the clock jitter issues are significantly alleviated, since the passive clock distribution transmission line does not induce jitters. This chapter is arranged as the following: section 5.2 presents the design topology of our CMOS SHC; section 5.3 gives the circuit measurement results; section 5.4 is the conclusions.

5.2 A CMOS SHC Based on Spatial Sampling Techniques

The basic idea of our CMOS SHC is to use spatial sampling, shown in Fig. 5.1, to achieve high sampling rate. It has three main parts: on-chip transmission lines for signal and clock transmission, a clock signal generator, and elementary samplers. Each elementary sampler has a sampling switch (M), a charge holding capacitor (C_H), and a charge amplifier. The SHC consists of a multiplicity of elementary samplers spatially distributed along a transmission line. Each sampler captures and stores signal information at its spatial position.

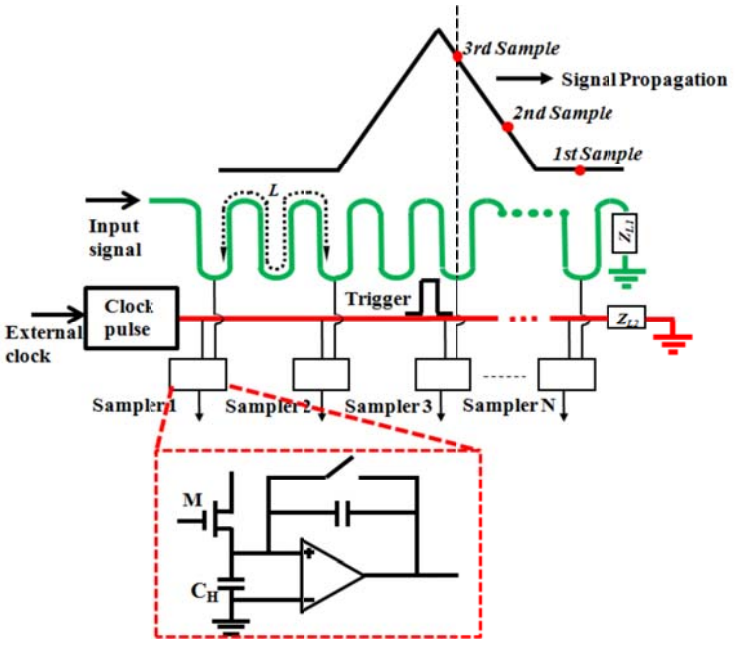


Fig. 5.1 A CMOS sample-and-hold circuit based on spatial sampling.

5.2.1 Periodically Loaded On-chip Transmission Lines

Two coplanar waveguides (CPW) are used in the circuit in Fig. 5.1, a meandered line for signal propagation and a straight-line for clock pulse propagation. We have demonstrated that on-chip CPW meander lines can be modeled as straight CPW lines

with signal propagation constants, $\gamma_0 = \alpha_0 + j\beta_0$, and characteristic impedance Z_0. The periodic loading of elementary samplers further changes signal propagation constant to $\gamma = \alpha + j\beta$. The constant γ and its frequency dependence can be obtained by considering a unit cell that is repeated N-times in Fig. 5.1. The ABCD matrix of the unit cell is [5.14]

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh(\gamma_0 l) + \frac{j}{2} Zb \sinh(\gamma_0 l) & Z \sinh(\gamma_0 l) + \frac{jbZ^2}{2}(\cosh(\gamma_0 l) - 1) \\ Z^{-1} \sinh(\gamma_0 l) + \frac{jb}{2}(\cosh(\gamma_0 l) + 1) & \cosh(\gamma_0 l) + \frac{j}{2} Zb \sinh(\gamma_0 l) \end{bmatrix}, \tag{5.1}$$

where b is the load from the elementary sampler, which can be modeled as a series of the channel resistance, R_d, of M and the capacitor C_H. Equation (5.1) shows that the ABCD matrix of the unit cell is equal to the product of the ABCD matrices representing the CPW lines with $L/2$ length and the shunt load from the elementary sampler. This ABCD matrix is a characteristic of the unit cell, which relates the frequency-dependent input voltage and current of the unit cell to the output voltage and current. The ABCD matrix of the unit cell is then converted to its scattering parameter matrix, and its transfer function can be derived. The inverse Fourier transform of the obtained transfer function gives signal transmission on these loaded CPW lines. Figure 5.2 shows the propagation of a narrow pulse on such a loaded CPW line when the line period L is 7.2 mm, C_H is 451 fF, and R_d=3.5 Ω, which are the same as the values in Fig. 5.6 in Section 5.3. The CPW line is a standard device component in advanced CMOS technologies, which has broader operating frequency range with less loss and dispersion. Figure 5.2 indicates that the pulse is attenuated and deformed. As a result, the number of elementary samplers for the SHC in Fig. 5.1 will be reduced. The clock signal pulse in Fig. 5.1 is deformed, which

causes an increase of the rise and fall times. Thus, the resolution of the SHC will be decreased.

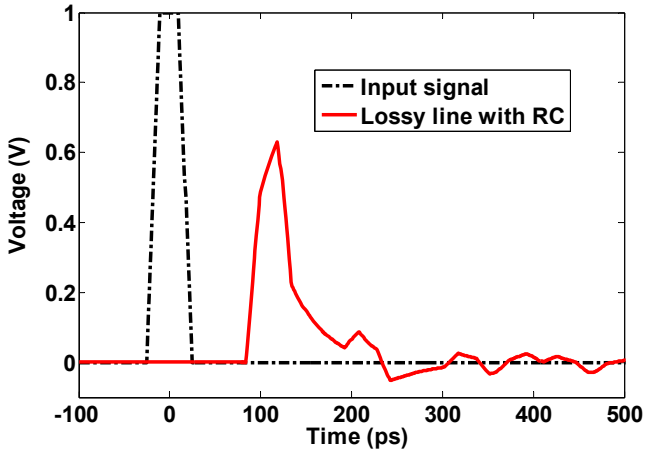


Fig. 5.2 The transmission of a narrow pulse on CPW lines.

5.2.2 On-chip Clock Signal Generation Circuit

Figure 5.3 shows the schematic of the clock pulse generator used in the SHC. This generator can convert an external trigger pulse with slow edges to a typical clock pulse signal with ~50 ps full-width-at-half-maximum (FWHM) [5.14] in a standard 0.13 μm CMOS technology. The main block in this generator is the CMOS NAND gate fed by the input signal and its delayed inverse, which is used to generate a short pulse with a duration determined by the propagation delay of the inverter. A chain of three inverters is used to shape the rise and fall times of the short pulses to drive the sampling MOSFET switch. Narrow clock pulse signal can help avoid interference from reflected waves at adjacent elementary samplers. Furthermore, it is useful to minimize the nonlinear components of the sampled signal.

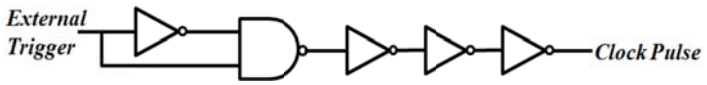


Fig. 5.3 On-chip clock pulse generator.

5.2.3 Elementary Sampler

NFETs (*M*) are used in Fig. 5.1 as sampling switches. The bandwidth of the elementary sampler is determined by its ON resistance, R_d, and the signal transmission line characteristic impedance. The 3-dB bandwidth can be approximated as [5.14]

$$f_{-3,dB} = \frac{1}{2\pi(R_d + Z_0/2)C_H}. \tag{5.2}$$

Figure 5.4 shows the charge amplifier with the sampling switch and the operational transconductance amplifier (OTA). The charge stored in the holding capacitor C_H determines the charge amplifier output. Increasing OTA g_m and minimizing parasitic capacitance at the output of charge amplifier is useful to improve the signal to distortion ratio (SDR) of the circuit. The configuration of the OTA in this charge amplifier is a cascade topology in series with a common source amplifier. Figure 5.5 (a) shows the clock signal ϕ generation circuit. Initially, when the transmission gate switch is closed, the charge amplifier is in reset mode. Before the arrival of the clock pulse signal ϕ controlled by signal set_in and clk_in, the charge amplifier switches to the amplification mode by opening the transmission gate switch. Figure 5.5 (b) shows the timing sequence relationship among signal set_in, clk_in, and clock signal ϕ. Assuming that the injected charge on C_H is Q_{in}, the amplifier output can be approximately expressed as [5.14]

$$V_{out} \approx -\frac{Q_{in}}{C_f}, \tag{5.3}$$

where C_f is feedback capacitor.

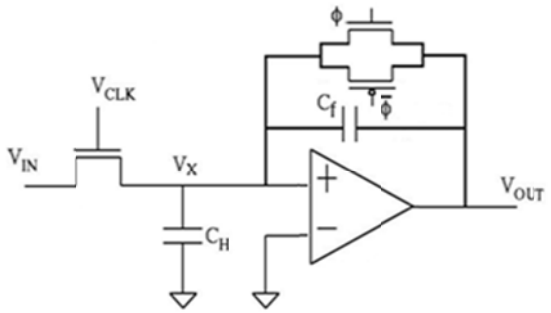


Fig. 5.4 The schematic of charge amplifier circuit.

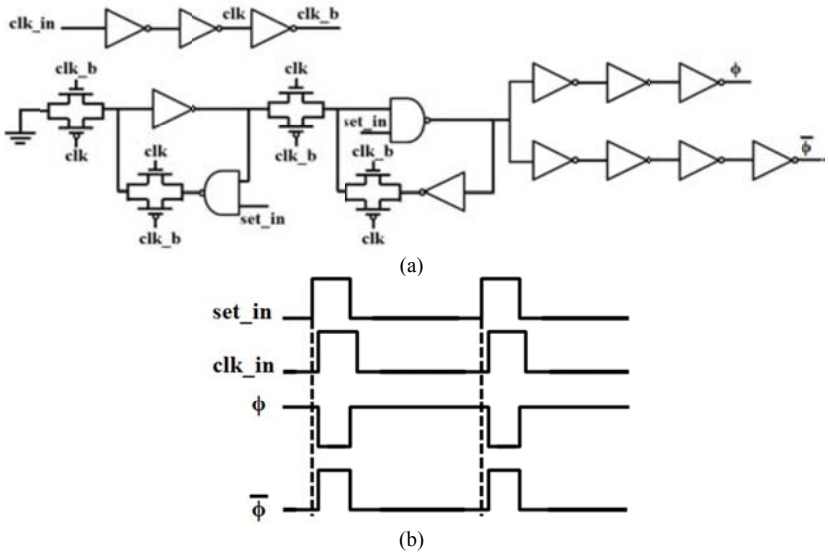


Fig. 5.5 Clock signal ϕ generation circuit (a) schematic (b) timing sequence when the charge amplifier in amplification mode.

5.3 CMOS Sample-and-Hold Circuit Implementation and Measurement Results

Figure 5.6 shows the micrograph of the proposed high-speed SHC. Only three channels with a projected 3 dB bandwidth of 12.6 GHz are considered in this design due

to chip size and measurement restrictions. As a result, for each simulation, only three readings from the three sampling channels can be obtained. Thus, we need to perform multiple simulations with different initial delay of the input signal to obtain sufficient data for analysis.

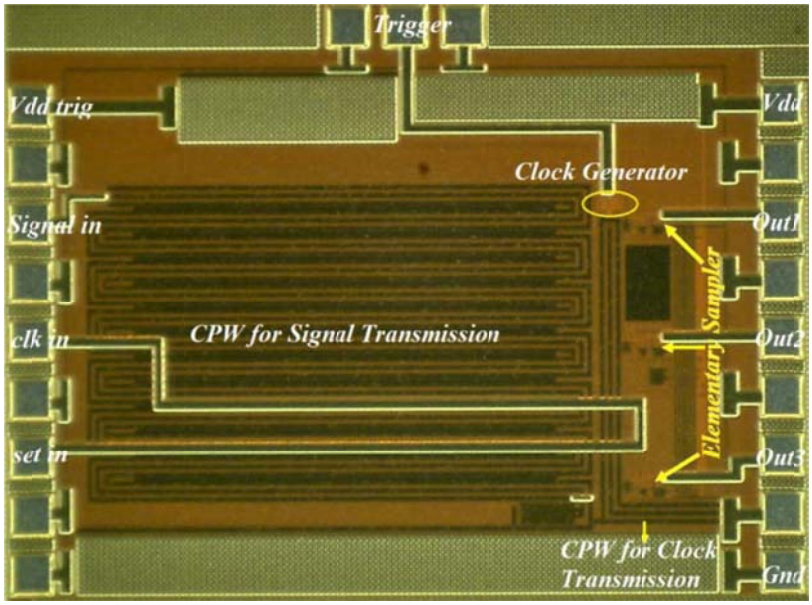


Fig. 5.6 The micrograph of the proposed high-speed SHC.

Firstly, a step waveform with 200 ps rise time, shown in Fig. 5.7, is used as the input signal. The obtained charge amplifier outputs are plotted in Fig. 5.7. It shows the SHC circuit can capture the signal with very fast edges. Secondly, a single pulse signal of 100 mV magnitude with 100 ps duration, shown in Fig. 5.8 (a), is used as input signal. The SHC outputs are plotted in Fig. 5.8 (b). It indicates our SHC circuit is capable of capturing the narrow single pulse. Note the step waveform polarity in Fig. 5.7 and the pulse polarity in Fig. 5.8 are opposite to that of the inputs. This is due to 180° phase shift of the charge amplifier.

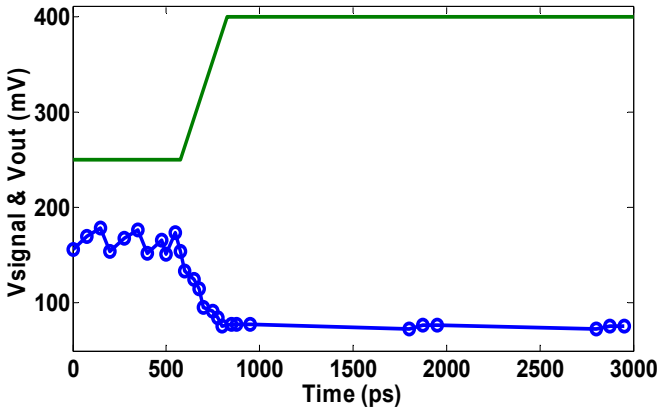
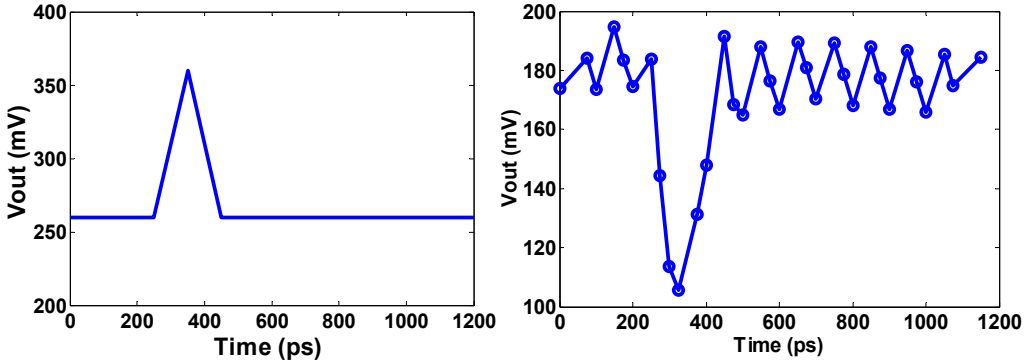


Fig. 5.7 SHC outputs with a step waveform with 200 ps rise time.



(a) (b)

Fig. 5.8 SHC with a single pulse (a) Input pulse (b) Simulated output pulse.

In addition to the pulsed signals, a 10 GHz sinusoidal signal with a peak-to-peak voltage of 100 mV is also used as the input. The initial delay of the sinusoidal signal is varied from 0 to 100 ps in 512 steps. The FFT plot of the 512 sampled voltages from the second sampling channel is shown in Fig. 5.9. Based on the FFT results, dynamic performance parameters of the three sampling channels are summarized in Table. 5.1. It indicates that the *SNR* values of the three channels are decreasing from channel 1 to channel 3. This is because the magnitude of the input signal is attenuated along the

meandered transmission line. Also, the *SDNR*, *SFDR*, and *THD* of the first channel are smaller than those of the other two channels. This is because the nonlinear effects are more severe in the first sampling channel due to larger input magnitude.

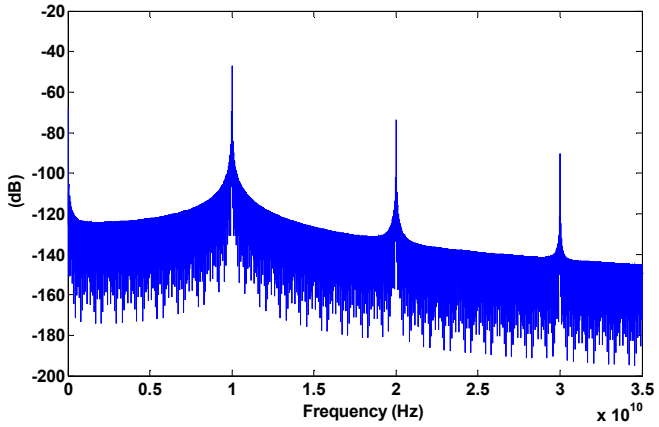


Fig. 5.9 The FFT plot for the second sampling channel

TABLE 5.1 Dynamic performance parameters of three sampling channels

	Output 1	Output 2	Output 3
SNR (dB)	74.7774	69.7521	53.3121
SDNR (dB)	21.8505	26.4982	23.2769
SFDR (dB)	21.9009	26.7465	23.2999
THD (dB)	-21.8505	-26.5693	-23.2812

The test setup shown in Fig. 5.10 was used to measure the SHC. Measurements were performed on chip by using high frequency multi-contact probes. Time domain measurements were conducted by using a Tektronix DPO7354 digital oscilloscope and a Model 4050B pulse generator from Picosecond Pulse Labs. Frequency domain measurements were evaluated by using the oscilloscope and an Agilent 83712B synthesized CW generator. The signals, generated by a Model 4050B pulse generator, are split into signal set_in, clk_in, and Trigger, respectively, by using power dividers.

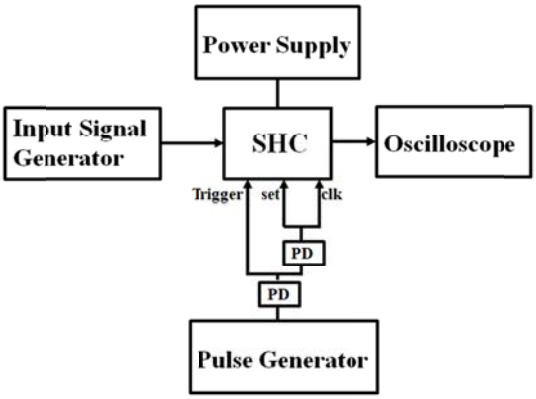
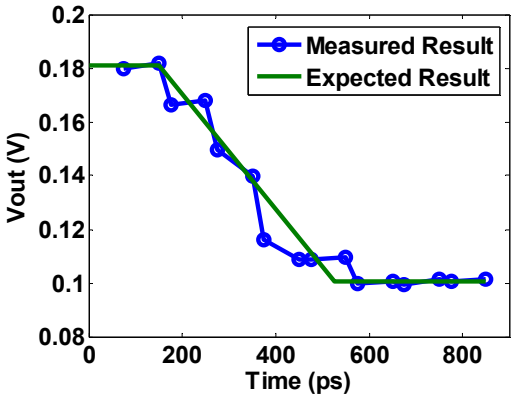


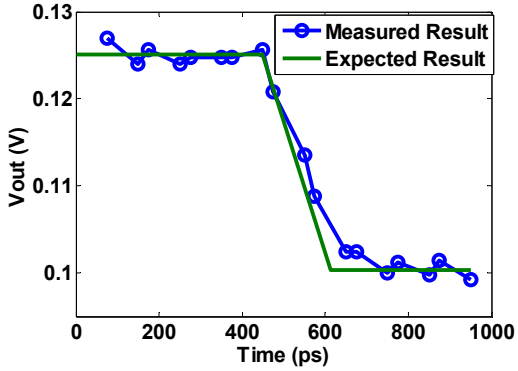
Fig. 5.10 Measurement setup. Component PD represents a power divider.

Figure 5.11 shows the output waveforms for input signals with 350 ps and 130 ps rise time, respectively at 13.3 Gs/s sampling rate. The total current for the sample-and-hold circuit is measured as 4.983 mA with a Keithley 2612 system source meter, where the power supply is 1.2 V. The total power consumption of the circuit, including the on-chip transmission lines, the clock signal generation circuit and the elementary samplers, is ~6 mW. The measurement results show that our SHC is capable of capturing very fast signals. Figure 5.12 (a) shows the input bandwidth of the sample-and-hold circuit obtained from Cadence post layout simulation. The circuit has approximately 12.5 GHz bandwidth, which agrees with the projected 3 dB bandwidth reasonably well. Sine waves generated by a 20 GHz CW generator are used as the input for the SHC. The input bandwidth of the circuit is evaluated with the output amplitude of sampled output signals over various input frequencies measured by the oscilloscope. Figure 5.12 (b) and (c) show the measured normalized amplitude of the sampled signals for the first and second sampling channel. The fundamental output signal component for 11.5 GHz input signal frequency is 3dB smaller than that of a 100 MHz input signal. It indicates that the

measured 3-dB bandwidths for channel one and channel two are larger than 11 GHz. The reason for the fluctuations in the frequency response of the SHC is mainly due to the parasitic inductance of probe-tip-pad contact.

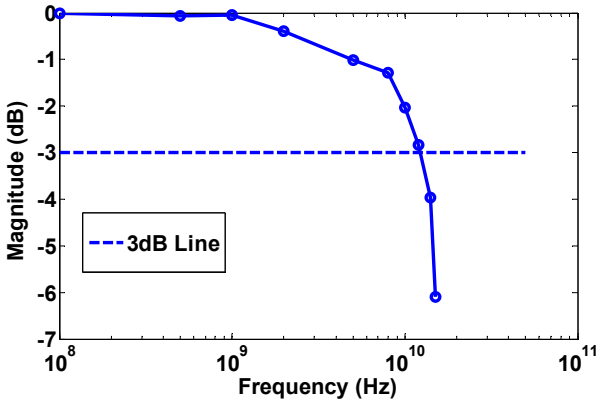


(a)

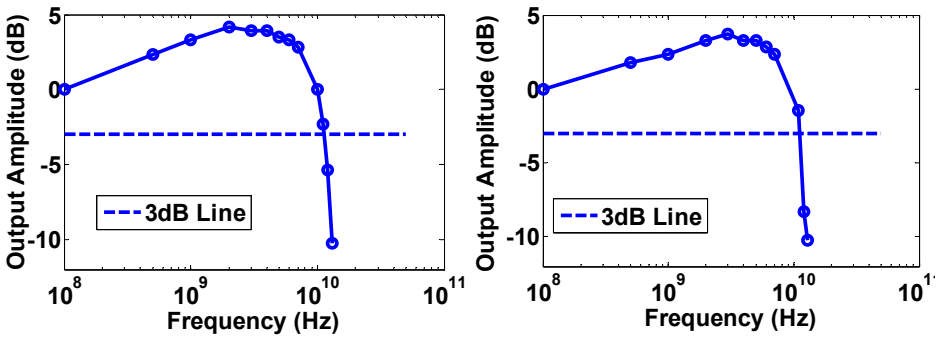


(b)

Fig. 5.11 Measured waveforms for input signals with (a) 350 ps and (b) 130 ps.



(a)



(b) (c)

Fig. 5.12 (a) Simulated input bandwidth of the sample-and-hold circuit (b) Measured output frequency response for channel 1 (c) channel 2.

Table 5.2 summaries the operation features of this circuit and some previously reported circuits. A few observations can be made. First, the input bandwidth for the circuit described in this work is much higher than other reported circuits. Second, the total power consumption is ~ 6 mW from a 1.2 V supply, a 90% improvement over previous designs. Third, the digitizer in Ref. 5.12 has higher sampling rate, but occupies much larger area. At the same time, based on distributed amplifiers periodically loaded on a transmission line, the circuit in Ref. 5.16 has 20 Gs/s sampling rate, higher than our SHC's. Yet, the circuit has larger power consumption and smaller input bandwidth.

TABLE 5.2. SHC circuit performance summary and comparison

Parameters	[5.12]	[5.15]	[5.16]	This work
Sampling Frequency	20 Gs/s	6.4 Gs/s	20 Gs/s	13.3 Gs/s
Input Bandwidth @ -3dB	8 GHz	> 6 GHz	1.8 GHz	11.5 GHz
Power Consumption		470 mW	71 mW	6 mW
Voltage Supply		5.1 V	1.2 V	1.2 V
Technology	0.18 µm GaAs PHEMT	0.25 µm SiGe BiCMOS	0.13 µm CMOS	0.13 µm CMOS
Chip Area	3×4 mm^2	1.1 mm^2	0.09 mm^2	1.36 mm^2

5.4 Conclusions

This paper presents a spatial-sampling-based sample-and-hold circuit for low voltage, low power, and high-speed operations. The circuit is implemented in a commercial 0.13 μm CMOS technology, with 13.3 Gs/s sampling rate and ~11.5 GHz input bandwidth. The power consumption is ~ 6 mW, which is significantly lower than previous reported multi-gigahertz SHCs. The post-layout simulations and measurements show that the circuit is promising to capture on-chip signals with 100 ps fast edges and is possible to capture very short single pulses with 100 ps duration.

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CHAPTER SIX

BROADBAND HIGH-SENSITIVITY ELECTRON SPIN RESONANCE SPECTROSCOPY

This chapter presents a novel electron spin resonance (ESR) spectroscopy technique, which provides wide frequency tuning capabilities while enables high-sensitivity ESR operations. The use of frequency sweeping eliminates microphonic noise, which is an inherent challenge for high-frequency ESR systems. We demonstrate the ESR technique by measuring 60 μg DPPH powder from 1 GHz to 10 GHz at the room temperature. A meandered microstrip line is built and used for the test.

6.1 Introduction

Broadband and multi-frequency electron spin resonance (ESR) spectroscopy, also referred to as electron paramagnetic resonance (EPR) spectroscopy, enables many important new applications, including the distinction between field-dependent and field-independent paramagnetic resonance processes, the study of frequency-dependent linewidth, and the differentiation between the spectra of different paramagnetic species [6.1]. Therefore, a few approaches have been explored to expand the frequency coverage capabilities of current ESR techniques, which often lead to single frequency operations for an ESR system. Using tunable cavities is a straightforward idea to cover multi-frequencies [6.2]-[6.3], but the ESR sensitivity is limited due to small filling factors and the degradation of cavity quality-factors when lossy materials are tested. Non-resonant

structures are broadband and can handle high filling factors [6.4]-[6.5], yet, the ESR sensitivity is compromised due to the absence of frequency-selectivity (e.g. 5 mg of DPPH is used in [6.5]). So are the superconducting coplanar waveguides (CPW) that were recently used for non-conventional ESR studies from 0.5 to 40 GHz at 1.4 K [6.6]. Thus, it is of great interest to develop new techniques that address the frequency tuning and sensitivity challenges.

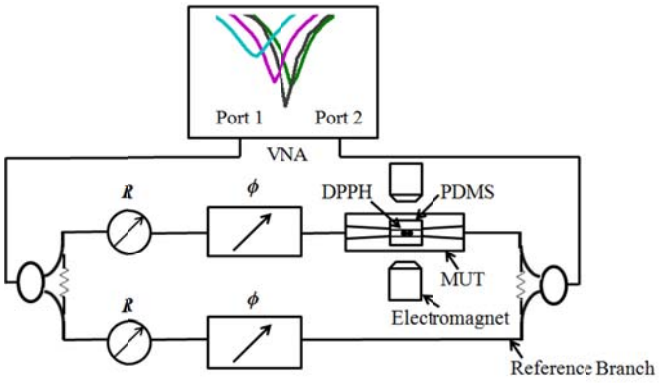
The use of narrow-band resonant cavities in conventional ESR techniques also requires field-modulation and field sweeping. As a result, it is challenging to use these ESR systems to investigate effects and processes that depend on magnetic field history as well as to detect small zero-field gaps in nanometer-size magnetic systems [6.5]. Additionally, modulating magnetic field induces microphonic noise [6.7]-[6.9], which becomes a very difficult issue at high-frequencies (e.g. at terahertz). Hence, exploring new approaches that can avoid field modulations is also of great interest.

Recently, an interference based radio-frequency (RF) device is proposed to achieve high sensitivity operations while covering a very wide frequency range [6.10]. In this work, we further develop the RF technique to address the ESR challenges mentioned above. The design considerations of our ESR system are given in Section 6.2. Section 6.3 presents our ESR measurement results with DPPH powders. Section 6.4 concludes the chapter.

6.2 ESR System Design Considerations

Fig. 6.1 (a) is the schematic of the proposed ESR system. It consists of a vector network analyzer (VNA), broadband Wilkinson power dividers, tunable phase shifters (ϕ)

and attenuators (*R*). Its basic operating principles, in terms of high-sensitivity measurement and frequency tuning, are similar to those of the dielectric spectroscopy systems as described in [6.10]. A main difference is the application of an external DC magnetic field, which is generated by an electromagnet (Model # 3470 from GMC).



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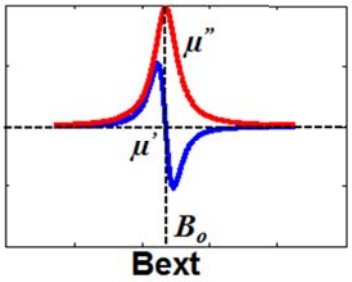
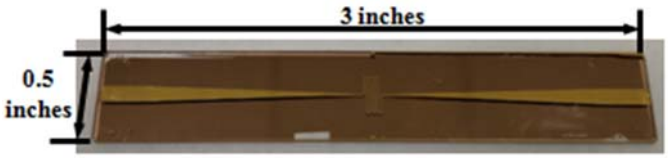


(b)

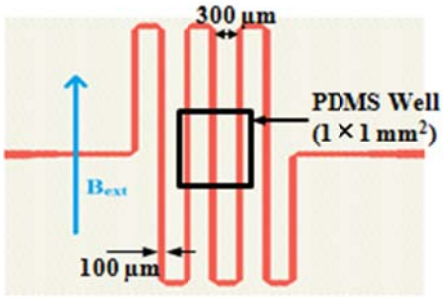
Fig. 6.1 (a) The schematic of the interference based ESR system. (b) Permeability real and imaginary parts versus external magnetic field.

A microstrip line, shown in Fig. 6.2 (a), is used to generate RF magnetic fields and transmit ESR signals from DPPH powders. The powders are placed in a polydimethylsiloxane (PDMS) well, which is attached to the microstrip line as shown in Fig. 6.2 (b). The meandered section at the center of the microstrip line is designed for

stronger ESR interactions since RF and DC magnetic fields need to be orthogonal, as illustrated in Fig. 6.2 (b). The microstrip line is built on a 1 mm thick fused silica substrate with conventional micro-fabrication procedures. Standard lift-off processes are used to deposit ~ 500 nm thick gold thin films on a ~ 10 nm titanium adhesion layer.



(a)



(b)

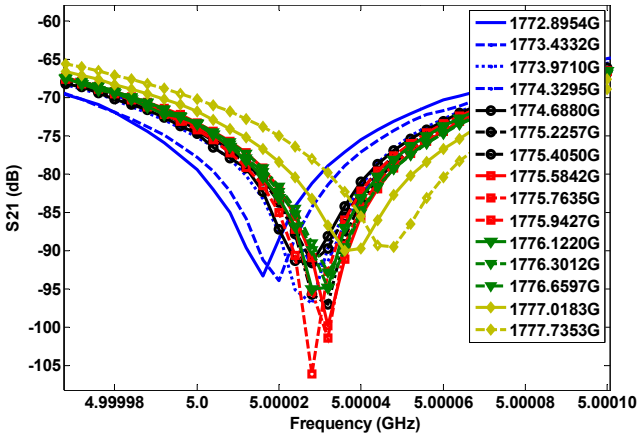
Fig. 6.2 (a) A photo of a meandered microstrip line. (b) Layout of the meandered microstrip line at the sensing zone.

Unlike conventional ESR systems, the proposed technique in Fig. 6.1 sweeps RF frequencies while keeping DC field constant. The transmission coefficient S_{21} is obtained. Then the DC field is tuned to a new value and the frequency sweep process is repeated. As a result, ESR signals are obtained and microphonic noise is avoided. From Fig. 6.2 (c), $|S_{21}|$ magnitude changes are caused by μ'' and frequency shifts are mainly caused by μ'. The spin resonance frequency, $f_s=g\mu_B B_{ext}/h$, depends on g factor, atomic unit of the magnetic moment μ_B, Planck constant h, and external magnetic field. Since the effective

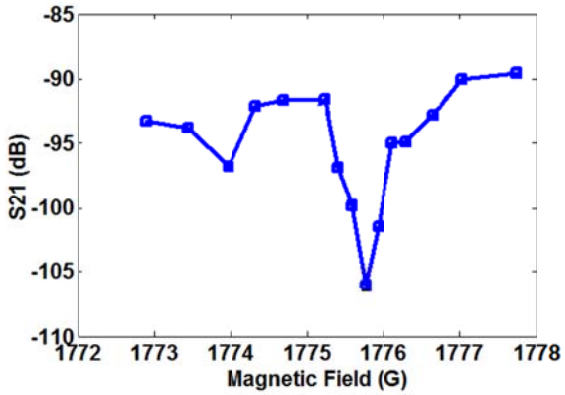
quality factor Q_{eff}, defined as $Q_{eff}=f_o/\Delta f_{3dB}$, of the system in Fig. 6.1 can be very high, e.g. ~ 3×10^6 in [6.10], therefore, we expect the sharp frequency selectivity can boost ESR sensitivity significantly when compared with the CPW and micro-coil based techniques. The operating frequency tuning range, from ~ 1 GHz to 10 GHz in this work, is determined by the components in Fig. 6.1 (a). If even broader frequency tuning is desired, different frequency bands can be combined as demonstrated from ~ 20 MHz to 40 GHz in [6.10].

6.3 ESR Experiments

To demonstrate the ESR system with high sensitivity and multi-frequency operation at room temperature, 60 μg DPPH powder was placed in the PDMS well at the sensing zone in Fig. 6.1. An RF power of 0 dBm is used in the experiment. We first tune the transmission coefficient $|S_{21}|_{\min}$ to -90 dB ~ -95 dB. Fig. 6.3 (a) shows the measured ESR signals of DPPH at 5 GHz, when the external magnetic field is swept. Fig. 3(b) summarizes $S_{21,min}$ in Fig. 3(a) at different external magnetic fields and Fig. 3(c) summarizes the frequency f_0 of $S_{21,min}$. If μ' and μ'' in Fig. 6.1(b) account for the observed absorption and phase shift, respectively, then Fig. 3(b) resembles the absorption ESR signals obtained in conventional ESR systems where magnetic field modulations are used. Fig. 3 (c) represents dispersion ESR signals from μ', which is different from expected one as shown in Fig. 1 (c). The reason for this difference is still under exploration. Such information is not currently available from conventional ESR techniques. Nevertheless, further work is needed to differentiate the contributions from μ' and μ''.



(a)



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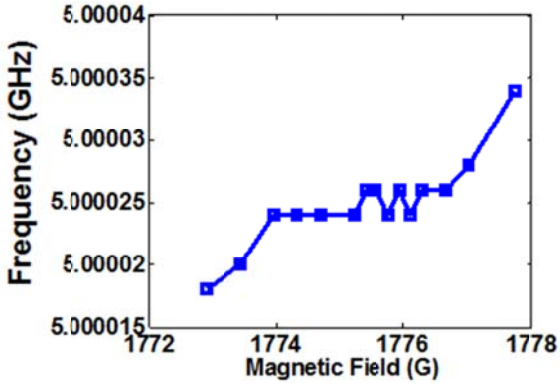

(c)

Fig. 6.3 (a) Measured $|S_{21}|$ changes for external magnetic field-swept ESR at 5 GHz. (b) Summary of minimum $|S_{21}|$ for different external magnetic fields from Fig. 6.3 (a). (c) Frequency of minimum $|S_{21}|$ from Fig. 6.3 (a) versus external magnetic field.

Fig. 6.4 (a) shows the obtained S_{21} at different frequencies. The minimum $|S_{21}|$ as a function of applied external magnetic field is shown in Fig. 6.4 (b). Its slope ($hf_s=g\mu_B B_{ext}$), gives a g-value of g=2.0126 ± 0.0016 for DPPH. This demonstrates the unique capabilities of our ESR approach to obtain accurate g-factors, which could be employed for label-free differention of paramagnetic species. Table 6.1 summaries the measured ESR signal at different resonance frequencies. The average linewidth ΔB=0.232 mT is in agreement with values reported for DPPH.

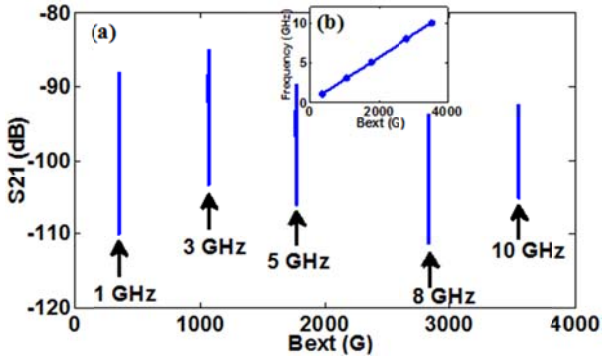

Fig. 6.4. (a) External magnetic field-swept ESR for various frequencies (b) Position of the absorption peak minimum versus magnetic field for all measured spectra shown in Fig. 6.4 (a).

TABLE 6.1 SUMMARY OF DPPH ESR SIGNALS AT DIFFERENT FREQUENCIES

	f_o=1 GHz	**f_o=3 GHz**	**f_o=5 GHz**	**f_o=8 GHz**	**f_o=10 GHz**
Magnetic field B_1 to B_2 [a]	358.233 G— 360.743 G	1065.2057 G— 1067.356 G	1774.329 G— 1776.6597 G	2840.5246 G— 2842.9586 G	3552.8748 G— 3555.0259 G
Linewidth ΔB [b]	0.251 mT	0.215 mT	0.233 mT	0.243 mT	0.216 mT
$\|S_{21}\|_{min}$	-110 dB	-104 dB	-107 dB	-112 dB	-106 dB
$\|S_{21}\|_{baseline}$ [c]	-6.1 dB	-7.6 dB	-11.3 dB	-12.85 dB	-13.26 dB
$\Delta \|S_{21}\|$ [d]	16 dB	15 dB	15 dB	16 dB	14 dB

[a] B_1 and B_2 : the starting point and ending point for ESR absorption occurrence, respectively.

[b] ΔB : linewidth as shown in Fig. 6.3 (b).

[c] $|S_{21}|_{baseline}$: background insertion loss

[d] $\Delta |S_{21}|$: largest $|S_{21}|$ magnitude changes during ESR absorption occurrence as shown in Fig. 6.3 (b).

6.4 Discussions and Conclusions

Compared with the results in [6.5], our ESR sensitivity is very high. But it seems that our sensitivity is less impressive when compared with the results in [6.11] and conventional high-Q cavity based ESR systems despite the fact that our effective Q is much higher than those systems. Further work is needed to understand the differences and issues.

Our proposed technique measures both the magnitude and phase of ESR signals quantitatively in frequency domain even though further work is needed to extract μ' and μ'' as well as the number of spins in the test sample. Conventional ESR techniques are often considered qualitative since cavity induced phase shift is often exploited for high-sensitivity operations. As a result, simultaneous measurements of ESR standards with known spin numbers are often needed to quantify the unknown ESR test samples.

In summary, our proposed ESR technique presents unique sensitivity enhancement schemes and frequency tuning approaches, which are promising to address the sensitivity and multi-frequency operations difficulties of current ESR techniques as well as the microphonic noise issues. Based on a simple meandered microstrip line, 60 μg of DPPH powder is characterized from 1 to 10 GHz. Both absorption and dispersion ESR

signals are obtained at high sensitivities even though further work is needed to quantify and differentiate the underline physical processes.

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CHAPTER SEVEN

CONCLUSION

This dissertation investigates high frequency devices and circuit modules for biochemical microsystems. These modules are designed towards replacing external bulky laboratory instruments and integrating with biochemical microsystems. Charge pump circuits are used as on-chip power supply. CMOS pulse generation circuits are designed for generating high voltage short pulses on chip. A sample-and-hold circuit and a six port circuit are used as on-chip analytical tools to analyze signals in time and frequency domain.

Charge pump circuits with modified triple well diodes as charge transfer switches are presented in Chapter II. Model parameters of the modified triple well diode are extracted based on measured diode characteristics. The proposed charge pump circuits are implemented in a commercial 0.13μm bulk CMOS process. The output voltage of the four-stage charge pump circuit can be up to 18.1V, which is much higher than the nwell/p-substrate breakdown voltage (~10V) of the given process.

Chapter III presents three types of on-chip pulse generation circuits. The first is based on CMOS pulse-forming-lines (PFLs). It includes a four-stage charge pump, a four-stacked-MOSFET switch and a 5 mm long PFL. The circuit is implemented in a 0.13 μm CMOS process. Pulses of ~1.8 V amplitude with ~135 ps duration on a 50 Ω load are obtained. The obtained voltage is higher than 1.6 V, the rated operating voltage of the process. The second is a high-voltage Marx generator which also uses stacked

MOSFETs as high voltage switches. The output voltage is 11.68 V, which is higher than the highest breakdown voltage (~10 V) of the CMOS process. The third is a CMOS Blumlein generator including a two-stacked-MOSFET high voltage switch, a Blumlein PFL network, and an on-chip Klophenstein taper. Gaussian-like pulses of 725 mV peak-to-peak amplitude, ~126 ps duration and 3.18 GHz bandwidth are measured on a 50 Ω load. After de-embedding the connection system and Klophenstein taper, the pulses of 1.88 V and 114 ps duration are obtained. These results significantly extend high-voltage short pulse generation capabilities of CMOS technologies.

A highly reconfigurable, low-power, and compact directional coupler is presented in Chapter IV. The active inductors and varactors are used in this directional coupler to tune operating frequencies and coupling-coefficients. The coupler is implemented in a 0.13 μm CMOS process. It occupies an area of 350 μm×340 μm and consumes 40 mW or less power. The obtained 1-dB compression point is -3.2 dBm, and the measured noise figure is ~23 dB. The measured coupling coefficient can be tuned from 1.3 dB to 9.0 dB at 4 GHz with 32 dB or better isolation and 15 dB or better return loss. The operating center frequency can be tuned from 2.0 GHz to 6.0 GHz for a nominal 3-dB operation. A six-port circuit based on four quadrature hybrids is also proposed, designed and simulated for analyzing signals in frequency domain on chip. However, the performance of the CMOS six-port circuit was seriously affected by large insertion loss and power measurement limitation. Thus, future work will be focused on designing miniaturized vector network analyzer integrated with our biochemical systems. The preliminary work on the miniaturized VNA is shown in Appendix A.

A high-speed sample-and-hold circuit (SHC) is designed and implemented for very fast signal analysis in time domain in Chapter V. Spatial sampling techniques are exploited with CMOS transmission lines in a 0.13 μm standard CMOS process. The SHC includes on chip coplanar waveguides (CPW) for signal and clock pulse transmission, a clock pulse generator, and three elementary samplers periodically (L=7.2 mm) placed along the signal propagation line. The SHC samples at 13.3 Gs/s. The circuit occupies an area of 1660 μm×820 μm and consumes ~6 mW at a supply voltage of 1.2 V. The obtained input bandwidth is ~11.5 GHz.

Finally, a novel electron spin resonance spectroscopy (ESR) technique with high sensitivity and wide frequency tuning capabilities is proposed for the development of biochemical microsystems in Chapter VI. The ESR technique was demonstrated by measuring 60 μg DPPH powder from 1 GHz to 10 GHz. A meandered microstrip line is built and used for the test. Further work is needed to extract μ' and μ'' as well as the number of spins in the test sample.

APPENDIX A

Miniaturized vector network analyzers (VNAs) integrated with biochemical microsystems offer an attractive approach to the measurement of the complex permittivity of different materials. Miniaturized VNAs, instead of bulky commercial VNAs, can be used to analyze signals generated by biochemical microsystems in frequency domain.

Fig. A-1 shows the schematic diagram of the miniaturized VNA [4.42]. The interferometer or sensor is excited with a RF signal. The measured signal is converted to an intermediate frequency (IF) f_{IF} by multiplying with a signal at a LO frequency. The RF and LO oscillator are linked through a phase locked loop to a common crystal-stabilized frequency reference. The IF filter is used to keep the noise out of the obtained IF signal. A small IF bandwidth increases the dynamic range of the miniaturized VNA. Another LO oscillator generates a sinusoidal signal which is used to mix the IF signal down to two DC signals. These two multipliers are known as I/Q demodulator. The low-pass filters are used to suppress all other frequency components and retain the two DC signals I and Q, corresponding to the real and imaginary parts of S_{21}. The dielectric permittivity of the materials under test onto the interferometer can be extracted from the S_{21} measurements.

Fig. A-2 shows the ideal ADS simulation model of the miniaturized VNA integrated with our interferometer. A harmonic balance simulation is used to obtain I and Q outputs of the I/Q demodulator. Fig. A-3 compares the S_{21} simulation results of the

interferometer directly obtained from ADS simulator with the simulation results of the miniaturized VNA. These two results agree with each other reasonably well.

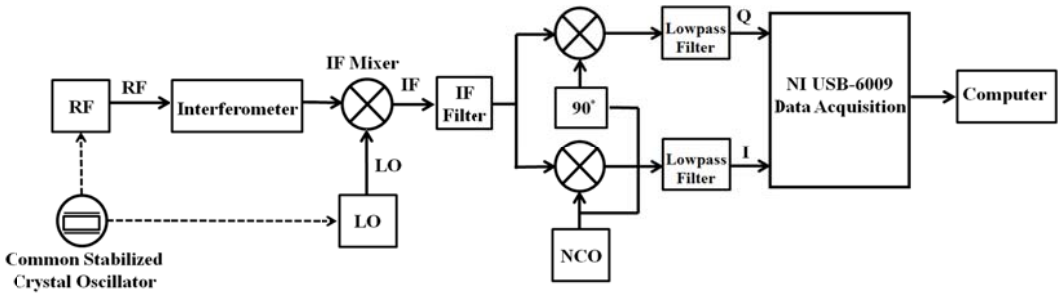


Figure A-1 Schematic diagram of the miniaturized VNA.

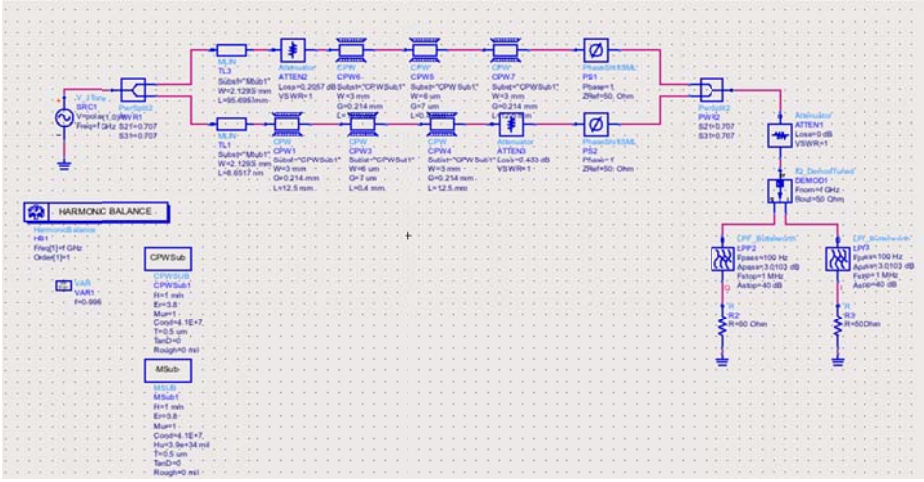
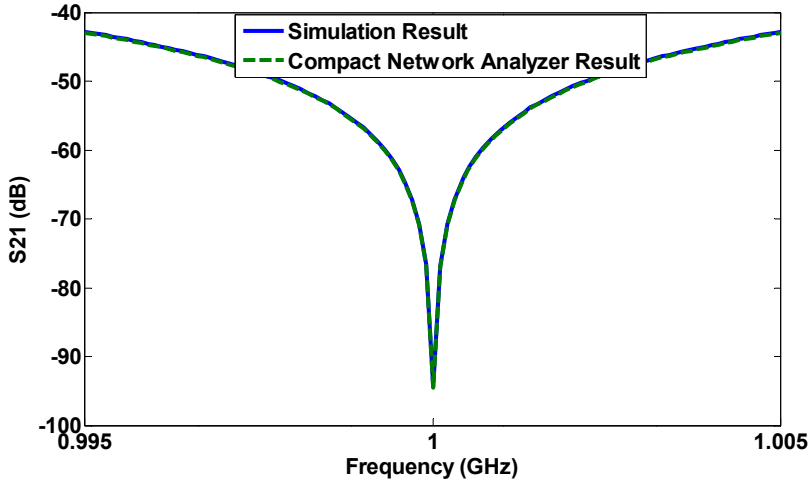
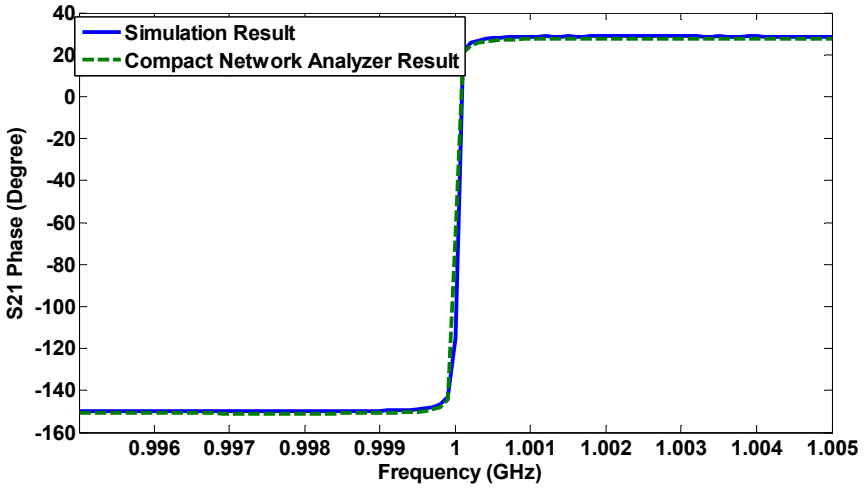


Figure A-2 ADS ideal model of the miniaturized VNA.



(a)



(b)

Figure A-3 S_{21} (a) magnitude (b) phase obtained from the ideal miniaturized VNA.

Fig. A-4 shows the real ADS simulation model of the proposed miniaturized VNA. In Fig. A-5, an attenuation of 7 dB for S_{21} simulation results of the miniaturized VNA is obtained by a comparison with ADS simulations, caused by the insertion loss of an IF mixer, an I/Q demodulator and low-pass filters. Thus, the calibration is needed to perform to compensate this loss.

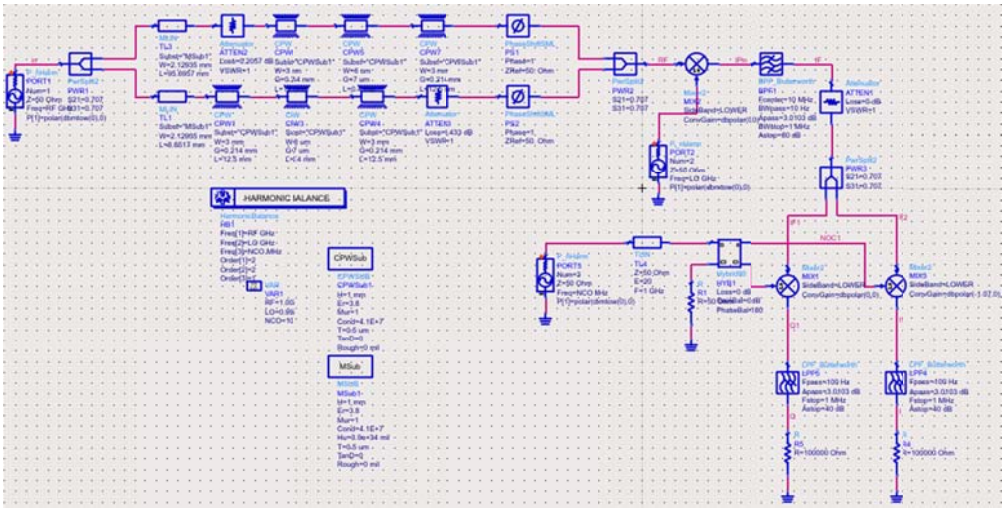
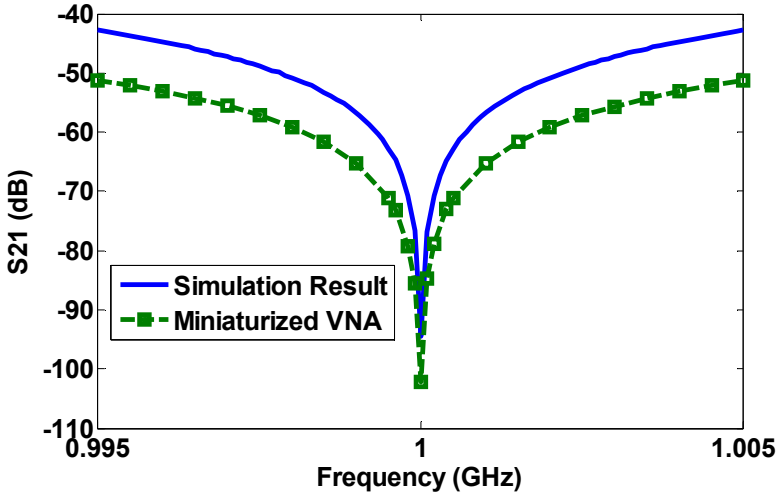
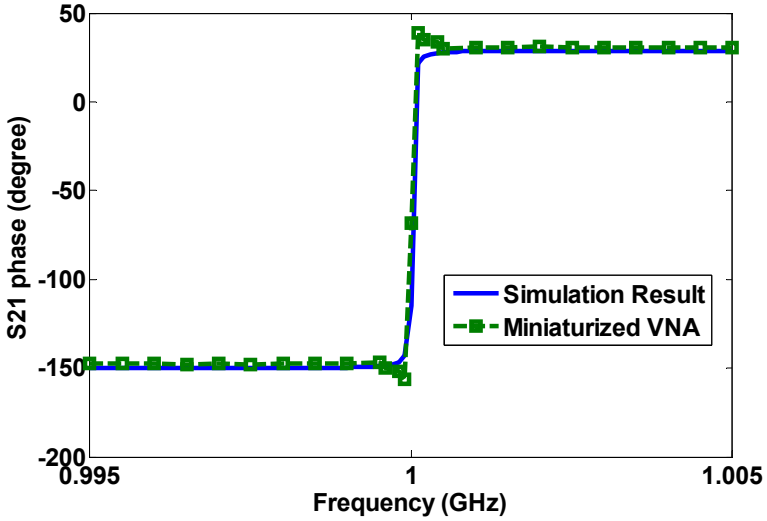


Figure A-4 ADS real model of the miniaturized VNA.



(a)



(b)

Figure A-5 S_{21} (a) magnitude (b) phase obtained from the real miniaturized VNA.

Fig. A-6 shows the preliminary lab setup to test the miniaturized VNA prototype. It consists of an ADL5380 I/Q demodulator, an ADF 4351 wideband synthesizer, and an ADRF6510 with programmable filters and variable gain amplifiers. A resonator was used

as the DUT to test the miniaturized VNA prototype. Fig. A-7 compares the S_{21} magnitude of the resonator obtained from our prototype with a commercial VNA.

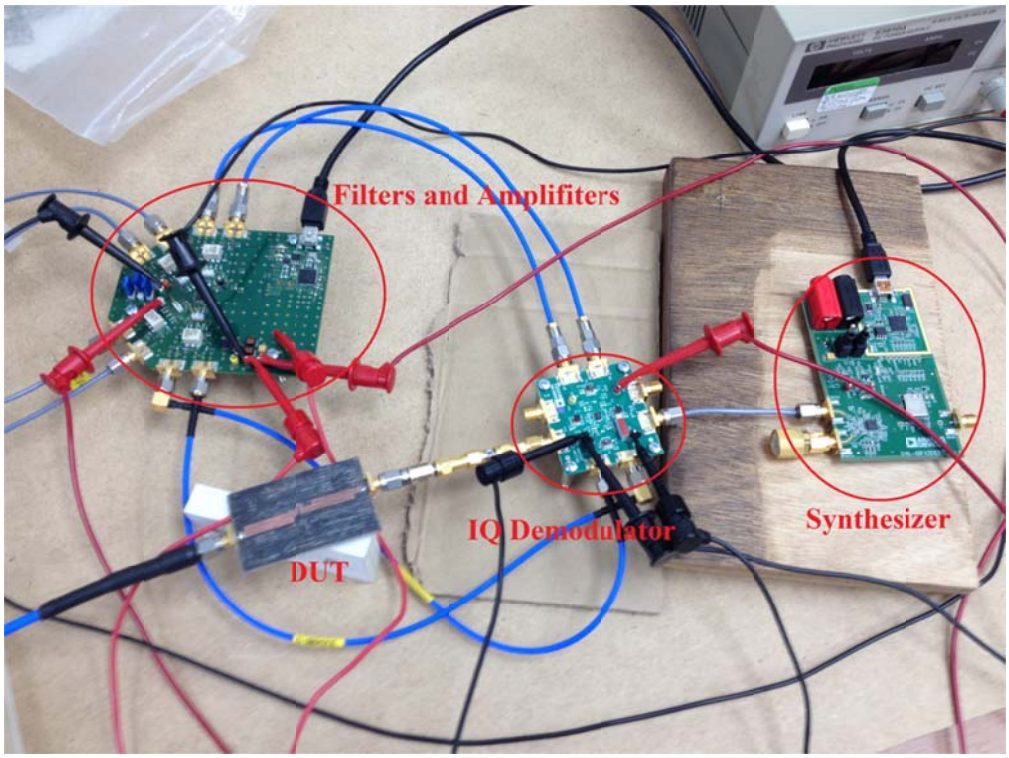
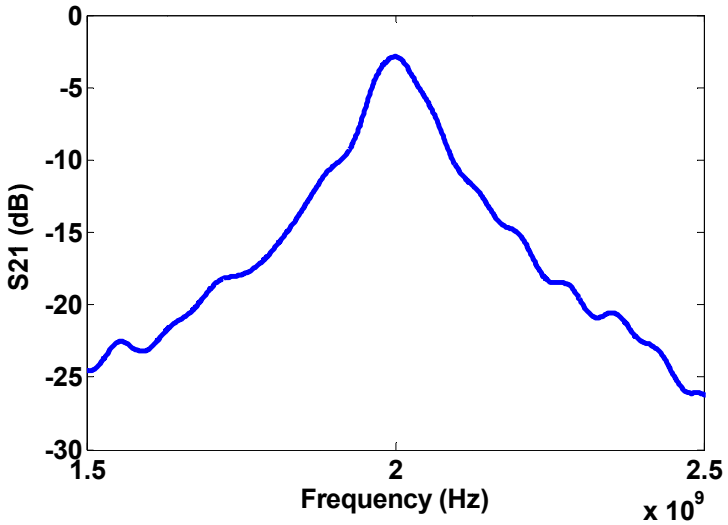
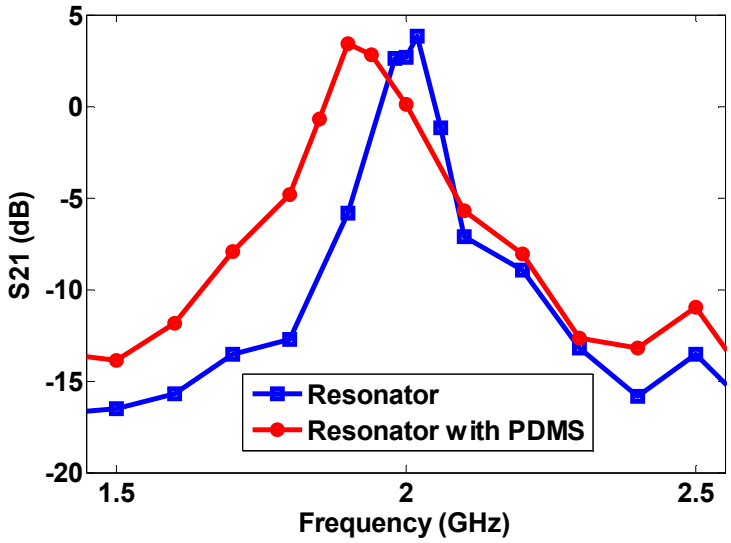


Figure A-6 Measurement setup of the miniaturized VNA.



(a)



(b)

Figure A-7 S_{21} magnitude of the resonator obtained from (a) a commercial VNA (b) our miniaturized VNA.

In Fig. A-7, the S_{21} magnitude of the resonator obtained from the miniaturized VNA resembles the shape of the measurement result obtained by the commercial VNA. However, an amplification of 7 dB for the S_{21} magnitude measured by our miniaturized VNA is obtained by a comparison with a commercial VNA, due to amplifiers used in the prototype shown in Fig. A-6. Thus, the calibration is needed to perform. Additionally, when a piece of PDMS is placed on the resonator, the peak of the S_{21} magnitude is shifted to the lower frequency. And this shift can be obtained by our miniaturized VNA, as shown in Fig. A-7 (b).

The preliminary measurement results shown above verify that the approach to the miniaturized VNA is valid. Therefore, our prototype for VNA can be continued to

implement and improve. Future works will be focused on obtaining S_{21} phases of DUT by our miniaturized VNA, improving the dynamic range and reducing the noise floor. Calibration procedure is also needed to develop for our miniaturized VNA. Furthermore, our prototype will be used in the measurement of the complex permittivity of different materials, which is important for the development of biochemical microsystems.