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FABRICATION AND CHARACTERIZATION OF Cu/4H-SiC SCHOTTKY DIODES

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ABSTRACT

Copper Schottky contacts to n-type 4H Silicon Carbide with nickel ohmic contacts were fabricated. The electrical and physical characteristics of these Schottky diodes were analyzed and the results are presented. I-V measurements revealed two sets of characteristics, one indicating nearly ideal Schottky behavior and the other exhibiting regions with two barrier heights. The reason for this observed phenomenon was studied and attributed to the in-homogeneity of the Silicon Carbide surface. The I-V and C-V characteristics were used to extract the electrical parameters, which include barrier height, ideality factor, reverse saturation current density, and doping concentration. The measured barrier height was close to the Schottky-Mott limit. The importance of an additional surface clean prior to the deposition of the Schottky contacts was established. Significant improvement in the electrical characteristics was observed when this second surface clean was performed. C-V measurements and XPS results indicate that this improvement was due to the removal of an oxide layer from the SiC surface which formed some time after the initial wafer clean. This thesis presents some of the first experimental data on Cu/4H-SiC Schottky diodes.

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CHAPTER 1

INTRODUCTION

1.1 Silicon Carbide – Properties and Advantages

Silicon Carbide is a compound-semiconductor material with many outstanding physical properties which make it a potential candidate for important applications in the electronics industry. It has the ability to provide momentum to the system miniaturization drive. It is the third hardest material known to man. Its ability to work in high temperature, high power, and high radiation environments will enable far-reaching performance enhancements to a wide variety of systems. SiC has a wide band gap, high thermal conductivity, high saturated drift velocity, and high breakdown voltage which makes it one of the most attractive materials for high temperature, high power and high frequency electronic devices. Owing to the superior electronic properties of 4H-SiC over 6H-SiC, including a higher electron and hole mobility, 4H-SiC has generated much interest in the semiconductor industry lately. Copper, with its high thermal conductivity and low resistivity, is one of the best materials for developing stable Schottky rectifiers for high power applications. This research focuses on the fabrication and characterization of Cu/4H-SiC Schottky contacts.

1.2 Overview of Chapters

In Chapter 2 we review the basic physical and electronic properties of Silicon carbide which make it an attractive material for many electronic applications. In this

chapter, we also present the different crystal growth mechanisms and the different kinds of defects prevalent in Silicon Carbide.

In Chapter 3 we review the fundamental theory of metal-semiconductor contacts, including both Schottky and ohmic contacts. The current transport mechanisms and capacitance-voltage characteristics of metal semiconductor contacts are also discussed in this Chapter.

In Chapter 4 we review the design of the SiC Schottky diodes used in this project. We also describe the fabrication process, which includes different surface preparation techniques and cleaning, ohmic contact formation, the Schottky metal deposition, and several protective coating deposition techniques.

In Chapter 5 the results from different types of measurements, which include Current Voltage measurements, and Capacitance Voltage measurements, are presented and conclusions based on these results are explained. From the current voltage characteristics we were able classify the devices into two sets. The difference in their performance was attributed to the in-homogeneity of Silicon Carbide wafers. This is discussed in Chapter 5 by comparing the different electrical parameters of these two sets of devices.

In Chapter 6 we establish the importance of a second surface clean just prior to the Schottky contact deposition. This affected the performance of the diodes drastically. This was attributed to an oxide layer at the Schottky contact interface and was verified using electrical and physical characterizations.

Chapter 7 is the final Chapter, in which we summarize the work done, goals achieved and prospective ideas for future research on Cu-SiC Schottky contacts.

CHAPTER 2

SILICON CARBIDE

Silicon Carbide is a material which has important applications in the electronics industry. It has the potential to dramatically extend the reach of electronic technology and give unprecedented momentum to the system miniaturization drive [1]. In this Chapter the physical and electrical properties of SiC, which make it an attractive material for future electronic applications, are discussed. The crystal structure of SiC is introduced in the first section. The next section focuses on the physical and electronic properties of SiC and crystal growth mechanisms. We conclude with a brief discussion of material defects, which limit the performance of SiC devices.

2.1 Physical Properties

2.1.1 Crystal Structure

Silicon Carbide consists of an equal number of Silicon and Carbon atoms. Each Silicon atom is covalently bonded to four Carbon atoms in a tetrahedral structure with the silicon atom in the center. Similarly, each Carbon atom is bonded to four other Silicon atoms. A sheet of Silicon Carbide consists of a bi-layer composed of one layer of Silicon atoms and another of Carbon atoms. The distance between neighboring Carbon or Silicon atoms, a, is 3.08 Å. The Silicon Carbon bond length is approximately 1.89 Å. The angle between the Carbon–Silicon–Carbon bonds is 109.5° [5]. Silicon Carbide exhibits one dimensional polymorphism known as Polytypism [2]. Polymorphism is the

phenomenon whereby a compound takes on different crystal structures due to the differences in stacking order. In SiC the difference among the polytypes arises in only one direction. This is discussed in detail in the following section.

2.1.2 Polytypes

If we consider a Silicon and a Carbon atom as a single unit, and if they were arranged in a plane called A, there are two possible arrangements, B and C, for the next layer. This is illustrated in Fig. 2.1. Likewise, there are two possible stacking arrangements A and C on layer B. Hence, a number of stacking arrangements are possible, which results in polytypism [3].

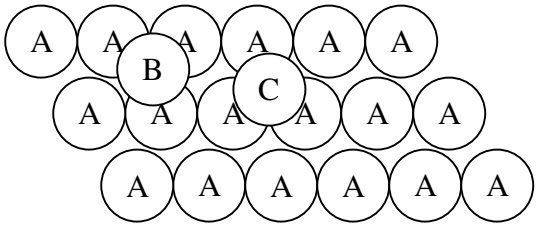


Fig 2.1 Stacking sequences of 3C and 4H-SiC

SiC can exist in more than 250 known polytpes [2]. The crystal structures of SiC are Cubic, Hexagonal or Rhombohedral. Some of the common polytypes of SiC are denoted as 3C, 2H, 4H, 16H, 15H, where C represents a cubic lattice and H represents hexagonal lattice. The numbers 3, 2, 2, 4, 16 and 15 represent the number of layers of SiC per unit cell. The stacking sequence for the most important polytypes is illustrated in

Fig. 2.2. The 3C crystal structure consists of 3 layers along the stacking direction in a cubic arrangement, while the 2H, 4H, 6H structures have 2, 4 and 6 layers respectively, periodically repeated in a hexagonal crystal structure. The unit cell for the hexagonal crystal structure is shown in Fig. 2.3, and will be discussed subsequently.

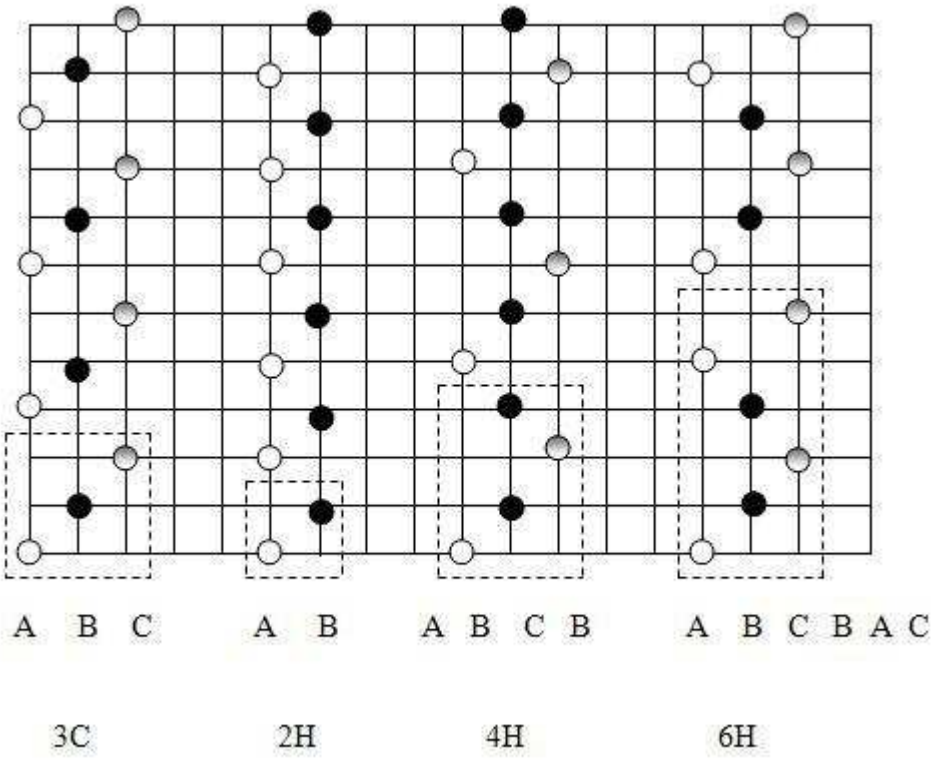


Fig. 2.2 Stacking sequences of 3C, 2H, 4H and 6H-SiC [4].

The number in the polytype specification represents the number of layers before which the pattern is repeated, and the letters represent the resulting structure. The first part of Fig. 2.2 shows a 3C polytype, in which 3 layers repeat periodically to form a Cubic structure. Similarly, two layers repeat periodically to form a hexagonal structure resulting in the 2H polytype. In the 4H structure four layers, for example ABCB, keep

repeating themselves and in the case of the 6H structure, a six layer pattern ABCBAC keeps repeating itself.

The unit cell of some polytypes of SiC is a hexagon, represented in Fig. 2.3. As shown, the c axis, which is perpendicular with respect to the base plane, is the direction of stacking. The other three axes are on the same plane with an angle of 120° with respect to each other. Most crystal planes can be represented by Miller indices using three numbers. The hexagonal system has four axes of reference; therefore, four numbers are needed to represent any plane in this crystal structure. Axes a1, a2 and a3 are perpendicular to the c axis. The shaded portion in grey is the [0001] plane, while the direction representing it is the c axis. As shown in Fig. 2.3, the plane shaded in grey meets the four axes at a1=∞, a2=∞, a3=∞ and c=1. When we take an inverse of these numbers we get four numbers which are represented as [0001]. The area shaded in black represents the $(1\bar{1}00)$ plane and the direction is indicated by the dotted line with an arrow. While calculating the Miller indices, if we end up with fractions, we need to multiply all the four numbers by their least common multiple.

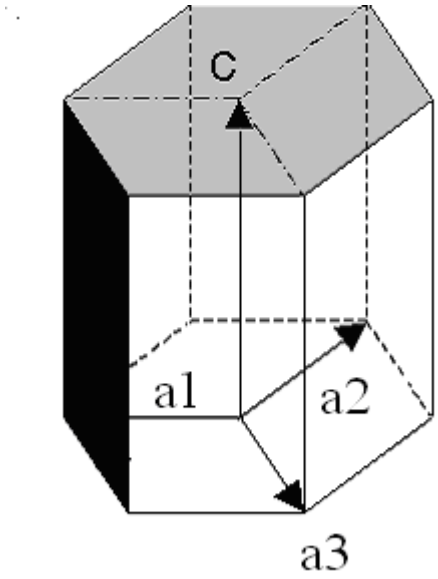


Fig. 2.3 Hexagonal SiC Unit Cell.

The plane formed by a bi-layer sheet of silicon and carbon atoms is known as the basal plane, while the crystallographic c-axis direction, also known as the stacking direction or the [0001] direction, is defined normal to the SiC bi-layer plane. Figure 2.4 depicts schematically the stacking sequence of the 6H-SiC polytype, which requires six SiC bi-layers to define the unit cell repeat distance along the c-axis [0001] direction. The $[1\bar{1}00]$ direction depicted in Fig. 2.4 is often referred to as the a-axis direction. The silicon atoms labeled 'h' or 'k' in Fig. 2.4 denote SiC double layers that reside in quasi-hexagonal or quasi-cubic environments with respect to their immediately neighboring atom above and below bi-layers. SiC is a polar semiconductor across the c-axis, in that one surface normal to the c-axis is terminated with silicon atoms while the opposite surface is terminated with carbon atoms. As shown in Fig. 2.4, these surfaces are referred to as the 'silicon face' and 'carbon face', respectively [19].

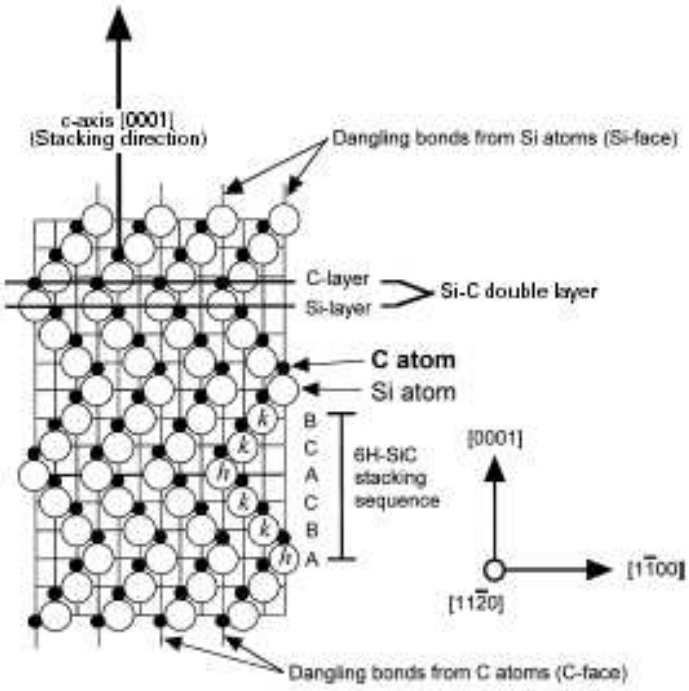


Fig 2.4 Schematic cross section of 6H-SiC polytype [18, 19].

2.2 Electronic properties of SiC

SiC is the third hardest material known to man. Its ability to operate in high temperature, high power, and high radiation environments will enable far-reaching performance enhancements to a wide variety of systems and applications [1].

Some of the important electronic properties of SiC are:

1) Wide Band Gap: The wide band gap of SiC makes it a suitable material for high temperature operation, without being affected by conduction due to intrinsic carriers [4]. At high temperatures, the thermally generated intrinsic carrier concentration can exceed the doping density, and hence the control over the

charge carriers in the device is lost. Materials with wide band gaps have a low intrinsic concentration, enabling them to perform well at high temperatures. The wide band gap results in metal semiconductor contacts with higher barrier heights, which implies a very low leakage current.

2) High Thermal Conductivity: The high thermal conductivity of SiC allows heat to readily flow through it. This allows SiC to perform well at high temperatures and high powers without heat sinks. SiC has a thermal conductivity almost three times that of Si and ten times that of GaAs [1].

3) High saturated electron drift velocity: Semiconductors like GaAs and GaN have high drift velocity in low electric fields, but it drops significantly as the electric field increases. This is illustrated in Fig 2.5. SiC has a high saturated drift velocity in the presence of high fields, which makes it a potential material for manufacturing devices which operate at high frequencies.

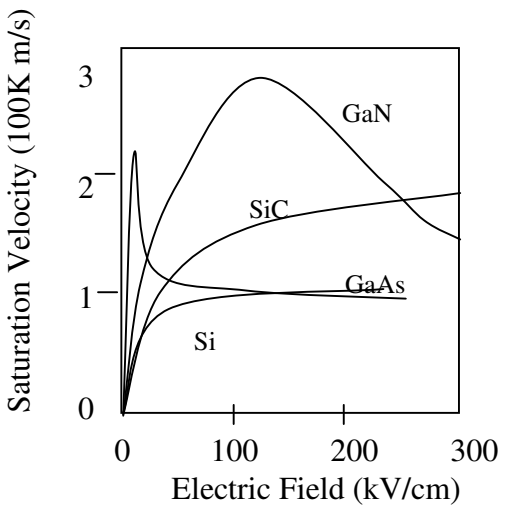


Fig. 2.5 Drift velocity vs. electric field [11].

4) High breakdown voltage: SiC can withstand very high electric fields without breakdown that are almost eight times that of GaAs and Si. Therefore, devices made of SiC have high breakdown voltages. This also allows devices to be placed in close proximity to each other, resulting in higher packing density [5]. The high breakdown voltage also reduces the on-resistance of SiC devices. SiC devices also exhibit a positive temperature coefficient of breakdown voltage [6]. This indicates the dependence of breakdown voltage on temperature. If the device has a positive temperature coefficient of breakdown voltage, then local junction heating from breakdown current increases the local breakdown voltage, preventing local concentration of breakdown current which prevents formation of hot spots. This helps devices perform better even in the presence of large reverse over-voltage transients.

Fig. 2.6 graphically compares some of the properties of Silicon and Silicon Carbide. This compares the magnitudes only. The Band gap is in eV, the breakdown field is in MV/cm and the thermal conductivity is represented in W/cm.K. It is clear from this figure that SiC is superior to Si in terms of properties which are essential for high temperature and high power applications.

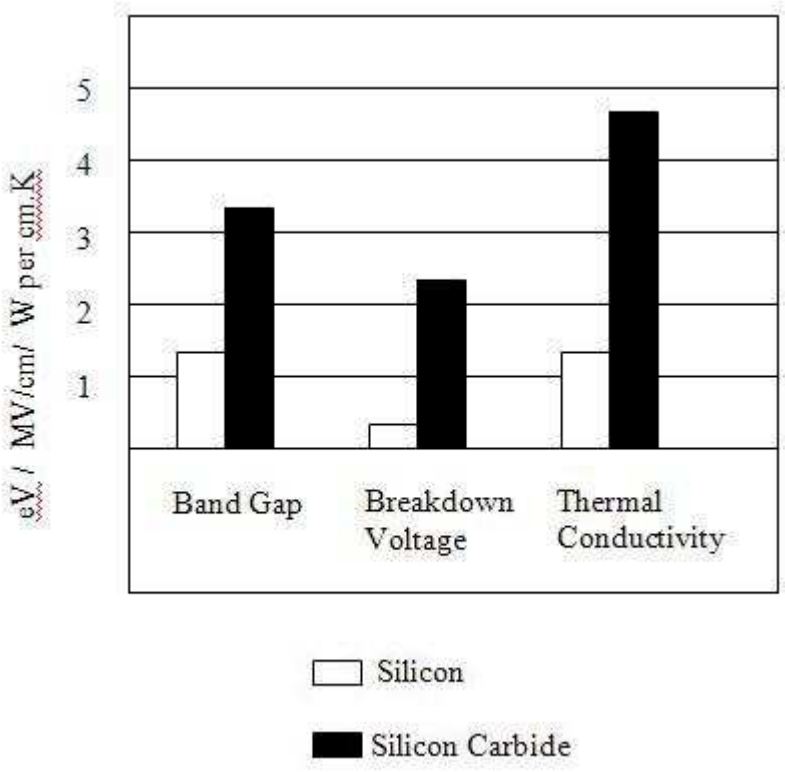


Fig. 2.6 Comparison of Electronic Properties of Si and SiC - magnitudes only [1].

Table 2.1 lists some of the electrical properties of 4H SiC which have been discussed earlier in this section, and compares them with the properties of Si, GaAs and two other polytypes of SiC of industrial interest. We can conclude from this table that

SiC has higher values for band gap, breakdown field, density, saturated electron drift velocity, and thermal conductivity compared to the other semiconductors used in the industry, while it has a smaller dielectric constant. Also, the diameter of commercially available wafers for SiC is much smaller compared to the other commercially used semiconductors. High density of yield-affecting mircopipe defects are reported as the primary limiting factor in increasing SiC wafer size [48].

Table 2.1 Comparison of the electronic properties of
Si, GaAs and 3 polytypes of SiC [10, 11]

	Si	GaAs	SiC		
			6H	4H	3C
Bandgap (eV)	1.1	1.42	3.0	3.2	2.3
Breakdown Field @ $10^{17}cm^{-3}$ (MV/cm)	0.6	0.6	3.2	3	>1.5
Commercial Wafer Diameters	12”	6”	1.375”	1.375”	None
Density (g/cm^3)	2.328	5.32	3.2	-	3.2
Dielectric Constant	11.8	12.8	9.7	10	9.6
Direct/Indirect Bandgap	I	D	I	I	I
Electron Mobility@ $10^{16}cm^{-3}$ (cm^{-2} /V.S)	1100	6000	370	800	750
Hole Mobility @ $10^{16}cm^{-3}$ (cm^{-2} /V.S)	420	320	90	115	40
Ionization Energy of Al (eV)			0.24	0.191	0.257
Intrinsic carrier concentration (cm^{-3})	1.5E10	1.8E6	2.3E-6	8.2E-9	6.9
Saturated Electron Drift Velocity (cm/s)	1E7	1E7	2E7	2E7	2.5E7
Thermal Conductivity (W/cm.K)	1.5	0.5	4.9	4.9	5.0

Of the 170 crystal types of SiC, there are only two polytypes, 4H and 6H, which are commercially available. 4H SiC is preferred over 6H SiC for many electronic applications, as it has a higher and more isotropic electron mobility and a wider band gap

compared to the 6H and 3C polytypes of SiC [12]. The above mentioned properties of SiC such as wide band gap, high electron drift velocity, high thermal conductivity, and high breakdown voltage make it a potential material for a wide variety of electronic applications, especially high power, high temperature and high frequency.

2.3 SiC Devices

SiC Schottky Diodes:

Current conduction in Schottky diodes is due to majority carriers, which allows them to operate at high switching frequencies without any reverse recovery, which slows switching. They do not exhibit dynamic avalanching or snap back due to the sudden disappearance of minority carriers [7].

SiC Schottky diodes operate with breakdown voltages almost five times larger than that of Si Schottky diodes. Due to the wide band gap of SiC, reverse current is relatively low. SiC diodes have high current density which makes them suitable for high current, high temperature, and high power applications. Schottky diodes target the high-speed, high-power-density switching market. This includes products or functions such as high-frequency power supplies, power factor correction, and power conversion in motor controls or power management appliances. Primarily, SiC Schottky diodes are targeting the market for components operating at 6-8 A and 600 V, for power factor correction in high-end AC/DC power supplies, and in uninterruptible power supplies [8].

SiC MESFETS

The quality of the material available now has led to the commercial availability of 10 W SiC MESFETs (Metal Semiconductor Field Effect Transistors). The MESFET has a Schottky contact as the gate and ohmic contacts to the source and drain, while the MOSFET has a metal-oxide- semiconductor contact as the gate. The control of the channel in the case of a MESFET is obtained by varying the depletion layer width underneath the metal contact which modulates the thickness of the conducting channel and thereby the current. SiC MESFETs have entered a pre-production level at Cree, Thales, and other companies; however, lifetime and production yield remain key issues when moving to full production [8].

2.4 Crystal Growth

Several methods are available for growth of SiC crystals. There are many issues related to the growth of good quality SiC. Due to the phase equilibrium in SiC, it cannot be formed from a congruent melt, because it sublimes before melting [13]. Sublimation is the most common form of SiC growth. Ultra pure SiC powder is sublimed to deposit SiC lengthwise on a crystalline SiC seed. This method is commercially used to grow 4H and 6H SiC [8]. The complex geometry of crucible and insulation materials and the high temperatures required of up to 2700K make direct measurements during the growth process very difficult [14]. The other methods available but not prevalently used, are high-temperature chemical vapor deposition, Heteroepitaxy of SiC on silicon [15], and Vapor liquid solidification [8].

2.5 Defects in SiC

The main factor which limits the performance of SiC devices is the presence of crystalline defects. Voids are the main form of defects which affect SiC. They are classified into three categories (1) Micro-nanopipes (5nm≤ diameter ≤ 15μm), (2) Macrodefects (pipes) (diameter ≥ 20μm), and (3) Planar voids (diameter ≥ 50μm) [16]. The primary impacts of defects in Schottky rectifiers are reduction in breakdown voltage and an increase in leakage current.

Micropipe defects are the major obstacles to the production of high performance SiC devices. Micropipes are defects unique to the growth of SiC. They are physical holes that penetrate through the entire crystal and replicate into the epitaxial layer. They become "killer defects" if they are found on the active region of the device [14]. Fig 2.7 is a picture of a micropipe defect, which was obtained using a Nikon AFX-II microscope with a 1000x lens. Neudeck and Powell [17], have shown that micropipe defects cause the devices to breakdown at voltages below the breakdown voltage expected due to avalanche multiplication. They report that 80% of $1mm^2$ 6H-SiC epitaxial pn junction devices they fabricated failed at voltages below 500V, well below the predicted avalanche breakdown values. In Fig 2.8, the typical reverse failure characteristics of these diodes are shown. Also, Neudeck and Powell establish the link between these junction failures and micropipe defects with microplasmas observed at the location of the micropipes, visible only when the diodes were biased beyond their unique breakdown voltage.

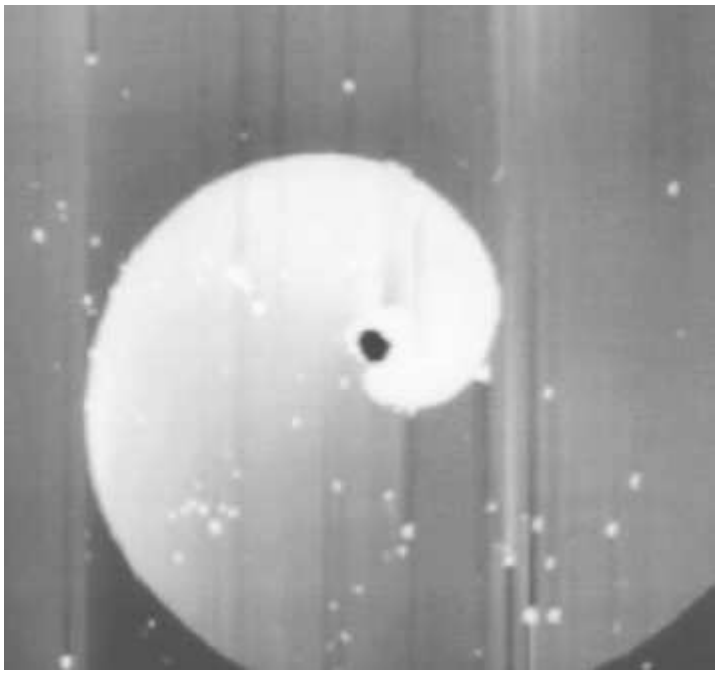


Fig. 2.7 Micropipe defect [17]

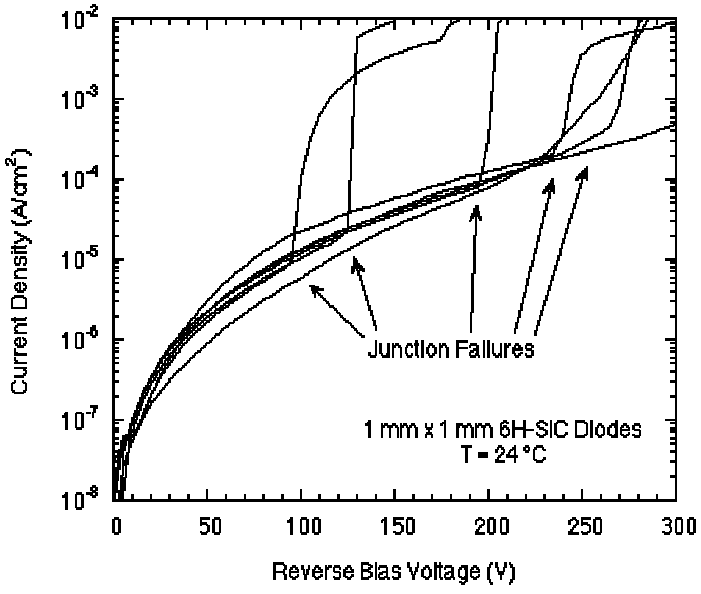


Fig. 2.8 Low break down voltage due to Micropipe defects [17]

High-power-density components require large micropipe-free areas, but current micropipe densities only allow active areas of about 20 mm^2. The realization of 4 inch wafers is difficult with the standard manufacturing techniques available. Table 2.2 shows the road map for production of SiC wafers. The road map predicts that by 2006, SiC will be commercially available with micropipe densities of about $0.1/cm^2$. It also shows that the maximum available area will increase to $40mm^2$, and the conducting wafer should increase to 4 inches, making it much more useful commercially.

Table 2.2 Roadmap for SiC wafers [7]

Features of SiC	2002	2003	2006
Micropipe density ($/cm^2$)	15	1	0.1
Maximum available area (mm^2)	8	16	40
Conducting wafer size (inches)	3	3	4
Semi-insulating wafer size	2	2-3	3

2.6 Conclusion

The properties discussed in this Chapter make Silicon carbide a suitable semiconductor for several electronic applications. Current research to overcome the problems with the crystal growth mechanisms and the formation of defects looks promising. Soon SiC wafers of reasonable diameter of industrial quality should be available on the market.

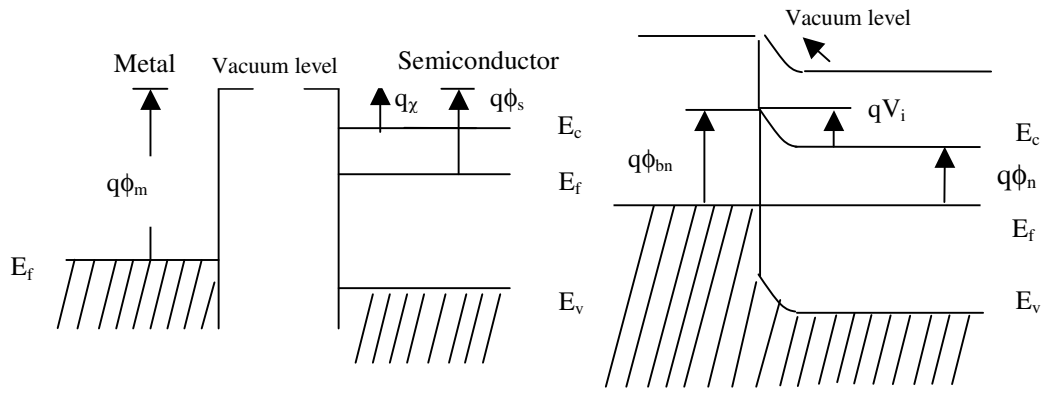
CHAPTER 3

METAL SEMICONDUCTOR CONTACTS

In this Chapter we review the theory of operation of metal semiconductor contacts. A brief introduction is given about ideal rectifying contacts, and then a description about the current conduction mechanisms involved. We also discuss the operation of ohmic contacts. Finally, the techniques for the extraction of different electrical parameters from the IV and CV characteristics are described.

3.1 Ideal Rectifying contacts

Metal-Semiconductor contacts exhibit rectification because of the existence of an electrostatic potential barrier between the metal and the semiconductor, which is due to the difference in work function between the two materials. Fig. 3.1(a) illustrates the energy band diagrams of an isolated n-type semiconductor and a metal. Here the work function of the metal is greater than that of the semiconductor. Work function is defined as the energy difference between the vacuum level and the Fermi level. ϕ_m is the work function of the metal. For a semiconductor the work function is equal to $\chi+\phi_n$, where χ is the electron affinity and ϕ_n is the difference in energy between the conduction band and the Fermi level [20].



(a) Separate materials (b) Metal Semiconductor Contact

Fig. 3.1 Ideal Metal semiconductor band diagram

When a metal and an n-type semiconductor are brought into intimate contact, and if the work function of the metal is greater than the work function of the semiconductor, electrons will flow from the semiconductor to the metal until the Fermi levels coincide. As they are brought closer, an increasing negative charge is built up at the metal surface with an equal and opposite charge in the semiconductor, resulting in an electric field in the junction [21]. This built-in potential opposes the flow of electrons and eventually forces a state of equilibrium to be attained. Since the carrier concentration in the semiconductor is much less than the concentration of electrons in the metal, the positive charges in the semiconductor form a layer of appreciable thickness and the bands in the semiconductor near the interface bend upwards [22].

When the metal and an n-type semiconductor are brought into close contact with each other, the barrier height formed between the metal and the n-type semiconductor, $\phi_{bn,}$ is defined ideally by the Schottky Mott limit, given by:

$$q\phi_{bn} = q(\phi_m - \chi) \quad \text{-- (3.1)}$$

In the case of a p-type semiconductor, the barrier height, ϕ_{bp}, is given by [20]:

$$q\phi_{bp} = E_g - q(\phi_m - \chi) \quad \text{-- (3.2)}$$

The Schottky Mott limit implies that the barrier height can be controlled by the choice of the metal. If there is a large density of interface states present at the metal semiconductor interface, then the barrier height is defined by the Bardeen limit, in which case the barrier height is only determined by the interface state density [26]. In between these two limits is where the barrier height will typically be for real Schottky diodes.

3.2 Current Conduction Mechanisms

The Principal current conduction mechanisms in metal semiconductor contacts, are illustrated in Fig. 3.2, and are described below:

1) Transport of electrons from the conduction band of the semiconductor into the metal over the barrier.
2) Quantum mechanical tunneling of electrons though the barrier into the metal
3) Recombination of holes and electrons in the space charge region
4) Injection of holes from the metal into the neutral region of the semiconductor

These mechanisms are discussed in detail in the next four sections of this Chapter.

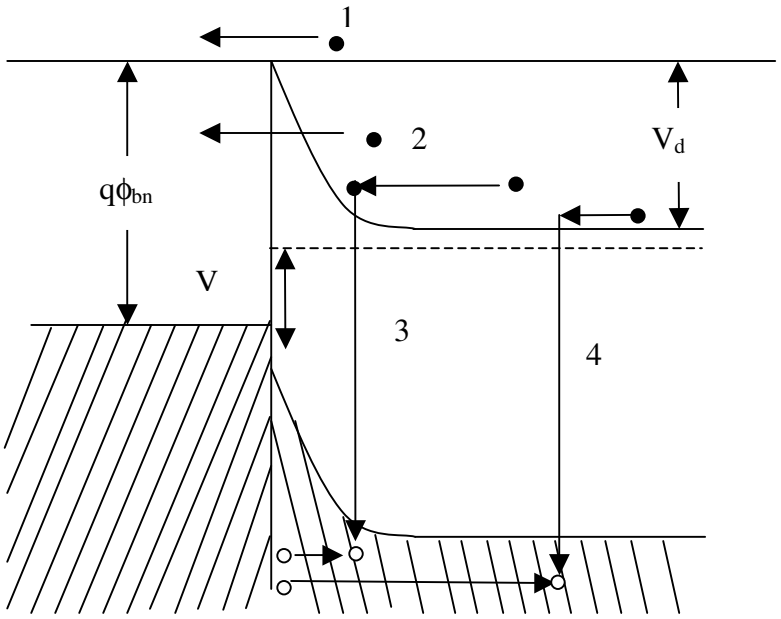


Fig. 3.2 Principal current conduction mechanisms in metal semiconductor junctions [27].

3.2.1 Emission over the Barrier

For the electrons to move from the conduction band of the semiconductor into the metal they have to first be transported through the space charge region and then emitted over the barrier. There have been two theories proposed for this phenomenon. One of them is the diffusion theory of Wagner (1931) and Schottky and Spenke (1939), and the other is the theory of themionic emission [21, 22 and 23]. According to diffusion theory, the current is limited by diffusion and drift in the depletion region. The electrons in the conduction band of the semiconductor are in equilibrium with the electrons in the metal near the interface. The applied voltage has no effect on the concentration of electrons at the interface. Hence, the quasi Fermi level in the semiconductor coincides with the Fermi level in the metal at the junction as shown in Fig. 3.3. Since the gradient of the quasi

Fermi level is the driving force for the electrons to move from the semiconductor to the metal, the transportation of electrons in the space charge region is the reason for the current flow [22].

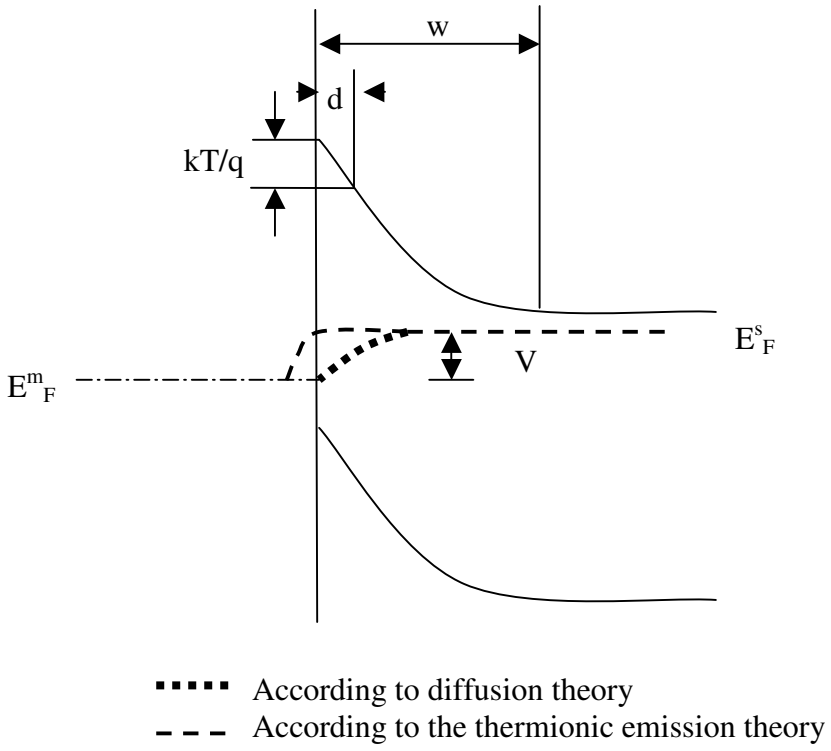


Fig. 3.3 Electron quasi-Fermi level in a forward-biased Schottky barrier

Thermionic emission theory suggests that the current is limited by emission of electrons over the barrier, similar to the thermionic emission of electrons from a metal into vacuum. The transported electrons are not in thermal equilibrium with the electrons in the metal. They lose energy as they move into the metal and the quasi Fermi level approaches the Fermi level in the metal. Hence, the electrons are not in thermal equilibrium at the interface and the quasi Fermi level does not coincide with the Fermi

level of the metal at the boundary, but remains constant throughout the barrier region. The condition for thermionic emission theory to be applicable is that the electron mean free path be greater than the distance d, in which the barrier falls by kT from its maximum value. Experimental data has shown that the thermionic emission theory is a better approximation than the diffusion theory [23].

The thermionic emission and diffusion theories were combined to give the thermionic emission diffusion theory. This theory suggests that the total current in the Schottky diode is a due to diffusion and thermionic emission and the equation for the current density is given by the Richard-Dushman equation [27]:

$$J = A^{**} T^2 \exp\left(\frac{-q\phi_{bn}}{kT}\right).\left(\exp\left\{\frac{qV}{kT}\right\} - 1\right) \qquad \text{-- (3.3)}$$

where, $A^{**} = \dfrac{f_p f_Q A^*}{1 + f_p f_Q v_R / v_D}$

A * = Richardson constant for the metal/semiconductor interface

T = Temperature in kelvin

k = Boltzmann constant

q = Electronic charge

V = Effective bias across the interface

f_p = Probability of an electron crossing the barrier into the metal without being scattered by a phonon.

f_q = Average transmission coefficient

v_R = effective recombination velocity

v_D = effective diffusion velocity

Equation 3.3 makes it easy to understand the effect of the dominant carrier transport mechanism on the J-V characteristics. It also takes into account the quantum mechanical tunneling of electrons through the barrier and the reflection of electrons by the barrier.

3.2.2 Tunneling through the barrier

Quantum mechanical tunneling of carriers though the barrier is another important current conduction mechanism, which has a significant effect at low temperatures and high doping concentrations. In the case of heavily doped semiconductors, the depletion region and the barrier width are narrow, allowing carriers to readily tunnel through the barrier. Tunneling of hot carriers near the top edge of the barrier is called thermionic field emission, while emission of electrons throughout the entire barrier is called field emission. The tunneling current density is given by [27]:

$$J = J_s \exp(V / E_o)[1 - \exp(-qV / kT)] \qquad \text{-- (3.4)}$$

where, E_o is given by:

$$E_0 = E_{00} \coth(qE_{00} / kT)$$
$$E_{00} = \frac{q\eta}{2}\sqrt{\frac{N_D}{\varepsilon_s m^*}} \qquad \text{-- (3.5)}$$

where, J_s is the saturation current density, T is the temperature, E_{00} is the diffusion potential of a Schottky barrier, $\eta = h/2\pi$ where h is the Planck's constant, m^* is the effective mass of an electron, N_D is the donor doping concentration, and ε_s is the permittivity of the semiconductor. Tunneling is the main current transport mechanism in Ohmic contacts. The devices we fabricated had ohmic contacts with very low contact resistance; therefore, we can conclude that tunneling is the dominant mechanism of current conduction in our ohmic contacts. Ohmic contacts are discussed in detail in a subsequent section of this Chapter.

3.2.3 Recombination in the depletion region

Recombination of electrons and holes in the depletion region may play an important role in the case of metal semiconductor contacts at low temperatures and at low bias voltages [21]. The current density due to recombination is given by:

$$J = J_r \exp\left(\frac{qV}{2kT}\right) \qquad \text{-- (3.6)}$$

where,

$$J_r = qniA'd/\tau' \qquad \text{-- (3.7)}$$

where, n_i is the intrinsic electron concentration which is proportional to exp (- *Eg/2kT), d* is the thickness of the depletion region, *A'* its area, and τ' is the lifetime within the depletion region. In cases where the recombination current is significant, the temperature variation of the forward current shows two activation energies. Above room temperature, the activation energy tends towards the barrier height $\phi_{b,}$ characteristic of thermionic

emission, while below room temperature it approaches Eg/2, characteristic of the recombination current [20]. The effect of recombination causes a deviation from the ideal Schottky behavior, either by a deviation called the ideality factor, *n*, from unity, or deviation from the exponential behavior of current as predicted by thermionic emission [21].

3.2.4 Hole Injection

Bardeen, Brattain (1949) [23] and Banbury (1953) [24] suggested the theory of hole injection from the metal. This theory states that when the barrier height exceeds one half the band gap, the region in the semiconductor near the interface becomes inverted. The hole density in this region exceeds the electron density and hence it becomes p-type. Thus, holes are injected from the metal near the interface into the bulk of the semiconductor on the application of a forward bias, which recombine with electrons in the neutral region of the semiconductor. This phenomenon is not of much concern to us because SiC is a wide gap material with a very low intrinsic carrier concentration.

3.3 Ohmic Contacts

Ohmic contacts are metal-semiconductor junctions with relatively low resistance and a very low potential barrier, allowing the free flow of carriers across the metal semiconductor junction in both directions. Ohmic contacts, which can supply the required current with a voltage drop negligible compared to the drop across the active region, are critical for satisfactory device performance. In Ohmic contacts, tunneling is the main phenomenon of current transport. The specific contact resistance of an ohmic contact is

defined as the reciprocal of the derivative of current density with respect to voltage. For contacts in which tunneling dominates, the specific contact resistance is given by [27]:

$$Rc = \exp\left[2\frac{\sqrt{\in_s m^*}}{\eta}\left(\frac{\phi_{Bn}}{\sqrt{N_D}}\right)\right] \qquad \text{-- (3.8)}$$

Equation (3.8) shows that the specific contact resistance varies exponentially with $\left(\frac{\phi_{Bn}}{\sqrt{N_D}}\right)$. Therefore low contact resistance can be achieved with a low barrier height and a high doping concentration [27]. In order to obtain a lower barrier height, the work function of the metal should be greater than or equal to the work function of a p-type semiconductor, and less than or equal to the work function a n-type semiconductor. Tunneling also dominates when the doping concentration is very high. Therefore, a proper choice of metals with appropriate work functions and semiconductors with a high doping concentration are desired for low resistance ohmic contacts. High doping by itself can alter the work function of the semiconductor and increase tunneling to form good ohmic contacts with the metal.

Another method of obtaining a low contact resistance is by annealing the contact at a temperature below the eutectic point of the metal. The melting point of a given alloy of one substance in another depends upon the percentages of the materials present. That point on a phase diagram of temperature vs. percent of each parent material present where a temperature minimum occurs in the liquidus line is known as the eutectic point. The liquidus line separates the all liquid phase from the liquid plus crystal phase. When

the contact is annealed above this temperature it drives the carriers from the metal into the semiconductor forming an n++ or p++ layer, thus forming a tunneling ohmic junction [27].

3.4 Extraction Of Schottky Parameters

3.4.1 Extraction of parameters from I-V Measurements

The equation for current density using the Thermionic emission model is given by:

$$J = J_s \exp\left(\frac{qV}{nkT} - 1\right) = A^{**}T^2 \exp\left(-\frac{q\phi_{bn}}{kT}\right)\exp\left(\frac{qV}{nkT} - 1\right) \qquad \text{-- (3.9)}$$

n is the ideality factor which indicates the deviation from the ideal exponential Schottky behavior due to effects of recombination. For a reasonably high forward voltage; i.e., when $\frac{qV}{kT} >> 1$, equation 3.9 can be approximated as:

$$J \cong J_s \exp\left(\frac{qV}{nkT}\right) = A^{**}T^2 \exp\left(-\frac{q\phi_{bn}}{kT}\right)\exp\left(\frac{qV}{nkT}\right) \qquad \text{-- (3.10)}$$

Taking the log of both sides of Equation (3.10) we obtain:

$$\ln(J) = \ln(J_s) + \frac{qV}{nkT} = \ln(A^{**}T^2) - \frac{q\phi_{bn}}{kT} + \frac{qV}{nkT} \qquad \text{-- (3.11)}$$

Thus, a semi-log J-V curve should be linear for thermionic emission and can be used to extract the barrier height, ideality factor, and saturation current density. The y-intercept

of the J-V curve gives the value of the saturation current density, J_s. The ideality factor, *n*, can be extracted from the slope using the equation (3.11).

$$n = \frac{\left(\frac{q}{kT}\right)}{\left(\frac{d \ln J}{dV}\right)} \qquad \text{-- (3.12)}$$

Knowing the value of saturation current, the barrier height can be calculated using the following equation:

$$\phi_{Bn} = \frac{kT}{q} \ln\left(\frac{A^{**}T^2}{J_s}\right) \qquad \text{-- (3.13)}$$

3.4.2 Extraction of parameters from C-V Measurements

The barrier height can also be determined from capacitance-voltage(C-V) measurements by measuring the variation of differential capacitance with applied reverse voltage. When a metal and semiconductor are brought into intimate contact, there is charge redistribution at the metal-semiconductor interface until thermal equilibrium is obtained. When a small ac voltage is superimposed on a dc bias, charges of opposite signs are induced in the metal and semiconductor respectively. For an n-type semiconductor, when a positive voltage is applied to the semiconductor with respect to the metal, the electric field attracts holes to accumulate near the interface in the semiconductor, and pushes the electrons to the end of the depletion region.

The depletion width, W, depends on the doping concentration, N_D, built-in voltage, V_{bi}, and the bias voltage, V. It can be expressed as:

.

$$W = \sqrt{\frac{2\varepsilon_s}{qN_D}(V_{bi} - V - \frac{kT}{q})} \quad \text{-- (3.14)}$$

where, N_D is the doping concentration, V_{bi} is the built in voltage, and V is the applied voltage. The depletion capacitance is given by [29]:

$$\frac{1}{C^2} = \frac{2(V_{bi} - V - kT/q)}{q\varepsilon_s N_D} = -\frac{2}{q\varepsilon_s N_D}V + 2(\frac{V_{bi} - kT/q}{q\varepsilon_s N_D}) \quad \text{-- (3.15)}$$

Therefore, the slope of a $1/C^2$ vs V curve is $-\frac{2}{q\varepsilon_s N_D}$, from which the value of the doping concentration can be extracted. The built-in voltage can be extracted from the intercept of the $1/C^2$ vs V curve. Knowing the value of doping concentration and the built-in voltage, the barrier height can be determined from [21]:

$$\phi_{Bn} = V_{bi} + \phi_n \quad \text{-- (3.16)}$$

where

$$\phi_n = \frac{kT}{q}\ln\frac{N_C}{N_D} \quad \text{-- (3.17)}$$

and N_c is the effective density of states at the conduction band edge. The junction capacitance is very important as it determines the switching speed of the devices, and

measurements of the capacitance can be used to extract important parameters of the Schottky diode.

3.4.3 Extraction of Series Resistance

The method for extraction of parameters from Current Voltage Measurements discussed in section 3.4.1 does not take into account the voltage drop due to series resistance of the device. Series resistance is due to the contact resistance, the probe tip resistance, and the bulk resistance of the diode. The effect of the Schottky diode series resistance is modeled with the series combination of a diode and a resistor R_s. The voltage drop across the diode is written as the voltage drop across the series combination of a diode (V_d) and a resistor ($I.R_s$) [20].

$$V_d = V - IR_s \qquad \text{-- (3.18)}$$

Therefore, equation (3.1) becomes:

$$J = J_s \exp\left[q \frac{(V - IR_s)}{nkT} \right] \qquad \text{-- (3.19)}$$

Substituting $J_s = A^{**} T \exp\left(-\frac{q\phi_{bn}}{kT} \right)$ in the above equation and solving for V we get equation:

$$V = R_s AJ + \frac{n}{\beta} \ln\left(\frac{J}{A^{**} T^2} \right) + n\phi_{Bn} \qquad \text{-- (3.20)}$$

where $\beta = \frac{q}{kT}$.

Hence, if we fit an equation of the form of equation 3.20 to the J vs V characteristic the ideality factor, barrier height, and series resistance can be extracted using [28],

$$V = aJ + b\ln\left(\frac{J}{A^{**}T^2}\right) + c \qquad \text{-- (3.21)}$$

From eq (3.20) and (3.21),

$$a = R_s A \;\; ; \; b = \frac{nkT}{q} \text{ and } c = n\phi_{Bn}$$

It is easy to see from the above expressions that the series resistance dictates the roll-over of the semilog J-V characteristics.

3.5 Conclusion

In this Chapter the different current conduction mechanisms operating in Schottky and ohmic contacts were reviewed. Methods were discussed to extract various electrical parameters such as ideality factor, barrier height, saturation current density, and doping concentration from J-V and C-V characteristics. These methods will be used in the next few Chapters to characterize fabricated 4H-SiC Schottky devices.

CHAPTER 4

DESIGN AND FABRICATION OF THE DIODE

Schottky diodes are of great commercial interest. They are used in several applications where fast switching time is important. They are used in MESFETS as gates to control the carrier flow from source to drain. SiC Schottky diodes can be used for high power and high temperature applications, and is of potentially important commercial device. Copper is a technologically important metal in the semiconductor industry. There are very few results for Cu contacts to 4H-SiC. Therefore, we have designed and fabricated Cu/4H-SiC Schottky diodes in order to explore the device characteristics. In this Chapter we present the design and fabrication of Cu Schottky contacts to 4H-SiC samples with a lightly doped n-type epilayer. Prior to the Schottky contact formation, Nickel ohmic contacts were deposited on to the substrate which had a higher doping concentration. In the first part of the Chapter we describe the design factors that were taken into account. Then we give a detailed description of the fabrication process we developed.

4.1 Design of the Schottky diode

The typical structure of a Schottky diode consists of a metal contact deposited onto an epilayer, a substrate, and a backside ohmic contact. The basic structure of a SiC Schottky diode is illustrated in Fig. 4.1. It consists of a semiconductor with an epilayer of lower doping concentration than that of substrate. The Schottky contacts are deposited onto the epilayer, while the ohmic contacts are formed with the substrate on the back side

of the sample. To form a good Schottky contact with low on-resistance, and good rectification at the same time, the epilayer doping has to be chosen on the order of 10^{16} cm^{-3} [41]. The reverse breakdown voltage and the series resistance due to the lower doping impose opposing constraints on the thickness of the epilayer. In order for the breakdown voltage to be high the epilayer thickness needs to be high, but for a low series resistance it needs to be low. To form good ohmic contacts, as discussed in section 3.3, the substrate should have a high doping concentration, on the order of 10^{18} cm^{-3} [42].

A typical I-V curve of an ideal Schottky diode is illustrated in Fig. 4.2. For low forward biases, the current increases exponentially with applied voltage, governed by thermionic emission. At higher applied voltages, the characteristics become linear as the series resistance takes over. In the reverse biased region, the leakage current increases and reaches saturation at relatively low reverse voltage. As the reverse bias is increased further, the current eventually increases exponentially due to avalanche breakdown. Avalanche breakdown occurs when the electric field is strong enough to accelerate free electrons to the point that, when they strike atoms in the material, they can knock other electrons free. The number of free electrons increases rapidly as generated electrons become part of the process. This is also known as reverse breakdown. The basic parameters of a Schottky diode illustrated in Fig 4.2 are, V_F, the forward drop for a given forward current, I_F, V_{WPR}, the working peak reverse voltage, I_{WPR}, the reverse current at V_{WPR}, and V_{BR}, the reverse breakdown voltage [30,31].

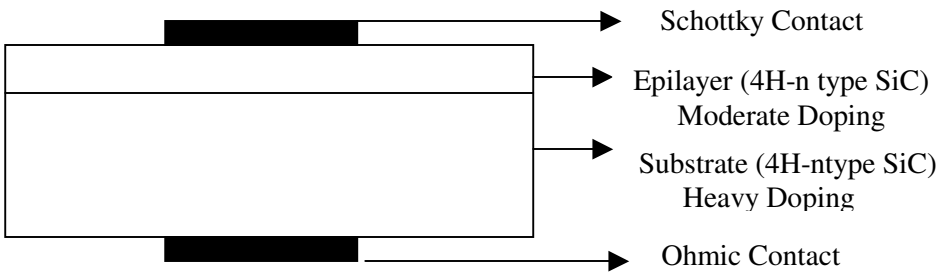


Fig. 4.1 Basic structure of a Schottky Diode

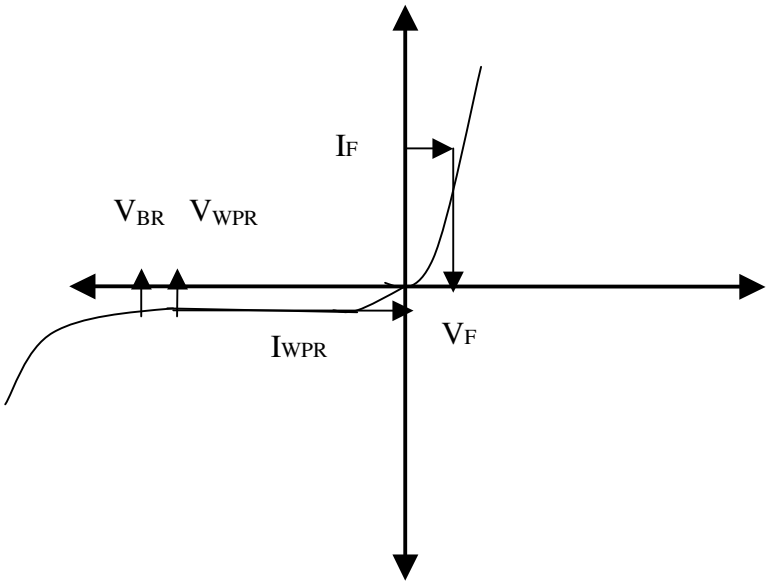


Fig. 4.2 Ideal I-V characteristics of a Schottky Diode

Schottky diodes are very attractive as high power devices. They have several advantages over pn junction diodes including very fast switching times, low forward voltage drop, and no reverse recovery time. The Schottky parameters and the design considerations are [31]:

1. Forward Voltage Drop (V_F): It is the voltage drop required for a specified current, I_F. The forward voltage can be expressed as a function of the barrier height and the series resistance [31]:

$$V_F = \frac{nkT}{q}\ln\left(\frac{J_F}{A^*T^2}\right) + n\phi_B + R_S J_F A \qquad \text{-- (4.1)}$$

In Equation (4.1), J_F is the forward current density, V_F is the forward voltage at that current, n is the ideality factor, R_S is the series resistance, k is the Boltzman's constant, T is the absolute temperature, A* is the Richardson's constant, and ϕ_B is the Schottky barrier height. For the forward voltage drop to be small, the series resistance has to be reduced. The series resistance R_S, can be written as [32]:

$$R_S = \left(\frac{W_{epi}}{q\mu_n N_{Depi}}\right) + \left(\frac{W_{sub}}{q\mu_n N_{Dsub}}\right) + R_{Ohmic} \qquad \text{-- (4.2)}$$

where W_{epi} and W_{sub} are the thickness of the epilayer and the substrate respectively, μ_n is the mobility of electrons, N_{Depi} and N_{Dsub} are the epilayer and substrate doping concentrations respectively, and R_{Ohmic} is the resistance of the Ohmic contact. Since the resistance of the highly doped substrate is negligible, the series resistance can be reduced by increasing the doping concentration of the epilayer, reducing the thickness of the epilayer, or reducing the resistance of the ohmic contact. However, we are limited in how much the epilayer doping can be

increased, as very high concentrations ruin the rectifying nature of the contact by increasing the tunneling probability.

2. Breakdown Voltage: The breakdown voltage depends on the Critical field and the doping density, and is given by [27]:

$$V_{br} = \frac{\xi_m W_{epi}}{2} \cong \frac{\varepsilon_s \xi_m^{\ 2}}{2qNd} \qquad \text{-- (4.3)}$$

where, ε_s is the semiconductor dielectric constant and ξ_m is the critical electrical field, which is defined as the electric field strength corresponding to the onset of bandgap ionization. Equation 4.3 implies that reducing the epilayer doping concentration increases the breakdown voltage; however, the critical electrical field might also change with doping concentration predicted by this 1st order model and nullify the effect [31].

3. Working Peak reverse voltage (V_{WPR}): This is the maximum reverse voltage for the maximum reverse current before breakdown occurs. This is specified in order to know the working voltage range of the diode [32]. It is defined as the highest value of the reverse voltage at which the device can operate.

4. Switching time: In order to provide quicker switching times, an n-type semiconductor is chosen since the electron drift velocity is greater than that for holes at a given field. The reverse recovery time of Schottky diodes is extremely

small. The short reverse recovery time these devices may exhibit is primarily dictated by their capacitance, rather than minority carrier recombination as in conventional p-n junction rectifiers. This characteristic provides very little reverse current overshoot when switching the Schottky diode from the forward conducting mode to the reverse blocking mode [32].

5. Power Dissipation: The power dissipation in a Schottky diode can be reduced by reducing the leakage current. In the reverse direction there is a small *leakage current* at voltages below the reverse *breakdown voltage*. So, the leakage current needs to be minimized for improved rectification, as well as reduced power dissipation (I^2R).

4.2 Fabrication of the Diodes

4.2.1 Starting Materials used

The diodes were fabricated using 0.25"x0.25" 4H-SiC samples sawed from a 2 inch wafer with Si face, which were purchased from Cree, Inc. The 4H polytype was chosen due to its high electron mobility. Nitrogen was the dopant for the substrate and the epilayer. In order to make good ohmic contacts, the n-type substrate chosen had a high doping concentration of $4.8 \times 10^{18} cm^{-3}$. The wafers had 5μm thick epilayers with a doping concentration of $5.0 \times 10^{15} cm^{-3}$, on which the Schottky contacts were deposited. To remove the impurities introduced during the wafer dicing process and also the native oxide layer, surface cleaning was performed at several points in the process. Before going

into the details of the process-steps, the objective at every step and the rationale behind the flow, the materials used, the techniques adopted with the subsequent steps in mind are briefly presented first. A schematic representation of the process flow is presented in Fig 4.3.

Process Overview:

1) Initial surface clean using HF to degrease and remove any native oxide layer, in preparation for the ohmic contact deposition.
2) Deposition of Nickel onto the backside of the sample, which has been shown to make good ohmic contacts with highly doped n-type 4H-SiC. This was done by evaporating a Nickel wire inside a vacuum chamber to prevent oxidation.
3) Annealing the deposited Ni to reduce the contact resistance, which can be explained in terms of Nickel silicide formation. This high temperature step required that the Schottky contacts be deposited later.
4) Similar to the initial surface clean, the preparation of the front surface (epi) for Schottky contact deposition involved cleaning with HF to remove any oxide layer that might have formed during the deposition and annealing of the Ni contacts. To prevent the HF from etching away the Ni ohmic contacts, a sacrificial protective layer of Aluminum was deposited by thermal evaporation on to the backside. Aluminum was chosen for its ease of deposition by evaporation and also its ease of removal by KOH without affecting the underlying Nickel contacts. This is because Nickel is chemically resistant to KOH [44].

5) Deposition of Copper on to the epilayer to form Schottky contacts, using an evaporator.
6) Removal of the sacrificial Al coating from the backside of the sample using KOH. Similar to step 4, this required a protective layer for the Cu contacts on the frontside, for which purpose, nail paint was sufficient.
7) Acetone, the primary component in nail polish removers, was used to remove the protective coating for the Schottky contacts without affecting the Copper or Nickel contacts.

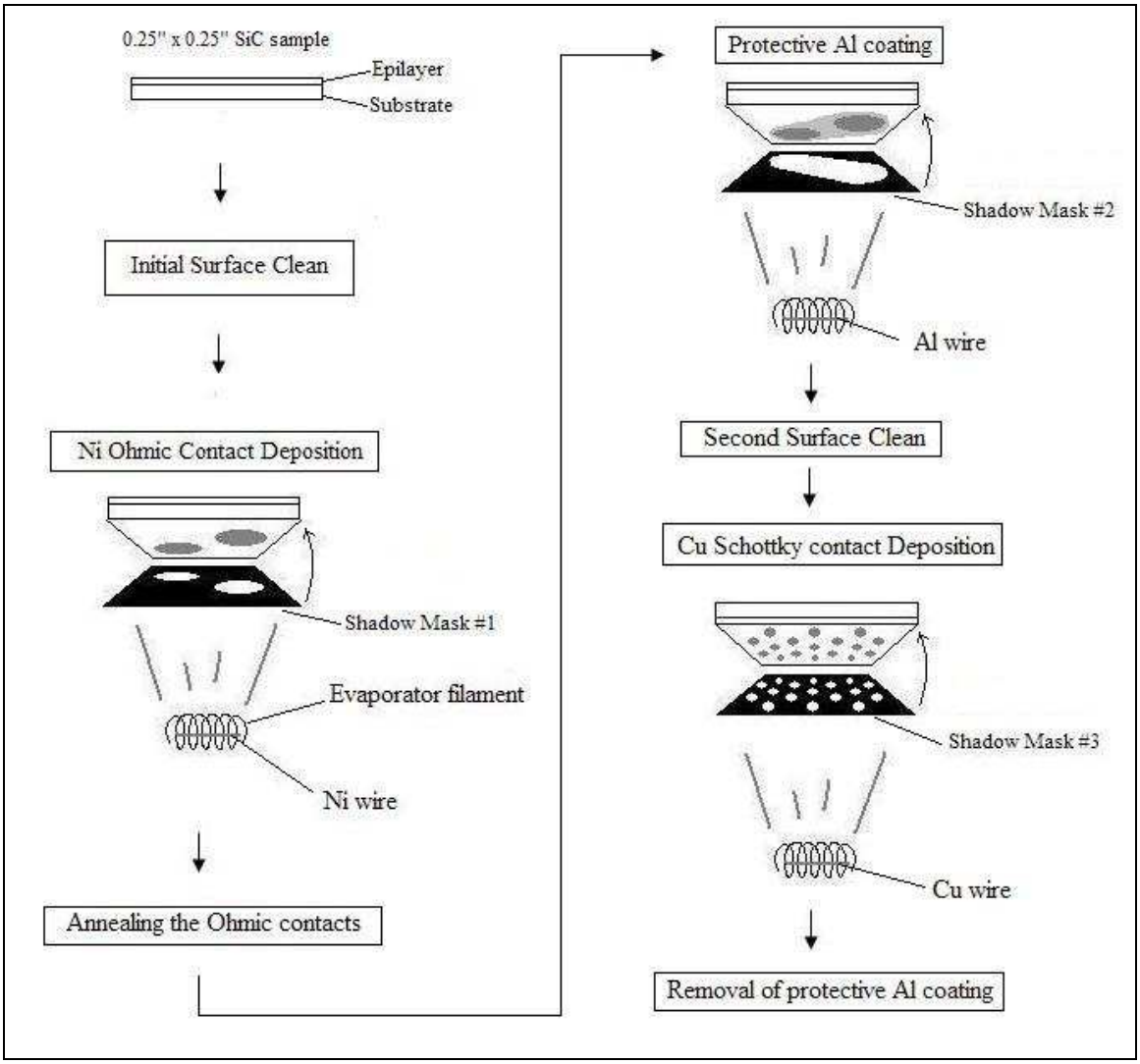


Fig 4.3 Overview of the process steps

4.2.2 Initial Surface Clean

This cleaning step was done in a class 100 clean room. Each SiC sample was degreased in acetone for 2 minutes and methanol for 2 minutes. The acetone and methanol were rinsed off by dipping the sample in a beaker of DI water for 6 minutes after each step. Then they were dipped in a solution of diluted HF (48%), consisting of

H_2O:HF (25:1), for 2 minutes to remove any native oxide. The samples were triple rinsed in DI water for 6 minutes, using 3 beakers containing DI water. The samples were rinsed in the first beaker for a minute to quickly rinse off most of the acid. Subsequent rinsing was performed in a second beaker for about 2 minutes and in the last beaker for 3 minutes. The samples were dried using a Nitrogen gun. As a result, samples with chemically clean surfaces were obtained.

4.2.3 Fabrication of Ohmic Contacts

Following the cleaning sequence, approximately 1700 Å of nickel was deposited on the back side of the samples using a vacuum evaporator at a pressure of 5 $x10^{-6}$ Torr. Nickel is a very popular ohmic contact metal to n-type SiC due to its reproducibly low contact resistance and good temperature stability [43, 44]. A shadow mask (#1) was used to deposit the Nickel dots as shown in Fig 4.4. Two contacts were deposited, to enable the measurement of the resistance of the ohmic contacts. The reason for this particular design of the ohmic contacts is elaborated upon in section 4.2.4.1. A Nickel wire of 2mm diameter and 17mm length was placed inside the filament of the evaporator. The sample was placed on the shadow mask, which rested on a holder at a height of 75mm above the filament. The amount of Nickel wire used and the distance to the sample were the parameters with which the thickness of the contacts was controlled. These specifications were calculated using a simulation program which uses the type of metal, the diameter of the wire and the desired thickness as inputs.

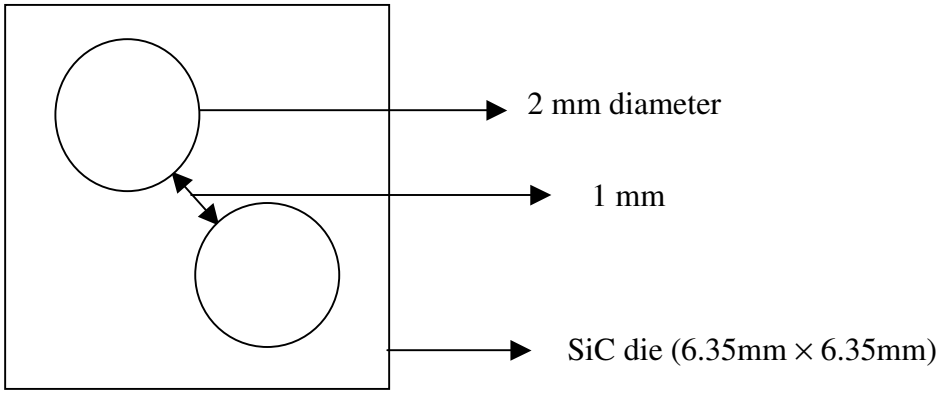


Fig. 4.4 Pattern of Ohmic contacts

The as-deposited Ni contacts were annealed at 1000°C for 3 minutes to minimize contact resistance. Annealing results in the formation of Nickel Silicide at the interface. Recent studies show that formation of Nickel Silicide results in free Carbon. This amorphous carbon transforms into conducting graphite like structures at around 900°C. This process is attributed to the formation of ohmic contacts at these temperatures [33]. The schematic of the annealing furnace and the heating and cooling sequences for the sample are illustrated in Fig 4.5. The furnace has three zones, the front, center, and end zones, with the center being the hottest. The sample was placed on a quartz boat and gradually pushed into a quartz tube running along the axis of the furnace, using a quartz rod. The high temperature at which the Nickel contacts are annealed makes them highly susceptible to oxidation. To prevent this, the quartz tube was continuously purged with forming gas (10% H_2 with Argon balance). The reason the sample had to be gradually

pushed into the furnace was to avoid stressing it by a sudden application of high temperature (1000ºC). It was also very important that after annealing, the sample was not exposed to the atmosphere while it was still hot. So, they had to be pulled out slowly and left to cool near the front end, with the forming gas still flowing and the furnace turned off. During the whole process the front end of the quartz tube was covered by an end-cap made of Aluminum foil. A hole was made in the end-cap to move the sample in and out with the quartz rod.

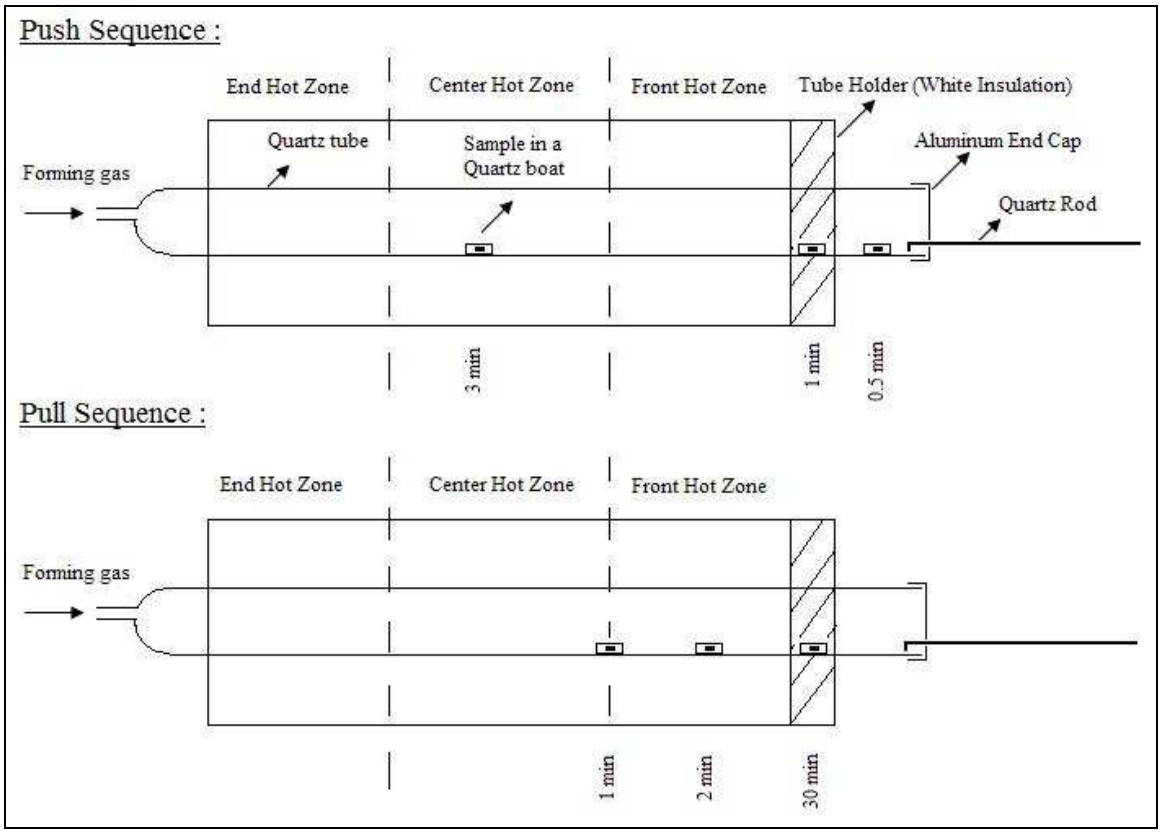


Fig 4.5 Schematic of the Annealing Furnace.

Details of the Annealing Sequence:

1. The temperature reading on the front panel of the furnace should be 1040^{o}C. Nickel ohmic contacts are required to be annealed at this high temperature in order to form good ohmic contacts.
2. Forming gas (10% H_2 +Argon balance) was injected into the oven at a flow rate of about 35ml/second.
3. Let the gas flow 3 minutes to purge the quartz tube, before putting in the samples.
4. The die was then heated slowly by incrementally pushing it to various locations in the furnace for various set times:
    a. 30 seconds at the front edge of the tube.
    b. One minute at the center of the tube holder (This is the white insulation part, before the tube enters the furnace).
    c. Finally the sample was pushed slowly through the front hot zone into the center hot zone.
5. Annealing Time: 3 minutes in the center of the hot zone.
6. After annealing in the hot zone, the die was allowed to cool slowly, with the forming gas still flowing, by pulling it out slowly, incrementally in the opposite manner as the heating process:
    a. 1 minute @ the boundary between the front hot zone and center hot zone
    b. 2 minutes @ the center of the front hot zone
    c. 30 minutes @ the center of the tube holder

After several trials which resulted in oxidized contacts, we arrived at this push-pull sequence which repeatedly produced unoxidized ohmic contacts with very low contact resistances. I-V measurements were made to test these contacts. The voltage between the two ohmic contacts was swept from -5V to +5V and the current was measured. This resulted in linear I-V characteristics, passing through the origin. The slope of this line was used to calculate the resistance of the ohmic contact. The resistance of the ohmic contacts typically was around 6 ohms. Such low resistance and linear I-V characteristics imply that these are good ohmic contacts.

4.2.4 Process developed for the Second Surface Clean

In order to remove any oxide layer that might have formed on the SiC surface, or any other contamination during Nickel deposition and anneal, a second surface clean was performed on some of our samples which was similar to the first. Five samples were fabricated. Samples I and II did not receive this second surface clean. Samples III, IV and V received this second surface clean. The process involved in this second clean was complicated and is described in detail here. This second clean improved the characteristics of our diodes considerably, as will be shown in a later Chapter. The annealing of the ohmic contacts makes the front surface of the diode susceptible to oxidation as well as exposes it to the atmosphere. This was established by comparing the characteristics of diodes which had a second surface clean with those which did not have a surface clean just prior to Schottky contact deposition. An elaborate process technique

was required to protect the ohmic contacts from being affected by the second surface clean.

4.2.4.1 Protective aluminum coating

The two ohmic contacts were 2mm in diameter separated by 1mm. To deposit a protective coating of Aluminum over these contacts, a shadow mask (#2) with an aperture enclosing both dots, with at least one 1mm overlap on all sides, was used. The pattern of Nickel contacts and Aluminum layer is shown in Fig 4.6. An Aluminum wire of diameter 2.5 mm and length 10 mm was used. Inside the evaporator, where the deposition was performed, the shadow mask was positioned 73 mm from the filament holding the Aluminum wire. At the end of the evaporation process all the aluminum had evaporated without leaving any residue on the filament. The amount of Aluminum used and the height of the metal from the sample ensured that the thickness of the deposited layer was close to 0.5 μm. This step was actually preceded by a trial with a glass plate. The thickness of Al deposited on the glass plate was measured using a Dektak Profilometer, and was found to be 0.464um on average. The sample was allowed to sit for 24 hours for the Aluminum to adhere to the surface. The reason the Nickel contacts were deposited diagonally was because this made the design for the shadow mask easier. Also the samples which were only 0.25 x 0.25 in size could be easily seated on the mask.

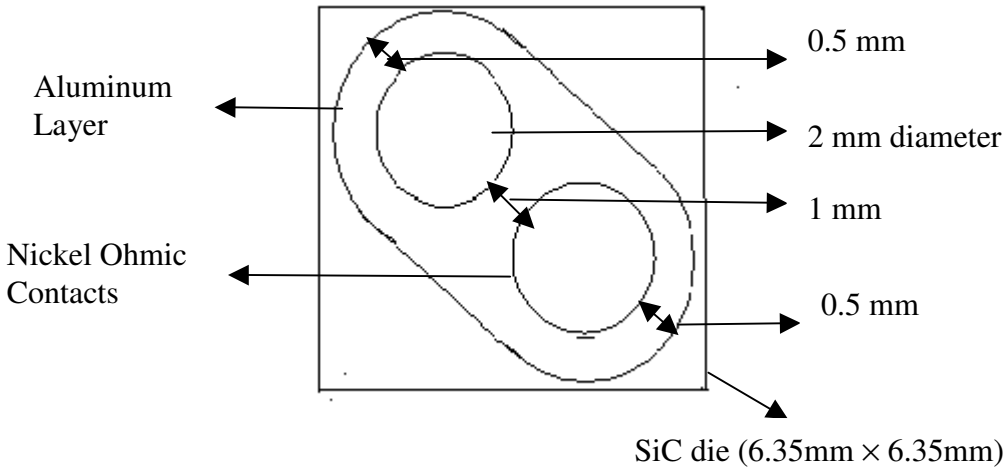


Fig. 4.6 Pattern of Ohmic contacts and the protective Aluminum layer

4.2.4.2 Second Surface Clean

The second surface clean was a very tricky procedure. Even though the chemicals used were the same as those used in the first surface clean, the HF etch had to be performed very carefully, without etching away much of the aluminum, so that the underlying Ni ohmic contacts stayed intact. The procedure adopted is as follows:

1. First, each sample was degreased in acetone for 2 mins and methanol for 2 mins.
2. Then the samples were rinsed in DI water for 6 mins after the acetone degrease and the methanol degrease.
3. The HF etch to remove any native oxide was performed by floating the sample for 2 minutes in a HF solution, with the front surface facing down to make sure the Nickel ohmic contacts were not affected. The solution consisted of one part 48% HF, diluted with 25 parts water. If a sample accidentally started immersing in the

HF, then it was quickly removed and rinsed in DI wafer. Water sticking to the front surface was an indication of the presence of an oxide. So the samples were floated in the HF solution and rinsed with DI water repeatedly until the water did not stick to the front surface of the sample. This HF etch took about 1-2 minutes depending on the thickness of the oxide formed after annealing. At the end of this step, usually some of the Aluminum was lost due to HF etch, but there was enough left protecting the underlying Ni contacts from the acid.

4. The samples were triple rinsed in DI water for 6 minutes, using 3 beakers containing DI water. The samples were rinsed in the first beaker for 1 minute to quickly rinse off most the acid, then in a second beaker for about 2 minutes and in the last beaker for 3 minutes. This was done to avoid the residual acid from etching the metals further.
5. The front surface was dried using a Nitrogen gun.

4.2.5 Schottky contact deposition

After the front surface was cleaned, Copper Schottky contacts were evaporated onto the epitaxial layer through a shadow mask (#3), at a pressure of 5 x 10^{-6}Torr. The shadow mask had 14 Copper dots and the pattern of the dots achieved is shown in Fig 4.7. Deposition of Copper by evaporation was difficult compared to that of Al or Ni, as Copper is a heavier metal and tends to form a melt and fall from the filament if not heated carefully. We used two filaments and two pieces of Copper wire to achieve Copper contacts with maximum thickness. The thickness we attempted to achieve was 0.46 um.

The two pieces of Copper each were supposed to contribute 0.23um of Copper. The two filaments each had a 45 mm long Cu wires of diameter 0.5mm, and were placed at a height of 46 mm from the sample. Since most of the Copper evaporated from the filaments, the thickness achieved was close to 0.46µm. The average diameter of the Schottky contacts was 630 µm, and fourteen diodes were fabricated on each 4H-SiC sample. Three Gold dots of average diameter 630 µm and of thickness 0.5 µm were deposited as a control and for comparison. The sample was cured for 2 days inside the clean room so that the contacts could adhere to the surface before any further processing was done.

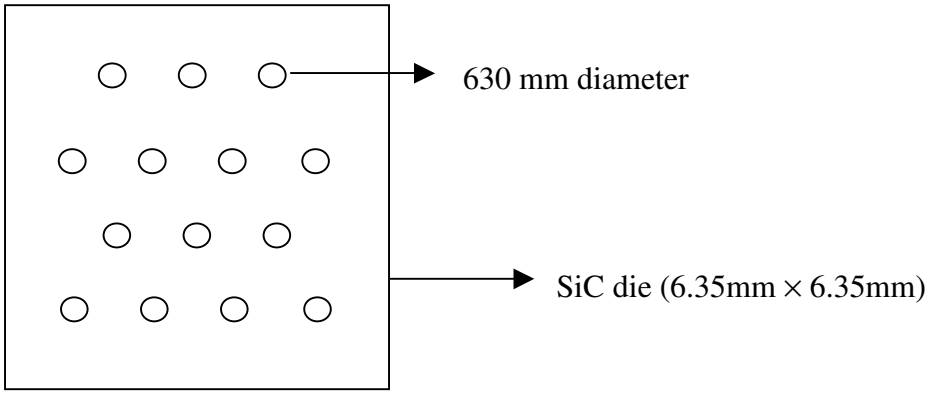


Fig. 4.7 Shadow mask for Schottky contact deposition

4.2.6 Removal of protective Aluminum layer

1. The Aluminum protective coating needed to be removed from the samples before electrical measurements could be performed. In order to make sure that the Aluminum removal process did not affect the Copper Schottky contacts a coating

of nail polish was deposited on them. To make sure all the contacts were properly coated with the nail-paint, the coating was performed with the help of a microscope. The nail-paint was allowed to dry for 2 hours.

2. The samples were rinsed with KOH until all the Aluminum dissolved. This took about 60 secs. Then the samples were rinsed in 3 beakers of DI water, for 1, 2 and 3 minutes, similar to the triple rinsing step following the HF oxide etch.
3. The nail paint was removed using acetone. The samples were immersed in acetone until the nail paint fully dissolved. This took about 3 mins.
4. Finally, the diode was rinsed in de-ionized water for 6 mins using the triple rinse technique described earlier.

4.3 Conclusion

In this Chapter we reviewed the detailed procedure involved with the design and fabrication of the SiC Schottky diode. Each step in the fabrication process played a critical role in the performance of the diodes. Results of electrical characterization of the fabricated diodes are presented in Chapter 5. The impact of the second surface clean, before depositing the Schottky contacts, is discussed in detail in Chapter 6. Results of the electrical characterization of the fabricated diodes are presented in Chapter 5.

CHAPTER 5

DIODE CHARACTERIZATION

In this chapter, we discuss the results of Current-Voltage (I-V) and Capacitance-Voltage (C-V) measurements performed on samples III, IV and V, which received a second surface clean. Each sample had 14 Copper-Schottky contacts. The electrical parameters extracted from the I-V and C-V curves, such as the ideality factor (n), barrier height (ϕ_B) and the reverse saturation current density, characterize the performance of these diodes.

5.1 I-V Characteristics

5.1.1 Equipment and Procedure

A Micromanipulator probe station and a HP4156B parameter analyzer were used to obtain the I-V characteristics of the diodes. The sample was loaded on the chuck of the micromanipulator. A vacuum pump was used to create suction to hold the sample tightly to the chuck, so that the Nickel ohmic contacts on the backside of the sample could make electrical contact through the chuck. The micromanipulator setup was enclosed in a vibration-isolation chamber.

The I-V characteristics of these diodes were studied at both forward and reverse voltages. Typically, the forward bias on all diodes was ramped up to 4 Volts, with the current compliance set to 100mA. The Source and Measure Unit (SMU) of the HP4156B can limit the current to prevent damaging the device under test. This limit, specified as the Current-Compliance, has a maximum value of 100mA on the HP4156B parameter

analyzer [45]. The sampling interval was set to 16.67ms by choosing the medium integration-time setting on the analyzer. The reverse bias on all diodes was ramped to 10 Volts to observe the reverse leakage current. Since many of the diodes had very good reverse blocking characteristics, some of the diodes were stressed to a reverse bias of 100 Volts in order to obverse the leakage current. Such high breakdown voltage is expected in SiC, as discussed in section 2.2.

5.1.2 Group A and B - Overview

Two classes of forward I-V characteristics emerged from measurements on the 42 diodes from samples III, IV and V. One group of diodes exhibited forward I-V characteristics typical of Schottky diodes, with a single linear region for almost 8 orders of magnitude on the semi-log plot, and is referred to as Group A. The other group exhibited two linear regions, parallel to each other, and is referred to as Group B. The characteristics of two diodes from Sample III, representing Groups A and B are illustrated in Fig 5.1 using solid and dotted lines, respectively. It can be observed that the Group A and Group B currents are similar at forward biases higher than 0.8V, while at lower forward biases, the Group B current is higher. The curves start to roll off due to series resistance just above a forward bias of 1V. Both the diodes reached a current compliance of 100 mA (J = 320 mA/cm^2) at about 1.8V of forward bias. The following sections discuss the modeling of these diodes based on thermionic emission theory.

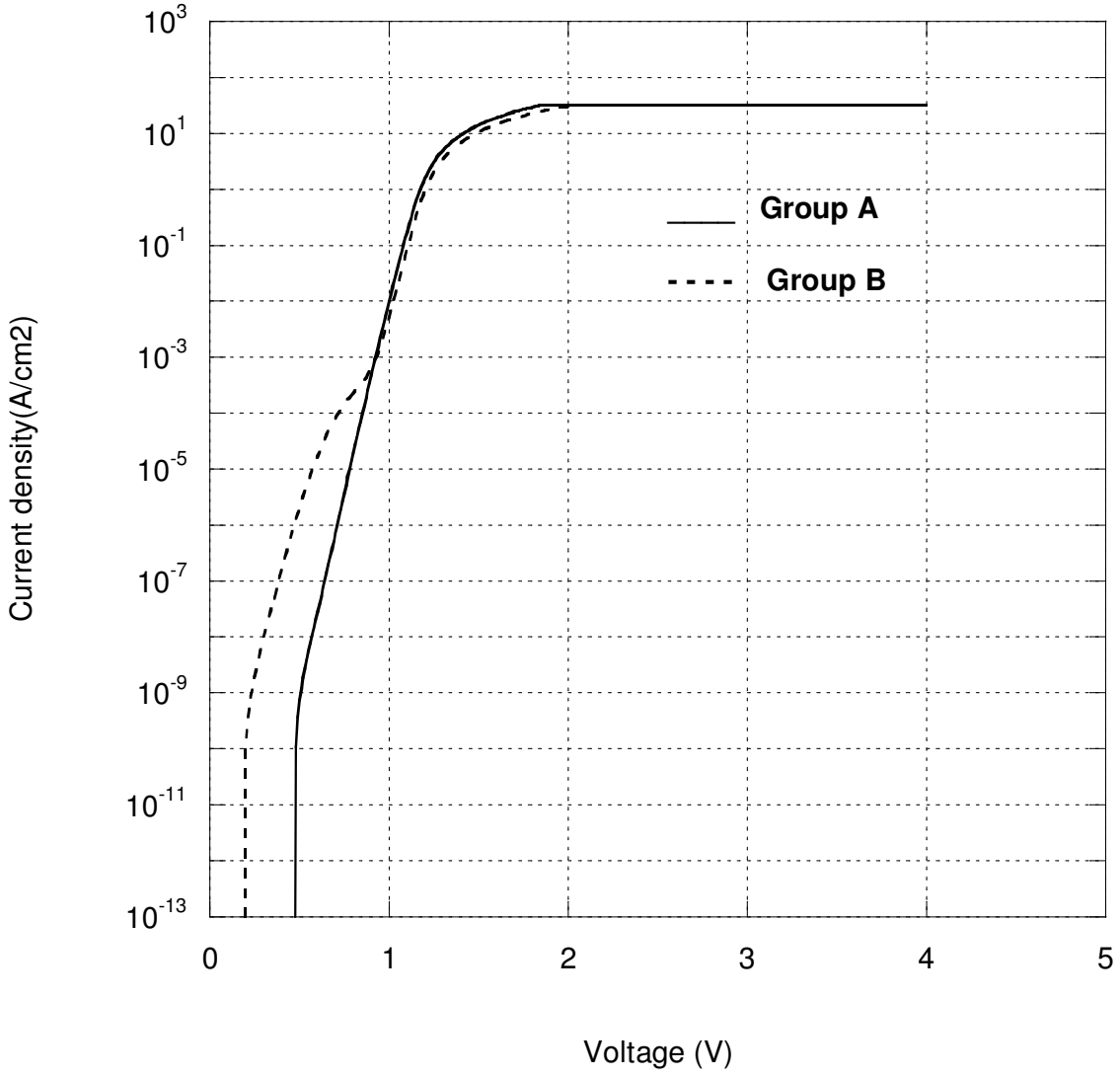


Fig 5.1 Forward I-V characteristics: Group A vs. Group B

5.1.3 Group A : Forward I-V Characteristics

In this section we analyze the forward I-V characteristics of 32 diodes which exhibited Group A characteristics. The semilog I-V curves of 15 diodes representing this group are shown in Fig 5.2 for forward biases in the range of 0V to 4V. For forward bias

voltages less than 0.5V the currents were very low in the sub-nA range, resulting in zero or negative measured values, which was mostly noise. Such values have been overridden to 1fA, since the Kaleidagraph software used to plot these curves accepted only positive values for a semilog graph. For forward biases in the range of 0.5V to 1.1V, all Group A diodes have a linear region of almost 8 orders of magnitude. For forward biases higher than 1.1V, series resistance began to dominate and the curves started rolling off until they hit compliance at about 1.8V. The tight distribution of these curves indicates that the process was well controlled.

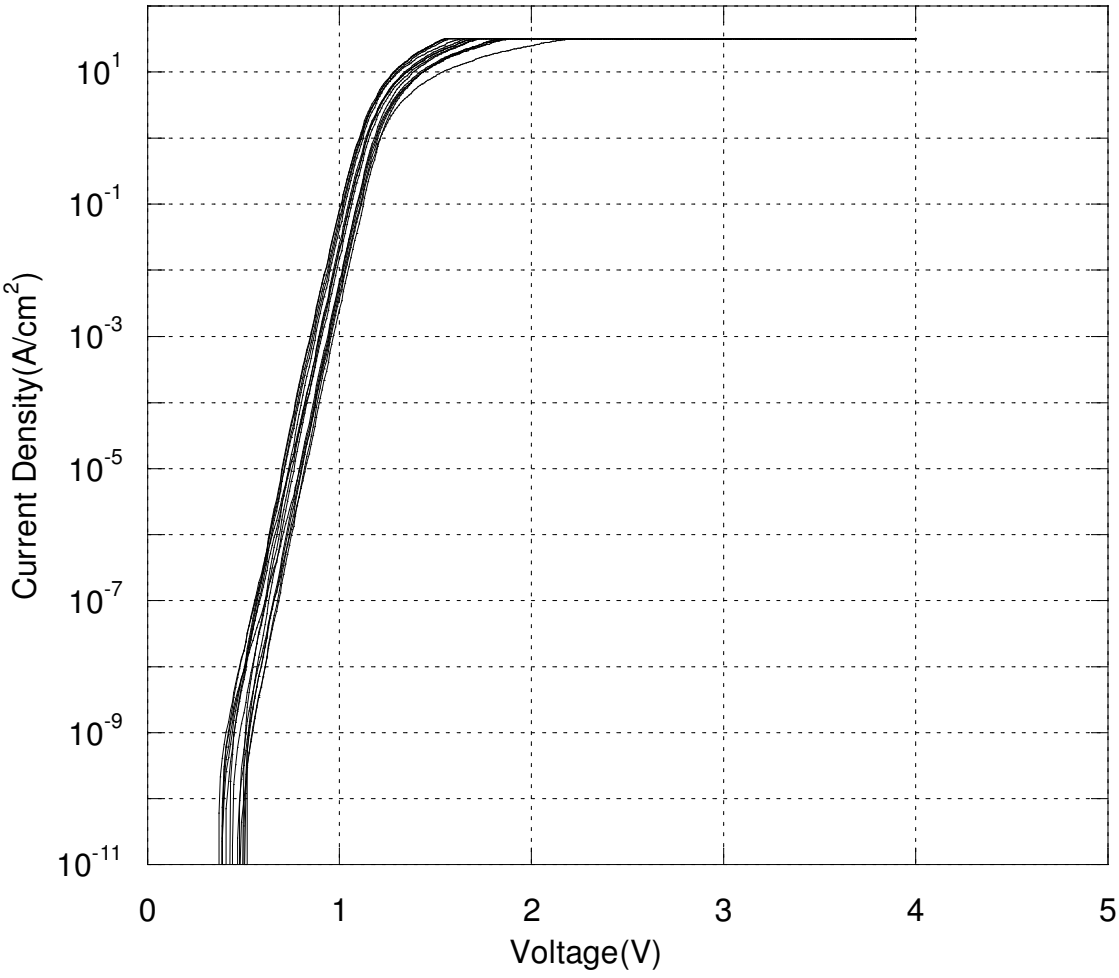


Fig 5.2 Group A : Forward I-V Characteristics

For an ideal Schottky diode the carrier transport over the barrier is governed by thermionic emission. The current density, J, is given by the Richard-Dushman equation,

$$J = A^{**}T^{2}\exp\left(\frac{q\phi_B}{kT}\right)\exp\left(\frac{qV}{nkT}\right) \qquad \text{-- (5.1)}$$

In order to analyze the electrical characteristics, the ideality factor, n, and the Schottky barrier height, ϕ_B, were extracted using the Richard-Dushman equation [27]. The value of

A^{**}, the effective Richardson's constant, is taken as 146 A/K^2cm^2 for 4H-SiC [10]. Thermionic emission predicts linear characteristics on semi-log *J-V* curves for forward voltages. The constant term, '1', is omitted from the argument of the second exponential in Equation 5.1, since we are analyzing the characteristics only for values of forward voltages greater than *3KT/q* [34, 35]. Equation 5.1 can also be written as:

$$J = J_s \exp\left[\frac{qV}{nkT}\right] \qquad \text{-- (5.2)}$$

where the reverse saturation current density, J_s, is given by:

$$J_s = A^* T^2 \exp\left(-q\phi_B / kT\right) \qquad \text{-- (5.3)}$$

Equation (5.2) was used to model the observed *J-V* characteristics. The procedure used to extract the ideality factor and the barrier height is illustrated using the first diode from Sample III as an example. The linear region in the forward semilog I-V characteristic of this device is presented in Fig 5.3. The current density for the forward bias range of 0.6-1.0 V was modeled with an exponential fit, given by the equation in Fig 5.3. The correlation coefficient for this fit is 0.9981, which is very close to unity. This indicates good exponential behavior in this region. The *y*-intercept of the linear region of the semi-log curve is the reverse saturation current density J_s. The value of barrier height extracted for this device, using Equation 5.3, is 1.42 eV, which is very close to the Schottky-Mott limit, 1.1 eV for Cu/4H-SiC. The ideality factor, *n*, determined using Equation 5.2, is 1.16, which is close to unity. Thus this diode behaved as a good Schottky

rectifier following thermionic emission at forward biases. The results for all the Group A devices is tabulated and discussed later in this chapter.

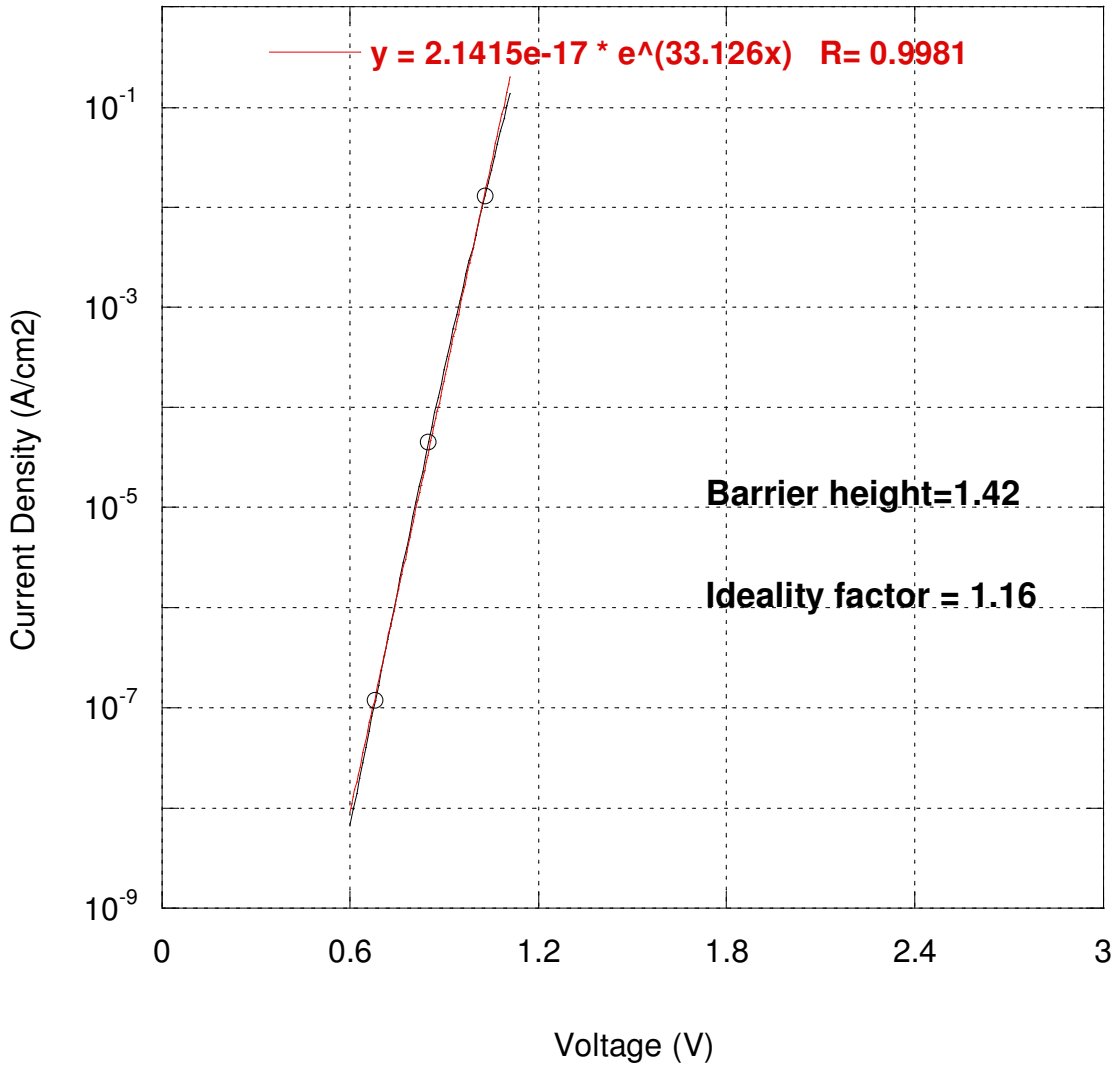


Fig 5.3 Group A : Extraction of Electrical Parameters

5.1.4 Group B : Forward I-V Characteristics

Some of the diodes from samples III, IV and V exhibited anomalous I-V characteristics that could not be explained by standard thermionic emission theory. As described in section 5.1.2, two linear regions could be observed on the semi-log I-V curves for 13 devices, and we refer to this set of devices as Group B. The forward I-V characteristics of the Group B devices have been presented together in Fig 5.4. It can be observed that the I-V curves for all devices are tightly distributed and linear for forward biases in the range of 0.8V to 1.2V. For forward biases less than 0.8V, the curves deviate from this linear trend at different voltages for different devices. A second linear region, parallel to the first one can be noticed at low forward voltages. In this section, we refer to the first linear region observed at high forward voltages as the HVLR (High Voltage Linear Region) and the second linear region observed at low forward voltages as the LVLR (Low Voltage Linear Region). The LVLR has a higher current level than what would be expected from the thermionic emission model fitted to the HVLR.

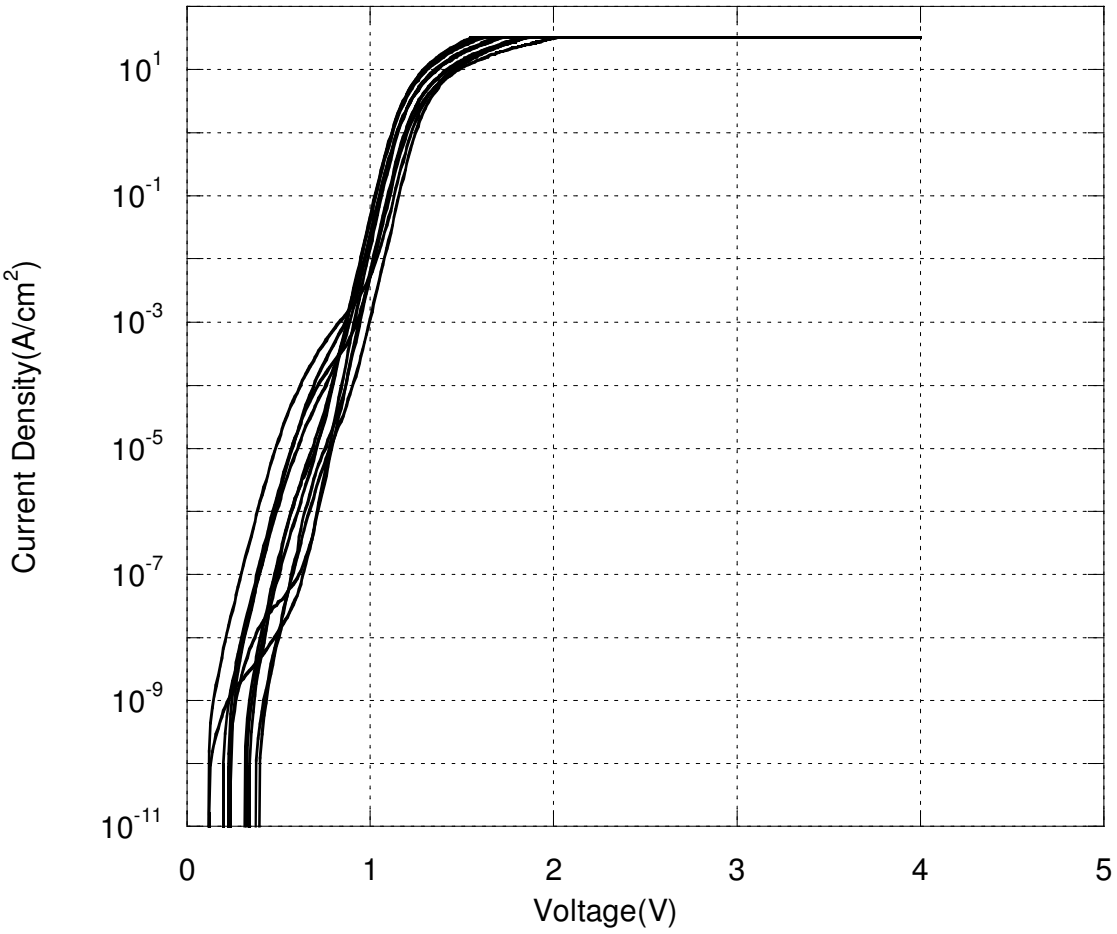


Fig 5.4 Forward Characteristics of Group B devices.

In section 3.4.1, we discussed the extraction of ideality factor and barrier height from forward I-V characteristics. From equations 3.12 and 3.14, we can see that the slope of the linear region of the semi-log I-V curve varies as the inverse of ideality factor, while the y-intercept varies as the inverse of barrier height. The LVLR and HVLR are parallel to each other, which indicates that the ideality factors associated with the two regions are similar. However, the y-intercept of LVLR is higher than that of the HVLR.

From this observation, we can infer that the barrier height associated with the LVLR is smaller than that associated with the HVLR.

The Group B behavior can be explained by a model with two diodes of different barrier heights connected in parallel [36]. The main idea behind this model is that a very small fraction, ε, of the Schottky contact area, A, exhibits a barrier height lower than that characteristic of the bulk of the contact. This is most likely due to inhomogeneities in the SiC epilayer. The equivalent circuit of this model is presented in Fig 5.5 [36]. The fraction of the contact area exhibiting the lower Schottky barrier height (LSBH) is represented by the smaller diode, identified by its ideality factor and barrier height, n^L and $\phi_b{}^L$, respectively. The rest of the contact area is represented by the larger diode, with ideality factor, n^H, and the higher Schottky barrier height (HSBH), $\phi_b{}^H$. Each diode is connected in series with its corresponding epilayer and substrate resistances. In Fig 5.5, R_c is the material resistivity ($\Omega.cm^2$), expressed in terms of the thickness, doping density, and the electron mobilities of the epilayer and substrate, in Equation 5.4.

$$R_c = \frac{W_{epi}}{q\mu_{nepi}N_{Depi}} + \frac{W_{sub}}{q\mu_{nsub}N_{Dsub}} \qquad \text{-- (5.4)}$$

The LSBH area, εA, is very small and corresponds to a larger resistance, $R_c/\varepsilon A$, shown in series with the LSBH diode. The series resistance of the larger HSBH area, $R_c/(1-\varepsilon)A$, is relatively small. The probe tip resistance, R_p, is connected in series common to both diodes.

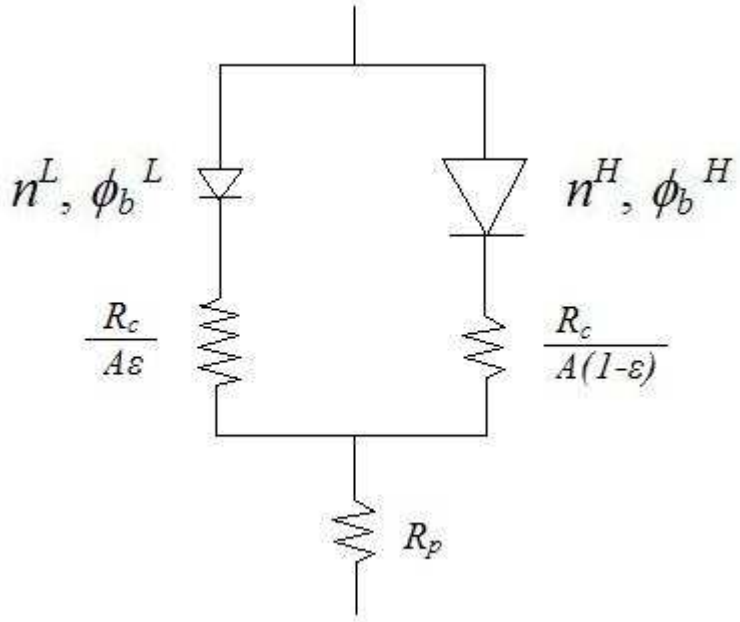


Fig 5.5 Parallel diodes model for Group B devices [36].

According to this model, the total forward current through the device must be equal to the sum of the currents through the individual diodes. To understand how the combined effects of the barrier height and area of the two diodes result in the Group B forward I-V characteristics, the individual contributions of the diodes are analyzed using Equation 4.1. Equation 4.1 can also be written in terms of the forward current instead of the current density as,

$$V_F = \frac{nkT}{q}\ln(I) + \left(\frac{R_c}{A} + R_p\right)I + n\phi_B - \frac{nkT}{q}\ln\left(AA^*T^2\right) \qquad \text{-- (5.5)}$$

where, $I = J_F{}^*A$, and $R_S = \frac{R_c}{A} + R_p$. Separating the logarithmic, linear and constant terms in Equation 5.5 allows us to draw two important conclusions. First, a change in the

barrier height simply shifts the I-V characteristics along the voltage or the x-axis. The second conclusion is that the area of the diode determines the onset of the resistive region in the I-V characteristics. These results are used to model the behavior of one of the Group B devices from Sample III. The forward semilog I-V characteristic of this device is presented in Fig 5.6 as a dotted line. The two solid straight lines are the extrapolated LVLR and HVLR regions. At forward voltages less than 0.5V, the thermionic current through the LSBH diode is much higher than that through the HSBH area. Thus, even with a small area, the LSBH area dominates the I-V characteristic at such low forward biases, because of its lower barrier height. So, the LVLR region can be modeled using Equation 5.5, with only the LSBH diode in series with $R_c/\varepsilon A$ and R_p as,

$$V = \frac{n^L kT}{q}\ln(I) + \left(\frac{R_c}{A\varepsilon} + R_p\right)I + n^L\phi_b^L - \frac{n^L kT}{q}\ln\left(A\varepsilon A^* T^2\right) \qquad \text{-- (5.6)}$$

As the forward voltage increases, the large epilayer resistance associated with the small LSBH area limits its contribution to the total forward current. This causes the first roll-off, which can be seen in the range of 0.5-0.8 V, for the device represented in Fig 5.6. With further increase in the forward bias, the thermionic current through the HSBH area exceeds the LSBH current, and completely takes over the I-V characteristic at approximately 0.9 V. Thus, the HVLR region can be modeled with only the HSBH diode in series with $R_c/(1-\varepsilon)A$ and R_p as,

$$V = \frac{n^H kT}{q}\ln(I) + \left(\frac{R_c}{A(1-\varepsilon)} + R_p\right)I + n^H\phi_b^H - \frac{n^H kT}{q}\ln\left(A(1-\varepsilon)A^* T^2\right) \qquad \text{-- (5.7)}$$

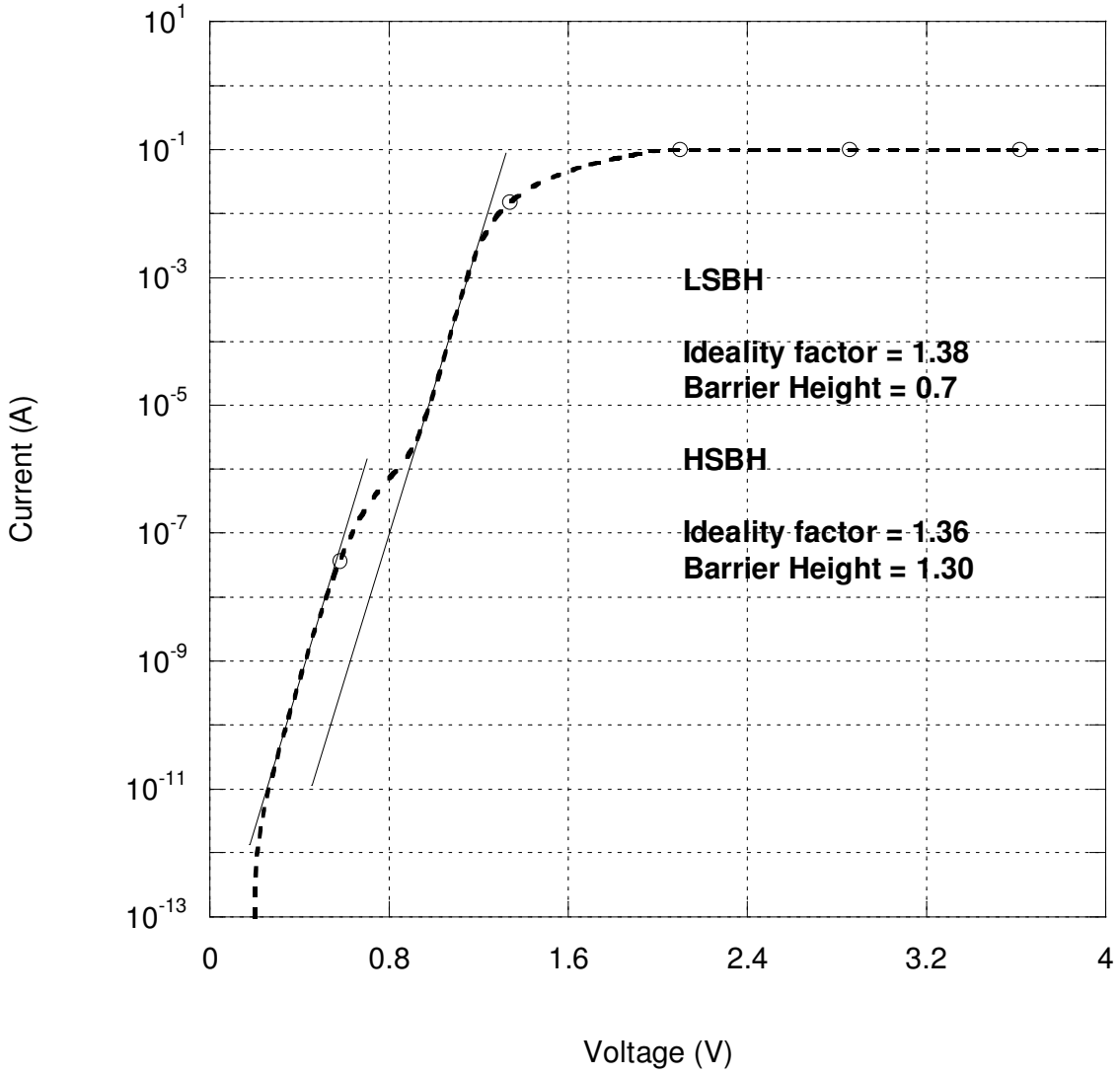


Fig 5.6 Extraction of parameters for a Group B device.

The procedure for the extraction of Group B parameters is outlined below, using the same device as an example. The details are included in Appendix I.

1) First, a linear model of the form $y = m1 + m2 * M0$, is fitted to the I-V data from the forward bias range of 1.5V to 1.9V. Here *y* is the forward current and *M0* is the

applied forward bias. The inverse of the slope of this fit, *1/m2*, gives the effective series resistance. The epilayer and substrate component of the series resistance, R_c/A, is calculated from Equation 5.4, using the electron mobility value for 4H-SiC from Table 2.1. This is subtracted from the extracted total resistance to obtain R_p, the probe tip resistance (in effect, the total of all resistances external to the device).

2) Next, the general form of equation 5.6,

$$y = m1 * \ln(M0) + m2 * M0 + m3, \qquad \text{-- (5.8)}$$

is fitted to the LVLR. Here y is the applied forward voltage and M0 is the forward current. The parameters n^L, ε, and $\phi_b{}^L$, which characterize the LSBH area, are then obtained by equating the coefficients *m1*, *m2* and *m3* to the corresponding terms in Equation 5.6.

3) Finally, the HSBH parameters, n^H and $\phi_b{}^H$, are obtained similarly, by fitting Equation 5.8 to the HVLR, and equating the coefficients to the corresponding terms in Equation 5.7.

The ideality factors for the LSBH and the HSBH extracted for the device represented in Fig 5.6 are 1.38 and 1.36, which are very close to each other. The barrier height of the HVLR region is 1.30 eV, which is higher than that of the LSBH region, 0.7 eV. The results from the forward I-V measurements on the Group B devices are tabulated and discussed in section 5.4.2. The value of ε extracted was in the range of 1e-9 to 1e-5,

which shows that size of the LSBH area ranges from 0.02–2 μm. Several research groups have reported such 'Two Schottky Barrier' behavior of SiC Schottky diodes. The maximum value of ε measured in this study compares well with values they have reported. Various phenomena like epitaxial growth pits, crystallographic defects, dopant clustering and contamination, have been considered as possible sources for such inhomogeneities in the barrier heights of SiC Schottky diodes [36, 47].

5.1.5 Reverse Characteristics

The reverse I-V characteristics of all diodes were measured by sweeping the voltage from 0 to 10 volts. In Fig 5.7, we show the reverse I-V characteristics of 13 devices. Eight diodes in this set exhibited Group A behavior and their characteristics are plotted using solid lines. The remaining five devices which exhibited Group B behavior have been plotted using dotted lines. In this graph, 2 diodes have higher reverse leakage current densities than the rest, and both of these devices belong to Group B. The J-V curves of the remaining diodes are all tightly distributed and appear as a solid line along the x-axis.

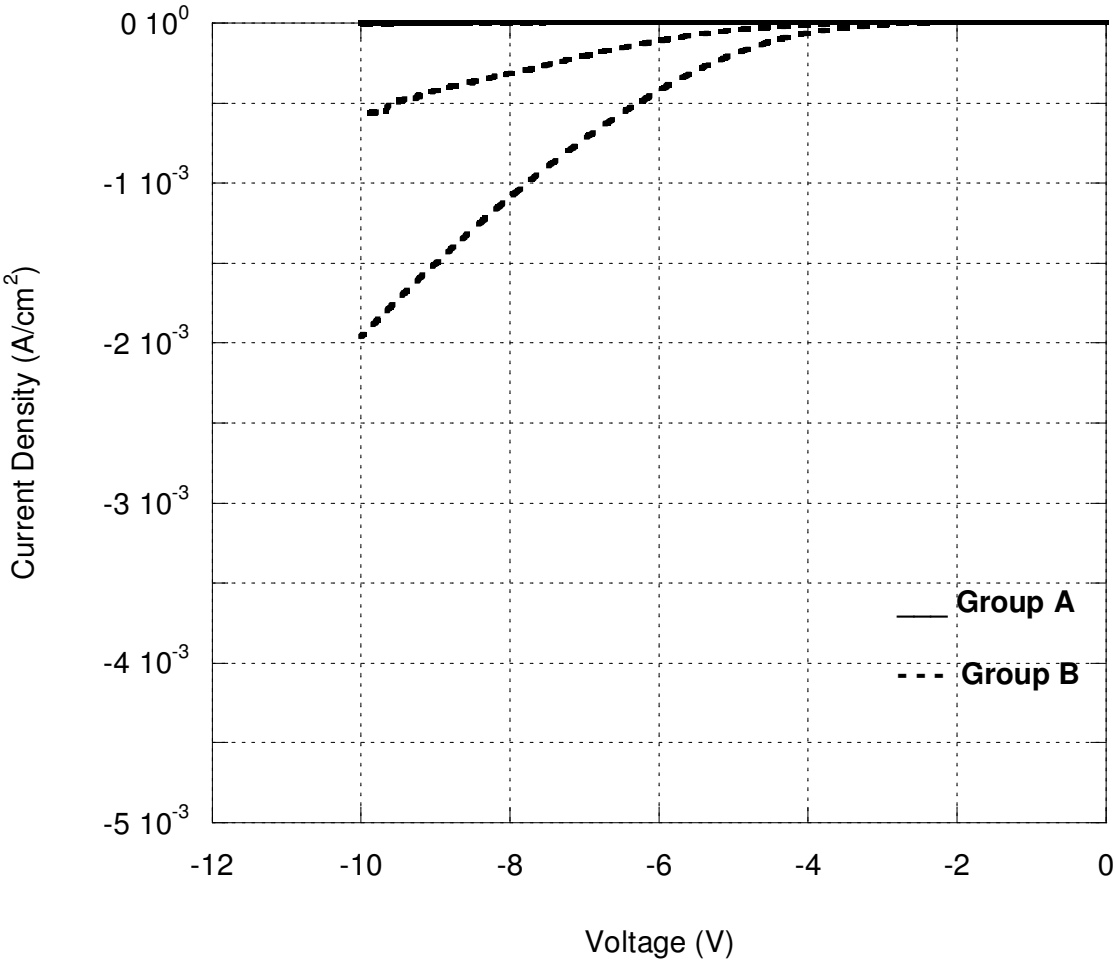


Fig 5.7 Reverse I-V Characteristics : Group A and Group B.

In Fig 5.8, we present the same set of reverse characteristics at a higher resolution to distinguish the individual curves for the devices with very low reverse current densities. The reverse characteristics of six diodes appear in this figure as a solid line along the x-axis. It can be noticed that 9 diodes, two of which belonged to Group B, had reverse current densities in the sub $\mu A/cm^2$ range even at a reverse bias of 10V. Thus not all Group B devices were inferior to the Group A devices in terms of reverse blocking

characteristics. Since the regions with a lower barrier could result in an excess leakage current under reverse bias, one would expect the diodes which belonged to Group B to exhibit poor blocking behavior, but this is not necessarily the case. These areas with lower barrier height can be shielded under reverse bias by the space charge region of the surrounding high barrier regions, provided they are small enough (i.e. they have a diameter less than the depth of the space charge region) [37] . The depletion width at a reverse bias of 10 V, calculated using equation 3.14, is about 5 μm. The value of ε extracted for the Group B devices was in the range of 0.02–2 μm, which is smaller than the depletion width, and the space charge region probably shielded some of the LSBH areas.

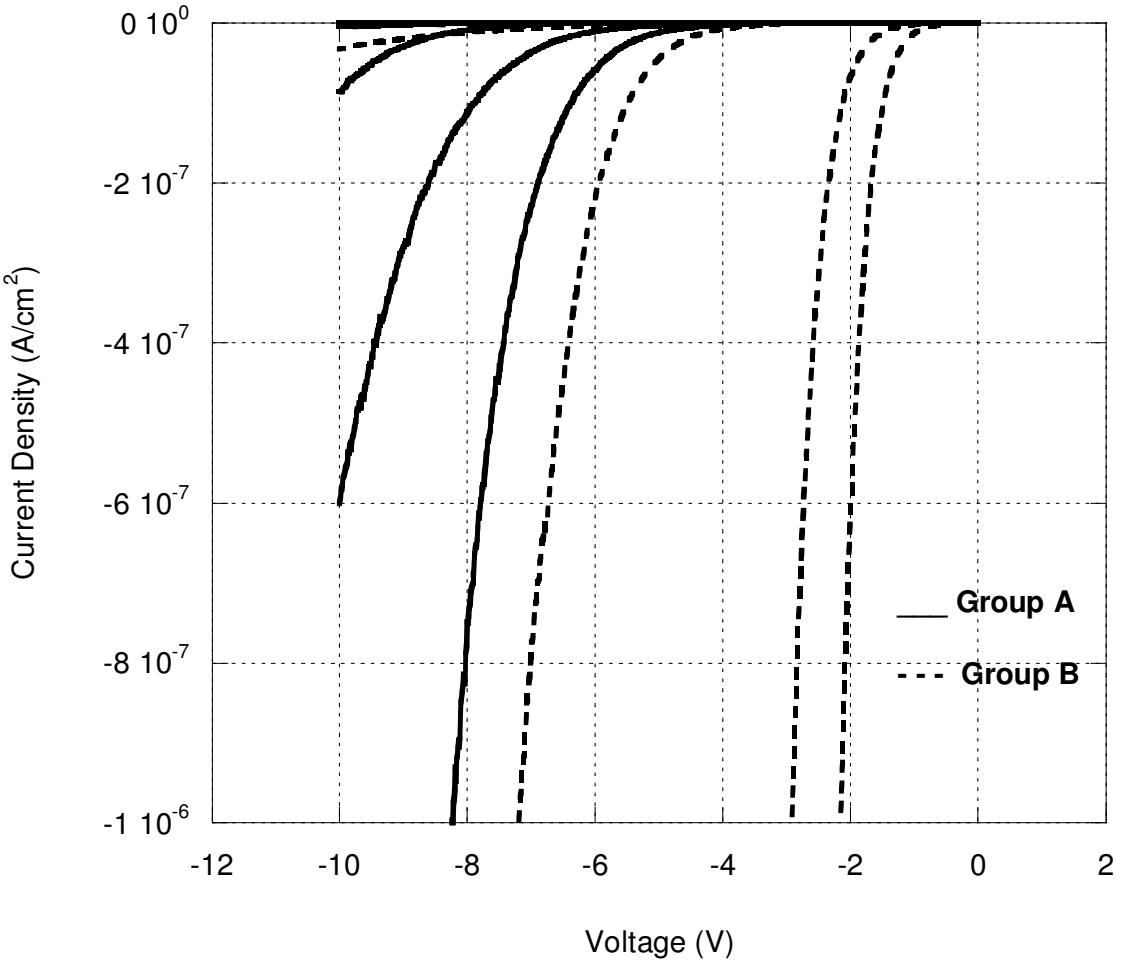


Fig 5.8 Reverse I-V Characteristics (high resolution)

The reverse voltage was swept up to 100V on some of the diodes which had good reverse blocking characteristics at -10V. The results from one of these measurements is presented in Fig 5.9. These high-voltage reverse measurements were repeatable indicating that the devices did not break down even at 100 V. Even at a reverse bias of 100 V, the current density for the example in Fig 5.9 is only in the range of about tens of $\mu A/cm^2$. These results indicate that the diodes exhibited good rectifying behavior.

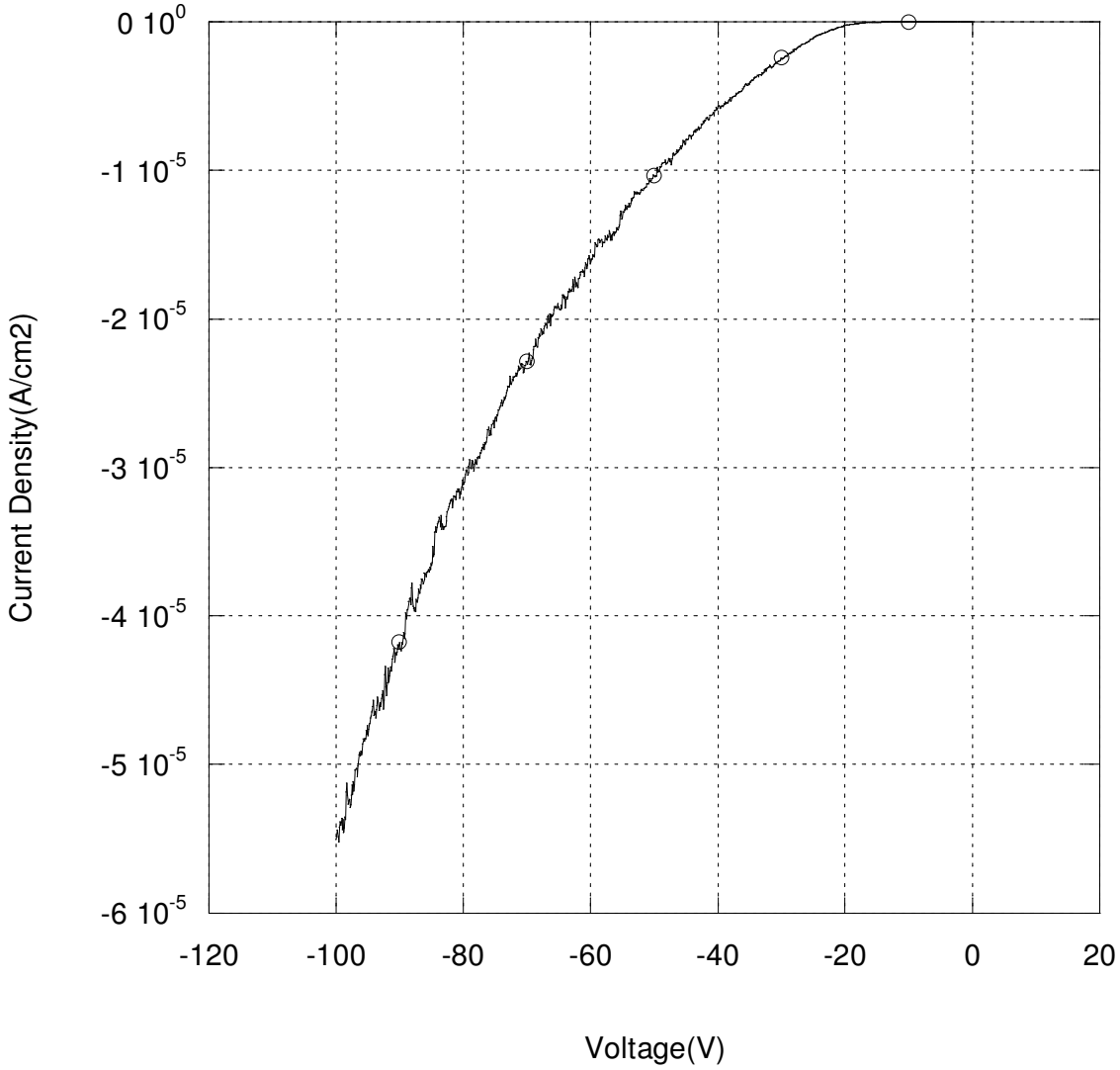


Fig 5.9 High Voltage Reverse J-V Characteristics.

To summarize the results from the I-V measurements, we have plotted the magnitude of the current density of one of the Group A devices from Sample III, against the applied voltage, in Fig 5.10. The results from both forward (0-10 V) and reverse (0-100 V) sweeps have been plotted together in this graph.

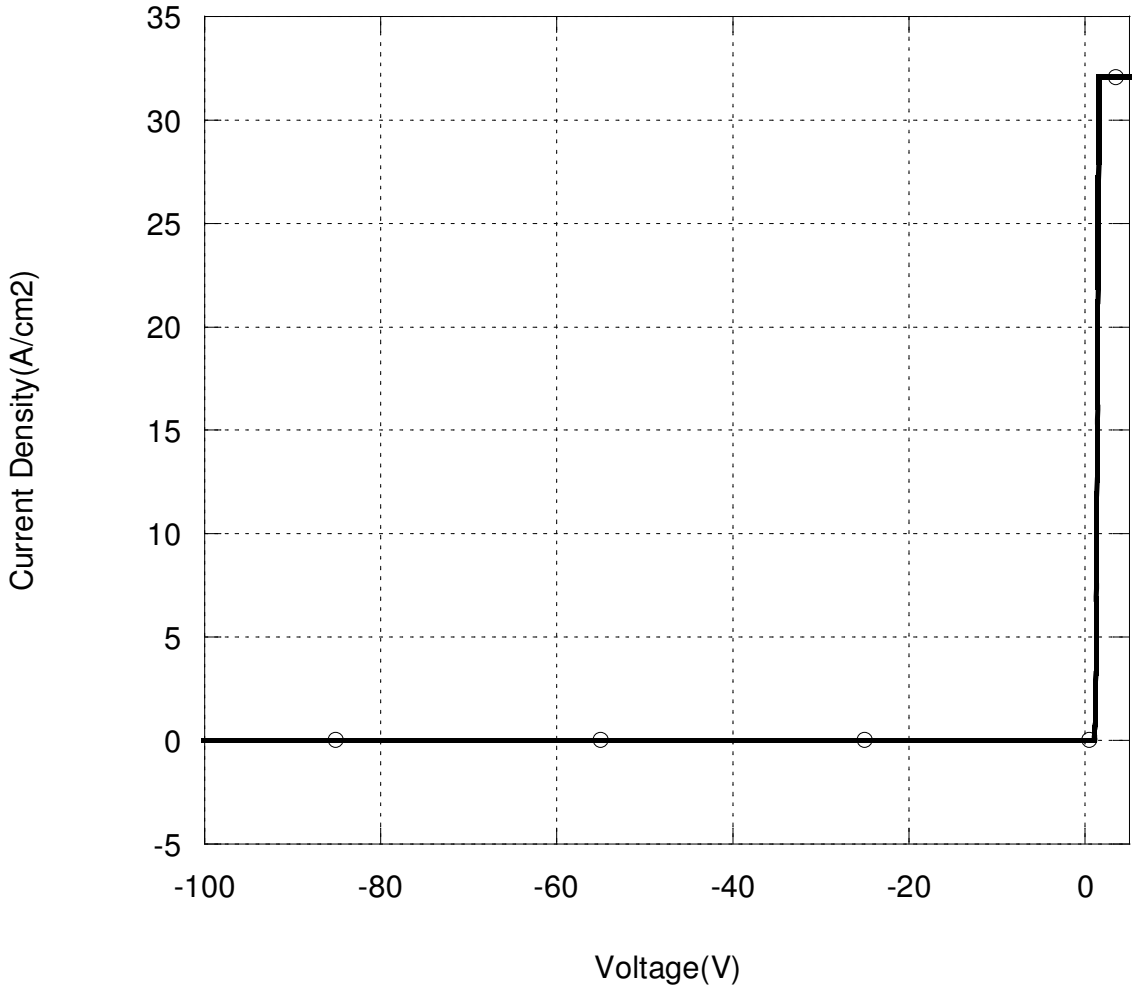


Fig 5.10 Forward and Reverse I-V characteristics.

It can be observed that the diode turns on sharply for forward biases and exhibits very low leakage current under reverse biases, similar to the I-V characteristics of an ideal diode illustrated in Fig 4.2.

5.2. C-V Characteristics

5.2.1 C-V Measurements

High Frequency (1MHz) C-V measurements were performed on the devices using a DLTS [Deep Level Transient Spectroscopy] system manufactured by Sula Technologies, Inc. The reverse bias on the devices was swept from 0-6 V. The C-V characteristics of 15 diodes, representing the total of 42 diodes from the samples which received a second surface clean, are presented in Fig 5.11. Four of the fifteen diodes belong to Group B and the rest belong to Group A. Group A characteristics are shown with solid lines and Group B with dotted lines. The C-V characteristics of Group A and Group B were not significantly different and have been presented together. The curves are tightly packed, which shows that the process was more controlled when these samples were fabricated.

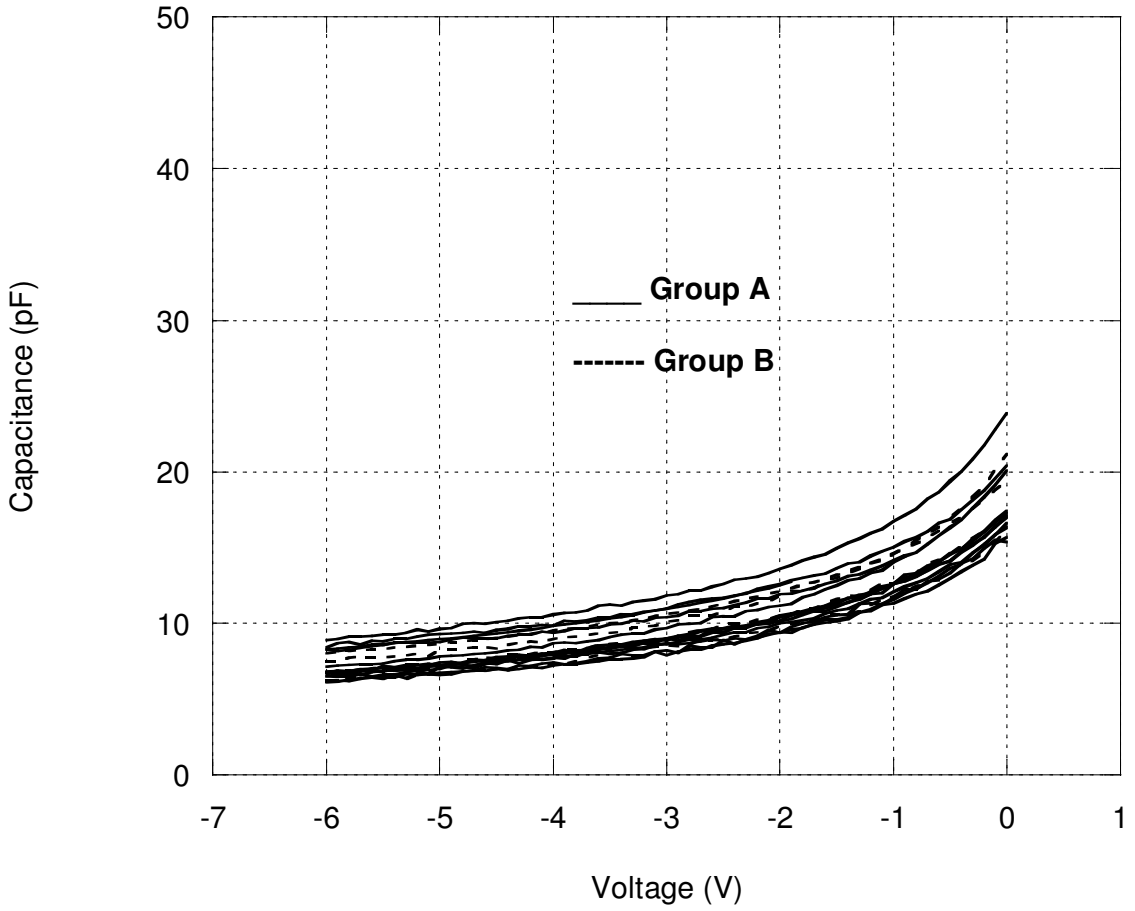


Fig 5.11 C-V Characteristics: Group A and B

5.2.2 Extraction of parameters from C-V Characteristics

A typical $1/C^2$ versus V characteristic of these Schottky diodes is shown in Fig 5.12. The junction capacitance of the diode can be written as [29],

$$\left(\frac{1}{C'}\right)^2 = \frac{2(V_{bi} + V_R)}{q\varepsilon_s N_d} \qquad \text{-- (5.9)}$$

where C' is the junction capacitance per unit area, V_{bi} is the built-in voltage, V_R is magnitude of the reverse voltage, ε_s is the dielectric constant of the semiconductor, and N_d is the donor dopant concentration. According to this equation, C-V measurements plotted as $1/C^2$ versus V_R should yield a straight line with a slope of $\frac{2}{q\varepsilon_s N_d}$ and a y-intercept of $\frac{2Vbi}{q\varepsilon_s N_d}$. The doping concentration was verified using the slope and the built in potential was extracted from the intercept of the $1/C^2$ vs. V characteristic. Using the values obtained for N_d and V_{bi}, the barrier height can be calculated from equations 3.16 and 3.17.

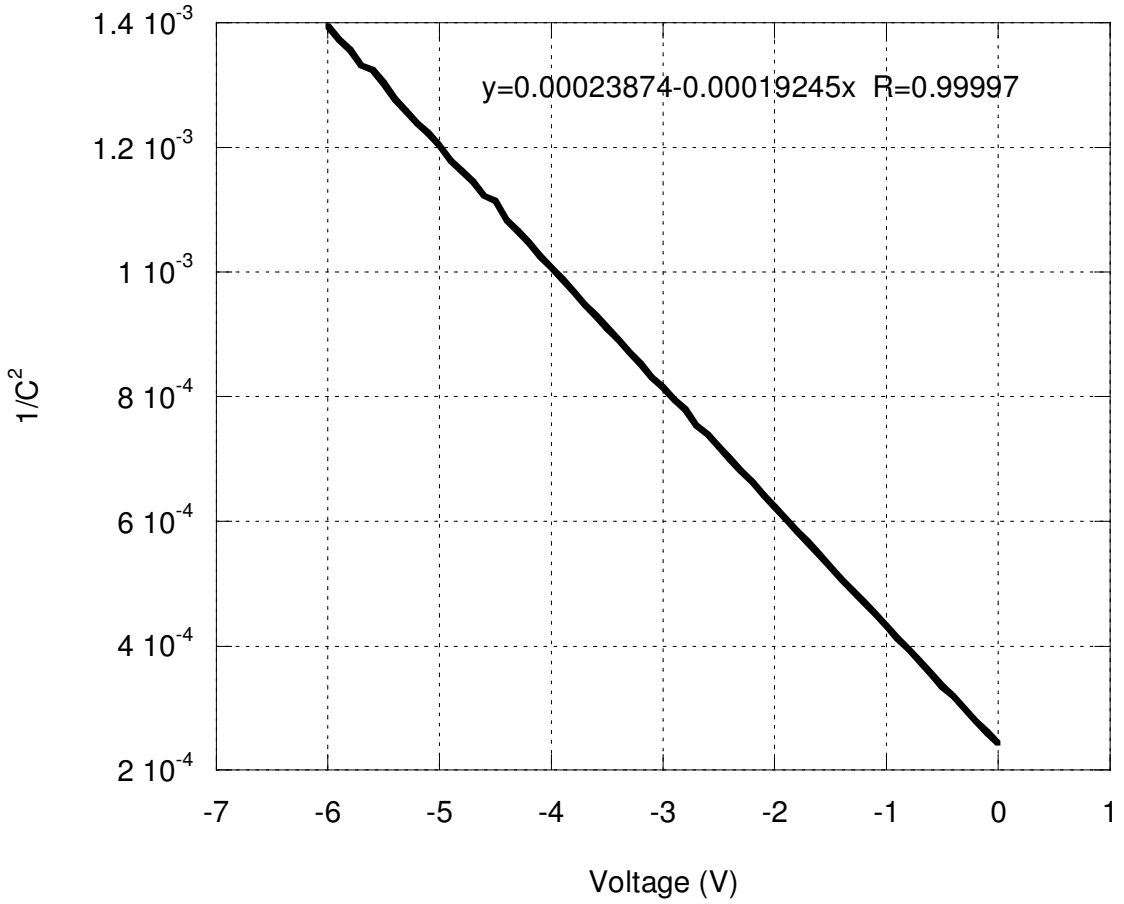


Fig 5.12 $1/C^2$ vs. V Characteristic for a device with the best linear fit.

The correlation coefficients for the best fit lines for the diodes from samples which received a second surface clean were in the range of 0.997-0.999, which shows that $1/C^2$ vs. V characteristics were almost perfectly linear. For the diode whose characteristic is presented in Fig 5.12, the linear-fit to $1/C^2$ vs. V appears on the top right as an expression for y in terms of x. The values for N_d, V_{bi} and ϕ_B extracted for this device are 7.57 x 10^{14} cm^{-2}, 1.24 V and 1.49 eV respectively. The results obtained from the CV measurements are also tabulated in Tables 5.1 and 5.3. On average the Schottky barrier

heights obtained from the $1/C^2$ vs. V characteristics are slightly higher than those obtained from the I-V characteristics. The higher barrier height obtained from C-V is attributed to the presence of a thin oxide layer at the interface. The oxide layer in series with the depletion capacitance would decrease the total capacitance, thus giving a higher built in voltage, and thereby resulting in a higher value of extracted barrier height [35].

5.3 Comparison with Schottky Mott limit

The Schottky Mott limit gives the barrier height for a Schottky diode under ideal conditions, assuming the absence of a significant density of interface states. The barrier height given by Schottky Mott limit is [27]:

$$q\phi_B = q\Phi_M - q\chi\,, \qquad \text{-- (5.10)}$$

where Φ_M is the metal work function, and $q\chi$ is the electron affinity of the semiconductor. Using a value of 4.7eV for the work function of Copper [27] and a value of 3.6eV for the electron affinity of 4H-SiC [46] in Equation 5.10, the Schottky Mott limit for the barrier height of Cu/4H SiC Schottky contacts is 1.1 eV. From Table 5.2 we can see that the average barrier height for the three samples extracted using the IV characteristics ranged from 1.32-1.43eV. These values are close to the calculated Schottky Mott limit of 1.1eV considering the fact these diodes were not fabricated under ideal conditions. This gives us a good comparison between the values that were obtained and the ideal value for the barrier height.

5.4 Results and Discussion

5.4.1 Group A Summary

The barrier height, ideality factor and the reverse saturation current density extracted from the I-V measurements on Group A devices from Samples III, IV and V are shown in Table 5.1. The barrier height and the doping concentration extracted from the C-V measurements on these devices are also presented in Table 5.1. The total results are summarized in Table 5.2. Several immediate observations can be made from tables 5.1 and 5.2. First, within each sample of devices, there is very little variation in the measured barrier heights and ideality factors, as seen from the I-V measurements section of table 5.2. This indicates the uniformity of the devices undergoing the same process sequence. The barrier height varies only by a few tenths of an eV. The difference between the maximum and minimum ideality factors in sample III is 0.44, while on samples IV and V, it is only 0.15 and 0.2, respectively. The reason for the higher spread of the ideality factor for Sample III can be attributed to the fact that it was the first one to be fabricated with a second surface clean before the technique was perfected. Even though the variation in the ideality factors is relatively high on Sample III, the standard deviation for the ideality factor between the devices for this sample is only 0.14. The barrier height measurements are accurate to the nearest 0.1 eV, while the ideality factors are accurate to within 0.1.

The average ideality factors are 1.26, 1.25 and 1.24 for samples III, IV and V, respectively. The maximum difference between the averages is 0.02 which shows that the process was very well controlled across samples. Also, the ideality factors are close to

unity, indicating that they perform almost like ideal Schottky diodes. The average barrier heights are also similar, with a maximum difference between the samples of 0.08eV. In section 5.3, we calculated the theoretical barrier height for an ideal Schottky contact as 1.1eV, based on the Schottky-Mott limit. The average values of the barrier heights for the three samples are 1.37, 1.29 and 1.35 from I-V measurements, and 1.40, 1.36 and 1.36 from C-V measurements. These measured values are close to the theoretical values, considering that these diodes were not fabricated under the most ideal conditions. Also, the average barrier heights extracted from the C-V measurements are only slightly higher than the values obtained from I-V measurements. As already discussed in section 5.2.2, the barrier heights are often overestimated from C-V measurements if there is a thin oxide layer at the Cu/4H-SiC interface. From Table 5.1, it can be seen that the measured doping concentration varies from 3.53×10^{14} cm^{-3} to 7.65×10^{15} cm^{-3}, which is close to the manufacturer's specification for the epilayer doping, 5×10^{15} cm^{-3}.

Table 5.1 Detailed tabulation of results for Group A

	I-V measurement results			**C-V measurement results**		
	n	ϕ_b (eV)	J_s (A/cm^2)	V_{bi}	ϕ_b	N_d (cm^{-3})
Sample III						
1	1.16	1.42	2.15e-17	0.80	1.06	5.12e14
2	1.24	1.36	2.45e-16	1.03	1.29	8.2e14
3	1.26	1.36	1.99e-16	1.20	1.46	7.28e14
4	1.16	1.43	1.02e-17	1.32	1.52	6.85e15
5	1.29	1.35	2.71e-16	1.26	1.46	7.34 e15
6	1.18	1.42	1.92e-17	1.26	1.46	7.16 e15
7	1.18	1.42	2.27e-17	1.26	1.46	7.65 e15
8	1.60	1.19	1.29e-13	1.26	1.46	7.59 e15
9	1.24	1.42	1.79e-16	1.26	1.46	7.59 e15
Sample IV						
1	1.34	1.25	1.324e-13	1.20	1.47	4.00e14
2	1.22	1.32	8.330e-15	1.19	1.45	6.79e14
3	1.20	1.34	4.790e-15	1.19	1.45	6.79e14
4	1.22	1.32	1.019e-14	0.95	1.23	3.66e14
5	1.22	1.31	1.430e-14	1.34	1.59	7.70e14
6	1.19	1.32	1.000e-14	1.13	1.40	4.32e14
7	1.29	1.27	5.922e-14	1.02	1.29	4.01e14
8	1.34	1.24	2.070e-13	1.15	1.42	4.36e14
9	1.23	1.30	1.850e-14	1.24	1.49	7.57e14
10	1.33	1.24	2.190e-13	1.10	1.16	3.77e14
11	1.25	1.28	3.970e-14	0.85	1.12	4.36e14
12	1.22	1.30	5.000e-14	0.97	1.25	3.53e14
Sample V						
1	1.14	1.40	3.410-17	1.2	1.47	4.00e14
2	1.40	1.27	3.360e-16	1.23	1.5	4.92e14
3	1.17	1.37	1.198e-16	1.11	1.38	4.42e14
4	1.33	1.25	3.160e-14	1.06	1.33	4.70e14
5	1.14	1.40	3.977e-17	1.04	1.31	4.47e14
6	1.312	1.28	3.390e-15	1.05	1.32	4.40e14
7	1.18	1.43	1.200e-16	1.08	1.35	4.66e14
8	1.18	1.37	1.350e-16	1.05	1.32	4.32e14
9	1.2	1.36	2.010e-16	1.04	1.31	4.68e14
10	1.19	1.35	2.380e-16	1.06	1.33	4.69e14
11	1.34	1.34	5.009e-16	1.06	1.37	4.45e14

Table 5.2 Summary of results from Table 5.1

	Number of Group A diodes	***Average***	***Max***	***Min***	***Std Dev***
Results from I-V measurements					
Ideality factor					
Sample III	9	1.26	1.6	1.16	0.14
Sample IV	12	1.25	1.34	1.19	0.06
Sample V	11	1.24	1.34	1.14	0.09
Barrier Height		*(eV)*	*(eV)*	*(eV)*	*(eV)*
Sample III	9	1.37	1.43	1.19	0.08
Sample IV	12	1.29	1.32	1.24	0.03
Sample V	11	1.35	1.43	1.14	0.06
Results from C-V measurements					
Barrier Height		*(eV)*	*(eV)*	*(eV)*	*(eV)*
Sample III	9	1.40	1.52	1.06	0.14
Sample IV	12	1.36	1.59	1.12	0.15
Sample V	11	1.36	1.50	1.31	0.06

5.4.2 Group B Summary

The results from the I-V and C-V measurements on the Group B devices from the samples III, IV and V are presented in Table 5.3, and the averages in Table 5.4. It can be observed from Table 5.3 that the ideality factors are similar between the LSBH and HSBH regions for all devices. As expected, the barrier heights extracted for the LSBH regions are much less than that of the HSBH regions. There is very little variation of

ideality factors within each sample, with the maximum being 0.2 for Sample V. The maximum variation of barrier heights for the HSBH regions within each sample is 0.21 eV. The HSBH barrier heights measured from the C-V data are on average higher than those obtained from I-V measurements, as expected and discussed earlier. Also, from Table 5.4, it can be seen that the average ideality factors and barrier heights did not vary significantly across the samples. The HSBH parameters compare well with those of the Group A diodes, which indicates that ignoring the inhomogeneities, the Group B devices behave like Group A devices from the same sample. From Table 5.3, it can be seen that the measured doping concentration varies from 3.86×10^{14} cm^{-3} to 8.33×10^{15} cm^{-3}, which is close to the manufacturer's specification for the epilayer doping, 5×10^{15} cm^{-3}.

Table 5.3 Detailed tabulation of results for Group B

	I-V measurement results			C-V measurement results		
		n	$\phi_b(eV)$	V_{bi}	ϕ_b (eV)	N_d (cm^{-3})
Sample III						
1	LSBH	1.38	0.84	0.83	1.09	5.62e14
	HSBH	1.30	1.35			
2	LSBH	1.23	0.5	1.21	1.47	6.83e14
	HSBH	1.25	1.25			
3	LSBH	1.18	0.82	1.32	1.52	8.33 e15
	HSBH	1.29	1.34			
4	LSBH	1.39	0.53	1.31	1.51	7.61 e15
	HSBH	1.33	1.36			
Sample IV						
1	LSBH	1.29	0.67	1.23	1.49	4.92e14
	HSBH	1.30	1.13			
2	LSBH	1.30	0.68	1.37	1.63	5.09e14
	HSBH	1.30	1.34			
Sample V						
1	LSBH	1.28	0.81	0.81	1.08	3.86e14
	HSBH	1.24	1.33			
2	LSBH	1.48	0.66	1.01	1.28	4.06e14
	HSBH	1.42	1.4			
3	LSBH	1.44	0.62	1.04	1.31	4.16e14
	HSBH	1.44	1.22			

Table 5.4 Averages of results from Table 5.3

		I-V Measurements		C-V Measurements		
		n	ϕ_b (eV)	V_{bi}	ϕ_b (eV)	Nd (cm-3)
Sample III	LSBH	1.29	0.67	1.167	1.39	6.23E+14
	HSBH	1.29	1.32			
Sample IV	LSBH	1.29	0.67	1.3	1.56	5.01E+14
	HSBH	1.30	1.23			
Sample V	LSBH	1.40	0.69	0.95	1.22	4.03E+14
	HSBH	1.33	1.36			

5.5 Conclusion

This work represents some of the first data published on Cu/4H-SiC devices. Based on the forward I-V characteristics, the diodes were classified into two categories, Group A and Group B, and studied individually. The Group A devices exhibited a single linear region in the forward semilog I-V characteristics for several orders of magnitude. These results could be modeled using the Richard-Dushman equation. The extracted ideality factors were close to unity and the barrier heights were close to the theoretical results obtained from the Schottky-Mott limit. Also, the spread of these values within and across the samples indicated that the process was uniform and well controlled. The Group B devices had two linear regions parallel to each other. This could be modeled as two Schottky diodes working in parallel, one with a lower barrier height and a much smaller area than the other. Such localized lowering of the barrier height exhibited by the Group B devices can be attributed to the inhomogeneities at the metal-semiconductor interface. With this model, the barrier heights and ideality factors were extracted separately for the two linear regions. The results confirmed well with our theory of the existence of regions with two barrier heights.

CHAPTER 6

COMPARISON OF DIFFERENT FABRICATION TECHNIQUES

Various types of fabrication techniques were experimented with to obtain the final samples. The main fabrication step which improved the I-V characteristics drastically was the addition of a second surface clean performed prior to depositing the Schottky contacts. Recall that the nickel contacts on the back side of the diode had to be annealed at 1000˚C temperature in order to make them low resistance ohmic contacts. The samples which were fabricated initially did not receive a front side surface clean after the nickel contacts were annealed. This second surface clean, which was performed on the later set of samples before the Schottky contacts were deposited, resulted in significantly improved I-V characteristics. The second surface clean was an elaborate procedure which involved protecting the ohmic contacts on the back of the sample while the front surface was cleaned, deposition of the Schottky contacts, coating the Schottky contacts while the protective layer on the ohmic contacts was etched off, and finally, removing the protective coating on the Schottky contacts without the affecting the ohmic contacts.

In this Chapter the I-V and C-V characteristics, and the extracted electrical parameters of samples with and without second surface clean are compared. The physical characterization of these samples using XPS (X-ray Photoelectron Spectroscopy) is also discussed. The presence of an oxide layer at the Cu/4H-SiC interface is established from the results of these electrical and physical characterizations.

6.1 Effect of Second Surface Clean on I-V Characteristics

The importance of a second surface clean was established while experimenting with the samples. Samples I and II did not receive a surface clean after annealing the ohmic contacts, resulting in contacts with poor forward I-V characteristics. The electrical characteristics of diodes from Samples III, IV and V which had a second surface clean were discussed in detail in the previous Chapter, and referred to as Group A and Group B. In this Chapter the samples which did not receive a second surface clean are referred to as Batch I and the ones which received a second clean as Batch II. In Fig 6.1, the semilog I-V characteristics of diodes from Batch I, represented by solid lines, are compared with a typical Group A diode from Batch II, represented by the dotted line. Several immediate observations can be made from Fig 6.1. In the forward bias range of 0.8–1.2 V, in which the Batch II device clearly follows thermionic emission, the current densities through the devices without the second surface clean are several orders of magnitude lower. The slope of the characteristics is also noticeably smaller for the Batch I devices than for the Batch II device. The I-V characteristics start rolling off at lower currents for Batch I devices than for the Batch II device, indicating that Batch I had a higher series resistance. All of these observations point to the poor Cu/4H-SiC interface quality of the Batch I devices. The added resistance due to the presence of an oxide layer at this interface could explain the apparent high ideality factors of the Batch I devices [35].

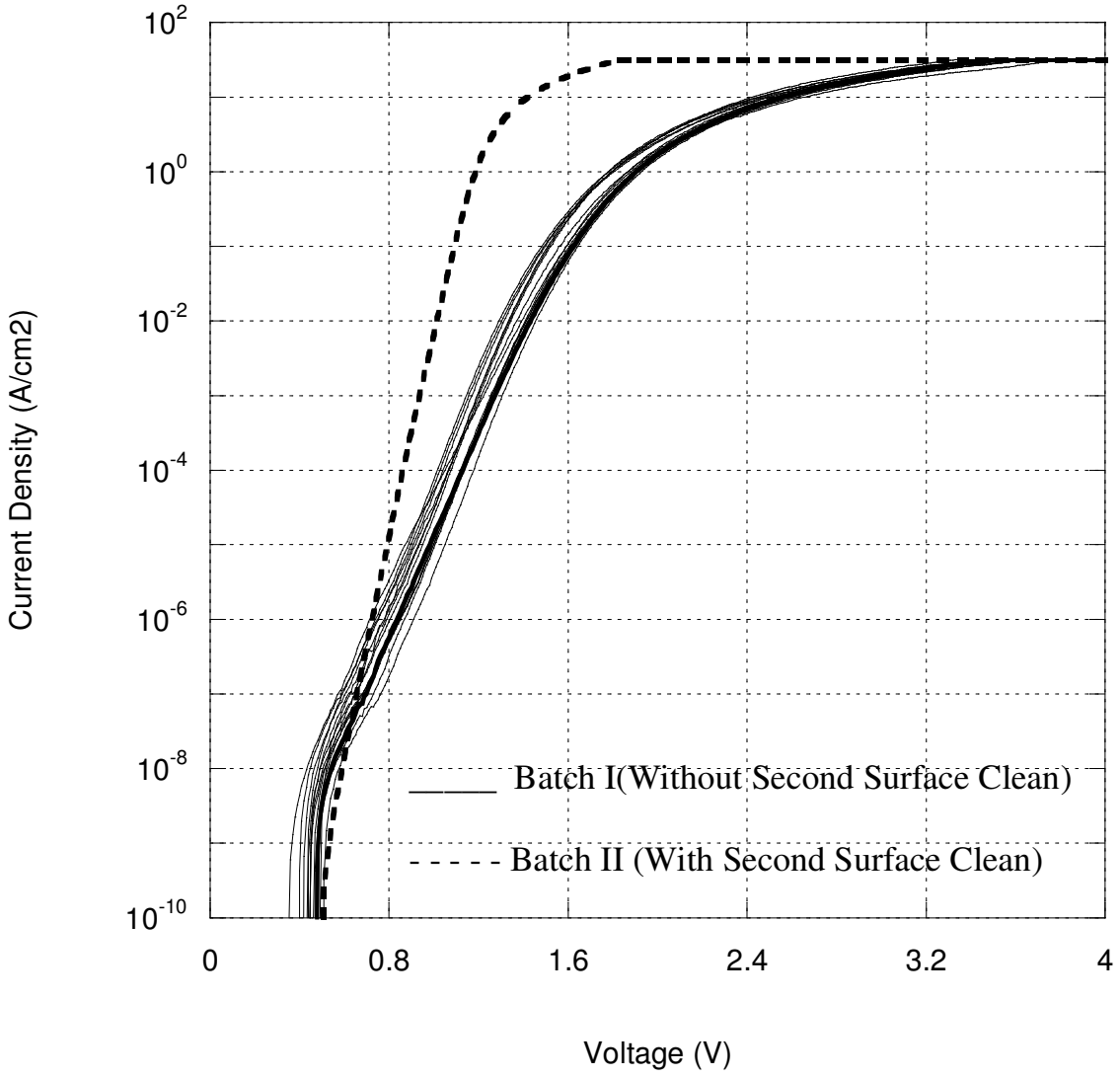


Fig 6.1 Effect of second surface clean on Forward I-V characteristics

In Fig 6.2, the linear regions of the semilog I-V characteristics of two diodes, one from the Sample which received a second surface clean and one which did not, have been presented. They were modeled using the Richard-Dushman equation, as described in section 5.1.3. The extracted barrier heights and the ideality factors for these two devices are also presented in Fig 6.2. It can be observed that the ideality factor is much closer to

unity for the diode which received a second surface clean. The barrier height for Batch I diodes are lower that the barrier height for Batch II diodes. The extracted parameters have been tabulated (Table 6.1) and discussed in section 6.3.

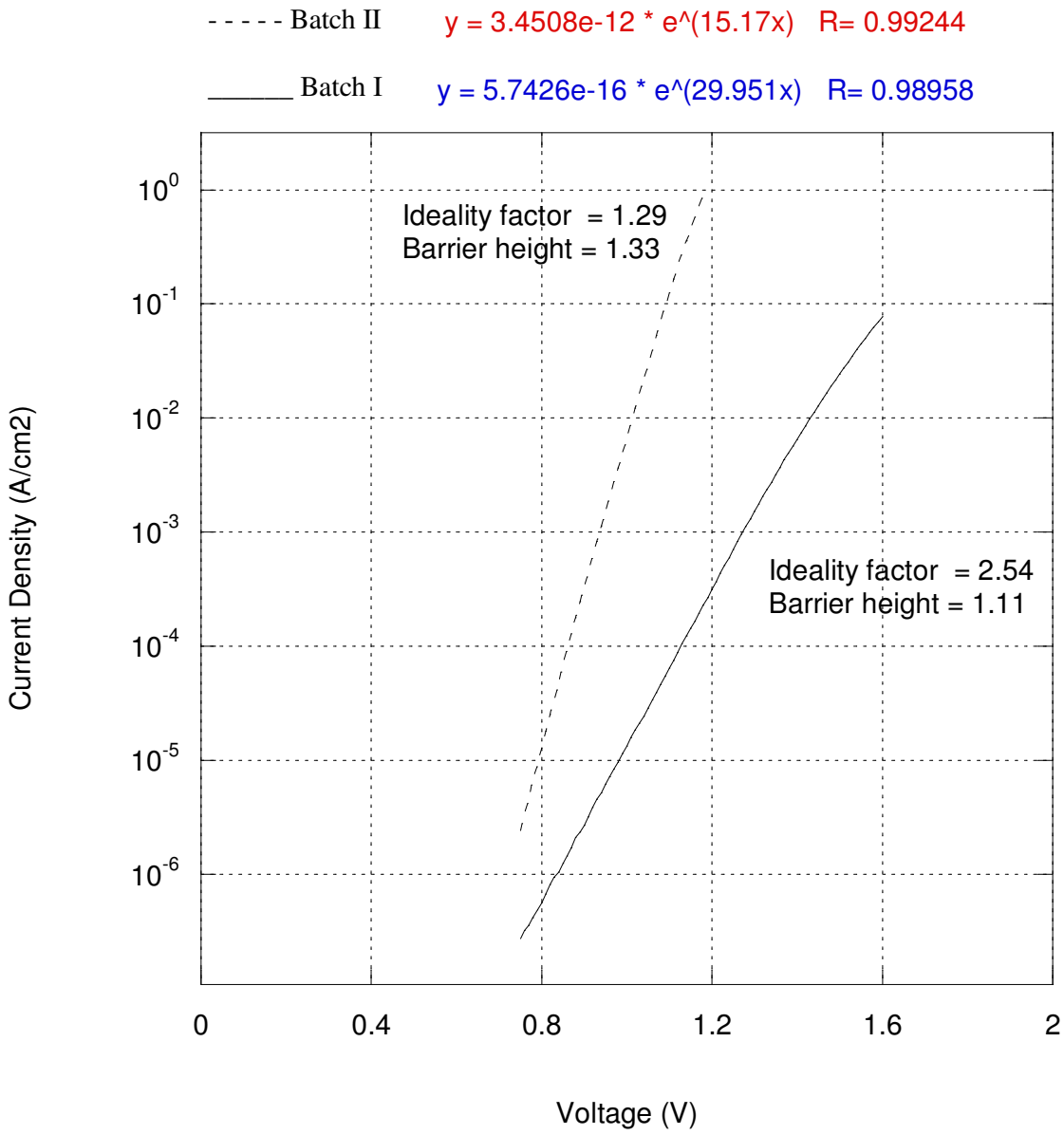


Fig 6.2 Extraction of Ideality Factor and Barrier Height for Batch I & II

The portion of the linear I-V characteristics where the series resistance dominates is presented in Fig 6.3 for the two devices discussed above. The inverse of the slope of a linear fit gives the series resistance per unit area, R_s/A. The series resistance, R_s, extracted for the Batch I device is more than double the R_s extracted for Batch II device, which can again be explained by the presence of an oxide layer at the Schottky contact interface.

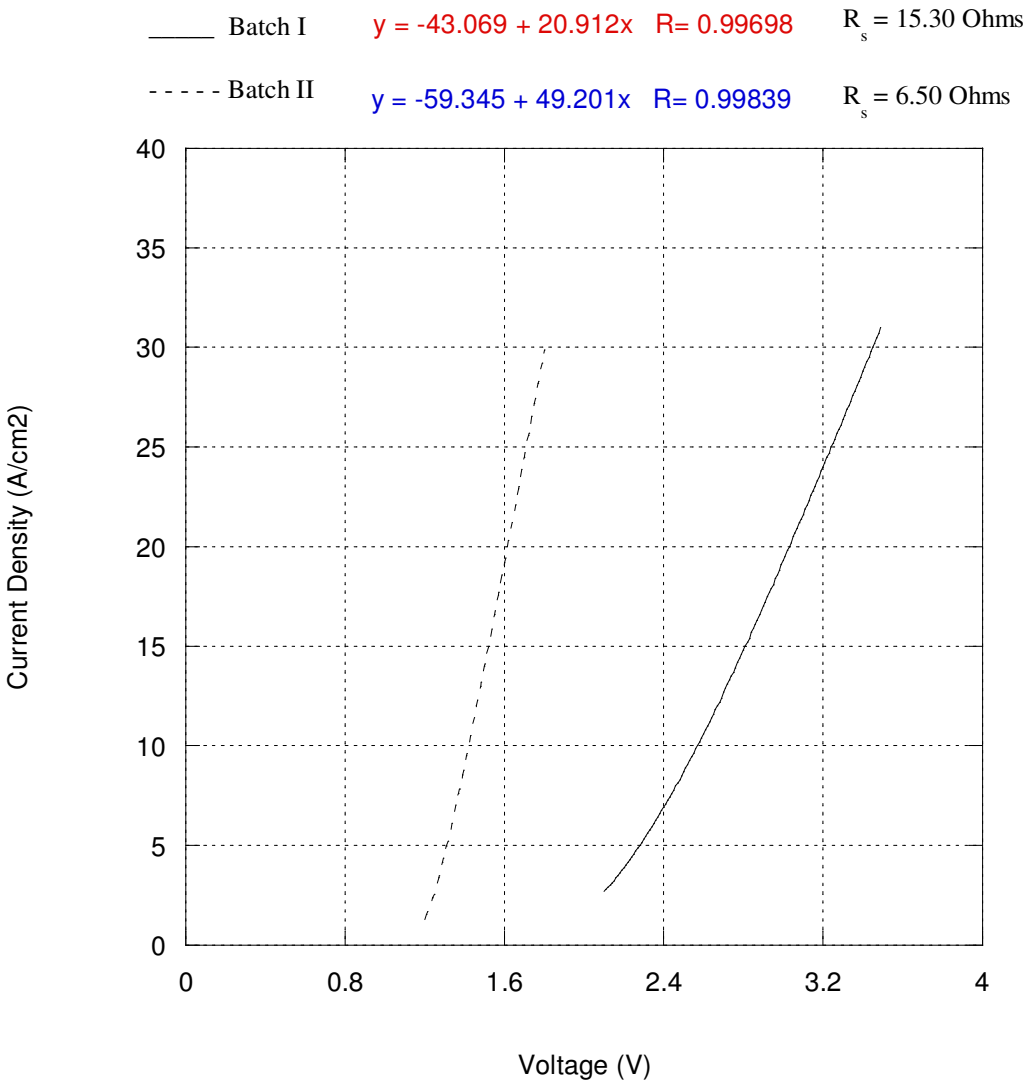


Fig 6.3 Extraction of Series Resistance for Batch I & II

6.2 Effect of second surface clean on C-V Characteristics

In Fig 6.4, we compare the C-V curves of the Batch I devices and one typical Batch II device. The capacitance of the Batch I diodes was almost 3 to 5 times lager than that of the Batch II diode. From the comparison of the results from the I-V measurements on the Batch I and Batch II devices in the previous section, it was suspected that there was an oxide layer at the interface of the Batch I devices. If the capacitance of this interfacial oxide layer acts in series with the depletion capacitance, we would expect the total measured capacitance to be smaller for the Batch I devices than for the Batch II devices. However, the difference in the measured capacitance between the two batches is in the opposite direction. This can be explained if the interfacial oxide actually screens the depletion region in the SiC from the field. This would reduce the depletion width and ultimately increase the measured capacitance, as the depletion capacitance is inversely proportional to the depletion width [35].

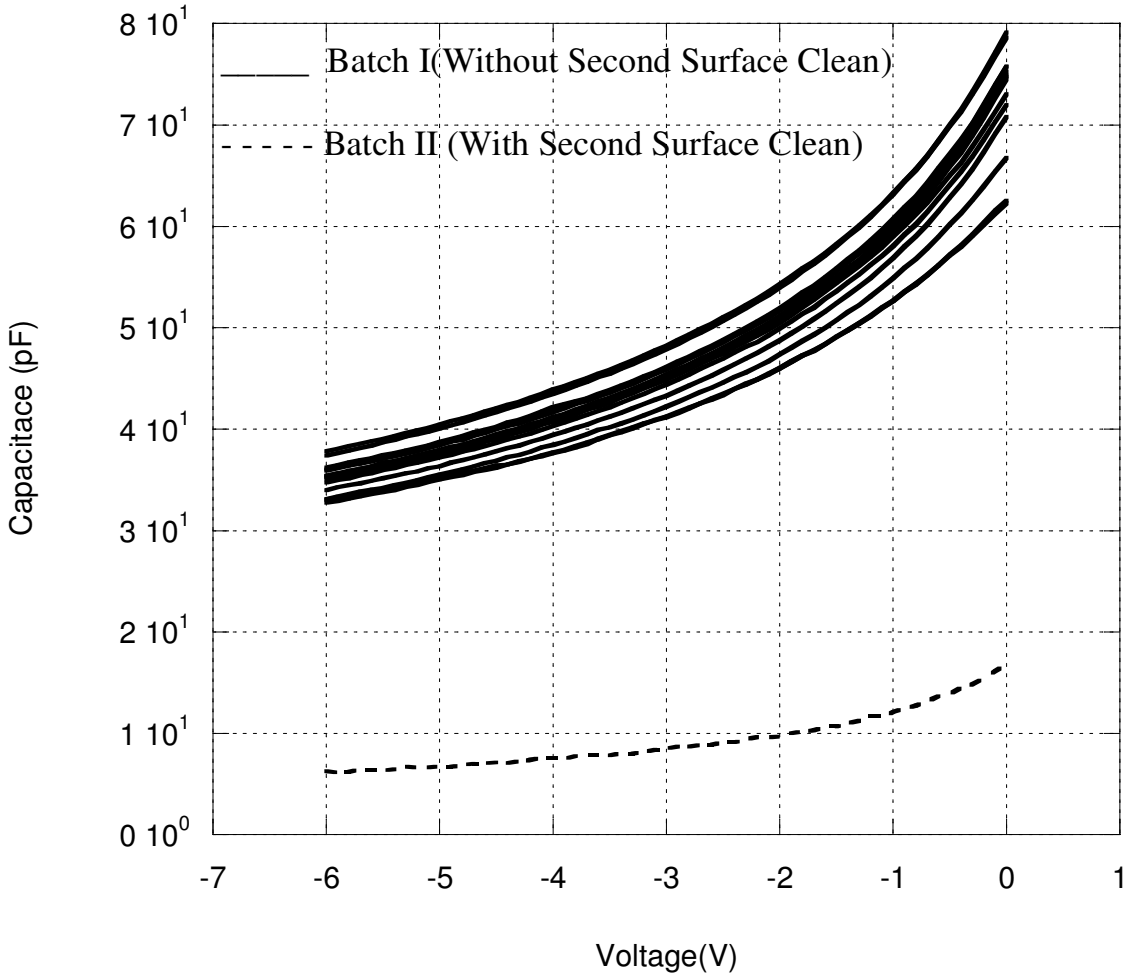


Fig 6.4 Effect of Second Surface Clean on C-V Characteristics

In Fig 6.5, the $1/C^2$ vs. V plots of typical Batch I and Batch II devices are presented. The barrier heights for these two devices, extracted using the procedure described in section 5.2.2, are also presented in Fig 6.5. The x-intercept for the Batch I device is greater than that for the Batch II device, which translates into a higher extracted barrier height. It can be observed that the barrier height for Batch I estimated from the C-V data is 2.46 eV, whereas the barrier height determined from the I-V measurements is

1.11 eV. This higher barrier height extracted from C-V measurements is also evidence of a thicker oxide layer on the Batch I devices.

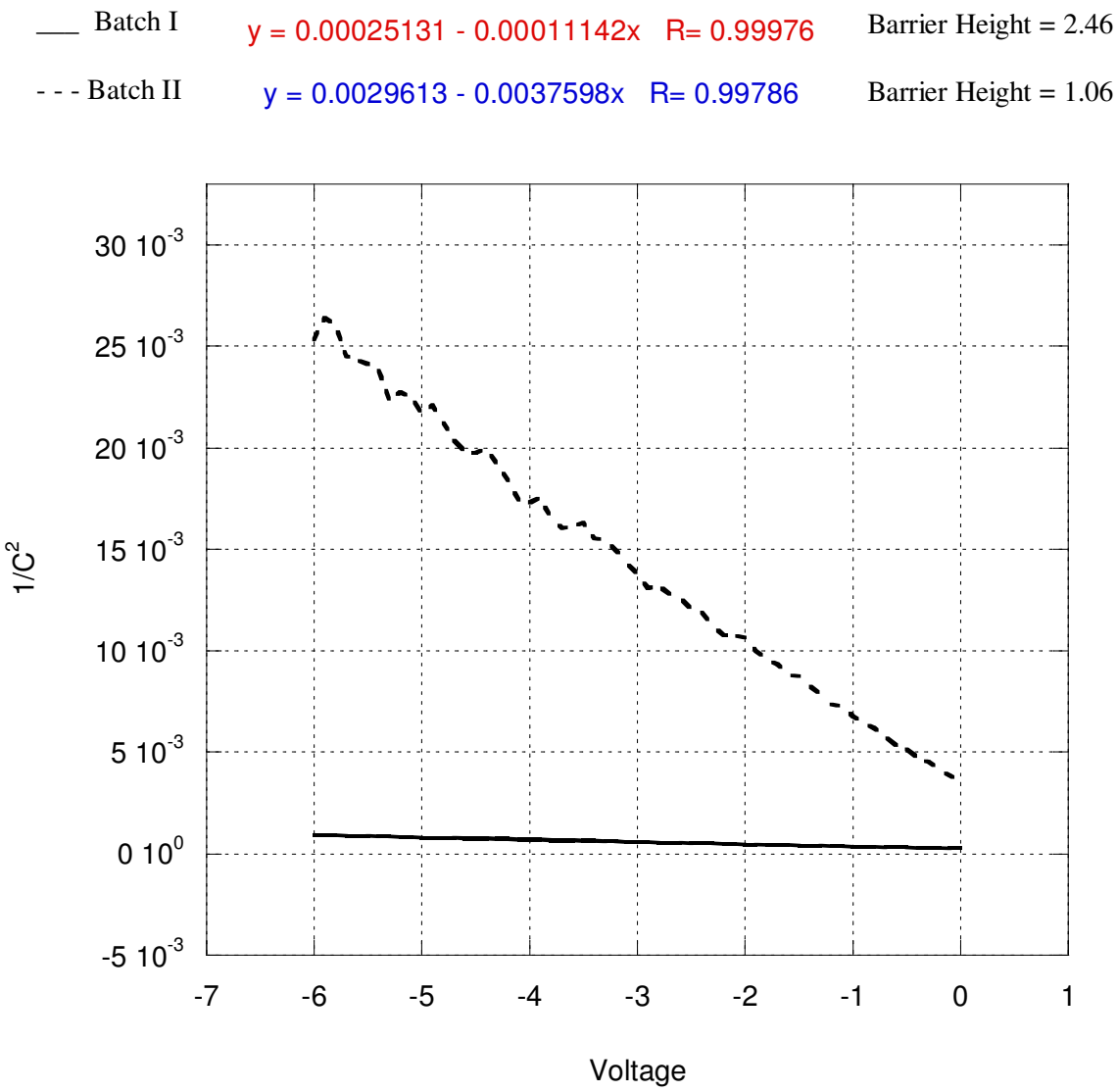


Fig 6.5 Barrier Height from $1/C^2$ vs. V for Batch I and Batch II

6.3 Tabulation of Results and discussion

Table 6.1 lists the detailed extracted values of ideality factor, Schottky barrier height and doping concentration obtained using the I-V and C-V curves. The average values for the extracted parameters are listed in table 6.2 for Batch I diodes and the Batch II diodes, which exhibited Group A behavior. The average ideality factor for Batch I diodes is 2.35 and for Batch II diodes is 1.24, indicating the drastic improvement in the performance due to the second surface clean. The Batch I diodes have a slightly lower barrier height from I-V measurements of 1.18eV compared to the average of 1.33eV for Batch II. The barrier height extracted from the C-V measurements for Batch I had an average of 2.02 which was much higher than that for Batch II. This is as expected since barrier heights tend to be overestimated from C-V measurements in the presence of an interfacial oxide layer.

Table 6.1 Results for samples without a second surface clean

	I-V measurement results		C-V measurement results		
	n	ϕ_b (eV)	V_{bi} (eV)	ϕ_b (eV)	N_d (cm^{-3})
1	2.26	1.22	2.28	2.46	1.31e16
2	2.54	1.11	1.81	1.99	1.32e16
3	2.35	1.17	1.81	1.99	1.63e16
4	2.78	1.10	2.20	2.34	1.29e16
5	2.36	1.20	1.80	1.98	1.38e16
6	2.26	1.24	1.73	1.91	1.58e16
7	2.28	1.18	1.79	1.97	1.49e16
8	2.31	1.21	1.82	2.00	1.42e16
9	2.45	1.18	1.78	1.96	1.47e16
10	2.28	1.17	1.76	1.94	1.42e16
11	2.26	1.18	1.92	2.1	1.28e16
12	2.23	1.20	1.72	1.90	1.41e16
13	2.31	1.20	1.74	1.92	1.45e16
14	2.31	1.16	1.69	1.87	1.38e16

Table 6.2 Average Extracted Parameters for Batch I & II

	I-V measurement results		C-V measurement results	
	n	ϕ_b (eV)	V_{bi} (eV)	ϕ_b (eV)
Batch I	2.35	1.18	1.85	2.02
Batch II -Group A	1.24	1.33	1.12	1.37

6.4 X-ray Photoelectron Spectroscopy Results

The presence of an oxide layer at the interface was verified using X-Ray photoelectron spectroscopy (XPS). In order to study the proportion of oxide present on the SiC surface with and without the second surface clean, two 6 mm x 6 mm die were processed identically as discussed in section 4.2, up to the step where the Ni contacts were annealed. After the Nickel contacts on both the samples were annealed

simultaneously, then, only one of the samples was treated with a second surface clean. XPS was done on both samples to determine the atomic concentrations of the elements at the surface (1-10 nm). The results from the XPS characterization are presented in Table 6.3. The results showed evidence of Silicon and Carbon and only traces of Oxygen on the surface of the sample which had a second surface clean. The sample which did not receive a second surface clean showed a considerable amount of oxygen on the surface, indicating the presence of oxides of silicon.

Table 6.2 XPS Results [Atomic Concentrations (%)]

	Sample with second surface clean	Sample without second surface clean
Carbon	49.66	0
Silicon	44.66	44.42
Oxygen	6.18	55.58

The sample which had a second surface clean showed Carbon and silicon in the ratio 1:1.1, with an atomic concentration of only 6.18 % of oxygen. This Si:C ratio is close to 1:1 and compares well with the empirical formula of SiC. The sample which did not have a second surface clean showed 0% of carbon and Silicon and oxygen in the ratio 1:1.25 , which indicates these samples had only oxides of silicon on the their surface. Thus, using both electrical and physical characterization we have strong evidence that the poor electrical characteristics of the diodes which did not have a second surface clean was due to the presence of an oxide layer at the Cu/SiC interface. This oxide layer may have been formed on the front surface during the annealing of the ohmic contacts at high temperatures.

6.5 Conclusion

In this Chapter we presented the characteristics of devices which did not have a second surface clean. The I-V and C-V characteristics along with the extracted ideality factor and barrier height for these devices were compared with the devices which had a second surface clean. The extracted values were tabulated and discussed. The ideality factors extracted from the I-V measurements and the barrier heights extracted from the C-V measurements were higher for the Batch I devices compared to the Batch II devices. It was suspected from these results that there was an oxide layer at the Cu/SiC interface when a surface clean was not performed before the Schottky contact deposition. This was later confirmed by performing XPS characterizations.

CHAPTER 7

SUMMARY AND CONCLUSIONS

In this research, Cu/4H-SiC/Ni Schottky diodes were fabricated, and the electrical characteristics and Schottky parameters are presented. The process steps followed in the fabrication of the diodes were complex, and were refined through several experiments. The first two samples fabricated exhibited poor electrical characteristics. A second surface clean was introduced into the process-flow just prior to the Schottky contact deposition, and this clean improved the electrical characteristics drastically. In our analyses, we categorized the samples without and with the second surface clean as Batch I and Batch II, respectively. Batch I yielded high ideality factors from I-V measurements and high barrier heights from the C-V measurements. These results indicated the presence of an interfacial oxide layer at the Schottky interface. This was confirmed by comparing the atomic compositions of the surfaces with and without a second surface clean, obtained using XPS measurements.

The Batch II diodes, which received a second surface clean, were categorized into Group A and Group B, based on their forward I-V characteristics. The Group A devices exhibited a single linear region over nearly eight orders of magnitude in their semilog I-V characteristics and were modeled using the Richard-Dushman equation. The extracted ideality factors were close to unity and the barrier heights were close to the Schottky Mott limit, indicating that performance of the Group A devices was close to that of an ideal Schottky diode. The Group B devices exhibited two linear regions in their forward semilog I-V characteristics. They were modeled as two Schottky diodes connected in

parallel, one with a lower barrier height than the other. This behavior was attributed to the presence of inhomogeneities at the Cu/4H-SiC interface, which resulted in localized barrier-lowering. The electrical parameters were extracted for the two regions separately, and it was found that the bulk of the contacts behaved similar to the Group A devices.

The results from this research represent some of the first experimental data on Cu/4H-SiC Schottky diodes. With the introduction of a second surface clean and the associated masking and etching sequences, we developed a controlled process to fabricate Schottky diodes which performed as excellent rectifiers. Further research could be directed towards the investigation and elimination of Schottky barrier inhomogeneities which caused the non-ideal behavior of the Group B devices.

APPENDIX

Group B – Extraction of Parameters

The Group B devices exhibited two linear regions in their forward semilog I-V characteristics. In Chapter 5, this behavior was explained using a model in which a fraction of the Schottky contact area exhibits a lower barrier height than the bulk of the contact. In section 5.14, it was explained how the different barrier heights and series resistances associated with the LSBH and HSBH contact areas result in their domination over the LVLR and HVLR portions of the forward characteristics, respectively. Based on this result, the general form of equation 5.5 can be fitted separately to the LVLR and HVLR regions, to extract the barrier heights and ideality factors of the LSBH and HSBH areas, respectively. In this appendix, using a Group B device from Sample III as an example, we describe the procedure followed to fit the forward I-V data to the predictions of this model. The forward semilog I-V characteristic for the same device was presented in Fig 5.6.

Step #1: Extraction of Series Resistance from Linear I-V Plot

The forward I-V characteristic of the device under study is plotted on a linear scale using a dotted line in Fig A-1. A linear region can be observed for forward biases above 1.4 V, until the analyzer's current compliance limit of 100 mA is reached at about 2 V. This region represents the forward ohmic current through the HSBH area, limited by the effective series resistance, R_{SH}.

So, the current in this region can be modeled as,

$$I = \frac{(V - V_{ON})}{R_{SH}}, \qquad \text{-- (A-1)}$$

where V_{ON} is the intercept of this linear region on the voltage axis. The general form of this linear model is given by

$$y = m1 + m2 * x, \qquad \text{-- (A-2)}$$

where y is the forward current (I), x is the applied forward bias (V), $m1 = -V_{ON}/R_{SH}$, and the slope $m2 = 1/R_{SH}$. Thus, the inverse of the slope of this linear fit, $1/m2$, gives the effective series resistance.

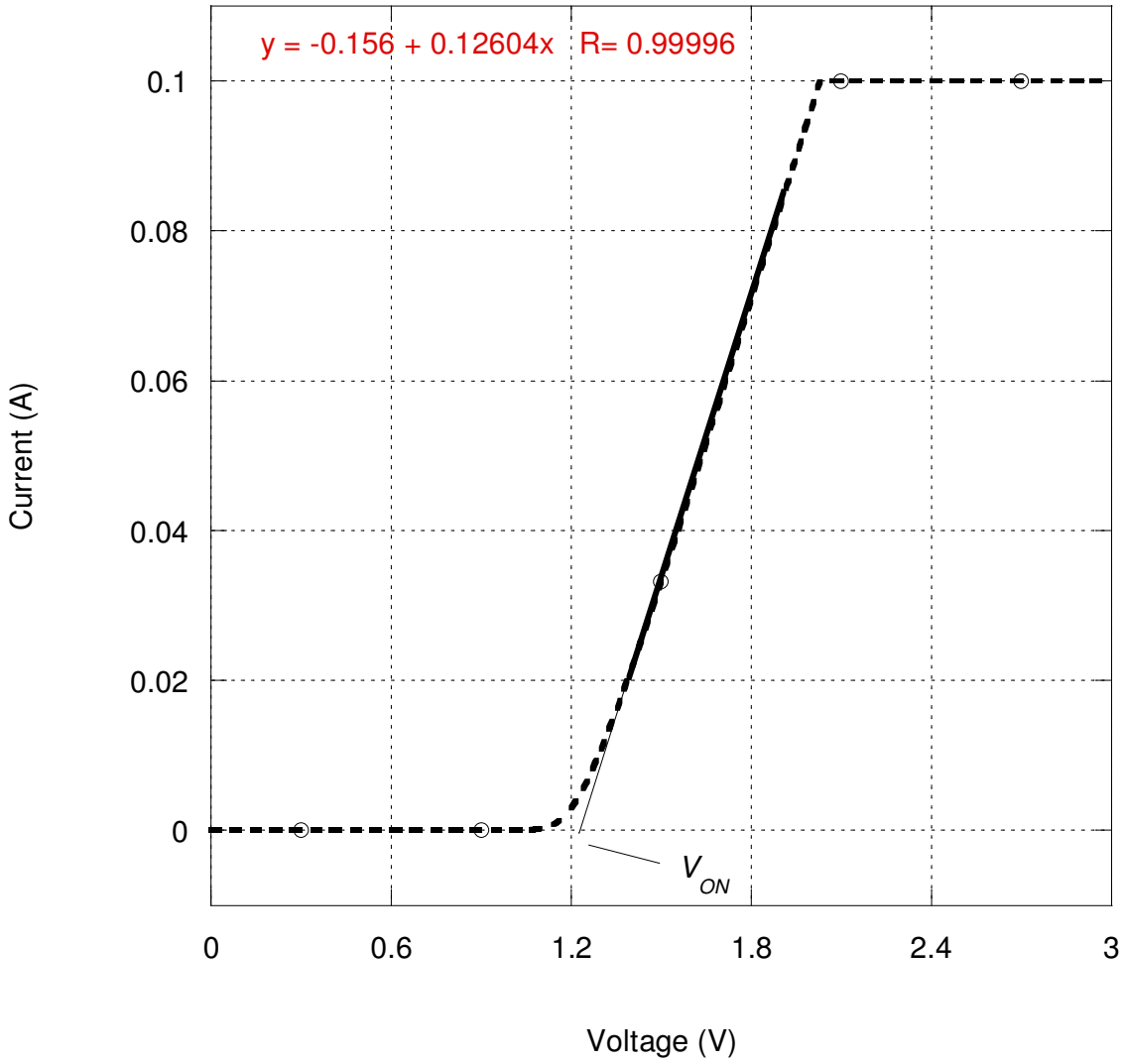


Fig A-1 Extraction of series resistance from linear I-V plot

The best linear fit for this particular device is $y = -0.156 + 0.12604x$, and appears as a solid line in Fig A-1. The correlation coefficient, R, for this fit is 0.99996, which is very close to unity and indicates that it is an excellent fit. The slope of this fit, $m2$, is 0.12604 in this case, so the effective series resistance is,

$R_{SH} = 1/m2 = 1/(0.12604) = 7.934\Omega$

The effective series resistance extracted above includes two components, R_c/A, which is the sum of the epilayer and substrate resistances, and R_p, which is the sum of the Ni-ohmic contact and the probe tip resistances. The R_c component can be estimated from equation 5.4, using the sample specifications and 4H-SiC properties, as shown below:

Epilayer thickness, $W_{epi} = 5 \text{ x } 10^{-4} \text{ cm}$

Epilayer doping concentration, $N_{Depi} = 5.0 \text{ x } 10^{15} \text{ cm}^{-3}$

Substrate thickness, $W_{sub} = 0.0345 \text{ cm}$

Substrate doping concentration, $N_{Dsub} = 4.8 \text{ x } 10^{18} \text{ cm}^{-3}$

Electronic charge, $q = 1.6 \text{ x } 10^{-19} \text{ C}$

Electron mobility in 4H-SiC [Table 2.1], $\mu = 900 \text{ cm}^{-2}/\text{V.s}$

Assuming that the electron mobility in 4H-SiC has the same value in both the epilayer and substrate ($\mu_{epi} = \mu s_{ub} = \mu$), from equation 5.4, we have,

$$R_c = \frac{1}{q\mu}\left(\frac{W_{epi}}{N_{epi}} + \frac{W_{sub}}{N_{sub}}\right) = \frac{1}{1.6\times10^{-19}\times900}\left(\frac{5\times10^{-4}}{5\times10^{15}} + \frac{0.0345}{4.8\times10^{18}}\right)$$

$R_c = 6.994375 \text{ x } 10^{-4} \text{ ohm.cm}^2$

Schottky contact diameter, $d = 0.063 \text{ cm}$

Schottky contact area,

$$A = \pi*(d/2)^2 = 3.14*(0.063/2)^2 = 0.00312\ cm^{-2}$$

The effective series resistance, $R_{SH} = \frac{R_c}{A} + R_p$. Thus, the sum of the Ni-ohmic contact and probe tip resistances can now be obtained as,

$$R_p = R_{SH} - \frac{R_c}{A} = 7.934 - \frac{6.994\times10^{-4}}{0.00312}$$

$$R_p = 7.7098\ \Omega$$

Step #2: Extraction of LSBH parameters

The LSBH parameters, such as the fraction of the total Schottky contact area, ε, barrier height, ϕ_b^L, and the ideality factor, n_L, can be extracted from the linear region of the semilog I-V characteristics observed at low forward biases. This LVLR portion of the I-V characteristic, for the example device is presented in Fig A-2, with the axes interchanged. As discussed in section 5.1.4, this region can be modeled using the general form of equation 5.6 given by,

$$y = m1 * \ln(M0) + m2 * M0 + m3, \qquad \text{-- (A-3)}$$

where,

$$m1 = \frac{n_L kT}{q},\ m2 = \frac{R_c}{A\varepsilon} + R_p, \text{ and } m3 = n_L\phi_b^L - \frac{n_L kT}{q}\ln\left(A\varepsilon A^* T^2\right) \qquad \text{-- (A-4)}$$

The best fit for this region, as seen from Fig A-2, has an excellent correlation coefficient of 0.99997. The values of the coefficients *m1*, *m2* and *m3* corresponding to this fit are then substituted into equation A-4 to extract the LSBH parameters.

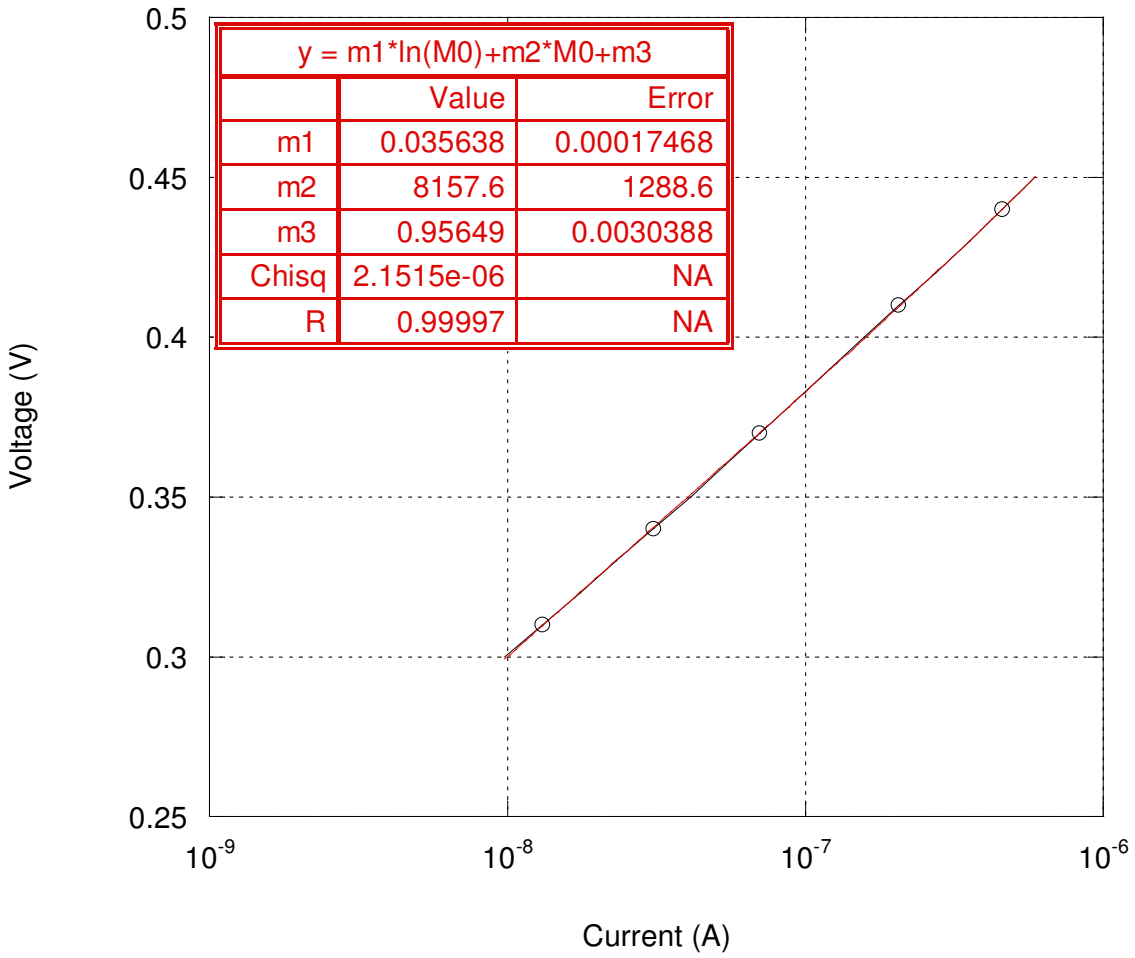


Fig A-2 Best Fit for LVLR

From equation A-4,

$$m1 = \frac{n_L kT}{q} = 0.035638$$

Substituting the value of thermal voltage at room temperature, *kT/q = 0.0259 V* into the previous expression, we get,

$$n_L = 1.376$$

Before we extract the barrier height from *m3*, we need the value of ε. This can be extracted from *m2* using the values of R_c and R_p obtained in Step #1. From equation A-4,

$$m2 = \frac{R_c}{A\varepsilon} + R_p = 8157.6$$

Using the values, R_c = *6.994375* x 10^{-4} *ohm.cm*^{2}, *A = 0.00312* cm^{-2}, and R_p = *7.7098* Ω, obtained in Step #1,

$$\varepsilon = 0.2242/(8157.6 - 7.7098)$$

$$\varepsilon = 2.751e\text{-}5$$

Finally, we substitute the values of n^L and ε into the expression for *m3* in equation A-4, to get the barrier height.

$$n_L \phi_b^L - \frac{n_L kT}{q} \ln\left(A\varepsilon A^* T^2\right) = 0.95649$$

$[\phi_b^L - 0.0259*\ln(0.00312*2.751e\text{-}5*156*90000)]*1.376 = 0.95649$

$\phi_b^L = 0.7$ eV

Step #3: Extraction of HSBH parameters

The HSBH parameters, such as the barrier height, ϕ_b^H, and the ideality factor, n^H, can be extracted from the HVLR region following a procedure very similar to the one described in Step#2. The HVLR portion of the I-V characteristic, for the example device is presented in Fig A-3, with the axes interchanged. This region can be modeled using the general form of equation 5.7 given by,

$$y = m1 * \ln(M0) + m2 * M0 + m3, \quad \text{-- (A-5)}$$

where,

$$m1 = \frac{n^H kT}{q},\ m2 = \frac{R_c}{A(1-\varepsilon)} + R_p, \text{ and } m3 = n^H \phi_b^H - \frac{n^H kT}{q}\ln\left(A(1-\varepsilon)A^* T^2\right) \quad \text{-- (A-6)}$$

The best fit for this region, as seen from Fig A-3, has an excellent correlation coefficient of 0.99978. The values of the coefficients *m1*, *m2* and *m3* corresponding to this fit are then substituted into equation A-6 to extract the HSBH parameters.

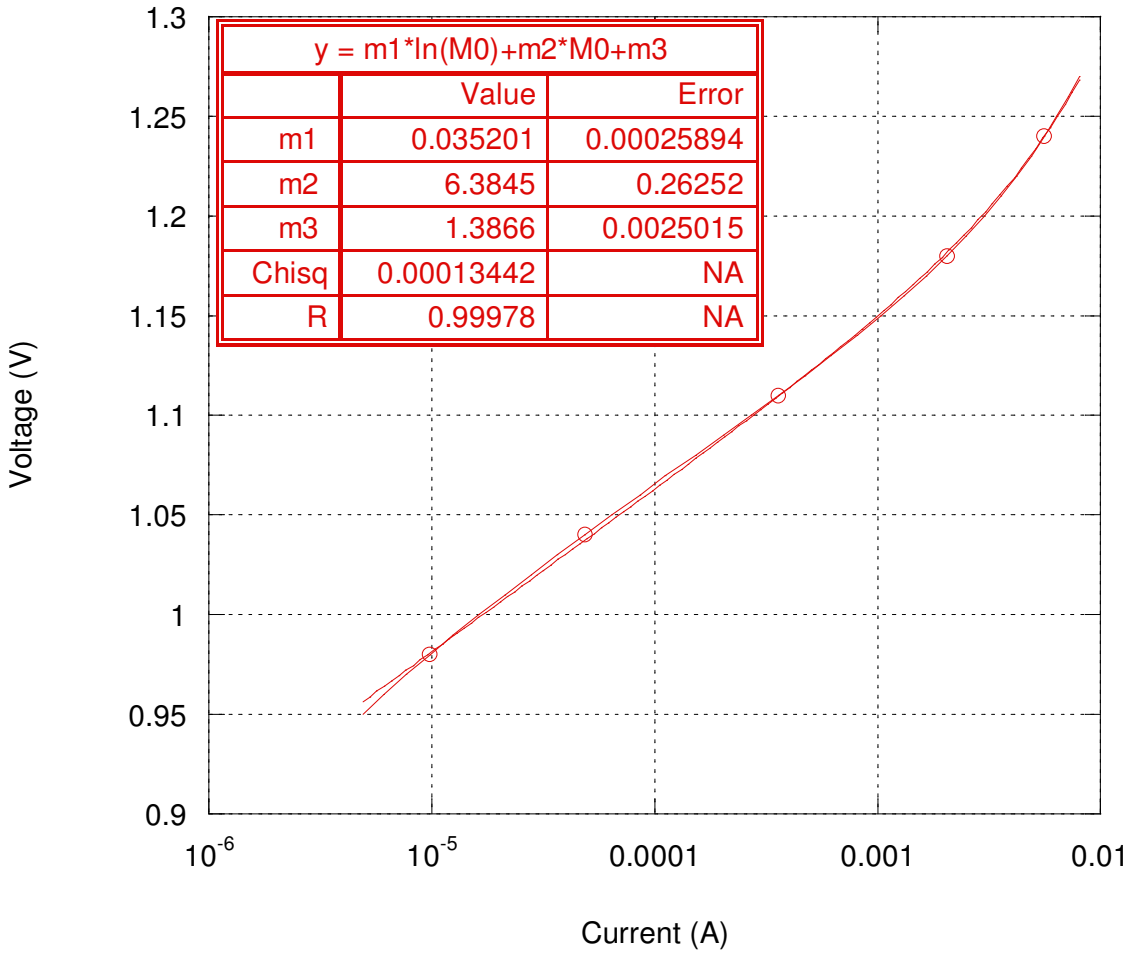


Fig A-3 Best Fit for HVLR

From equation A-6,

$$m1 = \frac{n^H kT}{q} = 0.035201$$

Substituting the value of thermal voltage at room temperature, $kT/q = 0.0259\ V$ into the previous expression, we get,

$$n^H = 1.376$$

Finally, we substitute the values of n^H and ε into the expression for *m3* in equation A-6, to get the barrier height.

$$n^H \phi_b^H - \frac{n^H kT}{q} \ln\left(A(1-\varepsilon)A^* T^2\right) = 1.3866$$

$$[\phi_b^H - 0.0259*\ln(0.00312*156*90000)\}*1.359 = 1.3866$$

$$\phi_b^H = 1.3 \text{ eV}$$

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