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A DUAL INPUT BIDIRECTIONAL POWER CONVERTER FOR CHARGING AND DISCHARGING A PHEV BATTERY

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A DUAL INPUT BIDIRECTIONAL POWER CONVERTER FOR CHARGING AND DISCHARGING A PHEV BATTERY

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ABSTRACT

This thesis looks at a new design for a dual input bidirectional power converter (DIBPC) for charging and discharging a PHEV battery. The design incorporates a power factor correcting rectifier aimed at optimizing the battery charging efficiency from either a 120 V_{AC} or 240 V_{AC} source or discharging the battery to a usable AC voltage at 120 V_{AC}. For simplicity and cost-effectiveness, the DIBPC is constructed using a standard IGBT 6-pack intended for motor control. The DIBPC is designed specifically to provide efficient operation with 120 V_{AC} and 240 V_{AC} inputs while achieving a very low THD_I. The DIBPC also needs to be able to provide AC output power at 120 V_{AC} with the flexibility to output at 240 V_{AC} in the future.

The DIBPC was tested first in simulation, and then in experimentation. The DIBPC consists of two portions, an AC/DC converter and a DC/DC converter. Although both were simulated, only the AC/DC converter was constructed. Testing under various load values and in each mode of operation provided ample data to show the DIBPC can meet all design goals.

When operating as a rectifier, the DIBPC produces between 7.4% and 13.35% THD_I and a DC voltage ripple of 8 V_{P-P} or less at 400 V_{DC}. At 120 V_{AC} and 240 V_{AC} an efficiency of 84.5% and 94.6% was achieved, respectively. When operating as an inverter, the DIBPC produces less than 6% THD_V and 7% THD_I, while outputting a voltage between 114 and 128 V_{RMS}. Overall, the THD_I in the charging mode easily meets and exceeds all standards and design constraints set forth, including IEC 61000-3-4. The efficiency with a 120 V_{AC} input, however, is less than expected – about 84%.

ACKNOWLEDGMENTS

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CHAPTER ONE

BACKGROUND

This thesis presents a modification of existing technology for a power converter designed specifically for the charging and discharging of a PHEV battery, herein called the Dual Input Bidirectional Power Converter (DIBPC). This chapter first provides the motivation driving need for this technology. Next, the many aspects of the problem are discussed. Once the problem is laid out, the power factor correcting rectifier is introduced as a solution. Finally, the existing technologies used to address these issues and accomplish these goals are considered and the pros and cons for each technology are weighed.

Motivation

Recent improvements in key technologies, including batteries and power electronics, have provided the technological means to the construction of hybrid electric vehicles. However, the technical superiority of hybrid electric vehicles has not solely moved them into the mainstream automotive market. Social and political trends have played a vital role in creating a popular niche for the hybrid electric vehicle.

For a long time now, the US has relied on large amounts of petroleum imports to supply gasoline and diesel to the transportation sector. As a result of this, many people are looking for ways to reduce their petroleum consumption. Hybrid electric vehicles have helped to provide a way for many people to do this.

Reliance on an imported petroleum is not the only sociopolitical factor which has proven to be favorable for the advancement of the hybrid electric vehicle. As more people are becoming aware of their environmental impact, they are looking for many ways to reduce their environmental footprint. One of the most obvious solutions available to most people is to reduce the use of internal combustion engines, a primary consumer of petroleum. The burning of gasoline or diesel produces various toxic and greenhouse gases which have been attributed to global climate change.

The success of the hybrid electric vehicle in both domestic and foreign markets has assured its continued place in the automotive industry. The hybrid electric vehicle incorporates an electric motor and generator along with some power electronics and a large battery to provide a more efficient alternative to a vehicle with only a combustion engine.

The hybrid electric vehicle comes in two forms. The first, and most common, is the parallel hybrid electric vehicle. The parallel hybrid electric vehicle is the most common because it is the most similar to a traditional combustion engine powered vehicle, and it is typically the cheapest. The parallel hybrid vehicle uses both an electric motor and the combustion engine to provide power directly to the wheels. Because the combustion engine provides power directly to the wheels, a transmission is still needed in this configuration. The battery is charged from an electric motor during regenerative braking and from power provided by the combustion engine when needed.

The second form of the hybrid electric vehicle is the series hybrid. The series hybrid electric vehicle is more closely related to a purely electric vehicle than a

combustion engine vehicle. The series hybrid electric vehicle, while being simpler in concept, is more expensive to construct. The series hybrid uses an electric motor only to provide power to the wheels. The combustion engine is only used to provide power to charge the batteries. One of the advantages of this configuration is that there is no need for a transmission. Series hybrid electric vehicles are currently in use in heavy equipment. Locomotives and large ships already use the series hybrid layout where they use a diesel generator to power electric motors. Because the engine is only used to generate electricity, it can be designed to work in a very small power band, increasing the operating efficiency of the combustion engine.

Hybrid electric vehicles provide a more efficient alternative to a pure combustion engine. They do not, however, release the dependence upon petroleum. If hybrid electric vehicles can be viewed as the first step towards achieving that aim, plug-in hybrid electric vehicles (PHEVs) can be viewed as the second step towards that same goal. A PHEV is, in its most basic form, a hybrid electric vehicle with the ability to recharge the battery from utility supplied AC power. A PHEV generally follows the same configuration as a series hybrid, with a couple of important differences. A PHEV generally contains a significantly larger battery along with power electronics that allow the battery to be charged from an external electrical power source, the power grid.

While PHEVs are not yet in full-scale production from a major automotive manufacturer, conversions and custom made PHEVs by small specialized companies can be obtained. A PHEV has all the advantages of a series hybrid electric vehicle with the additional advantage of having an “electric-only” range that is subsidized from the power

grid. Based on tests with existing conversion vehicles, PHEVs have easily achieved over 100 mpg by utilizing the battery charge from the power grid [1].

As the first PHEVs are mass produced and marketed, they are expected to have an electric only driving range that is sufficient to encompass the daily commute of most drivers. This will allow a typical commuter to drive to and from work with little need to use the combustion engine. If the driver then charges the PHEV each night before work, theoretically the majority of the driving will use just the energy from the grid. While PHEVs still rely on another form of energy (typically gasoline), they enable future technologies to supplant that as they become available.

As the power grid becomes cleaner from the use of renewable energy and alternative forms of energy, this means the electric charge on the PHEV will further reduce the production of pollutions and greenhouse gases associated with burning fossil fuels. As battery and power electronic technology improves, this will also increase the length of the electric driving range and further reduce the use of the combustion engine in the vehicle. The current state of PHEV technology and the predicted road of future progress in this field have made the prospects of PHEVs as a prominent holder of the market share a very real likelihood in the near future.

Because so many PHEVs may soon be in production, details surrounding the charging and discharging of these PHEV batteries have given rise to many questions and possibilities. The Chevy Volt, one of the first PHEVs slated to go into production, will contain a battery with approximately 16 kWh of energy storage [2]. This is a significant amount of energy, which will require a significant amount of power and time to charge it.

Many concerns regarding the capacity of the existing power grid have been raised in light of this possible increased load. If many PHEVs are adopted, it could result in a significant boost in power consumption.

PHEVs are uniquely flexible – they can be charged at any time and then have the battery energy available for use when needed. If a charger was provided with feedback from the utility grid, it could govern the charger to operate at optimal off-peak times, limiting the additional peak power that must be supplied by the grid. If a charger is made sufficiently adaptable, it could use supplied feedback from the grid along with a user programmable schedule to determine the best charging time during the day, making it "smart grid" enabled.

Problem Statement

There are several design issues surrounding the PHEV battery charger discussed in this section. On a high level, the constraints that most greatly affect the design of a PHEV battery charger are: the minimization of input current harmonics, the ability to accept 120 V_{AC} and 240 V_{AC} and the ability to transfer high power bidirectionally.

As more and more devices, including PHEVs, require a substantial amount of DC power, the need to control harmonic distortion arises. A typical "dumb" single phase AC – DC converter consists of a half-bridge or full-bridge set of diodes, which rectify AC to DC and charge a capacitor. The charging of a capacitor through diodes creates a large amount of input current harmonics. In sufficient quantity, harmonics can be detrimental

to almost every aspect of the power grid, including transformer derating, voltage drops and power losses in the distribution system.

In the US, IEEE develops the standards which govern things such as harmonic distortion; in Europe and elsewhere, IEC performs the same task. IEEE currently has no standards for harmonic content on end use devices; however IEC standards are in place which limit current harmonics. Total harmonic distortion (THD) is the standard measurement used to rate the amount of harmonic distortion present in a waveform. These standards impose limits on the amount of total harmonic distortion in the current (THD_I). The details of these standards will be discussed in the next chapter.

In order to be flexible enough to operate internationally, adhering to harmonic standards is not the only requirement. A PHEV charger would also need to have a wide range of input voltages. Because most PHEVs would, assumedly, be charged in residences, residential voltage sources must be used. For the US, 120 V_{AC} and 240 V_{AC}, 60 Hz are the typical values and in Europe, 220 V_{AC} 50 Hz is the norm. Therefore this wide range of operating input voltages would be desirable. Because the PHEV charger would be charged in a residential application, typical residential electrical power limitations apply. In the US, a typical circuit breaker on a 240 V_{AC} system would be 30 A. Using this as a limitation for the power that can be converter by the PHEV charger, 7.2kW of input power would be the power limitation at 240 V_{AC}.

If the development of PHEV technology continues to mature, a unique opportunity for PHEVs exists to benefit the stability of the power grid. If a complete and uniform set of standards are developed for safety and compatibility, PHEVs could also

provide a means for distributed energy storage through the power grid. If a large number of vehicles with partially or fully charged batteries are available on the grid during peak hour loading, utility companies could use those batteries to improve grid stability and reduce the need for low-efficiency peak-time generators.

In order for the utility company to use these batteries as distributed energy storage, the power converters between the vehicle and the utility grid would have to be bidirectional. Bidirectional power flow between the utility and the vehicle creates several issues that have to be addressed. One of the most important issues is safety. A house with a vehicle discharging power to the grid appears as a distributed energy source that is not known to the utility company. Among other issues, not always knowing the direction of the power flow in a distribution line can leave doubt as to whether or not a circuit breaker or switch can actually protect the system it intends to protect or disconnect.

In the US, residential 240 V_{AC} is provided from a transformer with a center tapped neutral. Therefore two voltage magnitudes are available from the same transformer, 120 V_{AC} and 240 V_{AC}. Two 120 V_{AC} lines are available, each with opposite polarity relative to the neutral. A transformer diagram and a phasor diagram of this can be seen in Figure 1.1. For the PHEV charger to operate bidirectionally, it needs to provide support for this installation.

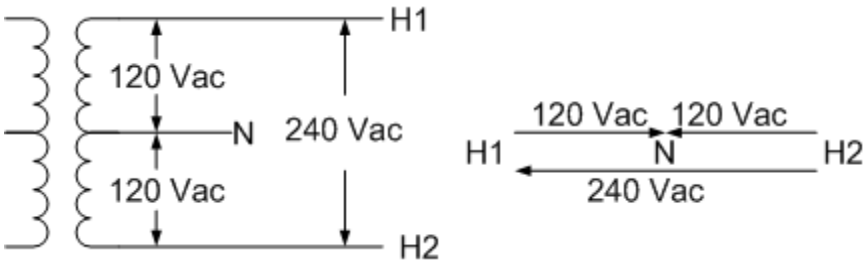

Figure 1.1: Typical US Residential Electrical Service

A power converter which can meet all of these tasks needs to be considered. A power converter needs to be able to charge a very high storage battery, perhaps 16 kWh or more. The power converter needs to be able to charge it quickly and without exceeding any current or future harmonic standards. Because the design is aimed at a typical residential application, the converter needs to operate within the bounds of a typical installation for 120 V_{AC} or 240 V_{AC} in the US or 220 V_{AC} in Europe. Finally, the converter needs to be able to discharge the battery and invert it for use as backup power or auxiliary power when the power grid is disconnected. The next section discusses how existing technology would meet these goals and the shortcomings they may have.

Power Factor Correcting Technology

PHEV battery chargers are not anything completely unique. The concept of a high power AC to DC rectifier is not new. Existing rectifiers are currently used in many applications where batteries are needed to be charged or where a DC motor or variable frequency drive is operated. Due to the limitations placed on harmonic content and the

side effects created by harmonic content, most large power rectifiers incorporate some means of power factor correction.

The term power factor correcting or power factor correction (PFC) technology refers to a device whose function is to improve the true power factor. True power factor, as opposed to displacement power factor, is defined as $\frac{P}{|S|}$ or $\frac{Real\ Power}{Apparent\ Power}$. Displacement power factor is defined as $cos(\theta_{v1} - \theta_{i1})$, where θ_{v1} and θ_{i1} are the phase angles of the fundamental frequency of the voltage and the current, respectively. For a perfectly sinusoidal waveform, the displacement power factor and true power factor are the same. When harmonic content is present, however, these two values can vary greatly. The true power factor can be greatly reduced by the presence of harmonic content in either the voltage or the current.

The difference between the true power factor and the displacement power factor is illustrated with two simulated waveforms in Figure 1.2. The blue waveform is a true sinusoidal waveform which represents the input voltage to a diode rectifier. The black waveform is a distorted waveform which represents the input current to a diode rectifier.

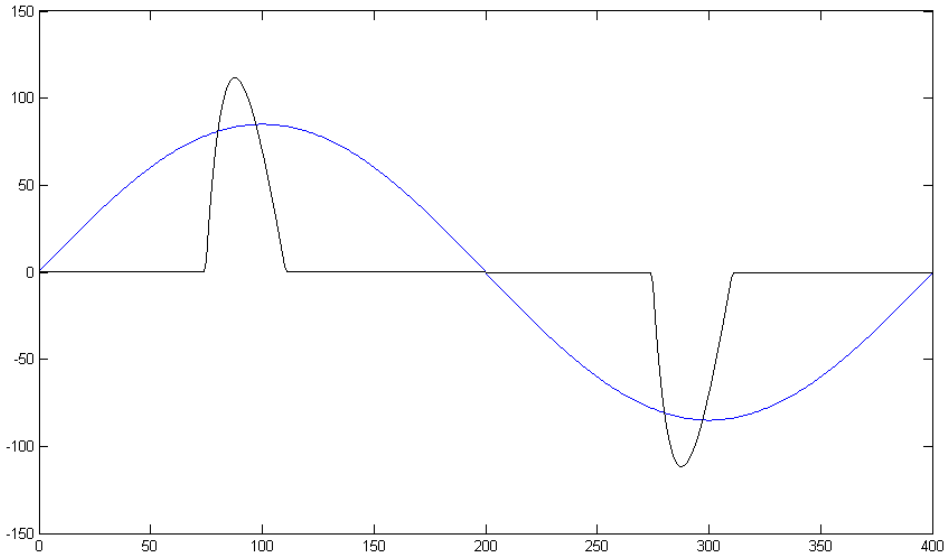

Figure 1.2: Simulated Rectifier Voltage and Current

The phase angles of the fundamental frequency for both of these waveforms are close to the same, only varying by about 8.5º; therefore the displacement power factor is 0.989. The true power factor, shown in Equation 1.1, is calculated by dividing the real power by the apparent power, which contains the harmonic content.

$$pf = \frac{P}{|S|} = \frac{V_{RMS(1)} * I_{RMS(1)} * \cos(\theta)}{V_{RMS} * I_{RMS}} = 0.54 \quad (1.1)$$

The harmonic content present in the distorted current waveform has created a true power factor that is much lower than the displacement power factor. As the true power factor gets closer to 1, the harmonic content present in both the voltage and the current is

reduced. Therefore when a device has power factor correction, it not only improves the phase shift between the voltage and current, but also reduces the harmonic content.

Power factor correcting (PFC) rectifiers are designed to convert AC to DC without producing the large amount of harmonics associated with a typical diode rectifier and DC filter capacitor. A PFC rectifier can be constructed as a passive device or an active device. Passive PFC rectifiers contain a low pass or a band pass filter to improve the true power factor by filtering out some of the undesirable harmonics. These produce very limited results, however, due to the hard to filter low frequency harmonics typically created by a diode rectifier. Because active PFC rectifiers typically result in much better power factor correction than passive PFC rectifiers, they are favored in applications requiring a significant power factor improvement.

An active PFC rectifier is typically designed by taking a rectifier and attaching a DC to DC converter. In order to illustrate the operation of a PFC rectifier, one of the most basic PFC rectifier designs is considered. This basic PFC rectifier design consists of a diode rectifier followed by a DC to DC boost converter. The boost converter is made up of an inductor, a diode, a switch (such as an IGBT or MOSFET) and a capacitor. The circuit can be seen in Figure 1.3.

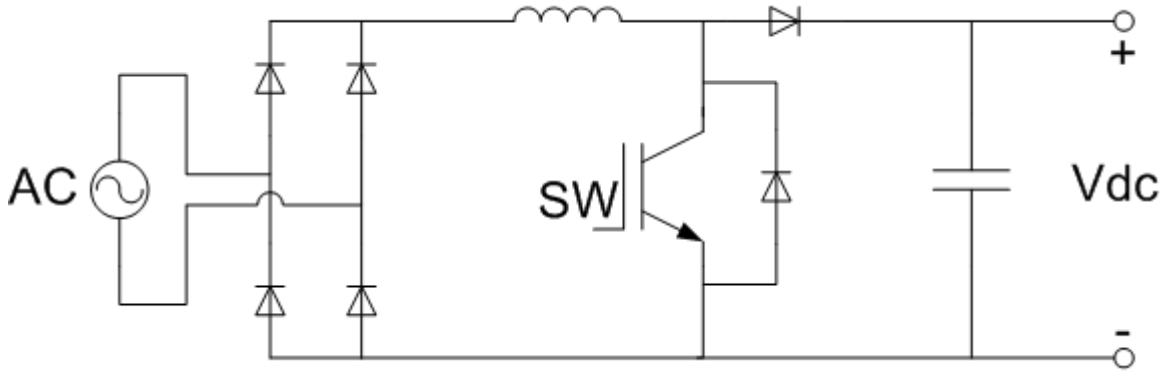

Figure 1.3: Typical PFC Boost Rectifier

A typical rectifier only charges the capacitor when the input voltage is greater than the capacitor voltage, near the peak of the voltage waveform. This only allows current to flow near that peak. In order to improve the power factor, current needs to flow at all points in the waveform, mimicking the voltage. In order to do this, the inductor is switched on and off very quickly. This allows current to spool in the inductor when the switch is closed. When the switch is closed, the voltage quickly rises across the inductor ($V_L = L * \frac{di_L}{dt}$). This rise in voltage forward-biases the diodes and allows current to flow into the capacitor. By modulating the switch, the input current can be made to follow the input voltage.

One undesirable effect of improving the input current waveform this way, is the DC voltage ripple present at twice the line frequency. The DC voltage ripple for a 60 Hz input voltage would be 120 Hz. This voltage ripple can be explained by considered the power balance. Because the current waveform now looks like the voltage waveform, the instantaneous power is greatest at the peak of these waveforms. This input power

decreases the closer you get to the zero crossing, and eventually reaches zero before increasing again. This varying input power results in a fluctuation of the voltage of the DC bus capacitor because the output power should remain essentially constant.

To mitigate this dc voltage ripple at twice the line frequency, some PFC rectifiers incorporate another DC / DC converter as a second stage. This DC / DC converter operates at a switching frequency fast enough to respond to the changes of the DC bus voltage resulting from the voltage ripple. The second stage DC / DC converter can easily provide a DC voltage output with very low ripple. Some PFC rectifier topologies are specifically designed to reduce the DC voltage ripple that is present without the addition of another DC / DC stage. These and other PFC rectifier technologies will be discussed in the following section.

Existing Technology

The present state of existing technology is a somewhat open ended question, in this field. Because PHEVs are not yet readily available in the current market, much of the PHEV charger designs are proprietary and/or contracted from other suppliers, . Because so many of the designs used for these applications are trade secrets, very little documentation regarding them is available. For this reason, the list of existing technology contains only the designs that are available through corporate or academic publications. Some of the relevant designs can be seen below.

Existing converters that could be used for PHEV battery charging applications can be broken down into two distinct groups. They can be distinguished based on their ability to discharge the battery back to a AC voltage. Therefore the following list will be broken down into two groups as well. First, the PFC rectifiers which can only operate unidirectionally to charge the battery are considered. While Unidirectional PFC rectifiers will not work for this application, two are discussed to demonstrate some of the techniques used to correct the power factor of a rectifier circuit. Next, the converters which can be operated bidirectionally (PFC rectifiers and inverters) are discussed.

The most common unidirectional PFC rectifier circuit can be seen above in Figure 1.3. This PFC rectifier is the most basic, containing the fewest components, and is therefore the cheapest and easiest to control. The drawbacks of this design, however, are the inefficiency, the inability to perform bidirectionally and the limited power factor correcting ability. This design operates with a lower efficiency because more semiconductor junctions are crossed. This design is generally used for low power, low cost applications. Because of these limitations, it is not suited for this application.

Now, one other, more specific application oriented PFC rectifier is examined. Figure 1.4 shows a PFC rectifier designed by Tyco Electronics [3]. This is a production system that can be bought as a PFC rectifier assembly. This is an excellent unidirectional PFC rectifier with a simple, cost effective and efficient design.

This topology is designed to minimize the number of semiconductor junctions that are crossed. It is designed to operate at up to 6kW, 160kHz switching frequency, 400V DC output. Experimentation has shown a 97.4% efficiency with an input voltage

of 230V AC and a 94.8% efficiency with 120V AC input. For unidirectional PFC rectifier applications, this design would be the most suited for the power levels, cost and efficiency requirements for the power converter. This design, however, does not allow for the flow of power in the opposite direction, thus is cannot be used for this application.

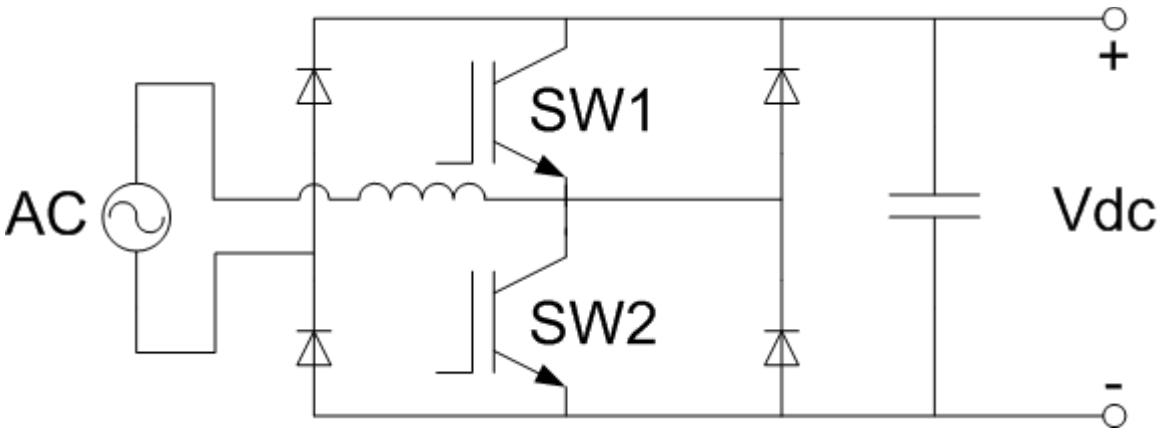

Figure 1.4: Tyco Dual Boost PFC Rectifier

The next design is very similar to the first PFC boost rectifier. It simply contains a couple more components. This topology was of interest because of the zero voltage transition cell, highlighted in Figure 1.5. Because this topology uses resonance to drive the voltage across the switch nearly to zero before switching, it has better switching characteristics and improved efficiency [4]. However, this ended up not being applicable due to its inability to operate bidirectionally.

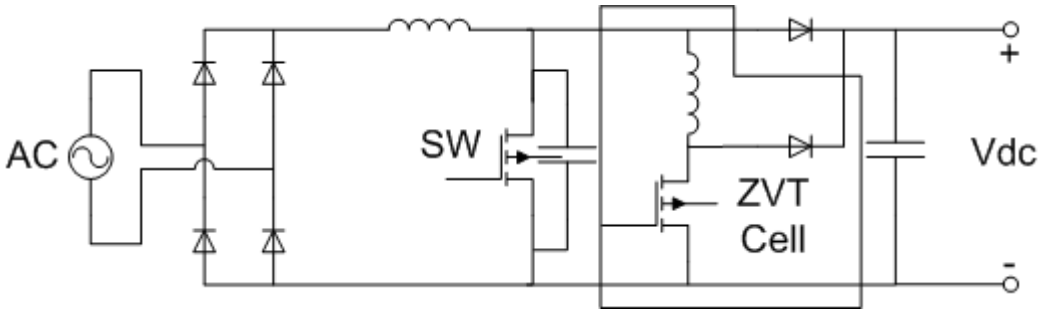

Figure 1.5: Zero Voltage Transition PFC Boost Rectifier

The interleaved full bridge rectifier with voltage doubler, seen in Figure 1.6, is an interesting solution. With this scheme, the converter can provide additional capability to double the voltage when rectifying 120V versus 240V AC by introducing a second capacitor, the boost capacitor. This increases efficiency with 120V AC input. However, there are a couple of serious drawbacks. To make this scheme operable bidirectionally, a non-trivial amount of semiconductor switches would have to be added and the bridge rectifier would have to be a fully controlled bridge with IGBTs. This would prove to be overly complicated and cost-prohibitive.

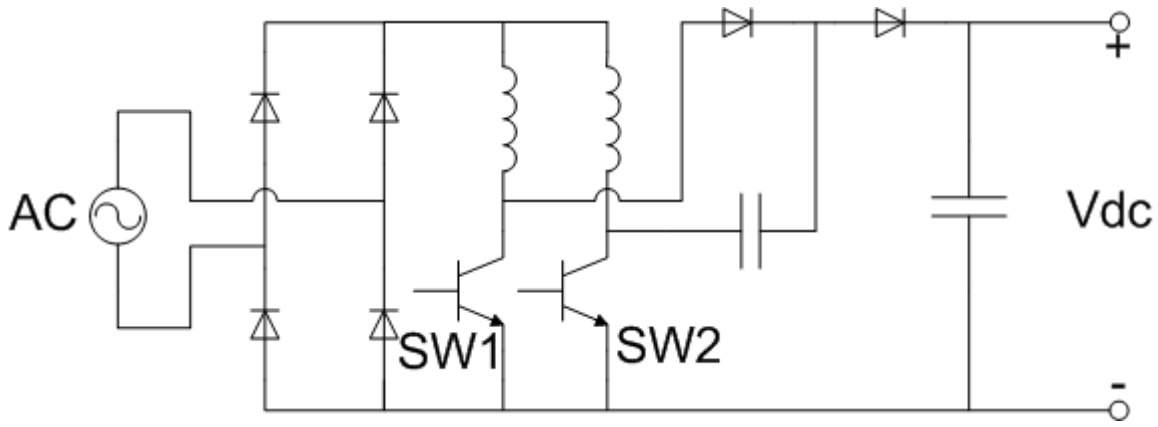

Figure 1.6: Interleaved Full Bridge Rectifier with Voltage Doubler

There are a wide array of unidirectional PFC rectifiers currently utilized, however, not nearly as many bidirectional PFC rectifiers. Next, some of the existing bidirectional PFC rectifiers are examined. A comprehensive review of all the significant PFC rectifiers, including bidirectional rectifiers, was performed in 2003 [5]. This review included several bidirectional PFC boost rectifiers, and those are discussed below. Most of the bidirectional designs are referenced from this comprehensive review.

For PHEV specific applications, some implementations have shown a combined AC to DC bidirectional converter and motor inverter [6]. This is an interesting design because it uses the motor windings as the spooling inductors for the PFC rectifier circuit. Seen below in Figure 1.6, the converter can be used for multiple purposes. When the vehicle is in operation, the converter is used as a DC to AC inverter for motor control. However, when the vehicle is being charged, the converter acts as an AC to DC PFC rectifier.

The contactors shown in K1, K2 and K3 allow the converter to utilize the windings of the motor as a PFC rectifier choke (inductor) for spooling current. Because this topology is designed to be used as a DC to AC inverter for motor control, it could also operate bidirectionally to discharge the battery back to the residential AC. This topology provides a unique method to reuse existing components, however at this point the design is simply a concept that depends on unknown components inside of the PHEV.

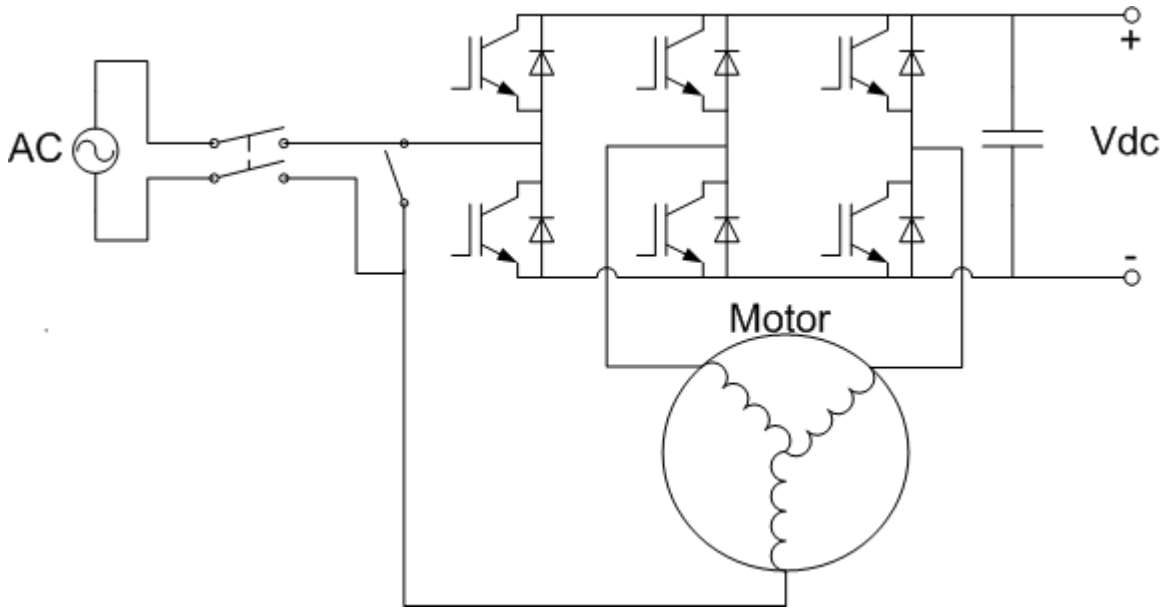

Figure 1.7: Combination AC to DC Converter and Motor Inverter

Figures 1.8 and 1.9 show similar bidirectional PFC boost rectifiers. The rectifier seen in Figure 1.8 has the addition of a third IGBT leg. This third IGBT leg allows the addition of the capacitor midpoint. This third leg can be switched in such a way as to provide mitigation for the DC voltage ripple seen at twice the line frequency [5]. The topology seen in Figure 1.9 has an inductor connected between two of the line IGBT legs.

This inductor serves the same purpose as the capacitors seen in Figure 1.8 by spooling current through the third IGBT leg to supply current which cancels out the current ripple in the capacitor. These designs would not require a second stage DC to DC converter. These designs are also not optimized for multiple input voltages, however, concentrating instead on filtering the dc output voltage.

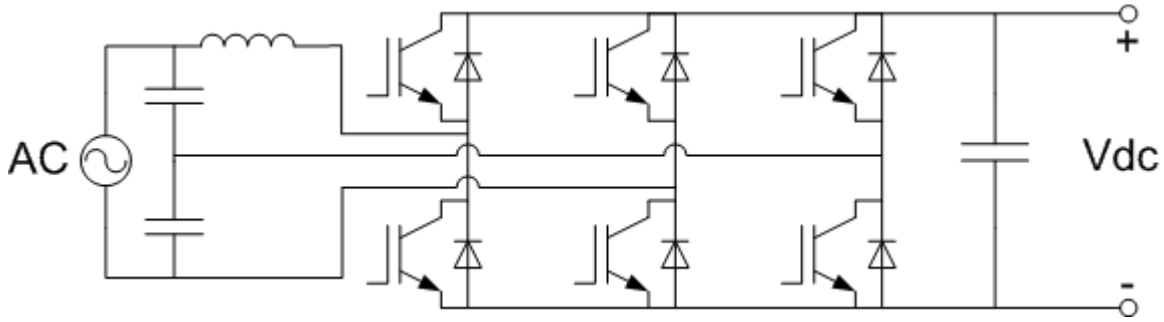

Figure 1.8: Bidirectional PFC Boost Rectifier with Capacitor Midpoint Ripple Mitigation

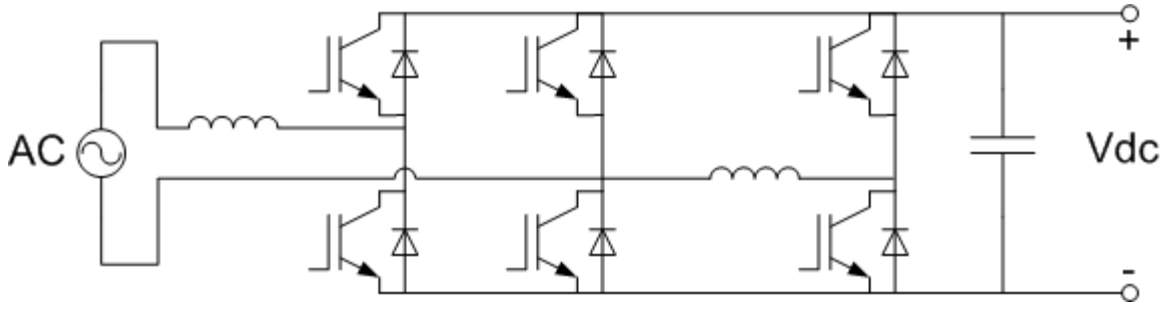

Figure 1.9: Bidirectional PFC Boost Rectifier with Third Leg Inductor Ripple Mitigation

The most basic bidirectional PFC rectifier is shown below in Figure 1.10. This simple design effectively provides the AC to DC or DC to AC conversion, but is not the

most efficient design. It does not provide any filtering for the DC voltage ripple which is present at twice the line frequency. It also does not operate as efficiently at varying input line voltages as it does at its designed line voltage. This design would require a DC to DC converter to filter the ripple at twice the line frequency.

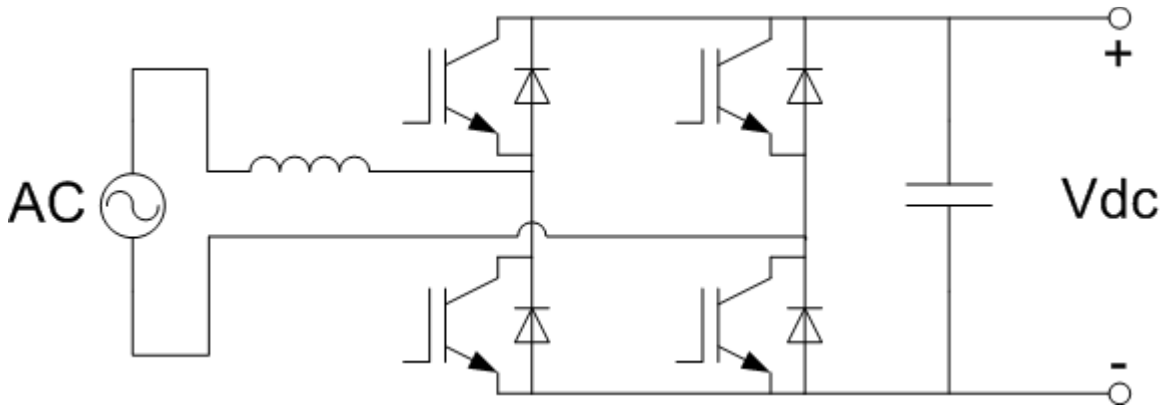

Figure 1.10: Simple Bidirectional PFC Boost Rectifier

While there are certainly other existing PHEV battery charger topologies, these are the most relevant and comparable topologies available in publications. Because of the specific design constraints of this PHEV battery charger, none of these optimally meet the design criteria. The basic bidirectional PFC boost rectifier seen in Figure 1.10 is the most closely suited to the needs of this application.

The design found in Figure 1.10 does not provide adequate flexibility for operation with multiple input voltages. The components for this topology would have to be designed to operate ideally at 240 V_{AC}. For this reason, the efficiency at 120 V_{AC}

would be significantly lower than at 240 $V_{AC.}$ Also, when inverting, this topology could only invert to 120 V_{AC} or 240V_{AC}.

Summary

This chapter discussed the background behind PHEVs and their relevance in today's world. The technology associated with the charging and discharging of the batteries and the technological problems that inherently need solutions were then considered. Finally, the existing technology that meets these goals was listed, along with the pros and cons of each.

Because none of these known existing technologies satisfactorily meets all the listed design constraints, a new bidirectional PHEV battery charger is proposed. The details of the constraints that govern the design along with the details of the design can be found in Chapter Two.

CHAPTER TWO

DESIGN OF THE DUAL INPUT BIDIRECTIONAL POWER CONVERTER

The existing technology offers several solutions to meet the goals of the PHEV battery charger and discharger. Through the study of the existing technology and comparisons of how it suits the existing need, a modified PFC rectifier design has been designed, simulated and constructed. This operation of the modified PFC rectifier design, herein called the Dual Input Bidirectional Power Converter (DIBPC) is discussed in detail in this chapter. First, the different stages and overall top down control scheme is discussed. Next, the constraints which govern the design are individually discussed followed by a detailed explanation of the design topology and operation. Finally, the method used for sizing and rating components is discussed.

Design Concept

The DIBPC is designed in two stages that can be broken up according to their general function, an important concept to note when considering the design. One stage, the AC/DC stage, takes an AC voltage and provides a constant DC output voltage or takes a constant DC voltage and inverts to a 120 V_{AC} output. The other stage, the DC/DC stage, takes a constant DC voltage and outputs a varying DC voltage to the battery or takes a varying DC voltage from the battery and outputs a constant DC voltage to the DC bus.

These two stages are both controlled by a single master controller. This master controller communicates directly with the battery, the AC/DC stage and the DC/DC stage of the DIBPC. Because the DIBPC is designed to operate with multiple battery types, the master controller must dictate the charging profile to both stages of the DIBPC. This controller must oversee the controllers for the two stages and ensure that they are providing the correct output to the battery in the charging mode,

Most batteries have two modes of operating during their charging. First, during the lower state of charges, they operate in a current limit mode. The voltage is varied so that the maximum current is reached and maintained. The other mode of operation is voltage limit mode. Once the battery nears its full state of charge, it will usually need to operate in the voltage limit mode, where the voltage is set to the peak value and the current will be variable below the maximum value to maintain voltage. These voltage and current limits are incorporated in the charging profile of the battery, which is stored in and controlled by the master controller.

The master controller would most likely be a controller that has a graphical user interface (GUI), such as Labview™. This would allow the user to configure the charging profile easily based on the battery being used. If this was built for a production operation, then a microcontroller could be used to control it with a preset battery charging profile or multiple battery charging profiles that could be chosen between.

The DIBPC is capable of operating in two different modes. The mode of operation is either the charging mode or the discharging mode, depending on the flow of energy to or from the battery. In the charging mode, the master controller will control the

DC/DC stage and set it to the correct voltage output. It will also ensure that the current in the AC/DC stage is not over the limit (this protection will also be redundantly provided in the AC/DC stage controller for faster operation). In the discharging mode, the master controller will ensure that the DC/DC stage is not operating the battery out of its state of charge limitation.

In the charging mode, the AC/DC stage is rectifying from AC to DC to constant DC voltage on the DC bus. The DC/DC stage is converting the constant DC bus voltage to the required battery DC voltage supplied from the master controller, as discussed later in this chapter. For a graphical explanation of the charging mode, see Figure 2.1.

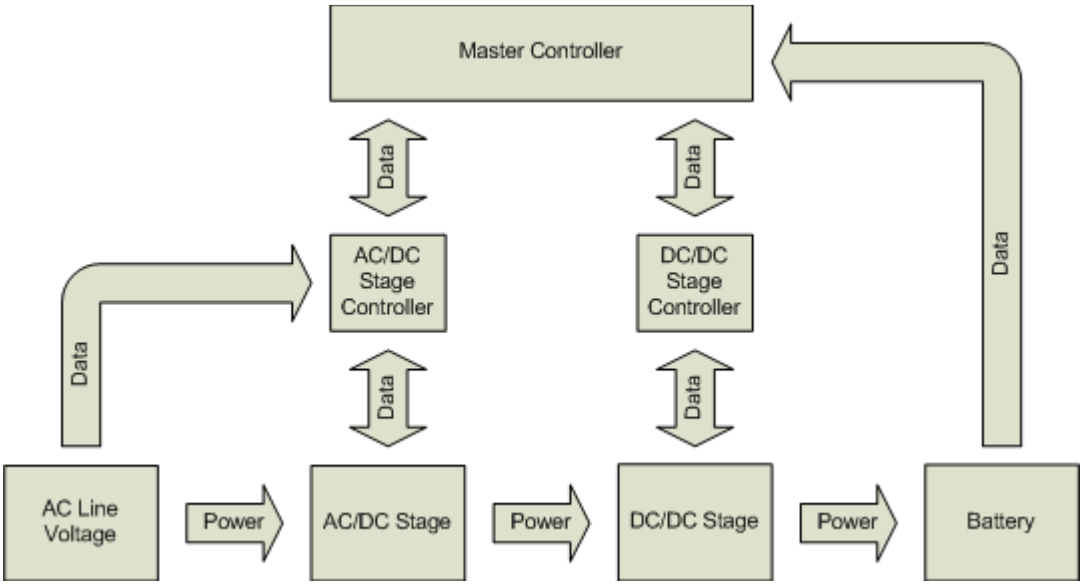

Figure 2.1: Charging Mode Block Diagram

In the discharging mode, the DC/DC stage of the DIBPC is outputting constant DC voltage to the DC bus. The input to the DC/DC stage is the varying DC battery

voltage. In the discharging mode, the AC/DC stage is inverting the DC bus voltage to AC line voltage. The discharging mode block diagram can be seen below in Figure 2.2.

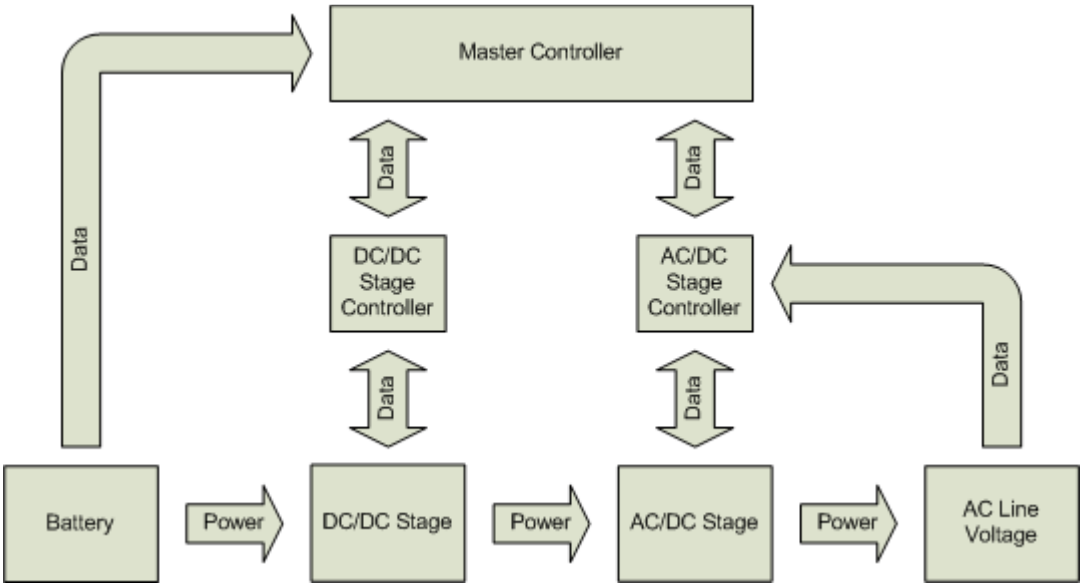

Figure 2.2: Discharging Mode Block Diagram

To make the DIBPC as flexible as possible, it is ideal to choose a DC bus voltage that is capable of charging many different types and styles of batteries. The battery with which the DIBPC is specifically designed to operate is a NiMH battery with a nominal voltage of 330 V_{DC}. Many other batteries operate in the same nominal voltage region. In the charging mode the AC/DC stage of the DIBPC is designed to have an output voltage of 400 V_{DC} to ensure the voltage remains high enough after the DC/DC stage to meet the maximum voltage limit for the battery. This voltage is chosen as a good median value which will allow lower voltage components to be used, yet still be capable of charging any battery with a required charging voltage up to about 380 V_{DC}.

The individual constraints of the charging mode are now considered. The system as a whole, including both stages, will have a variable DC output with a very low voltage ripple (ideally less than one volt) to nominally charge the battery. As discussed in the last chapter, the AC/DC stage has a large voltage ripple at a frequency equal to twice the line frequency. The DIBPC is designed to operate at 50 Hz or 60 Hz, so the ripple would be either 100 Hz or 120 Hz. The ripple magnitude is dependent upon the value of the filter capacitor, the input voltage and the load current. The DC/DC stage of the converter is designed to filter this ripple out, much like an active filter, while also providing a variable DC output voltage determined by the charging profile of the battery.

The second major constraint in the charging mode is the input current harmonic restrictions. In the US, there are currently no required limitations imposed on consumer device current harmonics, however, this may change in the future. There are international standards that do impose requirements on current harmonics and power factor which may eventually be applied in the US. Because products in the automotive industry such as this PHEV battery charger are usually designed and marketed for worldwide implementation, they generally meet the international standards everywhere they are implemented. Below, a couple of the most applicable standards are listed and described.

IEEE 519-1992 is an IEEE standard entitled "Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems." This standard is directed at utility distribution systems and distribution systems within industrial plants. Although this standard does not directly relate to consumer devices, it still provides some

insight into the expected limitations. IEEE 519, recommends limiting total voltage distortion to 3% of the fundamental and limiting total current distortion to 5% of the fundamental [7].

IEC 61000-3-4 (also the Euronorm (EN 61000-3-4) standard with the same number), entitled "Limitation of Emission of Harmonic Currents in Low-Voltage Power Supply Systems for Equipment with Rated Current Greater than 16 A," provides THD limitations for the input current [8]. This standard applies to the PHEV battery charger assuming the system is used within the jurisdiction of the IEC standards. The standards per harmonic are listed below in Table 2.1.

Harmonic Number n	**Admissible Harmonic Current $\%I_n/I_1$**	**Harmonic Number n**	**Admissible Harmonic Current $\%I_n/I_1$**
3	21.6	21	≤0.6
5	10.7	23	0.9
7	7.2	25	0.8
9	3.8	27	≤0.6
11	3.1	29	0.7
13	2	31	0.7
15	0.7	≥33	≤0.6
17	1.2		
19	1.1	Even	≤8/n or ≤ 0.6

Table 2.1: IEC 61000-3-4 Current Harmonic Limitations

Because IEEE Std 519 is directed at utility and industrial distribution systems which would typically require the use of a transformer (low pass filter) before their end use, the harmonic limitations are much more stringent than IEC 61000-3-4. For this

application, IEC 61000-3-4 provides more realistic current limitations; so for this charger, it is important for the harmonic limitations seen in IEC 61000-3-4 to be met.

One important variation that was considered for this design is the input voltage. In the US, two options are available, 120 V_{AC} or 240 V_{AC} at 60hz. Outside the US, varying voltages and frequencies are used, from 100 V_{AC} – 240 V_{AC} and 50 Hz – 60 Hz. To make the system as flexible as possible, it is designed to work from 120 V_{AC} – 240 V_{AC} and at either 50 Hz or 60 Hz. To maximize the rate at which the battery can be charged, the power of the DIBPC is limited only by the amount of current that can safely flow in typical residential wiring, and therefore by the circuit breaker size. A typical 120 V_{AC} breaker is 15 A and a typical 240 V_{AC} breaker that may be available in a residence is 30 A. Therefore the input power limitations for 120 V_{AC} and 240 V_{AC} are 1.8kW and 7.2kW, respectively.

In the discharging mode, there are several constraints that must also be considered in the design. Because of the safety issues discussed in Chapter One, the DIBPC is designed to only operate in the discharging mode when the main residential breaker is open. This will avoid any safety issues that arise from connecting to the utility grid. Because typical residential connections in the US have a center tapped 240 V_{AC} supply, inverting to both 120 V_{AC} lines relative to the neutral point would be required to emulate this connection and supply power to both residential circuits

To avoid this, the decision to only invert to 120 V_{AC} was made – however, the topology needs to be capable of outputting 240 V_{AC} with an available neutral if this is deemed necessary in the future. This decision makes the discharging mode and the

DC/DC converter much simpler. Because two 120 V_{AC} lines exist in a typical residential environment, they must both be powered individually. To do this, the DIBPC will supply the same 120 V_{AC} phasing to each line. This will result in a line to line voltage of zero between the two 120 V_{AC} and make all 240 V_{AC} appliances unable to operate. Therefore in the discharging mode, the DC bus voltage is set to 200 V_{DC}. This 200 V_{DC} voltage is converted from the battery voltage in the DC/DC stage. The AC/DC stage takes that 200 V_{DC} and then inverts it to produce 120 V_{AC}.

On the practical side of things, the design needs to be simple and cost-effective. This includes minimizing the component count, correctly sizing the components and requiring the minimal amount of system feedback for optimum operation. Simplifying the design minimizes opportunities for unexpected problems and component failures, increasing reliability. Simplifying the control will minimize the chances of software glitches and require less processing power.

Finally, the system needs to be efficient. Power losses in a battery charger would be analogous to gasoline being spilled while filling a tank. The efficiency of charging the battery therefore directly affects the amount of energy from the grid that is required per mile of driving, similar to a loss in the miles per gallon (mpg) of a combustion engine vehicle.

AC/DC Stage Design

The topology chosen for the AC/DC stage of the DIBPC design can be seen below in Figure 2.3. This topology was chosen for its simplicity, flexibility, and efficiency. The design meets all the design constraints, including the ability to effectively operate at 120 V_{AC} or 240 V_{AC} and to operate bidirectionally. This design can be implemented with the use of an IGBT 6-pack, which is typically used in three phase motor control applications. Because IGBT 6-packs with anti-parallel diodes are used so commonly in this configuration, these packs are readily available and cost-effective.

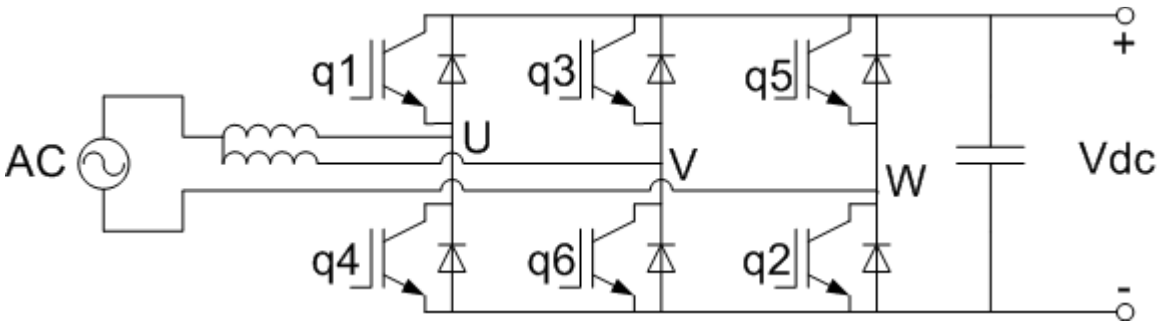

Figure 2.3: Dual Channel PFC Boost Rectifier and Inverter

The basic operation of this topology is relatively simple. It essentially consists of a diode rectifier intermingled with a DC – DC boost converter, much like the PFC rectifier described above. First, consider the charging mode. In the charging mode, either two or all three legs of the Rectifier will be modulated. When the input voltage is 120 V_{AC}, only the first leg, containing q1 and q4, and the third leg, containing q5 and q2,

are operated, leaving q3 and q6 gated off. However, when the input voltage is 240 V_{AC}, all three legs are operated. This third leg allows the addition of a second inductor to be used in conjunction with the first inductor. This allows more current to be used without increasing the current seen by each inductor. Inductor saturation, sizing and heat dissipation is a major concern, and this topology takes that into consideration.

Consider the case of the 120 V_{AC} input, knowing it can easily be extended to the 240 V_{AC} case. In this mode, q2 and q6 are modulated using pulse width modulation (PWM) generated with the aim of controlling the input current waveform and boosting the output voltage. When q2 and q4 (and q6 for 240 V_{AC}) are gated on, there is a path for the current to spool through the inductor, seen below in Figure 2.4. The path the current takes is bolded. The path that is unique to the positive half-cycle is shown bolded in red and the alternative path it takes during the negative half-cycle is shown bolded in blue. If the DIBPC was operating for 240 V_{AC}, q6 would perform the same function as q4, therefore using both inductors for spooling.

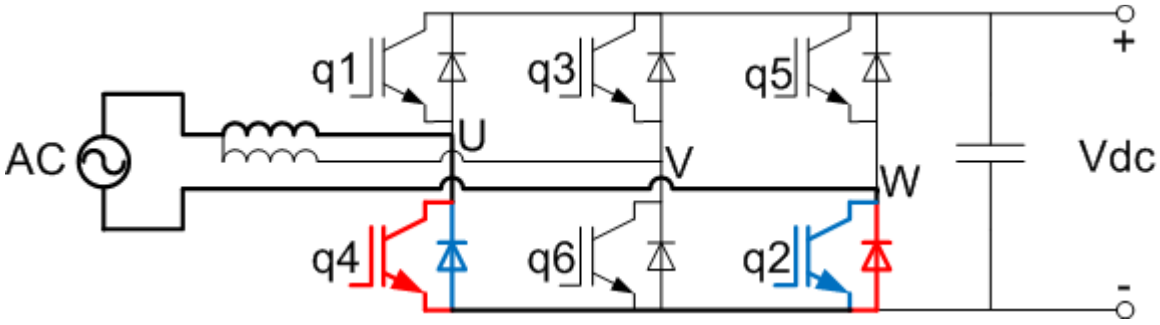

Figure 2.4: PFC Rectifier Spooling Paths

No distinction is made between the negative and positive half-cycles during the spooling mode. No distinction is necessary because both q2 and q6 can be operated together such that whichever half-cycle the input voltage is in, the spooling path will still be available. Once the current has spooled a sufficient amount (decided by the controller, described later in this chapter), q2 and q6 gated off, eliminating the path for the current to spool. Because the current in an inductor cannot change instantaneously, and the voltage across that inductor is proportional to the rate of change of the current through the inductor, the voltage of the inductor will rise enough to forward bias the anti-parallel diodes at q1 and q5 (and q3 in 240 V_{AC} mode) such that current can flow through the diodes and into the filter capacitor. This path can be seen below in Figure 2.5.

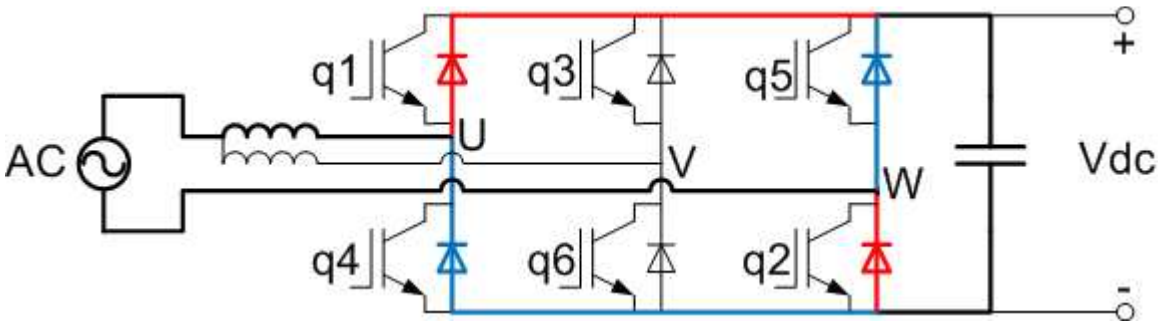

Figure 2.5: PFC Rectifier Current Path during Capacitor Charging

The discharging mode is operated much like a typical H-bridge inverter. Two possible discharging mode operations are discussed. First, a discussion of the potential operation versus the modified operation of the discharging mode is needed. In the potential operation of the discharging mode, the AC/DC stage would output two separate

120 V_{AC} sinusoidal voltages 180º apart. This would allow the discharging mode to output to each line in a typical US residence, powering any 120 V_{AC} and 240 V_{AC} circuits. First, this potential operation is discussed, and then the modified operation is discussed.

The potential operation of the DIBPC in discharging mode actually has two different states of operation per switching period during each half-cycle. Each switching period is broken into two parts where the first part is dedicated to modulating the first AC line and the second part is dedicated to modulating the second AC line. During the first half-cycle the first state of operation per switching period modulates q1 and q2 to produce a sinusoidal positive half-cycle in the first AC line, and the second state of operation modulates q5 and q6 to produce a sinusoidal negative half-cycle in the second AC line. During the second half-cycle, the first state of operation modulates q5 and q4 to produce a sinusoidal negative half-cycle in the first AC line and the second state of operation modulates q3 and q2 to produce a sinusoidal positive half-cycle in the second AC line.

Figure 2.6 is helpful in understanding the end result and the modes of operation for the potential operation. The red paths and waveform corresponds to the first AC line and the blue paths and waveform corresponds to the second AC line. One of the disadvantages of using this scheme is that the DC bus voltage must be equal to at least twice the maximum AC line to neutral voltage. This is because having two states of operation per switching period means that the maximum duty cycle for either AC line is 50% for a given switching period.

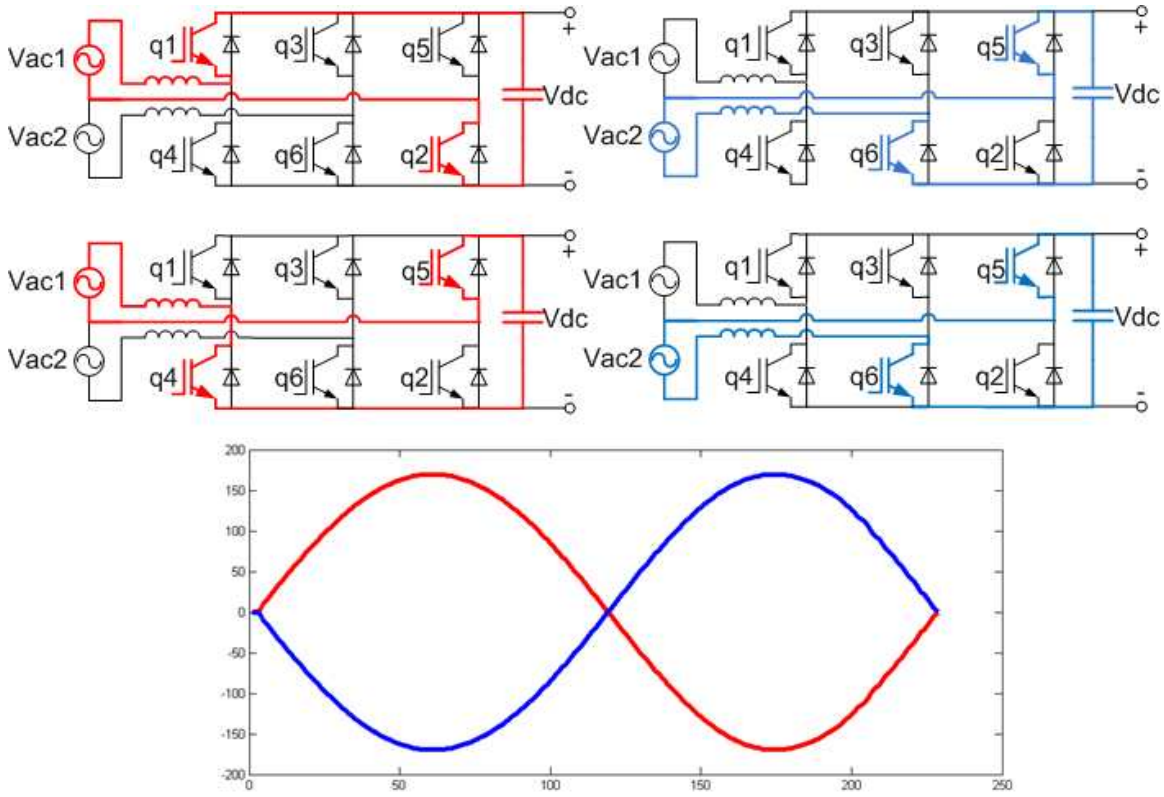

Figure 2.6: Discharging Mode Operation

The actual modified operation is a little different. This mode of operation was implemented as a simpler operation simply to demonstrate the ability of this topology to work in the discharging mode. In the modified operation, both the first and second AC lines output 120 V_{AC} with no phase shift between them. The result of this is that the line to line voltage is 0 V_{AC}, rather than 240 $V_{AC,}$ but both 120 V_{AC} circuits are powered. During this operation, only one state exists for each half-cycle switching period. In the positive half-cycle, q1, q2 and q6 are modulated to produce the sinusoidal positive half-cycle in both AC lines. In the negative half-cycle, q5, q3 and q4 are modulated to produce the sinusoidal negative half-cycle in both AC lines.

The simulated and experimental control methods and the derivation of the output to input voltage ratio and the duty cycle can be seen in the controls sections of Chapter Three and Chapter Five. One of the cons of this topology is the fact that the rated current for q1, q2, q3 and q4 is only half that of q5 and q6. The IGBT legs containing q1 and q4 and q3 and q6 both use the IGBT leg containing q5 and q2 as a return path. Because both IGBT legs use q5 and q2 as a return path, those IGBTs will have twice as much current as the remaining IGBTs. This is an issue considering typical IGBT 6-packs have identically rated IGBTs. However, the current rating required in each inductor is only half that it of what it would be if only two IGBT legs were present.

DC/DC Stage Design

The battery charger needs the addition of the DC/DC stage to successfully complete its operation. In the charging mode, the DC/DC stage is added at the end to buck the DC bus voltage down and to a variable voltage to charge the battery with the desired voltage. This DC/DC stage also operates as a buck converter in the discharging mode, decreasing the battery voltage to a steady 200 V_{DC}.

The DC/DC stage has two major functions in the charging mode. The first function is to provide a variable DC output which will be suitable for the needs of the battery following the charging profile. The second function is to eliminate the ripple voltage present at twice the line frequency. Because the ripple voltage is so low in frequency, it can easily be eliminated by a DC/DC stage.

The DC/DC stage is very simple, consisting of a typical implementation of a DC to DC buck converter. The DC to DC buck converter must operate bidirectionally, however. To achieve this, two IGBTs would need to be used, both with anti-parallel diodes. These are each in series with an inductor. Then another diode is placed between the negative and positive DC bus lines with the cathode at the positive side. The DC/DC stage begins with the DC bus capacitor at the left side. It ends with the battery connected to the DC capacitor at the right side. The topology can be seen below in Figure 2.7.

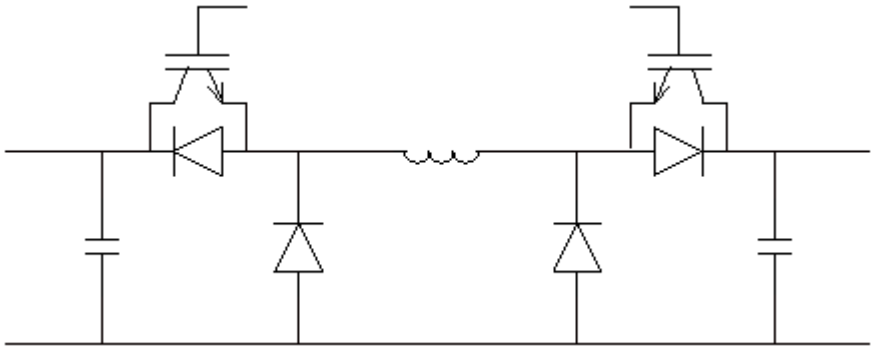

Figure 2.7: DC/DC Stage Topology

In either operating mode, the DC/DC stage can be treated like a normal DC to DC buck converter. In the charging mode, the right IGBT is inconsequential because the anti-parallel diode will always be forward biased and will provide the current path. The left IGBT is pulsed to provide a duty cycle which is proportional to the ratio of the output voltage to the input voltage. The relationship between the input and output voltage and duty cycle for a DC to DC buck converter in continuous conduction mode can be seen below in Equation 2.1 [9].

$$\frac{V_{out}}{V_{in}} = \frac{I_{in}}{I_{out}} = D \tag{2.1}$$

In the discharging mode, the left IGBT is not considered because its anti-parallel diode is forward biased. The right IGBT is pulsed in the same fashion as the charging mode to provide the desired constant DC bus voltage of 200 V_{DC}.

The DC/DC stage is designed, but it will not be implemented experimentally for the DIBPC. The DC/DC stage consists of two basic and commonly used DC to DC converters arranged such that one can act in either operating mode. Because DC to DC buck converters are used, the DC/DC stage's construction and control are somewhat trivial. The DC/DC stage is, however, simulated. This will be discussed in the next chapter on simulation.

Component Sizing and Rating

To optimize the DIBPC AC/DC stage design, the components need to be ideally sized. To do this, several pieces of information must be known. First, the maximum size of the load must be determined. The limiting factor for this design has been the typical size of a residential 240 V_{AC} circuit breaker, 30 A_{AC}. Therefore it can be assumed that the maximum input current must be 30 A – this also sets the limit for the output current. The next piece of information that must be known is the switching frequency, which has been designated at 20 kHz due to IGBT switching frequency limitations and to minimize

the number of switches that occur, and therefore the switching losses. The desired DC link voltage is also needed to determine the relationship between the input current and the output current, this is set to 400 V_{DC}. The final piece of information that is required is the maximum acceptable ripple current and ripple voltage.

The worst case scenario must be considered for sizing each component. First, the capacitor must be sized. The worst case scenario for the capacitor would be the 30 A_{AC}, 240 V_{AC} case, with an efficiency of 100%. This produces a maximum amount of current which will deplete the charge on the capacitor, creating a ripple voltage. Because the second stage of the converter will be a DC to DC converter which will filter the ripple voltage present at twice the line frequency, the ripple tolerance is quite high. As much as a 40 $V_{p\text{-}p}$ ripple is an acceptable amount that could easily be filtered by the second stage of the converter. Because DC capacitors have limitations on voltage ripple and current, 40 $V_{p\text{-}p}$ ripple limitation is chosen. Because the ripple voltage at twice the line frequency will be so much greater than the ripple voltage at the switching frequency, only the lower frequency ripple voltage is considered for capacitor sizing. Equation 2.2 shows the derivation of the desired capacitance.

$$P_{dc} = P_{ac} * \eta = I_{ac} * V_{ac} * 1.00$$

$$I_{cap} = I_{dc} = \frac{P_{dc}}{V_{dc}} = 18A$$

$$I_{cap} = C * \frac{dV_{cap}}{dt} \tag{2.2}$$

$$C = \frac{I_{cap}}{\frac{dV_{cap}}{dt}} = \frac{18A}{\frac{40V}{8.3333ms}} = 3750\mu F$$

The inductor value for a given inductor ripple current is not quite as easily calculated. The ripple current is only a function of the switching frequency, there is no relevant ripple voltage at twice the line frequency because the fundamental inductor current is AC, oscillating at the line frequency. The derivation of the inductor ripple current for a DC to DC boost converter can be seen in [10].

This inductor current ripple calculation can be applied to a PFC boost rectifier by assuming the line frequency is so much lower than the switching frequency that it can be viewed as a DC voltage in the reference timeframe. This line frequency voltage can then be converted similarly to a DC to DC boost converter. To assume a worst case scenario, the source voltage, V_s that produces a maximum ripple current is used. To limit electromagnetic interference (EMI), minimize THD and maximize the PF and the efficiency, the inductor current ripple is limited to $3A_{p\text{-}p}$. This value is selected by optimizing efficiency (balancing filter losses with harmonic losses).

IEC 61000-3-4 limits any harmonic greater than the 33rd to .6% of the fundamental, or about $500mA_{p\text{-}p}$ at maximum load. To meet this limit for the switching frequency (333rd harmonic), an AC line filter must be installed with an attenuation of at least 8 dB at the switching frequency of 20 kHz. [10] gives the derivation for the inductor ripple current and the relationship between the duty cycle, k, and the input and output voltages, seen in Equations 2.3 and 2.4.

$$k = \frac{V_{dc} - V_s}{V_{dc}} \tag{2.3}$$

$$\Delta I = \frac{V_s * k}{f * L} = \frac{V_s * \frac{V_{dc} - V_s}{V_{dc}}}{f * L} \tag{2.4}$$

$$\Delta I_{\max}: \ \frac{\mathrm{d}\Delta I}{\mathrm{dV_s}} = 0 = \frac{\mathrm{V_{dc} - 2V_s}}{\mathrm{f * L * V_{dc}}} \Rightarrow \mathrm{V_s} = \frac{\mathrm{V_{dc}}}{2}$$

$$\Delta I = \frac{\frac{V_{dc}}{2} * \frac{V_{dc} - \frac{V_{dc}}{2}}{V_{dc}}}{f * L}$$

$$L = 1.414mH$$

The other components do not have to be sized, only rated for their operation. The IGBTs and diodes in the neutral path (q5 and q2), need to be rated for 30 A_{RMS} and 400 V_{DC} continuous. The IGBTs and diodes in the other two legs need only be rated for 15A_{RMS} and 400 V_{DC}. However, because the duty cycle of this device could potentially be so high during charging and because inductive load switching could occur in discharging mode, a generous safety margin has been incorporated. The filter capacitor needs to be rated for at least 450 V_{DC} – this will include any maximum ripple or charging overshoot that may be present. The inductors need to be rated for at least 15 A_{RMS}. However, a safety margin should be incorporated here as well.

Summary

The DIBPC design is broken down to better separate the functions of each individual stage. Once the design was chosen, simulations were constructed. These simulations, detailed in the next chapter, were used during the design process to concrete some of the details of the design. Once the simulations were completed, the experimental process began. In the experimental implementation, the master controller was not constructed. The overall design focuses primarily on the AC/DC stage of the DIBPC, because the DC/DC stage consists of a common design with very little changes. The DIBPC AC/DC design takes into consideration the design of the DC/DC stage, ideally minimizing its complexity and cost.

CHAPTER THREE

SIMULATION

To better understand and design the PHEV battery charger, some simulations were constructed. The simulation process was employed to test different designs and to examine the effects changes have on the system. Simulations were also useful to explore and troubleshoot the hardware during the construction and experimentation phases.

Simulation Design

Two software programs were utilized for simulation purposes. The first software used was PSCAD™. PSCAD is a graphical based program designed for modeling and simulating power systems. PSCAD is mainly aimed at the utility industry for steady state and transient studies, including fault analyses, transient and harmonic effects and load flows. The second software employed was Matlab™. Matlab is a mathematical program designed to be flexible and applicable to almost any mathematical problem. Matlab has a graphical modeling and simulation interface called Simulink™.

Simulink comes equipped for typical mathematical systems, and capable of expansion through the use of toolboxes. Toolboxes for Simulink incorporate new blocks that can be used for a specific function. One of these toolboxes is the Simulink Power Systems Toolbox. This toolbox contains many useful blocks for this application,

including various transistors, diodes, multimeters, motor drives and controllers, passive elements, etc.

Basic models were constructed in each of these software packages. After initial simulations and some simple analyses were completed, it was decided to move forward using only Matlab/Simulink. Simulink has a more user friendly interface, but more importantly, it has more useful existing blocks. Simulink comes well equipped for many control problems, making it much more flexible than PSCAD for designing a controller. This was the major deciding factor in choosing between PSCAD and Simulink.

The Simulink Power Systems Toolbox operates in a somewhat unique manner from typical Simulink applications. The Power Systems Toolbox contains the PowerGUI interface which operates as a layer between the Matlab solver and the Simulink models. The PowerGUI layer discretizes the model system. This is done to improve performance of the simulation, and so that the model will converge in a realistic amount of time. PowerGUI also allows for many different analyses to be performed that are unique to Power Systems, including frequency sweeps, load flows, FFTs and steady state versus transient values.

One of the considerations that must be taken into account is solver step size. This determines how many iterations are calculated. Knowing the switching frequency would be around 20 kHz – 25 kHz, a step size of 1 μs was chosen. This step size allowed for plenty of resolution for the duty cycle. Tests were done at 10 μs steps, but the simulations contained a large ripple that was not present at 1 μs step size. Another important factor is the length of the simulation. The simulation must be long enough to

get past all the transient behavior so that only the steady state behavior is evident. This is typically not an issue, and a simulation run time of 250 ms was adequate. The only problematic situation is when the state of charge of the battery needs to be changed. To get an appreciable change in the state of charge, it would take thousands of seconds, much too long to run a simulation. Therefore some interpolation must be used.

One area of difficulty which often arises in simulation is how to model the load. In this case, the system was modeled and simulated in three different modes, including: the charging mode, the discharging mode and the charging mode with the DC/DC stage. Therefore several different load models had to be used. For the first mode, the charging mode, the load model was simply a resistive load. This was used to ensure that the basic operation of the AC/DC stage was effective when converting to a constant DC voltage. When considering how the AC/DC converter should operate, it was thought that it would be desirable to operate the system with a constant DC current. This was modeled with a simple ideal current source model. After some testing and comparison, however, it was determined that the constant DC current load and a simple resistive load had nearly identical results. Because the constant DC current load took significantly longer to solve in simulation time, the resistor was used.

The second mode of operation was the discharging mode. This mode required the use of a source on the AC side of the converter. When in this mode, the voltage source was modeled with a simple DC voltage source to emulate the output from the DC/DC stage that is fed from the battery. The load on the AC side was modeled as a resistor and

also as a resistive an inductive load. These should provide for some variation in loads that one might expect to see in a typical residential application.

When the DC/DC stage was added in, two loads were modeled. The first modeled load was also a resistor. This provided a simple way to determine if the overall system would act as expected when subjected to a constant impedance load. The second load model, though, was a NiMH battery model. This is a generic battery model contained within the Simulink™ Power Systems Toolbox.

The battery model allows certain parameters to be changed for the battery. These parameters include the DC voltage rating, the energy rating in amp-hours, the initial state of charge, the internal resistance and the discharge characteristics. Because the characteristics of the battery are not known at this time, the default values for a NiMH battery with a voltage rating of 330 V_{DC} and about 15 A-hrs were used. Unfortunately, due to computing restrictions, the simulation could not be run for a long enough period of time to accurately show what was happening as a result of the charge being applied. Because of this limitation, the battery essentially always looked and acted like a constant DC voltage source, creating essentially meaningless results. For this reason, only the resistive load results were considered.

Design Topology Model

The simulation is broken down into two major parts. The first part, discussed in this section, is the system model. The second part is the control structure. This is

discussed later in this chapter. The simulation model is organized using several subsystems. The operation of the simulation model will be discussed by subsystem.

The simulation implementation is broken into three subsystem layers. The inner most layer contains the component makeup of the IGBT 6-pack with anti-parallel diodes. This can be seen below in Figure 3.1. The inputs and outputs for this block are the same as you would expect from an IGBT 6-pack, one connection for each of the IGBT legs between the upper and lower IGBTs (A, B and C), a negative DC connection and a positive DC connection. The control connections consist of one gate connection for each IGBT.

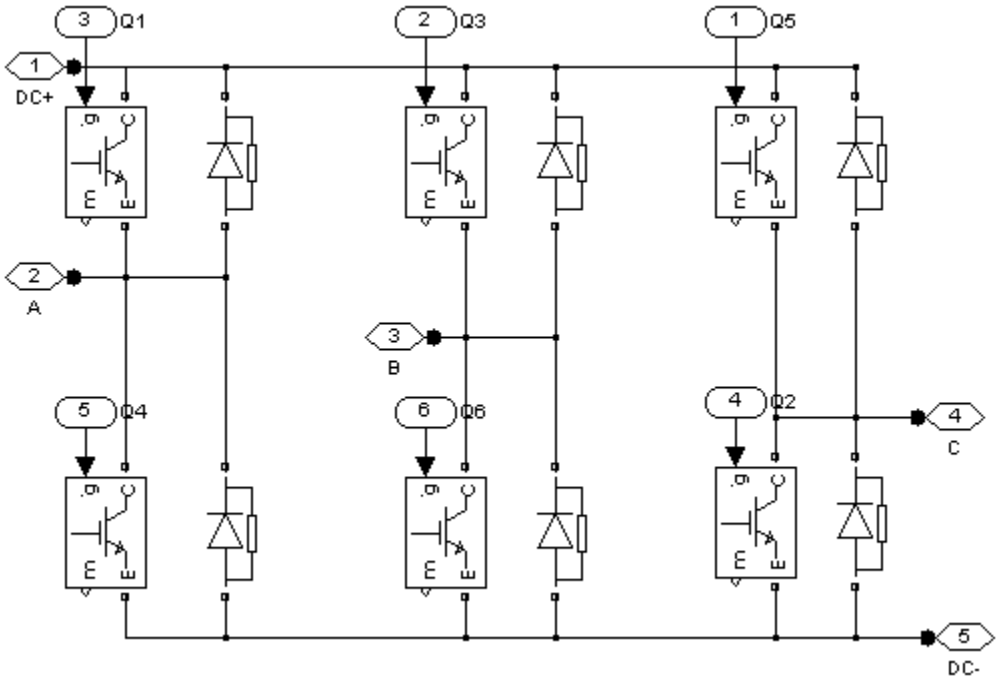

Figure 3.1: IGBT 6-pack Model

The middle layer of the controller consists of the external electronic components such as inductors, capacitors and filters, along with measurement blocks and ideal switches. This layer can be seen below in Figure 3.2. The two spooling inductors can be seen leading into the IGBT 6-pack subsystem. The capacitor with its modeled equivalent series resistance (ESR) is connected to the output from the IGBT 6-pack subsystem. The AC line filter, consisting of an AC capacitor and a series inductor can be seen on the left. Finally, four ideal switches are used to make any connection changes for use in all modes of operation. The connections from this layer go directly to the AC and DC input and output (load and source).

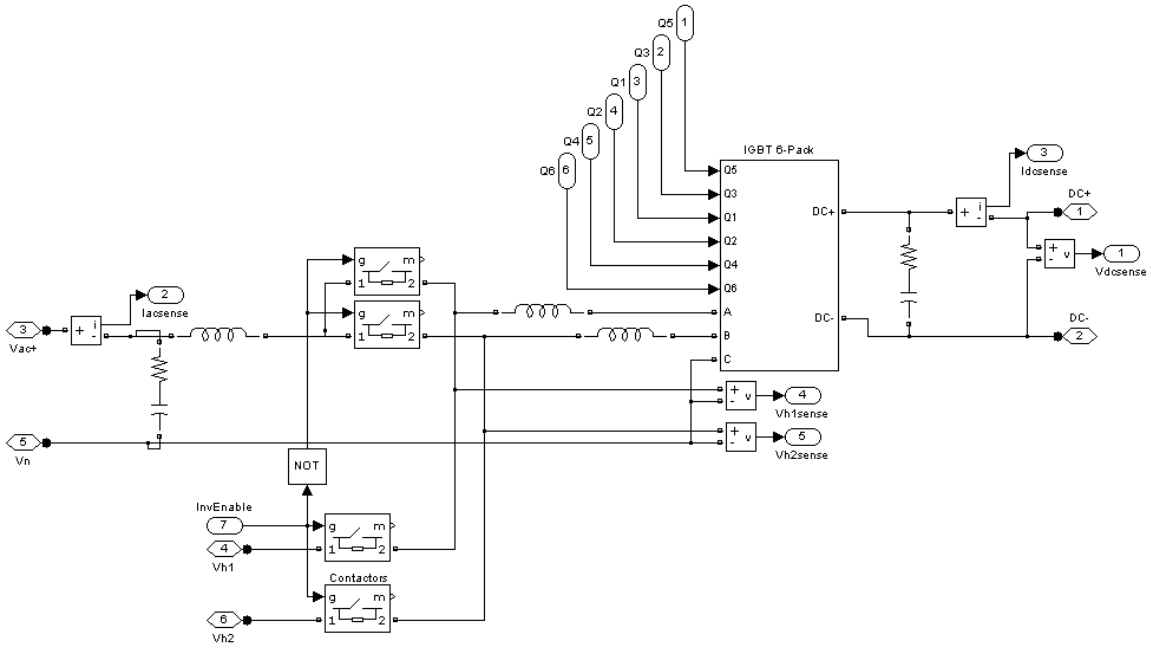

Figure 3.2: Electrical Circuit Model

Finally, the last layer of the simulation model is the outer layer containing the source and the load. This layer will vary depending whether the simulation is in the charging mode or the discharging mode. The charging mode will have a voltage source on the AC side and a load on the DC side. Conversely in the discharging mode this layer will have a voltage source connected on the DC side and a load connected on the AC side. In the charging mode, the model can be seen below in Figure 3.3 and the discharging mode model can be seen below in Figure 3.4.

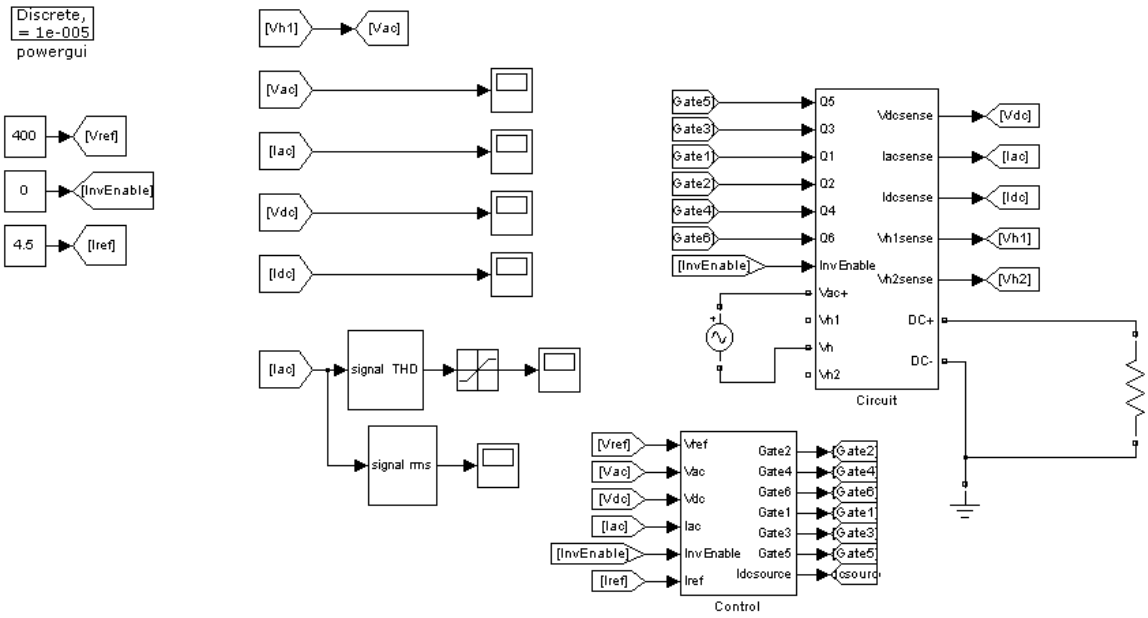

Figure 3.3: Charging Mode Model

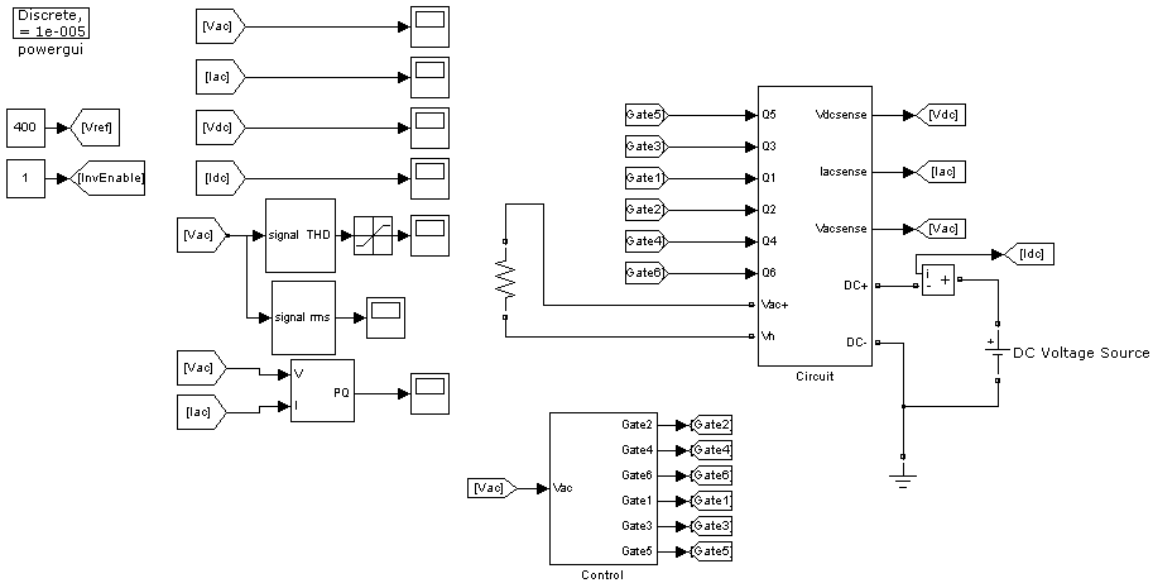

Figure 3.4: Discharging Mode Model

In the outside layer is where the measurements are plotted and calculations such as THD, RMS, and power are made. The control subsystem can be seen, and the measurements needed to make that operate are ported into the subsystem. Likewise the resulting control outputs for each gate are ported out of the subsystem and into the electrical circuit model subsystem. To properly emulate the control, only the measurements that would be absolutely necessary to the controller will be fed back into the controller. Enough measurements are taken otherwise to provide adequate feedback about the operation, efficiency, and effectiveness of the simulated converter.

Simulations do not require a significant amount of ancillary equipment. The IGBTs that are used in the model do not have completely realistic gate inputs. Because they are simplified gate inputs, a logic level input is all that is required. Because of this, no gate drivers are needed to gate the IGBTs. Likewise, switches can be implemented at

the logic level, eliminating the need to simulate transistor or optoisolators switches. Simulations do not require isolating equipment for measurements or avoiding ground loops, further reducing the need for ancillary equipment.

Simulation Controls

The simulation must control the gate pulses in both the charging and discharging modes of operation. It must distinguish between the modes and provide the correct signals to the IGBT gate inputs. To operate the IGBTs in such a way as to produce the desired effects, two control schemes were considered for the charging mode. The first control scheme is the PFC sinusoidal pulse width modulation (SPWM) current control scheme and the second control scheme is the PFC hysteresis control scheme. For the discharging mode, a typical SPWM inverter PI voltage control scheme was used. Each of these is discussed in detail in this section.

The PFC SPWM control scheme is a commonly used PWM technique used to generate gating pulses with duty cycles corresponding to a desired magnitude by comparing a reference waveform to a carrier waveform. The second control technique explored is the hysteresis current control. Hysteresis current control is not as common, although it is another way to achieve a desired duty cycle, using lower and upper bounds to determine the on/off periods of the IGBTs. For the discharging mode, a basic sine table was constructed and is referenced for the generation of the voltage waveform. A

Proportional Integral (PI) controller is then used to provide manage the feedback and track the desired magnitude.

The charging mode of the DIBPC must be operated under a current control scheme. The controller must track two reference signals. The first controlled state is the output DC voltage. This is accomplished by having a PI controller using the feedback from the DC measurement and creating an error signal from the reference value. This error signal is then fed into the PI portion of the controller. The PI controller works by breaking the error signal into two parts. The first part, the proportional part, is multiplied by some constant, determining the amount the error should proportionally affect the output of the controller. The second part is the integral term. The integral term takes the error signal and integrates it with respect to time then multiplies that value by a constant to determine how much the integral of the error affects the output of the controller. The proportional and integral components are then summed together and output.

The proportional term of the PI controller is designed to provide an increase in the output signal which is directly proportional to the distance between the reference signal and the measured signal. This can be a positive or negative value. This term is then added to the integral term. The integral term provides a long term effect to the system which is the accumulation of the errors. Each error is accumulated and added to the output. As the measured signal increases due to the increased output from the integral term, the amount the integral term contributes from each new error measurement is decreased. Once the measured signal increases above the reference signal, the integral term begins to decrement, while still remaining positive. This generally results in some

overshoot and eventually some oscillation. The idea of the integral term is that it will eventually settle around some constant value which leaves the error signal oscillating closely about zero.

This PI controller is used in both the SPWM and the Hysteresis controllers to force the DC voltage to the reference value. The output from the PI controller which drives the DC voltage error to zero is then fed into the second part of the controller, the current waveform controller.

The SPWM current control technique uses a PI controller to drive the current waveform to a desired value. This desired value is constructed in such a way as to create a power factor near one and a magnitude such that the DC voltage tracks the reference value. The SPWM current control technique first creates a desired AC current waveform. This waveform is constructed by taking the measured AC voltage waveform (for the wave shape) and multiplying it by the output from the DC voltage PI controller and then by some constant (to provide normalization).

The current measurement is subtracted from the desired current, creating an error signal. This error signal is put through another PI controller to generate the desired duty cycle. This duty cycle (normalized between zero and one) is compared to a sawtooth waveform with the desired switching frequency. When the duty cycle value is greater than the sawtooth waveform, the IGBTs are gated on. When the duty cycle is less, the IGBTs are gated off. This creates an effective duty cycle with a constant switching frequency to the IGBTs. This control can be seen below in Figure 3.5.

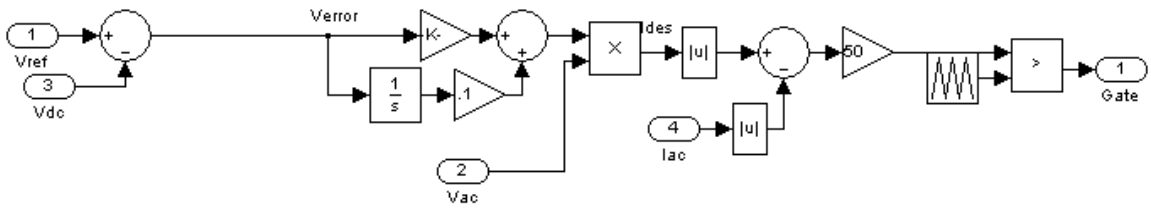

Figure 3.5: SPWM Current Control Block Diagram

The second controller that was tested was the hysteresis controller. The hysteresis controller uses the same PI controller for the DC voltage control. The output from this is then fed into the hysteresis portion of the control. It is multiplied by a constant and by the AC voltage waveform (all normalized) to create the desired AC current. The AC voltage is subtracted from this desired AC current, creating an error signal. The positive and negative hysteresis bands are placed equidistantly above and below the zero value of the error signal.

As the error signal moves around those bounds, the controller compares the error signal to the hysteresis bounds at each time step. When the error signal moves below the hysteresis band, the IGBTs are gated off. As the error increases, it moves within the hysteresis band. No change to the gating state occurs until the error increases above the hysteresis band, however. The IGBTs are then gated on. As the error decreases and eventually falls below the hysteresis bands, the IGBTs will gate off again. This cycle continues to repeat itself, forcing the error to oscillate around the zero point, nearly within those hysteresis bands. The range of the hysteresis band determines the switching frequency and the magnitude of the oscillation about the zero point. The block diagram of the hysteresis controller can be seen below in Figure3.6.

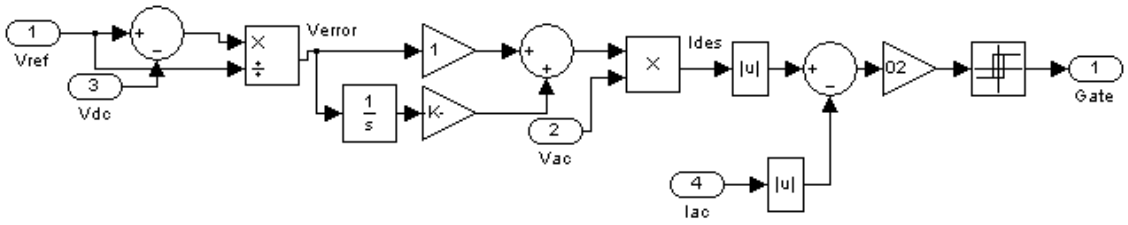

Figure 3.6: Hysteresis Current Control Block Diagram

The hysteresis control is all handled with one block in Simulink. The last block before the signal is output in Figure 3.6 is called a relay block. According to Matlab, the relay block's function is as follows. To "Output the specified 'on' or 'off' value by comparing the input to the specified thresholds. The on/off state of the relay is not affected by input between the upper and lower limits [11]." This block allows the error signal to be input to the block. It creates a hysteresis band about the positive and negative value selected as the threshold, and then reacts as described above.

Either of these controllers can be used to provide the gating signal. This gating needs to be directed to the correct IGBT gate, however. This is done by using some simple logic operations in simulation. A distinction must be made between whether the DIBPC is operating in the 120 V_{AC} mode or the 240 V_{AC} mode. In the 120 V_{AC} mode of operation, gates q2 and q4 are operated. Both of these gates can be operated with the same gating signal. The explanation of which IGBT must be gated during the positive and which during the negative can be seen in the topology section of the design of the dual input bidirectional power converter chapter. Figure 3.7 shows the simulation logic that is used to determine the gate operation.

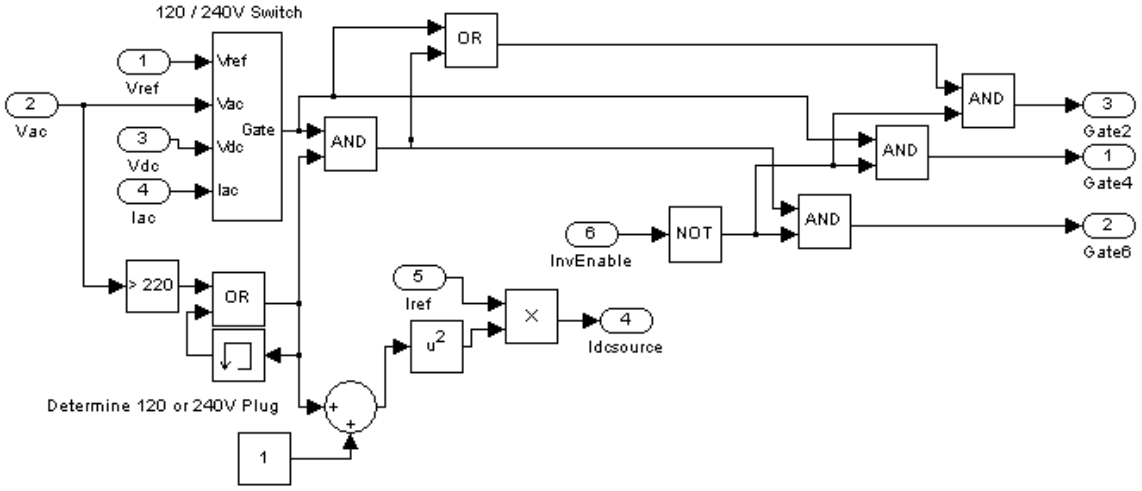

Figure 3.7: Gate Selection Logic

All of the gates operate with the same gating signal. This is accomplished by realizing that only the upper diodes will operate to release the spooled current and that only the lower portion of the 6-pack pertaining to the negative half-cycle of the signal will operate (i.e., an IGBT gating when the anti-parallel diode is forward biased will not affect the operation). There is no harm in operating the IGBTs that are required for the negative half-cycle during the positive half-cycle and vice versa. Therefore, there is no need to determine whether the waveform is in the positive or negative half-cycle, a rectified AC waveform is sufficient.

During the simulation process, the PI gain constants had to be tuned. The DC voltage PI controller could be tuned separately from the AC current controller. The DC voltage PI controller could be tuned using basic PI tuning techniques. The output from the controller had a linear response on the system. As the output increased, it linearly

increased the magnitude of the desired current. The magnitude of the desired current directly affected the magnitude of the actual current, which in turn had a direct and linear affect on the magnitude of the DC voltage. Because of this linear relationship, tuning the DC voltage controller was quite simple. Proportional gain was first increased to provide a constant output without too much oscillation. Then integral gain was increased until the DC voltage output reached the set point sufficiently fast without too much overshoot.

Next, the current controller had to be tuned. The SPWM current controller contains a PI loop which must be tuned and the hysteresis current controller contains a hysteresis band which must be tuned. The SPWM current controller has a PI loop with a nonlinear response to the system. The output from the SPWM current controller directly corresponds to a duty cycle. This duty cycle can then be treated as the duty cycle of a boost converter with a slowly varying DC input voltage. The relationship between the input and output voltage and the duty cycle can be seen below in Equation 3.1 [9].

$$\frac{V_{out}}{V_{in}} = \frac{I_{in}}{I_{out}} = \frac{1}{(1-D)} \tag{3.1}$$

Because the duty cycle of a boost converter corresponds to the ratio of the input to the output voltage, the effect the duty cycle has on the system changes depending on the instantaneous AC input voltage. This nonlinear affect on the system makes tuning the PI controller very difficult.

When tuning the SPWM current control PI controller, a very large amount of proportional gain was required to reduce the zero crossing distortion. When the input AC

voltage waveform approaches zero, the ratio of input to output voltage must be very high to increase the inductor voltage high enough to create any current flow. Although only a small amount of current is needed near the zero crossing, the ratio of the input voltage to the output voltage has not changed linearly with the amount of current needed. To compensate for this fact, additional proportional response is needed to increase the response near the zero crossing. The end result is a very large proportional gain.

Because of the nonlinear system response, the integral gain is not helpful. The integral term sums the errors regardless of what point in the waveform it occurs, providing a linear response, when a nonlinear response is needed. For this reason, the integral gain is set to zero.

The hysteresis controller is tuned by increasing the magnitude of the hysteresis bands away from the zero point. The hysteresis band had to be increased until the switching frequency was below 20 kHz. Once this constraint is achieved, the hysteresis band is ideally set. Increasing the hysteresis bands further will result in a larger error oscillation about the desired current.

Both of the PFC control schemes produce the desired results, and have advantages and disadvantages associated with them. The experimental implementation most closely follows the PFC SPWM current control scheme. This was chosen primarily due to the constant switching frequency, but also due to simplicity in implementation. This is discussed in greater detail in Chapter Four.

The inverter uses a SPWM inverter PI voltage control scheme that is commonly used for this purpose. The inverter must be controlled to output a sinusoidal voltage with

a preset frequency. Because this is designed to operate for a typical residential application, the US line frequency standard of 60 Hz was chosen. To invert the DC to AC, a reference waveform must be created. Creating a reference waveform in simulation is quite simple, because a sinusoidal reference block exists that relies directly on simulation time. This reference block is chosen to have a 60 Hz, $120V_{RMS}$ sinusoidal wave shape.

Once the reference signal is created, it is input to a PI loop. The output voltage is measured and subtracted from the reference waveform, and the error signal is used to create the PI output signal. This output signal is then treated much the same as the reference current signal in the SPWM current controller. It is normalized and compared to a sawtooth waveform, creating pulses which are used to gate the IGBTs. The control scheme can be seen below in Figure 3.8.

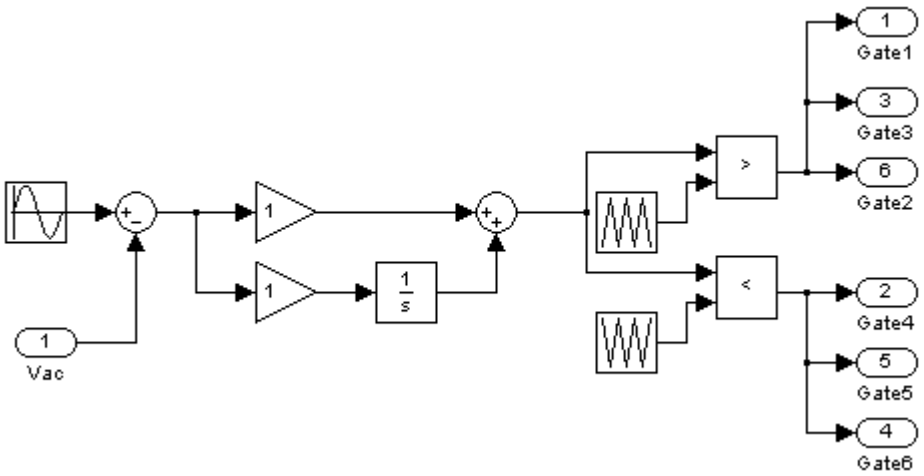

Figure 3.8: Inverter Control Block Diagram

Once the gating signal is created, it must be sent to the correct IGBTs along with a line frequency gate that corresponds to either the positive or negative half-cycles of the desired voltage output. Knowing that the simulation is going to essentially do things consistently and ideally, each of the IGBTs is switched using the gating signal, rather than one IGBT left on and the other operated at the switching frequency.

The simulation chooses which IGBTs to operate based on some simple logic and comparators. The sawtooth waveform is inverted to operate the other half-cycle inversely from the first. The simulation control blocks which direct the gating signal to the correct IGBTs can be seen above in the right hand side of Figure 3.8. Tuning the PI controller for the inverter results was very simple, following the same procedure described above for the PFC SPWM DC voltage control PI loop.

Finally, the simulation needs to distinguish between whether the converter is operating in the inverter mode or the PFC mode. This also is done with simple logic. Figure 3.7, above, has an INVenable input. The INVenable variable is set to a Boolean one in discharging mode and a Boolean zero in charging mode. This variable is operated with a logical AND for all IGBT gates so that they will not operate from the inverter controller when the DIBPC is operating in the charging mode. Likewise, the IGBTs used in the charging mode (the bottom three IGBTs) are operated inversely from INVenable with a logical AND so that they will not operate in the discharging mode.

DC/DC Stage Simulation

The DC/DC stage is constructed in simulation to determine what effect it will have on the AC/DC stage of the DIBPC. The DC/DC stage was connected to the output DC bus capacitor. In the charging mode, the DC bus capacitor voltage is constantly 400 V_{DC}. This voltage is bucked to 330 V_{DC} for this simulation, using the nominal battery voltage. The output from the DC/DC stage is a resistor. The DC/DC stage model can be seen below in Figure 3.9.

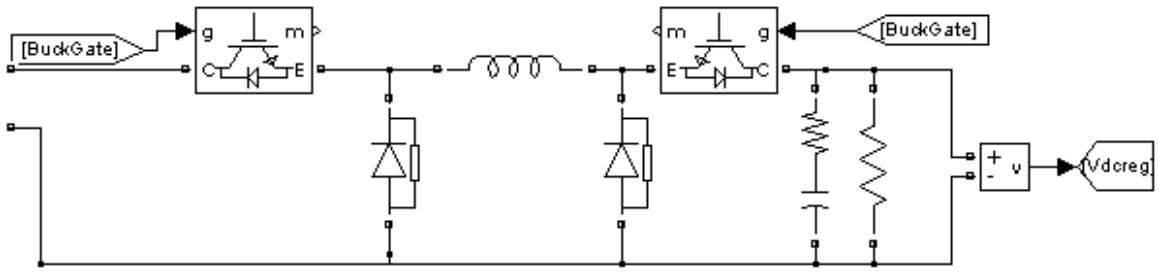

Figure 3.9: DC/DC Stage Model

In the charging mode, the left IGBT is pulsed to provide a duty cycle which is proportional to the ratio of the output voltage to the input voltage. The relationship between the input and output voltage and duty cycle for a DC to DC buck converter in continuous conduction mode can be seen below in Equation 3.2 [9].

$$\frac{V_{out}}{V_{in}} = \frac{I_{in}}{I_{out}} = D \tag{3.2}$$

The DC to DC buck converter is controlled using two control schemes. First, the DC/DC stage uses a voltage controlled PI loop with SPWM to emulate the battery operating in voltage limit mode. Next, the DC/DC stage is controlled with a current controlled PI loop with SPWM to emulate the battery operating in current limit mode. Both control schemes are used to see how the DIBPC will operate in the current control and voltage control regions.

The DC/DC stage operating in the voltage control mode consists of a basic PI voltage control loop. The PI loop uses feedback of the DC bus output voltage to generate an error signal from the reference voltage value, which could be an input from an outside controller. The PI loop uses the error signal to generate a desired duty cycle to operate the buck converter IGBT. This duty cycle is then compared to a sawtooth waveform with the desired switching frequency to generate the pulses to gate the IGBT. The block diagram for the control system can be seen below in Figure 3.10.

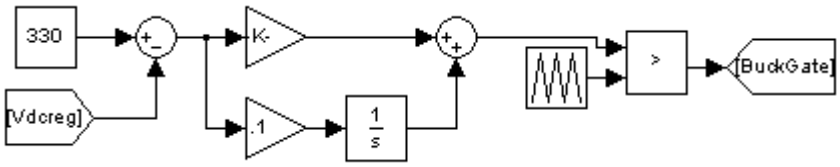

Figure 3.10: DC/DC Stage Voltage Control Block Diagram

The Vdcreg reference input for the regulated DC voltage value could be an input from an outside controller. This outside controller would determine the DC bus voltage

value based on the charging profile for the battery. The DC/DC stage could then provide the slowly varying DC bus voltage with a very low ripple voltage, efficiently charging the battery using its ideal profile while in the voltage control region.

The DC/DC stage operating in the current control mode uses the same control scheme. The only difference is that now the error signal for the PI controller is generated using a current limit. In practice, the input for this current limit would be from the master controller. For the purpose of the simulation, however, a constant value is chosen to ensure the DIBPC delivers maximum power. The block diagram for the current control scheme can be seen below in Figure 3.11.

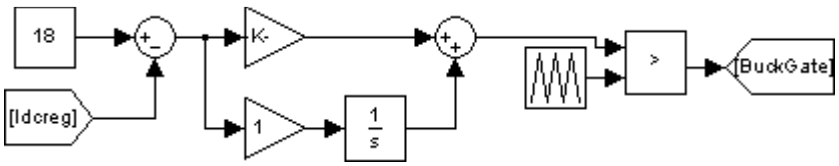

Figure 3.11: DC/DC Stage Current Control Block Diagram

Summary

The simulations constructed during the design and testing of the DIBPC were discussed in detail in this chapter. Several simulations had to be run to ensure the DIBPC topology would operate as expected in each mode. Simulations were also run to test the DIBPC under different control schemes and to see how the AC/DC stage of the DIBPC would operate with the DC/DC stage of the DIBPC. Each function of the simulation was broken down and explained, along with the basic control schemes. The next chapter will

discuss the experimental hardware setup of the AC/DC stage of the DIBPC, because the DC/DC stage was simulated but not constructed.

CHAPTER FOUR

EXPERIMENTAL HARDWARE SETUP

The experimental setup was constructed with a few practical constraints. The first constraint was the equipment available. To minimize costs, some components that were already available were used along with other components that were donated. Because of this fact, some hardware limitations were in place where a better, more efficient, newer or more practical component may have otherwise been chosen. This section is broken down into five major parts. The first four sections are descriptions of the critical and support equipment implemented along with the measurement devices and fault protection, and the last section is an explanation of issues that arose during the testing phase, diagnoses and resulting actions taken.

Critical Equipment

The first major piece of critical equipment is the IGBT 6-pack. The IGBT 6-pack selected was already available and being used in a three phase motor controller. The 6-pack is a Mitsubishi Intelligent Power Module PM75CVA120. This pack, shown below in Figure 4.1, consists of 6 IGBTs with anti-parallel diodes arranged in a three phase bridge [12]. Five line connections exist in the pack, one for each of the three IGBT legs connecting to the emitter of each positive IGBT and to the collector of each negative IGBT. The pack also provides connections for the negative and positive DC terminals.

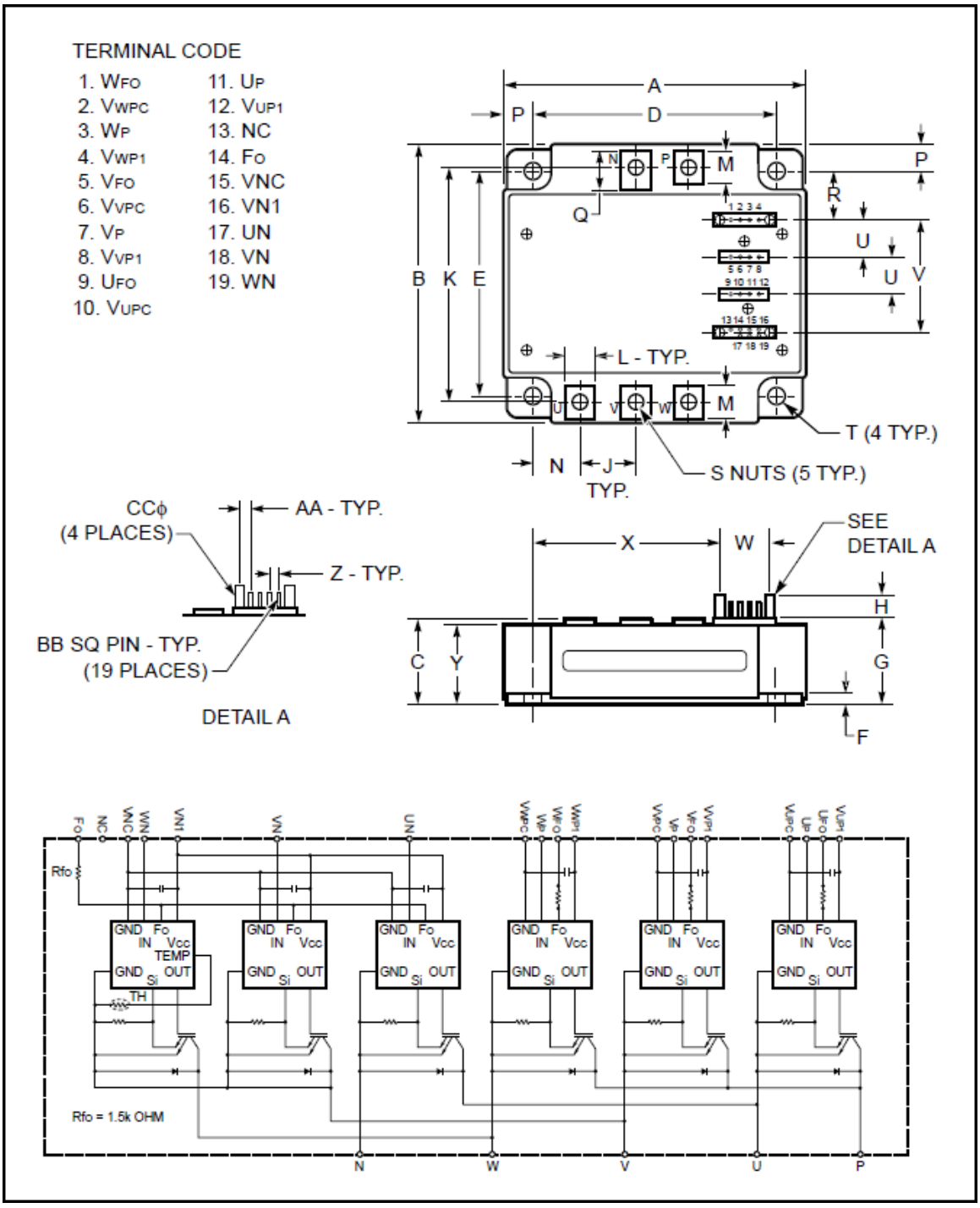

Figure 4.1: Mitsubishi® Intelligent Power Module PM75CVA120 [12]

The PM75CVA120 is rated for 75 A_{RMS} current and 1200 V_{DC} voltage and is limited to a 20 kHz operating frequency, a limiting factor in the design of the system. Because this device is designed to operate with such large currents and voltages, a significant amount of heat is generated. This heat is dissipated through the use of a heat sink that is affixed directly to the top of the heat sink, providing maximum heat transfer from the pack to the heat sink.

The 6-pack also contains built in control circuits which provide optimum gate drive. The control circuitry reduces the need for external gate drivers, but does not eliminate the need. The control circuitry requires an external power supply of 15 V_{DC} to be applied. Each of the positive IGBTs, Up, Vp and Wp, require an isolated 15 V_{DC} input to be supplied. Also, all of the IGBTs on the negative half, Un, Vn and Wn, require a single isolated 15 V_{DC} input to supply all of them collectively.

The isolated supplies are required because each IGBT gate must have a voltage applied relative to its emitter. Up, Vp and Wp each have unique emitter connection points while Un, Vn and Wn all have their emitters tied together at the N terminal. The IGBTs are individually gated by applying 15 V_{DC}, relative to each individually isolated power supply, to the respective gate. This gate drive signal is generated from individual gate drivers which were constructed for this circuit and are described later in this chapter.

This IGBT 6-pack provides integrated fault and thermal protection. The fault protection overrides the gate inputs and automatically gates all IGBTs off in the case of a shoot through fault (both IGBTs in one leg gating on together). This helps protect the IGBTs and the free-wheeling diodes from overcurrent from short circuiting the positive

and negative DC busses through the IGBT 6-pack. The trip level is set at 105 A and should operate in 10μs. The thermal protection is used to trip the system in the event of an over temperature condition from overuse or poor heat dissipation. The thermal protection is set to trip ideally at 110ºC.

Another 6-pack was also used during the operation of the converter. This 6-pack, donated from Powerex®, Inc., is a very similar pack to the Mitsubishi PM75CVA120. In fact, the only differences between the packs are the ratings, the efficiency and the layout. This Powerex® pack, the Powerex® Intellimod™ PM50CLA060, is rated for 50 A_{RMS} and 600 V_{DC}. The layout for this can be seen below in Figure 4.2 [13]. This pack was only used for a limited amount of time due to its destruction, documented later in this chapter.

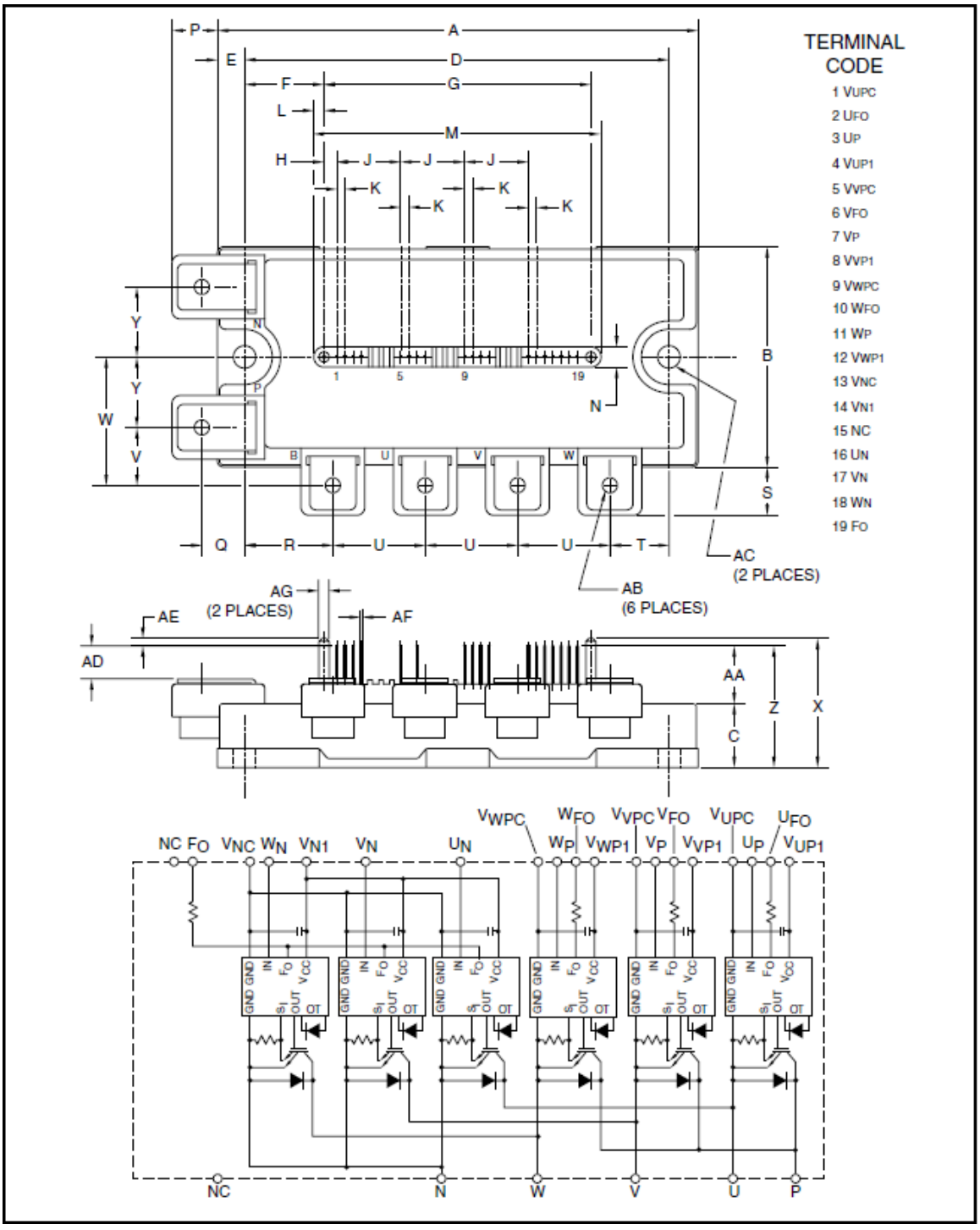

Figure 4.2: Powerex® Intellimod™ PM50CLA060 [13]

The next critical pieces of equipment used are the inductors and capacitors. The capacitors were DC capacitors that were available for use. Two 2400 μF, 450 V_{DC} capacitors that were also previously in a motor drive application were selected for the DC bus capacitor. These capacitors, when placed in parallel, give 4800 μF of capacitance, exceeding the desired capacitance for the design constraints.

The inductors have several constraints which make their selection a little more difficult. The inductors need to be able to withstand 15 A_{RMS} of current continuously without saturating or overheating. Therefore inductor cores with very high flux densities were chosen. Also, because of the high inductance needed, about 1.4 mH, many turns will be necessary. After looking at many various cores and completed inductor assemblies, it was determined that attaining the cores and winding them would be more cost-effective for this application.

Magnetics® Inc. sells various cores designed to withstand high flux densities. The core chosen for this application is the Mag-Inc.® 58868 high flux powder core, which Mag-Inc. donated. Mag-Inc provides a core selection application guide which is used to determine which product minimally meets the requirements, based on the desired DC current bias and inductance. The DC current bias refers to the line frequency current flowing through the current. For this application, 15 A, minimally, is selected.

The cores are selected by the power handling capability, LI^2. For this application, LI^2 , is about 315 mH-A^2. The selection charts recommend the 58868 core, with a relative permeability of 26. Then, from looking at the data sheets for the 58868 core, the number of windings to achieve the desired inductance can be found. The core is rated for

30 nH / turns^2. Therefore about 147 turns are required to achieve the desired inductance. Because so many turns are required on such a small core, a small gauge wire was required to allow for winding.

Because the current will be over its rated value for a typical wire of this gauge, 18 gauge high temperature wire was selected. These wires were wound around the cores in three layers. Once this was complete, the inductors were then measured. It was determined that both inductors have approximately 1.35mH of inductance. From the data sheets, it was determined that each of the inductors also contains about 200 mΩ of resistance. Measuring, however, suggests that the resistance is likely between 300 mΩ and 400 mΩ, possibly due to bad connections in the terminal blocks. This resistance would result in a quality factor between 1.25 and 1.75 at 60 Hz.

The last primary piece of equipment is the microcontroller. The microcontroller selection was based on the anticipated data acquisition requirements along with the various operating modules needed. Microchip Technologies Inc. is the developer of the PIC® line of microcontrollers selected for the task. In order to use one microcontroller to perform all the operations of the AC/DC stage of the DIBPC in both charging and discharging modes, the microcontroller would need sufficient analog to digital inputs, along with PWM outputs and digital inputs and outputs.

In the charging and discharging modes, the microcontroller needs three analog inputs, one each for AC current, AC voltage and DC voltage measurements. Along with those three inputs, a fourth input is desirable. The fourth input would be from the master

controller, containing a desired DC voltage reference value. While this is not implemented at this time, it is important for future flexibility.

The microcontroller also needs two digital inputs. These inputs are to determine if the microcontroller is operating in the charging or discharging mode of operation and in the 120 V_{AC} or 240 V_{AC} modes of operation. For future flexibility, it is important to have sufficient digital and PWM outputs. For this reason, three PWM outputs with unique time bases are needed for each leg of the IGBT 6-pack. Several digital outputs are needed for various auxiliary functions and for gating some IGBTs in the discharging mode (throughout one half-cycle). A total of five digital outputs are needed. Three digital outputs are needed for the IGBT half-cycle outputs, one to drive digital switches for charging and discharging mode distinction and one to limit startup current.

The microcontroller chosen to meet all of the requirements is the Microchip dsPIC30F2020 digital signal controller. This is a 28-pin 16-bit microcontroller that operates at 20 MIPs. The dsPIC30F2020's important features include: 21 digital I/O pins, eight 10-bit analog inputs, 8 PWM channels and 2 output compare channels. The dsPIC30F2020 is designed for applications such as motor controllers, power converters, uninterruptible power supplies, power factor correcting rectifiers and inverters.

Support Equipment

Because the IGBT 6-pack had some gate drive circuitry, but did not have true gate drivers included, some gate drivers had to be constructed. IGBTs require a voltage to be

applied to the gate of the IGBT relative to the emitter. A positive voltage applied will bias the internal junctions in such a way as to allow current to flow from the collector to the emitter. When a negative voltage is applied, the internal junctions will be biased in such a way as to prevent current from flowing from the collector to the emitter. When the negative voltage is applied, however, the reverse breakdown voltage is very low. Because of this fact, integrated anti-parallel diodes are used to prevent the voltage from the emitter to the collector to exceed the reverse breakdown voltage.

In order to properly bias the internal junctions, the voltage applied to the gate must be relative to the emitter. The voltage must be either positive or negative. The internal circuitry in the IGBT 6-pack simplifies this operation. Once the internal circuitry is powered with a 15 V_{DC} supply (relative to the emitter), zero volts applied to the gating input of the circuitry gates the IGBT on and 15 V_{DC} applied to the gating input gates the IGBT off. This means the gate drivers must be constructed so that the input is low-active.

In order to provide isolated gating inputs for each of the positive IGBTs individually and an isolated gating input for the negative IGBTs, two transformers with two 120 V_{AC} / 18 V_{AC} windings each were used, because four total gate driver circuits are needed. Gate driver assemblies are available for this IGBT 6-pack, but the decision was make to construct gate drivers due to the cost of the assemblies. A constant 120 V_{AC} source is used to supply the power for these transformers. Each of the transformers secondary sides are left floating for now. The output is put through a full bridge rectifier with a DC filter capacitor. This DC voltage is then input to a 15 V_{DC} voltage regulator.

This 15 V_{DC} voltage regulator is used to provide the isolated 15 V_{DC} power to the IGBT circuitry.

Because each of these IGBTs is controlled from the same controller, they need isolation for the digital logic. The microcontroller used to logically gate the IGBTs will provide digital outputs for each gate relative to the same reference voltage. To provide the isolation needed, optoisolators designed specifically for use as gate drivers were selected. These optoisolators are the J312. The input side of the J312 contains a LED used to optically gate a MOSFET when the diode is forward biased.

The digital output from the microcontroller is used to forward bias the diode. Because the IGBTs are low-active, the digital output from the microcontroller is compared to the +5 V_{DC} output from the microcontroller. Thus a digital low output from the microcontroller will result in the diode being forward biased. A 390 Ω resistor is used in series to limit the forward current through the diode.

When the internal diode is forward biased, the internal MOSFET will be gated on. This will switch the output from the J312 and provide a 15 V_{DC} input to the gating signal on the IGBTs. Therefore a low output from the microcontroller results in the IGBT being gated off and a high output from the microcontroller results in the IGBT being gated on. A complete diagram of the gate drivers can be seen below in Figure 4.3. The input 120 V_{AC} source to the transformers is supplied from a constant external source that can be switched on or off. The output from each gate driver is input directly into the IGBT 6-pack.

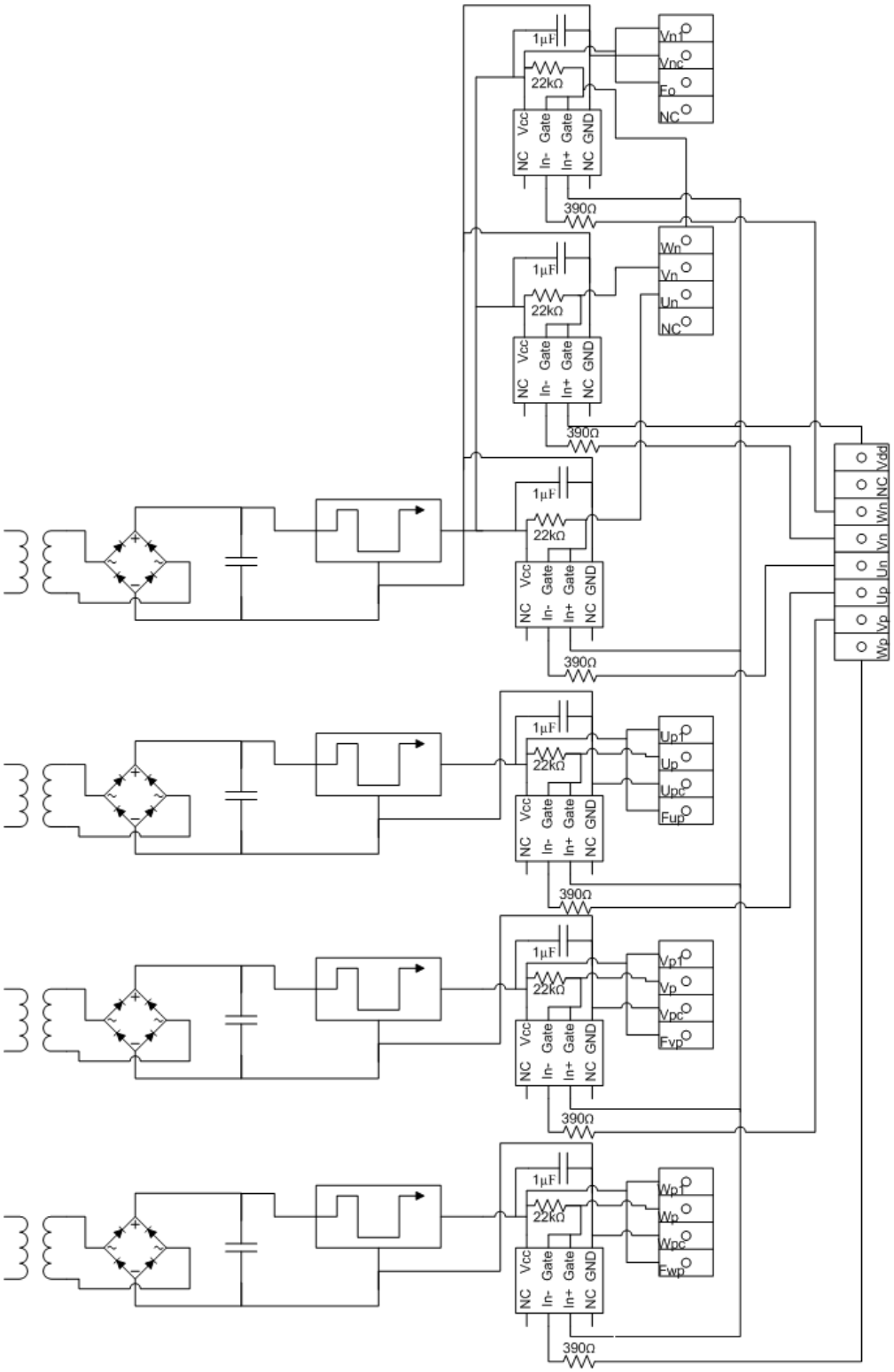

Figure 4.3: Gate Driver Circuit Diagram

In order for the microcontroller to be able to perform the correct functions, it must know which mode of operation is desired. The microcontroller has three modes of operation, 120 V_{AC} charging, 240 V_{AC} charging and discharging. There are two toggle switches on the converter. One is used to determine 120 V_{AC} or 240 V_{AC} operating mode and the other is used to distinguish between the charging and discharging modes.

In order for the microcontroller to be able to receive digital inputs corresponding to the state of the toggle switches, a small resistive circuit had to be built. This circuit was recommended by Microchip for the purpose of digital switching. The circuit consists of a basic resistive divider connected between the +5 V_{DC} power supply and the digital input as can be seen in Figure 4.4.

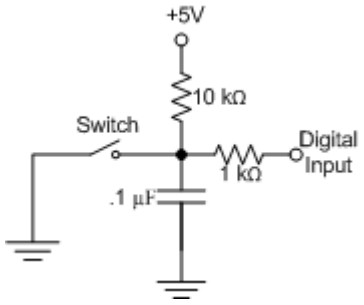

Figure 4.4: Digital Switching Circuit Diagram

When the toggle switch is closed, the digital input will be connected through a 1 kΩ resistor to ground, bringing the digital input low. When the toggle switch is opened, the digital input is connected through the 10 kΩ and the 1 kΩ resistors in series to the +5

V_{DC}, bringing the digital input high. This switching circuit is used for the charging / discharging mode switch and the 120 V_{AC} and 240 V_{AC} switches.

Depending on which mode the DIBPC is operating in, different microcontroller pins operate the gate drivers. In the charging mode, the OC1 and OC2 pins from the microcontroller are used to operate the lower IGBT gates, q4, q6 and q2. In the discharging mode, RE0, RE2, PWM1H and PWM2H are used to operate all six IGBT gates. In order to ensure the correct gate driver is connected to the correct microcontroller output, three optoisolators are used as switches. The input to the optoisolators is a digital output, RE7, from the microcontroller: digital high represents discharging mode and digital low represents charging mode.

The optoisolators each contain two channels. They are configured such that one channel is operating when the input is high and the other channel is operating when the input is low. Each optocoupler pair is used to switch the output to the gate drivers from one microcontroller output to another. The optoisolators switch the bottom three IGBT gates from OCx outputs in charging mode to PWMx or REx outputs in discharging mode. The optocouplers switching circuit can be seen below in Figure 4.5.

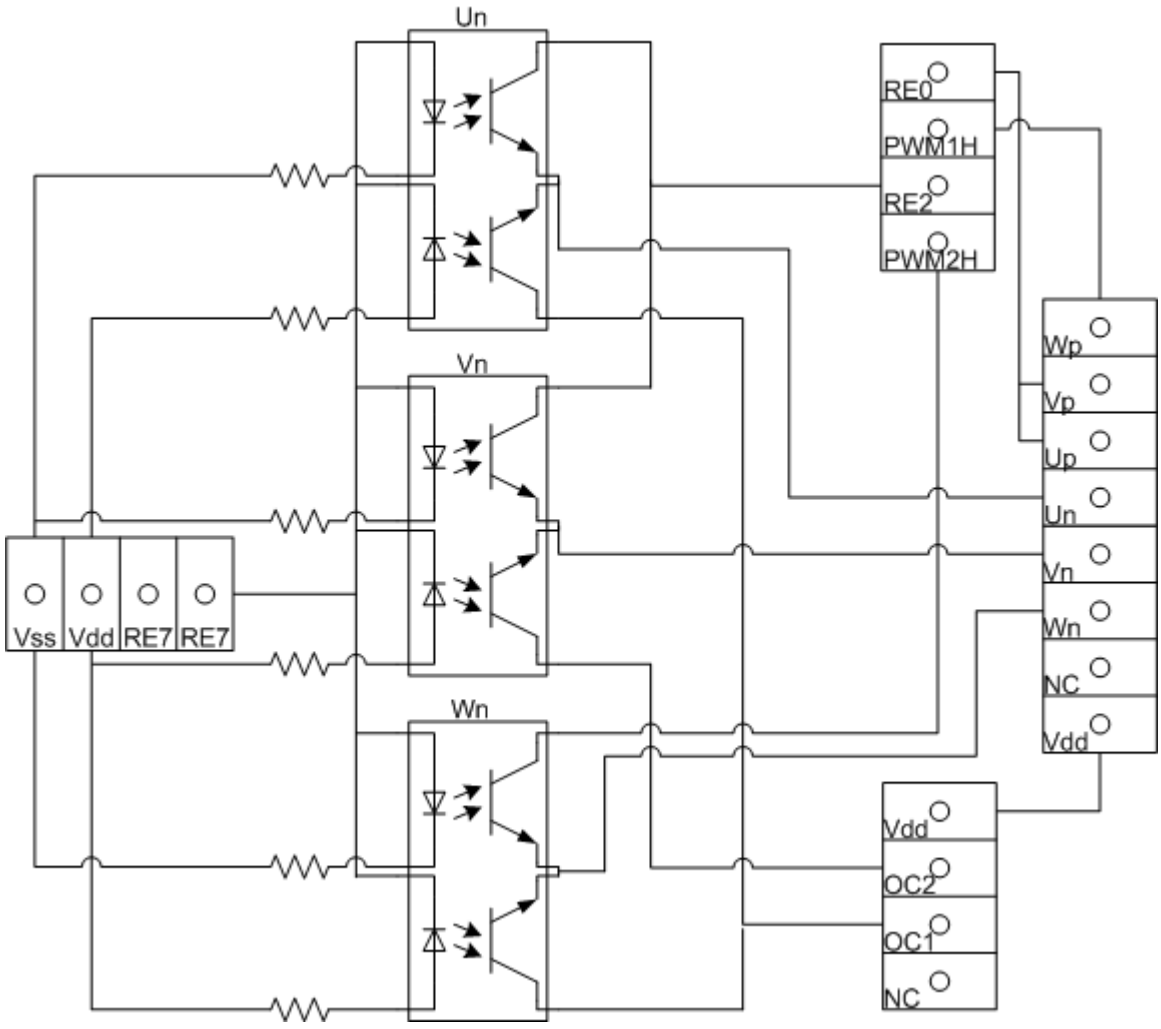

Figure 4.5: Optocoupler Gate Switching Circuit Diagram

In order to provide power for the microcontroller and the support equipment, a power supply circuit was constructed. This circuit uses 120 V_{AC} power as the source. A transformer with two 120 V_{AC} / 8 V_{AC} windings was used. The primary side used the same 120 V_{AC} source for both windings and the secondary windings were connected in series, providing a 16 V_{AC} output. This output was rectified, filtered with a DC capacitor and then connected to a 15 V_{DC} regulator. From this regulator, a 15 V_{DC} power supply

was available (used by the DC voltage measurement device discussed in the next section). Also from this 15 V_{DC} regulator, a 5 V_{DC} regulator was connected to provide a 5 V_{DC} power supply to the microcontroller and some other peripherals. This circuit can be seen below in Figure 4.6.

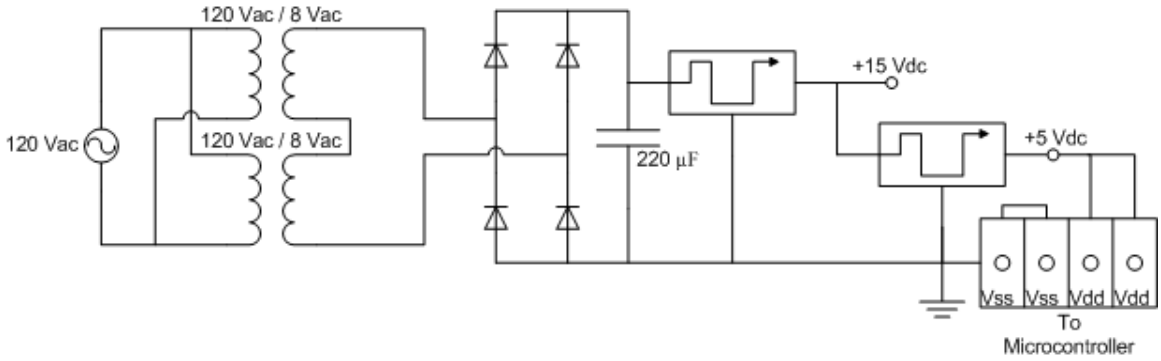

Figure 4.6: Power Supply Circuit Diagram

During the early construction phase of the DIBPC, a development board was used to aid in the development of the microcontroller program. The development board allowed easy programming and debugging of the microcontroller while supplying power and providing an interface to connect digital and analog inputs and outputs. Once the program gained stability, however, the microcontroller was moved to a circuit board. This move to a circuit board reduced the length of connections from the microcontroller to peripherals and eliminated the dependence on the development board and its connection to the PC. The development board was still used for programming, but during operation, the microcontroller was placed on the circuit board.

To operate the microcontroller independently, a 5 V_{DC} power supply must be connected to each V_{DD} pin and its reference connected to each V_{SS} pin. The $\overline{MCLR}$ pin must be connected to V_{DD} during operation, and can be pulsed with V_{SS} for a reset. Each analog device requires an analog V_{SS} (AV_{SS}) and analog V_{DD} (AV_{DD}) connection. AV_{SS} is connected to V_{SS} with a 10 Ω resistor and AV_{DD} is connected to V_{DD} with a 10 Ω resistor. Along with the 10 Ω resistors, a 10 µF capacitor is placed between AV_{SS} and AV_{DD}. The analog power supply is thus filtered to mitigate the effect digital noise has on the analog signals. These connections along with the connections the microcontroller has to each analog and digital device are shown in Figure 4.7.

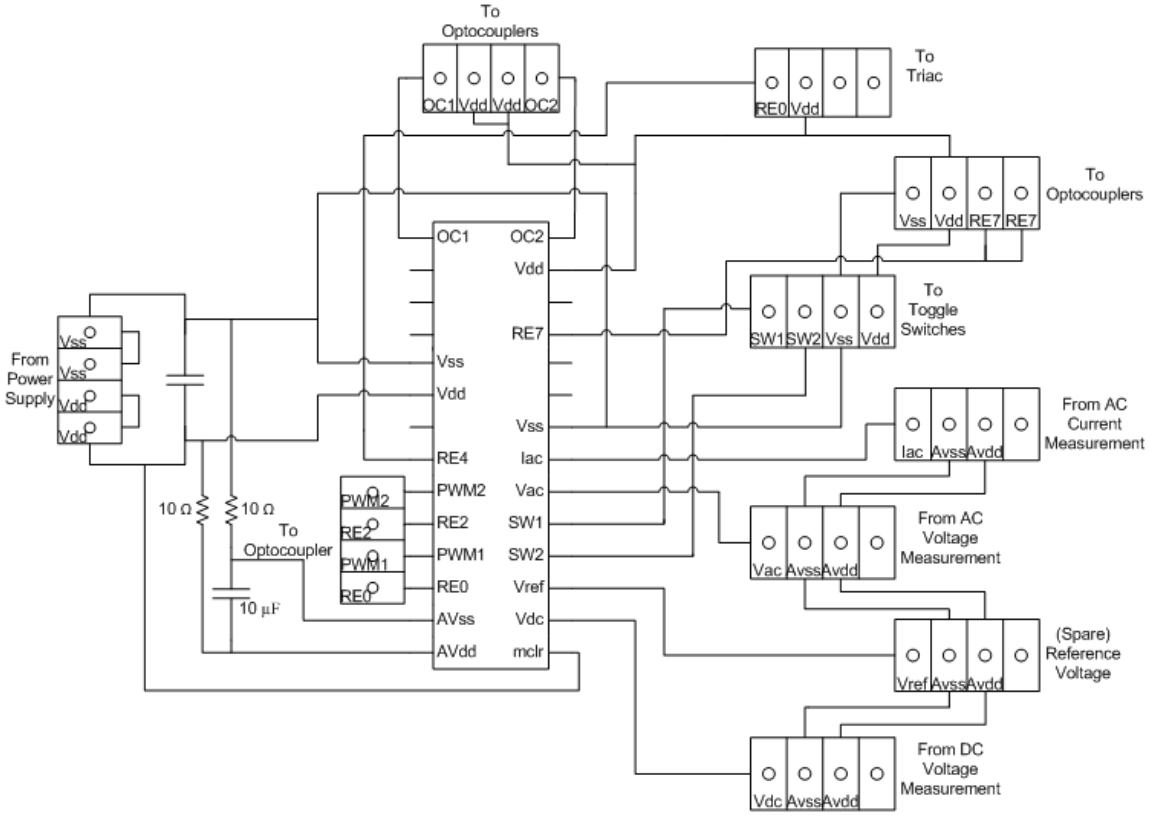

Figure 4.7: Microcontroller Board Layout

In order to reduce the high frequency current harmonics from the DIBPC, an input AC line filter was installed. This filter consists of a 1 mH series inductor and a 3μF shunt capacitor. The cutoff frequency is found from Equation 4.1 and the line frequency leakage current is found from Equation 4.2.

$$\frac{1}{\sqrt{2}} = \pm\left|\frac{Z_C}{Z_C + Z_L}\right| \therefore\ f_c = 4515\ Hz \tag{4.1}$$

$$I_L = \left|\frac{V_{AC}}{Z_C}\right| = 271\ mA\ (240\ V_{AC}), 136\ mA\ (120\ V_{AC}) \tag{4.2}$$

Because the cutoff frequency is 4515 Hz, the filter will be effective in reducing the high frequency current ripple that is present at 20 kHz. At 20 kHz, the filter would offer an attenuation of 16.7dB. This easily meets the requirements for higher order harmonics, including the harmonics from the inductor current ripple.

Other than measurement circuits, the last piece of supporting hardware is a triac used to limit current from capacitor charging during startup. This addition was an afterthought that became apparent after a startup current transient caused some hardware damage. A detailed breakdown of this failure can be seen later in this chapter. To effectively limit the current during startup, a triac was used to modulate the phase angle, slowly increasing the duty cycle of the AC input voltage waveform. This allowed only a limited amount of current to flow into the capacitor during each cycle.

The triac used for this is a Crydom® HD4850-10 solid state relay. The HD4850-10 is rated for 480 V_{AC}, 50 A_{AC} continuous with a 3 – 32 V_{DC} input. The 3 – 32 V_{DC} input has a typical input current of 2 mA, which is limited by internal circuitry in the HD4850-10. The HD4850-10 can turn on at any point in the waveform and has a turn-on time of 20μs [14]. To simplify the connection from the microcontroller to the triac, the digital channel used to gate the triac on is referenced against the V_{DD} pin, which is +5 V_{DC}. This means the digital output results in a low-active condition for the triac.

Feedback / Measurement Hardware

The controller requires the use of feedback for three circuit parameters, the AC voltage, the AC current and the DC voltage. In order to measure each of these, a small measurement circuit was constructed. These same measurements are used for both the charging and discharging modes, and the DC voltage measurement would be used by both the AC/DC and DC/DC stages of the DIBPC. The circuits used to perform each of these measurements and supply the isolated and scaled results to the microcontroller are discussed below.

The AC voltage measurement circuit consists of an isolation transformer and a voltage divider. The transformer is used to provide isolation to the circuit and to scale the voltage down. The circuit also needs to rectify the signal because the microcontroller can only receive inputs that are nonnegative relative to the microcontroller ground. The voltage being measured is the AC voltage connected outside of all filters, and outside of

the startup current control triac. This is the line to neutral voltage in the 120 V_{AC} operation and line to line voltage in the 240 V_{AC} operation.

The circuit contains a transformer with two 120 V_{AC} / 18 V_{AC} windings with the primary windings connected in series. The resulting output, between 0 and 18 V_{AC} is then rectified with a full bridge rectifier and a 100 Ω / 800 Ω voltage divider is used to ideally limit the voltage to 3.2 V_{peak}. The resulting output is not quite proportional to the ideal turns ratio, so this low output voltage is used to ensure the resulting voltage is never clipped by the 5 V_{DC} limit on the microcontroller analog input. The circuit can be seen below in Figure 4.8.

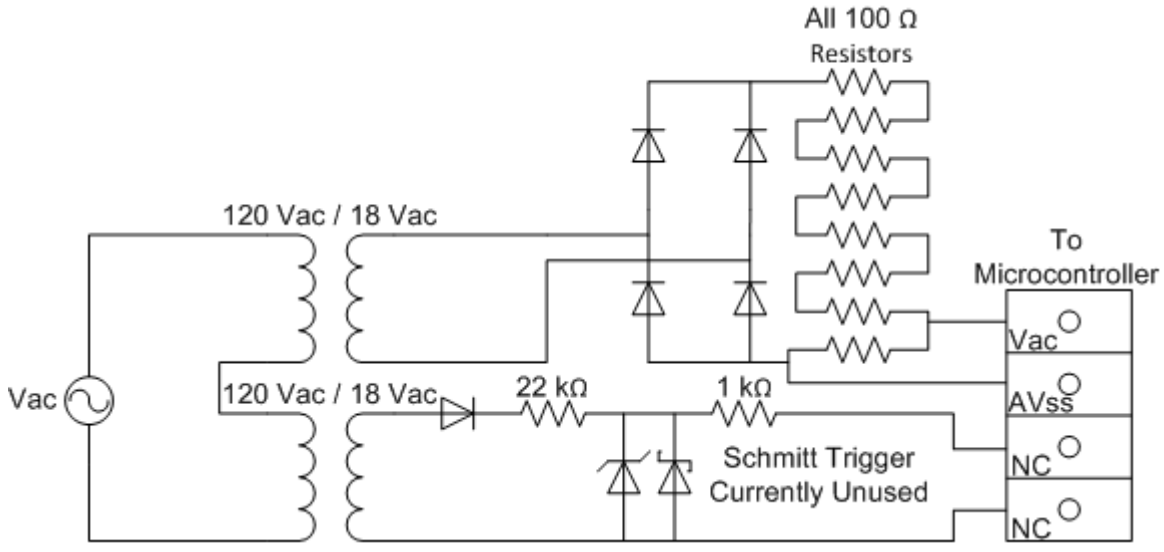

Figure 4.8: AC Voltage Measurement Circuit

In order for the PFC rectifier to shape the current, it requires high bandwidth AC current feedback. To do that, a hall effect current sensor is used. This sensor is

specifically designed for operation with a microcontroller – which is primarily why this style was chosen. The hall effect sensor is an Allegro® ACS756-050, rated for current up to 50 A_{peak}. The ACS756-050 requires ground reference and V_{CC} inputs, 0 and 5 V_{DC}, which is supplied from AV_{SS} and AV_{DD} respectively.

At 0 A, the ACS756-050 outputs a voltage equal to AV_{DD} / 2, relative to AV_{SS}. The output increases or decreases by 40 mV/A, between AV_{SS} and AV_{DD}, supplying an acceptable voltage range to the microcontroller. The hall effect sensor is placed in series with the return path from the AC/DC stage of the DIBPC, the path which carries the full AC current, regardless of the mode of operation. A simple low pass filter is placed on the output side of the ACS756-050, consisting of an output series resistor and two shunt capacitors with values of 1 kΩ and 0.1µF each, respectively. One shunt capacitor is placed between AV_{SS} and the ACS756-050 output and the other placed between AV_{DD} and the ACS756-050 output. This circuit can be seen below in Figure 4.9.

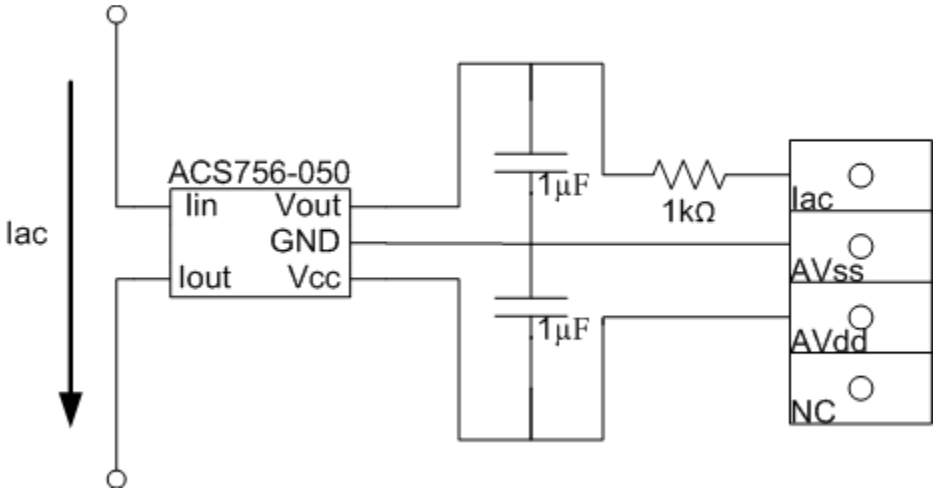

Figure 4.9: AC Current Measurement Circuit

Lastly, a voltage measurement must be taken at the DC bus. To ensure this voltage tracks the desired output, the voltage measurement must be taken. Due to the PFC rectifier's configuration, neither the DC bus voltage positive or negative are isolated or directly connected to the AC neutral or hot connections. Because the microcontroller connects to so many different peripherals (and for safety), it needs to remain referenced to either AC neutral or a floating voltage. Creating isolation between the DC bus reference and the microcontroller cannot be done with a simple transformer. To achieve this isolation, an isolation amplifier is used.

This isolation amplifier is capable of isolating DC or AC signals having a cutoff frequency at 2kHz and with an unity gain. For this application, the DC bus voltage ripple is low frequency (120 Hz), so this amplifier is easily able to capture an accurate waveform. A 10 kΩ / 1.11 MΩ voltage divider is used to keep the sample voltage within the range of the amplifier and the microcontroller ($0 - 5\ V_{DC}$). The amplifier requires a $15\ V_{DC}$ power supply relative to the amplifier output reference, which is sourced from the power supply shown in Figure 4.6. The output from the isolation amplifier is a voltage that can be input directly to the microcontroller. The DC voltage measurement circuit can be seen below in Figure 4.10.

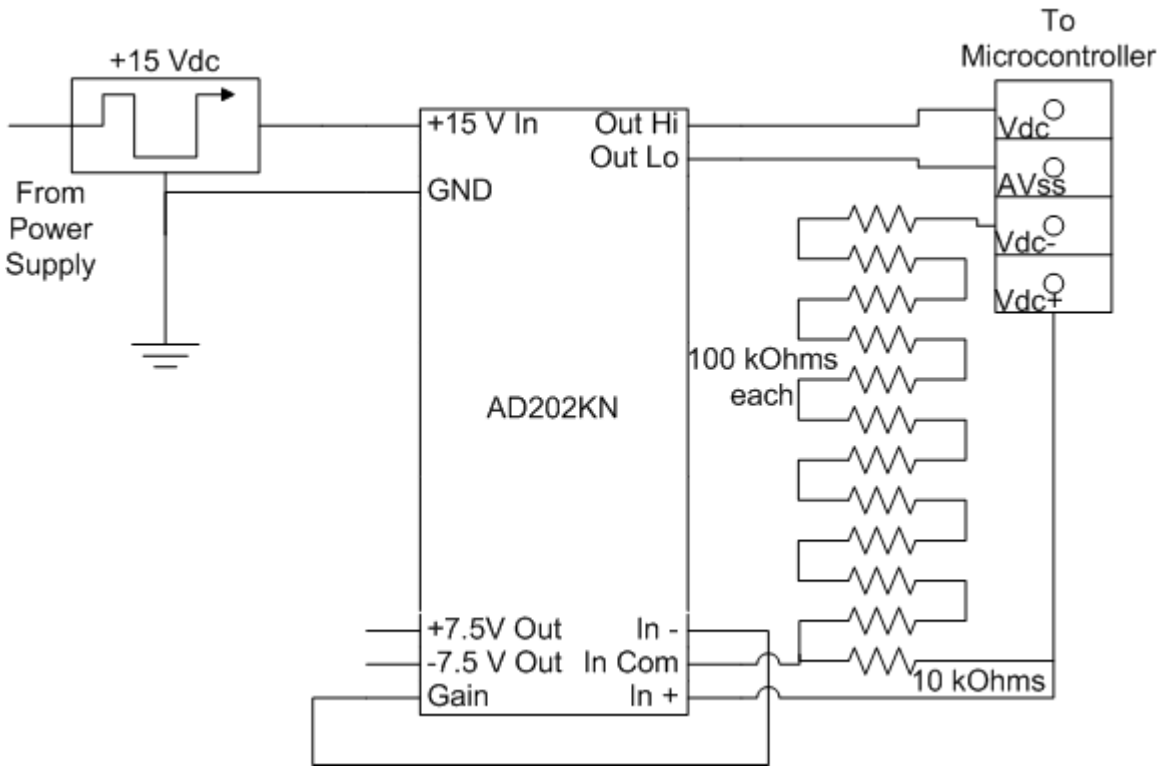

Figure 4.10: DC Voltage Measurement Circuit

Fault Protection

In order to provide continuously safe operation, fault protection has been incorporated into the DIBPC hardware. Overcurrent fault protection is implemented in hardware through the use of breakers and fuses on both the AC and DC portions of the DIBPC. AC overcurrent protection is provided by the AC/DC stage and DC overcurrent protection will be provided by the DC/DC stage of the DIBPC.

A circuit breaker is provided to protect against overloading and faults. This circuit breaker is a 15 A_{RMS} three phase circuit breaker. In the 120 V_{AC} operating mode,

only one channel of the 15 A_{RMS} circuit breaker is currently used. This provides integrated overload backup protection as well as fault protection. In the 240 V_{AC} operating mode, two channels of the circuit breaker are used, where the current is divided evenly between two of the channels. In the 240 V_{AC} mode, there are two hot channels. The circuit breakers are used to protect against bolted faults between the two hot leads and to protect against overloads. For hot to neutral (or ground) fault protection, an additional 30 A_{RMS} fuse is used on the hot line that is not operating through the circuit breaker.

For DC current protection, fuses are used. Because the DIBPC DC/DC stage was not constructed, temporary DC current protection was provided instead of the permanent protection that would be provided by the DC/DC stage. This was done through the use of semiconductor fuses which are applied between the DC bus capacitor positive and the positive of the IGBT 6-pack. This protects in the charging and discharging modes against shoot through faults in the IGBT 6-pack. This fuse also provides backup protection against AC loading faults which could occur in the discharging mode.

Hardware Issues and Troubleshooting

During the course of experimentation, several issues arose. The first issue that arose was a failure in the original IGBT 6-pack of one of the IGBTs or diodes. The second issue was the overloading of an inductor, resulting in its destruction. The final issue is the failure of four diodes in the second IGBT 6-pack. For each of these failures,

an analysis and diagnosis of the failure was performed along with the effect it has on the construction and the action taken in response.

The first IGBT 6-pack used, the PM75CVA120 from Mitsubishi®, was damaged very early during the testing process. When the gate drivers were being constructed and tested, a failure occurred. The upper IGBT (or diode) in the U branch of the IGBT was found to be short circuited. This failure is attributed to an error made during the initial construction of the gate drivers. The gate drivers were originally designed to invert the input signal, such that a digital high resulted in a low-state output to the IGBT 6-pack (the IGBT 6-packs are low-active). However, due to a mistake in wiring, the microcontroller's V_{SS} and V_{DD} outputs were swapped, resulting in no inversion in the gate drivers. When the gate drivers were tested on the U branch, the resulting inversion essentially resulted in an "always on" state when an off state should have been present. When the power to the gate drivers and the power to the test circuit were applied simultaneously, the upper U IGBT (or diode) was grossly overloaded, creating a short circuit.

In response to this failure, the U branch of the IGBT was not used. For all of the 120 V_{AC} charging mode testing, this was not an issue, as only two branches were needed. When the discharging or 240 V_{AC} charging modes needed to be tested, the third leg would be needed to operate as designed. Therefore the second IGBT 6-pack was acquired, the PM50CLA060, from Powerex®. This 6-pack was a direct replacement for the PM75CVA120, except with lower power ratings.

Chronologically, the second failure that occurred during testing was the overloading of the inductor. The inductor was self wound using the smallest gauge wire that could be used to still carry the current. This resulted in a very small safety margin in the loading of the inductor. During the charging mode software testing, the inductor was overloaded. This testing was aimed at improving the power factor of the input current by adjusting the proportional and integral gains of the PI controller discussed in the next chapter. During this testing process, the magnitude of the currents flowing through the inductors were not properly monitored, resulting in an unnoticed overload. Once the overload began, insulation began to melt, creating a short circuit in the inductor, and eventually resulting in the melting of most of the insulation and the destruction of the inductor.

In response to this failure, the existing damaged windings were removed from the inductor core and the core was wound again, using the same wire as before. To reduce the chance of this happening under normal operating conditions or during testing again, a 120 V_{AC} fan was installed to provide airflow across both of the inductors and across the heat sink connected to the IGBT 6-pack. This fan is operated using the same 120 V_{AC} supply that supplies power to the DC power supply for the gate drivers and microcontroller.

The last major failure that occurred was a failure of the second IGBT 6-pack. This failure resulted in the most damage, both in terms of components and cost. During the testing for the 240 V_{AC} charging mode, all four diodes in the U and V branches of the IGBT 6-pack failed. This failure occurred when 240 V_{AC} power was first applied to the

IGBT 6-pack across the U and V connections. Two branches of the 15 A_{RMS} circuit breaker were being used in parallel. The breaker tripped, but only after the diodes were short circuited.

After analyzing the failure, it was determined that the diodes each failed due to the current transient created while charging the capacitors. With the capacitors fully discharged, the 240 V_{AC} line was connected directly through the full bridge diode rectifier present as anti-parallel diodes in the IGBT 6-pack to the capacitors. Because the diodes failed as short circuits, the first diode failure cascaded into another diode failure. During the second half-cycle, the other two forward biased diodes failed as short circuits as well.

A simulation was performed to determine the maximum magnitude the current could have been based on the component values. The inductors were considered to be 1.35 mH and 300 mΩ each. The diodes each had a 1.2 V forward voltage drop. The simulation was run several times, closing the breaker at the peak of the waveform, at the zero crossing and at midpoints, seeing which resulted in the worst transient. The worst transient occurred when the breaker was closed with the AC voltage at 45º. The simulation results can be seen below in Figure 4.11.

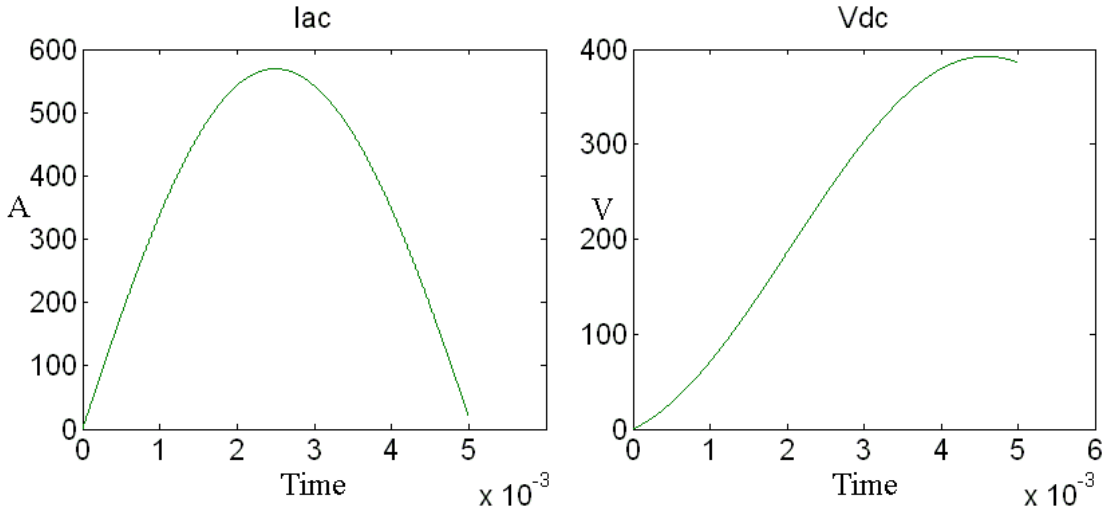

Figure 4.11: IGBT 6-pack Diode Failure Simulation Results

From the simulation, it can be seen that during the first half-cycle, a current spike of 550 A_{peak}, could be seen by the diodes. After reviewing datasheets and available literature, there is no listed surge rating for the diodes. Therefore there is no indication as to the amount of peak current that can be handled by the diodes for a half-cycle. Because these IGBT 6-packs are typically used in inverter applications, the diodes usually have no need to be rated for capacitor charging transients. It seems likely that a current of this magnitude for one half-cycle could result in the device being destroyed as seen. Once the first two diodes are short circuited in the first half-cycle, they would then create a short circuit path through the other two diodes in the second half-cycle, destroying those as well. A picture of the damaged IGBT 6-pack can be seen below in Figure 4.12.

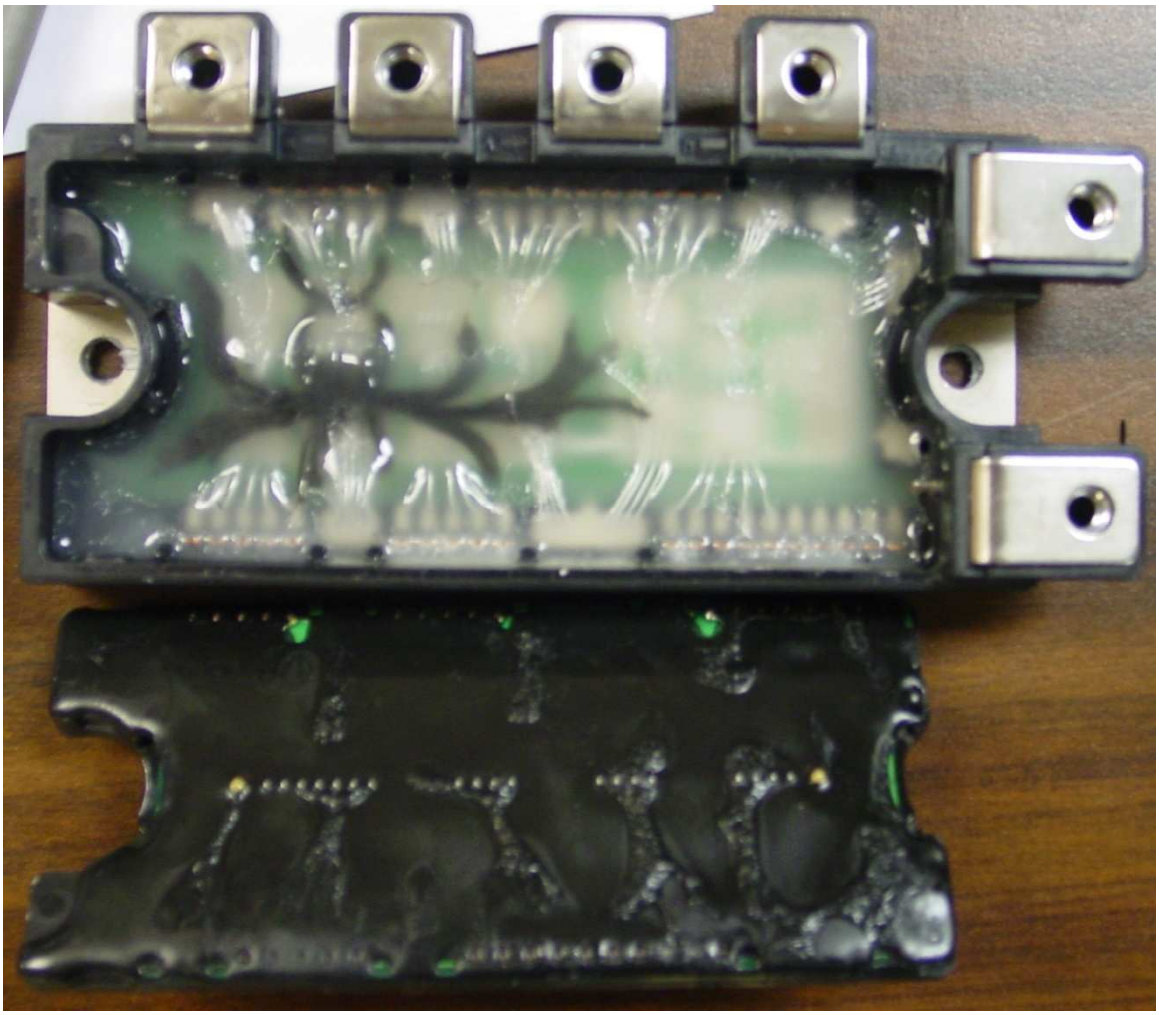

Figure 4.12: Damaged IGBT 6-pack

After analyzing the setup and the damage done, and after running those simulations, the following conclusion was reached. By line charging the capacitors, a current transient as high as 550 A_{peak} during the first half cycle destroyed one upper diode in either branch U or V and one lower in the other branch, resulting in short circuits through both. During the second half cycle those short circuits resulted in a short circuit

through the other two diodes of possibly even greater magnitude, destroying those diodes as well. The circuit breaker then tripped, preventing further damage to the system.

Due to limited resources, this second IGBT 6-pack was not replaced. To continue with the construction of the DIBPC, a design simplification was made which allowed the device to operate using only the two legs of the original IGBT 6-pack. The 120 V_{AC} charging mode only requires two legs and will proceed as before. The 240 V_{AC} charging mode requires all three IGBT legs, and must be modified. The discharging mode requires all three IGBT legs and must be slightly modified as well.

During the 240 V_{AC} charging mode, the connection to the IGBT U leg is now connected to V. This requires that all inductor current now travels through the one IGBT leg where both inductors are now connected in parallel at this point. To change back to the 120 V_{AC} charging mode, the second inductor should be lifted from this point. The modified configuration can be seen below in Figure 4.13

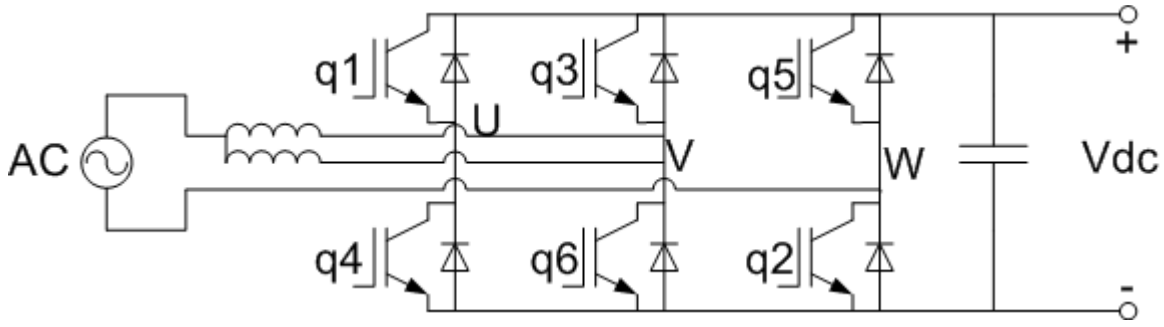

Figure 4.13: Modified 240 V_{AC} Charging Mode Configuration

In the discharging mode, now both 120 V_{AC} lines must be physically connected together at the IGBT leg V while the neutral remains at IGBT leg W. This only affects this configuration if it were operating such that it supplied 120 V_{AC} and 240 V_{AC}. In its current simplified operation, only 120 V_{AC} is output, and in phase. For this reason, the simplified operation remains essentially unchanged. The switching stresses are now the same on legs V and W, rather than U and V containing half that of W. If the discharging mode were to operate in the potential mode of operation, outputting full centered tapped 240 V_{AC} as described in the AC/DC stage design section of Chapter Two, it would be unable to operate with this modified configuration. In the potential mode, both AC lines are operated out of phase, which is impossible using this design. Figure 4.14 shows the modified discharging mode configuration.

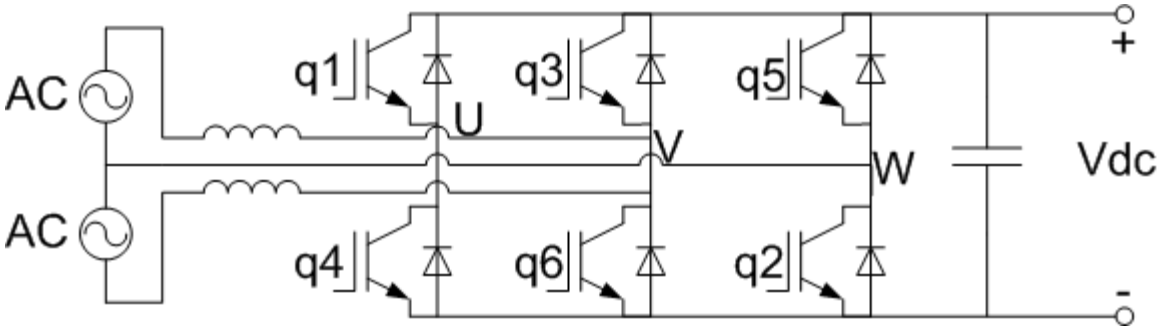

Figure 4.14: Modified Discharging Mode Configuration

With these changes, the construction of the DIBPC continued, although with losses in flexibility. To prevent the same event from occurring again, a capacitor charging current limiting circuit was constructed. This circuit uses a triac to control the

phase angle during startup, and therefore the duty cycle during capacitor charging. By measuring what point in the waveform the voltage is, the microcontroller can gate the triac on at varying phase angles, controlling the magnitude of the current flowing into the capacitors. The location of the triac can be seen in Figure 4.15, below

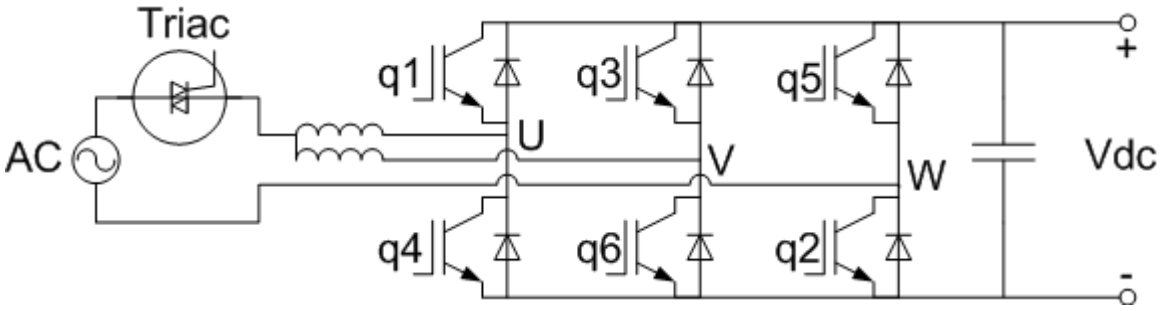

Figure 4.15: Slow Capacitor Charge Triac

This method allows a slow increase in the DC capacitor voltage and the AC current magnitude. By slowly increasing the duty cycle of the AC voltage waveform over a five second period, the capacitor voltage rises slowly as well, requiring the entire five second period to achieve its maximum voltage. Figure 4.16 shows the slow capacitor voltage rise and the constrained AC current.

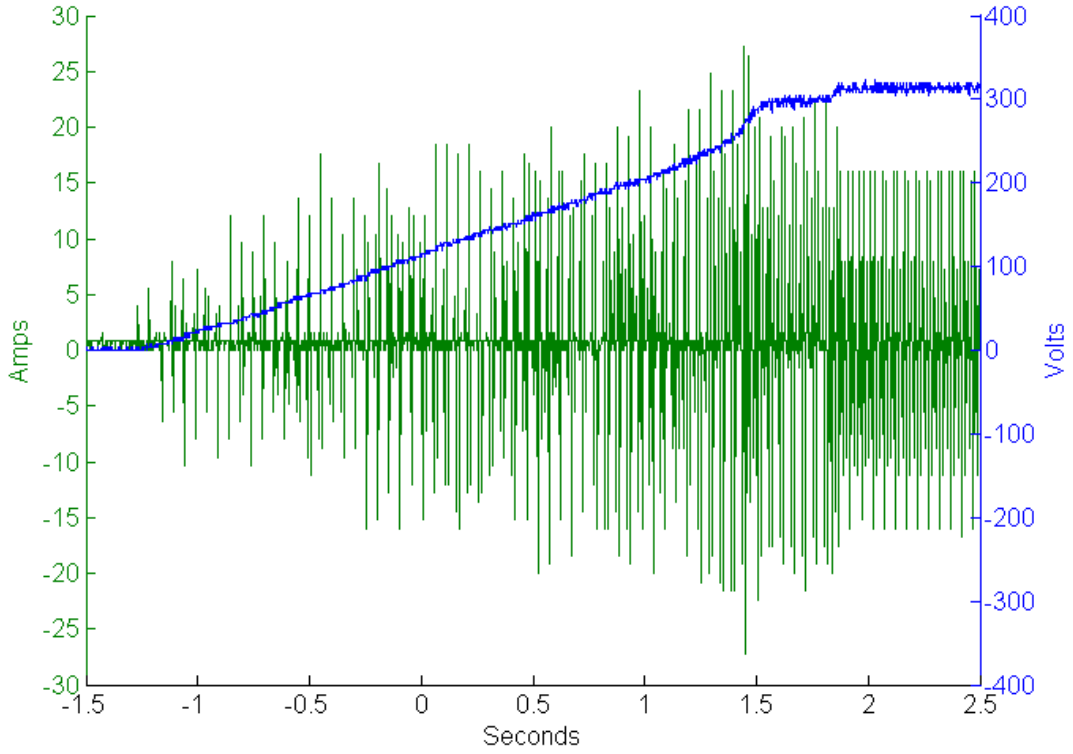

Figure 4.16: Slow Startup Capacitor Voltage and Input Current

Summary

The construction of the DIBPC was detailed in this chapter. Each major component along with all the supporting equipment was described and the integration into the overall system was illustrated. Because only the AC/DC stage of the DIBPC was constructed, this is the only part illustrated within this chapter. The major hardware issues that arose during construction along with any resulting actions taken were shown.

The next chapter discusses in detail the software used to control the system. The connections between the microcontroller and peripherals will be discussed and then the

operation of each function of the program will be explained. The hardware background given in this chapter along with the design concept given in Chapter Two should provide adequate background to understand the program used to control the DIBPC.

CHAPTER FIVE

EXPERIMENTAL SOFTWARE SETUP

The DIBPC requires a microcontroller to take measurements about the state of the DIBPC and to process that information. The microcontroller takes those measurements and performs scaling and calculations, then it converts those results into an output that can be used to operate the IGBT 6-pack gate drivers and other peripheral devices. In this chapter, the overview of the program is first discussed from a high level. Next, the setup for the microcontroller and the internal modules is explained followed by the main controller operation. The main controller operation is broken down into charging mode and discharging mode operation for simplicity. Finally, the ancillary functions performed by the microcontroller are detailed.

DsPIC30F2020 PIC® Overview Setup

As discussed in the last chapter, the microcontroller chosen for this application is the DsPIC30F2020 PIC® by Microchip. This microcontroller operates by executing a series of assembly instructions generated by the C compiler, MPLAB® C30. The DsPIC30F2020 operates at 20 million instructions per second (20 MIPS), with a clock frequency of 20 MHz. The microcontroller program is divided into several functions for easier understanding and more efficient operation. Because so many of these functions use the same variables, all of the variables used are defined globally.

The program is timed using interrupts, which occur at a predefined frequency. Therefore when the program first starts, it operates asynchronously, initializing all of the modules which will be used during operation. Once all of these initializations are complete, the last thing it will do is to start the interrupt timer (which is the analog to digital (AD) interrupt timer). Once this timer reaches its set point, the ADC module will trigger the AD conversion and then call the interrupt.

The interrupt handler will then store the AD buffers and begin operation of the controller. The first times the interrupt handler is called, it will call a startup sequence function to limit the startup current while charging the capacitors. Once this is completed, it will determine if it is in charging or discharging mode and begin operation. Each time the interrupt handler is called, it will perform all the calculations needed to update the gating outputs based on the system feedback. It will continue to loop through these update functions until the DIBPC is turned off or loses power. The flowchart for the program operation can be seen below in Figure 5.1.

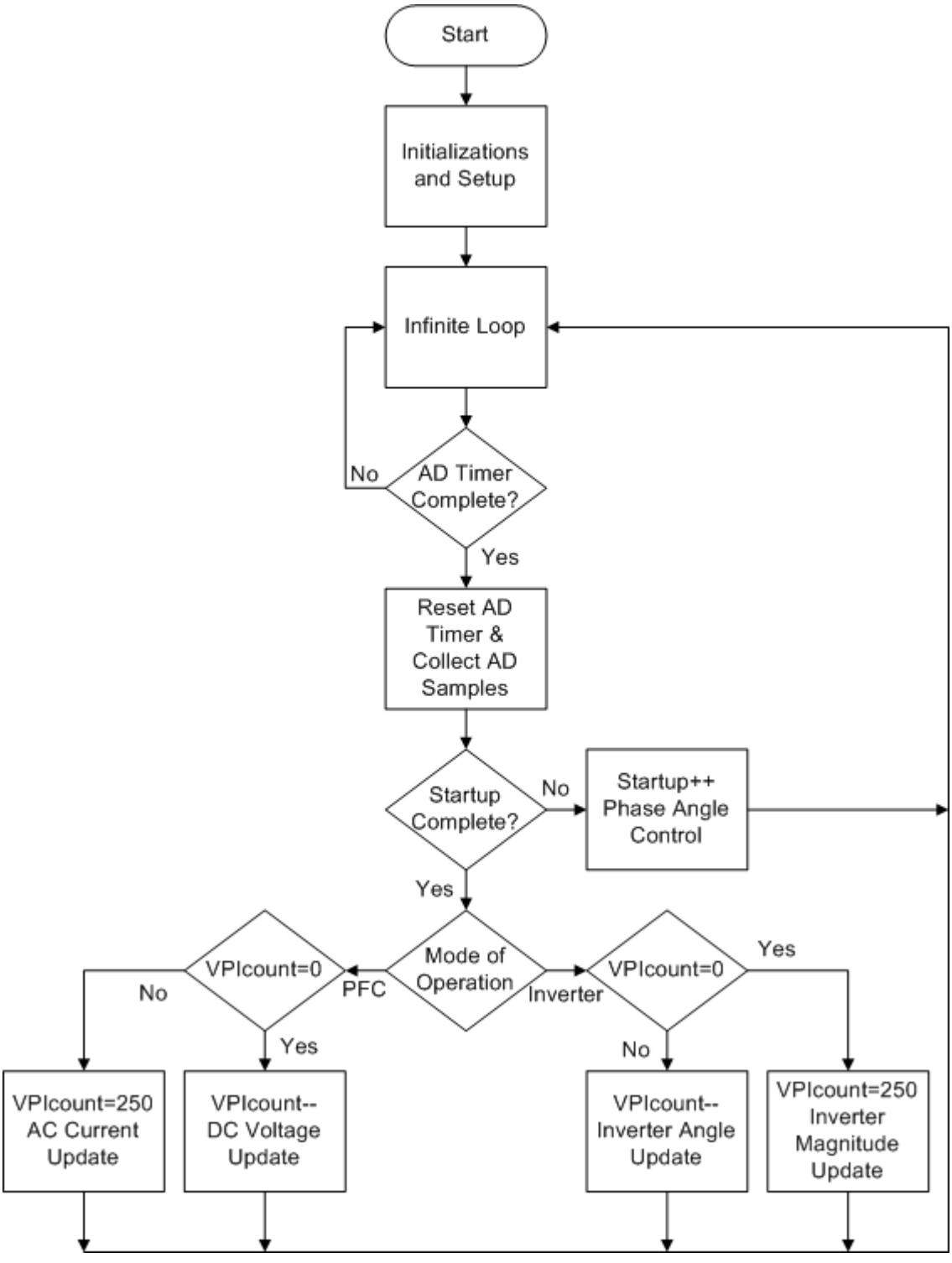

Figure 5.1: Microcontroller Program Flowchart

Microcontroller Module Setup

The microcontroller module setup is broken apart into the setup required for each different module. Each of these setups is performed using a different function within the program. These functions will be discussed one at a time in the order in which they are called. `SetupDigital()` is the first setup function called which is used to setup each individual digital input and output pin. Next, `SetupOC(), SetupTimers(),` and `SetupPWM()` are used to initialize the output compare module, the timers, and the PWM module, respectively. Finally, the `SetupAD()` function is used to initialize the ADC module and to begin the AD interrupt timer.

The `SetupDigital()` function contains the definitions for each used digital port. The `TRISBbits.TRISB2 = 0b1`; declaration sets the digital port `RB2` to be an input – `0b0` would be an output. Using these commands, the following digital ports are defined.

Port	I/O	Function
RB2	Input	Charging / Discharging Mode Toggle Switch
RB3	Input	120 V_{AC} / 240 V_{AC} Toggle Switch
RE0	Output	IGBTs q_1 (U_P) and q_3 (V_P) in Discharging Mode
RE2	Output	IGBTs q_4 (U_N) and q_6 (V_N) in Discharging Mode
RE4	Output	Triac Input Gate
RE6	Input	Originally Schmitt Trigger / Now Unused
RE7	Output	Output 120 V_{AC} or 240 V_{AC} State to Optocoupler Inputs

Table 5.1: Microcontroller Digital I/O Functions

Inside the `SetupDigital()` function, `RB2` and `RB3` are also defined as change notification inputs. The change notification function allows an interrupt to be inserted whenever the state of one of these inputs changes. At this time, however, the change notification interrupt handler is disabled due to false tripping. Finally, one last command must be addressed. The first line contains the `LATE` definition, forcing it to set the fifth bit (`RE4`) using a bitmask. This bit is initialized to one to ensure that the triac is not initially gated on (the triac is low-active from the digital output).

Once the digital setup is complete, the output compare module is initialized. This is done using the `SetupOC()` function. This function sets the registers which control the output compare module. Two output compare channels are used, one which operates the IGBT U and W legs and one which operates the IGBT V leg, but only in the charging mode. The registers set the output compare module to operate in the PWM mode and initialize the duty cycle to zero.

The `SetupTimers()` function is used to initialize the two timers. One timer is used for the output compare module timing (switching frequency) and one is used to control the AD interrupt frequency. The switching frequency is set to 20 kHz and the AD interrupt frequency, which controls the update rate, is set to 5 kHz. The AD interrupt is also enabled and the priority level set here.

The `SetupPWM()` function is used to configure the PWM module. This function contains the PWM switching frequency registers, determination of the operating mode (single PWM mode), instant update enable and deadtime settings. The deadtime settings are required to ensure that there is no small overlap once one IGBT is gated off and one

IGBT is gated on where they could both be on at the same time. The deadtime settings ensure that no shoot through fault can occur.

The last setup function is the `SetupAD()` function. This function determines what data type the AD buffer is stored as, sequential sampling, conversion frequency, converstion triggers, interrupt enables and analog input pin configurations. The AD channels are `AN0`, `AN1`, `AN4` and `AN5`, which input V_{DC}, V_{REF}, V_{AC}, and I_{AC}, respectively. The AD conversions occur in pairs, where `AN0` and `AN1` are a pair and `AN4` and `AN5` are a pair. This allows these to be sampled simultaneously and then converted sequentially. All conversions are triggered from the timer that also generates the AD interrupt. Lastly, the interrupt is enabled and the ADC module is enabled.

Charging Mode Controller

The AD interrupt handler, which controls the timing for the program, first contains a basic branch. The interrupt handler chooses the charging mode or discharging mode controller based on the status of the toggle switch connected to `RB2`. If the toggle switch is set to the charging mode, then the interrupt handler branch begins executing two functions. These two functions are used to update the duty cycle output of the output compare registers which correspond to the PFC rectifier IGBT duty cycle. The first function is used to control the output DC voltage. The second function is used to shape the AC current waveform and to improve the power factor.

The DC voltage function is only executed at a frequency of 20 Hz. This slow update is to eliminate the DC voltage ripple from propagating into the control feedback. By undersampling this ripple frequency (120 Hz), the controller operates much too slow to try to adjust the voltage for the 120 Hz ripple, avoiding a resulting increase in the ripple voltage. The function `DCVoltageLoop()` contains the calculations that update the desired AC current magnitude based on the DC voltage value. As the DC voltage decreases, the desired AC current magnitude is increased.

The `DCVoltageLoop()` function first sets a desired DC voltage value. This value is slowly increased so that the desired voltage does not cause a current spike. To save computational power, almost all variables that are used in the controller are stored as integers. In order to allow all operations to occur as integer operations, they must be normalized and then scaled so that they use all of the integer scale without overflowing. This normalization process is used in all functions.

Once all values are normalized, the DC voltage error is calculated and then a PI controller is used to determine the desired output. The PI controller is integral gain dominated, although all the gains are very slow. This is because the magnitude values need to respond slowly to change, avoiding oscillation due to a few noisy measurements. The output from this function is the variable `Vpi`, which is an input in the `ACCurrentLoop()` function.

The `ACCurrentLoop()` function is used to calculate the duty cycle which will be output via the output compare module to the IGBTs controlling the inductor spooling. To calculate this duty cycle, two components are summed together. First, a template of

the desired current is created from the AC waveform. Secondly, a proportional controller is created from the error between the AC current measurement and desired value. The template is used to overcome nonlinearities in the relationship between the duty cycle output and the current, and the proportional controller is used to conform the AC waveform to the desired value.

The template is used to boost the duty cycle output at the zero crossings and reduce it near the peak of the signal. Near the zero crossings, a very high duty cycle is needed for the inductor to spool enough current to forward bias the diodes when the IGBTs are gated off. Near the peak of the signal, a small change in duty cycle will result in a very large change in the output current. For this reason, the template is created by taking a constant value and subtracting a normalized version of the AC voltage from it.

The proportional controller takes the `Vpi` variable and multiplies it by a normalized version of the AC voltage. This creates the desired AC current waveform. The measured AC current waveform is subtracted from the desired to create an error variable. This error is then multiplied by a gain and then added to the template. The addition of these two components creates the duty cycle which is output to the IGBTs for current spooling. Figure 5.2 illustrates the effect each component plays on the overall duty cycle output.

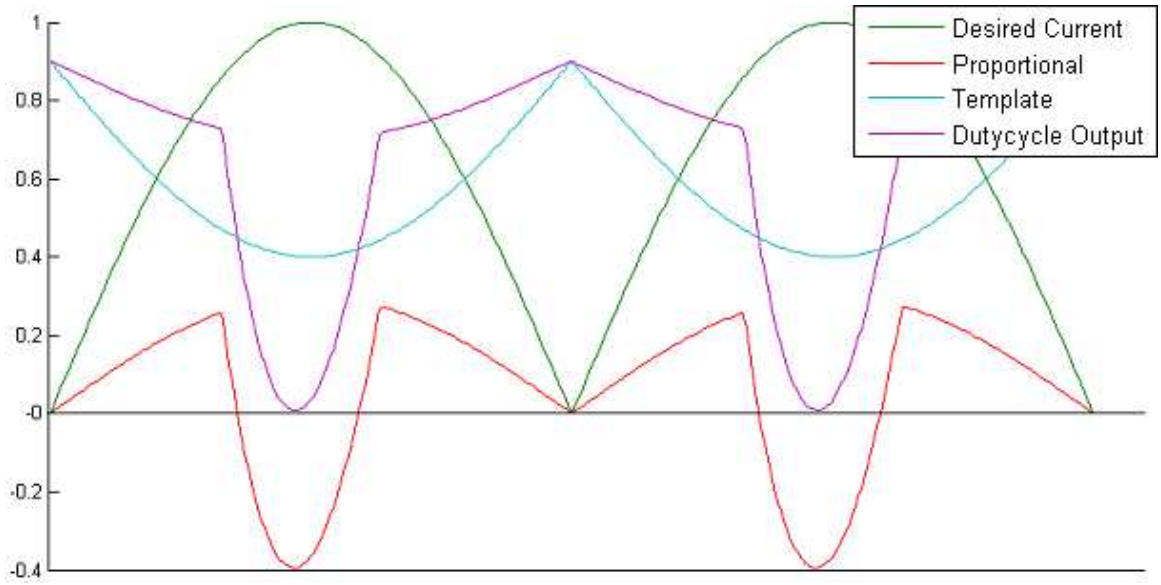

Figure 5.2: Duty Cycle Creation Components

Discharging Mode Controller

When the DIBPC is operated in the discharging mode, the AD interrupt handler executes a separate set of code. This code also consists of two separate functions. One function, the `InverterMagLoop()`, is used to update the magnitude of the desired AC voltage waveform at 20 Hz. The other function, `InverterSineLoop()`, is used to update the shape of the AC voltage waveform at 5 kHz. Once the duty cycle is determined, it is output to the PWM pins PWM1H and PWM2H. These pins are then directed to IGBTs q2 and q5.

The `InverterMagLoop()` consists of a PI controller that ensures the magnitude of the AC voltage tracks the desired value. The desired value is calculated by scaling a defined sine table to the same scale as the AC voltage measurement. The error

between the measured AC voltage and the desired AC voltage is used in a PI controller to ensure the voltage magnitude tracks the desired value. The PI controller gains are fairly slow moving, but mostly proportional, designed to minimize sharp changes based on just a few measurements. The output from this function is the `VinvPI` variable, which is used in the `InverterSineLoop()`.

The `InverterSineLoop()` function performs two actions. First, the function must calculate the PWM duty cycle. A sine table is defined and used to determine approximately what the duty cycle should be at each point in the cycle. The `VinvPI` variable from the `InverterMagLoop()` function is used as a scalar to ensure the output is of the correct magnitude. The scalar is multiplied by the sine table for the given angle (which is incremented after each iteration) and output as the duty cycle to the PWM module.

Next, the function must determine whether the inverter should output in the positive half cycle or the negative half cycle. An open loop timer is created to operate at about 120 Hz by counting the number of cycles that pass in the 5 kHz loop. Every 41 loops, the inverter toggles the IGBTs controlling the polarity of the output. The function continuously outputs to all the PWM pins, but every half cycle, half of the PWM pins are overridden in software to prevent them from operating in the wrong half cycle. Digital logic outputs RE0 and RE2 are also toggled at each zero crossing. These PWM and digital output pins are directed to the correct gate drivers through the optocoupler circuit described in the last chapter.

Microcontroller Ancillary Functions

The microcontroller is used to perform other functions that are not primary to the control of the system. The first of the three functions is digital switching, including 120 V_{AC} and 240 V_{AC} mode input along with charging and discharging mode. The second function is startup detection and the limiting of the startup current through the gating of the triac. The final function is for system protection, both AC overcurrent and DC overvoltage protection.

The microcontroller has two digital inputs which are dedicated to the toggle switches. These switches allow the program to decide in which mode it should operate. The microcontroller also uses a digital output for switching. This digital output is used to drive the three optocouplers. These optocouplers are driven through a circuit described above to direct the microcontroller PWM and digital outputs to the correct gate drivers. The optocoupler input is a digital input, representing either the charging or discharging mode.

The microcontroller also provides current limiting during startup. To do this, it must first determine when startup occurs. Once the power to the microcontroller is applied and the setup functions are completed, it will enter a wait state. The microcontroller is waiting to detect AC or DC voltage above a certain threshold. Once this threshold is exceeding, it enters the slow current startup routine.

The slow current startup routine is simply a couple of nested branches. The first iteration into this startup routine, the microcontroller determines what part of the

waveform the voltage is in. To activate the gate of the triac, and allow current to flow into the capacitors, three conditions must be met. The AC voltage magnitude must be decreasing (heading towards a zero crossing), it must be greater than a constant threshold (60 V), and it must be less than a starting threshold (80 V). When these conditions are met, the triac is gated on and the starting threshold that the AC voltage must be beneath is increased. When the conditions are met again (next half cycle), the triac will gate on at a slightly higher voltage. This loop will continue until the voltage of the capacitor has increased to almost the peak of the AC voltage. At this point, the triac gates on continuously and the startup routine is complete.

The final ancillary function of the microcontroller is software fault and overload protection. AC overcurrent protection is provided by limiting the magnitude of the desired AC current. This magnitude is limited to the breaker current (30 A_{RMS}) by limiting the output from the DC voltage PI controller to a constant which represents an AC current magnitude of 30 A_{RMS}. DC overvoltage protection is performed in the charging mode by simply outputting a duty cycle of zero whenever the DC voltage exceeds 450 V_{DC}.

Summary

This chapter explains the operation of the DIBPC microcontroller. The program is divided into several functions. The setup functions, executed initially, set the registers to the values needed for the proper operation of the microcontroller. After initialization,

the interrupt driven program begins to operate at an update frequency of 5 kHz. The interrupt handler waits until voltage is applied, then it begins the slow current startup sequence and then executes the code for the charging mode or the discharging mode function. In each of these modes, a function that updates at 20 Hz recalculates the magnitude and a function that updates at 5 kHz recalculates the next duty cycle value.

The next chapter will discuss the experimental and simulation results. Comparisons will be made between these results and between the simulations and theoretical expectations. Various analyses will be performed to determine the overall operation of the system in both the charging and discharging modes and in the various states of loading.

CHAPTER SIX

RESULTS AND DISCUSSION

This chapter examines the operation of the DIBPC. The experimental and simulated operations are compared under various tests. A series of tests have been used to determine how the DIBPC reacts to different loads in each mode of operation, first in the charging mode, then in the discharging mode. The simulation and experimentation results for each of these modes are discussed separately. For each mode of operation, several cases are considered, including various loads, input voltages and control strategies. Each parameter is examined in simulation and experimentation and compared for each case.

The results were analyzed to ensure that all the design constraints were met. For every charging mode test, the AC current and DC voltages are examined. The AC current THD and the power factor are calculated, and the efficiency is estimated. In the discharging mode, the AC voltage and current are examined. The AC voltage and current THD and power factor are calculated. These results are all each found for the experimentation and simulation and discussed.

Charging Mode

In the charging mode, four tests were performed experimentally, and one more was simulated. At 120 V_{AC}, 100 Ω and a 200 Ω loads were connected to the output. This

is representative of full load and half load at 120 V_{AC}. At 240 V_{AC}, 25 Ω and 50Ω tests were performed, also representative of full load and half load. All these cases were also performed in simulation, along with one other. In simulation, the 120 V_{AC} full load (100 Ω) case, was also performed using the hysteresis control scheme.

For each of these tests, several things were observed. First, the DC voltage was observed, looking for the value and the ripple. The simulated DC voltage ripples can be seen below in Figure 6.1.

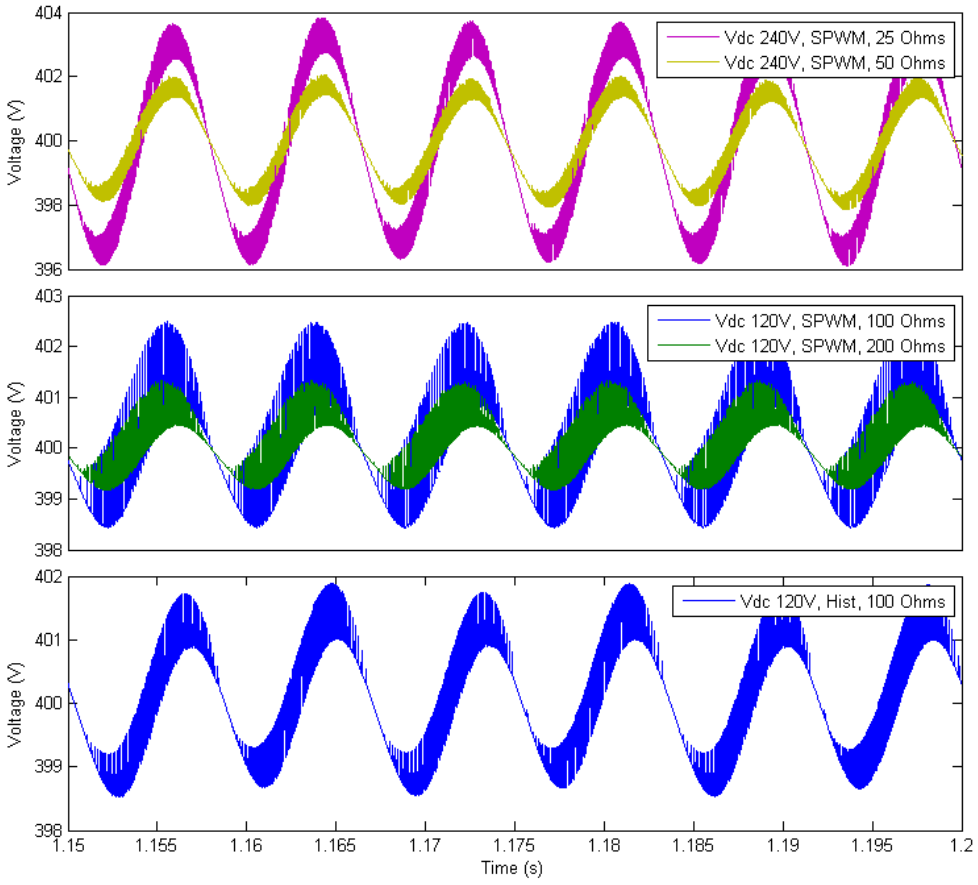

Figure 6.1: Charging Mode Simulated DC Bus Voltages

For each of these cases, the steady state voltage is very close to 400. The voltage ripple magnitude is proportional to the input current and present at twice the line frequency (120 Hz). The 30 A_{AC} input current (240 V_{AC}, 25 Ω case) has the maximum ripple of about 7 V_{P-P}. The 120 V_{AC} with 100 Ω load, the 240 V_{AC} with 50 Ω load and the 120 V_{AC} with 100 Ω load and hysteresis control cases all have an input current close to 15 A_{AC} and a ripple between 3 and 4 V_{P-P}. The 120 V_{AC} with 200 Ω load case has approximately 7.5 A_{AC} input current and a ripple voltage of about 2 V_{P-P}. Each of these cases is well within the tolerance for voltage ripple which would easily be filtered by the DC/DC stage. Figure 6.2, below, shows the experimental DC bus voltages.

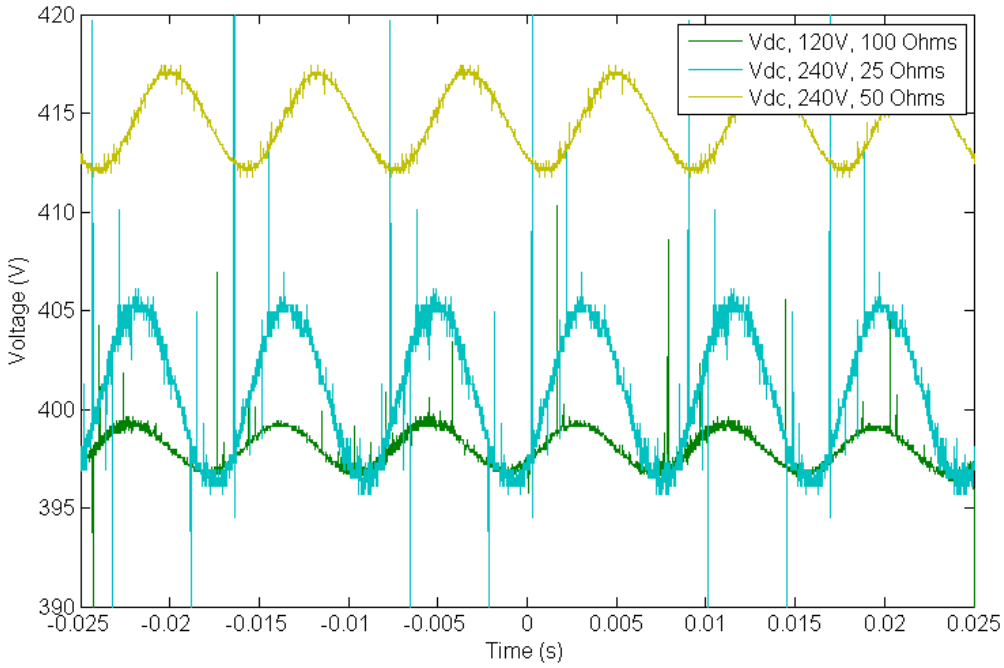

Figure 6.2: Charging Mode Experimental DC Bus Voltages

Experimentally, the DC bus voltage is measured for each case as well. For the 120 V_{AC} and 240 V_{AC}, 25 Ω cases, the steady state voltage is very close to 400 V_{DC}. However, for the 240 V_{AC}, 50 Ω case, the DC bus voltage is a little higher, closer to 415 V_{DC}. This would not be a problem for the capacitor ratings or the DC/DC stage; however it is indicative of an issue with the controller. The controller should be able to achieve a steady state voltage at 400 V_{DC}, and the inability to do this indicates some software limit is being reached which inhibits the integral term of the PI controller from reaching the desired steady state value. The ripple voltage values are proportional to the output power, ranging from 2 – 9 V_{P-P}, close to the simulated values.

Next, Figure 6.3 shows the simulated AC current values. These simulated values are not filtered, thus the switching frequency ripple can still be seen in the AC current waveforms.

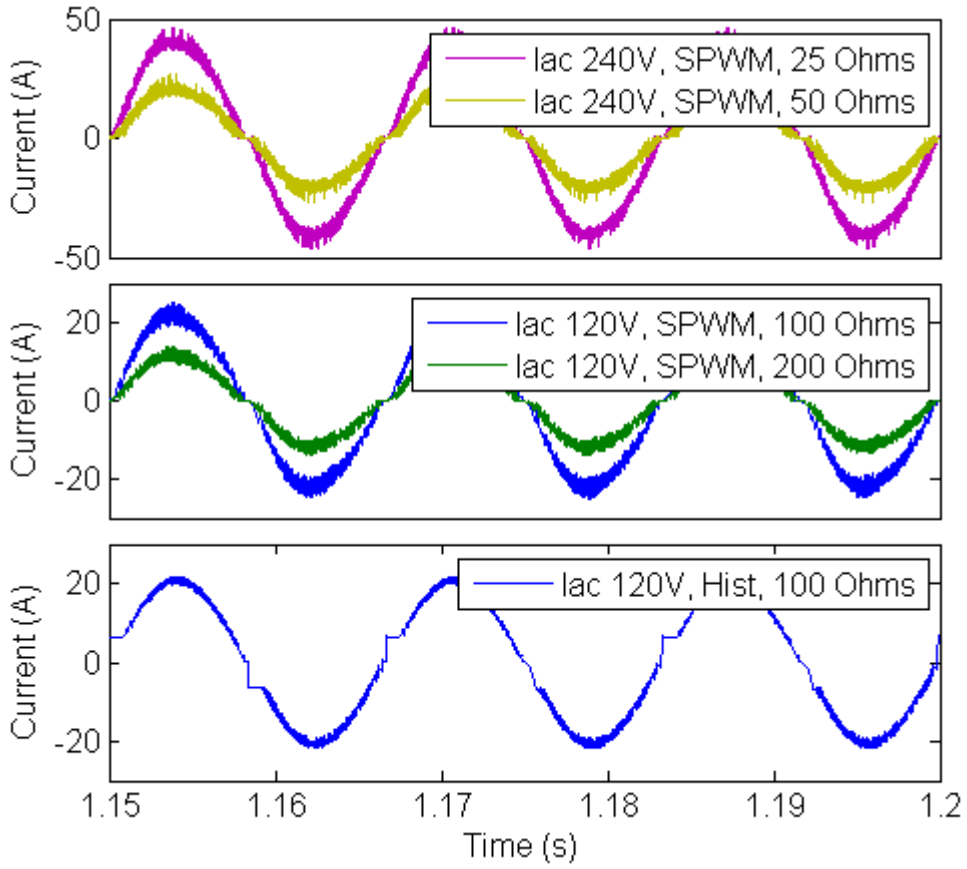

Figure 6.3: Charging Mode Simulation AC Currents

The sinusoidal PWM controlled currents all have similar wave shapes. They very closely follow the desired sinusoidal waveform with the exception of a small zero crossing distortion (flat spot), and the ripple current. These two distortions can be seen in each of the SPWM waveforms, regardless of the load size. The ripple magnitude is approximately proportional to the AC current magnitude. The hysteresis controlled waveform has a different kind of zero crossing distortion. In the hysteresis controlled simulations, each of the waveforms have a notch that begins at the positive and negative zero crossings. The ripple current is slightly less in the hysteresis controller as well, due

to the hysteresis band settings and a variable switching frequency that is sometimes higher than 20 kHz. The experimental currents measured for each case can be seen below in Figure 6.4.

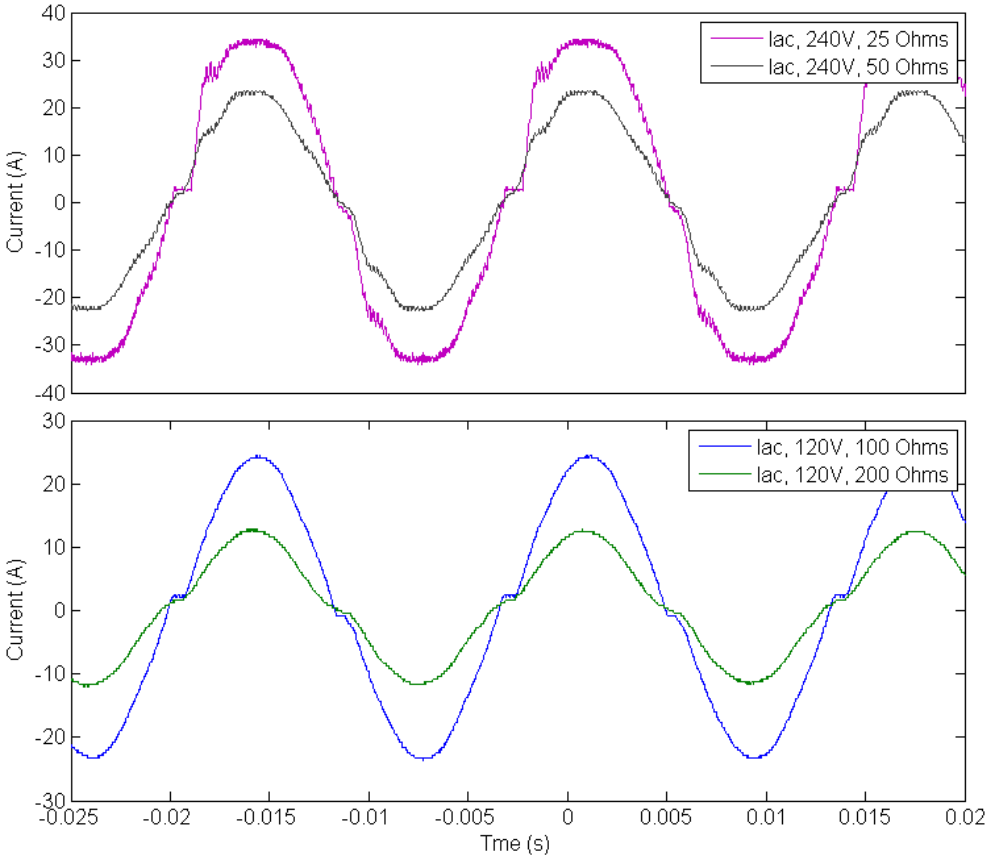

Figure 6.4: Charging Mode Experimental AC Currents

The measured currents for each of the experimental cases are filtered through the AC line filter discussed in Chapter Four, resulting in a very small ripple at the switching frequency. The distortion at both 120 V_{AC} cases can only be seen at the zero crossing;

the current otherwise looks very sinusoidal. The flat spot at the zero crossing is hard to minimize. The closer to the zero crossing, the higher the duty cycle must be in order to create a voltage across the inductor high enough to forward bias the diodes. This zero crossing flat spot exists in all experimental cases.

The 240 V_{AC} currents are distorted on the rising edge of the rectified waveform, near the peak. This distortion is due to the duty cycle template created from the AC voltage waveform to minimize the nonlinearities that are present in the duty cycle. The template is tuned at the peak and zero crossings of the waveform, leaving this midpoint distortion. The distortion is much more evident at 240 V_{AC} than at 120 V_{AC} because the 240 V_{AC} waveform has a much larger variation in the duty cycle throughout the half cycle – a very low duty cycle near the peak (<15%), and a very high duty cycle near the zero crossing (>95%) while the 120 V_{AC} only varies from about 57.5% - 95%, ideally.

The ideal waveform would be perfectly sinusoidal and exactly in phase with the AC voltage waveform. To attempt this, the microcontroller has to measure the AC voltage waveform as a reference. The true power factor is a measurement that encompasses the phase shift between the voltage and current and the harmonic content present. Figure 6.5, below, shows the voltage and current for the 120 V_{AC}, 100 Ω load case.

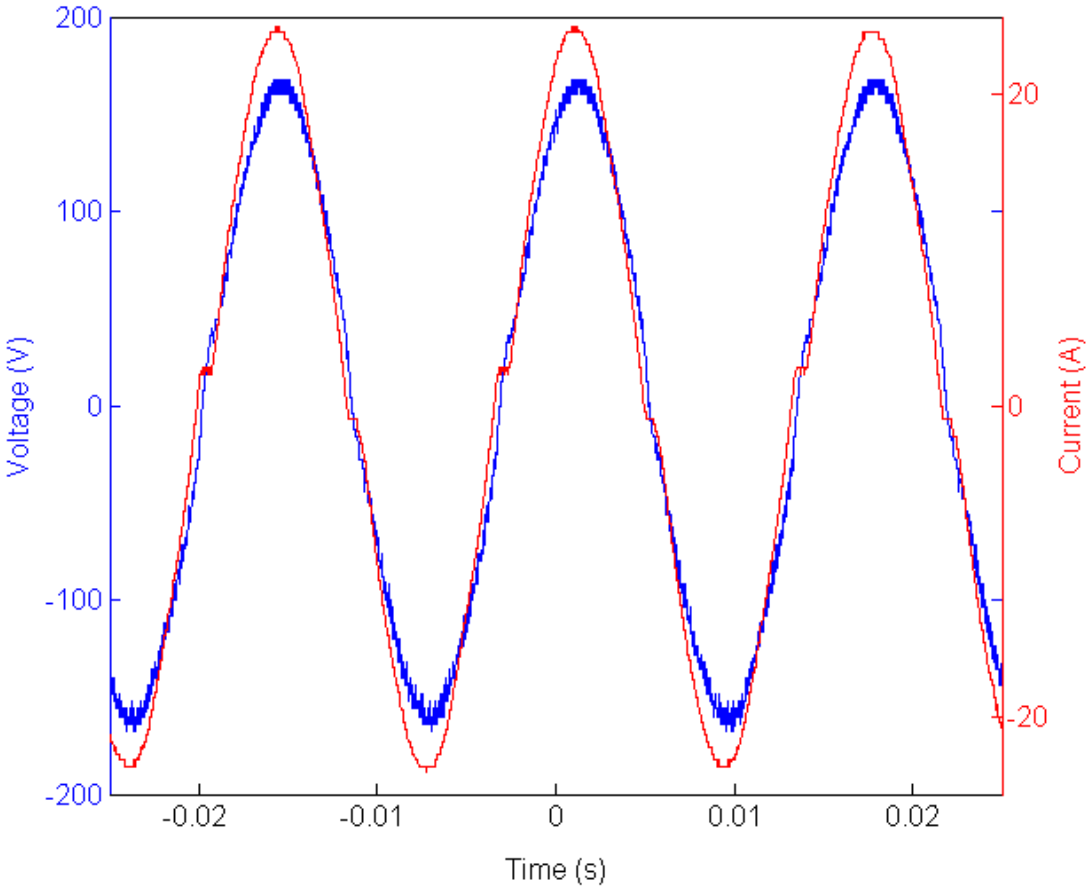

Figure 6.5: Charging Mode Experimental AC Current and Voltage

It can be seen in Figure 6.5 that the AC voltage and current have a very small phase shift between them, almost negligible. This produces a very high true power factor and minimizes the I^2R losses in the line. Table 6.1, below, shows the measured true power factor and THD from each experimental and simulated case. The true PF is very high in all cases, only reaching 0.97 in the worst case. These experimental true power factors were founding using the Tektronix® TPS2024 oscilloscope's power analysis function.

	Simulation True PF	Experimental True PF	Simulation THD_I	Experimental THD_I
120 V_{AC} 100 Ω	.995	.99	9%	7.7%
120 V_{AC} 200 Ω	.995	.99	13%	13.35%
120 V_{AC} 100 Ω Hysteresis	.990	N/A	7.5%	N/A
240 V_{AC} 25 Ω	.998	.97	15%	8.7% (5.5%)
240 V_{AC} 50 Ω	.985	.98	9%	7.4%

Table 6.1: Charging Mode True Power Factor and THD

The THD_I for each case was calculated using Matlab® over at least one period. The THD of the simulation, in most cases, was worse than the THD_I for the experiment. This can most likely be attributed to the AC filter that was used to minimize the high frequency ripple. The THD of the hysteresis controller is somewhat better in simulation than the equivalent SPWM controlled case – this is due to the slightly higher switching frequency resulting in a lower current ripple.

The THD in all experimental cases was primarily a result of the third harmonic. Because the third harmonic was the major harmonic distortion component, the IEC standards mandating that the third harmonic magnitude be less than 21.6% are easily met. The 240V_{AC} cases tend to show a higher THD, both in simulation and experimentation. This is most likely due to the range of the duty cycle throughout a given half cycle. Providing much more boost at 120 V_{AC} through the entire waveform tends to require a slower change in the duty cycle throughout the half cycle, making tuning easier. At 240 V_{AC}, the quick duty cycle variations required to boost to 400 V_{DC} from an AC signal of 0 – 340 V is more difficult to tune, resulting in more distortion.

Table 6.1 shows a 8.7% THD_I for the 240 V_{AC}, 25 Ω case, with 5.5% in parenthesis. This 5.5% indicates that a THD of 5.5% has been achieved for this load level; however these were not the optimum controller parameters for other cases. A THD of 5.5% in the 25 Ω case resulted in a very large distortion in the 50 Ω case. If enough time was spent optimizing the controller gains, significant improvements in the THD_I in all cases could likely be achieved. Next, the efficiency is examined, as seen in Table 6.2.

	Simulation Efficiency	Experimental Efficiency
120 V_{AC} 100 Ω	86.7%	83.7%
120 V_{AC} 200 Ω	83.8%	84.5%
120 V_{AC} 100 Ω Hysteresis	*91.4%	N/A
240 V_{AC} 25 Ω	94.1%	94.6%
240 V_{AC} 50 Ω	93.1%	89.7%

Table 6.2: Charging Mode Simulated and Experimental Efficiency

Table 6.2 lists the simulated and experimental efficiencies for all cases in charging mode. It is immediately obvious that a significant improvement in the efficiency can be seen at higher loading levels, especially at 240 V_{AC}. One of the major goals of this topology was the ability to insert and remove a second inductor and provide different tuning for 120 V_{AC} and 240 V_{AC} to improve the efficiency at 120 V_{AC}. Therefore the large drop in efficiency at 120 V_{AC} is very disappointing. The asterisk beside the hysteresis controlled efficiency indicates that some unrealistic components were used.

Most of the power lost can be attributed to a few devices. The largest power loss is probably seen in the IGBT switching losses, the inductor resistive and magnetic losses, the capacitor equivalent series resistance (ESR) and the AC filter. By lowering the switching frequency to 20 kHz, much lower than typical PFC rectifier applications, some of the switching losses were reduced, however this required the use of a larger inductor and more losses in the inductor.

The simulation results for the charging mode with the DC/DC stage can be seen below in Figure 6.6. The DC/DC Stage was added to the AC/DC stage in simulation to see the effect that the DC/DC stage would have on the AC/DC stage of the DIBPC. The simulation was performed for the 240 V_{AC} case with a 25 Ω load. The effect seen was almost negligible.

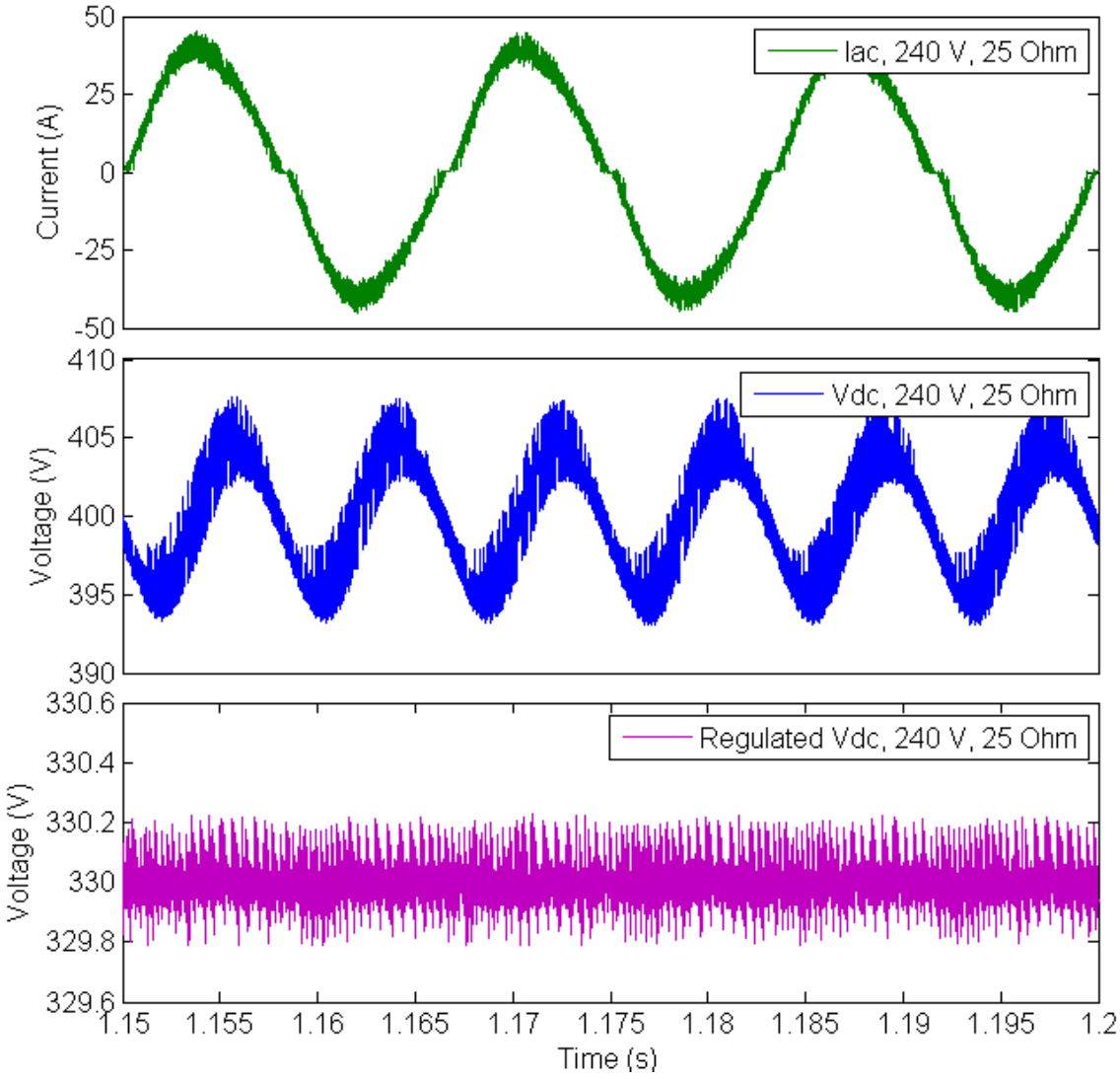

Figure 6.6: Charging Mode with DC/DC Stage Simulation

When the output power was set to the same value, the results in the AC/DC stage were very similar. The DC/DC stage was operated in two modes, much as it would be in implementation. The current controlled and voltage controlled modes offered almost no difference in the operation of the AC/DC stage of the device. The efficiencies listed

below in Table 6.3 may not be truly representative of the results, as several unrealistic components were included.

	True PF	THD_I	Efficiency
Current Controlled	.995	11%	92.9%
Voltage Controlled	.997	11%	92.8%

Table 6.3: Charging Mode with DC/DC Stage Simulation Results

The results for the charging mode showed that all of the major requirements for the DIBPC AC/DC stage have been achieved. The output voltage can be maintained while the true power factor remains high and the THD_I remains low. The disappointing $120V_{AC}$ efficiency results could probably be greatly improved, but the 120 V_{AC} efficiency would probably still remain significantly lower than the 240 V_{AC} efficiency. An achievable 120 V_{AC} efficiency is probably about 90% at full load. Next, the discharging mode results are discussed.

Discharging Mode

The discharging mode of operation underwent three experimental test cases and two simulated test cases. The simulated test cases were loaded at 4 Ω and 8 Ω, representing full load and half load. The experimental test cases were loaded at 6 Ω, 12 Ω and 30 Ω. The 4 Ω case could not be used experimentally because the DC source used

for testing reached its current limit at approximately 6 Ω of AC load. The simulated AC voltages can be seen below in Figure 6.7.

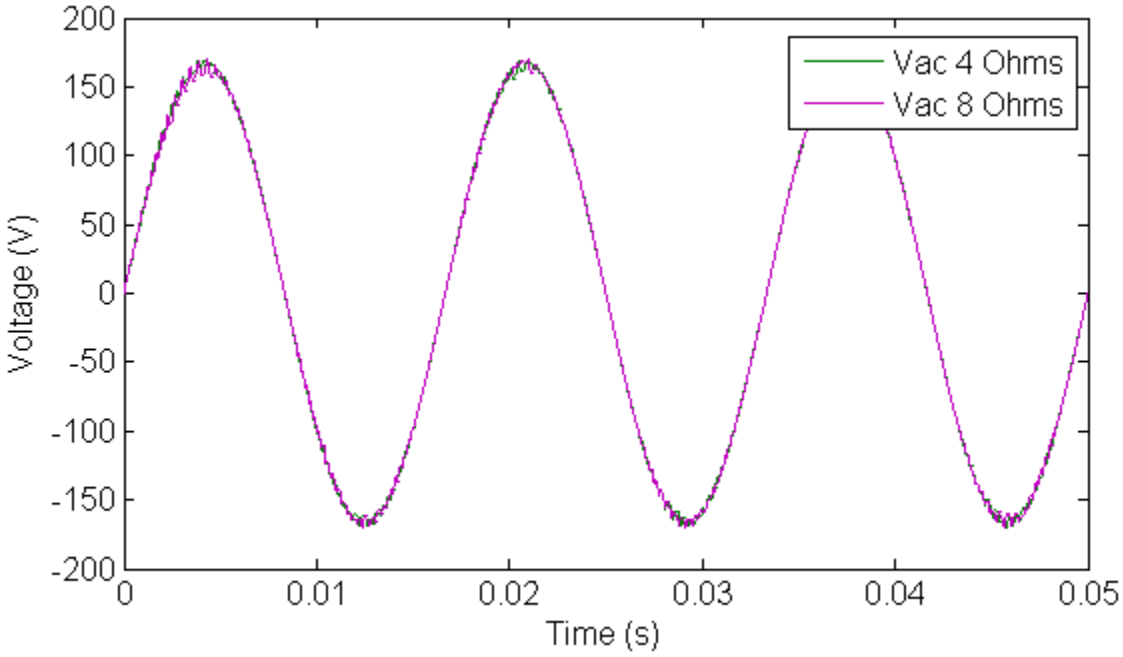

Figure 6.7: Discharging Mode Simulated AC Voltages

The AC voltage simulation performance exceeded expectations. Switching at 20 kHz resulted in a very good looking sinusoidal waveform. Both cases gave essentially the same output voltage, as expected from the PI controller. The experimental cases can be seen below in Figure 6.8.

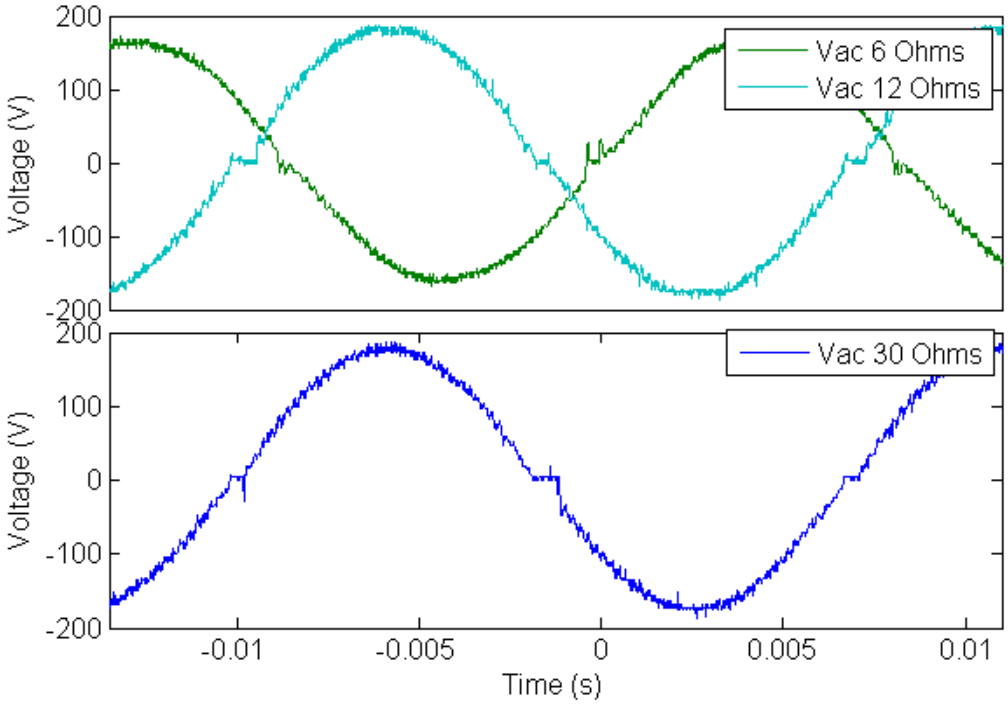

Figure 6.8: Discharging Mode Experimental AC Voltages

The experimental AC voltages look good as well. There is a little zero cross distortion – most likely from the triac, but other than that, the waveform looks very sinusoidal. The RMS voltage values all converge very close to 120 V_{AC}, as desired. The load value makes very little difference in the resulting voltage, which is expected. Figures 6.9 and 6.10 show the output currents in simulation and experimentation.

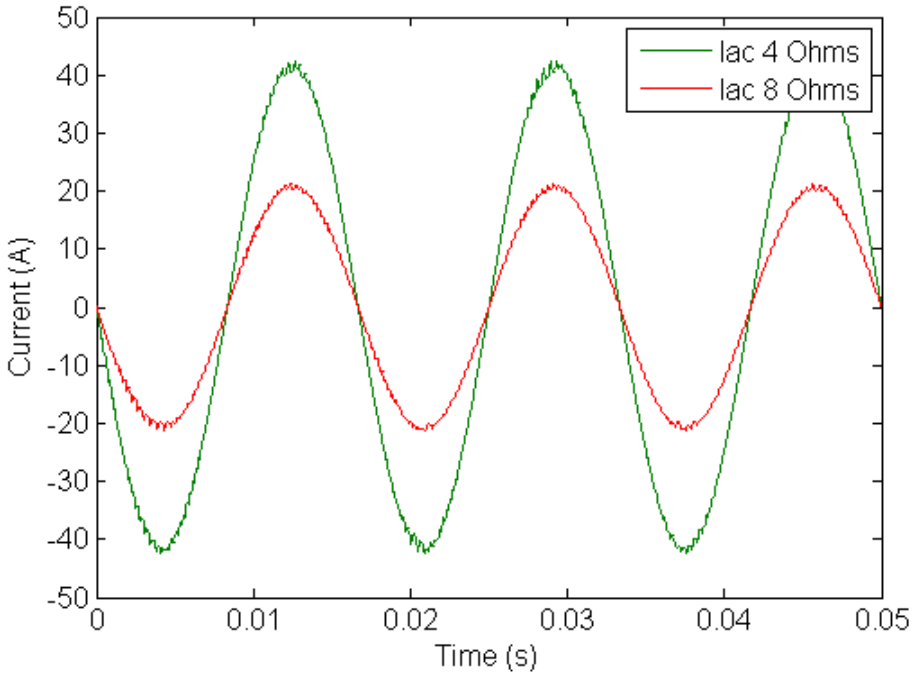

Figure 6.9: Discharging Mode Simulated AC Currents

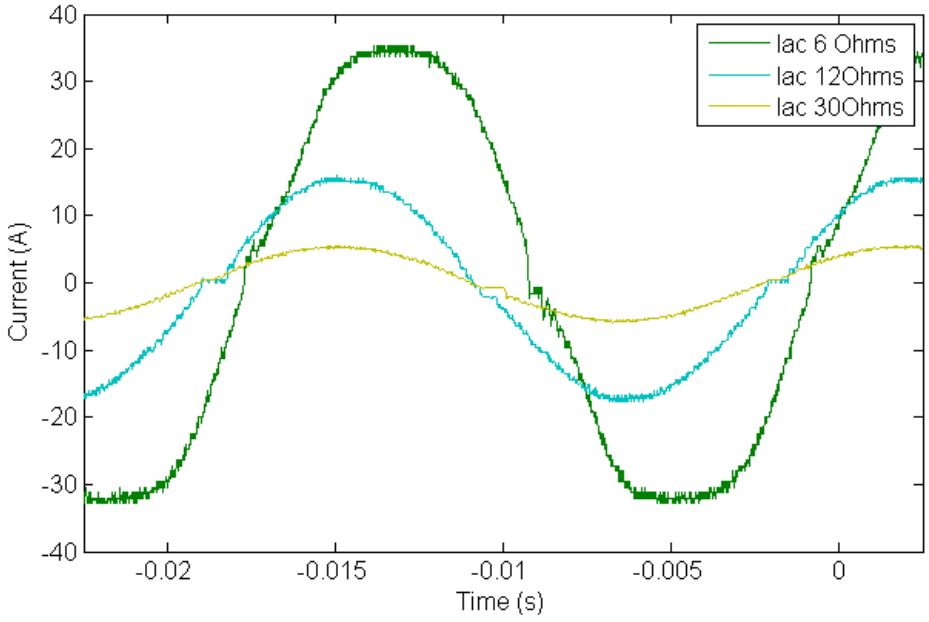

Figure 6.10: Discharging Mode Experimental AC Currents

Because the load is almost purely resistive, the currents and voltages look very similar. The experimental currents with the 12 Ω and 30 Ω loads look very much as expected. The 6 Ω load, however, has a flat spot at the peak of the waveform. This flat spot is somewhat hard to explain, considering the flat spot is only seen on the current, not the voltage. The likely explanation is that either the inductive filter is beginning to saturate or that the resistive load is heating and cooling unevenly throughout the cycle – resulting in a higher resistance near the peak and lower near the zero crossing (this effect can be seen in incandescent light bulbs). For the THD and voltage magnitudes, see Table 6.4, below.

	Experimental 6 Ω	Experimental 12 Ω	Experimental 30 Ω	Simulation 4 Ω	Simulation 30 Ω
THD_V	5.65%	4.95%	5.13%	1.2%	1.5%
THD_I	6.57%	4.81%	4.64%	1.2%	1.5%
V_{RMS}	114.14 V	127.5 V	123.3 V	117.8 V	117.7 V

Table 6.4: Discharging Mode THD and V_{AC} Magnitude

The THD values for the voltages and the currents for each case are all well within acceptable ranges. There is a small variation in the output magnitude of the AC voltage, however. Very small proportional and integral gains were used for the PI controller so changes would happen very slowly. A side effect of this, however, is that the microcontroller has some quantization errors when it assigns integer values to these updated values multiplied by these very small gains. It is likely that the quantization

error is causing the error to round to zero once it gets within some range, making the controller think it has reached steady state when it has not.

The discharging mode of the controller functions as expected, and meets all the requirements initially set for the AC/DC stage of the DIBPC in the discharging mode. Due to the limitations of the DC source used to test the DIBPC in the discharging mode, it could not be tested all the way to full load. Therefore some results are not known at this time. It is expected that the DIBPC would operate as expected at this load, but no tests have been performed to prove it.

Summary

This chapter presented the results for each experimental and simulated test that was performed on the DIBPC. Overall, the results look very promising. The DIBPC meets all the goals initially set forth in every mode of operation. The next chapter will discuss the conclusions that can be drawn from these results along with the pros and cons of this topology. The next chapter will discuss what further work is needed to improve the design of the DIBPC and stabilize its operation.

CHAPTER SEVEN

CONCLUSIONS AND SUGGESTIONS FOR CONTINUING STUDY

Conclusions

After reviewing the results of the DIBPC's AC/DC stage performance, some high points and low points were noted. In the charging mode, the DIBPC provided very good reduction in harmonic current, having a THD_I ranging from 7.4% - 13.35. The output voltage can be controlled as desired, easily providing the required input to the DC/DC stage of the DIBPC. In the discharging mode, the DIBPC provided a constant 120 V_{AC} output with a very low THD_I and THD_V in all loading situations.

One of the major reasons this topology was chosen was for flexibility in operation between 120 V_{AC} and 240 V_{AC} inputs in the charging mode. While most PFC rectifiers can operate over some range of voltages, including a range this large, there is often a large discrepancy in efficiency between the two. Despite efforts to improve the efficiency at 120 V_{AC}, a similar discrepancy can be seen in this topology. This topology is designed to incorporate a 6-pack of IGBTs, an assembly typically used in motor controllers. One drawback to the use of these readily available assemblies is their inherently low switching frequency capabilities. Using IGBTs that can switch faster would provide better performance and allow the use of significantly smaller inductors.

Another major reason this topology was chosen, especially as opposed to the basic bidirectional topology shown in Figure 1.10, was the ability to output both 120 V_{AC}

and 240 V_{AC} simultaneously in the discharging mode. While this feature is not currently implemented, this could still be a major advantage for this topology. This ability would allow the DIBPC to output twice as much power and to supply power to 240 V_{AC} appliances in the discharging mode.

While the DC/DC stage has not been built, the results presented in this thesis have provided ample evidence that the AC/DC stage is fully capable of successfully meeting the requirements set forth for the DIBPC. At this stage in the development, the results do not necessarily imply that this topology offers advantages over the basic bidirectional topology that would justify its additional expense. If the discharging mode was modified to operate such that it could output both 120 V_{AC} and 240 V_{AC} simultaneously, then this topology's advantages would be evident.

Suggestions for Continuing Study

While the AC/DC stage of the DIBPC met the requirements set forth for the design, some further research and development could significantly improve the operation of the DIBPC. First, some issues that have arisen during the testing need to be addressed. To optimize computational efficiency, most calculations internal to the microcontroller were performed as 16-bit integer operations. Upgrading the microcontroller to one that operates at 30+ MIPS, or even to a 32-bit microcontroller would provide several significant improvements for only a few dollars.

Some truncation that occurred as the results of integer operations limited the microcontroller's ability to react to small changes in measurements. Changing to double or floating point operations would improve those results significantly. Finding a microcontroller with more output compare outputs would also provide the ability to eliminate the optocoupler circuit, by simply having one output for every gate driver, rather than switching them externally.

Another improvement would be to more finely tune the gains. Tuning the gains such that the DIBPC operates optimally for every loading situation is a difficult process that takes a lot of time and patience. By making the duty cycle template gains a function of the DC voltage PI controller output, the microcontroller could optimally respond in every loading situation, resulting in a better looking waveform, even at very low load levels.

One aspect that was not studied in-depth was the fail-safe operation of the DIBPC. As was made painfully apparent during the experimental phases, small mistakes can result in the destruction of major hardware components. The DIBPC needs to incorporate more software and hardware protection which prevents damage to occur to these devices and to improve the overall safety and reliability of the device.

One way in which the safety could be improved is to make hardware changes in the gate drivers. Currently, the gate drivers are setup to invert the microcontrollers output to the IGBT gates. This creates an issue, however, if the power to the gate drivers turns off slower than the power to the microprocessor – resulting in a possible unexpected on state in the IGBTs. Another safety concern is if the toggle switches were switched during

the operation of the DIBPC. To eliminate this danger, the switches need to be disabled after the initial state of each is determined.

One other area of concern in the current state of the DIBPC is the potential for a step load change. If a step load change occurs, such as someone unplugging the DC output from the AC/DC stage during operation, the DIBPC needs to be able to safely cease operation without overcharging the capacitors. At the time, the only fail safe to prevent the overcharging of the capacitors is a software DC protection algorithm that temporarily outputs a zero duty cycle if the DC voltage is determined to be above a certain threshold in the charging state (450 V_{DC}).

One major drawback in the current stage of this design is the low efficiency. To improve the efficiency, several hardware changes could be made. A newer IGBT 6-pack can provide much lower losses during normal operation. A higher frequency 6-pack should be considered for better performance and to minimize the size of the inductors required. New inductors should also be used. Because the inductors used were made from donated high flux cores and manually wrapped insulated wires, their series resistance is very high. Inductor assemblies are available with resistances almost one hundred times smaller than the ones used. Optimized capacitors could also be used to reduce the losses in the ESR of the capacitors.

One upgrade that would provide more flexibility for the DIBPC would be the ability to output to 120 V_{AC} and 240 V_{AC} in the discharging mode. This would double the output power and provide more flexibility in terms of what appliances it could be used to power. The next logical step in the discharging mode would be to provide the

hardware and software upgrades to interface with the utility grid. This would require the DIBPC to synchronize with the frequency and phase angle of the power grid.

To further the design of the DIBPC, the DC/DC stage should be constructed. The DC/DC stage is necessary before the DIBPC can interface with the PHEV battery in either the charging or discharging modes. The construction of the DC/DC stage would complete the DIBPC and allow it to be tested and operated as originally envisioned.

In conclusion, the DIBPC AC/DC stage has been designed, constructed, and tested to effectively provide the desired AC to DC or DC to AC conversion to interface residential AC power to the battery DC power. The DIBPC charging mode has been shown to easily meet and exceed all harmonic standards domestically and internationally, and to meet the power transfer requirements to minimize charge time. The DIBPC discharging mode has been shown to provide a usable 120 V_{AC}, 60 Hz output from the DC input. The addition of the DC/DC stage will allow the interfacing of the AC/DC stage of the DIBPC to the battery, and permit the flow of power between 120 V_{AC} and the PHEV battery.

APPENDICES

Appendix A

Microcontroller Code

```
#include "p30f2020.h"
#include <math.h>
#include <dsp.h>

/* Configuration Bit Settings */
_FOSCSEL(FRC_PLL)
_FOSC(CSW_FSCM_OFF & FRC_HI_RANGE & OSC2_IO) //CLKO
_FPOR(PWRT_128)
_FGS(CODE_PROT_OFF)
_FBS(BSS_NO_FLASH)

void SetupDigital();
void SetupTimers();
void SetupAD();
void SetupOC();
void SetupPWM();
void SetupConstants();
void DCVoltageLoop();
void ACCurrentLoop();
void InverterSineLoop();
void InverterMagLoop();


/*Global Constants and user defined values*/
const double Kvp = .001;      //Voltage Proportional Gain Constant
const double Kvi = .005;      //Voltage Integral Gain Constant
const double Kvc = .005;      //Voltage Compensation Gain = Kvi / Kvp
const double Kip120 = .6;     //120V Current Proportional Gain
const double Kip240 = 1.5;    //240V Current Proportional Gain 1.5
const int Kdcmin = 0;
const int Kdcmax = 32000;
const int VPImax = 24576;
const double VPImin = 0;
const int Vdcdesnorm = 17000; //Desired DC voltage in volts, normalized
                              //by multiplying by .0025, then by 2^14
const int fswitch = 20;       //Switching Frequency in kHz

//Template = Ktemphi - Vac * Ktemplo
const int Ktemphi120 = 950;
const int Ktemplo120 = 400;
const int Ktemphi240 = 960;
const int Ktemplo240 = 1060;

const int SineTable[] =
{0,2508,5002,7466,9886,12249,14539,16745,18852,20848,22722,24463,26060,
27504,28787,29900,30839,31596,32168,32551,32743,32743,32551,32168,31596
,30839,29900,28787,27504,26060,24463,22722,20848,18852,16745,14539,1224
9,9886,7466,5002,2508};
```

```
const int Kinvmax = 10000;    //Maximum Inverter SineTable Gain can be
const int Kinvmin = 7500;     //Minimum Inverter SineTable Gain can be
const double Kinvp = .1;      //Inverter Proportional Gain
const double Kinvi = 0.01;    //Inverter Integral Gain

/* Global Initializations */
unsigned int j = 0, i = 0, l = 0, k = 0;
unsigned int Vpicount = 1;
int Iac = 0;
int Vac = 0;
int Vref = 0;
int Vdc = 0;
int dctemplate = 0;
int dcfinal = 0;
double Vacnorm = 0;
int Iacnorm = 0;
int Vdcnorm = 0;
int Idesired = 0;
int IPIout = 0;
int Kidesnorm = 0;
int Kiacnorm = 0;
double Kvacnorm = 0;
double Vpi = 0;
double Kip = 0;
int Vdcrefnorm = 150 * 41;  //Starting voltage for slow DC voltage rise
int VSum = 0;
int VExc = 0;
int VError = 0;
int VPIout = 0;
int VPIsat = 0;
int IError = 0;
int SineAngle = 0;
int InvDC = 0;
int PosHC = 0b0;
int VinvSUM = 9000;         //This will start the Integral gain at
about the right value;
int VinvACNorm = 0;
int VinvDes = 0;
int Vinverror = 0;
double VinvPIout = 0;
int VinvSum = 0;
double VinvPI = 0;
int slowrise = 0;
int Vold = 0;
int Von = 0;
int Ktemphi = 0;
int Ktemplo = 0;
```

```
int main(void)
{
      SetupDigital();
      SetupOC();
      SetupTimers();
      SetupPWM();
      SetupAD();
      while(1);
}


/*-----------------------------------------------------------------------*/
/*-------------AD Conversion complete interrupt handler--------------*/
/*-----------------------------------------------------------------------*/
void __attribute__ ((__interrupt__)) _ADCInterrupt(void)
{
      IFS0bits.ADIF = 0; /* Clear ADC Interrupt Flag*/

      Vref = ADCBUF1;
      Vdc = ADCBUF0;

      Iac = ADCBUF5;  /* Read the result of the second conversion */
      Vac = ADCBUF4;  /* Read the result of the second conversion */

      ADSTAT = 0;

      if (slowrise < 16000)   //Startup - Slowly increase DC voltage
      {
            if (Von < 3)
            {
                  if (Vac > 100)
                        Von++;  //Check if AC or DC voltages are on
                  else if (Vdc > 50)
                        Von++;
                  else
                        Von = 0;
            }
            else
            {
                  LATE = (PORTE | 0b0000000000010000);

                  if (PORTBbits.RB2 == 0b0)
                  {
                        //Output RE7 as 1 if in Inverter Mode
                        LATE = (PORTE | 0b0000000010000100);
                        //Output RE2 as 1
                        LATE = (PORTE & 0b1111111111111110);
                        //Output RE0 as 0
                  }
                  else
                        //Output RE7 as 0 if in PFC Mode
                        LATE = (PORTE & 0b1111111101111111);
```

```
                  if ((Vold > Vac) & (Vac > 120) & (Vold < (160 +
                  slowrise / 20)))
                        //Output RE4 as 0 for SCR slowrise
                        LATE = (PORTE & 0b1111111111101111);


                  Vold = Vac;
                  slowrise++;
                  if (slowrise > 15998)
                  {
                        LATE = (PORTE & 0b1111111111101111);
                        SetupConstants();
                  }
            }
      }

      else
      {
            if (PORTBbits.RB2 == 0b1)     //PFC Mode
            {
                  Vpicount--;
                  if (Vpicount == 0)      //Update at 20hz
                  {
                        Vpicount = 250;
                        DCVoltageLoop();
                  }
                  else
                  {
                        ACCurrentLoop();
                  }
            }

            else                          //Inverter Mode
            {
                  Vpicount--;
                  if (Vpicount == 0)
                  {
                        Vpicount = 250;
                        InverterMagLoop();
                  }
                  InverterSineLoop();
            }
      }
}
```

```
/*---------------------------------------------------------------------*/
/*---This is the DC Voltage Loop.  This should loop at about 20hz----*/
/*---------------------------------------------------------------------*/
void DCVoltageLoop(void)
{
      if (Vdcrefnorm < Vdcdesnorm)
      {
            Vdcrefnorm = (Vdcrefnorm + 123); //Raise Ref Voltage Slowly
      }
      Vdcnorm = Vdc * 24;     // Normalize the DC voltage to 0 - 2^14

      VError  = Vdcrefnorm - Vdcnorm;
      VPIout  = VSum + Kvp * VError;
      if(VPIout > VPImax)
            VPIsat = VPImax;
      else if(VPIout < VPImin)
            VPIsat = VPImin;
      else
            VPIsat = VPIout;

      VExc = VPIout - VPIsat;
      VSum = VSum + Kvi * VError - Kvc * VExc;

      Vpi = VPIsat * .000122;       // 1 / 2^14
}
```

```
/*---------------------------------------------------------------------*/
/*---This is the AC Current Loop.  This should loop at about 5khz----*/
/*---------------------------------------------------------------------*/
void ACCurrentLoop(void)
{
      // Normalize AC Voltage to pu for dctemplate .00294
      Vacnorm = Vac * Kvacnorm;
      // Normalize AC Current between 0 - 2^14
      Iacnorm = fabs(Iac - 515) * Kiacnorm;
      // Normalize Desired AC Current between 0 - 2^14
      Idesired = Vac * Vpi * Kidesnorm;
      IError = Idesired - Iacnorm;  // Calculate Current Error
      IPIout  = Kip * IError;       // Calculate Proportional Output
      if(IPIout > Kdcmax)
            IPIout = Kdcmax;        // Saturate Proportional Output

      // Calculate Current Control Template
      dctemplate = Ktemphi - Vacnorm * Ktemplo;
      dcfinal = (IPIout/33) + dctemplate; // Calculate Final Duty Cycle
      if (dcfinal < 0)
            dcfinal = 0;
      else if (dcfinal > Ktemphi)
            dcfinal = Ktemphi;      // Saturate Duty Cycle

      if (Vdc > 900)
            dcfinal = 0;      //Disable PWM if DC voltage is above 450V

      OC1RS = dcfinal;        //Output to OC1RS register for 120V&240V
      if (PORTBbits.RB3 == 0b1)
      {
            OC2RS = dcfinal;  //Output to OC2RS register for 240V
      }
}


/*---------------------------------------------------------------------*/
/*-----This is the Inverter Magnitude Loop.  Should loop at 20Hz-----*/
/*---------------------------------------------------------------------*/
void InverterMagLoop(void)
{
      VinvACNorm = Vac * 48;               //Normalize between 0 - 2^14
      VinvDes = SineTable[SineAngle] * .6; //Normalize between 0 - 2^14
      Vinverror = VinvDes - VinvACNorm;    //Calculate Voltage Error
      VinvPIout = VinvSum + Kinvp * Vinverror;//Calculate Updated Value
      if(VinvPIout > Kinvmax)
            VinvPIout = Kinvmax;           //Saturate Maximum
      else if(VinvPIout < Kinvmin)
            VinvPIout = Kinvmin;           //Saturate Minimum

      VinvSum = VinvSum + Kinvi * Vinverror; //Calc Integral Component
      VinvPI = VinvPIout / 10000;
}
```

```
/*---------------------------------------------------------------------*/
/*-------This is the Inverter Sine Loop.  Should loop at 5kHz--------*/
/*---------------------------------------------------------------------*/
void InverterSineLoop(void)
{
      SineAngle++;
      if (SineAngle >= 41) //41
      {                        //Zero Crossing Changes
            SineAngle = 0;
            PosHC ^= 0b1;
            IOCON1bits.OVRENH ^= 0b1;     //Toggle PWM Override 1
            IOCON2bits.OVRENH ^= 0b1;     //Toggle PWM Override 2
            LATE ^= 0b0000000000000101;   //Toggle Digital Out
      }
      InvDC = VinvPI * SineTable[SineAngle];    //VinvPI was .9
      PDC1 = InvDC;
      PDC2 = InvDC;
}


/*---------------------------------------------------------------------*/
/*--Setup Constants to Differentiate 120V & 240V PFC and INV Modes---*/
/*---------------------------------------------------------------------*/
void SetupConstants(void)
{
      if (PORTBbits.RB3 == 0b1)
      {
            Kidesnorm = 24;
            Kiacnorm = 45;
            Kvacnorm = .00147;
            Ktemphi = Ktemphi240;
            Ktemplo = Ktemplo240;
            Kip = Kip240;
      }
      else
      {
            Kidesnorm = 48;
            Kiacnorm = 89;
            Kvacnorm = .00294;
            Ktemphi = Ktemphi120;
            Ktemplo = Ktemplo120;
            Kip = Kip120;
      }
}
```

```
/*---------------------------------------------------------------------*/
/*-------------------------Setup PWM Module----------------------------*/
/*---------------------------------------------------------------------*/
void SetupPWM()
{
    /* ~~~~~~~~~~~~~~~~~~ PWM1 Configuration ~~~~~~~~~~~~~~~~~~~~~ */
    /* PWM1 I/O Control Register register */
      IOCON1bits.PENH = 1;    /*PWM1H is controlled by PWM module */
      IOCON1bits.OVRDAT = 0;  /*When Overriden, Select Low output */
      IOCON1bits.OVRENH = 0;  /*Initially, This PWM is not overriden */
      PWMCON1bits.IUE = 0b1;  /*Instant Update Enable */

    PDC1 = 0;                 /*Duty Cycle = PDC2*575nsec = 67.2nsec */
    DTR1 = 318;               /*Deadtime setting */
                              /*Deadtime = DTR1*575 = 67.2nsec */
    ALTDTR1 = 318;            /*Deadtime setting */
                              /*Deadtime = ALTDTR1*575 = 67.2nsec */


    /* ~~~~~~~~~~~~~~~~~~ PWM2 Configuration ~~~~~~~~~~~~~~~~~~~~~ */
    /* PWM2 I/O Control Register register */
      IOCON2bits.PENH = 1;    /* PWM2H is controlled by PWM module */
      IOCON2bits.OVRDAT = 0;  /* When Overriden, Select Low output */
      IOCON2bits.OVRENH = 1;  /* Initially, This PWM is overriden */
      PWMCON2bits.IUE = 0b1;  /* Instant Update Enable */

    PDC2 = 0;                 /* Duty Cycle = PDC2 * 1.575nsec */
    DTR2 = 318;               /* Deadtime setting */
                              /* Deadtime = DTR2*1.575 = 67.2nsec */
    ALTDTR2 = 318;            /* Deadtime setting */
                              /* Deadtime = ALTDTR2*1.575 = 67.2nsec */

 /* ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~ */

    /* Configure PTPER register to produce 20kHz PWM frequency */
      PTPER = 31746; /*PWM Period = PTPER*1.575nsec = 50usec = 20kHz */

    /* PWM Time Base Control Register */
      PTCONbits.EIPU = 1;
      PTCONbits.PTEN = 1;     /* Enable the PWM Module */
}
```

```
/*---------------------------------------------------------------------*/
/*-----------------------Setup the AD Converter------------------------*/
/*---------------------------------------------------------------------*/
void SetupAD(void)
{
      ADCONbits.ADSIDL = 0;         /* Operate in Idle Mode */
      ADCONbits.FORM = 0;           /* Output in Integer Format   */
      ADCONbits.EIE = 0;            /* Enable Early Interrupt */
      ADCONbits.ORDER = 0;          /* Even channel first */
      ADCONbits.SEQSAMP = 1;        /* Sequential Sampling Enabled */
      ADCONbits.ADCS = 0;           /* Clock Divider is Fadc/4 */

      ADPCFG = 0xFFCC;   /* AN0, AN1, AN4, AN5 are analog inputs*/
      ADSTAT = 0;                   /* Clear the ADSTAT register */
      ADCPC1bits.TRGSRC2 = 0xC;     /* Use timer trigger for AN4&AN5 */
      ADCPC0bits.TRGSRC0 = 0xC;     /* Use timer trigger for AN0&AN1 */
      ADCPC0bits.IRQEN0 = 1;        /* Enable the Interrupt */
      ADCPC1bits.IRQEN2 = 0;        /* Enable the Interrupt */
      ADCONbits.ADON = 1;           /* Start the ADC module */
}


/*---------------------------------------------------------------------*/
/*----Setup the Output Compare Module - only for use in PFC Mode-----*/
/*---------------------------------------------------------------------*/
void SetupOC(void)
{
      //120V and 240V Modes
      OC1CON = 0;
      OC1RS = 0x0000;   // This is the intial duty cycle
      OC1R = 0x0000;
      OC1CON = 0x2006;

      //240V Mode Only
      OC2CON = 0;
      OC2RS = 0x0000;   // This is the initial duty cycle
      OC2R = 0x0000;
      OC2CON = 0x2006;
}
```

```
/*---------------------------------------------------------------------*/
/*------Setup All Digital I/O and Change Notification Interrupt------*/
/*---------------------------------------------------------------------*/
void SetupDigital(void)
{
      LATE = (PORTE | 0b0000000000010000);
      TRISBbits.TRISB2 = 0b1; //Conf Port RB2 as Input (INV / PFC Mode)
      TRISBbits.TRISB3 = 0b1; //Conf Port RB3 as Input (120V/240V Mode)
      TRISEbits.TRISE0 = 0b0; //Conf Port RE0 as Output     (IGBTs)
      TRISEbits.TRISE2 = 0b0; //Conf Port RE2 as Output     (IGBTs)
      TRISEbits.TRISE6 = 0b1; //Conf Port RE6 as Input
      TRISEbits.TRISE7 = 0b0; //Conf Port RE7 as Output     (INV / PFC)
      TRISEbits.TRISE4 = 0b0; //Conf Port RE4 as Output     (SCR)

      CNEN1bits.CN4IE = 0b1; //Configure RB2/CN4 as Change Notification
      CNEN1bits.CN5IE = 0b1; //Configure RB3/CN5 as Change Notification
      IPC6bits.CNIP = 0b101; //Interrupt Priority Level 5
      IFS1bits.CNIF = 0b0;
      IEC1bits.CNIE = 0b1;
}


/*---------------------------------------------------------------------*/
/*-------------------Setup Timer for time runout---------------------*/
/*---------------------------------------------------------------------*/
void SetupTimers(void)
{
      T2CON = 0x0;
      TMR2 = 0x0;
      PR2 = 20000 / fswitch;
      T2CONbits.TCKPS = 0b00;       //1:1 prescale
      T2CONbits.TON = 0b1;

      T1CON = 0x0;
      PR1 = 4000;                   //5khz
      T1CONbits.TCKPS = 0b00;       //1:1 prescale
      //Wait so that it is between PWM Switching Off Cycles
      while(TMR2 > PR2 * .125);
      TMR1 = 0x0;
      T1CONbits.TON = 0b1;

      IFS0bits.ADIF = 0;      /* Clear AD Interrupt Flag*/
      IPC2bits.ADIP = 4;      /* Set ADC Interrupt Priority*/
      IEC0bits.ADIE = 1;      /* Enable the ADC Interrupt*/
}
```

```
/*-------------------------------------------------------------------*/
/*---------------Change Notification Interrupt Handler---------------*/
/*-------------------------------------------------------------------*/
void __attribute__ ((__interrupt__, no_auto_psv)) _CNInterrupt(void)
{
      IFS1bits.CNIF = 0b0;
      if (slowrise > 4000)
      {
      //    OC1RS = 0;
      //    OC2RS = 0;
      //    asm( "reset" );
      //    while(1);
      }
}

/*-------------------------------------------------------------------*/
/*----------------------Error Handling Routines----------------------*/
/*-------------------------------------------------------------------*/
//  Math Error Trap ISR

void __attribute__((__interrupt__ , auto_psv)) _MathError(void)
{
    INTCON1bits.MATHERR = 0;
}

//*******************************************************************//

//  Address Error Trap ISR

void __attribute__((__interrupt__ , auto_psv)) _AddressError(void)

{
    INTCON1bits.ADDRERR = 0;
}

//*******************************************************************//

//  Stack Error Trap ISR

void __attribute__((__interrupt__ , auto_psv)) _StackError(void)

{
    INTCON1bits.STKERR = 0;
}

//*******************************************************************//

//  Oscillator Failure Trap ISR

void __attribute__((__interrupt__ , auto_psv)) _OscillatorFail(void)

{
    INTCON1bits.OSCFAIL = 0;
}
```

Appendix B

Experimental Setup Pictures

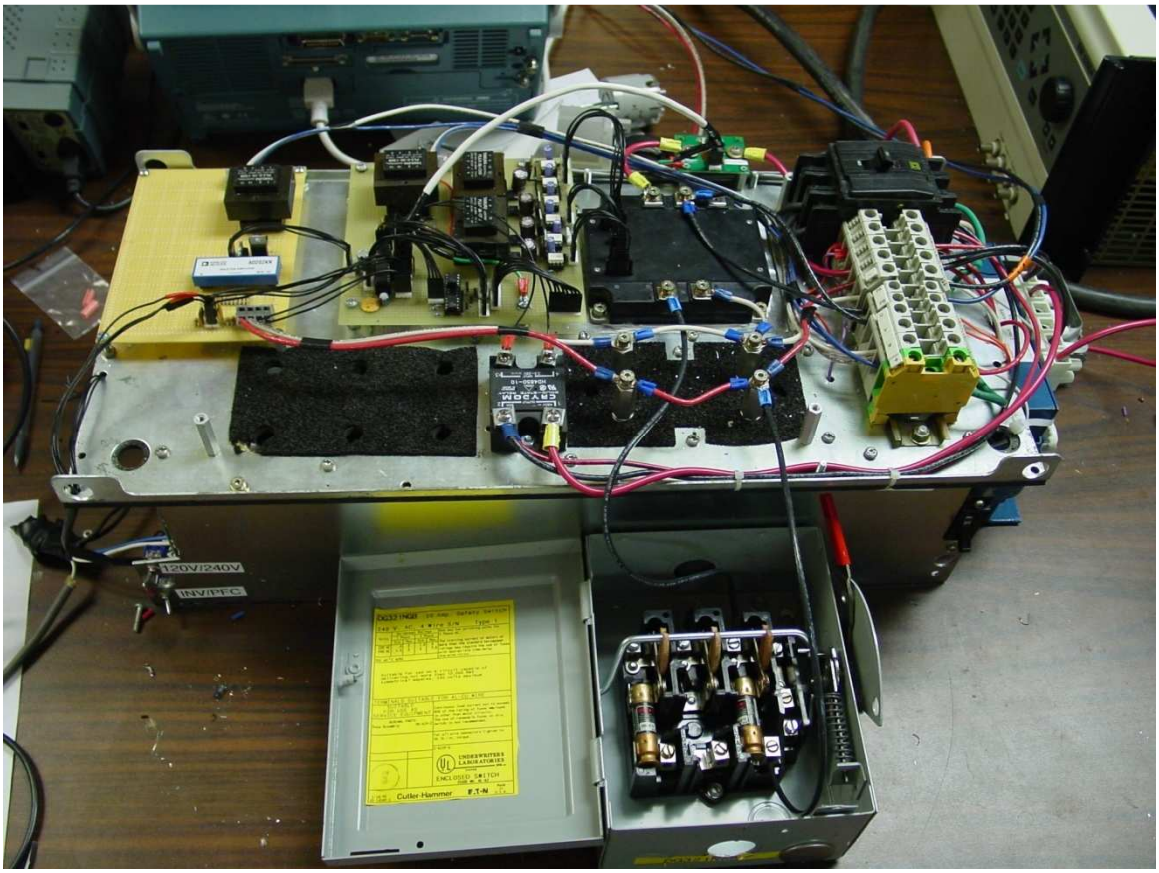

Figure B.1: Overview

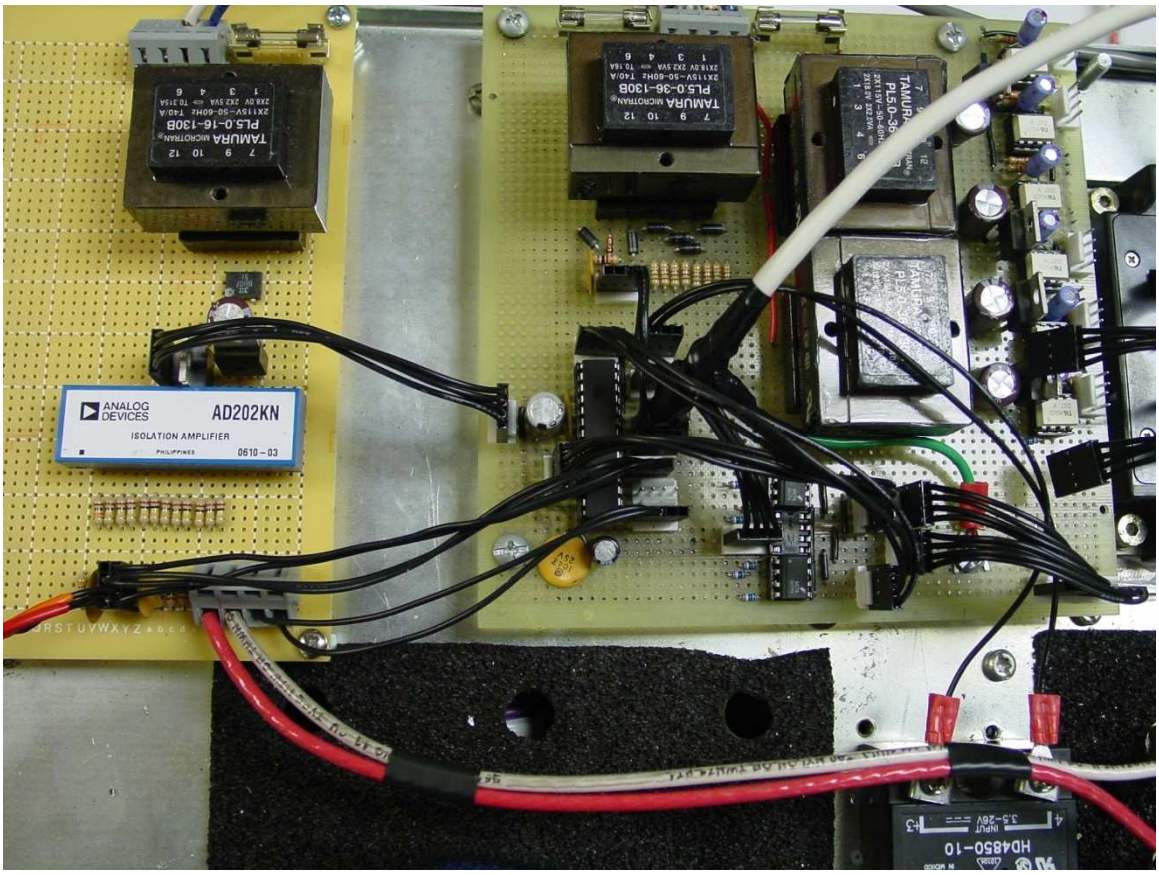

Figure B.2: Microcontroller, AC and DC Measurements

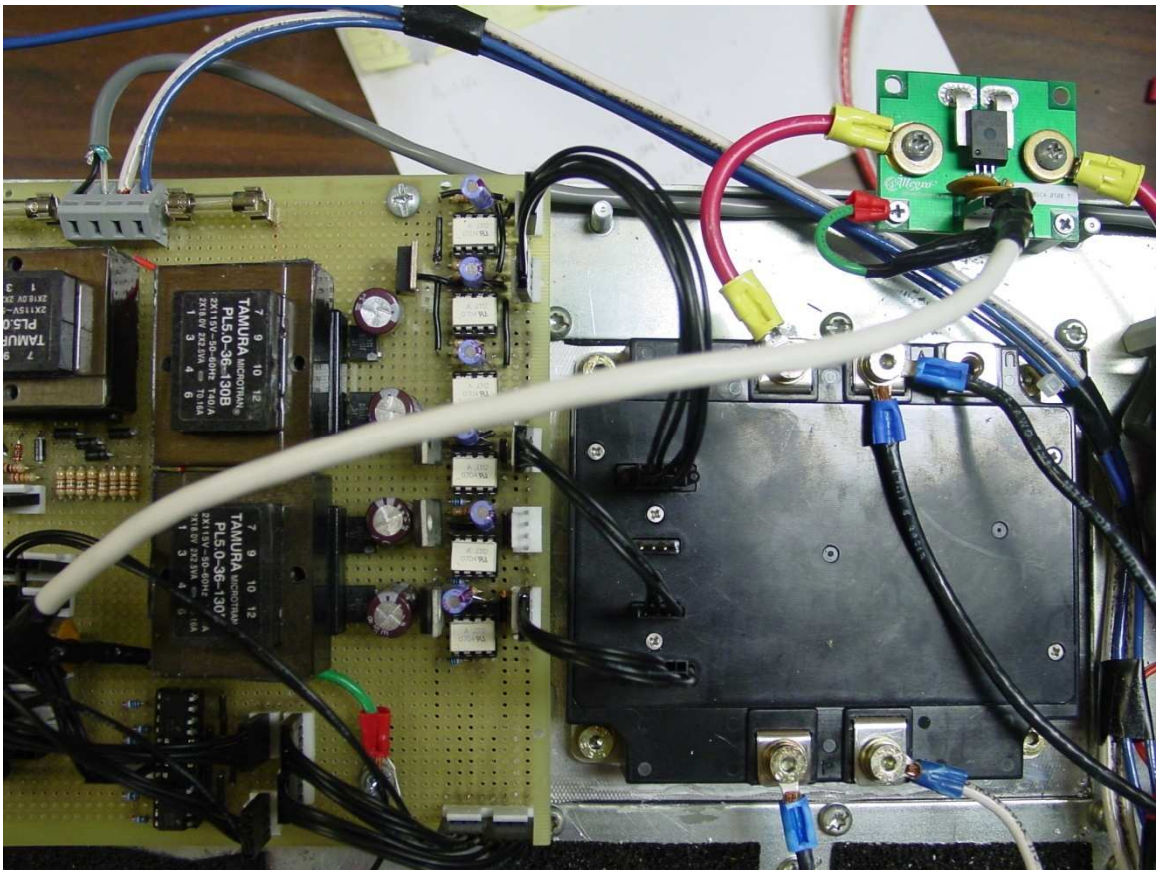

Figure B.3: Hall Effect Sensor, Gate Drivers and IGBT 6-pack

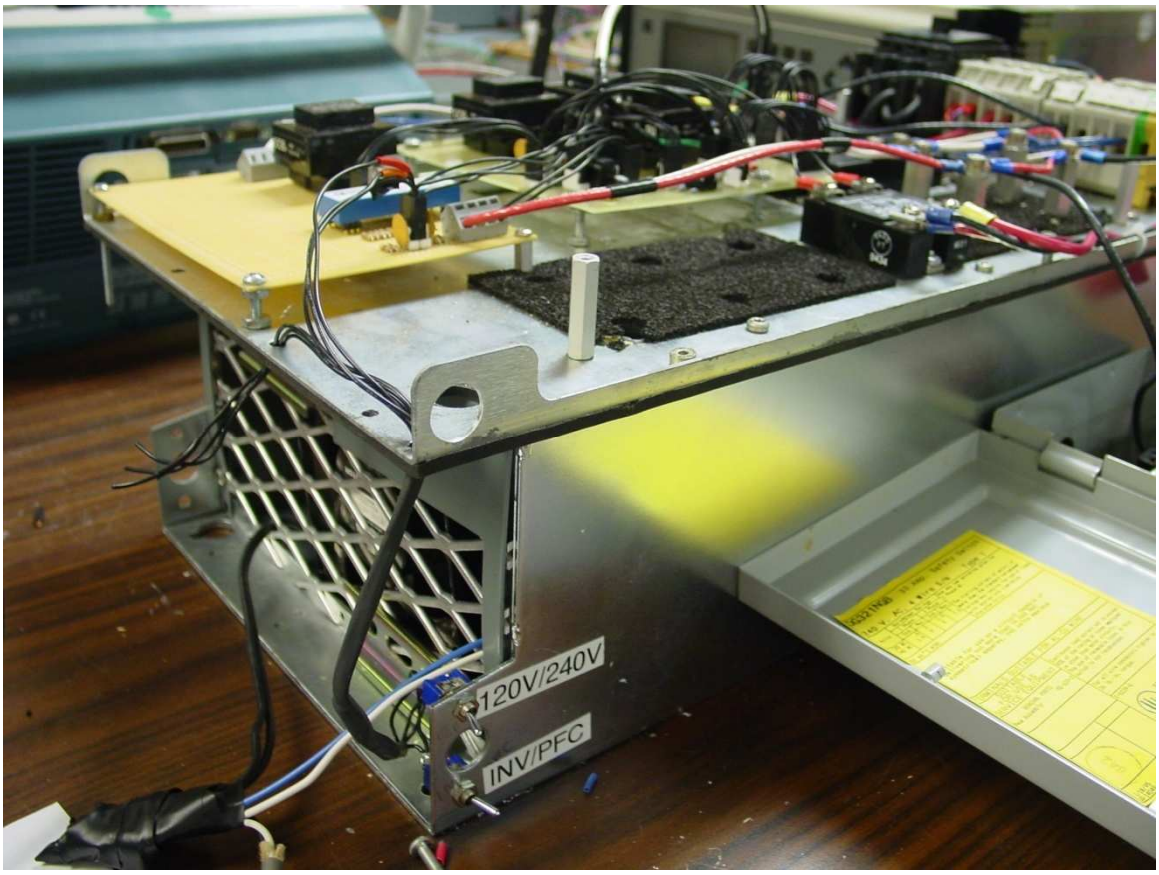

Figure B.4: Toggle Switches and Fan

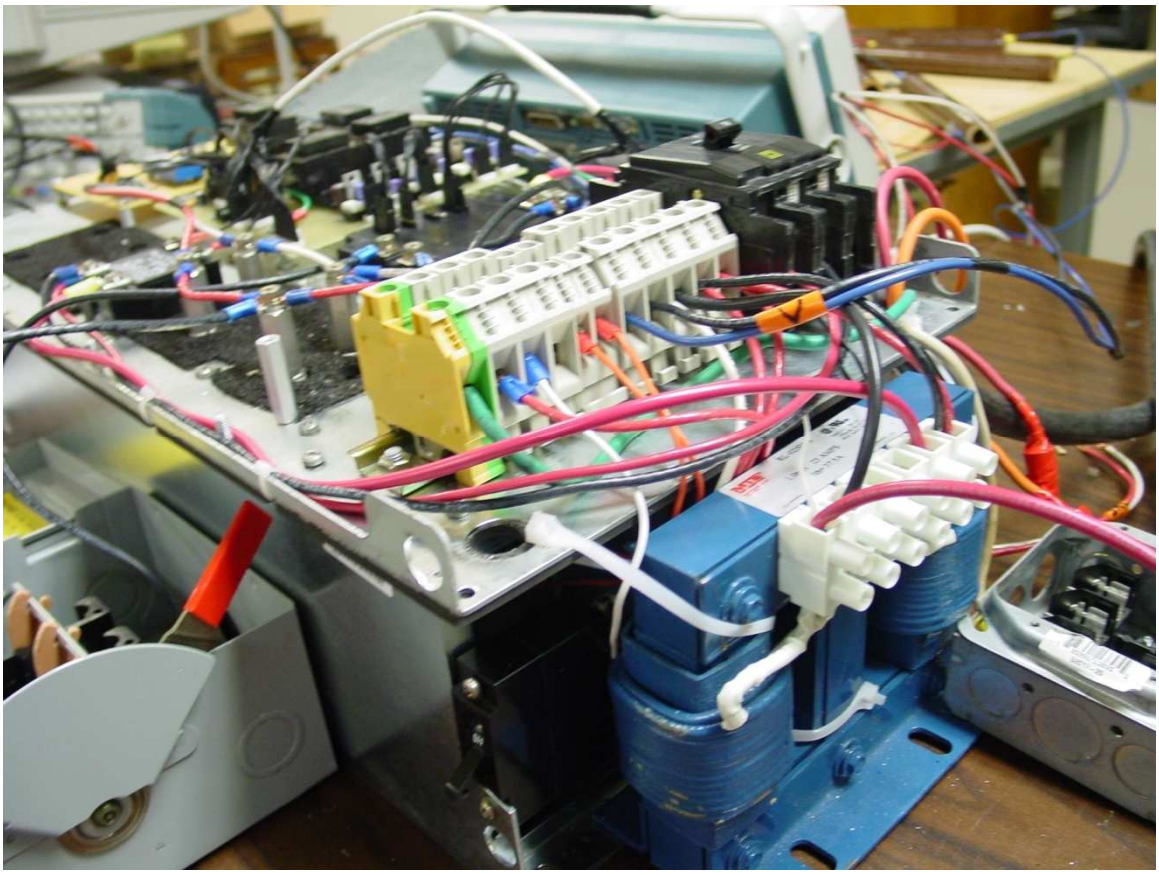

Figure B.5: Filter, Terminal Block and Breaker

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