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Circuit Modules for CMOS High-Power Short Pulse Generators

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CIRCUIT MODULES FOR CMOS HIGH-POWER SHORT PULSE GENERATORS

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ABSTRACT

High-power short electrical pulses are important for high-performance functionality integration, such as the development of microelectromechanical/nanoelectromechanical systems (MEMS/NEMS), system on chip (SoC) and lab on chip (LoC). Many of these applications need high-power (low impedance load) short electrical pulses, in addition to CMOS digital intelligence. Therefore, it is of great interest to develop new circuit techniques to generate high-power high-voltage short electrical pulses on-chip.

Results on pulse forming line (PFL) based CMOS pulse generator studies are reported. Through simulations, the effects of PFL length, switch speed and switch resistance on the output pulses are clarified. CMOS pulse generators are modeled and analyzed with on-chip transmission lines (TLs) as PFLs and CMOS transistors as switches. In the 0.13 μm CMOS process with a 500 μm long PFL, post layout simulations show that pulses of 10.4 ps width can be obtained. High-voltage and high-power outputs can be generated with other pulsed power circuits, such as Blumlein PFLs with stacked MOSFET switches. Thus, the PFL circuit significantly extends short and high-power pulse generation capabilities of CMOS technologies. A CMOS circuit with a 4 mm long PFL is implemented in the commercial 0.13 μm technology. Pulses of ~ 160 ps duration and 110-200 mV amplitude on a 50Ω load are obtained when the power supply is tuned from 1.2 V to 2.0 V. Measurement Instruments limitations are probably the main reasons for the discrepancies among measurement and simulation results.

A four-stage charge pump is presented as high voltage bias of the Blumlein PFLs pulse generator. Since Schottky diode has low forward drop voltage (~ 0.3V), using it as

charge transfer cell can have high charge pumping gain and avoid additional control circuit for switch. A four-stage charge pump with Schottky diode as charge transfer cell is implemented in a commercial 0.13 μm technology. Charge pump output and efficiency under different power supply voltages, load currents and clock frequencies are measured and presented. The maximum output voltage is ~ 6 V and the maximum efficiency is ~ 50%.

To my family

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I am extremely grateful to my advisor, Dr. Pingshan Wang, for his encouragement and support during my graduate study at Clemson. I would like to thank my group members. I appreciate my committee members for their help. At last, I would like to thank my family for the love that they have given me.

TABLE OF CONTENTS

Page

TITLE PAGE i

ABSTRACT ii

DEDICATION iv

ACKNOWLEDGMENTS v

LIST OF TABLES viii

LIST OF FIGURES ix

CHAPTER

I. INTRODUCTION 1

Motivation 1
Pulse Forming Line Based Pulse Generator 2
Charge Pump 3
Purpose of This Work 3
Thesis Organization 3

II. A 1.6V-6V CMOS CHARGE PUMP WITH SCHOTTKY DIODE AS CHARGE TRANSFER CELL 5

Introduction 5
Schottky Barrier Diode 6
Charge Pump Analysis and Design 7
Simulation and Measurement Results 11
Conclusion 12

III. SHORT PULSE GENERATION WITH ON-CHIP PULSE FORMING LINES 17

Introduction 17
A Pulse Forming Line Circuit and Switch Effects 17
Modeling and Analysis of the CMOS Pulse Forming Circuit 21
CMOS Implementation 41
Discussion and Conclusions 43

IV. SUMMARY AND FUTURE WORK 46

Summary 46
Future Work 47

BIBLIOGRAPHY 48

LIST OF TABLES

Table Page

3.1 Simulated and modeled parameters 37

LIST OF FIGURES

Figure Page

2.1 2 μm×4 μm Schottky diode 7

2.2 Schematic of four-stage charge pump 8

2.3 Micrograph of the charge pump 12

2.4 Output voltage V_O under different V_{dd} with 1MΩ//13pF load and different f_{CLK} 14

2.5 Measured output V_O and efficiency η under different V_{dd} with 2 μA I_O and 5 MHz f_{CLK} 15

2.6 Measured output V_O and efficiency η under different I_O with 1.2 V V_{dd} and 5 MHz f_{CLK} 15

2.7 Measured output V_O and efficiency η under different f_{CLK} with 1.2 V V_{dd} and 2 μA I_O 16

3.1 A schematic of the proposed short pulse generation circuit with an N-type MOSFET or BJT as the switch 18

3.2 Effects of time constant, τ, on switch voltage at node C, $V_C(t)$, and output voltages, $V_{out}(t)$ 22

3.3 Effects of different R_{ON} 23

3.4 Schematic of a CMOS short pulse generation circuit 24

3.5 Simplified schematic of the pulse generation circuit with parasitic capacitances 26

3.6 Simulated and modeled I_d-V_{ds} curves 26

3.7 Simulated, modeled and fitted V_g 31

3.8 Simulated drain voltages V_d with TL and without TL. 34

3.9 Simulated and modeled M3 drain voltage 34

List of Figures (Continued)

Figure Page

3.10 Proposed circuit implementation and simulation results 38

3.11 Output pulse width and amplitude vs. PFL length..... 39

3.12 Modeled and simulated output voltage..... 40

3.13 Blumlein PFL with cascade NMOS switch 42

3.14 Simulated output pulse of 5 mm Blumlein PFL 42

3.15 A micrograph of an on-chip pulse generator and measured output pulses with different V_{dd} 44

3.16 Frequency response of the cable, connector and probe 44

CHAPTER 1

INTRODUCTION

1.1 Motivation

Generating short electrical-pulses is important for high-performance functionality integration, such as the development of lab on chip, system on chip and microelectromechanical/nanoelectromechanical systems. Many of these efforts need high-power (low impedance load) high-voltage electrical pulses, in addition to CMOS digital intelligence. For instance, lab on chip has attracted a lot of recent interests since the development of microfluidics has enabled on-chip single cell handling capabilities [1]. Therefore, the integration of high-field short electrical pulses with microfluidics is intriguing since such pulses have unique biological effects and applications [2]-[5]. Because the dimensions of microfluidic channels can be controlled to that of a single cell, i.e. on the order of 10 μm, then a 1-10 V pulse can yield a field intensity of 1 kV/cm - 10 kV/cm. Such electrical pulses are high-voltage (i.e. higher than V_{dd}) and high-power (i.e. low impedance loads due to fluids in the channels) in standard digital CMOS technologies, where reliability issues (e.g. breakdown voltages and electromigration) are the limiting factors. Nevertheless, unlike off-chip cell studies [6]-[8], where kilovolt level or higher pulse generators are needed for similar sub-nanosecond electric fields, convenient experimental approaches, such as real-time microscope observations, can be

used in LoC to facilitate the study of electrical pulse biological effects. Therefore, developing new circuit techniques to generate high-power and high-voltage electrical pulses on-chip is of great interest for LoC development.

On the other hand, generating high-power electrical pulses with picosecond pulse duration on-chip is important for various applications, such as clocking high-speed analog-to-digital converters (ADC) [9], synthesizing ultra-wideband (UWB) signals for UWB communications [10], and developing inexpensive terahertz (THz) pulse technologies, which are currently dominated by electro-optic techniques [11], [12]. Due to device speed and parasitic effects, current on-chip short pulse generation circuits do not produce pulses (on a 50 Ω load) that are shorter than the fan-out-four (FO4) propagation delay of the given CMOS technologies. As a result, new techniques that can extend the high speed operation capabilities of standard CMOS devices and circuits are of great interest.

1.2 Pulse Forming Line Based Pulse Generator

Transmission line based pulse generation circuit [13], [14] is basic in conventional pulsed-power technologies to generate high-voltage and high-power short electrical pulses from low-voltage and low-power sources [15-17]. Yet, the circuits have not been studied for on-chip pulse generations, where transmission lines are available only recently as standard circuit components. Moreover, there is still a lack of quantitative studies on the effects of switch speed and switch resistance, which are the focus of this thesis.

1.3 Charge Pump

Charge pump is needed as high voltage bias for Blumlein PFL. Charge pumps are electronic circuits that generate voltages higher than the power supply voltage V_{dd} or lower than the ground voltage V_{gnd} of the process. Unlike the other traditional DC-DC converters, which employ inductors, charge pumps are only made of capacitors and switches (MOSFETs or diodes), thereby allowing integration on silicon [18], [19]. Charge pumps have been widely used in the nonvolatile memories, such as EEPROM or flash memories, to write or erase the floating-gate devices [20]. In addition, charge pumps can also be used in the low-supply-voltage switcher-capacitor systems that require high voltage to drive the analog switches [21].

1.4 Purpose of This Work

The purpose of this research is to analyze the output pulses quantitatively through modeling and simulations, and implement PFL pulse generator on-chip. Also, to bias Blumlein structure pulse generator, a high voltage CMOS charge pump is implemented and characterized.

1.5 Thesis Organization

In the next chapters, the realization of an on-chip PFL based pulse generator and a 1.6V-6V CMOS charge pump is described. Chapter 2 covers the four-stage charge pump with Schottky diode as charge transfer cell. In chapter 3, we report our results on pulse

forming line based CMOS pulse generator studies. Summary and future works are given in chapter 4.

CHAPTER 2

A 1.6V-6V CMOS CHARGE PUMP WITH SCHOTTKY DIODE AS CHARGE TRANSFER CELL

2.1 Introduction

The classical charge pump proposed by Dickson [22] uses a diode-connected MOSFET as charge transfer cell and it provides approximately an output voltage

$$V_o = (N+1)\cdot(V_{dd} - V_t) \tag{2.1}$$

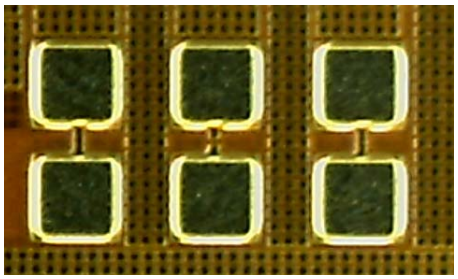
where N is the number of stages, and V_t is the threshold voltage of the diode-connected MOSFET. The main advantage provided by diodes is the absence of the switch control signals. The main disadvantage is the reduction of output voltage [19]. Indeed, when a diode is forward biased, i.e., when the corresponding switch is closed, it causes a voltage loss equal to the diode threshold voltage, V_t, which reduces the output voltage of a factor $(N+1)V_t$ [18], [19]. As the voltage is increased by charge pumping, the threshold voltage of the MOS transistors increases due to the body effect, the voltage gain of each stage is reduced and the overall efficiency decreases. In addition, since the threshold voltage cannot be scaled as much as the scaling trend of the supply voltage V_{dd}, the effect of the threshold voltage becomes more and more obvious as the technology scales down. It can

degrade charge pumping performance and is particularly critical under low power supplies [22].

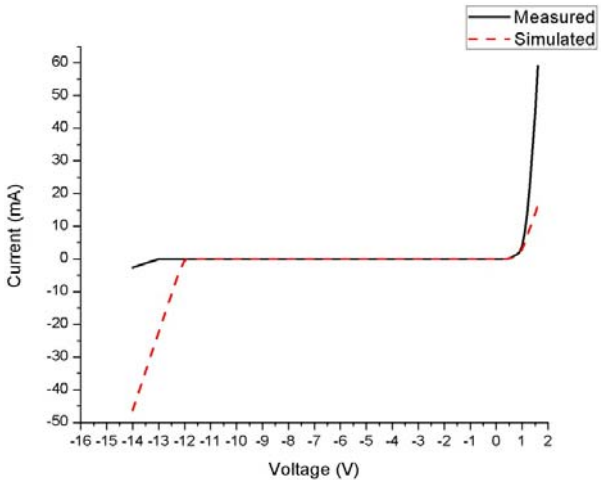
Therefore, several improvements were made to reduce the threshold voltage loss V_t [23]. To avoid the threshold voltage drop of the diode-connected transistors, additional MOSFET switches were used with the diodes. Then, the charge pump using only MOS switches was introduced to further increase the voltage gain [24]. However, for charge pumps with MOSFET as charge transfer cell, gate control signal is generated from additional circuit, which will consume larger area. For charge pumps with common diode as charge transfer cell, V_t is high (0.6-0.7V) which causes lower output voltage. Schottky diode has low threshold voltage (~ 0.3V), thus using it as charge transfer cell can have higher single-stage gain, also body effect is avoided and no additional control circuit is needed. In this paper, a charge pump is designed with Schottky diode as charge transfer cell.

2.2 Schottky Barrier Diode

A 2 μm×4 μm Schottky barrier diode (SBD) is implemented in IBM 0.13 μm CMOS technology. Its micrograph and *I-V* curves are shown in Fig. 2.1. The forward voltage of 2μm×4μm SBD is same with the value (0.3V) provided by IBM. The reverse breakdown voltage is about 13.1V, which much near the normal value 13.5V provided by IBM. But the forward current *I* is apparently larger than the simulated value when voltage reaches 1.0 V. The reason may be the process variation, considering that Schottky barrier diode has not qualified when we submitted its layout.



(a)



(b)

Fig.2.1. 2 μm×4 μm Schottky barrier diode (a) Micrograph (b) *I-V* curves.

2.3 Charge Pump Analysis and Design

2.3.1 Charge Pump Operation

We design a four-stage charge pump with Schottky diode as charge transfer cell, as shown in Fig. 2.2. Each stage includes a pumping capacitor *C* and a Schottky diode as switch. It needs a two-phase clock *CLK* and $\overline{CLK}$, one additional stage is also required to connect the output load to the final stage. Assume *CLK* is high in the first half clock

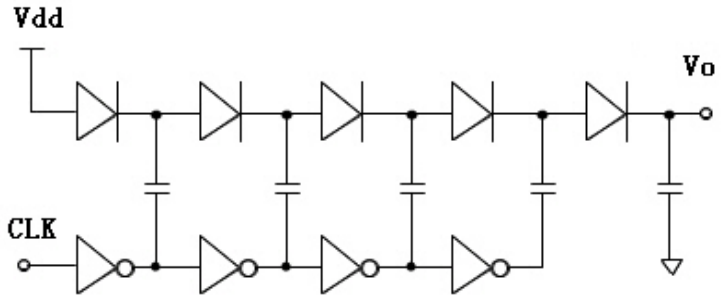


Fig. 2.2. Schematic of four-stage charge pump.

period of *CLK*, only the odd-stage switches are on. Thus the first pumping capacitor is charged to V_{dd} and all the even-stage pumping capacitors transfer the charge to the capacitor of next stage. In next half clock period, the signal *CLK* is low and only the even switches are on. All the even-stage capacitors receive the charge from the capacitor in the previous stage. The load capacitor is separated from the charge pump since the last switch is off [19].

2.3.2 Output Voltage

The output voltage V_O of the charge pump is

$$V_o = V_{in} + NV_{gain} - \frac{NI_o}{(C + C_{pt})f} \tag{2.2}$$

where V_{in} is the input voltage to the charge pump, V_{gain} is the voltage gain of each stage, N is the number of stages, I_o is the output current, C_{pt} is parasitic capacitances at the top layer of capacitor C, and f is the clock *CLK* frequency. The input voltage and the gain of each stage are reduced because of the threshold voltage and can be expressed as

$$V_{in} = V_{dd} - V_t \tag{2.3}$$

$$V_{gain} = \left(\frac{C}{C + C_{pt}} \right) V_{dd} - V_t \tag{2.4}$$

respectively. Due to its generality, (2.2) has been used as a model even for different topologies using MOS or diode switches and capacitors as the charge-pumping medium [24].

2.3.3 Current Consumption

The current consumption of the charge pump ideally depends only on the amount of the output current. However, the parasitic capacitances increase the current consumption of the charge pump [18], [19]. The extra current consumption includes the dynamic current to drive the parasitic capacitance at the top layer of the pumping capacitors and that at the bottom layer. Taking these parasitic effects into account, the current consumption of the charge pump is

$$I_{dd} = (N+1) I_o + N (I_{clk} + I_{st}) \tag{2.5}$$

where I_{clk} is the current to drive the bottom-layer parasitic capacitance C_{pb} and I_{st} is the current to drive the top-layer parasitic capacitance C_{pt}. They can be written as

$$I_{clk} = \beta C V_{dd} f \tag{2.6}$$

$$I_{st} = C_{pt} \Delta V_n f \tag{2.7}$$

where β is the ratio between the bottom-layer parasitic capacitance and the pumping capacitance C, which is technology dependent and varies between 0.1 (poly-poly capacitor) and 0.4 (other capacitors like metal-metal capacitor) [23]; ΔV_n is the voltage

swing across the pumping capacitor, which is same as V_{gain} in (2.4). Substituting (2.6) and (2.7) into (2.5), the current consumption becomes

$$I_{dd} = (N+1)I_o + N\left[\beta C V_{dd} f + C_{pt}\left(\frac{C}{C+C_{pt}}\right)V_{dd} f\right] \tag{2.8}$$

The current consumption is also a function of the pumping capacitance and the size of Schottky switch. As the bottom layer parasitic capacitance C_{pb} is generally more than one order of magnitude higher than C_{pt}, we can consider only C_{pb} to simplify the analysis. Therefore (2.8) becomes

$$I_{dd} = (N+1)I_o + N\beta C V_{dd} f \tag{2.9}$$

2.3.4 Efficiency

From [18], [19], a charge pump is considered based on pass-transistors or diode switches with threshold voltage V_t, and a simple expression for the power efficiency η is found, indicating the efficiency decrease caused by threshold voltage and the bottom plate parasitics of the pumping capacitors. Power efficiency can be written as:

$$\eta = \frac{I_o V_o}{I_{dd} V_{dd}} = \frac{K}{N+1+\beta\dfrac{N^2}{(N+1)(1-n_t)-K}} \tag{2.10}$$

where K is the multiplier factor

$$K = \frac{V_o}{V_{dd}} \tag{2.11}$$

and n_t is the ratio

$$n_t = \frac{V_t}{V_{dd}} \tag{2.12}$$

Notice that the parasitic capacitance C_{pt} in (2.2) is not considered in η derivation for simplification.

2.4 Simulation and Measurement Results

The four-stage charge pump in Fig. 2.2 is implemented in IBM 0.13 μm CMOS technology. Fig. 2.3 shows a micrograph of a fabricated charge pump. It occupies an area of ~ 250μm × 150μm. Output voltage and efficiency are measured with Tektronix DPO 7354 oscilloscope and Giga-tronic 8651A universal power meter.

2.4.1 Output Voltage and Efficiency under Different Source Supply V_{dd}

Output voltage measured with oscilloscope is shown in Fig. 2.4. The load is 1MΩ//13pF. Output voltage and efficiency on 2 μA load is shown Fig. 2.5. Output voltage is nearly linear with V_{dd}, which is predicted by (2.2). The maximum voltage is about 6V under 2 μA I_O and 15 MHz f_{CLK}. The efficiency is similar with the predication by (2.10) [18].

2.4.2 Output Voltage and Efficiency under Different Output Current I_o

From Fig. 2.6, output voltage V_O is pulled down by large load current I_O, as predicted by (2.2). Efficiency reaches maximum at I_O=3 μA. When I_O<3 μA, the ratio of inverters' power to total power is high, so efficiency is low. When I_O>3 μA, efficiency becomes lower with decreased output voltage.

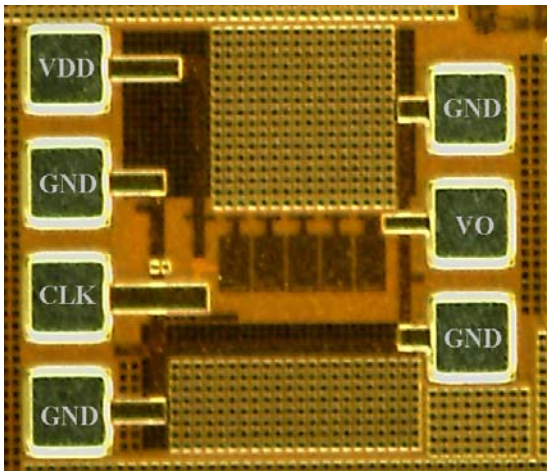


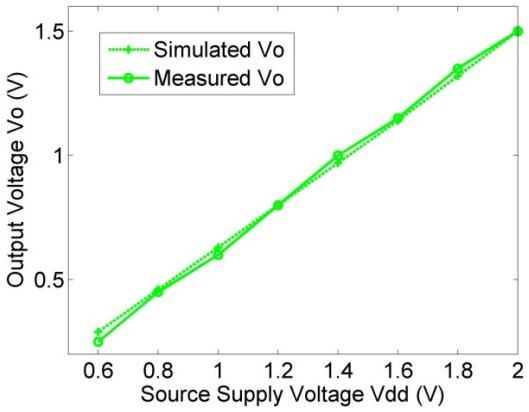
Fig. 2.3. Micrograph of the charge pump.

2.4.3 Output Voltage and Efficiency under Different CLK Frequency f_{CLK}

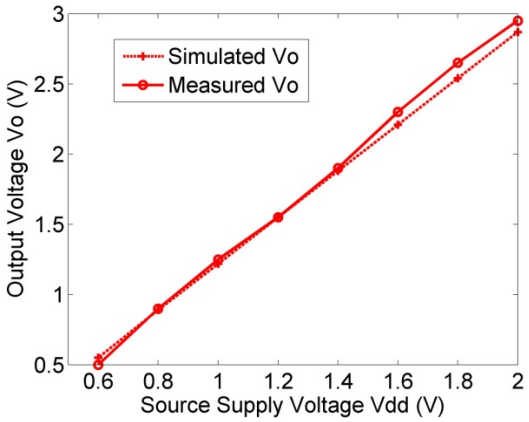
From Fig. 2.7, output voltage saturates and efficiency reach maximum at about f_{CLK}=5 MHz. Then output voltage enhances slowly and efficiency begins to decrease after f_{CLK}=5 MHz. The reason for efficiency decrease is that the inverters consume more dynamic power to pump capacitors at high frequency than low frequency.

2.5 Conclusion

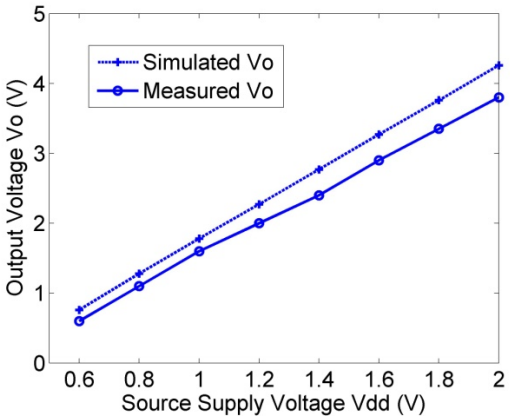
A four-stage charge pump with Schottky diode as charge transfer cell is proposed and implemented in IBM 0.13 μm technology. It occupies an area of ~ 250μm × 150μm. We measure and present charge pump performances under different power supply voltages, load currents and clock frequencies. The results show that the maximum output voltage is ~ 6V under 1.6 V V_{dd} and the maximum efficiency is ~ 50% under 3 μA load current.


Simulated Vo
Measured Vo
Output Voltage Vo (V)
Source Supply Voltage Vdd (V)
1.5
1
0.5
0.6
0.8
1
1.2
1.4
1.6
1.8
2

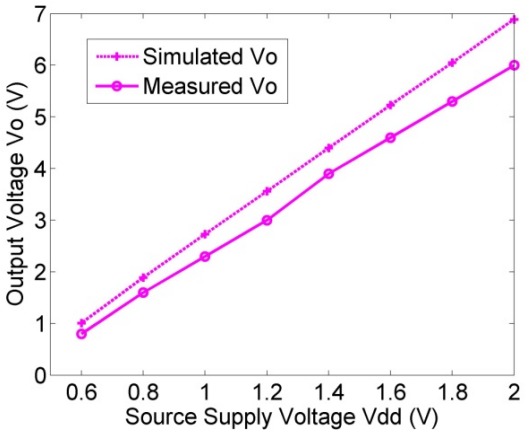
(a)


Simulated Vo
Measured Vo
Output Voltage Vo (V)
Source Supply Voltage Vdd (V)
3
2.5
2
1.5
1
0.5
0.6
0.8
1
1.2
1.4
1.6
1.8
2

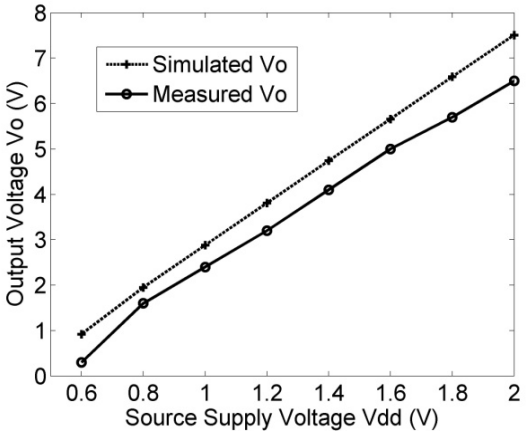
(b)


Simulated Vo
Measured Vo
Output Voltage Vo (V)
Source Supply Voltage Vdd (V)
5
4
3
2
1
0
0.6
0.8
1
1.2
1.4
1.6
1.8
2

(c)



(d)



(e)

Fig. 2.4 Output voltage V_O under different V_{dd} with 1MΩ//13pF load and f_{CLK} is (a) 200KHz (b) 500KHz (c) 1MHz (d) 5MHz (e) 15MHz.

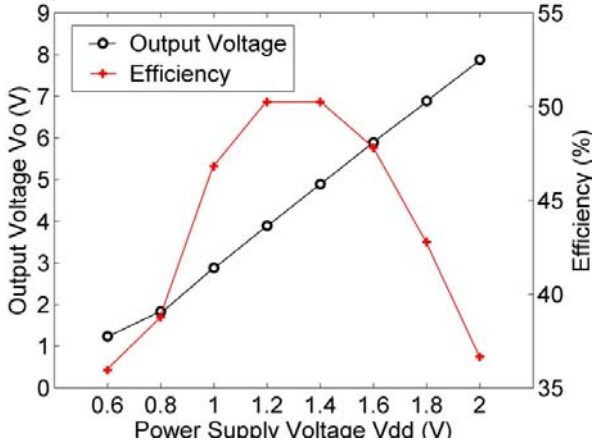


Fig. 2.5. Measured output V_O and efficiency η under different V_{dd} with 2 μA I_O and 5 MHz f_{CLK}.

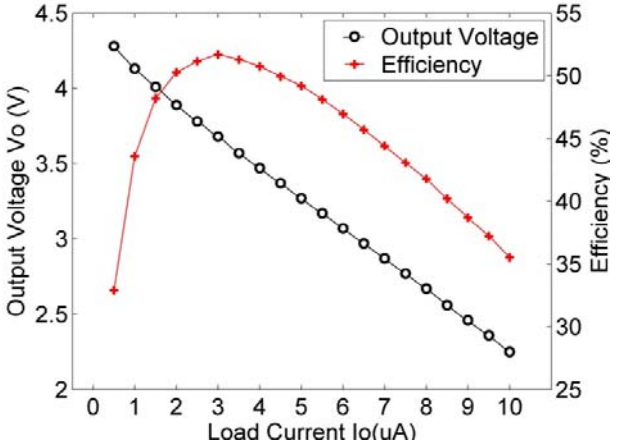


Fig. 2.6. Measured output V_O and efficiency η under different I_O with 1.2 V V_{dd} and 5 MHz f_{CLK}.

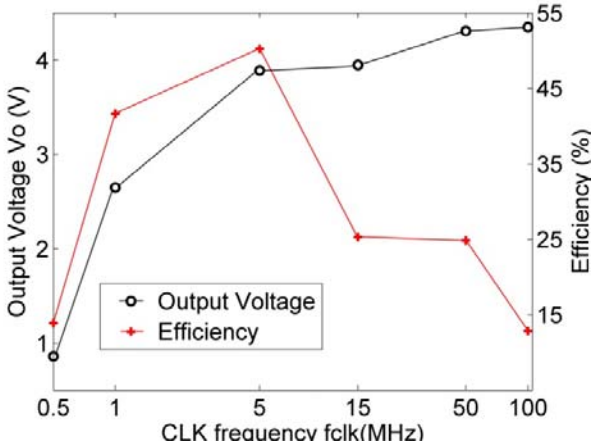


Fig. 2.7. Measured output V_O and efficiency η under different f_{CLK} with 1.2 V V_{dd} and 2 μA I_O.

CHAPTER 3

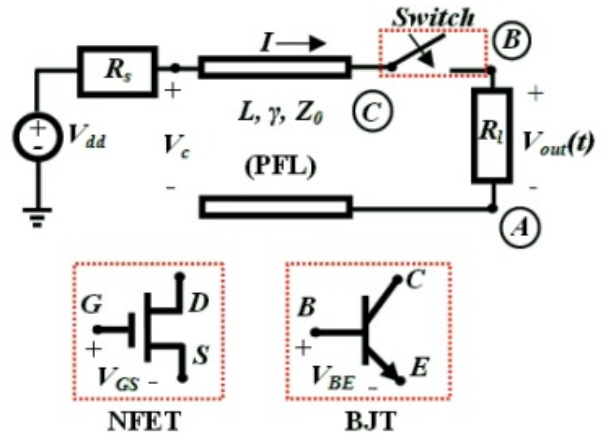
SHORT PULSE GENERATION WITH ON-CHIP PULSE FORMING LINES

3.1 Introduction

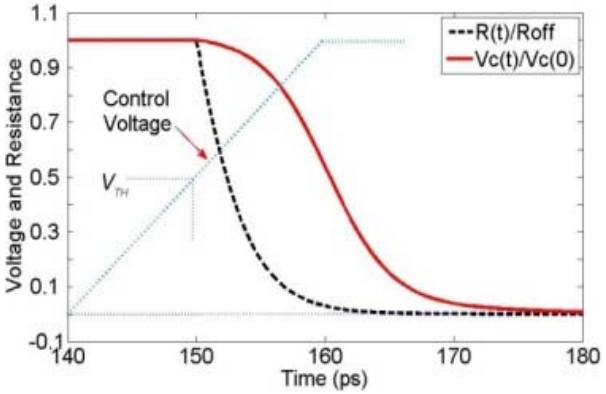
In this chapter we propose pulse forming line based CMOS circuits for high-power, high voltage short pulse generation on-chip [13], [14]. Then we analyze and model the PFL based CMOS short pulse generation circuits, and present the experimental measurement results. The rest of the chapter is arranged as the following: section 3.2 discusses the operation of a basic PFL based circuit with a focus on switch effects; section 3.3 presents detailed modeling and analysis of CMOS PFL circuit; section 3.4 is a CMOS implementation of the proposed circuit; section 3.5 is discussion and conclusions.

3.2 A Pulse Forming Line Circuit and Switch Effects

Fig. 3.1(a) shows the schematic of a basic transmission line based pulse generation circuit [13], [14]. It has two main components: a pulse forming line and a switch. The PFL has a length of L, signal propagation constant γ and characteristic impedance Z_0. Node B or A can be grounded. It operates as the following: after the PFL is slowly charged to



(a)



(b)

Fig. 3.1. (a) A schematic of the proposed short pulse generation circuit with an N-type MOSFET or BJT as the switch. (b) Normalized resistance and voltage across a PN junction switch when node B is grounded. The control voltage has a threshold voltage V_{TH}, after which the resistance model does not depend on the control voltage.

voltage V_{dd}, the switch closes. An output pulse, $V_{out}(t)$, is then formed with amplitude of ~ $V_{dd}/2$ and a pulse duration of $\tau_p \approx 2L/v$, where L is the PFL length, and v is the local speed of light. The switch determines the rise edge of the generated pulse, while the length of the PFL, not the switch, determines when the pulse ends. The circuit is basic in conventional

pulsed-power technologies to generate high-voltage and high-power short electrical pulses from low-voltage and low-power sources [15-17]. Yet, the circuits have not been studied for on-chip pulse generations, where transmission lines are available only recently as standard circuit components. Moreover, there is still a lack of quantitative studies on the effects of switch speed and switch resistance, which are the focus of this chapter.

The PFL in Fig. 3.1(a) is an on-chip TL, which has a few limitations. It is well known that CMOS TLs are lossy and dispersive due to limited metal thickness, dielectric layer thickness and lossy substrates. Nevertheless, the loss and dispersion of CMOS TLs are not major issues for the circuit in Fig. 3.1(a) since only relatively short TLs are needed. CMOS chips have size limitations, which limit straight TL lengths. Yet the performance of meandered TL is similar to that of straight ones [25]. Therefore, chip size is not a major concern for longer pulse generation on-chip.

The switch in Fig. 3.1 (a) is a critical component, which can be a MOSFET. Bipolar junction transistors (BJTs) can also be used when BiCMOS is considered. To investigate the applicability of these transistors in Fig. 3.1 (a), we need to understand how their switching speed and on/off resistance affect the pulse formation processes. Thus, we assume a trapezoid voltage with linear rise-edge for switch control. Such a voltage pulse can be generated on-chip and applied to V_{GS} or V_{BE} in Fig. 3.1 (a). Once the control voltages pass a threshold voltage, V_{TH}, we expect the switching resistances are $R_{DS}(t) \propto 1/t$ for a deep-submicron MOSFET and $R_{CE}(t) \propto e^{-\eta t}$ for a BJT (η is a coefficient). Then the approximate resistance models can be used to study MOSFET and BJT switches. In the following simulation analysis, however, we model the switch (time-dependent) resistance

with $R(t) = R_{on} \Big/ \left[\left(1 + e^{-\xi(t-\tau)}\right)^{-1} + R_{on}/R_{off} \right]$ [26], where R_{on} and R_{off} are the on and off resistance, respectively; τ is the time constant of the switching process and ξ is a coefficient related to the switch transition time. This model was proposed to describe the time dependent switching resistance of a PN junction under avalanche breakdown. The reasons for using this model, instead of a MOSFET or BJT resistance model, are (i) reverse biased PN junctions have been used to form extremely short electrical pulses [27], (ii) avalanche breakdown is the basic process in oil, gas and water switches in a conventional pulsed power system, and (iii) a different model, such as $R(t) \propto 1/t$, leads to similar conclusions. Therefore, the obtained results serve not only the design guidelines for the proposed CMOS short pulse generation circuits, but also help clarify the pulse forming processes in conventional pulsed power systems.

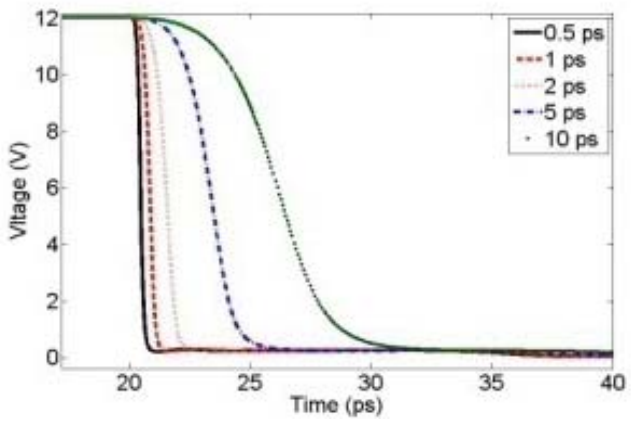
A macro switch model with our chosen resistance *R(t)* is used in circuit simulation analysis with Cadence Spectre. The used parameters are τ=20 ps, R_{on}=2 Ω, R_{off}=20000 Ω and ξ=*8*. All other circuit components, a 1 mm long 50 Ω transmission line, a 50 Ω load resistor, and a 1.5 kΩ charging resistor, are standard devices from IBM 0.13 μm 8RF CMOS technology. Fig. 3.1 (b) shows voltage $V_C(t)$ and resistance *R(t)*. It is clear that the switch voltage begins to drop quickly only after the switch resistance drops to a level close to the load resistance due to a voltage division between the switch resistance and the load R_l, which is much smaller than R_{off}. As a result, the effective switching time is much shorter than τ. Therefore, output pulses faster than the switching device speed can be obtained.

Fig. 3.2 shows the effects of different switching times τ on switch voltages $V_C(t)$ and output voltages $V_{out}(t)$. A $V_{dd}=12\ V$ is assumed for the presumed PN junction switch. Fig. 3.3 shows the effects of different R_{on}. The results indicate that (i) picosecond output pulses can be generated with relatively slow switches, (ii) the faster the switches, the sharper the output pulse edges, (iii) the smaller the ON resistances, the higher the output voltages. Thus MOSFETs and BJTs can be used as switches to generate picosecond pulses, albeit with V_{dd} determined by the given technologies. Thus, the circuit in Fig. 3.1(a) shows a great promise to significantly expand the short pulse generation capabilities of conventional digital circuits.

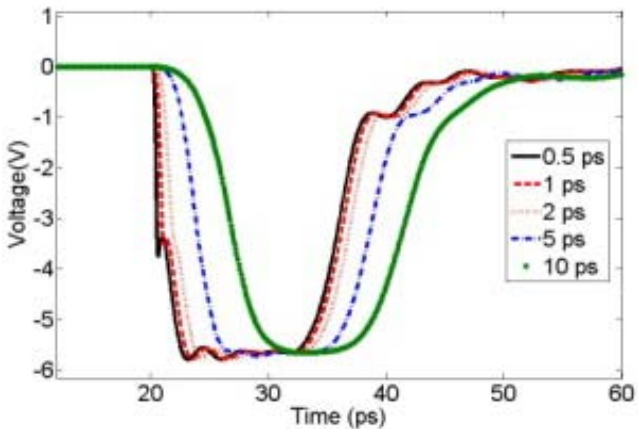
The PFL in Fig. 3.1(a) has 50-200 Ω impedance, which is low compared with the impedance values in digital circuits. The PFL can also be charged to voltages much higher than the breakdown voltages of individual CMOS transistors since PFLs use interconnect resources. Therefore, high-voltage high-power electrical pulses can be obtained as long as the reliability of the switch is not a problem. At the end of section 3.3, we show a Blumlein PFL with stacked transistor switch to generate pulses with voltages higher than V_{dd} on 140 Ω loads.

3.3 Modeling and Analysis of the CMOS Pulse Forming Circuit

Fig. 3.4 shows the short pulse generation circuit with an NMOS switch. A fast rise edge of its trigger signal (i.e. V_{GS}) is essential. Therefore, the usually slow rise-edge of an external trigger signal, V_{in}, needs to be sharpened. A Schmitt trigger or short pulse

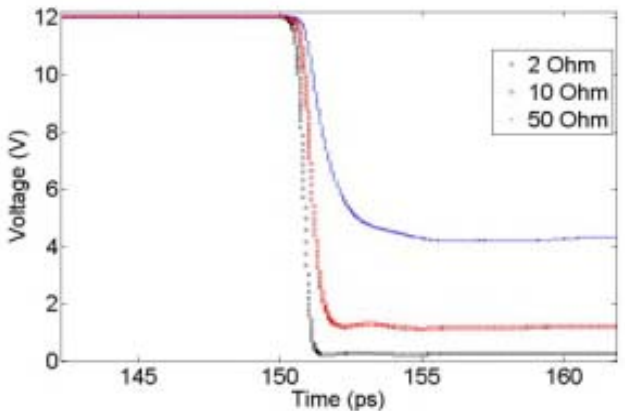


(a)

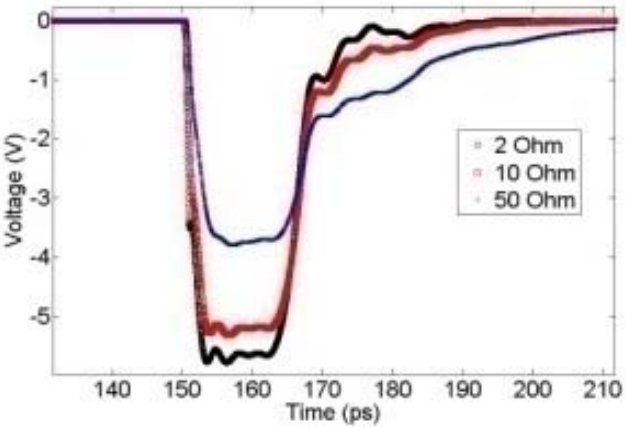


(b)

Fig. 3.2. Effects of time constant, τ, on (a) switch voltage at node C, $V_C(t)$, and (b) output voltages, $V_{out}(t)$. In the simulation, the switch model and parameters used for Fig. 3.1(b) are used.

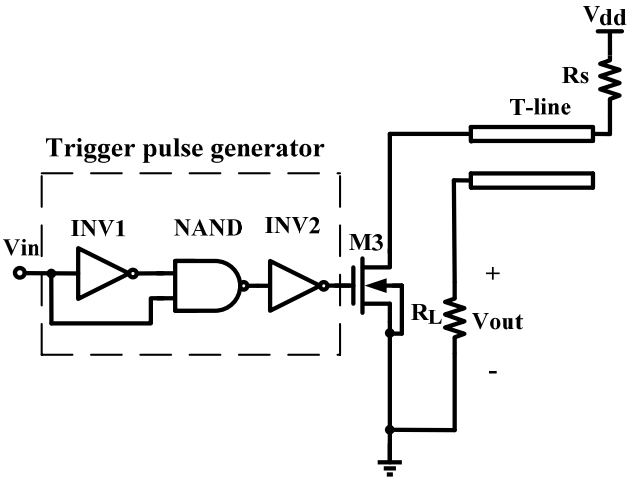


(a)

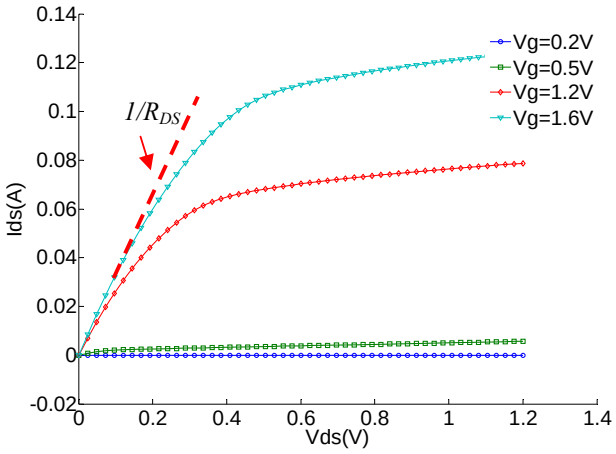


(b)

Fig. 3.3. Effects of different R_{on}. (a) Switch voltage $V_C(t)$. (b) Output voltage $V_{out}(t)$. In this simulation, $\tau=2$ ps. The rest of the circuit components are the same as those for Fig. 3.2.



(a)



(b)

Fig. 3.4. (a) Schematic of a CMOS short pulse generation circuit. (b) The I_{ds}-V_{ds} characteristics of the NMOS in (a). R_{DS} is the equivalent drain-source resistance

generator [28] can be employed for this purpose. Since the fall edge of V_{GS} is not critical, the obtained rise-time can be tuned much shorter than the gate propagation delay of an inverter. Nevertheless, we need large V_{GS} to drive the MOSFET switch into triode region so the NMOS is equivalent to a small resistor, as illustrated in Fig. 3.4 (b). The size of the

NMOS and V_{GS} shall be chosen so that R_{DS} is small. Hence, the amplitude and width of the output pulse, $V_{out}(t)$, are mainly determined by V_{dd} and transmission line length, respectively.

3.3.1 Modeling of the PFL Based Pulse Generation Circuit

To model the circuit in Fig. 3.4(a), we start from the inverter INV2 of the trigger pulse generator since conventional digital circuit techniques are used for INV1 and NAND. The simplified circuit is shown in Fig. 3.5, which includes the MOSFET parasitic capacitances.

We use α-power law [29-31] to model the MOSFETs in Fig. 3.5. The *I-V* equations are

$$I_{ds} = I_{dsat}\left(2 - \frac{V_{ds}}{V_{dsat}}\right)\frac{V_{ds}}{V_{dsat}} \qquad \text{triode region} \quad (3.1\text{-a})$$

$$I_{ds} = I_{ds0}\left(\frac{V_{gs} - V_{th}}{V_{dd} - V_{th}}\right)^{\alpha} + 2\left(I_{ds0} - I'_{ds0}\right)\left(\frac{V_{gs} - V_{th}}{V_{dd} - V_{th}}\right)^{\alpha}\frac{V_{ds} - V_{dd}}{V_{dd}} \qquad \text{saturation region} \quad (3.1\text{-b})$$

where I_{ds0} is drain-source current when $V_{gs}=V_{ds}=V_{dd}$, I'_{ds0} is drain-source current when $V_{gs}=2V_{ds}=V_{dd}$, α is velocity saturation index and closely related to the velocity saturation of carriers [29-31]. Parameter α can be obtained through data fitting from process model file or measured *I-V* data. α is 1.5 and 1.3 for PMOS and NMOS in IBM 0.13 μm CMOS process, respectively. The simulated and modeled I_d-V_{ds} curves of M2 and M3, shown in Figs. 3.6 (a) and (b), respectively, show that (1) describes MOSFET operations reasonably well.

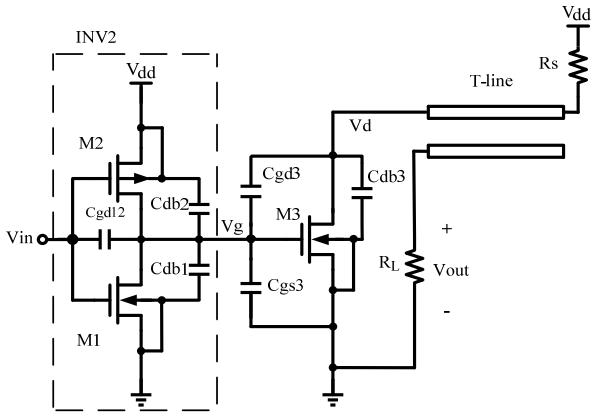
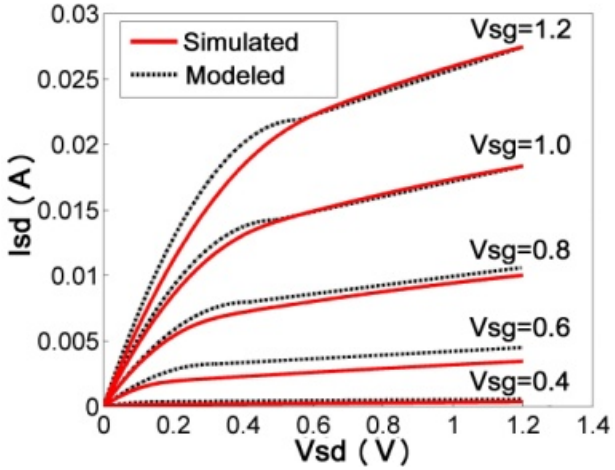
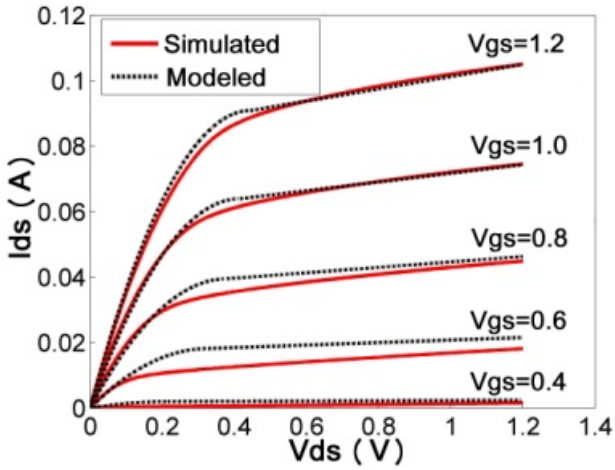


Fig. 3.5. Simplified schematic of the pulse generation circuit with parasitic capacitances.



(a)



(b)

Fig. 3.6. Simulated and modeled I_d-V_{ds} curves of (a) PMOS M2 and (b) NMOS M3.

3.3.1.1 Trigger Pulse Generator

The dynamic behavior of INV2 with load M3 is described by:

$$C\frac{dV_g}{dt} = C_{gd12}\frac{dV_{in}}{dt} + I_{sd2} - I_{ds1} \tag{3.2}$$

where C=C_{gd12}+C_{db1}+C_{db2}+C'_{gd3}+C_{gb3}+C_{gs3}, C_{gd12}=C_{gd1}+C_{gd2}, C_{gd1} and C_{gd2} are gate to drain capacitances of M1 and M2, respectively; C'_{gd3} is gate to drain capacitances of M3 (Miller effect is considered with the gain as -1); V_{in} is the input of inverter INV2, and V_g is the gate voltage of M3 as shown in Fig. 3.5.

The nonlinear capacitance C_{db} depends on drain-bulk voltage V_{db}, which are V_g and V_g-V_{dd} for M1 and M2, respectively. To simplify the analysis, we use C_{eq}=$k_{eq}C_{j0}$ over the voltage range of interest to estimate C_{db}. k_{eq} is a coefficient which can be calculated according to [32]; C_{j0} the junction capacitance under zero-bias. The obtained C_{db1}+C_{db2} is less than 8% of C. Thus the error from the estimation can be neglected.

Shown in Fig. 3.7(a), we assume V_{in} as

$$V_{in} = \begin{cases} V_{dd} - \dfrac{V_{dd}}{t_f}t & (0 \le t \le t_f) \\ 0 & (t > t_f) \end{cases} \tag{3.3}$$

where t_f is V_{in} transition time from V_{dd} to 0. According to the drive capability of trigger pulse generator, input voltage transition is so fast that NMOS M1 is turned off after triode region, without working in saturation region. Also, the PMOS M2 is still in saturation when V_{in} reaches zero as observed from the simulation results in Fig. 3.7(a). The following modeling of V_g is based on such fast input considerations [33-35].

Region I: $V_{dd} \geq V_{in} \geq V_{dd}-|V_{th2}|$, $0 \leq t \leq \frac{|V_{th2}|}{V_{dd}} t_f$, M1 is in triode region, and M2 operates in subthreshold region. Since subthreshold current equation is complex, the differential equation (3.2) cannot be solved analytically, so the value of I_{sub2} at $V_{in}=V_{dd}-V_{th2}/2$ is used as the drain current, i.e. $I_{sd2}=-I_{ds1}=I_{sub2}$. Then (3.2) becomes

$$C\frac{dV_g}{dt} = C_{gd12}\frac{dV_{in}}{dt} + 2I_{sub2} \tag{3.4}$$

which gives

$$V_{gI} = -\left(\frac{C_{gd12}V_{dd}}{Ct_f} - \frac{2I_{sub2}}{C}\right)t \tag{3.5}$$

where $C_{gd12}=(0.5C_{ox}W_1L_1+C_{gdo}W_1)+C_{gdo}W_2$.

Region II: $V_{dd}-|V_{th2}| \geq V_{in} \geq V_{th1}$, $\frac{|V_{th2}|}{V_{dd}} t_f \leq t \leq \frac{V_{dd}-V_{th1}}{V_{dd}} t_f$, M1 works in triode region, and M2 is saturated. $I_{ds1} \approx 0$ because V_{ds1} is nearly zero. For I_{sd2}, the second term of (3.1-b) is neglected due to the approximation $V_{sd2} \approx V_{dd}$, thus $I_{sd2}= I_{sd0}\left(\frac{V_{sg2}-|V_{th2}|}{V_{dd}-|V_{th2}|}\right)^{\alpha}$. (3.2) is

$$C\frac{dV_g}{dt} = C_{gd12}\frac{dV_{in}}{dt} + I_{sd0}\left(\frac{V_{sg2}-|V_{th2}|}{V_{dd}-|V_{th2}|}\right)^{\alpha} \tag{3.6}$$

which gives

$$V_{gII} = -\frac{C_{gd12}V_{dd}}{Ct_f}t + \frac{I_{sd0}t_f}{C\left(V_{dd}-|V_{th2}|\right)^{\alpha+1}(\alpha+1)V_{dd}}\left(\frac{V_{dd}}{t_f}t-|V_{th2}|\right)^{\alpha+1} + c_1 \tag{3.7}$$

where $C_{gd12}=(0.5C_{ox}W_1L_1+C_{gdo}W_1)+C_{gdo}W_2$, c_1 is a constant which makes $V_{gII}=V_{gI}$ at $t=|V_{th2}|t_f/V_{dd}$.

Region III: $V_{th1} \geq V_{in} \geq 0$, $\frac{V_{dd}-V_{th1}}{V_{dd}} t_f \leq t \leq t_f$, M1 is off, and M2 is in saturation region. $I_{ds1} \approx 0$, and $I_{sd2} = I_{sd0}\left(\frac{V_{sg2}-|V_{th2}|}{V_{dd}-|V_{th2}|}\right)^{\alpha}$. So V_{gIII} is the same as V_{gII} in (3.7), where $C_{gd12}=C_{gdo}W_1+C_{gdo}W_2$ and c_1 is another constant which makes $V_{gIII}=V_{gII}$ at $t=(V_{dd}-V_{th1})t_f/V_{dd}$.

Region IV: $V_{in}=0$ and $V_g \leq V_{dd}-|V_{dsat2}|$, $t>t_f$, M1 is still off, and M2 operates in saturation region. $I_{ds1} \approx 0$, and I_{sd2} is

$$I_{sd2} = I_{sd0} + 2\left(I_{sd0} - I'_{sd0}\right)\frac{V_{sd2}-V_{dd}}{V_{dd}}$$

$$= I_{sd0} - 2\left(I_{sd0} - I'_{sd0}\right)\frac{V_g}{V_{dd}} \tag{3.8}$$

(3.2) becomes

$$C\frac{dV_g}{dt} = I_{sd0} - 2\left(I_{sd0} - I'_{sd0}\right)\frac{V_g}{V_{dd}} \tag{3.9}$$

From (3.9) M3 gate voltage is given by:

$$V_{gIV} = \frac{I_{sd0}V_{dd}}{2\left(I_{sd0}-I'_{sd0}\right)} + \left(\frac{C_{gd12}V_{dd}}{C} + \frac{I_{sd0}t_f\left(V_{dd}-|V_{th2}|\right)}{C(\alpha+1)V_{dd}} + \frac{2I_{sub2}|V_{th2}|t_f}{CV_{dd}} - \frac{I_{sd0}V_{dd}}{2\left(I_{sd0}-I'_{sd0}\right)}\right) e^{\frac{2\left(I'_{sd0}-I_{sd0}\right)}{CV_{dd}}(t-t_f)} \tag{3.10}$$

where $C_{gd12}=C_{gdo}W_1+C_{gdo}W_2$.

Region V: $V_{in}=0$ and $V_g > V_{dd}-|V_{dsat2}|$, $t>t_f$, M1 is still off, and M2 works in triode region. $I_{ds1} \approx 0$, and $I_{sd2} = I_{dsat2}\left(2-\frac{V_{dd}-V_g}{V_{dsat}}\right)\frac{V_{dd}-V_g}{V_{dsat}}$.

$$C\frac{dV_g}{dt} = I_{dsat2}\left(2 - \frac{V_{dd} - V_g}{V_{dsat}}\right)\frac{V_{dd} - V_g}{V_{dsat}} \tag{3.11}$$

Solve (3.11), V_g is:

$$V_{gV} = V_{dd} - V_{dsat}e^{-\frac{2I_{dsat}}{CV_{dsat}}(t-t_0)} + c_2 \tag{3.12}$$

where $C_{gd12}=C_{gdo}W_1+(C_{gdo}W_2+0.5C_{ox}W_1L_1)$, t_0 is the time when $V_{gV}=V_{dd}-V_{dsat2}$, and c_2 is a constant which makes $V_{gV}=V_{gIV}$ when $V_g=V_{dd}-|V_{dsat2}|$.

The input voltage V_{in}, simulated V_g and modeled V_g are shown in Fig. 3.7(a). There are some discrepancies between the simulated and modeled V_g. However, the rise times of V_g are comparable.

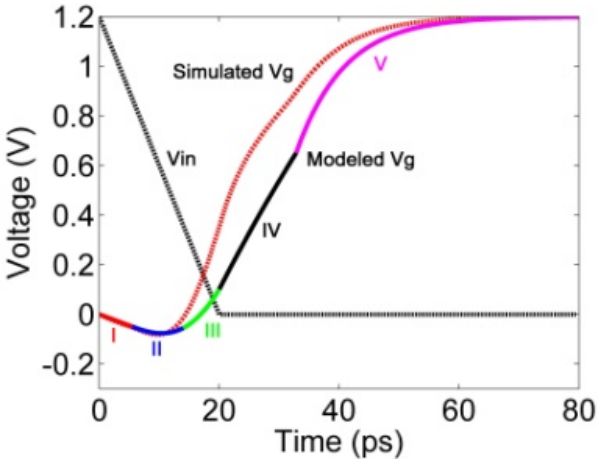
3.3.1.2 NMOS Switch

With the obtained gate voltages above, we can analyze the switch transistor operations. The differential equation that describes the discharge of the load capacitance C_{db3} is given by:

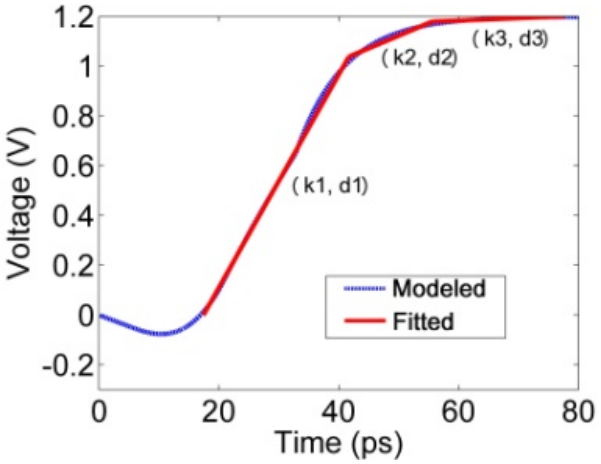
$$C'\frac{dV_d}{dt} = C_{gd3}\frac{dV_g}{dt} - I_{ds3} \tag{3.13}$$

where $C'=C_{gd3}+C_{db3}$, C_{gd3} is gate to drain capacitance of M3, V_d is the drain voltage of M3.

In order to use (3.13), the modeled V_g in Fig. 3.7(a) is linearized into three segments with Matlab polynomial curve fitting as shown in Fig. 3.7(b). The obtained V_g is



(a)



(b)

Fig. 3.7. (a) Simulated and modeled gate voltage V_g (region I-V)curves. (b) Modeled and fitted V_g curves. M3 W/L=200 μm/0.12 μm.

$$V_g(t) = \begin{cases} k_1 t + d_1 \\ k_2 t + d_2 \\ k_3 t + d_3 \end{cases} \tag{3.14}$$

where k_1, k_2, k_3 and d_1, d_2, d_3 are constants from data fitting. Therefore, the operation of the NMOS switch can be analyzed as the following.

Region I: $0<V_g \leq V_{th3}$, $0 \leq t \leq (V_{th3}-d_1)/k_1$, NMOS switch operates in subthreshold region. Similar to the operation of M2, I_{sub3} at $V_g=V_{th3}/2$ is used as the drain current. (3.13) becomes

$$C' \frac{dV_d}{dt} = C_{gd3} \frac{dV_g}{dt} - I_{sub3} \tag{3.15}$$

The initial condition of $V_d=V_{dd}$ at $t=0$, thus (3.15) can be solved as

$$V_{dI} = \frac{\left(k_1 C_{gd3} - I_{sub3}\right)t}{C'} + V_{dd} \tag{3.16}$$

Region II: $V_{th3}<V_g \leq V_d+V_{th3}$, $(V_{th3}-d_1)/k_1<t \leq (V_{th3}+V_d-d_1)/k_1$, NMOS switch works in saturation region. The capacitances at the drain are discharged by the drain current, which has a maximum value of

$$I_{dsmax} = \frac{V_{dd}}{R_l + Z_0 + R_{on}} \tag{3.17}$$

where R_{on} is the on-resistance of NMOS switch in (3.18).

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{w}{l}\left(V_g - V_{th3}\right)} \tag{3.18}$$

When I_{ds3} does not reach I_{dsmax} shown in (3.17), (3.13) becomes

$$C' \frac{dV_d}{dt} = C_{gd3} \frac{dV_g}{dt} - I_{ds0}\left(\frac{V_g - V_{th3}}{V_{dd} - V_{th3}}\right)^{\alpha} \tag{3.19}$$

$$V_{dII} = -\frac{I_{ds0}}{C'\left(\alpha+1\right)k_1\left(V_{dd} - V_{th3}\right)^{\alpha}}\left(k_1 t + d_1 - V_{th3}\right)^{\alpha+1} + \frac{C_{gd3}V_{dd}}{C' t_r} t + c_3 \tag{3.20}$$

where c_3 is a constant which make drain voltage V_d continuous at $V_d=(V_{th3}+V_d-d_1)/k_1$.

Region III: Drain current reaches I_{dsmax}, (3.13) is

$$C' \frac{dV_d}{dt} = C_{gd3} \frac{dV_g}{dt} - I_{ds3} \tag{3.21}$$

V_d is

$$V_{dIII} = \frac{C_{gd3} k_1 - I_{dsmax}}{C'} t + c_4 \tag{3.22}$$

where c_4 is a constant which make drain voltage V_d continuous when $I_{ds3} = I_{dsmax}$.

Region IV: $t \geq (V_{th3}+V_d-d_1)/k_1$, $V_d+V_{th3} \leq V_g \leq V_{dd}$, NMOS enters triode region. Since drain current keeps the maximum value I_{dsmax} in this region, V_d expression is the same with (3.22) until V_d reaches the minimum $V_{dIV}=R_{on}I_{dsmax}$.

As discussed in section 3.2, NMOS M3 resistance R_{eq} is much higher than TL characteristic impedance Z_0 before it is completely turned on. Therefore, currents that pass through the TL are small. Thus TL load effect on M3 is neglected in the analysis. Simulated drain voltages V_d in Fig. 3.8 further confirms our analysis.

With (3.16), (3.20) and (3.22), the modeled drain voltages are shown in Fig. 3.9. The overshoot of modeled V_d in region II is larger than the simulated result, and modeled V_d decreases slower than the simulated result. They are probably caused by C_{gd3} calculation error. For wider NMOS (W/L=200 μm/0.12 μm), C_{gd3} calculation error is larger. Larger C_{gd3} and V_d overshoot cause longer propagation delay and slower V_d fall edge. Nevertheless, the errors do not significantly affect output pulse modeling due to voltage division process discussed in section 3.2.

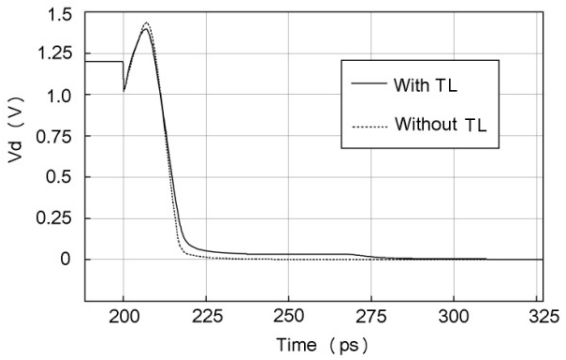
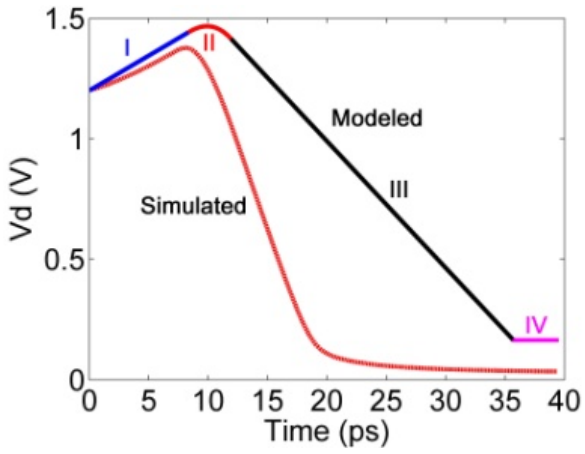
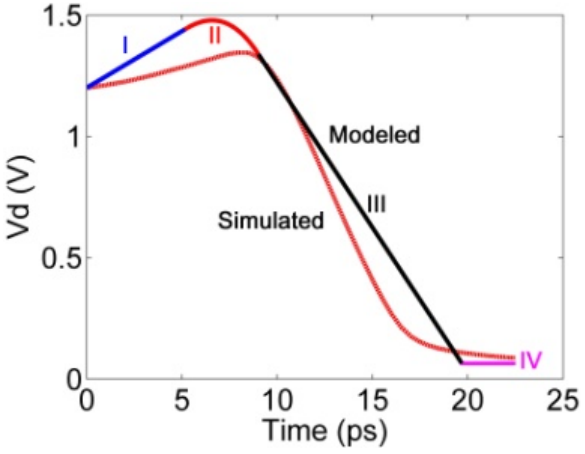


Fig. 3.8. Simulated drain voltages V_d with TL and without TL.



(a)



(b)

Fig. 3.9. Simulated and modeled M3 drain voltage (a) W/L=200 μm/0.12 μm (b) W/L=100 μm/0.12 μm.

3.3.1.3 Output Pulse

We follow the approach in [36] to obtain the output pulses. The Laplace transform for load current is

$$\dot{i}_l(s)=\int_0^{\infty} i(t)e^{-st}dt=\frac{V_{dd}}{s\left(R_l+R_{eq}+Z_0 coth(s\delta)\right)}$$

$$=\frac{V_{dd}\left(1-e^{-2s\delta}\right)}{s\left(Z_0+R_l+R_{eq}\right)}\left[1-\frac{Z_0-\left(R_l+R_{eq}\right)}{Z_0+\left(R_l+R_{eq}\right)}e^{-2s\delta}+\left[\frac{Z_0-\left(R_l+R_{eq}\right)}{Z_0+\left(R_l+R_{eq}\right)}\right]^2 e^{-4s\delta}-\ldots\right] \quad (3.23)$$

where R_l is the load resistance, and $\delta=l/v=\sqrt{LC}$ is the propagating time of voltage from input port to load port.

The inverse Laplace transformation of (3.23) gives the current in time domain

$$\dot{i}_l(t)=\frac{V_{dd}}{Z_0+R_l+R_{eq}}\left\{1-U\left(t-2\delta\right)-\frac{Z_0-\left(R_l+R_{eq}\right)}{Z_0+\left(R_l+R_{eq}\right)}\left[U\left(t-2\delta\right)-U\left(t-4\delta\right)\right]\right.$$

$$\left.+\left[\frac{Z_0-\left(R_l+R_{eq}\right)}{Z_0+\left(R_l+R_{eq}\right)}\right]^2\left[U\left(t-4\delta\right)-U\left(t-6\delta\right)\right]-\ldots\right\} \quad (3.24)$$

where $R_{eq}(t)=V_d(t)/I_{ds3}(t)$, U is Heaviside step function:

$$U(x)=\begin{cases}1 & (x>0)\\ 0 & (x<0)\end{cases}\cdots \quad (3.25)$$

where $x=(t-n\delta)$, $n=2,4,6\cdots$

The output voltage $V_{out}(t)$ is

$$V_{out}(t) = -R_l i_l(t) \tag{3.26}$$

When V_g reaches the maximum, since $R_{eq}(t) \ll Z_0+R_l$, output voltage $V_{out} \approx 0.5V_{dd}$.

3.3.2 Simulation and Modeling Analysis

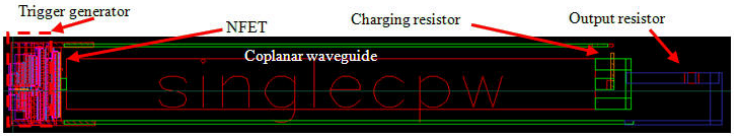
The circuit in Fig. 3.4(a) is implemented in IBM 0.13 μm CMOS technology. Fig. 3.10(a) shows a layout of the circuit for Cadence Spectre simulation analysis. The PFL is 500 μm long. All circuit components are standard devices provided by the process vendor. Fig. 3.10(b) shows the typical waveform obtained from post layout simulation. The input trigger signal, V_{in} in Fig. 3.10(b), has a 50 ps rise time. Such input pulses can be easily obtained on chip, for instance by using ring oscillators. The input trigger signal is then converted to a pulse with ~ 27 ps rise edge to drive the NMOS, shown in Fig. 3.10(b). The obtained output pulse on a 50 Ω load resistor shown in Fig. 3.10(c) has 10.4 ps full-width-at-half-magnitude (FWHM), which is close to the expected value (7.7 ps) determined by the line length and the signal velocity, ~ 1.3×10^{11} mm/s. The 2.7 ps difference mainly comes from the slow switching process of the NMOS due to the 27ps long trigger pulse rise edge and the parasitic drain capacitance of the NMOS switch. Nevertheless, the obtained pulse width is significantly shorter than ~ 43 ps, the FO4 delay of the technology. The obtained pulse amplitude is ~ 600 mV, which is ~ 200 mV less than $V_{dd}/2$ (800 mV). The difference is caused by NMOS resistance and relatively slow trigger pulse rise edge. Once again, the simulation results show that the simple circuit in Fig. 3.1(a) significantly expands the short pulse generation capabilities of conventional digital circuits.

Fig. 3.11 shows simulation results for different PFL length and V_{dd}. For longer PFLs, the obtained pulse parameters (both pulse width and amplitude) are closer to the expected values due to diminished significance of trigger pulse rise edge and parasitic effects. Higher V_{dd} results in faster trigger pulses, therefore, shorter output pulses with higher magnitudes. Repetitive pulses can also be generated with the circuit. The main limitation of the pulse repetition rate is the PFL charging time. For the circuit in Fig. 3.4(a), the repetition rate is up to 400 MHz.

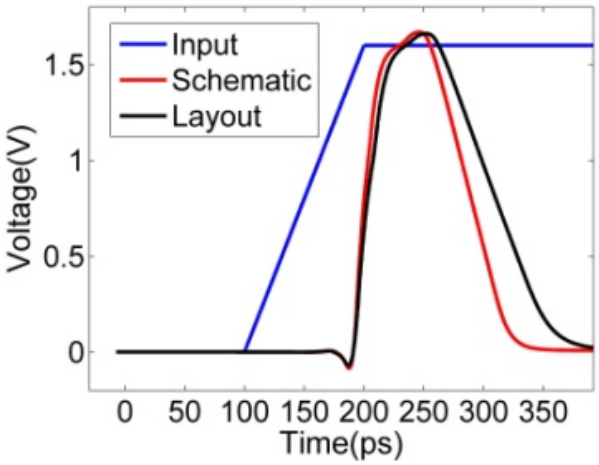
With $V_d(t)$ and $I_d(t)$ modeled in section 3.3.1 and considering M3 maximum drain current I_{dsmax}, $R_{eq}(t)$ can be calculated. Then using (3.26), output pulses for two NMOS switch sizes are modeled and the results are shown in Fig. 3.12. During the turning-on of M3, voltage at load is reflected because of mismatching at output port. The reflected voltage comes back from input port to output port and forms the rise edge of pulse. The modeled pulses on load resistor R_l are nearly the same with the simulated ones, which confirms the validity of V_{out} modeling method. A more detailed comparison of simulated and modeled parameters is in Table 3.1. Due to lower V_d decrease rate Fig. 3.9 (a), larger fall time discrepancies are observed for *W=200* μm NMOS switch case than *W=100* μm switch.

TABLE 3.1 Simulated and modeled parameters

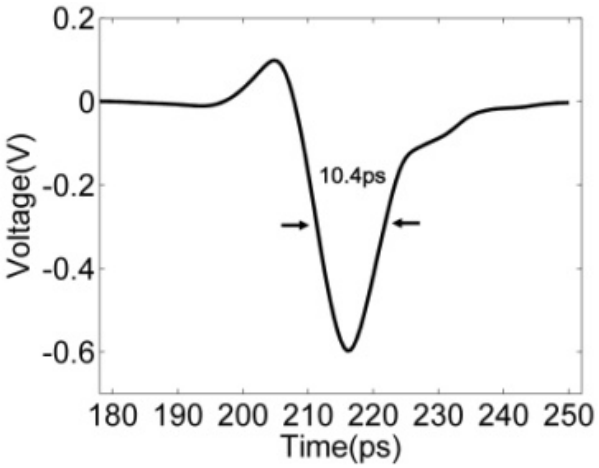
NMOS switch width (μm)	Result	Pulse width (ps)	Pulse amplitude (mV)	Pulse fall time (ps)
100	Simulated	62.08	-538.2	6.89
	Modeled	61.54	-587.5	9.63
200	Simulated	61.93	-554.8	7.83
	Modeled	61.54	-593.8	13.53



(a)

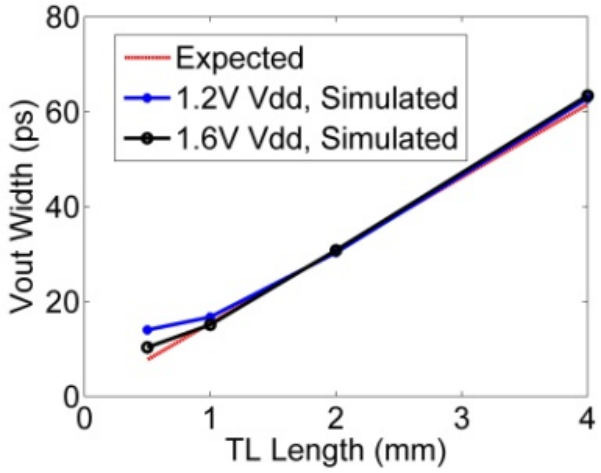


(b)

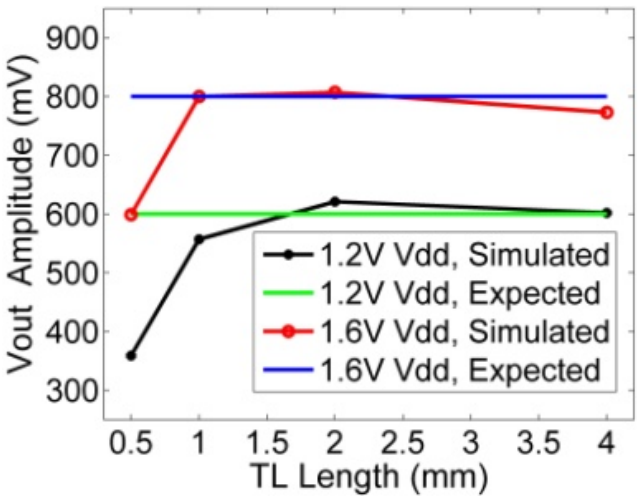


(c)

Fig. 3.10. Proposed circuit implementation and simulation results. (a) Circuit layout. (b) Waveforms of the input signal with a 50 ps rise time and NMOS trigger signal. (c) Output pulses on a 50 Ohm resistor.

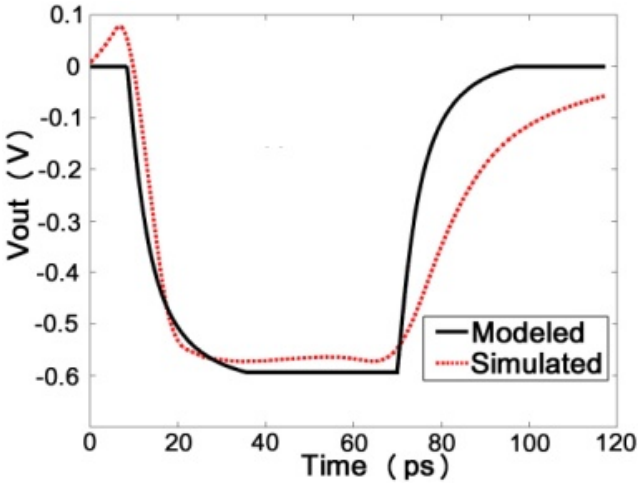


(a)

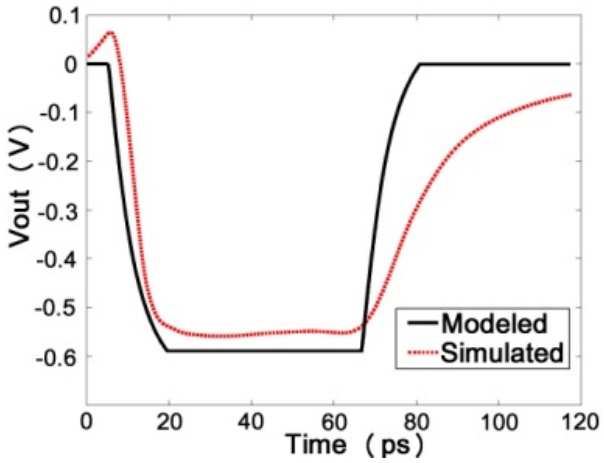


(b)

Fig. 3.11. Output pulse width (a) and amplitude (b) vs. PFL length.



(a)



(b)

Fig. 3.12. Modeled and simulated output voltage for NMOS switch with (a) *W*/*L*=200 μm/0.12 μm (b) W/L=100 μm/0.12 μm

3.3.3 Blumlein PFL with High Voltage Switch

Based on the circuit in Fig. 3.1(a), other circuits can be designed for high voltage pulse generations. Fig. 3.13 shows a Blumlein configuration PFL, which can generate

higher output pulse. V_{ddh} is $2V_{dd}$. The two-device (M1 and M2) cascade open-drain output circuit [37] works as a high voltage switch in the circuit. The voltage limit of resistor, NMOS breakdown voltage and P+/N-Well diode breakdown voltage should be considered to avoid breakdown. All the devices can work reliably under $V_{ddh}=2V_{dd}$. The simulated output pulse of 5 mm Blumlein line is shown in Fig. 3.14. The pulse amplitude and width of post-layout simulation are worse than expected values. The reasons may be sheet resistance of T-line metal, parasitic capacitance of the process resistor, on-resistance of cascaded NMOS switch and parasitic capacitance of wirebond pad.

3.4 CMOS Implementation

The circuit in Fig. 3.4(a) is fabricated in IBM 0.13 μm CMOS technology. Fig. 3.15(a) shows a micrograph of a fabricated pulse generator with 4 mm long meander TL. It occupies an area of ~ 400 μm × 900 μm. Output pulses are measured with Tektronix DPO 7354 oscilloscope. Fig. 3.15(b) shows the measured output pulse when the output is connected to a 50Ω terminated oscilloscope. The rise time is about 100 ps, fall time is about 100 ps and the pulse duration time is about 160 ps, which is much longer than the expected pulse width (~ 70 ps in Fig. 3.12(a)). The output signal amplitudes are from ~ 0.11 V to ~ 0.2 V, which are much lower than the expected $V_{dd}/2$.

Factors that limit the measurement accuracies include (i) the oscilloscope with ~3.5 GHz bandwidth, (ii) dispersion and loss caused by the measurement connection setup, which has probes, connectors, and cables. Fig. 3.16 shows the frequency response of the connection setup.

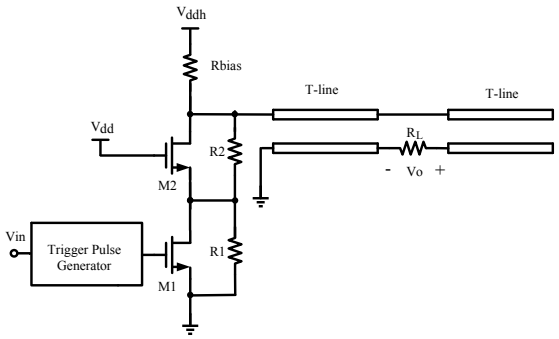
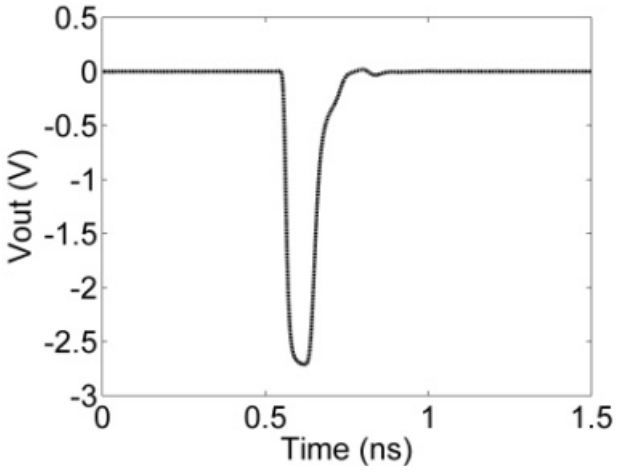
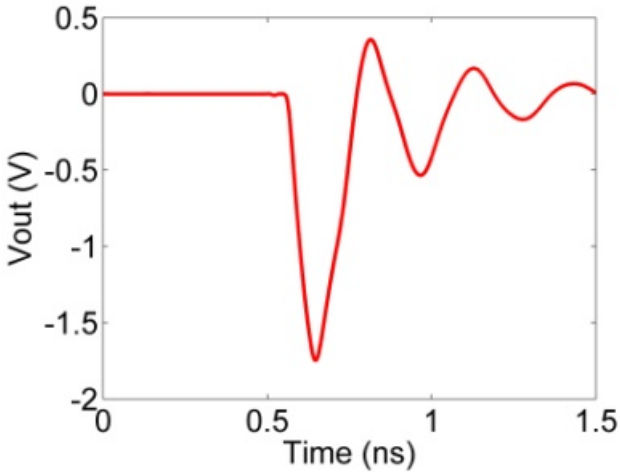


Fig. 3.13. Blumlein PFL with cascade NMOS switch



(a)



(b)

Fig. 3.14. Simulated output pulse of 5 mm Blumlein PFL for (a) schematic (b) post-layout.

We can estimate the rise time of a measureable signal with our system as [38]

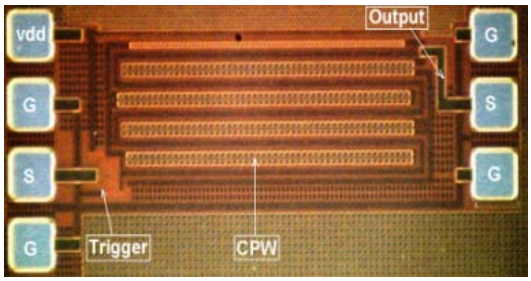
$$t_{rise\_system} = \sqrt{t_{rise\_cable}^2 + t_{rise\_osc}^2} \approx 147\,ps \tag{3.27}$$

where the 10%-90% rise time of cable, connector and probe is $t_{rise\text{-}cable}$=2.2/$\omega_{\text{-3dB}}$=25ps; the 10%-90% rise time of oscilloscope is t_{rise_osc}=145ps. The minimum measureable pulse duration of the system is $2t_{rise\_system}$≈300 ps.

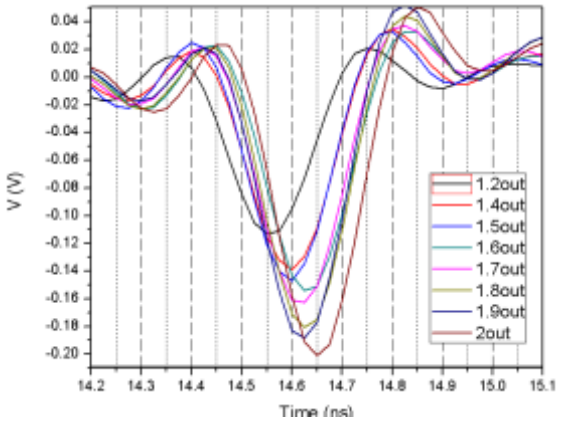
3.5 Discussion and Conclusions

The circuit in Fig. 3.1(a) is nonlinear with unique properties. Unlike nonlinear transmission line (NLTL) short pulse generation technologies [39-41] (which use long transmission lines and dozens of varactors), the circuit in Fig. 3.1(a) uses only one relatively short transmission line and one nonlinear device (i.e. the switch). In comparison with optoelectronic short pulse techniques, the circuit in Fig. 3.1(a) is an electronic approach amenable for integration. Furthermore, the above simulation analysis shows that the circuit is promising to expand short pulse generation capabilities of CMOS technologies. Therefore, the circuit is promising to generate high-power pulses on-chip. However, there are several issues that need further explanations and explorations.

The first is the validity of the above simulation analysis since our measurements only verify the results partially. The process vender verified corresponding circuit element models up to 50 GHz or 100 GHz. This frequency range corresponds to pulses of ~10 ps FWHM. Therefore, the validity of the simulation results is justifiable even though there are still concerns of un-accounted parasitic effects, which need further studies since their impact is elevated in picoseconds pulse generations.



(a)



(b)

Fig. 3.15. (a) A micrograph of an on-chip pulse generator. (b) Measured output pulses with different V_{dd} listed in the figure.

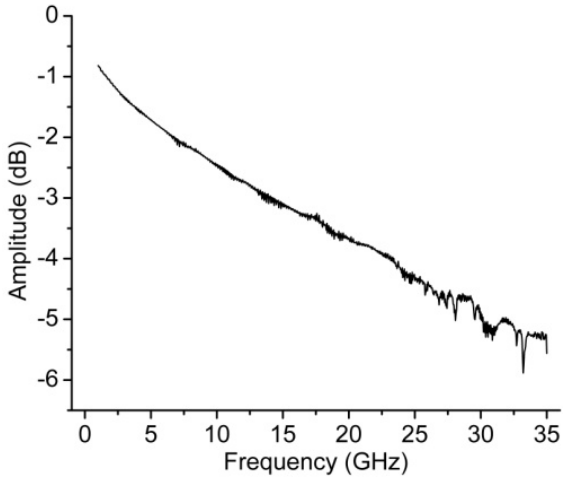


Fig. 3.16. Frequency response of the cable, connector and probe.

Second, when used for picosecond pulse generation, the corresponding measurement is challenging since there are no techniques currently available for picosecond pulse measurement on silicon. Nevertheless, we characterize the frequency response of the connection setup and estimate the rise time of whole measurement system to explain the main reasons for the discrepancies between measurements and simulation analyses.

Thirdly, the proposed circuits are simple and all the circuit components in Fig. 3.1(a) are realizable in GaAs and SiGe technologies [42-45]. Therefore, the proposed circuit can be implemented in GaAs and SiGe BiCMOS processes, where much shorter pulses can be generated and optoelectronic measurement approaches are possible.

Lastly, there are many challenges for high-voltage and high-power pulse generation on-chip due to various breakdown voltages of the devices in the 0.13 μm CMOS technology. Addressing the challenge need further work.

In conclusion, we study a PFL based CMOS circuit to generate high-voltage high-power short electrical pulses on chip. The effects of PFL length, switch speed and switch resistance on the output pulses are clarified. CMOS pulse generators with on-chip TLs and NMOS switches are modeled and analyzed. Modeled pulses agree with the simulated ones reasonably well. The analyses show that the circuits significantly extend the short and high-power pulse generation capabilities of CMOS technologies. A CMOS implementation of the circuit verifies the validity of the proposed approach. In a 0.13 μm CMOS technology, pulses of ~ 200 mV with ~ 160 ps FWHM are obtained. The pulse repetition rate is up to 400 MHz. Further work is needed to address issues on parasitic effects, measurements, and high-voltage pulse generations.

CHAPTER 4

SUMMARY AND FUTURE WORK

4.1 Summary

In this work, a CMOS PFL based pulse generator with a 4 mm long TL is implemented in the commercial 0.13 μm technology. Pulses of ~ 160 ps duration and 110-200 mV amplitude on a 50Ω load are obtained when the power supply is tuned from 1.2 V to 2.0V. Through simulation, modeling and measurement, the PFL circuit significantly extends short and high-power pulse generation capabilities of CMOS technologies. High-voltage and high-power outputs can be generated from Blumlein PFLs with stacked MOSFET switches.

To provide high voltage bias source for the pulse generator, a four-stage charge pump with Schottky diode as charge transfer cell is implemented in the 0.13 μm technology. Charge pump output voltage and efficiency under different power supply voltages, load currents and clock frequencies are measured and presented. The maximum output voltage is ~ 6 V and the maximum efficiency is ~ 50%.

4.2 Future Work

Before charge pump is used as V_{ddh} for Blumlein structure pulse generator, the load regulation should be considered and characterized, since the switching activity of switch can change charge pump's load, and then affect the output voltage.

In order to increase output voltage and pumping efficiency, Schottky diode can be replaced other charge transfer cells with lower forward drop voltage.

For Blumlein structure pulse generator, even higher voltage pulse can be generated if the multi-stage stacked switch in Fig. 5 of [37] or in Fig. 3 of [46] is used as switch.

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