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CIRCUIT MODULES FOR SIX-PORT REFLECTOMETER ON CHIP

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CIRCUIT MODULES FOR SIX-PORT REFLECTOMETER ON CHIP

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ABSTRACT

Broadband signal generator is an indispensable module for broadband Six-Port Reflectometer (SPR). To integrate a whole SPR system on a chip, the source must be compact. In this thesis, a three-stage voltage-controlled oscillator (VCO), using two parallel weak invertor-chain oscillators and sense amplifiers, is proposed and designed in a 0.13 µm CMOS process. These two parallel weak inverter-chain oscillators extend the low frequency operating range and the sense amplifiers expand the high frequency operation. The measurement results show that the oscillator can be tuned from 430 MHz to 12 GHz, which satisfies the targeted SPR operating frequency range.

In order to expand the operating frequency band of the SPR, an introduction of the tuning mechanisms is necessary. Inductors and capacitors are the two basic components for the circuit modules of an SPR. Varactors are provided by process vendors. In this thesis, a novel differential active inductor is proposed and implemented in a 0.13 µm CMOS process. The measured self-resonance frequency is 6 GHz, which is the highest self-resonance frequency published thus far for a differential inductor. The proposed structure is further improved by adding a symmetrical negative resistor. Post layout shows a 10 GHz self-resonance frequency.

A power divider is a common module in the SPR and microwave circuits. A new lumped-element power divider structure, which presents the strongest tolerance to parasitic resistors in capacitors and inductors, is proposed and analyzed in this thesis by even- and odd-mode method. Varactors and the above-mentioned active inductors are used to build the proposed power divider. The circuit is designed in a 0.13 µm CMOS

process with a core area of 300 µm×265 µm. Post layout simulation yields a tuning range from 1 GHz to 7.5 GHz.

DEDICATION

This work is dedicated to my parents, my brother, and my girlfriend for all their support and encouragement.

ACKNOWLEDGMENTS

I would like to thank God for my present achievements and for being my moral support throughout my life. I would like to thank my parents who give me life and my family for their support and encouragement, especially my mother who always helps me go up after the setbacks. I would like to thank Dr. Wang, my advisor, for providing valuable advice, support and encouragement throughout all the research work. I would like to thank Dr. W. Rod Harrell, Dr. Lin Zhu for serving on my committee, the time they spent reviewing my work and their invaluable suggestions. I would like to thank Dr. L. Wilson Pearson for serving on my committee, his support to the measurement experiment and suggestions. His enthusiasm will always be in my mind.

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CHAPTER ONE

INTRODUCTION

The six-port measurement technique was introduced in 1977 by Glen F. Engen in the National Institute of Standards and Technology [1.1]. The basic theory is, in a linear six ports network, as shown in Fig 1.1, the following relationships exist:

$$b_3 = Aa_2 + Bb_2 \tag{1.1}$$

$$b_4 = Ca_2 + Db_2 \tag{1.2}$$

$$b_5 = Ea_2 + Fb_2 \tag{1.3}$$

$$b_6 = Ga_2 + Hb_2 \tag{1.4}$$

where a_i and b_i are the reflective waves and complex incident at port P_i. *A*-*H* are complex constants.

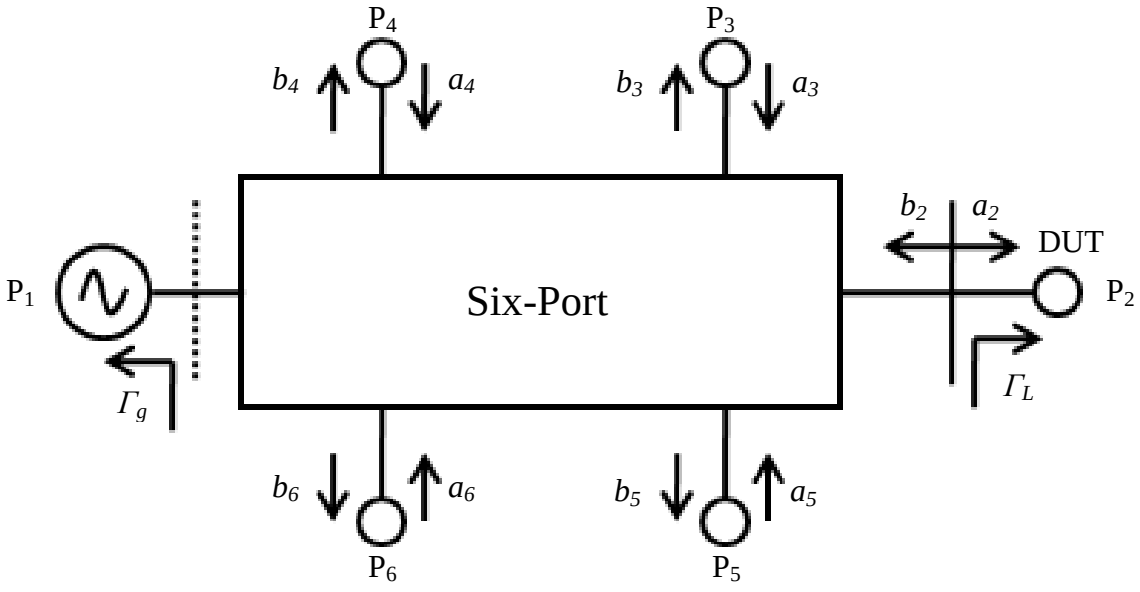

Fig. 1.1 Block diagram of six ports network. P_1 is connected to the power source, P_3-P_6 are the power measurement ports and P_2 is device under test (DUT) port.

The power response P_i (*i=3, 4, 5 and 6*) at port P_3-P_6 can be obtained from equations (1.1)-(1.4) and are shown in the following:

$$P_3 = |A|^2 |b_2|^2 |\Gamma_L - q_3|^2 \tag{1.5}$$

$$P_4 = |D|^2 |b_2|^2 |\Gamma_L - q_4|^2 \tag{1.6}$$

$$P_5 = |E|^2 |b_2|^2 |\Gamma_L - q_5|^2 \tag{1.7}$$

$$P_6 = |G|^2 |b_2|^2 |\Gamma_L - q_6|^2 \tag{1.8}$$

$$\Gamma_L = \frac{a_2}{b_2},\ q_3 = -\frac{B}{A},\ q_4 = -\frac{D}{C},\ q_5 = -\frac{F}{E},\ q_6 = -\frac{H}{G} \tag{1.9}$$

If P_4 is treated as a power reference port, then the power ratio P_i/P_4 (*i=3, 5, 6.*) are shown in the following:

$$\frac{P_3}{P_4} = \left|\frac{A}{D}\right|^2 \left|\frac{\Gamma_L - q_3}{\Gamma_L - q_4}\right|^2 \tag{1.10}$$

$$\frac{P_5}{P_4} = \left|\frac{E}{D}\right|^2 \left|\frac{\Gamma_L - q_5}{\Gamma_L - q_4}\right|^2 \tag{1.11}$$

$$\frac{P_6}{P_4} = \left|\frac{G}{D}\right|^2 \left|\frac{\Gamma_L - q_6}{\Gamma_L - q_4}\right|^2 \tag{1.12}$$

The parameters, three real and four complex values (q_3, q_4, q_5 and q_6), which are frequency-dependent, can be decided by a calibration procedure which will not be detailed in this thesis [1.2]-[1.4].

To simplify the algebraic process to obtain the parameters in equations (1.10-1.12), a match condition at source port P_1 is always desired. P_4 is isolated with P_2 (which means *C=0*). Then the power ratios are:

$$\frac{P_3}{P_4} = \left|\frac{A}{D}\right|^2 \left|\Gamma_L - q_3\right|^2 \tag{1.13}$$

$$\frac{P_5}{P_4} = \left|\frac{E}{D}\right|^2 \left|\Gamma_L - q_5\right|^2 \tag{1.14}$$

$$\frac{P_6}{P_4} = \left|\frac{G}{D}\right|^2 \left|\Gamma_L - q_6\right|^2 \tag{1.15}$$

The constants in equation (1.13)-(1.15) can be determined by doing calibration [1.2]-[1.4]. Then the reflection coefficient of the DUT can be obtained by measuring the power at the P_3-P_6. The performance of the SPR is determined by the distribution of q_i according [1.5] and the optimum condition is $|q_i|\approx 1.5$ and $arg(q_i)-arg(q_j)\approx 120^0$. The six-port is still considered functional as long as the phase differences of two q-points do not drop below 45^0 [1.6]-[1.8].

Many applications of six-port beside SPR for scatting parameter measurement have been published. Six-port wireless communication receivers are reported in [1.9]-[1.11] and cancer detection are presented in [1.12]-[1.13]. The six-port can also be used in complex permittivity measurement [1.14] and as six-port interferometer (SPI) radios [1.15].

The SPR has been built in many forms. The classic structure which owns close ideal property (The magnitude of q_3, q_5 and q_6 are $\sqrt{2}$, 2 and 2 respectively; the

differences of their phase angles are 135^0, 90^0, 135^0 respectively; the structure also has relatively broadband operating capabilities.) is presented [1.16]. The bandwidth is important since it has been one of the limitations of SPR in comparison with heterodyne architectures. Two lumped-element SPRs composed of resistors in MMIC technologies and owning multi-GHz bandwidth are introduced in [1.6]-[1.7]. Since the bandwidth is increased at the expense of large power loss which will decrease the sensitivity of the SPR, then finding a solution to extend the operating bandwidth of six-port is necessary.

According to Fig 1.1, a broadband source generator is indispensable. To integrate the SPR on a chip, the structure must be compact. The LC oscillator presents better noise performance than the relax oscillator, but the operation frequency bandwidth is a limitation even through there is some progress [1.18]-[1.19]. Since our target does not have strict requirements to the phase noise as that of the communication circuit, then the ring oscillator may be a reasonable choice.

In Chapter II, which is a paper to be submitted, a novel delay cell with a sense amplifier used to boost the maximum frequency is proposed and analyzed. The proposed delay cell is used in the design of a three-stage ring oscillator. Two weak inverter ring oscillators, which are used to extend the frequency to the low frequency, are added to the three-stage VCO. The circuit is implemented in a 0.13 μm CMOS process with an area of 630 μm×290 μm. The measurement tuning frequency range is 430 MHz to 12 GHz.

To extend the operating frequency band, as for the SPR, the introduction of a tuning mechanism is an option. Meanwhile, the tuning mechanism can filter the noise, which may be channeled to the broadband power detectors and increase the signal to

noise ratio. In the classic SPR structure [1.16], power dividers and couplers are needed. Despite the efforts in developing compact on-chip transmission lines to overcome chip-area constraints [1.20]-[1.21], the lumped-element structure is the best choice for a smaller area thus far. According to the present lumped-element structures [1.22]-[1.23], basic components are inductors and capacitors. Varactors are provided by CMOS process vendors and active inductors are research topics (There are dozens of papers published in *IEEE* even in this year.). The self-resonance frequencies of the differential active inductor structures reported until now are less than 4 GHz [1.24]-[1.26], which is not enough for our target.

In Chapter III, which is a published paper [1.27], a novel active inductor is proposed and analyzed. The post-layout simulation results show that the self-resonance frequency is up to 10 GHz. To verify the performance, a lumped-element Wilkinson power divider with 9.5 GHz center frequency using the proposed active inductor was designed successfully.

Chapter IV, which is a journal paper submitted, presents a novel lumped-element power divider structure, which occupies smaller area than those in [1.22]-[1.23] and presents strong tolerance to the parasitic resistors in the varactors and inductors. The proposed lumped-element power divider is designed in a 0.13 μm CMOS process using the proposed active inductors in Chapter IV. The post-layout simulation results show that it can be tunable from 1 GHz to 7.5 GHz which is the largest tuning range thus far. The conclusion and discussion are in Chapter V.

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CHAPTER TWO

SOURCE GENERATOR—A VOLTAGE-CONTROLLED DIFFERENTIAL OSCILLATOR TUNABLE FROM 430 MHz TO 12 GHz

***Abstract*—In this paper, a three-stage differential voltage-controlled oscillator (VCO) tunable from 430 MHz to 12 GHz band is presented and analyzed. To boost the maximum operating frequency, a sense amplifier is added to each ordinary differential delay cell. Then two three-stage weak inverter ring oscillators are added to extend the tunable frequency range to the low frequency. This structure is implemented in a 0.13 µm CMOS process and the core occupies an area of 140 µm×40 µm. The output power is -12 dBm to -29 dBm when the frequency is tuned from 430 MHz to 12 GHz.**

I. INTRODUCTION

A compact, low-cost source with a large tuning range is a key circuit block for integrated high-frequency systems and their applications. Software-defined radios (SDR), six-port network analyzer on chip (NAoC) are two examples [2.1]-[2.2]. The latter was proposed for broadband dielectric spectroscopy applications and is the targeted application of this work. It has been demonstrated that discrete component LC oscillators can have an octave frequency tuning range with superb phase noise performance for communication system applications. However, those oscillators occupy large areas; therefore, they are difficult for integration [2.3]-[2.4]. On the other hand, ring oscillators are compact and easy to integrate in CMOS technology, yet their phase noise is higher

than that of LC oscillators. Nevertheless, for many dielectric spectroscopy applications, phase noise requirement is not nearly as stringent as it for communication systems. Therefore, ring oscillators are reasonable choices.

There have been many efforts to extend the frequency tuning range of ring oscillators. By programming the number of paralleled inverter rings, a turning range from 103 MHz-1.02 GHz was achieved in [2.5]. A hybrid control scheme (tuning R and varactors) with 12-23 GHz range in SiGe-bipolar technology was developed in [2.6]. A coupled two-stage structure with frequency tunable from 2.5 GHz to 9 GHz was proposed in [2.7]. A new delay cell with a tuning range from 120-420 MHz was also demonstrated by use of replica bias and one additional discharge path [2.8]. A delay cell tunable from 100 KHz to 1 GHz was presented in [2.9], where the maximum operating frequency depends on the supplying ability of the current source. None of these circuits can cover from a few hundred MHz to 10 GHz which is the targeted frequency range of the NAoC development.

Here, a novel delay cell structure is presented. A sense amplifier is added to a classic differential pair to boost the maximum oscillating frequency. To expand its low frequency operation, two weak inverter ring oscillators are added. A three-stage ring oscillator based on the proposed structure is fabricated in a 0.13 μm CMOS process and the measured operating frequency is tunable from 430 MHz to 12 GHz.

This work is arranged as follows: the proposed delay cell is analyzed in Section II; Section III presents circuit design and measurement results. The conclusions are given in Section IV.

II. PROPOSED DELAY CELL STRUCTURE

Differential amplifiers with P latches or N latches are usually used in ring oscillators to sharpen both the rising and falling edges. The combination of the two latches is a sense amplifier which can operate at very high frequencies. Sense amplifiers can be used to increase the maximum oscillator frequencies or inject the energy into the oscillators utilizing wave phenomena. To construct oscillators with sense amplifiers, phase shifter or resonance stimuli are needed; otherwise the sense amplifier will get stuck. Standing wave oscillators and traveling wave oscillators are examples using phase shifters (normally by transmission line or lumped-element transmission line) and sense amplifiers, they can operate as high as Ku, K or Ka frequency bands, but their frequency tuning ranges are limited [2.10]-[2.11].

The proposed delay cell for broadband tunable VCO is shown in Fig. 2.1. A_1, A_2, A_3 and A_4 are inverters. The sense amplifier is composed of cross coupled inverters A_3 and A_4. The differential amplifier is composed by M_1, M_2, M_3 and M_4. The sizes of NMOS and PMOS in A_1 and A_2 are about 10% of M_1 and M_3, respectively. The function of differential amplifier and A_1, A_2 is similar to that of the transmission lines in the traveling wave oscillator. The difference is that there is gain here while transmission lines incur loss. The voltage gain of the delay cell is controlled by tuning the tail current source I_0, M_3 and M_4. As a result, the operating frequency is tuned.

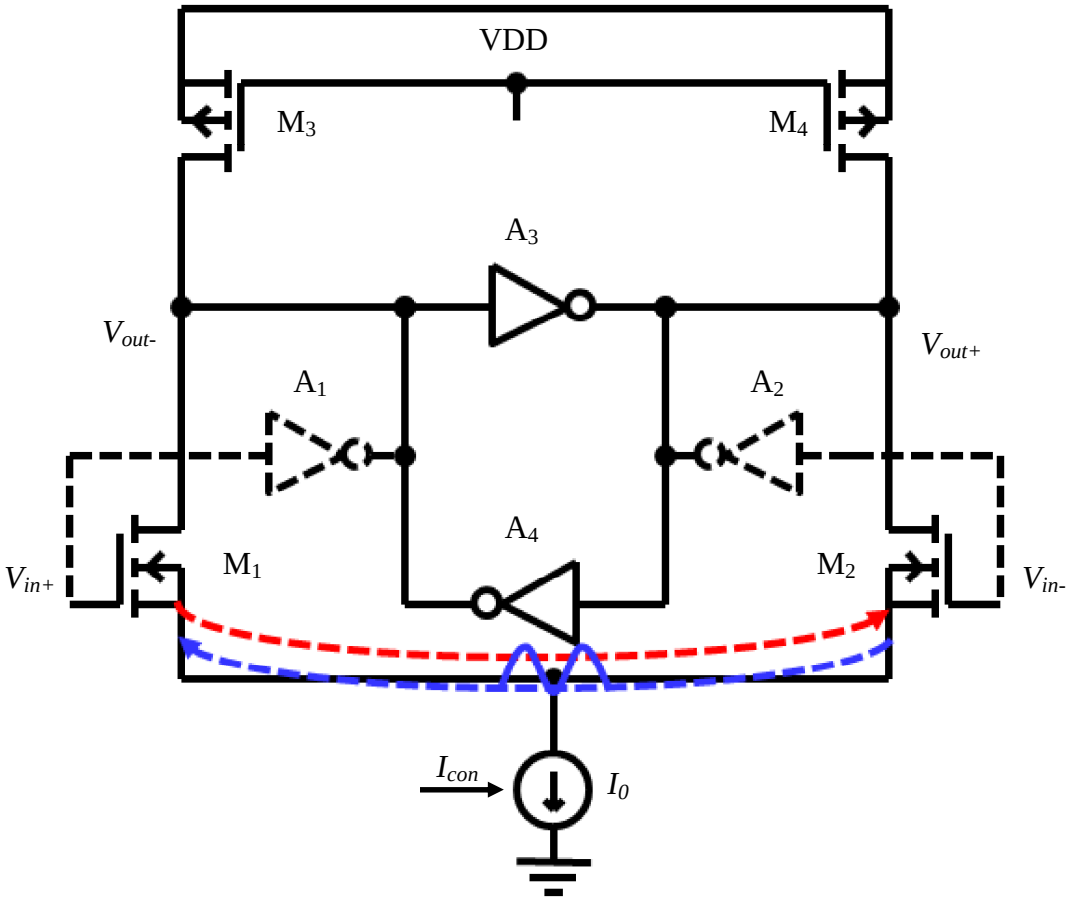


Fig. 2.1. The proposed delay cell.

According to the operating regions of transistors M_1, M_2, M_3 and M_4, the operation of the delay cell can be classified in three different states: minimum frequency state, when tail current source I_0 is small, and M_3 and M_4 are off; normal state when the tail current source is on but not very large, and M_3 and M_4 are in the saturation states; maximum frequency state, when the tail current source I_0 supplies maximum current, V_{con} is zero.

A. Minimum Frequency State

In the minimum operating frequency environment, the tail current source is off; M_3 and M_4 are in the cut off states too. But the transconductances of M_1 and M_2 are not totally zero and there is current flowing between their sources with double oscillation frequency, as indicated by the dashed lines in Fig. 2.1. There are DC biases supplied by A_1 to A_4 in both gates of M_1 and M_2 as well. For the half circuit of the delay cell, the voltage gain is $-g_{m1}\times(R+1/(j\omega C_L))$, in which R is the channel resistance and C_L is the parasitic capacitance at the $Out_{+/-}$ points. In a few hundred MHz, when M_3 and M_4 are tuned off, $1/(j\omega C_L)$ can be ignored and the phase is -180^0, which satisfies the phase requirement of the Barkenhausen criteria shown in equation (2.1) [2.12]:

$$\angle H(j\omega_0) = 180^0, \text{ and} \tag{2.1}$$

$$\left|H(j\omega_0)\right| \geq 1, \tag{2.2}$$

where ω_0 is the oscillation frequency and $H(j\omega_0)$ is the transfer function of the oscillator circuit.

The transconductance g_{m1} is very small when no DC current is flowing through M_1 and M_2. In order to ensure oscillation in the presence of possible temperature and process variations, the loop gain should be at least twice or three times the required value [2.12]. Then the gain of the present circuit must be increased. The simulation results show that A_1 and A_2 can supply large gain for a 0.52 V DC bias as shown in Fig. 2.2 and start the oscillation. In this state, the operating frequency is determined by the parasitic

capacitances at points $Out_{+/-}$ and the charging and discharging current abilities of the sense amplifier.

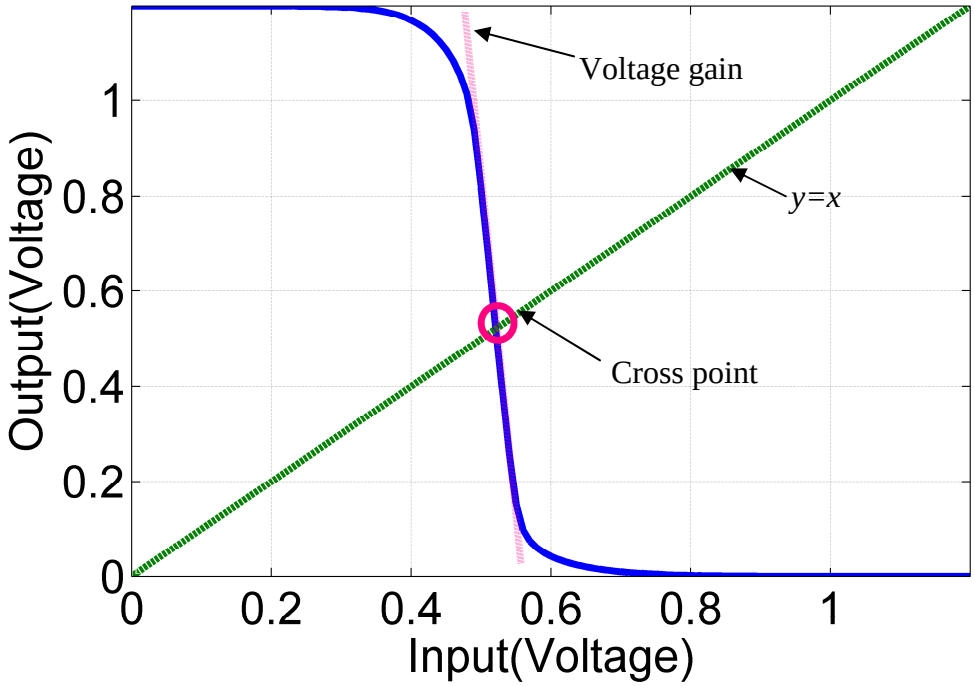


Fig. 2.2. Solid line is the DC analysis of A_1 and A_2. Dash line is $y=x$. The dotted line gives the gain at the cross point and is 14 V/V.

B. Normal State

In the normal state, A_1 and A_2 can be ignored because they are small. Then the proposed delay cell can be simplified, as shown in Fig. 2.3. It consists of two parts with the ability to function autonomously: the cross-coupled inverter pair (A_3 and A_4) and the tunable differential delay cell. When positive feedback is provided by M_5-M_8, the combined delay cell extends the high-frequency operating range. Meanwhile, the delay still kept symmetrical differential structure, which can inhibit the common mode noise. The small signal analysis is shown in Fig. 2.4.

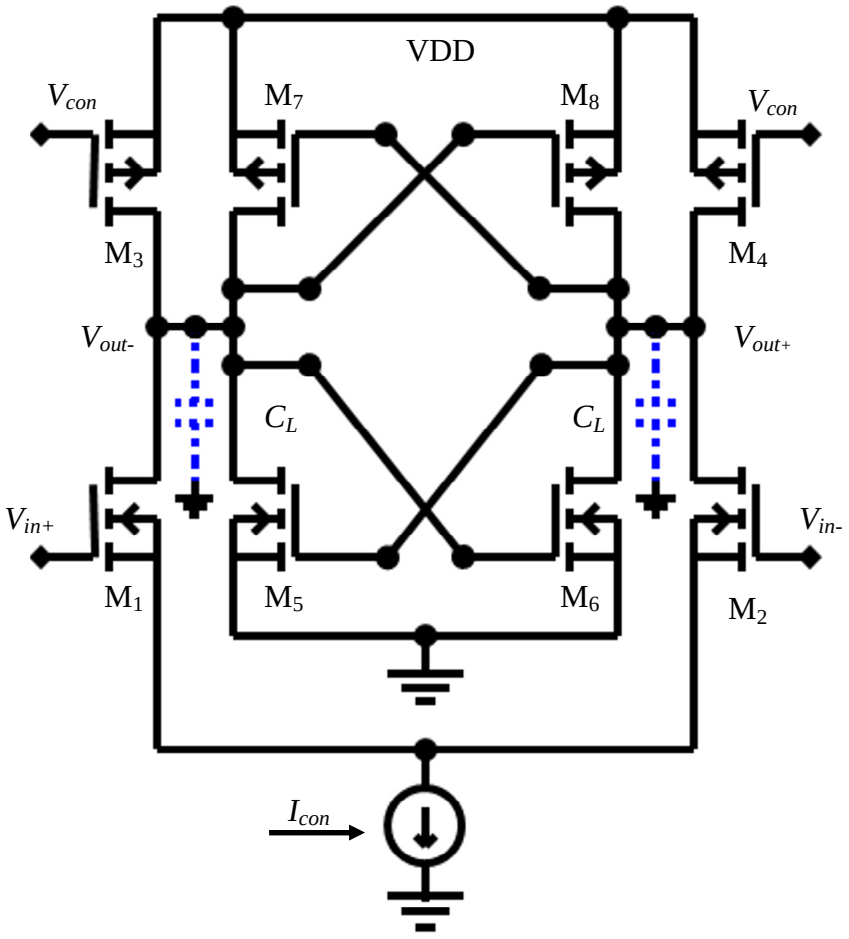


Fig. 2.3. Schematic of the delay cell under normal state.

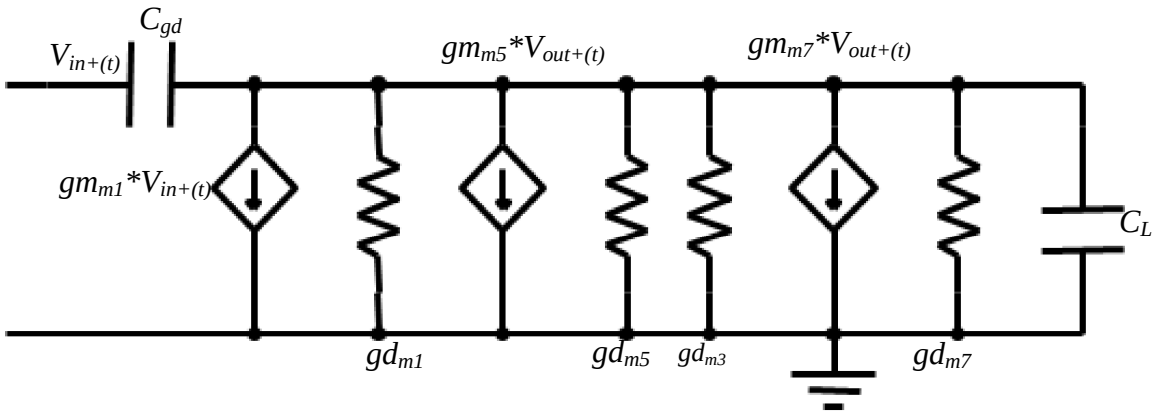


Fig. 2.4. Small signal model of half of the circuit in Fig. 2.3.

Fig. 2.4 shows the small signal model of half of the delay cell. The transfer function of the delay cell is:

$$A(s) = \frac{v_{out-}(t)}{v_{in+}(t)} = \frac{-gm_{m1} + sC_{gd}}{-gm_{m5} - gm_{m7} + gd_{m1} + gd_{m3} + gd_{m5} + gd_{m7} + s(C_L + C_{gd})} \tag{2.3}$$

where C_L is the total capacitance at the output node; C_{gd} is the gate drain capacitance, while gd_{mi} and gm_{mi} are the channel conductance and transconductance of transistor M_i, respectively.

According to the Barkenhausen criteria in equation (2.2), the following equation must be satisfied:

$$\left| \frac{-gm_{m1} + sC_{gd}}{-gm_{m5} - gm_{m7} + gd_{m1} + gd_{m3} + gd_{m5} + gd_{m7} + s(C_L + C_{gd})} \right| \geq 1 \tag{2.4}$$

Then the frequency can be obtained:

$$f_{osc} \le \frac{1}{2\pi}\sqrt{\frac{gm_{m1}^2 - B^2}{C_L^2 + (C_L + C_{gd})^2}} \tag{2.5}$$

with

$$B = -gm_{m5} - gm_{m7} + gd_{m1} + gd_{m3} + gd_{m5} + gd_{m7} \tag{2.6}$$

where C_L is assumed to be a constant. In the numerator, when current I_{ss} changes from 0 to $I_{ss,\,max}$, gm_{m1} changes from $gm_{m1,\,min}$ (~0) to $gm_{m1,\,max}$. Because the control voltage V_{con} ranges from 0 to Vdd, then gd_{m3} value ranges from $gd_{m3,\,max}$ to 0. Both of them can be used to tune the oscillation frequency. When the B^2 in the numerator cancels out the $gm_{m1,2}$, the oscillator operates at its minimum oscillation frequency. Likewise, when the maximum value of gm_{m1} is used and B is 0, the oscillator operates at its maximum frequency as shown in the following:

$$f_{osc} \le \frac{1}{2\pi}\frac{gm_{m1}}{\sqrt{C_L^2 + (C_L + C_{gd})^2}} \tag{2.7}$$

However, when gm_{m1} and gd_{m3} are tuned, the transfer function cannot always satisfy the oscillation requirement, and they are restricted by the Berkenhausen criteria in equation (2.1). For example, when selecting stage number $N=3$, the phase shift of each stage is expected to be 60^0, then:

$$\angle A(j\omega_0) = 60^0 \tag{2.8}$$

Consequently, the following equation can be derived from (2.3) and (2.8):

$$\frac{2\pi f_o\{C_{gd}B + gm_{m1}(C_L + C_{gd})\}}{-gm_{m1}B + 4\pi^2 f_o^{\,2} C_{gd}(C_L + C_{gd})} = \sqrt{3} \tag{2.9}$$

Considering the conditions for maximum frequency determined in the transfer magnitude analysis, and then the following equation can be determined from equation (2.9):

$$f_{o,\max} = \frac{gm_{m1,\max}}{2\sqrt{3}\pi C_{gd}} \tag{2.10}$$

Then the maximum operating frequency is determined by equations (2.7) and (2.10).

When M_3 is off and gd_{m3}=0, then the minimum operating frequency can be determined:

$$f_{\min} \approx \frac{1}{2\pi}\sqrt{\frac{gm_{m1,\min}^2 - (-gm_{m5} - gm_{m7})^2}{C_L^2}} \tag{2.11}$$

For the introduction of M_5, M_6, M_7 and M_8, $B=0$ became possible and it increases the maximum operating frequency range. Similarly, the addition of inverters A1 and A2, M_3 and M_4 can be turned off to achieve $gm_{m1,\ min}$ and gd_{m3} =0, then the minimum operating frequency. Otherwise, when M_3 and M_4 are turned off and gm_{m1}=0, then the oscillator is down for 0 transfer function.

C. Maximum Frequency State

In high frequency operation mode, the tail current source, M_3, and M_4 are on. According to the Barkenhausen criteria, there is an amplitude and a phase of the voltage gain required to the delay cell. But in transistor's high frequency model, the parasitic capacitance, C_{DB}, C_{GD}, and C_{DS} will affect the gain. If the total parasitic capacitance is C_L' and the resistor is signed as R', then the load is $Z= R'-j1/(\omega C_L')$. When $R>0$, then the

voltage gain value will be located in the second quadrant and the gain's phase of each delay cell is in 90^0~180^0 which can not satisfy the Barkenhausen criteria, 60^0 for each stage in a three-stage ring oscillator. When the sense amplifier supplies enough negative resistance and $R<0$, then it is possible for the gain value to be located in the first quadrant.

III. CIRCUIT DESIGN AND MEASUREMENT RESULTS

To verify the proposed structure, a three-stage CMOS ring oscillator was implemented in an IBM 0.13 μm process. The analysis in II shows that the delay cell has two input controllers: V_{con} controls the resistor and I_{con} controls the current source. In order to reduce the influences caused by the fluctuation of the input voltage, V_{con} and I_{con} are adjusted jointly in the design. To obtain constant output power and symmetrical waveforms, the DC bias of M_1 and M_2 should be kept constant as possible over the operating frequency range. So the controllers of tailor current source, I_{con}, and V_{con} for M_3 and M_4 are combined together to keep $I_{M3}+I_{M4}\approx I_0$.

Possible external influences, such as loading by probes, are also a concern. A buffer was added after the oscillator to reduce the effect of probes during measurement and to drive a 50 Ω load. The schematic is shown in Fig 2.5. The layout and the micrograph of the oscillator are shown in Fig. 2.6 with an area of 290 μm×630 μm.

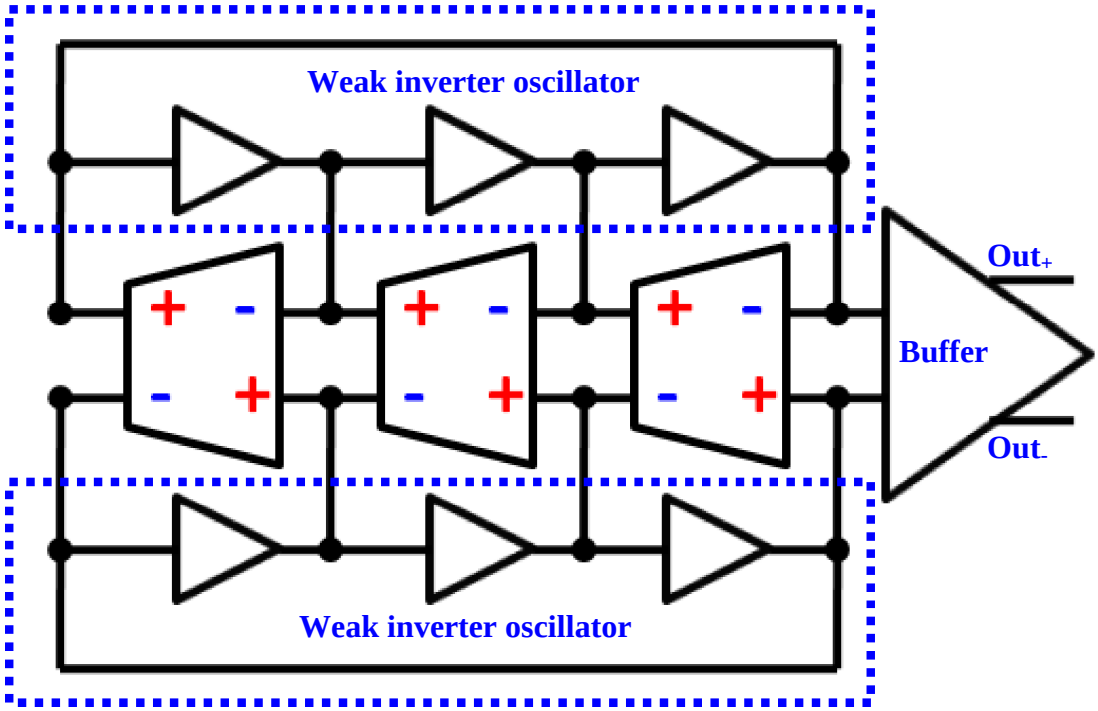
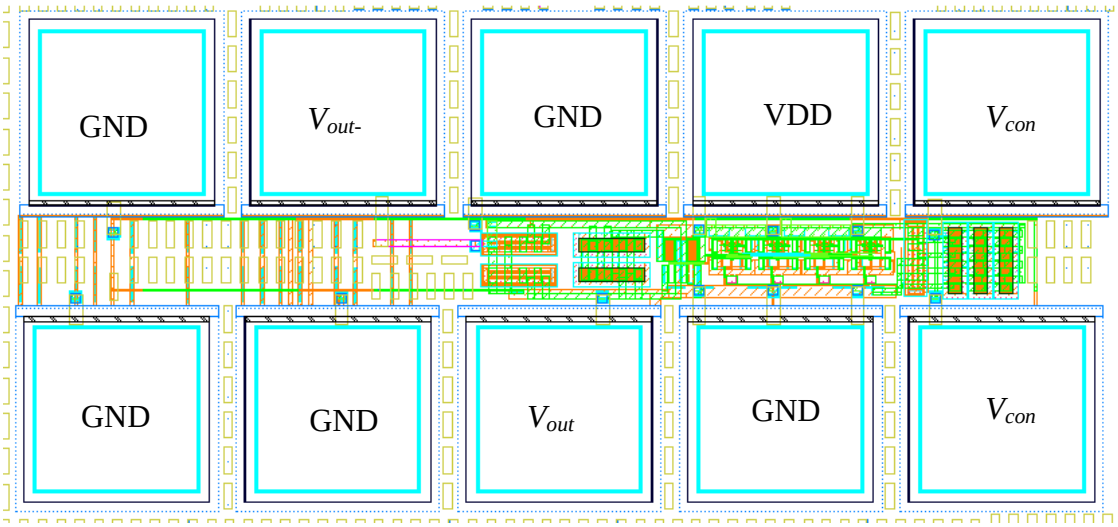
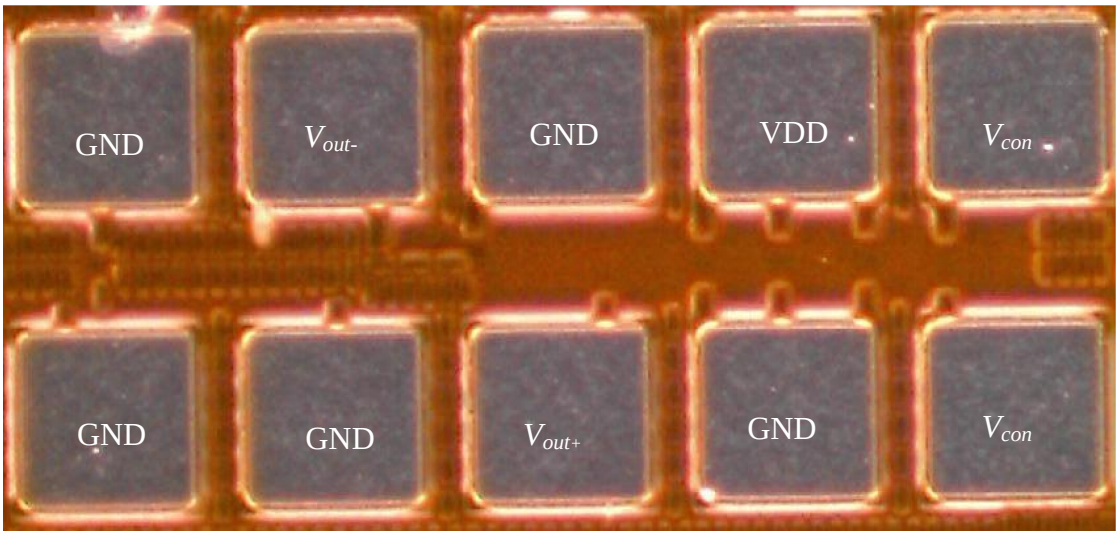


Fig. 2.5. Schematic of the implemented ring oscillator.

The output waveform is measured by using a Tektronix DPO 7345 Digital Phosphor Oscilloscope and is shown in Fig 2.8 at 2.55 GHz.



(a)



(b)

Fig. 2.6. (a)Layout (b) The micrograph of the ring oscillator.

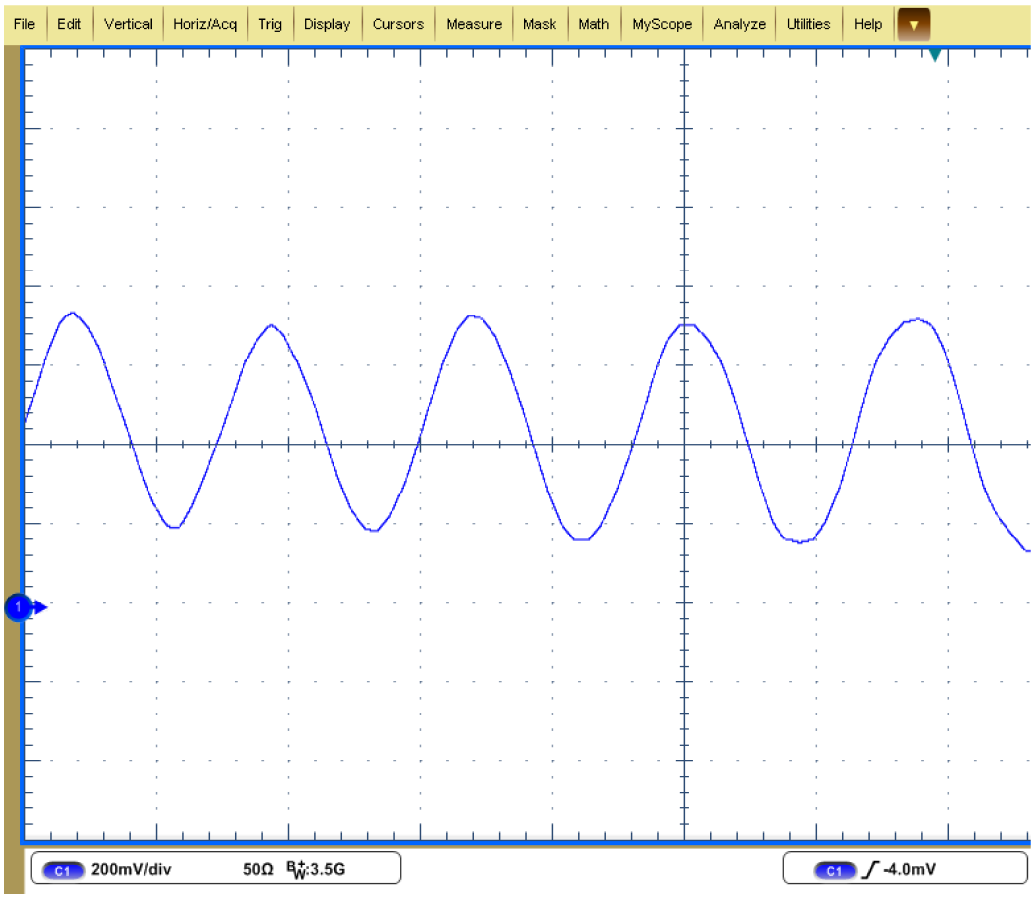


Fig. 2.7. The free running oscillator waveform measured by a Tektronix DPO 7354 Digital Phosphor Oscilloscope at 2.55 GHz. V_{pk}-V_{pk}=570 mV.

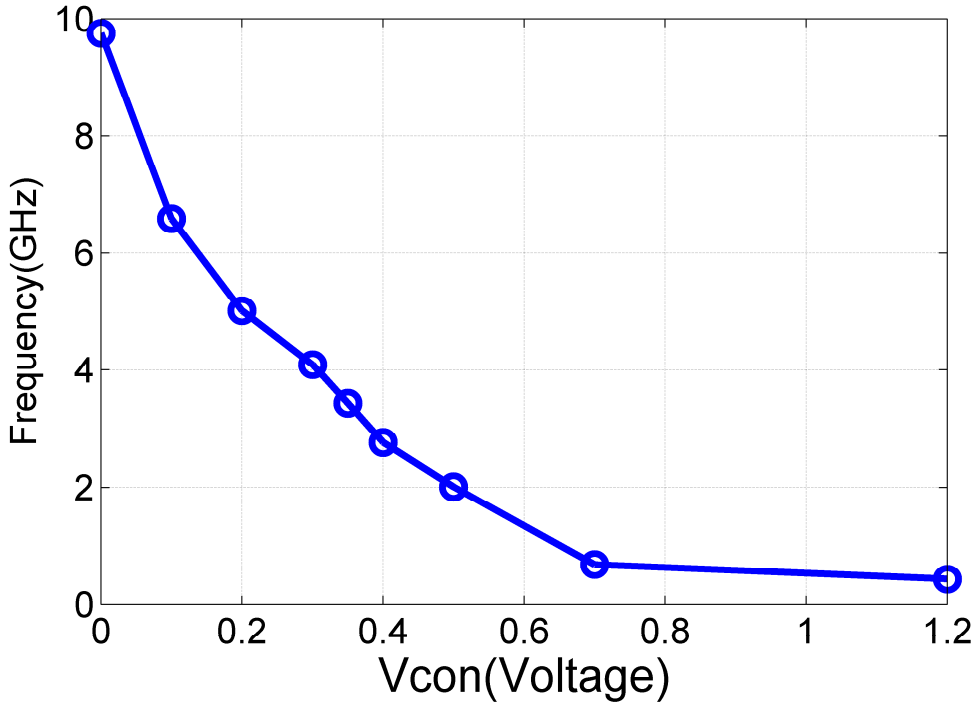


Fig. 2.8. Measured frequency-voltage characteristics varying the control voltage with 1.2 V power supply.

The frequency was measured by use of an HP 8565E spectrum analyzer. Spectrum measurement results show that at a 1.2 V power supply, the oscillator frequency is tunable from 430 MHz to 9.75 GHz. The frequency–voltage characteristic is shown in Fig 2.8. The maximum frequency is 12 GHz with 1.6 V power supply. The power at the output of the buffer decreases from -12 dBm at 430 MHz to -29 dBm at 12 GHz. The power consumption including the buffer will increase from 67 mW to 109 mW. Because this oscillator is designed for a network analyzer on chip application, which needs sufficient input RF powers, the buffer is necessary and it dissipates about 45 mW.

IV. CONCLUSIONS

A sense amplifier is added to the common differential amplifier structure to sharpen the rising and falling time of the delay cell. The delay cell is then used to construct a three-stage ring oscillator. To extend the frequency range to the low frequency, two weak inverter ring oscillators, whose sizes are about 10% of the main delay cell, are added. This circuit is implemented in a commercial 0.13 µm CMOS process. The measurement results show that it is tunable from 430 MHz to 12 GHz, which satisfies the targeted frequency tuning range. Noise analysis and power stability improvement are needed in the further work.

ACKNOWLEDGMENT

This work was supported by NSF Grant ECCS 0622082. Service of MOSIS is acknowledged.

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CHAPTER THREE

A HIGH FREQUENCY TUNABLE DIFFERENTIAL ACTIVE INDUCTOR AND ITS APPLICATIONS TO POWER DIVIDERS

***Abstract*--A CMOS high-Q differential active inductor is proposed in this paper. Simulation results show that the inductance is tunable from ~ 1 nH to 100 nH with operating frequency tunable from 300 MHz to 10 GHz. The inductor occupies 40×70 μm^2 in IBM CMOS8RF 0.13 μm process. It is used to design a 9.5 GHz Wilkinson power divider. The post layout simulation using Spectre shows that, with all ports matched to 50 Ω, the return loss and the output ports isolation are better than 20 dB with an insertion loss of ~ 3 dB. The active area of the miniaturized Wilkinson power divider is 160×170 μm^2, which is suitable for system integration.**

I. INTRODUCTION

Integrated inductors find extensive applications in many facets of radio-frequency integrated circuits (RFIC), including impedance matching circuits, filter circuits, oscillators, and lumped-element power dividers. However, CMOS passive inductors occupy large chip areas. Their fixed inductance values are inconvenient for reconfigurable circuit module design. As a result, there have been many efforts to implement active inductors [3.1]-[3.7].

There are two types of active inductors: single ended and differential. Both are based on the well-known gyrator-C architecture, which uses two transconductance

amplifiers to convert the susceptance of the capacitor C to inductive impedance [3.1]-[3.4]. A single ended inductor is shown in Fig. 3.1. The input impedance is

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{sC}{G_{m1}G_{m2}}. \qquad (3.1)$$

There are a few inherent disadvantages associated with single-ended design, including low inductance values, low quality factor, and narrow operating frequency range. There have been many efforts to overcome these limitations. For instance, Manetakis, et. al. [3.8] introduced a regulated cascade transconductance amplifier topology, which reduces the output conductance. As a result, the equivalent resistance is reduced. And the quality factor *Q*, of the active inductor is improved. The grounded inductor topology is used to implement various RFIC circuits, including a power divider at the center frequency of about 4.5 GHz by Lu et al. [3.9].

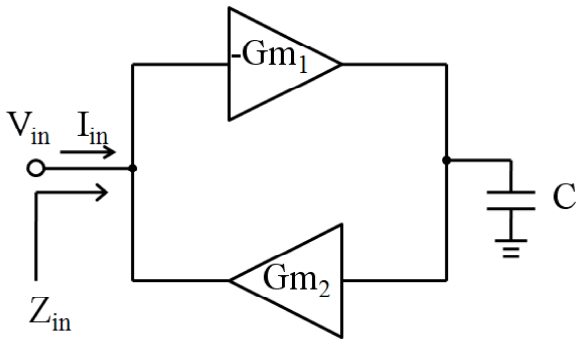

Fig 3.1. Gyrator-C topology for active inductors

The differential gyrator-C active inductor topology was proposed in [3.5]-[3.7]. Ref. [3.5] is a fully differential gyrator configuration comprising two balanced transconductors connected back to back. Ref. [3.7] is composed of two back to back differential transconductance amplifiers. The problems related to current differential active inductors are limited inductance tuning range and low self-resonance frequency (only 1.06 GHz in [3.5] and 3.98 GHz in [3.7]), which limits the operating frequency range of the inductors.

This paper presents a new differential active inductor that is tunable from ~ 1 nH to 100 nH and operating from 300 MHz to 10 GHz. Using the proposed active inductor, a lumped-element Wilkinson power divider is designed. The circuits are designed by use of the IBM CMOS 8RF_DM 0.13 μm process. The paper is organized as follows: Section II describes the proposed tunable differential active inductor. The power divider design is presented in section III. Section IV concludes the paper.

II. PROPOSED TUNABLE DIFFERENTIAL INDUCTOR

A simplified schematic of the proposed circuit is given in Fig 3.2. M1, M2, M3 and M4 compose the differential cascade transconductance amplifier. For just the half circuit, M1, M3, M5, M7 compose one gyrator-C structure and M2, M4, M6, M8 compose the other gyrator-C structure. Then the two gyrator-C structures are connected by M9, M10, M11 and M12. If the entire structure is considered as a differential pair, then M9, M10, M11 and M12 are the feedback pairs which can boost the self-resonance

frequency, inductor value and *Q* factor. There are two controlling terminal *Vcon1* and *Vcon2*. *Vcon1* controls the gain of the differential cascade transconductor amplifier and *Vcon2* controls the gain of the common source amplifier. The inductor value, *Q* factor and resonating frequency are varied by tuning the control voltage *Vcon1* and *Vcon2*. Fig 3.3 is the small signal model of the half circuit of the proposed structure.

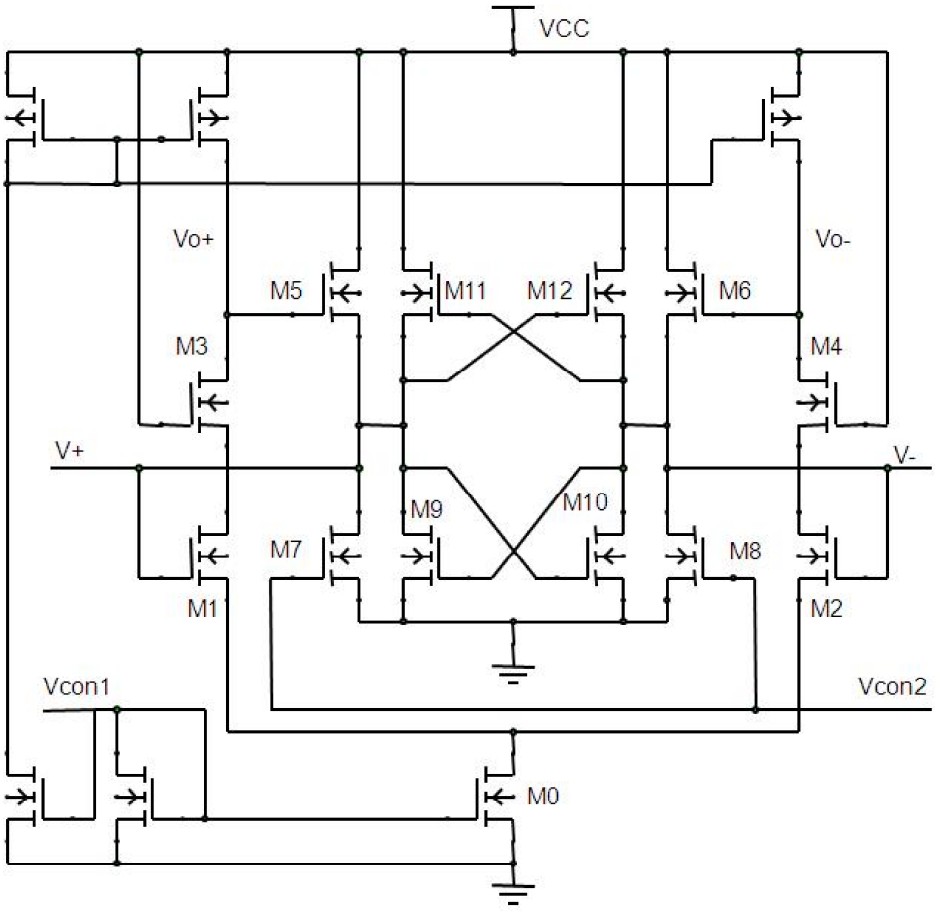

Fig 3.2. The proposed tunable differential active inductor

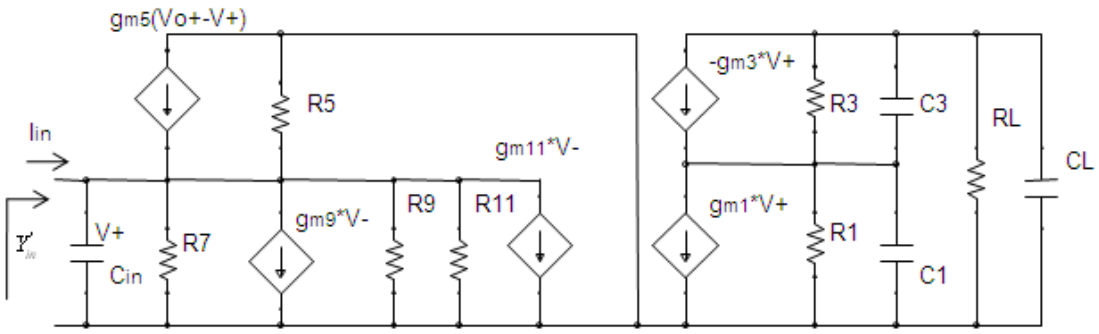

Fig 3.3. The small signal model of the half circuit of the proposed tunable differential active inductor.

g_{m*} is the transconductance of transistor M_* and C_* is the capacitance of the corresponding nodes.

From the small signal model in Fig. 3.3, the input impedance is $Y_{in}^{'}$:

$$Y_{in}^{'} = sC_{in} + \frac{1}{R_5} + \frac{1}{R_7} + \frac{1}{R_9} + \frac{1}{R_{11}} - g_{m5} - g_{m9} - g_{m11} + \frac{g_{m1}g_{m5}(\frac{1}{R_3} + sC_3 + g_{m3})}{B} \tag{3.1}$$

where

$$B = s^2(C_1C_3 + C_1C_L + C_LC_3) + s(C_1(\frac{1}{R_3} + \frac{1}{R_L}) + C_3(\frac{1}{R_L} + \frac{1}{R_1}) + C_L(\frac{1}{R_1} + \frac{1}{R_3} + g_{m3})) + \frac{1}{R_L}(\frac{1}{R_1} + \frac{1}{R_3} + g_{m3}) + \frac{1}{R_3R_L} \tag{3.2}$$

Using the equivalent model in Fig 3.4, the input impedance is

$$Y_{in} = G + sC + \frac{1}{R + sL}. \tag{3.3}$$

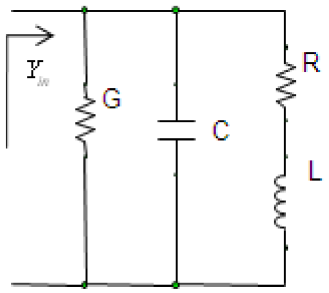

Fig 3.4. The equivalent model of the inductor

From (3.2) and (3.4), the component values in the equivalent model can be determined.

$$G = \frac{1}{R_5} + \frac{1}{R_7} + \frac{1}{R_9} + \frac{1}{R_{11}} - g_{m5} - g_{m9} - g_{m11}, \text{ and} \tag{3.4}$$

$$C = C_{in} \tag{3.5}$$

Both the inductor and resistor values can be simplified to

$$L \approx \frac{C_1C_3 + C_1C_L + C_LC_3}{g_{m1}g_{m5}C_3} \text{ and} \tag{3.6}$$

$$R \approx \frac{C_1(\frac{1}{R_3} + \frac{1}{R_L}) + C_3(\frac{1}{R_L} + \frac{1}{R_1}) + C_L(\frac{1}{R_1} + \frac{1}{R_3} + g_{m3})}{g_{m1}g_{m5}C_3}. \tag{3.7}$$

Equation (3.2) and (3.3) show that there is one zero and two poles if one ignores *G* and *C* (for G can be zero in the design and the poles have no relationship with C). The zero is

$$\omega_z = (\frac{1}{R_3} + g_{m3}) / C_3 . \tag{3.8}$$

The pole is ω_p. In (3.5), by subtracting g_{m9}, g_{m11} and tuning g_{m5}, G can be forced to be close to zero to increase Q factor.

$$\omega_p \approx \sqrt{\frac{(C_1(\frac{1}{R_3}+\frac{1}{R_L})+C_3(\frac{1}{R_L}+\frac{1}{R_1})+C_L(\frac{1}{R_1}+\frac{1}{R_3}+g_{m3}))^2}{4(C_1C_3+C_1C_L+C_LC_3)^2} - \frac{(\frac{1}{R_L}(\frac{1}{R_1}+\frac{1}{R_3}+g_{m3})+\frac{1}{R_3R_L})}{(C_1C_3+C_1C_L+C_LC_3)}} \tag{3.9}$$

By tuning g_{m1} and g_{m5} through V_{con1} and V_{con2}, the pole point, inductor and Q factor can be changed. The inductor post layout simulation results are shown in Fig 3.5, for the case where the signal amplitude is 50 mV, including the pad. It shows that its maximum self-resonance frequency is up to 10 GHz.

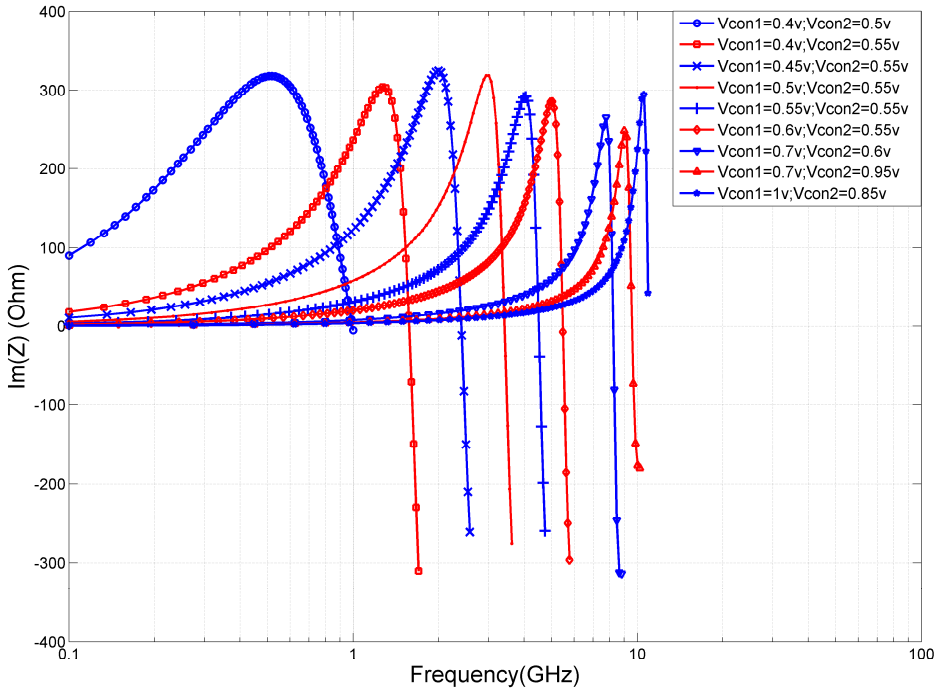

Fig 3.5. The imaginary part of inductor impedance at different control voltage conditions

III. CIRCUIT DESIGN AND POST LAYOUT SIMULATION

Fig 3.6 shows a typical lumped-element Wilkinson power divider with the following circuit components:

$$R = 2Z_0,\ C = \frac{1}{2\sqrt{2}\pi f_0 Z_0},\ \text{and}\ L = \frac{Z_0}{\sqrt{2}\pi f_0}. \tag{3.9}$$

If the center operating frequency is 9.5 GHz with a characteristic impedance of Z_0=*50* Ω, then *R=100* Ω. The capacitance should be *236.9 fF* and inductor should be *1.184 nH*.

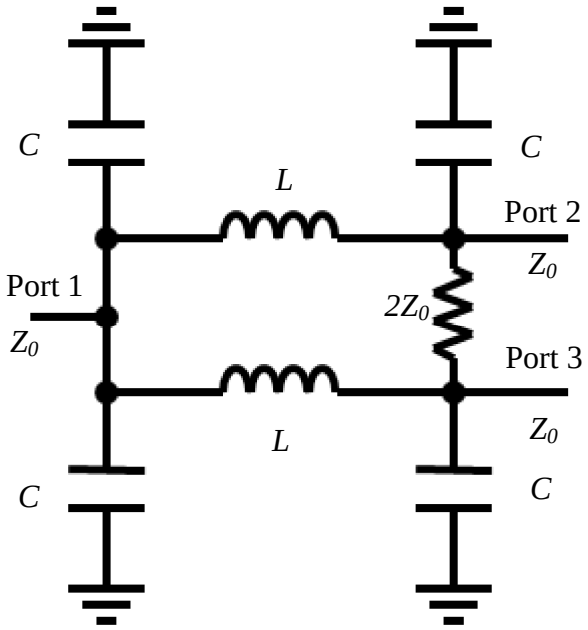

Fig 3.6. Typical lumped-element equivalent π-network power divider.

Fig 3.7 shows the input impedance of the active inductors used for the targeted Wilkinson power divider. The results are obtained from post layout simulations. Two DC isolation capacitors are used. The control voltages are $V_{con1}=800\ mV$ and $V_{con2}=785\ mV$. Fig 3.7 shows that the imaginary part of the input impedance is about 70 ohms at 9.5 GHz, which indicates an inductance value of ~ 1.18 nH. The real part of the input impedance is 0.9 Ohms, indicating $Q=87$ at 9.5 GHz.

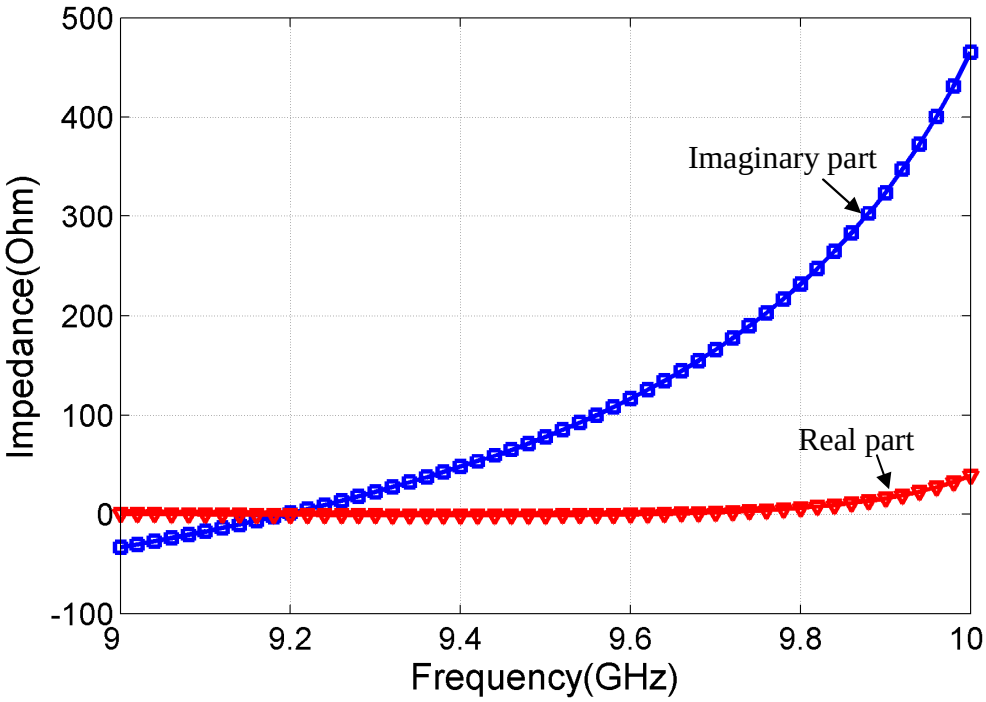

Fig 3.7. The input impedance of the inductor when V_{con1}=800 mV and V_{con2}=785 mV.

The differential active inductor without pads occupies an area of about 40×70 μm^2 and the power divider occupies about 160×170 μm^2 without pads. The layout of the power divider is shown in Fig 3.8.

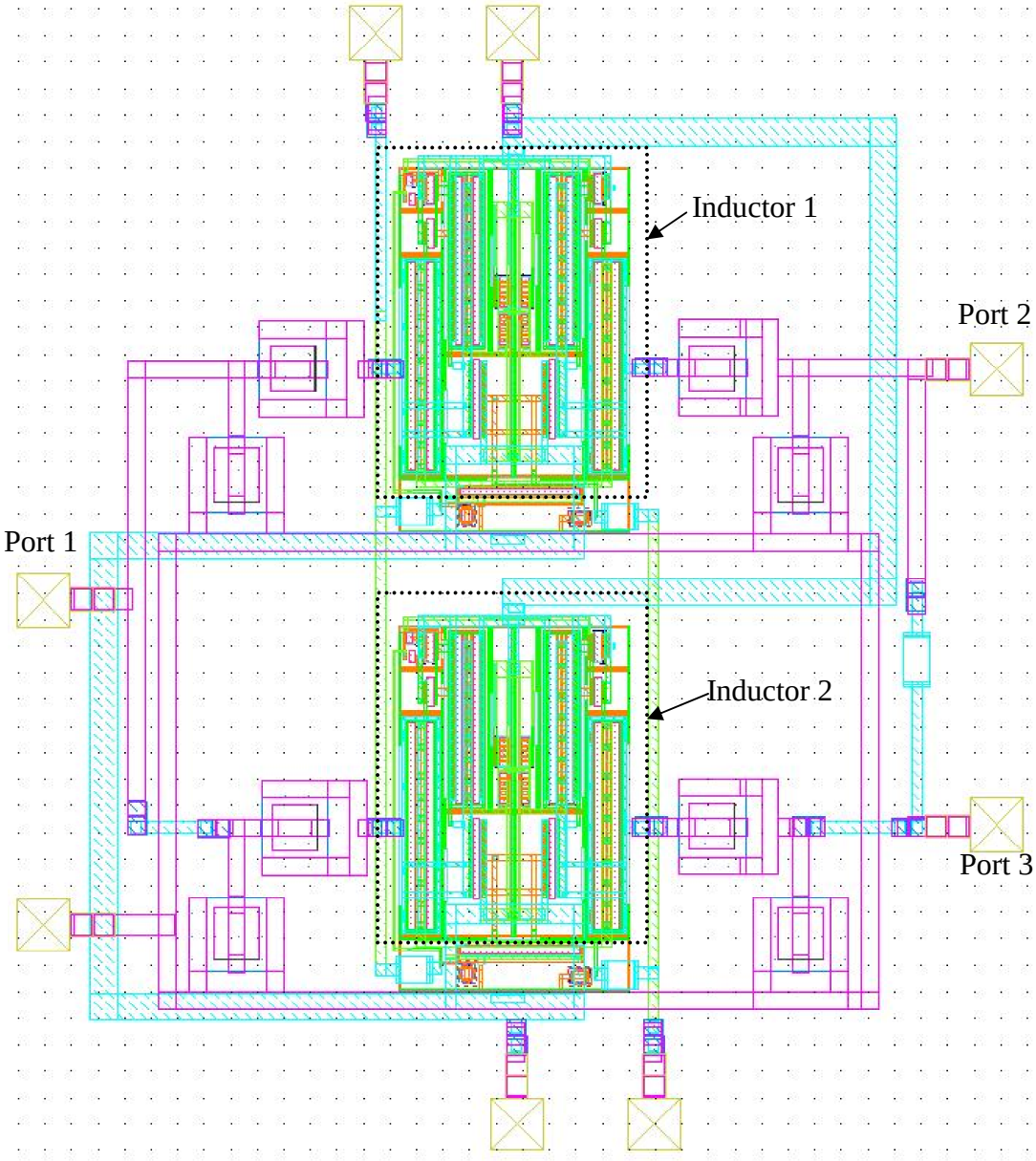

Fig 3.8. Layout of the power divider

For the Wilkinson power divider, when the input signal amplitude is 50 mV, all ports matched to 50 ohms, and with a 1.2 V standard power supply, the S-Parameters are

shown in Fig 3.9. It is shown that the output ports are well isolated and all the ports are well matched.

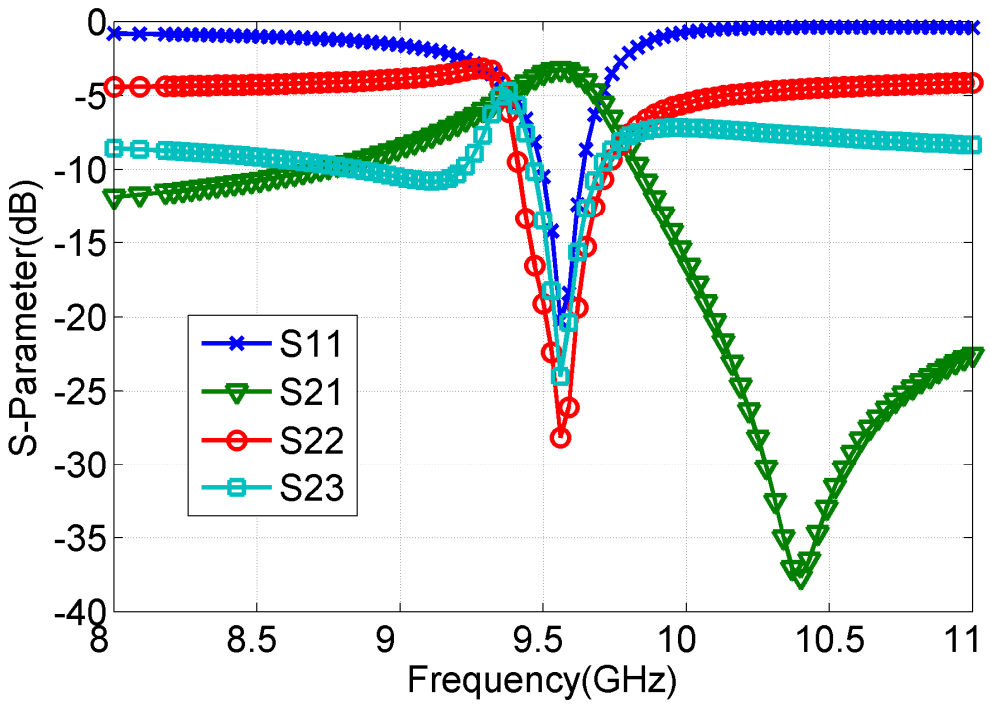

Fig 3.9. The S-Parameters of the Wilkinson power divider.

IV. CONCLUSIONS

This paper presents a novel differential active inductor that operates from 300 MHz to 10 GHz. The inductor is used to design a Wilkinson power divider at 9.5 GHz. Post layout simulations show that the power divider works well at about 9.6 GHz, ~ 0.1 GHz shift compared to the original design. In addition to its high self-resonance

frequency (up to 10 GHz), the inductor is tunable from 300 MHz to 10 GHz, which can be used in the broadband designs.

ACKNOWLEDGMENT

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CHAPTER FOUR

A CMOS RADIO FREQENCY POWER DIVIDER TUNABLE FROM 1-7.5 GHZ

***Abstract*--A new lumped-element power divider circuit is proposed for on-chip implementation. The circuit is compact and insensitive to losses in varactors and inductors compared with existing power divider architectures. Measurement results of a differential active inductor targeted for tunable power divider applications are presented. The inductor is tunable from 500 MHz to 5 GHz with inductance value tunable from 0.9 nH to 5 nH. The self-resonance frequency of the inductor is as high as 6 GHz. A quality factor value of 101 at 2 GHz is obtained. After adding a coupled inverter pair to improve circuit bias and quality factor, the self-resonance frequency is boosted to 10 GHz, which is demonstrated by post layout simulation. With the improved inductor, the proposed power divider is designed in a 0.13 µm CMOS process. The center frequency of the power divider is tunable from 1 GHz to 7.5 GHz with all three ports matched to 50 Ω. In the entire operating frequency range, the return loss is better than 20 dB and insertion loss is about 4 dB. The circuit dissipates 6.17 mW to 21.05 mW when it is tuned from 1-7.5 GHz with a standard 1.2 V power supply. The core area of the power divider is 300 µm×265 µm.**

I. INTRODUCTION

Power divider is a basic circuit module for microwave systems, including various six-port network analyzer architectures [4.1]. Fig. 4.1(a) shows the basic circuit schematic that was developed by Wilkinson [4.2]. The three-port network divides an input into two identical output signals while providing isolation between the two outputs. For integrated radio-frequency (RF) systems and their applications, lumped-element implementation of the circuit, such as the circuits in Fig. 4.1(b) and (c), is necessary despite the efforts in developing compact on-chip transmission lines to overcome chip-area constraints [4.3]-[4.4]. The bandwidth of the circuits in Fig. 4.1 is narrow. Multiple-stage power dividers have been proposed to overcome this limitation [4.5]-[4.7], which would result in larger chip area and higher signal loss for on-chip applications since there is parasitic resistor in on-chip passive inductors. Meanwhile, rather than a wide instantaneous bandwidth, the operating frequency tuning range is of great interest for some applications, such as software-defined radio [4.8]-[4.9] and six-port network analyzers, because narrower instantaneous bandwidth may help improve the sensitivity of the system. Thus far, efforts on tunable RF power dividers are limited, although a 4 GHz to 5 GHz design was published in [4.10].

Tunable (active) inductors and variable capacitors (varactors) are two basic elements in implementing tunable power dividers for a given embedding impedance (e.g. 50 Ω). Varactors are often available from process vendors. However, on-chip varactors have limited quality factors. The associated parasitic resistance seriously affects the performance of various lumped-element power divider structures, as discussed in Section

II. On the other hand, tunable inductors are active research topics. Therefore, power divider circuits need to be analyzed with attention to varactors and inductor losses.

In this work, we propose a new lumped-element tunable power divider for CMOS implementation. Section II shows that the proposed power divider is the most compact and least sensitive to varactors loss. The measured results of an inductor tunable from 500 MHz to 5 GHz are given in Section III. The inductor can be used in the proposed power divider circuit but the self-resonance frequency is still not high enough for the desired tuning range. An improved active inductor structure is also given and discussed. Section IV describes the design of a tunable power divider in a CMOS 0.13 µm process with post layout simulation results. Section V concludes this chapter.

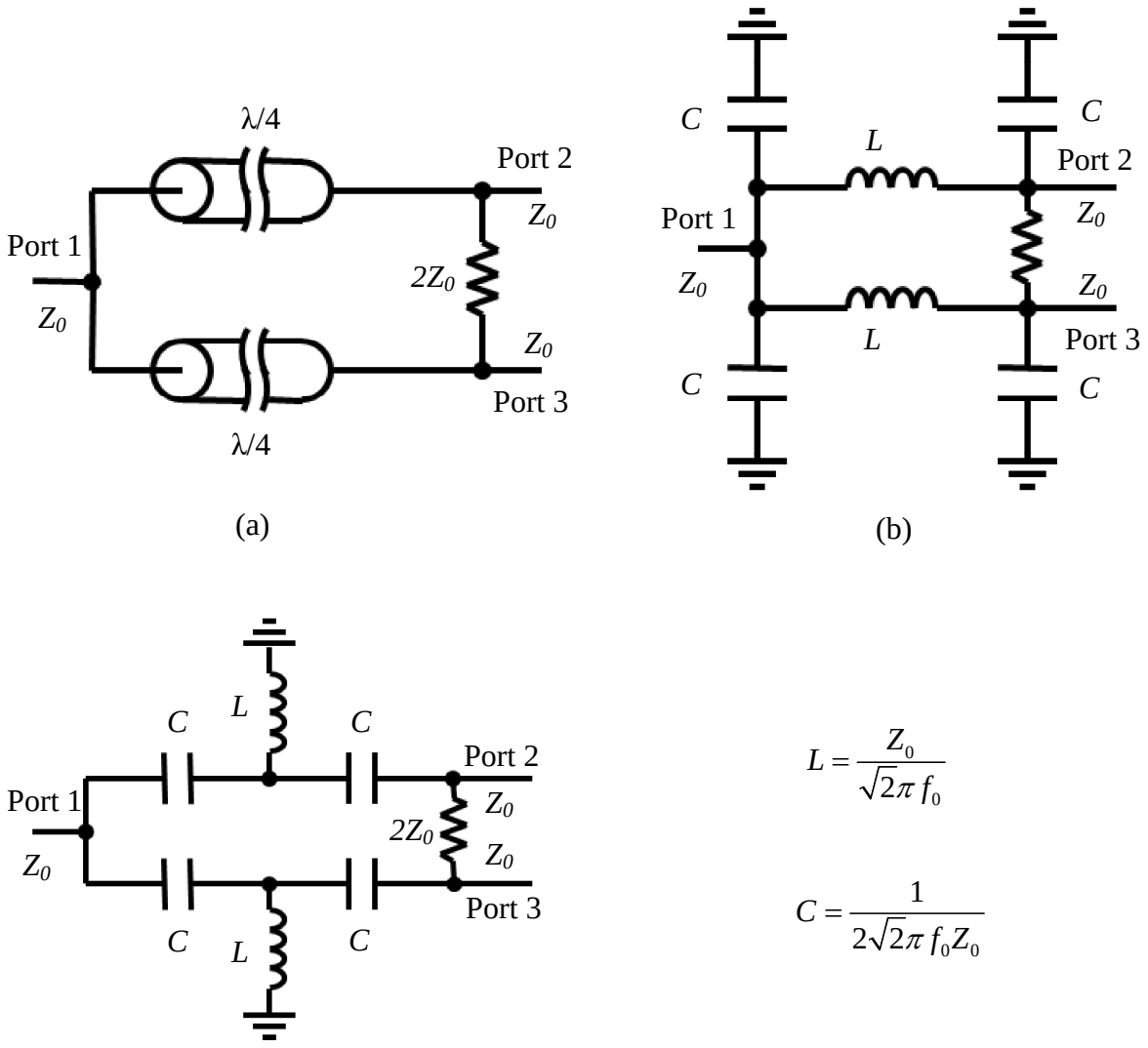


Fig. 4.1. Wilkinson power divider circuits with (a) two *λ/4* distributed transmission lines, (b) lumped-element equivalent π-network of the transmission lines, (c) lumped-element T-network. Z_0 is reference characteristic impedance.

II. A NEW LUMPED-ELEMENT POWER DIVIDER

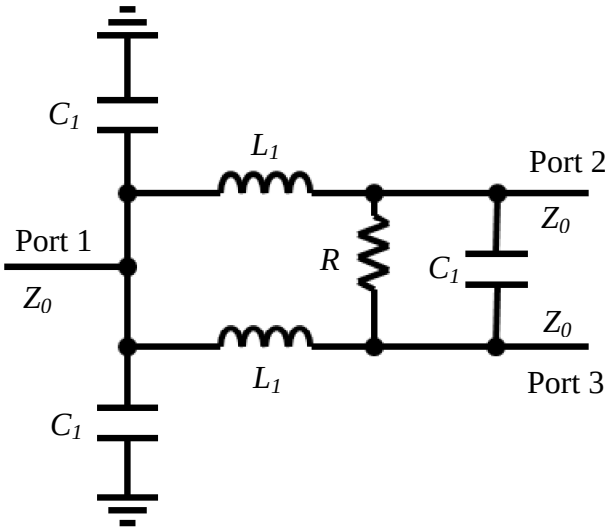
The proposed power divider is shown in Fig. 4.2(a) together with circuit component parameters (the analysis of the parameters is shown in Appendix A.). Figs.

4.2(b) and (c) are two power divider circuits recently presented in [4.11]. They are the most compact power divider circuit architectures published so far. The proposed circuit in Fig. 4.2(a) uses the same number of circuit components with similar element values (the two capacitors at port one can be combined together). As a result, the corresponding chip area is similar to those in Fig. 4.2(b) and (c). Table I shows that Fig. 4.2(a) also has a bandwidth similar to that of the other two when ideal inductors and capacitors are used.

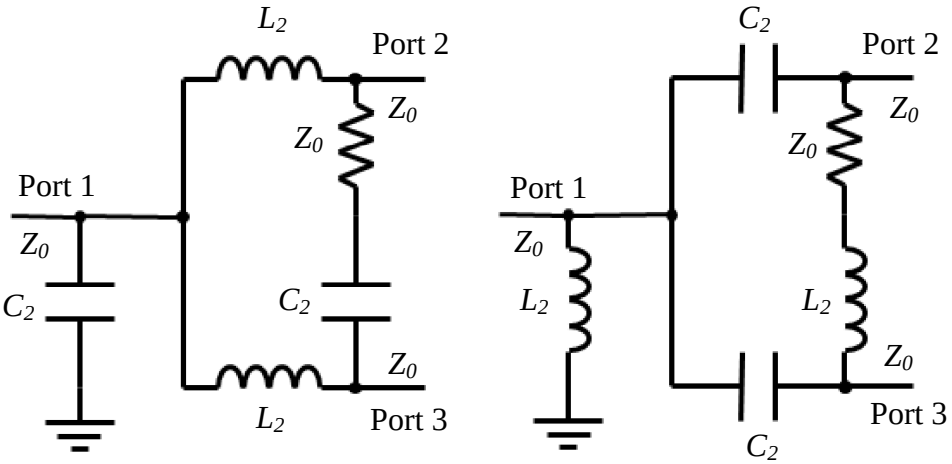
TABLE 4.1 Operating Frequency Bandwidth $\Delta f/f_0$

Fig.4.1(a)	Fig.4.1(b)	Fig.4.1(c)	Fig.4.3(a)	Fig.4.3(b)	Fig.4.3(c)
0.36	0.16	0.16	0.26	0.28	0.29

Δf is the frequency range that has -20 dB or better isolation and all three ports are matched. The center frequency f_0 is 1 GHz.



(a)



(b) (c)

Fig. 4.2 (a) the proposed power divider circuit. (b) and (c) are two compact power dividers proposed in [4.11].

In the figure

$$L_1 = \frac{Z_0}{2\pi f_0}, \tag{4.1}$$

$$C_1 = \frac{1}{4\pi f_0 Z_0}, \tag{4.2}$$

$$L_2 = \frac{Z_0}{2\pi f_0}, \text{ and} \tag{4.3}$$

$$C_2 = \frac{1}{2\pi f_0 Z_0}. \tag{4.4}$$

As discussed above, losses are inevitable for both varactors and inductors in CMOS technologies. It is possible to independently tune the inductance and quality factor (loss) of an active inductor. But there is no efficient approach to independently control the capacitance and resistance of a varactor for different frequency operations until now [4.12]. Therefore, these power divider circuits need to be analyzed and compared with losses considered, especially varactor's losses.

The even-odd mode method [4.13] can be applied for such analysis. Unfortunately, the addition of loss resistance makes the algebraic process and the final equations lengthy and complicated. Therefore, only the varactor's resistance effects in Fig. 4.2(a) and Fig. 4.2(b) are presented here. The performance of Fig. 4.2(c) is similar to that of Fig. 4.2(b), as will be shown in Fig. 4.4.

For even-mode operation, the circuits in Figs. 4.2(a) and (b) have identical equivalent circuits. Therefore, varactor's resistance should have similar effects. For the odd mode operation, however, different equivalent circuits arise, as shown in Figs. 4.3 (a)-(d). The impedance between node Port2 and ground for the circuit of 4.3(a) can be written as

$$R_A = Z_0\left(1+\frac{Z_0(\omega_0+\Delta\omega)^2 R_1}{(\omega_0+\Delta\omega)^2 R_1^2+\omega_0^2 Z_0^2}\right)^{-1} \text{ and} \tag{4.4}$$

$$X_{PA} = \frac{1}{(\omega_0+\Delta\omega)C_A} = \frac{\omega_0 Z_0}{\omega_0+\Delta\omega} + \frac{(\omega_0+\Delta\omega)R_1^2}{\omega_0 Z_0}\ , \tag{4.5}$$

while for the circuit of 4.3(b)

$$R_B = \frac{Z_0}{2} + R_2 + \frac{\omega_0^2 Z_0^2}{2(Z_0+2R_2)(\omega_0+\Delta\omega)^2}\ \text{, and} \tag{4.6}$$

$$X_{PB} = \frac{1}{\omega C_B} = \frac{\omega_0 Z_0}{2(\omega_0+\Delta\omega)} + \frac{\omega_0 Z_0^3}{2(\omega_0+\Delta\omega)(Z_0+2R_2)^2}\ . \tag{4.7}$$

Here $\omega = \omega_0+\Delta\omega$ with the operating center frequency $\omega_0=2\pi f_0$ and $\Delta\omega$ the frequency off-set. Ideal operations require R_A and R_B to be Z_0, which is the case when R_1, R_2 and $\Delta\omega$ are zero. Otherwise, matching to the embedding impedance will not be satisfied. Furthermore, the minimum points of scattering parameters do not overlap, as one can see in Fig. 4.4(a). Therefore, weaker dependence of R_A and R_B on frequency shift is desired. From equations (4.4) and (4.6), $\frac{\partial R_B}{\partial\Delta\omega}/\frac{\partial R_A}{\partial\Delta\omega}$ varies from 1.125 to 6.3 at 1 GHz when R_1 and R_2 changes from 4 Ω to 30 Ω which is the simulation range.

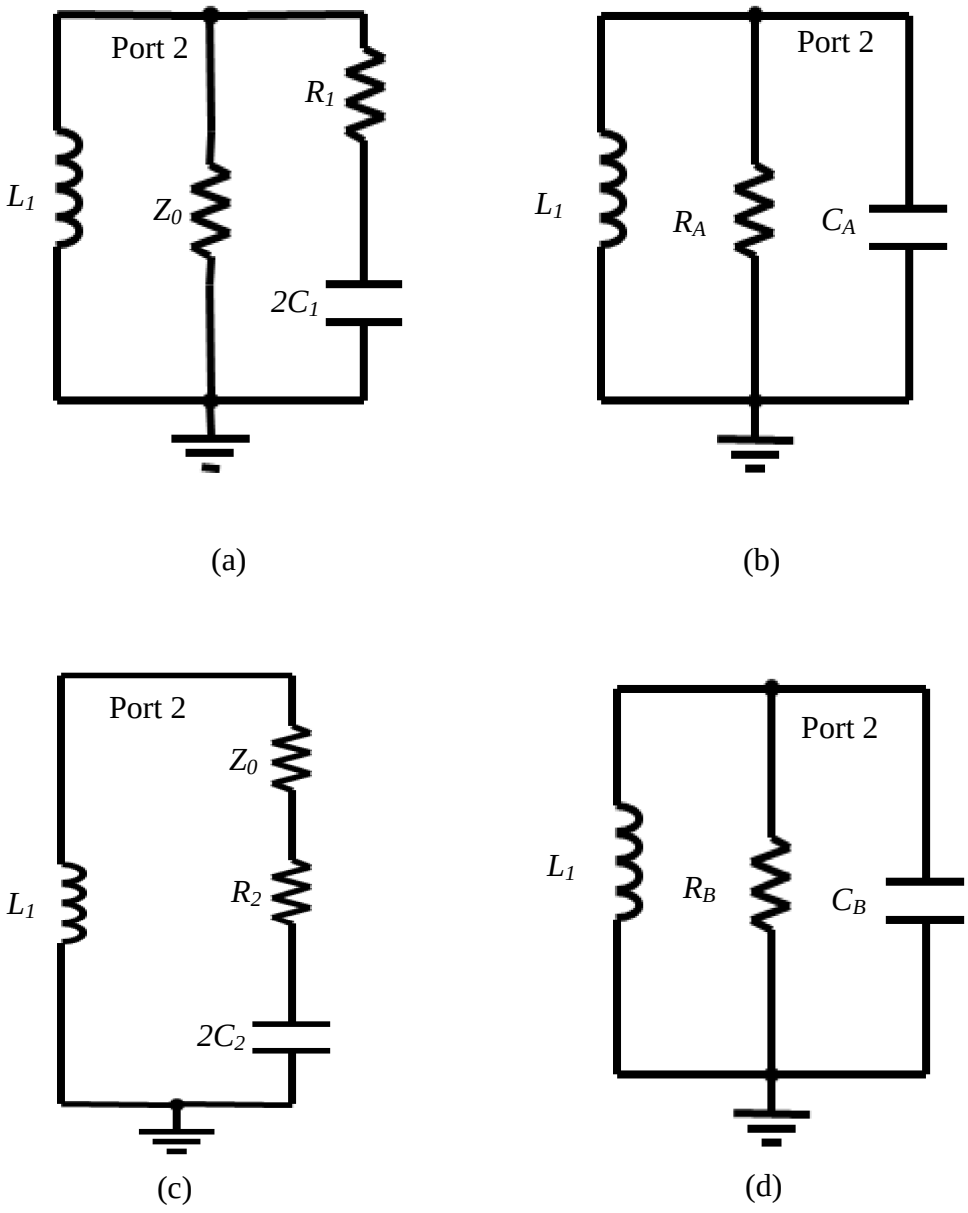
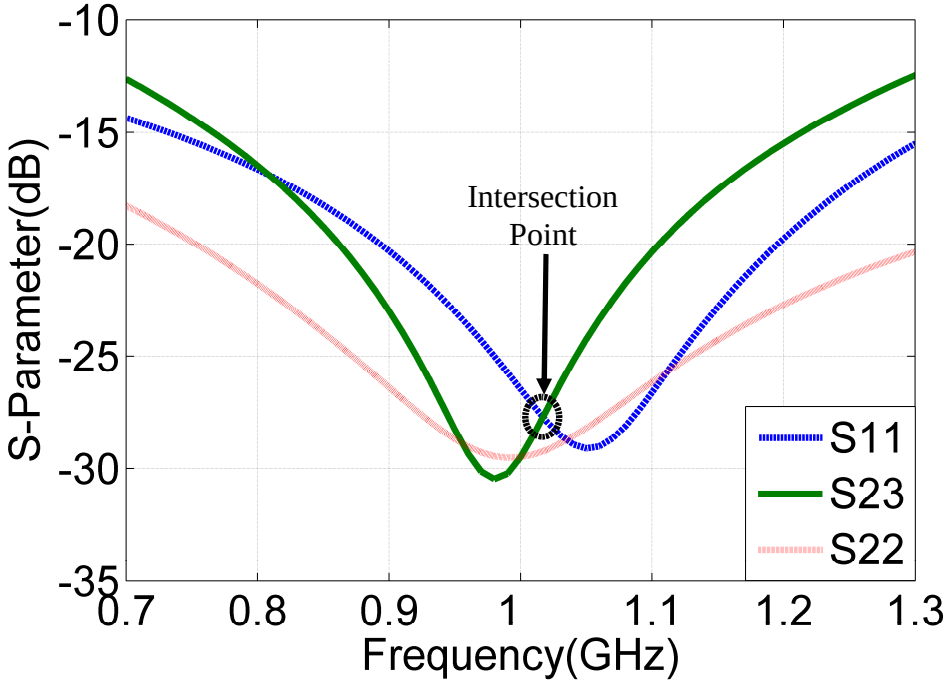
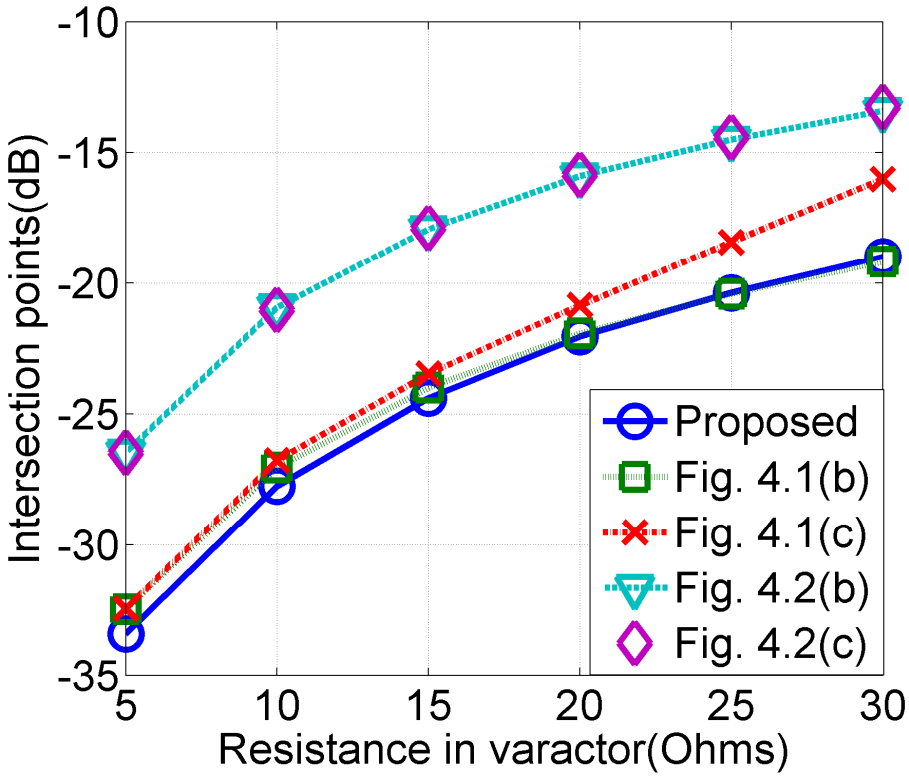


Fig. 4.3 (a) Equivalent circuit for odd mode operation of Fig. 4.2(a), R_1 is parasitic resistor of the varactor $2C_1$. Excitation source is not shown. (b) Equivalent circuit of (a). (c) Odd mode excitation of Fig. 4.2(b), R_2 is the parasitic resistor of the varactor of $2C_2$. (d) Equivalent circuit of (c).

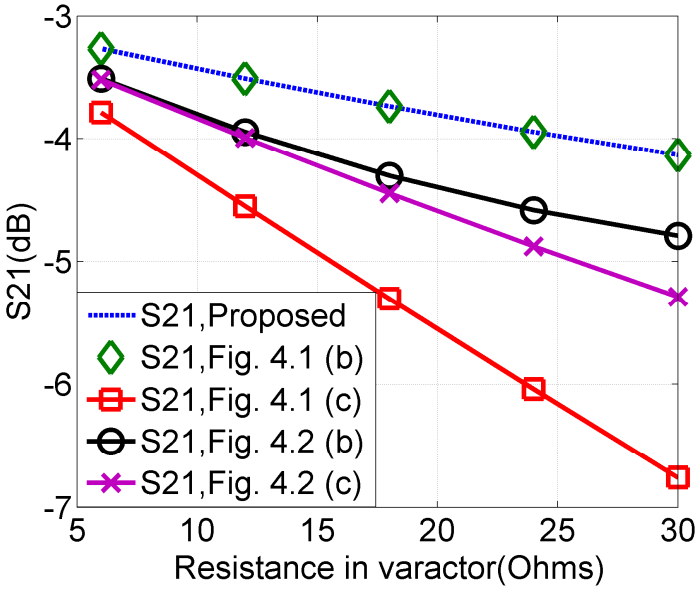
Simulation results for scatting parameter using Cadence Spectre and ADS are shown in Fig. 4.4. The results for the two simulators are identical. The circle in Fig. 4.4(a) shows the highest intersection point among reflection and isolation scattering parameters in the operating band. This point represents the best simultaneous minimum of the three parameters shown and hence the best possible performance of the power divider. Fig. 4.4(b) indicates the dependence of the intersection point on varactor's resistance for different power divider structures at 1 GHz. The proposed structure is the least sensitive to increase of the varactor's resistance. Figs. 4.4(c) shows the magnitude of transmission coefficients, S_{21}, for different resistance of varactor. Fig. 4.4(d) also shows the dependence on the inductor's resistance. The above analysis and the results in Fig. 4.4 show that the proposed power divider circuit is much less sensitive to the losses in inductors and varactors among all the power divider circuits in Figs. 4.1 and 4.2. Therefore, it is a better choice for on-chip implementation.


-10
-15
-20
-25
-30
-35
S-Parameter(dB)
0.7
0.8
0.9
1
1.1
1.2
1.3
Frequency(GHz)
Intersection
Point
S11
S23
S22

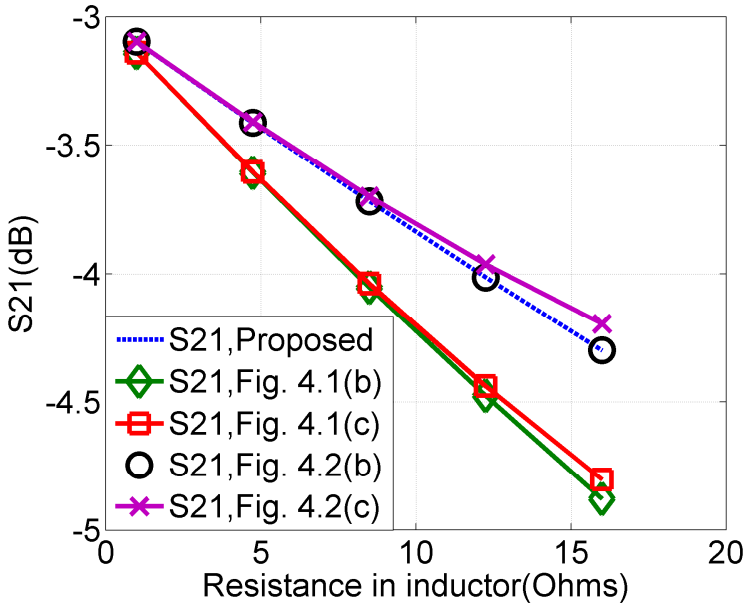
(a)


-10
-15
-20
-25
-30
-35
Intersection points(dB)
5
10
15
20
25
30
Resistance in varactor(Ohms)
Proposed
Fig. 4.1(b)
Fig. 4.1(c)
Fig. 4.2(b)
Fig. 4.2(c)

(b)



(c)



(d)

Fig. 4.4 (a) The highest intersection point of S_{11}, S_{22}, and S_{23}. (b) Intersection point value vs. parasitic resistance in varactors. (c) S_{21} vs. parasitic resistance in varactors at the designed center frequency. (d) S_{21} vs. parasitic resistance in inductor at the designed center frequency.

S-Parameters of the proposed structure at center frequency can be obtained when varactor's resistances are considered. A detailed derivation is shown in Appendix B and the results are summarized as follows:

$$S_{11} = \frac{(-1+j)R_1^2 - 2(1+j)R_1 Z_0}{(3+j)R_1^2 + 8(1+j)Z_0^2 + 2(1+j)R_1 Z_0} \approx \frac{-R_1}{4Z_0 + R_1} \tag{4.8}$$

In the even mode, the reflection coefficient at Port 2 is

$$\Gamma_2^e = \frac{(1+j)Z_0 R_1^2 - 2(1-j)R_1 Z_0^2}{8(1+j)Z_0^2 + (3+j)R_1^2 + 2(1+j)R_1 Z_0^2}. \tag{4.9}$$

In the odd mode, the reflection coefficient at Port 2 is

$$\Gamma_2^o = \frac{jR_1^2 - R_1 Z_0}{2Z_0^2 + (2-j)R_1^2 + R_1 Z_0}. \tag{4.10}$$

Then

$$S_{22} = \frac{1}{2}(\Gamma_2^e + \Gamma_2^o), \tag{4.11}$$

which can be simplified to

$$S_{22} = S_{33} \approx \frac{1}{2}\left(\frac{-(1-j)R_1}{(1+j)R_1 + 4(1+j)Z_0} + \frac{-R_1}{R_1 + 2Z_0}\right). \tag{4.12}$$

The expression for S_{21} is complicated but can be simplified to the following (seen in Appendix B):

$$S_{21} = S_{12} \approx \frac{8Z_0 + 4R_1}{8(1+j)Z_0 + (3+5j)R_1}. \tag{4.13}$$

Finally,

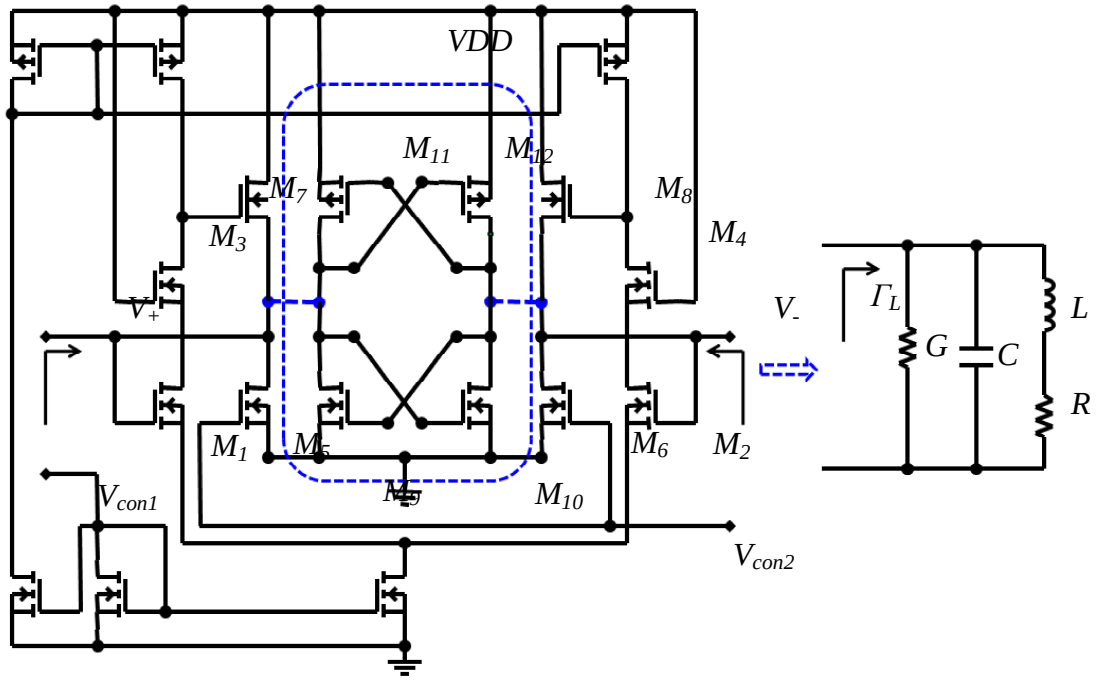
$$S_{23} = S_{32} = 0 \tag{4.14}$$

Equations (4.8)-(4.14) show that when R_1 is zero, the proposed power divider is matched at all ports with ideal isolation between Port 2 and 3. The phase delay between Port 1 and Port 2 or Port 3 is 45 degrees, not 90 degrees.

III. Active Inductors Design

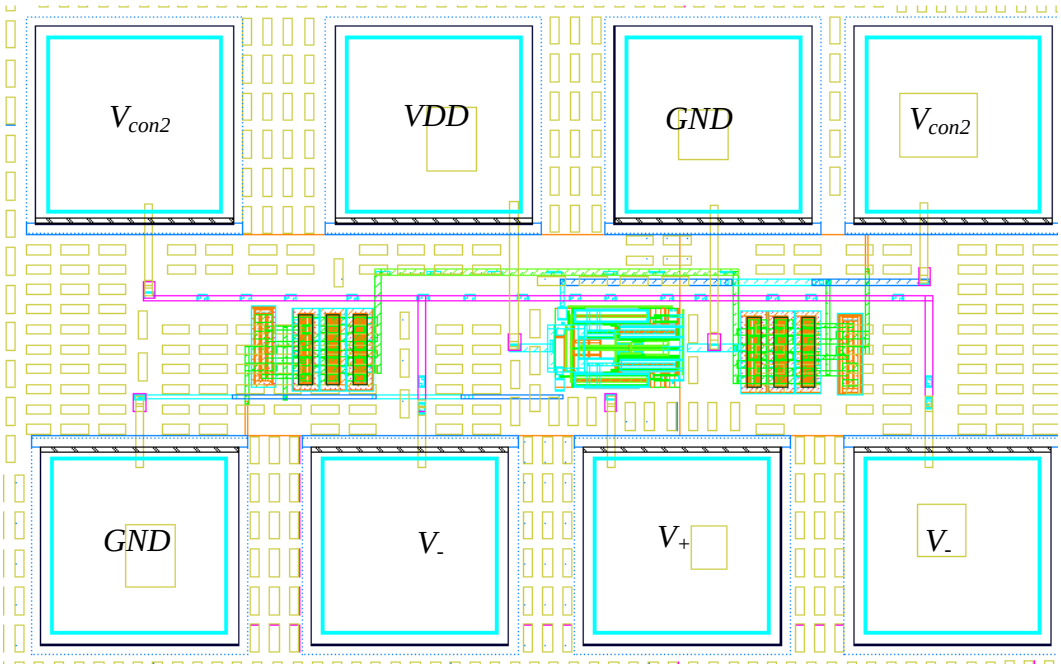
The two inductors in Fig. 4.2(a) need to have a wide tuning range in order for the power divider to be tunable over similar ranges. Active differential inductors are probably the only choice. High quality factor and high self-resonance frequencies are desired. Two of such inductors are shown in Fig. 4.5(a), with or without the coupled inverter pair in the dashed rectangle. Without the coupled inverter pair, the circuit is a gyrator-C type active inductor, hereafter referred to as type A inductor, with an estimated inductance value in equation (4.15) below. The inductor is tuned by tuning g_{m1} and g_{m7}. Fig. 4.6(a) and (b) shows the layout and the photo of this inductor implemented in a 0.13 μm CMOS process. The measured results for the inductor in Fig. 4.6(c) show a 6 GHz self-resonance frequency, which is close to Cadence simulation predictions. The inductance value can be tuned from 0.9 nH to 5 nH over a 500 MHz to 5 GHz frequency range. The maximum inductance value is 53.38 nH. When the self-resonance is 3.1 GHz, the Q value is 101 at 2 GHz. When V_{con1}= 0.65 V and V_{con2}=0.55 V, the measured inductance and quality factor are shown in Fig. 4.7.

$$L \propto \frac{C_{gs,M_7}}{g_{m1} g_{m7}} \tag{4.15}$$

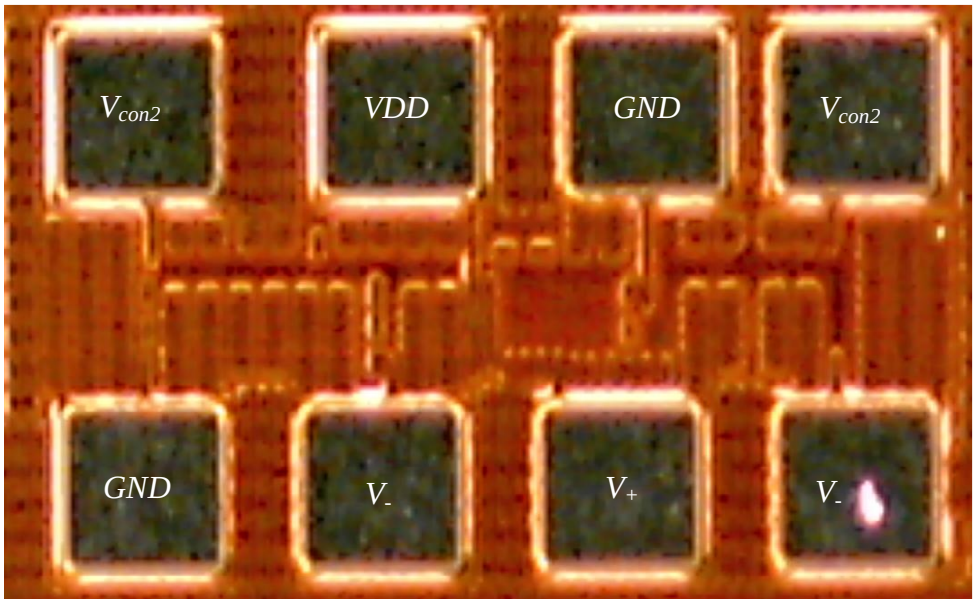


(a) (b)

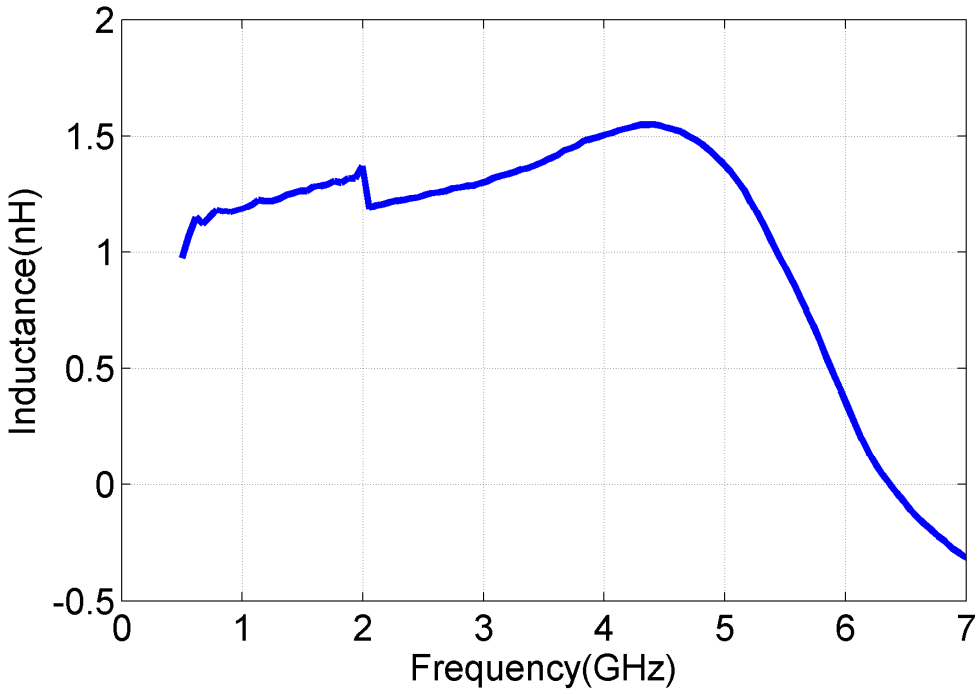
Fig. 4.5 (a) Schematic of two active inductors. The dashed rectangle encircles a coupled-inverter pair. Without it, the inductor is referred to as type A. With it, the inductor is type B. (b) Equivalent circuit of type B.



(a)



(b)



(c)

Fig. 4.6. (a) Layout of type A inductor (b) The micrograph of (a) implemented in a 0.13 µm CMOS process. (c) Measured inductance with 6 GHz self-resonance frequency. The inductance is measured between V_+ and V_- nodes by use of an HP 8510C network analyzer.

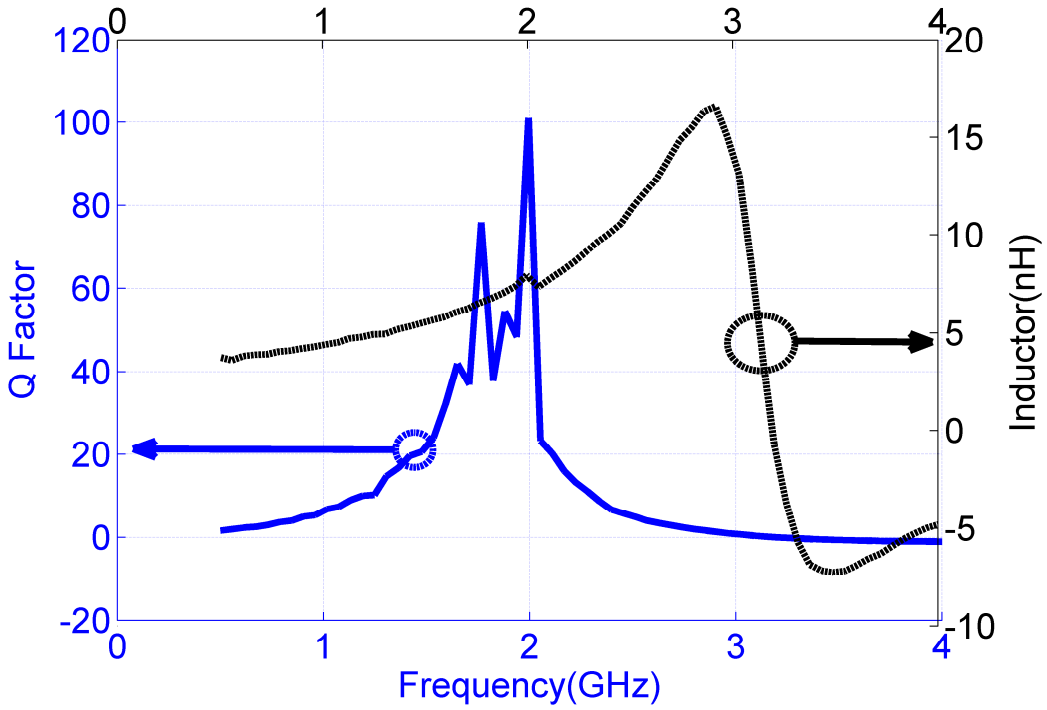


Fig. 4.7. Measured inductance and Q factor of type A inductor between V_+ and V_- nodes by HP 8510C. V_{con1}=0.65 V, V_{con2}=0.55 V and Vdd=1.2 V.

Although the measured frequency tuning range of the inductor in Fig. 4.6(a) is the largest among active inductors reported so far, higher operating frequency range is desired. The frequency limitation in Fig. 4.6(a) is mainly caused by the DC biasing condition of transistors M_1 and M_2. When g_{m7} (or g_{m8}) changes, g_{m1} (or g_{m2}) will change in the opposite direction, because the DC biases of the transistor $M_{1,2}$ are supplied by the drain voltage of $M_{5,6}$. When g_{m7} (g_{m8}) increases by increasing V_{con2}, the DC bias at the gates of $M_{1,2}$ decreases and they may even enter the cut-off regions (g_{m1} and $g_{m2}\approx 0$), then this circuit ceases functioning and will not yield the inductor characteristics. On the other hand, when g_{m7} (g_{m8}), decreases by lowing V_{con2}, the DC bias at the gates of $M_{1,2}$ will increase automatically. Therefore, g_{m1} (or g_{m2}) and g_{m7} (or g_{m8}) are dependent, so stable

DC biases for $M_{1,2}$ are needed. With some brief discussions in [4.14], we proposed to add the coupled inverter pair in Fig. 4.5 to form a new active inductor, type B. The addition of the coupled inverter pair improves the DC bias conditions of the circuit, and simultaneously provides negative resistors to increase the Q factor of the inductor.

Small signal analysis yields equivalent circuit parameters of the improved inductor structure. Expressions (4.17) to (4.22) below, help guide the design of the inductor.

$$G = \frac{1}{R_5} + \frac{1}{R_7} + \frac{1}{R_9} + \frac{1}{R_{11}} - g_{m5} - g_{m9} - g_{m11} \tag{4.17}$$

$$C = C_{in} \tag{4.18}$$

$$L \approx \frac{C_1C_3 + C_1C_L + C_LC_3}{g_{m1}g_{m7}C_3} \tag{4.19}$$

$$R \approx \frac{C_1(\frac{1}{R_3} + \frac{1}{R_L}) + C_3(\frac{1}{R_L} + \frac{1}{R_1}) + C_L(\frac{1}{R_1} + \frac{1}{R_3} + g_{m3})}{g_{m1}g_{m7}C_3} \tag{4.20}$$

$$Q \approx \frac{\sqrt{LC}}{(R^2 + R)C + LG} \tag{4.21}$$

$$\omega_0 = \sqrt{\frac{1}{LC}}\sqrt{1 - \frac{CR^2}{L}} \tag{4.22}$$

C_{in} is the parasite capacitance at the input point. C_1 is the parasite capacitance between node ***1*** and ground; C_3 is the parasite capacitance between node ***2*** and node ***1***. R_L and C_L are the resistance and capacitance between node ***2*** and ground. g_{mi} and R_i are the transconductance and channel resistance of transistor M_i. The introduction of the cross coupled inverter pair will reduce G in (4.17). Equation (4.18) shows that capacitance *C* increases due to the introduction of this inverter pair. Equations (4.19) and (4.20) indicate that there is little change for *L* and *R* since g_{m1} (or g_{m2}) will not be affected directly by g_{m7} (or g_{m8}) and can be tuned independently to some extent. Then, the inductance can be tuned over a larger range, so higher self-resonance frequency can be obtained according to (4.22).

In the design of the improved active inductor, the main circuit's parameters are shown in Table 4.2. The active area of the improved active inductor is 40 µm×70 µm. The post layout simulation results show better performance than type A in Fig. 4.6(a). The operating frequency is tunable from 300 MHz to 10 GHz and inductance value is tunable from ~1 nH to 100 nH. Fig. 4.8 shows the post layout simulation results of the improved active inductor.

TABLE 4.2 Circuit Parameters of Improved Active Inductor

Transistors	Size(µm/µm)	Transistors	Size(µm/µm)
M_1, M_2	156/0.2	M_7, M_8	39/0.12
M_3, M_4	13/0.12	M_9, M_{10}	13/0.12
M_5, M_6	117/0.18	M_{11}, M_{12}	13/0.12

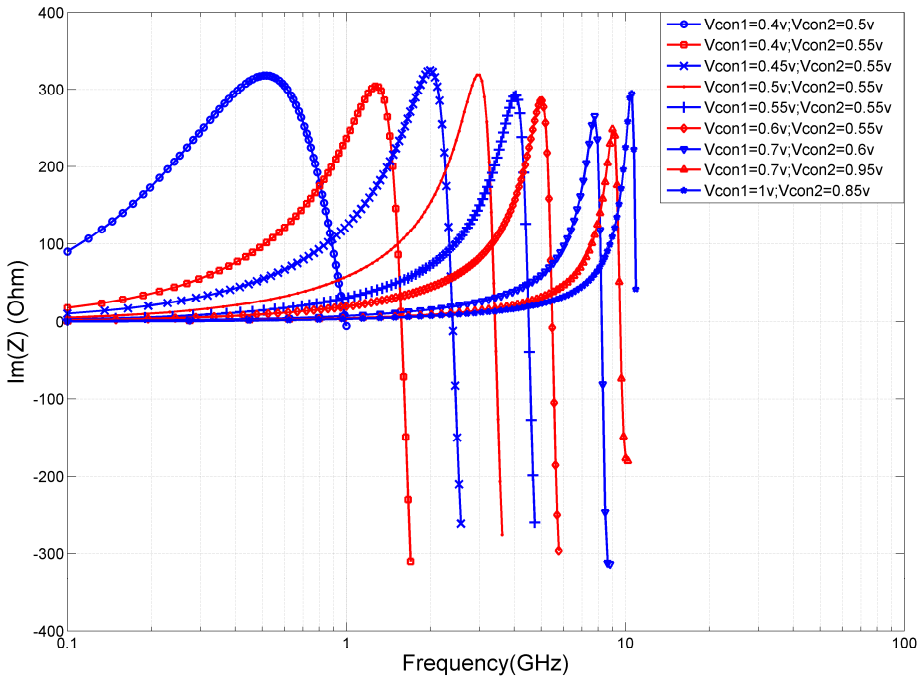


Fig. 4.8. Post layout simulation results of the improved active inductor in Fig. 5(a). Impedance $Z_{in}=1/Y_{in}$.

IV. Power Divider Design and Results

Two improved active inductors are used in Fig. 4.2 (a). Three C_1 are varactors. The Q factor and symmetrical characteristics of C_1 are important. In this design, two C_1 in Port 1 are combined together. The C_1 between Port 2 and Port 3 is separated into identical two varactors and then in parallel but with anode and cathode electrodes switched. The DC biases of the two identical varactors are combined together into V_{ar2} with AC isolation (large resistors). The DC bias of the two combined varactors C_1 is V_{ar1}. The active area of the tunable power divider is 300 µm×265 µm in a 0.13 µm CMOS process and the active area is shown in Fig. 4.9.

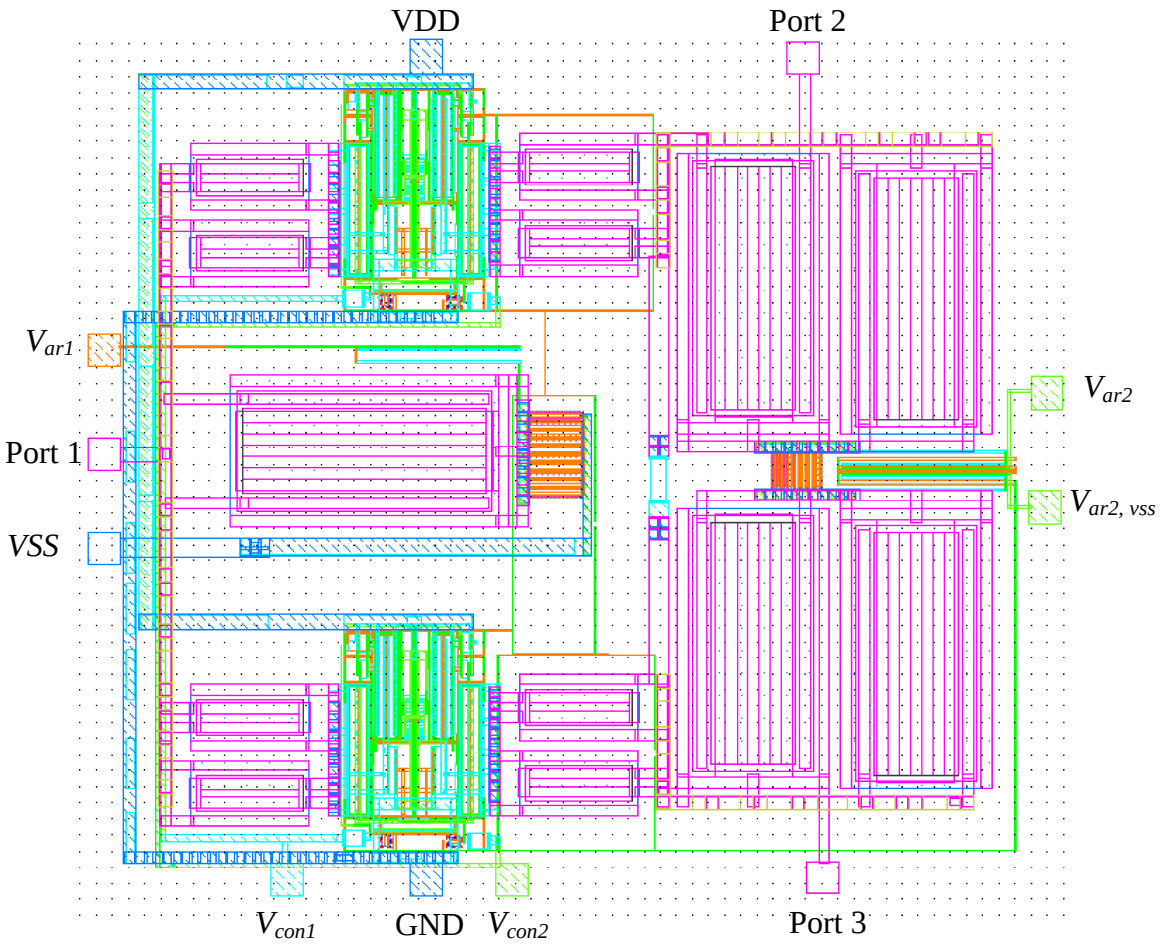


Fig. 4.9 Active area of the tunable power divider in a 0.13 µm CMOS process.

The simulated S_{11} and S_{22} results are shown in Fig. 4.10 from 1 GHz to 7.5 GHz. The valleys of S_{11} and S_{22} nearly coincide at the 1 GHz and 2 GHz, which indicates simultaneous good-match at the ports. As the frequency is increase, the two valleys are progressively separated, which indicates that simultaneous good-match is not possible due to the increase of varactor's resistance. If -20 dB taken as the maximum accepted match condition for all ports, the operating center frequency of the power divider can be

tuned from 1 GHz to 7.5 GHz within this bound. Fig. 4.11 presents the S_{21} parameters under the same conditions. The loss is around 4 dB in the frequency range. In the commercial CMOS technology, the varactor tuning range is limited (the maximum $C_{max}/C_{min}\approx 5$ according the IBM process model) and cannot satisfy the targeted application according equation (4.2). Further expansion of the power divider tuning range requires further work on improving varactor tuning range as well.

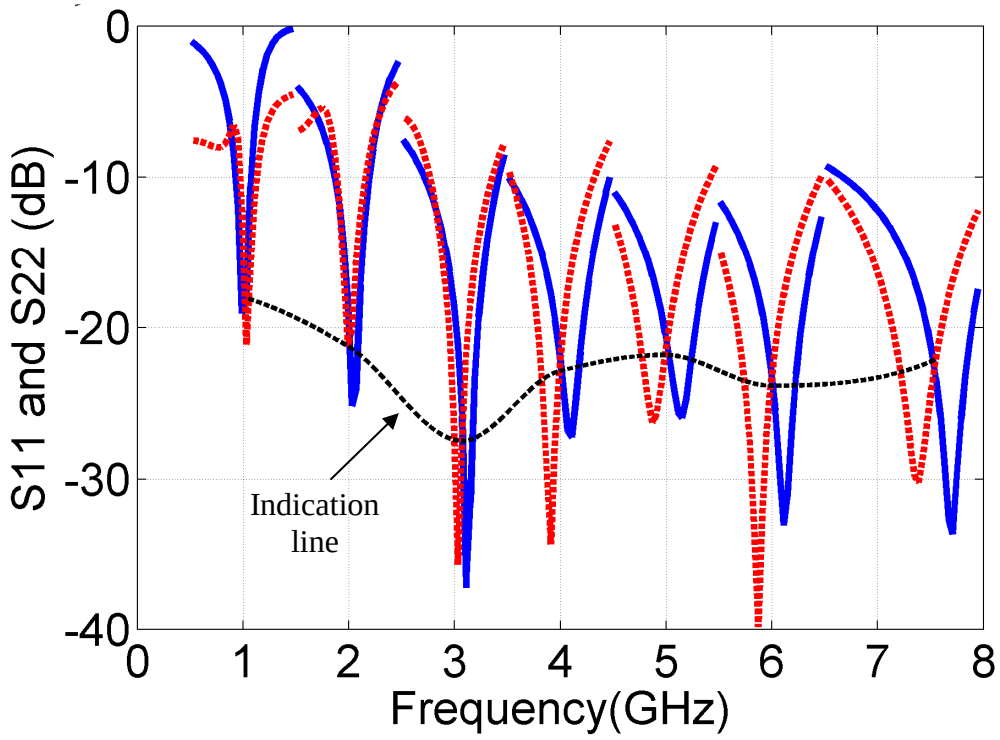


Fig. 4.10. Solid lines and dash lines are S_{11} and S_{22} of the power divider at different operating center frequencies. The dotted line indicates the S_{11} and S_{22} at the operating frequencies.

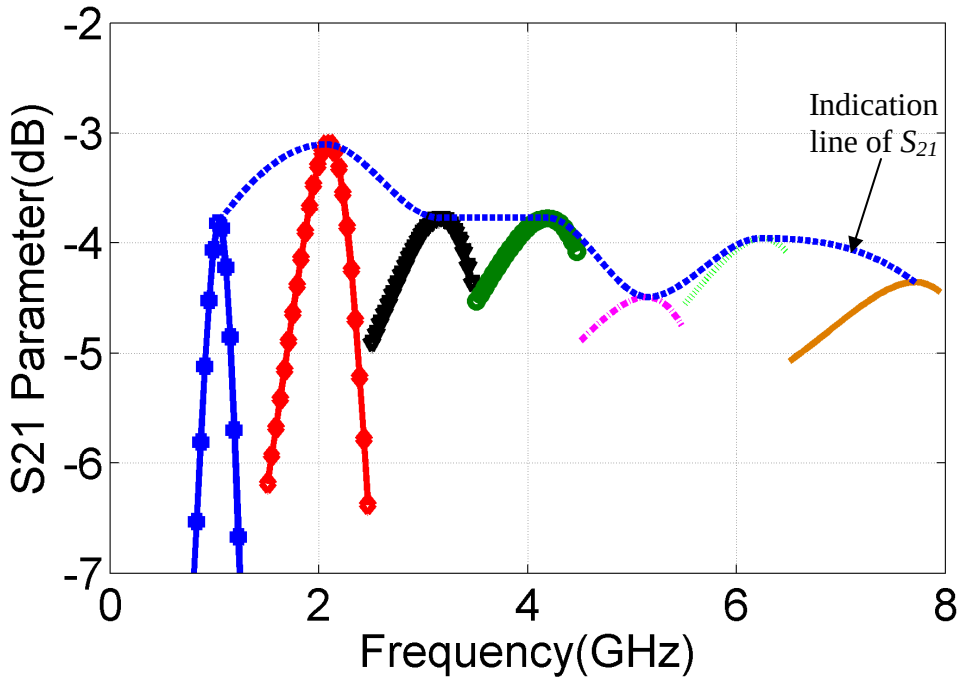


Fig. 4.11. S_{21} of the power divider. The dashed line indicates S_{21} at the operating frequencies.

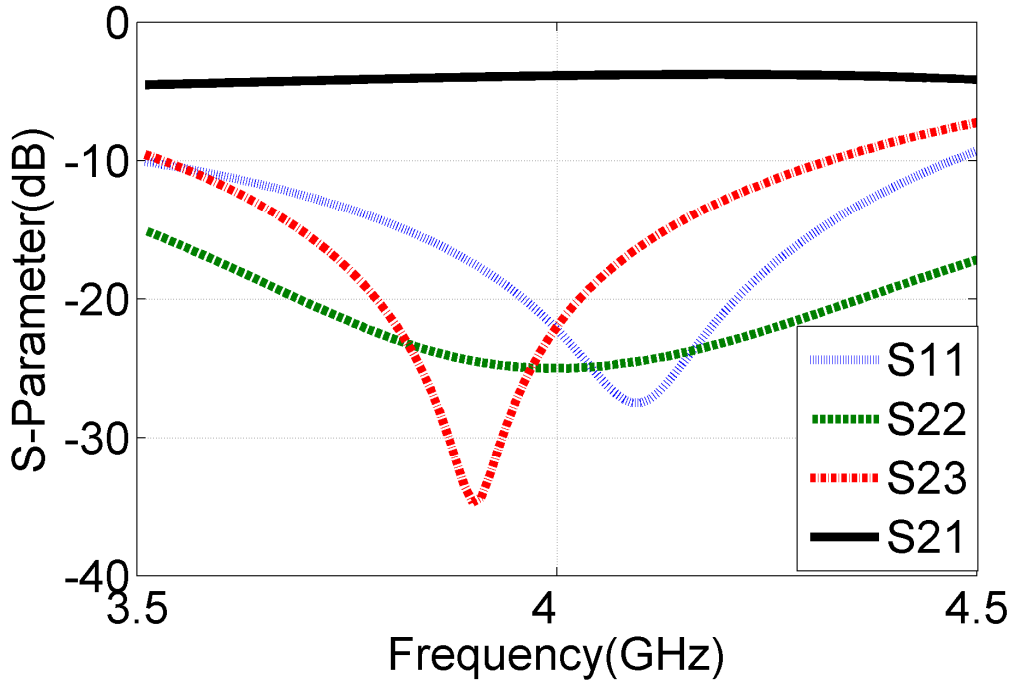


Fig. 4.12 The S_{11}, S_{22}, S_{23} and S_{21} of the power divider at 4 GHz center frequency. V_{con1}=0.67 V, V_{con2}=0.54 V.

V. Conclusions

A new lumped-element compact power divider is proposed and analyzed. Compared with current power divider circuits, the new power divider is least sensitive to the losses of varactors and inductors. A differential active inductor with 6 GHz self-resonance frequency is measured. The measured inductance tuning range is 0.9 nH~5 nH from 500 MHz to 5 GHz. The inductor can be used in the design of the proposed power divider. To further improve the operating frequency range of the inductor, an improved structure is analyzed. The post layout simulation results show a self-resonance frequency as high as 10 GHz. Using the improved inductors and varactors from a commercial 0.13

µm CMOS process, the design of the proposed power divider is tunable from 1 GHz to 7.5 GHz with -20 dB or better match at all ports. To further expand the frequency tuning range, the varactors' tunabilities need to be studied.

Acknowledgements

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CHAPTER FIVE

DISCUSSION AND CONCLUSION

This thesis focuses on extending the frequency range of the possible components for a six-port reflectometer. The second Chapter, the effort is to obtain a broadband source generator, and a voltage-controlled ring oscillator is presented. A sensor amplifier, which can operate at very high frequency, is added to the normal differential amplifier to sharpen the rising and falling edges. Then a three-stage ring oscillator using the proposed oscillator is designed. To extend the frequency range to the low frequency direction, two weak inverter oscillators are added to the differential ring oscillator. The circuit is implemented in a 0.13 µm CMOS process to verify the theory. The measurement tuning range is from 430 MHz to 12 GHz, which satisfies the initial target 1 GHz~10 GHz.

In the third Chapter, a high-Q differential active inductor is proposed to figure out the low self-resonance frequency limitation of the differential active inductor structure. Post layout simulation results show that the inductance is tunable from ~1 nH to 100 nH with operating frequency tunable from 300 MHz to 10 GHz. The inductor is designed in 0.13 µm CMOS process with an area of 40 µm×70 µm. To verify the high frequency performance, a π-model lumped-element power divider is designed with the proposed active inductor at the 9.5 GHz center frequency. The post layout simulation results show that the isolation and matching scatting parameter is better than -20 dB with an insertion loss of ~3dB. The miniaturized Wilkinson power divider occupies 160 µm×170 µm, which is suitable for system integration.

In the forth Chapter, a new compact lumped-element power divider, which is insensitive to the losses in varactors and inductor compared to the existing lumped-element power divider architectures, is proposed and analyzed. Measured results of a differential active inductor, which is targeted for tunable power divider applications, are presented. The inductor is tunable from 500 MHz to 5 GHz with inductance value tunable from 0.9 nH to 5 nH. The maximum self-resonance frequency is 6 GHz, which falls short of the target 1 GHz to 10 GHz. After this structure is improved, the self-resonance is boosted to higher than 10 GHz, which is demonstrated by post-layout simulations. With the improved active inductor, the proposed compact power divider is designed in a CMOS 0.13 µm process with a core area of 300 µm×265 µm.The power divider can be tuned from 1 GHz to 7.5 GHz as demonstrated by posy-layout simulation.

Future work

For the VCO, noise analysis is needed. As for the active inductor, improving the power consumption can be further discussed using the current recycling structure. At present, the tuning range of the power divider is limited by the tuning range of the varactors, which are supplied by the vendor. The other disadvantage of the varactors is the larger effective series resistor (ESR) in the high frequency. Large value ESR seriously distorts the performance of the power divider. The future direction is to find new tunable capacitor structures, which can supply larger tuning range and supply lower ESR in high frequency.

APPENDICES

Appendix A

L, C, R's Derivation for the Proposed Power Divider in Chapter Four

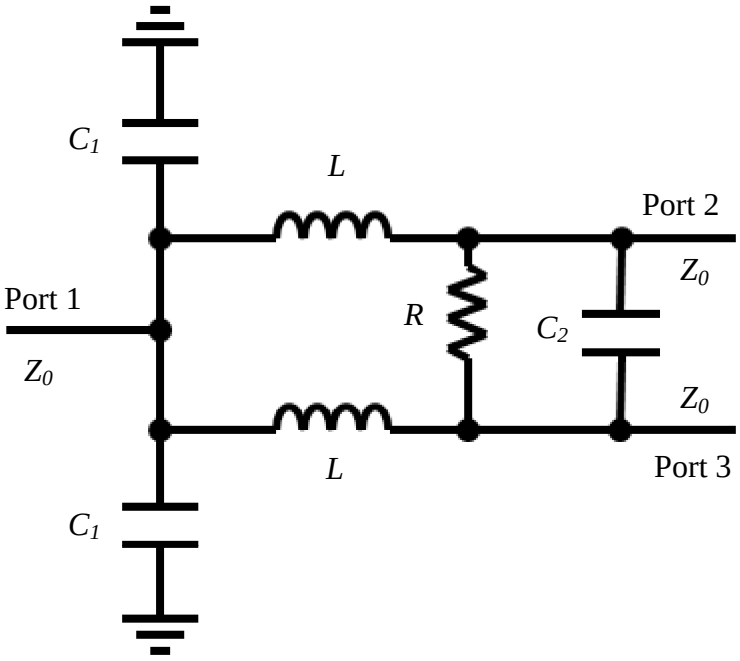

Fig. A.1 Proposed Lumped-Element Power Divider

In 1968, Cohn described an even- and odd-mode technique for analyzing the symmetric two-way power divider [A1.1]-[A1.2] that can be used to determine the circuit parameters for these power dividers. In the even-mode shown in Fig. A.2 (a), for impedance to match a Port 1 and Port 2, the following equation must be fulfilled:

$$\frac{2Z_0 \times \dfrac{1}{j\omega C_1}}{2Z_0 + \dfrac{1}{j\omega C_1}} + j\omega L_1 = Z_0 . \qquad \text{(A1)}$$

Here, ω is the angular frequency of the designed center frequency f_0. In the odd mode shown in fig. 2 (b), for matching at Port 2, equation (A2)

$$\frac{1}{j2\omega C_2 + \frac{2}{R} + \frac{1}{j\omega L_1}} = Z_0 . \qquad \text{(A2)}$$

From (A1) and (A2), the parameters in Fig. A1 can be determined.

$$R = 2Z_0, L_1 = \frac{Z_0}{2\pi f_0} and C_1 = C_2 = \frac{1}{4\pi f_0 Z_0} . \qquad \text{(A3)}$$

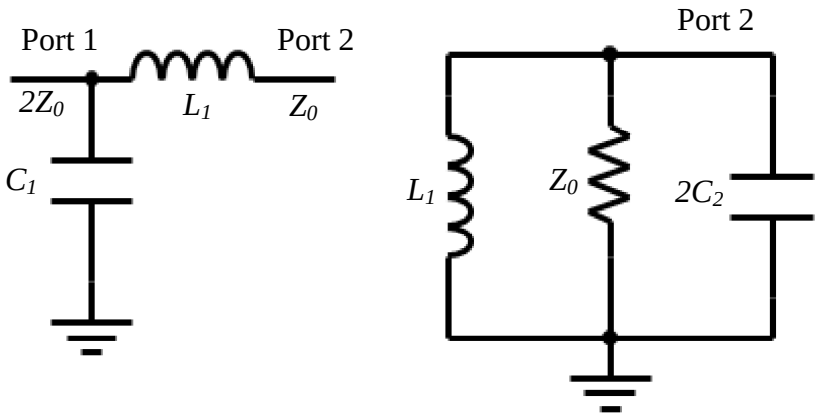

Fig. A2. (a) Even mode circuit for Fig A.1. (b) Odd mode circuit for Fig. A1.

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Appendix B

S-Parameters Derivation for the Proposed Power Divider in Chapter Four

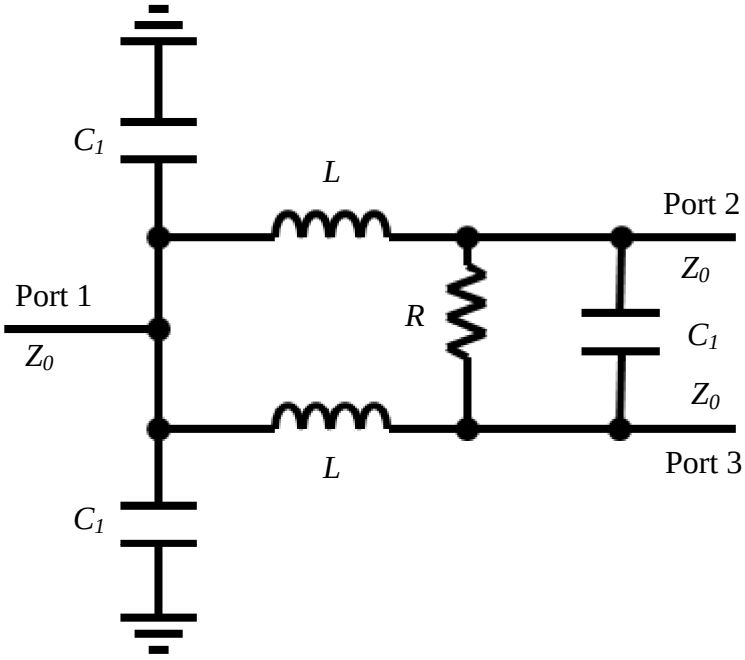

Fig. B1 Schematic of proposed power divider.

According to the even- and odd- mode analysis in Appendix A

$$R = 2Z_0,\ L_1 = \frac{Z_0}{2\pi f_0} \text{and } C_1 = C_2 = \frac{1}{4\pi f_0 Z_0}. \qquad \text{(B1)}$$

If we take the parasitic resistor in the capacitor to be R_1, then the capacitor C_1 is replaced by the series of resistor R_1 and the capacitor C_1 according to the MOSVAR model of [B1.1].

Even-mode analysis

The even-mode schematic appears in Fig B2.

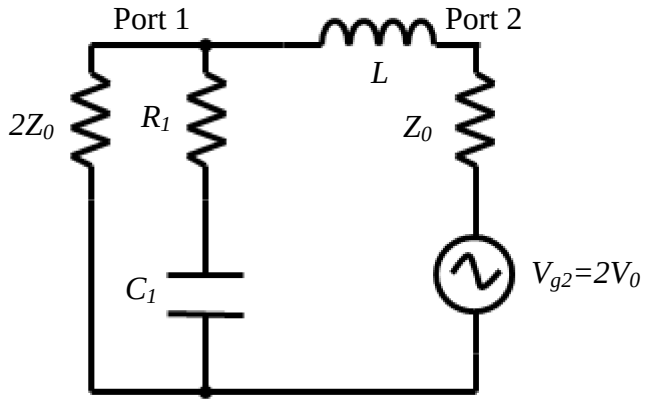

Fig. B2 Schematic of even-mode including parasitic resistor in the capacitor

An equivalent circuit to the circuit Fig B2 is shown in Fig. B3.

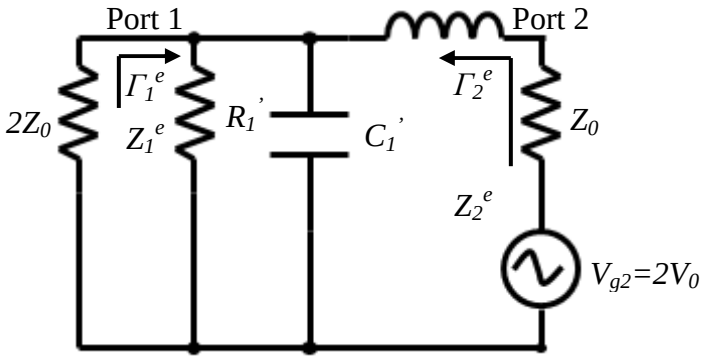

Fig. B3 Equivalent circuit of Fig. B2.

Then the parameter can be determined according [B1.2]:

$$j\omega_0 L = j\omega_0 \frac{Z_0}{\omega_0} = jZ_0, \qquad \text{(B2)}$$

$$\frac{1}{j\omega_0 C_1} = \frac{1}{j\omega_0 \frac{1}{2\omega_0 Z_0}} = -j2Z_0 , \tag{B3}$$

$$\begin{aligned} R_1^{'} &= R_1[1+(\frac{\frac{1}{\omega_0 C_1}}{R_1})^2] \\ &= R_1[1+(\frac{2Z_0}{R_1})^2] \\ &= R_1 + \frac{4Z_0^2}{R_1} \end{aligned} \quad , \tag{B4}$$

$$\begin{aligned} \frac{1}{j\omega_0 C_1^{'}} &= -j2Z_0[1+\frac{1}{(\frac{\frac{1}{\omega_0 C_1}}{R_1})^2}] \\ &= -j2Z_0[1+\frac{R_1^2}{4Z_0^2}] \\ &= -j(2Z_0 + \frac{R_1^2}{2Z_0}) \end{aligned} \quad , \tag{B5}$$

$$\begin{aligned} Z_1^e &= R \,\|\, \frac{1}{j\omega_0 C_1^{'}} \,\|\, (j\omega_0 L + Z_0) \\ &= \frac{1}{\frac{1}{R_1 + \frac{4Z_0^2}{R_1}} + \frac{1}{-j(2Z_0 + \frac{R_1^2}{2Z_0})} + \frac{1}{j\omega_0 L + Z_0}} \\ &= \frac{(1+j)Z_0(R_1^2 + 4Z_0^2)}{(1+j)R_1 Z_0 + 2(1+j)Z_0^2 + R_1^2} \end{aligned} . \tag{B6}$$

where Z_1^e presents the impedance in Port 1 in the even- mode analysis circuit.

$$\begin{aligned}\Gamma_1^e &= \frac{Z_1^e - 2Z_0}{Z_1^e + 2Z_0} \\ &= \frac{\dfrac{(1+j)Z_0(R_1^2+4Z_0^2)}{(1+j)R_1Z_0 + 2(1+j)Z_0^2 + R_1^2} - 2Z_0}{\dfrac{(1+j)Z_0(R_1^2+4Z_0^2)}{(1+j)R_1Z_0 + 2(1+j)Z_0^2 + R_1^2} + 2Z_0} \\ &= \frac{(-1+j)Z_0R_1^2 - 2(1+j)R_1Z_0^2}{(3+j)R_1^2 + 8(1+j)Z_0^2 + 2(1+j)R_1Z_0}\end{aligned} \quad , \tag{B7}$$

where Γ_1^e presents the reflect coefficient in Port 1 in the even- mode analysis circuit.

$$\begin{aligned}Z_2^e &= j\omega_0 L + 2Z_0 \,||\, R_1^{'} \,||\, \frac{1}{j\omega_0 C_1^{'}} \\ &= jZ_0 + \frac{1}{\dfrac{1}{2Z_0} + \dfrac{1}{R_1 + \dfrac{4Z_0^2}{R_1}} + \dfrac{1}{-j(2Z_0 + \dfrac{R_1^2}{2Z_0})}} \\ &= \frac{4(1+j)Z_0^3 + (2+j)Z_0R_1^2 + 2jZ_0^2R_1)}{4(1+j)Z_0^2 + 2R_1Z_0 + R_1^2}\end{aligned} \quad , \tag{B8}$$

where Z_2^e presents the impedance in Port 2 in the even- mode analysis circuit.

$$\begin{aligned}\Gamma_2^e &= \frac{Z_2^e - Z_0}{Z_2^e + Z_0} \\ &= \frac{\dfrac{4(1+j)Z_0^3 + (2+j)Z_0R_1^2 + 2jZ_0^2R_1)}{4(1+j)Z_0^2 + 2R_1Z_0 + R_1^2} - Z_0}{\dfrac{4(1+j)Z_0^3 + (2+j)Z_0R_1^2 + 2jZ_0^2R_1)}{4(1+j)Z_0^2 + 2R_1Z_0 + R_1^2} + Z_0} \\ &= \frac{(1+j)R_1^2 + 2(-1+j)R_1Z_0}{(3+j)R_1^2 + 8(1+j)Z_0^2 + 2(1+j)R_1Z_0}\end{aligned} \quad , \tag{B9}$$

where Γ_2^e presents the reflect coefficient in Port 2 in the even- mode analysis circuit.

$$
\begin{aligned}
V_2^e &= \frac{Z_2^e}{Z_2^e + Z_0} V_{2g} \\
&= \frac{\dfrac{4(1+j)Z_0^3 + (2+j)Z_0 R_1^2 + 2jZ_0^2 R_1)}{4(1+j)Z_0^2 + 2R_1 Z_0 + R_1^2}}{\dfrac{4(1+j)Z_0^3 + (2+j)Z_0 R_1^2 + 2jZ_0^2 R_1)}{4(1+j)Z_0^2 + 2R_1 Z_0 + R_1^2} + Z_0} \times 2V_0 \\
&= \frac{4(1+j)Z_0^2 + (2+j)R_1^2 + 2jR_1 Z_0}{(3+j)R_1^2 + 8(1+j)Z_0^2 + 2(1+j)R_1 Z_0} \times 2V_0
\end{aligned}
\tag{B10}
$$

where V_2^e presents the voltage in Port 2 in the even- mode analysis circuit.

$$
\begin{aligned}
V_2^{e+} &= \frac{V_2^e}{1+\Gamma_2^e} \\
&= \frac{4(1+j)Z_0^2 + (2+j)R_1^2 + 2jR_1 Z_0}{(3+j)R_1^2 + 8(1+j)Z_0^2 + 2(1+j)R_1 Z_0} \times 2V_0 \\
&\times \frac{1}{1 + \dfrac{(1+j)R_1^2 + 2(-1+j)R_1 Z_0}{(3+j)R_1^2 + 8(1+j)Z_0^2 + 2(1+j)R_1 Z_0}} \\
&= V_0
\end{aligned}
\tag{B11}
$$

where V_2^{e+} presents the input voltage in Port 2 in the even- mode analysis circuit.

$$
\begin{aligned}
V_2^{e-} &= V_2^{e+} \Gamma_2^e \\
&= V_0 \times \frac{(1+j)R_1^2 + 2(-1+j)R_1 Z_0}{(3+j)R_1^2 + 8(1+j)Z_0^2 + 2(1+j)R_1 Z_0}
\end{aligned}
\tag{B12}
$$

where V_2^{e-} presents the reflect voltage in Port 2 in the even- mode analysis circuit.

$$
\begin{aligned}
V_1^e &= \frac{2Z_0 \parallel R_1^{'} \parallel \frac{1}{j\omega_0 C_1^{'}}}{Z_2^e + Z_0} V_{2g} \\
&= \frac{\frac{2Z_0(R_1^2 + 4Z_0^2)}{(R_1^2 + 4Z_0^2) + 2Z_0(R_1 + 2jZ_0)}}{\frac{4(1+j)Z_0^3 + (2+j)Z_0R_1^2 + 2jZ_0^2R_1)}{4(1+j)Z_0^2 + 2R_1Z_0 + R_1^2} + Z_0} \times 2V_0 . \\
&= \frac{4(R_1^2 + 4Z_0^2)}{8(1+j)Z_0^2 + (3+j)R_1^2 + 2(1+j)R_1Z_0} V_0
\end{aligned}
\tag{B13}
$$

where V_1^e presents the voltage in Port 1 in the even- mode analysis circuit.

$$
\begin{aligned}
V_1^{e+} &= \frac{V_1^e}{1+\Gamma_1^e} \\
&= \frac{\frac{4(R_1^2 + 4Z_0^2)}{8(1+j)Z_0^2 + (3+j)R_1^2 + 2(1+j)R_1Z_0} V}{1 + \frac{(-1+j)Z_0R_1^2 - 2(1+j)R_1Z_0^2}{(3+j)R_1^2 + 8(1+j)Z_0^2 + 2(1+j)R_1Z_0}} . \\
&= \frac{2}{1+j} V_0
\end{aligned}
\tag{B14}
$$

where V_1^{e+} presents the input voltage in Port 1 in the even- mode analysis circuit.

$$
\begin{aligned}
V_1^{e-} &= V_1^{e+}\Gamma_1^e \\
&= \frac{2}{1+j} V_0 \times \frac{(-1+j)Z_0R_1^2 - 2(1+j)R_1Z_0^2}{(3+j)R_1^2 + 8(1+j)Z_0^2 + 2(1+j)R_1Z_0} , \\
&= \frac{(-1+j)Z_0R_1^2 - 2(1+j)R_1Z_0^2}{(3+j)R_1^2 + 8(1+j)Z_0^2 + 2(1+j)R_1Z_0} (1-j)V_0
\end{aligned}
\tag{B15}
$$

where V_1^{e-} presents the voltage in Port 1 in the even- mode analysis circuit.

Odd mode analysis

The schematic of the odd-mode is shown in Fig. B4.

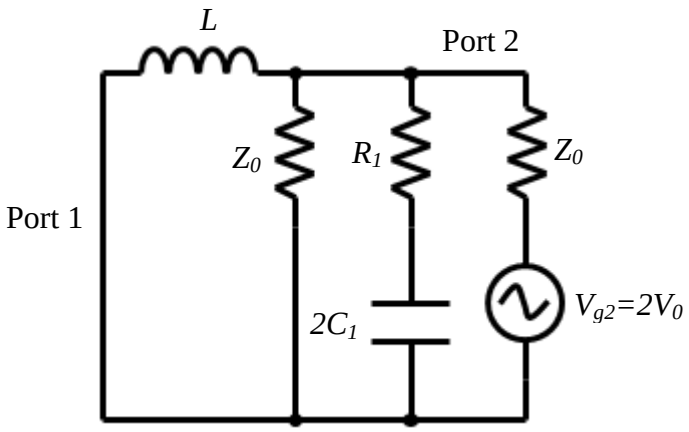

Fig. B4 Schematic of odd mode.

The equivalent circuit of Fig B4 is shown in Fig. B5.

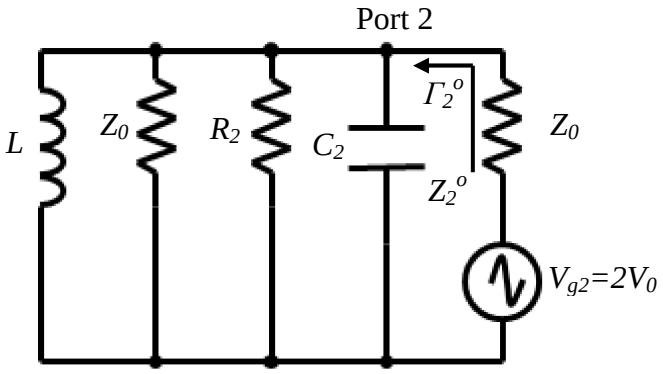

Fig. B5 Equivalent circuit of Fig B4.

Then the parameter can be determined according [B1.2]:

$$L = \frac{Z_0}{\omega_0}, \tag{B16}$$

$$C_1 = \frac{1}{2\omega_0 Z_0}, \tag{B17}$$

$$R_2 = R_1(1+(\frac{\omega_0 L}{R_1})^2) = R_1 + \frac{Z_0^2}{R_1}, \tag{B18}$$

$$\frac{1}{j\omega_0 C_2} = \frac{1}{j2\omega_0 C_1}(1+(\frac{\omega_0 L}{R_1})^2) = -jZ_0(1+\frac{R_1^2}{Z_0^2}), \tag{B19}$$

$$\begin{aligned} Z_2^o &= j\omega_0 L \,\|\, Z_0 \,\|\, R_2 \,\|\, \frac{1}{j\omega_0 C_2} \\ &= \frac{1}{\frac{1}{jZ_0}+\frac{1}{Z_0}+\frac{1}{R_1+\frac{Z_0^2}{R_1}}+\frac{1}{-jZ_0(1+\frac{R_1^2}{Z_0^2})}}, \\ &= \frac{Z_0(Z_0^2+R_1^2)}{Z_0^2+(1-j)R_1^2+R_1Z_0} \end{aligned} \tag{B20}$$

where Z_2^o presents the impedance in Port 2 in the odd- mode analysis circuit.

$$\begin{aligned} \Gamma_2^o &= \frac{Z_2^o - Z_0}{Z_2^o + Z_0} \\ &= \frac{\frac{Z_0(Z_0^2+R_1^2)}{Z_0^2+(1-j)R_1^2+R_1Z_0} - Z_0}{\frac{Z_0(Z_0^2+R_1^2)}{Z_0^2+(1-j)R_1^2+R_1Z_0} + Z_0}, \\ &= \frac{Z_0^3+Z_0R_1^2-Z_0^3-(1-j)R_1^2Z_0-R_1Z_0^2}{Z_0^3+Z_0R_1^2+Z_0^3+(1-j)R_1^2Z_0+R_1Z_0^2} \\ &= \frac{jR_1^2-R_1Z_0}{2Z_0^2+(2-j)R_1^2+R_1Z_0} \end{aligned} \tag{B21}$$

where Γ_2^o presents the reflect coefficient in Port 2 in the odd- mode analysis circuit.

$$
\begin{aligned}
V_2^o &= \frac{Z_2^o}{Z_2^o + Z_0} V_{2g} \\
&= \frac{\dfrac{Z_0(Z_0^2 + R_1^2)}{Z_0^2 + (1-j)R_1^2 + R_1 Z_0}}{\dfrac{Z_0(Z_0^2 + R_1^2)}{Z_0^2 + (1-j)R_1^2 + R_1 Z_0} + Z_0} \times V_{2g}, \\
&= \frac{Z_0^2 + R_1^2}{2Z_0^2 + (2-j)R_1^2 + R_1 Z_0} \times 2V_0
\end{aligned}
\tag{B22}
$$

where V_2^o presents the voltage in Port 2 in the even- mode analysis circuit.

$$
\begin{aligned}
V_2^{o+} &= \frac{V_2^o}{1 + \Gamma_2^o} \\
&= \frac{\dfrac{Z_0^2 + R_1^2}{2Z_0^2 + (2-j)R_1^2 + R_1 Z_0} \times 2V_0}{1 + \dfrac{jR_1^2 - R_1 Z_0}{2Z_0^2 + (2-j)R_1^2 + R_1 Z_0}}, \\
&= V_0
\end{aligned}
\tag{B23}
$$

where V_2^{o+} presents the input voltage in Port 2 in the odd- mode analysis circuit.

$$
\begin{aligned}
V_2^{o-} &= V_2^{o+} \Gamma_2^o \\
&= V_0 \frac{jR_1^2 - R_1 Z_0}{2Z_0^2 + (2-j)R_1^2 + R_1 Z_0},
\end{aligned}
\tag{B24}
$$

where V_2^{o-} presents the voltage in Port 2 in the odd- mode analysis circuit.

$$
\begin{aligned}
S_{11} &= \frac{V_1^{o-} + V_1^{e-}}{V_1^{o+} + V_1^{e+}} \\
&= \Gamma_1^e \qquad\qquad , \\
&= \frac{(-1+j)Z_0 R_1^2 - 2(1+j)R_1 Z_0^2}{(3+j)R_1^2 + 8(1+j)Z_0^2 + 2(1+j)R_1 Z_0}
\end{aligned}
\tag{B25}
$$

When $Z_0 >> R_1$, S_{11} can be simplified to the following

$$S_{11} \approx \frac{-R_1}{4Z_0 + R_1}, \tag{B26}$$

$$\begin{aligned} S_{22} &= \frac{V_2^{o-} + V_2^{e-}}{V_2^{o+} + V_2^{e+}} \\ &= \frac{V_2^{o+}\Gamma_2^e + V_2^{e+}\Gamma_2^o}{V_2^{o+} + V_2^{e+}} \\ &= \frac{1}{2}(\Gamma_2^e + \Gamma_2^o) \\ &= \frac{1}{2}\left(\frac{jR_1^2 - R_1Z_0}{2Z_0^2 + (2-j)R_1^2 + R_1Z_0}\right. \\ &\quad \left. + \frac{(1+j)R_1^2 + 2(-1+j)R_1Z_0}{(3+j)R_1^2 + 8(1+j)Z_0^2 + 2(1+j)R_1Z_0}\right) \end{aligned} \quad , \tag{B27}$$

When $Z_0 >> R_1$, S_{22} can be simplified to the following

$$S_{22} \approx \frac{1}{2}\left[\frac{-R_1}{2Z_0 + R_1} + \frac{-(1-j)R_1}{4(1+j)Z_0 + (1+j)R_1}\right], \tag{B28}$$

$$\begin{aligned} S_{12} &= \frac{V_1^e + V_1^o}{V_2^e + V_2^o} \\ &= \left(\frac{4(R_1^2 + 4Z_0^2)}{8(1+j)Z_0^2 + (3+j)R_1^2 + 2(1+j)R_1Z_0}V_0 + 0\right) \times \\ &\quad \frac{1}{\frac{4(1+j)Z_0^2 + (2+j)R_1^2 + 2jR_1Z_0}{(3+j)R_1^2 + 8(1+j)Z_0^2 + 2(1+j)R_1Z_0} \times 2V_0 + \frac{Z_0^2 + R_1^2}{2Z_0^2 + (2-j)R_1^2 + R_1Z_0} \times 2V_0} \cdot \\ &= \frac{2(8Z_0^4 + 4Z_0^3R_1 + 4(2-j)Z_0^2R_1^2 + Z_0R_1^3 + (2-j)R_1^4)}{16(1+j)Z_0^4 + (6+10j)Z_0^3R_1 + (24+17j)Z_0^2R_1^2 + (6+7j)Z_0R_1^3 + (8+j)R_1^4} \end{aligned} \tag{B29}$$

When $Z_0 >> R_1$, S_{12} can be simplified to the following:

$$S_{12} \approx \frac{8Z_0 + 4R_1}{8(1+j)Z_0 + (3+5j)R_1}. \tag{B28}$$

According to the symmetrical structure and the theory, then

$S_{21}=S_{12}=S_{31}=S_{13}$

$S_{33}=S_{22}$

$S_{23}=S_{32}=0$

Then all the scatting parameters $\begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix}$ are defined.

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