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MANUFACTURABLE PROCESS AND TOOL FOR HIGH PERFORMANCE METAL/HIGH-K GATE DIELECTRIC STACKS FOR SUB-45 NM CMOS & RELATED DEVICES

A Dissertation
Presented to
the Graduate School of
Clemson University

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy
Electrical and Computer Engineering

---

by
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August 2007

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ABSTRACT

Off state leakage current related power dominates the CMOS heat dissipation problem of state of the art silicon integrated circuits. In this study, this issue has been addressed in terms of a low-cost single wafer processing (SWP) technique using a single tool for the fabrication of high-κ dielectric gate stacks for sub-45 nm CMOS. A system for monolayer photoassisted deposition was modified to deposit high-quality HfO_2 films with in-situ clean, in-situ oxide film deposition, and in-situ anneal capability. The system was automated with Labview 8.2 for gas/precursor delivery, substrate temperature and UV lamp. The gold-hafnium oxide-aluminum (Au-HfO_2-Al) stacks processed in this system had superior quality oxide characteristics with gate leakage current density on the order of 1 x 10^{-12} A/cm^2 @ 1V and maximum capacitance on the order of 75 nF for EOT=0.39 nm. Achieving low leakage current density along with high capacitance demonstrated the excellent performance of the process developed. Detailed study of the deposition characteristics such as linearity, saturation behavior, film thickness and temperature dependence was performed for tight control on process parameters. Using Box-Behnken design of experiments, process optimization was performed for an optimal recipe for HfO_2 films. UV treatment with in-situ processing of metal/high-κ dielectric stacks was studied to provide reduced variation in gate leakage current and capacitance. High-resolution transmission electron microscopy (TEM) was performed to calculate the equivalent oxide thickness (EOT) and dielectric constant of the films. Overall, this study shows that the in-situ fabrication of MIS gate stacks allows for lower processing costs, high throughput, and superior device performance.

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CHAPTER 1

INTRODUCTION

The introduction of high-κ gate dielectrics in place of currently used silicon based gate dielectrics has the potential to push silicon complimentary metal-oxide-silicon (CMOS) technology to the fundamental limit of <10 nm feature size circuits. The ability of the semiconductor industry to continue scaling microelectronic devices to smaller dimensions is limited by quantum mechanical effects. As the thickness of conventional silicon dioxide (SiO_2) gate insulators is reduced to just a few atomic layers, electrons can tunnel directly through the dielectric films. Continued device scaling will therefore require the replacement of the insulator with high-dielectric-constant (high-κ) oxides, to increase its thickness, thus preventing tunneling currents while retaining the electronic properties of an ultra thin SiO_2 film.

In Chapter 2, published results of high dielectric constant gate dielectrics have been analyzed with process integration and manufacturing criterions. Required materials, performance, process and manufacturing requirements of high-k dielectrics are outlined. A careful study of published results shows that from the materials point of view, the MOSFET data does indicate significant advantages of using hafnium-based compounds as the gate material compared to any other material reported so far. Research is underway in the semiconductor industry to meet the manufacturing needs for process integration requirements to implement high-κ gate dielectrics. Based on the work reported in this dissertation, I propose a new tool/process for the integration of the metal/high-κ gate dielectric stack in the currently used CMOS fabrication sequence.

In Chapter 3, discussion on the development of rapid photothermal based mono layer deposition (RTPMLD) system is presented. Also, discussion on the basics of mono layer photoassisted deposition and UV based RTP or rapid photothermal process (RPP) is presented. Description of the system is detailed and some key features are discussed. It is shown that the RTPMLD processed gate dielectric has the potential to solve some of the manufacturing and process integration issues currently faced by the semiconductor industry. RTPMLD deposition of HfO_2 films showed a significant reduction in leakage current density as well as an increase in capacitance per unit area. Automation of the RTPMLD system was carefully designed using Labview 8.2 software from National Instruments for precise delivery of the MLD reactants and substrate heater control and this is described in Chapter 3. This automation enables the RTPMLD system to be robust, reliable and extremely precise for repeatable performance.

In Chapter 4, the impact of zero gate leakage current density on future CMOS technology nodes is discussed. The MLD process is characterized in great detail using the precursor tetrakis dimethyl amido hafnium (TDMAH) outlining critical and noncritical processes for growth rate, deposition cycles, temperature dependence and dielectric thickness. Results are reported for optimized process parameters. For effective oxide thickness of 0.39 nm, we have achieved a leakage current density as low as 1x 10^{-12} A/cm^2 at a gate voltage of +3 to -3 V. The leakage current density of 1.06 x 10^{-12} A/cm^2 for an EOT of 0.39 nm at 1 V represents the lowest value of leakage current reported by any one to date. The comparison in terms of leakage current density vs. EOT between our results and other reported results in the literature is shown. It shows that our leakage

current density with an EOT of 0.39 nm is four orders of magnitude lower than the best published results at higher EOT values. Detailed high resolution transmission electron microscopy (HRTEM) studies are also reported here. In the TEM micrographs, the interface between HfO_2 and Si(001) is atomically sharp and shows that the hafnium oxide layer appears conformal to the (100) silicon substrate having a uniform thickness. These two features along with the thin interfacial oxide layer hold the key to the excellent electrical properties for RTPMLD processed HfO_2. Finally, a brief discussion on repeatability and the effect of the front contact area are discussed.

In Chapter 5, the statistical optimization of process parameters is outlined for ex-situ/in-situ cleaning, deposition and annealing steps. A number of experiments were designed to achieve the lowest leakage current density through Box-Behnken multivariate design techniques. Statistical software, MINITAB, was used to outline surface and contour plots for optimizing the various parameters. Several samples were generated at the same optimal processing conditions to determine the descriptive statistics for leakage current density and capacitance and the results are reported here. Thermal processing of dielectrics is an integral part of advanced semiconductor manufacturing. The advantages of using UV assisted RTP were exploited to process thin dielectric films and is also reported in Chapter 5. The electrical data, after optimizing for all the parameters, is analyzed by statistical methods and the results are compared with 1% level of significance.

Finally, a summary of the significance of the work presented in this study is given in the conclusion chapter.

CHAPTER 2

HIGH-K GATE DIELECTRIC ISSUES

Introduction

Silicon dioxide has served for more than three decades as the gate dielectric material in CMOS devices. The reason for the nearly exclusive use of silicon dioxide in this application is that silicon dioxide uniquely possesses the required combination of several properties: good mobility of holes and electrons flowing in silicon at the silicon dioxide interface, ability to keep electronic states (surface states) at this interface low, relatively low trapping rates of holes and electrons, and excellent compatibility with CMOS processing. CMOS processes in current production feature oxides as thin as 1.2 nm, and device physics requires that this thickness must be further reduced to enable continued scaling improvements in density, performance, and power in very large-scale integrated (VLSI) circuits. Thus, understanding of the reliability of such thin oxides is critical [1-5]. Tunnel current limitations and newer dielectric reliability projections of the gate insulator continue to threaten an end to CMOS scaling unless a suitable replacement for silicon dioxide is soon developed [3-5].

Integrating new materials into a standard CMOS device flow raises many challenges in regard to compatibility with the currently used gate electrode materials, particularly the silicon surface itself [6]. Although several new high-k materials have been researched for several years now, there have been several roadblocks to integrating

these materials to the 65 nm node [7]. This study attempts to look at these issues and suggest solutions for the successful integration of high-k dielectrics.

Need for a High-κ Gate Material

In a recent publication we have outlined the needs of the semiconductor manufacturing industry in the 21st century [8]. In order to meet the needs of the 45 nm technology node, high-κ material has to be introduced. The challenges of integrating high-k into the existing CMOS process flow is discussed in great detail here [9]. Figure 1 shows the normalized total chip power dissipation versus the physical gate length and corresponding years of possible production of high-κ [10]. The possible trajectory with the inclusion of high-κ dielectrics shows a clear reduction of the total chip power dissipation.

Theoretically, the improved performance that is obtained when scaling logic device dimensions is seen clearly when you consider a simple model for the drive current associated with a FET [11]. The drive current can be written using the gradual channel approximation as:

$$I_D = \frac{W}{L} \mu C_{ox} (V_G - V_T - \frac{V_D}{2}) V_D \tag{1}$$

where W is the width of the transistor channel, L is the channel length, μ is the channel carrier mobility (assumed constant here), C_{ox} is the capacitance density associated with the gate dielectric when the underlying channel is in the inverted state, V_G and V_D are the voltages applied to the transistor gate and drain respectively, and the threshold voltage is given by V_T. Here the drain current is proportional to the average charge across the channel (potential is $V_D/2$) and the average electric field (V_D/L) along the channel

direction. Initially, I_D increases linearly with V_D and then eventually saturates to a maximum when $V_{D,sat} = V_G - V_T$ to yield

$$I_{D,sat} = \frac{W}{L}\mu C_{inv}\frac{(V_G - V_T)^2}{2} \tag{2}$$

The term (V_G - V_T) is limited in range due to reliability and room temperature operation constraints, since a very large V_G would create an undesirably high electric field across the oxide. Further, V_T cannot be easily reduced below 200 mV, because kT ~ 25mV at room temperature. Typical specification temperatures (≤ 100°C) could therefore cause statistical fluctuations in thermal energy, which would adversely affect the desired V_T value. Thus, even in this simplified approximation, a reduction in the channel length or an increase in the gate dielectric capacitance will result in an increased I_{Dsat}.

In the case of increasing the gate capacitance, consider a parallel plate capacitor (ignoring quantum mechanical and depletion effects from a Si substrate and gate) [11]

$$C = \frac{\kappa\varepsilon_0 A}{t} \tag{3}$$

where κ is the dielectric constant or the relative permittivity of the material [12]. ε_0 is the permittivity of free space (8.85×10^{-3} fF/μm), A is the area of the capacitor, and t is the thickness of the dielectric. This expression for C of the capacitor can be rewritten in terms of t_{eq} which is equivalent oxide thickness, and $\kappa_{ox,}$ which is the dielectric constant of Si, 3.9. The term t_{eq} represents the theoretical thickness of SiO_2 that would be required to achieve the same capacitance density as the dielectric (ignoring issues such as leakage current and reliability). For example, if the capacitor dielectric is SiO_2,

$$t_{eq} = 3.9\varepsilon_0\left(\frac{A}{C}\right), \quad (4)$$

and a capacitance density of

$$\frac{C}{A} = 34.5 fF / \mu m^2 \quad (5)$$

corresponds to t_{eq}=10 Å. Thus the physical thickness of an alternative dielectric employed to achieve the equivalent capacitance density of t_{eq}=10 A^o can be obtained from the expression

$$\frac{t_{eq}}{\kappa_{ox}} = \frac{t_{high-\kappa}}{\kappa_{high-\kappa}} \quad (6)$$

or simply,

$$t_{high-\kappa} = \frac{\kappa_{high-\kappa}}{\kappa_{ox}} t_{eq} = \frac{\kappa_{high-\kappa}}{3.9} t_{eq} \quad (7)$$

A dielectric with a relative permittivity of 16 therefore affords a physical thickness of ~40 A^o to obtain t_{eq}=10 A^o. In reality, actual performance of a CMOS gate stack does not scale directly with the dielectric due to possible quantum mechanical and depletion effects [10].

Required Properties of a Suitable Material

The new dielectric must satisfy a number of requirements based on material, properties, device performance and reliability. A complete understanding and control of these requirements can lead to the successful integration of high-κ dielectrics into the manufacturing sequence. In the following subsections, some critical properties of high-κ materials that are relevant for low power and ultra fast electronics are discussed.

a. Crystal Structure

The high-κ dielectrics can be either crystalline or amorphous in nature. In general, high dielectric constant materials do not remain amorphous at the temperature (about 900°C or more) used in processing silicon CMOS. Therefore, the crystal structure and the lattice constant of a material may be important parameters in deciding the quality of the silicon-dielectric interface. It is known that the crystalline structure should be identical to that of Si. The amount of deviation from that of the silicon structure will determine the defect density and the lattice strain at the interface, and those may also determine whether the presence of an interfacial SiO_2 layer is desirable or not [13].

b. Band Offset and Electron Affinity

The tunneling current depends on the carrier effective mass, m, in the dielectric, the barrier height between the silicon and the conduction or the valence band of the insulator, Φ_B, and the barrier thickness t_{di}. The tunneling probability for a rectangular barrier can be expressed as [10]:

$$T \equiv \exp\left(-2\frac{\sqrt{2mq}}{\hbar}\right)\sqrt{\phi_B t_{di}} \quad (8)$$

The issue of the bandgap and electron affinity of high-κ dielectric materials was discussed in [14]. In recent years, improved methods of calculations of band alignments of different oxides with respect to silicon have been reported [15]. However, in calculating the values of barrier height, the effect of image force barrier lowering should be considered, which is given by [10, 16]:

$$\Delta\phi_B = \sqrt{\frac{qE}{4\pi\kappa\varepsilon_o}} \tag{9}$$

where, E is the electric field at the interface, and ε_o is the free space permittivity. For SiO_2 at $E=1.5\times10^7$ V/cm, the barrier lowering is 0.75 V, while for a value of $\kappa=25$, the value of $\Delta\Phi_B$ is about 0.3 V.

c. Melting Point

Melting point of a material is very crucial [17]. High bandgap materials should have high a melting point. Lack of high melting point indicates inherent imperfection of the material (like weak bonds: contrast the melting point of diamond with that of graphite). Another important point is that deposition of a film much below the melting temperature tends to produce defects in the material. Addition of different types of energy sources (e.g. visible and ultra violet photons) along with thermal energy may be needed to increase ionization energy as well as atomic mobility, in order to obtain a defect free dielectric.

d. Device Requirements

The success of the silicon CMOS transistor as a high speed, low power, and low cost device is attributed to a large extent to the excellent quality of SiO_2 as the gate dielectric, as well as the excellent properties of the Si-SiO_2 interface. Any new gate dielectric material must satisfy a number of device requirements described in the following sections.

1 .Leakage Current Density

The leakage current of current high-κ based metal-insulator-semiconductor (MIS) structure should be atleast two or three orders of magnitude lower than the leakage current of the corresponding MOS (metal-SiO_2-silicon) structure with the same equivalent oxide thickness. Only under these conditions, the gate current will be negligible as compared to the drain current. Thus, from both the device performance and reliability point of view, and also from the power dissipation consideration, the leakage current criterion is critical for the use of high-κ dielectrics in the future generations of CMOS.

2. Bulk and Interface Defects

The interface between the insulator and silicon is extremely important for optimum device performance. Any particular mechanism that is responsible for the creation of defects and the manner in which they are responsible for dielectric degradation are still under debate. Most researchers believe that the creation of defects is related to the passage of electrons (and/or holes) through the dielectric. It is also well accepted that the energy of the electrons has a direct effect upon the generation of such defects and specifically the rate at which such defects are produced. An understanding of the carrier transport mechanisms is therefore a key to identifying the nature of defect generation. For example, if we consider the Si-SiO_2 system, the interface is atomically abrupt and electrically perfect to first order [18, 19]. Although the Si-SiO_2 interface is highly stressed with the oxide under compressive stress, the Si-SiO_2 system produces a virtually perfect electrical interface with trap and fixed charge densities corresponding to less than

one surface defect in 10^5 surface silicon atoms [19]. Thus, high-κ dielectric based transistors will require control of nanoscale atomic roughness at the Si-dielectric interface, and structural homogeneity is crucial for obtaining the desired performance and reliability.

3. Mobility

The drain current of a CMOS device is directly proportional to mobility. It has been shown recently [20] that even for a nanoscale MOSFET, mobility is an important factor in determining the on current, as long as the device does not approach the ballistic limit. A low value of the midgap interface state density does not guarantee that mobility will not be degraded under device operating conditions [20]. Therefore one of the major issues in the development of high-κ materials is to achieve low defect density for the Si-high-κ system, so that the mobility does not degrade. Perfectly controlled ultrathin (1-2 monolayer) high quality silicon-oxide (SiO_2) layer may be required to obtain mobility comparable to the Si-SiO_2 system.

4. Power Dissipation

The leakage current has become a very important issue and will present the most important obstacle for sub 45 nm designs. As can be seen from Figure 2 [21], while the active power remains approximately the same with the decreasing technology nodes, the leakage power is increasing. Hence, controlling this sensitive nature of leakage current will be the toughest challenge for both designers and manufacturers. A waste of more power in leakage current would imply more energy to do the basic operation of moving the carriers from source to drain which means more of battery power will be drained.

Leakage power is the dominant component of future nodes of technology. As Figure 2 points out, at the 50 nm node, the significant power problem is induced by the leakage component as opposed to the short circuit or switching power though they dominated in previous nodes of technology.

Sub threshold leakage power increases exponentially and accounts for about 42% of the total power in the 90nm technology [22]. The goal is to maximize the drive current, that is, the ratio between I_{ON} and $I_{OFF,}$ but at the same time reduce the leakage current to minimize power utilized by the chip. Techniques such as strained silicon [18, 22], stack effect [23], and reverse body bias [24] are being investigated for reduction of leakage power. Leakage power reduction being the main focus of low-power design, sleep transistors is one such solution where the majority of the functional blocks are only active for a small fraction of time. The use of the sleep transistors lowers leakage by the stack effect, where when functional block enters standby mode, sleep transistor isolates the supply from the block [22, 24]. Although this may be a solution to reducing leakage, the side effects include functional blocks incurring performance degradation during active operation and increase in area on the chip [25] among others; however, it is the most effective technology as technology scales.

e. Metal Gate Considerations

For the future generations of CMOS, metals have to be used as gate electrodes because of the problems related to polysilicon. Thus it has been shown that the entire gate stack has to be changed [23, 25]. In the case of metals, the gate electrode formation should occur during the final part of the process to avoid high temperatures and acids [10, 25]. The

damascene process will make it more complicated. Another problem concerning metal gate is that the work function of the gate electrode has to be selected in such a way that these are different for NMOS and PMOS, in order to adjust the threshold voltage to the optimum values. The combination of the high-κ gate dielectric with the metal gate enables a drastic reduction in current leakage while maintaining very high transistor performance, making it possible to drive and technology innovation well into the next decade. In order to achieve optimum device performance, work functions close to the band edges of silicon are desired. Materials with nearly the correct work function can be selected from the periodic table, but the integration of any two metals in a CMOS flow is very challenging.

f. Reliability Requirements

Early failures will become more important for the future generations of circuits [28]. The breakdown voltage of high-κ dielectrics is reasonably high enough for low voltage operation of the future generation devices. Defect generation both at the interface and in the bulk of the dielectric is directly related to the microstructure of the high-κ dielectric material [29]. Structural homogeneity will assure minimal defects in the starting material as well as defects generated during the lifetime of the device [26]. Particular attention needs to be paid to the trap generation and the impurities in the dielectric material. This will require the introduction of new concepts such as built-in reliability material. In other words, the process has to provide a perfect microstructure to assure the desired reliability [27]. The following steps, that were suggested to improve the reliability of the thin gate oxides, will also be applicable to high-κ dielectrics.

a. Careful monitoring of the intrinsic structural wearout will need to be carried out, as these are reliable indicators of dielectric quality [31, 32].

b. Statistical tools developed for the silicon-based dielectrics will be equally applicable to high-κ dielectrics.

In reality, integrated circuits operate in ac mode. The stress on the dielectric film caused by the ac operating mode is considered to be less destructive compared to the dc stress, and the ac lifetime might be considerably longer than the dc lifetime [30]. If we consider the stress due to ac operating conditions as a restoring mechanism, then under the normal operating conditions, the reliability of the device will increase [31]. These results will need to be included, since the fast switching field may affect the high-κ dielectric degradation in opposing ways.

A number of fundamental questions are still being resolved for the reliability requirements of the sub-45 nm technology node [28, 29]. These include:

1. Whether the mechanism of defect generation, at the semiconductor-dielectric interface and in the dielectric bulk, is basically different, for very low supply voltages and ultra-small gate areas, from the current models [28, 29]. In the case of ultra-small area and leaky gates, the stored energy in the capacitor may not suffice for an electrostatic discharge. In which case, dielectric and interface degradation would be more important and relevant than dielectric breakdown. In a tunnel gate dielectric, how relevant is the concept of hot electron injection into the dielectric [28]? The electron, tunneling through the gate dielectric, cannot be expected to expend any energy in the dielectric bulk. And, even if some electrons

are injected into the dielectric, would they have the energy for the generation of bulk defects, when the supply voltage is very low? In such a situation, would not the interface defects be more important than the bulk defects [30]?

2. In the case of very low supply voltages, ultra-small gate areas and high operation temperatures, how reliable are the current reliability evaluation procedures, particularly the voltage and area scaling procedures [28, 29]? For example, even now, all the voltage stressing is done above 2.0 V, often above 3.0 V, while the future circuits will operate at 0.7 – 1.0 V. Are the extrapolations from 2.0 – 3.0 to 0.7 – 1.0 V not too far fetched, in the light of the questions above?

g. Yield and Defect Management

Detection of ever shrinking yield-critical defects, high aspect ratio defects, nonvisual defects, and timely elimination of yield detracting systematic mechanisms top the list of challenges for yield enhancement for 45 nm and beyond. Moreover, the yield enhancement community is constantly challenged to achieve acceptable yield ramp and mature yields due to increasing process complexity and fewer yield learning cycles with each subsequent technology node [31]. The design for yield should basically incorporate the two most important ideologies of design for test and design for manufacturing.

(a) Cost-effective high throughput, high aspect ratio inspection tools are needed urgently to achieve acceptable yields for current and future process technology nodes [32].

(b) With increasing process complexity and longer cycle times, tools and methods are needed to increase the number of yield learning cycles for each technology node.

(c) With a move to smaller features, longer processes, 300 mm wafers, and new materials (low k, high k, etc.), numerous tools and methods are required to understand all yield detracting interactions. Use of SOI, new gate dielectrics and compound semiconductors will further challenge yield learning [26].

(d) Signal-to-noise improvements are required for defect metrology tools to detect ever shrinking critical defects of interest [33].

Defects enter the cost function at many levels. Firstly, minimizing the process related defects reduces costs of monitoring defects plus the cost related to excluding defected products. Minimizing process-generated defects improves yields and hence die costs. SWP has significant advantages over BP in keeping process related defects to a minimum. Secondly, defected components will fail early in service so this ends up as a cost function to the user. Current practice puts a lot of emphasis on defect monitoring, defect classification, and defect control after processing. The number of process steps that can be completed in-situ clearly reduces the defect density, leading to increased yield and ultimately lower costs.

Although scaling of CMOS technology [the design/process] is being pushed, it doesn't translate to system-level performance because of the leakage and yield issues. The yield enhancement challenges continue to grow with each subsequent technology node. Given the demanding requirements and the above issues, it will be highly unlikely to

achieve historical yield levels in the future unless the drastic approach is changed. The only realistic solution to achieve high-yield levels is to have the signature of the tool as early as the design stage.

h. Throughput and Cost of Ownership Issues

With continuous increase in the cost of modern IC fabrication facilities, issues such as throughput, equipment utilization, cost of ownership, etc., have become more important than ever. However, due to the importance of high-κ dielectrics in the development of sub-45 nm CMOS, these factors may be more tolerable than for other processing steps. Thus, even the low throughput processes (e.g. atomic layer chemical vapor deposition) may be acceptable provided they offer the desired performance, reliability and yield.

i. Low Temperature and Short Time Processing

Enhancement of product yield by controlling different parameters responsible for process fluctuation is going to be more important than ever for nanometer scale gate manufacturing. The surface and related interface nano-roughness of the deposited or a grown material is very important for sub-45 nm feature size geometries. Lower roughness can result in better electrical properties, such as high mobility, low leakage current and better reliability. In any deposition process, one of the major reasons for the formation of surface roughness and defects is the statistical roughening, which arises because of statistical fluctuation in the arrival of the vapor flux. The fluctuation in flux increases with processing temperature. During the deposition, statistical roughening and surface diffusion compete with each other, the first increasing the film roughness and the second smoothing it out. It is well known that at lower processing temperatures, the quality of

dielectrics and throughputs are inferior compared to dielectrics processed at higher temperatures. Thus, at a lower processing temperatures, activation energy reduction for a thermal process can be achieved by using plasmas, photons with wavelength less than infrared, ions, electrons or sonic energy sources. Out of these additional sources of energy, the use of ultra violet (UV) photons for in-situ substrate cleaning, growth or deposition, and in-situ cleaning is very attractive, since these photons provide beneficial effects in reducing microscopic defects, processing temperature and processing time. Combined with rapid thermal processing (RTP), UV photons can be used in developing better thermal processing for sub-45 nm IC manufacturing [37-39].

j. Metrology Related Issues

In order to control the microstructure of the dielectric film, in-situ process control may become a necessity. It has been observed that there is a one to one correspondence between the defects and stress of the dielectric film [40]. Thus, by in-situ monitoring of stress, the homogeneity of the microstructure may be accomplished. Recently, several issues related to metrology need for high-κ dielectrics was discussed in great detail [41].

k. Manufacturing Requirements

As we look forward to the 45 nm technology nodes, technical challenges arise in virtually every aspect of manufacturing. The challenges the industry faces involve more new materials and technologies, including new gate materials and designs, wider use of engineered substrates such as SoI, and the need for more powerful inspection and metrology tools, among many other issues [41]. Besides introducing these new materials and processes, we need to solve the integration issues in CMOS processing. The push for

new materials to increased frequencies creates challenges with deposition, patterning, integration and inspection, as well as packaging. Fab automation continues to be important, not only in terms of optimizing yield and fab efficiency, but also in terms of supply chain management. Equipment and materials suppliers, and their own suppliers of components and subsystems, are developing tools to meet these challenges. Without a doubt, process control, yield, defect management and process variation are major obstacles facing those considering technology requirements for work at the 45 nm node.

Key points that will provide the paradigm shift for integrating high-k dielectrics at 45 nm node and beyond:

(i) Manufacturing at 45 nm node & beyond is no more a game of evolution of existing processes and materials. Only the top integrated device manufacturers (IDM's) and most advanced foundries will be the key future players.

(ii) Most of the advanced 300 mm fabs employ about 80 % of the wafer manufacturing steps by single wafer processing and other 20 % by batch processing [43]. The cycle time for such fabs is about 90 days. On the other hand for single wafer processing fabs the cycle time is about 30 days. Packaging has become more important than ever. For advanced semiconductor products, wafer level packaging is gaining grounds. System on chip is a long term universal solution, and system in package is a near term profitable solution. The use of single wafer manufacturing in both

wafer processing and the wafer level packaging has the potential to reduce the volatility of the semiconductor industry (through better supply chain management). These issues are discussed at length in recent publications [25, 44-45].

(iii) The industry is moving from design for manufacturing (DFM) [management of technology constraint (rules, lithography) applied to a design] to design for yield (DFY) [management of design's sensitivity to the manufacturing process]. Both designers and manufacturers have to interact more closely than in the past. This favors location of foundry and fabless design house in close proximity.

(iv) With the fab tool signature existing right from the design stage combined with the benefits of single wafer manufacturing, high yield levels, and throughput and cost considerations can be incorporated into the tool. This will benefit Optical Proximity corrections (OPC), Automation Process control (APC) and manufacturing variations to be worked into the tool very early, benefiting the overall profitability and performance

Analysis of Published Results

There have been legitimate debates in terms of developing and processing a high-κ gate dielectric material for several years. Recently, in January 2007, Intel Corporation announced that it will incorporate the use of high-k dielectrics (hafnium based compounds) for the 45nm technology node. Although a number of materials have been

proposed as a potential high dielectric constant gate material, hafnium based compounds have emerged as the current material of choice. The published results shown here were compared based on the leakage current density J (A/cm^2) and EOT figures of merit. The lowest reported leakage current density in the open literature, to the best of our knowledge to date, is presented by Mikelashvili et al [46] to be 1.6 x 10^{-8} A/cm^2. It will be shown in Chapter 4 that our leakage current density with an EOT of 0.39 nm is four orders of magnitude lower than the best published results at higher EOT values [47].

Process Integration Considerations

Variations due to the process have to be taken seriously now, even though in the past, the industry could make a profit with serious variations caused by different processes. Tighter design rules have been successfully implemented to keep process variation issues at bay from the critical manufacturing issues [48]. However, as the critical dimensions are moving towards a few nanometers, process control at the atomic level is becoming a significant issue [49]. As future circuits will be capable of handling fewer process variations, both designers and process engineers have to coordinate in such a way that the process is optimized for the design or vice versa. Otherwise, yield will be affected and the profit will decline. This situation can be eased by developing a process that has the inherent property of introducing fewer defects during processing. Single wafer manufacturing has the advantage of precision and accuracy for each wafer, which increases performance and yield while reducing defects. Figure 3 shows the process integration challenged faced by the semiconductor industry today.

Conclusion

In this chapter, the key issues involved in the process integration and manufacturing of high-κ gate dielectrics for the next generation of silicon MOSFETs have been reviewed. An examination of the published results shows that from the materials point of view, even though there is a clear cut winner in hafnium-based compounds at this moment, the leakage current density is not low enough to scale to the fundamental limits of Silicon technology. Due to the fundamental limitations of the materials, currently used high-temperature processing techniques are inadequate to meet the process integration and manufacturing requirements. By innovations in process integration schemes, it will be possible to integrate high-κ dielectrics by using currently available low-temperature processing techniques. However, due to the cost of ownership, lack of high performance, and reliability issues, currently available low-temperature processing techniques may not be suitable for manufacturing. Based on published results, it appears that UV assisted rapid thermal processing based chemical vapor deposition tools are capable of meeting the process integration and manufacturing needs. The new tool should also have the in-situ cleaning, in-situ deposition and in-situ annealing capability for the entire gate stack for integration into the currently used CMOS fabrication sequence.

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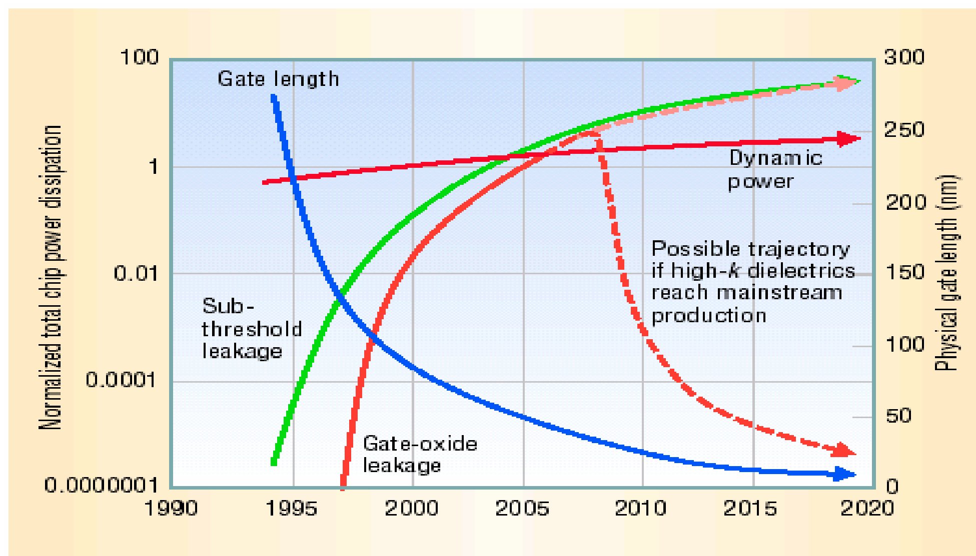

Figure 1 Chip power dissipation versus gate length [10]

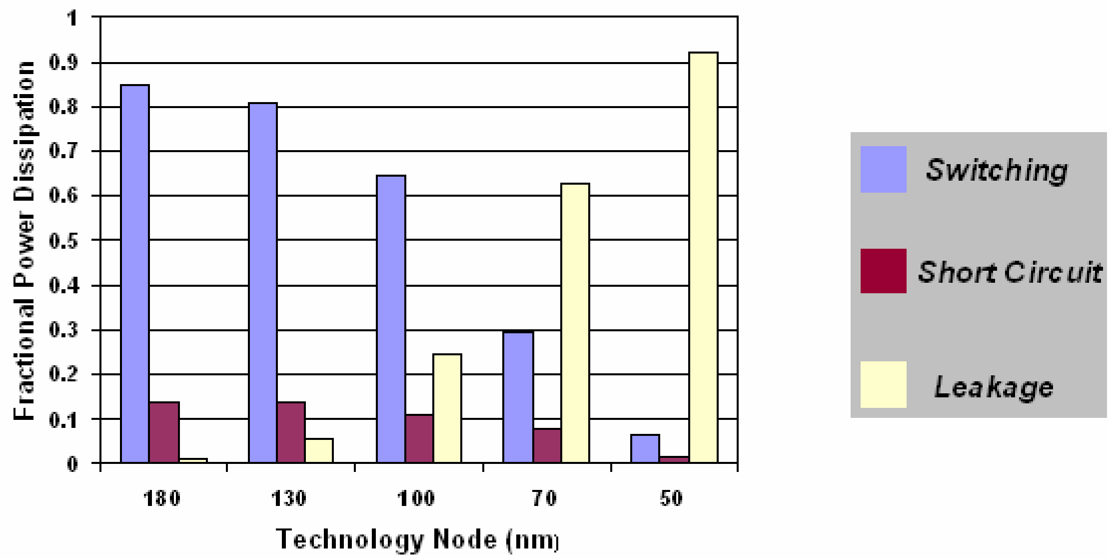

Figure 2 Power dissipation distribution for various technology nodes [21]

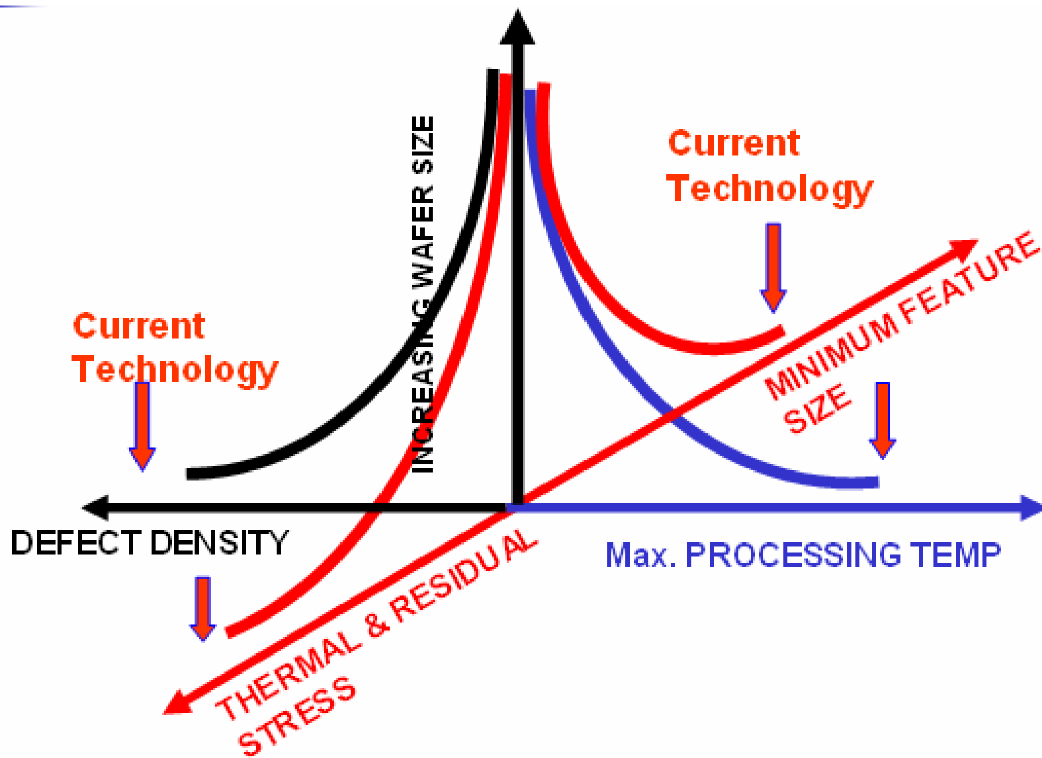

Figure 3 Process integration issues [26]

CHAPTER 3

MONOLAYER PHOTOASSISTED DEPOSITION SYSTEM

Introduction

As discussed in the previous chapter, successful use of a new high-κ material in the real manufacturing environment will depend on developing a new process that can be easily integrated with the existing CMOS process sequence. There is a need to develop a new tool that offers low temperature, short time process and has the built-in quality of minimizing statistical fluctuation as well as providing atomic level control of the film growth. The new tool should also offer in-situ cleaning, in-situ annealing and in-situ gate processing capability. Having all these characteristics in mind, a system was designed at Clemson University previously to deposit zirconium oxide films [1], and that system was modified for the deposition of hafnium oxide films. The tool was automated with Labview to control the UV source and provide pulsing for the precursor delivery, purge gas delivery, and water vapor delivery, in addition to accurate substrate temperature control. A process was developed to process reliable ultra-thin HfO_2 high-κ films by combining all the salient features of traditional monolayer deposition and UV assisted rapid thermal processing (RTP). Because of the high vacuum capability, the system also has the advantage of low pressure chemical vapor deposition (CVD). A low pressure system also offers the advantage of adding in-situ characterization techniques, otherwise not compatible with a high or atmospheric pressure system.

Monolayer Photoassisted Deposition

Monolayer deposition is a process to grow thin films of either crystalline or polycrystalline materials one layer at a time. During the process, a sequential reactant interaction is combined with a substrate at a specific temperature that prevents condensation of individual reactants on the growing surface. Temperature of the substrate is a key parameter to control the growth of the film. The temperature of the substrate should be low enough to allow the monolayer to react with the reactant but high enough to reevaporate any subsequent layers or add-on molecules on top of the monolayer. The control of monolayer growth can be better if there are additional sources of energy (i.e., ultraviolet or vacuum ultraviolet light), so that there is a greater difference between the bond energy of the monolayer and the bond energies of the subsequent layers.

During the process, both elemental and compound reactants can be used. As compound precursors were used in this study, the discussion will be limited to compound reactants. Using compound reactants solves the problem of low vapor pressure of elemental metal reactants. To process a compound; i.e., compound AB, the elements A and B are supplied on the substrate as an alternate exposure of compounds AX and BY. During a typical monolayer photoassisted CVD cycle, compound AX is supplied to the surface of the substrate for time t_1. Then the substrate is purged for time t_2 to ensure that no two reactants are simultaneously present at the substrate surface. Also, if there has been a condensation of the compound AX, it will re-evaporate during the purge time. Usually inert gases are used for the purging process. Figure 4 shows the profile of the cycling steps. For this study, TDMAH (Tetrakis Dimethylamino Hafnium) 99.95% Hf

from Strem Chemicals was used as the first compound, and the second compound BY (Y referring to 1 to n hydrogen atoms), water vapor was used. The compound BY is applied to the substrate for a time t_3, followed by another purge step of duration t_4. Therefore the total time t, needed for one complete process cycle is equal to the sum of t_1 ,t_2, t_3 and t_4. The vapor pressure of BY is usually high and condensation of BY does not occur during the normal monolayer CVD process [2]. During the purge steps, there is a certain amount of possibility of re-evaporation of a formed monolayer A(s) bonded to B. But under favorable process conditions, the re-evaporation probability of an atom A from a B surface is much less than the re-evaporation probability of an atom A from an A surface [2,3]. Also the bond energy of an atom B on surface A is generally higher than that of atom A on surface atoms B (non metal surface atoms generally form a more stable surface than metal atoms). This also prevents the re-evaporation of the B(s) surface [4]. The processing window of the monolayer photoassisted CVD process is shown in Figure 5. In that figure A_1 is the area where condensation of the reactants occurs, A_2 is the area where activation of the necessary reaction is not exceeded, B_1 is the area where decomposition of a reactant results in a non-evaporating surface layer on a monolayer, and B_2 is the area where re-evaporation of a formed monolayer occurs.

UV Radiation and Rapid Thermal Processing (RTP)

It is well known that as the temperature of a black body is increased, the color emitted by it becomes richer in shorter wavelengths. The thermal power of the radiation can be expressed as [5]:

$$P = hf\Delta f\left\{\frac{1}{e^{hf/kT}-1}+\frac{1}{2}\right\} \quad (1)$$

where Δf is the frequency band occupied by the radiation mode, h is Planck's constant, k is boltzman constant and T is absolute temperature. The factor ½ in the above equation is due to the contribution of zero point energy, which is a quantum phenomenon. The other factor inside the curly bracket is the Bose Einstein factor [4], which is the thermal part of radiation. It is evident from Figure 6, that in the lower frequency (higher wavelength) range, the thermal part is dominant but as the frequency goes up, the quantum part of the energy dominates. Therefore, when photons interact with matter there will be quantum effects in addition to thermal effect. It has been shown that photons with wavelength more than about 800 nm contribute to thermal effects [5]. Photons with wavelength between about 400 and 800 nm contribute to both thermal and quantum effects. Only quantum effects are observed with photons less than about 400 nm. The quantum energy of photons that can be used during UV and VUV assisted RTP without any adverse effects (e.g. ionic displacement leading to the formation of defects) is about 10-12 eV [6]. In this case, the use of ultra violet (UV) and vacuum ultra violet (VUV) photons exploits the quantum phenomena. The quantum effects have the following implications for UV assisted rapid thermal processing [6, 7]:

- At any given processing temperature, the bulk and surface diffusion coefficients are enhanced.
- The processing cycle time is reduced.

- Reduced microscopic defects are observed leading to higher performance and better reliability and yield.

The importance of optimized heating and cooling rates for RTP as well as for UV and VUV assisted RTP has been demonstrated in Refs. [8]. In Ref. [9] an algorithm for optimizing the heating and cooling rates has also been presented.

Monolayer Photoassisted Chemical Vapor Deposition System

The monolayer photoassisted chemical vapor deposition process, developed during this project, utilized an existing system which was a combination of an MBE type ALD system and a flow type ALD system. Monolayer photoassisted deposition is done in a high vacuum chamber and the precursor is delivered to the substrate by a carrier gas. For this system the four most important aspects to be considered are:

- Vacuum system – This provides the ultra high vacuum required to make the thin films
- Substrate Heater – Three different temperature profiles during in-situ cleaning, deposition and annealing should be accurately achieved by the heater.
- UV Source
- Precursor and water vapor pulsing delivery system
- Gas Flow control

a. Vacuum System

To create a high vacuum, a 6” Varian diffusion pump (Model type number: VHS-6, 0184) has been used in conjunction with a stokes rotary vane (special service, model: 900-013-241) roughing pump. The system provided high vacuum in the range of 2 x 10^{-7} Torr. Figure 7 shows a schematic diagram of the monolayer photoassisted CVD system. Figure 8 shows a simplified diagram of the monolayer photoassisted CVD system. The stainless steel deposition chamber was custom made. The chamber had a quartz port for viewing. Two built-in ports were available for attaching high intensity UV sources manufactured by Xenon Corporation.

b. UV and VUV Source

A modified version of the RC-500B system manufactured by Xenon Corporation was used as the UV source. During this study, for UV radiation, one lamp source (Part number: 890-1723) was used. This particular lamp, custom-made for effective operation in the test chamber, was chosen primarily because it offered the advantages of deeper penetration for full and consistent cures, process flexibility, and easy integration into the system at hand. In a recent publication the advantages of using RTP in semiconductor manufacturing were explained in detail [10].

c. Substrate Heater

The sample heater used in the monolayer photoassisted CVD system is called a Boraelectric® heater. It is manufactured by GE advanced ceramics (model: HTR 1002). This heater is made by combining pyrolytic boron nitride (PBN), a dielectric ceramic

material, with pyrolytic graphite (PG), an electrical conductor [11]. It is a high-purity resistance heating element with ultra-fast response and power outputs that can exceed 300 watts/sq. inch (45 watts/ sq. cm). Losses to power leads and mechanical support components can be 20 or 30 watts each. In principal, 1 watt with enough insulation will get to 1000°C, yet 1000 watts with high losses will be cool [11].

Boraelectric heaters can reach 1500+ ^{o}C in steady state with shielding and insulation, and that is the primary reason it was chosen as the substrate heater. Free standing parts can reach 1000+ ^{o}C in steady state [11, 12]. Analysis and tests were done to test the heater before its use to determine stability of each temperature profile, and to decide the voltage necessary to ramp up to each temperature at a reasonable time.

The resistivity of the PG conductive film in a Boraelectric® heater decreases with temperature, reaching a low point of about 40% of room temperature value at around 1200 ^{o}C as shown in Figure 9 [11]. Because of this property it requires less voltage as the temperature increases. Since resistance drops as the temperature increases, current also increases. For constant voltage, current will start out low and increase as temperature increases. It is important to remember in transients, before steady state, it is possible to blow fuses if no thermocouple is used, or if the thermocouple does not see the temperature quickly and accurately. For this reason, low mass and fast response thermocouples were used, typically bare wire 0.1” diameter at the tip. The most conservative approach is to use a maximum flux of about 50 watts/cm^2. This is more than adequate for most situations. Boraelectric heaters have been made with over 100 watts/cm^2.

Molybdenum nuts, bolts and washers were used for connecting the heater to the power source and also to mount the heater on the stainless steel sample mount. The heater mounting plate is shown in Figure 10. The temperature was controlled through a variac setting, with a temperature readout manufactured by Omega. Silicon wafers etched out into 1” pieces were used to hold the sample centered above the heater. The silicon wafer pieces were held in place by the moly nuts on the opposite end of the heater as one diagonal side was used for the power connections. A bare wire 0.1” K-type thermocouple manufactured by Omega was used as a sensor to calibrate the temperature controller used for controlling the temperature of the substrate heater.

d. Gas Flow Control

Gas flow was controlled by MKS mass flow controllers. The individual mass flow controllers themselves were controlled using the 647B MKS mass flow controller [12]. All the controllers were calibrated for the gases being used during the experiments. Without doing this one may not expect to get the correct value of the gas volume flowing into the chamber. The chamber and precursor supply lines of the system were maintained at different temperatures by using several tape heaters and temperature controllers manufactured by Omega Corporation. Mass flow controllers were used for the delivery of the following gases:

1. Nitrogen UHP carrier gas
2. Hydrogen in-situ clean gas
3. Nitrous oxide for annealing gas
4. Nitrogen UHP purge gas

5. Oxygen for annealing gas

The details of range specified by the manufacturer were entered into the 647B MFC with any gas correction factors as necessary. The individual gas flow controllers connected to the gas cylinders and to the chamber were turned “on” and “off” through the central 647B controller. The detailed gas flow control is shown in Figure 11.

Precursor and Water Vapor delivery lines

A stainless steel “Tee” manufactured by Nor-Cal Products was used to house the precursor. The precursor was placed in a ceramic boat, which was in turn placed inside the tee. Tape heaters were used on the outer end of the tee to heat the precursor to 85 ^{o}C (boiling point of TDMAH) and careful control through a thermocouple feedback loop to the temperature controller accurately controlled this temperature not to exceed 90 ^{o}C. For the specific precursor used, it is important to ensure that the temperature does not spike over 100°C as the precursor disintegrates at high temperatures. A 315L stainless steel tube was connected directly to the chamber port for the delivery of the precursor, with the carrier gas line connecting to the top of the tee. Figure 12 and Figure 13 clearly explains the precursor delivery system used in the system. The delivery line to the chamber was also heated (with tape heaters) and maintained at the temperature to prevent the gas from condensing along the wall of the tubing. A solenoid gate valve connected to this line enabled automated pulsing through Labview.

For the water vapor delivery system, a similar setup was used, with a DI water source inside a separate chamber. It was not necessary to heat this, as the vapor pressure of the water vapor was high enough to have sufficient water vapor needed for the process.

A solenoid gate valve was also used in this case to enable automated pulsing through Labview.

Precursor Selection

Selecting a precursor for gate oxide deposition requires extensive characterization of targeted molecules. Critical analytical parameters for MOCVD and ALD precursors, such as vapor pressure, thermal stability, and metallic contamination are presented and results discussed herein for the most promising Hf precursors currently under investigation: tetrakis (ethylmethylamino) hafnium (TEMAH), tetrakis (dimethylamino) hafnium (TDMAH), tetrakis (diethylaminohafnium) (TDEAH), tetrakis (tertbutoxy) hafnium (HTB) and hafnium tetrachloride ($HfCl_4$) [15]. The purity of chemicals used to manufacture semiconductor devices is of critical importance to fab engineers. Contamination in process materials can cause device failure and impact yield. Hafnium oxide films are promising candidates for high dielectric constant (high-κ) gate oxides in CMOS and for the next generation of DRAM. Hafnium oxide layers are typically formed by CVD or ALD, in which a hafnium precursor compound is introduced in the gas phase, and an ensuing chemical reaction is allowed to take place on the surface of the wafer. To be successfully used in production, potential precursor compounds must be reactive yet also possess sufficient stability to ensure safe handling, possess a suitable vapor pressure, and be pure enough so that the resulting film does not cause problems in the device (current leakage, threshold voltage shift, etc.) [15,16]. Compounds such as Tetrakis diethylamido hafnium (TDEAH), Tetrakis ethylmethylamido hafnium (TEMAH) and Tetrakis dimethylamido hafnium (TDMAH) have suitable physical and chemical

properties useful in CVD and ALD, but their purity is often questionable because of contamination traceable to the minerals from which hafnium is originally refined [17]. The vapor pressures of TDEAH, TEMAH and TDMAH are sufficiently high so that evaporation under a stream of an inert gas can be accomplished in a reasonably short time. To achieve Atomic Layer Deposition (ALD) characteristics and to be suitable as a practical vapor deposition process, ALD precursors must have specific properties. They must be sufficiently volatile (at least about 0.1 torr equilibrium vapor pressure at a temperature at which they do not decompose thermally). Furthermore, they should vaporize rapidly and at a reproducible rate, conditions that are usually met for liquid precursors, but not so much for solids. For self-terminating surface reactions, precursors must not self-react, including decomposing on the surface or in the gas phase. Precursors must also be highly reactive toward the other precursor previously attached to the surface, resulting in relatively fast kinetics and thus lower temperatures and cycle times [16]. Furthermore, the byproducts must be volatile and thus easily purged in order to prepare for the subsequent half-cycle. Moreover, byproducts should not be corrosive to prevent non-uniformities due to film etching and corrosion of the tool. Precursors having exothermic reactions with their complementary precursor tend to produce pure films because the ligands are completely removed. A large thermodynamic driving force also usually allows low deposition temperatures, resulting in the smooth, amorphous films needed for gate dielectrics [17]. Precursors for metal oxides are generally classified as metal precursors and oxygen sources. Metal precursors (ML_n) generally contain one metal atom M bound to n ligands L and can be categorized by the types and number of

atoms directly bound to the metal center as represented in Figure 14 [18]. Selecting precursors with all of the desired properties has not been straightforward because relatively little data is available, and detailed chemistry has not been well understood. The dominant reactions forming high-κ metal oxides appear to be ligand-exchange reactions as seen in Figure 15 [18]. When water is used as the oxygen source, as is common in CVD of high-k dielectrics, ligand-exchange involves breaking the metal-ligand bonds of the precursor and an O-H bond, and forming an M-O bond and a L-H bond. The strengths of the bonds that dissociate and form during the reactions directly determine the thermodynamics of the reaction and, less directly, influence the rates of reaction. Precursors with strong L-H bonds (again, when H_2O is used as the oxygen source) and weak M-L bonds have strongly exothermic reactions, tending to make pure, amorphous films at low temperatures [18]. Furthermore, unwanted side reactions will be less likely, and the process will usually be faster. However, the metal-ligand bond must be sufficiently strong for the precursor to be stable. Another important precursor property is its size. Ligands are attracted to each other through weak van der waals interactions and thus bulky ligands generally lower precursor volatility. However, bulky ligands can also shield the metal center from bonding interactions between precursors, thereby increasing precursor volatility. Because of these competing effects there may be an optimum ligand size that maximizes the precursor volatility. Large ligands can also restrict the packing density of precursors in the saturated precursor monolayer. However, more complete ligand exchange reactions during precursor exposure reduce the number of ligands remaining in the monolayer, increasing the monolayer density.

For ALD of hafnium oxide and hafnium oxynitride, hafnium ethylmethylamide, $Hf(N(CH_3)(C_2H_5))_4$, is a good liquid precursor, combining high reactivity toward water, ozone and ammonia, with sufficient volatility and stability. Tetrakis dimethyl amido hafnium (TDMAH) was chosen as the precursor for the deposition process of hafnium oxide films.

Labview Automation

Labview (short for Laboratory Virtual Instrumentation Engineering Workbench) is a platform and development environment for a visual programming language from National Instruments [19]. One benefit of Labview over other development environments is the extensive support for accessing instrumentation hardware. Drivers and abstraction layers for many different types of instruments and buses are included or are available for inclusion. These present themselves as graphical nodes. The abstraction layers offer standard software interfaces to communicate with hardware devices. The provided driver interfaces save program development time. Many libraries with a large number of functions for data acquisition, signal generation, mathematics, statistics, signal conditioning, analysis, etc., along with numerous graphical interface elements are provided in several Labview package options [20].

Automated pulsing of the precursor, purge gas and water vapor delivery was accomplished through Labview for precise delivery to the chamber. The user interface was made flexible to change the time (in seconds) for each valve and also the total number of cycles. The temperature of the delivery lines and heating of the precursor oven were also controlled by Labview through a thermocouple feedback. Substrate

temperature for the three different temperature profiles for in-situ cleaning, deposition, and annealing was controlled through a Boraelectric resistive heater and the temperature was controlled by a Labview thermocouple feedback. The UV lamp control was also automated through a Labview program. The details of the Labview code, including flowcharts and the user interface are provided in Appendix A.

Experimental Details

The monolayer photoassisted CVD system was used to process ultra-thin HfO_2 films. Figure 16 shows a schematic representation of bonding sites on substrate and of hafnium surface species during the reaction cycles of TDMAH and H_2O to grow HfO_2 film [20]. The HfO_2 films were deposited on n-type Si <100> substrates. The thickness of the films was 2-2.5 nm. To fabricate metal-insulator-semiconductor (MIS) capacitors, metal dots (Au and Al) were evaporated as front and back contacts respectively. Some relevant facts regarding the sample:

- Substrate: 2" Si <100>, n-type
- Resistivity: 1-10 ohm-cm
- Flats: 2
- Substrate thickness: 250-300 microns
- Surface: one side polish
- For the MIS structure Au was used as the front contact and Al as the back contact
- Thickness of the gold front contacts was between 190 nm and 203 nm. A dektak-3 surface profilometer was used to measure the thickness

- Thickness of the aluminum back contacts is 300 - 400 nm (approx)

Dots of various sizes were deposited initially to determine which was ideal. 1 cm, 4 mm, 3mm, 2mm, 1mm and 0.1mm was used initially. The area effect on leakage current density characterization is explained in the following chapter. 1 mm dots were used as they provided considerably good J-V characteristics. 16 dots were measured per sample, using a custom made shadow mask manufactured by the machine shop at Clemson University. After deposition, the diameter of these dots was usually measured individually by an optical microscope with 0.1 micron resolution to collect more accurate data on the diameters.

Typical Deposition process steps are listed as follows:

1. Clean Sample Ex-Situ in a 5 sec diluted 45% HF acid followed by three DI water rinses of 5 seconds each.
2. Load sample within 5 minutes of Ex-Situ clean into the deposition chamber.
3. Test Heater connection (for heater used it was about 12.6 ohm)
4. Rough pump the chamber and all gas lines keeping the MFC's closed
5. Open high vacuum valve and open precursor valve (Backing valve on)
6. At 10^{-5} Torr close the UHP N_2 Valve as line is leaky
7. Pump the chamber down to 2×10^{-7} Torr
8. Rough pump the water chamber below 1 m-Torr
9. Switch back to high vacuum chamber
10. At 2×10^{-7} Torr; close precursor valve and purge line valve V_1 and V_2
11. Close the high vacuum valve and backing valves

12. Open roughing valve
13. Supply 0.1 sccm UHP N_2 gas and start heating the sample. Add UV radiation. Once sample reaches in-situ cleaning temperature, add Hydrogen (20%) rest UHP N_2 and do the in-situ cleaning for desired time.
14. After the cleaning process, turn off the heater and UV radiation. Keep UHP N_2 gas flowing until the sample reaches room temperature. May have to close the roughing and open the backing valve to back the diffusion pump.
15. Once the sample reaches room temperature, stop flowing N_2 gas. Turn off UV.
16. Close H_2 and N_2 gas valves
17. Go to UHV mode with Venetian valve closed
18. Turn off UHV gauge
19. Turn on the heater for precursor and open Precursor and N_2 purge valve
20. Once the precursor oven temperature reached 85^oC, turn on the sample heater set at desired deposition temperature
21. Once the sample and precursor reaches the desired temperature, turn off precursor and purge valves
22. Turn off the gate valve and the backing valve and pump the water chamber down to 0.5 Torr
23. Close the water chamber roughing valve and open the backing valve
24. Close the backing valve and open the main chamber roughing valve again. Open purge line valve and start purging N_2.
25. Turn on UV lamp and start cycling steps (Labview program)

26. If necessary, for long cycles (thicker films) the process has to be stopped, including the UV source to open the backing valve for diffusion pump. This will usually take only a minute or less. This is done because of the limitations imposed by the roughing pump. Adding one more roughing pump would be necessary to exclude this step. For typically upto 75 cycles, it was found this was not necessary to do.
27. Once the deposition is completed, close precursor, purge gas and water valve and turn off heater and UV lamp.
28. Pump down the chamber to 2×10^{-7} Torr, keeping the N_2O line open
29. Gradually heat the sample to annealing temperature
30. Close the gate valve and backing valve and open roughing valve
31. Start flowing N_2O gas and turn on UV lamp. Do the annealing for desired time.
32. Close N_2O valve and turn off UV lamp.
33. Pump the chamber down to 2×10^{-7} Torr
34. Now the sample is ready to be taken out of the chamber for evaporation of metal contacts. The sample was usually loaded into the PVD chamber within 5 minutes of removing from the UHV chamber.

Evaporation of Metal Contacts

1. Turn Rotary Pump ON.
2. Turn Water chiller ON. Check temperature to be set at 10 ^{0}C
3. Turn gauges ON.
4. Wait for gauges to initialize and for the gauge on 3 to be < 2 10^{-2} Torr.

5. Turn the diffusion pump ON. This turns the heater to the pump ON and it takes 30 minutes for it to warm up approximately.
6. Turn the backing valve ON.
7. During the time that the pump is warming up the samples are loaded in the bell.
8. To open the bell jar, we need to let air in - Open the Air admittance valve.
9. Check for the filament loaded
10. Load the metal in the filament.
11. Place the shadow mask, sample for back Al evaporation, and the glass slide and position it according to what is required above the filament.
12. Close Bell Jar.
13. Place the aluminum shields back, place the bell jar back carefully and then the implosion guard with care. Close the air admittance valve.
14. Close the backing valve.
15. Turn on the roughing valve. The bell jar needs to be roughed. If the critical time has passed by now, the roughing valve can be kept open when the backing valve is closed for a period of 5 minutes, if not then it can be kept open for a period of 2 minutes.
16. Once the gauge 2 pressure had dropped below $4x10^{-2}$ Torr, close the roughing valve and open the backing Valve.
17. Turn the High-Vac valve ON.
18. Once the base pressure is reached, verify if the VARIAC is set at a zero.
19. Perform Al evaporation

20. Close the High-Vac valve.
21. Open air admittance valve
22. Open the bell jar and remove the samples and the shadow mask.
23. Close and Rough bell jar. For this close backing valve and open roughing valve.
24. Now close roughing valve and open backing valve.
25. Open High-Vac valve.
26. Wait for pressure to come down to $5x10^{-5}$ Torr.
27. Repeat instructions 18-26 and evaporate Gold dots using shadow mask for front contact
28. Close High Vac valve
29. Turn Diffusion pump OFF
30. Close Backing valve
31. Turn Rotary pump OFF
32. Turn the water chiller OFF
33. Turn Gauges OFF

After the above evaporation of front gold and back side aluminum contacts, the samples are now ready for electrical characterization. Typically, the J-V measurements were done within 10 minutes of removing the sample from the bell jar after evaporation. The C-V measurements were done immediately following the J-V characterization.

Electrical Characterization

The C-V measurements were carried out by using an HP 4140B Pico ammeter, HP 4280A 1 MHz C Meter/C V Plotter, and Sencore LC102 AUTOZ Capacitor Inductor Analyzer Current density-voltage (J-V) measurements were carried out by using an HP 4140B Pico ammeter. The thickness of the films was measured by a Sopra GES5 spectroscopic Ellipsometer and later verified through TEM measurements.

Results and Discussion

The developed process was used to grow excellent quality ultra thin HfO_2 films on silicon substrates. Table 1 shows details of the process conditions during the fabrication of various samples, before the design of experiments was done. For the purpose of sample naming, the letter 'M' is followed by three digits, which represents the sample number. Any number (either numerical or alphabetical) after the fourth position of the sample number actually implies the metal insulator semiconductor (MIS) device location on that substrate. For example, M004A3 means the sample number is M004 and the MIS device number is A3. This naming scheme has been followed throughout the entire study unless otherwise mentioned. Figure 17 shows the J-V characteristics of sample M012A3, at both positive and negative gate voltages. n-type silicon substrates were used during these experiments, The focus was more on the leakage characteristics while the p-MOS device would be in its off-state.

Table 2 shows the leakage characteristics of some more of the samples processed at various voltages. Figure 18 shows the J-V characteristics of some of the samples at positive and negative voltages. In the following chapters, there will be more discussion

on the data collected from some of the samples listed in table 1 and table 2 (samples M014, M016 and M012). The details of the other samples run during statistical optimization are given in Appendix B.

Conclusion

It is apparent from the data that the novel monolayer photoassisted CVD system is capable of producing high quality HfO_2 films. By adding UV radiation, in-situ cleaning and in-situ annealing we were able to achieve considerable improvement of the film quality. A more detailed discussion will be presented in the later chapters. The leakage current data presented is the best reported in the open literature so far. A systematically and statistically designed study has to be done in order to find the best possible combination of the process parameters. Precise and accurate control of gas flow, UV light and substrate temperature was provided through Labview automation. That has to be done for each of the materials being processed. The system can also be utilized for processing other ultra thin film materials with few modifications.

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Table 1 Sample numbers and processing conditions of samples processed.

Sample	**In-Situ**	**Ex-Situ**		**Hyd %**	**Anneal**	**Anneal**	**Dep**	**Dep**	**Front Area**	**Min Leakage**	**Max Leakage**
No.	**Time**	**Dip**	**Temp**		**Time**	**Temp**	**No. of Cycles**	**Temp**		**at 1 V**	**at 1 V**
M001	5 min	No	700C	5%	4 min	700C	80	300C	1mm	3.18E-08	5.36E-09
M002	5 min	No	700C	5%	4 min	**750C**	**70**	300C	1cm	4.08E-10	6.64E-10
M003	5 min	No	700C	5%	**10min**	750C	70	300C	1 mm	7.22E-11	8.70E-11
M004	5 min	No	**800C**	5%	10 min	750C	70	300C	1 mm	4.09E-11	5.36E-11
M005	5 min	No	800C	5%	10 min	**800C**	70	300 C	1 mm	2.82E-11	3.16E-11
M006	5 min	No	800 C	5%	10 min	800C	70	**250C**	1 mm	1.21E-11	4.43E-12
M007*		No	*ONLY*	*ELLIP*	*MEAS*	DONE					
M008	5 min	No	800C	5%	10 min	800C	**66**	250C	1 mm	6.30E-12	8.25E-12
M009	10 min	No	800C	5%	10 min	800 C	**67**	250C	1 mm	4.22E-12	4.18E-12
M010	**5 min**	No	800C	5%	10 min	800C	67	250C	1 mm	5.21E-12	5.67E-12
M011	5 min	No	**900C**	5%	10 min	800C	67	250C	1 mm	3.42E-12	2.32E-12
M012	5 min	No	**950C**	5%	10 min	800C	67	250C	1 mm	1.79E-12	2.10E-12
M013	5 min	No	950C	**10%**	10 min	800C	67	250C	1 mm	2.10E-12	3.20E-12
M114	**10 min**	No	950 C	10%	10 min	800C	67	250C	1 mm	1.06E-12	1.10E-12
M015	10 min	No	950C	**15%**	10 min	800C	67	250C	1 mm	3.21E-12	4.12E-12
M016	10 min	No	950C	15%	10 min	**850C**	67	250C	1mm	5.44E-12	6.27E-12
M017	10 min	No	950C	15%	10 min	**900C**	67	250C	1 mm	3.23E-12	2.24E-12
M018	10 min	No	950C	15%	10 min	**950C**	67	250C	1 mm	4.23E-12	6.77E-12
M019	10 min	No	950C	15%	**15 min**	950C	67	250C	1 mm	5.43E-12	5.23E-12
M020	10 min	**Yes**	950 C	15%	15 min	950C	67	250C	1 mm	3.12E-12	3.57E-12
M021	10 min	Yes	950 C	**20%**	15 min	950 C	67	250C	1 mm	4.56E-12	3.89E-12
M022	**8 min**	Yes	950 C	20%	15 min	950 C	67	250C	1 mm	3.44E-12	4.12E-12
M023	8 min	Yes	950 C	20%	**10 min**	950 C	67	250 C	1 mm	2.23E-12	2.77E-12
M024	8 min	Yes	**900 C**	20%	10 min	950 C	67	250 C	1 mm	2.17E-12	2.89E-12
M025	8 min	Yes	900C	20%	10 min	950 C	67	250 C	1 mm	1.99E-12	2.04E-12
M026			*ONLY*	*ELLIPSOM*	*MEAS*	DONE					

Table 2 Samples and their respective leakage current densities (J) at different voltages

No.	Sample #	J @ 0.3 V	J @ 0.5 V	J @ 0.8 V	J @ 1V
1	M032	4.23E-10	2.34E-11	4.34E-11	6.30E-12
2	M033	3.27E-09	3.44E-10	5.67E-11	4.18E-12
3	M034	2.33E-11	4.56E-11	6.78E-11	5.21E-12
4	M035	1.23E-09	3.45E-11	6.78E-11	2.32E-12
5	M036	2.02E-10	4.56E-11	5.35E-11	1.79E-12
6	M037	1.23E-10	7.89E-11	4.34E-11	2.10E-12
7	M038	1.44E-10	3.45E-11	8.98E-11	1.06E-12
8	M039	1.22E-10	4.53E-11	6.56E-11	3.21E-12
9	M040	4.44E-11	4.56E-11	7.86E-10	5.44E-12
10	M041	1.21E-11	3.45E-11	8.95E-10	2.24E-12
11	M042	2.36E-11	6.72E-11	9.90E-11	4.23E-12
12	M043	3.43E-10	5.65E-10	7.89E-11	5.23E-12
13	M044	1.32E-11	6.74E-11	8.87E-11	3.12E-12
14	M045	3.24E-11	7.72E-11	8.78E-11	3.89E-12
15	M046	2.37E-11	6.62E-11	7.87E-11	3.44E-12
16	M047	1.07E-11	4.34E-11	6.49E-11	2.23E-12
17	M048	1.23E-11	4.67E-11	5.67E-11	2.17E-12
18	M049	3.56E-11	5.48E-11	7.34E-11	1.99E-12

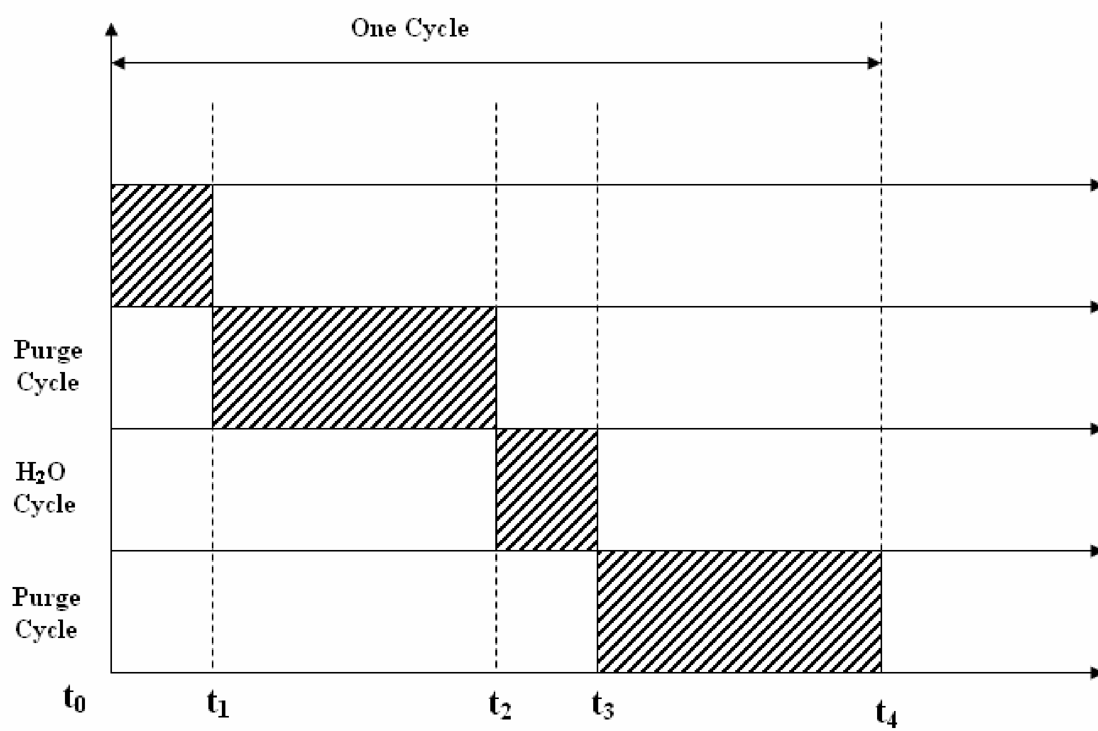


Figure 4 Cycling steps showing time profiles

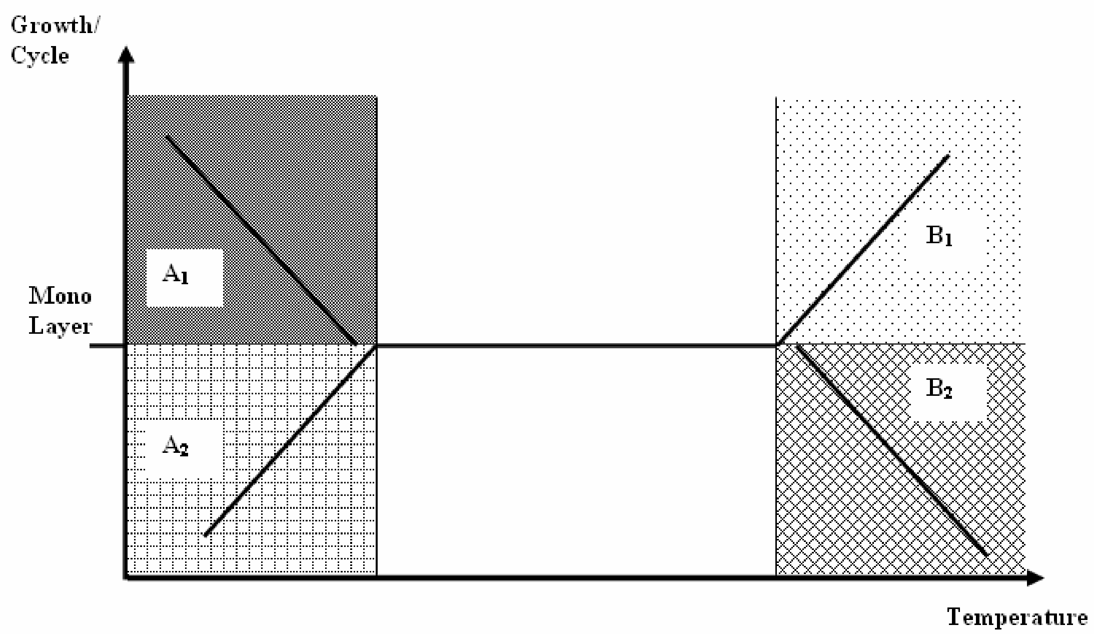


Figure 5 Processing window of the monolayer photoassisted CVD process

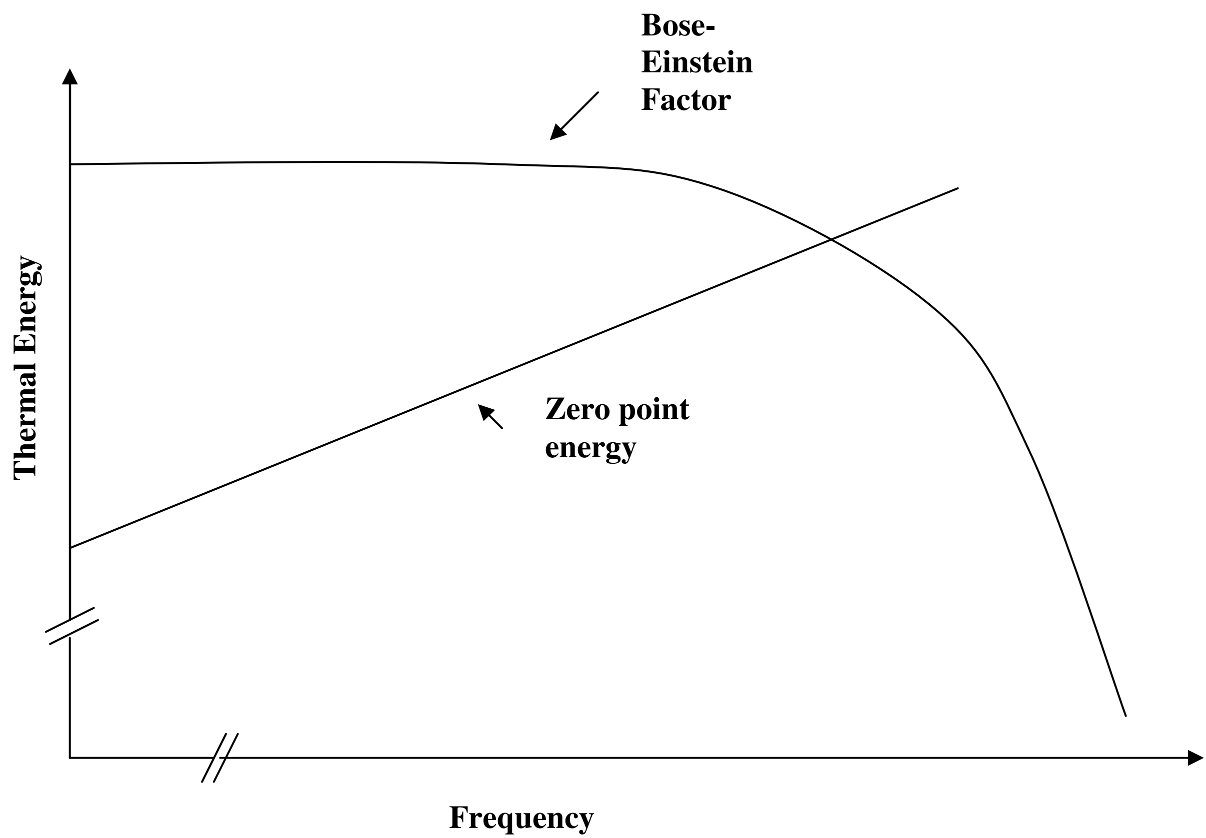


Figure 6 Representation of Bose Einstein factor in thermal energy dependence with frequency [4].

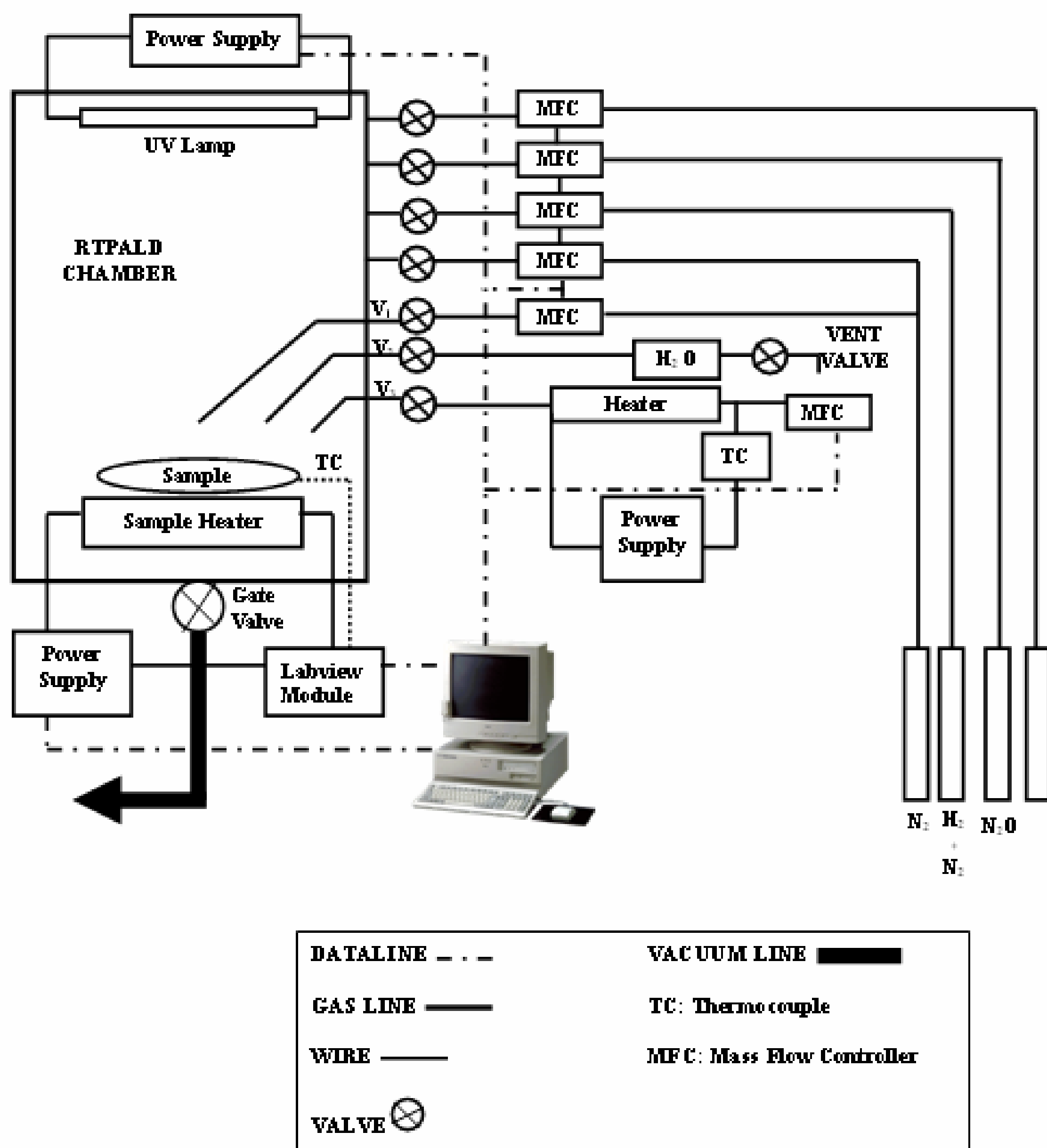


Figure 7 Schematic diagram of the monolayer photoassisted CVD system

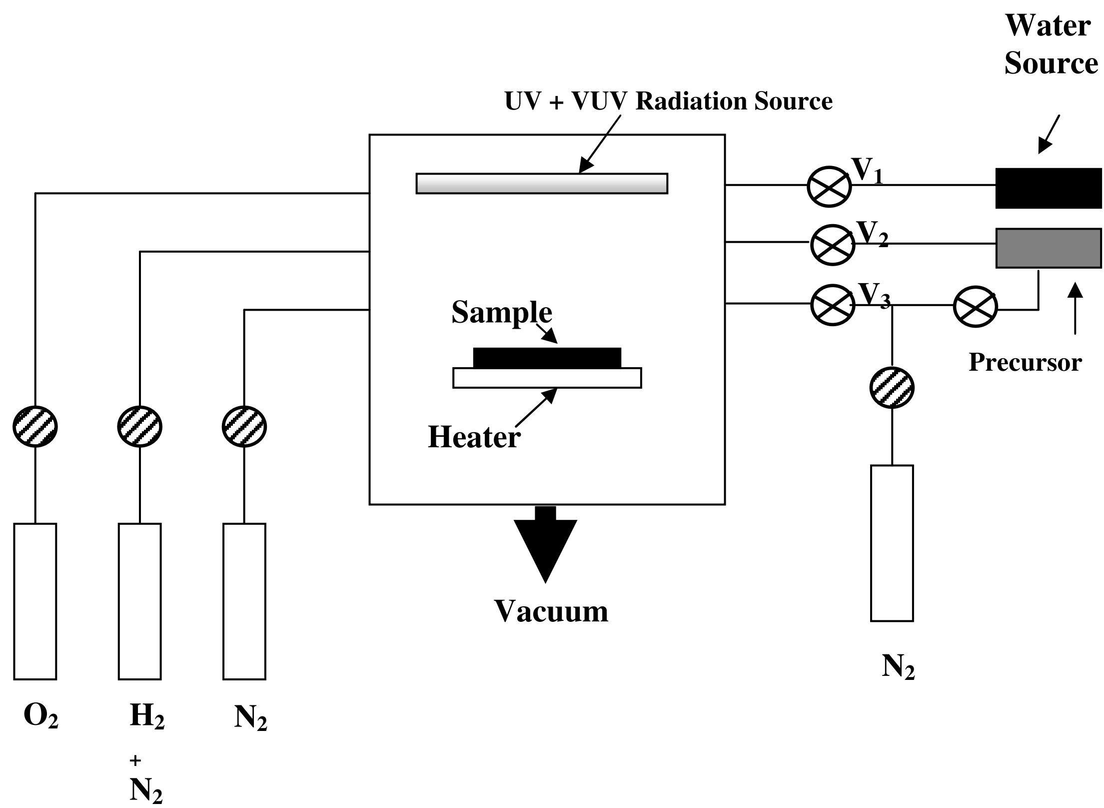


Figure 8 Simplified diagram of the monolayer photoassisted CVD system

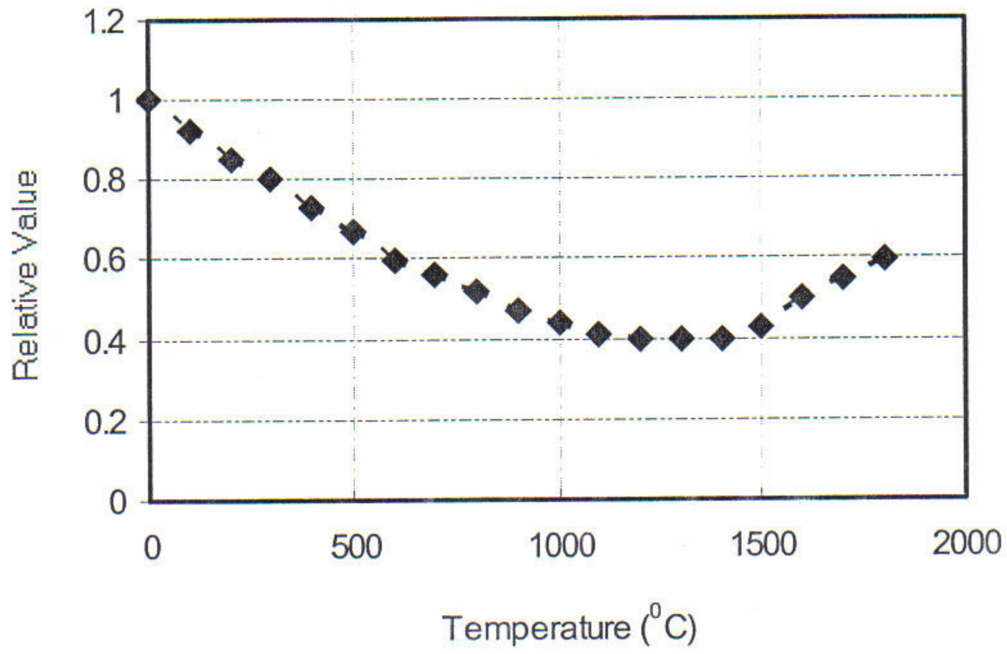
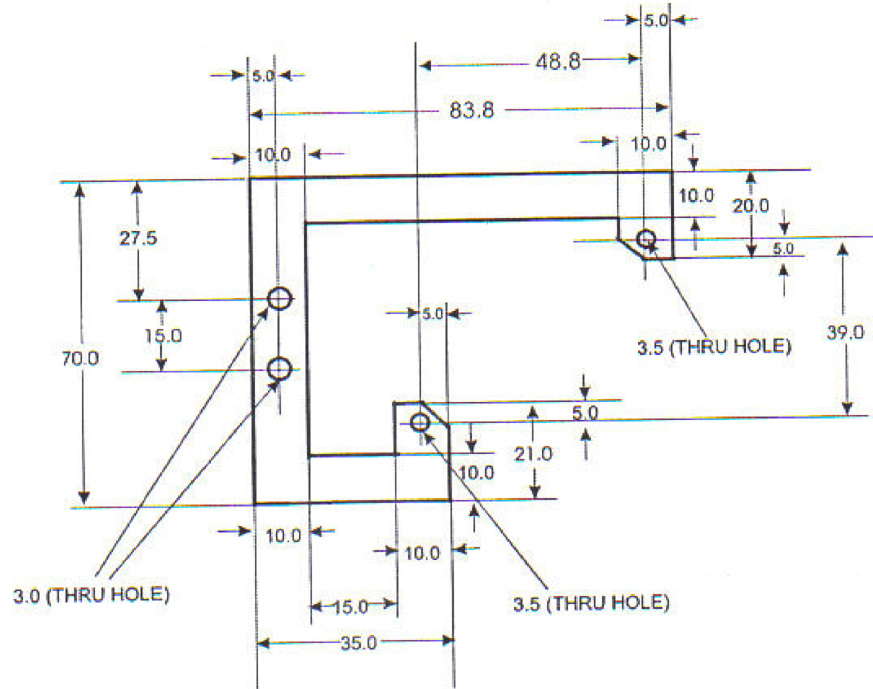
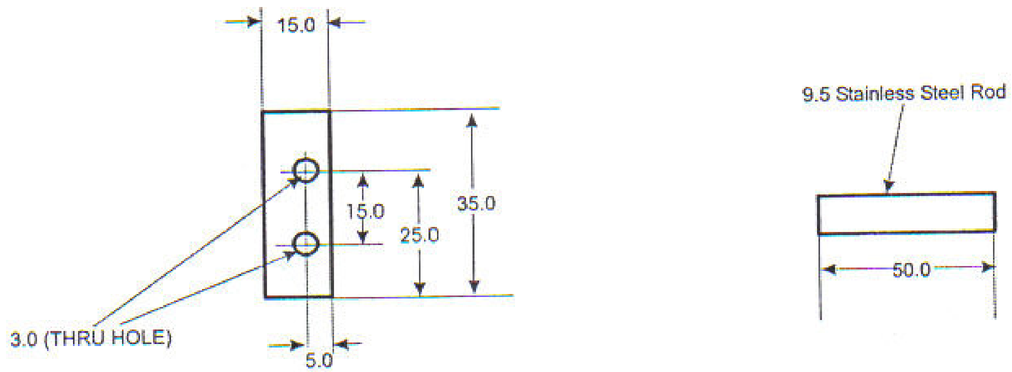


Figure 9 Resistivity of the PG conductive film in a Boraelectric® heater [12, 13].





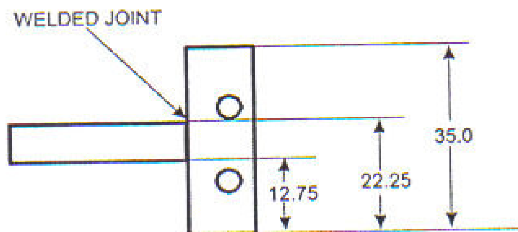


Figure 10 Heater mounting plate

CH	Model Number	Rated Gas	Flow gas	Range	Act Flow	Mode	GCF
2	1479A11CS1BM	N2	N2	10 sccm	0.2 sccm	Indep	1.000
3	1479A52CS1BM-S	H2	N2	500 sccm	20 sccm	Indep	0.990
4	1159B11413393	N2	O2	500 sccm	10 sccm	Indep	1.000
5	1179AS2CS1BV-S	Ar	N2O	500 sccm	10 sccm	Indep	0.518
6	1179A12CS1BU-S	H2	H2	100 sccm	3 sccm	Slave to 3	1.000

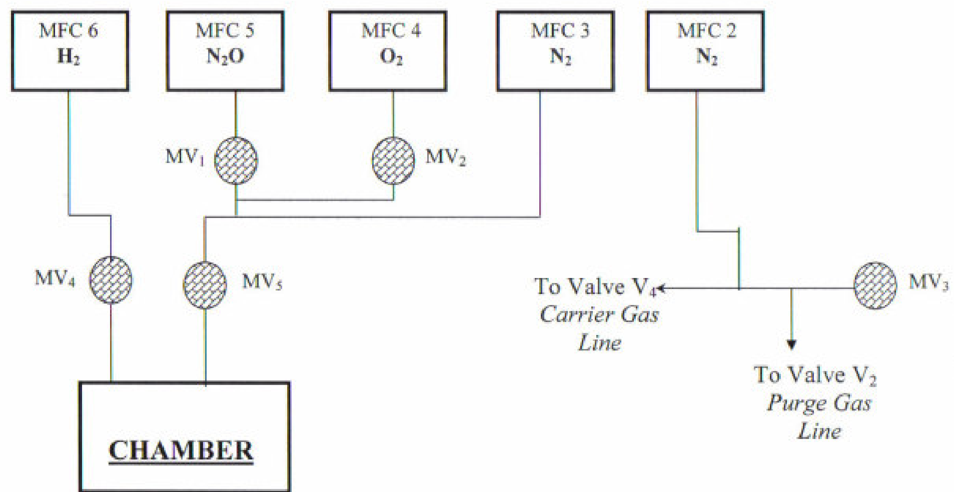


Figure 11 Detailed gas flow connections

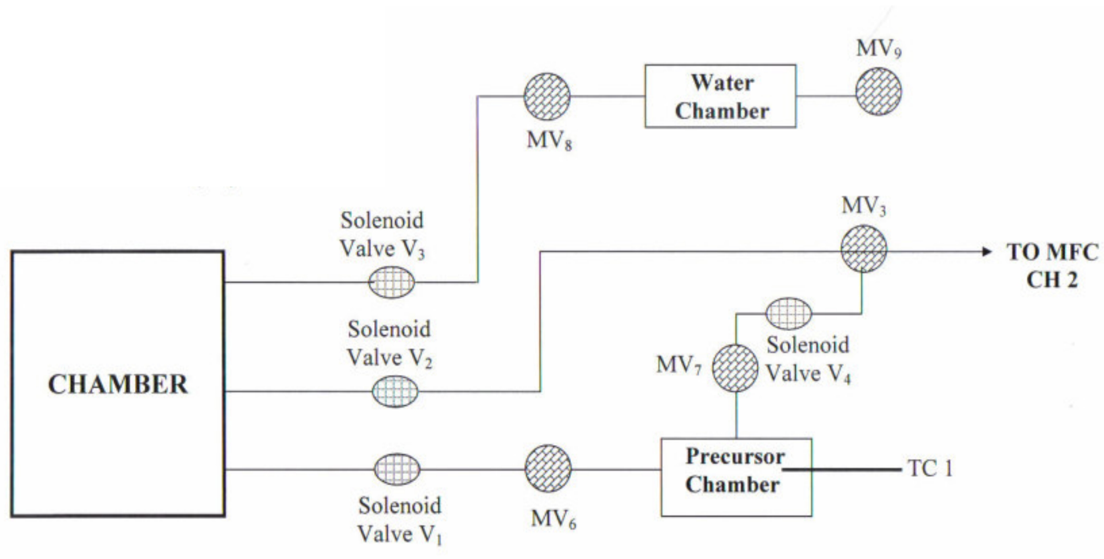


Figure 12 Precursor delivery line connections

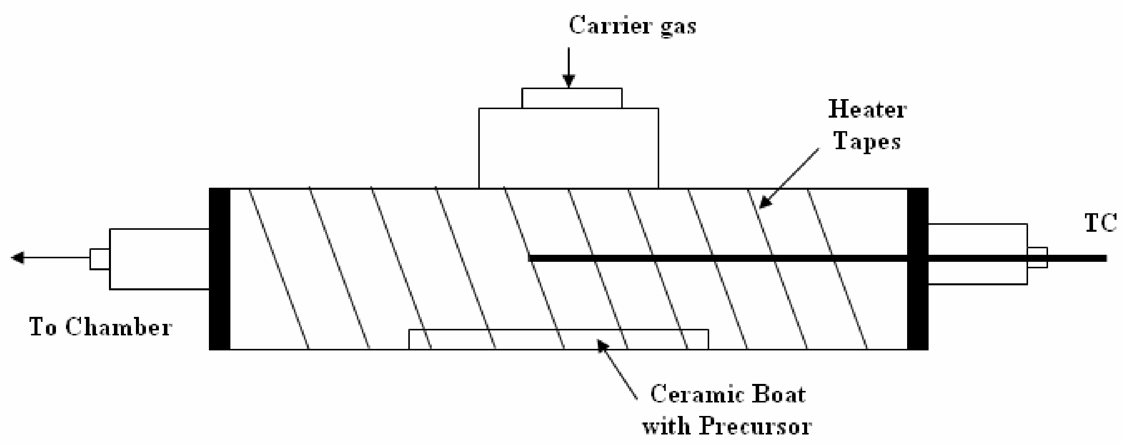


Figure 13 Precursor delivery system

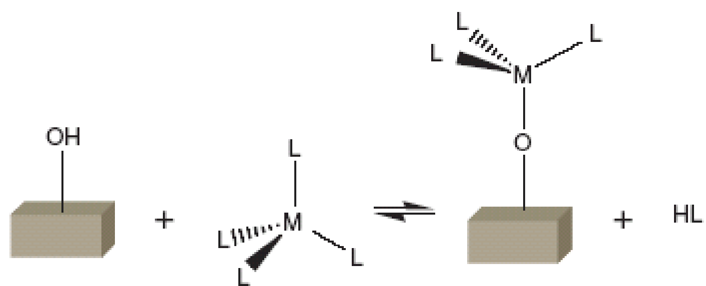


Figure 14 Schematic of a ligand exchange reaction for a ML_4/H_2O ALD [16]

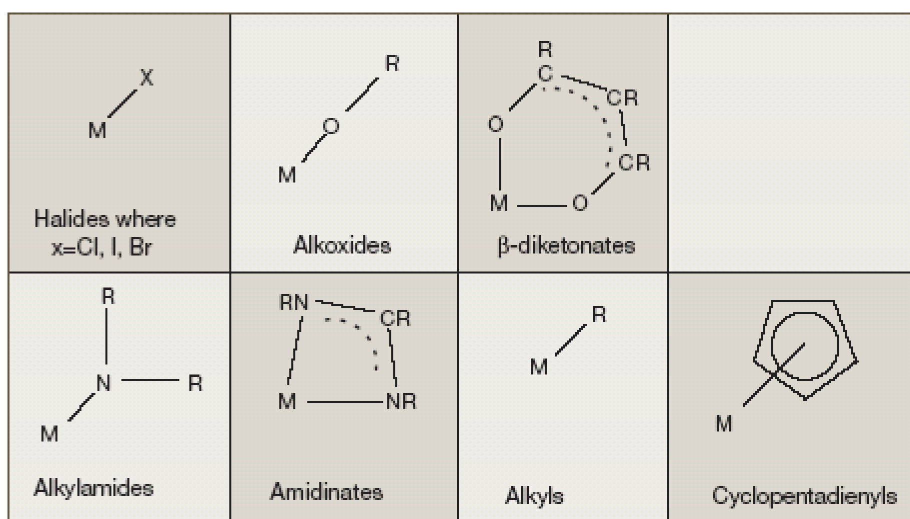


Figure 15 Precursor types - R's represent alkyl groups consisting of carbon and hydrogen, such as methyl (CH_3) or ethyl (C_2H_5) [17]

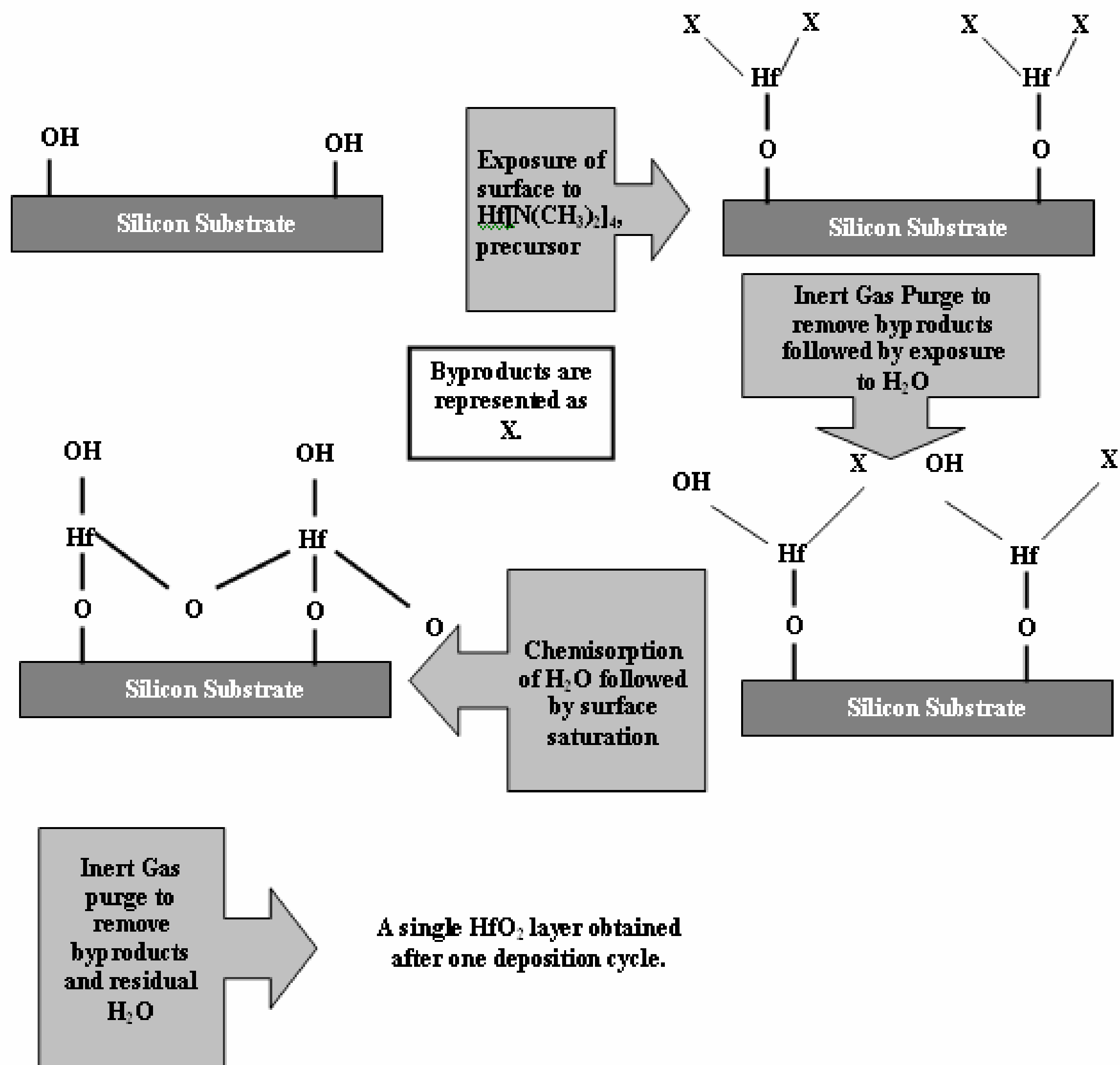


Figure 16 Formation of a single HfO_2 layer for one deposition cycle

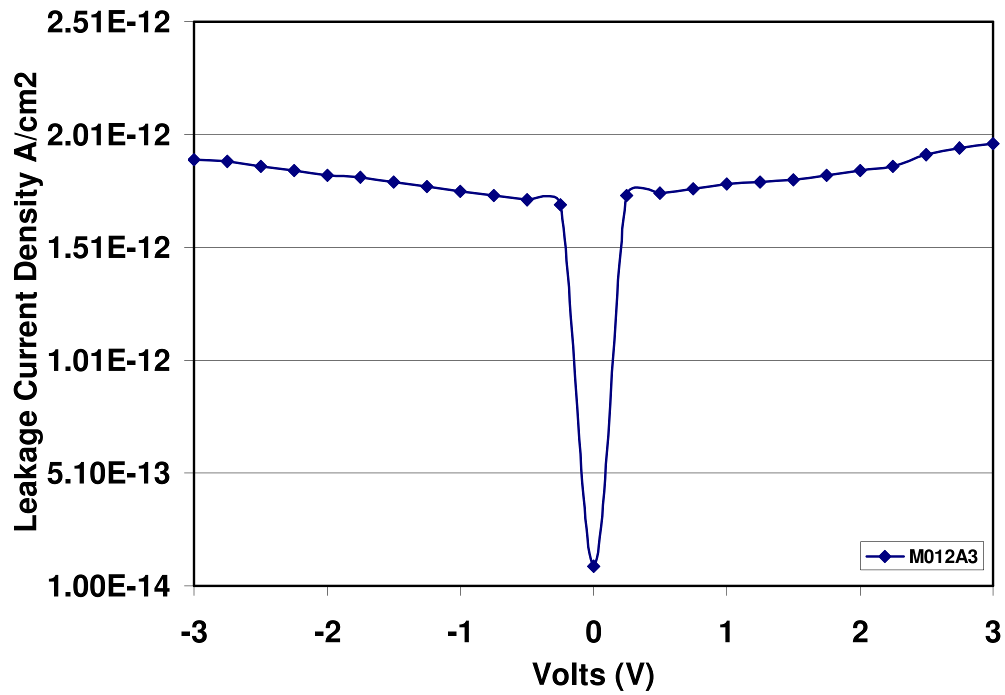


Figure 17 Leakage current density vs. voltage characteristics of sample M012A3 measured at both positive and negative gate biases

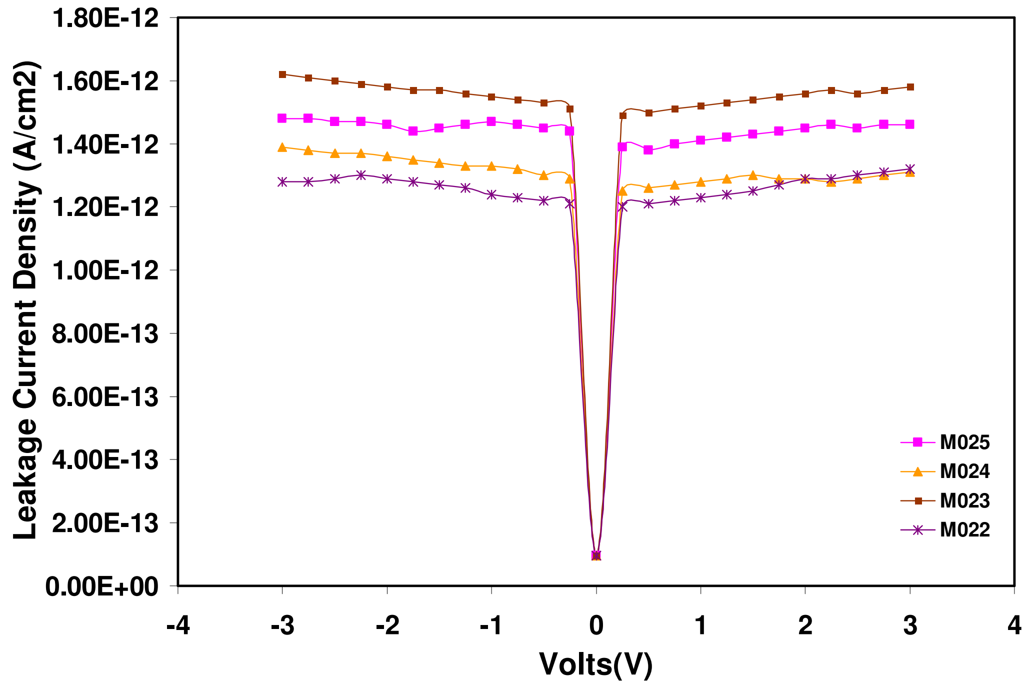


Figure 18 Leakage current densities of different samples processed differently by using the RTPMLD system. Process parameters for each of these samples are listed in Table 1.

CHAPTER 4

OFF STATE GATE CURRENT LEAKAGE POWER REDUCTION BY HFO_2

Introduction

Of all the issues facing chip and computer designers, none is more burning than the soaring levels of power flowing through integrated circuits [1]. Future big data centers might need 10 MW to run the computers and a further 5 MW to keep them cool enough to operate [1]. Thus power reduction of future generations of CMOS products is also very important from the point of reduction of carbon emission [2]. As compared to low-speed microprocessors, the high speed microprocessors generate more heat. On October 15, 2004 Intel announced the plans to scrap a milestone to introduce high speed microprocessors [3]. This was due to the fact that the Pentium 4 operating at 3.6 gigahertz draws 115 watts, compared with 84 watts for microprocessors operating at 3.2 gigahertz and below. The higher wattage microprocessor needs advanced cooling techniques and as a result packaging becomes more expensive. Starting from technology nodes of 65 nm and below, the off state leakage related power dominates the total power [4]. Thus reduction of leakage current related power becomes an important challenge. At the cost of profitability, Intel and other leading microprocessors are currently using two or more microprocessors in a single package. Each microprocessor in the dual core microprocessor operates at lower speed and generates less heat. Recently in January 2007, Intel Corporation announced that it will incorporate the use of high-κ dielectrics for the 45nm technology node [5], and the leakage current density has been reduced by one

order of magnitude [6]. The leakage current density for a current 1.2 nm silicon dioxide layer is about 100 A/cm^2 [7]. Although the gate current density reduction by an order of magnitude, provides some relief to the heat dissipation problem at the 45 nm technology node, the leakage current density is not low enough to further scale down CMOS to its fundamental limit of < 10nm. As shown in Table 3, the gate current density achieved so far is 2-3 orders of magnitude higher than the value required for the next generation of technology nodes. The presence of gate leakage current also has significantly increased the CMOS design complexity. The invention of a high-k gate dielectric material that can provide leakage current density at a level where the designer can assume a gate dielectric of current zero will solve a number of design problems.

In this chapter we report the results of a unique process to grow high-k dielectric materials. For an effective oxide thickness of 0.39 nm, we have achieved a leakage current density as low as 1x 10^{-12} A/cm^2 at a gate voltage of +3 to -3 V. Detailed characterization of the deposition characteristics has been performed to fully understand the precursor saturation behavior, thickness linearity, substrate temperature dependence, in-situ cleaning dependence on time, temperature and % hydrogen and annealing performance dependence on time, temperature, and % hydrogen. Detailed TEM characterization was performed to estimate the thickness and for the calculation of EOT and dielectric constant.

Impact of Zero Gate Dielectric Current On Future Generations Of CMOS

Any and all reductions of leakage current assist in the overall goal of reducing power consumption. The ability to reduce the gate current orders of magnitude below 10A/cm^2

using a high-κ dielectric is important since this is a significant component in the static power consumption equation at <65nm node.

Another important consequence of "zero" gate current is in the design of circuits which rely on gate charge storage for successful operation. Examples of these include switched capacitor, dynamic logic and voltage generator circuits. Reduced gate leakage current in the pA/cm^2 range will significantly improve the circuit designer's ability to implement these techniques with minimum sized devices. The net result is a reduction in dynamic power consumption.

Leakage is a dominant factor in sub threshold designs and many of the current techniques to reduce power consumption are all attempts to mitigate the effects of leakage. A process which significantly reduces the leakage by eliminating the dielectric leakage current is extremely desirable.

Experimental Procedure

A home-built monolayer photo-assisted CVD system was used for the deposition of hafnium oxide films. Hafnium oxide films were deposited on low resistivity 1-10 Ω-cm, <100> n-type Si substrates. The process flow is shown in Figure 19. Before processing each sample, an ex-situ etch was performed, where each sample was etched in 48% HF diluted in a 1:25 ratio with DI water. The sample was then placed within 5 minutes in a high vacuum chamber, which was pumped to a pressure of 2 x 10^{-7} Torr prior to processing the sample. Forming gas (20% H_2, and 80 % N_2) was used for in-situ cleaning, followed by the growth of the HfO_2 gate insulator. For the deposition of the oxide layer, Tetrakis dimethylamino hafnium $Hf[N(CH_3)_2]_4$, also referred to as TDMAH was used,

and H_2O as the co-reactant for oxidation. The layers were deposited in 65 cycles, where each cycle consisted of a TDMAH pulse, an N_2 purge pulse, a H_2O vapor pulse and again an N_2 purge pulse. The TDMAH and H_2O pulses had duration of 1 second, while the N_2 purge pulses were applied for 5 seconds. After the sample was annealed in a N_2O ambient, the sample was transferred to a PVD chamber for deposition of the front Au and back Al contacts for electrical characterization. The front contact area was normally 0.00785 cm^2 and 16 dots were measured per sample. Ultraviolet (UV) light was applied throughout the in-situ cleaning, deposition and annealing of hafnium oxide. The temperature profile for the entire process is shown in Figure 20.

The thickness of the films was measured by a Sopra GES5 Spectroscopic Ellipsometer and verified using high resolution transmission electron microscopy (HRTEM) and C-V data. The C-V measurements were carried out by using an HP 4140B Pico ammeter, HP 4280A 1 MHz C Meter/C V Plotter, and a Sencore LC102 AUTOZ Capacitor Inductor Analyzer. Current density-voltage (J-V) measurements were carried out by using an HP 4140B Pico ammeter.

Experimental Results

a. Deposition Rate – Saturation behavior and Linearity

Different amounts of the hafnium precursor (TDMAH) were delivered into the UHV chamber by adjusting the TDMAH pulse time at a substrate temperature of 250 ^oC. The deposition rate increased sharply as the TDMAH pulse time increased from 500 ms to 1 sec as can be seen from Figure 21. Further increase of the TDMAH pulse time above 1 sec caused the deposition rate to increase slightly showing that the hafnium precursor

reaction was reaching a self limited state for hafnium pulse times above 1 sec. The slow increase of the deposition rate indicates a gradual saturation behavior of TDMAH.

By changing the number of cycles of deposition in the experiment, the thickness of the deposited film changed linearly. Figure 22 shows the growth rate to be fairly linear, with the slope of the fitting line representing the deposition rate in angstroms per cycle. During the process optimization, by varying the deposition process parameters, several samples were generated for values of leakage current density measured at V_G=-3V to +3V. These results are shown in figure 23.

b. Substrate temperature dependence of deposition rate

In figure 24 it is seen that as the substrate temperature is increased from 200 ^oC to 300^oC, the film deposition rate decreased slightly. As the substrate temperature increased to 350^oC, the deposition rate started to increase, indicating the onset of thermal decomposition of TDMAH. As the substrate temperature increased to 400^oC, the deposition rate increased sharply, indicating that much more thermal decomposition took place in film deposition. Therefore in the current experimental setup, to have a good monolayer photoassisted deposition process for TDMAH, it is necessary to deposit films at a substrate temperature lower than 300^oC.

c. Annealing and In-Situ Cleaning Optimization

In order to optimize the process recipe, annealing parameters of anneal time and anneal temperature were investigated to optimize leakage current density. Figure 25 shows that as annealing temperature is increased from 700^oC to 900^oC, the leakage current density improves to 1.12 x 10^{-12} A/cm^2. As shown in Figure 26, with increase of the annealing

time from 5 minutes to 8 minutes the leakage current density improves to 1.10 x 10^{-12} A/cm^2. Further increase of the annealing time to 9 minutes did not improve the leakage current density any further.

To optimize the in-situ etch parameters, the in-situ temperature and time were also investigated to optimize leakage current density. As seen in Figure 27, as the in-situ cleaning temperature was increased from 700°C to 900°C, leakage current density improved to 1.10 x 10^{-12} A/cm^2. As seen in Figure 28, as in-situ cleaning time was increased from 3 minutes to 8 minutes, the leakage current density improved to 1.00 x 10^{-12} A/cm^2.

d. Growth Rate dependence on UV

In order to study the effect of UV/VUV on the TDMAH precursor used in this study, for two different substrate temperatures of 300°C and 400°C, the deposition characteristics of precursor pulse time, purge times, water vapor pulse times and number of cycles was kept identical and for one sample UV was used and another it was not. This was repeated for 2 different thicknesses, so that a thickness linearity distribution could be developed to calculate the growth rate per cycle. Thickness was measured by the Sopra Ellipsometer and the results are plotted in Figure 29. As can be seen from the results, for both temperatures UV provided an enhanced growth rate for the deposition of HfO_2.

e. Effective Oxide Thickness Measurement

High-frequency capacitance-voltage measurements were done at a frequency of 1 MHz. Figure 30 shows the C-V measurement of a typical sample. Figure 31 shows high-resolution cross-section TEM results in <110> direction of the HfO_2/ Si (001) specimen.

The interface between HfO_2 and Si(001) is atomically sharp with thickness of the oxide estimated to be 2.35 ± 0.05 nm. There is polycrystalline silicon above the oxide which is deposited as a protective layer for the oxide for the cross-section TEM. TEM data showed that the hafnium oxide layer appears conformal to the (100) silicon substrate having a uniform thickness. Figure 32 delineates the atomic structure of the oxide-silicon interface with arrow showing the oxide thickness. Figure 33 is a <110> cross-section transmission electron microscopy (TEM) micrograph, showing the presence of amorphous HfO_2 layer about 2nm thick. A thicker layer (about 40nm thick) of amorphous silicon oxide was deposited to protect the hafnium oxide layer near the interface.

TEM and Ellipsometry measurements correlated to show that the thickness of the oxide grown was 2.35 nm. The C-V measurements yielded a C_{max} of ~75 nF. The interfacial SiO_2 thickness was estimated to be 0.2 nm from TEM measurements. The total dielectric thickness $t_{tot=}\ t_{SiO2}+t_{highk}$ was calculated to be 2.37 nm. The dielectric constant calculations were done based on this data to get a dielectric constant of 25.42. Based on C-V, ellipsometry and TEM data, the EOT of 0.39 nm was calculated using the equation given below.

$$t_{eq} = t_{SiO2} + (\frac{k_{ox}}{k_{high-k}})t_{high-k} \qquad (1)$$

f. XRD Measurements

To show that RPP assisted CVD provides higher throughput material with less defects, we have shown the X-ray diffraction of HfO_2 films deposited with and without using UV

high energy photons in Figure 34. The use of optical energy reduces the defects in the deposited films. The large peaks indicate preferred orientations, and it is evident that a single crystal orientation is preferred and a higher ratio of the orientations indicated lower defects. In the case with UV, the results clearly demonstrate the importance of optical energy in providing films with higher throughput and lower defects in the deposited films. In the case of RPP assisted CVD, the process activation energy is reduced both in nucleation growth and bulk transport regions. As a result, it provides better materials than any other processing technique [8]. As an example, in the case of higher dielectric constant materials presented in this study, we have reported the lowest leakage current density (1 pA/cm^2 at 1 V) [8] ever reported for any non-silicon based dielectric constant material [9 – 17]. The continued scaling of CMOS below 45 nm may provide unacceptable off-state leakage currents or may degrade device performance and the process and tool presented in this study will allow the further scaling of CMOS to 10 nm feature sizes [18 - 20].

Manufacturability

As CMOS device features are continuously shrinking beyond the 65-nm technology node, effects due to process variation are becoming more pronounced on device performance, and reliability. Process variation can therefore result in the reduction of yield and increases the cost of automatic process control (APC). In order to reduce the number of design iterations and design cycle time, process variation should be controlled as early in the CMOS process flow as possible. Since capital being invested into new tools for the larger diameter wafers is at a premium, manufacturers must search for ways

to reduce the cost of the tool. If the process and the tool in question have an inherently reduced variation, then there is a direct reduction in cost associated with process control resulting in more economical cost of production and also better yield. Our process has reliably demonstrated the success achieved with low process induced variation of the system and this is the driving factor to convincingly make this an attractive alternate choice to existing tools.

Several samples were generated at the same optimal processing conditions to determine the descriptive statistics for leakage current density. A 99% prediction interval for the leakage current density at V_G=1V lies between 0.97e-12 A/cm^2 to 1.11e-12 A/cm^2. Also a two-sided tolerance interval that contains 99% of the population of wafer leakages with 99% confidence lies between 0.92e-12 A/cm^2 to 1.16e-12 A/cm^2. The details of design of experiments and related details will be published elsewhere.

Discussion

Figure 35 shows mean values of leakage current density measured for an optimized typical sample at V_G=-3V to +3V. The leakage current density of 1.06 x 10^{-12} A/cm^2 for an EOT of 0.39 nm at 1 V represents the lowest value of leakage current reported by any one to date. The comparison in terms of leakage current density vs. EOT between our results with other reported results in the literature [8-16] is shown in Figure 36. It shows that our leakage current density with an EOT of 0.39 nm is four orders of magnitude lower than the best published results at higher EOT values. Three samples which were processed at the same optimal conditions were measured; 25 points were measured on each sample to test for repeatability of leakage current density. Figure 37 shows the

measured sample points showing the interval to be between 1.06 x 10^{-12} A/cm^2 to 1.26 x 10^{-12} A/cm^2.

To investigate the effect front contact area has on leakage current density, samples processed under the same conditions were deposited with various diameter of the capacitor. As shown in Figure 38, with the reduction of the diameter of the capacitor from 4 mm to 2 mm, the leakage current density reduces in a fairly linear fashion. The 0.1 mm diameter capacitor gave the lowest leakage current density, which was the lowest leakage current value the measurement instrument could detect.

Conclusion

In this chapter we report the results of a new process and tool to deposit metal/high-k gate dielectric stacks. We report the results of a 0.39 nm effective oxide thickness (EOT) gate dielectric material with a leakage current density of about 1 x 10^{-12} A/cm^2 for gate voltages from +3V to -3V. The process is extremely repeatable, robust, and will transfer from a laboratory to a manufacturing environment with no major hurdles. The availability of such a tool for manufacturing with gate leakage current equal to zero will simplify the design complexity and will reduce design for manufacturing cost of the next generations of CMOS advanced products. This is a major breakthrough and will have a significant impact on silicon IC manufacturing.

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Table 3 Gate current related power consumption data from ITRS roadmap for future generations of CMOS (Source: ITRS updated roadmap for 2006)

Technology Node (nm)	Vdd (V)	Jg (A/cm^2)	Power (W/cm^2)	EOT (nm)
32	1.1	1.88E+02	2.07E+02	1.2
28	1.1	5.36E+02	5.90E+02	1.1
25	1.1	8.00E+02	8.80E+02	1;1
22	1	1.18E+03	1.18E+03	1.0
20	1	1.10E+03	1.10E+03	0.90
18	1	1.22E+03	1.22E+03	0.65
16	1	6.25E+02	6.25E+02	0.80
14	0.9	7.86E+02	7.07E+02	0.70
13	0.9	8.46E+02	7.61E+02	0.60

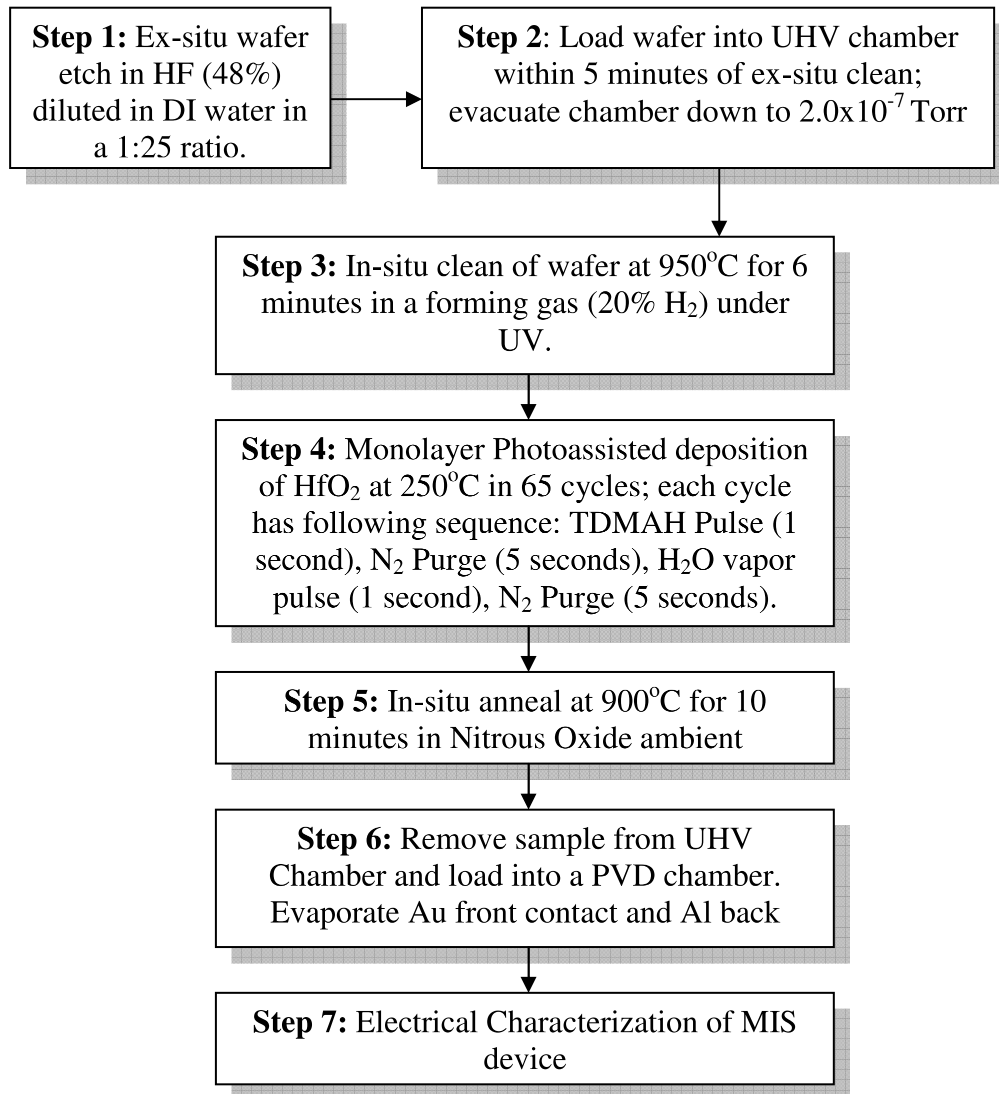


Figure 19 Experimental process flow for deposition of hafnium oxide

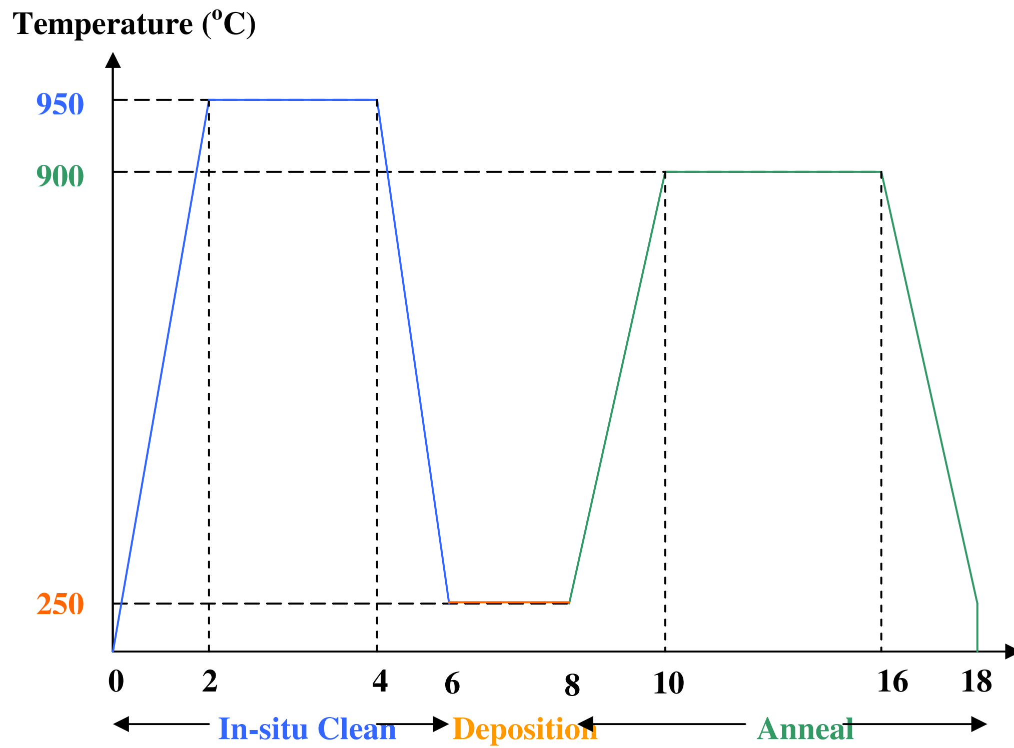


Figure 20 Temperature profile during monolayer photoassisted deposition process

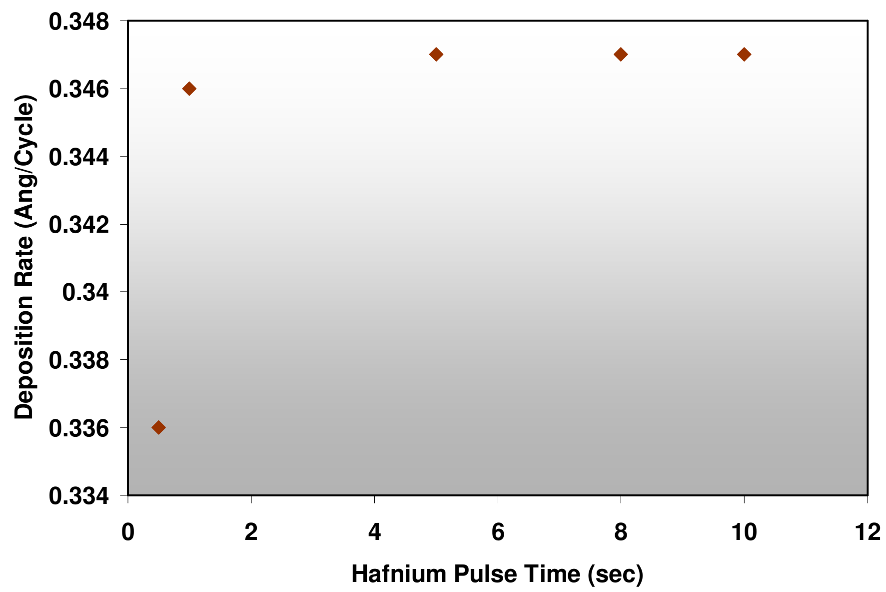


Figure 21 Deposition rate as a function of Hafnium precursor pulse time

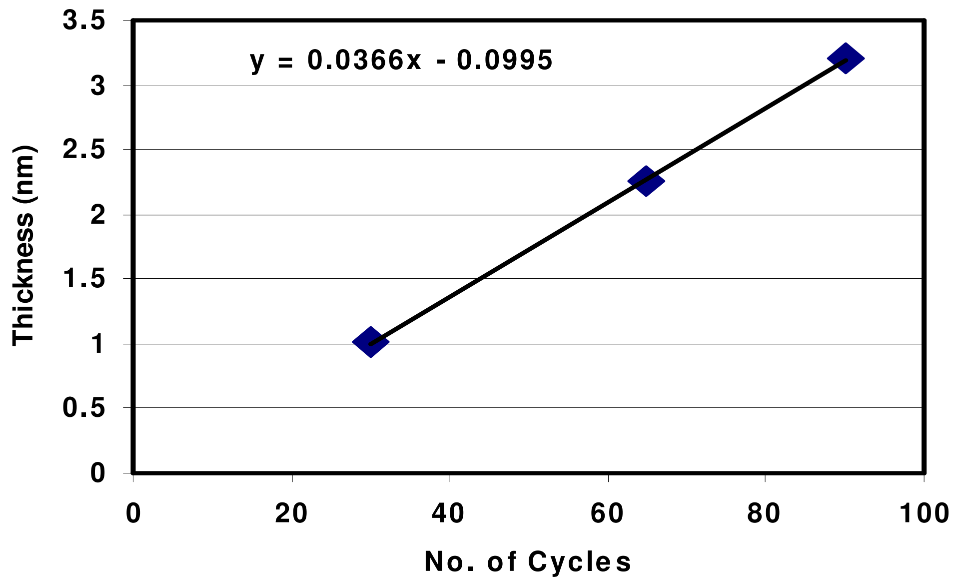


Figure 22 Film Thickness as a function of number of cycles used in the deposition process

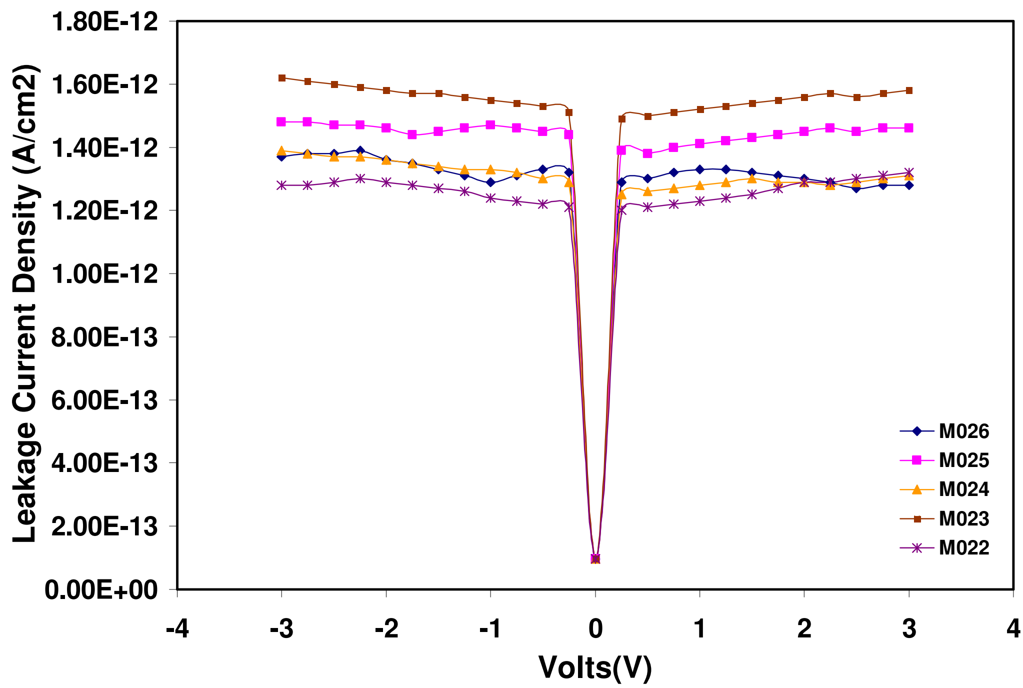


Figure 23 Leakage current density for various samples during deposition parameters optimization

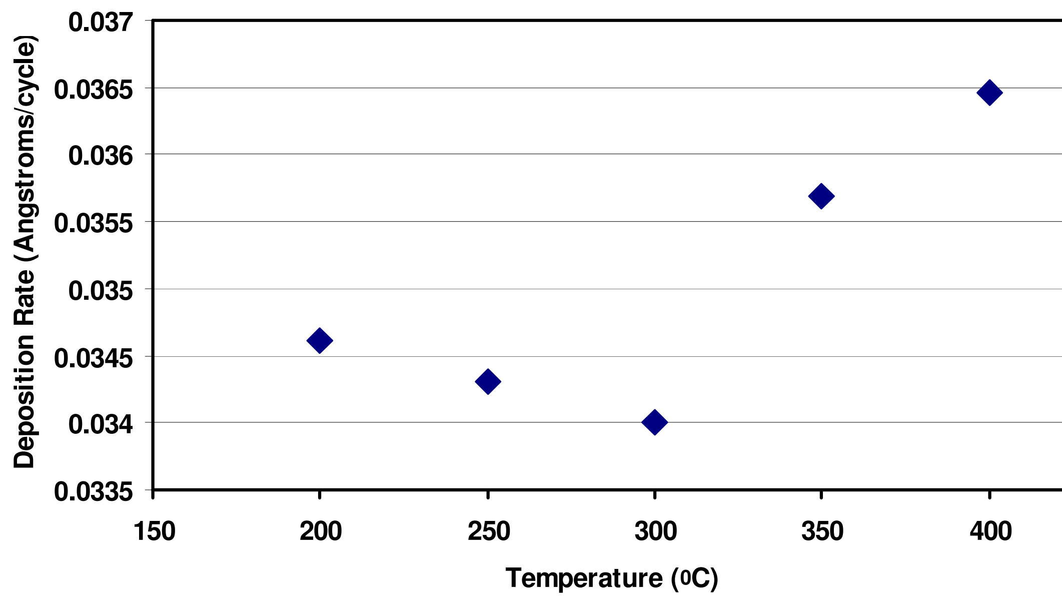


Figure 24 Temperature dependence on deposition rate

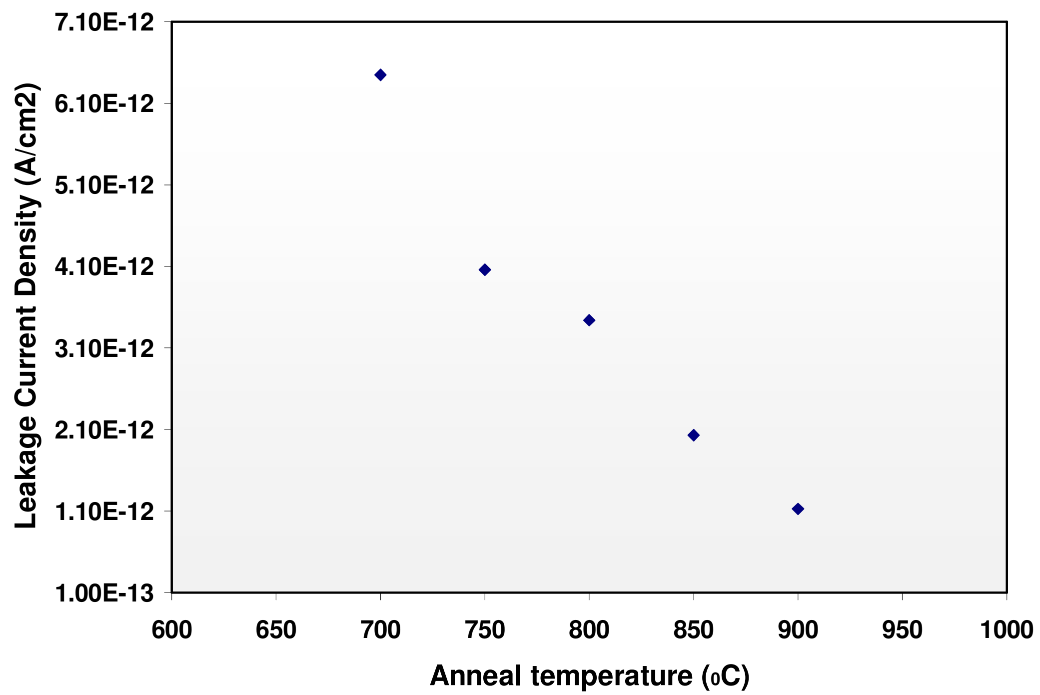


Figure 25 Anneal temperature dependence on leakage current

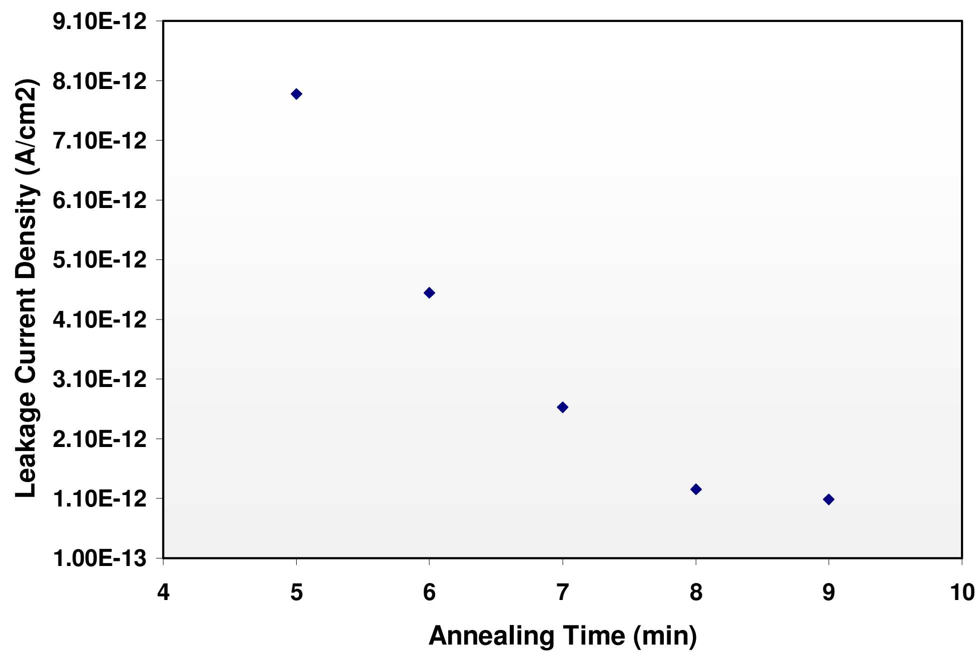


Figure 26 Anneal time dependence on leakage current

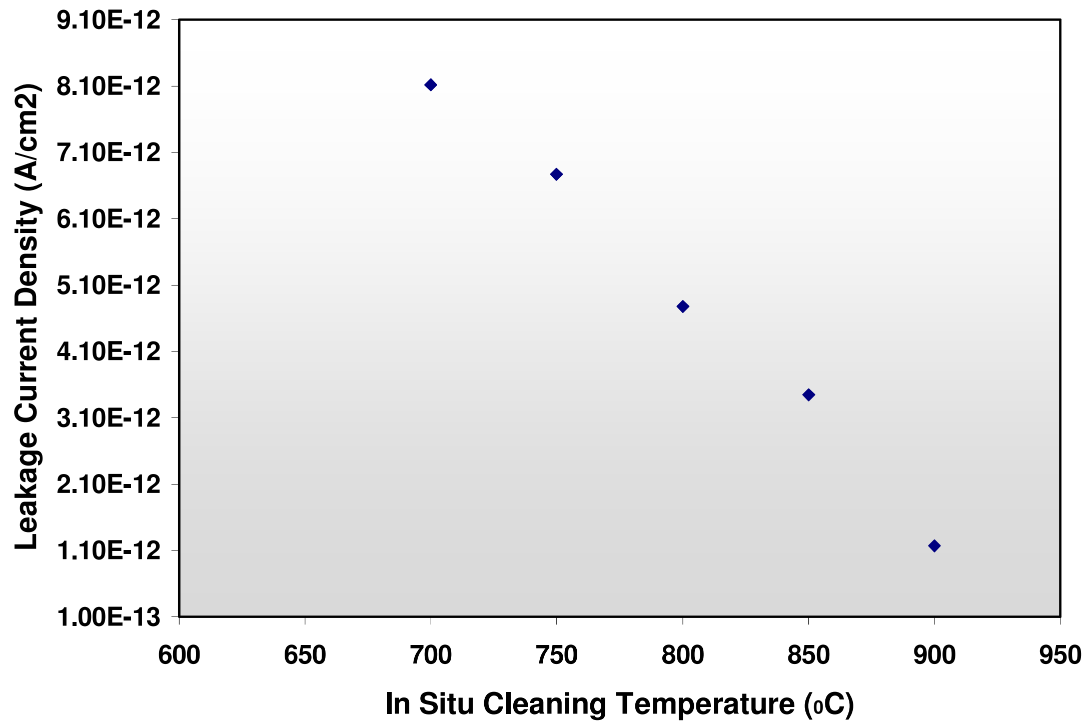


Figure 27 In-situ cleaning temperature dependence on leakage current

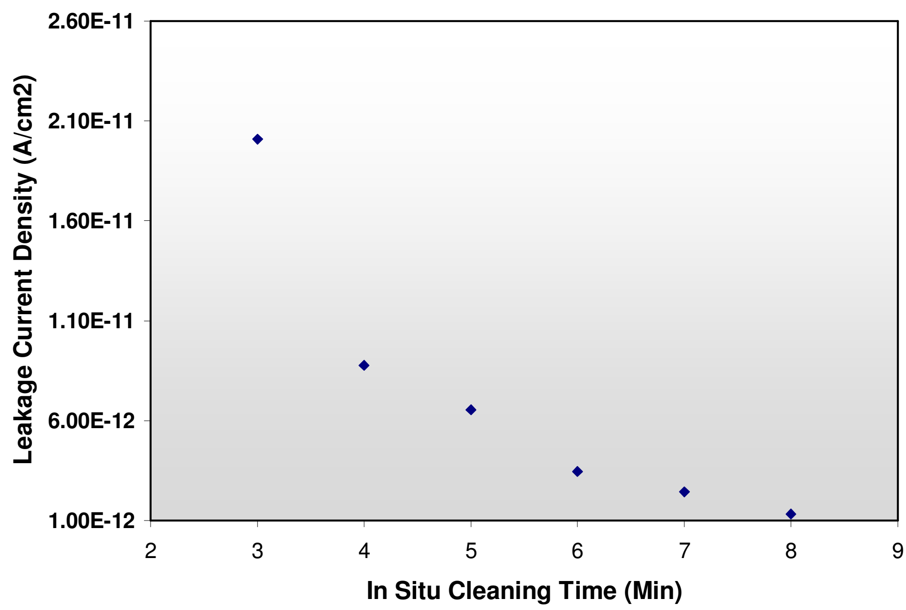


Figure 28 In-situ cleaning time dependence on leakage current

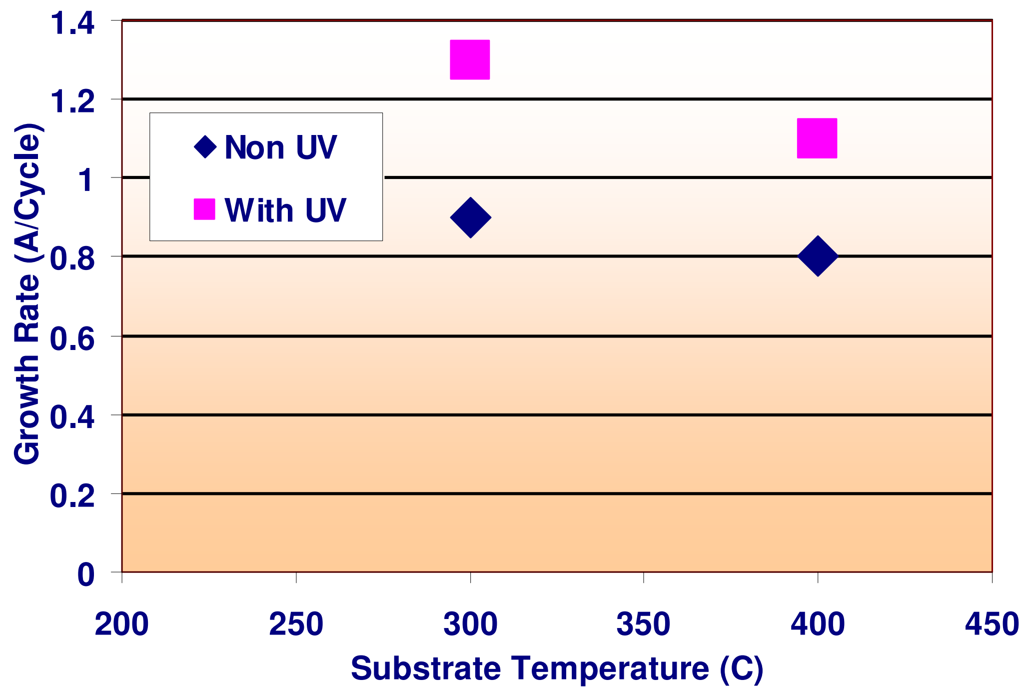


Figure 29 Dependence of UV on growth rate

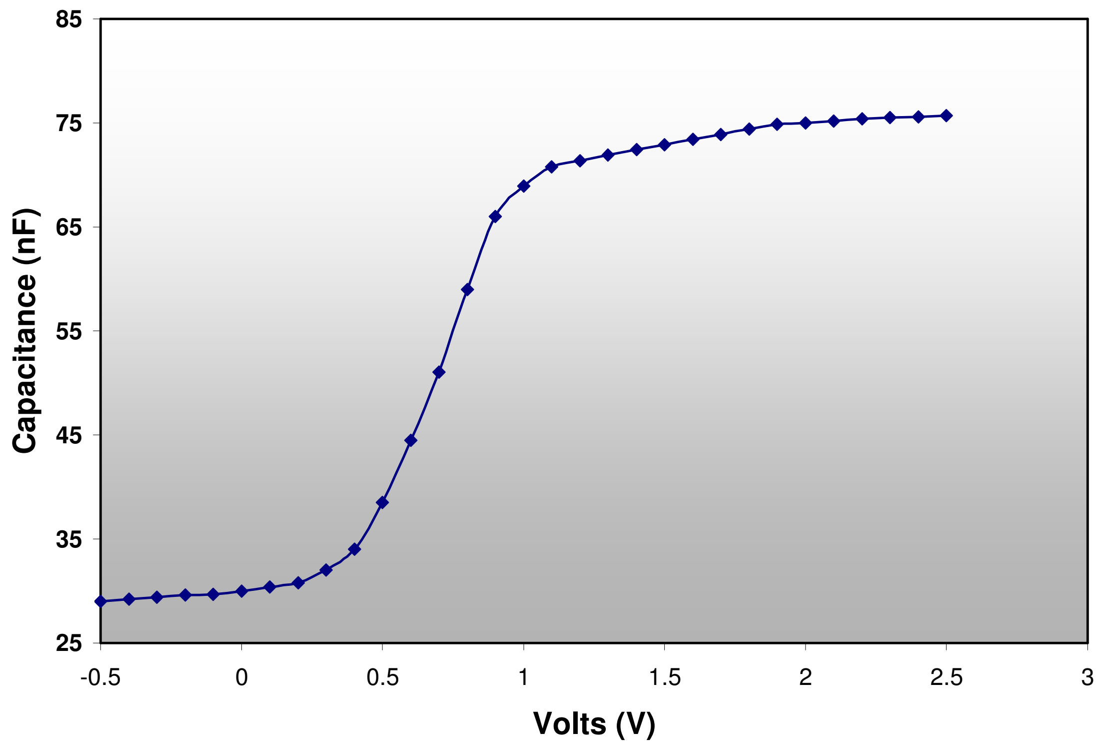


Figure 30 C-V measurements at 1 MHz

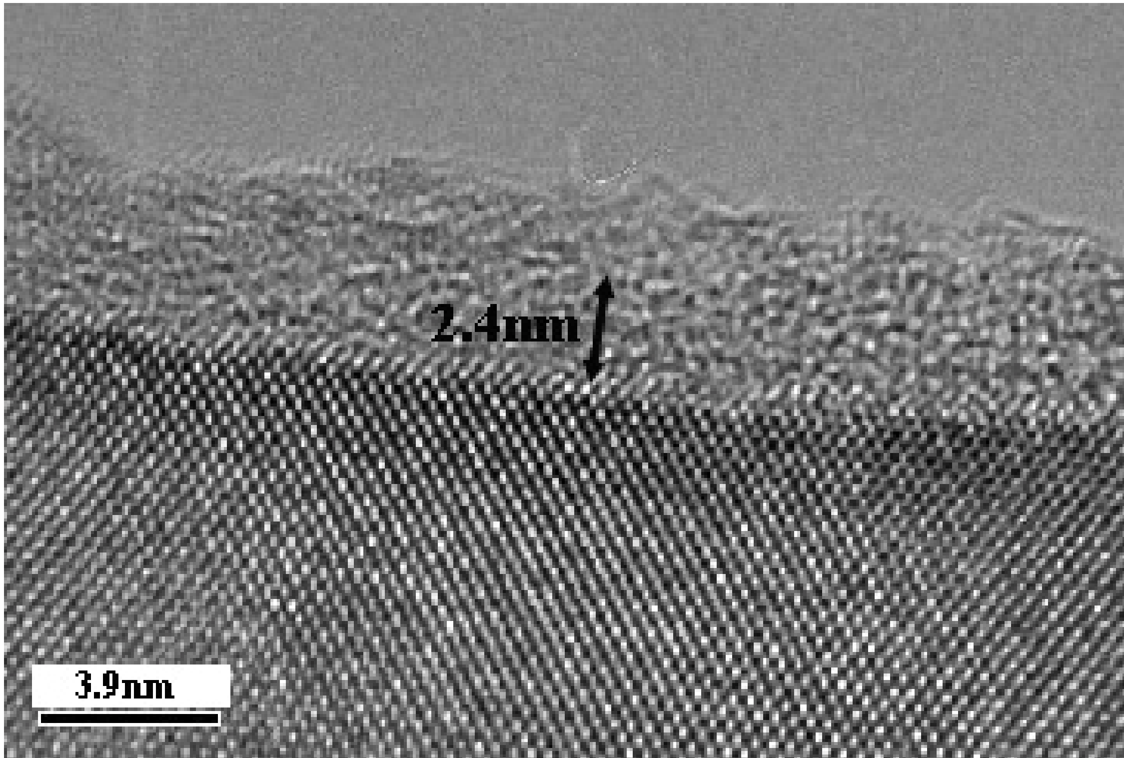


Figure 31 High-resolution cross-section TEM results in <110> direction of the HfO_2/ Si (001) specimen, showing the oxide and the interface

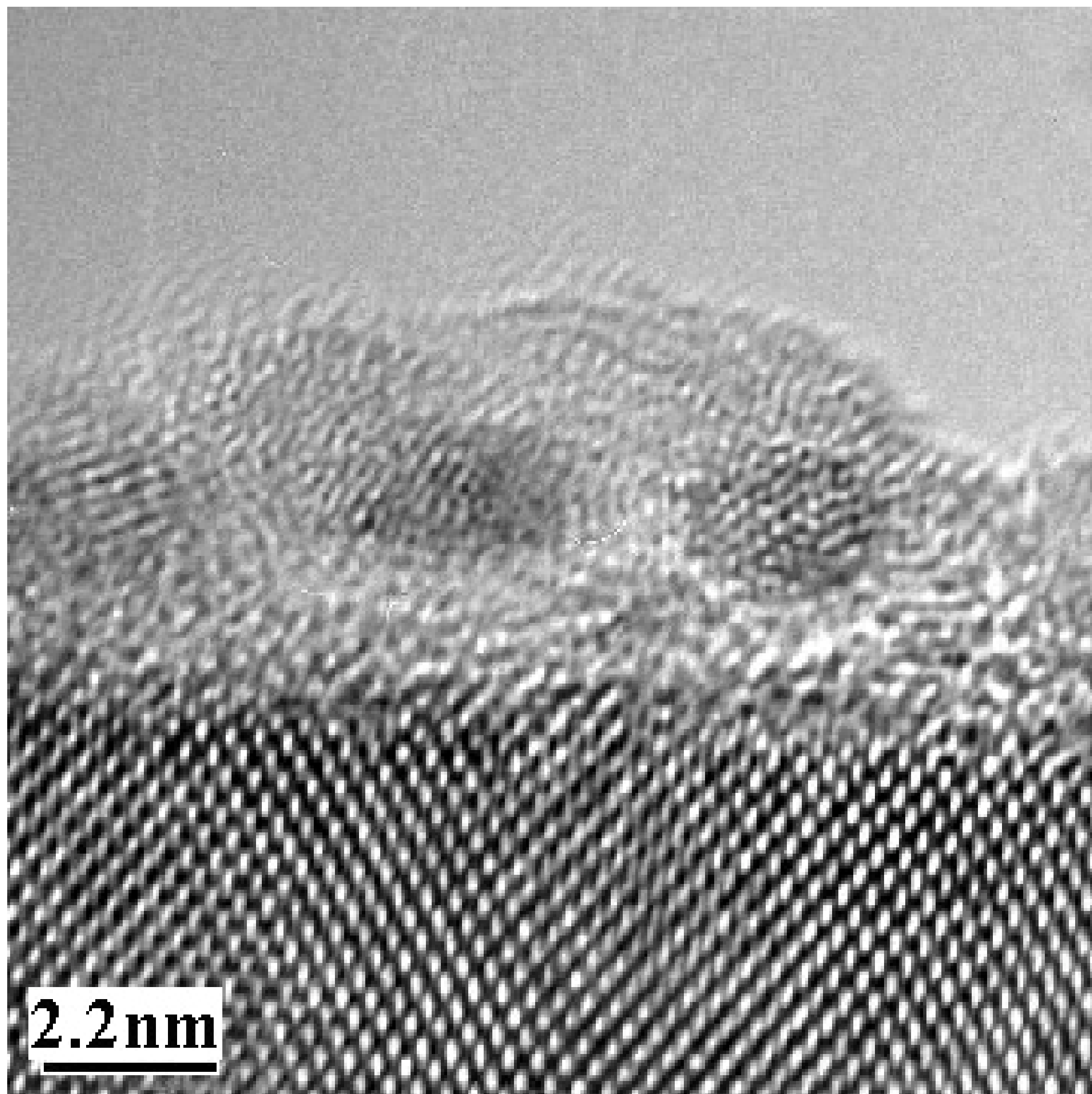


Figure 32 Atomic structure of oxide-silicon interface

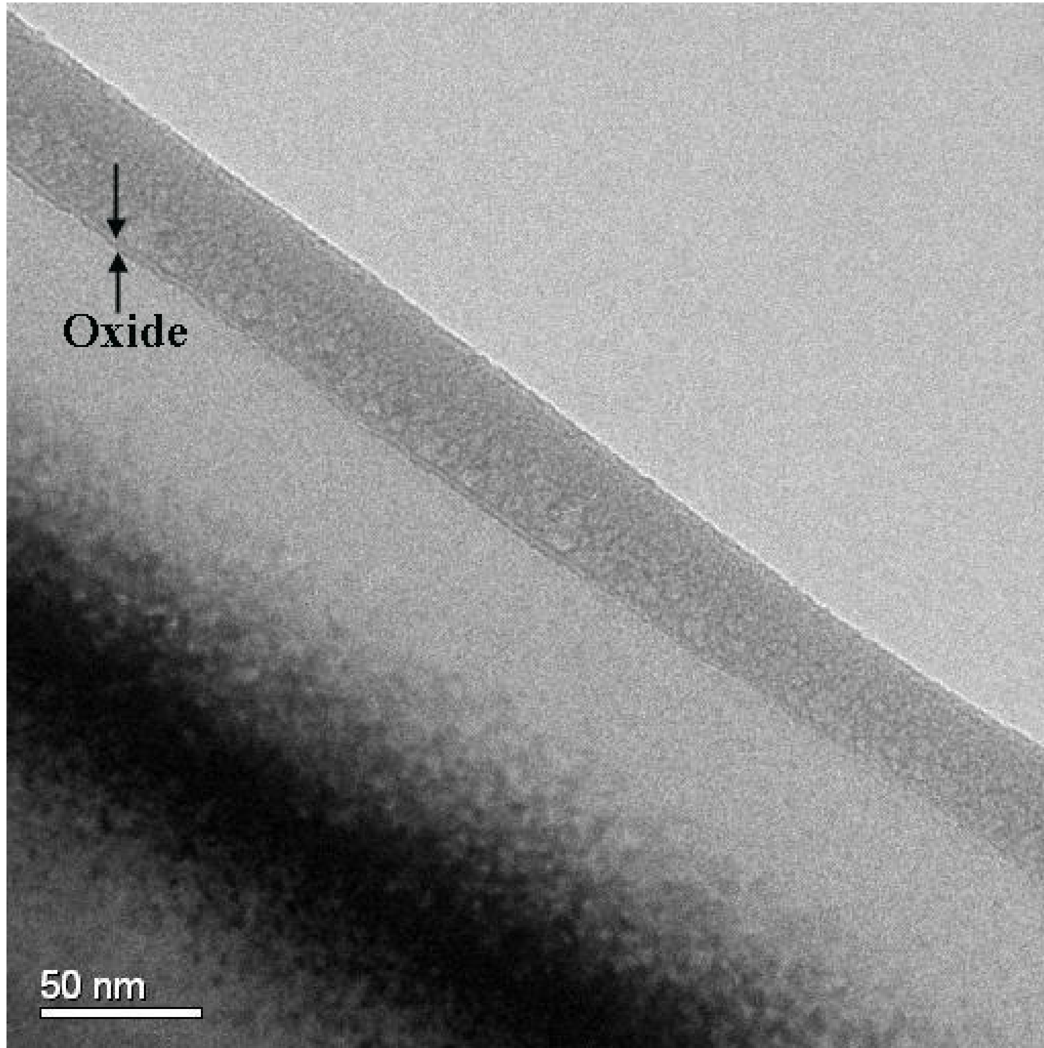
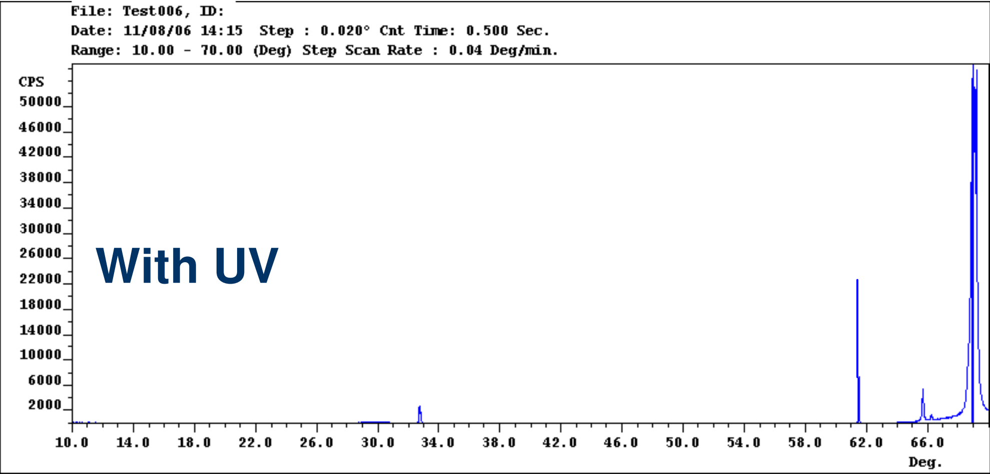


Figure 33 Cross-section transmission electron microscopy micrograph showing the presence of HfO2 layer



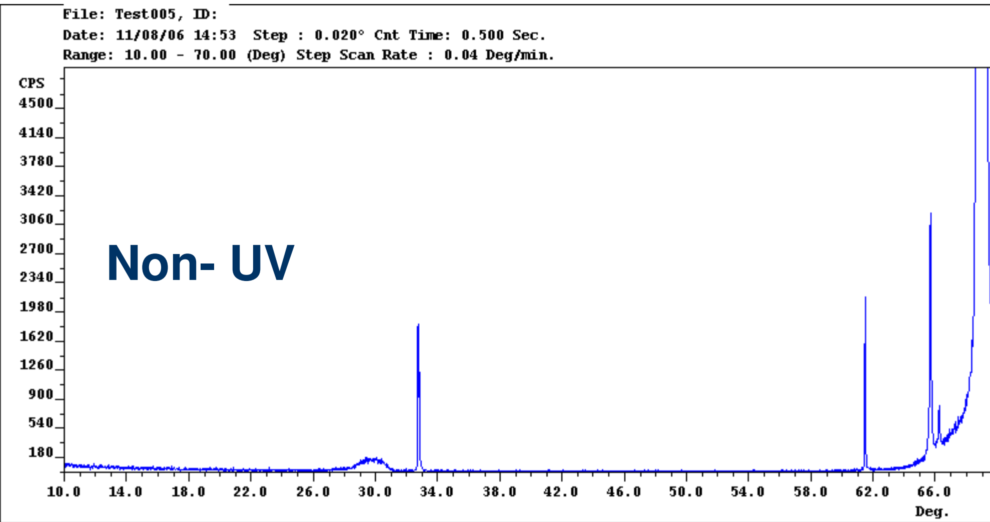


Figure 34 XRD measurements for UV and Non-UV samples

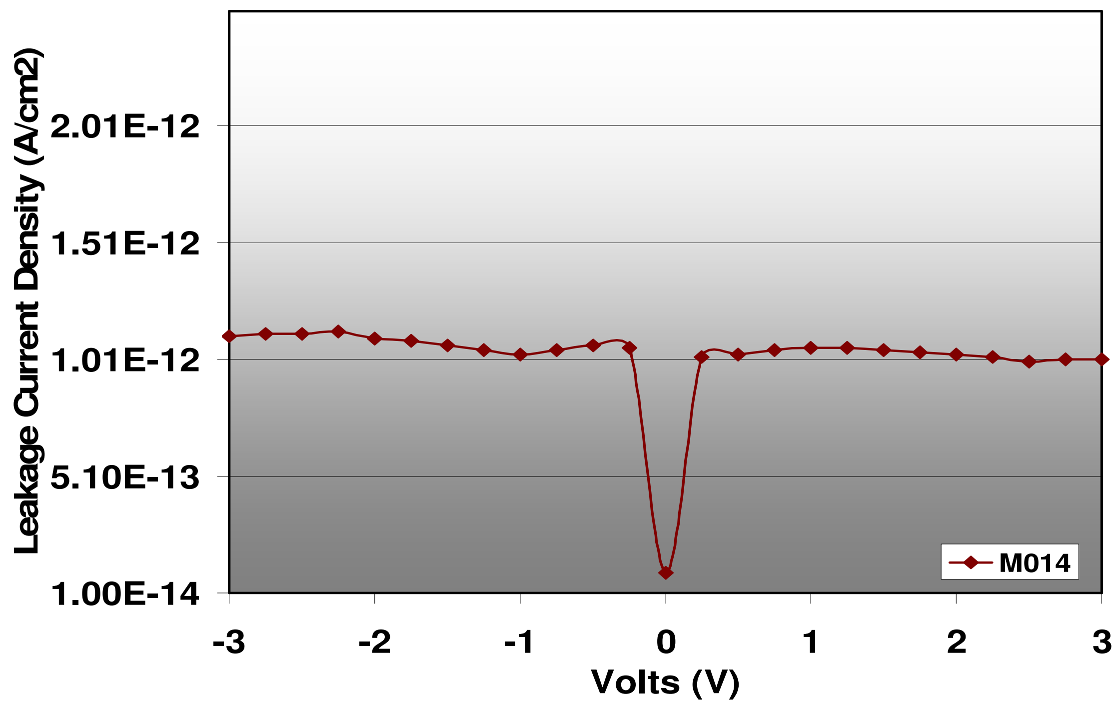


Figure 35 Leakage current density mean for optimized process recipe at various positive and negative gate voltage

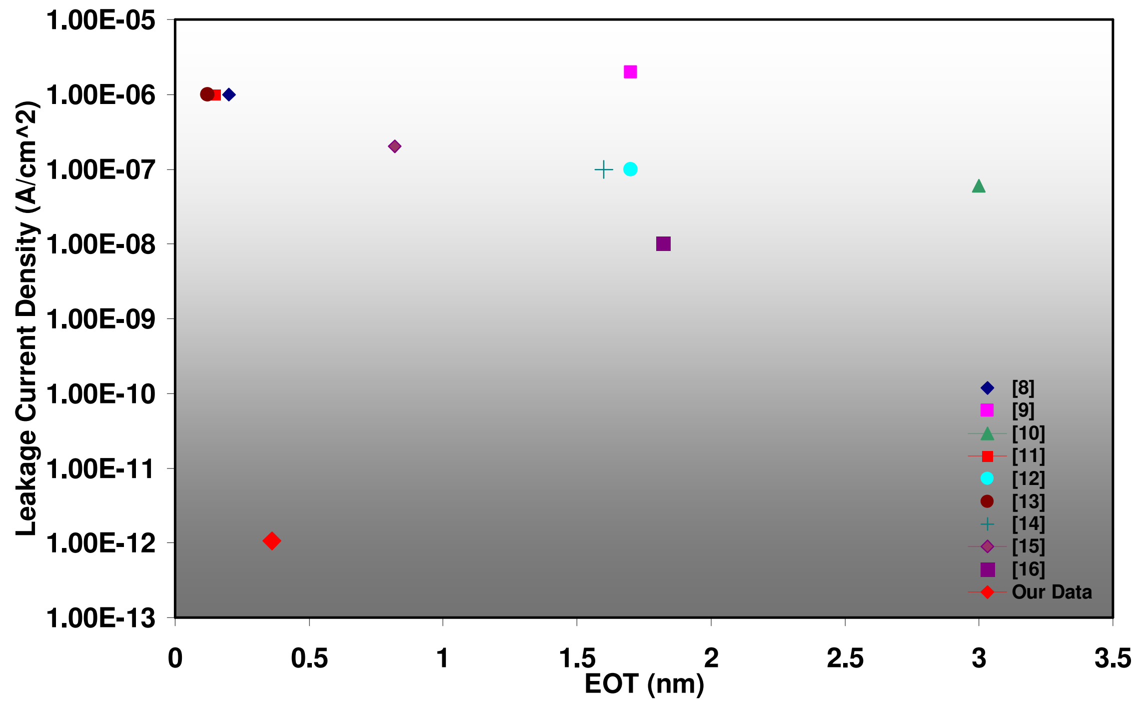


Figure 36 Comparison of published leakage current density data versus EOT

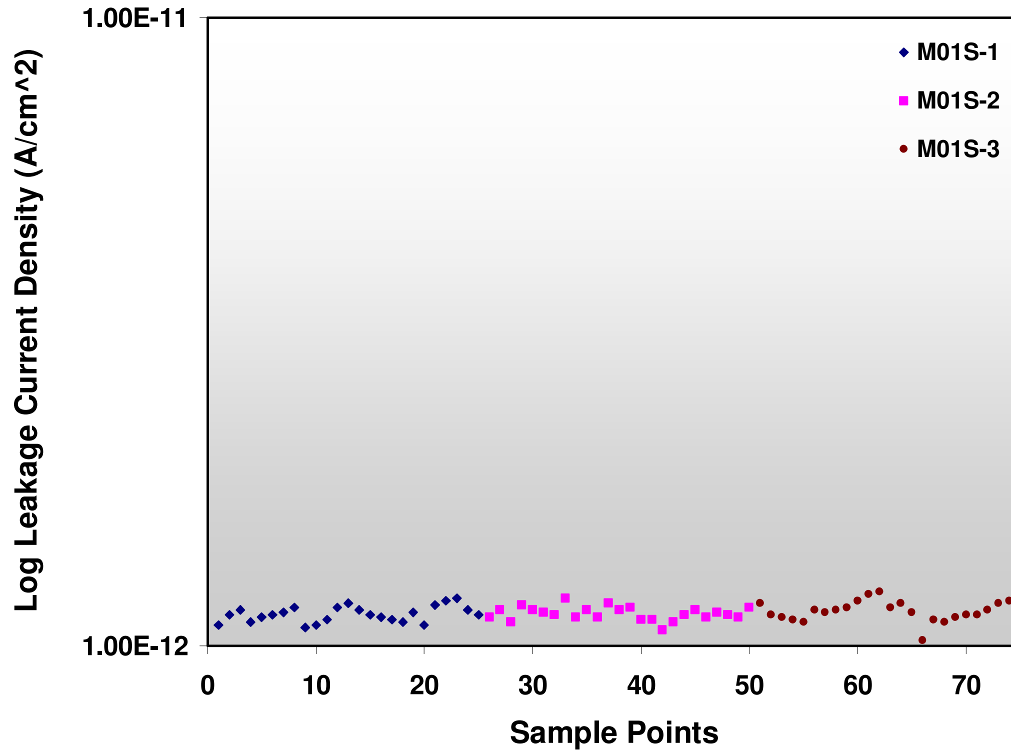


Figure 37 Repeatability of leakage current density for 3 samples

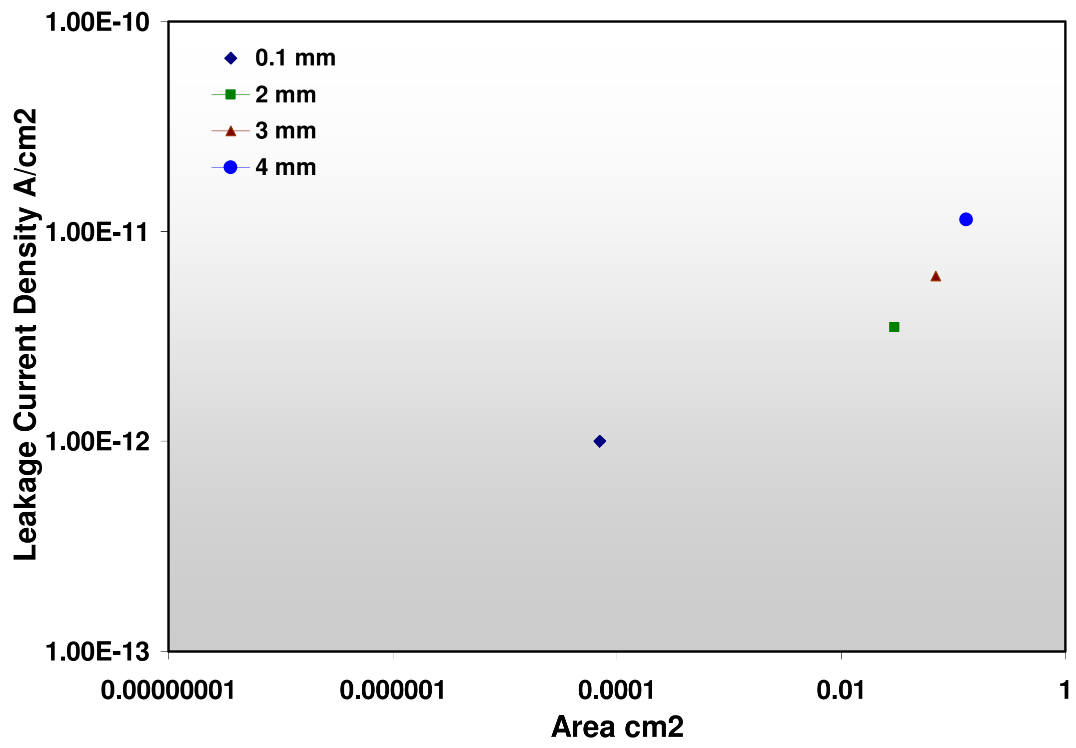


Figure 38 Area effect on leakage current density

CHAPTER 5

NEW PROCESS AND TOOL FOR METAL/HIGH-K GATE DIELECTRIC STACK

Introduction

There is a growing realization that no single semiconductor manufacturer can afford to develop next-generation technologies independently. With the growing cost of the fabs and process technologies, new EDA tools, co-development in design and packaging and low process variation are bottlenecks, designers and manufacturers have to contend with [1]. We have pointed out in an earlier publication [2] detailed analysis on key technical and business factors that hold the future of semiconductor industry. Design for manufacturing/design for yield (DFM/DFY) is a highly demanded necessity in order to ensure fast yield rampup and stable volume production. We have shown in a recent publication [3] that none of the proposed alternatives to Si CMOS can lead to manufacturing on a large scale and hence silicon CMOS will continue for many more years beyond the ITRS roadmap of 2020.

As gate oxides thicknesses scale down to a few atomic layers, process variation and design bottlenecks are dominant, with the gate leakage density posing as a serious challenge to further scaling [4]. Recently in January 2007, Intel Corporation announced that it will incorporate the use of high-k dielectrics for the 45nm technology node [5]. Off state leakage current related power dominates the CMOS heat dissipation problem making the necessity of reducing the gate leakage current density to zero, so that the designer will get relief to focus on other imposing challenges.

In this chapter we report the results of a new process and tool to deposit metal/high-k gate dielectric stack. We report the results of 0.39 nm effective oxide thickness (EOT) gate dielectric material with a leakage current density value of about 1 x 10^{-12} A/cm^2 for gate voltage from +3V to -3V. Statistical design of experiments was conducted to optimize process parameters of in-situ cleaning and annealing for lowest leakage current density. Since the process and the tool have inherently reduced process variation, there is a direct reduction in cost associated with process control resulting in more economical cost of production and better yield. With gate leakage current density so low, our process exploits the advantages of high-k dielectrics hence also easing the design bottle necks.

Our Manufacturing Mantra

Some of the key limitations on current processing tools besides from the high processing temperature is that the tools provide little or no control in reducing microscopic defects for sub-45 nm devices. Also, tools are unable to provide the required homogeneity of processed material. Current systems are also not suitable for providing in-situ cleaning and processing in the same chamber. Based on the fundamentals of RTP and the data presented in an earlier publication [7] it is obvious that furnaces, mini-furnaces, and resistive-heater-based RTP systems are inadequate to meet the process variation requirements of 45-nm technology nodes for 300-mm diameter wafers. Current lamp-based RTP tools can meet the process variation requirements at the 45-nm technology node for 300-mm diameter wafers. Based on the recent market data, more than 84% of current RTP tools are lamp based [8]. Thus the industry trend is towards the

lamp-based RTP systems. Beyond the 45-nm node, we have shown that the use of VUV photons as the source of optical energy in RTP and the use of in-situ thermal stress monitoring [9] can provide the desired process requirements of process uniformity and overall minimization and uniformity of thermal stress in the high-k dielectric. Currently, there are no 300-mm tools based on the use of UV photons in RTP systems in the market. It is also worth mentioning here that due to reduced cycle time, lamp-based RTP systems can free the yield-enhancement tools and an overall improvement in yield will be obtained [10]. Thus in the selection of manufacturing tools, one has to consider the impact of process variation on design and the yield of the semiconductor product. A more expensive lamp-based RTP tool may compensate excessive cost by providing higher yield and tighter process parameters.

Statistical Design Of Experiments

The Box-Behnken design is an independent quadratic design in that, it does not contain an embedded factorial or fractional factorial design [11, 12]. In this design the treatment combinations are at the midpoints of edges of the process space and at the center. These designs are rotatable (or near rotatable) and require 3 levels of each factor. The designs have limited capability for orthogonal blocking compared to the central composite designs. In a recent publication, the statistical design of experiment analysis is presented in detail [13, 14]

Figure 39 illustrates a 3 factor Box-Behnken design [12]. The geometry of this design suggests a sphere within the process space such that the surface of the sphere

protrudes through each face with the surface of the sphere tangential to the midpoint of each edge of the space

Table 4 contrasts the structures of four common quadratic designs one might use when investigating three factors. The table combines central composite circumscribed (CCC) and central composite inscribed (CCI) designs because they are structurally identical. For three factors, the Box-Behnken design offers some advantage in requiring a fewer number of runs. For 4 or more factors, this advantage disappears. The Box-Behnken design was chosen because of the fewer number of total runs needed compared to the other central composite type designs. The Box Behnken three factor designs with three levels for each was done in order to optimize the process parameters for in-situ cleaning and annealing.

In-Situ Cleaning DOE

In-Situ cleaning time, temperature and percentage of hydrogen were chosen as the 3 factors for the Box-Behnken design. Table 5 shows the three levels of optimization chosen The 15 experiments run are shown in Table 6. Table 7 shows the results for leakage current density for 8 points measured on each sample.

Figure 40 shows the contour plots for in-situ cleaning DOE. Figure 41 shows the surface response plot for the in-situ cleaning DOE. The response variable is mean leakage current density J in pA/cm^2. As can be seen from the figure the percentage of nitrous oxide played the most critical role in reducing leakage current density. Figure 42 shows the residual plot versus temperature, with leakage current density as the response factor. The statistical indicators and the various plots provided by the MINITAB program can be

used to assess the quality of the regression models and to compare between various models. This was done through residual plots, surface and contour analysis and cube plots. The residual plot shows the difference between the calculated and measured values of the dependent variable as function of the measured values. If the regression model represents the data correctly, the residuals should be randomly distributed around the line of err=0 with zero mean. As the residuals do not show a clear trend, this indicates that an appropriate model is being used in the analysis. Figure 43 shows the residual plot versus time, with leakage current density as the response factor.

The in-situ cleaning parameters of time, substrate temperature and % hydrogen were investigated in detail after the fitted model was obtained, to optimize the process parameters for lowest leakage current density. Figure 44 shows the surface and contour plots for leakage current density, with various temperatures and time. Figure 45 showing the contour plot for optimizing % hydrogen and time, clearly shows that as the % hydrogen and time increased, the leakage current density sharply reduced. Figure 46 showing the contour plot for optimizing % hydrogen and temperature shows that the lowest leakage was achieved for higher percentages of hydrogen and temperature greater than 900 ^{o}C. Therefore, from this set of design of experiments, the in-situ cleaning parameters were optimized at 950 ^{o}C for 10 minutes under 20% hydrogen ambient. Figure 47 shows the response for three levels of temperature for varying % hydrogen concentrations. 20% hydrogen was considered optimal case as increasing level of % hydrogen is not feasible in current system. Figure 48 clearly indicates that lowest leakage

is obtained at 20% hydrogen level. Figure 49 indicates lowest leakage is obtained at 15 minutes.

<u>Box Behnken design of experiments for annealing</u>

Three factors of annealing time, annealing temperature and % nitrous oxide were selected to optimize for the anneal process, shown in Table 8. Table 9 shows the 15 experiments for the design of experiments. Table 10 shows the results for leakage current density for 8 points measured on each sample. The statistical analysis was done using MINITAB software and the details are given below in Figures 50 -54. Figures 50 and 51 show the surface response plot for two different hold values of temperature. Figure 52 shows the contour plot for the annealing DOE with leakage current density as the response. Figure 53 shows the residual plot for % nitrous oxide with leakage current density as the response.

Using a 3-factor Box-Behnken design of experiments, the annealing parameters of time, temperature and ambient were investigated after fitting model to optimize process parameters for the lowest leakage current density. Figure 54 shows the surface and contour plots for optimizing the annealing time and temperature. As can be seen $< 1.0 \times 10^{-12}$ A/cm^2 was achieved for higher temperatures, with time not playing as critical a role. Figure 55 shows the surface and contour plots for optimizing anneal time and % nitrous oxide. Higher concentrations of nitrous oxide played a critical role in reducing the leakage current density. Figure 56 shows the surface and contour plots for optimizing % nitrous oxide and temperature. Again, as can be seen concentration of nitrous oxide played the more important role in reducing leakage current density. Therefore, the

annealing parameters were optimized at 900 ^{o}C for 10 minutes in a 100% nitrous oxide ambient. Figure 57 shows the leakage mean plotted versus the % nitrous oxide diluted with nitrogen. Hence the 0% nitrous oxide case represents 100% oxygen. 80% nitrous oxide gave us the lowest leakage. Figure 58 plots annealing time versus leakage mean and indicates that time is not a critical factor although it again reflects the nitrous oxide playing an extremely important role in reducing leakage current density. Figure 59 plots annealing temperature versus the leakage average showing us again that nitrous oxide plays critical role in lowering leakage current density.

Optimized Process Recipe

Once the statistical design of experiments was completed, an optimized process recipe was arrived at and it is shown in Table 11. As shown, the ex-situ clean was performed as three quick 5 second rinses in a diluted HF (1-2%) dip and a 200 second rinse in DI water. Once loaded into the chamber the in-situ clean was performed for 15 minutes at 950 ^{o}C under a 20% hydrogen ambient with rest 80% diluted with nitrogen. The deposition was performed at 250 ^{o}C substrate temperature, with precursor and water pulse times 1 second and purge times 5 seconds. The settling time between each pulse in a cycle was 0.3 seconds. 65 deposition cycles yielded a 2.1 nm thickness film which was measured by Ellipsometer and later verified through TEM measurements. The annealing was done for 7.5 minutes at 900 ^{o}C at a 100% nitrous oxide ambient.

Process Variation Analysis

Variations due to process have to be taken seriously by the semiconductor industry and tighter design rules have been implemented to keep process variation issues at bay from

the critical manufacturing issues [11]. But, as the critical dimensions (CD) are moving towards a few nanometers, process control at the atomic level is becoming a significant issue. As future circuits will be capable of handling fewer process variations, both designers and process engineers have to coordinate in such a way that the process is optimized for the design or vice versa. Otherwise, yield will be affected and the profit will decline. This situation can be eased by developing a process that has the inherent property of introducing fewer defects during processing. In order to reduce the number of design iterations and design cycle time, process variation should be controlled as early in the CMOS process flow as possible.

To illustrate the advantages of using UV during the steps of in-situ cleaning, deposition and annealing, several experiments were conducted with and without UV for all steps, then with UV for each step. Hypothesis test using the F Statistic was conducted to determine whether or not the variances for the mean leakage current values differed between process categories 1, 2 and 3. It was observed that the mean leakage currents and mean capacitances were significantly different for all three processing categories. The process variation results are illustrated in Figure 60 and Figure 61. Figure 62 shows the leakage current density means for samples run after the statistical optimization was done.

Conclusion

In this chapter we report the results of a new process and tool to deposit metal/high-k gate dielectric stack. We report the results of 0.39 nm effective oxide thickness (EOT) gate dielectric material with a leakage current density value of about 1 x 10^{-12} A/cm^2 for gate voltage from +3V to -3V. Statistical optimization of the process parameters has been

done to achieve lowest leakage current density and maximum capacitance. The availability of such a tool for manufacturing with gate leakage current equal to zero will simplify the design complexity and will reduce design for manufacturing cost of the next generations of CMOS advanced products. Our process and tool has the capability of providing for tighter control over process variation at the front end of the CMOS process and therefore has the potential to increase throughput and yield while lowering overall manufacturing costs due to yield loss.

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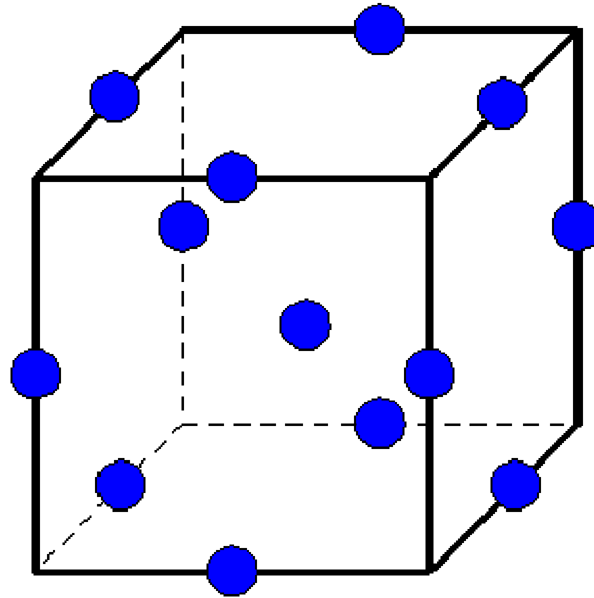


Figure 39 Illustration of a 3-factor Box Behnken design [11]

Table 4 Comparison of three factor designs

CCC (CCI)				CCF				Box-Behnken			
Rep	***X*1**	***X*2**	***X*3**	**Rep**	***X*1**	***X*2**	***X*3**	**Rep**	***X*1**	***X*2**	***X*3**
1	-1	-1	-1	1	-1	-1	-1	1	-1	-1	0
1	+1	-1	-1	1	+1	-1	-1	1	+1	-1	0
1	-1	+1	-1	1	-1	+1	-1	1	-1	+1	0
1	+1	+1	-1	1	+1	+1	-1	1	+1	+1	0
1	-1	-1	+1	1	-1	-1	+1	1	-1	0	-1
1	+1	-1	+1	1	+1	-1	+1	1	+1	0	-1
1	-1	+1	+1	1	-1	+1	+1	1	-1	0	+1
1	+1	+1	+1	1	+1	+1	+1	1	+1	0	+1
1	-1.682	0	0	1	-1	0	0	1	0	-1	-1
1	1.682	0	0	1	+1	0	0	1	0	+1	-1
1	0	-1.682	0	1	0	-1	0	1	0	-1	+1
1	0	1.682	0	1	0	+1	0	1	0	+1	+1
1	0	0	-1.682	1	0	0	-1	3	0	0	0
1	0	0	1.682	1	0	0	+1				
6	0	0	0	6	0	0	0				
Total Runs = 20				**Total Runs = 20**				**Total Runs = 15**			

Table 5 Box-Behnken in-situ cleaning DOE

	-1	0	1	
Temperature	800	900	1000	X1
Time	5 min	10 min	15 min	X2
% Hydrogen	10%	15%	20%	X3

Table 6 Experimental runs for in-situ cleaning DOE

Temp	Time	% Hyd	X1	X2	X3
800C	5 min	15%	-1	-1	0
800C	15 min	15%	-1	1	0
1000C	5 min	15%	1	-1	0
1000C	15 min	15%	1	1	0
800C	10 min	10%	-1	0	-1
800C	10 min	20%	-1	0	1
1000C	10 min	10%	1	0	-1
1000C	10 min	20%	1	0	1
900C	5 min	10%	0	-1	-1
900C	5 min	20%	0	-1	1
900C	15 min	10%	0	1	-1
900C	15 min	20%	0	1	1
900C	10 min	15%	0	0	0
900C	10 min	15%	0	0	0
900C	10 min	15%	0	0	0

Table 7 Results for leakage current density for 8 points on each sample

Time	Temp	% Hyd	Sample #	1	2	3	4	5	6	7	8
800C	5 min	15%	MB1	1.99E-12	2.01E-12	2.12E-12	2.13E-12	2.08E-12	2.05E-12	2.06E-12	2.15E-12
800C	15 min	15%	MB2	1.89E-12	1.83E-12	1.79E-12	1.81E-12	1.85E-12	1.86E-12	1.84E-12	1.82E-12
1000C	5 min	15%	MB3	1.58E-12	1.56E-12	1.55E-12	1.57E-12	1.55E-12	1.54E-12	1.56E-12	1.52E-12
1000C	15 min	15%	MB4	1.26E-12	1.29E-12	1.27E-12	1.28E-12	1.25E-12	1.22E-12	1.24E-12	1.24E-12
800C	10 min	10%	MB5	2.31E-12	2.32E-12	2.35E-12	2.37E-12	2.36E-12	2.35E-12	2.33E-12	2.30E-12
800C	10 min	20%	MB6	2.26E-12	2.27E-12	2.25E-12	2.23E-12	2.22E-12	2.25E-12	2.26E-12	2.25E-12
1000C	10 min	10%	MB7	1.31E-12	1.35E-12	1.32E-12	1.30E-12	1.36E-12	1.34E-12	1.35E-12	1.33E-12
1000C	10 min	20%	MB8	1.06E+12	1.05E-12	1.03E-12	1.01E-12	1.08E-12	1.09E-12	1.04E-12	1.02E-12
900C	5 min	10%	MB9	1.57E-12	1.55E-12	1.53E-12	1.57E-12	1.59E-12	1.51E-12	1.53E-12	1.54E-12
900C	5 min	20%	MB10	1.10E-12	1.11E-12	1.14E-12	1.12E-12	1.13E-12	1.14E-12	1.15E-12	1.19E-12
900C	15 min	10%	MB11	1.41E-12	1.46E-12	1.52E-12	1.55E-12	1.47E-12	1.49E-12	1.52E-12	1.53E-12
900C	10 min	20%	MB12	9.93E-13	9.95E-13	1.01E-12	1.02E-12	1.03E-12	1.01E-12	1.03E-12	1.01E-12
900C	10 min	15%	MB13	1.32E-12	1.35E-12	1.37E-12	1.39E-12	1.37E-12	1.38E-12	1.33E-12	1.36E-12
900C	10 min	15%	MB14	1.35E-12	1.36E-12	1.35E-12	1.38E-12	1.33E-12	1.31E-12	1.32E-12	1.32E-12
900C	10 min	15%	MB15	1.40E-12	1.30E-12	1.31E-12	1.32E-12	1.35E-12	1.38E-12	1.37E-12	1.33E-12

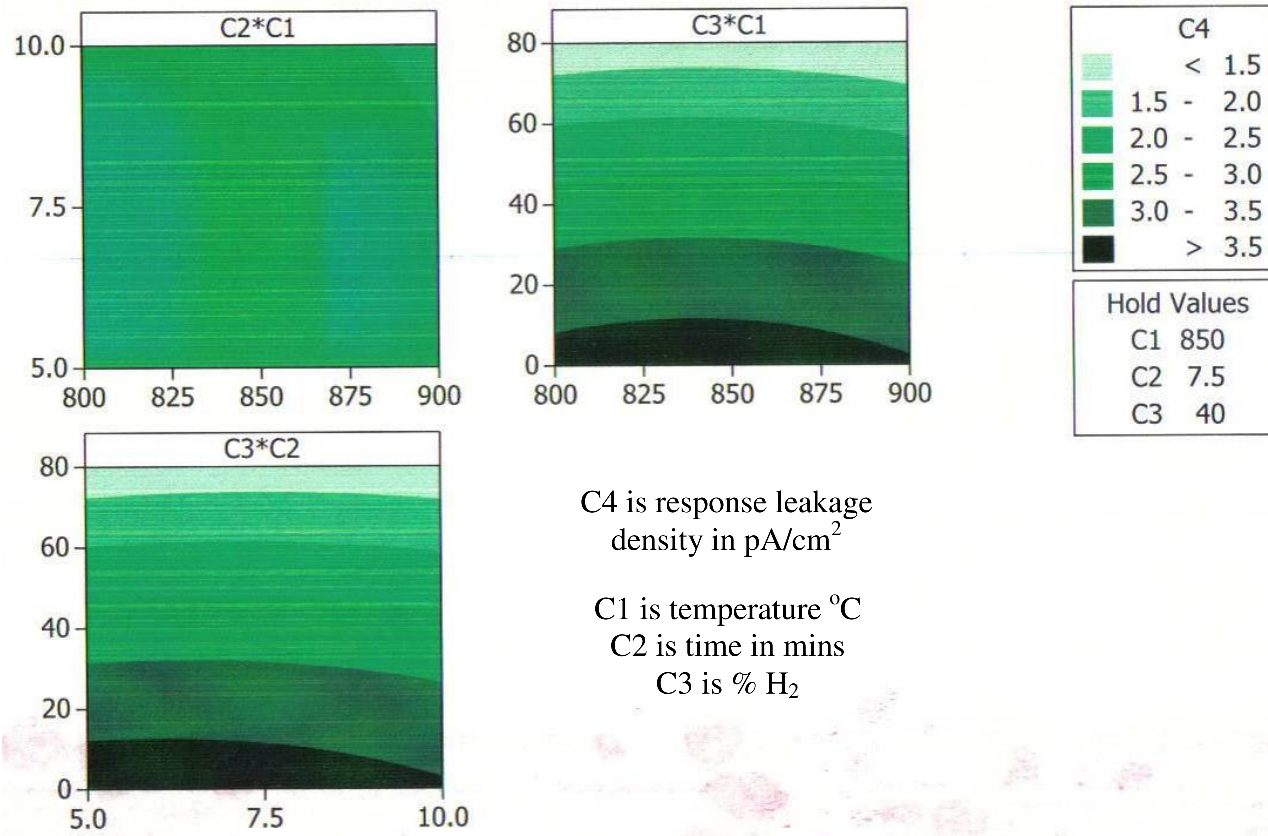


Figure 40 Contour plot for in-situ cleaning DOE

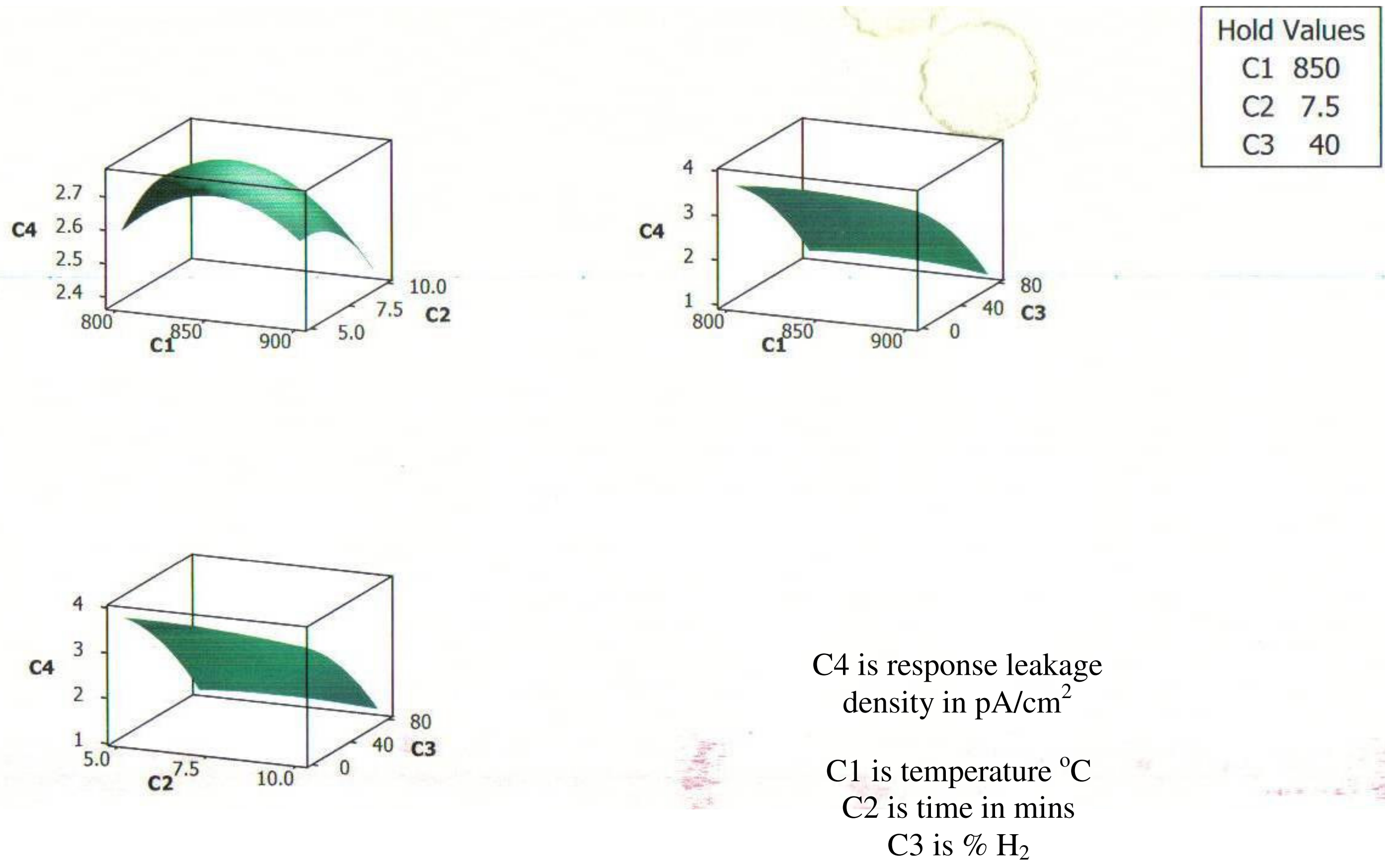


Figure 41 Surface plots for in-situ cleaning

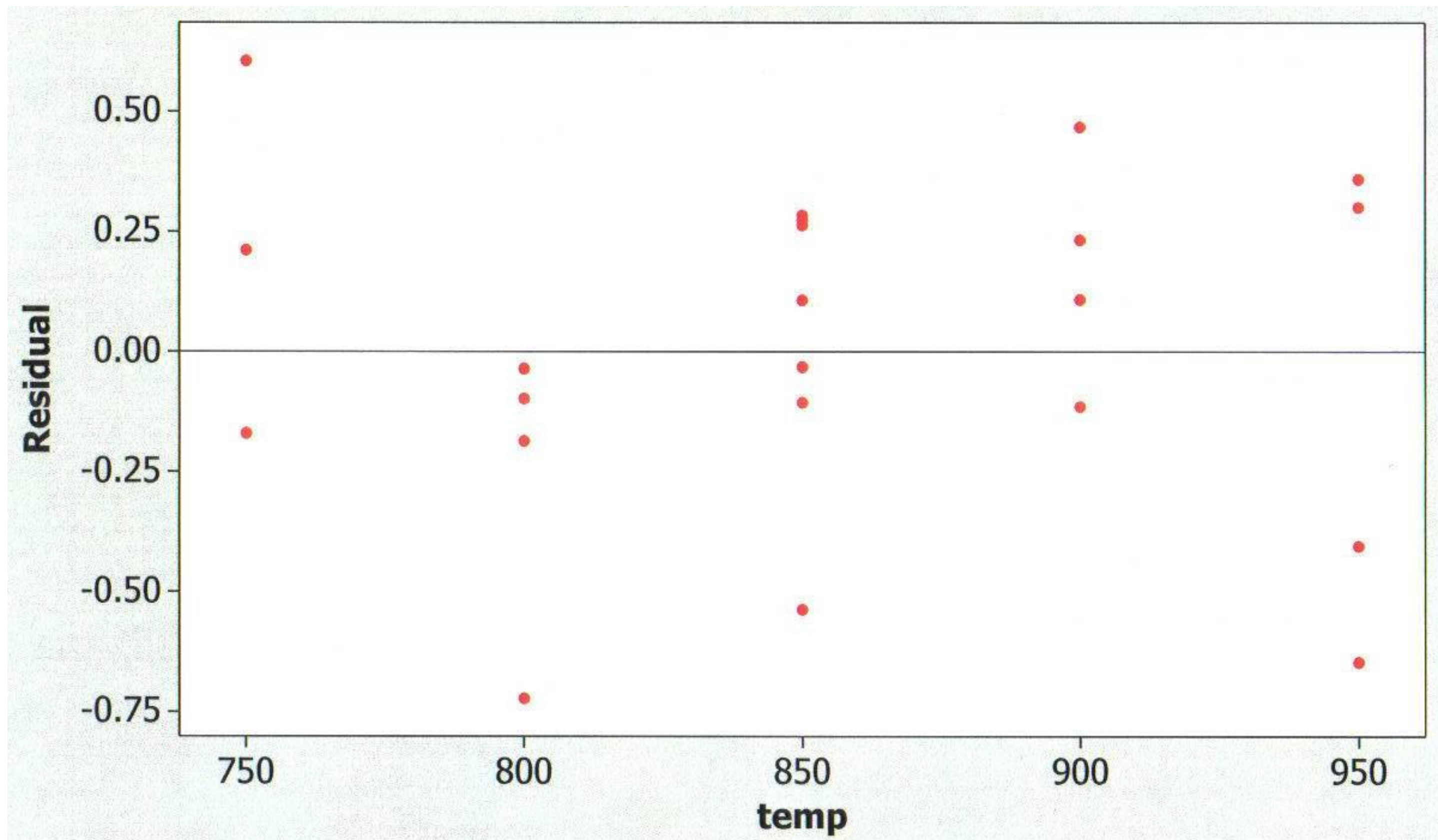


Figure 42 Residual plot for temperature

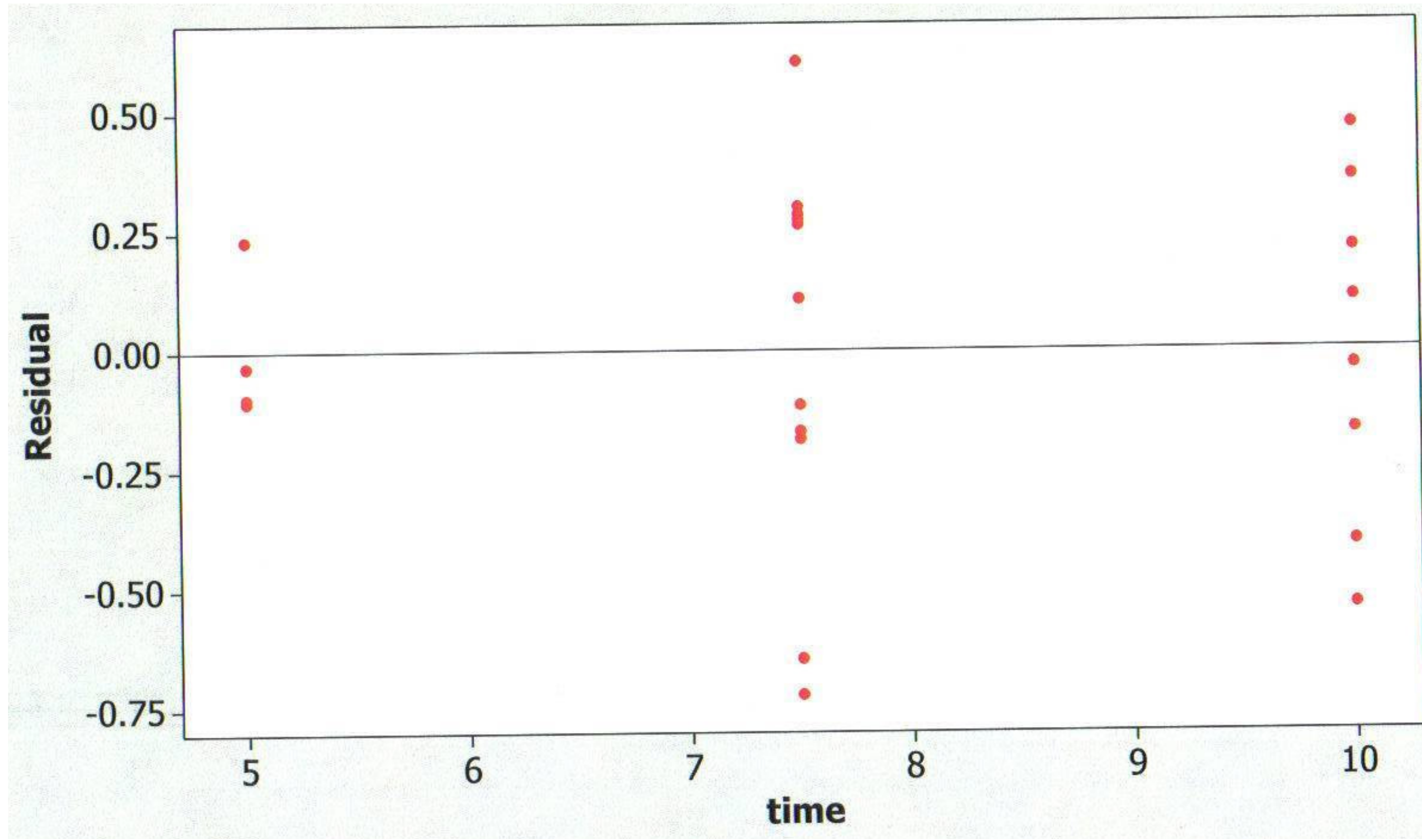


Figure 43 Residual plot for time

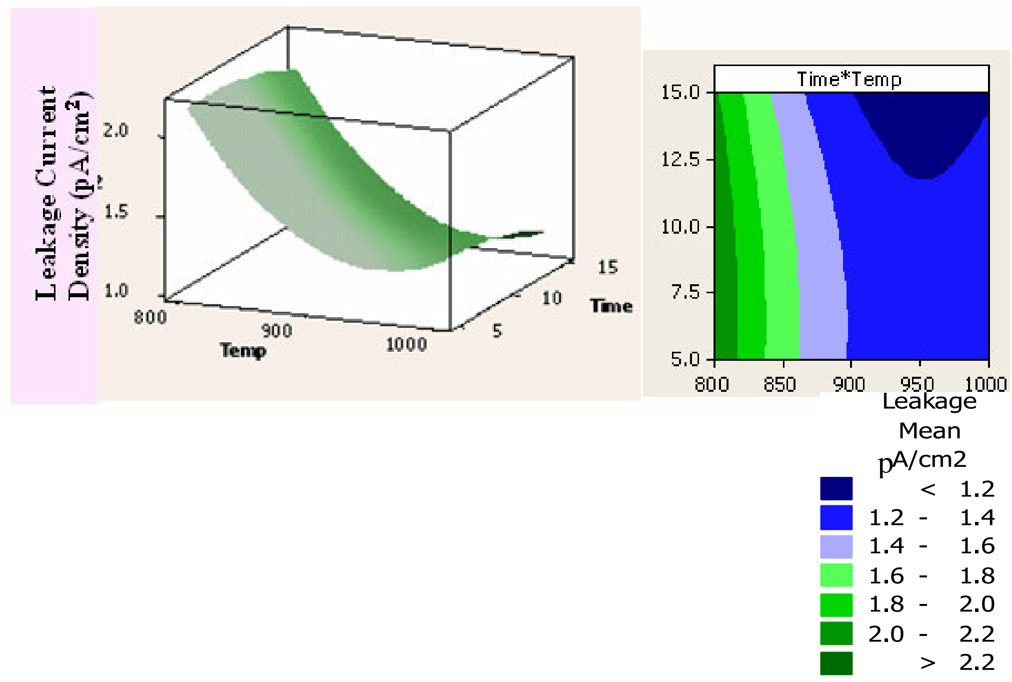


Figure 44 Response surface and contour plots for optimization of in-situ cleaning time and temperature

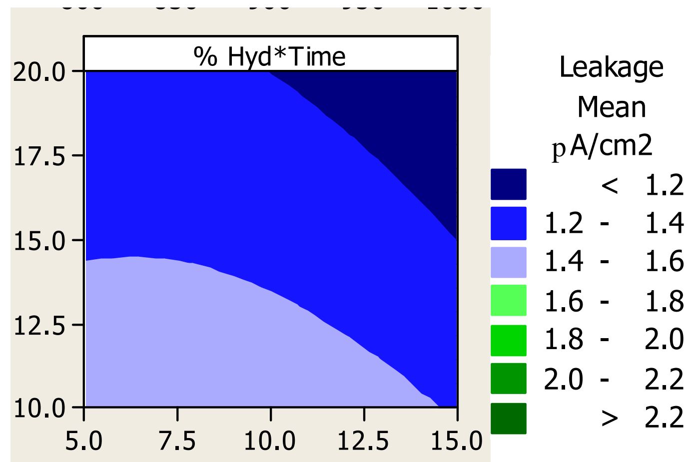


Figure 45 Contour plots for optimizing in-situ time and hydrogen concentration

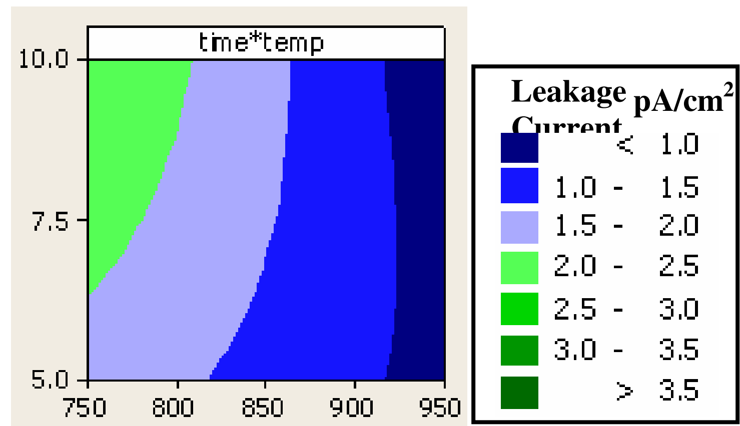


Figure 46 Contour plots for optimizing in-situ temperature and hydrogen concentration

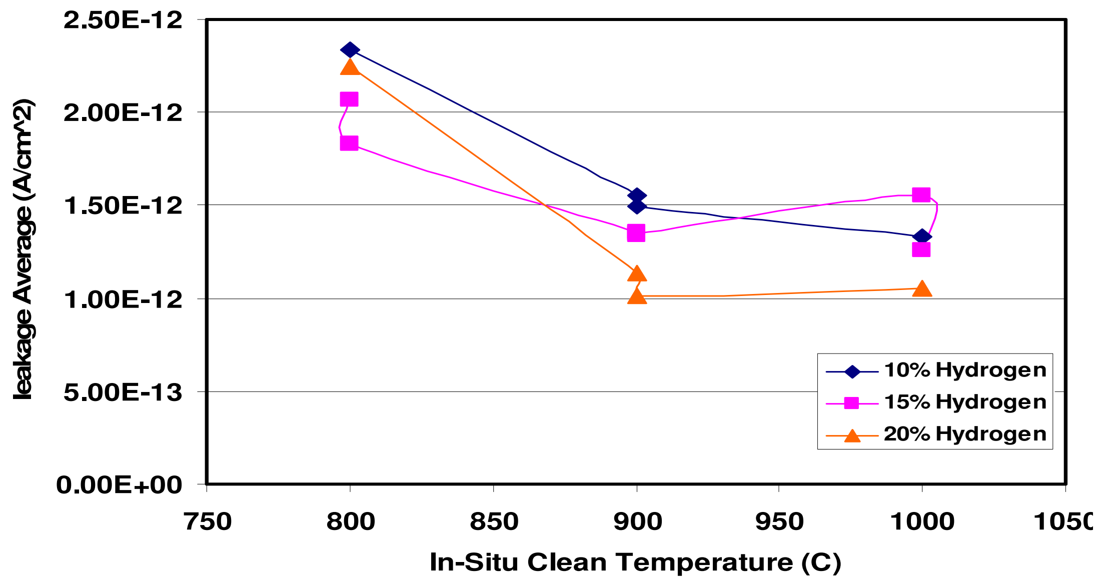


Figure 47 Leakage average vs. in-situ clean temperature

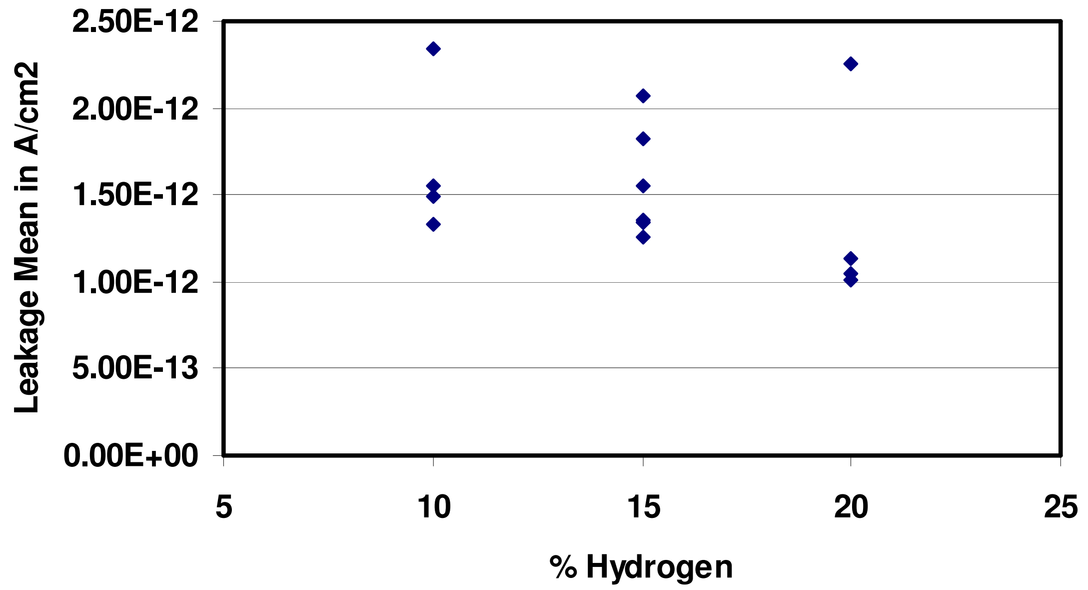


Figure 48 In-situ cleaning leakage mean vs. % hydrogen

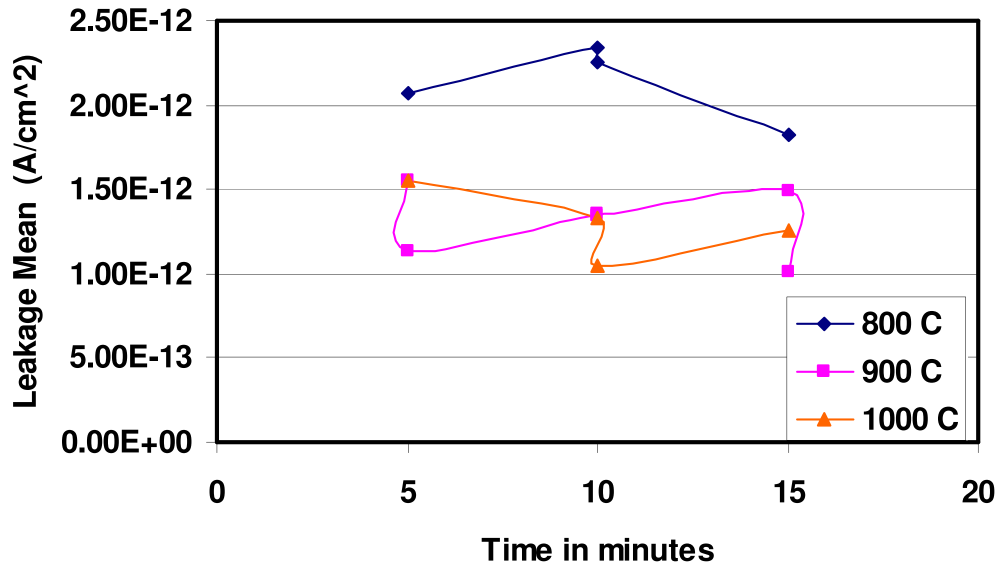


Figure 49 In situ cleaning leakage density vs. time in minutes

Table 8 Box Behnken annealing DOE with 3 levels chosen

Annealing	**-1**	**0**	**1**	
Time	800C	850C	900C	X1
Temperature	5 min	7.5 min	10 min	X2
% Nitrous Oxide	0%	40%	80%	X3

Table 9 Experimental runs for Box Behnken annealing DOE

X1	X2	X3	Time	Temp	% NO
-1	-1	0	800C	5 min	40%
-1	1	0	800C	10 min	40%
1	-1	0	900C	5 min	40%
1	1	0	900C	10 min	40%
-1	0	-1	800C	7.5 min	0%
-1	0	1	800C	7.5 min	80%
1	0	-1	900C	7.5 min	0%
1	0	1	900C	7.5 min	80%
0	-1	-1	850C	5 min	0%
0	-1	1	850C	5 min	80%
0	1	-1	850C	10 min	0%
0	1	1	850C	10 min	80%
0	0	0	850C	7.5 min	40%
0	0	0	850C	7.5 min	40%
0	0	0	850C	7.5 min	40%

Table 10 Box Behnken annealing DOE with 8 points measured on each sample

Time	Temp	% NO	1	2	3	4	5	6%	7	8
800C	5 min	40%	2.84E-12	2.81E-14	2.92E-12	2.94E-12	2.97E-12	2.83E-12	2.88E-12	2.85E-12
800C	10 min	40%	2.66E-12	2.68E-12	2.71E-12	2.74E-12	2.77E-12	2.73E-12	2.75E-12	2.67E-12
900C	5 min	40%	2.51E-12	2.52E-12	2.51E-12	2.53E-12	2.55E-12	2.57E-12	2.53E-12	2.56E-12
900C	10 min	40%	2.44E-12	2.41E-12	2.43E-12	2.48E-12	2.47E-12	2.46E-12	2.43E-12	2.44E-12
800C	7.5 min	0%	3.67E-12	3.69E-12	3.64E-12	3.62E-12	3.66E-12	3.69E-12	3.62E-12	3.59E-12
800C	7.5 min	80%	1.12E-12	1.17E-12	1.18E-12	1.13E-12	1.15E-12	1.16E-12	1.14E-12	1.16E-12
900C	7.5 min	0%	3.59E-12	3.58E-12	3.54E-12	3.52E-12	3.55E-12	3.57E-12	3.53E-12	3.58E-12
900C	7.5 min	80%	1.09E-12	1.08E-12	1.02E-12	1.01E-12	1.08E-12	1.05E-12	1.07E-12	1.06E-12
850C	5 min	0%	3.89E-12	3.84E-12	3.81E-12	3.77E-12	3.82E-12	3.71E-12	3.81E-12	3.88E-12
850C	5 min	80%	1.22E-12	1.25E-12	1.27E-12	1.24E-12	1.23E-12	1.21E-12	1.22E-12	1.27E-12
850C	10 min	0%	3.49E-12	3.45E-12	3.47E-12	3.44E-12	3.41E-12	3.48E-12	3.51E-12	3.52E-12
850C	10 min	80%	1.11E-12	1.09E-12	1.08E-12	1.06E-12	1.08E-12	1.12E-12	1.13E-12	1.07E-12
850C	7.5 min	40%	2.74E-12	2.75E-12	2.77E-12	2.78E-12	2.79E-12	2.71E-12	2.76E-12	2.77E-12
850C	7.5 min	40%	2.78E-12	2.75E-12	2.74E-12	2.71E-12	2.74E-12	2.76E-12	2.71E-12	2.72E-12
850C	7.5 min	40%	2.76E-12	2.74E-12	2.76E-12	2.73E-12	2.75E-12	2.78E-12	2.74E-12	2.76E-12

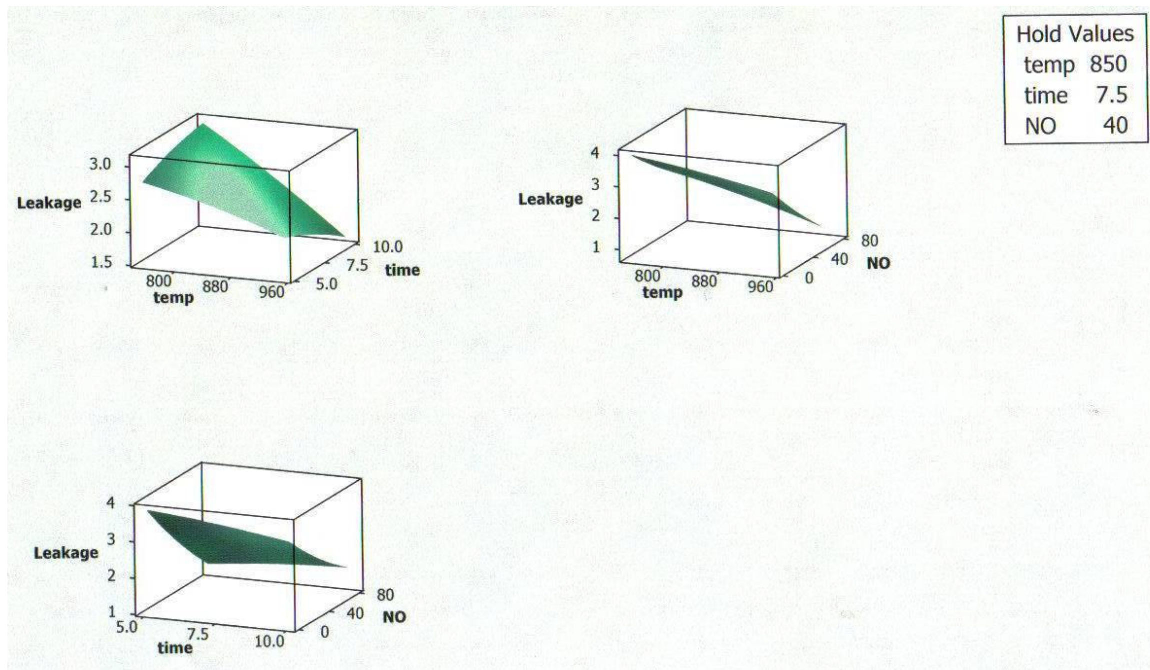


Figure 50 Surface response plot for annealing DOE

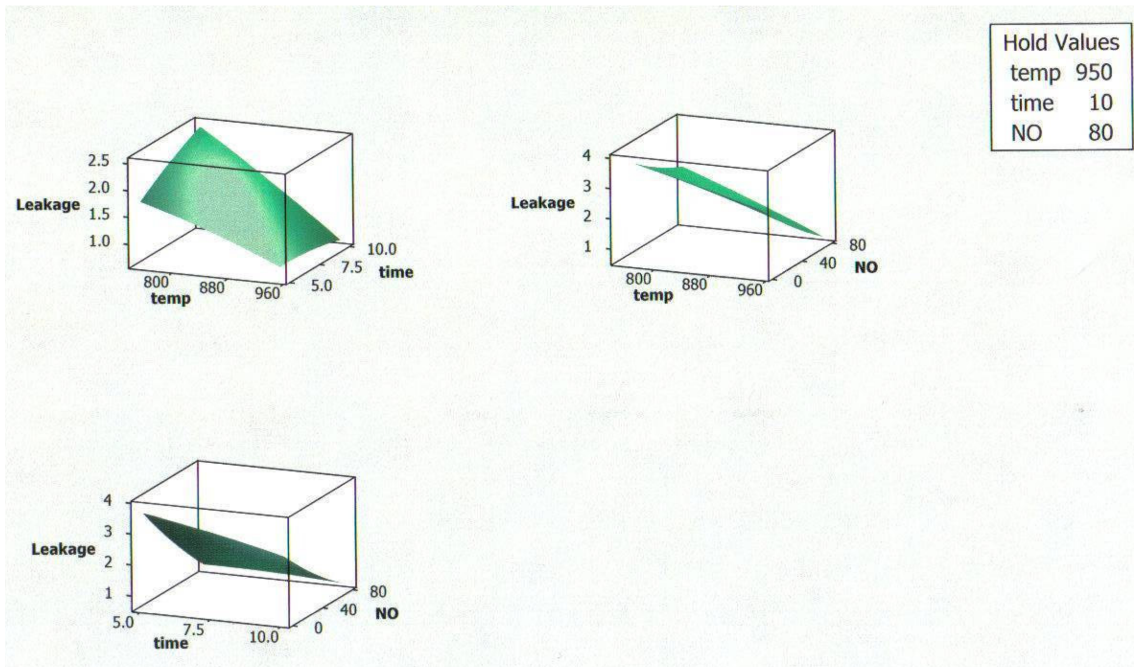


Figure 51 Surface response plot for annealing DOE with different hold values

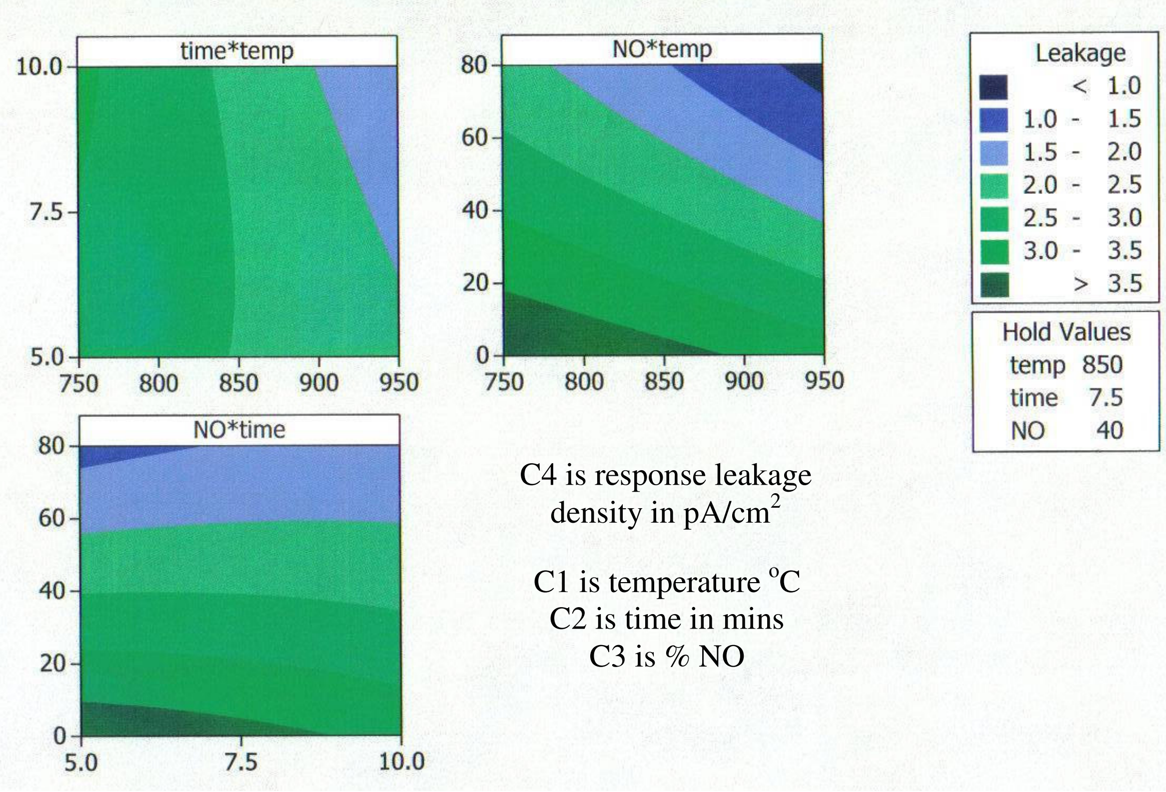


Figure 52 Contour plot for leakage current density for annealing DOE

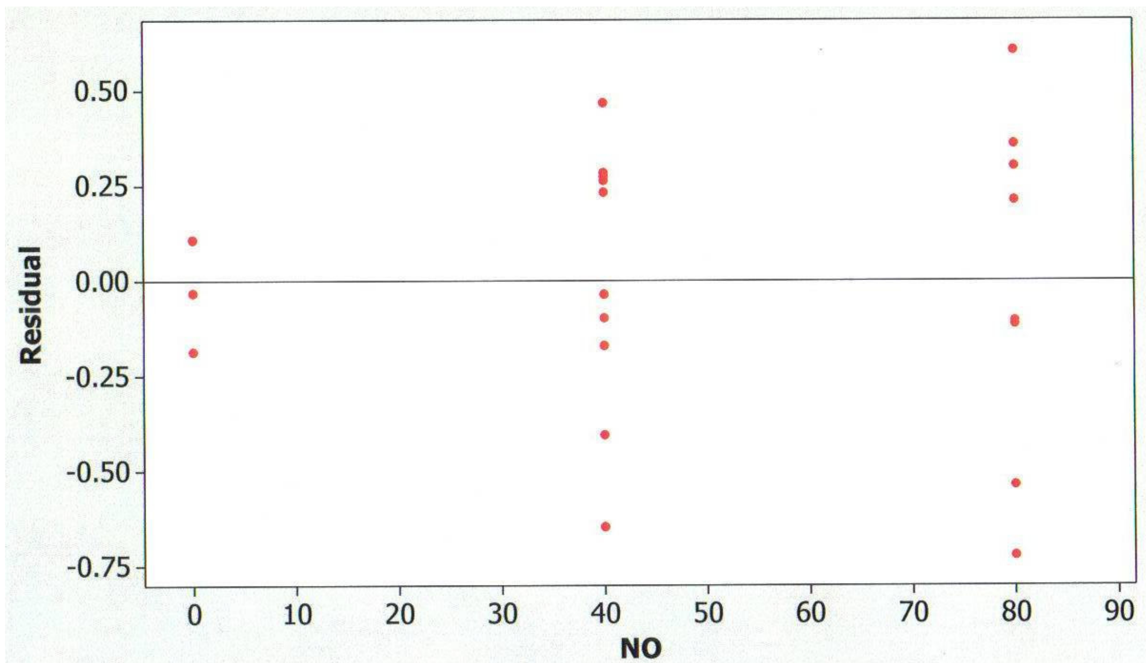


Figure 53 Residual plot for leakage versus % nitrous oxide

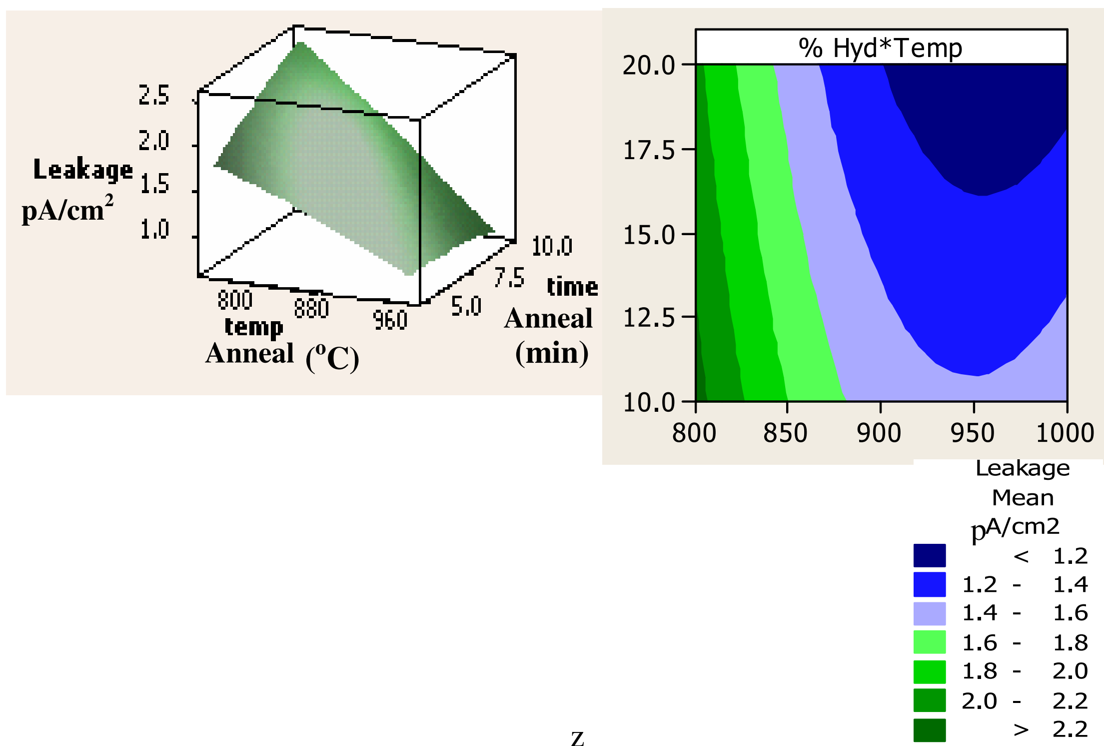


Figure 54 Response surface and contour plots for optimizing annealing time and temperature

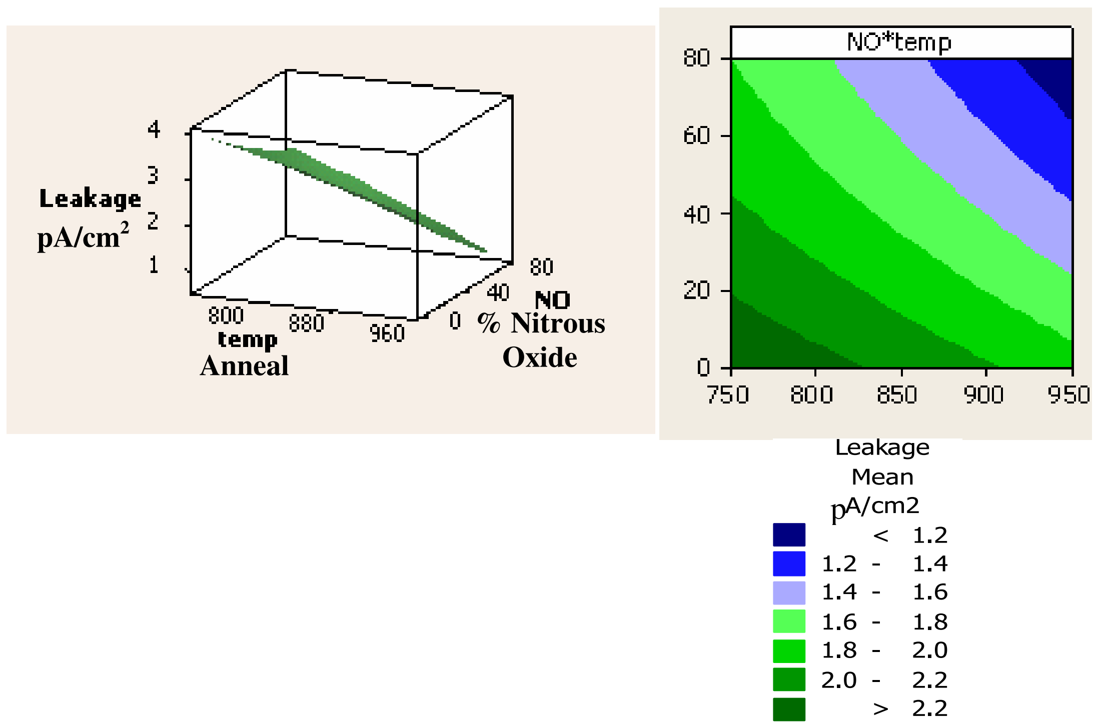


Figure 55 Response surface and contour plots for optimizing annealing temperature and nitrous oxide concentration

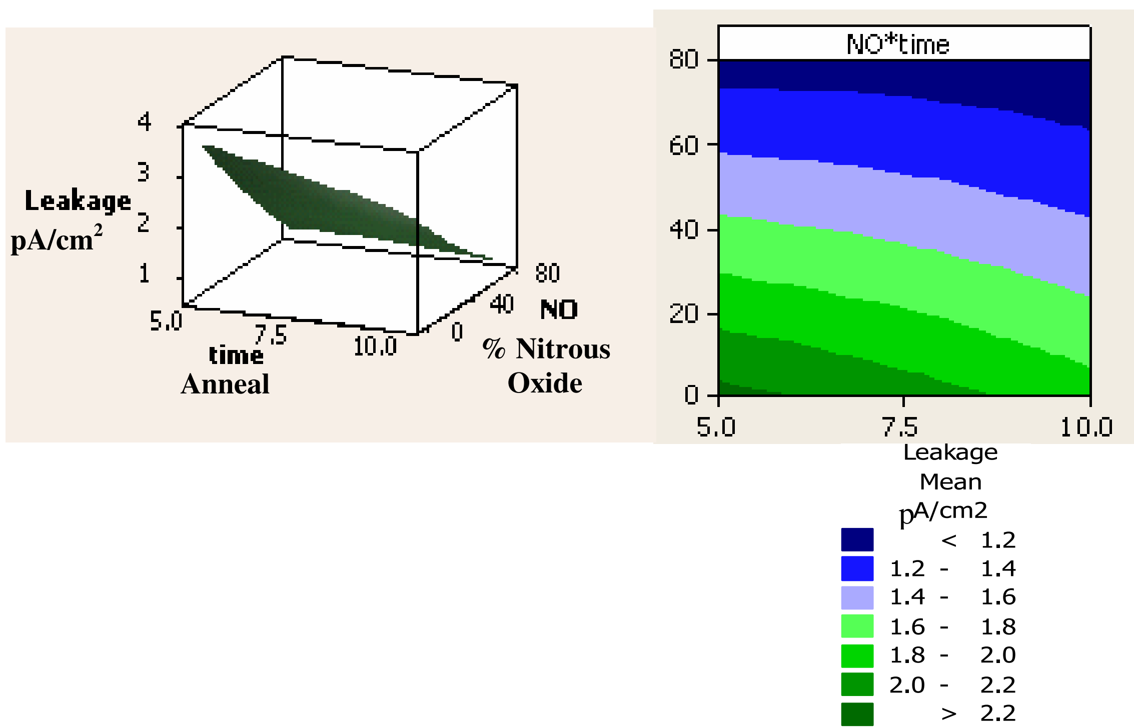


Figure 56 Response surface and contour plots for optimizing annealing time and nitrous oxide concentration

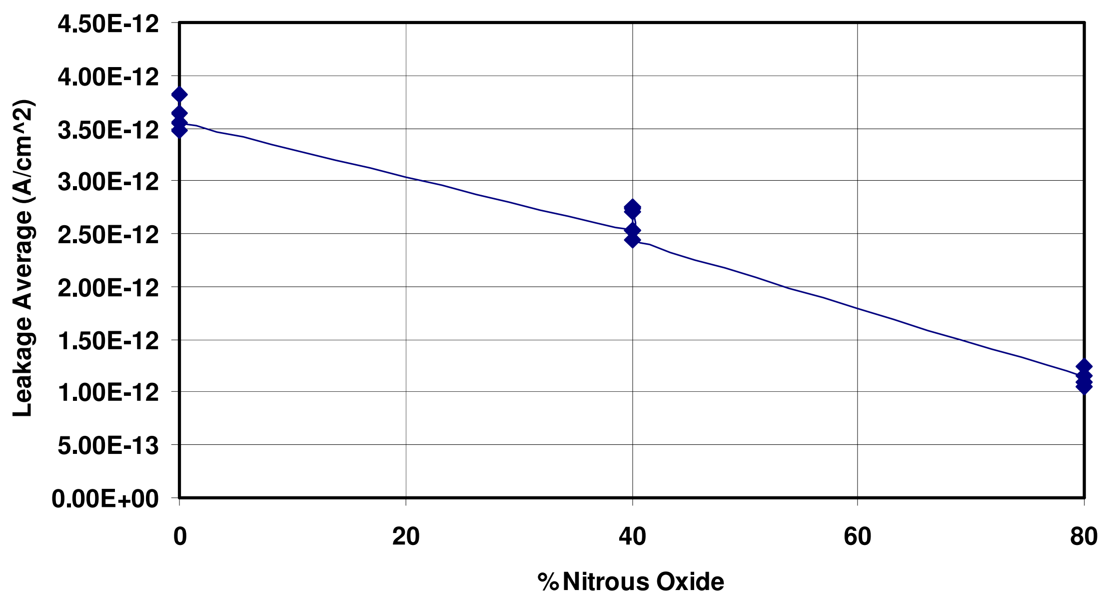


Figure 57 Leakage average for annealing vs. % nitrous oxide

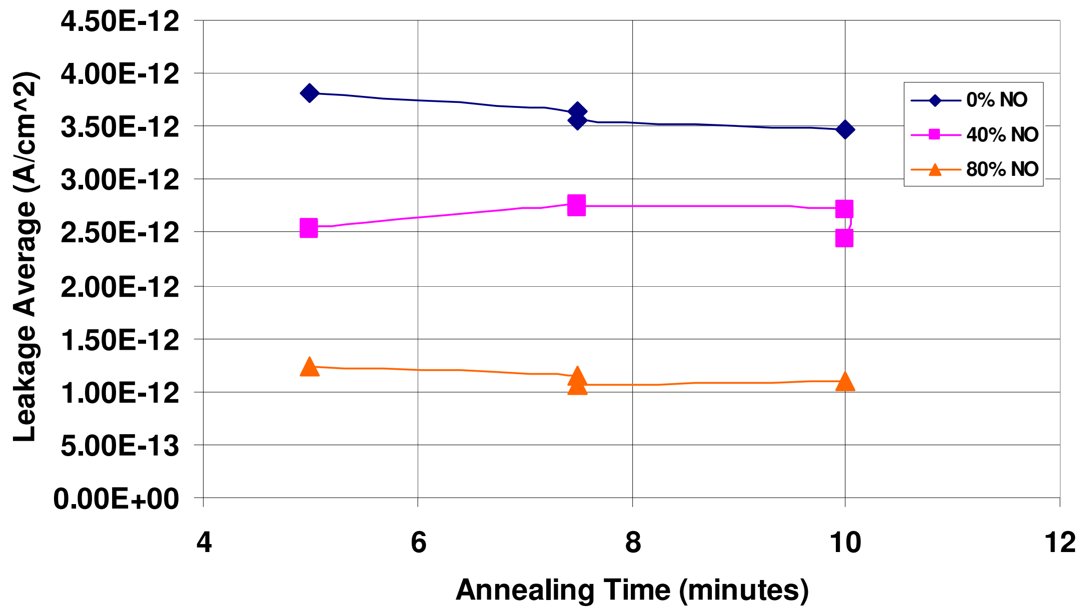


Figure 58 Leakage average vs. annealing time

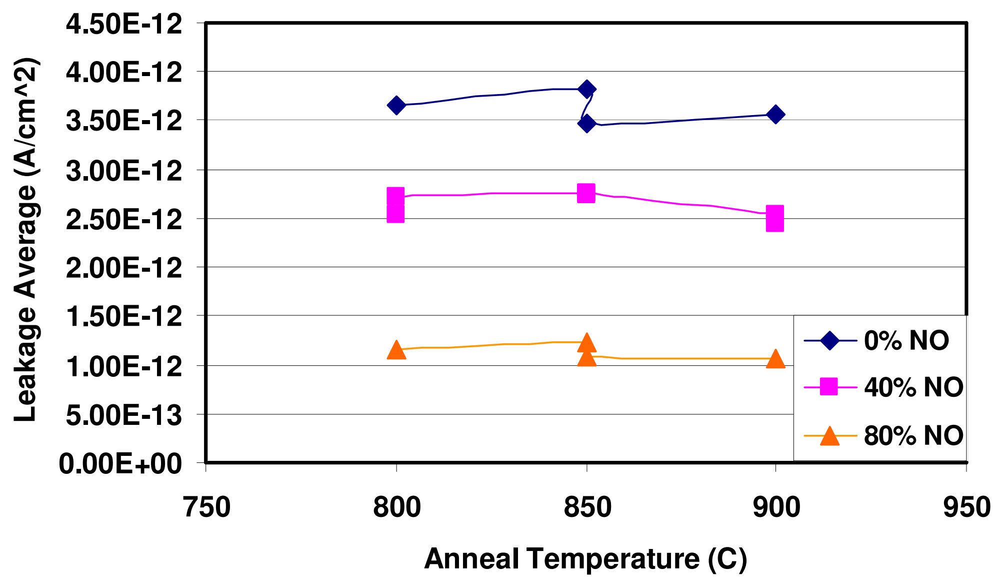


Figure 59 Leakage average vs. anneal temperature

Table 11. Final optimized process recipe for deposition of hafnium oxide films

EX-SITU CLEANING	
Diluted HF-dip (1-2% HF) rinse for 200 seconds.	
3 quick 5 sec DI water rinse.	
IN-SITU CLEANING	
Time	15 min
Temperature	950C
Ambient	20% Hydrogen
PROCESS	
Substrate Temperature	250C
Precursor Pulse Time	1 sec
Purge Pulse Time	5 sec
Water Pulse Time	1 sec
Settling Time	0.3 sec
No. of Cycles	65
ANNEALING	
Time	7.5 min
Temperature	900 C
Ambient	100% Nitrous Oxide

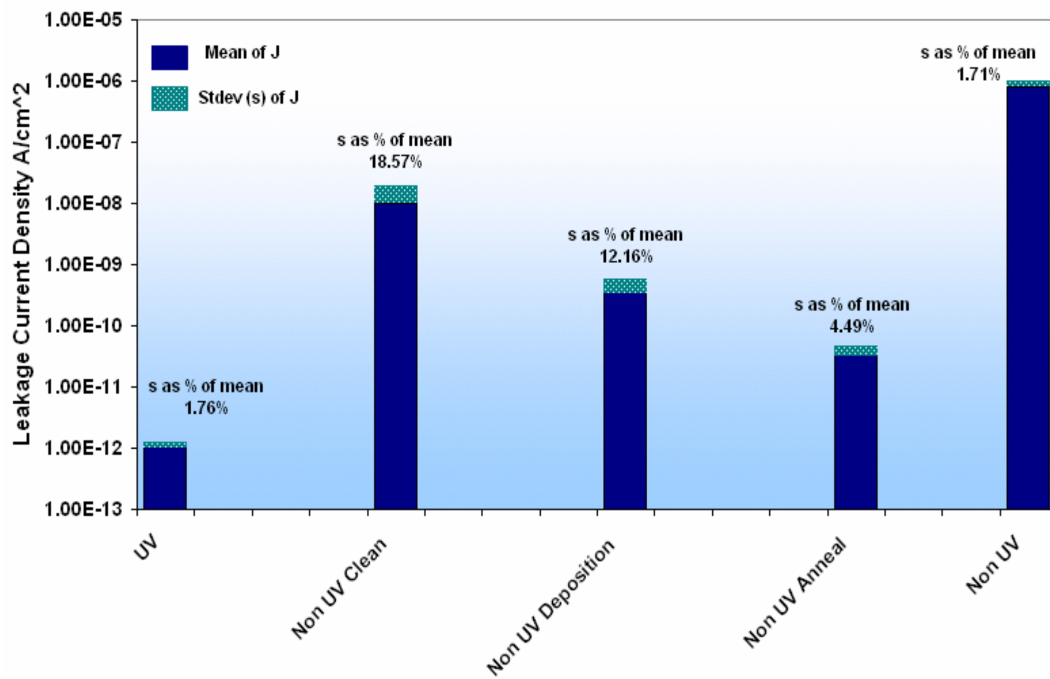


Figure 60 Effect of UV photons on process variation of leakage current for various steps used in the deposition process

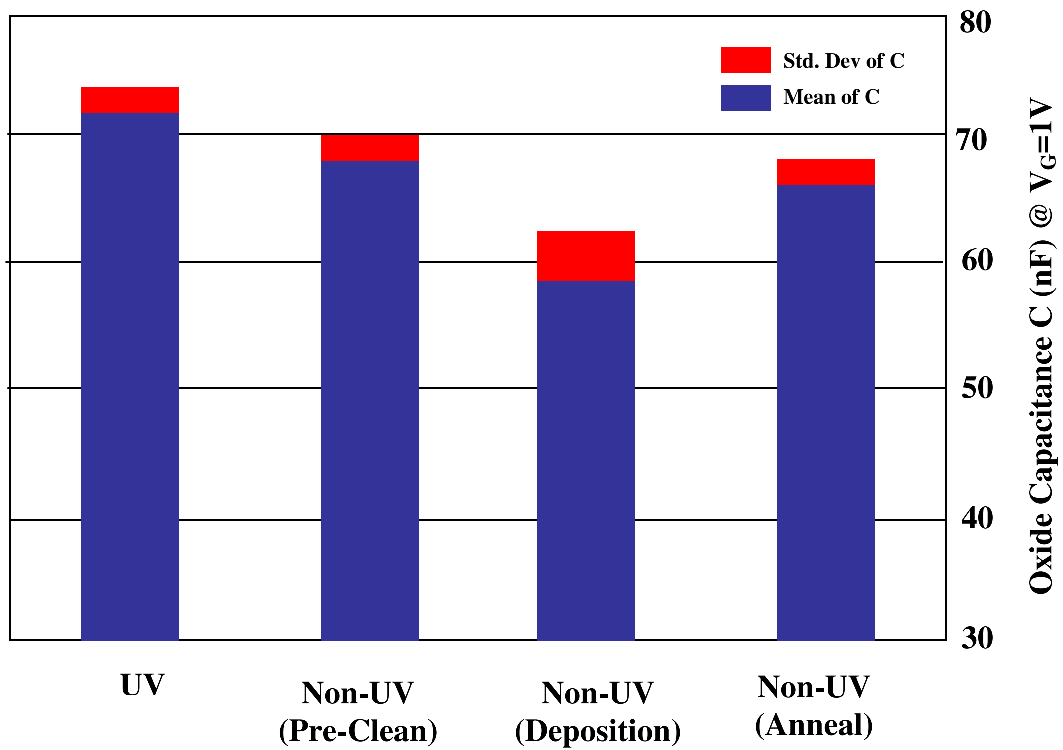


Figure 61 Mean capacitance values (@ VG = 1V) and their standard deviations for gate stacks processed using different UV treatments

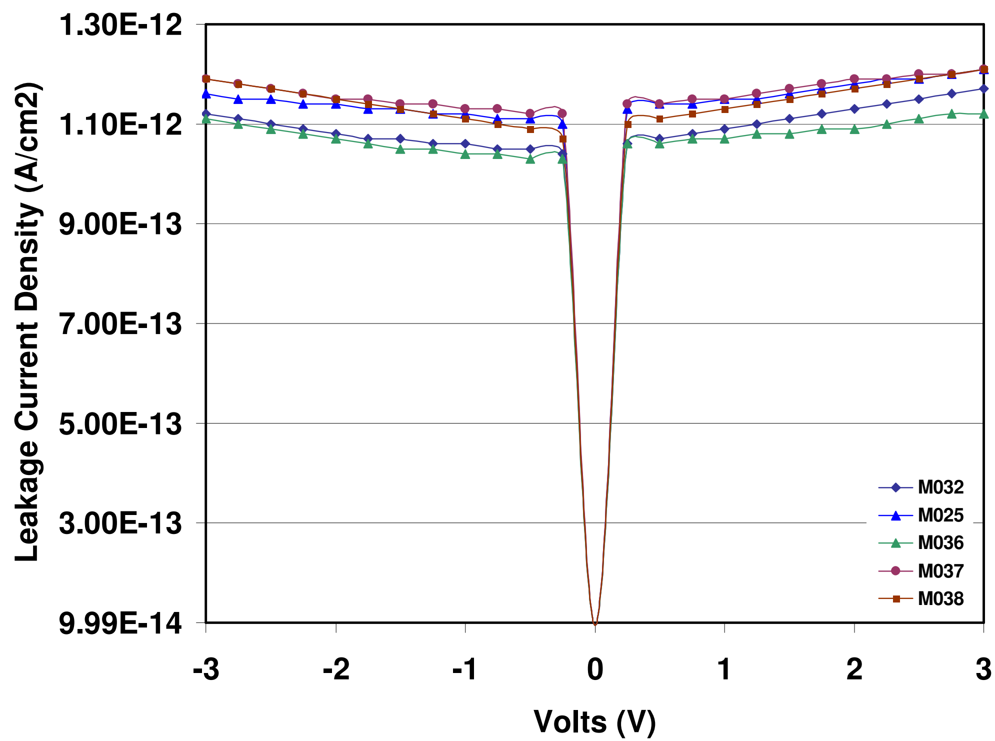


Figure 62 Mean leakage current densities for 6 samples after process optimization through design of experiments

CHAPTER VI

CONCLUSION

For the 45-nm CMOS technology node and beyond issues related to device performance, yield, and reliability are becoming increasingly pronounced. In this study, these challenges were met by developing a front-end CMOS process using RTPMLD for the fabrication of metal gate/high-κ gate dielectric stacks. The experimental data presented in this study demonstrates that the process is robust and manufacturing tools can be developed without any barrier. The availability of such a tool developed in this study with ultra low gate leakage current will simplify the design complexity and will reduce design for manufacturing cost of the next generations of CMOS advanced products. This is a major breakthrough and will have a significant impact on the silicon IC manufacturing.

In Chapter 2, a brief report published results of high dielectric constant gate dielectrics were analyzed with process integration and manufacturing criterions. A careful study of published results showed that from the materials point of view, the MOSFET data indicates significant advantages of using hafnium-based compounds as gate material. Research is ongoing in semiconductor industry to meet the manufacturing needs for process integration requirements to implement high-k gate dielectrics.

In Chapter 3, a new process for the development of rapid photothermal based mono layer deposition (RTPMLD) system was presented in detail. The details of Labview automation were described. It was shown that the RTPMLD processed gate dielectric has the potential to solve manufacturing and process integration issues faced by

the semiconductor industry. RTPALD deposition of HfO_2 films showed a significant reduction in leakage current density as well as increase in capacitance per unit area.

In Chapter 4, the impact of zero gate leakage current density on future CMOS technology nodes was discussed. The MLD process was characterized in great detail using precursor tetrakis dimethyl amido hafnium (TDMAH) for growth rate, deposition cycles, temperature dependence and dielectric thickness. Results were reported for optimized process parameters, for effective oxide thickness of 0.39 nm, we achieved a leakage current density as low as 1x 10^{-12} A/cm^2 at gate voltage of +3 to -3 V. The leakage current density of 1.06 x 10^{-12} A/cm^2 for an EOT 0.39 nm at 1 V represents the lowest value of leakage current reported by any one to date. Detailed high resolution transmission electron microscopy (HRTEM) results were reported showing the interface of silicon and the hafnium oxide. The interface between HfO_2 and Si (001) is atomically sharp and shows that the hafnium oxide layer appears conformal to the (100) silicon substrate having a uniform thickness.

In Chapter 5, the statistical optimization of process parameters was outlined for ex-Situ/in-situ cleaning, deposition and annealing steps. A number of experiments were designed to achieve the lowest leakage current density through Box-Behnken multivariate design techniques. Statistical software MINITAB was used to outline surface and contour plots for optimizing the various process parameters. The advantages of using UV assisted RTP in thin dielectric film were exploited to process thin dielectric films and that was also reported. The electrical data after optimizing for all the parameters was analyzed by statistical methods and the results were compared with 1% level of significance.

The following conclusions can be drawn from the results of this work:

- A new process and tool was developed for the fabrication of high-κ gate dielectric stacks using a single tool. In order to fabricate the Au-HfO_2-Al-Si gate stacks, the wafer pre-clean (in-situ clean), oxide deposition and oxide anneal were performed in-situ. As a result, the number of tools was reduced, reducing the overall process cost.
- The MLD characteristics were studied in detail and using a Box-Behnken multivariate design, statistical design of experiments were conducted to arrive at an optimum recipe for low leakage current density and maximum capacitance per unit area.
- The in-situ process allowed for the fabrication of gate stacks with improved performance characteristics. The in-situ manufactured gate stack displayed leakage currents in the order of 1 pA/cm^2, lowest reported value in the literature so far by four orders of magnitude.
- The in-situ process also allowed for the gate oxide films displaying superior quality at the interface. The Si-SiO_2-HfO_2 interface proved to be atomically sharp in TEM micrographs, with uniform thickness throughout the substrate.
- The effect of UV assisted in-situ processing on device performance and process variation was also investigated. It was shown that the variance in both gate leakage current and insulator capacitance was reduced when UV was used throughout processing. In addition it was found that the

performance characteristics were highly repeatable with 99% confidence using the SWP setup.

In short, the significance of this work for processing is that a front-end CMOS process and tool was developed for the in-situ fabrication of metal gate/high-κ gate stacks using RTPMLD, resulting in the reduction of number of tools needed and improved device performance. This tool can be transferred to a manufacturing environment without any fundamental barrier. This process and tool developed has the unique advantage of lower processing cost, higher throughput and improved device performance.

APPENDICES

Appendix A

Labview Automation

NI PCI-6025E low-cost multifunction I/O board and NI-DAQ for Win 2000/NT/9x was used along with type SH1006868 shielded cable assembly, 2 meters, split 100-pin to two 68-pin shielded cable connectors. This is used to connect 100-pin boards to 68-pin accessories. The 68- pin SCC-68 I/O Connector with 4 SCC module slots was used as the breakout boxes. The PCI-6025E is a 200 kS/s, 12-Bit, 16-Analog-Input Multifunction DAQ with two 12-bit analog outputs; 32 digital I/O lines; two 24-bit counters, 8 additional digital I/O lines (TTL/CMOS) and two 24-bit counter/timers with 4 analog input ranges, and an NI-DAQ driver that simplifies configuration and measurements.

The E series DAQ device was specifically chosen for this application since it offers the following unique advantages [Source: National Instruments]:

1. Temperature drift protection circuitry – Designed with components that minimize the effect of temperature changes on measurements to less than 0.0010% of reading/°C.
2. Resolution-improvement technologies – Carefully designed noise floor maximizes the resolution.
3. Onboard self-calibration – Precise voltage reference included for calibration and measurement accuracy. Self-calibration is completely software controlled, with no potentiometers to adjust.
4. NI DAQ-STC – Timing and control ASIC designed to provide more flexibility, lower power consumption, and a higher immunity to noise and jitter than off-the-shelf counter/timer chips.

5. NI MITE – ASIC designed to optimize data transfer for multiple simultaneous operations using bus mastering with one DMA channel, interrupts, or programmed I/O.
6. NI PGIA – Measurement and instrument class amplifier that guarantees settling times at all gains. Typical commercial off-the-shelf amplifier components do not meet the settling time requirements for high-gain measurement applications.
7. PFI lines – Eight programmable function input (PFI) lines that you can use for software-controlled routing of interboard and intraboard digital and timing signals.
8. RSE mode – In addition to differential and nonreferenced single-ended modes, NI low-cost E Series devices offer the referenced single-ended (RSE) mode for use with floating-signal sources in applications with channel counts higher than eight.
9. Onboard temperature sensor – Included for monitoring the operating temperature of the device to ensure that it is operating within the specified range.

Figure 54 shows the general overview of how Labview was interfaced with the monolayer photoassisted deposition system. Labview 8.0.1 was initially used to generate the code, after which the code was upgraded to Labview version 8.2. Labview was used to automate the pulsing routine for the monolayer deposition, accurate substrate and precursor temperature control and UV/VUV lamp control. In MAX (Measurement and Automation) the details of the global virtual channels used for wiring to the SCC-68 were specified as shown in Table 6. The first column shows the actual global virtual channel created and the next column indicates the terminals used to connect to SCC-68.

All the valves were connected to the Labview SCC-68 breakout box via solid state relays. A solid state relay is a control relay with isolated input and output, whose functions are achieved by means of electronic components without the use of moving parts. These electrical relays are ideal for applications with many contact closures since solid state relay switches offer a greatly extended life compared to other relays.

The SCC-68 is an I/O connector block, which was specifically chosen for this application for easy signal connection to a National Instruments E series DAQ device. The SCC-68 features screw terminals and a general breadboard area for I/O connection, and bus terminals for external power and grounding. The SCC-68 has four slots for integrating thermocouple, current input, isolated voltage input, all of which were used for this application. The pinouts for the SCC-68 I/O board are provided in Figure 55.

Labview code was written for the following:

1. Gas controller VI – This was to enable preset automatic switching of valves V1, V2 and V3, and also VMFC3, VMFC4, VMFC5 and VMFC6.
2. Individual Valve controller VI – In order to pump out each line in the vacuum system a individual valve control for V1, V2, V3 and VMFC3, VMFC4, VMFC5 and VMFC6 was used.
3. PID Control for Substrate Heater – In order to achieve the three different temperature profiles needed for in-situ cleaning, deposition and annealing, a PID control with thermocouple feedback labview program was written to prove +/- 2° C accuracy.

4. PID Control for Precursor oven and delivery – In order to accurately heat the ceramic boat containing the TDMAH precursor, which was placed in a stainless steel tee, a PID control through thermocouple feedback Labview program was written to provide +/- 2° C accuracy. The delivery line from the precursor oven to the chamber was also heated and maintained at the required temperature to prevent condensation.
5. Substrate Temperature readout – Although the PID Labview controller provided accurate temperature profiles of the heater, a thermocouple was clipped using silicon etched pieces to the edge of the wafer for a temperature readout of the substrate. A simple labview program was written to constantly read this temperature.
6. UV Lamp On/Off – Labview was used to interface with the RC-500B Pulsed UV system to switch the UV lamp on and off. Flexibility was provided in the VI to also specify a time for which the lamp should be kept on, if needed.

Table 7 shows the valve numbers, their corresponding SCC-68 pinouts and the solid state relays that were used to do the wiring to Labview. Table 8 denotes the same for the thermocouple controls used.

Gas Controller VI

Figure 56 shows the user interface that was used for this VI. 'PC' denotes the length of time in seconds the precursor delivery valve to the chamber should be open (Valve V1). Similarly N2 denotes the length of time in seconds the UHP nitrogen purge valve (Valve V2) should be open. H2O denotes the water vapor valve (Valve V3). N2 represents the

same valve, Valve V2, but for ease of using one cycle of deposition, it was represented as shown. The 'iterations' denotes the number of cycles of deposition. And the current count can be seen to estimate time remaining for the next step. Three LED's were used, and a green light glowed whenever that valve was On. The flowchart for the logic used to create the VI is shown in Figure 4. The code is shown in Figures 5.

PID Controller For Heater and Oven

The proportional integral derivative (PID) algorithm is one of the most common control algorithms used in industry. In PID control, you must specify a process variable and a set point. The process variable is the system parameter you want to control, such as temperature, pressure, or flow rate, and the set point is the desired value for the parameter you are controlling. A PID controller determines a controller output value, such as the heater power or valve position. The controller applies the controller output value to the system, which in turn drives the process variable toward the set point value. One can use the PID control toolkit VIs with National Instruments hardware to develop Labview control applications. Use I/O hardware, such as a data acquisition device, Field Point I/O module, or GPIB board, to connect your PC to the system you want to control. The I/O VIs provided in Labview with the Labview PID control toolkit was used to develop a control application or modify the examples provided with the toolkit through a DAQ-MX device. The Labview PID control toolkit includes PID and fuzzy logic control VIs and provided +/- 2° C accuracy for temperature control for both the Boraelectric heater and

precursor Oven temperature control. The user interfaces for these two VI's are provided in Figures 59 and 60. The PID toolkit is available through National Instruments website.

Substrate Temperature Readout

In order to ensure that the silicon wafer was at the required temperature, although the PID controller for the Boraelectric heater provided accurate control within 2° C, a bare-wire K-type thermocouple from Omega Inc was used to read out the temperature constantly of the silicon wafer edge. Several tests were conducted to ensure if the wafer was heated uniformly, by placing 4 thermocouples on four quadrants of the wafer. Since the substrate size was only 2" diameter, it was found that the position of the thermocouple did not make a difference and that the wafer was heated uniformly. For the Labview program, the thermocouple was attached to a wafer edge through a silicon etched piece, which was mounted off the Boraelectric heater moly nut (non power connections end) and hence provided reliable feedback throughout the processing steps. The user interface is shown in Figure 61. A digital readout provided constant monitoring of the silicon wafer, the code is shown in Figure 62. A MAX global virtual channel was created for the analog thermocouple channel.

UV Lamp Control

A custom made UV lamp was used, so that the lamp was placed over the wafer in the chamber in a quartz tube. The RC-500B Pulsed UV Curing System was modified for the lamp connections, and Labview was used to trigger the lamp on and off. The RC-500B is a high-intensity, timed or continuous mode system, intended to provide a broad spectrum

of high intensity pulsed light, in the range of 200 to 1100 nm. Figure 63 shows the user interface VI and Figure 64 shows the flowchart used for writing the VI code.

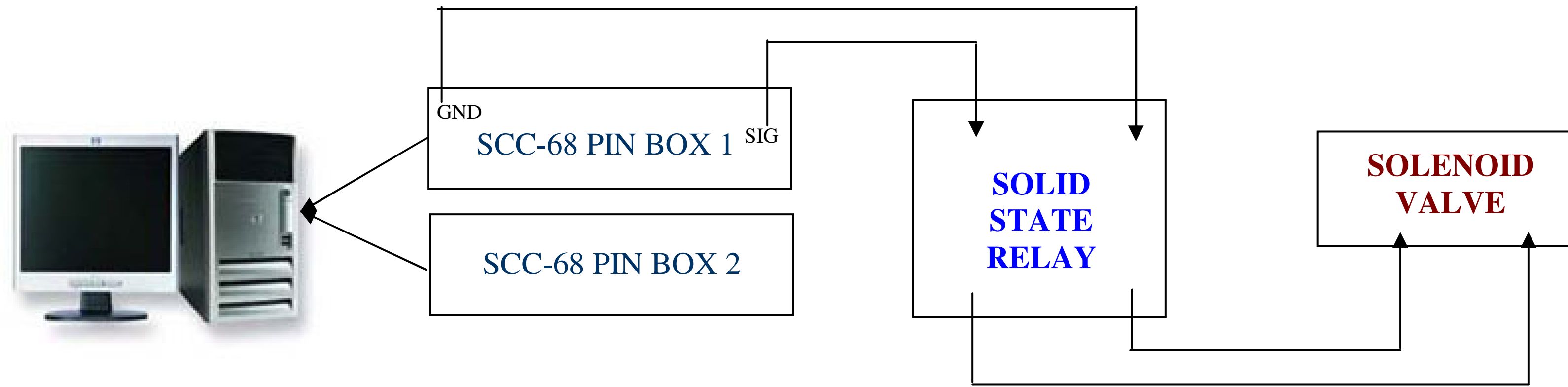


Figure 63 General Overview of Labview interface

Table 12 NI-DAQ MX Virtual channels and corresponding SCC-68 pinouts

NI-DAQ MX Global Virtual Channel	Terminal on SCC-68
MV1 LINE 0	52
MV2 LINE2	17
MV3 LINE 3	49
MV4 LINE 4	47
MV5 LINE 5	19
MV7 LINE 13	51
MV10 LINE 12	16
V1 LINE 10	48
V2 LINE 5	11
V3 LINE 6	10
V4 LINE 7	43
V5 LINE 11	42

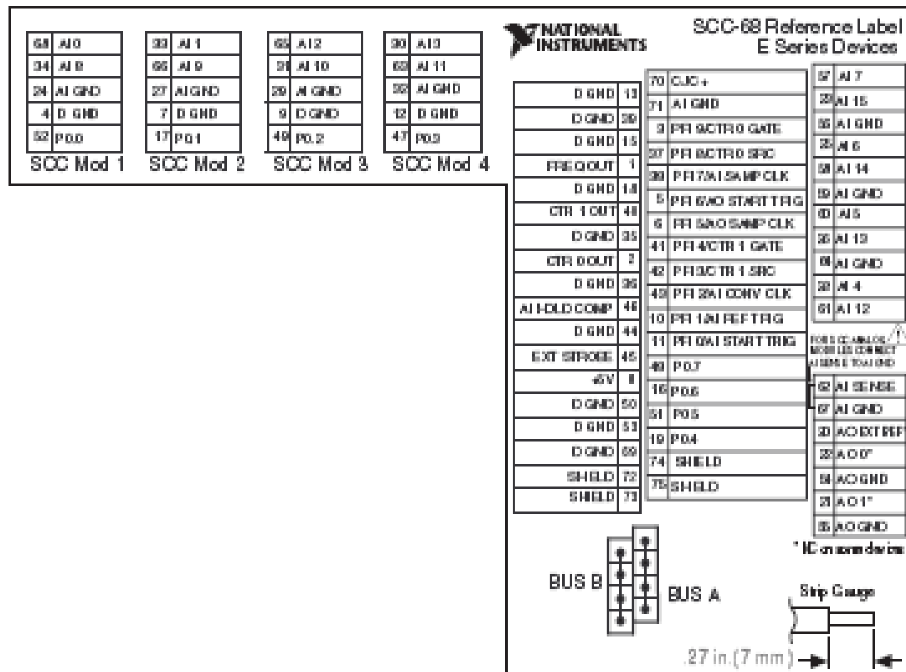


Figure 64 SCC-68 pinouts

Table 13 SCC-68 pinouts and corresponding solid state relays and valves

Valve	Port	LINE	Pin	Relay
V1	0	4	19	SR1
V2	0	5	51	SR2
V3	0	6	16	SR3
V4	0	7	48	SR4
V5	1	0	1	SR5
VMFC3	0	0	52	SR6
VMFC4	0	1	17	SR7
VMFC5	0	2	49	SR8
VMFC6	0	3	47	SR9
UV	1	2	43	SR10

Table 14 Analog inputs and corresponding SCC-68 pinouts

Thermocouple	Terminal on SCC-68
HEATER	AI4
WAFER	AI12
PC OVEN	AI13
PC DELIVERY	AI5

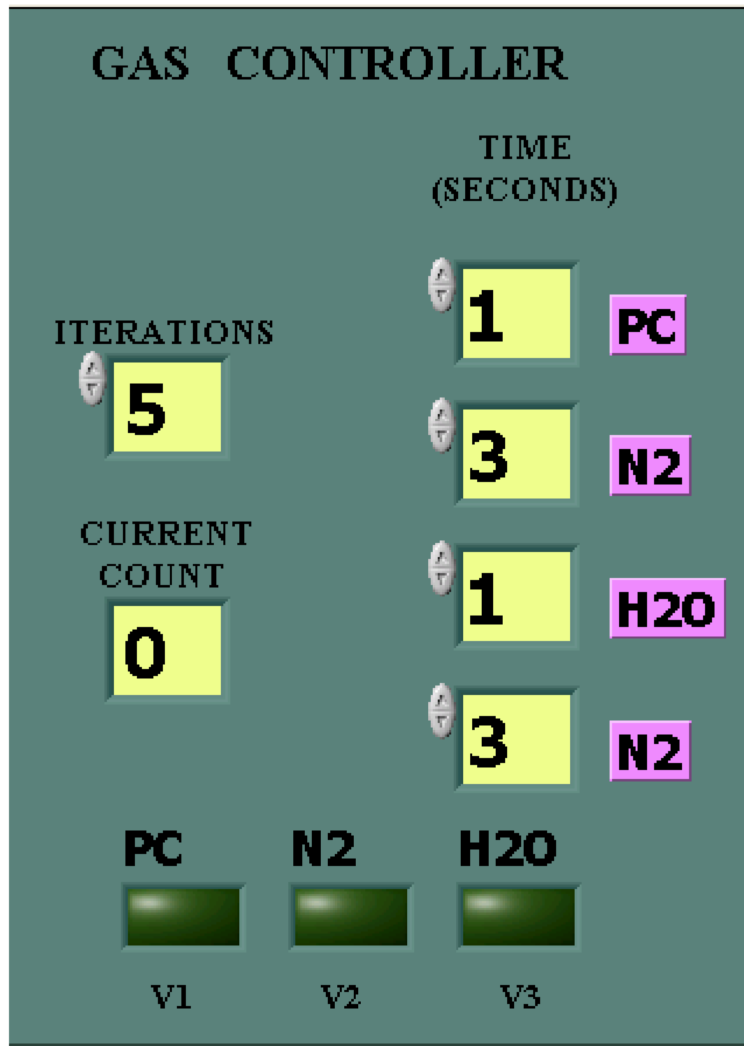


Figure 65 Gas controller VI user interface

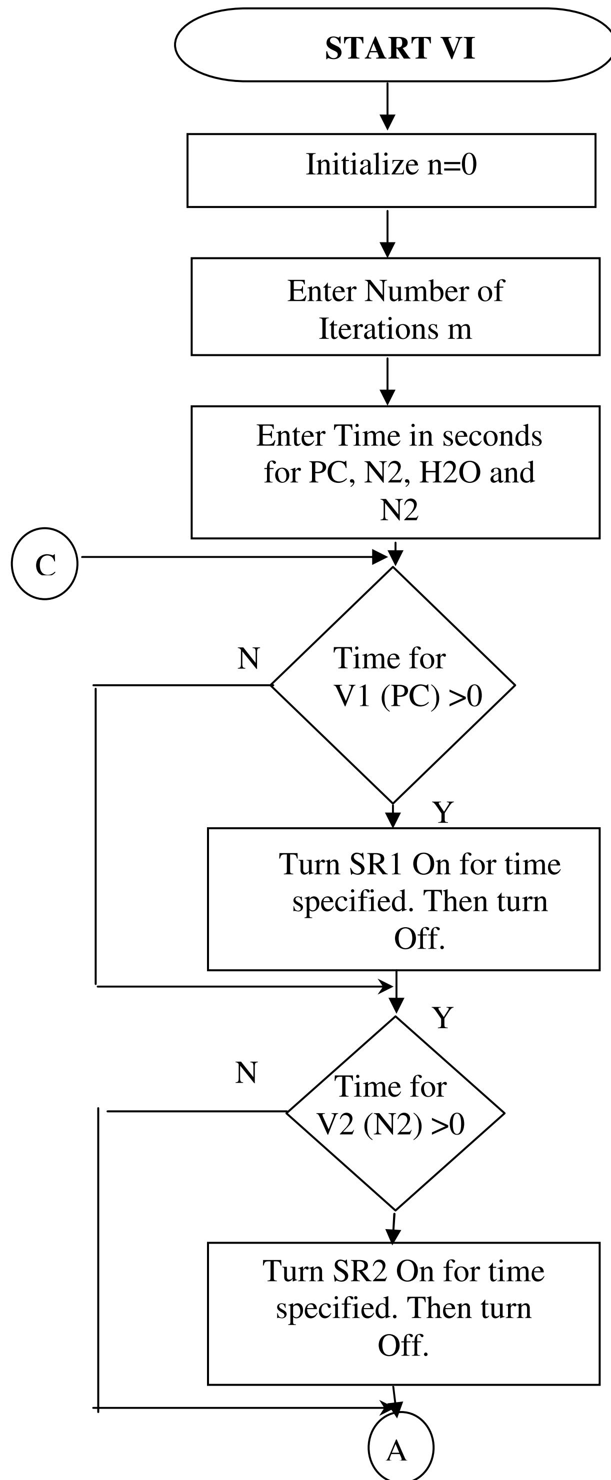
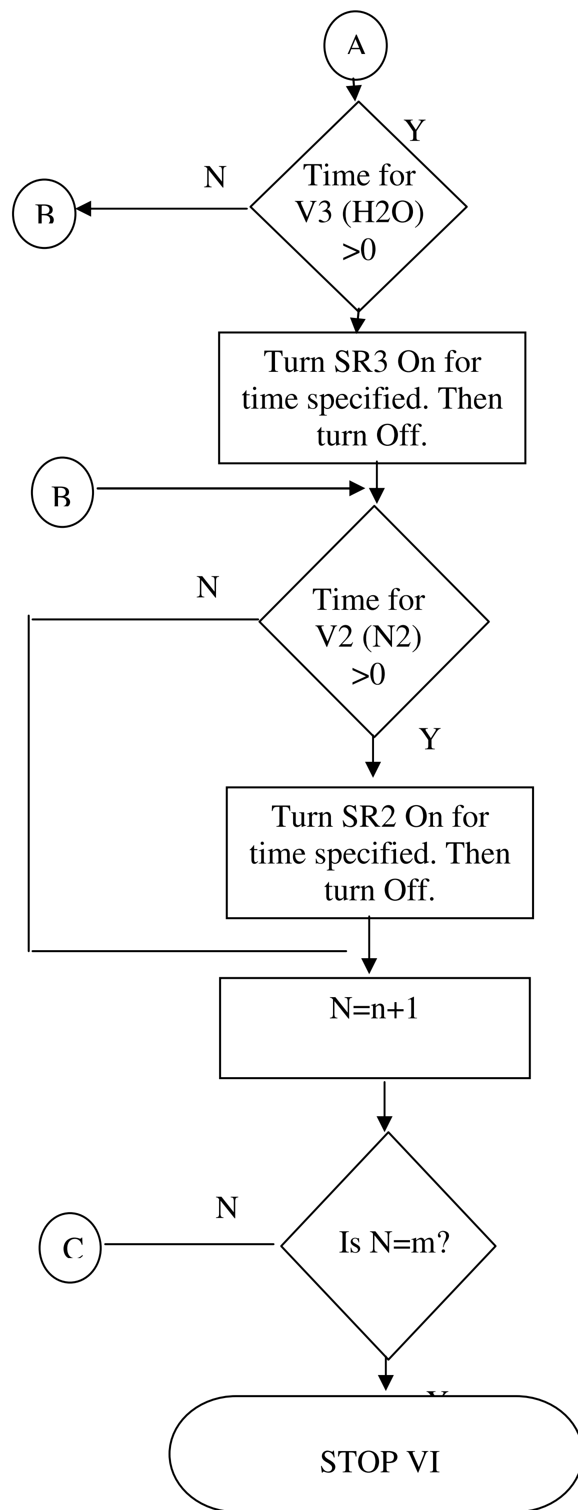


Figure 66 Flowchart for gas controller VI



(contd) Flowchart for gas controller VI

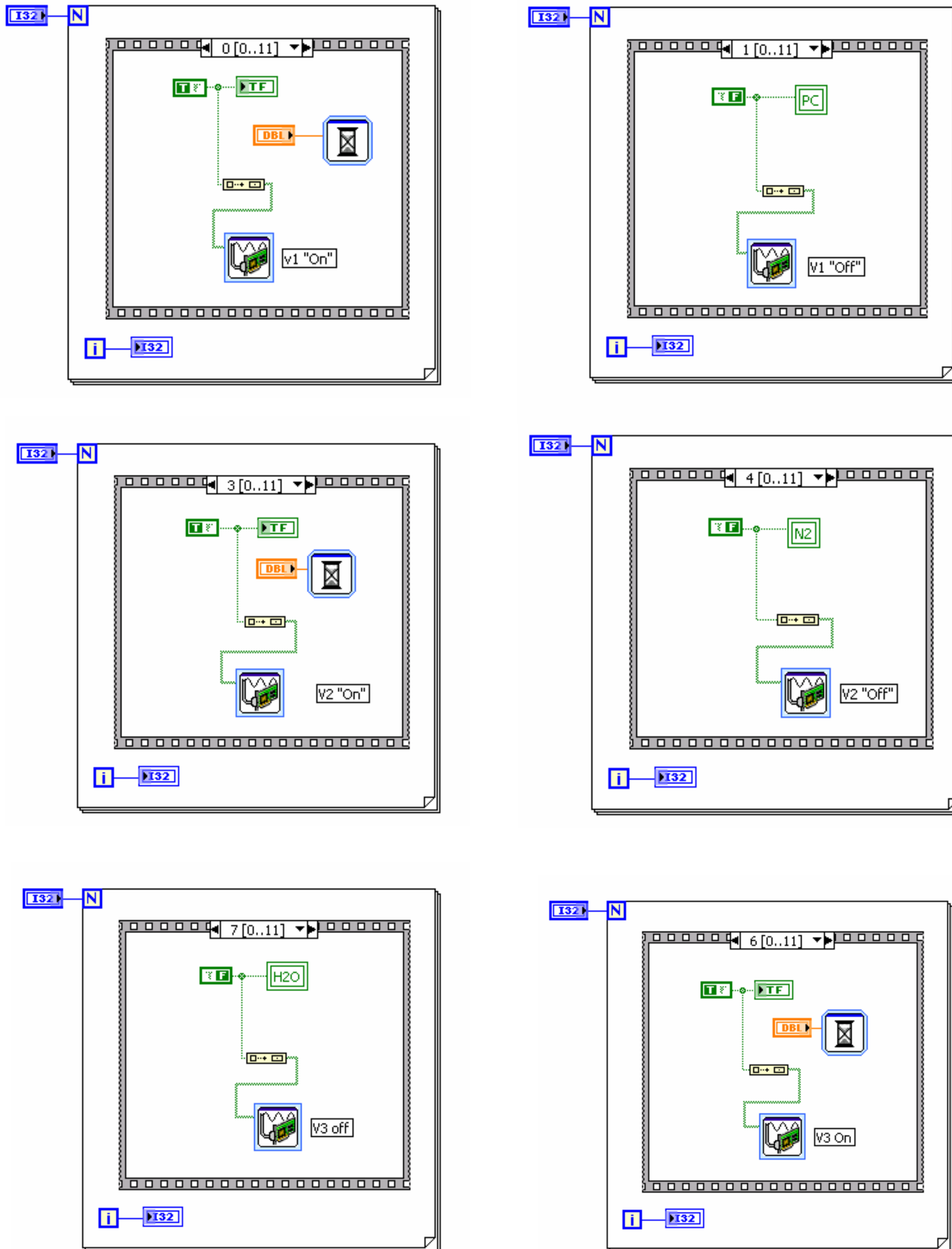


Figure 67 Gas controller VI Code

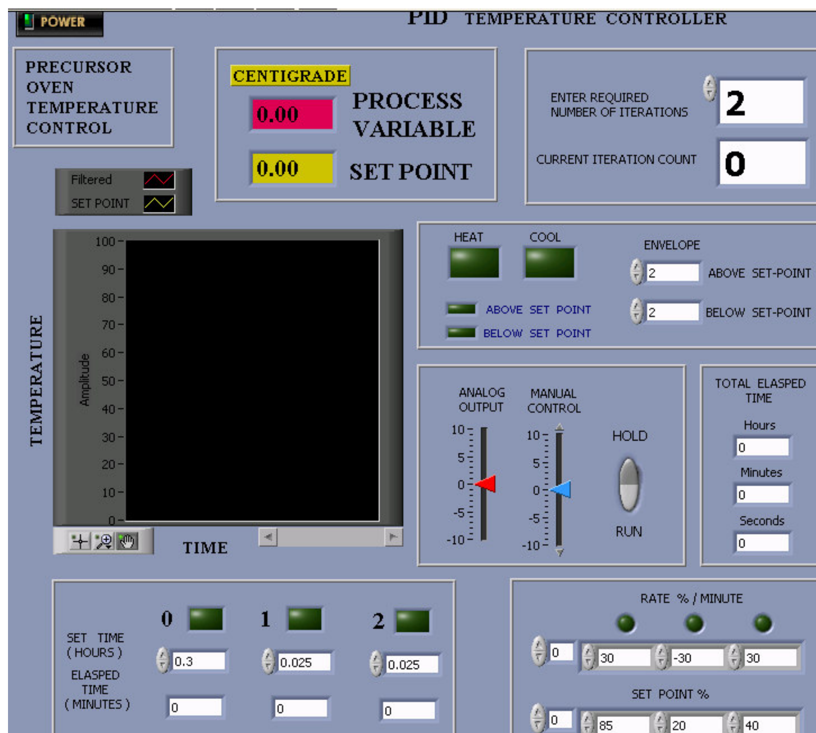


Figure 68 PID toolkit for precursor oven temperature control

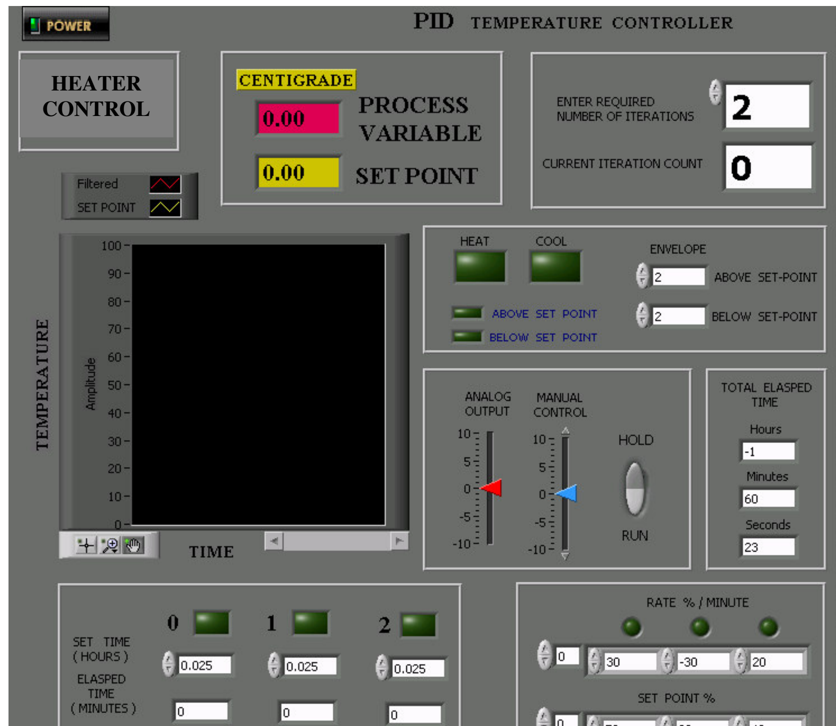


Figure 69 PID toolkit for heater control

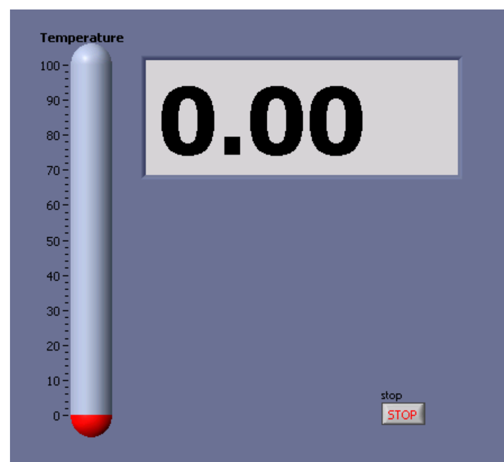


Figure 70 User interface for wafer temperature readout

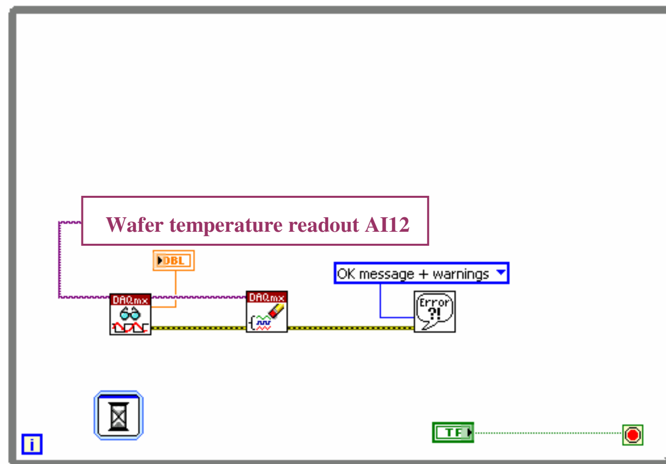


Figure 71 Labview VI for wafer temperature readout

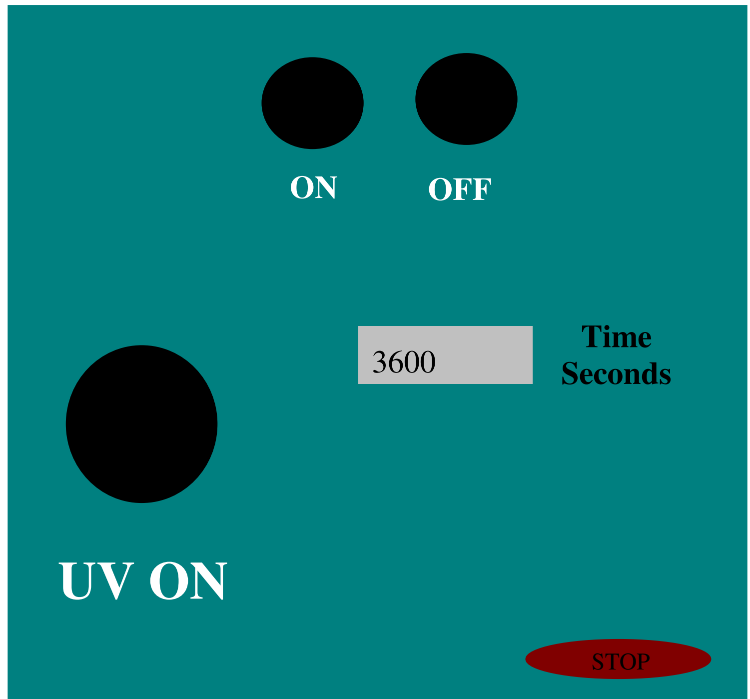


Figure 72 User interface for UV lamp control

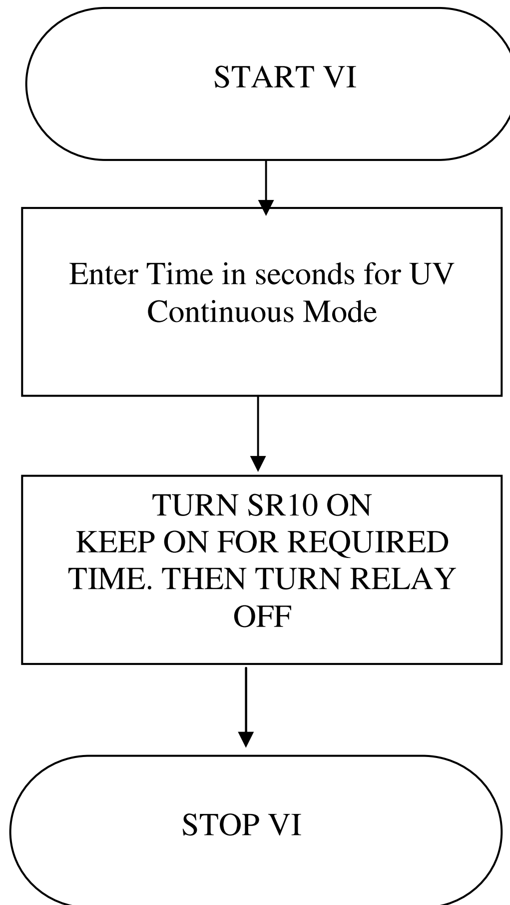


Figure 73 Flowchart for UV lamp control Labview code

Appendix B

Statistical design of Experiments

As an extension to the statistical design of experiments presented in Chapter 5, Figure 74 shows the shows the main interactions plot with fitted means and leakage current density as the response for in-situ cleaning. Figure 75 shows the main interactions for the annealing DOE with leakage current density as the response. Figure 76 shows the cube plot for the fitted means with the leakage response. Figures 77 and 78 show the overlaid contour plots for the three response factors to identify the main interactions. Figure 79 shows the summary of statistics for the annealing DOE. Figure 80 shows the SAS response showing the model fitted was acceptable.

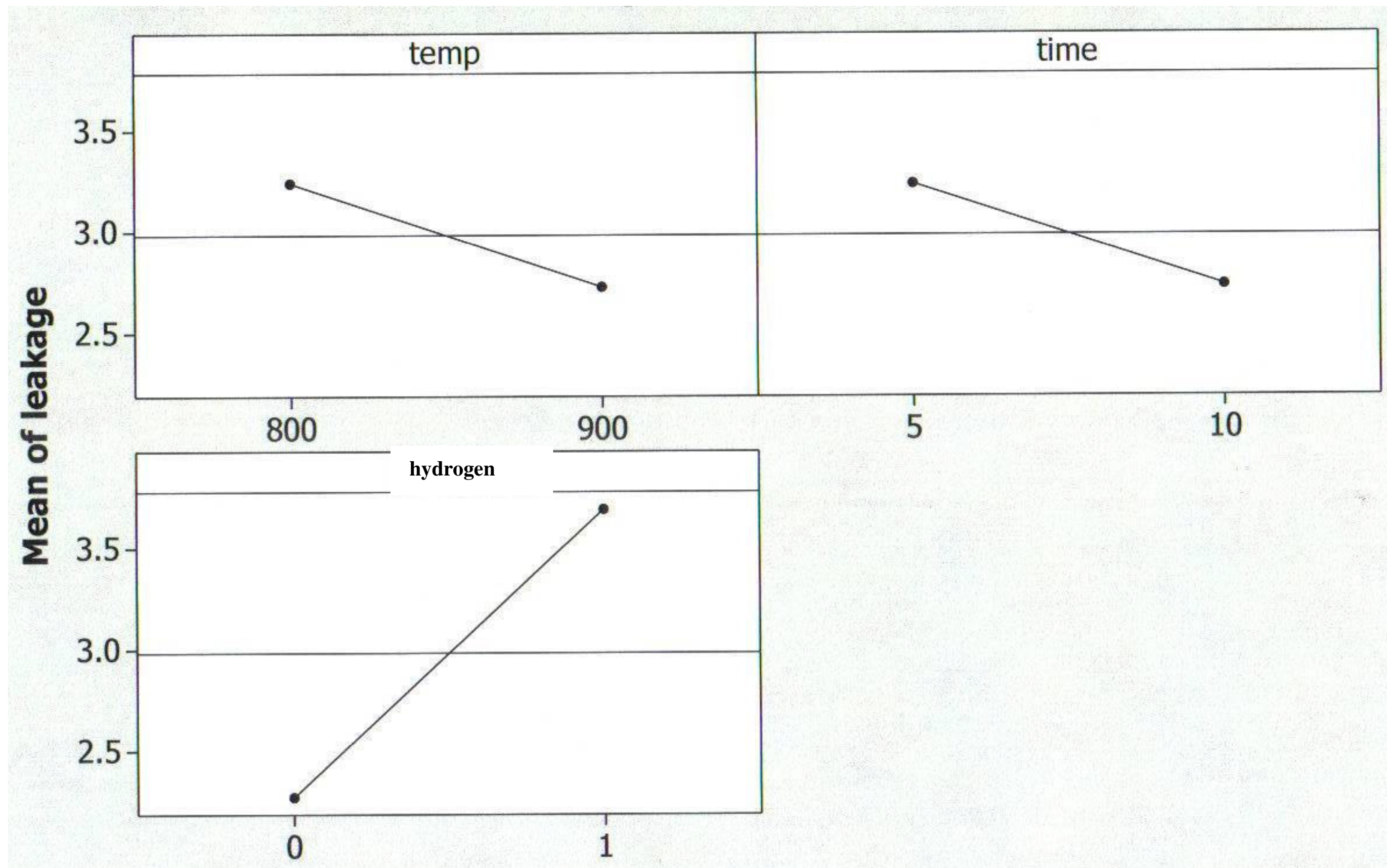


Figure 74 Main interactions plot for leakage response

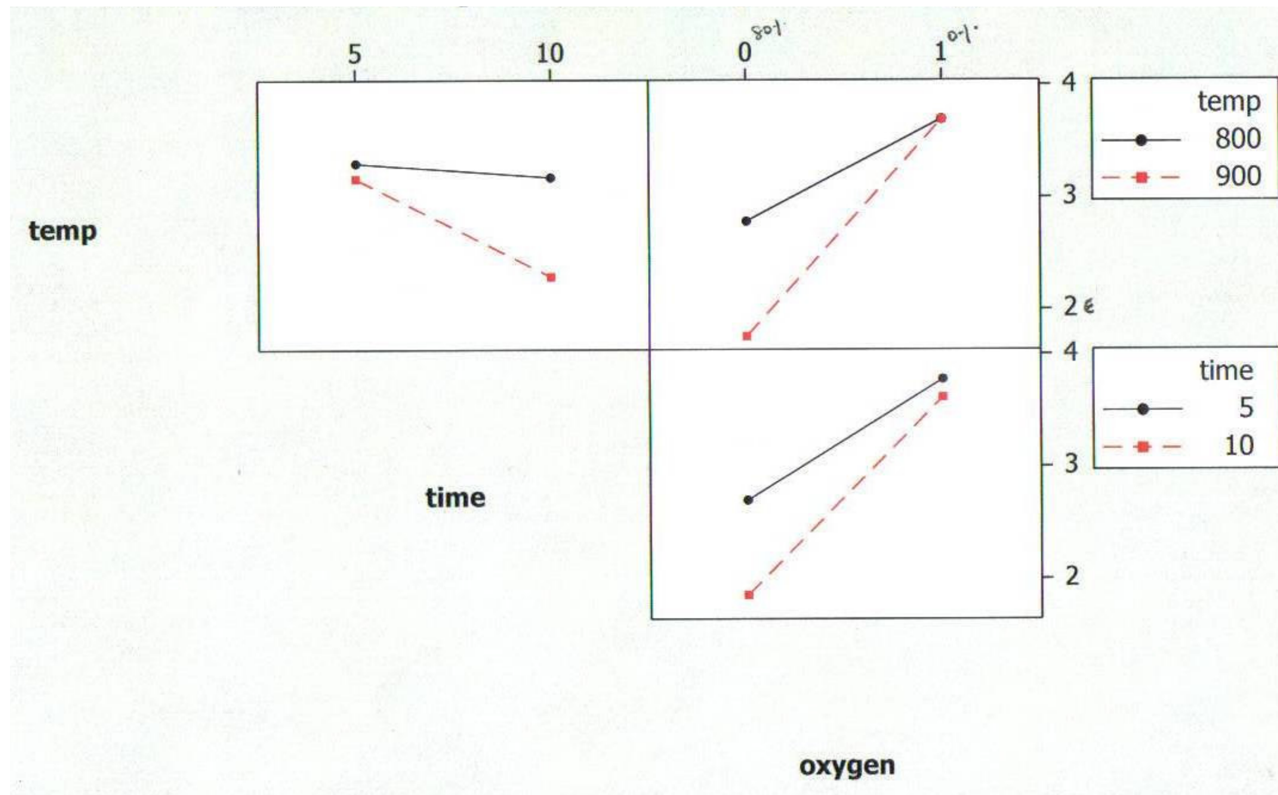


Figure 75 Main level interactions plot for annealing DOE

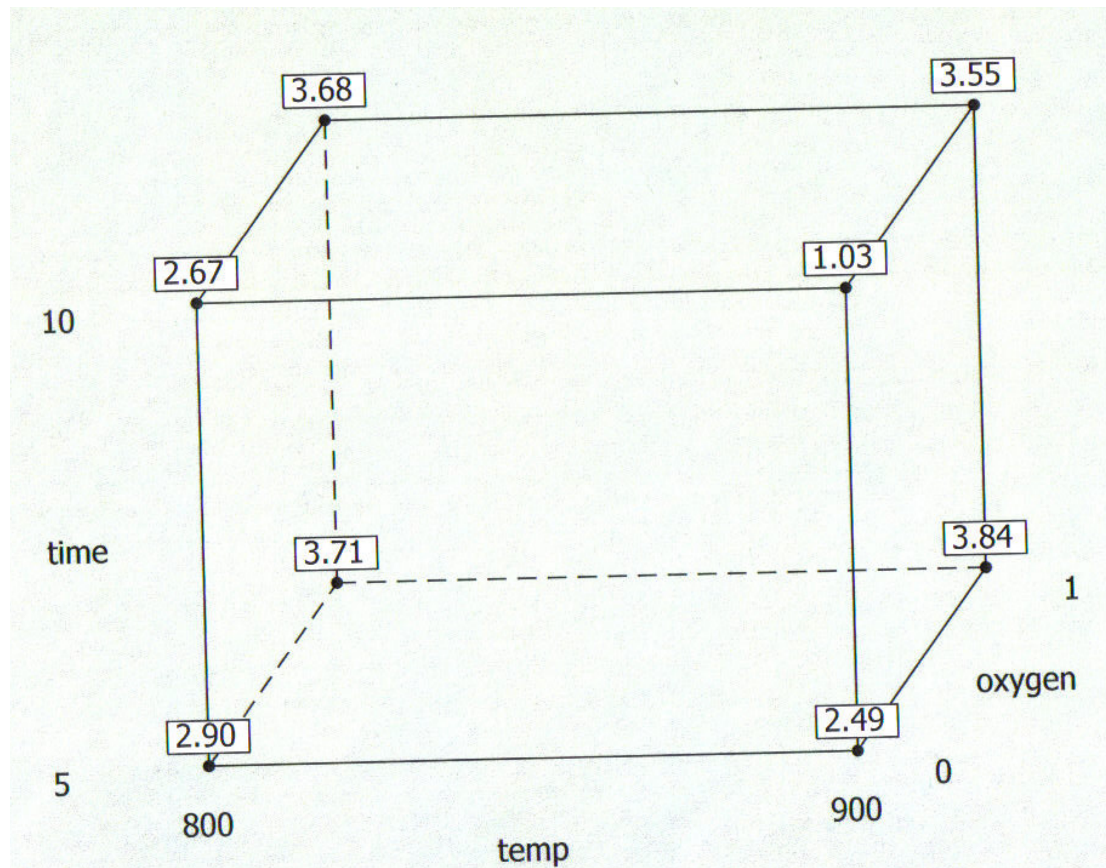


Figure 76 Cube plot for leakage (fitted means)

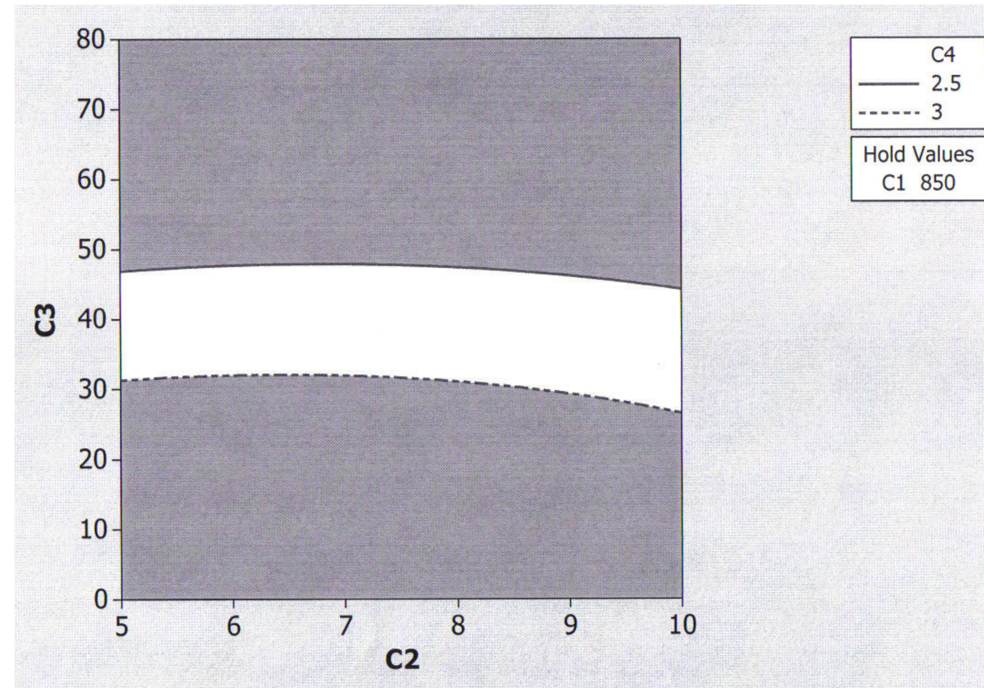


Figure 77 Overlaid contour plot for annealing DOE (C1 time, C2 temperature, C4 is leakage response)

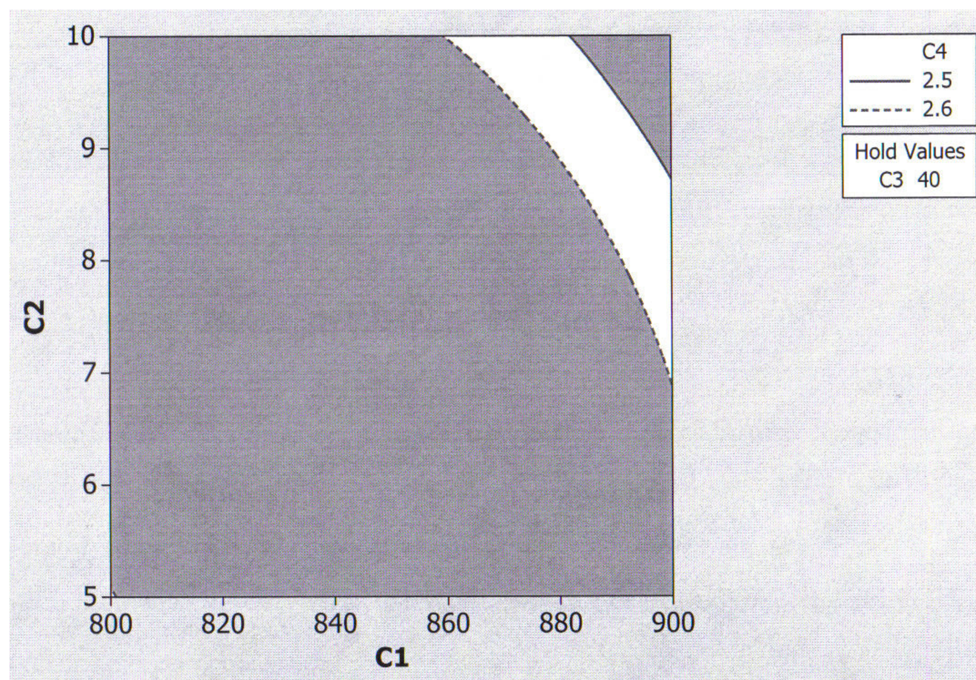


Figure 78 Overlaid contour plot for annealing DOE (C1 time, C2 temperature, C3 % Hyd)

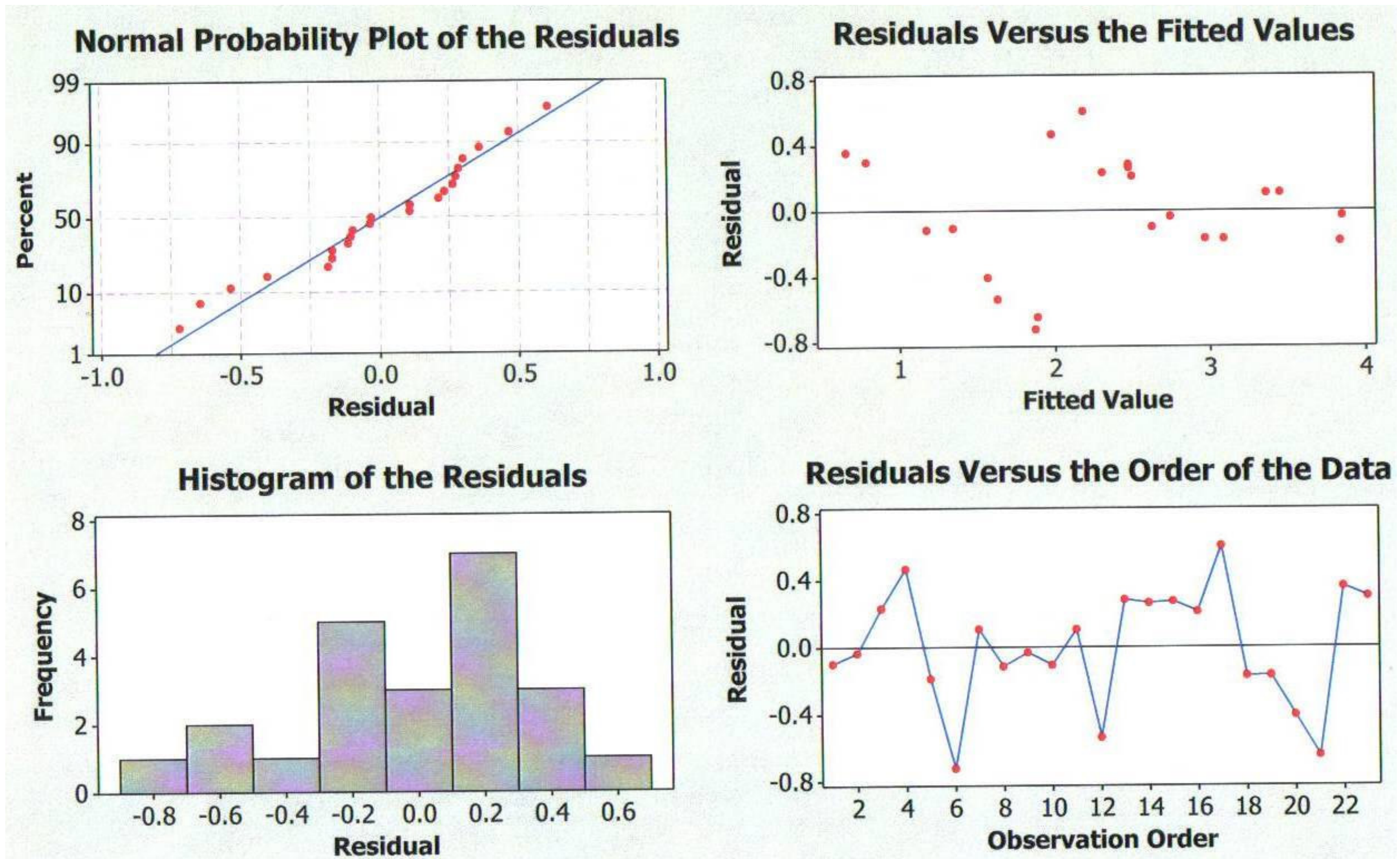


Figure 79 Descriptive statistics residual plot for annealing DOE

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The RSREG Procedure

Coding Coefficients for the Independent Variables

Factor	Subtracted off	Divided by
x1	850.000000	50.000000
x2	7.500000	2.500000
x3	40.000000	40.000000

Response Surface for Variable y

Response Mean	2.501333
Root MSE	0.094366
R-Square	0.9965
Coefficient of Variation	3.7726

Regression	DF	Type I Sum of Squares	R-Square	F Value	Pr > F
Linear	3	12.444325	0.9693	465.82	<.0001
Quadratic	3	0.320898	0.0250	12.01	0.0101
Crossproduct	3	0.028225	0.0022	1.06	0.4450
Total Model	9	12.793448	0.9965	159.63	<.0001

Residual	DF	Sum of Squares	Mean Square	F Value	Pr > F
Lack of Fit	3	0.044325	0.014775	147.75	0.0067
Pure Error	2	0.000200	0.000100		
Total Error	5	0.044525	0.008905		

Parameter	DF	Estimate	Standard Error	t Value	Pr > |t|	Parameter Estimate from Coded Data
Intercept	1	-34.186250	14.443306	-2.37	0.0642	2.750000
x1	1	0.085425	0.033534	2.55	0.0514	-0.053750
x2	1	0.589500	0.342590	1.72	0.1459	-0.051250
x3	1	-0.021188	0.020527	-1.03	0.3493	-1.245000
x1*x1	1	-0.000048500	0.000019644	-2.47	0.0566	-0.121250
x2*x1	1	-0.000540	0.000377	-1.43	0.2119	-0.067500
x2*x2	1	-0.011400	0.007858	-1.45	0.2065	-0.071250
x3*x1	1	0	0.000023592	0.00	1.0000	5.005245E-17
x3*x2	1	0.000500	0.000472	1.06	0.3378	0.050000
x3*x3	1	-0.000171	0.000030694	-5.57	0.0026	-0.273750

Figure 80 SAS results for annealing DOE

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The RSREG Procedure

Canonical Analysis of Response Surface Based on Coded Data

Factor	Critical Value Coded	Critical Value Uncoded
x1	0.128755	856.437772
x2	-1.258862	4.352845
x3	-2.388937	-55.557487

Predicted value at stationary point: 4.265911

Eigenvalues	Eigenvectors x1	x2	x3
-0.051986	-0.435802	0.894377	0.100826
-0.137362	0.899634	0.429489	0.078726
-0.276901	-0.027107	-0.125015	0.991784

Stationary point is a maximum.

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The RSREG Procedure

Factor	DF	Sum of Squares	Mean Square	F Value	Pr > F
x1	4	0.095620	0.023905	2.68	0.1539
x2	4	0.067982	0.016995	1.91	0.2474
x3	4	12.686898	3.171725	356.17	<.0001

Figure 80 SAS results for annealing DOE (contd)