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CIRCUIT MODULES FOR BROADBAND CMOS SIX-PORT SYSTEMS

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CIRCUIT MODULES FOR BROADBAND CMOS SIX-PORT SYSTEMS

A Dissertation
Presented to
the Graduate School of
Clemson University

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy
Electrical Engineering

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by
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December 2010

Accepted by:
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ABSTRACT

This dissertation investigates four circuit modules used in a CMOS integrated six-port measurement system. The first circuit module is a wideband power source generator, which can be implemented with a voltage controlled ring oscillator. The second circuit module is a low-power 0.5 GHz – 20.5 GHz power detector with an embedded amplifier and a wideband quasi T-coil matching network. The third circuit module is a six-port circuit, which can be implemented with distributed or lumped-element techniques. The fourth circuit module is the phase sifter used as calibration loads. The theoretical analysis, circuit design, simulated or experimental verifications of each circuit module are also included.

DEDICATION

I thank my Lord for guiding me and giving me faith. When I was weak, my mother, Yinzhi Wu, always told that she would pray for me and then my heart was filled with faith and hope. Without the love, trust, and support of my mother, I do not know where I would be at this time. My wife, Fei Gong, has been my partner throughout this work, and her love and understanding was invaluable.

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PUBLICATIONS

1. C. J. Li, F. Gong, P. Wang, “A Low-Power Active Inductor with Improved Q-factor and Its Application to Phase Shifter,” Analog Integrated Circuits and Signal Processing (In press).
2. C. J. Li, F. Gong, P. Wang, “A Folded, Low-Power Ultra-Wideband CMOS Power Detector with an Embedded Amplifier,” IEEE Trans. on Instrumentation and Measurement, 2010 (in press).
3. C. J. Li, F. Gong, P. Wang, “Analysis and Design of a High-Q Differential Active Inductor with Wide Tuning Range,” IET Circuits, Devices & Systems, 2010 (in press).
4. P. Wang, H. Wang, Y. Gao, Y. Geng, George Thomas, C. J. Li, “A High-Speed Sample-and-Hold Circuit Based on Integrated Transmission Lines,” Analog Integrated Circuits and Signal Processing, 2010 (in press).
5. P. Wang, Y. Geng, H. Zou, H. Wang, C. J. Li, “An on-chip Power Modulator,” IEEE Int. PMHVC, 2010 (in press).
6. H. Zou, Y. Geng, C. J. Li, P. Wang “A Comparison Study of On-Chip Short Pulse Generation Circuits Based on Transmission Line,” IEEE Int. PMHVC, 2010 (in press).
7. C. J. Li, F. Gong, P. Wang, “A Wideband LNA Matched with Quasi T-coil Networks in 0.13 μm CMOS,” IEEE 53rd Int. MWSCAS, pp. 926-929, 2010.

8. H. Zhang, C. J. Li, Ralu Divan, Axel Hoffmann, P. Wang, “Broadband Magnoise of Patterned Permalloy Thin Films,” IEEE Trans. on Magnetics, Vol. 46, No. 6, pp. 2442-2445, 2010.
9. C. J. Li, H. Zhang, P. Wang, “A Novel Six-port Circuit Based on Four Quadrature Hybrids,” Int. J. RF and Microwave CAE, Volume 20 Issue 1, pp. 128-132, 2010.
10. C. J. Li, P. Wang, “A High Frequency Tunable Differential Active Inductor and Its Application to Power Dividers,” IEEE 51st Int. MWSCAS, pp. 285-288, 2008.

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CHAPTER ONE

INTRODUCTION

The six-port measurement system was introduced at the National Institute of Standards and Technology [1.1]-[1.2]. Based on the linear assumption, the following equations exist in a six-port network shown in Figure 1.1(a):

$$b_3 = Aa_2 + Bb_2 \quad , \qquad (1.1)$$

$$b_4 = Ca_2 + Db_2 \quad , \qquad (1.2)$$

$$b_5 = Ea_2 + Fb_2 \quad , \qquad (1.3)$$

$$b_6 = Ga_2 + Hb_2 \quad , \qquad (1.4)$$

where A, B, C, D, E, F, G, H are complex coefficients.

A six-port measurement system includes a source generator which is connected to Port 1, a six-port circuit, and four power detectors which are connected to Port 3, Port 4, Port 5, and Port 6. The power response P_i (i=3, 4, 5, and 6) of the power detectors at port P_3-P_6 can be obtained from equations (1.1)-(1.4) and are given as:

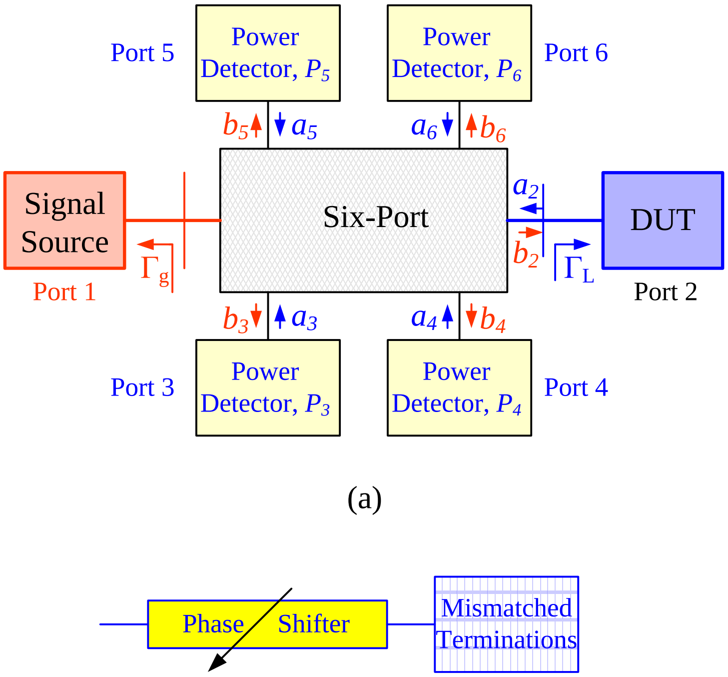
$$P_3 = |A|^2 |b_2|^2 |\Gamma_L - q_3|^2 \quad , \qquad (1.5)$$

$$P_4 = |D|^2 |b_2|^2 |q_4 \Gamma_L - 1|^2 \quad , \qquad (1.6)$$

$$P_5 = |E|^2 |b_2|^2 |\Gamma_L - q_5|^2 \quad , \qquad (1.7)$$

$$P_6 = |G|^2 |b_2|^2 |\Gamma_L - q_6|^2 \quad , \qquad (1.8)$$

$$\Gamma_L = \frac{a_2}{b_2},\quad q_3 = -\frac{B}{A},\quad q_4 = -\frac{C}{D},\quad q_5 = -\frac{F}{E},\quad q_6 = -\frac{H}{G}. \tag{1.9}$$



(a)

(b)

Figure 1.1 A six-port system. (a) A six-port network. The parameter a_i, b_i, p_i are incident waves, reflected waves, and power at port i, respectively. (b) Calibration loads.

If port 4 is treated as a power reference port and is isolated from port 2 (it means $q_4=0$) [1.1], then the power ratio P_i/P_4 (i=3, 5, 6.) are given as:

$$\frac{P_3}{P_4} = \left|\frac{A}{D}\right|^2 \left|\Gamma_L - q_3\right|^2 , \tag{1.10}$$

$$\frac{P_5}{P_4} = \left|\frac{E}{D}\right|^2 \left|\Gamma_L - q_5\right|^2 , \tag{1.11}$$

$$\frac{P_6}{P_4} = \left|\frac{G}{D}\right|^2 \left|\Gamma_L - q_6\right|^2 . \tag{1.12}$$

q_i (i=3,5, and 6) are complex constants, and $\left|\frac{A}{D}\right|^2$, $\left|\frac{E}{D}\right|^2$, $\left|\frac{G}{D}\right|^2$ are three real constants, and then there are nine unknown parameters which are only determined by the six-port physical structure. The nine unknown parameters can be obtained through calibration with calibration loads depicted in Fig. 1.1(b) [1.3]-[1.5]. With all those parameters, the magnitude and phase of the reflection coefficient for a Device-Under-Test (DUT) can be determined through power readings which are scalars and are easily measured. Compared with the heterodyne network analyzer, the six-port measurement device is significantly less expensive, and is useful for reflection coefficient measurements. Due to the robustness and simplicity of the six-port measurement device, it can be used for other applications, such as transceivers in communication systems [1.6], complex permittivity measurement devices [1.7], vector voltmeters [1.8], and cancer detectors [1.9].

At present, the theory of six-port measurement is fully understood and complete, and the calibration methods are close to optimum [1.10]. Current activities concentrate mainly on new six-port structures, new applications, and new implementation methods. Most published six-port structures are based on transmission line technology or a Wheatstone bridge with lumped elements (such as resistors) [1.11]-[1.15]. Even though the loss in the six-port circuits based on transmission line technique is low, the drawbacks of them are narrowband and a large area [1.11]. While the six-port circuits based on resistors can provide much larger operating frequency ranges, their loss is high, even up to 75% [1.12]-[1.13].

Considering the requirements for a large operating frequency range, small area, low loss in the six-port network and high measurement accuracy, this dissertation, for the first time, focuses on the integration of the six-port measurement system with CMOS technology. There are four circuit modules, a signal generator which can be a ring oscillator, four power detectors, a six-port circuit, and a phase shifter as depicted in Fig. 1.1.

In Chapter II*, a platform to estimate the oscillation frequency and waveform amplitude for a high frequency differential ring oscillator in deep submicron CMOS technology was developed. The nonlinear characterizations are specially analyzed. In Chapter III [1.17], a 0.5 GHz – 20.5 GHz CMOS low-power power detector with an embedded amplifier and a wideband quasi T-coil is proposed, analyzed, designed, and measured. In Chapter IV [1.18], a differential active inductor with 10.2 GHz self resonance frequency for a lumped-element six-port circuit is proposed, designed, and measured. The noise, self resonance frequency, nonlinearity, and power consumption of the proposed active inductor are also analyzed. In Chapter V [1.19], a new six-port circuit is proposed, simulated, and measured. In Chapter VI [1.20], a phase shifter with high Q-factor active inductor is proposed and simulated for calibration usage.

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* Chapter II is a manuscript submitted to the IEEE Transactions on Circuits and Systems II on August 13, 2009(Control Number: 6829). Since this independent work was partially similar to a paper appeared in the IEEE Transactions on Circuits and Systems-I: Regular Papers December 2009[16], it might not be published in future.

References

[1.1] ENGEN, G. F.: The Six-Port Reflectometer: an alternative network analyzer. IEEE Trans. on Microwave Theory and Techniques, vol. MTT-25, no. 12, p. 1075-1080, Dec. 1977.

[1.2] ENGEN, G. F.: An improved circuit for implementing the six-port technique of microwave measurements. IEEE Trans. on Microwave Theory and Techniques, vol. MTT-25, no. 12, p. 1080-1083, Dec. 1977.

[1.3] Glenn F. Engen, "Calibrating the Six-Port Reflectometer by Means of Sliding Terminations," IEEE Trans. on Microwave Theory and Techniques, Vol. MTT-26, No. 12 p. 951-957, December 1978.

[1.4] Ulrich Stumper, "Finding Initial Estimates Needed for the Engen Method of Calibrating Single Six-Port Reflectometers," IEEE Trans. on Microwave Theory and Techniques, Vol. 38, No. 7, July 1990.

[1.5] Frank Wiedmann, Bernard Huyart, Eric Bergeault, Louis Jallet, "A New Robust Method for Six-Port Reflectometer Calibration," IEEE Trans. on Instrumentation and Measurement, Vol. 48, No. 5, October 1999.

[1.6] Hyung-Sun Lim, Wan-Kyu Kim, Jong-Won Yu, Hyung-Chul Park, Woo-Jin Byun, and Myung-Sun song, "Compact Six-Port Transceiver for Time-Division Duplex Systems", IEEE Microwave and Wireless Components Letters, VOL. 17, NO. 5, MAY 2007.

[1.7] A. L. de S. Rolim, A. J. B. de Oliveira, M. T. Melo, “Measuring Complex Permittivity with the Six-port technique,” IEEE International conference on MTT-S Microwave and Optoelectronics, 2005.

[1.8] Marek E. Bialkowski, Amin M. Abbosh, Norhudah Seman, “Compact Microwave Six-Port Vector Voltmeters for Ultra-Wideband Applications,” IEEE Trans. on Microwave Theory and Techniques, Vol. 55, No. 10, October 2007.

[1.9] Norhudah Seman, Marek E. Bialkowski, “Design of a UWB 6-port reflectometer formed by microstrip-slot couplers for use in Microwave Brease Cancer Detection System,” IEEE International Symposium Antennas and Propagation, 2007.

[1.10] Vladimir Bilik, Six-Port Measurement Technique: Principles, Impact, Applications.

[1.11] Ji Yun Yao, Swee Ping Yeo, “Six-Port Reflectometer Based on Modified Hybrid Couplers,” IEEE Trans. on Microwave Theory and Techniques, Vol. 56, No. 2, February 2008.

[1.12] V. Bilik, V. Raffai, J. Bezek, “Miniature Broadband lumped six-port reflectometers,” Journal Communication, 42, p. 7-14, 1991.

[1.13] X. Z. Xiong, V. F. Fusco, “Wideband 0.9 GHz to 5 GHz six-port and its application as digital modulation receiver,” IEE. Proc.-Microw. Antennas Propagation, Vol. 150, No. 4, August 2003.

[1.14] Jan Hesselbarth, Frank Wiedmann, Bernard Huyart, “Two New Six-Port Reflectometers Covering Very Large Bandwidths,” IEEE Trans. on Instrumentation and Measurement, Vol. 46, No. 4, August 1997.

[1.15] Frank Wiedmann, Bernard Huyart, Eric Bergeault, Louis Jallet, “New Structure for a Six-Port Reflectometer in Monolithic Microwave Integrated-Circuit Technology,” IEEE Trans. on Instrumentation and Measurement, Vol. 46, No. 2, April 1997.

[1.16] Payam M. Farahabadi, Hosscin Miar-Naimi, Ataollah Ebrahimzadch, “Closed-Form Analytical Equations for Amplitude and Frequency of High-Frequency CMOS Ring Oscillators,” IEEE Trans. on Circuits and Systems-I: Regular Papers, Vol. 56, No. 12, December 2009.

[1.17] Chaojiang Li, Fei Gong, Pingshan Wang, “A Low-Power Ultra-Wideband CMOS Power Detector with an Embedded Amplifier,” IEEE Trans. on Instrumentation and Measurement, 2010 (In press).

[1.18] Chaojiang Li, Fei Gong, Pingshan Wang, “Analysis and Design of a High-Q Differential Active Inductor with Wide Tuning Range,” IEE Trans. on Circuits, Devices and Systems, 2010 (In press).

[1.19] Chaojiang Li, Hanqiao Zhang, Pingshan Wang, “A Novel Six-Port Circuit Based on Four Quadrature Hybrids,” International Journal of RF and Microwave Computer-Aided Engineering, Vol. 20 Issue 1, p. 128-132, 2010.

[1.20] Chaojiang Li, Fei Gong, Pingshan Wang, “A low-Power Active Inductor with Improved Q-factor and Its Application to Phase Shifter,” Analog Integrated Circuits and Signal Processing, 2010 (In revision)

CHAPTER TWO

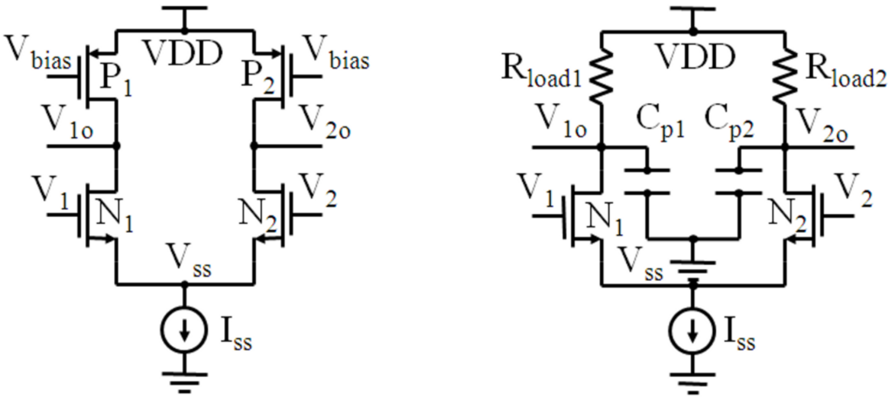
ANALYSIS OF A HIGH FREQUENCY DIFFERENTIAL RING OSCILLATOR IN DEEP SUBMICRON CMOS TECHNOLOGY

Abstract—In this chapter, analytical equations for oscillation frequency and waveform amplitude of a high frequency differential ring oscillator are derived with a new platform. The obtained equations describe the nonlinear dependence of amplitude and frequency on the number of delay cell stages and transistor sizes. The accuracies of the obtained equations are verified by the Cadence Spectre simulated results and experimental data. Compared with currently available expressions, the obtained equations show significantly improved accuracies; therefore they can be used to guide and facilitate oscillator design. The derivation platform can also be used to analyze other ring oscillator topologies.

I. INTRODUCTION

Ring oscillators (RO) are an integral part of phase-locked loops, clock recover circuits, frequency synthesizers and ultra-wideband impulse-radios [2.1]-[2.4]. The oscillation amplitude and frequency are two critical design parameters, which are also prerequisites for the analysis of phase noise [2.5]-[2.9]. Yet, the current calculation equations of oscillation amplitude and frequency are still inadequate to describe the nonlinear dependence of amplitude and frequency on design parameters despite many effects [2.9]-[2.13]. Therefore, more accurate equations are still needed to guide and facilitate oscillator CAD designs, in which tradeoffs in terms of power consumption, chip area, and noise performance are always needed for different applications. Deriving such equations through a new method is the purpose of this work.

Differential ROs are often used for their superior common mode noise rejection capabilities as opposed to single ended structures. The basic delay cell of a differential ring oscillator shown in Figure 2.1(a), in which the PMOS transistors $P_{1,2}$ are operated in the triode region as a resistor R_{load}, as shown in Figure 2.1(b), will be analyzed as an example through a new method in this chapter.



(a) (b)

Figure 2.1 (a) Schematic of a basic differential delay stage and (b) the equivalent circuit of (a). $C_{p1,2}$ are parasitic capacitors at corresponding nodes.

In this chapter, oscillation frequency and waveform amplitude equations are derived under steady state conditions. The validity and accuracy of equations derived with this method are verified through comparisons with Cadence Spectre simulated results and experimental data [2.14], and they can describe the nonlinear dependence of amplitude and frequency on design parameters. This chapter is organized in five sections. Section II presents the nonlinear dependence of waveform amplitude and oscillation frequency on design parameters in high frequency ring oscillation design. The derivation of new oscillation amplitude and frequency equations is described in Section III. Section IV is the verification of the equations obtained in Section III. Section IV concludes this work.

II. NONLINEARITY IN HIGH FREQUENCY RO

The oscillation amplitude V_p is often calculated with [2.6], [2.9]:

$$V_p = I_{ss} R_{load} / 2 , \tag{2.1}$$

which shows that V_p is only controlled by R_{load} and tail current I_{ss}. The V_p and delay time per stage t_d variation versus stage number N can be defined as (2.2a) and (2.2b), when the tail current, R_{load}, VDD, and MOS transistor sizes are fixed.

$$V_p \text{ var} \mathit{iation\ ratio} = \frac{V_{p,N} - V_{p,N=3}}{V_{p,N=3}} , \tag{2.2a}$$

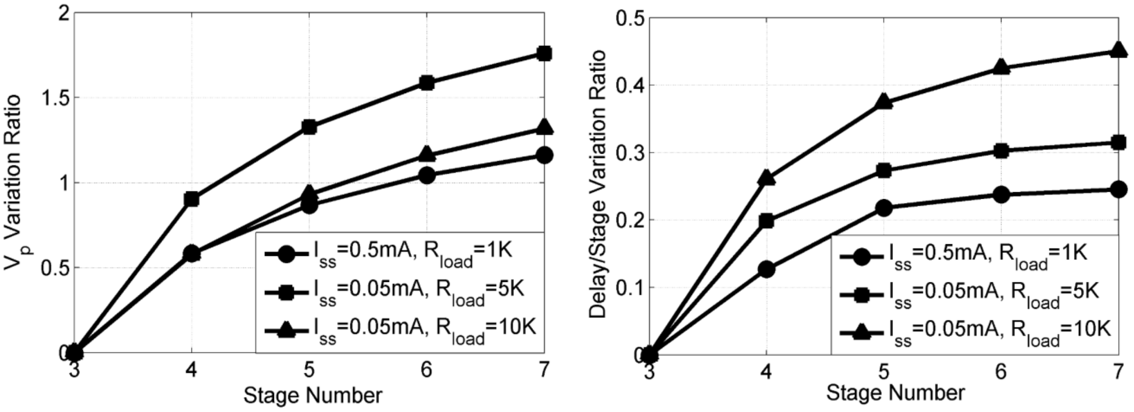
$$t_d \text{ var} \mathit{iation\ ratio} = \frac{t_{d,N} - t_{d,N=3}}{t_{d,N=3}} . \tag{2.2b}$$

According to the simulated results shown in Figure 2.2(a), the assumption in (2.1) that V_p is independent of frequency and stage number is far from accurate. Thus, this independence needs further examination. Theoretically, the oscillation amplitude of a ring oscillator changes with the operating frequencies for different charge or discharge levels of the parasitic capacitors. There may be enough time to fully charge (or discharge) the parasitic capacitors at a low frequency while there is not enough time at a high frequency. Different number of delay stages yields different output amplitudes for different oscillating frequencies.

For an N-stage ring oscillator, the often used frequency's estimation equation is [2.8]-[2.9]

$$f = 1/(2 \cdot N \cdot t_d), \tag{2.3}$$

in which the propagation delay per stage t_d, obtained by assuming that the current I_{ss} charges and discharge the parasitic capacitor C_p is $2 \cdot \ln 2 \cdot C_pV_p/I_{ss}$, will not be affected by N. However, Figure 2.2(b) shows large t_d variation with the varying of N. Simulated and measured results also show that oscillation frequency depends on I_{ss} nonlinearly [2.11]-[2.12]. More accurate frequency estimations were achieved by considering the time-varying parasitic capacitance, C_p, and gate resistance [2.12]-[2.13]. However V_p must first be determined. Furthermore, there are no discussions about the nonlinear dependence of the transistors' dimension [2.13].



(a) (b)

Figure 2.2 Simulated results of (a) V_p variation ratio versus stage number N, (b) Delay time per stage variation ratio versus stage number N with N=3 as reference. The transistor size of $N_{1,2}$ is W/L= 6.5 µm / 0.12 µm.

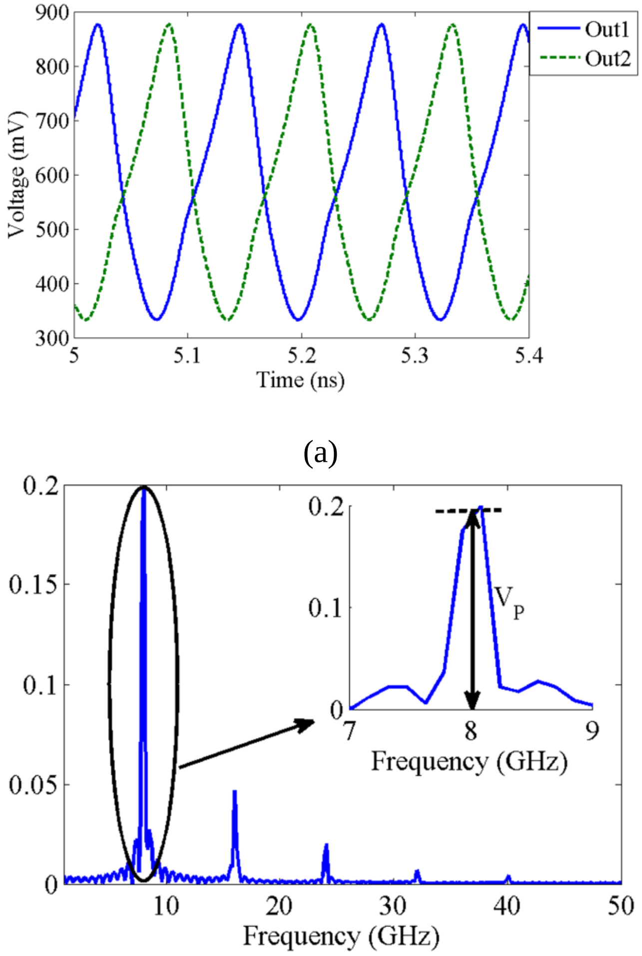
In Section III, we will propose a new platform to derive some simple equations, which can describe those nonlinearities in high frequency RO.

III. DERIVATION OF OSCILLATION AMPLITUDE, FREQUENCY

Figure 2.3(a) shows the simulated waveforms of a 3-stage ring oscillator with Figure 2.1(b) as the delay cell, and the corresponding spectrum of the output waves. Figure 2.3(b) shows that the power of the fundamental frequency, 8 GHz, is much larger than those of the 2nd or higher order harmonic components. That is the reason that the output waves can be assumed as sinusoidal waves in [2.3]-[2.5] [2.11]-[2.12]. The enlarged figure of the spectrum around the 8 GHz shows the nearby frequency has considerable power, in other words, there is phase noise. So according to the spectrum in Figure 2.3(b), the output wave can be assumed to be:

$$\begin{matrix} V_1 = V_0 + V_p \cos(\omega t + \Phi(t)) \\ V_{1o} = V_0 + V_p \cos(\omega t + \Phi(t) - \theta) \end{matrix}, \quad \begin{matrix} V_2 = V_0 - V_p \cos(\omega t + \Phi(t)) \\ V_{2o} = V_0 - V_p \cos(\omega t + \Phi(t) - \theta) \end{matrix}, \tag{2.4}$$

where V_0 is the DC bias, V_p is the oscillation amplitude, $\omega = 2\pi f$ and f is the oscillation frequency, $\theta=\pi(1+1/N)$ is the phase delay per stage and $\Phi(t)$ is the phase (To simplify the derivation, $\Phi(t)$ can be assumed to 0). Unlike the assumption in [2.11]-[2.12], both f and V_p are unknown parameters to be determined.



(a)

(b)

Figure 2.3 (a) Transient simulation results, (b) Partial DFT of the output wave with 5000GHz sampling frequency of a 3-stage ring oscillator. R_{load}=5K, I_{ss}=0.25mA, the transistor size of $N_{1,2}$ is W/L= 6.5 μm/0.12 μm.

We assume that transistors $N_{1,2}$ in Fig. 2.1 always operate in the saturation region even though they may enter the triode or cutoff region some time in a period, especially when V_p is large. To simplify the analysis, we will first use the long-channel drain current model in the derivations and then modify the final results to include velocity saturation effects in deep submicron transistors.

Applying the KCL at the common source node in Fig. 2.1(b), we have

$$I_{ss} = I_{ds1} + I_{ds2} \text{ and } I_{ds1,2} = \frac{\mu C_{ox}}{2}\frac{W_{1,2}}{L_{1,2}}(V_{1,2} - V_{ss} - V_{th})^2, \tag{2.5}$$

where $W_{1,2}$ and $L_{1,2}$ are the width and length of $N_{1,2}$, V_{ss} is the voltage at the common source node, μ is the charge carrier mobility and C_{ox} is the gate capacitance per unit area.

The voltage at the common source node is obtained from (2.5) as

$$V_{ss} = V_0 - V_{th} - \sqrt{\frac{I_{ss}}{2K_{1,2}} - V_p^2 \cos^2(\omega t)}, \tag{2.6}$$

where $K_{1,2}=\mu\ C_{ox} \cdot W_{1,2}/(2 \cdot L_{1,2})$.

To keep (2.6) valid, the term under the square root sign should be positive.

$$V_p \le \sqrt{\frac{I_{ss}}{2K_{1,2}}} \tag{2.7}$$

The frequency of V_{ss} is about two times the frequency of $V_{1,2}$ and also a source of 2nd order harmonic waves. Use the KCL at the output node,

$$\frac{VDD - V_{o1}}{R_{load}} = C_p \frac{d}{dt}(V_{o1}) + K_{1,2}(V_0 + V_p \cos(\omega t) - V_{ss} - V_{th})^2 \cdot \tag{2.8}$$

Putting (2.4) and (2.6) into (2.8) and rearranging, we have,

$$\begin{aligned}\frac{VDD - V_0}{R_{load}} - \frac{I_{ss}}{2} = {} & \frac{V_p}{R_{load}}\cos(\omega t - \theta) - C_p V_p \omega \sin(\omega t - \theta) \\ & + 2K_{1,2}V_p \cos(\omega t)\sqrt{\frac{I_{ss}}{2K_{1,2}} - V_p^2 \cos^2(\omega t)}\end{aligned} \; . \tag{2.9}$$

Integrating (2.9) over a period, the DC bias voltage can be obtained as

$$V_0 = VDD - R_{load}\frac{I_{ss}}{2}\cdot \tag{2.10}$$

Then (2.9) can be simplified as

$$C_p\omega\sin(\omega t-\theta)-\frac{\cos(\omega t-\theta)}{R_{load}} = 2K_{1,2}\cos(\omega t)\sqrt{\frac{I_{ss}}{2K_{1,2}}-V_p^2\cos^2(\omega t)}\cdot \tag{2.11}$$

Squaring (2.11), we obtain

$$\begin{aligned}&\frac{(\omega C_p)^2}{2}+\frac{1}{2R_{load}^2}-I_{ss}K_{12}+\frac{3}{2}K_{12}^2V_p^2\\&=(K_{1,2}I_{ss}-2K_{1,2}^2V_p^2)\cos(2\omega t)-\frac{1}{2}K_{1,2}^2V_p^2\cos(4\omega t)\\&+(\frac{(\omega C_p)^2}{2}-\frac{1}{2R_{load}^2})\cos(2(\omega t-\theta))+\frac{\omega C_p}{R_{load}}\sin(2(\omega t-\theta))\end{aligned}\quad . \tag{2.12}$$

Integrating (2.12), V_p can be obtained as

$$V_p = \sqrt{\frac{2}{3}(\frac{I_{ss}}{K_{1,2}}-(\frac{(2\pi f\ C_p)^2}{2K_{1,2}^2}+\frac{1}{2K_{1,2}^2R_{load}^2}))}\cdot \tag{2.13}$$

This equation clearly shows that V_p dependents on f as discussion in Section II. The term under the square root sign in (2.13) should be positive as well. The oscillation frequency range is thus determined by

$$f_{\min}=\frac{\sqrt{\frac{I_{ss}K_{1,2}}{2}-\frac{1}{R_{load}^2}}}{2\pi C_p}\le f\le\frac{\sqrt{2I_{ss}K_{1,2}-\frac{1}{R_{load}^2}}}{2\pi C_p}=f_{\max}, \tag{2.14}$$

which indicates that the tuning range of the oscillator increases when R_{load} increases. The maximum value of (f_{max} - f_{min}) / f_{min} approaches 1 when I_{ss} varies. By combining (2.12) and (2.13), the following equation is obtained

$$\begin{aligned}&(\frac{2}{3}(\omega C_p)^2 + \frac{2}{3R_{load}^2} - \frac{1}{3}K_{1,2}I_{ss})\cos(2\omega t)\\ &+(\frac{1}{6}(\omega C_p)^2 + \frac{1}{6R_{load}^2} - \frac{1}{3}K_{1,2}I_{ss})\cos(4\omega t)\\ &+(\frac{(\omega C_p)^2}{2} - \frac{1}{2R_{load}^2})\cos(2\omega t - 2\theta) + \frac{\omega C_p}{R_{load}}\sin(2\omega t - 2\theta) = 0\end{aligned} \quad . \qquad (2.15)$$

The integration of (2.15) over a full period is zero. An accurate method for obtaining ω is to conduct an eight piecewise-integration and find the average values of ω from (2.15). However, this method is quite tedious. We use the first order cosine power series expression to obtain the following frequency equation,

$$f = \frac{\frac{\sin(2\theta)}{R_{load}} + \sqrt{\frac{K_{12}I_{ss}}{9}(20 + 12\cos(2\theta)) - \frac{16}{9R_{load}^2}}}{2\pi C_p(\frac{5}{3} + \cos(2\theta))} . \qquad (2.16)$$

Equation (2.16) closely approximates the piecewise-integration approach according to our analysis. From (2.16), the relationship between oscillation frequency and transistor $N_{1,2}$ size (W/L ratio) can be approximated as

$$f \propto \sqrt{\frac{1}{W/L}} . \qquad (2.17)$$

Equations (2.16) and (2.17) are valid for circuits designed with long channel transistors. While in deep submicron technology, velocity saturation effect should be taken into account, the drain-source current of $N_{1,2}$ is [2.14]

$$I'_{ds1,2} \approx \frac{I_{ds1,2}}{1 + \frac{V_{GST1,2}}{E_c L}} , \qquad (2.18)$$

where $V_{GST1,2} = V_{1,2} - V_{ss} - V_{th} \approx \sqrt{\frac{I_{ss}}{2K_{1,2}}}$ and $E_c = \frac{2\upsilon_{sat}}{\mu}$.

Then $K_{1,2}$ in (2.13), (2.14), and (2.16) should be revised to:

$$K_{new} = \frac{K_{12}}{1+\sqrt{I_{ss}/2K_{1,2}}/(E_c L)}. \tag{2.19}$$

IV. VERIFICATION OF DERIVED EQUATIONS

A test bench, based upon CMOS 0.13 μm technology, was set up to verify the validity of (2.13), (2.14), (2.16), (2.17), and (2.19). VDD is 1.2 V. The parameters used in the following calculation are $\gamma = 2.5$, $F = 6e^{-15}$ C, T = 300 K, $\upsilon_{sat} = 1.93e^{6}$ m/s. When comparing the simulated and calculated V_p versus I_{ss} and N, a factor of ×2 is needed to compensate the calculation values from (2.13) for the initial assumption of a purely sinusoidal waveform. Fig. 2.4 compares the estimated V_p from (2.13) and simulated values for different I_{ss} when R_{load} is 5 kΩ and the stage number varies from 3 to 7. As N increases and other conditions remain the same, V_p increases as discussion in Section II since there is more time to charge and discharge C_p. Nevertheless, V_p does not increase linearly with I_{ss} as estimated by (2.1). Analytical results by (2.13) are close to the simulated results. Define the estimation errors as

$$error\ ratio = \frac{|simu.\,value - equation\ value|}{simu.\,value}. \tag{2.20}$$

The maximum error by (2.13) is about 6% as shown in Fig 3 when R_{load}= 5K, while the error for (2.1) is approximately 50%.

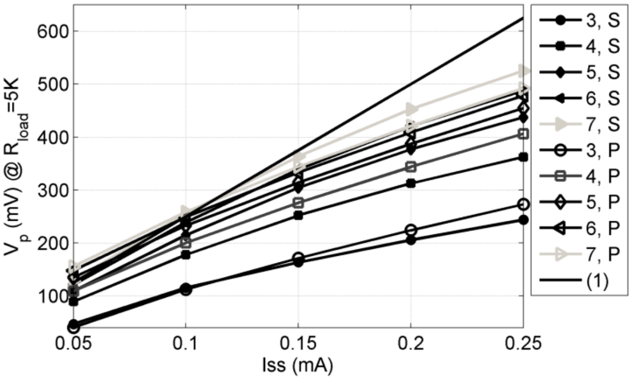


Figure 2.4 Comparison of simulated and calculated results with (2.13) and (2.1). Five different stage numbers are considered when R_{load}= 5 K and the transistor size of $N_{1,2}$ is W/L= 6.5 µm/0.12 µm. “S” and “P” indicate simulated and predicted results respectively.

Table I presents the measurement data from [2.13] and m is the transistor multiplicity factor with respect to the first transistor in table I. f_0=4.47 GHz is the reference frequency. Table I shows that (2.17) yields a good estimation of the relationship between frequency and transistor size.

TABLE 2.1

OSCILLATION FREQUENCY VS. W/L [2.14].

W/L (µm/µm)	m	R_{load} (Ω)	I_{ss}	f GHz	f_0 / m GHz	$f_0 / \sqrt{m}$ GHz
8.4/0.25	1	1K	1mA	4.47	4.47	4.47
16.8/0.25	2	1K	1mA	3.39	2.235	3.161
33.6/0.25	4	1K	1mA	2.24	1.1175	2.235
67.2/0.25	8	1K	1mA	1.19	0.559	0.873

Fig. 2.5 compares the relationship between frequency and W/L ratio of transistors $N_{1,2}$ from simulated and calculated results. It shows that the results from (2.16) and (2.19) agree with simulated results reasonable well as W/L increases by a factor of 6 and the tail current is tuned from 0.05 mA to 0.30 mA.

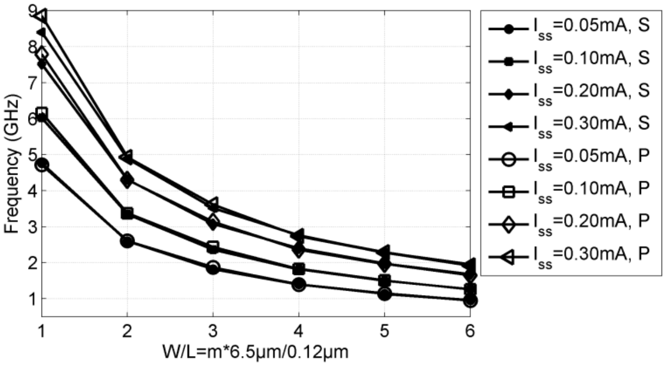
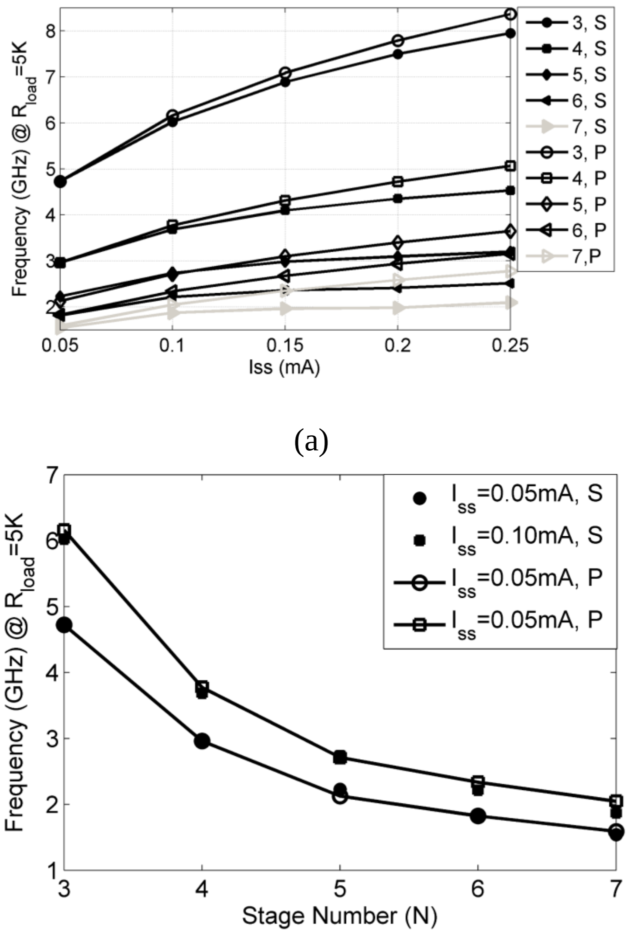
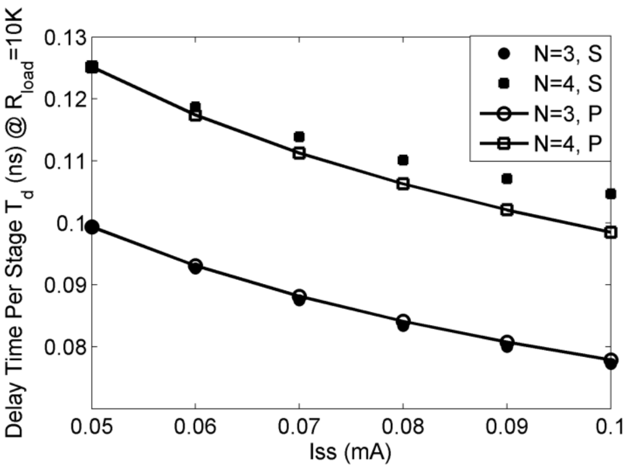


Figure 2.5 The comparison of simulated and calculated results with (2.16) and (2.19) for 6 different W/L ratios. “S” and “P” indicate simulated and predicted results, respectively.



(a)

(b)



(c)

Figure 2.6 Comparison of simulated and calculated results using (2.16) and (2.19) at 5 different stage number 3-7: (a) Oscillation frequency f versus I_{ss} when R_{load}= 5 K and (b) Frequency versus N when R_{load} = 5 K. (c) Delay time per stage td versus I_{ss} when R_{load}=10 K. The transistor size of $N_{1,2}$ is W/L= 6.5 µm / 0.12 µm. “S” and “P” indicate simulated and predicted results respectively.

Fig. 2.6(a) presents the comparison of frequency f versus tail current I_{ss} at 5 different stage numbers from simulated and calculated results with (2.16) and (2.19). Fig. 2.6(a) also shows that frequency f is not a linear relationship with I_{ss}. Fig. 2.6(b) is the frequency f versus stage numbers N and Fig. 2.6(c) is the delay per stage t_d versus I_{ss} at different stage number N. In Fig 2.6(a) and (c), for smaller I_{ss}, theoretical predictions agree with the simulated results very well, but the discrepancies grow larger when I_{ss} becomes larger. Larger I_{ss} means larger V_p, and then there are more harmonic frequencies components which is probably the reason of large discrepancies. In Fig. 2.6(c), t_d is seriously affected by N as predicted by the analysis in Section II. Regardless, our prediction curves in Fig. 2.6 closely approximate the simulation curves. When V_p is given, according to the experiments in [2.11]-[2.12], the prediction error of frequency with (2.2) is up to about 85%, (26) in [2.11] yields about 30% errors while (16) in [2.12] have about 8%, while our prediction error is about 10% without knowing V_p.

Furthermore, the frequency tuning range of a ring oscillator can also be determined. The measurement results in [2.14], shown in Table II, verified that the tuning range increases when R_{load} increases as the prediction in (2.14). Fig. 2.6(a) also shows that the maximum value of $(f_{max} - f_{min})/ f_{min} \approx 1$ while I_{ss} varies as predicted by (2.14).

TABLE 2.2
THE FREQUENCY TUNING RANGE VS. R_{LOAD} [2.14]

W/L (μm/μm)	R_{load} (Ω)	Tuning Range
33.6/0.25	250	25%
33.6/0.25	500	32%
33.6/0.25	1K	58%
33.6/0.25	2K	67%

The analytical equations for the oscillation amplitude and frequency of a differential ring oscillator in deep submicron technology were presented in this chapter. The equations derived with this new method are verified through the simulated and with experimental data from literature. These new equations describe the nonlinear dependence of oscillation amplitude and frequency on the number of stage, and on transistor sizes. The equations in this chapter can help designers make tradeoffs among phase noise performance, power dissipation, and chip area.

V. CONCLUSION

The analytical equations for the oscillation amplitude and frequency of a differential ring oscillator in deep submicron technology are presented in this chapter.

The equations derived with this new method are verified through the simulated and with experimental data from literature. These new equations describe the nonlinear dependence of oscillation amplitude and frequency on the number of stage, and on transistor sizes, load resistors, and on tail current. Compared with currently available expressions, the obtained equations show significantly improved accuracies. Therefore, they can be used to guide the differential oscillator design. For other ring oscillation topologies, such as single ended ring oscillators, corresponding equations can also be derived with this new method.

REFERENCES

[2.1] Kadaba R. Lakshmikumar, "Analog PLL Design with Ring Oscillators at Low-Gigahertz Frequencies in Nanometer CMOS: Challenges and Solutions," IEEE Trans. on Circuits and Systems-II: Express Briefs, Vol. 56, No. 5, May 2009.

[2.2] Zhinian Shu, Ka Lok Lee, Bosco H. Leung, "A 2.4-GHz Ring-Oscillator-Based CMOS Frequency Synthesizer with a Fractional Divider Dual-PLL Architecture," IEEE Journal of Solid-State Circuits, Vol. 39, No. 3, March 2004.

[2.3] Jafar Savoj, Behzad Razavi, "A 10-Gb/s CMOS Clock and Data Recovery Circuit with a Half-Rate Linear Phase Detector," IEEE Journal of Solid-State Circuits, Vol. 36, No. 5, May 2001.

[2.4] Bassem Fahs, Walid Y. Ali-Ahmad, Patrice Gamand, "A Two-Stage Ring Oscillator in 0.13-μm CMOS for UWB Impulse Radio," IEEE Trans. on Microwave Theory and Techniques, Vol. 57, No. 5, May 2009.

[2.5] Behzad Razavi, “A Study of Phase Noise in CMOS Oscillators,” IEEE Journal of Solid-State Circuits, Vol. 31, No. 3, March 1996.

[2.6] Todd Charles Weigandt, “Low-Phase-Noise, Low-Timing-Jitter Design Techniques for Delay Cell Based VCOs and Frequency Synthesizers,” PhD. Dissertation, Univ. California, Berkeley, 1998.

[2.7] Ali Hajimiri, Thomas H. Lee, “A General Theory of Phase Noise in Electrical Oscillators,” IEEE Journal of Solid-State Circuits, Vol. 33, NO. 2, February 1998.

[2.8] Shweta Srivastava, Jaijeet Roychowdhury, “Analytical Equations for Nonlinear Phase Errors and Jitter in Ring Oscillators,” IEEE Trans. on Circuits and Systems-I: Regular Papers, Vol. 54, No. 10, October 2007.

[2.9] Asad A. Abidi, “Phase Noise and Jitter in CMOS Ring Oscillators.” IEEE Journal of Solid-State Circuits, Vol. 41, No. 8, August 2006.

[2.10] Behzad Razavi, “Design of Analog CMOS Integrated Circuits,” McGraw-Hill Higher Education, 2001.

[2.11] Bosco H. Leung, “VLSI for Wireless Communication,” Upper Saddle River, NJ: Prentice-Hall, 2002.

[2.12] Stephen Docking, Manoj Sachdev, “A Method to Derive an Equation for the Oscillation Frequency of a Ring Oscillator,” IEEE Trans. Circuits and Systems-I: Fundamental Theory and Applications, Vol. 50, No. 2, Feb. 2003.

[2.13] Stephen Docking, Manoj Sachdev, “An Analytical Equation for the Oscillation Frequency of High-Frequency Ring Oscillators,” IEEE Journal of solid-State Circuits, Vol. 39, No. 3, March 2004.

[2.14] Ali Hajimiri, Sotirios Limotyrakis, Thomas H. Lee, "Jitter and Phase Noise in Ring Oscillators," IEEE Journal of Solid-State Circuits, Vol. 34, No. 6, June 1999.

[2.15] Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits, Fourth Edition," John Wiley & Sons, Inc. 2000.

CHAPTER THREE

A LOW-POWER ULTRA-WIDEBAND CMOS POWER DETECTOR WITH AN EMBEDDED AMPLIFIER

Abstract— A self-biased, low-power CMOS power detector (PD) is proposed and demonstrated in this chapter. The detector utilizes the nonlinear characteristics of short-channel MOS devices operating in either saturation or subthreshold regime to generate a DC current proportional to the input radio-frequency (RF) signal power. The operating regimes of MOS devices depend on the input RF power levels. A quasi T-coil matching network providing a 50 Ω matching from 0.5 GHz to 20 GHz is designed and analyzed. An embedded amplifier is added to enhance the sensitivity of the PD when the input power level is low. The circuit implemented in a 0.13 μm CMOS process occupies an active area of 0.085 mm^2. In the matched frequency range, the measured input dynamic range is 47 dB with an overall sensitivity of 26.8 mV/dB. The output DC voltage response is nearly frequency independent in the linear operating range, varying by less than 1.9 dB for a given input RF power level as the RF frequency is swept across the operating frequency range. With a standard 1.2 V supply, the static power consumption is about 0.1 mW, which decreases to 2×10^{-4} mW with a 0.5 V supply while the operating frequency remains unchanged.

Index Terms— CMOS, dynamic range, low power, low voltage, nonlinearity, power detectors, ultra-wideband.

I. INTRODUCTION

Signal power detectors are widely used in wireless communication systems, which often use automatic-gain-control (AGC) circuits to minimize power consumption and to optimize system performance [3.1]-[3.2]. The activation of AGCs is determined by the received or transmitted signal levels obtained from PDs. Power detection is also essential in the six-port system shown in Fig. 3.1, which has been developed for reflectometer and communication receiver applications [3.3]-[3.7]. For a six-port measurement system, when a load (i.e. device under test, DUT) is connected to port 2, its complex reflection coefficient can be determined by power readings at the measurement ports 3-6. For communication receivers, the received signal is connected to port 2. The modulation states of the received signals are determined by the power information from power measurement ports 3-6. These PDs require wideband operations, e.g. in six-port broadband impedance spectroscopy or ultra-wide-band communication (UWB, 3.1GHz - 10.6 GHz) applications.

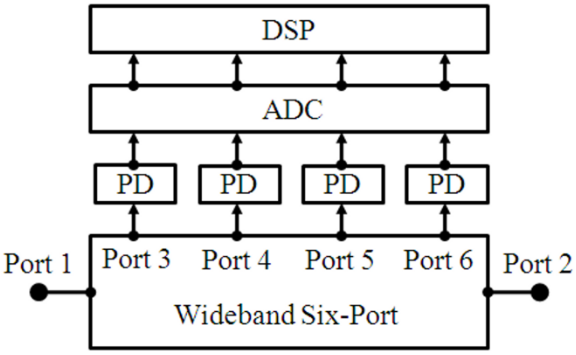


Figure 3.1 Schematic of a six-port for communication or measurement system.

There are several methods to implement on-chip PDs, such as Schottky diode detectors, Joules-heating-based detectors, bipolar and CMOS detectors. Among those candidates, Schottky diode detectors are good for RF signal detection. However, Schottky diodes are not standard components in CMOS foundry processes. Their performance depends on the process technologies provided by the foundries [3.8]. Joules-heating-based detectors require special attention to packaging, which prevent them from wide applications. Many efforts are also underway to develop bipolar transistor (BJT) power detectors [3.9]-[3.10]. However, these are incompatible with CMOS processes which are frequently used to fabricate other system parts. Though a PD based on MOS transistors operating in the deep triode regime has been demonstrated [3.11], the use of a resonant cavity limits the techniques to narrowband operations, and it is not amenable to integration. Using the square-law nature of MOS transistors' I_D-V_{GS} characteristics, the PD in [3.12] achieved a 20 dB input dynamic range from 0.125 GHz to 8.5 GHz, but multiple off-chip matching networks were used. Recently, a PD with NMOS devices operating in the triode regime was proposed [3.13]. An average current proportional to the RF input power level was generated and then was converted to voltage, which was then amplified with a piecewise linear logarithmic amplifier. The PD achieved an operating frequency range from 3.1 GHz to 10.6 GHz with an approximate 35 dB input dynamic range. The maximum detectable input power was approximately -10 dBm.

Most of the recent PD research focused on the AGC applications, which require low level power detections and low power consumption. However, for the six-port system in Fig. 3.1, the power level in each power measurement port can vary significantly due to load conditions in six-port measurement systems or signal modulation conditions in communications systems. The minimum input power in a power measurement port is close to 0, while the maximum power is close to the input power at port 1, which may be 5 dBm with a standard 1.2 V power supply. Therefore, larger input dynamic ranges compared with those reported PDs in [3.11]-[3.13] are desired. Furthermore, the outputs of PDs in a six-port circuit are expected to only respond to the incident waves in analyzing the q-point distribution, which determines the accuracy of a six-port circuit [3.3]-[3.5]. Therefore, PDs with large input matching frequency range can simplify the circuit analysis and facilitate the circuit design.

In addition, the output DC voltages of ideal PDs are expected to only respond to the input signal power levels. In other words, it should be independent of frequencies. However, in non-matching circuits, the reflection coefficients of PDs vary with the change of the input signal frequencies in wideband applications, as do the PDs' effective input RF power levels. Thus, the output DC voltage changes significantly as do the variation of input frequencies. The input matching networks of PDs can flatten the ratio between the effective input power of PD and the incident wave versus frequency, so the output DC voltage may remain constant for incident signals with a fixed RF power value. However, no RF power detector with ultra wideband on-chip matching networks has ever been reported as to the authors' best knowledge. In this work, a self-biased, low-power PD with an embedded amplifier is proposed and demonstrated for the first time with an on chip quasi T-coil matching circuit which provides input matching from 0.5 GHz to about 20 GHz. The MOS transistors in the self-biased structure operate in either saturation or subthreshold regime depending upon the input RF power levels. As a result, the input dynamic range is expanded. The embedded amplifier is used here to enhance the sensitivity of the PD at low input power levels. The PD reuses biasing currents and minimizes the power consumption.

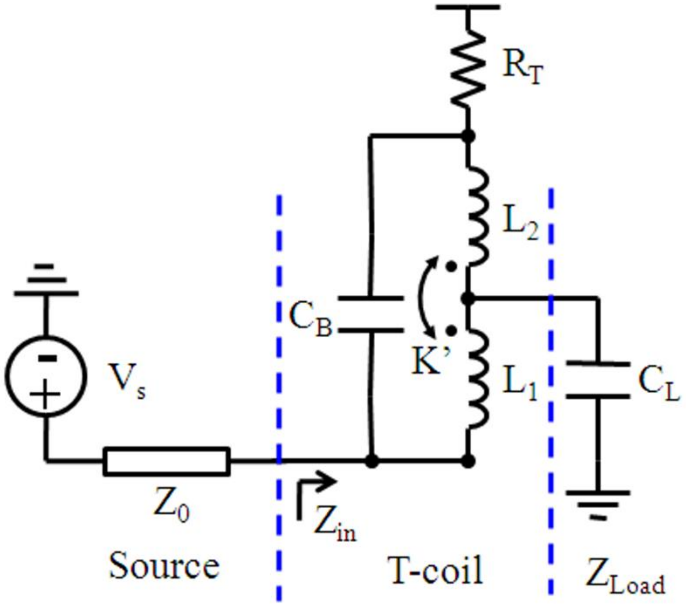
This chapter is arranged as follows. Section II analyzes a new wideband matching network. Section III details the operating principle of the MOS transistor detectors. Section IV presents measurement results and Section V concludes the paper.

II. WIDEBAND MATCHING CIRCUIT

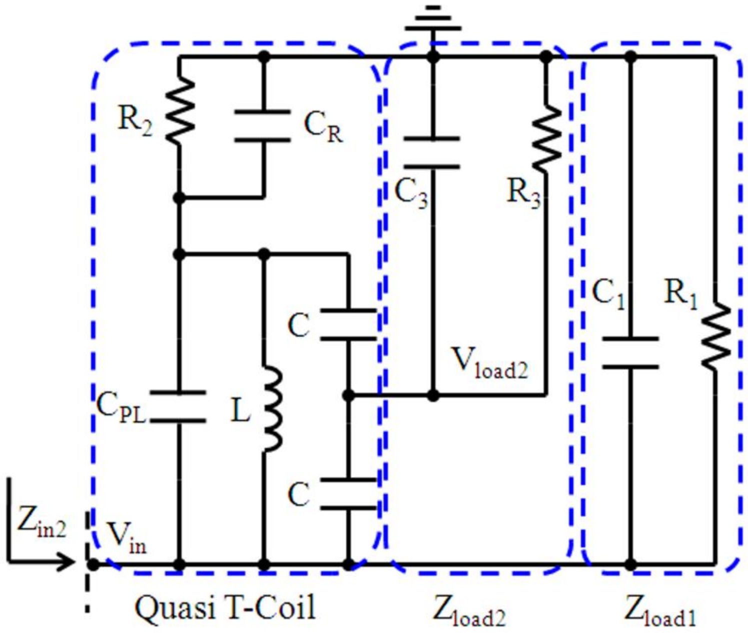
A T-coil structure, shown in Fig. 3.2(a) [3.14]-[3.16], is a possible choice for broadband matching. Here, K' is the mutual inductance between inductor L_1 and L_2. Unfortunately, the T-coil is not a standard CMOS component in commercial foundry processes. Moreover, controlling the performance of a customer designed T-coil is difficult due to the lack of model parameters and also the process variations in a certain foundry process. Furthermore, the following relationship is required for broadband T-coil matching:

$$C_B = \frac{C_L}{16\zeta^2} \tag{3.1}$$

where ζ is the damping factor of the network transfer function and C_L is the load capacitance [3.14]. Part of C_B is from the parasitic capacitance, C_p (not shown), between the two terminals of the transformer. This structure fails when load capacitance C_L is much smaller than the parasitic capacitance C_p. However, to save power consumption in a PD design, the parasitic capacitances of the transistors, which is the load of the matching network, is usually very small, so the T-coil match cannot be used here. To solve this problem, a quasi T-coil matching circuit, shown in Fig. 3.2(b), is proposed. To simplify the analysis, only the parasitic capacitors of resistor R_2 and inductors L are shown and taken into consideration in calculation.



(a)



(b)

Figure 3.2 (a) A T-coil network. (b) Proposed quasi T-coil circuit. C_{PL} and C_R are the parasitic capacitors of L and R_2 respectively.

To design the quasi T-coil matching network for the self-biased power detector, which is shown in Fig. 3.5(b) and discussed in Section III, Z_{load1} is used to represent the gate capacitance of M_1 and the resistance R_1. The gate capacitor of M_3 and resistor R_3 is represented by Z_{laod2}. The matching circuit can be treated as a three-port network, one input port and two output ports. The input port is connected to the signal source, and two output ports are connected to Z_{load1} and Z_{load2} respectively. In other applications with a single load, the load can be added to either Z_{load1} or Z_{load2}. To determine the components' values in the proposed quasi T-coil circuit, a general case is considered in the following analysis. If we assume the source voltage is V_s and resistance is Z_0 as shown in Fig.

3.2(a), then the voltage transfer coefficient from the source to Z_{load1} in Fig. 3.2(b) can be defined as:

$$T_{load1} = \frac{voltage\ on\ Z_{load1}}{incident\ wave\ \ from\ source} = 1 + \Gamma_{in2}\ ,\ V_s = V^+ + V^- . \qquad (3.2)$$
$$\Gamma_{in2} = \frac{V^-}{V^+} = \frac{Z_{in2} - Z_0}{Z_{in2} + Z_0}$$

where V^+ and V^- are the incident and reflected waves at the input interface [3.17]. When input impedance, Z_{in2}, is matched to Z_0, the reflection coefficient Γ_{in2} approaches 0, and then T_{load1} approaches 1 in the matching frequency range.

The relationship of R_2 with the load resistor R_1 and R_3 can be obtained from the condition Re $(Z_{in2}) \approx Z_0$.

$$R_2 \approx \frac{Z_0 R_1}{R_1 - Z_0} \qquad (3.3)$$

in which $R_1 > Z_0$ is required. From Im $(Z_{in2}) \approx 0$ in the matching frequency range, the inductance L can be expressed as follows:

$$L \approx \frac{1}{R_1 - Z_0} \cdot \begin{pmatrix} Z_0 R_2 R_1 (C_R + 2C + C_1) \\ + Z_0 R_3 (R_2 + R_1)(C_3 + 2C) - R_1 R_2 R_3 (C_3 + 2C) \end{pmatrix} . \qquad (3.4)$$

Since the output DC voltage of the PD is proportional to the amplitude of the input RF signals, the voltage transfer ability is important to the sensitivity of the PDs. The voltage transfer coefficient from the source to Z_{load2} can be defined as

$$
\begin{aligned}
A_{load2} &= \frac{V_{in}}{V^{+}} \cdot \frac{V_{load2}}{V_{in}} \\
&= T_{load1} \cdot \frac{sC(\frac{1}{R_2} + sC_R + 2sC_{PL} + \frac{2}{sL} + sC)}{(\frac{1}{R_3} + sC_3 + 2sC)(\frac{1}{R_2} + sC_R + sC_{PL} + \frac{1}{sL} + sC) - (sC)^2}
\end{aligned}
\quad . \tag{3.5}
$$

To guarantee a reasonable voltage transfer coefficient from the source to Z_{load2}, since T_{load1} approaches 1 at the designed center frequency, the capacitor C should satisfy the following equation:

$$
\left| \frac{sC(\frac{1}{R_2} + sC_R + 2sC_{PL} + \frac{2}{sL} + sC)}{(\frac{1}{R_3} + sC_3 + 2sC)(\frac{1}{R_2} + sC_R + sC_{PL} + \frac{1}{sL} + sC) - (sC)^2} \right| \approx \frac{1}{2} \, . \tag{3.6}
$$

Thus, all parameters in the quasi T-coil structure in Fig. 3.2(b) can be determined.

To match the power detector discussed in Fig. 3.5(b), the following parameters are chosen: $R_1 = R_2 = R_3 = 104\ \Omega$, L = 0.894 nH, $C_{PL} = 0.7$ pF, C= 60 fF, $C_1 = 1$ fF, $C_3 = 7.5$ fF, $C_R = 0.16$ fF. The calculated and simulated voltage transfer coefficients with Spectre from the source to Z_{load2} are given in Fig. 3.3. Under matched conditions, the transfer coefficient equals the voltage gain, i.e. $V_{load2}/V_{in} = V_{load2}/V_{+}$. Fig. 3.3 shows that the simulated results agree with the calculated results reasonably. At the design center frequency, 10 GHz, $|A_{load2}|$ is close to 0.5. When the frequency is higher than 15 GHz, the Q factors of the capacitors and inductors decrease, thus the voltage transfer coefficients from the simulation does not increase as indicated in the calculation.

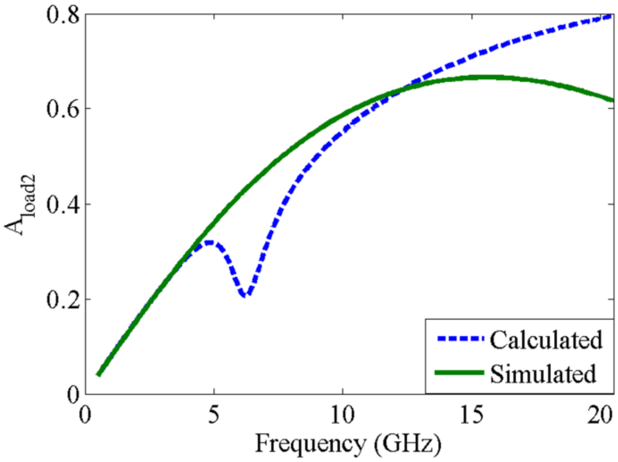
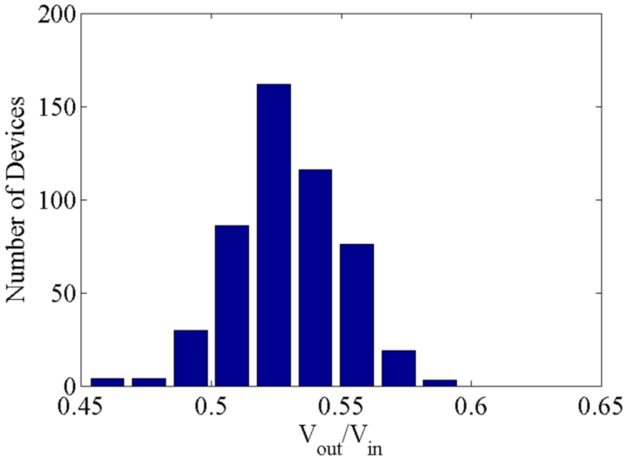
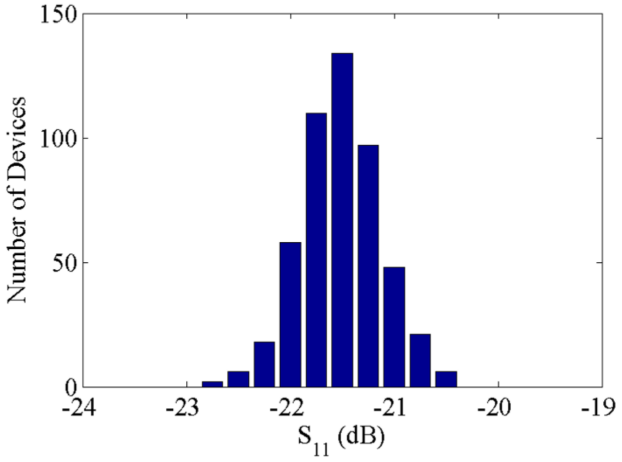


Figure 3.3 Calculated and simulated voltage transfer coefficients from the source to Z_{load2} in Figure 3.2(b).



(a)



(b)

Figure 3.4 Monte Carlo simulation depicting the process variations and the parameters mismatch effects on (a) the voltage transfer coefficients from the source to Z_{load2}, (b) input matching s-parameter S_{11} of the proposed quasi T-coil matching network for a 10 GHz sinusoidal input across 500 runs.

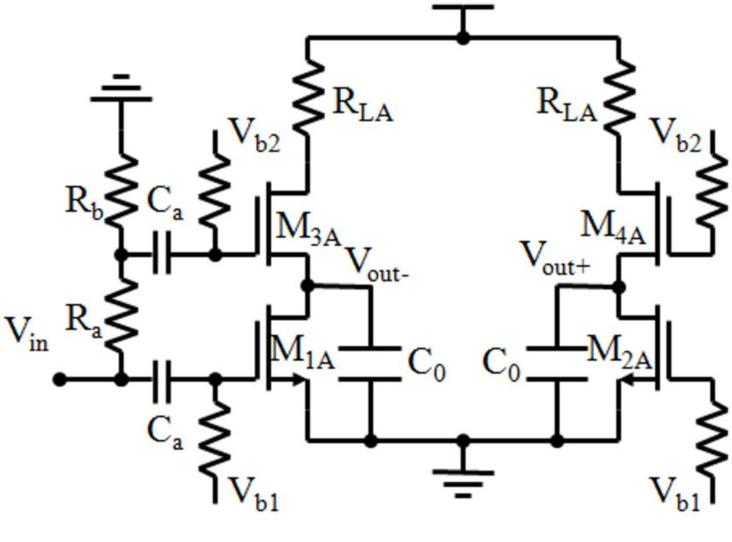
As shown in Fig. 3.3, the voltage transfer coefficient from the source to Z_{load2} is poor at low frequencies (i.e.500 MHz). This is due to the large impedance caused by the capacitor C. It is also opposite to that of the T-coil matching structure in Fig. 3.2(a), which exhibits poor voltage transfer characteristics at high frequency ranges. Thus the important load (such as M_1 and R_1 in Fig. 3.5(b)) should be treated as Z_{load1}, since the voltage transfer coefficient from the source to Z_{load1} is reasonably constant in the operating frequency range.

To demonstrate the effects of the process variations and the parameters mismatch on the input matching s-parameter S_{11} and voltage transfer coefficient from the source to Z_{load2}, a series of simulations was run. Fig. 3.4 shows the output generated by the Monte Carlo analysis in Cadence across 500 runs for the quasi T-coil network when the input frequency is 10 GHz. Fig. 3.4(a) shows the distribution of voltage transfer coefficients from the source to Z_{load2}, the mean of the response is 0.53 V/V with a standard deviation of 0.021 V/V. Fig. 3.4(b) shows the s-parameter S_{11}, where the mean is -21.52 dB and the standard deviation is 0.39 dB. Therefore, the variations of voltage transfer coefficient and S_{11} are small.

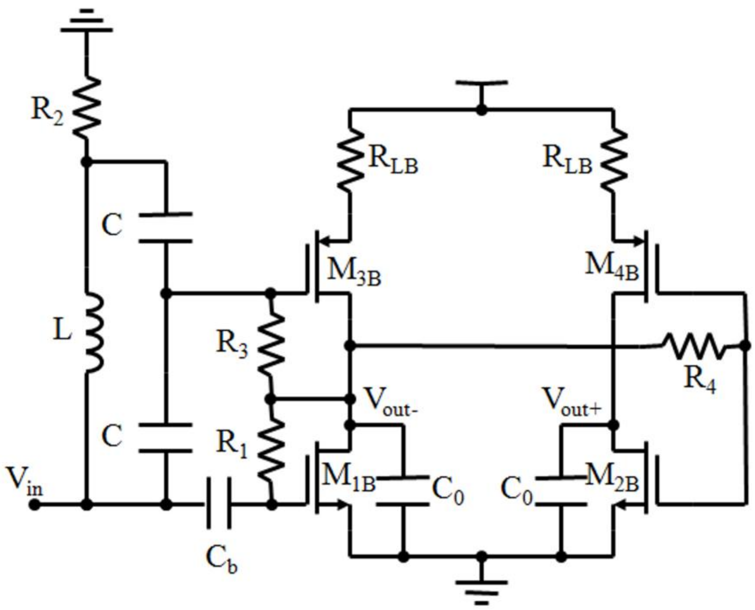
III. POWER DETECTOR DESIGN

Fig. 3.5 shows two power detectors configured for RF power detection. The shared drain/source of MOS transistors M_{1A} and M_{3A}, and of MOS transistors M_{2A} and M_{4A} are AC grounded by capacitors C_0. Fig. 3.5(a) is a power detector matched with resistors, the NMOS transistor M_{1A} acts as the main contributor of the DC current which is proportional to the input RF power level, M_{3A} (can be N or P type) acts in a similar function but as an auxiliary transistor and active load resistor to improve the output sensitivity. This circuit is mainly used for comparison with the proposed self-biased power detector matched with the quasi T-coil network discussed in Section II. The NMOS transistor M_{1B} in Fig. 3.5(b) is also the main generator of the DC current proportional to the input RF power level. PMOS transistor M_{3B} is also used as the auxiliary transistor and active load resistor. Since transistor M_{1B} is the critical transistor, it is connected as the Z_{load1} in the quasi T-coil matching network. M_{3B} and R_3 are treated as the Z_{laod2}. An amplifier comprised of M_{2B} and M_{4B} is embedded to enhance the sensitivity of the power detector at the low input power level. Compared to Fig. 3.5(a), the introduction of amplifier does not increase its DC power consumption.

In Fig. 3.5(b), when there are no RF signals, and if the secondary effects of MOS devices are ignored, MOS transistors M_{1B}, M_{2B}, M_{3B}, and M_{4B} are all operated in the saturation regime and the output voltage (V_{out+}-V_{out-}) is zero since the PD is symmetric in DC operation. For a very low level RF power input, V_{out-} shows a small decrease. Though it is difficult to detect the decrease directly, the embedded amplifier boosts the output voltage (V_{out+} -V_{out-}) and improves the sensitivity of the PD. As the input power level further increases, V_{out-} will decrease significantly, while V_{out+} will increase until it reaches V_{dd}. Then M_{1B} will enter the subthreshold regime when $V_{out-} < V_{th, M1}$, where $V_{th, M1B}$ is the threshold voltage of the MOS transistors. Thus, the power detector can operate at both very low and very high input power levels. In this structure, the DC currents through the transistors are very small. Particularly, when transistors operate in the subthreshold regime, the DC power consumption is reduced dramatically compared with that of the circuit shown in Fig. 3.5(a). Thus another advantage of the embedded amplifier is to decrease the DC power consumption.



(a)



(b)

Figure 3.5 (a) A power detector matched with resistors. (b) The proposed self-biased power detector with quasi T-coil matching network and an embedded amplifier. C_b is a DC isolation capacitor.

The operation principle of a CMOS power detector has been discussed in [3.12] with a long channel transistor model, but the results cannot describe the relationship between the sensitivity and the gate DC bias voltage. Since the transistors in the proposed structure may operate in saturation or subthreshold regimes at different input RF power levels, a unified equation to describe the principle of operation and sensitivity of the PD is necessary. For a general two-port system, one can write a Taylor series expansion relating input and output variables, i.e. the gate voltage and the drain current of a short-channel MOS transistor. The drain current versus gate voltage of $M_{1A,\,B}$ in an arbitrary operating regime is then expressed as [3.18]:

$$i_{DS}(V_{OD}+v_{gs}) = A_0 + A_1 v_{gs} + A_2 v_{gs}^2 + \cdots + A_n v_{gs}^n, \tag{3.7}$$

$$A_n = \frac{1}{n!}\frac{\partial^{(n)} i_{DS}(V_{OD}+v_{gs})}{\partial^{(n)} v_{gs}}. \tag{3.8}$$

where V_{OD} is the gate DC overdrive voltage and v_{gs} is the input RF signal. Assume the RF signal $v_{gs} = v_{rf} \cdot \cos(\omega t+\theta)$ where v_{rf} is the amplitude of the input RF signal. When two different RF input signals (any one of them can be zero also), v_{gs1} and v_{gs2}, are sent into a PD independently, the difference of the drain current between them is

$$\begin{aligned}
\Delta i_{DS} &= i_{DS1}(V_{OD}+v_{gs1}) - i_{DS2}(V_{OD}+v_{gs2}) \\
&= \begin{Bmatrix} A_0 + A_1\left(v_{rf1}\cos(\omega_1 t+\theta_1)\right) + A_2\left(v_{rf1}\cos(\omega_1 t+\theta_1)\right)^2 \\ + \cdots + A_n\left(v_{rf1}\cos(\omega_1 t+\theta_1)\right)^n \end{Bmatrix} \\
&\quad - \begin{Bmatrix} A_0 + A_1\left(v_{rf2}\cos(\omega_2 t+\theta_2)\right) + A_2\left(v_{rf2}\cos(\omega_2 t+\theta_2)\right)^2 \\ + \cdots + A_n\left(v_{rf2}\cos(\omega_2 t+\theta_2)\right)^n \end{Bmatrix} \\
&= A_1\left(v_{rf1}\cos(\omega_1 t+\theta_1) - v_{rf2}\cos(\omega_2 t+\theta_2)\right) + \frac{A_2\left(v_{rf1}^2 - v_{rf2}^2\right)}{2} + \\
&\quad \frac{A_2\left(v_{rf1}^2\cos\left(2\omega_1 t+2\theta_1\right) - v_{rf2}^2\cos\left(2\omega_2 t+2\theta_2\right)\right)}{2} \\
&\quad + A_3\left(\left(v_{rf1}\cos(\omega_1 t+\theta_1)\right)^3 - \left(v_{rf2}\cos(\omega_2 t+\theta_2)\right)^3\right) + \cdots
\end{aligned} \quad . \tag{3.9}$$

The difference of DC component in the drain current for the two different RF input signals is

$$\Delta I_{DS} = \frac{A_2\left(v_{rf1}^2 - v_{rf2}^2\right)}{2} + \frac{5}{8}A_4(v_{rf1}^4 - v_{rf2}^4) + \cdots. \tag{3.10}$$

In Figure 3.5, the output DC voltage differences for the two input signals are

$$\begin{cases} Figure\ 5(a): \Delta(V_{out+} - V_{out-}) = \Delta I_{DS,M1A}(R_L + r_{M,3A}) + \Delta I_{DS,M3A}R_{LA} \\ Figure\ 5(b): \Delta(V_{out+} - V_{out-}) = A_V\left(\Delta I_{DS,M1B}(R_L + r_{M,3B}) + \Delta I_{DS,M3B}R_{LB}\right) \end{cases} . \tag{3.11}$$

where $r_{m,3A,B}$ is the channel resistor of $M_{3A,B}$, and A_v is the voltage gain provided by the embedded amplifier. Equation (3.11) shows that $M_{3A,\ B}$ acts as an active load and auxiliary DC current generator. M_{3A} in Fig. 3.5(a) can be either P or N type. However, to construct the amplifier in Fig. 3.5(b) and to keep the structure symmetrical, M_{3B} in Fig. 3.5(b) must be PMOS. The DC output of the PD is a special case when $V_{rf2}=0$ in (3.9)-(3.11). The theoretical analysis of the unknown parameters A_2, $A_4 \cdots$ can be classified into two cases: the velocity saturation regime and the subthreshold regime.

Velocity Saturation Regime

In a short-channel MOS transistor, velocity saturation is the most important secondary effect in the triode and saturation regimes. The drain current including the velocity saturation effect in a short channel transistor can be described as [3.19]:

$$\begin{aligned} i_{DS}(V_{OD}+v_{gs}) &= \frac{\mu C_{ox}}{2}\cdot\frac{W}{L}\cdot x^2\left(1-\frac{x}{2E_cL}+\cdots\right)^2 \\ &= \frac{\mu C_{ox}W}{2L}\cdot x^2\cdot\left(1-\frac{x}{E_cL}+\frac{5}{4}\left(\frac{x}{E_cL}\right)^2-\frac{7}{4}\left(\frac{x}{E_cL}\right)^3+\cdots\right) \end{aligned} . \tag{3.12}$$

$$x = V_{OD}+v_{rf}\cos\left(\omega t+\theta\right). \tag{3.13}$$

where μ is the charge carrier mobility, C_{ox} is the gate-oxide capacitance per unit area, W and L are the width and length of the transistor, respectively, and E_c is the critical electric field. Then the unknown parameters in (3.10) can be obtained from (3.7), (3.8), (3.12), and (3.13) as

$$A_{2,v-sat} = \frac{\mu C_{ox}}{2}\frac{W}{L}\left(1-\frac{3V_{OD}}{E_CL}+\frac{15}{2}\left(\frac{V_{OD}}{E_CL}\right)^2-\frac{35}{2}\left(\frac{V_{OD}}{E_CL}\right)^3+\cdots\right). \tag{3.14}$$

If the higher order (n ≥ 4) terms in (3.10) are ignored, and putting (3.14) into (3.10), the DC current difference of the drain current caused by the two different RF input signals can be determined as

$$\Delta I_{DS,v-sat} = \frac{\mu C_{ox}}{2} \cdot \frac{W}{L} \cdot \frac{\left(v_{rf1}^2 - v_{rf2}^2\right)}{2} \cdot \left(1 - \frac{3V_{OD}}{2E_C L} + \frac{15}{2}\left(\frac{V_{OD}}{E_C L}\right)^2 - \frac{35}{2}\left(\frac{V_{OD}}{E_C L}\right)^3 + \cdots\right) . \quad (3.15)$$

To achieve the maximum sensitivity, (3.15) should be as large as possible when R_{LA} is fixed according to (3.11). In (3.15), when $V_{OD} > E_c \cdot L$, V_{OD} should be as large as possible. To keep the MOS transistor M_{1A} in the saturation regime, we can estimate the range of gate DC bias voltage V_{b1} in Fig. 3.5(a) as

$$V_{b1,\min} = V_{th} < V_{b1} < V_{th} + \frac{1 + \sqrt{1 + 2V_{dd}(R_L + r_{M,3}) \cdot \mu C_{ox} \frac{W}{L}}}{(R_L + r_{M,3}) \cdot \mu C_{ox} \frac{W}{L}} = V_{b1,\max} . \quad (3.16)$$

In the 0.13 μm CMOS process for circuit implementation $V_{th} = 0.45$ V, $\mu \cdot C_{ox} / 2 \approx 297$ uA / V^2. If W / L= 1.3 μm / 0.12 μm, V_{dd} =1.2 V, R_{LA} = 6000 Ω and $r_{M,3}$ is ignored, then $V_{b1,\max}$ = 0.67 V. The measurement results show that the circuit in Fig. 5(a) achieves maximum sensitivity when $V_{b1} \approx 0.6$ V (equal to the case when $r_{M,3}$ equals 8500 Ω).

Subthreshold Regime

When the input power is high enough, and $V_{out-} < V_{th}$, transistor M_{1B} enters the sub-threshold regime. Its drain current can be expressed as [3.19]

$$\begin{aligned} i_{DS}(V_{OD}+v_{gs}) &= I_S \cdot e^{\frac{x}{mKT/q}} \cdot \left(1-\exp\left(-\frac{v_{DS}}{V_T}\right)\right) \\ &\approx I_S \cdot \left(1+\cdot\frac{q\cdot x}{mKT}+\frac{1}{2}\left(\frac{q\cdot x}{mKT}\right)^2+\frac{1}{6}\left(\frac{q\cdot x}{mKT}\right)^3+\cdots\right) \end{aligned} . \tag{3.17}$$

where I_S and m are empirical parameters, K is the Boltzmann constant, T is the temperature, q is the electron charge, and V_T is the threshold voltage. Then A_2 in the subthreshold regime can be obtained from (3.7), (3.8), and (3.17) as

$$A_{2,sub} = I_S\left(\frac{1}{2}\frac{1}{\left(mKT/q\right)^2}+\frac{1}{6}\frac{3V_{OD}}{\left(mKT/q\right)^3}+\cdots\right). \tag{3.18}$$

Equation (3.18) also presents a positive relationship between A_2 and the gate overdrive voltage V_{OD}.

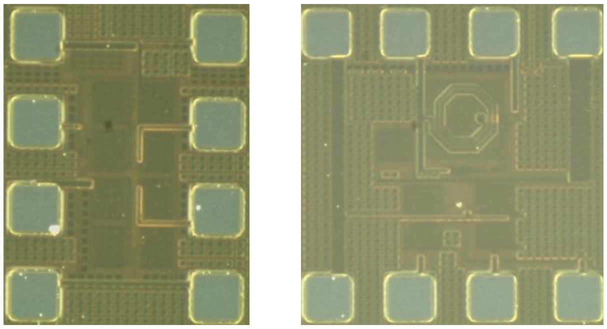
The above theoretical analysis can be used to guide the PD design to achieve the maximum output sensitivity. In the measurement applications, the unknown parameters A_2, A_4 $\cdots$can be obtained by calibration.

Theoretically, the minimum detectable input signal level depends on the noise floor and bandwidth. Without considering the matching networks in Fig. 3.5, and if the circuits are perfectly symmetric, the input noise floor caused by the source impedance is -174 dBm/Hz. However, the input matching networks yields noise. If the noise from inductors and capacitors is ignored and a 3 dB margin is added to the final calculated results, the calculated input noise floor is about -159 dBm/Hz for the circuit shown in Fig. 3.5(a) and -141 dBm/Hz for the circuit shown in Fig. 3.5(b). Considering the operating bandwidth, the total noise power would be -58 dBm and -38 dBm respectively. When used in six-port circuit [3.4], the minimum reflection coefficient at the DUT port is

-35 dB and the power loss from the DUT port to power measurement ports is around 6dB. If so, then the minimum input power to PD is -36 dBm if the input power at the DUT port is 5 dBm. Therefore, the proposed PD is appropriate for most applications even thought further work is needed to reduce noise for some applications, such as [3.20]-[3.21].

IV. EXPERIMENTAL RESULTS

The circuits in Fig. 3.5 have been implemented in a 0.13 μm CMOS process. The critical design parameters are shown in Table I. The circuit layouts are arranged as symmetrically as possible to minimize mismatch. In Fig. 3.5(a), M_{3A} and M_{4A} are chosen as NMOS transistors since normally NMOS transistors respond faster than the PMOS transistors, and V_{b2} is connected to V_{dd} directly to reduce the number of controlling terminals. The die microphotographs are shown in Fig. 3.6. The active circuit areas in Fig. 3.6(a) and (b) are 170×320 μm^2 and 250×340 μm^2, respectively. On-wafer measurements were done on a Cascade Microtech Summit 9000 probe station. The input pads were connected to a power source with GSG probes. The power loss in measurement setup was taken into consideration through calibration. The DC output voltage was measured by a Keithley 2600 SourceMeter. With a 1.2 V power supply, the structure shown in Fig. 3.5(a) shows the maximum sensitivity to the input power when V_{b1} = 0.6 V. Thus, all of the following results are measured when V_{b1} = 0.6 V. The static power consumption of the circuits shown in Fig. 3.5 (a) and Fig. 3.5(b) are 0.12 mW and 0.1 mW respectively with a 1.2 V power supply.



(a) (b)

Figure 3.6 (a) Die microphotograph of the circuit in Figure 3.5(a). (b) The circuit in Figure 3.5(b).

TABLE 3.1
CIRCUIT DESIGN PARAMETERS

Device	Unit	Designed Value	Device	Unit	Designed Value
M_1, M_2	µm / µm	1.3 / 0.12	M_3, M_4	µm / µm	13 / 0.12
C	fF	60	C_0	pF	20
$R_{1,2,3}$	Ω	104	L	nH	0.894
R_L	K Ω	6	R_4	K Ω	20
R_a	Ω	34	R_b	Ω	16

The S_{11}s were measured with an HP8510C network analyzer after on-wafer calibration. Fig. 3.7 shows the measured and simulated magnitude of S_{11} for the circuits in Fig. 3.5. Comparing the measured and simulated results, the measured results agree with the simulated results reasonably in trends. The measured results show that the return loss of the quasi T-coil matching network discussed in Section II is better than -14 dB in the measured frequency range from 500 MHz to 20.5 GHz, and its performance is much better than that of the circuit in Fig. 3.5(a) matched with resistors. Wideband input matching means a reasonable voltage transfer coefficient (close to 1) transferred from the source to the gate of transistor M_1 and also ensures a high sensitivity of the PD.

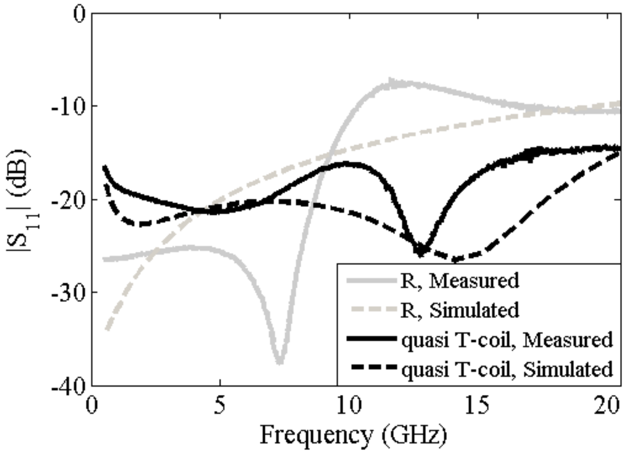
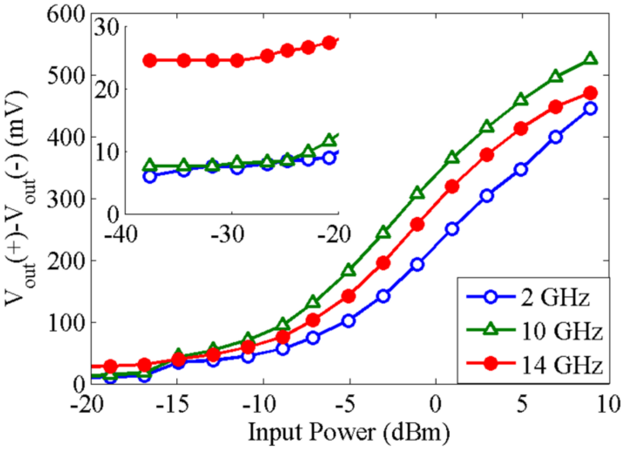
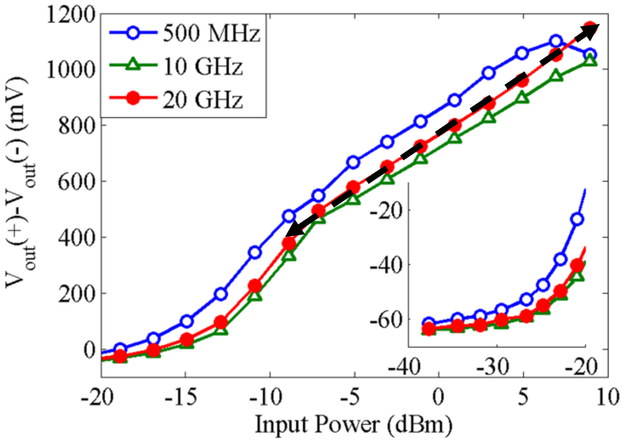


Figure 3.7 Measured and simulated S-Parameter $|S_{11}|$ of the circuits in Figure 3.5(a) (with R matched) and in Figure 3.5 (b) with quasi T-coil network.



(a)



(b)

Figure 3.8 Measured output voltage versus input RF power of (a) Figure 3.5(a), (b) Figure 3.5(b).

Fig. 3.8 shows the measured output voltage versus input power at different frequencies. Fig. 8(a) shows the measured results of the circuit in Fig. 3.5(a). When the circuit operates from 2 GHz to 14 GHz, the output DC voltage response difference is less than 3 dB for a given input RF power level as the input signals frequencies are swept. Fig. 3.8(b) shows the measured results of the circuit in Fig. 3.5(b). This circuit can operate from 500 MHz to 20 GHz. When the input RF power is larger than -10 dBm, transistor M_{1B} in Fig. 3.5(b) operates in the subthreshold regime and the output voltage is almost linear as indicated by the arrow in Fig. 3.8(b). From 500 MHz to 20 GHz, the output DC voltage response difference is less than 1.9 dB for input signals with a given input RF power level in the linear operating range as the arrow in Fig. 3.8(b). The optimal fitting curves with linear regression in the linear regime are

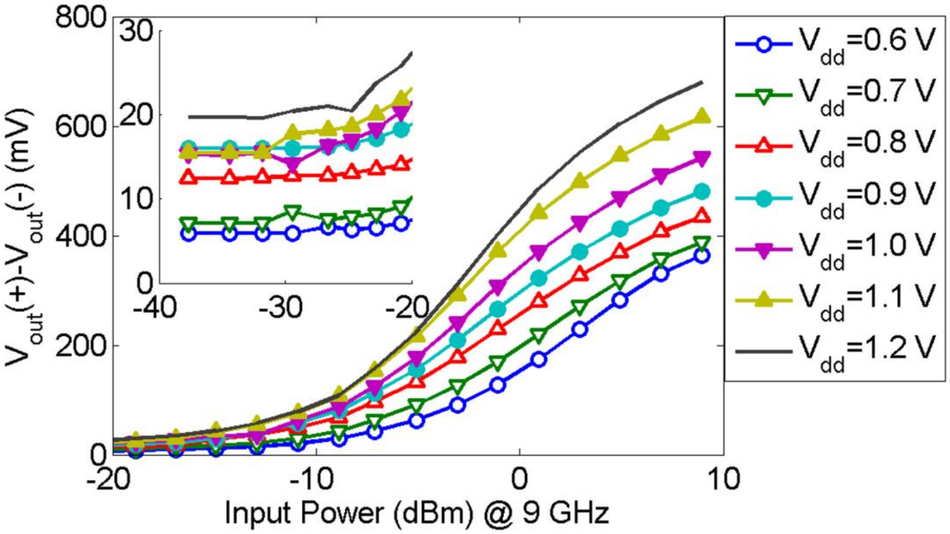
$$\begin{cases} 500\ MHz: output\left(mv\right) = 40\times\left(input\ \ power(dB)\right) + 885; \\ 10\ \ \ GHz: output\left(mv\right) = 36\times\left(input\ \ power(dB)\right) + 711; \\ 20\ \ \ GHz: output\left(mv\right) = 40\times\left(input\ \ power(dB)\right) + 775; \end{cases} \cdot \tag{3.18}$$

$$error\ ratio = \frac{calculated.value - measured.value}{calculated.value}. \tag{3.19}$$

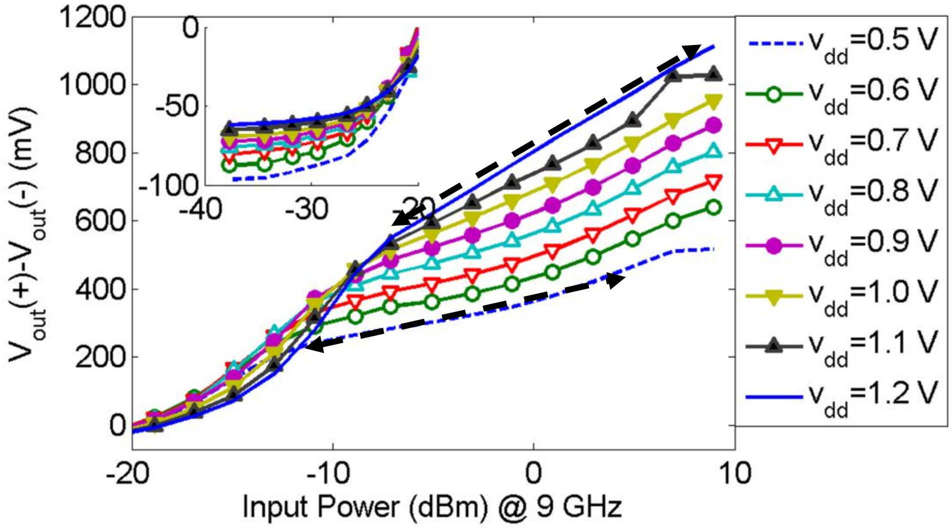
The error ratios between the output and the optimal fitting curves are less than ±1% for the linear operating range (16 dB-21 dB depending on frequency) with the definition in (3.19). When the input power is lower than -10 dBm, the MOS devices of the power detector in Fig. 3.5(b) operate in the saturation regime. If 1 mV/dBm is the minimum acceptable output sensitivity, the input power range of the circuit shown in Fig. 3.5(a) is -23 dBm to 9 dBm, and the input power range of the circuit in Fig. 3.5(b) is -38 dBm to 9 dBm. Thus, a 15 dB improvement in input power dynamic range is achieved for the circuit shown in Fig. 3.5(b) as compared to that shown in Fig. 3.5(a). The negative values in Fig. 3.8(b) are caused by the imperfect symmetric in the process and the secondary effects of the transistors. This does not affect its applications in measurement systems, since it can be absorbed during the calibration procedure.

When the power supply voltage is varied from 1.2 V to 0.5 V, Fig. 3.9(a) shows that the input dynamic range of the power detector in Fig. 3.5(a) decreases by approximately 10 dB, while Fig. 3.9(b) shows that the dynamic range of the power detector shown in Fig. 3.5(b) does not change as the power supply voltage decreases. When the power supply is varied from 1.2 V to 0.5 V, the linear operating range of the PD shown in Fig. 3.5(b) expands at the expense of lower output sensitivity with a decrease in the power supply voltage. Fig. 3.9(c) and (d) shows a dramatic reduction in power consumption when the power supply is varied from 1.2 V to 0.5 V. The static power consumption of the circuit in Fig. 3.5(b) is only 2×10^{-4} mW at a 0.5 V voltage supply, which makes it promising for applications in portable terminals. The peak in Fig. 3.9(d) is caused by the amplifier.

Table II is the comparison of this work with recent publication results. Even though, the published PDs were designed for communication applications, they also require large input dynamic range, low-power consumption, and high sensitivity [3.12]-[3.13]. Under the same definitions, Table II shows that this work achieves the maximum sensitivity, minimum power consumption, the largest input dynamic range, and the widest operating frequency range from 500 MHz to 20 GHz.

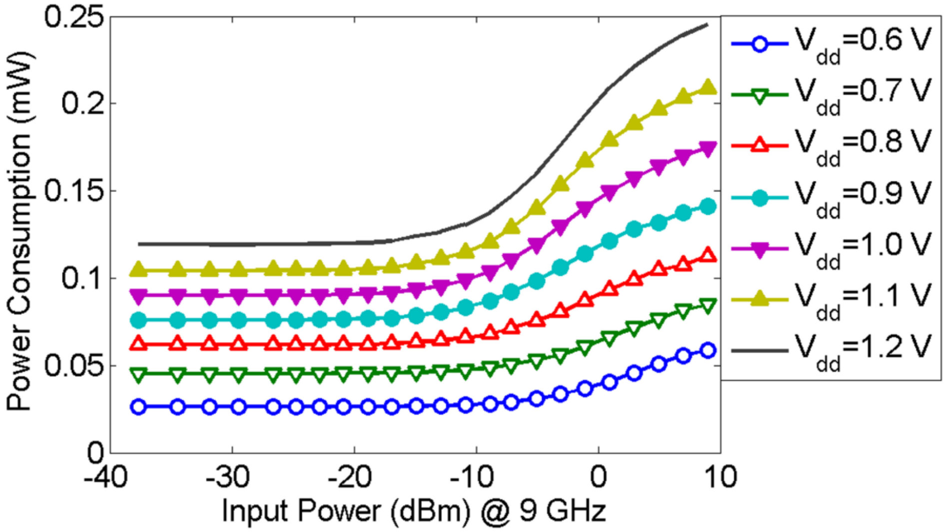


(a)



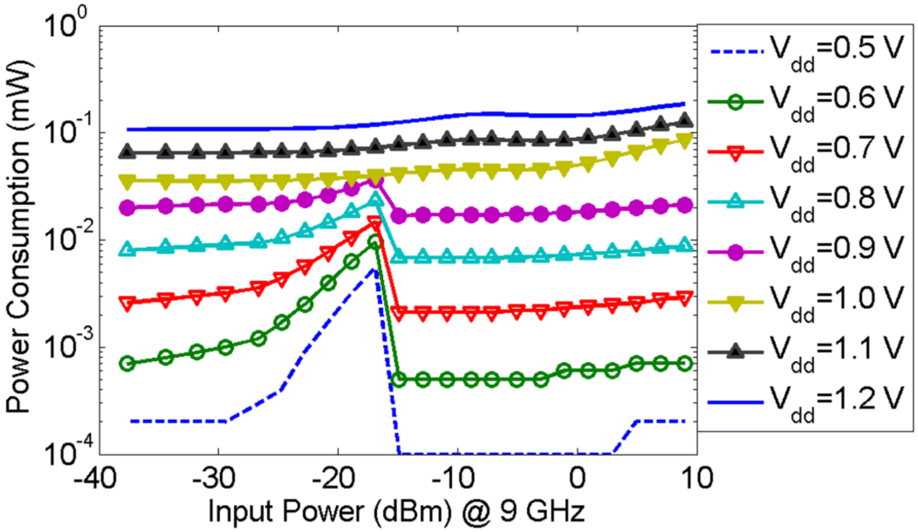
1200
1000
800
600
400
200
0
-20
-10
0
10
$V_{out}(+)-V_{out}(-)$ (mV)
Input Power (dBm) @ 9 GHz
0
-50
-100
-40
-30
-20
v_{dd}=0.5 V
v_{dd}=0.6 V
v_{dd}=0.7 V
v_{dd}=0.8 V
v_{dd}=0.9 V
v_{dd}=1.0 V
v_{dd}=1.1 V
v_{dd}=1.2 V

(b)



0.25
0.2
0.15
0.1
0.05
0
-40
-30
-20
-10
0
10
Power Consumption (mW)
Input Power (dBm) @ 9 GHz
V_{dd}=0.6 V
V_{dd}=0.7 V
V_{dd}=0.8 V
V_{dd}=0.9 V
V_{dd}=1.0 V
V_{dd}=1.1 V
V_{dd}=1.2 V

(c)



(d)

Figure 3.9 At different Vdd power supplies, measured output voltage versus input power of the circuit (a) Figure 3.5(a), (b) Figure 3.5(b); power consumptions versus input power of the circuit (c) Figure 3.5(a), (d) Figure 3.5(b).

TABLE 3.2

PERFORMANCE COMPARISON WITH RECENT PUBLISHED PD

	[3.12]*	[3.13]	Figure 3.5(b)
Technology	0.13 μm CMOS	0.18 μm CMOS	0.13 μm CMOS
Power Consumption	0.18 mW	3.8 mW	0.1 mW @1.2 V 2^{-4} mW @0.5 V
Operating Frequency	125 MHz -8.5 GHz	3.1 GHz -10.6 GHz	500 MHz – 20 GHz
Input dynamic range	20 dB	~35 dB	~47 dB
Linearity Error For Specified Input Range	±0.5 dB for 18 dB	± 2.4 dB for 20 dB	< ±1% for ~20 dB
Flatness of Frequency Response	12 dB	1.8 dB	4 dB (0.5 GHz -20 GHz) 1 dB (10 GHz - 20 GHz)
Output Sensitivity	~6.5 mV/dB	~4.3 mV/dB	~26.8 mV/dB

*Multiple off chip matching networks were used in measurement [3.12].

V. CONCLUSION

In this paper, a self-biased low-power power detector is proposed, analyzed, and demonstrated. Depending on input RF power levels, the MOS transistors of the PD operate in either saturation or subthreshold regimes. To enhance the sensitivity and to expand the operating frequency range, an ultra wideband quasi T-coil matching network was designed and an embedded amplifier was used. The operating frequency ranges from 500 MHz to 20 GHz. The output DC voltage response is nearly frequency independent, varying by less than 1.9 dB for a fixed RF power level in the operating frequency range. The linearity error in the linear operating range is less than ±1%.

Though the linear operating range is 16 dB to 21 dB depending on frequency, the detectable input dynamic range is up to 47 dB, which makes it very useful in both six-port communication and measurement systems applications, where the input RF power levels of the measurement port 3-6 may change dramatically as the input signal in port 2 varies.

REFERENCES

[3.1] Shuyun Zhang, Jelena Madic, Pavel Bretchko, Julius Mokoro, Raymond Shumovich, Rob McMorrow, "A Novel Power Amplifier Module for Quad-Band Wireless Handset Applications," IEEE Trans. on Microwave Theory and Techniques, Vol. 51, NO. 11, November 2003.

[3.2] Chun-Pang, Hen-Wai Tsao, “A 110-MHz 84-dB CMOS Programmable Gain Amplifier With Integrated RSSI Function,” IEEE Journal of Solid-State Circuits, Vol. 40, No. 6, June 2005.

[3.3] Glenn F. Engen, “The Six-Port Reflectometer: An Alternative Network Analyzer,” IEEE Trans. on Microwave Theory and Techniques, Vol. MTT-25, No. 12, December 1977.

[3.4] Chaojiang Li, Hanqiao Zhang, Pingshan Wang, “A Novel Six-Port Circuit Based on Four Quadrature Hybrids,” International Journal of RF and Microwave Computer-Aided Engineering, DOI: 10.1002 /mmce. 20410, Dec 2009.

[3.5] Glenn F. Engen, “An Improved Circuit for Implementing the Six-Port Technique of Microwave Measurements,” IEEE Trans. on Microwave Theory and Techniques, Vol. MTT-25, No. 12, December 1977.

[3.6] Yanyang Zhao, Jean-Francois Frigon, Ke Wu, Renato G. Bosisio, “Multi(Six)-Port Impulse Radio for Ultra-Wideband,” IEEE Trans. on Microwave Theory and Techniques, Vol. 54, No. 4, April 2006.

[3.7] J. Perez-Duenas, J. G. Wanguemert-Perez, I. Molina-Fernandez, “Novel Modulation Scheme and Six-Port Based RAKE Receiver for DS-UWB,” IEEE Trans. on Wireless Communication, Vol. 8, No. 7, July 2009.

[3.8] Veljko Milanovic, Michael Gaitan, Janet C. Marshall, Mona E. Zaghloul, “CMOS Foundry Implementation of Schottky Diodes for RF Detection,” IEEE Trans. on Electron Devices, Vol. 43, NO. 12, December 1996.

[3.9] Robert G. Meyer, “Low-Power Monolithic RF Peak Detector Analysis,” IEEE Journal of Solid-State Circuits, Vol. 30, No. 1, January 1995.

[3.10] Qizhang Yin, William R. Eisenstadt, Robert M. Fox, Tao Zhang, “A Translinear RMS Detector for Embedded Test of RF ICs,” IEEE Trans. on Instrumentation and Measurement, Vol. 54, No. 5, October 2005.

[3.11] Giorgio Ferrari, Laura Fumagalli, Marco Sampietro, Enrico Pratic, Marco Fanciulli, “CMOS Fully Compatible Microwave Detector Based on MOSFET Operating in Resistive Regime,” IEEE Microwave and Wireless Components Letters, Vol. 15, No. 7, July 2005.

[3.12] Yijun Zhou, Michael Yan-Wah Chia, “A Low-Power Ultra-Wideband CMOS True RMS Power Detector,” IEEE Trans. on Microwave Theory and Techniques, Vol. 56, No. 5, May 2008.

[3.13] Kenneth A. Townsend, James W. Haslett, “A Wideband Power Detection System Optimized for the UWB Spectrum,” IEEE Journal of Solid-State Circuits, Vol. 44, No. 2, February, 2009.

[3.14] Sherif Galal, Behzad Razavi, “Broadband ESD Protection Circuits in CMOS Technology,” IEEE Journal of Solid-Circuits, Vol. 38, No. 12, December 2003.

[3.15] Thomas H. Lee, “The Design of CMOS Radio-Frequency Integrated Circuits,” Cambridge University Press, 2004.

[3.16] Thomas T. True, “Bridged-T Termination Network,” U.S. Patent 3 155 927, 1964.

[3.17] David M. Pozar, “Microwave Engineering, Third Edition,” John Wiley & Sons, Inc, 2005.

[3.18] Theerachet Soorapanth, Thomas H. Lee, “RF Linearity of Short-Channel MOSFETS,” 1st International Workshop on Design of Mixed-mode Integrated Circuits and Applications, pages: 81-84, 1997.

[3.19] Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, “Analysis and Design of Analog Integrated Circuits,” John Wiley & Sons, Inc. 2001.

[3.20] Alessandro Ocera, Marco Dionigi, Elisa Fraticcioli, Roberto Sorrentino, “A Novel Techniques for Complex Permittivity Measurement Based on a Planar Four-Port Device,” IEEE Trans. on Microwave Theory and Techniques, Vol. 54, No. 6, June 2006.

[3.21] Hanqiao Zhang, Chunrong Song, Pingshan Wang, “A New Method for High-frequency Characterization of Patterned Ferromagnetic Thin films,” Journal of Applied Physics 105, 07E716, 2009.

CHAPTER FOUR

ANALYSIS AND DESIGN OF A HIGH-Q DIFFERENTIAL ACTIVE INDUCTOR WITH WIDE TUNGING RANGE

Abstract— The analysis and design of a high-Q differential active inductor with wide tuning range is presented in this chapter. The self-resonant frequency (SRF) and quality factor (Q) of the inductor can be tuned independently. The inductor was implemented in a 0.13 μm CMOS process. The measured SRF is tunable from 0.5 to 10.2 GHz. The obtained maximum quality factor is as high as 3000. The analysis shows that higher inductance corresponds to higher inductor noise while the correlation between quality factor and noise is relatively weak. Measurement results confirmed these predictions. The measured results show that this inductor structure is suitable for broadband reconfigurable radio-frequency (RF) system development. Further analysis and measurements show that the inductor is intrinsically nonlinear, so are gyrator-C based active inductors in general. A compensation circuit is proposed to improve the linearity characteristics of such inductors.

Index Terms— CMOS integrated circuit, Differential active inductor, high quality factor, radio frequency, wide tuning range

I. INTRODUCTION

CMOS inductors have a broad range of applications in radio frequency integrated circuit (RFIC) design [4.1]-[4.2], including filters [4.3], phase shifters [4.4], oscillators [4.5], low noise amplifiers (LNA) [4.6]-[4.7], power dividers, and hybrids [4.8]-[4.10]. Unfortunately, passive CMOS inductors occupy large chip areas, and their quality factors are very low. Furthermore, they can only provide limited inductance values in a certain operating frequency range. Therefore, their applications are constrained. Besides, passive inductors are also not tunable, which makes them inconvenient for reconfigurable circuit design. Active inductors, on the other hand, do not suffer from these problems since their inductance comes from emulating inductor impedance with active devices. As a result, CMOS active inductors have attracted much attention [4.2]. Of the two types of active inductors, i.e. single-ended and differential active inductors (DAI), DAIs have common-mode noise rejection properties with better linearity characteristics [4.11]. These properties make DAIs attractive. Thus, various DAIs have been proposed and studied [4.2], [4.11]-[4.13].

The main figure-of-merits (FOM) of an active inductor include its operating frequency range (represented by its SRF), quality factor (Q), noise performance, linearity, and tunability [4.2]. For DAIs, a CMOS source-degenerated structure yielded a 7.85 GHz SRF [4.12], which is the highest measured SRF reported so far to the best of our knowledge. Yet higher SRF is needed for higher frequency applications, e.g. the FCC ultra wideband (UWB) regime covers frequencies from 3.1-10.6 GHz. A Q of about 1000 was experimentally demonstrated in [4.13]. That Q is also the highest reported so far. The high-Q inductor is promising for frequency selection applications. However, high-Q operation of active inductors could dramatically deteriorate inductor noise performance, which is already aggravated by the use of active devices. For many active inductor architectures, it was shown that their noise is at least 2Q times higher than their passive counterpart if both have similar frequency characteristics [4.3], [4.14]. Nevertheless, integrated DAI noise characteristics need further investigations. Moreover, nonlinearity properties of high-Q active inductors require detailed studies since exceptionally high voltage could arise between the inductor terminals. For instance, when used in an RLC series resonator, the voltage across the inductor terminals is Q times the voltage across the resonator at resonance. Finally, frequency and inductance tunability are desired for reconfigurable RFIC implementations, such as software defined radios [4.15].

This chapter proposes and analyzes a DAI with a focus on its main FOMs. The experimental results of its noise and nonlinearity characteristics are also presented. The results show that this DAI structure does not have a strong correlation between its Q and noise. The DAI, gyrator-C based active inductors in general, is intrinsically nonlinear, i.e. its properties (e.g. inductance values) depend on input power levels. Circuit techniques to further improve the linearity of the DAI are also proposed. The paper is arranged as follows: section II presents the analysis of the DAI, section III describes the DAI design and experimental results. Discussions and conclusions are in Section IV.

II. DESIGN CONSIDERATIONS OF THE DIFFERENTIAL ACTIVE INDUCTOR

The proposed DAI is shown in Fig. 4.1(a), in which the inverter pair is used to provide negative resistance to boost the Q of the DAI. The voltage var_3 is to provide independent control of the negative resistor. Tuning Q with negative resistance has been reported previously by using only NFETs or PFETs, but not inverters. The main advantage of the cross-coupled inverter pair in Fig. 4.1(a) is that it establishes an independent DC current path from var$_3$ to ground for the negative resistor and provides an independent control of the negative resistance. As a result, M$_5$ (and M$_6$) does not need to carry all the DC current for the negative resistor. Therefore, it is possible to optimize M$_5$ (g$_{m5}$) for higher Q and higher L. Moreover, higher operating frequency and larger operating frequency range are possible since the full capacity of M$_5$ can be exploited.

A. Inductance values, quality factors and self-resonant frequency

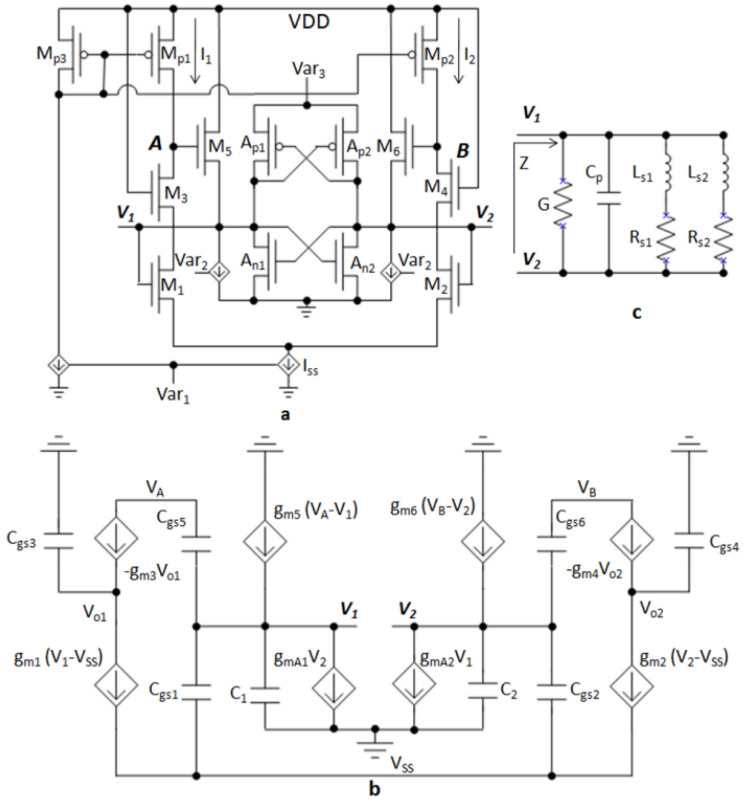


Figure 4.1 Proposed differential active inductor. (a) Schematic of the differential active inductor (DAI). (b) The small signal model for DAI in Fig. 4.1(a). (c) An equivalent circuit for the DAI in Fig. 4.1(a).

The small signal model of the DAI circuit in Fig. 4.1(a), without considering MOS transistor channel resistances, is shown in Fig. 4.1(b). Assume the DAI structure is symmetric, and then the admittance between terminals V_1 and V_2 can be obtained with small signal analysis.

$$Y = \frac{1}{Z} \approx -\frac{g_{mA1}}{2} + \frac{1}{2}\left(sC_1 + sC_{gs1}\right) + \frac{1}{2\left(\frac{s^2 C_{gs3} C_{gs5}}{g_{m1} g_{m3} g_{m5}} + \frac{sC_{gs5}}{g_{m1} g_{m5}}\right)} + \frac{1}{2\left(\frac{1}{g_{m3}} + \frac{sC_{gs3}}{g_{m1} g_{m3}}\right)} \tag{4.1}$$

where g_{mi} is the transconductance of transistor M_i; g_{mA1} is the sum of the transconductance provided by A_{n1} and A_{p1} (or A_{n2} and A_{p2}); C_A is the capacitance between point A (or B) and AC ground; C_{gs5} is the gate-source capacitance of M_5 (or M_6). Equation (4.1) indicates that the DAI shown in Fig. 4.1(a) has an equivalent circuit as shown in Fig. 4.1(c).

$$\frac{1}{Z} = G + j\omega C_p + \frac{1}{R_{s1} + j\omega L_1} + \frac{1}{R_{s2} + j\omega L_2} \tag{4.2}$$

Compare (4.1) and (4.2), the equivalent circuit parameters in Fig. 4.1(c) are

$$G \approx \frac{-g_{mA1}}{2} \quad , \tag{4.3}$$

$$C_p \approx \frac{C_1 + C_{gs1}}{2} \quad , \tag{4.4}$$

$$L_{s1} \approx \frac{2C_{gs5}}{g_{m1} g_{m5}},\ L_{s2} \approx \frac{2C_{gs3}}{g_{m1} g_{m3}} \quad , \tag{4.5}$$

$$R_{s1} \approx -\frac{2\omega^2 C_{gs3} C_{gs5}}{g_{m1} g_{m3} g_{m5}},\ R_{s2} \approx \frac{1}{g_{m1}} \quad . \tag{4.6}$$

The addition of negative resistance only affects G. The main contributor of inductance is L_{s1}, since R_{s2} is a large resistor and L_{s2} is small. Set the reactance of Z to zero (i.e. Imag Z =0), the SRF of the DAI is

$$\omega_{osc}^2 = \frac{g_{m3}}{2C_{gs3}}\left(\sqrt{\left(\frac{g_{m1}}{C_1+C_{gs1}}-\frac{g_{m3}}{C_{gs3}}\right)^2+\frac{4}{L_{s1}\left(C_1+C_{gs1}\right)}}-\left(\frac{g_{m1}}{C_1+C_{gs1}}-\frac{g_{m3}}{C_{gs3}}\right)\right) \quad . \qquad (4.7)$$

The DC current going through M_1 and M_3 is I_1 , which is half of the tail current (I_{ss}), then

$$g_{m1,3} = \sqrt{2K^{'}\frac{W_{1,3}}{L_{1,3}}I_1} \text{ and } \frac{g_{m1}}{g_{m3}} = \sqrt{\frac{W_1/L_1}{W_3/L_3}} . \qquad (4.8)$$

where W_i and L_i are the width and length of transistor M_i, respectively, and the parameter $K^{'} = \mu_n C_{ox}$, in which μ_n is electron mobility and C_{ox} is gate oxide capacitance per unit area. Equations (4.7) and (4.8) indicate that the inductor SRF can be tuned through tuning g_{m3}, in other words, by tuning the DC bias current I_1 which is controlled by the voltage controller var_1 in Fig. 4.1(a).

The quality factor Q can be calculated with

$$Q = \frac{\mathrm{Im}\,ag\left(Z\right)}{\mathrm{Re}\,al\left(Z\right)} = \left|\frac{A}{B}\right|, \qquad (4.9)$$

where

$$A = s^4 C_{gs3}^2 C_{gs5}\left(C_1+C_{gs1}\right)+s^2 C_{gs5} g_{m3}\left(g_{m1}C_{gs3}-g_{m3}\left(C_1+C_{gs1}\right)\right)-g_{m1}g_{m3}^2 g_{m5} \qquad (4.10)$$

and

$$B = -s^3 C_{gs3} C_{gs5} g_{mA1} + s C_{gs5} g_{m3} \left(g_{m1} g_{m3} - g_{mA1} g_{m3} - g_{m1} g_{m5} \right) \quad . \tag{4.11}$$

Equations (4.10)-(4.11) indicates that high Q can be achieved by tuning the negative transconductance g_{mA1}. The tuning of Q does not affect SRF and inductance value L. The tuning independence implies that high Q and high frequency operations are possible.

B. Noise

To evaluate the noise performance of the DAI in Fig. 1(a), its noise model is shown in Fig. 4.2, in which the noise model of MOS transistors in [4.16] is used. There are two kinds of noise sources in Fig. 4.2, channel induced noise and gate induced noise. They are

$$\frac{\overline{i_{ndi}^2}}{\Delta f} = 4KT \frac{\gamma}{\alpha_i} g_{mi}, \frac{\overline{i_{ngi}^2}}{\Delta f} = 4KT \delta g_{gi}, i = 1, \cdots 6, \tag{4.12}$$

where

$$\alpha_i = \frac{g_{mi}}{g_{d0i}} \, and \; g_{gi} = \frac{\alpha \omega^2 C_{gsi}^2}{5 g_{mi}} \, . \tag{4.13}$$

γ is the channel noise factor, δ is the gate noise coefficient, g_{d0i} is the drain conductance for transistor M_i, K is Boltzmann constant and T is temperature.

To simplify the analysis, we ignore noise contribution from the cross-coupled inverter pair while considering all the gate-induced and channel-induced noise sources for transistors M_1-M_6. The analysis, shown in Appendix A, gives the differential output noise as

$$\frac{\overline{V_{total}^{2}}}{\Delta f} \approx \sum_{i=1}^{6}\left|\frac{N_{ngi}}{\left(M_{ngi}+\frac{1}{R_{s1}+sL_{s1}}\right)}\right|^{2}\frac{\overline{I_{ngi}^{2}}}{\Delta f}+\left|\frac{N_{ndi}}{\left(M_{ndi}+\frac{1}{R_{s1}+sL_{s1}}\right)}\right|^{2}\sum_{i=1}^{6}\frac{\overline{I_{ndi}^{2}}}{\Delta f}. \qquad (4.14)$$

Equation (4.14) indicates that larger ωL_1 will cause higher differential output noise. On the other hand, there are no direct and explicit connections between noise voltage and quality factor Q in this DAI structure. This is different from those observations in [4.1], [4.14], in which the noise of active inductors is at least 2Q times higher than their passive counterparts when both have similar frequency characteristics. This property is very useful, especially in circuits that use T or π transmission line models. For examples, in the designs of lumped-element power dividers and lumped-element couplers, ωL is a constant which is related with the characteristic impedance [4.17]-[4.19]. Then (4.14) may be used to guide noise performance considerations.

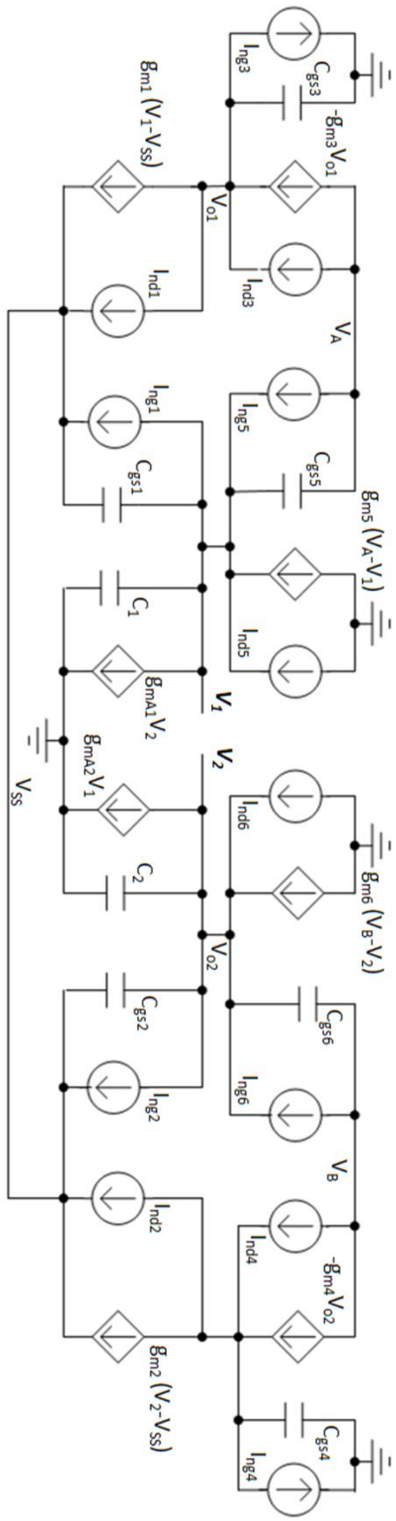


Figure 4.2 Noise model for the ADI structure shown in Fig. 4.1(a).

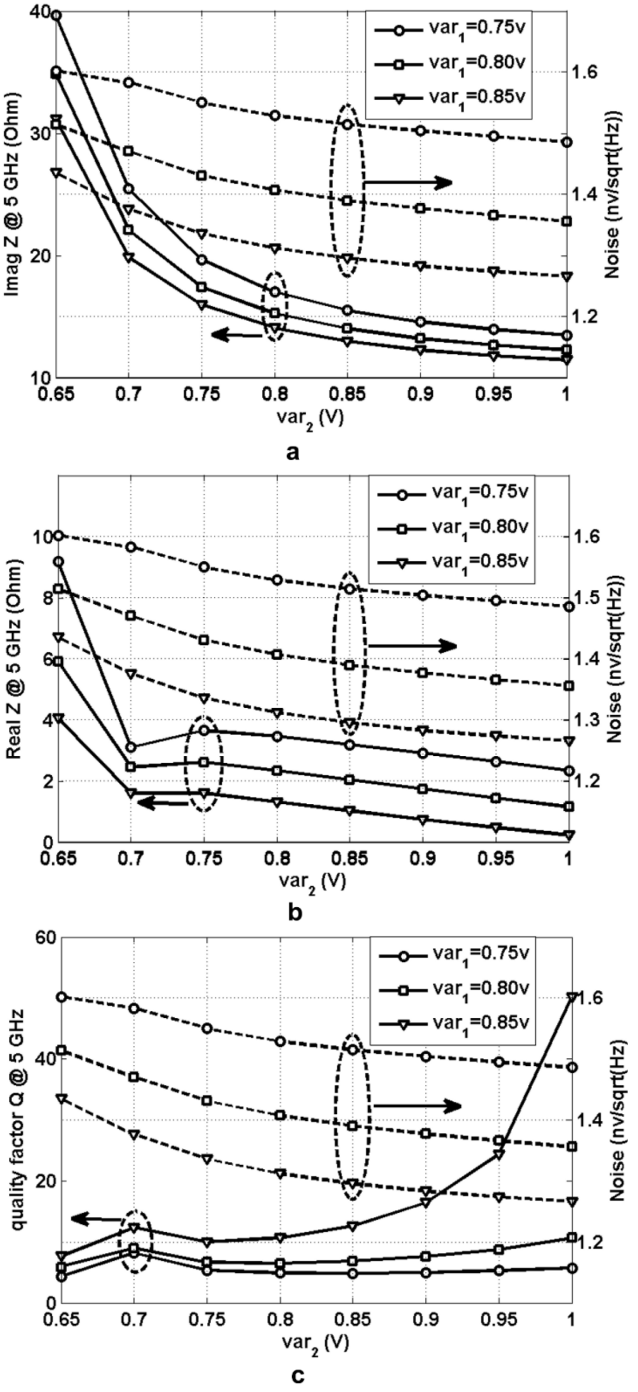


Figure 4.3 Simulated results of noise and (a) Imag Z. (b) Real Z. (c) Quality factor Q.

Fig. 4.3 shows the relationship between noise and Imag Z, Real Z, and quality factor Q for different var_2. The results are obtained from Cadence Spectre simulations. Fig. 4.3(a) shows that larger Imag Z (i.e. larger ωL) corresponds to higher noise. Fig. 4.3(b) shows noise voltage and equivalent resistance R (i.e. Real Z) of the DAI. Fig. 4.3(c) shows that noise does not change linearly with Q values. It is clear that their relationship is different from that of passive inductors, for which noise voltage changes linearly with the square root of parasitic resistance R. Using the linearity correlation analysis method in [4.20], the correlation coefficients between noise and Imag Z, Real Z, and quality factor Q are approximately 0.96, 0.6 and 0.4 (1 represents strong linear correlation and 0 presents weak correlation). Therefore, noise has relatively weak correlation with Q, but strong correlation with Imag Z values as predicted by (4.14). The weak relationship between Q and noise is important for active inductor applications since difficult trade-offs between the two critical parameters can be greatly relaxed.

C. Nonlinearity

As mentioned in the Introduction section, the DAI is intrinsically nonlinear, i.e. its properties, including inductance values, Q-factor, depend on input power. Usually, nonlinearity occurs due to high input signal levels. Then signal distortion will happen in the transconductance amplifiers and inductor characteristics will change accordingly. High signal levels can do occur across inductors in a circuit, such as Q-times input voltages in RLC series circuits as discussed in Section I.

If we ignore the negative resistor, the proposed DAI can be treated as three amplifiers: a differential cascode transconductance amplifier shown in Fig. 4.4(a) and two common drain amplifiers in Fig. 4.4(b), in which the active loads from the current sources are simplified as resistors. An examination of the circuit in Fig. 4.1(a) shows that the DC bias for $M_{5,6}$ in common drain amplifiers is affected by the DC output of transconductance amplifier composed of $M_{1,3}$ and $M_{2,4}$, and vice versa. The DC bias will change with input signal levels due to the square law of transistor currents. Consequently, the transconductance of M_1 and M_5 will change. So do the inductance values (and inductor FOMs). Therefore, the active inductor in Fig. 4.1(a) is inherently nonlinear, even for low input signal level. So are most other active inductors, which are based on gyrator-C architectures [4.2]-[4.11]. This observation explains the nonlinearity issues observed in [4.10] even when the input power was quite low.

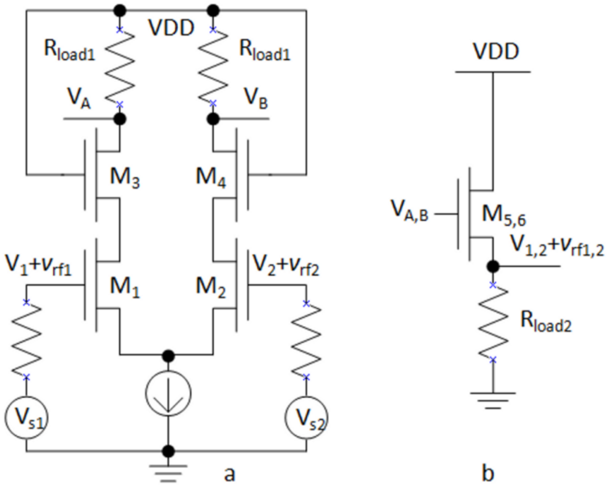


Figure 4.4 Symbols used in the analysis are $V_{a,b}=V_{A,B}+v_{a,b}$, in which $V_{1,2}$ and $V_{A,B}$ are DC voltage, while $v_{a,b}$ and $v_{rf1,2}$ are RF signals. (a) Differential cascade transconductance amplifier. (b) Common drain amplifier.

To quantify the inductance dependence on input signal level when the amplifiers are in linear region, we ignore the cascode transistors ($M_{3,4}$) in the following analysis to simplify the procedures since they do not change the current characteristics of the amplifiers (i.e. $M_{1,2}$). When there is no input RF signal, the currents of both current paths in Fig. 4.4(a) are

$$I_{ds,0} = \frac{K'}{2}\frac{W_{1,2}}{L_{1,2}}(V_{GS} - V_{th1,2})^2 \cdot \tag{4.15}$$

where V_{GS} is the DC bias of M_1 or M_2, V_{thi} is the threshold voltage of transistors M_i; W_i and L_i are the channel width and length of transistors M_i, respectively. Assume the amplitude of the input wave is v_{rf}, the transistors operate in active region and the effect of feedback circuit in Fig. 4.4(b) is negligible, then the drain source current is:

$$I_{ds1,2} = \frac{K' W_{1,2}}{2L_{1,2}}\left\{(V_{GS} - V_T)^2 + \frac{V_{rf}^2}{2} + 2(V_{GS} - V_T)v_{rf}\cos(\omega t) + \frac{V_{rf}^2\cos(2\omega t)}{2}\right\}. \tag{4.16}$$

Equation (4.16) indicates that the input RF signal induces a DC current variation, ΔI, which will cause a DC voltage variation at point A (or B). The ration is

$$\frac{\Delta V_{A,B}}{V_{A,B}} = \frac{-\Delta I R_{load1}}{V_{A,B}} = \frac{-v_{rf}^2}{2\left(V_{GS} - V_{th1,2}\right)^2}. \tag{4.17}$$

Similarly, this process happens in Fig. 4.4(b), and DC voltage variation ratio is:

$$\frac{\Delta V_{1,2}}{V_{1,2}} = \frac{\left(A_v v_{rf}\right)^2}{2\left(V_{GS5,6} - V_{th5,6}\right)^2}. \tag{4.18}$$

where A_v is the voltage gain from input to point A (B).

The DC bias voltage variation ratios of the circuit in Fig. 4.1(a) were simulated with PSS in Cadence Spectre and the results are presented in Fig. 4.5. When $var_1=var_2=0.8$ V, the variation trends of $V_{1,2}$ (increasing with the increase of input level) and $V_{A,B}$ (decreasing with the increase of input level) are consistent with the predictions of (4.17) and (4.18). The variation ratio of $V_{1,2}$ is obviously smaller than that of $V_{A,B}$. This is because the variation of $V_{1,2}$ is alleviated by the negative resistor circuit since the circuit operates in saturation region. Therefore, we need only consider the variation of $V_{A,B}$ in the following analysis.

The transconductance variation of g_{m5} and g_{m6}, caused by the variation of $V_{A,B}$, is

$$\Delta g_{m5,6} = K^{'} \frac{W_{1,2}}{L_{1,2}} \Delta V_{A,B} = -\left(K^{'} \frac{W_{1,2}}{L_{1,2}} \right)^2 \frac{v_{rf}^2}{2} R_{load1} \cdot \qquad (4.19)$$

According to the equivalent inductance (4.5), the inductance variation caused by the small signal input power variation is

$$\frac{\Delta L_{s1}}{L_{s1}} \approx \frac{R_{load1} \frac{1}{2} \left(K^{'} \frac{W_{1,2}}{L_{1,2}} \right)^2 v_{rf}^2}{g_{m5,6} + R_{load1} \frac{1}{2} \left(K^{'} \frac{W_{1,2}}{L_{1,2}} \right)^2 v_{rf}^2} . \qquad (4.20)$$

The simulated Imag Z (i.e. ωL_s) variation ratios of the inductor in Fig. 4.1(a) at 7GHz are presented in Fig. 4.5 for $var_1=var_2=0.8$ V. It is shown that bias voltage $V_{A,B}$ decreases with the increase of input power level. Obvious decline occurs even when the input is smaller than -10 dBm while $V_{1,2}$ is almost constant. Inductance increases as predicted by (4.17) and (4.20). When input power is larger than about 10 dBm, the transistors are entering triode regions. As a result, there are dramatic changes in Imag Z.

To improve the linearity performance of the inductor, a compensation circuit can be added as shown in Fig. 4.6. M_{n1} and M_{n2} are two NMOS transistors operating in saturation region. From the square current law, the RF input $-A_v v_{rf1,2}$ of the compensation transistors will generate DC current ΔI_C from VDD to point A and B, which will compensate the DC current ΔI produced by transistors M_1 and M_2. Therefore, the DC voltage drop $\Delta V_{A,\ B}$ caused by DC current ΔI going through R_{load1} will be compensated. When the size of $M_{n1,2}$ is W/L= 7 μm / 0.13 μm and var_1=var_2=0.8 V, Cadence Spectre simulations show that the addition of the compensation transistors improves the linearity and the results after the addition of the compensation circuit is also shown in Fig. 4.5.

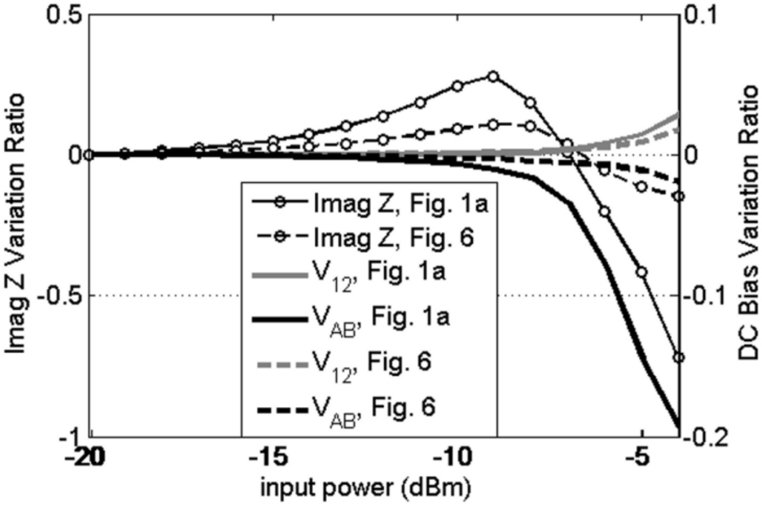


Figure 4.5 Variations of Imag Z and DC bias voltage with input power for var_1= 0.80 V and var_2= 0.80 V. The simulation is conducted with PSP in Cadence Spectre. The simulated circuits are in Fig. 4.1(a) and Fig. 4.6.

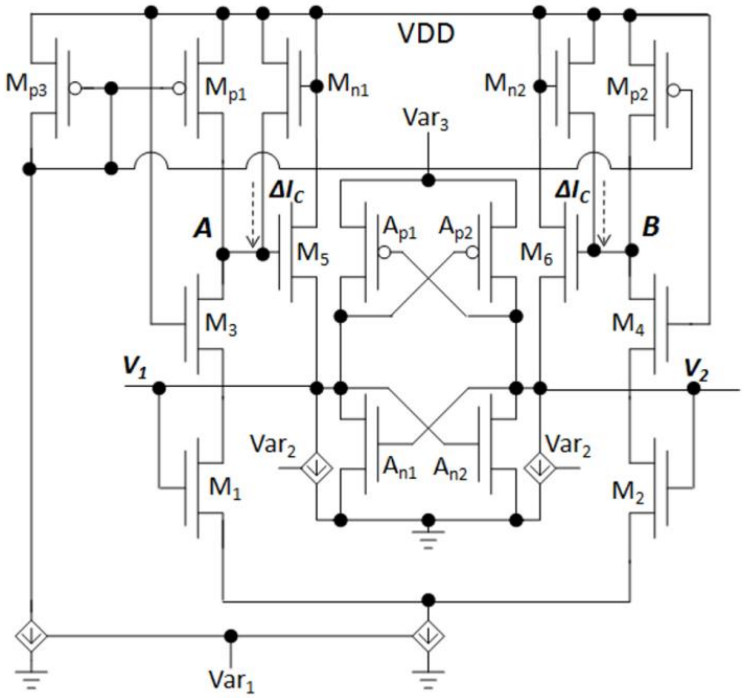


Figure 4.6 Possible DAI with nonlinearity compensation transistors.

D. Power Consumption

DC power consumption of active inductors is a disadvantage compared to passive inductors. The inverter pair in Fig. 4.1(a) dissipates more power and adds more parasitic capacitance (C_1, which will decrease the resonance frequency of the DAI.) simultaneously when compared with active inductors that do not use negative resistors. Fig. 4.7(a) shows a possible arrangement to reuse DC currents and save power. The loads of two common drain amplifiers can be replaced by the negative resistors, a cross-coupled pair. The disadvantage is that the quality factor and the inductance values cannot be tuned independently. When the DC power supply voltage VDD is 1.6 V and Var_1 is 1.2 V, the simulated results, shown in Fig. 4.7(b), indicate that both circuits in Fig. 4.1(a) and Fig. 4.7(a) can obtain similar Imag Z when operating frequency is below 13 GHz. But the SRF of the circuit in Fig. 4.7(a) increases to about 17.5 GHz compared with 14 GHz in Fig. 4.1(a). The circuit also saves more than 50% DC power consumption. The simulated results in Fig. 4.7(b) agree with our analysis.

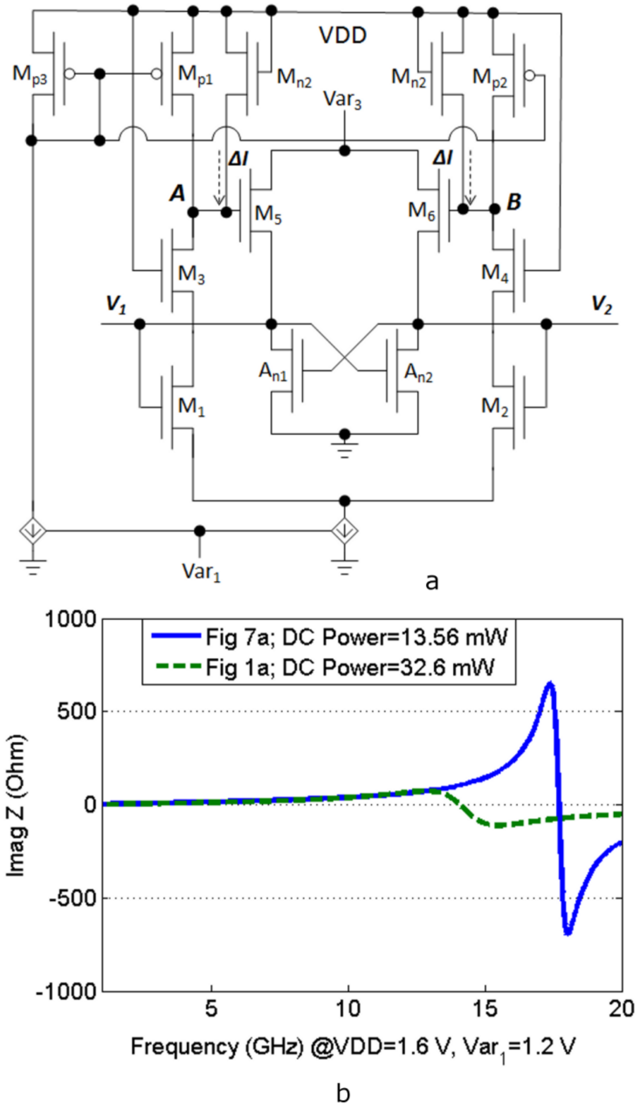


Figure 4.7 Proposed DAI with current reuse consideration. (a) Possible DAI with current reuse consideration. (b) Simulated results of the circuits in Fig. 4.1(a) and Fig. 4.7(a).

III. CIRCUIT IMPLEMENTATION AND EXPERIMENT RESULTS

The proposed DAI in Fig. 4.1(a) was fabricated in a 0.13 μm CMOS process. Transistor sizing is guided by (4.3)-(4.7). Table 1 shows the specific transistor dimensions. To save chip area and to facilitate differential measurement, one input terminal (V_1) was used as the virtual ground. Fig. 4.8(a) shows the microphotograph of the circuit and the active die area is 50 μm × 75 μm. In the measurement, var_3 is combined with VDD at 1.6 V. On-wafer probing was conducted to measure one-port S-parameters (S) of the inductor with an HP8510C network analyzer. The RF G-S-G probe was touched on the V_1-V_2-V_1 pads. Noise performance was measured with an R&H FSEK-30 spectrum analyzer. The measurement arrangement is shown in Fig. 4.9. The Z parameters and Q are calculated using the obtained S-Parameter S with the following equations.

$$Z = Z_0 \frac{1+S}{1-S}, \; Q = \frac{\mathrm{Im}(Z)}{\mathrm{Re}(Z)}. \tag{4.21}$$

The noise voltage is calculated with [4.17]:

$$\overline{V_n} = sqrt\left(\frac{8Z_0 \times 0.001 \times 10^{\frac{n}{10}} \,|1-S_{22}\Gamma_L|^2 |1-\Gamma_s\Gamma_{in}|^2}{|1-\Gamma_s|^2 |S_{21}|^2 \left(1-|\Gamma_L|\right)^2} \right). \tag{4.22}$$

where n is the measured noise power in dBm scale.

The measured result with maximum SRF (10.2 GHz) is shown in Fig. 4.10. The maximum SRF was obtained when Var_1 and Var_3 are 1.6 V, Var_2 is 1.0 V. Fig. 4.11

demonstrates that the inductance and quality factor can be tuned through var_2 as the prediction of (4.4) while keeping SRF almost unchanged as the prediction of (4.7). The inductance has more than 80% tuning range at the frequency point (3.7 GHz) when Q achieves the highest value.

TABLE 4.1

DEVICE SIZE OF THE OPTIMIZED CIRCUIT

Transistor	W/L (μm/μm)	Fingers
M_1, M_2	156/0.2	120
M_3, M_4	13/0.12	10
M_5, M_6	117/0.18	100
A_{n1}, A_{n2}	13/0.12	10
A_{p1}, A_{p2}	13/0.12	10

Fig. 4.12 shows the relationship between var_1 and Imag Z, Q, and noise voltage. Fig. 4.12(a) verifies that inductance decreases when g_{m1} increases as the prediction of (4.5). The self-resonant frequency increases when g_{m1} increase (i.e. var_1 increases) as the prediction of (4.7). Fig. 4.12(b) shows that a high quality factor Q, up to 3000, can be obtained. Fig. 4.12(c) shows the measured noise voltages. Compare Fig. 4.12(a), Fig. 4.12(b) and Fig. 4.12(c), the measurement results verify the prediction of (4.14) that the noise voltage has strong correlations with Imag Z, but weak correlations with Q. As Imag Z increases, the noise voltage also increases.

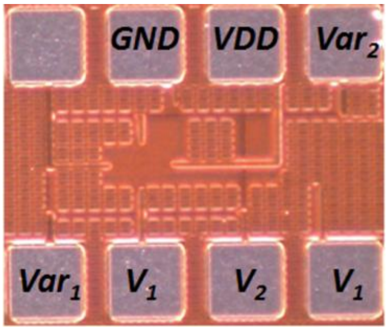


Figure 4.8 Microphotograph of the basic DAI.

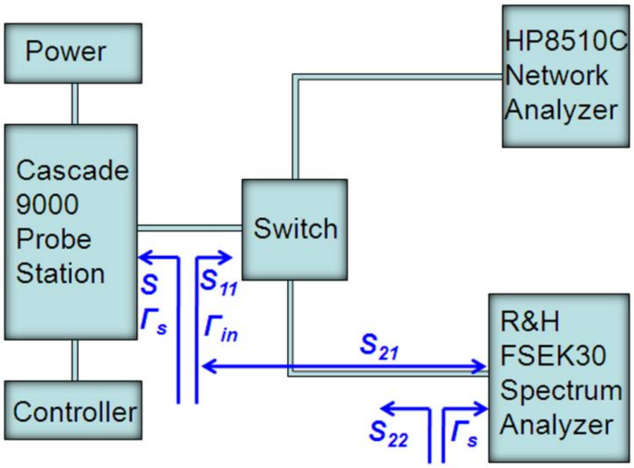


Figure 4.9 Inductor measurement arrangement.

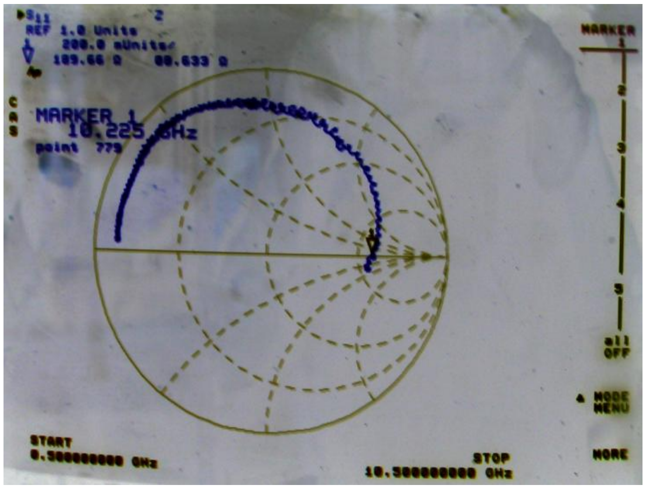


Figure 4.10 Measured smith chart with maximum self-resonant frequency.

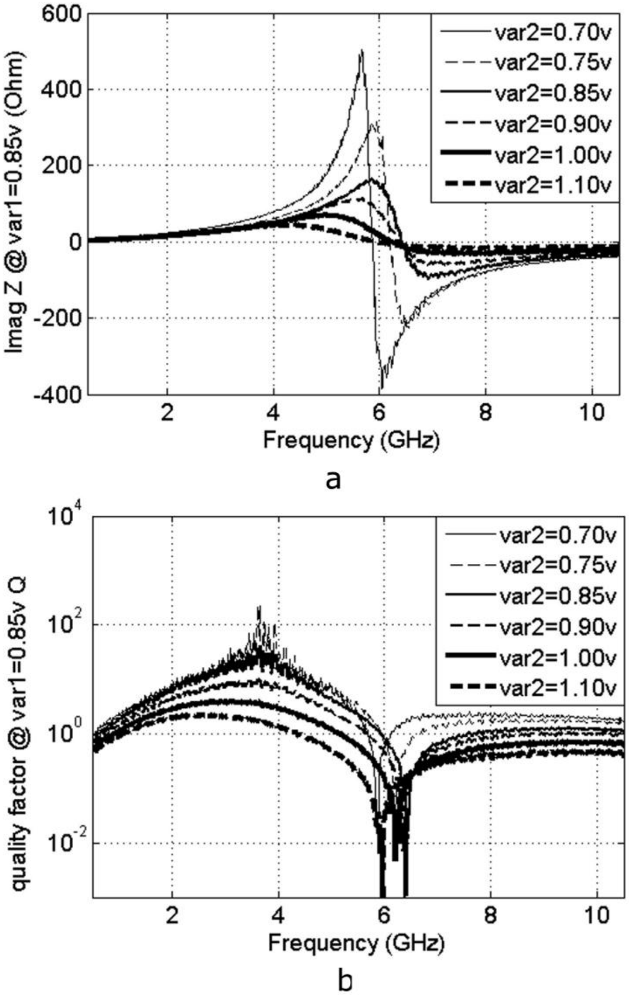


Figure 4.11 The measured relationship between var_2 and (a) Imag Z, (b) quality factor Q.

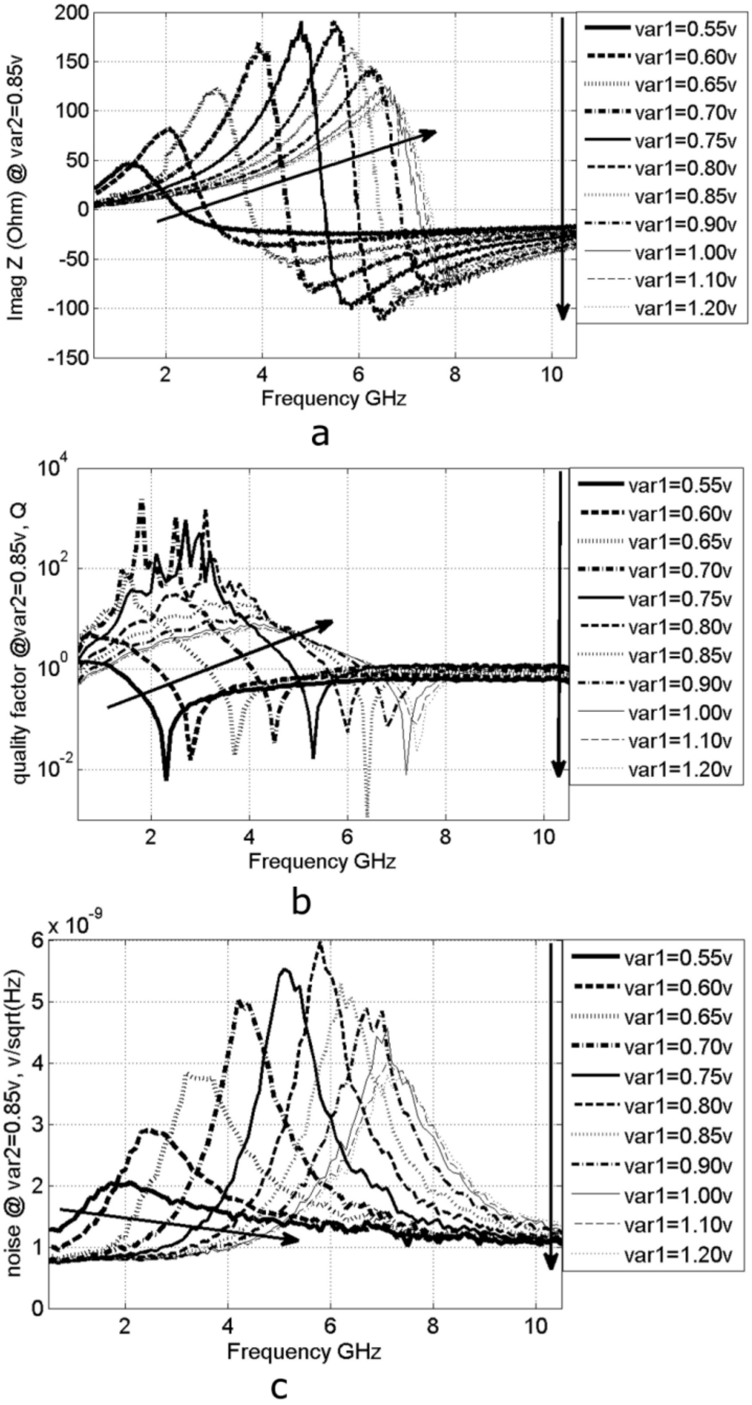


Figure 4.12 When var_2= 0.85 V and var_1 is tuned from 0.55 V to 1.20 V, measurement results of (a) Imag Z, (b) quality factor Q, (c) noise.

IV. CONCLUSION

We demonstrated a differential active inductor tunable from 500 MHz to 10.2 GHz. The obtained Q value is as high as 3000. The measured noise voltage does not exhibit direct correlations with quality factors as our analysis. The nonlinearity analysis shows that the active inductors are intrinsically nonlinear. A possible nonlinearity compensation circuit is proposed and simulated. The experimental results agree with theoretical analysis reasonably well. The inductor is a promising candidate for on chip communication circuit design.

REFERENCES

[4.1] Thomas H. Lee, “The Design of CMOS Radio-Frequency Integrated Circuits, Second Edition,” Cambridge University Press, 2003.

[4.2] Fei Yuan, “CMOS Active Inductors and Transformers principle, Implementation, and Applications”, Springer, 2008.

[4.3] Yue Wu, Xiaohui Ding, Mohammed Ismail, Hakan Olsson, “RF Band pass Filter Design Based on CMOS Active Inductors”, IEEE Trans. on Circuits and systems II: Analog and Digital Signal Processing, Vol. 50, No. 12, December 2003.

[4.4] Mohamed A. Y. Abdalla, Khoman Phang, George V. Eleftheriades, “Printed and Integrated CMOS Positive/Negative Refractive-Index Phase Shifters Using Tunable Active Inductors,” IEEE Trans. on Microwave Theory and Techniques, Vol. 55, No. 8, August 2007.

[4.5] Liang-Huang Lu, Hsieh-Hung Hsieh, Yu-Te Liao, “A Wide Tuning Range CMOS VCO with a Differential Tunable Active Inductor” IEEE Trans. on Microwave and Techniques, Vol. 54, No. 9, September 2006.

[4.6] M. U. Nair, Y. J. Zheng, Y. Lian, “1Vm 0.18μm area and power efficient UWB LNA utilizing active inductors,” Electronics Letters, Vol. 44, No. 19, September 2008.

[4.7] Tienyu Change, Jinghong Chen, Lawrence Rigge, Jenshan Lin, “A Packaged and ESD-Protected Inductorless 0.1-8 GHz Wideband CMOS LNA,” IEEE Microwave and Wireless Components Letters, Vol. 18, No. 6, June 2008.

[4.8] Chaojiang Li, Pingshan Wang, “A High Frequency Tunable Differential Active Inductor and Its applications to Power Dividers,” IEEE 51st Midwest Symposium on Circuits and Systems, 2008.

[4.9] Liang-Hung Lu, Yu-Te Liao, Chung-Ru Wu, “A Miniaturized Wilkinson Power Divider with CMOS Active Inductors,” IEEE Microwave and Wireless Components Letters, Vol. 15, NO. 11, November 2005.

[4.10] Hsieh-Hung Hsieh, Yu-Te Liao, Liang-Huang Lu, “A Compact Quadrature Hybrid MMIC Using CMOS Active Inductors”, IEEE Trans. on Microwave Theory and Techniques, Vol. 55, No. 6, June 2007.

[4.11] Thanachayanont, A., Payne, A., “CMOS floating active inductor and its applications to bandpass filter and oscillator designs”, IEE Proceedings, Circuits, Devices and Systems, p. 42-48, Feb, 2000.

[4.12] C. L. Ler, A. K. B. Aáin, and A. V. Kordesh, “CMOS source degenerated differential active inductor,” Electronics Letters, Vol. 44, no. 3, 2008.

[4.13] Chun-Lee Ler, Abu Khari bin Aáin Albert V. Kordesch, “Compact, High Q, and Low-Current Dissipation CMOS Differential Active Inductor”, IEEE Microwave and Wireless Components Letters, Vol. 18, No. 10, October 2008.

[4.14] A. A. Abidi, “Noise in Active Resonators and the Available Dynamic Range”, IEEE Trans. on Circuits Systems-I: Fundamental Theory and Applications, Vol. 39, No. 4, April 1992.

[4.15] Markus Dillinger, Kambiz Madani, Nancy Alonistioti, “Software Defined Radio: Architectures, Systems and Functions,” Wiley, July 2003.

[4.16] Aldert Van der Ziel, “Noise in Solid State Devices and Circuits”, John Wiley & Sons, Inc, 1986.

[4.17] David M. Pozar, “Microwave Engineering, third Edition”, John Wiley & Sons, Inc. 2005.

[4.18] Jeong Geun Kim, Gabriel M. Rebeiz, “Miniature Four-Way and Two-Way 24 GHz Wilkinson Power Dividers in 0.13 μm CMOS,” IEEE Microwave and Wireless Components Letters, Vol. 17, No. 9, September 2007.

[4.19] J. Reed, G. J. Wheeler, “A Method of Analysis of Symmetrical Four-Port Networks,” IRE Trans. on Microwave Theory and Techniques, Vol. MTT-4, p. 246-252, October, 1956.

[4.20] Kutner, Nachtsheim, Neter, Li, “Applied Linear Statistical Models, Fifth Edition”, McGraw-Hill Higher Education, 2004.

CHAPTER FIVE

A NOVEL SIX-PORT CIRCUIT BASED ON FOUR QUADRATURE HYBRIDS

Abstract: A novel six-port circuit is proposed and demonstrated. The circuit is based on four quadrature hybrids. A prototype circuit is fabricated and characterized with microstrip lines. Reflection coefficients for a few loads are measured with the fabricated circuit to evaluate its performance. The results agree with those from an HP8510C network analyzer reasonably well. Using active inductors and varactors, the six-port circuit is also designed with a 0.13 μm CMOS process. The simulated results show that the operating frequency is tunable from 1 GHz to 6.8 GHz.

I. INTRODUCTION

A six-port circuit, shown in Figure 5.1, is an essential component of a six-port reflectometer (SPR) [5.1]-[5.2], which measures the complex reflection coefficient of a device-under-test (DUT) at port 2. The measurement is performed by measuring the power P_i at the other four ports [5.2], where

$$P_i = |K_i|^2 |b_2|^2 |\Gamma_L - q_i|^2 , i = 3,5,6 \quad . \tag{5.1}$$

K_i is a coefficient determined by power levels, Γ_L is the reflection coefficient to be measured, and complex q_i is SPR q-point, which determines measurement accuracy [5.1]. Ideally, the magnitude of q_i should be ~ 1.5; the argument differences between two q-points should be ~120^0 [5.1]. In practice, 45^0 or larger argument differences are considered acceptable [5.3]-[5.4].

The simple power detection approach makes SPR an attractive candidate for developing an on-chip vector network analyzer (VNA) [5.5], which is promising for broadband dielectric spectroscopy analysis in micro total analysis systems (μTAS) [5.6]-[5.7]. However, CMOS processes have limited chip area and large process variations (e.g. up to 25% of resistance variation for resistors in addition to parasitic capacitance). These constraints need to be considered in designing CMOS SPRs.

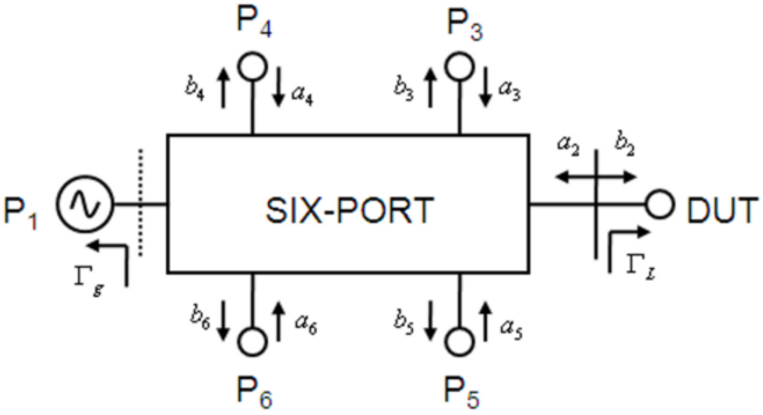


Figure 5.1 A six-port network. The parameters a_i, b_i, P_i are incident wave, reflected wave, and power at port i respectively.

Various six-port circuits have been proposed and implemented with distributed transmission lines, lumped elements or a mixture of both [5.2] - [5.4] [5.8] - [5.13]. For CMOS SPRs, only lumped elements are possible due to dimension constraints, even though distributed transmission line SPRs are conceptually straightforward to design with little power loss. The resistor-based SPRs are compact with operating frequency ranges which are much wider than that of distributed transmission line implementations, but signal loss due to resistors is high. For instance, about 75% of input power is lost in the network in [5.3]. The loss will degrade SPR sensitivity. Therefore, they are not optimal for CMOS implementation.

In this work, we propose a new six-port circuit that only uses four quadrature hybrids. Compared with Engen's classic six-port [5.2], the new circuit uses fewer components (i.e. without a directional coupler and two resistors) while keeping the similar q-point distribution and providing higher sensitivity. Therefore, the proposed six-port is more compact and suitable for integrations. The circuit is first demonstrated with microstrip line hybrids to evaluate its performance and then designed in a 0.13 μm CMOS technology with tunable lumped element hybrids. Our simulated results with Cadence Spectre show that the CMOS SPR has an operating frequency tunable from 1 to 6.8 GHz.

II. PROPOSED SIX-PORT CIRCUIT

The basic configuration of the proposed six-port circuit is shown in Figure 5.2. At the designed center frequency, the waves at each port are

$$b_2 = -\frac{jb}{2} \text{ and } \Gamma_L = \frac{a_2}{b_2} \quad , \tag{5.2}$$

$$b_3 = -\frac{b}{4}(\Gamma_L - (-2j)) \quad , \tag{5.3}$$

$$b_4 = \frac{b}{2} \quad , \tag{5.4}$$

$$b_5 = \frac{(1-j)b}{4\sqrt{2}}(\Gamma_L - (1+j)) \quad , \tag{5.5}$$

$$b_6 = \frac{-(1-j)b}{4\sqrt{2}}(\Gamma_L - (-1+j)) \quad . \tag{5.6}$$

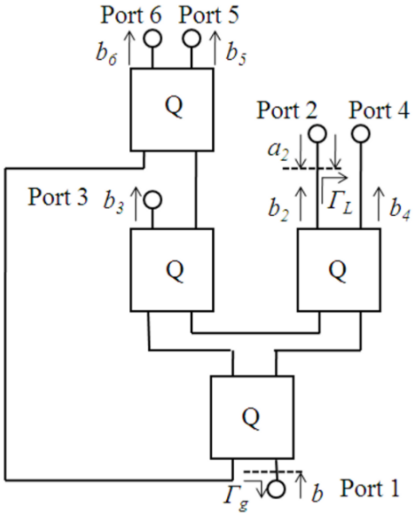


Figure 5.2 Schematic of the proposed six-port circuit

From Equations (5.1) to (5.6), the q points of the six-port are

$$q_3 = -2j = 2\angle 270^o \quad , \tag{5.7}$$

$$q_5 = 1 + j = \sqrt{2}\angle 45^o \quad , \tag{5.8}$$

$$q_6 = -1 + j = \sqrt{2}\angle 135^o \quad . \tag{5.9}$$

Therefore, the circuit satisfies the general six-port design criterion mentioned above [5.3]-[5.4]. Its q-point distribution is similar to that of the circuit in [5.2]. Furthermore, the power transmission coefficients from source to port i (i=2, 3, 4, 5, 6.) are: -6 dB for S_{21}, S_{31}, and S_{41}; -9 dB for S_{51} and S_{61}. The reflected power transmission coefficients from port 2 to port i (i=3, 5, 6) are $S_{32}=S_{52}=S_{62}= -6$ dB. Those coefficients are important since larger coefficient values imply higher signal to noise ratio for the detectors. Compared with the six-port in [5.2], the circuit in Figure 5.2 has 3 dB improvements in S_{31}, S_{41}, S_{52}, and S_{62}.

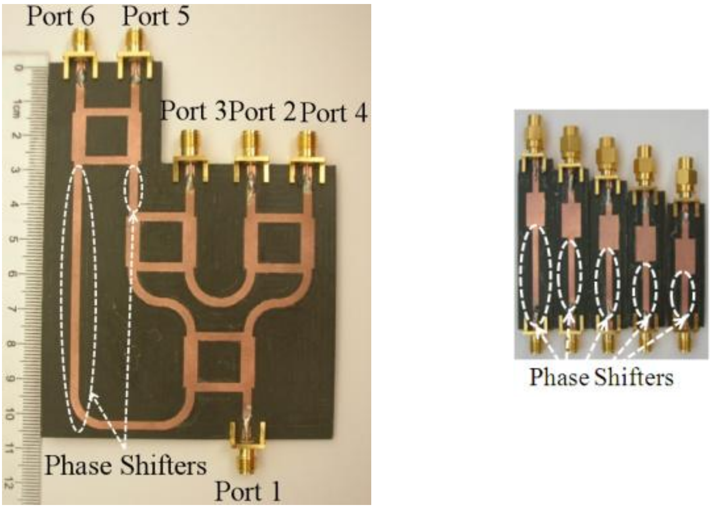
At frequencies other than the designed center frequency, q_i will deviate from the value given in (5.7)-(5.9), and the performance of six-port will deteriorate since it is determined by the q_i distribution [5.1]-[5.2].

III. EXPERIMENTS AND RESULTS

A: MIC Realization

To verify the functionality of the proposed six-port, a prototype circuit with 4 GHz center frequency is fabricated using Duroid RT/duroid 5870 substrate, shown in

Figure 5.3(a). For layout and measurement convenience, two phase shifters are used to avoid the intersection of two microstrip lines, as illustrated in Figure 5.3(a), while keeping the equivalent q-point distribution. This issue will not appear in CMOS implementation since there are different metal layers which can be used for connections.



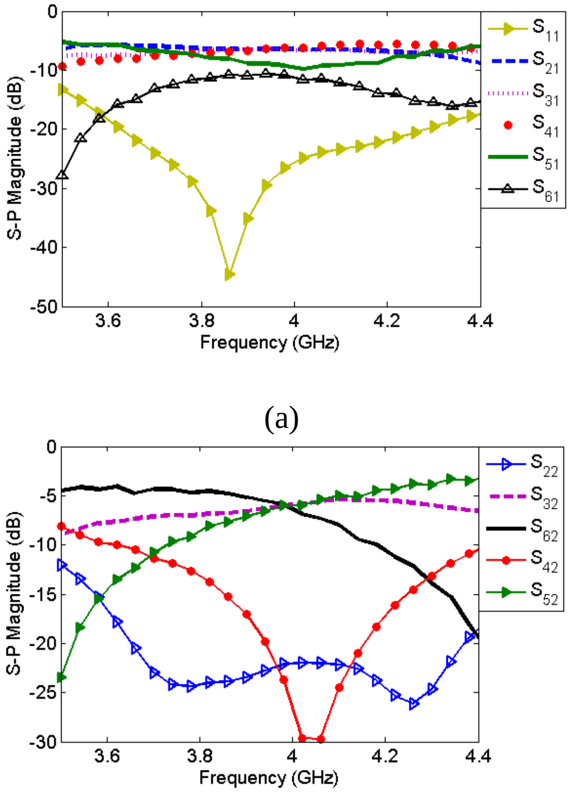
(a) (b)

Figure 5.3 (a) A photo of the prototype. (b) Calibration loads.

An HP 8510C network analyzer was used to measure the scattering parameters of the prototype circuit after a full two-port calibration. The measured S_{i1} and S_{i2} are shown in Figure 5.4. S_{42} presents reasonable isolation between port 2 and port 4. It satisfies the design criteria [5.1]. The measured values agree closely with the predicted values. The q-point distribution can be calculated from [5.14].

$$q_i = \frac{S_{i2} - (S_{i1} S_{22}) / S_{21}}{S_{i1} / S_{21}}, i = 3, 5, 6 \tag{5.10}$$

Figure 5.5 shows the calculated q-points with S-Parameters from measurements and simulations (with Agilent Advanced Design System (ADS)). If the phase differences between q_i are required to be larger than 45^0 [5.3]-[5.4], the operating frequency range is from 3.8 GHz to 4.3 GHz according Figure 5.5.



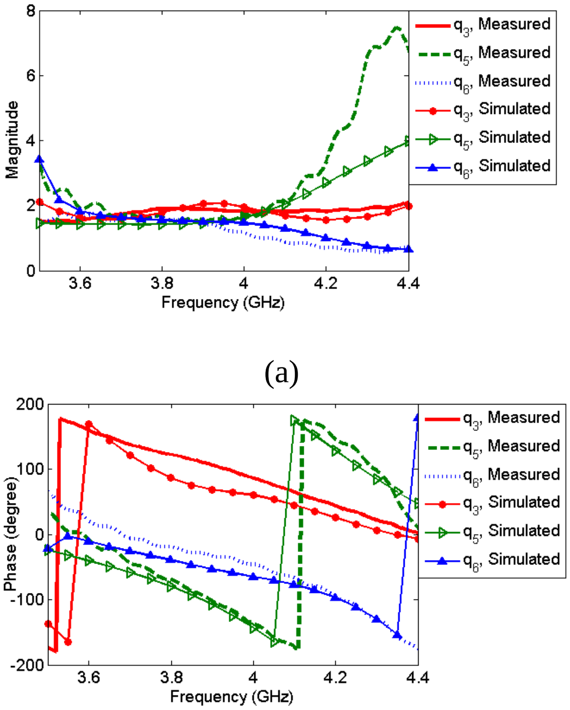
(a)

(b)

Figure 5.4 Measured S-parameters magnitude. (a) S_{i1}. (b) S_{i2}.

The calibration procedures described in [5.15]-[5.16] were followed and performed before measuring the reflection coefficients of 5 DUTs, which are made out of microstrip lines. The calibration loads shown in Figure 5.3(b) supply similar function as sliding loads. The six-port circuit is then used to measure the reflection coefficients of

DUTs, which are fabricated with microstrip lines. The power at port i (i=3, 4, 5, 6) were measured by use of 4 Gigatronics 8651A power meters with 80421A power sensors.



(a)

(b)

Figure 5.5 Q points (a) Magnitude (b) Phase.

Through calibration, the obtained q-point magnitudes are 2.06, 1.58, 1.37 and the argument differences are 120.8 °, 89 °and 150 °, which are close to the calculated values of equation (5.10). The measured reflection coefficients with the fabricated six-port are shown in Table 5.I. The results agree with those from direct measurements by an HP8510 C network analyzer reasonably well. Its operating frequency band is narrow due to the use of narrowband quadrature.

TABLE 5.1

COMPARISON OF THE REFLECTION COEFFICIENTS FOR DUTS MEASURED WITH THE PROPOSED SPR AND AN HP8510C AT 4GHZ

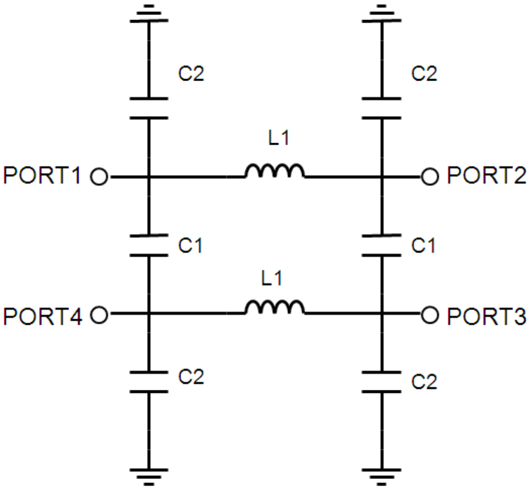
SPR	HP8510C	Difference
-0.3871+i0.6268	-0.397+i0.614	0.0099+i0.01281
0.1014+i0.6353	0.1115+i0.6141	-0.0101+i0.0212
0.3153-i0.481	0.2875-i0.4653	0.0278-i0.0157
-0.0772-i0.5748	-0.071-i0.5551	-0.0062-i0.0197
-0.0359-i0.5872	-0.0439-i0.5874	0.008+i0.0002

B: CMOS Design

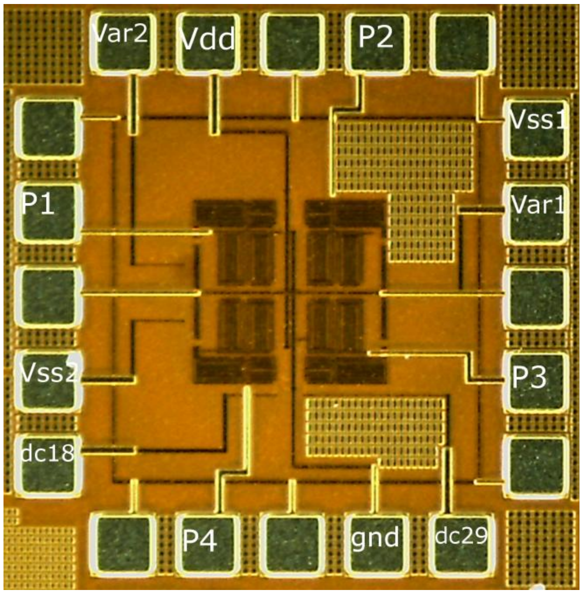
The proposed six-port circuit was also designed in a 0.13 μm CMOS process to verify its applicability in CMOS technologies. The operating frequency band can then be expanded by the introduction of tuning mechanism. The quadrature in Figure 5.2 was implemented with lumped elements [5.17], as shown in Figure 5.6(a). The parameters are given as

$$C_1 = \frac{1}{\omega_0 Z_0},\ L_1 = \frac{Z_0}{\omega_0 \sqrt{2}},\ C_2 = \frac{1}{\omega_0^2 L_1} - C_1 \quad , \tag{5.11}$$

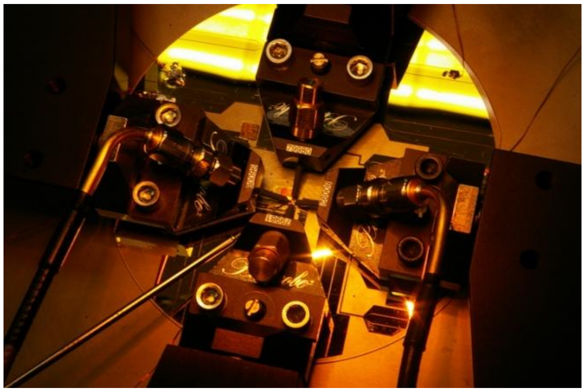
where $\omega_0 = 2\pi f$, f is the designed center frequency and Z_0 is the characteristic impedance.


C2
C2
L1
PORT1
PORT2
C1
C1
L1
PORT4
PORT3
C2
C2

(a)


Var2
Vdd
P2
Vss1
P1
Var1
Vss2
P3
dc18
P4
gnd
dc29

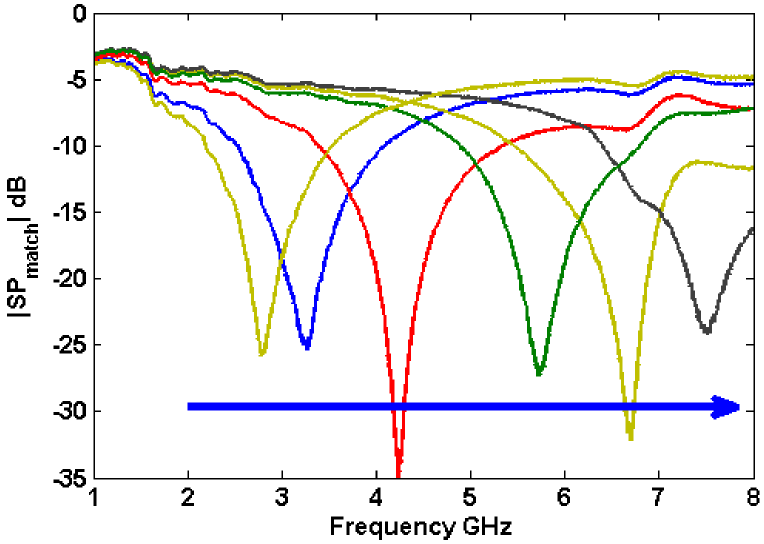
(b)



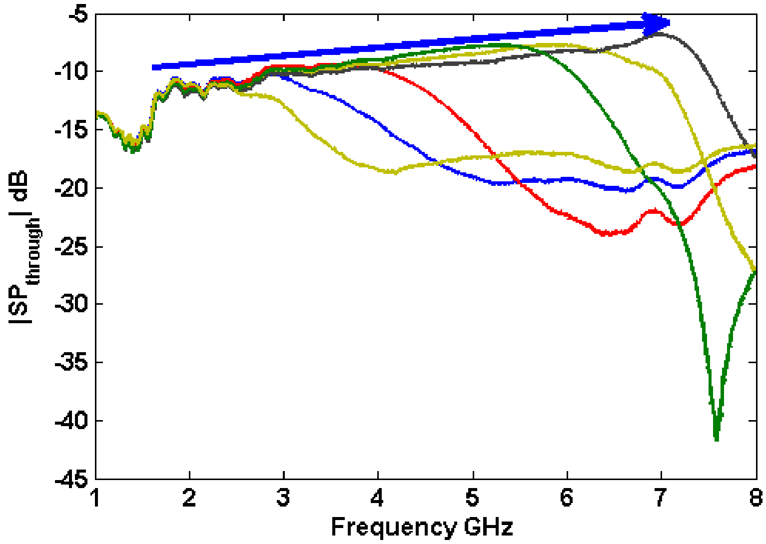
(c)

Figure 5.6 Lumped-element quadrature (a) Schematic of lumped-element quadrature. (b) Microphotograph of lumped-element quadrature. (c) Test bench for lumped-element quadrature.

Equation (5.11) shows that the center frequency of the quadrature can be tuned by varying inductances and capacitances. Consequently the center frequency (i.e. the operating frequency) of the SPR is tuned. As a result, the q-point distribution, i.e. measurement accuracy, at the center frequencies will be little affected over the SPR operating frequency range. To form the tuning mechanism, tunable active inductors [5.18] and standard varactors are used. Our measurement results of the tunable active inductors designed in the same 0.13 μm CMOS process as this chapter are close to the simulated results with maximum self-resonance frequencies up to 10.2 GHz. The microphotograph of the lumped-element quadrature is shown in Fig. 5.6(b) with an active area of 340 μm × 325 μm. The measured matching and through S-parameters are shown in Fig. 5.7 with a tuning range of 2 GHz-7.5 GHz.

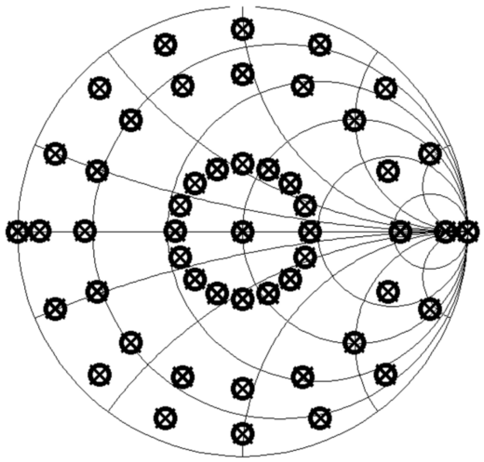


(a)

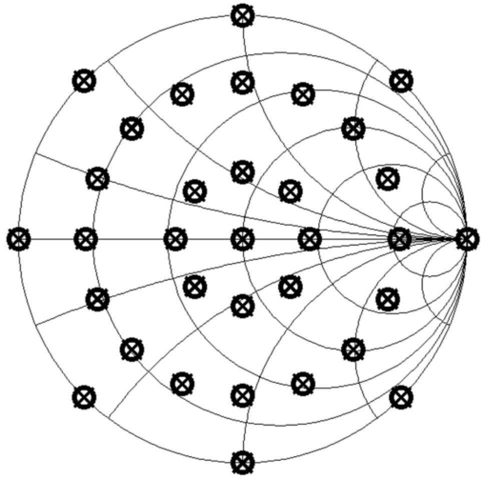


(b)

Figure 5.7 Measured results of Lumped-element quadrature (a) Matching S-parameter magnitude. (b) Through S-parameter magnitude.



(a)



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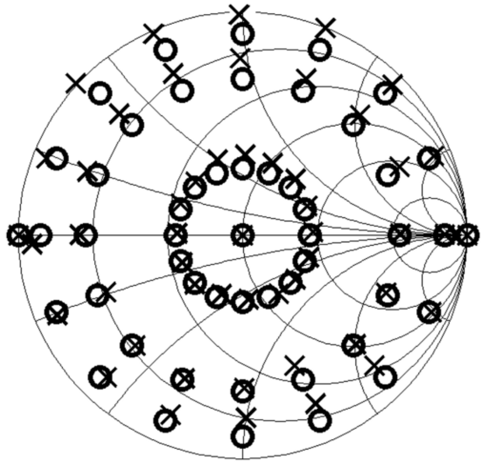
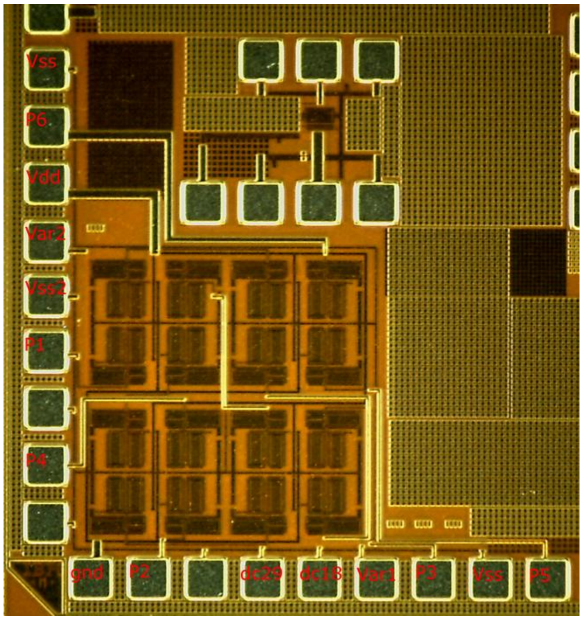


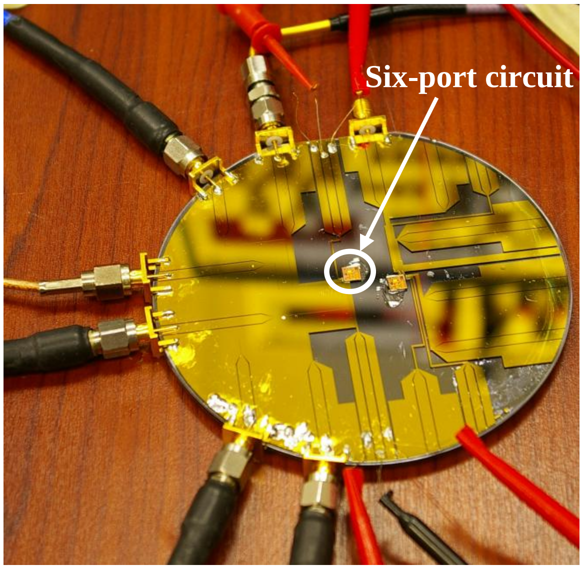
(c)

Figure 5.8 Simulated results (×) and expected results (O) of reflection coefficient at (a) 1 GHz, (b) 4 GHz, and (c) 6.8 GHz.

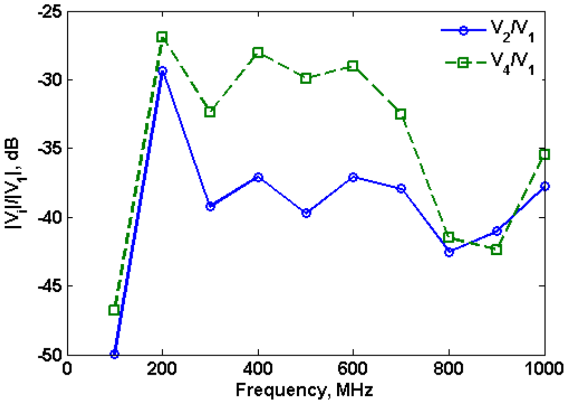
The two phase shifters which were used for connection in Fig. 5.3 are not used in CMOS six-port design. Then, the active area of the CMOS SPR is 750 μm × 750 μm. When different loads are connected to port 2 of the SPR, power at port i (i=3, 4, 5, 6) can be obtained in post-layout simulation analysis. Reflection coefficients can be obtained from the obtained power. The results are shown in Fig. 5.8(a), (b), and (c) for frequencies of 1 GHz, 4 GHz, and 6.8 GHz. The reflection coefficients agree with expected values reasonably well. The circuit was also implemented in a CMOS 0.13 μm process. The microphotograph is shown in Fig. 5.9(a). Due to the test equipment limitation, we cannot do on-chip test with G-S-G probe directly. A test bench shown in Fig. 5.9(b) was used. However, the loss caused by the CPW is about 1.68 dB/cm. The measured losses from port 1 to port 2 and port 4 are shown in Fig. 5.9 (c), and it shows that the loss is around 35 dB. Then the q-point distribution of the six-port was seriously affected. Furthermore, considering the nonlinearity of the active inductor in Chapter IV, the maximum input power should be smaller than -15 dBm. The maximum power reflected by DUT is about -50 dBm and the maximum reflected power into port 3 (or port 5, or port 6) is about -85 dBm, which is too small for our existing power measurement equipment.


Vss
P6
Vdd
Var2
Vss2
P1
P4
gnd
P2
dc29
dc18
Var1
P3
Vss
P5

(a)


Six-port circuit

(b)



(c)

Figure 5.9 CMOS six-port with active inductor (a) Microphotograph (b) Test bench (c) Measured loss from port 1 to port 2 and port 4.

Nonetheless, these simulated results show that the proposed six-port circuit is appropriate for on-chip integration and can provide wide operating frequency range.

IV. CONCLUSION

A novel six-port circuit based on four quadrature hybrids is proposed for CMOS integration applications. A prototype circuit was built with microstrip lines to evaluate the performance of the proposed structure. The reflection coefficients measured with the prototype six-port agree reasonably well with the results obtained from a commercial network analyzer HP8510C. The advantages of the proposed circuit include fewer circuit components and no need for matched loads, which are important for CMOS SPR implementations. The proposed circuit was also designed in a CMOS technology and simulated with Cadence Spectre. The simulated results show that the operating frequency range of the CMOS SPR can be tunable from 1 GHz to 6.8 GHz which is much wider than that of MIC SPR 3.8-4.3 GHz, but, it is narrower than the operating range of an active inductor 500 MHz to 10.2 GHz. We find that it is caused by the limited tuning range of the varactors. However, the measurement results show that the loss in the test bench is much larger, and then the q-points distribution of the six-port is distorted. So further work is needed to improve its operating frequency range, input dynamic range, and test bench for six-port system including power detection capability.

REFERENCES

[5.1] Glenn F. Engen, The six-port reflectometer: An alternative network analyzer, IEEE Trans. on Microwave Theory and Techniques, Vol. MTT-25, No. 12, p. 1075-1080, 1977.

[5.2] Glenn F. Engen, An improved circuit for implementing the six-port technique of microwave measurement, IEEE Trans. on Microwave Theory and Techniques, Vol. MTT-25, No. 12, p. 1080-1083, 1977.

[5.3] V. Bilik, V. Raffai, J. Bezek, Miniature Broadband Lumped Six-port Reflectometers, Journal on Communication, Vol. 42, p. 7-14, 1991.

[5.4] X. Z. Xiong, V. F. Fusco, Wideband 0.9GHz to 5 GHz six-port and its application as digital modulation receiver, IEE Proceedings-Microwave Antennas and Propagation, Vol. 150, p. 301-307, 2003.

[5.5] Cletus A. Hoer, A Network Analyzer Incorporating Two Six-Port Reflectometers, IEEE Trans. on Microwave Theory and Techniques, Vol. MTT-25, No. 12, p. 1070-1074, 1977.

[5.6] Petra S. Dittrich, Kaoru Tachikawa, Andreas Manz, Micro total analysis systems: Latest advancements and trends, Analytical Chemistry, Vol. 78, No. 12, p. 3887-3908, 2006.

[5.7] Hywel Morgan, Tao Sun, David Holmes, Shady Gawad, Nicolas G Green, Single cell dielectric spectroscopy, Journal of Physics D: Applied Physics, p. 61-70, 2007.

[5.8] William Kit Dean, Monolithic network analyzer, Ph.D. dissertation, Texas Tech University, December 1991.

[5.9] Ashraf S. Mohra, Six-port reflectometer based on four 00/1800 microstrip ring couplers, Microwave and optical technology letters, Vol. 40, No. 2, p. 167-170, 2004.

[5.10] R. Uttamatharin, R. Phromloungsri, V. Chamnanphrai, P. Sirisuk, M. Chongcheawchamanan, Design six-port Reflectometer based on inductively-compensated coupled lines, IEEE Asia-Pacific Conference on Communications, p. 323-326, 2007.

[5.11] Ji Jun Yao, Swee Ping Yeo, Six-port Reflectometer based on modified hybrid coupler, IEEE Trans. on Microwave Theory and Techniques, Vol. 56, No. 2, p. 493-498, 2008.

[5.12] Jan Hesselbarth, Frank Wiedmann, Bernard huyart, Two new six-port reflectometers covering very large bandwidths, IEEE Trans. on Instrumentation and Measurement, Vol. 46, No. 4, p. 996-969, 1997.

[5.13] Frank Wiedmann, Bernard Huyart, Eric Bergeault, Louis Jallet, New structure for a six-port Reflectometer in monolithic microwave integrated-circuit technology, IEEE Trans. on Instrumentation and Measurement, Vol. 46, No. 2, p. 527- 530, 1997.

[5.14] P. I. Somlo, J. D. Hunter, Microwave Impedance Measurement Chapter 7, Institution of Electrical Engineers, September 1985.

[5.15] Glenn F. Engen, Calibrating the six-port Reflectometer by means of sliding terminations, IEEE Trans. on Microwave Theory and Techniques, Vol. MTT-26, No. 12, p. 951-957, 1979.

[5.16] Ulrich Stumper, Finding initial estimates needed for the Engen method of calibrating single six-port Reflectometers, IEEE Trans. on Microwave Theory and Techniques, Vol. 38, No. 7, p. 946-949, 1990.

[5.17] Ryszard W. Vogel, Analysis and Design of lumped- and Lumped- Distributed-Element Directional Couplers for MIC and MMIC Applications, IEEE Trans. on Microwave Theory and Techniques, Vol. 40, No. 2, p. 253-262, 1992.

[5.18] Chaojiang Li, Pingshan Wang, A High Frequency Tunable Differential Active Inductor and Its Application to Power Dividers, IEEE International 51st Midwest Symposium on Circuits and Systems, p. 285-288, 2008.

CHAPTER SIX

A LOW POWER ACTIVE INDUCOR WITH IMPROVED Q-FACTOR AND ITS APPLICATION TO PHASE SHIFTER

Abstract— This chapter presents a low-power single-ended active inductor with its Q-factor enhanced by feedback. Without sacrificing the self-resonance frequency and increasing the DC power consumption of the main circuit, the feedback transistor introduces a negative resistance; therefore, high Q-factors can be achieved in a wide operating frequency range. The proposed inductor was designed in a 0.13 µm CMOS process and simulated using Cadence Spectre. The active area is ~4 µm × 5 µm. With ~ 0.1 mW power consumption, the designed active inductor shows a 17 GHz maximum self-resonance frequency and a 1-8 GHz peak-Q operating frequency range. Using this active inductor, a 3-bit digitally-controlled phase shifter was designed. The phase shifter can provide a phase shift range larger than 180 ° from 1.5 GHz to 4 GHz and a return loss better than 10 dB.

Key Words: Active inductor, feedback, high Q-factor, low-power, phase shifter

I. INTRODUCTION

CMOS active inductors have attracted much attention in RF/microwave circuit design because of their small chip area and wide tunability [6.1]-[6.4]. However, the operating conditions for low power consumption, high Q factor, and high self-resonance frequency (SRF) often conflict with each other. In other words, it is difficult to achieve high Q-factors in a wide operating frequency range, especially at high frequencies with a given power consumption constraint. To address this issue, a lot of work has been done. A current reuse single-ended active inductor with low power consumption, shown in Fig. 6.1(a), was proposed, analyzed, and demonstrated experimentally in [6.3]. But its Q-factor is intrinsically low since there is no self negative resistance generation mechanism. Boosting Q-factor with additional an external negative resistance circuit increases power consumption and lowers the SRF due to the increase of parallel capacitance in the equivalent circuit [6.3]. A structure was proposed in [6.4] to improve the Q-factor of the inductor in [6.3]. Simulations in [6.4] show that the improved inductor can operate up to 4 GHz with simulated Q-factors below 20. The resistor feedback technique increases the Q-factor, but the operating frequency bandwidth is narrow [6.5].

In this chapter, a new feedback technique is proposed to improve the Q-factor of the inductor in [6.3]. The proposed technique is analyzed with small signal models, and verified by simulated results with Cadence Spectre. The proposed active inductor is designed in a 0.13 μm CMOS process. It can achieve high Q-factors up to a few thousands from 1 GHz to 8 GHz with about 0.1 mW power consumption. One application example of the proposed active inductor, a 3-bit digitally-controlled phase shifter, is discussed and designed. It can provide more than 180° phase shift from 1.5 GHz to 4 GHz.

II. PROPOSED ACTIVE INDUCTOR STRUCTURE

The proposed active inductor structure is shown in Fig. 6.1(b) with a variant in Fig. 6.1(c). Compared with the conventional active inductor circuit in Fig. 6.1(a), a feedback transistor M_3 is introduced. Fig. 6.1(b) uses an NMOS feedback transistor, and Fig. 6.1(c) uses a PMOS feedback transistor. The currents flowing through the feedback transistors, i.e. I_2, should be much smaller than the currents flowing through the cascade transistors (i.e. I_1) to save power. Fig. 6.1(d) is a traditional inductor equivalent circuit. The performance of active inductor circuits shown in Figs. 6.1(a), 6.1(b), and 6.1(c) can be estimated by comparing their parameters in the equivalent circuit shown in Fig. 6.1(d).

The corresponding equivalent circuit parameters of the proposed active inductors in Figs. 6.1(b) and 6.1(c) can be determined through small signal model analysis, and they are depicting as (6.1).

$$
\begin{aligned}
\frac{1}{Z} &= sC_{equ} + \frac{1}{R_{equ1}} + \frac{1}{R_{equ2} + sL_{equ}} \\
C_{equ} &\approx C_{gs2} \\
\mathrm{R}_{equ1} &\approx \frac{C_A r_{o2} + C_B\left(r_{o2} + r_{o3} + g_{m3} r_{o2} r_{o3}\right)}{\left(g_{m2} + \dfrac{1}{r_{o2}}\right)\left(C_A r_{o2} + C_B\left(r_{o2} + g_{m3} r_{o2} r_{o3}\right)\right)} \\
\mathrm{R}_{equ2} &\approx \frac{r_{o2} - \omega^2 C_A C_B r_{o2}^2 r_{o3}}{\left(g_{m2} r_{o2} + 1\right)\left(g_{m1}\left(g_{m3} r_{o3} + 1\right) r_{o2} - 1\right)} \\
L_{equ} &\approx \frac{r_{o2}\left(C_A r_{o2} + C_B\left(r_{o2} + r_{o3} + g_{m3} r_{o2} r_{o3}\right)\right)}{\left(g_{m2} r_{o2} + 1\right)\left(g_{m1}\left(g_{m3} r_{o3} + 1\right) r_{o2} - 1\right)}
\end{aligned}
\qquad (6.1)
$$

where C_A and C_B are the parasitic capacitance at nodes A and B, respectively; r_{oi} and g_{mi} are the output resistance and transconductance of M_i, respectively. The self-resonance frequency (SRF) can be estimated with

$$SRF \approx \sqrt{\frac{\left(g_{m2}r_{o2}+1\right)\left(g_{m1}\left(g_{m3}r_{o3}+1\right)r_{o2}-1\right)}{C_{gs2}r_{o2}\left(C_A r_{o2}+C_B\left(r_{o2}+r_{o3}+g_{m3}r_{o2}r_{o3}\right)\right)}} \quad . \qquad (6.1)$$

Equation (6.1) shows that, by introducing the feedback transistor M_3, resistance R_{equ1} increases and a negative resistance R_{equ2} related to M_3 is generated. Equation (6.1) also indicates that as g_{m3} r_{o3} increase, both the inductance L_{equ} and the absolute value of the negative resistance R_{equ2} increase, so does the Q-factor. Furthermore, M_3 does not introduce any additional equivalent parallel capacitance, which would reduce the self-resonance frequency according to equation (6.2). As a result, the proposed active inductor can achieve a high self-resonance frequency and a high Q-factor with low-power consumption. Additionally, the addition of M_3 does not affect the input dynamic range. The main drawback is the additional noise introduced by M_3.

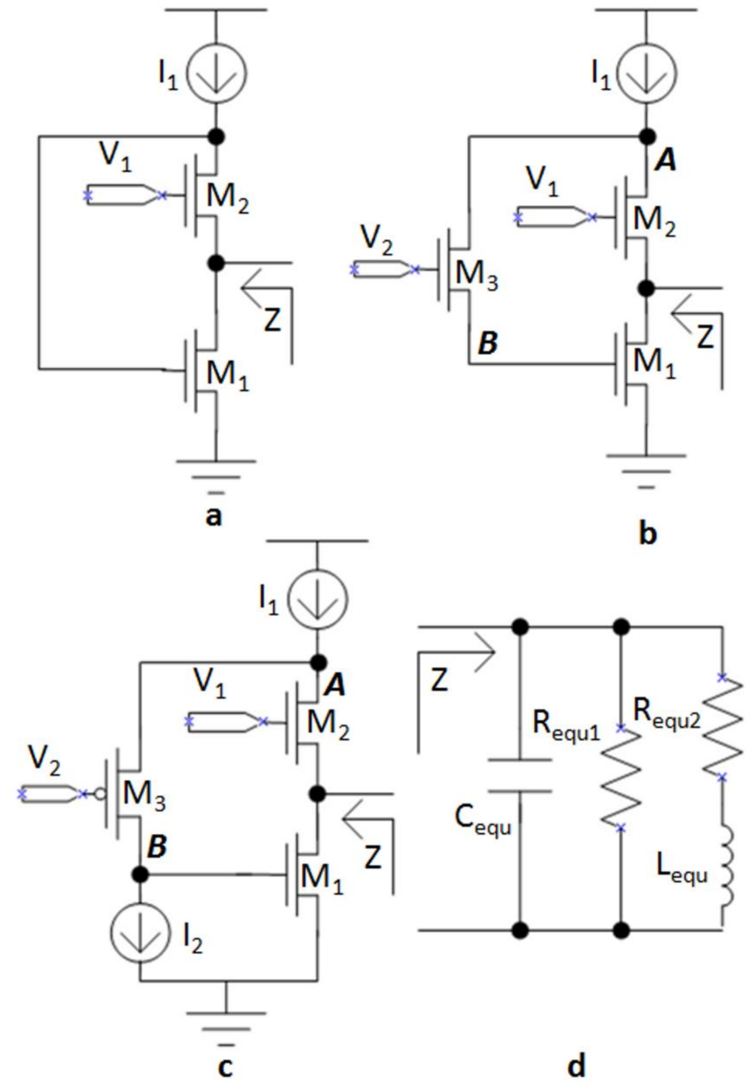


Figure 6.1. (a) Active inductor in [6.3]; (b) Proposed high-Q active inductor with NMOS feedback; (c) Inductor with PMOS feedback; (d) An equivalent inductor model.

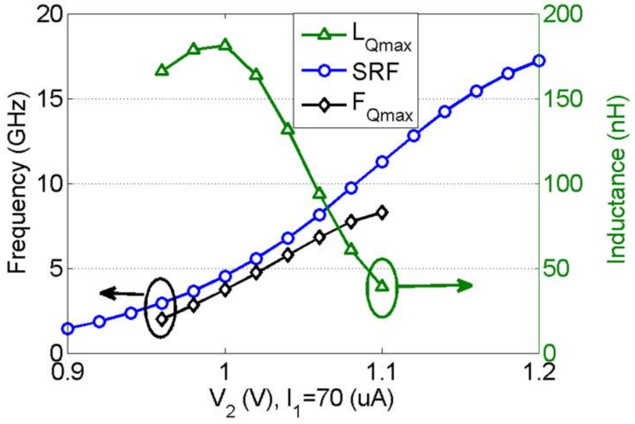
III. DESIGN REALIZATION AND SIMULATION

The proposed active inductor in Figs. 6.1(b) and 6.1(c) are designed and simulated in a 0.13 µm CMOS process using the Cadence Spectre simulator. The widths (W) of transistors M_1, M_2, and M_3 are 2.6 µm, 2 µm, and 1 µm, respectively. The channel length for all transistors (L) is 0.12 µm, and the active area is 4 µm × 5 µm.

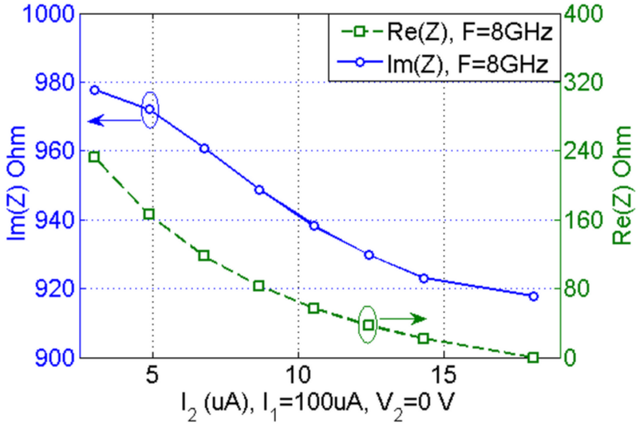
When current I_1 is 70 μA and power supply voltage is 1.2 V, the simulated results in Fig. 6.2(a) demonstrate a maximum SRF up to 17 GHz. The maximum peak-Q frequency, where the equivalent resistance Re(Z)≈0, F_{Qmax}, is 8 GHz. The simulated results, Re(Z)≈0, indicate high Q-factors up to a few thousands. The F_{Qmax} can be tuned from ~1 GHz to 8 GHz, which covers most of the present commercial communication frequencies and is much wider than the peak-Q operating frequency range in [6.2]-[6.5]. The inductance L_{Qmax} corresponding to the F_{Qmax} is also shown in Fig. 6.2(a). It shows that the inductance value of the active inductor is sensitive to the bias voltage V_2, about 1 nH/mV. This provides sufficient inductance tenability. One the other hand, it indicates that a stable voltage source V_2 is required, such as on-chip voltage sources [6.6]. Simulations show that the sensitivity can be reduced by increasing the size of M_3 at the expense of self-resonance frequency and chip area. Therefore, tradeoffs among the control voltage source V_2, inductor frequency performance, and transistor sizes in Fig. 6.1(b) are needed.

Fig. 6.2(b) is the simulated Im(Z) and Re(Z) versus I_2 with a power consumption constraint of 0.12 mW for the circuit shown in Fig. 6.1(c). It indicates that the Re(Z) can be tuned close to Zero through increasing I_2.

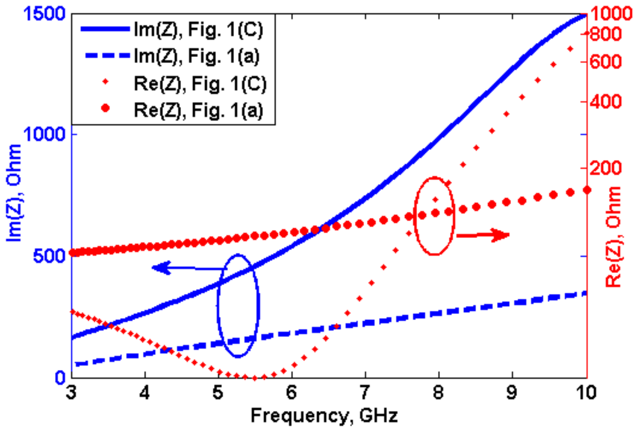
To compare the performance of the inductors, Fig. 6.2(c) shows simulated results of the circuits in Fig. 6.1(a) and 6.1(c) with the same current (95 μA) passing through transistors M_1 and M_2. It clearly shows that the equivalent inductance increases and the equivalent resistance decreases with the addition of M_3 in Fig. 6.1(c), as indicated by our small signal analysis in section 2. In other words, the Q-factor of the proposed inductor is increased.



(a)



(b)



(c)

Figure 6.2 Simulated results: (a) The tuning characteristics of the circuit in Figure 6.1(b); (b) The impedance of the circuit in Figure 6.1(c), (c) A comparison of the circuits in Figure 1(a) and 1(c) under the same conditions, I_1=100 uA, I_2=5 uA, V_2=0 V.

A series of simulations were conducted for the circuit shown in Fig. 6.1(c). Fig. 6.3 shows the output generated by Monte Carlo analysis in Cadence Spectre with 500 runs when I_1 is 100 uA, I_2 is 15 uA, and V_2 is 0 V. Fig. 6.3(a) shows the distribution of Im(Z) at 8 GHz. The mean of the Im(Z) is 929 ohm with a standard deviation of 145 ohm. The mean of Re(Z) across 500 runs at 8 GHz is 9.1 ohm and the standard deviation is 5.6 ohm. Similar process variation effects on the circuit in Fig. 6.1(b) are expected since its operating principle and structure is similar to the circuit in Fig. 6.1(c). Nevertheless, the process variation effects can be overcome by tuning the bias voltages.

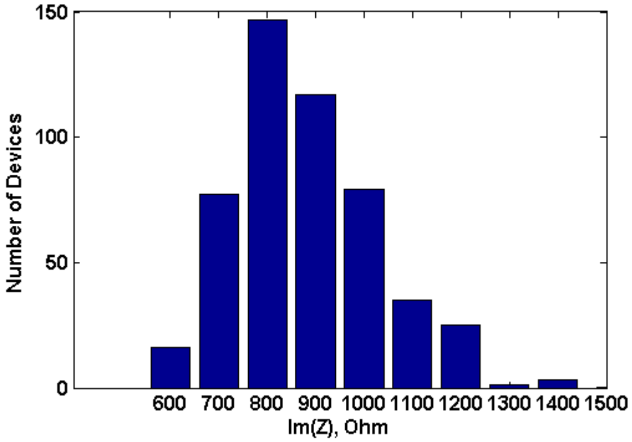


Figure 6.3 Monte Carlo simulation results of process variation effects on inductance of the circuit shown in Figure 6.1 (c) with 500 runs at 8 GHz when I_1=100 uA, I_2=15 uA, V_2=0 V.

IV. APPLICATION TO DIGITALLY-CONTROLLED PHASE SHIFTER

To further demonstrate the performance and applicability of the proposed circuits, the proposed active inductor is used to realize a phase shifter with wide frequency band. A 3-bit digitally-controlled phase shifter, Fig. 6.4(a), is proposed and designed with the active inductors discussed in Section 2. Fig. 6.4(b) is a conventional high-pass phase shift cell. A fixed Metal-Insulator-Metal (MIM) capacitor (C_H), instead of a varactor, is used due to insertion loss considerations [6.7]. However, the use of a fixed C_H limits the phase shift range although our proposed active inductor can operate in a much wider operating frequency range and with a larger inductance tuning range. Simulated results indicate that a single phase shift cell in Fig. 6.4(b) can only provide ~40 ° phase shift at the designed center frequency under matching conditions. Therefore, the digital control technique is exploited to extend the phase shift range. The diagram of the phase shifter is shown in Fig. 6.4(a).

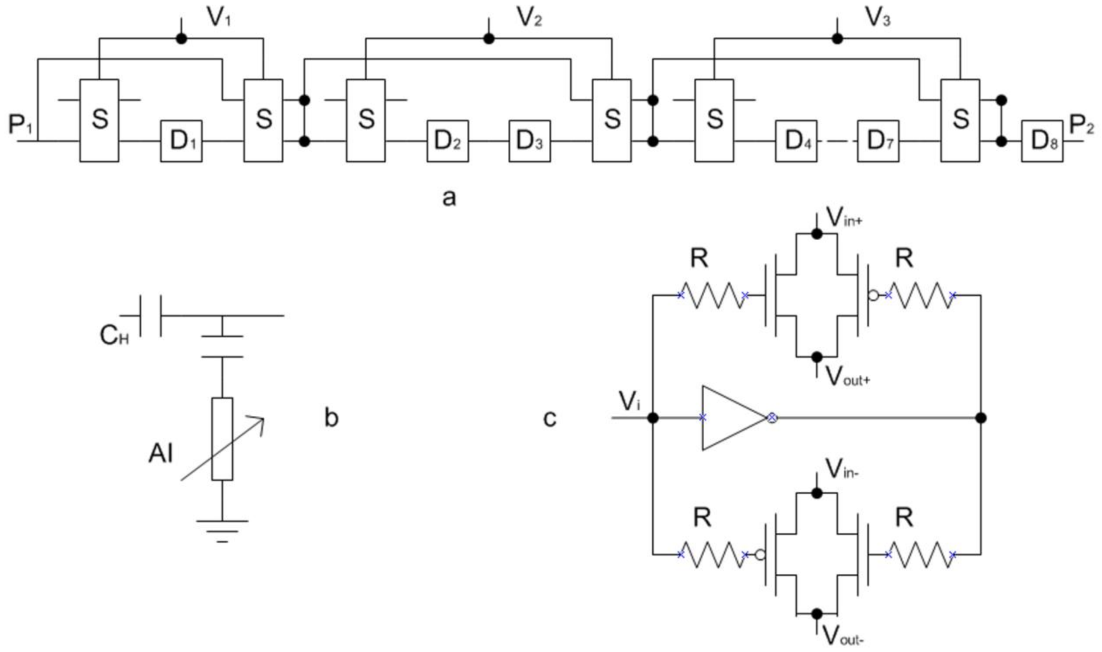


Figure 6.4 (a) A phase shifter; (b) A phase shift cell (D in (a)); (c) The switch (S in (a)).

Fig. 6.4(c) is the switch used in Fig. 6.4(a). To minimize the insertion loss caused by the switch, the switch transistor size should be large. Then, the gate-drain/source parasitic capacitors are large. To reduce the coupling from the signal path to ground caused by the parasitic capacitors, resistors are added on purpose at the gates of the transistors in switch transistors as shown in Fig. 6.4(c).

In Fig. 6.4(a), there are three digital inputs (V_3, V_2, V_1) acting as coarse phase shift controllers. They control exactly the 8 phase shift cells. For example, digital input (0, 0, 0) means only one phase shift cell works, and (1, 1, 1) means all 8 phase shift cell work. The fine phase shift controller is I_1 and I_2, which tunes the inductance value and Q-factor.

When the return loss (S_{11}) and the insertion loss (S_{21}) are set to be better than -10 dB and -4 dB, respectively, the simulated results are shown in Fig. 6.5. It indicates that the phase shifter can provide a phase shift range larger than 180 ° from 1.5 GHz to ~4 GHz by controlling digital inputs (V_3, V_2, V_1) and tuning the current source I_1. The power consumption is less than 0.96 mW, which is much lower than 31.5 mW in [6.7]. If the high-pass capacitor C_H can be tunable, a wider operating frequency range can be achieved. One possible application of this phase shifter is for on-chip six-port calibration, in which sliding loads are needed [6.8].

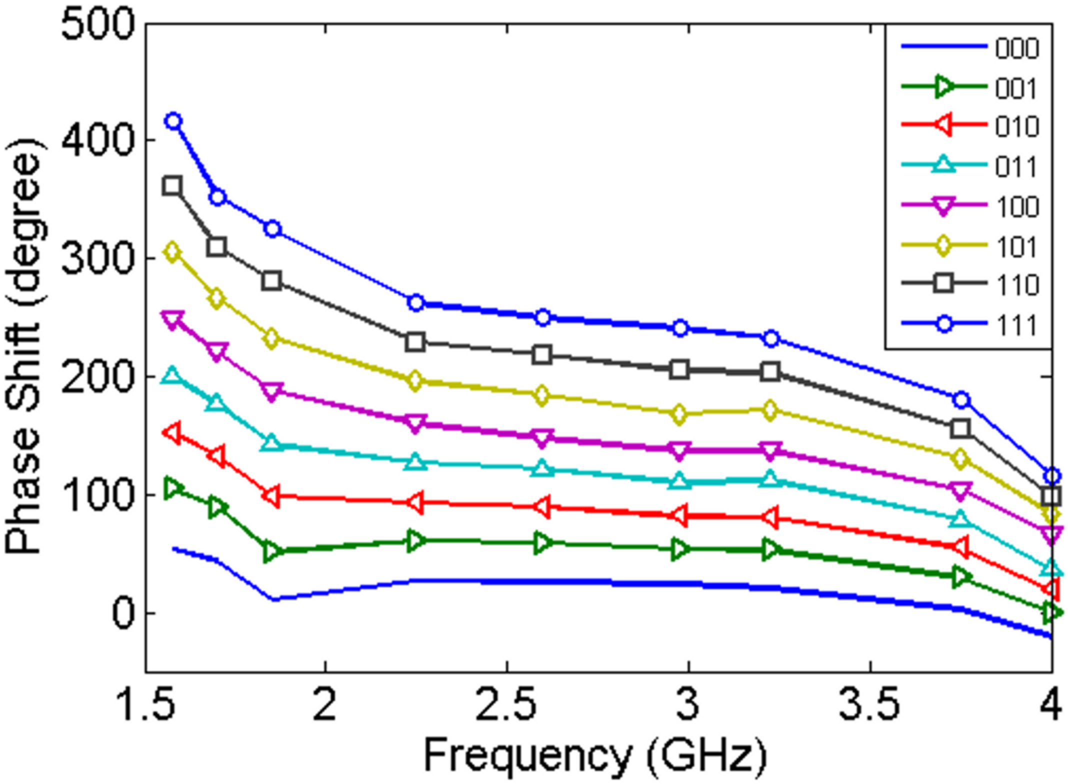


Figure 6.5 Simulated results of tunable phase range with digital control (V_3, V_2, V_1).

V. DISCUSSION AND CONCLUSION

A tunable, low-power, high-Q, single-ended active inductor is proposed and designed in this work. By introducing a feedback transistor, a negative resistor is generated and therefore the Q-factor can be increased to a few thousands without additional DC power consumption. The simulated results also verify that the equivalent resistance can be tuned close to zero when operating frequency is lower than 8 GHz. In other words, extremely high Q-factors up to a few thousands can be achieved. The maximum self-resonance frequency of the inductor is about 17 GHz. The Monte Carlo analysis results show that the proposed structure is reasonable stable. Since the performance of the proposed structure is sensitive to the bias voltage, a high precision and well-controlled bias voltage source is needed. To demonstrate the application of the proposed active inductor, a 3-bit digitally-controlled phase shifter using the proposed active inductor is designed. It can provide a phase shift range larger than 180 ° from 1.5 GHz to 4 GHz.

REFERENCES

[6.1] Thanachayanont, A., Payne, A., “VHF CMOS Integrated Active Inductor,” Electroncs Letters, vol. 32, no. 11, pp. 999–1000, 1996.

[6.2] M. M. Reja, I. M. Filanoovsky, K. Moez, “Wide Tunable CMOS Active Inductor,” Electronics Letters, vol, 44, no. 25, pp. 1461–1463, 2008.

[6.3] Yue Wu, Xiaohui Ding, Ismail, M., Olsson, H., “RF Bandpass Filter Design Based on CMOS Active Inductors,” IEEE Trans. Circuits and Syst. II: Analog and Digital Signal Process, vol. 50, no. 12, pp. 942–949, 2003.

[6.4] A. Tang, F. Yuan, E. Law, “A New constant-Q CMOS active inductor with applications to low-noise oscillators,” Analog Integrated Circuits and Signal Processing, Vol. 58, pp. 77-80, 2009.

[6.5] Chaochih, Hsiao, Chinwei Kuo, Chienchih Ho, Yijen Chan, “Improved Quality-Factor of 0.18um CMOS Active Inductor by a Feedback Resistance Design,” IEEE Microwave and Wireless Components Letter, vol. 12, no. 12, pp. 467–469, 2002.

[6.6] Adriana Becker-Gomez, T. Lakshmi Viswanathan, T. R. Viswanathan, “A Low-Supply-Voltage CMOS Sub-Bandgap Reference,” IEEE Trans. on Circuits and Systems-II: Express Briefs, Vol. 55, No.7, July 2008.

[6.7] M. A. Y. Abdalla, K. Phang, G. V. Eleftheriades, “Printed and Integrated CMOS Positive/Negative Refractive-Index Phase Shifters Using Tunable Active Inductors,” IEEE Trans. MTT, 2007, vol. 55, no. 8, pp. 1611–1623, 2007.

[6.8] C. Li, H. Zhang, P. Wang, “A Novel Six-Port Circuit Based on Four Quadrature Hybrids,” Int. J. RF Microwave Comput.-Aided Eng., vol. 20, no. 1, pp. 128–132, 2010.

CONCLUSION

This work investigated the circuit modules for CMOS six-port measurement system, including a source generator, which can be implemented by a voltage controlled ring oscillator, power detectors, a six-port circuit, and a phase shifter for six-port calibration.

In chapter II, the oscillation frequency and waveform amplitude expressions for a differential N-stage ring oscillator are derived with large signal analysis. The equations derived from the this new platform can explain the nonlinearity phenomena, such as delay time t_d versus stage number N, and waveform amplitude V_p versus tail current I_{ss} or load resistance R_{load}. The equations can be used to guide the voltage controlled ring oscillator design, such as the tradeoffs among power consumption, area, frequency, output power, and phase noise requirements.

In chapter III, a low power wideband power detector with embedded amplifier was proposed, designed, and measured. First, in the conventional power detector system, the input matching network is off chip and not convenient. So, a 0.5 GHz – 20.5 GHz quasi T-coil input matching network saving about 50% area was first proposed and analyzed. Furthermore, there is less loss in quasi T-coil matching network compared with the conventional T-coil network. Second, an amplifier is embedded in the power detector system rather than following it in the conventional power detector system. Simultaneously, the power consumption is decreased and the sensitivity is increased by introducing the embedded amplifier.

A novel six-port circuit saving about 20% area is proposed in chapter V, while keeping similar sensitivity when it is compared with the conventional structure. This structure is analyzed and verified by a prototype circuit based on transmission line techniques. To implement this six-port circuit in CMOS technology, lumped-element technology was used. To introduce the tuning mechanism for expanding the operating frequency range, an active inductor is needed. So a novel differential active inductor with 10.2 GHz self resonance frequency is proposed, analyzed, and designed in chapter IV. The measured results show that the operating frequency range satisfies the design requirement. The potential issues are the input dynamic range and intrinsic nonlinearity, which still need further work and improvement. The CMOS six-port with the proposed active inductors in chapter IV was also fabricated and measured. Due to the limitation of the measurement equipment, a test bench was designed. However, the loss in the test bench seriously shifts the q-point of the six-port system. Advanced equipment and a test bench with low loss are required in further work.

Finally, a tunable phase shifter was also designed to be used for calibration loads. To implement the phase shifter, a low-power 1GHz – 8 GHz high Q-factor active inductor was proposed and verified by simulated results. The Q-factor of the proposed active inductor was improved by introducing a feedback transistor based on the conventional single ended structure. The only drawback of the proposed structure is the additional noise by the feedback transistor.

APPENDIX A

Assume all the gate-induced and channel-induced noise sources, I_{ngi} and I_{ndi} (i=1, …, 6), are independent, and the DAI are symmetrical, then according to the noise model in Fig. 4.2 for DAI circuit in Fig. 4.1a, the differential noise output introduced by each noise source can be calculated.

$$\overline{V_{out,ng1}^2} = \left| \frac{1}{s\left(C_1 + C_{gs1}\right) - g_{mA1} + \frac{1}{R_{s1} + sL_{s1}} + \frac{1}{R_{s2} + sL_{s2}}} \right|^2 \overline{I_{ng1}^2} \tag{A-1}$$

$$\overline{V_{out,nd1}^2} = \left| \frac{g_{m3} g_{m5}}{\left(g_{m3} + sC_{gs3}\right) sC_{gs3} \left(s\left(C_{gs1} + C_{gs5} + C_1\right) - g_{mA1} + \frac{1}{R_{s1} + sL_{s1}} \right)} \right|^2 \overline{I_{nd1}^2} \tag{A-2}$$

$$\overline{V_{out,ng2}^2} = \left| \frac{1}{s\left(C_1 + C_{gs1}\right) - g_{mA1} + \frac{1}{R_{s1} + sL_{s1}} + \frac{1}{R_{s2} + sL_{s2}}} \right|^2 \overline{I_{ng2}^2} \tag{A-3}$$

$$\overline{V_{out,nd2}^2} = \left| \frac{g_{m3} g_{m5}}{\left(g_{m3} + sC_{gs3}\right) sC_{gs3} \left(s\left(C_{gs1} + C_{gs5} + C_1\right) - g_{mA1} + \frac{1}{R_{s1} + sL_{s1}} \right)} \right|^2 \overline{I_{nd2}^2} \tag{A-4}$$

$$\overline{V_{out,ng3}^2} = \left| \frac{g_{m3}\left(g_{m5} + sC_{gs5}\right)}{sC_{gs5}\left(g_{m3} + sC_{gs3}\right)\left(s\left(C_1 + C_{gs1}\right) - g_{mA1} + \frac{1}{R_{s1} + sL_{s1}} + \frac{1}{R_{s2} + sL_{s2}}\right)} \right|^2 \overline{I_{ng3}^2} \tag{A-5}$$

$$\overline{V_{out,nd3}^2} = \left| \frac{g_{m5}C_{gs3}}{C_{gs5}\left(g_{m3} + sC_{gs3}\right)\left(s\left(C_1 + C_{gs1} + C_{gs5}\right) - g_{m5} - g_{mA1} + \frac{1}{R_{s1} + sL_{s1}}\right)} \right|^2 \overline{I_{nd3}^2} \tag{A-6}$$

$$\overline{V_{out,ng4}^2} = \left| \frac{g_{m3}\left(g_{m5} + sC_{gs5}\right)}{sC_{gs5}\left(g_{m3} + sC_{gs3}\right)\left(s\left(C_1 + C_{gs1}\right) - g_{mA1} + \frac{1}{R_{s1} + sL_{s1}} + \frac{1}{R_{s2} + sL_{s2}}\right)} \right|^2 \overline{I_{ng4}^2} \tag{A-7}$$

$$\overline{V_{out,nd4}^2} = \left| \frac{g_{m5}C_{gs3}}{C_{gs5}\left(g_{m3} + sC_{gs3}\right)\left(s\left(C_1 + C_{gs1} + C_{gs5}\right) - g_{m5} - g_{mA1} + \frac{1}{R_{s1} + sL_{s1}}\right)} \right|^2 \overline{I_{nd4}^2} \tag{A-8}$$

$$\overline{V_{out,ng5}^2} = \left| \frac{g_{m5}}{sC_{gs5}\left(s\left(C_1 + C_{gs1}\right) - g_{mA1} + \frac{1}{R_{s1} + sL_{s1}} + \frac{1}{R_{s2} + sL_{s2}}\right)} \right|^2 \overline{I_{ng5}^2} \tag{A-9}$$

$$\overline{V_{out,nd5}^2} = \left| \frac{1}{\left(s\left(C_1 + C_{gs1}\right) - g_{mA1} + \frac{1}{R_{s1} + sL_{s1}} + \frac{1}{R_{s2} + sL_{s2}}\right)} \right|^2 \overline{I_{nd5}^2} \tag{A-10}$$

$$\overline{V_{out,ng6}^2} = \left| \frac{g_{m5}}{sC_{gs5}\left(s\left(C_1 + C_{gs1}\right) - g_{mA1} + \frac{1}{R_{s1} + sL_{s1}} + \frac{1}{R_{s2} + sL_{s2}}\right)} \right|^2 \overline{I_{ng6}^2} \tag{A-11}$$

$$\overline{V_{out,nd6}^2} = \left| \frac{1}{\left(s\left(C_1 + C_{gs1}\right) - g_{mA1} + \frac{1}{R_{s1} + sL_{s1}} + \frac{1}{R_{s2} + sL_{s2}} \right)} \right|^2 \overline{I_{nd6}^2} \tag{A-12}$$

Since the noise sources are independent, the total output noise is

$$\begin{aligned} \frac{\overline{V_{total}^2}}{\Delta f} &= \sum_{i=1}^{6} \frac{\overline{V_{out,ngi}^2}}{\Delta f} + \sum_{i=1}^{6} \frac{\overline{V_{out,ndi}^2}}{\Delta f} \\ &\approx \sum_{i=1}^{6} \left| \frac{N_{ngi}}{\left(M_{ngi} + \frac{1}{R_{s1} + sL_{s1}} \right)} \right|^2 \frac{\overline{I_{ngi}^2}}{\Delta f} + \left| \frac{N_{ndi}}{\left(M_{ndi} + \frac{1}{R_{s1} + sL_{s1}} \right)} \right|^2 \sum_{i=1}^{6} \frac{\overline{I_{ndi}^2}}{\Delta f} \end{aligned} \tag{A-13}$$

where N_{ngi}, M_{ngi}, N_{ndi}, M_{ndi} are constants and can be determined by (A-1)-(A-12).