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INVESTIGATION OF TECHNIQUES FOR REDUCING UNINTENTIONAL ELECTROMAGNETIC EMISSIONS FROM ELECTRONIC CIRCUITS AND SYSTEMS

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INVESTIGATION OF TECHNIQUES FOR REDUCING UNINTENTIONAL
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Ho-Cheol Kwak
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ABSTRACT

This dissertation describes three independent studies related to techniques for reducing unintentional electromagnetic emissions from electronic circuits and systems. The topics covered are: low-inductance multi-layer ceramic capacitor for high frequency circuit board decoupling, the application of imbalance difference model to various circuit board and cable geometries, and balanced cable interface for reducing common-mode currents from power inverter.

The first chapter discusses the importance and the meaning of the connection inductance associated with MLCCs and analyzes the effect of plate orientation in MLCCs. It demonstrates that vertically oriented plates have no more or less inductance than horizontally oriented plates when the overall dimensions of the plate stack are similar. Decoupling capacitance options at the various levels of a high-speed circuit is investigated to determine the range of frequencies that decoupling at each level is likely to be is effective. Innovative low-inductance capacitive-stem capacitor configurations are described and their connection impedance is compared to that of standard surface-mounted capacitors.

The second chapter investigates the imbalance difference model that is a method for modeling how differential-mode signal currents are converted to common-mode noise currents. Various cable geometries to determine how well imbalance factor's values of DM-to-CM conversion compare to full-wave calculations are explored. The imbalance difference model can be applied to cables with more than two conductors are demonstrated.

The third chapter investigates the balanced cable interface for reducing common-mode currents from power inverter. The concept of a *balancing network* to reduce the common-mode currents on power inverter cables above 30 MHz is introduced. An experimental test set-up is used to demonstrate the effect of a balancing network on the common-mode current, differential-mode current and the common-mode rejection ratio on a balanced cable with an imbalanced termination. The balancing network is also evaluated using a 3-phase brushless DC motor driver to verify its effectiveness in a real application.

DEDICATION

This dissertation is dedicated to my family, especially…

To my wife, Deunyi Jeong for her support and sacrifice;

To my parents and parents-in-law for their love and encouragement;

To my sons, Dong-geon (Michael) and Hyesung (Gabriel) — may you also be motivated

and encouraged to reach your dreams.

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I can't imagine I can be here without my family's support. I really thank my parents and parents-in-law for their endless love and unconditional sacrifices for their children. I also can't forget my brother, sister-in-law, for their encouragement and support.

My special thanks go to my two sons, Dong-geon (Michael) and Hyesung (Gabriel), for giving me such a joy during the challenging period as a Ph.D. student. Most of all, I am deeply grateful to my wife, Deunyi Jeong. Without her love, prayer, patience, and dedicated support, I would not have been able to complete my Ph.D. works.

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CHAPTER ONE

EVALUATION OF LOW-INDUCTANCE CAPACITOR CONFIGURATIONS FOR
HIGH FREQUENCY CIRCUIT BOARD DECOUPLING

Abstract

In high-speed circuits, the value of the inductance associated with a connection to

a MLCC (Multi-Layer Ceramic Capacitor) is often more important than the nominal

value of the capacitor. This paper has four main sections. The first section discusses the

importance and the meaning of the connection inductance associated with MLCCs. The

second section analyzes the effect of plate orientation in MLCCs. It demonstrates that

vertically oriented plates have no more or less inductance than horizontally oriented

plates when the overall dimensions of the plate stack are similar. The third section

describes decoupling capacitance options at the various levels of a high-speed circuit (i.e.

on-die, on-package and on-board). This section describes how the geometries at each

level affect the relationship between connection inductance and resistance, and therefore

determine the range of frequencies that decoupling at each level is likely to be effective.

The fourth section describes innovative low-inductance capacitor configurations.

A capacitor having a stem that is designed to be inserted into a single, large-diameter via

hole drilled in a printed circuit board is described, wherein the stem may have conductive

rings for making the positive and negative connections to the printed circuit board power

distribution planes. Inside the capacitive stem, current, or at least a portion thereof, may

flow to the main body of the capacitor through low-inductance plates that are interleaved

to maximize their own mutual inductance and, therefore, minimize the connection

inductance. Alternately, the capacitor may include a coaxial stem that forms a coaxial transmission line with the anode and cathode terminals forming the inner and outer conductors. Capacitive-stem capacitor configurations are described and their connection impedance is compared to that of standard surface-mounted capacitors.

I. INTRODUCTION

A decoupling capacitor acts as a low impedance source of current to minimize supply voltage fluctuations caused by the rapid switching of active devices. Typically, the decoupling capacitance for silicon processors is implemented in multiple stages ranging from large bulk capacitors physically located near regulated power supplies, to board-level capacitors that stabilize the voltage supply on the printed circuit board (PCB), to package-level decoupling incorporated on the processor package, and die-level capacitance located on the die itself. This decoupling network regulates the current moving through the system between the silicon die and the regulated power supply. The required response time of the decoupling capacitors decreases as the current moves towards the processor. The impedance of the power distribution bus versus frequency can be equated to the decoupling capacitor response time. At relatively low frequencies, a low impedance is achieved with high capacitance (i.e., low capacitive reactance). At relatively high frequencies, low impedance is obtained by using capacitors with a low connection inductance. In between these frequency ranges, there is a series resonance. At resonance, the impedance is equal to the equivalent series resistance (ESR) of the capacitor. Therefore, to make a capacitor work at the highest possible frequencies, it should have the lowest possible connection inductance.
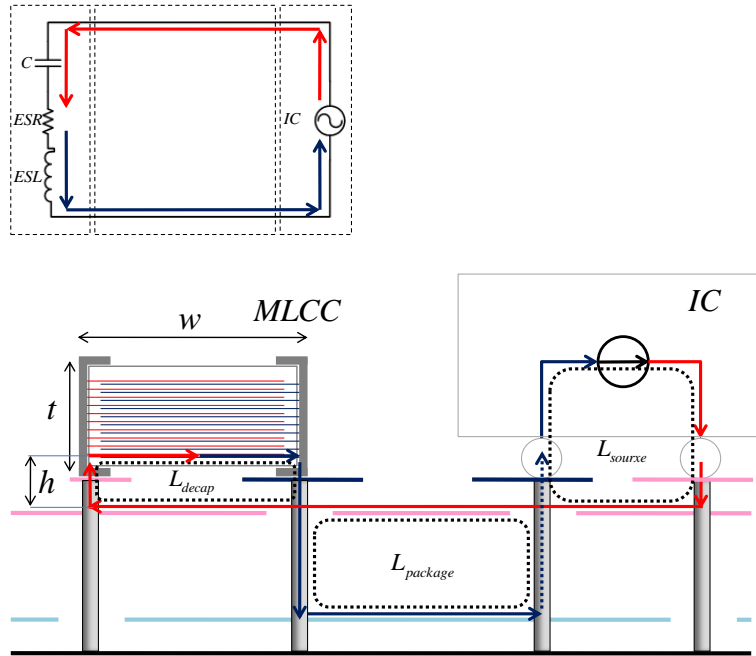
Fig. 1.1. Simple RLC equivalent circuit of a capacitor and connection inductance loop of an MLCC mounted to PCB planes.

When considering the parasitics of bypass capacitors, a widely used simple model is a series R-L-C network, where C is the capacitance of the part, R is the Equivalent Series Resistance (ESR) and L is the connection inductance as illustrated in Fig.1.1. The capacitance may be frequency dependent, primarily due to a redistribution of the current at very high frequencies. The inductance is determined by the connection of the capacitor to the rest of the circuit as well as the geometry of the capacitor itself.

In a multi-layer ceramic capacitor (MLCC), the inductance can be slightly higher at low frequencies where the resistance in the copper plates forces the current to flow uniformly through all plates. At high frequencies, most of the current flows along the lowest inductance path and is concentrated on the lower plates. The parasitic inductance

of MLCCs is becoming more and more important in the decoupling of high-speed digital systems. The relationship between the inductance and the ripple voltage induced on the DC voltage line is, *V=L×di/dt*. The parasitic inductance results from the interaction of magnetic flux created by the electric current flow in and out of the device on a circuit board. The current path or loop includes not only the multilayer capacitor's internal electrodes and external termination, but also the power planes, vias, mounting pads and solder fillets of the substrate/packages. At very high frequencies and low connection inductances, the current path is not defined by the entire capacitor multilayered stack, but most of the current is confined to the lower internal electrodes as the path of least impedance for the current flow [1].
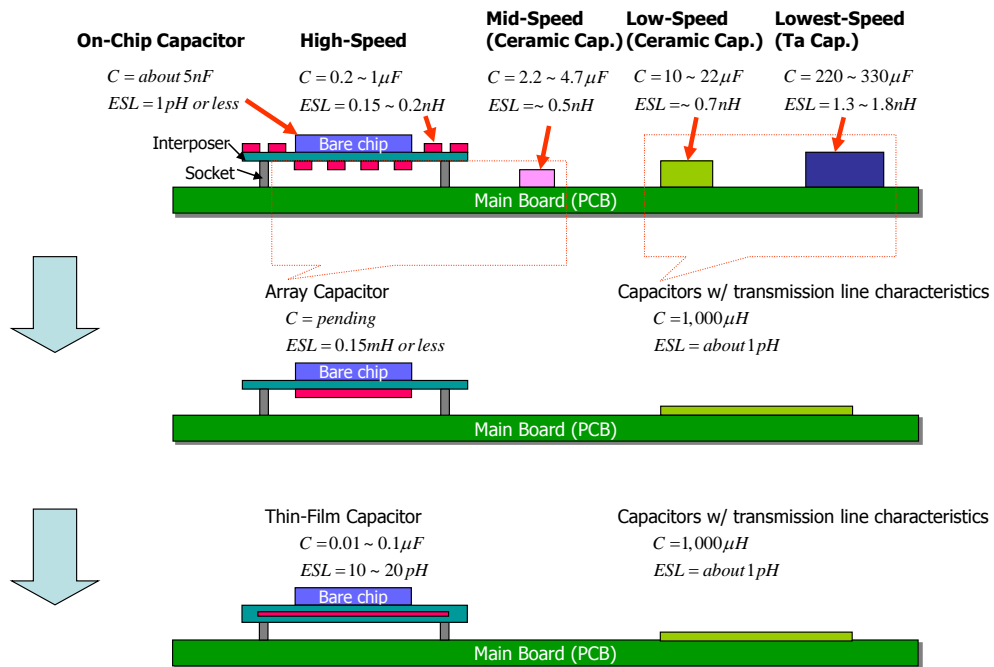
Fig. 1.2. Moving decoupling capacitors next to bare chip [3].

Over the past 10-12 years, decoupling capacitors have evolved into various types. This progress has been driven by the requirement to lower the inductance of power distribution systems to keep up with faster switching speeds and increased transistor density in silicon processors. The board pads and vias form closely spaced cancellation paths that support low inductance design strategies. When component companies characterize their devices, considerable care is taken to extract the influence of the test coupon to give a "part-only" ESL (Equivalent or Effective Series Inductance). However, inductance is a property of current loops and a low-inductance capacitor does not have a well-defined ESL independent of its connection to the board. The inductance of a mounted capacitor does not equal the sum of the connection inductance and the inductance internal to the capacitor unless there is no mutual inductance between the two portions of the loop. For low-inductance capacitors, this mutual inductance is always significant, making published values for the ESL practically meaningless.

As illustrated in Fig. 1.2, high-frequency noise reduction in a power distribution bus requires moving the decoupling capacitance close to the bare chip. As packaging structures continue to evolve, opportunities to develop new, optimal, low-inductance decoupling capacitors will continue to present themselves.

II. PLATE ORIENTATION EFFECT ON THE INDUCTANCE OF CONVENTIONAL MLCCs

In high-speed circuits, the value of the inductance associated with a connection to an MLCC (Multiple-Layer Ceramic Capacitor) is often more important than the nominal value of the capacitor. ESL is a value often quoted in capacitor data sheets for comparing

different capacitor designs. However, the actual connection inductance for small SMT (Surface Mount Technology) capacitors depends on several parameters that are not part of a typical ESL measurement. The actual high-speed performance of an SMT capacitor is generally unrelated to its nominal ESL. Capacitors that have the lowest published ESL may not be the best capacitors to use in a particular application. In this section, the effect of electrode (plate) orientation on the connection inductance of MLCC capacitors is investigated. It is shown that a single vertical plate has a higher inductance than a single horizontal plate when mounted over a board with a ground plane. However, as more vertically oriented plates are stacked side by side, the value of the self-inductance decreases significantly, whereas the inductance of horizontal plates that are vertically stacked is relatively independent of the number of plates in the stack. For large stacks, the overall width of the stack is the most significant parameter affecting the connection inductance. When the width and height of the stacked plates is the same, the effective inductance with either orientation is the same. Thus, capacitors with vertically oriented multiple plates do not inherently provide an advantage over capacitors with horizontally oriented multiple plates. The primary capacitor geometry parameters that affect the connection inductance are the plate stack width (which should be maximized) and the loop area associated with current flowing into and out-of the capacitor plates (which should be minimized).

2D modeling of horizontal and vertical plates

Two-dimensional models were used to isolate the contributions of the plates from the contributions of the end caps to the overall connection inductance of typical MLCC geometries. These models are illustrated in Fig. 1.3.
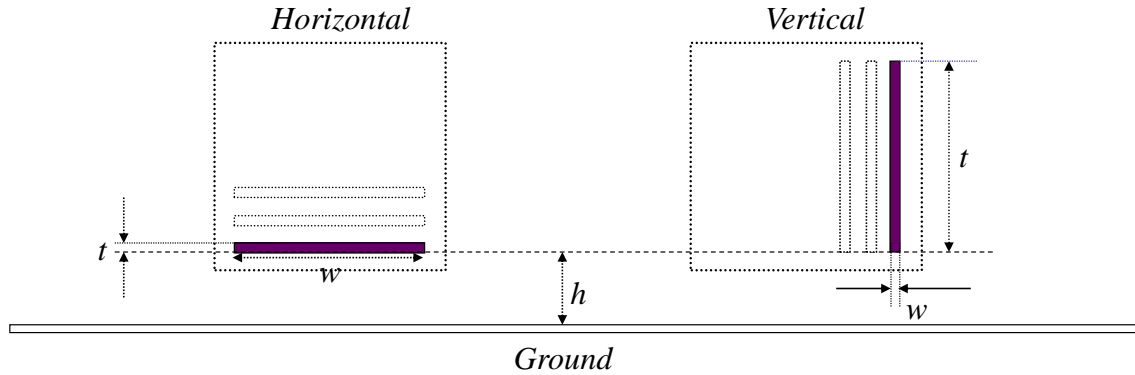
Fig. 1.3. Cross-sectional view of two-dimensional plate geometry.

The simulation of the self-inductance of a single plate over a ground plane was performed using a 0.4342 mm by 0.4342 mm plate located 0.0829 mm over a ground plane. The calculated inductance per unit length values were multiplied by a length of 0.94 mm (corresponding to a 0402 capacitor package) to give a value for the partial-inductance associated with the plates.

As the results in Table 1.1 indicate, the partial inductance of a vertically oriented single plate is significantly higher than that of a horizontally oriented plate. As the current spreads across the surface of the vertically oriented plate, the loop area formed between the plate current and the ground current increases. The horizontal plate provides the lowest inductance current path for a given height and plate surface area.

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Table 1.1. Partial inductance of a single plate (length = 0.94 mm)

	Self-inductance (Plate)	Mutual-inductance (GND-to-Plate)	Loop inductance (SI – MI)
Horizontal plate	0.899 nH	0.772 nH	0.128 nH
Vertical plate	0.972 nH	0.750 nH	0.222 nH

The two top plots in Fig. 1.4 illustrate the magnetic field intensity and the bottom plots show the lines of magnetic flux for each configuration evaluated.

Modeling stacked plate pairs as blocks

Quasi-static models of the MLCC inductance require shorting the positive and negative electrodes together where the plates overlap. This allows the current to spread out over the plates in the same way that it would at high frequencies, while eliminating the capacitive reactance from the models. Plate pairs are represented as solid conducting "blocks" as illustrated in Fig. 1.5. The three key dimensions of the structure, w, t and l denote the width, thickness and length of the stacked plates respectively.
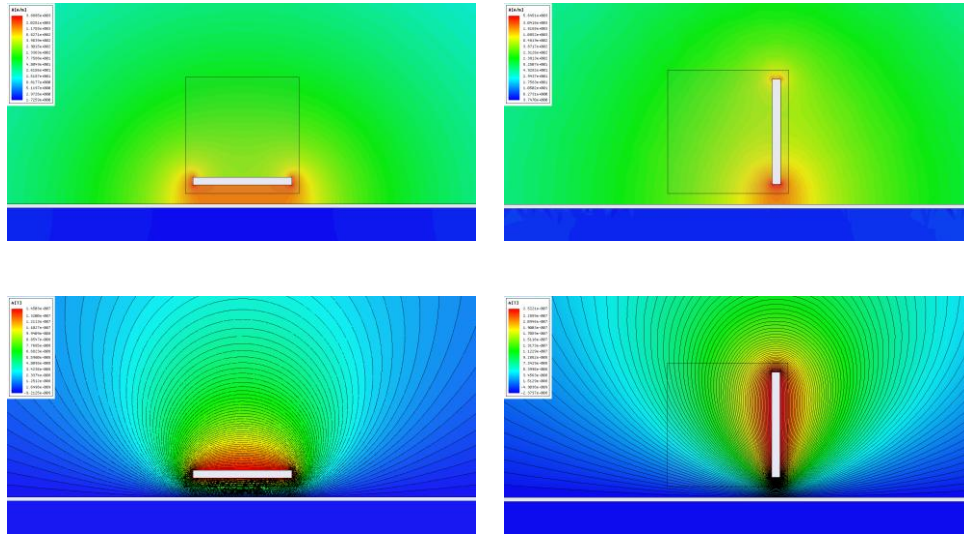
Fig. 1.4. Magnetic field intensity (top) and magnetic flux lines (bottom) for each plate orientation.
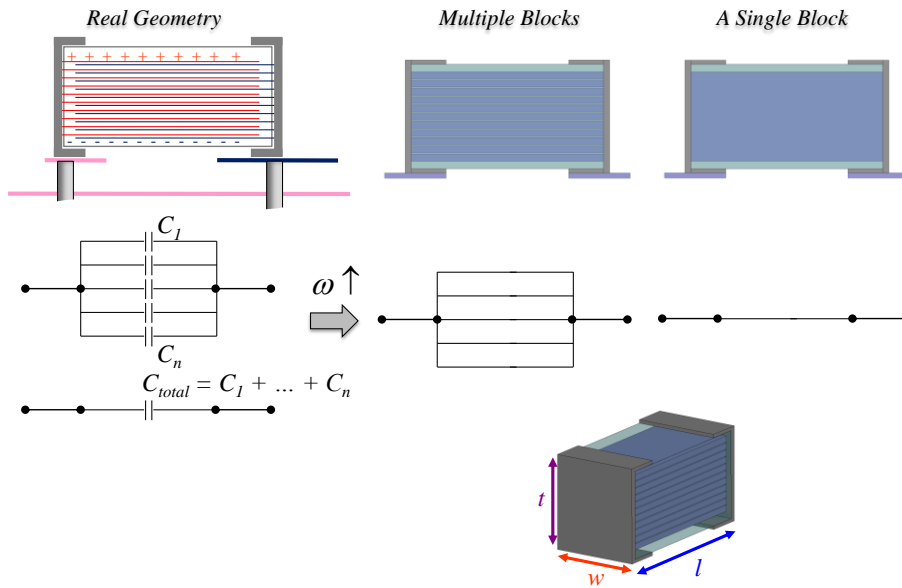
Fig. 1.5. Simplified inductance models for MLCCs.

Although the inductance of a single plate is higher when the plate is oriented vertically, this inductance decreases as we add more plates in parallel. Single horizontal plates have lower inductance, but stacking more plates on top of the first one has little effect on the high-frequency inductance. To illustrate this, we use the model in Fig. 1.6. The parameters of a 2D single block were varied to determine the effect of the plate stack size and orientation on the capacitor inductance. A block represents a set of internal electrodes forming the capacitor structure for high-frequency current flow. The ground conductor under the block is an ideal ground plane. The stack size (t for the horizontal blocks and w for the vertical blocks) was increased from 1 to 21 plate-pair thicknesses. A single plate-pair thickness was 0.0342 mm. The height of the block above the plane was 0.0829 mm.
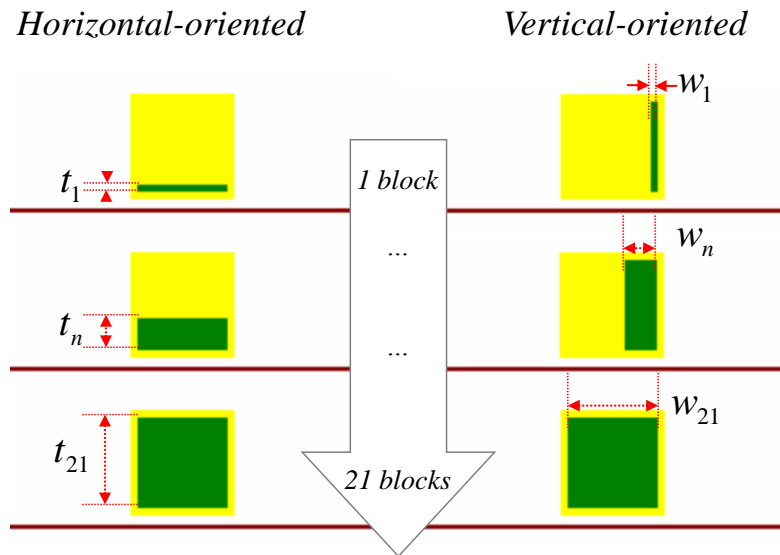
Fig. 1.6. Parameter variations of single block MLCC model.

As shown in Fig. 1.7, the self-inductance of the vertically oriented block is much higher than that of the horizontally oriented block. As the number of blocks increases, the inductance of the vertically oriented blocks decreases significantly. However, the inductance of the horizontal blocks shows little change as the number of blocks increases.

3D modeling for analyzing effective inductance

Fig. 1.8 illustrates a 3D model for an MLCC. It is not possible to quantify a meaningful inductance for this structure without specifying a test fixture that completes the current loop. Therefore, a 3D structure for extracting effective inductance was defined. The structure consisted of a two-layer printed circuit board with an input port and a capacitor mounting port as illustrated in Fig. 1.8.
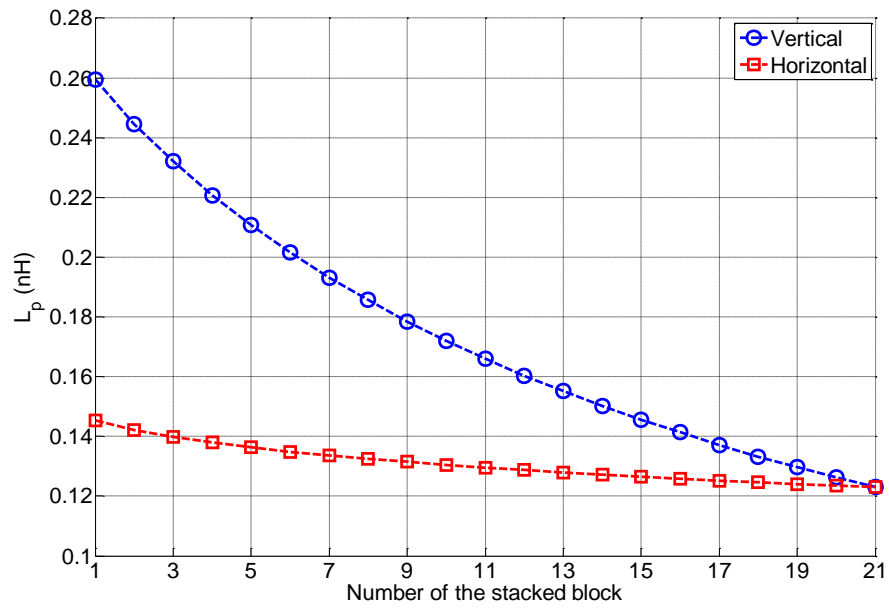
Fig. 1.7. Partial self-inductance values by the stack size.
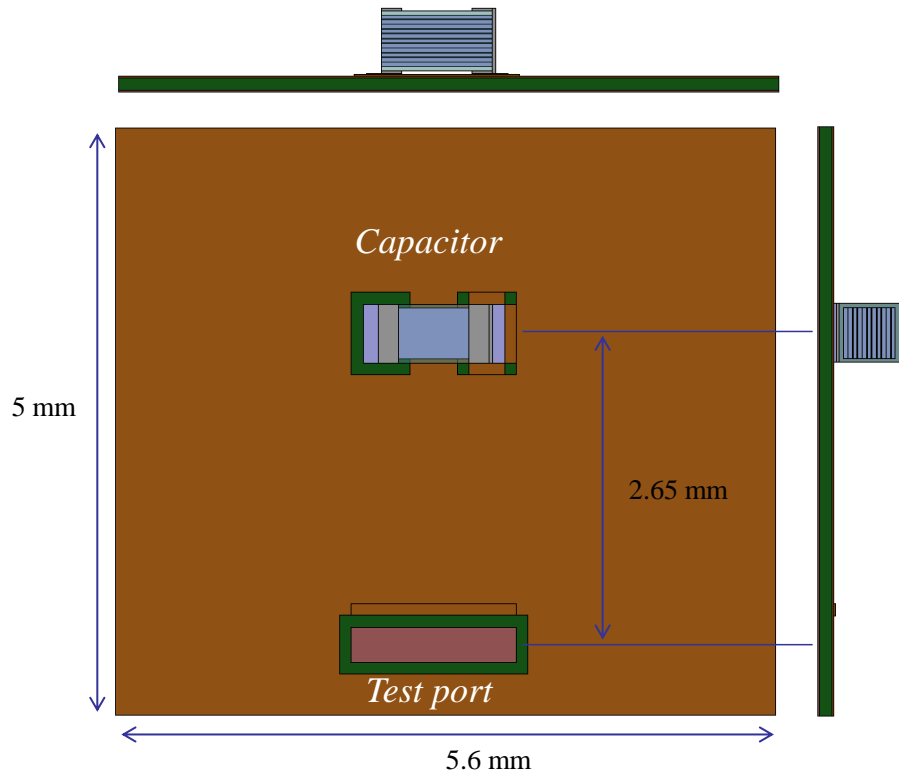
Fig. 1.8. Top and side views of 3D model for an MLCC mounting fixture.

Commercial simulation software (Ansoft Q3D Extractor[TM]) was used to determine the effect of the stack size on the effective inductance. The AC frequency was set to 1 GHz. The number of blocks was varied from 1 to 11 with a slight dielectric gap between adjacent blocks in both orientations as illustrated in Fig. 1.9. The stack order was from bottom to top for the horizontal orientation and from right to left for the vertical orientation.
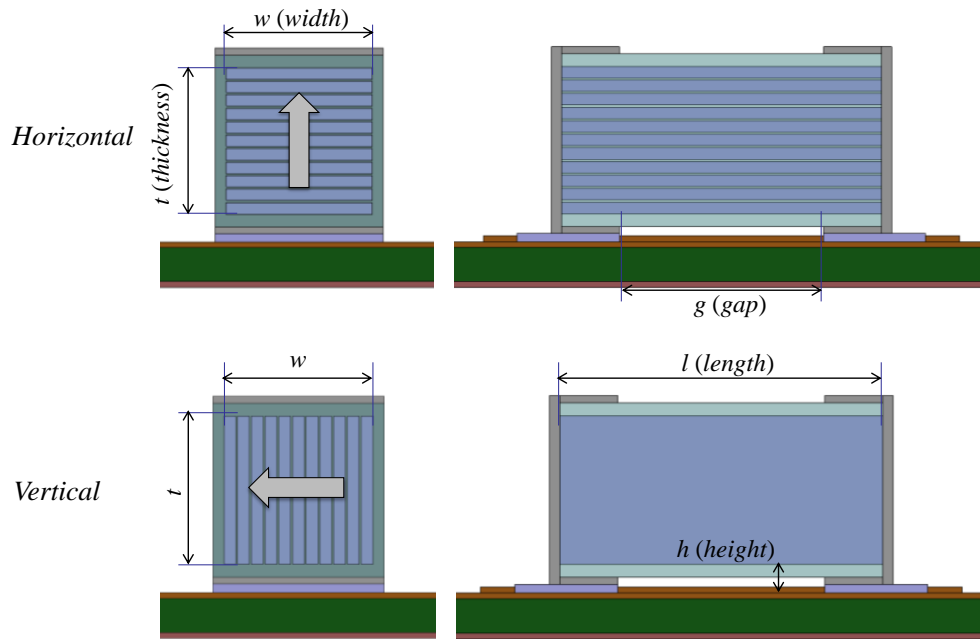
Fig. 1.9. Three-dimensional view of multiple block MLCC model.

The effective inductance of a vertically oriented block was found to be higher than that of a horizontally oriented block just as it was in the 2D simulation results. As the number of blocks increased so that the outer dimensions of the stacks were the same, the effective inductances approached the same value for both block orientations as shown in Fig. 1.10.

<u>Effect of the dimensions of a single block on the effective inductance</u>

This process was repeated without the dielectric gaps between blocks as illustrated in Fig. 1.11. The effective inductance of a single block was analyzed as a function of the parameters t or w. The stack size was incremented in 0.02-mm steps, with the final dimension denoted as t_e or w_e.
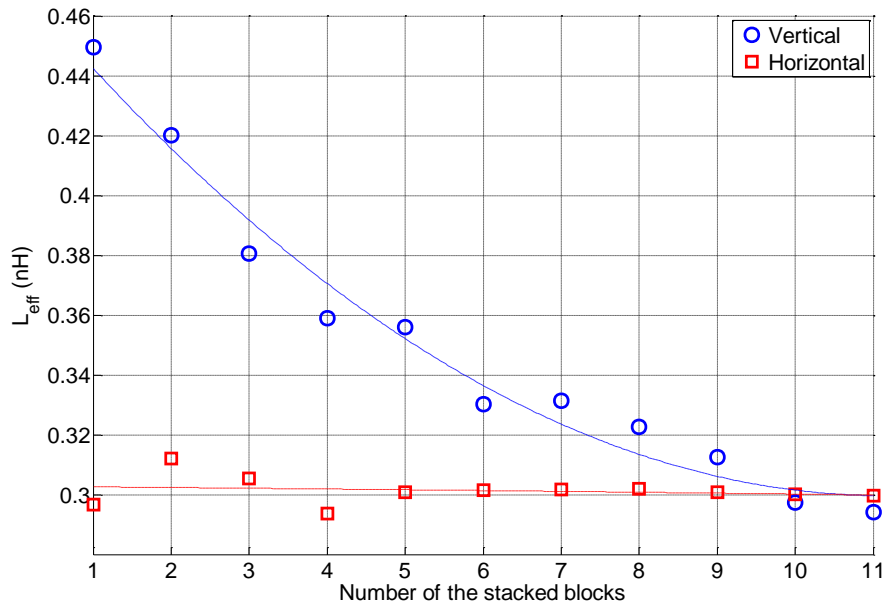
Fig. 1.10. Effective inductance values by the number of blocks.
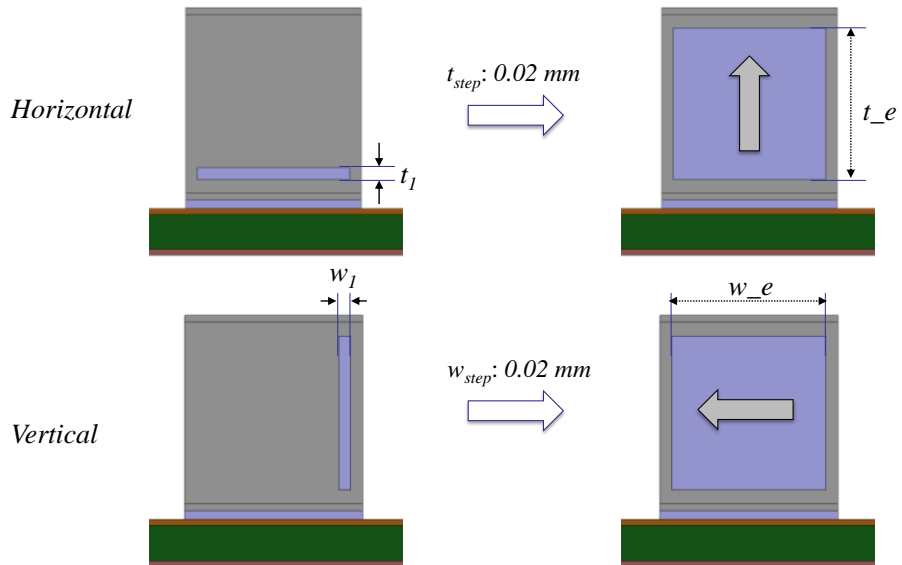
Fig. 1.11. Parameter variations of three-dimensional single block MLCC model.

As shown in Fig. 1.12, the results mimic the results obtained with the dielectric between each block. For the horizontal orientation, as the height, *t*, increased, the effective inductance varied little. For the vertical orientation, the effective inductance decreased as the width of the stack increased.
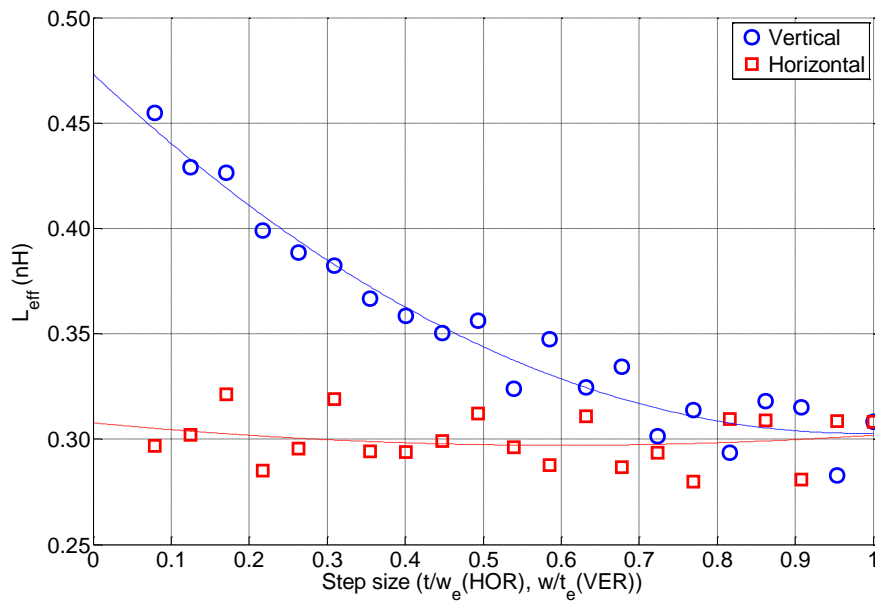
Fig. 1.12. Effective inductance values by the step size of plate geometry.

The results in presented indicate that a vertically oriented single plate has a higher inductance than a horizontally oriented single plate. The simulation of multiple plates indicates that as more vertically oriented plates are stacked to increase the overall width of the capacitor, the value of the capacitor's inductance decreases. Stacking horizontal plates vertically has relatively little effect on the inductance, since most of the high-frequency current flows only on the lower plates. The inductance of the plate stack is

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primarily a function of the width and height of the stack and relatively independent of the plate orientation. Therefore, MLCC designs with vertically oriented plates do not necessarily provide an advantage over designs with horizontally oriented plates in terms of providing the lowest possible connection inductance.

III. INDUCTANCE CALCULATIONS FOR ADVANCED PACKAGING IN HIGH-PERFORMANCE COMPUTING APPLICATIONS

Effective decoupling is crucial for the optimum performance of the power distribution network in an electronic system. As component-packaging technologies evolve enabling tighter integration and faster performance of electronic systems, it is essential to develop better decoupling strategies. This section describes several new or proposed packaging structures and evaluates the connection inductance associated with possible decoupling locations. As expected, connections made on the chip tend to have a lower inductance than connections made on the package; and connections made on the package tend to have a lower inductance than connections made on the board. This illustrates the importance of providing decoupling capacitance as close to the chip as possible in order to maximize the effective bandwidth of the power distribution network.

Power bus decoupling issues in electronic systems are shifting from the printed circuit board to the component packaging. This trend is being driven by the miniaturization of electronic systems and the shift of the package manufacturing process to the IC foundry level. Traditional wire bonding technology is steadily being replaced by

area array (bump) interconnections and three-dimensional silicon integration technologies.

The evolution of advanced packaging techniques is being driven by two electronic device platforms; mobile communication applications with an emphasis on miniaturization, and computing applications with an emphasis on high performance. High-density integration is required for both platforms. Ultimately, the roadmap of both platforms calls for the implementation of SOC (System-on-Chip) or SOP (System-on-Package) structures including; 3D chip stacks, silicon carrier packaging, silicon interconnection or bonding, copper-to-copper stud bonding and integrated decoupling capacitors [5].

Advanced packaging includes wafer-level and 3D stacked ICs, as well as traditional packaging technologies [6]. Vertical interconnection technology for different packaging levels is evolving from traditional wire bonding and flip-chip bumping to wafer-level packaging and copper-to-copper bonding. Key design parameters for power bus decoupling of advanced packaging structures can be categorized depending on the location or type of decoupling capacitor. Decoupling capacitors can be discrete, singulated or distributed. They can be individual local capacitors or global arrays.

<u>Decoupling schemes for high-performance packaging</u>

Table 1.2 shows key design parameters affecting the decoupling capacitor connection inductance at different interconnection levels. Typically, the vertical scaling dimensions become smaller as the interconnections go from the PCB level to the IC level.

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Table 1.2. Key design parameters by interconnection levels

Interconnection level		Key design parameters	Vertical scaling
PCB	trace	w (width), t (thickness), l (length)	~ mm
	via	d (diameter), h (height), s (distance)	
BGA	bump	d (diameter), p (pitch; I/O pitch)	~ 500μm
Package substrate	trace	w (width), t (thickness), l (length)	~ mm
	core via	d (diameter), h (height; S_PG), s (distance; d_mutual)	
Flip chip	μ-bump	d (diameter), p (pitch; I/O pitch)	~ 100 μm
Silicon substrate	through-silicon via	d (diameter), h (height), s (distance)	50 ~ 300 μm
IC	chip	W (width), L (length)	~ 10 μm
	through-silicon via	d (diameter), h (height; h_tvs), s (distance; d_tvs)	~ 10 μm
	Cu-to-Cu bond	d (diameter), p (pitch; I/O pitch)	~ μm
Decoupling capacitor	MLCC	w (width), h (SMT height; h_decap), l (length; l_decap)	Variable
		p (terminal pitch)	
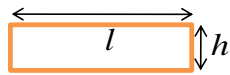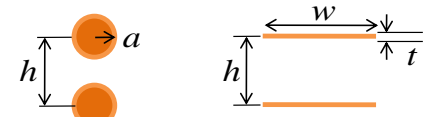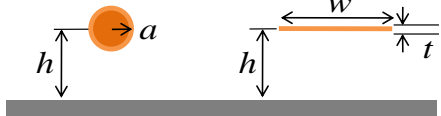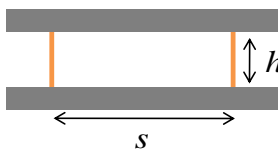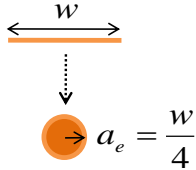
Cases	Short current loop (l < 5h)	Long current loop (l > 5h)
Rectangular loop *Decap. where power is routed on traces*	$$L_{rectloop} \approx \frac{\mu_0}{\pi}\left[\begin{array}{l}-2(l+h)+2\sqrt{h^2+l^2}-h\ln\left(\frac{h+\sqrt{h^2+l^2}}{l}\right)\\-l\ln\left(\frac{l+\sqrt{h^2+l^2}}{h}\right)+h\ln\left(\frac{2h}{a}\right)+l\ln\left(\frac{2l}{a}\right)\end{array}\right]$$	$L_{wire-pair}=\frac{\mu_0\mu_r}{2\pi}\cosh^{-1}\frac{h}{2a}\ (H/m),\ h>>a$ $L_{wire-pair}=\frac{\mu_0\mu_r}{w}h,\ w>>h,\ h>>t$
Rectangular loop above a plane *Decap. connected to power plane*	$$L_{rectloop} \approx \frac{\mu_0}{\pi}\left[\begin{array}{l}-2(l+h)+2\sqrt{h^2+l^2}-h\ln\left(\frac{h+\sqrt{h^2+l^2}}{l}\right)\\-l\ln\left(\frac{l+\sqrt{h^2+l^2}}{h}\right)+h\ln\left(\frac{2h}{a}\right)+l\ln\left(\frac{2l}{a}\right)\end{array}\right]$$	$L_{wire-ground}=\frac{\mu_0\mu_r}{2\pi}\cosh^{-1}\frac{h}{a}\ (H/m),\ h>>a$ $L_{wire-pair}=\frac{\mu_0\mu_r}{w}h,\ w>>h,\ h>>t$
Two vias between planes	$L_{vias\ between\ planes}=\frac{\mu_0 h}{2\pi}\ln\left(\frac{s}{r}\right)$	**Estimation of wire radius 'a_e'** $a_e=\frac{w}{4}$
Resistance *Metal of on-chip capacitor*	$R_{DC}=\frac{l}{\sigma A}=\frac{l}{\sigma wt},\quad R_{AC}\cong\frac{l}{\sigma A}=\frac{l}{\sigma 2\pi a\delta},\quad \delta=\frac{1}{\sqrt{\pi f\mu\sigma}}$	

Fig. 1.13. Formulas for loop inductance of common circuit geometries [24].

The following sections describe key design parameters for several packaging structures with the decoupling capacitor located on-chip, off-chip, and on the top or bottom of the carrier. Formulas for calculating the inductance and resistance of circuit board configurations are provided in Fig. 1.13.

Fig. 1.14 illustrates five possible locations for the decoupling capacitors in a high-performance package; stacked on chip, stacked on Si-carrier, top side of package substrate, bottom side of package substrate, and embedded in the package substrate. The

current paths, including the dominant factors affecting the loop inductance, are indicated for each location.
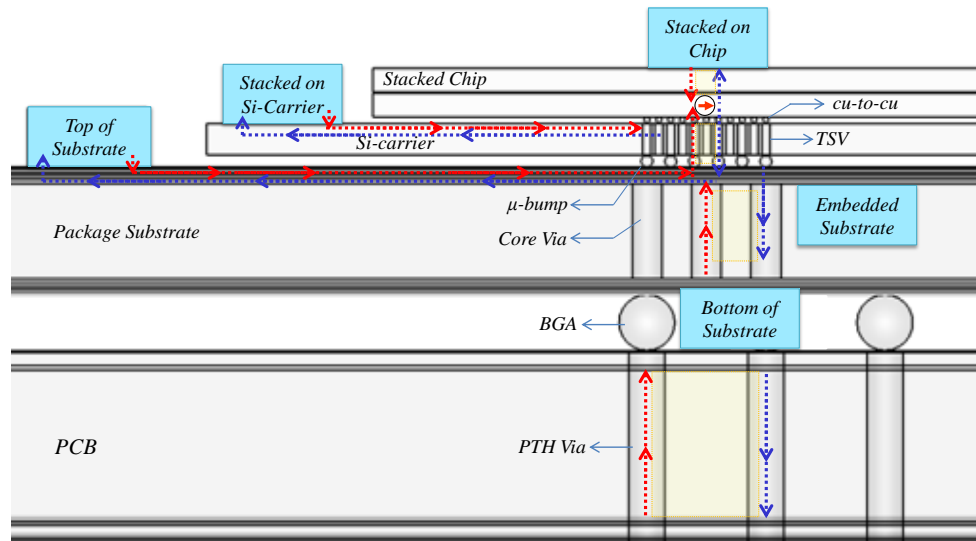
Fig. 1.14. Possible locations of decoupling capacitors for high-performance packaging.

As illustrated in Fig. 1.14, the 'stacked-on-chip' location is closest to the source and permits the lowest possible connection inductance. A typical inductance calculation for a 'stacked-on-chip' decoupling capacitor is determined by modeling the current path as a pair of vias between two solid planes. This model is reasonable because the on-chip grids that connect to the vias are relatively wide and contribute little to the overall path inductance. For example, suppose that the radius of the through-silicon vias is 5 µm, the distance between adjacent vias is 50 µm, and the height of a die is about 200 µm. Via inductances associated with these vias can be calculated using the formula in Fig. 1.13. In

this case, the connection inductance would be 92 pH. The via resistance would be

$R = 2h/\sigma\pi r^2 = 89$ mΩ. In this case, the inductance would be more important than the

resistance at frequencies above 150 MHz.

Resistance on-chip

A decoupling capacitor placed within a die is referred to as an on-chip decoupling capacitor. The loop area to be considered when calculating the inductance includes the on-chip decoupling capacitor, power/ground metal and the circuit being decoupled. The loop area should be minimized to reduce the resistance as well as the inductance of the connection. In many cases, the resistance of the connection overwhelms the inductance ($R > j\omega L$).
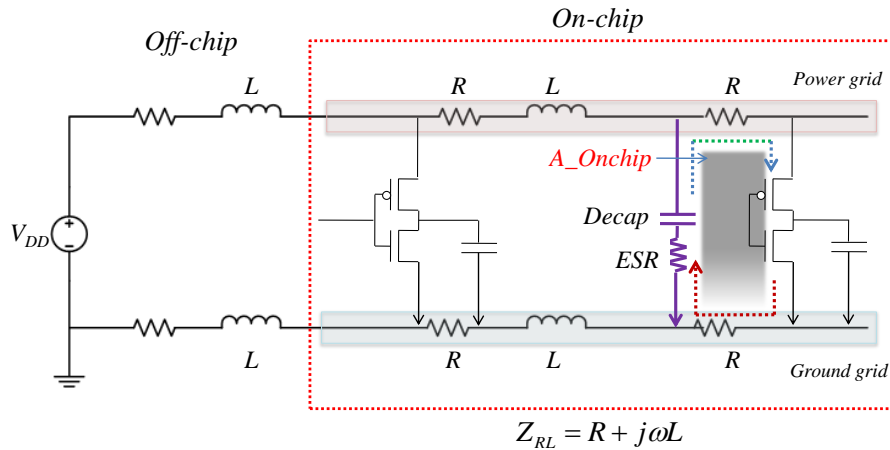
Fig. 1.15. On-chip decoupling capacitor in power/ground metal grid.

For example, a rectangular loop of wire in a 0.13-μm process might have a total length of 20 μm, a width of 5 μm and a height of 20 μm. Assuming that the wire thickness was 1 μm and the conductivity of the copper was 5.7 x 10^7 S/m, the resistance of the wire loop would be 275 mΩ. The inductance of the same loop would be approximately 32 pH. Therefore, the resistance would be more important than the inductance at all frequencies below 1.37 GHz.
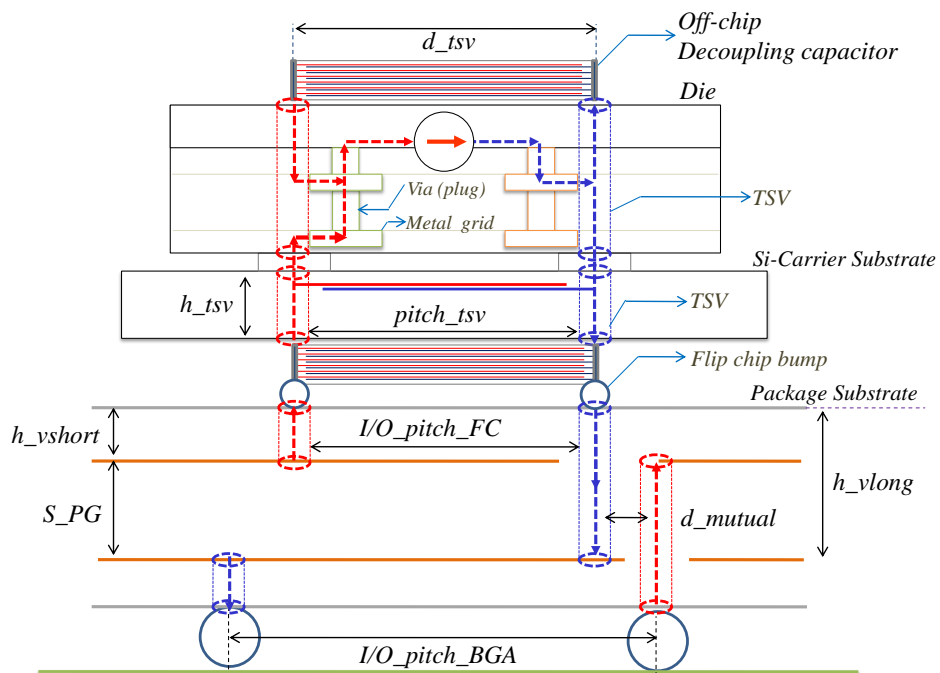
Fig. 1.16. Current flow in the off-chip capacitors mounted on a chip or Si-carrier package.

Loop inductance off-chip

As illustrated in Fig. 1.16, the decoupling capacitor can also be stacked on the die, placed on the top or bottom side of a silicon carrier substrate, or even embedded in the silicon substrate using TSV (through-silicon via) technology to connect the switching gates to the decoupling capacitor. For these 'off-chip' locations, the interconnections should be close to the circuit being decoupled in order to minimize the loop area.

Inductance instead of resistance is more likely to be the key parameter in an off-chip configuration. For example, if through-silicon vias have a length of 300 μm, a diameter of 70 μm and a spacing of 100 μm, the loop inductance of the vias would be 63 pH; whereas these same vias would only have about 0.9 mΩ of resistance. Therefore, at frequencies above 2.3 MHz, the inductance would dominate.

Loop inductance in top/bottom-side of package substrate

Design strategies for mounting decoupling capacitors on either side of the package substrate can be divided into two cases depending on the distance between the power planes of a multi-layer package substrate [7].
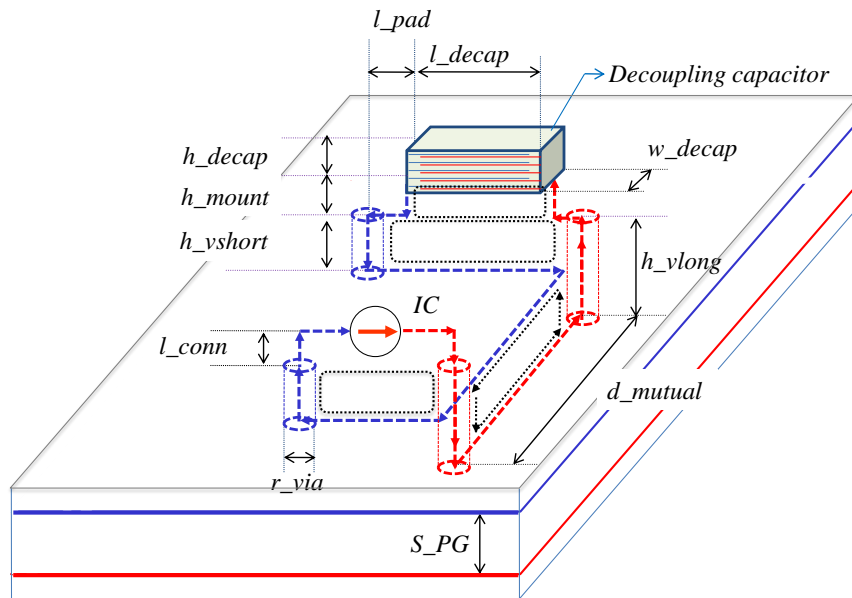
Fig. 1.17. Current loops in the top side of package substrate.

On circuit boards with closely spaced power planes, ~ 0.3 mm or less, the location of the local decoupling capacitors is not critical. To minimize the connection inductance, all local decoupling capacitors should be mounted on the face of the board nearest to the planes. Capacitors should be connected directly to the planes without using traces. Vias should be in or adjacent to the capacitor mounting pads as close to each other as possible. When a chip and decoupling capacitor are both mounted on the top side of the package substrate, the inductance of the loop can be expressed as the sum of the inductances of the two half-loops above the top plane and the inductance of the loop between the planes. (Note that it is the absence of any mutual inductance that allows us to simply add the two partial inductances of these half-loops.)

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When the spacing between the planes is less than ~ 0.3 mm, the inductance of the loop between the planes tends to be small relative to the connection inductance above the planes. When the spacing between the planes is greater than ~ 0.5 mm, the inductance between the planes is no longer negligible. In fact, by placing the vias that carry current to and from the lower plane near each other, it is possible to take advantage of the mutual inductance between these vias to force the current to be drawn from the decoupling capacitor rather than the planes. This reduces the noise on the power planes [7]. Therefore, when the planes are > 0.33 mm apart, it is important to locate the decoupling capacitors near the source.

When the capacitor is mounted on the same side of the board as the device it is decoupling, it can share the via connecting to the lower plane with the active device. When the capacitor is on the opposite side of the board, the calculation of the inductance is done using the same formulas used when the capacitor is on the same side as the active device. However, the currents flowing on the vias in between the planes are now being drawn from different planes. The rules for locating the decoupling capacitors are the same, except it is no longer possible to share the via that carries current between the planes. Therefore, the active device and the capacitor should each have their own vias connecting to the planes (i.e. they should not share vias).
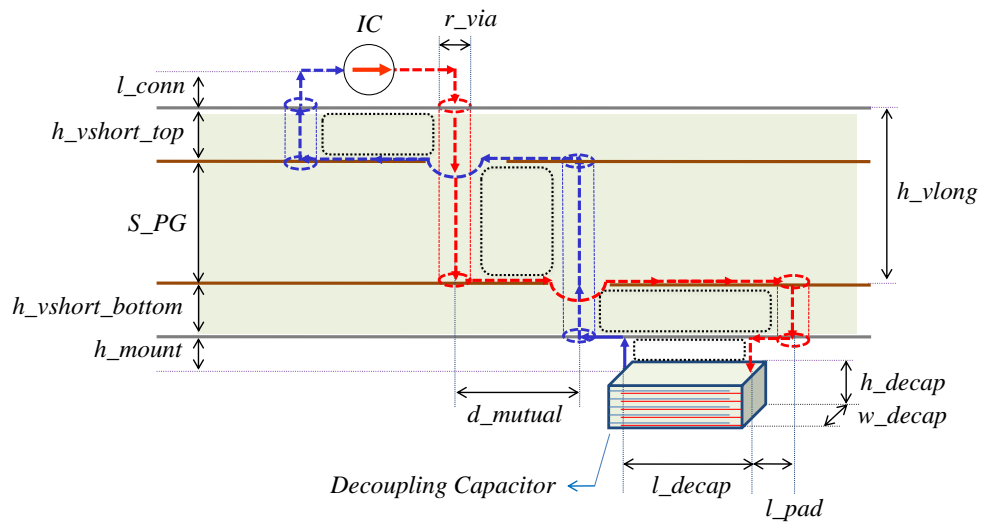
Fig. 1.18. Current loops in the bottom side of package substrate.

Inductance calculations for MLCCs on a packaging substrate

Loop inductance of two vias at different packaging levels

Table 1.3 shows the inductance of two vias between planes at different interconnection levels and typical values of capacitance available at each of these levels. Fig. 1.19 illustrates this trend schematically.

Table 1.3. Typical capacitance and loop inductance of two vias by different packaging levels

Packaging level	Via types	Vertical scaling, h (µm)	s (µm)	r (µm)	L (nH)	C (µF)		Operating Frequencies (Z_{target} = 1 Ω)
PCB	PTH	1200	1000	150	0.46	C_local	2.2	72 kHz - 346 MHz
Package Substrate	Core via	800	750	125	0.29	$C_{package}$	0.1	1.6 MHz - 549 MHz
Si-Carrier	TSV	300	100	35	0.06	C_{sisub}	0.01	160 kHz - 2.65 GHz
IC	TSV	200	100	5	0.12	C_{onchip}	0.01	160 kHz – 1.33 GHz
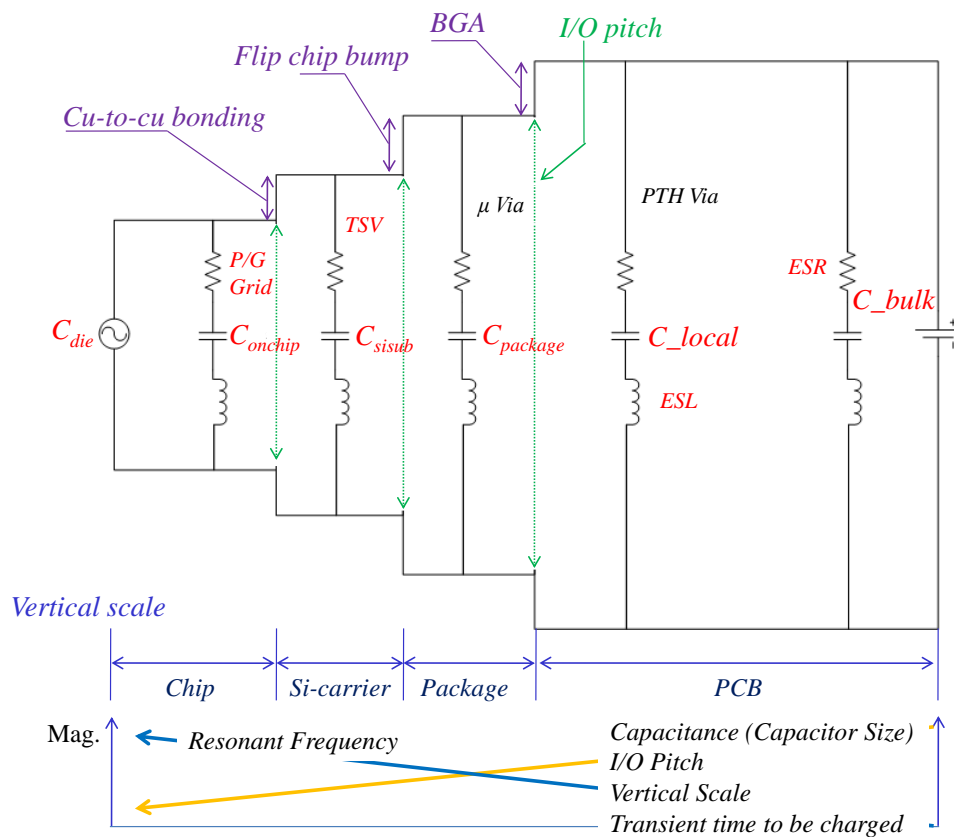
Fig. 1.19. Equivalent circuit diagrams by different packaging levels.

Note that the connection inductances tend to get lower as we locate the decoupling capacitors nearer the source. This suggests that capacitors within the packaging structure nearer the source will be effective at higher frequencies as illustrated in Fig. 1.19.

The capacitance available limits the low-frequency effectiveness of the decoupling. The connection inductance limits the high frequency effectiveness. For a given target impedance, we can calculate the range of frequencies at which a given capacitor is expected to be effective,

$$\frac{1}{2\pi \left| Z_{t\arg et} \right| C} < f < \frac{Z_{t\arg et}}{2\pi L} \tag{1}$$

The operating frequencies for a target impedance of 1 ohm are in the last column of Table 1.3. These are typical values, however in many applications, the target impedance will be different from 1 ohm and the effective frequency range of the various package levels will vary accordingly.
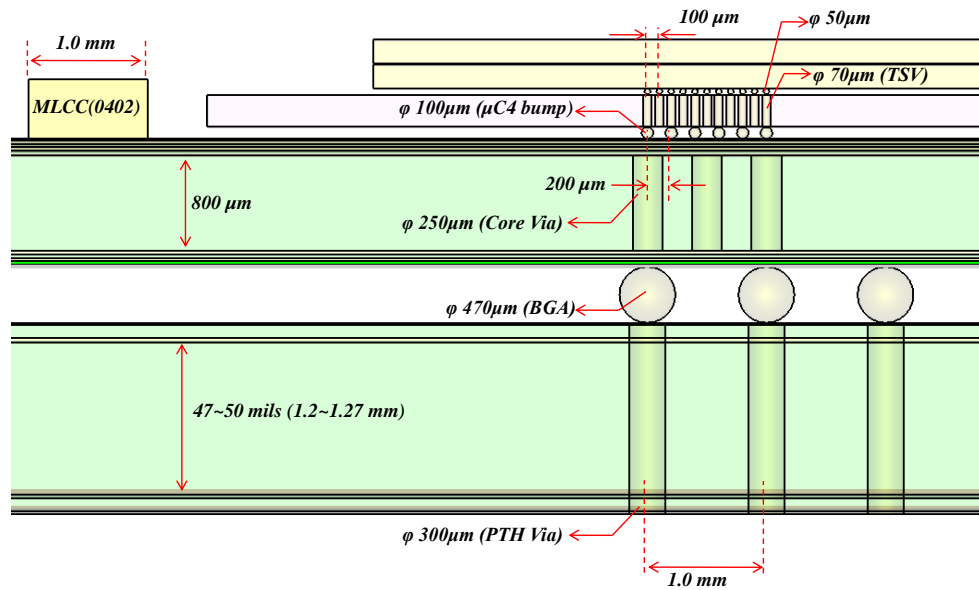
Fig. 1.20. An example of advanced packaging for high-performance computing application.

Fig. 1.20 illustrates an example of a package structure in a high-performance computing application. The stacking order from the bottom up is the printed circuit board, then the package substrate (organic interposer), and finally the silicon-carrier package and possibly stacked dies. The possible interconnection technologies are solder bump, flip chip bumping, through-silicon vias and copper-to-copper bonding. Multi-layer decoupling capacitors may be mounted on or in the circuit board, on or in the interposer, or between the stacked dies. Fig. 1.20 illustrates how the vertical scaling reduces as one moves from the bottom to the top of the geometry.
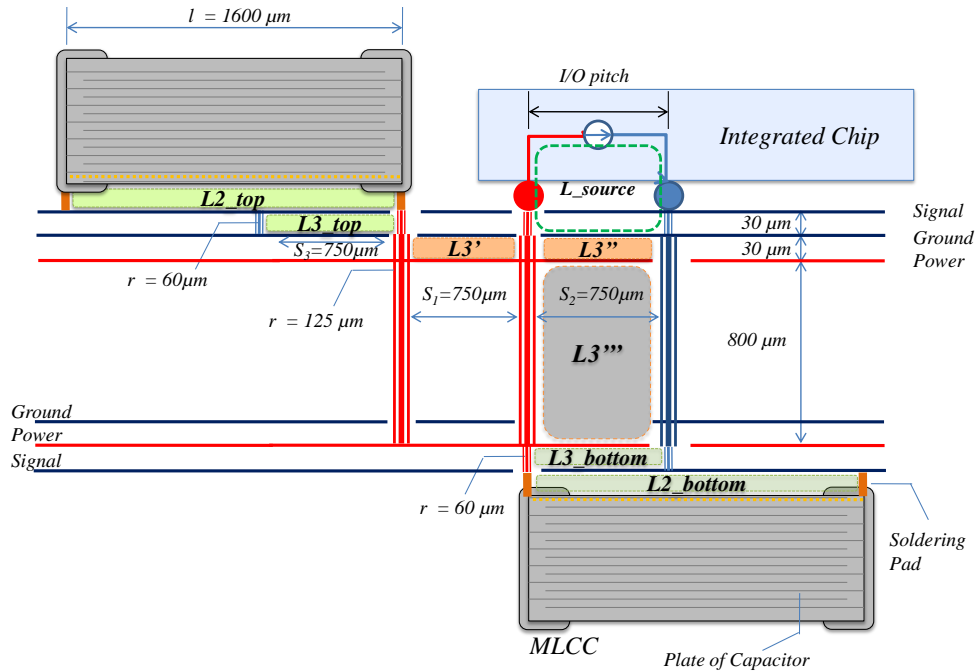
Fig. 1.21. Inductance loops for possible locations of the decoupling capacitors on a six-layered package.

Fig. 1.21 illustrates how two 1608 decoupling capacitors would typically be located on the top or the bottom of a packaging substrate. We can determine which position has the lower connection inductance by using simple analytical formulas for determining the connection inductance [24].

In the case of the top-side location, the total connection inductance is equal to the sum of the loop inductances denoted as $L2\_top$, $L3\_top$, $L3'$ and $L3\_source$. In the case of the bottom-side location, the total connection inductance is equal to the sum of $L2\_bottom$, $L3\_bottom$, $L3''$, $L3'''$ and L_source. If there is no metal plane on the signal layer adjacent to the decoupling capacitor, $L2\_top$ and $L3\_top$ must be considered one loop instead of two separate loops. Even though the $L2\_top$-$L3\_top$

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loop is not rectangular, a good estimate of the inductance can be obtained by approximating the loop as a rectangle with an equivalent area.

Table 1.4. Inductance calculation of the illustrated packaging structure (l > 5h, w >> h)

Location	Total inductance (nH)	$L2\_top$ (L2_bottom) (nH)	$L3\_top$ (L3_bottom) (nH)	$L3'$ (nH)	$L3''$ (nH)	$L3'''$ (nH)
On the Top side	0.12	0.1	0.01	0.01	-	-
Bottom side	0.42	0.1	0.01	0.01	0.01	0.29

In the top-mounted case, the total connection inductance ($L2\_top + L3'$) is about 0.12 nH compared to 0.42 nH ($L2\_bottom + L3'' + L3'''$) on the bottom. In this case, the decoupling capacitor located on the top side has a lower connection inductance than the capacitor on the bottom side. The difference is primarily due to the inductance associated with the loop area between the inner planes, $L3'''$.

Power bus decoupling inductance for high performance packaging in computing applications is decided primarily by the loop area formed by the current path from the switching device to the decoupling capacitor and to a lesser extent by the effective radius of the connecting conductors. The spacing between the power and ground layers in the packaging substrate, the height of through-silicon vias in the silicon carrier substrate and the solder ball diameter for flip-chip bumping are all key factors when calculating connection inductance. Another important factor is the horizontal distance between vias carrying current to and from the decoupling capacitor. Vias should be placed close to each other to reduce the inductance of the path.

IV. NEW CAPACITOR CONFIGURATIONS FOR ADVANCED PACKAGING

New packaging technologies for system-on-chip (SOC) and system-in-package (SIP) structures allow engineers to design faster, more tightly integrated electronic devices that require new approaches for providing adequate decoupling capacitance. Fortunately, SOC and SIP packaging technologies open the door to a wide range of new decoupling options. Each option has its own merits and presents its own set of challenges. Selecting the best decoupling option involves a cost/performance trade-off. As performance demands increase and the costs of new packaging techniques come down, we can expect to see a variety of new decoupling schemes rise in popularity. The following sections describe new decoupling capacitor schemes for advanced packaging technologies.

Capacitive-stem capacitor

The greatest contributor to the connection inductance of capacitors mounted on printed circuit boards (PCBs) or interposers is often the loop formed by the vias that carry current between the MLCC and the printed circuit board power planes. This inductance can be minimized by adding more interconnecting vias or locating the vias as close as possible to one another, but it is still generally on the order of a nanohenry. Fig. 1.22 shows a capacitor design that eliminates the traditional via-loop area. This capacitor has a stem with metal rings for making the positive and negative connections to the PCB planes. The stem drops into a single large-diameter via hole drilled in the PCB. Inside the stem, the current is carried to the main body of the capacitor through low-inductance

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plates that are interleaved to maximize their own mutual inductance and therefore minimize the connection inductance.
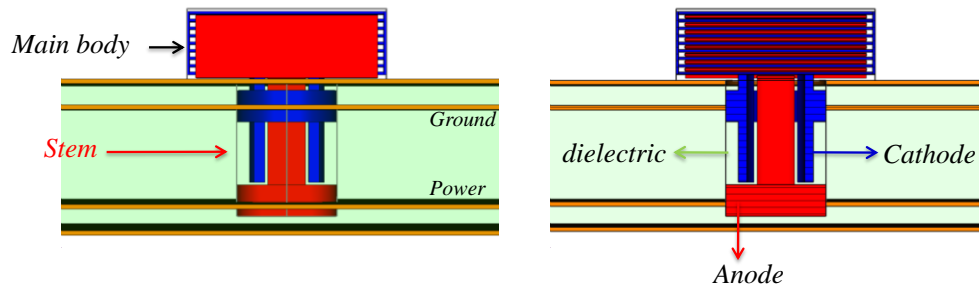
Fig. 1.22. Cross-sectional view of a ringed-stem capacitor mounted in PCB/package.

Fig. 1.23 shows the three-dimensional geometry of the ringed-stem capacitor. Possible variations of this capacitive stem design based on the ringed stem capacitor include:

1. A capacitor with circular horizontal rings but the rings are only metallic in $90°$ arcs on opposite sides.

2. A capacitor with a rectangular stem that has positive connection terminals on two opposing sides and negative connection terminals on the remaining two sides. This capacitor design also can be divided into two variations by plate orientation. This design and the one above facilitate easy soldering, since vertical shearing of solder cannot short the connection.

3. A capacitor with a coaxial stem that connects to both planes.

4. A capacitor with a cylindrical or rectangular stem that has no head. This capacitor could be embedded in the board and does not require space above the surface of the board.

Modeling of effective inductance

In order to compare the low-inductance performance of the proposed ringed-stem capacitor with that of conventional MLCC, a full-wave simulation was performed. As illustrated in Fig. 1.24, the test configuration consisted of a two-layer printed circuit board with an input port having a source and sink and an MLCC mounting port in the left side. The size of the MLCC is 1.0 mm $\times$ 0.5 mm $\times$ 0.5 mm. The test board for the ringed-stem capacitor has a single large-diameter via hole drilled in the PCB for a stem with metal rings. The diameter of the drilling via hole is a_2 as illustrated in Fig. 1.28. The capacitor structure of the main body was simplified to a single block as described in Fig. 1.5, Section II.
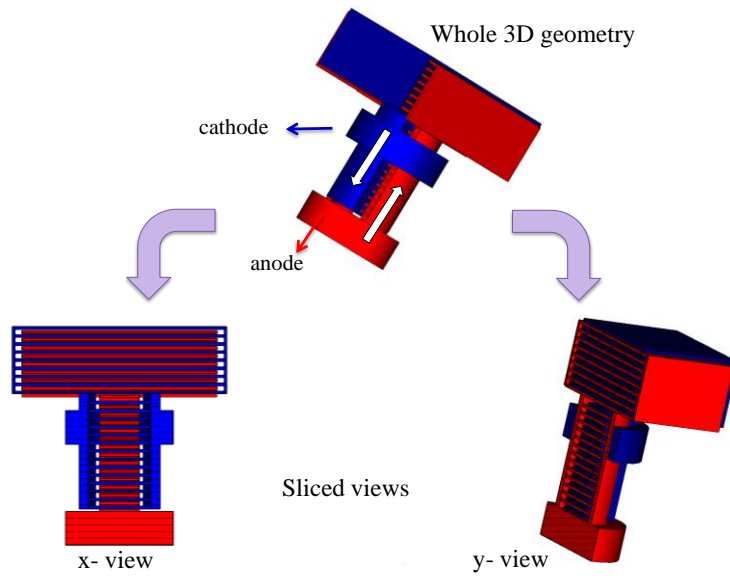
Fig. 1.23. 3D geometry of ringed-stem capacitor.
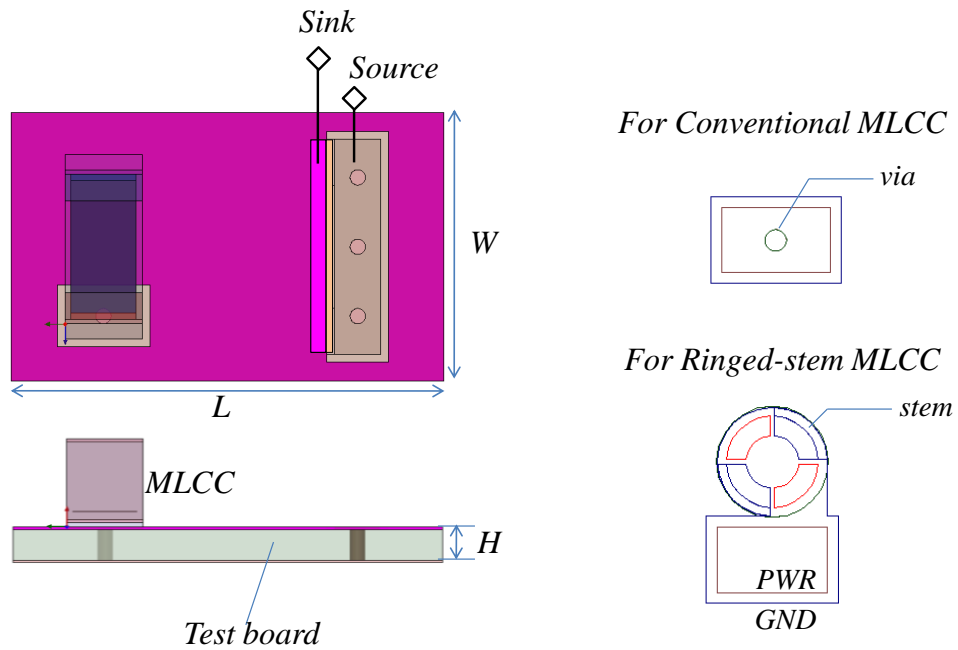
Fig. 1.24. Test configuration for effective inductance simulation.

Fig. 1.25 shows the equivalent circuit of a conventional MLCC and the proposed ringed-stem capacitor. The ringed-stem capacitor includes a capacitive stem that is designed to extend into a printed circuit board and make connections with two or more power distribution planes. In addition, the ringed-stem includes multiple interleaved low-inductance plates. The metal bands may extend at least partially around the outside of the capacitive-stem. In the equivalent circuit, the stem is represented as a capacitance C_2, in parallel with capacitor C_1.
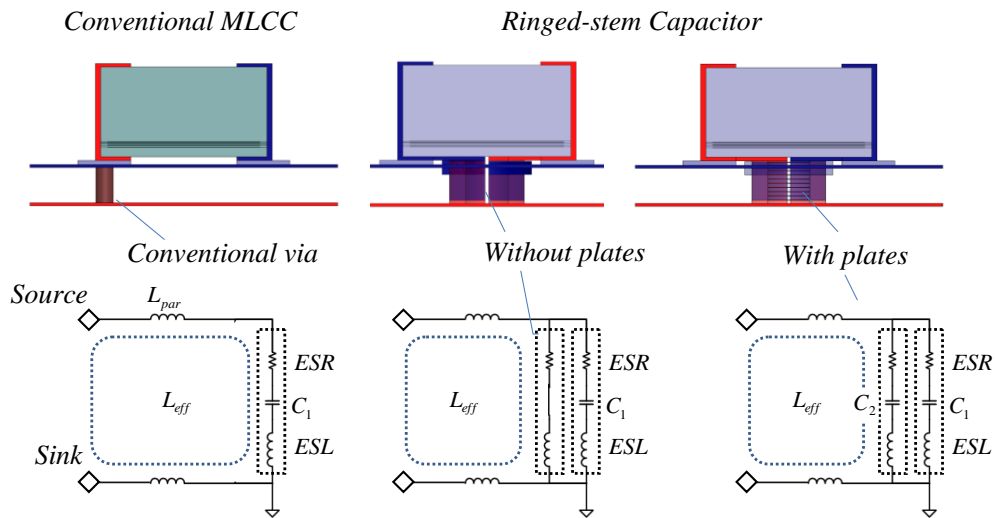
Fig. 1.25. Equivalent circuit of effective inductance loop: conventional MLCC (left), ringed-stem without electrode (middle), and ringed-stem (right).
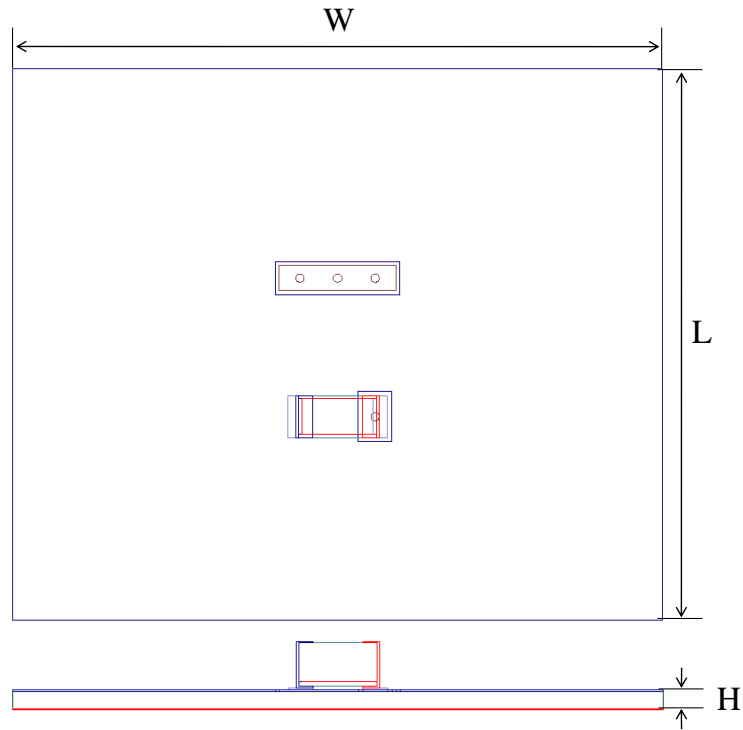
Fig. 1.26. Test board dimensions (L×W×H).

Table 1.5 shows the effective inductance at 1 GHz derived from Q3D Extractor [TM] simulations. The effective inductance of a proposed ringed-stem MLCC without plates is significantly lower than that of a conventional MLCC. The effective inductance of ringed-stem MLCC is slightly lower than that of a ringed-stem MLCC without plates. This shows that the stem, designed to reduce or eliminate the traditional via-loop, contributes to the connection inductance.

As the board size increases in Fig. 1.26, the effective inductance of the connection loop decreases. As the board size approaches that of case 3, the effective inductance becomes less dependent on the board size.

Table 1.5. Effective inductance for three test board sizes

Test board dimension (L×W×H)		Conventional MLCC	Ringed-stem MLCC	
			w/o plates	w/ plates
Case 1	2.81×1.74×0.2 mm	471.1 pH (0.47 nH)	275.9 pH (0.28 nH)	232.9 pH (0.23 nH)
Case 2	3.31×4.2×0.2 mm	432.8 pH (0.43 nH)	232.5 pH (0.23 nH)	185.3 pH (0.19 nH)
Case 3	6.58×7.8×0.2 mm	430.3 pH (0.43 nH)	227.6 pH (0.23 nH)	175.4 pH (0.18 nH)

Table 1.6 shows the effective inductance value for two test board heights. Doubling the height, increases the effective inductance.

Table 1.6. Effective inductance for two test board heights (6.58×7.8×H mm)

Height of board (stem) (H)		Conventional MLCC	Ringed-stem MLCC	
			w/o plates	w/ plates
Case 1	0.2 mm	430.3 pH (0.43 nH)	227.6 pH (0.23 nH)	175.4 pH (0.18 nH)
Case 2	0.4 mm	636.2 pH (0.64 nH)	399.6 pH (0.40 nH)	333.8 pH (0.33 nH)

Figs. 1.27 and 1.28 show how a conventional MLCC and a ring-stem capacitor connect to the power planes of the test board. Table 1.7 shows the dependence of the effective inductance on the diameter of the MLCC power via. The effective inductance is lower for larger diameter vias. Additionally, the connection at the test port contributes to the effective inductance. A solid rectangular block connection to the power plane at the test port has contributes less to the inductance than the three via connection illustrated.

Table 1.7. Effective inductance by the diameter of via (6.58×7.8×0.2 mm)

Conventional MLCC		Power via connection at test port	
Diameter of via (*a₁*)		3 via connection	Whole connection (0.3×1.4 mm)
Case 1	0.10 mm	430.3 pH (0.43 nH)	429.1 pH (0.43 nH)
Case 2	0.21 mm	399.2 pH (0.40 nH)	373.1 pH (0.37 nH)
Case 3	0.42 mm	179.4 pH (0.18 nH)	154.5 pH (0.15 nH)

Conventional MLCC

a_1

Power Via connection at Test port

Whole connection
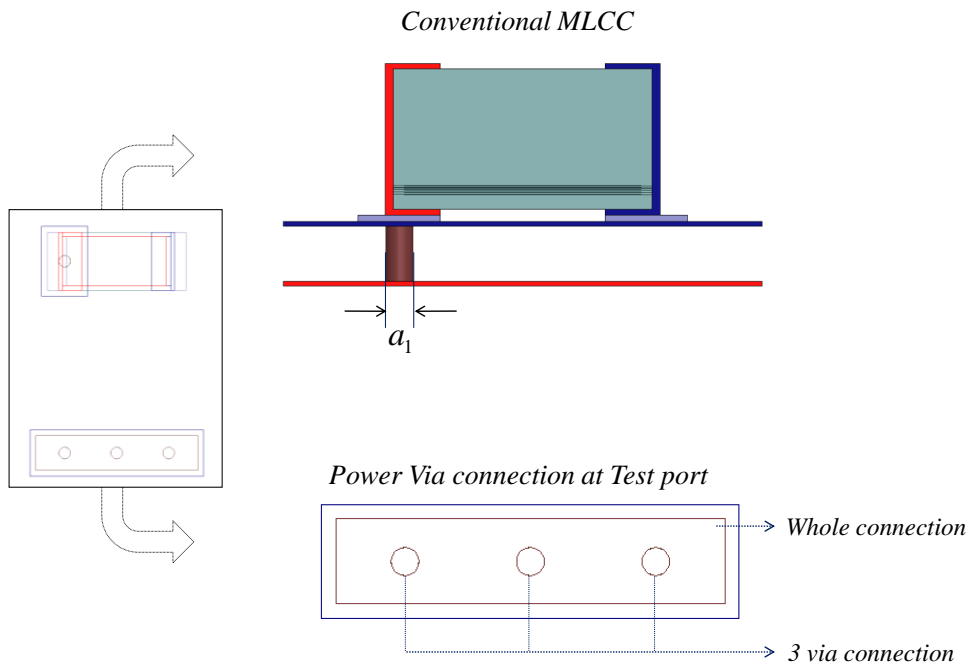
3 via connection

Fig. 1.27. Via connection of conventional MLCC (top) and test port (bottom)

Table 1.8 shows how the diameter of the stem of the proposed ringed-stem capacitor affects the effective inductance. As the diameter of the stem increased, the effective connection inductance of the ringed-stem capacitor decreased. The ringed-stem capacitor with electrodes (plates) in the stem has less inductance than the capacitor without electrodes.

Table 1.8. Effective inductance for two stems diameters (6.58×7.8×0.2 mm)

Ringed-stem MLCC		Power via connection at test port			
Diameter of stem		3 via connection		Whole connection	
(a_2)		w/o plates	w/ plates	w/o plates	w/ plates
Case 1	0.21 mm	0.28 nH	0.21 nH	0.25 nH	0.18 nH
Case 2	0.42 mm	0.22 nH	0.18 nH	0.20 nH	0.15 nH

The simulation results from Table 1.5 to 1.8 show how the connection's effective inductance is dependent on each segment forming the current loop. The wider and shorter each segment is, the smaller the overall loop inductance will be. Additionally, this data shows that the proposed ringed-stem capacitor performs better than a capacitor connected to power planes through a traditional via connection.

Ringed-stem Capacitor

a_2

Power Via connection at Test port

Whole connection
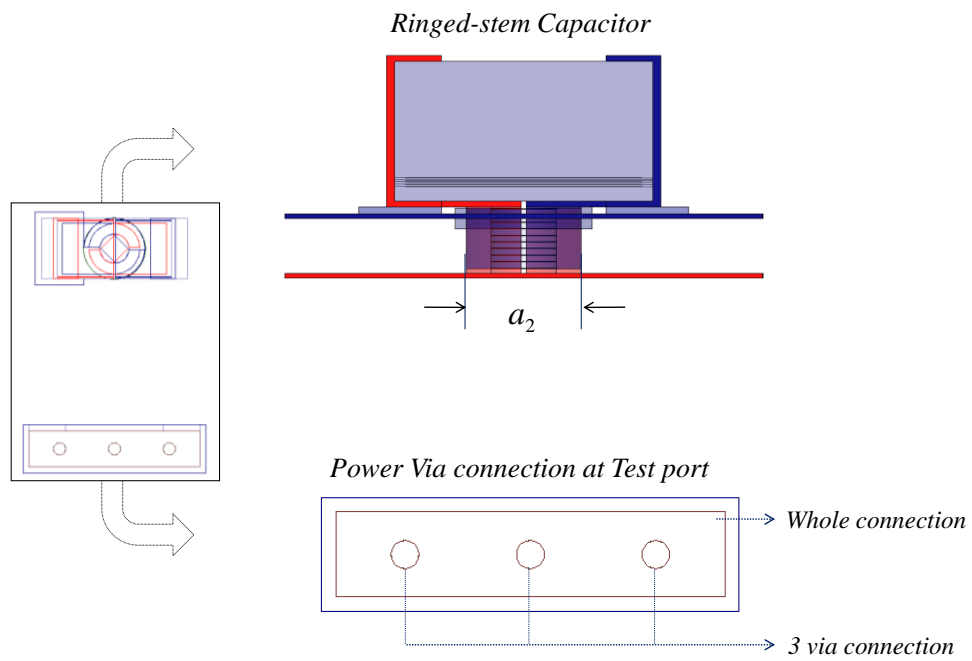
3 via connection

Fig. 1.28. Via connection of ringed-stem capacitor (top) and test port (bottom)

MLCC

G S

G S

G S

G S

$L_{partial}$

S   S

Port 1 C Port 2

G   G

Conventional MLCC

$L_{partial}$

S   S

Port 1 C_{stem} C_{main} Port 2

G   G

Ringed-stem MLCC
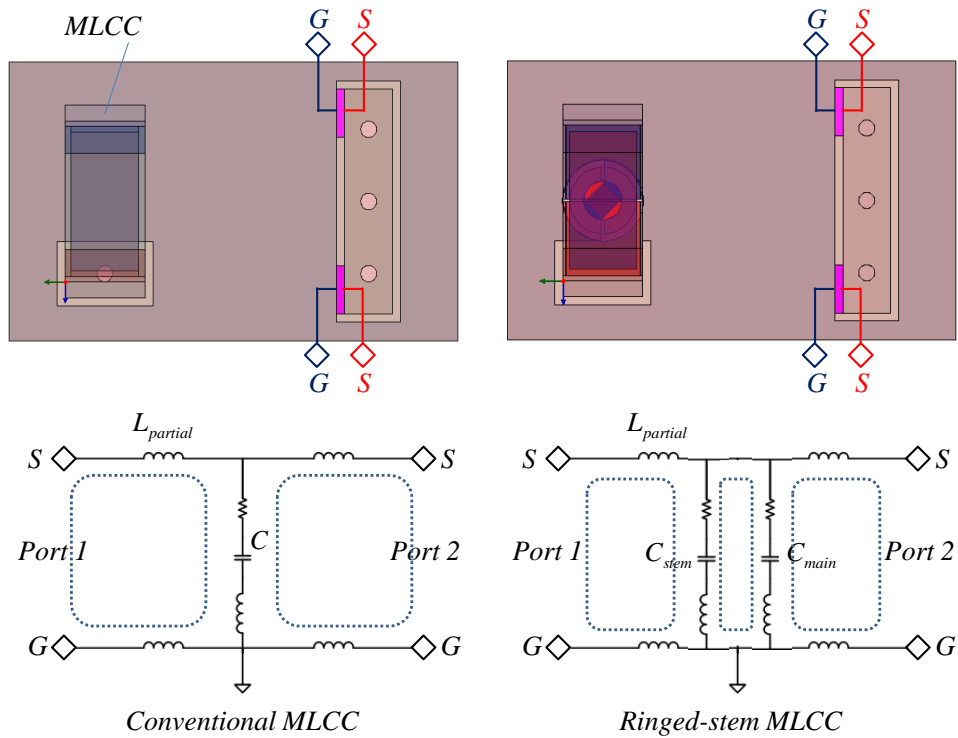
Fig. 1.29. Evaluation configuration and equivalent circuit model for insertion loss.

Transfer function analysis of proposed capacitors

The purpose of decoupling capacitors is to stabilize the voltage on the power bus. The magnitude of the transfer function between two ports at different locations on the planes is an indication of how well the decoupling is performing. Lower values indicate better performance. The $|S_{21}|$ for a standard MLCC and ringed-stem MLCC as illustrated in Fig. 1.25 was calculated using the model in Fig. 1.29 and the full-wave simulation tool, HFSS^{TM}. In an equivalent circuit for this configuration, the stem of ringed-stem MLCC is represented as a smaller capacitor in parallel with the larger capacitance of the MLCC.

Fig. 1.30 shows the simulation results for three types of MLCC: a conventional MLCC, a ringed-stem MLCC without plates and a normal ringed-stem MLCC. The equivalent circuit of the stem, as shown in Fig. 1.30, is represented as a series R-L-C circuit in parallel with the circuit representing the MLCC. Due to the lower overall effective inductance, the resonance frequency of the ringed-stem capacitor is at a higher frequency than that of the conventional MLCC. At frequencies above the self-resonance of both capacitors, the $|S_{21}|$ of the ringed-stem MLCC is 10 dB higher than that of the conventional MLCC. Above the frequency where the stem plate resonates, the performance of the ringed-stem MLCC with plates in the stem is 2–3 dB better than that of the ringed-stem MLCC without electrodes.
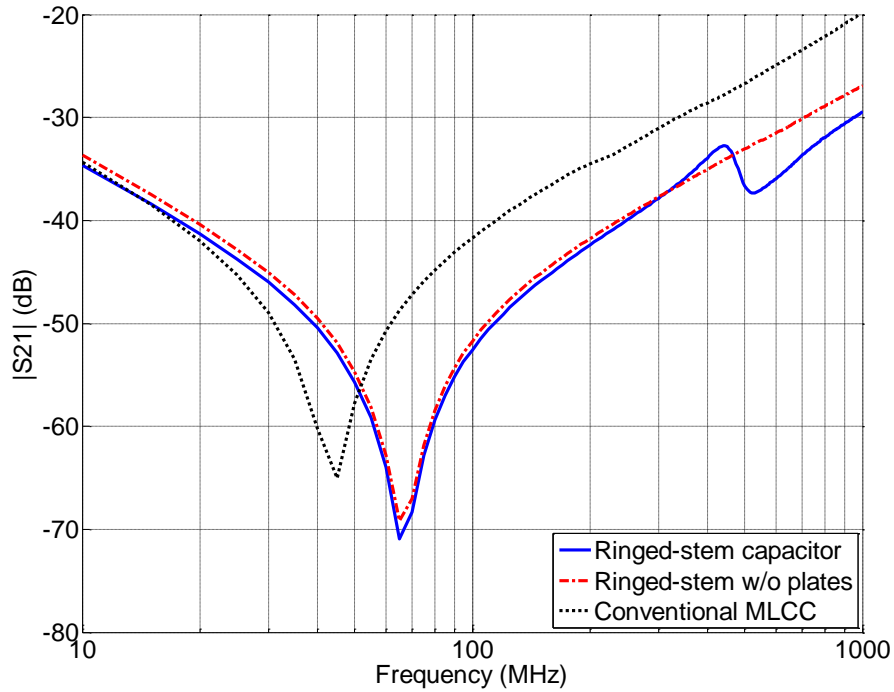
Fig. 1.30. Full-wave simulation responses for the proposed capacitors.

V. CONCLUSION

Power bus decoupling inductance for high performance packaging in computing applications is dependent on the size of the conductors forming the current path from the switching device to the decoupling capacitor and the overall loop area. Advanced packaging geometries employing stacked silicon wafers, through-silicon vias, new organic and ceramic substrates, micro-bumps and other unique structures provide unique opportunities for implementing novel low-inductance decoupling schemes employing multilayer ceramic capacitors (MLCCs). Section II of this paper discussed the effect of plate orientation in MLCCs and concluded that plate orientation does not have a

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significant effect on the connection inductance of an MLCC of given dimensions. Section III outlined the relative significance of die-level, package-level and board-level decoupling. This section showed that higher frequency decoupling is easier to achieve close to the die level, while lower frequency decoupling is easier to achieve further from the die.

Section IV describes "ringed-stem" capacitors that reduce connection inductance by moving some of the capacitance between the planes of a power distribution bus. The improvement in connection inductance was demonstrated using 2-D and 3-D simulations.

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CHAPTER TWO

INVESTIGATION OF THE IMBALANCE DIFFERENCE MODEL AND ITS
APPLICATION TO VARIOUS CIRCUIT BOARD AND CABLE GEOMETRIES

Abstract

The imbalance difference model introduced by Watanabe is a method for modeling how differential-mode signal currents are converted to common-mode noise currents. A parameter called the current division factor (CDF) or imbalance factor uniquely defines the degree of imbalance of a transmission line. The imbalance difference model shows that changes in the imbalance are responsible for differential-mode to common-mode conversion. This paper explores various cable geometries to determine how well Watanabe's values of DM-to-CM conversion compare to full-wave calculations. This paper also demonstrates how the imbalance difference model can be applied to cables with more than two conductors.

I. INTRODUCTION

Determining the distribution of signal and noise currents in circuit boards or electronic systems is an important step in analyzing sources of electromagnetic interference. In a two-conductor transmission line, currents that flow in one direction on one conductor and in the opposite direction on the other conductor (differential-mode) are not likely to be a significant source of radiated emissions. On the other hand, currents that flow in the same direction on both conductors (common-mode) are often a primary

source of radiated emissions [1]. While the differential-mode currents are generally intentional, common-mode currents are often the result of unintentional differential-to-common-mode conversion resulting from electrical imbalance.

Several models have been introduced to describe differential-mode to common-mode conversion. Hockanson [1] introduced current-driven and voltage-driven source models to describe how differential-mode signals on circuit boards induce common-mode currents on attached wires.

An equivalent model for estimating the radiated emissions from a printed circuit board with attached cables driven by a signal voltage on a trace was developed by Shim [4]. This model employed an equivalent common-mode voltage source located at the junction between the PCB ground structure and the attached wire. The magnitude of the common-mode voltage was proportional to the ratio of the self-capacitance of the trace to the return plane of PCB structure (effectively a measure of imbalance).

Watanabe [6] introduced the concept of an *imbalance difference factor* to quantify the electrical imbalance of various transmission line configurations. He showed that imbalance is not responsible for the conversion of differential-mode currents to common-mode currents. Instead, it is *changes* in imbalance that facilitate this conversion. Using various printed circuit board structures as examples, he showed that it is possible to calculate the common-mode currents by replacing the differential-mode source with equivalent common-mode sources at points where changes in the imbalance occur. This *imbalance difference* modeling technique can greatly simplify the analysis of radiated emissions due to common-mode currents.

In this paper, the imbalance difference theory is extended to apply to structures with more than one differential-mode current. The procedure is demonstrated using a three-phase power system example, but can be generally extended to apply to multi-wire cable geometries in other applications.

II. THE IMBALANCE DIFFERENCE MODEL

A two-wire transmission line circuit with a voltage source (V_S), source impedances (Z_{S1}, Z_{S2}, Z_{SG1}, and Z_{SG2}), load impedances (Z_{L1}, Z_{L2}, and Z_{LG}), and cable impedances ($Z_{CableG1}$ and $Z_{CableG2}$) is shown in Fig. 2.1. The currents, I_1 and I_2 flow on each transmission line conductor. These currents can be decomposed into differential-mode and common-mode components. If we assume that the two conductors are perfectly balanced ($Z_{S1} = Z_{S2}$, $Z_{SG1} = Z_{SG2}$, $Z_{L1} = Z_{L2}$, $Z_{CableG1} = Z_{CableG2}$), the currents, I_1 and I_2, have equal magnitude but opposite direction and the common-mode component is zero. If one side of the circuit has a different impedance to ground than the other side, then the circuit is not perfectly balanced. According to the imbalance difference theory, and change in the imbalance in a circuit results in the conversion of differential-mode currents into common-mode current. We can define a current division factor (or *imbalance factor*), h, that describes how much of the common-mode current flows on each conductor,

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h & 1 \\ 1-h & -1 \end{bmatrix} \begin{bmatrix} I_{CM} \\ I_{DM} \end{bmatrix} \tag{1}$$

where $0 \le h \le 1$, and perfect balance is achieved when $h = 0.5$.

In an unbalanced circuit, the common-mode current is not divided equally between the two conductors. Rearranging Eq. (1), the currents, I_1 and I_2 can be decomposed into common-mode and differential-mode components,

$$\begin{bmatrix} I_{DM} \\ I_{CM} \end{bmatrix} = \begin{bmatrix} 1-h & -h \\ 1 & 1 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{2}$$
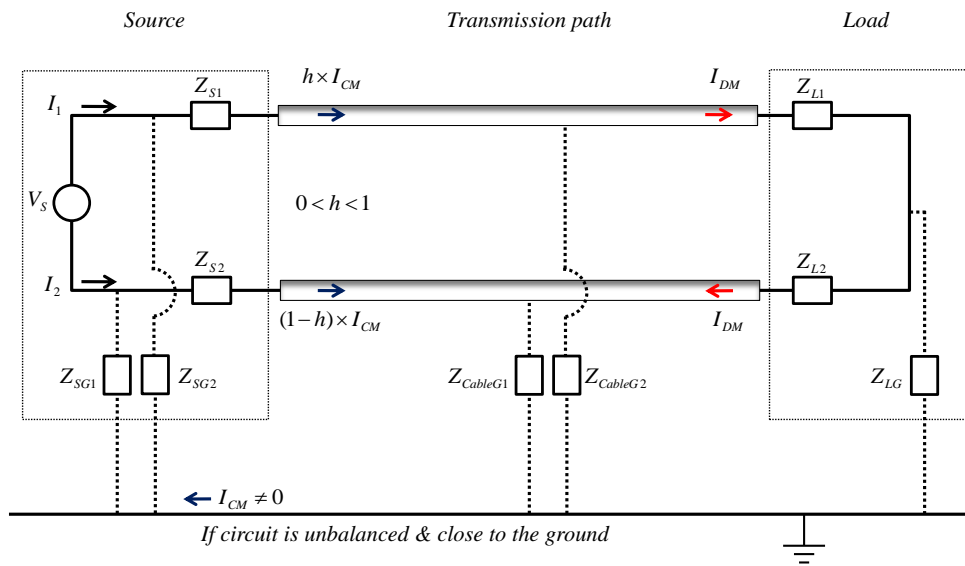
Fig. 2.1. Current flow decomposition of two-transmission line circuit.

The imbalance difference method is a method for modeling how differential-mode signal currents are converted to common-mode noise currents. Watanabe [6] showed that the imbalance factor can be determined from the capacitances of each conductor to ground.

(*a*) Two-wire transmission line (*b*) Microstrip structure
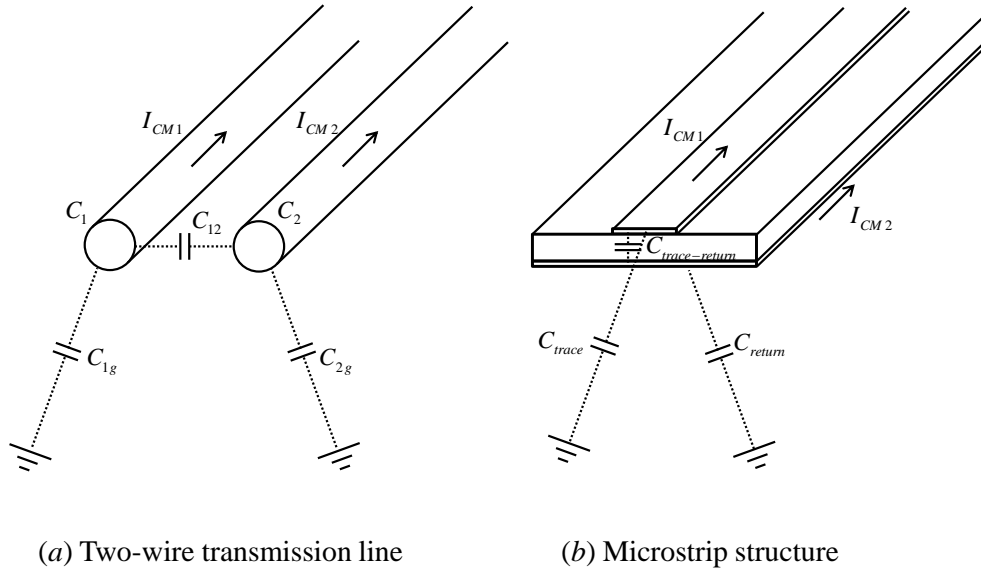
Fig. 2.2. Stray capacitance for two transmission geometries.

For example, for the transmission line geometries in Fig. 2.2, the imbalance factor, *h*, can be described in terms of the per-unit-length capacitances [6],

$$h = \frac{C_{1g}}{C_{1g} + C_{2g}} . \tag{3}$$

For TEM propagation, this can be shown to be equal to the static charge distribution that is obtained when both conductors have the same voltage relative to ground,

$$h = \frac{Q_1}{Q_1 + Q_2} . \tag{4}$$

Note that "ground" may be a nearby metal structure (e.g. a ground plane or chassis), or it may represent a point far away (e.g. at infinity). When the ground is nearby, the common-mode currents are generally the currents that return to the source on

this ground conductor. When the ground is far away, the common-mode currents are "antenna mode" currents that return to the source as displacement current. The imbalance difference method applies equally well in either situation. In order to evaluate the common-mode current distribution on an EMI antenna structure, the imbalance difference model postulates that the common-mode currents on a transmission line can be precisely determined by removing all differential-mode sources from a circuit and placing equivalent common-mode sources at all points where a change in the imbalance occurred. The amplitude of these equivalent voltage sources is given by

$$V_{CM} = \Delta h \times V_{DM}(x) \tag{5}$$

where Δh is the changed in the imbalance factor and V_{DM} is differential-mode voltage at the point where the change in imbalance occurs.

III. MODELING OF COMMON-MODE CURRENT DISTRIBUTIONS

Wire model with voltage and current driven source

A two-wire transmission line with one of the wires extended at both ends is illustrated in Fig. 2.3 [1]. The electrical length of the entire circuit is short in terms of the free-space wavelength (10 m at 30 MHz). The wire radius is 0.8 mm. The vertical wires have a length of 10 mm. $V_S = 1$ volt at 30 MHz. $R_S = 50$ Ω. The length of each wire attached to the loop circuit is 30 cm.
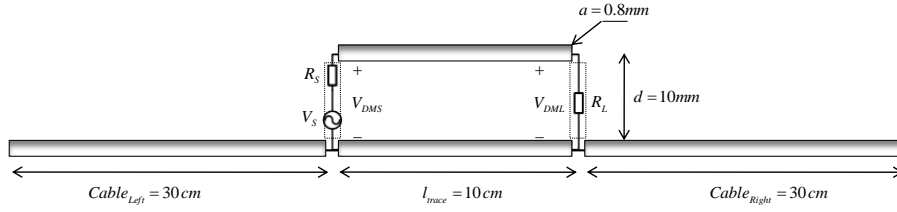
(a) Original circuit
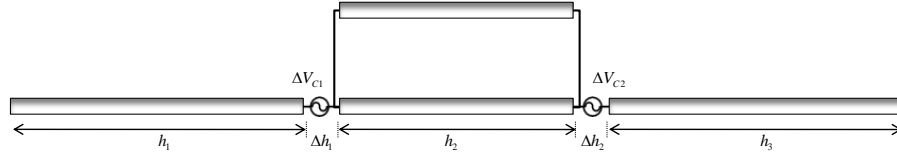
(b) Imbalance difference model

Fig. 2.3. A wire circuit geometry and its equivalent imbalance difference model.

The common-mode current induced in this structure including the two wires on each side of the circuit was computed using a full-wave electromagnetic modeling code [16]. Simulations were run with three load impedances: an open circuit, a short circuit and a 50-Ω load.

The magnitude of the common-mode current for the open circuit ($R_L = \infty$) case is indicated by the solid black curve in Fig. 2.4. Note that the common-mode current peaks at either end of the transmission line structure and is zero at the center.

The solid blue curve shows the magnitude of the common-mode current for the short circuit case ($R_L = 0$). In this case, the common-mode current peaks at the source end of the transmission line. The solid red curve shows the common-mode current when $R_L = 50\ \Omega$, which is a superposition of the currents for the short- and open-circuit cases.

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Table 2.1. Voltages for the circuits in Fig. 2.3.

Source/Load impedance	V_{DMS}	ΔV_{C1}	V_{DML}	ΔV_{C2}
$R_S = 50\,\Omega,\ R_L = 50\Omega$	$0.53 \angle 9.8$	$0.26 \angle 9.8$	$0.49 \angle -11.1$	$0.25 \angle 168.9$
$R_S = 50\,\Omega,\ R_L = open$	$1 \angle 0$	$0.5 \angle 0$	$1 \angle 0$	$0.5 \angle 180$
$R_S = 50\,\Omega,\ R_L = short$	$0.36 \angle 69.2$	$0.18 \angle 69.2$	0	0

According to the imbalance difference model, the geometry in Fig. 2.3(b) is equivalent to the geometry in Fig. 2.3(a) in terms of the common mode currents produced. The amplitude of the equivalent voltage sources is determined by (6). Table 2.1 shows the common-mode excitation voltages, ΔV_{C1} and ΔV_{C2}, for each load impedance when the differential-mode source voltage is 1 V. The differential-mode voltage, V_{DMS} at the source location was calculated as

$$V_{DMS} = V_S \frac{Z_{in}}{R_S + Z_{in}}, \tag{6}$$

where Z_{in} is the input impedance of the transmission line.

Full-wave common-mode current calculations for the structure in Fig. 2.3(b) are indicated by the dotted lines in Fig. 2.4. These results are labeled IDM (for Imbalance Difference Model) and are virtually identical to the results obtained by the analysis of the original configuration in Fig. 2.3(a).

The imbalance difference model for the open-circuit case consists of two equal and opposite sources located at each end of the transmission line structure. The symmetric nature of this model makes it clear that the common-mode currents be zero at the center.

The imbalance difference model for the short-circuit case has only one non-zero equivalent source located at the source end of the transmission line. It is clear from the model that the common-mode currents must peak at the source end of the transmission line and decrease to zero at the end of each wire. This simple example demonstrates both the accuracy of the imbalance difference model, and its ability to provide an intuitive understanding of how and where differential-mode currents are converted to common-mode currents.
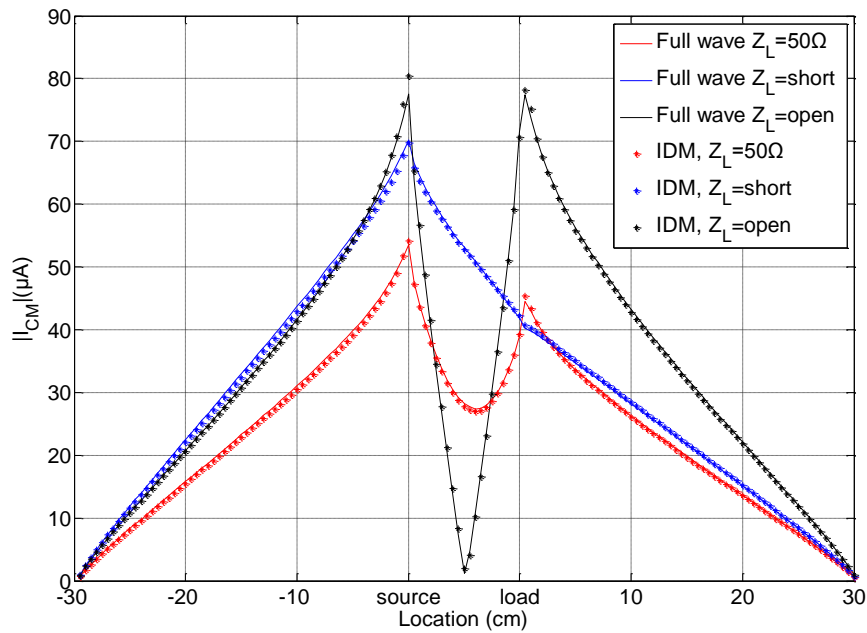
Fig. 2.4. Common-mode current distribution at 30 MHz.

Cable structure attached to a PCB

Fig. 2.5 shows a simple printed circuit board configuration and its equivalent imbalance difference model. The return plane dimensions are 10 cm by 4 cm. A 1-mm wide trace is located 3 mm above the plane (this dimension is exaggerated in the figure for clarity), and a 100-cm wire is attached to the return plane of the board and oriented horizontally. A 1-volt source in series with a 50-Ω source impedance is located between trace and the return plane at the left side of the board. The other side of the trace is terminated with a 50-Ω resistor. The board is located far away from any other conductors.
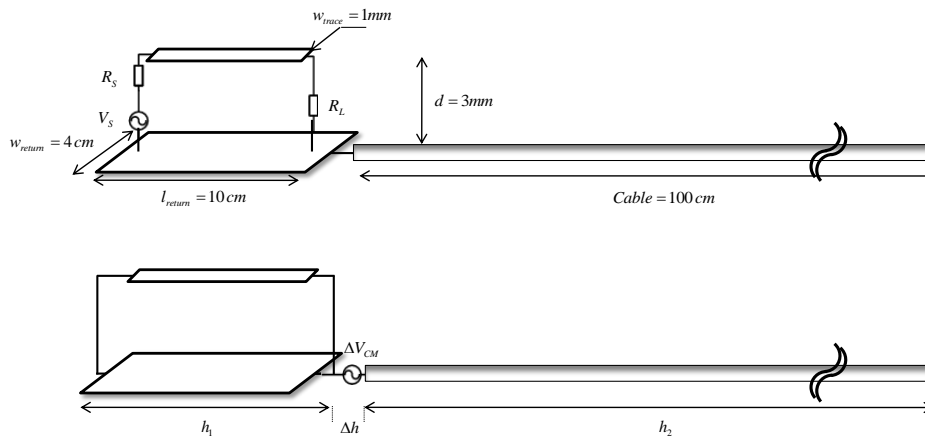
Fig. 2.5. PCB model with attached wire (top) and its imbalance difference model (bottom).

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The imbalance factor, h, for the imbalance difference model is obtained from the ratio of the stray capacitance of the trace to the stray capacitance of the return plane of the board as described in (3), where the "ground" is at infinity because we are interested in the antenna-mode currents induced on the wire. The stray capacitance of the trace and the return plane of the board can be computed by two methods: an approximate closed-form solution or a 2D-FEM simulation.

A closed-form solution for the stray capacitance of a trace in a microstrip structure is provided in [3],

$$C_t \approx \frac{6.189}{\pi} \frac{d}{W} \frac{C_{DM} l_t}{\ln\left[1 + 3.845\left(\frac{L}{W}\right)\right]}, \tag{7}$$

where W and L are the width and the length of the board, l_t is length of the trace, d is the distance between the trace and the return plane of the board, and C_{DM} is the capacitance of the trace over an infinitely wide return plane. The stray capacitance of the board is defined as [4],

$$C_{board} \approx 8\varepsilon_0 \sqrt{\frac{Board\ Area}{\pi}}. \tag{8}$$

Table II shows the capacitances and imbalance factors calculated using the closed form equations and also those calculated using a 2D FEM simulation [17].

Table 2.2. Comparison of h-parameter calculation

	C_{board}	C_{trace}	h_1
Closed form	2.53	0.11	0.042
FEM	2.57	0.08	0.048

Fig. 2.6 shows the magnitude of the common-mode current induced on the attached cable as determined by a full-wave model of the entire configuration, an IDM model based on the imbalance factors computed by the 2D FEM code, and an IDM model based on the closed form calculations of the imbalance factor. The magnitude of the common-mode current is highest at the junction between the printed circuit board and the wire. There is excellent agreement between the full-wave model and the imbalance difference model (IDM) employing the 2D FEM. Both models calculate a current of approximately 12 μA at the board-cable junction. The IDM results obtained using the closed-form imbalance factor estimates a slightly lower magnitude, ~10 μA.
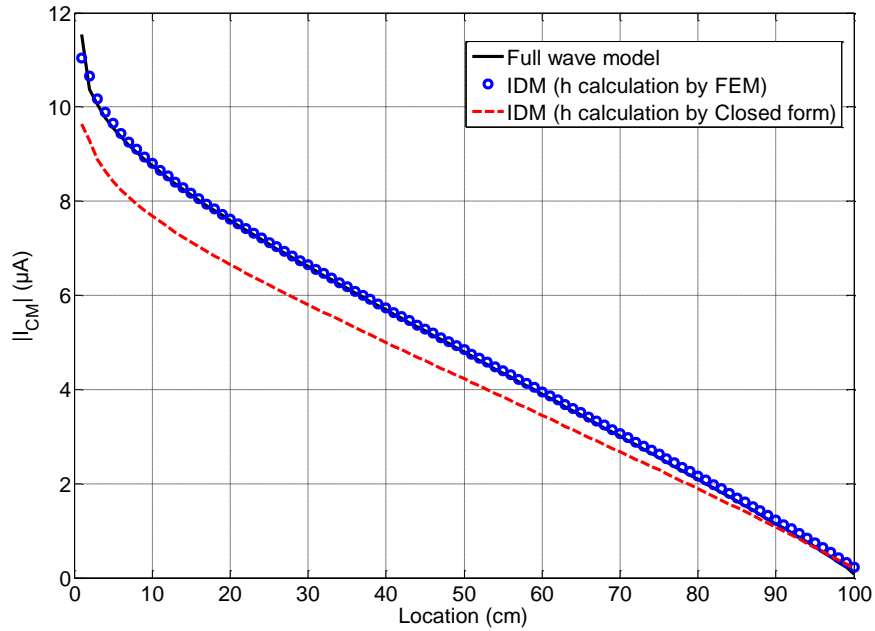
Fig. 2.6. Common-mode current distribution at 30 MHz.

Long wire model with imbalance

Fig. 2.7 shows a 2-wire transmission line structure where the radius of one wire changes in the middle represented as the sum of two alternative structures: one that is perfectly balanced and carries only differential-mode currents, and one that is the equivalent IDM model and carries only common-mode current [10]. From the imbalance difference model, we know that the change in the balance occurring at the center of the transmission line will result in a common-mode current distribution that peaks in the center and goes to zero at both ends.
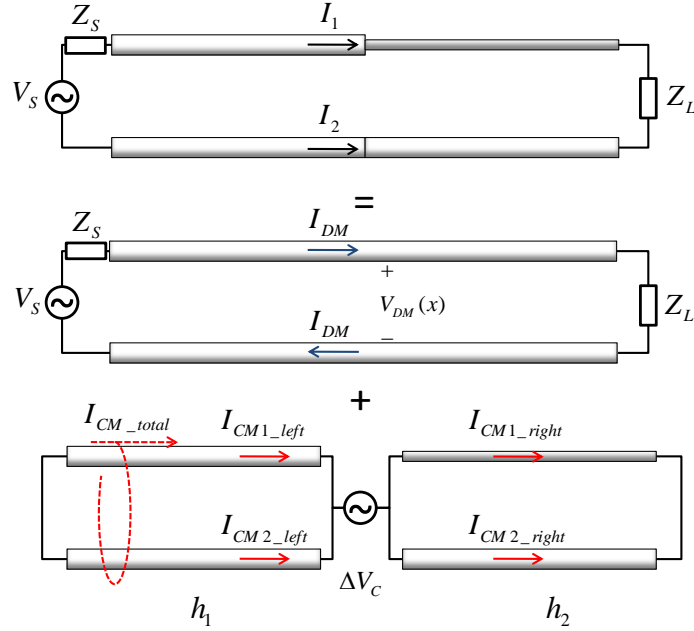
Fig. 2.7. Long wire circuit (top) and its decomposition (transmission line and antenna mode).

Fig. 2.8 shows the dimensions of the wires in the configuration modeled. The right half of the transmission line has different wire radii, *a* and *b*. The characteristic impedance of this part of the transmission line can be calculated as [14],

$$Z_{01} = 60 \cosh^{-1}\left[\frac{1}{2}\left(\frac{d^2}{ab} - \frac{a}{b} - \frac{b}{a}\right)\right]. \tag{9}$$

The wires on the left half of the transmission line have the same radius, *a*. The characteristic impedance of this transmission line can be calculated from [14] as,

$$Z_{02} = 120 \cosh^{-1}\left(\frac{d}{2a}\right) \tag{10}$$
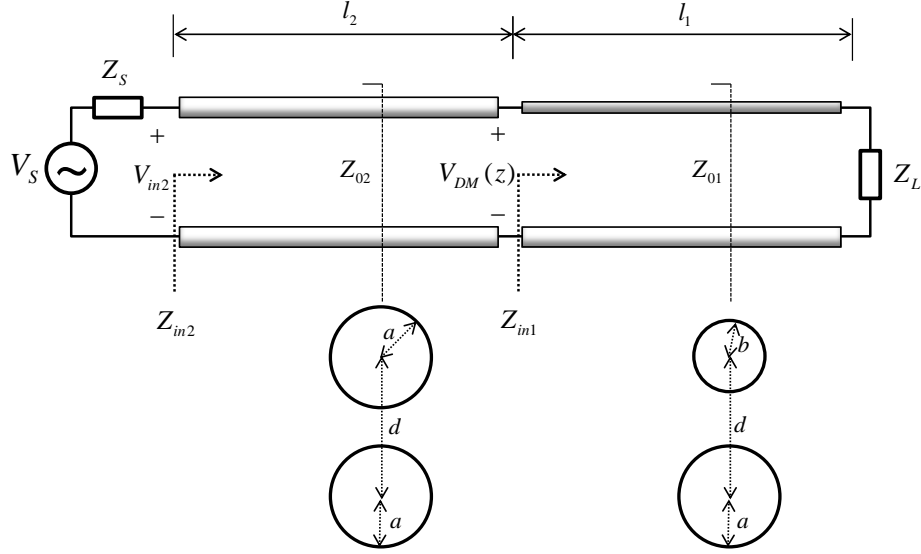
Fig. 2.8. Cross-sectional view of Fig. 2.7 transmission line structure.

At the source location, the input voltage is,

$$V_{in2} = V_S \frac{Z_{in2}}{Z_S + Z_{in2}}, \tag{11}$$

where $Z_{in2} = Z_{02} \dfrac{Z_{in1} + jZ_{02}\tan(\beta l)}{Z_{02} + jZ_{in1}\tan(\beta l)}$ *and* $Z_{in1} = Z_{01} \dfrac{Z_L + jZ_{01}\tan(\beta l)}{Z_{01} + jZ_L\tan(\beta l)}$.

At the location of the discontinuity, the differential-mode voltage is

$$V_{DM}(l_1) = V_S \frac{Z_{in2}}{Z_S + Z_{in2}} \left(\frac{1 + \rho_L}{e^{j\beta l_2} + \rho_L e^{-j\beta l_2}} \right), \tag{12}$$

where $\rho_L = \dfrac{Z_{in1} - Z_{02}}{Z_{in1} + Z_{02}}$.

The amplitude of the equivalent common-mode voltage source can be calculated from (5) using the differential-mode voltage determined from (12).

Two parallel wires having radius a_1 and a_2, respectively, and a separation distance, d, can be modeled by one wire having an equivalent radius a_e where [15],

$$\ln(a_e) \cong \frac{1}{(S_1 + S_2)^2} \times \left[S_1^2 \ln a_1 + S_2^2 \ln a_2 + 2S_1 S_2 \ln d \right] \tag{13}$$

as illustrated in Fig. 2.9. Typically, when applying the imbalance difference model, the equivalent source drives all the conductors on one side of the imbalance discontinuity relative to all conductors on the other side of the discontinuity as illustrated by the configuration labeled "IDM" in Fig. 2.9. In many cases, it is possible to represent the conductors on each side of the discontinuity with a single conductor as illustrated by the configuration labeled "Equivalent Dipole Antenna" in Fig. 2.9.
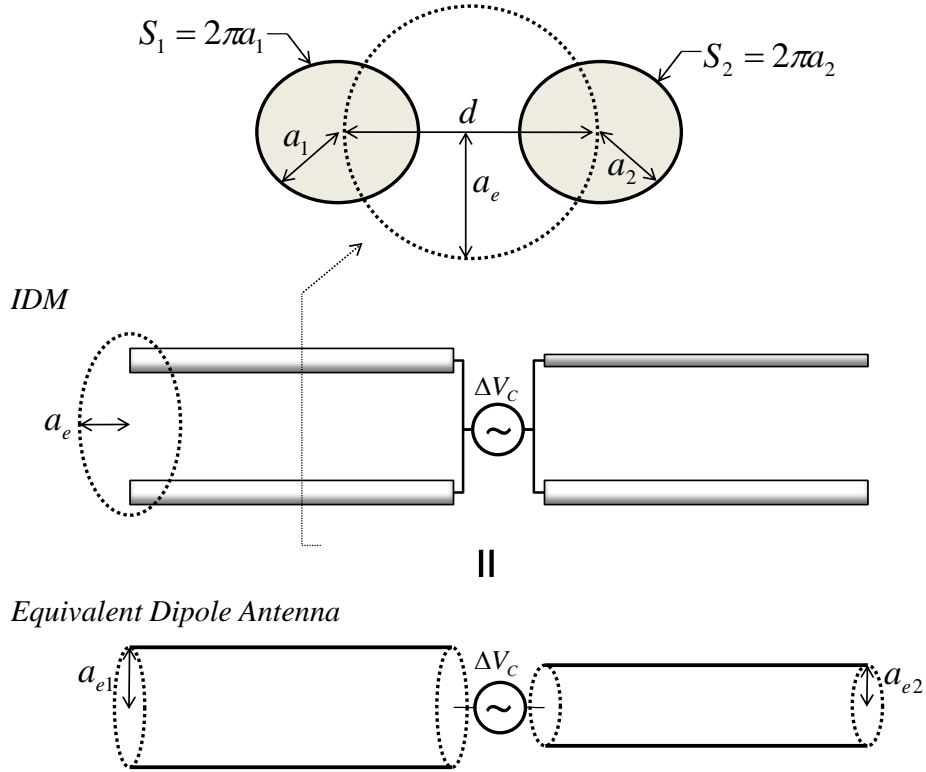
Fig. 2.9. Equivalent geometric conversion from two conductors to one [15].
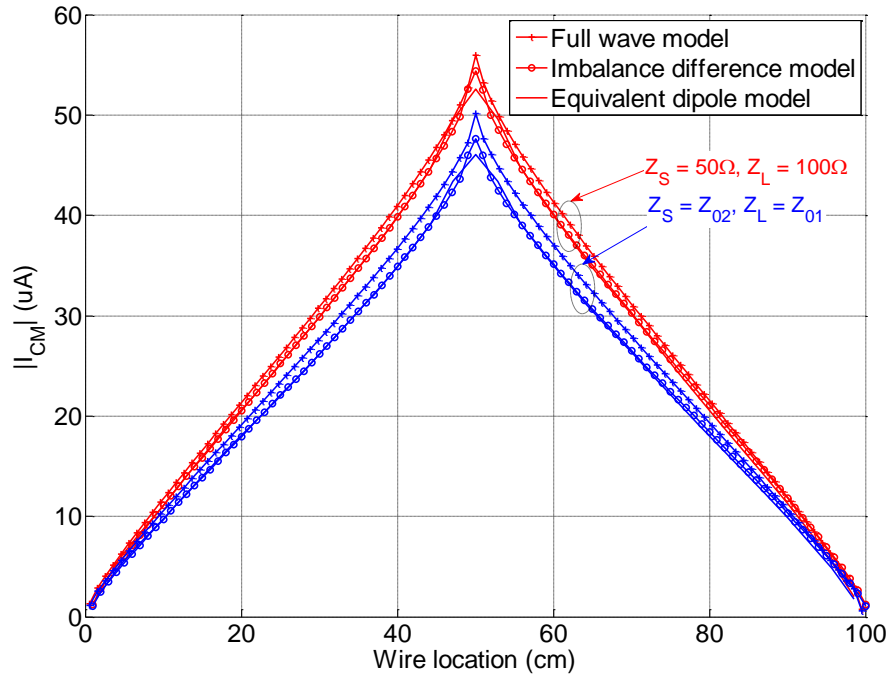
Fig. 2.10. Common-mode current on the structure in Fig. 2.8 (matched and unmatched).

Fig. 2.10 shows the common-mode currents obtained from a full-wave model of the whole configuration, an IDM model and an equivalent dipole antenna driven by an IDM equivalent source. The excitation frequency is 30 MHz and the wire is 100 cm long (50 cm per section). Each wire on the left half of the transmission line has same radius, 2.5 mm; however on the right half of the transmission line the radius of one of the wires decreases to 1.25 mm. The center-to-center spacing of the wires is 7.5 mm. The red curves were obtained with source and load impedances that were mismatched to the characteristic impedance of transmission line. In this case, the source impedance was 50 Ω and the load impedance was 100 Ω. The characteristic impedances of each half of the transmission lines, Z_{01} and Z_{02} are 164.2 and 115.5 Ω, respectively. The blue curves were

obtained with source and load impedances that were matched to the characteristic impedance of the transmission line. The source impedance was $Z_{02} = 115.5 \ \Omega$ and the load impedance was $Z_L = Z_{01} = 164.2 \ \Omega$. The magnitude of common-mode current was lower when impedances were matched because the differential-mode voltage at the point of the imbalance change was lower.

IV. MULTIWIRE CONFIGURATIONS
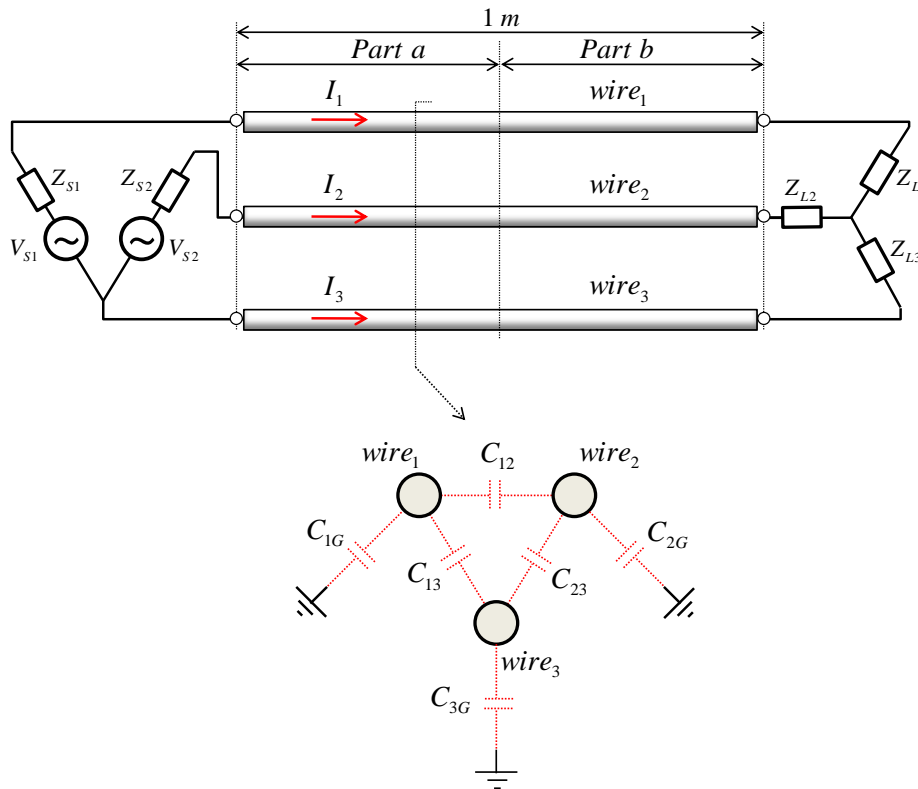
Fig. 2.11. A three-phase circuit with two differential-mode sources and y-connected loads.

Previous work published in the literature has not addressed the problem of multiwire configurations where there are multiple differential-modes. For example, in a three-phase transmission line, two independent differential mode currents can be defined. The three-phase system illustrated in Fig. 2.11 has two independent differential-mode voltage sources, V_{S1} and V_{S2}. The system is terminated by three load impedances, Z_{L1}, Z_{L2}, and Z_{L3}, connected in a "Y" configuration. A change in the radius of one or more wires in the middle of the transmission line creates an imbalance difference that causes differential-mode to common-mode conversion.

Superposition of multiple common-mode excitation

Since there is more than one differential-mode signal that may be converted to common-mode current, more than one equivalent source is required to model this conversion. The total common-mode current in a three-phase system is the sum of the currents flowing on each wire,

$$I_{CM} = I_1 + I_2 + I_3 \tag{14}$$

Each of the differential-mode signals encountering a change in imbalance contributes to this common-mode current. In Fig. 2.11, we've chosen wire 3 as the reference for our two independent differential-mode signals, so we denote the voltage between lines 1 and 3 with the subscript "1" and the voltage between lines 2 and 3 with the subscript "2". Quantities on the left- and right-hand sides of the imbalance discontinuity are denoted by the subscripts "a" and "b", respectively. Using this notation,

we can define four imbalance factors corresponding to the imbalance associated with the

two differential-mode signals on the left- and right-hand sides of the transmission line;

$$h_{1a} = \frac{C_{1Ga}}{C_{1Ga} + C_{2Ga} + C_{3Ga}} \ , \ h_{1b} = \frac{C_{1Gb}}{C_{1Gb} + C_{2Gb} + C_{3Gb}} \tag{15-a}$$

$$h_{2a} = \frac{C_{2Gb}}{C_{1Gb} + C_{2Gb} + C_{3Gb}} \ , \ h_{2b} = \frac{C_{2Gb}}{C_{1Gb} + C_{2Gb} + C_{3Gb}} \ . \tag{15-b}$$

where, C_{iGn} means the self-capacitance (capacitance to ground at infinity) of the ith

conductor on side n.
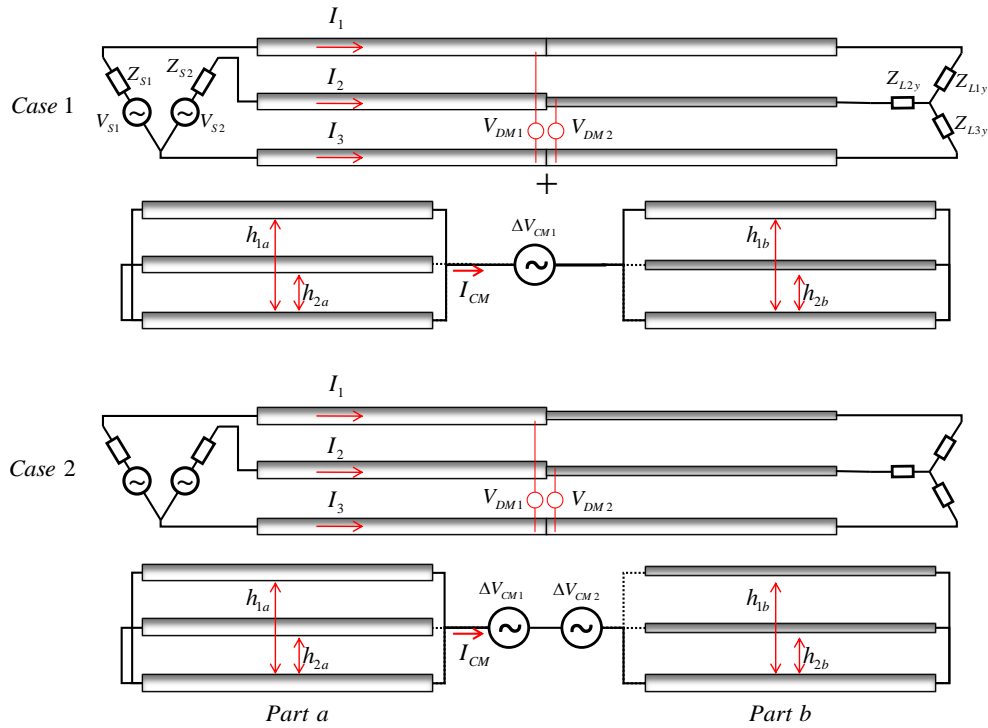
Fig. 2.12. Imbalance difference models for 2 three-phase circuits.

The equivalent common-mode voltages at discontinuity points were defined by

the following equations based on the superposition theorem as illustrated in Fig. 2.12.

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$$V_{CM1} = \Delta h_1 V_{DM1} + \Delta h_2 V_{DM2} \tag{16}$$

$$V_{CM2} = \Delta h_1 V_{DM1} + \Delta h_2 V_{DM2} \tag{17}$$

where V_{DMi} is the ith independent differential-mode voltage at the point of the imbalance change and $\Delta h_1 = h_{1b} - h_{1a}$, $\Delta h_2 = h_{2b} - h_{2a}$.

The total common-mode excitation due to imbalance difference is the sum of the common-mode excitations,

$$V_{CM} = V_{CM1} + V_{CM2}. \tag{18}$$

In general, for multi-wire transmission lines, the equation for the equivalent common-mode source voltage is,

$$V_{CM} = \sum_i \Delta h_i V_{DMi} \tag{19}$$

where V_{DMi} is the ith independent differential-mode voltage at the point of the imbalance change, and Δh_i is the change in the imbalance experienced by that component of the signal.

Multiple common-mode excitations due to the imbalance in a circuit with multiple wires can be described as the sum of each common-mode excitation as illustrated in Fig. 2.12. Case 1 is an example where one wire's diameter changes in the middle of the cable. In Case 2, two wires exhibit a change in diameter.

$\sum V_{CMi}$	Part a	Part b
Case 1 (V_{CM1})		
Case 2 ($V_{CM1} + V_{CM2}$)		

Fig. 2.13. Detailed geometry expression for multiple common-mode excitations.

Fig. 2.13 shows the cross-sections of the wire geometries in Fig. 2.12. The circuits evaluated have two differential-mode voltage sources with 1-V amplitudes and 50-Ω source impedances connected to three y-connected 50-Ω resistors. The transmission line between the source and load is 1 meter long. As illustrated in Fig. 2.13, two cases were modeled. In Case 1, there is one discontinuity resulting in one equivalent common-mode source. In Case 2, there are two discontinuities and two equivalent common-mode sources.

Fig. 2.14 compares the common-mode currents on the original structure (solid curve) to the common-mode currents on the IDM structure (dotted curves) for each case (calculated using FEKO [16]). The blue curves are the results for Case 1 and the black

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curves are the results for Case 2. In each case, there is excellent agreement between the original circuit results and the imbalance difference model results.
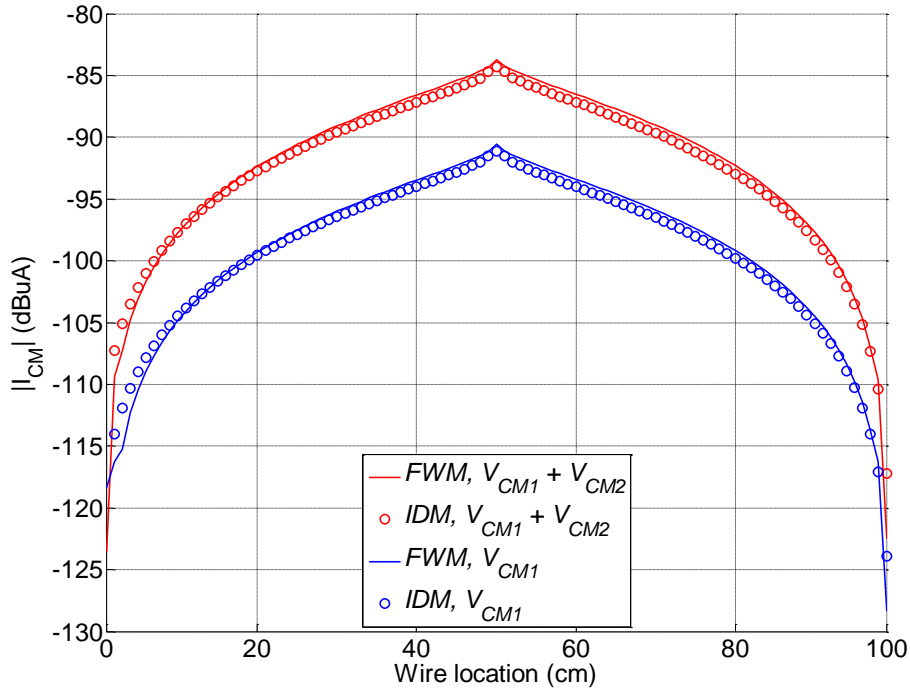
Fig. 2.14. Two differential-mode sources and single imbalance wire.

V. CONCLUSION

The imbalance difference model describes how changes in the imbalance of a circuit result in the conversion of differential-mode signals to common-mode noise. A parameter called the *current division factor* (CDF) or *imbalance factor* uniquely defines the degree of imbalance experienced by a differential-mode signal at any location as it moves through a circuit. Various cable and printed circuit board geometries have been evaluated to illustrate how calculations of the common-mode currents on structures can

be simplified and better understood using the imbalance difference model. A technique for applying the imbalance difference model to multiwire structures with more than one differential-mode signal was also introduced. This technique superimposes the equivalent common-mode voltage sources for each independent differential-mode signal that encounters a change in electrical imbalance.

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CHAPTER THREE

A NOVEL BALANCED CABLE INTERFACE FOR REDUCING COMMON-MODE
CURRENTS FROM POWER INVERTERS AND OTHER ELECTRONIC DEVICES

Abstract

Common-mode current is a significant source of radiated emissions from power
inverters. In an ideal power inverter, the currents flowing in one direction on the wires
between the inverter and the load are exactly equal to the currents flowing in the opposite
direction in the same wire bundle. Unfortunately, imbalances in the switching
components and circuit geometry can cause the electrical potential of the wire bundle to
change with time resulting in common-mode currents. Most inverters employ pulse-width
modulated switching at frequencies below 100 kHz. Balancing an inverter at low
frequencies without affecting the performance or efficiency of the inverter can be
challenging. However, radiated emissions are more likely to be a problem at higher
frequencies (e.g. >30 MHz). One method for reducing common-mode current emissions
at high frequencies is through the use of common-mode or differential-mode filters.
Common-mode filtering can add significantly to the cost and weight of an inverter.
Effective high-frequency differential-mode filtering can be difficult to implement without
impacting the inverter performance, and imbalances in differential-mode filters can
actually increase common-mode currents. This paper introduces the concept of a
balancing network to reduce the common-mode currents on power inverter cables above
30 MHz. Balancing networks are relatively inexpensive to implement and can be more
effective than common-mode chokes or ferrites. An experimental test set-up is used to

demonstrate the effect of a balancing network on the common-mode current, differential-mode current and the common-mode rejection ratio on a balanced cable with an imbalanced termination. The results show that a balancing network reduces the common-mode noise currents significantly more than the differential-mode signal currents. This balancing network is also evaluated using a 3-phase brushless DC motor driver to verify its effectiveness in a real application.

I.   INTRODUCTION

Power inverters convert electrical power at one voltage or frequency to power at another voltage or frequency. Most inverters employ pulse-width modulation schemes that rely on frequently switching signals with ultra-fast rise and fall times. These signals have significant energy at frequencies well above the fundamental switching frequency. Imbalances in the switching circuitry, transmission path, and load convert some of the power in the differential drive currents into common-mode noise currents (Fig. 3.1). These common-mode currents can interfere with other electronic devices, especially devices that rely on wireless communications.

A typical method of dealing with this form of electromagnetic interference is to apply common-mode filtering. However, this can add significantly to the cost and weight of a motor driver or power inverter and contributes nothing to the system's overall functionality or efficiency. A better approach is to actively enforce the electrical balance of the driver circuitry, while simultaneously compensating for imbalances in the transmission lines and load. Electrical balance is a measure of the relative impedance of

the conductors in a circuit or transmission line to a zero-potential reference (ground) [1-4]. Changes in electrical balance convert differential-mode signals to common-mode noise. By ensuring that all of the signal or power-carrying conductors in a source-transmission-line-load configuration have the same impedance to ground, differential-to-common-mode conversion can be essentially eliminated.
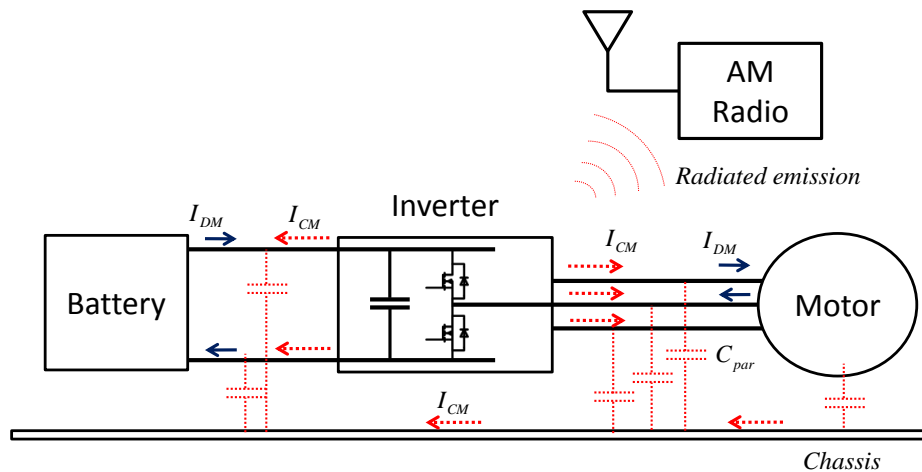
Fig. 3.1. Illustration of a typical power electronics system.

Active balancing (i.e. actively compensating for naturally occurring changes in balance) at the operating frequency of power inverters has the potential to drastically reduce electrical noise and to actually improve the overall efficiency of the power transfer. However, actively compensating for changes in balance at frequencies as high as 30 MHz is generally not achievable. At high frequencies, passive balancing can be used to prevent the conversion of differential-mode signals to common-mode noise on cables.

This paper introduces the concept of a passive balancing network and demonstrates how passive balancing can be a cost-effective way to reduce common-mode currents on cables. An experimental test set-up is used to demonstrate the effect that a

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balancing network has on the common-mode (CM) current, differential-mode (DM) current and common-mode rejection ratio (CMRR) of a balanced cable with an imbalanced termination. Also, experimental results are compared to simulations based on full-wave modeling. A passive balancing network is then applied to a three-phase brushless direct current (BLDC) motor to verify its effectiveness in a real application.

II. PASSIVE BALANCING NETWORKS

Electrical Balance

Several models have been introduced to describe differential-mode to common-mode conversion. Hockanson [5] introduced current-driven and voltage-driven source models to describe how differential-mode signals on circuit boards induce common-mode currents on attached wires.

An equivalent model for estimating the radiated emissions from a printed circuit board with attached cables driven by a signal voltage on a trace was developed by Shim [6]. This model employed a common-mode voltage source located at the junction between the PCB ground structure and the attached wire. The magnitude of common-mode voltage was proportional to the ratio of the self-capacitance of the trace to that of the return plane of a PCB structure.

Watanabe [1] introduced the concept of a *current division factor* to quantify the electrical imbalance of various transmission line configurations. He showed that imbalance is not responsible for the conversion of differential-mode currents to common-mode currents. This conversion is the result of *changes* in the level of imbalance. Using

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various printed circuit board structures as examples, he showed that it is possible to calculate the common-mode currents by replacing the differential-mode source with equivalent common-mode sources at points where changes in the imbalance occur. This imbalance difference modeling technique can greatly simplify the analysis of radiated emissions due to common-mode currents.

Several factors contribute to imbalance in power inverter systems: geometrical asymmetries, unequal turn-on and turn-off times of the switching components, unbalanced PWM control schemes, unbalanced filtering, switching device parasitics, and imbalances in the load impedance. These sources of imbalance can convert the rapidly switching differential-mode currents to common-mode currents resulting in EMI problems [7].
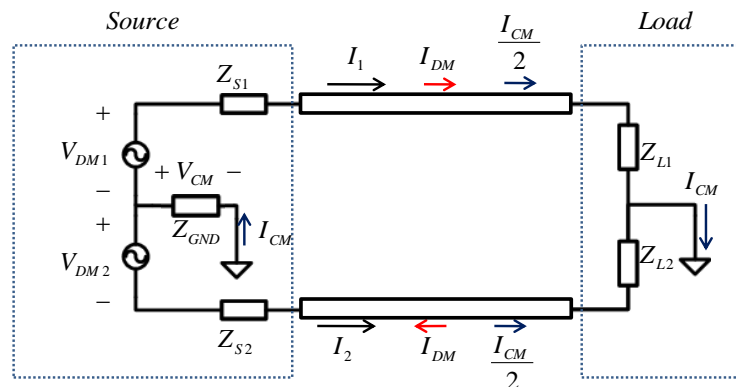

Fig. 3.2. Circuit with DM and CM currents.

Fig. 3.2 shows a circuit with DM and CM currents. This circuit has dual differential-mode voltage sources, a single common-mode source impedance connected to ground, differential source and load impedances, and a transmission path as shown. If the two wires connecting the source to the load have the same impedance to ground, the

currents I_1 and I_2 flowing on the two wires can be decomposed into two modes, I_{DM} and I_{CM}, defined as

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 1/2 & 1 \\ 1/2 & -1 \end{bmatrix} \begin{bmatrix} I_{CM} \\ I_{DM} \end{bmatrix}. \tag{1}$$

The differential-mode current, I_{DM}, and the common-mode current, I_{CM}, on these balanced wires can be determined from I_1 and I_2 as

$$\begin{bmatrix} I_{DM} \\ I_{CM} \end{bmatrix} = \begin{bmatrix} 1/2 & -1/2 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}. \tag{2}$$

Imbalance factor

Watanabe et al. [1, 2] developed techniques for quantitatively defining electrical imbalance and developed a method for calculating common-mode currents using equivalent common-mode voltage sources. Watanabe showed that the common-mode current in a system can be precisely modeled by placing an equivalent common-mode voltage source in the circuit at places where changes in the imbalance occur. The amplitude of these voltage sources is given by

$$\Delta V_C = \Delta h \times V_{DM} \tag{3}$$

where Δh is the change in the current division factor (or *imbalance factor*) and V_{DM} is the differential-mode voltage at that point in the circuit.

Fig. 3.3 illustrates how this approach is applied. Fig. 3.3(a) shows a pair of cable conductors above a ground plane with the source and load impedances indicated. In Fig. 3.3(b), if we assume that $V_{DM1} = -V_{DM2}$, $Z_{S1} = Z_{S2}$, and $Z_{Cable1-gnd} = Z_{Cable2-gnd}$, then

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Part A of the circuit is perfectly balanced ($h_A = 0.5$). Part B of the circuit has an imbalance factor,

$$h_B = \frac{Z_{L2}}{Z_{L1} + Z_{L2}} = \frac{Y_{L1}}{Y_{L1} + Y_{L2}} = \frac{I_{CM1}}{I_{CM1} + I_{CM2}}. \tag{4}$$

The equivalent source that drives the common-mode current is then given by

$$\Delta V_C = |h_B - h_A| \times V_{DM_{Load}} = \left| \frac{Z_{L2}}{Z_{L1} + Z_{L2}} - 0.5 \right| \times V_{DM_{Load}} \tag{5}$$

where $V_{DM_{Load}}$ is differential-mode voltage cross the load. The common-mode currents in the imbalance difference model (Fig. 3.3(b)) are exactly equal to the common-mode currents in the original circuit, Fig 3.3(a). Note that if $Z_{L1} = Z_{L2}$ in (5), the equivalent common-mode voltage and the common-mode currents are zero.
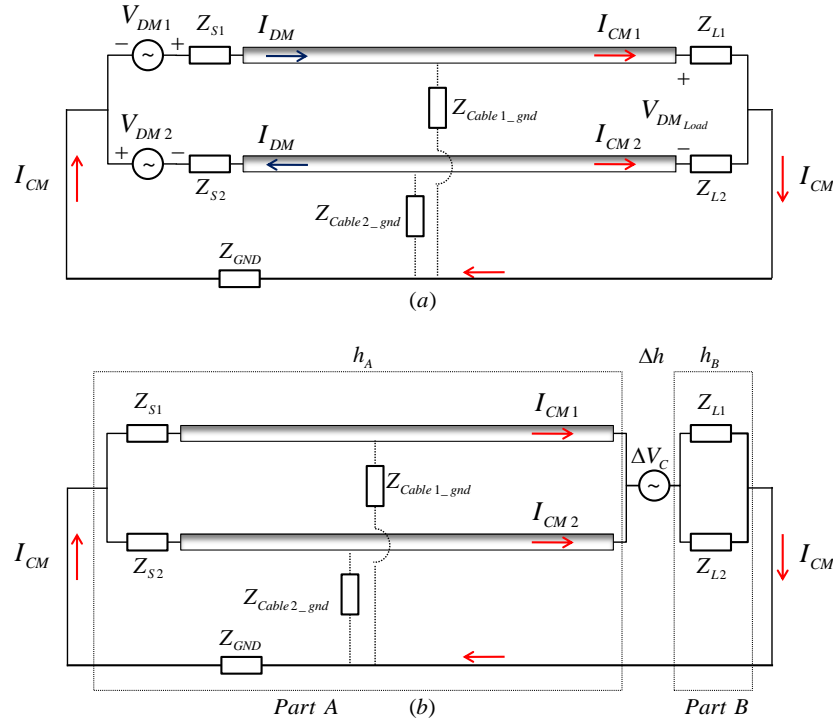
Fig. 3.3. Common-mode currents generated from unbalanced load condition (a) and imbalance difference model (b).

There is no common-mode current if both parts of the circuit are balanced. There is also no common-mode current if both parts are equally unbalanced. In unbalanced circuits, it is necessary to define the relationship between I_1, I_2, I_{CM} and I_{DM} as [1],

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h & 1 \\ 1-h & -1 \end{bmatrix} \begin{bmatrix} I_{CM} \\ I_{DM} \end{bmatrix} \tag{6}$$

$$\begin{bmatrix} I_{DM} \\ I_{CM} \end{bmatrix} = \begin{bmatrix} 1-h & -h \\ 1 & 1 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}. \tag{7}$$

In balanced circuits ($h = 0.5$), (6) and (7) are the same as (1) and (2), respectively. Whether the circuit is balanced or unbalanced, the common-mode current, I_{CM}, is the sum of the currents on both wires.

Balancing Networks

Common-mode current on balanced cables can be reduced by introducing *balancing networks* to compensate for imbalances in the source or load as illustrated in Fig. 3.4. These balancing networks, indicated by the components with a BN subscript in Fig. 3.4, are designed to have an impedance that is lower than the existing source and load impedances at the frequencies where they are effective.

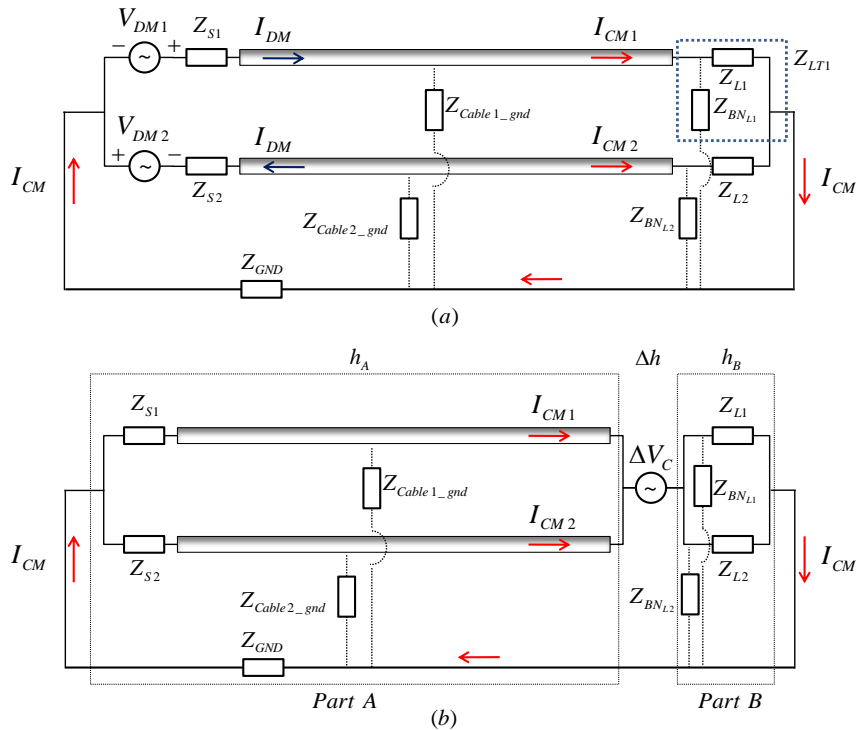
Fig. 3.4. Equivalent circuit of wire model with balancing network (a) and its imbalance difference model (b).

The precise value of the impedance is not critical, but it is important that the impedances on each side of the circuit are the same. The goal of the balancing network is to make the impedance of each phase have the same value as viewed from the cable looking into the source and load.

If our goal is to balance the circuit at high frequencies without affecting the operation of the circuit at low frequencies, a good choice for a balancing network is a resistor, R_B, in series with a capacitor, C_B. This circuit has a high impedance and is relatively invisible at low frequencies. At high frequencies it has an impedance equal to its resistance, which is relatively stable and easy to match to other resistances in the balancing network.

In this paper, Z_{BN} is a series RC (R_B, C_B) circuit connecting each phase wire to system ground. In the circuit in Fig. 3.4(a), the impedance looking into the load from each phase wire (including the RC balancing network), Z_{LT}, is

$$Z_{LT1} = Z_{L1} // Z_{BN_{L1}} = 1 / \left(\frac{1}{Z_{L1}} + \frac{1}{Z_{BN_{L1}}} \right) = \frac{Z_{L1} \times Z_{BN_{L1}}}{Z_{L1} + Z_{BN_{L1}}} = \frac{Z_{L1} \times (j\omega R_{B1} C_{B1} + 1)}{j\omega R_{B1} C_{B1} + 1 + j\omega Z_{L1} C_{B1}}, \qquad (8\text{-}1)$$

$$Z_{LT2} = Z_{L2} // Z_{BN_{L2}} = 1 / \left(\frac{1}{Z_{L2}} + \frac{1}{Z_{BN_{L2}}} \right) = \frac{Z_{L2} \times Z_{BN_{L2}}}{Z_{L2} + Z_{BN_{L2}}} = \frac{Z_{L2} \times (j\omega R_{B2} C_{B2} + 1)}{j\omega R_{B2} C_{B2} + 1 + j\omega Z_{L2} C_{B2}}. \qquad (8\text{-}2)$$

Fig. 3.5 shows how the RC balancing network causes the load impedance to ground of each phase wire to approach the same value at high frequencies without affecting the low-frequency differential load impedance. For this calculation, the load impedances without the balancing network are, $Z_{L1} = 178$ Ω and $Z_{L2} = 90$ Ω. The RC balancing network component values are $R_B = 51$ Ω and $C_B = 1$ nF. As shown in Fig. 3.5, near balance is achieved at frequencies above approximately 20 MHz. Although the balance is not perfect ($h_{with\_BN} = \frac{51 \| 90}{(51 \| 90) + (51 \| 178)} = 0.45$), it is significantly improved relative to its value at low frequencies ($h_{without\_BN} = \frac{90}{90 + 178} = 0.33$). The equivalent

common-mode voltage is proportional to the change in the balance factor, so the reduction in common-mode voltage with this balancing network at high frequencies would be,

$$20\log\frac{h_{cable}-h_{without\_BN}}{h_{cable}-h_{with\_BN}}=20\log\frac{0.50-0.33}{0.50-0.45}=10.6\,dB\,.\tag{9}$$

Fig. 3.6 shows the actual common-mode current calculated for the circuit in Figs. 3.3 and 3.4, without and with the balancing network. The balancing network and load impedances used for this calculation were the same as in Fig. 3.4. The source impedances were $Z_{S1} = Z_{S2} = 75\ \Omega$. The source voltages were $V_{DM1} = -V_{DM2} = 0.5$ V. Z_{GND} was zero.
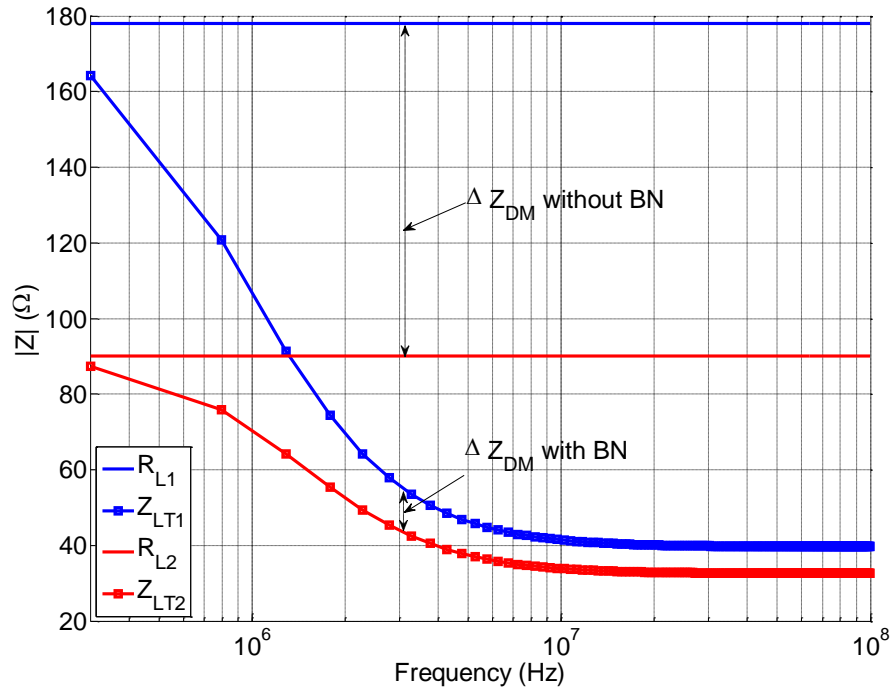

Fig. 3.5. Imbalance at 'without' and 'with' balancing network (BN).
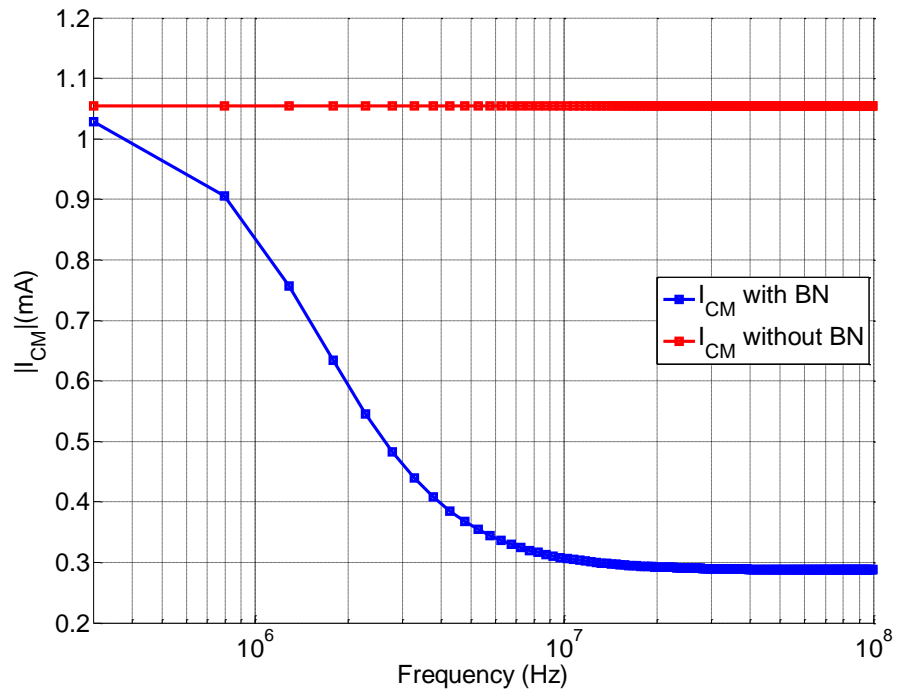
Fig. 3.6. I_{CM} comparison depending on the balancing network at load side.

III. EVALUATION OF A HF BALANCING NETWORK

The test set-up illustrated in Fig. 3.7(b), was used to demonstrate how a balancing network can reduce common-mode currents. The equivalent circuit for this set-up, Fig. 3.7(a), has two voltage sources with opposing polarities, V_{DM1} and V_{DM2}, that drive a pair of wires above a ground plane. The normalized amplitude of V_{DM} is 1.0 V. Each wire is terminated with a resistor to the ground plane. To create an unbalanced condition, the load resistors were given different values, $Z_{L1} = 178.3\,\Omega$ and $Z_{L2} = 91\,\Omega$. The total differential-mode termination impedance is $Z_{L1} + Z_{L2} = 269.3\,\Omega$. The length of the wires between the source and load is 920 mm.

(a)

(b)

Fig. 3.7. Equivalent circuit (a) and test configuration (b) used to demonstrate the balancing effect.

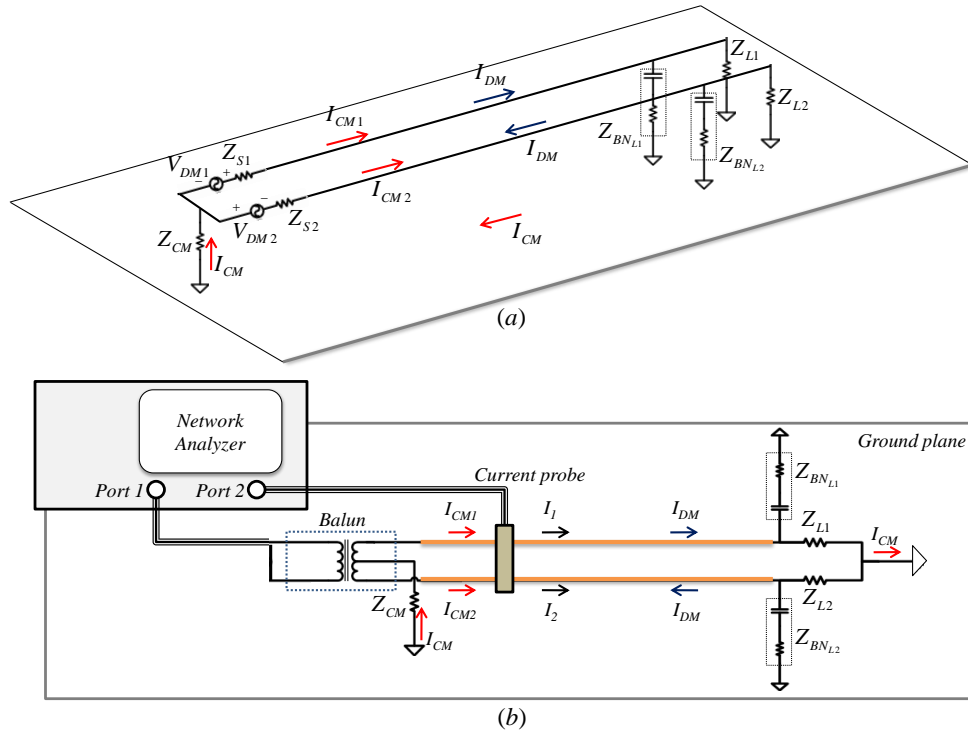The magnitude of the transfer coefficient, $|S_{21}|$, between port 1 and port 2 of the network analyzer was measured to determine the relationship between the common-mode (CM) current and differential mode (DM) current in the circuit. Port 1 of the network analyzer was connected to the single-ended side of a wide-band transformer (balun). Port 2 was connected to a current probe (FCC F-33-1), which was clamped around both wires to measure the common-mode current. To measure the differential-mode current, current probes were placed around each of the wires. While measuring the differential-mode current, I_1 or I_2, both current clamps were in place in order to avoid any unbalancing of the circuit due to current clamp loading. An Agilent E5070B Network Analyzer was used to measure S_{21} from 1 MHz to 100 MHz.

The balancing network is indicated by the series R-C circuits labeled Z_{BNL1} and Z_{BNL2} in Fig. 3.7. The value of each capacitor in the balancing network is 0.001 μF, and each resistor is 51 Ω. This RC combination has little effect on the termination impedance below $f_c = 1/2\pi RC = 3$ MHz. At 30 MHz and higher, its nominal impedance is approximately 51 Ω.

<u>Correlation of the $|S_{21}|$ measurement with current amplitude</u>

For the configuration in Fig. 3.7, the value of $|S_{21}|$ is a measure of the ratio of the common-mode current, I_{CM}, to the differential-mode voltage at the output of the balun,

$$20\log_{10}|S_{c1}| = 20\log_{10}\left|\frac{I_{CM} \times 50}{V_{DM}}\right| + Calibration\_Factor(dB) \qquad (10)$$

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where *Calibration_Factor(dB)* is a constant determined by the transfer coefficients of the balun, current probes, and other fixed pieces of the test set-up. If we assume that the differential-mode current is much greater than the common-mode current, and the current probe on Port 2 is clamped around just one wire, $|S_{21}|$ is a measure of the ratio of the differential-mode current, I_{DM}, to the differential-mode voltage at the balun,

$$20\log_{10}|S_{d1}| = 20\log_{10}\left|\frac{I_{DM} \times 50}{V_{DM}}\right| + Calibration\_Factor(dB). \tag{11}$$

A common-mode rejection ratio (CMRR) can be defined as the ratio of the differential-mode current to the common-mode current. Higher values indicate better rejection of the common mode. The CMRR for the configuration in Fig. 3.7 is given by the difference (in dB) between measurements of $|S_{21}|$ with the current clamp around one wire and both wires,

$$CMRR\ (dB) = 20\log_{10}\left|\frac{I_{DM}}{I_{CM}}\right| = 20\log_{10}|S_{d1}| - 20\log_{10}|S_{c1}| \tag{12}$$

<u>Characteristic impedance of coupled transmission line</u>

In Fig. 3.8, the height from ground to the center of the each wire, *height*, is 35 mm, the distance between the two wires, *d*, is 25 mm, and the radius of the wire, *r*, is 2.5 mm. The width of the plane in this test set-up, *w*, is 230 mm.

d = 25 mm

r = 2.5 mm
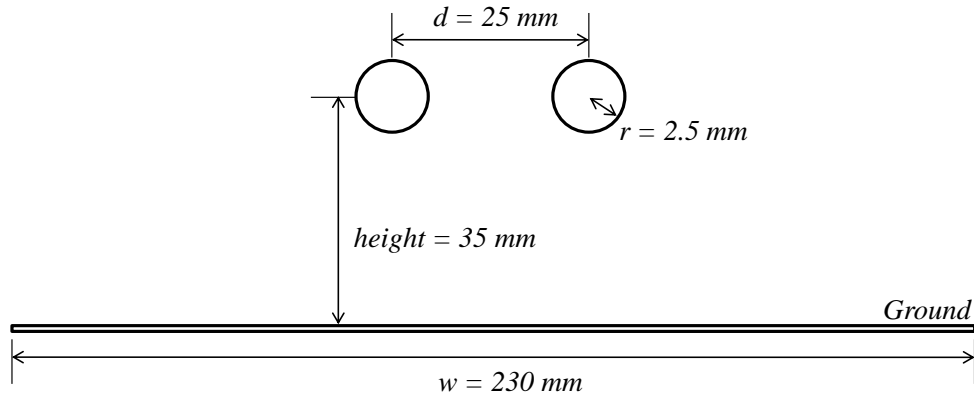
height = 35 mm

Ground

w = 230 mm

Fig. 3.8. Cross-sectional geometry of test configuration.

Using a two-dimensional static electric-field simulation tool [39], it was determined that Z_{11} (equal to Z_{22}) and Z_{12} (equal to Z_{21}) were 201.9 Ω and 67.4 Ω, respectively, and the differential-mode characteristic impedance Z_{DM} was 269.3 Ω. In this configuration, the load impedances ($Z_{L1} = 178.3$ Ω, $Z_{L2} = 91$ Ω) without the balancing network provide a matched termination for the differential-mode signals.

Balun characteristics

In order to correlate model results with measurement results, the CM and DM impedances of the balun had to be determined. As illustrated Fig. 3.9, a 50-Ω load was used to terminate the input side of the balun, while measuring the impedance looking into the balun output. The DM impedance was the impedance between the two output pins of the balun as indicated in the upper part of Fig. 3.9. The CM impedance was the impedance measured between the two output pins tied together and the grounded center-

tap of the balun output as indicated in the lower part of the figure. The measured balun

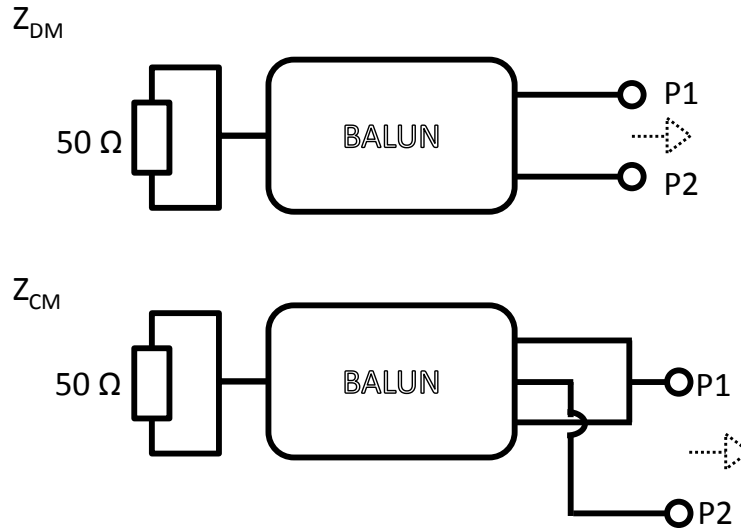impedances are plotted in Fig. 3.10.

Z_{DM}

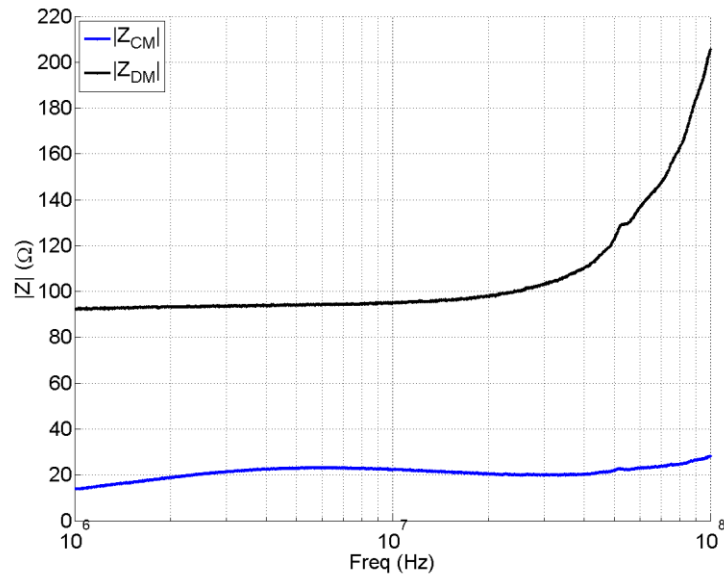Fig. 3.9. Test configuration to measure Z_{CM} and Z_{DM} of the balun output.

Fig. 3.10. Measured values of the balun's CM and DM impedance.

The common-mode impedance of the coupled transmission line in Fig. 3.8 is 67 Ω, while the CM impedance of the balun is approximately 20 Ω. Thus, a 46.5-Ω resistor was added between the center tap of balun and the ground plane to help match the common mode. The impedances, Z_{S1} and Z_{S2} in Fig. 3.7 each represent half of the balun's DM output impedance, which is a function of frequency as indicated in Fig. 3.10. The measured balun impedances used for modeling this test configuration are listed in Table 3.1.

Table 3.1. Measured values of Z_{CM} and Z_{DM} for the balun

Frequency	Z_{CM}	Z_{DM}	$Z_{CM}+46.5\Omega$	$Z_{DM}/2$ (= Z_{s1} = Z_{s2})
1 MHz	13.8	92.3	60.3	46.2
2 MHz	18.9	93.2	65.4	46.6
3 MHz	21.3	93.6	67.8	46.9
4 MHz	22.3	93.6	68.8	46.9
5 MHz	23.0	94.3	69.5	47.2
6 MHz	23.0	94.1	69.5	47.0
7 MHz	23.0	94.5	69.5	47.0
8 MHz	22.9	94.5	69.4	47.1
9 MHz	22.7	95.2	69.1	47.6
10 MHz	22.4	94.9	68.8	47.5
20 MHz	20.6	97.9	67.0	48.9
30 MHz	19.9	103.2	66.4	51.6
40 MHz	20.3	110.4	66.7	55.2
50 MHz	22.2	123.1	68.7	61.6
60 MHz	23.0	136.6	69.5	68.3
70 MHz	23.6	147.2	70.1	73.6
80 MHz	24.7	162.4	71.3	81.2
90 MHz	26.5	183.8	72.9	91.9
100 MHz	28.1	205.5	74.6	102.7

Full-wave modeling

A full-wave analysis (using FEKO [40]) was applied to the configuration in Fig. 3.7. The essential elements of the model are illustrated schematically in Fig. 3.11 with and without the balancing network in place. In these models, the 92-cm wire length was divided into 100 segments. V_{DM1} and V_{DM2} were set to 1 V. Z_{S1}, Z_{S2} and Z_{CM} were given the frequency-dependent values indicated in Table I. Z_{L1} was 178.3 Ω and Z_{L2} was 91 Ω. The currents I_1 and I_2 were monitored at the 1st segment to find I_{CMS} and I_{DMS} at the source side, and at the 100th segment to determine I_{CML} and I_{DML} at the load side.
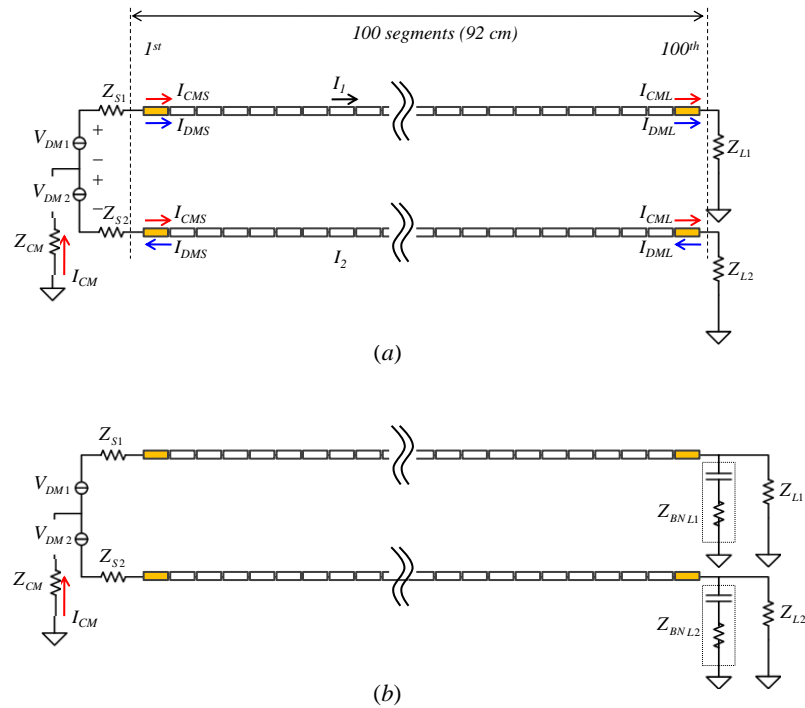

Fig. 3.11. Wire segmentation and termination for modeling without BN (a) and with BN (b).
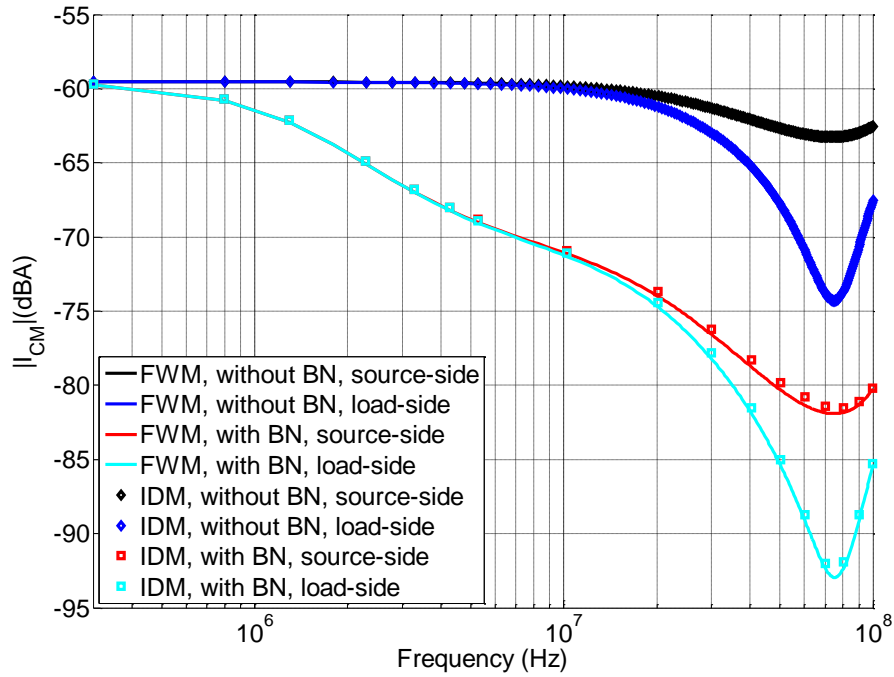
Fig. 3.12. I_{CM} comparison with BN and without BN.

Comparison with imbalance difference model (IMD)

Fig. 3.12 shows the magnitude of the common-mode current in the Fig. 3.7 test set-up as calculated using the full-wave model and the imbalance difference model with the imbalance parameters in Equation (9). Both analyses are well correlated between 300 kHz and 100 MHz. Because there was no need to model the balun for this comparison, the 46.5-Ω resistor for common-mode impedance matching at the source side was left out of the circuit and the differential-mode impedance value of the source side was fixed to 150 Ω instead of the frequency-dependent value in Table 3.1.

The balancing network should not have a significant effect on the differential-mode current below the 3-MHz cutoff frequency. Fig. 3.13 shows the measured $|S_{d1}|$ (proportional to I_{DM}) with and without the balancing network in place. At 10 MHz, the balancing network increases the current at the load end of the circuit by 6 dB. At approximately 80 MHz, where the wires are a quarter-wavelength long, the effect on the current is greater. This is because the balancing network creates a mismatch between the differential-mode characteristic impedance of the transmission line and the differential-mode termination impedance.

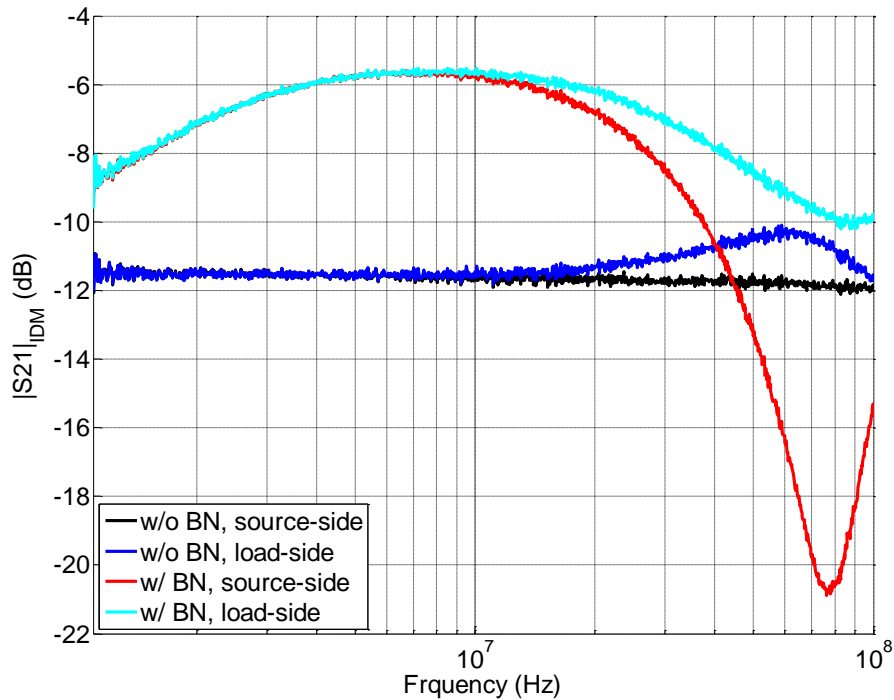Fig. 3.13. I_{DM} response depending on the different monitoring locations.

Fig. 3.14 shows the measured $|S_{c1}|$ (proportional to I_{CM}) with and without the balancing network. The balancing network attenuates the common-mode current by about 7.5 dB at 3 MHz, and the attenuation is 15 dB or more between 30 and 100 MHz.
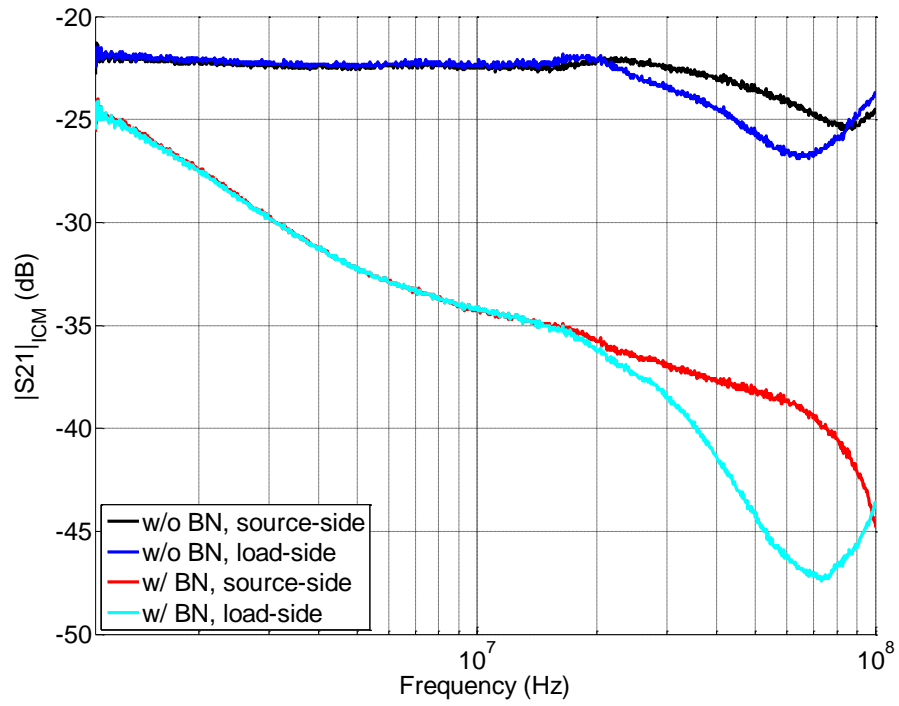
Fig. 3.14. I_{CM} response depending on the different monitoring locations.
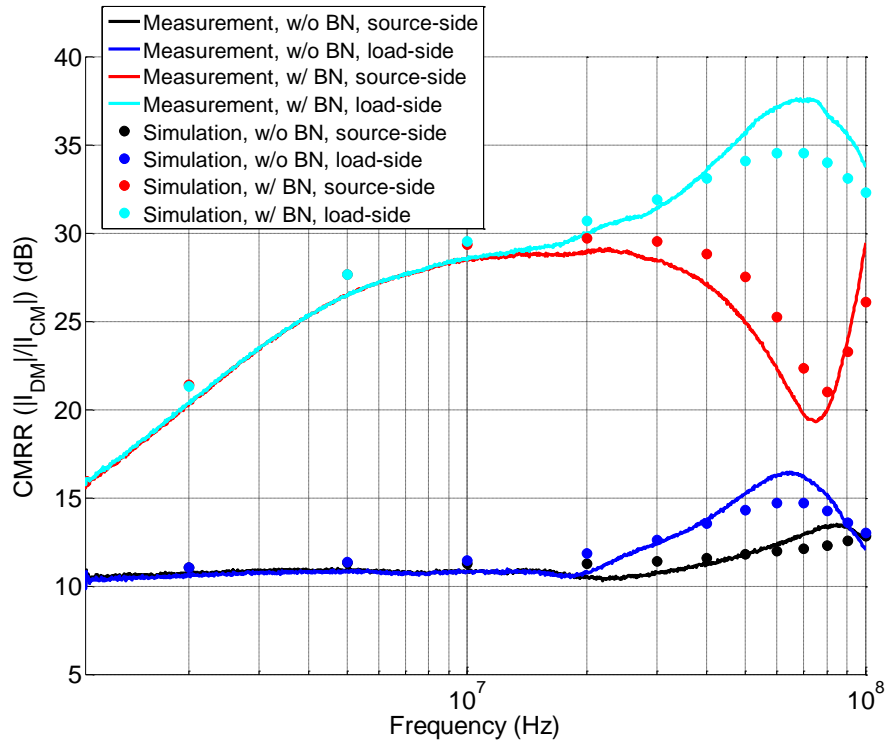
Fig. 3.15. Measured and simulated CMRR ($|I_{DM}/I_{CM}|$ in dB).

Fig. 3.15 shows the CMRR with and without the balancing network. Both measured results and full-wave simulation results are shown. With the balancing network in place, the CMRR is more than 30 dB higher between 30 and 70 MHz on the load side. On the source side, where the differential-mode currents experience a null around 80 MHz, the CMRR is still improved by at least 6 dB with the balancing network in place.

Note that in this measurement, the balancing network increases the mismatch between the characteristic impedance of the transmission line and the differential-mode termination impedance. These values were chosen to make the point that the reduction in common-mode current had nothing to do with better matching. In practical applications,

the resistances of the balancing network could be chosen to improve the matching of the differential-mode signal, rather than make it worse.

IV. A POWER INVERTER APPLICATION

The fast switching that is an inherent part of efficient motor drives and power inverters produces a high amount of electrical noise. Imbalances in the switching circuitry, transmission path, and load convert differential drive noise into common-mode currents that can be significant sources of broadband radiated emissions typically peaking around 30 - 70 MHz. These emissions can interfere with other electronic devices, especially devices that rely on wireless communications. The 3-phase inverter and brushless direct-current (BLDC) motor illustrated in Fig. 3.16 exhibited unacceptable levels of radiated emissions at frequencies between 30 and 70 MHz. These emissions were due to the common-mode current flowing on the cable connecting the inverter to the motor.
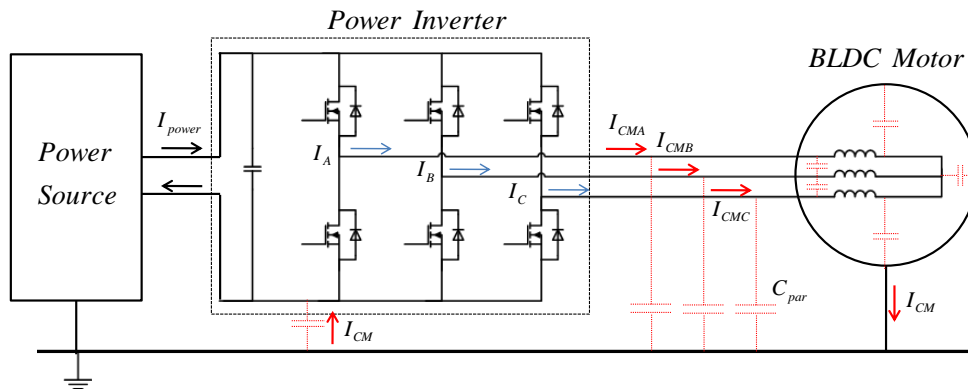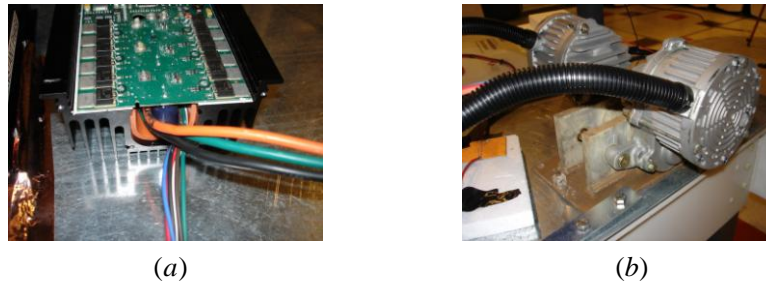
Fig. 3.16. Three-phase BLDC Motor system; (a) power inverter (b) BLDC motor.

The objective of the balancing network is to provide a constant, balanced impedance to the transmission lines between the inverter and the BLDC motor at frequencies between 30 and 70 MHz. A 1-nF capacitor in series with a 51-ohm resistor was connected between each phase wire and a local ground plane at each end of the cable as shown in Fig. 3.17. This provided a constant impedance of approximately 50 ohms from each wire to the ground plane of the balancing network. 50 ohms was chosen as a value that was low relative to the inverter output impedance and motor input impedance at 30 MHz, but high enough to overwhelm the impedance associated with the inductance of the connection between the components and the ground plane. While it is important

that all three terminations have the same impedance to ground, the exact value of this impedance is not critical.

The cable length between power inverter and BLDC motor was about 1.5 m and the test configuration was set up on a metal table top that connected to the chassis ground of the inverter and the wires lied on a 7-mm thick insulating pad.

The common-mode current was measured using a current probe connected to a spectrum analyzer. In these tests, the BLDC motor was loaded by driving another motor through a shaft.
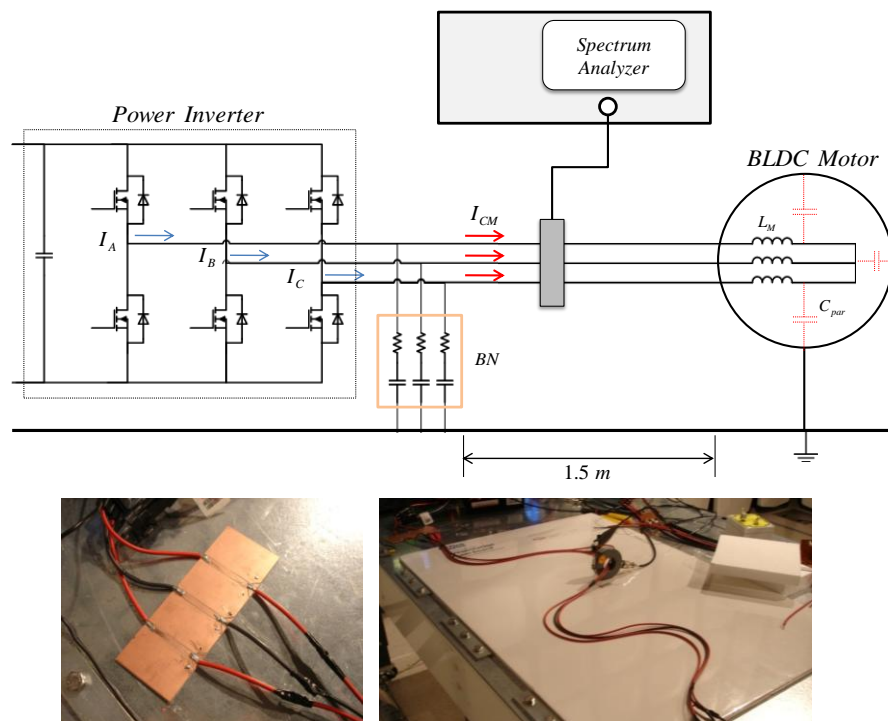

Fig. 3.17. Test configuration for evaluating the balancing network.

A three-phase motor/driver system like this would be perfectly balanced if the impedance of all three phase wires to ground was the same, and if the average of the voltages between each wire and ground were constant. In a balanced system, there would

be no conversion of differential-mode currents to common-mode currents. The six-step PWM driving scheme employed by this inverter system is inherently unbalanced. At various stages of the drive cycle one or two of the phase wires may be floating, tied high or tied low. Fig. 3.18 shows the measured phase voltage (to chassis ground), gate voltage on the high side MOSFET, and line current for one of the three wires in this system.

(a) Phase V_{A-to-GND}

(b) Gate V_A of high-side MOSFET

(c) Line current of phase A
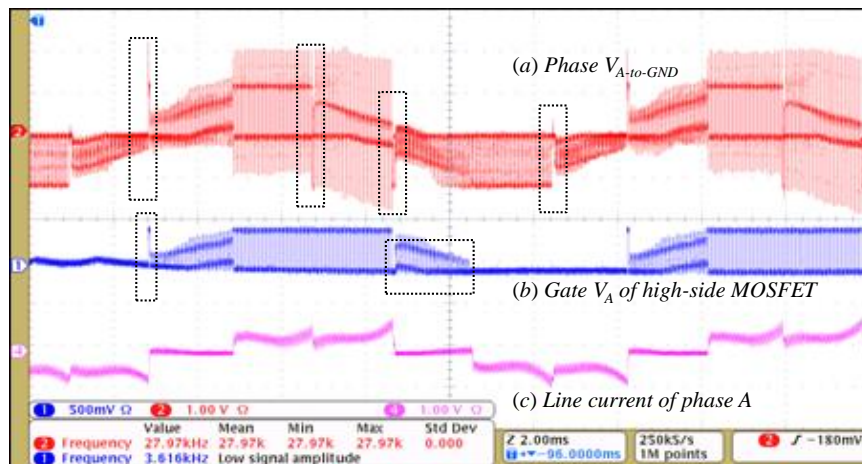
Fig. 3.18. Phase voltage and line current from one of three-phase cables.

Fig. 3.19 plots the common-mode current on the three wires without the balancing network. The upper plot is in the time domain and the lower plot shows the frequency components from 30 to 100 MHz as a function of time. Spikes in the common-mode current correlate with the spikes in the differential-mode current that occur during the switching of the MOSFETs. The original design suppressed these currents using ferrite cores clamped around the cable.
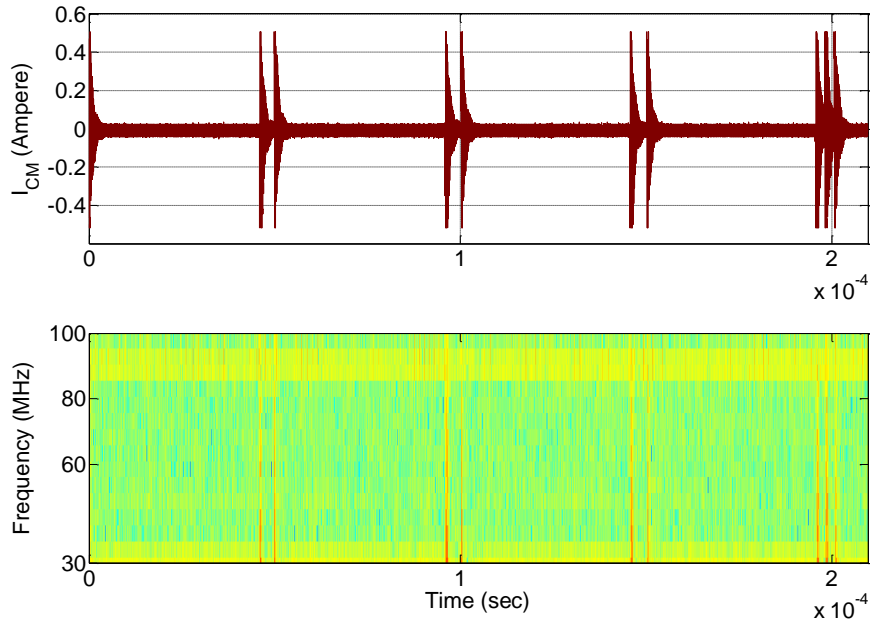
Fig. 3.19. Measured I_{CM} waveforms and short-term FFT.

The maximum common-mode current was observed when the inverter was driving the motor at maximum speed. The maxhold function of the spectrum analyzer was used to capture the maximum level of common-mode current on the 3-wire cable. The current supplied to the inverter was adjusted to 2.0 amperes. As shown in Fig. 3.20, when the balancing network was applied to the phase wires at the output side of the power inverter, the common-mode noise on the cable between 30 and 80 MHz was significantly reduced.
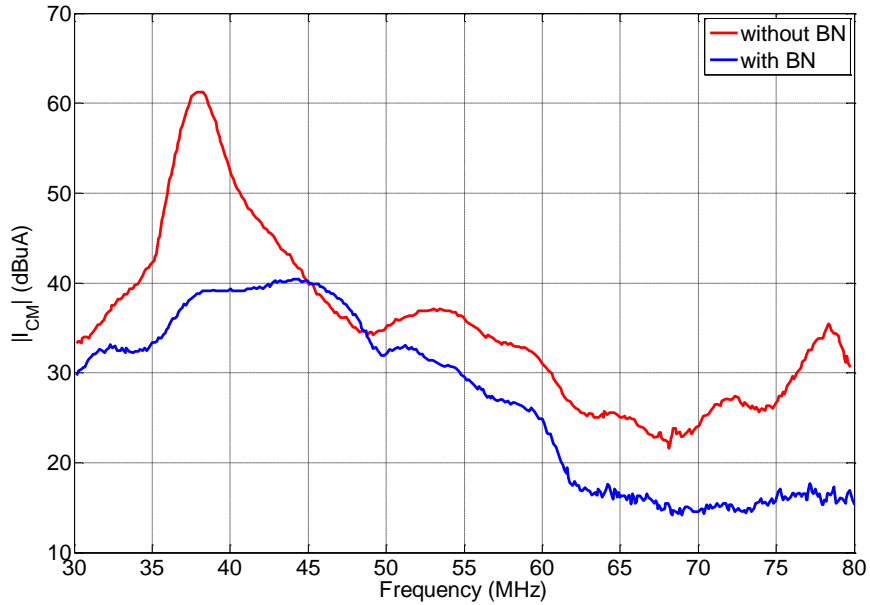
Fig. 3.20. I_{CM} at maximum speed.

V. CONCLUSION

Differential-mode voltages can be converted to common-mode currents by changes in circuit balance resulting in EMI problems. Passive balancing networks can cost-effectively prevent DM-to-CM conversion at high frequencies without impacting the low-frequency operation of the circuit. Unlike DM filtering, passive balancing has a greater effect on CM currents than it does on DM currents. Unlike most CM filtering, passive balancing networks can be highly effective without requiring relatively bulky and expensive inductors or ferrites. However, it should be noted that passive balancing networks only attenuate common-mode currents that result from changes in imbalance.

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They do not attenuate common-mode currents resulting directly from common-mode sources.

One particularly attractive application of passive balancing is the suppression of common-mode currents in power inverters. Power inverters rely on very fast switching at kHz frequencies. Since most power inverter driving schemes are inherently unbalanced, the differential-mode signals produced by these inverters can be converted to common-mode currents in balanced cables and loads. Filtering power inverter outputs can be expensive and/or affect the efficiency of the inverter. Balancing networks can significantly reduce the common-mode currents from power inverters without similarly attenuating the differential-mode drive currents.

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