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THERMO-MECHANICAL EFFECTS OF THERMAL CYCLED COPPER THROUGH-SILICON VIAS

A Thesis
Presented to
the Graduate School of
Clemson University

In Partial Fulfillment
of the Requirements for the Degree
Master of Science
Materials Science and Engineering

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by
James Marro
August 2013

Accepted by:
Dr. Kathleen Richardson, Committee Co-Chair
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Dr. Marian Kennedy
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ABSTRACT

The semiconductor industry is currently facing transistor scaling issues due to fabrication thresholds and quantum effects. In this “More-Than-Moore” era, the industry is developing new ways to increase device performance, such as stacking chips for three-dimensional integrated circuits (3D-IC). The 3D-IC’s superior performance over their 2D counterparts can be attributed to the use of vertical interconnects, or through silicon vias (TSV). These interconnects are much shorter, reducing signal delay. However TSVs are susceptible to various thermo-mechanical reliability concerns. Heating during fabrication and use, in conjunction with coefficient of thermal expansion mismatch between the copper TSVs and silicon substrate, create harmful stresses in the system. The purpose of this work is to evaluate the signal integrity of Cu-TSVs and determine the major contributing factors of the signal degradation upon in-use conditions. Two series of samples containing blind Cu-TSVs embedded in a Si substrate were studied, each having different types and amounts of voids from manufacturing. The samples were thermally cycled up to 2000 times using three maximum temperatures to simulate three unique in-use conditions. S_{11} parameter measurements were then conducted to determine the signal integrity of the TSVs. To investigate the internal response from cycling, a protocol was developed for cross-sectioning the copper TSVs. Voids were measured using scanning electron microscope and focused ion beam imaging of the cross-sections, while the

microstructural evolution of the copper was monitored with electron backscattering diffraction. An increase in void area was found to occur after cycling. This is thought to be the major contributing factor in the signal degradation of the TSVs, since no microstructural changes were observed in the copper.

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LIST OF ACRONYMS

2D: Two-Dimensional

3D: Three-Dimensional

AC: Alternating Current

AFM: Atomic Force Microscopy

Al: Aluminum

AR: As-Received

BEOL: Back End Of The Line

BSE: Backscattered Electrons

CD: Critical Dimension

CMP: Chemical Mechanical Polishing

CTE: Coefficient of Thermal Expansion

Cu: Copper

CVD: Chemical Vapor Deposition

DRIE: Deep Reactive Ion Etching

EBSD: Electron Backscattering Diffraction

ECD: Electro-Chemical Deposition

FCC: Face Centered Cubic

FEA: Finite Element Analysis

FEM: Finite Element Modeling

FEOL: Front End Of The Line

FIB: Focused Ion Beam

GaAs: Gallium Arsenide

Ge: Germanium

IC: Integrated Circuit

IPF: Inverse Pole Figure

ISE: Ion Induced Secondary Electrons

LMIS: Liquid Metal Ion Source

NV: Non-Voided Samples

Poly-Si: Polycrystalline Si

PVD: Physical Vapor Deposition

RF: Radio Frequency

SE: Secondary Electrons

SEM: Scanning Electron Microscope

Si: Silicon

SiO_x: Silicon Oxide

SiP: System-in-Package

SoC: System-on-Chip

Ta: Tantalum

TEOS: Tetraethyl Orthosilicate

Ti: Titanium

TSV: Through Silicon Via

V: Voided Samples

VNA: Vector Network Analyzer

W: Tungsten

WLI: White Light Interferometer

WLP: Wafer Level Packaging

CHAPTER ONE

MOTIVATION AND OBJECTIVES

1.1 Motivation

Traditional integrated circuits (IC) have been available since the mid 1900's, replacing the vacuum tube with the invention of integrated based solid state, fabricated on thin semiconductor substrates (i.e., wafers) [1]. The segmented devices (i.e., chips) have provided the basis for which electronics are built, and has propelled higher performance and other needs to meet the demand of the end-user.

Traditionally, higher performance generally means cramming more devices into a unit area of semiconductor substrate; this is accomplished by geometrically shrinking the device features such as reduction of the feature size of fabricated transistors. This shrinkage, also described as feature scaling, lead to an increased density of devices on a single chip. The scaling trend has motivated an empirical relationship between performance and chip complexity is known as Moore's Law, which states that the amount of transistors on a chip increases two fold about every two years as seen in Figure 1.1 [2]. Over the past 40 years, scientists and engineers have relentlessly followed this law. This has led to current devices with critical dimensions (CD) of 22 nm, as illustrated by the production of Intel's smallest platform (Ivy Bridge) transistors [3]. However, the

size of transistors is quickly approaching the size of an atom, a few angstroms, and this presents numerous challenges. First, the tools and the lithography-based fabrication technology needed for the continued geometric scaling down of transistor feature size is not scaling with Moore's law. Furthermore, continued scaling of the transistor will also lead to a change in device physics, as quantum mechanics sets in. As transistors shrink, so must interconnects. Unlike transistors, decreasing cross-sectional area of an interconnect decreases its performance. The resistance of a wire can be calculated using equation 1,

$$R = \rho \frac{L}{WH} \qquad (1)$$

where R is the resistance, ρ is the resistivity, and the length, width, and height of the interconnect are denoted by L,W, and H respectively; hence, the resistance is inversely proportional to the interconnect's cross-section (WH) [1]. The smaller distances between interconnects and other devices on the chips as well as longer interconnect lengths, increase the parasitic capacitance [4] and cross-talk between adjacent devices. Thus, as scaling down continues, interconnects become the performance-limiting component as opposed to transistors. This situation is known as "the interconnect bottleneck" within the semiconductor industry.

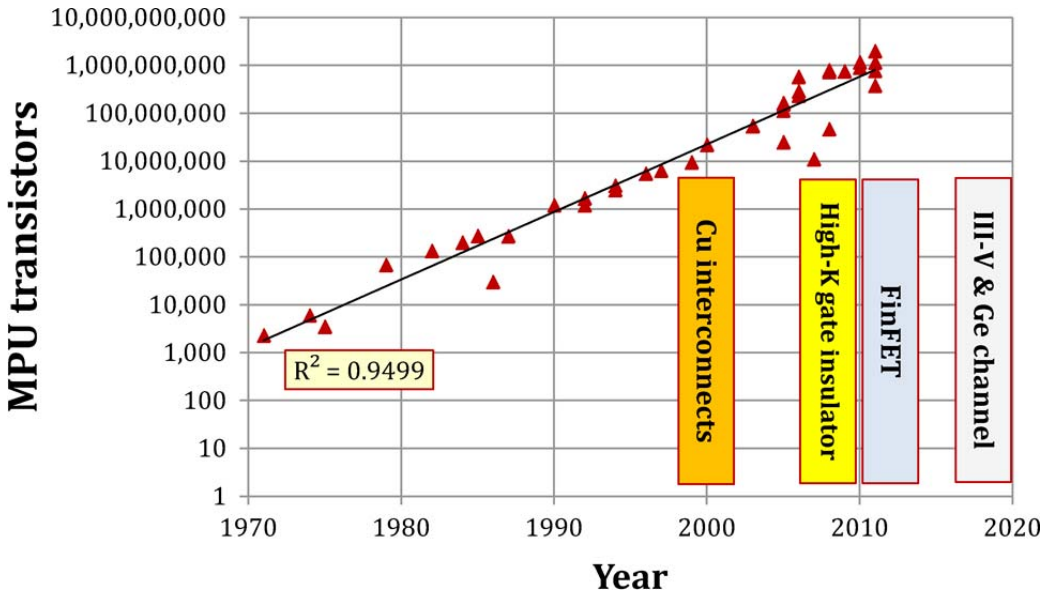

Figure 1.1: Graph showing the accuracy of Moore's law up to 2011, taken from reference [6].

Three-dimensional (3D) devices are emerging as a potential solution to this bottleneck. Interestingly, the 3D stacking of ICs enables the co-integration of devices that perform different functions into a single system. This co-integration of devices has ushered in the so-called 'More-than-Moore' era [5]. The More-than-Moore approach focuses on system integration as opposed to transistor down-scaling (Moore's law). The stacking of chips allows for more transistors on a device, benefiting from increased performance, form factor, and integration. 3D interconnects are necessary for communication across multiple chips. While there are many different interconnect technologies for achieving 3D-stacked dies, the use of through-silicon vias (TSV) has emerged as the most efficient and preferred technique. These interconnects are achieved by vertically drilling

through the active silicon chip and subsequently filling it with a conductive material, such as copper to realize electrical connectivity, between stacked layers.

While TSVs are just one part of the 3D electronic system, their effectiveness in providing 'connectivity' will ultimately limit the device's overall performance. The temperature of chips in electronic devices fluctuates during fabrication, and during use. Thus, thermo-mechanical reliability concerns have risen due to mismatch between the thermal characteristics of the materials used in the TSV. Typically, the electrically conducting pathways in the interconnect expand differently than the surrounding semiconductor material resulting in stress build-up during use. Thus, a detailed understanding of the inter-material interactions and potential failure mechanisms are needed to understand the reliability limits of such devices. Such multi- and inter-material interactions are of utmost importance to design, fabrication and implementation of TSVs in future semiconductor device systems.

1.2 Objectives

TSVs provide an interconnect basis for the 3D stacking of chips, which make up 3D integrated circuits (3D-IC). This study strives to investigate the thermo-mechanical reliability of through-silicon vias (TSV) when subjected to thermal cycling. This investigation aims to define possible causes of

degradation/failure through pre- and post-cycling evaluation of TSV morphology and microstructure to draw a correlation between radio-frequency (RF) signal integrity and the material changes seen in the via structure. The thermal cycling in the present effort serves to simulate the typical lifetime conditions or long-term use of the device.

This study was carried out on non-stacked wafers, containing blind Cu-TSVs. Two wafer types were studied, where the processing conditions were slightly different. Due to this variation in initial via processing methods, different amounts and types of pre-existing voids have been observed in each wafer type. Thus, this variation has allowed a side-by-side basis by which initial defect formation and in-service evolution with thermal cycling conditions can be observed. As discussed in detail in subsequent chapters, samples containing TSVs underwent thermal cycling from room temperature to an established varied maximum temperature and the TSVs were studied to examine the following factors to realize the thesis' target goals:

1. Evaluate the RF reflection coefficient (S_{11}) parameter to determine the signal integrity of commercially-prepared Cu-TSVs from simulated use conditions.
2. Develop a method for examining the microstructure and defects within the Cu-TSVs.

3. Identify the pre-existing defects in the TSVs of the two commercially manufactured wafers and how these defects form and evolve with thermal cycling.
4. Quantify the difference in Cu microstructure of the two wafer type TSVs as well as how this microstructure evolves due to thermal cycling.
5. Correlate the performance variation of the Cu-TSVs to the internal aspects of the TSVs, such as defect and microstructure changes.

Thermo-mechanical effects on TSVs, typically found in 3D ICs, were studied in conjunction with thermal cycling. Thermal cycling simulates what transpires in electronic chips during their lifetime. As an electronic device is used, it experiences temperature fluctuations due to energy dissipation. When electrical current flows through the interconnect to devices on a chip, it meets resistance from the material, which converts the current into heat from Joule heating. In general, not all of the electrons' energy is used to carry information in the interconnects. Instead, the energy is dissipated as different energy forms, such as light or heat. When the device is put to sleep or is not in use, it cools down, because the circuits are not pushing current. Over time these temperature fluctuations may cause the chips to fail. 3D ICs sport a higher level of density than traditional 2D ICs and thus are exposed to heat for longer intervals of time. Hence, thermo-mechanical reliability becomes an essential factor in these

systems. Limited research has been conducted on thermally cycled Cu-TSVs, however, the cycling conditions used typically simulate the heating profiles utilized during the processing of these chips, with slow ramp rates and higher maximum temperatures, rather than in-use conditions [7, 8].

Thermal cycling is expected to induce more defects from the stress created by the mismatch in the coefficient of thermal expansion (CTE) between the Cu of the TSVs and the Si wafer. The voids may congregate, forming larger voids and resulting in larger amounts of signal loss, since voids act as scattering centers. Although some microstructural changes are expected in the Cu, such as grain coarsening, from the elevated temperature of thermal cycling, these changes may be minimal due to the fast cycling times. Furthermore, preferential grain orientation has not been found in Cu-TSVs [8, 9, 10, 11]. The lack of texture, or random granular orientation, impedes performance of these interconnects and creates local stresses within the copper from inter-granular anisotropy, causing void formation and, subsequently, signal loss.

1.3 Thesis Scope

The organization of this thesis is as follows. Chapter two gives an introduction by including the state-of-the-art research in this field. Chapter three describes the experimental procedure employed to complete this investigation. Chapters four and five highlight the results and discussion, respectively, of the

electrical loss, defect, and microstructure measurements. Lastly, the conclusions and future work are enclosed in Chapter six.

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CHAPTER TWO

INTRODUCTION

This chapter provides an introduction to the research presented in this thesis. The current state of art for 3D-IC devices and up-to-date studies of TSVs and their reliability issues, are discussed. Furthermore, the instruments used to characterize these reliability concerns and questions this work will answer, are included.

2.1 3D Stacking of Chips

The effort to maintain Moore's law has led to the development of other 3D technologies, each showcasing the progress of the semiconductor industry toward 3D ICs. Each are discussed here with contrast shown as to technology attributes. These include 3D system-in-packages, 3D wafer-level-packaging, and 3D integrated circuits.

2.1.1 3D System-in-Packages

3D System-in-Package (SiP) designs consist of several devices stacked in one package. SiPs usually utilize a silicon interposer to connect multiple chips. These connections are generally made using wirebonds. Wirebonds are long interconnects as shown in Figure 2.1. The use of wirebonds is the limiting factor in SiPs due to their length and amount of space taken up. There is still a large

increase in density for these systems compared to systems-on-chips (SoC), however the wirebonding still occupies a large area compared to other 3D systems. Furthermore, this technology is currently the most well developed amongst 3D stacked chips [1].

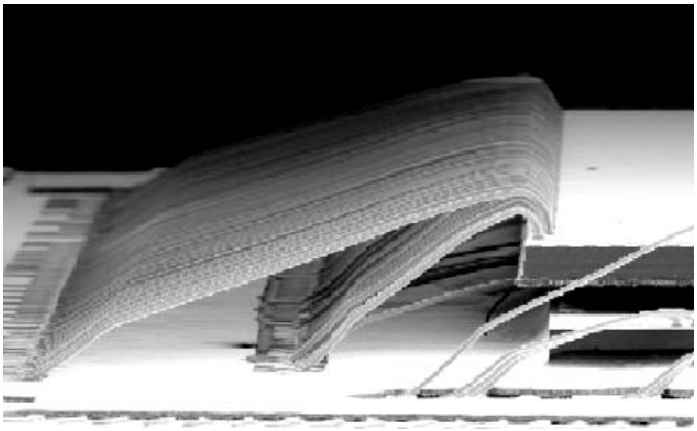

Figure 2.1: A SiP which utilizes wire bonding, taken from reference [2].

2.1.2 3D Wafer-Level-Packaging

3D Wafer-Level-Packaging (WLP) is a more dense package than the SiP, because of their interconnecting methods. Some WLPs contain through-silicon vias (TSV), or vertical interconnects that are perpendicular to the surfaces of the chip. TSVs need less space to operate and provide a shorter pathway for current, increasing the performance of the chips. At the end of these TSVs are bondpads that are used for flip chip bumping. Flip chip bumping is the application of solder bumps on the bottom of a chip to allow them to communicate when stacked. Bumps and microbumps, like TSVs, make the WLP

more densely packed then SiPs [1]. Figure 2.2 shows a cross section of a WLP with TSVs and microbumps. While SiPs are constructed after dicing, the stacking of chips in WLPs precedes the dicing of the wafers [3].

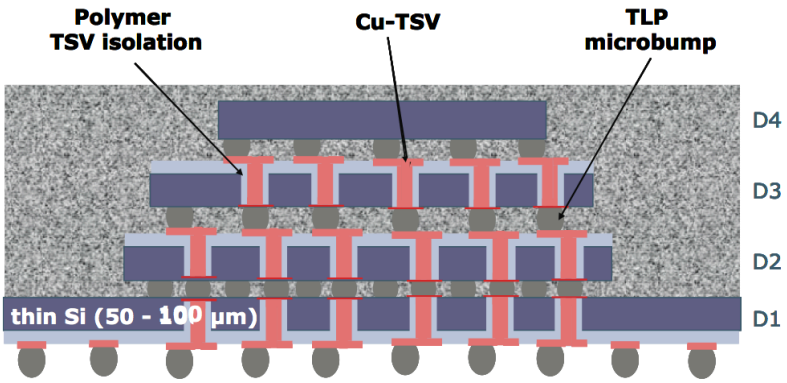

Figure 2.2: Illustration of an Imec WLP, which uses microbumps, taken from reference [4].

2.1.3 3D Integrated Circuits

3D Integrated Circuits (IC) presents superior density to SiP and WLP stacked chip technologies. In these systems, the use of wirebonds has been abandoned and replaced fully with TSVs. While all the advantages of 3D ICs will be presented in the next section, the use of TSVs brings the chips closer together and makes the stacked chips more highly integrated. Design is crucial for these ICs because everything must be integrated together. 3D ICs allow one chip to do the function of many, all the while, reducing the form for the system. It also shortens the interconnect path length and minimizes power losses via Joule heating. An example of a 3D IC is found in Figure 2.3.

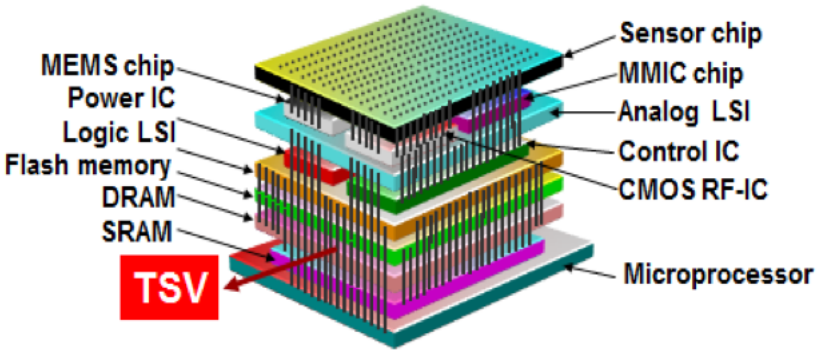

Figure 2.3: Breakdown of a 3D IC, taken from reference [5].

2.2 Benefits of 3D IC

The semiconductor industry is always striving to reduce chip volume. 3D stacking of chips allows for increases in density of the system and thus a smaller form factor. Such designs take full advantage of the silicon wafer, having a silicon efficiency, defined as the ratio of the available area on the silicon over the total area of the substrate, of over 100% compared to 2D systems [6]. Thinning of the wafers allows these systems to further achieve a greater density. These compact chips easily fit into mobile devices, such as cell phones and tablets, without reducing the number of components on the chips. Also, since interconnects can be utilized in another dimension, more transistors and other devices can be added to the chips because less surface area is occupied.

Performance is shown to increase in these 3D ICs compared to their 2D counterparts [6-11]. This is due to the reduced length of interconnects. With single chip systems, the interconnects are only limited to two dimensions and

thus the signal must travel further to reach its destination. 3D ICs have much shorter vertical interconnects, reducing the time it takes for the signal to be transmitted. Davis *et.al*. have suggested that about a 65% delay drop could be seen in 3D ICs over their 2D equivalencies [7], while Al-Sarawi *et. al.* suggests a 30% decrease in delay due to lower parasitic capacitance [6]. This also leads to a decrease in signal scattering, which in turn means up to 30% less power is required to drive the system [6]. Furthermore, interconnect density is increased and thus the signal throughput is much greater.

Heterogeneous integration allows for a variety of chips to be stacked, as illustrated by Figure 2.3. Incompatibility is no longer an issue as different wafers and materials can be stacked to form 3D ICs. The most advanced chips and devices can all be packaged into one seamless system, using this 3D technology [11].

2.3 Challenges of 3D Integrated Circuits (ICs)

Complexity is a major issue for chip designers and architects [6]. Vertical integration of chips means that professionals need to rethink the layouts of these chips for optimal performance. This adds more opportunity for flaws in the design and structures. Since most components rely on each other, given the increase in integration, one component failure could lead to a decrease in overall

chip performance or entire chip breakdown. Reparability is limited when everything is that tightly integrated.

The increased density of these chips makes heat dissipation a major concern [11]. Temperature excursions can affect the system greatly and has the potential to change many material properties, as the involved multi-materials create thermal expansion mismatches. This results in added stress to the system which as will be discussed in subsequent chapters, can cause many different types of failure, from delamination of the substrate to via cracking.

Since 3D ICs are a relatively new technology, many unknowns are still being tested. The manufacturability and optimization of the design and materials of these 3D structures are in question. Stacking these chips will require precise wafer thinning and accurate alignment methods. It is expected that perfecting the structure, reliability, and manufacturability of these circuits will take many more years.

2.4 TSV Structure

While the shape of TSVs has been studied extensively, this thesis will only focus on tapered cylindrically shaped TSVs. The semiconductor industry is always looking to minimize the surface area of these structures. Electrical properties have been shown to degrade with increasing TSV height to diameter aspect ratios [12]. Larger aspect ratios show increased probability of void and

other defect formation during fabrication. However, larger aspect ratios are becoming reality due to advanced filling techniques, which will be discussed later in this chapter. It is speculated that by the year 2015 the maximum aspect ratio will double from the current 10:1 to 20:1 and the minimum global TSV diameters will be cut in half from 4 μm to 2 μm, while height remains unchanged. Due to the size changes, the maximum pitch is also predicted to reach 4 μm from its present 8 μm by 2015 [13]. Smaller pitch means more densely packed arrays of TSVs that occupy less chip area.

TSVs are made up of several layers, each serving its own purpose. Figure 2.4 shows an optical micrograph of the structure for a blind TSV such as that examined in the present study. A typical TSV is conceptually similar in structure to an electrical transmission line; it contains three different layers, the isolation liner, barrier layer, and a conduction layer. The outermost layer, the isolation liner, is in contact with the silicon substrate and prevents cross talk between adjacent vias as well as loss of current through sneak paths into the substrate. Sandwiched between the isolation liner and conduction layer is the barrier layer. There are two critical requirements of such a barrier layer: (1) it must be a good adhesive to the isolation layer and the innermost conductive layer, and (2) the barrier layer must prevent diffusion between the conduction and Si substrate. The adhesive attributes of the barrier layer aids in the filling process, allowing the TSV to be filled while maintaining its shape. The

conduction layer is the inner most layer of TSVs. It consists of a conductive material, which provides a path for electric current to flow. Diffusion from the conduction layer into the isolation layer must be prevented, as such contamination will adversely affect the performance of front-end-of-line (FEOL) devices located in the Si matrix. As can be seen in the micrograph in Figure 2.4 taken from reference [14], the metallic conductive fill material of the via, is not perfect in its cross-sectional uniformity as it contains defects and other non-uniformities, directly related to the processing methodology used in its fabrication. These attributes and their possible influence on RF signal integrity and changes in microstructure that can be induced with thermal cycling, are discussed in subsequent sections.

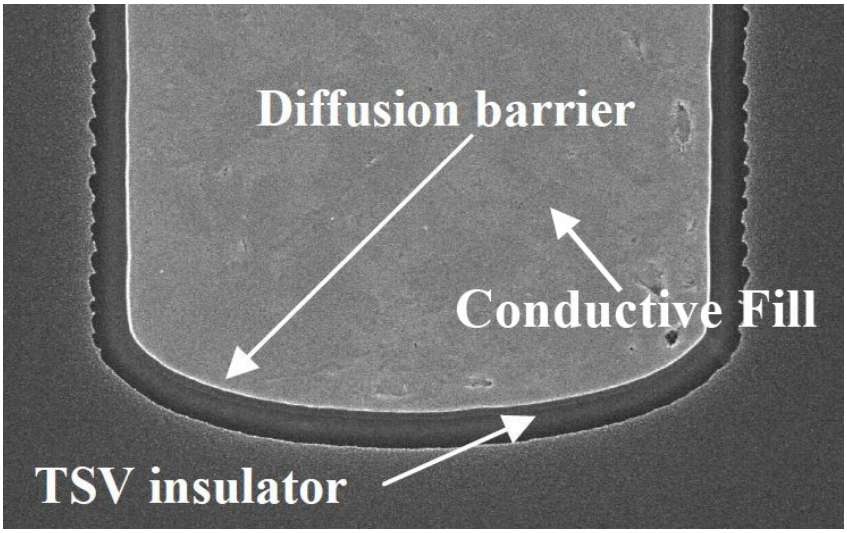

Figure 2.4: Illustration of the three layers of typical TSV, insulator, diffusion barrier, and conductive layer, taken from reference [14].

2.5 Integrated Circuit (IC) Materials

2.5.1 Wafer Materials

High purity semiconductors wafer substrates are the backbone of IC structures. Semiconductors are utilized because their properties are readily manipulated and controlled through doping. Silicon (Si) is the most common material for this application; although Germanium (Ge) and gallium arsenide (GaAs) are relatively expensive alternatives. Another qualification for semiconductor substrates is homogeneity. Maintaining property consistency throughout the entire wafer is crucial for the prevention of failure and to minimize variability across the wafer. It is for this reason that chips are made from monocrystalline (single crystal) substrates instead of polycrystalline materials, which introduce defects in the form of grain boundaries.

2.5.2 TSV Filling Materials

Silicon oxide (SiO_x) derived from tetraethyl orthosilicate (TEOS) precursors is primarily used as the isolation liner for the TSV. The amorphous nature and poor electrical conductivity of this material impedes propagation of current. The silicon oxide's lack of free electrons makes this material a good insulator. Ta-based barrier layers are commonly used with Cu interconnects. Ta compounds used are generally inert to Cu as well as Si. Thus, it resists diffusion between itself and the Cu as well as the isolation liner [15].

The conductive layer of the TSV is perhaps the most important material. Its characteristics control the current flow. Many materials have been exploited because of their good conductive properties, including aluminum (Al), tungsten (W), and polycrystalline silicon (Poly-Si), but nothing matches copper's (Cu) low resistivity and cost. Due to its lower resistivity and superior electro-migration resistance, Cu replaced Al as the conventional material of choice for interconnects [16].

2.6 TSV Processing

The TSV processing scheme is characterized by the chronology in which the TSVs are integrated into chip fabrication. There are three categories for TSV processing. Via-first, is the fabrication of the TSVs at the beginning of the chip production cycle, before the integration of front-end-of-line (FEOL) devices, such as transistors. Via-last processing includes the creation of vias toward the end of the chip production steps, after the back-end-of-line (BEOL), or planar interconnects, have been deposited. In via middle production, TSVs are constructed between the integration of FEOL devices and the BEOL interconnects. Currently, via middle processing is the industry standard. While via middle processing forces the TSVs to undergo heat treatments from the BEOL addition, via first requires more extensive heating from the FEOL and via

last fabrication creates design problems from the many layers of devices and materials already added to the wafers.

Integrating the fabrication of TSVs in the process flow of 3D ICs requires many steps. The visual representation of via middle manufacturing scheme, shown in Figure 2.5, gives a hint of the complexity associated with TSV fabrication. First, FEOL devices such as transistors, capacitors, and other devices are implanted on the chip. Afterwards, a deep reactive ion etching (DRIE) process, which utilizes ion bombardment, is used to create high aspect ratio via trenches in the silicon substrate. Next, the TEOS isolation liner is deposited using chemical vapor deposition (CVD). A physical vapor deposition (PVD) process, is then employed for deposition of the barrier layer and copper seed layer. The Cu seed layer enables the impending electrochemically deposited (ECD) copper to have optimal microstructure. A chemical mechanical planarization process rids the surface of excess material from the deposition processes and leaves the surface flat for the BEOL. The BEOL, consisting of layers of planar interconnects and dielectric insulators, are the last features positioned onto the wafer, before the chip is flipped, thinned, and aligned to be stacked. Integrating the BEOL and stacking the chips usually require thermal processes, 350 °C for BEOL [17] and up to 400 °C for chip bonding [18].

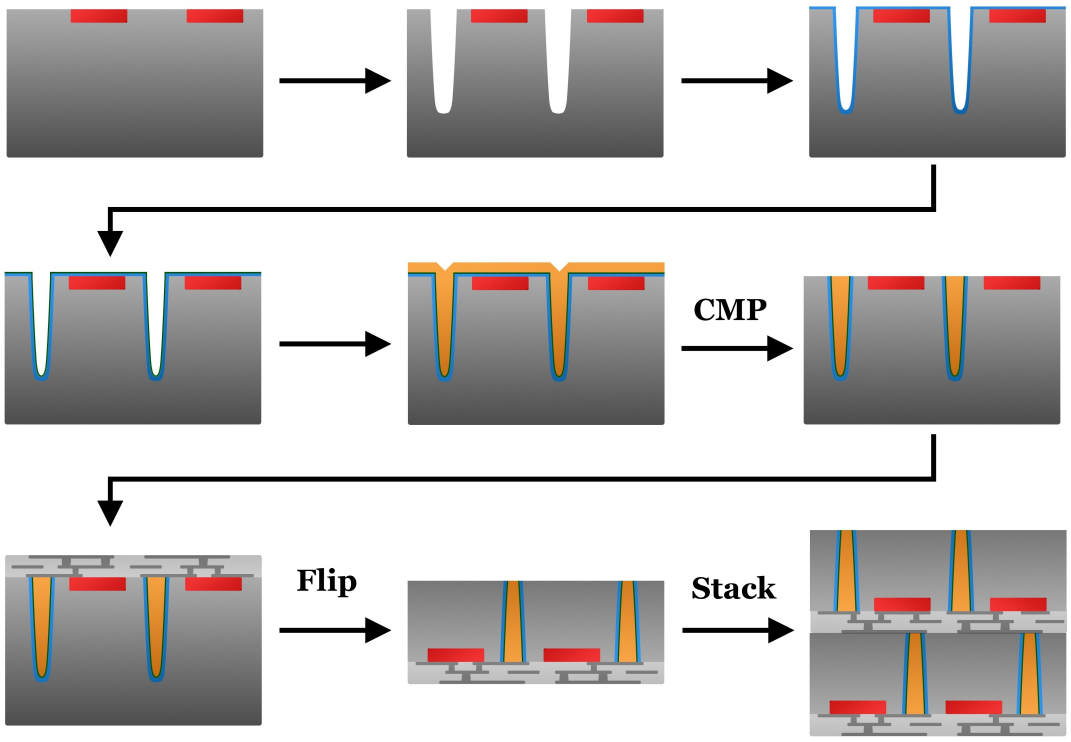

Figure 2.5: Process flow of via middle filling. a.) FEOL is placed on chip; b.)DRIE cuts via holes in the Si chip; c.) CVD of isolation layer; d.) PVD of barrier layer; e.) deposition of Cu seed layer and fill using PVD and ECD respectively; f.) CMP of surface; g.) addition of BEOL; h.) flipping of the chip in preparation for final steps; i.) alignment and stacking of multiple chips.

2.7 Thermo-Mechanical Reliability of TSVs

2.7.1 Thermo-Mechanical Stresses

The Cu-TSVs and Si matrix have very different material properties as made evident by Table 2.1. Due to the mismatch in coefficient of thermal expansion (CTE), 16.7 ppm/°C for Cu and 2.3 ppm/°C for Si, the Cu expands much faster than the surrounding Si substrate when heated. This creates stresses in the system. Chip processing, joule heating, and environmental conditions constitute

for heat changes in 3D ICs. These temperature fluctuations generate thermo-mechanical reliability concerns. Non-destructive methods, such as Raman spectroscopy and finite element analysis (FEA), have been utilized to measure and estimate stresses in the Si surrounding the TSVs. At room temperature the Si regions nearest to copper TSVs were found to be under compression, however, when moving further from the TSVs, there are tensile stresses in the Si, before they dissipate far from the TSVs [19-24]. This stress profile is seen in Figure 2.6. These thermo-mechanical stresses also cause TSV reliability concerns, such as out of plane expansions, defect formation and growth, and microstructural changes, all of which are discussed in this section.

Table 2.1: Material properties of Si and Cu, data taken from reference [25].

Material	Young's Modulus [GPa]	Poisson Ratio	Coefficient of Thermal Expansion (CTE) [ppm/°C]
Silicon	169	0.26	2.3
SiO_2	75	0.17	0.5
Copper	117	0.3	16.7

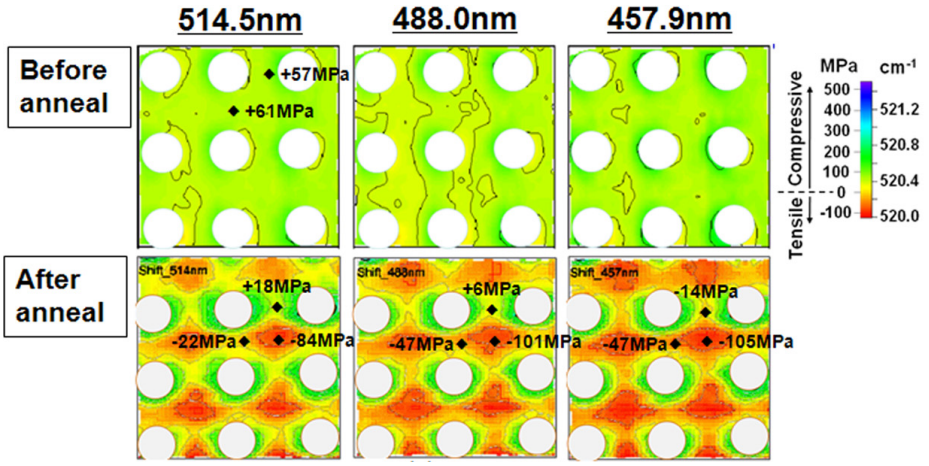

Figure 2.6: Stress map of Silicon substrate, measured by micro-raman, taken from reference [23].

2.7.2 Out of Plane Expansion

Out of plane expansion of TSVs are observed as these thermo-mechanical stresses build up. The Cu is constrained by the surrounding Si substrate so the only expansion direction for the Cu is axially, out of the trench. There are two possible mechanisms proposed for this protrusion. The temperature increase could be pushing the Cu past its elastic limit and causing plastic deformation to occur [26]. Kumar *et.al*. suggested that another possible mechanism for copper protrusions is diffusional sliding, where the copper atoms want to minimize stresses and move out of the compressive stress field found in the copper [27]. The amount of expansion has been found to increase linearly with heat treatment temperature [26]. Furthermore, increasing the amount of thermal cycling, slows down the rate of expansion [27]. Deformation and delamination of the BEOL can result from this copper TSV expansion. This is

illustrated in Figure 2.7. However, this problem can be alleviated by heating immediately following deposition and chemical mechanical polishing (CMP) to flatten the surface. It has been found that by heat treating these Cu-TSVs, less expansion will occur upon reheating during processing or use [26,28,29].

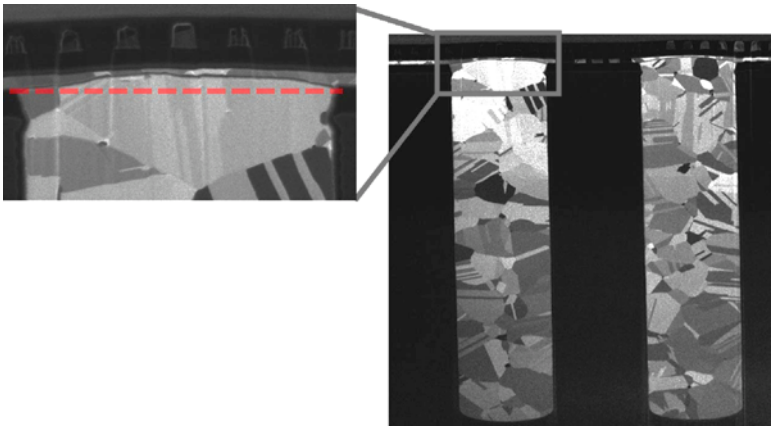

Figure 2.7: Cross-section of a TSV, which has undergone out-of-plane expansion, leading to deformation of the BEOL. A dashed line has been added for planar reference, taken from reference [29].

2.7.3 TSV Defects

2.7.3.1 Voids

Voids are a defect in Cu-TSVs, which can be detrimental to electrical stability and overall reliability. They are characterized as local regions in a TSV, which are not occupied by the Cu. Their shapes and sizes vary greatly. Seams, as illustrated in Figure 2.8a, accommodate vertical areas along the center of TSVs. On the other hand, micro-voids are generally small spherical voids that are dispersed throughout the TSV, such as those in Figure 2.8c. Electrical

properties, such as resistance and capacitance, are sensitive to voids. Voids can serve as a scattering center for electrical current, causing high losses in the TSVs and even failure if the voids become too big.

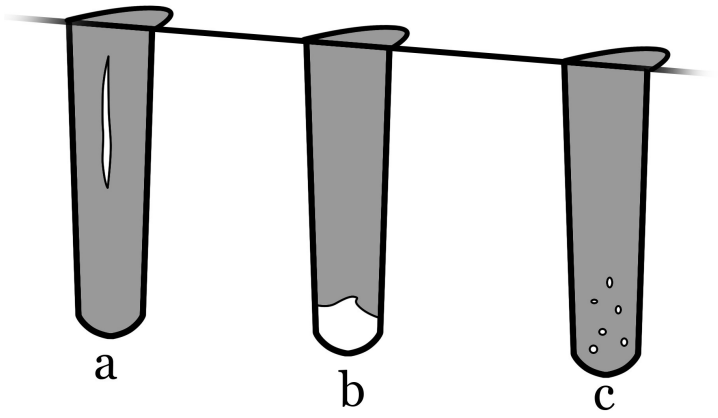

Figure 2.8: Different void types found from flawed processing. A.) seam void; b.) void at bottom of a incompletely filled TSV; c.) microvoids.

Voids originate in one of two fashions, most commonly through processing or stress. Pre-existing voids in TSVs are formed due to inadequate processing procedures. Filling techniques are a major cause of voids in high aspect ratio TSVs. When TSV trenches are filled with conductive material from the sidewalls, air easily becomes encapsulated. At the end of deposition, the result is usually a seam of air trapped in the center of the TSV. Since high aspect ratio TSVs are tall and narrow, they are more prone to these defects. The sequence in Figure 2.9 demonstrates this phenomenon. Deposition chemistries and electro-chemical deposition (ECD) parameters have also been found to greatly affect void formation upon filling [30-34]. Probably the most notable development in

filling processes is bottom-up ECD. Instead of filling from the sidewalls, the conductive material is deposited onto the bottom surface of the TSV and filled upwards, greatly reducing the probability of trapping air. Significant reduction in void formation is found when utilizing this filling method [35-37].

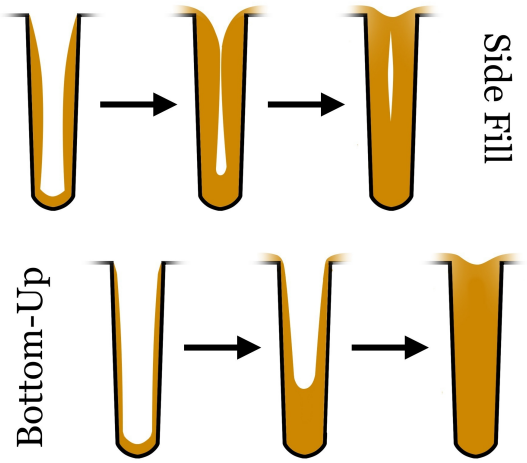

Figure 2.9: The process flow for filling TSVs, revealing how bottom up filling creates void-free TSVs while sidewall filling can produce seams.

Unlike pre-existing, process-induced voids, stress-induced voids nucleate as TSVs are introduced to stress. As mentioned previously, most stresses in TSVs are caused by CTE mismatch between the copper interconnects and silicon matrix when heating occurs. This, along with differences in grain orientation, give rise to stress gradients from the highly anisotropic copper grain growth. As a result, voids form along grain boundaries to relieve stresses [30,38]. Coble creep, or diffusion along grain boundaries, has been identified as the mechanism for void formation [30].

Similar to void formation, void growth also occurs in high purity copper due

to grain boundary diffusion. Vacancy diffusion along the grain boundaries can cause microvoids, which are formed in adjacent locations, to coalesce during heating. Furthermore, void growth has been shown to occur almost exclusively along high angle grain boundaries [39]. X-ray imaging was used by Kong et al. to confirm that increasing holding temperatures from 225 °C to 300 °C, increased the sizes of voids in Cu-TSVs [40].

2.7.3.2 Barrier Layer and Isolation Liner Defects

Interfaces result from the multiple layered TSVs, including the conduction/barrier layer interface, barrier layer/isolation liner interface, and the isolation liner/substrate interface. These interfaces are vulnerable areas in the structure that are suseptible to defects and create reliability concerns. Improper etching of the TSV trenches can form scallops, or uneven sidewalls, like those shown in Figure 2.10. Once the barrier layer and isolation liner are deposited, they are prone to defects like cracking and thinning. Defects in the isolation liner give the current a pathway out of the TSV, causing leakage. Smooth isolation liners have proven to be much more thermally stable. Nakamura *et al.* concluded that increasing heat treatment temperature for scalloped TSVs increases the amount of current leakage drastically, compared to TSVs with even sidewalls [41].

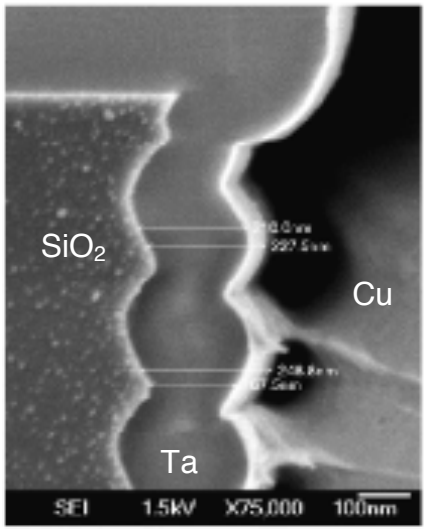

Figure 2.10: Scalloped Ta barrier layer, taken from reference [20].

Like the isolation liner, the barrier layer must also be thermally stable. Material choice and deposition thickness are important as this layer prevents diffusion of the copper into the substrate. Studies have found tantalum, (Ta) to be more thermally stable than titanium (Ti) barrier layers. Therefore, smaller Ta thicknesses are needed to fulfill its duty compared to Ti [42]. In addition, the barrier layer can dictate grain sizes of the electrodeposited copper layer. Ta barrier layers were also found to be superior compared to Ti based layers in that Ta promotes seed layers of strong orientations. Strong grain oriented Cu seed layers translate to smoother seed layers and larger grain sizes [43]. The microstructure of the copper has a large impact on TSV reliability, as will be discussed in further detail in the next section as well as throughout the rest of this proposal.

2.7.4 Microstructure

Microstructure can affect the electrical properties of a metal. Since grain boundaries are defects that resist the flow of electrons, electrical properties are inherently affected by grain size. As grain size increases, the amount of grain boundaries generally decreases. Since electrons don't have to flow through as many of these defect areas, this results in less signal scattering and loss, decreasing the electrical resistance.

Heat treatment of copper TSVs have revealed much about the microstructural evolution of these structures. The middle and bottom of blind TSVs tend to have larger grains than the top region [38,44,45]. These results are postulated to be related to an excess of additives from copper plating at the top of the TSVs [44]. Upon heat treatment, average grain sizes have been found to increase with holding temperatures above 300 °C. Little growth is seen at lower temperatures [26,38,45]. As in all systems, enough energy needs to be provided to cause the movement of grain boundaries, leading to grain growth.

To our knowledge, microstructural effects from long term thermal cycling have not been studied extensively for these structures. Okoro *et al.* cycled Cu-TSVs from room temperature to 420 °C to replicate chip processing conditions [30]. Thermal cycling was found to increase Cu grain sizes in the TSVs. Furthermore, the electroplating chemistry may have affected the type of grain growth (abnormal and normal) that occurred [30]. Although these microstructural

changes were observed in the TSVs, a small number of cycles were performed and slow heating/cooling rates were used. No studies were found in the literature that observes the microstructural evolution of Cu-TSVs over many thermal cycles. Additionally, heat treatments have been shown to have little to no effect on the Cu grain orientation. Preferential grain orientation has not been found in Cu-TSVs due to thermal cycling or isothermal heat treatments [26, 30, 44, 45].

Although there are not many studies conducted on long term cycling of TSVs, Joule heating has been applied to small structures, such as Cu thin films, to examine thermal fatigue. Alternating current (AC) is passed through thin metal films inducing Joule heating, which results in cycling due to the fluctuations in current applied. This is different from the blanket thermal cycling performed in most TSV studies, where the entire sample is heated instead of local heating. If the power is held constant, the frequency of the current dictates the maximum temperature of cycling, where lower temperature ranges were applied at higher frequencies [46]. Increasing thermal cycling causes more defects to build up until failure occurs and current can no longer pass through the film. Also, increasing the temperature range of cycling also increased the likelihood of failure at an earlier number of cycles [46]. As mentioned in earlier sections, the mismatch in CTE between the Si substrate and the Cu films results in stresses that are detrimental to the material's reliability. Wang *et.al.* found that the thickness of the films widely impacts the mechanisms for defect formation in the Cu films [47].

Below 0.1 μm thick films, cracks initiate and propagate along grain and twin boundaries, however, between 0.1 μm and 1 μm film thicknesses, cracks form proceeding extrusions within the grains. The extrusions occur sequentially along slip planes until the stresses eventually form cracks at the intrusions of the multi-material interface that propagate through the slip planes and lastly across these extrusions. Cu film thicknesses above 1 μm were shown to typically contain an insignificant amount of cracks compared to the smaller film thicknesses, as extrusions were found to make up a majority of the deformation in these films [47]. Thus, the mechanisms for defect formation and growth become reliant on grain boundary diffusion rather than slip plane gliding as film thicknesses are decreased and the Cu consists of smaller average grain sizes [46]. Grain growth was also found to occur from cyclic Joule heating in these Cu thin films [46,48]. Lastly, defects were more susceptible in certain Cu grain characteristics, such as larger grains and the <001> orientation [48].

2.8 Real World Conditions and Potential Impact on TSVs

While consumer electronic components are typically expected to operate below 100 °C, extreme applications, such as military and aerospace, may require more extreme, higher threshold conditions. Consumer electronics can undergo up to 10 cycles a day if extensively used and are designed to last up to 10 years. On the other hand, specific applications can see up to 14 cycles per day with an

expected lifetime of up to 25 years [49]. Powering on and off devices as well as using these devices for overbearing tasks are the major contributors to the thermal cycling in electronics. Environmental changes also cause temperature fluctuations for these chips. This thesis will simulate the thermal cycling of Cu-TSVs and analyze the effects it has on reliability.

2.9 TSV analysis – Common Analytical Techniques

To examine the various thermo-mechanical reliability concerns of Cu-TSVs many analytical tools can be utilized. Some of the following analysis tools were mentioned in section 2.7, but all present different ways of viewing the multifaceted problems TSVs face. Some of these tools will be employed in the present study and will be discussed in more detail in Chapter 3 along with the specifics of their use and specific experimental and sample conditions.

1. Finite Element Analysis (FEA): Is also known as finite element modeling (FEM). These computer simulations provide a pre-experimental analysis of the stresses seen in the three layers of the TSVs and surrounding substrate.
2. Raman Spectroscopy: A non-destructive technique, which can determine relative stresses on the surface of the TSV-enveloping substrate through atomic interaction.

3. Nano-Indentation: C. Okoro *et al*. used nano-indentation to deduce the elastic modulus and hardness values of the electroplated Cu with thermal treatments [30].
4. Focused Ion Beam (FIB): The FIB is a high precision ion beam used to cross-section and image the TSVs for defect analysis.
5. Scanning Electron Microscope (SEM): SEM is utilized for void and other defect analysis of the TSV layers.
6. X-Ray Microscope: This instrument allows for a non-destructive means for examining void size and growth within the TSVs [40].
7. Electron Backscattering Diffraction (EBSD): EBSD can be conducted to investigate microstructural changes, such as grain size and grain orientation, of the Cu-TSVs.
8. White Light Interferometry (WLI): Like atomic force microscopy (AFM), WLI can be applied to detect the magnitude of Cu protrusion after heat treatments.

2.10 Focus of This Work

This thesis will strive to answer the following questions:

1. With the tools available, can a sample preparation method be developed to monitor variations of the following TSV characteristics?
    a. Assessment of TSV process uniformity/variation

        i. Within wafer uniformity (vias on the same wafer)
        ii. Wafer-to-wafer uniformity (vias on different wafers processed using the same fabrication method)
    b. Void and other defect configurations
    c. Defects and uniformity of the barrier layer and isolation liner
    d. Grain sizes
    e. Grain orientations
2. Are thermal cycling induced defects forming and evolving in industry prepared TSVs?
3. Is the RF performance hindered by thermal cycling parameters such as:
    a. Number of cycles
    b. Maximum temperature of cycling
    c. Cycling samples with or without pre-existing voids
4. Are one or more thermal cycling conditions altering the following internal TSV properties?
    a. Void and other defect size and probability
    b. Microstructure
5. Can links be made between shifts in the TSV signal loss and changes found within the TSVs?

6. What conclusions can be drawn from the results of these analyses, which will aid in understanding the relationship between processing and performance characteristics of TSVs.

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CHAPTER THREE

EXPERIMENTAL PROCEDURE

Solutions to the questions presented in section 2.10 were found by, first, obtaining samples of TSVs from industry partners who have been investigating process optimization for their fabricating, characterizing the as-received materials, simulating the conditions of typical integrated circuit operations via thermal cycling, and then developing a sample handling protocol to evaluate the post-cycling changes to physical attributes and microstructural attributes from that of the as-received samples. As-received (AR) wafers containing TSVs were evaluated as discussed below. A sample preparation method was then developed to enable easy access for material property changes upon testing the TSVs. The radio frequency signal loss, defect nucleation and growth, as well as the microstructure evolution were all monitored after the samples were exposed to the various simulated conditions. This chapter contains descriptions of how the TSVs were prepared, tested and analyzed, with a description of process methodologies specific to this thesis.

3.1 Preparation of The TSVs Used In This Study

This work was carried out in partnership with the National Institute of

Standards and Technology (NIST) as part of the institute's ongoing efforts to evaluate promising technologies for future IC communication strategies. To that goal, evaluation of new materials used in novel IC architectures are ongoing in the Semiconductor and Dimensional Metrology Division group, and this project with NIST focuses on one part of that architecture, TSVs, as discussed in Chapter 2. For this effort, two types of Si wafers containing Cu-TSVs were obtained by NIST partners from SEMATECH.

The substrates for each sample type are made of monocrystalline Si and contain Cu bond pads, under which blind Cu-TSVs are located. Under each bond pad is a 6 by 6 array of TSVs with a TSV to TSV pitch of 12.5 μm. These Cu-TSVs are cylindrical in shape with a slight taper. They are approximately 5.5 μm in diameter and 50 μm tall, giving them an aspect ratio of approximately 10:1. The primary distinction between the two sample sets is that one set contains TSVs with pre-existing voids while the other does not. For easy identification and distinction, the sample types will be referred to as voided and non-voided samples respectively. The pre-existing voids were engineered into the TSV by tuning the Cu deposition process. Both sample types were held at 150 °C for 60 minutes after Cu electrodeposition. In addition, the voided sample wafer received additional thermal cycling to simulate the process for BEOL addition.

For this work, a total of 32 samples were used in this study. The RF measurements were conducted on 24 samples, while cross sectional analysis

was run on 8 different samples as shown in Table 3.1. Four voided and non-voided samples were designated for each of the three maximum thermal cycling temperatures for RF signal measurements. Cross sectional analysis, including polishing, focused ion beam (FIB) milling, defect analysis, and EBSD, was administered on one as-received sample from each sample type as well as one sample after every cycling interval, for each maximum cycling temperature, and for each sample type. Further thermal cycling details are discussed in the next section. For more details on how the samples were divided for testing see Appendix A. Figure 3.1 illustrates sequence in which the experiments were conducted.

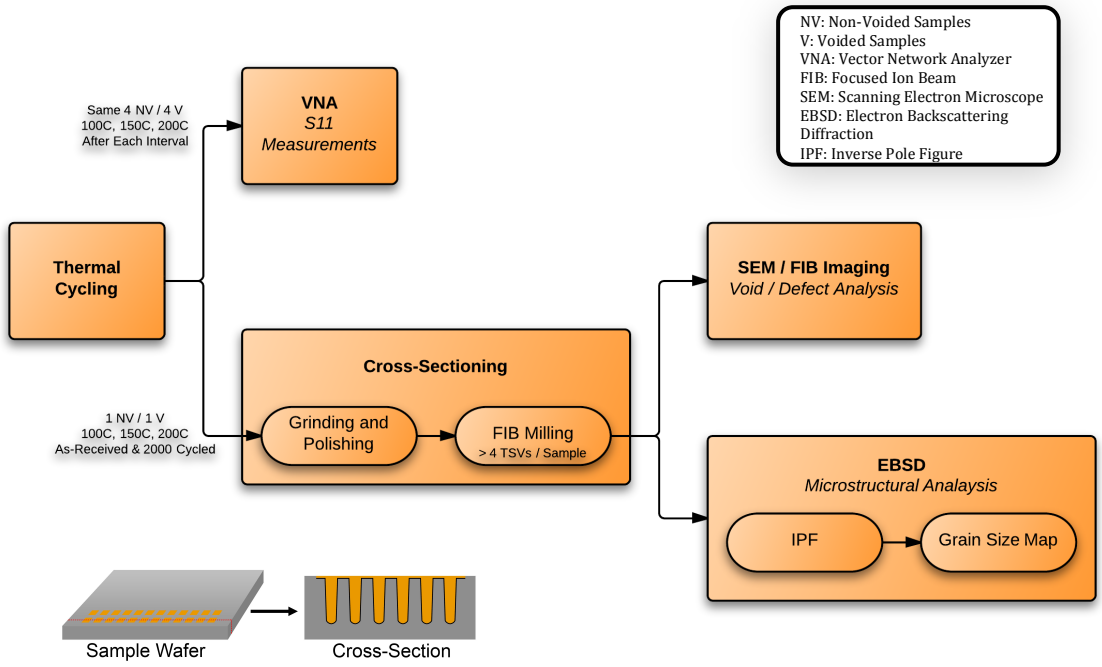

Figure 3.1: Diagram showing the experiment sequence of this study.

3.2 Pre- and Post-Fabrication Materials Characterization

3.2.1 Sample Preparation

Prior to any evaluation, samples were received, cataloged and inspected using visual, and optical microscopic techniques to inspect for any shipment related defects. All samples were labeled with their identity and known history. This registration was carried forward in further analysis. This registration and assignment of samples to specific tests are summarized in table 3.1.

3.2.1.1 Thermal Cycling

As discussed in Chapter 2, thermal excursions are a natural consequence of IC device life, as the device undergoes cycling through use that will ultimately dictate device life-cycle and failure. To simulate the in-service life and the effect on sample properties and microstructure, a series of experiments were designed to evaluate material changes with various maximum use temperatures and numbers of heating/cooling cycles the wafer was subjected to. The goal here was to impart excursions in temperature, which might result from typical use, on the wafer and TSVs to probe how such cycling modified via attributes and performance. As-received sample wafers underwent thermal cycling in a chamber as seen in Figure 3.2. The chamber consists of a hot plate, containing a channel for chilled water to flow, allowing for increased cooling rates. A thermocouple connected to a computer records the temperature and communicates to the system. A typical temperature profile for thermal cycling is

shown in Figure 3.3. Once the desired temperature is reached the hot plate is turned off and water is allowed to flow. When the 30 °C is attained, the process is repeated until all thermal cycles are complete. Thermal cycling was performed from 30 °C to a maximum temperature of 100 °C, 150 °C, or 200 °C. Samples were cycled up to 2000 cycles in increments of 500 cycles. The cycling sequence is illustrated in Figure 3.4.

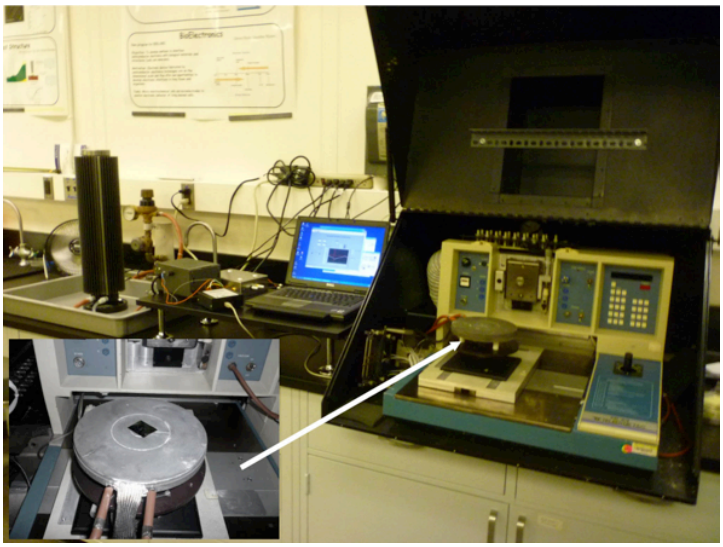

Figure 3.2: The thermal cycling instrument used for heat-treating samples. The sample chamber, on the right, contains a hot plate, which exposes the samples to heat and allows fast cooling.

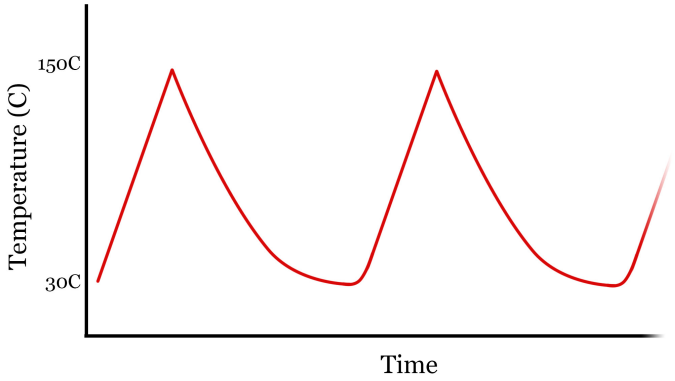

Figure 3.3: A typical thermal cycle temperature profile for a maximum cycling temperature of 150°C.

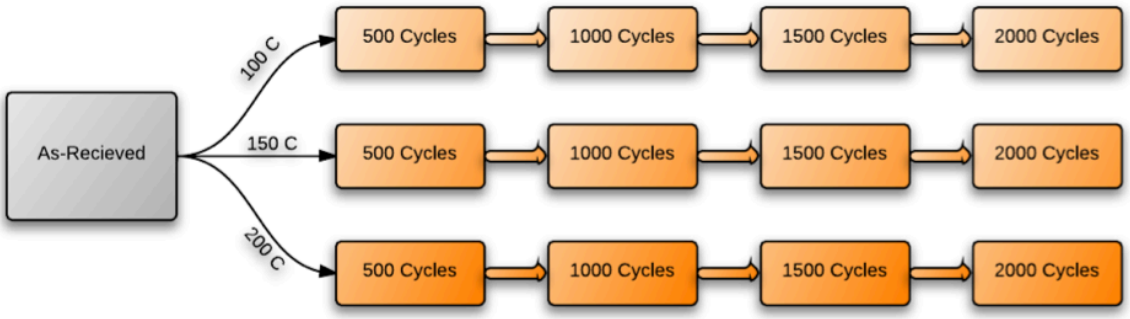

Figure 3.4: Diagram showing the thermal cycling conditions, including the three maximum cycling temperatures and cycle numbers at which measurements were made.

3.1.2 TSV Sample Preparation - Cross Sectional Milling

To be able to view the starting TSV sample structure (depth, width, wall thickness and uniformity, oxide layer thickness, presence (or not) of voids, microstructure/grain features, and the changes to these attributes with thermal cycling, a dedicated sample preparation methodology specific to these specimens had to be developed. Specifically, a technique to cut the wafers, expose the vias, polish them for optical/electron microscopy viewing and subsequent imaging and image analysis, was developed. The goal of this process development was to create a repeatable specimen fabrication process that would not impart fabrication-induced artifacts into the Cu of the TSVs, which could interfere or affect the FIB milling for suitable EBSD patterning. The procedure developed and used for all samples evaluated in this study, are discussed below.

After subjecting the samples to heat treatment cycle(s), the copper TSVs were cross-sectioned using two consecutive techniques for post-cycling

evaluation. Samples were first polished down to the TSVs' center using a protocol developed for grinding and polishing. The cross-sections were milled further with a focused ion beam (FIB). The ultimate goal of cross sectioning is to provide sufficient surface quality for void and other defect investigations as well as grain analysis. One sample from each subset after every cycle interval was designated for cross sectioning.

3.2.1.2.1 Grinding and Polishing

Grinding and polishing was used to help reduce the time needed for future analysis with the FIB. A protocol was established for grinding and polishing these TSVs accurately and precisely. A similar method was used by T. P. Moffat and D. Josell to polish Cu-TSVs [1]. The surfaces of the samples were first cleaned. A semi-transparent, quick-curing epoxy was applied to the surface before adding a thin cover glass to protect the sample surface. This cover glass proved to be necessary later in the polishing phase for providing good edge retention. This is to ensure the top of the samples and TSVs are not rounded off during polishing. The samples were mounted on a cross sectioning platform, shown in Figure 3.5. As mentioned previously, these samples contain rows of 12 bond pads which each contain an array of six by six TSVs. The samples are aligned to section through these 12 bond pads, guaranteeing multiple TSVs are milled simultaneously. Diamond lapping paper of different fineness were used to grind down the samples. Stepping down in abrasive grit size (from 6 μm to 0.5

μm) helped control the speed at which the samples were milled and the surface quality of the cross section. Grinding was executed down to 0.5 μm grit and until the tips of the TSVs were revealed on the cross section. FIB of sectioned samples showed that particles from the diamond lapping paper were getting embedded into the soft copper of the TSVs and was causing uneven ion beam milling as seen in Figure 3.6. To eliminate this, an extra polishing step was added using a Buehler Microcloth polishing pad in conjunction with Masterprep, a 0.05 μm alumina suspension. This polishing step was conducted until a cross section of the middle of the TSVs was complete. To reduce charging from imaging techniques such as SEM and FIB, the cover glass was ground down. A final polished cross section is shown in Figure 3.7.

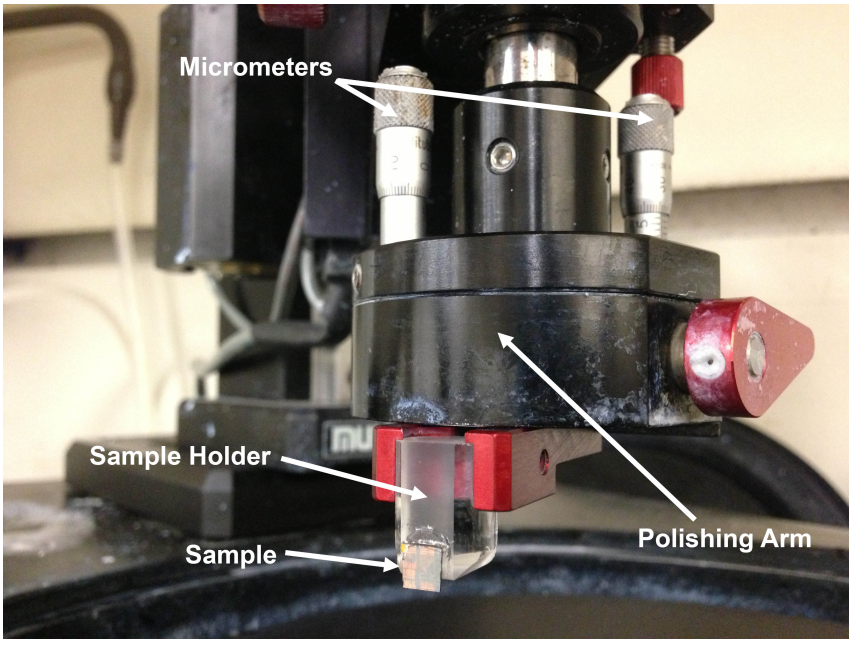

Figure 3.5: The polishing arm and sample holder for cross-sectioning samples. The two micrometers on the arm are used to align the sample, for accurate cross-sectioning and the sample is mounted to the glass on the sample holder.

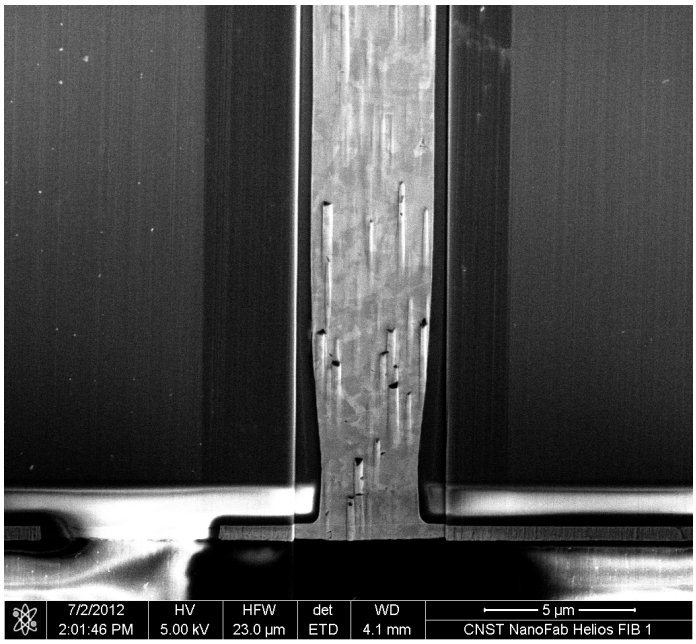

Figure 3.6: Ion beam image of TSV after milling, where diamond is embedded into the Cu, causing uneven FIB milling.

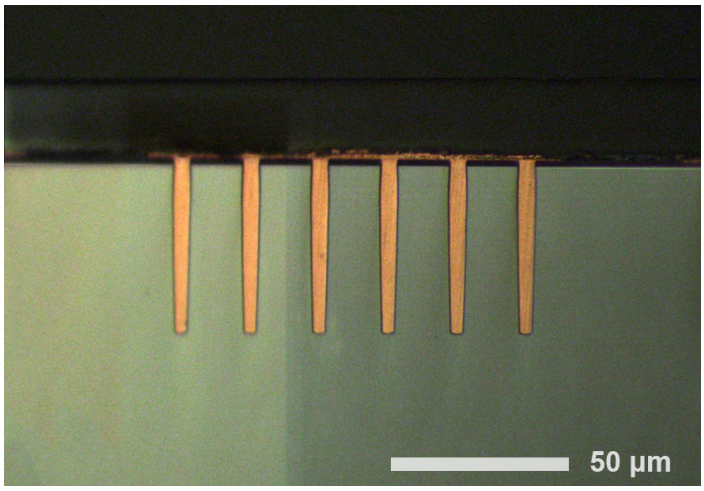

Figure 3.7: A successfully polished cross section of a sample. The cover glass remains on top of the sample and six Cu-TSVs are shown.

3.2.1.2.2 Focused Ion Beam

The Advanced Materials Research Laboratory's (AMRL) Hitachi Dual Beam NB 5000 was used to mill the polished cross-sections and provide a smoother TSV cross-section, which could be analyzed for defects, visually, and microstructural changes, using the EBSD. It is a dual beam instrument that contains a scanning electron microscope (SEM) and focus ion beam (FIB). The instrument's Ga^+ liquid metal ion source (LMIS) was used for precision milling and imaging. Ga^+ ions are propelled at the surface of the sample sputtering away ions and atoms. The FIB produces smooth etched surfaces that reveal grain structure and can be used for electron backscattering diffraction (EBSD) studies. It also provides good edge retention, a feature that can plague grinding and polishing. Edge retention is needed to analyze voids and other defects in the system.

Figure 3.8 illustrates the method used to mill from the cross section. The samples were milled parallel to the cross section and from the top of the sample down. A 41 keV source was used for milling. This high beam energy is the maximum for the Hitachi NB5000 and makes it very precise, compared to lower beam energies, which would spread out the beam area, creating lower quality and longer to mill cross sections.

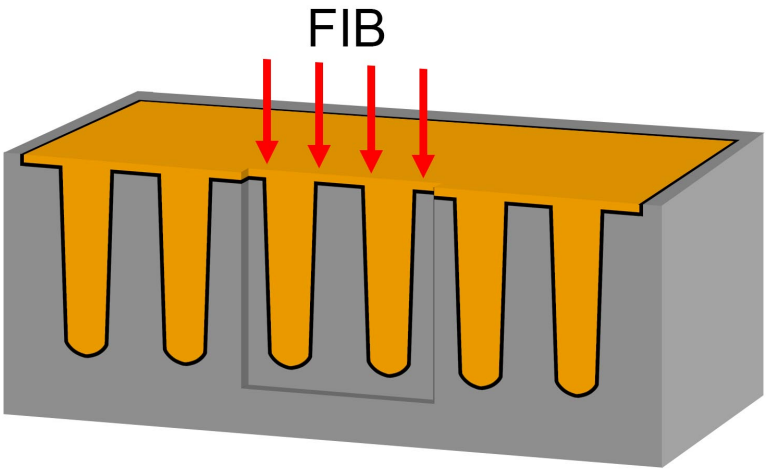

Figure 3.8: Illustration of the FIB milling direction, parallel to the cross section.

3.2.2 Material Property Analysis and Measurement Techniques

Discussed in this section are details of the S_{11} measurements, taken before cross-sectioning, and void and microstructure measurements, conducted after sectioning the TSVs, both prior to and following thermal cycling. The two wafer types were first characterized by visually inspecting the TSV cross-sections. To accomplish this, the cross-sectioning protocol described in section 3.2.1.2 was used.

3.2.2.1 Radio Frequency Properties

Proceeding the thermal cycling, the TSVs were tested for signal integrity. The goal of these measurements is to determine if signal loss tracks with thermal cycling. The PNA N5230A a radio frequency (RF) vector network analyzer (VNA), was used for these measurements and is shown in Figure 3.9. An optical

microscope attached to the instrument is needed to locate the area of interest and verify that the probe touches down on the sample's bond pads. The probe is three-pronged, as illustrated in Figure 3.10, with the middle prong sending and receiving the signal.

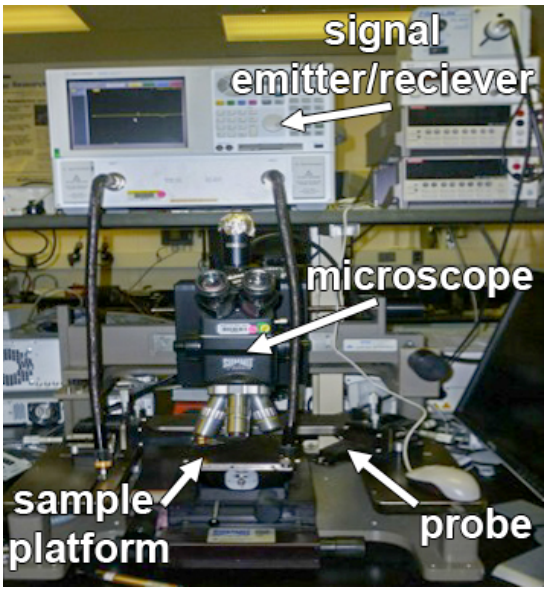

Figure 3.9: The components of the VNA used to measure S_{11} parameter.

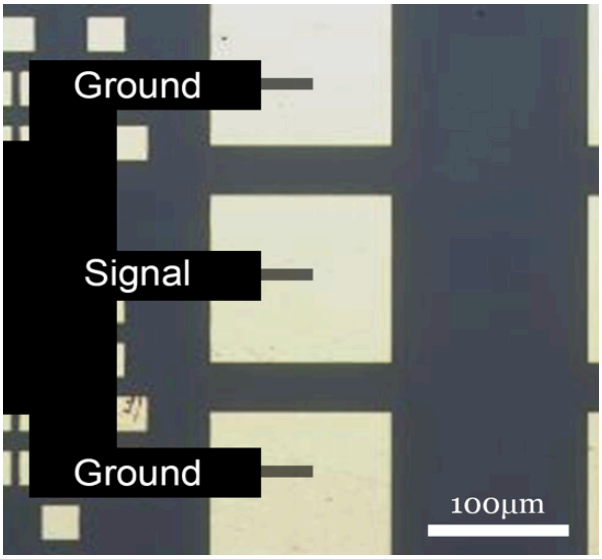

Figure 3.10: Illustration of the three-pronged probe used by the VNA to measure the S_{11} parameter.

The VNA works by sending an RF signal with different frequencies into the bond pad. By doing so, the signal bounces off the walls of the TSVs and is detected by the instrument. The VNA records the percent of the signal that is reflected back to measure the S_{11} parameter. The S_{11} parameter, otherwise known as the reflection coefficient, is a complex number that consists of a magnitude and phase shift.

Before beginning measurements on each sample set, a baseline is conducted. A measurement is taken without the probe in contact with the sample. This will be used later to eliminate any irregularities caused by the probe. There are twelve aligned bond pads, ten of which are measured with the VNA. Under each bond pad is an array of six by six Cu-TSVs, therefore every measurement is the average of 36 TSVs. The same four samples from each set were measured after each cycling interval to reduce sample inconsistency. Lastly, measurements were conducted from 700 MHz to 40 GHz.

3.2.2.2 Defect Analysis

Once cross sections have been completed with the FIB, defect analysis is conducted. Voids and other defects in the TSVs are analyzed to show their formation and evolution with thermal cycling. Four TSVs from each sample are randomly selected to study. Each TSV is closely analyzed using either SEM or FIB to inspect for many types of defects, including cracks, interfacial defects, and voids. Ion imaging with the FIB can help indicate where the defects are in

correlation with the copper grains due to its superior grain contrast over SEM imaging. At low beam currents, instead of sputtering away ions, the incoming ions force secondary electrons to part from the surface. These electrons are known as ion-induced secondary electrons (ISE). They are lower energy then secondary electrons, seen from SEM. The major difference between imaging with the SEM and FIB is ion channeling that occurs due to the ion beam. When the ions penetrate into the sample, they interact with the crystal lattice. Depending on the orientation of the crystal, the ion hits a different amount of atoms through the material emitting a different amount of ISE from the sample. This is what creates contrast in grain structures, making it beneficial to use the ion beam for microstructural analysis [2]. The location, quantity, and total defect area have been investigated with respect to sample type, as well as the number and maximum temperature of thermal cycling.

Most of the defect analysis took place using the scanning electron microscope (SEM) available at Clemson University's Advanced Materials Research Laboratory. A SEM functions by exposing electrons to the surface of a material under some amount of vacuum. The vacuum helps keep the electrons in focus. As the electron beam is exerted from the column and "scanned" across the surface of the specimen, detectors within the chamber record data into an image that is then projected onto a computer monitor. The SEM chamber is seen in Figure 3.11. Two main types of detectors document this data, the secondary

electron detector and backscattered electron detector, which record the secondary electrons (SE) and backscattered electrons (BSE), respectively, that derive from the original primary electron beam. SE is relevant for topographical analysis and emit from the surface of the sample. BSE penetrate further into the sample and thus reveals more compositional or microstructural information.

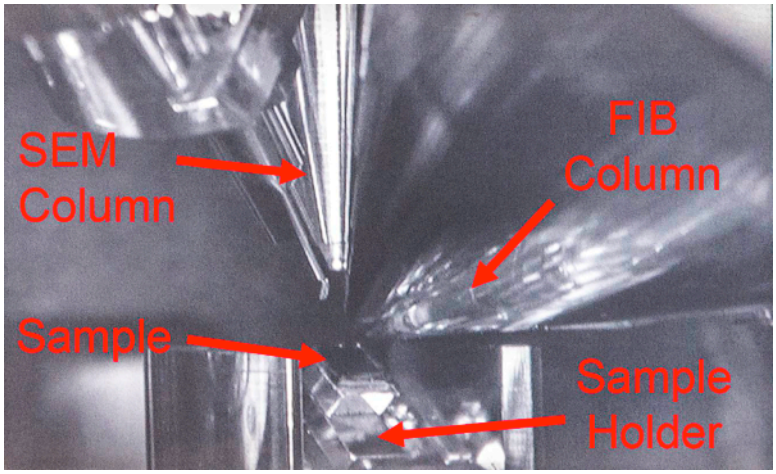

Figure 3.11: Infrared image of the Hitachi NB5000 dual beam chamber.

3.2.2.3 Microstructural Analysis

To examine the microstructural development as thermal cycling progresses, EBSD was performed. The two key aspects of interest from the microstructure are the grain size and orientation, but other characteristics, such as grain aspect ratio, were analyzed. As mentioned earlier, the FIB provides a slightly etched, smooth cross section of the TSVs, which is ideal for EBSD. EBSD utilizes the SEM column to detect the orientation of crystals in a material. The sample is placed in the SEM chamber and tilted at an 80° angle. If the

sample is placed in the proper configuration, this tilt allows diffracted electrons to be detected by a phosphor screen, which is placed 90° from the column. To diffract, electrons must satisfy Bragg's law (eq. 3.1) and constructive interference ensues.

$$n\lambda = 2d \sin\theta \qquad (3.1)$$

Bragg's law takes into account an integer, n, the wavelength of the incident wave, λ, the lattice spacing of the crystal, d, and the diffraction angle of the electron, Θ. Constructive interference occurs when the phase shift between two incident waves is a multiple of 2π. Since crystals are periodic, this principle allows the detection of different crystallographic orientations through known lattice spacings. As electrons are diffracted and detected by the phosphor screen, patterns, called Kikuchi bands, form. A camera offers a live feed of the Kikuchi bands from which a database detects the orientation of the crystal. A diagram of the EBSD set up and example of Kikuchi bands are shown in Figure 3.13. EBSD was conducted, with a 0.05 μm step size, on at least four FIB milled TSVs per sample. EBSD analysis has the ability to determine grain orientation with inverse pole figures (IPF).

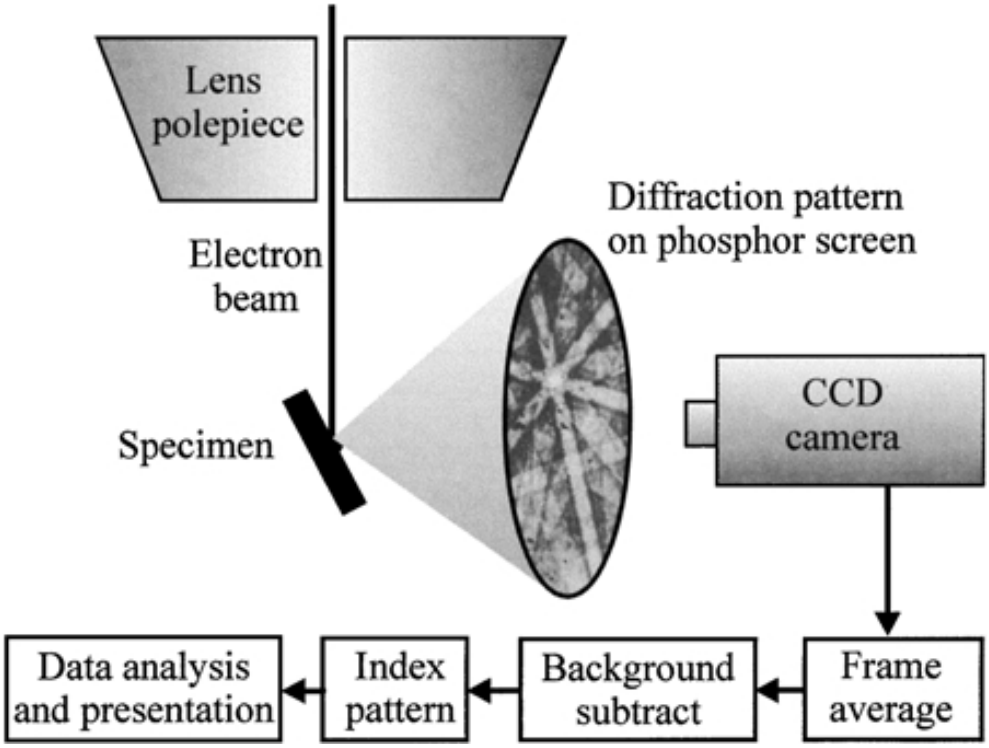

Figure 3.12: Diagram showing a normal EBSD setup, taken from reference [3].

The EBSD analysis software also produces grain size maps, which exclude twin boundaries [4]. These maps highlight every grain with a different color making them more distinguishable. Copper grain size measurements were conducted on each grain individually using the grain size maps.

$$GS = \sum \frac{L+D}{2} \qquad (3.2)$$

Equation 3.2 is used to measure average grain size in the TSVs, where GS is the grain size, L is the longest length of a grain, and D is width of the grain perpendicular to L, as shown in Figure 3.14. The TSVs were also divided into three equal regions, top, middle, and bottom, for further grain size evaluations. Figure 3.15 illustrates these regions. For regional grain size measurements, a

weighted equation was used since some grains span into multiple regions. The average grain size in each region is calculated using equation 3.2. The grains' area fraction within the region is also considered as the weighted average regional grain size is calculated with equation 3.3,

$$RGS = \frac{\sum GS*AF}{fN} \quad (3.3)$$

where RGS is the regional grain size, GS is the grain size of a single grain, AF is the area fraction of that grain, and N is the total number of grains in the region. When a grain is only encompassed by one region it counts as one, but the area fraction is used for those grains that cross into multiple regions to calculate N.

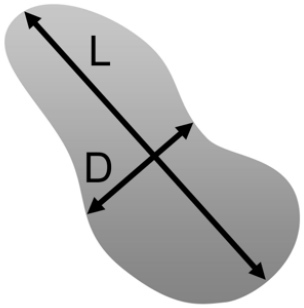

Figure 3.13: An illustration of the measurements needed for grain size calculations. L is the longest length of the grain and D is the width perpendicular to L.

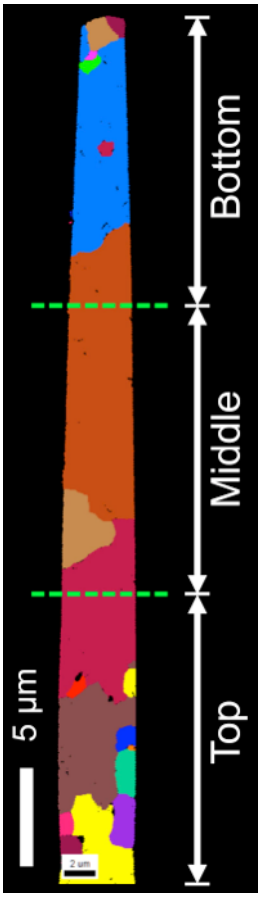

Figure 3.14: A grain size map of a TSV, showing the regions used for regional grain size measurements.

In summary, two types of samples, voided and non-voided, were thermal cycled up to 2000 cycles at 500 cycle intervals. Three different maximum cycling temperatures, 100 °C, 150 °C, and 200 °C, were used to simulate various in-use thermal excursions. A VNA was used to conduct S_{11} parameter measurements on four samples from each maximum cycling temperature and sample type after each cycling interval. A different sample from each cycling condition was cross-sectioned using the protocol developed. This required polishing and FIB milling.

Void analysis was then conducted on the TSV cross sections with SEM and FIB imaging. Finally, the copper of the TSV cross-sections underwent microstructural analysis, via EBSD, to determine average grain sizes, grain shapes, and preferential grain orientations. Results from these measurements are discussed in Chapter 4.

3.3 References

1. T. P. Moffat and D. Josell, 'Extreme Bottom-Up Superfilling of Through-Silicon-Vias by Damascene Processing: Suppressor Disruption, Positive Feedback and Turing Patterns,' *Journal of The Electrochemical Society*, 159 [4] D208-D216 (2012).

2. C. A. Volkert and A. M. Minor, 'Focused Ion Beam Microscopy and Micromachining,' *MRS Bull*, 32 [05] 389 (2007).

3. F. J. Humphreys, 'Review Grain and subgrain characterisation by electron backscatter diffraction,' *J. Mater. Sci.*, 36 [16] 3833-3854 (2001).

4. OIM Data Analysis (vers. 6) EDAX Inc. 2010.

CHAPTER FOUR

RESULTS

As mentioned in previous chapters, thermo-mechanical failure is a major concern in Si substrates that incorporate Cu-TSVs. Heat treatment via thermal cycling was performed to simulate real world use of these chips containing Cu-TSVs. Cycling took place up to 2000 times and the maximum cycling temperature was varied for different samples between 100 °C, 150 °C, and 200 °C. A cross-sectioning protocol was developed. The signal integrity of these interconnects was extracted from analysis of these data, and the results are disclosed along with the defect and microstructural analysis.

4.1 As-Received Sample TSV Characterization

The as-received (AR) samples, or samples straight from SEMATECH, did not undergo the thermal cycling discussed in 3.2.1.1. As was stated in Chapter 3, the two sample types, voided and non-voided, underwent different via processing protocols. The TSVs of interest in both sample types lie underneath bond pads. In each, there are two rows of twelve bond pads, each containing a total of 36 TSVs as shown in Figure 4.1. Although every TSV is unique and slightly differs in structure and properties, they are approximately 50 μm tall and

have a diameter of about 5.5 μm.

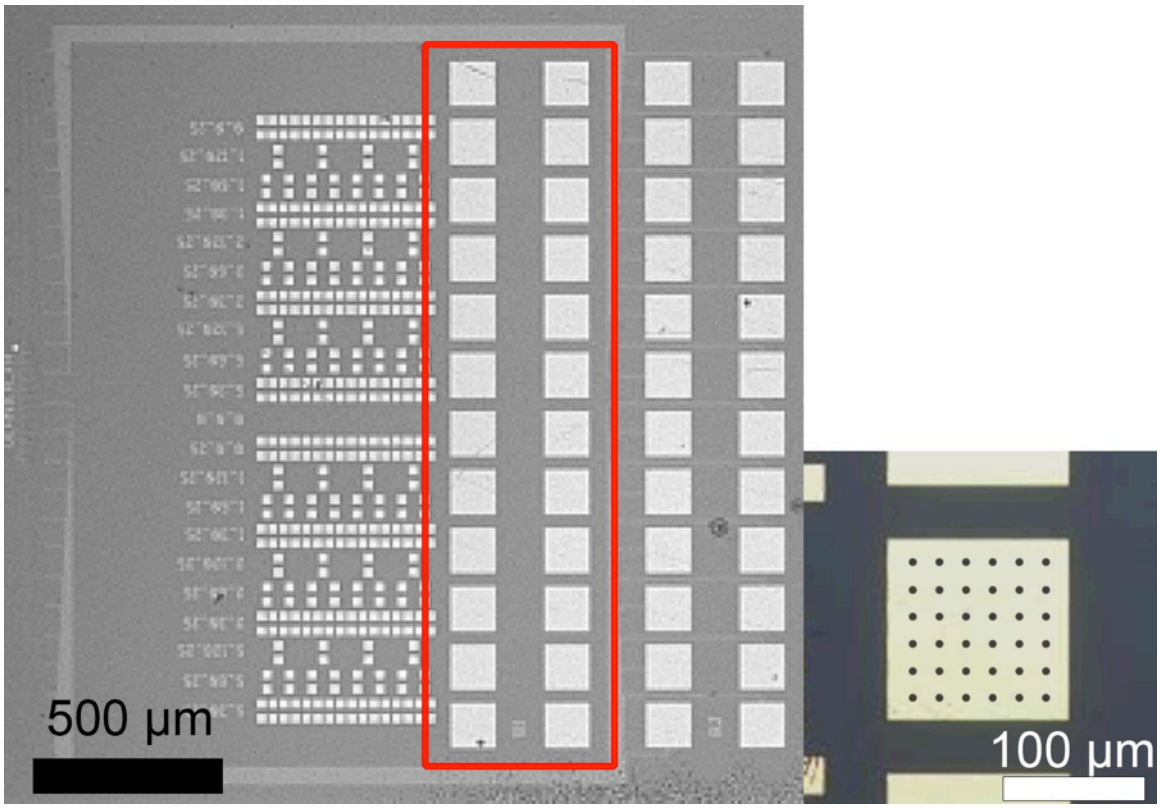

Figure 4.1: Optical images of an as-received sample. The left shows the two rows of twelve bond pads of interest highlighted in red. On the right is a close up optical image of a single bond pad, where the black dots represent the 6 by 6 TSV matrix that lies underneath the bond pad.

The cross-sections of the as-received voided and non-voided samples, produced by the method developed in section 3.2.1.2, are shown in Figure 4.2. The TSVs of the voided sample typically contained seams at the top, large spherical voids in the lower region, and microvoids dispersed throughout. Only microvoids, typically less than 0.5 μm, were found distributed throughout the top and mid regions of the non-voided sample TSVs.

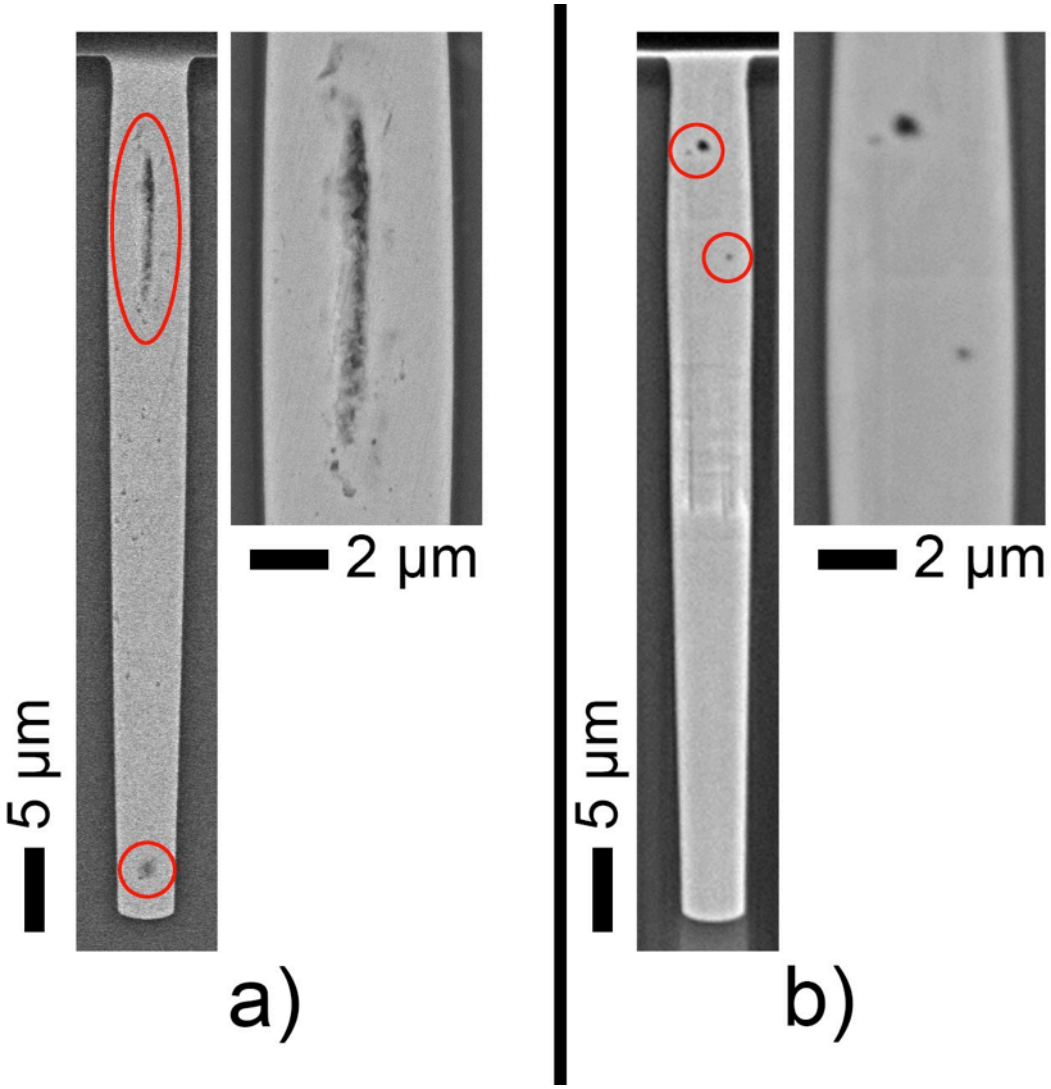

Figure 4.2: SEM images of the as-received sample cross-sections with the voids circled in red and a zoomed in image of each sample for the a) voided sample and b) non-voided sample.

4.2 Cross-Sectioning Protocol – Repeatability of Process

The cross-sectioning method developed in section 3.2.1.2 was a two-step process involving polishing and focused ion beam (FIB) milling. Grinding and polishing was necessary to reduce FIB milling time. The major setback in the

fabrication method, alluded to earlier, was diamond grinding particles becoming embedded in the copper from the diamond lapping paper used during grinding. A scanning electron microscope (SEM) image of a cross section containing these diamond particles is shown in Figure 4.3. As discussed in section 3.2.1.2 uneven FIB milling, shown in Figure 3.6, results from these diamond particles, making the quality of electron backscattering diffraction (EBSD) inadequate. Polishing with a 0.05 μm alumina suspension solved this problem. The addition of a cover glass to the top of the samples was necessary in preventing rounding of the samples and the TSVs and consistently creates particle-free cross-sections, such as the TSVs shown in Figure 3.7. This adds to the extra step of grinding down the cover glass and coating the sample with platinum to reduce charging from the glass during milling. Uneven ion milling was still seen if the roughness of the top surface was too high resulting from the grinding of the cover glass. Grits less than 3 μm were required to produce repeatable EBSD quality milling. However, if the TSV being milled contains large voids, the voids can act as a rough surface as well, creating irregular milling patterns. Voids are unavoidable in some of these samples and are one of the main focuses of this work. Acceptable quality ion milling is arbitrary when large voids are exhibited in the Cu-TSVs. High quality EBSD results are very distinct, however, making it easy to include only these results in the findings. This difference in EBSD quality is shown in Figure 4.4.

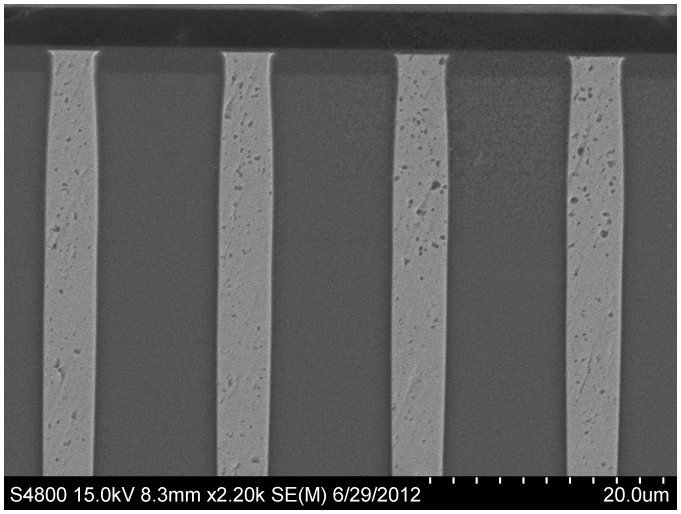

Figure 4.3: Diamond particles from the diamond lapping paper embedded in Cu-TSVs.

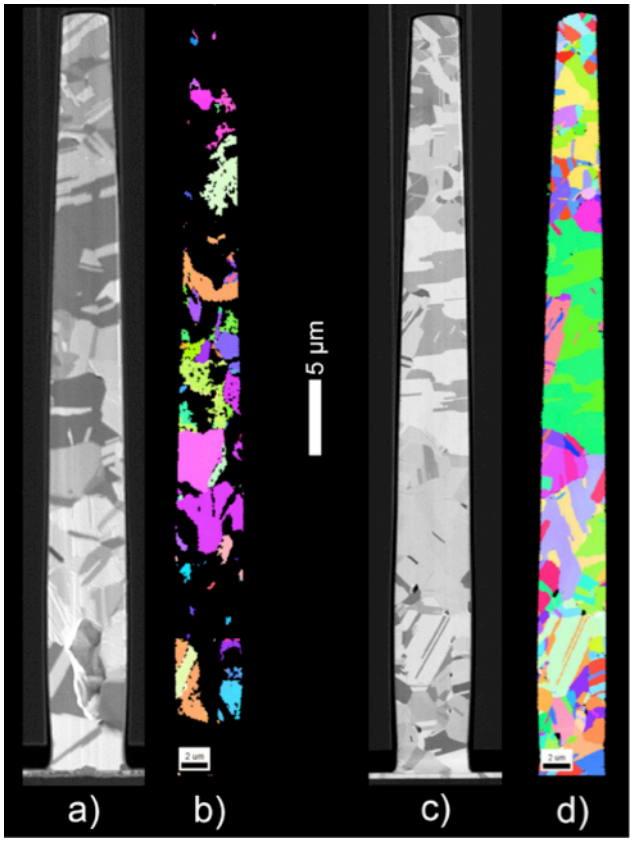

Figure 4.4: FIB images and IPF maps from the EBSD. a) FIB image of voided sample, b) IPF map of TSV shown in a), c) FIB image of non-voided sample, d) IPF map of TSV shown in c).

With the dual beam setup of the Hitachi NB5000, it is difficult to determine how close to the center the TSVs have been milled during the process. Since both the SEM and FIB column are above the sample (as shown in Figure 3.12), the cross-sectional area cannot be easily viewed during milling, which occurs from the top of the sample. Even if the cover glass was not there, the copper bond pads lay atop the TSVs, so the TSVs are not visible from the top of the sample. This makes it difficult to precisely determine when the center of the TSVs have been reached in the sectioning process.

4.3 RF Signal Measurements

Thermal cycling tests were used to simulate and assess in-use changes in the Cu-TSVs and the subsequent variation of the RF properties that might result from such cycling-induced changes to the specimens. Following each thermal cycling interval, described in section 3.2.1.1, the S_{11} parameter was measured using a vector network analyzer (VNA). As shown in Table 3.1, four samples were measured for each of the six thermal cycling conditions, a combination of maximum cycling temperature and sample type, after each cycling interval, shown in Figure 3.4. After every interval, the S_{11} parameter was measured on 10 bond pads for each specimen, to produce the best estimate of the mean value. The S_{11} parameter was extracted over a range of 700 MHz to 40 GHz radio frequencies. The graph in Figure 4.5 is a representative plot of S_{11} parameter in

decibels (dB) versus frequency (MHz) for the non-voided sample, following thermal cycling at a maximum temperature of 100 °C. Measurements were performed at 500 cycle intervals as defined in the legend. The line drawn is the best fit from ten individual data points obtained by averaging measurements from four samples, where each sample is measured ten times. The error for each data set (line) is less than 0.1 dB in both directions and results from sample and calibration variation. The S_{11} curve shapes remain similar between the two sample types (voided and non-voided), as well as with cycling amount. This figure, which shows a similar decrease in S_{11} through ~ 15 GHz followed by an increase in S_{11} at higher frequencies, is representative of the graphs for all the cycling conditions. The increase at high frequency is followed by a dip. Raw data for all RF measurements, not shown here, are included in Appendix A.

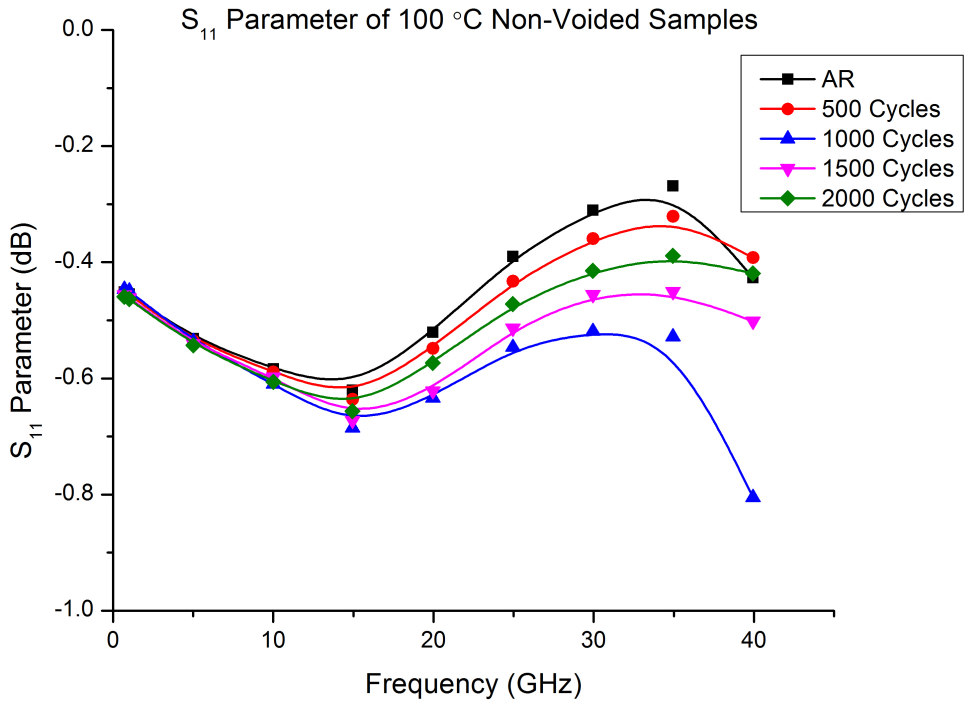

Figure 4.5: The S_{11} parameter as a function of frequency for the non-voided samples cycled to a maximum temperature of 100 °C.

For a more detailed assessment of the data, the 10 GHz and 20 GHz data points were separated from the previous plots and averaged. These averages are shown in Figure 4.6, where the non-voided specimens are on the left and the data from the voided specimens, are to the right. A clear distinction can be seen in the S_{11} frequency response between the two sample types. The voided samples have a much worse S_{11} parameter than their non-voided counterparts. Furthermore, a decrease in S_{11} is seen in the non-voided samples as maximum cycling temperature is increased from 100 °C to 150°C, while the voided samples don't show a shift in S_{11} with temperature. Instead, S_{11} of the voided samples take a drastic dive after any amount of cycling. Lastly, the S_{11} parameter does

not appear to change as the number of thermal cycles, the samples were subjected to, increased.

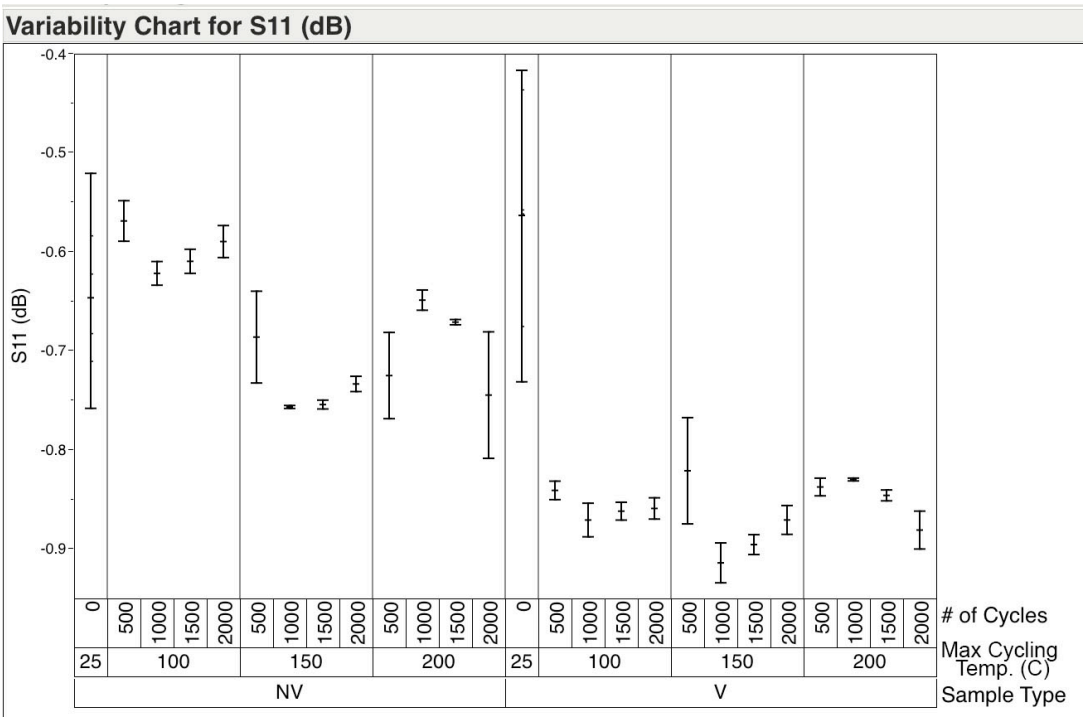

Figure 4.6: Graph of the S_{11} parameter at 10 GHz and 20 GHz for all samples, showing how the non-voided samples have less loss than the voided samples.

4.4 Void and Other Defect Measurements

All cross-sectioned samples were examined for defects, both within the Cu and other TSV layers, using SEM and FIB imaging. Voids were observed in both sample types, even in as-received (AR) samples, which were not thermally cycled. SEM images of the two as-received sample type cross-sections were shown earlier this chapter in Figure 4.2. To reiterate the findings, there is a drastic difference in void size and type between the non-voided and voided samples. While the non-voided samples' TSVs contained microvoids, that are

small and spherical in shape, most of the TSVs within the voided samples consisted of microvoids as well as large seams and bottom voids. Most voids, regardless of type, were found on grain boundaries, as shown in Figure 4.7. The seams and bottom voids were typically located near the center of the TSVs for the voided samples. On the other hand, the microvoids found in the non-voided samples were usually found at the top and middle of the TSVs.

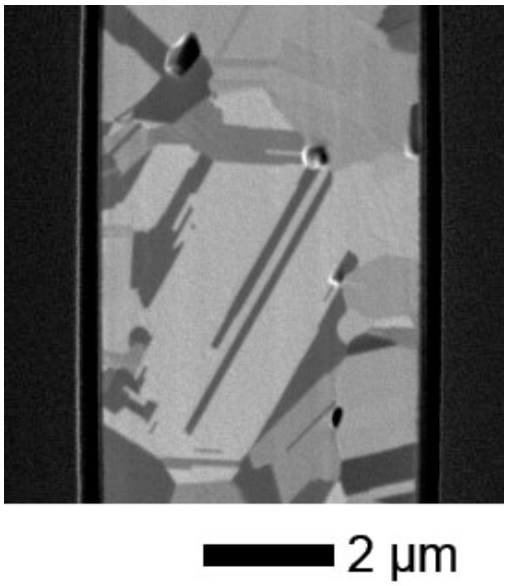

Figure 4.7: FIB image of typical void location in the Cu grain boundaries.

Figure 4.8 shows a plot of the average void area per TSV for both sample types before cycling and after 2000 cycles for all three maximum cycling temperatures. As expected, the voids in the as-received voided sample encompassed a larger area on average (2.62 ± 0.17 μm) compared to the non-voided as-received samples, with a lower average void area (0.22 ± 0.06 μm).

Both sample types show an increase in void area after cycling, which scaled with maximum cycling test temperature. Furthermore, as shown in Figure 4.9, the average void size in the TSVs increases after cycling, but does not appear to be affected by the maximum cycling temperature.

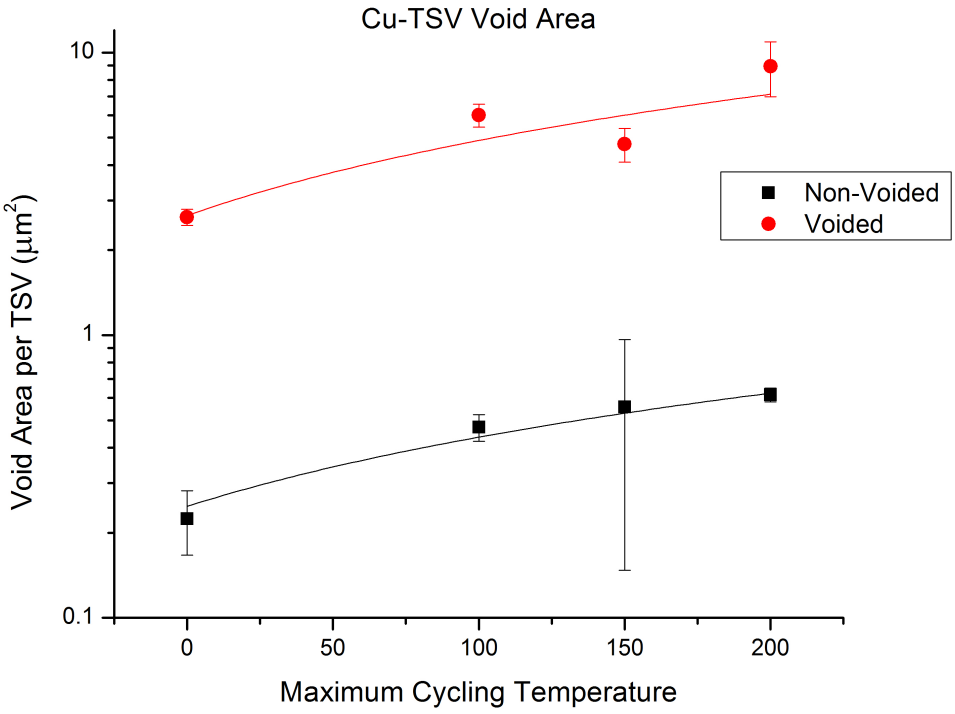

Figure 4.8: The average void area within in the TSVs before and after cycling for both sample types, which shows a linear correlation to maximum cycling temperature.

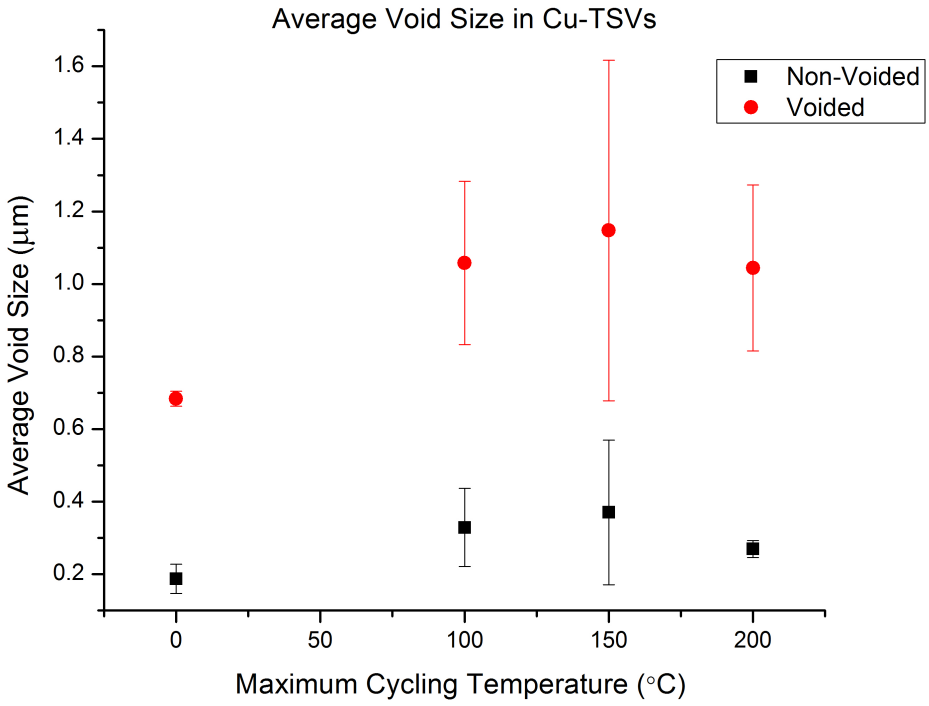

Figure 4.9: The average void size for both sample types before and after 2000 thermal cycles. No significant change in average void size is seen from thermal cycling.

Other, more uncommon, defect types were seen from the cross-sectional images of the TSVs. Some instances were observed where the Cu separated from the barrier layer of the TSVs, as shown in Figure 4.10a. Voids were sometimes observed at the interface between the Cu-TSVs and the bond pads, like in Figure 4.10b, before and after cycling. Lastly, no defects were found in the barrier layer or isolation liner of any of the cross-sectioned TSVs.

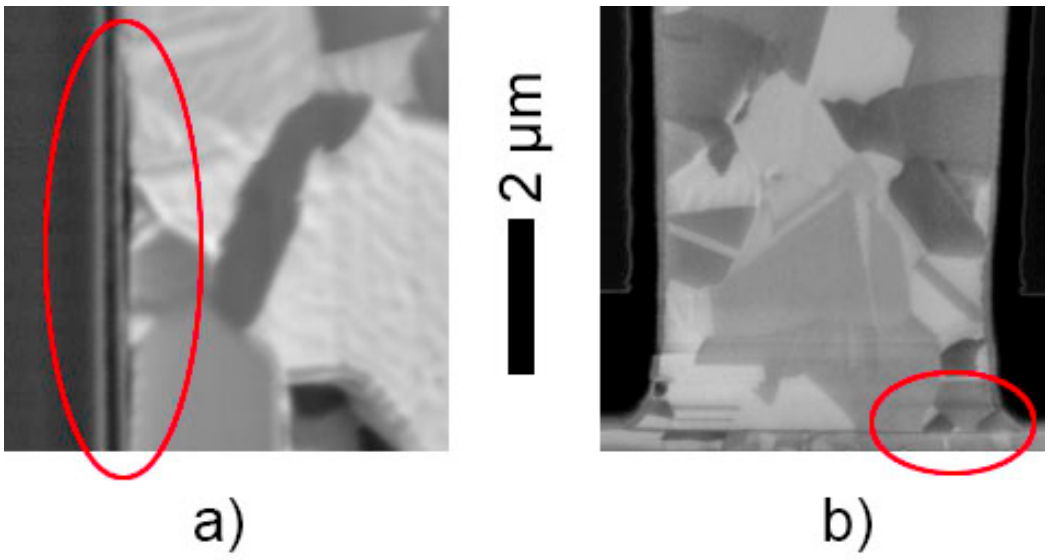

Figure 4.10: Ion beam images of a) delamination between the Cu and the barrier layer after 2000 cycles with a max cycling temperature of 200 °C and b) voids at the Cu-TSV/bond pad interface before thermal cycling.

4.5 Microstructure

The cross-section methodology developed in section 3.2.1.1 of this thesis for purposes of examining TSVs and their changes when subjected to in-use conditions, allowed microstructural evaluation of the Cu-TSVs, via EBSD.

At least four TSVs from each sample were analyzed for grain size and grain orientation. The EBSD produces an array of microstructural data, including grain orientation, and grain size maps. These were among the important information interpreted from each EBSD run. Figure 4.11 reveals the EBSD maps studied in this work for each TSV.

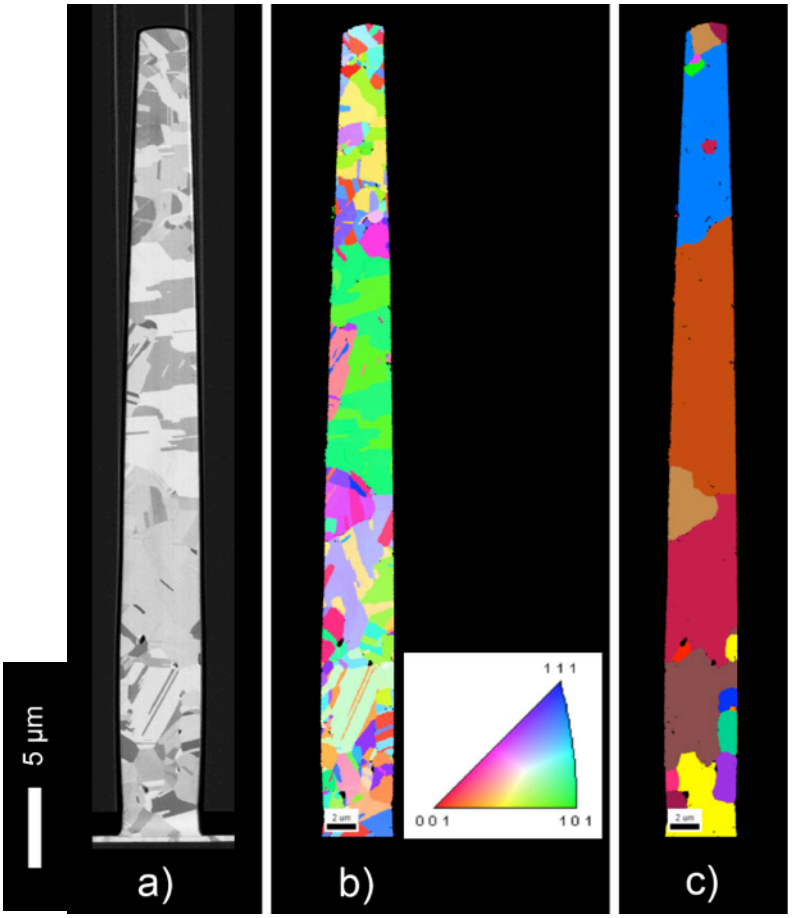

Figure 4.11: Examples of the EBSD maps used to study TSVs: a) FIB image, b) IPF map, c) grain size map after twin refining. The small scale bars at the bottom of each map are 2 µm, but a more legible scale bar is shown on the right side of the figure.

Inverse pole figure (IPF) maps use color to show grain orientations. The legend in Figures 4.12 and 4.13, as in 4.11b indicate which colors were attributed to the different crystallographic orientations. As can be seen in these two figures, none of the TSVs evaluated showed signs of preferential crystallographic grain orientation. The grains are randomly oriented in all regions of the TSVs.

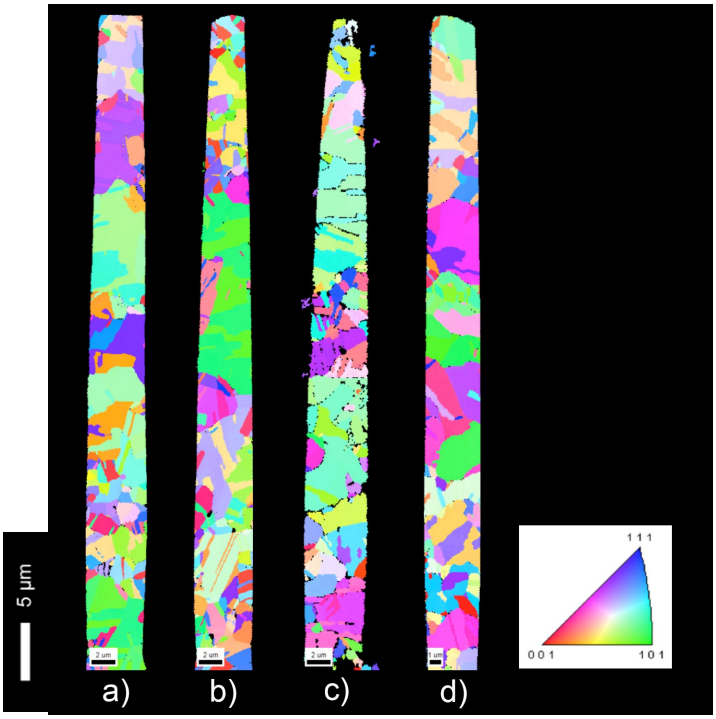

Figure 4.12: Normal direction inverse pole figure maps of the non-voided 2000 cycled, a) as-received, b) 100 °C, c) 150 °C, d) 200 °C, TSVs. No preferential grain orientation is apparent.

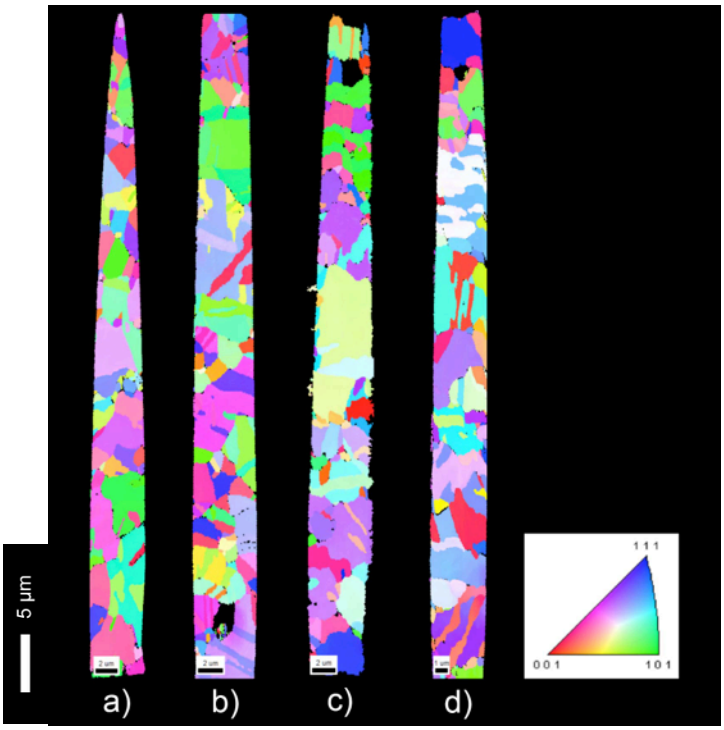

Figure 4.13: Normal direction inverse pole figure maps of the voided 2000 cycled, a) as-received, b) 100 °C, c) 150 °C, d) 200 °C, TSVs. The Cu-TSVs are randomly oriented.

After refining the maps to eliminate twin boundaries, mapping, like those seen in Figures 4.14 and 4.15, made it easy to calculate other microstructural aspects, such as grain size and aspect ratio. Although the colors have no significance in these figures, they make grains far more distinguishable than when observed with traditional optical microscopy.

Figure 4.14 and 4.15 depict data from measurements of vias from each maximum cycling temperature after 2000 cycles for the voided and non-voided samples. Grain sizes are relatively large, many spanning the width of the TSVs. Grain size measurements were conducted manually by averaging the longest length of the grains and the width perpendicular to the longest direction. The average grain size measurements of the TSVs exposed to different maximum cycling temperatures is shown in Figure 4.16. There is no apparent difference between the grain size of the sample types. The non-voided samples show no strong correlation between maximum cycling temperature and average grain size. On the other hand, the voided samples display a slight increase in grain size from 2.19 μm and 3.74 μm as maximum cycling temperature increases from 100 °C to 200 °C.

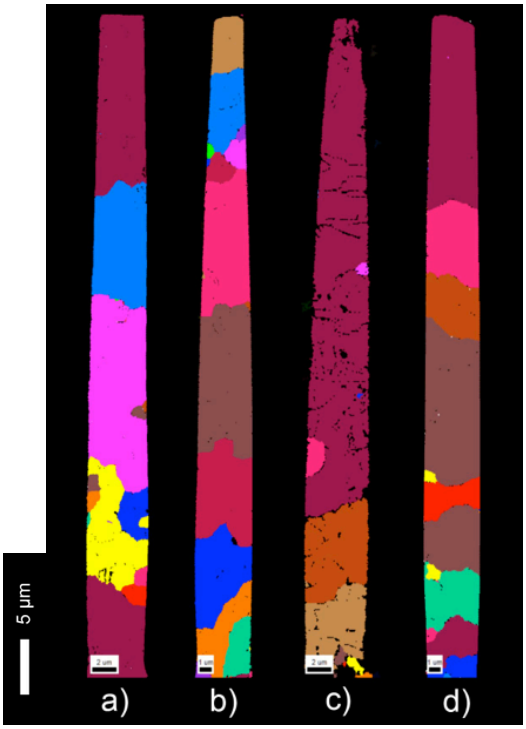

Figure 4.14: Grain size maps of the non-voided 2000 cycled, a) as-received, b) 100 °C, c) 150 °C, d) 200 °C, TSVs after twin refining. No significant changes in grain size or shape.

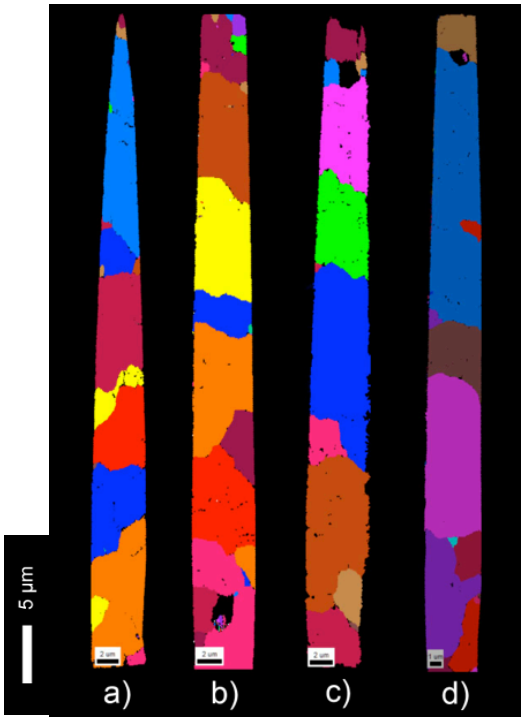

Figure 4.15: Grain size maps of the voided 2000 cycled, a) as-received, b) 100 °C, c) 150 °C, d) 200 °C, TSVs after twin refining. No significant changes in grain size or shape.

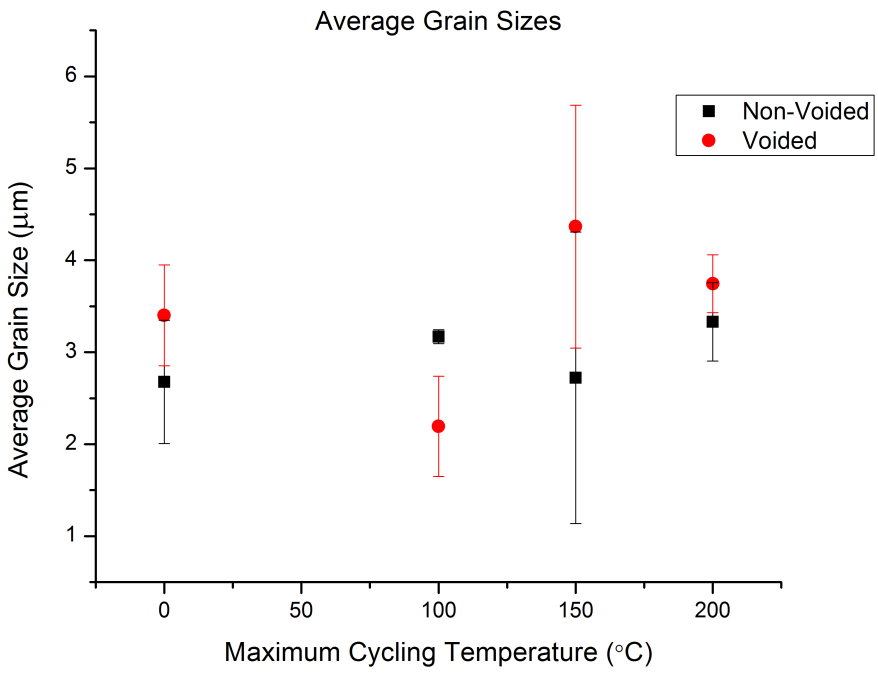

Figure 4.16: Graph of the average grain size changes due to the maximum cycling temperature for the 2000 cycled samples. The grain size does not appear to change with cycling temperature.

The grain sizes were also measured individually for each of the three regions (top, middle, and bottom) of each TSV. The average grain sizes for each region of the non-voided and voided samples are shown in Figure 4.17 and 4.18 respectively. Again, data was averaged over at least three vias from each of the wafers. While no difference can be seen between regions of the non-voided samples, the as-received and 2000 cycled 100 °C max cycling temperature voided samples have smaller grain sizes in the bottom of the TSVs compared to the middle region of the via length.

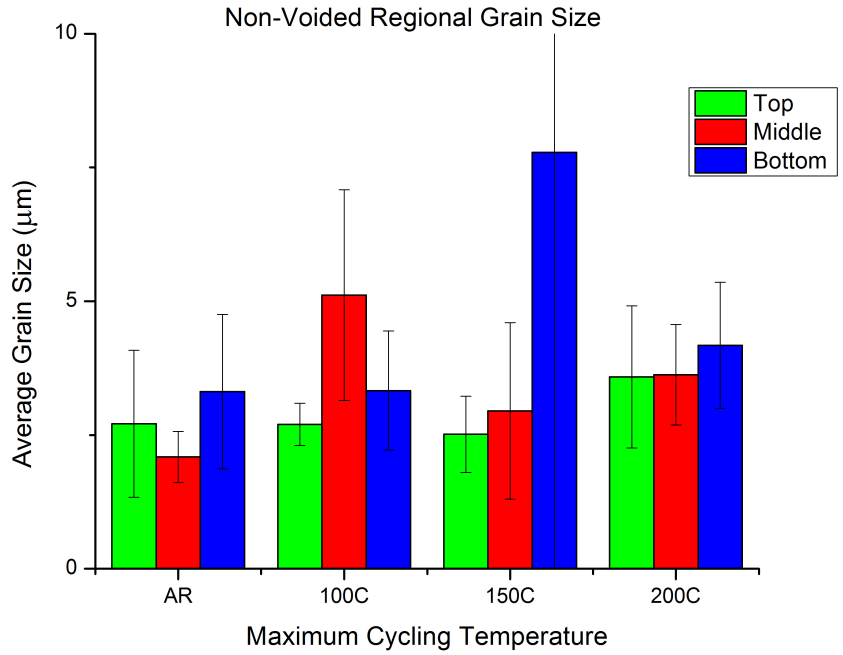

Figure 4.17: Average regional grain sizes of the non-voided samples, where there is no discernable difference between regions.

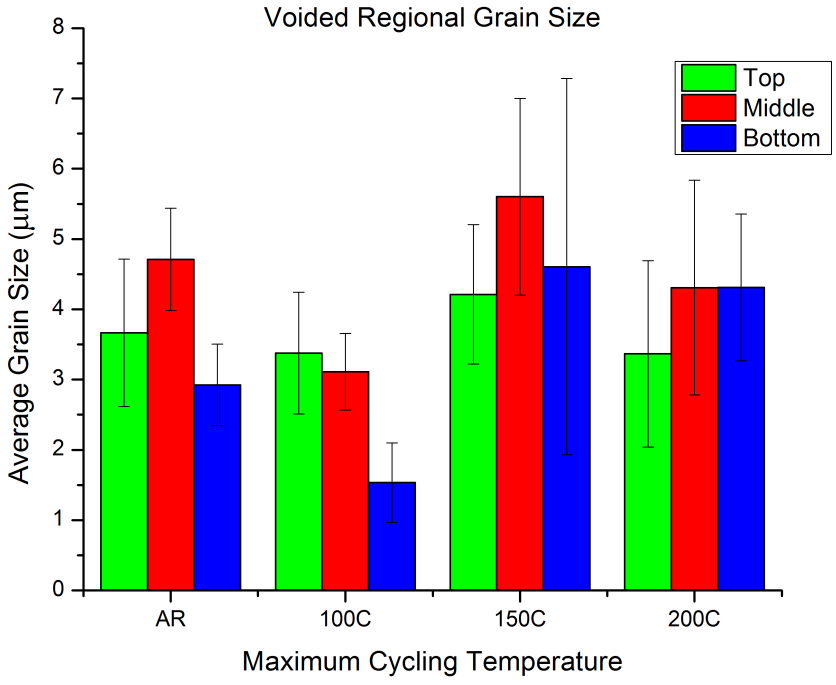

Figure 4.18: The average regional grain sizes of the voided samples, where the grain size of the bottom region is shown to be smaller than the middle region some samples.

For further investigation into the grain size measurements, the grain size distribution was calculated for the as-received and thermally cycled samples. The grain size distribution curves for the cycled samples can be found in Appendix B, where the distribution did not appear to change as the samples were cycled. However, Figure 4.19 shows the non-voided samples have a much sharper distribution at smaller grain sizes than the voided samples.

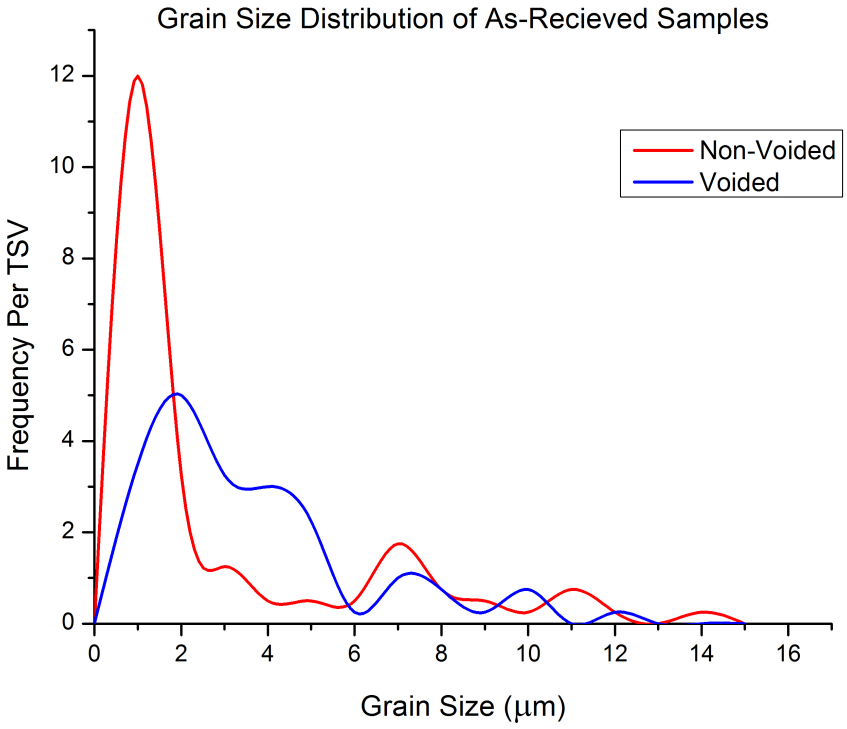

Figure 4.19: Grain size distribution of the Cu-TSVs for the as-received samples, which shows the voided samples have a broader distribution than the non-voided samples.

The aspect ratio of the grains was also measured by dividing the longest length by the width of each grain. Table 4.1 includes the average aspect ratio for

the TSVs under the different cycling conditions. Aspect ratio does not change significantly as maximum cycling temperature increases for either sample type. The aspect ratios of the voided and non-voided samples lie within their error so no difference can be concluded between the two sample types.

Table 4.1: Average grain aspect ratio of the as-received, 2000 cycled non-voided and voided samples. There is no indication that the aspect ratio changes with cycling.

Max Cycling Temperature (°C)	As-Received	100	150	200
Non-Voided	2.4 ± 0.1	2.3 ± 0.2	2.4 ± 0.3	2.4 ± 0.2
Voided	2.7± 0.03	2.5 ± 0.2	2.5 ± 0.7	2.5 ± 0.1

CHAPTER FIVE

DISCUSSION OF RESULTS

Now that the findings have been gathered and revealed in Chapter Four, we can discuss the changes in the Cu-TSVs studied under the different thermal cycling treatments. The cross-sectioning method developed enabled a deeper look into the defect and microstructural transformations occurring.

5.1 As-Received Sample Characterization

The optical image of the sample surface from Figure 4.1 is consistent in both voided and non-voided samples. Both substrates appear the same from the exterior. They all contain two rows of twelve bond pads, with each bond pad having an array of six by six, a total of 36, TSVs. The shape of the TSVs from the cross-section is shown in Figure 4.2. Each TSV is unique since fabrication processes can only be fine-tuned to a certain point. Also apparent from Figure 4.2 is the difference in void type and size between the two sample types. Voided samples contain seams, large bottom voids, and microvoids. Seams and bottom voids are typically due to non-optimal fabrication conditions. Both void types form from the trapping of air during electroplating, so these voids are most likely fabrication induced. The non-voided samples contain smaller microvoids, which could also be processing related, but may also have to do with heat treatments

after the TSVs were filled. Inconsistencies during electroplating could be creating these differences shown in Figure 4.2. It has been speculated that the age of the bath played a role in void formation in the voided samples.

In summary, the TSVs in both as-received sample types contain voids. The voided samples comprise of seams, bottom voids, and microvoids, while the non-voided samples only contain microvoids. These seams and bottom voids in the voided samples are much larger than those found in the non-voided samples. The fabrication processes and subsequent thermal treatments from the manufacturer created these voids.

5.2 Cross-Sectioning Methodology

The key element in producing the high quality electron backscattering diffraction (EBSD) results shown was to create smooth focus ion beam milled surfaces. Diamond particles becoming embedded in the copper of the TSVs, as seen in Figure 4.3, created rough cross-sections after ion milling. The reason for this finding is that, being hard, diamond is milled much slower than the soft copper; thus differential milling rates from the top surface down produces trails below the diamond particles. Since the samples are being milled from the top down, the first area exposed to the ion beam during milling is the cover glass on the sample's top surface. If the cover glass is too thick, the ion beam will create an uneven cross-section. As the ion beam mills deeper into a sample, the

focused beam becomes more spread out and give these unwanted results. To prevent this, the cover glass is ground down as thin as possible. Furthermore, if the grit paper used to grind down the cover glass is too rough, the uneven top surface of the sample can cause the ion beam to generate an uneven cross-section. The samples were also cleaned with ethanol to prevent dust or dirt from hindering the FIB. Since voids are pockets of air, they can act as uneven surfaces as well. Samples containing large voids were found to be difficult to achieve high quality EBSD. Like Figure 4.4, the EBSD quality of the cross-section usually diminishes below voids as the milling from FIB becomes uneven. It has been shown that when the protocol developed and discussed in section 3.2.1.2 was used to cross-section these Cu-TSVs, high quality EBSD maps suitable for via microstructural analysis, were obtained.

5.3 RF Measurements - Signal Integrity of the Cu-TSVs

As seen in Figure 4.5, the shape of the S_{11} parameter curves remain consistent in shape with frequency, as thermal cycling is performed. This is also true for all sample types and maximum cycling temperatures. Thus, the RF signal propagates similarly in these TSVs over the 700 MHz to 40 GHz range, regardless of pre-existing voids and thermal treatment.

Samples containing voided TSVs were shown, in Figure 4.6, to have a worse S_{11} parameter than non-voided TSVs. Smaller S_{11} parameters means a

smaller percentage of the incident wave is being detected, thus more losses are seen. Higher signal loss due to voids is expected and has been found in other studies, since voids can act as scattering centers [1]. Increased signal losses are also observed when the maximum cycling temperature is increased for the TSVs, which doesn't contain pre-existing voids, the non-voided samples. This is not true for the voided samples. It is possible that voids or other defects are nucleating and growing in the non-voided samples. This will be discussed later in this chapter. It is proposed that stress could be building up in the non-voided TSVs, but not the voided TSVs, due to their pre-existing voids. Through void formation, stresses can be relieved. Lastly, the number of thermal cycles appears to have no affect on amount of RF signal loss in the TSVs, suggesting there are minimal effects on the via system after the first cycle they experience.

A variance component chart was constructed to reveal which cycling parameters affect the S_{11} parameter the most. Table 5.1 presents these statistical measurements from Figure 4.6. The visual findings from Figure 4.6 are confirmed as sample type in conjunction with temperature is shown to have the most influence on the S_{11} parameter at 47.4%. As previously stated, the S_{11} parameter also appears to be reliant on the sample type at 22.4% dependence, however is not affected by the number of cycles. These findings mold the remaining studies in this thesis. Since no change in signal loss was found from cycling number, further investigation into the defects and microstructure of the

TSVs were only conducted on the as-received and 2000 cycled samples for the three maximum cycling temperatures and both sample types.

Table 5.1: Variance component chart, which shows the amount of influence each component has on the S_{11} parameter. The sample type in conjunction with temperature is shown to be the most influential factors.

Component	Var Component	% of Total	20406080	Sqrt(Var Comp)
Sample Type	0.00459229	22.4		0.06777
Temperature (C)	0.00263356	12.9		0.05132
Sample Type*Temperature (C)	0.00971283	47.4		0.09855
# of Cycles	0.00000000	0.0		0.00000
Sample Type*# of Cycles	0.00000000	0.0		0.00000
Temperature (C)*# of Cycles	0.00000000	0.0		0.00000
Sample Type*Temperature (C)*# of Cycles	0.00000000	0.0		0.00000
Within	0.00354739	17.3		0.05956
Total	0.02048608	100.0		0.14313

The S_{11} parameter was measured to determine how thermal cycling affected radio frequency signal losses in the TSVs. The signal integrity was found to be influenced the most by the sample type and maximum cycling temperature, but not by the number of cycles. More signal losses were recorded in the samples containing larger voids, which act as scattering centers for signal propagation. Higher maximum cycling temperatures were also found to increase the amount of signal loss in the samples in the non-voided samples, but not in the voided samples. It is proposed that the stress buildup from higher temperatures causes more voids to form or pre-existing voids to grow in the non-voided samples. The large voids in the voided samples may serve to relieve the

stresses caused by the thermal cycling.

5.4 Void and Other Defect Evolution in Cu-TSVs

SEM and FIB imaging were used to evaluate the TSV cross-sections to find defects before and after thermal cycling was conducted. Section 5.1 discussed that fabrication-induced voids were found in both sample types. The voided samples contained seams at the top, large voids at the bottom, and micro-voids dispersed throughout the top and middle of the TSVs. The non-voided samples typically consisted of microvoids, which were less than 0.5 μm. Most voids observed in these Cu-TSVs were located along grain boundaries as shown in Figure 4.7. The high stresses from the misorientation of the anisotropic Cu grains along with vacancy diffusion in the grain boundaries, makes these areas prone to void nucleation and growth.

The average area of the voids is displayed in Figure 4.8. As expected, there are larger areas consumed by voids in the TSVs of the voided samples compared to the non-voided TSVs, due to the large processing-induced voids, like seams and bottom voids. As mentioned earlier these processing induced defects are most likely due to the age of the bath used for the electrodeposition of the Cu. To alleviate the stresses caused by the mismatch in CTE between the Cu and Si, new voids appear to be formed or pre-existing voids grow, thus yielding an increase in void area as seen as higher maximum cycling

temperatures are performed. While both sample types exhibit this behavior, the voided samples have much more experimental error. Since the seams and bottom voids are rarely in the same plane, it is difficult to cross-section through both simultaneously, affecting the measured void area. The lack of void size growth with maximum cycling temperature as shown in Figure 4.9, indicates that the cause of larger void areas is most likely due to new voids forming as opposed to pre-existing void growth. The void area data correlates well with the non-voided S_{11} measurements. Increasing the cycling maximum temperature causes more voids to form acting as scattering centers, which increases the RF signal loss. There may be a point at which larger void area has little impact on signal loss, baring the voids do not span the entire width of the TSVs. The voided samples may have surpassed this point.

The defects shown in Figure 4.10, like grain boundaries, indicate the areas of the TSV structure that are susceptible to high stresses, such as interfaces between differing materials or parts. Additionally, no defects were visible in the isolation liner or barrier layer of the TSVs from the SEM and FIB micrographs used. This along with stable TSV dimensions signify that stresses did not reach a level in the system large enough to cause cracking of the isolation liner or deformation of the TSV structure.

In summary, voided samples were found to contain seams, bottom voids, and microvoids, while non-voided samples solely contain microvoids. These pre-

cycled samples demonstrate a plausible reason for higher signal loss in voided samples over the non-voided samples. Lastly, voids are forming during cycling, causing further RF signal loss.

5.5 Microstructural Evolution of Cu-TSVs

The Cu-TSVs in both sample types exhibited no signs of preferential orientation by both looking at the IPF maps in Figures 4.12 and 4.13. No effects on orientation were found due to the thermo-mechanical stresses from thermal cycling. Similar findings have been published for isothermally held heat treatments of Cu-TSVs, where random orientations were also recognized [2-4]. Although Cu has a face centered cubic (FCC) structure, which is anisotropic, the random orientation found within the Cu of the TSVs gives the TSVs isotropic properties, overall. On the other hand, it creates local stresses from the many Cu grain misorientations.

Grain boundaries are defects in the microstructure, consisting of atoms that don't belong to either of the adjacent crystal lattices. To lower the overall system energy, the system wants to reduce these boundaries. The heating that occurs during thermal cycling is expected to activate grain boundary migration in the Cu, increasing the grain size in the process. There is no evidence that grain growth is occurring either sample type under any cycling conditions tested. Differences in electro-deposition chemistry could play a role in the magnitude of

grain growth, as this has been shown to affect how grains grow in previous studies [5]. While grain growth has been found to occur in Cu-TSVs, most of the thermal treatments used had maximum temperatures of at least 300 °C and were either isothermally held or long-interval thermal cycling [2-5]. The higher temperatures used make it more likely for grain boundary migration to be activated. Furthermore, the time at elevated temperatures was much longer in those studies compared this study, where the duration of a single 150 °C cycle is approximately 5 minutes. The short duration of cycling allows only minimal diffusion to occur. From Figure 4.16, the average grain size is shown to increase in the voided samples with an increase in maximum cycling temperature from 100 °C to 200 °C. Higher temperature not only translates to more energy for boundary movement, but also longer times at elevated temperatures, since a single 100 °C cycle takes about three and a half minutes compared to the seven minutes of a 200 °C cycle. As stated before, the longer the TSVs are exposed to high temperatures, the more time there is for diffusion to occur. Average grain size is significant because of the grain boundary's detrimental effects on the signal. Larger grain sizes lessen grain boundary area, reducing the amount of defects the RF signal needs to pass through.

The average grain size was then calculated for top, middle, and bottom regions of the TSVs in Figures 4.17 and 4.18 to determine if grains were growing in specific regions. Past work has found that the middle of the TSVs typically

contain larger grain sizes than the top and bottom of the vias [2,6]. Additives hinder grains from growing in the top region of Cu-TSVs [6]. The grain sizes of the non-voided samples used in this study appear to be distributed evenly across all three regions. Neither sample type shows grain growth in any particular region after cycling, however the TSVs in the voided sample show smaller grain sizes in the bottom of the TSV than in the top and middle regions. A majority of the cross-sections examined for the voided samples only contained the bottom void instead of the seams. Not only is there less Cu area in the regions where large voids are present, but smaller grains appear to surround the large voids, as illustrated in Figure 4.15c, giving the region a lower average grain size.

The grain size distributions were conducted to determine if the average grain size measurements accurately depicted the lack of Cu grain growth seen in these TSVs. Figure 4.19 shows that most of the grains in the non-voided samples lie below 3 μm, while the voided sample has a wider distribution, with a majority of its grains being less than 5 μm. This is reflected in the average grain size measurements, where the voided samples were found to have a larger grain size than the non-voided samples.

The grain size maps in Figures 4.14 and 4.15 also show that grains typically span the width of the TSVs. This can make grain shape an important factor in characterizing the microstructure of these TSVs. The grain shape was found by measuring the aspect ratio of the grains. The aspect ratio is the longest

length of the grain divided by the width of the grain. Since the width is basically fixed for a majority of the grains, grain aspect ratios, like the average grain size, can show how many grain boundaries an RF signal must penetrate when travelling through a TSV. The ideal microstructure of a TSV would consist of a single grain, eliminating the defects that make up grain boundaries. Thus, larger aspect ratios are desired. There appears to be no difference in average grain aspect ratio between the voided and non-voided samples as indicated by Table 4.1. The grain shape of the copper, also, does not appear to be influenced by thermal cycling to any of the maximum temperatures. This is indicative of the grain growth as well, since grains are constrained between the sidewalls of the TSVs.

Minor differences between the microstructure of the non-voided and voided TSVs were observed. The average grain size in non-voided and voided samples do not appear to be affected by cycling. There is also no distinguishable difference between the average grain aspect ratios of the voided and non-voided TSVs. Since the maximum cycling temperature has little to no influence on the non-voided TSVs' microstructure, the microstructure is not significantly contributing to the variation that is occurring in the S_{11} parameter. Instead, results from the void analysis in earlier sections indicated that defects have a large impact in the degrading RF signal integrity.

5.6 References

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CHAPTER SIX

CONCLUSIONS AND FUTURE WORK

The recent slowing of Moore's law has propelled the semiconductor industry to find new ways to increase integrated circuit performance. With the stacking of chips to make 3D-ICs, these demands can be met. Since the performance-limiting factor has shifted from transistors to interconnects, much emphasis has been put into this area. Through-silicon vias provide the pathway for these stacked chips to communicate. TSVs are vertical interconnects, typically made of copper that penetrate through the silicon substrate. A major concern for these structures is their thermo-mechanical reliability. Since copper has a coefficient of thermal expansion about eight times that of silicon, heating that occurs during chip use and fabrication causes stresses to build in the system. These stresses have been found to cause failures in the system through copper out-of-plane expansion and defect formation in the TSVs.

The goal of this thesis was to study the changes that occur in Cu-TSVs as they undergo thermal cycling similar to what the chips would see over their lifetime. Two sample types were observed, one containing TSVs with large fabrication-induced defects and the other with minimal defects. This allowed for defect formation and their evolution to be observed. Also, it enabled the study on signal loss due to these defects. Samples underwent thermal cycling from room

temperature to an established varied maximum temperature and the TSVs were studied to with the following goals in mind:

1. Evaluate the S_{11} parameter to determine the signal integrity of commercially-prepared Cu-TSVs from simulated use conditions, such as maximum cycling temperature and the amount of thermal cycling.
2. Develop a method for examining the microstructure and defects within the multilayered Cu-TSVs.
3. Identify the pre-existing defects in the TSVs of the two commercially manufactured wafers and how these defects form and evolve with thermal cycling.
4. Quantify the difference in Cu microstructure of the two wafer type TSVs as well as how this microstructure evolves due to thermal cycling.
5. Correlate the performance variation of the Cu-TSVs to the internal aspects of the TSVs, such as defect and microstructure changes.

6.1 Conclusion

Two sample types, voided and non-voided, were used in this study and contained two rows of twelve bond pads on their surface. Underneath each bond pad was an array of 36 blind Cu-TSVs. The TSVs were cylindrically shaped with

a slight taper, approximately 50 μm tall, and 5.5 μm in diameter. The TSVs in both as-received sample types contain voids. The voided samples comprise of seams and bottom voids, while the non-voided samples have microvoids, which are less than 1 μm in diameter. These voids in the voided samples are much larger than those found in the non-voided samples. The formation of these voids is most likely due to the fabrication processes and subsequent thermal treatments the TSVs underwent.

To complete the research objectives, a protocol for thermal cycling was, first, developed to accurately simulate the heat treatments these TSVs might be exposed to in the real world. Three different maximum cycling temperatures, 100 °C, 150 °C, and 200 °C, were established. Both sample types were exposed to the three maximum cycling temperatures up to 2000 cycles in 500 cycle intervals. After each cycling interval, the same four samples for each sample type and max cycling temperature were electromagnetically measured for signal integrity. A radio frequency vector network analyzer was used to measure the S_{11} parameter and determine the amount of signal loss present in the TSVs. Following the cycling, a method was developed to cross-section the TSVs for defect and microstructural analysis. Scanning electron microscopes (SEM) and focused ion beam (FIB) imaging were used to evaluate the TSV cross-sections for voids within the copper and other defects within the TSVs. The microstructure of the Cu within the TSVs was then evaluated using electron backscattering diffraction

(EBSD). The average grain size, grain aspect ratio, and amount of high angle grain boundaries (HAGB) were found using EBSD. The following results were found:

- Based on the S_{11} parameter, the signal integrity of the TSVs is mostly influenced by a combination of the sample type and maximum cycling temperature, but not by the number of cycles.
- TSVs containing less pre-existing voids, had less signal loss than those with larger amounts of voids, and increased in signal loss as the maximum cycling temperature was increased.
- To conduct defect and microstructural analysis on the TSVs' interior, a protocol for cross-sectioning the TSVs, which includes polishing and FIB milling of the wafers, was successfully developed.
- One sample type was found to contain TSVs with seams and large bottom voids, while the other sample set had TSVs with microvoids, which typically had a diameter less than 1 μm. These voids were most likely formed due to the processing steps of the substrates.
- Void area increased with maximum cycling temperature for both sample types and is thought to be caused by the formation of new voids.
- No microstructural differences were found in the Cu-TSVs of either

sample type and from thermal cycling. The grain sizes in both samples remained approximately 3 μm, showing limited diffusion took place. Preferential orientation was not found in the TSVs as well.

- The microstructure was found to have little to no influence on the signal integrity of the TSVs, however the void area was found to correlate with signal loss.

6.2 Future Work

Now that a method has been developed for examining the microstructure and defects within Cu-TSVs, the process can be developed further to more accurately measure these structures. By focusing on one TSV at a time, layers of a TSV can be cross-sectioned and composited to form a 3D microstructural and defect model containing all the grains and defects within a single TSV. Furthermore, the following future works can be pursued:

- Vary the cycling conditions further to determine the mechanisms behind microstructural and void evolution
- Utilize modeling results with experimental findings to refine and help understand these mechanisms
- Correlate these mechanisms with stresses in the system by using finite element modeling (FEM) and x-ray diffraction (XRD)

APPENDICES

Appendix A:

Sample Organization

Table A1: The number of samples used for the different procedures conducted in this study separated by sample type and maximum thermal cycling temperature.

Sample		Cycling Condition		Processes	Notes
Type	Name	Max Temp.	# of Cycles		
Non-Voided	2-8	100	0 500 1000 1500 2000	RF Signal Integrity Measurements	Measurements were conducted on each sample after every cycling interval up to 2000 cycles.
	7-6				
	1-5				
	4-7				
	9-3	150			
	6-4				
	3-1				
	9-0				
	4-1	200			
	4-4				
	7-3				
	8-0				
	C6	N/A	0	Cross-Sectioned, Void Analysis, and Microstructure Analysis	This was an as-received sample and did not undergo cycling.
	2-3	100	2000		One sample from each maximum cycling temperature were characterized after 2000 cycles.
	4-3	150			
	9-4	200			
Voided	4/-4	100	0 500 1000 1500 2000	RF Signal Integrity Measurements	Measurements were conducted on each sample after every cycling interval up to 2000 cycles.
	7/-4				
	2/-5				
	5/-5				
	7/-2	150			
	2/-3				
	5/-2				
	3/-1				
	1/-4	200			
	7/-3				
	5/-1				
	9/0				
	8/-5	N/A	0	Cross-Sectioned, Void Analysis, and Microstructure Analysis	This was an as-received sample and did not undergo cycling.
	6/-4	100	2000		One sample from each maximum cycling temperature were characterized after 2000 cycles.
	4/-1	150			
	3/0	200			

Appendix B:

S_{11} Parameter Measurements

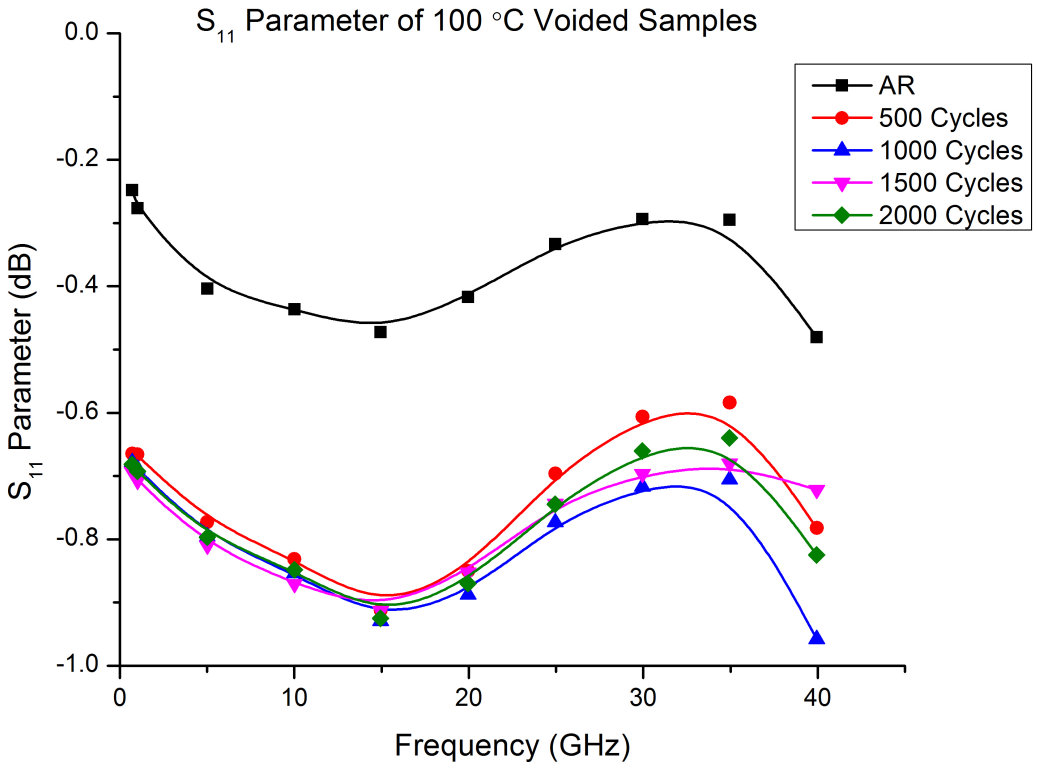

Figure B1: S_{11} parameter as a function of frequency for the voided samples as they underwent cycling with a maximum temperature of 100 °C.

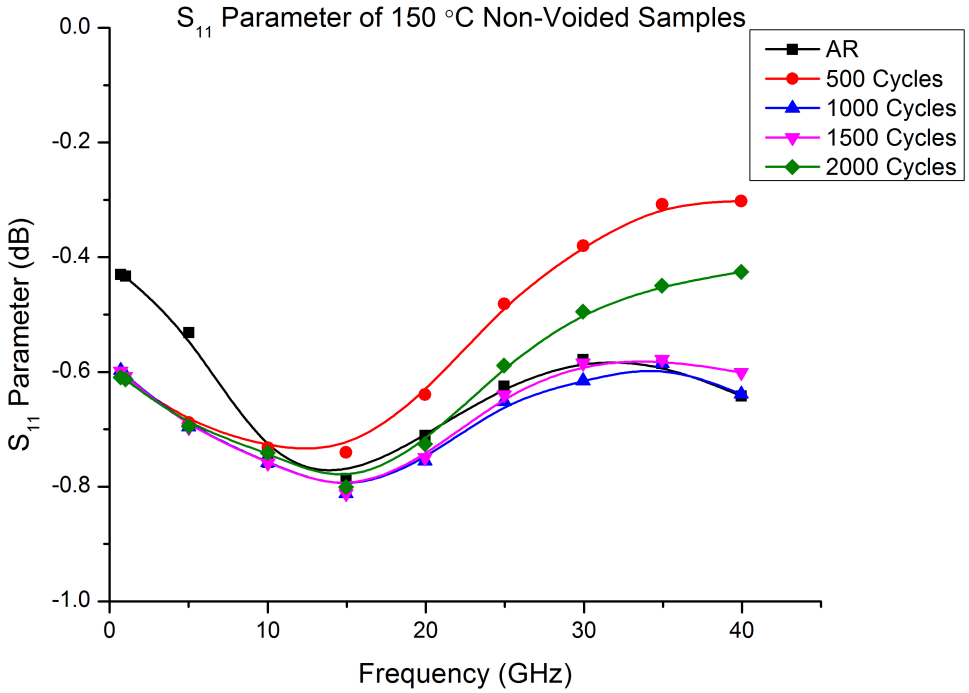

Figure B2: S_{11} parameter as a function of frequency for the non-voided samples as they underwent cycling with a maximum temperature of 150 °C.

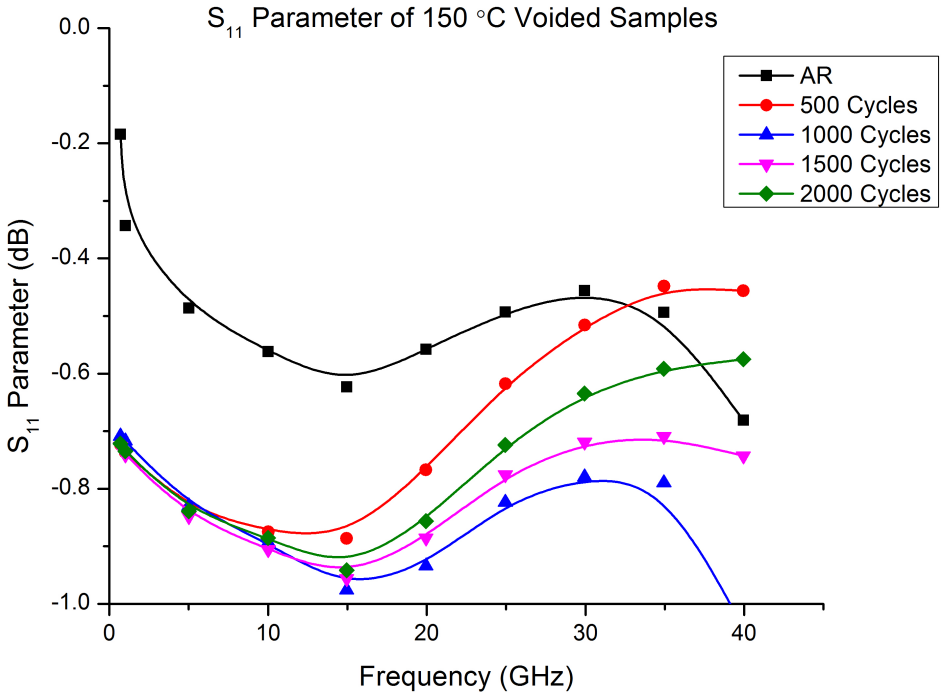

Figure B3: S_{11} parameter as a function of frequency for the voided samples as they underwent cycling with a maximum temperature of 150 °C.

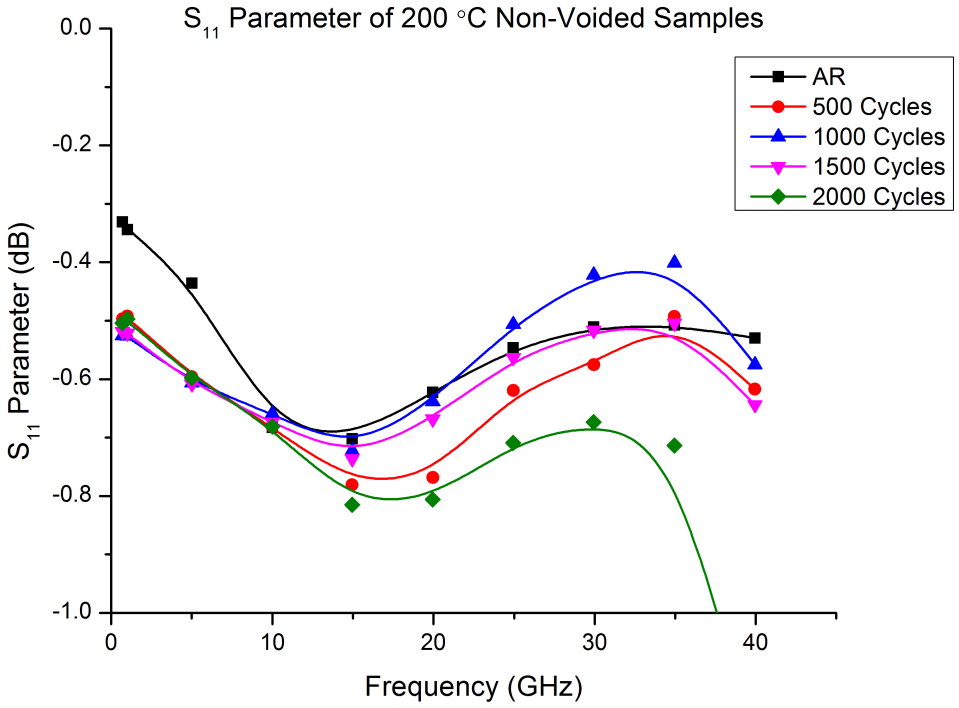

Figure B4: S_{11} parameter as a function of frequency for the non-voided samples as they underwent cycling with a maximum temperature of 200 °C.

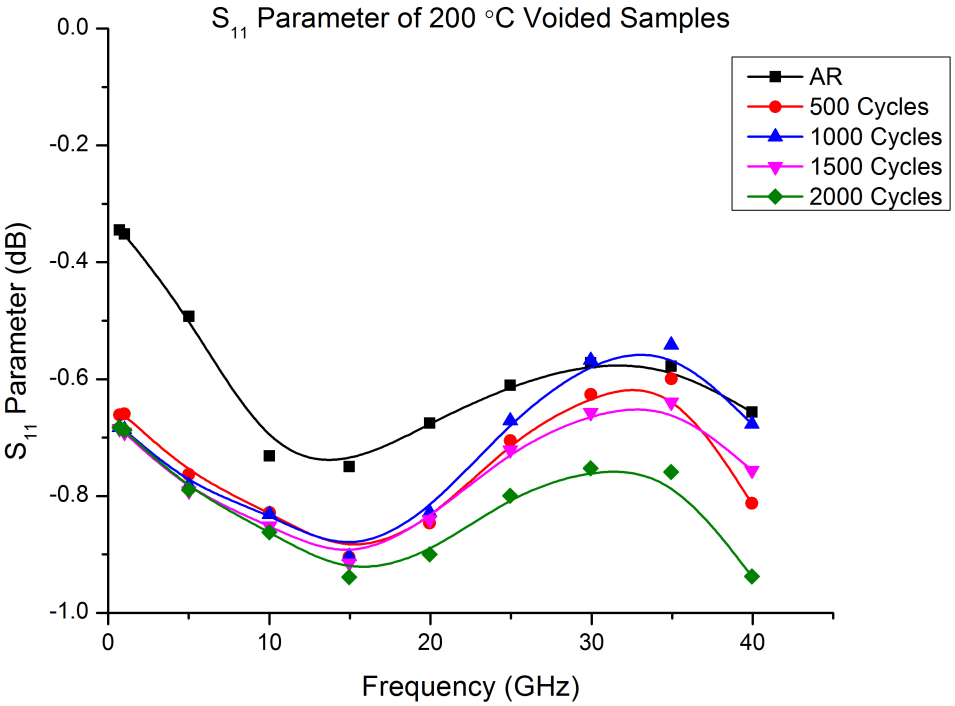

Figure B5: S_{11} parameter as a function of frequency for the voided samples as they underwent cycling with a maximum temperature of 200 °C.

Appendix C:

Grain Size Distribution by Sample

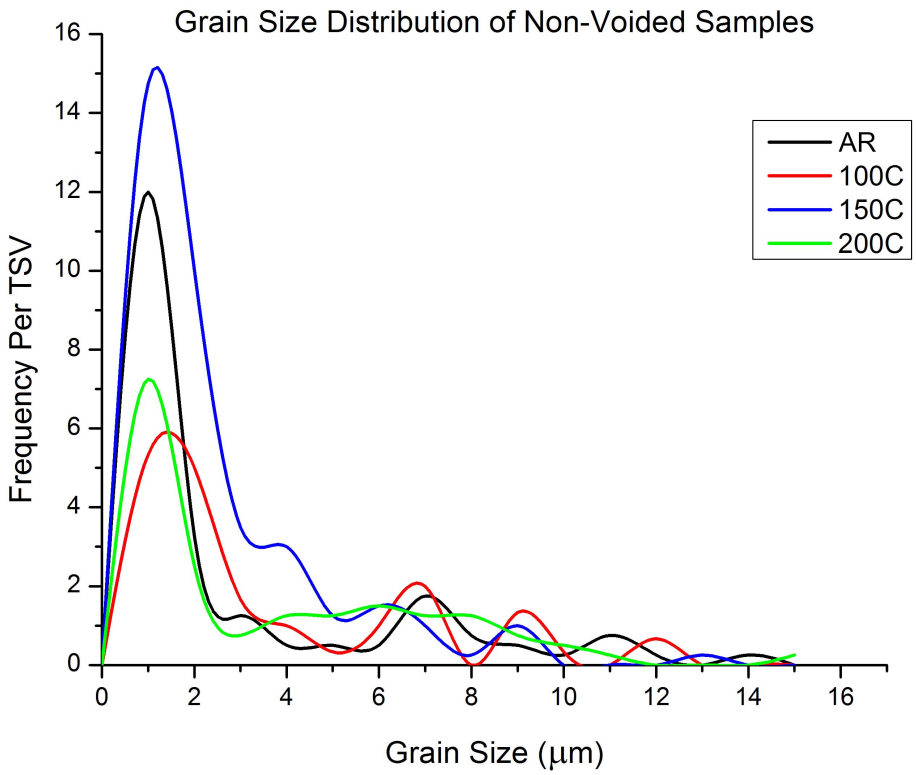

Figure C1: Grain size distribution of non-voided samples cycled with different maximum cycling temperatures.

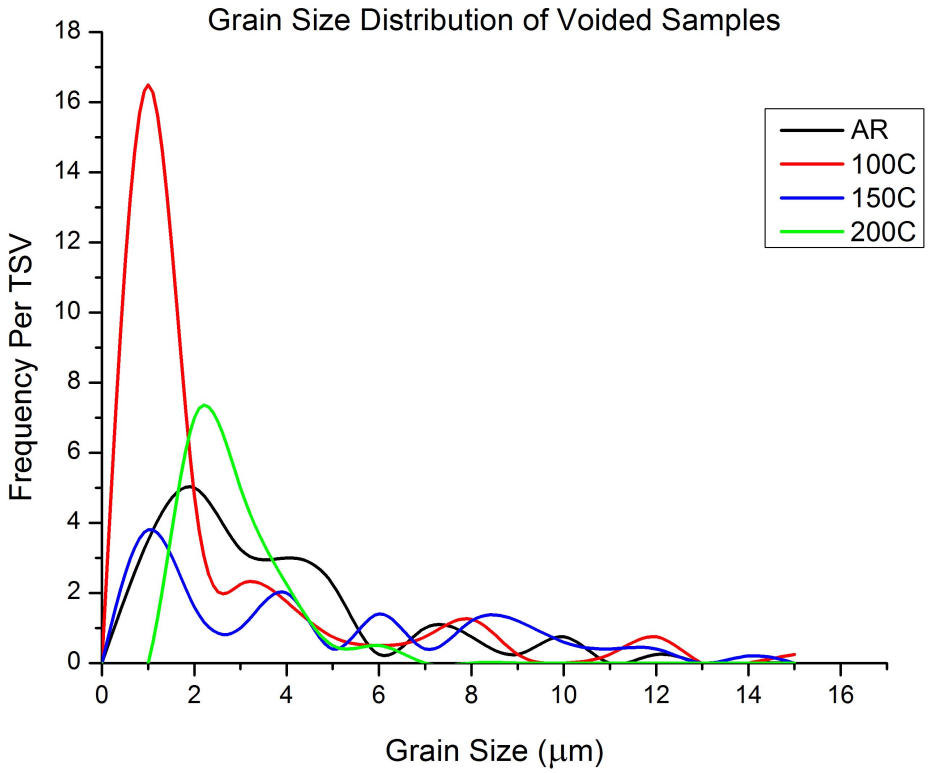

Figure C2: Grain size distribution of voided samples cycled with different maximum cycling temperatures.